October 12, 1970
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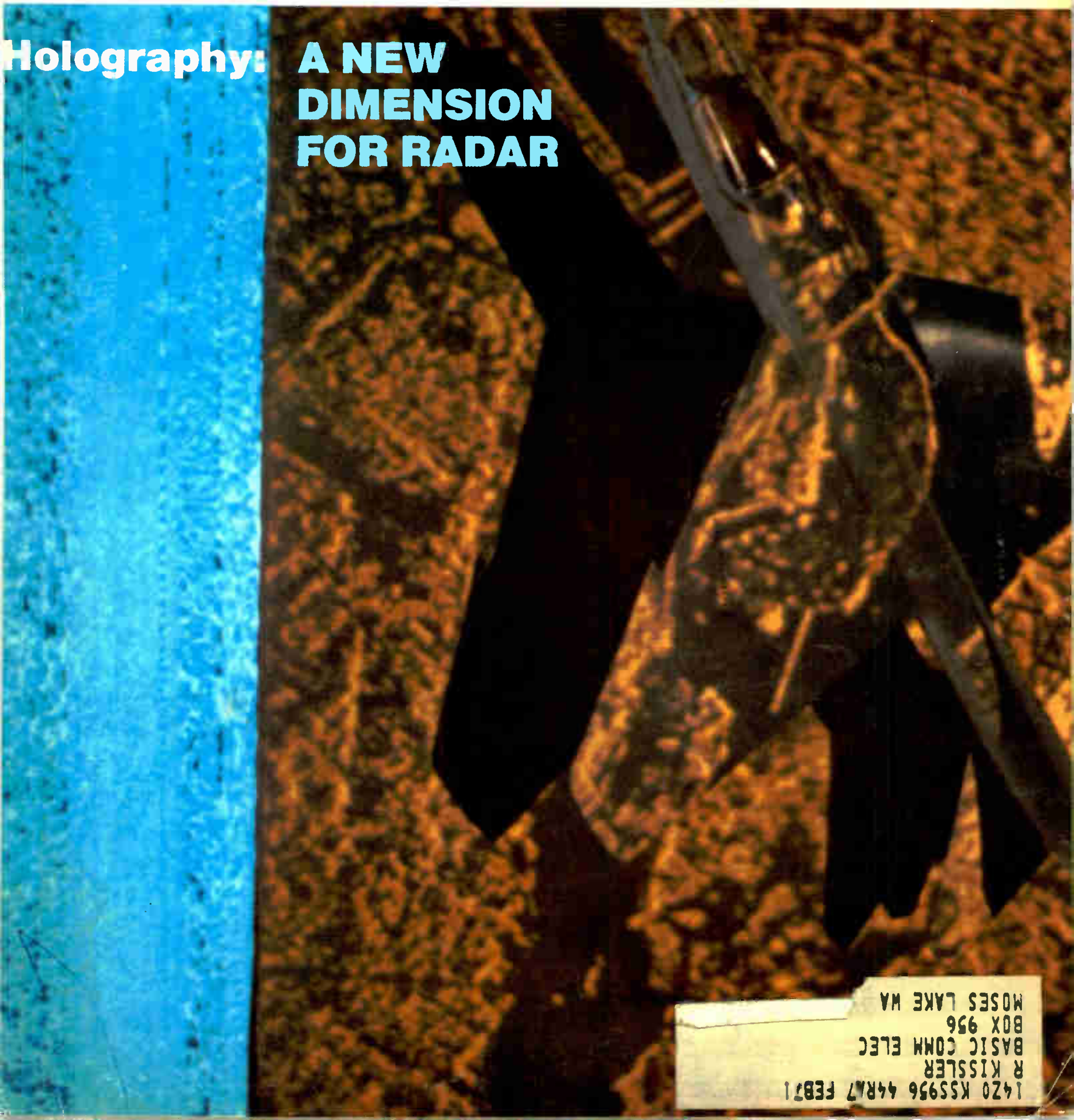
Electronics®

Holography: A NEW DIMENSION FOR RADAR



GR knocks down the price of Frequency Synthesizers!

Across-the-board price changes now offer you the chance to pick up just the synthesizer you need at the lowest prices ever!

GR's fully equipped synthesizers (including 7 programmable digits and a continuously adjustable decade) have been reduced by as much as 26%. For instance:

- The 1161 and 1162 Synthesizers, with respective frequency ranges of 0 to 100 kHz and 0 to 1 MHz, are now only $4990.
- The 1163, with 30-Hz to 12-MHz range, is reduced to $5290.
- The 1164 (10-kHz to 70-MHz range) is now $7195.

If you don't need fully equipped models, you can compound the savings by omitting some of the features. You can save $300 if you have no need for the continuously adjustable decade. Or you can order your synthesizer with as few as three digits – subtract $230 for each digit you leave out.

These are the same synthesizers you wanted before because of their specifications – now they're even better because economy has been added to quality! Even with the new lower prices you still get a room-temperature quartz-crystal oscillator with a temperature coefficient better than $2 \times 10^{-7}/^{\circ}C$, 200-$\mu$s switching time, rms phase-noise modulation as low as −70 dB, spurious signals down 60 dB and beyond, and compact size (only 5½ inches high)! It's a buyer's market!

If you're looking for performance up to 160 MHz without an oversized price tag, GR also has the 1165 Synthesizer for only $5900.

Complete pricing information and specifications are available from the General Radio District Office nearest you or from our home office at 300 Baker Ave., West Concord, Mass. 01781. In Europe write Postfach 124, CH 8034, Zurich, Switzerland.

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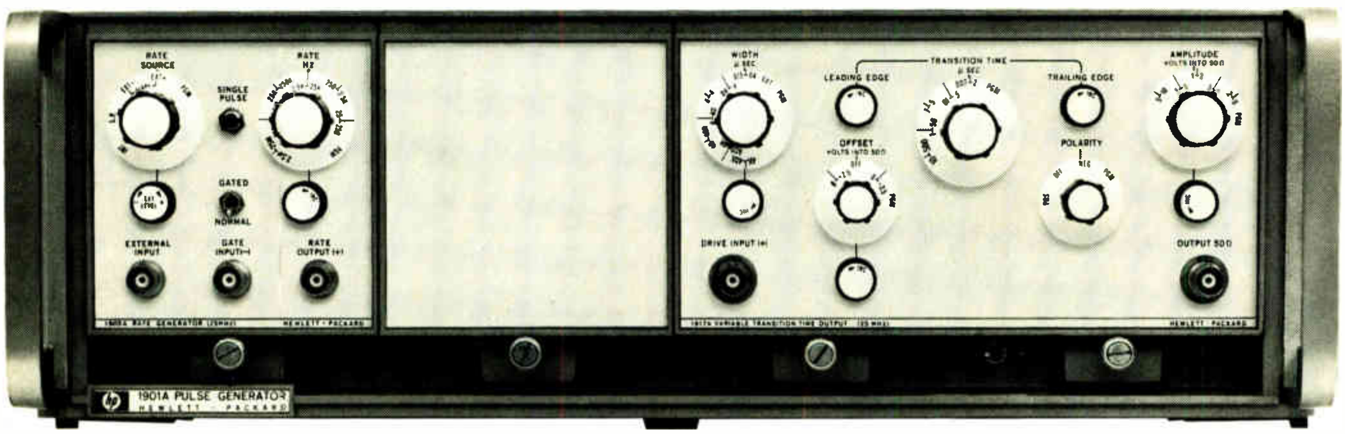
Circle 900 on reader service card

Today, fast, low-cost pulses with variable rise and fall —tomorrow, a system!



HP's new, all-solid-state 1900 Pulse System gives you the best of two worlds. **For only $1195, you can get a 7 ns variable rise and fall generator,** right away. Then, as your needs and/or funds increase, plug-in capability allows you to get additional features, without having to buy a whole new generator.

Our basic package consists of a rate generator, a pulse shaping output, and a mainframe.

The 1917A pulse shaping output provides 10 V pulses with variable rise and fall times as short as 7 ns, **reversible polarity, and dc offset.** It takes up only half of a mainframe, and can handle rep rates of up to 25 MHz. A unique external-width function allows the 1917A to be used as a **pulse amplifier,** also, maintaining width and spacing of externally-supplied pulse trains.

The 1905A Rate Generator ("clock") is a quarter-size plug-in. It provides output triggers at repetition rates from 25 Hz to 25 MHz in six decade ranges. Rep rate can be determined internally, by external triggering, or by single-pulse push-button. **Gating feature allows pulse bursts.**

The 1901A Mainframe is a standard rack size unit, and contains power supplies that can be used to power other 1900-series plug-ins. **Built-in EMI and RFI shielding are standard.**

Price of this three-part package (including a blank plug-in) is only $1195. As your needs change, available plug-ins include a 350 ps output, **a 16-bit (RZ, NRZ) word generator,** variable delay generators, fan-in and fan-out generators, and optional analog programming—plus a high power pulse-shaping output (1 A, 50Ω) and mainframe.

Call your local HP field office for ordering. For further information on the HP 1900 Pulse System, see pp. 254-261 in your 1970 HP catalog, or send for our new free brochure on pulse generators. Hewlett-Packard, Palo Alto, California 94304. In Europe: 1217 Meyrin-Geneva, Switzerland.

080/10

HEWLETT hp PACKARD

SIGNAL SOURCES

Circle 1 on reader service card

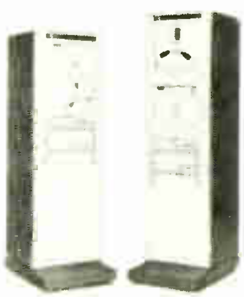
HP instrumentation recorders work with hours less downtime. How much is your time worth?

When you're putting instrumentation measurements on tape, the last role you want to play is maintenance man. And who can afford all those time-wasting adjustments? Hewlett-Packard's instrumentation recorders are so reliable they require up to five times less routine maintenance than most machines. Both the HP 3950/3955 Series Systems for lab use and the lightweight HP 3960 portable for the field have what it takes to make you more researcher and less caretaker.

You won't be plagued by misalignments that cause you slowdowns on other recorders. Tape transport components on all HP machines are mounted to a single, rugged cast-aluminum frame that's precision machined to assure permanent alignment. So you'll never have to make shimming or other adjustments in the field. You can use the time you gain for more rewarding work.

Both the IRIG-compatible lab models and 50-pound portable feature a simple, uncluttered tape path that lets you clean head assemblies in just seconds. Even mounting of tape reels and tape threading goes easier and faster with a snap-on reel hub assembly.

Whether you choose the interchangeable 7 or 14-track lab models or the economy 4-track portable, you'll have high-performance recorders that will sharply reduce your operating costs.



To that, add the initial low price that comes with HP quality electronics. If you want to see what these recorders can do, it's easy to set up. Your local HP field engineer will be happy to demonstrate the wide uses of these recorders in the medical, scientific and industrial fields. Call him. Or write Hewlett-Packard, Palo Alto, California 94304; Europe: 1217 Meyrin-Geneva, Switzerland.

HEWLETT hp PACKARD

MAGNETIC RECORDERS

42004

Circle 2 on reader service card

Electronics

Volume No. 43, Number 21 October 12, 1970

Features

Probing the News

Electronics Review

Electronics International

New Products

Articles

Departments

Electronics

About this issue

The temper of the times, when the Pentagon and nearly everyone in it are a target for society's critics, was evident to Washington bureau chief Ray Connolly inside the office of David Packard, Deputy Defense Secretary. Connolly saw Packard to cap a series of interviews aimed at assessing his impact on the military bureaucracy [page 117]. "The door that separates Packard's large inner office from that of his secretaries has two peepholes—one for Packard to look out and another for a secretary to look in," reports Connolly. "None of his predecessors had them; the door was usually open."

A second security measure counters the argument that the peepholes merely permit the founder of Hewlett-Packard Co. a bit more privacy in public life. It is the door-wide, carved and gilded wooden name-plaque identifying the office of the Deputy Secretary of Defense from other executives on the third floor of the Pentagon's "E" ring, facing the Potomac. The plaque is not on Packard's suite, but hangs over the door of an auxiliary office across the corridor staffed with support personnel. "Don't bother going in there," warned an information officer jokingly. "It's just a front."

With one exception, Connolly finds David Packard "the same soft-spoken, shirt-sleeved executive who ran Hewlett-Packard. The most noticeable change is that he now looks like everyone else who works at the top of government—tired. A Packard day probably consists of 12 to 16 hours work and four to six hours of sleep."

The orchid-fancying master detective, Nero Wolfe, for all his adventures, probably never carried on as diverse a batch of investigations as has fellow orchid grower, Winston E. Kock, author of the cover article. Radar holography is the latest field of study for the Bendix Corp.'s vice president and chief scientist. The subject is a natural outgrowth of his earlier work, just as were the two basic books he has written. "Sound Waves and Light", is already read in Italian, Russian, and Japanese, with German and French translations to come. And "Lasers and Holography" has Russian and Japanese editions.

With a Ph.D. from the University of Berlin and a flair for piano and organ playing, Kock, who hails from Cincinnati, started his career at the Baldwin Piano Co., where he developed the electronic organ. A 14-year stint at Bell Labs added microwave radar, underwater sound, speech transmission, and the Picturephone to his areas of investigation. After moving to Bendix, he took a two-year leave during which he was the first director of NASA's Electronic Research Center. He is also a trustee of the Argonne Universities Association, a director of several companies and a member of the American Orchid Society.

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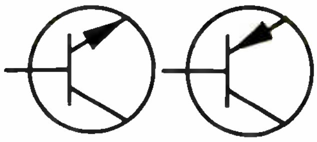

GOOD NUMBERS TO KNOW: 2N5381 2N5383

REPLACE OLD 2N3904 and 2N3906 PLASTIC TRANSISTORS AND GAIN 3 WAYS. 360 mW P_D vs 310. T_J (max) = 150°C vs 135. TO-18 PINNING.

These two new Sprague plastic transistors give you 20% more power dissipation, 15° C higher junction temperature, and industry standard TO-18 pinning when used as direct electrically interchangeable replacements for 2N3904 and 2N3906.

The 2N5381 and 2N5383 are two of twenty new TO-18 pinned plastic transistors from Sprague. Check the replacement chart, then make your move. Sprague industrial distributors have stock. The sales offices listed below can supply samples. Call them now. Or get complete specifications by writing Technical Literature Service, Sprague Electric Company, 35 Marshall Street, North Adams, Mass. 01247, or use the reader service number below.

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2N3903	2N5380	MPS6514	TPS6514
2N3904	2N5381	MPS6515	TPS6515
2N3905	2N5382	MPS6516	TPS6516
2N3906	2N5383	MPS6517	TPS6517
2N4123	TP4123	MPS6518	TPS6518
2N4124	TP4124	MPS6519	TPS6519
2N4125	TP4125	MPS6520	TPS6520
2N4126	TP4126	MPS6521	TPS6521
MPS6512	TPS6512	MPS6522	TPS6522
MPS6513	TPS6513	MPS6523	TPS6523

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Readers comment

Complementary squared

To the Editor: I read with great interest the article "Complementary MOS and bipolar make it together on a single chip" by Fred J. Link, Robert Cook, and Robert J. Lesniewski that appeared on page 72 in the August 31 issue.

The authors mention the low "base-collector breakdown voltage" of lateral pnp transistors as are typically used in conventional linear integrated circuits. They also claim that this is due to the shallower diffused structure.

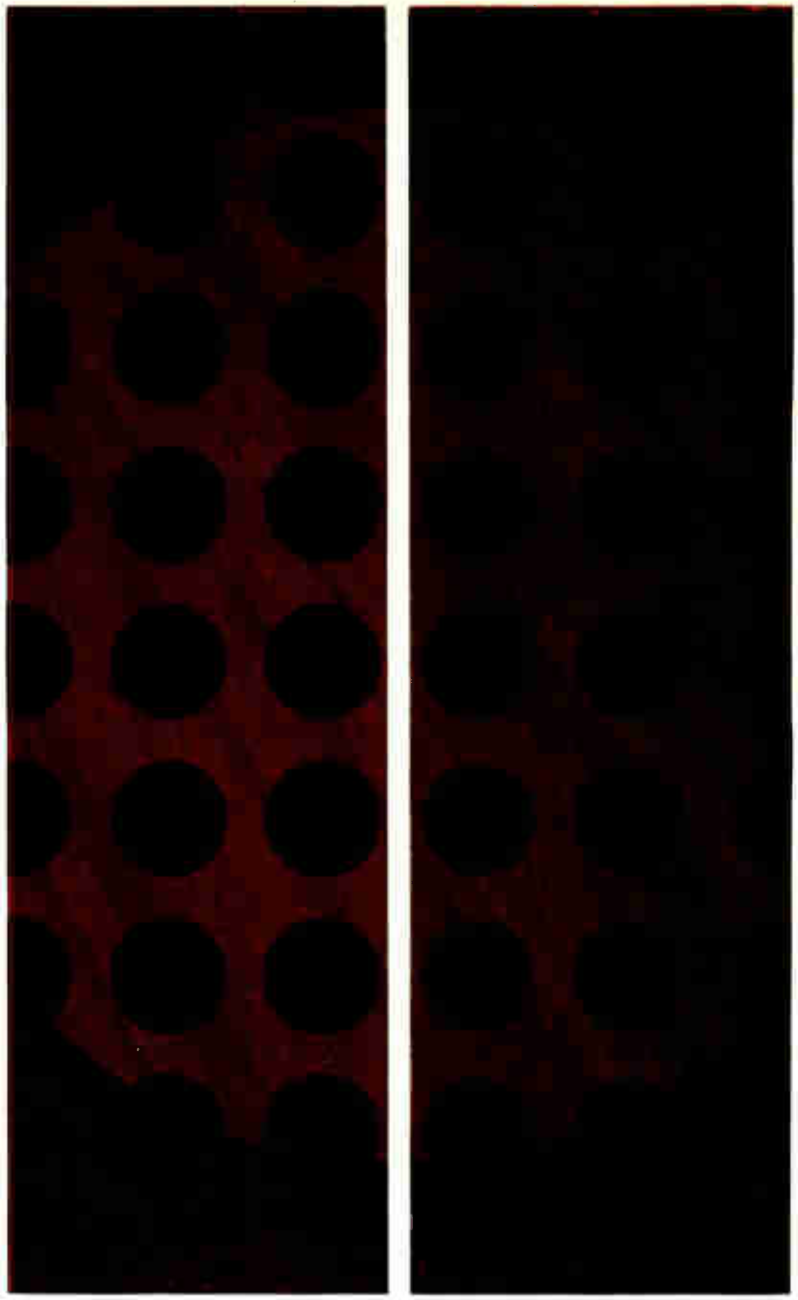
The authors apparently are not familiar with conventional lateral pnp structures. In actuality, the lateral pnp has a collector-base breakdown voltage (BV_{CBO}) which is quite high; for example, with a standard base diffusion and a 5 ohm-cm epitaxial layer, BV_{CBO} is well over 100 volts. Since the collector-base structure of this device is formed of the same base-collector junction as the companion npn transistors in the standard buried-layer IC process, the depths are identical. Npn transistors not limited by punch-through breakdown have a BV_{CBO} very nearly equal to the BV_{CBO} of the lateral pnp transistor, which is one of the highest breakdowns on the transistor chip.

The figure on page 73 indicates that the vertical pnp has higher beta and larger base-emitter breakdown voltages (BV_{EBO}). In general, the vertical transistor as shown has a lower BV_{EBO} than the lateral pnp transistor, because of the required doping densities. It has been demonstrated that without any substantial process changes the lateral pnp transistors can be made that have current gain (h_{FE}) of 100-200 and that substrate pnp transistors can be made that have h_{FE} of 400-500 without compromising breakdown voltages.[1,2] The emitter-base breakdown voltage of the lateral pnp structure is also quite high (typically over 100 V) as the junctions are the same as the collector-base of the npn transistors

(Continued on p. 8)

There's a one micron difference in these mesh screens magnified 100,000* times

Can you see it?



* estimated

Not likely. You couldn't spot a 25 micron difference in these screens with the human eye, let alone one. We picture the enlarged micro-mesh screens because we regularly produce mesh to micron tolerances, or even millionths of inches.

Buckbee-Mears has all sorts of exotic capabilities in electroforming and the precision etching of metal and glass. We've been making precision parts since we began etching metal fire control reticles for the military in World War II. Today, with our automated computer-plotter system (BMAPS), we can do things 20 times faster than a few years ago. And do them more accurately, too.

For example, we electroform standard stock sieves down to 5 micron hole sizes, guaranteed accurate within ± 2 microns. In quantity. We can do even better on special orders.

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Circle 7 on reader service card

Readers comment

and the lateral pnp transistor devices.

The BV_{EBO} of a substrate pnp may be made quite high, depending upon the geometrical configuration chosen; when a large BV_{EBO} is not needed, the geometry is usually such that the reverse emitter-base breakdown is in the range of 6-8 V.

References

1. T.I. Internal Report, X490, 1970.
2. Robert J. Widlar, "Design Techniques for Monolithic Operational Amplifiers," IEEE Journal of Solid-State Circuits, SC-4, August, 1969, 184-191.

Michael J. Callahan Jr.
Integrated Circuits Development
Components Group
Texas Instruments
Dallas

■ *The authors reply: We agree to everything that Mr. Callahan says when applied to the fabrication of conventional bipolar integrated circuits. However, our "complementary-squared" circuits are far from conventional and in selecting the pnp structure, we had to keep in mind compatibility with complementary transistors as well as with bipolar npn transistors, and this compatibility had to be achieved in a low cost, highly reproducible process. To go with a lateral pnp transistor, we would have had to resort to an epitaxial layer to get the breakdown voltage and gain that were necessary. This would have greatly complicated the process, making it more expensive and less reproducible. Hence our decision to use the substrate pnp structure.*

Credit where due

To the Editor: There has been a mistake in giving credit for "Two op amps simplify design of oscillator" [April 27, p. 92]. The circuit authored by Professor Knowlton was in fact written by Robert Selman, an electronics engineering undergraduate at the University of Wyoming.

Dennis Knowlton
Professor,
University of Wyoming
Laramie

"If you're calling Radiation and Harris answers...

Don't hang up!"

RADIATION MICROELECTRONICS HAS CHANGED ITS NAME TO HARRIS SEMICONDUCTOR

Circle 9 on reader service card

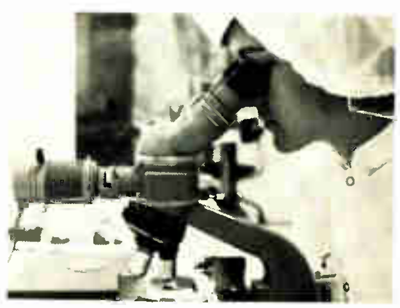
NEW PLANT:

HARRIS SEMICONDUCTOR . . . a new name and a new IC manufacturing facility with approximately 113,000 sq. ft. of the latest innovations in wafer manufacturing and development. (Located in Melbourne, Fla.)

HARRIS SEMICONDUCTOR, the new name for Radiation Microelectronics, is just in time for the opening of one of the most up-to-date IC manufacturing facilities in the country. Smooth production flow and exacting quality control have been the keynote of its design. To assure environmental integrity there are four completely isolated modules right in the heart of the building: two for wafer manufacturing and inspection . . . one for engineering development and assembly . . . and the fourth for photomasking and process development. Each has its own vertical laminar-flow ventilation system which blankets the entire module with super-clean air kept at 72° ± 1°F and 45% ± 1% relative humidity. And as added environmental protection, the air is filtered again by the laminar-flow hoods at each individual production station. That assures us of maximum yield for our high-quality chips. And it assures Harris Semiconductor customers that they'll get IC's with the *best price/performance ratio on the market.*

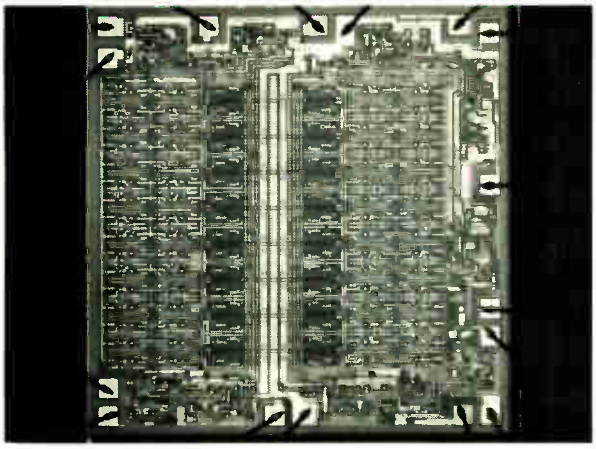
SUPER-CLEAN AIR . . . In vertical laminar-flow hoods designed to provide additional air filtering, wafer photo resist is exposed to ultraviolet light after precise mask alignment.

. . . THE LATEST DIFFUSION EQUIPMENT Six furnace chambers on each of these Brute diffusion systems are regulated within 0.25°C for precise uniformity of wafer diffusion rates.



All material moving through the manufacturing process is continually monitored to assure conformance to the rigid standards of high quality Harris Semiconductor has been noted for.

NEW PRODUCTS

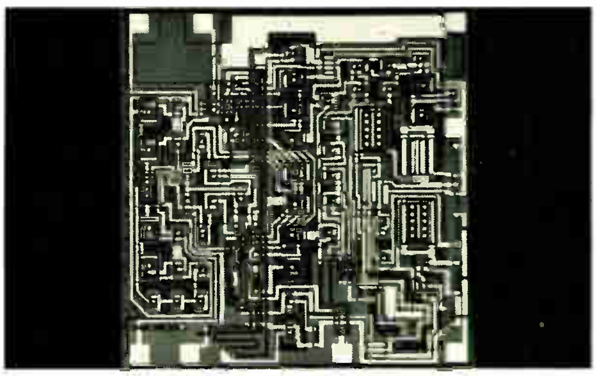


64-BIT BIPOLAR RAM WITH 35ns ACCESS

Using Schottky clamped transistors the Harris RAM-0064 is the first bipolar read/write memory capable of 35ns access times. As a high-speed scratch-pad memory, it provides:

- **DTL/TTL compatibility**
- **Full decoding to 16 words by 4 bits per word**
- **Uses single 5 volt power supply**
- **Open collector output for "Wired-Or" expansion**
- **16 pin dual in-line package**
- **0° to +75°C, $25.60***
- **−55° to +125°C, $32.00***

**100 to 999 unit price*



NEW WIDE-BAND, HIGH-IMPEDANCE OP AMP

Harris' new HA-2620 and HA-2625 Wide Band Op Amps have gain bandwidths which are an order of magnitude better than standard op amps on the market today. In addition, they provide:

- **Input impedance of 500 Megohms**
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**100 to 999 unit price*

And in addition to our recently introduced PROM and 8-bit D/A Converter, watch for these new products soon to be announced:

MEMORIES	DIGITAL	LINEAR
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16 BIT BIPOLAR RAM	9304 DUAL ADDER	
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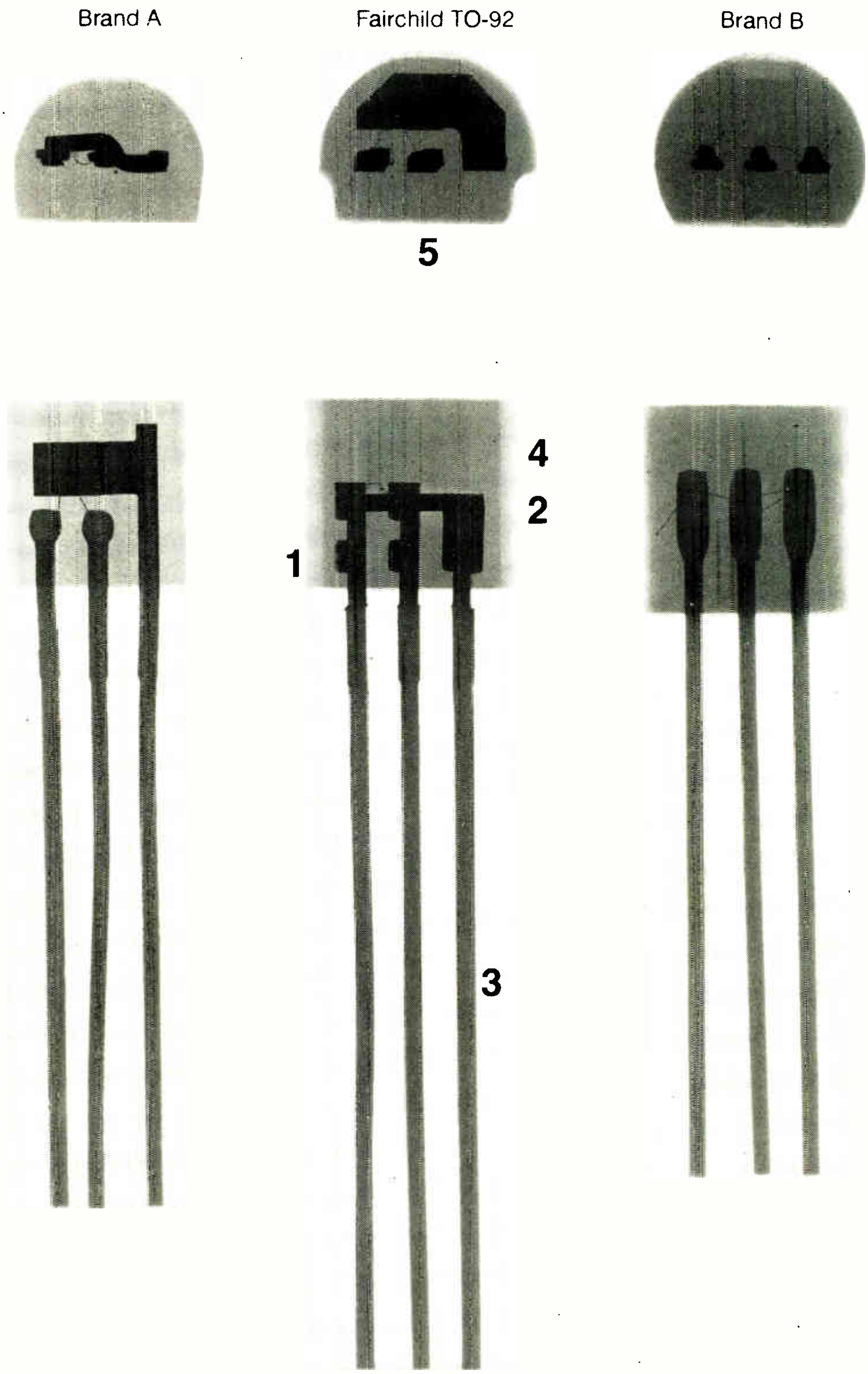

X-RAY PHOTO PROVES FAIRCHILD BUILDS BETTER TO-92 PACKAGES 7 WAYS. **1.** Double-Locked Leads are anchored more firmly, make structure less subject to intermittent opens and shorts from vibration or thermal stress. **2.** Collector Pad mounted perpendicular to natural parting plane gives greater plastic-to-plastic interface, makes body stronger. Also permits top-post bonding, which buries connecting wires deeper into package away from vibrational stress, for increased bond strength. **3.** Copper Alloy Leads dissipate 625 mW in free air, compared to 200-360 mW for most other TO-92 designs. **4.** Special Silicone Moulding Compound permits operation at 150°C min. **5.** Longer Moisture Path, because of chip location and because path is interrupted by 90° change in planes, inhibits moisture progress along lead, provides greater protection from moisture damage.

AND WHAT THE X-RAY DOESN'T SHOW: **6.** Most highly mechanized production in the industry (only 3 operator decisions). Operator dependence is minimized. Product is consistent. Turn-around time is swift. Fairchild distributors can maintain a dynamic inventory. **7.** Computer-Controlled Test Facility is the most sophisticated in the industry. 12 programming modules can each test for 300 conditions (3600 selection tests possible). For you that means faster delivery of more reliable packages.

Our new TO-92 meets JEDEC outline specs, of course. But the internal design, the materials, the production methods, create a package that also meets Fairchild stringent specs for reliability and quality. It's moisture resistant, stable under internal and external temperature stress, resistant to physical damage on your assembly line.

Need further proof? Contact your friendly Fairchild distributor. Or write to us for a catalog, and we'll throw in a free TO-92 with a transparent case so you can see for yourself.

75 Devices

2N3903	FPSA13
2N3904	FPSA14
2N3905	FPSA65
2N3906	FPSA66
2N4123	FPS5551M
2N4124	FPS6511
2N4125	FPS6512
2N4126	FPS6513
2N4264	FPS6514
2N4265	FPS6515
2N4400	FPS6516
2N4401	FPS6517
2N4402	FPS6518
2N4403	FPS6519
2N4409	FPS6520
2N4410	FPS6521
2N5086	FPS6522
2N5087	FPS6523
2N5088	FPS6530
2N5089	FPS6531
2N5209	FPS6532
2N5210	FPS6533M
2N5219	FPS6534M
2N5220	FPS6535M
2N5221	FPS6560
2N5223	FPS6561
2N5224	FPS6562
2N5225	FPS6563
2N5226	FPS6565
2N5227	FPS6566
2N5228	FPS6568
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Circle 13 on reader service card

The crowd around the IEEE's suggestion box must grow if it's to remain a viable organization providing its members with services they want and need. This is the edict of James H. Mulligan, who takes the IEEE helm in January after 25 active years in the organization. He will succeed J.V.N. Granger, director of Granger Associates.

Mulligan, also executive secretary of the National Academy of Engineering, got involved in the Institute of Radio Engineers in 1945, some 20 years before it merged with the American Institute of Electrical Engineers to become the IEEE. He has been active in the IEEE's Computer Group, and is now institute vice president.

Tall and bespectacled, the 50-year-old Columbia University engineering Ph.D. thinks the major problem at the institute is dissemination of information to member engineers, and opening up two-way communication. He has several ideas on how the engineers who created information technology can put it to their own use, through closed-circuit television aural and video cassettes, and the use of educational television channels during non-prime time hours. Until now, he says, there has been only "casual consideration" of new information transfer programs.

In addition to improving the data flow to members, Mulligan's activities next year cover a "multitude of sins," he says, naming first, increased attention to the "integrated effect of activities on career development of the individual." He says the institute must develop programs geared for engineers at various stages in their career. The programs would have to suit the graduate engineer just making the transition from academic life to fulltime employment, as well as the technical manager who has been in the business for 10 or 20 years. IEEE has 22,000 student members, and 140,000 professional members, who pay $25 a year in dues plus from $4 to $9 for membership in each of the institute's 31 technical sections.

During his presidency, more emphasis will be placed on stimulating membership activity in new engineering areas—such as the urban environment, including transportation and pollution control. But, he cautions, any new programs will depend on "The interest in the marketplace. I do think there is going to be increased Government support in these areas, and people are highly motivated toward urban systems."

Of his post at the NAE, Mulligan says, "The two activities complement each other. The NAE is concerned with broader problems: how the engineering community can best serve the nation, and the IEEE is one segment of the engineering community." It helps, he says, to be well informed about developments in the entire engineering community.

In the view of John H. Sidebottom, new director of marketing at Raytheon's equipment division, "we need a broader customer base." The division's product line includes radars, microwave communications, displays, intelligence equipment, and inertial navigation systems. A good 75% of its sales are to the military—but the military is funding fewer new starts these days—and a major customer for the communications and data processing gear is NASA, whose budget has been cut.

Instead of seeing the current procurement situation as a dead end, however, Sidebottom considers it a challenge. "The customer's problems are still there," he says, "but his ability to make investments and his priorities are changing, and we have to be smart enough to manage the change. He hopes to beat it by "concentrating more heavily on creative product development which will expand present product lines and by doing work which will lead to new ideas. We'll add on to, and improve, systems and products rather than buy time in 1975 and

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Who's who in electronics

Sidebottom

beyond." He would also like to see "a transfer of techniques into commercial aviation; we have a lot of good products. We are looking to areas where we have worked with NASA in the past to see if we can expand them."

Accordingly, he intends to increase the division's already high R&D investment. "We have to continue to put increased amounts of effort into R&D, and into more inventive applications." He also plans research and development in solid state technology.

By expanding into commercial areas, Sidebottom expects that civilian sales, which now account for only 10% of the total, "could almost equal total government sales in three to four years." But handling this increase will take different sales skills and a different marketing organization.

"A good bit of government business is sold by the engineers, program managers, and executives," he says, "and is mostly done through home base." For commercial customers, however, a field service organization would have to be developed and Sidebottom is now studying the problem, although he says the changeover "won't be rapid; it will grow and develop in the next year or two."

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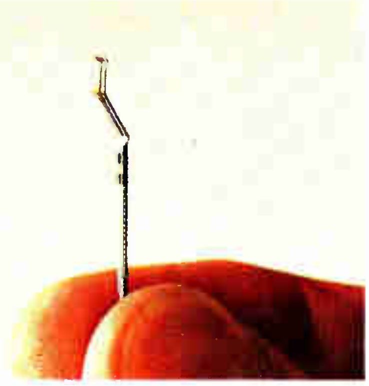

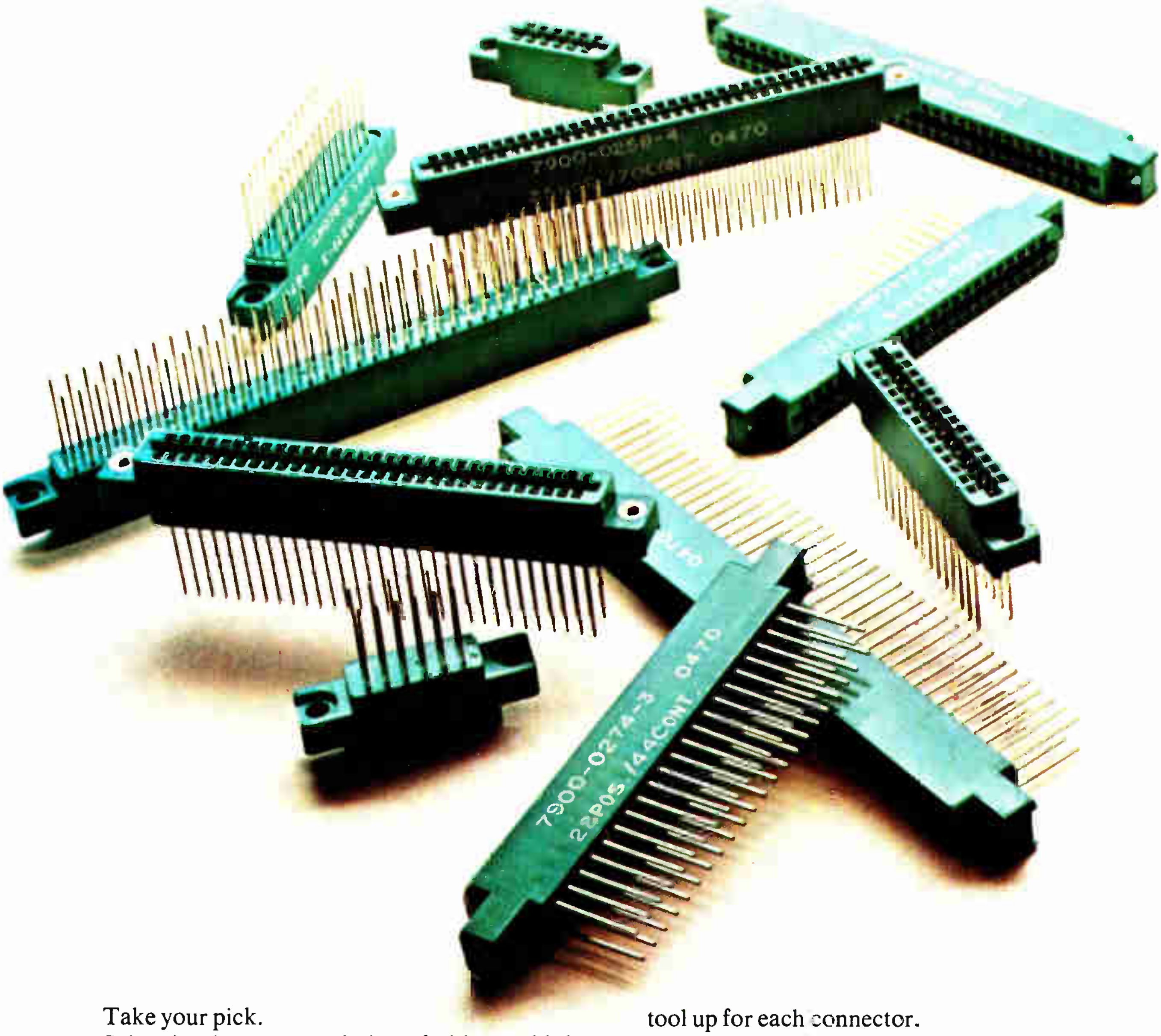

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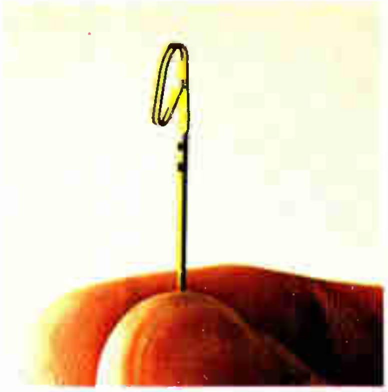

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Circle 21 on reader service card

Job hunting at Nerem

As always, Nerem (November 4, 5, and 6 in Boston) will reflect the industrial profile of the New England area in its technical program. But this year it will reflect the economy, too, in two sessions that don't appear in the official program and in a job opportunities center that may be the first of its kind at any IEEE-sponsored convention. The so-called brown bag lunches and the job center are the part of the Nerem lineup that will probably hit the hardest. The lunches cost $3, with reservations made in advance, and this buys a seat and a box lunch.

On Nov. 5, Albert J. Kelly, former deputy director of the NASA Electronics Research Center and now dean of Boston College's School of Management, will detail the outlook for scientific and technically based businesses and professions in today's recessive economy. He'll cover the implications of Government spending cuts, the problems of converting aerospace technology to commercial use, potential new market areas for budding entrepreneurs, and the future of the technical professional as such—a very disillusioned group after nearly two years of layoffs and cutbacks.

The Nov. 6 lunch features the next IEEE president, James H. Mulligan. He'll try to summarize the institute's position on employment, portable pensions, unionization, and other similar topics. As one local IEEE member put it, "The IEEE could turn into a union right there." And even if it doesn't, Mulligan's opinions are going to get an interested hearing; he'll be IEEE president for the next year, one in which the institute may be forced to change its stance on many employment-related questions.

One of the busiest fixtures at Nerem from Nov. 3 on should be the job opportunities center in the headquarters hotel, the Sheraton Boston. The center appears to be a break with the tradition of damning the resume rooms that have crowded around the fringes of past IEEE meetings. The Nerem executive committee is asking companies nationwide to submit paragraph-long descriptions of openings to be posted, bulletin-board fashion, in the Andover Room. Attendees can look for jobs that interest them, but must make contacts by themselves; no interviews or resume passing is going to be allowed in the center, and the IEEE still plans to discourage the commercial "body snatchers."

For those interested in the technical program, activities begin Nov. 3 with a preconvention tutorial seminar in digital signal processing which takes its attendees from basics through applications like speech processing, and on into hardware implementation both of simple digital filters and signal processing systems. The seminar starts at 9 a.m. and ends at 10:15 p.m., and requires a special reservation to be made through the regional IEEE headquarters.

The conventional technical program runs from Nov. 4 through 6 and includes sessions on such "now" topics as pollution control (session 1), evolving minicomputer systems (session 11), and three sessions on varying aspects of medical electronics (13, 18, and A-1). Others touch on magnetic logic and storage devices (session 20), and the Department of Transportation will man a session on air traffic control in the 1970s.

For information (and preregistration for the luncheons and digital signal processing seminar) contact: IEEE Boston Section, 31 Channing St., Newton, Mass. 02158.

Calendar

Society of Engineering Science Meeting, George Washington University; Washington, **Nov. 9-11.**

International Congress on Microelectronics, International Electronics Group; Munich Fairgrounds, Germany, **Nov. 9-11.**

Symposium on Man-Machine Systems, IEEE; Langford Hotel, Winter Park, Fla., **Nov. 12-13.**

Symposium on Communications, IEEE; Queen Elizabeth Hotel, Montreal, Canada, **Nov. 12-13.**

Annual Conference on Engineering in Medicine and Biology, Alliance for Engineering Medicine and Biology; Washington Hilton Hotel, Washington,

(Continued on p. 24)

Meetings

(Continued from p. 22)

Nov. 15-19.

Magnetism and Magnetic Materials Conference, IEEE; Diplomat Hotel, Hollywood Beach, Fla., **Nov. 15-19.**

Hybrid Microelectronics Symposium, International Society for Hybrid Microelectronics; Century Plaza Hotel, Beverly Hills, Calif., **Nov. 16-18.**

Conference on Magnetism and Magnetic Materials, IEEE, American Institute of Physics; Hotel Plaza, Miami Beach, **Nov. 17-20.**

Asilomar Conference on Circuits and Systems, University of Santa Clara, Naval Postgraduate School; Asilomar Hotel and Conference Grounds, Pacific Grove, Calif., **Nov. 18-20.**

Short courses

Hybrid Computing Techniques, Programing, and Applications, Schools of Engineering and Laboratory for Applied Industrial Control; Purdue University, Lafayette, Ind., **Nov. 9-20;** $350 fee.

System Effectiveness—From the Support Point of View, University of California at Los Angeles, Boelter Hall, Room 2444, **Nov. 30-Dec. 4;** $320 fee.

Technical Data Requirements for Systems Engineering and Support, University of California at Los Angeles; Boelter Hall, Room 5704, **Nov. 30-Dec. 11;** $420 fee.

Call for papers

Reliability Physics Symposium, IEEE; Stardust Hotel, Las Vegas, March 31-April 2, 1971. **Nov. 16** is deadline for submission of abstracts and summaries to Dr. O.D. Trapp, Technical Program Chairman, 1971 Reliability Physics Symposium, Fairchild Semiconductor, 313 Fairchild Drive, Mountain View, Calif. 94040.

Symposium on Theory of Computing, Association for Computing Machinery; Shaker Heights, Ohio, May 3-5, 1971. **Dec. 1** is deadline for submission of extended abstracts to Dr. Philip M. Lewis, G.E. Research and Advanced Development Center, Schenectady, N.Y. 12305.

Symposium on Commercial Applications of Ultrasonics, Ultrasonic Manufacturers Association; International Hotel, JFK International Airport, Jamaica, N.Y., March 24, 1971. **Dec. 15** is deadline for submission of abstracts to Ultrasonic Manufacturers Association, 271 North Ave., New Rochelle, N.Y. 10801.

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PD mW	I mA	NPN JEDEC Type	NPN h: I .1 V 1V	NPN h: I =300 V 2V	NPN h: I 800 V 5V	NPN Noise fig. dB (max)	PNP JEDEC Type	PNP h: I 1 V 1V	PNP h: I =300 V 2V	PNP h: I 800 V 5V	PNP Noise fig. dB (max)
400†	500	2N6000	50	40		3.0	2N6001	90	35		3.0
400†	500	2N6002	130	80		2.0	2N6003	210	50		1.5
400††	500	2N6004	50	40		3.0	2N6005	90	35		3.0
400††	500	2N6006	130	80		2.0	2N6007	210	50		1.5
500††	800	2N6010	45	85	45	5.0	2N6011	70	65	45	3.0
500††	800	2N6012	90	160	50	3.0	2N6013	180	135	70	2.0
500†††	800	2N6014	45	65	15	5.0	2N6015	70	60	35	3.0
500†††	800	2N6016	90	60	15	3.0	2N6017	180	125	55	2.0

† BV = 25V, †† BV = 40V, ††† BV_{CEO}=60V

GE Type	Replaces	GE Type	Replaces	GE Type	Replaces
GET706	2N706	GET2221A	2N2221A	GET3013	2N3013
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GET914	2N914	GET2222A	2N2222A	GET3638	2N3638
GET929	2N929	GET2369	2N2369	GET3638A	2N3638A
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POWER at + 70°C	2.25 W	3 W	0.5 W	0.8 W	0.5 W	0.5 W
TEMPERATURE RANGE	−55°C to +120°C	−55°C to +150°C	−55°C to +120°C	−55°C to +150°C	−55°C to +120°C	−55°C to +120°C
RESISTANCE RANGE (Tolerances: ±10 and 20%)	50 ohms to 5.0 megs	50 ohms to 5.0 megs	100 ohms to 5.0 megs	100 ohms to 5.0 megs	100 ohms to 5.0 megs	100 ohms to 5.0 megs
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FEATURES (Many electrical and mechanical options available from factory)	Single, dual, and triple versions available. Long rotational life. Ideal for attenuator applications. Snap switches can be attached to single and dual.	Single, dual, and triple versions available. Long rotational life.	Miniature size. Immersion-proof. SPST switch can be attached.	Miniature size. Immersion-proof.	Commercial version of type G. Immersion-proof.	DUAL section version of type G. Ideal for attenuator applications. Immersion-proof.

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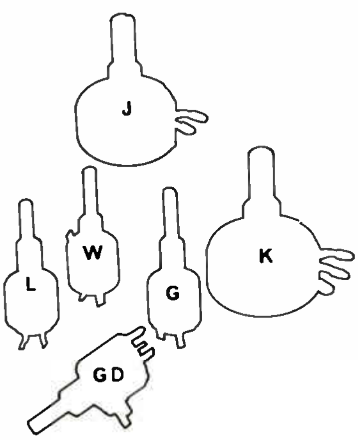
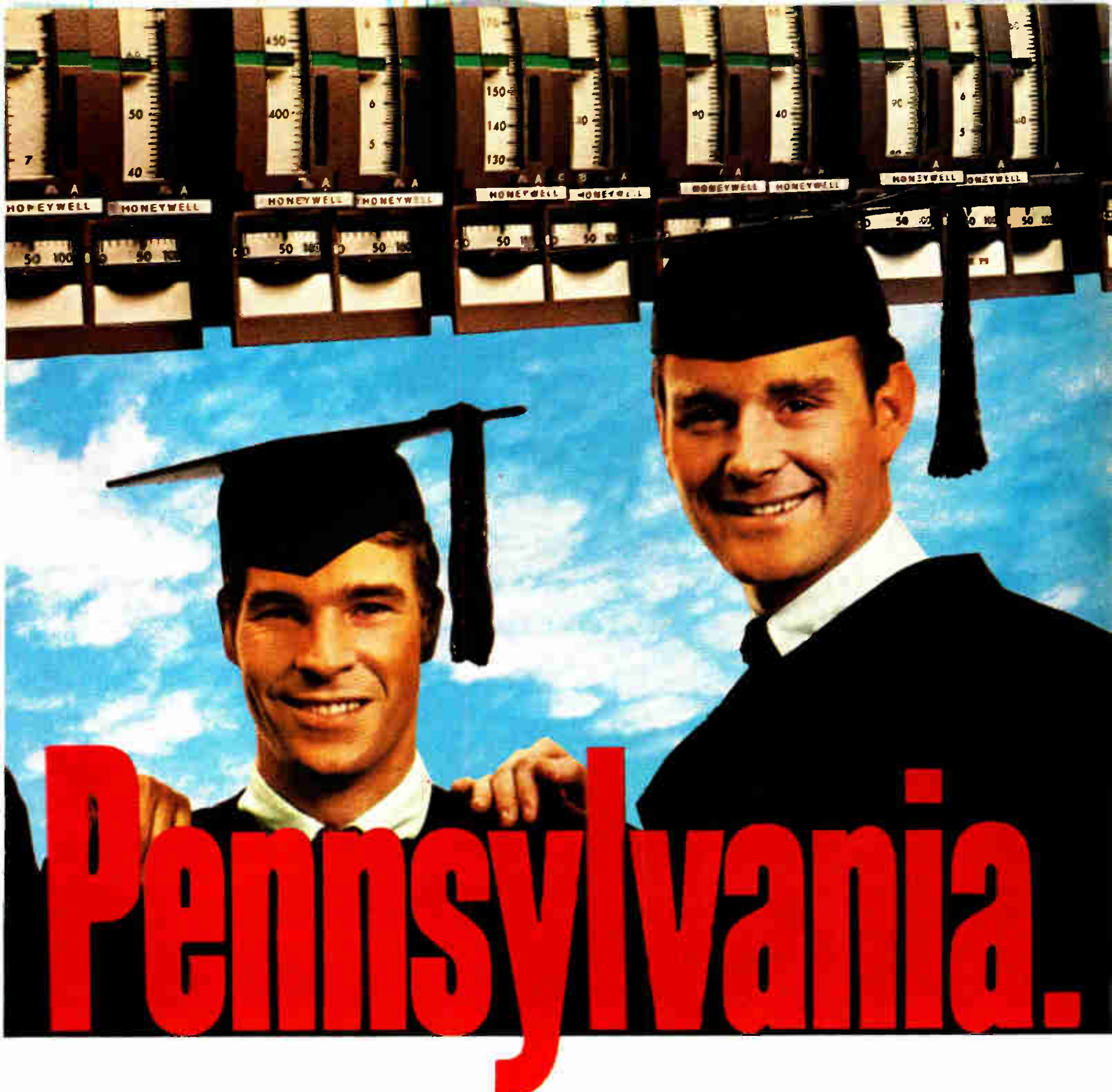


Circle 27 on reader service card



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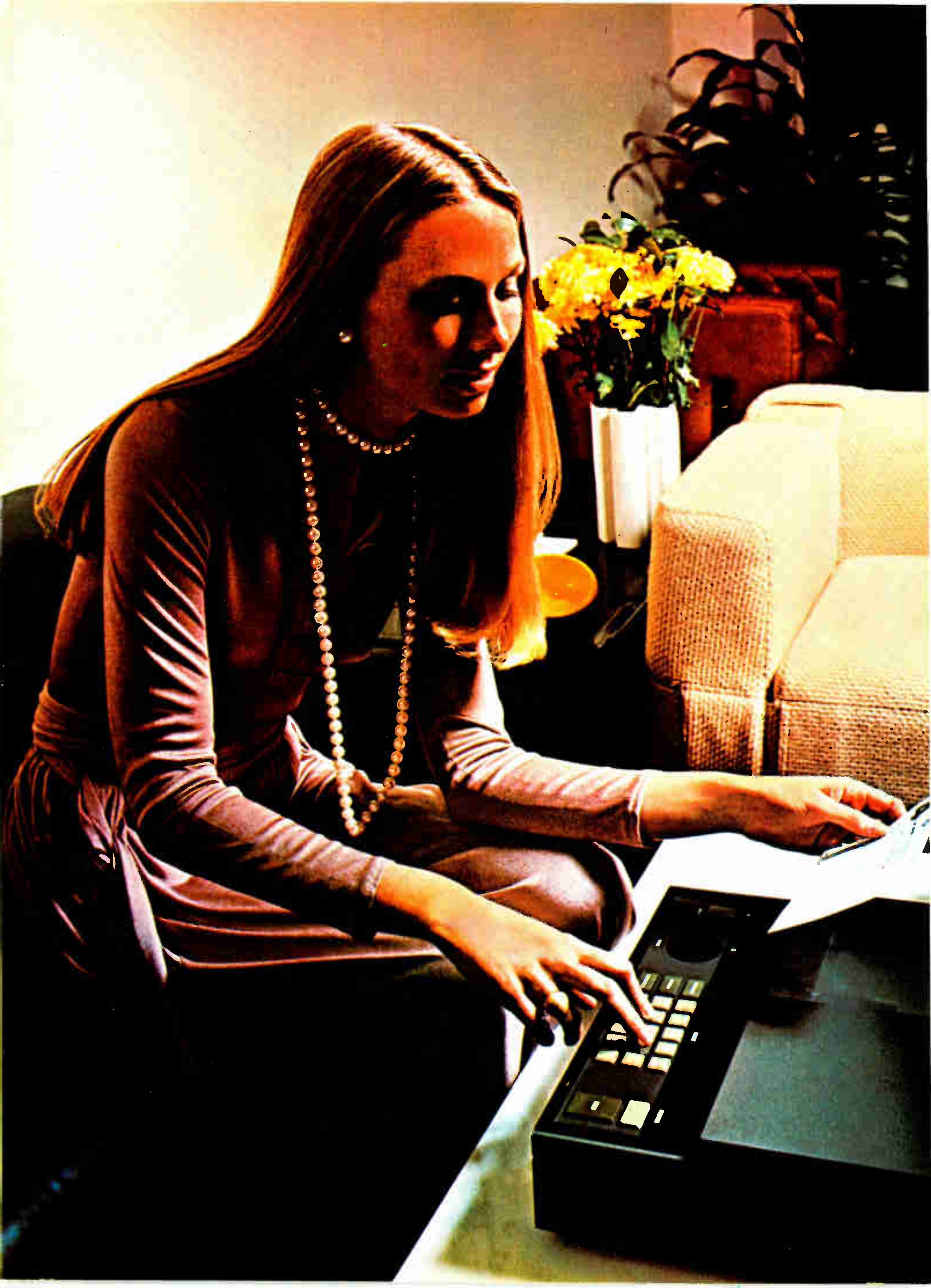

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Electronics Newsletter

October 12, 1970

Signetics mounts MOS drive

Signetics is about to make a marketing push in MOS. The company's present line consists only of six shift registers, but sources close to the company expect from 12 to 15 new products to be introduced in the next month. They will include fast random-access memories (less than 200-nanosecond access times), large shift registers, and 2,000-bit read-only memories. One of the first units will be the 256-bit RAM that the company is delivering to National Cash Register under a development contract.

The buildup has been taking shape over the past six months. About 20 MOS design and fabrication experts have been hired to form the central MOS team, and equipment has been assembled at both the company's Sunnyvale, Calif., headquarters and its Utah plant. Both standard (high-threshold) and silicon gate (low-threshold) processes will be employed.

Two-year guarantee on color TV readied by Motorola

Keeping ahead of the consumerism push in Washington, Motorola will guarantee for two years all labor and parts for all of its color television receivers beginning this fall. Edward P. Reavey Jr., vice president and general manager of the Consumer Products division, says the move is made possible by confidence in Motorola's modular construction. He says the guarantee will add about $12 to the price of each unit.

Motorola also will anticipate information labeling regulations by printing all details of its new guarantee clearly on the color television receivers so the consumer cannot be confused by dealer claims and promises.

Photocathode copier readied for market

Look for prototype and field test units early next year of electrostatic office copiers featuring a photocathode image-conversion device. Being developed by Allied Paper Co., a division of SCM, this type of copier is faster than those using the selenium drum photoconductive technique. Allied obtained patents on photocathode image conversion almost two years ago and has since completed a research contract with CBS Labs to perfect a photocathode tube. When the machine is ready for production, Allied will build and market copiers and the special reproduction paper.

FTC probing Toshiba oven claims

In the first of many expected consumer interest actions against microwave oven makers, the Federal Trade Commission and Public Health Service indicate they're investigating a complaint against Toshiba America Inc. for deceptive advertising. The investigation was instigated by Amana Refrigeration Inc., a subsidiary of Raytheon which also makes such ovens.

The Toshiba advertisement claims its oven is the "space age cooking unit that meets 1971 standards now," and that no unit will leak more than 5 milliwatts of radiation per square centimeter "during its useful life." The advertisement also claims that the product has received the approval of Underwriters' Laboratories and the Federal Communications Commission.

Electronics Newsletter

Laser to track DC-10 during FAA tests

A laser tracking system designed to monitor in-flight performance of new jet aircraft during Federal Aviation Agency certification tests is being produced by Sylvania Electric Products, Mountain View, Calif. **Capable of tracking aircraft up to 60,000 feet, the system will evaluate avionic, aerodynamic, and acoustic performance of the McDonnell Douglas Corp.'s DC-10.**

In tests, a low-powered, infrared laser beam from a mobile ground station near a runway locks onto a reflector mounted below the nose of an aircraft in flight. The reflected beam is picked up by sensing equipment in which the tracker determines the precise speed, azimuth and elevation angles, and altitude of the aircraft. The system will offer greater accuracy than that of commonly used tracking arrangements of onboard sensors.

Work on the laser tracker is being done under contract from McDonnell's Douglas Aircraft division in Long Beach, Calif. Delivery is scheduled for December.

Motorola switching to laser scriber

North American Rockwell Microelectronics Co. isn't the only semiconductor manufacturer that has conferred production status on laser wafer scribers [*Electronics*, Aug. 17, p. 34]. Motorola's Semiconductor Products division, after quietly evaluating the technique for more than a year, has bought and is dicing zener diode wafers with a $55,000 laser scriber made by the Quantronix Corp. of Smithville, N.Y. **The machine eventually will replace all four diamond scribers on the Motorola zener diode line.**

Ronald Roberts, materials manager for zener diodes, calls the machine, believed to be the first designed from the floor up as a silicon wafer scriber, "the only major breakthrough I've seen in wafer dicing in 11 years." **He looks for the machine to cut Motorola's yield loss in the scribe-and-break step from between 10% and 15% to 5% or less,** and to pay for itself possibly within a year.

CBS develops low-light-level color television

Sensitivity that's 100 times better than that of present color television cameras is the promise of a low-light-level color system now on the bench at CBS Laboratories. Expected to be ready in about a year, the **field-sequential camera picks up subtle color variations at light levels equivalent to a quarter moon at night** when the human eye cannot discern gradations in shades.

The bench unit uses a monochrome image intensifier to boost output from the video tube. A color image intensifier would make for better quality color plus no high-voltage (23,000-volt) component breakdowns, but one has yet to be developed. **Potential users will be the military, for real-time night reconnaissance, and physicians, for viewing internal organs.**

Westinghouse to sell commercial SEC

The Westinghouse Electric Corp. hopes to make a dent in the color TV camera tube market dominated by Philips' Plumbicon. The company's Elmira-based Electronic Tube division **is planning to introduce a commercial version of its burn-resistant Proxicon SEC,** heretofore aimed exclusively at the military and space markets. Westinghouse formerly made TV sets for the consumer market.

"ZERO" Reaction Time

clip transients...

with the New Uni-Imp Voltage Surge Protector

- **Impulse Ratio** .... **1.1 to 1**
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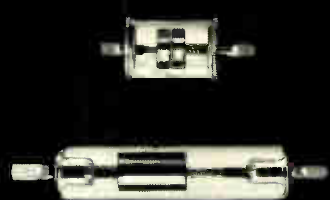
Now it is possible to protect sensitive components, even semi-conductor equipment, against voltage transients without concern for the rate of voltage rise. The "zero" reaction time of Signalite's new Uni-Imp is only one of its many unique features. Others including its Bi-Polarity, immunity to di/dt restrictions, infinite leakage resistance, are described in a new data sheet.



AVAILABLE UPON REQUEST Detailed Data Sheet . . . on Signalite's Uni-Imp Zero Reaction Time Voltage Surge Protectors.

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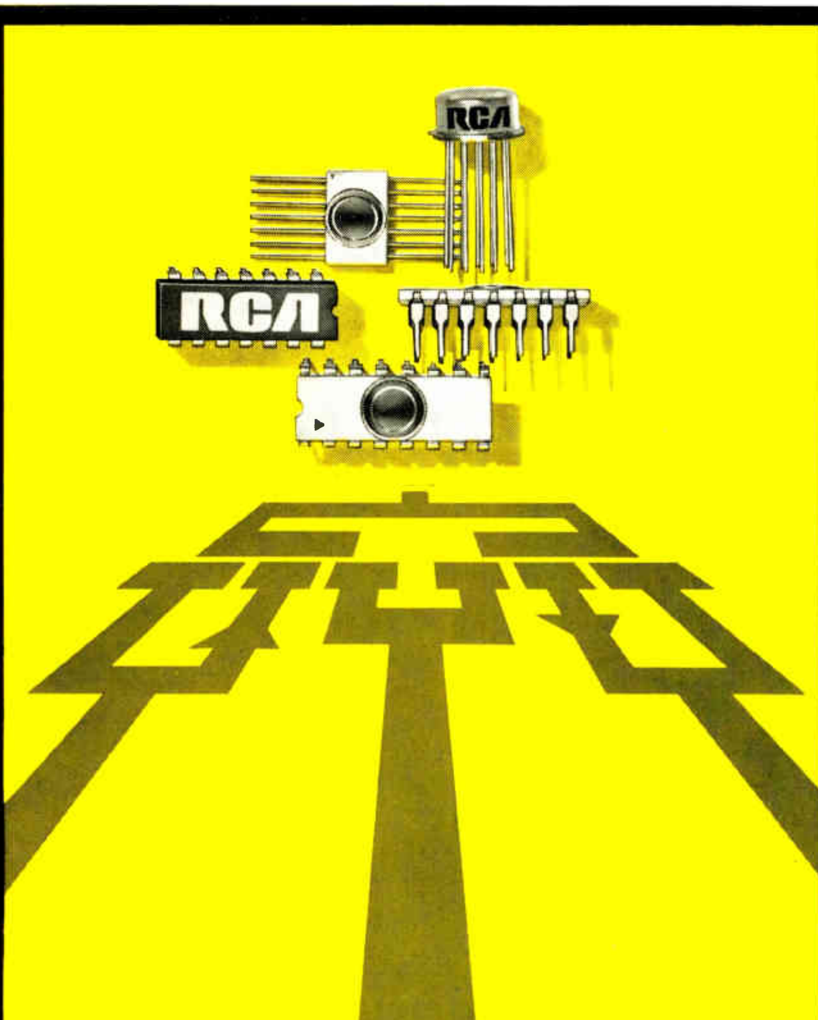

RCA COS/MOS PERFORMANCE FEATURES

Wide Operating Supply-Voltage Range: 5 to 15 V

Ultra-Low Power Dissipation:

- Gates—CD4000 and CD4000D Series:* $P_T = 10$ nW/pkg (typ) at $V_{DD} = 10V$
  —CD4000E Series:** $P_T = 50$ nW/pkg (typ) at $V_{DD} = 10V$
- MSI Circuits—CD4000, CD4000D and CD4000E Series: $P_T = 10\ \mu W$ (typ) at $V_{DD} = 10V$

High dc and Dynamic Noise Immunity: 4.5 V (typ) at $V_{DD} = 10V$ over full operating-temperature range

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Single Phase Clock

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**Plastic dual-in-line package

RCA
Integrated Circuits

New diode cathode may take heat off more tubes

RCA researchers find optoelectronic approach magnifies efficiencies of solid state cathode

In many applications, the old hot-wire thermionic-cathode vacuum tube defies replacement by solid state devices. But the high temperature essential for generating electrons from the cathode is also the chief source of tube failure. Enter, therefore, the tube with a solid-state cathode, providing truly cold electron emission into a vacuum.

At the David Sarnoff Research Labs in Princeton, N.J., RCA scientists under the direction of Henry Kressel have taken a unique optoelectronic approach to cold cathodes. With the aid of a double heterojunction gallium arsenide diode structure, photons are produced very efficiently and are transported to an absorbing p+ region. There, they generate electrons which, due to a specially treated (low work function) surface layer, are emitted at overall efficiencies up to 1,000 times better than other solid state cathode attempts.

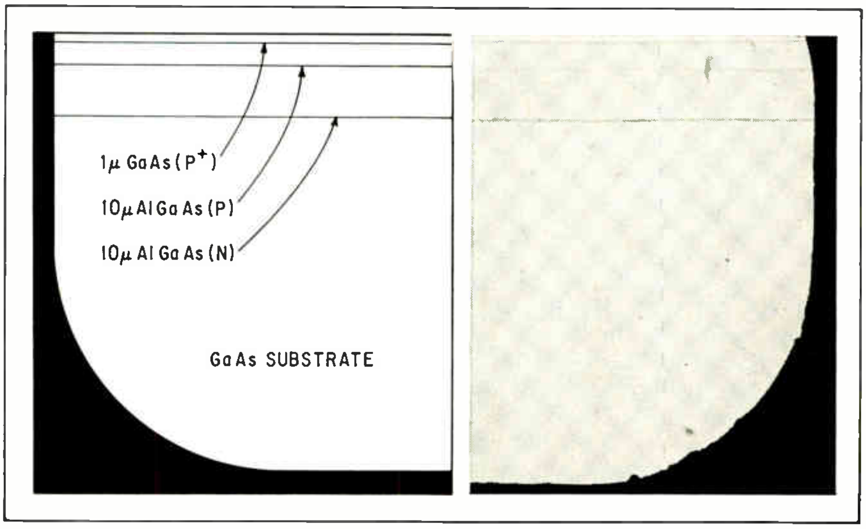
The cathode is still in the research stage. But if its efficiencies can be increased by a further factor of 10, and if its operating current densities also can be increased, it could start assuming many of the present functions of the vacuum tube.

A solid state electron source would also be a natural where the marriage of solid state and vacuum technology already has been accomplished. In the silicon-target vidicon, for example, the present hot-electron scanning source could be replaced by a cold solid state source, doing away with the high temperature: the tube would be simpler in construction, last longer, and, since solid state electron beams have lower energy than thermionic ones, facilitate focusing. Moreover, electron-beam diode arrays could be used to match the silicon diode target array, eliminating the need for scanning.

The cold electron source also can be used in transistors. In fact, this approach, called an Electron Beam Injection Transistor (EBIT), could be the start of a whole new high-power, high-frequency transistor technology, for it could eliminate the emitter, the villain in frequency-limiting parasitics, substituting the electron beam for emitter functions.

There have been other attempts at solid state electron emission: forward-biased p-n junctions, Schottky barriers, conventional photosurfaces (S-1) illuminated by electroluminescent diodes. But overall electron-emission efficiencies were bad, as low as 10^{-5} to 10^{-10}, and current densities were also low. These approaches achieved electron emission by direct injection and electron transport to the surface of the p-n diode—and this meant that the p-layer through which the transport occurs had to be very thin to prevent the electrons from being absorbed and lost in too great numbers. But then

Cooling it. Photons are transported to absorbing GaAs layer where recombining electrons escape into vacuum. Heterostructure allows efficient photon production; surface allows efficient escape.



the electrode contacts on their thin p-layer surface produced high fields which crowded the current wastefully under the electrode and blocked the emission.

RCA got around this by using light transport for electron emission. The junction is forward biased so that light is generated with internal quantum efficiencies in excess of 50%. The photons are then transported with little attenuation to a highly doped light-absorbing region near the surface where they are reconverted into electrons. On the zinc-doped GaAs p region is a specially treated epitaxial layer (cadmium sulfide and oxygen under vacuum) which permits a large fraction of the electrons—potentially up to 20%—to escape into the vacuum.

Companies

Sylvania closes Semiconductor division

For the company that introduced transistor-transistor logic to the commercial integrated circuit buyer, it was an ignominious end—a simple shutdown of the Semiconductor division of Sylvania. While the company called it a three-month phaseout, it's estimated that only about 50 employees of the 1,235 affected are still on the job—winding up assembly and test work—less than two weeks after the October 1 closing announcement was made.

Sylvania Electric Products, a General Telephone and Electronics subsidiary, blamed its decision on the "disorderly conditions" in the semiconductor industry and the outlook. The firm felt there is no indication of stability within the foreseeable future. It added that the decline in defense spending and extreme price competition in sales to the computer industry had a "particularly severe impact on semiconductor profitability."

However, the division's problems went beyond the current business recession. It's estimated that Sylvania Semiconductor lost on the order of $3 million to $6 million annually in recent years. With other divisions profitable, the company had carried Semiconductor as a tax writeoff. But with overall profits declining, the company simply was not willing to carry the division any longer.

Book value of the division's three plants in Woburn, Mass., Hillsboro, N. H., and Bangor, Maine, is estimated to total about $25 million, including inventories. Although other Sylvania units will probably move into some of these facilities, probably two of the three plants will be closed. Until the division closes its books Dec. 31, it will take care of business already contracted for from inventory.

It was probably high-level management's refusal to fund the division's advanced development programs that caused its ranking in the TTL market to drop from first place in the early 1960s to near the tag end. Low development budgets and a series of repressive administrative decisions hamstrung the division, say insiders.

But it didn't have to happen, they say. "We had it all in the back room," declares one sad Sylvanian. "We had a great beam-lead IC capability that was never released for production; we had an automated beam-lead bonding system 18 months ago; and we had a new MOS process in house that had the highest threshold-to-breakdown ratios yet. It was TTL compatible, promised the same kinds of speed, and used smaller geometries than other MOS schemes. We really could have packed the logic onto those chips," he says wistfully.

Late in September, the division's lab made its first metal oxide semiconductor chip—256-bit memories—using the new process and they worked well.

No Sale

The Sylvania Semiconductor closing apparently signaled defeat for Robert Castor, general manager, who had been spending much of the last few months, up to the last minute, looking for a buyer for his division. One company that had been very interested was Corning Glass Works, according to one Sylvania executive. He said that Corning had been close to buying the division and merging it with Signetics. "It was a good customer fit, and there was very little product overlap," he noted. However, the deal fell through. A Corning spokesman said his firm is not interested in acquiring the Sylvania division, and would not comment on whether or not Corning had been talking to Sylvannia about such a deal.

One segment of the Semiconductor division that Sylvania says it isn't phasing out is the microwave diode department. The reason is that the company is in "hard negotiations" to sell this as a unit. As far as the rest of the division, piecemeal sales of some patents and production equipment and plants is expected.

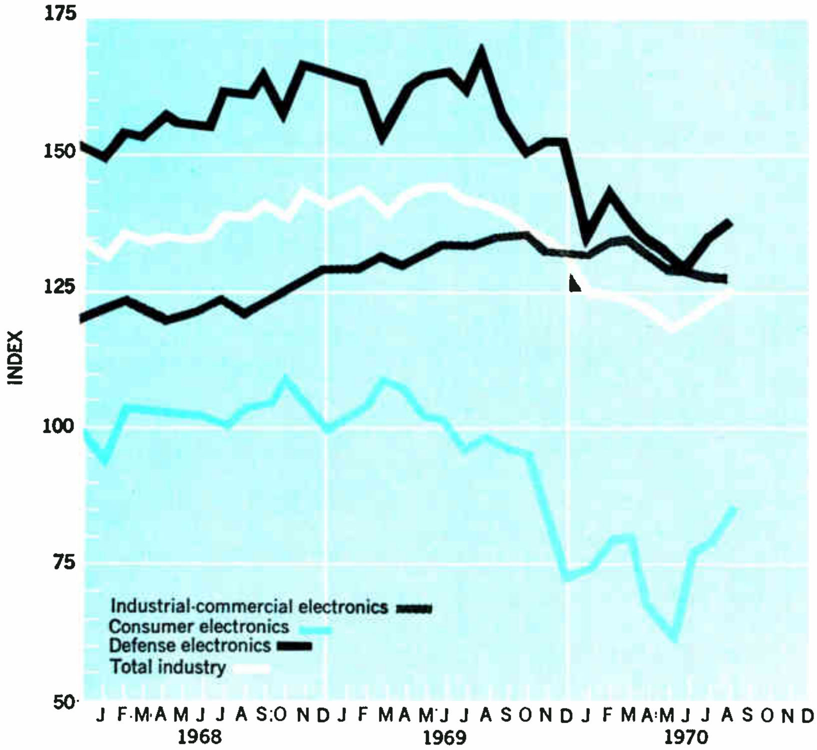
Medical electronics

Hill unlikely to act on device regulation

Despite the Health, Education and Welfare Department's efforts to bring the $550 million medical electronic devices market under its regulatory scrutiny, passage of enabling legislation is unlikely, Capitol Hill sources say. HEW has recommended that the devices be regulated through its Food and Drug Administration and assorted advisory groups.

Problems of improper design, high electrical leakage from equipment, shoddy cables, and poor assembly of parts in many medical devices, are recognized by many Congressmen. But they question the competence of the Federal Government to regulate the market. Some say it would take 10 years to set up an effective regulatory procedure. "The FDA hasn't caught up with the legislation of 1962" providing for drug efficacy testing, says one source.

In addition to skepticism about



Electronics Index of Activity

Oct. 12, 1970

Electronics production in August rebounded a bit from July's revised figure. It gained 2.7 index points to 126.3. Leading the climb was the consumer area, up a healthy 6.8 to 87.0. This third straight monthly increase appears to signal the arrival of the long-awaited recovery in this sector.

Defense electronics also showed signs of life, climbing 3.0 points from the previous month to 138.2. However, defense is still down 21.2 points from its August 1969 level. The only component of the index to drop for the month is industrial-commercial electronics. It edged down 0.4 point from July's revised 128.4.

Segment of Industry	Aug. '70	July '70*	Aug. '69*
Consumer electronics	87.0	80.2	97.6
Defense electronics	138.2	135.2	159.4
Industrial-commercial electronics	128.0	128.4	133.2
Total industry	126.3	123.6	141.1

Indexes chart pace of production volume for total industry and each segment. The base period, equal to 100, is the average of 1965 monthly output for each of the three parts of the industry. Index numbers are expressed as a percentage of the base period. Data is seasonally adjusted.
*Revised.

Federal ability to regulate devices, the House Public Health and Welfare committee, whose approval is required first, has placed medical device regulation far down the priority list following such items as alcoholism, heart disease, cancer, Indian health, and communicable diseases.

Medical devices are loosely defined as drugs, and as such come under FDA regulation, but current procedures empower the FDA only to ask a manufacturer to voluntarily recall a device—if a defective device is discovered. The procedure is a "joke," says Rep. Seymour Halpern (R., N.Y.), one of the House's staunchest proponents of medical device safety regulation.

The HEW report has prompted the FDA to begin taking a two-year inventory of medical devices on the market to see which can be exempted from standards or preclearance, those for which standards exist, and those which should be made subject to performance review prior to marketing. Standards and laboratory testing for electrical components and electronic devices should be required, the report recommends.

Consumer electronics

Laughing on the outside, restrained on the inside

Home entertainment manufacturers are permitting themselves the luxury of optimism for the first time since consumers began staying away in droves a year ago. Besides a gut feeling that buyers are again in the mood for phonographs, radios, and television receivers, manufacturers now have figures to back them up.

The Electronics Index of Activity (see chart) this month shows that consumer electronics has registered its third straight monthly gain in August, with a jump of 8.5% over July's 26% rise.

A survey of leading U.S. manufacturers indicates that industry belt tightening in national distribution, a raft of extra sales during the summer, and surprisingly good acceptance of technical innovations plus just a general seasonal upturn may be some of the reasons.

On the other hand, though things have improved, it's still true that the month's index is more than 10 points below that of a year ago. For example, the consumer manufacturers' darling, color TV, will have to strain to hit the 5 million sets mark. This is a far cry from the sales of 10 million predicted by the industry just two years ago as to where color TV would be in 1970.

As one cautious TV marketing

man philosophized: "This business just isn't as good as we thought. This year may be good, but not great." And by next year, he says, there may be a shakeout in the television industry that'll leave only five or six of the big manufacturers in business.

The figure to watch, say industry observers, is what comes out for September, the month that marked the beginning of the decline last year.

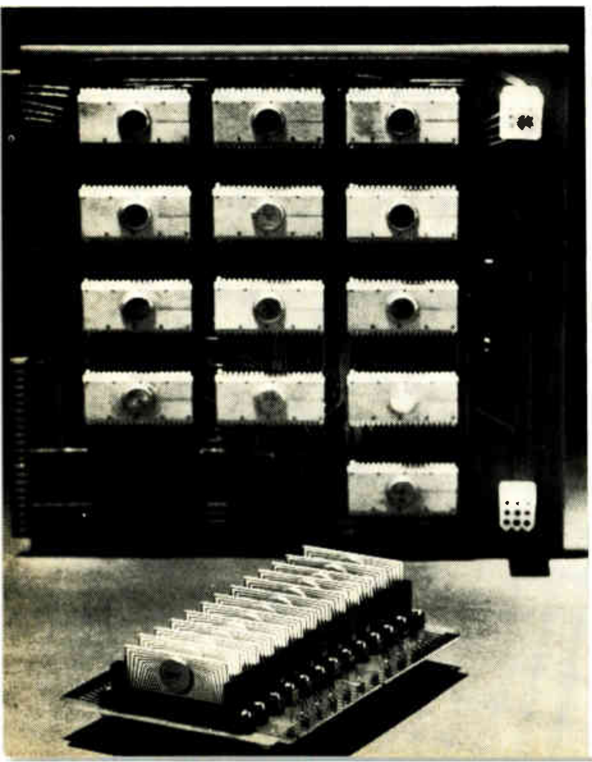
Packaging

How to save cost and real estate

Large-scale integration presents as much a problem in packaging as it does in design. Present 40-lead dual-in line packages that use lead frames are expensive and take up a lot of real estate on the printed circuit board. But a new leadless package, called the edge mount, may overcome these problems. It is being offered for MOS circuits made by American Micro Systems of Santa Clara, Calif.

The edge mount is a ceramic substrate with screened-on conductor patterns and gold-plated contacts at the edge to plug into an edge connector developed by Texas Instruments in Attleboro, Mass. The device is bonded on a pad on the substrate and leads are wire-bonded from the MOS device to the conductor pattern. Cost, including connector, is estimated at 50% less than for present packages. Pc board space required is nearly 40% lower.

Well stacked. Edge mounts take less space, allow better cooling than equivalent pc board assembly.



Lyle Irwin of AMI says that about 40% of the current 40-lead MOS circuits, which comprise about 60% of all AMI shipments, could use this package. AMI says there's nothing to stop other semiconductor manufacturers from using the package.

The key cost saving is in eliminating the lead frame used with the 40-lead dual in-line packages. DIP devices are not tested until after they are placed in the packages. This means if, as is typical, only half the devices are actually good, as many lead-frame packages are thrown away as are shipped. But under the edge-mount system, the device can be inserted in a connector in the test jig; if it fails, only the ceramic substrate is yielded along with the chip.

The edge-mount package, which is being made at Coors Porcelain Co., Golden, Colo., is made from a single layer of ceramic, rather than the three layers needed for the dual in-line.

The connector must be able to stand the highly abrasive ceramic during insertion and withdrawal. Standard gold plating over nickel would have given only about 30 connect-disconnect cycles before deterioration began, says Ray Larsen of TI. Therefore, TI's bonded stripe contacts (a thick gold inlay in the cantilevered contact) were used, raising the life to the 300-cycle range.

The package, which will be described by Irwin and Larsen in a paper at the Connector Conference Oct. 21 in Cherry Hill, N.J., has interesting possibilities: since it's installed upright, it's possible to use a two-sided substrate with a device on each side. In addition, the connector was designed for matched-impedance operation in high-speed systems. Even though this property is not needed for present MOS designs, it could be useful with high-speed bipolar circuits, such as emitter-coupled logic. The conductor patterns on the ceramic also lend themselves to high-speed circuits, since they are essentially microstrip lines when a ground plane is added on the opposite side.

Integrated electronics

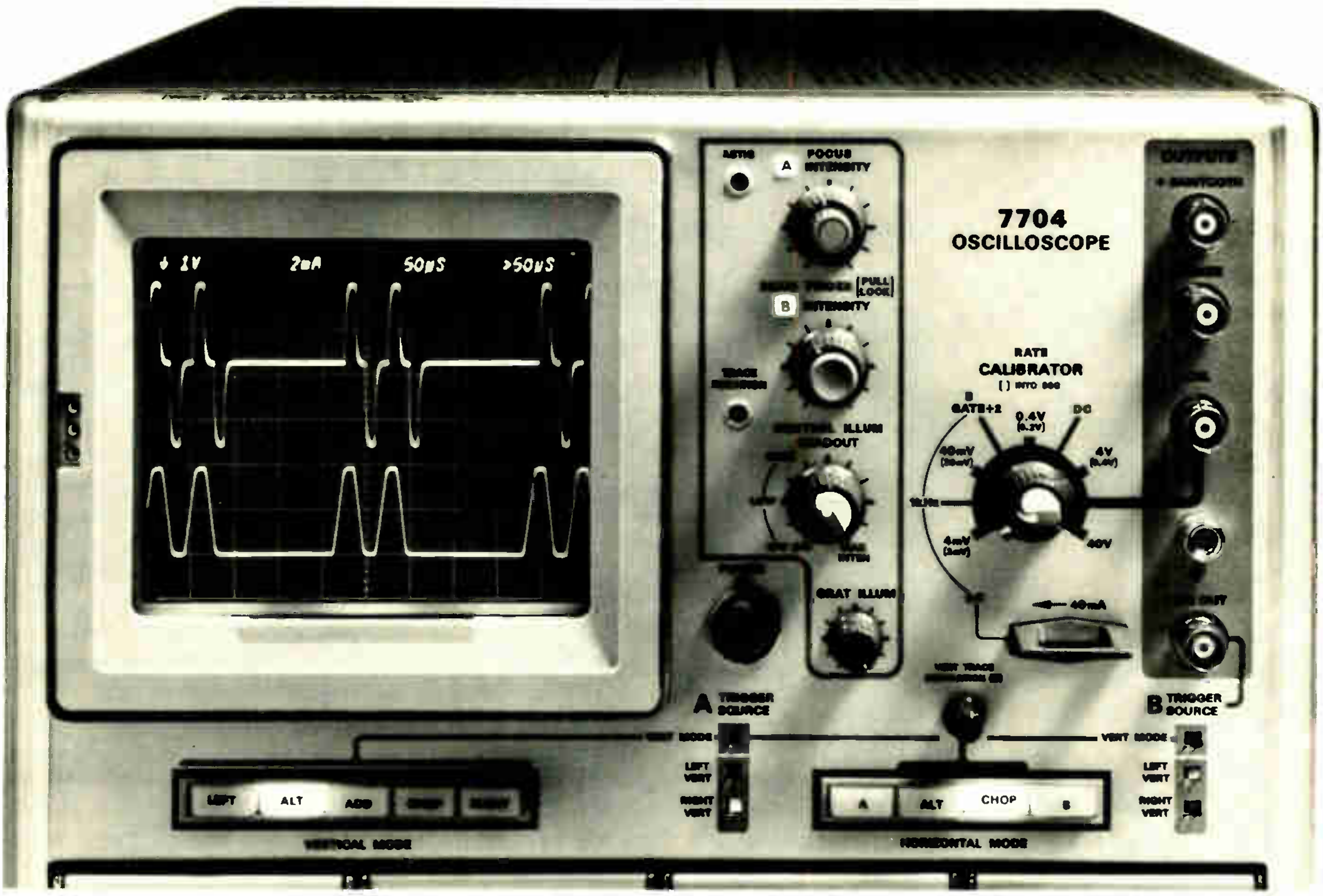
Metal-core board keeps heat off

The packing density of components on circuit boards is often limited by heat-dissipation problems. This means more size in equipment that might be shrunk if thermal dissipation were more efficient and there were no need for convection cooling with blowers and the familiar staggered-finger heat dissipators to which individual component packages are mounted. The International Electronic Research Corp. in Burbank, Calif., has attacked this problem with what it believes is the first true heat-dissipating metal-core circuit board.

Metal-core boards used in avionics hardware, for example, are inefficient heat dissipators. That's because they use a standard G-10 epoxy-fiberglass board cemented to an aluminum plate that serves as a heat sink, but the board itself acts as a thermal barrier between the heat-generating components and the heat-dissipating metal. So does the cement that bonds the board to the metal core. The IERC solution: a thermally conductive board that replaces the G-10.

IERC engineers say their metal pc board will dissipate four to five times more heat than a conventional board. "Then when you connect it in a good cold-wall system, you can put 12 to 15 times more power on it," says John McAdams, IERC's vice president for engineering. But it costs more, too.

IERC, which specializes in ther-



With Tektronix 7000-Series Oscilloscopes

versatility begins with the mainframe

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With mainframe versatility, and four plug-in capability, a wider range of measurements can be made with only one oscilloscope.

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Prices of instruments shown:

7704 150-MHz Four-Plug-In Oscilloscope	$2500
7A16 150-MHz Single-Trace Amplifier .	$ 600
7A14 105-MHz Current Amplifier	$ 575
7B71 Delaying Sweep Time Base	$ 685
7B70 Delayed Sweep Time Base	$ 600

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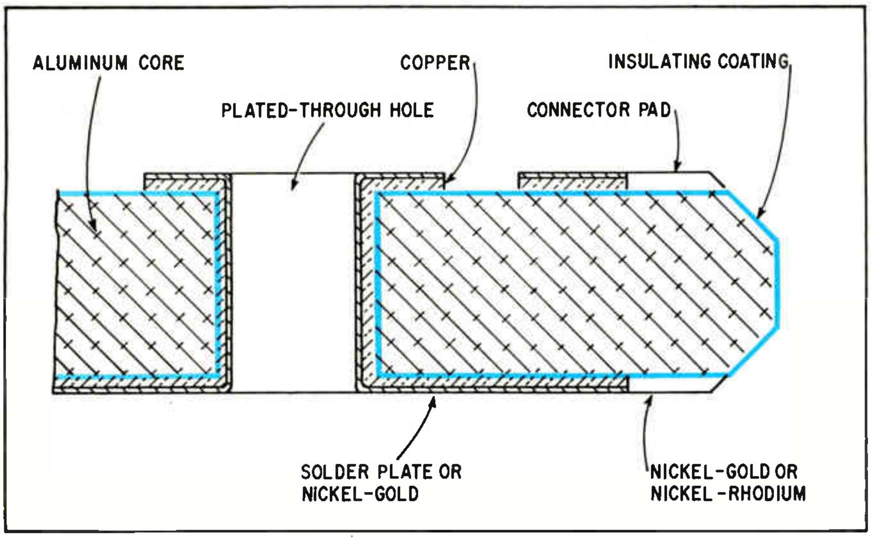


Cooler. Cross-section of IERC's aluminum-core circuit board shows composition of each layer. Insulating layer or dielectric is only 4 to 6 mils thick.

mal problems, also manufacturers the finned heat dissipators. For the metal-core board, the company begins with a commercially available aluminum alloy in which IERC drills all holes to the customer's specification. The 50-mil-thick aluminum then is spray-coated with Insultek, a proprietary dielectric material that will both electrically isolate components from the heat-dissipating board and thermally couple them to the metal board.

William Mueller, IERC senior scientist, explains that the board next gets a thin metal film to facilitate plating. Then a photoresist is applied over the entire board surface and only the customer's interconnect and hole pattern is exposed so that the interconnect lines and holes may be built up simultaneously by copper plating both sides and through holes.

The copper interconnect lines finally are plated with tin-lead, gold, or to the customer's specifications; the photoresist is removed, and the finished board is shipped to the customer, ready to accept his components.

An IERC metal-core circuit board will cost approximately five to seven times the cost of a G-10 board that sells in the $5 to $8 range; the differential drops to two or three times more for the IERC board when compared with a G-10 board costing $35. As production increases, IERC believes that the price will be competitive.

Manufacturing

Getting it all into one package

Trimmer resistors pop up everywhere in circuits using operational amplifiers, and for good reason: they're needed to make the extremely small adjustments of voltage and current that will insure that the op amp operates at peak performance. And since op amps often come in dual in-line packages (DIP) a number of trimmer manufacturers have also started packaging their wares in DIPs so the trimmers and op amps can be put onto circuit boards using the same assembly equipment.

Now the Amphenol Controls division of the Bunker Ramo Corp.—with some help from a customer—has come up with an even better idea for cutting assembly costs and improving packing density on DIP board assemblies. They've incorporated the trimmer and the additional discrete resistors in thick film form for biasing the op amp, as well as the op amp itself, into one DIP. The concept opens up many possible combinations for monolithic ICs and, perhaps, trimmer capacitors.

At present, the Janesville, Wis., facility is going ahead with the development of such ideas, but meanwhile the company is manufacturing just the basic trimmer-and-bias-resistor combination for introduction in December. One trimming potentiometer and five fixed resistors are contained in a standard plastic 14-lead DIP that will sell for about $3 in production quantities. The resistive elements are made of a new cermet material with a low 50 parts per million temperature coefficient over the —40°C to 85°C temperature range. Because the resistors are all deposited simultaneously and because they are all exposed to the same temperature environment within the package, their relative change in value with temperature variations is extremely small—temperature tracking is 10 ppm standard, 2 ppm on special order.

Resistance values of 10 ohms to 1 megohm will be available, with a 10% tolerance standard and a laser-adjusted ±1% tolerance on special order.

Amphenol's trimmer differs from previous DIP trimmers in that the resistor surface is parallel to the circuit board instead of perpendicular to it. This 90° rotation of the surface provided the added real estate to accommodate the fixed resistors or whatever IC chips it seems appropriate to incorporate. It also reduces the height of the trimmer package, making it identical to that of IC DIPs, and allowing for closer stacking of the printed circuit boards and easier conformal coating.

Memories

ROM programed by forging link

The increasing popularity of read-only memories has prompted many companies to look for ways to program the device in house. One

Circle 51 on reader service card→

method is to break a metal link by scratching it [*Electronics*, Aug. 17, p. 40]. Another is to pass a high current through the link and "burn" it away. But Joseph D. Rizzi, vice president of bipolar operations at the Intersil Memory Corp., Cupertino, Calif., says he has a better way. Instead of breaking a link, he makes one.

The process is called avalanche-induced migration, and with it, says Rizzi, "Electrical contact is made permanently, not broken." The process, for which Intersil Memory is seeking a patent, is triggered by a pulsed signal applied to the leads.

With avalanche-induced migration, the component is altered within the semiconductor bulk and the resultant contact is "extremely stable," says Rizzi. "Since no material is fused, the problem of contaminants is eliminated and the technique produces a reliable product." The other advantage is that no masking or fabrication steps are needed. "Unlike scratches or fusing, the characteristics of the formed contact can be precisely controlled and are very consistent," he claims.

According to Rizzi, the problem with scratching as a means of programing ROMs is that it "isn't sufficiently reliable to be a production technique even if the process is automated." Fusing also has its drawbacks, he says. "The process of producing a fusable link must be tightly controlled and requires steps that aren't needed in an ordinary IC process." And, he adds, when a link is fused, material is released inside the hermetically sealed package "and this can cause long-term reliability problems." Worst of all, sometimes the fused links flow back together after extended operation, changing the memory's truth table. "So while the fusable link approach does produce electrically alterable ROMs," asserts Rizzi, "the reliability of the altered device is questionable."

Presently, Intersil is producing a 256-bit ROM employing avalanche-induced migration. It's organized as a 32-word-by-8-bit array and has complete address decoding and output buffering. "And," says Rizzi, "it's pin-for-pin compatible with several existing products."

An unprogramed memory contains all zeros. Ones are programed by using the five address inputs to select the desired word and by pulsing the desired bit output. The programing can be done manually or by some automated means controlled by punched cards or tape.

Rizzi says the 256-bit ROM was built "to satisfy an existing market, but the concept also offers some distinct advantages for larger arrays. With some further development, the programable element, though currently as small as those in standard devices, could be significantly smaller, yet still use the same design rules and tolerances." A 2,048-bit ROM is next.

Commercial electronics

For identification, flash your hologram

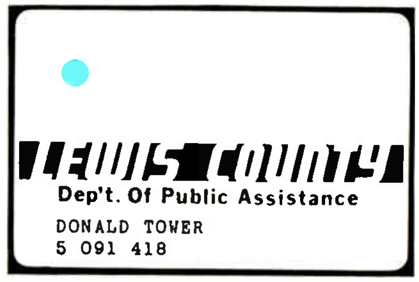
Identification of customers at banks and stores or of employees at security check points is possible with a new hologram and pulsed laser display combination recently developed by a small California manufacturer [*Electronics*, Sept. 28, p. 34].

Using a tiny hologram cut into a standard plastic credit card, the shoebox-sized display shows the bearer's name, signature, and other identifying information on a small screen. The hologram can include a picture of fingerprint of the individual as well.

Developer ICV Inc. of San Jose makes the holograms from information supplied by the user either from typed forms or directly from microfilm. The card can't be read without the laser display; if necessary, ICV will prepare a "scrambled" hologram that can only be read on its own units.

The display weighs about 15 pounds and measures 8 by 12 by 16 inches. Designed to sell for $650

Window. Circle at upper left is hologram containing credit information.



in 100 quantities, it features a helium neon laser operating at 2 milliwatts. Identification cards cost from 50 cents to $1 depending on quantity and amount of information included.

Also in the works is a more elaborate reader with a stored data. This unit handles credit verification or calls up special instructions from holograms stored on a 3.5-inch-square film inside. Right now, ICV can get 100,000 to 200,000 separate accounts on a sheet, but expects to be able to store up to two million for production units. This sheet would be updated weekly or monthly, depending on the application.

The credit verifier requires a card with two overlaid holograms. When inserted into the display, one appears on the screen for identification and the other deflects laser energy to select the stored information, which is flashed to the screen via a detector array in the system.

The key to getting its displays down in size and weight for counter-top use was a change earlier this year from a single to a multimode laser. This permitted more power in a smaller package. The next step may be solid state lasers.

Instrumentation

Market for detectors beginning to takeoff

Markets come and markets go. But while it lasts, the market for electronic sensors to detect sky-

Here's important news for every cost-conscious designer—RCA's COS/MOS line in dual-in-line plastic packages, at prices you can't afford to overlook.

This new COS/MOS line, RCA's CD4000E series, offers a broad range of gate-level and MSI devices with the low-power, high-noise-immunity features of hermetically packaged COS/MOS devices. And this plastic package gives you a broad operating temperature range and built-in reliability for industrial, commercial, and consumer applications. Look into RCA's CD4000E series for automotive systems, appliances, avionics applications, alarm systems, communications equipment, computers, industrial controls, and instrumentation.

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- ☐ Operation from single unregulated voltage supply: 5 to 15 V range
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- ☐ Speed Gates—propagation delay (t_{pd}) = 50 ns (typ) @ V_{DD} = 10 V, C_L = 15 pF MSI circuits—clock pulse frequency (f_{CL}) = 2.5 MHz (typ) @ V_{DD} = 10 V
- ☐ Single phase clock
- ☐ Clock voltage equal to supply voltage
- ☐ Compatible gate level and MSI functions
- ☐ Protected inputs and outputs

For further information, see your local RCA Representative or RCA Distributor. Ask for technical bulletin File No. 445, and the following publications: "RCA CD4000E Series COS/MOS IC Reliability Data," RIC 103; "Counters and Registers," ST-4166; "Noise Immunity," ICAN-6176; "Astable and Monostable Oscillator Designs," ICAN-6267. Or write: RCA, Commercial Engineering, Section 70J-12/CD47, Harrison, New Jersey 07029. International: RCA, 2-4 rue du Lièvre, 1227 Geneva, Switzerland, or P.O. Box 112, Hong Kong.

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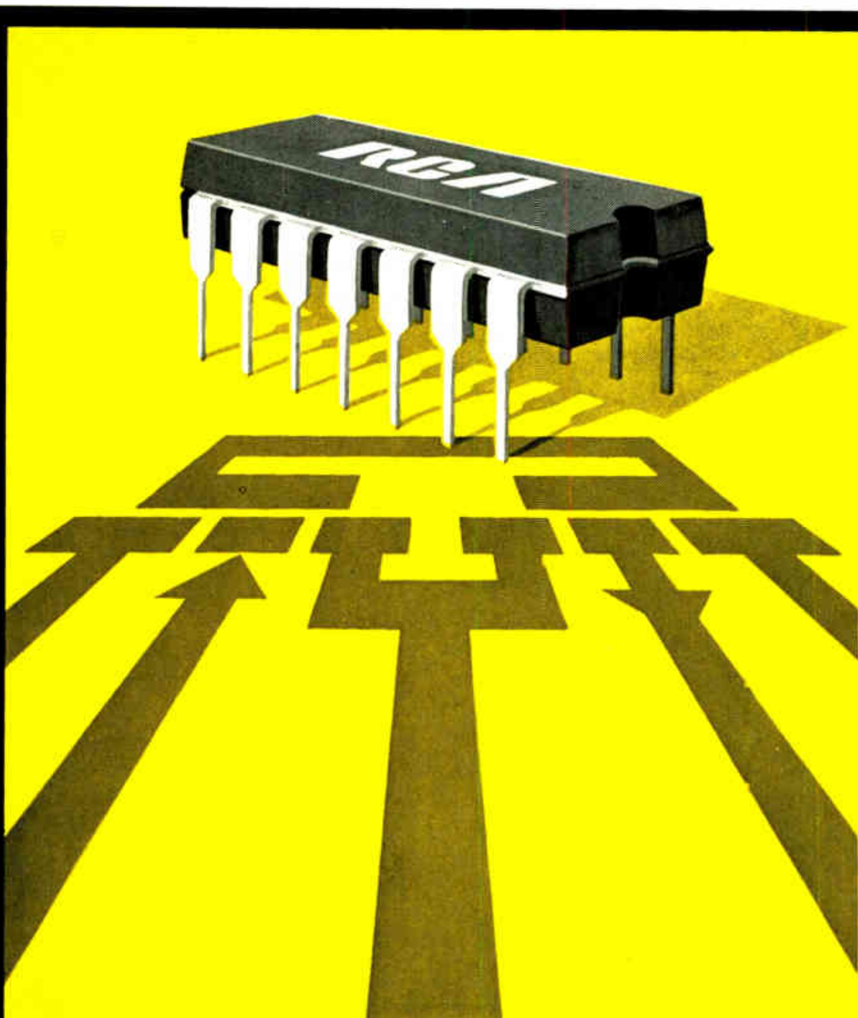


TYPE	DESCRIPTION	PRICE (1000 Unit level)
Gates		
CD4000E	Dual 3-input NOR plus inverter	$2.20
CD4001E	Quad 2-input NOR	2.30
CD4002E	Dual 4-input NOR	2.50
CD4007E	Dual complementary pair plus inverter	2.30
CD4011E	Quad 2-input NAND	2.30
CD4012E	Dual 4-input NAND	2.50
CD4019E	Quad AND-OR select gate	3.70
Flip-Flops		
CD4013E	Dual "D" with set/reset capability	3.30
Hex Buffers/Logic-Level Converters		
CD4009E	Inverting	3.60
CD4010E	Non-inverting	3.60
Multiplexer		
CD4016E	Quad bilateral switch	3.30
Static-Shift Registers—MSI		
CD4006E	18-stage register	7.75
CD4014E	8-stage synchronous parallel or serial-input/serial-output	7.75
CD4015E	Dual 4-stage serial-input/parallel-output	7.75
Counters—MSI		
CD4004E	7-stage ripple counter/frequency divider	5.60
CD4017E	Decade counter/divider with 10 decoded outputs	8.00
CD4018E	Presettable divide-by "N" counter	7.00
CD4020E	14-stage ripple-carry binary counter/divider	9.50
Adder—MSI		
CD4008E	4-bit binary full-adder with parallel carry-out	7.50

RCA
Integrated Circuits

Circle 53 on reader service card

jacker weapons may become a real high flyer. Companies rushing to market with new products to meet the airlines' needs cover the spectrum from giant corporations to small, new outfits operating out of a garage. Among the latest entries is Westinghouse Electric and the three-man SPS Corp. of Garland, Texas.

Although details of most of the new devices are not released for security reasons, they both differ from the passive magnetometers offered by the leaders in the field—Infinetics Inc. and Schonstedt Instruments Co. [*Electronics*, Sept. 28, p. 93]—in that they generate their own magnetic or electromagnetic field instead of relying on changes in the flux of the earth's magnetic field.

The new Westinghouse Detector, for example, uses an alternating current magnetic gate 3 by 7 by 3 feet through which airline passengers move at normal walking speed. The firm says its system detects and identifies weapons of small size and mass but ignores common objects, such as radios, cameras, keys, and acrosal cans.

Top airlines security officials, however, aren't so sure that the Westinghouse device will find its way into airports for some time. "It's only a theory right now," says one airline source. "I haven't seen it yet, and they've told me they can't show it for six months."

Another device, also described as an active unit by the four-month-old SPS Corp. is portable, thus permitting random deployment. Tom Allen, the firm's president, describes the system, dubbed WD 100, as a shoebox-sized package with a sensor about the size of a ping-pong ball. He says it uses both the earth's magnetic field and its own field to detect ferrous metals. The battery-powered unit will sell for $1,000.

Meanwhile, the Federal Aviation Administration is looking further down the road for the ideal device. It has recently signed a $106,000 contract with the Bendix Corp.'s Aerospace Systems division to develop a magnetic screening device that will pinpoint suspicious metallic objects. Suspects would then be led through a short pulse X-ray machine that would examine both their luggage and their bodies for the outlines of suspicious devices. The unit's X-ray pulse would be so short and safe that it wouldn't even expose film, sources say.

Airline security officers say that the device could also be used to spot explosives. They add that a similar device is now under development by North American Phillips Broadcasting Electronics Group. Yet the high cost of the units may restrict their use.

Computers

RAM's design aims at mainframes

The announcement by IBM that its new model 370/145 computer will have a semiconductor mainframe memory [see p. 125] couldn't have been timed better as far as the Intel Corp. is concerned. Last week the Mountain View, Calif., firm introduced its 1,024-bit metal oxide semiconductor random access memory—a memory that's designed for mainframe applications at a mainframe price of under a penny a bit.

The penny-a-bit price for a RAM has long been the siren song of the semiconductor memory people. It's at this price level that semiconductor memories can be competitive with core, but computer designers had become somewhat cynical about how soon such prices would be realized.

"We're going after mainframe cores," says Robert Graham, vice president and director of marketing at Intel, "and we've got the memory to do it." Intel's RAM is a fully decoded silicon gate device with an access time of 300 nanoseconds and a cycle time of 600 ns; it's packaged in an 18-pin plastic dual in-line package. Pricing for the unit is on a sliding scale that starts at $38.40 for 100 devices and then drops to $20 for the first 5,000 units, $15 for the next 10,000, $10 for the next 25,000, and so on down to $5 in quantities of one million devices. And Graham makes no bones about it; once the unit gets designed into mainframes, Intel expects to be selling them by the millions.

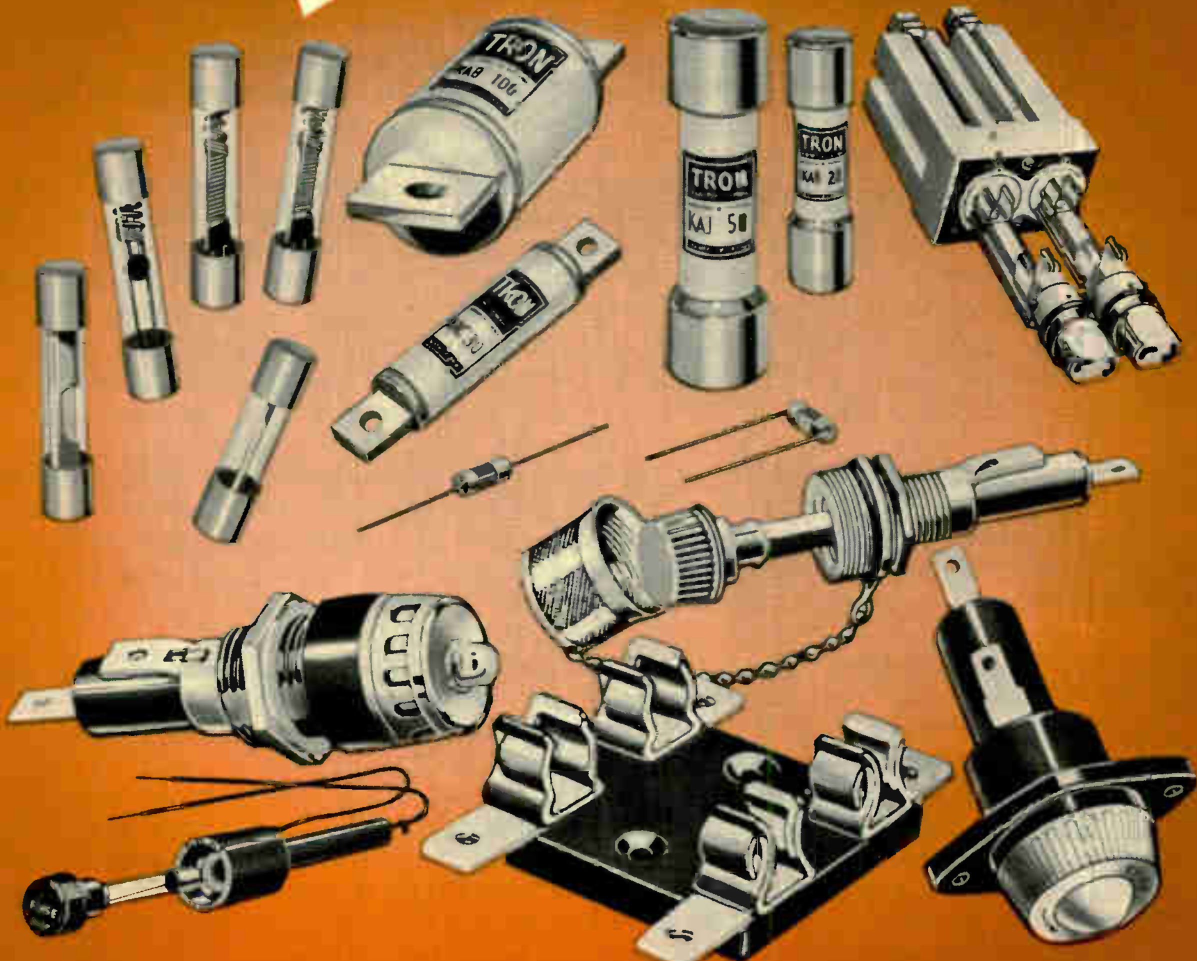
"Because there are so many people in the semiconductor memory business," says Graham, "the way to succeed is to be the guy that gets designed in. You've got to get your product to be the universal one: the one that the other guys have to build. We think our spec is right, and we know our price is right."

Like many companies in the semiconductor industry, Intel suffered heavy losses this summer, but unlike most, the company, is ahead of its plan. For the first six months of 1970, Intel lost $900,000 on sales of $1.5-million. But most Bay Area memory watchers (both financial and technical) agree that this is not unusual for a young company that is as heavily committed to R&D as Intel is; it's present rate is about 30% of sales. According to Graham, the company's plan called for it to show a profit in the first quarter of 1971, "but we're ahead of schedule. We expect to show a net profit of about $150,000 this month."

Solid state

MOS arrays remember organist's stop

Capture-combination systems for organs have been used since 1889. They store and recall combinations of stop settings that the organist has preset to create a desired tone to produce a sequence of notes, or to make the organ imitate other musical instruments. But mechanical or electromechanical models are usually quite bulky, require a large power supply, and have a small memory. Those are the limitations that engineers at North American Rockwell Microelectronics Co. attacked in designing a new



kind of system for the Allen Organ Co., Macungie, Pa.

It's built around MOS/LSI arrays, but also contains 420 or 550 discrete components which the Anaheim, Calif., company will not make but buy to NMREC specs.

All the elements are assembled onto a single 10-by-14-inch circuit board, which can be mounted in the organ's console, an impossibility with mechanical techniques. One version to be offered by Allen controls 24-stop combinations, and an extended version controls 34. Either may also be retrofitted to organs already in use—both electronic organs and pipe organs can be adapted without major revisions.

Two kinds of MOS chips are used. One is a hex 80-bit shift register that also contains a two-phase clock generator and a 2-to-4 phase clock converter, and the other's a control chip that provides reference timing for the entire system, including the shift register chips. Two of the shift register chips are used in the 24-stop-combination version, three in the extended unit. Only one control chip is needed for either unit (it contains address decoding and multiplexing for selecting the appropriate shift register). Apart from the chips, there are two diode matrixes, the power supply, and a set of relays.

The system will sell for approximately half the $4,000 that electromechanical capture-combination units generally cost.

For the record

F-15 avionics. Hughes Aircraft Co., with an $82.6 million initial contract for development and test of the Air Force's F-15 air superiority fighter, tops the list of six avionics suppliers to prime contractor McDonnell Douglas Corp. Hughes defeated Westinghouse Electric in the flyoff competition for the lightweight, semi-automatic system for tracking and targeting aircraft at all altitudes down to treetop levels.

Other subcontractors are Conductron Corp., with $6.4 million to develop the head-up radar display; Hoffman Electronics with $1.38 million to provide the first 18 microminiaturized tactical air navigation (Tacan) systems for reproduction tests; Bendix Corp.'s Navigation and Control division, with $700,000 for the lead gyro computing system, including a digital computer, force-balance accelerometer, and a two-degree-of-freedom gyro. Also, Collins Radio Co. has received $770,000 for AN/ARC-109 uhf transceivers for the first planes, while Brunswick Corp. will develop the nose radome with a $590,000 award.

TI lays off 1,210. Since its emergence as a major semiconductor company, Texas Instruments has gone to great lengths to avoid mass layoffs. But despite short work weeks and other measures, the company has reduced its Dallas work force by 1,210.

Not for sale. Aerojet-General has "no plans to go into the commercial component business," says executive vice president Allen Grant. The firm's Azusa, Calif., Electronics division will not market the thin film ICs it has been working on in the labs [*Electronics*, Sept. 28, p. 33]. Indications earlier were that Aerojet had decided to go into the components business with the thin film ICs.

Principally a subsystems and systems house, the Aerojet division is working almost entirely in the sensors and data systems areas. Its thin films circuit operation exclusively supports in-house systems work. Currently it is building a hybrid amplifier circuit—thin film passives and flip chip devices—for the signal processing in a classified military infrared system. The lab isn't doing any work presently on active thin film devices.

Modular monitor. What one industry source calls the next generation in patient-monitoring systems will probably be introduced by the Abbot Medical Electronics

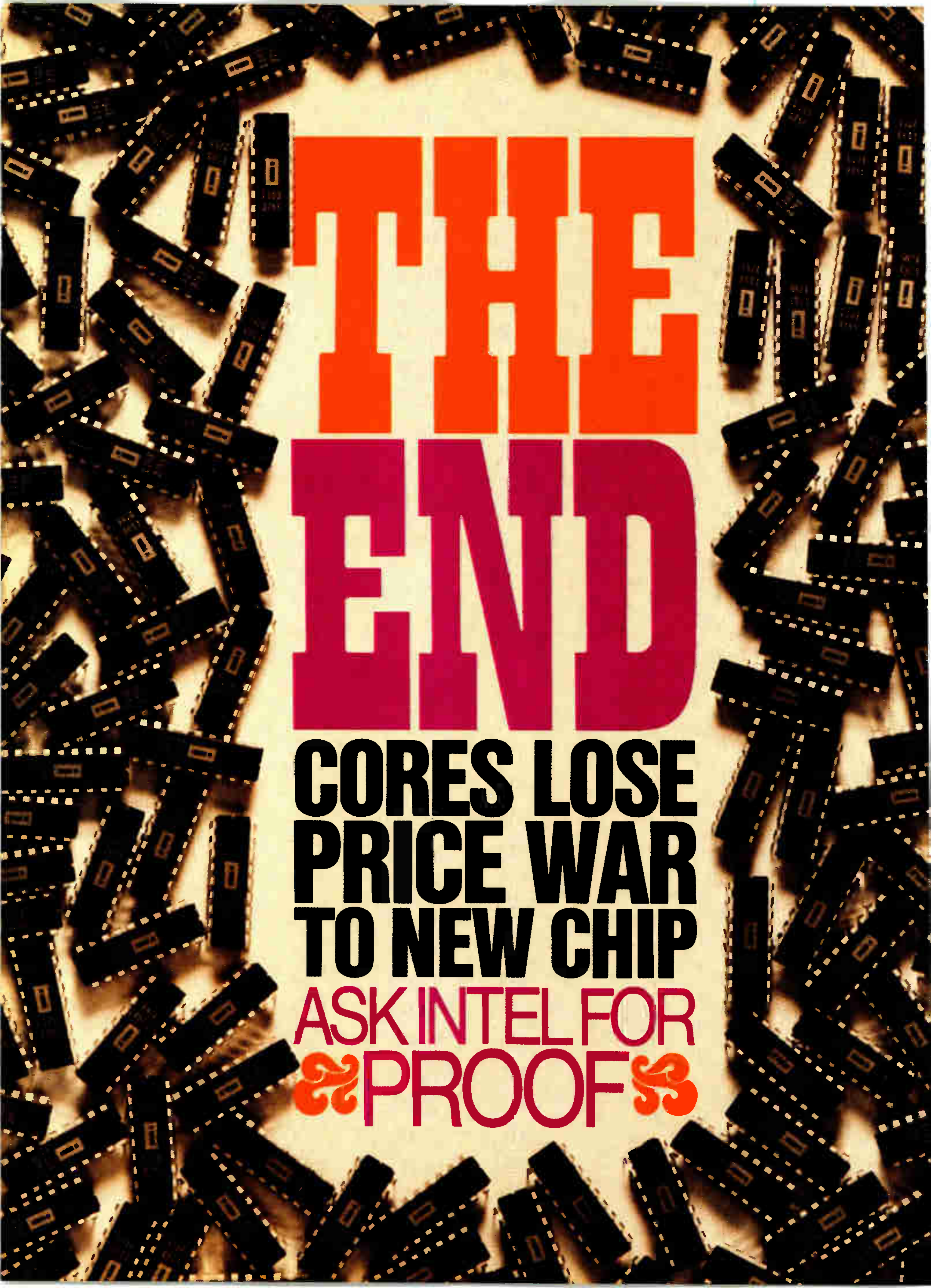
Co. of Chicago at the American Heart Association Show in November. The new units are to be made with sealed modules, and sold with replacement plug-ins for every module type. In addition, Abbot's system is expected to have a limited self-test ability. A separate module will continually check frequency response, leakage current, and the paper speed of strip-chart recorders. The goal of the modular approach is easier maintenance.

New 4 Pi. IBM has developed a successor to its medium-sized 4 Pi CP-2 airborne computer which it says offers twice the speed and communications capability at the same price. Called the 4 Pi AP, the new model already is earmarked for the Air Force's F-15 air superiority fighter. It occupies 0.89 cubic foot compared to 0.78 for its predecessor.

New entry. The Burroughs Corp. has joined the Great 1970 Computer Derby in competition with IBM, National Cash Register, and RCA, (Univac also is about to announce). Burroughs has introduced three new computers called the 700 Series, and hints that more will follow. The three, called the 5700, 6700, and 7700, are growth versions of Burroughs' older 5500 and 6500 systems, but represent some significant new advances.

All three are available in multiprocessing systems containing from two to eight central processors and varying configurations of interleaved memory modules and input-output channels and processors. The 6700 offers three memory levels, while the 7700 has a semiconductor buffer memory.

Also announced with the 700 series were two new lines of magnetic disk auxiliary storage units, one big, fast, and presumably expensive, and one smaller, slower, and cheaper. The fast ones use Burroughs' tried and true head-per-track design, the inexpensive ones use disk packs and have movable heads that are driven magnetically much the same way as a loudspeaker. This is an unusual technique but it's not new.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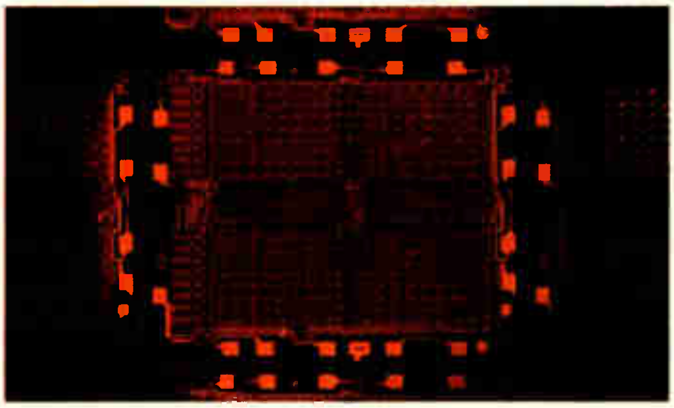

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Kokomoan's Regional Headquarters. Union, New Jersey* 07083, Box 1018 Chestnut Station, (201)-687-3770 ■ Chicago, Illinois* 60656, 5151 N. Harlem Avenue, (312)-775-5411 ■ Kokomo, Ind. 46901, 700 E. Firmin, (317)-459-2175 Home Office ■ **Office includes field lab and resident engineer for application assistance.*

MSI/TTL CIRCUITS:

DECODERS

- SN54/7442 BCD-to-Decimal Decoder*
- SN54/7443 Excess-3-to-Decimal Decoder*
- SN54/7444 Excess-3-Gray-to-Decimal Decoder*
- SN54/7445 BCD-to-Decimal Decoder/Driver*
- SN54/7446 BCD-to-7-Segment Decoder/Driver*(30V)
- SN54/7447 BCD-to-7-Segment Decoder/Driver*(15V)
- SN54/7448 BCD-to-7-Segment Decoder*
- SN54/7449 BCD-to-7-Segment Decoder*
- ■ SN54/74141 BCD-to-Decimal Decoder/Driver*
- SN54/74145 BCD-to-Decimal Decoder/Driver*
- SN54/74154 4-to-16-Line Decoder/Demultiplexer*
- ■ SN54/74155 Dual 2-to-4-Line Decoder/Demultiplexer
- ■ SN54/74156 Dual 2-to-4-Line Decoder/Demultiplexer (O-C)

MEMORIES/LATCHES

- SN54/7475 Quad Bistable Latch*
- SN54/7477 Quad Bistable Latch*
- SN54/7481 16-Bit RAM*
- SN54/7484 16-Bit RAM, Gated Write Inputs*
- ■ SN54/7488 256-Bit ROM, Custom Programmed*
- SN7489 64-Bit RAM*
- SN54/74100 Dual Quad Bistable Latch
- ■ SN54/74170 4-by-4 Register File (Buffer Memory)

ARITHMETIC ELEMENTS

- SN54/7480 Gated Full Adder*
- SN54/7482 2-Bit Binary Full Adder*
- SN54/7483 4-Bit Binary Full Adder*
- ■ SN54/7485 4-Bit Magnitude Comparator
- ■ SN54/74L85 4-Bit Magnitude Comparator*
- SN54/7486 Quad 2-Input Exclusive-OR*
- SN54/74L86 Quad 2-Input Exclusive-OR*
- SN54/74H87 4-Bit True/Complement*
- ■ SN54/74181 4-Bit Arithmetic Logic Unit, Function Generator*
- ■ SN54/74182 Look-Ahead for Arithmetic Logic Unit*
- ■ SN54/74H183 Dual Carry-Save Full Adder

■ New circuit introduced 1970 ★Multi-source product

SHIFT REGISTERS

- SN54/7491A 8-Bit*
- SN54/74L91 8-Bit
- SN54/7494 4-Bit (Parallel-In, Serial-Out)*
- SN54/7495 4-Bit Universal*
- SN54/74L95 4-Bit Universal*
- SN54/7496 5-Bit (Dual Parallel-In/Out)*
- SN54/74L98 4-Bit Data Selector/Storage Register
- SN54/74L99 4-Bit Universal
- ■ SN54/74164 8-Bit Serial-In, Parallel-Out*
- ■ SN54/74165 8-Bit Parallel-In, Serial-Out*
- ■ SN54/74166 Synchronous Parallel-Load 8-Bit
- ■ SN54/74198 Universal 8-Bit Parallel-In/Out, Left/Right
- ■ SN54/74199 8-Bit Parallel-In/Out, J-K Inputs

DATA SELECTORS/MULTIPLEXERS

- SN54/74150 16-Bit Data Selector*
- SN54/74151 8-Bit Data Selector*
- SN54/74152 8-Bit Data Selector
- SN54/74153 Dual 4-to-1-Line Data Sel./Multiplexer*

COUNTERS

- SN54/7490 Decade*
- SN54/74L90 Decade
- SN54/7492 Divide-by-12*
- SN54/7493 4-Bit Binary*
- SN54/74L93 4-Bit Binary*
- ■ SN54/74160 Synchronous 4-Bit Decade*
- ■ SN54/74161 Synchronous 4-Bit Binary*
- ■ SN54/74162 Fully Synchronous 4-Bit Decade
- ■ SN54/74163 Fully Synchronous 4-Bit Binary
- ■ SN54/74190 Synchronous 4-Bit Up/Down Decade, 1-Line Mode Control*
- ■ SN54/74191 Synchronous 4-Bit Up/Down Binary, 1-Line Mode Control*
- ■ SN54/74192 Synchronous 4-Bit Up/Down Decade*
- ■ SN54/74193 Synchronous 4-Bit Up/Down Binary*
- ■ SN54/74196 Asynchronous Presettable Decade*
- ■ SN54/74197 Asynchronous Presettable Binary*

PARITY GENERATOR

- SN54/74180 8-Bit Parity Generator/Checker

SCHOTTKY-CLAMPED TTL CIRCUITS:

These represent the latest development in TTL integrated circuits. A totally new technology, TI's Schottky-clamped TTL circuits combine the high speed of unsaturated logic and the low power of TTL saturated logic: 3 ns at 20 mW. Here's a brand-new list of recently announced devices. For more information on this fastest TTL family, circle 191 on the Reader Service Card.

- ■ SN74S00 Quad 2-Input Positive NAND Gate
- ■ SN74S03 Quad 2-Input NAND Gate, Open-Collector Output
- ■ SN74S04 Hex Inverter
- ■ SN74S10 Triple 3-Input NAND Gate
- ■ SN74S11 Triple 3-Input AND Gate
- ■ SN74S15 Triple 3-Input AND Gate, Open-Collector Output
- ■ SN74S20 Dual 4-Input Positive NAND Gate
- ■ SN74S22 Dual 4-Input NAND Gate, Open-Collector Output
- ■ SN74S40 Dual 4-Input NAND Buffer
- ■ SN74S64 4-2-2-3-Input AND-OR-INVERT Gate
- ■ SN74S65 4-2-2-3-Input AND-OR-INVERT Gate, Open-Collector Output
- ■ SN74S112 Dual J-K Negative-Edge Triggered Flip-Flop, Separate Preset, Clear and Clock
- ■ SN74S140 Dual 4-Input NAND Line Driver

SSI/TTL CIRCUITS:

STANDARD SSI CIRCUITS

- SN54/7400 Quad 2-Input NAND Gate*
- SN54/7401 Quad 2-Input NAND Gate, Open-Collector Output*
- SN54/7402 Quad 2-Input NOR Gate*
- SN54/7403 Quad 2-Input NAND Gate, Open-Collector Output*
- SN54/7404 Hex Inverter*
- SN54/7405 Hex Inverter, Open-Collector Output*
- ■ SN54/7406 Hex Inverter Buffer/Driver, Open-Collector High-Voltage Output
- ■ SN54/7407 Hex Buffer/Driver, Open-Collector High-Voltage Output
- ■ SN54/7408 Quad 2-Input Positive AND Gate*
- ■ SN54/7409 Quad 2-Input Positive AND Gate*
- SN54/7410 Triple 3-Input NAND Gate*
- ■ SN54/7412 Triple 3-Input NAND Gate, Open-Collector Output
- ■ SN54/7413 Dual 4-Input NAND Schmitt Trigger*
- ■ SN54/7416 Hex Inverter Buffer/Driver, Open-Collector High-Voltage Output
- ■ SN54/7417 Hex Buffer/Driver, Open-Collector High-Voltage Output
- ■ SN54/7420 Dual 4-Input NAND Gate*
- ■ SN54/7423 Expandable Dual 4-Input Positive NOR Gate with Enable
- ■ SN54/7425 Dual 4-Input Positive NOR Gate with Enable*
- ■ SN54/7426 Quad 2-Input High-Voltage Interface NAND Gate*
- ■ SN54/7427 Triple 3-Input NOR Gate*
- SN54/7430 8-Input NAND Gate*
- ■ SN54/7432 Quad 2-Input OR Gate*
- ■ SN54/7437 Quad 2-Input NAND Buffer*
- ■ SN54/7438 Quad 2-Input NAND Buffer with Open-Collector Output
- SN54/7440 Dual 4-Input NAND Buffer*
- SN54/7450 Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate*
- SN54/7451 Dual 2-Wide 2-Input AND-OR-INVERT Gate*
- SN54/7453 Expandable 4-Wide 2-Input AND-OR-INVERT Gate*
- SN54/7454 4-Wide 2-Input AND-OR-INVERT Gate*
- SN54/7460 Dual 4-Input Expander*
- SN54/7470 J-K Flip-Flop*
- SN54/7472 J-K Master-Slave Flip-Flop*
- SN54/7473 Dual J-K Master-Slave Flip-Flop*
- SN54/7474 Dual D-Type Edge-Triggered Flip-Flop*
- SN54/7476 Dual J-K Master-Slave Flip-Flop, Preset and Clear*
- SN54/74104 Gated J-K Master-Slave Flip-Flop*
- SN54/74105 Gated J-K Master-Slave Flip-Flop*
- SN54/74107 Dual J-K Master-Slave Flip-Flop, Preset and Clear*
- ■ SN54/74110 Gated J-K Master-Slave Flip-Flop, Data Lockout
- ■ SN54/74111 Dual J-K Master-Slave Flip-Flop, Data Lockout
- SN54/74121 Monostable Multivibrator*
- ■ SN54/74122 Retriggerable Resettable Monostable Multivibrator*
- ■ SN54/74123 Dual Retriggerable Resettable One-Shot*

HIGH-SPEED SSI CIRCUITS

- SN54/74H00 Quad 2-Input NAND Gate*
- SN54/74H01 Quad 2-Input NAND Gate, Open-Collector Output*
- SN54/74H04 Hex Inverter*
- SN54/74H05 Hex Inverter, Open-Collector Output*
- SN54/74H10 Triple 3-Input NAND Gate*
- SN54/74H11 Triple 3-Input AND Gate*
- SN54/74H20 Dual 4-Input NAND Gate*
- SN54/74H21 Dual 4-Input AND Gate*
- SN54/74H22 Dual 4-Input NAND Gate, Open-Collector Output*
- SN54/74H30 8-Input NAND Gate*
- SN54/74H40 Dual 4-Input NAND Buffer*
- SN54/74H50 Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate*
- SN54/74H51 Dual 2-Wide 2-Input AND-OR-INVERT Gate*
- SN54/74H52 Expandable 4-Wide 2-2-2-3-Input AND-OR Gate*
- SN54/74H53 Expandable 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate*
- SN54/74H54 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate*
- SN54/74H55 Expandable 2-Wide 4-Input AND-OR-INVERT Gate*
- SN54/74H60 Dual 4-Input Expander*
- SN54/74H61 Triple 3-Input Expander*
- SN54/74H62 4-Wide 3-2-2-3-Input AND-OR Expander*
- SN54/74H71 J-K Flip-Flop with AND-OR Input*
- SN54/74H72 J-K Master-Slave Flip-Flop*
- SN54/74H73 Dual J-K Flip-Flop, Separate Clock*
- SN54/74H74 Dual D-Type Edge-Triggered Flip-Flop*
- SN54/74H76 Dual J-K Flip-Flop, Preset and Clear Inputs*
- SN54/74H78 Dual J-K Flip-Flop, Preset and Clear Inputs*
- SN54/74H101 J-K Flip-Flop, AND-OR Inputs
- SN54/74H102 J-K Flip-Flop, AND Inputs
- SN54/74H103 Dual J-K Flip-Flop, Separate Clock Inputs
- SN54/74H106 Dual J-K Flip-Flop, Preset and Clear Inputs
- SN54/74H108 Dual J-K Flip-Flop, Preset and Clear Inputs

LOW-POWER SSI CIRCUITS

- SN54/74L00 Quad 2-Input NAND Gate*
- ■ SN54/74L01 Quad 2-Input NAND Gate, Open-Collector Output
- ■ SN54/74L02 Quad 2-Input NOR Gate
- ■ SN54/74L03 Quad 2-Input NAND Gate, Open-Collector Output
- SN54/74L04 Hex Inverter*
- SN54/74L10 Triple 3-Input NAND Gate*
- SN54/74L20 Dual 4-Input NAND Gate*
- SN54/74L30 Single 8-Input NAND Gate*
- SN54/74L51 Dual 2-Wide 2-Input/2-Wide 3-Input AND-OR-INVERT Gate*
- SN54/74L54 2-2-3-3-Input AND-OR-INVERT Gate*
- SN54/74L55 2-Wide 4-Input AND-OR-INVERT Gate*
- SN54/74L71 R-S Master-Slave Flip-Flop*
- SN54/74L72 J-K Master-Slave Flip-Flop*
- SN54/74L73 Dual J-K Master-Slave Flip-Flop*
- SN54/74L74 Dual D-Type Edge-Triggered Flip-Flop*
- SN54/74L78 Dual J-K Master-Slave Flip-Flop, Common Clear and Clock*

■ New circuit introduced 1970 ★Multi-source product

Looking for low-cost solutions to high-performance design problems?

You'll find a lot of new ones in TI's 54/74 line —still your broadest choice of state-of-the-art TTL integrated circuits.

If you're going to design the best equipment for your customers, you need the best tools available. Design after design has proven TTL the top logic tool from a standpoint of circuit efficiency and cost effectiveness.

Not for your state-of-the-art system? Look again. A lot has happened in the last few months. Enough to justify a careful review of your latest logic diagrams and product plans.

Take another look at the TTL leader—TI's 54/74 family.

MSI choice and complexity. Begin with the opposite page. Here, to help you reduce package count, simplify designs and improve performance, is an unmatched array of catalog MSI functions. The line has just about doubled in the past nine months and there are still more to come of ever-increasing complexity.

SSI back-up in depth. But in using TTL/MSI, you need the substantial back-up of versatile SSI circuits. Check the opposite page again.

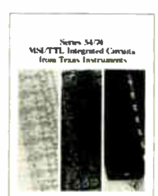
Four speed/power choices. Within TI's big TTL family, you have a selection of four speed/power ranges to help optimize your designs. There are 1 mW per gate low power circuits, standard- and high-speed circuits *plus* the revolutionary new Schottky-clamped TTL functions which attain speeds of 3 ns at 20 mW.

Complete compatibility. Even with this wide choice, you avoid compatibility problems. All members of TI's Series 54/74 family are designed to work together—saving you both design and component costs.

And TTL logic is also most economical on the basis of cost-per-function...in whatever package types you need: ceramic and plastic DIP or flat pack.

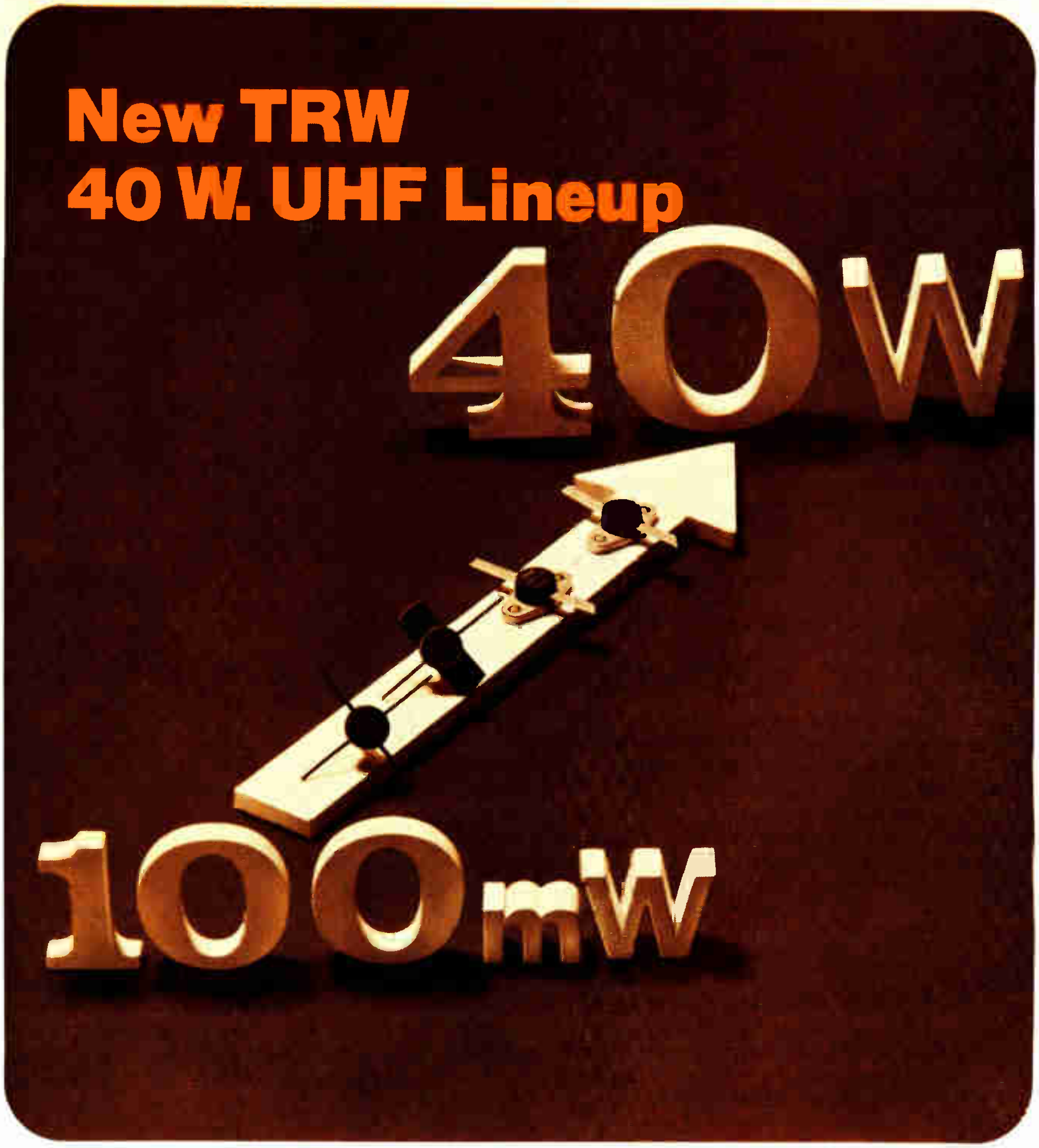
Ready availability. Not only has TI significantly increased its TTL production capacity, but we maintain large factory inventories (averaging more than 150,000 MSI parts alone) in all three packages and in both temperature ranges. More than 100 authorized distributor locations stock full inventories of TI's TTL circuits...representing an additional stock, in the field, of more than 300,000 MSI parts.

And if your system requires multiple sources, you'll find more of TI's 54/74 line is backed up by other reputable semiconductor suppliers. It makes good business sense. (Asterisks on opposite page indicate multiple-source devices.)



The time is now to consider TTL for today and tomorrow. The decision-making facts are in our new MSI brochure, CB-125. For your copy, circle 189 on the Reader Service Card or write Texas Instruments Incorporated, P.O. Box 5012, M.S. 308, Dallas, Texas 75222. Your authorized TI Distributor has copies, too.

TEXAS INSTRUMENTS
INCORPORATED



8-70

...optimized for bandwidth, ruggedness, and power gain

A new TRW series of four ruggedized UHF transistors makes 40 watts of output power available across the full 225-400 MHz band. The lineup can be varied to meet precise input and output requirements.

Ruggedized for performance under severe mismatch conditions, these 24-28 volt 'building blocks" provide high uniformity, reduce or eliminate variable circuit elements...and cost less. And the 1.5 W. 2N5773, 8 W. 2N5774, 20 W. 2N5775, and 40 W. 2N5776 are all available for immediate delivery from any TRW distributor.

For applications assistance, contact TRW Semiconductor Division, 14520 Aviation Blvd., Lawndale, Calif. Phone: (213) 679-4561. TWX: 910-325-6206.

TRW®

Washington Newsletter

October 12, 1970

Congress wipes out 1971 Mallard funds; Pentagon tries again

The Department of Defense is not giving up on its multinational, all-service communications network, Project Mallard [*Electronics*, March 2, p. 41], even though a joint House-Senate conference committee has just eliminated all fiscal 1971 funds for the program. **Chopped was some $15 million in the R&D account of the Army, which is overseeing** the project at Ft. Monmouth, N.J., **plus more than $1.5 million for the Air Force, which is coordinating international efforts with Australia, Canada, and Great Britain.** Among the disappointed contractors are Booz-Allen Applied Research, Vitro Corp., and Sylvania Electronic Systems.

The **Directorate of Defense Research and Engineering is drafting still another position paper so Deputy Defense Secretary David Packard can attempt to recover some funding,** but the outlook for the rest of this fiscal year is grim. Industry can draw little solace from a Pentagon man's observation that "the program hasn't been killed. We still have Project Mallard as a line item, but with zero dollars." Nevertheless, military brass believe they can legally employ some unallocated communications R&D money to keep going on selected aspects. Louis DeRosa, telecommunications assistant to Defense Secretary Melvin Laird, suggests Mallard **may turn up in next year's budget in less vulnerable form—smaller, less visible segments with new names.**

Big cuts expected in space budget

The survival of an on-going manned space program is on the line in the coming budget year. In upcoming discussions, the White House Office of Management and Budget will ask the National Aeronautics and Space Administration to make greater cuts in the space program, which has already been hit by the cancellation of two Apollo flights and sizable layoffs. Sources close to the program say the **White House will push for a $500 million cut in the $3.2 billion-a-year space program.** NASA will counter with a request for about $3 billion and, if tradition holds, the final NASA budget request will fall in the middle. **However, even a $2.7 billion to $3 billion budget would require NASA to fall back into a study mode on its reusable shuttle program and may require closing another research center.**

Domestic satellites may operate in 12-GHz band

The FCC is urging development of the technology necessary for domestic communications satellite operation at 12 gigahertz. **In action taken just two months before the Dec. 1 cutoff for submitting domestic systems applications, the FCC says applicants should include proposals for operation in the higher bands.** Frequency proposals originally were restricted to 4 to 6 GHz.

Potential "considerable difficulty" in coordinating satellite ground systems with common carrier microwave operations in the lower bands forced the change, the FCC says. Operation at 12 GHz also could permit earth stations closer to urban areas—instead of the 40 to 80 mile separation from major cities considered probable with 4-to-6-GHz operation. **What's more, the higher bands reflect the proposed U.S. position at next June's World Administrative Radio Conference, where world satellite frequencies will be allocated** [*Electronics*, Sept. 14, p. 45].

Univac pushes 3X2 as modular entry for airborne EDP

One more entry into the modular avionics computer race [see p. 122] will be made before year end by Sperry Rand's Univac division. Called the 3X2, **the system uses modules that can be wired together to build a machine consisting of three processors, six memory modules with 16 kilowords of 32 bits each, and two four-channel I/O units.** The machine, developed in-house by Univac, was bid on an Air Force avionics laboratory multiprocessor contract earlier this year. The award went to Burroughs [*Electronics*, July 20 p. 67]. But Univac believes that the low cost of the machine, the high level of circuit integration, and its databus design make it a good bet for avionics needs of the 70s. **The machine will use 200- to 500-gate hybrid TTL circuits and an 0.005-inch plated wire memory.**

AT&T seen altering its position on data transmission

AT&T's plan to build a separate private-line data network is viewed by many in the communications industry as a fundamental shift in corporate philosophy about the data transmission market. AT&T has long championed the virtues of a totally integrated communications system. The plan, and the wording of AT&T's comments to the FCC on specialized common carriers—a thinly veiled charge of incompetence aimed at the FCC's Common Carrier Bureau—**raise speculations that AT&T is making a last ditch attempt to head off competition by asking for more hearings on the issue.** Nonetheless, FCC chairman Dean Burch is expected to take the advice of the Common Carrier Bureau [*Electronics*, Aug. 3, p. 37] that further hearings would be a waste of time. **While AT&T and its rivals would like a final decision by yearend, none is expected until February or March.**

NSF lab to study environment has eager followers

First funds for a new national environmental laboratory, to be operated by the National Science Foundation, might show up in the President's budget request for fiscal 1972, now in preparation. **Capital-based electronics industry marketing men are monitoring the project's progress for corporate offices anxious to find new, non-military technical outlets.** It's thought the new basic research center will be located in Maryland's Chesapeake Bay region and will be patterned after such institutions as the National Center for Atmospheric Research at Boulder, Colo., and the Oak Ridge National Laboratory in Tennessee.

EIA membership, financing are first problems for Adduci

Electronic Industries Association President-select Vincent J. "Jim" Adduci faces multiple economic problems on Nov. 1 when he officially succeeds George D. Butler, who resigned after 16 months on the job. **Litton Industries confirms it is one of the 14 active members dropping EIA membership, citing tight economic conditions.** Also, 23 associate members have submitted resignations. With only five new membership applications pending, EIA would fall to 260 members. What's more, Adduci, now a senior vice president of the Aerospace Industries Association, will have to bring in a new general counsel to replace Graham McGowan, who is also leaving, according to EIA sources. **Then, too, the operating surplus is reportedly down to $800,000**—outlays for last fiscal year exceeded income by about $200,000—but much of that is tied up in equipment or already committed, leaving about one-tenth of that available for use.

The only miniature storage tube that can hold an image for 1 month...and erase it in one TV frame.

Actually our TME 1239 acts as an electronic buffer memory. It can store a full TV gray-scale image for 15 minutes with constant refreshing, and a black and white image for half an hour. If the power is turned off, storage capability is at least one month.

A unique feature of the TME 1239 is its fast erasing capability: thanks to a specially developed gun*, one TV frame is enough to erase a complete image down to the residual noise level of a good amplifier. Because the display function is separated from the storage system, the user can selectively edit the stored image or if he is interested in blow-up, zoom-in on any portion of the image.

The 1.5″-diameter structured silicon target of the TME 1239 permits a resolution of 1200 TV lines at a 50% modulation. It also permits operation with standard vidicon hardware, at a voltage level of 750 volts. The resulting flexibility and low cost of associated electronics make the TME 1239 ideal for a number of applications such as TV image storage, bandwidth compression or expansion, scan conversion, peripheral buffer memory, etc.

Also available is the TME 1238: its 1″ target permits a resolution of 800 TV lines at 50% modulation.

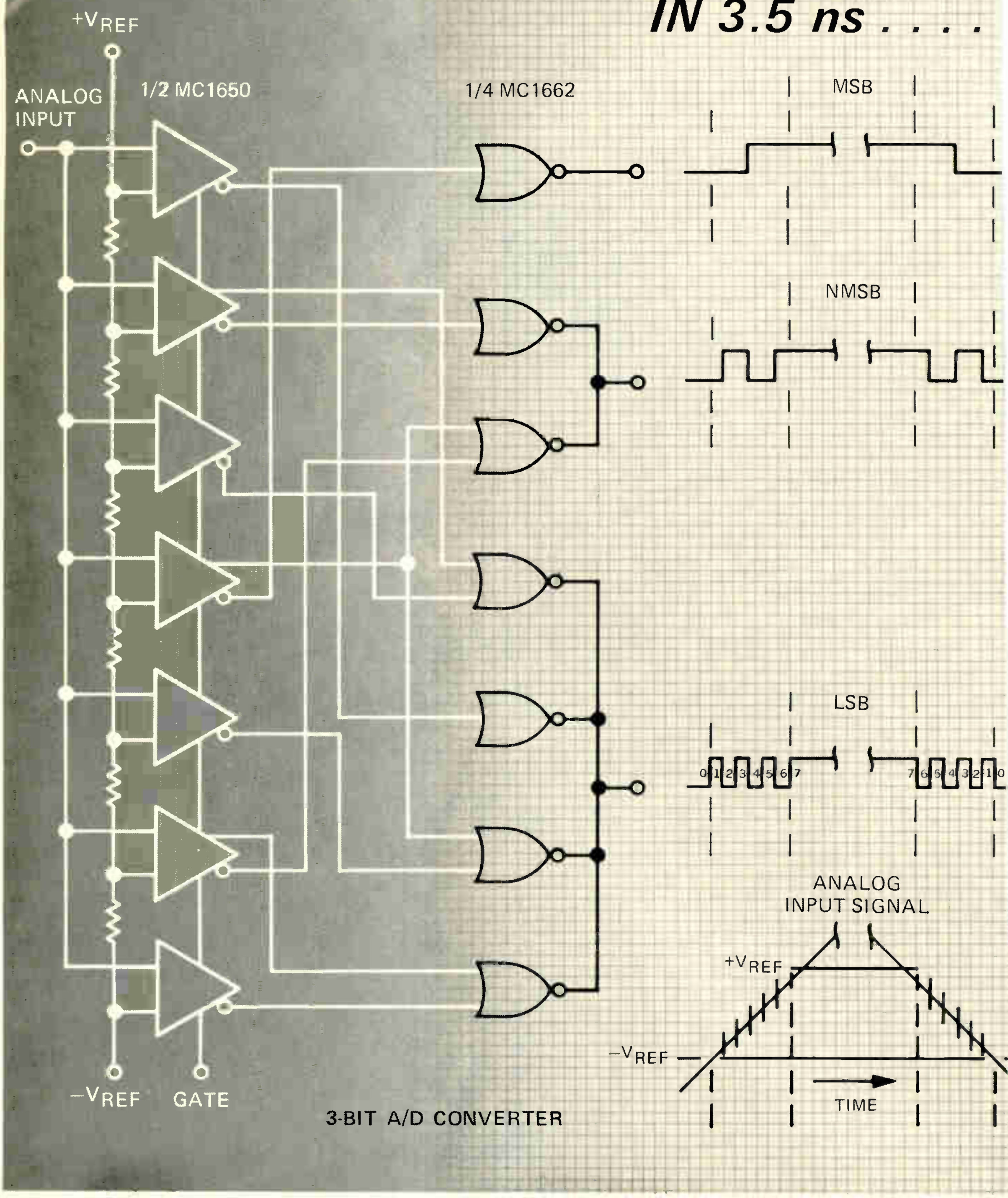
For more information about these tubes and our entire line of storage and display tubes, please circle the appropriate number on the Reader Service Card or contact us directly.

*Thomson-CSF patent.

THOMSON-CSF

Thomson-CSF Electron Tubes, Inc. / 50 Rockefeller Plaza / New York, N.Y. 10020 / (212) 245-3900

FROM ANALOG-TO-DIGITAL IN 3.5 ns . . . .



. . . MECL III MAKES IT HAPPEN

In this computer world of rapidly accumulating data it is imperative to develop new high-speed techniques for analog-to-digital data conversion. To meet these demands Motorola now offers the MC1650 A/D Comparator, a digital integrated circuit providing faster conversion rates than any comparable IC system available today — at no increase in cost!

Basically, the MC1650 compares an analog signal to a reference voltage when the gate is in the logic "1" state. When the analog level is greater than the reference, the output (Q) of the comparator goes to a logic "1". When the analog signal is less than the reference voltage, the comparator output voltage goes to a logic "0".

The comparator will accept analog signals with slew rates up to 340 V/μs and provides digital information at rates up to 200 megabits per second, at the least significant bit (LSB). And the MC1650 features a built-in memory whereby the gate input, when taken to a logic "0" level, will cause all bits of digital information to remain in the present state, regardless of a change at the analog input. The MC1650 incorporates two comparators in one package and operates at MECL III logic levels. Other features include a typical delay of 3.5 ns and complementary outputs which increase flexibility of design.

In the 3-bit A/D converter illustrated, the analog signal is represented as a straight line, but may assume any form as long as the maximum slew rate is not exceeded. The incremental steps are determined by the bias values supplied by resistors between $+V_{REF}$ and $-V_{REF}$. Equal values for all resistors (assumed here) will break the analog sensitivity of the system into equal increments, while different values result in unequal increments.

Apply the MC1650 to instrumentation applications such as frequency measurement, high-frequency sample and hold, and peak voltage detection. In navigation and aviation use the comparator for application in altimeters, peak detectors, and electromechanical system-control interfacing. And consider the high-speed applications for computer terminals and memory translation and amplification.

For complete MC1650 specifications write to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036. Your local Motorola distributor has evaluation devices available now. Evaluation will introduce you to the latest concept of high-speed A/D data conversion where MECL III makes things happen.

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MOTOROLA MECL

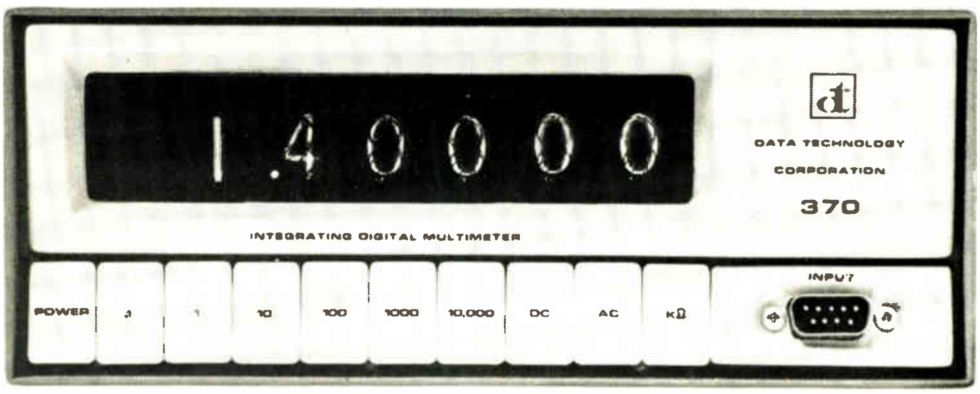
the only way to go . . . FASTER

The $1450

For price, for performance, it's tough to match our 5-digit multimeter. There's just no one else doing the job with so many goodies thrown into the low basic cost.

Standard on our Model 370 DVM: autorange in all ranges for all functions, buffered/isolated BCD outputs, remote control and programming. And TTL logic levels sufficient to drive a DTL printer. Plus microvolt capability builtin. DC accuracy of .0025% RDG and hard-rock stability that lets us skip the front panel zero pot.

You get a push-button reach from 1μV to 1000V—



You'll get the direct print paper on the right faster.

There's no need for "hurry" stamps on Astroprint oscillographic papers. Easy ordering and direct delivery are part of the package.

You also get a direct print, orthochromatic paper unsurpassed for trace density, instant pop-up (less than 1 second), excellent image stability and sharp contrast. On mercury vapor, Xenon, and cathode ray light sources.

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The paper will prove itself.

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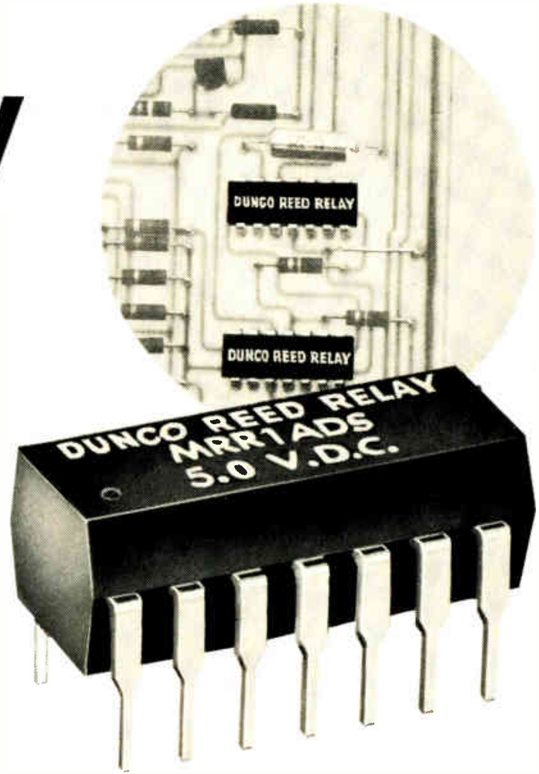
High sensitivity DIP reed relays that minimize IC buffering



Dunco 14-Pin Dual In-Line Relay Series

9.0 mA from a 5-volt IC drives the Dunco MRR1ADSR reed relay without interface buffering. That makes it about the most sensitive DIP relay available.

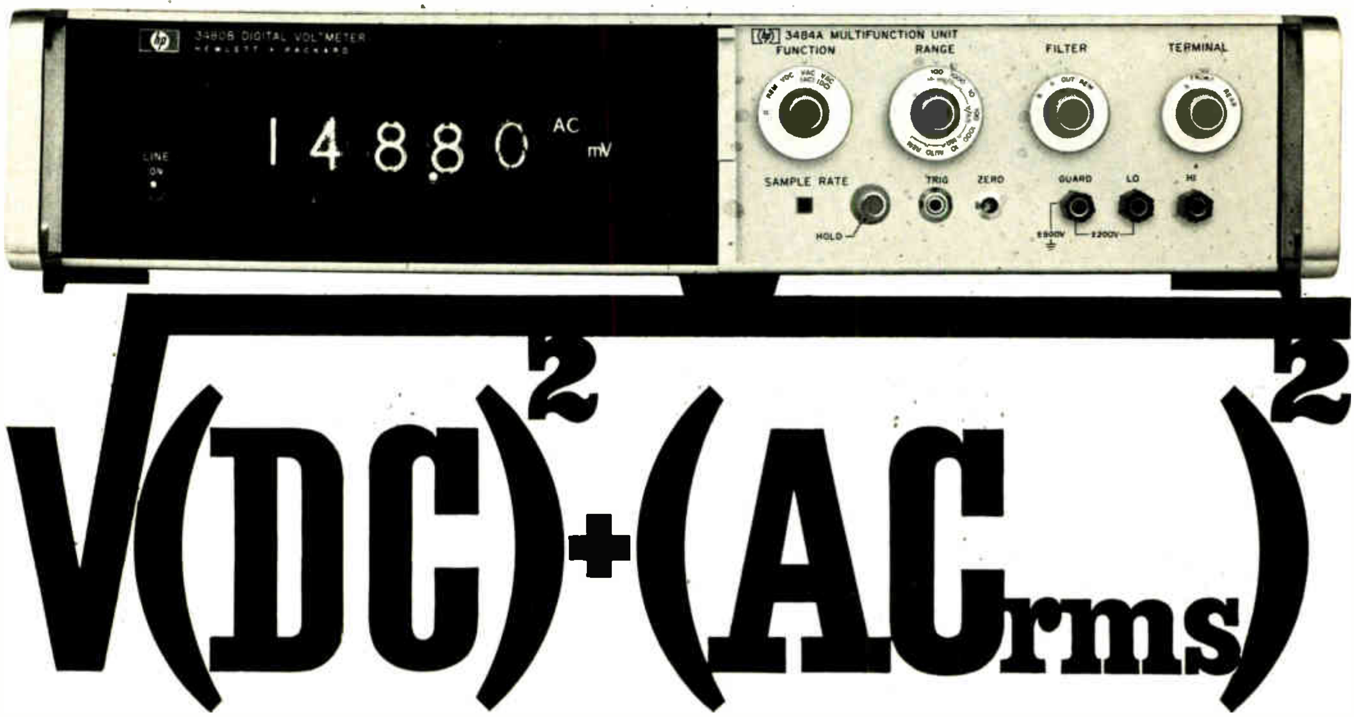
Or, with a few more milliwatts, you save money by choosing from five other models. All are the same size, have the same terminal spacings as 14-terminal dual in-line ICs. Types with 5, 6, 12, and 24-volt coils span DTL and TTL computer logic, High Noise Immunity Logic for industrial control systems, and general-purpose applications.

Stock types have one Form A, 10 VA miniature reed switches. Options include one Form C or two Form A switches, electrostatic shielding, internal clamp diodes.

Get complete information by writing for Data Bulletin B/3200.

STRUTHERS-DUNN, INC.
PITMAN, NEW JERSEY 08071
Canada: Struthers-Dunn Relay Div., Renfrew Electric Co., Ltd.
8S-0103

When is True RMS Really True RMS?



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DIGITAL VOLTMETERS

Article Highlights

Holography helps radar find new performance horizons
page 80

Conventional radar techniques encounter a focusing limitation that no longer has to restrict their effectiveness, thanks to the application of holography. The key is to recognize that coherent radar actually is a form of microwave holography. As such, it can be combined with optical signal processing techniques to greatly expand performance parameters. A marked improvement in target resolution and system versatility are two of the benefits that could result from this new combination.

Parallel multiplier gets boost from IC iterative logic
page 89

A parallel rather than a serial approach long has been advocated for speeding up multiplication in computers. Now, enough iterative logic cells can be combined on a single integrated circuit chip to make the parallel technique practical and economical. One approach puts a four-bit by two-bit multiplier in a 20-pin dual in-line package.

Semiconductor memories: How much do they really cost?
page 94

Systems builders often elect to put together their own memories from packaged chips because the initial price quote for this approach is much lower than for a complete memory system. But after the costs of assembly, testing, engineering, and circuitry are factored in, the users may discover that the initial price disparity has shrunk considerably.

Help yourself to a good dc-to-dc converter design
page 103

The dc-to-dc converter is an inexpensive method of providing several different power supplies through a single device. The usual approach often results in considerable design time spent on trial-and-error procedures. But by using a set of basic equations, a converter can be designed quickly and simply.

Coming

Vietnam report

In the history of military technology, Vietnam will likely be known as the first digital war. That's the verdict of *Electronics'* international managing editor, Art Erikson, who's just returned from Vietnam. In the first of his two-part series, Erikson examines the way technology is influencing the course of the war, and vice versa.

Holography can help radar find new performance horizons

Coherent radar is a form of microwave holography, and combined with optical signal processing techniques, it can overcome the focusing limitations of radar systems while improving resolution and versatility

By Winston E. Kock, *Bendix Corp., Southfield, Mich.*

□ Combining holographic techniques and optical signal processing can overcome the focusing limitations of radar systems, and add greater resolution versatility and simplicity to side-looking, bistatic, passive, and pulse compression radars. The key is that coherent radar is a form of microwave holography, and as such can circumvent the performance barriers imposed on conventional radar by its reliance on antennas and reflectors that focus on only one plane of the image field.

The similarity of coherent radar, which requires single-frequency emission for operations, and holography is apparent in examining a simple synthetic-aperture aircraft radar technique. As an aircraft moves along a very straight path, its radar continuously emits successive microwave pulses as shown in Fig. 1a. The frequency of the microwave signal must be constant for the signal to remain coherent with successive signals for long periods.

During these periods in which the signals remain coherent the aircraft travels several thousand feet, and because the signals are coherent, the many returned echoes appear to be received by a single antenna. Thus, this antenna has a long synthetic aperture, equal to the distance traveled. This effectively large antenna length provides both the very high gain and resolving power of coherent radar, yielding extremely fine detail, as in the aerial photograph, Fig. 2.

As in holographic imaging, the microwave generator that provides the illuminating signal also acts as a reference wave. The reflected signals received along the flight path form a complex interference pattern with the reference signal which, photographically processed and superimposed, becomes a record, called a zone plate, of the area of interest. Such zone plates, in fact, are exactly what's produced during the first stage of holographic reconstruction. Thus the photographic record of the echoes received by coherent radar actually is a microwave hologram.

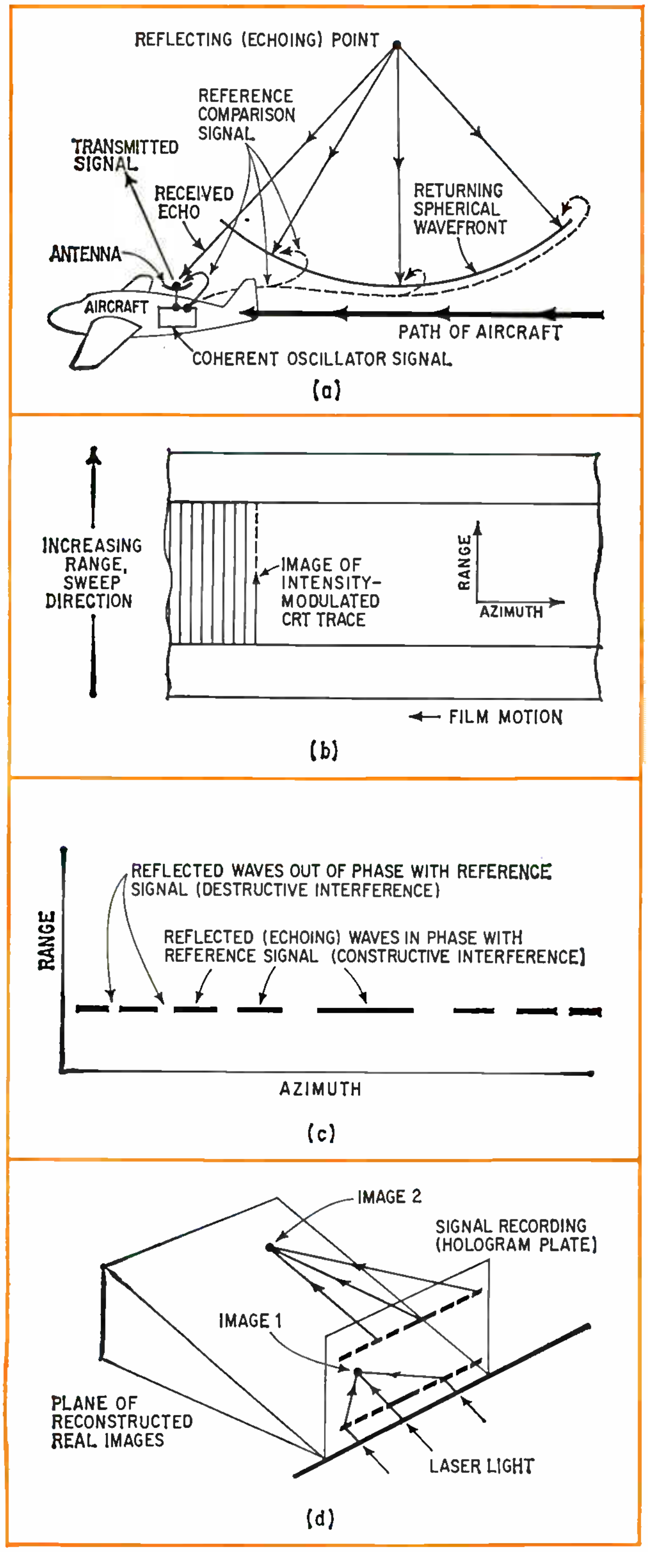
How the interference pattern is formed is illustrated in Fig. 1a. For simplicity, only one reflecting point is sketched. Reflections returning from this point exhibit spherical wave fronts, while the reference signal acts as a set of plane waves perpendicular to the airplane's path. The combination of the received signal and the coherent reference signal is amplified and modulates the intensity of a cathode ray tube trace (Fig. 1b). Each vertical line represents signals received from all range points; the points at greater range are recorded nearer the top of the vertical trace. As the aircraft moves and new pulses are emitted, the film is indexed (moved slightly to the left) to record a new set of returns—a new vertical line.

When there's only one reflecting point at a given range, the upward-moving cathode ray beam would be brightened for every pulse, only at that one point in range—at the same level on each vertical trace. The echoes thus would be recorded as a single horizontal line. But this line is not continuous, as shown in Fig. 1c. Because the returning waves are circular, different points on the wave reach the receiver at different times, so that the combination of the returning signal and the reference waves successively produces constructive and destructive interference areas. And because of the circular nature of the waves the slant azimuth range (the distance from the aircraft to the reflecting point) changes.

At the greater slant angles, where the distance from the plane to the point changes rapidly, this succession of in-phase and out-of-phase conditions occurs rapidly. But when the aircraft is nearly abreast of the reflecting point, the range is almost constant, so the changes come more slowly. The resulting record is a one-dimensional zone-plate hologram, which, if illuminated by laser light, reconstructs the reflecting point just as illuminating a hologram reconstructs an image of the original scene.

Plane wave laser light (Fig. 1d) reconstructs the range and azimuthal position of the reflecting points that generated the zone plates. The two reflecting points shown are displaced appreciably in range and slightly in azimuth. The reconstructed images fall on a plane; the tilt of the plane is determined by the radar's vertical tilt.

Many people first questioned whether high resolution could be maintained for nearby objects. Because of the synthetic aperture antenna's great length, the majority of reflecting objects are not in the far field, where most conventional radar antennas operate, but



1. In action. In side-looking radar (a), circular wavefronts returning from a target combine with a coherent reference signal as aircraft flies a straight path. The recorded interference patterns (one-dimensional Fresnel zone plates) can be made into a hologram record by photographing intensity-modulated CRT trace (b). For two point-source targets, the hologram zone plate (c) of each target is reconstructed (d) by radar hologram laser light.

in the near field as shown by Cutrona of KMS.

For near-field reflection, radars with large-aperture antennas can achieve maximum efficiency and resolution only when the phases of the antenna elements are adjusted so that the beam pattern forms an arc of a circle centered on the object. Yet for other near-field targets located at other ranges and azimuth directions, the phases of all antenna elements similarly must be adjusted to correspond to the arcs of circles centered on these other points. Such a result would be difficult to achieve with standard phased array radar procedures.

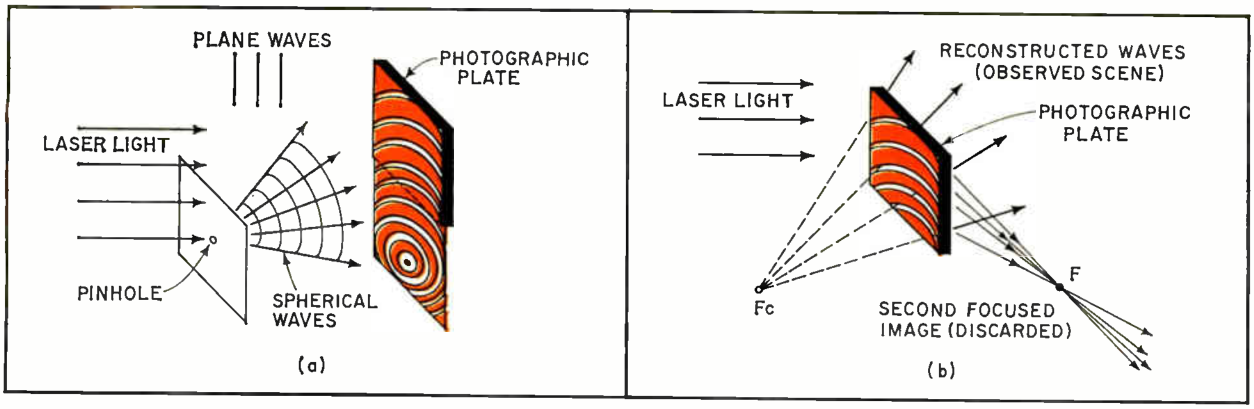
However, once it's recognized that a coherent-radar record is a hologram, it becomes apparent that high resolution in the near field can be accomplished without complex phased-array techniques. In holography, each small light-reflecting point generates its own zone plate; each of these then is used to reconstruct each point in space. Similarly, synthetic aperture radar photographically captures the curved wave fronts emanating from each reflecting point by combining them with a reference wave, generating many one-dimensional zone plates.

In reconstruction, diffraction of a coherent laser beam by the zone plates produces the properly curved wave fronts in the beam, so that the light will be focused at points corresponding to the reflecting targets in the original landscape. Just as in an optical hologram each point of a three-dimensional scene is brought into sharp focus at any distance from the photographic plate, so the microwave hologram of the radar record provides good focus on all its reconstructed points.

This capability is common to both coherent radar and holography, and sets them apart from ordinary radar and photography. Usual optical imaging processes employ lenses or paraboloidal reflectors that permit only one plane section of the image field to be recorded in truly sharp focus, a limitation that doesn't apply to both holography and synthetic aperture radar.

However, one inherent processing limitation does apply to holographic radars: a photographic record must first be made, and this record, after the film is developed, must be illuminated with coherent light. The delay involved cannot meet the real time requirements of many applications. But real time readout can be achieved without film by using ultrasonic cells. These, by virtue of the Debye-Sears effect, can modulate (diffract) a coherent light beam illuminating the cell in almost the same way as a photographic film. When the entire microwave-acoustic signal has moved into the ultrasonic cell, it is briefly illuminated with laser light, and the resulting diffraction pattern provides the target information.

Still broader uses can be made of hologram radar concepts, particularly when large apertures are involved. In side-looking radar, dopler effects are introduced into the received signals by the airplane's motion. However, in forming holograms, relative motion, and hence doppler effects, are absent; thus through holographic methods, stationary coherent radars become feasible. Such radar antennas could be extremely long



Two of a kind

The similarity between holograms and coherent radar recordings (zone plates) becomes clear when it is realized that both are recordings of interference patterns. In fact, a simple hologram of a point source of light is merely a photographically produced zone plate bearing alternate transparent and opaque rings as shown above. The open spaces on the photographic plate pass only energy that will be constructively used at the desired focal point; the opaque rings filter out energy that would interfere destructively at that point. Thus, when the plate is illuminated with laser (coherent) light, diffraction causes converging waves to create a real image of the original scene at the focal point.

Diffraction at the zone plate also generates diverging waves, and these create the illusion of a point source of light located at the conjugate focal point F_c—a virtual image of the point source of light. This diverging light is indistinguishable from that which originally issued from the pinhole; thus the viewer seems to see this source of light located in space behind the illuminated plate.

If there were two point sources of light in the original scene, two superimposed zone plates would have been recorded. The hologram then would provide an image of both original light sources, again fixed in space. Since any scene can be resolved into many such individual light sources, each forming with the reference wave its own zone plate on the photographic plate, the hologram of an actual scene will generate a composite combination of virtual images of all the multiple original light sources. Thus, the combination of images is an exact replica of the original scene.

Because holograms are a form of zone plate, and because the design and function of a zone plate is based on one particular wavelength, only single-frequency light waves can properly reconstruct a holographically recorded image. Similarly, operation of coherent radar also requires single frequencies, and therefore it depends on electromagnetic signals having a very highly stabilized frequency. This characteristic is called frequency coherence or temporal coherence.

The degree of laser frequency coherence is often described in terms of the coherence length of the device. This is a measure of how far two long-wave trains can be slid past one another with the wave crests remaining aligned. Though laser light is extremely coherent, the very short wavelengths of light waves limit coherence lengths to a few meters. Because wavelengths of the radio waves used in coherent radars are much longer, coherence lengths extend to many kilometers. This permits effective coherent radar operation over extremely large ranges.

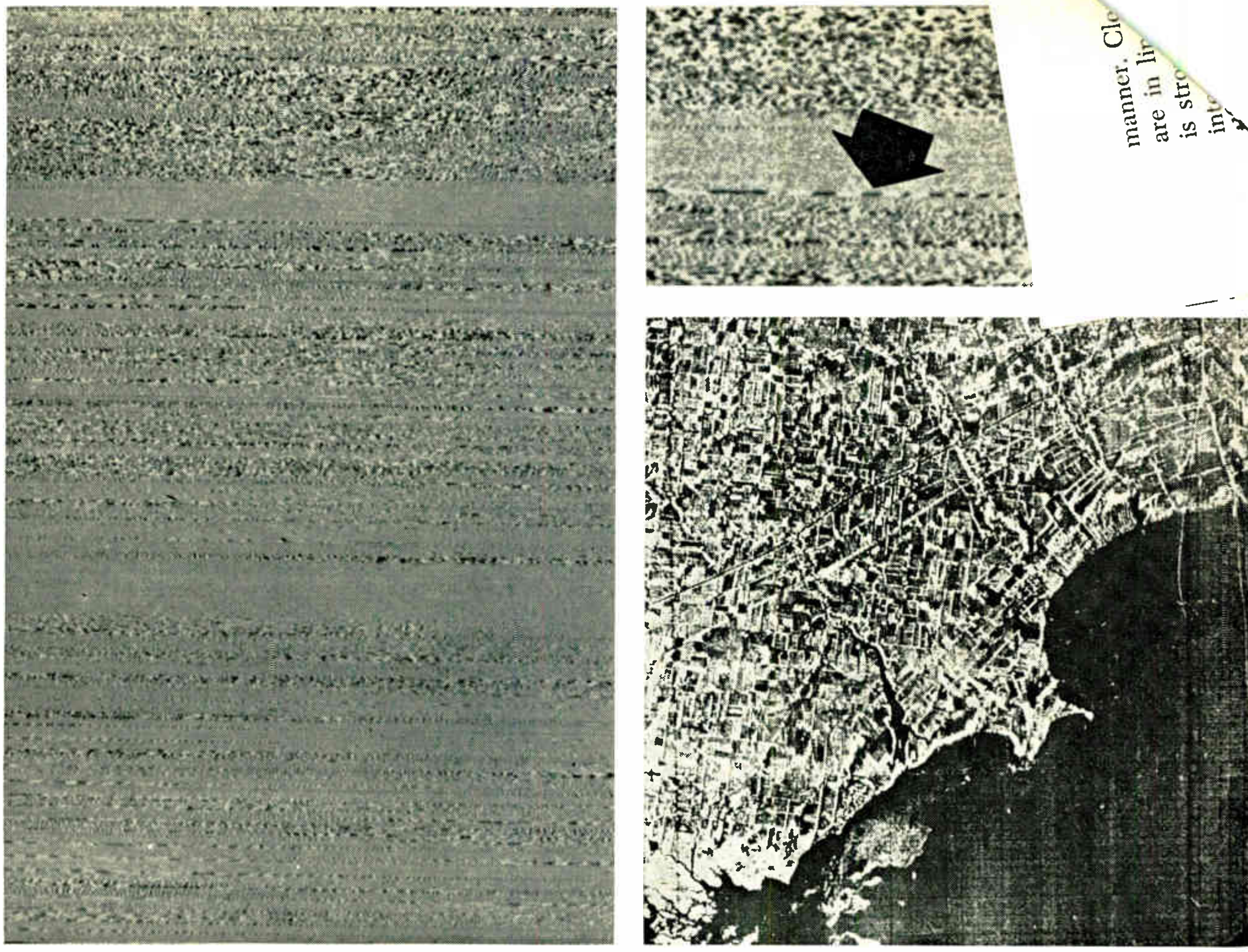
linear arrays of independent receivers. Other possibilities include crossed arrays (Mills Crosses), and square arrays.

It should be noted that in holography, even a small portion of the hologram is able to reconstruct the full image. Similarly, in stationary coherent radars, just the end sections of the long linear arrays, or the four-corner sections of square arrays, could be used to maintain maximum resolution.

Probably the simplest form of a stationary coherent radar antenna would be a long linear array of elements identical to the aircraft-borne antenna described earlier. In operation, each element would first transmit a short pulse, following which it would act as a receiving element. The process is repeated, with the transmitted signal successively transferred from one antenna element to the next, matching the aircraft motion to be simulated. Small amounts of coherent signal must be fed continually to each element to provide the holographic reference signal. The returning echoes, interfering at each receiver element with this reference wave, would produce an interference pattern. The returning signals then are recorded on film, indexed each time the transmitted signal is passed on to the next antenna element.

A significant feature of airborne synthetic-aperture radar is that the aperture size varies with range. This makes the radar's resolution independent of range. In Fig. 3 is shown the focusing action of a zone plate. The heavy lines indicate the envelope (to the first null) of the wave energy being diffracted by a zone plate Z with aperture 2a. If this energy concentration is diffraction-limited, the azimuthal resolution R_a is approximately equal to λ r/a, range resolution R_r is about equal to $\lambda r^2/a^2$. When r = 10,000 ft., $\lambda = 0.1$ ft., and $\Delta a = 20\lambda$, then R_a is 2 ft. (exactly the antenna size), whereas R_r is 40 ft. Thus, azimuthal resolution for these parameters is 20 times better than the range resolution.

When range r is increased or decreased, the zone



2. Radar records. Like holograms, side-looking radar recordings (left), consist of many superimposed zone plates from which the original scene may be reconstructed. In the enlarged section (top, right), an isolated reflecting point generates (as marked) an easily recognized one-dimensional zone plate which by monochromatic processing will yield azimuth information corresponding to a tiny fraction of the zone plate length. The zone plate can be thought of as a long, broadside synthetic antenna with its inherently high gain and beam sharpness. The photograph of the Lake Erie shoreline is a reconstructed hologram made from such records.

plate Z becomes larger and moves to the left or becomes smaller and moves to the right. In the process, the angle θ and the values of R_a and R_r remain unchanged. When Δa extends only one wavelength, the range and azimuth resolutions become equal, so that good range resolution is possible simply through the action of the superimposed zone plates alone, without the use of the more complex simulation technique.

In the superimposed zone plate technique, all of the horizontal zone plates in the radar record would be collapsed into one horizontal line. In usual radar records, superposition of one-dimensional zone plates occurs only for reflectors located at the same range. Here, though, superposition of zone plates would occur for all reflecting points. But as in a true hologram, this superposition would not hamper reconstruction of the original scene.

In addition to side-looking radar, hologram concepts also can be extended to forward scatter, bistatic systems. Here the targets are located between the transmitter and a physically separate receiving array, taking advantage of the high forward-scatter signal diffracted by targets. The receiving array again could be either one long linear array of many elemental receivers or two end sections of that array.

For a single-point scatterer, the interference pattern between the scattered signal and the reference signal again would be a zone plate. The receiving array would intercept a linear section of it (a one-dimensional zone plate). By photographically recording the individual outputs of all of the receiving array elements as one photographic line, comparable to the one line of a side-looking coherent radar record, the range and azimuth of this scatterer then can be determined from the one-dimension zone plate.

With many scatterers, multiple zone plates are generated; these would be photographically superimposed, and positional information on all of the scatters could be retrieved in the usual holographic

…arly, if the transmitter and receiver array …e exactly (180°), the forward scatter signal …ngest from a target placed between them. The …erference fringe size is then the greatest, so that …the fewest elements are needed in the receiving array and the coherence length requirements on the signal source are minimal. However, at 180° twin images are encountered. This corresponds to the observed effect in holographic reconstruction when angles between real and virtual image rays are so small that they interfere with one another. Hence, it's preferable to place the transmitter at some off-axis angle, say 135°. In bistable arrangements, the transmitter operates continuously.

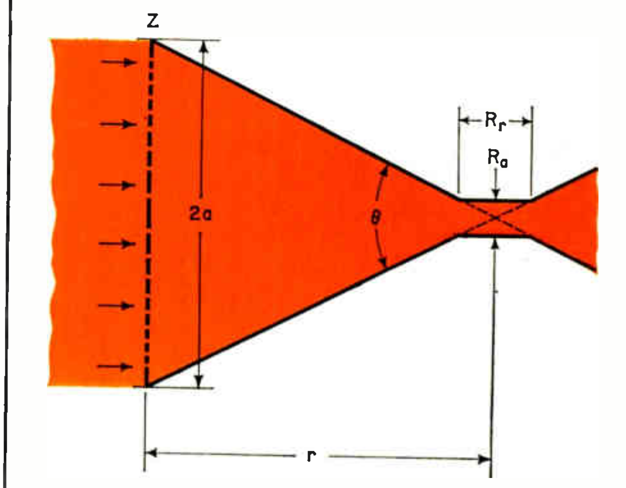
In addition to achieving the equivalent gain of a very long linear broadside array, the synthetic aperture procedure also permits synthetic end-fire gain, In fact, the same directivity gain can be achieved as in the linear broadside antenna. Such an end-fire radar technique would endow a small airborne antenna with a very high forward directivity gain. The resulting pencil-shaped beam could enable the aircraft to detect weakly reflecting objects in its path.

In the end-fire case, the interference pattern produced by echoes from a front target interfering with a reference wave is a one-dimensional, uniformly spaced, sinusoidally varying density pattern, instead of the non-uniformly spaced, one-dimensional zone plate pattern of the side-looking radar. This pattern is equivalent to a one-dimensional grating, which is used to reconstruct the image. The plane waves of coherent light diffracted by this grating are converted by a lens into circular waves converging at a focal point. Light concentration equals that obtained with a one-dimensional zone plate. Also achieved is a correspondingly high effective antenna gain, with its accompanying high signal-to-noise ratio.

The narrowness of the synthetic end-fire beam minimizes reflections from the ground when the aircraft is in flight at high altitudes. Only those targets in the direct path of the plane will return a strong signal. The high synthetic gain thus achieved may permit detection, at useful ranges, of those discontinuities having small indexes of refraction which occur in regions of clear air turbulence. However, real time reconstruction and display is essential if the aircraft is to take corrective action when the returns indicate turbulence.

A passive form of coherent radar becomes possible when a target radiates a highly coherent signal. Such radiation could originate from specially equipped aircraft in the vicinity of airports whose location then could be determined. The equipment might comprise one long array of receiver elements, with one or more elements receiving, amplifying, and feeding the signal as a reference wave to the other elements. These elements also would be receiving the radiated signal directly. Thus an interference pattern would be generated along the array, which, following a recording and reconstruction process, would locate the radiating object.

A variation of the procedure is to put a transmitter at the location of interest, say an airport, sending signals to aircraft. These targets would receive the signal, amplify it, and reradiate it, preferably after shifting the frequency slightly to prevent "ringing" between the plane's transmitter and receiver. The transmitted signal similarly would be shifted in frequency and fed, as a reference wave, to the individual receivers of the receiving arrays.

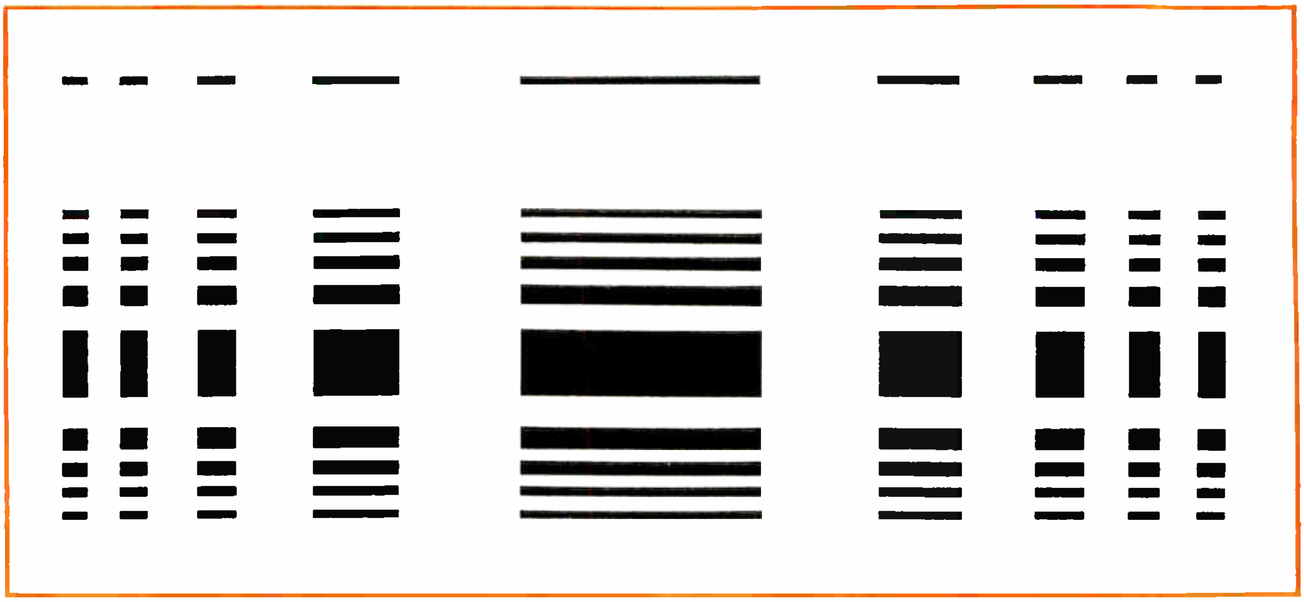


3. **Focus.** Zone plate, Z, with aperture 2a, provides focusing action that yields both azimuthal and range resolution, R_a and R_r, respectively. For configuration shown, azimuthal resolution is 20 times better than range resolution.

Holographic methods also may be valuable in pulse compression radar. Pulse compression techniques convert long, high power transmitted pulses to shorter, high-resolution pulses, at the reviewer. Often the frequency is varied (chirped) over the duration of the pulse and then is detected and compressed by a matched (dispersive) filter. The filter causes signals of different frequencies to travel at different velocities, thereby permitting the more rapidly traveling portion of the long pulse to catch up to the slower, earlier generated portion.

In another, newer technique, the amplitude of the long pulse is varied instead of its frequency. In amplitude pulse compression, the total time of the original pulse corresponds to the total length of the zone plate; thus the long c-w pulse gets an amplitude modulation pattern corresponding to the spacing of a one-dimensional zone plate.

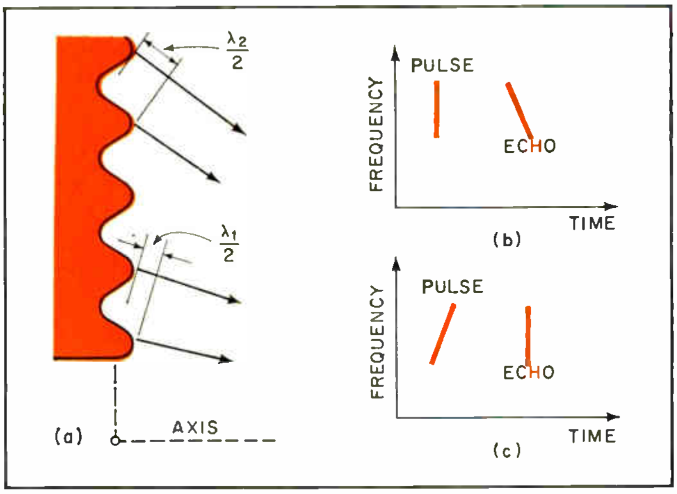
As before, the received echoes are photographically recorded, each from a single, isolated target generating its own photographically recorded zone plate pattern. Optical processing is accomplished by focusing a laser beam onto a tiny focal area, thereby providing a very accurate range for the reflecting point, equal to the zone plate dot spacing that can be resolved. The ratio of this resolution width to zone plate length corresponds to the pulse compression ratio. With this method compressions of 5,000 to 1 are

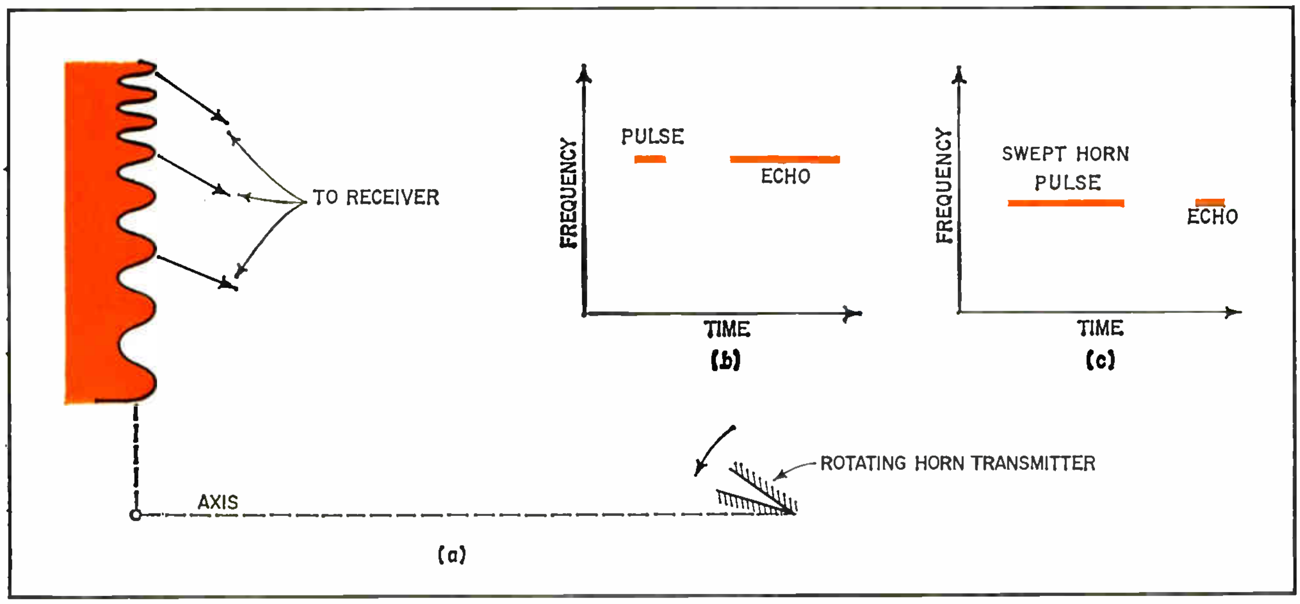


4. Spreading records. Synthetic aperture radar using short pulses generates one-dimensional zone plates (top), where the line thickness is a measure of the pulse duration. When the pulse is made long and given a zone plate amplitude contour, the record (bottom) spreads into parallel zone plates.

5. Chirping. An off-axis period grating (a) reflects short wavelength (high frequency) waves (λ_1) from points near the axis, longer waves (λ_2) from more distant points. The return echo is heard as a descending chirp (b). If an ascending chirp is transmitted, the return undergoes a compression in duration (c).

6. Compression. Zone plate grating reflect single-frequency waves toward its focal area (a). More distant reflections return later, yielding stretched echo (b). However, areas illuminated at different times by a rotating horn result in pulse compression (c).





Holography and doppler radar

Recently the operation of holography has been extended to the processing of pulse doppler radar signals. For cases where both the range and the range rates of many separate targets must be measured, Arm and King of Riverside Research Institute showed that the holographic procedure would take a sequence of radar returns and store them as holograms, with optical reconstruction yielding the desired information.

In this system, good range resolution implies short pulses; range rate data based on doppler frequency-shift measurements of the return signal demands a long radar pulse. To accomplish both, a coherent pulse burst (top Fig.) is used. A burst consists of a train of N pulses equally spaced T seconds apart with each pulse τ seconds long. Pulse duration determines range resolution; burst duration, NT, determines the doppler frequency-shift resolution of 1/NT hertz.

The lower diagram of the Fig. shows that each radar transmission elicits a return from each of four targets. The delay between each short transmitted pulse of the train and the time of the corresponding return from one of the targets accurately resolves range.

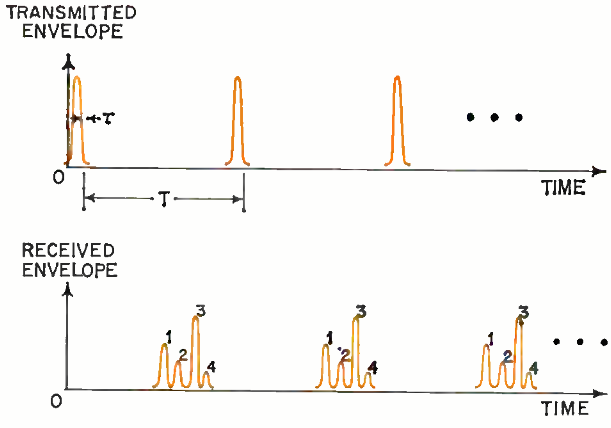
The range rate of each target usually is obtained by feeding the entire sequence of N returns from the target into a spectrum analyzer, and determining the doppler frequency shift. Since this analysis must be performed for each required range element, many spectrum analyzers will be needed. However, with holography, optical procedures do the same task.

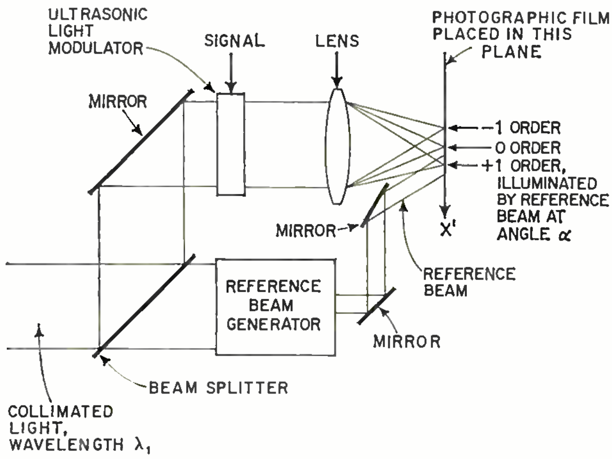
In the first step, returns are stored holographically (middle Fig.). A collimated beam of laser light is split into reference and signal components; it's later recombined to form an interference pattern on a vertical strip of the photographic film. The upper path contains the signal beam and records the radar return signal as it passes through an ultrasonic light modulator. The lower path directs the reference beam onto the same film strip.

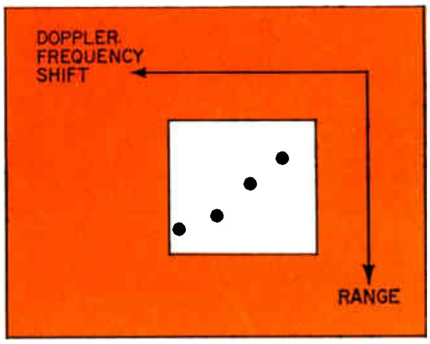
The signal of the ultrasonic light modulator's aperture is the signal reflected from the four targets as produced by a single transmitted radar pulse. When the complete reflected signal (comprising in this case only four echoes) reaches the ultrasonic modulator, the laser light is turned on briefly, and the hologram is recorded. Thus, the hologram occupies a narrow vertical strip on the film. After each pulse, the film is indexed, or moved perpendicular to the plane of the figure. When the return signal from the next pulse fills the acoustic cell, the laser is again activated. Thus an entire sequence of N radar returns is recorded as N holograms side by side on the photographic film.

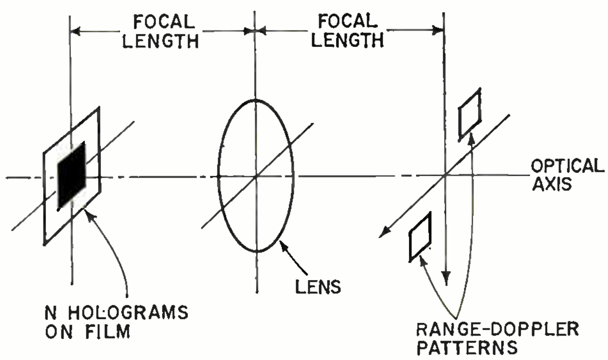
This series of holograms forms, for each target, a grating whose tilt is a function of the target's range rate or doppler frequency so that the four gratings are superimposed, and each has a different degree of tilt. After development, the film sheet of many side-by-side holograms is coherently illuminated and the original configuration reconstructed (lower Fig.). Two areas appear in the output or frequency plane containing all the range-doppler information.

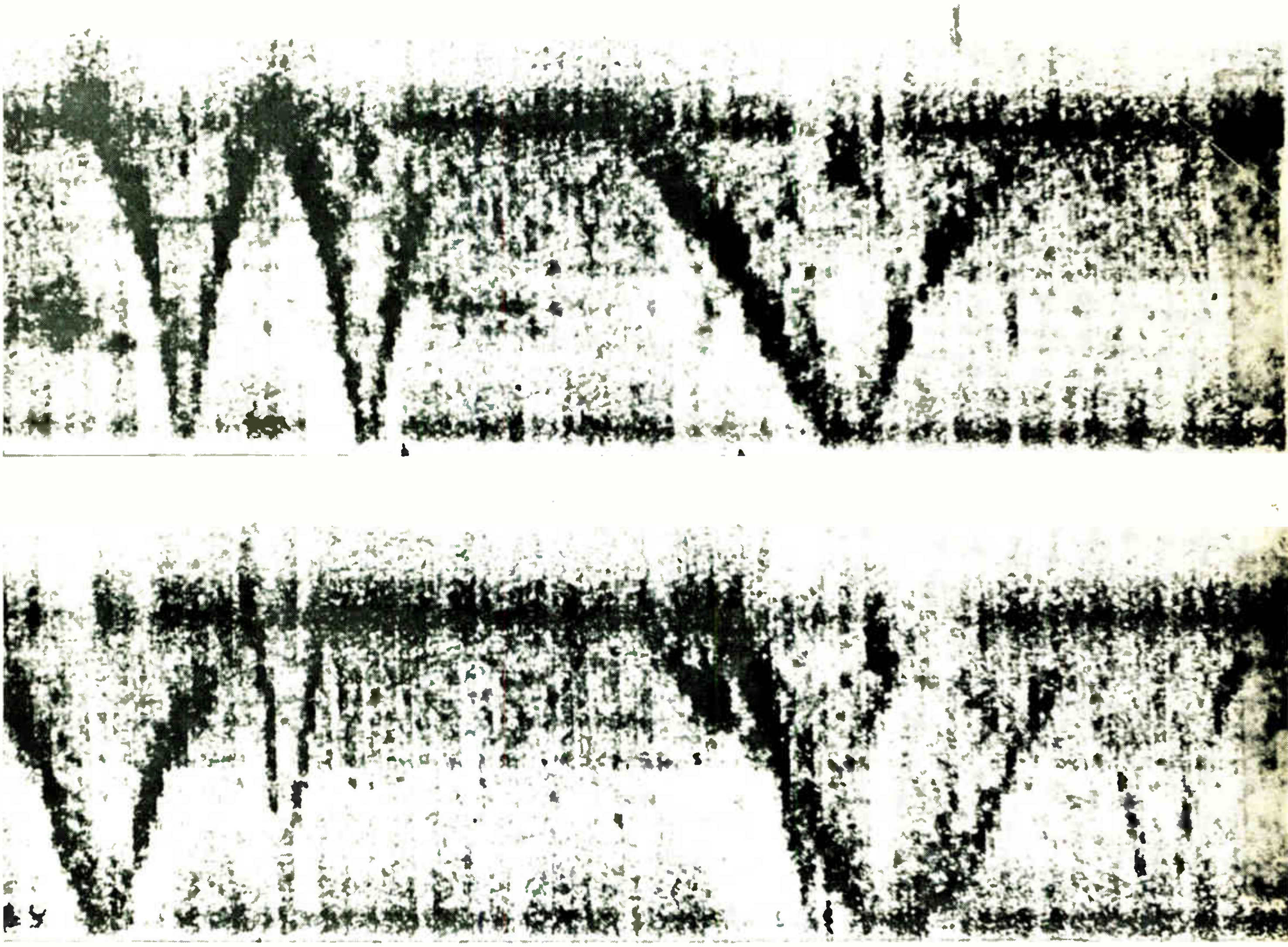
In an expanded view of one of these information areas each of the four bright spots of light corresponds to one of the targets interrogated by the N transmitted radar pulses. Vertical positions corresponds to the target's range, and the horizontal position its range rate.











7. **Enhancing.** Time-frequency record of the interference effects caused by aircraft flying over a transmission path illustrates principle underlying holographically generated bistatic radar zone plate. Holographic techniques can be used to enhance weak signals shown on bottom right record.

feasible. Moreover, a zone-plate dot spacing yielding an a-m length of 20 carrier cycles, would impose an extremely modest bandwidth requirement of approximately ±2.5%.

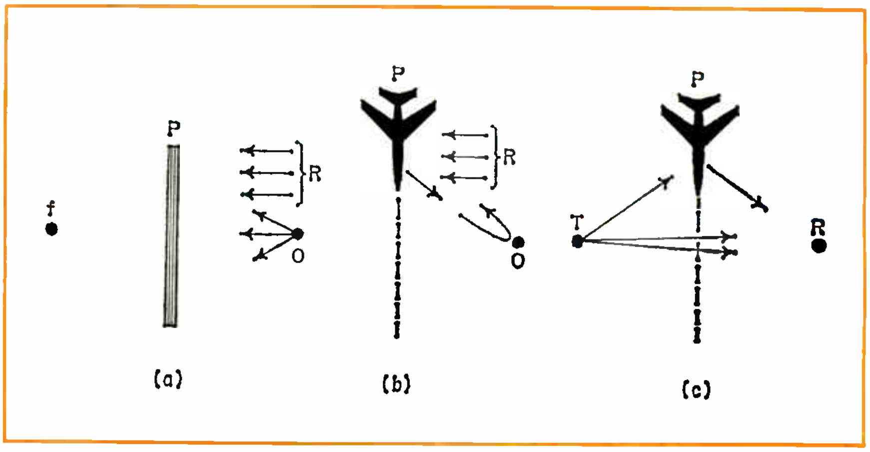
As for many reflectors at various ranges, many received zone plates would be generated. These would be superimposed on the photographic record, yielding a line recording of numerous superimposed zone plates. This radar record then would be laser processed to yield individual targets.

This a-m procedure is particularly adaptable to synthetic aperture radar where optical processing techniques already are employed. To increase the energy in the outgoing pulse of such radars, the a-m pulse can also be made quite long, and be given a shape corresponding to the diffraction pattern (envelope) resulting from the zone plate. This pulse shape will cause the thin, one-dimensional zone plate illustrated in Fig. 4 to acquire an extended vertical dimension, thereby becoming a sort of two-dimensional zone plate as shown in the bottom of the Fig.

With optical processing procedures, this pattern is collapsed into a one-dimensional pattern for range information. In a second step, the normal holographic processing would be applied to retrieve the azimuth information. With many targets at different ranges and azimuthal positions, zone plate superposition would occur in both horizontal and vertical directions, but optical processing still would permit full retrieveal of the information.

Periodic gratings can convert a short noise pulse to a "chirp". This is sketched in Fig. 5a. A grating is placed off-axis, (at a slight angle to the incoming wave) so to enhance first-order diffracted components relative to the zero-order reflections. Also the sinusoidal corrugations tend to suppress the higher order diffracted components. Since shorter wavelength components of an on-axis noise pulse will constructively interfere nearer the axis then will the longer wavelength ones, and because the more distant re-

8. **Similar.** Point source hologram (a) recorded on photographic plate, P, is similar to radar situations shown in (b) and (c). In (b), an object, O, is recorded on a radar record when combined with a reference signal, R. A one-dimensional zone plate similar to the point-source case of (a) results. In (c) the transmitter, T, is the reference and the plane is the moving reflector, yielding combined signals almost identical to those of (b).



flections return to an on-axis receiving point later, a descending frequency chirp results, as shown in Fig. 5b. Conversely, if an ascending frequency chirp is used as the outgoing pulse, the reflected signal undergoes a length compression as shown in Fig. 5c.

Figure 6 illustrates the case when the grating has a zone plate outline rather than the sinusoidal one. For single-frequency waves, a zone plate acts much like a lens in that all portions diffract energy toward a focal point. Thus, if a short burst of single-frequency energy is directed toward a reflector, all areas would reflect energy to the focal point. But the greater travel time to more distant areas would convert a short, single-frequency pulse on reflection to a long single-frequency pulse (Fig. 6b).

This process can be reversed for use in pulse compression radar; it is sketched in Figs. 6a and 6c. By its motion, a rotating directional horn first illuminates the more distant portions of the zone plate, and the nearer portions later. Since all areas reflect the single-frequency waves back toward the focal point, all components of the long reflected pulse can be made to arrive at this focal area at approximately the same time. The key is to make the rotational motion of the horn match the travel times of the various portions of the outgoing pulse.

In another interesting application, holographic signals can be used to enhance c-w bistatic radars where weak signal returns are lost in noise.

For example, fringe area television reception is degraded when an aircraft flies between the transmitting station and the receiver. The signal reflected from the aircraft generates interference effects which cause variations in picture brightness—rapidly at first, then slowly, then rapidly again.

A time-frequency plot of such changing-frequency signals is shown in Fig. 7 for a number of passing aircraft. Time is plotted horizontally in both top and bottom records, and frequency vertically. The shapes of the two records at the left of center show that the first plane, which generated the wider v-curve, passed by more slowly than the second.

The principle has been applied to a bistatic transmission-line arrangement in a c-w radar for observing meteor trails. Constant-velocity targets generate return signals in such radars, which have a time-amplitude pattern closely resembling that of a zone plate. Accordingly, the same coherent optical techniques employed in holography and synthetic aperture radar should improve the receiver's signal-to-noise ratio. This would improve the readability of patterns that are obscure or very weak, like those in the lower right of Fig. 7.

The similarity between transmission path interference signals and certain hologram and coherent aperture radar records are indicated in the three situations sketched in Fig. 8. In (a), a point source hologram is being recorded on photographic plate, P. A two dimensional zone plate results when c-w spherical waves from the laser source, O, interferes at the plate with the plane waves of a reference beam, R, generated by the same source.

In (b), a single reflecting object O is recorded on a synthetic aperture radar record. The plane, P, flying along the dotted-line path, periodically transmits short pulses of coherent microwaves, and the signals reflected from the object, O, combine with a coherent reference signal shown as the set of plane waves, R. The interference pattern thus formed again corresponds to a one-dimensional zone plate when photographically recorded.

In (c) the aperture of the c-w signal from the transmitter acts as the reference signal at the receiver but now reflector P is moving rather than the transmitter and receiver as in (b). The resultant combined signal recorded at R is (for identical aircraft motion) almost equal to the combination signal recorded photographically in the aircraft of situation (b).

Obviously, the individual v-curves of Fig. 7 also could have been recorded photographically, as in Fig. 8b, thereby forming one-dimensional zone plates. In this case, each recorded zone plate would have a focal length determined by the plane's speed. Thus, the cluster of undetectable records at the lower right of Fig. 7 would be transformed into a set of superimposed zone plates. Standard coherent optical processing procedures then could retrieve the desired information for each target. The chief advantage would be the very large increase in signal-to-noise ratio, equivalent to the very sizable signal-to-noise improvement obtained by synthetic aperture radar procedures. □

Parallel multiplier gets boost from IC iterative logic

Thanks to IC fabrication on the medium-scale level, multibit functions for partial products, sums, and carries can be placed on one chip, economically solving the old problem of numerous interconnections

By John Springer and Peter Alfke, *Fairchild Semiconductor, Mountain View, Calif.*

☐ Multiplication is one of the most common and time-consuming operations in data processing. Computers multiply essentially by a series of additions, and when two mathematical matrixes are multiplied, that's a lot of adding to do. The task consumes expensive computer time, and for computers that operate in real time the situation can often be intolerable.

At various times, iterative logic cells for parallel multiplication have been proposed as a solution. Functionally, the basic iterative logic cell consists of a full adder and an AND gate, as shown in Fig. 2. The cell operates by forming the AND of inputs X and Y, adding the result to inputs K and M, and thus producing a sum, S, and a carry, C.

Implementation of the iterative cell approach has been impeded by the lack of communication between theoreticians in universities and engineers in the semiconductor industry, and by the fact that a single cell on a chip would be uneconomical. However, now that the demand for high-speed multiplication has grown to sizable proportions, these impediments have been overcome and high-speed transistor-transistor logic has been used to implement the function of many cells on a single chip.

One of the most attractive applications for iterative cells is the implementation of the fast Fourier transform—itself a multiplication shortcut—which probably constitutes the most urgent need for high-speed multi-

1. Fast times. Integrated high-speed multiplier can yield the product of a four-bit and a two-bit number. Used for parallel multiplication, the IC has provision for summing partial products of equal weight from an array of similar circuits. The circled terms indicate chip inputs and outputs.

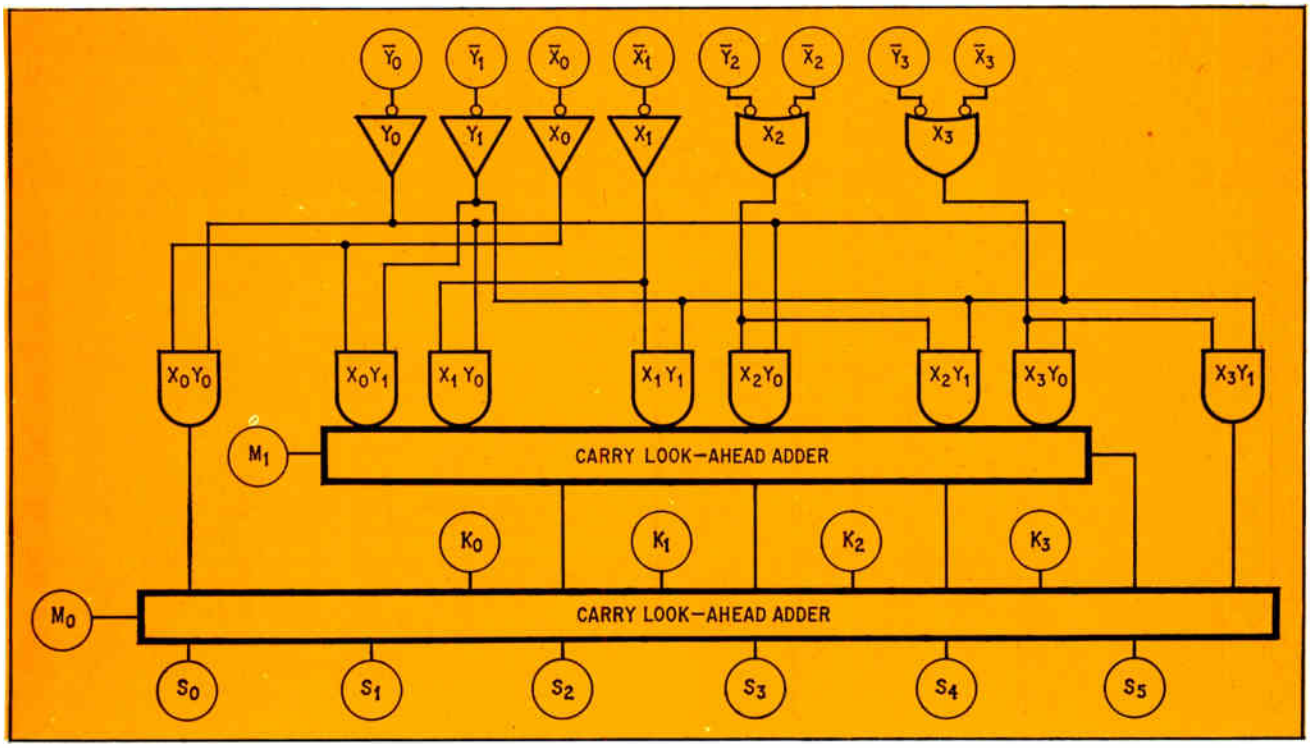


TABLE I – BIT COUNT AND PIN COUNT						
Structure	X, Y	K	M	Output	Power	Total
1 x 1	1, 1	1	1	2	2	8
2 x 2	2, 2	2	2	4	2	14
4 x 2	4, 2	4	2	6	2	20
4 x 4	4, 4	4	4	8	2	26

TABLE II – MULTIPLICATION TIME AS A FUNCTION OF BIT CAPACITY		
Number of bits	Packages	Time (ns)
8 x 8	8	184
10 x 10	13	232
12 x 12	18	280
16 x 16	32	376
24 x 24	72	568

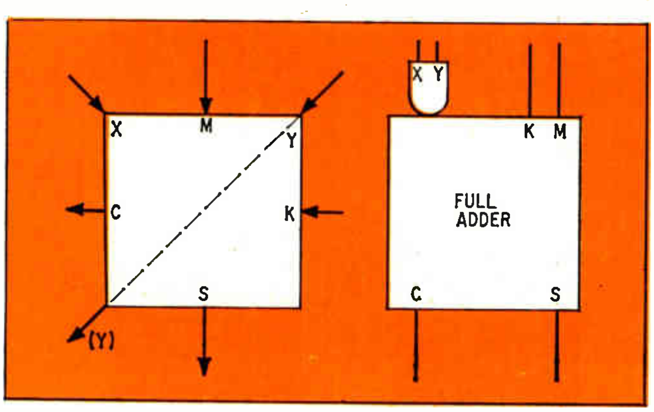
plication. The FFT is a set of recurring equations that operate on periodically sampled data to generate a set of points representing a frequency spectrum. When designing digital filters, an engineer can use the FFT method to perform the convolution of two time series, as well as the correlation of two time series. These uses of the FFT are employed more and more by designers of radar and communications systems.

When employing this basic iterative cell to multiply a four-bit number by another, the interconnection scheme shown in Fig. 3 would be used. Each cell in the array produces a single partial product which is added to the products of equal weight from the cell above it (M), and to the carry from a lower weight cell (K). The sum, S, is fed to the next cell of equal weight, and the carry, C, to an adjacent cell of higher weight.

A significant advantage of the iterative logic scheme is that it is possible to perform addition simultaneously with the multiplication. Thus in the four-bit by four-bit multiplication shown in Fig. 3, it's possible to make two four-bit additions at the same time. One addend is applied along the top and another added along the right edge. The time required for the multiplication is the time it takes to ripple through the longest chain of cells—seven cells in the example.

A basic question is how many functions should be placed on a chip? After all, an inexpensive dual in-line package (DIP) offers a limited number of input and output pins. A single cell on a chip would need eight leads (including two power leads), a two-by-two array would need 14, and a four-by-four array would need 26, as indicated in Table I. A four-by-two multiplier seems to be the best configuration—it requires 20 pins,

2. Symbol and function. The block symbol, at left, represents the basic multiplication cell used in iterative logic. Functionally, the cell consists of an AND gate and a full adder (right). Symbols X and Y are the bits to be multiplied; S is the sum; M represents previous products of equal weight; K is the carry from a previous stage, and C is the carry going to a succeeding stage.



The multiplication problem

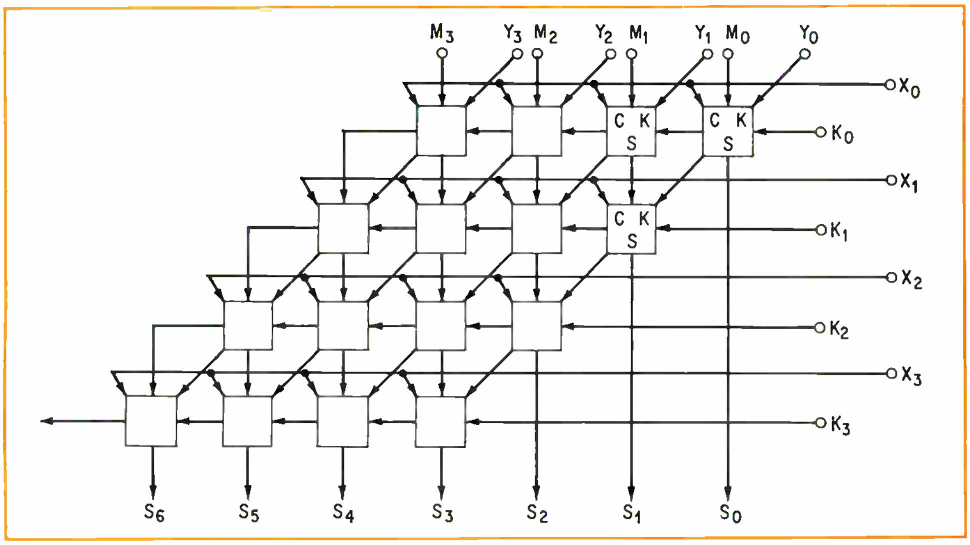
Why does binary multiplication consume so much computer time? The answer lies in the many small, distinct operations taking place: partial products must be formed, and then equally weighted partial products must be added. Consider the multiplication of X and Y, each of four-bit number:

			X_3	X_2	X_1	X_0
			Y_3	Y_2	Y_1	Y_0
			X_3Y_0	X_2Y_0	X_1Y_0	X_0Y_0
		X_3Y_1	X_2Y_1	X_1Y_1	X_0Y_1	
	X_3Y_2	X_2Y_2	X_1Y_2	X_0Y_2		
X_3Y_3	X_2Y_3	X_1Y_3	X_0Y_3			
S_6	S_5	S_4	S_3	S_2	S_1	S_0

Each partial product X_nY_m is formed by taking the AND of one bit of the multiplicand X with one bit of the multiplier Y. A line of partial products is the multiplicand, shifted one place to the left, if the multiplier bit is 1, or the line is all 0s if the multiplier bit is 0. The computer, then, must look at a bit of the multiplier, add the multiplicand if the multiplier bit is 1, shift the sum to the left, and repeat the process for the next bit of the multiplier. Although there are some tricks that can be used to reduce the number of operations (it's possible, for example, to look ahead for the first 1 after a string of 0s and save time by skipping over the 0 bits), multiplication in a series arrangement still involves many steps.

However, multiplication can be speeded up by a parallel process of some kind: that is, by using combinational logic instead of the sequential add and shift method. This is where the iterative cell technique described in this article comes in. Essentially, the iterative cells form several partial products simultaneously, assign a weight to each partial product (equivalent to the column in which the partial product would appear in serial multiplication), and then sum all equally weighted partial products to give the final product.

To dig deeper into the theory of fast multiplication, see K.J. Dean's "Some Applications of Cellular Logic Arithmetic Arrays," *The Radio and Electronic Engineer*, April 1969.



3. Bit by bit. Parallel multiplication of a four-bit X number by a four-bit Y number would require 16 iterative logic cells connected to allow carries and sums of equal weight to be transferred from one cell to another.

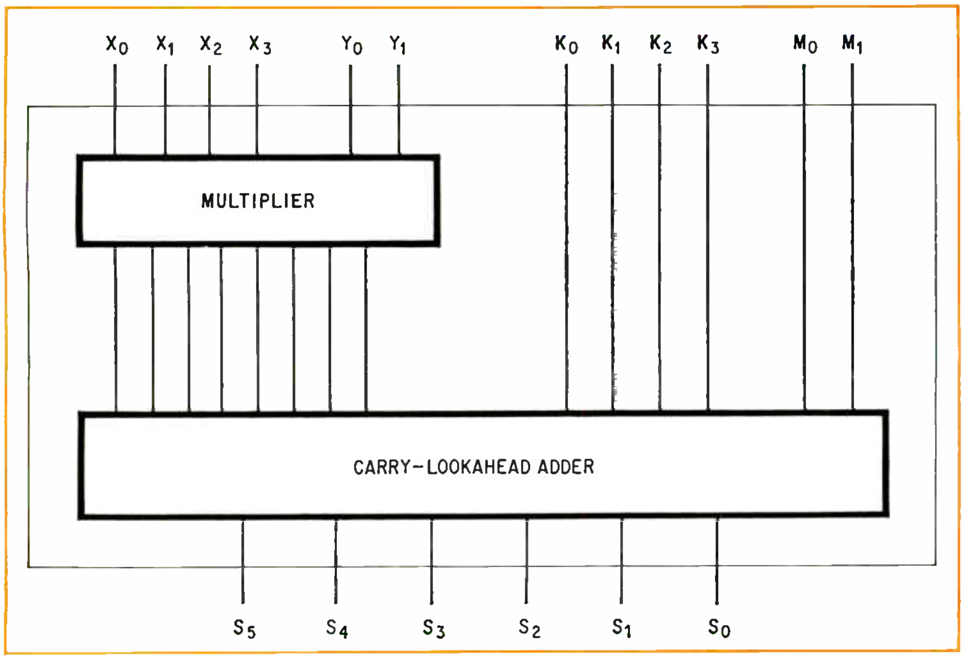
therefore compatible with a 24-lead DIP. If four bits are multiplied by two bits, the largest product that can result is 15 x 3 = 45, which requires all six bits of the output. So, in addition to summing the partial products, it is possible to add a number up to 18 without overflowing the six output bits (whose capacity is all 1s, or 63). The additive inputs are partitioned into a four-bit number K (less than or equal to 15) and a two-bit number M (less than or equal to 3) for the sums and carries from other units. The device now performs the function:

$$S = X \cdot Y + K + M$$
$$S_{max} = 15 \cdot 3 + 15 + 3 = 63$$

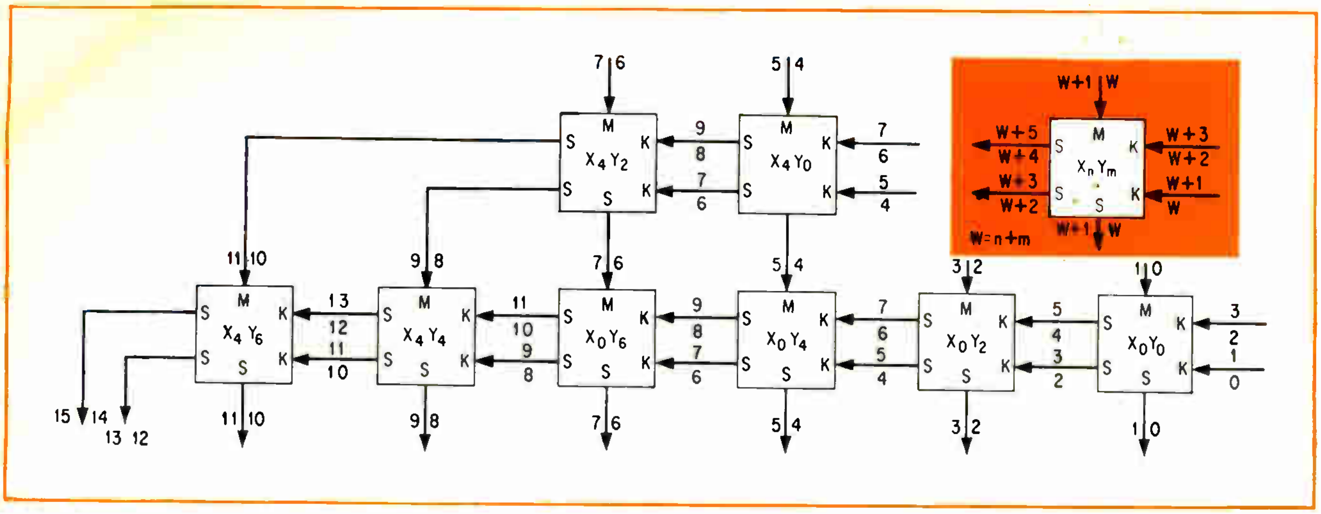
Of these 20 pins, four are required for the X input, two for Y, four for K, two for M, and six for the output as shown in Fig. 4. Two pins are needed for the power supply.

The device can be represented functionally as in Fig. 4 or as a logic block as in Fig. 5. Because the inputs and the outputs are always connected in pairs when the device is used in an array, they have been reduced to single lines in the logic symbol, with weights as indicated. The X and Y inputs are designated X_nY_m, where X_n is a four-bit word whose least significant bit is weighted 2^n and Y_m is a two-bit word with least significant bit weighted 2^m.

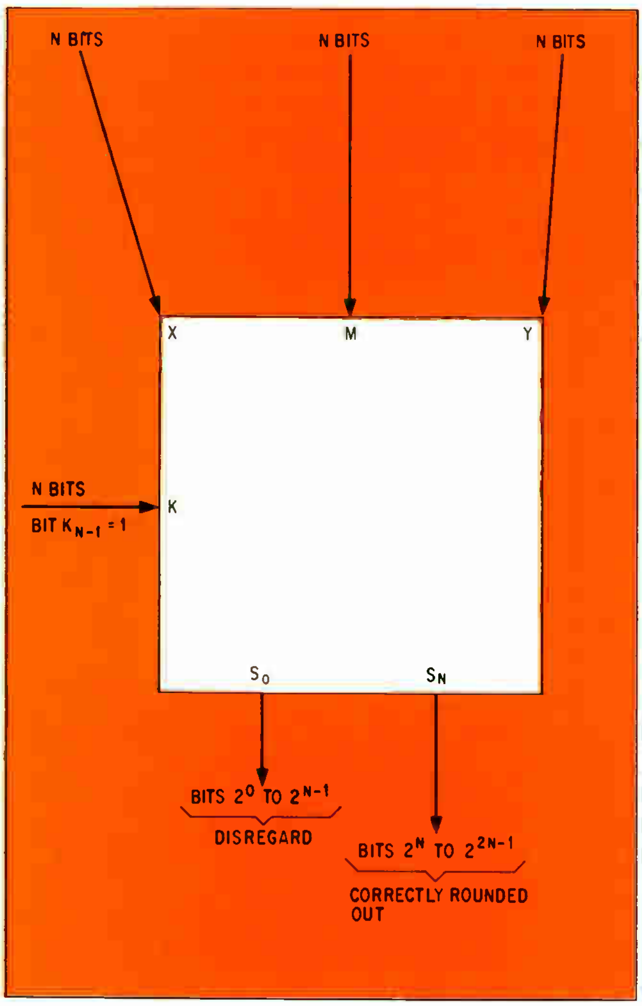
To multiply longer words, such as the two eight-bit words shown in Fig. 5, the building block multiplier cells are interconnected to form all the partial products and to sum all the partial products of equal weight. The arrangement of the multiplier divides each eight-bit word into subwords, each of which will be handled by a different cell. Word X is divided into a four-bit word, X_0, and a four-bit by two-bit product, $X_4 \cdot 2^4$. Similarly, Y is grouped into words and products: $Y_0 + Y_2 \cdot 2^2 + Y_4 \cdot 2^4 + Y_6 \cdot 2^6$ where each Y_n consists of two bits.



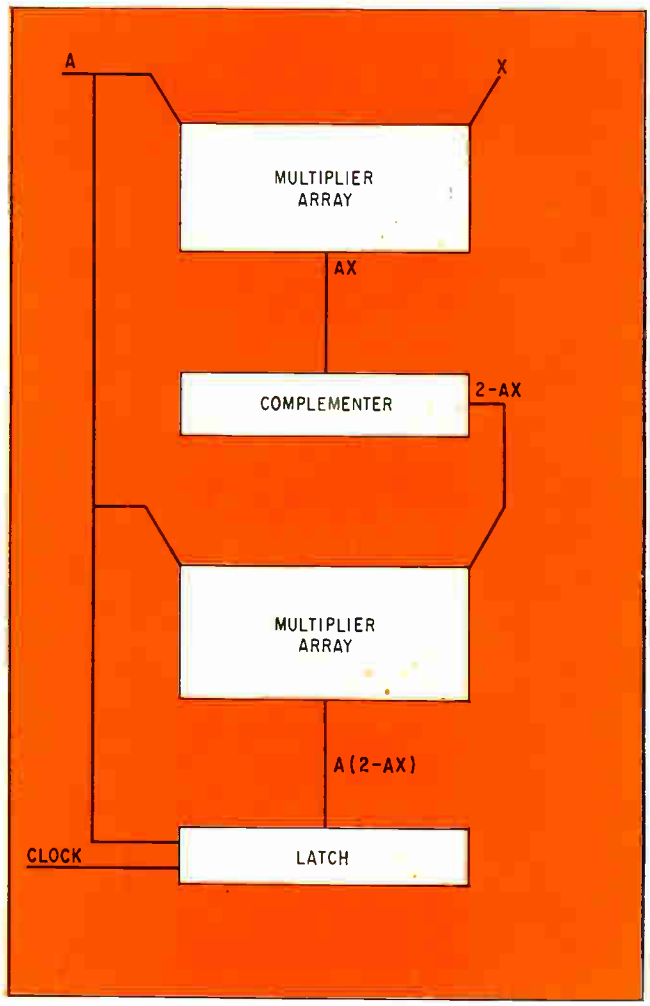
4. Optimum. Considering maximum number of pins available in a dual in-line package, a four-bit by two-bit multiplier seems to be the best choice for the basic multiplier array. This configuration requires 20 external leads, including two (not shown) for the power supply.



5. **Implementation.** To multiply two eight-bit numbers, eight of the two-by-four multipliers are needed. (The simple block at top represents the basic two-by-four multiplier and indicates the weighting factors attached to each of the inputs and outputs.) The interconnections of the blocks, as shown, allows partial products of equal weight to be added together.



6. **Rounding.** Logical 1 applied to the K terminal of the multiplier causes insignificant bits to be discarded and significant bits to be correctly rounded off.



7. **Reciprocal.** To find the reciprocal A of a number X, Newton's approximation can be implemented by two multiplier arrays, or by one array, if a multiplexer is employed.

The multiplication then consists of the following operations:

$$X \cdot Y = (X_0Y_0) + (X_0Y_2)2^2 + (X_0Y_4 + X_4Y_0)2^4 + (X_0Y_6+X_4Y_2)2^6+(X_4Y_4)2^8+(X_4Y_6)2^{10}$$

Each term in parentheses is a partial product formed by a multiplier cell. Representing the product of a four-bit X and a two-bit Y, each term produces a six-bit answer. The cells must be interconnected to insure that bits of equal weight will be summed, as indicated in Fig. 5. The order of summation of the partial products (that is, the path of the sum and carry propagations) is slightly different in an array of four-by-two blocks than it is in an array of individual cells (Fig. 3).

In a four-by-two multiplier implemented at Fairchild using TTL gates (see Fig. 1), to make for flexibility in interconnection of the packages, the $\overline{X}_2$ and X_3 inputs were OR-connected and brought out on the other side of the package with the $\overline{Y}$ inputs. Either the X word or the Y word can be four bits long, with the other word becoming two bits.

To be put into a logic system, the eight-bit by eight-bit multiplier of Fig. 5 would require eight IC packages if the four-by-two multiplier cell were used. As a general rule, the number of four-by-two packages required for an N-bit by N-bit multiplication is $N^2/8$.

Speed of multiplication is the raison d'être for the whole iterative cell scheme. Delay time in the multiplier array is the time required to form and add all the partial products in each package, as well as the time it takes to ripple through the array in the longest cell chain. The most significant delay is that between K inputs and the S outputs, shown in Fig. 5, because this is the longest ripple addition path. In the multiplier chip, the partial products can be formed and added in about 40 nanoseconds, and the K inputs can be added in 24 ns. The general rule is that the time for multiplying N bits by N bits is 40 + (N − 2) 24ns. Table II lists the total multiplication time and the package count for several representative multiplications.

The output of the multiplier array is a double-length word, as indicated in the single block used to represent a multiplier array of any size, Fig. 6. If a shorter result word is desired, the output should be rounded by adding a 1 into the free K input with weight of the highest discarded output. Consider two N-bit words which are multiplied to produce a product with 2N bits. The single-length result is the most significant half of the product, designated S_N and consisting of N bits with weights 2^N to 2^{2N-1}. Rounding should add 1 to S_N if the value of the lower half of the product (S_O) is greater than or equal to $\frac{1}{2}(2^N)$; that is, a 1 should be added to the least significant bit of S_N when the most significant bit of S_o is a 1. This function is performed by placing a 1 on the most significant input to add 1 to bit 2^{N-1}. Then, if the product generates a 1 there, a carry will be added into S_N, and the bits 2^{2N-1} to 2^N will be the accurately rounded result. Bits 2^{N-1} to 2^0, the least significant bits, are ignored.

The multiplier array can also be applied to the important task of finding reciprocals by using the technique of Newton's approximation. For example, the reciprocal of a number X must be found. Stated mathematically, if A_i is an approximation of 1/X, then A_{i+1}, which is equal to $A_i(2 - A_iX)$, is a closer approximation. This particular relation holds for values of X between 0 and 2. The Newton approximation technique is implemented in the multiplier array in the scheme shown in Fig. 7. Starting with an initial value of 1 for A, the product AX is formed in a multiplier. The complement of this product is formed to get 2 − AX. This value, when applied to another multiplier, along with A, produces the reciprocal's approximation, A(2 − AX). By repetition the process will reach the required accuracy. If a multiplexer is used, a single multiplier can perform each of the two multiplications in a separate cycle.

The multiplier story

The Fairchild 9344 full multiplier mentioned in this article appears to be the only such transistor-transistor logic integrated circuit on the market. A designer seeking an alternative way to perform the equivalent high-speed parallel multiplication would have to use several TTL IC packages: NAND gates to form the partial products, and full adders to form the sums of the partial products. If the full adders have a carry-look-ahead capability, the speed of the multiplication would be about as fast as that of the 9344 full multiplier.

Depending on the digital system, there are other alternatives. In a minicomputer, for example, the way to perform multiplication is with read-only memories that store a multiplication algorithm, according to Dale Mrazek, applications engineer at the National Semiconductor Corp. With bipolar ICs used for the ROMS multiplication speed would be high—less than 100 nanoseconds, Mrazek says.

The original proponents of iterative-cell parallel multiplication believed that the technique would first be implemented in metal oxide semiconductor ICs rather than with bipolar because of the greater packing density and lower cost of MOS. The iterative cell approach has not been used, however; multiplication equipment has been designed with adders that operate in the bit-parallel, word-serial mode.

An interesting variation, the series-parallel multiplier, has been developed at the North American Rockwell Microelectronics Co. Words are entered in parallel and multiplied in series. This is a fast arrangement because the multiplication proceeds from the least significant bit of the parallel word. Data can be discarded from the word register and new data entered as the multiplication proceeds. By the time the entire word is multiplied, the word register contains a completely new set of data, and the next multiplication can start immediately.

Surprisingly, there are no true parallel MOS multipliers now on the market. There are, however, a few such circuits being built for in-house use. Sylvania Electronic Systems, for example, is making a four-bit by four-bit parallel multiplier. Such a circuit, however would be "high-speed" only in relation to other MOS circuitry; it would still be considerably slower than a TTL iterative cell array.—GFW

Semiconductor memory systems: How much do they really cost?

Those who seek to avoid high costs of complete systems by starting with packaged chips may wind up paying much more than anticipated once the necessary components, assembly, and testing are factored in

By William Taren, *Cogar Corp., Wappingers Falls, N.Y.*

☐ The seductive sound of low cost per bit is a strong selling point among manufacturers of both core and semiconductor memories. Many buyers seek to avoid the seemingly greater expense of complete memories by assembling their own systems from packaged chips. They have found, however, that the real cost of a memory system—including support components, assembly, testing, and engineering—often turns out much higher than their initial expectations. In fact, the lower the quoted price, the higher the proportionate increase incurred in the ultimate cost.

The tendency to underestimate actual cost took root and still flourishes in core memories. Quoted prices for core memories often exclude necessities such as power supplies, controls for shutting down power in the proper sequence, registers, decoding, and self-testing equipment. Sometimes only cost per bit for a naked core plane is quoted; the purchaser is stuck with the task of assembling the planes into stacks, interconnecting them, and adding the support circuitry.

The very low price quoted by some semiconductor memory manufacturers often covers little more than the equivalent of a core plane. Although the user, in return, gains maximum flexibility for his particular application, he may overlook how much the added hardware and engineering is going to cost him.

In general, the hardware requirements for any semiconductor memory includes, in addition to the storage array itself, such things as support circuit packages, printed-circuit cards, decoupling capacitors, terminators, and connectors. And using these components implies that the purchaser has or will need to have assembly and memory test capabilities.

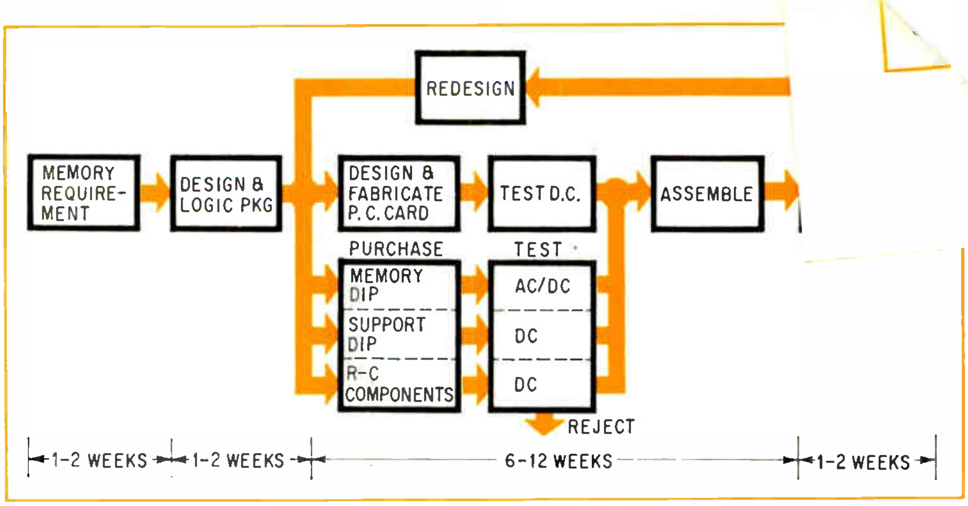
As a basis for examining the cost of these components and operations, look at today's readily available semiconductor memories. These ordinarily come in dual in-line packages with one chip per package; each chip carries from 64 to 256 bipolar circuits or 256 to 1,024 metal oxide semiconductor circuits. Both circuit types sell for about $25 per package. This corresponds to about 40 cents per bit for bipolar circuits with cycle times of 50 to 100 nanoseconds, and 10 cents per bit for MOS cycling at about 1 microsecond.

It's not unreasonable to expect this $25 figure to drop 50% within 1 to 2 years and the MOS cycle time to decrease to about 25% of those quoted. During this time, technological improvements together with lowering prices should make 256-bit bipolar chips and 1,024-bit MOS chips considerably more attractive and widely used than they are today. Such popularity would also bring the price down. By 1972 the price per bit could be down to 10 cents for bipolar and perhaps 2 cents for MOS, presupposing an optimum price/performance ratio for both types.

However, even these projections, once arrived at, still exclude the additional hardware and engineering required to adapt the memories to particular applications. The additional cost depends on the price quoted for the individual package. And although the absolute cost added decreases as the basic cost decreases, it doesn't fall off as quickly, so that the percentage of added cost rises sharply for the lower costs per bit. For example, an unmounted chip in a dual in-line package, at 10 cents per bit costs 2.8 cents, or 28%, more to incorporate in a complete memory. At 5 cents per bit, the necessary extras add 2 cents, or 40%. And where the quote is 1 cent per bit, added outlay cost is 1.4 cents per bit, or 140%.

The first and most obvious additional expense is support circuitry for the memory. This includes selection and decoding, to pick out one of a number of DIPs on a single printed-circuit card; latches, for address and data input and output; and timing pulse generators. Furthermore, if the memory circuit's output is at a logic level unacceptable to such standard logic circuit forms as diode transistor, transistor transistor, or emitter coupled, more support circuitry is necessary to convert from the memory level to the logic level or vice versa.

After the memory circuits and the support circuits have been purchased, the DIPs are still up in the air, so to speak: they need a printed-circuit card to hold them. The size and number of pc cards required depends on the kind of memory being built. A small buffer, for example, containing 256 words of 16 bits each would need 64 memory packages of 64 bits each, along with another 12 to 24 packages containing support circuitry. This number of packages might be possibly mounted on one card; however, if two cards



are needed, a few more packages would be required to compensate for longer signal paths. In a few cases one DIP occupies no more than a square inch; 1½ to 2 in.² is more typical, leaving space for interconnections and for connectors, test points, and stiffeners. Today the larger pc cards have an effective area of 60 to 120 in.² Thus a single card can't hold the 256-by-16 buffer mentioned; two cards are necessary, together with extra support circuits.

A typical main memory for a minicomputer contains 4,000 words of 16 bits each, and can be packaged in 256 DIPs, each containing 256 bits in MOS circuitry. To these should be added 24 packages of support circuits, all of which should require about six pc cards. A larger memory is likely to have an even larger proportion of support packages.

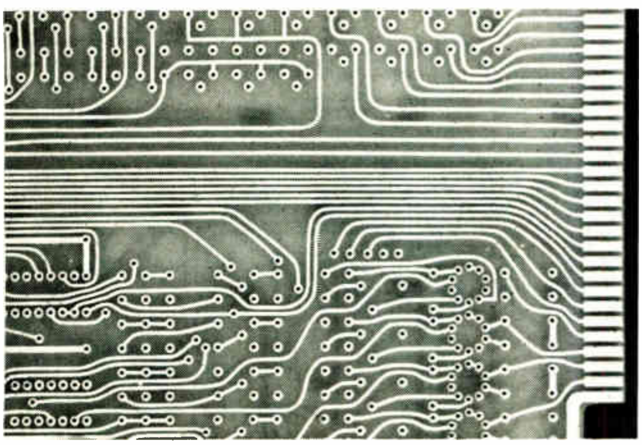
Packages in a memory can be fitted more closely together on the pc card than the above figures suggest, if one spends more time and money designing the voltage and signal distribution system, or if the memory system's performance objectives are adjusted to permit the dense packing. Another factor that controls packing density is the available laminating and etching facilities for making the cards.

For example, a double-sided pc card with gold-plated card tab connections and no internal interconnection planes costs around 20 cents per square inch. Adding multiple internal planes increases the cost radically, as does the use of conductive line widths and spacings as little as 0.010 in.; the cost may reach $2 per in.², but performance of the system, interconnection problems or noise may justify the expenditure. In any case, it's much less expensive to solve these problems at an early stage in the design than to grapple with them after a system has been installed.

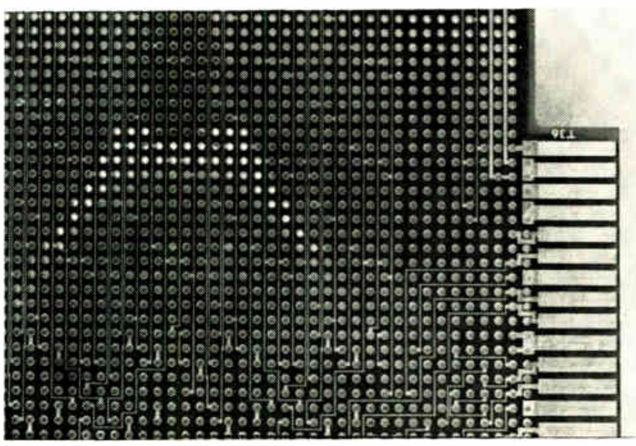
Not all the components of a memory assembly are high-technology devices or expensive frills. Take decoupling capacitors and terminating resistors, for example. The capacitors cost maybe 25 cents to a dollar, and the resistors are at the nickel and dime level. These necessary components add perhaps $2.50 to $7 to the cost per card.

This takes care of all the components required for assembling a semiconductor memory on a production-line basis. And at this point another cost factor raises its head—inventory. To support normal manufacturing procedures, at least a six week's supply of all components should be kept on hand. Inventory includes not only the cost of the stocked pieces themselves, but also the interest on the investment the stock repre-

Double-sided. This pc card's wiring is much denser than that on the multilayer card at right.



Multilayer. Simpler connections and higher performance are obtainable at the cost of extra internal planes.



Summary of a memory's true cost

A. Cost of testing DIPs
1. First tester
   a. Capital depreciation $50,000 based on purchase price of $150,000, five year life, no salvage value, and sum-of-digits depreciation
   b. Cost of operation in man-years

Operator	1.0
Supervision	0.2
Load, unload	0.5
Programing	0.5
Documentation	0.5
Returns to vendor	0.2
Maintenance and calibration	0.5
Inventory and miscellany	0.4
Total man-years	3.8

3.8 man-years @ $26,000 = $100,000

Rate includes wages, support costs, fringe benefits, etc.

2. Additional testers
   Each tester tests 500 DIPs per hour maximum
   Shifts are 8 hours, shift efficiency 0.6, less than 1.0 because of operator breaks, maintenance, and other pauses. If the production rate is higher, more than one tester is necessary. Additional testers have the same capital depreciation but only half the operating cost, because of functions shared with the first tester.
3. Total cost of testing
   a. Number of DIPs
   = (500 DIPs/h) × (8 h/shift) × (0.6 shift efficiency) × (5 shift/wk) × (50 wk/yr) = 600,000 DIPs/yr per tester
   b. Cost per DIP, first 600,000 = 25 cents
   c. Cost per DIP over 600,000 = 17 cents

Total cost:
$D_y[(1 + R_d)(1 + R_s) - 600{,}000] \times 0.17 + 150{,}000$

B. Cost of raw cards
$= (B_y/B_d)(1 + R_d)(1 + R_s)(A_d)(C_c)$
$= (D_y)(1 + R_d)(1 + R_s)(A_d)(C_c)$

C. Cost of support DIPs
$= (D_y)(R_d)(C_s)(1 + R_s)$

D. Cost of termination and decoupling
$= (C_t/D_c)(D_y)(1 + R_d)(1 + R_s)$
$= (C_t/D_c)(D_{yg})$

E. Cost of storage DIPs $= (D_y)(1 + R_s)(C_{sd})$

F. Cost of assembly $= (D_{yg})(C_a)$

G. Cost of card test $= (D_{yg})(C_{ct}/D_c)$

H. Cost of inventory $= (I)(T/52)(D_{yg}) \times [(A_d)(C_c) + (C_t/D_c) + (C_s) + (C_{sd})/(1 + R_d)]$

J. Cost of DIPs rejected at incoming inspection
1. Number of faulty DIPs $= (R_i)(D_{yg})$
2. Number of faulty DIPs rejected $= (E_i)(R_i)(D_{yg})$
3. Cost of rejected DIPs
   $= (E_i)(R_i)(D_y)(1 + R_s)(C_sR_d + C_{sd})$

K. Cost of card repair, as a result of faulty DIPs that pass incoming inspection
1. Number of faulty DIPs installed in cards
   $= (1 - E_i)(R_i)(D_{yg})$
2. Number of cards repaired at card test level
   $= (E_t)(1 - E_i)(R_i)(D_{yg})$
3. Number of cards repaired at system test level
   $= (1 - E_t)(1 - E_i)(R_i)(D_{yg})$
4. Cost of repair, card and system test levels
   $= [(C_{ra})(E_t) + (C_{rs})(1 - E_t)][(1 - E_i)(R_i)(D_{yg})]$

L. Cost of quality and reliability test samples
$= (C_sR_d + C_{sd})(R_q)(D_y)(1 + R_s)$

Definitions

Symbol	Definition	Example	Symbol	Definition	Example
A_d	Card area per DIP	1.5 in.^{2}	D_c	DIPs per card	40
B_d	Bits per DIP	256	D_y	DIPs per year net $= B_y/B_d$	
B_y	Bits per year	100 million	D_{yg}	DIPs per year gross $= D_y(1 + R_d)(1 + R_s)$	
C_a	Assembly cost per DIP	$ 0.10			
C_c	Cost per in.^{2} of card	$ 0.50	E_i	Efficiency, incoming inspection	70%
C_{ct}	Testing cost per card	$ 5	E_t	Efficiency, card test	80%
C_{ra}	Cost per repair at card level	$ 20	I	Interest on investment	8%
C_{rs}	Cost per repair at system level	$200	R_d	Ratio, support to storage DIPs	1:3
C_s	Cost per DIP, support circuit	$ 2	R_i	Rejection rate, incoming inspection	2%
C_{sd}	Cost per DIP, storage circuit		R_q	Sample rate, reliability check	1%
C_t	Cost per card, termination and decoupling	$ 4	R_s	Proportion of spares at DIP level	1:10
			T	Inventory and assembly time	12 weeks

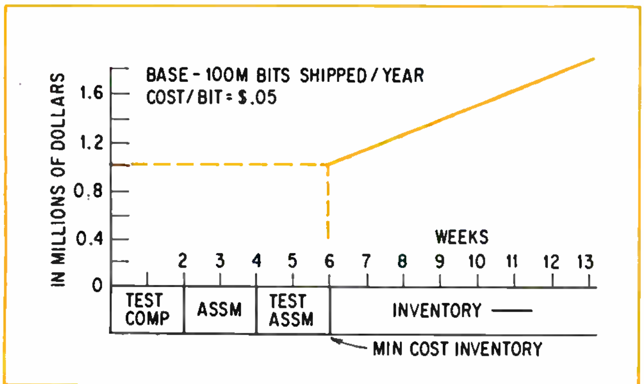
Expensive but invaluable. Although testing equipment like this is almost frighteningly expensive, its use on purchased components is essential. Its rejection rate may be as high as one component in 10.

sents. This interest period begins when the stock appears on the shelf and continues through the assembly process. An inventory time of six weeks and an assembly and testing time of six weeks make the total investment period 12 weeks; if the stock to produce 100 million bits costs $6 million, the interest over a 12-week period at 8% is over $100,000.

All components are presumably tested by the supplier before shipment. Nevertheless, the user must test them again. Past data on medium-scale integrated logic circuits indicates that rejection rates at incoming inspection are likely to be between 1% and 10%—much too high to be neglected.

A purchaser may be tempted to minimize these rejection rate percentages when he looks at the $50,000 to $250,000 price for functional memory component testers. Furthermore, the tester's cost of operation per year can equal the required initial capital investment. However, these dollar outlays can be justified if the testing facilities have a high throughput: 250 to 300 DIPs per hour, on a single work shift for the year, add

Shelf cost. The sooner tested assemblies can be shipped after completion, the less their total cost.



Cost summary For shipping 100 million bits per year

All figures in thousands of dollars

Item	In 256-bit chips*			In 64-bit chips**
	10¢/bit	5¢/bit	1¢/bit	10¢/bit
A. Testing DIPs	160.0	160.0	160.0	436.9
B. Raw cards	429.6	429.6	429.6	1,716.0
C. Support DIPs	283.6	283.6	283.6	1,166.0
D. Termination/decoupling	57.4	57.4	57.4	228.8
E. Storage DIPs	11,000.0	5,500.0	1,100.0	11,000.0
F. Assembly	57.3	57.3	57.3	228.8
G. Card Test	71.6	71.6	71.6	286.0
H. Inventory	213.2	114.7	33.7	339.1
J. Rejected DIPs	158.0	81.0	19.4	218.3
K. Card repair	196.0	196.0	196.0	769.4
L. Quality, reliability	165.4	57.9	13.9	123.2
Totals	12,792.1	7,009.1	2,422.5	16,512.5
Total cost/bit	$.128	$.07	$.024	$.165

*In dual-in-line packages, 4K by 16 bit system

**In dual-in-line packages, 256 by 16 bit system

up to more than 500,000 DIPs or 100 mi

Unfortunately, even at these produc

dollar outlays, no component tester is

mally 60% to 90% effective, the testers

a few bad, marginal, or intermittently

nents slip through to inventory. In th

500,000 DIPs per year mentioned prev

2% incoming defect level, between 1,(

faulty units each year can make it to the shelves.

In addition to incoming inspection, all purchased components should be subjected to a quality-control or reliability test—a destructive procedure. Although the proportion of parts used for this purpose can be decreased after an extended period of purchasing from well-qualified vendors, the tests will still consume anywhere from 0.1% to 2% of incoming parts.

Assembling these components to the cards, with the attendant soldering, marking, and inspection operations is the next cost item. With automatic insertion and wave-soldering equipment, the amortized cost for assembly averages 5 cents per component; but if cards of many types are produced in low volume, the cost can easily reach 20 cents per component.

To a great degree the total cost involved in these operations is inversely related to the investment in card assembly equipment. For example, if a 256-bit MOS DIP costs $25 and if 40 of these are used per card, then the card costs $1,000—not counting the card itself or any other components mounted on it. If the least expensive assembly process spoils 1% of the cards produced, this effectively adds $10 to the card cost, or 25 cents for each DIP. But if spending an extra nickel per component on assembly equipment —such as automatic insertion machines—eliminates the spoilage of cards, the investment is worth while. In fact, the investment proves valuable if the cost increment is less than the 25 cents per component that the cost of spoilage—provided, of course, that the costlier equipment does reduce spoilage measurably.

After soldering, the assembled card must also be tested—to screen faulty assemblies, not to repair them. Screening is usually a semiautomatic operation; the cards are plugged by hand into a test fixture, and a computer-controlled test sequence compares the cards with a set of performance specifications, including a full range of power supply and timing variations. These tests, depending on their degree of complexity can cost as little as $1.50 per card or as much as $10—but, like the component tests, they still are not perfect. In any event, the identified bad cards must be repaired—another cost item.

Unquestionably, the most expensive place to find a failure is at the system level—when the flaw that got past the component test and the card test finally shows up. The cost includes the down time for the system as well as the cost for labor and equipment to locate and repair the failed component. The time involved ranges from an hour to a full day, and the costs, if a large system is down, runs into thousands of dollars.

Although far from complete, this analysis of the true cost of a semiconductor memory provides a relative guide. The costs are summarized on page 96. ☐

Designer's casebook

Designer's casebook is a regular feature in Electronics. Readers are invited to submit novel circuit ideas and unusual solutions to design problems. Descriptions should be brief. We'll pay $50 for each item published.

Op amps form self-buffered rectifier

By Jerald Graeme

Burr-Brown Research Corp., Tucson, Ariz.

A new design for a precision full-wave rectifier uses two operational amplifiers and two diodes and eliminates the need for a buffer. Self-buffering occurs because the input signal sees the high common-mode input resistances of the amplifiers rather than the conventional summing resistors.

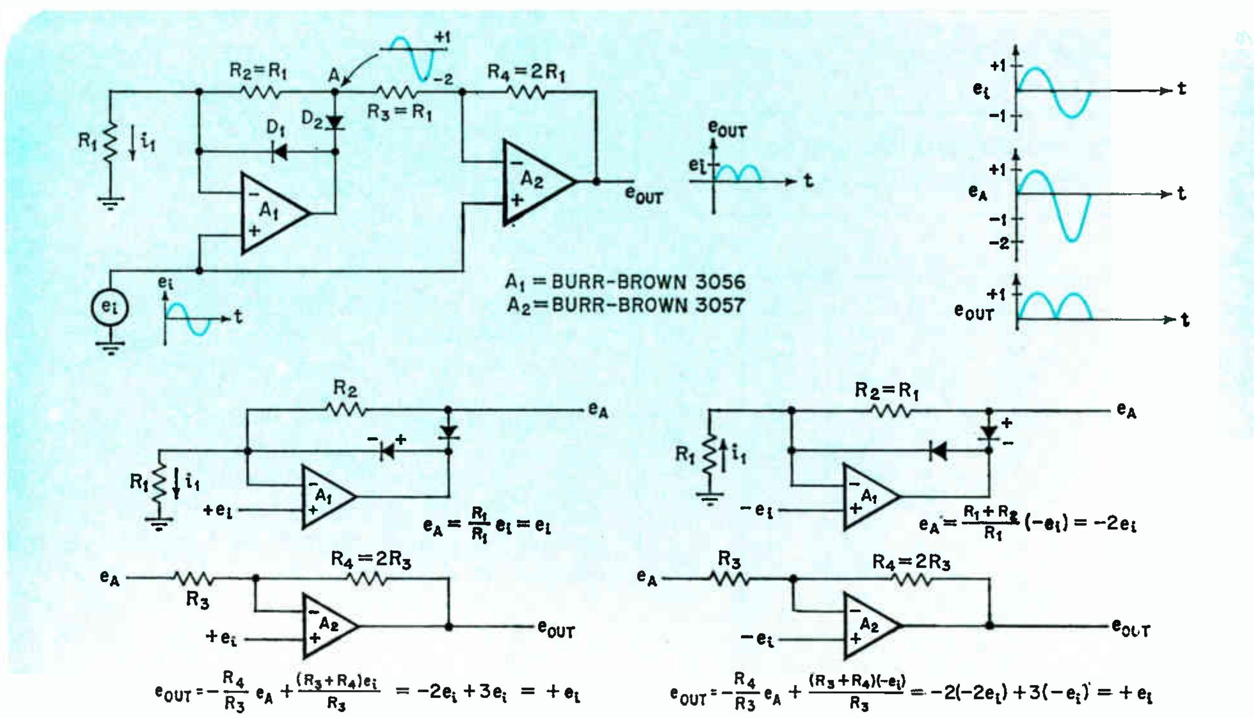
Amplifier A_1 sets up A_2 to complete the rectification process, but not in the same manner as the classic design. Instead of being a half-wave rectifier, A_1 provides a gain of unity if signal e_i is positive and a gain of two if e_i is negative. Then A_2 inverts and doubles the first-stage output giving the input signal a gain of three. Thus, an over-all gain of ± 1 is achieved and a positive output having the absolute value of the signal voltage results.

The partial schematics break down the operation into bite-sized chunks. A_1 develops a positive current i_1 through resistor R_1 with $+e_1$ at the input. The current must go through rectifier D_1 because the amplifier input cannot supply the current and because D_2 is reverse-biased by current of this polarity. Thus forward-biased, D_1 turns on, shorting R_2 out of the feedback path. The gain of A_1 is held to unity, and voltage at node A rises only to $+e_i$.

Conversely, when e_i goes negative, i_1 becomes negative, D_1 turns off and D_2 turns on. Now, the gain goes to 2, and node A goes to $2e_i$.

Stage A2 sums $-2e_i$ and $+3e_i$ at node B, resulting in an output of $+e_i$ regardless of the polarity of the input. The signal-input impedance remains at about 25 MΩ when bipolar-input amplifiers are used and about $10^{11}\Omega$ with FET input op amps. The external resistances have a negligible effect on input characteristics, eliminating the need for a high-impedance input buffer.

Where's the buffer? There is no buffer. Another high-input-impedance op amp is not needed because the signal input always sees a high resistance in the amplifier inputs. The conventional summing resistors are avoided by establishing A_2's output as the sum of $-2e_A$ and $+3e_i$. The output is $(-2e_i + 3e_i)$ or $(+4e_i - 3e_i)$.



Rf linear IC squares high-frequency sine waves

By Norman Tweit and Wes Vincent

Motorola Inc., Scottsdale, Ariz.

Squaring high-frequency sine waves with amplitudes up to about 10 V peak-to-peak is an easy task for low-cost rf linear IC amplifiers. The cascode-connected type of rf/i-f monolithic amplifier needs only an output driver to complete the squaring circuit.

Normally, the automatic gain control function for the IC calls for the differential amplifier to start switching when a control voltage is at a threshold near ground. When the agc voltage on the base of Q_2 increases, Q_2 takes more and more of the emitter current provided by Q_1 and shunts the rf or i-f input signal away from the output transistor, Q_3.

Detecting the zero crossing of a sine wave follows a similar procedure. The sine wave replaces the agc signal, no rf signal is applied to the input stage, and the differential amplifier is biased around ground. In the squaring circuit, the IC substrate is connected to the negative supply voltage.

Q_1 supplies current by switching between Q_2 and Q_3 as the level of the sine wave changes. When the sine wave drops toward zero, Q_3 comes on. The selected value of resistor R_1 allows Q_3 to saturate while biasing off the npn driver transistor, Q_4. The output rises to the supply level of 5 V and remains there until the sine wave comes back up toward zero.

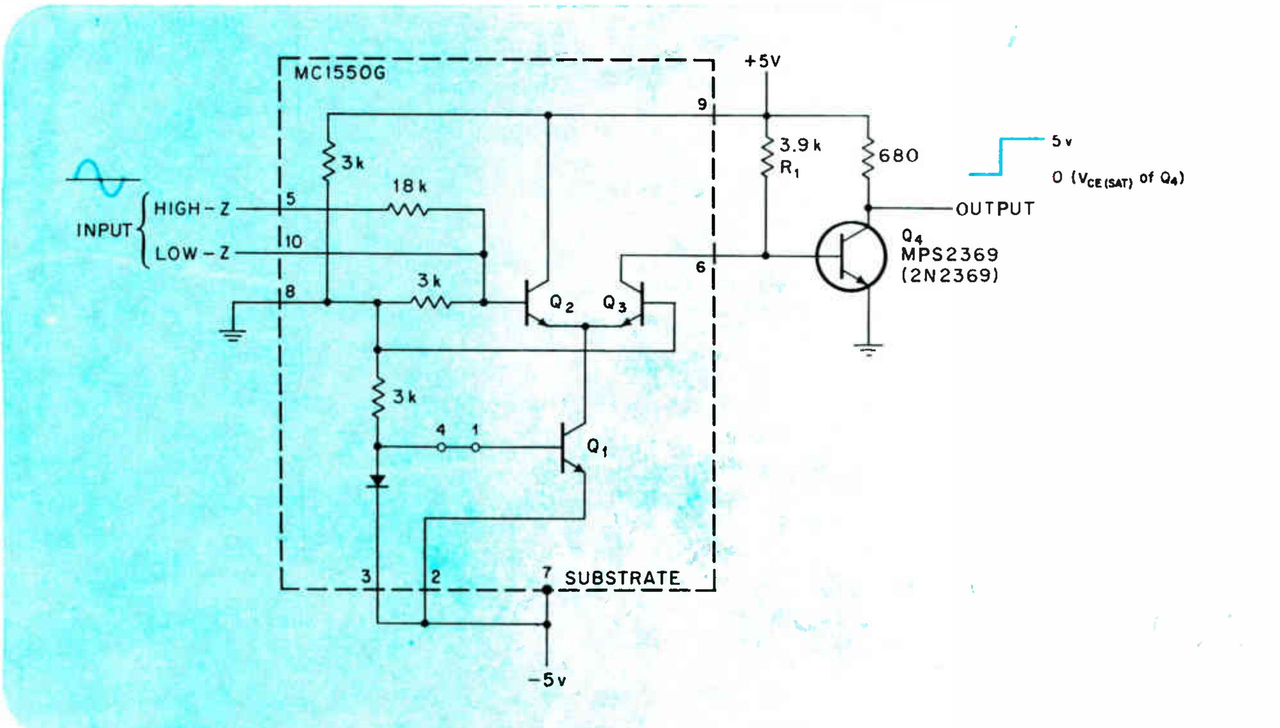
As the input continues rising, Q_2 turns on and Q_3 turns off. When Q_3 is off, its collector is clamped by the base-emitter diode of Q_4, and Q_4 saturates. The output drops to a zero level equal to $V_{CE(sat)}$ of Q_4. The turn-on time for Q_4—about 10 ns—defines the output rise time; the fall time is 25 ns.

The IC supply voltage specifications limit sine-wave amplitudes to a range from about 500 mV peak-to-peak to 10 V pk-pk. Feedthrough at the larger amplitudes—a common problem in Schmitt-trigger types of squaring circuits—doesn't occur. This circuit has an output symmetry of 90% or better to 1 MHz and about 80% at 5 MHz.

The sine wave can be applied to the IC's high-impedance or low-impedance input. The low-Z input gives the best threshold, about 500 mV pk-pk. The 18-kilohm resistor raises the impedance of the low-Z input to form the high-Z input at the cost of reduced threshold.

Together, the IC and the output driver transistor cost about $2.

Round in, square out. Sine-wave control input to Q_1 and Q_3 switches output transistor Q_3 of cascode-connected amplifier on and off. Resistor R_1 makes Q_3 saturate quickly, turning off Q_4 quickly. When Q_3 turns off, Q_4 saturates rapidly. This action gives the output square wave nanosecond rise and fall times, with excellent symmetry.



Stable unijunction VCO needs no critical components

By L. G. Smeins

Ball Brothers Research Corp., Boulder, Colo.

Placing a unijunction transistor and an integrator together produces a voltage-controlled oscillator with more temperature stability than a unijunction VCO and more linearity than an ordinary integrating oscillator.

Unijunction transistor Q_1 serves as a voltage-sensitive reset switch in a Miller integrator formed by amplifier A_1, capacitor C_1 and input resistor R_1. Temperature coefficients are predominantly those of the RC network components, which can be low-drift types. Also, the reset time of Q_1 rather than the output current limit of A_1 determines the linearity of the VCO.

The oscillator's period is

$$t = \frac{C_1(\eta V_{B2} + 0.4)}{I_{in}(1 - \eta)}$$

where η is Q_1's intrinsic standoff ratio, V_{B2} its base-2 voltage and 0.4 its emitter-voltage recovery time (characteristically 0.4 microsecond at C = 0.01 microfarad).

The output of A_1 goes through a peak-to-peak rectifier (D_1, D_2 and C_2, C_3) and a filter (R_2, R_3 and C_3, C_4). Comparator A_2 compares the peak-to-peak value with a reference voltage V_{REF} set by zener diode D_3. The voltage drops through D_1 and D_2 are canceled by D_4 and D_5.

A_2's output drives base 2 of Q_1. Since V_P depends on V_{B2}, the system will seek a level at which the peak-to-peak voltage at the output of A_1 equals V_{REF}. Placing a resistor, R_4, in series with base 2 compensates for the negative coefficient of V_D.

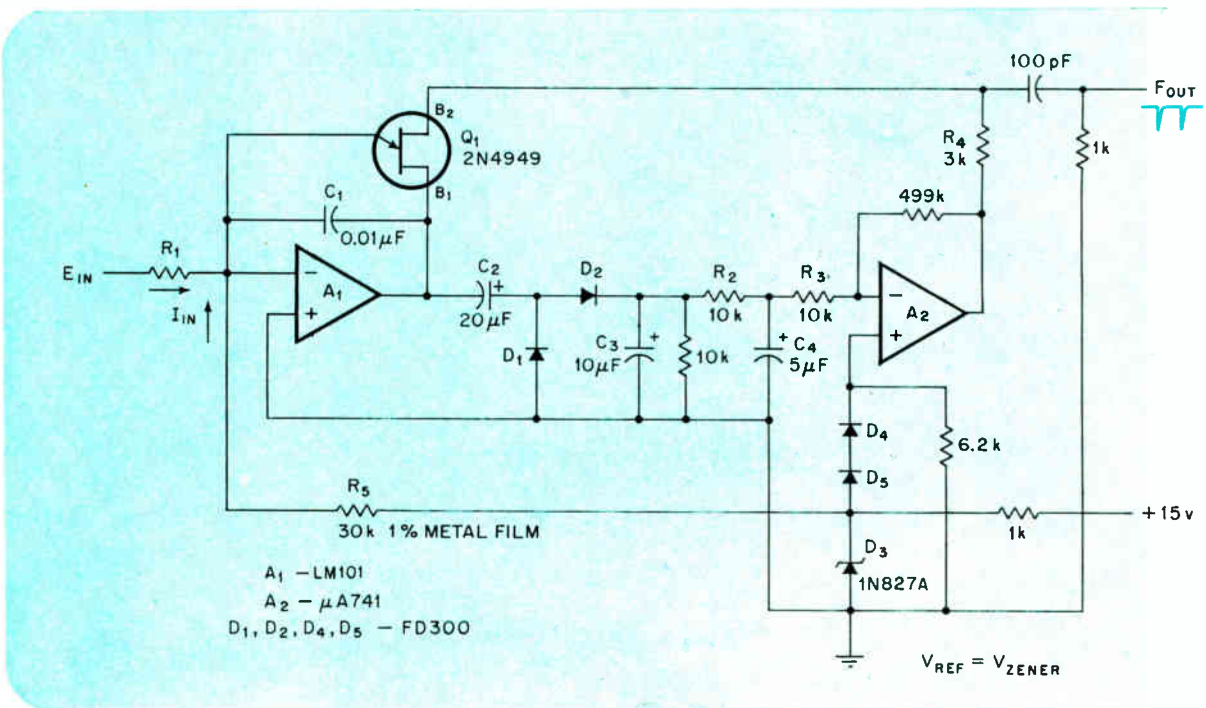
With the closed-loop gain of A_2 now much greater than one and the integrator getting dc feedback through R_5, the oscillation period becomes

$$t = \frac{R_1 R_5 C_1 V_{REF}}{R_5 E_{in} + R_1 V_{REF}}$$

The values shown give a center frequency of approximately 3 kHz, but component values do not have to be specially selected. If C_1 has a temperature coefficient of 100 ppm/°C and the resistors have one of 50 ppm/°C, the VCO coefficient will be about 100 ppm/°C. A voltage follower can drive R_1 if a high input impedance is needed.

Reliable oscillation requires that the current to C_1 be between Q_1's peak-point emitter current I_P and its valley current I_V. In addition, the filter's time constant should be much longer than the period of oscillation, and R_6 should be large enough to allow Q_1 to fire when A_2 is saturated in the positive direction.

All-weather VCO. Temperature coefficients of RC network's passive components limit voltage-controlled oscillator's drift. Unijunction transistor Q_1 is a voltage-sensitive reset switch in integrator A_1. Comparator A_2 stabilizes output, keys period and level to reference voltage.



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Circle 101 on reader service card

Help yourself to a good dc-to-dc converter design

Simple equations used with cores and transistors provide basis of transformer design for top performance

By Del Johnson,* *Lear Siegler Inc., Cimron division, San Diego, Calif.*

☐ Dc-to-dc converters offer a compact, economical way to supply several different isolated voltages from a single dc input. These features find ready applications in aerospace work and the growing battery-powered instrumentation field. In ac line-operated equipment the device can replace several regulated voltage supplies. And there's a bonus—the converter is inherently immune to short circuits, and usually restarts when the short is removed.

Dc-to-dc converters can be described in a few equations which do provide the basis for any design. Further, this straightforward design approach is theoretically rigorous and almost devoid of trial-and-error routines.

In designing a typical converter, the first step is to select the core. In cross section, it should be just large enough for the applied voltage to induce a saturation level of flux every half cycle. In window area—the area available for building up the windings—it must be of a size that accommodates all the windings necessary.

The core usually is a tape-wound toroid made from 50% nickel-iron alloy, a material that exhibits a very square, very narrow hysteresis loop; these cores are small and cost only a few dollars. But any other type that satisfies the size, cost and operating-frequency requirements may be used.

Manufacturers tabulate core sizes by the product of window area, W, and cross-sectional area, A_C. On page 104 is a short list of commercially available tape-wound toroids.

To discover the value needed for WA_C, an equation in terms of known parameters is derived from

$$e = N\,d\phi/dt$$

This is the basic equation that defines how the voltage applied to an N-turn coil is related to the rate of change of flux. Once WA_C is known, its equation can be used for the second step of the design—finding the number of primary turns, N_P.

Because voltage applied to the converter is constant, $d\phi/dt$ is too. And since this voltage is applied to only half the primary, N equals $N_P/2$. So the basic equation can be rewritten as

$$E\Delta t = (N_P/2)\Delta\phi$$

In one half cycle of operation, T/2, the core flux goes from the saturation level in one direction to the saturation level in the other. Therefore $\Delta\phi$ equals $2B_MA_C$, where B_M is the saturation flux density. Expressing the period as the reciprocal of the operating frequency, f, and solving for the cross-sectional area leads to:

$$A_C = \frac{E}{2B_M N_P f}$$

Before finding an expression for W, it's necessary to estimate the fraction of window area that the primary will take up. Since the transformer can become difficult to wind, the primary and secondaries together shouldn't occupy more than 40% of W. In most cases if it's estimated that the primary will take up 20% of W, the final window utilization factor will be less than this 40% figure. In any event, if this fraction of the total space occupied by the primary is called k, the window area is given by

$$W = N_P A_W/k$$

where A_W is the cross-sectional area of the primary wire. The value is found by summing the power requirements of the secondary windings, estimating the converter's efficiency, and calculating the required amount of primary current. Since each half of the primary conducts only during alternate half cycles, the wire need only be capable of handling half the primary current. Its gauge can be determined from a standard wire table.

Combining the equations for A_C and W, and including the conversion factor 10^{-8} to allow all parameters to be expressed in their usual dimensions, yields

$$WA_C = \frac{EA_W}{2B_M kf \times 10^{-8}}$$

where W is in square centimeters; A_C and A_W are in circular mils; B_M is in gauss and is specified by the core manufacturer; f is in hertz and is specified by the core manufacturer; and E is in volts.

The calculated value of WA_C is a minimum. To accommodate a standard core size a larger value may have to be used, though this will of course result in a larger transformer with fewer turns.

After a core with above the minimum WA_C has been selected, step two of the calculations is reached—determining the number of primary turns. This is done by rearranging the equation for WA_C, using the value for A_C given for the core in the manufacturers data (see typical table on p. 104)

* Mr. Johnson is now with Deltec, San Diego, Calif.

$$N_P = \frac{E}{2B_M A_C f \times 10^{-8}}$$

The number of turns in the feedback winding, N_F, depends partly on the voltage, E_B, which the primary induces in the feedback winding and which provides the forward and reverse bias that alternately switches the transistors. In the positive direction, E_B is clamped at the transistor's base-emitter saturation level, $V_{BE(SAT)}$. But if the reverse bias that appears across the conducting transistor is to stay within safe operating units, E_B must be less than the sum of the magnitudes of $V_{BE(SAT)}$ and the transistor's base-emitter breakdown voltage, BV_{BEO}.

With the value of E_B known, N_F can be calculated from

$$N_F = E_B N_P / 2E$$

To insure that the transistors will switch the desired primary current, the base current, I_B, of the conducting transistor must be at least equal to the primary current divided by the forward current transfer ratio, h_{fe}. The actual value of I_B depends on the parallel combination of R_1 and R_2, called R_P, which can be expressed in terms of known parameters

$$R_P = \frac{GE - E_T}{I_B}$$

The voltage E_T is the potential at the center tap of the feedback winding, with the short-duration voltage spike being ignored. It's given by

$$E_T = V_{BE(SAT)} - E_B/2$$

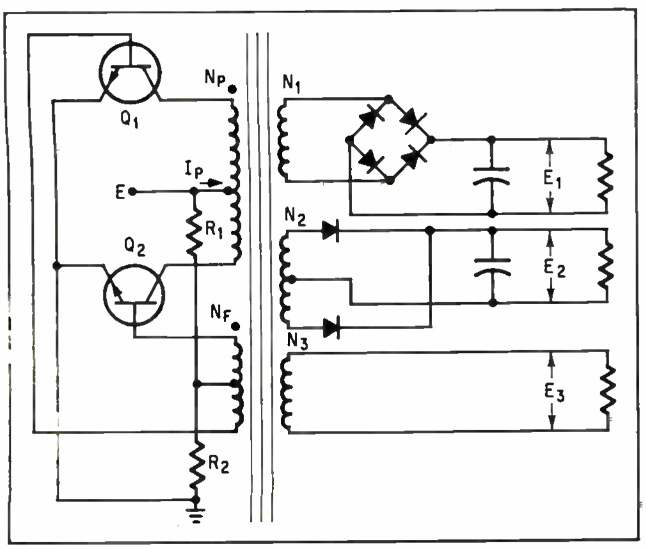
The symbol G is the divider ratio given by

$$G = \frac{R_2}{R_1 + R_2}$$

and is picked to insure safe and reliable starting of the converter. Usually a value between 3 volts and 6 volts across R_2 when the divider isn't loaded should suffice. With this criterion G should be between 3/E and 6/E.

Once R_P and G are known, the actual resistances of the divider network can be found from

$$R_1 = R_P/G$$
$$R_2 = R_P/(1 - G)$$



1. Many from one. A dc-to-dc converter produces several square-wave voltages from a single dc source, E. Each of these voltages is isolated and, if desired, can be rectified. In a typical converter, the transistors alternately switch the primary current whenever the flux density in the core reaches the saturation level. The feedback winding, N_F, provides the switching signal to each transistor that turns one on and the other off.

Once through the circuit

The converter works by periodically saturating the core and thereby inducing square-wave voltages in the secondaries. When power is first applied to the primary's center tap, current tries to flow to the bases of both transistors. But, since they're not perfectly matched, one turns on before the other can. With one transistor conducting, the input voltage, E, is applied across half of the primary and, being constant, causes the flux density to increase linearly. While the flux is growing, the current in the primary is almost constant since it's proportional to the magnetizing force, H.

The linearly changing flux induces a constant voltage in the secondaries—the load windings and the feedback winding. In the latter the voltage supplies a forward bias to the conducting transistor and a cutoff bias to the nonconducting one.

When the flux density reaches the core's saturation level, B_M, the primary impedance and mutual inductance drop to very low values. As the impedance falls, there's a momentary surge in the primary current. Nevertheless, since there's no significant voltage coupled to the feedback winding, the conducting transistor turns off. Within a few microseconds, an inductive transient caused partly by residual inductance in the windings reverses both the base bias conditions. The other transistor turns on, and E is applied to the other half of the primary. The exact mechanism of this field reversal in the core isn't perfectly understood, but the result is that the core comes out of saturation and couples a positive bias to the base of the transistor that's now conducting. So the flux goes to saturation in the opposite direction, completing the cycle.

The kind of short-circuit protection provided by the dc-to-dc converter is unique—and needs no additional circuitry. A secondary short causes a very heavy primary current, the equivalent of the collector current that flows at the instant of core saturation. Since the resistor-limited base current of the conducting transistor cannot maintain saturation, the transistor moves out of saturation as if to begin the switching that occurs at the end of each half cycle. However, because of the short, the primary impedance remains low. So the collector current in the second transistor is also too high to permit the base current to maintain saturation. The oscillation stops, and all the secondary voltages drop to zero. Usually, the oscillator will restart when the secondary short is removed.

Once with numbers

Suppose that the converter in Fig. 1 is to operate from a 24-volt battery, and supply 22 v dc at 120 milliamps, 5 v dc at 1.5 amps, and 10 v peak-to-peak at 10 mA to the loads.

The size of the converter will depend on its operating frequency, which in turn will depend on the nature of its core. A good compromise between cost and bulk is a nickel-iron toroid. Several of these are listed below, where they are tabulated by the product of their window area, W, and cross-sectional area, A_C.

The first step in finding the product required for the core is to determine the size of the wire needed for the primary, which depends on the primary current. To find its value, the power demands of loads are summed

$$P = (22 + 2)0.12 + (5 + 1)1.5 + (10/2)0.01$$
$$= 11.93 \text{ watts}$$

where the 2-v and 1-v terms are the drops in the rectifiers. Next it's necessary to know the converter's efficiency; a reasonable estimate is 80%. So the primary current is 11.93/(0.8)(24), or 621 mA. Since each half of the primary conducts for only half a cycle, the primary can be wound with 25 AWG (424 circular mils) wire which is rated at 320.4 mA.

Besides primary current, WA_C depends on: the input voltage which is known; the core saturation level and operating frequency, which the manufacturer gives (14,000 gauss and 3,000 hertz for the cores in the table); and the fraction of window area taken up by the primary. This last parameter must be estimated. Its value is related to the window area that will be taken up by all the windings together, which determines how easy the transformer will be to wind. In most instances, the windings will not occupy too much window area if the primary fraction is put at 0.2. If so,

$$WA_C = (24\times424)/(2\times14{,}000\times3{,}000\times0.2\times10^{-8})$$
$$= 0.0606\times10^{6}$$

Therefore a core with a minimum cross-sectional area of 0.076 square centimeters is suitable. One with an A_C of 0.151 cm^2 will be used, however, to provide extra room for the windings.

With this value of A_C, the number of turns in the primary can be calculated

$$N_P = 24/(2 \times 14{,}000 \times 0.151 \times 3{,}000 \times 10^{-8})$$
$$= 190$$

The transistors may be of almost any general-purpose type. Suppose the ones used have a base-emitter saturation voltage of 1 v and a base-emitter breakdown voltage of 5 v. To preclude exceeding the breakdown level, the voltage induced in the feedback winding ought to be less than (5v + 1v). Suppose that 5v is selected. Then the number of turns in the feedback winding is

$$N_F = (5 \times 190)/(2 \times 24)$$
$$= 20$$

The resistance values are found indirectly by setting a value on $R_2/(R_1 + R_2)$, calculating what the parallel combination of R_1 and R_2—called R_P—should equal, and then solving for R_1 and R_2.

First of all, to ensure proper starting of the converter, the voltage across R_2 when the divider isn't loaded should be between 3v and 6v. If it's picked to be 4v, $R_2/(R_1 + R_2)$ is 4/24, or 1/6.

R_P depends on this value, and on the desired primary current, which should at least equal the primary current divided by the forward current transfer ratio of the transistors. If this ratio is 15, the base current should be at least 0.621/15, or 414 mA, and R_P should be at most

$$R_P = (24/6 + 1.5)/0.0414$$
$$= 133 \text{ ohms}$$

Therefore R_1 should be at least 133/(1/6), or 797 ohms, and R_2 at least 133/(5/6) ohms.

For the three load circuits, the number of turns in each winding is

$$N_1 = 190(22 + 2)/(2 \times 25)$$
$$= 95$$
$$N_2 = 190(5 + 1)/24$$
$$= 48$$

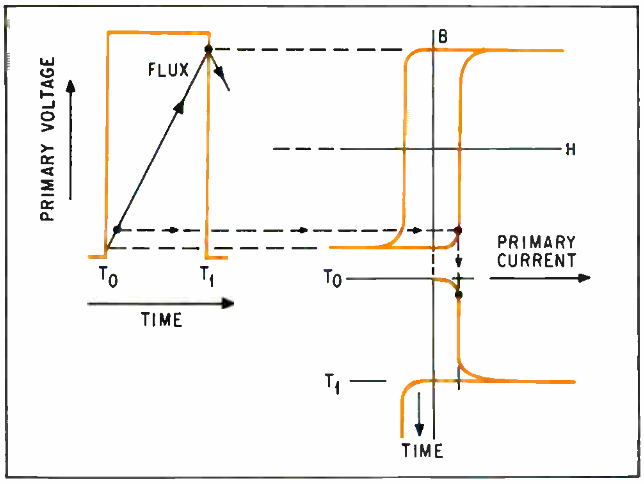
and

$$N_3 = (190)(10)/(4 \times 24)$$
$$= 20$$

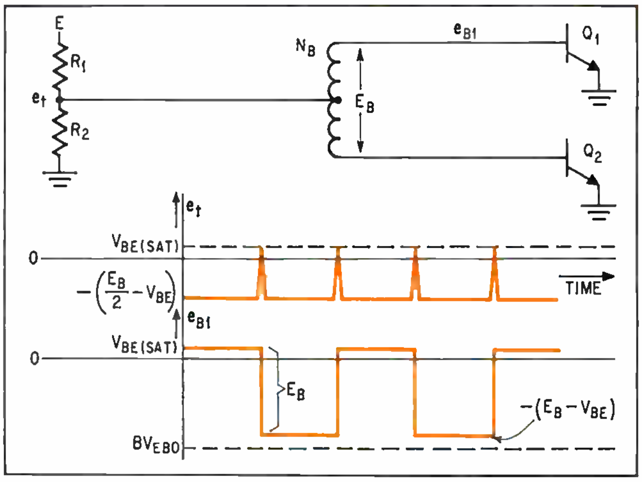
To verify that the selected core really does have a large enough window, the fraction of it taken up by all the windings is calculated. First, for each winding the number of turns is multiplied by the wire's cross-sectional area, and then all the products are summed. The point at which winding gets difficult is around 40%, but in this example it turns out that the windings take up less than 32% of the window.

TAPE WOUND CORES

			Manufacturer's Designation				Core Dimensions (inches)		
WA_c	W (cmil)10^6	A_c cm^2	Arnold Engineering Co.	G-L Industries, Inc.	Magnetics, Inc.	Magnetic Metals Co.	I.D.	O.D.	Height
0.026	0.348	0.076	5515	1030	50002	5	0.650	0.90	0.125
0.053	0.308	0.171	5958	1018	50076	37	0.625	1.0	0.188
0.066	0.865	0.076	4168	1060	50011	9	1.0	1.25	0.125
0.070	0.462	0.151	5502	1040	50061	79	0.75	1.0	0.250
0.070	0.308	0.227	5651	1020	50007	3	0.625	1.0	0.250
0.079	0.462	0.171	5504	1050	50106	7	0.75	1.125	0.188
0.415	1.369	0.303	5387	1120	50030	13	1.25	1.75	0.250
0.523	0.865	0.605	6847	1110	50038	62	1.0	1.5	0.500
2.37	1.96	1.21	5320	1140	50001	15	1.5	2.5	0.500
4.37	3.61	1.21	6110	1170	50103	76	2.0	3.0	0.500
13.0	5.35	2.42	5468	1190	50042	20	2.5	3.5	1.0
88.0	14.54	6.05	5611	1220	50112	25	4.0	5.25	2.0
140.6	14.53	9.68	9260	1222	50426	78	4.0	6.0	2.0



2. Primary action. Core hysteresis accounts for primary current behavior. Because the primary voltage is constant, the core flux increases linearly until the core saturates. During this time the current is constant. When the core saturates, primary impedance drops, producing a current surge. At the same time the polarity of the input voltage reverses, restarting the cycle in the opposite direction.



3. At the base. The voltage waveform observed at the base of both transistors is square and clamped in the positive direction at their base-emitter saturation voltage. Except when the transistors are switching, the voltage at the feedback winding's center tap is constant. When the core saturates, however, an inductive transient induces a voltage spike which switches the transistors.

The transistors can be of almost any general type. But there are a few parameters that must be considered. The collector-emitter breakdown voltage should be greater than 2E since this voltage level always exists across the nonconducting transistor. The rated collector current must be greater than the primary current, and the switching speed must be high enough to insure efficient operation at the converter's operating frequency.

The final design step is to calculate the number of turns needed for each load winding. (The total number of loads that can be tied to a dc-to-dc converter is limited partly by the economics of coil winding, and partly by the decline in converter efficiency that results when there are too many load windings; for the more there are, the further some of them are from the primary, and as a result these have a high leakage inductance.) Calculation of the number of turns for the secondary windings requires taking into account the voltage drop across the rectifiers—the drops across the load windings are usually small enough to ignore. For example, in the typical converter in Fig. 1, which supplies two dc voltages and one ac voltage, the number of turns for the bridge-rectifier circuit is given by

$$N_1 = N_P(E_1 + E_{L1})/2E$$

where E_{L1} is the combined voltage drop of two rectifier diodes. For the center-tap circuit, the equation is

$$N_2 = N_P(E_2 + E_{L2})/E,$$

where E_{L2} is the drop across one diode. For the ac load, the number of turns, N_3, is

$$N_3 = N_P E_3/4E$$

where E_3 is a peak-to-peak value.

All the values needed to build the converter are now known, and the finished device should perform to within a few percentage points of them. How close the actual voltages come to the calculated values depends mostly upon the turns ratios and semiconductor specifications, while core characteristics influence efficiency and the operating frequency.

Core parameters are rather stable over a wide temperature range. For a rise of O°C to 50°C, the core saturation level changes by about 5%, but affects only the operating frequency. The squareness ratio, which describes the departure of the hysteresis loop from the ideal rectangle, will drop by less than 1% over the same range. However, the resistance of copper wire will increase by about 20% for a 50°C rise, and this usually significantly decreases the currents in the primary and in other windings carrying a current whose density is near to the maximum rated density of the winding wire.

When it comes to actually winding the transformer, it's necessary to minimize leakage inductance, for good efficiency, and transient distortion, for protection of the transistors. The most important requirement is to maximize the coupling between the feedback winding and the primary. The primary should be placed on the core first, wound with a minimum number of layers, and evenly distributed over the entire surface of the toroid. A useful criterion for core selection is to obtain one with a diameter large enough to allow the primary to be applied in one layer.

The feedback winding is wound next, again evenly distributed. The load windings also should have an even distribution, but it's not nearly as important for them as it is for the primary and feedback windings. □

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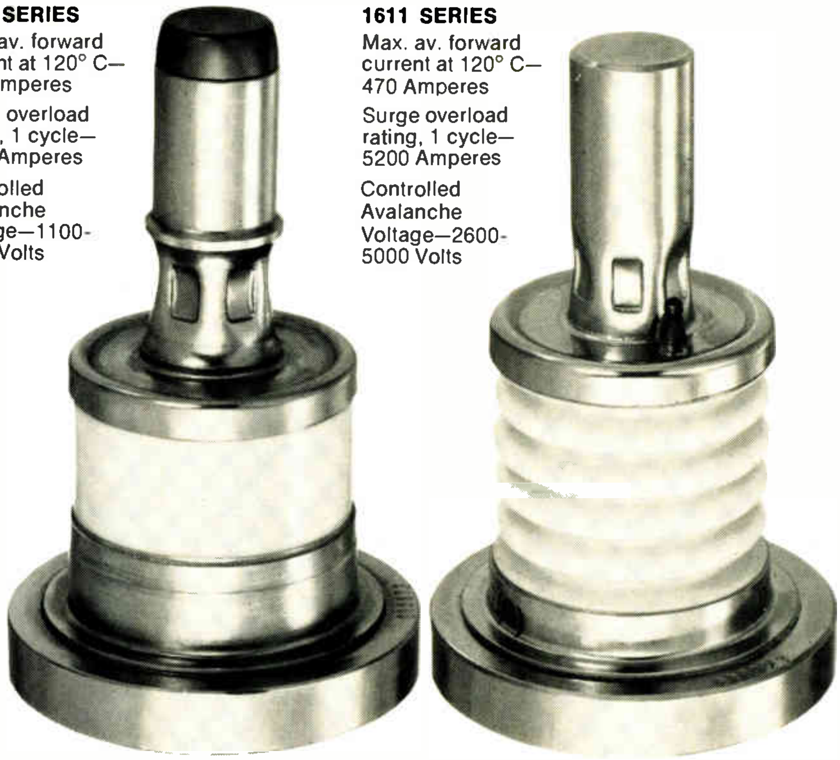

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• Accessory coax devices and probes to monitor the unknown's responses to the swept test signal.

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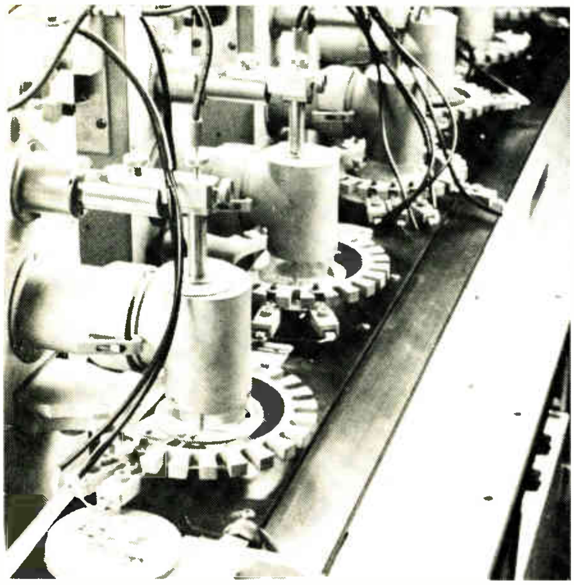

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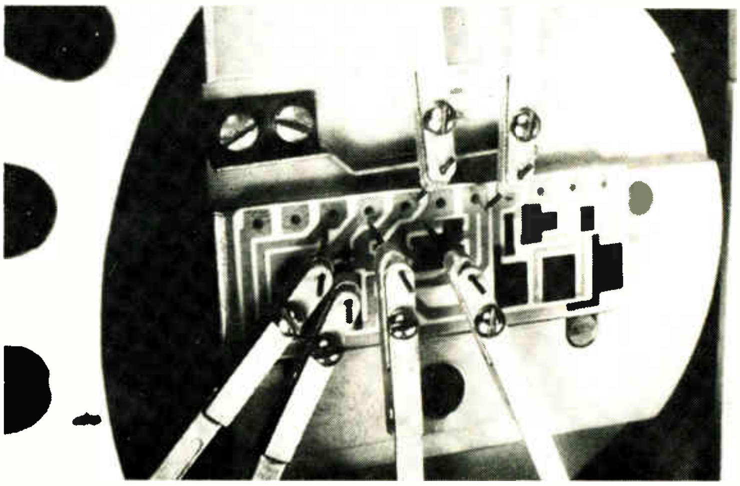
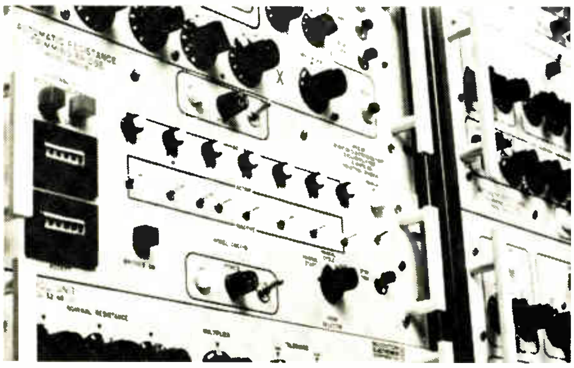
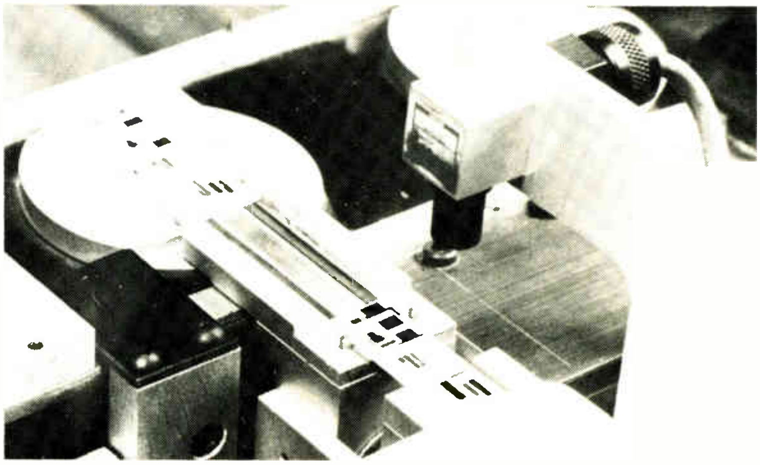


After the trim, probes flash data to memory bank for referral to accept/reject station.



Trim parameters are dialed on separate console. Memory bank and bridges control and monitor the entire cycle.



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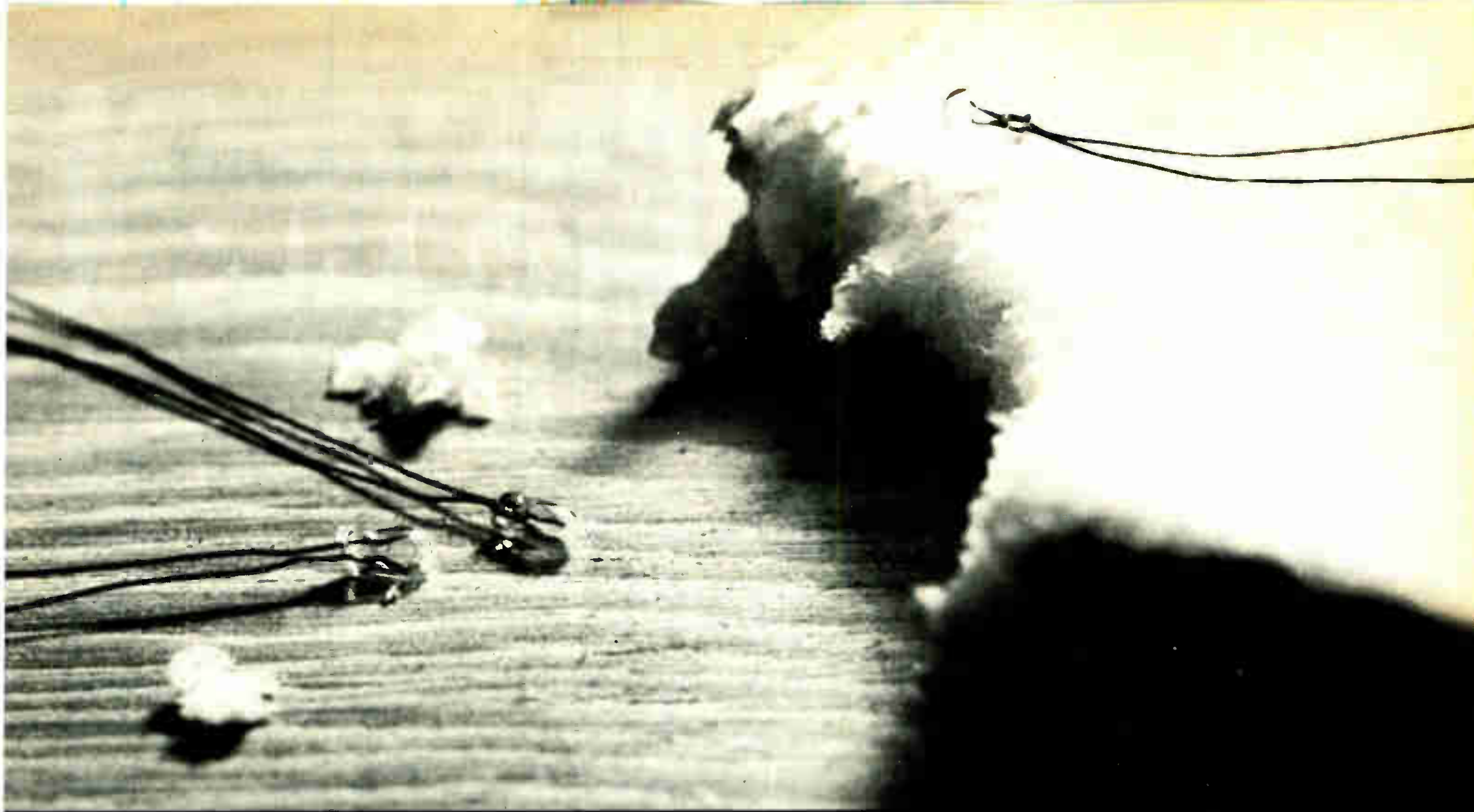

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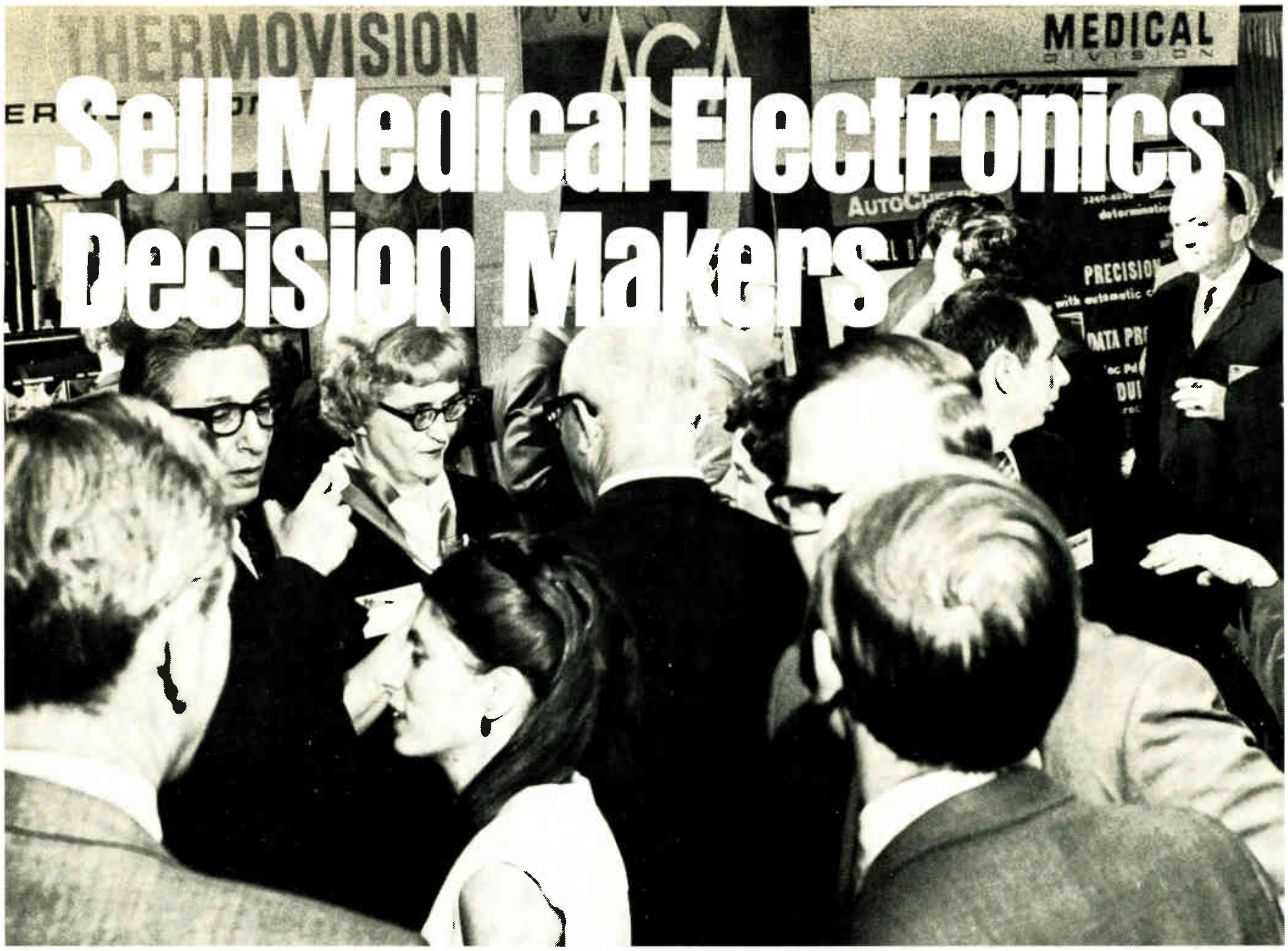

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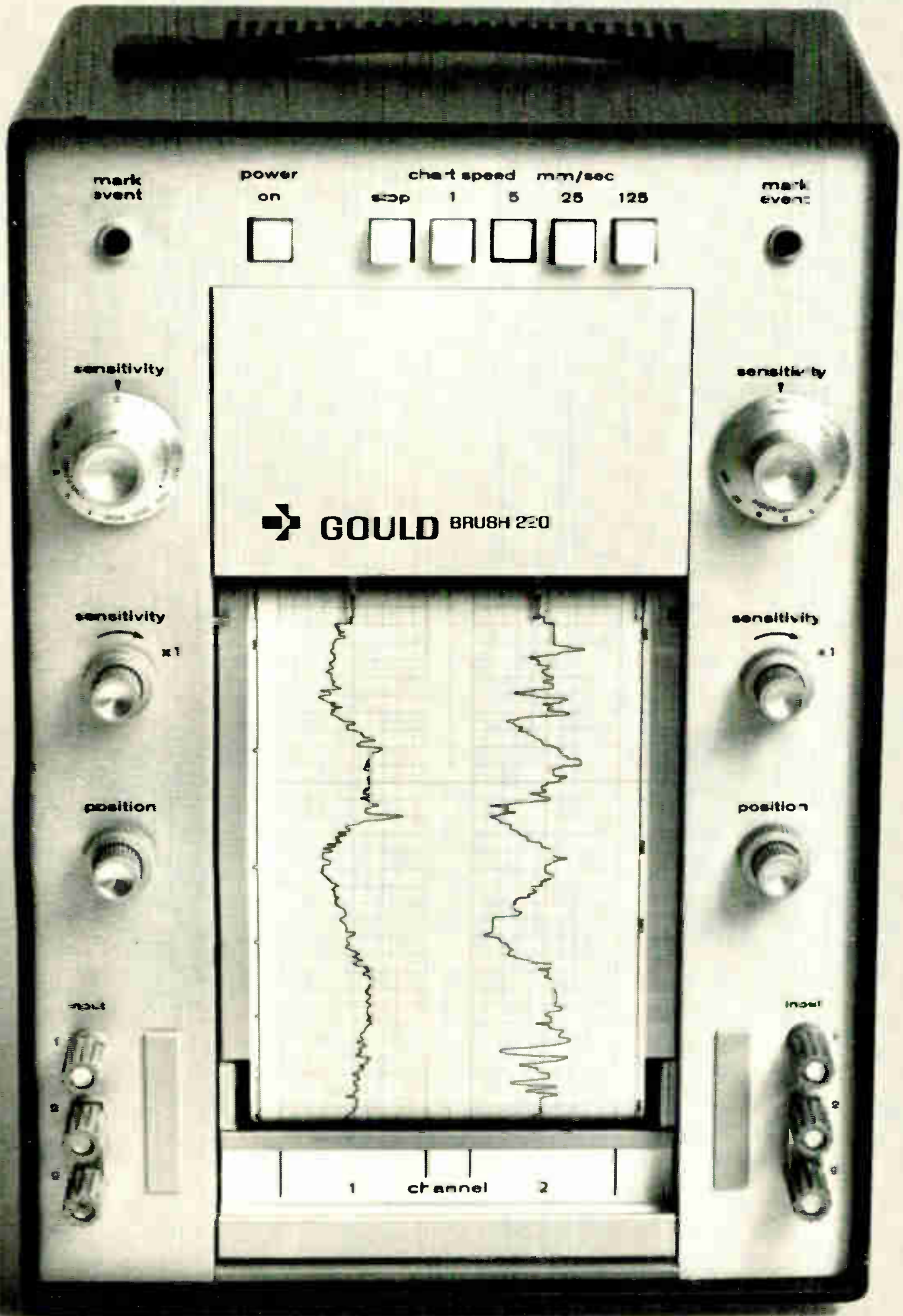

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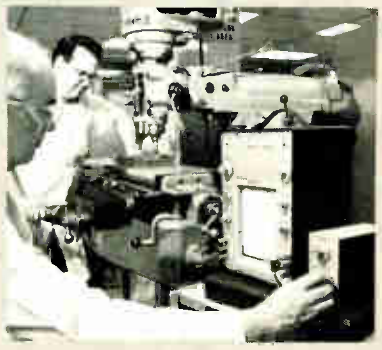

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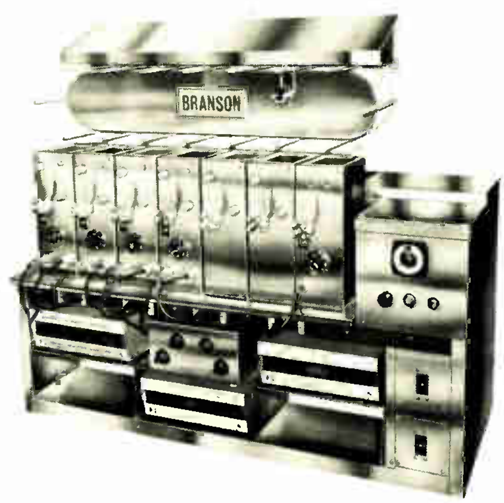

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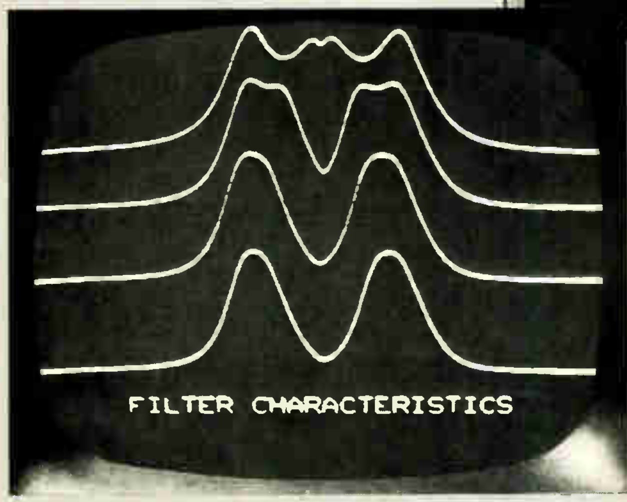

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How Packard prevails at the Pentagon

In his first 20 months, the former Hewlett-Packard chief decentralizes authority, buys technology from abroad, and cuts military overhead

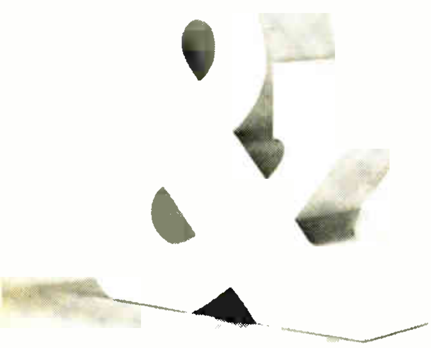
By Ray Connolly, *Washington bureau manager*

Deputy Defense Secretary David Packard's apparently successful management of the Pentagon's bureaucratic Goliath is becoming as legendary in Washington as the feat of an earlier David who, the Old Testament says, "prevailed over the Philistine with a sling and a stone." Yet Packard, whose six-foot, five-inch frame makes him something of a Goliath himself, surprised an industry audience on the West Coast not long ago by confessing some "shame" at not having done more to resolve the "real mess" in military procurement [*Electronics,* Aug. 31, p. 51].

After 20 months in office, he is not altogether satisfied with either his own or industry's performance in providing the military with economical, reliable systems. Says one executive who was at the meeting and who used to know Packard at Hewlett-Packard Co., "I guess I was more surprised at the 'shame' part of the speech than his cracks about industry's performance. Dave has no qualms about knocking heads if the need arises, but I never heard him suggest that he was up against a job he had trouble handling." That observation, however, ignores the fact that Packard, generally acknowledged to be the most powerful deputy defense secretary ever, has come to grips with a staggering management job that has broken some powerful men. When former Defense Secretary Robert S. McNamara, with whom Parkard is sometimes compared, left DOD after seven years, he was by all accounts emotionally and physically drained.

If McNamara failed, why should Packard succeed? "Simple," responds one of Packard's old associates, "Dave has dealt with technological innovation all his life, and that's a tremendous skill. McNamara's experience was all in large-scale production at Detroit," where innovation doesn't have a high priority. Supporters also note that Packard's brand of decentralized management runs counter to the McNamara approach, which tripled the size of the Office of Secretary of Defense and more than tripled its paperwork. "McNamara was an autocrat," says one Packard fan. "Dave is anything but that."

In fact, Packard even gives a visitor an impression of shyness. He speaks softly, plucking frequently at his left eyebrow as he formulates answers. Yet despite



his colleagues' agreement that "he's terrible on a speaker's platform" and prefers notes to prepared texts when speaking on key public issues, no one doubts that he has come up with hard answers to some of the tougher questions being posed by defense industry contractors and critics.

For instance, at a time when new defense procurements are declining, the Pentagon is expanding its horizons, buying some of its electronics in European markets to the dismay of U.S. competitors. Packard's response is that America "has partners in Europe" and needs "all the advantages and ingenuity we can get" for successful systems development. But when the Army made known its plans earlier this year to buy a number of $500,000 field artillery radars developed jointly in the mid-1960s by France and West Germany, a senior Pentagon official attributed the purchase more bluntly to "Dave Packard's fetish for things that work." [*Electronics,* July 6, p. 60]. Others suggest the purchases are political, part of a grander strategy to compensate for Europe's balance of payments loss when President Nixon decides to make major defense cuts by pulling back most U.S. troops from Europe.

However, the reasons the deputy secretary of defense cites are economic. "Research is generally less expensive than in the U.S.," he says, pointing to the fact that "a good many European firms are slimmer and trimmer than some in the U.S." and enjoy lower labor rates.

In Packard's thinking, if the U.S. "can find something already developed" overseas, there is no reason to repeat the development cycle. This philosophy seems evident in the U.S. Marine Corps' decision to invest in Britain's Hawker-Siddeley Harrier vertical takeoff and landing (VTOL) fighter (though most of the Harrier's avionics will come from American inventory). And while overseas purchases of several million dollars' worth of aircraft and radars don't necessarily indicate a major switch in procurement policy, they do suggest that the United States, as Packard puts it, "is working very hard to find more ways to buy more defense for its dollar."

Another way he hopes to economize is to shake out weapons problems early in development. His program to give military system managers more responsibility, hold them to performance milestones in each step of the effort, and keep them on the job until it is done, has been widely publicized. Less well known are his beliefs that there can be greater commonality of equipment within the services; that there have been occasions when too much emphasis has been placed on formal mil specs when "high-quality commercial equipment" could have done as well; that military operating commands are top-heavy with personnel; and that the Directorate of Defense Research and Engineering (DDRE) has been spending "too much time on hardware and not enough on R&D."

The ultimate in commonality was sought by McNamara when he pressed an Air Force plane, the F-111, on the Navy. Packard, however, stops at subsystems. "Packard is an engineer and a good one," says a subordinate, "and he knows how far he can go. That's the difference between engineers and economists. McNamara almost killed the commonality concept with the F-111 because he went too far, too fast. Besides, there were too many unknowns to be resolved with the plane when it was committed to production. Nevertheless, there is still plenty of room for common equipments in the military." Packard's most

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recent move in that direction was to kill the Air Force AIM-82 Dogfight missile for the F-15, replacing it with an upgraded version of the Raytheon-built Sidewinder, to be called Super Sidewinder [*Electronics*, Sept. 14, p. 56]. It was a case, he says with finality and a smile, "where I decided there were too many missiles."

On manpower, Packard is on record against the recommendation of the Blue Ribbon Defense Panel headed by insurance executive Gilbert Fitzhugh that DOD move to have three Deputy Secretaries of Defense. Packard's against this because it would centralize authority at the top, rather than place more responsibility at lower levels. But he notes, "I'm in agreement with most of the things they want us to do," and he plans to implement the recommendations on a step-by-step basis. For example, Packard views some operating military command structures as topheavy with people. "I've just been looking at this," he says with a wave at the papers on his desk. "There are too many people in the overhead of these commands." Thus he believes "significant reductions in personnel" can be made without damaging military capability. Industry contractors, who tend to build their staffs on a man-for-man basis to match their customers, are likely to find pending cutbacks will permit reductions in their own manpower heads as well.

In DDRE, David Packard wants to see more emphasis on research and development, and less on building hardware. The engineering function suggests "another organization," he says, agreeing with the Blue Ribbon Defense Panel recommendation. Such an organization might have the responsibility for "more operational tests of weapons."

Packard's own approach to new technology has not changed much since the days when he ran the nation's biggest instrument house. According to one who has known him in both his government and his industry roles, "Dave tends to the cautious side. He'll spend all the money that's needed to research something as long as the signs are hopeful, but he has no regrets about shutting a project off if he's convinced the return won't match the investment."

Hewlett-Packard succeeded by using technology with a track record, and Packard is applying the same principle to defense systems. "H-P wasn't the first to go with transistors in its instruments," recalls one industry executive, "but when it did, the thing worked. That's about the nicest thing you can say about a competitor."

Such stories about the deputy defense secretary's industrial record explain much about the way he runs DOD from the inside, while Secretary Melvin Laird works outside with the White House, formulating policy and running a war in Southeast Asia. As one military program manager put it, "Being first in the field with a new piece of gear is something every commander wants—provided it does the job. And doing the job is the first requirement for everything we buy now."

The potency of the Laird-Packard team is underscored by Louis De Rosa, the recently named Assistant to the Secretary for Telecommunications, who says, "It's the unusual combination of having proficiencies in the political and economic areas at the same time as you have proficiencies in the operations and technological areas. This is a very powerful combination, which I've never seen before."

About the future . . .

David Packard's remarkable candor is an uncommon trait in the Washington milieu. It comes through clearly in this exchange with *Electronics*.

Q. Mr. Secretary, on the basis of your experience within the government, briefly, what would you say you have learned about defense contracting that would be most useful to your former counterparts in industry?

A. Briefly, I would say that they must learn to get along with a lot less money.

Computers

Modules making waves in EDP market

LSI and bus advances allow interconnection of modules with near-limitless capabilities; competitive picture in industry could change radically

By James Brinton, *Boston bureau manager*

The traditional approach to computers as black boxes accessible only through software may be undergoing significant evolutionary change. Particularly in the minicomputer field, more and more machines are being sold as architectural building blocks. This allows users to buy only what they need or can afford and enables them to control the capabilities of their machine through its hardware.

"In as little as two years users may not buy computers by model number any more but instead pick from a shopping list of modules and thus completely control the architecture of their machines," comments an industry spokesman.

This trend to a more fluid architecture is certain to change the nature of competition among vendors. It could blur the distinction between generations of computers and might even allow minicomputer makers to grab a share of the business now going to large mainframe houses.

Making the building block concept feasible is the advent of large scale integrated circuits, with which entire functional blocks can be put on one or two printed circuit boards. At the same time, computer makers have developed bus interconnection schemes that make it possible to combine these blocks into data processors of near-limitless power and complexity.

Started only about two years ago with self-contained modules, the trend toward large-scale modularity has firmed up in recently introduced minicomputers. First came the GRI-909 from GRI Computer Corp., Newton, Mass. [*Electronics*, July 7, 1969, p. 14]. Then the Digital Equipment Corp., Maynard, Mass., introduced its PDP-11 [*Electronics*, Jan. 5, p. 161] and PDP-8/E [*Electronics*, July 6, p. 105]. The most recent entry was Modular Computer Systems Inc., Ft. Lauderdale, Fla., with its Modcomp I and II, 8- and 16-bit computers.

Large-scale modularity is also spurring interest in universities and in the defense industry. At Washington University in St. Louis, a team of scientists has been working since the mid-1960s on modular processing applications for the scientific and medical communities. Wesley A. Clark, director of WU's computer systems laboratory envisions libraries of architectural blocks at campuses and research centers around the country. A scientist who needs a special purpose processor perhaps only once could "check out" the blocks he needs, assemble them into the desired processor, do his task, and return them. Clark hopes this "macro-

The macromodular approach

Because he feels "research often is limited by available tools," and "goals can be hardware limited," Wesley A. Clark, director of the Computer Systems Laboratory, Washington University, St. Louis, Mo., began developing the "macromodular" computer approach in the mid-1960's. He and his co-workers feel macromodules checked out like library books and plugged together would do specialized processing jobs easily, and offer vast growth possibilities.

The first library will be ready sometime late this year or early next at WU and will consist of 300 to 350 "cells", one or more of which make up a macromodule. Cells are adders, registers, memories and comparators. By combining these to make macromodules, Clark's group feels it has avoided as much logic redundancy and cost as possible.

This first experimental library is a result of several hundred man-years of effort and about $6 million of funding from the Advanced Research Projects Agency and the National Institutes of Health. WU is funded two years ahead in its work, which many researchers feel is as important as, and is a complement to, the Advanced Research Projects Agency network.

Using emitter-coupled logic (Motorola's MECL-2) and asynchronous data paths, the modules are designed to make plugging together a performance-degrading or physically-harmful configuration impossible. Electrically, each macromodule is almost self-sufficient and can operate with a near-infinite number of other modules except for speed and size; macromodular system behavior is determined only by the logical structure of the whole.

At present rates, the cost of macromodular processors would run about $500 per cell, estimates Clark. Thus a 24-bit general-purpose, stored-program computer using about 35 cells would cost about $18,000—low by commercial standards. And they're fast: a proposed fast-Fourier processor would be 10 times faster than an IBM 360/50 or 7094 at 1/10th the costs.

modular" approach will make specialized computer power available to more researchers and at a low cost, since an entire research center would share the bill. The government agrees; WU's work has been funded by both the Advanced Research Projects Agency and the National Institutes of Health.

Defense contractors also are working on modular processors for both air and ground applications. Perhaps the most significant work in this area is being done by the Naval Air Systems Command, whose goal is a modular advanced airborne digital computer capability by 1975 [*Electronics,* Aug. 3, p. 89]. With 20 to 30 standard modules, the Navy estimates parts and spares cost could be reduced enough to save 90%-95% of the cost of a hardwired computer for similar applications.

This across-the-board interest in modular computers is easy to understand. The user need buy only enough logic for his job; if need be, he can buy and add more without having to debug a whole new mainframe. Nor is he locked into a given computer generation; new technology would appear as modules that offer improved performance.

The computer maker's engineering can be divided into smaller chunks, to be amortized separately. And by building only the most-used modules, he can keep volume high and end product cost low.

Since a modular computer breaks into relatively inexpensive architectural blocks, each with its own engineering cost, introduction of a competing processor with better performance would only require designing upgraded modules to meet it. This would mean longer average product lifetimes, say industry spokesmen. "Let's suppose a competitor with a black-box computer philosophy comes up with a faster machine," says Roger C. Cady, manager of small computer engineering at DEC. "Instead of redesigning a whole mainframe we just add new arithmetic and/or memory modules to our line for those who need them," he notes. Meanwhile, the basic engineering and standardized interconnection structure in DEC's PDP-11 and PDP-8/E don't change; only the modules' added cost must be amortized.

Basic to such architectural freedom is a unified bus structure concept that first appeared in GRI's machines. GRI vice president Saul

Modules for the military

By far the most ambitious effort under-way on military modular computers is the Naval Air Systems Command's Advanced Airborne Digital Computer program. Modular computers would be fashioned out of sequential and parallel processors, mass memory, and random-access memory modules, all making use of super-scale integrated circuits. AADC building blocks also would feature byte modularity, permitting, for example, eight-bit registers to be wired together in groups of eight to form a 64-bit register.

Another program is being launched under the aegis of the Air Force Avionics Laboratory. Burroughs Corp. has a $469,000 contract to develop three modules—a switching matrix, a processor module, and a memory module—that could be assembled into computers for all types of aircraft.

Meanwhile, computer companies are developing military modular systems on their own. Last fall, Control Data Corp. introduced its Alpha series, a set of processing, nondestructive readout, and destructive readout memory modules that can be assembled to form simplex and duplex processors. CDC has already interested the Royal Canadian Air Force.

Another manufacturer, Hughes Aircraft, is betting that military interest in modular computers will extend to ground-based systems. Hughes plans to bid its H-4400 series, which uses as many as eight processors and 16 memory modules to form four million-operation-per-second machines, as part of command and control systems for this decade.

—Jim Hardcastle

Dinman says the unified bus originally was designed to ease input-output interfacing problems in process control and similar applications. But the bus and modularity concepts have allowed GRI to both expand and shrink its original $3,600 machine to fit varying market niches and buyer budgets. Thus the four modular 909 models are suited to markets ranging from industrial control work to middle-sized computer applications.

The parts list for Modular Computer Systems' Modcomp I reads like half the list for its Modcomp II—indeed the II is largely two Is in parallel. These are forerunners of a family of 12 or 13 machines designed for applications from dedicated industrial control to very high-powered multiprogramed multiprocessing. All are built around a common two-line bus, except for the upcoming III series which will use two such buses in parallel with shared memory bridging the gap to form a 16-bit basic dual processor.

With minicomputer makers almost ready to start taking orders for parallel processors, the next step is to extend the common-bus-and-module approach for larger multiprocessors.

DEC is preparing at least two new products that will allow PDP-11s to be linked into complex nets using shared memory and peripherals. And other firms aren't far behind.

Still in development, DEC's devices are called simply "the switch" and "the interconnection." The switch, by acting as a small communications processor, will allow data transfer from one PDP-11 bus to another. The interconnection would allow communication, plus time-shared access, to any of the devices in other systems or on peripheral busses, except for reserved cores.

Using interconnected sets of PDP-11 modules, says a DEC consultant, a 16-bit processor network could outperform a Control Data Corp. 6600 when operated in a task-sharing format. In fact, one DEC customer already has an application for eight or nine PDP-11s linked in just that way to perform fast Fourier computations.

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Computers

IBM goes all out for IC memory

By bringing out the 370/145 with a semiconductor main memory, the giant of the computer industry may alter the storage game

By Peter Schuyten, *New York bureau manager*

To many in the semiconductor memory business, IBM's announcement late in September of its first computer with an all-semiconductor main memory sounded like the trumpets of the second coming.

George Cogar, for one, president of Cogar Corp., an aspiring semiconductor memory maker, happily predicts that IBM's innovation in computers is every bit as significant as the introduction of jet engines was to commercial travel.

Lee Boysel, president of Four Phase Systems Inc., who recently announced his own computer with a mainframe semiconductor memory [*Electronics*, Sept. 14, p. 52], says, "We've been saying for a long time that solid state memories are the way to go. Now IBM is backing us up."

But perhaps Robert Graham, vice president of marketing, Intel Corp., another semiconductor memory company, sums it up best when he says: "IBM has shown that cores aren't necessary, and when IBM says it, people listen."

But even if IBM's new computer, the 370 Model 145, does not herald a rush of other semiconductor memory machines, its technological importance cannot be doubted. As one IBM official put it: "Historically, computers have always been memory-limited because the processor has for years been capable of outrunning the memory. All kinds of tricks have been used to help the memory keep up, the most important of which is perhaps the cache. Now, with compatible memory and processor technology, the computer is no longer memory-limited—and we have a whole new ball game."

IBM's announcement could have been meant to steal some of the thunder from RCA, which went on record early in September [*Electronics*, Sept. 28, p. 47] as taking dead aim at IBM's market with its new line of computers. RCA, however, is still using core technology in its main memory systems. Some industry observers go so far as to speculate that IBM has had a semiconductor memory ready for some time, and, on discovering RCA's plans early this summer, rushed it into production readiness for whatever psychological and marketing advantage could be gained from it. IBM, however, denies it—despite the fact that the 145's average cycle time of around half a microsecond is still within the range of cores.

Most surprising to some industry observers, however, was that IBM's latest entry in its 370 series uses a memory based on bipolar monolithic technology and not MOS. But logically enough, while the 145's circuits themselves are new, the technology behind them has evolved directly from that used for the cache memories in IBM's System 360 Models 85 and 195 and its first two 370's, the 155 and the 165. (One key difference between new and old, however, is that the chips in the 145 contain 128 bits, and IBM's largest previous bi-

Also starring

A semiconductor main memory isn't the only new wrinkle in IBM's 370/145 computer. Another feature is reloadable control storage (RCS), which replaces the read-only memory of other 370 models and most 360s. Data stored in the RCS can be loaded from a prewritten disk cartridge supplied by IBM—indicating, however, that there is no apparent way the operator can make his own cartridge.

IBM also is offering an optional disk storage unit, the 2319, with the 145. The 2319 attaches directly to the central processor; a separate control unit isn't required. Though a money-saver, this direct connection to the processor is relatively inflexible in its applications, and it takes up two of the four high-speed input/output channels that could be used with other peripherals. To the independent peripheral maker the hard-wired approach means no plug-to-plug compatibility, which is often their life blood. Not that the 2319 in itself represents much of a threat to the peripheral maker: it would only if it signifies a trend for other IBM equipment.

Finally, the 145 offers the user a unique approach to solving a problem normally associated with a computer's error correction scheme. Ordinarily, data is checked against a correction code as it passes through the logic circuitry, incurring a time penalty while the data goes through the required extra layer of logic. But the 145's semiconductor memory is faster than the processor's logic, so error correction can use this extra speed without any performance penalty.

Monthly rental for the 145 ranges from $14,950 to $37,330, depending on memory size. First shipments of the machines are expected to begin in the third quarter of 1971.

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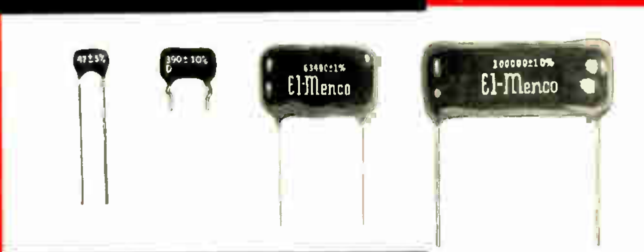

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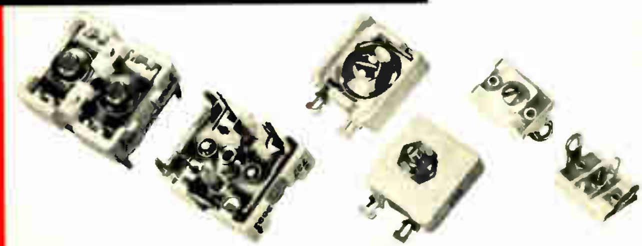

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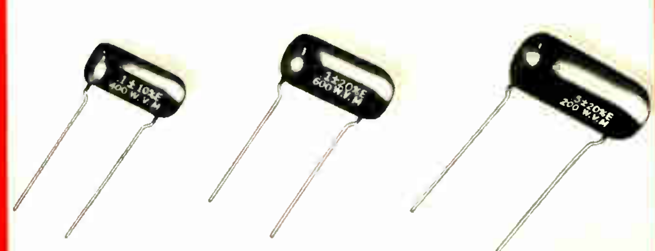

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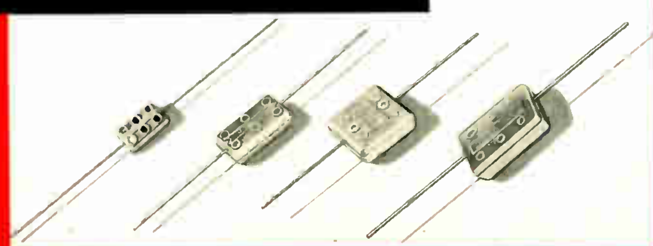

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But the decision to go the bipolar route should not have come as a shock. According to IBM officials, at this point in time bipolar is "the most cost effective approach." So far, no one seems willing to argue. William R. Arnold, president of Semiconductor Electronic Memories Inc., says, "We've always believed MOS mainframes were several years down the road—perhaps 1974 or 1975. They'll come simply when they become more cost effective; and frankly, some of the shrill claims for MOS have bordered on the irresponsible."

Each memory chip in the 145 measures 113 by 122 mils. To form the basic memory module, two chips are packaged on a half-inch-square ceramic substrate; two substrates are double-decked. Depending on the overall size of the main memory, the modules are packed either 16 or 24 to the card. There are 36 memory cards on a board. Up to six of these boards plus an additional one containing error correction circuits make up what IBM calls a memory unit. Thus one memory unit in its maximum configuration contains a total of 256,000 bytes (eight bits to the byte); and two such memory units make up the 145's maximum storage capacity of 512,000 bytes. Minimum memory size available is 112,000 bytes.

Access time at the card level is less than 90 nanoseconds, while cycle time is less than 150 ns, nearly four times slower than the 40-ns minimum cycle time for the cache memories featured in the 370/155 and 165. The 145's relative slowness is due in part to the denser packing of circuits on its chips. Usually higher density means faster speed, but it also means more heat. IBM slowed down the 145's memory circuits on purpose to help overcome cooling problems.

The main memory fetch cycle for eight bytes is 540 ns, while four-byte store cycle is 607.5 ns. These times include, respectively, two and three of the 150-ns cycles, plus a certain amount of "dead" or idling time.

Probing the news

Industrial electronics

Computer control grows in nation's oil fields

EDP gear runs 1 million barrels of daily output; suppliers see $20 million-a-year market growing

By Marvin Reid, *McGraw-Hill World News*

Forced to pinch expenses, profit-squeezed oil companies nevertheless are spending millions each year on computerized production-control systems for their oil and gas fields. Computers already control about one million barrels of daily production, and production efficiency has increased 3% on the average and up to 10% in some cases.

System makers estimate the annual market for their gear at about $20 million, and predict it will continue to grow since present computer-controlled production represents less than 20% of existing fields and wells.

One spur to the market will be the entrance of those oil companies that were put off by the poor performance of computer-controlled systems in the early sixties. "Some of the electronics companies that came into this thing early thought all they needed were hard-wired computers and telemetry systems made up of relays," recalls William G. Pearson, president of TRW Controls, an operating unit of TRW Inc., in Houston. "The first three systems that went in were fantastic losers."

Today's system includes solid state supervisory control, one or more minicomputers tailored to gather mass data and alarms from remote locations, special sensing devices, and software. TRW, along with Baker Automation Systems Inc., Houston, and Moore Associates, San Carlos, Calif., are the principal suppliers.

A basic system starts with a remote field terminal that picks up data from sensors installed in wellheads, lines and tanks. Telephone lines, microwave radio, or private lines then transmit the data to a computer interface unit at a master station where it is fed to a general purpose or process computer.

In most fields where maximum monthly production quotas are fixed by state regulatory agencies, these systems make it possible to hit the exact allocation. With manual monitoring of field operations, companies allow some leeway and often produce less than their quotas. In nonregulated fields, the systems have upped production either by reporting on incipient equipment breakdowns or by catching them as they happen.

One of the most ambitious conversions to computer control is being undertaken by Humble Oil & Refining Co., which is spending $50 million to automate 61 of its domestic fields. When Humble completes the conversion in 1973, it will have 80% of its domestic reserves under computerized production control.

Humble's pilot system at the Friendswood Field near Houston handles 192 wells, producing 25,000 barrels of oil daily. Sensors, such as pressure transducers, temperature probes, level switches, and flow sensing switches, are located at metering devices, where salt is removed from the oil, and at treating facilities, where the oil is processed. These devices are linked by telephone cable to remote field terminals, which in turn are linked to an IBM 1800 and a master unit. Information is projected on

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"Previously," says O.R. Harrison, project manager of the pilot installation, "problems frequently went unnoticed for hours until discovered on a periodic check by field personnel. Now they are spotted immediately."

Mobil has had a system for several years that monitors and controls wells in its Pegasus field, about 30 miles from Midland. The system is tied into a gas plant, and the computer, an IBM 1800, runs material balances and controls plant operations.

Continental Oil, which has systems in several fields, is planning to re-do its Ventura field in California, using TRW's telemetry system and an IBM 1800. The new system will include 38 to 49 remote terminal units and a microwave communication system.

Shell Oil Co. has systems in several fields, but has lagged behind the pace set by Humble, Mobil, and Continental. Texaco, too, has dragged its feet, but a systems firm reports the oil company is in the process of launching a program comparable in size and scope to Mobil's.

Atlantic Richfield Co. has installed its first computerized control system at its High Island, Texas, offshore field. On line for several months, the system collects data, monitors, and controls several production operations. It's expected to pay its own way this year.

But other major companies—Gulf Oil Corp. and Getty Oil Co., for instance—have been providing little business, say systems makers. One of the few non-major companies to make the move to computer control is Placid Oil Co. of Dallas, an independent producer.

Overseas, perhaps the biggest and most challenging computerized production-control system is being completed by Baker Automation in Libya's Amal Field. With a Data General Nova computer as the heart of its supervisory portion, the system will monitor some 118 producing wells and nine water injection wells, operating in ambient temperatures that reach 140° F.

Advanced technology

New perspective sought for displays

Experimental devices seek to add feel and depth to expand usefulness and accuracy; air traffic control and graphic editing could benefit

By Wallace B. Riley, *Computers editor*

Advanced as today's interactive display systems are, they still have a long way to go. Feeding back data via two-dimensional screens and sometimes through audio outputs, they haven't yet tapped the other senses and dimensions. But experimenters at two universities are working to create computer-controlled displays that could add new perspective to the comprehension of difficult problems.

One group, at the University of North Carolina, is working with a display that allows information to be felt, as well as seen. The other, at the University of Utah, is developing a three-dimensional headset display that puts the user literally in the picture. The depth and dynamic nature of the computer-generated image creates a sense of being able to walk around the image and even climb inside it.

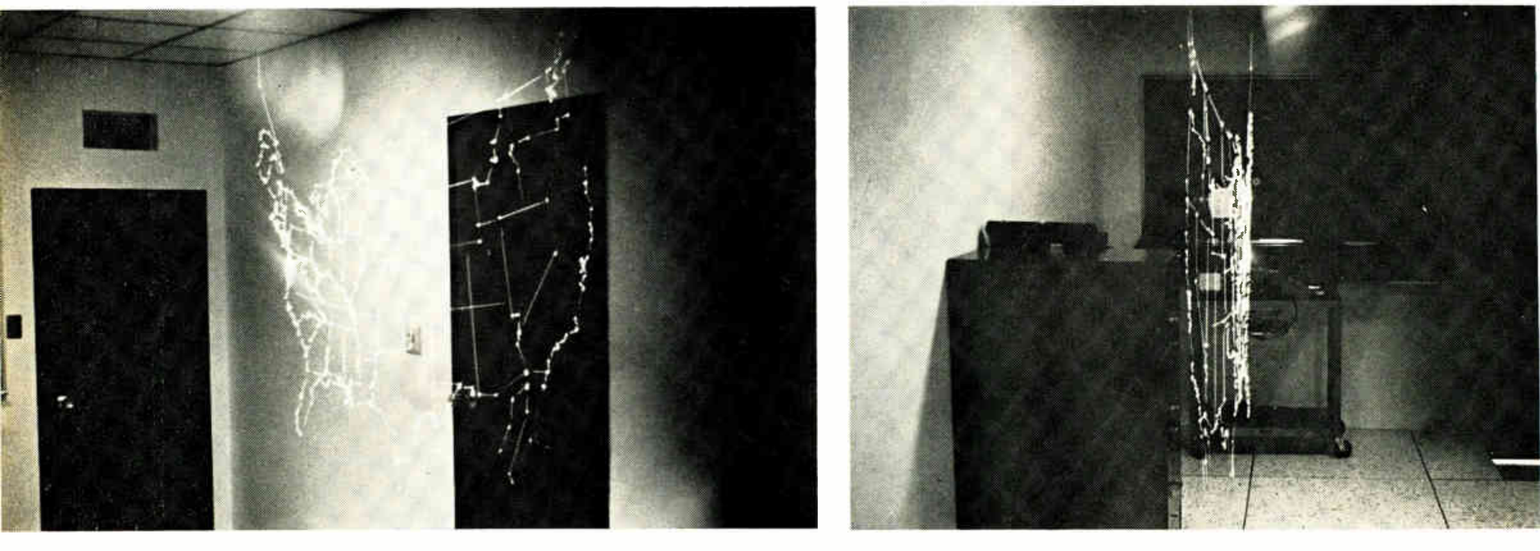
Neither group is even thinking of a commercial version yet. "But the headset display might help air traffic controllers get planes off collision courses," notes Donald L. Vickers, one of the Utah researchers. "It would put the controller right in a simulated airspace. He could walk around approaching planes, if necessary, to determine whether they were actually headed for a smashup."

The kinesthetic system could make editing of electronic texts with light pens easier—by helping the user to position a cursor over a word to be deleted, for example. Another use might be in positioning components in a circuit with a light pen. The joystick could be programed to push back if the operator tried to draw in a component with a drastically wrong value.

The North Carolina work, known as "Project Grope," is under the direction of Prof. Frederick P. Brooks Jr. So far graduate students have built a two-dimensional kinesthetic display and are now working on a "seven-dimensional" unit. In the two-dimensional unit, a joystick control moves the cursor—a position-indicating spot or cross—either up and down or left and right on a screen, just as in conventional graphic displays. But in the Grope setup, the joystick pushes back or pulls away if the cursor movement represents repulsion or attraction between two objects.

For example, the system can be programed so that the screen displays a field between two or more electrodes, and the cursor represents a charged particle. Then if the operator moves the particle against the field in the wrong direction, the joystick pushes back. Or, if the particle moves toward one of

Room with a view. Head-mounted display at the University of Utah projects three-dimensional images that are viewed through goggles. As the wearer moves, the image adjusts accordingly so that it's possible to "walk around" objects.



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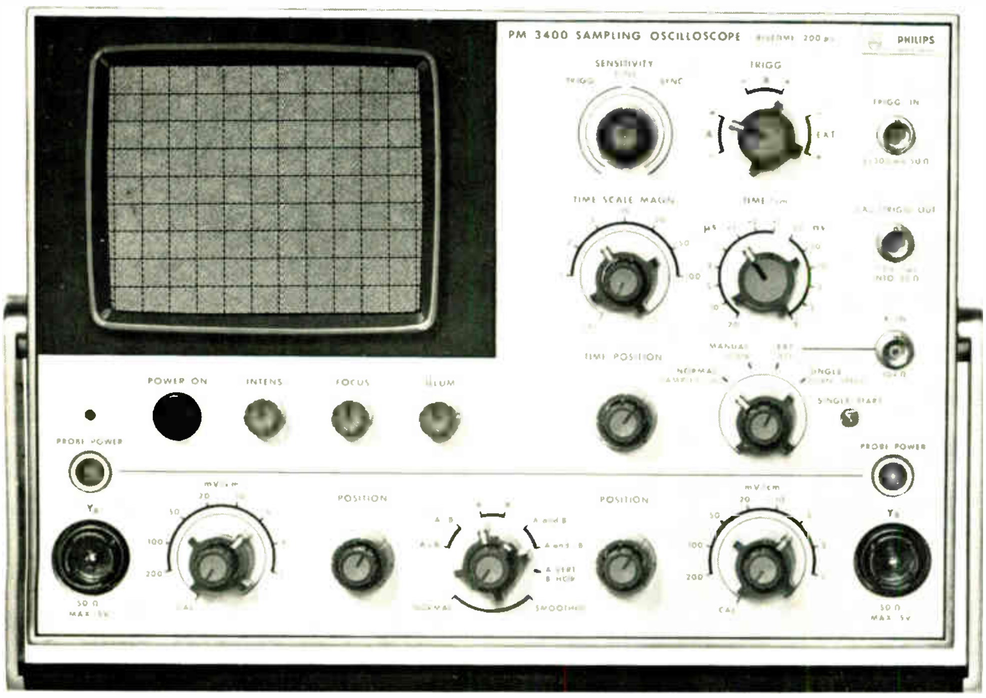

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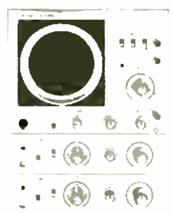

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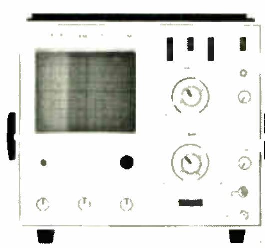

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the electrodes, the operator has to tug at the control to hold the particle back.

Each of the two coordinate axes has a servomotor and a potentiometer that link the mechanical motion to the display control and the computer. As with conventional joysticks, a movement in any direction changes the setting of one or both potentiometers. This generates an analog signal that is converted to digital form and transmitted to the display control, where it will be translated into a cursor movement. The linkage between the hand control and potentiometers includes the output shafts of the servomotors. An IBM 1827 data control unit converts the analog outputs to digital form, feeding them to a 360/40 computer, which Project Grope shares with other users. Current amplifiers have been added to the 1827 for driving the servomotors. The CRT display unit connects directly to the 360/40.

The display system can locate a point on the screen to an accuracy of one part in about 300. The servomotors that push back on the handle generate nine inch-ounces of torque, geared to about half an ounce of linear force.

The right touch. North Carolina display can be felt as well as seen. For instance, if the operator moves particle in the wrong direction, the joystick pushes back.

Thomas B. Sheridan, professor of mechanical engineering at MIT, developed the two-dimensional input unit used in the system to help study communication with the blind. North Carolina borrowed the system for its research project, and James J. Batter, a graduate student, is using it as an aid in undergraduate instruction.

The seven-dimensional input device is being built from a pair of radioactive material manipulators borrowed from the Atomic Energy Commission. The display—an ordinary two-dimensional tube—is driven by a computer to show the operator an apparent three-dimensional picture through perspective and orthogonal projection. The manipulator, tied into the computer, can be used to operate the display, moving an object linearly around all three coordinate axes and rotating it around the axes. The seventh "dimension" is a grasping force that "isn't essential to any of the experiments we have in mind," says Brooks. "Since the way to make it operate is the same as for the other movements, we plan to hook it up, but we don't know at this point just what we'll do with it."

Brooks' group plans to control the system through a small Interdata computer, which may be linked to the 360/40 or to a larger machine. The Interdata processor will replace the IBM 1827. And the university eventually hopes to replace the 360/40 with a larger computer that would control the 7-D unit and at the same time convert elementary display coordinates into perspective form and suppress hidden lines.

The University of Utah display consists of a headset shaped like a huge pair of goggles, a head position sensor, and a collection of high-powered computing equipment. Two small precision CRTs face forward on either side of the headset; an optical assembly brings stereoscopic images of the tubes in front of the observer's eyes. Half-silvered mirrors are included to let the wearer see through the CRT image, which thus appears to float in midair.

Ivan E. Sutherland started work on the system while a professor at Harvard University. Now president of the Evans and Sutherland Computer Co. in Salt Lake City, he is also a part-time lecturer at the university where he directs graduate students on the display project.

The system senses changes in head position and adjusts the observed image accordingly. This is achieved with high-resolution counters connected to two universal joints and a spring-loaded, telescoping shaft. The shaft, in turn, connects the top of the headset to a reference point on the ceiling and keeps track of the observer's position changes in the room and the direction of his glance. It has a resolution of $\frac{1}{1,300}$ inch vertically and $\frac{1}{21}$ to $\frac{1}{15}$ inch horizontally. The shaft allows the user to move in a space measuring about five feet square and two feet high. Head tilt range covers 33° up to 80° down.

Control equipment includes a general-purpose computer and two special-purpose computers: a matrix multiplier and a clipping divider. These allow the display to follow the observer's movements around the room in real time. The matrix multiplier does most of the computations that translate the observer's head positions and the coordinates of displayed objects into display coordinates. The clipping divider eliminates objects that are out of the observer's field of view and cuts the ends off line segments that are only partially in view.

Every display is generated twice, once for each CRT, to achieve a 3-D effect. However, the investigators have learned that head motions contribute to the observer's depth perception far more than does the stereoptic presentation.

At present all objects appear as wire models. Ultimately, the developers hope to factor in other display work so that edges on the rear of the displayed object would not be shown and the image would appear solid. This appearance would be enhanced further if halftones could be added. Other projects at the university are involved in these problems.

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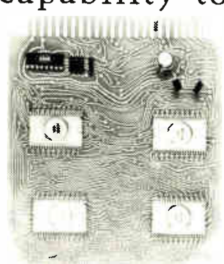

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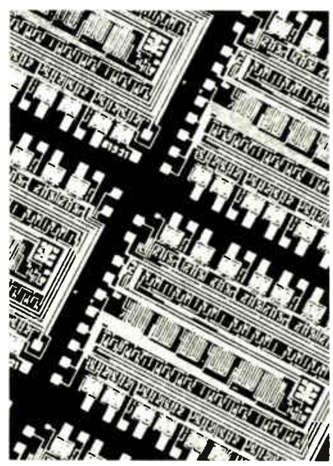

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Minicomputer has 300-ns IC memory

Desktop Supernova, all-semiconductor machine, uses silicon-gate technology; 2 new Novas also unveiled

Less than two months after an all-semiconductor desktop computer appeared on the market [*Electronics*, Sept. 14, p. 52], and immediately after a semiconductor main-frame memory appeared in a large general-purpose computer (see p. 125), an all-semiconductor minicomputer showed up alongside them. These developments—the first by Four Phase Systems, the second by IBM, and the third by the Data General Corp.—make incontestable the thesis that semiconductor main memories are here to stay.

The minicomputer—Data General's Supernova SC—made its debut with two other 16-bit minicomputers, the Nova 1200 and the Nova 800, which are faster, more advanced versions of the company's two-year-old Nova and have core memories.

In some ways, the Supernova SC isn't so mini. In speed, it outclasses the more sophisticated model IV/70 of Four-Phase Systems—thanks to the use of silicon-gate technology. This permits the SC's memory to cycle at 300 nanoseconds, compared to 1.9 microseconds with the IV/70's aluminum-gate technique.

Both the Supernova SC and the Nova 800 are fully parallel 16-bit machines; the Nova 1200, which also has a 16-bit word length, processes data internally in 4-bit "nibbles." The machines' precursors, the unnumbered Nova and Supernova, processed 4-bit and 16-bit chunks of data, respectively. Data General says it will use the Intel Corp's 1,024-bit random-access metal oxide semiconductor memory [*Electronics*, Aug. 3, p. 68] and that it is also considering several alternative sources.

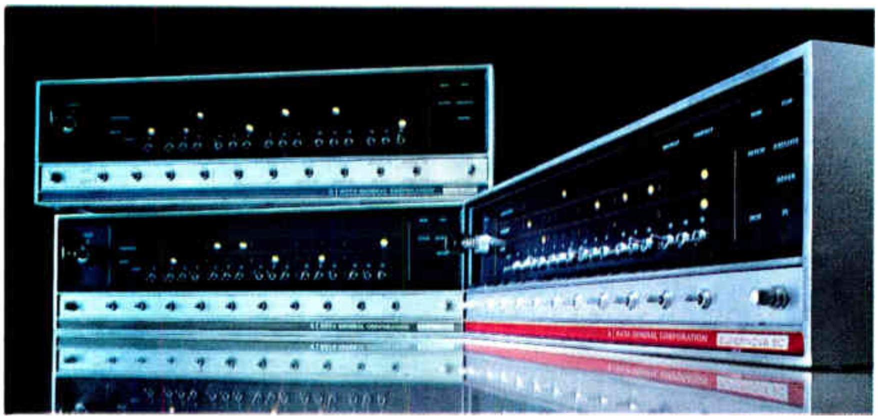
The three new Data General computers are compatible with each other and with the company's previous machines. Software is common for all of them, and input-output interface hardware is interchangeable.

Principal applications for the Supernova SC are expected to be in market areas requiring speed previously unavailable in small-scale computers. Even more important than cycle time, says the company, is the ability of the Supernova SC to execute arithmetic and logic operations in a single memory cycle. It can add two numbers in 300 ns, for example. This is possible because the machine is designed to overlap instructions: its central processor reads out a new instruction while it executes the previous one.

The instruction overlapping technique takes advantage of the inherent nondestructive readout characteristic of a semiconductor memory. With a core memory, data first must be read. and immediately rewritten. Most minicomputers are designed to execute instructions during the rewrite phase. A semiconductor memory, however, does not require the rewrite phase, since it is nondestructive, that is, reading data doesn't alter the memory. Therefore, the Supernova SC is designed to execute instructions during the read phase, the rewrite phase having been eliminated.

Supernova SC uses a high-speed, dynamic MOS semiconductor memory. Use of MOS technology offers

Small and fast. The Supernova SC can be a processor in a time-shared system, or a stand-alone computer handling a group of peripherals.



low operating power requirements, simpler manufacturing techniques compared to those for other semiconductor memories, and provides approximately twice the density of bipolar techniques.

Dynamic MOS also yields approximately twice the bit density of static MOS for equally sized chips. The Supernova SC will sell for $11,900.

The Nova 1200, with a base price of $5,450, is the least expensive in the Data General line. It is also the first minicomputer to use large scale integration. LSI chips, each with 64 bits plus address decoding, store 16-bit accumulators.

The use of LSI, along with advanced medium scale integration technology, opened the way for an entire Nova 1200 central processor built with less than 115 integrated circuit packages and mounted on a single printed circuit board. The whole computer, including central processor, a 4,000-word core memory, basic interface, and control panel, uses 230 IC packages.

In spite of its compactness, the Nova 1200 has a basic memory cycle time which makes it more than twice as fast as the original Nova (1.2 versus 2.6 microseconds).

Nova 1200 achieves this speed using a "pipeline" technique. A series of four-bit data "nibbles" flows constantly through the various data paths in the central processor. All of these paths can be operating on different four-bit nibbles at the same time.

The Nova 1200 can perform any of its arithmetic and logical instructions or its jump instructions in 1,350 ns, including time for the pipeline to fill up and empty, and time to execute the instruction.

The I/O facility has a port directly to memory. During data channel operations, data can bypass the central processor. Thus, these data channel operations take place at memory speed.

The core memory system for the Nova 1200 includes several design innovations. Conventional x-y drive circuits and their associated selector circuits have been replaced in the Nova 1200 by sixteen ICs that combine the selection and current driving functions.

The space saved by using the new monolithic x-y drivers, as well as an 18-mil core, have made it possible to construct the Nova 1200 core memory utilizing a mother-daughter printed circuit board configuration. The 4,000-word core system consists of a 9-inch-square daughter board permanently mounted on a 15-inch-square mother board.

The advantage of using the mother-daughter configuration is that the two boards can be built and tested independently, and joined at the last assembly step.

In its basic version, the Nova 1200 consists of only three 15-inch pc boards mounted in a seven-slot chassis, and requires no interboard cabling: all connections are made using built-in connector panels.

The Nova 800 is a fully parallel minicomputer with an 800-ns cycle time. It is a faster, more powerful computer than the Nova 1200, and is designed for use in applications with high I/O requirements.

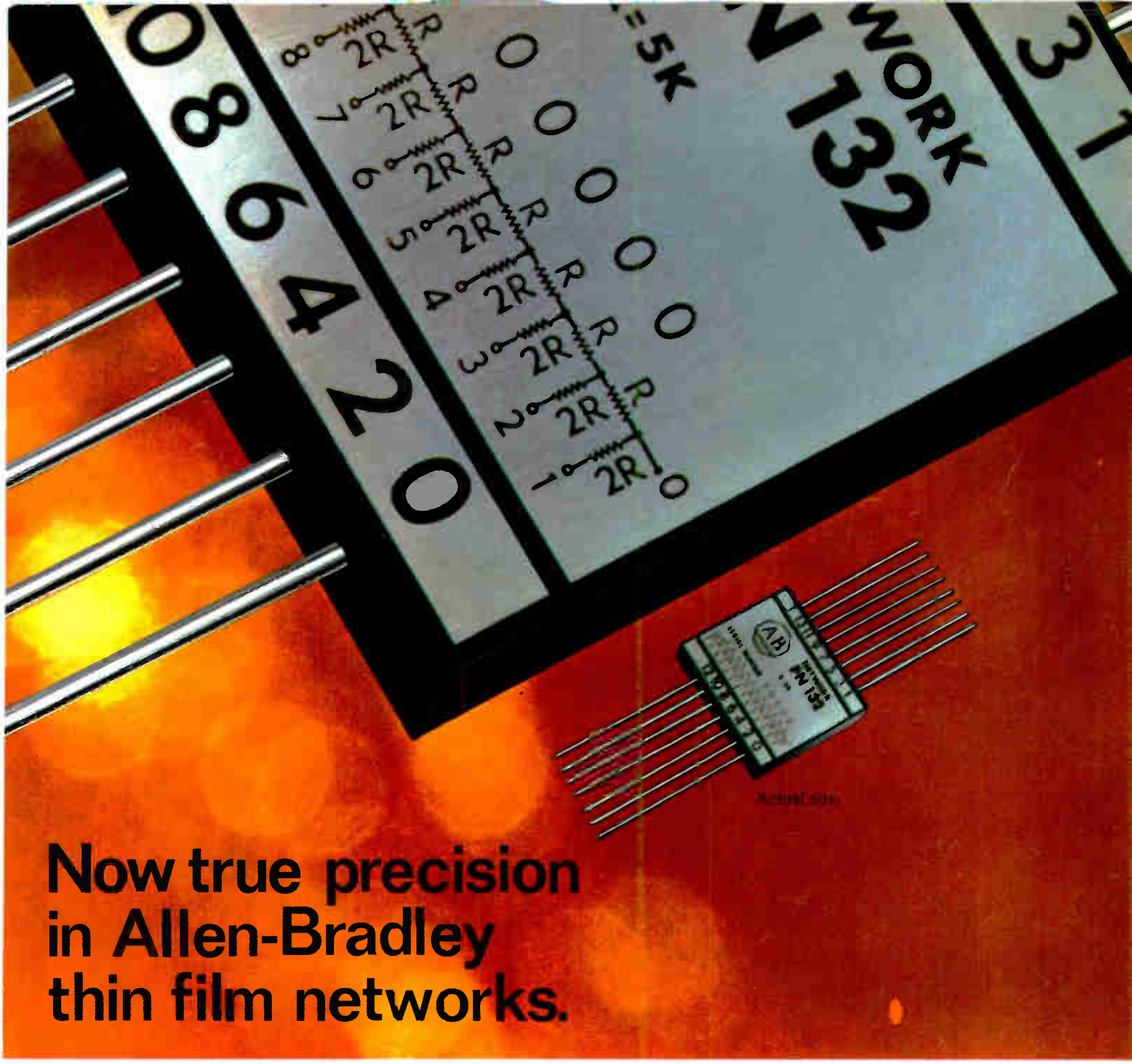
The package for Nova 800 is the same as that for the 1200 except that the 800's more powerful central processor fits on two pc boards. The Nova 800 is a faster computer than the 1200, has a basic cycle time of 800 ns, and has a fully parallel 16-bit central processor.

The Nova 800 includes features which give it a flexible, powerful I/O structure, making it attractive for use in heavily I/O oriented applications. Its I/O system operates at a variable speed. This means that the time required for an I/O operation depends on the nature of the operation.

Hardware multiply-divide, power failure monitor, and automatic restart are built-in options on the Nova 800. Base price for a 4,000-word machine with Teletype interface and data channels will be $6,950, and discounts are available.

First deliveries of the Supernova SC will be in June 1971. The 1200 will be ready in February, and the 800 in April.

Data General Corp., Route 9, Southboro, Mass. [338]



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Data handling

Punched cards alive and well

2 recorders, reader, sorter marketed by new company to handle 96-column format introduced by IBM

After a death watch on the punched card had been proclaimed by some data processing people, that sturdy symbol of the computer age showed new life last summer when IBM introduced the System/3, which uses small 96-column cards instead of the 80-column type. More evidence of vigor appeared this month when Decision Data Corp., formed 10 months ago by a group of ex-Univac employees, announced a line of data handling equipment that will eventually compete across the board with IBM's 96-column-card machines.

First products in the line are two data recorders, a high-speed sorter, and a card reader. All use a metal oxide semiconductor memory developed for the line by Texas Instruments Inc. Decision Data says the memory and other features allow an operator to key data and manipulate cards faster, and at a lower cost, than comparable IBM equipment that uses glass delay lines. What's more, the TI memory is compatible with transistor-transistor-logic circuits.

Jerome R. Dahme, manager of electrical engineering at Decision Data, says the fixed-length delay line was not considered a suitable storage medium, particularly since the company was designing a complete line of both high-speed and low-speed machines, each with its individual requirements for memory size and speed. Cores looked competitive on a cents-per-bit basis, Dahme adds, but not when the designers looked at the cost of the extra interface logic, sense amplifiers and other hardware.

The new machines also use a keyboard supplied by Honeywell's Micro Switch division that incorporates a feature Honeywell says it is now adding as an option on its standard unit.

Called N-key rollover, this feature guarantees the proper se-

Storage for peripherals. The three larger packages on the board at left make up MOS memory for new line of card-handling equipment. At right is a high-speed, multifunction data recorder that uses the memory.

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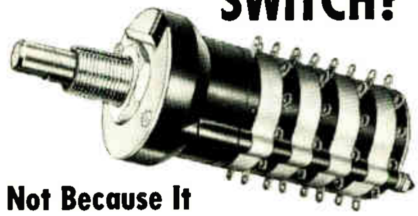

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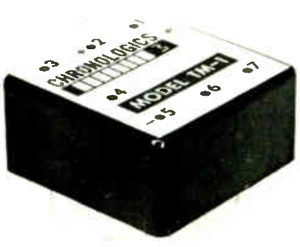

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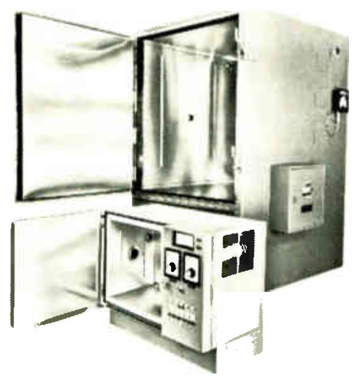

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quence of key input no matter how fast the operator works, and regardless of the let-go sequence in a long succession of inputs. Data bits from the first depressed key are stored in the MOS memory until a second one is actuated, and so on. Honeywell says the feature means 30% fewer errors than in a two-key-rollover system.

In addition to capturing a share of the System/3 market, Decision Data is aiming for replacement of the 80-column card and of key-to-tape equipment "on a cost-of-operation and speed basis," says Frank H. McPherson, marketing vice president. "Thanks to the MOS memory and other innovations, we can operate much more quickly than 80-column equipment or existing 96-column machines." McPherson says his company's data recorders are equivalent in performance to key-to-tape machines while offering the advantages of a readable punched card. "We have the MOS memory's buffering capability just like the tape consoles," he says, "so an operator can't out-key the machine—and we have the convenience of cards for doing rapid consolidation of multi-keypunch output and fast data-handling turnaround."

Decision Data's initial goal will be to sell to original equipment manufacturers, but marketing plans include direct sales to users.

The company's basic data recorder, model 9601, is compatible with System/3 and offers additional features that include blank-card feeding during verification, plus and minus right justification, and fast card feed times—20-30% faster than 80-column equipment, Decision Data says. A more expensive model, the 9610 interpreting data recorder, additionally can print on the card during keypunching and verification. Feed rate of both models is 250 cards per minute and punch rate is 60 cpm for all 96 columns. Price for the 9601 is $5,900; for the 9610, $7,400. Deliveries of the 9601 will begin in December, and in March 1971 for the 9610.

The company says its 9620 alphanumeric sorter can sort 96-column cards 50% faster than current System/3 equipment. The new machine sorts the full 64-character set at 1,500 cards per minute. It has 11 pockets and sorts numeric data with one pass per card column, alphabetic data with 1⅔ passes per column. Effective speed of alphabetic sorting is 900 cpm. The 11 output stackers, with a total capacity of 1,200 cards, minimize card handling by the operator and also result in fewer stops for stacker-full conditions. The 9620 will sell for $5,600. Deliveries will begin in June 1971.

Decision Data's card reader is compatible with IBM's System 360 and similar machines. To reduce operator fatigue, a 2,000-card input hopper and three 1,200-card output stackers have been positioned at tabletop height, and controls are at eye level. An automatic overflow feature increases efficiency by eliminating the need to stop the reader for unloading of cards. In the overflow mode, cards are automatically stacked in the secondary output stacker when the primary stacker is full. Reading continues while the operator unloads the primary stacker and resets card selection to the primary receiver. Pocket selection also can be program-controlled. The company says the 9630 card reader brings economies of 96-column data preparation to large-system users.

Two models are available. The 9630-01, priced at $5,800, includes power supply, control electronics and connectors to interface with the multiplexer channel of System 360/25 and up. Software is available as an option. The 9630-02 is a tabletop unit for OEM use with basic controls and buffer memory to connect with a variety of computer systems. It sells for $4,500. Deliveries of both models begin this month.

The company says it's planning a reader that can be used with the IBM System/3. That computer has a multifunction card unit that is integral to the system.

Decision Data Corp., 300 Jacksonville Road, Warminster, Pa. 18974 [339]

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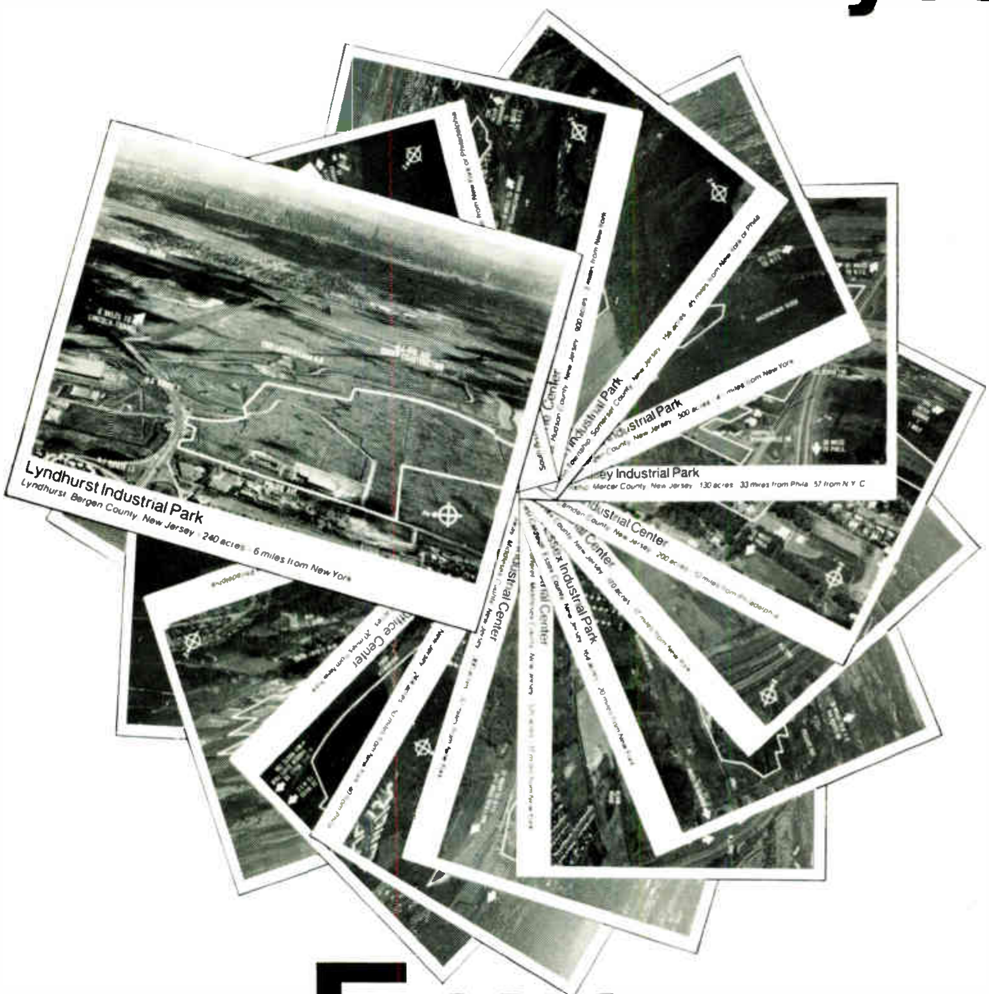

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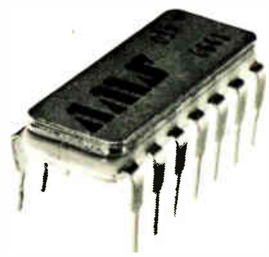
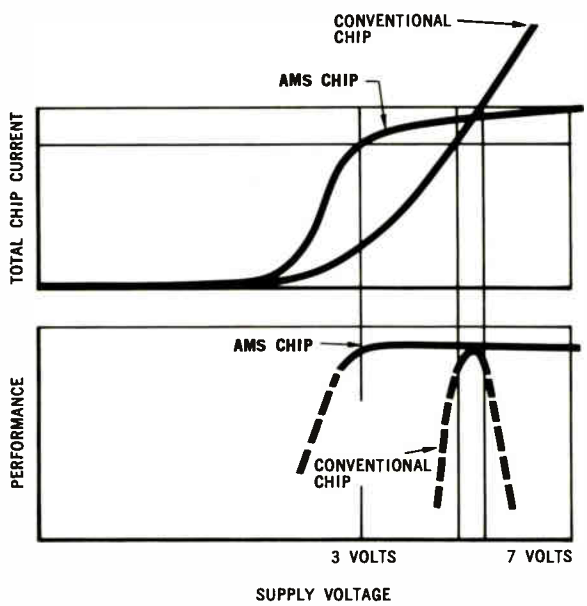
Circle 143 on reader service card





Here's a 7-nanosecond CML memory cell with 64 bits of storage for scratch-pad, register, cache, buffer and control applications.

It's the AMS 0641 — a monolithic, ECL compatible non-destructive-readout RAM. Full address decoding and output sense amplification are included on the chip. Organization is 64 words by 1 bit. Typical access time is 7 nanoseconds and power dissipation is only 6 mW/bit at 5 volts.

Take a look at the curves. The AMS 0641 draws virtually constant current at any supply voltage from 3.5 to 6.5 volts with no sacrifice in performance. And that means a saving in power-supply regulation and power distribution. If you operated the 0641 memory at 3.5 volts instead of the usual 5.2 volts, you'd save 33% on power and still get 7 nanoseconds access time.

To make it easy to use the AMS 0641, we've designed a companion support logic circuit, the AMS SSC-1. It will minimize overhead circuitry and optimize I/O buffering and chip selection. The AMS SSC-1 also operates with a 3.5- to 6.5-volt supply.

For complete information about the AMS 0641 and its companion support circuit, contact

ADVANCED MEMORY SYSTEMS, INC.
1276 HAMMERWOOD AVE., SUNNYVALE, CALIF. 94086 TEL. (408) 734-4330

New products

Components

Connector has up to 155 pins

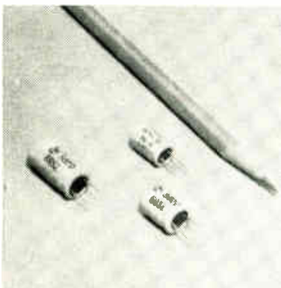
Dielectric retention disk permits high-contact density in standard and power types

Using a one-piece molded dielectric retention disk, the Amphenol Connector division is expanding its line to include high-contact-density connectors in general purpose and power versions for the first time. The new family meets Mil-C-81511 specifications and is keyed to applications in computers, missile and aerospace systems, commercial avionics, radar, conventional and mobile television cameras, and portable communications equipment.

The molded dielectric disk permits higher-density configurations without sacrificing the connector's electrical spacing characteristics, says Don Wehrenberg, product marketing manager. The common method of holding the contacts with metal clips, Wehrenberg says, sacrifices electrical integrity in high-density inserts.

The dielectric, known as polyarylsulfone, was developed by the 3M Company three years ago, when it was discovered that the polysulfone previously used corroded when exposed to cleaning agents such as carbon tetrachloride.

In the highest-contact-rated size 12-12 (12-gauge wire) power versions, the connectors provide 11 contacts in a size 20 shell, 14 contacts in size 22 and 19 contacts in size 24. Beyond 12-12 for power, the new families offer a choice of 16-16 (16-gauge wire), 20-20 (No. 20 AWG), and 23-22 (No. 22 AWG) contacts in a variety of high-density configurations incorporating from 24 through 155 contacts per con-

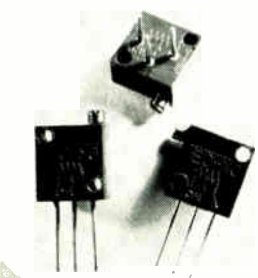


Single-ended, miniature aluminum electrolytic capacitors type 502D are for vertical installation on high-density printed-wiring boards. They will withstand an 85° C life test for 1,000 hours at rated voltage. They are furnished as polar units with an indeterminate resistance between the cathode and the aluminum case. Sprague Electric Co., North Adams, Mass. [341]

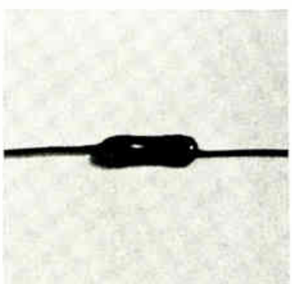
Solid state communications relays in seven different models cover all neutral, polar and complementary input and output combinations. Their most common use is as isolated low-to-high and high-to-low level converters for telegraph and Teletype circuits, data acquisition, machine controls, differential circuits and alarm circuits. Flight Systems Inc., Mechanicsburg, Pa. [342]

Two-pole, double-throw relay series 400 is for applications where light weight and extreme environmental capability are important. The unit, featuring wedge-wipe action, offers optimum performance in accordance with MIL-R-5757/8. It has a low level contact rating to 2 A at 26.5 V dc. Deutsch Relay Division, 65 Daly Rd., East Northport, N.Y. [343]

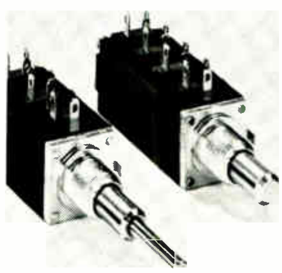
Contactless, solid state relay features complete isolation between input circuit (coil excitation) and output (switching elements). This is obtained by a magnetoresistor which does not require a separate reference voltage. Operating speeds range from micro- to nanoseconds. Normal load current is 200 mA. Emanuel Wolff Co., 1241 Welsh Rd., Huntingdon Valley, Pa. 19006 [344]



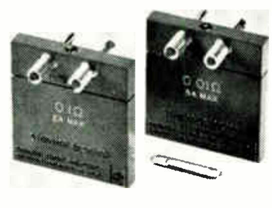
Non-wirewound trimming pots in the Cermet series feature three 3/8-in. square RF24 units with differing pin configurations. The multiturn models meet or exceed MIL-R-22097, characteristic C. Units have a resistance range of 200 ohms to 1 megohm. Temperature coefficient is 150 ppm/°C, with 100 ppm/°C available. Techno-Components, Van Nuys, Calif. [345]



Tera-ohm resistor model 102 measures 0.13 x 0.040 in. diameter. The thick-film devices are presently used in liquid hydrogen cooled infrared detectors at 4.2°K. A semiconductive glass resistive element provides high stability and reliability. Temperature coefficient of resistance is −0.3%/°C maximum. Price (1-24) is $8. Eltec Instruments Inc., Lancaster, N.Y. [346]



Versatile, panel-mounted, 5/8 inch square potentiometers in the series 70 family are supplied as single- or multiple-section units. They are available in cermet, carbon, and combination cermet and carbon, with resistance ranges of 100 ohms to 2.5 megohms for cermet and 50 ohms to 10 megohms for composition. Allen-Bradley Co., 1201 South Second St., Milwaukee 53204 [347]



Two models of the type 1440 standard resistors, the 0.1- and 0.01-ohm versions, are made of sheet Manganin punched in a random pattern to reduce inductance. Both come in sealed, oil-filled diallyl phthalate boxes to promote long-term stability and to provide mechanical protection. Temperature coefficient is 20 ppm/°C. General Radio Co., West Concord, Mass. [348]

Joining the family. High-density version saves 20% in costs over present 128-pin assemblies.

nector insert arrangement.

Previously, a 42,000-circuit application calling for size 24 shell, for example, was limited to 128-contact connectors—for a total system requirement of 328 units. With the 155-contact configurations, the number of required connectors drops to 271.

Another comparison made by the company—taking a square size-24 flange receptacle's contact-per-square-inch factor for Amphenol's 155-contact configuration versus the conventional 128 contacts—shows an improved contact efficiency of 20%.

In evaluating cost-per-circuit, the price per connector pair is divided by the number of mated contacts. The 128-contact version costs about 62 cents per contact pair, against the 155 version's 50 cents.

Other features include shell-to-shell grounding fingers prior to contact mating for maximum attenuation of radio frequency interference, triple-track bayonet coupling for positive locking and vibration resistance, multiple mating seals for environmental protection, and six key positions in each shell size for prevention of mismating and ability to gang-mount similar insert arrangements.

Mil-C-81511, design standard for the new line, has been recommended as the tri-service connector standard for all military electronic equipment produced by NATO countries. This should minimize the number of connectors and simplify logistics.

Amphenol Connector Division, The Bunker-Ramo Corp., 2801 South 25th Ave., Broadview, Ill. 60153 **[349]**

New products

Switch's color, intensity change with on-off state

In high ambient light, it is often difficult to see whether an illuminated pushbutton switch is on or off. But a new type, called the Rainbow line, solves the problem in a bright way.

Developed by Marco-Oak Industries, a division of Oak Electro/Netics Corp., this device has a prism arrangement at the sides of the cap. Switching it on allows the ambient light to hit the prism, causing a color band in the button to glow brightly. Switching it off causes another color band to light up dimly. So, the brighter the ambient light, the greater the change in the button.

The first model in the line has a 0.75 inch by 1 inch cap that is divided into three sections—a color band at top and bottom separated by a fixed color band. If the top and bottom bands are of different colors and the button is pressed, both intensity and color change. Further, each band may carry a legend which will appear or disappear as the colors change. The center bar also can be made to disappear as the switch changes state.

This switch is available in almost any color, and its two color bands may be the same or different in hue. The switch requires a small amount of tooling for mounting in a circular hole. However, among the new sizes and shapes planned for the line is one that will snap into a rectangular hole in a panel; it will have either a ¾ inch by 1 inch or a ⅝ inch by ¾ inch cap.

Applications include the control panels in military and commercial aircraft, pleasure boats and data processing equipment.

The cap and switch assembly is priced between $4 and $6 in 1,000 lots, depending on size and type. The cap is also sold separately for 70 cents each in 1,000 lots, but fits only into a Marco type 771 or 772 Press-Light switch assembly.

Marco-Oak Division of Electro/Netics Corp., Anaheim, Calif. [350]

Instruments

Tester checks ICs in 10 s

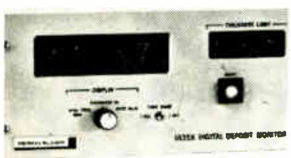
System for pc boards uses Gray code to try all possible circuit states

Incoming inspection of integrated circuits has become common practice, but even though the circuits are tested, the chance of error in a completed board may run as high as 40% because of solder bridges and open lines. The only way to catch these errors is to test the completed board, and up until now this has meant either the purchase of a $20,000 piece of equipment or many hours of testing with an oscilloscope. But the Data Test Corp. has changed this with the announcement of its model 4000 printed circuit card test system which sells for $2,000.

According to Dan Marshall, marketing manager at Data Test, the 4000 was designed "specifically for intermediate and small manufacturers of IC cards. It can be used for troubleshooting and diagnostic work both in the field and on the bench."

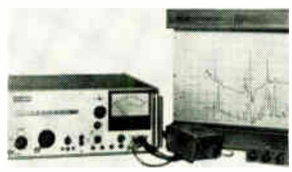
The 4000 works by applying square waves to the inputs of the board and then checking the outputs to see how they have changed. The input signal is a Gray code—a digital code that produces only one change of state at any given instant of time. In this way, every possible combination of input signal from all 0s to all 1s can be achieved, and so all of the possible states of the circuits on the board can be duplicated.

To set up a board for testing, a unit that is known to be good is put on the tester and the different inputs are exercised. Because not

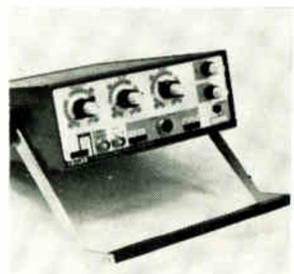


Digital deposit monitor DDM eliminates mode changes and temperature effects. It measures thickness and rate digitally to 5 places and provides analog signals to control these functions. It resets to zero in less than 100 ms. Accuracy of thickness measurement will not be lost when a rate is set before shutter is opened. Ultek Div., Perkin-Elmer, Box 10920, Palo Alto, Calif. [361]

Broadband phase meter series 305 features a direct reading accuracy of $\pm 0.1°$ over the full 360° range. With independent input levels of greater than 60 dB, the instrument requires no adjustment for input level or frequency change either during warmup or over extended operating periods. Frequency range is 5Hz to 10 MHz. Dranetz Engineering Laboratories Inc., Plainfield, N. J. [362]



Simultaneous plotting of the peak and average levels of received signals is possible when detector/junction box model DJB-25 is used with interference analyzer/receiver model EMC-25 and dual-pen recorder model EXY-250. Such dual plotting was not previously possible with only a single receiver. Electro-Metrics Corp., 88 Church St., Amsterdam, N. Y. 12011 [363]



MOS driver model G720 is intended for use as a clock or data driver for MOS ICs. It features 5 Hz to 10 MHz repetition frequency, delay and width from 50 ns to 200 ms, risetime 1 ns/V with a 100 pF load, and two separate, buffered trigger outputs. Dimensions are 3½ x 8½ x 12 in. Price is $495. E-H Research Laboratories Inc., P. O. Box 1289, Oakland, Calif. 94604 [364]

Pseudo-noise transmission test set model 1100 tests synchronous and asynchronous digital data transmission system modems, digital multiplexers, time sharing networks and advanced communications systems. Simply plug the test set into the standard EIA interface that is common to most modems and turn power on. International Data Sciences Inc., Providence, R. I. [365]

Real-time calibrated frequency domain measurements can now be interpreted automatically by a minicomputer using the new Mini-Ubiq spectrum analyzer model UA-10. Unit is specifically designed for ease of interface with digital computers. Timing and transfer of frequency data is controlled by the computer. Federal Scientific Corp., 619 W. 131st St., New York, N. Y. [366]

Digital transducer indicator model CD23 is for use with variable reluctance transducers and other bridge excited units. It provides a 3½-digit readout in addition to the ± 10 V dc output for recording and dynamic monitoring. It operates on 105 to 125 V, 60 Hz at 7W, providing long-term stability of 0.1%. Validyne Engineering Corp., 18819 Napa St., Northridge, Calif. [367]

Tong-type ammeter 705A has extended ranges for both dc and ac measurements (0-400A). It offers 4 linear scales with 2% full scale accuracy. Test measurements are made by selecting correct range (dc or ac) and clamping tongs around single conductor (insulated or bare), bus bar, or cable up to 1¼-in. diameter. Pacer Industries Inc., 17035 Burnham Ave., Lansing, Ill. [368]

all input combinations will have an effect on the output, each output will go through a certain number of transitions for one set of inputs. Thus, if the number of transitions for an output on a good board is noted, it can be compared to the number from a board under test. If the numbers are the same, that particular output is good. The 4000 can check boards with up to 20 outputs with front-panel push-button selection, and a three-digit counter readout is provided; a fourth digit is optional.

The other pc card testers on the market are large machines that have to be programed to supply only the inputs that affect an output. Marshall says these testers run at a 4 to 5 kilohertz rate whereas the 4000 runs at 250 kHz. Thus, even though the 4000 runs through all possible input combinations, the 20 tests take only 10 seconds. "And we run through all of the inputs twice," says Marshall, "so the ICs are always in the same state when the test starts."

Once a bad output is spotted, the fault on the board can be located by using a probe connected to the 21st input on the tester. The procedure is then similar to checking the outputs: the inputs are stepped through all combinations while a specific point on the board is checked and the count compared to a known total.

For customers who want a more automatic system or one that is programable, Data Test offers the model 4300, which automatically sequences through the 20 tests, and the 4700, which is an automatic test station that can be programed with punched cards. The 4300 sells for $4,450, the 4700 for $10,750. Optional equipment can tailor a system for a user's special needs. The options include card readers, printers, program boards, test adapters to interface the board to the tester, and level shifters to change transistor-transistor-logic voltage levels to metal oxide semiconductor levels.

Data Test Corp., 822C Challenge Drive, Concord, Calif. 94520 **[369]**

Digital meters priced to vie with analog units

Most multimeters found in industrial laboratories or used by service organizations are of the analog variety. But as prices for digital meters drop closer to the $100 top figure for analog types, a trend favoring digital units could begin.

In Numeric Laboratories' 300 series of digital multimeters, the model 350 is priced at $179 and measures dc voltage, dc current, and resistance. The model 351, at $195, measures dc voltage and current, resistance, and ac voltage and current. Robert Battes, president of Numeric, says the meters are comparable in accuracy to analog instruments but are not intended to compete with more accurate digital multimeters that are priced in the $400 range. Key to the low price, Battes says, is a new input signal conditioning circuitry design that provides the basic analog-to-digital conversion process.

The meters feature high sensitivity. They resolve 10 millivolts and 10 nanoamperes—values beyond the capabilities of bench-type analog meters. Both models have a basic accuracy of 1%, and a minimum of 10% overrange within specifications. In addition, they include an automatically positioned decimal point and a sampling rate of 60 times per second.

Each of the two units measures 5¼ by 6¾ by 2½ inches and weighs under two pounds. A battery pack is offered as an option.

Numeric Laboratories, 329 S. Greenwood Avenue, Palatine, Illinois 60067 **[370]**

Subassemblies

2-chip op amp challenges 740

Hybrid format permits separate optimization of FET input function

No longer dependent on outside suppliers for special-design integrated circuits, Analog Devices has gone to market with a line of advanced operational amplifiers using circuits developed and manufactured by its affiliate, Nova Devices of Wilmington, Mass.

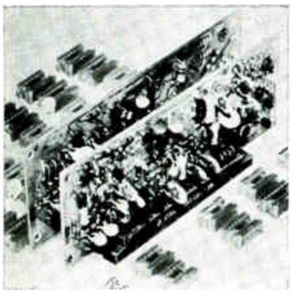
The first entry takes direct aim at a highly visible target, the widely used 740-type op amp. Analog says its AD 503 series meets or beats the 740 spec for spec, and at a lower price.

Typical bias current for the 503J is 15 picoamperes, versus 100 pA for the 740C—maximums are 50 pA and 2,000 pA respectively. The narrow bias spread of its unit, says Analog, is due to tight process control procedures at the Nova plant.

Voltage and current offset specs also favor the Analog/Nova device. The 503J's typical offset voltage is 20 millivolts and 30 mV for the 740C. Typical current offset is 5 pA for the 503J, versus 60 pA for the 740C.

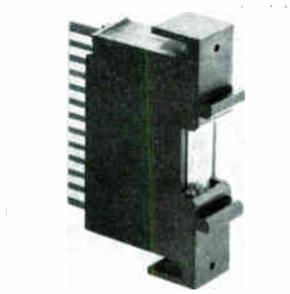
Voltage offset temperature coefficient—which several makers of 740s don't specify—is 20 mV/°C for a typical 503J and 30 mV/°C for a 740C.

To reach this level of performance, Analog/Nova went to a hybrid format; the input FETs are on a separate chip and thus can be optimized for their task and the rest of the op amp optimized for its functions. According to Analog/Nova, monolithic FET-input 740s are limited by the incompatibility

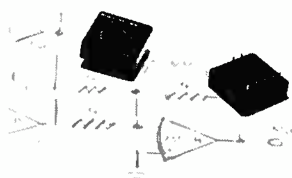


Plug-in, bipolar voltage-to-frequency converter 1700-5072-00 provides linear conversion of 0 to ±10 V dc to 0-to 1-MHz frequency in a compact, modular package. Linearity is better than 0.01% and the operating temperature range is −10° to + 65° C. Converter is priced at $350. Anadex Instruments Inc., 7833 Haskell Ave., Van Nuys, Calif. [381]

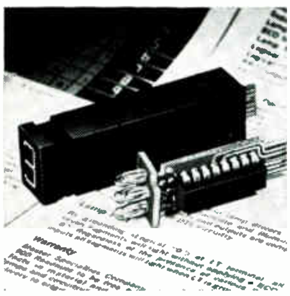
Class S amplifiers type K-201 are being offered from 5 Hz to 1 MHz and with power ratings from 0.5 to 50 kVA. Class S offers efficiency over 90% and is particularly applicable to driving underwater sound sources which contain matching networks so that the harmonic components of square cornered waveforms are suppressed. Instruments Inc., Midway Dr., San Diego, Calif. [382]



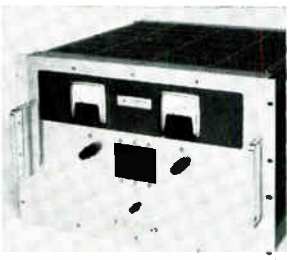
Plug-in modules series DM-17G are factory-assembled, ready-to-use devices featuring a miniature Elfin display and decoder-driver. The neon Elfin is front mounted on a pc board that contains the decoder-driver and the logic required to accept 4-line BCD inputs. All input-output contacts appear on the pc connector. Alco Electronic Products Inc., Box 1348, Lawrence, Mass. [383]



Differential FET op amp 3400B has a 100 MHz small-signal bandwidth and a large-signal slew rate of 1,000 V/μs. As a result of the differential input, the unit can be used as a noninverting buffer amplifier. The FET input gives a maximum bias current of 100 pA. Common mode voltage is ±10 V minimum. Burr-Brown Research Corp., Int'l Airport Industrial Park, Tucson [384]



Fiber-optic readout model 901 D2-D8, available with a choice of five different built-in decoder/driver ICs, reduces mounting, wiring and pc board requirements as well as equipment size. The IC decoder and lamp drivers will accept 4 line 8-4-2-1 BCD inputs, translate them and then illuminate proper readout segments. Master Specialties Co., 1640 Monrovia, Costa Mesa, Calif. [385]



High-current power supply series LB-720 is for use in main-frame computers, component life tests, aging racks and test equipment. It performs at 80% efficiency at current ratings to 300 amperes and voltage ranges to 300 V dc. Six different models are offered at voltage ranges from 0-7.5 V to 0-300 V. Lambda Electronics Corp., 515 Broad Hollow Rd., Melville, N.Y. 11746 [386]

Six crystal-controlled frequency sources in the 5400 series generate frequencies from 1 kHz to 10 MHz and come in graded stabilities from 1 part per million to 10 ppm from 0° to 65° C. All frequency/stability combinations are available in either flat-pack or compact cases. All models operate on +5 V input, logical output. MF Electronics Corp., 118 E. 25th St., New York [387]

Class A amplifier 300P covers the frequency range of 250 kHz to 110 MHz. The solid state module can provide over 30 W of power output from virtually any signal or sweep generator. Characteristics include a gain of 40 dB, input/output impedance of 50 ohms, and VSWR less than 1.5:1. Price is $450. Electronic Navigation Industries Inc., 1337 Main St. East, Rochester, N. Y. [388]

of FET transistors with the lightly doped n-type epitaxial silicon needed for the bipolar chip—a lightly doped p-channel diffusion creates the needed FETs, but also means high leakage current; for example, the 2-nanoampere maximum bias current specified for the 740C.

The FETs in the 503 are n-channel devices, binned for low leakage (as low as 1 pA with separate FETs), with their offset voltage trimmable to zero.

FETs are also said to reduce yield in the monolithic format, and Analog/Nova spokesmen state that this is one reason why 740 makers generally settle for higher leakage specifications.

The 503 and 740 are a long way from identical even in schematic form. The 503 uses only 26 transistors, versus 33 for the 740 type. In the process, the 503 achieves a lower noise specification: typically 7 microvolts rms, compared with 24 μV rms for 740.

Analog/Nova also uses a different trimming technique that helps keep down temperature-induced drift. Instead of trimming the input FET's base current, the 503 is trimmed by changing the emitter current through two resistors at the first pnp transistors, dissipating 90% of the nulled-out current in the resistors and 10% in the transistors. Thus, trimming adds no more than 6.6 μV/°C to the circuit's drift.

With a typical 740, there are four added transistors and four more resistors at the input, mostly to aid trimming. But with the average offsets of most 740s, trimming will add about 160μV/°C to the drift specification, according to Analog engineers.

The 503 is available in a TO-99 can, and is shipped from stock in both industrial and Mil-Spec versions. Price for evaluation lots is $22 for the AD503JH, and $33 for the military type AD503KH. In lots of 100 to 999, prices fall to $15 and $22, respectively.

Analog Devices Inc. (Nova Devices affiliate), Wilmington, Mass. 01887 [389]

Winter on Colorado's front range?

No. Winters on Colorado's Front Range of Science and Technology – the 150-mile span where the high plains meet the mountains – are dry, mild, sunny and warm. What you are seeing here is 50 miles away, in the higher elevations of the Rocky Mountains . . . where "Ski Country, USA" is the world's winter playground.

It's something else.

While skiers are on the slopes, there's shirtsleeve golf and tennis in Metro Denver and other Front Range communities. There's more sunshine than most places. It's a great place to be. And that's part of the reason that IBM, Kodak, Honeywell, Bell Telephone Laboratories, Western Electric, Martin Marietta, Hewlett-Packard, Sundstrand, Colorado Instruments, Inc., Monsanto, Beech Aircraft, Ball Corp., and other top blue-chip companies are here.

DENVER IN WINTER: WARM, DRY, SUNNY. HOW IS IT WHERE YOU'RE AT?

	Maximum Daily Temp. Average	Average Mo. Precipitation	Average Pct. Available Sunshine
October	66.6	1.01	75
November	51.6	.69	66
December	45.2	.47	68
January	42.1	.55	73
February	44.6	.69	71
March	49.9	1.21	71
	50.0°F	4.62	70.6%

Source: National Weather Record Center, Ashville, North Carolina

WRITE TODAY – There's a very pleasant economic climate, too. If you are looking for a single location for a new plant site, research facility, administrative headquarters, or distribution center . . . or for a large unit tract of land . . . Forward Metro Denver will give you complete information. Everything in absolute confidence. Write Manager, Forward Metro Denver, Department 309, 1301 Welton Street, Denver, Colorado 80204. Phone: (303) 534-3211.

FORWARD METRO DENVER

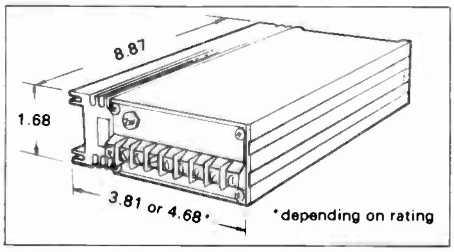
Circle 155 on reader service card

A new low in power supply design.

Acopian's new low profile power supply offers outstanding performance. Line and load regulation is .005% or 2 mv. Ripple is 250 microvolts. Prolonged short circuits or overloads won't damage it. And built-in overvoltage protection is available as an option.

Yet, it's the thinnest, flattest, most "placeable" 4.0 amp series regulated power supply ever offered . . . just 1.68" low. This low profile makes it perfect for mounting on a 1¾" high panel, or vertically in a narrow space. Acopian's new flat package gives you design flexibility never before possible. And a surprisingly low price gives you extra budget flexibility as well.

Standard models include both wide and narrow voltage ranges. Outputs from 0 to 48 volts. Current ratings from 1 to 4 amp. Prices from $80.00.



For the full low-down on the new low-down power supply, write or call Acopian Corp., Easton, Pa. 18042. Telephone: 215-258-5441. And remember, Acopian offers 82,000 other power supplies, each shipped with this tag . . .

Semiconductors

3-state TTL line expanded

National adds demultiplexer and party-line driver for bus-organized data systems

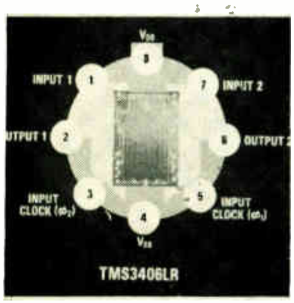
With increasing emphasis being placed on data-bus design in computers and peripherals, National Semiconductor has added two medium-scale integrated devices to its family of three-state transistor-transistor-logic circuits [*Electronics*, Sept. 14, p. 78].

For use with a multi-connection data bus, the most important characteristic of the line is that, in addition to the conventional TTL logical 1 or logical 0 outputs, the devices also can be switched into a third, high-impedance state that will virtually disconnect an output from a transmission line so that no data can flow.

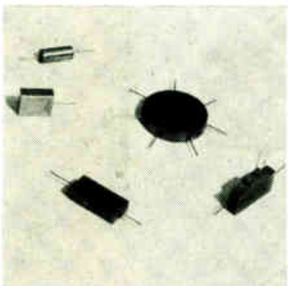
The new units are the DM7230/8230 demultiplexer and the DM-7831/8831 line driver.

The party-line driver is the most powerful of the tri-state logic devices. Each of the four drivers in the monolithic circuit puts out 40 milliamperes and can drive up to 900 feet of bus line, or up to 25 standard TTL inputs. Yet it is as fast as standard TTL, and is completely compatible with it in logic levels and also in power supply requirements.

The device can drive four different bus lines in a quad single-ended mode, drive two pairs of bus lines in a dual single-end mode, or operate as a dual differential driver on twisted-pair transmission lines. And with about 20 gates on the chip, the DM7831/DM8831 can perform special logic functions such as control interlock and comple-

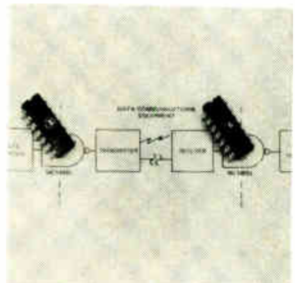


MOS shift register IC designated model TMS3406LR features a 2 MHz guaranteed frequency operation and low power dissipation of 0.4 mW per bit typically at 1 MHz. It consists of two separate 100-bit shift registers with independent input and output terminals. Price in 100 to 249 piece quantities is $6.50. Texas Instruments Inc., Box 5012, M/S 308, Dallas, 75222 [436]

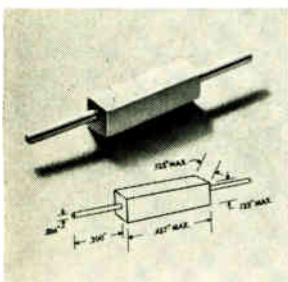


Semiconductor integrated limiter modules MA-8460 and MA-8445 are designed for use from 0.1 to 12 GHz. They feature complete hermetic sealing using metal-to-glass seals, seam-welding techniques, and passivated diode chips integrated into broadband distributed filter networks. These features help in reducing package size. Microwave Associates Inc., Burlington, Mass. [437]

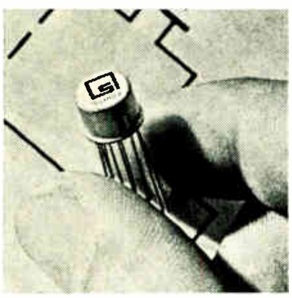
Pnp, diffused alloy power, germanium transistors feature high current capabilities and extremely fast switching times. They may be used in commercial and military applications including inverters, converters, switches, power supplies and control circuitry. Units are available for off-the-shelf delivery. Solitron Devices Inc., 1177 Blue Heron Blvd., Riviera Beach, Fla. 33404 [438]



Two modem ICs meet the requirements of EIA RS-232-C standard. Both the MC1488L quad line driver and the MC1489L quad line receiver are DTL/TTL compatible devices designed to provide systems interfacing between communication networks and data terminal equipment. Each operates over the 0° to 75° C range. Motorola Semiconductor Products Inc., Box 20912, Phoenix [439]

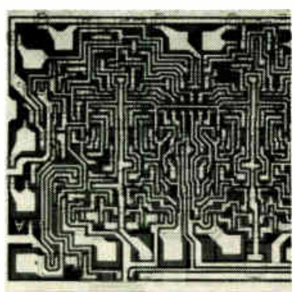


Fast recovery, high-voltage silicon rectifiers series DR measure 0.437 in. in length x 0.125 in. square with leads 0.016 in. in diameter and 0.200 in. in length. Furnished from 3,000 to 10,000 peak inverse voltages and rated at 25 mA, the units have avalanche characteristics with max. reverse recovery time of 300 ns. Electronic Devices Inc., 21 Gray Oaks Ave., Yonkers, N.Y. [440]



MOS dual 100-bit static shift register model N2010K operates at shift rates ranging from zero to 3 MHz. The unit allows replacement of dynamic registers that require attendant refreshing circuits. Typical propagation delay is 200 ns, and 250 ns is maximum. Operating temperature range is 0° to + 70° C. Signetics Corp., 811 E. Arques Ave., Sunnyvale, Calif. [441]

Silicon power transistors STS-1131 to STS-1134 are triple diffused npn units. The collector emitter voltage ratings range from 225 V for the 1131 to 400 V for the 1134. Current gain at 3A is a minimum of 18 and a maximum of 60. Temperature range is 200° C, which permits reliable operation in high ambients. Sensitron Semiconductor, 221 W. Industry Ct., Deer Park, N.Y. [442]



Low-power MSI series 9200 operates with fan out and speeds that allow designers to replace 9300 devices with 9200 units in most applications to take advantage of reduced power operation. Typical of the series are the 9210/16 counters that operate with 75 mW of power producing a counting speed of 13 MHz. Advanced Micro Devices Inc., 901 Thompson Pl., Sunnyvale, Calif. [443]

←Circle 156 on reader service card

menting of data and clocks being transmitted.

Each of the four party-line drivers on the chip has a line-drive or fanout capability of at least 25 at 70°C at a minimum guaranteed input short-circuit current of 40 mA. The maximum—which is not guaranteed—is 120 mA, equivalent to a fanout of about 75.

Output current is 100 times the standard TTL device's 400 microamps. Since very little of the 40 mA is needed for fanout (40 μA per receiver), the rest can be put to work supplying leakage current to other drivers in the third state on the same bus line.

Each device contains two input and four output data channels. Either of the two input channels can be switched to any of four bus lines. The two inputs also can be switched simultaneously to two outputs. Input data or clock signals can be complemented for transmission over twisted-pair lines or conventional bus lines.

The demultiplexer can perform an almost limitless variety of data-transfer functions in bus-organized digital systems. And many devices can be connected to bus lines. As many as 128 demultiplexers—512 individual outputs—can time-share four lines of a single bus. And the new unit is also the first high-speed TTL demultiplexer that can handle two-way communications on a bus.

The principal use of the DM-7230/DM8230 in TTL bus-organized systems, will be in replacing conventional demultiplexers, bus-interchange logic assemblies, and open-collector TTL gates with pull-up resistors and buffers.

Standard TTL can only be connected to bus lines through open-collector gates, which have very low fanout and are slow—about 30 nanoseconds propagation time per gate. The DM7230/DM8230's typical propagation delay is 18 ns and it can change modes in 20 ns.

Commercial versions of both devices are priced at $5.85 each.

National Semiconductor Inc., 2900 Semiconductor Dr., Santa Clara, Calif. [444]

Fast random memory includes full decoding

When 256-bit bipolar random access memories were first designed, only partial decoding was included on the chip. The devices would have been too big and thus yield would have been too low if complete decoding had been included. But a new 256-bit RAM from the Intersil Memory Corp., the IM5503, employs a smaller cell size and so the company was able to include complete decoding without adversely affecting yield. And as a bonus, "the device is twice as fast (60 vs. 120 nanoseconds) as the others on the market," says Joseph D. Rizzi, vice president of bipolar operations at Intersil.

"Other companies use an epitaxial resistor made of 180-ohm per square material," says Rizzi, "but we employ material that's 1,000 Ω per square. We get higher resistance in less space and so our device is smaller." He adds that the process is easy and so yield is not affected. The chip measures 120 mils on a side.

The memory is organized as 265 words by one bit and designed for high-speed scratchpad, fast buffer, and mainframe applications. Moreover, it is compatible with diode-transistor and transistor-transistor logic circuitry. On-chip address decoding along with chip select, write enable, and uncommitted collector outputs allow for easy connection of the units into large arrays.

Another feature of the memory is its low power dissipation—1.5 milliwatts per bit; and the entire chip, including address decoding and the write and sense circuitry, dissipates less than 625 mW maximum. Typical word access time is 75 ns.

The device is available off-the-shelf in a 16-pin ceramic dual in-line package, and in two temperature ranges. The 0° to 75° C unit sells for $57 in quantities of 100, and the —55° to 125° C unit sells for $85 in quantities of 100.

Intersil Memory Corp., 10900 North Tantua Ave., Cupertino, Calif. [445]

New products

Materials

Adhesive for instruments cures in 30 min at 65°C

Low-viscosity epoxy adhesive, called Epo-Tek 305, is recommended for optical and instrumentation applications. It is spectrally transparent from 2,500 angstroms to 2.6 microns. The two-component compound cures overnight at room temperature or in 30 minutes at 65°C. It bonds tenaciously to a wide variety of substrates with a lap shear strength of 1,700 lb/in.². A 4-oz trial evaluation kit is available at a nominal price of $10. Epoxy Technology Inc., 65 Grove St., Watertown, Mass. **[401]**

Ferrite beads, designed to solve noise and filtering problems, feature easy installation and considerable savings in space. They provide effective rf decoupling, shielding, and parasitic suppression without sacrificing low-frequency power or signal level. The beads are installed by simply sliding one or more over the conductor leads. They can, but need not, be grounded. National Moldite Co., Newark, N.J. **[402]**

Metalclad DP-537 is a printed circuit board protective coating that illuminates under ultraviolet light to show any defects that might occur during the coating process. It features moisture vapor permeability, chemical resistance, abrasion resistance, and resiliency in thin films. The system protects against oxidation and corrosion on metal substrates. Mereco Products, 530 Wellington Ave., Cranston, R.I. 02910 **[403]**

Abletherm 12-1 is a highly-filled, silicone base adhesive designed for instrument bonding applications that require both high thermal conductivity and repairability. It is suited for flatpack to heat sink bonds. The material withstands continuous exposures to 400°F. Its insulation resistance exceeds 1×10^{14} ohm-cm at 77°F. Ablestik Adhesive Co., 833 W. 182nd St., Gardena, Calif. **[404]**

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New Books

Shaping up

Active filters: lumped, distributed, integrated, digital, and parametric
Lawrence P. Huelsman
McGraw-Hill Book Co., N.Y.
372 pp., $16.50

For many years the shaping of electrical signals was almost exclusively the domain of the passive LC filter. Today, this job is being shared among active filters, digital filters, and parametric-frequency converters.

Each of these techniques has been explored extensively during the last five years by engineers at many companies, Government agencies, and universities. Their findings, for the most part, comprise the text of this book.

The author, himself well known in the filter field, has called upon six other experts to contribute chapters on their specialties. William Kerwin of Ames Research Center describes "Active RC Network Synthesis Using Voltage Amplifiers." J.J. Orchard of the Lenkurt Electric Co. offers "Gyrator Circuits" many of which he developed. Graham A. Rigby of University of California at Berkeley presents "Electronic-circuit Aspects of Active Filters." John V. Wait of the University of Arizona at Tucson covers "Digital Filters." B.J. Leon of Purdue University at Lafayette, Ind., describes "Parametric Frequency Converters." Jan A. Narud of Motorola in Phoenix, Ariz., details "Present and Future Trends in Integrated Circuits."

The chapters cover a wide variety of newly developed techniques that can be applied to signal filtering and the processing of signal information.

A detailed introduction aimed at the engineer unfamiliar with the subject precedes topic. The chapters provide design information and a description of current research results. Other topics covered include: active filter sensitivity, distributed network elements used to produce filters; the advantages and disadvantages of combining different filters; a treatment of reconstruction errors in digital filtering; and the design techniques for parameter amplifiers.

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Technical Abstracts

Faster modulation

Optical modulation at gigahertz rates
G. White
Bell Telephone Laboratories
Holmdel, N.J.

A communications system has been developed that transmits and receives optical pulse-code-modulation word patterns at rates of one gigabit per second. The system uses a traveling-wave modulator whose main part is a lithium tantalate rod in a microstrip package. The high bit rate is achieved by multiplexing four channels operating at 250 megabits per second with subnanosecond pulses.

By being mounted in microstrip, the $LiTaO_3$ crystal provides a real driving point impedance for efficient interfacing with the electronic driving circuits. The 10 by 10 mil modulator rod is 400 mils long and acts as a parallel plate transmission line with a 50 ohm characteristic impedance operating in the transverse electric and magnetic mode.

The traveling-wave interaction is obtained between the transverse electric field disturbances of the crystal and the laser's beam polarization states by electrical and optical signals traveling in the same direction along the modulator crystal. Obtaining an essentially real load impedance improves interfacing with high-speed solid state circuitry and reduces the use time of the electro-optic device relative to that of a lumped parameter structure with the same dimensions. In this system, the rise time is 0.365 nanosecond per inch of rod length.

Boff (snap-off) diode spike generators form the high speed pulses in the individual channels. Operating in the shunt mode, these generators produce 10-volt pulses whose base widths are 700 picoseconds. Information is impressed onto the individual channels by inhibiting, or transmitting pulses from these spike generators and by information bearing pulses fed into a high speed AND gate.

Multiplexing of the four channels is accomplished with a Schottky barrier-diode OR gate that is made in a microstrip package. With this gate the parasitic capacitance of the diode can be as low as 2 pF.

The argon laser in the system operates at a single frequency whose wavelength is 496 nanometers and uses etalon tuning. This manner of tuning eliminates mode competition allowing the low voltage beam modulation to be detected with signal-to-noise ratios less than 20 decibels. The use of partial modulation of a continuous wave beam allows low-level modulation without tying the system rate to the frequency separation of the laser's longitudinal modes. Beam power of 30 milliwatts produces intensities of 500 W per centimeter at the diffraction limited waist in the modulator crystal. The use of field annealing allows the $LiTaO_3$ crystal to withstand these power levels.

System losses are dominated by the insertion loss of the modulator crystal—40%. The temperature variations in the modulator crystal, together with the use of etalon tuning, are the prime reasons for system stability on the order of several hours.

Presented at ICC, San Francisco, June 8-10.

Herringbone cable

Woven electronic interconnect systems of the seventies
E.A. Ross
Southern Weaving Co.
Mauldin, S.C.

The same programed weaving systems used to produce textiles is now producing woven flat cables with such special features as accordion folds and controlled impedances. A mixture of wire gages and types can be handled—twisted pairs, shielded wires, and single-conductor wires. The weaving process also can easily produce completed harnesses, where wires leave the bundle to connect to a terminal and then return to the bundle. Other advantages over flat cable with homogeneous insulation are that the woven cable is easier to strip, and it's easier to separate wires—simply by cutting the binder yarn.

Presented at Eastern Electronics Packaging Conference, Massachusetts Institute of Technology, June 8-9.

New Literature

Magnetic components. Pulse Engineering Inc., P.O. Box 12235, San Diego, Calif. 92112, has available a six-page short-form catalog on its miniature magnetic components.
Circle **446** on reader service card.

Programing devices. Sealectro Corp., Mamaroneck, N.Y. 10543. A 12-page quick reference brochure details six programing or data acquisition product lines. **[447]**

Microwave power measurement. PRD Electronics Inc., 1200 Prospect Ave., Westbury, N.Y. 11590. A 12-page application note describes and compares microwave power measurement techniques. **[448]**

Display computer systems. Honeywell Computer Control Division, Old Connecticut Path, Framingham, Mass. 01701, offers a color brochure describing several ways that its series 16 computers are communicating with graphic display terminals. **[449]**

Reed switches. Hamlin Inc., Lake and Grove Sts., Lake Mills, Wis. 53551, has released a 12-page, illustrated guide to selection and application of reed switches. **[450]**

Housed instrument torquers. Clifton Division, Litton Precision Products Inc., Marple at Broadway, Clifton Heights, Pa. 19018. A four-color bulletin features new housed instrument torquers which can integrally incorporate various feedback elements. **[451]**

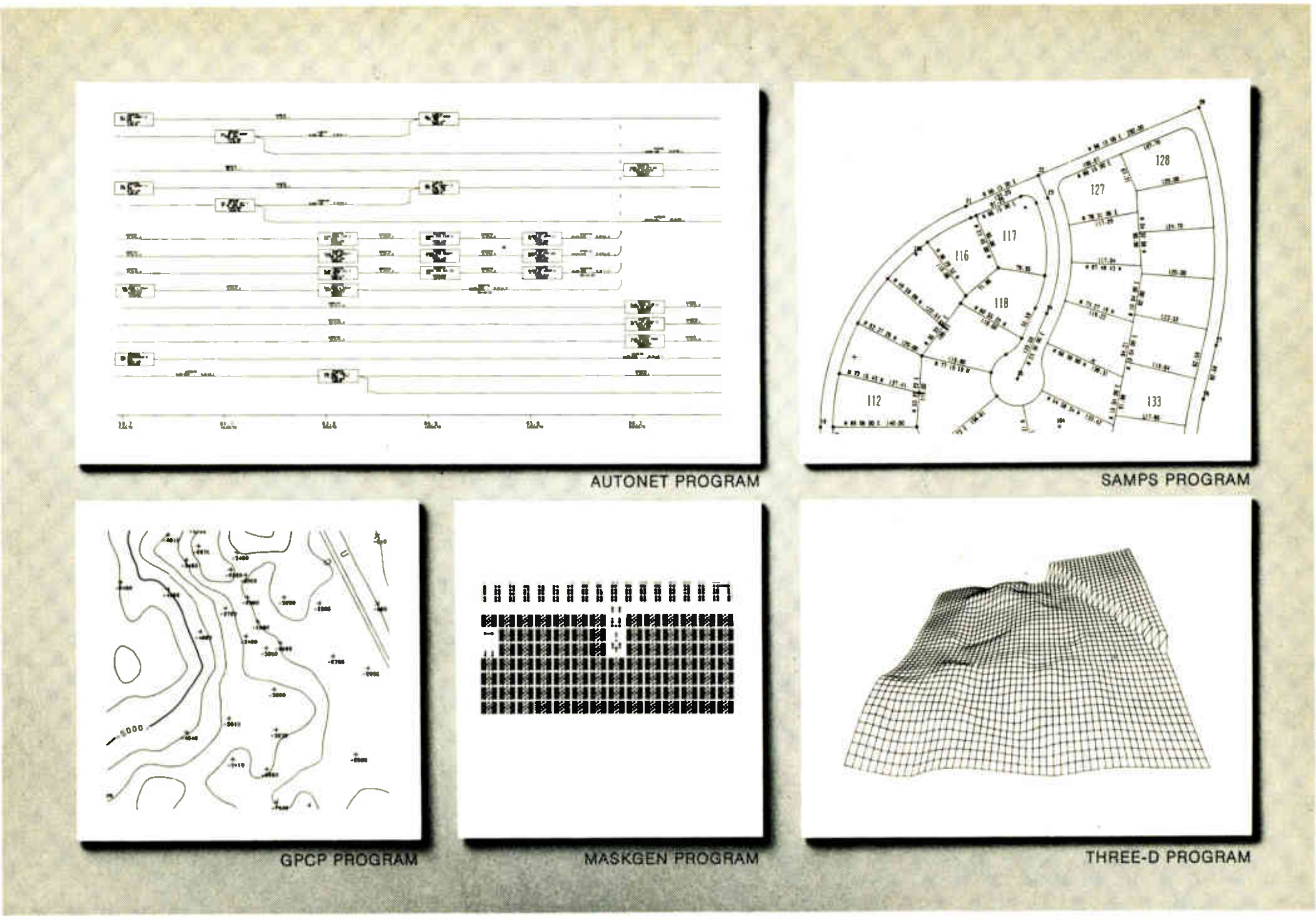
Thick-film hybrid ICs. Circa Tran Inc., P.O. Box 832, Wheaton, Ill. 60187. How thick-film hybrid ICs can be built economically is described in a single-page bulletin. **[452]**

Anechoic chambers. Eckel Industries Inc., 155 Fawcett St., Cambridge, Mass. 02138. Brochure 70031 details the use of echo-free enclosures for acoustic testing and research. **[453]**

Timing motors. A.W. Haydon Co., 232 North Elm St., Waterbury, Conn. 06720. Two-page bulletin CM801-R1 spotlights 60 or 50 Hz commercial industrial timing motors for 6, 12, 24, 115 or 230 V ac operation. **[454]**

Keyboard key modules. Cherry Electrical Products Corp., 3600 Sunset Ave., Waukegan, Ill. 60085. Electronic data entry keyboard key modules, human engineered for the sound and feel of typewriter keys, are described in specifications bulletin KM-201. **[455]**

Ceramic chip capacitors. Monolithic Dielectrics Inc., P.O. Box 647, Burbank, Calif. 91503, offers a six-page technical bulletin on monolithic ceramic chip capacitors. **[456]**



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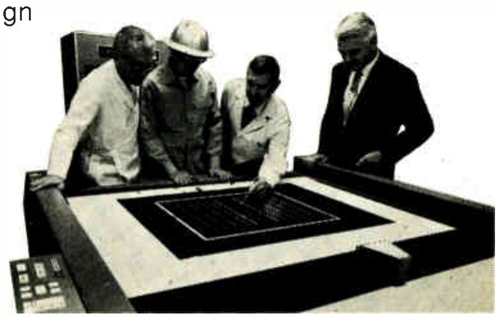


International Newsletter

October 12, 1970

AEG-Telefunken and Hitachi to trade know-how, patents

The Japanese are beginning to challenge Western Europe's color TV makers in their own territory. AEG-Telefunken, which holds patents on the PAL color broadcasting technique used in Western Europe outside France, is not worried, however. To get anywhere, the Japanese are going to have to come to terms with the company to get the all-important licenses. First to make a deal is Hitachi Ltd., which has just signed a know-how and patent cross-license agreement for products including consumer electronics, closed-circuit television, and studio equipment. For its part, AEG-Telefunken has placed its home market off-limits to Hitachi and, while some details are still being held back, may gain access to Hitachi's all-transistor color TV and the one-vidicon color camera patents of Nippon Columbia, an Hitachi affiliate. Also, AEG-Telefunken will get royalties on all PAL sets over 100,000 exported by Hitachi. To appease Japan's Ministry of International Trade and Industry, which must approve the pact, the agreement is nonexclusive. That leaves the door open to other Japanese companies to start lining up for PAL licenses.

French television's third channel to start next year

France is to get its long-awaited third television network next year. It will be state-owned like the other two, and not a commercial channel, as had been proposed [*Electronics,* June 22, p. 184]. The state TV monopoly has budgeted $6 million to be spent next year equipping the new, all-color network. Like France's second channel, it will broadcast a 625-line picture. The first channel still uses an odd-ball 819-line system, which the French have promised to change to the 625-line European standard, though signs are their 1972 target will not be met. "There are just too many TV sets in use that can receive only 819 lines," says a TV network official.

Russians eye technological deals with West Germany

With the Russo-German treaty now signed, it's now up to scientists and economists to embark on a more intensive dialogue toward normalization of Bonn-Moscow relations. Following his 12-day exploratory visit to the Soviet Union, Hans Leussink, West Germany's Minister for Science and Education, let it be known that both sides soon would take concrete steps towards closer cooperation in science and technology. A team of German experts will depart for negotiations in Moscow next month. A similar Russian delegation is expected to visit Bonn early in 1971. High on the agenda are scientific and technical documentation, electrotechnology, data processing, and selected areas in nuclear physics.

Independently, at least one West German electronics firm, Siemens AG, already has made initial contacts with Russian authorities. Siemens men think the contacts may lead eventually to a cooperative deal in computers, most likely in the form of a know-how exchange agreement.

Japanese unveil big computer

Nippon Electric Co. has just rolled out Japan's largest commercial computer, the NEAC series 2200 Model 700. A multiprocessor configuration, composed of two central processors and their associated peripheral equipment, will be delivered by the end of the year to the first buyer, Tohoku University.

Nippon Electric puts the capability of the computer somewhere between IBM's recently announced 370 models 155 and 165. The central processing unit has a memory capacity of 2,097,000 characters and 24 input/output channels. In a multiprocessor system the two central processors can control up to 256 peripheral units. **Look-ahead control allows fixed decimal point addition in 0.5 microseconds and floating point addition in 0.8 μs.**

All-Swedish air defense system . . .

Worried about maintaining a strong yet independent technological stance, Swedish groups are pushing for a number of all-Swedish military and space projects. For one, an entirely Swedish designed and built system should form the basis for the nation's air defense system in the 1980s, according to recommendations by a royal commission. The system would require both aircraft and ground-to-air missiles. What's more, the commission recommended that design work start soon on an aircraft to supersede the SAAB-Scania-built Viggen, a Mach-2 all-purpose aircraft. The Viggen is being produced in an attack version, with parliamentary approval of an interceptor version expected soon. **The commission also urged a Swedish ground-to-air missile to replace the British-made Bloodhound now used.**

. . . and expanded space role proposed

The Swedish Board for Technical Development wants Sweden to invest about $64 million over the next five years to develop an all-weather sounding rocket, a satellite to study the ionosphere, and other space works. The investments, the board said, **would bring Swedish space technology up to a level with other industrialized Western European** nations. Part of a Ministry of Industry study on Sweden's future in space, the report will help the ministry make a decision, expected within the next two months, on European projects and a national program.

Now Sweden spends about $1.5 million annually for space activities. Sources in the government say that Sweden will probably increase its European cooperative projects, but unless some down-to-earth technological fallout of a satellite and rocket program can be guaranteed, **the chances are that the government may not go along with the plan.**

Germany earmarks $3.2 billion for aerospace

Continued high government spending is in the offing for West Germany's aircraft and space industries. Now before Parliament is a bill that calls for an outlay of $3.2 billion over the next five years both for military and civil aircraft projects and for space ventures. **As expected, the Defense Ministry is asking for the largest slice of the appropriations pie —$2.52 billion.** Civil aircraft projects will absorb $270 million and space projects about $420 million.

The biggest projects in the military sector include the Multirole Combat Aircraft now being developed jointly with the British and Italians. The German share in this venture is around $550 million. The standout project in the civil aircraft sector is the government-sponsored VFW 614, a short-haul passenger transport now in serial production. Another is the development of the German-French A-300 Airbus, which will take $192 million next year. **The space program will strengthen German participation in international satellite projects, among them the construction of a research satellite and, together with France, the development and construction of the Symphonie communications satellite.**

Combining two methods improves ICs

MOS FETS from Hitachi display the advantages of both ion implantation, silicon gate technologies

Ion implantation and silicon gates are two methods currently being used to improve the characteristics of metal-oxide semiconductor field effect transistors and integrated circuits. A team at the Central Research Laboratory of Hitachi Ltd. feels they can build better ICs by combining the two processes. This work, like much of the other important ion implantation work in Japan today, was carried out with financial support from the Research and Development Corp. of Japan [*Electronics*, March 16, p. 61].

Two approaches to ion-implanted MOS ICs are used in the U.S. One of these approaches, pioneered by the Hughes Aircraft Corp., uses the aluminum gate as a mask for implantation of self-aligned source and drain regions. Actually, the ion implantation only produces small extensions of previously diffused source and drain regions. And so the nominal width of the implanted regions is only slightly wider than the tolerance in positioning the aluminum gate of the transistors.

The other approach is used by Sprague-Mostek, which uses ion implantation in the channel region to lower the threshold voltage or to produce depletion-type rather than the more commonly used enhancement-type transistors.

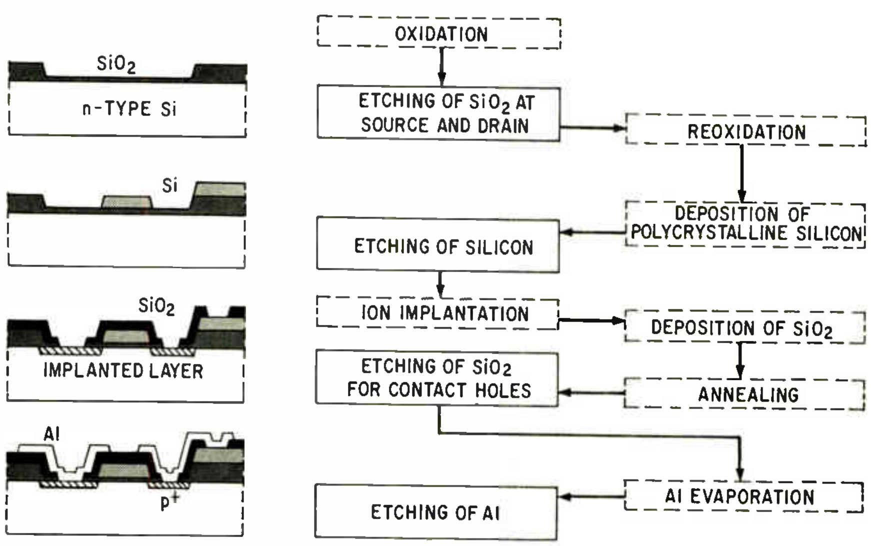
Hitachi's new technique avoids some inherent disadvantages of the Hughes approach. Diffusion and ion implantation in the making of source and drain regions means extra process steps. The aluminum gate prevents annealing of the transistors above about 550°C, where annealing is not complete, giving high sheet resistance in the implanted source and drain regions and excess noise. Despite its advantages, the Sprague-Mostek approach does not give the improvement in switching speeds that result from lower parastic capacitance, a major feature of transistors using a self-aligned fabrication process. This process might, though, be used to produce n-channel devices that switch faster than comparable p-channel ones.

The silicon gate technology pioneered by the Intel Corp. and Fairchild Semiconductor makes possible not only a self-aligned geometry, but also a lower gate threshold voltage because of the lower work function difference of the gate to the substrate compared with that of aluminum. A further advantage of the silicon gate process is high-temperature processing of wafers after gate fabrication.

An experimental memory cell made by Hitachi engineers combines the advantages of both the ion implantation and silicon gate techniques. The Hitachi process starts with oxidation of n-type silicon. The silicon dioxide layer is then etched away at the regions that will become the source, and drain. The cleared regions are reoxidized to a thickness of about 1,000 angstroms.

If channel ion implantation is to

Stepping up. Japanese company's process features self alignment, but avoids aluminum gates, which put a limit on annealing temperatures.



be used for lowering the threshold voltage this would probably be done either after the etching step or after the reoxidation step. This implantation would have no effect on the source and drain regions because an even higher density of the same impurities would later be implanted in these regions. But if some of the MOS transistors were to receive channel ion implantation to convert them to depletion types, the channels of transistors to remain enhancement types would have to be masked during this process, probably by thick oxide.

Next a layer of polycrystalline silicon heavily doped with boron is deposited at about 800°C from SiH_4 and B_2H_6 with H_2 as the carrier gas. Resistivity of the polycrystalline silicon is about 2×10^{-3} ohm-centimeters. Polycrystalline silicon is etched away except where required as gates or as a cross-under connector. Boron ions with an energy of about 100,000 electron-volts are then implanted in the source and drain regions at room temperature to a concentration of about 1×10^{15} per square centimeter. Chemical vapor deposition of silicon oxide follows.

The wafers are annealed at 900°C for 10 minutes. Then the silicon dioxide is etched for contact holes, aluminum is evaporated over the entire surface, and the aluminum is etched for interconnections.

For MOS transistors fabricated on 1-0-0 silicon, threshold voltages are about 1 volt. For a silicon dioxide thickness of about 8,000 Å in regions other than under the gate, the threshold voltage of parasitic MOS transistors is about 15 V. The sheet resistance of the implanted layer is about 100 ohms per square, about an order of magnitude lower than for units annealed at 550°C. Threshold voltage and hole mobility of the units annealed at the higher temperature are identical with units annealed at temperatures as low as 400°C. Yet low frequency noise characteristics, compared with those of units fabricated by diffusion, are two thirds that of units annealed at 550°C.

France

Computer for the lycee teaches computing classes

Philips turned up with a $3,000 minicomputer. International Business Machines was on hand with its new 370 series. Then there were Honeywell-Bull, Univac, Italy's Olivetti, West Germany's Siemens, Britain's ICL, and all the others. With such a lineup at the annaul Paris Sicob office machines and computers show, it's hard to imagine there are chinks in the spectrum of data processing machines on the French market.

Electronique Marcel Dassault, though, thinks it's spotted a gap and has moved fast to fill it. EMD unveiled at the show a minicomputer that's designed mainly to give students at the lycée, the American equivalent of junior high and high school, their first fling with computers. Although the new minicomputer can be programed to teach subjects like math and grammar, its main purpose is to develop students' skills in carrying on dialogues with computers through a terminal. So EMD envisions that students will try their hand at simplified models of real-life data-processing problems, such as checking out business decisions or studying auto traffic at nightmarish intersections like Paris' Etoile, where 11 major avenues merge in a ring surrounding the Arc de Triomphe.

EMD calls its teaching computer by the acronym Esope, which, not coincidentally, is the French name for the Greek story-teller Aesop. The system is based on a minicomputer, the EMD 7000, and can handle up to 64 terminals, although EMD executive Jean Louis Michel figures that 10 terminals would be the typical lycée installation.

In performance, Michel says, the 7000 compares with the Sigma 2 of Xerox Data Systems. The French computer's characteristics: 131 instructions, a memory cycle of 0.95 microseconds, an add time of 2 μs, multiplication time of 8 μs, and a basic memory of 4 kilowords of 16 bits each, expandable to 16 kilowords. Although run of the mill in calculating speed and memory-cycle time, the machine has a multiplexed input-output channel that needs no program control.

This channel interrogates each terminal in sequence, sending oı receiving one seven-bit character to a terminal at a time. The cycle rate is 1 μs/bit. In addition to the multiplex channel, which is controlled by hardware, there are a programed channel and a channel for direct access to the memory.

So far EMD has no firm orders for Esope. But Michel has high hopes. The market could run to 100 systems during the next five years, he figures, and at the moment no other company in France has quite the same equipment. And Michel thinks the price is right—between $37,000 and $55,000—for a system with 10 or so terminals. That works out to a cost per student of $11 a year, equivalent to two or three textbooks, Michel points out, given a five-year amortization for a 10-terminal system installed in a 1,000-student school with each student getting 15 hours of terminal use each year.

West Germany

Op amps aim at consumer product jobs

As far as West Germany's Siemens AG is concerned, operational amplifiers are good for many more uses than their present applications, which are primarily in automatic control equipment and in analog computer systems.

Because they can be integrated easily and are well suited as low-drift dc amplifiers or as boosters for frequencies up to 30 kilohertz, op amps can find jobs in automotive electronic systems, in low-frequency devices and in such consumer products as washing machines, refrigerators and in air-conditioners, the company feels.

A new integrated op amp from

Siemens has been developed for just such uses. Designated the TAA 861, the new device is now beginning to hit the market. To make the circuit attractive for widespread consumer applications, versatility and cost-savings considerations have been prime factors in its design. The TAA 861 uses only six resistors and eight transistors—much less than other IC op amps built so far—all packed on a 1-by-1-millimeter chip. It sells for between 75 cents and $1.

Despite its small number of components, the TAA 861, Siemens says, has the characteristics of the standard 709 class of op amps developed in the U.S. On top of that it has some significant advantages. One is the circuit's large common-mode range. Since this range is almost as wide as the supply voltage range, the possibility of latch-up is practically eliminated. Furthermore, its supply voltage can be as low as ±2 volts, and this allows the device to operate off batteries. Also, to achieve circuit stability through frequency compensation, all that's needed is a single external capacitor. Still another extra is the circuit's relatively high output current, which can drive relays and voltage regulators directly.

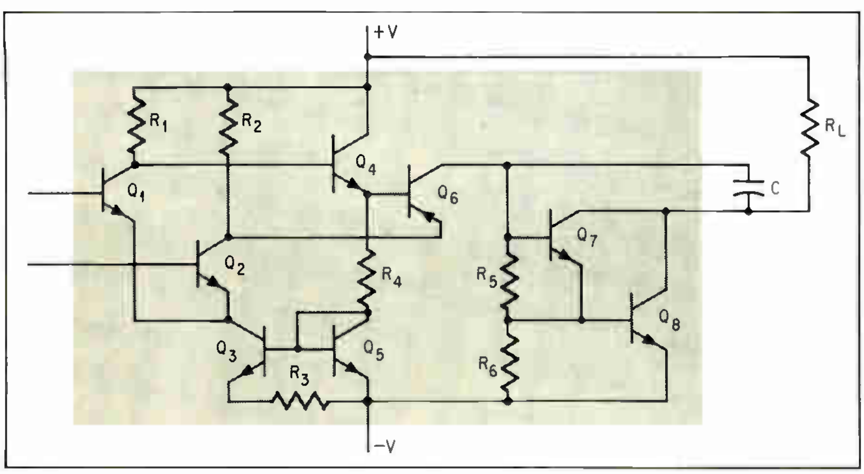
The first stage, made up of transistors, Q1 and Q2, is a difference amplifier. The output stage, comprising Q7 and Q8, is a single-ended amplifier in a Darlington configuration. To keep the sum currents of the difference amplifier constant, a transistor—Q3—is used instead of a resistor. This also holds the dc voltage fall-off in the circuit to a small value at high dynamic resistances. Furthermore, an integrated transistor requires less space than a resistor.

Transistor Q5 supplies the reference voltage—about 700 millivolts—for Q3, the constant current source for the difference amplifier. These two transistors, together with emitter follower Q4, form a control loop which stabilizes the circuit's operating points. The pnp transistor Q6 is used to transfer the potential from the input to the output.

To limit second stage drift, the gain of the first stage must be as high as possible. This is insured by the manner in which Q6 couples the two stages. The same signal appears between its emitter and base as is present between the collectors of the input transistors Q1 and Q2. The whole signal swing produced by the first stage can be used for amplification, and since resistor R5 is large, gain is high.

This high gain and the high impedance at the base of Q7, eases frequency compensation. A single external capacitor causes the frequency response curve to fall off at a constant 6 decibels per octave. The compensating capacitor is not integrated because at 45 picofarads it takes up too much chip space.

Situation wanted. Aimed at consumer markets, Siemens' new op amp has wide common-mode range and output current high enough to drive relays directly.



JAPAN

Low-dislocation process promises low-noise devices

Toshiba engineers have found a way to reduce noise in transistors and integrated circuits. They start with extremely high quality substrates—with fewer than 500 dislocations per square centimeter—and make sure no dislocations are introduced during device fabrication. By comparison, ordinary wafers have several thousand to more than 10,000 dislocations per cm^2.

Another advantage of the process—and one that may be even more crucial to its successor or failure—is that, according to Toshiba, it does not infringe on Fairchild's planar patents in Japan: Toshiba company engineers call their discovery PCT, for perfect crystal technology.

In conventional processes, the extremely high surface concentrations of dopants prior to diffusing and the thick glass on the surface of the wafer multiply the number of disloactions in the active regions of the wafer. The latter does so because it has a different temperature coefficient of expansion than silicon. The former does so because the lattice size of commonly used dopants like phosphorus and boron differs from that of silicon. High concentrations may also cause abnormal precipitation of dopants.

The PCT process is based on low temperature deposition of doped glass, followed by high temperature diffusion from the glass into the crystal. Since the glass acts as a source of dopants, it is never necessary to have a very high concentration of dopants on the surface.

For regions that require relatively high densities of impurities, such as the emitters of transistors and the buried collector layer in ICs, two dopants are used. A small amount of arsenic is added to phosphorus. The theory is that the phosphorus atom may cause dislocations because it is small compared with silicon, and a few of the larger arsenic atoms compensate in some way to prevent dislocations. The use of another two-element dopant containing boron and a small amount of arsenic prevents defects in emitters of pnp transistors, although the arsenic makes a bit more boron necessary.

Aside from lower noise, there are other advantages to this process. Because dislocations are not generated in the PCT process, the part of the base under the emitter is not driven further into the wafer during theemitter diffusion. And, because the buried layer under the collector does not cause dislocations in the substrate, it is possible to grow dislocation-free epitaxial material over the buried layer.

Moreover, Toshiba also anticipates higher yields. One engineer says that with present processes devices must be designed with sufficient margin to offset the effects of dislocations and other crystal imperfections—a margin that can now be traded for higher yield. The new process should also permit development of improved devices for operation at high frequencies, high switching speeds, and high voltages, and Toshiba intends to use it for high-voltage devices such as silicon controlled rectifiers.

The use of an "island" rather than a mask diffusion process for the base of the transistor differentiates the new method from Fairchild's planar patents. A thin boron-doped oxide is deposited over the entire surface of the wafer, and then removed by a photomasking process from all regions except over the base; a thin layer of oxide is next grown over the entire wafer; and the temperature is raised to diffuse boron from the doped oxide into the wafer to form the transistor base. Toshiba points out that the initial oxide layer is mostly removed and, where it does remain, is used as a source of dopants rather than as a mask in the planar process.

The company claims that it can now make integrated circuits with lower noise than the best low noise transistors it could previously make, and discrete transistors with still lower noise. Two transistors and two integrated circuits using this process have been developed. Sales of the first of these devices will start this month, and all four will be ready by early next year.

Diagram reading robot figures out assembly steps

Hitachi has given eyes and a hand to a computer, producing a somewhat intelligent decision-making robot. Reading an assembly diagram and figuring out how to assemble components in accordance with the diagram are among the feats in the robot's repertoire. The Hitachi visual image processing robot Mark-1, a prototype for R&D work on commercial units, was built in the company's Central Research Laboratory.

The robot has two vidicon cameras for eyes. One reads a three-view drawing and, in conjunction with computer programs, recognizes the overall spatial configuration of the object shown in the drawing, as well as the number and shape of the components that make up the object. What's more, the programs enable the robot to recognize not only the way these components are assembled to make up the drawing, but also the order of assembly.

The second vidicon views the components and, with the aid of computer control, is able to recognize their shape, size, position, and attitude—and determine which are needed to assemble the completed object and which should be ignored. Then the computer determines how the components must be transposed and rotated to bring them together correctly.

The Hitachi robot is equipped with handling facilities, including an articulated hand, that is operated by electrical servos, and a handling control unit. The hand has seven degrees of motion: translation along three axes, rotation about three axes, and gripping. The viewing and handling sections are connected to a Hitac 7250 control computer, which has 32 kilowords of core memory and 384 kilowords of drum memory.

The cameras operate at 60 frames per second, and 240 effective lines per frame. Each line is divided on a time basis into 320 picture elements, which gives a total of 76,800 picture elements in a frame. Each picture element is digitally coded with five bits, which give 32 brightness levels.

Software provides three levels of precision. Initially the entire field is scanned to detect the presence or absence of objects and their position. Then the effective window is reduced to single out an object, so that its shape and attitude is picked up in more detail. For study purposes, the computer can set an arbitrary clipping point at which to divide the image into two brightness levels, a method which converts images into outline drawings. But the ordinary method of finding the outlines is more complex, including searches for individual edges. If there is noise in the image the same edge may be represented by several crossing lines with an angle of only several degrees between them, or corners may not coincide. If so, the computer performs further processing to make the outline agree with shape expected from the drawing.

Even if dotted lines are omitted the views, the computer can fill in the missing information. However, the robot is blind to curves. In general, multifaceted objects of the type that can be fabricated on milling machines and have up to eight surfaces can be recognized.

The software used in this robot represents a big advance in the techniques for processing information on objects, which has been considered very difficult. An important step forward is the method of describing and entering into computer memory the relationships between objects. This capability should ease the way to pattern recognition computers and toward artificial eyes for industrial use. The next generation of machines might, for example, be able to spot such things as scratches, soiling and cracks.

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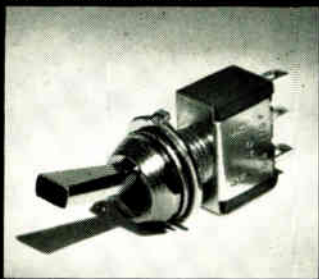

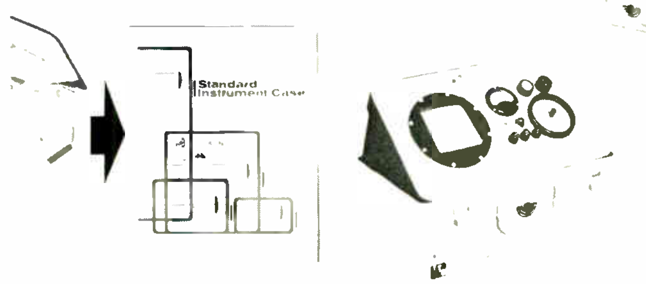
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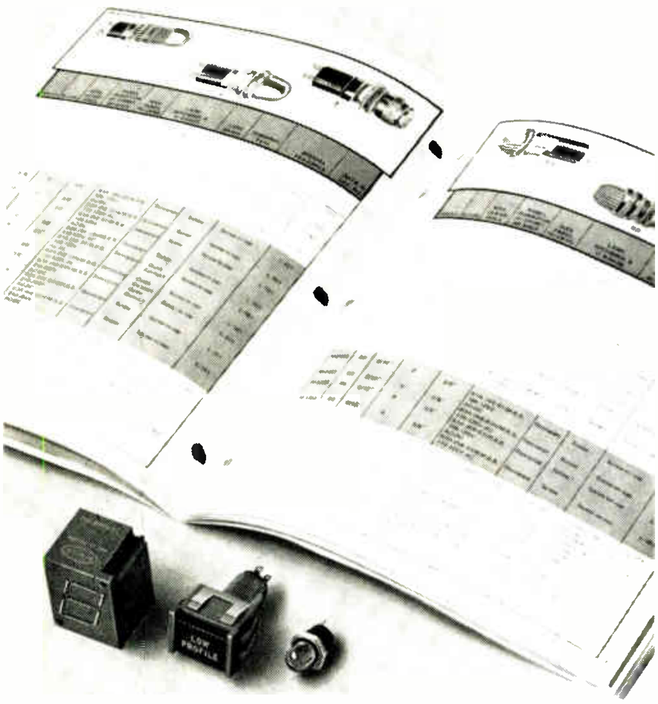

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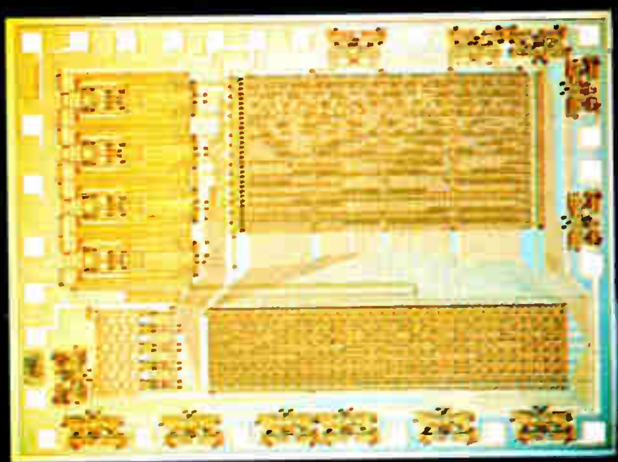

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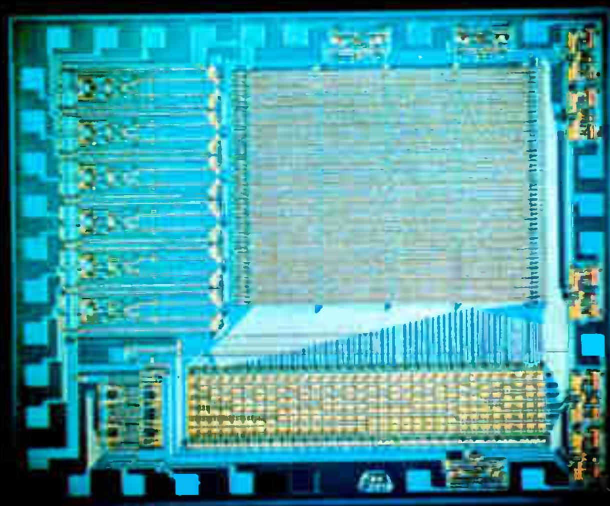

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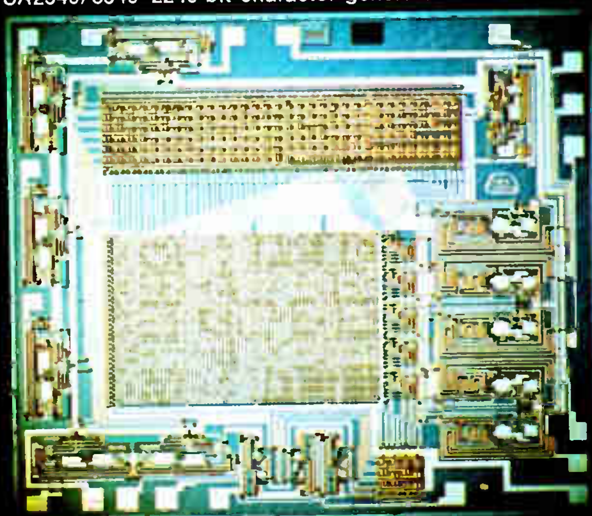

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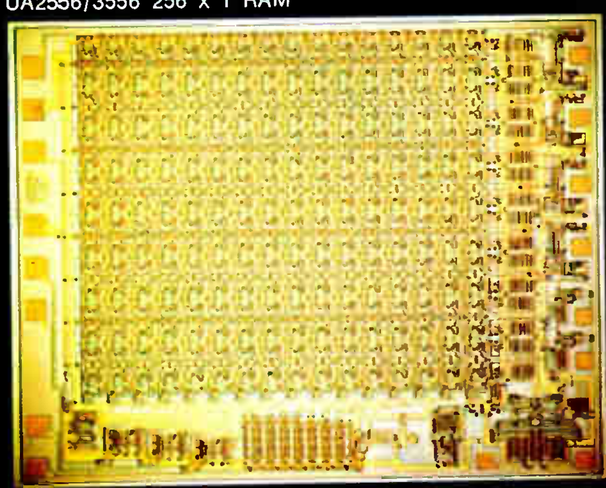

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