VHF
COMMUNICATIONS

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Measuring with a PC

Contents

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NOAA HRPT Receiver

The reception of weather satellite images always attracts lots of interest among radio amateurs. Of course, after the initial experiments one always wants to improve the results, trying to obtain even better pictures with less noise, better contrast and better geometrical resolution. The current receiver technology allows us to quickly reach the limits imposed by the satellite sensors and picture transmission standards.

1.
RECEPTION OF NOAA HRPT IMAGES

Almost everyone starts by receiving the simple APT/WEFAX analogue picture transmissions. After perfecting the APT/ WEFAX receiver, the next logical step is to switch to digital transmissions. Most weather satellites offer an improved signal-to-noise ratio and an im-

proved geometrical resolution on their digital picture transmissions.

The main drawback of the digital picture transmissions is that they are much less standardised than the simple APT/WE-FAX transmissions. Almost every satellite is using a different image data format, that requires different hardware for reception. In addition, the digital transmissions usually require a larger antenna operating on higher frequencies, making the ground station much more expensive.

The most popular digital image format is certainly the NOAA HRPT format, which has been used since the launch of the TIROS-N satellite in 1978. The NOAA HRPT format offers an improved geometrical resolution of 1km and an excellent signal-to-noise ratio (10-bit quantization) when compared to the analogue APT format with 4km resolution originating from the same satellites of the NOAA series (1), (2), (3). The same data transmission standard is still used today by many weather satellites (5), (6).
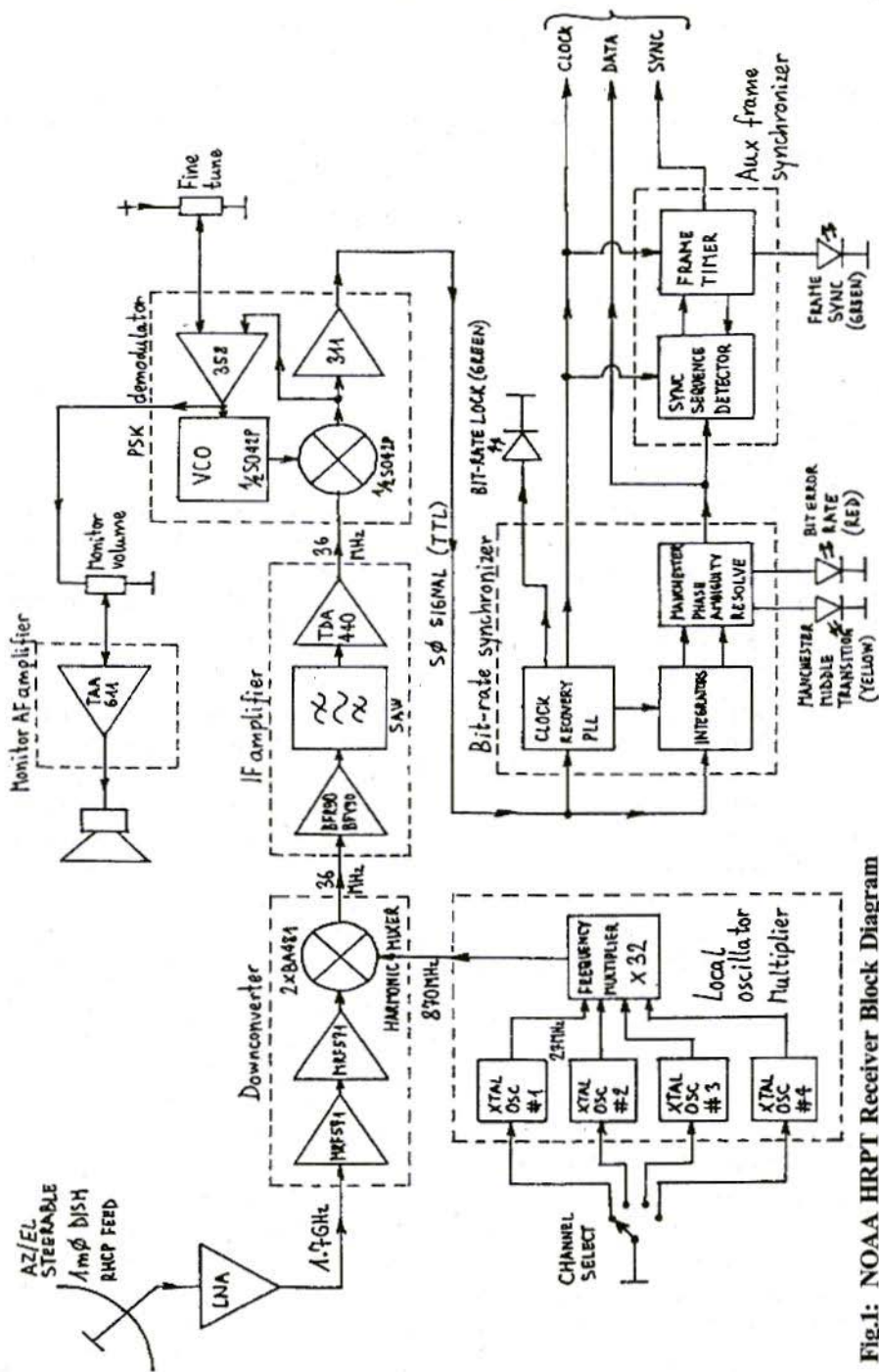
Fig.1: NOAA HRPT Receiver Block Diagram

At the beginning, NOAA HRPT reception was a rather difficult technology for radio amateurs. The first amateur experiments (4) required hand-steering of the antenna and immediate conversion of the digital data into an easier-to-handle analogue APT-like format. There were no suitable computers available and microwave semiconductors were very expensive (the first GaAsFETs like the famous CFY11 were priced over £80 each).

Today the situation is completely different. Inexpensive computers can be used both for antenna tracking and for image storage and display. Parabolic dishes of various sizes and AZ/EL antenna positioners are easily available too. Microwave components became inexpensive as well and top performance low-noise preamplifiers can be readily built (7).

The only missing part is a suitable receiver to process the NOAA HRPT RF signal and output the data in a suitable format to a computer. Such a receiver will be described in this article, based on a design that has been operating for more than five years in the author's receiving station and has been successfully duplicated by many other radio amateurs as well.

2.
NOAA HRPT RECEIVER BLOCK DIAGRAM

The general block diagram of the NOAA HRPT receiver is shown on figure 1. Using a state-of-the-art LNA

(7), a 1m diameter dish antenna with a RHCP feed will provide an error-free reception at elevations above 10 degrees. Of course, the antenna needs to be installed on a computer-controlled AZ/EL rotator to track the quickly-moving polar-orbiting NOAA satellites.

A similar antenna/feed/LNA combination for the reception of amateur satellites in the 2.4GHz band has been described in (8). The latter can be easily scaled to the lower frequency band of 1.7GHz. Since the helical feed described and the LNA are both wideband, even the original 2.4GHz version actually operates in an excellent way at 1.7GHz as well, making it possible to use one antenna and one LNA for both weather satellites at 1.7GHz and amateur radio satellites at 2.4GHz.

To receive NOAA HRPT transmissions, most amateurs usually use different downconverters and IF strips. Such designs tend to be unnecessarily complex and the overall receiver performance is poor due to the unsuitable hardware. Therefore it was decided to develop a completely new design to avoid such problems.

The circuit shown in Fig. 1 is a single conversion receiver with an IF of 36 MHz. The latter is a convenient choice since widely-available television receiver SAW filters have just the appropriate bandwidth for the NOAA HRPT signals as well. Since 36 MHz is a relatively low value when compared to the input frequency in the 1.7 GHz range, the downconverter needs to be designed carefully. On the other hand such a design is still simpler than a double or even multiple conversion receiver.
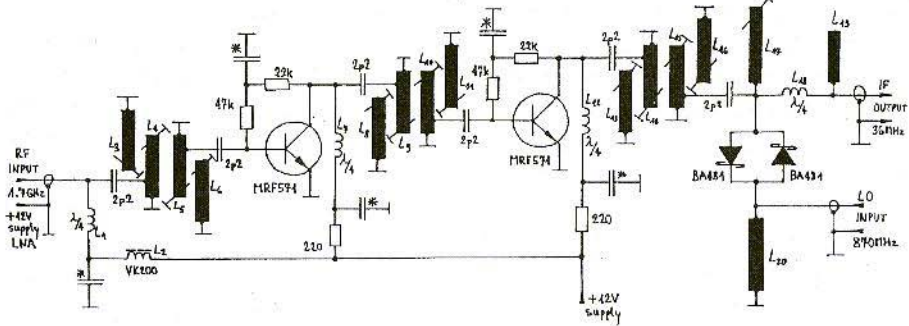
Fig.2: NOAA HRPT Receiver Downconverter

Besides the choice of the IF frequency one also has to consider the required demodulator(s). The demodulation of a NOAA HRPT signal can be split into three different steps.

In the first step, a digital ·signal is obtained from the modulated RF carrier in a PSK demodulator. The second step involves bit-rate synchronisation and bit conditioning. Finally, the third step is the frame synchronisation. All three demodulation steps are included in the described receiver that provides a serial data stream, a bit clock and frame pulses as its output. These signals are usually required by the computer interfaces used. However, if a computer interface already includes the frame synchronisation or even the bit-rate synchronisation, the corresponding circuits can simply be omitted.

A matching HRPT interface to the "DSP computer" was presented in (11). Of course, there are many different interfaces available for the "IBM PC compatible" computer family. Finally, one can also feed the digital data to a D/A converter and convert the signal to a 2400 Hz amplitude-modulated subcar-

rier, but in this way both the signal-to-noise ratio and the geometrical resolution of the images are degraded.

3.
NOAA HRPT DOWNCONVERTER

The circuit diagram of the NOAA HRPT downconverter is shown in figure 2. Since the downconverter is included in the indoor receiver, it is supposed that an external LNA with a gain of 25-30dB is used all of the times. Therefore the downconverter is not optimised for the best noise figure. At 1.7 GHz one has to consider the cable loss between the LNA and the indoor receiver. At a typical distance of about 25m it is easy to keep the cable loss below 10dB, for instance by using the low-loss coax cables developed for satellite TV IF. Of course the circuit of the downconverter includes the supply network for the LNA that provides +12Vdc on the RF input connector.

The downconverter includes two RF amplifier stages (two MRF571s) and a harmonic mixer with two BA481 Schottky diodes. Due to the low IF of only 36 MHz, filtering the image frequency, just 72 MHz above the desired frequency, is not easy. Since high-Q resonators can not be built in microstrip technology, the downconverter is using band-reject filters to attenuate the unwanted image response.

The downconverter includes three almost identical filters, each consisting of four microstrip resonators. The two inner microstrip resonators (for example L4 and L5 in the first filter) operate as a rather wide band-pass filter with the bandwidth in the range of 200 MHz. Of course L4 and L5 alone are not able to provide any significant attenuation of the image frequency.

The two outer resonators (for example L3 and L6 in the first filter) operate as absorption traps for the image frequency, 72 MHz above the desired reception frequency.
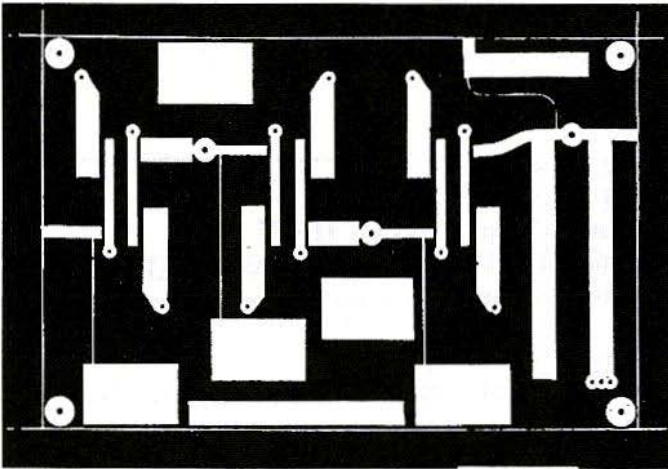
Fig.3:
NOAA HRPT
Receiver Downconverter, upper side
(top view)
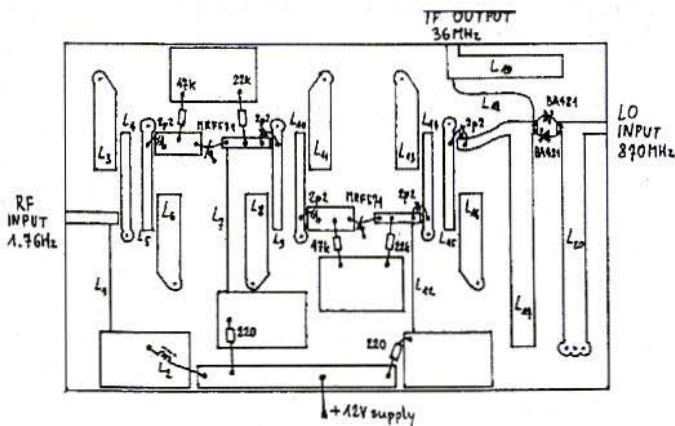
Fig.4:   NOAA HRPT Receiver Downconverter, Component Overlay
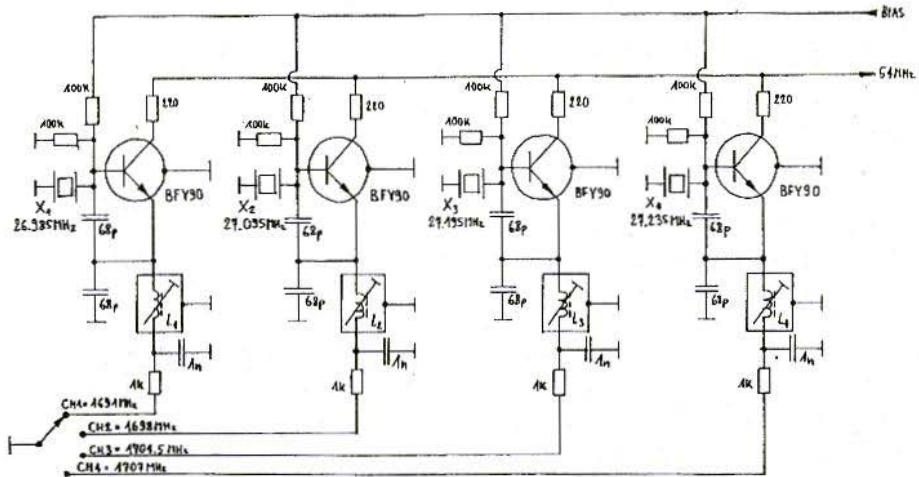
Fig.5:   NOAA HRPT Receiver Local Oscillator

The overall combination is a band-pass/band-reject filter. Three such filters provide more than 40dB attenuation of the unwanted image frequency. The main purpose of the two RF amplifier stages is to compensate for the loss in these filters.

The mixer uses two antiparallel Schottky diodes (BA481) and requires a local oscillator signal at half the conversion frequency (around 870 MHz). The main drawback of this simple circuit is a higher noise figure, usually around 15dB.

The downconverter is built as a micros-trip circuit on a double-sided FR4 glassfibre-epoxy printed-circuit board with the dimensions of 80mm x 125mm. The upper side is shown in figure 3, the lower side is not etched. The component location is shown in figure 4. The construction of similar microstrip circuits has been widely discussed in (9) and (10).

An adjustable-frequency signal source is required for the correct alignment of the image frequency traps. In practice, L3, L6, L8, L11, L13 and L16 usually need to be shortened by about 1mm during the alignment procedure.

Other microstrip resonators hardly need any adjustments. L17 may be made slightly longer for the best mixer noise figure. Since the mixer includes two antiparallel diodes, no DC voltage is generated during operation.

The local oscillator chain is therefore adjusted by connecting an ohmmeter to the IF output and tuning the multiplier stages for the minimum resistance. The maximum LO drive may not correspond to the best noise figure, but in this case it is better to have some safety margin on the LO signal level.

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4.
NOAA HRPT RECEIVER LOCAL OSCILLATOR MULTIPLIER

NOAA HRPT transmissions are usually encountered on two different frequencies: 1698.000 MHz and 1707.000 MHz. The 1698.000 MHz channel is usually assigned to the morning/evening satellites while the afternoon/midnight satellites transmit on 1707.000 MHz. All NOAA satellites carry onboard three 1.7 GHz transmitters and in addition may transmit HRPT signals on 1702.500 MHz in the case of failure of both primary transmitters.

However, the transmitter on 1702.500 MHz is connected to a LHCP antenna and requires a polarisation switching capability at the ground station. Maybe this is the main reason why the 1702.500 MHz transmitter has never been used for HRPT transmissions although it has been used for other data transmissions. A NOAA HRPT receiving station therefore only requires two channels, 1698.000 MHz and 1707.000 MHz, both with RHCP antenna polarisation.

Other satellites may transmit on different frequencies. For example, the Chinese FENG-YUN satellites were transmitting fully NOAA HRPT compatible images on 1695.500 MHz and 1704.500 MHz. Although this receiver is not suitable for the digital transmissions originating from geostationary weather satellites, due to the different data rates and modulation techniques, it is nevertheless useful to have the reception

Fig.6: NOAA HRPT Receiver Multiplier

capability of at least the main WEFAX channel at 1691.000 MHz. The reception of the latter is convenient for antenna rotator calibration and LNA/RF front-end checkout.

Since a NOAA HRPT receiver only needs to be tuned to three or four different frequencies, the local oscillator can be crystal-controlled, followed by a multiplier chain.

The crystal-controlled local oscillator is shown in figure 5. Each crystal has its own oscillator and channel selection is performed by turning on the desired oscillator. The following multiplier chain is shown in figure 6. The overall multiplication factor is 64, but the last frequency doubling is performed by the harmonic mixer itself.

The oscillator transistors are already able to provide the

second harmonic at around 54 MHz. This frequency is then multiplied by four to about 217 MHz, then doubled to 435 MHz and finally doubled to 870 MHz.

The NOAA HRPT receiver local oscillator multiplier is built on a single-sided printed-circuit board with the dimensions of 80mm x 100mm, as shown in figure 7. The corresponding component location is shown in figure 8. L1, L2, L3 and L4 have an inductance of about 1.2uH and their main purpose is to force the crystals to oscillate on the desired third overtone at 27 MHz. In addition these adjustable coils allow some fine

Fig.7:
NOAA HRPT
Receiver Local
Oscillator Multiplier,
bottom view.

Fig.8:
NOAA HRPT
Receiver Local
Oscillator Multiplier
Component Overlay

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Fig.9: NOAA HRPT Receiver IF Amplifier

frequency tuning to compensate for the crystal tolerances. L5 and L6 have about 0.3uH each. In practice L1, L2, L3 and L4 have 10 turns each on a miniature TV IF transformer core while L5 and L6 have 5 turns each on the same type of core.

L7, L8 and L9 are self-supporting coils with three turns of 1mm copper enamelled wire each, closely wound on a

5mm internal diameter. All three coils should have the same orientation to obtain the proper magnetic coupling. L12 is a self-supporting coil with three turns of 0.5mm copper enamelled wire, closely wound on a 3mm internal diameter.

Finally, L10, L11, L13 and L14 are etched on the printed circuit board.

Fig.10: NOAA HRPT Receiver IF Amplifier, bottom view.

Fig.11: NOAA HRPT Receiver IF Amplifier Component Overlay

The oscillators should operate immediately without any alignment. The multiplier chain however requires alignment. The latter should be performed stage by stage by checking the corresponding signal level on the base of the following multiplier transistor. In fact it is enough to check the DC voltages, since the BE junction operates as a rectifier. If the operation of the last multiplier stage is found unstable, the wire leads of the BFY90 transistor should be shortened. If this does not suppress parasitic oscillations, the spacing of the turns of L12 should be modified.

5.
NOAA HRPT RECEIVER IF AMPLIFIER

The NOAA HRPT receiver IF amplifier is shown in figure 9. The design of the IF amplifier is based on the avail-

able 36 MHz SAW filters. The overall bandwidth of NOAA HRPT transmissions is around 3 MHz, so a PAL television receiver SAW filter with a bandwidth of about 4-5 MHz is a very convenient choice. SAW filters have a flat passband and very steep edges, but most important of all they have a flat group delay so that they do not distort fast digital signals.

The remaining circuit of the IF amplifier is also based on available components for television receivers. The first low-noise amplifier stage with the BFR90 transistor is followed by yet another amplifier stage (BFY90) to compensate for the high insertion loss (15-20dB) of the SAW filter. The SAW filter is followed by an integrated IF amplifier TDA440. The latter also includes an AGC circuit.

In addition to the SAW filter, some selectivity is also provided by the tuned circuit with L1. On the other hand, there is a wideband transformer L2 on the output of the TDA440.
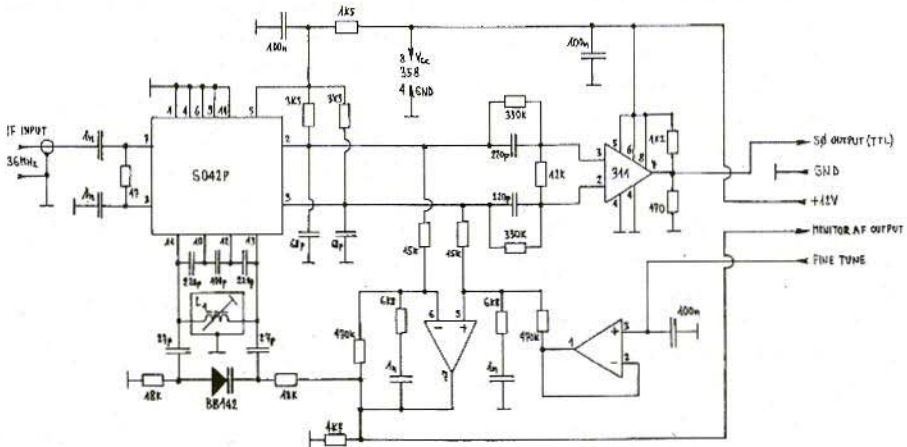

Fig.12: NOAA HRPT Receiver PSK demodulator

The video demodulator inside the TDA440 is not used except for steering the AGC. Although the NOAA HRPT PSK signals can be limited, operating the IF amplifier in the linear region makes the bandwidth of the filters much less critical.

The NOAA HRPT receiver IF amplifier is built on a single-sided printed-circuit board with the dimensions of 40mm x 100mm, as shown in figure 10. The corresponding component location is shown in figure 11.

L1 has about 0.3uH or 5 turns on a miniature TV IF transformer core. L2 is a wideband transformer with the primary inductance of about 2uH and the turns ratio of 5:1, in practice 10 turns and 2 turns on a miniature 10.7 MHz IF transformer core. Of course, L1 needs adjustment while the core of L2 can simply be adjusted for the maximum inductance.

Any 36 MHz SAW filter with a single input and output should be suitable for the IF amplifier. These filters are available in two different packages: TO-8 metal can and plastic single-in-line. The printed-circuit board has holes for both types of packages. A slight offset of the SAW filter centre frequency or local oscillator crystals can always be corrected with L1.

The 10kohm trimmer sets the AGC threshold or the output signal level. Warning! The circuit does not work with some integrated circuits, in particular with the TDA440S. Therefore be careful to obtain a TDA440 without any suffix letters!

6.
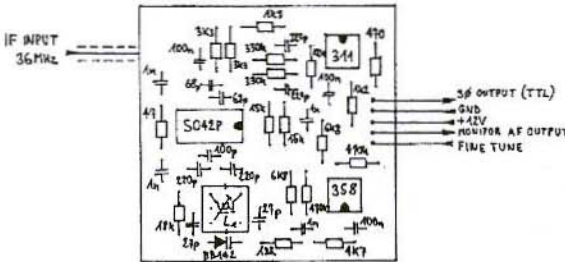# NOAA HRPT RECEIVER PSK DEMODULATOR

The 665.4kbit/s NOAA HRPT serial data stream is first Manchester (split-phase) encoded. The Manchester-encoded signal then modulates the phase of the RF carrier. The phase modulation amounts to +/-67.5 degrees nominally. The RF· spectrum of such a signal includes an unmodulated carrier at the centre frequency and two symmetrical sidebands with the maximum offset +/-655.4 kHz from the centre frequency. The unmodulated carrier level is about 8dB weaker than the overall signal strength. In other words, about 0.7dB of the transmitter power is lost in the residual carrier and the remaining power goes to the information-carrying sidebands.

In spite of the rather wide signal spectrum and power loss in the residual carrier, such a transmission standard was probably selected to keep both the satellite transmitters and the ground station demodulators as simple as possible. A coherent demodulator only requires filtering out the residual carrier, phase-shifting it by 90 degrees and multiplying the regenerated carrier by the raw RF signal. All of these functions can be performed by a single, simple phase-locked loop.

The phase-locked loop NOAA HRPT receiver PSK demodulator is shown in figure 12. The VCO and multiplier are included in the integrated circuit S042P. The same multiplier is used both as the PLL phase detector and as the PSK data demodulator.

Fig.13:
NOAA HRPT Receiver
PSK Demodulator,
bottom view.

Fig.14:
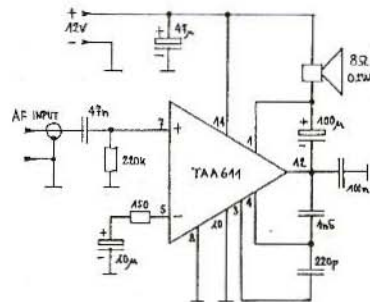NOAA HRPT Receiver
PSK Demodulator
Component Overlay

The PLL loop filter includes a 358 dual Op-amp, while the output data is converted to TTL level by a 311 voltage comparator.

The locking range of the PLL should allow for VCO drift and for the Doppler shift, which amounts to about 100kHz for a polar-orbiting NOAA satellite at 1.7 GHz. From this point of view, the choice of 36 MHz as an intermediate frequency is a fortunate coincidence. Finally, the described PLL PSK demodulator is also an efficient FM demodulator that can be used to receive the analogue WEFAX transmissions from geostationary weather satellites.

The audio-frequency monitor is however mainly intended to check the proper operation of the receiver and detect any interference. The PLL demodulator also includes a fine tuning control. When the latter is set correctly and the demodulator locks on a valid NOAA HRPT

signal, the audio frequency noise simply disappears.

The NOAA HRPT receiver PSK demodulator is built on a single-sided printed-circuit board with the dimensions of 60mmX60mm, as shown in figure 13. The corresponding component location is shown on figure 14. L1 has an inductance of about 0.3uH or 5 turns on a miniature TV IF transformer core.

Fig.15: NOAA HRPT Receiver
Monitor AF Amplifier

The alignment of the PSK demodulator consists in tuning the VCO to the desired frequency. In practice this means setting the inductance of L1 so that locking occurs in the middle of the fine-tune control. The fine tune potentiometer should supply a voltage up to about 9V and this power supply should be well filtered and stabilised. On the other hand, a single-turn potentiometer (100kohm lin) is sufficient for the fine-tune function.

7.
NOAA HRPT RECEIVER MONITOR AF AMPLIFIER

A simple audio-frequency amplifier is required as an AF monitor in a NOAA HRPT receiver. The circuit diagram is shown in figure 15. The TAA611 may be an obsolete type, but it has a low power drain and does not generate much interference to the other circuits.

The single-sided printed-circuit board measures 40mm x 60mm and is shown in figure 16. The corresponding component location is shown in figure 17. A practical value for the volume potentiometer is 100kohm log.

8.
NOAA HRPT RECEIVER BIT-RATE SYNCHRONISER

The PSK demodulator supplies a Manchester-encoded serial data stream at 665.4kbit/s. The main function of the

Fig.16: NOAA HRPT Receiver Monitor AF Amplifier, bottom view.
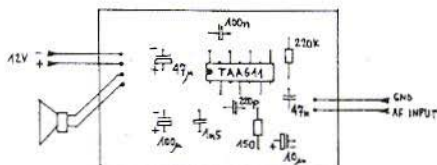
Fig.17: NOAA HRPT Receiver Monitor AF Amplifier Component Overlay

bit-rate synchroniser is bit-clock recovery. In addition, the bit-rate synchroniser also removes the Manchester encoding and supplies the original NRZ data stream.

A Manchester-encoded signal always includes a signal-level transition in the middle of a data bit. Additional signal-level transitions may be present at the beginning and/or end of one bit period. All of these transitions may be used for bit-clock recovery.

The circuit diagram of the NOAA HRPT receiver bit-rate synchroniser is shown in figure 18. The bit clock recovery includes a transition detector with a delay line (74LS164 shift register) and an EXOR gate. The output of the transition detector is fed to a PLL with the VCXO operating at 16 times the bit rate (10.6464MHz). The PLL includes two phase detectors, implemented with EXOR gates. The in-phase

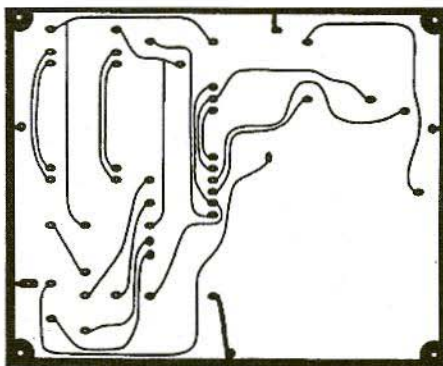Fig.18: NOAH HRPT Receiver Bit-Rate Synschroniser

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detector is used to indicate the lock condition while the quadrature detector feeds the feedback amplifier. The polarity of the obtained 665.4 kHz clock is still ambiguous, since the PLL may lock on the beginning/end transitions or on the middle-bit transitions. An additional circuit is therefore required to resolve the correct clock phase.

The Manchester decoding is performed by a simple EXOR operation between the encoded data and the synchronised, square-wave clock. Since there are two possible clock phases, two identical bit-conditioning circuits are required. The latter use one 74LS161 synchronous counter each as an integrator. Both integrators count for 15 CLK*16 periods and dump the result to a buffer in the 16th CLK*16 period. In addition, the result of the first integrator is intentionally delayed by one-half bit period with an additional buffer to be available at the same time as the result from the second integrator.

The final decision is simple: a count between 0 an 7 indicates a logical zero, while a count between 8 and 15 indicates a logical one. In addition, one can assume that a count between 0 and 3 and between 12 and 15 indicates a "good" bit, while a count between 4 and 11 indicates a corrupted bit. A corrupted bit may be generated by noise, but it may also indicate a wrong clock phase.

Corrupted bits from both bit conditioners are integrated the corresponding RC networks and then fed to the decision circuit with the 339 comparators. The final decision is stored in the RS flip-flop with the two 74LS02 gates. The output of this flip-flop drives the
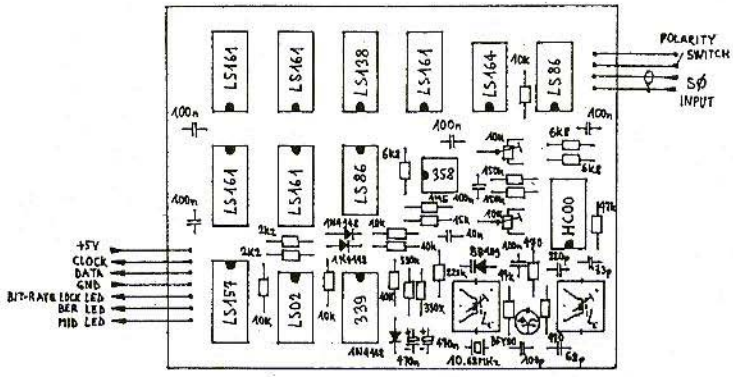

Fig.19: NOAA HRPT Receiver Bit-Rate Synchroniser upper side
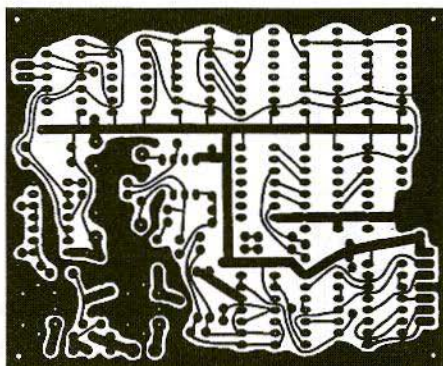
Fig.20: NOAA HRPT Receiver Bit-Rate Synchroniser lower side

74LS157 to select the the bit conditioner driven by the correct clock phase.

The 74LS157 also drives three LEDs. The green LED indicates the bit-rate lock. The yellow LED indicates the missing transitions at the beginning/end of single bits and therefore signals the Manchester mid-bit transitions. Finally, the red LED indicates the missing mid-bit transitions and is an early indication of poor signal quality or increasing bit-error rate.

Fig.21:
NOAA HRPT
Receiver
Bit-Rate
Synchroniser
Component
Overlay

Without a valid input signal or when just noise is present at the receiver input, the green LED is off and both red and yellow LEDs are on. When a signal is applied, the green LED will go on. As the signal strength increases and the signal-to-noise ratio improves, the red LED will slowly go off. The yellow LED should stay on all of the times. If the yellow LED goes off or starts flashing, there is something wrong with the satellite transmission like long sequences of logical ones or zeroes. During normal HRPT reception the yellow LED makes just perceptible intensity variations, synchronised to the 6Hz HRPT frame period.

Since the NOAA HRPT modulation format includes a residual carrier, the polarity of the demodulated data stream is not ambiguous. However, if the RF signal is converted to a different frequency, the polarity of the phase modulation will be reversed if the signal spectrum is reversed in the frequency-conversion process. The bit-rate synchroniser therefore includes a polarity switch right at the input of the circuit. This polarity switch is only needed if the downconversion scheme is changed.

If the bit-rate synchroniser is only used in the described receiver, the above mentioned polarity switch should be left open all of the time!

The NOAA HRPT receiver bit-rate synchroniser is built on a double-sided printed-circuit board with the dimensions of 80mm x 100mm. The upper side is shown in figure 19 while the lower side is shown in figure 20. The corresponding component location is shown in figure 21.

The alignment of the bit-rate synchroniser should start by bringing the VCXO to the desired frequency range with a frequency counter. The VCXO is using a crystal with a higher nominal frequency of about 10.68 MHz, so that the pulling range with the BB109 varicap diode may be made wider with the aid of L1. The exact value of L1 depends on the crystal used and may be as large as 30uH (40 turns on a 10.7 MHz IF transformer core) to pull the crystal down to 10.4646 MHz.

The function of L2 (1.2uH or 10 turns on a TV IF transformer core) is to prevent the oscillator to jump on the overtone crystal resonances.
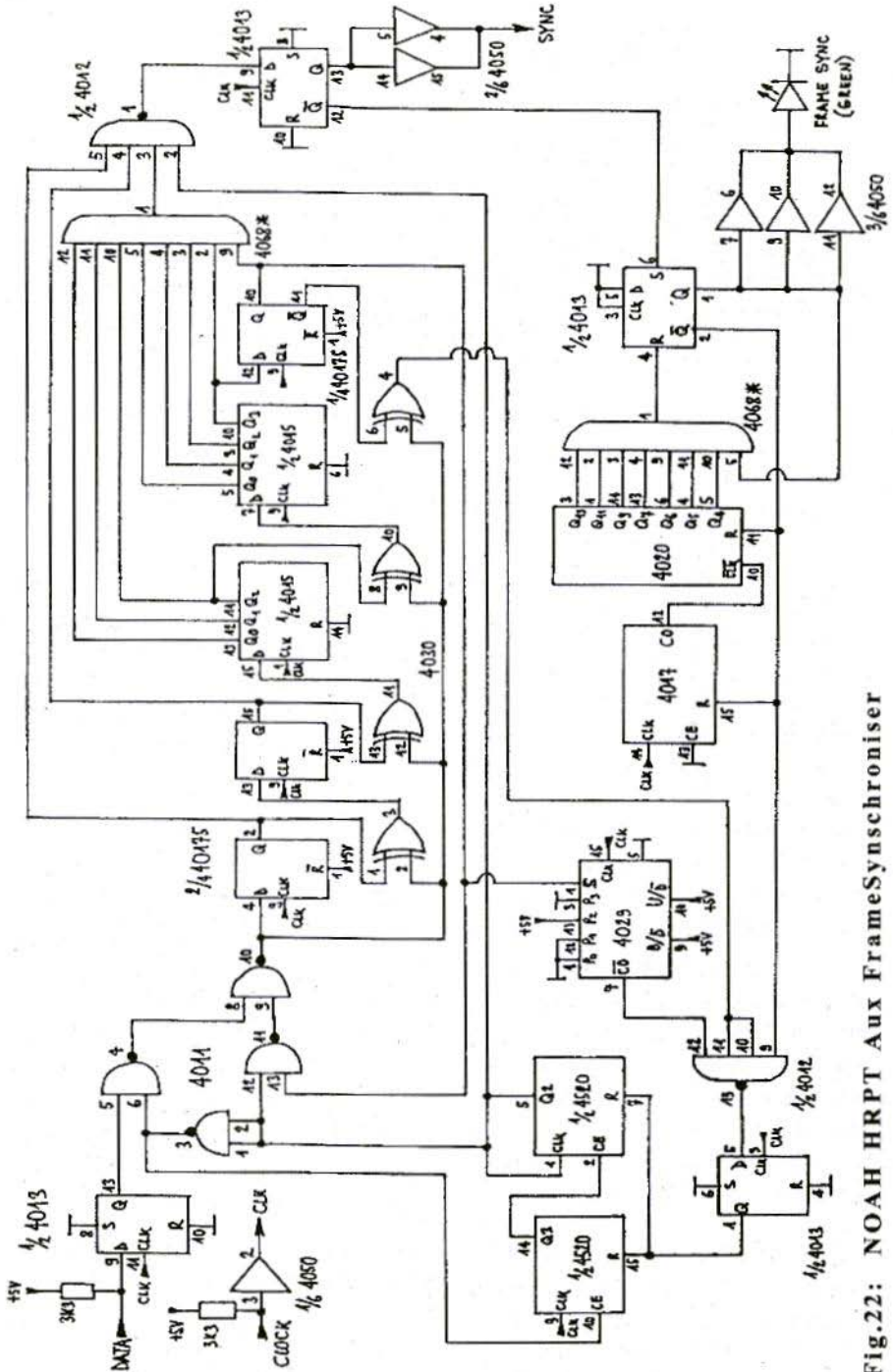
Fig.22: NOAH HRPT Aux FrameSynchroniser

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Without any input signal one should first obtain 2.5V on the varicap diode by the corresponding 10kohm trimmer and then tune L1 for 10.4646 MHz. The bit-rate lock threshold trimmer (10kohm) should be set so that the green LED just goes off. When a valid NOAA HRPT signal is applied and the green LED goes on, one should finally check that the voltage on the varicap diode is close to 2.5V and eventually correct the setting of L1.

9.
NOAA HRPT RECEIVER AUX FRAME SYNCHRONISER

The HRPT transmission includes the data originating from all of the sensors onboard a NOAA satellite (2), (3). The serial data is organised into words and frames. Words are 10 bits long and the MSB is transmitted first. One frame includes 11090 words or 110900 bits so that exactly 6 frames are transmitted in one second at a speed of 665.4kbit/s.

The frame rate is also synchronised to the main radiometer (AVHRR) mirror rotation, so that one frame contains the data of one AVHRR scan line. The AVHRR image data takes most of the frame and consists of 10240 words, starting with word 751 and ending with word 10990. The first five words of the AVHRR data correspond to the first pixel data in five spectral channels. The following five words correspond to the second pixel. Finally, the last five words of AVHRR data correspond to the last, 2048th pixel.
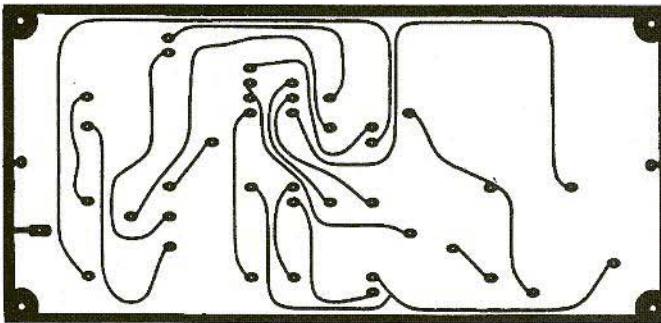
Fig.23:
NOAA HRPT receiver, Aux Frame Synchroniser upper side
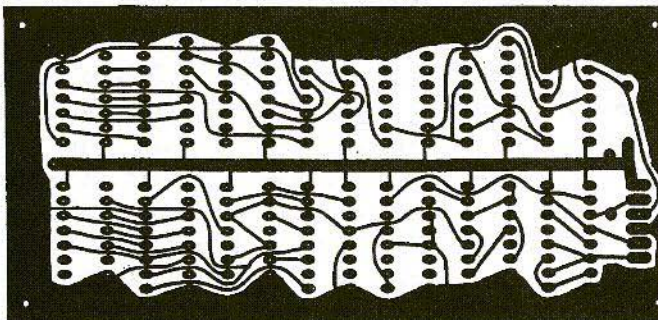
Fig.23:
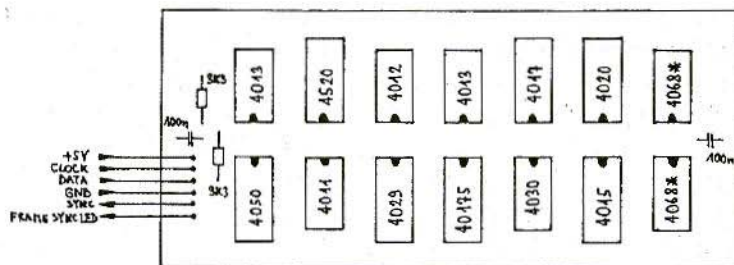NOAA HRPT receiver, Aux Frame Synchroniser lower side

Fig.25: NOAA HRPT Receiver Aux Frame Synchroniser Component Overlay

Frame synchronisation is achieved by detecting known patterns in the frame structure. In the NOAA HRPT frames there are two such patterns: a 6 words (60 bits) long frame sync at the beginning of a frame and a 100 words (1000 bits) long auxiliary frame sync the end of a frame. Both patterns are not arbitrary, but are generated by mathematical algorithms, known as binary polynomial division. Besides interesting mathematical properties, these patterns are also easy to generate with shift registers and EXOR gates.

However, in real receiving conditions, some bits may get corrupted due to a poor signal-to-noise ratio. This is especially true in an amateur receiving station with a small antenna. Of course, bit sync and frame sync should not be lost with moderate bit-error rates. Therefore the frame sync circuit should not just be able to detect the sync pattern but should also tolerate a certain amount of errors in the sync pattern. Simply speaking, the frame synchroniser should lock on a signal even if just an arbitrary part of the sync pattern is received correctly.

The circuit presented in figure 22 is designed to look for the auxiliary sync

pattern in a NOAA HRPT transmission. The auxiliary sync pattern is generated by a 10th degree polynomial (10 stage shift register)

$$X**10+X**5+X**2+X+1.$$

The frame synchroniser includes an identical shift register with an identical EXOR network. The incoming data is fed to the shift register and compared with the locally computed result at the same time. If the two results match, the incoming sequence corresponds to the given polynomial.

If a match is found for 64 consecutive bits, the 4520 counter will signal that frame sync has been achieved. However, the exact position of the detected sync sequence inside the 1000 sync bits is not known yet. Therefore the 4011 gates switch the EXOR network back to the shift register input and the circuit is clocked on until the shift register reaches the all-ones state.

The all-ones event is detected by AND gates and is finally signalled out a valid frame-sync pulse. The frame pulse also triggers a timer (4017 and 4020) that inhibits the aux frame-sync circuits until the next expected aux frame-sync pattern. The timer output also drives the frame-sync LED.
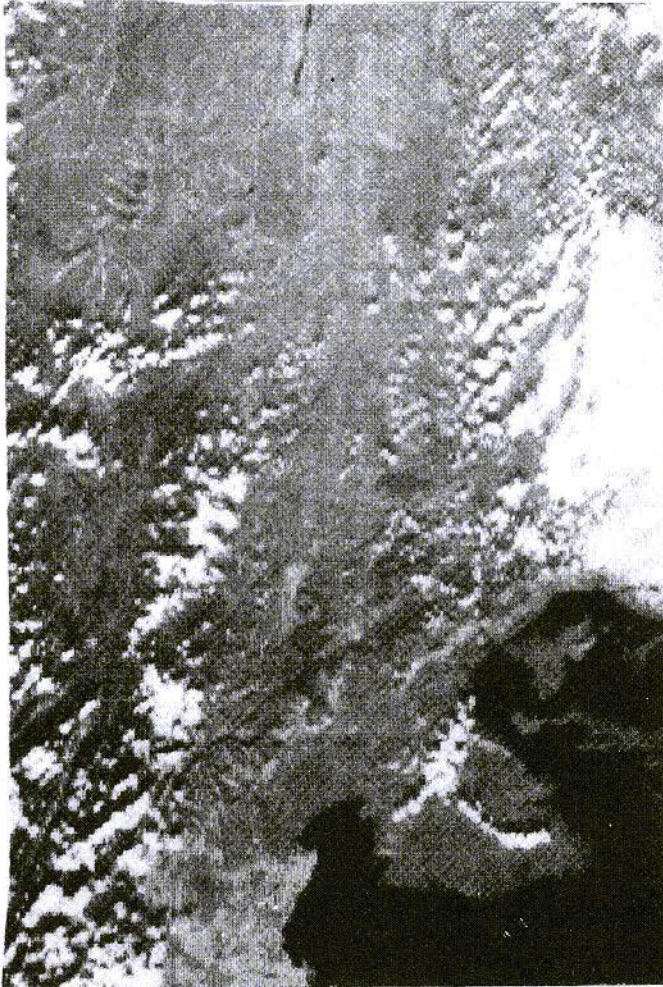
**Fig.26;
NOAA-11 HRPT
Image (VIS2) of
Slovenia and
Neighbouring
Countries (15/08/94)**

The auxiliary sync pattern detector described is also sensitive to a long sequence of zeroes. Since the latter do not represent a valid sync signal, the circuit is inhibited by the 4029 counter as soon as 12 consecutive zeroes are detected. In a valid aux sync pattern there are at most 9 consecutive zeroes, since the 10-stage shift register pattern generator never goes through the all-zeroes state.

The frame synchroniser described checks 64 consecutive bits. Since the shift register needs to be filled with 10 valid sync bits first, a correct reception of 74 sync bits is required to trigger the described frame synchroniser.

These 74 bits may occur anywhere in the available 1000 aux sync bits. Therefore the described frame synchroniser will lock reliably even at bit-error rates as poor as 10^{**-2}.

The NOAA HRPT receiver aux frame synchroniser is built on a double-sided printed-circuit board with the dimensions of 60mm x 120mm. The upper side is shown in figure 23 while the lower side is shown in figure 24. The corresponding component location is shown in figure 25.

Being a completely digital circuit, the described aux frame synchroniser should not require any alignment. It is however necessary to understand its principle of operation in the case when troubleshooting is required.

Warning! The circuit includes a "difficult" component: the 4068 AND/NAND gates. These devices should be supplied by the companies RCA or SGS. The 4068 devices from other manufacturers are only NAND gates with the output on pin-13, while pin-1 is not connected. If the latter are used, two additional CMOS inverters are required to perform the AND function on pin-1. 74HC4068 devices were not tested yet, so these may be AND/NAND devices.

10.
NOAA HRPT RECEIVER CONSTRUCTION NOTES

In the above description, the operation and construction of the various parts of the NOAA HRPT receiver was discussed.

When assembling the complete receiver, one should however notice that the overall gain is rather large and the

signal levels range from the noise floor up to TTL levels. To avoid harmful interaction it is recommended that the downconverter, local oscillator multiplier and IF amplifier are located in one shielded container. The PSK demodulator, bit synchroniser and frame synchroniser may be located in a separated shielded container, maybe together with the computer interface. More information about the installation and shielding of microstrip and other RF circuits can be found in (9), (10).

Before building the described circuits one should first check what kind of signals are required by the computer interface. If the latter requires the frame-sync pulse, some variable delay may be required using shift registers and/or counters. The polarity of the bit clock may also be reversed. Even if the receiver is not used with the "DSP computer", it is recommended to check (11) to understand the operation of NOAA HRPT computer interfaces in general.

Of course it is hoped that everyone is able to reproduce high-quality pictures like the one shown in figure 26.
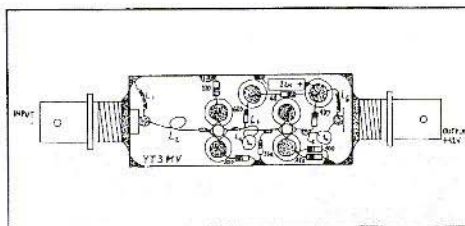
11.
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(10) Matjaz Vidmar: Microstrip Transverters for 23cm and 13cm part-2, VHF Communications 3/86, pp143-164

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Wolfgang Schneider, DJ8ES

VHF, UHF and SHF Measuring Methods Using a PC

Part- 4: High-Frequency Test Rig for up to 1.4 GHz

Following the introduction to the subject of VHF, UHF and SHF measuring using a PC, we now come to the real focal point of this series of articles - the development of a high-frequency test rig for up to 1.4 GHz.

Specifically, this means a frequency synthesiser, an mW meter, a wobbler and a spectrum analyser, combined into a measuring apparatus.

The result of all this is no miracle machine, but with minimal use of hardware a high-frequency test rig for up to 1.4 GHz can be created which makes interesting additional measuring options available for us radio amateurs.

1. CONCEPT

The PC takes over control of the individual assemblies (Fig.1) and of plotting the test results on the screen. A "486", such as is common nowadays, or
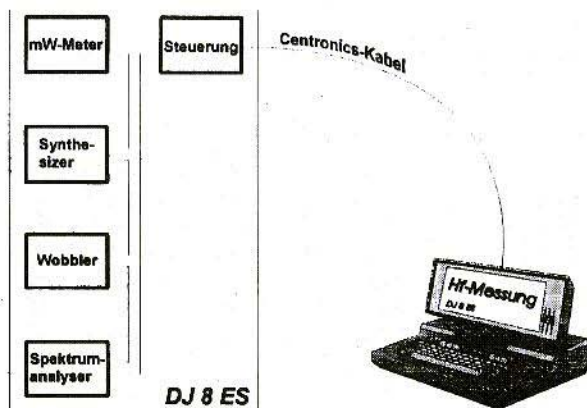
Fig.1:
The PC Controls all Functional Units
Steurung = Control, *Kabel* = Cable, *Messung* = Measurement
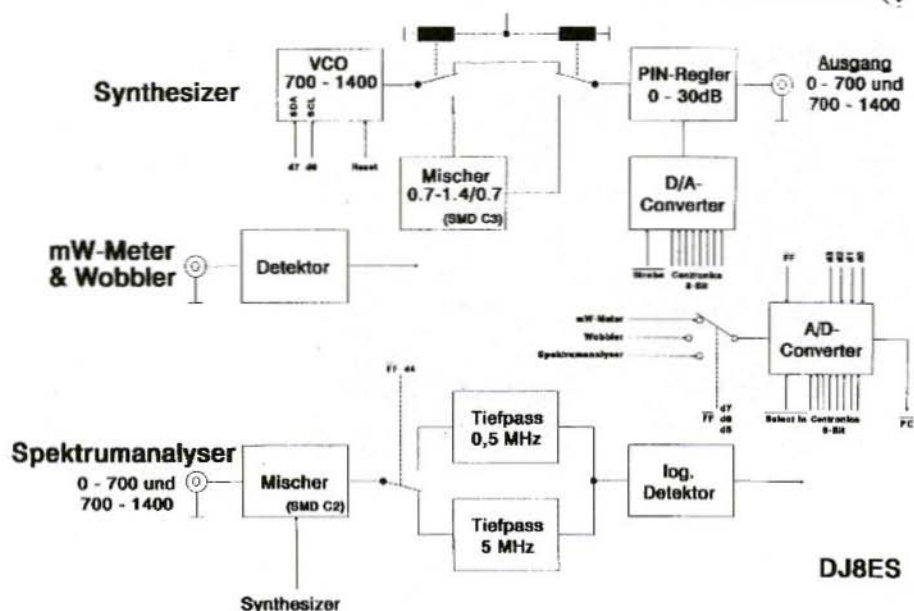
Fig.2: Automated Logic Diagram of High-Frequency Test Rig up to 1.4 GHz
Und = And, *Detektor"* = Detector, *Mischer* = Mixer, *Tiefpass* = "Band
pass, *Regler* = Controller, *Log. Detektor* = Logarithmic detector,
Ausgang = Output

even a "386" with a hard disk and a colour monitor, can meet the requirements.

The interface between the PC and the hardware is provided by a Centronics printer interface (e.g. LPT 1), which many people will have already.

The automated logic diagram (Fig.2) shows the individual assemblies and their inter-connections.

The complete hardware consists of the following units:

– VCO with PLL (700 - 1,400 MHz)

– Mixer with LO (10 - 700 MHz)

– PIN diode controller

– Diode detector

– Analogue / digital converter

– Mixer with logarithmic intermediate-frequency amplifier

The measuring apparatus referred to at the start can be created through a suitable combination of these assemblies:

– mW meter: Diode detector and A / D converter

– Synthesiser: VCO and PLL, mixer and LO, PIN diode controller

– Wobbler: VCO and PLL, mixer and LO, PIN diode controller, diode detector and A / D converter
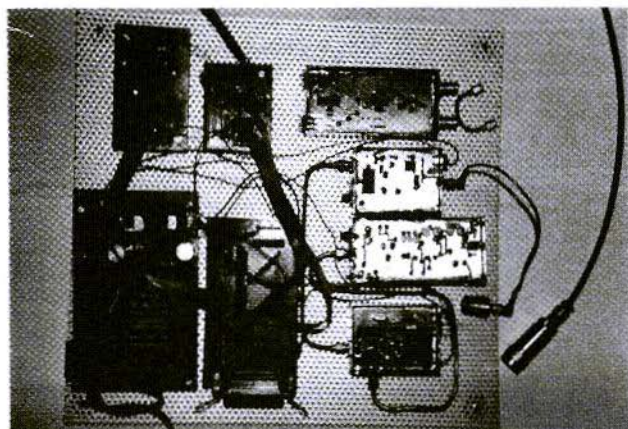
Fig.3:
The High-
Frequency Test
Rig in Experi-
mental Form

– Spectrum analyser: VCO and PLL, mixer and LO, PIN diode controller, mixer and logarithmic intermediate-frequency amplifier and A / D converter

These relationships and the circuits will be dealt with more specifically in the appropriate section. Thus, for example, the inter-action of the diode detector and the A / D converter in the mW meter will be described separately.

2.
PC INTERFACE

The standard equipment for the Centronics printer interface includes an 8-bit data output, a 5-bit input capacity and also 4 output lines. A comprehensive description explaining the functioning and, above all, the control of this interface can be found in Part 1 of this series of articles [1].

The only additional information to be given at this point is the pin occupancy layouts (not completely identical) of the 25-pin and 36-pin plug connections on the lines which are relevant for us.

Connection	Pin (24)	Pin(36)
Data 1	2	2
Data 2	3	3
Data 3	4	4
Data 4	5	5
Data 6	5	5
Data 7	8	8
Data 8	9	9
Strobe	1	1
Auro Feed (FF)	14	14
Reset	31	16
Sel In	36	17
PE	12	12

2.1. Circuit Description

Controlling all the test rig hardware requires more lines than are available in the Centronics interface. This applies both to the control of the individual
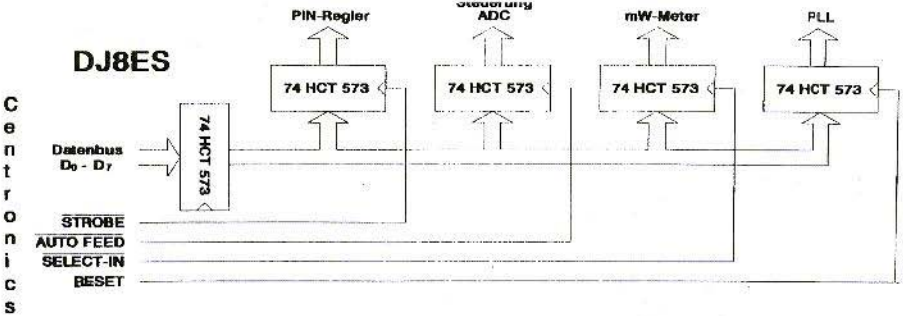
Fig.4: Interface Card for Connection to Centronics Interface
Datenbus = Data bus, *Regler* = Controller, *Steurung* = Control

assemblies, e.g. the A / D converter, and to the lines connecting the units to each other.

4 type 74HC573 data latches distribute the data (Fig.4). The control data from the PC are deposited in the associated latch by means of a transfer pulse. An additional IC 74HC573 acts as a bus drive. The blocking-off capacitors (100 nF) for the 5-V operating voltage are in SMD format and are soldered directly onto the individual IC pins on the underside of the board.

2.2. Assembly Instructions

The double-sided interface card boards (DJ8ES 029) have only a Centronics socket, 5 74HC573 data latches and the associated rod strips for the internal wiring of the rig (Fig.5). The data bus is through-hole plated with short pieces of wire.
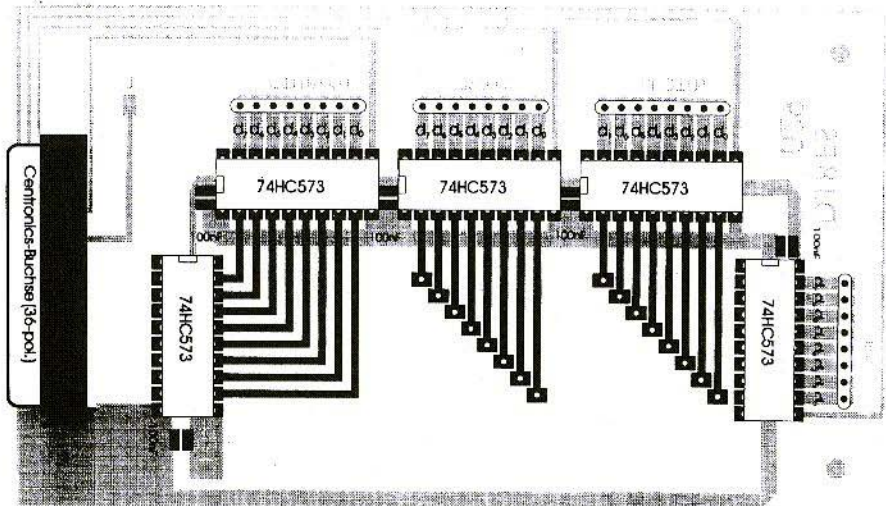
Fig.5: Component Overlay for Interface Card; *Buchse* = Socket, *Pol* = Pin

of stability and secondly to guarantee a good earth connection.

2.3. Parts List

5 x   74HC573 5 x   100 nF (SMD, model 1206) 1 x   Centronics socket (print model) 4 x   rod strips (8-pin) 2 x M3 screws (10 mm. long) with   nuts 3 x solder posts (1.3 mm.) c/w plug 1 x DJ8ES-029 board

3.
FREQUENCY SYNTHESISER

As has already been seen in the auto-mated logic diagram (Fig.2), the com-plete frequency synthesiser consists of three assemblies; VCO with PLL, mixer and PIN diode controller. When these are inter-connected, the combination covers the frequency range from 10 MHz to 1,400 MHz. The output level here can be adjusted between 10 mW (+ 10 dBm) and 10 W (-20 dBm).

Fig.6:   Prototype Interface Card

It is also important that the Centronics socket is connected to the board by M3 x 10 screws (Fig.6), firstly for reasons
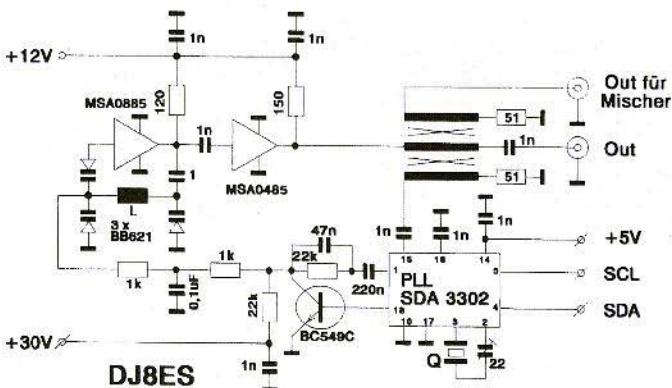
Fig.7:
Wiring Diagram of 700 MHz - 1,400 MHz VCO
Für Mischer = For mixer
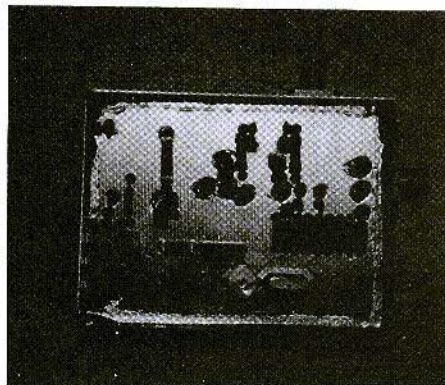
Fig.8: VCO Prototype with PLL
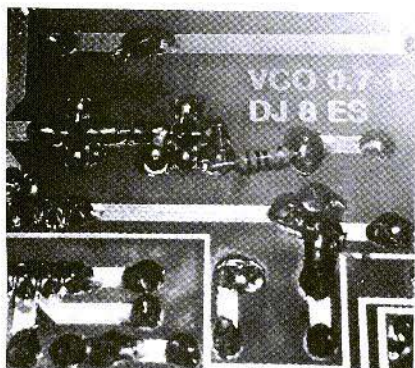
Fig.9: Magnified View

3.1. VCO with PLL

3.1.1. Circuit Description

The VCO, with a MSA 0885, spans the frequency range from 700 MHz to 1,400 MHz. The combination of three BB621's and the inductive resistor, L, is used for tuning. The signal then passes through the amplifier stage (equipped with an MSA 0485) and achieves a good 20 mW of output power (Fig.7).

The VCO has a special output of app. - 10 dBm, which avoids saturating the mixer and thus creating unnecessary inter-modulation products.

The SDA 3302 component, familiar from TV engineering, acts as a control circuit (PLL). This makes tuning steps of 62.5 kHz possible in the above-mentioned frequency range.

The frequency data required are serially transferred to the PLL module from the PC through an I2C bus (SDA = data, SCL = clock).

3.1.2. Assembly Instructions

The complete circuit is assembled on a two-sided coated epoxy board, with dimensions of 54 mm. x 72 mm.. It thus fits into a standard tinplate housing, dimensions 55.5 mm. x 74 mm. x 30 mm. (Fig.8).

Drill-holes should be cut out on the earth side with a 2.5 mm. drill. Only the earth contacts are to remain!

The assembly of the VCO and the subsequent broad-band amplifier has been described in detail by DF 9 IC in [2]. The frequency is essentially determined by the length of the inductive resistor, L, and fine calibration is also possible, through a slight bending of the wire strap.

The BB 621 tuning diodes are flush with the surface of the board (Fig.9)! All additional details can be taken from the components diagrams (Fig's.10, 11).

As always with relatively high frequencies, special attention should be paid to an assembly suitable for high frequency - short connection wires are an absolute must! This can not be said too often.

Fig.10: Components on Foil Side of VCO

Fig.11: Components on Earth Side of VCO

3.1.3. Parts List

1 x	SDA 3302 (Siemens)
1 x	MSA 0885 (Avantek)
1 x	MSA 0485 (Avantek)
3 x	BB 621 capacitance diodes
1 x	BC 549C (Valvo)
1 x	4 MHz crystal HC18U/HC25U
1 x	22-pF foil trimmer (Valvo, green)

1 x	47-nF MKT capacitor 7.5 mm. basic grid
1 x	0.1-µF MKT capacitor 7.5 mm. basic grid
1 x	0.22-µF MKT capacitor 10 mm. basic grid
1 x	120Ω / 1 W, carbon film resistor in 12.5 mm. basic grid
1 x	150Ω / 1 W, carbon film resistor in 12.5 mm. basic grid

Fig.13: Circuit Diagram of 10 MHz - 700 MHz Mixer

Fig.14: Mixer Components Diagram

Fig.15: Components on Foil Side   Mixer

1 x   tinplate housing
       55 x 74 x 30 mm.
1 x   wire strap, 15 mm. long
       CuAg Θ 1 mm. (see text)
2 x   SMA flanged bushes (4-hole)
5 x   Teflon bushings
1 x   DJ8ES-030 board

1/8 Watt resistors, 10 mm. basic grid
2 x   1 k
2 x   22 k

Ceramic Capacitors 2.5mm Grid
6 x   1 nF

and in SMD format (model 0805 or 1206)
2 x   51Ohm
1 x   1 pF
3 x   1 nF

3.1.4. Putting into Action

The VCO needs an operating voltage of + 12V / 115mA and + 5V / 35mA, together with a tuning voltage of +30V.

First the tuning range of the VCO should be tested. For this purpose, the control circuit is disconnected (collector BC 549C). With a tuning voltage between 0 V and 30 V, the oscillator must cover the frequency range 700 MHz to 1,400 MHz and more. The output power is an almost constant 20 mW over the entire frequency range.

3.2. Mixer / LO

So that the lower frequency range can also be used, a mixer / LO module is wired up subsequent to the VCO (Fig.12). This provides functional access to the range between 10 MHz and 700 MHz.

3.2.1. Circuit Description

The local oscillator required (117 MHz) is created with the oscillator circuit which is normal in amateur radio circles, using a U310. The subsequent twelve-fold circuit with 3 x BFR 90 A (Fig.13) gives an output power of app. 20 mW at 1,404 MHz.

An SMD-C3 serves as a mixer module, followed by an MMIC MSA 0104, the 9-pin deep-pass filter, and an MSA 1104 as an additional amplifier. A level of max. 50 mW can be expected at the output to control the PIN diode controller over the range from 10 MHz to 700 MHz.

3.2.2. Assembly Instructions

The mixer with the LO is also created on a double-sided coated epoxy board - the dimensions are 54 mm. x 108 mm.. The circuit thus fits into a standard tinplate housing with the dimensions 55.5 mm. x 111 mm. x 30 mm..

The through-platings on the ring mixer (SMD C3) are of 1.5 mm. CuAg wire, while 3 mm. long hollow rivets have been used for the other platings.

Otherwise, the type and manner of assembly are the same as those for the VCO assembly. The position of the assembly elements can be taken from the components diagrams (Fig.14 and Fig.15) for the foil side of the DJ8ES 031 board.

The SMD-C3 mixer should be soldered on only following the complete calibration of the frequency multiplier stages. The assembly can thus be put into operation faster and more easily.

3.2.3. Parts List

1 x	MSA 0104 (Avantek)
1 x	MSA 0304 (Avantek)
1 x	78LO9, voltage controller
1 x	U310 (Siliconix)
3 x	BFR 90A (Valvo)
1 x	SMD C3, mixer
1 x	117 MHz crystal, series resonance, HC18-U or HC25-U
1 x	BV 5061, Neosid, 0.1 µH blue / brown
3 x	5 pF Sky-Trimmers (green)
2 x	6 pF foil trimmers (grey)
2 x	22 pF foil trimmers (green)
7 x	1 nF trapezoid capacitors

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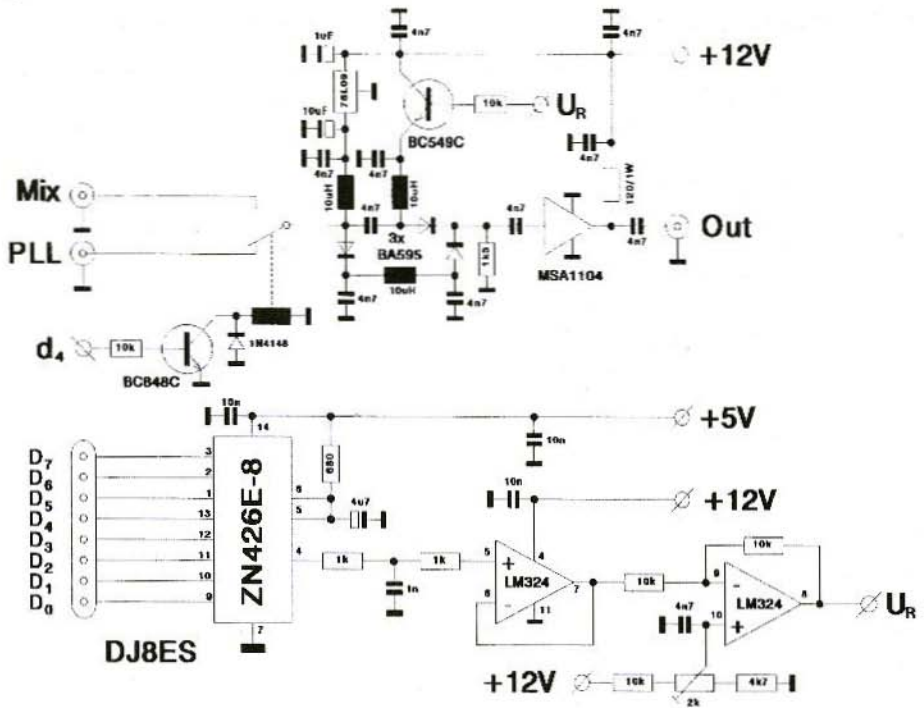
Fig.16: Pin Diode Controller
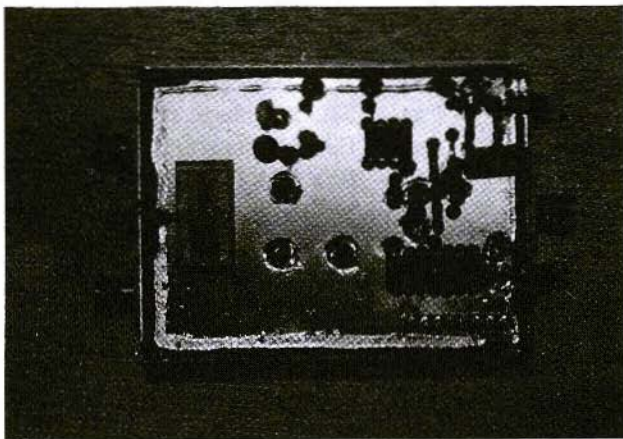
Fig.17:
Pin Diode Controller
Prototype

1 x   1 μF / 20 V
tantalum electrolytic capacitor

1 x   10 μF / 20 V
tantalum electrolytic capacitor

1 x   tinplate housing
55 x 111 x 30 mm.

2 x   SMA flanged bushes (4-hole)

16 x   hollow rivets, length 3 mm.

1 x   Teflon bushing

1 x   DJ8ES-031 board

1/8 Watt resistors, 10 mm. basis grid

4 x   47 Ohm
2 x   68 Ohm
1 x   100 Ohm
2 x   120 Ohm
1 x   220 Ohm
2 x   1.5 k
1 x   10 k
2 x   15 k

Ceramic capacitors, 2.5 mm. basic grid

1 x   10 pF
1 x   82 pF
7 x   1 nF
1 x   100 nF

All SMD capacitors (model 0805)

1 x   2.7 pF
2 x   3.9 pF
2 x   8.2 pF
1 x   10 pF
3 x   1 nF

3.2.4. Putting into Operation

With an operating voltage of + 12 V, the assembly picks up about 160 mA of current. Only 50% of this is allocated to the two amplifiers MSA 0104 and MSA 1104.
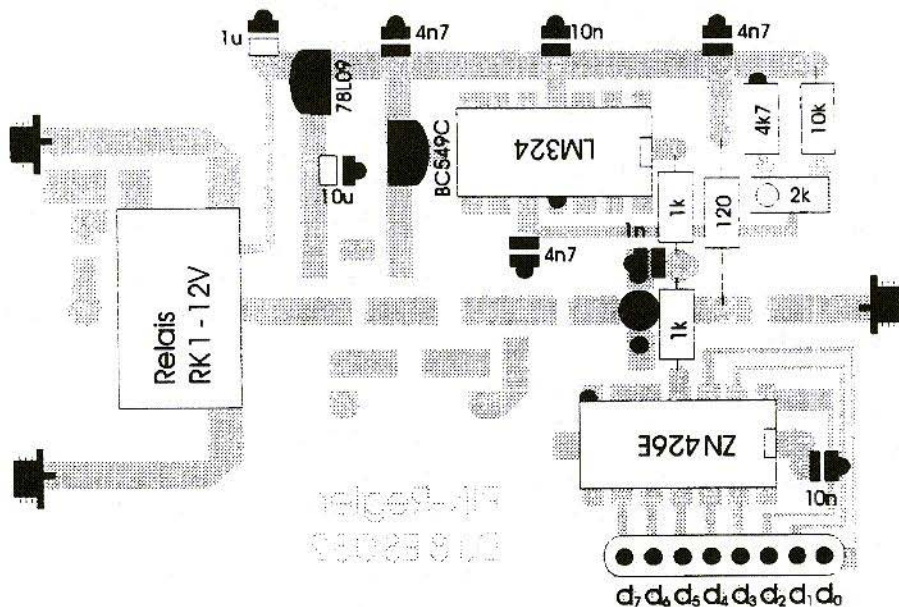
Fig.18: Pin Diode Controller Components Diagram
Relais = Relay
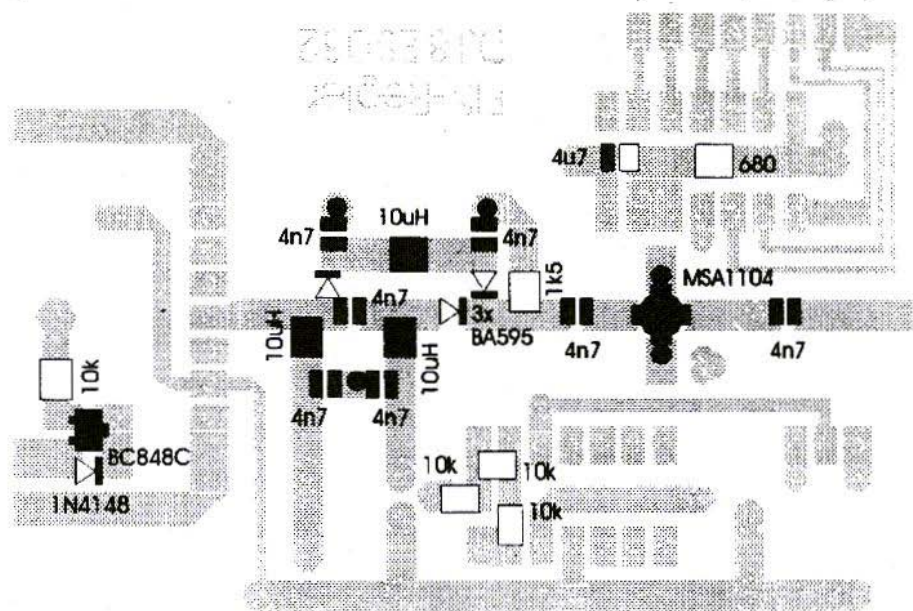
Fig.19: Foil Side Components

After the oscillator (U310 with a BV5061 coil) has been made to oscillate at 117 MHz, the frequency multiplier is calibrated step by step. With the VCO connected up, the mixer achieves an output power of max. 50 mW in the range between 10 MHz and 700 MHz.

3.3. Pin Diode Controller

3.3.1. Circuit Description

A circuit which was previously standard in television engineering is used as the pin diode controller (Fig.16). Three SMD diodes (BA 595) thus control the output power of the synthesiser at the desired value.

The control circuit is voltage-controlled and is controlled by the PC by means of a D / A converter (ZN 426E). Thus with

8 bits, about 256 steps are generated in all in the 0 to 2.5 V range for every 10 mV.

Because of the circuit, a control value of "0 dez" corresponds to maximum output power. The maximum possible damping is obtained with "225 dez". Depending on the frequency, it is at max. 70 dB in the short-wave range and is still 30 dB at the upper frequency limit of 1,400 MHz (Fig.17).

3.3.2. Assembly Instructions

The pin diode controller is created on a double-sided coated epoxy board. The dimensions are 54 x 72 mm.. The circuit thus fits into a standard tinplate housing which has dimensions of 55.5 mm. x 74 mm. x 74 mm. x 30 mm..

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The position of the assembly elements can be seen in Fig.18 for the components side, and in Fig.19 for the foil side, of the DJ8ES 032 board. In other respects, the same assembly instructions apply here as for the assemblies already described.

3.3.3. Parts List

1 x	ZN 426E-8, D / A converter
1 x	MSA 1104 (Avantek)
1 x	LM 324
1 x	78L09, voltage controller
1 x	BC549C
1 x	BC848C (SMD)
1 x	1N4148 (SMD)
3 x	BA595 (SMD)

1 x	2 kΩ, trimmer (vertical, 2.5 mm. basic grid)
1 x	120 Ω / 1 W 12.5 mm. basic grid
1 x	1 µF / 35 Vtantalum
1 x	10 µF / 20 Vtantalum
1 x	RK 1-12V, relay (Matsushita)
3 x	SMA flanged bushes (4-hole)
1 x	post strip (8-pin)
3 x	Teflon bushings
5 x	hollow rivets (3 mm. long)
1 x	tinplate housing 55 x 74 x 30 mm.
1 x	DJ8ES-032 board

1/8 Watt resistors, 10 mm. basic grid

2 x	1 k
1 x	4.7 k
2 x	10 k

Ceramic capacitors, 2.5 mm. basic grid

1 x	1 nF
3 x	4.7 nF
2 x	10 nF

and in SMD format:

3 x	10 µH chokes
1 x	4.7 µF / 25 V tantalum

SMD resistors and capacitors (model 1206 or 0805)

1 x	680 Ohm
1 x	1.5 k
4 x	10 k
7 x	4.7 nF

3.3.4. Putting into Operation

The PIN diode controller needs two operating voltages: + 12 V / 65 mA for the analogue section and + 5 V / 10 mA to operate the ZN426E D / A converter.

For calibration, the spindle trimmer must merely be set in such a way that a high-frequency signal can be fed in and given maximum amplification. For this purpose, the data connections D0 to D7 must be connected to earth, which corresponds to a D / A converter output voltage of 0 V.

The entire assembly has a transit amplification of app. + 3 dB.

The output level can later be reduced to the desired value using the program.

4.
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---

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     Simple Measuring and Calibrating
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     Preparations
     VHF Congress, Weinheim, 1991,
     Congress Proceedings

ERRATUM: 10 GHz Super-Regenerative Receiver, Issue 1/1997

Please accept our apologies for an error which appeared in Fig.3 (page 3). The supplies at the bottom right-hand side of the diagram were incorrect. The corrected diagram is reproduced below.
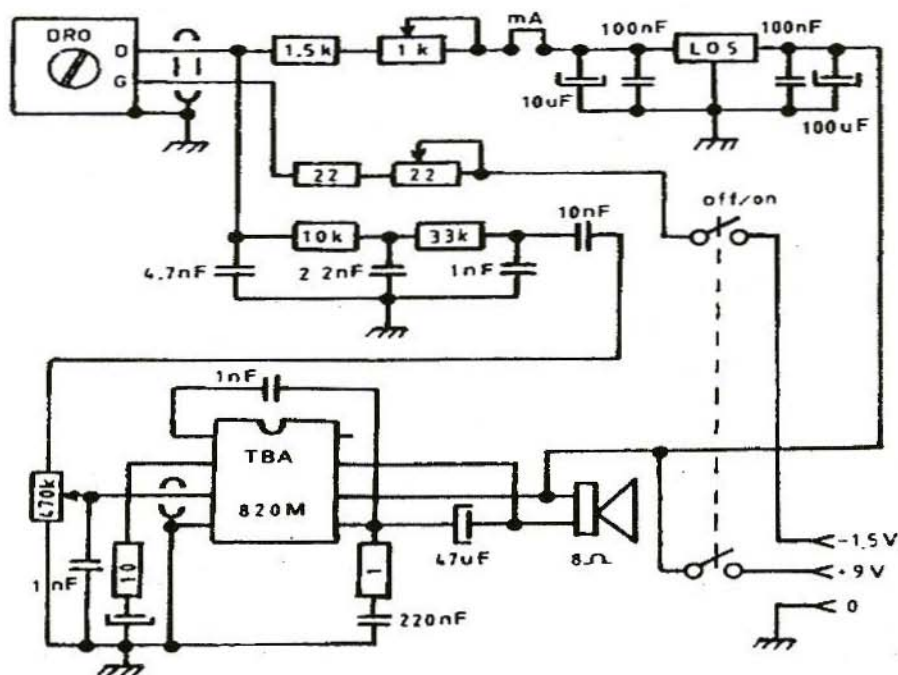
Gunthard Kraus, DG8GB

Design and Realisation of Microwave Circuits Part-3

6.2.7. Board Layout for both Versions of the Circuit

For a project on a board, we also need the width and the length of the striplines used. But for this purpose we also need to carry out a few more simulations:

Puff in fact also supplies us with the behaviour of the circuit for "non-ideal striplines", in which the losses through the board and the skin effect are taken into account, together with the dispersion (= scattering, i.e., for example, the emergence of lines of electric flux at the edges of the stripline and the consequent impedance level changes, etc.).

Here, experience shows that the more accurate the material data are the more precisely the simulation will reflect reality, and the discrepancies can be reduced to less than 1%!

For this purpose, the Puff file for the amplifier circuit to be processed has first to be loaded into the word processor and the board material data have to be entered. For the FR4 material with a thickness of 1.5mm. and 2 x 35µm.

\b{oard}		{.puf file for PUFF, version 2.0}
d	0	{display: 0 VGA or PUFF chooses, 1 EGA, 2 CGA, 3 One-color}
o	1	{artwork output format: 0 dot-matrix, 1 LaserJet, 2 HPGL file}
t	0	{type: 0 for microstrip, 1 for stripline, 2 for Manhattan}
zd	50.000 Ohms	{normalizing impedance. 0<zd}
fd	1.693 GHz	{design frequency. 0<fd}
er	4.300	{dielectric constant. er>0}
h	1.500 mm	{dielectric thickness. h>0}
s	150.000 mm	{circuit-board side length. s>0}
c	0.100 mm	{connector separation. c>=0}
r	0.010 mm	{circuit resolution, r>0, use Um for micrometers}
a	0.000 mm	{artwork width correction.}
mt	0.035 mm	{metal thickness, use Um for micrometers.}
sr	2.000 Um	{metal surface roughness, use Um for micrometers.}
lt	1.5E-0002	{dielectric loss tangent.}
cd	5.8E+0007	{conductivity of metal in mhos/meter.}
p	5.000	{photographic reduction ratio. p<=203.2mm/s}
m	0.600	{mitering fraction. 0<=m<1}
\		

Table 1

```
===== F2 : PLOT =====
Points 499
Smith radius 0.20
   f   1.6948 GHz
□ S21  15.08dB -60.3°
× S22 -24.25dB 178.0°
```

```
Time   24.9 secs
```

```
===== F3 : PARTS =====
a  l  47nH
b  l  15nH
c  tline! 71.83Ω 91.2°
d  tline! 141.5Ω 91.2°
e  device cfy30.dev
f  tline! 141.5Ω 34.4°
g  tline! 141.5Ω 6mm
h  tline! 50.5Ω 91°
i
```

```
===== F4 : BOARD =====
zd   50.000  Ω
fd    1.693 GHz
er    4.300
h     1.500 mm
s   150.000 mm
c     0.000 mm
Tab  microstrip
```

```
===== F1 : LAYOUT =====
```

file : ukuber3
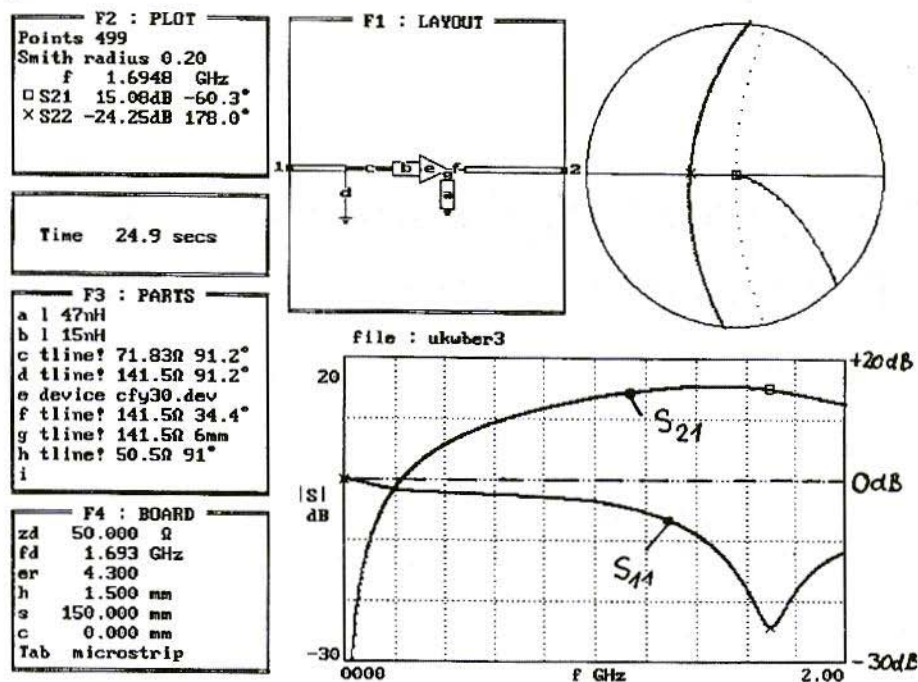
Fig.13: "Puff" Screen Print-Out: Ideal Amplifier with CFY 30

copper plating, it should look like this for 1.693 GHz - the important entries are marked out in bold and the rest of the file, with the S-parameters, etc. is left out (Table 1).

When the file has been stored, Puff is called up again and the amplifier circuit to be processed is loaded. In field F3, for each stripline, an exclamation mark, "!", is now placed directly after the entry "tl" or "tline". This switches to "advanced modeling", the most accurate reflection of reality.

But now there is more work to do. If the cursor is moved to each of the individual striplines in turn and the equals sign, "=", is keyed in, then the actual current characteristics of the line being scanned are displayed in dialogue field

F1. It should come as no surprise if there are divergences, sometimes considerable, from the (ideal) value entered. But keep correcting the impedance level and the electrical length of the line in field F3 until the values in F1 or the frequency responses correspond to the ideal when plotted once more (call-up into field F2 with letter p)!

If this has been tackled correctly (and don't forget, the new circuit in field F2 has to be stored under a suitable name, using the command "CTRL s"), then we obtain a Puff screen in accordance with Fig.13.

The mechanical dimensions of the striplines corrected in this way, which are in fact needed for the board project, are obtained as follows:
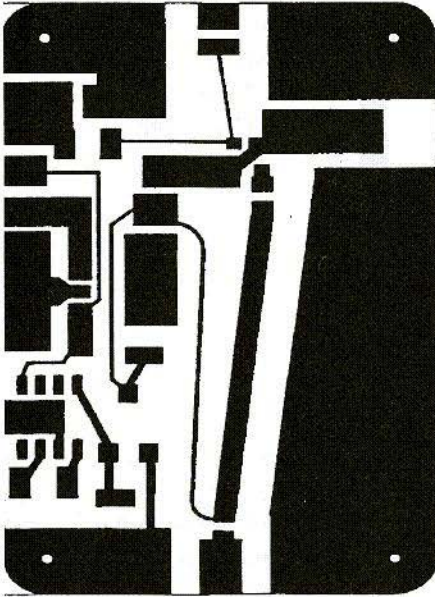
Fig.14: Printed Circuit Board Layout
for Circuit with Directly
Earthed Source Pin and
Negative Gate Bias Voltage
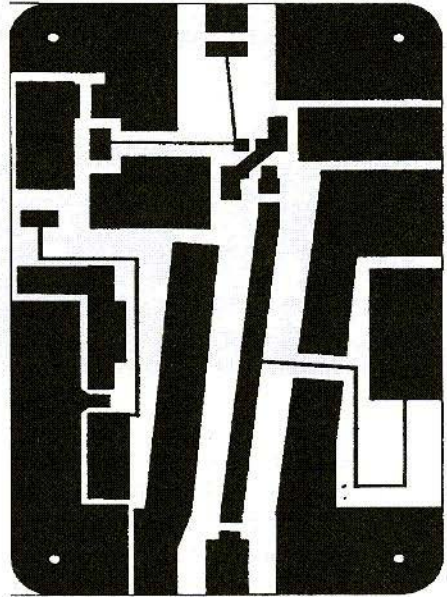
Fig.16: Layout of Circuit with Source
Resistance and Capacitive
Source Earthing

Move the cursor back to the line in question in field F3, delete the exclamation mark after "tl" or "tline" - for example, by pressing the space bar - and re-enter the equals sign. The length, l, and the width, w, of the selected microstrip appear immediately in dialogue field F1. Make a note of these readings and do not forget to re-enter

the deleted exclamation mark in field F3 afterwards. Repeat the process for all lines to obtain the following list (Table 2).

Now we can move on to the actual project board. For this purpose, of course, we require a modern layout CAD system of some kind.

Component	Description	Z in Ω	El. Mechanical Length	Length mm	Width mm
c	Microstrip	71.83	91.20 Grad	25.301	1.504
d	"	141.50	91.20 Grad	26.597	0.221
f	"	141.50	91.20 Grad	10.032	0.221
g	"	141.50	20.04 Grad	6.000	0.221
h	"	50.50	91.00 Grad	24.614	2.874

Table 2
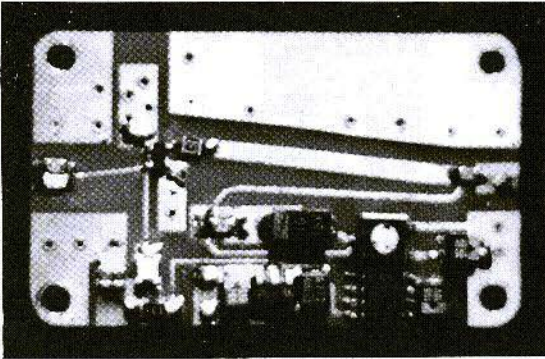
Fig.15:
Completed Prototype of
Low-Noise Amplifier
Direct Earthing

I am making no recommendations here, as there is a very wide choice. I myself still enjoy working with Geddy-CAD, which is frequently to be found on electronic CD's, on diskettes or in mailboxes. Once you have cleared the initial hurdles, it is extremely suitable for the direct drafting of Puff layouts. (Contact the publishers for more details on Geddy CAD.)

Fig.14 shows the finished layout. The board and the components for the circuit version with a directly earthed source pin and an IC 7660 for generating the negative gate bias voltage are depicted in Fig.15.

Fig.16 shows the layout of the circuit version with the gate earthed by means of a quarter-wave transmission line and a shorted-out source resistance. Fig.17 shows the prototypes.

To produce the boards, I use a somewhat unconventional but thoroughly practical method. The layouts are printed out onto transparent paper (greaseproof paper) by the laser printer on a 1:1 scale, and are used for direct exposure of the photo-coated FR4 material. Conductor widths going down to 0.2 mm. can be handled without problems. For higher precision requirements - for example, stripline filters or (small)

Fig.17:
Fully Fitted-Out Prototype
of LNA Capacitively
Earthed Source Pin

series production - the drafts are magnified before printing until they just fill a DIN A4 sheet. They are then printed out onto pure white paper with as smooth a surface as possible, and then this is filmed, with the film, again, showing the board on a 1:1 scale. In this way, printing errors during scaling down are greatly reduced, and we can get down as far as a 0.1 mm. track width.

The layouts themselves, of course, are the product of any amount of experience and likewise of many mistakes and discarded habits. So there follows a series of clarifications, which can also be consulted during the drafting of additional converter circuits:

a) Earth surfaces should be selected to be as large as possible. The minimum distance between them and the striplines should be 1 to 2 x the thickness of the board. Thus, firstly, the impedance level of the line is not too strongly influenced, and secondly the leakage fields of the lines can now no longer wander around so much in the region and cause the circuit to oscillate.

b) The earth surfaces of the input section (= gate area), the source area and the output section (= drain area) must be separated from one another, as otherwise there will be more and more of a tendency to oscillate due to couplings of one kind or another.

These individual surfaces should now be connected to the continuous earth surface on the underside of the board in as low-impedance and low-inductive a manner as possible. In practice (e.g. with SAT-LNC's), this is done

through many little holes which are then through-plated. I don't have this option, and found a solution in a Philips application circuit with silver-plated hollow rivets of 0.8 mm. diameter.

c) The source connection is particularly critical for the layout, since every effective or blind resistance has an immediate negative feedback effect here. The consequences can never be forecast precisely, but can be estimated using a Puff simulation:

The amplification often falls more rapidly than expected in the upper frequency range, but just as often the input or output reflection exceeds 1 and the circuit oscillates!

The manufacturer therefore also connects this electrode diagonally to two pins of the housing; firstly as a screen between the gate and drain, secondly to halve the impedance to earth, as now both pins are wired in parallel.

Consequently, each source pin has its own earth surface, which must be earthed using at least 5 rivets, starting as close as possible to the pin!

A Puff simulation can be used at any time to demonstrate that even changes of 1nH in the gain slope have a noticeable effect above 1 to 1.5 GHz!

d) When soldering on SMD components, you must ensure that these through-platings or hollow rivets do not become full of zinc, for any bore which is full is ineffective for high-frequency work, because of the low

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penetration depth (= skin effect!) at these high frequencies the current path through this bore is blocked! In this way, unfortunately, the total inductance of the through-platings then increases again somewhat, and we give away the advantages we took so much trouble to obtain.

e) Should the circuit not fill the housing with its striplines, we also need a means of connection to the input and output plugs. This is brought about, naturally, through 50-Ohm striplines of appropriate length, so the widths of these lines are also in the list above.

f) Once capacitors become necessary in any high-frequency path, several SMD chip capacitors are connected in parallel, if possible. This again reduces the total inductance of the configuration, and the coupling or earthing becomes more broad-band.

g) Should it not be possible to gain

control of the tendency of an amplifier circuit to oscillate, in spite of these measures, SAT-LNC's tried and trusted method using damping material made of conducting foamed material can be turned to on a trial basis.

These strips or panels of black foamed material are used as packaging material for CMOS-IC's. As a trial, a suitable piece is placed onto the circuit, and a test is carried out of how effective it is in damping. Subsequently, this material is glued to the inside of the housing cover (if gluing is necessary). Of course, there are very wide divergences in the effects of the various materials in circulation. For micro-wave engineering, the versions with low surface resistance are required, which can be recognised by the fact that they have a resistance of max. 10 to $100k\Omega$, measured at a distance of 10mm.. Moreover, these are usually the "harder" versions of the foamed material.
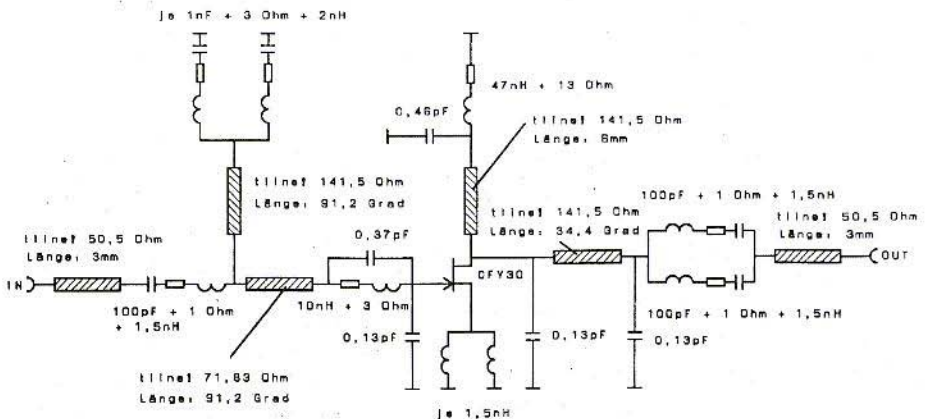
Fig.18: Advanced Simulation Circuit using Puff
Länge = Length
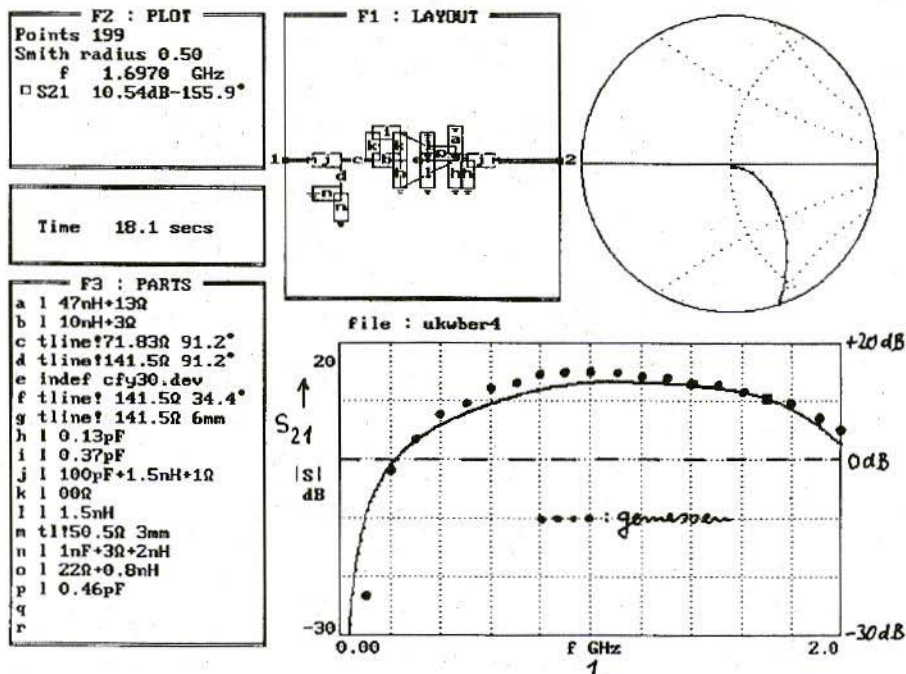
Fig.19: Puff Screen Print-Out: Simulation Result for Circuit with Directly Earthed Source Pin: Amplification I S21 I from 0 to 2 GHz

6.2.8. Simulation Results and Test Readings of the Version with Directly Earthed Source Pin

When we assemble the project circuit and measure its frequency response for the first time, we will certainly be greatly disappointed at the divergence from the simulation results. If we can gain control of the unintentional oscillation, that still does not mean the battle is won. The behaviour at high frequencies is not as desired, with the amplification falling relatively faster there. The "artificial model" must therefore be considerably expanded and refined to approach the reality.

The following facts, in particular, should be taken into consideration:

a) At all soldering points in the high-frequency stage which do not form part of a stripline, a capacity of app. 0.1pF must be provided for the "soldering scab" towards the underside of the board, i.e. the continuous earth surface. A value of 0.13pF produced the best agreement between theory and practice.

b) All chip earthing and coupling capacitors display a low inductance and also a series resistance, due to losses in the ceramic material. There is usually a diagram somewhere in the manufacturer's data books which gives the impedance gradient up to the maximum frequencies. The replacement values can be calculated
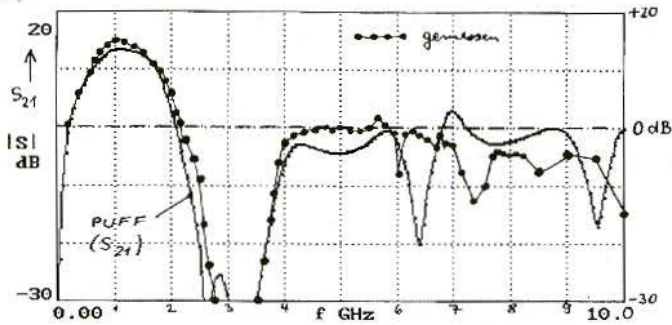
Fig.20:
Comparison of
Simulation Result
and Measured
Values for Circuit
with Directly
Earthed Source Pin
in Frequency Range
0 to 10 GHz

from this, or from the self-resonant frequency and the rise in impedance above the self-resonance.

For the chip capacitors used at 10pF, made of the material NPO, a series circuit is thus obtained, as a sufficient approximation, from 10pF + 1Ω + 1.5nH.

c) The SMD coil, with 10nH at the gate of the FET, has a quality grade of 50 at 1,700 MHz. Due to the unavoid-

able self-capacitance, its inductance has already risen to 13 nH. According to the data sheet, its self-resonant frequency lies at "2,300 MHz". I have measured values of between 2,500 and 2,600 MHz.

Its replacement wiring diagram gives an inductance of 10nH in series with a resistance of 3Ω. A 0.37pF capacitor is wired in parallel with this series circuit.
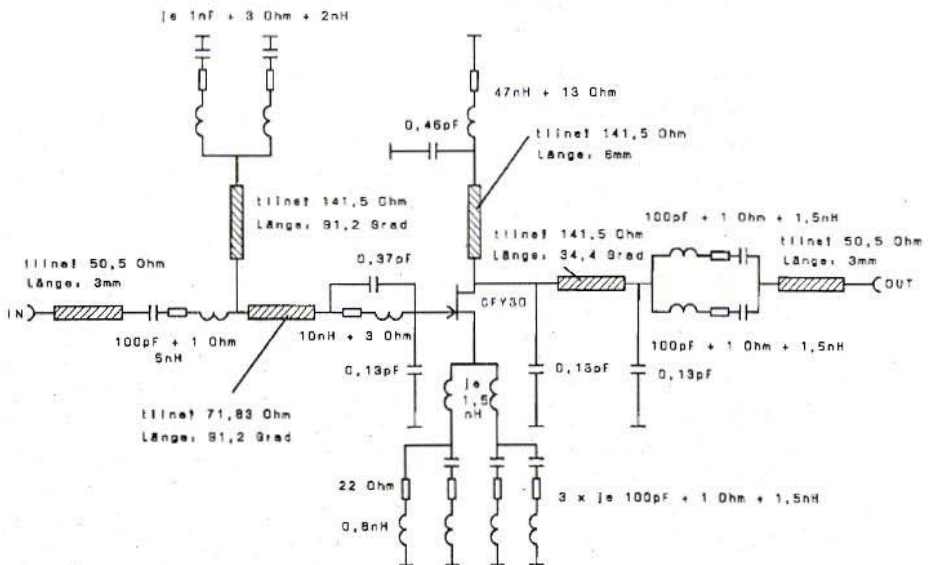
Fig.21: Replacement Wiring Diagram for Circuit with Capacitively Earthed Source Pin
Länge = Length

```
═══ F2 : PLOT ═══
Points 99
Smith radius 0.50
    f    1.6939  GHz
□ S21   10.23dB-154.8°

━━━ Time   10.5 secs ━━━

═══ F3 : PARTS ═══
a 1 47nH+13Ω
b 1 10nH+3Ω
c tline!71.83Ω 91.2°
d tline!141.5Ω 91.2°
e indef cfy30.dev
f tline! 141.5Ω 34.4°
g tline! 141.5Ω 6mm
h 1 0.13pF
i 1 0.37pF
j 1 100pF+1.5nH+1Ω
k 1 00Ω
l 1 1.5nH
m tl!50.5Ω 3mm
n 1 1nF+3Ω+2nH
o 1 22Ω+0.8nH
p 1 0.46pF
q
r
```
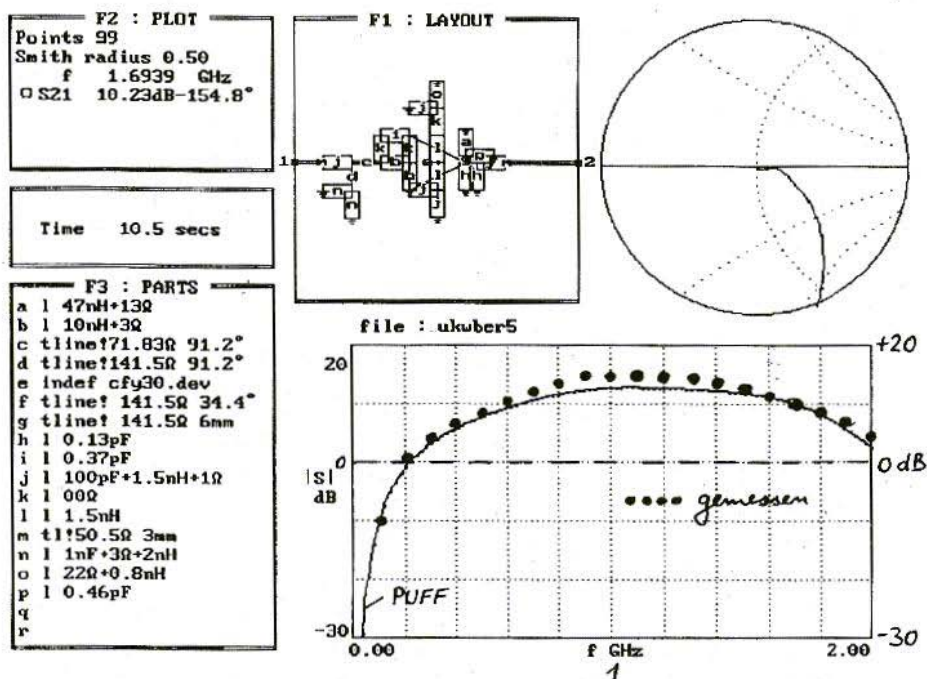
Fig.22: Puff Screen Print-Out: Gain Slope I S21 I for Circuit with Capacitively
Earthed Source Pin in Simulation / Measured Values Comparison from
0 to 2 GHz

d) The SMD choke with 47nH (in the drain circuit), has a quality grade of app. 30 to 40. In addition, the unavoidable self-capacitance, of app. 0.2pF, should be taken into account, as this forms the basis for the self-resonant frequency given in the data sheet. Because of its size 1210 SMD, the throttle also needs a soldering scab about twice as big, and with double the capacity.

For this component, a series circuit is used, with values of 47nH and 13Ω, parallel to which lies a capacitor, with a total value of 0.2pF + 0.13pF + 0.13pF = 0.46pF.

e) At the source connection, the through-platings from the two earth scabs on the top face to the bottom earth surface, in the form of two inductances (each of app. 1.5 nH) between the source pin and the earth potential, are to be taken into account in the simulation.

But in addition the following change is necessary:

The entry for the GaAsFET used in the F3 parts list must be amended from "device cfy30.-dev" to "indef cfy30.dev". That means a "dipole" is suddenly converted into a "tri-polar network", and the source connection, which was previously not accessible, can

now be earthed through the two parallel-wired coils, each of 1.5 nH.

f) On the feed for the negative gate bias voltage, rather high capacity values were set for the earthing using "standard materials" at the end of the quarter-wave transmission line, to make the screening more broad-band. This naturally leads to somewhat higher losses and series inductances, so a new component has to be entered in the F3 list for this.

So we come to the Puff simulation circuit as per Fig.18. Anyone who now starts to complain about the confusion and the lack of room when entering numerous components in layout field F1 may be interested in a tip:

Define a "resistance with 0Ω", i.e. a shunt. You can now extend the "connecting legs" of the components. I have, of course, discovered that this works correctly only at low frequencies, and that in broad-band simulations up to a few GHz - above all, as soon as striplines come into the picture - significant errors will be observed, as against the "original circuit", so be careful!

Finally, Fig.19 shows the new simulation result.

Anyone who is surprised, when the simulation starts, to receive the message "Danger - Circuit too big for Puff, not enough memory" need only make a significant reduction in the number of plot points. In certain circumstances, it makes sense to reduce them to only 50. Sometimes it is also necessary simply to have the main memory organisation of the PC re-optimised, using the DOS service program "Memmaker".

In addition, the readings obtained for the gain slope for the frequency range from 100 MHz to 2 GHz should be plotted into the frequency response curve. The approximation is already very close!

In the range between 1 and 1.5 GHz, Puff prophesies that amplification will be too low, the reasons for which might well be:

a) As the frequency decreases, the board material losses also diminish, but calculations are carried out using a constant loss factor of 0.015, which then becomes too high.

b) For coils and capacitors, Puff can calculate only for a constant loss resistance, but not for a constant quality, as would be the case in
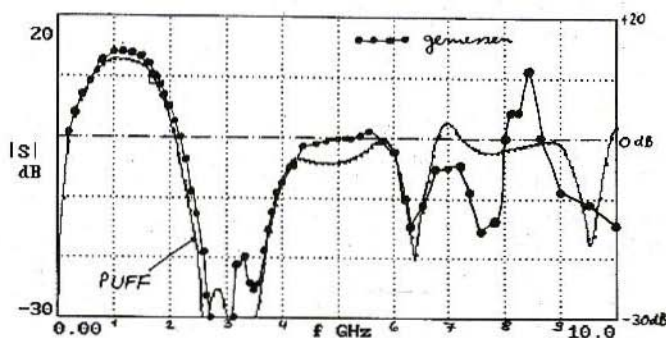
Fig.23:
Expanded Simulation
Range 0 to 10 GHz:
Comparison of
and
Measured Values
Capacitively Earthed
Source Pin
Gemessen = Measured
values
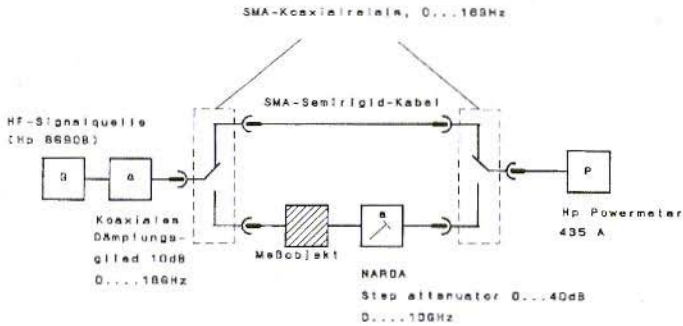
Fig.24: Basic Structure of a Calibration Device

HF-Signalquelle = High-frequency signal source, *Koaxiales Dämpfungsglied* = Coaxial damping module, *Koaxialrelais* = Coaxial relay, *Semirigid-Kabel* = Semirigid cable, *Meßobjekt* = Measurement Object

practice; so the series resistances for blind components are too high at relatively low frequencies

Finally, it was also of interest to know up to what frequency the Puff simulation supplies a result which can be used in practice. So Fig.20 shows the calculated and measured gain slopes in a joint diagram, up to a frequency of 10 GHz.

It can be seen from this that up to about 5 GHz the simulation model drawn up provides results which are confirmed by the measurements. For frequencies above this, a more accurate replacement circuit has to be worked out first, and tests also have to be done to determine whether wave guide effects are already playing a part in the closed housing. Moreover, the capacitive couplings between the various areas of the board (with values markedly below 0.1pF) can no longer be neglected.

6.2.9. Theory and Practice in the Circuit Version with Capacitively Earthed Source Pin

In principle, the existing circuit is used for the simulation, but in the source area it includes the replacement circuits for three parallel-wired capacitors, each of 100pF, and the source resistance with 22Ω (Fig.21). Please remember that even such a little mite of an SMD resistance as a model 0805 has a self-inductance. It was determined by the measurement circuit as approximately 0.8nH and has been immortalised in the F3 parts list. If this is too much, you must help yourself a bit by linking two components in a parallel circuit.

It would also be a rewarding task to reduce the connection soldering scabs for all SMD components used in the high-frequency branch (FET's, throttles, capacitors, resistances, etc.) in order to reduce the interfering capacities towards the continuous earth surface, but the minimum size of the soldering scabs is very firmly based on the solderability

and positioning accuracy of the components!

The rest is now almost routine, and leads to the results depicted in Fig.22 (frequency range 0 to 2 GHz) and Fig.23 (frequency range 0 to 10 GHz). The measured values should again be entered as well, so that they can be compared with the simulation. In the range between 0 and 3 GHz, the response differs only insignificantly from the version with a directly earthed sourced pin. Above this, the chip capacitors begin to cause concern, and at app. 8 GHz create a resonance peak with 12dB amplification.

To sum up, it can be stated that:

a) Right up to 3 GHz and above, the two circuit versions not only display almost identical frequency responses, but display messages which very precisely confirm the predictions made by Puff.

b) If the source connection is earthed through several chip capacitors, then above 3 GHz divergences occur, which have their origin in the impedance cycle of the source earthing component. The circuit with direct earthing of the source connection displays a more uniform response there, without the extreme resonance step-up. For this reason, it should probably be controlled rather more strictly and should display less broad-band noise. You should just test the use of the wickedly expensive 10-GHz ATC chip capacitors, which consist of a solid porcelain chip.

c) For the housing construction, the

layout, the selection of components and the mounting, there is a series of rules, the infringement of which is immediately punished by unsatisfactory frequency responses, or even by a tendency to oscillate.

d) As soon as you have some experience in estimating all the effects involved and the behaviour of the components correctly, you can virtually have blind faith in Puff's predictions - to such an extent that, after initially trying out a new circuit with Puff, you can draft more and more complicated replacement images, to determine where measurement divergences will arise.

6.3. A Few More Measuring Tips

To conclude the chapter on amplifiers, a few more hints on measurement technique and on plotting frequency response curves:

The ideal, and most modern, method, is to use a network analyser. Fortunately, there are fellow radio amateurs who use this kind of equipment at work, and can occasionally run something through. However, in order to reach one's goal with one's own measuring equipment, which is usually rather out-of-date, two things are necessary:

a) Increased patience and time for "manual measurement", since this involves rotating, adjusting, recording and correcting, and:

b) Constructing a measurement apparatus which imitates the "self-calibration process" of modern equipment (Fig.24). Here, you can simply

switch from "Calibrate" (= signal passing through a section of cable) to "Measure" (= signal passing through the object of measurement), or vice versa, with the help of two SMD coaxial relays. If, in the "Calibrate" position, we now turn the output voltage up until the power meter shows precisely end-scale deflection, "Zero dB", we then finally just have to switch over to "Measure" and observe the rise or fall in the instrument reading.

The change in the display then exactly matches the desired amplification or damping in dB.

Many inherent errors and many frequency responses from the measurement equipment, cables and connecting plugs in use are eliminated in this way, as they have the same effect in the calibration channel and the measurement channel, and we are interested only in the differences.

Of course, different transmission loss readings from the two relays lead to an incorrigible and permanent error, so only the finest kit must be used for this (military versions, gold-plated SMA sockets with a frequency range up to 18 GHz, and crosstalk attenuation of min. 60dB, reflection factors below 10%, etc.). In the same way, you must fake an ideal moving load to the test transmitter by means of a subsequently switched-in coaxial attenuation member, to keep down the level of any additional measurement errors caused by a poor input reflection factor for the object of measurement.

Since, in addition, the measurement range of the power meter does not usually exceed 40dB, a reversible calibrating line, with 0 to 40dB and a usable frequency range going up to over 10 GHz must be positioned after the object of measurement if it is, for example, an amplifier. In this way, the rise in the level after an amplifier can be damped down until it is again within the range of measurement of the power meter.

(To be continued)

D.Eckart Schmitzer, DJ4BG

Transistor Calculations using Rules of Thumb

In many cases approximate values are sufficient for the rough dimensioning of transistor circuits, and thus help to save time in circuit design.

1. INTRODUCTION

When I had to dimension my first transistor circuit of my very own for a piece of industrial equipment, more than 25 years ago, an "old hand" helped me out with a few rules of thumb. I was surprised how simple it all really was! In engineering faculties, calculations using h-parameters and other highly scientific but impractical processes make this field appear complicated and somewhat mysterious.

I would like to introduce these rules of thumb, which are founded on an entirely correct basis, and show how they can be applied. They can frequently make life easier for us. Which makes it all the more amazing that they are so little

known! True, at first glance these formulae have little to do with high-frequency technology, but these basic principles can be useful here too. As it is irrelevant for practical application, we can dispense with their derivation. The following section explains how the other formulae can be determined from the basic formula, step by step, when additional conditions are taken into consideration. No doubt one or two people can establish parallels with tube technology!

2. THE BASIC FORMULA

If we simplify the formula for the relationship of current and voltage in a semi-conductor diode as much as possible, we arrive at the relationship:

$$S = 39 \cdot I_d \quad (mA/V) \qquad (1)$$

For a current of, for example, 1 mA, the curve has a gradient or a steepness (S) with the dimension of a conductance of
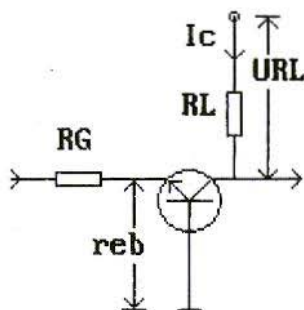
Fig.1: The Basic Circuit with NPN

39mA/V, at 10mA it is 390mA/V, and so on.

It should be noted that only the characteristics of the semi-conductor itself are being considered here, but not, for example, feed and contact resistances!

But it can also be deduced from such a curve that a specific alteration in voltage is required for a specific current change, which can also be regarded as a dynamic resistance (r - dU / dl).

Thus, the steeper the curve, the more low-impedance the diode becomes. This resistance can be obtained directly from the reciprocal value of the steepness:

$$rd = 1/S \quad \text{also} \quad rd = 1 / (39 \cdot 1) \quad \text{or}$$

$$rd = 26 / 1(\Omega = mV / mA) \qquad (2)$$

Thus, a current of 1mA gives a resistance of 26Ω.

3.
APPLICATION TO THE TRANSISTOR

3.1. The Basic Circuit

The same formulae for the basic emitter diode apply to a transistor in a basic circuit (Fig.1).

The wiring diagrams are shown in simplified form and without the components for setting the DC operating point.

The steepness of a transistor can thus be calculated from formula (1), and the input resistance in the basic circuit (now referred to as reb) from formula 2.

But this also allows the voltage amplification (v) to be calculated:

$$v = S \cdot R_L \qquad (3a)$$

But the steepness (S) can also be expressed using formula (1) and then has:

$$v = 39 \cdot I_C \cdot R_L \qquad (3b)$$

But here (Ic.RL) is the voltage drop on the load resistor, from which the (open-circuit) voltage amplification can be derived as follows:

$$v = 39 \cdot U_{RL} \qquad (3c)$$

Thus, we can already estimate the maximum possible amplification of a transistor amplifier from a simple measurement of the emitter current.

Since, with a sufficiently high current amplification, the difference between the emitter current and the collector current is only very small, this also applies to the measurement of the collector current. This is somewhat simpler, since the
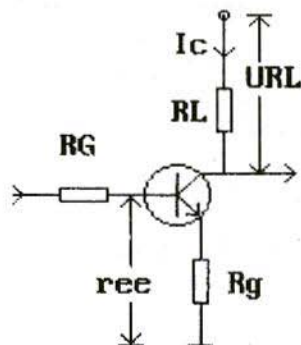
Fig.2: The Emitter Circuit

tuned by the internal resistance of the instrument.

If we take the reciprocal value of the steepness from formula (2), we obtain:

$$v = R_L / r_{eb} \qquad (3d)$$

But this reveals to us another important point, namely that this amplifier would have to be controlled from a generator with the resistance (RG = 0), since otherwise a voltage division would take place between the generator resistance and the input resistance.

If we now also include the generator resistance (RG), we finally obtain the basic circuit voltage amplification:

$$v = R_L / (r_{eb} + R_G) \qquad (4)$$

But the influence of the generator resistance can also be regarded as a reduction in the steepness (negative current feedback!), if, as has already been done above, we use the formula (r = 1/S) and invert it:

$$S' = 1 / (r_{eb} + R_G) \qquad (5)$$

Here, S' is the effective steepness when there is negative feedback from the

generator resistance (RG). If, with a sufficiently strong current, reb becomes considerably smaller than RG, then, within certain limits, steepness and amplification are practically independent of the characteristics of the transistor.

3.2. The Emitter Circuit

To begin with, nothing alters with the transistor in an emitter circuit (Fig.2). However, it must be borne in mind that an AC level which has been reduced by the current amplification (ß) is flowing in the base electrode. But this means that we obtain the same control effect as in the basic circuit, only with less control current.

The input resistance has thus been increased by the factor (ß):

$$r_{ee} = ß \cdot r_{eb} \qquad (6)$$

If we think first of all of having the emitter completely shunted to earth, no negative feedback occurs, and the voltage amplification can again be determined from the formulae (3a) to (3d).

If there is negative feedback from an additional resistance in the emitter cir-
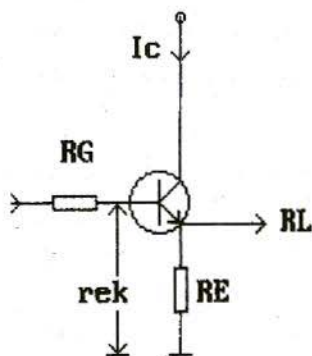
Fig.3: The Collector Circuit

cuit, the formulae (4) and (5) for amplification or the effective gradient apply again. In this connection, RG should now be replaced by the negative feedback resistance (Rg), thus:

$$v = R_L / (r_{eb} + R_G) \qquad (7)$$

and

$$S' = 1 / (r_{eb} + R_G) \qquad (8)$$

We must extend formula (6) to take in the negative feedback resistance:

$$r_{ee} = \beta \cdot (r_{eb} + R_G) \qquad (9)$$

The input resistance can thus be further increased by the negative feedback resistance.

In the emitter circuit too, formula (3c) applies, with which the open-circuit voltage amplification can be determined through a DC voltage measurement, provided no additional negative feedback occurs.

Maximum contrallability of the circuit, i.e. maximum possible output voltage, is obtained when half the transistor voltage falls away from the load resistor. This is the voltage which remains from the emitter up to the high point of the load resistor.
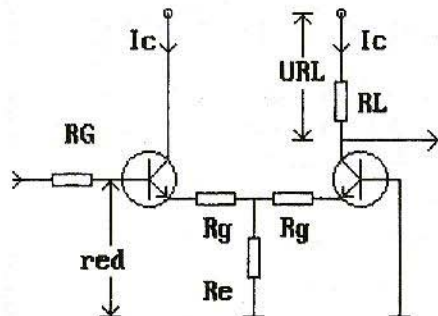
Fig.4: A Differential Amplifier

With no negative feedback, such a circuit will again have an open-circuit amplification in accordance with formula (3c). This is only about half as big as the maximum value for the maximum possible load resistor, but with a very much lower controllability.

3.3. The Collector Circuit

In the collector circuit, also known as the emitter follower (Fig.3), formula (9) can be applied by analogy, for the input resistance is:

$$r_{ee} = \beta \cdot (r_{eb} + R_1) \qquad (10)$$

where in open circuit rl is equal to the emitter resistance, RE, and under load equal to the parallel circuit made from the emitter resistance, ReE, and the load resistor, RL, thus:

$$R_1 = (R_E \cdot R_L) / (R_E + R_L)$$

The emitter follower has a low output resistance, but one at which the generator resistance can usually not be neglected. Reduced by the current amplification factor, (β), it breaks down as:

$$r_{ik} = r_{eb} + R_G / \beta \qquad (11)$$

The amplification of such a stage as an emitter follower is about $v = 1$. However, it is worth while to check this, for there is, all the same, a voltage division between the internal resistance and the load resistance, so that we obtain:

$$v = R_L / (R_L + r_{eb} + R_G / \beta) \qquad (12)$$

Only with a very big load resistor will the amplification really come anywhere near 1!

3.4. The Differential Amplifier

The differential amplifier may perhaps

be quoted here as a special case (Fig.4), though it does represent a combination of emitter follower and basic circuit. The first stage has the input resistance of the basic circuit as load resistor, i.e. reb, so its input resistance is:

$$r_{ed} = \beta \cdot (r_{eb} + r_{eb}) = \beta \cdot 2 \cdot r_{eb} \quad (13)$$

With identical current levels in both transistors, the input resistance is thus twice as high as with one stage in the emitter circuit. By contrast, the second stage sees the output resistance of the emitter follower as the source resistance (cf. formula 11), so that its gradient can be represented as:

$$S = 1 / (r_{eb} + r_{eb} + R_G / \beta) \quad \text{also}$$

$$S = 1 / (2 \cdot r_{eb} + R_G / \beta) \quad (14)$$

The voltage amplification can be represented by:

$$v = R_L / (2 \cdot r_{eb} + R_G / \beta) \quad (15)$$

This already gives proper importance to the influence of the emitter follower. It can be seen from equations (14) and (15) that, with a very low generator resistance, the gradient and amplification are just half as big as with the emitter circuit, but on the other hand (in accordance with formula 13), the input resistance is twice as high. In addition, the feedback critical at higher frequencies is markedly less.

The characteristic curve of the differential amplifier displays another additional special feature. It is now symmetrical, and thus very linear in the central section, in complete contrast to the single transistor stage. It will be understood that here too, through negative feedback (for reasons of symmetry, with two Rg resistances in the emitter feeds), it is possible to obtain an increase in the input resistance and a simultaneous reduction in the gradient and the amplification, plus further linearisation. This then leads to a gradient of:

$$S = 1 / (R_g + R_g + r_{eb} + r_{eb} + R_G / \beta)$$

and so

$$S = 1 / (2 \cdot [R_g + r_{eb}] + R_G / \beta) \quad (16)$$

which gives an amplification of:

$$v = RL / (2 \cdot [Rg + reb] + RG / \beta) \quad (17)$$

André Jamet, F9HX

A Broadband VHF-UHF-SHF Amplifier

The use of MMIC (Monolithic Micro-wave Circuit) is now very common for professional and amateur applications. Numerous deisgns have been done from Hewlett-Packard and Mini-Circuits leaflets. Well known MSA and MAR are available at a very low cost. Articles published in the amateur magazines give description of amplifiers (1) and even frequency multipliers (2).

The frequency limit of those MMIC does not exceed our 1296 MHz band but a new product is now available, the Mini-Circuits family (3) which reaches 10 GHz, for a very low cost too.

Shown here is an example of a very simple, but meticulous design. The PCB is made from glass-PTFE engraved by acid or with a cutter, input and output capacitors should be High-Q grade ones. Other components are SMA sockets and standard SMD resistors and capacitors.

To make an amplifier which operates at frequencies lower than 432 MHz, one needs to increase input and output capacitors up to 100 pF, with a possibility of damaging the 10 GHz behaviour owing to the parasitic inductance increase. But I have not tried to do that.

Frequency MHz	Gain Linear dB	Power at 1dB Compression dBm	Power at Saturation dBm
432	11	10	13
1296	12	10	13

Table1: Test results of measurements on the Prototype

This small module can be used to help as a measurement amplifier when the level is too low to be used directly. It also can increase the level of a low-power local oscillator. Test measurements made on a prototype are shown in Table 1.

The circuit diagram of the unit is shown in Fig.1. 'C' is made up from a 1nF + 100nF + pcb pad. 'L' is a U-shaped inductor made from 10mm of 0.1mm diameter silvered copper wire.

The PCB design is shown in Fig.2. The actual size of the board is 25mm x 17mm. It is manufactured from 0.79mm thick Glass-PTFE material. The line width is 2.5mm and the through-connecting rivets are 1.2mm diameter.

A view of a completed unit is shown in Fig.3.
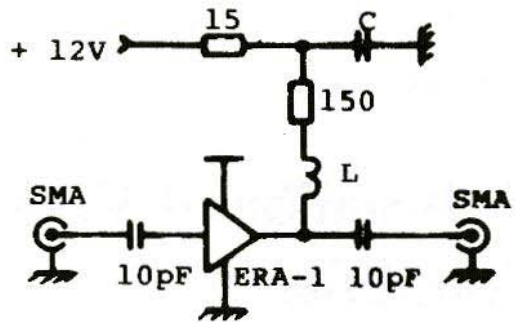
Fig.1: Circuit Diagram
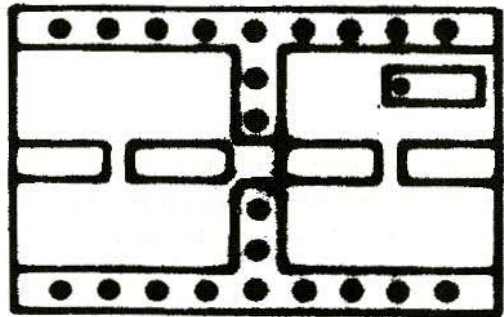
Fig.2: The Printed Circuit Board
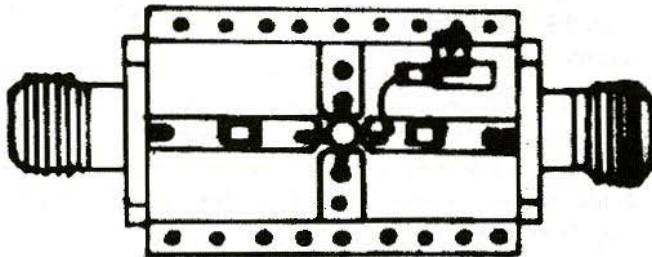
Fig.3: An Overall View

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(1) VHF and Microwave Applications of Monolithic Integrated Circuits, WB5LUA, The ARRL UHF/Microwave Experimenters Manual

(2) Frequency Multipliers Using MMICs, WA8LNC, The ARRL UHF/Microwave Projects Manual

(3) ERA Amplifiers; ERA-97-1, Mini-Circuits

Tips, Improvements and Corrections

DIY Construction of a Receiver for GPS and GLONASS Satellites by Matjaz Vidmar S53MV; Issues 1/94 to 4/95

For those having difficulty obtaining a suitable display module, the Philips LBN 244F-90 (with LED rear illumination) can be used.

In diagrams 26 and 28 (1/95) some minor errors crept in and are corrected in the diagrams overleaf.

In Fig.38 (2/95) the identification of L2 is missing on the 100µH inductor next to IC CA3089.

In Fig.42 (2/95) the identification of the diode HSCG 1001 is missing, it leads away from pin-19 of the DTACK IC 74HC245.

In Fig's.41 and 42 (2/95) and 46 and 47 (3/95) the logic gates are incorrectly drawn. Corrected diagrams are shown overleaf.

Also in Fig.46 (3/95) the crystal is shown as 10 MHz instead of 12 MHz.
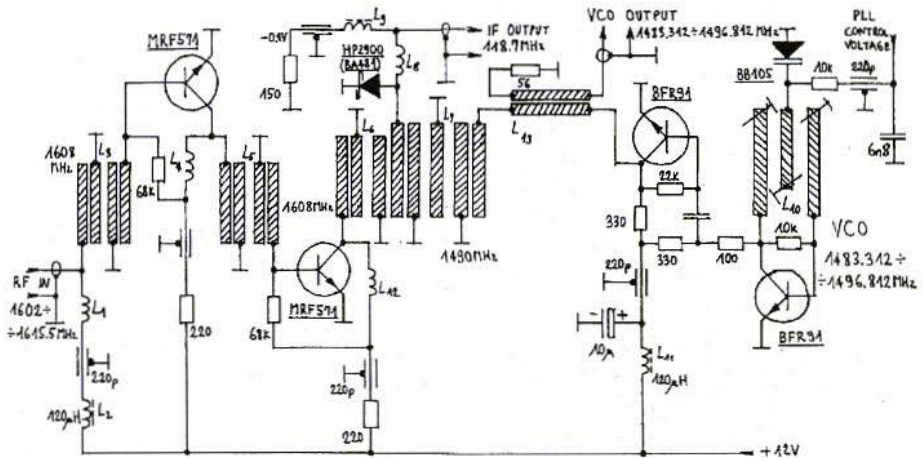
Fig.26 GLONASS RF Module
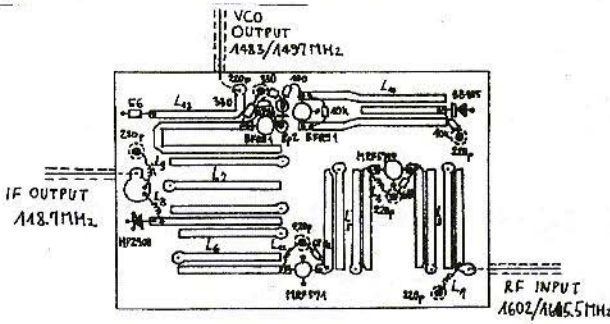
Fig.28:
**GLONASS RF Module
Component Overlay**

Below:
**Fig's:41 and 42
GPS/GLONASS DSP
Hardware parts-1 and 2**
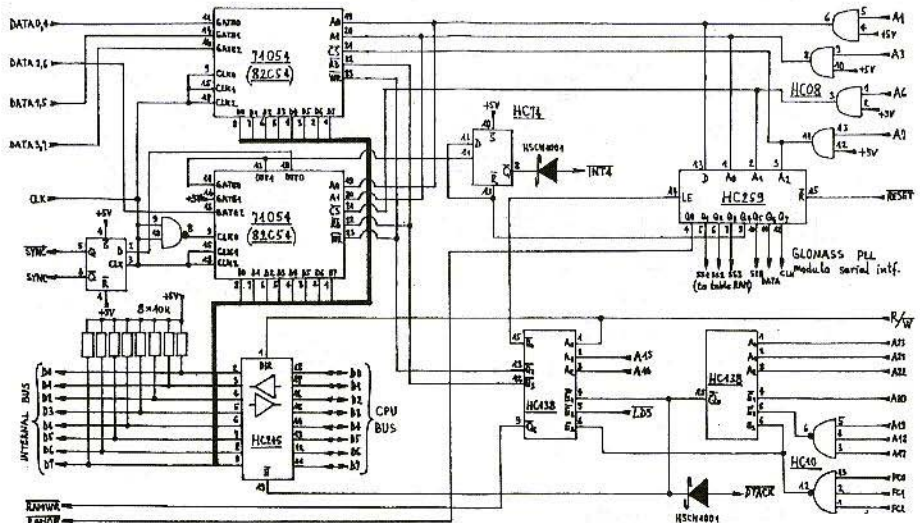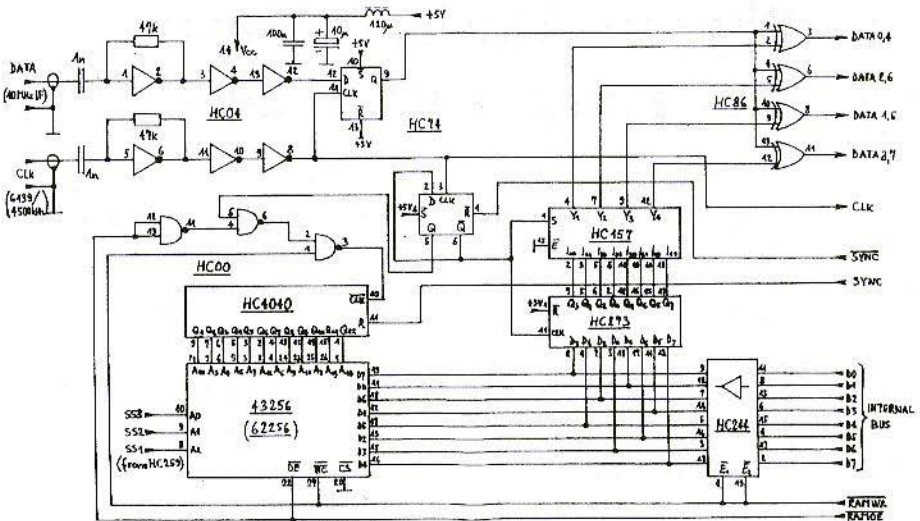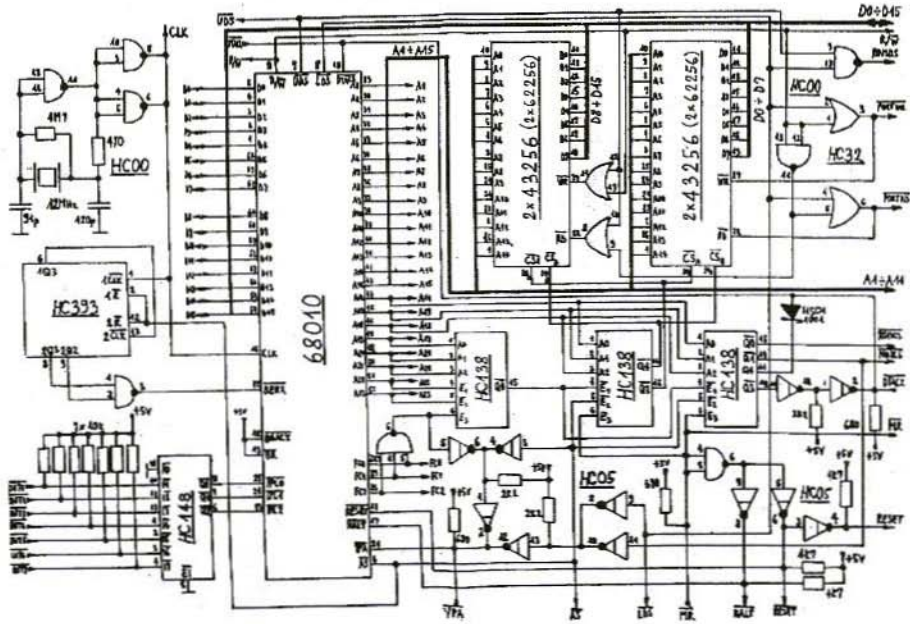
Fig.46: CPU Board Circuit Diagram (part-1)
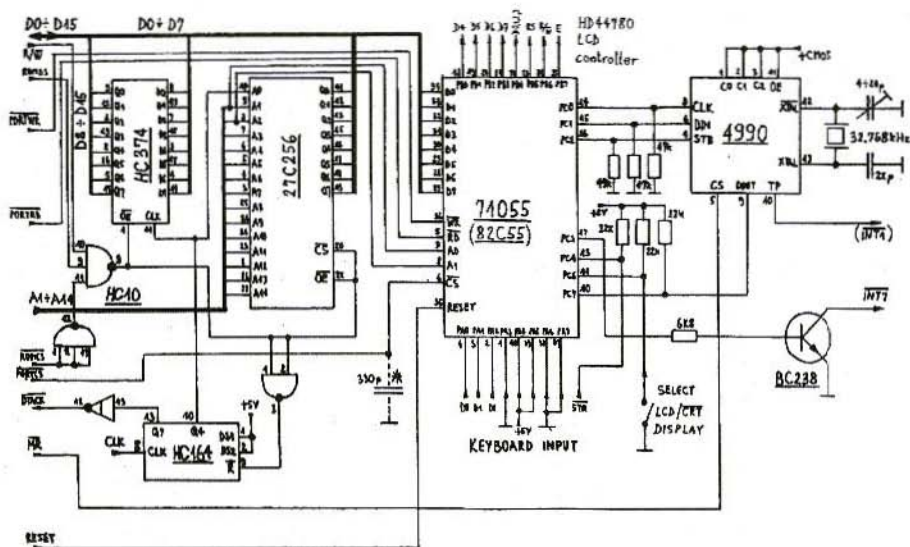
Fig.47: CPU Board Circuit Diagram (part-2)

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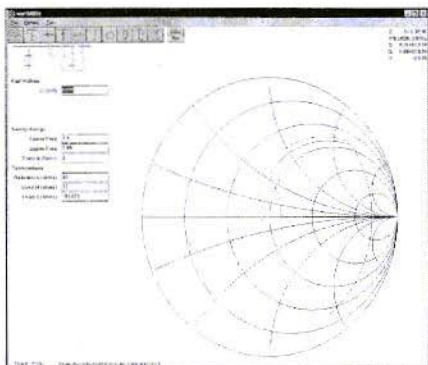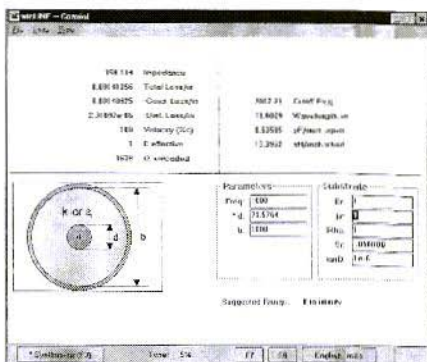
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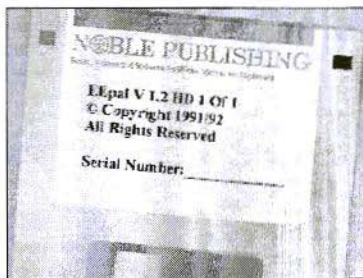
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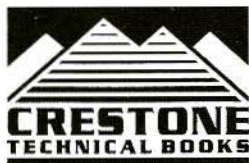
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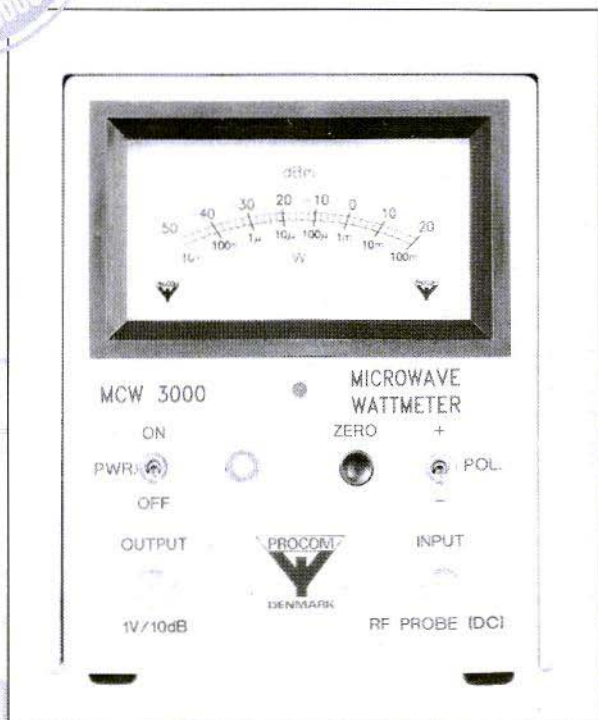**www.noblepub.com**