RADIOTRONICS

IN THIS ISSUE

COVER

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WIDE-BAND AMPLIFIER AND DISCRIMINATOR INTEGRATED CIRCUITS

Introduction

The following note describes the CA3011 and CA3012 wide band amplifier and the CA3013 and CA3014 amplifier-discriminator integrated circuits. The circuits are primarily designed for use in television, FM and communications receivers. The CA3011 and CA3012 are basically if amplifier-limiters intended for use with external FM detectors. The CA3013 and CA3014, however can provide if amplification, noise limiting, FM detection, and low-level audio amplification in the sound-if section of intercarrier television receivers or in FM receivers without the use of external components other than tuned coupling networks and bypass elements.

Circuit Description

The circuit configurations of the CA3011 and CA3012 are identical; the circuits differ, however, in that the CA3012 is capable of operation at higher levels of dc voltage and current. Similarly, the CA3013 and CA3014 are identical, except that the CA3014 has higher dc voltage and current ratings.

Figure 1 shows the schematic diagram of the CA3011 or CA3012 wide-band amplifier. The amplifier consists of three direct-coupled cascaded differential-amplifier stages and a built-in regulated power supply. Each of the first two stages consists of an emitter-coupled amplifier and an emitter follower. The operating conditions are selected so that the dc voltage at the output of each stage is identical to that at the input to the stage. This condition is achieved by operation of the bases of the emitter-coupled differential pair of transistors at one-half the supply voltage and selection of the value of the common-emitter load resistor to be one-half that of the collector load resistor.

As a result, the voltage drops across the emitter and collector of the emitter-coupled stage operates at a voltage equal to V_{BE} plus the common-base potential. The potential at the output of the emitter follower, therefore, is the same as the common-base potential.

Figure 2 shows the schematic for

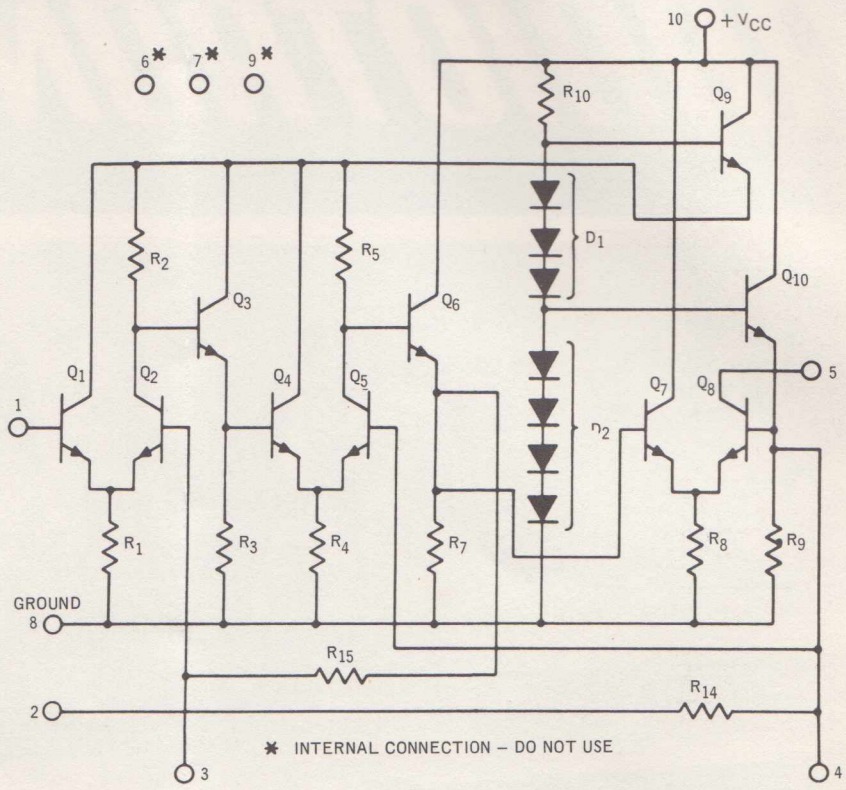


Fig. 1 Schematic diagram of the CA3011 or CA3012 integrated-circuit wide-band amplifier.

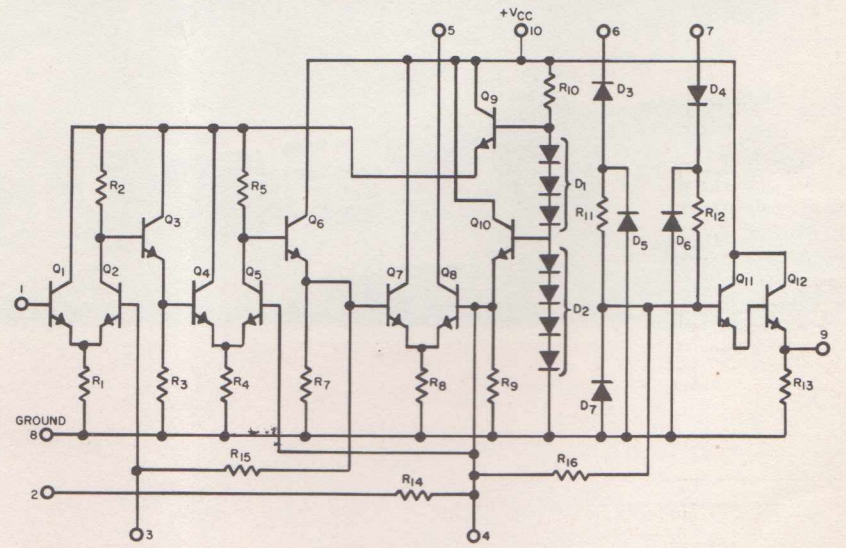


Fig. 2 Schematic diagram of the CA3013 or CA3014 integrated-circuit.

the CA3013 or CA3014 amplifier-discriminator. Each amplifier-discriminator includes a three-stage, direct-coupled, amplifier-limiter cascade and regulated power supply identical to those in the CA3011 and CA3012 wide-band amplifiers, together with an FM detector and

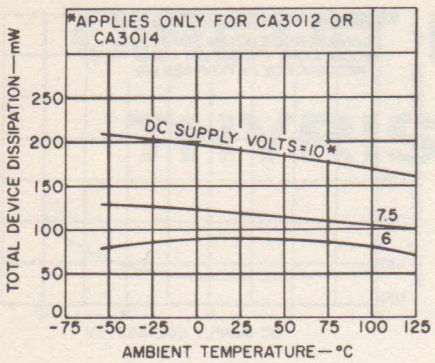


Fig. 3 Total dissipation as a function of temperature.

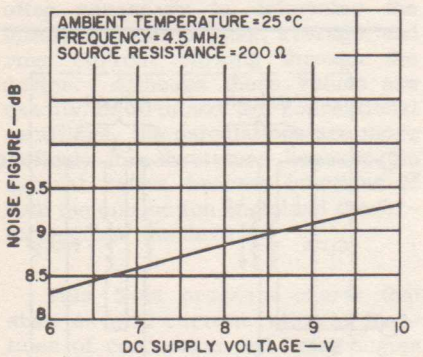


Fig. 4 Noise figure as a function of dc supply voltage.

a Darlinton pair low-level audio output stage, on the same silicon chip. The operation of the amplifier-limiter stages and the regulated power supply is identical to that of the wide-band amplifiers.

The FM detector includes all the components required for FM demodulation except the tuned phase-shift transformer. In the design of the integrated detector, the large non-integrable diode load capacitors conventionally used to obtain peak rectification in balanced phase-shift discriminators and in ratio detectors are eliminated, and average detection is employed with a substantially resistive load. Filtering of the signal frequency and its harmonics is provided by the distributed capacitance of the load resistors; additional filtering is provided by the capacitance of the small reverse-biased diode junctions D_5, D_6, and D_7. The parallel input resistance at the discriminator terminals 6 and 7 is typically 12,000 ohms, the parallel input capacitance at these terminals is typically 7 picofarads.

Operating Characteristics

The CA3011 and CA3013 are designed to operate at various levels of dc supply voltage up to 7.5 volts. The CA3012 and CA3014, which have higher supply-voltage and dissipation ratings, may be operated at dc supply voltages up to 10 volts.

For each circuit, the external dc voltage is applied to terminals 10 and 5; dc voltages required at other terminals are derived from the internal power supply. When the circuits are operated at the same dc levels, the characteristics of their amplifier-

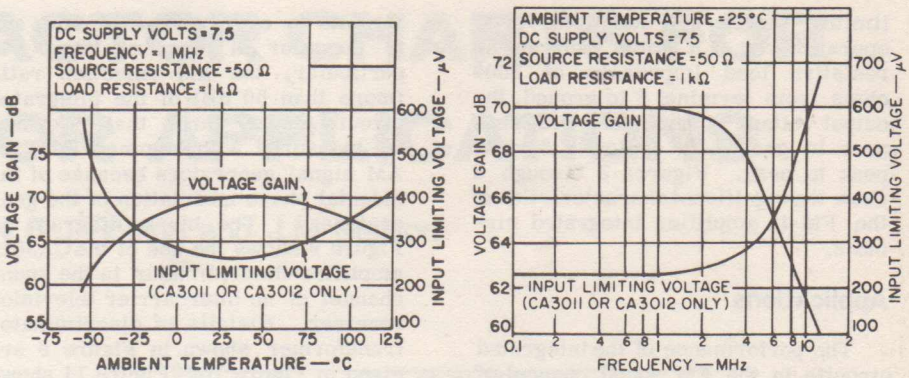


Fig. 5 Voltage gain and input limiting voltage as a function of temperature and frequency.

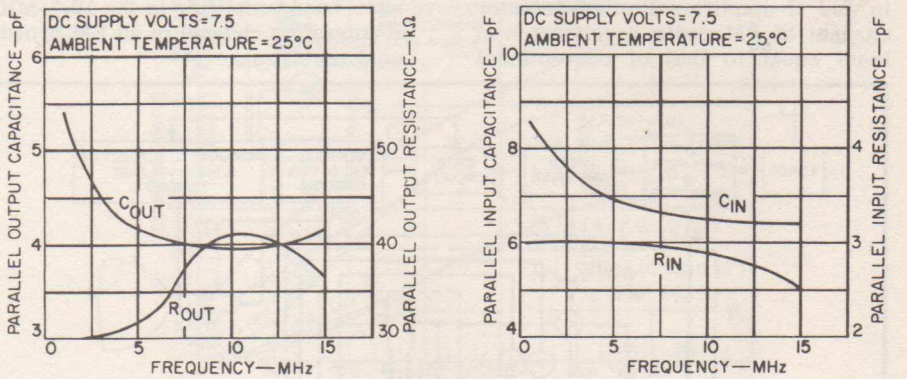


Fig. 6 Input and output impedance as a function of temperature.

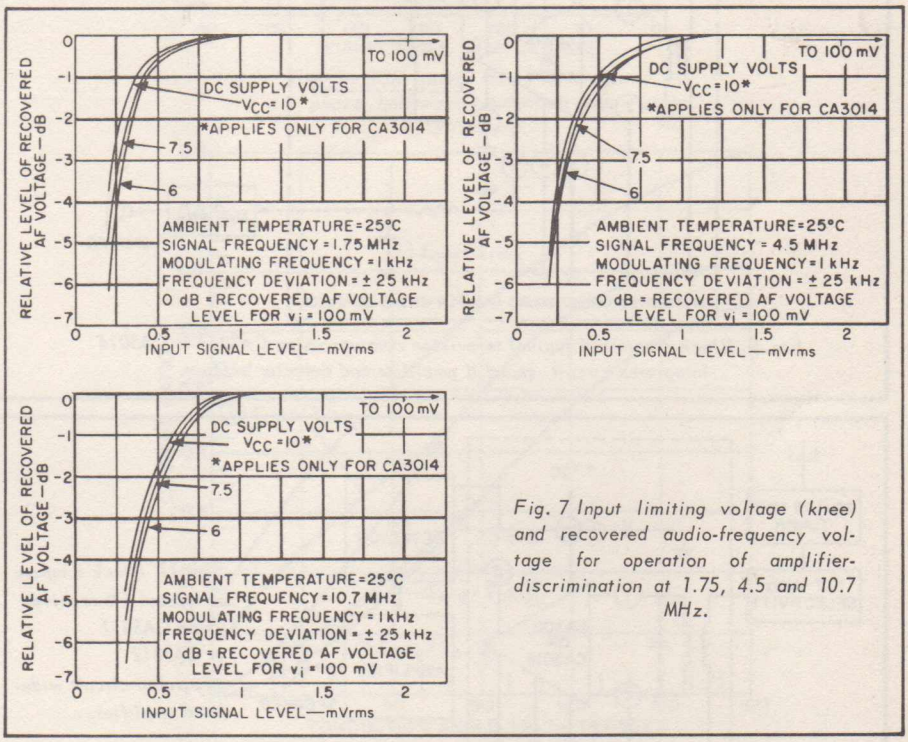


Fig. 7 Input limiting voltage (knee) and recovered audio-frequency voltage for operation of amplifier-discrimination at 1.75, 4.5 and 10.7 MHz.

limiter stages are identical. For operation at 7.5 volts with an ac resistive load impedance of 3000 ohms from terminal 5 to ground, the output voltage at terminal 5 with respect to ground is typically 3 volts peak to peak. Figures 3 through 8 show the significant characteristics of the FM-if amplifier integrated circuits.

Applications

The performance of the integrated circuits in the FM sound channel of intercarrier television receivers and in the if-amplifier-limited-detector channel of FM radio receivers is at least equal to that of conventional circuits in every characteristic, and is superior in many of them. In particular, the AM rejection ratio (more than 50 dB) of the integrated circuits is so large that it cannot be measured with commercial FM-AM signal generators because of incidental phase modulation of the generators. The block diagram in Figure 9 shows the use of the CA3014 amplifier-discriminator in the sound channel of an intercarrier television receiver. (Details of discriminator transformer shown in Figure 9 are given in Figure 10) Figure 11 shows the use of the CA3011 or CA3012 wide-band amplifier in the 10.7-MHz if-amplifier channel of an FM broadcast receiver.

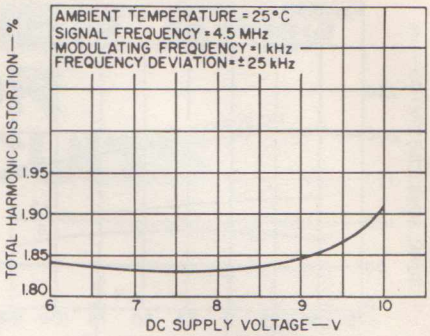


Fig. 8 Total harmonic distortion as a function of dc supply voltage.

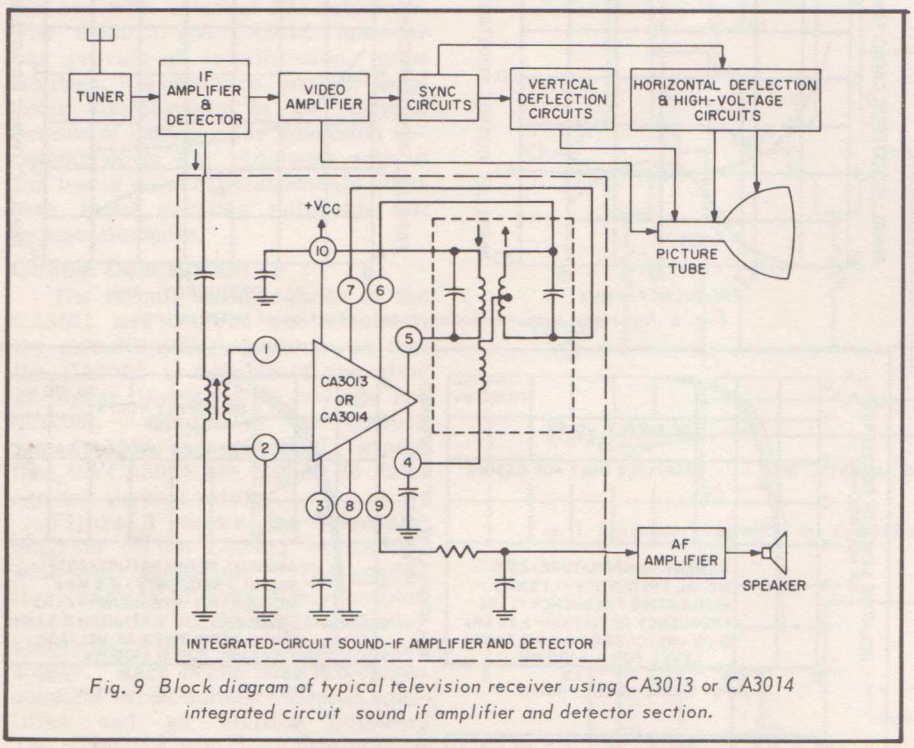


Fig. 9 Block diagram of typical television receiver using CA3013 or CA3014 integrated circuit sound if amplifier and detector section.

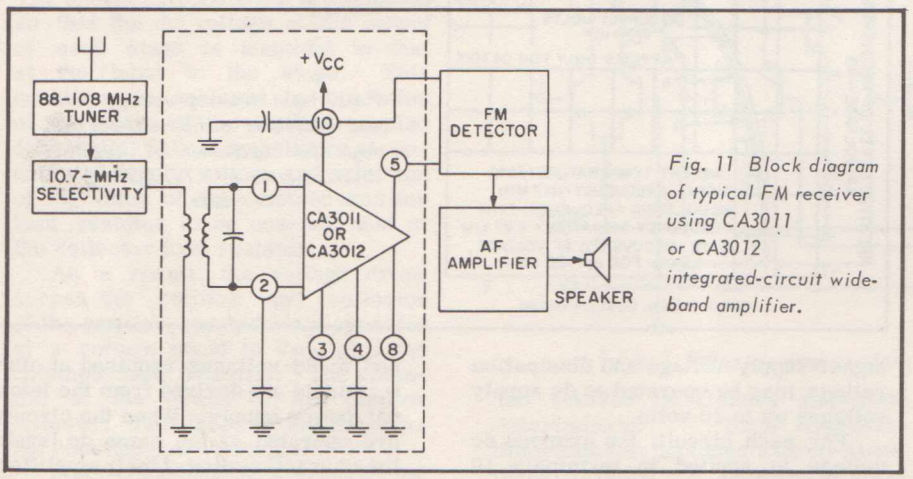
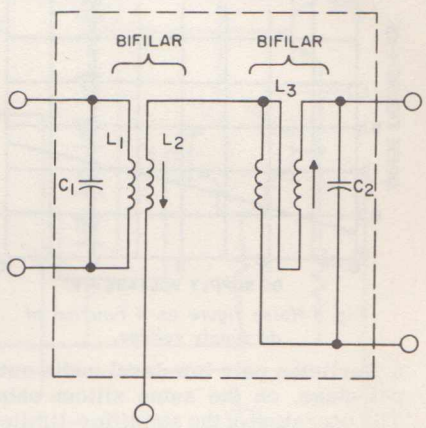


Fig. 11 Block diagram of typical FM receiver using CA3011 or CA3012 integrated-circuit wide-band amplifier.



* Registered Trade Mark, Phelps-Dodge Copper Products
▲ Wound bifilar
▼ Two sections bifilar wound; bifilar turns = ½ total turns

▪ At this frequency, TRW Type No. 21685, or equiv., may be used for discriminator transformer

• At this frequency, TRW Type No. 21590-R1, or equiv., may be used for discriminator transformer.

Discriminator-Transformer Construction Details

Coil-form outside diameter = 7/32 inch.
Slugs: Radio Industries, Inc., Type "E" material, or equiv.
Wire Type: GRIPEZE,* or equiv.

f	Size	Turns			C_1	C_2
MHz	AWG#	L_1▲	L_2▲	L_3▼	pF	pF
1.75	36	44	20	44 total	820	820
4.5▪	40	18	7	22 total	560	330
10.7•	36	18	18	18 total	100	100

Fig. 10 Details of discriminator transformer shown in Figure 9.

• *WITH ACKNOWLEDGEMENT TO RCA*

CIRCUIT FACTOR CHARTS FOR THYRISTOR APPLICATIONS

by B. J. Roman and J. M. Neilson

In the design of circuits using thyristors (SCRs and triacs), it is often necessary to determine the specific values of peak, average, and rms current flowing through the device. Although these values are readily determined for conventional rectifiers, the calculations are more difficult for thyristors because the current ratios become functions of both the conduction angle and the firing angle of the device.

This Note presents charts that show several current ratios as functions of conduction and firing angles for some of the basic SCR and triac circuits. Examples are given of the use of these charts in the design of half-wave, full-wave ac, full-wave dc, and three-phase half-wave circuits using thyristors. Current and voltage waveforms for the various circuits are also included, as well as curves of per-cent ripple in load current and voltage.

Current-Ratio Curves

Fig. 1, 2, and 3 show current-ratio curves for a single-phase half-wave SCR circuit with resistive load, a single-phase SCR or triac full-wave circuit with resistive load, and a three-phase half-wave SCR circuit with resistive load, respectively. These curves relate average current I_{avg}, rms current I_{rms}, and peak current I_{pk} to a reference current I_o. This reference current I_o is a constant of the circuit equal to the peak source voltage V_{pk} divided by the load resistance R_L; it represents the maximum value that the current can obtain and corresponds to the peak of the sine wave. The peak current I_{pk} is the current which appears at the thyristor during its period of forward conduction. For conduction angles greater than 90 degrees, I_{pk} is equal to I_o; for conduction angles smaller than 90 degrees, I_{pk} is smaller than I_o.

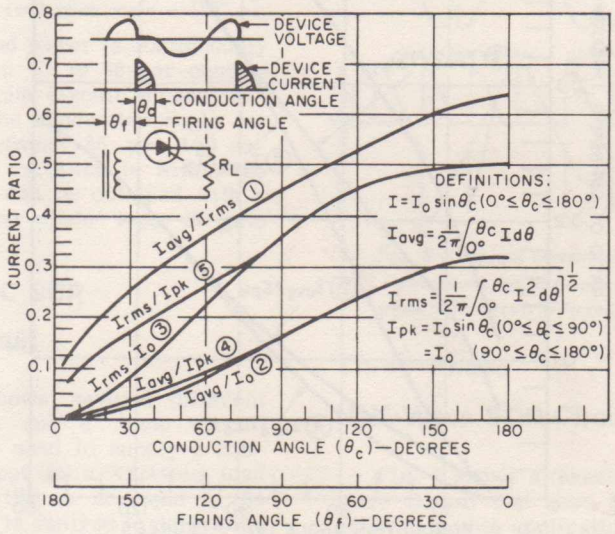


Fig. 1 - SCR current ratios for single-phase, half-wave conduction with resistive load.

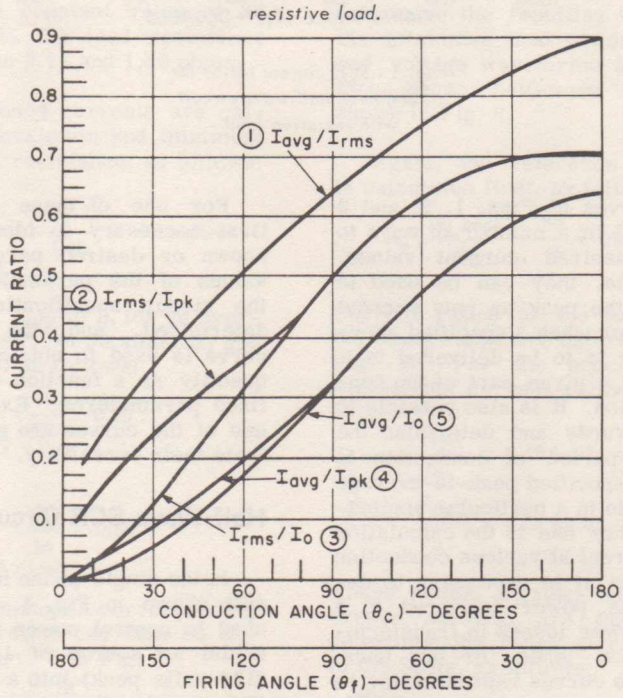


Fig. 2 - SCR or triac current ratios for single-phase, full-wave conduction with resistive load.

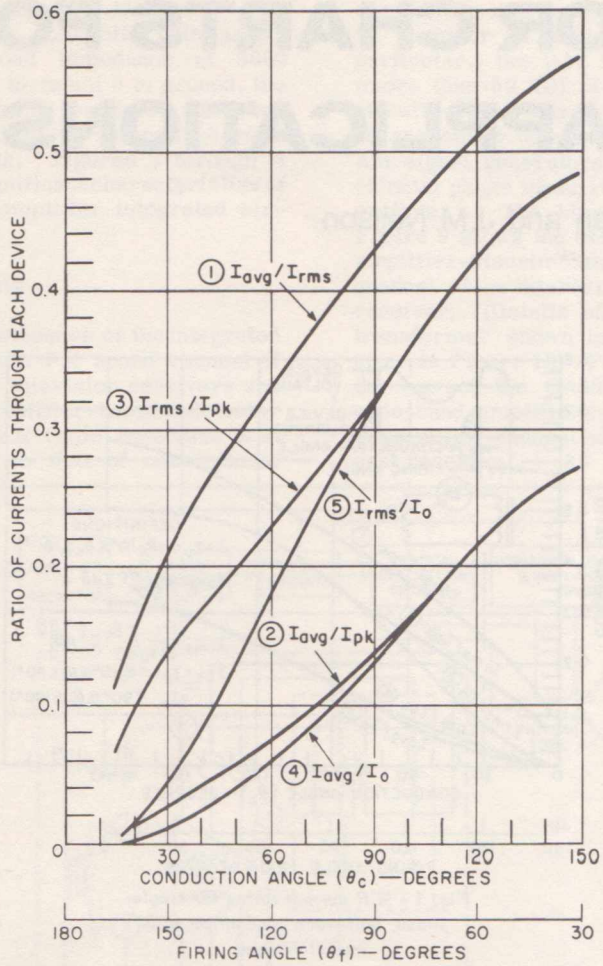


Fig. 3 - SCR current ratios for three-phase half-wave circuit with resistive load.

The curves of Figs. 1, 2, and 3 can be used in a number of ways to calculate desired current values. For example, they can be used to determine the peak or rms current in a thyristor when a specified average current is to be delivered to a load during a given part of the conduction period. It is also possible to work backwards and determine the necessary period of conduction to maintain a specified peak-to-average current ratio in a particular application. Another use is the calculation of rms current at various conduction angles when it is necessary to determine the power delivered to a load, or power losses in transformers, motors, leads, or bus bars. Although the curves represent device currents, they are equally useful for calculation of load current and voltage ratios.

For use of these curves, it is first necessary to identify the unknown or desired parameter. The values of the parameters fixed by the circuit specifications are then determined, and the appropriate curve is used to obtain the unknown quantity as a function of two of the fixed parameteres. Examples of the use of the curves are given to illustrate their versatility.

Half-Wave SCR Circuit

In the single-phase half-wave circuit shown in Fig. 4, an 2N3897 is used to control power from a sinusoidal ac source of 120 volts rms (170 volts peak) into a 2.8 ohm load. This application requires a load current which can be varied from 2 to 25 amperes. It is necessary to determine the range of conduction angles required to obtain this range of load current.

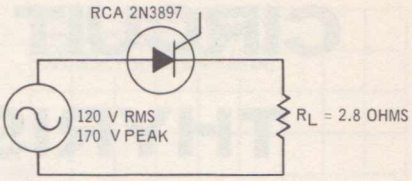


Fig. 4 - Half-wave SCR circuit.

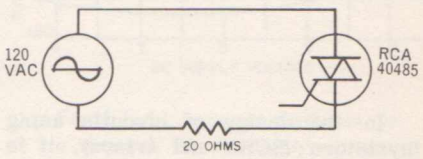


Fig. 5 - Full-wave triac control circuit.

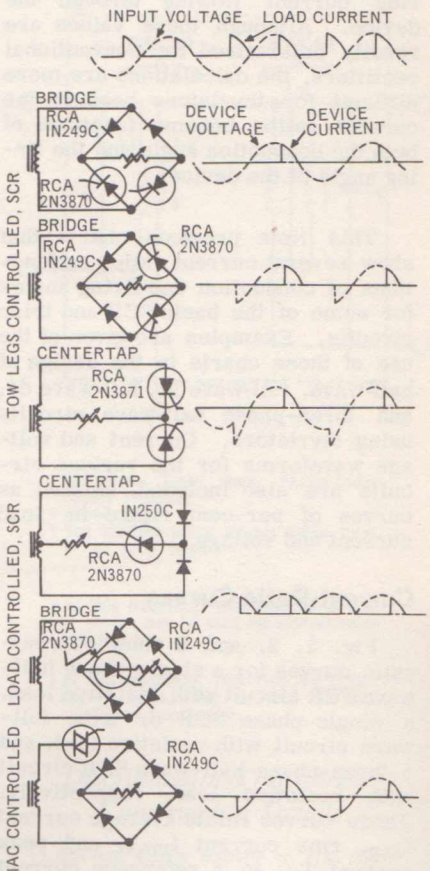


Fig. 6 - Typical current and voltage waveforms for single-phase, full-wave thyristor circuits with resistive load.

The reference current I_o is first calculated, as follows:

$$I_o = \frac{V_{pk}}{R_L} = \frac{170}{2.8} = 61 \text{ amperes}$$

The ratio of rms current I_{rms} to I_o is then calculated for the maximum and minimum load-current requirements, as follows:

$$(I_{rms}/I_o)_{max} = (25/61) = 0.41$$

$$(I_{rms}/I_o)_{min} = (2/61) = .033$$

The conduction angles corresponding to the ratios can then be determined by use of curve 3 in Fig. 1:

$$\theta_{c\,max} = 106^\circ$$

$$\theta_{c\,min} = 15^\circ$$

Full-Wave AC Triac Circuit

Fig. 5 shows a circuit in which an RCA-40485 triac is used to control the power to a 20 ohm resistive load. It is desired to find the range of conduction angles the gate circuit must be capable of supplying to provide continuous variation in load power between 5- and 97-per cent of the full power which the load could draw.

Full power P is given by

$$P = \frac{V_{rms}^2}{R_L} = \frac{120^2}{20} = 720 \text{ watts}$$

Therefore, the 5- and 97-per-cent power points are as follows:

$$P_5 = 36 \text{ watts}$$

$$P_{97} = 698 \text{ watts}$$

The rms current corresponding to each point is given by

$$I_5 = \sqrt{P_5/R_L} = \sqrt{36/20} = 1.3 \text{ amperes rms}$$

$$I_{97} = \sqrt{P_{97}/R_L} = \sqrt{698/20} = 5.9 \text{ amperes rms}$$

The reference current I_O is determined as follows:

$$I_o = \frac{V_{peak}}{R_L} = \frac{120 \times \sqrt{2}}{20} = 8.5 \text{ amperes}$$

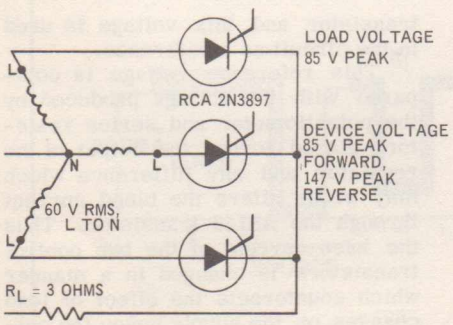


Fig. 7 - Three-phase, half-wave SCR circuit.

The current ratios for the 5- and 97-per-cent power levels then become

at 5%, I_{rms}/I_o = 1.3/8.5 (amperes) = 0.153

at 97%, I_{rms}/I_o = 5.9/8.5 (amperes) = 0.695

Because the circuit shown in Fig. 5 is a full-wave circuit, the calculated current ratios are used in curve 3 of Fig. 2 to determine the required conduction angles:

at 5% power, conduction angle = 35°

at 97% power, conduction angle = 150°

Thus, the load power is continuously variable from 5- to 98-per-cent of full load if gate circuit is constructed so that the conduction angle can be varied between 35 and 150 degrees. This variation is within the range which can be obtained with a simple trigger-diode type of gate circuit.

Full-Wave DC SCR or Triac Circuit

Fig. 6 shows several different SCR circuits and a triac circuit which can be used to supply a constant dc output to a variable load resistance with an ac input of 64 volts rms. It is desired to determine the variation in conduction angle required to maintain the average load current at a constant value of 30 amperes while the load resistance varies between 0.12 and 1.80 ohms.

The reference currents are calculated for maximum and minimum values of load resistance, as follows:

$$I_{o\,min} = \frac{V_{peak}}{R_{L\,max}} = \frac{64\sqrt{2}}{1.80} = 50 \text{ amperes}$$

The ratios of I_{avg} to I_O for an average load current of 30 amperes are then calculated as follows:

$$\frac{I_{avg}}{I_{o\,max}} = \frac{30}{750} = 0.40$$

$$\frac{I_{avg}}{I_{o\,min}} = \frac{30}{50} = 0.60$$

The conduction angles corresponding to these two ratios can then be obtained from curve 5 in Fig. 2.

$$\theta_{c\,min} = 28^\circ$$

$$\theta_{c\,max} = 153^\circ$$

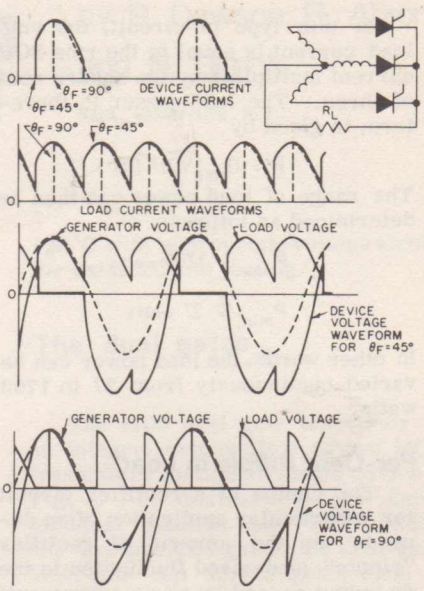


Fig. 8 - Typical current and voltage waveforms for three-phase, half-wave SCR circuit with resistive load.

Three-Phase Half-Wave SCR Circuit

Fig. 7 shows a three-phase, half-wave circuit that uses three 2N3897 SCRs. In this application, the firing angle can be varied continuously from 30 to 145 degrees. It is desired to determine the resulting variation in the attainable load power. Current and voltage waveforms for SCRs in three-phase, half-wave circuits are shown in Fig. 8.

Again, the reference current I_O is calculated first, as follows:

$$I_o = \frac{V_{L\,peak}}{R_L} = \frac{85}{3} = 28 \text{ amperes}$$

Current ratios at the extremes of the firing range are determined from Fig. 3. For the specified firing angles, the current ratios are given by

$$\frac{I_{rms}}{I_o} = 0.49 \text{ for } 0_f = 30^\circ$$

$$\frac{I_{rms}}{I_o} = 0.06 \text{ for } 0_f = 145^\circ$$

These ratios, together with the reference current, are then used to determine the range of rms current in the SCRs, as follows:

$$I_{rms\,max} = (0.49)(28) = 13.7 \text{ amperes}$$

$$I_{rms\,min} = (0.06)(28) = 1.7 \text{ amperes}$$

In this type of circuit, the rms load current is equal to the rms SCR current multiplied by the square root of three. The load power P, therefore, is given by

$$P = (I_{rms}\sqrt{3})^2 (R)$$

The range of load power can then be determined as follows:

$$P_{max} = 1700 \text{ watts}$$

$$P_{min} = 27 \text{ watts}$$

In other words, the load power can be varied continuously from 27 to 1700 watts.

Per-Cent Ripple in Load

The choice of a rectifier circuit for a particular application often depends on the amount of rectifier "ripple" (undesired fluctuation in the dc output caused by an ac component) that can be tolerated in the application. Fig. 9 shows per-cent ripple in load current and voltage for single-phase half-wave, single-phase full-wave, and three-phase half-wave thyristor circuits.

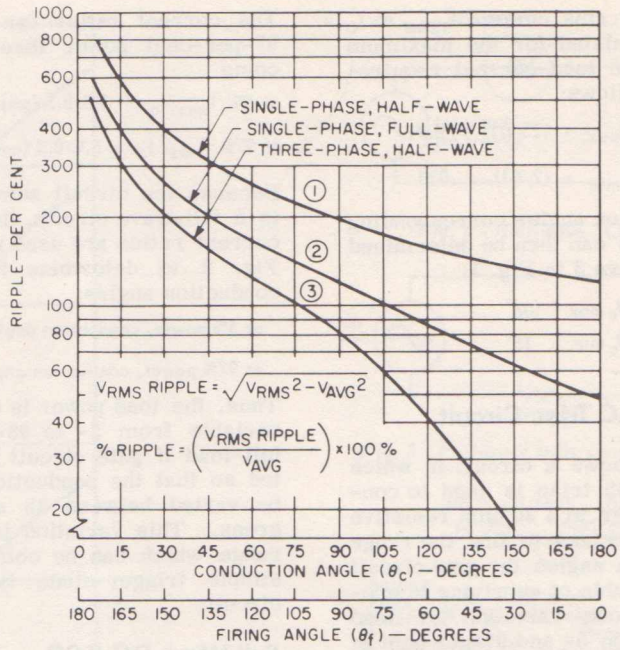
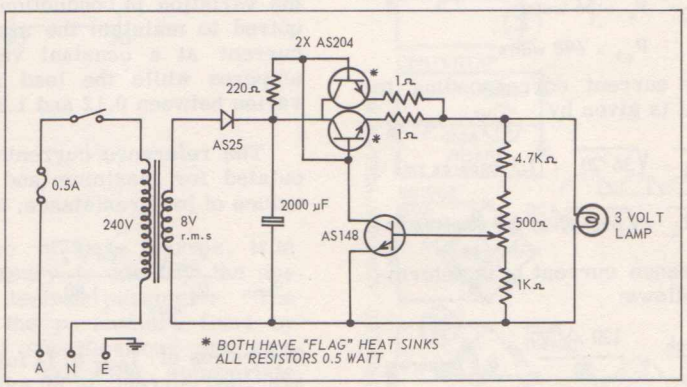


Fig. 9 - Output ripple in thyristor circuits as a function of conduction and firing angles.

3 VOLT REGULATED POWER SUPPLY

Recently the A.W.V. Applications Laboratory received a request for a 3V, mains operated regulated power supply to replace ordinary torch cells used in an Auroscope. An Auroscope is an instrument used by veterinary surgeons for examining the ears of animals. The torch cells operate a high intensity lamp which is rather critical as to the voltage applied to it.

Although the simple regulated 3 volt power supply design described in this note was primarily intended for use with the Auroscope it has many other applications. The unit was designed to provide a nominal 3 volts at 300 milliamps. The output voltage is maintained to within ± 0.1 volt for a load variation of ± 50mA around the mean 300mA and a mains voltage variation of ± 15%. A potentiometer allows the output voltage to be adjusted to the nominal 3.0 volts and in addition provides a variation over the range of 2.5 to 3.5 volts approximately. With the potentiometer set to minimum output voltage the dissipation in the control transistor is a maximum and under these conditions the unit can be operated safely in an ambient temperature up to 65 degrees C. The maximum load current the power supply will handle is 350mA. The output voltage variation for the output current range 0-350mA is ± 0.3 V.



Circuit Description

The power transformer supplies 8V r.m.s. to the rectifier. The filtered output voltage is then applied to the two parallel connected AS204 series control transistors.

The turn-on base to emitter voltage of a silicon transistor is relatively constant for a particular transistor and this voltage is used in the circuit as a reference.

This reference voltage is compared with the voltage produced by the potentiometer and series resistors placed across the output of the regulator and any difference which may occur alters the bleed current through the AS148 transistor. Thus the base current of the two control transistors is changed in a manner which counteracts the effect of load changes on the supply hence the output voltage is maintained relatively constant.

Understanding and using the dual-gate MOSFET

by R. Dawson, R. Ahrons and N. Ditrick

RCA, Somerville, N.J.

The MOS dual-gate field-effect transistor is ideally suited for high-frequency applications. In effect, it is the solid state analog of the multi-grid vacuum tube and is very useful in performing multigrid functions. It has already been successfully used for r-f and i-f bandpass amplifiers, mixers and demodulators. Many other applications are also possible. Addition of gate No. 2 adds little to its cost, eliminates many circuit components, and gives it many performance advantages.

Utility of the MOS dual-gate relies, to some extent, on properties common to field effect devices:

- Low third-order distortion.
- Low noise at high frequency.
- Small sensitivity to overload.

Low third-order distortion in the transfer characteristics gives an order of magnitude improvement in cross-modulation voltage over bipolar transistors and makes the FET comparable to a vacuum tube. Observed noise figures for FETs are generally comparable to those for bipolar transistors in h-f applications; whereas sensitivity to overload isn't as great as the bipolar's, which suffers under forward bias attenuation. Overload capability of the MOS device is greater than a bipolar device because the driving point admittance changes little during AGC. Thus, detuning isn't a problem and the noise figure remains low over a substantial AGC range[1].

MOS vs. junction gate FET

Although the MOSFET retains a high input impedance for either polarity of gate voltage, if the rather high gate breakdown voltage is exceeded, the MOS device is easily destroyed. In comparison, the junction gate FET dissipates more energy in the breakdown region before destruction. The MOS device, however, with its generally higher gate breakdown is less susceptible to burnout in a circuit in which the input is tuned or has a low impedance. Although a diffused gate affords a more rugged device, its use results in a higher drain-to-gate feedback capacitance than that of an MOS device of equivalent transconductance. Thus a higher stable power gain can be obtained with the MOS.

Until recently, MOS units have shown long term drift instabilities; now, improved processes for making them have yielded devices stable at 125 °C with appropriate voltage stress for extended life testing.

The dual gates

The MOS dual gate transistor is an integral combination of two MOS transistors forming a single device[2], Fig. 1. In contrast to the four-terminal junction gate FET[3] which has two parallel gates, the dual-gate MOS has two series gates each of which has independent control of the device characteristics. The isolated series elements control the flow of electrons from source to drain.

Performance of the dual gate transistors in cascode form can be seriously degraded by the center point capacitance (region C in Fig. 1). If the circuit were composed of planar bipolar transistors, the center point capacitance would be dominated by a large collector capacity. If vacuum tubes were used, both filament and cathode would be floating above ground potential and the result again would be large center point capacity. With MOS transistors, this capacity can be minimized by making the central region a very narrow buried junction without any contact. If the R-C cut-off frequency of the centerpoint were lower than the operating frequency, both the power gain and noise figure would be degraded. Tuning this capacity can improve these characteristics, but an additional tuned circuit is needed. At 400 MHz the effect of this capacity on dual gate MOS performance appears to be negligible; at 800 MHz, sufficient power gain has been achieved with experimental units.

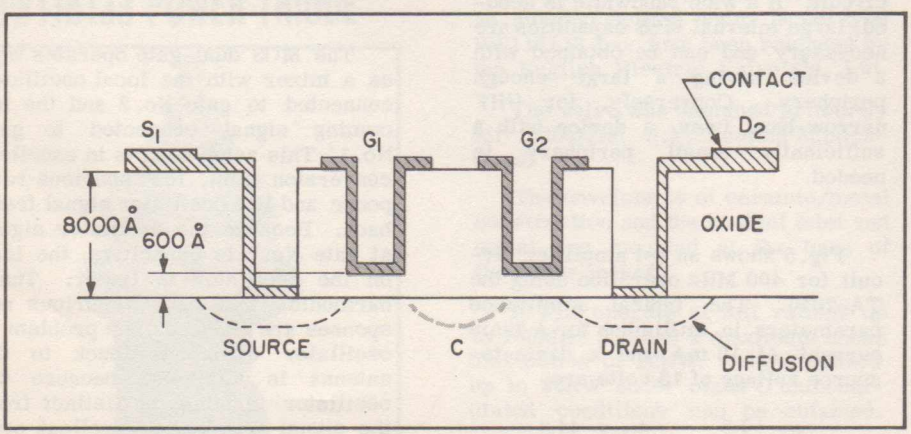


Fig. 1: Cross section of the MOS dual gate transistor. It is an integral combination of two MOS transistors forming a single device.

Fig. 2 shows the drain characteristics with respect to gate No. 1 voltage. The gate No. 2 voltage is held at a fixed value. These characteristics resemble those of the vacuum tube pentode. The transconductance characteristic is shown in Fig. 3.

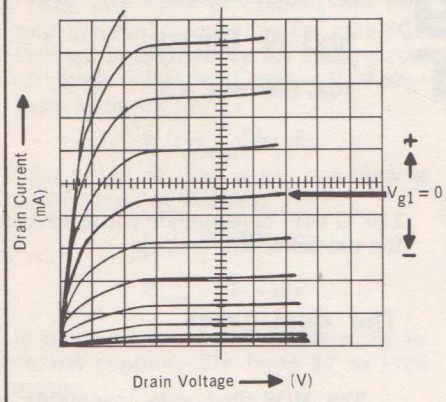


Fig. 2 (left): Drain characteristics of MOS dual gate ransistor. Vertical trace = 2mA/div., horizontal trace = 2V/div., Vg1 = 0.2 V/step, and Vg2 = +3V.

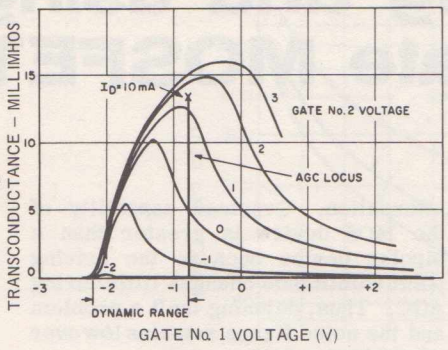


Fig. 3 (above): Typical locus for AGC and the dynamic range of the signal gate. Transconductance characteristic is plotted as a function of gate No. 1 voltage at various values of gate No. 2 voltage with drain voltage held constant.

Applications as an r-f amplifier

As an r-f amplifier, the TA-7010 MOS dual-gate has a typical unconditionally stable power gain of 14 dB with a noise figure of 4.5 dB at 400 MHz. Experimental UHF units had a maximum stable power gain of 15 dB with a noise figure of 3.6 dB at 800 MHz. As an r-f amplifier, the dual-gate unit is used as a grounded source amplifier driving an r-f grounded gate amplifier. Because gate No. 2 is at r-f ground potential, it forms a shield between drain and input signal gate and produces low feedback capacitance of 0.01 to 0.02 pF. Gate No. 2 can also be used as the input for AGC, eliminating the need for an r-f choke.

In r-f transistor design many factors must be considered: power gain, noise figure, r-f stability, AGC range, cross modulation distortion, dynamic range and selectivity.

Considerihg these factors the MOS dual-gate transistor provides the best compromise. A good r-f amplifier possesses adequate power gain and low noise figures. If the feedback capacitance is low, good r-f stability can generally be obtained with neutralization. With the MOS dual-gate device, the feedback capacity is low enough that neutralization isn't needed, at least up to 800 MHz. With low feedback, an AGC range of greater than 40 dB is obtainable.

Cross-modulation distortion of the MOS dual-gate is low over the complete AGC range. Fig. 4 shows interfering signal for 1% cross-modulation distortion as a function of attenuation.

Because the MOS dual-gate is shut off by AGC action applied at the second gate, the input swing can be large without distortion; thus the device has excellent dynamic range (Fig. 3).

Selectivity or bandwidth is a function of the device's inherent stray capacities and L-C ratio of the tuned circuit. If a wide bandwidth is needed, large internal MOS capacities are necessary and can be obtained with a device having a large enough periphery. Conversely, for UHF narrow-band uses, a device with a sufficiently small periphery is needed.

Fig. 5 shows an r-f amplifier circuit for 400 MHz operation using the TA-7010. The typical admittance parameters in millimhos for a drain current of 10 mA and a drain-to-source voltage of 13 volts are:

$gis = 7.8$	$bis = 14.0$
$gos = 0.46$	$bos = 5.2$
$gfs = 6.0$	$bfs = -16.0$

From this a maximum available power gain of 13 dB and a Linville Stability Factor of C = 0.125, were calculated.

$$MAG = \frac{|Y_{21}|^2}{4\ gis\ gos} \qquad C = \frac{|Y_{21}\ Y_{12}|}{2\ gis\ gis - Re\ (Y_{21}\ Y_{12})}$$

The low value of C < 1 shows that the device is unconditionally stable: hence, neutralization isn't needed. The potential of the MOS has been shown by experimental devices which gave 9 dB unilateralized power gain at 800 MHz.[5] Replacing the r-f ground in the gate No. 2 circuit with a tuned circuit permits adjustment between unilateralization and oscillation.[6] At a stability factor of C = 0.7, a power gain of 12 dB at 800 MHz has been obtained.

I-f application

The i-f amplifier, like the r-f amplifier, is a bandpass device. Again, gate No. 1 becomes the signal gate and gate No. 2 becomes the gate at r-f ground. All stages of the amplifier may have a common AGC without need of decoupling chokes. Furthermore, neutralization components are not needed. The TA-7010 operates well in all stages except the last. If the signal level at the last device is high enough, a large size (periphery) MOS may be needed. The i-f strip requires a minimum of components. Intermodulation distortion is low for the same reasons discussed with regard to cross-modulation distortion.

Mixer application

The MOS dual-gate operates well as a mixer with the local oscillator connected to gate No. 2 and the incoming signal connected to gate No. 1.[7] This setup results in excellent conversion gain, low spurious response and low oscillator signal feedback. Because the oscillator signal at gate No. 2 is capacitive, the load on the oscillator is linear. Thus, harmonics that cause spurious responses are reduced. The problem of oscillator signal feedback to the antenna is alleviated because the oscillator terminal is distinct from the signal terminal. Excellent conversion transconductance results from the linear, steep variation of

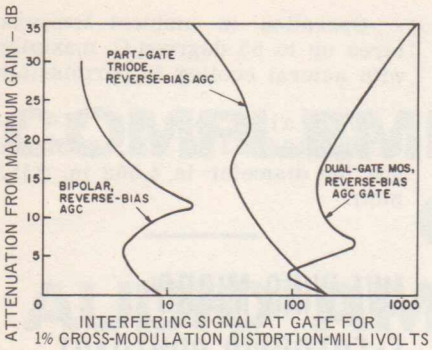


Fig. 4: These curves indicate that an interfering signal of greater than 100 mV can be tolerated over most of the 35 dB attenuation range shown.

transconductance (Fig. 3). Measurements of conversion transconductance at 100 MHz indicate a value of 2200 μmhos with a maximum conversion gain of 22 dB.

Demodulators

The quadrature detector and the osillating detectors for FM and SSB detectors are good potential applications for the MOS dual-gate FET. In the case of the quadrature detector, the quadrature coil can be placed in the gate No. 2 circuit. Operation of this detector to obtain enough signal for the quadrature coil depends upon the gate No. 2-to-center point capacitance. Devices have not yet been optimized for this operation.

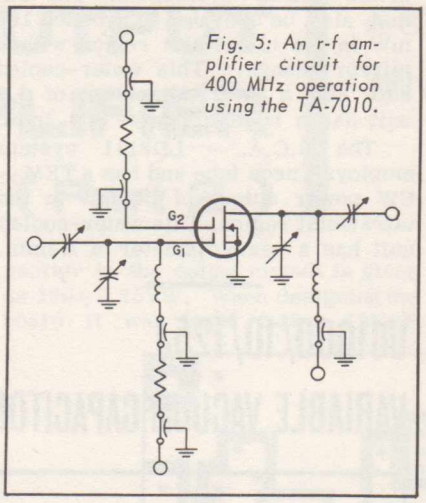


Fig. 5: An r-f amplifier circuit for 400 MHz operation using the TA-7010.

The balanced demodulator requires tow double-gate units. With present MOS technology it is possible to make two double-gate units on a single silicon chip to obtain optimal balance.

Acknowledgements

Development of the MOS dual-gate transistor involved the work of many persons associated with RCA, in particular: L. Jacobus, F. Carlson, E. McKeon, W. Babcock, R. Glicksman, M. Mitchell, and S. Katz. The authors are indebted for the support of the U.S. Army Electronics Command, Fort Monmouth, N.J., during the early investigation of the MOS dual-gate transistor.

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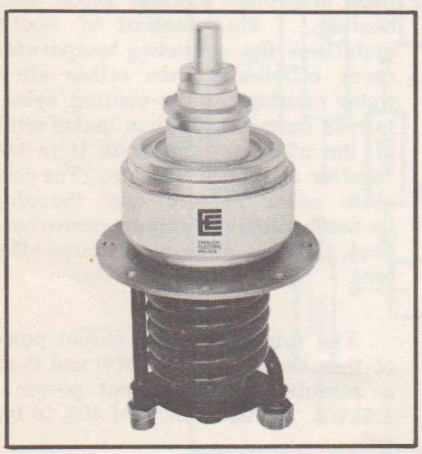
7. Kleinman, H., "Application of Dual-Gate MOS Field-Effect Transistors in Practical Receivers." *IEEE Trans. on Broadcast TV Receivers*, July 1967.

NEWS & NEW RELEASES

BW1181J3 POWER TRIODE



A new water cooled triode with an integral helical water jacket type BW1181J3 has just been released by the English Electric Valve Co. Ltd.

The valve was designed primarily for industrial R.F. heating applications.

The envelope is of ceramic/metal construction and the coolant inlet and outlet are mounted at the base of the water jacket.

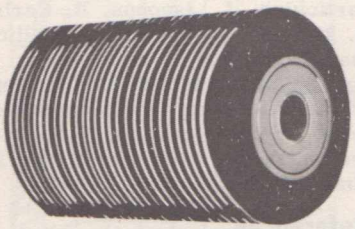
It will operate at full ratings up to 100MHz and has a maximum anode dissipation of 12KW. Output powers up to 26KW under class C unmodulated conditions can be obtained.

The BW1181J3 is physically interchangeable with the BW1169J3, having overall dimensions of 10 in. (266.7mm) length and 5 in. (133.4mm) diameter.

RCA HEAT PIPES

R.C.A. have released three developmental heat pipes. A heat pipe is an evacuated enclosure with a capillary structure (wick) along its inside surfaces and contains a relatively small amount of fluid which saturates the capillaries. At the desired operating temperature, the fluid is evaporated at the heat input end (evaporator end) and develops a substantial vapor pressure. The vapor then condenses at the heat output

end (condenser end) and the condensate is "pumped" by capillary action (through the wick) to the evaporator end.



The three types that have been released are J15105, J15120 and J15121. The J15105 heat pipe has an overall length of 14.75" and diameter of 0.438" with a maximum thermal power rating of 1000W at an operating temperature of 900 degrees C.

The J15120 and J15121 are heat pipes with integral radiators which improve their heat dissipation over that of a standard-pipe. The J15120 permits a dissipation of thermal power up to 25,000 watts at 160 degrees C. with an air flow of 1200 cubic feet per minute. The J15121 has been designed principally for use with power transistors and will dissipate 150 watts at 99 degrees C. with natural convection and 1000 watts at 125 degrees C. with forced-air cooling.

GAS LASER SYSTEMS

A series of four new gas laser systems have been announced by R.C.A.

The first system the LD2125 is said to be the worlds smallest pulsed, argon laser system for hologram readout applications. The LD2125 employs an argon tube and has a fundamental transverse mode TEM_{oo} peak power output of 50 milliwatts in the visible wavelengths. The natural air-cooled unit has been a beam diameter of 0.6 millimeter operating at a repetition rate up to 60Hz with a pulse width of approximately 50 microseconds.

Among the other new laser systems introduced by R.C.A. were a 10 milliwatt continuous-wave argon unit; a 400 milliwatt visible and 100 millwatt ultraviolet krypton laser; and a 50 milliwatt ultraviolet CW neon unit.

The RCA - LD2108 laser system employs an argon tube and has a TEM_{oo} CW power output of 10 mW in the visible wavelengths. This forced-air cooled unit has a beam diameter of 0.5mm.

The RCA - LD2127 laser system employs a krypton tube and has a TEM_{oo} CW power output of 400 mW in the visible wavelengths. The unit may also be operated to produce 100 mW in the ultraviolet region with a mirror change. This water-cooled unit has a beam diameter of 1.2 unit has a beam diameter of 1.2mm.

The R.C.A. - LD2111 system employs a neon tube and has a TEM_{oo} CW power output of 50 mW in the ultraviolet region. This water-cooled unit has a beam diameter of 1.2mm.

UC1000/10/125J VARIABLE VACUUM CAPACITOR

English Electric Valve Co. Ltd. have added a further type to their range of ceramic variable vacuum capacitors.

The type UC1000/10/125J has a capacitance range of 25pF to 1000pF, maximum r.f. peak working voltage rating of 10kV and maximum r.f. current rating (r.m.s.) of 125A at frequencies up to 27MHz.

Operation in ambient temperatures up to 55 degrees C. maximum with natural cooling is permissible.

Overall length of the UC1000/10/125J is 8in. (203.2mm) and the diameter is 4.562 in. (115.9 mm).

AWA WINS MICRO ELECTRONIC CONTRACT

The Department of Supply has awarded a three year contract to A.W.A. for the development of micro electronic circuit technology in Australia. The contract will help to expand the work that has already been done in this field by the A.W.A. Advanced Devices Laboratory since its inception in 1965. Last year the laboratory produced Australia's first micro circuit and since that time have been manufacturing both digital and linear circuits.

M5048 EEV MAGNETRON

The English Electric Valve Co. Ltd. have commenced production of a new tunable pulse magnetron M5048 which has been designed for use in high power radar equipment.

The M5048 has a frequency coverage of 2900MHz to 3000MHz. It is the first of four tunable magnetrons covering a frequency range from 2700 MHz to 3100MHz in increments of 100MHz.

The anode is vapour cooled by an integral boiler, fitted with a thermal fuse to protect against anode overheating. This method of cooling stabilises the operating temperature more efficiently than either air or water cooling. As the cooling system is less complicated than that of either of the other two methods it is both smaller and more reliable. The complete radar system can therefore be mechanically simpler, more compact, lighter, quieter and more efficient.

The minimum peak output power of this magnetron is 1MW and it has a minimum mean output power of 1.5kW. An efficiency of 45% is typical.

2 WATT COMPLEMENTARY OUTPUT AUDIO AMPLIFIER (Part 2.)

W. R. EASON

A.S.T.C., A.M.I.E. (Aust.), M.I.R.E.E.

AWV Applications Laboratory.

As mentioned in the first part of this article in the May issue a circuit board has been designed to suit one channel of this amplifier.

The overall dimension of the board is 3¼" × 2¾". All the amplifier components except the input potentiometer and power transformer are mounted on the board. The drawing in figure 1 is an actual size template used to make the board from blank printed circuit material. Fig. 2 is a top view of the board showing the location of the various components and the aluminium heat sink for the AS128.

The value of the electrolytic capacitor in the output circuit is given as 100μF 15VW. When designing the board it was found that a 125μF 15VW capacitor was physically more suitable and gave a slight improvement in low frequency performance.

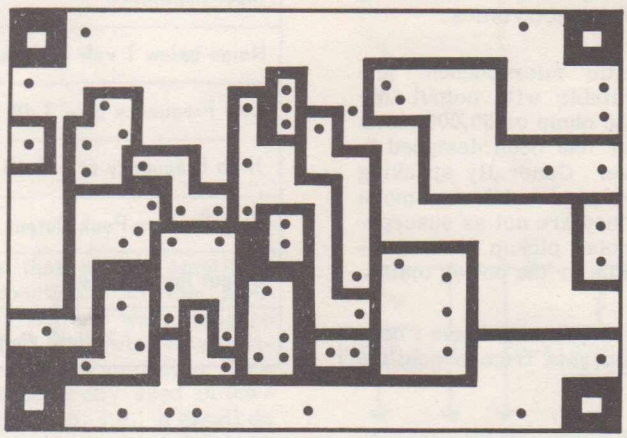


Fig. 1 Actual size Template of Board.

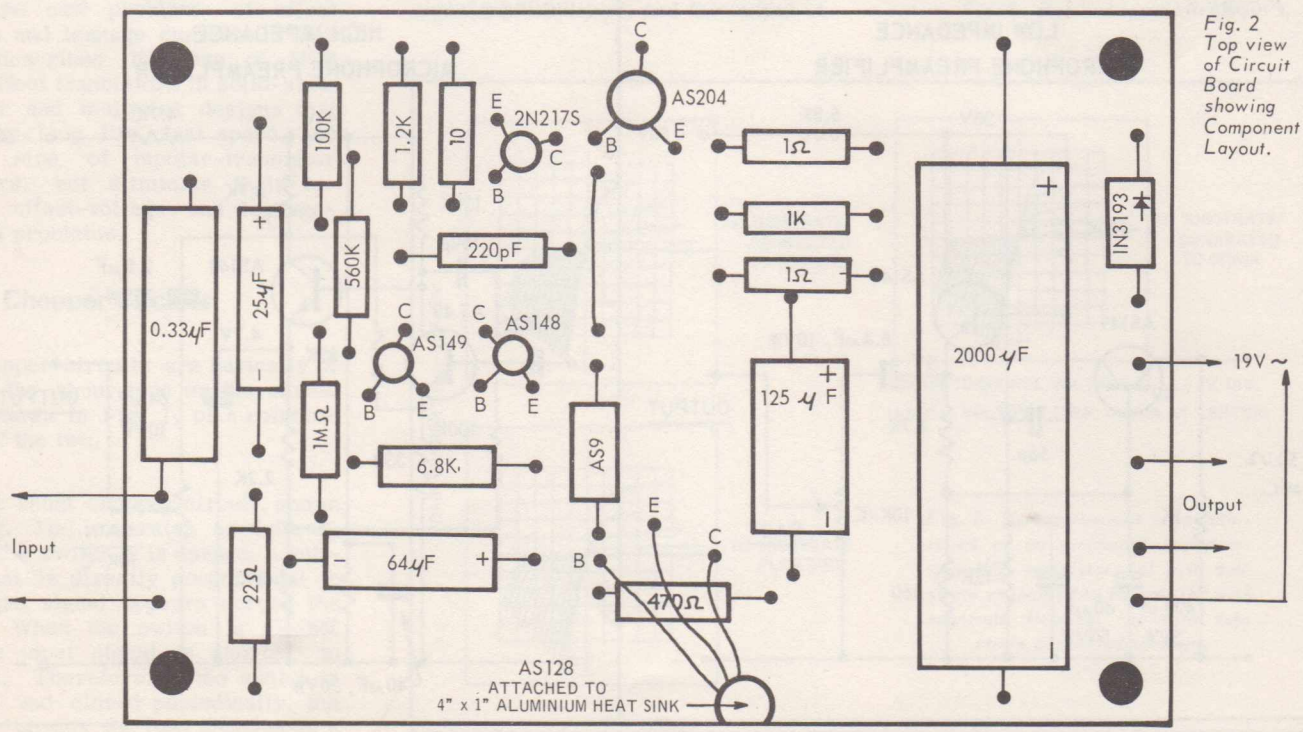


Fig. 2 Top view of Circuit Board showing Component Layout.

MICROPHONE PREAMPLIFIERS

W. R. EASON
A.S.T.C., A.M.I.E. (Aust.), M.I.R.E.E.
AWV Applications Laboratory

A microphone preamplifier is required to suitably terminate the impedance of the microphone and provide sufficient voltage gain to drive the main power amplifier.

This article describes two magnetic microphone preamplifiers designed to be used with the series of power amplifiers described in the May 1967 issue of Radiotronics. They would also be quite suitable for use in front of any amplifiers having similar input characteristics.

As magnetic microphones are normally available with output impedances of 50 ohms or 50,000 ohms a preamplifier has been designed to suit each case. Generally speaking the low impedance units are more desirable as they are not as susceptible to line noise pickup from electrical apparatus or the power mains.

Both preamplifiers have been designed to operate from a positive supply rail of 50 ± 5 volts. Supply potentials outside this range will require adjustments to the value of the series resistor. If the value of this resistor requires to be lowered the bypass filter capacitor should be increased to maintain the original time constant.

Circuit Figure Number	1	2	
Nominal Microphone Impedance	50	50k	ohms.
Voltage Gain (Max. Volume)	54	46	dB
Input Impedance	300	70k	ohms.
Noise below 1 volt RMS Output	70	50	dB
Low Frequency at – 3 dB	50	50	Hz
High Frequency at – 3 dB	15	15	KHz
Max. Peak to Peak Output Voltage	5	5	volts
Output Impendance	25	3k	ohms.

Table 1 Performance specifications of the two preamplifiers.

FIGURE 1

LOW IMPEDANCE
MICROPHONE PREAMPLIFIER

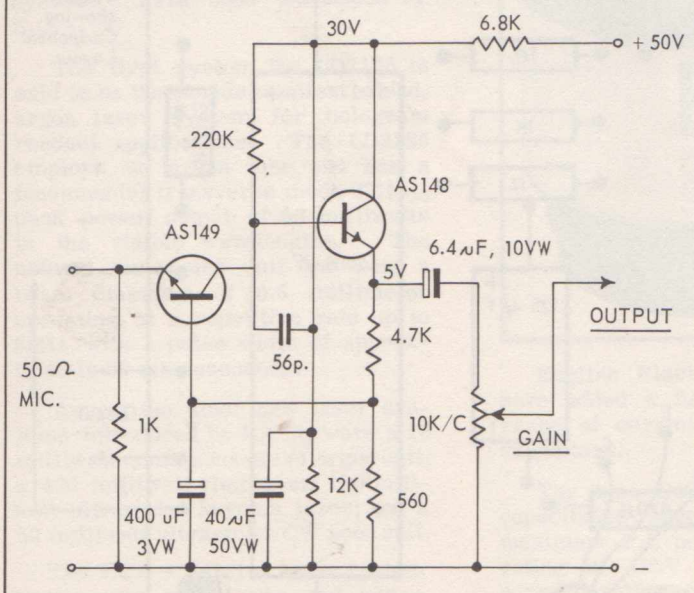
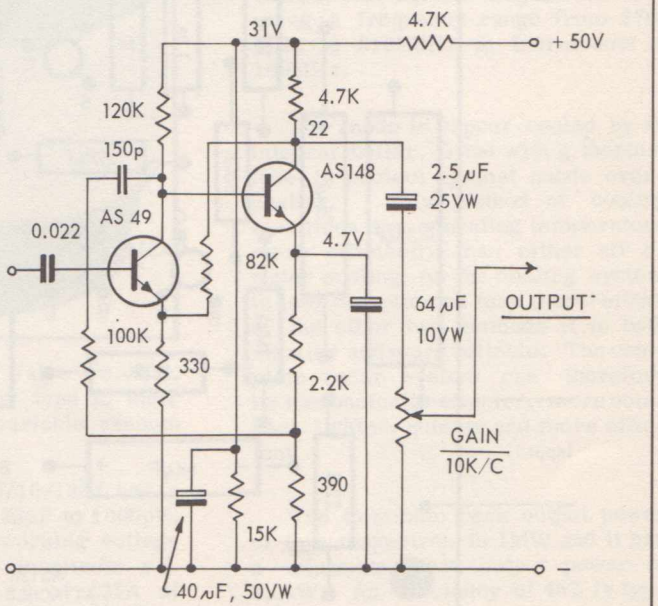


FIGURE 2

HIGH IMPEDANCE
MICROPHONE PREAMPLIFIER



CHOPPER CIRCUITS USING MOS FIELD-EFFECT TRANSISTORS

by F.M. Carlson

Although electromechanical relays have long been used to convert low-level dc signals into ac signals or for multiplex purposes, relays are seriously limited with respect to life, speed, and size. Conventional (bipolar) transistors overcome the inherent limitations of relays, but introduce new problems of offset voltage and leakage currents. This Note describes the use of MOS field-effect transistors in solid-state chopper and multiplex designs that have the long life, fast speed, and small size of bipolar-transistor choppers, but eliminate their inherent offset-voltage and leakage-current problems.

Basic Chopper Circuits

Chopper circuits are basically of either the shunt type or the series type, shown in Fig. 1, or a combination of the two.

The shunt chopper circuit, shown in Fig. 1(a), operates as follows: When the switch S is opened, a voltage that is directly proportional to the input signal appears across the load. When the switch is closed, all the input signal is shorted to ground. Therefore, if the switch is opened and closed periodically, the voltage across the load appears as a square wave that has an amplitude directly proportional to the input signal. This square wave may be highly amplified by a relatively drift-free, stable-gain ac amplifier. This procedure is generally used in low-level dc amplifiers, i.e., a small dc input is chopped, the resulting ac signal is amplified, and the output of

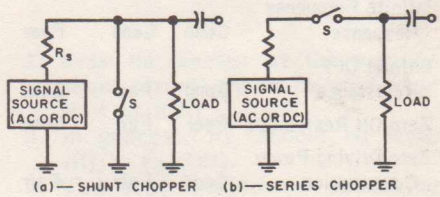


Fig. 1 - Basic chopper circuits.

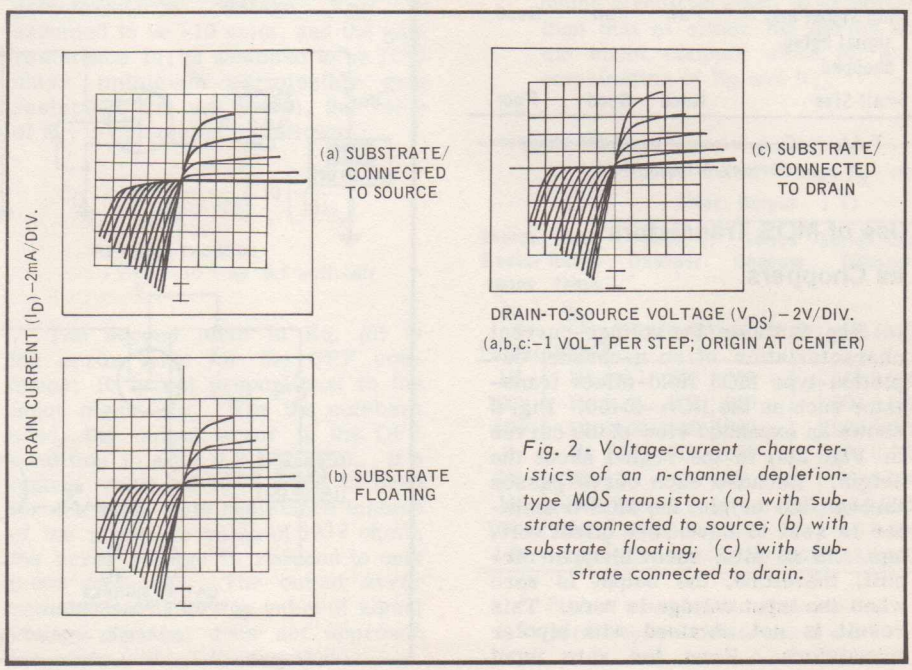


Fig. 2 - Voltage-current characteristics of an n-channel depletion-type MOS transistor: (a) with substrate connected to source; (b) with substrate floating; (c) with substrate connected to drain.

the ac amplifier is rectified to produce a dc output directly proportional to the input.

The series chopper circuit, shown in Fig. 1 (b), can also be used to chop dc signals. This type of circuit is particularly useful in telemetry or other systems in which a signal source such as a transducer is to be connected periodically to a load such as a transmitter.

An ideal chopper is simply an on-off switch that has certain desirable characteristics. Table I lists some of these characteristics, and shows the relative merits of relays, bipolar transistors, and MOS transistors in each area.

Ideal Chopper Characteristics	Available Chopper Devices Compared to Ideal		
	MOS	Bipolar	Electro-mechanical Relay
Infinite Life	Good	Good	Poor
Infinite Frequency Response	Good	Good	Poor
Infinite OFF Resistance	Good	Fair	Good
Zero ON Resistance	Poor	Fair	Good
Zero Driving-Power Consumption	Good	Fair	Fair
Zero Offset Voltage	Good	Poor	Good
Zero Feedthrough between the driving signal and signal being chopped	Fair	Fair	Good
Small Size	Good	Good	Poor

Table I - Comparison of available chopper devices with an ideal

Use of MOS Transistors as Choppers

Fig. 2 shows the voltage-current characteristics of an n-channel depletion-type MOS field-effect transistor such as the RCA-40460. Fig. 3 shows an expanded view of the curves in Fig. 2(a) in the region about the origin. Because each curve passes through the origin, the MOS transistor is said to have zero offset voltage. In an MOS shunt chopper circuit, therefore, the output is zero when the input voltage is zero. This result is not obtained with bipolar transistors. Even for zero input voltage, a bipolar transistor has an offset voltage equivalent to the collector-to-emitter saturation voltage $V_{CE}(sat)$ between its collector and emitter terminals. MOS transistors have no parameter comparable to $V_{CE}(sat)$.

When the gate-to-source voltage V_{GS} is zero, an MOS transistor such as the 40460 has an effective resistance of 200 to 300 ohms between its drain and source terminals. If the gate-to-source is made positive, this resistance decreases to about 100 ohms (typical to 90 ohms for the 40460). No significant increase in gate current occurs when V_{CE} is made positive because the gate of an MOS transistor is insulated from the source-to-drain channel by an oxide layer. (In a junction-gate field-effect transistor, the gate and the channel form a p-n junction, and low gate current can be obtained only when this junction is reverse-biased). When the resistance between the drain and source terminals is low (100 to 300 ohms), an MOS transistor is said to be ON; the drain-to-source channel resistance is then designated as $r_{ds}(ON)$. This ON condition corresponds to the closed-switch condition in the circuits of Fig. 1.

When a negative voltage of about -6 volts or more is applied between the gate and the source of the MOS transistor, the channel resistance

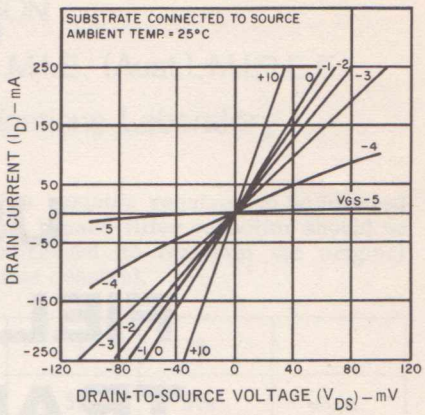


Fig. 3 - Low-level drain current as a function of drain-to-source voltage in an n-channel depletion-type MOS transistor with substrate connected to source.

between drain and source becomes extremely high (typically thousands of megohms). In this condition, which is known as "cut-off" or "pinchoff", it is impractical to measure the channel resistance directly; instead, the leakage current that flows from drain to source is cutoff is normally specified. This current $I_D(OFF)$, is typically 0.1 nanoampere for the 40460. Because $I_D(OFF)$ is measured at a drain-to-source voltage of 1 volt, the equivalent channel resistance is 10,000 megohms. This OFF condition corresponds to the open-switch condition in the circuits of Fig. 1.

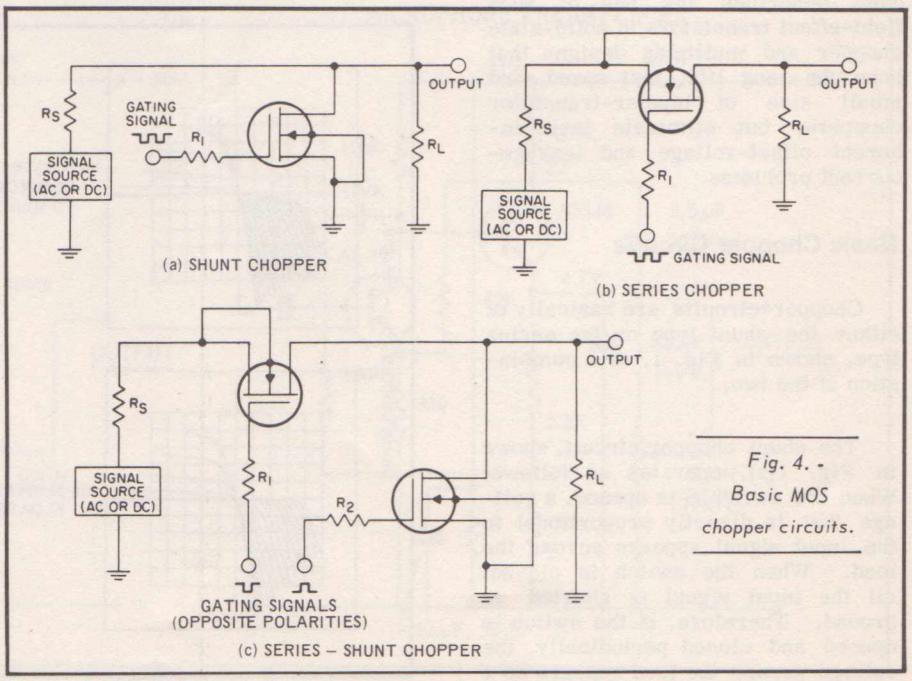


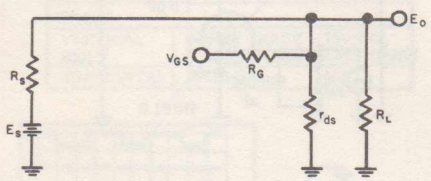
Fig. 4. - Basic MOS chopper circuits.

Fig. 4 shows three basic chopper circuits using the MOS field-effect transistor. The gating signal for the 40460 should swing from zero to at lease -6 volts, and may cover a range as large as ±10 volts. The substrate (and thus the case) of the 40460 transistor is usually connected to the source. However, if the incoming signal to be chopped exceeds -0.3 volt, the substrate must be "floated", connected to the drain, or biased negatively so that the source-to-substrate and drain-to-substrate voltages never exceed -0.3 volt. If this value is exceeded, the substrate, which forms two p-n junctions with the drain and the source, becomes forward-biased and the resulting flow of diode current shunts the incoming signal to ground.

Steady State Conditions

Ideally, when an MOS transistor in a shunt chopper circuit is ON, the output voltage of the circuit should be zero. Because the drain-to-source resistance r_{ds} is some finite value, however, the output cannot reach true zero. Fig. 5 shows an equivalent circuit for steady-state conditions in an MOS shunt chopper. For the ON condition, the output voltage E_O is given by

$$E_O = E_S \left[\frac{\frac{r_{ds} R_L}{r_{ds} + R_L}}{R_S + \frac{r_{ds} R_L}{r_{ds} + R_L}} \right] \quad (1)$$



NOTE: ALTHOUGH RESISTANCE R_G IS ACTUALLY DISTRIBUTED ALONG THE LENGTH OF rds, CONNECTION SHOWN ASSURES A WORST – CASE ANALYSIS.

Fig. 5 - Steady-state equivalent circuit of MOS shunt chopper.

In Eq. (1), it is assumed that the gate leakage resistance R_G is much larger than the drain-to-source resistance r_{ds}. If the load resistance R_G is also much larger than r_{ds}; Eq. (1) can be simplified as follows:

$$E_O = E_S \left[\frac{r_{ds}}{R_S + r_{ds}} \right] \quad (2)$$

For E_O to approach zero, it is necessary that the source resistance R_S be much greater than r_{ds}. The value of E_O is then given by

$$E_O = E_S (r_{ds}/R_S) \quad (3)$$

A typical value for R_S and R_L in an MOS shunt chopper is 0.1 megohm. A typical value of $r_{ds}(ON)$ for the 40460 transistor is 90 ohms. If these values are substituted in Eq. (3) and the signal voltage E_S is assumed to be 1 millivolt, E_O is calculated as follows:

$$E_O = 10^{-3} (90/10^5) = 0.9 \text{ microvolt}$$

In the ON condition, therefore, the dc error voltage is less than 0.1 per cent for the values used, and is directly proportional to the input signal.

For the OFF condition, the steady-state output voltage E_O is given by

$$E_O = E_S \left[\frac{\frac{r_{ds} R_L}{r_{ds} + R_L}}{R_S + \frac{r_{ds} R_L}{r_{ds} + R_L}} \right] + V_{GS} \left[\frac{\frac{r_{ds} R_L}{r_{ds} + R_L}}{R_G + \frac{r_{ds} R_L}{r_{ds} + R_L}} \right] \quad (4)$$

In most MOS transistors, both $r_{ds}(OFF)$ and R_G are much greater than R_L. Therefore, Eq. (4) may be simplified as follows:

$$E_O = E_S \frac{R_L}{R_S + R_L} + V_{GS} \frac{R_L}{R_G} \quad (5)$$

If R_S, R_L, and E_S are assumed to have the values used previously, the gate-to-source voltage V_{GS} is assumed to be -10 volts, and the gate resistance R_G is assumed to be 10^{12} ohms (minimum permissible gate resistance for the 40460), the value of E_O is calculated as follows:

$$E_O = 10^{-3} \left[\frac{10^5}{2 \times 10^5} \right] - 10 \left[\frac{10^5}{10^{12}} \right]$$

$$= \frac{10^{-3}}{2} - 10^{-6} \approx 0.5 \text{ millivolt}$$

The second term in Eq. (5) is the error term for the OFF condition; it is not proportional to the input signal E_S. For the numbers used, the output error in the OFF condition is only 0.2 per cent. If a typical value of 10^{14} ohms is used for the 40460 gate resistance instead of the minimum value of 10^{12} ohms, the error voltage is reduced to only 0.002 per cent. The output error remains small for any value of signal voltage E_S that does not approach the error voltage in magnitude.

Because the error voltage is inversely proportional to the gate leakage resistance R_G, most junction gate field-effect transistors produce larger error voltages than MOS transistors (the minimum R_G of most junction-gate devices is only 1 to 10 per cent that of MOS transistors).

A similar procedure may be used for analysis of series chopper and series-shunt chopper circuits.

The operation of all MOS chopper circuits is greatly affected by the magnitude of the source and load resistances. Table II lists the output voltages of the three basic chopper circuits for various combinations of source and load resistance. It is assumed that the input voltage E_S is 1 millivolt, and that the drain-to-source resistance r_{ds} is 100 ohms in the ON condition and 1000 megohms in the OFF position. The gate leakage resistance R_G (10^{12} ohms or more) is neglected. The following conclusions can be drawn from the data shown:

1. Only the series or the series-shunt circuit should be used when $R_S < r_{ds}(ON)$.
2. In general, R_L should be high. ($R_L >> r_{ds}(ON)$.
3. The load resistance should be higher than the source resistance. ($R_L \geq R_S$).
4. The performance of the series-shunt circuit is equal to or better than that of either the series or the shunt chopper alone for any combination of R_S and R_L.

Source Resistance R_S (ohms)	Load Resistance R_L (ohms)	Approx. Output Voltage E_O - mV (Max. Output = 1 V) Shunt Chopper (ON)	Shunt Chopper (OFF)	Series Chopper (ON)	Series Chopper (OFF)	Series-Shunt Chopper (ON)	Series-Shunt Chopper (OFF)
1M	1M	0.1	500	500	1	500	0.0001
100K	1M	1	900	900	1	900	0.0001
100	1M	500	1000	1000	1	1000	0.0001
0	1M	1000	1000	1000	1	1000	0.0001
1M	100K	0.1	90	90	0.1	90	0.0001
1M	100	0.05	0.1	0.1	0.0001	0.1	0.00005
100K	100K	1	500	500	0.1	500	0.0001
100	100	333	500	333	0.0001	333	0.00005

Table II - Steady-state chopper output voltage for various source and load resistances.

Transient Conditions

Fig. 6 shows the ac equivalent circuit of an MOS shunt chopper. The interelectrode capacitances of the MOS transistor affect operation of the circuit at high frequencies. The input capacitance C_{gs} increases the rise time of the gate driving signal and thus increases the switching time of the chopper. This effect is not usually a serious limitation, however, because the switching time of the MOS transistor depends primarily on the input and output time constants. Switching times as short as 10 nanoseconds can be achieved when an MOS transistor is driven from a low-impedance generator and the load resistance is less than about 2000 ohms.

The output capacitance C_{ds} also tends to limit the maximum frequency that can be chopped. When the reactance of this capacitance becomes much lower than the load resistance R_L, the chopper becomes ineffective because $X_{C_{ds}}$ is essentially in parallel with R_L and $r_{ds(OFF)}$.

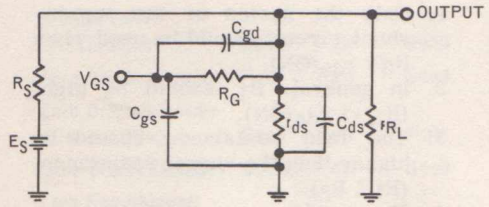


Fig. 6 - AC equivalent circuit of MOS shunt chopper.

The feedthrough capacitance C_{gd} is the most important of the three interelectrode capacitances because it couples a portion of the gate drive signal into the load circuit and causes a voltage spike to appear across R_L each time the gate drive signal changes state. C_{gd} and R_L form a differentiating network which allows the leading edge of the gate drive signal to pass through. The output capacitance C_{ds} is beneficial to the extent that it helps reduce the amplitude of the feedthrough spike.

The effect of the feedthrough spikes can be reduced by several methods. Typical approaches include the following:

(a) use of a clipping network on the output when the input signal to be chopped is fixed in amplitude,
(b) use of a low chopping frequency,
(c) use of an MOS transistor that has a low feedthrough capacitance C_{gd} (some MOS transistors have typical C_{gd} values as low as 0.13 picofarad),
(d) use of a gate drive signal that has poor rise and fall times,
(e) use of a source and load resistance as low as feasible,
(f) use of a shield between the gate and drain leads,
(g) use of a series-shunt chopper circuit.

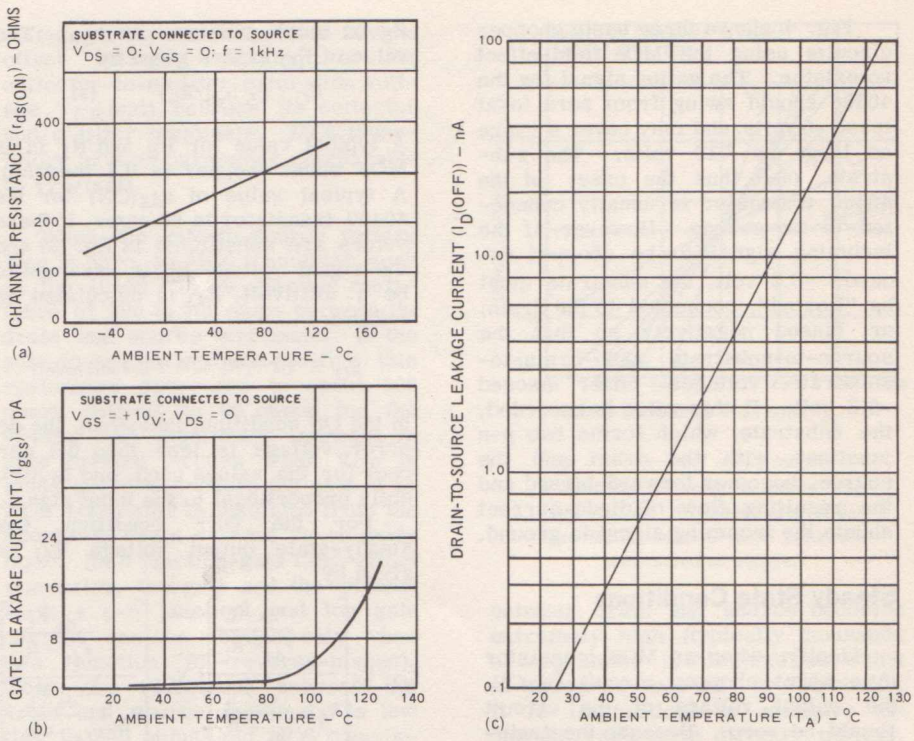


Fig. 7 - Variation of 40460 parameters with ambient temperature: (a) channel resistance r_{ds}; (b) gate leakage current I_{gss}; (c) drain-to source leakage current $I_{D(OFF)}$.

Temperature Variations

The variation of MOS transistor parameters with temperature can affect the operation of a chopper circuit unless allowance is made for such variations in the circuit design. It is important, therefore, to determine the approximate degree to which each parameter can be expected to change with temperature. Fig. 7 shows curves of channel resistence r_{ds}, gate leakage current I_{gss}, and drain-to-source leakage current $I_{D(OFF)}$ as a function of temperature for the 40460. I_{gss} and $I_{D(OFF)}$ were not measured at temperatures below 25°C because condensation and frost that form on the test chassis result in erroneous and/or erratic readings of picoampere currents. Test circuits used to measure these parameters are shown in the Appendix.

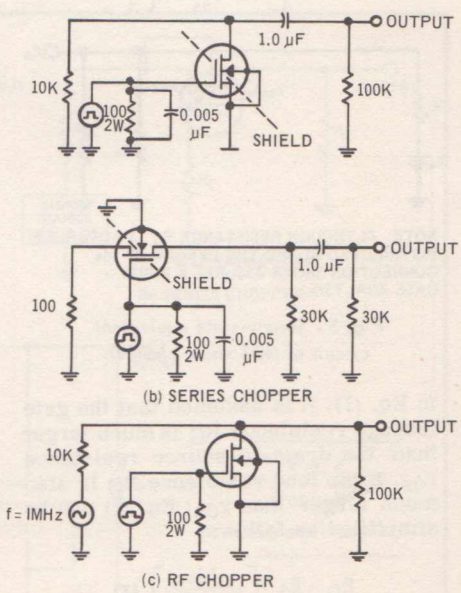
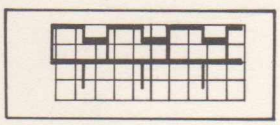


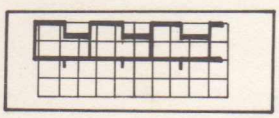
Fig. 8 - Typical MOS chopper circuits: (a) shunt chopper; (b) series chopper; (c) rf chopper.

Typical Circuits

Fig. 8 shows three chopper circuits that were constructed for demchopper, (b) a series chopper, and (c) an ac chopper. The 0.005 microfarad capacitor across the gate drive generator in circuits (a) and (b) indrive signal. A resistor is used in each circuit to simulate the impedance of the signal source. The actual input voltage was set at zero so that spike feedthrough and offset voltages could be measured. The dc offset voltage, which is caused primarily by the average value of the spikes over the whole cycle, was too small to be measured on the equipment available. Fig. 9 shows the actual spike feedthrough for the 40460 and 3N128 MOS transistors in the shunt and series circuits of Figs. 8(a) and 8(b); the rise time of the gate drive signal was 1 microsecond.

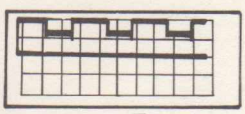


40460 GATE DRIVE OUTPUT (0 to -8V)

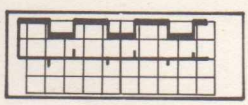


3N128 SHUNT CIRCUIT GATE DRIVE OUTPUT (0 to -8V)

SCALE	
VERTICAL	UPPER TRACE = 10V/DIV. LOWER TRACE = 10mV/DIV.
HORIZONTAL	100 μS/DIV.



40460 GATE DRIVE OUTPUT (0 to -8V)



3N128 SERIES CIRCUIT GATE DRIVE OUTPUT (0 to -8V)

SCALE	
VERTICAL	UPPER TRACE = 10V/DIV. LOWER TRACE = 20mV/DIV.
HORIZONTAL	100 μS/DIV.

Fig. 9 - Actual spike feedthrough in shunt and series chopper circuits employing the 40460 and 3N128 MOS transistors.

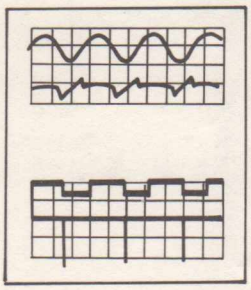


Fig. 10 - Comparison of sine and square-wave gate drive for an MOS shunt chopper employing the 40460.

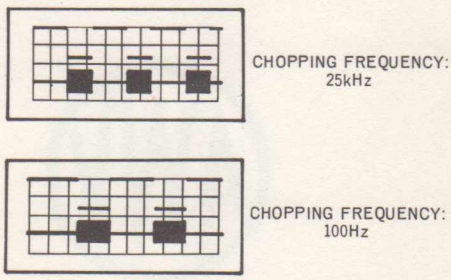


Fig. 11 - Results of using MOS rf chopper at a fast and a slow chopping frequency.

It is recommended that MOS choppers be driven from a square-wave source. Fig. 10 shows the feedthrough that results when the circuits of Figs. 8(a) and 8(b) are driven from a sine-wave generator instead of a square wave.

Fig. 11 shows how the circuit of Fig. 8(c) can be used to chop an rf signal at either a slow or a fast chopping frequency. The 40460 transistor can be used to chop rf signals extending up to the low vhf region. The frequency of the gate drive signal can be as high as several hundred kilohertz before excessive degradation of the square wave occurs. The rise time of the gate drive signal for the circuit of Fig. 8(c) was 15 nanoseconds.

In field-effect-transistor choppers using a version of the series-shunt circuit shown in Fig. 8(c), noise and offset voltages as low as 10 microvolts or less have been obtained.[1] Balanced MOS chopper circuits using special compensating networks have also been developed to chop 0.1 microvolt signals at impedance levels up to 40,000 ohms and chopping frequencies up to 250 Hz.[2]

REFERENCES

1. "Airpax Electronics", ELECTRONICS, March 20, 1967, page 61.

2. J.J. Hitt and G. Mosley, "FET Chopper Circuits for Low-Level Signals", 1967 IEEE CONVENTION DIGEST, page 488.

APPENDIX

Test Circuits

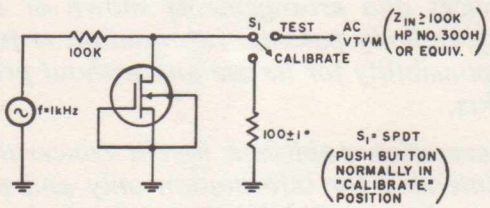


Fig. A-1 - Channel resistance ($r_{ds}(ON)$) measurement circuit.

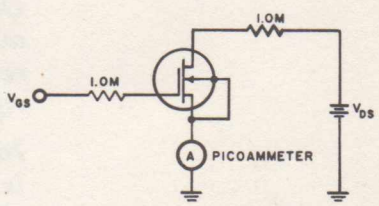


Fig. A-2 - Cutoff current ($I_D(OFF)$) measurement circuit.

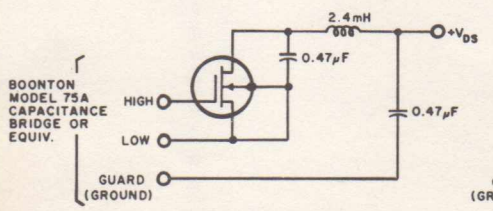


Fig. A-3 - Input capacitance (C_{iss}) measurement circuit.

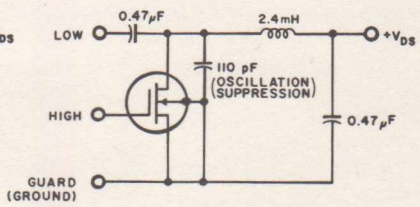


Fig. A-4 - Reverse transfer (Feedback) capacitance (C_{rss}) measurement circuit.

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