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*A variety of interesting work is constantly being undertaken by engineers in the Applications Laboratory of A.W.V. at Rydalmere, N.S.W.*

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# PLATE AND GRID VOLTAGE DISPLAY UNIT FOR DEFLECTION VALVES

G. N. TAYLOR


## Summary

The measurement of operating conditions of valves in deflection circuits of television receivers has long presented serious problems due to the high impedances and high voltages present. One is generally interested in specific portions of the waveform, namely voltages during scan at the plate, and end-of-scan voltage at the grid in the case of horizontal deflection.

Display and measurement of minimum plate voltages of the order of 30-100 volts in the presence of a pulse of up to 10 kV are made possible with the unit described. The unit also permits the display and measurement of end-of-scan grid voltages of one or two volts in the presence of a peak-to-peak voltage of the order of 150 volts. The accuracy of the measurements is limited by the accuracy to which the vertical amplifier of the oscilloscope can be calibrated.

An added advantage of the unit, when used in conjunction with a current probe, is the ability to display in its entirety, an X-Y plot of the load line of the horizontal output valve or an expanded view of that part of the load line through which the scan is traced.

Designed primarily for use with horizontal output circuits, the unit may be used equally well with vertical output valves.


## Description of Instrument

When used in conjunction with a suitable oscilloscope the unit described is capable of the following:—

(1) Displaying plate voltage waveforms and permitting the measurement of voltage during scan.

(2) Displaying the grid voltage at the end of scan and permitting voltage measurements in this region.

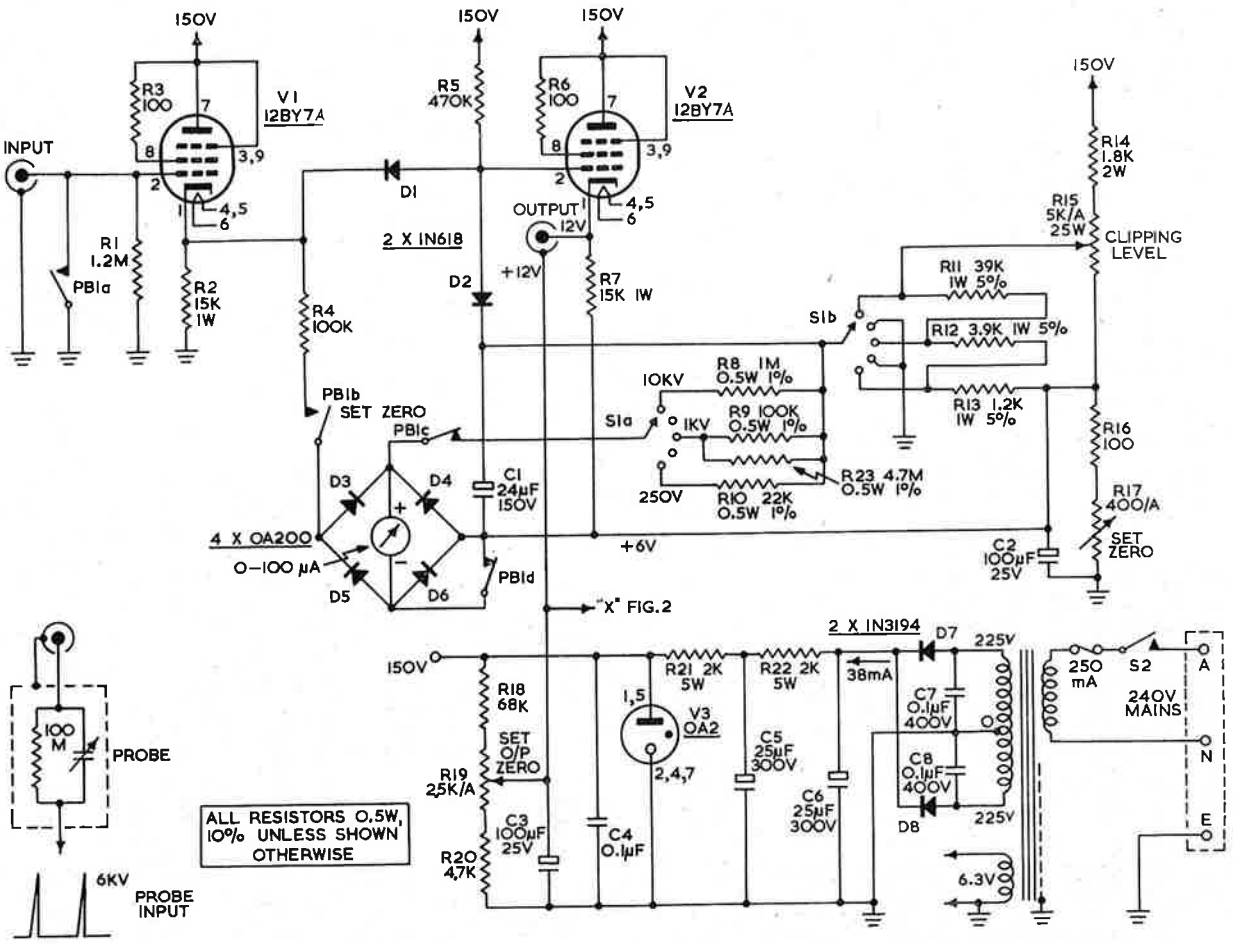



**Fig. 1. Circuit of Plate Voltage Display Unit**

## Plate Voltage Measurement

The portion of the plate voltage waveform of considerable interest is that during scan.

The use of a high voltage probe directly connected to an oscilloscope to display this portion of the waveform, is impractical since the pre-amplifier of the oscilloscope is overloaded when the sensitivity is sufficiently increased to observe the scan portion of the waveform. This results in drift of d.c. levels as well as non-linear amplification.

In order to observe this region with any degree of accuracy, the flyback peak must be removed by some means. This voltage is typically 6 kV in the case of a modern monochrome television receiver. The plate circuit is of high impedance and loading by the test instrument must be kept to a minimum. For this reason a high impedance, low capacitance probe has been constructed.[1] The probe presents a loading of 100MΩ and 3 pF giving an attenuation of 100X when used with this unit. Variable capacitive compensation is provided to match the probe to a variety of indicating units.

A unit for similar measurements[2] was proposed in which the input, a vacuum diode, was connected directly to the plate of the output valve. The diode was biased so that only voltages below the bias level appeared at the output. Heavy loading of the output valve plate circuit was apparent with this arrangement resulting in erroneous measurements.

In the unit to be described (refer to circuit diagram Fig. 1), measurement of plate voltage is achieved as follows: The signal is attenuated by means of the probe to a level which may be handled by the grid of a cathode follower without causing grid current to flow or distorting the waveform. A clipping circuit follows the cathode follower. The clipping level is adjustable in three variable ranges. For voltages below the clipping level, diode $D_1$ conducts and $D_2$ is cut-off. Above the clipping level the situation is reversed. The cathode follower is used to provide high input impedance to the probe and a low output im-

[1] Details of this probe will be published in a later issue.
[2] Ref. Mullard Technical Communications Vol. 3, 25, June, 1957.

pedance. The latter is necessary since the clipping circuit presents two different impedances, one for that part of the waveform when clipping takes place and another when clipping is absent. The clipping level is metered and may be read directly or measured on the oscilloscope after calibration. In order to off-set the quiescent voltage at the cathode of the first stage, the divider and metering circuits are raised above ground by a similar voltage. The "set-zero" control R17 is used to adjust the difference between these voltages to zero. The push button PB1 short circuits the input to ground and connects the meter for the "set-zero" operation. The unusual connection of the diode bridge is used to reduce errors in the meter readings (caused by the forward and reverse resistances of the bridge diodes), when the meter is used to measure clipping level. Silicon diodes have been used to reduce these errors to a minimum.

If the output from the clipping network is directly applied to the oscilloscope, the charge on the input capacitance of the oscilloscope and connecting leads tends to cut off the series diode when the voltage at the cathode of the first stage rapidly increases. (The current required to charge the probe and cable capacitance is comparable with the diode current since the diode current must be kept low to permit normal operation of the cathode follower.) Diode current is controlled by $R_5$. For this reason the output from the clipping circuit is applied to a further cathode follower from which the output is taken.

A d.c. voltage adjustment is provided in the final stage to offset the standing voltage to ground and so avoids the use of the vertical shift control on the oscilloscope. The omission of this voltage adjustment would require the oscilloscope shift control to have a range adequate to cope with the 12 volts d.c. appearing at the output. Its incorporation necessitates operating the low potential side of the oscilloscope input at approximately +12 volts, and not earthed!

Capacitors $C^7$ and $C^8$ are included to reduce r.f. interference which may be present on the mains supply.

## Grid Voltage Measurement

## (Refer to Fig. 2)

The grid circuit impedance in the normal deflection circuit of a television receiver is high (2 MΩ) and consequently the loading by a typical 100X probe (10 MΩ) is quite appreciable. Also to observe the grid voltage at the end of the scan, the input to the oscilloscope must be expanded above the overload level of the pre-amplifier and, as discussed in connection with the plate voltage measurement, causes drift and non linearity in the oscilloscope.

This unit clips the input voltage below about —20 volts, thus enabling the portion at the end of scan to be sufficiently expanded to make accurate measurements. The grid return of the horizontal output stage is used as the grid return for the cathode follower and, since no grid current is drawn by the cathode follower of the display unit, loading is reduced to a minimum.

An alternative method of measurement is to use a probe of much greater impedance than that of the grid circuit. The associated high attenuation would require a subsequent amplifier of considerable gain. The unit proposed achieves this high impedance with an attenuation that can be easily overcome by means of the gain calibration on the oscilloscope.

## NOTES ON THE OPERATION OF THE DISPLAY UNIT

### Plate Voltage Unit

The output of the unit is directly connected to the oscilloscope by means of a short coaxial lead to reduce capacitive attenuation at high frequencies.

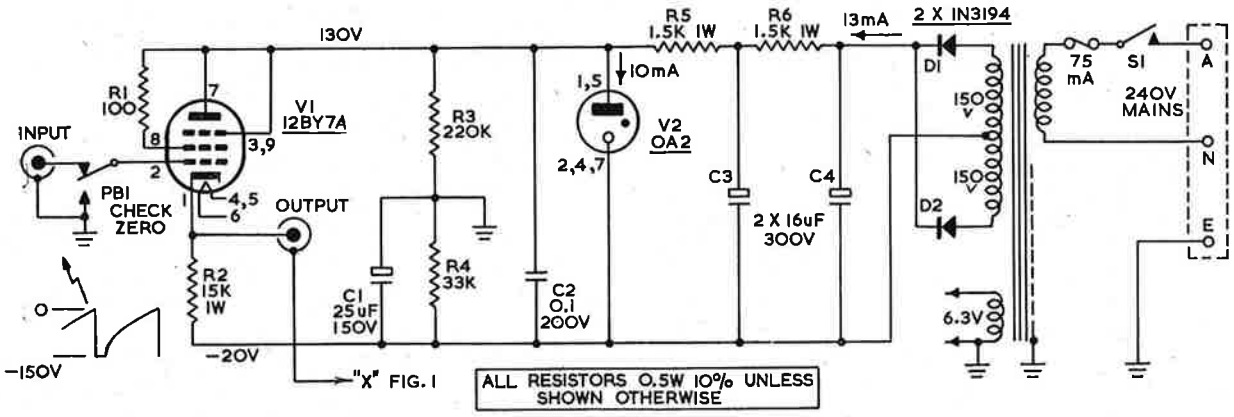



**Fig. 2. Circuit of Grid Voltage Display Unit**

An earth connection must be made between the circuit under test and the display unit either through the probe braid or by a direct connection to the earth terminal of the display unit.

The high frequency compensation of the probe must be adjusted with the aid of a suitable input waveform and with the clipping level controls set above the maximum excursions of the input signal. The overall system gain must be calibrated by means of the variable attenuator on the vertical preamplifier of the oscilloscope. A 100 volt 1 Kc/s square wave has been found suitable for both the above adjustments. The accuracy of the latter adjustment determines the accuracy of subsequent measurements made on the oscilloscope. Overall attenuation of the unit is initially adjusted by means of $R_1$. The meter is intended as an approximate indicator of clipping level, its accuracy being dependent on $R_1$, the calibrating resistors $R_8$, $R_9$, $R_{10}$, $R_{23}$ and the cut-off behaviour of the diodes $D_1$ and $D_2$.

Once the probe has been connected to the plate of the valve of which the waveform is to be displayed, the clipping level is adjusted approximately to that desired by means of the meter range switch and clipping level control. The meter zero is then set by means of the push button $PB_1$ and potentiometer $R_{17}$.

The output zero is adjusted as follows:—

While operating the "set zero" push button PB1, the oscilloscope input is switched between A.C. and D.C. The "set O/P zero" control $R_{19}$ is adjusted until no shift of the oscilloscope trace results. The clipping level may now be read from the meter or from the directly coupled oscilloscope. Intermediate levels may be measured on the oscilloscope.

If the clipping level is changed, both zero-set adjustments must be re-checked.

## Grid Voltage Unit

The connection between the grid of the valve under test and the display unit is made by a short low capacitance lead to keep loading of the grid circuit to a minimum. A twisted pair of 10/.010 P.V.C. insulated tinned copper wire has been found satisfactory for this application.

The output connection to the oscilloscope is made by a short coaxial lead as in the case of the plate voltage display.

The input zero level may be checked by operating the push button.

End of scan voltage may then be measured on the oscilloscope.

It may be found necessary to compensate for the slight attenuation of the cathode follower by increasing the gain of the oscilloscope preamplifier. However, only minor errors in measurements will result if this adjustment is not carried out.

## Notes

1) The oscilloscope must NOT be earthed since the output braid of both units is at approximately +12 volts above ground. Having the briad of both plate and grid display units common, permits them to be connected to the one dual trace oscilloscope.

2) Although both units work independently, adjustment of the output zero control of the plate voltage display unit will alter the d.c. level of the output from the grid display unit. To avoid this, the low potential side of the output of the grid display unit, may be earthed rather than connected to "X" in Fig. 1. With this connection the low potential sides of the outputs of both units must not be shorted together as would be the case if they were simultaneously connected to a double beam oscilloscope.

## Caution

Since direct coupling is used throughout the display unit and oscilloscope to determine the d.c. level, care must be taken to allow for any drift in the amplifier system. When used in conjunction with a Tektronix oscilloscope a drift of typically 20 mV has been observed. This amounts to an equivalent shift of approximately 2 volts in the input voltage to the probe. The drift occurs when the input to the display unit is suddenly changed either by operating the zero set push button or by applying a voltage with a high direct component to the probe. It takes approximately 2 seconds for the drift to cease after the signal is changed. Provided a reference point on the waveform is noted the instant the input is changed, any drift may be taken care of by readjusting the shift control on the oscilloscope.

## Acknowledgment

The author wishes to acknowledge the assistance given by the staff of Amalgamated Wireless Valve Co. Pty. Ltd. Applications Laboratory during the development and construction of this instrument.

# TOTAL STORED CHARGE IN JUNCTION TRANSISTORS, ITS MEASUREMENTS AND APPLICATION

BY J. S. FLEISCHMAN

## Introduction

This Note describes a technique for measuring total stored charge in a junction transistor. The RCA 2N955A ultra high-speed, epitaxial, NPN germanium transistor was used for all measurements.

The variation of total stored charge with collector current, collector voltage, and temperature is described. Variation of total "turn-off" time with collector current is also presented. In addition, the usefulness and application of these measurements in the worst-case design of computer logic circuitry is given.

## General Information

At all times, there exists some minority carrier density in the transistor. When the transistor is in the "off" condition (emitter and collector reverse biased), the total minority stored charge is a minimum. However, when the transistor is operating in the saturation region ("on" condition) with both junctions forward biased, there is an increase of stored charge in the device. For alloy types and in epitaxial mesa transistors, most of the storage occurs in the base region with a relatively small amount in the collector, while in standard mesa types, much more charge is stored in the collector. This excess stored charge must be removed before the transistor can be returned to the "off" condition. This is generally the characteristic that limits the switching speed of the device.

In high-speed switching circuits, it is essential that transistor "turn-on" and "turn-off" times be as fast as possible. The base input waveform shown in Figure 1, although impractical to generate, would be ideal for high-speed transistor switching.

For fast "turn-on", the base current should rise instantaneously to $I_{B_1}$, producing a large overdrive current. After the initial "turn-on", the current should level off to the value required to keep the transistor "on", $I_{B(SAT)}$. Reducing the current to this lower value avoids excessive stored charge during the "on" time, thereby reducing the time required for turning the transistor "off". For fast "turn-off", current should fall instantaneously to the reverse current $I_{B_2}$, thereby providing a large reverse drive. Immediately after "turn-off", the current should reduce to a level where emitter reverse bias voltage is just sufficient for maintaining the "off" condition. A large reverse bias voltage would cause an increase in "turn-on" time due to the capacitive effects of the device.

The ideal waveform (Figure 1) is approximated from a simple square wave input by the addition of a "speed-up" capacitor as shown in the RCTL circuit of Figure 2. This circuit provides an input base current waveform as shown in Figure 3. When the input pulse goes positive, speed-up capacitor $C_F$ provides an instantaneous high base current for rapid "turn-on". When the capacitor becomes fully charged, the base current levels off to the value:

$$I_{B(SAT)} = \frac{V_{IN} - V_{BE}}{R_F} - \frac{V_{BB} + V_{BE}}{R_B}$$

When the input pulse returns to zero, the charge on the capacitor is discharged into the base of the transistor, neutralizing the charge stored during the time the device was "on". This discharge provides the necessary instantaneous high current ($I_{B_2}$) for fast transistor "turn-off".

Because the transistor is more difficult to turn-off than to turn-on, the size of capacitor $C_F$ is determined by turn-off requirements. This will guarantee that "turn-off" as well as "turn-on" are fast.

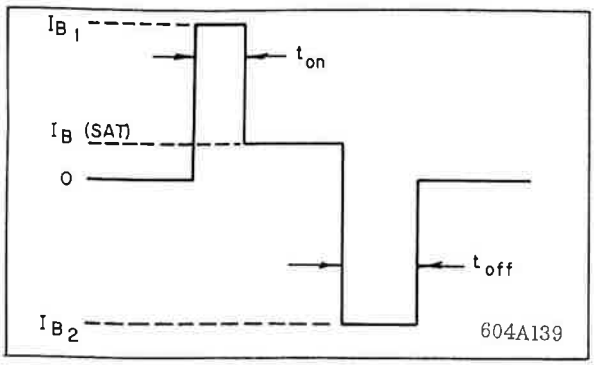



Figure 1

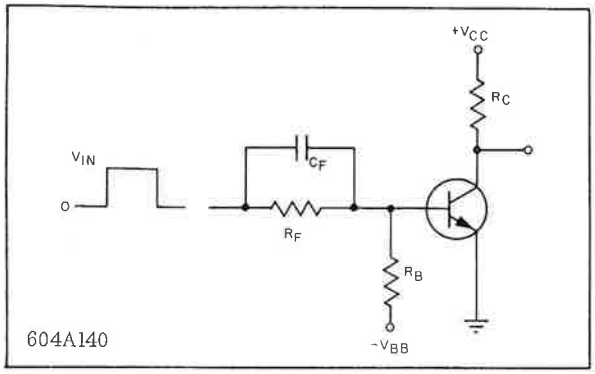



Figure 2

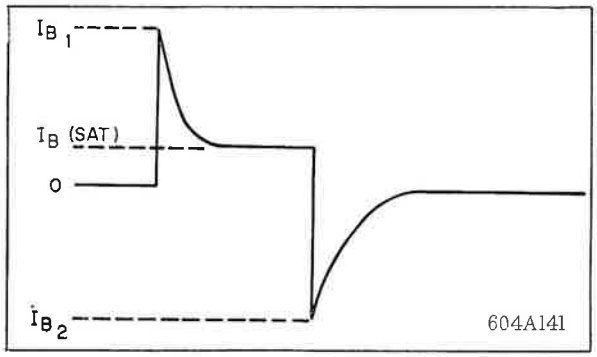



Figure 3

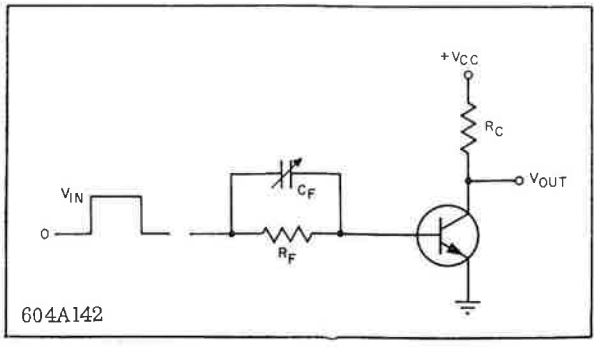



Figure 4

### Measurement of Total Stored Charge ($Q_s$) and Total Turn-Off Time (tqs)

The stored charge of a transistor is measured with the circuit shown in Figure 4. A capacitor with known charge is discharged into the base of the transistor. The capacitance of $C_F$ is increased until it compensates the charge stored in the transistor during the "on" time.

Compensation occurs when increasing the capacitance no longer reduces "turn-off" time. The total stored charge ($Q_s$) is then given by:

$$Q_s = C_F(V_{IN} - V_{BE})$$

where $V_{BE}$ is the base-to-emitter saturation voltage. This is not the exact charge that flows into the base of the transistor. A slight error is introduced due to the charge that flows through $R_F$, however, since the value of the input impedance of the device is much lower than the resistance of $R_F$, this charge is very small and for all practical purposes can be neglected.

By observing the output waveform, the critical value of stored charge can be determined and the total "turn-off" time (tqs) for compensated $Q_s$ can be measured. The input and output waveforms are shown in Figure 5. The compensated collector waveform indicates that the base charge, plus the charge in the collector and emitter, is compensated.

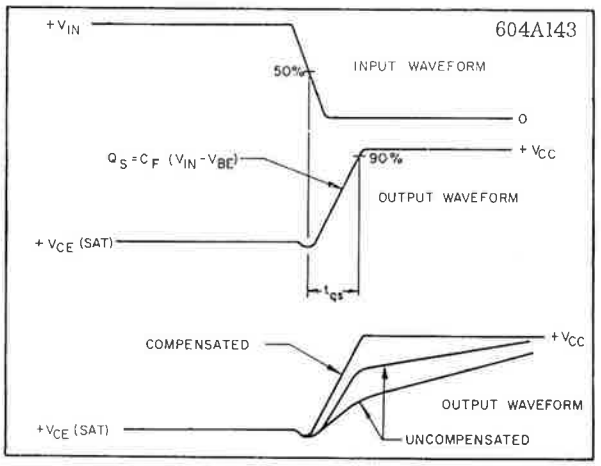



Figure 5

The base waveform can also be observed for the $Q_s$ test. This waveform is shown in Figure 6. The base waveform shows only the compensation of the charge stored in the base. In some types of transistors, the stored base charge may differ considerably from the total stored charge and this method of measurement cannot be utilized.

### Stored Charge Characteristics of the 2N955A

The stored charge characteristics of the RCA 2N955A were obtained by using limit units (units with $Q_s$ at the maximum specified limit). This was done so the maximum stored charge characteristics obtained would be useful as worst-case circuit design data.

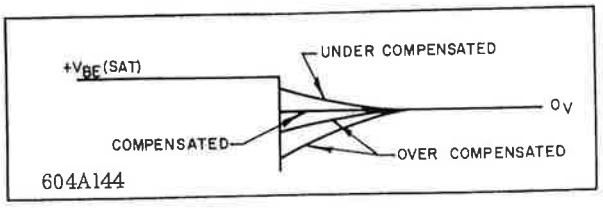



**Figure 6**

Figure 7 shows the variation of total stored charge with collector current (base current as the running parameter). The variation with collector current is linear, with charge decreasing as current increased for a fixed base current. Variation with base current is also linear at a fixed collector current.

The equation of the curves of Figure 7 is given by:

$$Q_{s_{max}} = -\frac{I_C}{3} + 23.4\, I_B + 39.9$$

where $Q_s$ is in picocoulombs and $I_C$ and $I_B$ are in milliamperes.

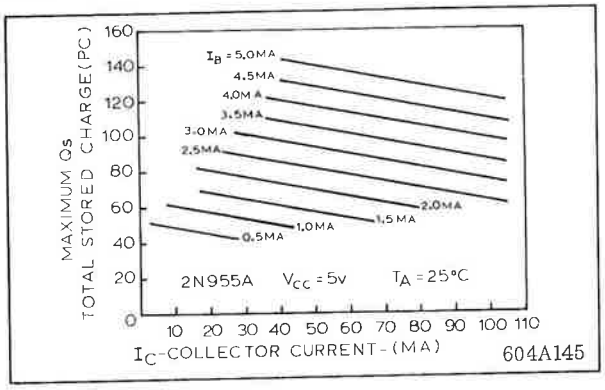



**Figure 7**

With the 2N955A expitaxial transistor, the stored charge decreased as collector current increased. For most non-epitaxial mesa types, the stored charge increases with increasing collector current. Some alloy-type transistors exhibit a flat stored charge characteristic. These effects can be explained by a detailed investigation of the equations of Ebers and Moll[1] (see page 6).

Figure 8 shows the maximum per cent change of $Q_s$ with temperature. As the temperature of the device increases, the total stored charge also increases.

The value of collector voltage ($V_{CC}$) also effects the stored charge. As the collector voltage is increased, the collector capacitance must charge to a higher voltage (during "turn-off"), therefore, the total stored charge in the device increases as collector voltage is increased. This effect is illustrated in Figure 9.

The plot of Figure 10 shows the variation of total "turn-off" time tqs (for compensated $Q_s$) with collector current. As the current increased, the "turn-off" time decreased for a fixed value of $V_{CC}$. To increase collector current, the collector resistance must be decreased. This reduces the collector circuit time constant $R_cC_c$ which results in a shorter "turn-off" time.

The usefulness of Figures 7, 8, and 9 for determining the stored charge of the 2N955A under any particular operating condition can be illustrated by the following example:

Assume it is desired to determine the stored charge of the 2N955A under the following conditions:

$$T_{A_{max}} = 50°C,\ I_C = 30\ ma,\ I_B = 3\ ma,\ V_{CC} = 6v$$

From Figure 7:

For an $I_C$ of 30 ma and $I_B$ of 3 ma, $Q_s$ max. = 101 pC at 25°C and $V_{CC}$ = 5v.

From Figure 8:

At 50°C, the % change in $Q_s$ is +17%.

From Figure 9:

At a collector voltage of 6v, the % change in $Q_s$ is +7%.

Therefore, the maximum total stored charge under the above mentioned operating conditions is:

$$Q_{s_{max}} = 101 + (.17 + .07)\ 101 =$$

$$101 + 24.1 = 125.1\ pC$$

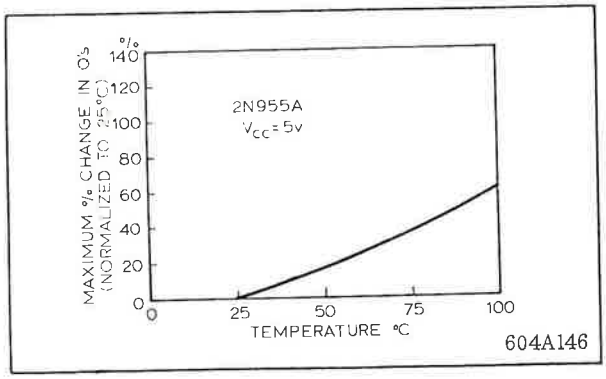



**Figure 8**

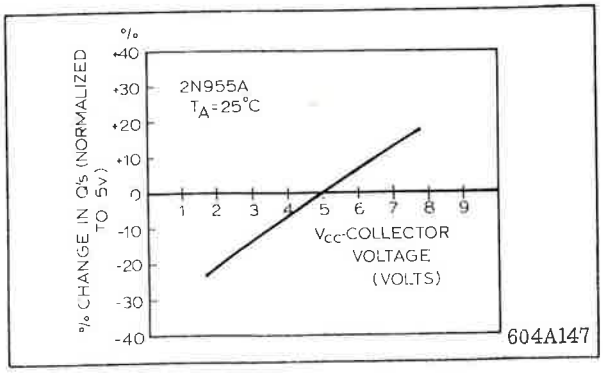



**Figure 9**

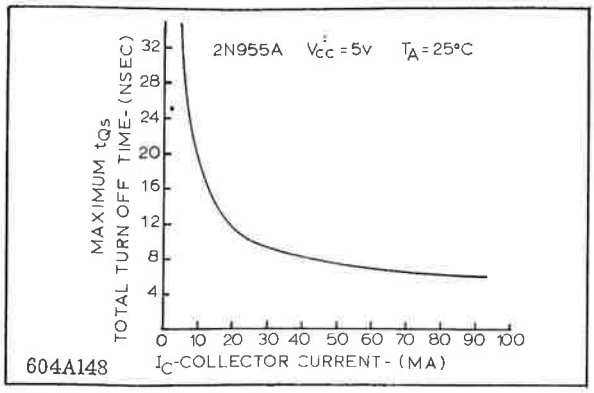



Figure 10

## Applications

Worst-case conditions must be considered when designing switching circuits. This is essential to guarantee reliable operation of the circuit under the most adverse conditions. These conditions include variations of resistors, power supplies, transistors, change of transistor parameters due to temperature and probable transistor degradation. All of these conditions were considered in the following applications.

With a speed-up capacitor, the 2N955A can provide high-speed switching in both RCTL (resistor-capacitor-transistor-logic) and DTL (diode-transistor-logic) circuits. The RCTL circuit and performance data are shown in Figures 11 and 12.

Design equations for this circuit are as follows:

$$\frac{\overline{V}_{CC} - \underline{V}_{CE}}{\underline{\beta}\underline{R}_C} \leq \frac{\underline{V}_{C_1} + \underline{V}_F - \overline{V}_{BE}}{\overline{R}_F} - \frac{\overline{V}_{BB} + \overline{V}_{BE}}{\underline{R}_B} \quad (1)$$

$$\underline{V}_{BE}(\text{off}) \leq \frac{\underline{V}_{BB} - \overline{V}_{CE}\overline{R}_B/\underline{R}_F - \overline{I}_{BO}\overline{R}_B}{1 + \overline{R}_B/\underline{R}_F} \quad (2)$$

$$\overline{m} \leq \frac{\dfrac{\underline{V}_{CC} - (\overline{V}_{C_1} + \overline{V}_F)}{\overline{R}_C} - \overline{n}\,\overline{I}_{CO}}{\dfrac{\overline{V}_{C_1} + \overline{V}_F - \underline{V}_{BE}}{\underline{R}_F}} \quad (3)$$

$$\underline{C}_F \geq \frac{\overline{Q}_s}{(\underline{V}_{C_1} + \underline{V}_F - \overline{V}_{BE}) - \overline{V}_{CE}} \quad (4)$$

$$\left[\overline{Q}_s \text{ determined at } I_C = \frac{\underline{V}_{CC} - \overline{V}_{CE}}{\overline{R}_C}\right] \quad (5)$$

$$\left[\text{and } I_B = \frac{\underline{V}_{C_1} + \underline{V}_F - \overline{V}_{BE}}{\underline{R}_F} - \frac{\underline{V}_{BB} + \overline{V}_{BE}}{\overline{R}_B}\right] \quad (6)$$

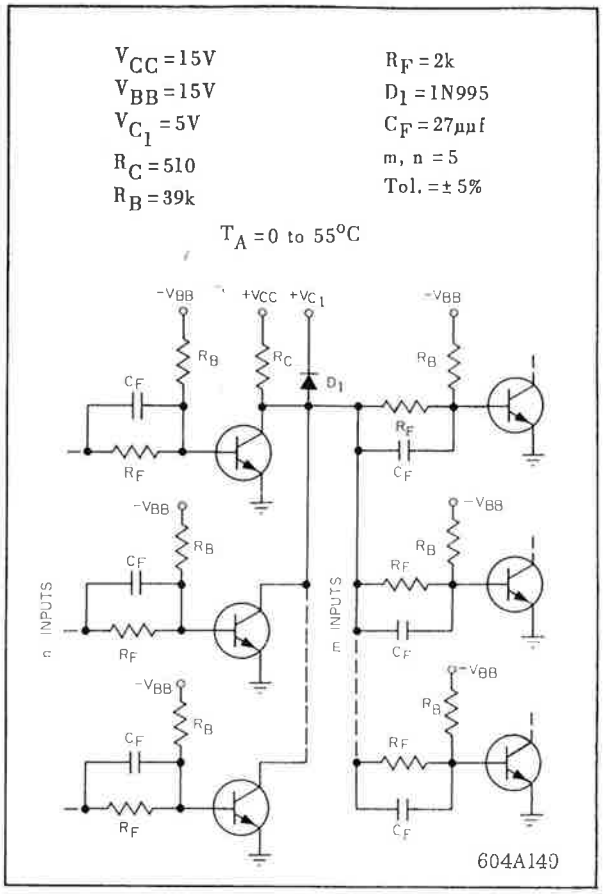



Figure 11

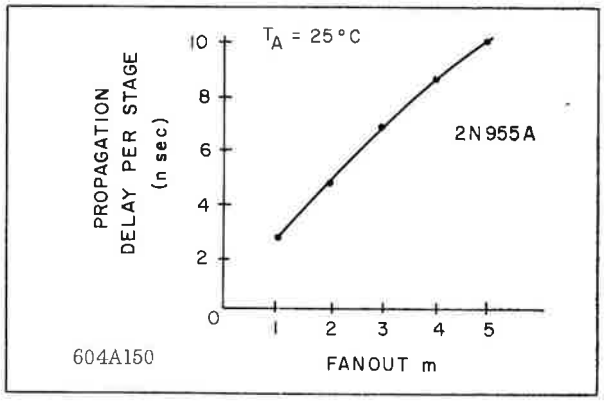



Figure 12

The maximum stored charge ($Q_s$) indicated in equation (4) is somewhat greater than the charge the speed-up capacitor must supply for fast "turn-off". This is because the hold-off bias current from the $V_{BB}$ supply compensates for a small amount of the stored charge in the device. This effect can generally be neglected.

From equation (4), it is seen that the correct selection of the speed-up capacitor is a pertinent part of the design. This value is readily obtained by

using the methods and graphs described in this Note. Then, using equation (4), the best value of speed-up capacitor can be calculated and optimum design and operation can be obtained.

The worst-case conditions in equations (4), (5), and (6) are arrived at as demonstrated in the following:

Equations (4), (5), and (6) without worst-case conditions are:

$$C_F \geqq \frac{Q_s}{(V_{C_1} + V_F - V_{BE}) - V_{CE}} \quad (7)$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \quad (8)$$

$$I_B = \frac{V_{C_1} + V_F - V_{BE}}{R_F} - \frac{V_{BB} + V_{BE}}{R_B} \quad (9)$$

Substituting the equation derived from the curves of Figure 7 for $Q_s$, equation (7) becomes:

$$C_F \geqq \frac{23.4\, I_B + 39.9 - I_C/3}{(V_{C_1} + V_F - V_{BE}) - V_{CE}} \quad (10)$$

Substituting equations (8) and (9) for $I_B$ and $I_C$ into equation (10), the following is obtained:

$$C_F \geqq \frac{23.4\left(\frac{V_{C_1}+V_F-V_{BE}}{R_F} - \frac{V_{BB}+V_{BE}}{R_B}\right) + 39.9 - \left(\frac{V_{CC}-V_{CE}}{3R_C}\right)}{(V_{C_1} + V_F - V_{BE}) - V_{CE}} \quad (11)$$

For worst-case design, the left side of equation (11) must be a minimum and the right side a maximum. For this to occur, the following conditions must be used in the equation.

$$\underline{C_F};\ \underline{V_{BB}};\ \overline{V_{CE}};\ \underline{V_{CC}};\ \underline{R_F};\ \overline{R_B};\ \overline{R_C} \quad (12)$$

Since factors $V_{C_1}$, $V_F$, and $V_{BE}$ appear in both the numerator and the denominator, it is impossible to tell if they should be a maximum or a minimum for worst-case design. This must be investigated by direct substitution of values into equation (11). The substitution which yields the maximum value of speed-up capacitor is chosen as the worst-case condition. For the 2N955A, the maximum value of speed-up capacitor is obtained when the following condition occurs:

$$\underline{V_{C_1}};\ \underline{V_F};\ \overline{V_{BE}} \quad (13)$$

For other transistor types, the opposite situation may be true.

Substituting the results of equations (12) and (13) into equations (7) through (9), give the design equations (4), (5), and (6) for worst-case conditions using the 2N955A.

$$\underline{C_F} \geqq \frac{\overline{Q_s}}{(\underline{V_{C_1}} + \underline{V_F} - \overline{V_{BE}}) - \overline{V_{CE}}} \quad (4)$$

$$I_C = \frac{\underline{V_{CC}} - \overline{V_{CE}}}{\overline{R_C}} \quad (5)$$

$$I_B = \frac{\underline{V_{C_1}} + \underline{V_F} - \overline{V_{BE}}}{\underline{R_F}} - \frac{\underline{V_{BB}} + \overline{V_{BE}}}{\overline{R_B}} \quad (6)$$

The disadvantage of the RCTL circuit is the need of a transistor for isolation of each input. In the DTL circuit, the same function is accomplished with relatively inexpensive diodes while still retaining the high-speed of the RCTL circuit.

The DTL circuit and performance data are shown in Figures 13 and 14.

The design of DTL circuits is accomplished by utilizing the following equations:

$$\frac{\underline{V_{CC}} - (\overline{V_{C_1}} + \overline{2V_F})}{\overline{R_L}} \geqq \frac{(\overline{V_{C_1}} + \overline{2V_F}) - \underline{V_{BE}}}{\underline{R_F}} \quad (14)$$

$$\frac{\overline{I_C}}{\underline{\beta}} \leqq \frac{\underline{V_{C_1}} + \underline{2V_F} - \overline{V_{BE}}}{\overline{R_F}} - \frac{\overline{V_{BB}} + \overline{V_{BE}}}{\underline{R_B}} \quad (15)$$

$$\underline{V_{BE}}(\text{off}) \leqq \frac{\underline{V_{BB}} - (\overline{V_{CE}} + \overline{V_F})\overline{R_B}/\underline{R_F} - \overline{I_{BO}}\,\overline{R_B}}{1 + \overline{R_B}/\underline{R_F}} \quad (16)$$

$$m \leqq \frac{\overline{I_C} - \frac{\overline{V_{CC}} - \underline{V_{CE}}}{\underline{R_C}}}{\frac{\overline{V_{CC}} - \underline{V_F} - \underline{V_{CE}}}{\underline{R_L}} + (\overline{n} - 1)\overline{I_R} - \frac{\underline{V_F} + \underline{V_{CE}} + \underline{V_{BB}} - \overline{I_{CO}}\,\overline{R_B}}{\overline{R_F} + \overline{R_B}}} \quad (17)$$

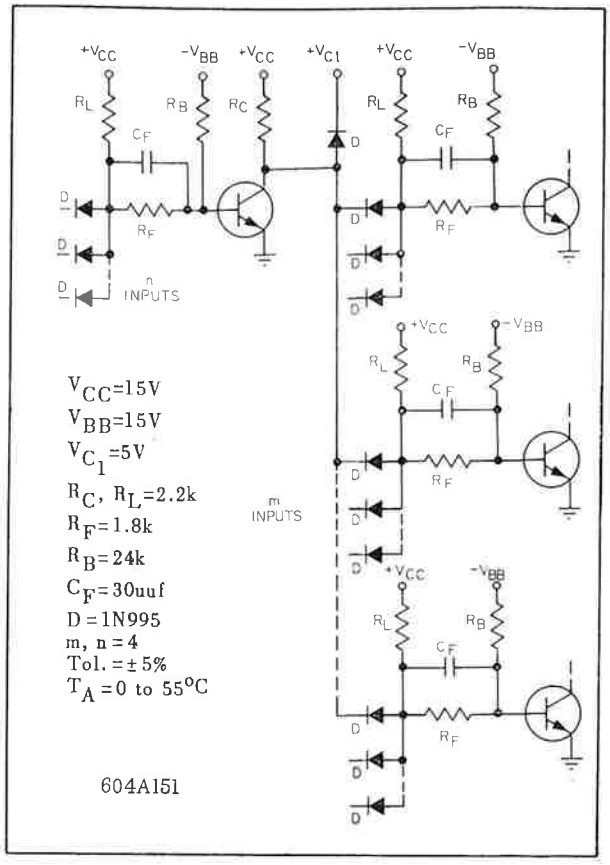



Figure 13

$$\underline{C_F} \geq \frac{\overline{Q_s}}{(\underline{V_{C_1}} + 2\underline{V_F} - \overline{V_{BE}}) - (\overline{V_{CE}} + \overline{V_F})} \quad (18)$$

$$\left[\overline{Q_s} \text{ determined at } I_C = \frac{\underline{V_{CC}} - \overline{V_{CE}}}{\overline{R_C}}\right] \quad (19)$$

$$I_B = \frac{\underline{V_{C_1}} + 2\underline{V_F} - \overline{V_{BE}}}{\underline{R_F}} - \frac{\underline{V_{BB}} + \overline{V_{BE}}}{\overline{R_B}} \quad (20)$$

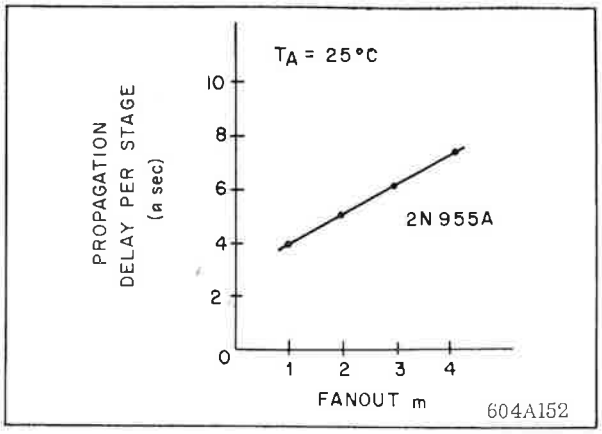



Figure 14

Here again, as seen in equation (18), the knowledge of $Q_s$ is important for optimum design. Equations (18), (19), and (20) are obtained in the same manner as previously described for the RCTL circuit.

## Conclusion

The specification and measurement of total stored charge ($Q_s$) as one of the basic transistor parameters provides a great deal of information in determining the switching speed and general operation of a device in switching circuits. This measurement provides more information than any other similar parameter. Other specifications such as $t_d$, $t_r$, $t_s$, and $t_f$ measurements are more difficult to work with and do not convey the necessary information for optimum design as is available from $Q_s$ and $t_{qs}$ measurements.

Hence, the measurement and specification of total stored charge and total "turn-off" time of a transistor furnish a practical and useful tool in the operation and design of transistor logic circuitry and an insight into the capabilities of the transistor itself.

(1) J. J. Ebers and J. L. Moll, "Large Signal Behavior of Junction Transistors" Proc. IRE, Vol. 42, No. 12, Dec., 1954.

(With acknowledgements to RCA)

# MORE ON MUSIC POWER

**B. J. Simpson**

A great deal has been said in these pages about the various ways of rating audio amplifiers, including the so-called "music-power" rating, that some apology may be needed for raising the matter again. However, only a few weeks ago a letter appeared in a magazine enquiring about music power, and it seems there must still be a large number of people who are not familiar with the term. Further, the reply appeared to be incomplete in some ways, and must have been rather unsatisfactory to the correspondent.

This then is the reason for raising the matter again, and for those who are already familiar with the information, perhaps we can go a little further and do a little thinking around the subject. A little philosophy can often be a good thing if only because it excites the mental processes. Allowance must be made, however, for statements which are speculative rather than factual and for some thoughts that are included solely to generate others.

If we assume from the start that we know nothing about music power, we could make a start by looking up the official definition of the expression. This will be found in a standard issued by the Institute of High Fidelity Manufacturers (U.S.A.), and it is I.H.F.M. Standard I.H.F.M.-A-200. This standard was mentioned in these pages in October, 1962.

Music power, in the standard quoted, is defined as "the greatest single-frequency power that can be obtained without exceeding rated total harmonic distortion when . . . . . the measurement is taken immediately after the sudden application of a signal, and during a time interval so short that supply voltages within the amplifier have not changed from their no-signal values." Music power, therefore, is in the nature of a transient rating. The defence for the use of this rating, apart from the obvious one that it makes the amplifier sound better on paper, is that the measurement condition more closely represents or approximates the conditions obtaining when the amplifier is reproducing music.

Most types of programme material, but not all, are transitory in their general nature, consisting of a main body of sound at a medium or low level with only short excursions into loud passages, the whole having few sustained notes of high sound level. The argument therefore is that under these conditions (assuming that the gain control of the amplifier is so adjusted that clipping does not occur on loud passages) the amplifier spends most of its time handling signals considerably below its maximum capability, and is driven to something approaching its maximum capability at comparatively infrequent intervals. When this does happen, the loud passage is short and transient-like in nature. It follows from this, according to the argument, that these short loud notes will be passed by the amplifier before the amplifier voltages have had a chance to drop as the normal result of increased power output, and that a higher maximum power output will be realised under this type of condition than would be the case where a continuous tone is applied to the amplifier.

Now this is a difficult sort of argument to evaluate, because it is very plausible and logical as far as it goes, and in fact in the majority of cases will probably be substantially borne out in practice. Whilst certainly not wishing to take sides, but merely to study the situation, one must consider some of the weak spots in the theory. The most obvious one that comes to mind is the case of, say, sustained organ tones at high volume, a fairly common thing in organ music. Obviously here the sustained tones will certainly be of sufficient duration to change the dc conditions in the amplifier. They will be similar to the application of a continuous test tone, and will place the amplifier in the situation where the maximum

undistorted output is the rms power output at the rated distortion figures, or something very close.

Another weakness follows a similar theory but goes a little further. How long can a transient be before dc conditions in the amplifier are disturbed? Between this figure and the continuous tone case, the maximum undistorted power output will follow a sliding scale if we follow the music power theory. Some of these criticisms may be rather carping criticisms, but, on the other hand, they may serve to put the matter in its true perspective. After all, if one is being offered an output power of n watts, he is entitled to know that under some circumstances he may get only n-x watts.

The extent to which dc conditions will be disturbed by transients of varying length or duration will depend on the time constants present in the amplifier power supply and other relevant circuits. This will naturally vary from one model to another, so that no reliable correlation of results will be available. The characteristics of the power supply must of necessity be ignored in music power measurements, whereas this is not so in the more conventional, or perhaps one might say "old-fashioned," rms methods of measuring performance.

If we turn back and look at the relevant part of the I.H.F.M. standard as quoted above, it will be apparent that the measurement of music power under the specified conditions is by no means an easy task. It would be possible to use certain items of specialised equipment, such as an amplifier manufacturer might assemble for his own use. Where only normal items of laboratory equipment are available, the procedure must be adjusted to suit the means available.

However, before going on to discuss how to carry out the measurement, it may be worth a few moments to examine just what has to be done. Firstly, it is clear that the "supply voltages" mentioned in the standard are in effect those around the output stage, and small variations in voltages in earlier stages will not (or should not) affect results. The supply voltages are therefore in practical terms and in the case of a valve amplifier the plate, screen and cathode-control grid voltages, have to be held or adjusted during the measurement.

The problem of arranging this is eased when the screens are returned directly to the B+ line, as often happens. Where cathode bias is used, there may be a slight drift in the value of the bias voltage even when the plate and screen voltages are held stationary. To correct this would be troublesome in that it would make the measurements more involved. Where the drift is small it could probably be neglected, as a small change in bias voltage will have little effect either on the output power or the distortion level.

Following on this a test procedure for valve amplifiers is suggested as follows:

1. Quiescent voltages around the output stage are carefully measured and recorded.

2. The main B+ line from the amplifier power supply is opened, and the output of a 0-50 volt low impedance power supply is connected into the line, so that the B+ value can be boosted by adjustment of the auxiliary supply. Where the screens have a separate supply or are fed through series resistors of high enough value to produce a significant voltage drop, similar means of boosting the screen voltages may have to be used, depending on the precise condition obtaining.

As an alternative to the use of boosted auxiliary supplies, and remembering the remark just made about screen supplies, all of the heaters, including the rectifier heater where applicable, are disconnected from the mains transformer in the amplifier and are fed from a separate heater transformer; the B+ line is then boosted at will by connecting a variable auto-transformer or similar device to control the input to the normal mains transformer.

3. The amplifier is now switched on and loaded up into a dummy load by applying a single-tone input signal. Adjustments to the signal input level and the B+ boost must now be made successively until the maximum output power at the rated distortion figure is achieved. At the same time, the voltages around the output stage are the same as those measured and recorded in the first step.

It is important when making these measurements to keep such factors as screen dissipation in mind. It is quite possible to exceed permissible screen dissipation or even plate dissipation during this test, especially when it is recalled that valves are often run very close to their published maximum ratings under normal conditions. However, providing the setting up and measurement is carried out within a reasonable time it is unlikely that damage will result.

The matter of cathode bias has already been mentioned, but there are also many cases in audio amplifiers where fixed bias is used. In cases of this kind, suitable measures will be required to hold the bias at the correct value, depending on the precise circuit arrangement. Fixed bias is in general derived either from the main B+ supply or from an auxiliary power supply which uses the same mains transformer. Suitable steps must be taken, possibly by the temporary connection of a variable resistor or potentiometer into the circuit, to ensure that during the final measurement, the value of fixed bias is in fact the value that is obtained under normal quiescent conditions.

It was mentioned previously that small changes in the value of cathode bias would probably be of no effect on the measured results. However, if a more rigid approach is thought desirable, or the variation in voltage is significant, then measures similar to those just mentioned will be required to restore the voltage to the quiescent value. It is a fact that whilst a small change in cathode bias may have no measurable effect on the maximum power output, a greater effect could be found on the distortion content. Having said this, the matter can probably be left to the reader's discretion.

The measurement of music power in most transistorised amplifiers is a much simpler matter. As a rule, all that is necessary is to arrange for the mains input to the amplifier to be fed through an adjustable auto-transformer. This component can then be used to boost the collector supply voltage to the quiescent value, the general technique remaining as before. The absence of heaters greatly simplifies matters, although one must watch out for pilot lamps that might suffer damage; the answer is to remove them temporarily.

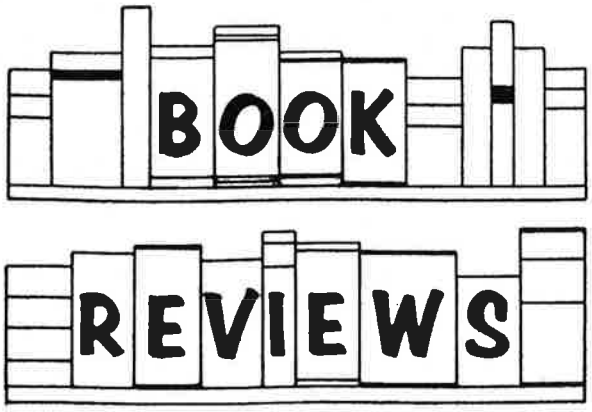
Some suggestions have been made that instead of the rather elaborate methods just described, a CRO be used to measure the music power rating. It has been suggested that the output of the amplifier be monitored on a CRO, and that programme material be fed into the amplifier, increasing gain and/or input level until clipping is observed on the programme peaks. The amplitude at which peak clipping sets in is then measured on the CRO and the corresponding output power calculated.

The utility of this method as far as the measurement of music power is concerned is doubted, except perhaps as a rough approximation. In the first place the conditions laid down in the definition are not complied with, as the definition calls for a single-tone input. Further, the mean programme level, which will cause some shift in dc conditions, in relation to the peak at which clipping is taking place is a difficult source of error either to evaluate or to allow for. Then again, the observation of fast transients on a CRO by eye is a notoriously difficult thing to do. It is, for example, quite likely that the clipping which is observed may be occurring on longer transients of less than maximum amplitude, whilst shorter transients of higher amplitude which are running past clipping level are unobserved due to their high writing speed. As far as any serious measurements are concerned it would seem that the CRO must be discounted.

The writer has had occasion to wonder just how frequently these measurements are in fact carried out. It is possible to arrive at a substantially similar result by graphical methods, which may well be cheaper than laboratory tests. Perhaps the thought could be left up in the air to see what comment it attracts.

The difference between rms power ratings and music power ratings will, as already mentioned, be affected by the regulation of the amplifier power supply, and also by the type of amplifier circuit configuration used. In a class A amplifier, the difference, if any, will be small. Class B is a broad term covering a wide area of operating conditions, which can probably most easily be individually described by the ratio of quiescent to full-load current. Those amplifiers in which the quiescent current is lowest or in which the ratio is highest will be expected to show the widest difference between rms and music power ratings. This is the sort of thing that is so confusing, it often renders direct comparison of different amplifiers impossible, and brings much derogatory comment upon the use of music power and peak music power ratings. Peak music power, as the name implies, is the peak power measured in the same way as music power.

One final thought before closing. Class D amplifiers, otherwise known as switching amplifiers or modulated pulse width amplifiers, could be back in the running in Australia, at least in experimental form, in a very short time. In fact, they may already be getting more mention by the time this note arrives. How will one apply music power ratings to these amplifiers, and what sort of ratio will there be between rms and music power ratings?




**"NONLINEAR & PARAMETRIC PHENOMENA IN RADIO ENGINEERING," A. Kharkevich, Edited by K. Pullen Jr., Iliffe Books Ltd., 190 pp inc. 151 text illustrations. Size 8¾" x 5½".**

Almost all electronic functions, rectification, detection, oscillation and so on, are inherently nonlinear. But even at this stage in the development of the art, comparatively few electronic engineers know a great deal about nonlinear circuit theory, apart from the simplest elements, such as the B-H curve, the construction of a load line, and the calculation of harmonic distortion.

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