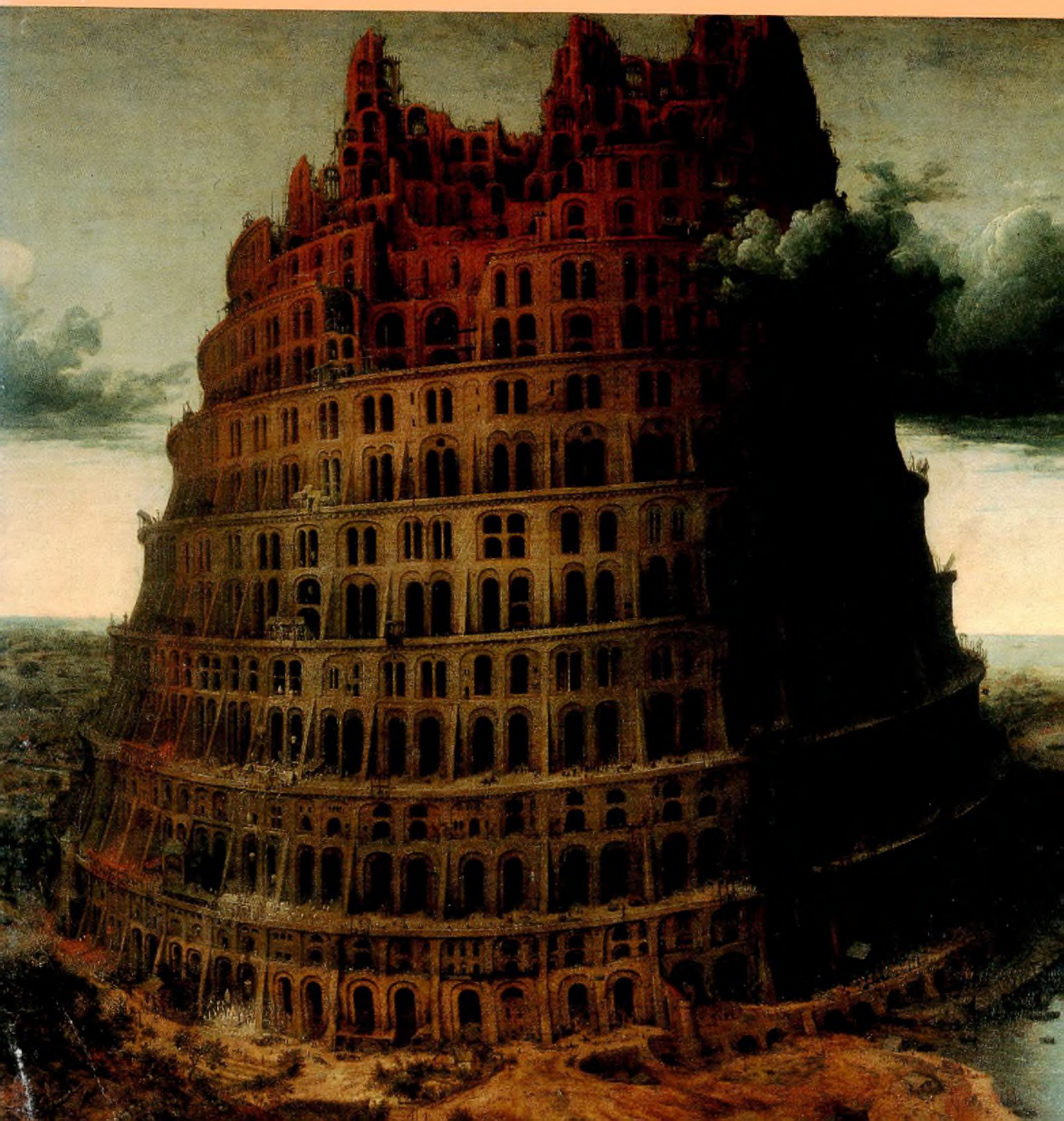
Electronic components & applications

Vol. 8, No



ISSN 1041 – 6219

Electronic components & applications

Volume 8, No.1

Contents

Since the dawn of history, man has striven to improve communication. His first primitive attempts with horns, drums and smoke signals had the major disadvantages of being short-distance and in code. Not till the invention of the telegraph, about 150 years ago, was a real breakthrough made. Although still in code, telegraphy opened the door for plain language, long-distance communication media such as telephony, radio and more recently, tv and computers. With every success, demands grew so that now the only way existing networks can efficiently handle the enormous volume of information that has become the life-blood of modern society is to go digital. The IST (Integrated Services Terminal) bus described on page 52 allows many benefits of the fully-digital ISDN systems of the future to be enjoyed today. The perfect communication medium may be in sight, but will this really lead to perfect understanding? Or will the legacy of Babel continue to confound us!

High-speed 12-bit tracking ADC using field-programmable logic sequencers

DAVID WONG

The high-speed 12-bit tracking ADC described in this article is based on two logic sequencers type PLS179 from our bipolar Schottky Programmable Logic Device (PLD) Series-24 (24-pin DIL) Family. These ICs are field-programmed by selective blowing of fusible Nichrome links and interconnected to form a 12-bit Successive Approximation Register (SAR), up/down counter and biphase clock generator. Features of the PLS179 logic sequencer are:

- 45 product terms (32 logic terms, 13 control terms)
- 20 inputs (8 dedicated)
- 4 I/Os and 8 registered I/Os
- typical propagation delay 25 ns (input to output)
- typical power dissipation 725 mW
- maximum clock frequency 18 MHz
- operating temperature range 0 to 75 °C
- encapsulated in 24-pin plastic DIL (PLS179N or 28-pin PLCC (PLS179A)
- supported by Automated Map And Zap Equation (AMAZE) PLD design software which is free of charge to PLD users.

Further details of the PLS179 and the AMAZE software are given in the Reference.

OPERATING PRINCIPLES OF THE ADC

The simplified block diagram in Fig.1 illustrates the principle of operation of the ADC.

When input $\overline{ST}$ is set LOW, the 12-bit SAR is initially loaded with its half full-scale value (2^{11} = 2048) which is then converted to analog form by a 12-bit DAC. An analog comparator senses whether the output level from the DAC is greater or less than the analog input level and causes the SAR to increment or decrement until parity is achieved by successive approximation. Output DONE is then set HIGH. When output DONE is HIGH, and as long as inputs $\overline{ST}$ and $\overline{HOLD}$ are HIGH, a tracking mode of operation is available during which the SAR is converted into a 12-bit up/down counter by setting the $\overline{TRACK}$ input LOW. The up/down counter is incremented or decremented under control of the COMPARE inputs at the rate of one LSB per clock period to follow the analog input variations. The up/down counting can be halted at any time by setting the $\overline{HOLD}$ input LOW. The digital data output then remains constant indefinitely. This facility provides a very good sample-and-hold function because, unlike with analog sample-and-hold circuits using capacitor storage, the output level doesn't decay due to charge leakage.

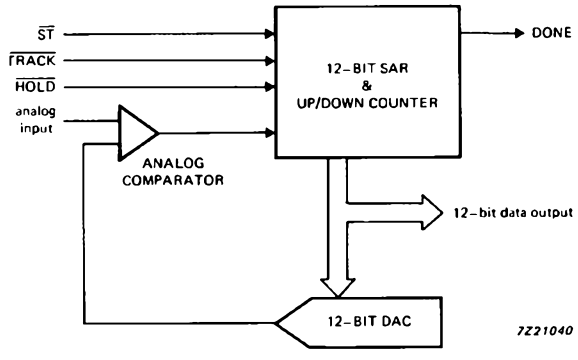


Fig.1 Simplified block diagram of the 12-bit high-speed ADC.

DETAILED DESCRIPTION OF THE ADC

Figure 2 is a complete schematic diagram of the ADC, Fig.3 is the timing diagram for the successive approximation cycle.

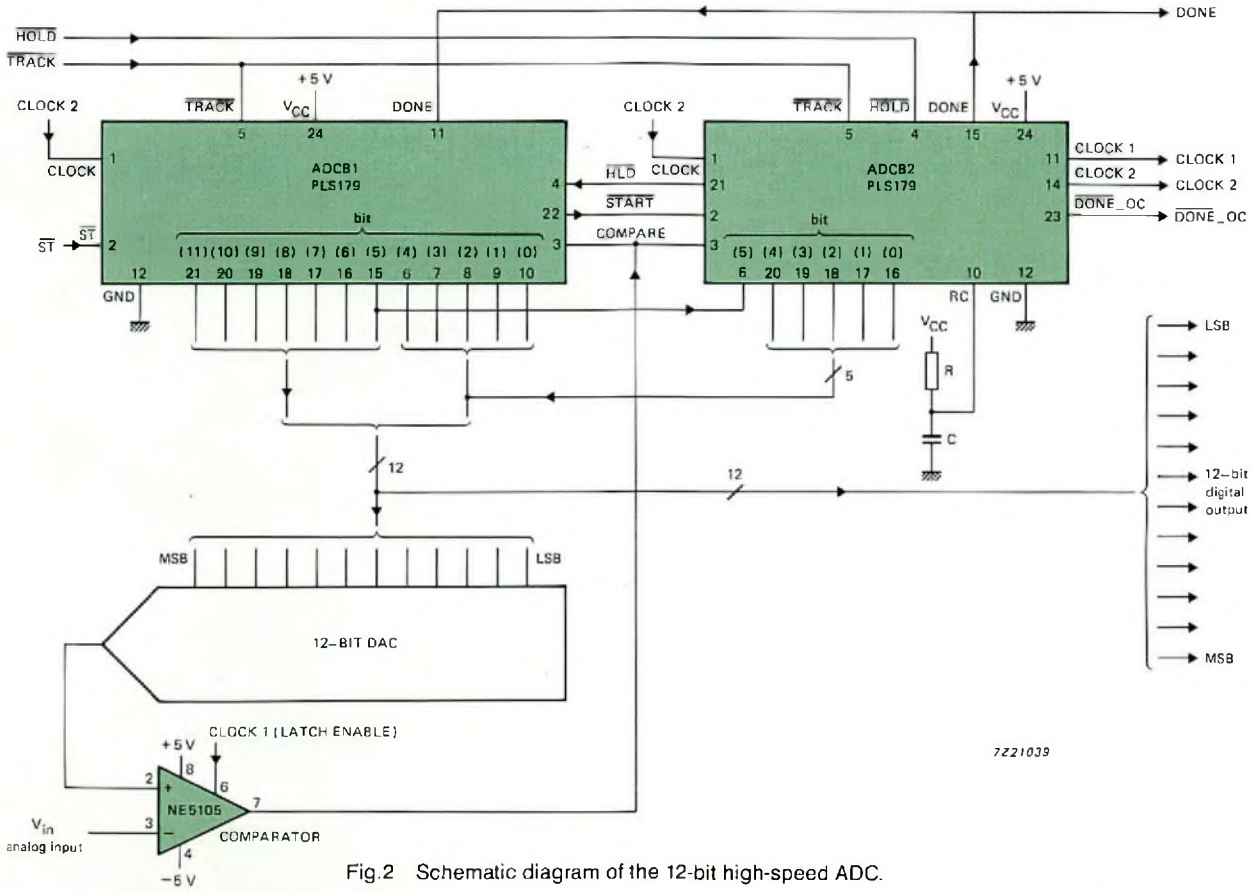


Fig.2 Schematic diagram of the 12-bit high-speed ADC.

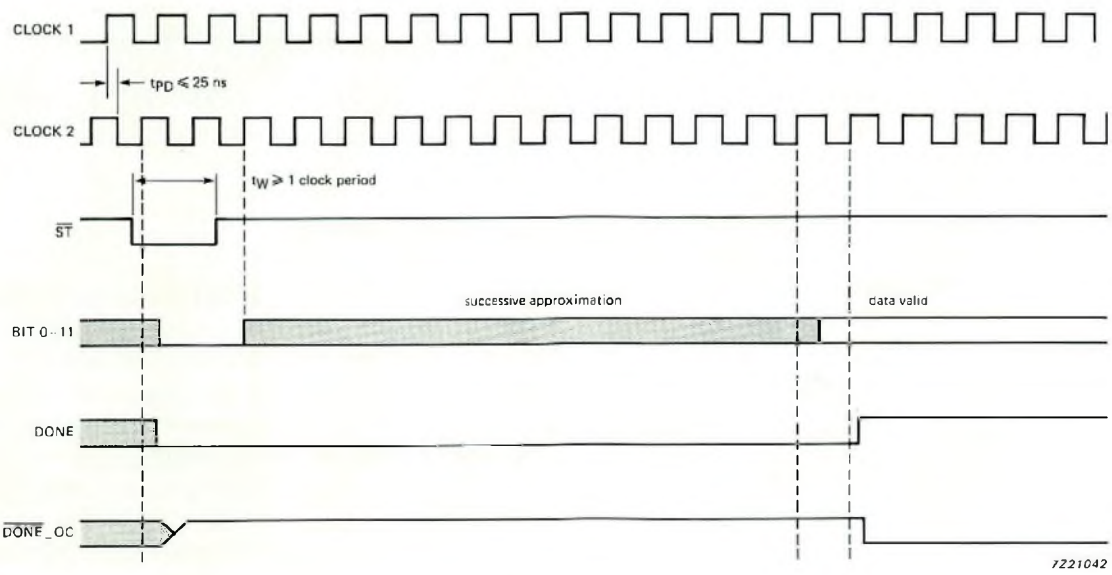


Fig.3 Timing diagram of the successive approximation cycle.

Successive approximation register

The starting conditions for the initial successive approximation cycle are the $\overline{\text{TRACK}}$ and $\overline{\text{HOLD}}$ inputs set HIGH and the $\overline{\text{ST}}$ input set LOW. On the rising edge of the first CLOCK 2 pulse after the $\overline{\text{ST}}$ input has been set LOW, the 12-bit SAR is loaded with its half full-scale value (2^{11} = binary 2048) and the DONE output is reset LOW (open-collector output $\overline{\text{DONE}}$_OC high-impedance). The digital output from the SAR is in natural binary format i.e. if all twelve bits are '0' the digital output value is zero; if all twelve bits are '1' the digital output value is $2^{12} - 1 = 4095$. As shown in Fig.2, bits 0 to 4 are registered in PLS179 ADCB2 and bits 5 to 11 are registered in PLS179 ADCB1.

The digital output value from the SAR (initially binary 2048) is converted to analog form by the 12-bit DAC and compared with the analog input level by the SE/NE5105 comparator. The comparator output (HIGH if the digital output value is greater than the analog input level, and LOW if it is less) is applied to the COMPARE input of both PLS179s. The output from the SE/NE5105 comparator is latched by CLOCK 1 to prevent violation of the set-up time due to changes of the analog input level whilst the SAR/counter is incrementing/decrementing. If an analog comparator without a latching facility is used instead of an SE/NE5105, an external latch must be used.

Figure 4 is a flow chart of the successive approximation algorithm for the SAR which can be summarized as follows. If the digital output value from the ADC is greater than the analog input level (D>A), move the last bit in the SAR that was set to '1' one position to the right; otherwise, set the next bit to the right to '1'. Repeat this procedure until all 12 bits have been operated upon. Consequently, the last action in the successive approximation cycle is always to set the LSB in the SAR (bit 0) to '1'.

At the rising edge of the CLOCK 2 pulse following the setting of the LSB in the SAR to '1', the initial successive approximation cycle is complete and output DONE is set HIGH and open-collector output $\overline{\text{DONE}}$_OC is set LOW. The states of these two outputs are latched until they are reset by setting the $\overline{\text{ST}}$ input LOW again to start another successive approximation cycle. Bit maps illustrating the SAR contents during successive approximation of analog input levels higher and lower than the initial half full-scale value of the SAR (binary 2048) are given in Fig.5 and Fig.6 respectively.

The initial successive approximation cycle takes 13 periods of CLOCK 2 to complete. It is essential that the analog input level to the comparator remains constant during this period. If rapidly varying analog inputs are to be converted it will therefore be necessary to incorporate an analog sample-and-hold circuit (controlled by output DONE) at the analog input to the ADC.

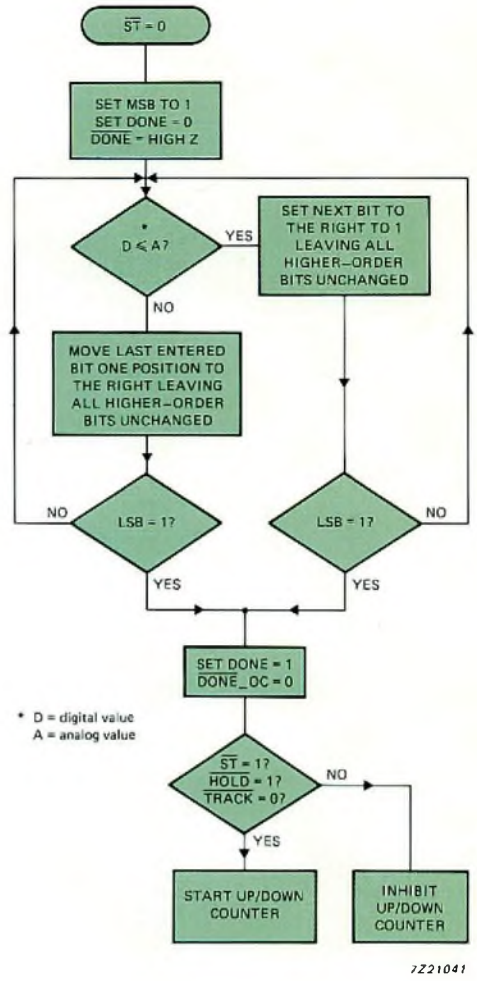


Fig.4 Flow chart of the SAR algorithm.

Up/down counter

When output DONE is HIGH (successive approximation cycle complete) and input $\overline{\text{HOLD}}$ is HIGH, input $\overline{\text{TRACK}}$ can be set LOW to convert the SAR into a 12-bit up/down counter consisting of 12 toggle flip-flops, each with two p-terms for directional control. The up/down counter can track variations of the level of the analog input signal at the rate of one LSB per CLOCK 2 period. The counting can be inhibited at any time by setting the $\overline{\text{HOLD}}$ input LOW. The digital output value from the ADC then remains constant indefinitely.

A = 3000

D	BIT NUMBER												
	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	set to half full-scale
2048	1	0	0	0	0	0	0	0	0	0	0	0	D < A: set bit 10 to 1
3072	1	1	0	0	0	0	0	0	0	0	0	0	D > A: shift bit 10 right
2560	1	0	1	0	0	0	0	0	0	0	0	0	D < A: set bit 8 to 1
2816	1	0	1	1	0	0	0	0	0	0	0	0	D < A: set bit 7 to 1
2944	1	0	1	1	1	0	0	0	0	0	0	0	D < A: set bit 6 to 1
3000	1	0	1	1	1	1	0	0	0	0	0	0	D = A: set bit 5 to 1
3032	1	0	1	1	1	1	1	0	0	0	0	0	D > A: shift bit 5 right
3016	1	0	1	1	1	1	0	1	0	0	0	0	D > A: shift bit 4 right
3008	1	0	1	1	1	1	0	0	1	0	0	0	D > A: shift bit 3 right
3004	1	0	1	1	1	1	0	0	0	1	0	0	D > A: shift bit 2 right
3002	1	0	1	1	1	1	0	0	0	0	1	0	D > A: shift bit 1 right
3001	1	0	1	1	1	1	0	0	0	0	0	1	LSB=1: set DONE=1
	MSB											LSB	

D = digital value
A = analog value

Fig.5 SAR bit map for counting up to binary 3000.

A = 523

D	BIT NUMBER												
	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	set to half full-scale
2048	1	0	0	0	0	0	0	0	0	0	0	0	D > A: shift bit 11 right
1024	0	1	0	0	0	0	0	0	0	0	0	0	D > A: shift bit 10 right
512	0	0	1	0	0	0	0	0	0	0	0	0	D < A: set bit 8 to 1
768	0	0	1	1	0	0	0	0	0	0	0	0	D > A: shift bit 8 right
640	0	0	1	0	1	0	0	0	0	0	0	0	D > A: shift bit 7 right
576	0	0	1	0	0	1	0	0	0	0	0	0	D > A: shift bit 6 right
544	0	0	1	0	0	0	1	0	0	0	0	0	D > A: shift bit 5 right
528	0	0	1	0	0	0	0	1	0	0	0	0	D > A: shift bit 4 right
520	0	0	1	0	0	0	0	0	1	0	0	0	D < A: set bit 2 to 1
524	0	0	1	0	0	0	0	0	1	1	0	0	D > A: shift bit 2 right
522	0	0	1	0	0	0	0	0	1	0	1	0	D < A: set bit 1 to 1
523	0	0	1	0	0	0	0	0	1	0	1	1	LSB=1: set DONE=1
	MSB											LSB	

D = digital value
A = analog value

Fig.6 SAR bit map for counting down to binary 523.

Input latches

Since inputs $\overline{ST}$ and $\overline{HOLD}$ may not be synchronised with CLOCK 2 there would be a possibility of them assuming a metastable state if some precautions were not taken. They are therefore each effectively latched by a flip-flop and two p-terms configured as a non-inverting D flip-flip at outputs $\overline{START}$ and $\overline{HDL}$ respectively. Once latched, their logic states become effective at the rising edge of the next clock pulse.

Clock generator

PLS179 ADCB2 generates biphase clock pulses (CLOCK 1 and CLOCK 2), the frequency of which is controlled by the RC network at pin RC. It is recommended that the value of the capacitor be made less than 1 nF. The actual RC time-constant for a particular frequency must be determined experimentally (see Application Note 13 in the Reference for further details). The two clocks are basically anti-phase but the propagation delay of CLOCK 2 is 25 ns longer than that of CLOCK 1. CLOCK 2 controls the SAR and the up/down counter. CLOCK 1 controls the comparator latch.

Comparator SE/NE5105

Our high-speed, high-precision comparator SE/NE5105 has an input offset voltage of only 100 μV, an input offset current of 3 nA and a response time of 36 ns with 1.2 mV of overdrive. It operates from a dual 5 V supply and incorporates an active-HIGH output latch. It has a voltage gain of 88 dB and is capable of driving 10 TTL loads.

FIELD PROGRAMMING THE PLS179s

The PLS179s are field-programmed using our PLD programming software called Automated Map And Zap Equation (AMAZE) as shown in the appendices. The SAR circuit is first designed as a state-machine (file name: ADCS.SEE) and then, after pin assignments have been made, partitioned into two PLS179s. The up/down counter, input latches, bi-phase clock generator and open-collector output $\overline{DONE}$_OC are then implemented by using Boolean equations in the appropriate .BEE files (file names: ADCB.BEE and ADCB2.BEE) in AMAZE. These files are then assembled to produce fuse maps for programming the two PLS179s (ADCB1.STD and ADCB2.STD).

AMAZE SOFTWARE

The AMAZE software consists of the following five modules:

- Boolean Logic And State Transfer (BLAST) entry program
- Program Table Editor (PTE)
- PAL To PLD (PTP) conversion program
- Device Programmer Interface (DPI) program
- PLD SIMulator (PLD SIM) program.

Each AMAZE software package will be made available in various combinations of the foregoing modules.

Features

- multiple modules allow expansion for future requirements
- modules are user-friendly
- both HELP and ERROR messages available
- document print-out: header, pin diagram, Boolean equation and fuse map
- interfaces with most commercially available programmers
- SIMULATOR programs provide test and applications assistance

BLAST module

This module helps engineers to implement their designs in PLD logic. It checks design data and automatically compiles a program table from Boolean and state-machine equations. Data from the program table is then used to produce a Standard File which contains the fusing codes in a form that is acceptable to AMAZE modules PLD SIM and DPI.

BLAST reports any logic or syntax errors and lists the equations in a sum-of-products form which helps the user to minimize the number of logic equations entered. BLAST automatically partitions state-machine designs into specified devices and then deletes any redundant terms during compilation.

BLAST can also be used to modify a logic-set currently programmed into a device by overlaying new data onto unused fuses.

The main features of BLAST are:

- screen menus for inputs
- full compiler for performing product term manipulation
- document print-out: header, pin diagram, fuse map etc.

PTE module

The Program Table Entry (PTE) module is an interactive editor which allows the logic designer to enter data into AMAZE in the form of program tables. Each PLD data sheet in the Reference includes the program table format applicable to the specified IC. PTE can also be used to document completed designs and to change logic functions which have previously been defined in the BLAST module.

The main features of PTE are:

- program tables are exactly as defined in the data sheets
- interactive with BLAST
- uses our standard H and L input format.

PTP module

The Programmable array logic To Programmable logic device (PTP) module is a conversion program which allows easy transfer of the PAL20 circuits to our 20-pin PLDs. PTP can automatically upload the PAL pattern from a commercially available programmer, convert the pattern into a PLD pattern, and then download it into the programmer. The PAL pattern and its corresponding PLD pattern are documented, and the PLD pattern can be directed to other AMAZE modules. PTP can also convert the PAL fuse file in a HEXPLOT format.

The main features of PTP are:

- automatic assembler
- reduces duplicated p-terms
- supports all our 20-pin PLS15X programmable logic sequencers.

DPI module

The Device Programmer Interface (DPI) software module provides the interface between the standard file created by the AMAZE modules and a commercial programmer. It allows both download (sending from host to programmer) and upload (sending from programmer to host) operations. It supports both JEDEC and our H and L formats to convey fusing information to and from most commercially available programmers.

The main features of DPI are:

- screen menus for inputs
- provides JEDEC or H and L formats
- download/upload to/from commercially available programmers uses our standard H and L input format.

PLD SIM module

The PLD SIMulator (PLD SIM) software module simulates the operation of the logic defined for our PLDs. The input to the program is the Standard File generated by other AMAZE modules. The simulator can be run manually or automatically. In the automatic mode, it creates a file of vectors for testing the programmed IC. In the manual mode, it allows the operator to assign an input vector and observe the resultant output.

The main features of PLD SIM are:

- simple input form
- test vector generation (on Rev.D or later)
- output can be used as input to PLD fault grader
- software applications support prior to programming.

AMAZE software compatibility

software	*hardware requirements*
82SOFT523-SS	IBM-PC or IBM-XT or compatible computer 256K memory PC-DOS operating system, version 2.0 or higher 2 floppy disc drives or 1 floppy + 1 hard disc
82SOFT211-SS	VAX series computer VMS operating system (any revision)

AMAZE is supplied fully-documented and complete with the appropriate magnetic media. Applications support is provided by our field service engineers in most areas. Contact your local sales organization listed on the rear cover for further information about AMAZE and our Programmable Logic Devices (PLDs).

REFERENCE

Philips Data Handbook IC13 "Semi-custom Programmable Logic Devices (PLD)", ordering code 9398 139 00011.

Appendix 1 – State equations for the SAR

```
@DEVICE SELECTION
ADCB1/PLS179
ADCB2/PLS179

@STATE VECTORS
[ /START, BIT11, BIT10, BIT9, BIT8, BIT7, BIT6, BIT5, BIT4, BIT3, BIT2,
BIT1, BIT0, DONE ]

INIT       = 0 ---- ---- ---- - b ;   "START CONVERSION PROCESS"
HALFSCALE  = - 1000 0000 0000 0 b ;   "SET SAR TO HALF SCALE"
ST2048     = 1 1000 0000 0000 0 b ;   "PRESENT STATE = 2048 (HALF SCALE)"
ST1024     = 1 -100 0000 0000 0 b ;
ST512      = 1 --10 0000 0000 0 b ;
ST256      = 1 ---1 0000 0000 0 b ;
ST128      = 1 ---- 1000 0000 0 b ;
ST64       = 1 ---- -100 0000 0 b ;
ST32       = 1 ---- --10 0000 0 b ;
ST16       = 1 ---- ---1 0000 0 b ;
ST8        = 1 ---- ---- 1000 0 b ;
ST4        = 1 ---- ---- -100 0 b ;
ST2        = 1 ---- ---- --10 0 b ;
ST1        = 1 ---- ---- ---1 0 b ;

AD1024     = - -1-- ---- ---- - b ;   "ADD 1 BIT TO THE RIGHT"
AD512      = - --1- ---- ---- - b ;
AD256      = - ---1 ---- ---- - b ;
AD128      = - ---- 1--- ---- - b ;
AD64       = - ---- -1-- ---- - b ;
AD32       = - ---- --1- ---- - b ;
AD16       = - ---- ---1 ---- - b ;
AD8        = - ---- ---- 1--- - b ;
AD4        = - ---- ---- -1-- - b ;
AD2        = - ---- ---- --1- - b ;
AD1        = - ---- ---- ---1 - b ;
END        = - ---- ---- ---- 1 b ;

SH1024     = - 01-- ---- ---- - b ;   "SHIFT ONE BIT TO THE RIGHT"
SH512      = - -01- ---- ---- - b ;
SH256      = - --01 ---- ---- - b ;
SH128      = - ---0 1--- ---- - b ;
SH64       = - ---- 01-- ---- - b ;
SH32       = - ---- -01- ---- - b ;
SH16       = - ---- --01 ---- - b ;
SH8        = - ---- ---0 1--- - b ;
SH4        = - ---- ---- 01-- - b ;
SH2        = - ---- ---- -01- - b ;
SH1        = - ---- ---- --01 - b ;
SH0        = - ---- ---- ---0 1 b ;

@INPUT VECTORS
[ COMPARE ]
GREATER = 1 b ;  "IF DIGITAL OUTPUT IS GREATER THAN ANALOG INPUT, ...."
LESS    = 0 b ;  "IF DIGITAL OUTPUT IS LESS THAN ANALOG INPUT, ...."
```

Appendix 1 (cont.)

```
@OUTPUT VECTORS

@TRANSITIONS
WHILE [ INIT ]
        IF [] THEN [ HALFSCALE ]  "INITIALIZE REGISTER TO HALF SCALE"
WHILE [ ST2048 ]
        IF [ GREATER ] THEN [ SH1024 ] "IF GREATER THAN, SHIFT 1 BIT"
        IF [ LESS ] THEN [ AD1024 ]    "IF LESS THAN, ADD 1 BIT"
WHILE [ ST1024 ]
        IF [ GREATER ] THEN [ SH512 ]
        IF [ LESS ] THEN [ AD512 ]
WHILE [ ST512 ]
        IF [ GREATER ] THEN [ SH256 ]
        IF [ LESS ] THEN [ AD256 ]
WHILE [ ST256 ]
        IF [ GREATER ] THEN [ SH128 ]
        IF [ LESS ] THEN [ AD128 ]
WHILE [ ST128 ]
        IF [ GREATER ] THEN [ SH64 ]
        IF [ LESS ] THEN [ AD64 ]
WHILE [ ST64 ]
        IF [ GREATER ] THEN [ SH32 ]
        IF [ LESS ] THEN [ AD32 ]
WHILE [ ST32 ]
        IF [ GREATER ] THEN [ SH16 ]
        IF [ LESS ] THEN [ AD16 ]
WHILE [ ST16 ]
        IF [ GREATER ] THEN [ SH8 ]
        IF [ LESS ] THEN [ AD8 ]
WHILE [ ST8 ]
        IF [ GREATER ] THEN [ SH4 ]
        IF [ LESS ] THEN [ AD4 ]
WHILE [ ST4 ]
        IF [ GREATER ] THEN [ SH2 ]
        IF [ LESS ] THEN [ AD2 ]
WHILE [ ST2 ]
        IF [ GREATER ] THEN [ SH1 ]
        IF [ LESS ] THEN [ AD1 ]
WHILE [ ST1 ]
        IF [ GREATER ] THEN [ SH0 ]
        IF [] THEN [END]
```

Appendix 2 – Pin lists

```
File Name : ADCB1
Date :
Time :

######################## P I N   L I S T ########################

   LABEL     ** FNC **PIN --------- PIN** FNC **     LABEL
CLOCK        ** CK  **  1-|       |-24 ** +5V **VCC
/ST          ** I   **  2-|       |-23 ** /B  **N/C
COMPARE      ** I   **  3-|       |-22 ** O   **/START
/HLD         ** I   **  4-|   P   |-21 ** O   **BIT11
/TRACK       ** I   **  5-|   L   |-20 ** O   **BIT10
BIT4         ** I   **  6-|   S   |-19 ** O   **BIT9
BIT3         ** I   **  7-|   1   |-18 ** O   **BIT8
BIT2         ** I   **  8-|   7   |-17 ** O   **BIT7
BIT1         ** I   **  9-|   9   |-16 ** O   **BIT6
BIT0         ** I   ** 10-|       |-15 ** O   **BIT5
DONE         ** I   ** 11-|       |-14 ** /B  **N/C
GND          ** OV  ** 12-|       |-13 ** /OE **N/C
                          ---------
```

```
File Name : ADCB2
Date :
Time :

######################## P I N   L I S T ########################

   LABEL     ** FNC **PIN --------- PIN** FNC **     LABEL
CLOCK        ** CK  **  1-|       |-24 ** +5V **VCC
/START       ** I   **  2-|       |-23 ** /B  **/DONE_OC
COMPARE      ** I   **  3-|       |-22 ** B   **N/C
/HOLD        ** I   **  4-|   P   |-21 ** O   **/HLD
/TRACK       ** I   **  5-|   L   |-20 ** O   **BIT4
BIT5         ** I   **  6-|   S   |-19 ** O   **BIT3
N/C          ** I   **  7-|   1   |-18 ** O   **BIT2
N/C          ** I   **  8-|   7   |-17 ** O   **BIT1
N/C          ** I   **  9-|   9   |-16 ** O   **BIT0
RC           ** /B  ** 10-|       |-15 ** O   **DONE
CLOCK1       ** O   ** 11-|       |-14 ** /O  **CLOCK2
GND          ** OV  ** 12-|       |-13 ** /OE **N/C
                          ---------
```

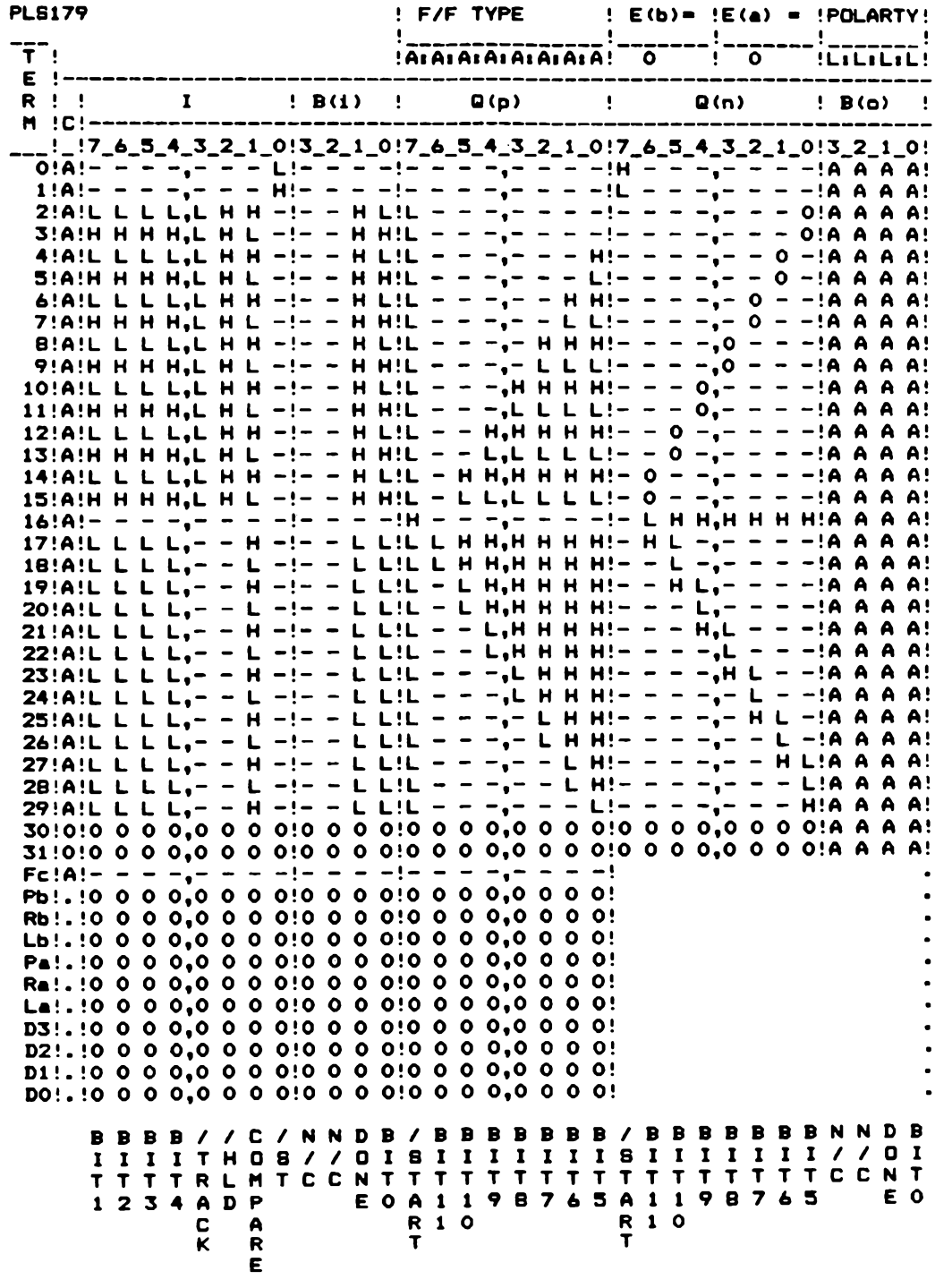
Appendix 3 – Boolean equations for the up/down counter and input latches

```
@DEVICE TYPE
PLS179
@DRAWING
@REVISION
@DATE
@SYMBOL
    FILE NAME : ADCB1

@COMPANY
@NAME
@DESCRIPTION
@COMMON PRODUCT TERM
@COMPLEMENT ARRAY
@I/O DIRECTION
@OUTPUT POLARITY
@FLIP FLOP CONTROL
     FC = 1 ;          "SET ALL FLIP FLOP TO BE J/K"

@OUTPUT ENABLE
@REGISTER LOAD
@ASYNCHRONOUS PRESET/RESET
@FLIP FLOP MODE
@LOGIC EQUATION
 "NON-INVERTING INPUT LATCH: /START = /ST "
  START  : J =  ST ;
           K = /ST ;
 "UP/DOWN COUNTER ROUTINE"
  /BIT5  : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 +
               /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *
                BIT2 *  BIT3 * BIT4 ;
  /BIT6  : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 * /BIT5 +
               /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *
                BIT2 *  BIT3 * BIT4 *  BIT5 ;
  /BIT7  : T = /START * TRACK * DONE * /HLD *  COMPARE *
               /BIT0 * /BIT1 * /BIT2 * /BIT3 * /BIT4 * /BIT5 * /BIT6 +
               /START * TRACK * DONE * /HLD * /COMPARE *
                BIT0 *  BIT1 *  BIT2 *  BIT3 *  BIT4 *  BIT5 *  BIT6 ;
  /BIT8  : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 * /BIT5 * /BIT6 * /BIT7 +
               /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *
                BIT2 *  BIT3 *  BIT4 *  BIT5 *  BIT6 *  BIT7 ;
  /BIT9  : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 * /BIT5 * /BIT6 * /BIT7 * /BIT8 +
               /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *
                BIT2 *  BIT3 *  BIT4 *  BIT5 *  BIT6 *  BIT7 *  BIT8 ;
  /BIT10 : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 * /BIT5 * /BIT6 * /BIT7 * /BIT8 *
               /BIT9 +
               /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *
                BIT2 *  BIT3 *  BIT4 *  BIT5 *  BIT6 *  BIT7 *  BIT8 *
                BIT9 ;
  /BIT11 : T = /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 *
               /BIT2 * /BIT3 * /BIT4 * /BIT5 * /BIT6 * /BIT7 * /BIT8 *
               /BIT9 *
               /BIT10 +
               /START * TRACK * DONE * /HLD * /COMPARE * BIT0 * BIT1 *
                BIT2 *  BIT3 *  BIT4 *  BIT5 *  BIT6 *  BIT7 *  BIT8 *
                BIT9 *  BIT10 ;
```

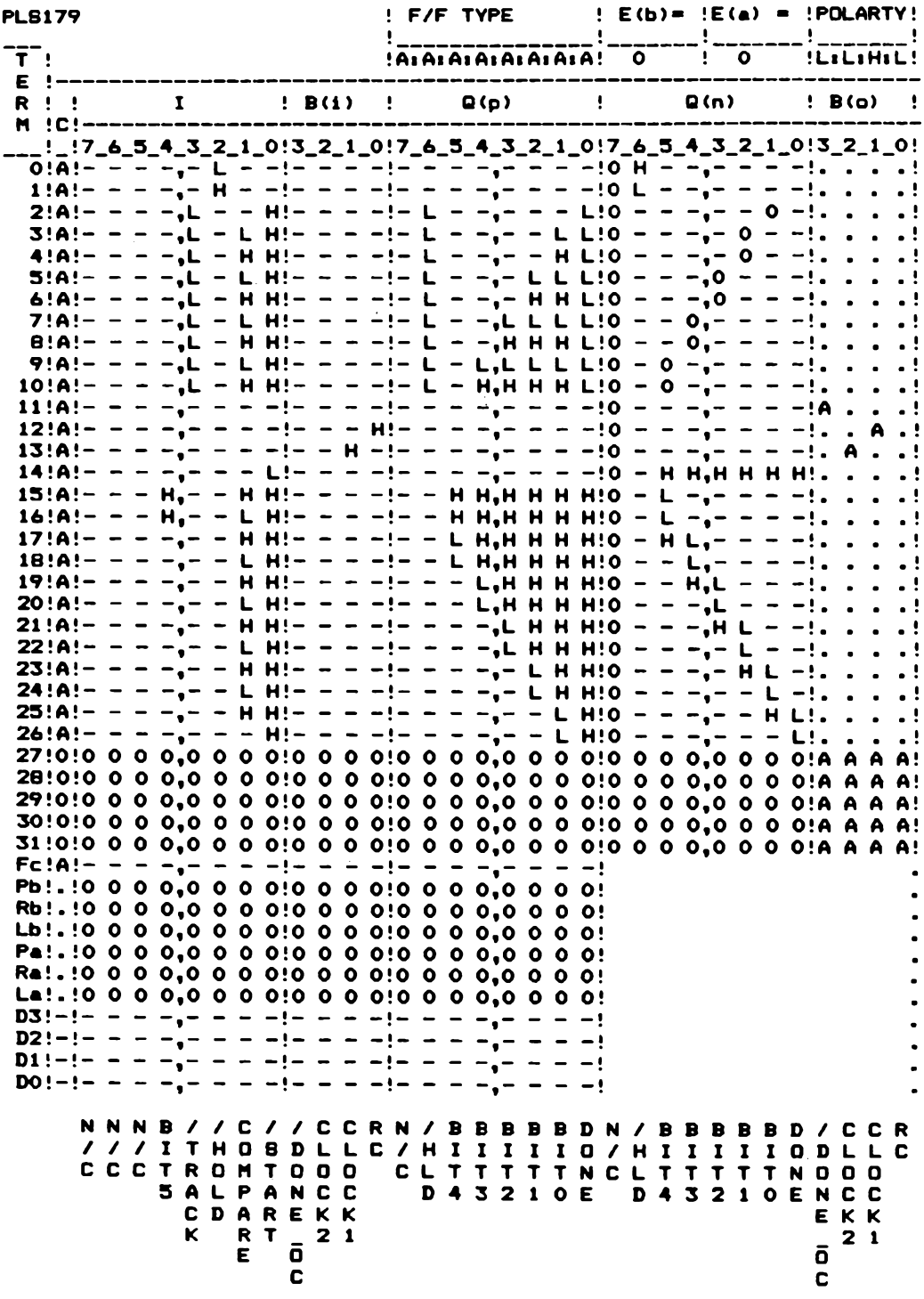
Appendix 3 (cont.)

```
@DEVICE TYPE
PLS179
@DRAWING
@REVISION
@DATE
@SYMBOL
  FILE NAME :  ADCB2

@COMPANY
@NAME
@DESCRIPTION
@COMMON PRODUCT TERM
@COMPLEMENT ARRAY
@I/O DIRECTION
     DO = RC ;            "RC OSCILLATOR"
     D3 = DONE ;          "ENABLE /DONE_OC TO OUTPUT A LOGIC LOW."
@OUTPUT POLARITY
@FLIP FLOP CONTROL
     FC = 1 ;
@OUTPUT ENABLE
@REGISTER LOAD
@ASYNCHRONOUS PRESET/RESET
@FLIP FLOP MODE
     "M0, M1, M2, M3, M4, M5 = 1 ;  SET F0 - F5 TO J/K FLIP FLOPS."

@LOGIC EQUATION
 "NON-INVERTING INPUT LATCH :  /HLD = /HOLD "
  HLD    : J =  HOLD ;
           K = /HOLD ;

 "UP/DOWN COUNTER ROUTINE"
 /BIT0   : T = /START * TRACK * DONE * /HLD ;
 /BIT1   : T = /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 +
               /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 ;
 /BIT2   : T = /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 +
               /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 ;
 /BIT3   : T = /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *  BIT2 +
               /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 * /BIT2 ;
 /BIT4   : T = /START * TRACK * DONE * /HLD * /COMPARE *  BIT0 *  BIT1 *  BIT2 *
                BIT3 +
               /START * TRACK * DONE * /HLD *  COMPARE * /BIT0 * /BIT1 * /BIT2 *
               /BIT3 ;
 /DONE_OC    = /( 1 ) ;

 "RC OSCILLATOR"
  RC         = /(1) ;
  CLOCK1     = RC ;
  CLOCK2     = /( CLOCK1 ) ;        "BUILT-IN DELAY OF 1 tPD"
```

Appendix 4 – Fuse maps



Appendix 4 (cont.)



Ceramic-chip capacitors
high-rel products with a promising future

W. LANGENHORST and R. WASER

As surface-mount technology started picking up in a big way, it was inevitable that it would create headaches for component manufacturers. The task of converting leaded components into SMDs isn't always a straightforward one, and if these components have to be supplied as naked chips, the headaches, for some manufacturers at least, can be quite severe.

A perfect example of this can be found in ceramic-multilayer capacitors. In earlier times when these were leaded devices, a lot of manufacturers experienced a disturbing number of early failures due to breakdown at low voltage. These failures were the result of metallic bridging between electrodes induced by electromigration. And this was caused by ingress of moisture due to delamination, cracks and voids in the ceramic, all the result of poor manufacturing methods. The answer was quite simple. Many manufacturers just sealed the ceramic from moisture by encapsulating their capacitors, and were thus able to continue with their manufacturing methods unchanged. The customer, of course, was quite satisfied since these encapsulated capacitors were then perfectly reliable.

For these manufacturers, however, the problem was not solved, just contained. And with the rapid growth of surface-mount technology, ceramic-multilayer capacitors in chip form became increasingly in demand and the problem returned. This time there could be no easy answer, so despite their many attractive properties, ceramic-'chip' capacitors have not been accepted by the market as readily as they might have been.

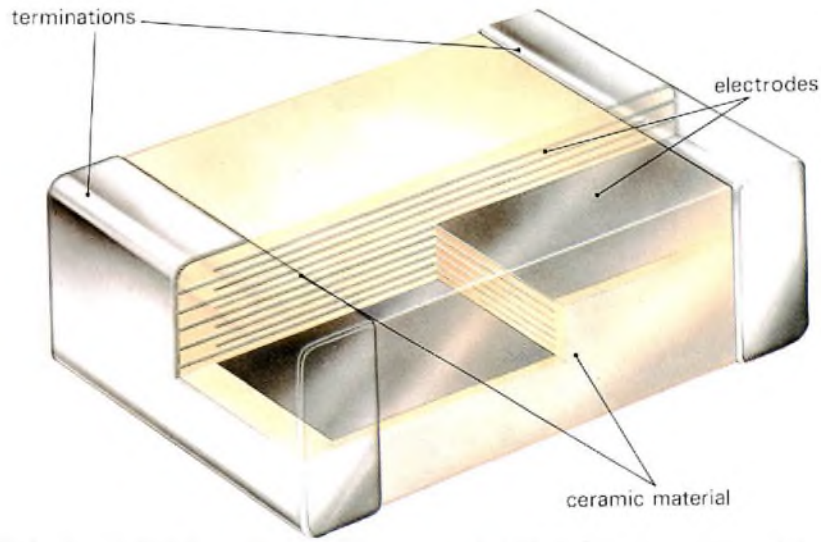


Fig.1 Ceramic 'chip' capacitors can't be encapsulated like their leaded counterparts to protect them from ingress of moisture. Exacting manufacturing methods are the only way to guarantee their integrity

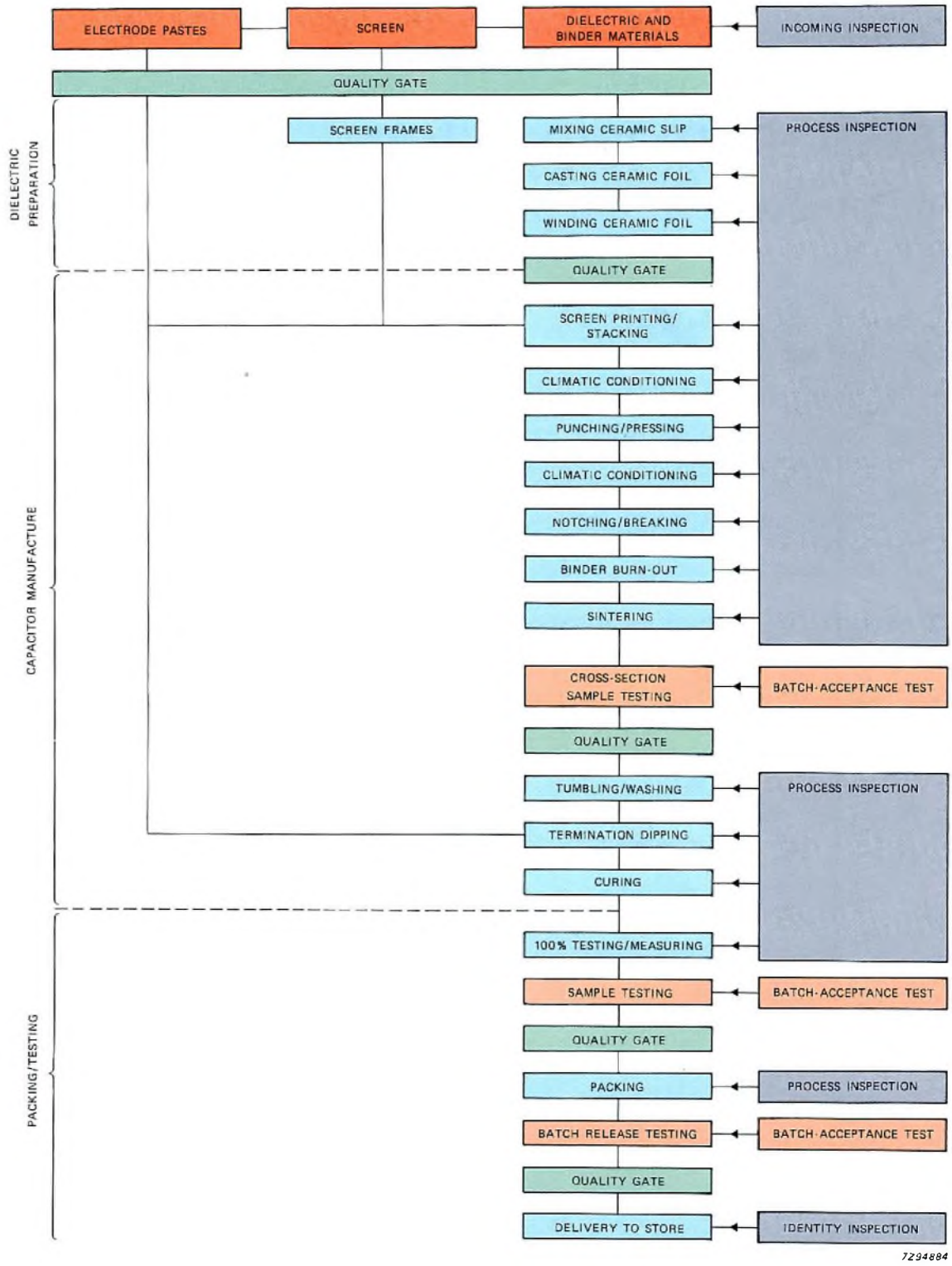


Fig.2 Production flow chart for our ceramic multilayer capacitors showing the principal features assuring their high quality which includes among other things their immunity from low-voltage breakdown

But not all manufacturers relied solely on encapsulation to guarantee the integrity of their multilayer capacitors. For many, their manufacturing methods were sufficiently stringent from the start to assure that their capacitors would never suffer from low-voltage breakdown. For these manufacturers, the apparent reluctance of the market to accept ceramic-chip capacitors is totally unjustified.

Our ceramic-multilayer capacitors are a prime example of this. Recognizing at an early stage the coming importance of surface-mount technology, we entered the market directly with chip capacitors. Our manufacturing methods, therefore, had to be stringent from the start, with the result that our capacitors are virtually immune from low-voltage breakdown. With this, potentially the most common cause of early failure in ceramic-multilayer capacitors, eradicated, the short-term reliability of our capacitors, as we'll demonstrate, can be considered beyond reproach.

And what of long-term reliability? Long-term failures are generally a function of material properties, and one of the most common causes of long-term failure in ceramic-multilayer capacitors has been dielectric degradation. This is the decrease in insulation resistance that can occur when a capacitor is stressed at high voltage and high temperature over a long period. Since dielectric degradation occurs only late in life, and ceramic-multilayer capacitors normally have a very long lifetime, it's difficult to detect by normal life testing.

Using accelerated-life testing techniques, however, at temperatures up to 500 °C and voltages up to 250 V, we've demonstrated that the ceramic used in our capacitors is highly stable and not subject to dielectric degradation during the normal lifetime of the capacitors. Thanks to these stringent testing techniques and to the advances in ceramic technology made in recent years, we can confidently predict lifetimes for our ceramic multilayer capacitors running into tens or even hundreds of years.

EXACTING MANUFACTURING METHODS

Figure 2 is a production flow chart for our ceramic-multilayer capacitors showing the features assuring their integrity. Foremost among these are the following:

- Careful control of ceramic properties. This is done by our incoming inspection procedure which accepts only the highest grade ceramic and which carefully meters particle size (Fig.3) to ensure optimum size distribution to produce the best possible ceramic density.
- The use of a proprietary multilayer manufacturing process specially developed to optimize ceramic properties and minimize mechanical defects (see box).
- Built-in safety margins on key parameters such as dielectric thickness and creepage distance. The latter, which is the overlap between adjacent silver-palladium electrodes and hence the distance between each set of electrodes and the opposite end termination (Fig.4), must be greater than 0,15 mm.
- Closely controlled in-line processes (see Fig.2).
- 100% final electrical inspection in which the capacitors are subjected to a 350 V pulse (6 times nominal voltage). Although not in itself a test that induces low-voltage failure, this test is invaluable for weeding out weak components and components that may later become liable to low-voltage failure.

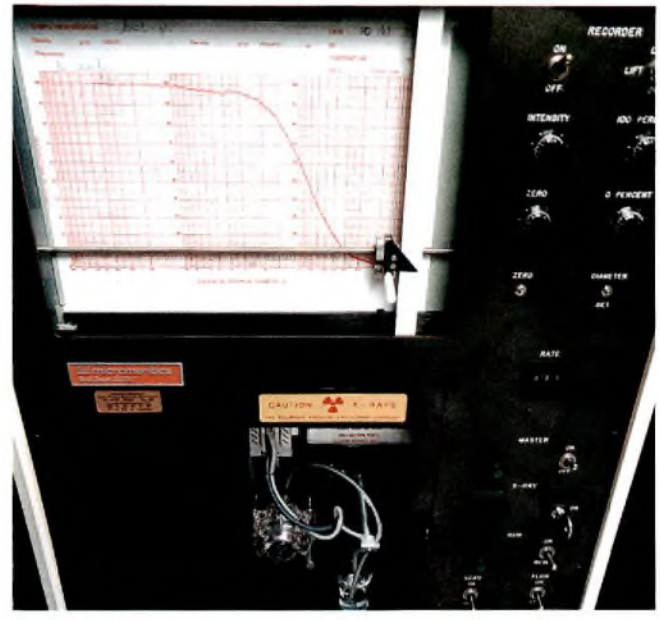


Fig.3 The equipment shown here meters particle size to ensure that we use only the highest grade ceramic

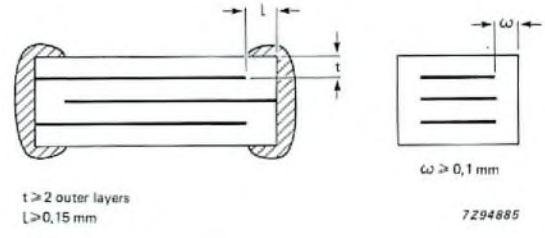


Fig.4 The overlap between adjacent silver-palladium layers determines the gap between each set of electrodes and the opposite end termination. This gap can form a creepage current path and is hence known as the creepage distance. Thanks to our proprietary manufacturing process (see box) we can ensure that this distance is never less than 0,15 mm

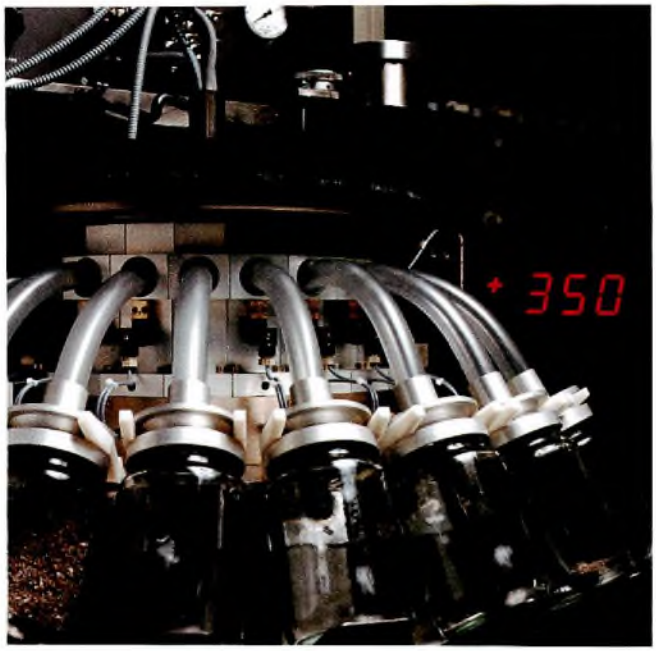


Fig.5 Capacitors undergoing 100% final electrical inspection. More than 40 000 capacitors an hour can be tested with this equipment which among other things subjects each capacitor to a 350 V pulse

THE CERAMIC IS THE KEY

A major feature of our manufacturing process is the use of a water-based system for manufacturing the ceramic foil. In contrast to other processes, in which the ceramic slip is produced from a mix of ceramic particles, an organic solvent and a high concentration of plastic binder, in our process, the slip is made up of ceramic particles lightly coated with plastic binder and suspended in water. The slip, therefore, has a much lower binder content than that of most of our competitors. So on drying out, the 'green' ceramic, as it's called, has initially a high porosity, allowing rapid drying of the silver-palladium electrode layer after screen printing. This, in turn, allows screen printing and stacking to be performed at a single station, giving far greater accuracy of electrode alignment. What's more, the high porosity of the ceramic foil gives greater adhesion between the ceramic and the silver-palladium layer, and so significantly reduces the risk of delamination.

After screen printing and stacking, the multilayer sheets are compacted (at a pressure of around 3000 kg/cm^2) to remove air trapped between the layers and to increase their 'green' density. Although this reduces the porosity considerably, its initial high value means that after compacting, the porosity is still higher than it would be with ceramic produced by conventional processes. This ensures that the next stage: binder burn-out, can take place with a far lower risk of voids appearing in the ceramic; and this risk in further reduced thanks to the very low binder content.

Another possible source of voids, dust falling on the green ceramic, is virtually eliminated by confining all production stages before firing to a production area with an advanced air-conditioning system that keeps dust levels below 10 000 particles*/ft^3 in the ceramic-casting, screen-printing and termination-dipping areas, and below 100 particles*/ft^3 in the screen fabrication area.

To further reduce the risk of delamination, the silver-palladium used for the electrodes is impregnated with ceramic. This minimizes mechanical stresses during sintering by reducing the shrinkage of the electrodes so that it more closely matches that of the dielectric.

* dust particles larger than 5 μm.

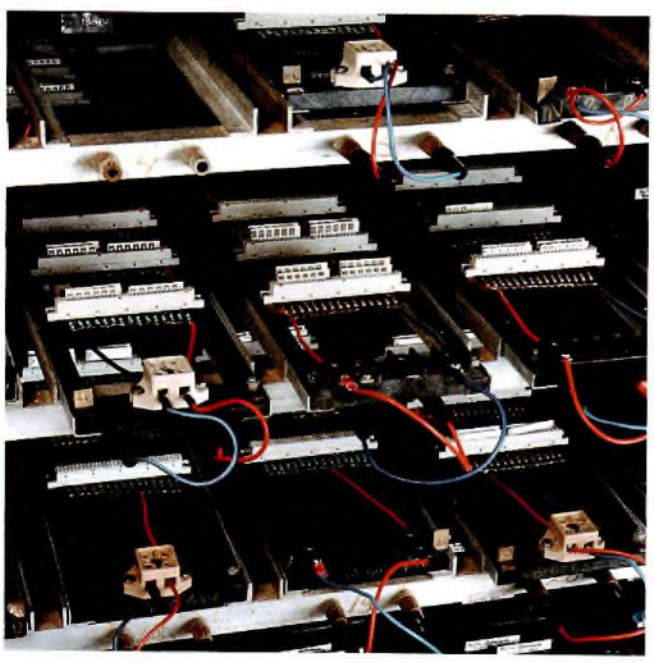


Fig.6 Capacitors undergoing the loaded humidity test

PROVEN INTEGRITY

Our component testing procedure eminently demonstrates the effectiveness of our manufacturing process.

Since low-voltage breakdown is the result of shortcomings in the manufacturing process, it's necessarily batch related. Many of the tests in our batch-release procedure are therefore directed specifically towards triggering low-voltage breakdown in our capacitors. Most notable of these is the loaded humidity test during which we attempt to induce breakdown by subjecting the capacitors to low voltage under extremes of temperatures and humidity. We also limit the maximum current through the capacitors to prevent the current from 'healing' potential breakdown spots by melting away any metallic bridges induced by electromigration.

Results of testing for early failures

quantity tested	period of test	component-hours of test	test parameters				catastrophic failures
			voltage (V)	temp. (°C)	relative humidity (%)	series resistance (Ω)	
5000	1000 hr.	5×10^6	5	125	–	150	0
5000	56 days	$6{,}7 \times 10^6$	1	40	95	1 M	0
384	56 days	$0{,}52 \times 10^6$	1,5	85	85	1 M	0
* 75	56 days	$0{,}1 \times 10^6$	63	85	85	1 M	0
* 46	56 days	$0{,}06 \times 10^6$	50	85	85	6,8 k	0

definition of catastrophic failure:
$\Delta C/C > 1{,}5$ x specified value
$\tan \delta > 1{,}5$ x specified value
$R_{ins} < 0{,}1$ x specified value.

* development group experimental tests.

The table gives the latest results of our loaded humidity tests. By the end of 1985 we had completed more than 12 million component-hours of testing *without a single catastrophic failure.*

As a further check on our manufacturing process, we perform what's known as destructive physical analysis (DPA) of selected capacitors in which we take a section through the ceramic and examine it microscopically (40x to 1500x magnification) for cracks, voids and delaminations, as well as for poor screen printing, misaligned layers and bent electrodes. With this test, even minor faults in the production process show up (Fig.7) and can be quickly traced and corrected.

LONG-TERM RELIABILITY

Since the lifetime of ceramic-multilayer capacitors can be reckoned in hundreds of years, it's obviously impractical to search for long-term failures using standard life tests. Instead, we've conducted extensive accelerated-life testing of our capacitors at temperatures up to 500 °C to determine how their most common long-term failure mechanism: dielectric degradation, is likely to affect their lifetime.

The equipment shown in Fig.8 has been specially developed to measure leakage currents of ceramic multilayer capacitors at temperatures up to 500 °C, and at test voltages

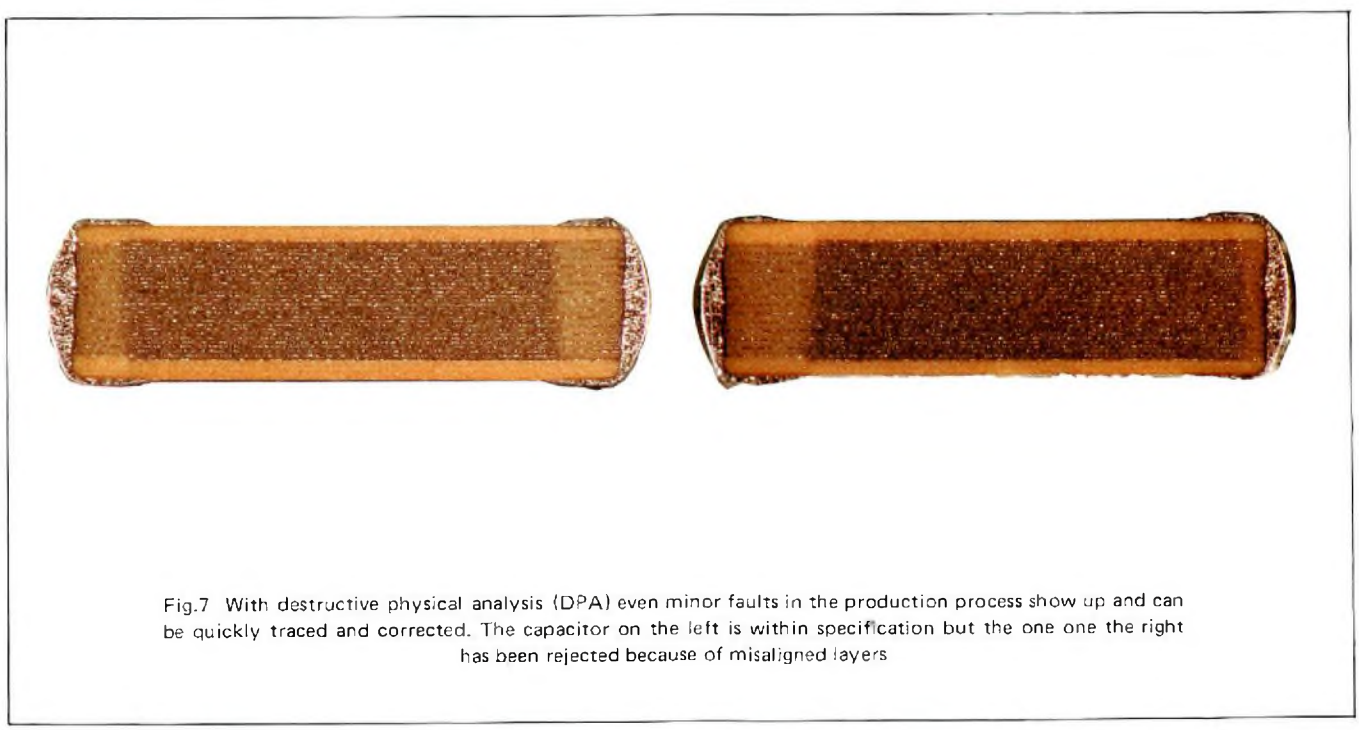


Fig.7 With destructive physical analysis (DPA) even minor faults in the production process show up and can be quickly traced and corrected. The capacitor on the left is within specification but the one one the right has been rejected because of misaligned layers

up to 2 kV. Figure 9 shows results of tests using this equipment. The figure plots insulation resistance against time for a typical test batch and clearly demonstrates that dielectric degradation is indeed a material-related phenomenon.

Figure 10 shows typical plots of insulation resistance against time, in this case at applied voltages between 25 V and 200 V, and at a test temperature of 200 °C. The figure clearly shows that at 200 °C, dielectric degradation of the ceramic can begin within around 10 hours.

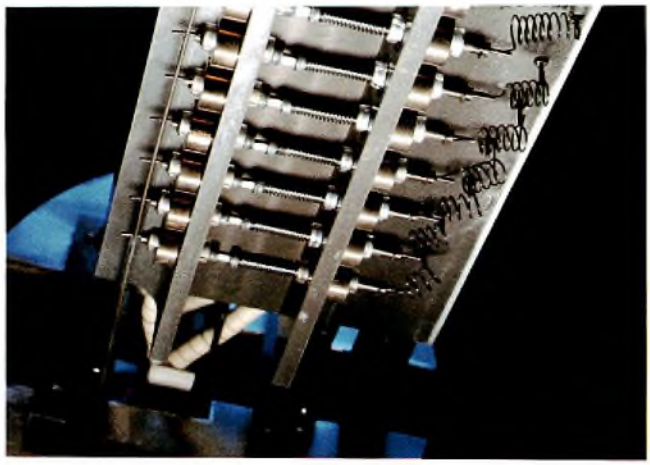


Fig.8 Specially designed furnace insert that holds up to 16 capacitors to allow their insulation resistance to be measured at temperatures up to 500 °C and at test voltages up to 2 kV

From curves such as these we can determine the mean lifetime τ, arbitrarily defined as the time at which insulation resistance has fallen to 10% of its maximum value. (Note: this failure criterion is much more stringent than that used

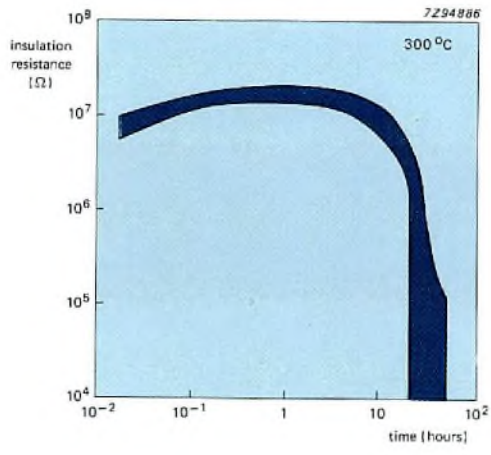


Fig.9 Plot of insulation resistance against time for Z5U ceramic-multilayer capacitors at 300 °C, 5 V. For all capacitors tested the trend (allowing for individual spread) is quite clear (a slight increase in insulation resistance followed by a rapid drop), and clearly demonstrates that dielectric degradation is a material-related phenomenon

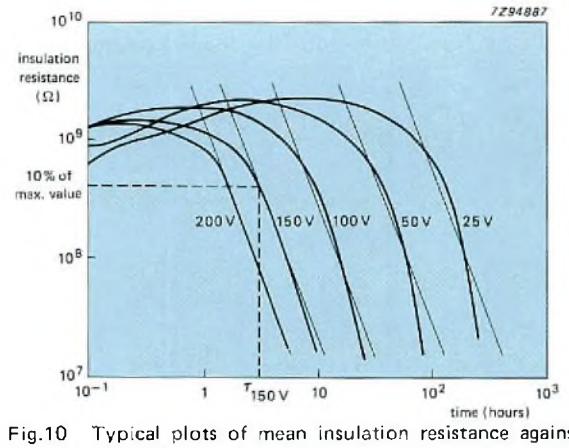


Fig.10 Typical plots of mean insulation resistance against time for 16 Z5U ceramic-multilayer capacitors measured at applied voltages between 25 V and 200 V, and at a test temperature of 200 °C

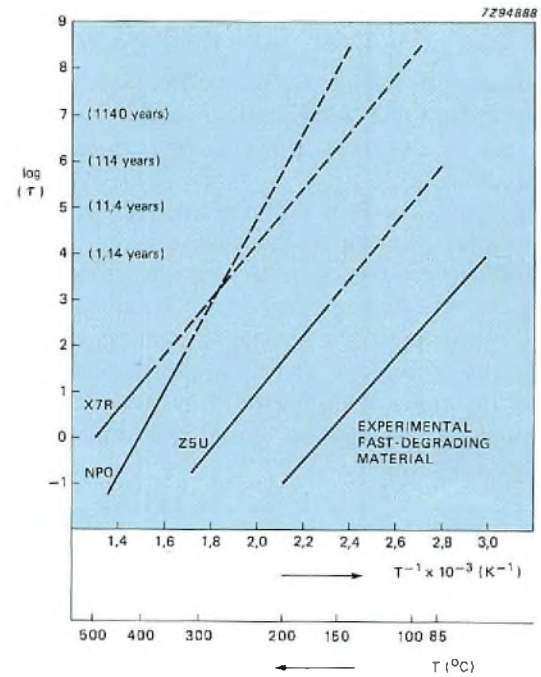


Fig.11 Extrapolated Arrhenius plots with 50 V applied to various ceramic materials. The line on the far right is the measured behaviour of an experimental fast-degrading material and demonstrates the validity of extrapolating the other plots as straight lines

in standard life tests according to IEC regulations which just count the number of capacitors failing to meet specification.) Arrhenius plots of log (τ) against reciprocal temperature (1/T) can then be made. As Fig.11 shows, such plots are substantially linear, allowing extrapolation of capacitor lifetimes for normal operating temperatures.

From Arrhenius plots like these, we've predicted lifetimes for our ceramic multilayer capacitors extending into hundreds and even thousands of years. For example, capacitors produced from our X7R material under an applied voltage of 50 V have a predicted lifetime at 125 °C of over *1000 years.*

Stereo sound generator for sound effects and music synthesis

MIKE ROBERTS

All the sophisticated application software in the world can't compensate for a home computer that communicates with its user in an unattractive or confusing way. To enhance present levels of visual and audio communication from computer to user, a stereo sound generator, SAA1099, and a 64-colour encoder, TEA2000 (Ref.1), have been developed, each giving software and hardware designers the scope to add more realism to their products.

The sound generator SAA1099 is described in this article. It can produce a wide variety of sound effects including simulations of musical instruments, and the sounds required for arcade/home-computer games. Whereas most integrated sound generators have only three frequency generators, the SAA1099 has six, and the tones from each can be mixed with several kinds of noise. Because there are six frequency generators, full musical chords (including the tonic) can be produced, and two chords (excluding tonics) can overlap. All musical notes in an 8-octave range can be produced. A stereo effect that can give width to scenes in video games is produced by duplicating the six sound components to form identical left and right-channel signals, weighting the signals of each channel, and combining them to form a stereo signal.

Besides the stereo sound facility, effects such as Doppler shifts can be imitated with a minimum of software control. Outside the home computer market, the SAA1099 can be used to good effect in model railways and cars, electronic musical instruments and audible alarms, to name just a few applications.

The SAA1099 readily interfaces with most 8-bit microcontrollers and requires only a simple filter to suppress any high-frequency components in the audio output. It has been designed in such a way that a minimum of external components are required. Table 1 gives additional data on the SAA1099; see also Refs 2 and 3.

TABLE 1
Brief data on the SAA1099 (all values are typical)

supply voltage	V_{DD}	5 V
supply current	I_{DD}	70 mA
reference current (pin 6)	I_{ref}	250 μA
total power dissipation	P_{tot}	500 mW
external clock		8 MHz
data input		8-bit parallel (TTL-compatible)
output frequency range		31 Hz to 7,81 kHz (8 octaves)
output		pulse width modulated
operating ambient temperature range	T_{amb}	0 to +70 °C
package		18-pin plastic DIL

COMPLETE SOUND GENERATOR

Figure 1 shows a complete sound generating system. From an 8-bit wide data input from a microprocessor, the SAA1099 generates a variable-amplitude stereo analog signal chopped at a rate of 62,5 kHz. A simple external low-pass filter suppresses the high frequency components of the output signal. The incoming data which shapes the spectrum of the audio output is multiplexed to simplify interfacing, the signal A0 being used to indicate whether the data is a register address, or data for the register. The A0 signal is used with the $\overline{CS}$ and $\overline{WR}$ signals to control the data transfers from the microprocessor to the SAA1099. These control signals are compatible with a wide range of microprocessors. In addition, for optimum interfacing with an SCN68000 series microprocessor, the SAA1099 has a $\overline{DTACK}$ output. All internal timing is derived from an external 8 MHz clock.

TABLE 2
Function of the A0 input

A0	data bus input								function
	D7	D6	D5	D4	D3	D2	D1	D0	
0	D7	D6	D5	D4	D3	D2	D1	D0	data for internal registers, see Table 3
1	X	X	X	X	A3	A2	A1	A0	internal register address, A3 is the MSB

X = don't care

Table 2 shows the function of the A0 input. When A0 = 1, the bus data indicates the address of the control register in the SAA1099 to be written and this address is loaded into the command register. The next data byte on the bus, which contains the control information for the register that has been addressed, is written to the register when A0 = 0. Once addressed, a control register can be updated without further addressing.

CIRCUIT DESCRIPTION

Frequency generators

The SAA1099, see Fig.2, has six frequency generators each of which can generate 256 tones in each of eight octaves from 31 Hz to 7,81 kHz. Each generator can be switched on and off individually, making it possible to preselect a tone and to make it audible when required. To simplify the software, the frequency generators can be synchronized at start-up and when changing frequencies, octaves and envelopes using the frequency reset bit, see 'Synchronization'. The outputs of frequency generators 0 and 3 can each control a noise generator while those of generators 1 and 4 can each control an envelope generator for creating special effects.

Table 3 gives the addresses and the bit allocation of the SAA1099's internal registers used to control the frequency generators and its other sound-generating circuitry.

Noise generators

Two noise generators each have a programmable output controlled by the contents of register 16 which determines whether the output is:

- software-controlled via frequency generator 0 or 3 (which then produces no tone). The 'colour' of the noise generated is derived from twice the frequency of the frequency generator output, i.e. from 61 Hz to 15,6 kHz.

- one of three pre-defined noises based on clock frequencies of 7,8 kHz, 15,6 kHz or 31,25 kHz. In this case, the output of noise generator 0 can be mixed with the outputs of frequency generators 0, 1 and 2, and the output of noise generator 1 can be mixed with the outputs of frequency generators 3, 4 and 5, see Fig.2. For mixing, the amplitude of the tone is increased relative to that of the noise.

Noise/frequency mixers

The SAA1099 has six mixers, one per frequency generator, for mixing tones with noise. Dependent on the status of bits D0 to D5 of registers 14 and 15, each mixer can be set:
- to mix the noise and the tone
- to pass the tone only
- to pass the noise only
- to pass neither tone nor noise.

Amplitude controllers

The SAA1099 has six amplitude controllers used, for example, to create a stereo effect. Each controller duplicates the signal from one of the noise/frequency mixers to form left and right-channel components and assigns one of sixteen amplitudes set by the contents of the control registers 00 to 05 to each component. A stereo effect can be produced simply by varying the amplitude of each component. To move a sound from one channel to another requires, per tone, only one update of the contents of the appropriate amplitude register.

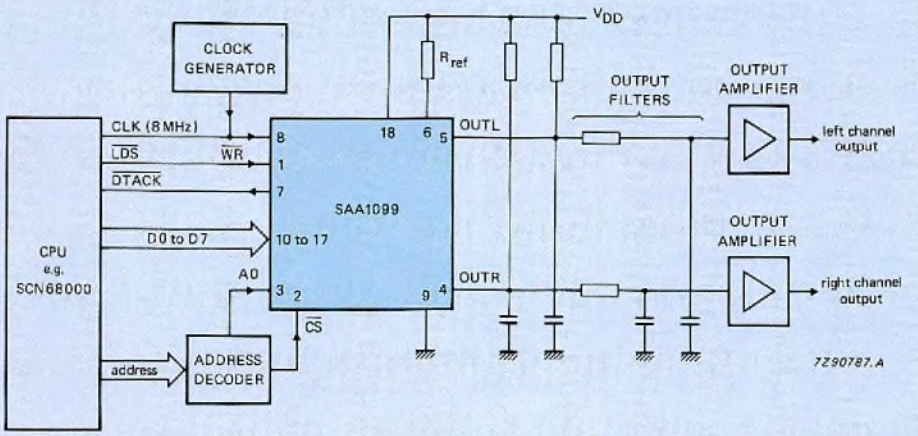


Fig.1 Sound generation system for home computers and video games equipment.

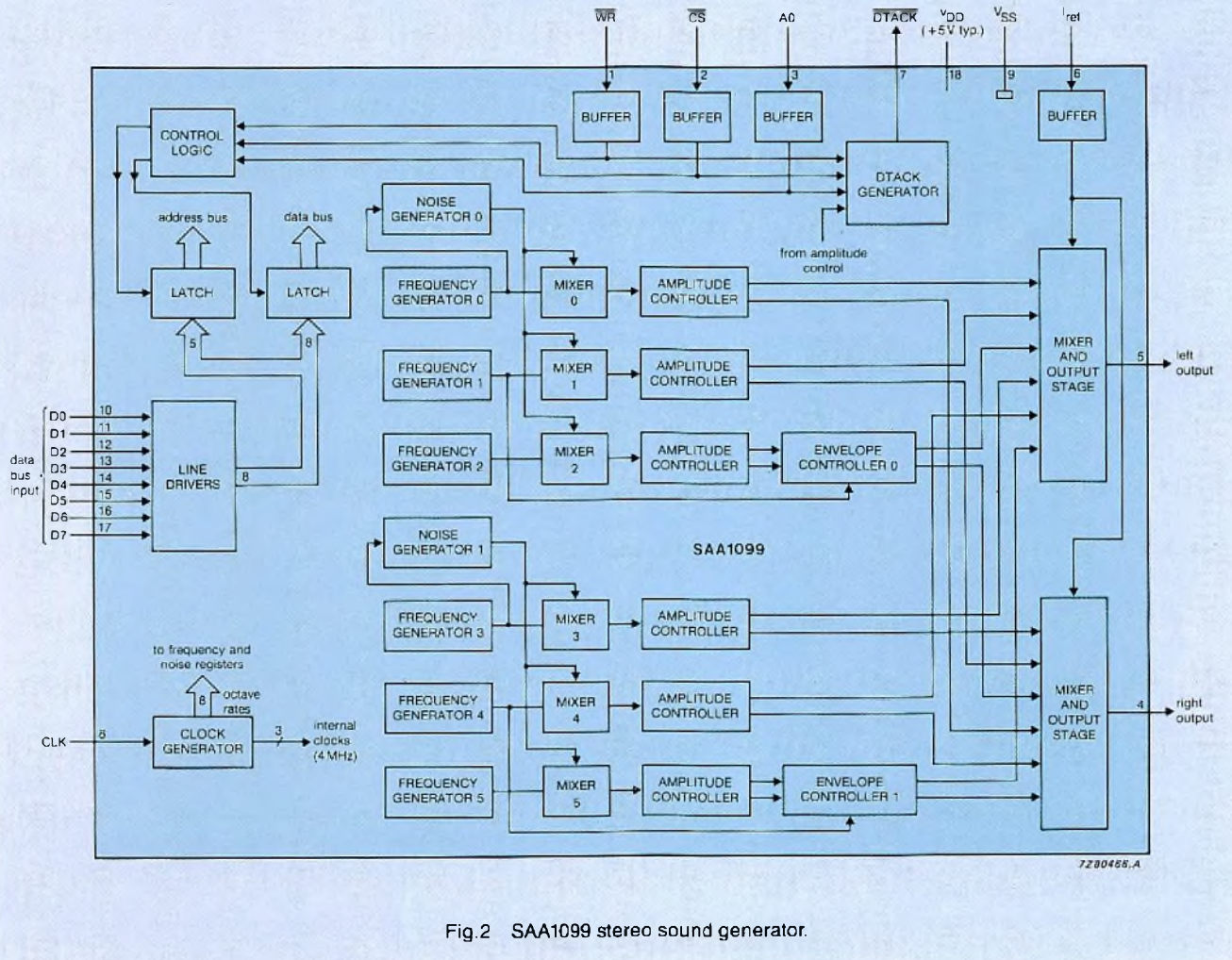


Fig.2 SAA1099 stereo sound generator.

TABLE 3
Bit allocation of the internal registers of the SAA1099; A0 = 1

register address	data bus input D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	description/remarks
00	amp. right channel				amp. left channel				controller 0
01	amp. right channel				amp. left channel				controller 1
02	amp. right channel				amp. left channel				controller 2
03	amp. right channel				amp. left channel				controller 3
04	amp. right channel				amp. left channel				controller 4
05	amp. right channel				amp. left channel				controller 5
06	X	X	X	X	X	X	X	X	reserved for possible expansion
07	X	X	X	X	X	X	X	X	reserved for possible expansion
08	tone number for frequency generator 0								frequency of tone (Hz) = $\frac{15625 \times 2^{\text{octave number}}}{(511 - \text{tone number})}$, see notes
09	tone number for frequency generator 1								
0A	tone number for frequency generator 2								
0B	tone number for frequency generator 3								
0C	tone number for frequency generator 4								
0D	tone number for frequency generator 5								
0E	X	X	X	X	X	X	X	X	reserved for possible expansion
0F	X	X	X	X	X	X	X	X	reserved for possible expansion
10	X	octave no. of freq. gen. 1			X	octave no. of freq. gen. 0			octave 0 (0 0 0): 31 Hz to 61 Hz; octave 1 (0 0 1): 61 Hz to 122 Hz octave 2 (0 1 0): 122 Hz to 244 Hz; octave 3 (0 1 1): 245 Hz to 488 Hz octave 4 (1 0 0): 489 Hz to 977 Hz; octave 5 (1 0 1): 978 Hz to 1,95 kHz octave 6 (1 1 0): 1,96 kHz to 3,91 kHz; octave 7 (1 1 1): 3,91 kHz to 7,81 kHz
11	X	octave no. of freq. gen. 3			X	octave no. of freq. gen. 2			
12	X	octave no. of freq. gen. 5			X	octave no. of freq. gen. 4			
13	X	X	X	X	X	X	X	X	reserved for possible expansion
14	X	X	5	4	3	2	1	0	frequency enable (active-HIGH); 0 to 5 refer to the noise/frequency mixers
15	X	X	5	4	3	2	1	0	noise enable (active-HIGH); 0 to 5 refer to the noise/frequency mixers
16	X	X	generator 1		X	X	generator 0		noise generator clock frequency:
			0	0			0	0	31,25 kHz
			0	1			0	1	15,6 kHz
			1	0			1	0	7,8 kHz
			1	1			1	1	61 Hz to 15,6 kHz (freq. generator 0 or 3 controlling noise generator 0 or 1 respectively)
17	X	X	X	X	X	X	X	X	
18	envelope generator 0								see Table 4 and Fig. 3
19	envelope generator 1								see Table 4 and Fig. 3
1A	X	X	X	X	X	X	X	X	
1B	X	X	X	X	X	X	X	X	
1C	X	X	X	X	X	X	RST	SE	RST: reset for all freq. generators (active-HIGH); SE: sound enable for all channels (active-HIGH), see notes
1D	X	X	X	X	X	X	X	X	
1E	X	X	X	X	X	X	X	X	
1F	X	X	X	X	X	X	X	X	
	D7	D6	D5	D4	D3	D2	D1	D0	

This block of 32 registers is repeated eight times between addresses 00 and FF in the full internal memory map. All don't cares (X) should be written as zeroes.

Tone numbers of 1 to 256 are valid.

At power-on, the sound enable bit is set to 0 (all channels disabled). When the frequency reset bit is set, all frequency generators are reset and synchronized.

Envelope controllers

Two envelope controllers enable the left and the right components of two stereo channels to be modified for:

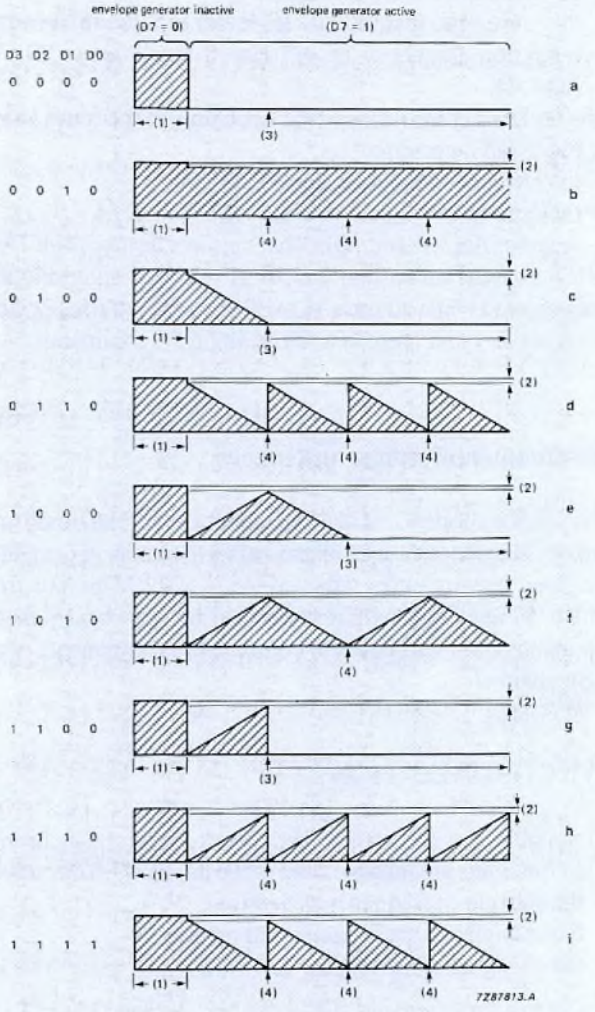
- single attack
- single decay
- single attack and decay (triangular)
- maximum amplitude
- repetitive attack
- repetitive decay
- repetitive attack and decay (triangular)
- zero amplitude.

Figure 3 shows the envelopes which are selected by bits D1 to D3 of the envelope registers 18 and 19, see Table 4. The repetition frequency of the envelopes can be software-controlled by writing to the envelope address register (the data written is irrelevant), or clocked internally at the output frequency of the frequency generator (1 or 4). An envelope will always be completed before a new envelope instruction is implemented. In the case of repetitive envelopes, the envelope returns to its starting level which may not necessarily be zero.

When the envelope facilities are used, and the maximum amplitude set by the contents of registers 00 to 05 is chosen, the amplitude is 7/8ths that normally available.

TABLE 4
Bit allocation of the envelope generator registers (addr. 18 and 19)

bit	function
D0	
0	identical envelopes for the left and right channel components
1	inverse envelopes for the left and right channel components
D3 D2 D1	
0 0 0	zero amplitude
0 0 1	maximum amplitude
0 1 0	single decay
0 1 1	repetitive decay
1 0 0	single triangular
1 0 1	repetitive triangular
1 1 0	single attack
1 1 1	repetitive attack
D4	
0	4-bit envelope resolution
1	3-bit envelope resolution
D5	
0	internal envelope clock (frequency generator 1 or 4)
1	external envelope clock (address write pulse A0)
D6	don't care
D7	
0	reset (no envelope control)
1	envelope control enabled



Notes:
(1) normal amplitude control; envelope generator inactive.
(2) when the envelope generator is active, the maximum amplitude is 7/8ths of the maximum set by registers 00 to 05.
(3) after position (3), a new envelope will be implemented as soon as the new buffered controls are received.
(4) when an envelope is interrupted, the new envelope starts at the positions indicated (4).

Fig.3 Envelope waveforms. (a) to (h) the waveforms of one channel, the left say, of an envelope generator; (a) zero amplitude, (b) maximum amplitude, (c) single decay, (d) repetitive decay, (e) single attack and decay, (f) repetitive attack and decay, (g) single attack, (h) repetitive attack, (i), as (h), but for the right channel showing the operation of the inverse envelope bit D0, see also Table 4.

Two types of envelope control are stored in the envelope registers – direct-acting controls and buffered controls. The direct-acting controls always take immediate effect and are:
- the envelope enable/reset (bit D7)
- the envelope resolution: 16 levels up to an envelope repetition frequency of 977 Hz, 8 levels above 977 Hz (bit D4).

The buffered controls are acted upon only at the times shown in Fig.3 and determine:
- the envelope waveform (bits D1 to D3)
- the type of envelope clock (bit D5)
- whether the left and right channels are inverted (bit D0).

When an external envelope clock is selected, an envelope is only created when address 18 or 19 is written to (that is when A0 is set to 1 and there is a 'write 18 or 19' command).

Six-channel mixers/output stages

The six components of the left channel are combined in a mixer. The output stage of the mixer contains six equally-weighted current sinks which provide a PWM output from which an analogue output is derived by low-pass filtering. An identical mixer is used to combine the components of the right channel.

SYNCHRONIZATION

To simplify the software writer's work, several synchronization functions are incorporated in the SAA1099. They affect:
- the starting of frequency generators
- the changing of frequencies and octaves
- the changing of envelopes.

Synchronizing frequency changes

The internal architecture of the SAA1099 is such that when a new tone in an octave different from that currently selected is required, the frequency register should be written to before the octave register. Failure to write to the registers in this order with the sound enabled, may produce a click in the audio output. The frequency and octave registers can, however, be written to at any time, but data can only be acted upon by the SAA1099 on a transition of the associated frequency generator, that is, data won't be acted upon until half the period of the current frequency has elapsed. This means that:

- when the frequency and octave registers are set for the lowest frequency of 31 Hz, the new frequency data or octave data may not be acted upon for up to about 17 ms (half a period). Therefore, to ensure this interval has elapsed, a delay corresponding to half a period of the existing tone should be written in the software between writing the new frequency or octave and enabling the output.
- at the higher end of the spectrum, if it is required to change the frequency and octave registers simultaneously, both new values must be written (frequency first, octave second) within half the period of the current frequency (i.e. within 64 μs for a 7,74 kHz tone).

Synchronization on reset

All frequency generators can be reset by setting bit D1 (RST) of the register at address 1C. In this state, frequency and octave data can still be written to the SAA1099, but will not be acted upon. Therefore, as long as RST is active, a register value can be overwritten with new data. However, any new data in the register will not be acted on until half the period of the frequency whose value is held in the register when RST was set has elapsed. This is because RST not only sets all generators to a known state, it synchronizes their start-up.

APPLICATIONS

Probably the most obvious application for the SAA1099 is in video games where the wide range of sound effects available can be used to make games more appealing. The stereo effect, for example, can be used to give width to scenes and to create the impression of movement of objects in the scene. More interesting is the possibility of relating both channel amplitudes and Doppler shift in frequency to the position of an object relative to the user. For example, the sound of passing vehicles or swooping spaceships can be realistically produced.

Many of the sounds in computer games are based on 'coloured' noise (e.g. aircraft, gunfire and car engines). The two noise generators of the SAA1099 with full software control of the noise colour, and the ability to mix the noise with tones, enable two separate 'coloured' noises to be produced in stereo for increased realism.

As mentioned earlier, the SAA1099 can produce all musical notes across eight octaves from 31 Hz to 7,81 kHz. The availability of six frequency generators enables full musical chords (including the tonic) to be produced and allows two chords (excluding tonics) to overlap.

The advanced envelope generation facilities and software control of amplitude and frequency enable musical instruments to be mimicked including vibrato and tremolo effects.

Software modules that generate specific sounds can be created, e.g. piano and trumpet, as well as modules that generate sounds that can be altered to suit the situation in a video game, e.g. laser gun, sirens and error warnings.

The following sections outline how several sound effects can be produced. Programming details aren't given (these are published in Ref.3), but some salient points and data are.

Notes and chords

A scale of middle C to high C can be produced using just one frequency generator set for maximum amplitude on both outputs, with the signal from the appropriate noise generator disabled. Table 5 shows the tone numbers and octave numbers required. Note that the same note in different octaves has the same tone number, e.g. C is tone H21 in octave 3 and octave 4. With an 8 MHz crystal-derived clock, all the notes are produced to an accuracy better than 0,1%.

Chords, for example C major and A minor, can be produced using all six generators by writing the appropriate values to the tone and octave registers, then enabling the notes in sequence, without disabling those already active.

Musical arrangements are produced in a similar fashion by an appropriate combination of writing/enabling of tone and octave registers. A stereo effect is producing by giving the treble clef predominance on one channel and the bass clef predominance on the other.

TABLE 5
Chromatic scale

note	tone number (hex)	octave number	required frequency (Hz)	actual frequency* (Hz)
middle C	21	03	261,626	261,506
C #	3C		277,183	277,162
D	55		293,665	293,427
D #	6D		311,127	310,945
E	84		329,628	329,815
F	99		349,228	349,162
F #	AD		369,994	369,822
G	C0		391,995	391,850
G #	D2		415,305	415,282
A	E3		440,000	440,141
A #	F3		466,164	466,418
B	05	04	493,883	494,071
C	21		523,251	523,013

* with an 8 MHz crystal-derived clock

Siren

The sound of a siren can be simulated using only one frequency generator. All possible values (from high to low) are written to a tone register, changing the octave where necessary, and repeated. A repetitive triangular envelope with the left channel set to be the inverse of that of the right gives the impression of side-to-side movement. When the envelope generator is externally clocked at 85 clocks/second using the address write pulse A0, the sound repeats every 2,7 s.

Aircraft

A dogfight between two aircraft can be simulated using both envelope controllers. One envelope should be set for repetitive attack to simulate gunfire, the other set for repetitive decay to simulate the noise of a propeller. These can be combined with two different types of noise and can be internally clocked. Writing different values to the amplitude registers to vary the volume in the two outputs creates the impression of movement.

A combination of noise and tone can be used to simulate a jet plane preparing for take-off. The colour of the noise should be held constant while the frequency of the tone should be increased smoothly by successive writing to the frequency register. A sawtooth envelope with the invert bit set suggests taxiing movement. If the envelope is clocked to its maximum value on the left output before the sound is enabled, then not clocked during tone changes, the right channel will not be heard, and the plane will appear to be located on the left of the scene.

To give an impression of movement from left to right, the envelope should be clocked eight times when the tone reaches some desired amplitude, reducing the level on the left and increasing that on the right. The left output can then be disabled and the envelope clocked another eight times to reduce the level on the right to zero, giving the impression of movement to the right.

Gun, cannon-fire and laser guns

The sound of a machine gun can be produced using an internally-clocked sawtooth envelope to shape continuous coloured noise. Another gun can be simulated using noise of a different colour and a repetitive decay envelope. Lulls in firing are produced by enabling and disabling the sound enable bit.

The sound of a cannon can be simulated in the same way as the first machine gun just described with the envelope clocked externally and much more slowly. The direction and distance of the cannon is determined by the contents of the amplitude register.

A space gun or 'laser sound' can be produced using a 500 Hz tone (tone H0F in octave 4) and a sawtooth envelope with external envelope clock.

Space-ships

To suggest two swooping space-ships, two identical envelopes clocked at different rates and each with the invert bit set are used with two tones whose frequencies are varied between preset points at different rates.

Steam locomotive

To simulate the sound of a steam locomotive, coloured noise (15,6 kHz clock) and a repetitive triangular envelope are used. With the sound disabled, the envelope is clocked through to its peak, then with the sound enabled clocked slowly to its trough to give the sound of a gentle hiss of steam. After a pause, the envelope should be clocked continuously (beginning for example at 3,5 clocks per second and increasing to 28 clocks per second to suggest a locomotive gathering speed.

The sound of a locomotive's whistle can be produced using a 480 Hz tone (tone HFF in octave 3) mixed with noise.

Telephone ringer

The sound of a telephone ringer such as that fitted to a Trimphone® is simulated using an internally-clocked saw-tooth envelope mixed with an appropriate tone (3,3 kHz, tone H6F in octave 6). The cadence is produced by enabling and disabling the sound (0,46 s enabled, 0,23 s disabled, 0,46 s enabled and 2,3 s disabled).

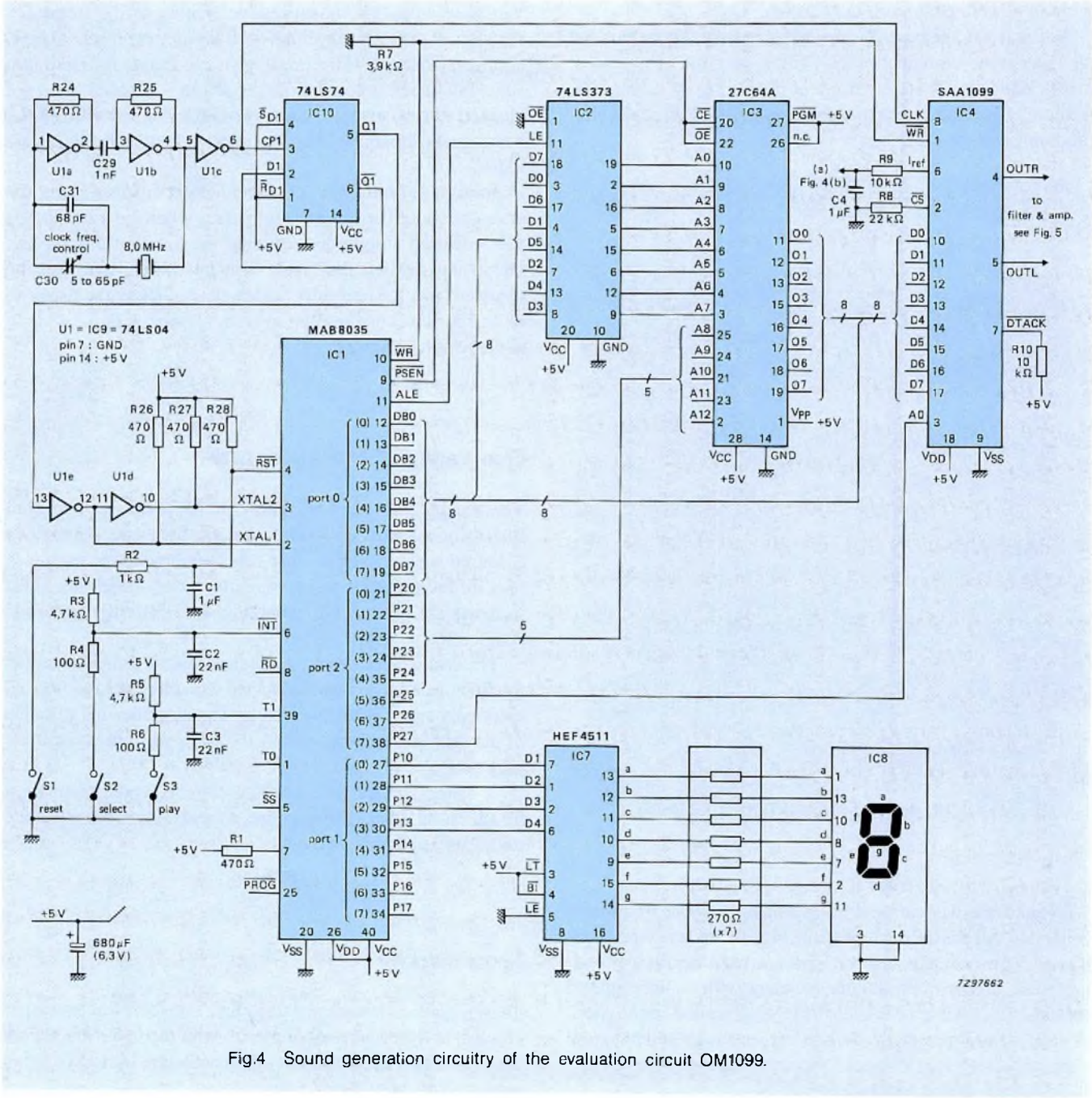


Fig.4 Sound generation circuitry of the evaluation circuit OM1099.

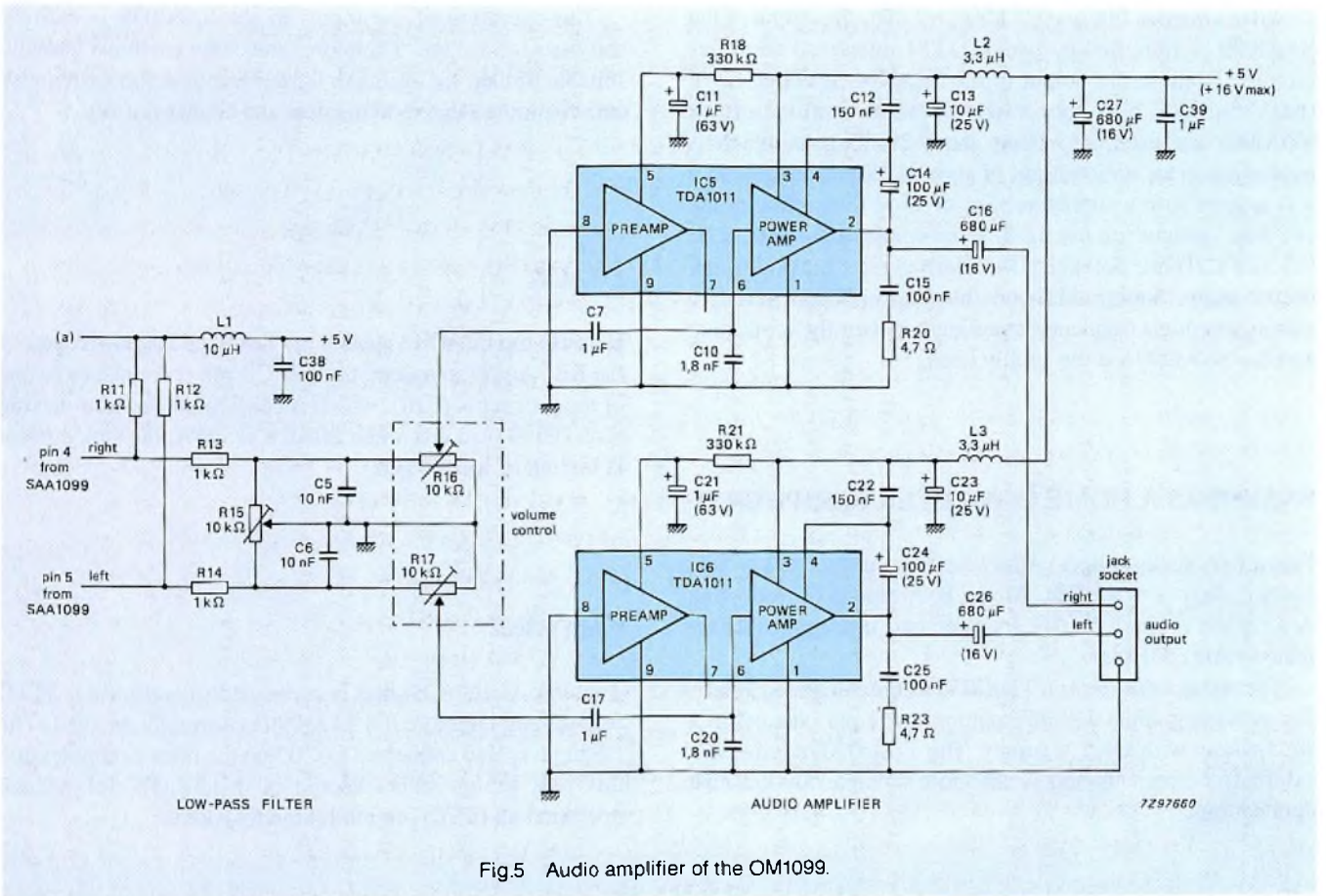


Fig.5 Audio amplifier of the OM1099.

EVALUATION CIRCUIT

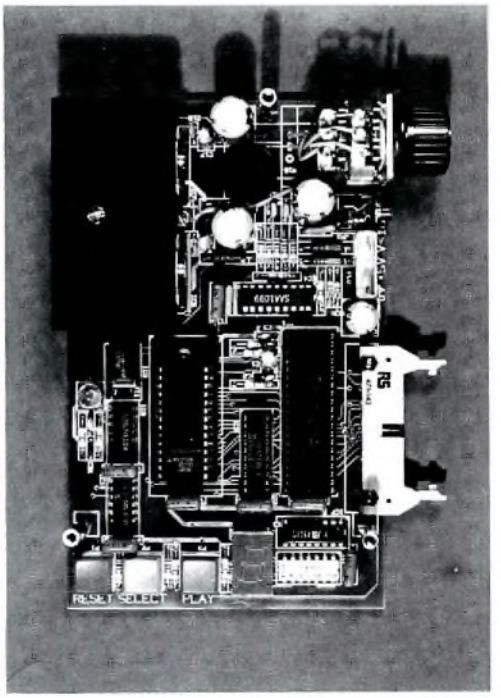
Figure 4 shows a circuit that is available for you to evaluate the SAA1099 in your application. The circuit which includes an integrated stereo power amplifier can be ordered using part number OM1099. A description of the circuit's hardware and software appears in Refs 4 and 5 respectively.

Data bytes held in an EPROM (the MAB8035HL microprocessor has no on-chip ROM) are sent via the microprocessor to the data inputs of the SAA1099 together with the A0 and $\overline{WR}$ signals.

Pre-programmed sound modules can be selected using the 'select program' key which interrupts the current sound module being played. A display indicates the program selected. The 'play' key is used to play the selected program. Software support is available on request. For timing details, the reader is referred to the SAA1099 data sheet (Ref.2).

The standard MAB8035 requires a clock in the range 1 to 6 MHz. It is convenient to use the 8 MHz crystal oscillator for the SAA1099 with a divider to provide a 4 MHz clock for the microprocessor.

Since the SAA1099 can always accept data faster than the rate at which the MAB8035 can produce it in the circuit of Fig.4, the $\overline{DTACK}$ output has not been used. However, when a faster processor such as the SCN68000 is used, $\overline{DTACK}$ must be used to prevent data being missed by the SAA1099.



Laboratory model of the sound generation circuit shown in Fig.4.

After low-pass filtering (17 kHz, −3 dB), the output of the SAA1099 is amplified by two TDA1011 integrated amplifier circuits. Because the output of the SAA1099 is about 1,3 V (peak-to-peak), only the power amplifier sections of the TDA1011s are used, providing about 23 dB gain which is equivalent to an audio output of about 6 W per channel in a 4 Ω system with a supply voltage of 16 V. Even though the pre-amp sections are not used, some components (R18, R21, C11 and C21) are necessary to ensure correct biasing of the output stage. Some additional filtering has been added to reduce any high frequency coupling between the amplifiers and the SAA1099 via the supply lines.

SAA1099 AS A HOME COMPUTER PERIPHERAL

Figure 6 shows how the SAA1099 can be connected to a typical home computer – the BBC Model B. Although the following description is based on this arrangement, it is applicable for many home computers.

The audio amplifier is a TDA7050 stereo integrated amplifier providing about 140 mW output power per channel in a 16 Ω system with a 4,5 V supply. The TDA7050 requires few external components and is therefore suitable for low-cost applications.

The operation of the inputs to the SAA1099 is entirely software-controlled. Therefore, the software must provide suitable timing, for example, for the length of the write pulse and its timing relative to the data and changes of A0.

$\overline{\text{DTACK}}$

Because the $\overline{\text{DTACK}}$ signal is too fast to be acknowledged by the BBC home computer, the $\overline{\text{DTACK}}$ pin is connected to one of the user ports (CB1), which is configured in a non-driving state (HIGH) so that when $\overline{\text{DTACK}}$ is LOW, the sink current is limited to about 3 mA.

Chip select

The chip select ($\overline{\text{CS}}$) line is connected to earth via a 22 kΩ resistor and therefore the SAA1099 is normally enabled. The $\overline{\text{CS}}$ input is also connected to CB2 on the microcomputer and this port or equivalent should be held LOW for normal operation and HIGH to inhibit the SAA1099.

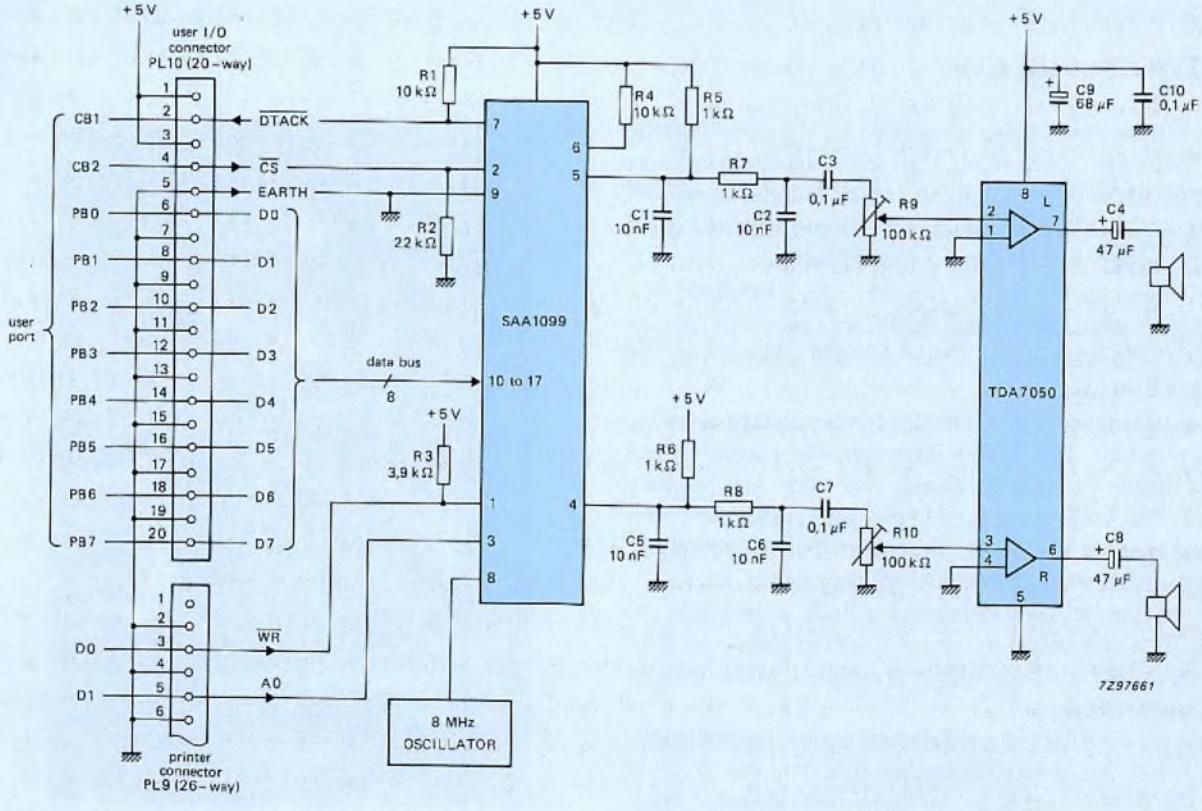


Fig.6 SAA1099 connected to a BBC Model B home computer.

Linear section

The performance of the audio amplier section of Fig.6 is poorer than that of Fig.4, but the circuit is cheaper. An integrated stereo amplifier circuit TDA7050 provides a voltage gain of 26 dB per channel, corresponding to about 50 mW per channel output power with 50 Ω loudspeakers. The low-frequency response of the amplifier (70 Hz, −3 dB point with 50 Ω loudspeakers) is mainly determined by the value of the coupling capacitor C4 or C8 (47 μF).

Before amplification, each signal is filtered to suppress the high-frequency content of the signal (62,5 kHz and above) due to the amplitude and envelope control of the SAA1099. The filter network produces a 3 dB attenuation at 17 kHz. If small speakers are used, their lack of low-frequency response emphasizes the higher harmonics in the SAA1099 output, producing a rather harsh sound which can be removed by additional high-frequency attenuation of the audio signal.

REFERENCES

1. TEA2000, PAL/NTSC colour encoder, Philips Elcoma data sheet, ordering code 9397 085 70142, Sept. 1985.

2. SAA1099, Microprocessor controlled stereo sound generator for sound effects and music synthesis, Philips Elcoma data sheet, Data Handbook IC14, Microprocessors, microcontrollers and peripherals, 1985. Ordering code 9398 132 40011.

3. Sound generator with an added dimension, Mullard laboratory report MTH8503, 1985, Mullard Application Laboratory, Mitcham, England.

4. A demonstration board for the SAA1099 stereo sound processor, Mullard Laboratory report THM85102, 1985, Mullard Application Laboratory, Mitcham, England.

5. Control programs and sound modules for the SAA1099 stereo sound processor, Mullard laboratory report THM85104, 1985, Mullard Application Laboratory, Mitcham, England.

Harvard architecture pushes microcontroller IC into high-speed realm

GREG GOODHUE, JESSE JENKINS and ATA KHAN

Developing a fast microcontroller has never been easy. The most demanding applications: signal processing and communications and peripheral control, outpace the convenient single-chip MOS microcontroller, sending designers back to bipolar bit-slice devices and hand-written microcode. Easing the situation is a new bipolar microcontroller, the 8X401A, that increases designers' chances of success in meeting high-speed controller challenges.

To blend speed with programming simplicity, the new 8X401A microcontroller dispenses with the traditional von Neumann structure. Instead, its Harvard architecture helps squeeze the most from the chip's 100-ns instruction cycle. In fact, except when it handles interrupts, the processor spends only an exceptionally small portion of each cycle – 25% – on decoding an instruction. The remaining 75% is left to executing the operation.

The microcontroller and its 150-ns version, the 8X401, are just two of a growing family of ECL-based components equipped with TTL buffering (see "Technology Tale"). Other current members are the 8X470 programmable I/O port and the 8X450 RAM, a 2-kbit device having a 20-ns access time and organized as 256 by 8 bits. In the pipeline are a priority interrupt controller, a 32-byte RAM, and a 32-byte LIFO stack. Moreover, designers can also select from the earlier 8X300 and 8X305 microcontroller series. The older models perform subset functions of the new ones, and the peripherals include DMA and floppy-disk controllers and a dual-port register file.

Data instruction formats

Instruction	Field length (bits)				
	4	3	5	3	5
Move, Add, AND, XOR, Add with Carry	Op Code	Length	Source	Rotation	Destination
XMIT and Add Immediate (8 bits)	Op code	Length	Destination	Data	
XMIT and Add Immediate (5 bits)	Op Code	Length	Destination	Rotation	Data
AND and XOR Immediate (8 bits)	Op Code	Length	Source	Data	
AND and XOR Immediate (5 bits)	Op Code	Length	Source	Rotation	Data

Besides higher speed, the 8X401A microcontroller's biggest improvement over its predecessors is its ability to handle both interrupts and subroutines in their entirety, as well as four new instructions for jumps and returns and more arithmetic and logic operations. What's more, it has a powerful group of development tools – namely, a symbolic cross-assembler called Fortress and a prototype development board.

Unlike bipolar bit-slice devices, for which the user writes microcode, this microcontroller has its own set of 16 instructions. Grouped into data and address classes, they are designed to be easily understood by the user yet sufficiently flexible for any controller application.

SIMPLE INSTRUCTIONS

The 13 data instructions include Move, Add, ADC, AND, XOR, and XMIT (see the Table). The first five operate on data from the source specified in one of their fields and leave the results at the destination specified in another of their fields. Move transfers data; Add executes binary addition; ADC is like Add but includes the Carry flag; and AND and XOR are the respective logic operations.

XMIT, however, transmits immediate data (data contained in one of its fields) to the destination it specifies. Six variants of the Add, AND, and XOR instructions can also have an immediate data field. A three-bit field in the op code specifies the length of data in that field for one to eight bits. When the length is specified, the most significant position becomes the top bit in any operation. In other words, the Carry bit automatically corresponds to the length of the data specified. For example, a four-bit chunk of data will generate the Carry flag when the fourth bit overflows.

A rotation field within the data type of instruction rotates the source or the data field by a number of bit positions. (With other controllers, that's the job of a separate instruction, repeated once for every bit rotated.) The field causes bits to be shifted down toward the least significant position on entering the ALU; on leaving the ALU, the bits are then shifted back upward by the same number of positions. The field can also permit independent values for the number of upward and downward shift operations.

The address instructions can be grouped into conditional branches and returns, subroutine branches and returns, and the Execute instruction (XEC). The first group includes jumps and returns, both of which depend on four status bits, and an unconditional branch operation. In the second group, the subroutine return is conditional; it can set and clear the controller's Carry bit, pop the stack, and branch to some specified address (not necessarily the popped address).

Last, the XEC single-instruction branch imposes no stack-handling overhead. Instead it branches to the address stored in a register and then automatically returns the controller to the instruction following XEC. (An exception arises if the instruction branched to is itself a branch.)

In more detail, XEC performs an indirect branch to the address contained in the chip's B register. The instruction specifies up to eight bits, which are placed in the address register before branching. It then branches to that address. After the controller performs the operation indicated, XEC fills the address register with the location following the (XEC) instruction and resumes normal operation.

With this instruction a programmer can test various conditions simply by loading different pointers into the B register, doing so without the overhead associated with linking jumps to returns. It also allows delayed branching, in other words, branching on a status flag that was set previously. In this way conditional jumps are executed quickly because the instruction pipeline is never disrupted.

Fundamental to the chip's 100-ns instruction cycle is it's Harvard architecture, which affords parallel paths to instructions, to their addresses, and to a mix of operands and peripheral device addresses. Three buses keep those accesses separate: a 20-bit-wide path for instructions, a 13-bit-wide path for instruction addresses, and an 8-bit bidirectional data-and-address bus, which carries operands and peripheral device addresses (Fig.1).

With this arrangement, the controller fetches, decodes, and executes instructions in only one read-modify-write cycle. On the negative side, however, the chip incurs extra package pins, duplicated resources, and some loss in flexibility. Nevertheless, for high-speed control jobs, the costs are well worth it.

The chip can address a program containing as many as 8192 instructions, each 20 bits wide. Arithmetic and logic instructions operate on any contiguous sub-field – from 1 to 8 bits long – that appears in any of its registers or on the data-and-address bus. For example, a sub-field can be selected from a data byte, operated on, and written back to the source without changing the other bits. Compare that with the customary sequence of separate instructions that read a byte, mask the unused bits, and write the byte to a destination field. With similar efficiency, two barrel shifters, one placed before and one after the chip's ALU, can rotate data fields independently of each other (see "A Quick Software Reflection")

Moreover, the chip's 8-bit ALU can fully rotate and merge data, and wrap the carry bit around for multiple byte additions. Its program-counter and address-register section contains a four level push down stack and an independent 13-bit incrementer. Also making up the chip are 16 byte-wide data registers and four status flags. These flags are Carry, ALU $\neq$ Zero, a user-programmable bit (PS) and the Interrupts Receivable bit, which goes active when an interrupt mask is cleared and the stack is not full.

As for interrupts, the chip accepts maskable and non-maskable types, with the latter triggering on falling edges to prevent a stuck-at-0 fault from hanging up the controller. The chip responds to enabled interrupts within two instruction cycles of a request.

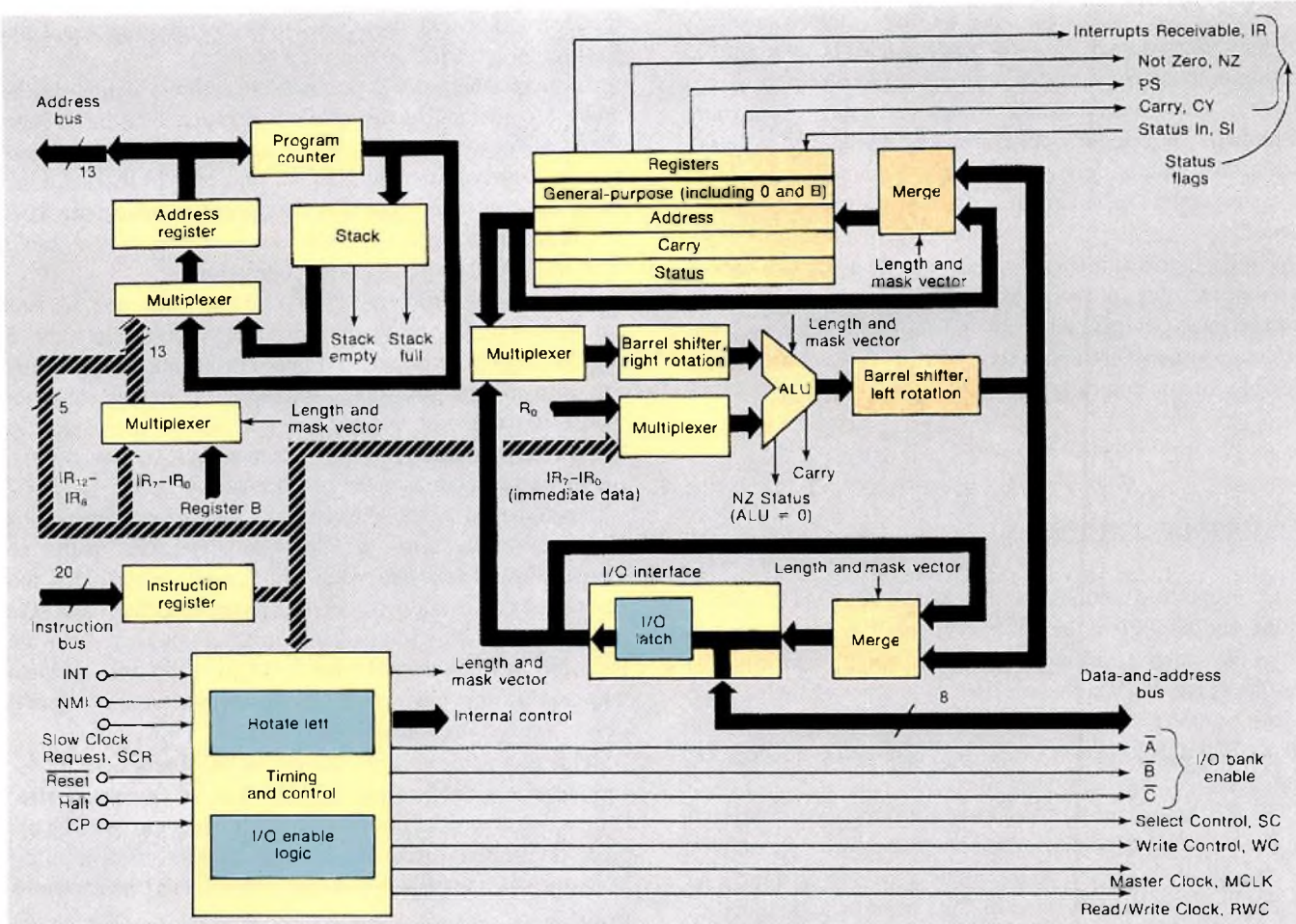


Fig.1 The 8X401A microcontroller depends on a Harvard architecture to execute instructions every 100 ns (even those that get data from a source), process it, and send it to a destination. The address, instruction, and data-and-address buses all carry information in parallel so that they can keep pace with the fast instructions. Barrel shifters placed before and after a data ALU make quick work of rotating bits.

FAST YET FIXED INSTRUCTION CYCLES

The need for tight and accurate timing loops characterizes many controller applications, and therein lies a prime advantage of having a fast yet fixed instruction cycle. To execute all the tasks included in an instruction, each 100-ns cycle contains four quarters. During the first quarter, instructions are latched and decoded; during the second, the operand is fetched and latched while the address of the next instruction is generated. The third and fourth quarters make up the output phase. Data and stack operations occur first, followed by the output data and a strobe signal. The program counter is also updated during the last quarter.

All timing signals derive from an external TTL clock, whose maximum frequency is 40 MHz. However, to accommodate slow peripherals, such as those in the earlier 8X300 family, the chip has a Slow Clock Request input (SCR) that divides the clock by four instead of by the usual factor of two.

TECHNOLOGY TALE

To meet the primary goal of a 100-ns instruction cycle, the 8X400 family relies on ECL circuitry. As a result, the 8X401A microcontroller is one of the most complex ECL chips ever to be designed. Specifically it is built with a 3-μm, washed-emitter, dual-metal bipolar process. Internal gates, about 3400 of them, are made from multiple layers of ECL and EFL (emitter-follower logic) and have TTL I/O buffers. Data and control outputs can switch 100-pF loads and sink 16 mA, whereas address lines sink 8 mA and can also drive up to 100 pF. Fully loaded, a gate typically exhibits delays of 1 to 2 ns.

The 64-pin chip is housed in a ceramic package, runs off a single 5 V d.c. supply, and dissipates 2,5 W maximum. Internally, a bandgap voltage regulator with a small negative temperature coefficient controls the gate operating current, so that power dissipation and gate speeds remain stable over supply voltage, temperature, and processing variations.

Asserting the signal executes instructions in 200 ns instead of 100 ns. Typically, the instruction memory would contain an extra data bit to activate the slower option invisibly to the software.

To execute instructions in a single chip, the chip uses three signals to select memory banks. These signals eliminate the extra cycle normally required to address data memory during any read-modify-write operation that involves external memory or peripherals. Through the selection signals, moreover, peripheral chips of the current and previous families can tie directly into the controller without decoding, multiplexing, or buffering. The signals switch as an instruction goes through its input and output phases. Only one signal is active during a read cycle, but more than one can be active during a write operation. That way data can be written to two external memory addresses by the same instruction.

PERIPHERAL VISION

Obviously, the microcontroller must have a number of basic control lines that govern its operation. For example, the $\overline{\text{Reset}}$ input clears the address register and program counter, puts all address and data buses into their high-impedance state, drives all control signals inactive, and sets the internal sequencer to its first phase. In addition, a $\overline{\text{Halt}}$ signal stops execution without altering the processor's internal state. It also allows a designer to single-step the controller's operation or to insert wait states for the sake of very slow or asynchronous peripherals.

Nonetheless, any microcontroller-based design would do better with peripheral devices that can keep pace with the controller. Except for Schottky or FAST devices, octal registers and transceivers ordinarily cannot match the fast read-modify-write sequence that characterizes transactions on the controller's data-and-address bus. That, however, is certainly not the case with the family's 8X470 fuse-programmable I/O port (Fig.2). Moreover, the I/O port insulates the user side from the bus's rigorous timing without resorting to extra circuitry for handshaking. Each of the chip's eight data lines may be programmed individually (by blowing the correct fuses) to yield a synchronously or asynchronously latched output, an input, or a transceiver.

To keep the handshaking simple, the port's user and controller sides each have a status bit associated with it. For example, if data is written from the user's side, the microcontroller senses that the Status bit is set, reads the data, and automatically resets the bit. Similarly, when the controller writes to the port, that port's Status bit is set. When the peripheral on the user side reads the data, the bit resets itself automatically.

Moreover, an unusual feature of the I/O chip lets a designer program any of the port's eight data lines as the Status bit, thereby letting the controller poll eight 8X470 ports at a time. For that to occur, each of the ports must have its Status bit programmed for a different line on the controller's data-and-address bus, in effect forming an 8-bit status register across that bus.

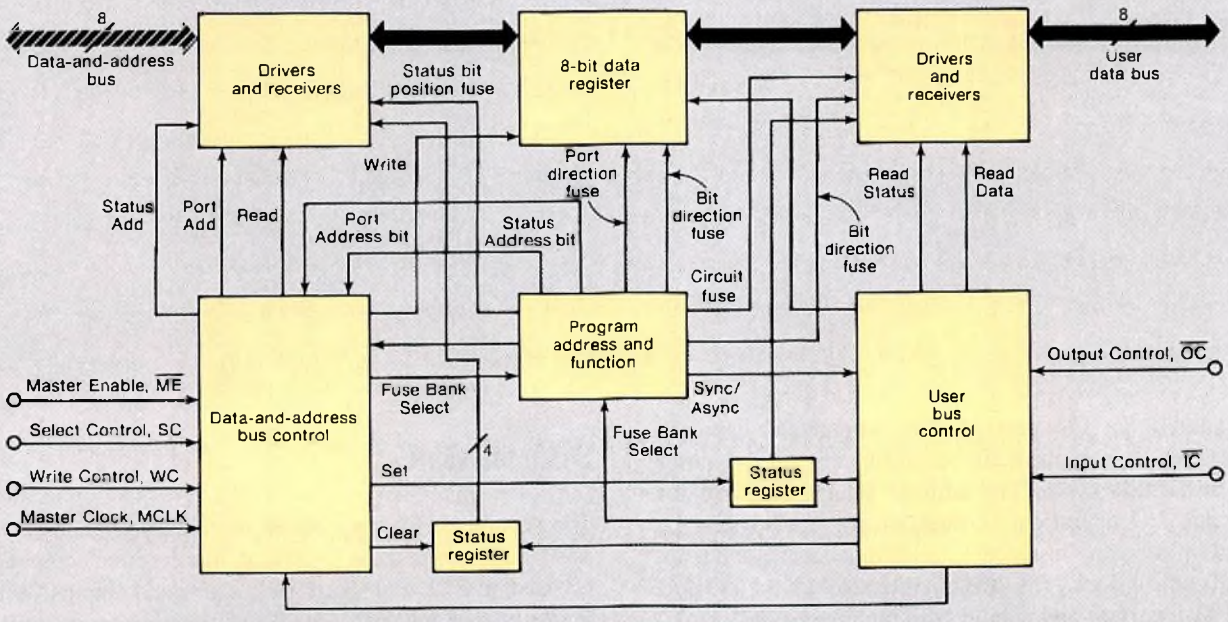


Fig.2 Within the 8X470 I/O port, fuses program individual bits for inputs, outputs, or transceivers between the data-and-address and user buses. In addition, a status bit for the data-and-address bus can be programmed for any of the eight lines, making multiport polling as simple as reading the byte formed by eight status bits.

A QUICK SOFTWARE REFLECTION

The prowess of the 8X401A's instruction set comes to light in a byte reflection calculation, a technique commonly used to find addresses during a fast Fourier transform. The result of the calculation is a bit-by-bit reversal of a particular byte of data: bit 0 becomes bit 7, bit 6 becomes bit 1, and so on.

Although the process is simple, it can rarely be reduced to efficient microprocessor code. Typically, each data bit is rotated out of a source location, through a carry register, and then shifted in the reverse direction into a destination. But the 8X401A offers a better way.

Given a useful relationship between the original and reversed data bits – namely, bit pairs 7 and 3, 6 and 2, 5 and 1, and 4 and 0 all start and end four bit positions from each other – rotation and merging operations can handle the reversal. The resulting code takes input data from register 1 and puts reflected data in register 0 (Program A). It is only eight instructions long and therefore executes in eight cycles, or 800 ns – roughly the time an 8-bit microprocessor needs to operate on one internal register or a 16-bit machine needs for two operations.

Faster execution is possible by adding a lookup table, so that a shorter, four-line program may be run (Program B). The table contains the data required to "reflect" a nibble. Each XEC instruction maps four bits to a Transmit Immediate instruction (op code XT8), which moves four bits of immediate data into register B without changing the other bits.

The total program takes 20 words, including the lookup table, but it executes in just six cycles: four for the four-line program and two for the instructions in the table. If speed is paramount, a different program can be written that runs in only three cycles and occupies 258 words. For this approach, the lookup table contains full bytes instead of nibbles.

PROGRAM A. AN EIGHT-CYCLE REFLECTION

```
REFLECT AN8  R1, 11H     ; Using AND immediate, get
                           two bits of data.
        MOV  RF, 1, R0   ; Move two bits to proper
                           position in result.
        AN8  R1, 22H     ; Get the next two bits, and
        XOR  RF, 3, R0   ; Merge into proper position
                           in the result.
        AN8  R1, 44H     ; Get the next two bits.
        XOR  RF, 5, R0   ; Merge the bits into the
                           result.
        AN8  R1, 88H     ; Get the last two bits.
        XOR  RF, 7, R0   ; Merge the bits for form the
                           final result.
```

PROGRAM B. A SIX-CYCLE REFLECTION

```
REFLECT MOV  R1, RB      ; Put the data byte in
                           register B.
        XEC  L4, TABLE   ; Form one nibble of result in
                           register B.
        MOV  RB, 4, RB   ; Swap nibbles in register B.
        XEC  L4, TABLE   ; Finish the result in
                           register B.

TABLE   XT8  L4, RB, 0   ; 0000 = 0000.
        XT8  L4, RB, 8   ; 0001 = 1000.
        XT8  L4, RB, 4   ; 0010 = 0100.
        XT8  L4, RB, 0CH ; 0011 = 1100.
        XT8  L4, RB, 2   ; 0100 = 0010.
        XT8  L4, RB, 0AH ; 0101 = 1010.
        XT8  L4, RB, 6   ; 0110 = 0110.
        XT8  L4, RB, 0EH ; 0111 = 1110.
        XT8  L4, RB, 1   ; 1000 = 0001.
        XT8  L4, RB, 9   ; 1001 = 1001.
        XT8  L4, RB, 5   ; 1010 = 0101.
        XT8  L4, RB, 0DH ; 1011 = 1101.
        XT8  L4, RB, 3   ; 1100 = 0011.
        XT8  L4, RB, 0BH ; 1101 = 1011.
        XT8  L4, RB, 7   ; 1110 = 0111.
        XT8  L4, RB, 0FH ; 1111 = 1111.
```

To address an I/O port, the microcontroller issues a peripheral address on the main bus during the fourth quarter of an instruction cycle. The address selects a device for subsequent I/O operations. (Alternatively, devices can be selected by decoding instruction fields that correspond to an external control store.) Like the microcontroller, the I/O port has a TTL interface and is built with high-speed ECL parts. Conventional bipolar programming instruments will blow the nickel-chromium fuses, which are arranged in four banks of eight. In all, the fuses can create up to 2^{31} port configurations.

FAST MEMORY

The second peripheral chip in the controller family is the 8X450, a 256-byte static RAM that, like the other components, is based on ECL and sports TTL inputs and outputs. With an access time of only 20 ns, the RAM can serve the controller in many ways: as a deep register, for example, or as a data buffer on the main bus. It exchanges a conventional Address Latch Enable signal ($\overline{\text{ALE}}$) with the controller in order to latch an 8-bit address.

Like the I/O port, the RAM is accessed either directly through the controller (during its fourth quarter of the instruction cycle) or through externally stored bits that generate addresses and control the chip's Master Enable input ($\overline{ME}$). The latter case allows multiple RAMs to make up one bank. For example, four of the chips can make up a 1 k-by-8-bit space on the data-and-address bus when an extended control field generates the addresses. In this arrangement, the lower eight bits of the ten-bit addresses are common to all four chips, and the two high-order bits are decoded externally (Fig.3). In addition, because of the chip's conventional handshaking signals: Chip Select (CS) and $\overline{ALE}$, it makes a suitable general-purpose RAM for other processors.

The microcontroller and its support chips can team up in a data concentrator, also known as a front-end processor or a terminal multiplexer. Commonly part of a large time-sharing system, a data concentrator offloads the slow I/O polling and character-level transactions of a large cluster of terminals, all communicating with a mainframe computer (Fig.4). Smaller, low-cost processors accumulate characters from terminals in order to exchange (through a DMA operation) lines and pages with the mainframe. In this way, data is processed while the mainframe attends to other tasks.

The concentrator can manage about 240 terminals, although the precise number depends on factors like the type of editing actions required, the rate at which data arrives at a UART, and the number of users logged on.

WHICH WAY DID IT GO...?

In operation, bytes travel between an array of UARTs. Each one strobes its data into a corresponding I/O port, which sets the Status bit, to indicate a transfer. The microcontroller can poll the ports in groups of eight, looking for a non-zero eight-bit status word to check for available data. Based on the bits that it finds set, it takes the data from corresponding ports. Then it issues successive data bytes over its data-and-address bus to a 24-kbyte static RAM.

The RAM buffers one line for every UART, letting the controller perform local editing by acting on carriage returns and other control characters. For example, on receiving a control character, a DMA address generator passes its contents to the buffer RAM, whereupon the controller initiates the DMA transfer from the buffer to the host. Alternatively,

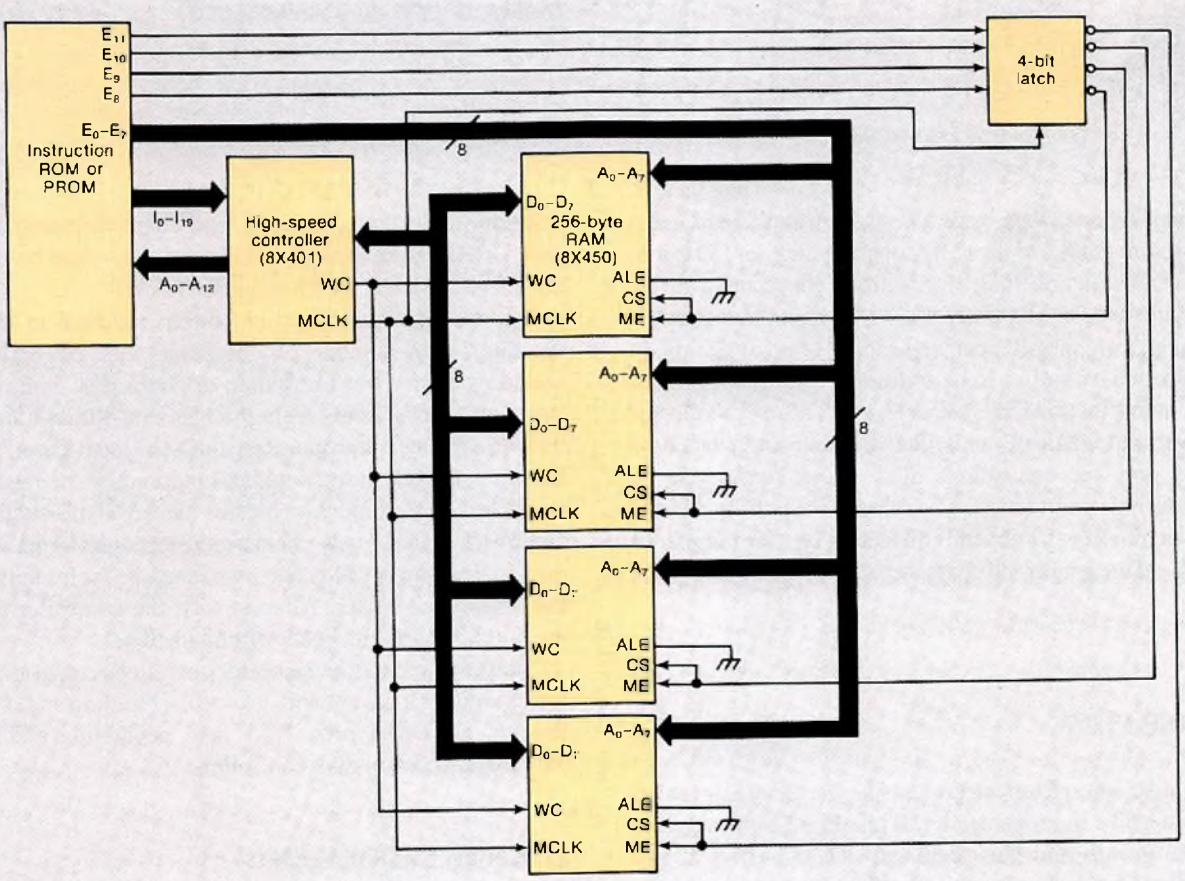


Fig.3 With the help of external decoding logic, four 256-byte RAMs each with a 20-ns access time create a large memory space on the main data bus. The lower eight bits are common to all four memory chips, and the two high-order bits come from external logic. The standard CS and $\overline{ALE}$ pins make it easy to use these fast RAMs with other processors as well.

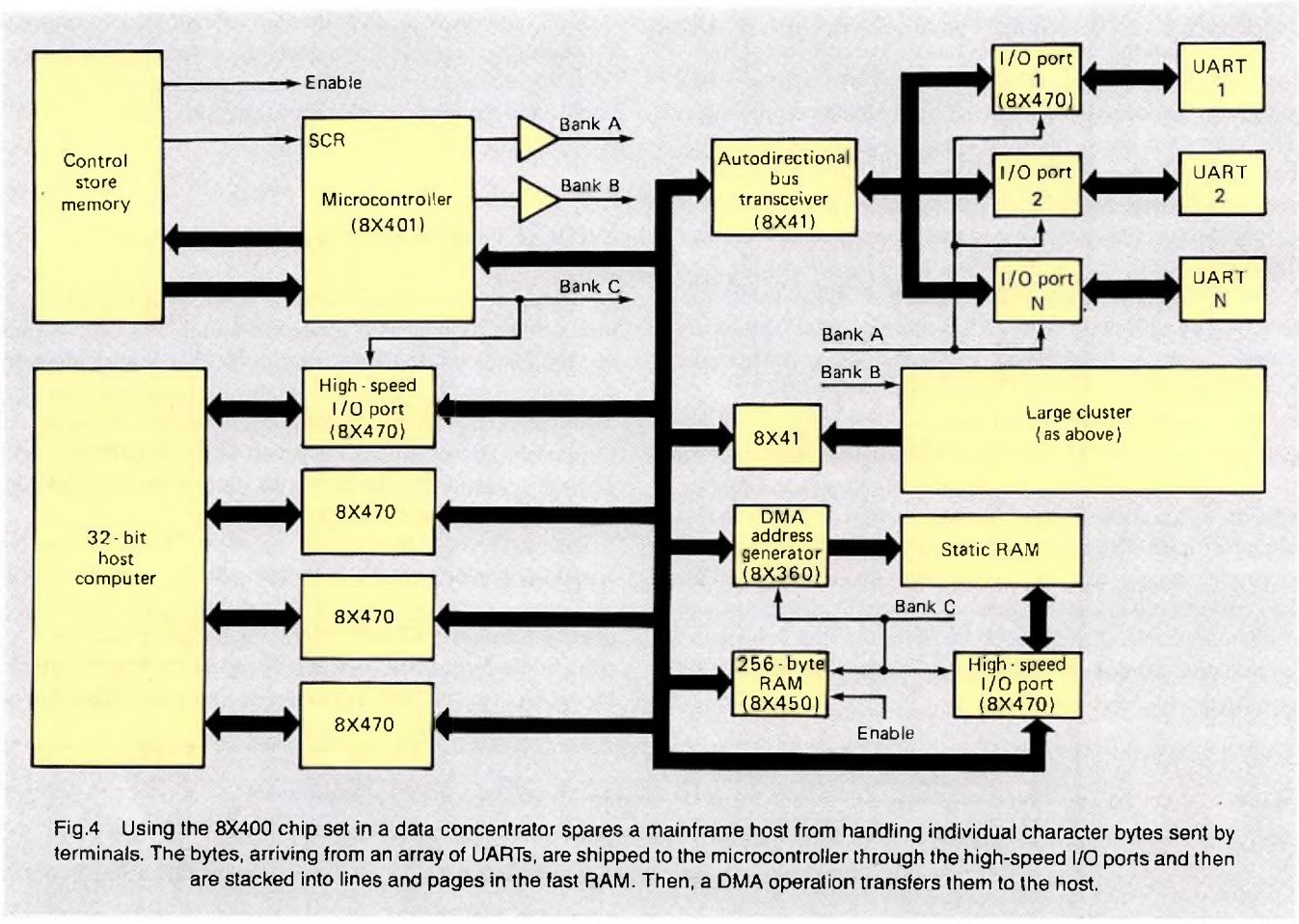


Fig.4 Using the 8X400 chip set in a data concentrator spares a mainframe host from handling individual character bytes sent by terminals. The bytes, arriving from an array of UARTs, are shipped to the microcontroller through the high-speed I/O ports and then are stacked into lines and pages in the fast RAM. Then, a DMA operation transfers them to the host.

editing can be done when bytes are taken from their I/O port on their way to the RAM array. Through an array of I/O ports, each one constructing long words from consecutive bytes, either path can be configured for a 32-bit host processor.

Although the controller can drive loads of up to 100 pF, in this application it requires some additional drive in the form of the 8X41 autodirectional bus transceivers. The open-collector transceivers automatically sense the direction of the data flow and need only the controller's Slow Clock Request to be asserted during a transaction. The value of the pull-up resistor for the bus transceivers depends on factors like the number of I/O ports and the length and characteristics of the transmission line.

REVERSE FLOW

Passing information from the host to specific terminals is also supervised by the microcontroller. It breaks 32-bit words into four equal groups and puts them into RAM buffers at full speed. When the buffers are full, the controller empties them into the 24-kbyte static RAM for processing and eventual distribution to a UART. The controller's software must maintain a large number of pointers, so that the correct position, underflow condition, and character translation for each UART can be monitored. These pointers can be stored in the 256-byte or the 24-kbyte buffer RAM.

Depending on the kind of editing required in the concentrator, any number of operations can be performed, including a very fast translation of characters. Software can intercept all characters from the data-and-address bus, send them to a register, and undertake the XEC instruction, thereby transferring control to an address indexed by the intercepted characters. If that address contains the XMIT instruction, the controller issues a new character in response to the original one. In this way, it needs only two machine cycles to translate the original character. Alternatively, the controller can test and modify only sub-fields within any byte.

These same bit-stream control operations can also be used for generating local network protocols, building and stripping headers for DMA processors, and generating and testing correction codes in disk controllers.

ACKNOWLEDGEMENT

This article originally appeared in the May issue of "Electronic Design", copyright 1986, Hayden Publishing Co. Inc.; permission to reprint is gratefully acknowledged.

Integrated video programming system (VPS) decoder

AXEL LENTZER and GÜNTHER STÄCKER

When television programmes are recorded under control of the timer of a conventional video cassette recorder, any unscheduled changes of the programme timing will result in failure to record the beginning or end of the desired programme material. This can cause considerable frustration during playback.

As a result of work carried out in West Germany, European broadcasting authorities have decided to introduce a Video Programming System (VPS) code into television transmission formats which, when decoded at the receiver, will enable the actual start and stop times of a programme to be identified.

We have developed a set of two chips, the SAA5235 Data Line Slicer and the SAF1134P or SAF1135P Data Line Decoder, for decoding the VPS signal and controlling a video cassette recorder via the simple 2-wire inter-IC bus (I^2C bus).

The bipolar SAA5235 is in a 28-pin DIL package. It operates from a nominal 12 V supply and requires a supply current of typically 70 mA. The CMOS SAF1134P is in a 24-pin DIL package. The nominal supply voltage is 5 V and typical current consumption is 5 mA. The CMOS SAF1135P is functionally similar to the SAF1134P, but higher density fabrication allows it to be accommodated in a smaller 14-pin DIL package. It also has the additional capability of decoding sound status as well as programme timing information. The supply voltage for the SAF1135P is also 5 V but its typical current consumption is only 1 mA.

Notable features of the chip set are:

- complete system in two chips with a minimum number of peripheral components.
- high performance due to the use of well established videotex techniques
- high reliability resulting from a high level of integration

ELEMENTS OF THE VPS CODE

The VPS Code is transmitted in line 16 of the first field of every tv picture frame in the format shown in Fig.1. The bit rate is 2,5 Mbit/s and the encoding method is bi-phase (BI-ϕ). Fifteen words, each 8 bits long, are contained within the data stream. The repetition period of the data line is 40 ms when operating on a 50 Hz tv field system.

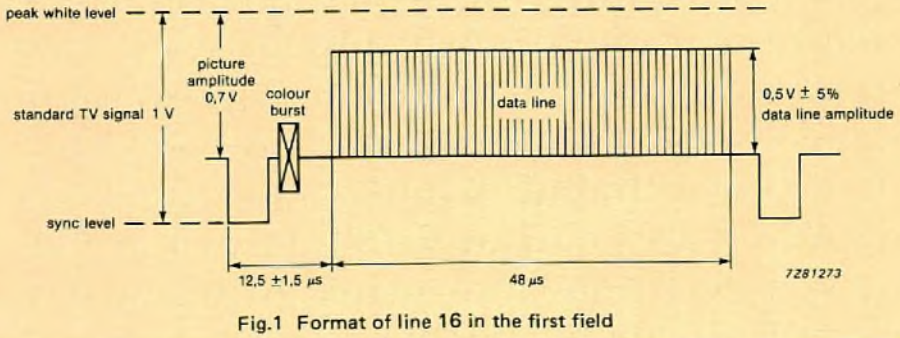


Fig.1 Format of line 16 in the first field

Figure 2(a) shows the assignment of information to each word. At present, only words 5 and 11 to 14 inclusive are relevant. The control information for the video recorder is detailed in Fig.2(b).

Using the VPS information, it is possible to inform the video recorder of any changes made in the planned programme structure. Essentially, there are two groups of codes carrying this information:

– the regular VPS label with data, time of day and programme source
– special system codes; i.e. system status code (handing back control to the video recorder if no VPS label is transmitted) interrupt code (identifies interruptions within a programme) and pause code (to allow for unscheduled announcements to be made between two programmes).

There is no special code to indicate the delay of a broadcast. The label of a delayed programme appears, as appropriate, at the later transmission time.

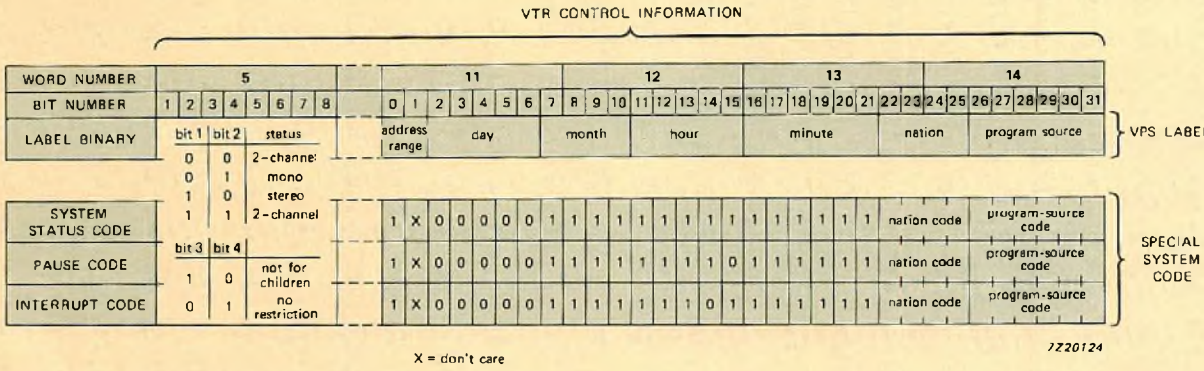


Fig.2(a) Assignment of information in the data stream

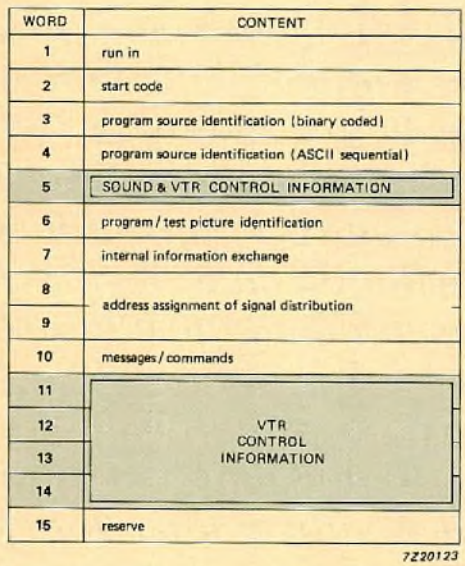


Fig.2(b) Video recorder control information

OPERATION OF THE VPS DECODER

Figure 3 is a functional block diagram of a VPS decoder with the SAA5235 Data Lince Slicer and the SAF1135P Data Line Decoder.

Data Line Slicer

The input to the SAA5235 requires a composite video plus blanking and sync signal (CVBS) from a source impedance of less than 250 Ω. This may be conveniently obtained from the vision i.f. stage of the video recorder. Information describing peak sync level and black level is extracted from the CVBS signal and stored as a voltage in external capacitors C1 and C2. The sync slicer in the SAA5235 is adaptive, and uses this information to maintain a slicing level of 50% peak sync amplitude over a wide dynamic range of input signal levels.

The sync sliced video signal is clamped to the black level and fed, via a gain selector switch which allows typical peak-to-peak CVBS input levels of 1 V or 2,5 V, to a high-frequency loss compensator. Capacitor C3 acts as a high frequency video filter and C4 is used to store the high frequency level value during data transitions. The purpose of the high frequency loss compensator is to improve the definition of the data transitions and allow accurate decoding of the BI-ϕ data under poor reception conditions. The equalized signal is applied to the input of an adaptive data line slicer which, using stored information describing video

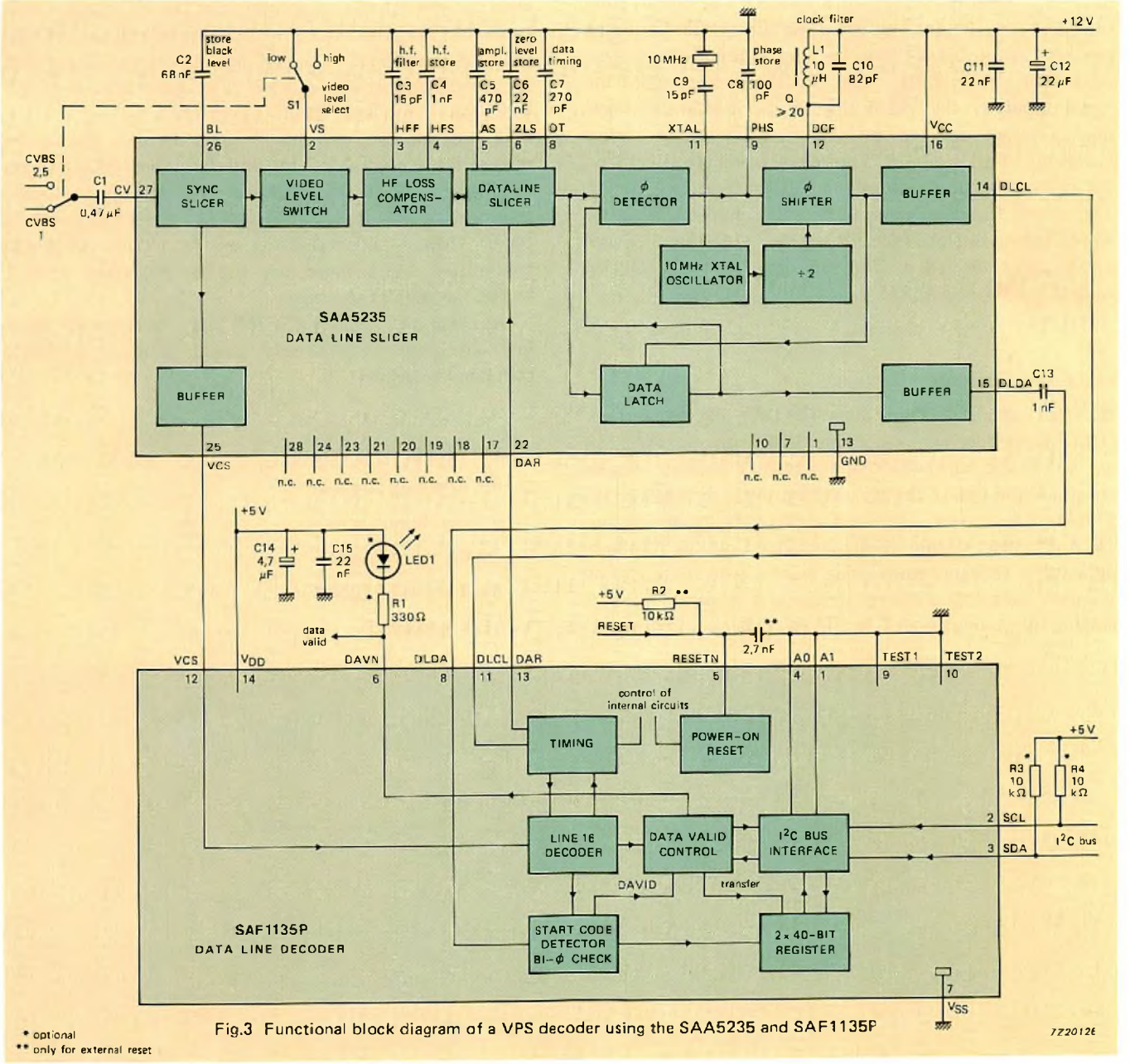


Fig.3 Functional block diagram of a VPS decoder using the SAA5235 and SAF1135P

amplitude and black level (again as a voltage in external capacitors C5 and C6), enables the video level to be sliced at the 50% value. Timing for the data line slicer is determined by C7 in conjunction with an internal current source and voltage level switches. The timing circuit may be reset by an external data reset signal.

A stable 5 MHz clock (as required for BI-ϕ decoding) is generated by a 10 MHz crystal-controlled oscillator and divide-by-two counter in the SAA5235.

The phase of the clock and BI-ϕ data stream is synchronized by a digital phase-locked loop. The data stream is fed to one input of a phase-sensitive detector and also to the serial input of a shift register (data latch). The output from the shift register is taken to the second input of the phase-sensitive detector and is also buffered to form the data line data (DLDA) output from the SAA5235. The output from the phase-sensitive detector is fed, via a loop filter (requiring one external capacitor C8) to the control input of a voltage-controlled phase shifter. The 5 MHz clock provides the signal input to the phase shifter; the fundamental frequency being selected by the parallel-resonant circuit consisting of L1 and C10. To provide adequate selectivity, the Q-factor of this resonant circuit must be at least 20. The output from this stage, (after being clipped to a square wave), is used to clock the shift register, so closing the loop, and is then buffered to form the data line clock (DLCL) output from the SAA5235.

Data line Decoder

Buffered signals data line data (DLDA), data line clock (DLCL) and video composite sync (VCS) from the SAA5235 are fed to the startcode detector/biphase checker, timing generator and line 16 decoder respectively in the SAF1135P. The line 16 decoder identifies the first field and selects line 16. A data reset (DAR) signal is generated and the startcode detector is activated to examine word 2 (the startcode) of the data stream. If a correct startcode is received, words 5 and 11 to 14 are decoded and an error check is performed. The decoded data is loaded into a register bank. The data reset signal is fed back to the SAA5235 where it is used to clear the data line slicer and leave it in a condition to process the next line 16 information.

Internal signals data valid (DAVID) and data available (DAVN) are generated if the BI-ϕ data stream is error-free. DAVN is reset LOW after reception of an error-free data line and set HIGH at the beginning of the next field 1. If no valid data is available, DAVN remains HIGH but a 100 ns pulse is inserted at the start of the next line 16. DAVN is available externally and can be used as a trigger. Timing for DAR and DAVN is shown in Fig.4 and Fig.5.

DAVID is used to initiate transfer of the data into a second register ready to be read to the I^2C bus. If the system is addressed at this time, the transfer is delayed until the next start/stop condition of the I^2C bus has been received. The data stored in the second register remains valid only until read to the I^2C bus. An internal flag is then set to indicate that new data will be available after error-free reception of line 16 of the next field 1.

A bus master is needed to clock the data out of the second latch via the I^2C bus interface. The dataline data (DLDA) circuit on the chip can operate only as a slave transmitter. Data is sent MSB first in the format shown in Fig.6. There is no restriction on the number of words transmitted, but if more than five are requested, word 5 will be repeated as necessary.

An external reset (RESETN) may be applied which invalidates any data already stored. When a RESETN command is applied:

- the I^2C bus logic is reset
- the new data flag is set
- internal timing is reset
- DAVN is forced LOW
- DAR is forced HIGH
- SDA is released.

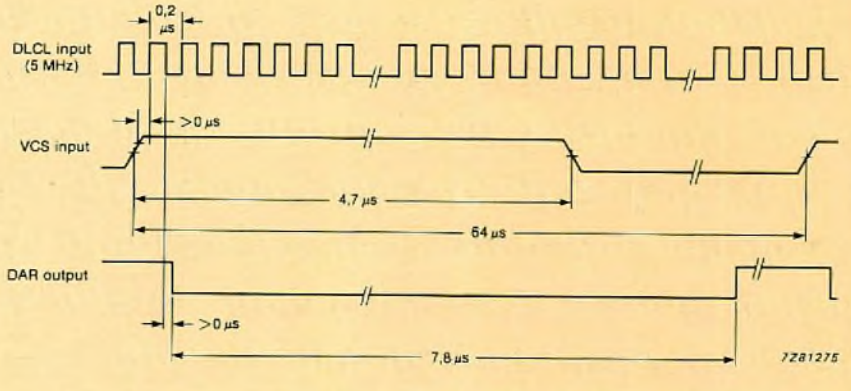


Fig.4 Timing diagram of DAR

When RESETN goes HIGH, the reset period is terminated with the next negative edge of DLCL. DAVN then goes HIGH and the normal operating procedure is resumed.

The rise time of the applied RESETN pulse should be longer than 50 μs. This period is determined by the 10 kΩ resistor and 2,7 nF capacitor connected to the RESETN pin. If the external reset facility is not required, RESETN should be connected to V_{DD}.

Two of the I^2C bus address bits can be externally preset by connecting pins A0 and A1 to either V_{DD} or V_{SS}. This allows up to four I^2C bus interfaces to be connected to the bus, giving it much greater control capacity.

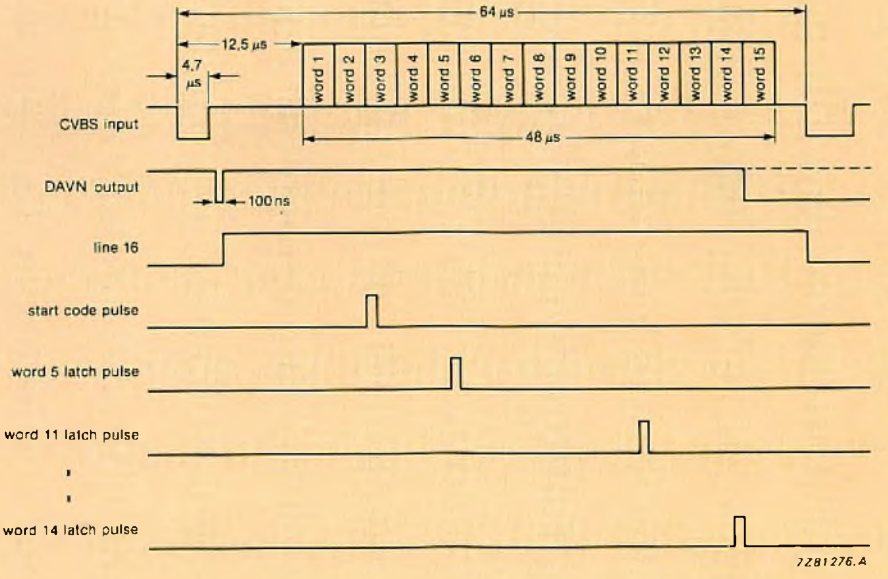


Fig.5 Timing diagram of DAVN

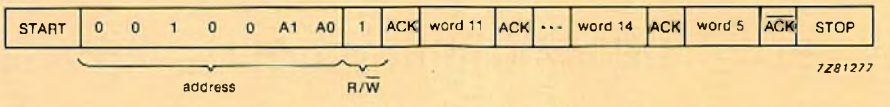


Fig.6 Format of I^2C-bus data

AN ALTERNATIVE VPS DECODER

The connection diagram of an alternative VPS decoder using the SAF1134P Data Line Decoder is shown in Fig.7.

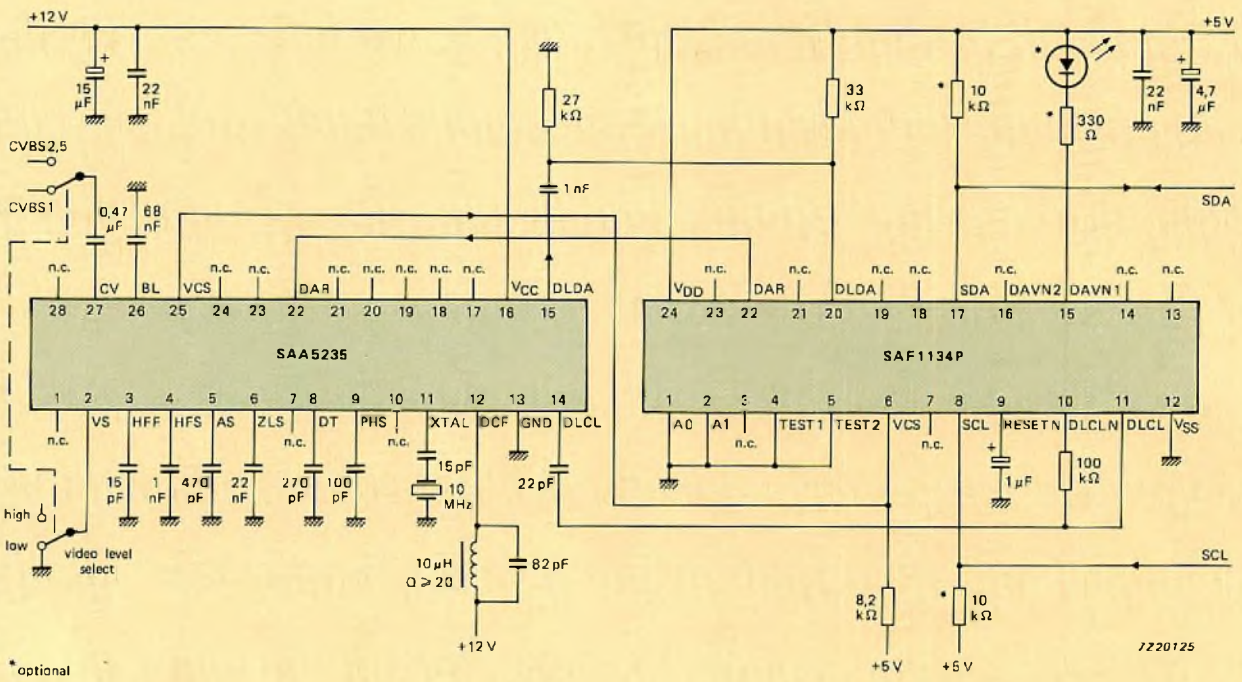


Fig.7 An alternative VPS decoder using the SAF1134P Data Line Decoder

REFERENCE

"I²C bus specification". Philips publication, 1983, ordering code 9398 615 0001.

High-temperature electrolytic capacitors

AD OTTEN and JUST SLAKHORST

During the past decade the operating temperature of non-solid electrolytic capacitors has doubled to its present value of 125 °C (or even 150 °C for short periods of time). This high-temperature capability has opened up new applications, for example in military electronics and automotive systems. The higher-temperature capability is also very desirable for switched-mode power supplies and other electronic power applications because it allows a much higher level of ripple current to be tolerated. For example, at an ambient temperature of 70 °C, an electrolytic capacitor with a maximum operating temperature of 125 °C could tolerate a temperature rise of 55 °C due to power dissipation caused by additional ripple current.

Another advantage of an increased temperature rating is that it results in a considerable increase in life expectancy at lower temperatures. This article describes the 2222 118 ..... range of high-temperature electrolytic capacitors and discusses design criteria for high-temperature operation. It shows how to calculate life expectancy, gives life-test data and suggests suitable application areas.

CAPACITOR CONSTRUCTION FOR HIGH-TEMPERATURE OPERATION

The basic construction of a non-solid aluminium electrolytic capacitor has been described in detail (Ref.). For operation at high temperature, special care must be taken with all aspects of the construction. A cut-away view of the construction of the 2222 118 ..... range of high-temperature capacitors is shown in Fig.2.

Fig.1 The 2222 118 ..... range of high-temperature electrolytic capacitors offers a high volumetric efficiency. An extensive range of C-V products is available in six can sizes and two can styles.

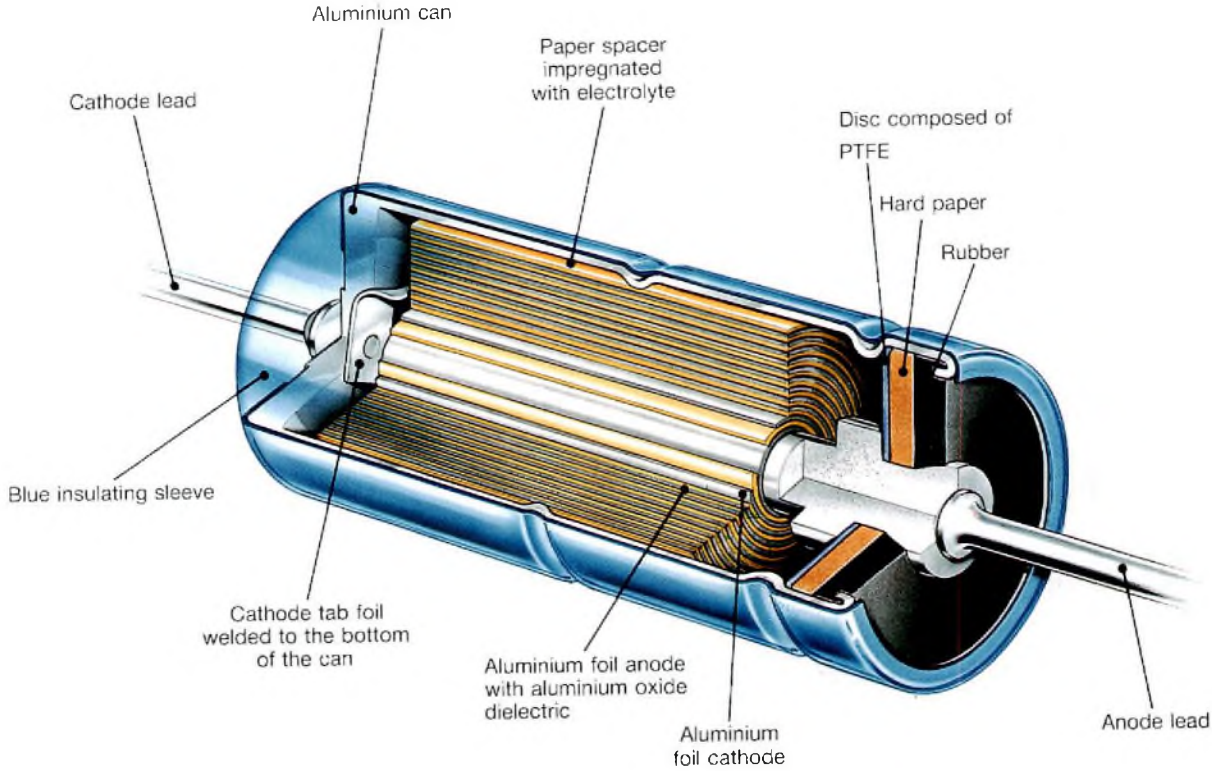


Fig.2 Cut-away view showing the axial construction of the 2222 118 ..... range of high-temperature non-solid aluminium electrolytic capacitors.

The anode foil

The dielectric of a non-solid electrolytic capacitor is formed by anodizing the anode foil to convert its surface to aluminium oxide (Ref.). The thickness of the dielectric determines the rated voltage of the capacitor. Theoretically, the breakdown field strength of a perfect aluminium oxide crystal (Al_2O_3) is 7×10^6 V/cm. This means that such a layer of aluminium oxide can withstand 1 V for each 1,42 nm thickness. However, the dielectric on the anode foil is not completely perfect. In fact, defects can occur in the oxide layer during capacitor manufacture due to mechanical damage and temperature gradients. As a result, there will be some interaction between the dielectric and the electrolyte resulting in the creation of a leakage-current path.

This leakage current is constant up to the rated voltage V_r but then starts to rise as shown in Fig.3. The maximum voltage that the oxide layer can withstand is known as the forming voltage V_f.

During the life of the capacitor, the leakage current will generate hydrogen gas which will either be absorbed by the electrolyte or stored in the free volume of the capacitor. By careful design of the electrolyte/anode foil combination the evolution of gas can be minimized. In addition, to obtain a low leakage current, the optimum ratio of V_f/V_r must be selected. This is done by measuring the I-V characteristic (Fig.3) of the foil and then selecting V_f as the highest voltage possible before the steep increase in current starts. In practice V_f occurs at about 30% above the rated voltage V_r. For example, for a capacitor rated at 85 °C an expected life of 2000 hours can be achieved by selecting $V_f/V_r = 1,3$.

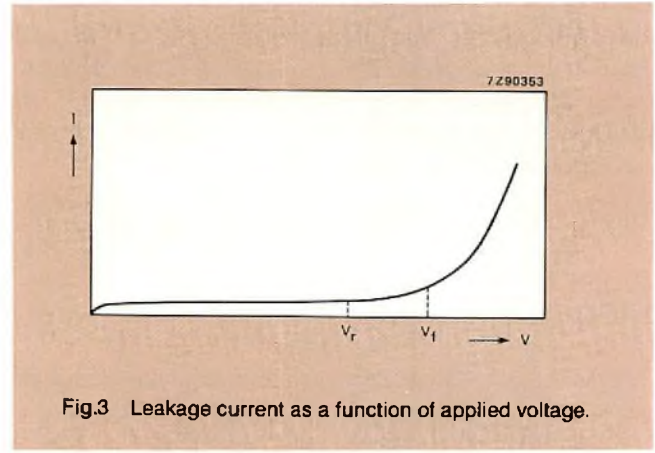


Fig.3 Leakage current as a function of applied voltage.

However, V_f is inversely proportional to absolute temperature, so for the same low leakage current at 125 °C, the ratio of V_f/V_r must be increased to:

$$\frac{V_f}{V_r} = 1{,}3 \frac{(273 + 125)}{(273 + 85)} = 1{,}45$$

So, for higher temperature operation, a higher forming voltage must be used. However, for any dielectric/electrode combination, $V_f \times C$ = constant, so the use of a higher forming voltage means lower values of capacitance for a given rated voltage. Rated voltages of capacitors are quoted in the R5 range of 6,3 V; 10 V; 16 V; 25 V; 40 V etc. The equivalent forming voltages at 85 °C are 1,3 times higher and so fall into the range 8,1 V; 13 V; 20,8 V; 32,5 V; 52 V etc. .

In designing the 2222 118 ..... range of high-temperature electrolytic capacitors, a margin on forming voltage has been deliberately included. For example, to make a 10 V capacitor for use at 125 °C would require a forming voltage of 14,5 V. However, the next-highest available forming voltage is 20,8 V and this value is therefore used.

So, it will be seen that the 10 V, 125 °C capacitor could also be used at 16 V, 85 °C. This is a very powerful feature of the range.

The electrolyte

The electrolyte is an organic solution. The solvent can be either pure glycol, a water/glycol mixture or an organic solvent such as DMAC (dimethyl acetamine), DMF (dimethyl formanide), NMF (N methyl formanide), butyrolactone or mixtures of organic solvents. Since the electrolyte largely determines the ESR (equivalent series resistance) and therefore the impedance of the capacitor, it must have a low resistivity over a wide temperature range (from −55 °C to the maximum operating temperature). Furthermore, the breakdown voltage of the electrolyte must be well above the rated voltage of the capacitor at the maximum operating temperature.

Additionally, in order to ensure long life of the capacitor during storage and operation, the electrolyte must not corrode the aluminium oxide and must be self-healing when voltage is applied. Since aluminium oxide is susceptible to attack by water, electrolytes with a water content must be avoided in long-life electrolytics to prevent unacceptably high leakage current. However, low resistivity at low temperatures can only be achieved with glycol electrolytes by adding a considerable amount of water and so glycol and water/glycol solvents cannot be used for long-life electrolytics. Operation at temperatures as high as 125 °C requires a very stable solvent mixture which further reduces the choice of electrolyte. The 2222 118 ..... range of high-temperature electrolytic capacitors uses a DMAC mixture electrolyte which has low resistivity and will withstand 150 V at up to 150 °C.

Table 1 Can sizes for the available values of nominal capacitance C (μF) and rated voltage U_R (V)

can size	nominal dimensions (mm)
	miniature
4	ø 6,5 × 18
5	ø 8 × 18
6	ø 10 × 18
7	ø 10 × 25
	small
00	ø 10 × 30
01	ø 12,5 × 30
02	ø 15 × 30
03	ø 18 × 30
04	ø 18 × 40
05	ø 21 × 40

C_{nom} (μF)	U_R (V)							
	6,3	10	16	25	40	63	100	200
1						4		
1,5						4		
2,2						4		
3,3						4		
4,7						4		
6,8						4		
10						4		
15						4		00
22						4		01
33						5		02
47					4	5	00	03
68					5	6	01	04
100				4	5	7/00	01	05
150			4	5	6	01	02	
220		4	5	6	7/00	01	03	
330	4	5	6	7	01	02	04	
470		6	6	7/00	01	03	05	
680		6	7/00	01	02	04		
1000	6	7/00	01	01	03	05		
1500	7/00	01	01	02	04			
2200	01	01	02	03	05			
3300	01	02	03	04				
4700	02	03	04	05				
6800	03	04	05					
10000	04	05						
15000	05							

Sealing the can

For high-temperature capacitors the can seal must be of extremely high quality. DMAC electrolyte has very high penetration properties and is known to dissolve plastics. Additionally, at high temperatures many plastics melt and deform. The seal of the can must prevent dielectric seepage through the end-cap and along the sealing edge of the can. It must also be sufficiently robust to withstand internal pressures caused by electrolyte gas and hydrogen generated by leakage current. PTFE has the best resistance to electrolyte penetration and hard-paper is cost-effective and offers extremely stable properties. When combined with a rubber-cap, which compresses when folding the can, a very effective seal is obtained. The seal used for the 2222 118 ..... range of electrolytic capacitors is shown in Fig.2.

Extensive tests carried out on these capacitors fully demonstrate the high quality of this seal.

CAN SIZES

The construction shown in Fig.2 has been selected for the 2222 118 ..... range. The use of an advanced deeply-etched foil gives this range of capacitors a very high volumetric efficiency for any given rated voltage. However, high volumetric efficiency does not provide the lowest ESR, and so the range of can sizes has been chosen to provide an optimal trade-off between high volumetric efficiency and low ESR. All can sizes are available with axial leads. Can sizes 4 to 7 are also available on bandoliers.

Can sizes 02 to 05 are also available in a single-ended style with printed wiring pins, especially suitable for use where severe shock or vibration is likely to occur.

The range of can sizes available for the values of capacitance and rated voltage is given in Table 1.

LIFE EXPECTANCY

When ripple current (I_R) passes through a capacitor, the ESR of the capacitor (R) causes power ($P=I^2R$) to be dissipated in the capacitor.

This power will increase the core temperature (T_c) of the capacitor. The maximum permissible ripple current (I_{Rmax}) is defined as the current that produces a temperature difference (ΔT) of 10 K between core temperature and ambient operating temperature. The actual ripple current (I_A) will therefore cause a temperature difference (ΔT) of

$$\Delta T = \left(\frac{I_A}{I_{Rmax}}\right)^2 \times 10\,K$$

so the actual core temperature (T_c) will be

$$T_c = T_{amb} + \left(\frac{I_A}{I_{Rmax}}\right)^2 \times 10\,K$$

$$\text{So } \frac{I_A}{I_{Rmax}} = \frac{T_c - T_{amb}}{10} \qquad (1)$$

In general the lifetime of a component increases as operating temperature decreases. For non-solid electrolytic capacitors we can say the following:

- The life expectancy of an electrolytic capacitor depends only on core temperature (T_c).
- At ambient operating temperatures up to 85 °C (maximum core temperature 95 °C), the life expectancy of the capacitor doubles for a 10 K decrease in temperature.

This can be expressed mathematically as

$$L = 2^{\frac{(T_{cmax} - T_c)}{10}} \qquad (2)$$

Where L = life multiplier,
T_{cmax} = maximum core temperature (°C)
and T_c = actual core temperature (°C)

When extended to higher operating temperatures, the following changes occur:

- At ambient operating temperatures between 85 °C and 125 °C (maximum core temperature between 95 °C and 135 °C), the life expectancy of the capacitor doubles for a 15 K decrease in temperature, and Eq.2 is modified to

$$L = 2^{\frac{(T_{cmax} - T_c)}{15}}$$

- At ambient operating temperatures between 125 °C and 150 °C (maximum core temperature between 135 °C and 160 °C), the life expectancy of the capacitor doubles for a 20 K decrease in temperature, and Eq.2 is modified to

$$L = 2^{\frac{(T_{cmax} - T_c)}{20}}$$

Figure 4 plots I_A/I_{Rmax} against T_{amb} according to equation 1, with life multiplier L as a parameter.

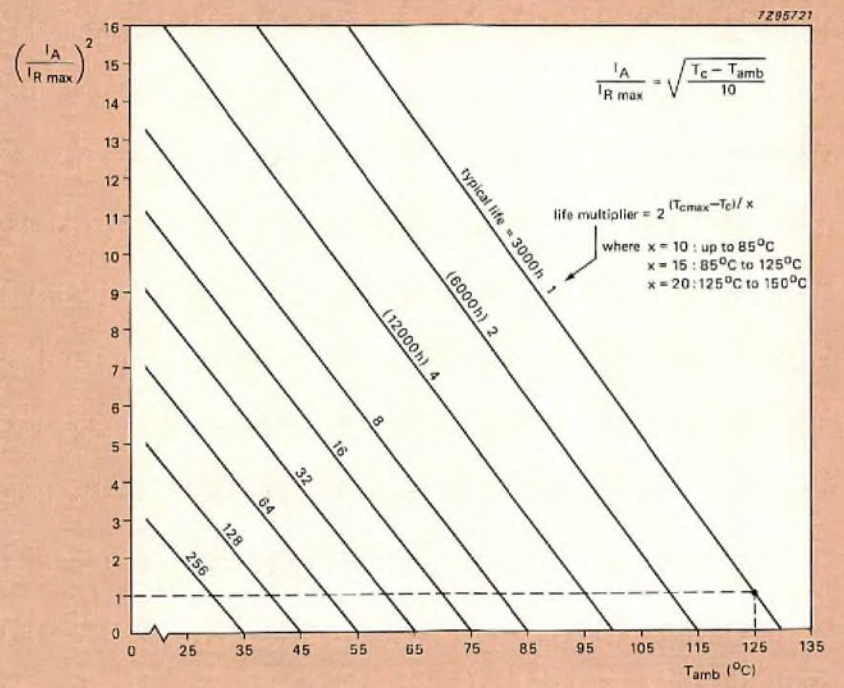


Fig.4 Typical life expectancy graph for a 2222 118 15472 capacitor (4700 μF, 16 V, can size 18 mm diameter × 40 mm).

At T_{amb} = 125 °C $I_A = I_{Rmax}$, and from the 2222 118 15472 data sheet I_{Rmax} = 1363 mA. Similarly, the data sheet defines the typical lifetime at T_{amb} = 125 °C as 3000 h. So, Fig.4 shows that typical lifetime increases dramatically at lower temperatures. For example, at T_{amb} = 75 °C, life multiplier L = 16, so typical lifetime = 16 × 3000 h = 48000 h, which is about 5 years. Figure 4 is of course a generalized graph which applies to all types of 2222 118 ..... high-temperature capacitors.

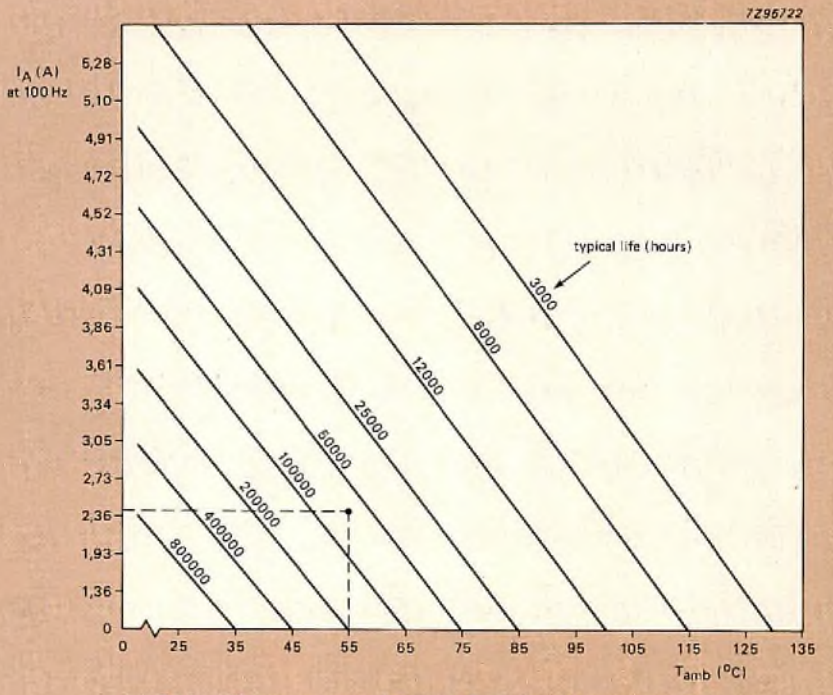
Figure 5 compares the life expectancy of a 4700 μF, 16 V high-temperature capacitor (2222 118 15472) with that of the equivalent standard capacitor (4700 μF, 16 V type 2222 021 15472). It can clearly be seen that, when used at an ambient temperature of 55 °C and with a ripple current of 2,4 A, the expected life of the high-temperature capacitor (70000 h) exceeds that of the standard capacitor (10000 h) by a factor of 7. This feature makes high-temperature electrolytics extremely suitable for long-life applications, for example in telephony or military applications.

Life-test results

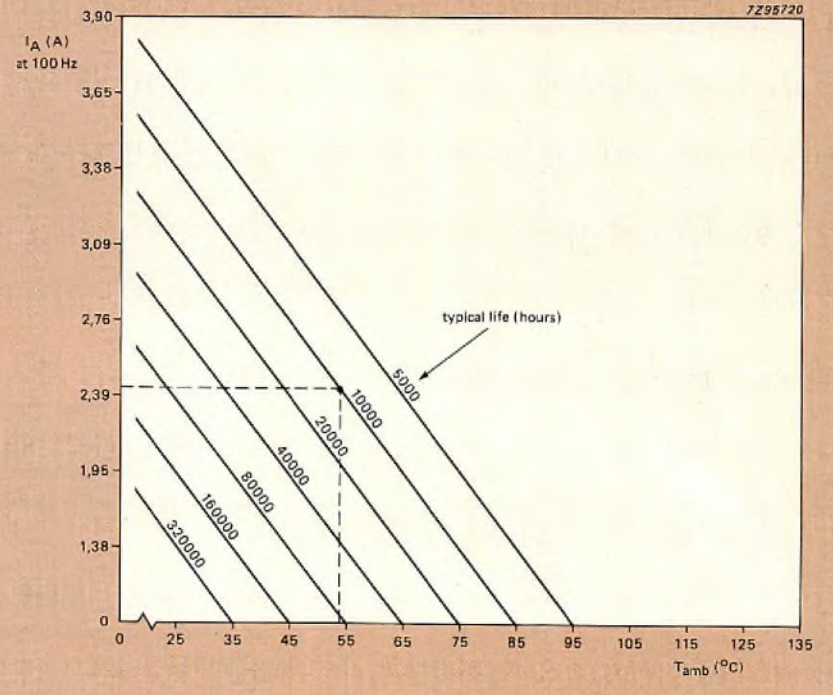
Life-test curves of some typical capacitors from the 2222 118 ..... range are shown in Fig.6.

Based on statistical evaluation of life-test data, we know that the specified guaranteed life is 2000 h at 125 °C (or 500 h at 150 °C).

These curves show that the typical life is well above the specified life, since the practical end-of-life can be set where ESR or impedance have increased to approximately 3 times their initial level. This gives a typical life of greater than 6000 hours at 125 °C or greater than 2000 hours at 150 °C. Because of the limitations set by the electrolyte breakdown voltage, the higher-voltage capacitors cannot be used reliably at 150 °C. In fact, 100 V is the highest recommended rated voltage at 150 °C whereas rated voltages up to 250 V can be reliably used at 125 °C.

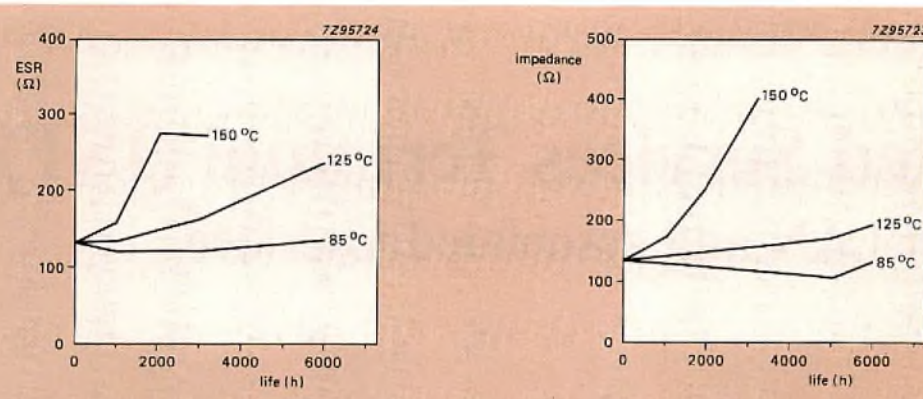


(a) Typical life expectancy of a 4700 μF, 16 V, high-temperature electrolytic capacitor type 2222 118 15472 (18 mm diameter × 40 mm).

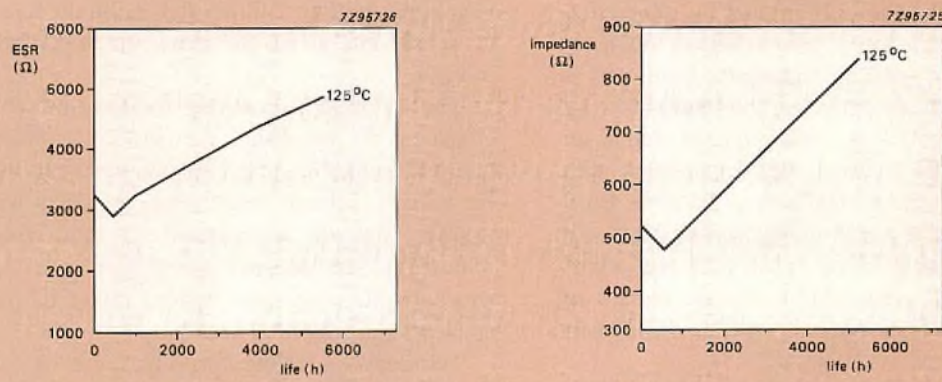


(b) Typical life expectancy of a 4700 μF, 16 V, standard electrolytic capacitor type 2222 021 15472 (18 mm diameter × 30 mm).

Fig.5 Typical life expectancy comparisons between high-temperature and standard electrolytic capacitors of the same nominal capacitance and rated voltage.



(a) Curves of ESR (Ω) at 100 Hz and impedance (Ω) at 10 kHz against life (h) at temperatures of 85 °C, 125 °C and 150 °C for a 2200 μF, 40 V capacitor type 2222 118 .7222 (21 mm diameter × 40 mm).



(b) Curves of ESR (Ω) at 100 Hz and impedance (Ω) at 100 kHz against life (h) at a temperature of 125 °C for a 15 μF, 200 V capacitor type 2222 118 92159 (10 mm diameter × 30 mm).

Fig.6 Typical life-test-curves.

APPLICATIONS

High-temperature electrolytic capacitors are used in three main application areas:

- where ambient temperatures are high, for example in 'under-the-bonnet' automotive systems;
- where high ripple currents are likely to occur at high ambient temperatures, for example as input capacitors in SMPS. This is because the high ripple current heats up the capacitor internally. Since the 2222 118 ..... range of high-temperature electrolytic capacitors goes up to 200 V rated voltage they can be used as input capacitors for SMPS applications. Additionally, their high ripple current capability is advantageous in high-performance SMPS applications. For multiple-mains input applications two 200 V capacitors in series could be used in a voltage-doubler circuit;
- where extra-long life is required at lower ambient temperatures, for instance in the electronic ballast circuit of a fluorescent lamp, where 5 to 10 years' useful life would be expected.

REFERENCE

OTTEN, A and SLAKHORST, J., "Recent developments in wet aluminium electrolytics", Electronic Components and Applications, Vol.5, No.4, Sept.1983, also available as an offprint: Philips Elcoma Technical Publication 119, ordering code 9398 043 80011.

Integrated Services Terminal (IST) Bus
the low-cost LAN and associated interface

RENÉ KOHLMAN

The requirements of modern data, voice and video communications have made increasingly greater demands on existing telephone networks which can only be met by using completely digital systems. This will require extensive modification and replacement of existing equipment so that it is vital to have international agreement on the standards to be used. At present the CCITT is attempting to define an Integrated Services Digital Network (ISDN) together with the transmission and interface standards to be used. Until agreement is reached most telephone subscriber lines will remain analog and business users, faced with the urgent needs for efficient data communications, are forced to install Local Area Networks that are separate from their in-house telephone systems.

The IST-bus provides a low cost, ISDN-compatible, solution to this office communications problem by allowing voice, data and text services to be integrated and transmitted down the same pair of twisted wires. The IST-bus can be used to simultaneously send, for example, computer, telephone, remote control and facsimile data. An example of an IST-bus office communications system is illustrated in Fig.1.

The IST-bus is a simple twisted-pair of wires with a characteristic impedance between 75 Ω and 150 Ω and in many cases existing telephone wiring can be used. Assuming the wire is correctly terminated, the delay will be less than 3000 ns and the attenuation no more than 6 dB. This represents a considerable saving over Local Area Networks which require expensive coaxial cables in addition to the conventional telephone wiring.

Terminals, including telephones, can be connected via a single-chip IST-bus interface (IBI) at any point along the bus by simply making tap points onto the two wires. The only limitation is that terminals must be at least 2 metres

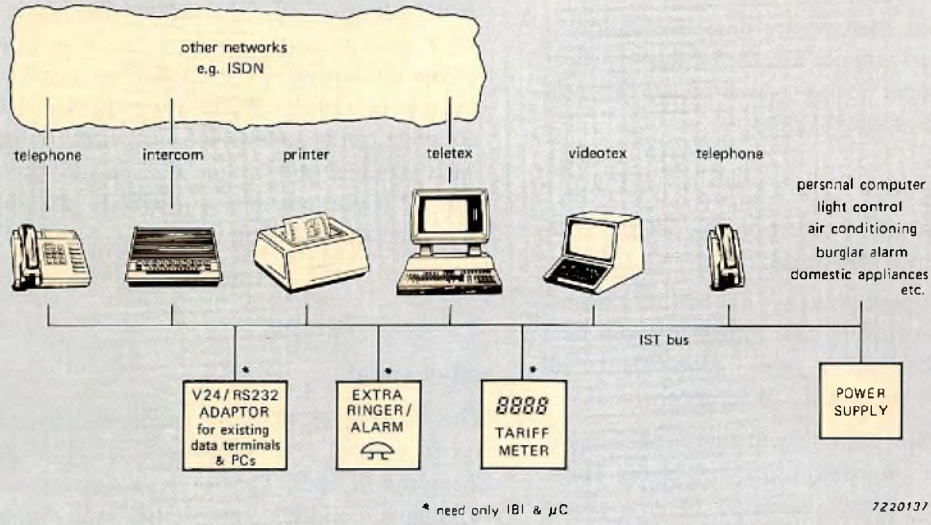


Fig.1 IST-Bus used in an office communications system

apart and must be connected to the bus by no more than 5 metres of wire. Up to 31 connections can be made to the same IST-bus which can be up to at least 300 metres long. The IST-bus can be used as a simple stand-alone full digital network or it can be part of larger communications networks. For example:

- Several IST-bus systems (sections) can be connected via a PCM-30 switch.
- The IST-bus can be linked to other communications networks by using one or more suitable "gateways" (or terminals with gateway functions).
- As the IST-bus is fully ISDN compatible, connections to new ISDN public or private exchanges can easily be made via the "S" or "U" reference points.
- It is even possible to construct a gateway to existing analog exchanges.

All these factors make the IST-bus applicable to both the present transition period systems and to future full ISDN systems.

As the majority of present inter-office transmissions are voice (and this is likely to remain the case for some considerable time) the IST-bus transmission capability has been optimised for 64 kbit/s transmissions which conform to the CCITT PCM transmission standard. By using a time-division multiplex system the bus can carry 8 kHz sampled digitized voice and/or 64 kbit/s data signals in eight half-duplex channels (b1-b8, Fig.2). In addition, a 64 kbit/s packed-switched half-duplex (bd) channel provides system control, signalling and transmission for packet data. Up to eight terminals can communicate simultaneously in the b1-b8 channels while all 31 terminals are exchanging packet data in the bd-channel.

The main features of the IST-bus are:

- Fully integrated simultaneous transmission of voice, text, and image data.
- Up to at least 300 metres long using a low-cost twisted-pair of wires.
- Simple, inexpensive installation of up to 31 terminals at any point on the bus.
- Eight 64 kbit/s circuit-switched channels optimised for voice and data communications.
- One 64 kbit/s packet-switched channel provides full layer 1* and layer 2* protocol with error-free transmission of data packets and flow control. The access is via an improved CSMA/CD protocol which guarantees access even under 100% load conditions.
- Easy interconnection and synchronization with other IST-buses/networks. The IST-bus is made fully ISDN-compatible by the use of an 8 kHz synchronized frame, (which can be externally synchronized), and 64 kbit/s channels. It also allows simple interfacing to the ISDN "S" or "U" reference points in gateway applications.
- One integrated circuit (IBI; PCB2310) provides full layer 1 and layer 2 functions for the bd-channel and interfaces with the Terminal Highway (THW), the Subscriber Line Data bus (SLD) and a PCB80C51-compatible microcontroller I/O port. The circuit is completely controllable via instructions (commands) through the microcontroller I/O port.
- AMI transmission code allows phantom power to be distributed to terminals via the single twisted-pair wires of the bus.

* As specified by the ISO in their Open System Interconnection (OSI) model.

TRANSMISSION ALONG THE IST-BUS

The nine communications channels are time-division multiplexed into 8 kHz (125 μS) frames together with a synchronization, or Frame channel, giving a total of ten channels and a transmission speed of 1,024 Mbit/s.

The ten channels are:

- One 32 kbit/s F-channel for synchronizing all the connected terminals to the 8 kHz frame.
- One 64 kbit/s half-duplex packet-switched (bd) channel which can transmit signalling (s), control (c) and data (d) packets. This channel is *freely* accessible to all terminals by means of the CSMA/CD access protocol.
- Eight 64 kbit/s half-duplex circuit-switched PCM channels (b-channels 1-8) for encoded voice and data. These channels can also be *freely* allocated to any of the terminals connected to the bus via the access mechanism of the bd-channel and are also suitable for real-time applications such as process control.

Each channel is preceded by a bit which indicates if the channel is occupied. (If the status of this bit is logic "1" then the channel is occupied).

The frame structure is illustrated in Fig.2. The initial 5-bit pattern is fixed. The first bit is the occupied signal and the next four bits are the frame signal. Due to line delays, a four bit shift in the b1-b8 channels is allowed and half a bit is used for channel separation. (The channel separation between the F and b1 and between the b8 and F channels is 1 bit).

The code used for the transmission of data along the bus is the Alternate Mark Inversion (AMI) system where logical "1"s are alternately coded as equal positive and negative pulses and logical "0"s result in no signal on the line. The bit rate is 1 Mbit/s. Using this code means that transformer coupling can be used which ensures the galvanic isolation of each terminal and, as the d.c. power spectrum of AMI is zero, it is also possible to distribute phantom power across the interface and along the bus.

bd-channel

The bd-channel transfers packet-switched, signalling ("s" type), control ("c" type) and data ("d" type), messages along the IST-bus. The "s" type messages are used for call routing and address one specific, or all terminals (broadcast messages). The "c" type messages are used to control the F and b-channels and address all terminals.

Error-free transmissions in this channel are assured by the use of a single-frame HDLC-like protocol which detects transmission errors with a Cyclic Redundancy Check (CRC) and then corrects them by re-transmission of the packet. Flow control of packets is also possible because, if a packet is incorrectly received or if the receiver is unable to handle it (e.g. due to receiving packet memory not being free), the packet is rejected immediately after the transmission. It must then be re-transmitted by means of the IST-bus interface circuit and/or the higher layer control software of the terminal.

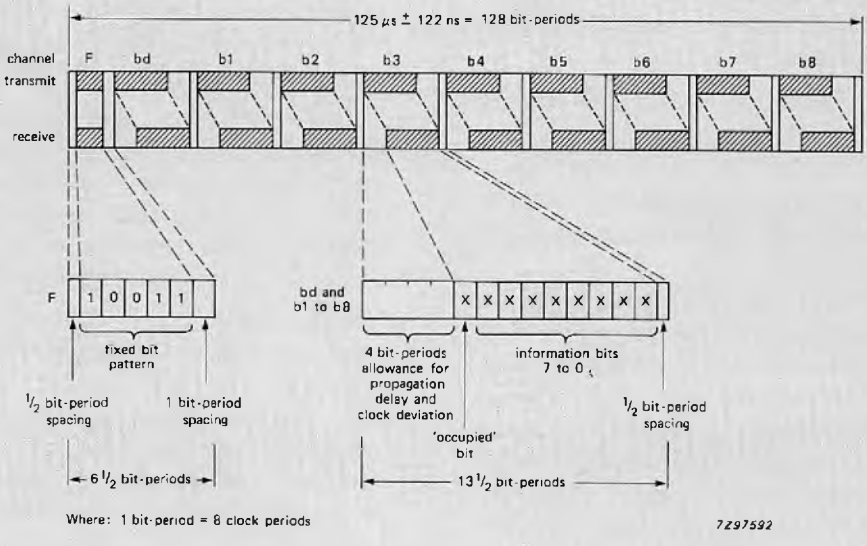


Fig.2 Frame structure

A packet will be rejected after two frames (2 x 125 μs) if:

– the calculated CRC at the receiver differs from the actual received CRC

or

– a message cannot be received due to pending messages

or

– a collision has occurred (see following paragraphs).

The bd-channel access is based on slotted CSMA/CD (Carrier-Sense Multiple-Access with Collision Detection).

A terminal can start to transmit when the channel is detected as being free (i.e. occupied bit is logic "0"). However, when two or more terminals start to transmit at the same time, or within the propagation time of the bus, a "collision" occurs and the messages will be corrupt.

To shorten the average bus occupation time during collisions, an exclusive-OR system has been implemented between the transmitter and the receiver. This facilitates immediate collision detection without having to wait for the CRC errors at the end of the message. The AMI transmission code used means that with the exclusive-OR circuit, when a transmitter compares the transmitted and received signals, the positive or negative levels of a logic "1" will always override the "no signal" condition of a logic "0" and any differences will be immediately detected.

When a terminal discovers that a collision has occurred it transmits all "1"s in the next frame, to stop ongoing messages, followed by a reject message. This process clears the channel and greatly increases the traffic capacity of the bd-channel during busy hour conditions by ensuring that access is maintained, even under 100% load.

The access priority is: Control packets have priority over signalling packets, and signalling packets have priority over "normal" data packets. To guarantee fair access, previously collided messages have priority over new messages. The complete priority scheme for messages in the bd-channel is thus:

1. Collided control/signalling messages.
2. New control/signalling messages.
3. Collided data messages.
4. New data messages.

b-channels

The b-channels provide eight channels for the exchange of circuit-switched data via the IST-bus.

Within the b-channels, the access protocol is fully decentralized and there is no network manager. Any terminal can request, and then gain access to, a free b-channel.

To allow the use of enquiry or call transfer facilities between terminals it is possible for a terminal to request access to a specific channel as soon as it is free. The requested channel is seen to be free as soon as its occupied bit is logic "0" for one frame. This channel will then be accessed by the terminal to which the equiry or call transfer is intended.

THE IST-BUS INTERFACE CIRCUIT

Cost effectiveness of the IST-bus is maintained in the simple interface which connects each terminal to the bus. This consists of one IST-bus Interface (IBI) IC PCB2310, a simple matching transformer and a length of twin connecting wire.

The PCB2310 is an intelligent CMOS VLSI circuit which forms the interface between the IST-bus and the internal terminal interfaces formed by the 2 Mbit/s Terminal Highway (THW), the Subscriber Line Data (SLD) bus and an 8-bit multiplexed address/data microcontroller I/O port. The chip has an internal 8 kHz clock which be can synchronized to an external source. The IBI can access any number of free circuit-switched channels on the IST-bus (b1 to b8). It also relieves the terminal controller from the layer 1 and layer 2 functions for the packet-switched (bd) channel. An example of a typical voice terminal configuration is shown in Fig.3.

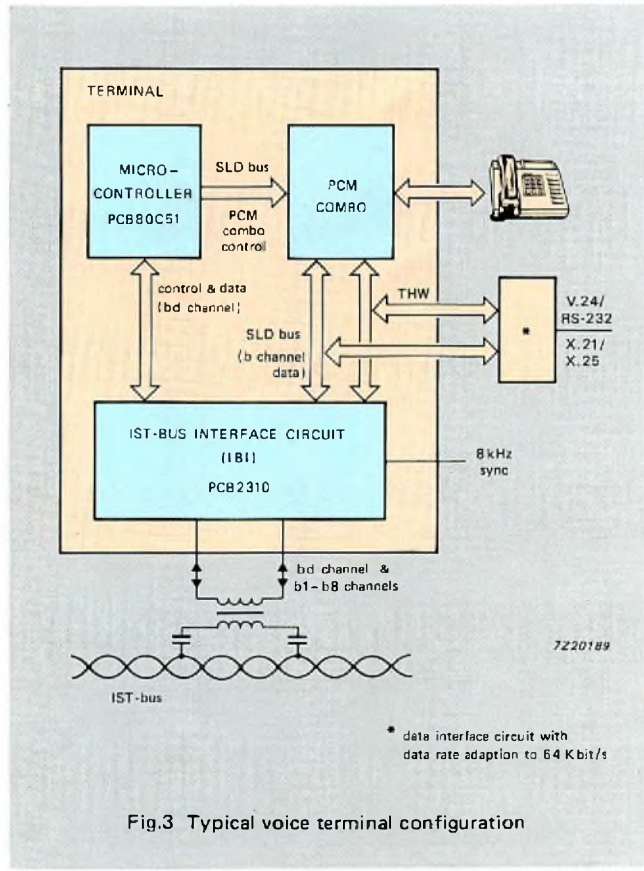


Fig.3 Typical voice terminal configuration

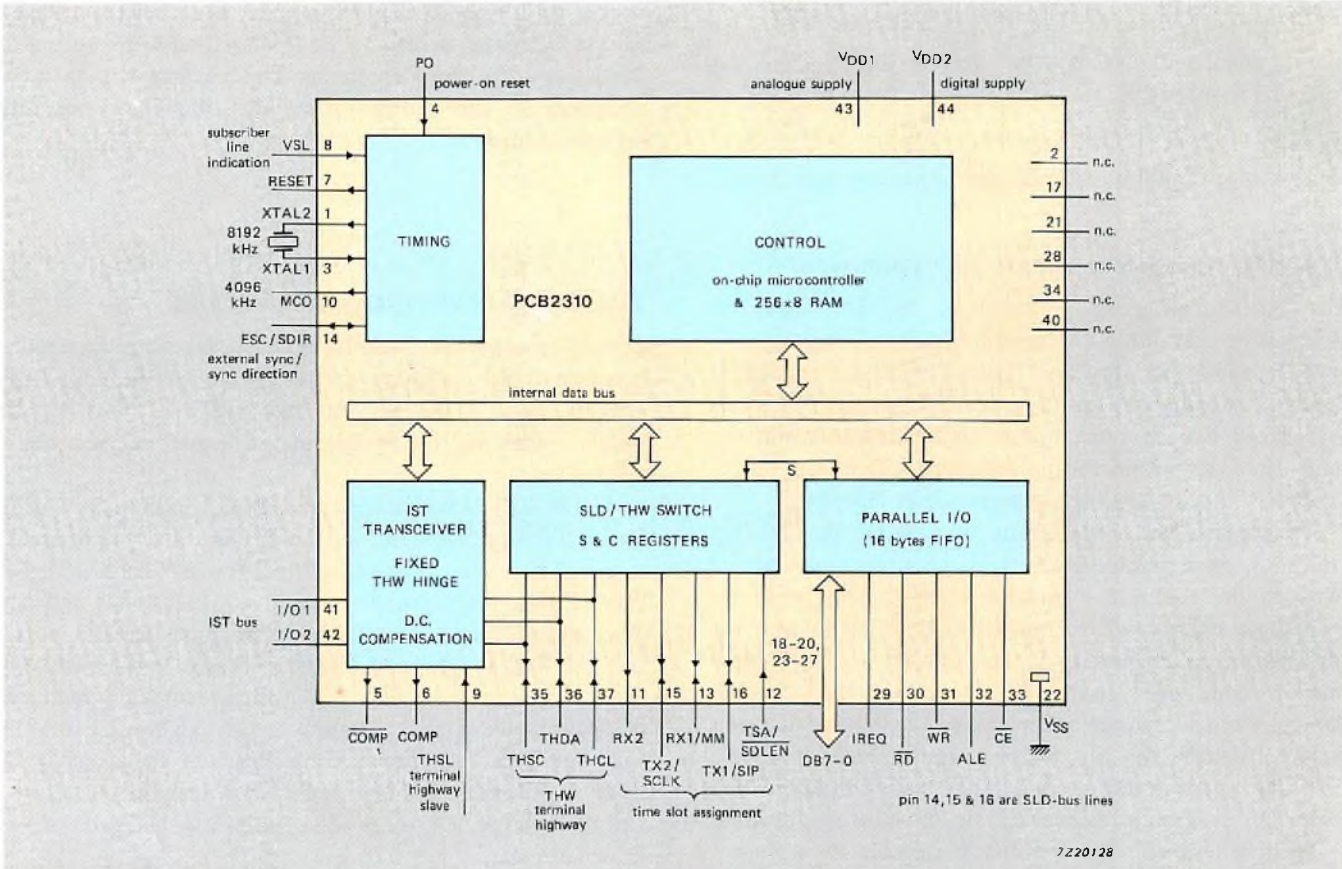


Fig.4 IBI block diagram

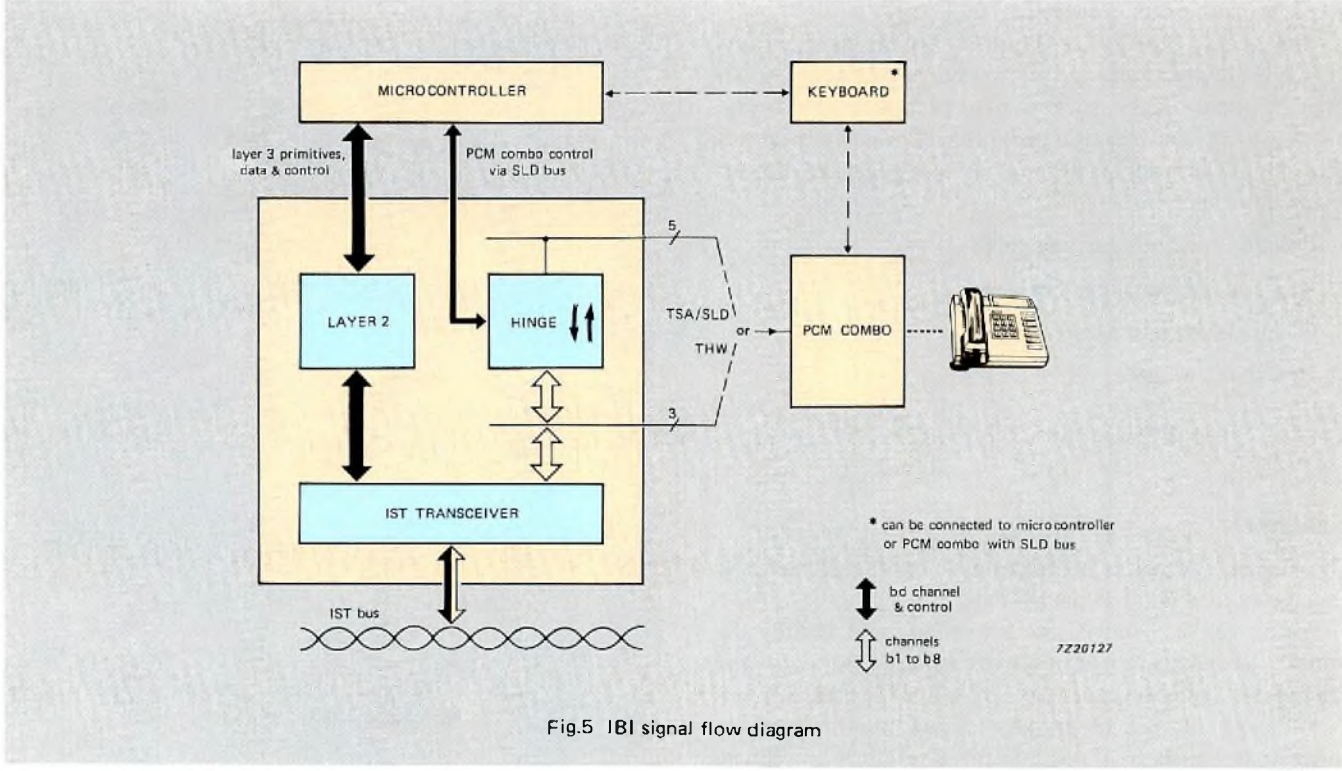


Fig.5 IBI signal flow diagram

Figure 4 is a block diagram of the PCB2310 (IBI) and Fig.5 is a signal flow diagram. The circuit-switched (b) channels on the IST-bus are mapped onto THW time-slots and/or are switched to the SLD bus B_1 and B_2 channels. The packet switched (bd) channel is routed through the layer 2 entity to the parallel I/O port.

The IBI provides:

- Bus power-on procedures.
- 8 kHz generation/locking. The circuit has an on-chip 8192 kHz crystal-controlled clock generator and a 4096 kHz clock output for peripherals. The IBI can also be externally synchronized for gateway applications.
- IST-bus address recognition.
- Channel status detection.
- Connection/disconnection of circuit-switched channels.
- Packet-switched message transfer including error-check/re-transmission.
- Multiplexing/demultiplexing of signalling and data packets.

Terminal Highway (THW)

The THW is a full-duplex, 3-wire, 2,048 MHz, 32-channel PCM highway which is normally used to connect to a PCM combo (voice signal encoder/decoder and band limiting filters) or a b-channel data terminal. The eight circuit-switched b-channels and the packet-switched bd-channel on the IST-bus are mapped in fixed time-slots on the THW. The THW offers 32 time-slots, 17 of which are used to transmit and receive IST-bus channels, the remaining time slots are free for other 64 kbit/s switching applications.

The THW interface has three modes of operation:

- The master mode for normal operation.
- The slave mode for instances when several IBIs are connected together.
- The monitor mode to allow easy monitoring of the bd-channel (for testing and system development).

The master mode is the normal operating mode for the THW. In this mode the IBI provides the THW bus with a 2048 kHz clock output (THCL; IBI pin 37) and an 8 kHz synchronization output (THSC; IBI pin 35).

The THW monitor mode can be used to monitor the bd-channel. In this mode, the IBI provides the Time Slot Assignment (TSA) signal on the 8 kHz synchronization output (THSC). If the bd-channel is occupied the TSA pulse is extended with a strobe signal for the time-slot that is mapped to the bd-channel. By this means the bd-channel information can be easily monitored using a PC or dedicated analyzing equipment connected, with a minimum of extra hardware, to the THW of the IBI.

When several IST-buses are connected together (e.g. by a PCM-30 switch) to form a "multi-section" system (Fig.6) the THW slave mode is used by all terminals except the network master. In this mode the terminal highway synchronization input (IBI pin 35) and the clock input (IBI pin 37) are provided by the network master. One IBI provides the 2 MHz THW clock and will also be master of its IST-bus section. The other IBIs in the section-switch will be slaves of the THW but masters of their own section.

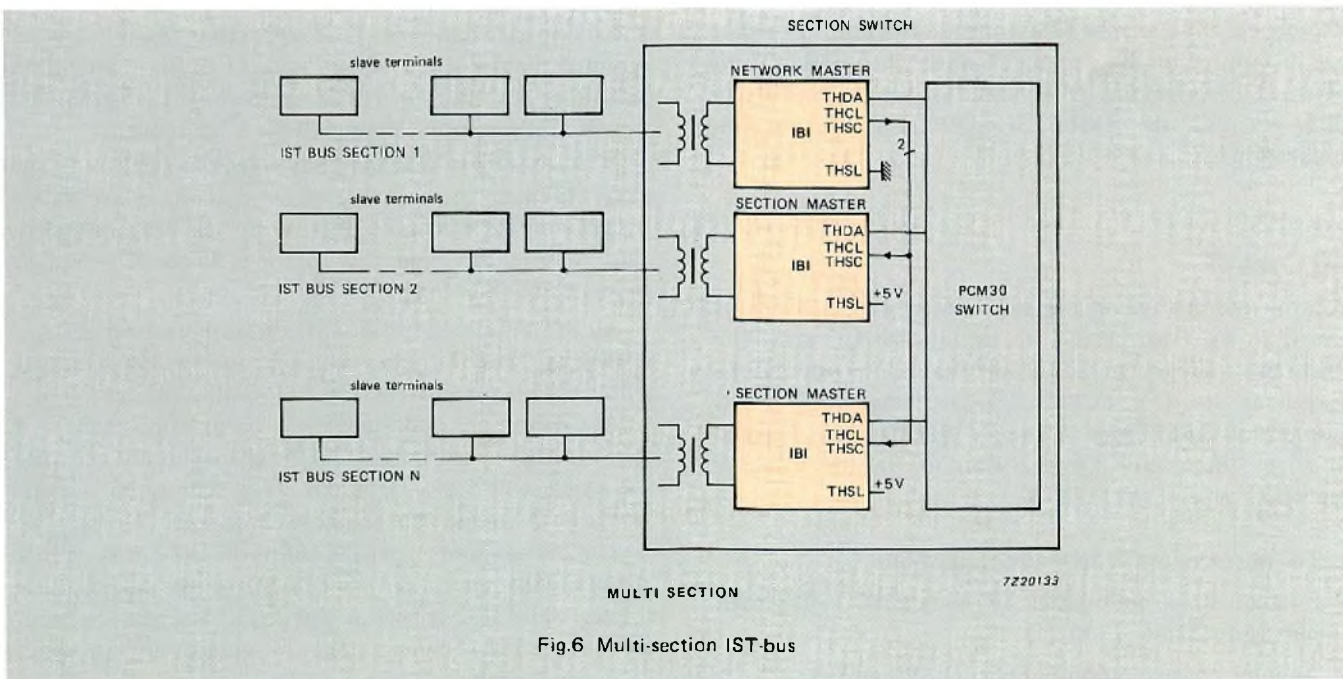


Fig.6 Multi-section IST-bus

Subscriber Line Data (SLD) Bus

The 3-wire bidirectional SLD-bus is used to connect B-channel devices such as interfaces to other networks or PCM combos like the PCB2060 (signal processing codec filter). It carries two 64 kbit/s circuit-switched data (B) channels, one 64 kbit/s control (C) channel and one 64 kbit/s signalling (S) channel in each direction. The microcontroller can access the C and S channels on the SLD-bus through the I/O port.

The B_1 and B_2 channels of the SLD-bus can be switched to any of the THW time-slots by the SLD switch. In this way it is possible to map IST channels b1-b8 via the THW onto the SLD B_1 or B_2 channels, and vice versa. The selection of channels is programmable via the microcontroller I/O port. This process is shown in the IBI Signal Flow Diagram (Fig.5).

The IBI can be either master or slave on the SLD-bus. In the case where an IBI is connected to another network, the SLD slave mode is selected and the other network controls the SLD-bus. In all other cases where the SLD is used to connect a codec or other peripheral devices, the SLD master mode is selected.

During the SLD master mode, IBI provides the SLD-bus with the 512 kHz clock signal (SCLK; IBI pin 15) and the 8 kHz synchronization (ESC/SDIR; IBI pin 14). In this mode the IBI controls the SLD-bus and thus the peripheral devices connected to it.

The B_1, B_2, C and S channels are transmitted by the IBI when ESC/SDIR is HIGH. When ESC/SDIR is LOW, the SIP output pin (IBI pin 16) is high-impedance and can receive data. A microcontroller can control the duplex C channel via the control path of the IBI.

In the SLD slave mode, the IBI acts in a similar way to an SLD peripheral. The S and C channel outputs are high impedance, and it can be programmed to transmit on either one or both of the B_1 and B_2 channels when ESC/SDIR is LOW. If, however, the IBI is master of the IST-bus it synchronizes with the 8 kHz ESC/SDIR signal (in network applications).

IBI Control

Control information on the packet-switched bd-channel is routed to the 8-bit parallel microcontroller I/O port. The IBI is also completely controllable via this interface and the microcontroller (e.g. PCB80C51) can access the S and C channels of the SLD-bus. A 16-bit FIFO register is included to adapt the microcontroller interface to the 64 kbit/s processing capability of the IBI.

The microcontroller I/O port consists of:

- 8 data/address multiplexed I/O lines (DB7 to DB0; IBI pins 18 to 20 and 23 to 27).
- An interrupt request output ($\overline{\text{IREQ}}$; IBI pin 29).
- A read input ($\overline{\text{RD}}$; IBI pin 30).
- A write input ($\overline{\text{WR}}$; IBI pin 31).
- A chip enable input ($\overline{\text{CE}}$; IBI pin 33).
- An address latch enable input (ALE; IBI pin 32).

When ALE is HIGH and $\overline{\text{CE}}$ is LOW, data on the DB7-0 I/O port is latched into the address latch. The IBI then writes the data byte from the data bus I/O port into the addressed register.

Timing

The source of the IBI timing is an 8192 kHz ± 100 ppm crystal connected to pins 1 and 3. An external clock output is available on pin 1. When using an external clock generator, pin 1 is not connected and the clock input is via pin 3.

THE IST-BUS IN OPERATION

After switch-on, one of the terminals will transmit the fixed bit pattern "10011" in the F-channel, where the initial "1" is the occupied bit and "0011" is the frame signal. This terminal will thus become the master controlling the 8 kHz synchronization of the IST-bus while the other terminals will be slaves. The terminal which becomes the master is decided by a "master-slave arbitration" algorithm and if any master fails, the next in line in the algorithm will automatically take over. In theory, any terminal can become the master of the F-channel; however, if a gateway, or gateway terminal, to another 8 kHz synchronous network is connected to the bus and it is not the master, it will transmit a control message called Transfer Of Master (TOM) in the bd-channel. The current master will then cease transmission and the master-slave procedure will restart. As this type of terminal always has a higher priority in the master-slave arbitration algorithm it will always become the master and thus ensure synchronization with the other network.

It is possible to connect more than one gateway to the same IST-bus. In this case the master-slave arbitration occurs only between the IBIs of the gateway terminals, thus making sure that one of these terminals is always master of the F-channel.

All IST slaves will synchronize on the F-channel as transmitted by the IST master which in turn will synchronize with the 8 kHz external sync at ESC/SDIR (IBI pin 14).

An IBI can only transmit in the bd or b1-b8 channels if it is correctly synchronized and the channel is not occupied (occupied bit = logic "0"). To be synchronized it must recognise the frame signal in three consecutive frames.

The output/input from the IBI to the IST-bus is via I/01 and I/02 (IBI pin 41 and pin 42). I/01 drives the bus transformer while I/02 is held at $V_{DD}/2$. I/01 is also the input for the receiver comparator, the comparator reference voltage being driven from pin 42.

If any terminal wants access to a b-channel, the command Fetch Free Channel (FFC) is issued by the terminal's microcontroller to the IBI which then transmits an occupy channel (OCP) control message in the bd-channel. After successful transfer of this message, the IBI can access a free b-channel. A channel is free if the occupied bit is at logic "0" for at least two consecutive frames after the OCP message has been transferred. When a channel is occupied the IBI sends a CHannel Connected (CHC) primitive (primitive = interface signal) followed by a parameter (indicating which channel is occupied) to the microcontroller. The data, or digitized voice, signal in the THW time-slot will then be transmitted in the occupied b-channel. On completion, the command Release CHannel (RCH) followed by the channel parameter will be sent from the microcontroller to the IBI to release the channel(s).

The transfer of calls from one terminal to another is possible after the first terminal sends a message (via the bd-channel) to the other terminal to take over the call. The second terminal will then issue the command Occupy After Release (OAR) to its IBI followed by a parameter indicating the b-channel occupied by the call and will also acknowledge (via the bd-channel) that it will take over the call. The specific channel requested will be occupied immediately after it has been released by the first terminal (sensed by the occupied bit being logic "0" for one frame). The call is thus transferred.

When a terminal wants to communicate with another network via a gateway, it can request the IST-bus to synchronize with the external 8 kHz source of that network. The procedure is initiated by an External Sync Request (ESR) primitive . If the terminal is not the master, the IBI will transmit a Slave Asks Synchronization (SAS) control message in the bd-channel. In a gateway terminal, the IBI will issue an External Sync Wanted (ESW) indication upon receipt of a SAS message. If the external synchronization is established, the SynChronization On (SCO) control message will be sent in the bd-channel and, on receipt, an External Sync On (ESO) confirmation is given by the IBI.

To end synchronization with the external source the gateway terminal issues a Release External Sync (RES) request to the IBI. The Ask to Finish Synchronization (AFS) control message is then sent in the bd-channel and all terminals receive a Release of external Synchronization will Proceed (RSP) indication. If there is no reply from the other terminals connected to the IST-bus within 8 seconds, the master will release the external synchronization.

To disconnect from the bus, a terminal generates a TRansfer Of Master (TRM) primitive to the IBI to release the F-channel and no longer takes part in the master/slave arbitration. Then, after all the b-channels are released, the F-channel is switched off and the terminal can disconnect from the bus. If the terminal was the master this is indicated by a Transfer of Master Proceeding (TRM) bus-down primitive to all terminals. If it was a slave a Transfer of Master Finished (TMF) bus-up primitive indicates that another terminal is the master on the IST-bus. This procedure is intended to prevent any loss of circuit-switched data within the b-channels.

EXAMPLES OF IST-BUS APPLICATIONS

Figures 7, 8 and 9 provide examples of IST-bus applications. With reference to Fig.9, the IOM interface is a local, point-to-point, duplex communication channel for interconnecting layer 1† ICs to layer 1† or layer 2† ICs in ISDN networks. This provides the flexibility to connect a wide variety of subscriber terminals to telecommunication networks meeting present and future ISDN specifications. It makes it easy to meet the requirements of any future standard because the layer 1 IC can be modified without influencing the function of the layer 2 IC to which it is connected via the IOM* interface.

† As specified by the ISO in their Open System Interconnection (OSI) model.

* Philips Elcoma/Siemens ISDN-Orientated Modular architecture.

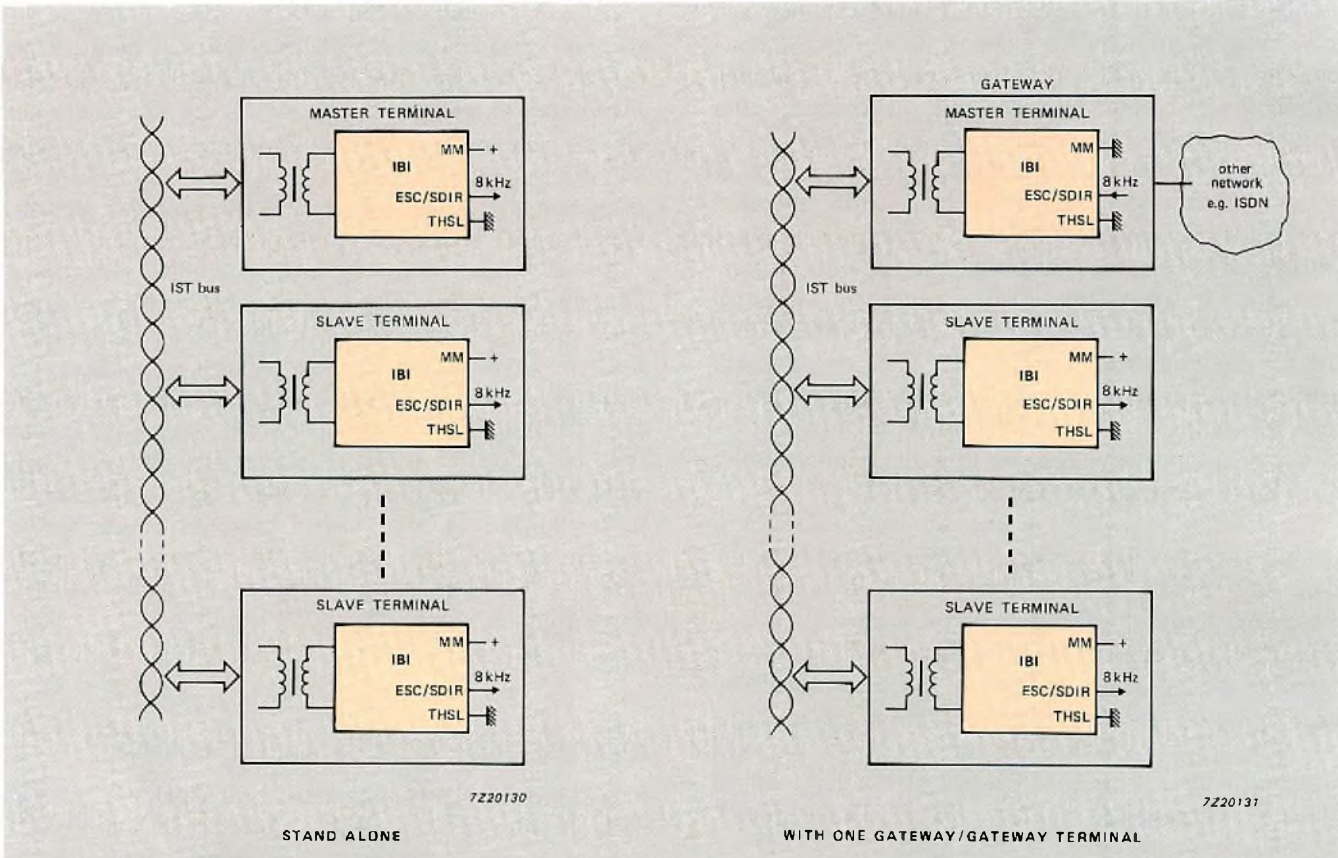


Fig.7 Stand-alone system and one gateway system. For the stand-alone IST-bus, the master terminal provides the 8 kHz synchronization. For the IST-bus with a gateway terminal, the 8 kHz synchronization is provided by the external network

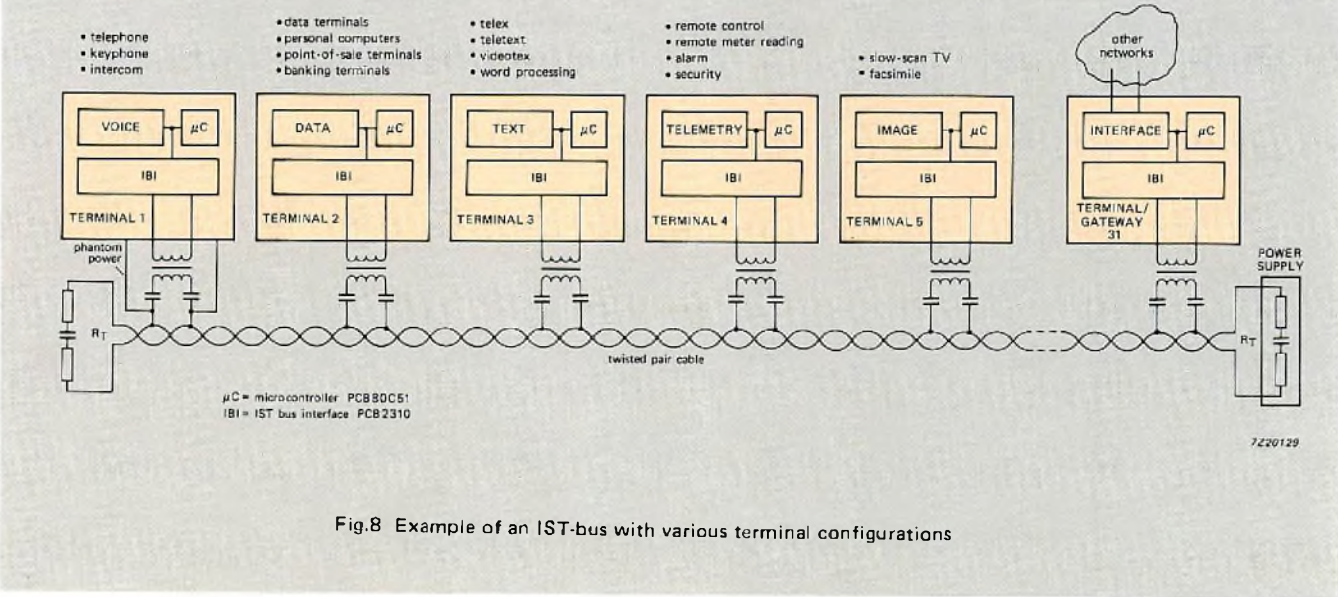


Fig.8 Example of an IST-bus with various terminal configurations

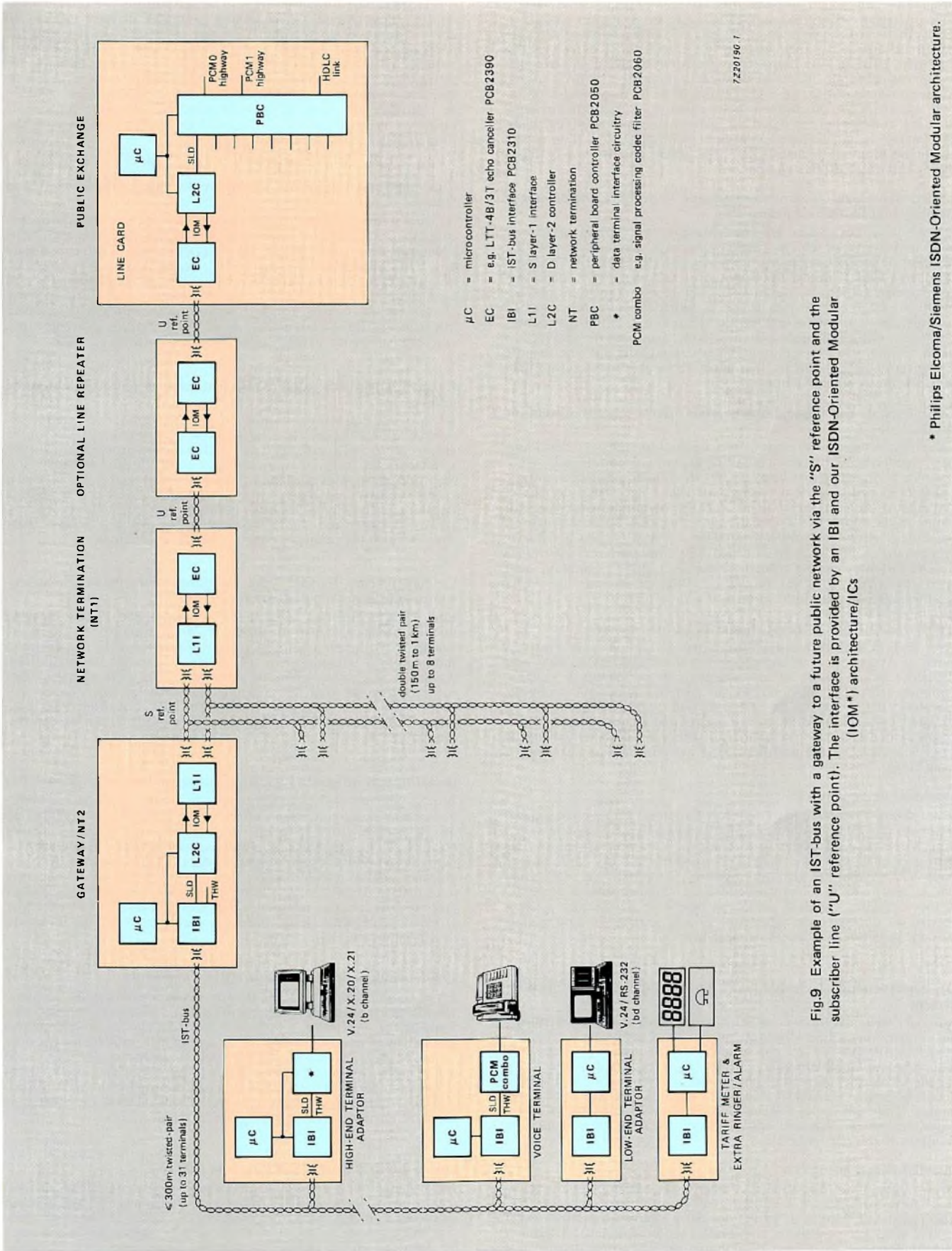


Fig.9 Example of an IST-bus with a gateway to a future public network via the "S" reference point and the subscriber line ("U" reference point). The interface is provided by an IBI and our ISDN-Oriented Modular (IOM®) architecture/ICs

® Philips Elcoma/Siemens ISDN-Oriented Modular architecture.

Un convertisseur analogique-numérique 12 bits ultra-rapide, basé sur deux séquenceurs logiques programmables par l'utilisateur

Ce convertisseur analogique-numérique est équipé de deux séquenceurs logiques type PLS 179 de notre famille de dispositifs logiques programmables (PLD), programmés et interconnectés pour constituer un registre d'approximations successives (SAR), un compteur-décompteur et un générateur de signaux d'horloge biphasé. Un convertisseur numérique-analogique et un comparateur perçoivent les disparités entre le signal numérique fourni et le signal d'entrée analogique et provoque l'accroissement ou la diminution du SAR jusqu'à obtention de la parité. Le SAR devient alors un compteur-décompteur et augmente ou diminue pour suivre les variations du signal d'entrée analogique. Le signal de sortie numérique peut également être maintenu indéfiniment constant; on dispose alors d'un échantillonneur-bloqueur à niveau de sortie stable, insensible à la dégradation due aux fuites de charge.

Les condensateurs microparés-céramique – des produits de grande fiabilité dont l'avenir est prometteur

On ne peut encapsuler les condensateurs microparés céramique comme les condensateurs conventionnels à connexions pour les protéger de la pénétration de l'humidité, ce qui explique que certains fabricants aient éprouvé de nombreuses défaillances précoces dues au claquage sous basse tension. Ces défaillances sont dues uniquement à une mauvaise qualité de la fabrication. A condition de prendre des précautions suffisantes, la fiabilité de ces condensateurs peut être considérée comme irréprochable. Suite aux progrès récents de la technologie des céramiques, ces composants ont une fiabilité à long terme exceptionnelle, leur durée de vie atteignant des dizaines et même des centaines d'années.

Générateur de son stéréophonique pour effects sonores et musique synthétique

Un circuit intégré générateur de son stéréophonique a été développé pour améliorer les niveaux actuels de la communication audio entre ordinateur et utilisateur. Il est capable de simuler des instruments de musique et de produire des sons pour jeux vidéo (salles de jeux et ordinateurs domestiques). Il est capable de produire des accords complets et toutes les notes dans une gamme de 8 octaves. Le générateur peut être connecté directement à la plupart des microcontrôleurs 8 bits et nécessite peu de composants extérieurs. En dehors du marché de l'ordinateur domestique, le générateur peut servir utilement dans les modèles réduits de chemins de fer et d'automobiles et dans les dispositifs d'alarme sonore.

Un microcontrôleur ultra-rapide à architecture Harvard

Avec trois bus parallèles, une technologie ECL et un cycle d'instructions de 100 ns, le nouveau microcontrôleur 8X401A satisfait sans difficulté les impératifs les plus exigeants en traitement de signaux, communication et commande de périphériques, par exemple. Outre sa grande rapidité, le 8X401A présente d'autres avantages sur ses prédécesseurs: aptitude à traiter entièrement aussi bien les interruptions que les sous-programmes, quatre nouvelles instructions de branchement et de retour et les opérations arithmétiques et logiques supplémentaires.

Décodeur de signaux VPS

Etant donné l'impossibilité de prévoir les retards ou les changements d'horaire, l'utilisateur d'un magnétoscope classique risque de ne pas enregistrer ce qu'il désire. C'est pourquoi les organismes de télédiffusion européens ont décidé d'incorporer à leurs émissions un code VPS (Video Programming System) permettant l'identification par le récepteur de l'heure effective de commencement et de fin d'une émission. L'article décrit un ensemble de circuits intégrés servant au décodage du signal VPS et à la commande d'un magnétoscope par l'intermédiaire du simple bus I^2C.

Des condensateurs électrolytiques à haute température de fonctionnement

Au cours de la décennie écoulée, la température de fonctionnement des condensateurs électrolytiques non solides a doublé pour atteindre actuellement 125 °C, ce qui a ouvert de nouvelles perspectives d'applications en électronique militaire, dans les systèmes pour automobile et dans les alimentations à découpage, par exemple. L'article décrit la gamme 2222 118.. de condensateurs électrolytiques pour hautes températures et expose leurs critères de conception. Il indique également comment calculer l'espérance de vie et donne les résultats de tests de longévité.

Bus IST compatible RNIS

Avec l'équipement électronique moderne de bureau, la communication entre ordinateurs et autres postes terminaux nécessite fréquemment des réseaux de câbles coaxiaux séparés. Une solution est le bus IST, qui permet de transmettre simultanément les signaux téléphoniques et les signaux de données sur une paire torsadée peu coûteuse, par l'intermédiaire d'un simple circuit d'interface. L'article décrit le fonctionnement du bus IST et du circuit intégré qui l'accompagne, et donne des exemples d'intégration de l'IST dans des installations existantes et futures.

CAD de seguimiento de gran velocidad de 12 bitios con dos ASIC programables

Lleva dos secuenciadores lógicos del tipo PLS179 de nuestra gama de dispositivos lógicos programables (PLD) programados y conectados entre sí para formar un registro de aproximación sucesiva (SAR) de 12 bitios, contador alternativo y generador de reloj bifásico. El convertidor y el comparador detectan si la señal de salida digital coincide con la de entrada analógica y hace que el SAR aumente o reduzca hasta lograrse la paridad y convertirse entonces en contador alternativo que aumenta o disminuye para seguir toda variación de las señales analógicas de entrada. La señal de salida digital también se mantiene constante indefinidamente, para facilitar función de muestreo y retención cuya intensidad de señal de salida es estable, sin pérdidas por causa de fugas de carga.

Condensadores cerámicos: productos de gran seguridad con gran futuro

Al igual que los dispositivos con terminales, los condensadores chip cerámicos no se pueden encapsular para protegerlos de la entrada de humedad. A resultado de ello, algunos fabricantes se han encontrado con fallos prematuros a causa de descargas a baja tensión, resultado del mal acabado, pues siempre que se ponga el debido cuidado en su fabricación, la seguridad de los condensadores cerámicos es irreprochable. Lo que es más, con los últimos avances en las técnicas cerámicas, la seguridad a largo plazo de dichos elementos es excepcional, con vidas útiles que se calculan en decenios e incluso en siglos.

Generador de sonido estereofónico para efectos sonoros y síntesis de música

Se ha perfeccionado un circuito integrado generador de sonido estereofónico para mejorar la calidad actual de la comunicación sonora entre ordenador y usuario. Los sonidos que se producen incluyen: simulación de instrumentos musicales y para juegos de ordenador. Se producen acordes musicales completos y todas las notas musicales en ocho octavas. El generador se conecta fácilmente con la mayoría de microcontroladores de 8 bits y necesita pocos elementos exteriores. Aparte del mercado de los ordenadores domésticos, el generador sirve también para trenes y coches miniatura y alarmas.

La construcción Harvard lleva los circuitos integrados de microcontrolador al mundo de la gran velocidad

Con sus tres buses en paralelo, circuitos del tipo ECL y ciclo de instrucción de 100 ns, el nuevo microcontrolador 8x401A se adapta eficazmente a las aplicaciones más exigentes, por ejemplo, tratamiento y comunicación de señales y control de periféricos. Aparte de la gran velocidad de este dispositivo, otras ventajas sobre sus predecesores son: su capacidad de negociar interrupciones y subrutinas en su totalidad, sus cuatro nuevas instrucciones para saltos y retornos y sus operaciones aritméticas y lógicas complementarias.

Decodificador integrado para sistema de programación de video (VPS)

Al no poder pronosticarse los errores de programación con los sistemas normales de grabación (VCR), existe siempre la posibilidad de que se graben partes indebidas de la misma. Por consiguiente, los responsables de las emisiones europeas han decidido introducir una clave (VPS) Video Programming System en los formatos de transmisión televisiva que se decodifica en los receptores para detectar la hora precisa de comienzo y fin del programa. El artículo describe un juego de dos circuitos integrados para descifrar la señal VPS y mandar el videomagnetófono mediante un colector intercircuito integrado de dos hilos (I^2C bus).

Condensadores electrolíticos para alta temperatura

En el transcurso de la última década, las temperaturas de funcionamiento de los condensadores electrolíticos no sólidos se han doblado, hasta llegar a su valor actual de 125 °C, lo que ha abierto nuevas posibilidades de aplicaciones en la electrónica militar, sistemas de automoción y fuentes de alimentación conmutadas, entre otros. El artículo describe la gama 2222-118... de condensadores electrolíticos de alta temperatura y trata los criterios de diseño para su funcionamiento a alta temperatura. También da el método de calcular la esperanza de vida y datos de las pruebas de vida.

Bus de terminal de servicios integrado (IST)

Los ordenadores y demás terminales de datos de una oficina electrónica moderna presentan el problema de exigir con frecuencia redes de cables coaxiales para comunicación. El bus de terminal de servicios integrado da la solución, al permitir la transmisión simultánea de datos y señales telefónicas a través de un circuito de interconexión sencillo mediante un par de hilos trenzados de bajo coste. El artículo describe el funcionamiento del bus IST y su circuito integrado de interconexión y da ejemplos de integración en sistemas existentes y futuros.

Abstracts

A high-speed 12-bit tracking ADC based on two field-programmable ASICs

In this ADC, two logic sequencers type PLS179 from our Programmable Logic Device (PLD) family are programmed and interconnected to form a 12-bit Successive Approximation Register (SAR), up/down counter and biphase clock generator. A DAC and comparator sense whether the digital output matches the analog input and causes the SAR to increment or decrement until parity is achieved. The SAR then converts into an up/down counter and increments or decrements to track any analog input variations. The digital data output can also be held constant indefinitely to provide a sample-and-hold function with a stable output level which is not subject to decay due to charge leakage.

Ceramic-chip capacitors – high rel products with a promising future

Ceramic-chip capacitors can't be encapsulated like their leaded counterparts to protect them from ingress of moisture. Some manufacturers therefore have experienced early failures due to breakdown at low voltage. These failures are purely the result of poor workmanship, and, provided care is taken in their manufacture, the reliability of ceramic chip capacitors can be considered beyond reproach. What's more, with the recent advances in ceramic technology, the long term reliability of these components is exceptional.

Stereo sound generator for sound effects and music synthesis

To improve present levels of audio communication from computer to user, a stereo sound generator IC has been developed. The sounds that can be produced include simulations of musical instruments and the sounds for arcade/home computer games. Full musical chords and all musical notes in an 8-octave range can be produced. The generator readily interfaces with most 8-bit microcontrollers and requires few external components. Outside the home-computer market, the generator can be used to good effect in model railways and cars and in audible alarms.

Harvard architecture pushes microcontroller IC into high-speed realm

With its three parallel buses, ECL-based circuitry and 100 ns instruction cycle, the new 8X401A microcontroller has no trouble filling the most demanding roles, in for example, signal processing and communication, and peripheral control. Besides the 8X401's high speed, other advantages over its predecessors are its ability to handle both interrupts and subroutines in their entirety, its four new instructions for jumps and returns and its extra arithmetic and logic operations.

Integrated video programming system (VPS) decoder

Since programme timing error cannot be predicted with conventional VCR timing systems, there is a possibility of incorrect programme material being recorded. European broadcasting authorities therefore intend to introduce a Video Programming System (VPS) code into television transmissions which will be decoded at the receiver to detect the actual start and stop times of a programme. This article describes a set of two ICs for decoding the VPS signal and controlling a VCR via the simple 2-wire inter-IC bus (I^2C bus).

High-temperature electrolytic capacitors

During the past decade the operating temperature of non-solid electrolytic capacitors has doubled to its present value of 125 °C, and this has opened up new applications in, for example, military electronics, automotive systems and SMPS. This article describes the 2222 118 ..... range of high-temperature electrolytic capacitors and discusses design criteria for high-temperature operation. It also shows how to calculate life expectancy and gives life-test data.

Integrated Services Terminal (IST) bus

A problem that has arisen with the modern electronic office is that computers and other data terminals often require separate co-axial cable networks to communicate. The IST-bus provides a solution by allowing both data and telephone signals to be transmitted simultaneously via a simple interface circuit on a low-cost pair of twisted wires. This article describes the operation of both the IST-bus and its associated interface IC, and provides examples of how IST can be integrated into existing and future systems.

Schneller nachlaufender 12 bit-Analog/Digitalwandler, basierend auf zwei feldprogrammierbaren ASICs

In diesem ADC bilden zwei Logik-Sequenzer des Typs PLS179 aus unserer Familie der integrierten Programmierbaren Logikschaltungen (PLD) ein 12 bit breites Successive-Approximation-Register (SAR) und einen Vorwärts-/Rückwärtszähler mit Zweiphasen-Taktgenerator. Ein DAC und Komparator vergleicht den digitalen Ausgangswert mit dem analogen Eingangswert und bewirkt durch Inkrement oder Dekrement im SAR, dass Gleichheit hergestellt wird. Der SAR wird dann als Vorwärts-/Rückwärtszähler geschaltet und inkrementiert oder dekrementiert zur Aufspürung von Schwankungen des analogen Eingangssignals. Der digitale Datenausgang kann auch für unbegrenzte Zeit konstant gehalten werden. Diese Möglichkeit ist eine sehr gute Abtast-/Haltefunktion mit stabilem Ausgangspegel, da die Ausgangsspannung nicht durch Leckströme abnimmt.

Keramik-Chip-Kondensatoren – Produkte hoher Zuverlässigkeit mit vielversprechender Zukunft.

Keramik-Chip-Kondensatoren können nicht in gleicher Weise umhüllt werden, wie die entsprechenden mit Drahtanschlüssen versehenen Kondensatoren, um sie unmittelbar gegen das Eindringen von Feuchtigkeit zu schützen. So sind bei einigen Herstellern Frühausfälle erforscht worden, die von Durchschlägen bei niedrigen Spannungen herrühren. Diese Ausfälle sind eindeutig auf Herstellungsfehler zurückzuführen. Bei sorgfältiger Herstellung ist die Zuverlässigkeit von Keramik-Chip-Kondensatoren über jeden Zweifel erhaben. In Verbindung mit den jüngsten Fortschritten der Keramiktechnologie ist die Langfrist-Zuverlässigkeit dieser Bauelemente ausserordentlich hoch.

Stereofoner Schallerzeuger für Klangeffekte und synthetische Musik

Um den gegenwärtigen Stand der akustischen Kommunikation zwischen Computer und Benutzer zu verbessern, wurde ein Stereo-Schallgenerator-IC entwickelt. Die Klänge, die erzeugt werden können, schliessen die Simulation von Musikinstrumenten und die Töne für Home-Computer-Spiele ein. Volle Musikakkorde und alle musikalischen Töne im Bereich von acht Oktaven können generiert werden. Der Generator lässt sich ohne weiteres von den meisten Mikrocontrollern steuern und benötigt nur wenige externe Bauelemente. Ausserhalb des Home-Computer-Marktes eignet sich der Generator zur Erzeugung von Klangeffekten für Modelleisenbahnen und Modellautos sowie für akustische Alarme.

Harvard-Architektur bringt Mikrocontroller-IC in den Hochgeschwindigkeitsbereich

Mit seinen 3 parallelen Bussen, Schaltungsaufbau in ECL-Technik und 100 ns Befehlszykluszeit erfüllt der neue Mikrocontroller 8X401A problemlos die aktuellen Hochgeschwindigkeitsaufgaben, wie z.B. Signalverarbeitung, Datenkommunikation und Peripherie-Steuerung. Neben der hohen Arbeitsgeschwindigkeit bestehen weitere Vorzüge des 8X401 gegenüber seinen Vorgängern in seinen vollständigen Möglichkeiten zur Verarbeitung von Interrupts und Subroutinen. Darüber hinaus sind vier neue Sprung- und Return-Befehle und zusätzliche arithmetische und logische Operationen in diesem Mikrocontroller verfügbar.

Integrierter Video-Programm-System (VPS)-Decoder

Da die Timer konventioneller Videorecorder fehlerhafte Programmzeitangaben nicht berücksichtigen, besteht die Gefahr, dass unerwünschte Programme aufgezeichnet werden. Die europäischen Fernsehanstalten wollen daher einen Video-Programm-System-Code (VPS) in Fernsehsendungen einführen, der im Empfänger decodiert wird, so dass die aktuellen Anfangs- und Endzeiten für ein Programm in korrekter Form vorliegen. Dieser Beitrag beschreibt ein Schaltungspaket aus zwei ICs, welches das VPS-Signal decodiert und den Videorecorder über den einfachen Zweidraht-I^2C-Bus steuert.

Elektrolytkondensatoren für hohe Temperaturen

Während der letzten 10 Jahre ist die Betriebstemperatur von nassen Elektrolytkondensatoren bis auf den aktuellen Wert von 125 °C (doppelter Wert) angestiegen. Dies ermöglicht neue Anwendungen z.B. in der Automobil- sowie Militärelektronik und für Schaltnetzteile. Der vorliegende Beitrag behandelt die Reihe 2222 118..... von Elektrolytkondensatoren für hohe Temperaturen, ferner die Designkriterien für den Betrieb bei hohen Temperaturen. Es wird gezeigt, wie sich die Lebensdauererwartung berechnen lässt, und es werden Resultate von Lebensdauerprüfungen mitgeteilt.

IST-Bus (Integrated Services Terminal)

Mit dem modernen elektronischen Büro kam das Problem auf, dass Computer und andere Datenterminals häufig separate Koaxialkabel-Netzwerke benötigen, um miteinander kommunizieren zu können. Eine Lösung bietet hier der IST-Bus, der über eine einfache Interfaceschaltung die gleichzeitige Übertragung von Daten- und Telefonsignalen auf einer preisgünstigen verdrillten Zweidrahtleitung erlaubt. Dieser Beitrag beschreibt die Arbeitsweise sowohl des IST-Busses als auch des zugehörigen Interface-ICs. Ausserdem wird anhand von Beispielen gezeigt, wie der IST-Bus in bestehende und künftige Systeme integriert werden kann.

Authors

Ad Otten joined Philips Research Laboratories, Geldrop, The Netherlands in 1964, after completing his studies at Eindhoven Polytechnic. Initially he worked on electron and ion optics. In 1978 he moved to the Electronic Components and Materials Division of Philips, Eindhoven, where he was responsible for marketing electrolytic capacitors, and since 1986 he has been responsible for strategic planning at the Industrial and Electro-acoustic Division.

Greg Goodhue is a senior applications engineer for Signetics' Microprocessor Division at Sunnyvale, California, working on developing and supporting new products. He holds a BS degree in computer science from the California State University at Chico.

Mike Roberts studied electronic engineering and physics at the University of Technology, Loughborough, U.K. After graduating in 1974, he joined the IC Division of Mullard Southampton, initially working as a product engineer. Since 1982 he has been a member of the International Product Marketing Team for MOS ICs, with special responsibility for speech synthesis and Teletext circuits.

Ata Khan is a Design Engineering Manager in Signetics' Microprocessor Division, specializing in advanced microprocessor design. He has an MSEE from the University of California at Berkeley and an MBA from the University of Santa Clara. He has been with Signetics since 1976.

Just Slakhorst received his degree in materials science from Twente University, The Netherlands, in 1973, and his doctorate in 1977 from the Dutch Foundation for Fundamental Research of Matter. The same year he also received the Brandoma Award for his work on recrystallization textures. He joined Philips Electronic Components and Materials Division at Zwolle in 1978 fulfilling several functions in development and production. He is currently product manager for the complete range of Philips products manufactured at Zwolle.

René Kohlman studied electrical engineering at the University of Technology, Enschede, The Netherlands, graduating in 1982. Since May 1983 he has been a member of the Central Applications Laboratory of Philips' Electronic Components and Materials Division, Eindhoven, where he works on ICs for ISDN. Since 1984 he has also worked on the International Standardization Committee CCITT.

Günther Stäcker was born in Schlichting, Germany, in 1944. After military service he studied electrical engineering at the Fachhochschule, Hamburg, graduating in 1970. The same year he joined the Valvo Applications Laboratory and was initially engaged in the development and application of line deflection circuits for television receivers. He is currently working on special digital video systems.

W. Langenhorst was born in 1935 and studied chemical technology at the Technical High School, Delft, The Netherlands, graduating in 1960. The same year he joined Philips, Roermond, working in the area of passive components, including film and ceramic capacitors, and on the development of nickel-cadmium batteries. He is currently head of product development for ceramic capacitors at Roermond.

Reiner Waser was born in Frankfurt/Main, Germany in 1955. After gaining an MSc and subsequently a PhD in chemistry from the University of Darmstadt, he joined Philips Research Laboratories, Aachen, working in the Electronic Ceramics Group. His main interests there have been the study of reliability aspects in ceramic-multilayer capacitors, with particular emphasis on defect chemistry and transport properties of point defects in oxide ceramics.

Axel Lentzer was born in Hamburg, Germany in 1949. After graduating in communications engineering from the Technical University of Hanover in 1977, he joined the VCR/TV IC development department of the Philips Bipolar Semiconductor Factory in Hamburg. Since May 1984 he has been a member of the International Product Marketing Department responsible for bipolar VCR ICs.

David K. Wong is Applications Manager of PLD products at the Applications Specific Products (ASP) Division of Signetics, California. David has been working in the semiconductor industry for over 11 years and has been with Signetics since 1983. He received his MSEE/BSEE from San Jose State University, California.

Philips Electronic Components & Materials

Elcoma – Philips Electronic Components and Materials Division – embraces a world-wide group of companies operating under the following names:

PHILIPS RTC
IBRAPE Signetics
Miniwatt
Mullard VALVO

Elcoma offers you a technological partnership in developing your systems to the full. A partnership to which we can bring

- *world-wide production and marketing*
- *know-how*
- *systems approach*
- *continuity*
- *broad product line*
- *fundamental research*
- *leading technologies*
- *applications support*
- *quality*

DISPLAY SYSTEMS

B & W tv display systems
Colour tv display systems
Data & graphic display systems

INTEGRATED CIRCUITS

Microprocessors, microcontrollers & peripherals

Memories (MOS, TTL, ECL)

Industrial integrated circuits

Integrated circuits for telephony

Semi-custom gate arrays & cell libraries (ISL, ECL, CMOS)

Semi-custom integrated circuits (IFL)

Radio, audio and associated systems

Video and associated systems

HE4000B CMOS logic family (incl. uncased types)

High-speed CMOS logic family (74HC/HCT/HCU)

ECL 10K and 100K logic families

TTL logic families (incl. LSTTL and FAST)

Hybrid integrated circuits

ELECTRO-OPTICAL DEVICES

Image intensifier devices
Infra-red image detectors
Camera tubes
Imaging devices

SEMICONDUCTORS

Small-signal diodes
Medium and high-power diodes
Controlled rectifiers
LF & HF small-signal transistors
LF & HF power transistors
Microwave semiconductors
Opto-electronic semiconductors
Semiconductors for hybrid ICs
Semiconductor sensors

PROFESSIONAL TUBES

Industrial cathode-ray tubes
Photomultiplier tubes
Geiger Müller tubes
Transmitting tubes
Microwave devices
Reed switches

MATERIALS

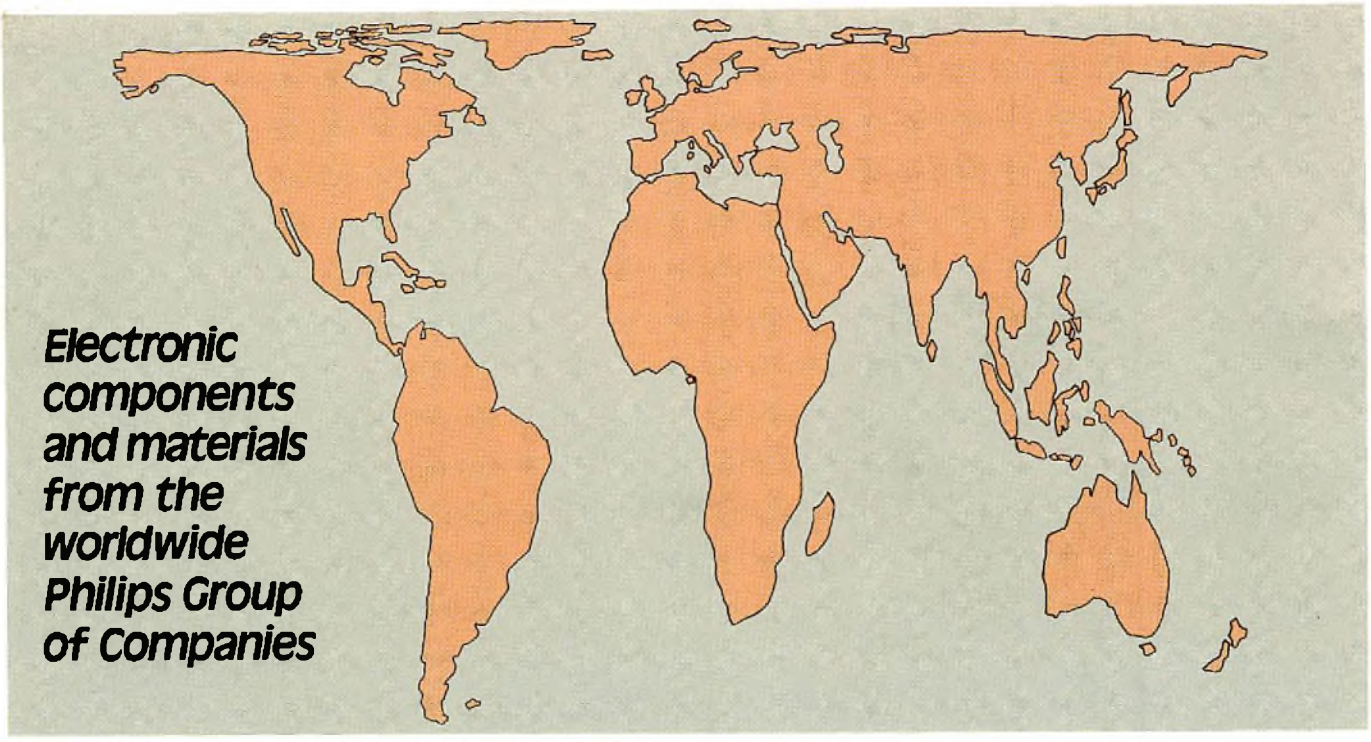
Ferroxcube products
Permanent magnets
Piezoelectric products
White ceramic products

PASSIVE COMPONENTS

Ceramic, film and foil capacitors
Electrolytic capacitors
Fixed resistors
Variable capacitors
Potentiometers and resistor trimmers
Varistors, thermistors and sensors
Delay lines
Piezoelectric quartz devices

ASSEMBLIES

Electric motors
Loudspeakers
Tuners
Printed circuit boards
Variable transformers



Electronic components and materials from the worldwide Philips Group of Companies

Argentina: PHILIPS ARGENTINA S.A., Div. Elcoma, Vedia 3892, 1430 BUENOS AIRES, Tel. (01) 541 - 7141 to 7747.
Australia: PHILIPS INDUSTRIES LTD., Elcoma Division, 11 Waltham Street, ARTARMON, N.S.W. 2064, Tel. (02) 439 3322.
Austria: ÖSTERREICHISCHE PHILIPS INDUSTRIE G.m.b.H., UB Bauelemente, Triester Str. 64, A-1101 WIEN, Tel. (0222) 62911-0.
Belgium: N.V. PHILIPS & MBLE ASSOCIATED, 80 Rue Des Deux Gares, B-1070 BRUXELLES, Tel. (02) 525-61-11.
Brazil: CONSTANTA-IBRAPE; (Active Devices): Av. Brigadeiro Faria Lima, 1735-SAO PAULO-SP, Tel. (011) 211-2600,
(Passive Devices & Materials): Av. Francisco Monteiro, 702 - RIBEIRAO PIRES-SP, Tel. (011) 459-8211.
Canada: PHILIPS ELECTRONICS LTD., Elcoma Division, 601 Milner Ave., SCARBOROUGH, Ontario, M1B 1M8, Tel. (416) 292-5161.
Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. (02) 773816.
Colombia: IND. PHILIPS DE COLOMBIA S.A., c/o IPRELENSO LTD., Cra. 21, No. 56-17, BOGOTA, D.E., Tel. (01) 2497624.
Denmark: MINIWATT A/S, Strandlodsvej 2, P.O. Box 1919, DK 2300 COPENHAGEN S, Tel. (01) 541133.
Finland: OY PHILIPS AB, Elcoma Division, Kaivokatu 8, SF-00100 HELSINKI 10, Tel. (90) 17271.
France: RTC-COMPELEC, 130 Avenue Ledru Rollin, F-75540 PARIS 11, Tel. (01) 43388000.
Germany (Fed. Republic): VALVO, UB Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-0.
Greece: PHILIPS HELLENIQUE S.A., Elcoma Division, No. 15, 25th March Street, GR 17778 TAVROS, Tel. (01) 4894339/4894911.
Hong Kong: PHILIPS HONG KONG LTD., Elcoma Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)-245121.
India: PEICO ELECTRONICS & ELECTRICALS LTD., Elcoma Dept., Band Box Building,
254-D Dr. Annie Besant Rd., BOMBAY - 400025, Tel. (022) 4930311/4930590.
Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Elcoma Div., Setiabudi II Building, 6th Fl., Jalan H.R. Rasuna Said (P.O. Box 223/KBY) Kuningan,
JAKARTA 12910, Tel. (021) 517995.
Ireland: PHILIPS ELECTRICAL (IRELAND) LTD., Elcoma Division, Newstead, Clonskeagh, DUBLIN 14, Tel. (01) 693355.
Italy: PHILIPS S.p.A., Div. Componenti Elcoma, Piazza IV Novembre 3, I-20124 MILANO, Tel. (02) 6752.1.
Japan: NIHON PHILIPS CORP., Shuwa Shinagawa Bldg., 26-33 Takanawa 3-chome, Minato-ku, TOKYO (108), Tel. (03) 448-5611.
(IC Products) SIGNETICS JAPAN LTD., 8-7 Sanbancho Chiyoda-ku, TOKYO 102, Tel. (03) 230-1521.
Korea (Republic of): PHILIPS ELECTRONICS (KOREA) LTD., Elcoma Div., Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. (02) 794-5011.
Malaysia: PHILIPS MALAYSIA SDN BHD, Elcoma Div., 345 Jalan Gelugor, 11700 PULAU PINANG, Tel. (04) 870044.
Mexico: ELECTRONICA, S.A de C.V., Carr. México-Toluca km. 62.5, TOLUCA, Edo. de México 50140, Tel. Toluca 91 (721) 613-00.
Netherlands: PHILIPS NEDERLAND, Marktgroep Elonco, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 783749.
New Zealand: PHILIPS NEW ZEALAND LTD., Elcoma Division, 110 Mt. Eden Road, C.P.O. Box 1041, AUCKLAND, Tel. (09) 605-914.
Norway: NORSK A/S PHILIPS, Electronica Dept., Sandstuveien 70, OSLO 6, Tel. (02) 680200.
Pakistan: PHILIPS ELECTRICAL CO. OF PAKISTAN LTD., Philips Markaz, M.A. Jinnah Rd., KARACHI-3, Tel. (021) 725772.
Peru: CADESA, Av. Alfonso Ugarte 1268, LIMA 5, Tel. (014) 326070.
Philippines: PHILIPS INDUSTRIAL DEV. INC., 2246 Pasong Tamo, P.O. Box 911, Makati Comm. Centre, MAKATI-RIZAL 3116, Tel. (02) 868951 to 59.
Portugal: PHILIPS PORTUGUESA S.A.R.L., Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. (019) 683121.
Singapore: PHILIPS PROJECT DEV. (Singapore) PTE LTD., Elcoma Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 3502000.
South Africa: S.A. PHILIPS (Pty) LTD., EDAC Div., 3rd Floor Rainer House, Upper Railway Rd. & Ove St., New Doornfontein, JOHANNESBURG 2001,
Tel. (011) 402-4600/07.
Spain: MINIWATT S.A., Balmes 22, BARCELONA 7, Tel. (03) 3016312.
Sweden: PHILIPS KOMPONENTER A.B., Lidingövägen 50, S-11584 STOCKHOLM 27, Tel. (08) 7821000.
Switzerland: PHILIPS A.G., Elcoma Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. (01) 4882211.
Taiwan: PHILIPS TAIWAN LTD., 150 Tun Hua North Road, P.O. Box 22978, TAIPEI, Taiwan, Tel. (02) 7120500.
Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. (02) 233-6330-9.
Turkey: TÜRK PHILIPS TICARET A.S., Elcoma Department, Inönü Cad., No. 78-80, 80090 Ayazpasa ISTANBUL, Tel. (01) 1435910.
United Kingdom: MULLARD LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. (01) 5806633.
United States: (Active Devices & Materials) AMPEREX SALES CORP., Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000.
(Passive & Electromech. Dev.) MEPCO/CENTRALAB, INC., 2001 West Blue Heron Blvd, RIVIERA BEACH, Florida 33404,
Tel. (305) 881-3200.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. (408) 991-2000.
Uruguay: LUZILECTRON S.A., Avda Uruguay 1287, P.O. Box 907, MONTEVIDEO, Tel. (02) 985395.
Venezuela: IND. VENEZOLANAS PHILIPS S.A., c/o MAGNETICA S.A., Calle 6, Ed. Las Tres Jotas, App. Post. 78117, CARACAS, Tel. (02) 2393931.

For all other countries apply to: Philips Electronic Components and Materials Division, International Business Relations, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Telex 35000 phtcnl

A54

Printed in The Netherlands

9398 704 90011