

# Electronic components & applications

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# Electronic components & applications

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Electronics technology is advancing so quickly that it's constantly opening-up new worlds for us. For example, we're no longer surprised when we're spoken to by our cars, our personal computers and even our weighing machines. Strange as it may seem, the principle that makes this possible is no newer than the street organ illustrated on the front cover of this issue. This instrument is very similar to the human speech production mechanism. Digital storage of the sound from the organ would require an enormous number of bits per second to be generated, but it's controlled at a much slower rate by a musical 'score' stored on linked punched cards like the ones shown above. The required bit rate for our CMOS speech synthesizer PCF8200 described on page 229 is similarly reduced by extracting the voice 'score' which contains only the control information for the voice producing instrument that generates the required sounds.

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# Parallel processing and pipelining usher DSP into the future

PETER ANDERS and TON VAN KAMPEN

The course of digital-signal processing is now pretty well established for the future. When standard microprocessors, constrained by their von Neumann architectures and weak arithmetic ability, proved inadequate for the task, the first specialized DSP chips began to appear. These devices were fortified with Harvard-like parallel architecture, multiplication-accumulation hardware and instruction pipelines.

Current stage of development sees these chips relying on faster IC technologies and even greater degrees of parallelism in their architecture. Two DSP chips falling into this category are the new PCB5010 and PCB5011, the former with data ROM and program memory, the latter without. The chips are realized in the latest high-speed CMOS technology, and with their pipelining mechanism, they take only 125 ns to complete an instruction.

The chips have the processing power (see table) to handle many of the most sophisticated DSP algorithms needed in telecommunications, speech and image processing, and general industrial applications. As a result, either version can replace multiple ICs in current designs, affording a single-chip solution that makes many applications practical for the first time. Moreover, their flexible I/O structure qualifies them for the multiple processor configurations that offer still more signal-processing power.

Architecturally, twin 16-bit data buses, X and Y, connect five functional sections, all working in parallel (Fig.1). The sections include a 16-bit multiplier and 40-bit accumulator, an ALU teamed with a multiport register file, and combined data memory and address computation logic. Completing their functional foundation are a versatile program control section and 16-bit serial and parallel I/O circuits.

Although the chips generate 8 MIPS, that figure gives only part of the performance picture. Because of the architecture's parallelism, each instruction can perform up to six

operations instead of the usual one. In other words, the chips can be said to execute the equivalent of 48 million operations/s.

Yet despite their highly parallel and pipelined nature, programming is not complex. Effective development tools assume part of the programmer's burden, but some of the chips' own features help, too. For example, each of the functional units falls under the control of a different field within the 40-bit instruction word. The programmer, therefore, need concentrate only on one field at a time and not worry about unwieldy instructions that control several functional units together.

## MULTIPLIER-ACCUMULATOR

The multiplier-accumulator section uses two 16-bit operands. Those operands can come from one of the internal buses, or they can be inverted values on the Y bus or previous multiplier operands. An operand can also be set to  $-1$ . The section's single pipeline multiplies and accumulates operands every clock cycle. In addition, a 40-bit accumulator gathers up to 255 successive 32-bit products without overflowing. The large capacity is especially useful for executing filter and Fourier transform algorithms.

A sign and scale-down unit allows subtraction, multiplication (without accumulation), and multiprecision operations. For subtraction, it inverts the contents of the accumulator register before adding the multiplier result; for multiplication without accumulation, it adds a zero to the multiplier result. Finally, it handles multiprecision operations by feeding the value in the accumulator register, divided by  $2^{15}$ , back to the accumulator.

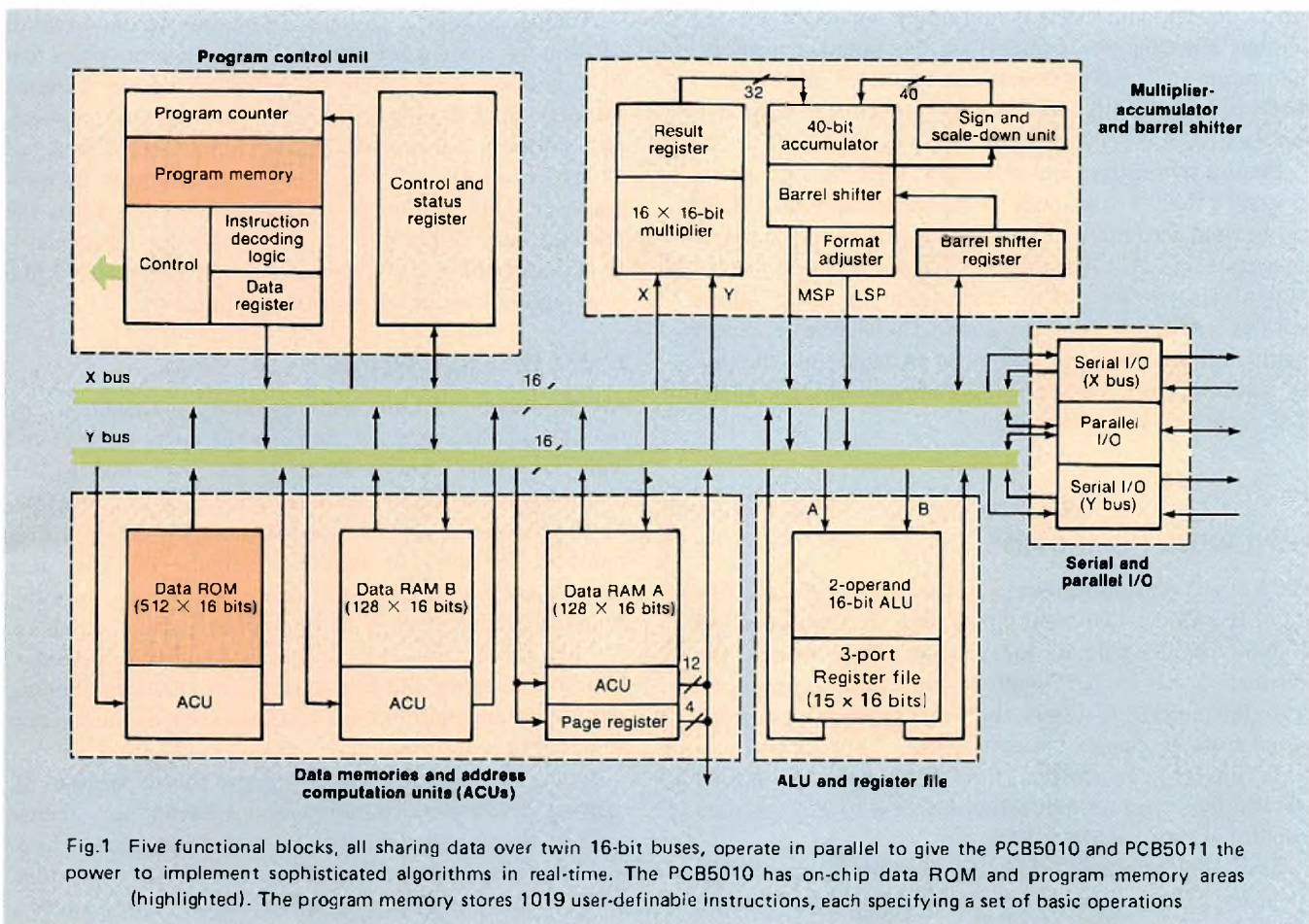


Fig.1 Five functional blocks, all sharing data over twin 16-bit buses, operate in parallel to give the PCB5010 and PCB5011 the power to implement sophisticated algorithms in real-time. The PCB5010 has on-chip data ROM and program memory areas (highlighted). The program memory stores 1019 user-definable instructions, each specifying a set of basic operations

Results flow from the accumulator register to a barrel shifter which, in turn, feeds a format adjuster. The barrel shifter is controlled by the contents of a register, and extracts a 32-bit word (1 of 16) from the accumulator. The format adjuster facilitates multiprecision operations. It also reverses a result's bit order, if needed, for serial transmission.

A second functional unit combines the ALU and a register file. The ALU performs 31 operations, some of them as multiprecision functions, on data from the X and Y buses or on an earlier ALU operand. All operations can be executed while products are gathering in the accumulator register.

Results from the ALU are written to a three-port 15-by-16-bit register file. During any clock cycle, data can be read from two registers within the file and written to one. For easy programming of DSP algorithms, the registers can also serve as scratchpad memory, directly accessible by any DSP algorithm by way of the two buses.

Three data memories and three address-computation units (ACUs) constitute another functional block within the chips. All three memories, the two 128-by-16-bit static RAMs and the 512-by-16-bit ROM (PCB5010 only), can be accessed in one clock cycle. The ROM is particularly valuable for storing filter coefficients, cosine values, and other types of data.

Related to each memory is an ACU that calculates the next address while the previous address is still being accessed. Beside incrementing, decrementing, and stepping through addresses, each unit can perform ring-buffer addressing, paging, and bit reversals (the last for efficient FFT operations).

## PROGRAM CONTROL

The program control section differs for each chip. In the PCB5011, the associated program memory is missing. Yet, using a small amount of external logic, the chip can address 64k-by-40-bit words from external memory. In the PCB5010, the 1k-by-40-bit program space, composed mostly of ROM, holds 987 mask-programmable, user-defined instructions, and a fixed five-word routine that can dynamically load instructions into its 32 RAM locations.

In both chips, the section contains a program counter and an instruction decoder and register. Both chips also have hardware-reset and maskable interrupt logic. In addition, interrupt vectors can be written into the program counter via the X bus. Similarly, subroutine starting addresses

can be loaded and different subroutine sequences selected without changing the contents of the program memory. Subroutine calls and interrupts can be nested in a five-level hardware stack, with deeper stacks programmable through software.

Besides subroutines and interrupts, flags can also alter a program's flow. For example, processor status and I/O flags can be used separately or together to control branch operations. In addition, when the chip's repeat register is loaded with a value, it iterates an instruction up to 255 times without additional program code. The power to repeat instructions on command means, for example, that the chip can execute the kernel of a finite-impulse-response (FIR) filter from only three instructions.

**POWERFUL I/O SECTION**

The I/O section is fundamental to the strength of these new chips. It includes two serial inputs, two serial outputs, and a 16-bit parallel port, all independent of the others. The I/O section can connect multiple processors to produce a powerful multi-DSP system (Fig.2(a)) or, in telecommunication systems, can tie together separate network and user ports (Fig.2(b)). In addition, the PCB5011 sports a second 16-bit port to sustain bidirectional access to external data memory, whether RAM or ROM.

Each serial port transfers up to 4Mbits/s under the command of its own hardware and external clock. Transfers occur asynchronously without interrupting any on-chip processing. Each serial port's word length can be set at between for 1 and 16 bits, and for handshaking each one has its own status flag.

The parallel port's 16 lines can address up to 64 kwords of memory – one word every 125 ns for memory chips that have a 60-ns access time or better. Accessing external memory, instead of internal memory, exacts no performance penalty, and a wait input accommodates slower, less expensive memories without any attention from the programmer. One of the ACUs generates bits for 12 of the address lines, and a page register holds the remaining 4. If 4k words or less of external memory is connected, the page register is available as a control output.

**EASY INSTRUCTIONS**

All the functional units are controlled simultaneously by the chip's instruction set, avoiding the delay encountered with sequential control schemes. As mentioned earlier, every 40-bit instruction contains separate fields, or operations, that either control a specific unit or define a data transfer. The basic operations are similar to those of a normal microprocessor, but many are more powerful. Among the operations are 45 that multiply and accumulate, 31 that invoke the ALU, and 8 that compute addresses. In addition, move and load-immediate operations abound, and 50 status conditions can be checked by the instruction set's four branch operations.

In all, instructions are classified into four types (0 to 3), each with its own set of basic operations. Each type computes three addresses and reads the data memory at each address. In addition, type 0 instruction includes an ALU operation, as well as two move operations over the data buses; a type 1 instruction multiplies and accumulates, and executes two moves over the data buses. Type 2 instructions are all branches, and type 3 instructions perform a Load Immediate operation.

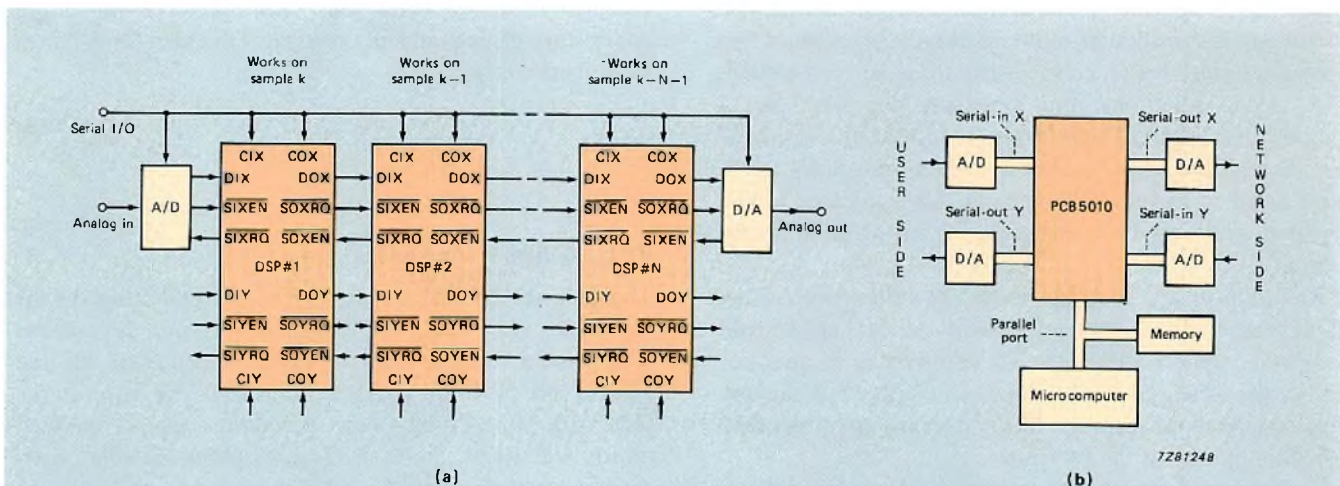


Fig.2 (a) The architecture's four serial ports can be used to implement a powerful multi-DSP system without additional logic. Shown here is a so-called pipelined system. Only one input and output port are used. The second input/output port may be used to increase the inter-DSP communications or to connect several peripherals. (b) PCB5010 used in a telecom terminal (modem, ISDN etc.). The serial ports take care of the bidirectional user and network communication paths. The parallel port is connected to a microcontroller and external data memory

A typical type 1 instruction starts with the binary value 01 in its first field (Fig.3). Following that are two fields that control the multiplier-accumulator section and select operands for it. Next come source and destination fields that specify transfers over the X and Y buses. Following those is a field that defines a destination in the register file, and three fields that control the ACUs for RAMA, the ROM, and RAMB.

Fortunately, the chips' programming language and assembler simplify the work of writing instructions. For example, the assembler will translate the following line of code into a type 1 instruction.

```
MPY(ROM,MYL,+ACR)
RAMB:=MSP
AC(RAMA,INCA)
AC(RAMB,DECA)
AC(ROM,STEP);
```

Executing that instruction causes the multiplier to act on operands from the data ROM and a Y bus multiplier latch, MYL containing on "old" operand; the accumulator then adds the multiplier result to the value in ACR, the accumulator register. The most significant part of the barrel shifter output, MSP, is transferred over the Y bus to RAMB. Also, the ACU for RAMA increments its address by 1, while the one for RAMB decrements its own address by 1. The ROM's ACU increments its address by a previously loaded constant. After all the address changes are made, the memories are accessed and data is written to their output registers.

The assembly listing helps programmers by indicating where, in the program, pipelined results are available. That information can be invaluable, since the pipeline depth ranges from one clock cycle for basic operations to as many as four cycles for compound operations. (The chips also have a non-pipelined mode for basic operations.)

To assist designers, a macroroutine library is available that contains basic functions like multiprecision, complex-number, and bit-manipulation operations. It also has parameterized macroroutines of common algorithms like those for finite- and infinite-impulse-response filters and for fast Fourier transforms. The macros will serve both as programming examples and as routines that can be tailored to a system under development.

### AN APPETITE FOR APPLICATIONS

A sample 128-point complex FFT shows how the chips might be used for fast digital signal processing (Fig.4). The chips perform the FFT in only 0,9 ms, or 1,1 ms including the I/O and windowing functions.

The calculations are done using three external FIFO memories, each organized as 256 by 16 bits. The chip calculates the FFT of the 128 complex input samples in FIFO 1, while another 128 samples are collected in FIFO 2. When FIFO 2 is filled, the chip starts processing the contents; incoming samples are now directed to FIFO 1. The output samples are either stored in FIFO 3 or used immediately in further calculations by the chip.

The FFT calculation itself begins when the chip reads the real and imaginary parts of each sample – 256 values in all – over the 16-bit parallel bus into the two internal data RAMs. Here, the bit-reversal feature of the ACUs allows the samples to be stored in an order suitable for FFTs.

Before executing the actual FFT, the samples are modified by a shaping signal. The modification, called windowing, takes place in the chip's multiplier unit, which draws the necessary coefficients from the on-chip data ROM. Next, the chip performs a radix-2 decimation-in-time FFT. Automatic scaling of the butterflies avoids any overflow, and

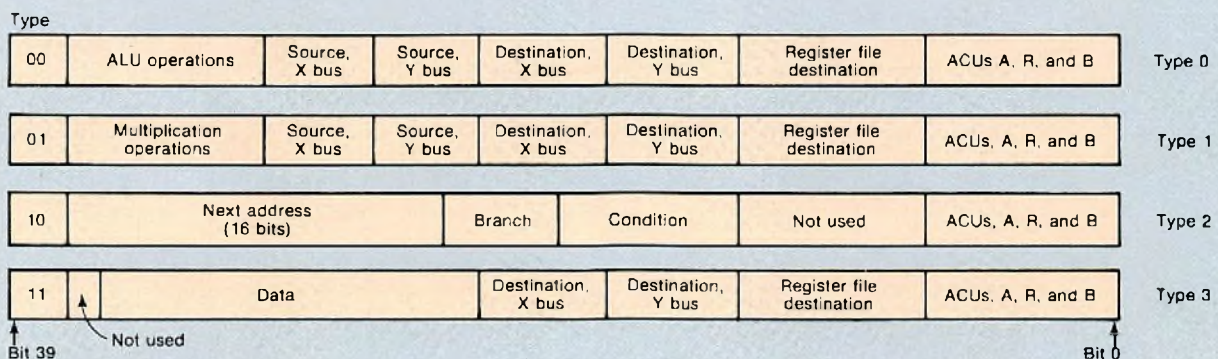


Fig.3 The chips' 40-bit instructions fall into four categories, each defining its own specific set of basic operations. A type 1 instruction, for example, multiplies and accumulates two operands, executes two move operations over the X and Y data buses, and undertakes three address calculations and data read operations

sine values are taken from the data ROM as needed. The results are stored in the on-chip RAM for further calculations or for transfer over the parallel bus to FIFO 3.

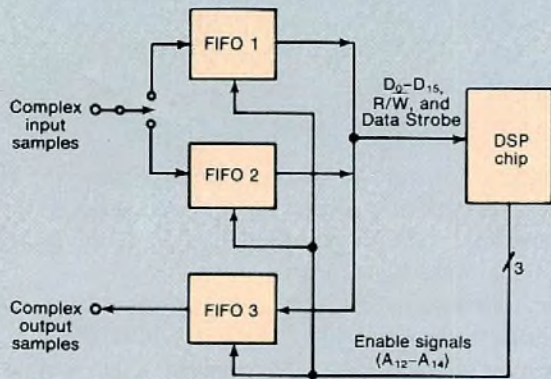


Fig.4 Three FIFOs and the PCB5010 (or PCB5011) run a complex FFT on 128 samples in 1,1ms, taking I/O and windowing functions into account. As one FIFO fills with samples, another supplies the DSP chip with earlier samples. The third FIFO holds the results, if necessary. For a greater number of samples, the input FIFOs can be replaced with RAMs

If the number of complex samples doubles to 256, all of them cannot be stored in the on-chip RAM at once. In that case, two external RAMs, 512 by 16 bits each, replace FIFOs 1 and 2. Similar to the previous example, the first RAM would be accessed for calculation while the second RAM is filling with samples. When the latter is filled, its samples start feeding the DSP chip, and the first RAM now starts filling.

The first part of the FFT algorithm is executed directly on the data in the external RAM, without the use of the multiplier unit. As before, the second part of the algorithm involves performing two 128-point FFTs inside the chip, and the output is either fed to FIFO 3 or retained by the digital signal processor. The total processing time, including windowing and I/O operations, is only 2,3 ms.

The FFT calculations can be incorporated into larger systems and modified as needed with, say, overlapping windows, different I/O requirements, or further computation. Still, the basic rates of calculation for the 128- and 256-point complex FFTs are valuable for estimating a system's processing requirements.

Consider, for example, a speech recognition system specified for a sample frequency of 10kHz, a frame size of 256 samples, and a frame shift of 100 samples (Fig.5). For each frame, a Hamming window is required, along with a 256-point complex FFT, 256 amplitude calculations on the result, and an analysis leading to the 16 filter-bank outputs.

In all, the time that is available for processing a frame is 10 ms – well within the chip's capacity, as the previous example showed. A host microprocessor takes over the remaining tasks of reducing and normalizing data and comparing it with reference templates. It gets the raw data – that is, the 16 filter-bank outputs – from one of the DSP chip's serial output ports.

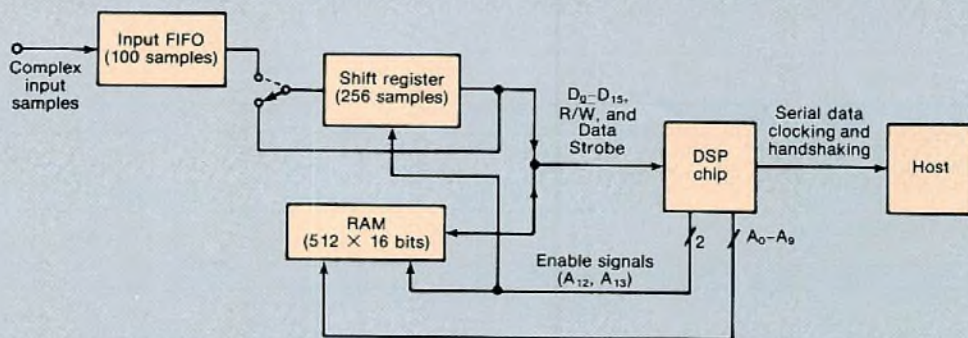


Fig.5 A speech recognition system exploits the PCB5010's fast computational ability, requiring a 256-point FFT and other calculations every 10 ms. Sixteen filter-bank output values are sent over a serial bus to the host for data reduction, normalizing, and comparison with reference templates

**Parallel architecture's benchmark ratings**

function	execution time ( $\mu$ s)
2nd-order infinite-impulse-response (IIR) section (kernel only)	0,625
2nd-order IIR section (including initialization function and I/O)	2,125
8th-order filter (cascaded 2nd-order IIR sections, including initialization and I/O)	3,125
64-tap FIR filter (kernel only)	9,25
16-point complex FFT (kernel only, straight line)	28,38
16-point complex FFT (kernel only, looped*)	76,6
128-point complex FFT (kernel only, straight line)	457,0
128-point complex FFT (kernel only, looped)	927,0
128-point complex FFT (kernel only, looped, I/O, shuffling window, scaling)	1100,0
256-point complex FFT (kernel only, straight line)	1200,0
256-point complex FFT (kernel only, looped)	2112,0
256-point complex FFT (kernel only, looped, I/O, shuffling window, scaling)	2300,0
1024-point complex FFT (kernel only, straight line)	6850,0

Note: Overflow handling is included in the FFT benchmarks.

\* 40 instructions.

**ACKNOWLEDGEMENT**

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# Thermal resistance of SO and PLCC packages

PAUL MELVILLE

The thermal characteristics of integrated circuits are major considerations for both manufacturers and users of electronic components. Now, with the increasing use of surface-mounted integrated circuits (SM ICs), these characteristics are even more important, for not only are the packages much smaller than conventional DILs, but the thermal dissipation is concentrated on densely populated substrates. Therefore, an understanding of these characteristics, particularly the thermal resistance, is essential for effective thermal management.

This article outlines the technique of measuring the thermal resistance for small-outline (SO) and plastic-leaded chip carrier (PLCC) SM ICs, and demonstrates how it is influenced by both internal and external factors. The results are presented graphically, and show the relationship between the thermal resistance (both from junction to ambient,  $R_{thj-a}$ , and from junction to case,  $R_{thj-c}$ ) and the die size, with both alloy-42 (a nickel/iron alloy – for SO only) and copper leadframes. The characteristics of DIL packages are shown for comparison.

All tests from which the graphs were derived are carried out on SM ICs soldered to special test boards (see "Test conditions"). It is important to recognize that the board is an essential part of the test environment, and that boards of different size and compositions may give slightly different results from those reproduced here. This must be considered when comparing published data.

In addition to examining thermal resistance of SO and PLCC packages, some general aspects of thermal management are also discussed. For example, the influence of forced-air cooling, board area, trace length, and power dissipation are shown.

## TEST METHOD

To measure the junction temperature of an IC, we use a technique known as the temperature sensitive parameter (TSP) method. The TSP is a temperature-dependent electrical characteristic of the junction under test which can be calibrated with respect to temperature and subsequently used to detect the junction temperature. This is in accordance with MIL-STD-883C, Method 1012.1. (Ref.1).

We use the forward voltage drop (at a constant forward current) of an on-chip p-n junction to measure the change in junction temperature due to known power dissipation. Ideally, the junction with the greatest power dissipation density ( $W/mm^2$ ) should be selected, as this will generally have the highest temperature on the chip.

To obtain a realistic estimate of the average operating junction temperature ( $T_{j(av)}$ ), the whole chip must be powered to provide the proper internal temperature distribution. The measured junction temperature of the TSP ( $T_{j(m)}$ ) is indicative of the temperature only in the vicinity of the TSP junction. But if the TSP junction is dissipating power with a uniform heating current distribution, then  $T_{j(av)} \approx T_{j(m)}$ .

The thermal resistance from junction to ambient can be calculated using the expression:

$$R_{thj-a} = \frac{\Delta T_j}{P_D} = \frac{T_j - T_{amb}}{P_D} \text{ K/W}$$

where:

$T_j$  = junction temperature ( $^{\circ}C$ )

$T_{amb}$  = ambient temperature ( $^{\circ}C$ )

$P_D$  = power dissipation (W).

**TEST PROCEDURE**

The test procedure consists of two steps, as follows:

1. *TSP calibration.* The TSP diode is calibrated to determine its change in forward voltage with temperature (at a constant forward current). Placed in a constant temperature oil bath, the device is subjected to calibration temperatures of 25 °C and 75 °C, measured to an accuracy of ±0,1 K.

The calibration current is kept constant at a low level to avoid significant junction heating during the measurement interval (data given in this publication was derived using constant currents of either 1,0 mA or 3,0 mA). This current is also chosen such that the TSP-diode forward voltage decreases linearly with increasing temperature over the range of interest. The forward voltage of the diode is measured at both calibration temperatures.

Figure 1 shows the basic calibration circuit and Fig.2 shows a typical resulting characteristic. The constant-current voltage/temperature coefficient (k-factor) of the TSP diode is the gradient of this characteristic and is calculated using the following expression:

$$k = \frac{V_{F2} - V_{F1}}{T_2 - T_1} \quad | \quad \text{for constant current } I_F$$

where:

- T<sub>2</sub> = higher calibration temperature (°C)
- T<sub>1</sub> = lower calibration temperature (°C)
- V<sub>F2</sub> = forward voltage at I<sub>F</sub> and T<sub>2</sub> (mV)
- V<sub>F1</sub> = forward voltage at I<sub>F</sub> and T<sub>1</sub> (mV).

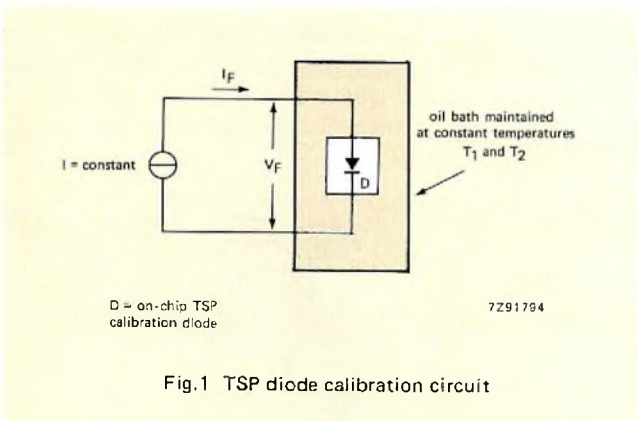


Fig.1 TSP diode calibration circuit

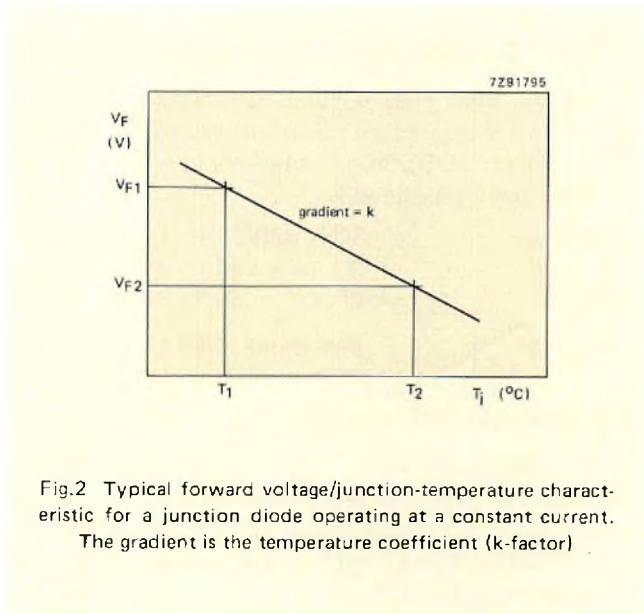


Fig.2 Typical forward voltage/junction-temperature characteristic for a junction diode operating at a constant current. The gradient is the temperature coefficient (k-factor)

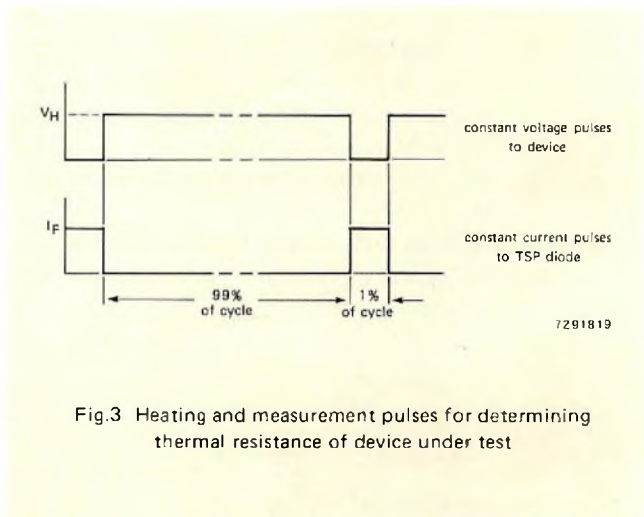


Fig.3 Heating and measurement pulses for determining thermal resistance of device under test

The measurement pulse is very short (less than 1% of the cycle) compared with the heating pulse to minimize junction cooling during measurement. The measurements start at ambient temperature and continue until a steady-state temperature condition is reached. The thermal resistance from junction to ambient (of the TSP diode, and hence of the device under test) can then be calculated using the expression:

$$R_{thj-a} = \frac{\Delta T_j}{P_D} = \frac{V_{FA} - V_{FS}}{k(V_H \times I_H)} \text{ K/W}$$

where:

- V<sub>FA</sub> = forward voltage of TSP diode at T<sub>amb</sub> (mV)
- V<sub>FS</sub> = forward voltage of TSP diode at steady-state temperature (mV)
- V<sub>H</sub> = heating voltage (V)
- I<sub>H</sub> = heating current (A).

**TEST CONDITIONS**

**Thermal-resistance tests (junction to ambient)**

All data for these tests is obtained with the SO devices soldered to Philips thermal-resistance test boards, and the PLCCs soldered to Signetics thermal-resistance test boards with the following specification:

- Board size
  - SO (small) 28,4 × 19,1 × 1,5 mm
  - SO (large ) 40,1 × 19,1 × 1,5 mm
  - PLCC 56,9 × 56,9 × 1,6 mm
- Board material
  - glass epoxy, FR-4 type, 1 oz. copper, solder coated
- SO device stand-off
  - 0,1 to 0,3 mm (see Fig.4).

Still air (natural convection) tests are run in a box having a volume of one cubic foot (0,0283 m<sup>3</sup>) of air at room temperature. Forced-convection tests (forced-air cooling) are run in a 100 × 100 mm cross-section, 660 mm long wind tunnel with air at room temperature.

SO and PLCC devices are soldered on test boards and held horizontally in a zero insertion-force (ZIF) socket with a 4 mm board stand-off height (Fig.4). For the forced-convection tests, the air flow is perpendicular to the longest axis (that along which the leads run) of SO devices when they are held in a horizontal position. Air is forced through the wind tunnel at 200, 400 and 800 linear feet per minute (lfpm).

DIL packages are mounted horizontally in a ZIF socket, with a 2 mm device stand-off (between package bottom and socket).

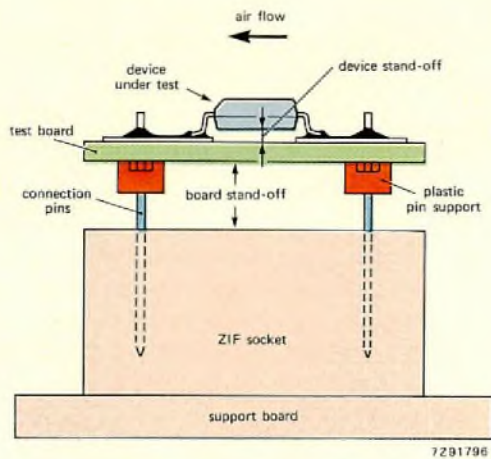


Fig.4 End view of  $R_{th j-a}$  test set-up for SO

**Thermal resistance tests (junction to case)**

The  $R_{th j-c}$  tests are run by holding the devices against an “infinite” heatsink (a water-cooled copper block, approximately 175 × 100 × 20 mm). This gives a thermal resistance from case to ambient ( $R_{th c-a}$ ) approaching zero. The copper heatsink is maintained at a constant temperature

(about 20 °C) and monitored with a thermocouple mounted flush with the heatsink surface, and centred below the die in the test device.

SO and DIL devices are mounted with the bottom of the package held against the heatsink, for which the leads must be straightend. Wires are soldered to appropriate leads for test connections and a heatsink compound is used to assure good thermal coupling.

PLCC devices are mounted with the top of the package held against the heatsink. A small spacer is used between a spring-loaded hold-down mechanism and the bottom of the PLCC. Again, wires are soldered to appropriate leads for test connections, and a heatsink compound is used for good thermal coupling. Figure 5 shows the PLCC mounting.

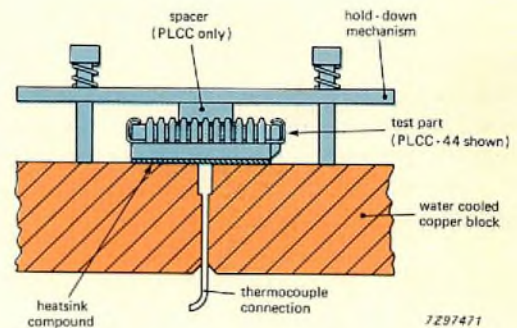


Fig.5  $R_{th j-c}$  test set-up for PLCC

**DATA PRESENTATION**

All data is derived from tests carried out on devices run at a constant power dissipation (the actual dissipation is given with each graph). Higher or lower dissipation will have a slight effect on  $R_{th j-a}$ , and the general trend is for it to decrease with increasing power dissipation (found in all package sizes tested). Figure 6 shows the average effect of power dissipation on thermal resistance from junction to ambient of plastic SM ICs.

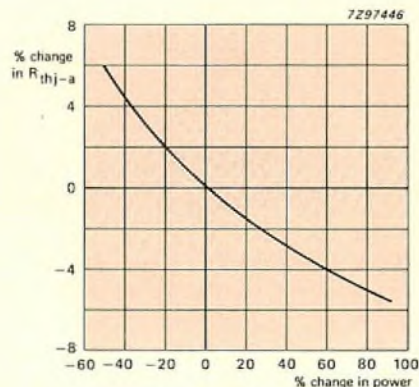


Fig.6 Average effect of power dissipation on  $R_{th j-a}$ . Effective range: 0,3 to 1,0 W for SO; 0,5 to 2,0 W for PLCC

Slight variations in internal leadframe design will nominally affect thermal resistance. For example, a larger die-pad gives slightly lower thermal resistance for the same die size. However, variations due to internal leadframe design are within the  $\pm 15\%$  accuracy stated for the thermal resistance graphs.

**THERMAL RESISTANCE DATA**

The graph in Figs 7 to 16 show the relationship between thermal resistance and die size for SO, PLCC and plastic DIL packages. Accuracy of all characteristics shown is  $\pm 15\%$ . Data is presented for the devices listed in Table 1, and so a comparison between package types can be made; characteristics for devices with the same lead-count are drawn on

the same graph. Where no equivalent DIL version exists, a package with a similar lead-count is shown.

The following data is presented:

- the relationship between  $R_{thj-a}$  and die size for SO packages with both alloy-42 and copper leadframes in still air;
- the relationship between  $R_{thj-a}$  and die size for PLCC and DIL packages with copper leadframes in still air;
- the relationship between  $R_{thj-c}$  and die size for SO, PLCC and DIL packages with copper leadframes mounted on an infinite heatsink.

Packages are mounted onto the test boards or into ZIF sockets as detailed in "Test Conditions". All data is based on the plastic packages constructed using materials with the thermal conductivities given in Table 2.

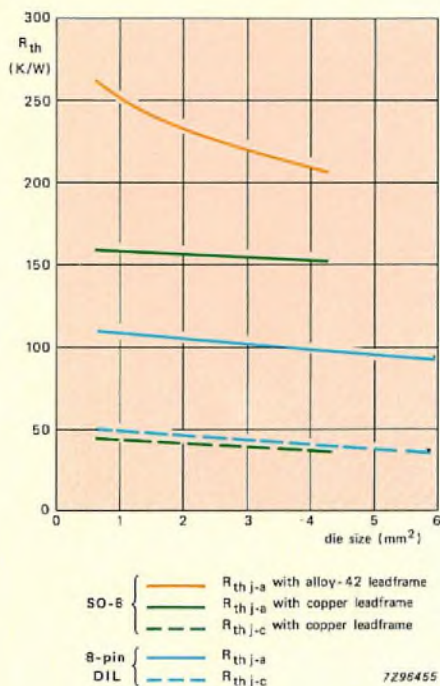


Fig.7 The relation between thermal resistance and die size for 8-lead plastic packages

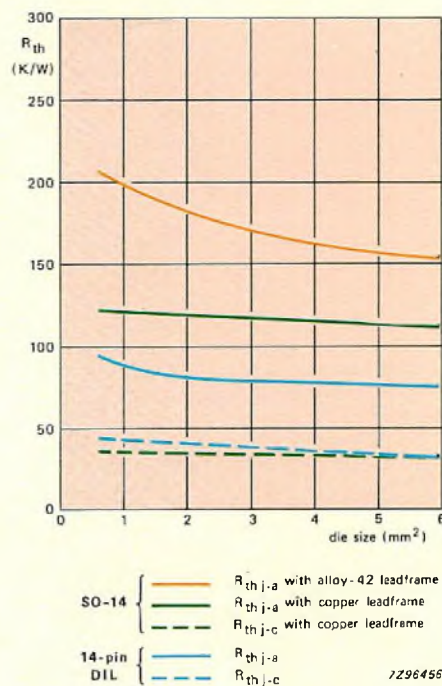


Fig.8 The relation between thermal resistance and die size for 14-lead plastic packages

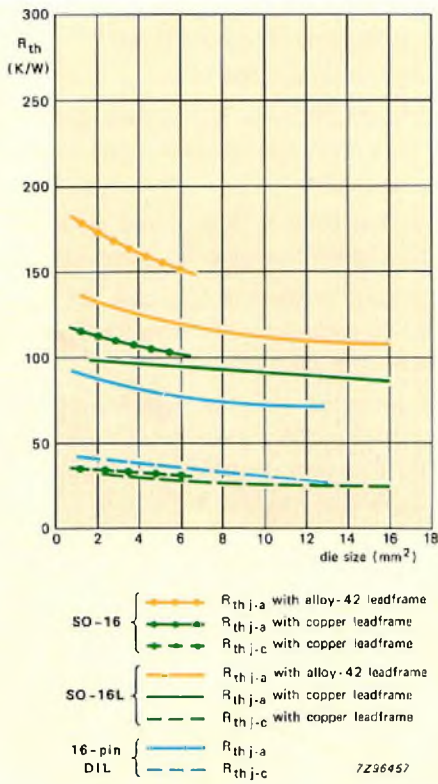


Fig.9 The relation between thermal resistance and die size for 16-lead plastic packages

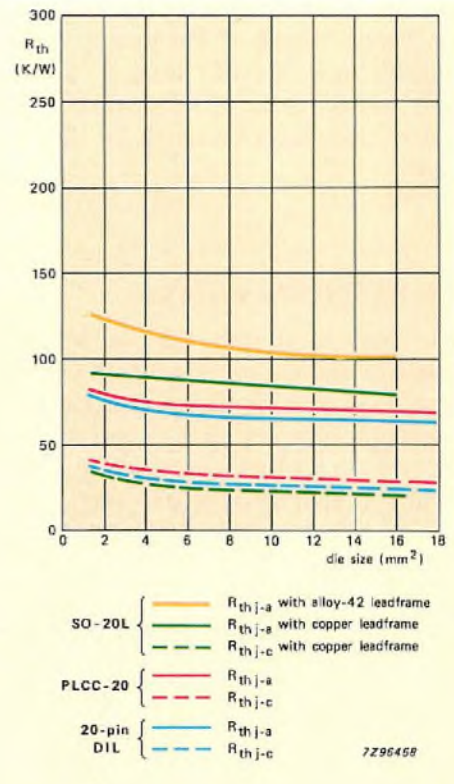


Fig.10 The relation between thermal resistance and die size for 20-lead plastic packages

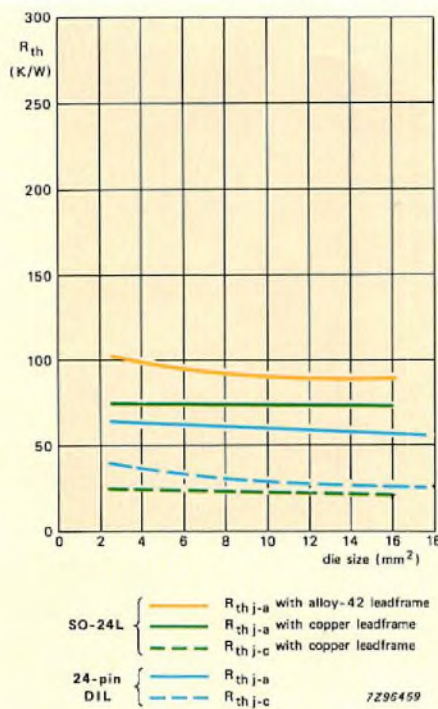


Fig.11 The relation between thermal resistance and die size for 24-lead (300 mil wide) plastic packages

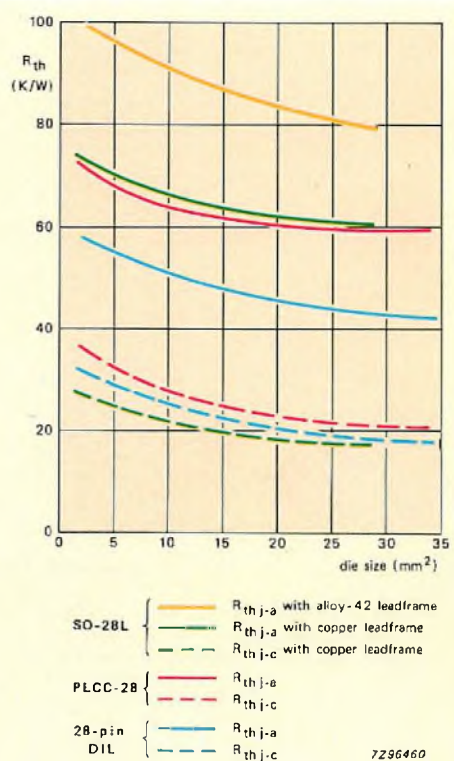


Fig.12 The relation between thermal resistance and die size for 28-lead plastic packages

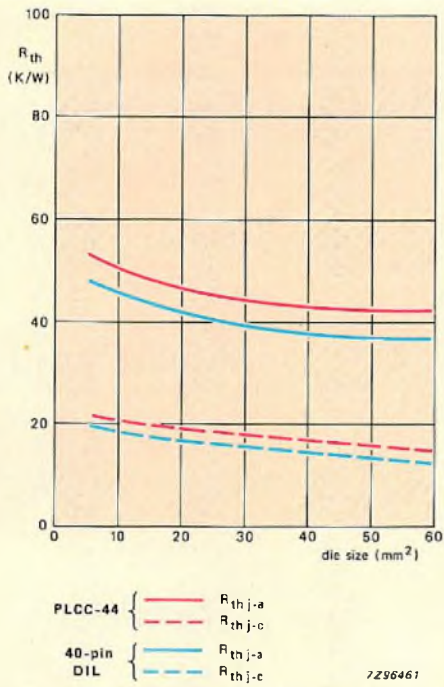


Fig.13 The relation between thermal resistance and die size for 40 and 44-lead plastic packages

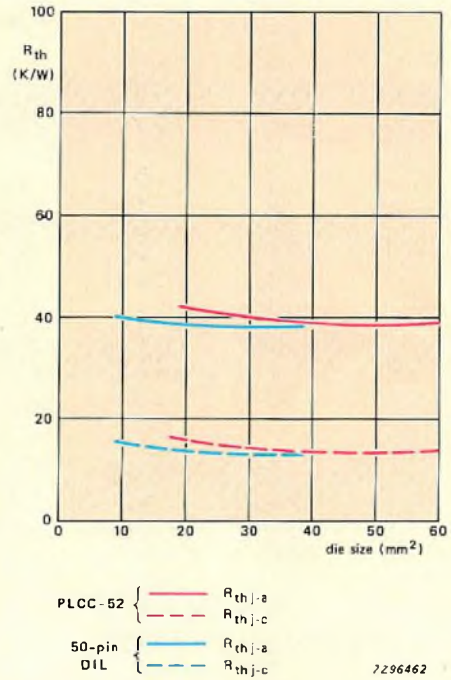


Fig.14 The relation between thermal resistance and die size for 50 and 52-lead plastic packages

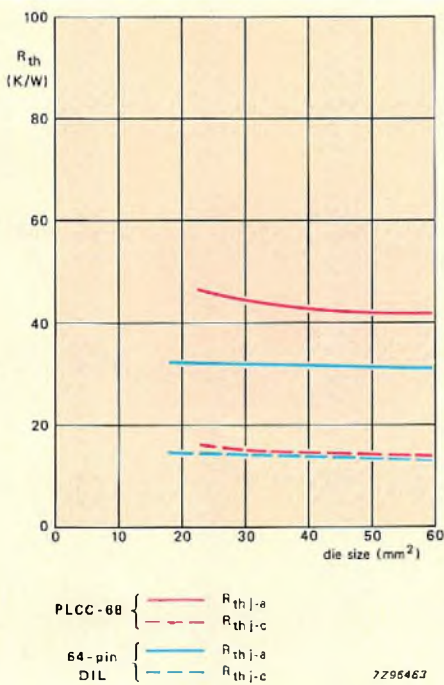


Fig.15 The relation between thermal resistance and die size for 64 and 68-lead plastic packages

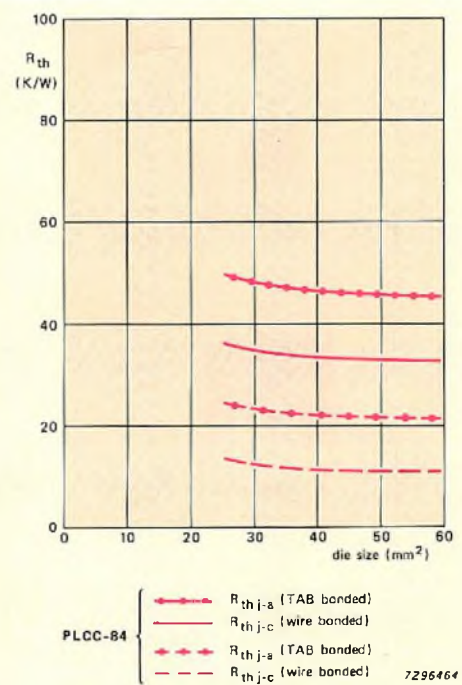


Fig.16 The relation between thermal resistance and die size for 84-lead plastic packages

**TABLE 1**  
Plastic packages tested

lead count	SO (small)	SO (large)	PLCC	DIL
8	SO-8	–	–	8-pin
14	SO-14	–	–	14-pin
16	SO-16	SO-16L	–	16-pin
20	–	SO-20L	PLCC-20	20-pin
24	–	SO-24L	–	24-pin
28	–	SO-28L	PLCC-28	28-pin
44	–	–	PLCC-44	40-pin*
52	–	–	PLCC-52	50-pin*
68	–	–	PLCC-68	60-pin*
84	–	–	PLCC-84	–

\* where an equivalent pin-count DIL package is not available for comparison, the nearest equivalent is used.

**TABLE 2**  
Thermal conductivity of materials used in SO and PLCC package construction

material	thermal conductivity W/(mK)
alloy-42	14,7
copper alloy leadframe	259
die attach adhesive	2,3
epoxy plastic moulding compound	0,67
silicon	157

**SM IC PACKAGE CONSIDERATIONS**

Experience with DIL packages has shown the value of good leadframe design in attaining optimal thermal characteristics. The leadframes of surface-mounted ICs are smaller than standard DIL leadframes, but the die-pad must be as

large, as it accepts the same chip (in fact, it can be actually larger in some types, see Fig.17). The size and shape of the leads, the die-pad size and tie-bar size all influence  $R_{thj-a}$  to some extent.

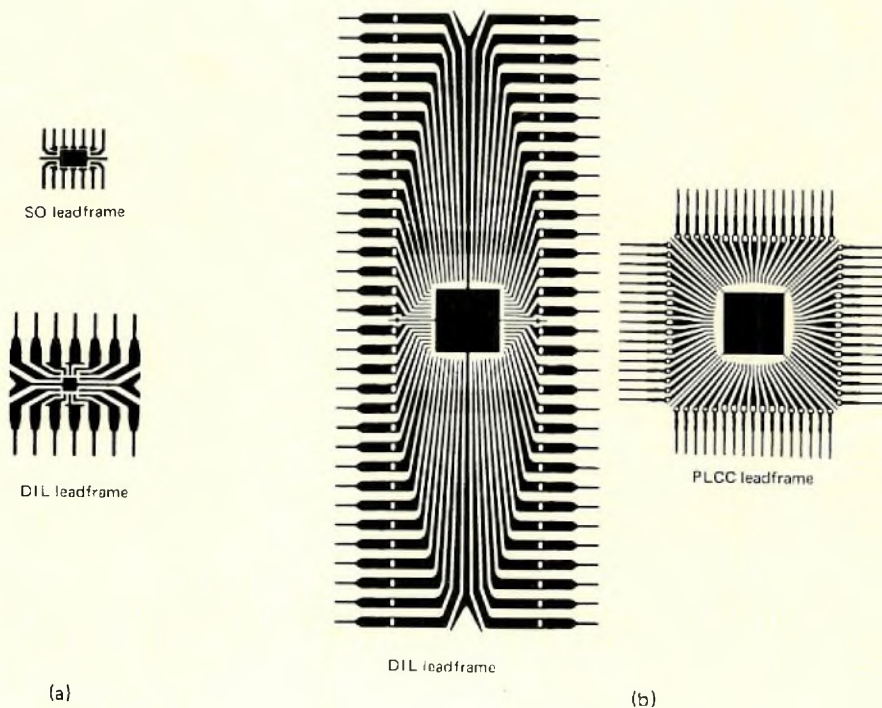


Fig.17 Leadframe comparisons for (a) 14-pin DIL and SO-14 packages, and (b) 64-pin DIL and PLCC-68

Another important factor is leadframe material. For years, DIL packages have used alloy-42 (nickel/iron alloy) leadframes as this provides the required stiffness to withstand insertion and extraction forces. The heat conduction of the DIL leadframe is considered less critical due to the larger surface area of the package.

SO and PLCC packages, however, do not have to contend with insertion and extraction forces, so a softer leadframe with a high copper content can be used. The copper alloy used has an electrical and thermal conductivity of about 95% that of pure copper, and this significantly lowers the thermal resistance.

Other package-related factors affecting  $R_{thj-a}$  include die size, die attachment, bonding wire, and moulding compound. Of these, the die size is by far the most significant, and this is reflected in the test results reproduced in this article.

Looking now at the die attachment method, although there is a difference between the thermal resistance of a silver polyimide and a gold silicon eutectic die attach, the layer is so thin (between 0,02 and 0,05 mm) that the difference is insignificant. Similarly, using either gold or aluminium bonding wire, typically 0,025 to 0,033 mm thick, does not significantly influence the thermal characteristics.

The moulding compound we use for these packages is the same high-purity epoxy plastic as used for our DIL packages, as this not only reduces  $R_{thj-a}$ , but also reduces corrosion caused by impurities and absorption of moisture.

**SYSTEM CONSIDERATIONS**

So far, we have only discussed thermal considerations relating to the internal structure of the SM IC packages. These characteristics are inherent to the design, and therefore fixed by the IC manufacturer. But there are other, system-related, thermal considerations which are under the control of the system designer.

External cooling is one such consideration. Forced-air cooling, for example, reduces  $R_{thj-a}$ , and Fig.18 shows the average effect of increased air-flow on  $R_{thj-a}$  for all SM IC packages tested,

Other system considerations affecting  $R_{thj-a}$  include the device stand-off height (for SO ICs), the average length of the traces soldered to the packages, and the total area of the substrate. Looking first at the device stand-off height (the gap between the bottom of the package and the board surface), our research shows that the larger the gap, the higher  $R_{thj-a}$  becomes (see Fig.19).

The average length of printed-wiring traces connected to an IC also affects the package's thermal resistance. The metal traces conduct heat away from the package and dissipate it to ambient, so the longer the trace, the lower  $R_{thj-a}$ . Figure 20 shows this effect for a PLCC-28 package.

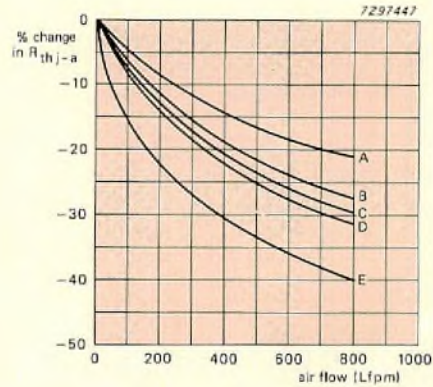


Fig.18 Average effect of air flow on  $R_{thj-a}$   
 A – SO (small) with alloy-42 leadframe  
 B – SO (small) with copper leadframe  
 C – SO (large) with alloy-42 leadframe  
 D – SO (large) with copper leadframe  
 E – PLCC with copper leadframe

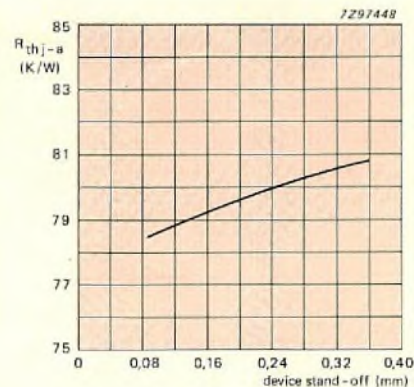


Fig.19 Effect of device stand-off on  $R_{thj-a}$  for SO-20 L with copper leadframe in still air; die size = 7,3 mm<sup>2</sup>;  $P_D$  = 0,75 W

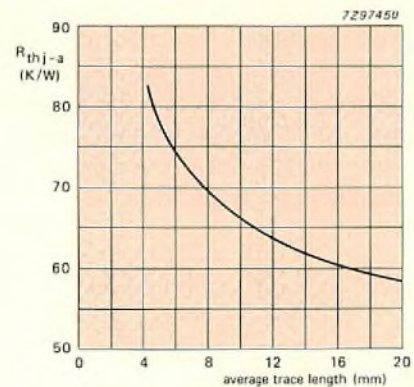


Fig.20 Effect of trace length on  $R_{thj-a}$  for PLCC-28 in still air; die size = 6,7 mm<sup>2</sup>;  $P_D$  = 1,0 W; traces are 0,7 mm wide 1 oz. copper



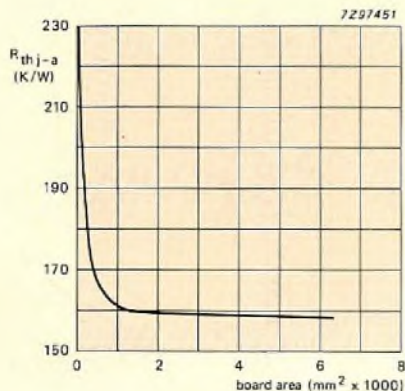


Fig.21 Effect of board area on  $R_{thj-a}$  for SO-14 with copper leadframe in still air; device stand-off 0,2 – 0,22 mm; die size = 3,25 mm<sup>2</sup>;  $P_D = 0,6 W$ ; 1,6 mm thick board with no traces

As we have already stated, the board is an essential part of the test environment. When devices are densely packed on a small board (frequently the case when using SMDs), the heat dissipation is also concentrated in a small area. To demonstrate how board size affects  $R_{thj-a}$ , a copper leadframe SO-14 package is mounted on a 1,6 mm thick glass/epoxy laminate and tested for various board sizes (see Fig.21).

**CONCLUSION**

The thermal resistance characteristics given in Figs. 7 to 16 show that the larger the SMIC package, the closer the thermal resistance is to a DIL package of equivalent pin-count. Similarly, SMIC packages with the copper alloy leadframe also have significantly lower thermal resistances than their alloy-42 counterparts. This situation is summarized in Fig.22. Please note that this diagram is intended to show the general trend as lead-count increases, and we recognise that lead count is not a continuously variable function as represented in the graph.

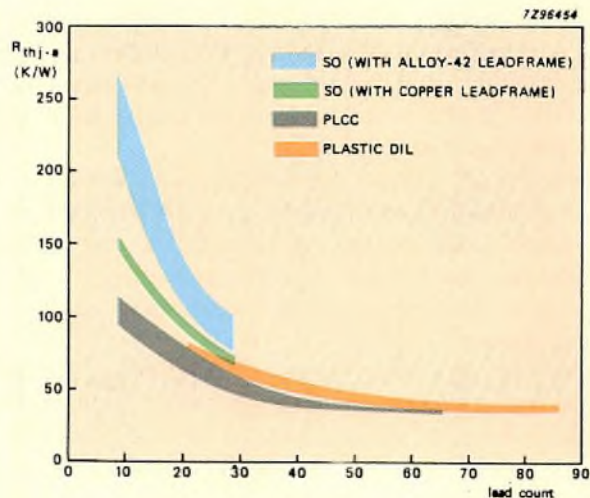


Fig.22 This diagram shows the range of thermal resistance for SO, PLCC and DIL packages against pin-count

**THERMAL PARAMETERS**

The IC junction temperature ( $T_j$ ) is the most important operating parameter in thermal management calculations. Excessive  $T_j$  lowers reliability and shortens operating life. The key thermal parameters are:

*Power dissipation ( $P_D$ )* – is the product of maximum  $V_{CC}$  and typical  $I_{CC}$ . Maximum  $I_{CC}$  values are not used since  $I_{CC}$  decreases with temperature.

*Thermal resistance ( $R_{th}$ )* – expresses the ability of the package to conduct heat away from the chip to the environment (in K/W). The thermal resistance from junction to ambient,  $R_{thj-a}$ , is the sum of  $R_{thj-c}$  (thermal resistance from junction to case); and  $R_{thc-a}$  (from case to ambient).

*Junction temperature ( $T_j$ )* – is the temperature of a powered IC chip.  $T_j$  will rise above the ambient temperature ( $T_{amb}$ ) when an IC dissipates power. If  $R_{thj-a}$  is known,  $T_j$  can be calculated as follows:

$$T_j = (P_D \times R_{thj-a}) + T_{amb}$$

Many factors affect the management of these parameters. Package variables include leadframe design and materials, encapsulation epoxy, and die size. External (system-related) variables influencing  $R_{thj-a}$  include the substrate on which the IC is mounted, the layout density, the air-gap between package and substrate, and cooling methods (for example, heatsinks or forced-air cooling).

**REFERENCE**

1. MIL-STD-883C (25 Aug. 1983). Test methods and procedures for microelectronics, Method 1012.1 (revised 15 August 1984).

# ZrO<sub>2</sub> oxygen sensor

C. FRANX

Conventional oxygen sensors are often bulky and expensive. The sensor described here is small, requires no reference gas and gives an output signal proportional to the oxygen partial pressure of the gas mixture to be measured. The sensor has an operating pressure range from a few mbar up to several bar. It can be used in gases up to 500 °C\* flowing at up to 10m/s. A feature of the sensor is that it can be operated in such a way that the temperature-dependence of the output signal is virtually zero, eliminating the need for temperature control circuitry in all but the most exacting applications. The circuitry needed to operate the sensor is simple. Calibration is straightforward and once this has been done, the oxygen content of a gas mixture can be measured to an accuracy better than 2 mbar. Table 1 (page 220) gives additional data on the sensor.

The sensor's wide operating temperature range and ruggedness make it ideal for:

- analysing the exhaust gases of industrial burners and car engines
- controlling furnace atmospheres
- high-efficiency self-controlling domestic oil-fired and gas-fired boilers.

In flue gas analysis, an advantage of an oxygen sensor is that it can be used both to measure and to control the efficiency of combustion.

\* versions for use in gases up to 700 °C are available.

## OPERATING PRINCIPLE OF EXISTING SENSORS

Most oxygen sensors make use of one of two properties of stabilised zirconium oxide, ZrO<sub>2</sub>, namely:

- at high temperatures, ZrO<sub>2</sub> is a solid electrolyte for oxygen
- and
- when the partial pressures on each side of a ZrO<sub>2</sub> disc are unequal, a voltage (Nernst voltage) is generated across it.

## Oxygen sensors using Faraday's Law

At about 700 °C, stabilized zirconium oxide is a solid electrolyte for oxygen. A ZrO<sub>2</sub> disc with porous electrodes connected to a d.c. current source can therefore transport oxygen ions from the ambient through the disc, liberating at the anode an amount of oxygen proportional to the charge transported, which according to Faraday's First Law of Electrolysis is:

$$N = \frac{it}{zF}$$

where N is the number of moles of oxygen transported in t seconds by a constant current i, z is the ionic valence of oxygen (4) and F is the Faraday constant 96 487 C/mol.

In sensors using Faraday's Law, a  $ZrO_2$  disc is attached to a porous disc of known leakage. The current needed to maintain a constant oxygen transport through the  $ZrO_2$  disc is a measure of the surrounding oxygen pressure.

A disadvantage of this type of oxygen sensor is the requirement for very accurate oxygen dosing or a 'calibrated leak'. Furthermore, both dose rate and leakage are very dependent on temperature, the gases in the system and on the system cleanliness.

**Oxygen sensors using Nernst's Law**

Sensors that make use of Nernst's Law also employ a  $ZrO_2$  disc. When the oxygen partial pressures on each side of the disc are unequal, the voltage generated across the disc,  $V_s$ , is proportional to the logarithm of the ratio of the two partial pressures:

$$V_s = \frac{RT}{zF} \ln (p_1/p_2)$$

where:

$V_s$  is the voltage generated across the disc (the Nernst voltage)

R is the universal gas-constant (8,314 J/mol K)

T is the absolute temperature of the gas (K)

$p_1$  is the higher of the two oxygen partial pressures  $p_1$  and  $p_2$  on each side of the disc.

Sensors of this type require a reference pressure. Often atmospheric pressure is used as the reference, but variations in this and the relative humidity of the atmosphere limit the accuracy of this type of sensor.

**A NEW OXYGEN SENSOR**

The new sensor uses Faraday's First Law and Nernst's Law simultaneously, overcoming the drawbacks of conventional oxygen sensors. For example, the new sensor doesn't require a reference gas, accurate dosing or a calibrated leak.

**CONSTRUCTION**

As Figs 1 and 2 show, the sensor consists of two identical  $ZrO_2$  discs with porous platinum electrodes and a platinum ring which enclose a small chamber. One disc is used as a reversible pump for oxygen ions by connecting it to a reversible constant-current source (the reason why the pump is reversible will become apparent presently). The other is used as an oxygen partial pressure sensor, generating a Nernst voltage proportional to the logarithm of the ratio of the oxygen partial pressure in the chamber to that outside.

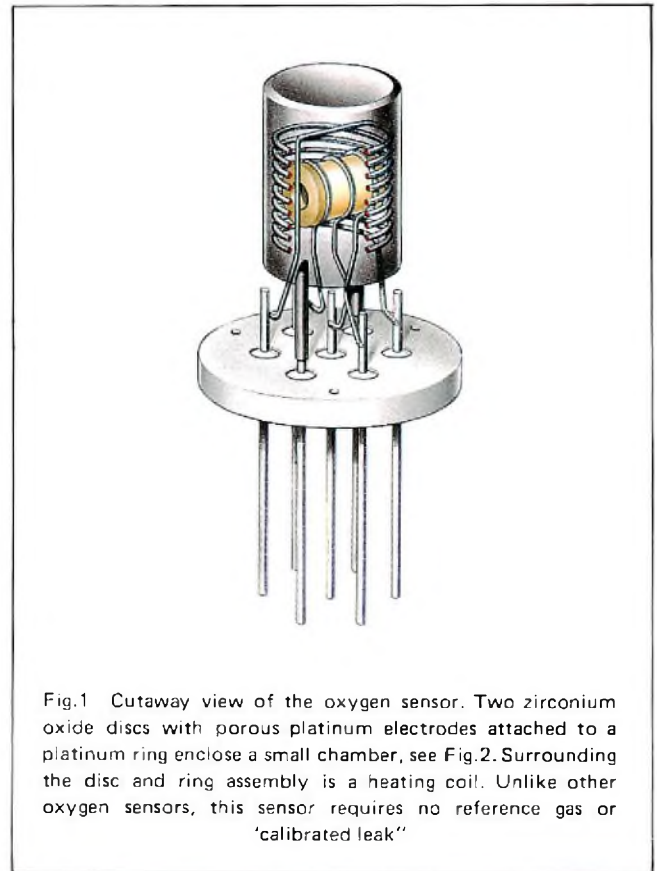


Fig.1 Cutaway view of the oxygen sensor. Two zirconium oxide discs with porous platinum electrodes attached to a platinum ring enclose a small chamber, see Fig.2. Surrounding the disc and ring assembly is a heating coil. Unlike other oxygen sensors, this sensor requires no reference gas or "calibrated leak"

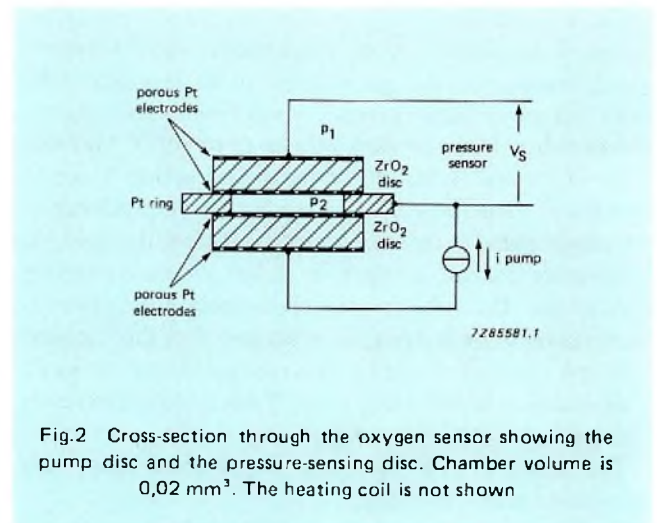


Fig.2 Cross-section through the oxygen sensor showing the pump disc and the pressure-sensing disc. Chamber volume is 0,02 mm<sup>3</sup>. The heating coil is not shown

The ring and disc assembly is surrounded by a heating coil used to maintain the  $ZrO_2$  at 700 °C, keeping the internal resistance of the ion pump low and constant, irrespective of the surrounding gas temperature.

The platinum electrodes catalyse the ionization and re-combination of oxygen in both the gas mixture whose pressure is to be measured and the chamber.

A feature of the sensor is its small size, just 17,5 mm long (excluding leads) and its maximum width, less than 10 mm. The mass of the sensor is 1,2 g.

**OPERATION**

Assume that the sensor is at operating temperature and that the oxygen partial pressure in the chamber is  $p_{2\text{ high}}$  and that of the gas to be measured is  $p_1$ . The ratio of these pressures as a function of the Nernst voltage  $V_1$  generated across the sensing disc is from Nernst's Law:

$$p_{2\text{ high}}/p_1 = \exp(-4FV_1/RT) = c_1 \text{ say.} \quad (1)$$

The constant-current ion pump is now turned on so as to pump oxygen out of the chamber. The amount of oxygen transported ( $N$  moles) is proportional to the charge supplied by the pump (Faraday's First Law):

$$N = \frac{it}{4F} \quad (2)$$

The fall in pressure in the chamber (volume  $v$ ) due to pumping out  $N$  moles of oxygen at temperature  $T$  is:

$$(p_{2\text{ high}} - p_{2\text{ low}}) = RTN/v \text{ (from the Gas Laws)} \\ = RTit/4Fv \text{ from Eqn. (2).} \quad (3)$$

And the ratio of the pressure in the chamber,  $p_{2\text{ low}}$ , to the unknown pressure  $p_1$  is indicated by the Nernst voltage  $V_2$  ( $V_2 > V_1$ ) where:

$$p_{2\text{ low}}/p_1 = \exp(-4FV_2/RT) = c_2 \text{ say.} \quad (4)$$

From equations (1), (3) and (4):

$$p_1 = \frac{RT}{4Fv(c_1 - c_2)} it. \quad (5)$$

Equation (5) shows that the unknown oxygen partial pressure  $p_1$  is proportional to the charge ( $it$ ) transported by the pump in time  $t$ . For a constant pump current and a constant temperature,  $p_1$  is simply proportional to the time to pump between any two pressures  $p_{2\text{ high}}$  and  $p_{2\text{ low}}$ , a parameter that can be measured easily. The temperature dependence of  $c_1$  and  $c_2$  can be compensated by appropriate choice of operating conditions.

One could continue to evacuate the chamber, however the minimum allowable chamber pressure will eventually be reached. A suitable method of operation which provides a continuous output is to operate the sensor between two reference voltages, reversing the pump each time the output of the sensor reaches one of the references. In theory, any two voltages can be used, as defined above, because from these and a knowledge of the charge transported, the partial pressure can be calculated, see Eqn.(5). The choice of references is described in the next section.

Suppose the constant-current ion pump is reversed when the output voltage of the sensor is  $V_2$ , see Fig.3. The pump transports oxygen into the chamber, increasing the pressure there and causing  $V_s$  to decrease. When  $V_s$  falls to  $V_1$  say, the pump is reversed again and the cycle repeated, generating a voltage waveform whose period,  $t_p$  is proportional to the unknown oxygen partial pressure  $p_1$  to be measured.

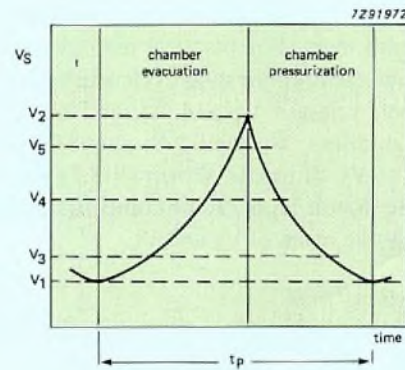


Fig.3 Nernst voltage as a function of time for a constant pump current and constant ambient temperature. The period of the Nernst voltage generated ( $t_p$ , set by levels  $V_1$  and  $V_2$ ) is proportional to the pressure surrounding the sensor. In practice, use is made of three additional preset voltages  $V_3$ ,  $V_4$  and  $V_5$  in the measurement of the period. This is to overcome the effect of an electric double layer formed at the platinum-electrolyte interface

In this description, oxygen was pumped out of the chamber. Clearly, the same relationship between  $p_1$  and the pumping time can be derived if oxygen is pumped into the chamber.

**PRACTICAL CONSIDERATIONS**

Let's now assign values to  $V_1$  and  $V_2$  at which the ion pump is reversed. In theory, any two values can be used, in practice,  $V_1$  and  $V_2$  are chosen:

- to eliminate the effect of an electric double layer in the  $ZrO_2$  discs formed by space charges
- for the best response time for the application
- to eliminate the temperature-dependence of Nernst's Law and the Gas Laws.

**Compensating for the electric double layer**

Not all the charge supplied by the current source contributes to a pressure change in the chamber; some is absorbed by an electric double layer formed at the platinum-electrolyte interface as the current source is reversed. The effect of the double layer is particularly noticeable:

- at extremes of pressure
- near the pump reversal points.

At extremes of pressure, substantially more charge is needed to change the pressure in the chamber, reducing the accuracy of the sensor. To compensate for this effect, the working chamber pressure range should be about 1% to 10% of the ambient pressure.

To overcome the influence of the double layer near the pump reversal points, pumping times should be measured, not between the reversal points, but for Nernst voltages well away from them. For practical reasons, two measurements are made each compression cycle and each evacuation cycle, between voltages  $V_3$  and  $V_4$ , and  $V_4$  and  $V_5$ , see Fig.3. As a guideline,  $V_1$  should be about 90% of  $V_3$ ;  $V_2$  about 110% of  $V_5$ . It can be shown (Ref.1) that the effect of the electric double layer can be compensated when  $V_4$  is approximately the mean of  $V_3$  and  $V_5$ .

**Response time**

When operated as described, the response time of the sensor is about one period of  $V_s$ , see Table 1. Therefore,  $V_1$  and  $V_2$  should be close to each other for a fast response when measuring high pressures. This will not affect the accuracy of the sensor significantly, because the effect of offset variations at high pressures is small.

**TABLE 1**  
Brief data on the oxygen sensor

ambient gas	virtually all exhaust gases of combustion, and many gas mixtures <sup>1)</sup>
ambient gas temperature range	0 to +500 °C
ambient gas flow rate	up to 10 m/s
measuring range of oxygen partial pressures	1 mbar to several bar
accuracy	±2 mbar <sup>2)</sup>
calibration	in air; no reference gas needed
sensor output voltage $V_s$	$0.0495T \log(p_1/p_2)$ mV <sup>3)</sup>
operating output voltage $V_s$	25 to 110 mV range (typ.)
response time	one period of $V_s$
period of $V_s$	
at 200 mbar	1 s (typ.)
at 20 mbar	100 ms (typ.)
warming-up time	45 s (typ.)
supplies	
oxygen pump	35 µA (typ.) constant-current source
heater, in still gas	1,8 A; 10 W (typ.)

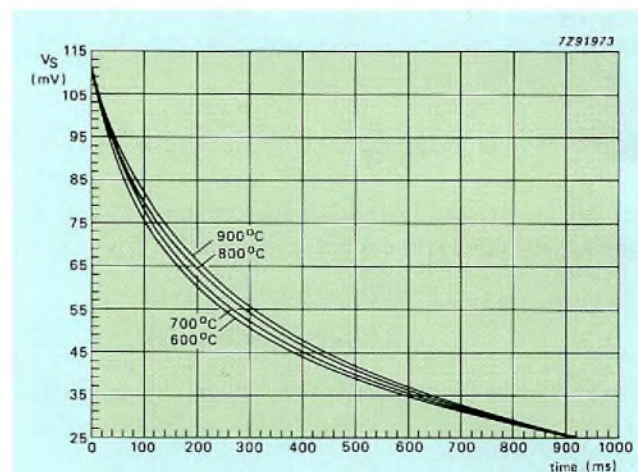
<sup>1)</sup> Halides, lead and particulate matter can degrade performance over long periods of operation. Reducing atmospheres may in time impair the catalytic effect of the platinum electrodes.

<sup>2)</sup> with OMA21 measuring assembly.

<sup>3)</sup> T is the sensor temperature in K;  $p_1$  is the higher of the pressures  $p_1$  and  $p_2$  on each side of the pressure-sensing disc.

**Compensating for temperature-dependence**

That the period  $t_p$  of the Nernst voltage is temperature-dependent can be seen in Eqn.(5). However, the temperature-dependence is such that under certain operating conditions, the combined temperature-dependence of Nernst's Law and the Gas Laws is virtually zero, see Fig.4. A similar effect can be observed for different voltage pairs  $V_1$  and  $V_2$ . In Ref.1, values of  $V_1$  and  $V_2$  that correspond to a zero temperature coefficient are given.



**Fig.4** Reversing the sensor's current pump at Nernst voltages of about 25 mV and 115 mV largely eliminates the temperature-dependence of the period of the Nernst voltage generated. Refinement of this approach gives zero temperature coefficient.  $i = 40 \mu A$ ;  $p_1 = 208$  mbar

Table 2 lists values of  $V_3$ ,  $V_4$  and  $V_5$  that will give a zero temperature coefficient (to a 1st-order approximation) and a linear response. The values are for a sensor operating at 750 °C, a pumping current of 40 µA, an equilibrium pressure of 0,316 mbar and  $V_4 = (V_3 + V_5)/2$ . The cycle time,  $t_p$ , is for an oxygen pressure of 50 mbar. The remaining relative error in pressure readings due to temperature is plotted in Fig.5 for 700 °C, 750 °C and 800 °C.

**TABLE 2**  
Output voltages  $V_3$ ,  $V_4$  and  $V_5$  for a linear output and zero temperature coefficient

$V_3$ (mV)	$V_4$ (mV)	$V_5$ (mV)	$t_p$ (ms)	Relative error in % at		
				650 °C	750 °C	850 °C
60,38	66,38	72,38	125	-1,23	0	-1,53
57,72	66,72	75,72	163	-1,23	0	-1,53
54,38	67,38	80,38	214	-1,22	0	-1,51
51,28	68,28	85,28	266	-1,20	0	-1,49
48,40	69,40	90,40	317	-1,19	0	-1,47
45,11	71,11	97,11	382	-1,16	0	-1,43
42,15	73,15	104,15	447	-1,14	0	-1,39
39,50	75,50	111,50	511	-1,12	0	-1,34
36,71	78,71	120,71	586	-1,10	0	-1,27

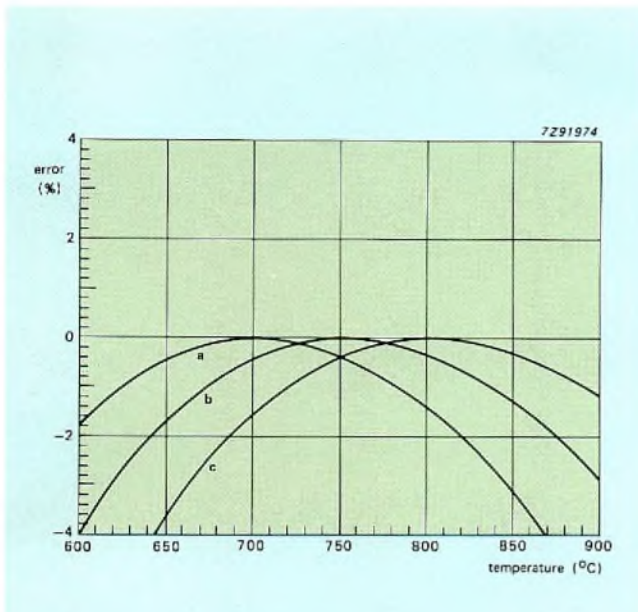


Fig.5 Output error (normalized) as a function of temperature for a sensor operating in the zero temperature coefficient mode optimized for operating at (a) 700°C, (b) 750°C and (c) 800°C.  $p_1 = 208$  mbar.

At 700°C,  $V_3 = 49$  mV;  $V_4 = 68$  mV;  $V_5 = 89$  mV.  
 At 750°C,  $V_3 = 52,5$  mV;  $V_4 = 71,5$  mV;  $V_5 = 92,5$  mV.  
 At 800°C,  $V_3 = 56$  mV;  $V_4 = 75$  mV;  $V_5 = 96$  mV.

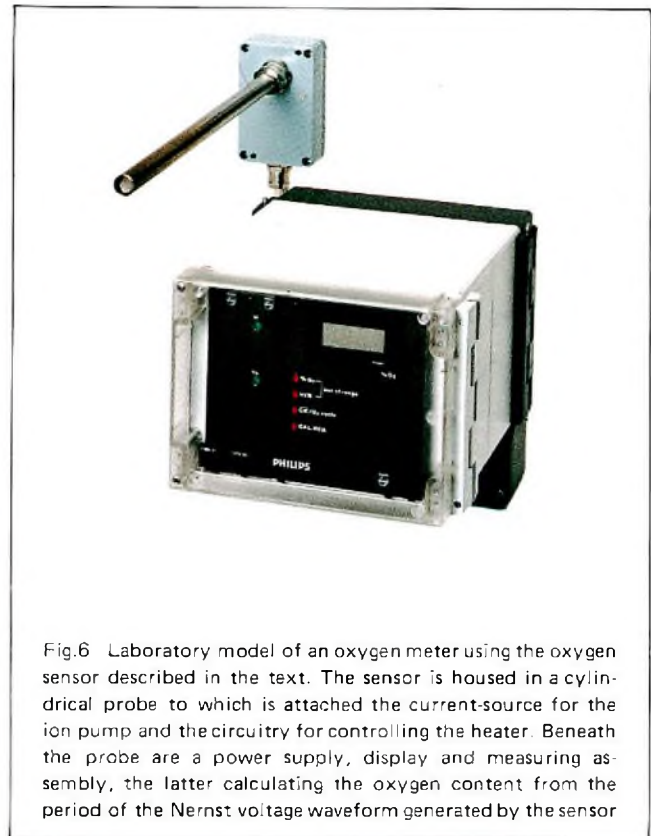


Fig.6 Laboratory model of an oxygen meter using the oxygen sensor described in the text. The sensor is housed in a cylindrical probe to which is attached the current-source for the ion pump and the circuitry for controlling the heater. Beneath the probe are a power supply, display and measuring assembly, the latter calculating the oxygen content from the period of the Nernst voltage waveform generated by the sensor

The voltages  $V_3$  and  $V_5$  in Table 2 correspond to pressures in the chamber between 1% and 10% of the ambient pressure. Note that the accuracy of the sensor improves for longer response times.

The error due to temperature variations is less than 1,6% between 650°C and 850°C. This compares favourably with errors due to variations of ambient temperature of tens of percent for conventional zirconia sensors calibrated against air.

**CONTROL CIRCUITRY**

The oxygen sensor can be readily incorporated in an oxygen meter such as that shown in Figs 6 and 7 which comprises:

- OPA20/22 probe assembly
- OMA21 measuring assembly used to control the sensor and to calculate the oxygen content from the Nernst voltage waveform
- OPS20/22 power supply.

If the zero temperature coefficient procedure is observed, additional circuitry to measure and control temperature is unnecessary in most cases.

Measurements of the Nernst voltage and reversal of the oxygen pump is controlled by a microcomputer and a voltage comparator. An 8-bit binary output is obtained by measuring the period of the Nernst voltage, comparing with a crystal-controlled timing reference and multiplying by an appropriate calibration factor.

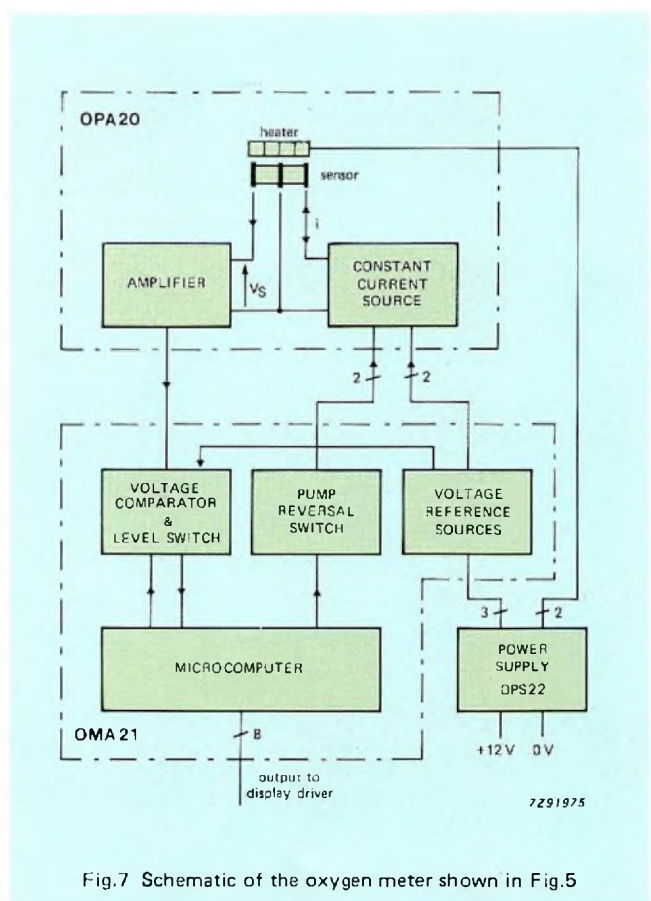


Fig.7 Schematic of the oxygen meter shown in Fig.5

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1. FRANX, C. 1985. A dynamic oxygen sensor with zero temperature coefficient. *Sensors and Actuators* 7, 263-270.
2. ZrO<sub>2</sub> oxygen sensor. Elcoma Technical Publication, ordering code 9398 021 60011.
3. OSU21: Dynamic oxygen sensor unit. Ordering code 9398 328 90011. This leaflet introduces the sensor, its power supply and measuring circuitry.

# State-of-the art ICs simplify SSB-receiver design

ROBERT ZAVREL

Single-sideband (s.s.b.) transmission offers many advantages over f.m. and full-carrier double-sideband modulation: more efficient spectrum use, better signal-to-noise ratios at low signal levels, and better transmitter efficiency. Unfortunately, s.s.b. systems have historically required the use of expensive multipole filters. Today, however, some new r.f. and digital ICs allow you to circumvent the need for these filters. You can use these ICs to good advantage in developing a cost-effective s.s.b. receiver.

Good s.s.b.-receiver design requires some knowledge of the three basic methods of single-sideband generation. All three methods use a balanced modulator to produce a double-sideband, suppressed-carrier signal. The undesired sideband is then removed by high-Q multipole filters (the *filter method*), by phase and amplitude nulling (the *phasing method*), or by a variation of the phasing method called the *Weaver method*. The reciprocal of the generator functions is used to develop sideband detectors.

Generators accept audio input and produce the s.s.b. signal; detectors receive the s.s.b. signal and reproduce the audio signal. It's worth noting that all three methods of removing a sideband are complementary; an s.s.b. signal produced by the Weaver method can be reproduced by the phasing method, etc. The sideband signal is typically in the r.f. range, so you can amplify it and apply it to an aerial or use it as a subcarrier.

## FILTER METHOD

In generation and detection using the traditional filter method, the generator (Fig.1(a)) produces a double-sideband signal, and the balanced modulator nulls the carrier. A high-Q crystal-type bandpass filter then removes the undesired sideband. The transmit mixer then converts the s.s.b. signal to the desired output frequency.

The detection scheme (Fig.1(b)) simply reverses the operation. A receive mixer converts the input frequency to the i.f. The filter has a narrow response and passes only the required s.s.b. bandwidth. The product detector demodulates the signal.

This s.s.b. signal-generation method has one major drawback. The filter is tuned to one fixed frequency. As a result, you'll need to incorporate a number of transmit and receive mixers for multi-frequency operation.

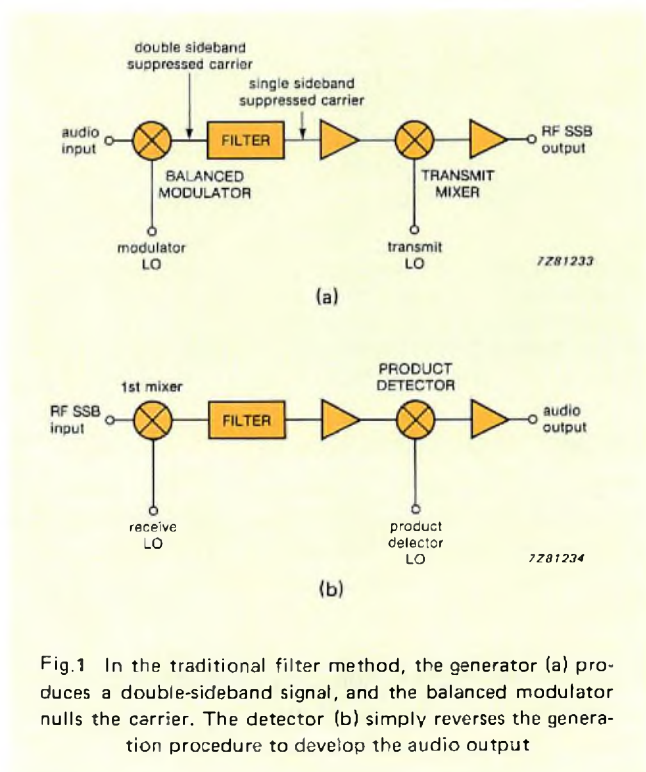


Fig.1 In the traditional filter method, the generator (a) produces a double-sideband signal, and the balanced modulator nulls the carrier. The detector (b) simply reverses the generation procedure to develop the audio output



**PHASING METHOD**

Figure 2 shows block diagrams of generator and detector circuits for the phasing method. In the detector (Fig.2(a)), the input signal is fed in phase to two r.f. mixers. A local oscillator (LO) supplies a second signal to the mixers in quadrature. Summing the differentiated output of one of the mixers with the output of the other produces an audio output.

In most cases, the mixer's output will be in the audio passband (300 to 3000 Hz). Running the passband through the differentiator circuit imposes a 90° phase shift over more than three octaves. As a result, it's quite difficult to use the phasing method for voice-band s.s.b. applications.

The phasing method uses a generator (Fig.2(b)) that duplicates the circuit elements of the detector. Note that in the generator, the differentiator (phase shifter) is located between the audio input and the mixer. In the generator circuit, a divide-by-4 flip-flop provides the  $\sin(yt)$  and  $\cos(yt)$  signals for the mixer. As a result, the clock signal's frequency must be four times the r.f. output frequency.

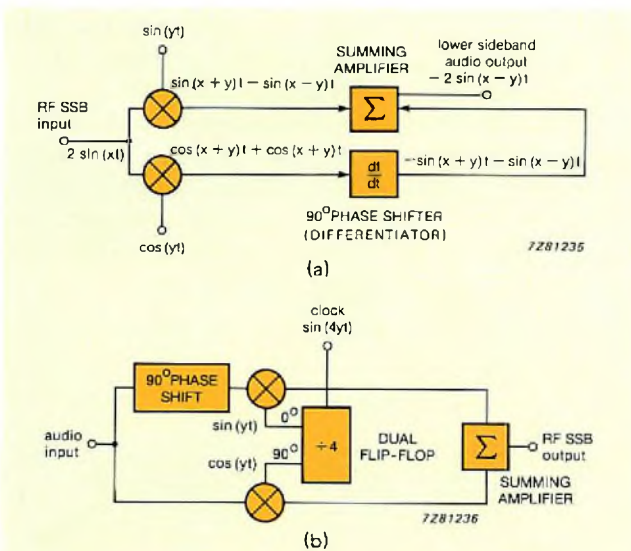


Fig.2 The input signal feeds in phase to two r.f.mixers in the phasing-method detector (a). A local oscillator supplies a second signal to the mixers in quadrature. In the generator (b), a divide-by-4 flip-flop provides the  $\sin(yt)$  and  $\cos(yt)$  signals for the mixer

**Versatility in datacomm systems**

You can use the phasing method for FSK, PSK, and quadrature PSK datacomm systems. For FSK, for example, you can alternately key two discrete frequencies to correspond to ones and zeros. By tuning the receiver at the halfway point, you can let these two frequencies represent the upper- and lower-sideband signals. When you implement rectification and filtering, you can use simultaneous upper/lower-sideband detection to drive both clock inputs of a flip-flop. This type of FSK receiver can have better sensitivity characteristics than traditional f.m. receivers. In

addition, the scheme uses discrete frequencies, so you will not have to use a broadband phase shifter, simple discrete RC networks will suffice.

**THE WEAVER METHOD**

The Weaver method (Fig.3) eliminates the difficulty of having to maintain an accurate broadband phase shift in voice communications systems. A derivation of the phasing technique, the Weaver method does require more circuit elements (four mixers instead of two, for example) in both the generator (Fig.3(a)) and the detector (Fig.3(b)).

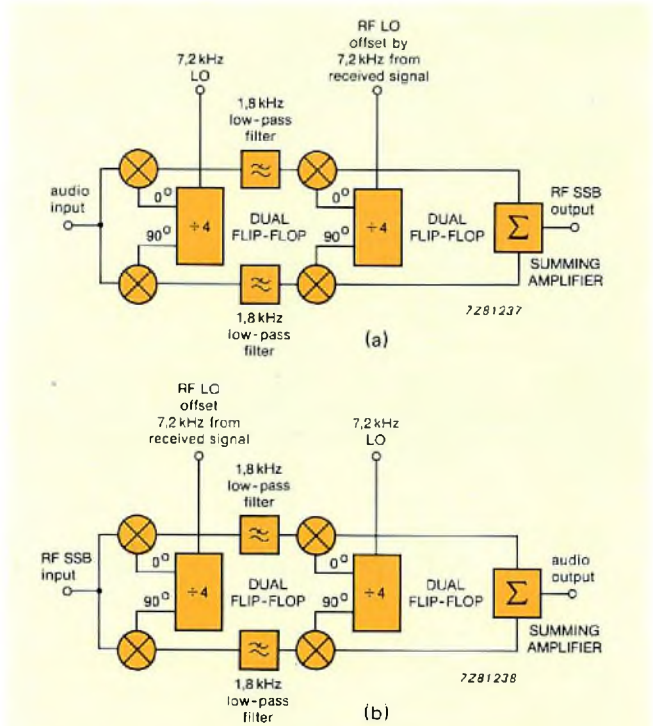


Fig.3 There's no need to maintain accurate phase shift when using the Weaver method in voice systems. It does require more circuit elements than the phasing method — four mixers in both the generator (a) and the detector (b), for example

**Low-frequency subcarrier vs phase shift**

The basic difference between the two schemes is that the Weaver method uses a low-frequency (1,8 kHz) subcarrier in quadrature, rather than a broadband, 90° audio phase shift. The desired sideband folds over the 1,8 kHz subcarrier, and its energy appears between 0 and 1,5 kHz. The undesired energy appears at least 600 Hz away (above 2,1 kHz). As a result, you can reject the undesired sideband with a simple low-pass filter.

It's much easier to design a filter with a steep low-pass response than it is to achieve the accurate phase and amplitude balance that the phasing method requires. As a result, the Weaver method will have much better sideband rejection than that obtainable with the phasing method.

## QUADRATURE DUAL MIXER CIRCUITS

Once you've chosen the manner in which you wish to develop the s.s.b. signal, you're ready to add the other circuits that help complete an s.s.b. receiver. You'll need quadrature-dual-mixer circuits for the first stage when using the Weaver method. Figure 4 illustrates two methods of obtaining quadrature LO signals for dual-mixer applications. Both circuits are inherently broadband circuits; they are far more flexible than designs using passive LC circuits (which fail to maintain a quadrature relationship when the operating frequency changes), and they do not require adjustments. In addition, the circuits shown in Fig.4 are not limited to s.s.b. applications; you can also apply them in FSK, PSK, and quadrature-PSK digital communications systems.

In Fig.4(a), a divide-by-4 dual flip-flop generates all four quadrature signals. Most of the popular dual flip-flops will work in this circuit; the choice depends on the application. This example uses the CMOS HEF4013B, which consumes little power and maintains excellent phase integrity at clock rates up to several megahertz. As a result, it will work quite well at the ubiquitous 455 kHz i.f.

For higher clock rates (up to 120 MHz), the fast-TTL 74F74 is a good choice for the flip-flop. Tests on this IC at 30 MHz show good results – greater than 20 dB s.s.b. rejection. At frequencies in the neighbourhood of 5 MHz, use of the 74F74 will result in sideband rejection of nearly 40 dB. The ultimate low-frequency rejection is mainly a function of the audio phase shifter. You can improve performance by using resistors and capacitors with tighter tolerances in the phase shifter.

### Match clock and operating frequencies

The circuit shown in Fig.4(b) illustrates a different technique for producing a broadband quadrature phase shift for the LO. In this case, the clock and operating frequencies are identical, an advantage when compared with the flip-flop circuit, because you don't need the high-speed components. Phase accuracy, however, is more difficult to achieve.

A phase-locked loop (PLL) will maintain a quadrature phase relationship when the loop is closed and the VCO voltage is 0 V. The d.c. amplifier enhances the accuracy of the quadrature output by providing gain for the VCO control circuit. PLL circuits tend to be noisy, however, which can be a problem. Sideband noise is troublesome in both s.s.b. and f.m. systems, but s.s.b. transmission is less sensitive to phase noise in the LO than f.m.

After developing the LO signals, you have to provide some drive circuitry. The circuit shown in Fig.5(a) provides an effective means of driving the 74F74 (or other TTL gates) with an analog LO. Assuming you're using 50  $\Omega$  input and output impedances, the NE5205 amplifier provides approximately 20 dB of gain from d.c. to 450 MHz.

External-component requirements are minimal. The 1 k $\Omega$  value of the resistor is about optimum for pulling the input voltage down near the logic threshold. A 0 dBm

output level will drive the NE5205 and 74F74 to 120 MHz. By cascading two NE5205s, you can increase the sensitivity without sacrificing the wide bandwidth.

Figure 5(b) shows the interface circuitry between the 74F74 and the NE602 mixers' LO ports. The total resistance establishes a conservative current drain (about 10 mA) from the 74F74 outputs; the voltage-divider tap optimizes the operation of the NE602s. The low signal-source impedance helps maintain phase accuracy. A miniature ceramic capacitor should be used for d.c. isolation.

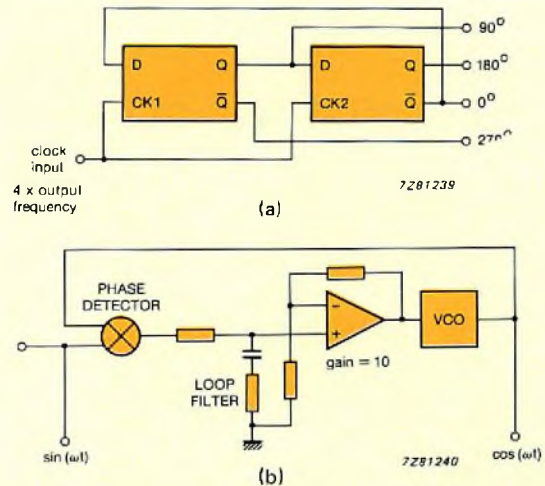


Fig.4 You need quadrature dual mixers whether you're using the phasing or the Weaver method. The mixer in (a) maintains good phase integrity at clock rates up to several megahertz. Clock and operating frequencies are equal in the mixer circuit (b), which provides an advantage over the flip-flop design

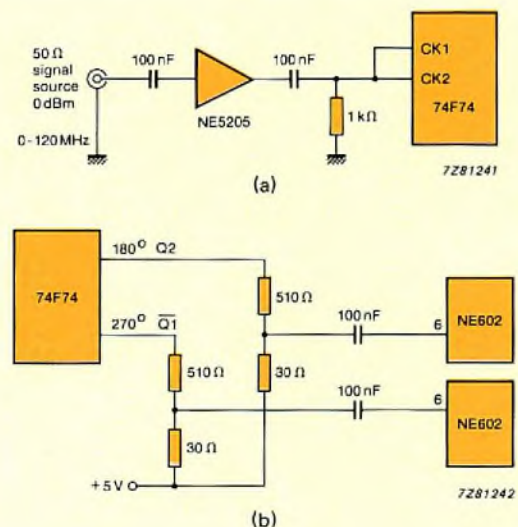
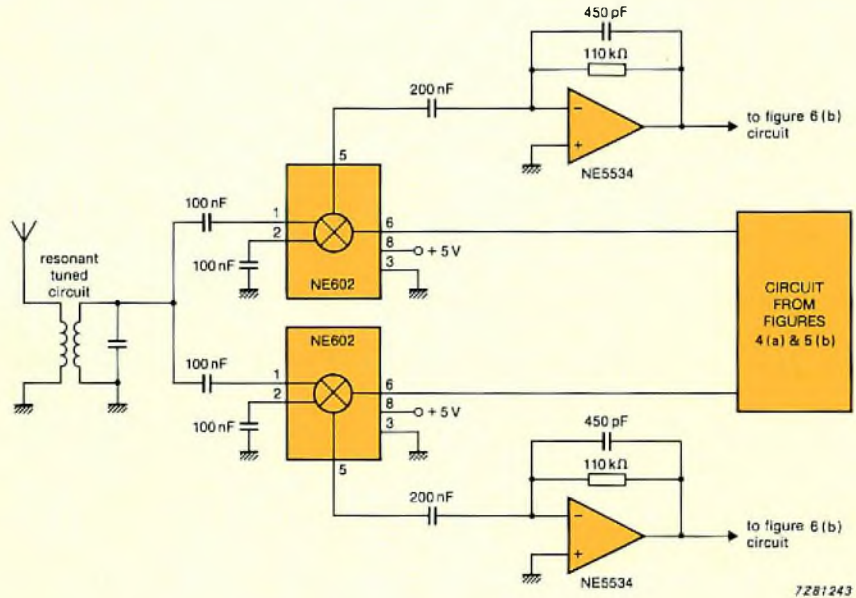
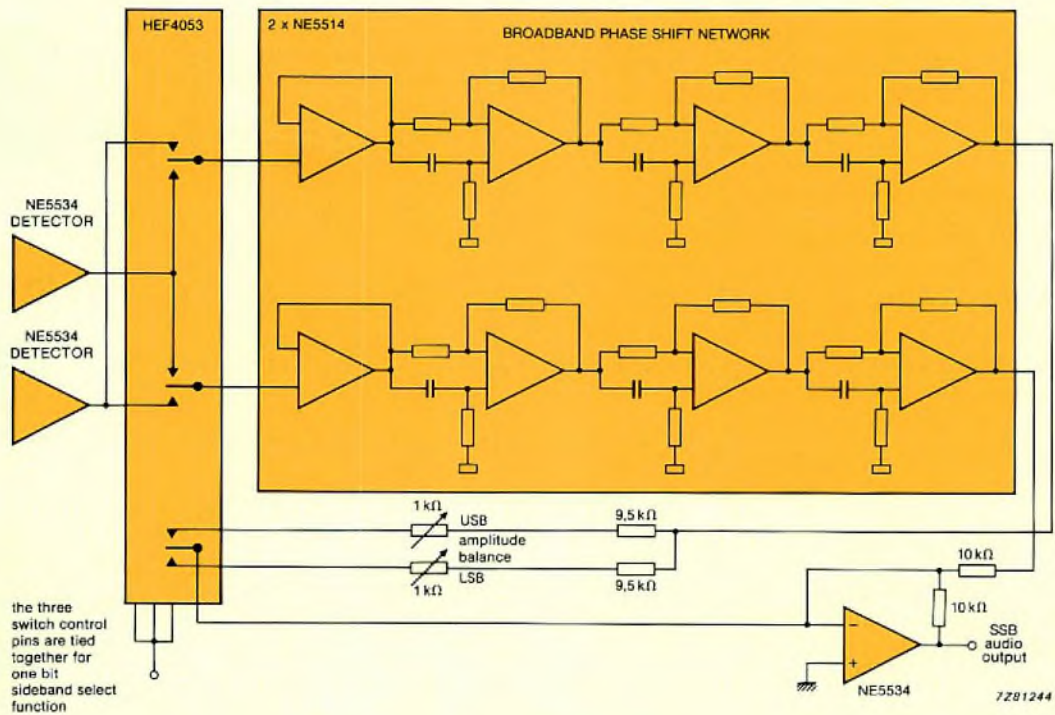


Fig.5 You can effectively drive the 74F74 and other TTL gates with the circuit shown in (a). The total resistance in the interface circuit (b) establishes a conservative current drain (approximately 10 mA) from the 74F74, and the divider tap optimizes NE602 operation



(a)



(b)

Fig.6 You can reliably obtain 35 dB rejection levels using this circuit in direct-conversion applications. Add an inexpensive 2-pole crystal or ceramic filter and you will realize the required 70 dB sideband rejection levels

## AMPLIFYING AND SWITCHING FUNCTIONS

The use of active mixers like the NE602 will provide conversion gain – typically 18 dB. In more traditional applications, which use passive diode-ring mixers, there is a conversion loss – typically 7 dB. Consequently, the detected audio level will be about 25 dB higher when you use the active-mixer approach. This means that you can significantly reduce the noise and gain requirements of the first audio stage and eliminate microphony. This is a great advantage in direct-conversion receivers.

Traditional direct-conversion-receivers use passive audio LC filters at the mixer output and low-noise discrete JFETs or bipolar transistors in the first audio stages. Because of the conversion loss associated with passive mixers, these amplifiers must have very high audio sensitivity, so they readily respond to mechanical vibration and produce microphony. The conversion gain available from an active mixer allows you to use a simple NE5534 opamp stage (Fig.6), set up as an integrator to eliminate ultrasonic and r.f. instability.

You can use an HEF4053B CMOS-analog switch to provide the sideband-select function. This triple double-pole switch drives the phase network and engages one of two amplitude-balance potentiometers – one for each sideband. The buffer opamp shown with the two sideband-select sections reduces the total harmonic distortion, maintains amplitude integrity, and prevents changes in the resistance values of the filter network due to switch resistance. If the gain distribution within both legs of the receiver is consistent, you can eliminate the amplitude-balance potentiometers in less demanding applications.

## PHASE SHIFTING

In the phasing method, the broadband audio phase shifter (differentiator) is a critical stage. The analog all-pass differential phase-shift circuit shown in Fig.6 uses one of several available broadband phase-shift techniques. When you

short the inputs together and drive them with a microphone circuit, the outputs will be 90° out of phase over the 300 to 3000 Hz band. This splitting and phase-shift action is required for phasing-generator operation.

For phasing demodulation, the circuit filters receive their inputs from the two audio detectors. The filter outputs are then summed to null the undesired sideband and reinforce the desired sideband.

The filter circuit uses standard 1% resistors and capacitors. You can improve gain tolerances by using 0,1% laser-trimmed integrated resistors. To maximize audio performance, it's best to use polystyrene, polypropylene, or Mylar capacitors.

Two quad opamps (NE5514s in this case) fit nicely into Fig.6's approach. One section of each quad IC serves as a switch buffer, and the other three form a phasing section. The quad opamps also provide linearity and high dynamic range. These characteristics are much easier to achieve at audio frequencies than they are at common intermediate frequencies. Audio i.f. systems have other advantages too: they have no LC-tuned circuits, they have no need for shielding, and power requirements are low.

## PUTTING IT ALL TOGETHER

Specification for high-quality s.s.b. radios call for sideband rejection greater than 70 dB. Using the circuit shown in Fig.6, you can reliably obtain rejection levels of 35 dB. Add an inexpensive 2-pole crystal or ceramic filter, and you can meet the 70 dB requirement.

Figure 7 shows a complete s.s.b. receiver that uses the phasing-filter technique. The block labelled "direct-conversion phasing s.s.b. receiver" is Fig.6's circuit. The aerial connects (via a bandpass filter) directly to the inputs of the NE602s.

The direct-conversion phasing s.s.b. receiver circuit has a 10 dB signal/noise sensitivity of 0,5  $\mu$ V and a dynamic range of about 80 dB. Single-tone audio harmonic distortion is less than 0,05%, and 2-tone intermodulation products are

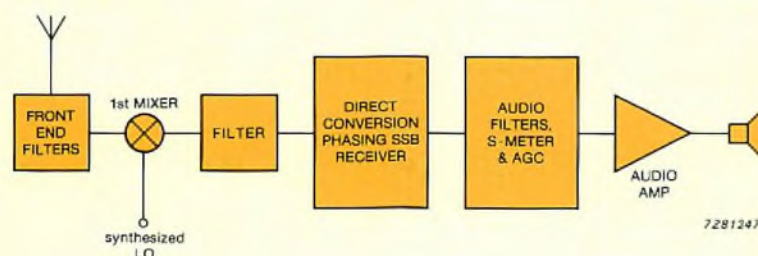


Fig.7 Using the phasing filter technique, you can design a complete, yet simple, SSB receiver. The antenna connects directly (via a bandpass filter) to the inputs of the NE602s' mixer stage

more than 55 dB down at r.f. input levels only 5 dB below the 1 dB compression point. The sideband rejection is about 38 dB at a 9 MHz operating frequency.

You can also use the same quadrature dual mixer in a Weaver-method receiver. Figure 8 shows an experimental Weaver receiver circuit. The subcarrier stage here can use HEF4066B CMOS analog switches to minimize power drain.

A 1,8 kHz subcarrier requires a 7,2 kHz clock frequency. In the Weaver-method circuit, a common 8,6864 MHz crystal combines with the HEF4060B oscillator and +512 circuit to provide the required clock signal. When you use switched-capacitor filters for the low-pass audio circuits, a single clock generator (with appropriate dividers) suffices for all circuit-timing signals.

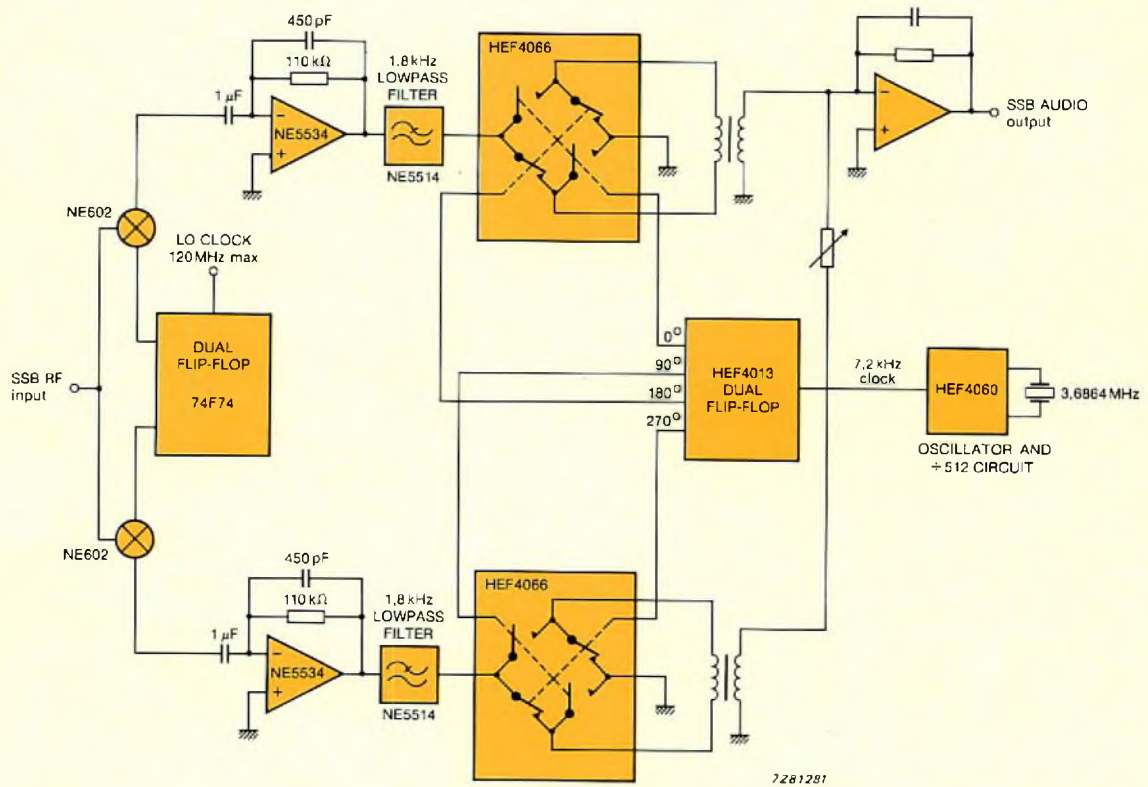


Fig.8 To minimize power drain, you can use HEF4066 CMOS analog switches in the subcarrier stage of this experimental Weaver receiver circuit

# Speech synthesis – the complete approach with the PCF8200

MENNO TEN HAVE

The PCF8200 is a CMOS integrated circuit for generating high quality speech from digital code. It is primarily for use in microprocessor-controlled systems where the speech code is stored in a separate memory.

In vehicle-information systems, telephony equipment, personal computers, annunciators and aids for the handicapped, the PCF8200 sets a new standard in digitally-synthesized voice output.

Like its predecessor the MEA8000, the PCF8200 uses vocal formant synthesis (a variation of linear predictive coding) for a very low bit rate, so only a small memory is needed to store the speech code. A programmable bit rate allows about 40 seconds of speech to be stored in a 64K memory.

A speech demonstration board (OM8200) with a very large vocabulary (up to 12 minutes speech) and a speech development system (OM8210) for use with personal computers are available. The latter performs all the functions required to generate speech codes for the PCF8200 and is described at the end of this article.

## Features of the PCF8200

- 5 kHz speech bandwidth
- male and female speech possible
- programmable speech rate
- low bit rate: 455 to 4545 bits/s
- CMOS technology
- operating temperature range  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- single 5 V supply
- stand-by power-saving mode
- I<sup>2</sup>C and parallel buses
- internal low-pass filter and 11-bit digital-to-analog converter.

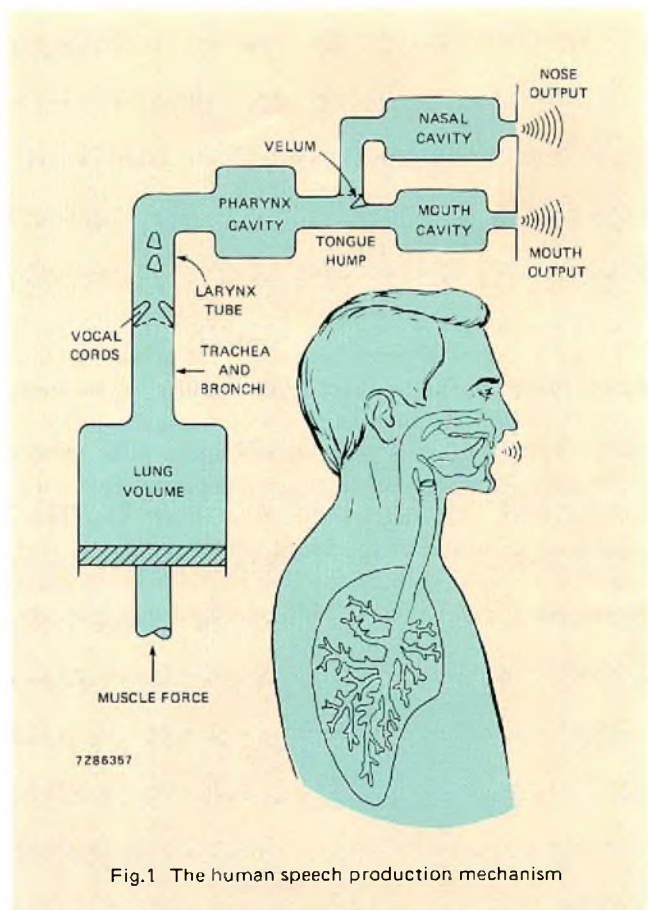


Fig.1 The human speech production mechanism

## PRINCIPLES OF FORMANT SYNTHESIS

A formant speech synthesizer such as the PCF8200 electronically models the human speech production mechanism, Fig.1. To produce speech, the lungs build up air pressure, opening the normally closed vocal cords. The pressure then starts to reduce, causing the vocal cords to close again. This

movement of the vocal cords imparts a periodic pulse train to the vocal tract, the frequency of which is referred to as 'pitch'. Sounds generated in this way for example the vowels 'A' and 'E' are commonly known as the voiced elements of human speech.

Besides the voiced elements, unvoiced or noise source elements are required to generate speech. The unvoiced elements are produced by exciting the vocal tract with the vocal cords slightly open, so that the air in the tract is turbulent. Sounds produced in this fashion are known as the sibilants.

Situated above the vocal cords are the pharyngeal, nasal and oral cavities which shape the spectrum of the sounds. The vocal tract, which can be thought of as an acoustic tube is almost closed by the vocal cords at one end, and open at the other where sound dispersion take place. The frequency response of such a tube with constant diameter is characterized by a number of equally-spaced resonances known as formants, see Fig.2.

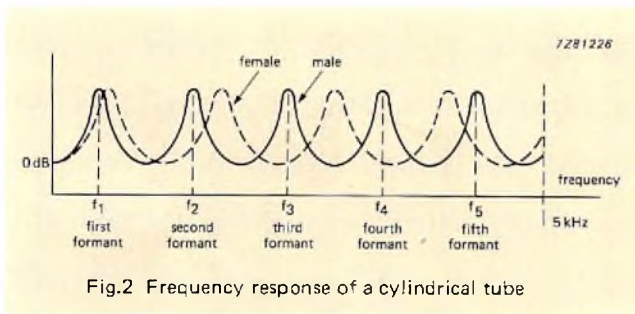


Fig.2 Frequency response of a cylindrical tube

Figure 3 shows a simplified electronic model of the human speech production mechanism similar to that used in the PCF8200. The voiced and unvoiced sounds of speech are represented by a periodic source and a noise source respectively. These are amplified, combined and fed to the formant filter that mimics the vocal tract. This filter consists of a cascade of five second-order resonators that individually model each of the five formants or resonant frequencies found within a 5 kHz speech bandwidth. By

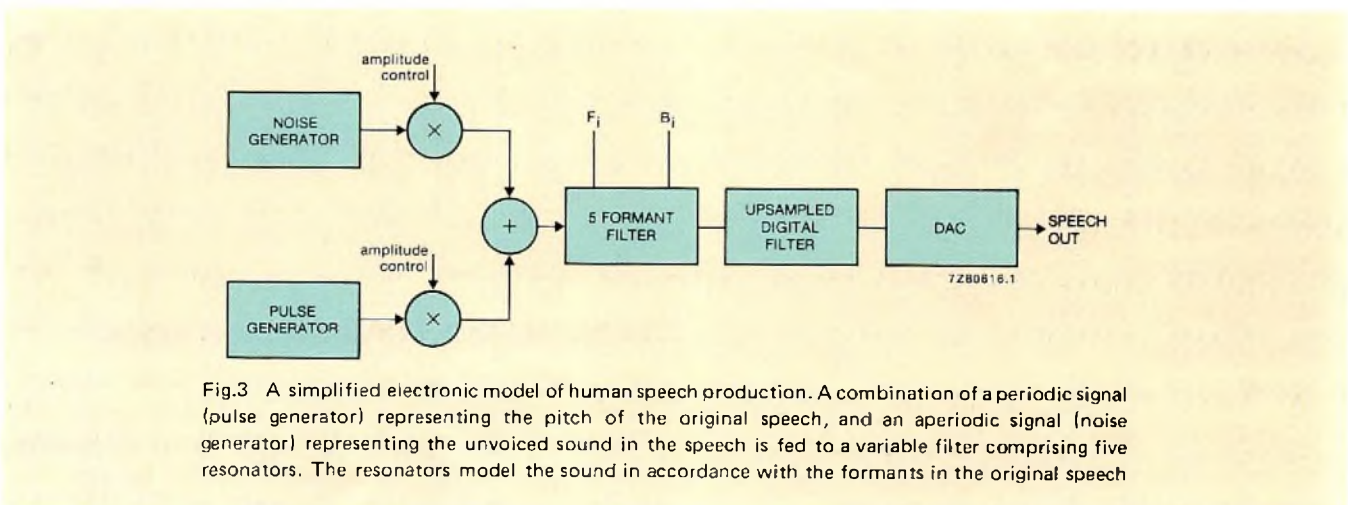


Fig.3 A simplified electronic model of human speech production. A combination of a periodic signal (pulse generator) representing the pitch of the original speech, and an aperiodic signal (noise generator) representing the unvoiced sound in the speech is fed to a variable filter comprising five resonators. The resonators model the sound in accordance with the formants in the original speech

altering the response of the filter and the amplitude of the periodic and noise sources, a good imitation of speech can be produced.

### REDUCING THE BIT RATE IN FORMANT SYNTHESIS

To create the data needed to make the PCF8200 synthesizer talk, a recording of the speech to be synthesized is analysed using our development system. During analysis, the recorded speech is divided into intervals called 'frames'. For each frame, the amplitude, pitch, formant frequencies and bandwidths are found. These are represented by thirteen parameters. To digitally store all this information then retrieve it later to produce synthesized speech would require an enormous memory and an extremely high bit rate. However, the data rate is reduced significantly by:

- limiting the number of values each parameter may take (quantization) and using coded speech parameters
- using interpolation to smooth the transition from one set of parameters to the next
- altering the frame duration.

Coded speech parameters which are converted to the absolute values by an on-chip look-up table reduce the data rate. In addition, for the pitch frequency, it isn't necessary to transmit the absolute value, only the differences between successive frames. Within the 5 kHz bandwidth of the PCF8200, male speech has five formants while female speech has only four, so the PCF8200 has two look-up tables. Interpolation is used to smooth frame transitions.

Another technique used to reduce the data rate is to alter the frame duration. For example, if the speech parameters change linearly, the frame length can be up to five times the standard frame duration (which can also be set to suit the characteristics of the speech). In total, the speech frame can be altered from 8,8 ms (4545 bits/s) to 88 ms (454 bits/s). A typical average bit rate is 1500 bits/s.

### THE PCF8200

The synthesizer can be divided into three sections:

- microcomputer interface/control
- formant synthesizer
- output stage.

### Microcomputer interface and control

Speech code files from an external memory are transferred to the synthesizer using either the I<sup>2</sup>C bus or the parallel bus D0 to D7, see Fig.4. The signals  $\overline{CE}$ ,  $\overline{R/W}$  and  $\overline{W}$  are used to write speech data and to read/write the status/command register, see Table 1. Figure 5 illustrates how the control inputs can be used when interfacing the PCF8200 to a microcontroller.

TABLE 1

Truth table of the control signals  $\overline{CE}$ ,  $\overline{R/W}$  and  $\overline{W}$

$\overline{CE}$	$\overline{R/W}$	$\overline{W}$	
0	1	0	write data
0	0	X	read status
0	1	1	3-state parallel bus
1	X	X	3-state parallel bus

For timing details, see PCF8200 data sheet.  
X = don't care.

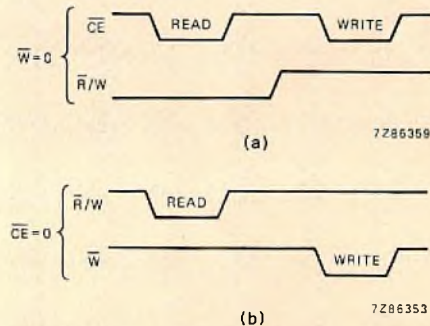


Fig.5 Control signal timing, (a) Chip enable  $\overline{CE}$  used as a read or write strobe; (b) separate read and write strobes

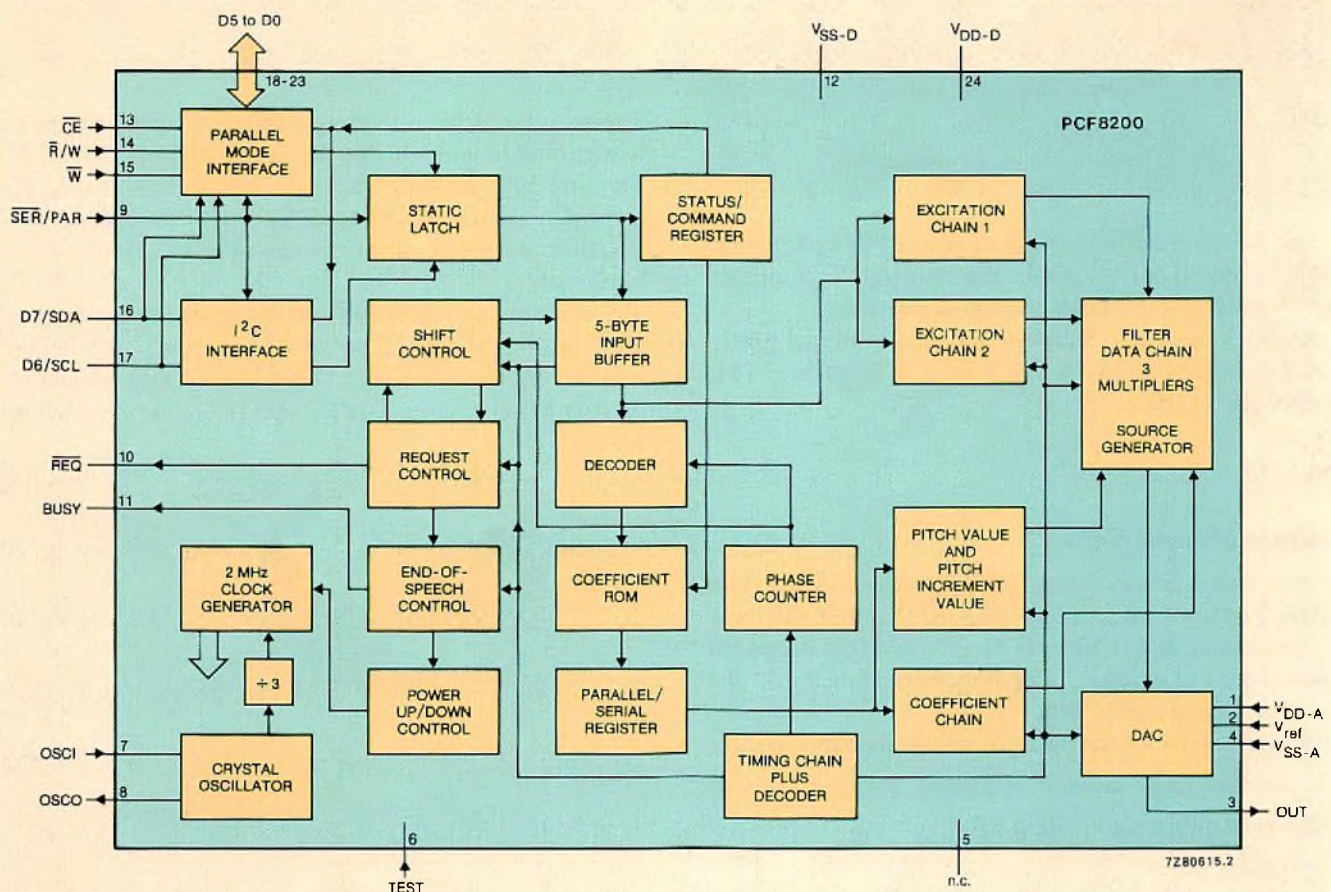


Fig.4 Block diagram of the PCF8200



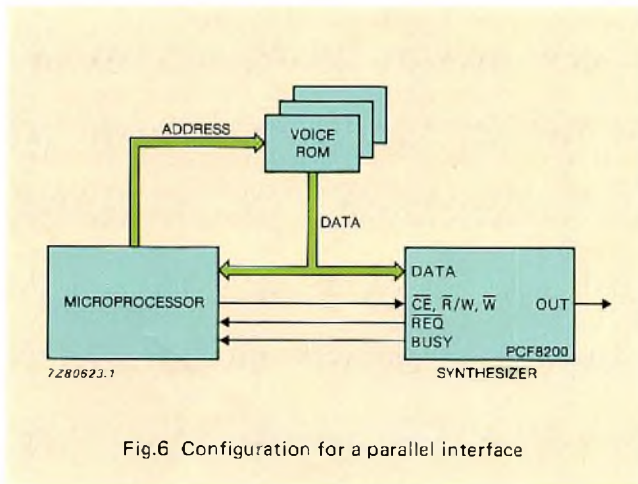


Fig.6 Configuration for a parallel interface

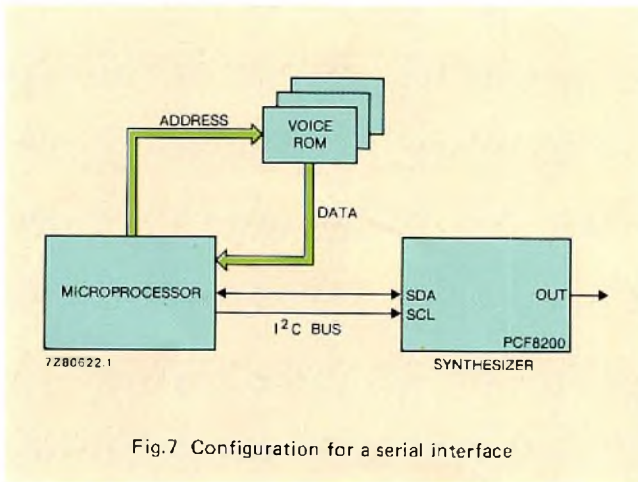


Fig.7 Configuration for a serial interface

The **BUSY** and  $\overline{\text{REQ}}$  pin signals of the PCF8200 permit efficient and fast data transfer. Figures 6 and 7 are circuits using parallel and serial data transfer respectively.

System timing can be set by either an external 6 MHz crystal connected between OSCI and OSCO, or by a TTL clock signal on OSCI.

**Status/command register**

Control data is stored in the status/command register. This register contains two read-only flags:  $\overline{\text{REQ}}$  and **BUSY**, three write-only bits:  $\overline{\text{M/F}}$ , FS0 and FS1 and the **STOP** flag which can be read and written. Table 2 shows the function of the status/command register bits.

At power-on reset, the status/command register is set for:

- a standard frame duration of 12,8 ms (FS0 and FS1 = 0)
- the male quantization table ( $\overline{\text{M/F}}$  = 0)
- **STOP** bit = 0
- idle mode (**BUSY** = 0)
- no data requested ( $\overline{\text{REQ}}$  = 1).

**TABLE 2**  
**Function of the status/command register bits**

bit	status	function/remarks
$\overline{\text{REQ}}$	1	no data required
	0	synthesizer wants new data
<b>BUSY</b>	1	busy (speech is in progress)
	0	idle mode. $\overline{\text{REQ}}$ will be set to 1, the synthesizer will be in the STOP or BADSTOP mode
<b>STOP</b>		Written to the device with a command write;
	1	indicates that the synthesizer was stopped by the user when <b>BUSY</b> = 0
	0	indicates a BADSTOP (i.e. data not provided in the specified time) when <b>BUSY</b> = 0
$\overline{\text{M/F}}$	0	male quantization table
	1	female quantization table
FS0	FS1	speed option bits
0	0	12,8 ms standard frame duration
1	0	8,8 ms standard frame duration
0	1	10,4 ms standard frame duration
1	1	17,6 ms standard frame duration

Control information is written to the synthesizer using two bytes via data lines D0-D7, or via the I<sup>2</sup>C bus, see Fig.8. The first byte is always 00H, the second may contain information relevant to the speaking speed, the male/female selection, or the command issuing a **STOP** signal to the synthesizer.

The three status bits  $\overline{\text{REQ}}$ , **BUSY** and **STOP** are used to monitor or govern the flow of speech data from external memory to the synthesizer. They can be read without a preceding 00H byte via data lines D0-D7, or via the I<sup>2</sup>C bus, see Fig.9.

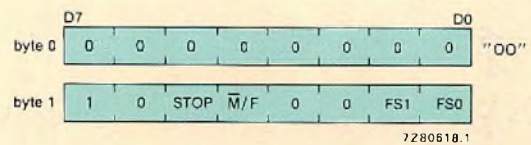


Fig.8 Format of the control bytes

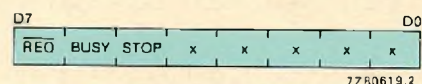


Fig.9 Format of the status bits  $\overline{\text{REQ}}$ , **BUSY** and **STOP** on the data bus

The  $\overline{\text{REQ}}$  signal, which indicates a request by the synthesizer for new speech data, is also available at pin 10 which can be connected to an interrupt input of a host processor.

The BUSY signal is available at pin 11, and is usually interpreted together with the  $\overline{\text{REQ}}$  signal. The BUSY signal indicates when the PCF8200 is pronouncing an utterance. As soon as the first data byte is received, the BUSY signal is set to a 1. Thereafter, the start pitch may be sent as soon as the  $\overline{\text{REQ}}$  flag goes to 0. When both BUSY and STOP are set to 0, a block of speech data has not been sent to the synthesizer in the specified time and a signal known as BADSTOP is generated, see 'Software: Interface Protocol'.

### Setting the speech rate

For good quality speech, the synthesizer's parameters must be updated every few tens of milliseconds. With the PCF8200, the standard frame duration can be set using speed option bits FS0 and FS1 in the status/command register to 8,8, 10,4, 12,8 or 17,6 ms. In addition, the duration of each individual speech frame is programmable to 1, 2, 3 or 5 times the standard-frame duration dependent on the frame duration bits FD0 and FD1. Table 3 shows the frame durations that are available. This programmable bit rate requires an 8-step linear interpolation to smooth the transition from one set of parameters to the next.

FD0	FD1	FS0 = 1	FS0 = 0	FS0 = 0	FS0 = 1	ms
		FS1 = 0	FS1 = 1	FS1 = 0	FS1 = 1	
0	0	8,8	10,4	12,8	17,6	ms
0	1	17,6	20,8	25,6	35,2	ms
1	0	26,4	31,2	38,4	52,8	ms
1	1	44,0	52,0	64,0	88,0	ms

### Formant synthesizer

A coefficient ROM converts the incoming speech codes to 16-bit parameters representing the absolute values of the amplitudes, formants and the pitch increment which after passing through the parameter interpolation logic are sent to the electronic model. One value of the pitch increment parameter is used to turn on the noise source for unvoiced sounds, in all other cases, the programmable pulse generator is active. The signal amplitude from each source is controlled by one of the parameters in the speech code. Pitch

is updated eight times per standard speech frame. The signal from the sources is filtered by the formant filters – a cascade of second-order sections. The amplitudes, formant frequencies and bandwidths are updated eight times per speech frame, giving high quality speech. Figure 10 illustrates the speech frame format and Table 4 gives the bit allocation.

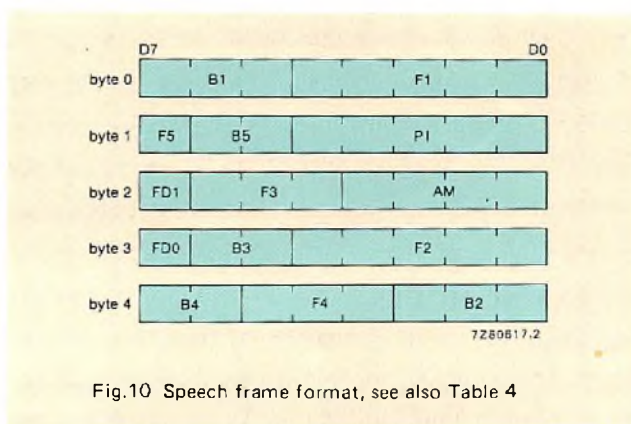


Fig.10 Speech frame format, see also Table 4

TABLE 4  
Speech frame bit allocation, see Fig.10

pitch increment/decrement value	PI	5 bits
amplitude	AM	4 bits
frame duration	FD0, FD1	2 bits
frequency of 1st formant	F1	5 bits
frequency of 2nd formant	F2	5 bits
frequency of 3rd formant	F3	3 bits
frequency of 4th formant	F4	3 bits
frequency of 5th formant	F5	1 bit
bandwidth of 1st formant	B1	3 bits
bandwidth of 2nd formant	B2	3 bits
bandwidth of 3rd formant	B3	2 bits
bandwidth of 4th formant	B4	2 bits
bandwidth of 5th formant	B5	2 bits

The hexadecimal codes of the speech parameters are published in the PCF8200 data sheet.

### Output stage

To reduce the off-chip filtering needed, the output of the formant filters is passed through a low-pass digital filter with eight-times oversampling and a notch filter with its first zero at 5,6 kHz. After it has been filtered, the 25-bit signal is scaled up or down for optimum use of the on-chip 11-bit DAC. The scaling factor is contained in the DAC control byte transmitted at the start of each utterance. The additional filtering required is minimal, for example, a simple RC filter, see Fig.11, which shows a complete audio amplifier for the PCF8200.

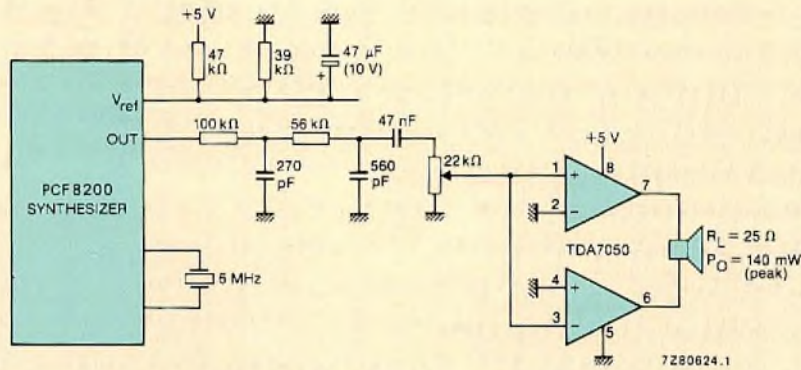


Fig.11 Audio amplifier for the PCF8200

**OPERATING MODES**

**Stand-by**

Whenever the synthesizer is not pronouncing an utterance, and provided it is not hardwired to be permanently active (see 'Serial communication'), the PCF8200 automatically switches to stand-by. In stand-by, the clock oscillator is switched off, but the parallel input latches and the contents of the status/command register remain active. The synthesizer is activated upon receipt of a DAC control byte or any parallel write command.

**Parallel communication**

The parallel bus D0 to D7 can be used by connecting pin 9 (SER/PAR) of the synthesizer to VDD. Data can be written to the synthesizer when REQ=0, or when REQ=1 and BUSY=0. When BUSY=0, the synthesizer is in stand-by.

**Serial communication**

The serial I<sup>2</sup>C bus can be used by connecting pin 9 (SER/PAR) of the synthesizer to ground. However, in stand-by, the synthesizer will not acknowledge when addressed. Therefore, before a DAC control byte can be sent or the status can be read, the synthesizer must be activated by transmitting a write command on the parallel bus. The synthesizer can be made permanently active by hardwiring the control lines CE and W to ground, and R/W to VDD.

The two-line I<sup>2</sup>C bus and the I<sup>2</sup>C interrupt system relieve the host processor of time-consuming polling schemes when transmitting data to the synthesizer.

**SOFTWARE**

**Interface protocol**

Figure 12 shows the input data cycle and the function of the BUSY and REQ flags. Data may be written to the synthesizer when REQ=0 or, when REQ=1 and BUSY=0. The first data byte of a speech file is the DAC control byte.

As soon as the DAC control byte is received, the BUSY signal is set to 1. The second byte, the start pitch byte, which sets the initial pitch of the pitch generator prior to excitation may be sent as soon as the REQ flag goes to 0. If no control data is required, then successive speech codes make up the five bytes of a speech frame and these are used to generate the parameters for the excitation sources and formant filters.

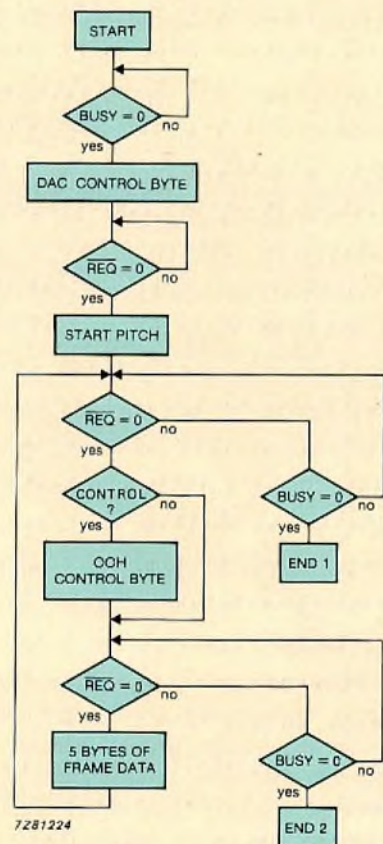


Fig.12 Flow chart illustrating interface protocol

When both **BUSY** and **STOP** are set to 0, a block of speech data has not been sent to the synthesizer in the specified time (within half a frame duration of the falling edge of **REQ**) and a signal known as **BADSTOP** is generated. The synthesizer stops talking, even though the **STOP** bit is not set, and the external controller has to start a new utterance, if desired.

**External memory mapping**

The external memory, usually a ROM, that stores the speech file used by the synthesizer to produce an utterance, also stores the starting pitch and the DAC control byte. The memory contents can be arranged in a number of ways. Figure 13 shows the speech code memory map used in our

OM8200 demonstration board and OM8210 speech development system. At the head of the ROM is a short index which contains the two-byte start addresses of each file. The end of the index field is indicated by the value **FF00H**. Unused positions are given the value **FFFFH**.

Each file contains a five-byte header comprising:

- byte 0, 1 the total length of the file including the header.
- byte 2 the final pitch of the utterance.
- byte 3 the DAC control byte.
- byte 4 the start pitch.

It is advisable, when transferring speech codes to the synthesizer, to store a write command after the start pitch, and a **STOP** command at the end of each file.

**SPEECH DEMONSTRATION BOARD OM8200**

An inexpensive demonstration board (OM8200) is available for you to evaluate the PCF8200 in your own application. The board which requires a minimum of interfacing comes complete with an audio amplifier (TDA7050) and can be operated from a battery. Figure 14 shows the circuit. An MAB80C39 microprocessor operating at 6 MHz supplies all the main control signals for the board and interfacing. Four sockets are provided for the ROMs (27C16 to 27C256) which store the speech code and software to operate the board. Up to twelve minutes of speech can be stored.

When the bus is addressed, the board can:

- select each ROM in turn and pronounce the first utterance in each
- pronounce all the words/utterances stored in the selected ROM
- pronounce a word/utterance repeatedly
- speak at several speech rates.

If desired, the software for operating the board can be altered to provide other effects.

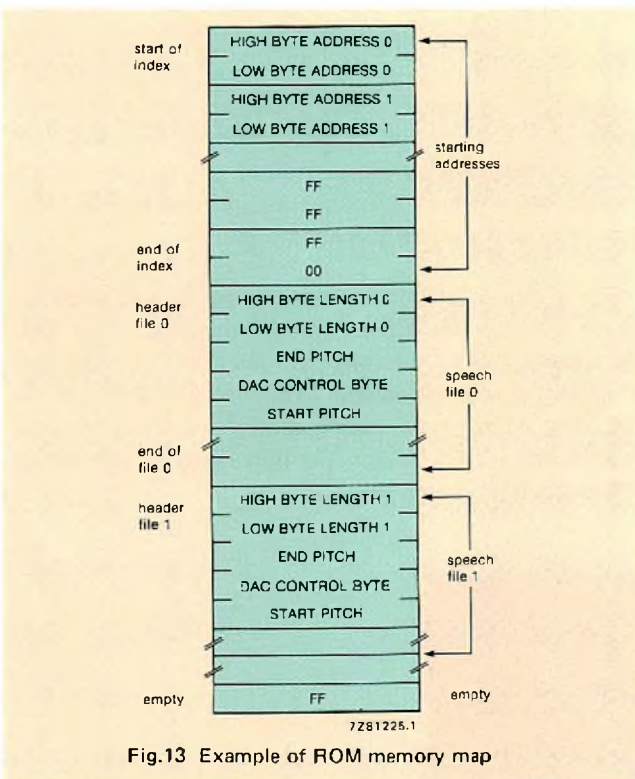


Fig.13 Example of ROM memory map

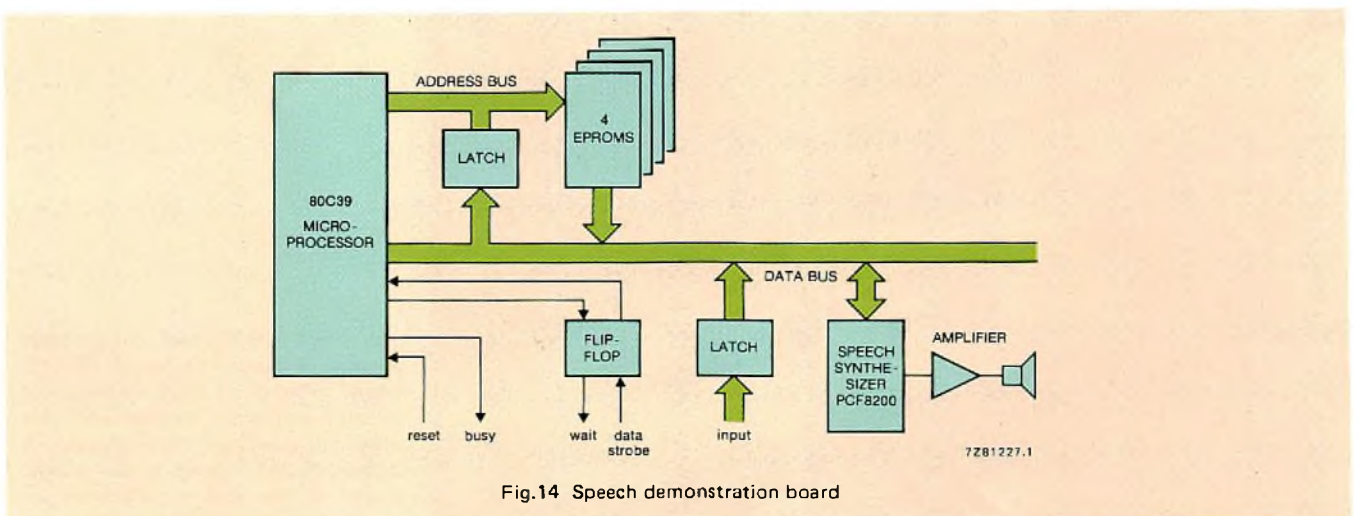
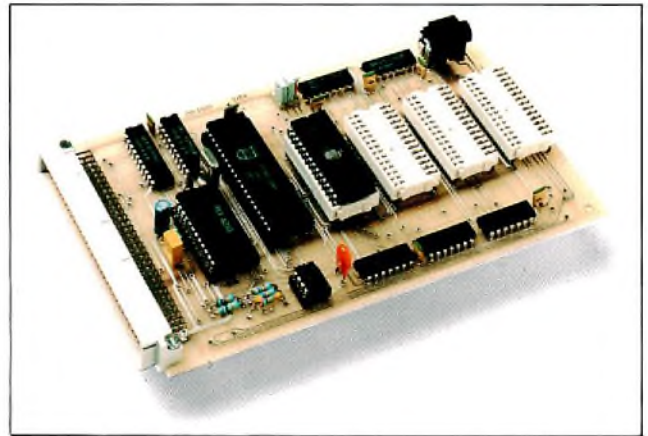


Fig.14 Speech demonstration board

### Features of the OM8200

- PCF8200 speech synthesizer
- low current consumption
- very large vocabulary (up to 12 minutes of speech)
- low data rates
- easy interfacing
- simple operating modes
- single Eurocard size board
- single +5 V supply
- low cost.



Speech demonstration board OM8200

### SPEECH DEVELOPMENT SYSTEM OM8210

Much of the work associated with speech synthesis is generating the speech codes for the synthesizer. Although manufacturers of synthesizers offer a speech-coding service, this is usually performed on a mainframe computer, making it an expensive and time-consuming proposition for the customer, who must travel to and from the manufacturer.

To solve this problem, we have created a speech-development system for use with personal computers. The system also presents a display of the synthesized speech.

The fact that coded speech parameters can be displayed graphically, a revolution in speech editing, has simplified editing so much that it can be learned in a day. By using a personal computer, it is possible to generate speech codes at home or at the office in just a few hours.

The system is a hardware input/output device, called the speech adapter box (SAB) for the computer. The SAB which uses a PCF8200 formant synthesizer can be upgraded as new synthesizers become available. The software for analyzing, editing, and coding speech is available for the Hewlett-Packard Co. 9816S, the IBM PC series and several IBM-compatible computers.



Our speech development system comprises a hardware I/O for an IBM PC (shown here) or an HP9816S computer and all the software (on floppy disk) for analyzing, coding and editing speech. A feature of this system is the graphic display of the speech parameters representing the synthesized speech

**Easier editing**

Editing speech to improve the intelligibility of the synthesizer output and to minimize the data rate without loss of speech quality is normally a specialized task. This is because editing systems usually display the speech to be edited on a screen in the form of complex tables of coded speech parameters, which are difficult for an untrained person to understand. The new system was developed to overcome these shortcomings.

In addition to the benefits of a graphical representation of speech parameters, the speech-development system features:

- speech-interactive operation with which synthesized speech segments or single frames can be pronounced and checked for quality
- software that is arranged in eight modes for optimum user convenience
- menu display of all commands
- keystroke confirmation of all commands that destroy data before the commands are executed.

Figure 15 shows the procedure for generating speech codes for the PCF8200 synthesizer.

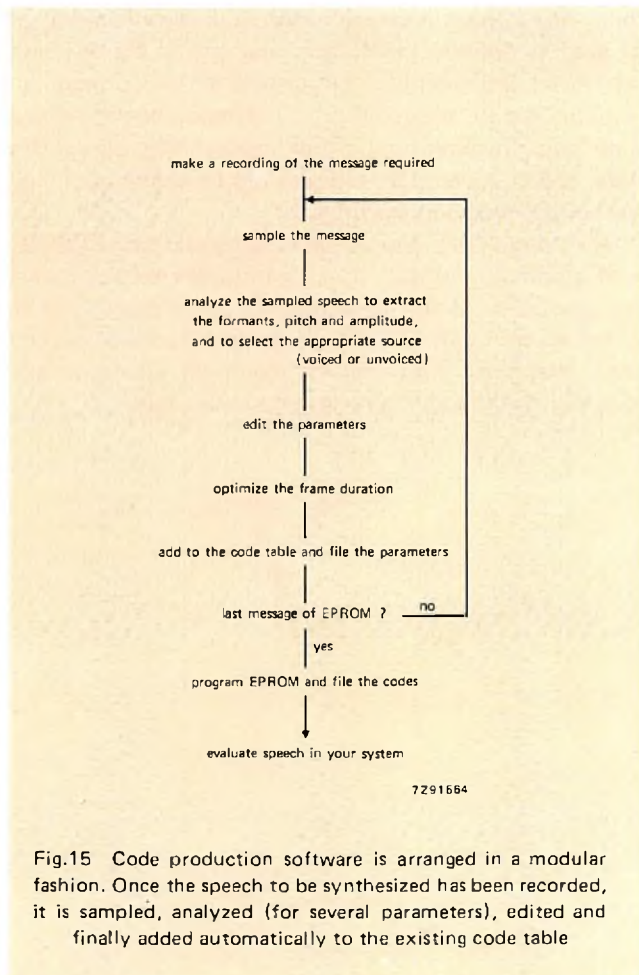


Fig.15 Code production software is arranged in a modular fashion. Once the speech to be synthesized has been recorded, it is sampled, analyzed (for several parameters), edited and finally added automatically to the existing code table

After the speech to be synthesized has been recorded on tape, the Sample mode is used to sample and digitize the recorded speech, check the amplitude of the digitized speech segments, and select speech segments for analysis, the next stage of speech coding. The sampled speech is stored in memory arrays, see Fig.16, used for sampling, parameter input and edit, and coding. Sampled speech can be displayed (Fig.17) or made audible.

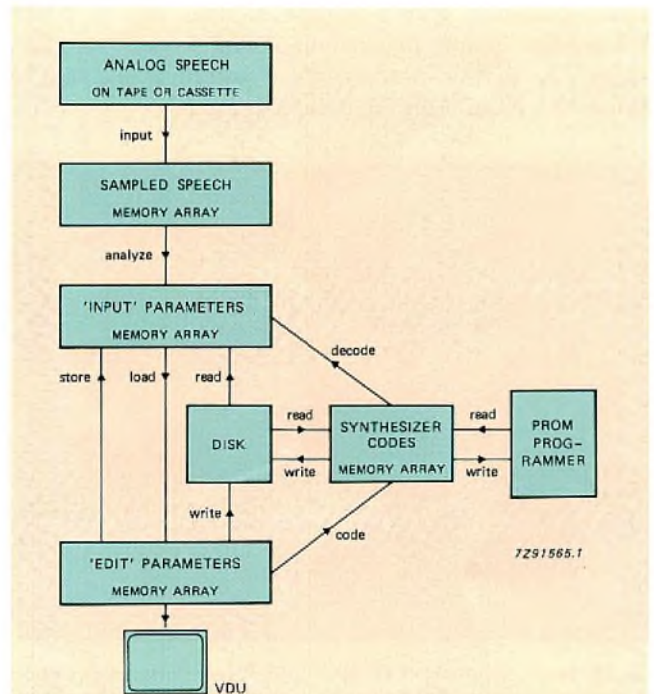


Fig.16 Data flows during the speech coding procedure of Fig.15. Handling speech samples, speech parameters and codes demands a speech development system with extensive data movement facilities

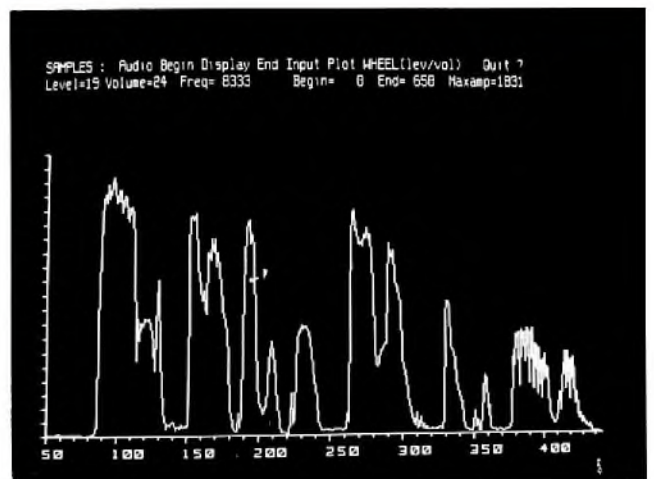


Fig.17 Word picture generated from an HP9816S equipped with our speech system. Analysis takes about 50 seconds for each second of speech. Pauses are not analyzed, so complete phrases can be investigated at about 40 seconds per second of speech

### Converting samples to parameters

In the Analysis mode, speech samples are converted to speech parameters that can be used by the synthesizer. First, the amplitude of the sounds is determined. Then the voiced and unvoiced parts of speech are identified and the pitch of the voiced sounds is extracted together with the formants and their bandwidth. Each parameter is rounded to the nearest one that can be produced by the synthesizer. Using quantized speech parameters that can be coded reduces significantly the amount of data needed to recreate speech. In general, one second of speech is analyzed in about 50 seconds using the HP-based system.

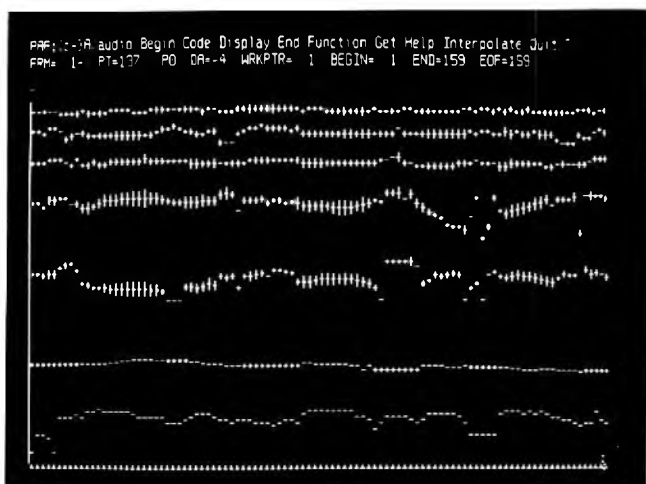


Fig.18 In the Parameter Edit mode, the speech pattern can be modified for a closer match with the source parameters, a graphic display of the speech parameters making it easy to make modifications. Pitch, contour, amplitude and rhythm are adjustable; word sounds can be isolated, separated or moved closer together. The figure shows how the parameters are represented on the display. The top five traces represent the five formant frequencies and bandwidths, the next trace represents the pitch and voiced/unvoiced source selection, the next the amplitude, and the bottom trace represents the speech frame duration

After analysis, the quantized speech parameters are stored in the input-parameter memory and are ready for editing using the Parameter Edit mode. In this mode, a copy of the parameters is loaded into the edit memory. Parameters are displayed graphically on a visual display unit (Fig.18), so that the user can easily identify any errors from analysis.

The speech can also be improved by altering the pitch contour, amplitude, and rhythm. Words and sounds can be isolated or connected. The amount of data to be stored can be reduced by increasing the length of speech segments when the speech parameters are constant or changing at a constant rate. Samples, input parameters and edit parameters are stored in the personal computer's RAM. Therefore, editing mistakes can be corrected readily because the unedited speech is always available. The audio commands are a feature of the parameter-edit mode. They enable the user, at any stage of editing, to hear and compare the speech represented by the contents of the input and edit memories with the original sampled speech stored in the memory array.

### Compressed speech code

Compressed speech code is generated from the data in the parameter-edit memory using the Code mode. The speech codes are stored in a memory array with an address map at its head to indicate the number and size of the different utterances. The order of the utterances in the code map can be optimized for the application. Utterances can be deleted if no longer required, and can be made audible even at this stage. Speech parameters or codes can be stored on floppy disks at any time during editing.

The system can program four industry-standard EPROMs with automatic verification of the EPROM contents against the code map. About 40 seconds of coded speech can be stored on each 64K EPROM. Programs for making backup disks, initializing disks, and for modifying system parameters such as the audio sampling rate are available.

# Line-locked digital colour decoding

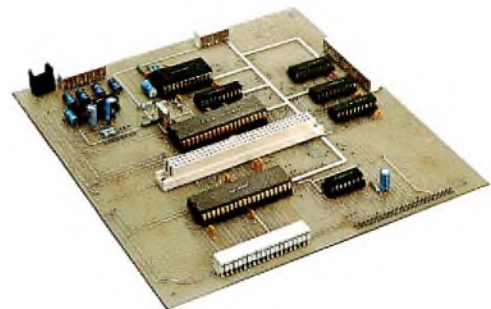
A. H. H. J. NILLESEN

To digitally decode composite-video PAL or NTSC signals in a tv receiver, it is advantageous for the sampling rate to be related to the colour subcarrier frequency because this simplifies the demodulator and the chroma filters. However, after colour decoding, the component video signals (YUV) are available and the colour subcarrier is no longer relevant, so that line-locked sampling is then a better choice. In fact, for picture processing and picture conversion to other scanning frequencies, line-locked sampling is a natural choice because it results in orthogonal sampling (samples of the current line falling directly beneath those of previous lines and fields) which simplifies picture processing with line and field memories. Furthermore, the circuitry for processing line-locked component signals is substantially independent of transmission standard.

Although line-locked samples can be generated from subcarrier-locked samples using a digital sample rate converter, such a converter is both expensive and complex, see Fig.1 and panel. A better approach is to generate line-locked samples directly. However, digital colour decoders operating with line-locked sampling frequencies should also be able to handle non-standard signals in which the line frequency isn't coupled to the subcarrier frequency. An extreme example of this is when a tv receiver has to change the horizontal deflection frequency in steps to correct the phase jumps in the video signals from a video recorder. Obviously, such an unstable frequency cannot be used as a time reference for subcarrier regeneration; at least one stable reference frequency is required. To meet this requirement, the decoder described generates a variable line-locked sampling frequency from a crystal frequency reference. Because of its stable source, this sampling frequency is suitable for subcarrier regeneration, but coupling is

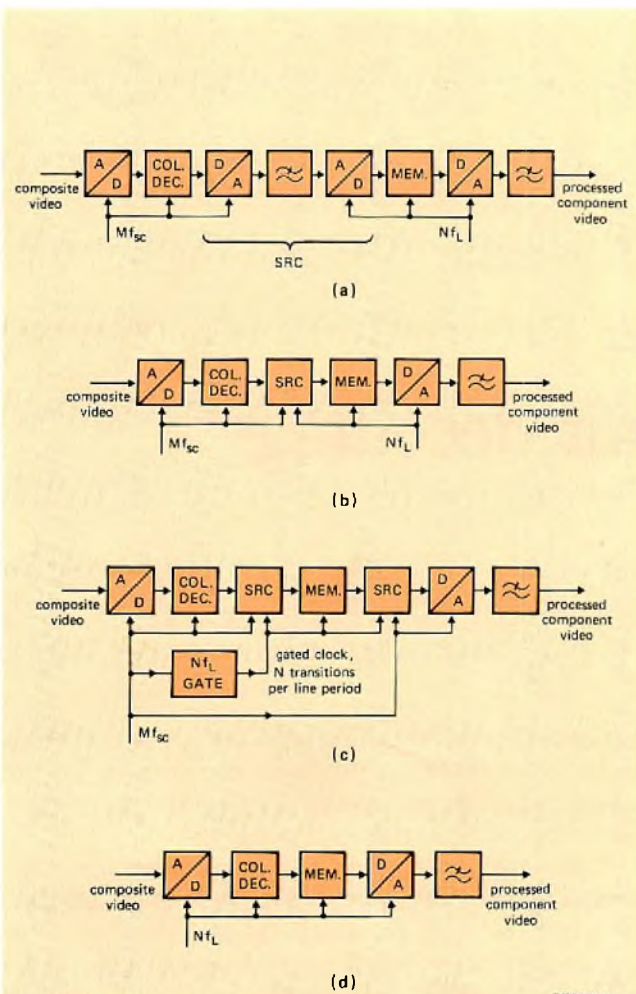
required between the horizontal and subcarrier phase-locked loops (PLLs). Although the decoder uses only one crystal frequency, any subcarrier frequency can be generated to suit different transmission standards.

Line-locked colour decoding is optimised for video processing and standard conversion. In interline, interfield or interframe signal processing, for example, it simplifies the circuitry for reducing cross-colour and noise, or for enhancing resolution. In standard conversion, it simplifies the circuitry for reducing flicker and for providing features such as (multi)picture-in-picture. And looking ahead, a line-locked sampling frequency is essential for decoding C-MAC transmissions, for matrix displays such as LCDs, the index tube and dot matrix printers, and for displaying good quality characters.



Laboratory model of a line-locked digital tv colour decoder. The decoder generates line-locked digital Y, U and V signals which can be sent direct to an RGB processor, or via picture-processing circuitry such as our 'features processor,' — a processor designed around a field memory comprising seven SAA9001 CCDs. The use of line-locked sampling simplifies picture processing with memories and makes the processing circuits substantially standard-independent





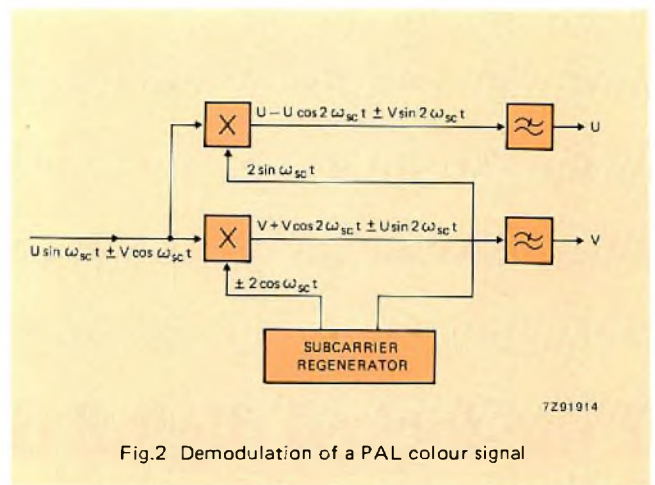
MEM. = memory system  
 COL. DEC. = colour decoder  
 SRC = sample rate converter

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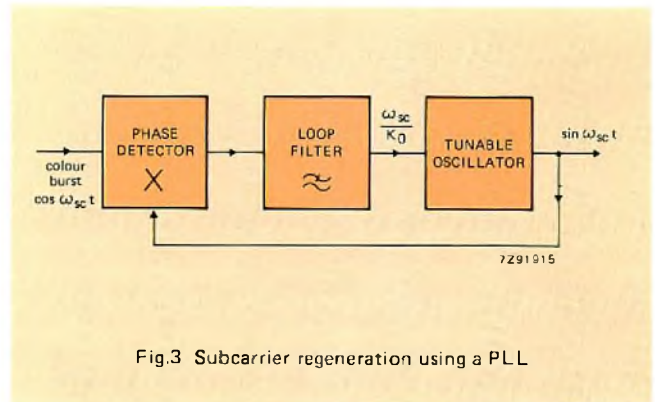
Fig.1 Sample rate conversion (SRC) is a well-known technique that can be used to generate a line-locked frequency in an otherwise subcarrier-locked decoder. But SRC has its drawbacks. Analog SRCs (a) are expensive, they degrade the video signal and require two clocks coupled to the video, one burst-locked, the other line-locked. Digital SRCs with either two clocks (b) or one gated clock (c) require complex interpolating algorithms especially when compatibility with non-standard signals is required. The line-locked decoder described uses a single crystal reference to derive a line-locked sampling frequency directly (d). Since this frequency is derived from a crystal reference, it can be used for subcarrier regeneration

**DIGITAL COLOUR DECODING**

The NTSC and PAL colour systems use suppressed-carrier amplitude modulation with quadrature subcarriers. In an analog decoder, the chroma signal is demodulated by multiplying it by appropriately-phased subcarriers and low-pass filtering the products, see Fig.2. In a digital decoder, the chroma signal has to be multiplied by *sampled* subcarriers



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(Ref.3). If the sample rate is four times the subcarrier frequency (with the correct phase relationship), successive samples are multiplied by 1, 0, -1 and 0. With line-locked sampling frequencies, or any other sampling frequency asynchronous with the subcarrier, real four-quadrant multipliers are required for demodulation with the asynchronously sampled subcarrier.

As is well-known, the subcarrier phase information is transmitted in the colour burst. To reduce the effects of noise, the phase information extracted from several colour bursts is averaged by a narrow bandwidth filter which is usually implemented as a PLL, see Fig.3. In analog circuits, the phase detector is usually a multiplier. The output of the loop filter is proportional to the output of the phase detector and to a time integral of that signal. A digital version of this part of the circuit can therefore be realized with adders, multipliers and an accumulator (integrator).

The tunable oscillator is usually a voltage-controlled sinewave oscillator with a control sensitivity of  $K_0$  rad/s per volt. Therefore, for an output subcarrier frequency  $\omega_{sc}$ , the loop filter should deliver a control voltage of  $\omega_{sc}/K_0$ . The output of the oscillator is the sine of the ever-increasing instantaneous phase  $\omega_{sc}t$ , so the oscillator can be considered as a time integrator with a sinusoidal overflow. Because of the sine function, the output is the instantaneous phase, modulo  $2\pi$  radians.

## DISCRETE TIME OSCILLATOR

The integrating and modulo function of the oscillator can be realized digitally with an accumulator comprising an adder and a multi-bit flip-flop, see Fig.4. At one input of the adder, a constant (multi-bit) value  $p$  is applied. At the second input, the multi-bit ( $n$ ) output of the adder is applied via a multi-bit flip-flop clocked at  $f_{CL}$ . Therefore each clock period, the value in the accumulator is incremented by  $p$  until overflow occurs at a value  $q$ . The first value after overflow is the last value plus  $p$  modulo  $q$ . This circuit is called a discrete time oscillator (DTO). The DTO is also known as a ratio counter since the average frequency of the carry signal is proportional to  $p/q$  of the clock frequency. A third name – accumulator – is also used because of the integrating function of the circuit.

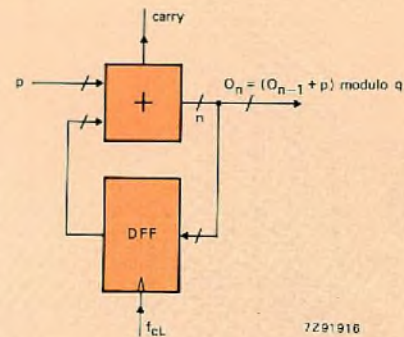


Fig.4 Discrete time oscillator (DTO)

### WHY DIGITAL SIGNAL-PROCESSING?

The use of digital signal-processing in a tv receiver can reduce distortion and eliminate many precision components and (manual) adjustments. Furthermore, digital signal-processing facilitates the use of memory-based features.

### WHY LINE-LOCKED SAMPLING?

In a tv receiver with digital video-signal processing, the rate at which the analog video is sampled is an important design criterion because all subsequent processing is related to this rate. Although asynchronous video-processing is possible, it is advantageous to link the sampling rate to the signal frequencies, such as a suitable harmonic of the colour subcarrier frequency or the line frequency (Ref.1). For composite-video PAL or NTSC signals, a sampling rate related to the colour subcarrier frequency simplifies the demodulator and the chroma filters. However, after the colour decoder, the component video signals (luminance and colour difference) are available and the colour subcarrier is no longer relevant, so that line-locked sampling is then a better choice. Tipping the balance in favour of line-locked sampling is the substantial interest in picture processing with memories which suggests that colour decoding will form only a small part of the video processing in future tv receivers. In fact, for picture processing, picture conversion to other scanning frequencies, and new features with line and field memories, line-locked sampling is a natural choice because it provides orthogonal samples – samples of the current line falling directly below those of previous lines and fields and exactly overlaying samples of the previous picture. This simplifies picture processing with line and field memories and makes the processing circuits substantially standard-independent.

### WHY NOT SAMPLE RATE CONVERSION?

In the main text, the principles of a line-locked colour decoder that can handle non-standard line frequencies such as those from video recorders is described. The line-locked sampling frequency is derived from a crystal frequency used

to clock a digital oscillator. Because of its stable source, this sampling frequency is suitable for subcarrier regeneration.

Generating line-locked luminance and colour-difference samples in this way overcomes the disadvantages of sample rate conversion (SRC) needed with subcarrier-locked digital decoders. For example, one form of sample rate conversion (analog SRC) involves converting the digital samples to analog ones and resampling with a line-locked frequency. Although this is a well-known technique:

- it is expensive, requiring 3 ADCs and 3 DACs for the component video signals, plus pre-filtering and post-filtering
- it degrades the video signal owing to the additional conversion
- it requires two clock signals coupled to the video signal – one burst-locked, the other line-locked.

Another approach is digital SRC which like analog SRC requires two clock signals, although the line-locked clock doesn't have to be physically available. But the main disadvantage of digital SRC is the complexity of the interpolating algorithms required to generate the line-locked samples from subcarrier-locked ones, especially when compatibility with non-standard signals is required. Linear interpolation, for example, is simply not good enough to preserve signal quality. Each sample has to be calculated from several surrounding original samples with proper weighting factors. For compatibility with non-standard video signals with variable line-frequencies, there is the additional complication that the sample conversion-rate cannot be expressed as a simple ratio of small prime integers, but is irrational and time-varying. Consequently, the interpolating filters are complex with many filter coefficients (Ref.2). Add to this the large number of weighting factors needed and the accuracy of the factors for adequate timing accuracy (about 0,2 ns for a video signal with a 5 MHz bandwidth and 8-bit quantization), and it is clear that a digital SRC has another disadvantage – large chip area.

These then are the reasons for considering line-locked colour decoding which produces line-locked samples of the luminance and colour difference signals directly.

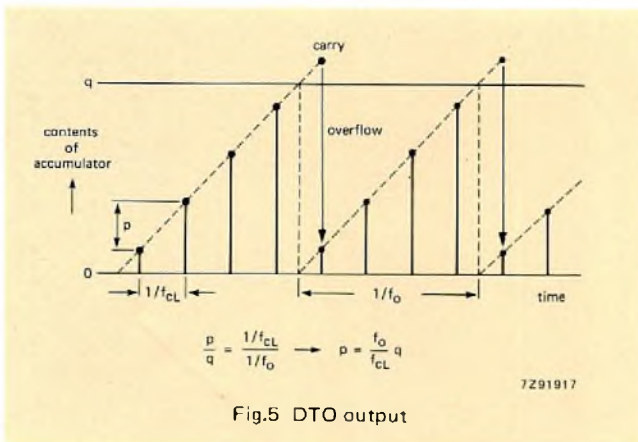


Fig.5 DTO output

Figure 5 shows the DTO output which resembles a quantized and sampled sawtooth signal of frequency set by  $p$ . Clearly, the ratio  $p/q$  equals the ratio of the flip-flop clock period to the period of the DTO output signal, so the control value  $p$  should be  $f_o/f_{CL}q$ . For an overflow value of  $q = 1$ , the required control value is simply  $f_o/f_{CL}$  for a constant output frequency  $f_o$ , see Fig.6.

Note that the control signal  $f_o/f_{CL}$  is dimensionless, simply a ratio indicating the (subcarrier) phase increment per clock period, whereas the DTO output signal indicates the instantaneous phase, in periods modulo one. In binary notation, both signals can be approximated to any desired accuracy. However, if the clock frequency is not constant (e.g. line-locked), it must be sufficiently accurate for making the frequency control if a constant output frequency (subcarrier) is to be generated. Therefore, for accuracy\* and stability, the line-locked clock is derived from a crystal frequency reference.

**LINE-LOCKED CLOCK GENERATOR**

It is beneficial to use a DTO to generate the line-locked sampling frequency from a crystal-controlled frequency reference, because the frequency control for this 'sampling frequency' DTO can be used to correct another DTO in the subcarrier regeneration circuitry for variations in the latter's line-locked clock.

Figure 7 shows how a line-locked clock with crystal accuracy can be generated. The DTO is clocked with the crystal-controlled reference frequency  $f_c$ . Since the desired output frequency is  $Nf_L$ , where  $N$  is an integer and  $f_L$  is the line frequency, the input to the DTO from the loop filter in the horizontal PLL should be  $Nf_L/f_c$ . A continuous line-locked clock frequency is generated from the quantized sawtooth output of the sampling frequency DTO via a sine-ROM which suppresses unwanted frequency components, a DAC, a reconstruction filter which reduces quantization noise, and a wave shaper which converts the sine-wave to the desired logic levels.

\* The line period should be accurate to within 5-10 ns and for a 5 MHz bandwidth composite-video signal linearly-quantized into 8-bits, the sampling clock must be accurate to within 0.2 ns.

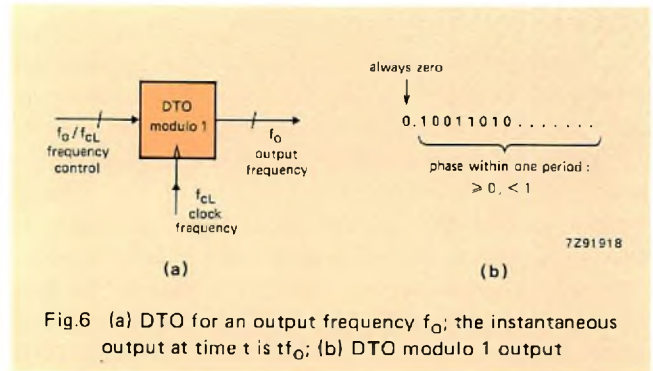


Fig.6 (a) DTO for an output frequency  $f_o$ ; the instantaneous output at time  $t$  is  $f_o$ ; (b) DTO modulo 1 output

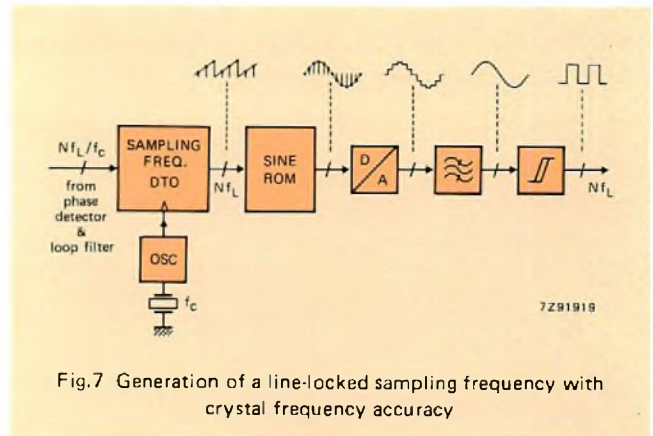


Fig.7 Generation of a line-locked sampling frequency with crystal frequency accuracy

**FORWARD CONTROL OF THE SUBCARRIER REGENERATOR**

Because the relationship between the instantaneous line-locked clock and the crystal-controlled frequency reference is known (the frequency control value  $Nf_L/f_c$ ), it can be used to correct the DTO in the subcarrier phase-locked loop.

Figure 8 shows the subcarrier PLL comprising a burst phase detector (V-demodulator followed by a burst gate), loop filter, subcarrier DTO and the sine/cosine ROM which delivers the demodulating sine and cosine signals. Between the loop filter and the DTO, correction is made for variations in the line-locked clock frequency (forward control). This correction is the key to line-locked colour decoding.

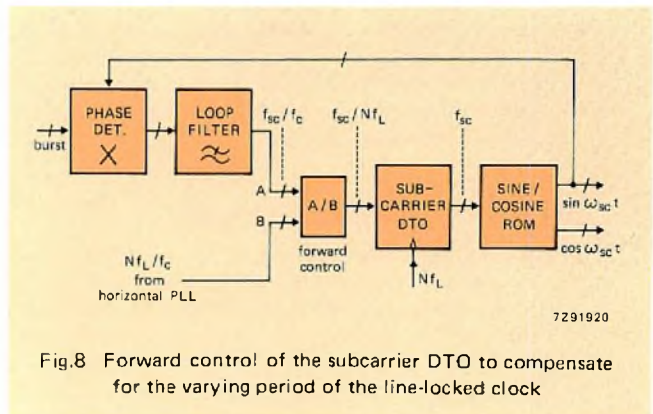


Fig.8 Forward control of the subcarrier DTO to compensate for the varying period of the line-locked clock

Since the subcarrier DTO is clocked with the line-locked clock  $Nf_L$ , a value  $f_{sc}/Nf_L$  (where  $f_{sc}$  is the subcarrier frequency) should be applied to its input to correct for variations in the clock. This value is obtained via an arithmetical divider (A/B) which divides the intermediate control value by the control signal  $Nf_L/f_c$  from the sampling frequency PLL. The intermediate control value should therefore be  $f_{sc}/f_c$ , the ratio of the subcarrier frequency to the crystal frequency. Apart from long-term variations, this ratio remains constant irrespective of the line-locked clock. The subcarrier loop filter can therefore have a narrow noise bandwidth for optimum subcarrier regeneration. Any inaccuracy of the forward control due to the limited wavelength of the signals is treated by the loop as internally-generated noise.

### BASIC LINE-LOCKED DIGITAL COLOUR DECODER

Figure 9 is a schematic of a line-locked digital colour decoder based on the foregoing principles. For clarity, several functions such as automatic colour control, colour killer and compensating delays have been omitted. The signal paths in the line-locked sampling frequency PLL and in the subcarrier PLL are indicated with bold lines.

The left-hand part of the circuit operates with the crystal-controlled clock frequency  $f_c$  and generates the line-locked sampling frequency  $Nf_L$  at which the rest of the circuit operates. A resynchronization register R couples the two circuit parts.

In the sync processing section, the clock frequency  $Nf_L$

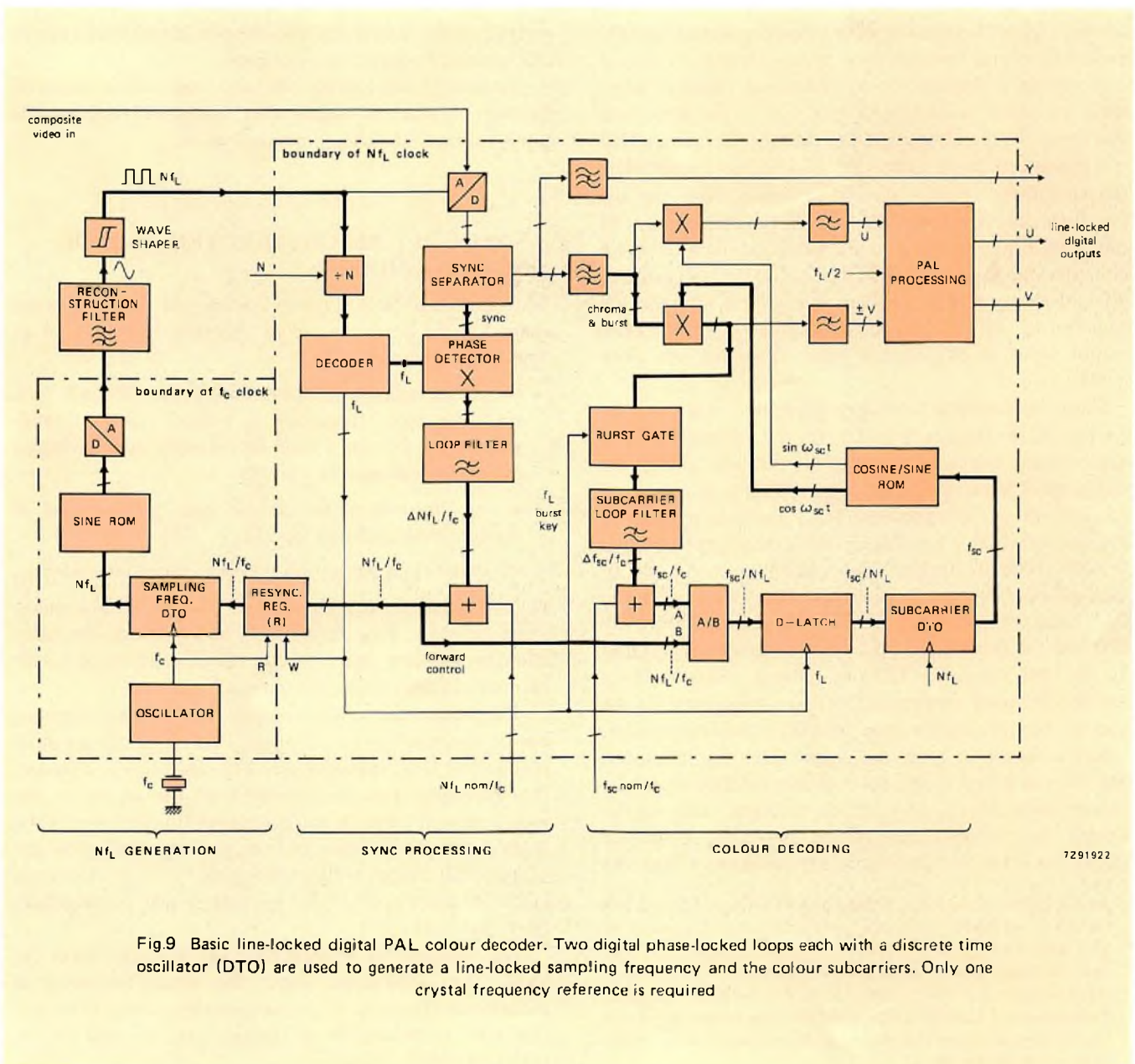


Fig.9 Basic line-locked digital PAL colour decoder. Two digital phase-locked loops each with a discrete time oscillator (DTO) are used to generate a line-locked sampling frequency and the colour subcarriers. Only one crystal frequency reference is required

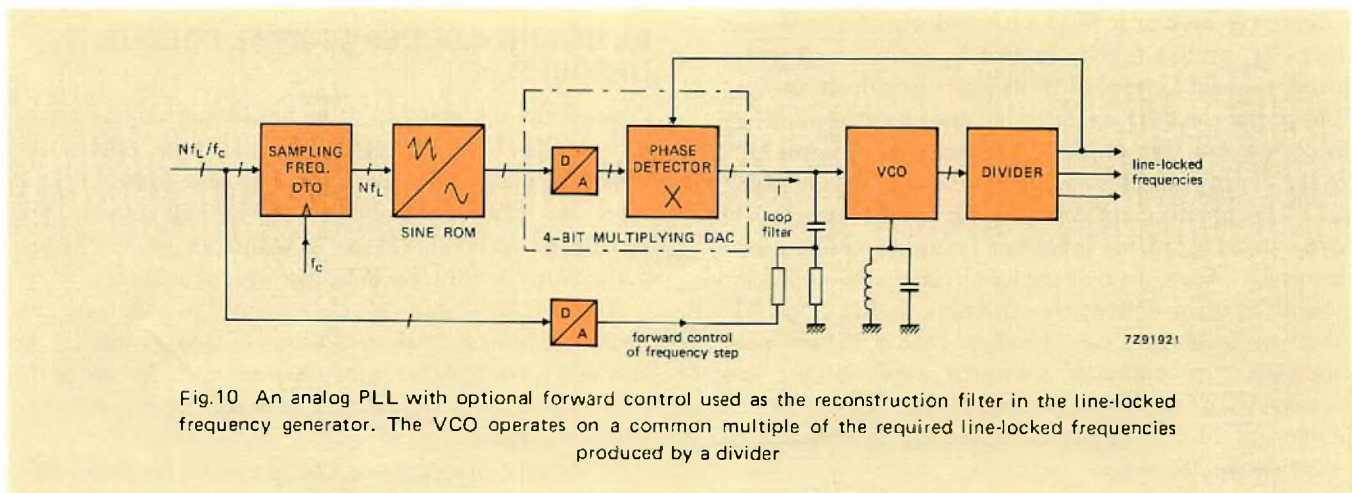


Fig.10 An analog PLL with optional forward control used as the reconstruction filter in the line-locked frequency generator. The VCO operates on a common multiple of the required line-locked frequencies produced by a divider

is divided by  $N^*$  to obtain the line frequency, a state decoder producing several timing signals at line frequency. One of these signals is applied to the horizontal phase detector where its phase is compared with that of the horizontal sync signal. The result is applied to the loop filter and added to the nominal input value ( $Nf_{Lnom}/f_c$ ) for the sampling frequency DTO which is selected externally. Note that the loop filter output is simply the error in the nominal control value ( $\Delta Nf_L/f_c$ ), so the nominal value can be altered for different line frequencies (50 Hz and 60 Hz systems) and different numbers of samples per line without affecting the operation of the PLL. When the PLL is locked, the DTO control input is  $Nf_L/f_c$ , the phase increment per clock period.

Since the sampling frequency is updated only once per line period, the frequency control for the subcarrier DTO is kept constant during a line period. In this 'idle' period, the next control input to the subcarrier DTO is calculated in several clock cycles using restoring algorithms in order to save hardware. Once calculated, the updated control values for both DTOs are applied using a line frequency signal  $f_L$  from the state decoder to clock the write (W) input of the resynchronization register preceding the sampling frequency DTO and the D-latch (D) preceding the subcarrier DTO. In practice, the subcarrier DTO is updated somewhat later than the sampling frequency DTO to compensate for the delay of the video signals from the ADC to the demodulator.

In the subcarrier loop, the output from the subcarrier-loop filter is added to the nominal intermediate subcarrier control value ( $f_{scnom}/f_c$ ), which is preset and can be selected for different transmission standards. Thus, the system has excellent multistandard capabilities and the

\* An attractive choice for N is 858 for 60 Hz tv systems and 864 for 50 Hz systems, since this gives a sampling frequency of 13.5 MHz which is in accordance with the CCIR recommendation for digital processing in studio equipment. The number of active samples per line period is then 720 for all tv standards. Furthermore, 13.5 MHz is the basic sampling frequency chosen for our memory-based features, so no interfacing circuitry would be required (Refs.4 and 5).

output of the subcarrier loop filter is simply the error in the nominal frequency control value.

To prevent side-locking, the loop filter output should be limited so that the regenerated subcarrier frequency is always close to the chosen nominal value.

### ANALOG PLL RECONSTRUCTION FILTER AND WAVE SHAPER

It is advantageous for the reconstruction filter and wave shaper of the line-locked clock generator to be part of an analog PLL, because:

- the centre frequency of the reconstruction filter will then track the input frequency, so a much narrower bandwidth than that for a fixed filter can be used, giving an extremely low noise bandwidth
- several line-locked frequencies can be generated if dividers are included in the PLL
- the entire clock generation circuitry can be integrated.

Figure 10 shows a suitable analog PLL with a charge-pump phase detector, loop filter, VCO and dividers, the latter allowing the first part of the circuit to operate on a sub-harmonic of the sampling frequency.

The phase detector is driven by a DAC, so these functions can be combined in a multiplying DAC. Experiments show that a 4-bit DAC requiring very little chip area is adequate, the resolution required depending on the quality of the reconstruction filter. A narrow-bandwidth filter means the DAC can have fewer bits, but the narrow noise bandwidth of the PLL causes a slower response to frequency steps (such as those from video recorders) and consequently larger phase errors.

The response can be improved by forward control of the VCO. The information about the actual frequency is available at the input of the sampling frequency DTO and can, after conversion to an analog signal, be used to pre-correct the VCO frequency.

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# In-line system for surface-mount assembly accepts large circuits boards

J. J. DE JONG

Answering the need of consumer electronics manufacturers to extend the benefits of surface-mount assembly to larger circuit boards, MCM-VI is the latest addition to a now well-known series of modular placement systems. Boards it can accommodate range up to 250 mm by 430 mm.

## IN-LINE SYSTEM WITH MULTIPLE PLACEMENT MODULES

Like the MCM-IV described in *Electronic Components and Applications*, Vol. 7 No. 2, MCM-VI uses placement modules in which pick-and-place pipettes on a servo-driven

beam accept surface-mount devices (SMDs) from feed tapes and convey them to software-defined placement sites. Each module can have up to 32 pipettes for SMDs packaged in 8 mm tapes. Modules with specially adapted tape-reel cassettes are available for SMDs packaged in 12 mm, 16 mm or 24 mm tapes, or for a mix of 8 mm to 24 mm tapes. Depending on circuit-board layout and the corresponding software, SMD placement at each module can be purely sequential or a combination of sequential and simultaneous for faster throughput. Using the maximum of eight placement modules fed by 8 mm tapes, and with pipettes working two-at-a-time at each module, an MCM-VI can place 120 000 SMDs an hour.



Fig.1 Shown here with four placement modules, an MCM-VI installation can accommodate a maximum of eight

A modular conveyor consisting of paired chains running at constant speed supports the edges of the boards and advances them from module to module. When a board reaches a placement module an arrester mechanism halts its progress but leaves the movement of the chains unaffected so that boards elsewhere in the system can continue to move down the line. To accommodate boards of different widths the spacing between the chains can be set to any value between 80mm and 250mm. A valuable option, especially for large boards supporting two identical circuits that are later to be separated, is a system for indexing boards at two successive positions at each placement module.

The inherent flexibility of the placement modules enables rapid changeover from production of one type of board to another. When pre-loaded tape-reel containers for different board types are kept in reserve, such a changeover can usually be effected in about five minutes. Reliability, which is equally important, has been amply demonstrated in the MCM-I, MCM-II and MCM-IV systems in which, up to mid-1986, some 170 such modules have been put in service.

### ALTERNATIVE GLUING MODES

A feature that adds to the system's ability to deal with a variety of assembly situations is the provision of two gluing options. In one, a software-controlled unit integral with the placement modules applies glue to the underside of each SMD before it is conveyed to the placement site. For short production runs and for boards that are still subject to design changes, this is generally the preferred mode. Board design changes involving, for example, addition or relocation

of SMDs can be accommodated in software without the time or expense of hardware modification.

For large production runs of boards no longer subject to change the alternative is an in-line glue application module preceding the first placement module. Using a pin-transfer die, this applies glue dots simultaneously to all the SMD placement sites on the board, rather than to the SMDs themselves. Proved over several years in the MCM-III in large-volume production of boards for car radio and electronics modules, tv tuners and the like, this option can cut the cycle time at each placement module by as much as 15%.

Whichever alternative is chosen, the placement pipettes, which combine vacuum and mechanical action, make a final check on the security of SMD adhesion. Persistence of vacuum in the central tube of a pipette after it withdraws from a placement site signals that the SMD has not stuck to the board but is still lodged in the pipette. The control system then interrupts the machine cycle and alerts the operator.

### SOFTWARE SUPPORT INCREASES OPERATING ECONOMY

A user-friendly software package is available under the name 'Domino' for data preparation on an off-line computer. Starting from the board layout, parts list and SMD coordinates, this works out the time needed for SMD placement, using optimization programs to arrive at the shortest possible time. By comparative evaluation of board-layout and circuitry variants, Domino also enables a minimum sum of PCB, SMD and placement costs to be achieved.

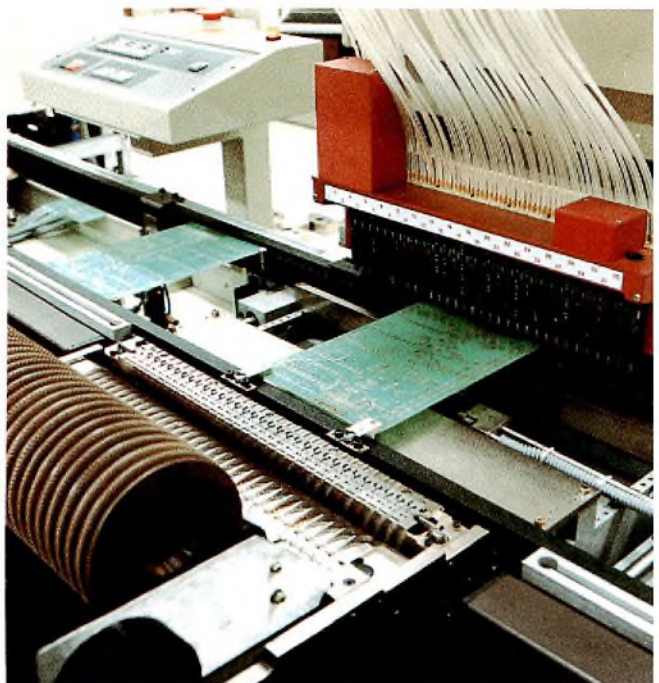


Fig.2 MCM-VI placement modules with pipette beam (right) and tape-reel cassette and software-controlled glue applicator (left). As a circuit board enters the module an arrester mechanism (lower right) halts it and a lifting unit raises it clear of the transport chains; tapered pins engage positioning holes in the board, which is then clamped. An automatic gate stops new boards from approaching the module before the one in process has been released

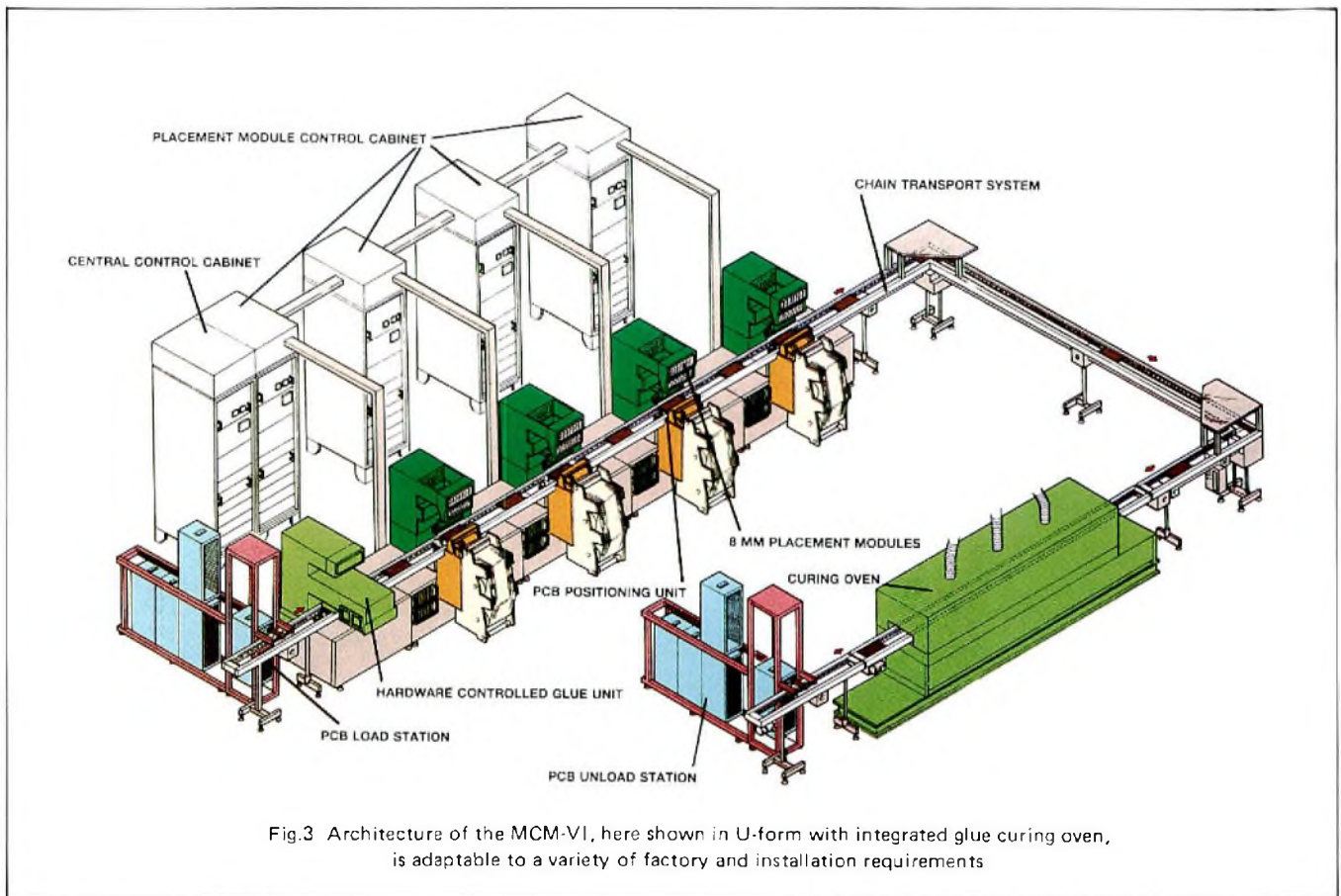


Another software package, 'Zone Inhibiting System', enables groups of boards having minor differences to be processed on the same line without hardware changes. For this, data is prepared for a notional board containing all the SMDs present on all members of the group. When a specific board is to be produced, SMDs not present on that board are simply omitted from the placement specification. To change from one board to another it is only necessary to change the digital cassette containing the placement specification in the central controller. Used in conjunction with an optical recognition system, the 'Zone Inhibiting System' software can also prevent wasteful placement of SMDs, for example, on boards with multiple identical circuits one of which has been marked as defective.

**ADAPTABLE TO DIFFERENT INSTALLATION REQUIREMENTS**

MCM-VI can be installed as a stand-alone system with manual or automatic board loading and unloading stations. It can also be integrated into a production line, accepting bare boards, or boards with pre-inserted leaded components, from one part of the line and delivering them to another with all SMDs in place. In such an installation it might be followed, for example, by an in-line glue curing oven, a facility for placing 'odd components', and a double-wave soldering machine.

MCM-VI systems are already in operation in consumer electronics factories in Louvain, Belgium, and Vienna, Austria; others are due to be installed in Belgium, France, Germany and Brazil.



### CONSUMER ELECTRONICS INDUSTRY SETS NEW TASKS FOR SURFACE-MOUNT ASSEMBLY

Surface-mount assembly won its spurs in high volume production of small circuit boards. Typical was a tv tuner on a board measuring, say 70 mm x 100 mm with seldom more than about 100 surface-mount devices (SMDs) representing some 30 part numbers, all packaged in 8 mm tapes. Production-runs upward of a million identical boards a year in one factory were not unusual. What repaid the investment in surface-mounting machinery several times over was smaller size, lower production cost and, most important in today's competitive markets, improved quality — both conformity and reliability. The next logical step was to apply the technology to larger boards.

But in the consumer electronics industry that's not just a matter of scaling up the machinery. Market commitments play a decisive role. Take a line of tv receivers for instance. Over a range of picture tube sizes all of them will use the same chassis board. But they won't all have the same features; top-of-the-line models will boast a lot more than the bare-bones economy model. And what's on the chassis board will differ accordingly. Assembling a few tens of thousands of one version, then rearranging the production machinery to assemble a few tens of thousands of another isn't the answer. Warehousing excess inventory is expensive, and the market wants a steady supply of the whole line. What can make that economically possible is an assembly facility that can be quickly and cheaply rearranged by altering software, not hardware.

A tv chassis board may measure up to 250 mm x 380 mm, so the assembly facility has to be able to handle that as well as the many smaller boards common in consumer electronics. Because the board may contain as many as 400 SMDs packaged in 8 mm and larger tapes and representing perhaps 150 part numbers, the facility also has to allow for a large number of tape reels in various sizes, possibly intermixed.

Total assembly time depends very much on how the SMDs are placed. If a particular SMD is used, say, four times on the board, it may be necessary to draw it from two or four separate sources to achieve the required placement time. Moreover, it might be used four times on one version of the board but only three on another. Allowing for such alternatives implies a facility with provision for several placement stations, preferably modular. Implementing the chosen alternative for a specific board version can be done in the software that controls the placement stations.

In common with a lot of other consumer electronics boards, a chassis board usually relies on a number of leaded components too. One way of coping with that would be to accumulate boards with pre-inserted components and feed them to the surface-mount facility in large batches. But with a software-controlled modular SMD placement system that's not necessary. Such a system can be slotted into the total assembly process with its operating pace tuned to the supply of boards.

Addressing these requirements led to the philosophy underlying the new MCM-VI.

### ACKNOWLEDGEMENT

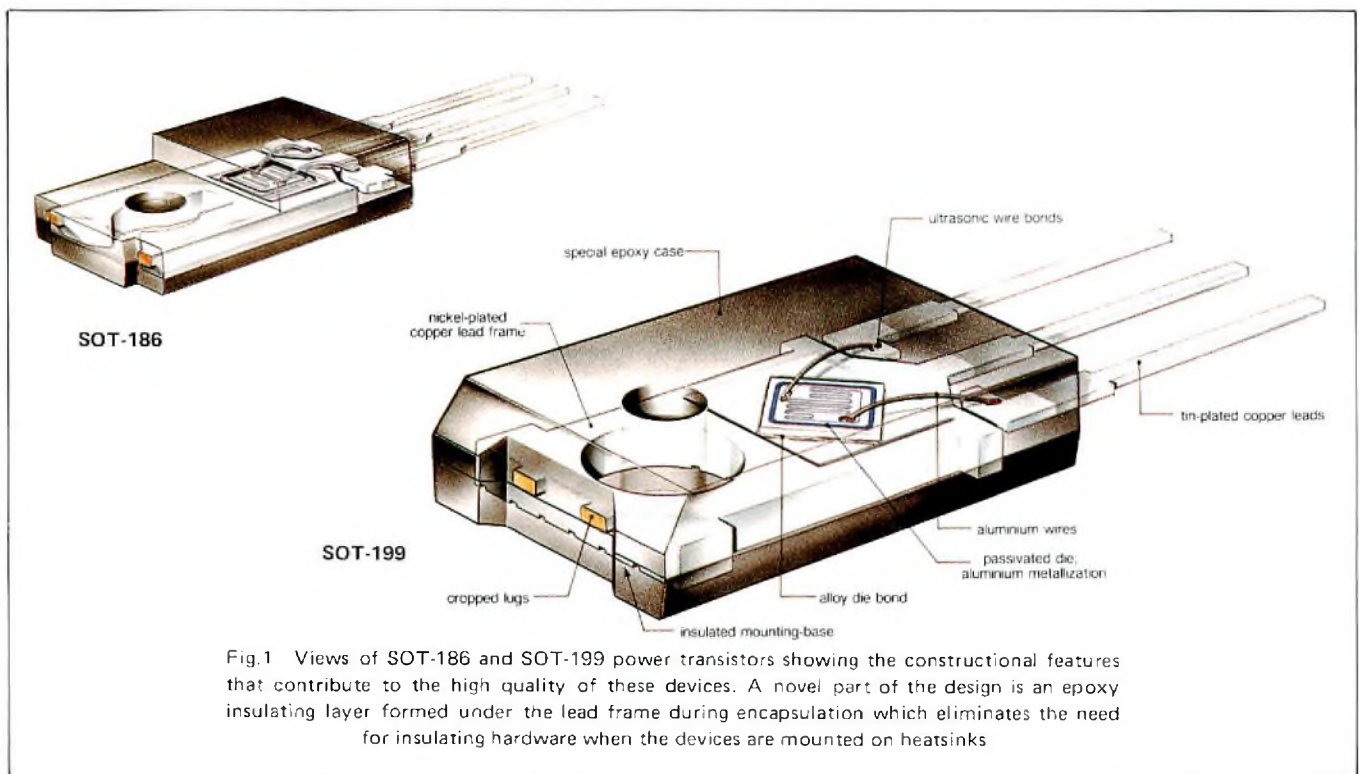
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# Insulated encapsulations for easier mounting of power semiconductors

Improper assembly of the insulation accessories is a common cause of premature failure of power transistors, diodes and thyristors. A multitude of incompatible accessories and the need for a variety of accurately-drilled counterbored heatsink holes increase the probability of mistakes during equipment assembly, causing overheating or inadequate insulation in operation. In addition, ordering, storing and handling insulation accessories is time-consuming and expensive. To solve these problems, two encapsulations with integral insulation have been developed, see Fig.1:

- the SOT-186, equivalent to an insulated mounting of a TO-220 component
- the SOT-199, equivalent to an insulated mounting of a SOT-93 component.

Requiring only a spring clip, or screw, washer and nut to hold them in place on a heatsink, components in the new encapsulations are attractive alternatives to TO-220 and SOT-93 components insulated in the conventional way with a separate mica or flexible insulator, see Fig.2.



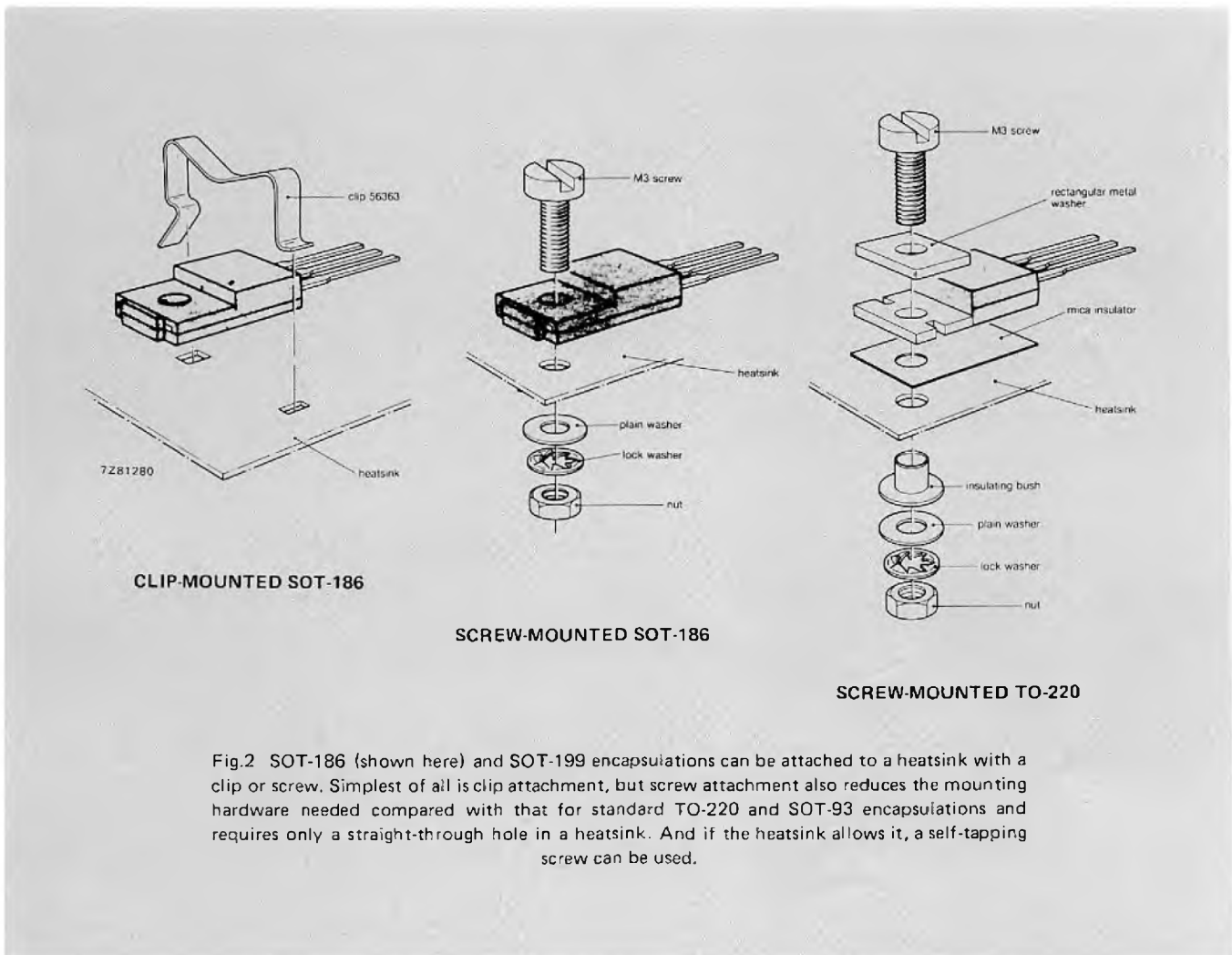


Fig.2 SOT-186 (shown here) and SOT-199 encapsulations can be attached to a heatsink with a clip or screw. Simplest of all is clip attachment, but screw attachment also reduces the mounting hardware needed compared with that for standard TO-220 and SOT-93 encapsulations and requires only a straight-through hole in a heatsink. And if the heatsink allows it, a self-tapping screw can be used.

Because the dies and alloy die-bonding used in SOT-186 and SOT-199 components are the same as those used in the standard TO-220 and SOT-93 versions, the reliability of the new components, as initial life-test results confirm, is anticipated to be similar to that of TO-220 and SOT-93 components. Furthermore, the thermal and electrical characteristics of the new components are always at least as good. Free-air dissipation, for example, is 30% higher for a SOT-199 component and more than 15% higher for a SOT-186 component compared with their SOT-93/ TO-220 counterparts. In most cases, SOT-186 and SOT-199 components are direct replacements for TO-220 and SOT-93, although there are minor differences in size. And virtually every component in TO-220 and SOT-93 is available in the new encapsulations.

## CONSTRUCTION

Unlike the TO-220 and SOT-93 encapsulations where the nickel-plated copper mounting base is visible, for SOT-186 and SOT-199, it is hidden under an extremely thin layer of

epoxy formed during manufacture and chosen for its excellent thermal and insulating properties. For consistent performance, the thickness of the layer is controlled to within  $\pm 25\mu\text{m}$ , which required the development of new leadframes and headers. Less than  $400\mu\text{m}$  thick in the case of the SOT-186 (less than  $500\mu\text{m}$  thick for SOT-199), the layer has a breakdown voltage in excess of 2000V and a thermal resistance comparable to that of a  $50\mu\text{m}$  mica insulator.

During moulding, two lugs on the lead frame and the leads support the header, maintaining a constant distance between the underside of the mounting base and the bottom of the mould. After the epoxy injected into the mould has cured, the lugs are cropped. The underside of the header is grooved for optimum adhesion of the insulating layer.

The insulating layer creates a small parasitic capacitance of about 20 pF between the leadframe and the heatsink on which the component is mounted. However, this capacitance is less than half that of a standard TO-220 or SOT-93 component mounted on a heatsink and insulated with a  $50\mu\text{m}$  mica insulator.

Dimensions in mm

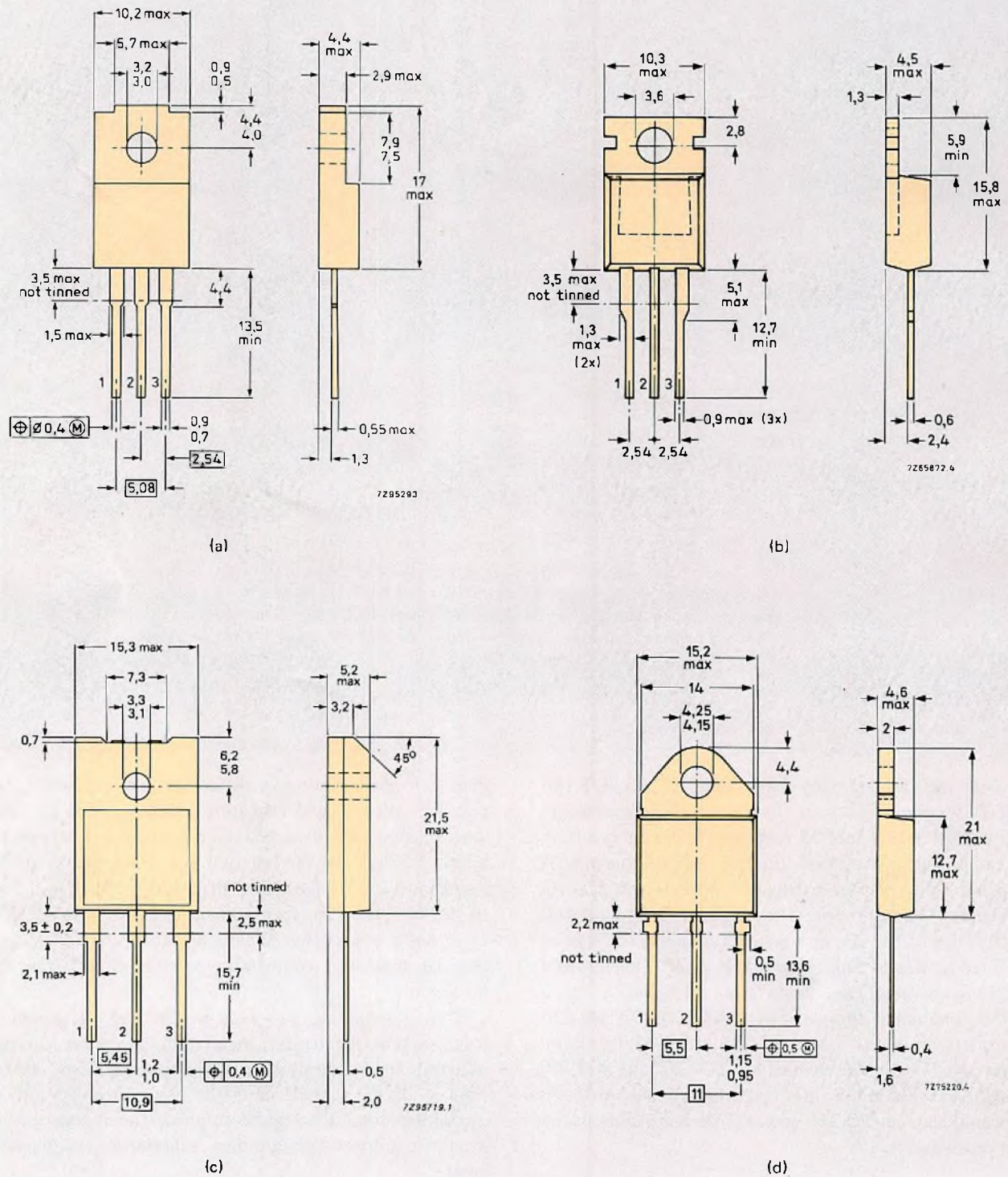


Fig.3 Dimensions of (a) SOT-186, (b) TO-220, (c) SOT-199 and (d) SOT-93 encapsulations. Outwardly similar to a TO-220 encapsulation, a SOT-186 encapsulation is distinguished by its integral insulator, flatter leadframe and thicker tab. Besides its integral insulator, the main distinguishing feature of a SOT-199 encapsulation compared with a SOT-93 is its larger body

## COMPATIBILITY WITH TO-220 AND SOT-93

The new encapsulations are designed to be direct replacements for TO-220 and SOT-93 encapsulations in existing designs.

### Dimensions

Although the new encapsulations have many of the features of their TO-220 and SOT-93 counterparts, some external dimensions are slightly different which may necessitate minor modification to existing heatsink mountings, see Fig.3. When heatsinks aren't used, SOT-186 and SOT-199 components are direct replacements for TO-220 and SOT-93 components.

### Voltage ratings

Although the insulating layer has a breakdown voltage in excess of 2000 V under standard conditions of temperature, pressure and humidity, voltage ratings of 1000 V and 1500 V are specified for the SOT-186 and SOT-199 encapsulations respectively because the lead spacing at the encapsulation is slightly less than that for their uninsulated equivalents. For this reason, transistors in TO-220 with voltage ratings higher than 1000 V have no equivalent in SOT-186. However, the dies of such transistors are available in SOT-199 (voltage rating 1500 V).

## THERMAL RESISTANCE AND POWER DISSIPATION

There is no need to derate when you replace a TO-220 or SOT-93 component by its insulated equivalent – the new encapsulations can dissipate as much heat as the standard ones even though published power ratings can, at first sight, suggest lower power-handling capability than an equivalent TO-220 or SOT-93 component.

Because of their unique construction, the published values of power dissipation for the new components are specified for a *heatsink temperature* of 25 °C, whereas for TO-220 and SOT-93, the reference is a *mounting-base temperature* of 25 °C.

For SOT-186 and SOT-199:

$$P_{\text{tot max}} = \frac{T_{\text{j max}} - 25}{R_{\text{th j-h}}}$$

For TO-220 and SOT-93:

$$P_{\text{tot max}} = \frac{T_{\text{j max}} - 25}{R_{\text{th j-mb}}}$$

where  $T_{\text{j max}}$  is the maximum junction temperature in °C,  $R_{\text{th j-h}}$  is the thermal resistance from junction to heatsink, and  $R_{\text{th j-mb}}$  is the thermal resistance from junction to mounting-base.

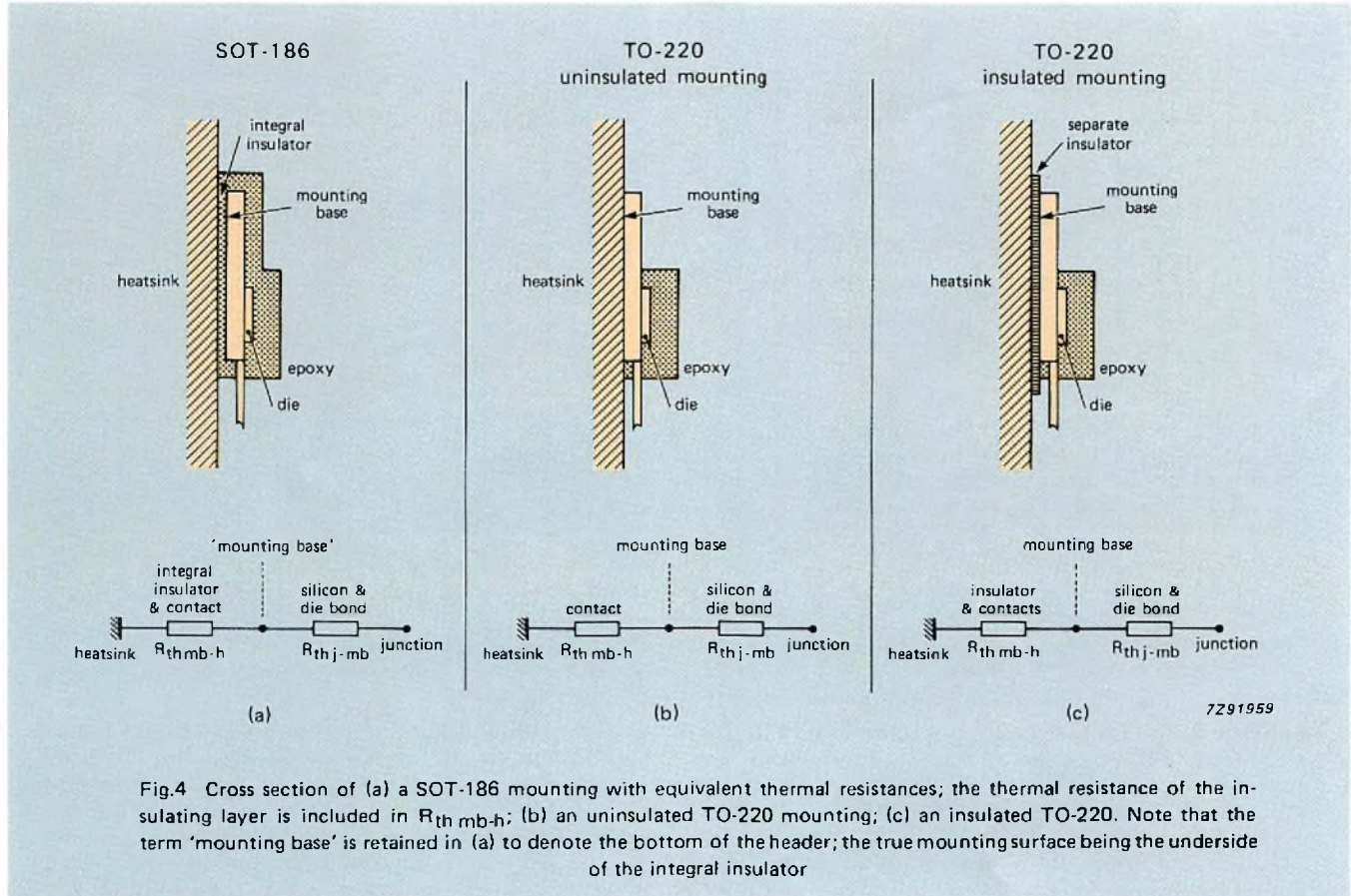


Fig.4 Cross section of (a) a SOT-186 mounting with equivalent thermal resistances; the thermal resistance of the insulating layer is included in  $R_{\text{th mb-h}}$ ; (b) an uninsulated TO-220 mounting; (c) an insulated TO-220. Note that the term 'mounting base' is retained in (a) to denote the bottom of the header; the true mounting surface being the underside of the integral insulator

**TABLE 1**  
**Thermal resistance  $R_{th\ j-a}$  and the maximum dissipation in air of several plastic encapsulations**

encapsulation	$R_{th\ j-a}$ (K/W)	max. dissipation in air at 25 °C; $T_j = 150$ °C (W)
SOT-199	35	3,6
SOT-93	50	2,8
SOT-186	55	2,3
TO-220	70	1,8
TO-202	60	2,0
SOT-82	88	1,4
SOT-32	100	1,2

The specification for the new components gives a better indication of the power handling capability, because it includes the effect of the thermal resistance of the integral insulator and all contact thermal resistances, see Fig.4. And when the thermal resistances of the different encapsulations are compared, it can be seen that the new encapsulations are at least as good at dissipating heat.

**Mounted in free air**

In free air, the new encapsulations can dissipate more power than their standard versions, owing to a lower thermal resistance from junction to ambient,  $R_{th\ j-a}$ , due to larger bodies and the use of black epoxy, see Table 1 and Fig.5.

**Mounted on a heatsink**

Mounted on a heatsink, the new encapsulations can dissipate as much power as the standard encapsulations insulated

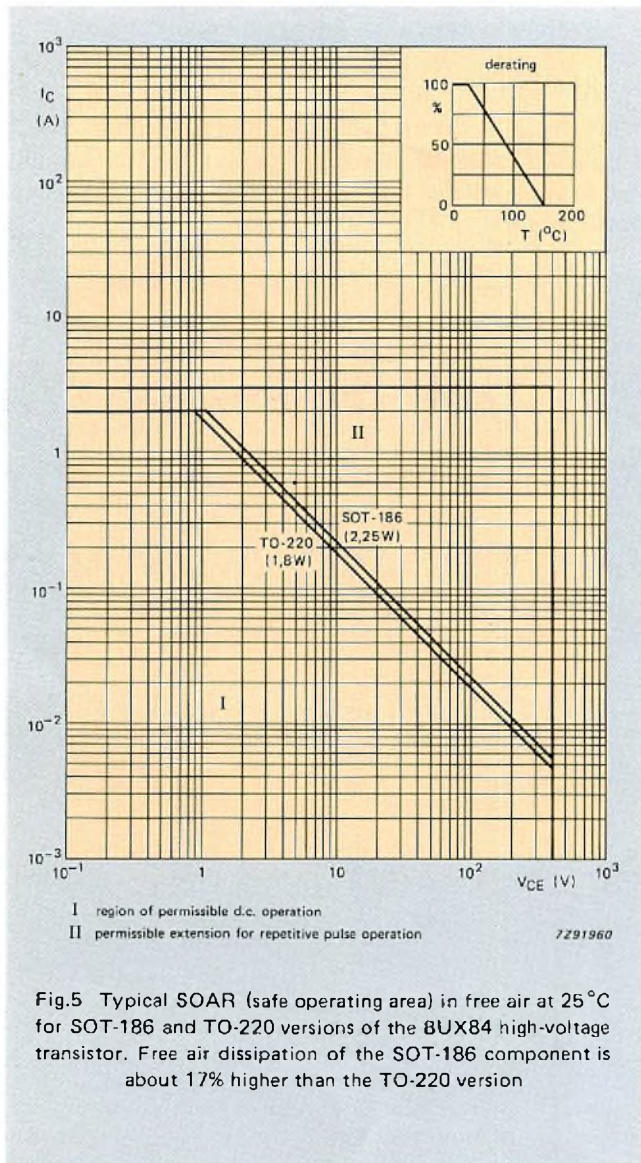


Fig.5 Typical SOAR (safe operating area) in free air at 25 °C for SOT-186 and TO-220 versions of the BUX84 high-voltage transistor. Free air dissipation of the SOT-186 component is about 17% higher than the TO-220 version

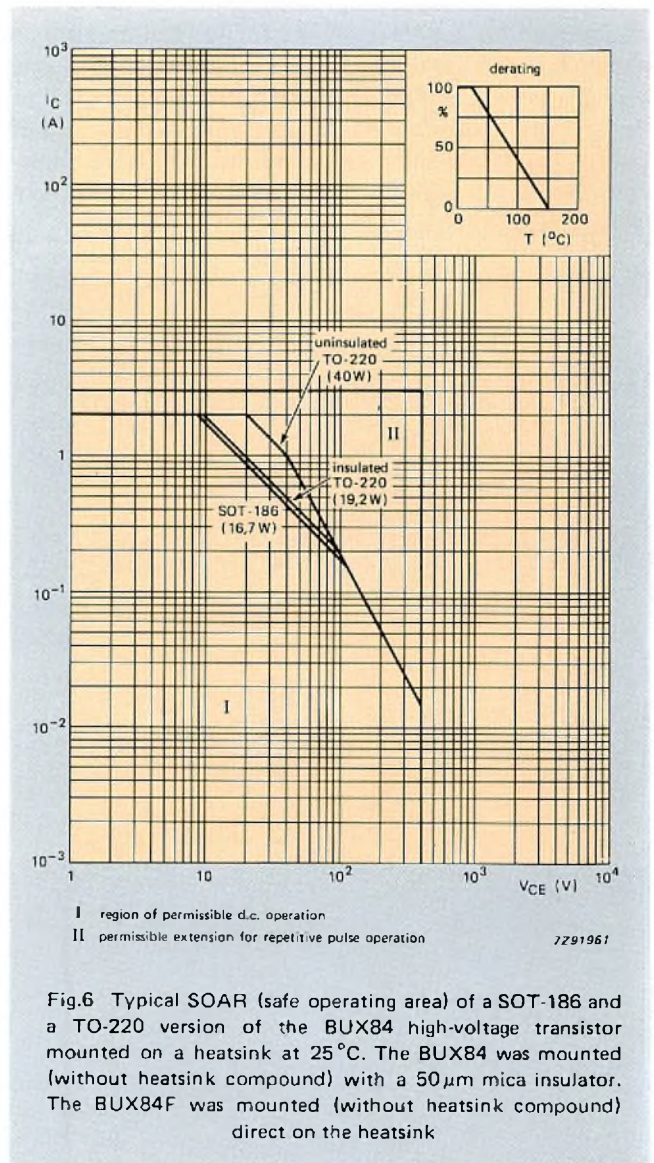
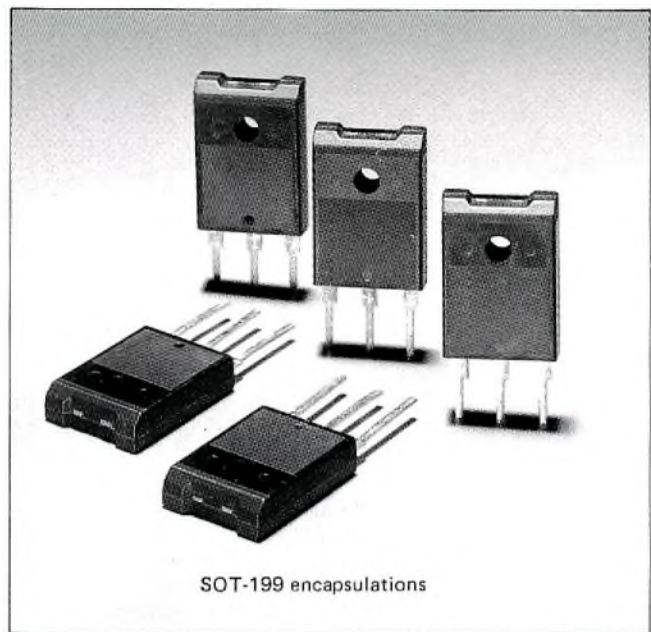


Fig.6 Typical SOAR (safe operating area) of a SOT-186 and a TO-220 version of the BUX84 high-voltage transistor mounted on a heatsink at 25 °C. The BUX84 was mounted (without heatsink compound) with a 50 μm mica insulator. The BUX84F was mounted (without heatsink compound) direct on the heatsink

with a separate insulator, see Fig.6, because the total thermal resistance from the device junction to heatsink is approximately equal in each case.  $R_{th\ j-mb}$  is the same because the same dies and the same alloy bonding of dies to headers are used, and  $R_{th\ mb-h}$  is about the same. However, the separate insulator required for TO-220 and SOT-93 encapsulations is a well-known potential cause of high contact thermal resistances, eliminated by the integral insulators of the new encapsulations.

For TO-220 and SOT-93 components mounted directly on to a heatsink (not practical in most applications),  $R_{th\ mb-h}$  is of course lower than for either an insulated TO-220/SOT-93 mounting or SOT-186/SOT-199 mounting.

Table 2 gives an overview of  $R_{th\ mb-h}$  for several plastic encapsulations with and without insulators. Even though the thickness of the insulator of the new encapsulations is about ten times that of the mica insulator of a conventional mounting, the thermal performance is as good as standard TO-220 or SOT-93, owing to the design of the new lead-frames and the thermal conductivity of the insulating layer.



**TABLE 2**  
 **$R_{th\ mb-h\ max}$  for several plastic encapsulations**

encapsulation	insulation	$R_{th\ mb-h\ max}$ (K/W)			
		clip mounting		screw mounting	
		with heatsink compound	without heatsink compound	with heatsink compound	without heatsink compound
SOT-186	375 $\mu\text{m}$ epoxy <sup>1)</sup>	2,5	5,0	2,5	3,0
TO-220	50 $\mu\text{m}$ mica	1,5	4,0	1,6	4,5
TO-220	250 $\mu\text{m}$ alumina	0,8	–	–	–
TO-220	Silpad 400 <sup>2)</sup>	–	6,0	–	–
TO-220	direct mounting	0,3	1,5	0,5	1,4
SOT-199	475 $\mu\text{m}$ epoxy <sup>1)</sup>	1,5	3,0	1,5	3,0
SOT-93	50 $\mu\text{m}$ mica	0,8	3,0	0,8	2,2
SOT-93	Silpad 400 <sup>2)</sup>	–	4,0	–	4,0
SOT-93	Cho-therm 1674 <sup>3)</sup>	–	2,5	–	2,5
SOT-93	direct mounting	0,3	3,0	1,5	3,0

<sup>1)</sup> integral insulator

<sup>2)</sup> silicone rubber with fibre glass

<sup>3)</sup> silicone rubber.

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# YJ1600 magnetron for microwave heating up to 6 kW

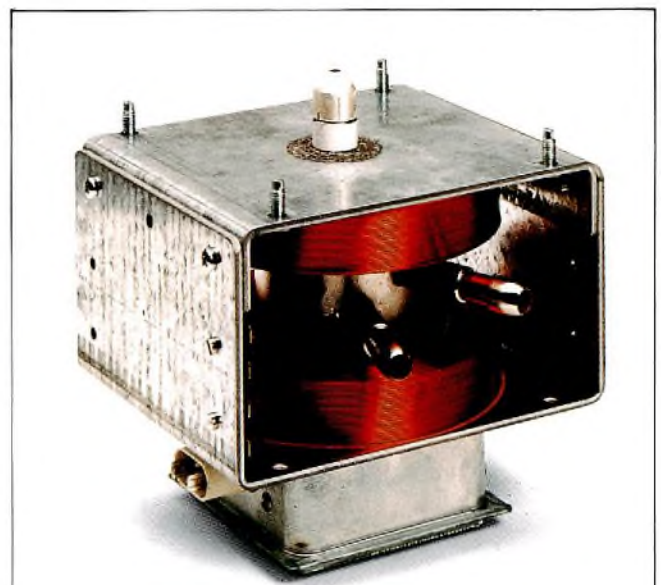
P. F. DE JONGH and S. B. WORM

The YJ1600 is a fixed-frequency continuous-wave magnetron for microwave heating. It sets a new standard for compactness, efficiency and installation ease. The output power can be continuously adjusted from 0,5 kW to 5 kW.\* For higher powers, two or more tubes can operate from one high-voltage supply. Control and stabilization of the output power are straightforward. The YJ1600 uses permanent-magnet and electromagnet field generation to enhance operating flexibility and to reduce the total cost of microwave generators.

The main features of the YJ1600 are:

- low-voltage/low-power stabilization and regulation by using an electromagnet which cuts control circuit complexity and cost, and simplifies the high-voltage supply
- instant response to variation of the electromagnet field permits instant adaptation to process requirement variations, hence optimal energy use and improved product quality
- can be operated without a circulator up to 5 kW output power (in the sink region) provided  $v.s.w.r. \leq 4$
- no stray magnetic field
- no constraints on mounting position
- high basic efficiency
- integrated cathode filter prevents spurious radiation
- can be coupled directly into the waveguide.

\* output powers up to 6 kW are possible.



The YJ1600 is a continuous-wave magnetron for microwave heating up to 6 kW. It has an efficiency of up to 72%. In addition, the combination of permanent-magnet and electromagnet field generation with instant response to changes in the latter ensures optimum energy use. It is compact (158 mm x 150 mm x 120 mm) for its output power, produces no stray magnetic field and there are no constraints on mounting position

**TABLE 1**  
**Quick reference data on the YJ1600; v.s.w.r. = 2,5 in the sink phase**

		output power		
		0,5 to 5 kW	6 kW	
frequency, fixed within the range	f	2,45 to 2,47	2,45 to 2,47	GHz
output power control and stabilization		by electromagnet	by electromagnet	
anode voltage, peak	V <sub>ap</sub>	7,2	7,2	kV
anode current	I <sub>a</sub>	100-950	1150	mA
filament voltage:				
during warm-up	V <sub>f</sub>	5	5	V
during operation	V <sub>f</sub>	0-4	0	V
filament current during warm-up	I <sub>f</sub>	33	33	A
efficiency		72%	72%	
maximum v.s.w.r.		4	*	
cooling (typ.):				
anode block		2 ℓ/m water	2 ℓ/m water	
r.f. filter box		120 ℓ/m air	120 ℓ/m air	
antenna		60 ℓ/m air	60 ℓ/m air	
mounting position		any	any	
mass (typ.)		4,3	4,3	kg

\* For 6 kW output power, the tube must only be operated with a v.s.w.r. of about 2,5 in the sink phase, see main text.

Table 1 gives additional data on the YJ1600.

## CONSTRUCTION

The YJ1600 is an integral-magnet, metal-ceramic, continuous-wave magnetron with integral r.f. cathode filter. The tube has a strapped-vane resonator tuned to operate at 2460 MHz and a metal-ceramic antenna. A directly-heated carburised thoriated tungsten cathode gives a very short warm-up time and long tube life.

The magnetic field in the resonator is produced by two ferrite permanent magnets surrounded by two coils used to alter the magnetic field and therefore the microwave power generated. The high coercivity of the permanent magnets permits large field variations without degrading the permanent field. The combination of permanent magnet and electromagnet simplifies the power supply.

## CONNECTION TO R26 WAVEGUIDE

The microwave output of the YJ1600 can be fed directly into an R26 rectangular waveguide via a coupling section, see Reference. Provided the v.s.w.r. in the waveguide is  $\leq 4$ , the YJ1600 can be operated up to 5 kW without a circulator.

To prevent any arcing in the waveguide from reaching the magnetron, a photodetector whose output can be used to switch off the anode voltage of the magnetron has been incorporated in the coupling section.

A measuring probe (type 55386) for taking "cold" measurements of the output loading of the magnetron is available. Instead of the magnetron, the probe is connected to the waveguide during testing. It has an N-type connector and the v.s.w.r. and phase at the reference plane of the connector are the same as those on the axis of the YJ1600's antenna. The dimensions of the probe and of the YJ1600 are given in the Reference.

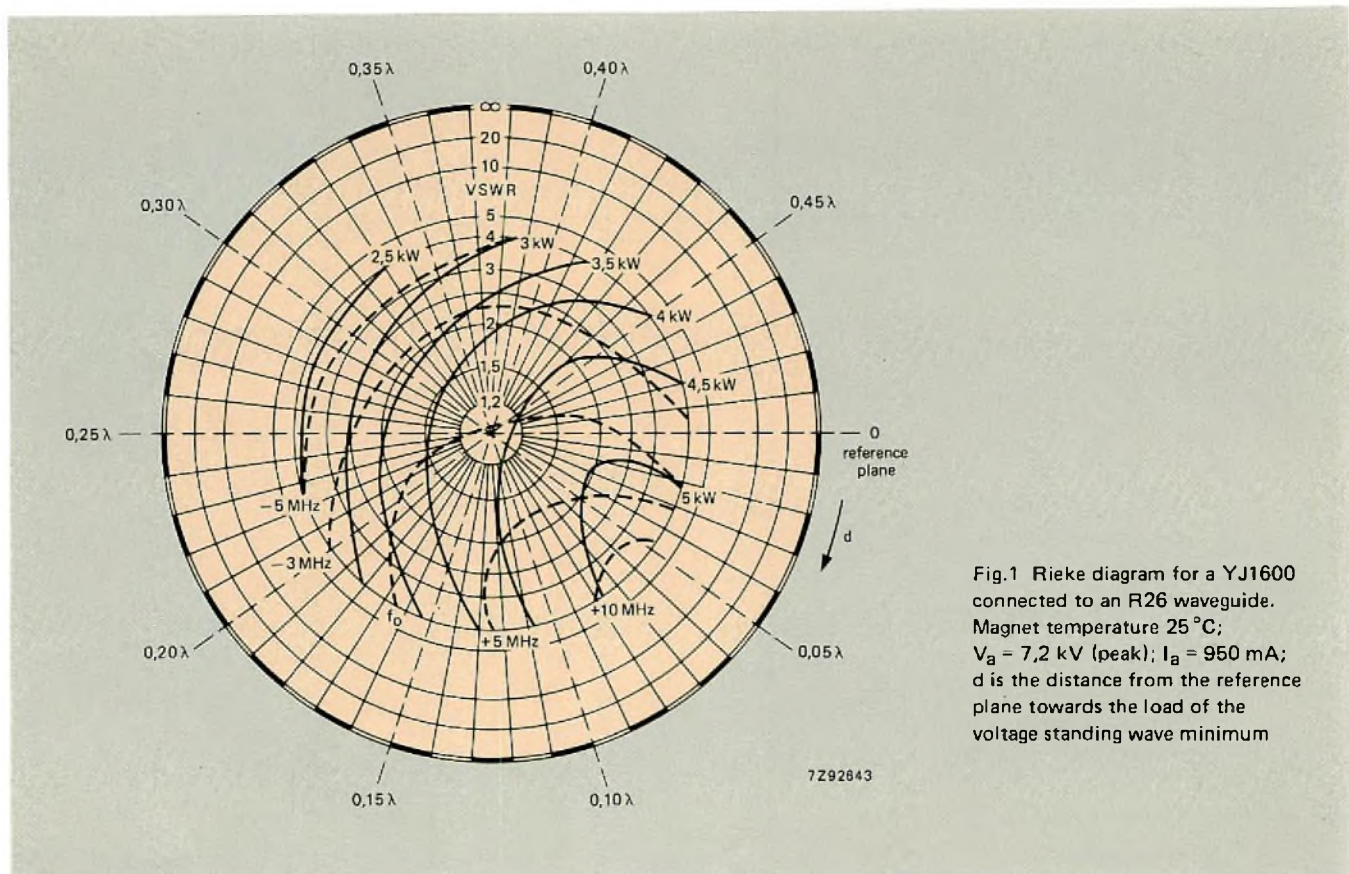


Fig.1 Rieke diagram for a YJ1600 connected to an R26 waveguide. Magnet temperature 25 °C;  $V_a = 7,2$  kV (peak);  $I_a = 950$  mA;  $d$  is the distance from the reference plane towards the load of the voltage standing wave minimum

**RIEKE DIAGRAM**

Figure 1 is the Rieke diagram for a YJ1600 connected to an R26 waveguide. The reference plane is the transverse plane passing through the antenna axis. The maximum output power of 5 kW is obtained near the sink region with a distance from the reference plane to the voltage minimum of the standing wave of about  $0,05\lambda$  and a v.s.w.r. of about 2,5. Continuous operation of the magnetron in the antisink region should be avoided because the efficiency is low and the life of the tube will be shortened.

For maximum efficiency, the magnetron should be loaded for a v.s.w.r. of 2,5 in the direction of the sink phase. This can be realised by a reflector in the waveguide coupling section. The reflector can be a metal cylinder. To load the magnetron in the sink phase, the distance from the centre of the reflector to the antenna axis should be  $109 \pm 0,5$  mm, if the output of the coupling section sees a matched load. To prevent a mismatch, the use of a circulator is recommended. For 6 kW operation, a circulator should always be used.

**PRINCIPLE OF POWER CONTROL**

The input characteristics of the YJ1600 are shown in the performance chart of Fig.2 with, as parameter, the electromagnet coil current ( $I_m$ ) used to alter the output power ( $W_o$ ) of the magnetron.

With the electromagnet turned off ( $I_m = 0$ ), the operating point on the  $V_a/I_a$  characteristic is determined solely by the field in the interaction space between the anode and cathode due to the permanent magnets. This point can be moved by energizing the electromagnet, for example, to alter the anode current when the mains voltage is constant, or to maintain a constant anode current for a varying mains voltage.

In Fig.2, load lines for the high-voltage supply have been plotted for noninal, nominal plus 10% and nominal minus 10% mains voltage. The slope of each load line,  $\tan \alpha$ , is:

$$\tan \alpha = \frac{\Delta V_i}{\Delta I_i} = R_i$$

where

- $V_i$  is the voltage of the h.v. supply
- $I_i$  is the h.v. supply current
- $R_i$  is the internal impedance of the supply.

At nominal mains voltage and a coil current of  $-1,7$  A, the typical operating point of the magnetron is  $P_1$ , given by the intersection of the  $V_a/I_a$  curve with the load line  $V_i/I_i$  at nominal mains voltage.

At  $P_1$ , the anode voltage  $V_a = 7,2$  kV, the anode current  $I_a = 0,95$  A and the output power  $W_o = 5$  kW. To reduce the output power from 5 kW to 1 kW, the coil current has to be

reduced (made more positive). Reducing  $I_m$  to  $-0,7\text{ A}$  moves the operating point along the load line to  $P_2$  where  $V_a = 7,35\text{ kV}$ ,  $I_a = 0,21\text{ A}$  and  $W_o = 1\text{ kW}$ .

From Fig.2, it is also clear that if the slope of the load line of the supply is small, only a small change in coil current will be needed to produce a large change in output power. Therefore, the internal impedance of the h.v. supply should be low.

In a working magnetron, not all the electrons contribute to the generation of microwave power. After their energy has been increased by the r.f. field, some electrons return to the cathode, striking it with a kinetic energy high enough to increase its surface temperature considerably. This effect, known as backbombardment, depends on the mean anode current of the magnetron. To maintain an acceptable cathode temperature, the filament voltage of the YJ1600 must be reduced in accordance with Fig.3 as the anode current increases.

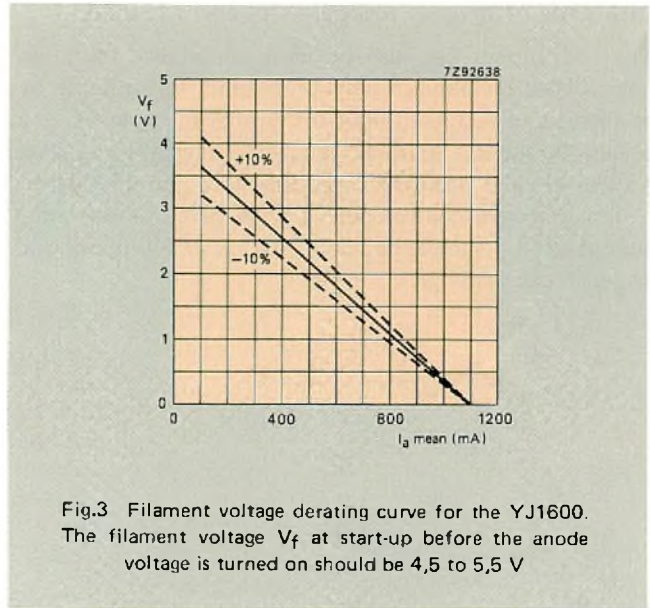


Fig.3 Filament voltage derating curve for the YJ1600. The filament voltage  $V_f$  at start-up before the anode voltage is turned on should be 4,5 to 5,5 V

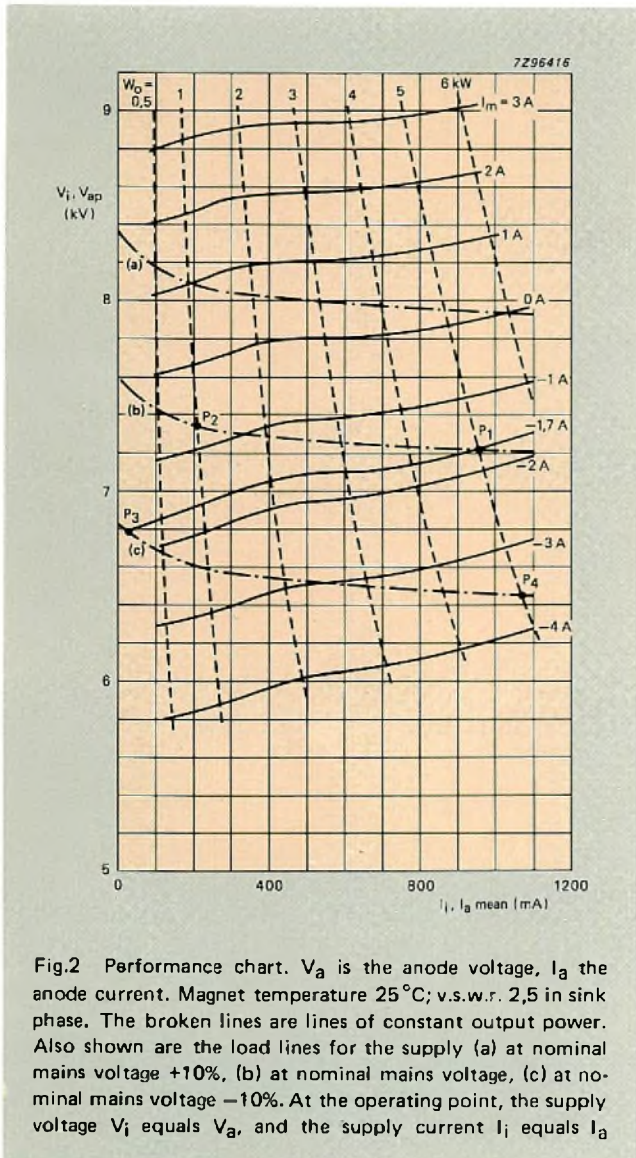


Fig.2 Performance chart.  $V_a$  is the anode voltage,  $I_a$  the anode current. Magnet temperature  $25^\circ\text{C}$ ; v.s.w.r. 2,5 in sink phase. The broken lines are lines of constant output power. Also shown are the load lines for the supply (a) at nominal mains voltage +10%, (b) at nominal mains voltage, (c) at nominal mains voltage -10%. At the operating point, the supply voltage  $V_i$  equals  $V_a$ , and the supply current  $I_i$  equals  $I_a$

### CONSTANT INPUT POWER STABILIZATION

The output power of a microwave generator using the YJ1600 can be influenced by:

- mains voltage variations (see Fig.3)
- an increase in temperature of the ferrite magnets. This weakens the magnetic field, lowering the anode voltage
- changes in the r.f. load which alter the anode voltage at a given anode current. For example, starting from the typical load condition of a v.s.w.r. of 2,5 in the sink phase (see Fig.2) and shifting to the anti-sink region causes the anode voltage to decrease.

Because the efficiency of the YL1600 is virtually constant for a fixed load under all operating conditions, to stabilize the output power it's only necessary to stabilize the *input* power. Constant-input-power stabilization is suitable for most applications using the YJ1600. However, for a varying load, the efficiency of the magnetron will vary depending on the operating point on the Rieke diagram.

### Mains voltage variations

At the operating point  $P_1$  in Fig.3, the output power is 5 kW at nominal mains voltage and a coil current of  $-1,7\text{ A}$ . With no stabilization, if the mains voltage falls by 10% say, the operating point moves to  $P_3$ , corresponding to an output power of less than 0,5 kW. To keep the output power at 5 kW for a 10% fall in mains voltage, the desired operating point is  $P_4$ , which can be reached by increasing the coil current to  $-3,6\text{ A}$ . At  $P_4$ , the input power  $V_a I_a$  is the same as that at  $P_1$ , namely 6,83 kW, and because the efficiency of the magnetron is virtually constant between  $P_1$  and  $P_4$ , the output power is stabilized.

### **Influence of magnet temperature and r.f. load**

The coil current can also be used to stabilize the input power when the anode voltage is lowered, for example, by an increase in temperature of the permanent magnets, or a change in the r.f. load. In each case, increasing  $I_m$  (i.e. making it more positive) keeps the input power constant.

For effective control over a wide range of operating conditions,  $I_m$  should be about  $-1.7\text{ A}$  at full power and nominal mains voltage.

### **POWER SUPPLIES**

Two supplies for continuous control of the output power over the full operating range of the YJ1600 are described in the Reference. Each supply uses constant-input-power stabilization.

### **REFERENCE**

YJ1600 magnetron for microwave heating up to 6 kW. Philips Elcoma Technical Publication 219, ordering code 9398 054 60011.

# Abstracts

## Parallel processing and pipelining usher DSP into the future

When standard microprocessors, constrained by their von Neumann architectures and weak arithmetic ability, proved inadequate for digital signal processing (DSP), the first specialized DSP chips appeared. These were fortified with Harvard-like parallel architecture, multiplication-accumulation hardware and instruction pipelines. Current stage of development sees these chips relying on faster IC technologies and even greater degrees of parallelism in their architecture. Two DSP chips falling into this category are the new PCB5010 and PCB5011, the former with data ROM and program memory, the latter without. The chips are realized in the latest high-speed CMOS technology, and with their pipelining mechanism, they take only 125 ns to complete an instruction.

## Thermal resistance of SO and PLCC packages

A major concern for users of surface-mounted integrated circuits (SM ICs) is increased thermal dissipation arising from packing more devices on a PCB. To assist them in their thermal calculations, this article shows how to measure the thermal resistance of plastic-packaged SM ICs (both SO and PLCC types), and compares the graphically presented results with data for plastic DIL packages. The article also discusses the factors that influence the thermal resistance characteristics.

## ZrO<sub>2</sub> oxygen sensor

Conventional oxygen sensors are often bulky and expensive. The sensor described is small, relatively inexpensive and, unlike many oxygen sensors, doesn't require a reference gas. The sensor can be operated in such a way that the temperature-dependence of the output is virtually zero, simplifying control circuitry. A wide range of operating temperatures and a rugged construction make the sensor ideal for analysing the flue gases in gas and oil-fired central heating boilers and industrial burners and the exhaust gases of internal combustion engines.

## State-of-the-art ICs simplify SSB receiver design

Single-sideband (SSB) transmission has served well for decades in radio and telephone systems. Unfortunately, cost considerations have historically limited its use to only the most demanding applications. Today, however, state-of-the-art ICs allow the design of low-cost SSB receivers that perform as well as their expensive predecessors.

## Speech synthesis – the complete approach with the PCF8200

This article introduces a CMOS speech synthesizer using formant synthesis for generating high quality speech from digital code. The synthesizer is intended for use in microprocessor-controlled systems where the speech code is stored in a separate memory. A programmable bit rate allows a large vocabulary to be stored in a small memory – typically 40 seconds of speech in a 64 K memory. Applications are in vehicle information systems, personal computers and annunciators. Besides the synthesizer, a speech development system for generating the codes for the synthesizer is described.

## Line-locked digital colour decoding

In a tv receiver with digital video-signal-processing, the rate at which the analog video is sampled is an important design criterion because all subsequent processing is related to this rate. Although asynchronous video-processing is possible, it is advantageous to link the sampling rate to the signal frequencies, such as a harmonic of the colour subcarrier frequency or the line frequency. For picture processing, picture conversion to other scanning frequencies and new features with line and field memories, line-locked sampling simplifies picture processing compared with a subcarrier-locked decoder. In this article, the principles of a line-locked digital colour decoder are described.

## In-line system for surface-mount assembly accepts large circuits boards

MCM-VI is the latest addition to the now well-known series of MCM modular placement systems, and answers the need of consumer electronics manufacturers to extend the benefits of surface-mount assembly to larger circuit boards. MCM-VI can accommodate boards ranging up to 250 mm by 430 mm and like other systems in the series, it uses placement modules in which up to 32 pick-and-place pipettes on a servo-driven beam accept SMDs from feed tapes and convey them to software-defined placement sites.

## Insulated encapsulations for easier mounting of power semiconductors

Many premature failures of power semiconductors can be attributed to poor assembly of the insulating accessories and poor machining of the heatsink, causing overheating due to insufficient conduction of heat from the semiconductor chip, and flashover at high voltages. To overcome these problems, two encapsulations which incorporate an insulator have been developed. The new encapsulations are direct replacements for standard TO-220 and SOT-93 encapsulations in virtually all applications and the same chips are used in the insulated and standard versions.

## YJ1600 magnetron for microwave heating up to 6 kW

A combination of permanent magnet and electromagnetic field generation with instant response to changes in the latter for optimum energy use is just one advantage of the YJ1600 continuous-wave magnetron. In addition, the YJ1600 is compact for its output power, produces no stray magnetic field and there are no constraints on mounting position.

## Parallel- und Pipeline-Verarbeitung sind zukunftsweisend für die digitale Signalverarbeitung

Als sich herausstellte, dass Standard-Mikrocontroller wegen ihrer von-Neumann-Architektur und ihrer schwach ausgeprägten arithmetischen Fähigkeiten den Anforderungen der digitalen Signalverarbeitung (DSP) nur ungenügend entsprechen, erschienen die ersten dafür spezialisierten integrierten DSP-Schaltungen. Diese waren mit einer parallel gestalteten Hardware-ähnlichen Architektur, einer Hardware zur Multiplikation/Akkumulation sowie mit Befehls-Pipelines ausgerüstet. Beim gegenwärtigen Entwicklungsstand beruhen die Schaltungen auf schnelleren IC-Techniken und einem noch grösseren Mass an Parallelität ihrer Architektur. Zu dieser neuen Kategorie von integrierten DSP-Schaltungen zählen der PCB5010 und PCB5011, erstere Schaltungen mit Daten-ROM und Programmspeicher, letztere ohne diese Speicher. Die Chips werden in modernster High-Speed-CMOS-Technik hergestellt und benötigen wegen ihrer Pipeline-Verarbeitung nur 125 ns zur Befehlsausführung.

## Thermischer Widerstand von SO- und PLCC-Gehäusen

Ein wichtiges Kriterium für Anwender von Integrierten Schaltungen für Oberflächenmontage (SM-ICs) ist die höhere thermische Verlustleistung, die aus der grösseren Packungsdichte auf der Printplatte resultiert. Zur Unterstützung des Entwicklers bei seinen thermischen Berechnungen zeigt dieser Beitrag, wie der thermische Widerstand von SM-ICs mit Plastikgehäuse (sowohl SO- als auch PLCC-Typen) gemessen wird. Die Ergebnisse werden graphisch dargestellt und mit den Daten für Plastik-DIL-Gehäuse verglichen. Darüber hinaus geht der Beitrag auf die Faktoren ein, die die thermischen Widerstandseigenschaften beeinflussen.

## Zirkondioxid-Sauerstoffsensoren

Herkömmliche Sauerstoffsensoren sind oftmals sperrig und teuer. Der hier beschriebene Sensor ist klein, relativ preisgünstig und benötigt im Gegensatz zu vielen Sauerstoffsensoren kein Bezugsgas. Der Sensor kann so betrieben werden, dass die Temperaturabhängigkeit der Ausgangsspannung praktisch Null ist, was die periphere Schaltung vereinfacht. Wegen seines grossen Betriebstemperaturbereichs und seines robusten Aufbaus ist der Sensor ideal geeignet zur Analyse von Rauchgasen aus gas- und ölbetriebenen Zentralheizungskesseln und Industriebrennern sowie von Abgasen aus Verbrennungsmotoren.

**Spezielle Integrierte Schaltungen vereinfachen die Entwicklung von Einseitenband-Empfängern**

HF-Übertragungen mit Einseitenbandmodulation (SSB) haben sich seit Jahren in Radio- und Telefonsystemen gut bewährt. Leider haben die relativ hohen Kosten den Einsatz dieses Verfahrens bisher auf die notwendigsten Anwendungsfälle beschränkt. Heute stehen jedoch spezielle Integrierte Schaltungen zur Verfügung, die den Bau von preiswerten SSB-Fmpfängern ermöglichen, welche ebenso arbeiten wie ihre teuren Vorgänger.

**Sprachsynthese – die komplette Lösung mit PCF8200**

Dieser Beitrag beschreibt einen neuen CMOS-Sprachsynthesizer, der nach dem Prinzip der Formantensynthese aus digitalem Sprachcode Sprache hoher Qualität erzeugt. Der Synthesizer ist für den Einsatz in Mikroprozessor-gesteuerten Systemen vorgesehen, bei denen der Sprachcode in einem separaten Speicher abgelegt wird. Eine programmierbare Bit-Rate erlaubt die Unterbringung eines grossen Sprachvorrats in einem kleinen Speicher – typischer Wert: 40 Sekunden Sprache in einem 64K-Speicher. Typische Applikationsmöglichkeiten bestehen in Automobil-Informationssystemen, Personal Computern sowie Auskunfts-, Warn- und Alarmsystemen in öffentlichen Verkehrseinrichtungen, in Industrie und Büros. Neben dem eigentlichen Synthesizer wird auch ein Spracheditiersystem beschrieben, das den Sprachcode für den Synthesizer erzeugt.

**Zeilenverkoppelte digitale Farbdecodierung**

In einem Fernschempfänger mit digitaler Videosignalverarbeitung ist die Taktfrequenz, mit der das analoge Videosignal abgetastet wird, ein entscheidendes Entwurfskriterium, da alle nachfolgenden Verarbeitungsschritte von dieser Taktfrequenz abhängen. Obgleich eine asynchrone digitale Videosignalverarbeitung grundsätzlich durchgeführt werden kann, ist es vorteilhaft, die Abtastezeit an eine massgebende Signalfrequenz zu koppeln, wie etwa eine Harmonische der Farbträger- oder Zeilenfrequenz. Für Verbesserungen der Bildqualität, für Normwandlungen auf andere Zeilen- und Bildfrequenzen sowie für neue "Features" mit Hilfe von Zeilen- und Bildspeichern vereinfacht eine zeilenfrequenzverkoppelte Abtastung die Bildsignalverarbeitung, verglichen mit Systemen, die eine Farbträgerfrequenzverkopplung verwenden. In diesem Artikel werden die Prinzipien eines zeilenfrequenzverkoppelten digitalen Farbdecoders beschrieben.

**In-line-System für Oberflächenmontage nun auch für grössere Printplatinen geeignet**

MCM-VI ist die neueste Ergänzung unseres inzwischen allseits bekannten Programms an modular aufgebauten MCM-Bestückungsautomaten. Damit wird den Anforderungen der Konsumelektronik-industrie, die Vorteile der Oberflächenmontage auch bei grösseren Printplatinen zu nutzen, Rechnung getragen. MCM-IV kann Platinen mit Abmessungen bis zu 250 mm x 430 mm verarbeiten. Sie arbeitet wie die übrigen Systeme des MCM-Programms mit Bestückungsmodulen, bei denen bis zu 32 "Pick and Place"-Pipetten an einem servogesteuerten Aufnehmer SMDs aus Gurten entnehmen und zu über die Software definierten Bestückungsorten befördern.

**Isoliertes Gehäuse zur einfacheren Montage von Leistungshalbleitern**

Viele Frühhausfälle von Leistungshalbleitern sind mangelhaftem Aufbau des Isolationszubehörs und schlechter Bearbeitung des Kühlblechs zuzuschreiben, wodurch Überhitzung infolge unzureichender Wärmeableitung vom Halbleiterchip sowie Überschlüge bei hohen Spannungen verursacht werden. Um diese Schwierigkeiten zu überwinden, sind zwei Gehäuse entwickelt worden, deren Isolation integriert ist. Die neuen Gehäuse ersetzen unmittelbar die Standard-Gehäuse TO-220 und SOT-93 in praktisch allen Anwendungen. In der isolierten und in der Standard-Version werden die gleichen Chips verwendet.

**YJ1600 – ein Dauerstrichmagnetron für die Erwärmung mit Mikrowellen bis 6 kW**

Die Kombination aus einem Permanentmagneten und einem Elektromagneten beim Dauerstrichmagnetron YJ1600 bietet bei der Erzeugung von Mikrowellen die Möglichkeit, die Ausgangsleistung rasch zu ändern und damit den Vorteil optimaler Energieausnutzung. Weiterhin ist das Dauerstrichmagnetron YJ1600 für seine Ausgangsleistung kompakt aufgebaut, es ruft keine magnetischen Streufelder hervor, und es bestehen keine Einschränkungen in seiner Einbaulage.

**Le traitement en simultanéité et "pipeline" préfigure le traitement numérique des signaux de l'avenir**

Les premières puces spécialisées dans le traitement numérique des signaux sont apparues lorsque les microprocesseurs standard s'y sont révélés inappropriés, car handicapés par leurs architectures de von Neumann et leur faible puissance arithmétique. Elles ont été renforcées par une architecture parallèle type Harvard, une unité de multiplication-accumulation et des pipelines d'instruction. Au stade actuel de leur développement, ces puces bénéficient de technologies de circuits intégrés plus rapides et aussi d'un plus grand parallélisme de leurs architectures. Les deux nouveaux circuits de traitement numérique de signaux PCB5010 et PCB5011 relèvent de cette catégorie, le premier avec ROM de données et mémoire de programmes, le second sans ROM. Ces puces sont réalisées en technologie CMOS ultra-rapide 2 µm. Grâce à l'architecture en pipeline, l'exécution d'une instruction ne prend que 125 ns.

**Résistance thermique des boîtiers SO et PLCC**

Un gros souci des utilisateurs de circuits intégrés montés en surface est l'accroissement de la dissipation thermique due au grand nombre de dispositifs sur un même circuit imprimé. En vue de les aider dans leurs calculs thermiques, cet article montre comment mesurer la résistance thermique de circuits intégrés CMS en boîtier plastique (de type SO ou PLCC) et compare les résultats graphiques aux données correspondantes de boîtiers DIL plastique. L'article analyse également les facteurs qui influent sur les caractéristiques de la résistance thermique.

**Capteur d'oxygène à ZrO<sub>2</sub>**

Les capteurs d'oxygène classiques sont fréquemment volumineux et coûteux. Le capteur décrit est petit, relativement peu coûteux et, contrairement à de nombreux autres modèles, il ne nécessite pas l'emploi d'un gaz de référence. Le capteur peut être utilisé de telle manière que sa tension de sortie soit pratiquement indépendante de la température, ce qui simplifie les circuits de commande. Sa gamme étendue de températures de fonctionnement et la robustesse de sa construction le rendent idéal pour l'analyse des gaz de combustion des chaudières de chauffage central à gaz et à mazout et des brûleurs industriels, ainsi que des gaz d'échappement des moteurs à combustion interne.

**Des circuits intégrés évolués simplifient la conception des récepteurs BLU**

L'émission sur bande latérale unique (BLU) a rendu de bons et loyaux services pendant des décennies dans les systèmes radio-phoniques et téléphoniques. Malheureusement, du fait de son coût élevé, son emploi est resté limité aux applications les plus exigeantes. Mais actuellement, l'emploi de circuits intégrés évolués permet de concevoir des récepteurs BLU moins chers et aux performances comparables à celles de leurs coûteux prédécesseurs.

**Synthèse de la parole – traitement complet à l'aide du PCF8200**

Cet article présente un synthétiseur de parole CMOS de haute qualité qui utilise un code numérique et la synthèse de formants. Ce synthétiseur est destiné aux systèmes pilotés par microprocesseur, où le code vocal est enregistré dans une mémoire séparée. Une cadence de bits programmable permet d'enregistrer un vocabulaire étendu dans une petite mémoire – typiquement 40 secondes de parole dans une mémoire de 64 K. L'appareil est destiné aux systèmes d'information des véhicules, ordinateurs personnels et avertisseurs. L'article décrit également un système de développement pour la génération de codes, destiné à ce synthétiseur.

**Décodage couleur numérique à verrouillage de ligne**

Dans un téléviseur à traitement numérique des signaux vidéo, la fréquence d'échantillonnage du signal vidéo analogique est un important critère de conception, parce que tous les traitements ultérieurs sont fonction de cette fréquence. Bien que le traitement asynchrone des signaux vidéo soit possible, il est avantageux d'associer la fréquence d'échantillonnage aux fréquences du signal, par exemple à une harmonique de la fréquence de sous-porteuse couleur ou à la fréquence de ligne. Pour les besoins du traitement de l'image de la conversion de l'image à d'autres fréquences d'analyse et de la réalisation de nouvelles versions à mémoire de ligne et de trame, l'échantillonnage à verrouillage de ligne simplifie de traitement de l'image en comparaison d'un décodeur à verrouillage de sous-porteuse. Les principes d'un décodeur couleur numérique à verrouillage de ligne sont décrits dans cet article.

### Un système en ligne permet le montage de composants en surface sur des cartes plus grandes

Le MCM-VI est le dernier né de la série maintenant bien connue de systèmes MCM modulaires de placement. Il répond au besoin des constructeurs de matériels électroniques grand public d'étendre à des cartes plus grandes les avantages du montage en surface. Le système MCM-VI peut travailler sur des cartes de dimensions pouvant atteindre 250 mm sur 430 mm et, comme tous les systèmes de la série, il est équipé de modules de placement à 32 pipettes de transfert montées sur un balancier servo-commandé qui reçoivent les CMS en bande et les amènent aux points d'implantation définis par logiciel.

### Boîtier isolé facilitant le montage des semiconducteurs de puissance

Les pannes prématurées des semiconducteurs de puissance peuvent fréquemment être attribuées à la qualité médiocre de l'assemblage des accessoires d'isolement et de l'usinage du dissipateur thermique, provoquant un échauffement excessif dû à l'évacuation insuffisante de la dissipation de la puce, et des courts-circuits aux hautes tensions. Pour résoudre ces problèmes, on a mis au point deux boîtiers incorporant un isolateur. Ceux-ci remplacent directement les boîtiers standard TO-220 et SOT-93 dans pratiquement toutes les applications et les mêmes puces sont utilisées dans les versions isolées et standard.

### Magnétron YJ1600 pour chauffage par micro-ondes jusque 6 kW

La combinaison d'un aimant permanent et de la génération d'un champ électromagnétique, réagissant instantanément aux modifications de ce champ en vue d'un emploi optimal de l'énergie, n'est qu'un des avantages du magnétron YJ1600 à ondes entretenues. De plus, l'YJ1600 est compact pour sa puissance de sortie, il ne produit pas de champ magnétique parasite et sa position de montage n'est soumise à aucune contrainte.

### El proceso en paralelo y el encauzamiento abren una nueva era para el DSP

Los primeros chips para el proceso de la señal digital (DSP) especializados aparecieron cuando los microprocesadores standard, limitados por sus arquitecturas von Neumann y su insuficiente capacidad aritmética, demostraron ser inadecuados para el proceso de la señal digital. Estos chips contaron con la ayuda de una arquitectura en paralelo con la de Harvard, equipos para la acumulación por multiplicación y encauzamientos de instrucciones. La etapa corriente de evolución ve estos chips sujetos a tecnologías de CI más rápidas e incluso a mayores grados de paralelismo en su arquitectura. Dos chips DSP que forman parte de esta categoría son el nuevo PCB5010 y el PCB5011, el primero con una ROM de datos y una memoria de programa, y el último sin ello. Los chips están realizados en la tecnología CMOS de alta velocidad más moderna y su mecanismo de encauzamiento sólo necesita 125 ns para llevar a cabo una instrucción.

### Resistencia térmica de encapsulados SO y PLCC

Una cuestión de gran importancia para los usuarios de circuitos integrados montados en superficie (SM ICs) es el aumento de la resistencia térmica resultante de encapsular más dispositivos en una placa de circuito impreso. Para ayudarles en sus cálculos térmicos, este artículo explica como medir la resistencia térmica de los circuitos integrados montados en superficie, encapsulados en plástico (en los tipos SO y PLCC), y compara los resultados presentados gráficamente con datos para encapsulados de plástico DIL. El artículo estudia también los factores que influyen en las características de la resistencia térmica.

### Sensor de oxígeno ZrO<sub>2</sub>

Los sensores de oxígeno convencionales son a menudo voluminosos y caros. El sensor que describimos es pequeño, relativamente económico y a diferencia de muchos otros sensores de oxígeno no necesita un gas de referencia. El sensor funciona de forma que la dependencia de la temperatura de salida es prácticamente cero, lo que simplifica los circuitos de control. Una amplia gama de temperaturas de funcionamiento y una construcción sólida hacen que el sensor sea ideal para el análisis de los gases de combustión en calderas para calefacción central a gas y aceite, quemadores industriales y de los gases de escape de máquinas de combustión interna.

### Circuitos integrados de avanzadísima tecnología simplifican el diseño del receptor de SSB

La transmisión en banda lateral única (SSB) se ha utilizado durante décadas en radio y sistemas telefónicos. Lamentablemente, sus costos han limitado históricamente su uso a sólo aplicaciones de mucha demanda. Sin embargo, hoy en día los circuitos integrados de avanzadísima tecnología permiten el diseño de receptores de banda lateral única de bajo costo con un funcionamiento tan bueno como el de sus predecesores.

### Síntesis de la palabra – un enfoque completo con el PCF8200

Este artículo está dedicado a un sintetizador CMOS que utiliza síntesis formantes para generar palabras de alta calidad partiendo de un código digital. El sintetizador se ha concebido para uso en sistemas controlados por microprocesador en los que el código de la palabra está almacenado en una memoria aparte. Una velocidad programable de bit permite poner en una pequeña memoria (40 segundos de palabras en una memoria de 64 K) un amplio vocabulario. Sus aplicaciones se han pensado en sistemas de información para vehículos, ordenadores personales y avisadores. Además del sintetizador se describe un sistema formador de palabras para generar los códigos destinados al sintetizador.

### Decodificación digital de color enclavada en línea

En un televisor con proceso digital de la señal de vídeo analógica, la velocidad a la que ésta se muestrea es un criterio importante en el diseño ya que posteriormente todo el proceso está relacionado con esta velocidad. Aunque es posible el proceso de la señal de vídeo asíncrona, conviene ligar la velocidad de muestreo a las frecuencias de la señal, como por ejemplo un armónico de la frecuencia de la subportadora de color o de la frecuencia de línea. Para el proceso de la imagen, conversión de la imagen a otras frecuencias de exploración y nuevas características con memorias de línea y campo, el muestro de línea enclavada simplifica el proceso de la imagen en comparación con un decodificador de subportadora enclavada. En el presente artículo se describen los principios del decodificador digital de color enclavado en línea.

### El sistema en línea para montaje en superficie acepta placas de circuito grandes

El MCM-VI es lo último que se ha añadido a la ya conocida serie de sistemas de montaje modular MCM, y responde a la necesidad manifestada por los fabricantes de aparatos electrónicos de consumo de aumentar los beneficios del montaje en superficie en placas de circuito mayores. El MCM-VI puede ajustar placas de hasta 250 mm por 430 mm y al igual que otros sistemas de la serie utiliza módulos de colocación en los que hasta 32 pipetas de cogida y colocación sobre un haz servo excitado aceptan SMDs de cintas de alimentación y los transportan a determinados lugares definidos por software.

### Encapsulados aislados para un montaje más sencillo de semiconductores de potencia

Muchos de los fallos prematuros en los semiconductores de potencia pueden atribuirse a un deficiente montaje de los accesorios aislantes y a una mala adaptación del disipador térmico, lo que origina un exceso de calentamiento debido a una conducción insuficiente del calor del chip semiconductor y a una descarga disruptiva a altas tensiones. Para poner fin a estos problemas se han diseñado dos encapsulados que incorporan un aislador. Los nuevos encapsulados son sustituciones directas de los normalizados: TO-220 y SOT-93 prácticamente en todas las aplicaciones, utilizándose los mismos chips en las versiones aisladas y standard.

### Magnétron YJ1600 para calentamiento por microonda hasta 6 kW

Una de las ventajas del magnétron de onda continua, YJ1600, es la generación permanente de un campo magnético y otro electromagnético en combinación con una repuesta instantánea a los cambios para un uso óptimo de la energía. Además, el YJ1600 es compacto para su potencia de salida, no origina un campo magnético de radiación y no existen limitaciones para la posición de montaje.



# Authors



Menno ten Have was born in Utrecht in 1958. He studied electronics at the Technical University of Twente in Enschede, The Netherlands, obtaining a Master's Degree in 1983. The same year he joined the Central Applications Laboratory of Philips Electronic Components and Materials Division, Eindhoven, and is currently involved with the development of speech synthesis systems and the use of field memories in digital television.



Peter Anders holds a doctorate in electrical engineering from the University of Bremen, Germany. Since joining Valvo's Application Laboratory, Hamburg in 1983, he has been involved with digital signal processing, and is currently group leader responsible for DSP circuits.



Ton van Kampen graduated with a masters degree in electrical engineering from the University of Delft, The Netherlands. After joining Philips he spent six years in the company's research laboratories and is now strategic product marketing manager responsible for Philips' forthcoming family of digital signal processors.



C. Franx was born in Rotterdam in 1925 and graduated from the Technical University at Delft in 1951. Joining Philips in 1952, he was first involved in the development of quartz crystal elements and, later, of ultrasonic delay lines. From 1969 to 1979 he was concerned with hybrid integrated circuits, interconnection technologies, and solar energy systems. He is currently responsible for electronic subassembly development in the Energy Systems group.



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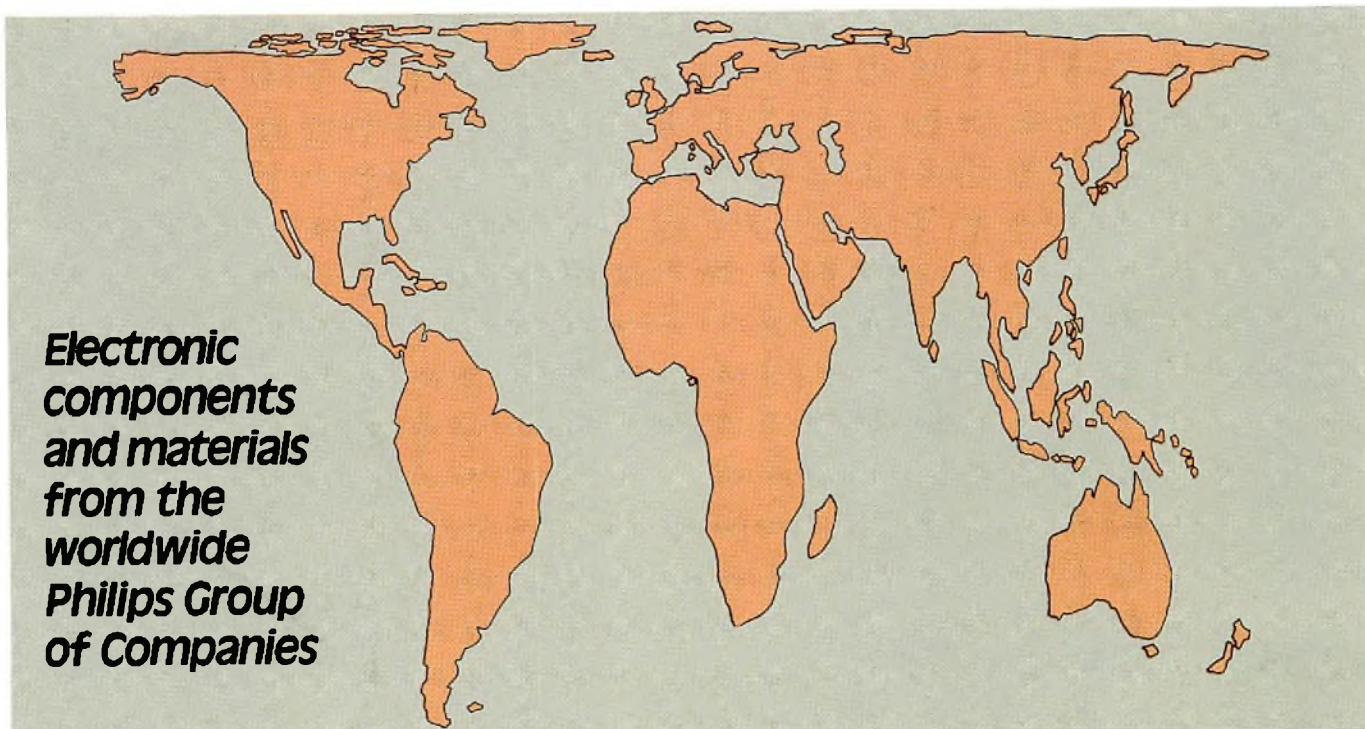
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