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Contents

With the advent of cellular communications systems, mobile radio is facing a period of explosive growth. Formerly an exclusively professional preserve, mobile radio gained its initial consumer stimulus from CB. But the new cellular communications systems can offer a significantly better service and are likely to multiply the user market several thousand-fold, providing opportunities and challenge for communications equipment manufacturers. Building on an enviable reputation in professional r.f. and a well-known capability in large scale production, Elcoma is ready with new generations of consumer r.f. components to serve this demanding new market.

Stand-alone speech development system using a personal computer

M. TEN HAVE and J. DEN OUDEN

Today, synthesized speech can be heard increasingly in lifts, trains, and cars, providing warnings and messages formerly announced by humans or indicated by displays. For the visually handicapped, telephones that speak the numbers dialled and talking typewriters and ovens greatly assist day-to-day life. In the future, developments such as the incorporation of speech output in a compact-disc read-only-memory-based navigation system could revolutionize route planning on the road.

Much of the work associated with speech synthesis is generating the speech codes for the synthesizer. Although manufacturers of synthesizers offer a speech-coding service, this is usually performed on a mainframe computer, making it an expensive and time-consuming proposition for the customer, who must travel to and from the manufacturer.

To solve this problem, we have created a speech-development system for use with personal computers. The system also presents a display of the synthesized speech (Fig.1).

Fig.1 Our speech-development system comprises a hardware I/O for an IBM PC (shown here) or an HP 9816S computer and all the software (on floppy disk) for analyzing, coding and editing speech. A feature of this system is the graphic display of the speech parameters representing the synthesized speech

The fact that coded speech parameters can be displayed graphically, a revolution in speech editing, has simplified editing so much that it can be learned in a day. By using a personal computer, it is possible to generate speech codes at home or at the office in just a few hours.

The system is a hardware input/output device, called the speech adapter box (SAB) for the computer. The SAB which uses an MEA8000 formant synthesizer can be upgraded as new synthesizers become available. The software for analyzing, editing, and coding speech is available for the Hewlett-Packard Co. 9816S and the IBM PC series.

EASIER EDITING

Editing speech to improve the intelligibility of the synthesizer output and to minimize the data rate without loss of speech quality is normally a specialized task. This is because editing systems usually display the speech to be edited on a screen in the form of complex tables of coded speech parameters, which are difficult for an untrained person to understand. The new system was developed to overcome these shortcomings.

In addition to the benefits of a graphical representation of speech parameters, the speech-development system features:

- speech-interactive operation, with which synthesized speech segments or single frames can be pronounced and checked for quality
- software that is arranged in eight modes for optimum user convenience
- menu display of all commands
- keystroke confirmation of all commands that destroy data before the commands are executed.

The procedure for generating speech codes for the MEA8000 synthesizer begins by recording the desired message. The process is completed with the evaluation of the encoded speech in the system in which it will be used (Fig.2).

After the speech to be synthesized has been recorded on tape, the Sample mode is used to sample and digitize the recorded speech, check the amplitude of the digitized speech segments, and select speech segments for analysis, the next stage of speech coding. The sampled speech is stored in memory arrays, see Fig.3, used for sampling, parameter input and edit, and coding. Sampled speech can be displayed (Fig.4) or made audible.

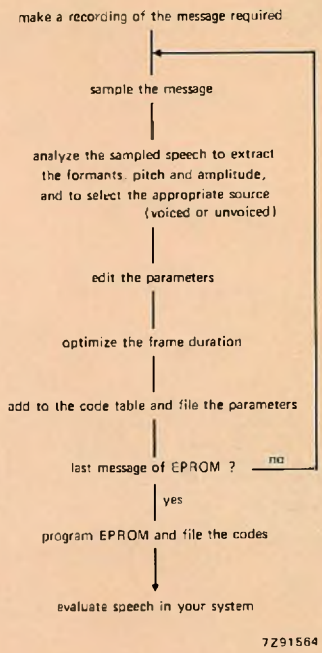


Fig.2 Code-production software is arranged in a modular fashion. Once the synthesized speech has been recorded, it is sampled, analyzed (for several different parameters), edited optimized, and finally added automatically to the existing code table

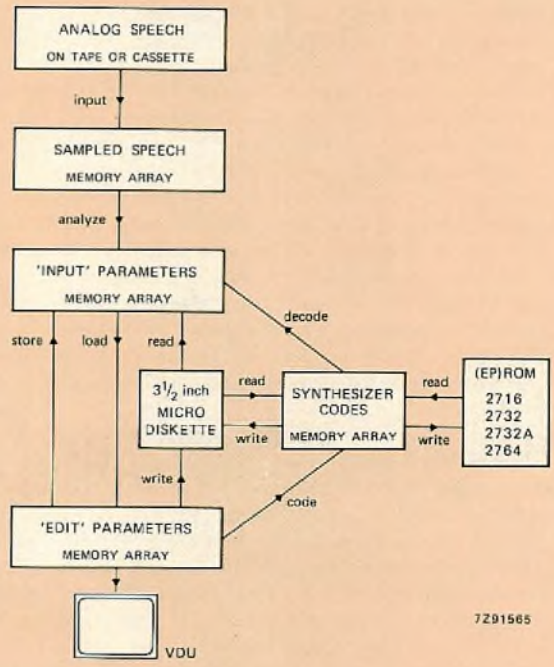


Fig.3 Data flows during the speech coding procedure of Fig.2. Handling speech samples, speech parameters and codes demands a speech development system with extensive data movement facilities

HUMAN SPEECH PRODUCTION MECHANISM

All speech is derived from a periodic signal source or a noise source. During speech, the source and its amplitude are always varying, sometimes quite rapidly. To produce speech, the lungs build up air pressure, causing the previously closed vocal cords to open (Fig.A). As a result, pressure drops, the vocal cords close, and pressure builds up again. This mechanism excites the vocal tract with a periodic train of sawtooth pressure pulses. Sounds generated in this way, for example, the vowels A and E, are called voiced sounds (Fig.B). The frequency of this periodic signal is commonly referred to as pitch. The vocal tract can also be excited with the vocal cords always slightly open, so that air passes continuously through them, causing turbulence in the vocal tract. Sounds produced in this manner, such as sibilants, are called unvoiced sounds.

Situated above the vocal tracts are the pharyngeal, oral, and nasal cavities, which shape the spectrum of the generated sounds. The nasal cavity is accessed through the velum. Speech synthesizers do not simulate the velum and the nasal cavity; consequently, for speech synthesis, the vocal tract can be analyzed as if it were an acoustic tube. This tube is almost closed by the vocal cords at one end and is open at the other, where mouth radiation takes place.

The frequency response of a tube with constant diameter is characterized by a number of equally spaced resonances (Fig.C) at frequencies given by

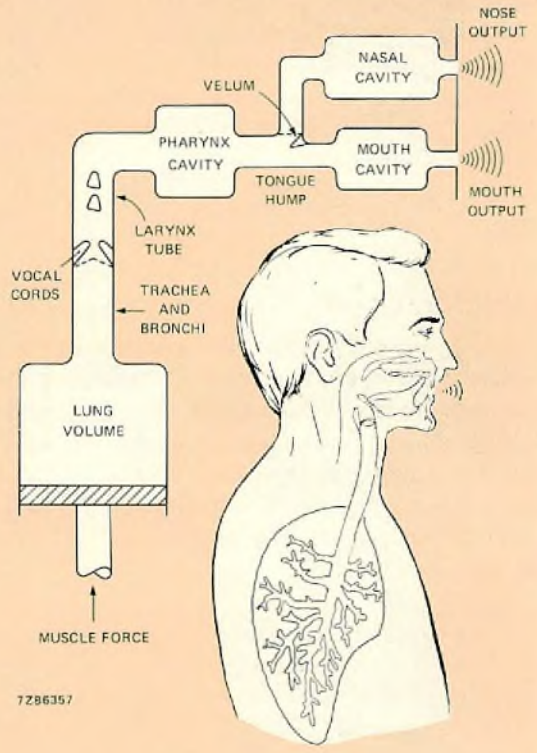
$$f(n) = 340(2n - 1)/4L \text{ Hz}$$

where n = 1, 2, 3, 4, . . ., and L is the tube length in metres. These resonant frequencies are called the formants of the vocal tract. Within a 4-kHz bandwidth (typical of most synthesizers), four formants are present for a male voice (L = 0,175 m) and three for a female voice, because of a woman's shorter vocal tract.

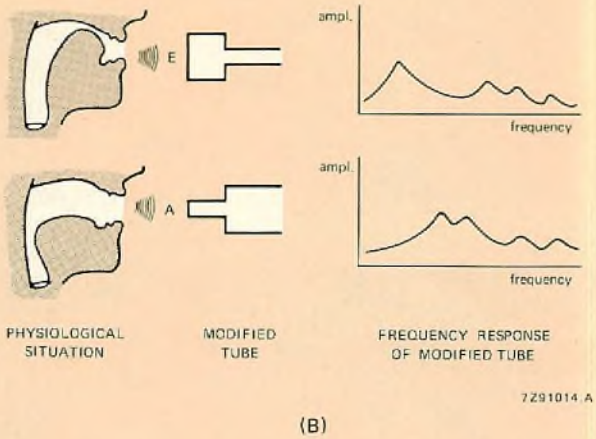
During speech, the shape of the vocal tract is constantly changing. For example, when an E is pronounced, the pharyngeal cavity is large while the oral cavity is small. This increases the frequency of the second formant. When an A is pronounced the situation is reversed, reducing the separation between the first and second formants. Each formant is further characterized by its bandwidth. The first two or three formants are the most important for intelligible speech; most formant synthesizers generate and shape four or five formants.

Until a few years ago, communication between man and machine had been mainly in sign language from visual displays; audible communication was restricted to cries of alarm emitted by beepers, bells, and buzzers. Voice communication was impractical because analog storage of speech required the use of moving parts such as tape drives, which unduly prolonged the retrieval time; digital storage required handling an enormous number of bits. The development of speech synthesis techniques has dramatically reduced the bit rate and the memory required for digital speech synthesis, allowing inexpensive wideband voice channels between machine and man to be implemented.

Three main methods of generating speech are used in speech-synthesizer integrated circuits today: waveform coding, phoneme coding, and vocal-tract modelling.



(A)



(B)

In waveform coding, speech is sampled, digitized, and compressed by eliminating symmetrical redundancy and pauses in the digitized speech. The speech is then stored in a memory. To regenerate a sound, the process essentially is reversed, so the recreated sound closely resembles the original. Very high quality can be obtained when a high bit rate is used – up to 64 kbits/s for a male voice. A disadvantage of waveform coding is the large memory required for even a limited vocubulary.

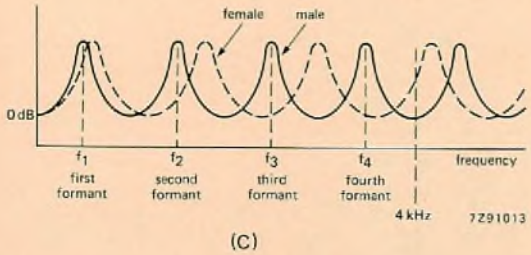
With the phoneme-coding method, spoken words are sliced into their constituent sounds (phonemes), which are stored in memory as a series of codes and reconstructed as desired. Phoneme coding offers very low data rates (typically 70 bits/s) but generates speech of a poor quality, owing to allophones.

For applications requiring a high-quality voice and a substantial vocabulary, vocal-tract modelling using linear predictive coding (LPC) is the most cost effective. In LPC, speech is sampled, digitized, and passed through a digital analyzing filter that shapes the voice-frequency spectrum. The filter is described by coefficients that represent either the shape of the vocal tract or the formant centre frequencies and bandwidths of vocal-tract resonances.

An LPC synthesizer using the latter technique is commonly called a formant synthesizer. An advantage of a formant synthesizer is that the speech parameters controlling the filter have perceptual significance; that is, they are not merely coefficients but represent frequencies and bandwidths. Furthermore, the parameters are fairly insensitive to quantization, which is essential if the amount of data to be stored is to be kept within practical limits.

For formant synthesis, a complex analysis algorithm is needed to generate speech parameters from the original speech. The pitch-detection part of the algorithm involves a search for periodicity in the speech, either in the frequency or the time domain. Both methods are sensitive to noise, which can cause octave errors or completely incorrect results. Once generated, all the parameters that control the filter are coded and stored in memory. To recreate speech, the appropriate codes are retrieved from memory, then sent to an electronic model of the vocal tract (inverse analyzing filter). A word can be pronounced by the synthesizer in a variety of ways by altering the vocal tract model.

Vocal-tract modelling offers excellent quality sound with low data rates. It does, however, require comprehensive analysis and editing of the speech to be recorded in order to improve the intelligibility of the synthesized speech and to minimize the data rate without loss of speech quality.



(C)

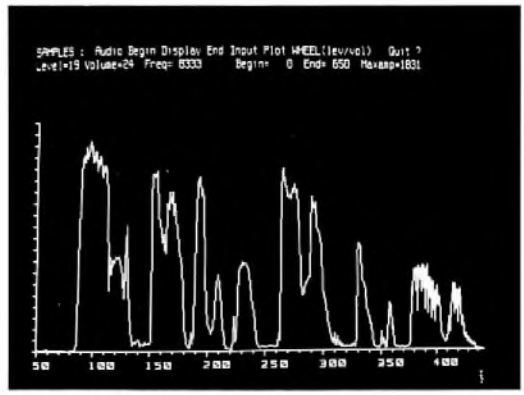


Fig.4 Word picture generated from an HP 9816S equipped with our speech system. Analysis takes about 50 seconds for each second of speech. Pauses are not analyzed, so complete phrases can be investigated at about 40 seconds per second of speech

CONVERTING SAMPLES TO PARAMETERS

In the Analysis mode, speech samples are converted to speech parameters that can be used by the synthesizer. First, the amplitude of the sounds is determined. Then the voiced and unvoiced parts of speech are identified and the pitch of the voiced sounds is extracted together with the four formants and their bandwidth (see panel "Human speech production mechanism"). Each parameter is rounded to the nearest one that can be produced by the synthesizer. Using quantized speech parameters that can be coded reduces significantly the amount of data needed to recreate speech. In general, one second of speech is analyzed in about 50 seconds using the HP-based system.

After analysis, the quantized speech parameters are stored in the input-parameter memory and are ready for editing using the Parameter Edit mode. In this mode, a copy of the parameters is loaded into the edit memory. Parameters are displayed graphically on a visual display unit (Fig.5), so that the user can easily identify any errors from analysis.

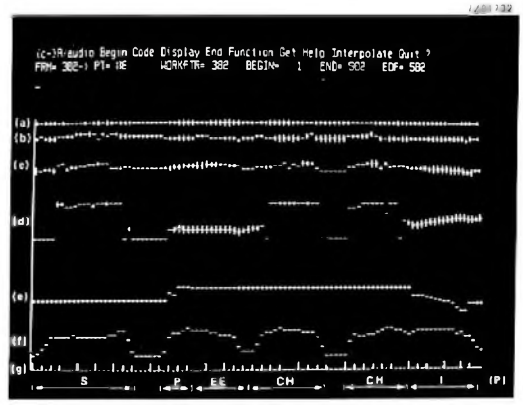


Fig.5 In the parameter edit mode, the speech pattern can be modified for a closer match with the source parameters, a graphic display of the speech parameters making it easy to make modifications. Pitch, contour, amplitude and rhythm are adjustable; word sounds can be isolated, separated or moved closer together. In the figure, the parameters for the words 'speech chip' are shown: (a)-(d) represent the formant frequencies and bandwidths; (e) the pitch and voiced/unvoiced source selection; (f) amplitude; (g) speech frame duration

The speech can also be improved by altering the pitch contour, amplitude, and rhythm. Words and sounds can be isolated or connected. The amount of data to be stored can be reduced by increasing the length of speech segments when the speech parameters are constant or changing at a constant rate. Samples, input parameters and edit parameters are stored in the personal computer's RAM. Therefore, editing mistakes can be corrected readily because the unedited speech is always available. The audio commands are a feature of the parameter-edit mode. They enable the user, at any stage of editing, to hear and compare the speech represented by the contents of the input and edit memories with the original sampled speech stored in the memory array.

COMPRESSED SPEECH CODE

Compressed speech code is generated from the data in the parameter-edit memory using the Code mode. The speech codes are stored in a memory array with an address map at its head to indicate the number and size of the different utterances. The order of the utterances in the code map can be optimized for the application. Utterances can be deleted if no longer required, and can be made audible even at this stage. Speech parameters or codes can be stored on floppy disks at any time during editing.

The system can program four industry-standard EPROMs with automatic verification of the EPROM contents against the code map (EPROM mode). About 50 seconds of coded speech can be stored on each 64K EPROM. Programs for making backup disks, initializing disks (Media mode), and for modifying system parameters such as the audio sampling rate (Option mode) are available.

CHOICE OF PC

Besides their wide availability, the HP9816S and IBM Personal Computer were chosen for their:

- single-user single-tasking facility for stand-alone operation
- IEEE-488/IEC 625 bus interface for communication with the SAB.
- 512-Kbyte machine RAM memory for storing the analysis and editing programs, sampled speech data, and the input and edit parameters representing, at any one time, up to 9 seconds of speech
- high-resolution display for the graphics
- acceptable price
- worldwide service facilities.

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Quality – high-speed CMOS

G. SCHONK

Our range of HC/HCT/HCU high-speed CMOS (HCMOS) ICs includes devices which are pin-compatible with many LSTTL and HE4000B CMOS circuits. The HC series are high-speed alternatives to the 4000B series; the HCT series are low-power replacement for LSTTL. Both are produced using our proven Isolated Oxide technology, but with tighter layout rules than for the HE4000B series (3 μm gate structures with thinner gate oxide). Propagation delays are of the order of 10 ns.

Our HCMOS ICs combine the latch-up immunity of our HE4000B CMOS and the high quality achieved by a zero-defect-oriented organization. All are protected against electrostatic discharge damage.

On the way to our goal of zero defects we expect to achieve a process average reject level of 100 ppm for HCMOS during 1985. Life-test results indicate a failure rate at 50 °C of less than 5 FITS (5×10^{-9}/h).

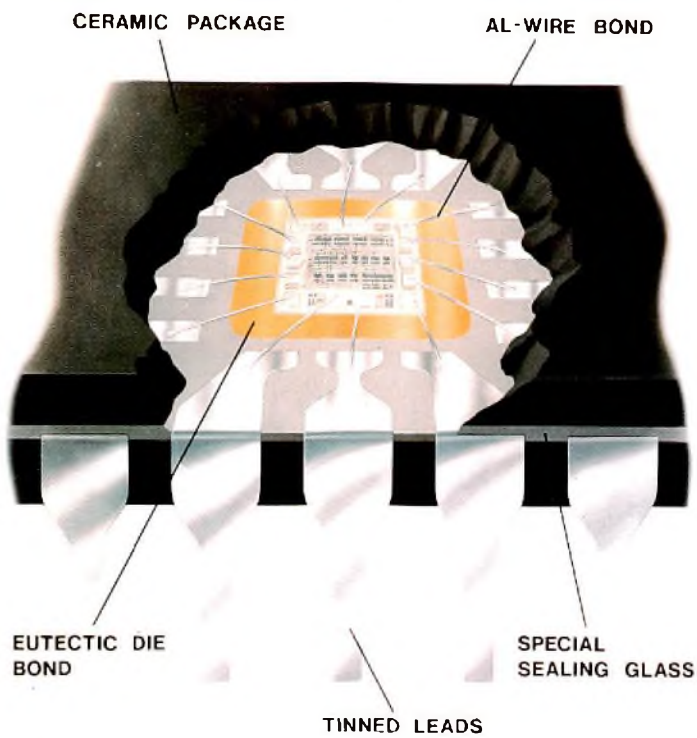


Fig. 1 High-speed CMOS circuit, showing the principal quality-determining features

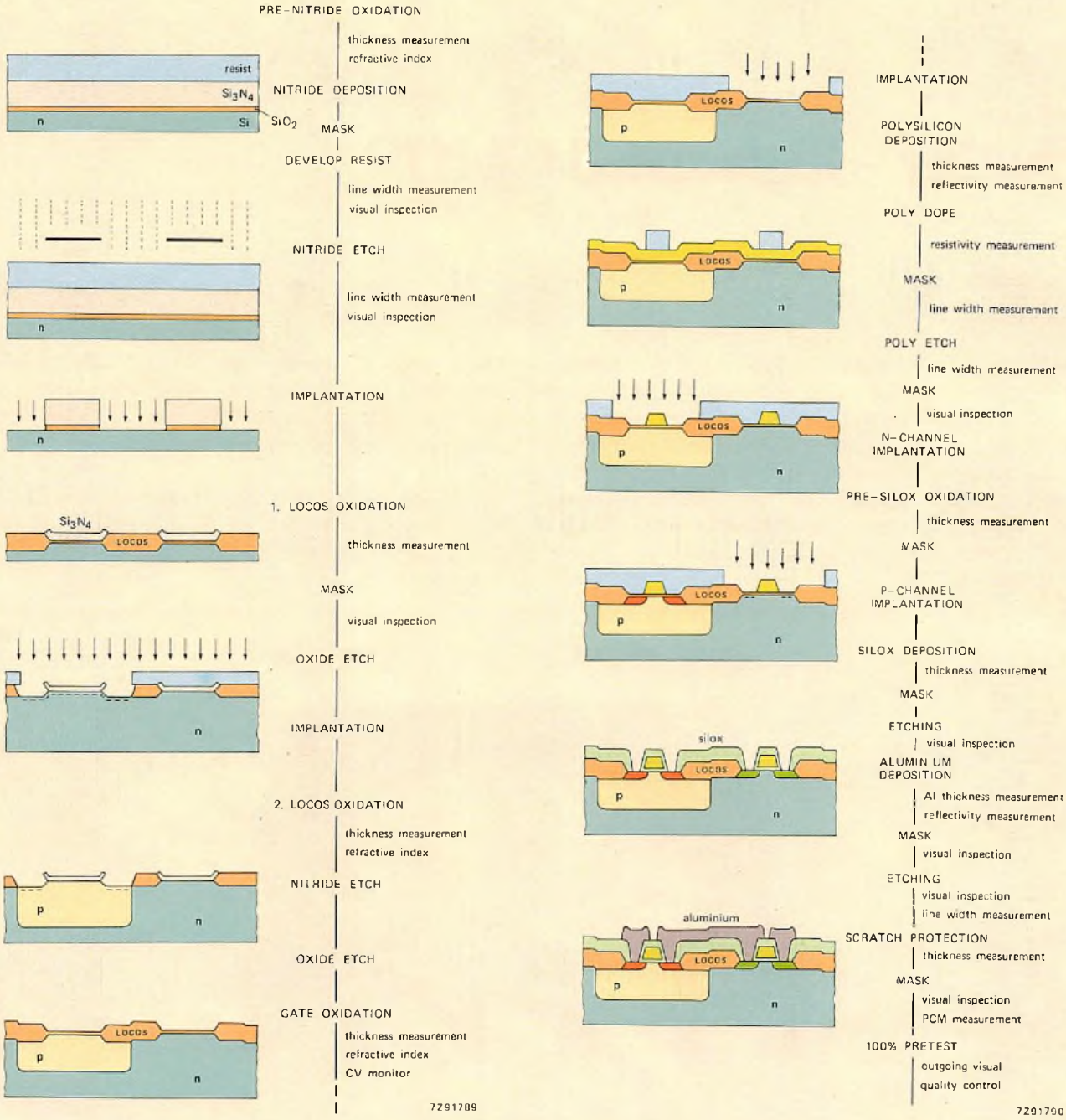


Fig.2 Wafer fabrication flow chart for our HCMOS ICs

QUALITY ASSURANCE

Our Quality Department is fully involved in all stages of the production cycle of our HCMOS ICs:

- design and development
- wafer fabrication
- assembly
- inspection and testing
- batch release
- customer liaison.

This results in a continuous feedback of data which enables us to refine production conditions, test methods and designs to yield optimum quality in the final application.

Design and development

Layout rules and design parameters for our HCMOS series ICs are specified in our Design Manual which reflects more than ten years' experience in CMOS silicon-gate production.

During the CAD generation of new circuit designs, layouts are automatically checked against the rules laid down in the Design Manual. Each layout is further checked by the Quality Department against not only the Design-Manual requirements, but also the capabilities of the assembly process and product specifications.

Wafer fabrication

To realize the full performance potential of our HCMOS technology we have developed a new organizational structure for the wafer fabrication process. Production flow is now divided between technology-oriented Control Groups that are responsible for

- process control
- equipment engineering
- calibration
- contamination control
- training.

Activities of these Groups are coordinated by Process Engineering and supported by extensive data-processing facilities.

Figure 2 shows the flow of wafers through the various fabrication stages and the associated process controls. Overall wafer fabrication activity, Fig.3, is monitored by frequent audits by the Quality Department.

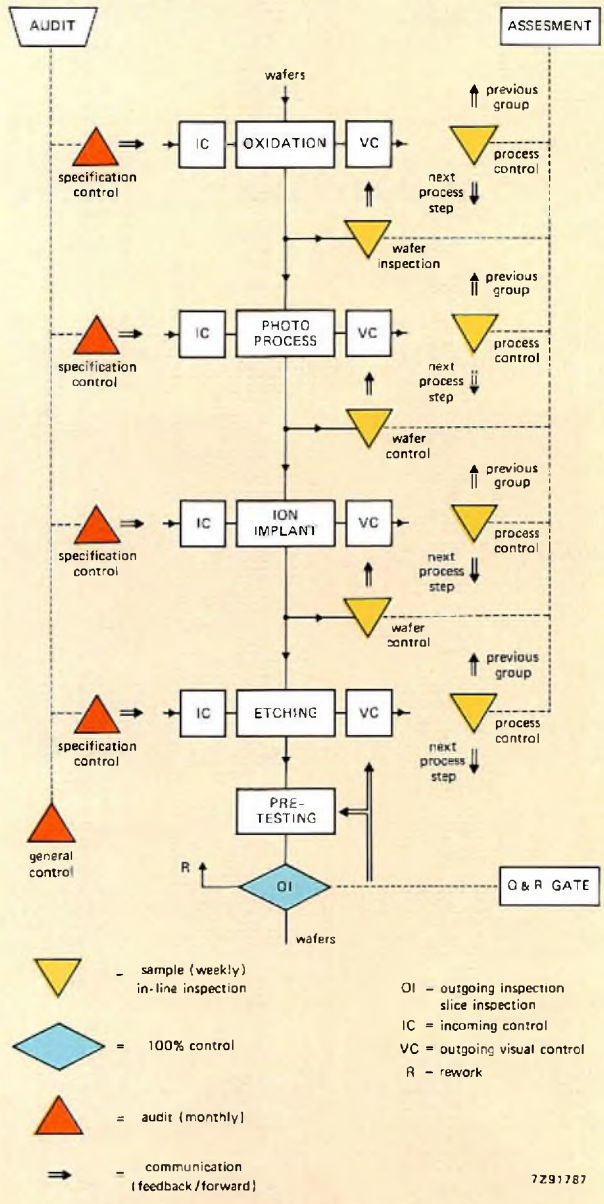


Fig.3 Quality control during wafer fabrication is the responsibility of Control Groups centred around specific process areas. Control Group activities are monitored by frequent Quality Department audits

Assembly

Quality control is fully integrated with the assembly process, as shown in Fig.4.

Dice are assembled into packages on highly automated assembly lines. Fully automatic die attach and wire bonding ensure a high and consistent assembly quality. Tube to tube handling after moulding (or sealing, for cavity devices) ensures excellent mechanical and visual quality.

Quality College in session: a cornerstone of our quality-improvement programme

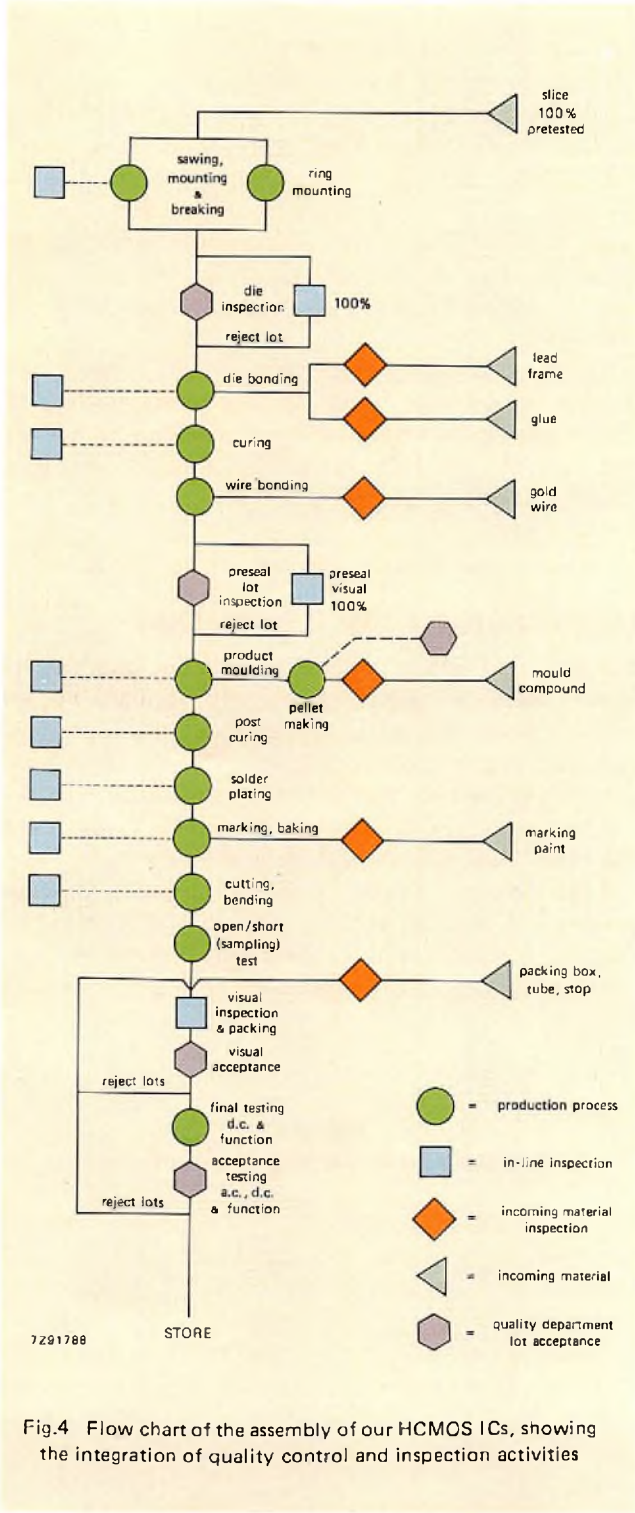


Fig.4 Flow chart of the assembly of our HCMOS ICs, showing the integration of quality control and inspection activities

Quality improvement programme

To develop quality awareness in all areas of our Integrated Circuit Group, we have instituted a 14-step Quality Improvement Program. This program, with its regular Quality College courses, is designed to improve all aspects of our IC business by:

- Monitoring the quality of
  - R&D
  - wafer fabrication
  - assembly
  - marketing and sales
  - support services
  - stores and shipping.
- Extending responsibility for error-cause removal to everyone in the operation
- Exposing everyone to performance indicators
- Improving response to customers' problems and improving resultant cause tracing
- Continuous analysis of product performance to enable continual specification improvement
- Regular quality audits and analysis.

We are totally committed to quality improvement and invite our customers to share in achieving it.

NEW PRODUCT RELEASE

The Quality Department is involved not only in the design and development phases of new products, but also in the qualification and approval of new diffusion processes, packages and assembly methods. Improvements or changes in either product or process must be fully specified, qualified and approved before entering production. As example, Table 1 lists the qualification tests for a new wafer fabrication process.

TABLE 1
Wafer fabrication process qualification tests

test	conditions	duration
electrical endurance	150 °C, 6 V	2000 h
electrical endurance	175 °C, 6 V	2000 h
temperature, humidity bias	85 °C, 85% RH 6 V	2000 h
autoclave	132 °C, 85% RH, 6 V	150 h
temperature cycling	−65 °C to 150 °C	1000 cycles
storage – low	−65 °C	1000 h
storage – high	+150 °C	1000 h
electrostatic discharge	1.5 kΩ, 100 pF, >2 kV	–

ACCEPTANCE AND PERIODIC TESTING

Following the 100% final electrical test, each lot of our HCMOS ICs is sampled by the Quality Department for Acceptance testing. In Group A, a full inspection over the rated temperature range is performed on each device to the following AQLs:

	AQL (combined) (%)	inspection level
functional + electrical parameters	0.1	II
visual + mechanical	0.1	II

Electrical parameters include all those quoted in the device Data Sheet; visual and mechanical inspection includes marking legibility, straightness of leads, plating and cosmetic defects.

A further sample is drawn weekly from each structurally-similar group of ICs and subjected to Group B testing:

- dimensions
- solderability
- temperature cycling (10 cycles)
- electrical endurance (168 h at 125 °C).

To explore quality in greater depth, each structurally-similar group is further sampled quarterly and subjected to Group C Tests (see Table 8). Some THB tests and endurance tests of longer than 1000 h are also performed to examine long term effects.

Every reject found, whether in-house or by customer return, is subjected to an in-depth failure analysis using the most comprehensive and up-to-date equipment. The results obtained provide valuable data that can be used for continual product improvement.

LATCH-UP PREVENTION

Conventional CMOS circuits are inherently latch-up prone. Latch-up is the thyristor action in four-layer p-n-p-n structures formed from parasitic p-n-p and n-p-n transistors; it is usually destructive.

When no circuit junction is forward biased, there is no minority-carrier injection and no parasitic transistor is activated. In practice, forward biasing leading to latch-up is due to voltages at the input or output terminals above positive supply voltage V_{DD} or below negative supply voltage V_{SS}. Although these voltages are clamped by junctions at the terminals, over-voltage spikes on the supply lines can result in forward biasing through avalanche breakdown. Fast-switching and supply-line spikes can enter through junction capacitances to cause forward biasing at circuit nodes.

Thanks to geometry precautions and the epitaxial substrate in our HCMOS process, the d.c. current required to initiate latch-up at either an input or output terminal is over 100 mA; our HCMOS can therefore be considered virtually latch-up proof.

ELECTROSTATIC DISCHARGE (ESD)

The improved CMOS technology used for our HCMOS families allows polysilicon resistors to be used at all inputs to slow down fast input transients due to electrostatic discharges and dissipate some of their energy. Despite the improved protection provided by these resistors, and the use of two stages of diode clamping, Fig.5, the usual CMOS handling precautions should still be observed.

ESD resistance of our HCMOS is measured for both positive and negative discharge from a 100 pF capacitor through a 1,5 kΩ resistor. Pulse rise time is 13 ± 2 ns. Results obtained from Acceptance testing are given in Table 2.

TABLE 2
ESD resistance of our HCMOS (cumulative results)

	polarity	1% fail	50% fail
inputs	positive	2050 V	2700 V
	negative	2300 V	> 3000 V
outputs		> 3000 V	> 3000 V
supply		> 3000 V	> 3000 V

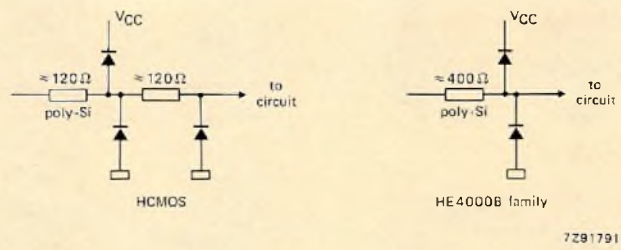


Fig.5 Input networks used to protect our HCMOS and HE4000B ICs from electrostatic discharge damage.

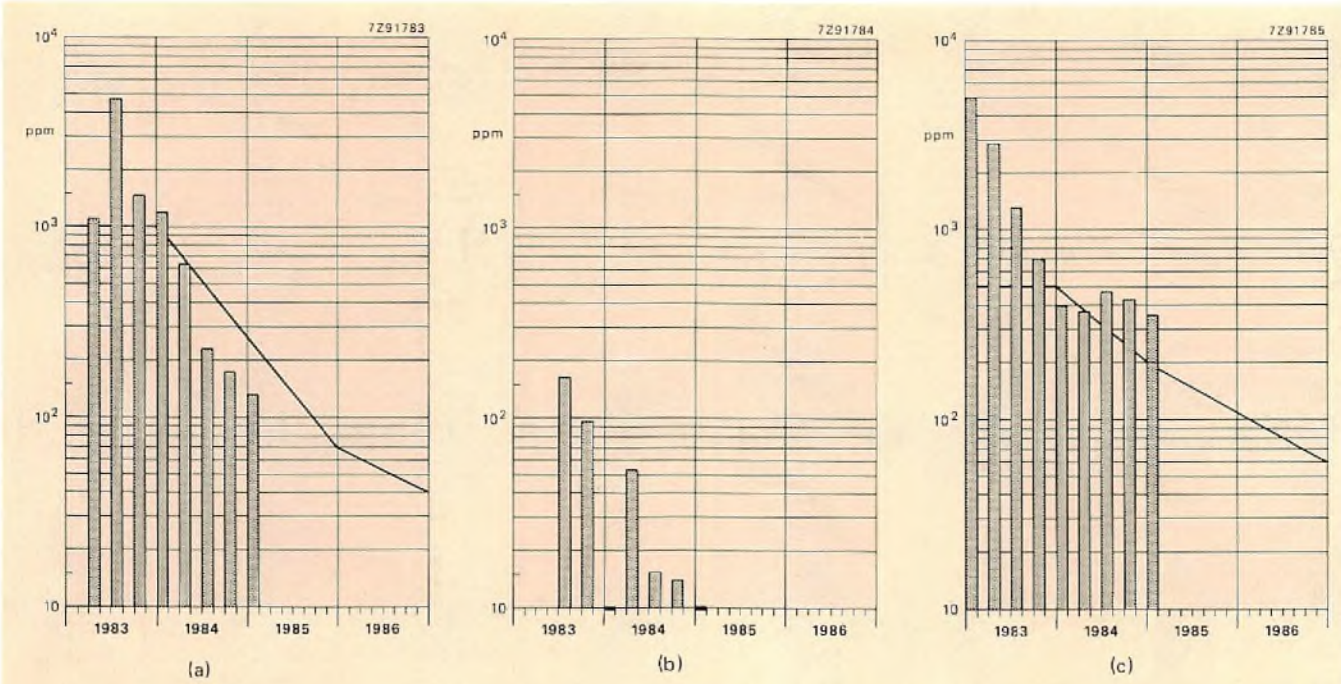


Fig.6 Process average reject levels (in ppm) for (a) electrical parameters and functions combined; (b) function only; (c) mechanical and visual defects. Target quality levels are also indicated

OUTGOING QUALITY

The results from Quality Department Acceptance testing provide a good indication of the outgoing quality of our HCMOS. Figure 6 shows, in terms of 'electrical parameters and function' and 'mechanical and visual', the reject levels recorded in ppm (parts per million) for 1983, 1984 and the first quarter of 1985, together with the projected levels for 1985 and 1986.

ENDURANCE AND ENVIRONMENTAL TEST RESULTS

Temperature-humidity-bias

THB testing measures the moisture resistance of plastic DIL and SO packages. It is performed at 85 °C and 85% relative humidity with an applied bias of 6 V. Electrical measurements (against the Device Specification) are made after 168 h, 500 h, 1000 h, and every 1000 h thereafter. Functional failures are subjected to failure analysis.

Results from tests done from 1983 to May 1985, Table 3, show the excellent moisture resistance of our packages, even after extended test durations.

If confidence bands are taken into account, results of THB testing confirm that no significant difference between DIL and SO packages can be observed.

Autoclave with bias

This is essentially an accelerated THB test with an acceleration factor of 30. This means that 120 hours' autoclave is comparable with 3600 hours' THB. We have extended the conventional autoclave test to include 6 V bias at a temperature of 132 °C in unsaturated steam at a relative humidity of 85% and a pressure of 250 kPa (2,5 atmospheres). The results given in Table 4 attest to the excellence of the silicon-nitride/PSG protection layer and the workmanship of the package.

TABLE 3
Temperature-humidity-bias (85 °C/85% RH/6 V)

DIL package

test time (h)	sample N	failures (cum) param.	failures (cum) function	cumulative % failure
1000	818	3	3	0.73
2000	698	3	6	1.29
3000	420	5	8	3.10
4000	360	6	5	3.06
6000	120	3	3	5.00

SO package

test time (h)	sample N	failures (cum) param.	failures (cum) function	cumulative % failure
1000	140	0	0	0
2000	100	0	0	0
3000	40	0	0	0

Failure analysis of rejects:
Parameter: I_{DD} leakage
Function: mostly corrosion, some I_{DD} leakage.

TABLE 4
Autoclave with bias (132 °C/85% RH/6 V)

DIL package

test time (h)	sample	failures (cum) P	failures (cum) F	cumulative % failure
120	700	6	3	1.29
180	530	1	6	1.32
240	530	5	13	3.40
300	530	3	23	4.91
360	480	3	31	7.08

SO package

test time (h)	sample	failures (cum) P	failures (cum) F	cumulative % failure
120	355	5	3	2.25
180	210	0	3	1.43
240	150	0	2	1.33
300	150	0	2	1.33
360	60	0	0	0

Failure analysis of rejects:
Parameter: I_{DD} leakage
Function: mostly corrosion, some I_{DD} leakage.

Accelerated life testing

To obtain data for failure rate predictions quickly, some life tests are done at elevated temperatures. Devices are biased at their nominal operating voltage of 6 V; ambient temperatures are up to 150 °C for plastic packages and up to 225 °C for ceramic. Devices are tested for function and electrical parameters before the test starts, and then after 48 h, 168 h, 1000 h, and then every 1000 h. Every failure found is analysed. The results from such testing of more than 35 types of HC and HCT ICs in ceramic, plastic DIL and SO packages are summarized in Tables 5 and 6. No significant difference between the results obtained from different packages has been detected.

In Table 6 the results given in Table 5 are derated to 50 °C operating temperature, using an activation energy E_A of 0,7 eV. Figure 7 gives the derated failure rates for various activation energies.

Temperature cycling

Cycling between −65 °C and +150 °C generates stresses that test the structural integrity of dice and packages. We perform this test according to the requirements of MIL-STD-883C, Method 1010, Condition C. Samples are checked before and after the test for function and electrical parameters against the published values. No failures have been observed in 2400 cycles, as reported in Table 7.

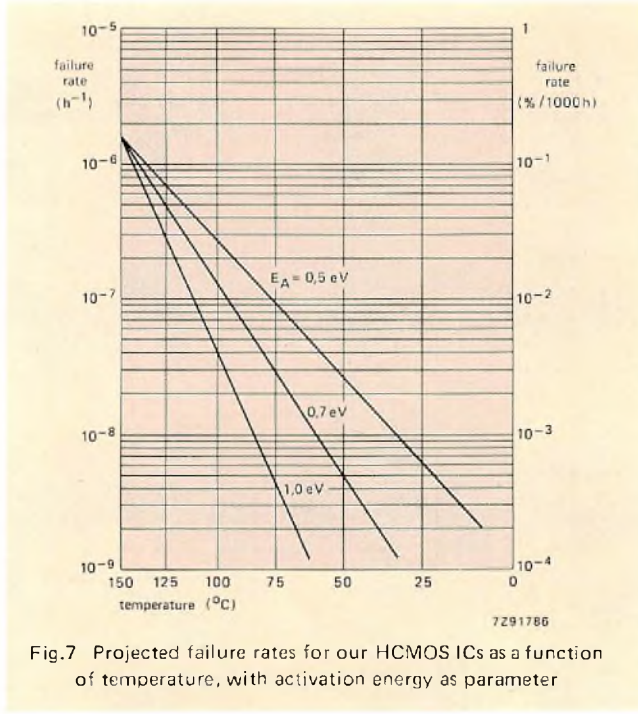


Fig.7 Projected failure rates for our HCMOS ICs as a function of temperature, with activation energy as parameter

TABLE 5
Life test results: HCMOS, 1983/May '85 (cumulative)

T (°C)	test duration (h) 1000	2000	4000	8000
	(failures/sample)			
150	8/2460[1])	8/1049[2])	2/468[3])	2/160[4])
175	2/320[5])	3/320[6])	3/80[7])	
225	0/48			

Failure analysis; (F) = function, (P) = parameter.
[1]) 6 × I_{DD} (P); 1 × I_{DD} (F); 1 × hole in gate oxide (P)
[2]) 5 × I_{DD} (P); 2 × I_{DD} (F); 1 × hole in gate oxide (P)
[3]) 1 × hole in gate oxide (F); 1 × I_{DD} (F)
[4]) 1 × I_{DD} (P); 1 × I_{DD} (F)
[5]) 1 × I_{DD} (F); 1 × V_T shift
[6]) 1 × I_{DD} (P); 1 × I_{DD} (F); 1 × V_T shift
[7]) 1 × I_{DD} (P); 2 × I_{DD} (F).

TABLE 6
Failure rates (from test data of Table 5)

test temp. T °C	device hours (10^6)	50 °C device hours (10^6)	failures
150	5.085	1942.9	8
175	0.800	892.6	3
225	0.048	330.7	0
	Totals:	3166.2	11

derived failure rate for E_A = 0,7 eV: λ = 3,5 FITS (3,5 × 10^{-9}/h)
at 60% confidence λ = 4,7 FITS (4,7 × 10^{-9}/h).

TABLE 7
Temperature cycling: −65 °C to +150 °C in dry air

	DIL		SO	
no. of cycles	sample	failures	sample	failures
200	1161	0	288	0
400	967	0	288	0
800	430	0	288	0
1200	260	0	288	0
1600	195	0	288	0
2400	195	0		

RELIABILITY TEST PROGRAM

Conditions for the endurance tests performed regularly on structurally-similar groups of our MOS products are derived from IEC68 and MIL-STD-883C specifications. These are listed in Table 8, together with results obtained during 1983 and 84.

TABLE 8
Periodical reliability test program: 1983/84 results

sub-group	description	IEC 68	derived from MIL-STD-883B method no.	plastic N	plastic n_F	SO N	SO n_F
C1	dimensions	–	2016	324	0	36	0
C2	marking permanence	–	2015	440	0	72	0
C3	robustness of termination	68-2-21	2004	234	0	108	0
	– tensile	Test Ua	cond. A				
	– bending	Test Ub	cond. B1				
	– lead fatigue	Test Ub	cond. B2				
C4	temperature treatments (sequential)			1739	0	157	0
	– resistance to soldering heat (10s at 300 °C)						
	– thermal shock (10 × 0 °C to 100 °C)	68-2-27 Test Nc	1011 cond. A				
	– temperature cycling (10 × −65 °C to +150 °C)	68-2-14 Test Na	1010 cond. C				
	– storage to 85 °C and 85% RH for 21 days						
C6	THB* 85 °C/85% RH/6V/1000 h	68-2-3 Test Ca	1004	(see Table 3)			
C8	electrical endurance 1000 h at 125 °C		1005	(see Tables 5 and 6)			
C10	temperature cycling						
	200 × −65 °C to +150 °C	68-2-14 Test B	1010 cond. C	1161	0	290	0
C11	storage endurance	68-2-2 Test Ba	1008 cond. C	863	0	105	0
	1000 h at T_a = 150 °C						
C12	storage endurance	68-2-1 Test Ab		625	0	105	0
	1000 h at T_a = −65 °C						
C13	transient energy		3015				
C15	salt mist	68-2-11 Test Ka	1009 cond. A				
	solderability	68-2-20 Test T	2003	960	1	384	0
	autoclave						
	121 °C/100% RH/60 h			548	0	160	0

* Temperature-humidity-bias.

N = sample size.
n_F = number failures.

CECC RELEASE

The CECC (CENELEC Electronic Components Committee) Quality System, which dates from the early 1970s, harmonizes quality standards throughout Europe; fifteen countries now participate. Electronic components released under CECC must have satisfied the inspection requirements of the appropriate CECC Specification. The inspection and the application of the CECC System by suppliers are monitored by independent National Supervising Inspectorates, such as the British Standards Institute in the UK.

The component specification, which describes the component in sufficient detail to enable a customer to select it for a particular application, includes

- electrical values and their tolerances and limits
- behaviour under defined climatic, mechanical and endurance conditions
- acceptance criteria for batches of the component.

To qualify for the CECC Mark or Certificate of Conformity

a component manufacturer must satisfy the National Supervising Inspectorate that:

- his Quality Department runs strictly according to CECC rules, and especially that it is independent of Production Management
- his production departments run according to CECC rules for each component inspected.

Our HE4000B family ICs obtained CECC Approval in 1982 in cerdip packages, and in 1983 in plastic packages. CECC Approval of our HCMOS products is expected to be made official in the second half of 1985.

Datacomm peripherals for the 68000 microprocessor

J. MAGILL and G. THOMSEN

Single-chip data-communication peripherals have become so powerful, they now implement a variety of software-selectable protocols. A large family of such ICs has been designed for interfacing with the 68000 microprocessor (Fig.1). The ICs, which are also suitable for 8-bit systems, provide a compact, cost-effective and flexible set of data communications building blocks. Furthermore, they allow designers to meet protocol requirements easily, because they perform much of the processing needed to interpret protocol rules.

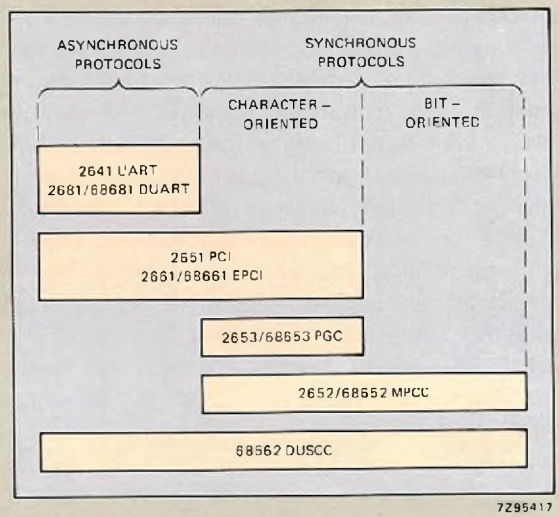


Fig.1 68000 datacomm peripherals for a variety of protocols. Of the peripherals with dual type numbers, e.g. 2681 and 68681, the former is the processor-independent version, the latter a version that can be connected direct to a 68000 microprocessor with a minimum of interface circuitry. The internal control sections of each version are virtually identical

DATACOMM PROTOCOLS

Protocols are the standard procedures and conventions that govern the transfer of data between communicating data-processing machines. The purpose of all data communications protocols is to avoid losing data and to provide data security in the case of unauthorized recipients. Protocols are also called line protocols, line disciplines, line formats and conventions.

Protocols may be classified by the manner in which they allow data to be transmitted. If the protocol coordinates the transmitter and receiver, the protocol is called *synchronous*. If the protocol allows the transmitter to send data at random times without having to notify the receiver of a transmission, the protocol is called *asynchronous*. Asynchronous transmission is usually limited to low data rates while synchronous transmission is normally used above ~1200 bits/s.

Synchronous protocols can be subdivided into character-oriented protocols (COPs) and bit-oriented protocols (BOPs). COPs, dominated by IBM's BISYNC and DEC's DDCMP, use blocks that contain error-checking and error-correcting information as well as data. BOPs, although relatively new, have proliferated fast and are more straightforward than COPs. BOP messages are transmitted in frames and adhere to a common format. Two of the more common BOPs are HDLC (ISO's high-level data-link control) and SDLC (IBM's synchronous data-link control). And while COPs are suitable for asynchronous as well as synchronous communication, BOPs aren't.

While there are many protocols in use, some defined by national and international standards organizations, others defined by digital equipment manufacturers, the characteristics of protocols are by no means standardized. Some asynchronous protocols, for example, have a single bit at the beginning of a character transmission, others have several. Some synchronous protocols have a single synchronization character at the beginning of a message, others have several. Even when manufacturers use the same number of sync characters, the characters may be different.

The 68000-compatible datacomm ICs described in this article can implement all these protocols at minimum cost and with maximum reliability.

THE 68000 DATACOMM PERIPHERALS

68562 Dual serial communications controller (DUSCC)

The 68562 provides two independent multiprotocol full-duplex channels. It supports bit-oriented protocols and character-oriented protocols (both byte count and byte control), synchronous data-link controls as well as asynchronous protocols. The internal logic for both channels provides formats, synchronization and validation for data transferred to and from the channel interface. The 68562 interfaces with the 68000 using bus control signals, and can program polled, interrupt or DMA (direct memory access) data transfers.

2652/68652 Multi-protocol communications controller (MPCC)

The 2652 is dedicated to synchronous protocols both bit-oriented and character-oriented. In addition, it includes extra support for BISYNC operation. Transparency of synchronous communication is enhanced for bit-oriented protocols because the 2652 can recognize and create special characters such as message delimiters (flags), sync characters and other link-control operators.

2653/68653 Polynomial generator checker (PGC)

The 2653/68653 supports character-oriented protocols by creating and checking message-redundancy characters using polynomials for cyclic redundancy (CRC-16 and CRC-12) and linear redundancy (LRC-8). Depending on the protocol used, not all characters of the message may be subjected to the redundancy check (for example, character-oriented protocols using control characters to bracket data or to maintain synchronization).

2661/68661 Enhanced programmable communications interface (EPCI)

The 2661 is an upgraded version of the 2651 programmable communications interface. It is a universal synchronous/asynchronous data communications controller chip with special support for BISYNC which frees the host system from pre-processing data, ensuring that idiosyncracies of the protocol don't result in data loss. For example, if the microprocessor can't feed data to the EPCI fast enough, the EPCI inserts control characters that serve as controlled datacomm 'Wait' states, so the controller doesn't lose synchronization with the other node, or lose data.

2641 Universal asynchronous receiver/transmitter (UART)

The 2641 is a single-channel version of the asynchronous part of the 2661. It has an on-chip baud-rate generator and diagnostic and operates at 1 MHz.

2681/68681 Dual universal asynchronous receiver/transmitter (DUART)

The 2681 provides two independent full-duplex asynchronous receiver/transmitter channels. Besides two asynchronous data channels, it has independent bit-rate generators, self-testing and interrupt handling. Moreover, it can be used in either polled or interrupt-driven systems. The 2681 is available in 24, 28 or 40-pin versions dependent on the I/O. For interfacing with the 68000, the 40-pin 68681 supplies the asynchronous handshake signals the 68000 requires as well as an interrupt vector to indicate receipt of an interrupt-acknowledge signal.

DESIGN EXAMPLES

The interface circuits described support most standard datacomm protocols. However, they can't handle the more complex protocols such as those used in networking schemes. To help you select the best interface for your system, several design examples are presented (Figs.2 to 6).

Software

All the interface circuits shown operate on the same basic principles, and require similar software routines. Before initiating data communication, you must instruct the controller to program the peripheral's operational mode by performing write operations to the mode and command registers. You can reconfigure the peripherals any time during program execution, but disable the transmitter and receiver pair before loading the new command and mode information. This reduces the possibility of truncating a character during transmission or losing it during reception.

After initialization, software can control the transfer of information by either polling or interrupt subroutines. In both cases, the software must determine the request for transmission or reception. The routines should also check for any errors that might have occurred and resolve them. In addition, the routine must reset the condition that indicated the request. Usually, it does so by reading or writing data to the appropriate buffers on the communication IC.

HARDWARE

Asynchronous interface, 8-bit designs

Figure 2 shows an asynchronous interface circuit which performs simple datacomm tasks such as connecting dissimilar communication devices like printers and modems.

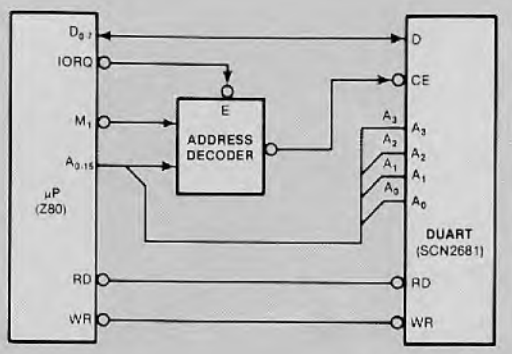


Fig. 2 Asynchronous interfacing can be simple – especially for 8-bit designs. Here, a Z80/SCN2681 dual universal asynchronous receiver/transmitter (DUART) interface requires only one address decoder

It uses a 2681/68681 DUART which interfaces with either an 8-bit or 16-bit system with a minimum of interconnection circuitry. The I/O-mapped Z80 interface shown requires only an address decoder. The processor's M_1 signal inhibits the chip enable (CE) signal during interrupt-acknowledge cycles. A Wait state ensures that the data lines settle before the peripheral reads the data.

An even simpler interface using the 2641 UART, and which also requires only a decoder, reduces the number of connections to eight data lines, the CE signal, and three address lines for device selection and read/write control.

Asynchronous interface with DMA, 16-bit designs

In the asynchronous interface of Fig.3, the DUART takes advantage of the DMA capability provided by the 68430 DMA interface (DMAI). As a peripheral or system master, the DMAI provides all the necessary signals to interface with the 68000. The control signals drive the bus directly, while five other ICs demultiplex the address/data bus from the DMAI. During a register read/write cycle, U_4 and U_5 function as bidirectional data buffers and U_1 serves as an input buffer for the register address. U_1 to U_3 are active during the DMA operation and drive the memory address onto the bus.

The rest of the circuitry connects the DUART as a peripheral to the 68000 or as a DMAI. The address lines to the DUART are from multiplexer U_6, and the DMAI selects U_6's output with its $\overline{OWN}$ signal ($\overline{OWN}$ is an output-control signal asserted during DMA transfers). The controller therefore selects one of two sets of multiplexer inputs – the address bus and $\overline{UDS}$ (upper data strobe) or a hard-wired address.

Because it has two channels, the DUART is normally addressed at even or odd memory locations. To address contiguous memory locations, however, AND the DUART select with $\overline{LDS}$ or $\overline{UDS}$ (U_8 and U_9) to generate the DUART $\overline{CS}$ signal, and then use $\overline{UDS}$ for the DUART least significant address. The hard-wired address, selected during DMA operations, addresses the transmitter/receiver registers. The most significant bit of this address comes from flip-flop U_7, which determines the channel that is accessed. The flip-flop is set during initialization.

To control the data path to the DUART during system and direct memory access, multiplexer U_{10} gates the DUART's $\overline{CS}$ and R/$\overline{W}$ signals. The ANDed signals from U_8 and U_9 also enable the proper transceiver buffer for the data to or from the DUART through multiplexer U_{10}. During DMAI operation, R/$\overline{W}$ of the DUART is inverted because a memory-read is a memory-write to the DUART.

During host access, the system requires a $\overline{DTACK}$ (data transfer acknowledge) signal at the proper time. For this purpose, U_8 and U_{13} gate the DUART's $\overline{DTACK}$ signal onto the system bus during host access. Finally, the interrupt request $\overline{INTR}$ asks for a DMA operation by being routed to the DMAI's $\overline{REQ}$ input. When a DMA transfer is in progress, the $\overline{DTACK}$ from the DUART serves as $\overline{RDY}$ for the DMAI.

Synchronous interface, BISYNC mode, 8-bit design

The BISYNC protocol can be implemented in both 8-bit and 16-bit synchronous designs using the 2661/68661 EPCI and the 2653/68653 PGC. In BISYNC mode, these two circuits minimize software requirements by providing control-character and character-sequence comparisons, and automatic DLE (data link escape) character insertion and detection.

You can easily interface these circuits with the 68000 (Fig.4). The EPCI and PGC connect in parallel to the 68000 data bus's lower eight bits. The processor's A_1 and A_2 lines connect to the same lines on the two circuits, which are addressed on a word boundary with the data in the lower byte of the data word.

Standard address decoding provides the chip enable for the EPCI (CE) and the PGC (CE_1). The signals are delayed to allow for address and read/write set-up times. The $\overline{DTACK}$ signal is delayed an additional clock period to extend the chip enable to the required period for the two circuits. When $\overline{DTACK}$ is asserted, the 68000 completes the cycle.

Because the EPCI and PGC require an idle between successive accesses, a 74LS163 counter generates a HOLD signal used to delay the second read or write request. This circuit provides the proper idle time if the 68000 attempts a second access, for example, in a MOVEP instruction. The circuit is configured for a 10 MHz system, but it can be modified for 8 MHz and 12,5 MHz clocks simply by changing the counter's preload count.

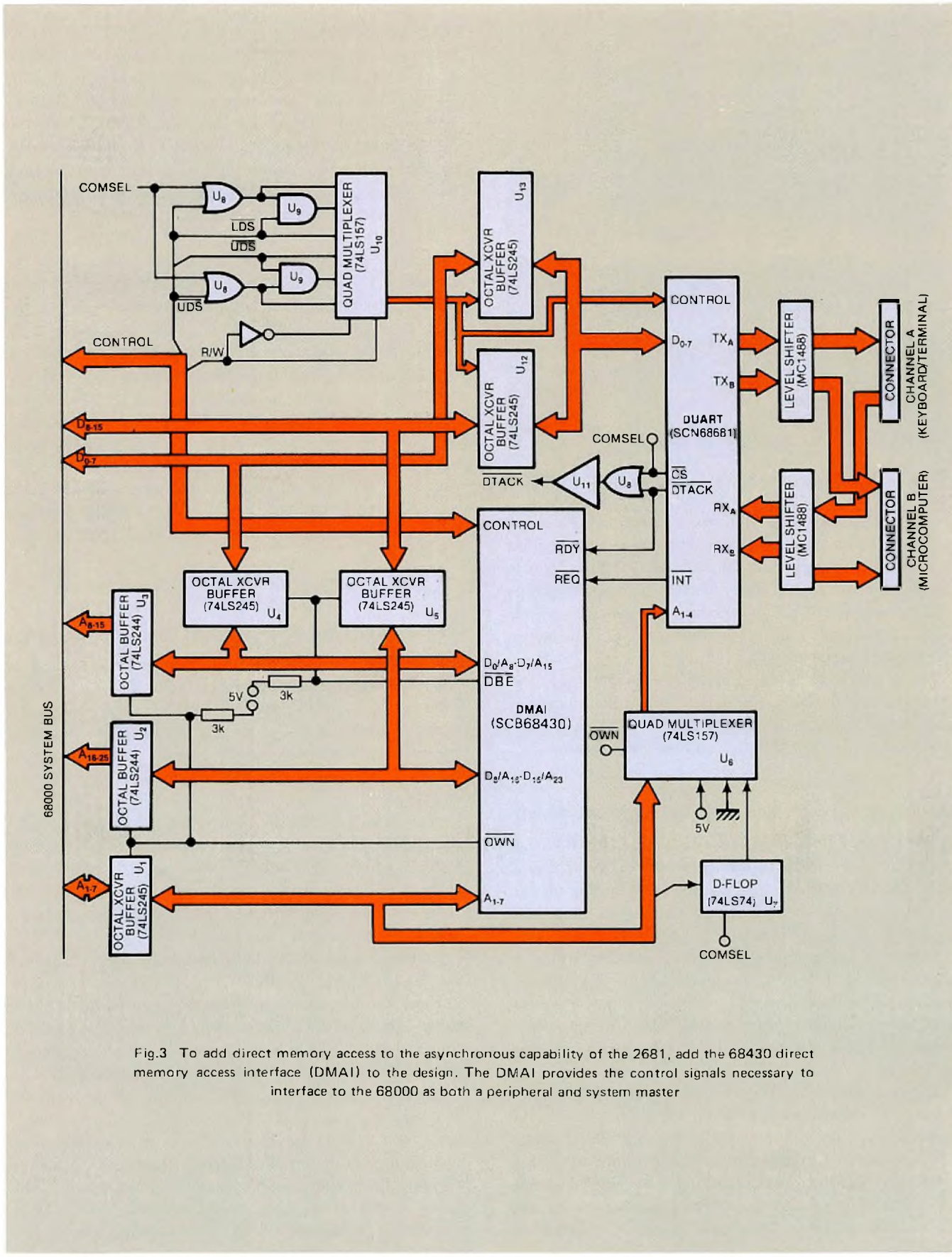


Fig.3 To add direct memory access to the asynchronous capability of the 2681, add the 68430 direct memory access interface (DMAI) to the design. The DMAI provides the control signals necessary to interface to the 68000 as both a peripheral and system master

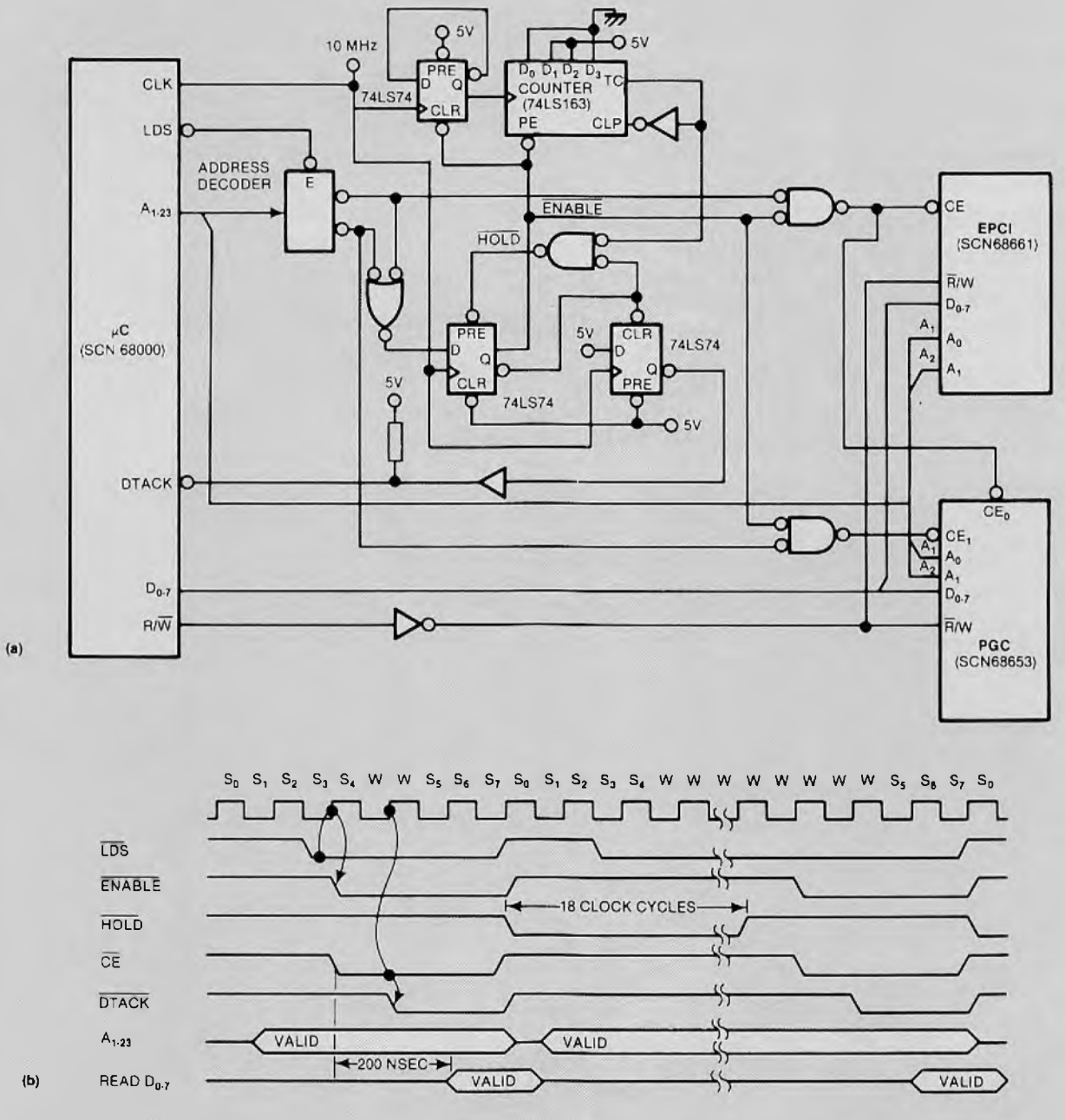


Fig.4 Combine the 68661 EPCI and the 68653 PGC to release the host system from the task of monitoring the data transfer in Bisync transmissions. The EPCI handles most of the protocol interfacing; the PGC ensures data is transmitted and received correctly

Asynchronous interface, BISYNC mode, 8-bit design

BISYNC implementations using the 2661 EPCI and 2653 PGC in 8-bit systems are even simpler, see Fig.5. In the 16-bit implementation, the EPCI and PGC are connected to the lower half of the data bus (Fig.4), so there's no problem with an 8-bit bus. In the I/O-mapped interface shown, the processor's M_1 signal inhibits the chip enable signals during interrupt-acknowledge cycles.

Synchronous interface, DDCMP mode, 16-bit design

For the DDCMP mode, instead of BISYNC, the 2652/68652 MPCC (which also supports other high-level protocols including SDLC and HDLC BOPs) is available. This circuit interfaces with 8-bit or 16-bit processors. Figure 6(a) shows a 16-bit interface, the more common application for this circuit.

The 16-bit word transfer is selected when the 68000 asserts both $\overline{LDS}$ and $\overline{UDS}$ LOW, setting the MPCC's byte input LOW. If either $\overline{LDS}$ or $\overline{UDS}$ isn't asserted, the byte input remains HIGH, thereby selecting the byte-transfer mode for 8-bit operation. The $\overline{LDS}$ signal, which the 68000 toggles, also remains tied to the A_0 input to select either the upper or lower byte for data transfers ($\overline{LDC}$ selects the upper byte).

Standard address-decode logic generates the $\overline{ENABLE}$ signal gated with the HOLD signal. HOLD is delayed to allow the $\overline{DBE}$ (data bus enable) signal to have the proper set-up relationship with respect to the address and read/write inputs. $\overline{DTACK}$ is delayed for an additional clock period to force the 68000 to insert Wait states which guarantee the correct $\overline{DBE}$ time to the MPCC, Fig.6(b).

ACKNOWLEDGEMENT

This article is based on an article that appeared in the March 22 issue of EDN, pp. 177-184, copyright 1984, Cahners Publishing Co.; permission to publish is gratefully acknowledged.

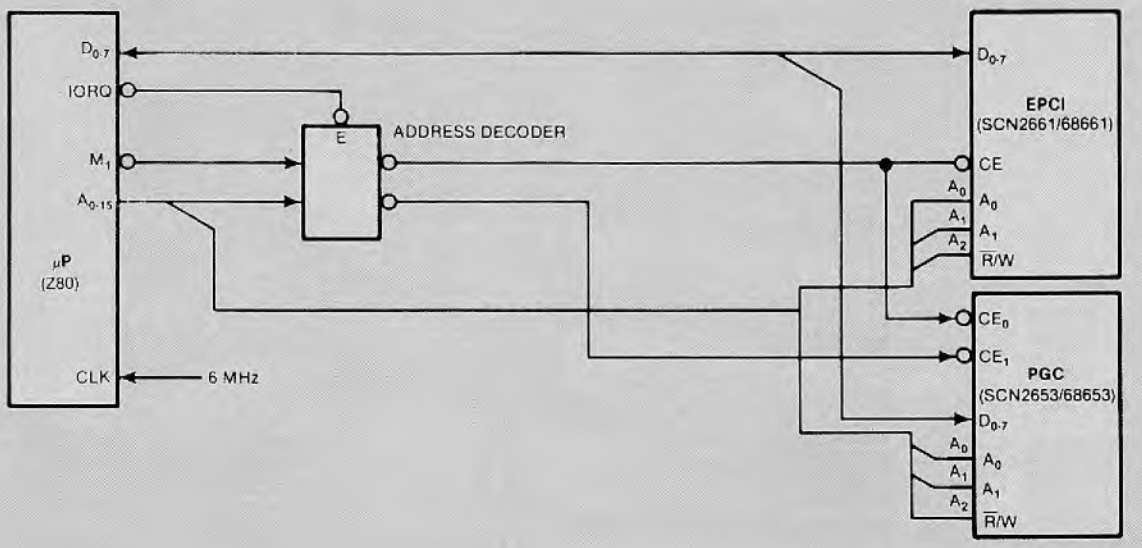


Fig.5 Asynchronous links needn't use many components. This desgin combines the Z80 with a 2661 EPCI and requires only an address decoder in addition to the Polynomial Generator Checker

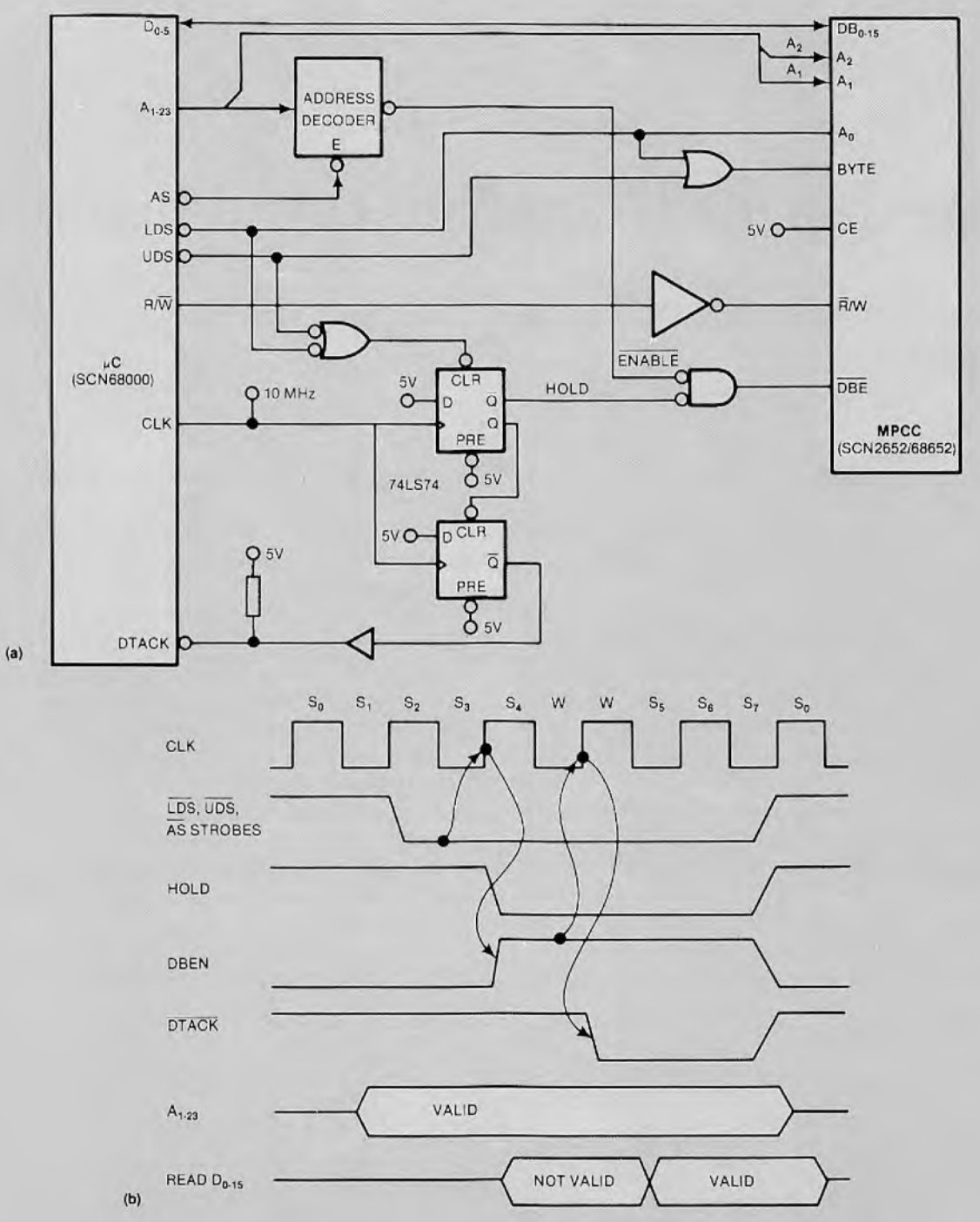


Fig.6 With the 2652/68652, you can implement several high-level protocols including SDLC, HDLC and DDCMP. For a 68000-based system, pay special attention to address-decoding and chip-enable functions

Single-chip multi-standard colour decoder

ANDRIES SMAAL

In areas where tv transmissions to more than one colour standard can be received, colour receivers are required which can handle multistandard transmissions without additional manual switching. This requirement will greatly increase with the introduction of satellite tv.

Such receivers have, in the past, incorporated a multistandard colour decoder (MSD) using several integrated circuits to automatically select the standard of the received signal. However, the growing need for these MSDs makes it economically and technically desirable to incorporate all the active parts in one IC and to reduce, as far as possible, the external circuitry.

This publication describes two new single-chip MSDs using bipolar technology, the TDA4555 and TDA4556. The ICs are similar except for the polarity of the colour difference signals at the output. The TDA4555 provides –(R–Y) and –(B–Y) signals; the TDA4556 provides +(R–Y) and +(B–Y) signals. Only the TDA4555 will be described.

Since all the active parts of the MSD are in a single IC, the design and layout of the printed circuit board is considerably simplified and assembly cost is reduced. The greater reliability of "wiring on silicon" increases the overall reliability of the decoder and reduction of external circuitry simplifies assembly.

The ICs are universally applicable and allow the design of a range of tv receivers having a common main chassis. Automatic selection of the required standard has been made more reliable and the maximum time required for identification and switching is a little over half a second.

When reception is difficult because signals are weak, noisy, or badly distorted, the automatic standard recognition (ASR) can be switched off and the standard chosen manually.

Although the ICs are capable of processing multistandard signals, their performance is as high as that for single-standard decoders.

Figure 1 is a block diagram of a typical multistandard colour decoder incorporating the TDA4555.

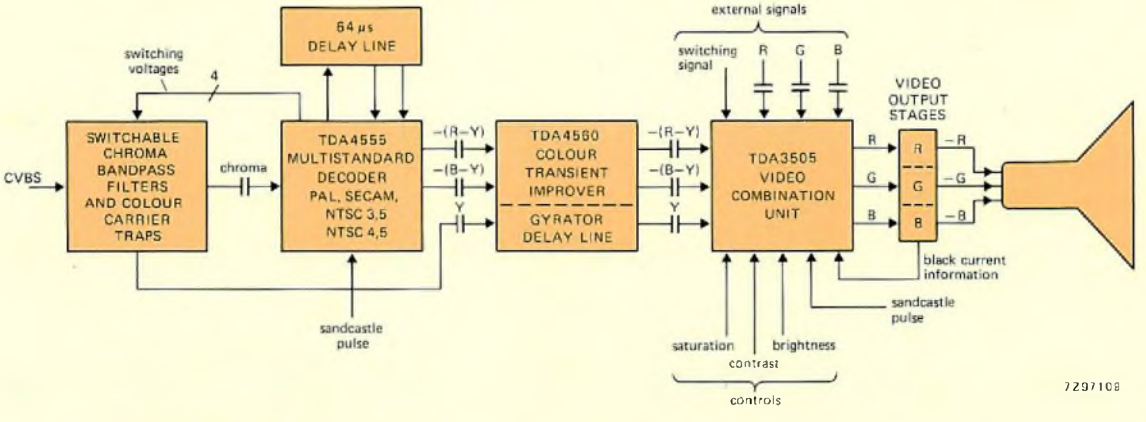


Fig.1 Block diagram of a multistandard decoder incorporating the TDA4555

The composite video input signal (CVBS) is fed via switchable filters to the input of the MSD. The filters separate the chrominance and luminance signals according to the standard selected, which, for ASR, is controlled by the colour decoder IC.

Chrominance signals from the filters are a.c. coupled to the input of the TDA4555, which produces the colour difference outputs, that are, in turn, a.c. coupled to the Colour Transient Improvement (CTI), part of the TDA4560. This IC also contains an adjustable delay-line formed by gyrators, so a conventional wirewound delay line is not needed.

The signals are then fed to the Video Combination IC, TDA3505, which converts the colour difference signals $-(R-Y)$ and $-(B-Y)$ and the luminance signal (Y) into the RGB signals. The TDA3505 also incorporates the saturation, contrast, and brightness control circuits and allows for the insertion of external RGB signals. Finally, the processed video signals are applied, via the RGB output stage to the picture tube.

The new MSD can decode colour tv signals transmitted according to the following standards:

A. QAM (Quadrature Amplitude Modulation of the colour carrier by the colour difference signals).

1. NTSC standards with any colour subcarrier frequency, for example
   - NTSC-M (f_O = 3.579 545 MHz), referred to as NTSC-3.5.
   - Non-standard NTSC systems, for example with

     $f_O = f_{OPAL}$ = 4.433 618 75 MHz.

     This system is used in the United Kingdom and in the Near East and is referred to as NTSC-4.4. As the colour subcarrier frequency is the same as that of the normal PAL system, the same crystal can be used without switching in the reference oscillator for both systems.
2. PAL standard, characterised by phase reversal of the $(R-Y)$ signal on alternate scan lines. The colour subcarrier frequency for normal PAL is 4.433 618 75 MHz.

B. SECAM, characterised by transmission of the colour difference signals $(R-Y)$ and $(B-Y)$ on alternate scan lines and frequency modulation of the colour subcarriers. The frequency of the colour signals may vary between 3.900 MHz and 4.756 MHz. The frequencies of the colour subcarriers are:

f_{OB} = 4.250 MHz for a "blue line"

f_{OR} = 4.406 25 MHz for a "red line".

With these capabilities, the new decoders can handle most of the colour tv transmissions in central Europe and also some in other areas.

DESIGN CONSIDERATIONS

To minimise the number of integrated components and reduce the required crystal area and power dissipation of the MSD, the same sections of the IC are used, where possible, for several standards. For example:

- the gain controlled input stages,
- the common switching pulse generators,
- the PAL and NTSC quadrature demodulators and oscillators,
- the PAL and SECAM delay line,
- the common driver stage preceding the delay lines,
- part of the stage following the delay line and the demodulator.

The number of connections are kept to a minimum compatible with the required functions. With the new ICs, the reference oscillator, its filter, and the SECAM identification circuit, each require only a single pin. The sandcastle pulse is the only external pulse signal required and is also input via a single pin. These, and other measures, allow the TDA4555 chip to be housed in a 28-lead SO117 encapsulation, despite the many functions it performs.

There are three ways an MSD can be formed:

- Separate parallel-connected decoders for each standard with the appropriate output selected by switching. This is the principle used in the three-standard decoder comprising the TDA3510 for PAL, TDA3520 for SECAM, and TDA3570 for NTSC. The colour ON/OFF switch voltages generated in each decoder are used for automatic switching of the standards, and each decoder has to be kept at least partially activated.
- A single PAL decoder can be switched to handle NTSC signals. SECAM signals are converted into quasi-PAL signals by a SECAM-PAL transcoder. The PAL decoder derives the colour-difference signals from this quasi-PAL signal. An example of this approach is the circuit using the single-chip PAL decoder TDA3562A with NTSC option and one of the SECAM circuits, TDA3590, TDA3590A, or TDA3591.
- The two methods described above are not suited to a single-chip MSD because the multiple use of circuit blocks is limited. A much better usage can be obtained if the standards are scanned sequentially. In this approach the decoder circuit, including the filters at the input, is switched to decode each standard in turn. The switching continues until the standard recognition circuit (SRC) indicates that the standard of the received signal corresponds to the standard of decoding selected at that moment. The scanning procedure is restarted if the standard of the input signal changes because of tuning to another transmitter or switching to an external signal source. The same thing applies if the signal temporarily

becomes too weak or disappears. A major advantage of sequential standard switching is that it allows the complete decoder, including the external filters at its input, to be optimized for each standard. This is why the TDA4555/56 are built in this way.

TDA4555 CIRCUIT DESCRIPTION

Figure 2 is the circuit of a multistandard colour decoder using TDA4555/56.

Pulse generation

The IC only requires a single sandcastle pulse at pin 24 for the generation of all internal pulses (e.g. burst key, horizontal and vertical blanking pulses). The sandcastle pulse levels are >8 V for the burst key; 4,5 V for horizontal blanking: and 2,5 V for vertical blanking.

Level detectors in the sandcastle pulse detector separate the three levels which are used to generate the required key pulse and clamp pulses.

Standard control circuit

A special System Control and Standard Scanning circuit (SCSS) provides the switching voltages to set the MSD to the desired standard.

As long as no colour standard is recognized, the SCSS circuit switches the decoder sequentially to the PAL, SECAM, NTSC-3,5 and NTSC-4,4 standards. If the standard of the received signal is not recognised after four field periods (80 ms), the next decoding system is activated. This time interval, also called the standard scanning period, is a good compromise between fast switch-on of the colour and effective interference suppression with noisy signals. The maximum time between the start of scanning and switching on the colour is 360 ms, including the colour switch-on delay of two field periods. However, in the TDA4555, a PAL priority circuit is incorporated to improve the reliability for SECAM, so the scanning can last for another two scanning periods (520 ms maximum).

After recognition of a SECAM signal, the information is stored and the decoding is switched to PAL. A second SECAM recognition is only provided if no PAL recognition occurs. This gives reliable SECAM recognition when the SECAM-PAL transcoding at the source (e.g. in cable systems) is not perfect, or when PAL signals are distorted by reflections so that they simulate SECAM signals.

With b/w signals, the scanning is continuous and the colour is kept switched off because there is no standard recognition.

The switch voltage corresponding to the recognised standard ramps from 2,5 V to 6 V during scanning and the remaining switch voltages are held at 0,5 V maximum. These voltages are used to switch the filters at the input, the crystals of the reference oscillators, and the colour subcarrier traps, and also to indicate the recognised standard (e.g. by LEDs).

To prevent unnecessary restarting of scanning because of momentary disturbances (e.g. short-term interruptions of the colour signal), the TDA4555 incorporates a delay of two field periods (40 ms) before scanning can start.

Finally the IC allows the automatic standard recognition (ASR) to be switched-off by applying external switching signals and forcing one of the decoding modes by applying at least 9 V to pin 28 for PAL; pin 27 for SECAM; pin 26 for NTSC-3,5; and pin 25 for NTSC-4,4. These pins also serve as outputs for the internally generated switch voltages which indicate the selected standard. The automatic colour switch-off is active in both cases.

Colour signal control

The MSD must provide colour-difference output signals with an amplitude referred to a given test signal, despite amplitude variations (within limits) of the colour input signal. This is required to maintain a fixed amplitude relationship between the luminance signal (Y) and the colour-difference signals, independent of different i.f. filters or receiver detuning. The TDA4555/56 incorporate an Automatic Colour Control circuit (ACC) for this purpose.

In the case of PAL and NTSC, the reference for the control is the burst amplitude. For SECAM, the complete colour signal is used. The colour signal is a.c. coupled, via pin 15, to a gain-controlled amplifier and the control voltage is obtained by in-phase synchronous demodulation of the burst or the colour signal.

This approach has the advantage that the same demodulator, having only one external capacitor at pin 16, can be used for all standards and also results in noise reduction with noisy signals. Unwanted increase of saturation with noisy signals (colour bright-up effect) is prevented without an extra peak detector being required.

In-phase synchronous demodulation has the advantage that it is independent of synchronization and the state of the decoder, so the colour gain can settle quickly and the colour standard scanning period is therefore short. Special low-distortion symmetrical circuits were chosen for the gain control stage and the following amplifier stage so that H/2 components in the colour-difference channel are reduced as far as possible during SECAM reception. Biasing of the colour gain control stage is stabilized by a d.c. feedback loop decoupled by an external capacitor at pin 14.

The nominal amplitude of the colour input signal at pin 15 is 100 mV_{pp} for a 75% colour-bar signal. It may vary between 10 mV_{pp} and 200 mV_{pp}. This range is chosen so that, for a normal 1 V_{pp} composite video signal at the input to the filters, transformation is not required.

For PAL and NTSC decoding, the amplitude-controlled colour signal, including its burst, is then fed to the SRC, reference generation, and burst blanking stages. The output of the latter stage is applied to the colour signal demodulators and the delay-line driver stage.

Standard recognition circuit

The SRC tells the SCSS whether the activated decoding mode is the same as that of the incoming signal. This task is performed using the signals occurring during the back porch.

For SECAM, it is necessary to distinguish between line (H)-identification signals of carrier frequency at the back porch and field (V)-identification (special lines carrying identification signals during the field blanking period).

The standard recognition comprises the following parts: a phase discriminator which compares the burst phase of PAL and NTSC signals with the internal reference signal; a frequency discriminator for generating an H/2 signal during SECAM reception; an H/2 demodulator for PAL and SECAM signals; and the logic circuits for the final recognition.

The two phase discriminators for PAL and NTSC signals are supplied with the colour signal, and the amplitude-controlled burst. The phase detector for the PAL signals uses the (R–Y) reference signal for the phase comparison; the NTSC phase detector uses the (B–Y) reference signal. Both reference signals are generated by dividing the reference oscillator output. When the correct signals are received, the phase discriminators output the demodulated burst signal for standard recognition.

The discriminator for generating the H/2 signal comprises an internal phase discriminator and an external phase-shift circuit, known as the SECAM identification reference, connected to pin 22.

The polarity of the PAL and SECAM phase discriminator output signals is reversed line sequentially. With PAL, this is caused by a change of phase of the burst at line frequency. With SECAM, it is the result of the colour subcarrier frequency changing at line frequency.

Since the signal is changing polarity, it is of no use for the following circuitry. Therefore, the discriminator output signals are fed to the H/2 demodulator which line-sequentially reverses the signal polarity. The pulses are then integrated by external capacitors connected to pin 21 (PAL and SECAM discriminator output) and to pin 20 (NTSC phase discriminator output). The voltages on these capacitors are the identification signals which are used by the comparator and logic circuits to derive the control signals. They are dependent on the standard of the incoming signal and on the activated decoding standard and are composed of an internal biasing at half the supply voltage (6 V) and a contribution from the identification signal. In the following explanation only the latter part ΔV_{20} and ΔV_{21} is considered.

(a) When the decoder is set to PAL, the frequency of the reference signal is about 4,43 MHz. The NTSC discriminator is switched off and the voltage at C_{20} is only the bias voltage. The H/2 demodulator is therefore driven by the output of the PAL discriminator. The output of the SECAM discriminator is not used. With a PAL signal at the input, the H/2 demodulator delivers pulses with equal polarity so that capacitor C_{21} is charged to ΔV_{21} if the reference oscillator is correctly locked.

With an NTSC-4,4 input signal, the H/2 modulator provides no pulses or, in case of phase faults, small pulses with a line-sequentially changing polarity. The latter is caused by the constant burst phase of NTSC signals which is line-sequentially reversed by the H/2 demodulator. The average charge current of C_{21} is, therefore zero and the capacitor voltage equals the biasing voltage.

When a SECAM or NTSC-3,5 signal is received, the difference between the burst and f_0 frequency is so large that the phase changes very rapidly and, as a result, the H/2 pulses are irregular. This causes the average charge current of C_{21} to be zero.

(b) When the decoder is set to NTSC-4,4 the PAL and NTSC-4,4 phase discriminator is activated and the SECAM frequency discriminator is switched off. The PAL phase discriminator and the H/2 demodulator operate as previously described.

With an NTSC-4,4 signal at the input, the output of the NTSC phase discriminator consists of pulses with the same polarity because the burst of the NTSC signal and the reference signal (B–Y) have the same phase.

With a PAL input signal, the NTSC phase discriminator also outputs pulses with the same polarity, because the PAL burst comprises a component which is stable in the negative (B–Y) direction for each line. Capacitor C_{20} at the output of the NTSC phase discriminator is therefore charged by an NTSC-4,4 as well as a PAL input signal, although the decoder is set to the NTSC-4,4 mode.

With NTSC-3,5 and SECAM signals, the average output current of the NTSC phase discriminator is zero ($\Delta V_{20} = 0$) because the frequency of the burst of the carrier frequency does not match that of the reference.

(c) When the decoder is set to NTSC-3,5, the oscillator circuit (including dividers) generates reference signals of about 3,58 MHz and the SECAM frequency discriminator is switched off. The NTSC-3,5 phase discriminator provides demodulated burst pulses with constant polarity. At the H/2 demodulator output, no pulses, or, in case of phase faults, small pulses with alternating polarity appear as in the NTSC-4,4 mode.

For all other colour input signals (PAL, SECAM, NTSC-4,4), the large difference between burst or carrier frequency and reference signal frequency

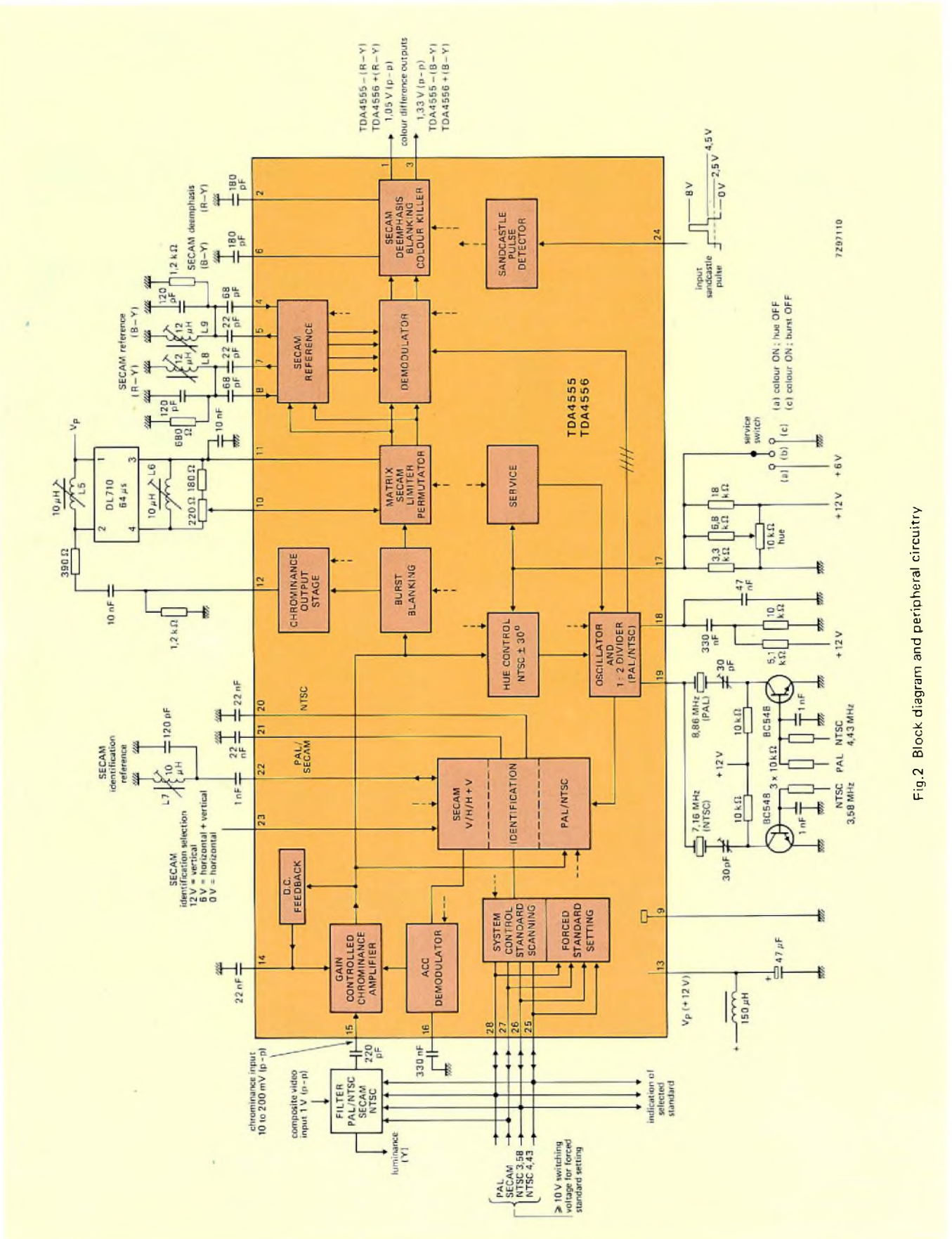


Fig.2 Block diagram and peripheral circuitry

prevents defined discriminator output pulses. As a result, the average charge currents of capacitor C_{20} and C_{21} are zero.

(d) When decoding SECAM, the H/2 demodulator obtains its signals from the SECAM discriminator. The output of the PAL phase discriminator is not used and the NTSC phase discriminator is switched off so no output signal is available ($\Delta V_{20} = 0$).

For SECAM decoding, a frequency discriminator in the recognition block is active. H/2 pulses with line alternating polarity occur when the frequency of the applied signal is alternately higher and lower than the resonant frequency f_{res} of the SECAM identification circuit.

$$f_{res} = (f_{oB} + f_{oR})/2 \simeq 4{,}43 \text{ MHz}$$

Therefore, the output of the H/2 demodulator is a train of equal polarity pulses charging the capacitor C_{21}.

For PAL, NTSC-3,5, and NTSC-4,4 signals, the burst frequency is constant so the output of the frequency discriminator consists of unipolar pulses and the H/2 demodulator outputs alternating polarity pulses. The average charge current of capacitor C_{21} is therefore zero ($\Delta V_{21} = 0$).

The TDA4555 is designed so that identification of SECAM signals can be performed as required by using the special signals in each field blanking period (V-identification) or the burst signal at the back porch (H-identification), or both signals at the same time (H + V-ident). The required standard is selected by applying the appropriate voltage to pin 23 as follows:

$V_{23} < 2$ V (e.g. ground)	H-identification
$V_{23} > 10$ V (e.g. Vsupply)	V-identification
$V_{23} = 6$ V or floating	H + V-identification.

V-identification is more reliable than the H-identification because the identification signals are longer and have a greater frequency deviation ($\Delta f_{I,B} = 3{,}9$ MHz; $\Delta f_{I,R} = 4{,}756$ MHz). With H-identification, only the normal carrier signal at the end of the back porch is available for identification. When it is required to transmit other information during the field blanking period, several transmitters (e.g. in France) stop transmitting the V-identification signals. However, the TDA4555 can easily be adapted to such system changes.

Table I summarizes the foregoing. For b/w signals, the average charge current is zero, so no standard is recognized and the scanning is continuous.

Generation of PAL and NTSC reference signals

For demodulation and identification of the quadrature amplitude-modulated PAL and NTSC colour signals, the reference signals Ref(R−Y) and Ref(B−Y) are needed. These signals are derived from the transmitted burst by a PLL which comprises a voltage controlled oscillator (VCO), a 2:1 frequency divider and a phase discriminator. The oscillator frequency is twice the subcarrier frequency ($2f_o$) and the circuit has the advantage that the two quadrature reference signals are available at the output of the divider.

With PAL and NTSC, the phase discriminator compares the (R−Y) reference signal and the burst. The burst and the colour signal obtained from the a.c.c. stage are applied to the discriminator directly for PAL and via the hue control for NTSC. In the hue control block, the phase of the burst signal can be shifted ±30° by an external voltage of between 2 V and 4 V at pin 17. This voltage is derived from the supply by a simple resistor network. Pin 17 also receives the voltage from the "service" switch. If V_{17} is less than 1 V (e.g. ground), the colour is forced ON and the oscillator free runs because the burst is switched OFF. The oscillator frequency can be adjusted with the trimmers in series with the crystals. If V_{17} is greater than 6 V (e.g. the supply voltage), the colour is forced ON and the hue control is switched OFF.

TABLE I

Charge on storage capacitors C_{20} and C_{21} for combinations of input signals and decoding mode

decoding mode	standard of the colour input signal									
	PAL		NTSC-4,4		NTSC-3,5		SECAM		b/w	
	C_{20}	C_{21}	C_{20}	C_{21}	C_{20}	C_{21}	C_{20}	C_{21}	C_{20}	C_{21}
PAL	0*	+	0*	0	0*	0	0*	0	0	0
NTSC-4,4	+	+	+	0	0	0	0	0	0	0
NTSC-3,5	0	0	0	0	+	0	0	0	0	0
SECAM	0*	0	0*	0	0*	0	0*	+	0	0

0 average charge current $I_{AV} = 0$, $\Delta V_c = 0$, $V_c = \frac{1}{2}$ supply.
\+ average charge current $I_{AV} > 0$, $\Delta V_c > 0$ (assuming correct locking of the reference oscillator and proper switching of the H/2 demodulators)
* NTSC phase discriminators switched off.

The phase discriminator, which provides a VCO control voltage which depends on the phase difference between burst and reference signal, is activated by a burst key pulse. The control voltage is filtered by an external second-order low-pass filter connected to pin 18.

The two crystals for the reference oscillator are both connected between pin 19 and ground via a switch circuit comprising two transistors driven by the external standard switch voltages. To prevent interference, the oscillator is switched off during SECAM decoding.

Colour signal demodulators

Demodulation of the colour signals is performed in the same way as in single standard predecessors.

In the PAL decoding mode, the burst signal is removed from the colour signal derived from the gain controlled chroma amplifier to prevent disturbances caused by reflections in the glass delay-line delayed by other than a single line period. The colour signal is applied to an 18 dB amplifier and driver stage (emitter follower) which compensate for the "worst case" loss in the external delay-line circuit. Colour subcarrier signals CSC_{R-Y} and CSC_{B-Y} are separated by the delay line connected to pin 12 and terminated at both input and output. Direct and delayed signals are matched by a potentiometer in the output termination. Phase matching can be obtained with coils L_5 and L_6 which compensate the delay-line capacitances.

The delayed signal is taken from the potentiometer slider and fed to the internal matrix via pin 10, where the direct and delayed signal are added and subtracted to obtain the separated colour subcarriers CSC_{R-Y} and CSC_{B-Y}. The matrixing is very simple because the demodulators have symmetrical differential inputs and the direct colour signal is available in both polarities. Signals of one polarity are applied to one of the (B–Y) demodulator inputs, and signals of the other polarity to one of the (R–Y) demodulator inputs. The remaining input of both demodulators is supplied with the delayed signal. Unlike in previous PAL decoders, the PAL switch is located just in front of the (R–Y) demodulator, i.e. in the CSC_{R-Y} signal path.

The actual colour signal demodulators are conventional synchronous types comprising an analog multiplying differential stage with a current source in the emitter circuit and balanced cross-coupled switching stages in the collector circuit. The latter are driven by reference signals Ref(R–Y) or Ref(B–Y) and one or both analog inputs receive the colour signal $CSC_{(R-Y)}$ or $CSC_{(B-Y)}$. The colour-difference signals CD, obtained after demodulation, are blanked during the line blanking interval to provide signals with clean levels.

For NTSC decoding, the colour signal is demodulated in a similar manner except that only the direct (undelayed) signal is used. The PAL switch in the $CSC_{(R-Y)}$ path is not used.

For reception of the line sequential SECAM colour signals, a parallel-crossover switch ("permutator") is required before the demodulators. This permutator alternately feeds both demodulators with a direct and (via the external delay-line) a delayed colour signal of the same subcarrier frequency.

After the permutator, both colour channels incorporate a limiter stage to eliminate amplitude modulation. The colour signals are demodulated by quadrature demodulators each comprising an internal multiplier and an external single-tuned phase-shift circuit, known as the SECAM reference circuit. These reference circuits, connected to pins 5/6 and 7/8 cause a phase shift of about 90° for the unmodulated subcarrier frequency. Thus, for unmodulated subcarrier signals, there is no output apart from the biasing voltage. The SECAM reference circuits are adjusted by L_8 and L_9 so that the reference levels appear at the CD outputs when the subcarrier is unmodulated or when the colour is switched off.

In each colour-difference channel, the demodulators are followed by internal low-pass de-emphasis networks which remove the unwanted high-frequency components (harmonics of reference and colour signals).

The colour-difference signals pass, via the output emitter followers with current sources in their emitter circuits, to pins 1 and 3, no matter what decoding mode is selected. They have the following nominal amplitudes referred to a 75% saturated colour bar:

$$V_{(R-Y)} = 1{,}05\ V_{p\text{-}p};\ V_{(B-Y)} = 1{,}33\ V_{p\text{-}p}.$$

For the TDA4555, the polarity of the signals is negative and therefore suitable for input to the Video Combination family TDA3500 (except TDA3506).

The TDA4556 is similar to the TDA4555 except for the positive polarity of the TDA4556 colour difference output signals. Therefore, this TDA4556 can be used with the Video Combination TDA3506.

APPLICATION CONSIDERATIONS

Circuit example

Figure 2 is a tested circuit of a multistandard decoder. A more detailed circuit of the input filters is shown in Fig.3. These filters separate the luminance signal (Y) from the colour signals for the four decoding modes.

The same filters can be used for PAL and NTSC-4,4 signals since they have a similar frequency spectrum. For SECAM signals, it is possible to use the 4,4 MHz subcarrier trap of the PAL/NTSC-4,4 filter but it is then necessary to add a trap tuned to about 4,05 MHz in the Y channel. This filter suppresses the colour signal components below about 4,2 MHz which mainly occur during the "blue SECAM line".

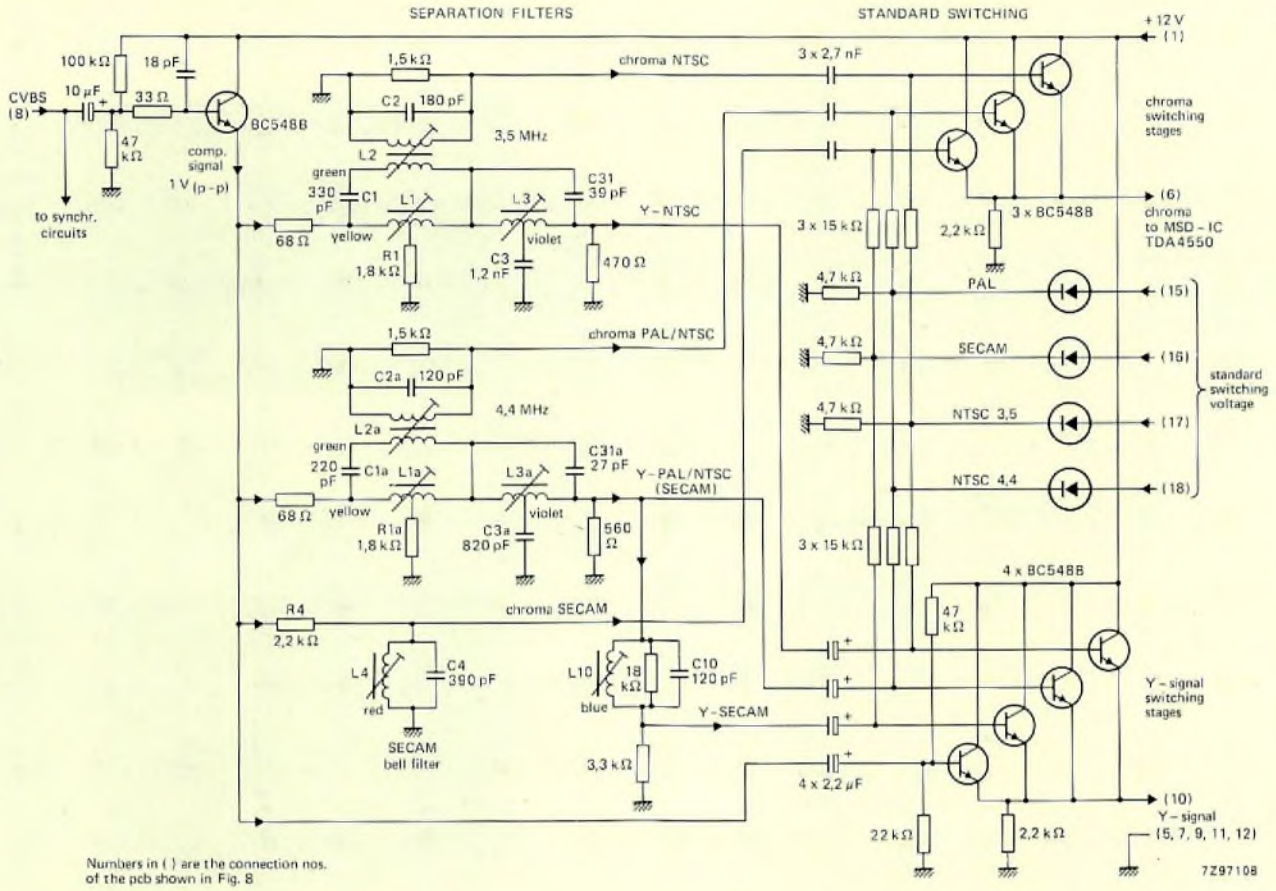


Fig.3 Input filters and standard switching

TABLE 2
Coil data for the multistandard decoder of Fig.2 and Fig.3

coil no.	inductance (µH)	Q	toko type no.	no. of turns	colour	use
L_1/L_{1a}	5,5	>90 (4,4 MHz)	119 LNS-A 4449 AH	8+8	yellow	separation filter
L_2/L_K L_{2a}/L_{Ka}	12,5	>90 (4,4 MHz)	119 LNS-A 4451 DY	24/1	green	colour bandpass filter
L_3 L_{3a}	66,0	60 (2,52 MHz)	KANS-K 4087 HU	19+46*	violet	phase delay correction
L_4	3,8	60 (4,4 MHz)	113 CNS-2 K 843 EG	17 (=14+3)	red	bell filter
L_5, L_6, L_7 & L_{10}	10,0	>80 (4,4 MHz)	119 LN-A 3753 GO	11+11	blue	decoder board and SECAM trap for f_{oB}
L_8, L_9	12,0	>80	119 LN-A 3753 GO	12+12	blue	decoder board

The filter circuits for PAL and NTSC signals are based on a separation filter which also equalizes phase delay. This means that, besides separating the luminance and colour signals, the impulse response of the luminance channel is improved and has symmetrical overshoots, giving the impression of better resolution on the screen. This type of filter is only given as an example. Simpler filters can also be used. The SECAM circuit contains the obligatory "bell" filter. Coil data for the circuit shown in Fig.3 is given in Table 2.

Figure 4 shows oscillograms of the luminance and colour filtering in the three signal paths. It can be seen that the colour passband in the PAL and NTSC decoding mode has its minimum just below the colour subcarrier frequency. This means that mainly the lower sideband of the colour signal is used and, as a result, the filter may have a narrower bandwidth. Generally, the upper sideband of the colour signal is already attenuated by the i.f. filter. The passband of the filter in the SECAM colour signal path has the required "bell" shape as shown in Fig.4(c).

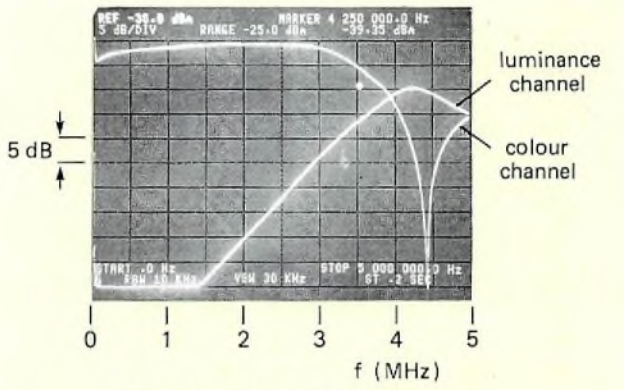
From the low-pass characteristics of the luminance channels, it follows that the subcarriers (4,43 MHz for PAL/NTSC-4,4; and 3,58 MHz for NTSC-3,5) and the unmodulated carrier frequency ($f_{0B} \simeq 4{,}41$ MHz for SECAM) are strongly attenuated. Additionally, low-pass filter ($L_{10}C_{20}$) of the SECAM luminance channel resonates at about 4,05 MHz which provides the required attenuation of frequencies below 4,2 MHz for modulated carriers.

All three separation filters are fed with the CVBS input signal via an emitter-follower (transistor BC548B). Therefore, the complete decoder has a high input resistance and the filters are driven for a low impedance signal source.

Depending on the decoding mode, the luminance signal is fed from the appropriate filter, via the luminance delay line, to the Video Combination IC, and the colour signal is fed via a small coupling capacitor (220 pF) to input pin 15 of the decoder IC.

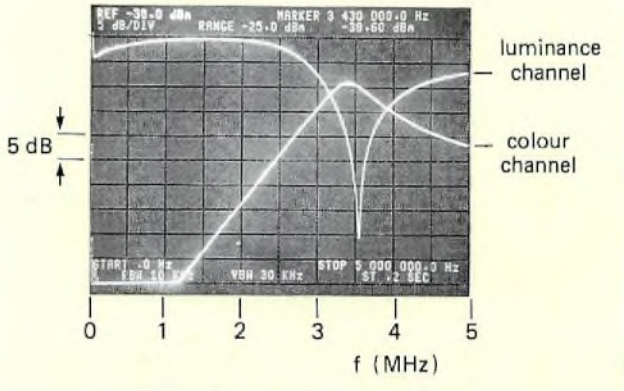
Emitter followers in the colour signal path provide the required switching. There is one for each mode, PAL/NTSC-4,4, NTSC-3,5, and SECAM, feeding a common emitter resistor. Three more emitter followers in the luminance signal path are combined with a fourth which supplies the unfiltered video signal to the Video Combination IC during b/w reception, or while the standards are being scanned. The video signals are applied to the bases of the transistor switches via coupling capacitors, the switch voltages being supplied via resistor-diode networks. The fourth transistor switch in the luminance channel has fixed base biasing of about 4,4 V.

The resistors in parallel with the SECAM tuned circuits determine their Q and therefore the conversion efficiency (dV/df) of the demodulators in the SECAM mode and can be used to set the nominal output values of the CD signals (with a colour bar signal). The switch transistors for the oscillator crystals at pin 19 have their collectors connected, via 10 kΩ resistors, to the supply line. Because they are either fully conducting or completely cut-off and the voltages are low (12 V max.), the type of transistor is not critical.



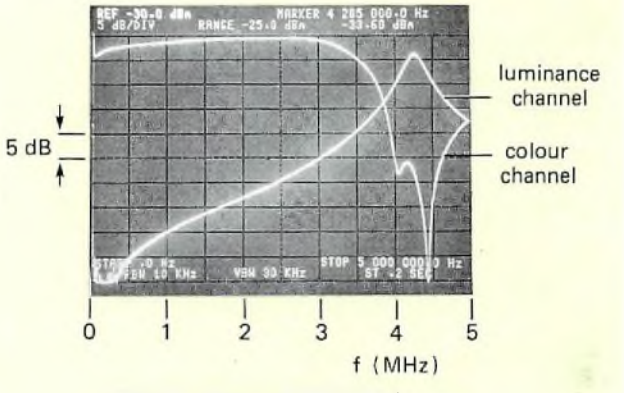
PAL/ NTSC 4,4 (f_0 = 4,433 MHz)

(a)



NTSC 3,5 (f_0 = 3,579 MHz)

(b)



SECAM (f_{0B} = 4,250 MHz)
(f_{0R} = 4,406 MHz)

"Bell" filter (f_{res} = 4,286 MHz)

(c)

Fig.4 Amplitude-frequency characteristics of input filter

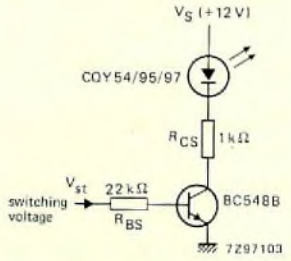


Fig.5 Example of standard indicator circuit

The standard control voltage outputs (pins 25 to 28) can deliver a current of 3 mA which is insufficient to drive a LED to indicate the standard to which the circuit is set. An additional transistor amplifier such as that shown in Fig.5 is therefore required. Resistor R_{CS} determines the current through the LED, and R_{BS} limits the maximum base current.

If an indication is provided for each of the standard switch voltages, then it is easy to establish which standard, if any, is recognized. When all the diodes light up in sequence, the circuit is still scanning and no standard has been recognized.

Alignment of the input filter

The alignment of both the PAL/NTSC-4,4 and NTSC-3,5 separation filters consists of three procedures for each separation filter.

1. *Alignment of the colour bandpass*

   Apply a sweep signal [f = 3,5 MHz (4 MHz); $\Delta f \cong \pm 3$ MHz (±3 MHz)] to the filter input (PCB pin 8). Connect an oscilloscope to PCB pin 6 and make the filter output available at IC pin 6 by applying an external switch voltage to the appropriate switch transistor. Adjust L_2(L_{2a}) for maximum output at 3,45 MHz (4,2 MHz).

2. *Alignment of the compensation circuit*

   Apply a 3,58 MHz (4,43 MHz) subcarrier to the filter input (PCB pin 8) and adjust L_1(L_{1a}) so that the voltage at the Y output of the filter is minimum. This Y output can be measured at the 470 Ω (560 Ω) terminating resistor, or at PCB pin 10, if the proper switch transistor is activated by an external switch voltage.

3. *Alignment of the phase delay equalizer*

   Apply a 16-100 kHz square-wave to the filter input (PCB pin 8) and connect an oscilloscope to the output of the luminance filter (470 Ω or 560 Ω terminating resistor). Alternatively, the oscilloscope can be connected to PCB pin 10, if an external switch voltage is applied to the appropriate input. Adjust coil L_3(L_{3a}) to obtain a symmetrical overshoot at the leading and trailing edges of the pulse.

Because the impulse response of a receiver also depends on the i.f. filter, it is recommended that the filter be included in the test signal path when aligning L_3/L_{3a}. In practice a square-wave-modulated i.f. signal should be applied to the input of the i.f. circuit for this adjustment.

Filter $L_{10}C_{10}$, attenuates the SECAM colour signal in the luminance channel below 4,2 MHz. L_{10} is adjusted so that an applied 4,05 MHz signal has minimum amplitude at the output of the SECAM Y-filter (terminating resistor 3,3 kΩ, or PCB pin 10, if an external switch voltage is applied to the appropriate input).

To align the SECAM "bell" filter, a SECAM colour bar is applied to the filter input (PCB pin 8) and an external switch voltage (e.g. the supply voltage) to PCB pin 16 to force the SECAM decoding mode. L_4 is then adjusted for minimum amplitude-modulation of the filtered colour signal (PCB pin 6).

To locate the coils to be adjusted, it is useful to colour code them as shown in Table 2 and Fig.3.

Decoder alignment

a. PAL and NTSC-4,4 signals

Force the PAL decoding mode by an external voltage exceeding 9 V (e.g. the supply voltage) applied to pin 28 of the IC (or PCB pin 15) and apply a PAL colour signal (e.g. colour bar) to the filter input, PCB pin 8. Connect IC pin 17 to ground with the service switch. The colour is forced ON and the oscillator is free-running because the PLL oscillator circuit does not receive the burst.

Adjust the trimmer in series with the 8,8 MHz crystal for minimum colour rolling. Alternatively, observe the colour-difference signals at IC output pins 1 and 3 and minimize the beat frequency with the trimmer. This 8,8 MHz oscillator adjustment is also valid for the decoder in NTSC-4,4 mode.

To adjust the phase of the delay-line decoder, apply a PAL colour bar signal to the input of the circuit (PCB pin 8) with the service switch in its normal (middle) position. Adjust L_5 and L_6 to minimize amplitude differences of each colour bar in the (B-Y) output signal (IC pin 3 or PCB pin 13).

Alternatively, minimize the PAL structure (pairing of the lines) observed on the screen. If the adjustment range of L_5 is too small, adjust L_6.

To adjust the amplitude of the delay-line decoder, apply an NTSC-4,4 colour bar signal to the input of the circuit (PCB pin 8) and connect IC pin 17 to the supply line with the service switch. The colour is forced ON and the hue control is switched off. Adjust the 220 Ω potentiometer connected to pin 4 of the DL 711 delay line for minimum amplitude differences of each colour bar in the (R–Y) output signal (IC pin 1 or PCB pin 14)

using an oscilloscope, or, observing the picture-tube screen, minimize the PAL structure (pairing of the lines).

Special test patterns can also be used for delay line adjustment.

Finally, remove the external switching voltage applied to pin 28 and put the service switch in the mid (normal) position.

b. NTSC-3,5 signals

In this case only the 7,2 MHz oscillator has to be adjusted. Force the circuit to the NTSC-3,5 decoding mode by connecting IC pin 26 or PCB pin 17 to the supply voltage. Apply an NTSC-3,5 colour signal to the filter input (PCB pin 8). Connect IC pin 17 to ground with the service switch. The colour is forced ON and the oscillator is free-running because the PLL oscillator does not receive burst signals.

Adjust the trimmer in series with the 7,2 MHz crystal for minimum colour rolling. Alternatively, observe the CD signals at the IC output pins 1 and 3 and minimize the beat frequency.

Finally remove the connection between PCB pin 17 and the supply voltage and put the service switch back to its mid position.

c. Alignment for SECAM signals

Force the circuit in the SECAM decoding mode by connecting the supply voltage to IC pin 27 (or PCB pin 16). Apply a SECAM colour bar to the filter input (PCB pin 8).

Connect IC pin 23 (or PCB pin 20) to the supply line to activate the H-identification. Connect a high impedance (>10 MΩ) voltmeter between IC pin 21 and ground. Adjust coil L_7 for the maximum voltage at IC pin 21.

Observe the –(R–Y) output signal at IC pin 1 (PCB pin 14) with an oscilloscope. Adjust L_8 so that the levels of the black and white bars are in accordance with the level inserted during blanking.

Observe the –(B–Y) output signal at IC pin 3 (PCB pin 13) with an oscilloscope. Adjust L_9 so that the levels of the black and white bars are in accordance with the levels inserted during blanking.

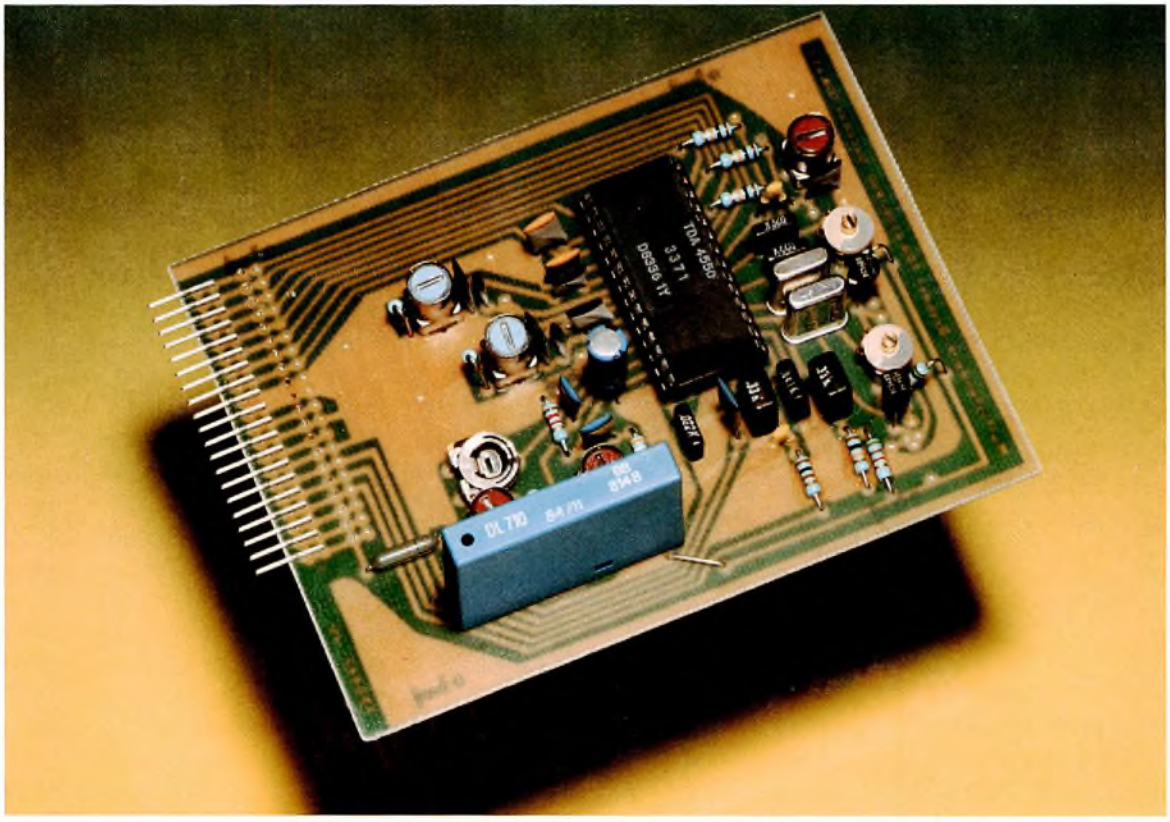


Fig.6 Photograph of decoder board of Fig.7

Example of a printed circuit board

Figure 7 is an example of a printed-circuit board for the decoder shown in Fig.2. Figure 6 is a photo of the component side of the assembled board. The board does not incorporate the hue control, the service switch, or the input filter circuits, but a suitable pc board for the input filter circuit is shown in Fig.8. This latter board is designed so that it can be plugged into the AMP connector shown in Fig.7 and 8.

The two boards together form the complete MSD including the input filter. The external signals are applied to, or taken from, the decoder via the pins of the decoder board connector. The composite video input signal at PCB pin 8 and the luminance signal at PCB pin 10 are available for further processing. PCB pin 6 (the colour signal) is not used.

It is possible to connect the filter board differently or use a different filter circuit. Then the decoder board receives the colour signal from the filter board via PCB pin 6. PCB pins 8 and 10 (the composite video and the luminance signal respectively) are not used. The luminance signal for the Video Combination IC is taken directly from the filter board. All other details of the pc board are as shown in Fig.6 to 8.

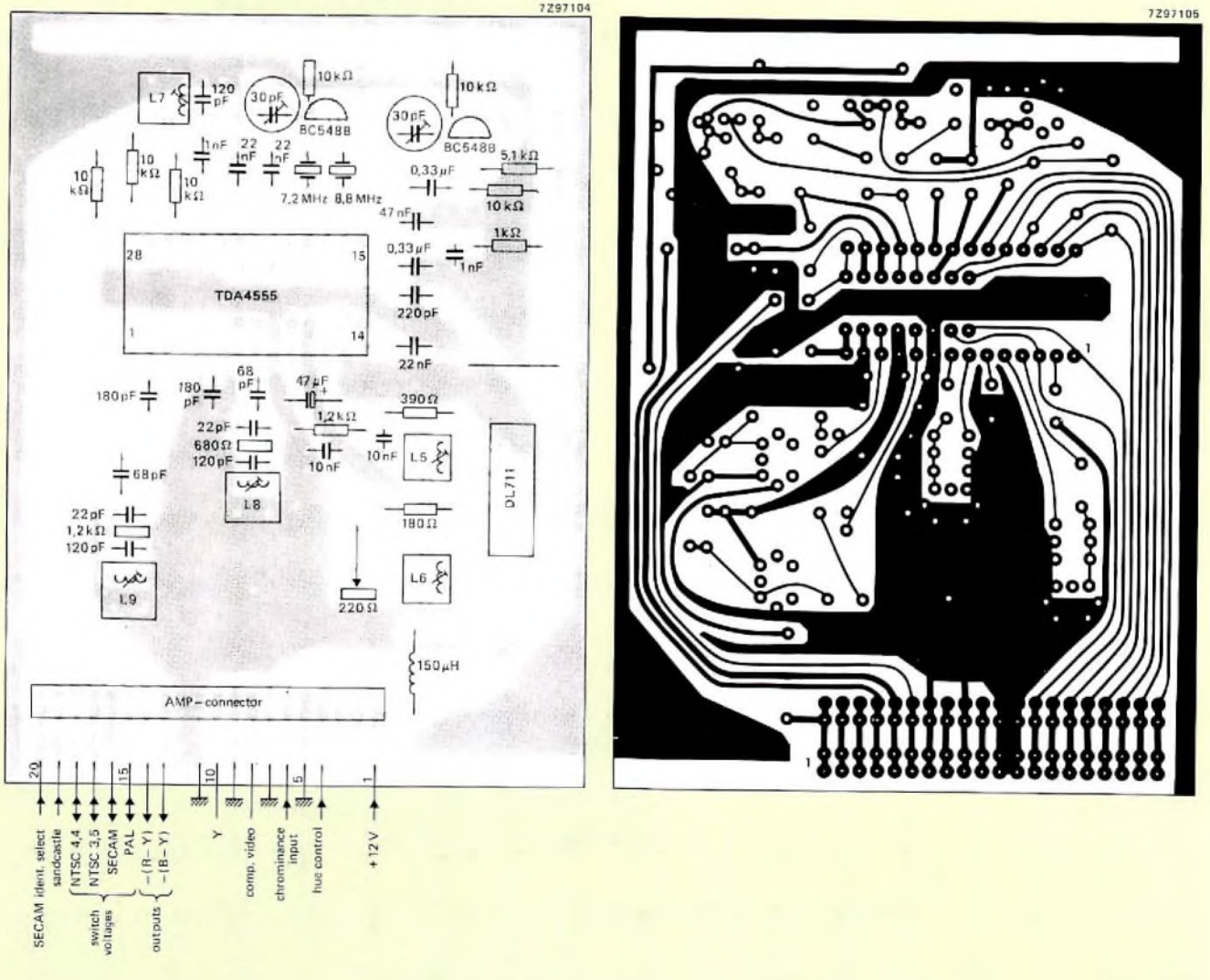


Fig.7 PCB for circuit of Fig.2 – No input filter

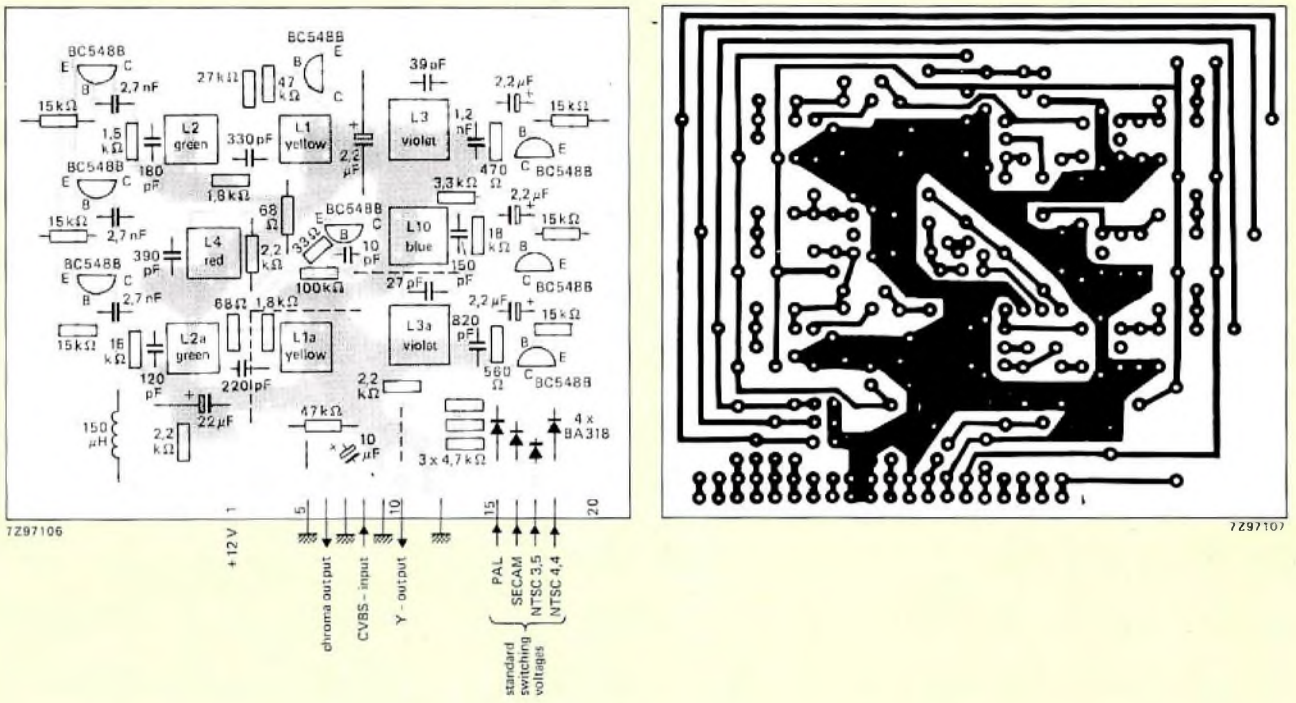


Fig.8 PCB for input filter and standard switching

Use of the PC board for a PAL only decoder with the TDA4510

To efficiently manufacture a family of receivers, based on the same main pc board, the TDA4555/56 can be used as a single standard decoder (e.g. a PAL only decoder) but the 'pin-aligned' TDA4510 is a cheaper alternative. The connections of the TDA4510 and those of the TDA4555 are shown in Fig.9. Apart from the omission of many peripheral components, only small changes in the external circuitry are needed.

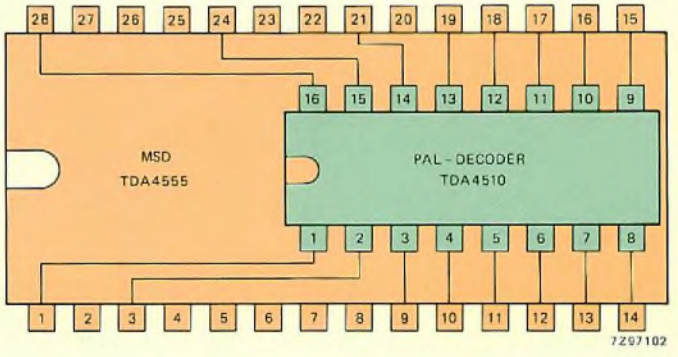


Fig.9 Multistandard decoder TDA4555 and PAL decoder TDA4510 are "pin-aligned" to allow them to be easily interchanged

RF ICs for portable communications equipment

D. ANDERSON and R. J. ZAVREL jr.

With applications for low-power, battery-supplied r.f. circuits on the rise, designers of portable communications equipment will have to pay closer attention to power consumption and circuit size. Low-power r.f. ICs can replace many discrete components in the r.f. signal-processing chain.

Two radio-frequency ICs that work at frequencies previously unattainable in low-power r.f. devices allow the design of receiver circuits that serve many of today's communications applications. These applications – particularly those in the new field of cellular radio – gain the obvious benefits of the ICs' lower power consumption and smaller size.

The NE602 is a 200 MHz mixer, and the NE604 combines the usual i.f. amplifier, limiter, and demodulator functions with a logarithmic-response received-signal-strength indicator, or RSSI (Fig.1). Each IC draws about 2,5 mA using the recommended 6 V power supply. Consequently, combined power consumption is typically 30 mW. The chips meet industry standards for cellular mobile radio systems.

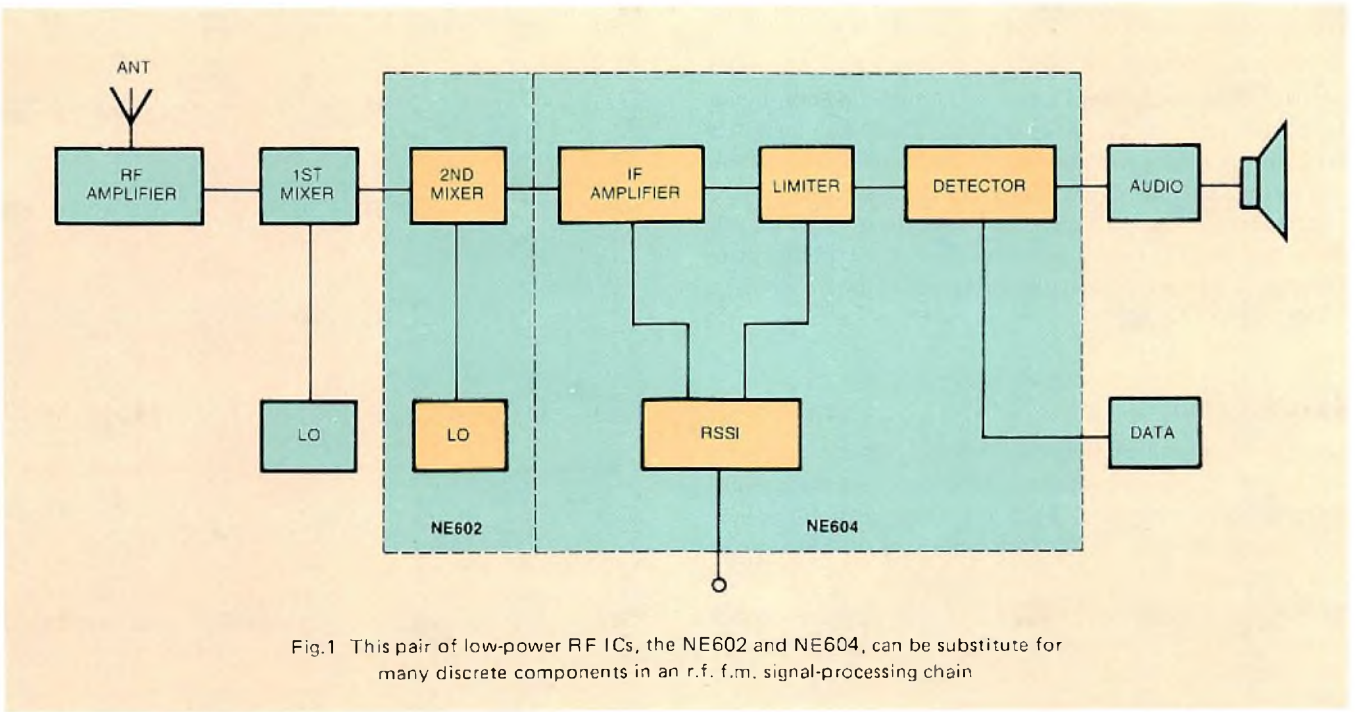


Fig.1 This pair of low-power RF ICs, the NE602 and NE604, can be substitute for many discrete components in an r.f. f.m. signal-processing chain

THE NE602

Figure 2 is a functional diagram of the NE602. The chip's mixer and local oscillator (LO) operate at frequencies up to 200 MHz. The chip features 18 dB conversion gain, a third-order intercept point at −15 dB input level, a 5 dB noise figure, and 0,25 μV input sensitivity (with a 10 dB signal-to-noise ratio). The oscillator works in the usual fashion with an external crystal (LC tank circuit). Alternatively, you can use the oscillator simply as a buffer for an external local oscillator.

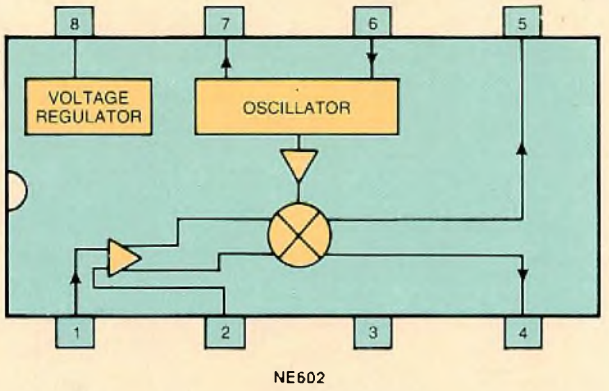


Fig.2 The NE602's local oscillator drives a switching section, or "Gilbert Cell", instead of a passive diode mixer

A cascode differential amplifier (at pins 1 and 2) provides most of the conversion gain and determines the intermodulation and noise performance of the NE602. This amplifier feeds the switching section while the LO toggles that section. Taken together, the cascode and switching sections form a multiplier, or "Gilbert Cell". The multiplication of the r.f. input and the LO signals produces the desired intermediate frequency, which is usually the difference of the frequencies.

Spurious products

Because the analog multiplier isn't perfect, other frequencies will appear at the chip's output. Harmonic- and intermodulation-distortion products result from imperfect multiplicative transfer functions. The switching action of the mixer also produces other spurious signals because the LO signal is, in effect, a square wave. Because of the strong harmonic content of the LO square wave, its harmonics will also mix with the r.f. signal and produce a complex set of sum and difference Fourier-series components.

Improving a multiplicative transfer function generally requires that you implement faster mixer switching, which, in turn, usually requires higher LO signal voltages and currents. However, by virtue of its low-power mixer design and a very fast low-power bipolar process (f_T = 6 GHz), the NE602 exhibits a good transfer function without the need to resort to higher power levels. To provide comparable intermodulation performance, the more common passive diode-ring mixers typically require LO power levels that are an order of magnitude greater than the NE602's. In addition, the diode ring will cause a conversion loss of at least 6 dB; the additional amplifier stages needed to compensate for this loss thus require even more power, chip area, and components.

THE NE604

Figure 3 is a functional diagram of the NE604. The chip consists of an i.f. amplifier, a limiting amplifier, a detector, a muting circuit, and a voltage regulator.

The NE604's i.f. and limiting-amplifier section forces the input signal to clip regardless of the signal's amplitude. The frequency-modulated, constant-amplitude (limited) signal then goes to the quadrature detector. The detector receives two equivalent i.f. signals: the limiter's original output signal and the same signal shifted in phase by the quadrature filter (Fig.4). The detector multiplies the two out-of-phase signals to yield the modulated audio component (using a technique similar to that used by the NE602's multipliers). This audio current appears at both the audio and data outputs (pins 6 and 7). The two outputs are identical but for the fact that the muting circuit affects the audio output while leaving the data output alone.

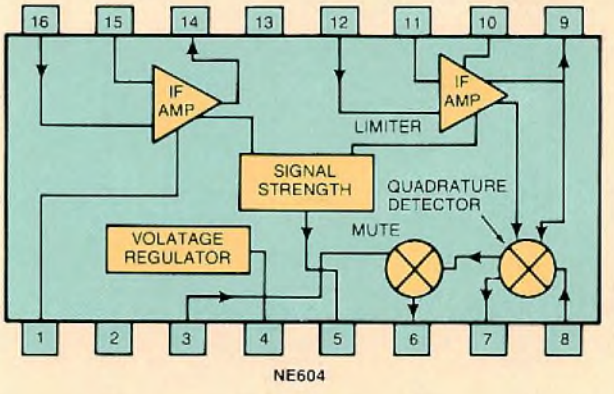


Fig.3 The NE604 has the usual i.f. amplifier and limiting amplifier; it also generates the received-signal-strength indication that's required for cellular radio systems

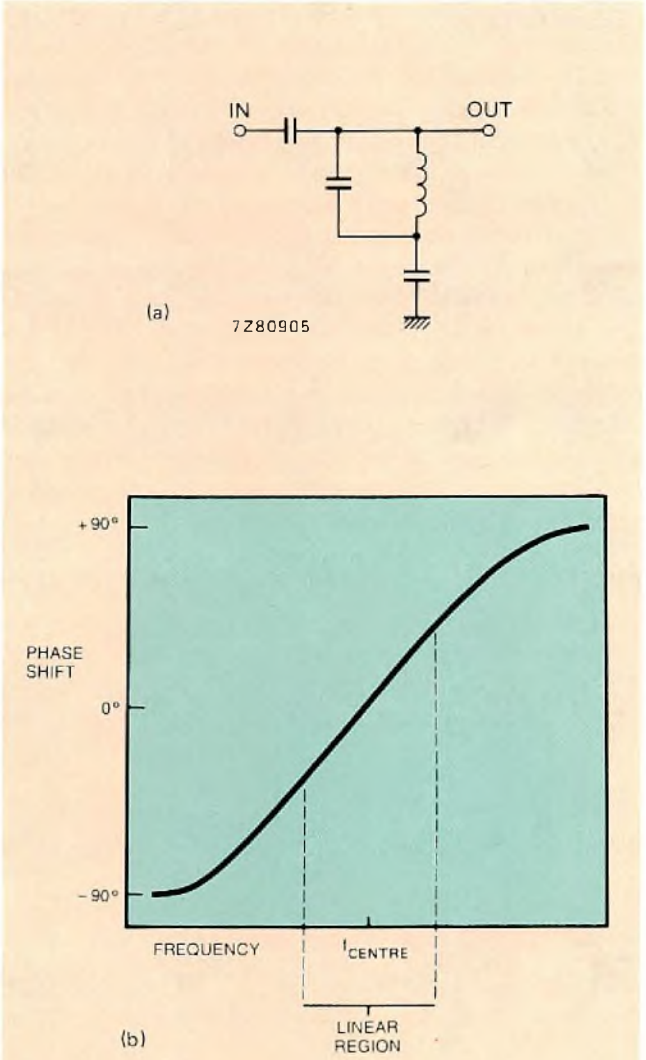


Fig.4 The NE604 requires an external quadrature filter for proper operation of its internal quadrature detector. The filter phase-shifts the limiter's output signal. The detector receives this phase-shifted signal and the limiter's output signal

RSSI specs present challenge

The most stringent specs to meet in cellular-radio applications are those for the RSSI. Specifications call for a 1 V d.c.-output change for every 20 dB r.f.-input change. The tolerance is 3 dB over an 80 dB dynamic range. To meet this spec, the NE604 RSSI output is a function of the sum of the output amplitudes of each of the i.f. and limiting stages. Each stage contributes to the RSSI until it saturates. As the r.f.-input level increases, stages will sequentially saturate. A proprietary technique derives the RSSI's required logarithmic response from this sequential-stage limiting and stage-amplitude summing. The summing circuit then drives a current source whose output appears on pin 5.

The inner workings of the RSSI would be of little interest to engineers if they always used both of the NE604's i.f. stages. In some cases, however, designers use only the second-i.f./limiter stage. Under these circumstances, you cannot get the full range of the RSSI, because its summing circuit doesn't receive information from all the i.f. stages.

USING THE NE602 AND NE604

The NE602's application is relatively straightforward once you have certain essential design information. Figure 5 shows several possible input and output circuit configurations, and Table 1 summarizes their relative advantages and disadvantages. If you use the single-ended configuration, you must a.c.-couple one of the input leads to ground. For single-ended outputs, you can allow the unused output pin to float. Figure 6 shows the internal circuitry associated with NE602's oscillator at pins 6 and 7. The circuit in Fig.7 is recommended for third overtone crystal-controlled applications. A fundamental trap assures correct overtone oscillation. In this circuit, you specify the crystal for its parallel-mode resonant frequency. The crystal's equivalent-loading capacitance should be 3 pF. Although Fig.7 shows a

Table 1
NE602 I/O characteristics

	configuration	advantages	disadvantages
input (pins 1, 2)	single-ended	no sacrifice in third-order performance	increase in second-order products
	balanced	reduced second-order products	impedance match more difficult
output (pins 4, 5)	single-ended	simple interface to filters	3 dB reduction in output, less r.f. and LO isolation
	balanced	3 dB improvement in output, better LO and r.f. isolation at the output	more complex circuitry required

crystal oscillator, you can use a Hartley or Colpitts tank circuit to the same effect. If you use an external LO, pin 6 can act as a buffer/driver input. The optimal drive level in this mode is between 200 and 300 mV rms.

Figure 8 shows a simple demonstration circuit incorporating both the NE602 and NE604. The input frequency to the NE602 is 45 MHz (a typical first intermediate frequency for cellular radio applications). The circuit has ceramic filters between the NE602 and NE604 and between the i.f. and limiter sections of the NE604 (pins 14 and 12). Depending on its passband, the filter between pins 14 and 12 can not only improve the circuit's selectivity, it can also reduce broadband noise contributed by the NE604's signal-processing stages. Not all designers choose to incorporate this second filter. They rely instead on prefiltering the input to the NE604.

The RSSI's output linearity depends to some degree on the insertion loss between pins 14 and 12. The circuit realizes optimal RSSI tracking when the total interstage loss is 6 dB. Figure 9 shows a simple op-amp buffer for the RSSI output that provides a low-impedance voltage source. Depending on the external load's impedance at pin 5, you may or may not need this source.

Figure 10 shows that the RSSI output is temperature dependent. As the device heats up, pin 5 sources more current. Figure 11 shows a simple temperature-compensation circuit. You can use either a single silicon diode, as shown here, or two Schottky diodes in series to lower the equivalent resistance of the voltage divider at pin 5 as the temperature increases. Alternatively, a thermistor or other temperature-compensation techniques offer possible solutions. The choice of a scheme depends on your application and choice of buffer op amp.

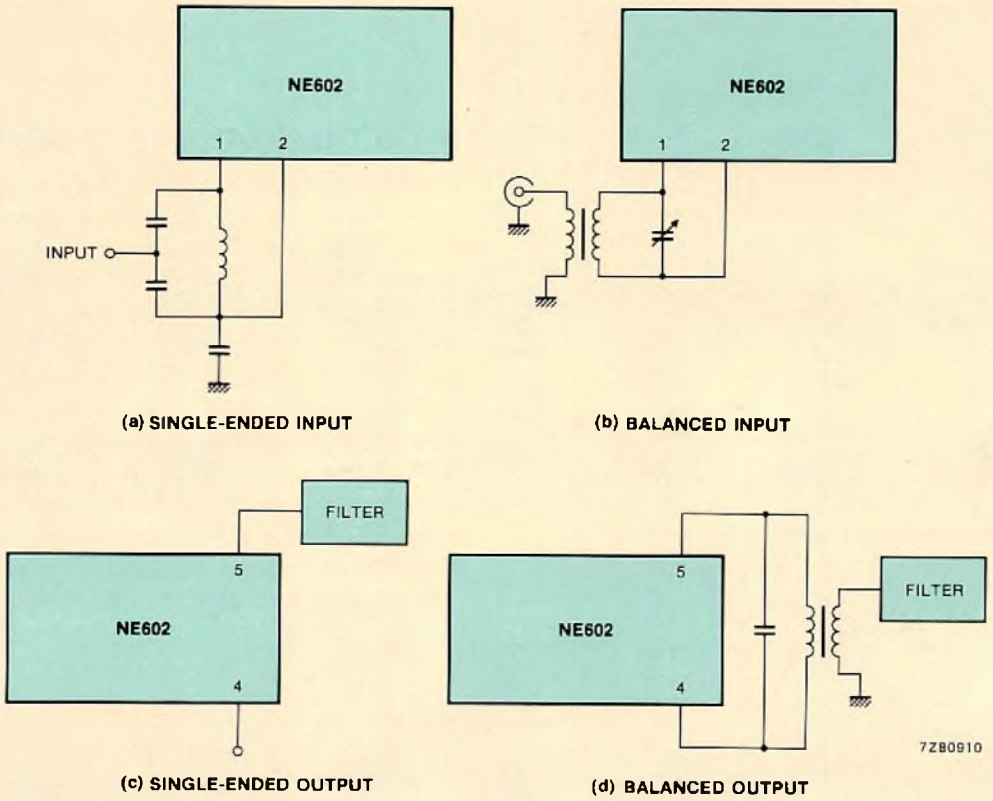


Fig.5 Amenable to a variety of input and output configurations, the NE602 allows you to build less complex circuits at lower costs

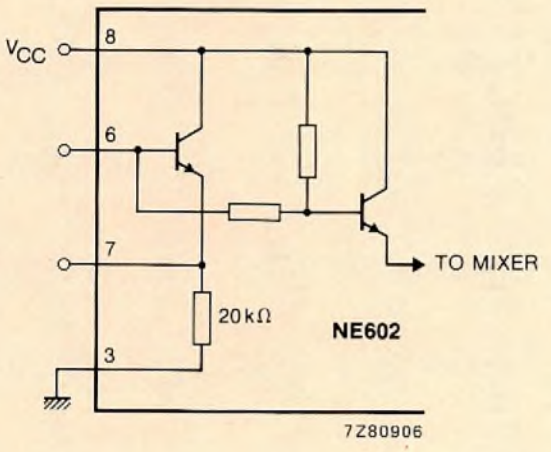


Fig.6 In addition to driving a conventional LC tank circuit, the NE602's oscillator circuit can function as a buffer/driver for an external local oscillator

Figure 12 summarizes the five important system-performance parameters of the NE602 and NE604 plotted against received-signal strength. The data comes from the demonstration circuit shown in Fig.8. The audio output at pin 6 is constant above an r.f. input level of −110 dBm at the NE602's input. The THD+noise curve represents the rms sum of all harmonic distortion products plus noise appearing at the audio output.

Table 2 shows which pins on both devices you can connect to either V_{CC} or ground. It also indicates the resistive component (whether source- or load-impedance values) for signal-path device pins. Although V_{CC} can range from about 4,5 to 8 V for both devices, 6 V is the optimal supply value. Figure 13's graphs show the performance of the NE602 with respect to input level, temperature, and supply voltage.

Though the chips meet cellular-radio specs, they also suit other battery-powered r.f. applications. Moreover, the NE602 works just as well as a modulator as it does as a demodulator. As a consequence, with a computer-controlled, varactor-tuned LO, you could use the chips to frequency-multiplex and demultiplex data on a local-area network. The demodulator of the NE604 suits either narrowband or broadband demodulation. Test-equipment designers can use the RSSI of the NE604 for spectrum analyzers, r.f. voltmeters, filter alignment, or channel-strength measurements.

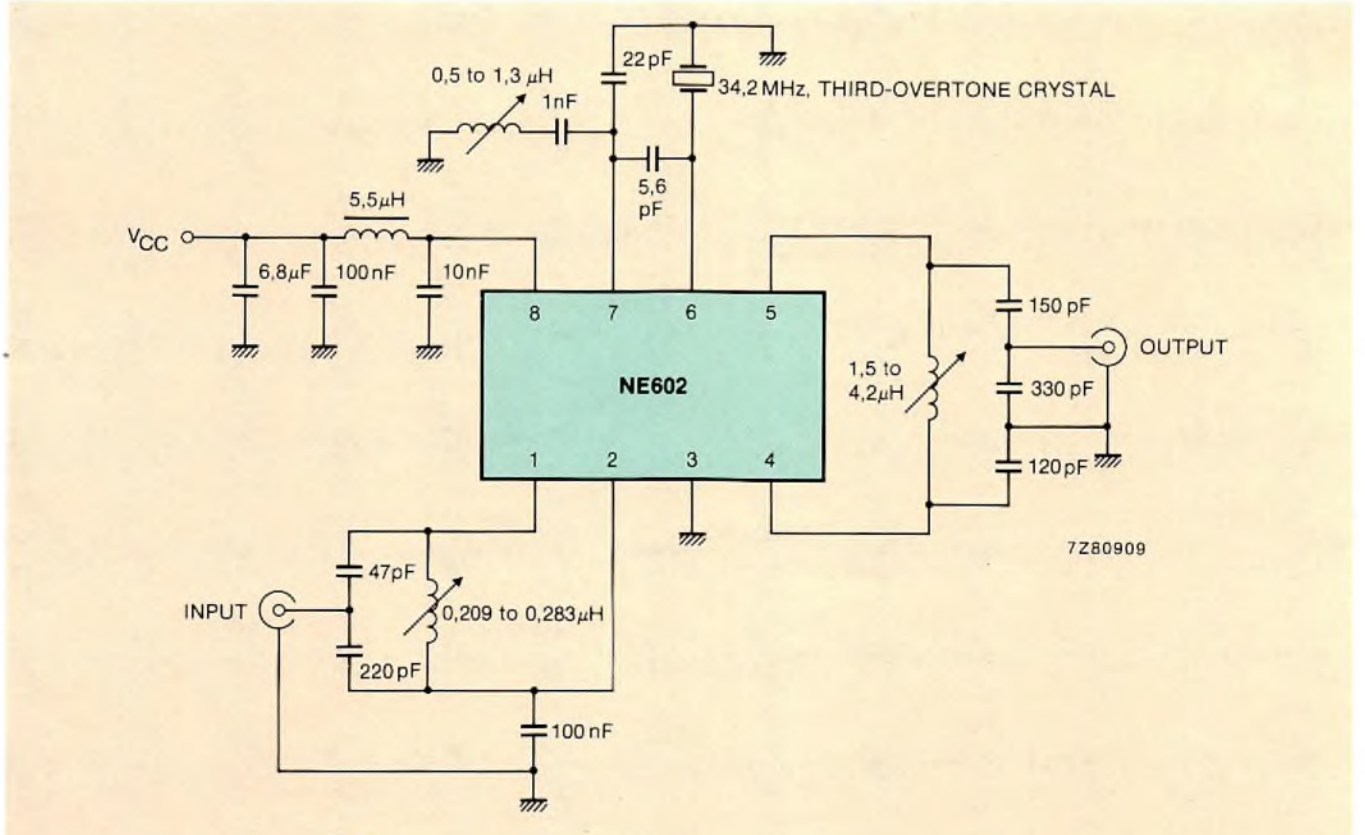
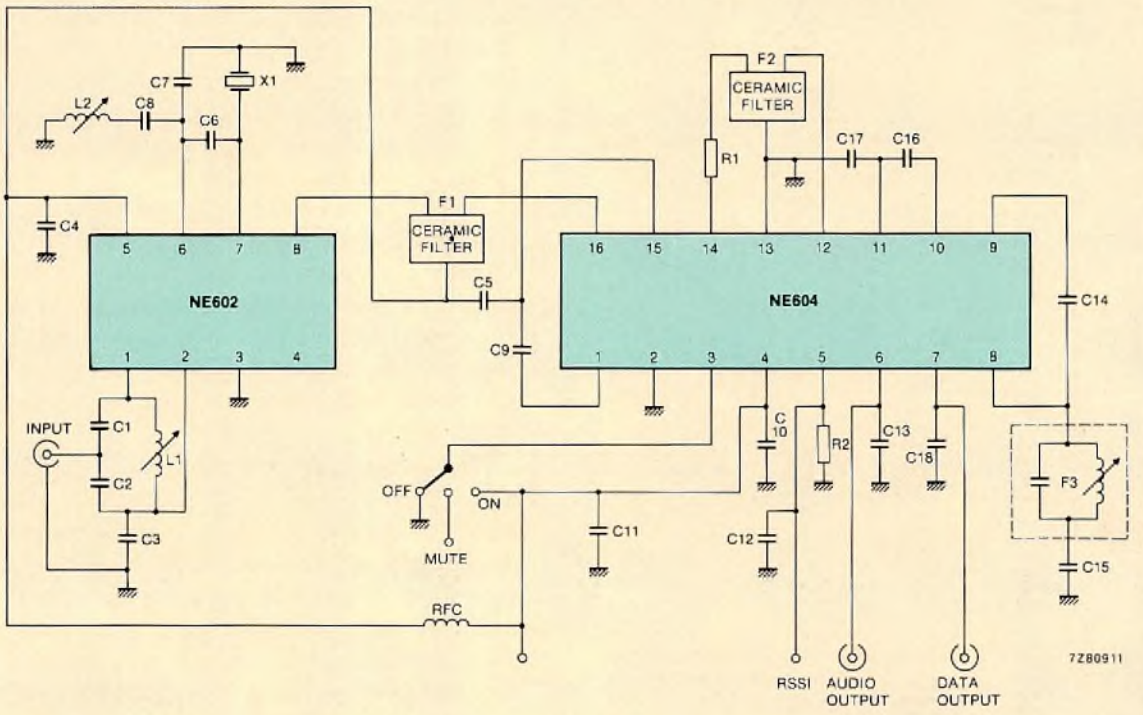


Fig.7 This is a recommended oscillator configuration for third overtone applications. The NE602 can also be used in the fundamental mode



(a)

C_1 = 47 pF ± 2%, 100 V, N750 ceramic
C_2 = 200 pF ± 2%, 100 V, N750 ceramic
C_3 = 0,1 μF ± 10%, 50 V, polyester
C_4 = 10 nF ± 80%, 63 V, K10000 – 25X ceramic 20%
C_5 = 0,1 μF ± 10%, 50 V, polyester
C_6 = 5,6 pF ± 25%, 100 V, NPO ceramic
C_7 = 22 pF ± 2%, 100 V, N150 ceramic
C_8 = 1 nF ± 10%, 100 V, K2000 – Y5P ceramic
C_9 = 0,1 μF ± 10%, 50 V, polyester
C_{10} = 0,1 μF ± 10%, 50 V, polyester
C_{11} = 6,8 μF ± 20%, 25 V, tantalum
C_{12} = 1 nF ± 10%, 100 V, K2000 – Y5P ceramic
C_{13} = 15 nF ± 10%, 50 V, polyester
C_{14} = 10 pF ± 2%, 100 V, NPO ceramic
C_{15} = 0,1 μF ± 10%, 50 V, polyester
C_{16} = 0,1 μF ± 10%, 50 V, polyester
C_{17} = 0,1 μF ± 10%, 50 V, polyester
C_{18} = 150 pF ± 2%, 100 V, N1500 ceramic
R_1 = 1,5 kΩ ± 5%, 1/8 W, carbon composition
R_2 = 100 kΩ ± 1%, 1/4 W, metal film
RFC = 5,5 μH, r.f. choke JW Miller 542-4609
L_1 = 0,209 to 0,283 μH, adjustable v.h.f. coil Miller 48A257MPC
L_2 = 0,5 to 1,3 μH, adjustable coil 1811-0036TW
F_1 = 455 kHz, ceramic filter Murata SFG 455A3
F_2 =
F_3 = 455 kHz, i.f. filter Toko A2549
X_1 = 44,545 MHz, third-overtone crystal

(b)

Fig.8 This demonstration circuit (a) and parts list (b) is the basis for all the performance data given in Figs 10, 12 and 13. Note the two interstage ceramic filters — one between the chips and the other between pins 14 and 12 of the NE604. Designers have some latitude in choosing the values for filters when setting the circuit's selectivity

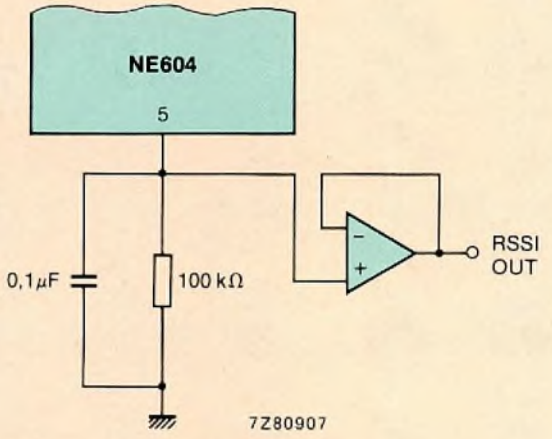


Fig.9 The received-signal-strength indicator may require buffering, depending on the load impedance at pin 5

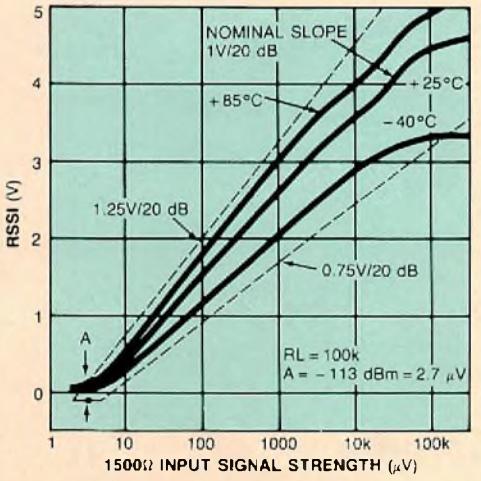


Fig.10 RSSI varies with temperature and may need temperature compensation for some applications

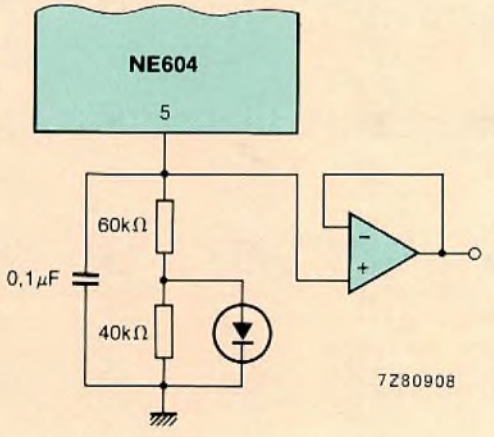


Fig.11 A simple silicon-diode/voltage-divider circuit provides some temperature compensation. Depending on your application, you might need a thermistor or a pair of Schottky diodes in series instead of the silicon diode

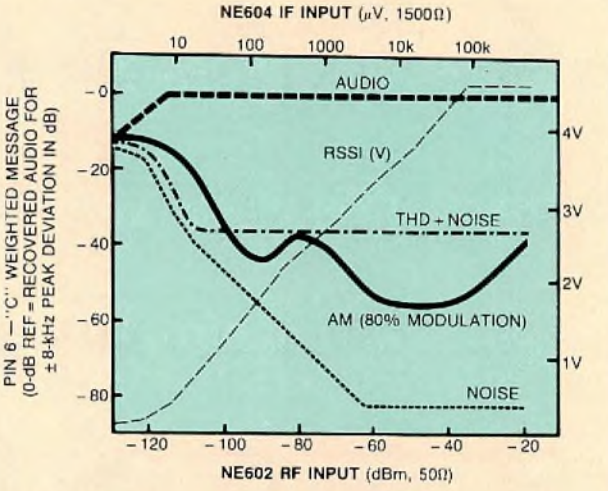


Fig.12 Summarizing the chip pair's performance over its input-signal range, this graph shows a flat audio output and a nearly linear received-signal-strength indication

Table 2
NE602 and NE604 pin-outs

pin	d.c. path to V_{CC}	d.c. path to GND	impedance (if applicable) and other information
NE602			
1	no	no	1500 Ω with o
2	no	no	a.c. coupled to ground
3	no	yes	ground connection
4	yes	no	1500 Ω internal
5	yes	no	resistors to V_{CC}
6	yes	no	several kΩ
7	no	no	
8	yes	no	V_{CC}
NE604			
1	no	no	
2	no	yes	ground
3	no	no	
4	yes	no	V_{CC}
5	no	no	RSSI out
6	no	no	audio out
7	no	no	data out
8	no	no	detector input
9	no	no	i.f. amp output
10	no	no	
11	no	no	limiter output
12	no	no	limiter input
13	no	yes	ground
14	no	no	i.f. amp. output
15	no	no	i.f. amp. input
16	no	no	i.f. amp. input

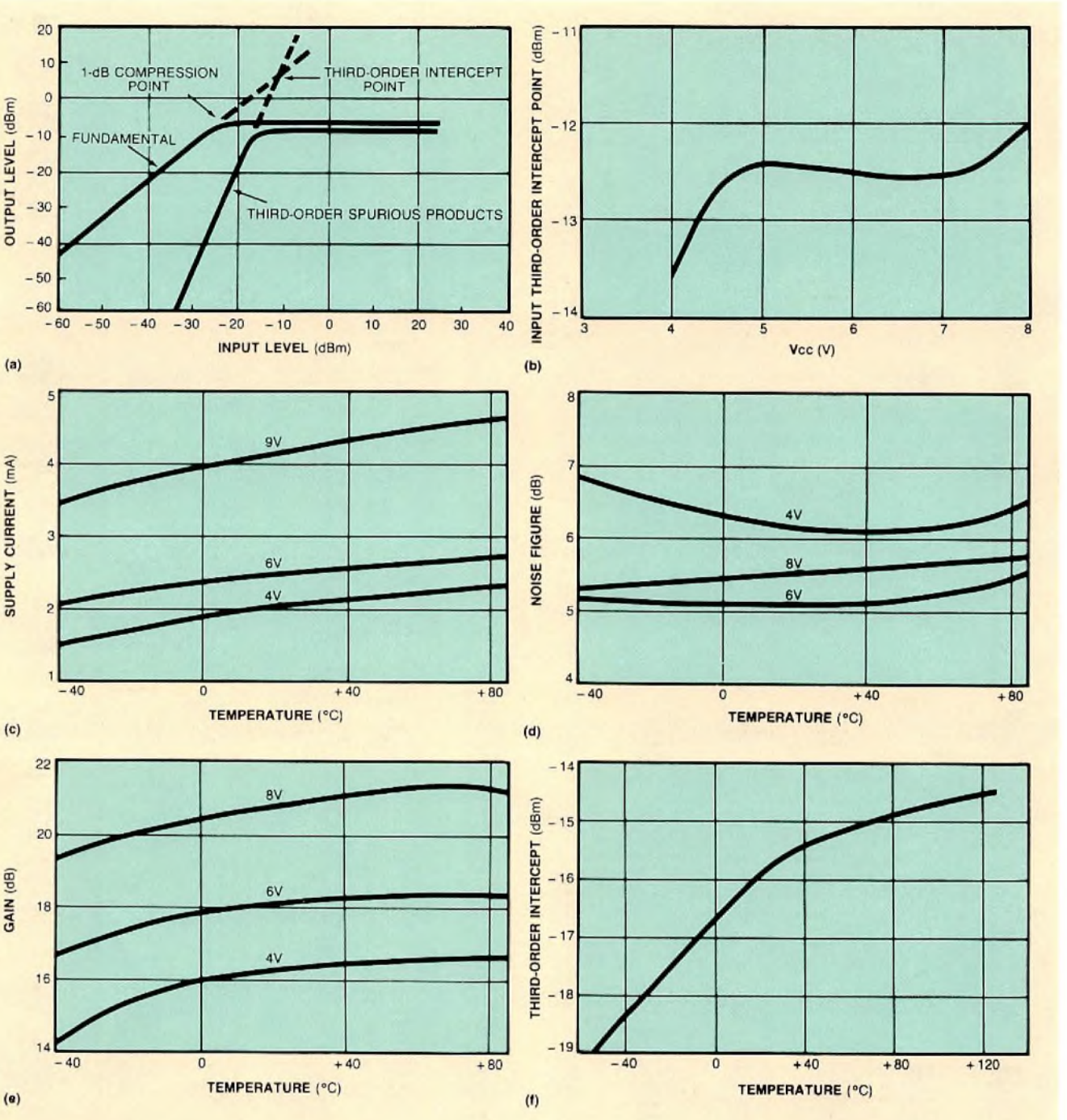


Fig.13 These graphs describe how the NE602 performs with respect to variations in input level, supply voltage, and temperature. The third-order intercept point in (a), (b) and (f) is a useful parameter that indicates a mixer's performance in a single figure of merit and allows you to compare one mixer's design with another. Part (a) shows how the dominant third-order spurious harmonics increase in strength more rapidly than does the fundamental. Although the two lines cannot actually cross (the mixer saturates at the 1 dB compression point), the imaging third-order intercept point shows that you need to keep the input level to the mixer below saturation (within signal-to-noise ratio constraints) to avoid high levels of unwanted products

ACKNOWLEDGEMENT

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Integrated a.m. receiver circuit

J. SCHUYLENBURG

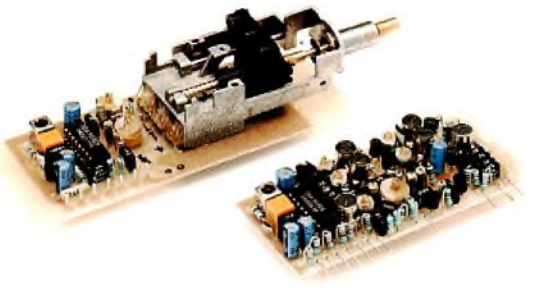
Successor to the well-known TDA1072, the TDA1072A is an inexpensive integrated a.m. radio circuit that performs all the active functions between the aerial and the audio power amplifier. Its ability to handle a wide dynamic range of input signals and its low distortion make the TDA1072A suitable for use in a wide range of car radios, domestic radios and tuners. The TDA1072A brings the TDA1072 right up-to-date to meet present trends in the design of the a.m. section of a radio, trends such as varicap diode tuning, a.m. stereo facility and electronic search tuning. Performance improvements include a 6 dB increase in sensitivity over most of the input signal operating range, and 55 dB ripple rejection between the supply voltage and the oscillator output.

With the TDA1072A, designers have complete freedom of choice in tuning method, gain and selectivity, since none of the aerial circuit has been integrated. And the TDA1072A is ideal for use with low-cost hybrid i.f. filters.

Semi-professional and professional applications outside the a.m. broadcast bands using local oscillator frequencies up to 60 MHz and down to ultrasound frequencies are also possible.

The main features of the TDA1072A are:

- high sensitivity: 15 μV aerial input for 26 dB signal-to-noise ratio, m = 0,3
- large signal handling capability, low distortion and high signal-to-noise ratio
- particularly suitable for use with varicap diode tuning owing to a constant low-level output voltage (typ. 130 mV r.m.s.) from the local oscillator
- separate buffered local oscillator output (320 mV p-p, pin 10) for digital frequency synthesizers
- internal a.g.c. circuit with fast settling time – essential in electronic search tuning – and low distortion at low modulation frequencies
- logarithmic field-strength output for simple generation of stop-pulses and for driving a signal strength indicator or meter
- internal stand-by switch operated by logic levels
- requires very few peripheral components
- operates from supply voltages between 7,5 and 18 V
- ambient operating temperature –40 °C to +80 °C.



Laboratory models (left) of the permeability-tuned medium-wave car radio of Fig.2 and (right) of the varicap diode tuned car radio of Fig.8

CIRCUIT AND PERFORMANCE

Figure 1 shows the block diagram of the TDA1072A. Although basically similar to its predecessor (Ref.1), the TDA1072A offers:

- 6 dB improvement in signal-to-noise ratio owing to redesigned input circuitry
- 55 dB improvement in ripple rejection owing to redesigned oscillator circuitry
- new field strength curve optimized for LED bar indicators and easy stop-pulse generation with selectable level.

The main differences in performance between the two circuits are given in Table 1.

R.F. input

A redesigned input circuit gives a 6 dB improvement in signal-to-noise ratio over most of the operating range, see Figs.2 and 3. To obtain the full improvement, the source impedance of the r.f. input circuit should be reduced from 1,6 kΩ (TDA1072) to 1 kΩ (f_i = 1 MHz), the latter value being a compromise between large signal capability (low cross modulation) of permeability-tuned circuits and sensitivity.

In addition, this value allows low-impedance electronically-tuned r.f. input stages with FETs (especially those used as source-followers) to be used. Moreover, it allows a home-radio frame antenna to be connected to the TDA1072A without using a FET. The antenna forms part of the r.f. input circuit coil, which is a transformer directly connected to the r.f. input of the TDA1072A.

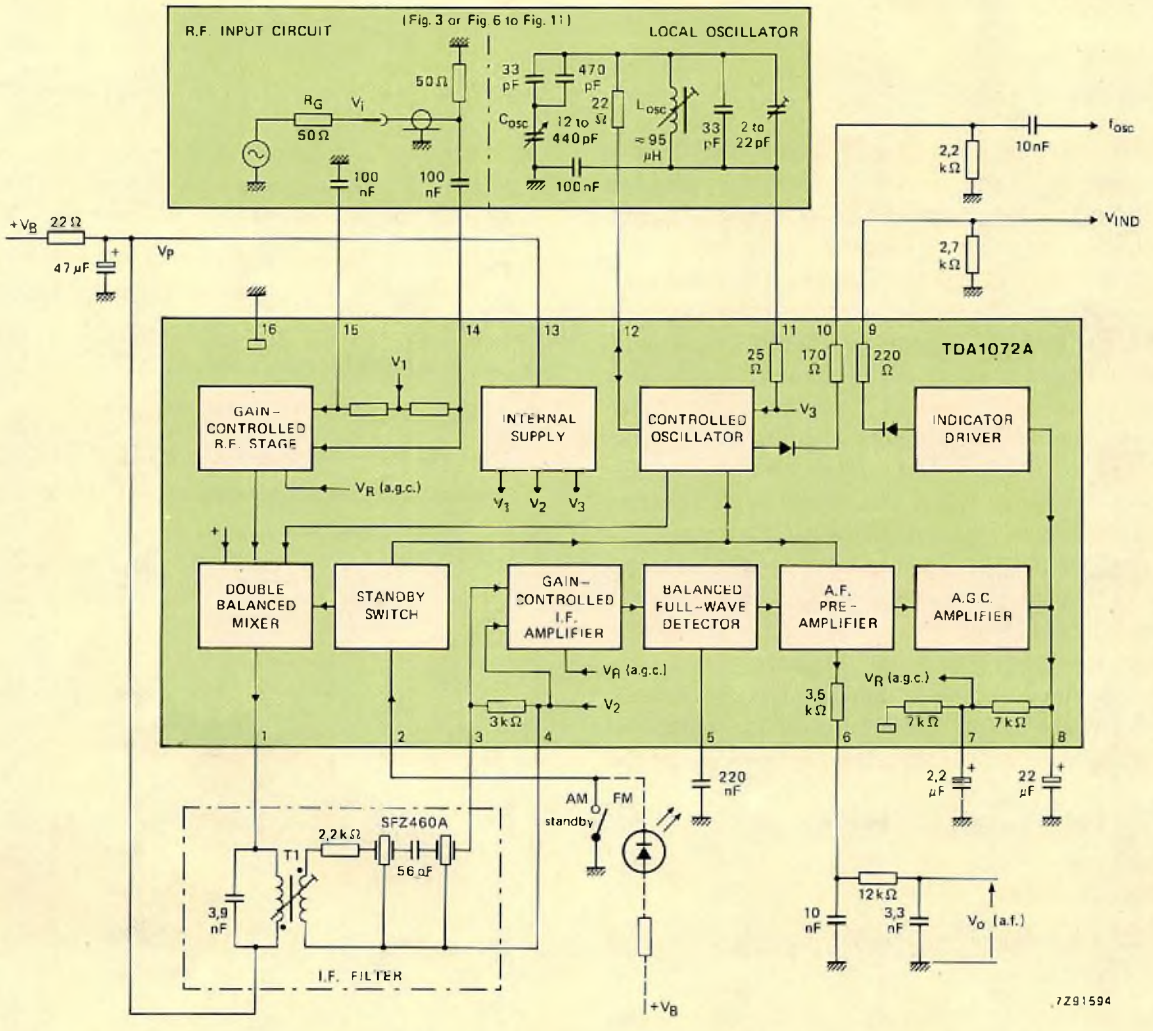


Fig.1 TDA1072A and test circuit

TABLE 1. Performance of the TDA1072A and TDA1072

		TDA1072A	TDA1072	
sensitivity (see also Fig.3):				
r.f. input voltage[1]) for				
(S+N)/N = 6 dB	V_i	1,5	2,2	μV
(S+N)/N = 26 dB	V_i	15	30	μV
(S+N)/N = 46 dB	V_i	150	550	μV
start of a.g.c.	V_i	30	14	μV
large signal handling:				
max. r.f. input voltage (pins 14 & 15)				
d_{tot} = 3%, m = 0,8	V_i	500	600	mV
d_{tot} = 3%, m = 0,3	V_i	700	800	mV
d_{tot} = 10%, m = 0,3	V_i	900	1200	mV
a.g.c. control range				
for a 6 dB change of V_o	dV_i	91	91	dB
1 dB change of V_o	dV_i	86		dB
a.f. output voltage at V_i = 1 mV, f_i = 1 MHz, m = 0,3 and f_m = 400 Hz	V_o(af)	310	300	mV
THD of a.f. output voltage (see Fig.3) V_i = 500 mV; m = 0,3	d_{tot}	1% (m = 0,3)	1,8% (m = 0,8)	
oscillator frequency range	f_{osc}	0,6 – 60[2])	0,6 – 60	MHz
oscillator output current	$-I_{11}$ max.	20	15	mA
ripple rejection	dV_{11}/dV_{13}	55	0	dB
field strength indication range		114	114	dB

All values are typical and measured in the circuit of Fig.1 unless specified otherwise.
[1]) V_p = 8,5 V (TDA1072A), 15 V (TDA1072); f_i = 1 MHz, f_m = 400 Hz; m = 0,3.
[2]) operation at < 0,6 MHz possible.

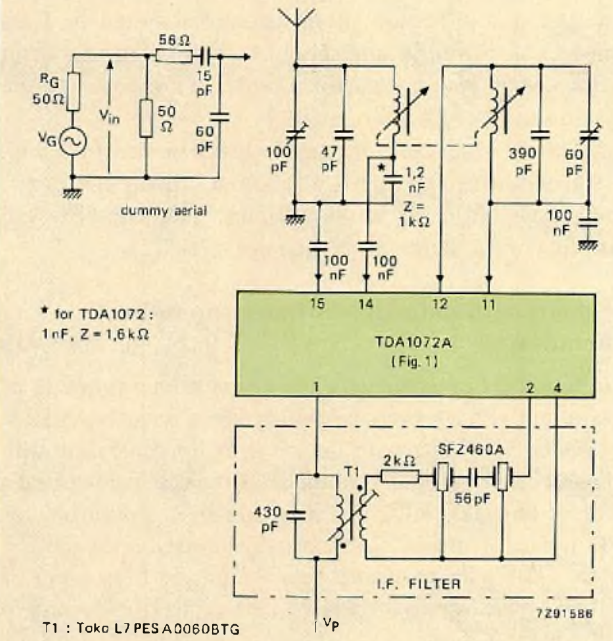


Fig.2 Aerial and local oscillator circuits for a permeability-tuned medium-wave car radio whose performance is shown in Fig.3

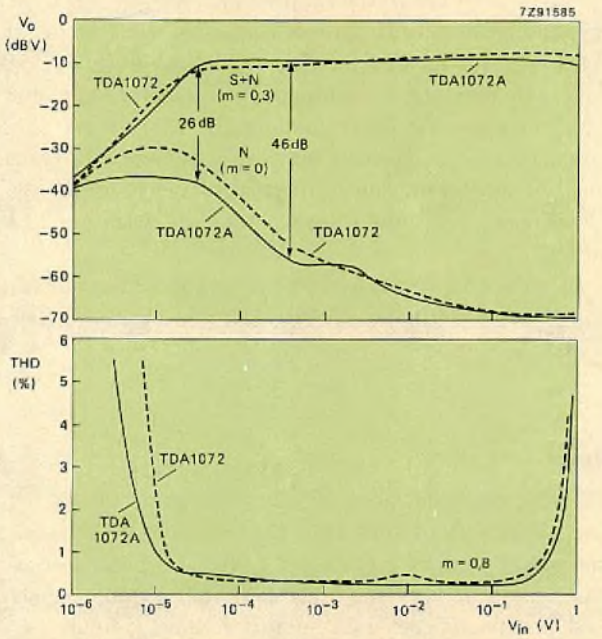


Fig.3 Performance of the a.m. section of the car radio circuitry shown in Fig.2. f_m = 400 Hz; V_p = 8,5 V

The input impedance at 1 MHz (pins 14 and 15, both surge-protected) is 5,5 kΩ//22 pF for an r.f. input <300 μV; 8 kΩ//22 pF for an input >10 mV.

Tuning behaviour of the TDA1072 and TDA1072A are different owing to the former's proportional a.g.c. and the latter's more integrating a.g.c. With the TDA1072, the optimal tuning position could be identified by the rapid increase of noise with detuning. With the TDA1072A, the noise only increases slowly with detuning. This is advantageous in mechanically-tuned radios since slight detuning (due to vibration, temperature) produces only a small increase in noise and distortion.

For optimal tuning and sensitivity at very low r.f. input signals, a 220 nF metal foil capacitor should be connected between pin 5 and earth. This replaces the 470 nF electrolytic capacitor needed with the TDA1072.

Local oscillator

The voltage-controlled oscillator provides signals of low distortion and high spectral purity even when tuned with varicap diodes. It delivers an almost constant output of typically 130 mV for impedances from 500 Ω to 200 kΩ. Internal temperature compensation circuitry ensures ultra stable signals even on short waves. Only a few external components are required to complete the oscillator.

An additional buffered oscillator output is provided (pin 10, 320 mV p-p; 200 mV TDA1072) for use in synthesizer-tuned radios.

The oscillator of the TDA1072A is d.c. referenced to earth (V_{11} = 4,2 V i.e. 6 V_{BE}) unlike the TDA1072 which was d.c. referenced to the supply ($V_{11} = V_{13} - 1{,}4$ V). This new arrangement has improved the ripple rejection between the supply voltage and the d.c. oscillator voltage by 55 dB. Hence, frequency modulation of the oscillator signal due to supply voltage ripple is minimised. Note, there should always be a d.c. connection between pins 11 and 12 (usually a coil or resistor) owing to internal biasing. For stability, a 100 nF capacitor should be connected between pin 11 and earth.

In order that band-switching diodes as well as transistors may be used with the TDA1072A, pin 11 can switch up to 20 mA.

Mixer

A double balanced mixer is used to generate the i.f. signal. The mixer output (pin 1) is the collector of a transistor pair which requires a positive d.c. voltage. Since a resistive load would reduce the maximum i.f. output signal, an inductor should be used in the coupling circuit to the i.f. amplifier.

High i.f. gain allows the i.f. selectivity to be provided by an external hybrid or ceramic filter. Hybrid i.f. filters are recommended for reasons of cost. These should have a transfer impedance of

$$Z_{21} = V_{34}/I_1 = 700\ \Omega,$$

and an input impedance between 3 kΩ and 5 kΩ to prevent overloading the mixer.

I.F. amplifier and detector

The i.f. amplifier comprises two cascaded differential amplifier stages with independent gain control.

The low-noise full-wave balanced envelope detector provides a linear low-distortion output over a wide dynamic range. Residual i.f. carrier is blocked from the signal path by an internal low-pass filter.

A.F. preamplifier

The emitter-follower output with an internal series resistor enables external low-pass filtering of the a.f. signal to be designed as required. Note: in applications with ferrite rod aerials, the external capacitors should be close to the IC to minimize i.f. interference.

AGC amplifier

This amplifier provides a control voltage proportional to the carrier amplitude. Second-order filtering of the a.g.c. voltage gives low distortion over the whole range of amplitudes (even at low modulation frequencies) in addition to fast settling time of the a.g.c. – essential when this signal is used to derive stop pulses in electronic search tuning. The values of the capacitors (pins 7 and 8) in the external filter shown in Fig.1 provide a compromise between short settling time and low distortion. Both capacitors should be positioned close to the IC and should be connected to a main earth to avoid coupling earth currents. In low-cost sets, the capacitor at pin 7 can be omitted.

An 86 dB a.g.c. control range holds the level of the a.m. i.f. signal constant (within 1 dB) over a broad range of r.f. input levels. In a.m. stereo systems, this simplifies the matrixing of the stereo difference signal (Ref.2).

Field strength indicator output/stop-pulse generation

A buffered d.c. output which is a logarithmic function of aerial input voltage over the full dynamic range is available for driving a field strength indicator or for generating stop pulses in search-tuning systems (Fig.4). The field-strength curve of the TDA1072A (Fig.5) has been optimized for LED indicator drivers, but can still be used with meters. Up to 2 mA may be drawn (pin 9) and with an input of 500 mV between pins 14 and 15, the typical field-strength output is 2,8 V.

A diode is incorporated in the output stage so a common indicator can be used to display f.m. and a.m. field strengths without the need for a switch.

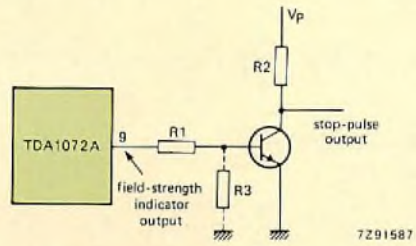


Fig.4 Simple stop-pulse generation circuit

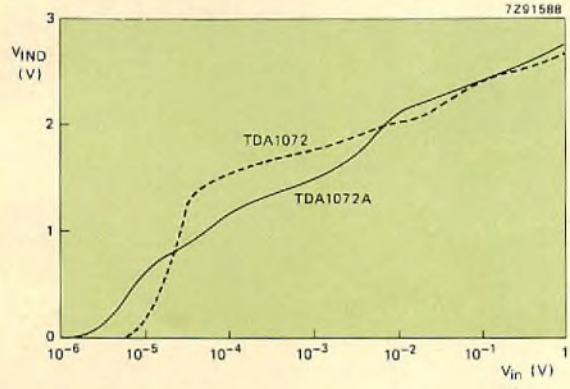


Fig.5 Field-strength indication voltage characteristic for the circuit of Fig.2. f_i = 1 MHz, f_m = 0, m = 0, V_p = 8,5 V

Internal supply voltage

An internal hum filter is completed by connecting a 47 μF electrolytic capacitor to pin 13. The connections from the capacitor to pin 13 and to the i.f. filter should be short.

APPLICATIONS

Existing designs using the TDA1072 can usually be upgraded using the TDA1072A. However, some circuits may have to be modified owing to different d.c. levels (Table 2) and the new field strength curve.

Figures 6 to 11 give an indication of the applications possible with the TDA1072A.

TABLE 2
Difference in D.C. voltages (volts) between the TDA1072A and TDA1072, supply 8,5 V

pin	TDA1072A	TDA1072
10	0,7	4,5
11 & 12	4,2	7,2
14 & 15	4,2	2,7

all other voltages remain unaltered.

MECHANICALLY-TUNED RADIOS

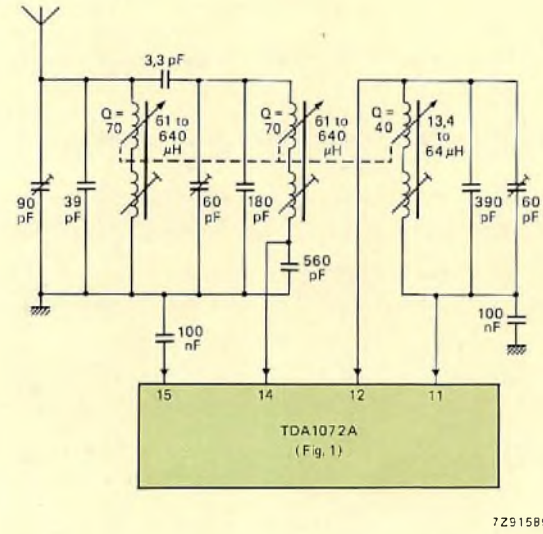


Fig.6 Aerial and local oscillator circuits for a permeability-tuned car radio with input band-pass filter. Permeability tuning coil: Hopf VM BC2.4.2A

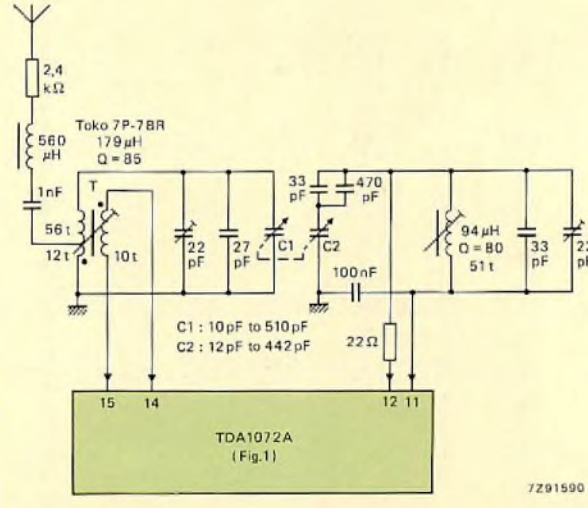


Fig.7 Aerial and local oscillator circuits for a variable-capacitor tuned medium wave domestic radio

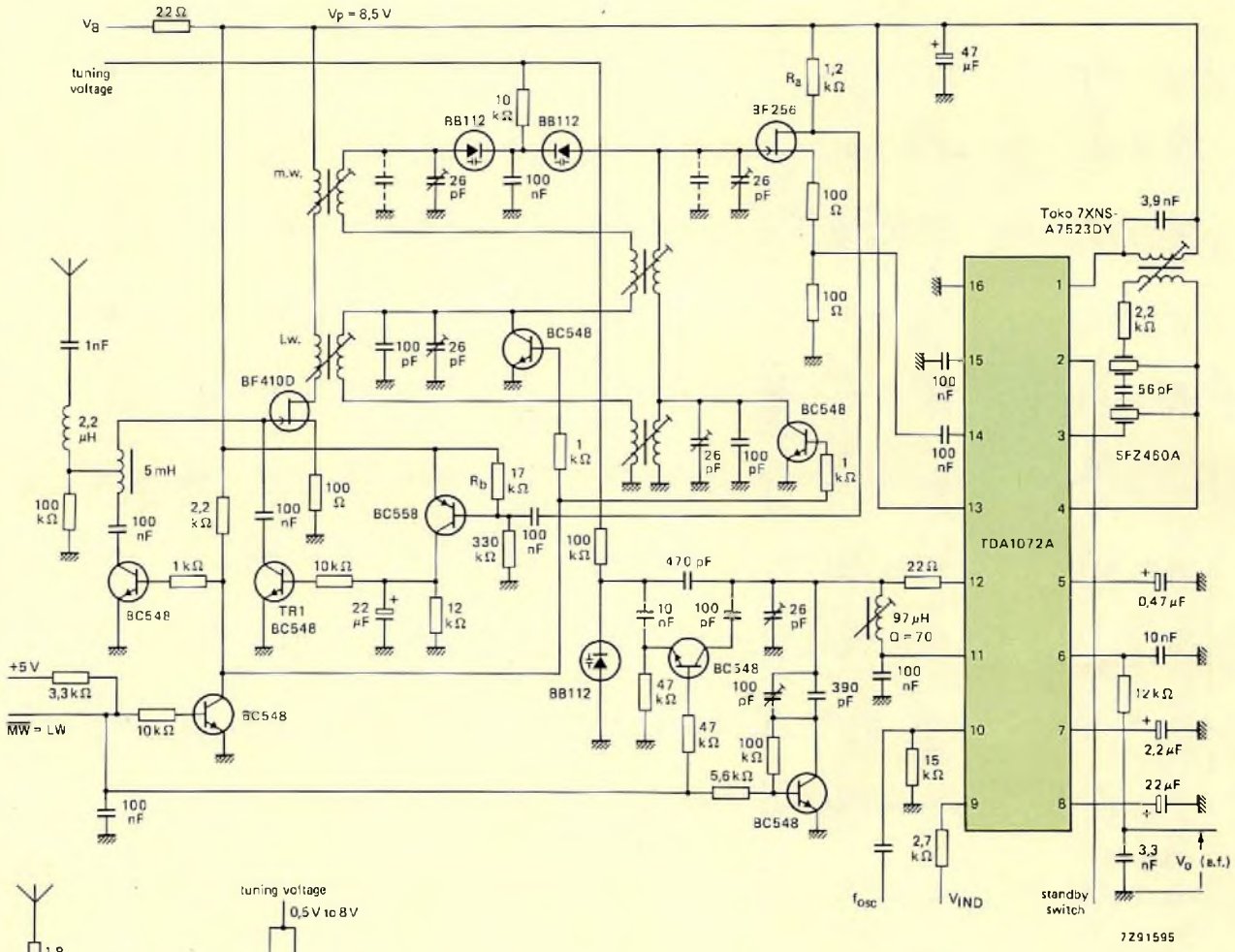


Fig.8 A varicap diode tuned long/medium-wave car radio with a.g.c. for large signal handling capability. The diode-tuned r.f. preamplifier provides large signal handling capability. For strong aerial signals, TR1 loads the antenna, keeping the gate voltage of the BF410D and the a.c. voltage across the varicap diodes low (130 mV for r.f. input signals exceeding 5 V). The slope of the a.g.c. is set by R_a and the onset of gain control by R_b. Because the r.f. gain control is derived from the output of the tuned r.f. preamplifier, there is no masking of desired weak signals situated close to strong ones

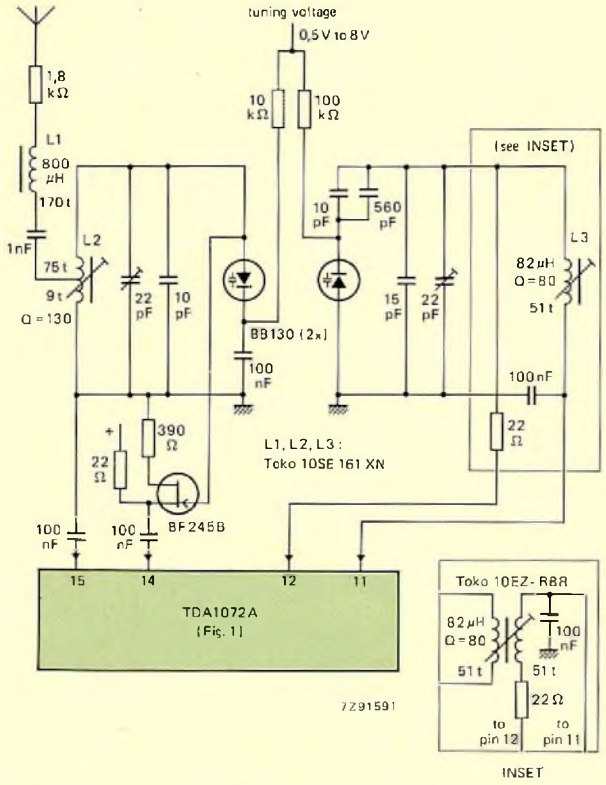


Fig.9 Aerial and local oscillator circuits for a varicap diode tuned medium-wave domestic radio. For high Q and aerial decoupling, a BF245B fet is used.

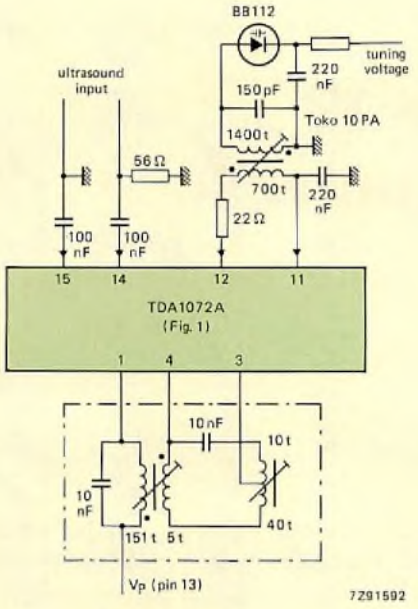


Fig.10 Receiver for 25 kHz to 35 kHz transmissions such as those used in Doppler rangefinders. The i.f. filter is tuned to 60 kHz. The IC oscillator is tuned by a varicap diode to between 25 and 35 kHz

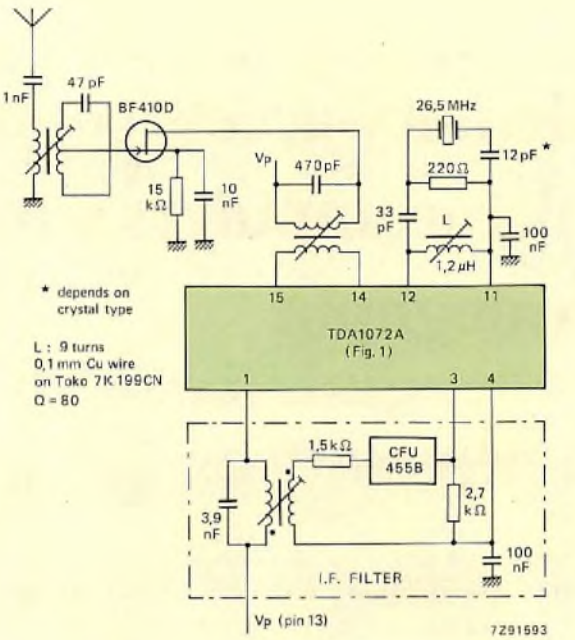


Fig.11 Aerial and local oscillator circuits for a 27 MHz receiver for remote control of garage doors, projectors, curtains etc. A crystal oscillator is used so that a narrow-band hybrid i.f. filter can be used

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Memory-access controllers give microcomputers a minicomputer's throughput

C. KAPLINSKI and M. FREEMAN

The 68010 and 68020 microprocessors should be able to match the throughput of a VAX minicomputer. In practice however, they may not live up to expectations, even when surrounded by an expensive boardful of components. But with a memory access controller (MAC) this situation is remedied. A MAC controls a hierarchy of memories – cache, local and main – and allows the processor to run without wait states even when using virtual addresses. While doing this, it provides a protection scheme to prevent illegal access to the memory hierarchy. A MAC also enables DMA controllers to use virtual addresses.

Our memory access controllers 68910 and 68920 combine memory management, a low-cost cache and access protection, to reduce wait states and bus traffic in multiprocessor systems. The 68910 is specifically designed for the 68010 16/32-bit microprocessor, and the 68920 is designed for the 32-bit 68020. Both MACs are fabricated in 2.5 μm HCMOS, containing over 90 000 transistors, and they are architecturally identical. However, the 84-pin 68910 has a 16-Mbyte address range (24-bit address), while the address range of the 120-pin 68920 matches the 68020's 4-Gbyte address space (32-bit address). A third chip, the 68905 with most of the 68920's features, will be available this year for software development.

In a multiprocessor system, there would be one MAC for every microprocessor, one of its jobs being to control that processor's external cache memory. The cache is made up of static RAMs and can be any size between 1 and 32 Kbytes.

The chip itself contains three main subsystems: a cache controller, a translation look-aside buffer (TLB), and a microcontroller (Fig.1). The cache controller provides all the matching and control logic needed to maintain an external static RAM as the data portion of the cache, while the translation look-aside buffer helps to translate a virtual address into its physical counterpart in main memory. These two subsystems in particular help the overall system performance. They allow write operations to overlap with subsequent read operations, and permit memory management and cache operations to overlap subsequent read operations. Also, memory management and cache operations can overlap as well. The third sub-section is the microcontroller that performs several tasks, among them updating the translation look-aside buffer.

The chip provides unusually flexible memory system control. It allows the designer to choose from a variety of virtual memory and memory protection schemes. The engineer can also create a multiprocessor system simply by adding processor-controller pairs and making minor changes to the operating system.

VIRTUAL MEMORY

The MAC's virtual-address space matches that of its associated processor. When the chip receives a virtual address, it checks the content-addressable memory in the cache controller to see if the address is in the cache. If it is and access to it is permitted, the MAC directs the cache contents to the microprocessor, along with the Data Acknowledge (DTACK) handshake the processor expects.

The translation look-aside buffer is accessed at the same time as the cache controller, but it activates the system only if the latter signals that the cache does not contain the desired information. In that case, if there is a matching physical address in the buffer's content-addressable memory and access is permitted, the physical address is presented to the system memory and a memory access is started.

If, on the other hand, the translation look-aside buffer does not contain the virtual-to-physical address map, it must get that map to complete the access. To do this, the chip's microcontroller asserts its Halt and Bus Error (BERR) signals to acquire the system bus from the processor. Then

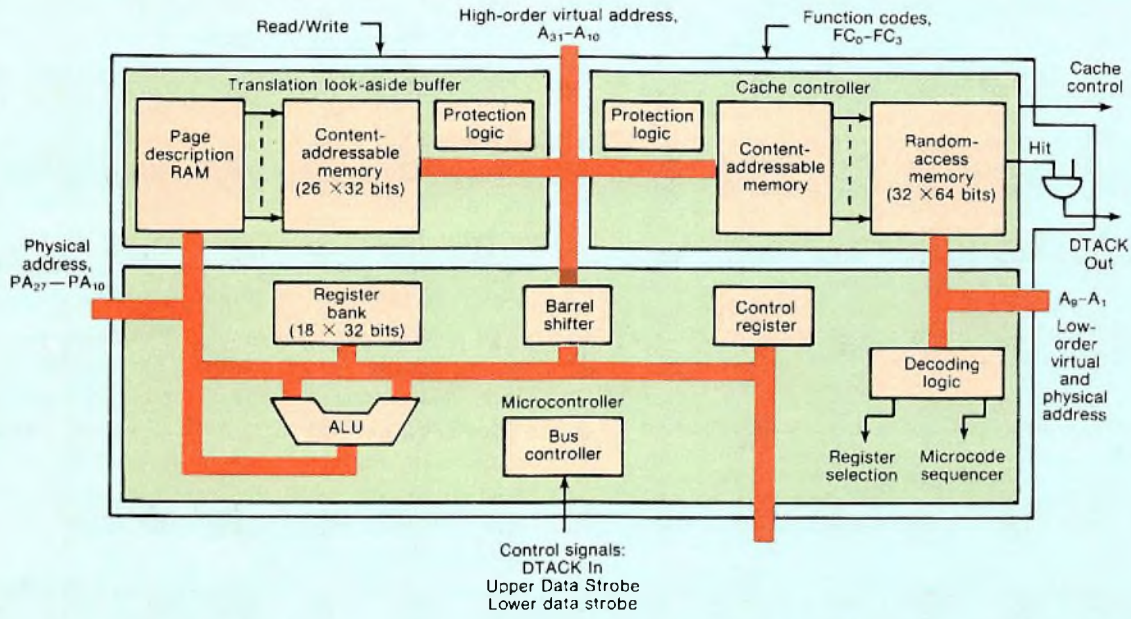

Fig.1 Three main subsystems make up the Memory Access Controller (MAC) IC. The cache controller contains matching and control logic to maintain an external static RAM cache. The translation look-aside buffer (TLB) helps translate virtual addresses into their physical counterpart, and the microcontroller performs numerous tasks, among them updating the TLB

the microcontroller fetches the necessary mapping information from the system memory and loads it into the translation look-aside buffer. With the mapping information on hand, the microcontroller returns the bus to the processor, which once more requests the original virtual address.

If no virtual-to-physical translation is possible (because the requested data is only on the disk), the processor is interrupted and forced to enter the operating system's memory management routine. This routine transfers the data from the disk into the RAM and, if necessary, moves blocks of data from the RAM to the disk to make space.

The need for a cache stems from the fact that processors are inherently faster than memories, a mismatch that keeps a processor from running as fast as it otherwise might. By creating a hierarchy of memories, however, a designer can minimize the time a processor spends waiting and thus take it closer to its theoretical performance maximum.

In such a hierarchy, the cache memory is closest to the processor. Consisting of a few fast static RAMs, the data portion of the cache is dynamically loaded with a copy of the contents of each processor memory reference, whether it be a program instruction or data. Typically, a 16-Kbyte cache satisfies up to 95% of all memory read requests.

However, very few microprocessor systems operate with a cache. Of those that do, most place the cache after the system's memory management unit (MMU) so that information is fed from the processor to the MMU and then in to the cache. Such systems waste at least one clock cycle in just translating the MMU addresses.

The MAC however, provides a faster alternative. With it, the cache and the MMU (actually the translation look-aside buffer) are accessed together, and the decision whether the cache contains the desired information is based solely on the virtual addresses. In addition, the cache controller checks access permission and thus can provide data from the cache without causing the processor to wait.

Moreover, in a multiprocessor environment, this unique architecture also speeds memory accesses. For example, since each processor uses the same virtual address for a different physical address, the cache must be flushed for a context change – a difficult and slow job to perform with standard logic and RAM.

The MAC however, marks all cache entries with the "region" to which they belong. On a context change, only those memory sections that are in the process-dependent regions are flushed. The controller does this automatically whenever its on-chip mapping information changes.

To avoid discrepancies, the cache must be updated when the processor writes to main memory. The controller employs a write-through method so that, as each write operation is performed, it is almost immediately written to the main memory. But if the cache contains that data word as well, it is also written into a cache location.

Since in a typical system at least 50% of the write operations are followed by a read access from the cache memory, the controller overlaps any write operations with the read accesses that follow. This action alone increases system throughput by about 6%.

A HIT OR MISS PROPOSITION

There are many ways to improve the performance of a single-processor cache-based system, but the most important is to improve the hit rate (how often a memory access is satisfied from the cache memory rather than the main memory). The higher the hit rate, the closer the processor comes to ideal performance.

Issues such as bus traffic are not important here, since I/O processing takes up only a small part of bus transfers. Moreover, by altering other factors — like decreasing the cache and main-memory-access times and minimizing the overhead of updating the cache — the designer can boost performance only so far. The most important factor affecting cache performance is the hit rate, and the key to that is a large cache block size.

The block size for the IBM 3084, for example, is 128 bytes. It achieves this by interleaving the main memory, using a wide data path between the main memory and the cache, and executing several memory transfers to fill a block. Although interleaving is not generally used in microprocessor buses, several transfers over the memory bus are feasible. In fact, the MAC supports such transfers with two techniques: multiple single access and sequential access.

In multiple single accesses, logic within the MAC arbitrates among the requests for the memory bus and fills the cache over several memory accesses. On the other hand, sequential access overlaps the next memory access with the transfer of the present access on the bus. The pipelining results in a memory access, which is followed by faster sequential accesses.

To gauge the effect of a high hit-rate on the performance of the 68010 in a single-microprocessor system, the designer can calculate the average number of clock cycles (wait states) that are added to the four in an ideal memory access. A typical address mix from a processor might consist of 85% read accesses and 15% write accesses. If it is assumed that all virtual-to-physical address translations are found in the translation look-aside buffer (that is, are available from the main memory), and if it is also assumed that each write operation updates main memory and that 50% of all write operations are overlapped with subsequent reads from the cache, a 95% hit rate yields an average total overhead of only 0,64 wait state.

The designer can derive this figure by summing the average wait states incurred by the four access possibilities: read hit, read miss, write overlap, and write miss. Read hits and write overlaps incur no wait states, but read and write misses do. Specifically, a read miss might incur 2 memory accesses to fill the cache (8 clock cycles) and a write miss might incur 1 memory access (4 clock cycles). Therefore the number of wait states = (85% read accesses x 5% read misses x 8 cycles per read miss) + (15% write access x 50% write misses x 4 cycles per write miss) = 0,64.

(Note that for the MACs, this calculation includes the time spent for memory management. In other systems, this can add a whole wait state to the average memory access).

For the 68010, an average of 0,64 wait state brings it to within 87% of its theoretical performance limit. Measurements show that the processor requires memory accesses on the average of every 4,33 cycles, leading to a performance given by 4,33/(4,33 + 0,64) = 0,87.

At this level of efficiency, a processor rated for a maximum of 1,23 MIPS (million instructions/s) would achieve a practical speed of 1,1 MIPs. Dropping the read hit rate to 90% adds an average of 0,94 wait states per cycle and reduces the practical speed to 1,0 MIPs.

In a multiprocessor system, the problem is harder to analyze, since increasing the block size (for a better hit rate) also results in a greater demand for the bus and the potential for additional delays.

A SECTOR-ASSOCIATIVE CACHE

The cache technique employed by the controller is called sector-associative. In this scheme, main memory is partitioned into equal-sized sectors, and the cache data RAM is partitioned into 32 sector-sized slots (Fig.2). Thus any main memory sector can occupy one of these 32 slots. However, since there are too many main memory sectors to fit each one into its own cache slot, the controller employs a mapping procedure using 32-position content-addressable memory (CAM) to identify those sectors in the cache.

To find out if a sector is in the cache, the controller first breaks any virtual address it receives into sector, block, and offset fields. If the sector field matches the contents of one of the CAM's positions, the requested sectors is in that position's corresponding cache slot. A cache hit occurs when the sought sector is found in the cache; a miss occurs when the sector is not found (see "A Hit or Miss Proposition").

Although sectors are normally large (1 Kbyte can be accommodated), filling 32-Kbyte cache one sector at a time is not at all practical. For that reason, sectors are partitioned into blocks made up of 2, 4, 8, or 16 bytes.

To address a block, the virtual address contains a block field. However, because not every block in a sector is necessarily in the cache, a group of presence bits is needed to say whether or not the address block is there.

If during a read operation, the presence bit for a requested block is not set, a block miss occurs, and the memory system controller accesses the main memory. In that case, the controller transfers the block into cache and sets the presence bit. The cache blocks are filled as a whole, and because a block can be wider than the system bus, the chip's cache controller sequentially accesses the system memory as needed to fill the block.

The advantages of a sector-associative cache, especially for an integrated circuit, are best appreciated when this approach is compared with the set-associated approach used in most other cache systems.

In a set-associative cache, there are usually one or two sets, implemented in separate RAMs. Each set is indexed by part of the desired address to yield an associated tag and data word. If any tag matches the most significant portion of the applied address, there is a cache hit and the data word goes to the requester. This organization is not practical for the MAC, partly because the time needed to complete the two-step process (accessing an external RAM for each set and comparing tags) is prohibitive and partly because it would be prohibitively expensive to integrate.

The sector-associative cache does not have this problem. The memory system controller compares address tags and almost simultaneously accesses block-presence bits indicating if a desired block within a sector is in the cache. Furthermore, when the controller is used, the external RAM contains only program and data values and no tags.

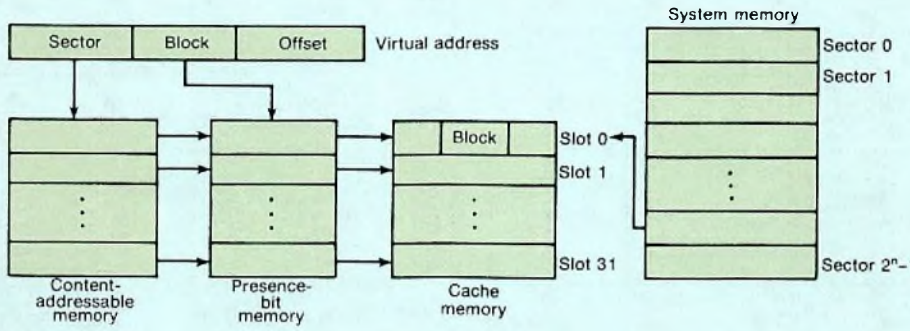

Fig.2 The controller uses a sector-associative cache technique to locate and retrieve memory blocks. To find out if a memory sector is stored in the cache, the chip breaks a virtual address into sector, block, and offset fields. Then its content-addressable memory indicates if the desired sector is in the cache memory, and the block field determines if the sector contains the desired block. If it does, the offset bit locates the exact byte sought

Since all control bits and tag-match logic are on the controller chip, the controller detects a match at the same time that the requested data is being accessed. In addition, a sector-associative cache is more cost-effective and more sparing in its use of chip area than the set-associative approach.

It turns out that the sector-associative cache is a good choice for multiprocessor systems as well. Recent studies show that sectors composed of many smaller cache blocks tend to place less demand on the memory bus than do other schemes.

Studies also show that with a 32-entry fully associative translation look-aside buffer, as found on the memory system controller chips, the hit rate is over 99% for a ½-Kbyte page size and 99,5% for a 4-Kbyte page. Also, the 32-entry translation look-aside buffer matches in size the 32-entry matching logic in the cache controller, and so both fit nicely on the chip.

VIRTUAL ADDRESSING

Besides its cache-controlling ability, the MAC acts as a memory management unit and offers a large, linear virtual-address space. The system designer is not restricted in the use of this space.

Three options are available. The first method, called segmentation, divides the address space into segments that are continuous in memory and allocated in multiples of a page size (Fig.3(a)). In this case, the designer can choose to have a segment length of between 128 Kbytes and 4 Gbytes for the 68920 and of between 8 Kbytes and 16 Mbytes for the 68910.

In the second approach, called paging, the address space is divided into pages of fixed sizes, with each page arranged to be 1, 2, 4, or 8 Kbytes long (Fig.3(b)).

The third method, called segmentation with paging, divides the address space into segments, but unlike the first method, the segments are not contiguous. Instead, the pages can be scattered throughout memory (Fig.3(c)).

In all these methods, mapping from a virtual address to a physical address uses the mapping table (in the content-addressable memory) of the chip's translation look-aside buffer. The buffer contains descriptors of the 32 most recently accessed pages. Each descriptor, in turn, indicates its associated subdivision's access rights, its ability to be cached, whether it has been written-to since cached, and other information (Fig.4).

In order to share code and data, the controller can partition a processor's virtual address space into as many as four regions. For security, or any other reason, the designer can assign an operating system kernel to one region, a subroutine library to another, and all code and data that is specific to a process to yet another region. In addition, access to any region, segment, page, or paged segment is based on a five-level protection scheme (See "A Policy of Protection").

Despite their separation, the contents of separate regions can still interact through entry points, a useful feature for sharing a library of function subroutines. In a typical Unix program, for example, there may be several references to such a library. In fact, a small program can increase its size several times when linked with library subroutines. In such cases, the system library region would avoid duplicating code for every linked program, and instead each subroutine entry point would be a fixed member of the virtual space of each program (Fig.5).

The controller determines the region number from the most significant 5 bits of the applied virtual address. This splits the virtual address into 32 pieces. These pieces are mapped into as many as four memory regions on the chip (a system designer may use only one or as many pieces as desired over a maximum of four regions). For example, a two-region system might have 12 pieces in region 0 and 20 pieces in region 1.

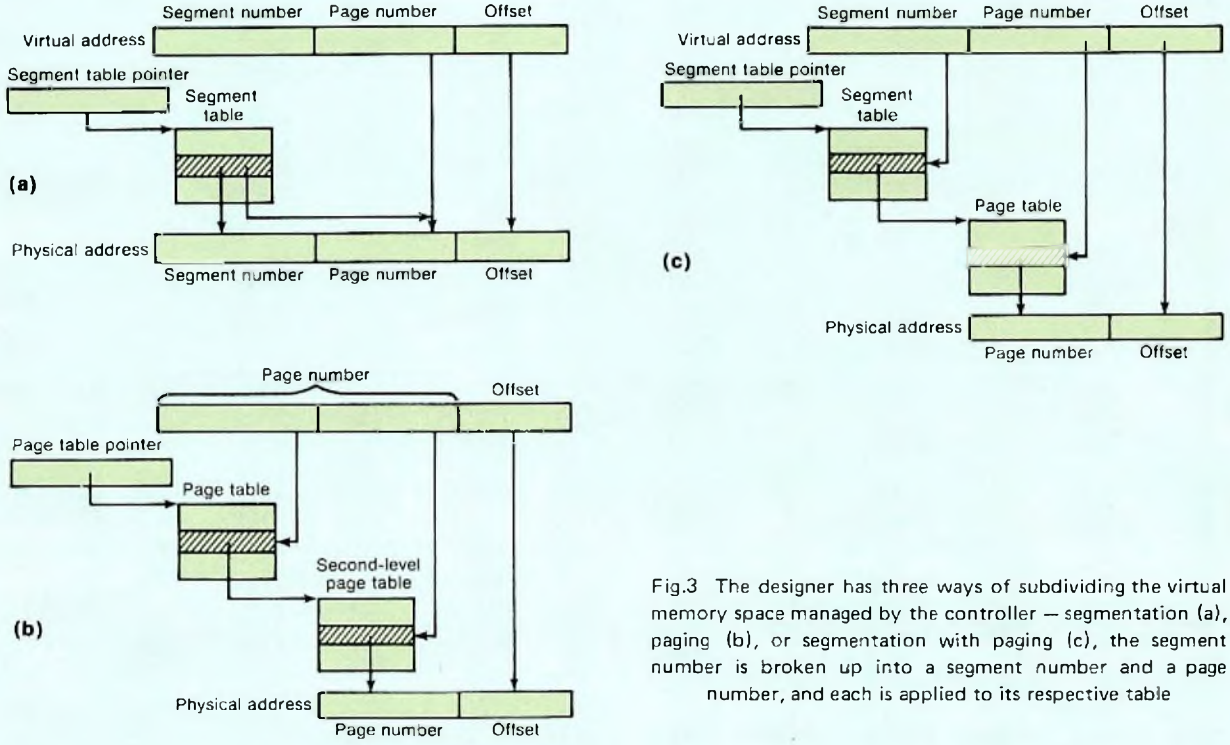

Fig.3 The designer has three ways of subdividing the virtual memory space managed by the controller — segmentation (a), paging (b), or segmentation with paging (c), the segment number is broken up into a segment number and a page number, and each is applied to its respective table

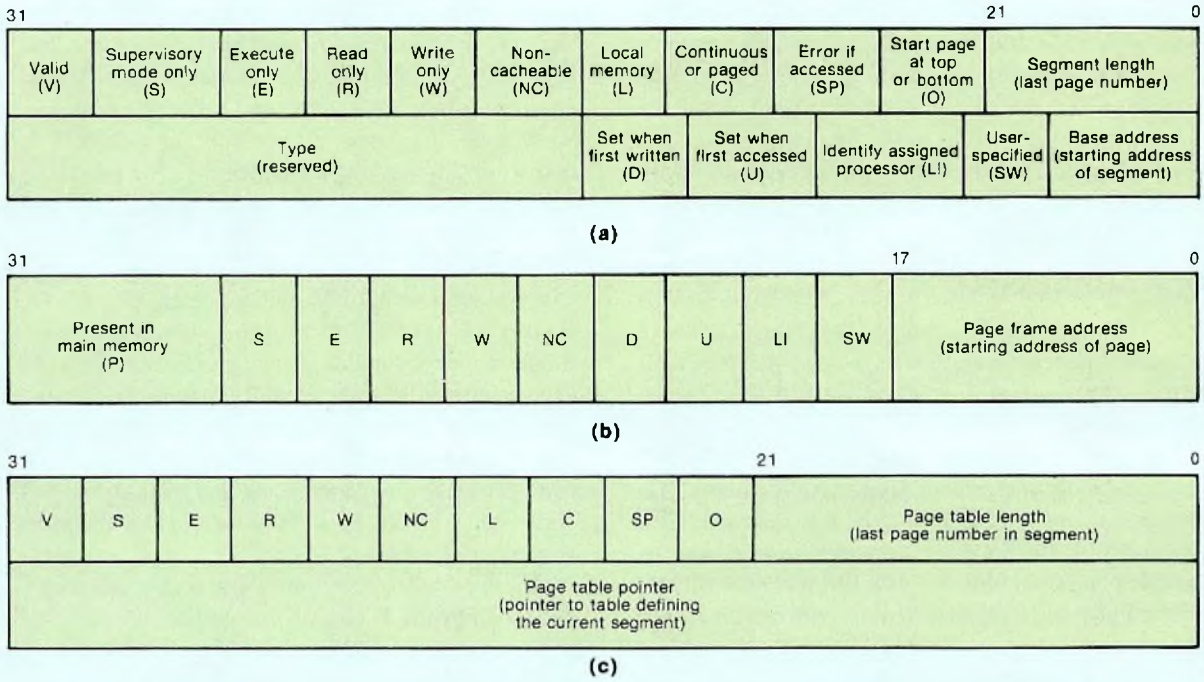

Fig.4 Each of the three virtual-memory mapping techniques stores one descriptive pointer (descriptor) in the transition look-aside buffer for each of the 32 most recently accessed segments (a), pages (b), or paged segments (c). A descriptor gives the subdivision's access level, whether or not it can be cached, if it has been written-to since cached, and other relevant information

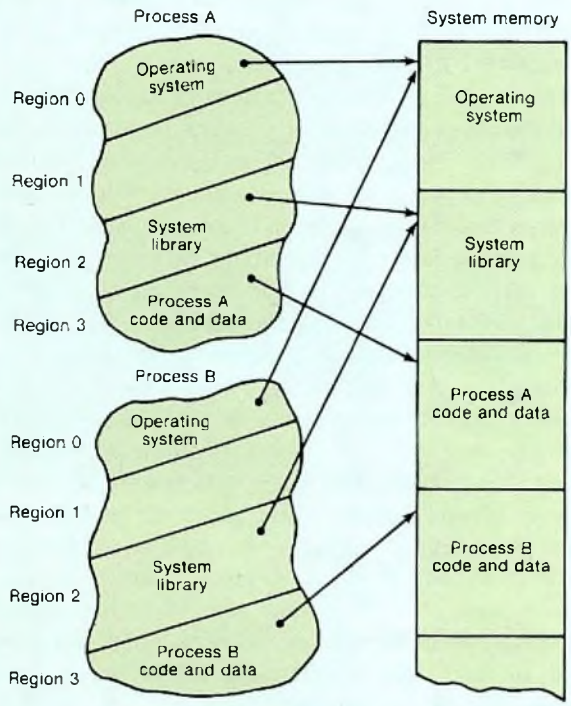

Fig.5 With the controller, the designer can divide the memory space into as many as four regions for sharing purposes. The same system subroutine library does not have to be copied into each processor's physical address space to keep unrelated sections of code from interfering with one another. However, entry points are available to permit interaction between the regions

In addition, to support the four regions, there are four register pairs on the MAC, each consisting of a segment-table pointer register (STPR) and a segment-table-length register (STLR). Each region also has an associated segment table or first-level page table. When the controller cannot find a virtual address in its cache or its translation look-aside buffer, it uses the registers to search the main memory descriptor tables.

The search first determines the region number of the virtual address, and the controller then accesses the pointer register of that region's associated segment table. In the case of a paged segment, the region's segment-table-length register determines the size of the segment. Then, using the segment field number from the virtual address as an index, the MAC accesses the segment table referred to by the segment table pointer register. In turn, the accessed segment descriptor contains the associated page table pointer and page length.

The controller then uses the page number field of the virtual address as an index to the page table to find the physical page-frame-address. It computes the physical address by linking the physical page-frame address with the offset field of the virtual address.

A POLICY OF PROTECTION

Memory protection — the ability to control access to any segment or page of memory — comes on five levels in a translation table on the MACs. Each segment or page of memory has several access permissions for each process. Permissions are accessible only in a processor's system state, executable (can run as a program), readable as data, or writable.

If a prohibited access is attempted — for example, if the processor tries to execute some nonexecutable code — the MAC does not complete the memory access. Instead it sends a Bus Error signal (BERR) to the processor, telling the operating system to take action.

All protection-setting bits apply at either the segment or the page subdivisions of a virtual-memory address space. In addition, the MAC can grant access at one level of a page table but prevent access at another level. This feature allows for operating systems that use a copy-on-write operation, in which, for example, two programs use the same physical memory area until one of the programs does a write to it. In this case, a bus error is generated, and the operating system makes a copy of the affected page.

However, the controller's protection ability extends beyond the permissions in the translation table. It permits a program's access through specific entry points to certain code and data, such as functional modules — in effect, dynamically extending the program. In turn, access to the extra code usually requires access to other data, and the controller provides for that, too.

For example, if a file system implements a set of four entry points — say, for reading, writing, opening, and closing files — the code to perform these actions needs access to system-wide tables that embody the state of the file system. The controller allows for this, and by using the entry points to restrict entrance to a section of code, it ensures the extra code is used only as intended.

In fact, the access scheme is similar to that of existing systems that divide the address space into a set of hierarchical concentric rings, where the radius of each ring is an address. In these systems, a program in any given ring has access only to the address space of its own ring and all the rings outside itself. Furthermore, ring crossings are controlled by gates that indicate the entry points to a ring as well as the more privileged rings to which entry is allowed.

The MAC, however, provides support for a scheme known as guarded regions, which need not be hierarchical but which can be any gate. In this scheme, a memory segment (marked in its descriptor as a gate segment) contains a list of gates, and each gate contains an allowed entry point, as well as pointers to additional information about the new context. This information consists of the segment table pointer register (STPR) and the segment table length register (STLR) of a new region definition. Thus, accessing routines through a gate involves redefining the contents of the virtual address space associated with a region. In this way, a new set of routines is made available because their memory addresses have been newly mapped.

The system designer defines the specific protection mechanism to be implemented by writing a small section of code that is run by the microprocessor and MAC under special guarded conditions. Moreover, because the MAC replaces a gate whenever a guarded region is entered, no check is required upon entry. The gate's availability to the program implies that the program had permission to use it. The use of guarded regions allows system designers to specify their own protection scheme — for example, rings or even, for the first time in a economical manner for a microprocessor, a capability-based scheme.

VIRTUAL I/O

As well as calculating physical addresses from virtual ones, the MAC can use virtual addresses of the I/O functions, and thus creates a "virtual" I/O. This is particularly important for paged virtual memory, where logically contiguous pages may not occur in consecutive locations. Without virtual I/O, disk operations, for one thing, would require complicated computations in software to read and write data that is across scattered pages. However, the controller solves this problem by allowing a DMA controller (for example, a disk controller to use virtual memory.

The I/O unit indicates with a function code bit designated FC_3 that it is performing an I/O rather than a processor memory reference. When FC_3 indicates that an address is an I/O reference, all protection checking is suspended and the remaining function code bits, FC_0 to FC_2, define which I/O controller is involved. It is necessary to define the I/O controller, because the MAC must report any errors caused by illegal accesses by an I/O unit, and FC_0-FC_2 identify the offending unit.

Because multiple I/O errors can occur before the processor can investigate the reason, a single error register in the controller is not enough. Instead, a communication area in main memory, indexed by the I/O address, is dedicated to writing I/O error messages (the portion of memory indexed by device 0 is reserved for the processor).

When an error occurs, the MAC writes an error message into the appropriate memory area. There the most significant bit of an error message field indicates whether it is a valid error message. The field also indicates the memory region and address at which the error occurred, as well as an error message number to identify the cause. In addition the MAC aborts a transfer with a BERR signal to the peripheral.

When an I/O controller receives the abort, it interrupts the processor, which in turn executes an interrupt service routine to identify the failure. This routine determines the I/O unit number and uses it as an index into the memory's communication area. There the routine searches for all valid error messages, processes them, and resets the most significant error bit.

CACHE ADVANTAGE

An important benefit of the controller is to lighten the load on the system bus, so that more processors can be added. In a typical 68000-based virtual memory system with a cache, a typical program will, on average, read on 85% of its memory accesses and write on 15%. Since about 90% of the read accesses will be satisfied by the cache memory, the system bus is lightly loaded.

In contrast, in a non-cache system, the processor must access the bus for every memory reference. But with the controller and a cache memory, this figure can be reduced to 23% of all references. This conclusion is derived from the following formula: percentage of bus accesses = read miss rate x percentage of read accesses + percentage of write accesses = 0,1 x 0.85 + 0,15 = 23%.

Thus, with a cache system, a designer can add a few processors without significantly reducing performance. Still, with ordinary memory controllers, a processor must wait if it tries to access a bus that is occupied. With the MAC, however, this is not a common occurrence, since (as noted earlier) it overlaps write operations with any read operations that are resolved by the cache memory. In fact, simulations show that using the MAC four processors can share a VMEbus without an appreciable decline in performance.

Multiprocessing makes demands on software as well as hardware, and here, too, the MAC distinguishes itself by letting the designer mark pages or segments of the main memory as non-cacheable. This capability is necessary when access to sections of software must be limited to one processor at a time. When the controller encounters such a page or segment, it places the page or segment mapping information in its translation-look-aside buffer, but it never places the page or segment in cache. Thus it prevents access by more than one processor at a time.

The controller offers a similar solution for acquiring semaphores – locations used to restrict access to a section of code to one processor at a time. Say a processor has a semaphore in its cache. If another processor attempts a semaphore action on the same semaphore, the semaphore values seen by both processors could be different. Ultimately this might result in a software crash. The MAC solves this problem by marking the semaphore itself as uncacheable.

Furthermore, marking a segment or page as uncacheable is also useful for I/O operations. For example, in an ordinary cached system that reads data from a UART (universal asynchronous receiver-transmitter), the data will end up in the caches as well as in the main memory. When the processor attempts to read successive characters, it will get stale data from the cache rather than updated characters from the UART. It is necessary therefore that all data areas for devices that can change state autonomously – I/O devices and coprocessors, for example – be marked as uncacheable.

If more than four processors are required in a design, the MAC uses a powerful multiprocessing scheme that adds a relatively small local memory to each processor (Fig.6). Whenever the processor accesses a page, the MAC will check to see if that page is in a local memory and specifically within the local memory of the requesting processor. If the page is in local memory, the access takes place unhindered. If it is not, however, the MAC sends a Bus Error signal to the processor, which then loads the local memory with the requested data. This is analogous to paging data from the disk to RAM, and it occurs unseen by the programmer.

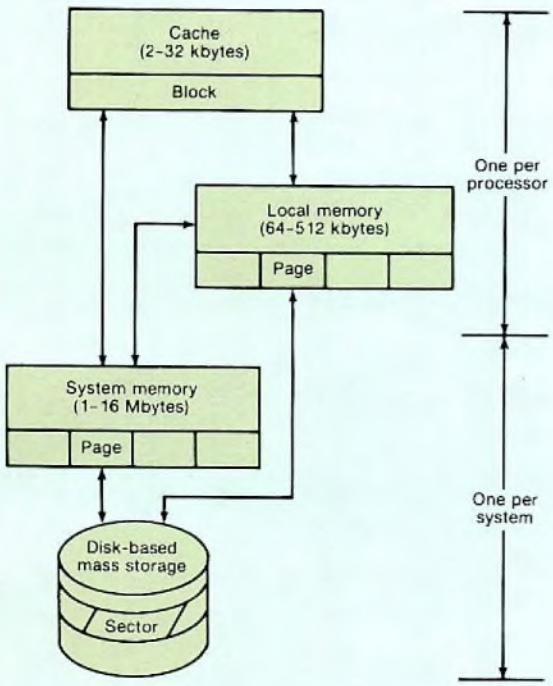

Fig.6 The controller supports a powerful multiprocessing scheme that adds a relatively small local memory to each processor. Use of the local memory for stack wiring, a large percentage of all writing operations, speeds the process and reduces the traffic on the bus

WHAT KIND OF DATA SHOULD THE DESIGNER PUT IN A LOCAL MEMORY?

An analysis of 68000 programs and VAX11/780 processor accesses for C programs shows that a large percentage of write operations are directed to the stack. Therefore placing the stack in a local memory would speed most write operations and reduce the bus traffic. In fact, simulations suggest that a local memory could free the bus enough to allow up to 10 processors to share it, and since stack sizes rarely exceed 4 Kbytes in depth, a local memory of four 64 K-by-4-bit RAMs would allow each 68010 microprocessor to handle 32 processes at once.

Before such a system could be used, however, the system's operating system would have to be altered. The compiler would need changing to mark stack segments as local. At the same time, the page-turning algorithm would have to account for the addition of the local memory to the hierarchy. Possibly, the schedular would have to be altered, since it prepares a table of dispatchable processes and, for optimal efficiency, should prepare a separate table for each processor. Finally, the dispatcher would require slight alterations to make it look first at its own list of dispatchable processes. Only when that list is empty will it look at the others.

ACKNOWLEDGEMENT

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Research news

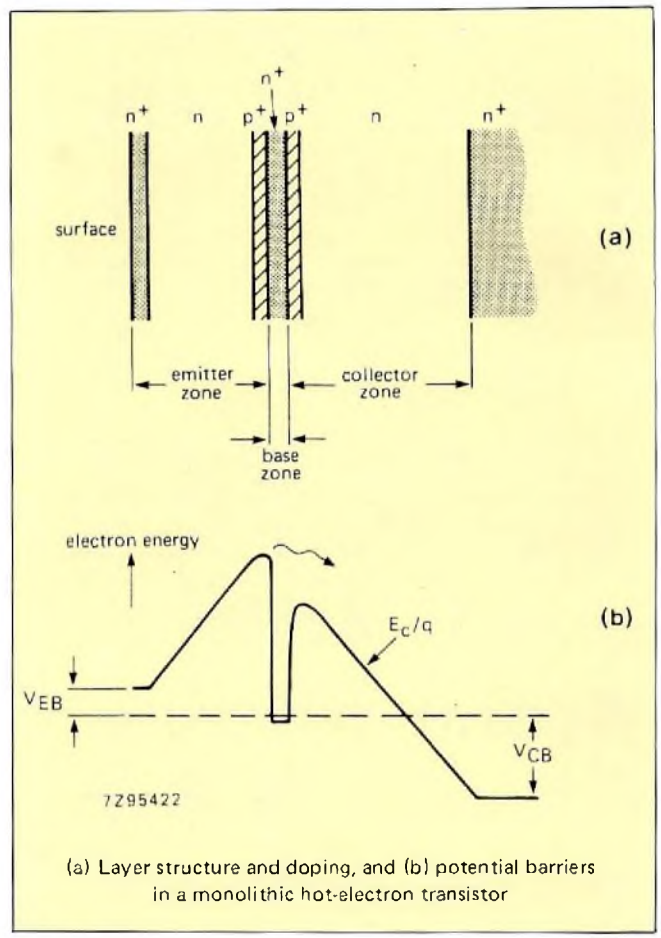
HOT ELECTRONS FOR EXTREMELY-HIGH-FREQUENCY TRANSISTORS

Recent work centred on hot electrons, which move faster than average in semiconductors, opens the prospect of manufacturing transistors with useful gain in the e.h.f. band.

Interest in hot electrons is not new. As long as twenty years ago attempts were made to obtain transistor action by injecting hot electrons from a Schottky barrier into a metal base; owing to very low collector efficiency, however, no amplification was realized. Invention of a new type of diode has now overcome that problem.

The 'bulk unipolar diode' developed at Philips Research Laboratories at Redhill, England, has an extremely fast response (>1000 GHz) and can function both as a highly efficient collector and emitter of hot electrons. In principle, two such diodes separated by a base zone should operate as a hot-electron transistor. A critical question, however, is whether, with a large enough separation to ensure low base resistance, a sufficient number of hot electrons to provide reasonable amplification can still be made to reach the collector.

Work at Redhill using molecular-bundle epitaxy and ion implantation has now demonstrated that it is indeed possible to transport hot electrons with good efficiency over practical distances. In both silicon and low-resistivity gallium arsenide hot electrons transported over several tens of nanometres have been collected with efficiencies up to 95%. This corresponds to twenty-fold amplification and opens the way to practical realization of monolithic hot-electron transistors (HMETs) capable of operating at frequencies in excess of 50 GHz.



(a) Layer structure and doping, and (b) potential barriers in a monolithic hot-electron transistor

Abstracts

Stand-alone speech development system using a personal computer

Much of the work associated with speech synthesis is generating the software for the synthesizer. Although manufacturers of speech synthesizers offer speech coding services, the speech coding is usually performed on a mainframe – expensive and time-consuming for the customer who must travel to the manufacturer. A new approach using a personal computer and a simple I/O device brings the analysis and editing to the customer. With the new system, synthesized speech is displayed on a VDU graphically, not as codes, so speech editing can be learnt in a day.

Quality – high-speed CMOS

Our range of HC/HCT/HCV high-speed CMOS (HCMOS) includes devices that are pin-compatible with many LSTTL and HE4000B CMOS circuits. They are produced using our proven Isolated Oxide technology, but with tighter layout rules (3 μm gate structures with thinner gate oxide). They share the latch-up immunity of our HE4000B CMOS, and the tight quality achieved by a zero defect-oriented organization. All our HCMOS devices incorporate a high degree of protection against electrostatic discharge damage. The 1985 target process-average reject level is 100 ppm. Life test results indicate a failure rate at 50 °C of less than 6 FITS (6×10^{-9}/h).

Datacomm peripherals for the 68000 microprocessor

A large family of single-chip datacomm peripherals is available for interfacing with the 68000 microprocessor. This article surveys these peripheral circuits which can implement a wide variety of software-selectable protocols. Because they perform much of the processing needed to interpret protocol rules, these circuits allow designers to meet protocol requirements easily. Several design examples are given.

Single-chip multi-standard colour decoder

In areas receiving tv transmissions to more than one colour standard, colour receivers are needed that can handle multistandard transmissions without additional manual switching. Two new single-chip multistandard colour decoders, the TDA4555 and TDA4556, fulfil this function by allowing automatic switching between PAL, NTSC and SECAM. The ICs differ only in the polarity of the colour-difference signals at their outputs. Identification and switching takes little more than half a second, and where signals are weak, noisy or badly distorted, the automatic standard recognition (ASR) can be switched off and the standard chosen manually.

RF ICs for portable communications equipment

Two r.f. ICs, the NE602 and NE604, that work at frequencies previously unattainable in low-power r.f. devices allow the design of receiver circuits that serve many of today's communications applications. With their low power consumption these ICs are ideal for use in cellular radio and other portable communication equipment.

Integrated a.m. receiver circuit

The TDA1072A is an integrated a.m. radio circuit that performs all the active functions between the aerial and the audio power amplifier. Its ability to handle a wide dynamic range of input signals and its low distortion make it suitable for use in a wide range of car radios, domestic radios and tuners. The circuit has been designed to meet present trends in the design of the a.m. section of a radio: varicap diode tuning, a.m. stereo facility and electronic search tuning. In addition, it features a VCO which provides signals of very low distortion and high spectral purity even when tuned with varicap diodes.

Memory-access controllers give microcomputers a minicomputer's throughput

The 68010 and 68020 microprocessors should be able to match the throughput of a VAX minicomputer, but in practice they don't live up to expectations. A MAC (memory access controller), however, such as the 68910 and 68920, can remedy this situation. They combine memory management, a low-cost cache and access protection, to reduce wait states and bus traffic in multiprocessor systems. The 68910 is specifically for the 68010 16/32-bit microprocessor and the 68920 for the 32-bit 68020. The MACs are architecturally identical and both are produced in 2.5 μm HCMOS.

Autarkes Spracheditiersystem mit Personalcomputer-Einsatz

Ein grosser Anteil der mit der Sprachsynthese verbundenen Arbeit besteht in der Generierung der Software für den Synthesizer. Obwohl die Hersteller von Sprachsynthesizern Sprachcodierdienste anbieten, sind diese meist teuer und zeitaufwendig für den Kunden, da sie gewöhlich auf einem Grossrechner abgewickelt werden. Ein neues System, das einen eingeführten Personalcomputer und eine einfache Ein-/Ausgabeeinheit verwendet, überträgt die Aktivitäten Sprachanalyse und Spracheditierung auf den Kunden. Hierbei wird die synthetisierte Sprache nicht in codierter, sondern in grafischer Form auf dem Datensichtgerät dargestellt. Die Spracheditierung ist daher in einem Tag vom Kunden erlernbar.

Qualität von High-speed CMOS-Schaltungen

Unser Lieferprogramm von HC/HCT/HCV-High-speed CMOS-(HCMOS-)Schaltungen enthält ICs, die mit vielen LSTTL- und HEF4000B-CMOS-Schaltungen pin-kompatibel sind. Sie werden in unserer bewährten Isolationsoxid-Technologie hergestellt, aber mit schärferen Anforderungen an das Layout (3-μm-Gatestrukturen mit dünnerem Gateoxid). Wie unsere HEF4000B-CMOS-Schaltungen sind sie unempfindlich gegen den Latch-up-Effekt und erfüllen ebenfalls unsere strengen Qualitätsanforderungen (Nullfehler-Programm). Unsere gesamten HCMOS-Schaltungen bieten einen hochgradigen Schutz gegen elektrostatische Aufladungen. Für 1985 besteht das Ziel, eine mittlere Rückweisungsquote von 100 ppm beim Herstellungsprozess zu erreichen. Bei 50 °C vorgenommene Lebensdauerprüfungen ergeben eine Fehlerquote von weniger als 6 FITS (6×10^{-9}/h).

Datenübertragungs-Peripherieschaltungen für den Mikroprozessor SCN 68000

Für den Betrieb am Mikroprozessor SCN 68000 steht eine grosse Familie von Einchip-Datenübertragungsschaltungen zur Verfügung. Dieser Beitrag befasst sich mit diesen Peripherieschaltungen, die ein breites Spektrum an über die Software wählbaren Übertragungsprotokollen abdecken. Da diese Schaltungen viele der zur Interpretierung der Protokoll-Regeln erforderlichen Datenverarbeitungsschritte intern ausführen, erlauben sie es dem Entwickler, Protokoll-Anforderungen mit geringem Aufwand zu erfüllen. Einige Applikationsbeispiele werden vorgestellt.

Einchip-Multistandard-Decoder

In Gebieten, in denen nach verschiedenen Farbfernseh-Standards ausgestrahlte Fernsehsendungen zu empfangen sind, benötigt man Farbfernsehgeräte, mit denen diese Sender möglichst ohne eine manuelle Umschaltung empfangen werden können. Zwei neue Einchip-Multistandard-Farbdecoder mit den Typenbezeichnungen TDA4555 und TDA4556 schalten automatisch zwischen den Standards PAL, SECAM, NTSC mit 3,579 MHz Farbträgerfrequenz und NTSC mit 4,434 MHz Farbträgerfrequenz um und erfüllen damit die gewünschte Funktion. Die beiden Schaltungen unterscheiden sich nur in der Polarität der Farbdifferenz-Ausgangssignale. Identifikation des jeweiligen Fernsehsignals und Umschaltung auf den entsprechenden Standard dauert im ungünstigsten Fall nur 520 ms. Bei schwachen, verrauschten oder stark gestörten Signalen lässt sich die automatische Umschaltung auf die einzelnen Standards ausschalten und die Wahl des Standards von Hand vornehmen.

Integrierte HF-Schaltungen für transportable Geräte zur Nachrichtenübermittlung

Die beiden integrierten HF-Schaltungen NE602 und NE604 können noch in einem Frequenzbereich eingesetzt werden, in dem bisher integrierte Kleinleistungs-HF-Stufen nicht mehr arbeiten. Die hier vorgestellten Schaltungen eignen sich daher für den Einsatz in zahlreichen heute vorkommenden Anwendungen zur Nachrichtenübermittlung. Wegen der geringen erforderlichen Versorgungsleistung sind diese integrierten Schaltungen prädestiniert für die Verwendung in tragbaren Funkgeräten und anderen Übertragungseinrichtungen, die in modularer Weise aufgebaut sind.

Die integrierte AM-Empfängerschaltung TDA1072A

Die integrierte AM-Empfängerschaltung TDA1072A enthält alle Stufen, die für die Signalverarbeitung zwischen Antenne und NF-Leistungsverstärker erforderlich sind. Durch den grossen dynamischen Eingangsspannungsbereich und die geringen auftretenden Signalverzerrungen ist die Schaltung besonders für den breiten Einsatz in Autoradios, Heimempfängern und Tunern geeignet. Der Schaltungsentwurf berücksichtigt die gegenwärtigen beim Bau von AM-Empfängern vorhandenen Trends: Varicap-Dioden-Abstimmung, AM-Stereo-Übertragung und Suchlauf-Abstimmung. Der amplitudengeregelte Oszillator sorgt für sehr niedrige Signalverzerrungen und eine hohe Spektralreinheit des Oszillatorsignals sogar dann, wenn die Abstimmung über Varicap-Dioden vorgenommen wird.

Mit Memory Access-Controllern erzielen Mikrocomputer den Datendurchsatz von Minicomputern

Die Mikroprozessoren SCN 68010 und SCC 68020 sollten in der Lage sein, den Datendurchsatz eines VAX-Minicomputers zu erreichen; in der Praxis entsprechen sie jedoch diesen Erwartungen nicht. Ein MAC (Memory Access Controller), wie der SCC 68910 oder SCC 68920, kann hier Abhilfe schaffen. Sie vereinigen in sich eine Memory Management Unit, einen kostengünstigen Cache-Speicher sowie Schutzschaltungen gegen unberechtigten Zugriff, um Wartezustände und Busverkehr in Multiprozessorsystemen zu reduzieren. Der SCC 68910 ist speziell für den 16/32-bit-Mikroprozessor SCN 68010 und der SCC 68920 für den 32-bit-Mikroprozessor SCC 68020 vorgesehen. Die Architektur der MACs ist identisch, und beide werden in 2,5-µm-HCMOS-Technologie hergestellt.

Ensemble de développement de vocabulaire à l'aide d'un ordinateur personnel

La synthèse de la parole nécessite essentiellement de générer le logiciel utilisé par le synthétiseur. Les fabricants de synthétiseurs vocaux proposent des services de codage de la parole effectués habituellement sur une unité centrale – opération longue et coûteuse pour le client qui doit se rendre chez le fabricant. Une nouvelle méthode, utilisant un ordinateur personnel de type courant et un dispositif d'entrée/sortie simple, permet d'effectuer le codage et l'édition chez le client. Avec ce système, la parole synthétisée est affichée sur un écran sous forme graphique et non sous forme codée, de sorte que le client peut apprendre en une journée à éditer son propre vocabulaire.

Des circuits CMOS rapides de haute qualité

Notre gamme de circuits CMOS rapides HC/HCT/HCV (HCMOS) comprend des dispositifs compatibles broche à broche avec de nombreux circuits TTL-LS et HE4000B. Ils sont réalisés en technologie à Oxyde Isolé, mais selon des règles de configuration plus strictes (structures de porte 3 µm avec oxyde de porte plus mince). Ils sont dotés de la même immunité au blocage que nos CMOS HE4000B et de la qualité rigoureuse obtenue par une organisation orientée vers l'absence totale de défauts. Tous nos circuits HCMOS jouissent d'une forte protection contre les décharges électrostatiques. Le taux moyen d'erreurs opérationnelles prévu pour 1985 est de 100 ppm. Des tests de durée de vie montrent que le taux de défaillance à 50 °C est inférieur à 6 FITS (6×10^{-9}/h).

Des circuits de communication de données pour le microprocesseur 68000

Une importante famille de circuits de communication de données à cristal unique est disponible pour l'interfaçage avec le microprocesseur 68000. L'article présente ces circuits périphériques capables de mettre en oeuvre des protocoles variés sélectionnables par logiciel. Comme ils effectuent une grande partie du traitement nécessaire pour interpréter les règles du protocole, ces circuits permettent au concepteur de répondre facilement aux besoins de ce dernier. Plusieurs exemples de réalisation sont donnés.

Décodeur couleur multistandard sur un seul cristal

Les régions recevant des émissions TV sur différents standards couleur ont besoin de téléviseurs capables de recevoir ces émissions sans commutation manuelle supplémentaire. Deux nouveaux décodeurs couleur multistandards à un seul cristal, le TDA4555 et le TDA4556, assurent la commutation automatique entre PAL, NTSC et SECAM. Ces circuits ne diffèrent que par la polarité des signaux de différence de couleur à leurs sorties. L'identification et la commutation ne prennent guère plus d'une demi-seconde et, dans les cas où les signaux sont faibles, bruyants ou fortement déformés, il est possible de couper la reconnaissance automatique des standards (ASR) et de choisir le standard manuellement.

Circuits intégrés radiofréquence pour matériels de communications portables

Deux circuits intégrés radiofréquence, le NE602 et le NE604, qui fonctionnent à des fréquences que ne pouvaient atteindre les dispositifs à basse puissance, permettent de réaliser des circuits récepteurs utilisables dans la plupart des applications actuelles de communications. La faible consommation de ces circuits intégrés les rend idéals pour les postes de radiophonie cellulaire et autres appareils de communications portables.

Circuit récepteur A.M. intégré

Le TDA1072A est un récepteur radio A.M. intégré qui réalise toutes les fonctions entre l'antenne et l'amplificateur de puissance audio. La gamme étendue des signaux dynamiques d'entrée qu'il peut capter et son faible taux de distorsion le rendent approprié aux autoradios, récepteurs domestiques et tuners. Le circuit a été réalisé selon la conception actuelle de la partie A.M. des récepteurs radio: accord par diode varicap, possibilité de stéréophonie en A.M. et recherche électronique; en outre, il est équipé d'un oscillateur commandé en tension et fournit des signaux à très faible distorsion et réponse spectrale parfaite même avec accord par diodes varicap.

Des contrôleurs d'accès mémoire donnent à des microcontrôleurs la capacité de traitement d'un miniordinateur

Les microprocesseurs 68010 et 68020 sont censés avoir une capacité de traitement équivalente à celle d'un miniordinateur VAX, mais, en pratique, il ne répondent pas à cette attente. On peut y remédier à l'aide de contrôleurs d'accès mémoire comme le 68910 et le 68920. Associant une gestion mémoire, une antémémoire peu coûteuse et une protection d'accès, ceux-ci réduisent les attentes et le trafic du bus dans les systèmes multiprocesseurs. Le 68910 est spécifiquement destiné au microprocesseur 68010 16/32 bits, le 68920 au 68020 32 bits. Les contrôleurs d'accès mémoire ont une architecture identique et tous deux sont réalisés en technologie HCMOS 2,5 µm.

Sistema de desarrollo de voz con ordenador personal

Muchos trabajos asociados con la síntesis de voz consisten en generar el programa para el sintetizador. Aunque los fabricantes de sintetizadores de voz ofrecen servicios de codificación de voz, usualmente la codificación de voz se realiza en un procesador central – caro y con pérdida de tiempo para el usuario que debe desplazarse al fabricante. Un nuevo método, que utiliza un ordenador personal sencillo y un dispositivo de E/S, realiza el análisis y la edición para el usuario. Con el nuevo sistema, la voz sistetizada se visualiza gráficamente en una pantalla, no como código, de modo que la edición de voz se puede conocer en un dia.

CMOS de gran velocidad y calidad

Nuestra gama de CMOS de alta velocidad HC/HCT/HCV (HCMOS) con incluye dispositivos terminales compatibles con muchos circuitos CMOS HEF4000B y LSTTL. Están fabricados con nuestra probada tecnología de óxido aislado pero con líneas impresas más delgadas (estructuras de puerta de 3 μm con óxido de puerta más delgada). Estos comparten la inmunidad de nuestros CMOS HE4000B, y la gran calidad lograda mediante una organización orientada a la perfección. Todos nuestros dispositivos incorporan un alto grado de protección frente a daños por descargas electrostáticas. El nivel de rechazo medio en 1985 es de 1000 p.p.m. Los resultados de pruebas de vida indican una tasa de fallos a 50°C inferior a 6 FITS (6×10^{-9}/h).

Periféricos del microprocesador 68000 para comunicación de datos

Se dispone de una gran familia de periféricos monochip para comunicación de datos, que se acoplan con el microprocesador 68000. Este artículo informa sobre estos circuitos periféricos que pueden introducir una amplia variedad de protocolos seleccionables por programa. Como estos circuitos llevan a cablo la mayoría del proceso necesario para interpretar las reglas del protocolo, permiten al diseñador encontrar fácilmente sus requerimientos. Se dan varios ejemplos de diseño.

Decodificador de color de normas multiples en un solo chip

En las zonas que reciben transmisiones de TV en más de una norma de color, los receptores de TVC necesitan manejar transmisiones de normas multiples sin conmutaciones manuales adicionales. Los dos decodificadores de color multi-estándar y monochip TDA 4555 y TDA 4556 cumplen esta función permitiendo la conmutación automática entre PAL, NTSC y SECAM. Ambos CI difieren solamente en la polaridad de las señales de diferencia de color de sus salidas. La identificación y la conmutación de se llevan a cabo en poco más de medio segundo, y si las señales son débiles, ruidosas o muy distorsionadas, el reconocimiento automático de norma (ASR) se desconecta y se elige manualmente.

Circuitos integrados para equipos portátiles de comunicaciones

Dos circuitos integrados de R.F., el NE 602 y NE 604, que trabajan a frecuencias que no se podían obtener anteriormente en dispositivos de R.F. de baja potencia, permiten el diseño de circuitos receptores adecuados para muchas aplicaciones actuales de comunicaciones. Con su bajo consumo, estos circuitos integrados son ideales para radio celular y otros equipos portátiles de comunicaciones.

Circuito receptor de A.M. integrado

El TDA1072A es un circuito integrado de radio A.M. que realiza todas la funciones activas entre la antena y el amplificador de potencia de audio. Su capacidad para manejar un amplio margen dinámico de señales de entrada y su baja distorsión lo hacen adecuado para usarlo en un amplio margen de autoradios, radios y sintonizadores. El circuito ha sido diseñado para cumplir las actuales tendencias en el diseño de la sección de A.M. de una radio: sintonía con diodo varicap, posibilidad de A.M. estéreo y búsqueda de sintonía eléctronica, y realiza un VCO que proporciona señales de muy baja distorsión y alta pureza espectral incluso cuando se sintoniza con diodos varicap.

Controladores de acceso a memoria para dar a los microordenadores la potencia de los miniordenadores

Los microprocesadores 68010 y 68020 pueden tener la capacidad de manejo de datos de un miniordenador VAX, pero en la práctica no satisfacen las previsiones. Sin embargo, un MAC (Controlador de acceso a memoria), como el 68910 y el 68920, pueden remediar esta situación: combinan la dirección de memoria, con una protección de acceso de bajo coste, para reducir estados de espera y tráfico del bus en sistemas de multiprocesadores. El 68910 es específico para el microprocesador 68010 de 16/32 bitios y el 68920 para el 68020 de 32 bitios. Estos MACS son estructuralmente idénticos y ambos están fabricados en HCMOS de 2,5 μm.

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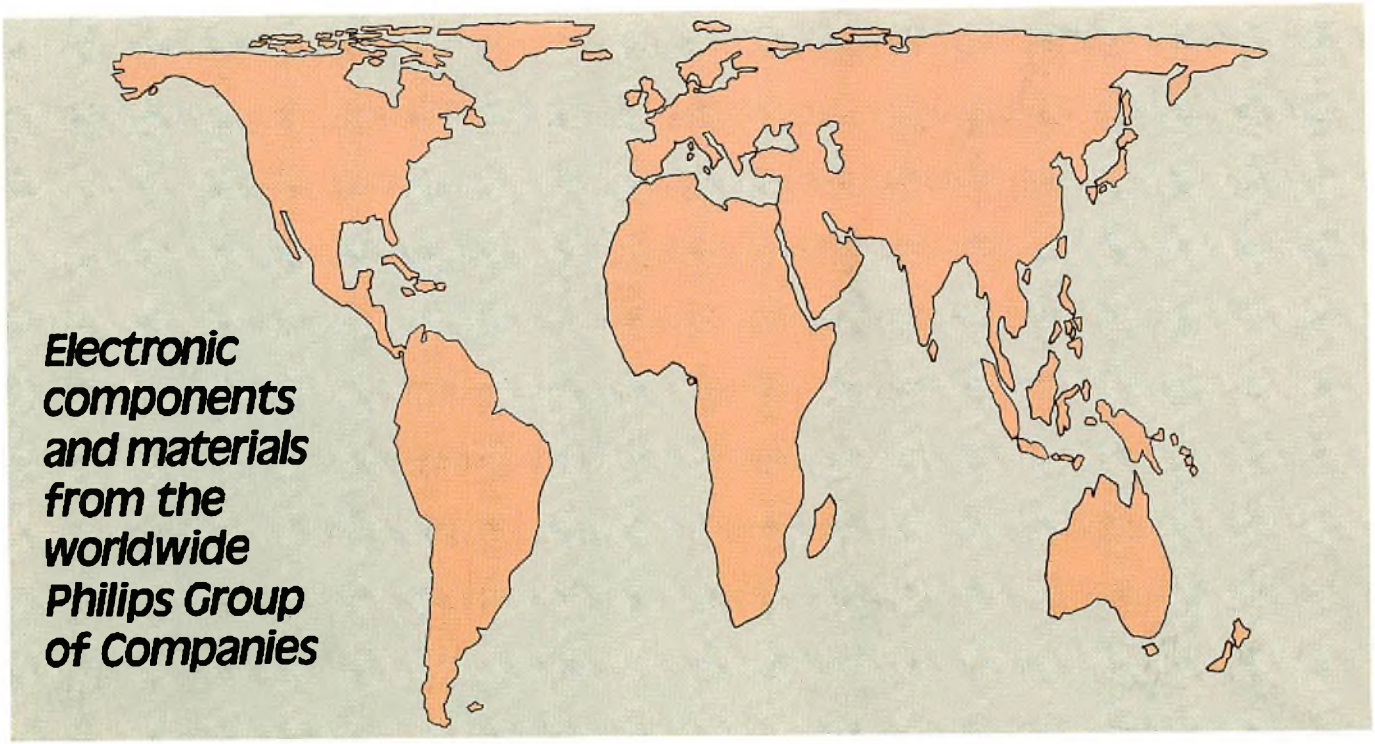

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