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Contents

In the age of solid-state the cathode-ray tube is still very much alive. Not only in its traditional role as measuring instrument but, even more so, as a display medium for the quantities of information that the advances of solid-state now put at our command. It may be that a successor is already waiting in the wings, but until it makes a decisive appearance the CRT is unlikely to step down. One article in this issue tells how to choose the right CRT to match particular display requirements; another describes a set of four LSI chips that dramatically reduce the parts count in CRT data and text display units.

Asymmetric silicon controlled rectifiers (ASCRs) block higher forward voltages and switch faster and with lower losses than conventional thyristors. This article describes their structure and manufacture, tells how to interpret their data, and illustrates their application in a single-phase inverter circuit.

Fast turn-off asymmetric silicon controlled rectifiers

F. BURGUM and A. WOODWORTH

Modern power switching applications require thyristors with high voltage-blocking capability, low losses, and fast switching performance. In practice these requirements are interrelated, and a particularly high specification with respect to one parameter can only be achieved by some loss of performance in one or both of the others. The Asymmetric Silicon Controlled Rectifier (ASCR) is a development of the conventional thyristor which allows a better trade-off between these conflicting requirements. In particular, for a given forward-blocking capability, losses can be reduced and operating frequencies increased. This improved specification is achieved at the expense of reverse-blocking capability. However, reverse blocking is a relatively minor aspect of thyristor performance, and in many applications it is unnecessary. If reverse voltage blocking is required, a diode must be connected in series with the ASCR. If reverse current must be allowed to flow, a diode must be connected in anti-parallel.

We are currently marketing two ASCRs: the BT155 and the BTW63. The BT155 has an average on-state current rating of 6.5 A (mounting-base temperature 85°C), and is encapsulated in a TO-220AB envelope. The corresponding average on-state current rating of the BTW63 is 22 A, with a TO-48 envelope being used for encapsulation. Both devices are available with turn-off times of 6, 9, or 12 μs. A suitable series/anti-parallel diode for use with the BT155 is the BYW19, while the BYV24 or BYW25 can be used with the BTW63. A more comprehensive description of the device data is given below, but before considering the performance of these devices in detail, it will be helpful to review the structural differences between ASCRs and conventional thyristors.

DEVICE STRUCTURE

Simplified cross-sections of a conventional thyristor and an ASCR are shown in Fig.1. In both devices the n^- regions are the wide high-resistivity bases; the n^+ regions are the cathode emitters, and the p^+ regions are the anode emitters. A p^+ region also forms the diffused base (gate contact region) of the conventional thyristor, while in the ASCR a p region forms the diffused base. The purpose of the n region in the ASCR is explained below. In a conventional thyristor forward- and reverse-blocking capability is obtained by the reverse biasing of junctions J_1 and J_2 respectively. The p^+ base and p^+ emitter diffusions of the conventional device are generally symmetric, being produced by a double-sided diffusion, with the result that forward- and reverse-blocking capabilities are very similar. Under forward- and reverse-blocking conditions, a depletion layer spreads across the n^- base, and the maximum blocking condition corresponds to the situation where this layer is just on the point of punching through to the opposite p^+ region. The value of the maximum blocking voltage is then given by the integral of the electric field intensity over the depletion layers; see Fig.2a.

For a given resistivity of the n^- base, it is clear that in a conventional thyristor a high blocking capability can only be obtained by having a wide n^- base. However, increasing the width of the n^- base will result in higher losses, since the on-state forward voltage drop will be increased, and the turn-on and turn-off times will be longer. In an ASCR the doping profile of the n^- base is modified so that high blocking capability can be combined with low losses. The n^- base is very lightly doped, giving an almost constant field intensity, and an additional n diffusion (the punch-through

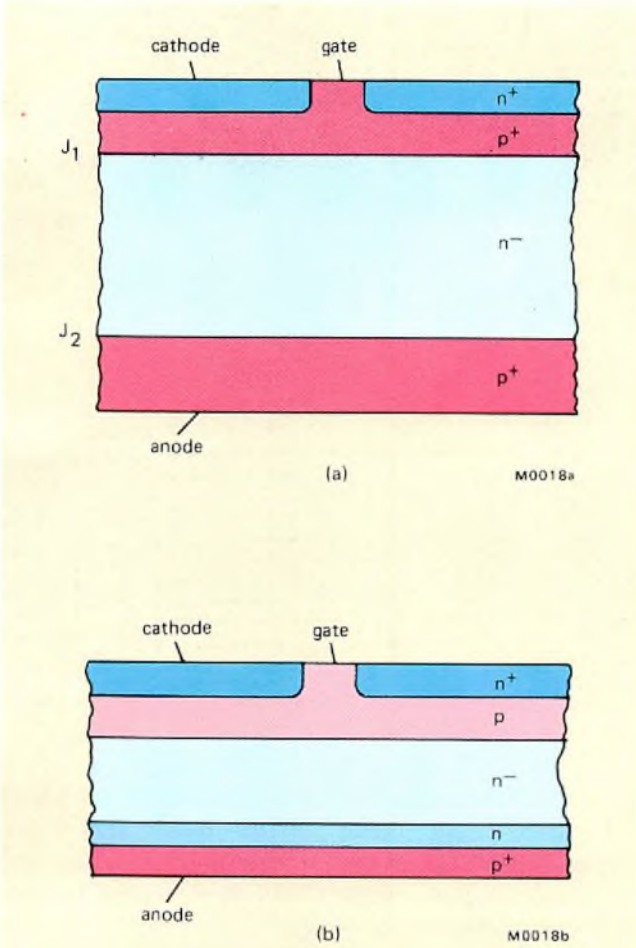


Fig.1 (a) Simplified cross-section of a conventional thyristor
(b) Simplified cross-section of an ASCR

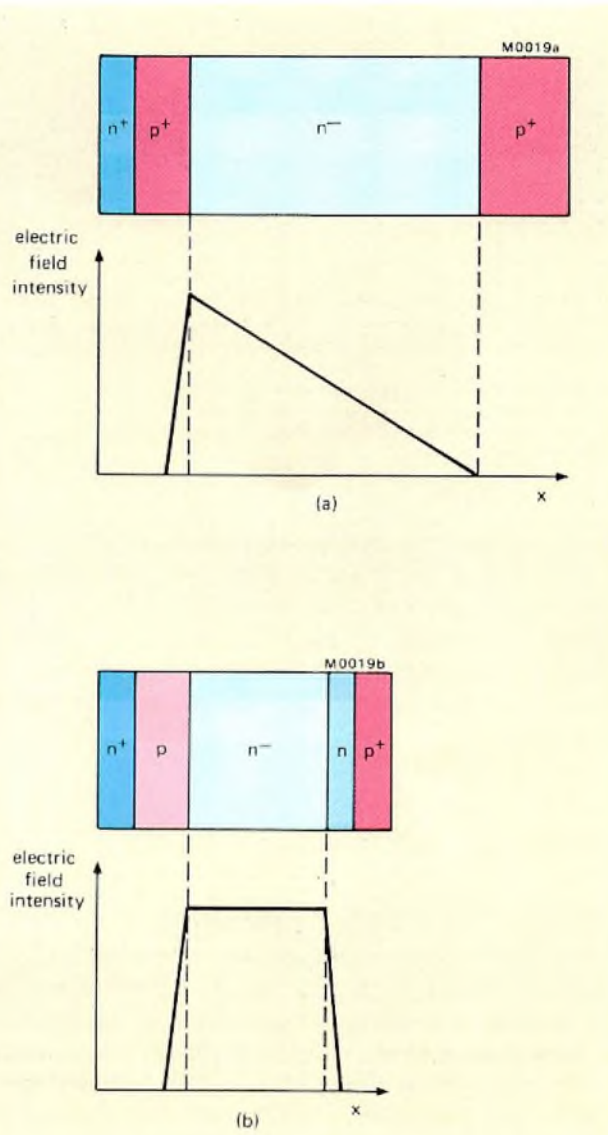


Fig.2 Variation of electric field intensity across depletion regions at maximum forward blocking voltage:
(a) conventional thyristor (b) ASCR
In both cases the value of the forward blocking voltage is proportional to the area under the curve of the field intensity

buffer) is introduced between the n^- base and the anode emitter; see Fig.1b. Although essential in ensuring a high forward-blocking capability, the introduction of the punch-through buffer results in an asymmetric device. High forward-blocking capability is thus achieved at the expense of reverse-blocking performance. The profile of the field intensity in an ASCR at the maximum forward-blocking condition is shown in Fig.2b.

Figures 2a and 2b have been drawn so that the areas under the curves of field intensity are the same, giving identical forward-blocking voltages. Although Fig.2 is a simplified representation, it does illustrate the scale of the reduction in the thickness of the n^- base in an ASCR. In practice, reductions of 40% are readily achieved.

While the relatively low loss characteristics of an ASCR are clearly desirable, still more important is the way in which these characteristics can be exploited to give a fast turn-off device. Thyristor turn-off times can be reduced by the introduction of gold into the n^- base, thereby reducing the average lifetime of the minority carriers. This gold-killing technique has the disadvantage of increasing the forward voltage drop in the on-state, and to a lesser extent gives a slower turn-on. The use of gold killing in a conventional thyristor is thus severely limited by the level of additional losses incurred. However, because the losses in an ASCR are inherently lower, a higher level of gold doping is possible and a faster device can be obtained. The very short turn-off times of the BT155 and the BTW63 are made possible by gold killing, and by the basic ASCR structure.

The device geometry of the BT155 and BTW63 is shown

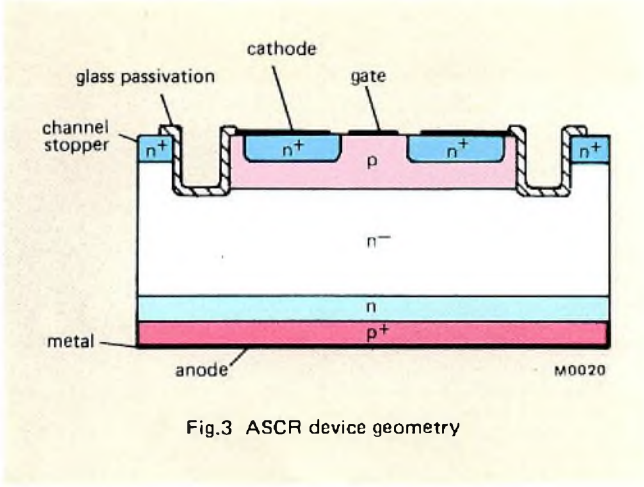


Fig.3 ASCR device geometry

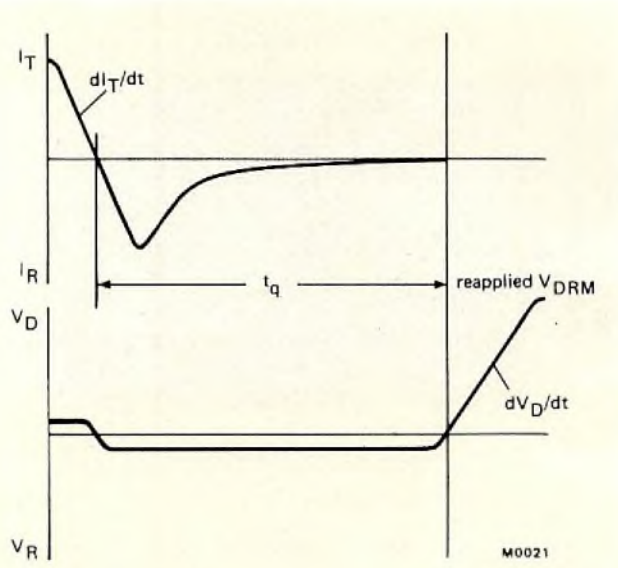


Fig.4 Definition of circuit-commutated turn-off time

in Fig.3. The doping level and diffusion depth of the punch-through buffer are critical in determining the device parameters, and ion implantation has been found to be an excellent means of obtaining consistent results. Reliable electrical performance is ensured by glass passivation of the forward-blocking junction and the use of an n^+ channel stopper.

DEVICE DATA

Ratings and switching characteristics

Table 1 gives details of the principal ratings and switching characteristics of the BT155 and the BTW63. The ratings are limiting values in accordance with the Absolute Maximum System (IEC134).

The measuring conditions for the turn-off times given in Table 1 are much more exacting than those used for previous generations of inverter-grade thyristors. The ASCR is turned-off from a high forward current, and a very small reverse voltage is applied during the turn-off time. Forward voltage is then reapplied at a high linear rate up to the repetitive peak off-state voltage V_{DRM}. These conditions reflect the operating requirements of fast inverters, and the values of turn-off time given in Table 1 can be confidently used in design calculations with the assurance that the circuit will be reliable. The definition of thyristor turn-off time is illustrated in Fig.4.

Losses

An assessment of the losses in an ASCR is an essential requirement in determining the appropriate heatsink. Losses are incurred in both the on- and the off-state. For low-frequency applications, the on-state losses are proportional to the product of the average on-state current and the on-state voltage. The total low-frequency losses, on-state plus off-state, can be determined from the left-hand section of the nomogram shown in Fig.5. At higher frequencies, or for current pulses with high peak values, turn-on switching losses become increasingly important, and the average on-state current is no longer an accurate guide to the level of the on-state losses.

The origin of turn-on losses is evident from Fig.6. For the first few microseconds after triggering, the voltage across the thyristor remains above the on-state voltage. Increasing the height of the current pulse, while reducing the pulse width to keep the value of the average on-state current unchanged, will result in an increasingly high proportion of the current pulse coinciding with the period of higher voltage, and the on-state losses will be correspondingly increased. It should be noted that because the anode current is externally commutated, equivalent additional losses are not incurred at turn-off. The on-state losses at high frequencies can be obtained by multiplying the total energy loss per pulse (the integral of $I \times V$ over the pulse width) by the number of pulses per second (the switching frequency). Details of the total energy loss per pulse for differing values of pulse width t_p and repetitive peak on-state current I_{TM} are given in Fig.7. As a rough guide, it is suggested that in the case of the BT155 on-state losses should be calculated via Fig.7 for pulse widths of less than 25 μs, while for the BTW63 Fig.7 should be used for pulse widths of less than 100 μs.

For a given mounting-base temperature, the maximum allowable losses are completely determined by the switching frequency, the pulse width, and the repetitive peak on-state current I_{TM}. The maximum allowable value of I_{TM} (corresponding to the maximum losses) is plotted as a function of

TABLE 1
Brief data for BT155 and BTW63

Ratings		BT155-600R	BT155-800R	BTW63-600R	BTW63-800R	
Repetitive peak off-state voltage	$V_{DRM\,max}$	600	800	600	800	V
Continuous off-state voltage	$V_{D\,max}$	500	650	500	650	V
Transient reverse voltage	$V_{RSM\,max}$	5		5		V
Average on-state current at mounting-base temperature = 85°C	$I_{T(AV)\,max}$	6.5		22		A
Repetitive peak on-state current: $t_p = 50\,\mu s$; $\delta < 0.05$	$I_{TRM\,max}$	90		250		A
Operating junction temperature	$T_{j\,max}$	110		125		°C
Thermal resistance						
From junction to mounting base	$R_{th\,j\text{-}mb}$	2.0		0.9		K/W
From mounting base to heatsink with heatsink compound	$R_{th\,mb\text{-}h}$	0.3		0.2		K/W
Characteristics						
On-state voltage: $I_T = 20$ A (BT155), $I_T = 50$ A (BTW63), $T_j = 25^o$ C	V_T	<2.65		<2.6		V
Off-state current: $V_D = V_{D\,max}$; $T_j = T_{j\,max}$	I_D	<1.5		<6.0		mA
Circuit-commutated turn-off time BT155 $-dI_T/dt = 30$ A/μs; $dV_D/dt = 500$ V/μs (linear to $V_{DRM\,max}$) $R_{GK} = 10\Omega$; $T_j = 110^o$ C; $V_G = 0$; switched from:						
$I_T = 30$ A and $t_p = 200\,\mu s$ (suffix K)	t_q	<6				μs
$I_T = 30$ A and $t_p = 200\,\mu s$ (suffix N)	t_q	<9				μs
$I_T = 90$ A and $t_p = 60\,\mu s$ (suffix P)	t_q	<12				μs
Circuit-commutated turn-off time BTW63 $-dI_T/dt = 50$ A/μs; $dV_D/dt = 500$ V/μs (linear to $V_{DRM\,max}$); $R_{GK} = 10\,\Omega$; $T_j = 125^o$ C; $V_G = 0$; switched from: $I_T = 100$ A; $t_p = 150\,\mu s$						
suffix K:	t_q			<6		μs
suffix N:	t_q			<9		μs
suffix P:	t_q			<12		μs

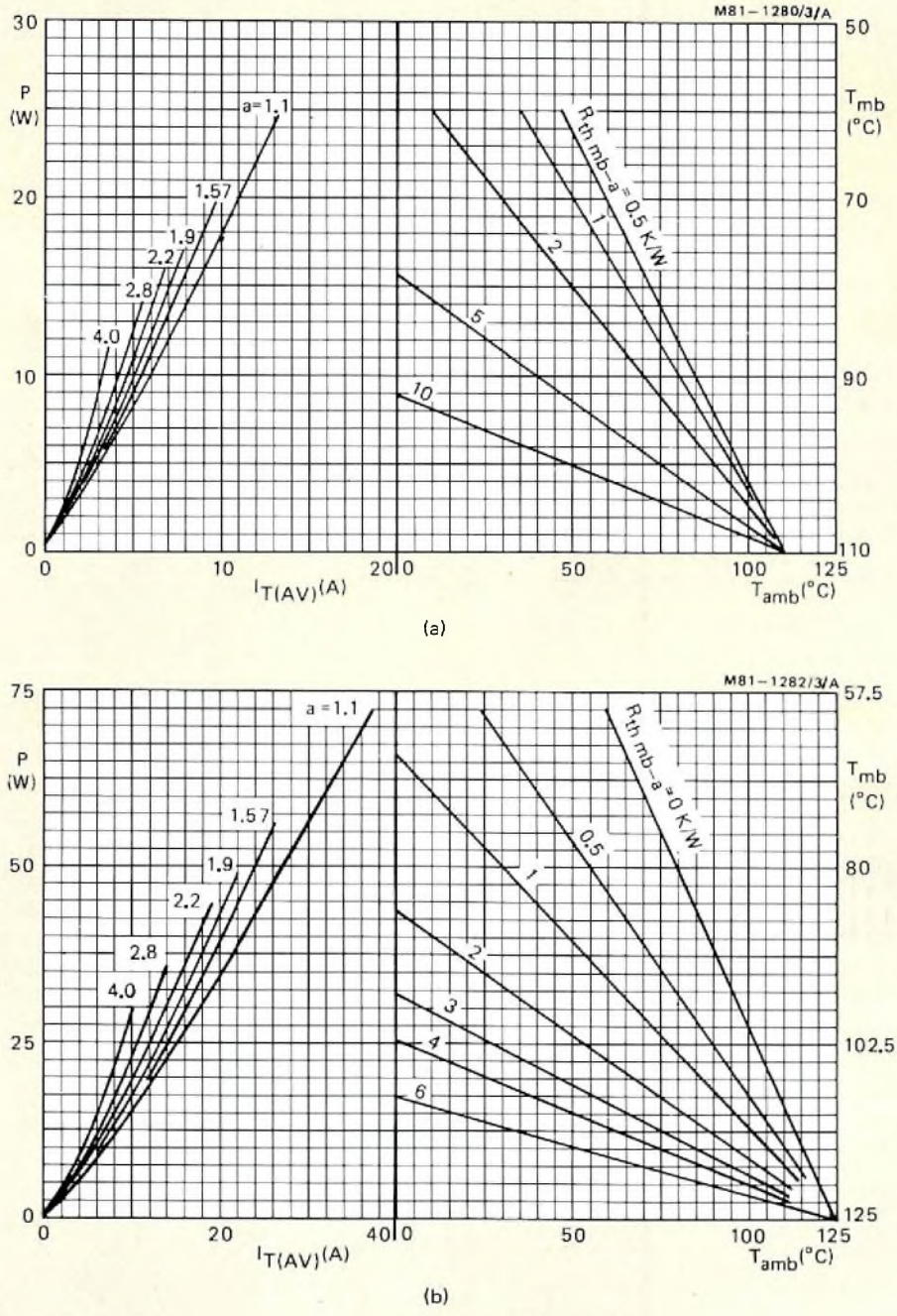


Fig.5 Nomogram for obtaining the appropriate value of thermal resistance between mounting base and ambient for a given value of average on-state current:

(a) BT155 (b) BTW63

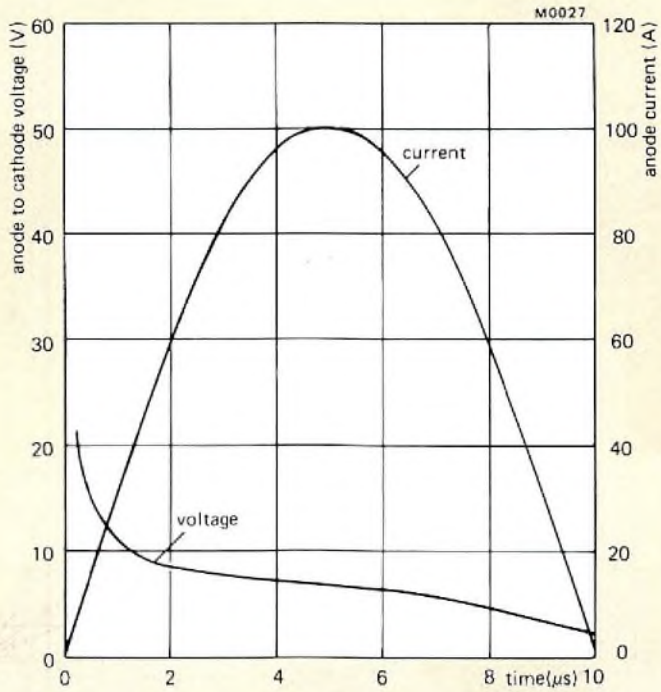
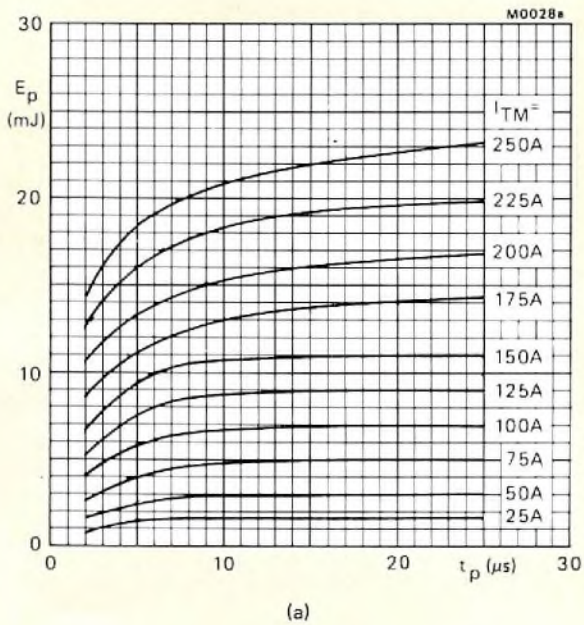


Fig.6 Typical turn-on characteristic for BTW63 illustrating origin of turn-on switching losses (I_{TM} = 100 A, t_p = 10 μs)



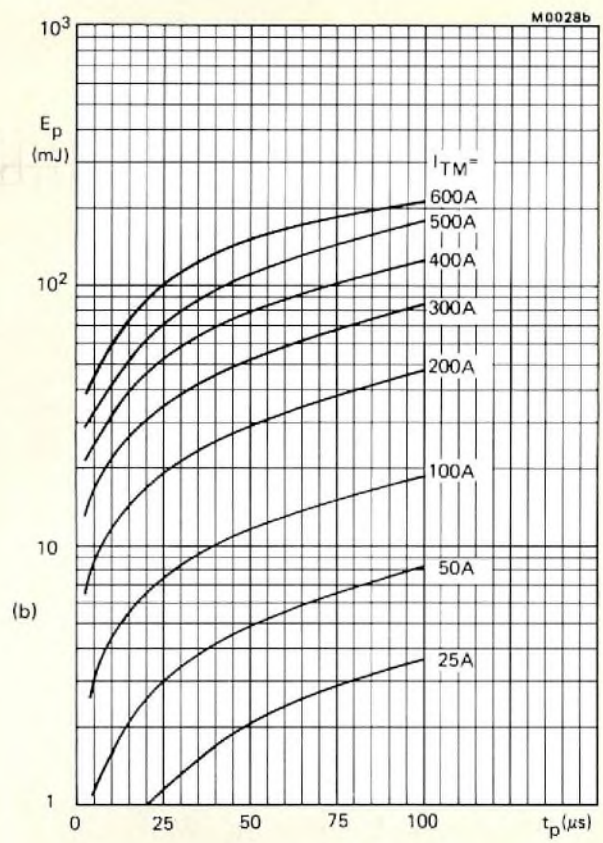
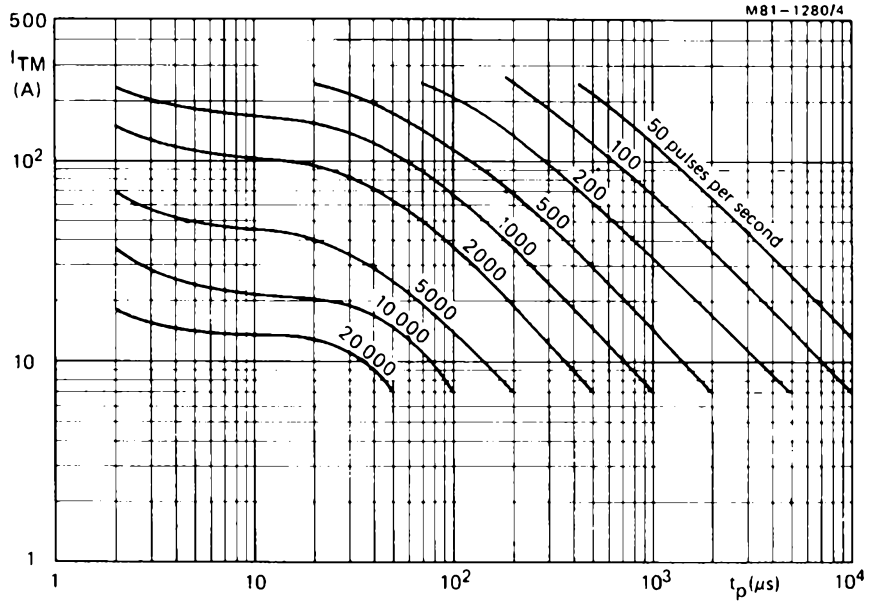


Fig.7 Maximum energy loss per pulse when switching a half-sinusoidal pulse from 600 V:
(a) BT155 (b) BTW63

(a)



(b)

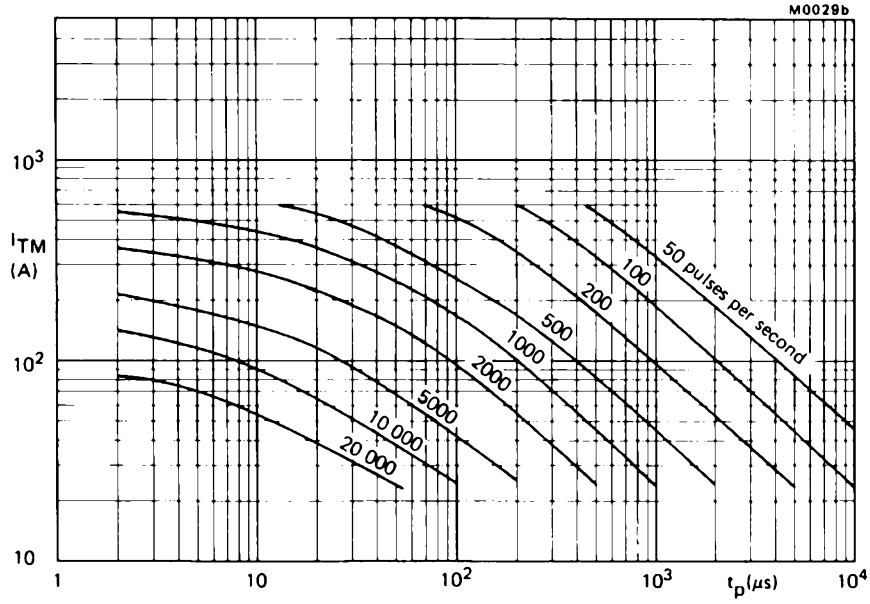


Fig.8 Maximum allowable repetitive peak on-state current against pulse width (T_{mb} = 85°C):

(a) BT155 (b) BTW63

pulse width and switching frequency in Fig.8. For a given application, Fig.8 provides a simple means of selecting the appropriate switching device.

DEVICE SELECTION

To illustrate the use of the device data for the BT155 and BTW63, the selection of ASCRs for a PWM inverter is now described. The particular inverter design under consideration was developed for our PWM a.c. motor speed control system; a general introduction to this system is given in Ref.1.

A single phase of the inverter is shown in Fig.9. The circuit contains four thyristors: two main thyristors Th1 and Th2 which chop the rectified mains, and two commutation thyristors Th3 and Th4 which force-commutate Th1 and Th2. The motor current is conducted alternately via Th1 and the flywheel diode D2, or via Th2 and D1. The anti-parallel connection of the main thyristor-diode combination (for example, Th1 and D2) permits the use of

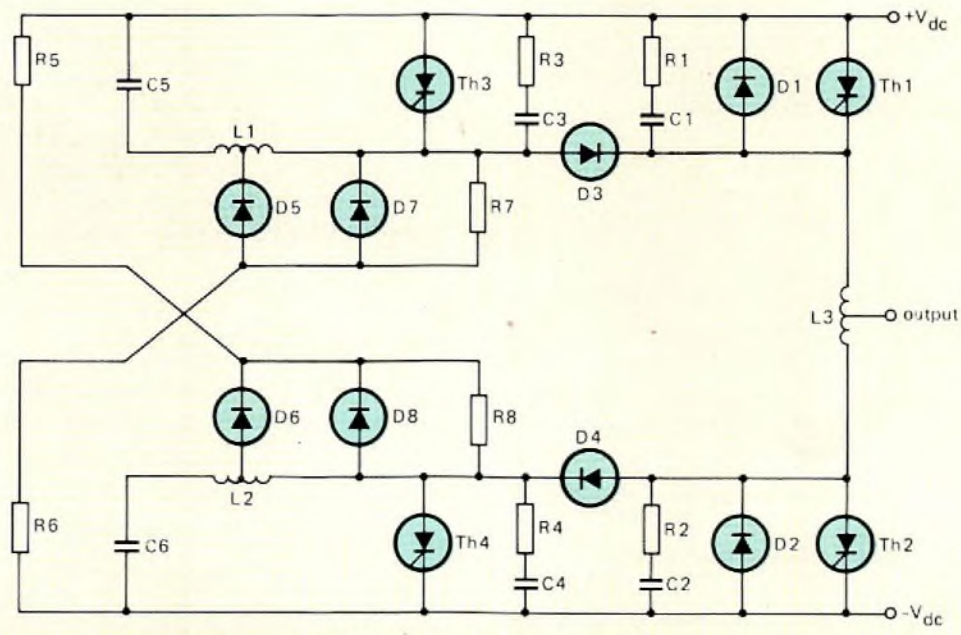


Fig. 9 Single phase of PWM inverter

ASCRs as switching elements. A complete description of the inverter design, including an explanation of the design equations, is given in Ref.2.

In the following example it is assumed that the inverter is being used to control a 4 kW 380 V motor with up to 50% overload.

Input data

Assuming European three-phase mains, 380 V ± 10%, then after rectification the minimum d.c. supply voltage is:

$$V_{dc(min)} = 462 \text{ V},$$

the nominal d.c. voltage is:

$$V_{dc(nom)} = 513 \text{ V},$$

and the maximum d.c. voltage (during regenerative braking) is assumed to be:

$$V_{dc(max)} = 750 \text{ V}.$$

The maximum line current $I_{m(max)}$ for a 4 kW 380 V motor varies between manufacturers, but may be taken to be 14 A at maximum overload. The maximum inverter switching frequency $f_{s(max)}$ is assumed to be 1 kHz, and the ambient temperature T_{amb} is assumed to be 50° C.

Selection of main thyristor

A safe design figure for V_{DRM} is given by:

$$V_{DRM} = V_{dc(max)} + 50,$$
$$= 800 \text{ V}.$$

Assuming that the worst-case thyristor current is approximated by a half-wave rectified sinewave then:

$$I_{T(AV)} = I_{m(max)} \times \frac{\sqrt{2}}{\pi}$$
$$= 6.3 \text{ A}.$$

It is advantageous to have a short turn-off time, although this must be balanced against the high unit cost of the faster device and increased snubber dissipation. The BT155-800RN, with a 9 μs turn-off time, is a good thyristor for this application.

Selection of commutation thyristor

Assuming a motor current ripple factor of 1.4, the peak inverter output current $I_{o(pk)}$ is given by:

$$I_{o(pk)} = I_{m(max)} \times 1.4 \times \sqrt{2},$$
$$= 27.7 \text{ A}.$$

It can be shown that an approximate value of the repetitive peak on-state current for the commutation thyristor is:

$$I_{TM} = 2.0 \times I_{o(pk)} \times \frac{V_{dc(max)}}{V_{dc(min)}},$$
$$= 90 \text{ A}.$$

A more accurate calculation can be performed when the commutation components have been selected; see Ref.2.

The width of the commutation current pulse is about twice the turn-off time of the main thyristor, that is 18 μs. Referring to Fig.8a, the maximum allowable value of I_{TM} for an 18 μs pulse at 1 kHz is over 150 A. A BT155 type is

thus a suitable choice for the commutation thyristor. The allowable turn-off time of the commutation thyristor can be up to one and a half times that of the main thyristor, or 13.5 μs. A BT155-800RP should therefore be used.

Heatsink selection

Main thyristor

For the purpose of heatsink selection, the current through the main thyristor may be approximated by a low-frequency half-wave rectified sinewave. Figure 5 will thus provide a reasonably accurate determination of the total power dissipated by the main thyristor. We have $I_{T(AV)}$ = 6.3A, and the form factor for a half-wave rectified sinewave is 1.57, so that from the left-hand section of Fig.5a, the power dissipated is 12 W.

For these losses, at an ambient temperature of 50°C, the required thermal resistance between the mounting base and ambient is about 3 K/W; see Fig.5a. From Table 1 the thermal resistance between mounting base and heatsink is 0.3 K/W, so that the required thermal resistance of the heatsink is 3 − 0.3 = 2.7 K/W.

Commutation thyristor

Under nominal conditions the commutation current pulse is a half-sinewave pulse of height $V_{dc(nom)}\sqrt{(C5/L1)}$, and width $\pi\sqrt{(C5L1)}$. Using the approach illustrated in Ref.2, suitable values of C5 and L1 can be calculated as 0.65 μF and 48 μH respectively. The commutation pulse height is thus 59.7 A, and the pulse width is 17.5 μs.

From Fig.7a, the average energy loss per pulse is approximately 4 mJ. For a switching frequency of 1 kHz, this corresponds to a rate of power dissipation of 4 W. The off-state losses can be found from the leakage current (1.5 mA from Table 1) and the off-state voltage, which may be taken to be $V_{dc(nom)}$ or 513 V. The off-state losses are thus $1.5 \times 10^{-3} \times 513 = 0.77$ W, giving a total power dissipation of about 4.8 W. Using the same approach as that adopted for the main thyristor, the required thermal resistance of the commutation thyristor heatsink can be determined as 9.7 K/W.

FURTHER APPLICATIONS

Although developed primarily for PWM power inverters, the BT155 and BTW63 are suitable for any application that requires a fast power switch. Additional areas of application include:

- uninterruptable power supplies
- medium-to-high power switched-mode power supplies
- magnetron power supplies for microwave ovens
- domestic induction cookers
- general-purpose high-frequency inverters (up to 20 kHz)

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2. BURGUM, F. and NIJHOF, E.B.G., 'Inverter circuit for PWM motor speed control system', Electronic Components and Applications, Vol.2. No.3, May 1980. pp.130 to 142.

Our comprehensive range of ICs for hi-fi radios and tuners allows the same combination of circuits to be used to obtain the required performance standard for a number of different applications. Three radios are described: an economy version, a high-performance version, and a luxury microcomputer-controlled version.

Integrated circuits for hi-fi radios and tuners

W. KANOW and I. SIEWERT

During the last decade, there has been intensive competition between electronic equipment manufacturers to meet the diverse requirements of the hi-fi stereo radio/audio market. This has resulted in the development of a diversity of units with widely varying performance, facilities, combination of functions and styling. Reduced manufacturing costs and increased reliability of this equipment are the direct result of widespread use of ICs which are now available for performing most of the active circuit functions. The use of ICs has allowed the introduction of more appealing styling, slimmer cabinets, micro-towers and microcomputer-control.

Obviously, the performance of the ICs must meet the standards laid down for hi-fi sound reproduction. To minimise manufacturing costs, they must also permit sufficient design flexibility to allow the same combination of ICs to be used in all classes of equipment without incurring the penalty of partial circuit redundancy. To minimise the number of discrete components required, a systems approach must be followed during the design of the ICs. These considerations form the basis of the philosophy behind our comprehensive range of hi-fi radio/audio ICs shown in Fig.1. For the f.m. part of the tuner we have one IC for the mixer, another for the i.f. amplifier and quadrature demodulator, and a third for the PLL stereo decoder. The a.m. channel is entirely contained within one IC. There is a choice of two ICs for providing a stabilised tuning voltage for variable-capacitance-diode tuning systems. For audio preamplifiers, there are three source-selectors/active filters and three circuits for d.c. control of tone, volume and balance. Additional ICs allow the economical construction of power output stages, motor control systems, electronic pointers and microcomputer-controlled radios with a host of additional facilities including remote control.

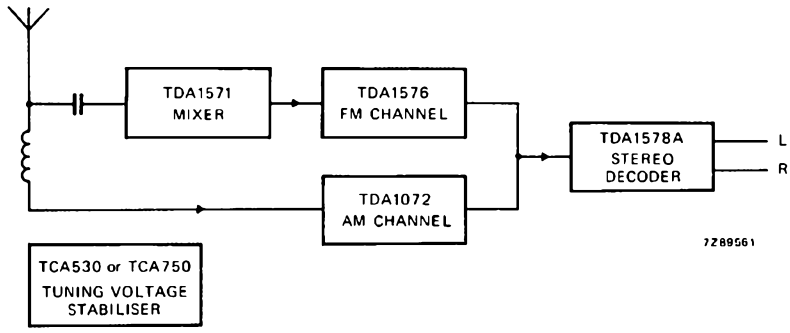
Since so many circuits cannot be adequately discussed in one issue of EC & A, this article only shows how our ICs can be used in the h.f. section of hi-fi radios, tuners and music centres. Three circuits using the same combination of ICs are presented; an economy circuit, a top-performance circuit and, based on the latter, a microcomputer-controlled hi-fi tuner with frequency synthesiser, search tuning, digital frequency display and remote control.

REQUIREMENTS FOR HI-FI RADIOS

There are basic requirements that every hi-fi radio must meet. Part of these is conformance with objective national and international hi-fi standards and regulations such as DIN45500, IEC268, IEC581, Amtsblatt 69 and the requirements of the FTZ. For example, the i.f. amplifier in the f.m. channel must have a good limiting characteristic so that there is a constant input level to the demodulator over a wide range of aerial voltages. This limiting removes noise and suppresses a.m. that would otherwise be heard in the recovered stereo sound.

A hi-fi radio must also pass critical subjective (listening) tests. For example, careful attention must be paid to the muting of hiss caused by rapid changes of signal strength, and to suppression of interstation noise and edge-of-station 'plop' that occurs when tuning in the f.m. band. These points are particularly important because the audio output from a hi-fi tuner is amplified to a level of up to several hundred watts and the listener would find the highly-amplified interstation noises intolerable. In our hi-fi f.m. radio ICs, particular attention is given to the elimination of these noises by using a very effective muting system which is controlled by both signal strength and the output from an innovative noise and detuning detector. This is the first multi-

BIPOLAR CIRCUITS FOR THE H.F. SECTION



OTHER BIPOLAR CIRCUITS

Pick-up amplifiers

NE542	dual op-amp for RIAA equaliser
NE5533	dual op-amp for RIAA equaliser

DC-controlled audio functions

TDA1028	dual, 2-input stereo source selector for mono/stereo switch and filters
TDA1029	4-input stereo source selector
TDA1527	single, 2-input stereo source selector for mono/stereo switch and filters
TCA730A	stereo volume and balance control
TCA740A	stereo treble and bass control
TDA1074A	dual stereo potentiometer for volume + balance or treble + bass

Audio power ICs and hybrids

TDA1512	7 W rms into 8 ohms @ d_{tot} = 0.05 % or 15 W rms into 4 ohms @ d_{tot} = 0.05 %
OM931	30 W rms into 4 or 8 ohms @ d_{tot} = 0.02 %
OM961	60 W rms into 4 or 8 ohms @ d_{tot} = 0.02 %

Electronic pointers

TDA1569	6 LEDs
TDA1594	11 LEDS

for signal strength and tuning displays

PLL motor speed control

TDA1533	for turntables, cassette recorders and reel-to-reel recorders

Remote control

TDB2033	gain-controlled remote IR receiver amplifier

Frequency synthesiser

SAA1057	radio tuning PLL frequency synthesiser

Display drivers

SAA1060	32 segment LED
SAA1062	20 static outputs for LCD

MOS CIRCUITS

Display drivers

PCE2100	40 segment LCD
PCE2110	60 segment LCD + 2 LEDs
PCE2111	64 segment LCD

in duplex mode

SAA1061	16 static outputs for LED drive and switching functions

Single-chip 8-bit microcomputers

MAB8021	with 1K byte ROM and 28-pin package
MAB8048	with 1K byte ROM and 40-pin package
MAB84XX	NMOS family with 0.5 to 4 kbyte ROM and I^2C bus
MAB85XX	CMOS family with 0.5 to 4K byte ROM and I^2C bus

Memories

PCD8571	128 x 8-bit CMOS memory with serial I/O
PCB1400	100 x 16-bit EEPROM with serial I/O

Clock/timer

SAB3019	clock/timer with serial I/O

Remote-control receivers

SAB3023	receiver and analogue memory
SAB3033	receiver and analogue memory
SAB3042	receiver and decoder with C-bus
SAB3028	receiver and decoder with I^2C bus

Remote-control transmitters

SAB3021	2 x 64 commands
SAB3027	32 x 64 commands

Fig.1 Our range of ICs for hi-fi radios and tuners

path muting system which also very effectively suppresses noise between strong, closely-spaced signals, even in difficult f.m. reception areas where critical aerial installations must be used.

Hi-fi sound can only be reproduced from radio transmissions in the f.m. band. To cater for areas with insufficient f.m. coverage, hi-fi radios and tuners often incorporate an a.m. channel which can receive transmissions from a greater distance. The a.m. channel must have high input sensitivity and a wide dynamic range so that weak signals can be received with as little noise as possible. Cross modulation of weak signals by adjacent strong signals must be minimised. These requirements are met by our single-chip totally integrated a.m. channel which requires very few additional components to be used to build an a.m. section with electronic (variable-capacitance diode) or mechanical tuning.

General requirements for hi-fi radios and tuners

- Insensitivity to mains voltage fluctuations and hum.
- Suppression of the i.f. image and 2nd and 3rd (a.m.) or 9th and 10th (f.m.) harmonics of the i.f. to prevent whistles ('tweets').
- Rejection of aerial signals within the a.m. and f.m. i.f. passbands.
- Simple switching between the a.m. and f.m. channels.
- Simple extraction and feedback-free connection of the local-oscillator signals for driving frequency displays and synthesisers in electronic tuning systems.

Requirements for the a.m. channel

- High input sensitivity and wide dynamic range.
- Low distortion from aerial input to audio output.
- Wide a.g.c. range.
- Prevention of cross-modulation of weak signals by strong adjacent signals.

Requirements for the f.m. channel

- A high signal-to-noise ratio and low distortion from aerial input to audio output.
- Low noise and high suppression of a.m. in the i.f. amplifier. This demands low-level limiting so that the drive voltage to the demodulator remains constant over a wide range of aerial input voltages starting from a level of about 1 μV.
- An audio output level of at least 0.5 V from the stereo decoder when the f.m. deviation is 40 kHz.
- Stereo channel separation of at least 40 dB at 1 kHz.
- The transition from mono to stereo (channel separation) must be smoothly controlled as a function of signal strength.
- Low cross-modulation between the pilot signal and audio signals.
- A signal strength indication voltage, which remains logarithmic over several decades of aerial input voltage, must be available from the i.f. amplifier.
- A noise muting system which is controlled by signal strength, noise and detuning.
- An a.f.c. system that can be switched off during tuning.
- A simple method of superimposing a.f.c. on the tuning voltage for radios and tuners without a PLL frequency synthesiser.

The integrated circuits shown in Fig.1 meet all of these requirements and permit sufficient design flexibility for the same combination of ICs to be used in economy sets or in high-performance hi-fi radios and tuners which can be either manually operated or microcomputer-controlled. The different standards of small-signal performance for these two categories are obtained by variation of the peripheral circuitry. All of the radios described in this article therefore consist of a basic hi-fi radio circuit into which appropriate f.m. front-ends, filters, and selectivity blocks can be inserted to obtain the required performance.

THE STANDARD PART OF THE HI-FI RADIO CIRCUIT

The standard part of the hi-fi radio circuit is shown in Fig.2. It contains an f.m. i.f. amplifier and demodulator TDA1576, a PLL stereo decoder TDA1578A and an a.m. channel TDA1072. The components for the f.m. i.f. preamplifier, f.m. demodulator 90° phase-shift network, MPX filter, stereo decoder PLL filter and pilot tone filter blocks in Fig.2 vary for the economy and high-performance versions of the radio and will therefore be separately described later.

F.M. i.f. amplifier and demodulator

The i.f. output from the f.m. front-end is coupled to the i.f. amplifier and quadrature f.m. demodulator TDA1576 via a discrete component i.f. preamplifier and a ceramic filter. The i.f. preamplifier ensures good a.m. suppression, even during the reception of weak signals and compensates for the insertion loss of the ceramic filter. The completely integrated four-stage symmetrical limiting i.f. amplifier in the TDA1576 has an input sensitivity of 22 μV at 3 dB before limiting and a signal-to-noise ratio of 90 dB ($\Delta f = \pm 75$ kHz, de-emphasis = 50 μs) with an input of 1 mV. The a.m. suppression is 50 dB ($\Delta f = \pm 22.5$ kHz, m = 0.3, f_{mod} = 1 kHz) over most of the i.f. amplifier input signal range. The i.f. amplifier is followed by a muting attenuator (not used in hi-fi radios) and a quadrature demodulator which is entirely integrated except for the 90° phase-shift network. The radio generates much less noise during tuning and the recep-

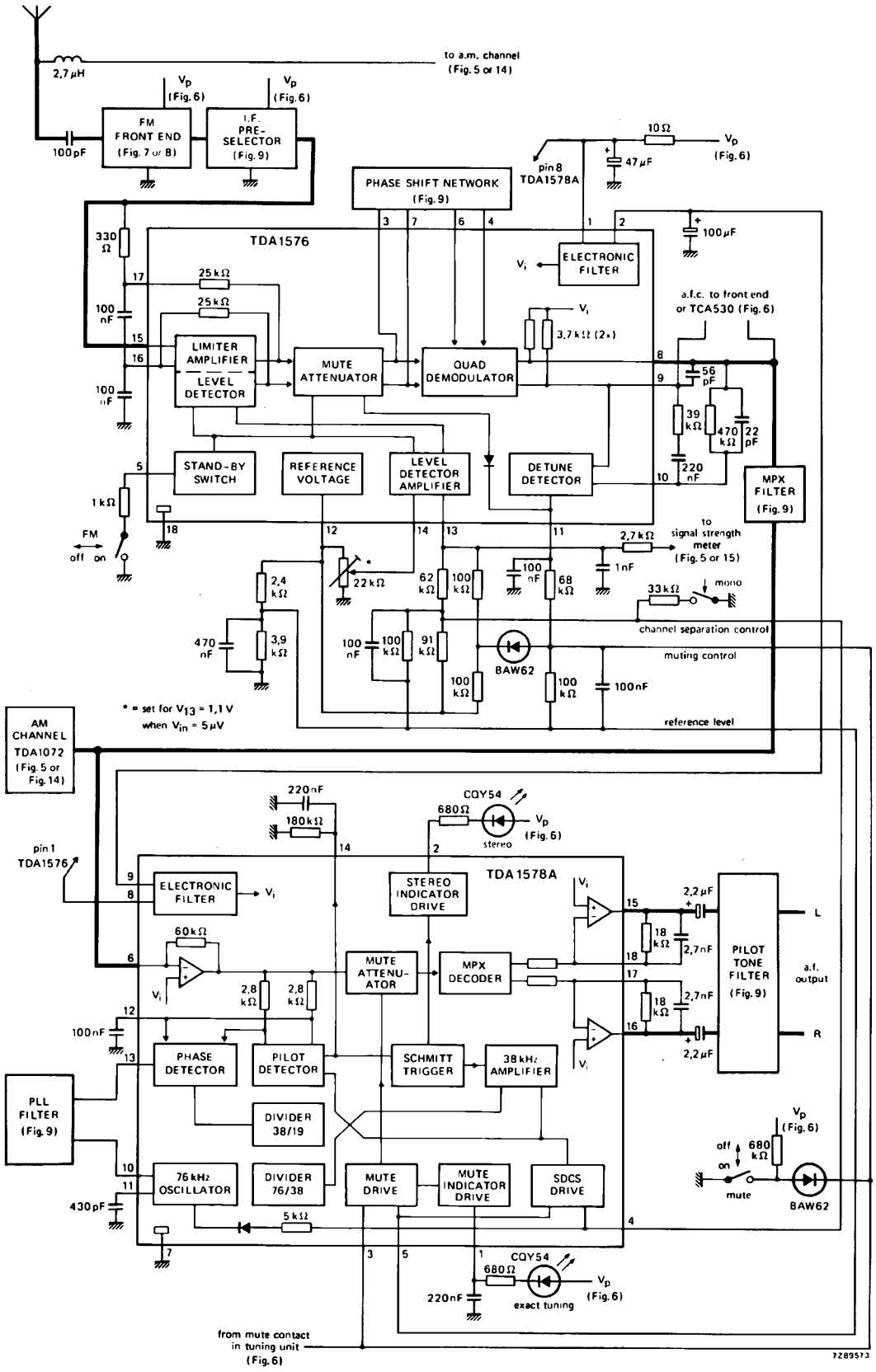


Fig.2 The standard part of the hi-fi radio circuit

tion of weak signals than conventional high-gain systems with quadrature detectors. This is due to a unique fast-acting muting attenuator in the stereo decoder TDA1578A. The level detector/amplifier and detune detector in the TDA1576 drive this muting system which is separately described later in this article. The output from the level detector/amplifier at pin 13, which is a logarithmic function of signal strength over several decades of aerial input voltage, is also used to drive a 1 mA f.s.d. signal strength meter. Other features of the TDA1576 include a symmetrical a.f.c. output with low spread and d.c. offset shift, electronic supply smoothing to eliminate hum in the MPX output, and an internal standby switch to allow a.m./f.m. switching by simply connecting pin 5 to the common return.

PLL stereo decoder

In the time-division multiplex PLL stereo decoder TDA 1578A, the demodulated stereo MPX signal from the TDA 1576 is buffered by an emitter-follower in the preamplifier and fed to the phase detector which forms part of a phase-locked loop (PLL). The frequency of the 76 kHz output from the voltage-controlled oscillator (VCO) in the PLL is halved to 38 kHz, and halved again by a flip-flop to provide two antiphase 19 kHz signals. One of these signals is the other input to the PLL phase detector. The output from the phase detector is fed, via the PLL filter between pins 13 and 10, to the VCO to control its frequency at precisely 76 kHz, thereby closing the loop. The PLL filter determines the bandwidth of the feedback loop and reduces the distortion that can occur due to cross modulation between the desired signal and the stereo pilot tone. During a.m. reception, the VCO in the PLL is not switched off because it has a symmetrical triangular waveform and the oscillator capacitor presents a very small load. If 6 V is applied to pin 4, it becomes a test point at which the VCO output is available for alignment purposes. The uncompensated temperature coefficient of the free-running frequency of the VCO is typically zero with spreads to 100 p.p.m./°C.

The MPX input signal to the TDA1578A and the second 19 kHz output from the divider in the PLL are applied to the inputs of the pilot presence detector. When the PLL is locked, the pilot presence detector generates a d.c. level to activate the mono/stereo Schmitt trigger. Although the switching level of this Schmitt trigger is proportional to the supply voltage, it is compensated for supply voltage fluctuations because the audio output level from the quadrature f.m. demodulator in the TDA1576 has the same degree of supply voltage dependence. The mono/stereo Schmitt trigger has two functions; it lights the stereo LED via the stereo indicator driver, and it connects the 38 kHz output (regenerated stereo subcarrier), from the first part of the VCO divider, to the MPX decoder where it is used for synchronous demodulation of the L and R stereo signals. The mono/stereo switching and stereo channel separation are controlled as a function of the signal-strength dependent level applied to the SDCS (signal dependent channel separation) block at pin 4. The SDCS block switches the pilot detector on and off (mono/stereo) and regulates the amplitude of the regenerated 38 kHz subcarrier applied to the MPX decoder to control the stereo channel separation. The pilot detector is switched off (mono) when the difference between the reference voltage at pin 5 and the control voltage at pin 4 is more than 275 mV. It switches on when the voltage difference between pins 4 and 5 reduces to 250 mV. The channel separation control starts when the voltage between pins 4 and 5 has fallen to 200 mV and full channel separation is achieved when the voltage between pins 4 and 5 reaches 0 V. The characteristics of the SDCS control are determined by the reference voltage on pin 5 and the value of the components between the level detector in the TDA 1576 and pin 4 of the TDA1578A. In the circuit shown, channel separation is smoothly controlled between input levels of 5 μV (0 dB separation) and 100 μV (full separation).

De-emphasis of the left and right stereo audio signals is applied by the capacitors at the stereo decoder output pins 15 and 16. Since the resistors at these pins set the overall gain of the decoder, the gain spread is solely dependent on external components.

Noise muting system

The aim of all hi-fi f.m. stereo radios is to reproduce all received transmissions with high fidelity. In practice however, even the highest performance radios cannot provide adequate quality of reproduction if the strength of the received signal falls below a certain threshold, or when interference is present. It is therefore desirable that the radio should incorporate a muting system which inhibits the audio output under weak signal or interference conditions but does not react when the signal-to-noise ratio is high. The noise muting system contained in the hi-fi radio integrated circuits TDA1576 and TDA1578A not only meets these requirements but also suppresses the following particularly troublesome forms of interference:

- Excessive audible noise when the radio is not tuned to a station or is tuned to a weak signal.
- Interstation noise during tuning. This is particularly obtrusive between two stations transmitting on closely spaced frequencies.
- Side responses above and below the centre frequency of the desired station.
- Harmonic distortion caused by very inaccurate tuning.

Basically, the muting system shown in Fig.3 consists of an audio attenuator in the TDA1578A driven by control voltages from the signal-level detector and the noise/detuning detector in the TDA1576. The TDA1576 also provides a fixed level of about 5.3 V at pin 12 to which both control voltages are referred. Since a portion of this reference voltage is also applied to the mute drive circuit at pin 5 of the

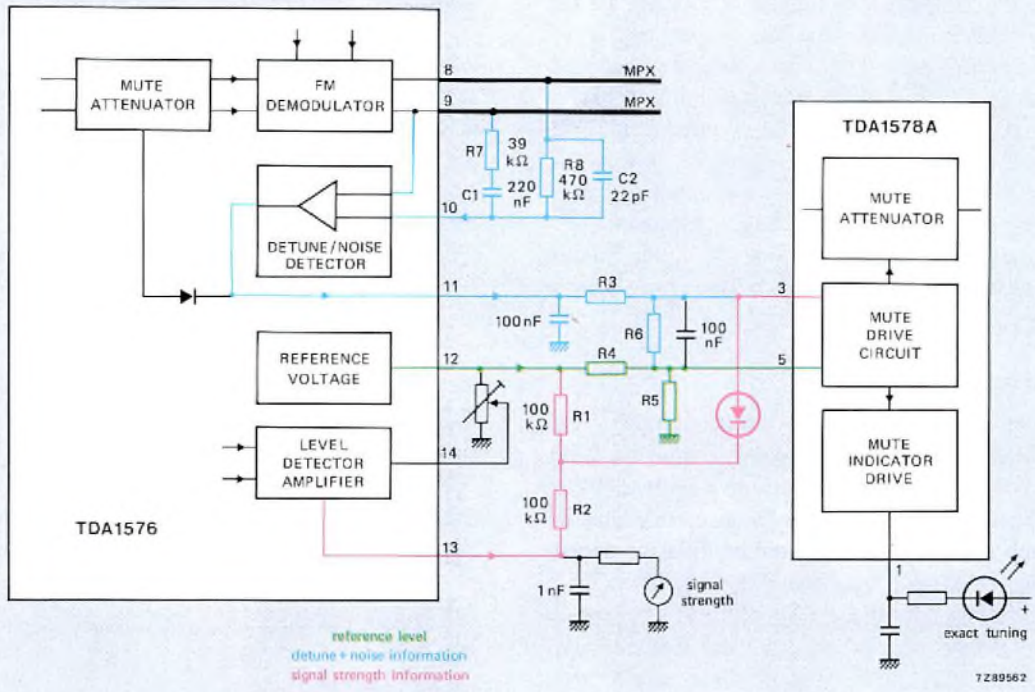


Fig.3 F.M. noise muting circuit

TDA1578A, the muting control system is automatically compensated for fluctuations of supply voltage and operating temperature. The audio attenuation range is 0 dB to 80 dB for a muting control voltage range of 0 to −0.5 V between pins 3 and 5 of the TDA1578A.

The signal-level detector in the TDA1576 generates a d.c. muting control voltage at pin 13 of the TDA1576. This voltage is a logarithmic function of signal strength over several decades of r.f. input voltage. As shown in Fig.4, the preset potentiometer between pin 14 and the reference voltage at pin 12 is adjusted to set the control level at pin 13 to 1.1 V for an r.f. input level of 5 μV. The entire voltage range at pin 13 is used to drive the signal strength meter. The voltage range below 1.1 V controls the muting system. The signal-level dependent control voltage is routed from pin 13 of the TDA1576 to the mute drive input at pin 3 of the TDA1578A via D_1 and voltage divider R_1/R_2 which sets the slope of the muting control voltage characteristic. Increasing the resistance ratio R_1/R_2 increases the range of r.f. input voltage required to cover the muting range 0 dB to 80 dB. Diode D_1 prevents the voltage at pin 13 from activating the muting system during the reception of strong r.f. signals. The muting control voltage is then derived solely from the detune/noise detector in the TDA 1576.

As previously explained, inaccurate tuning, tuning drift and interference can cause poor quality reception, even of stations with adequate signal strength. Under these conditions, the detune/noise detector in the TDA1576 generates a muting control voltage at pin 11 from the inputs it receives from the f.m. demodulator. If the radio is inaccurately tuned, a d.c. level is present at the f.m. demodulator output between pins 8 and 9 of the TDA1576. This d.c. level is 0 V for correct tuning and, in the described application, it is plus or minus 850 mV when the radio is detuned by 100

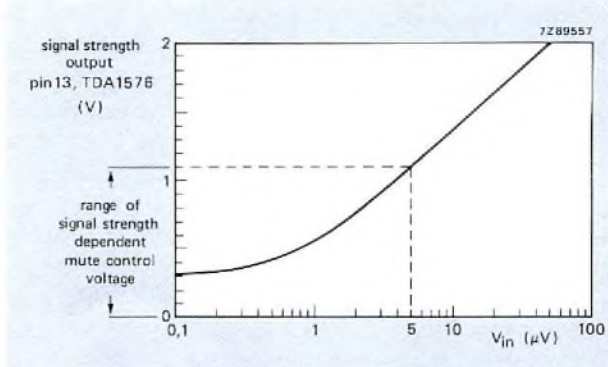
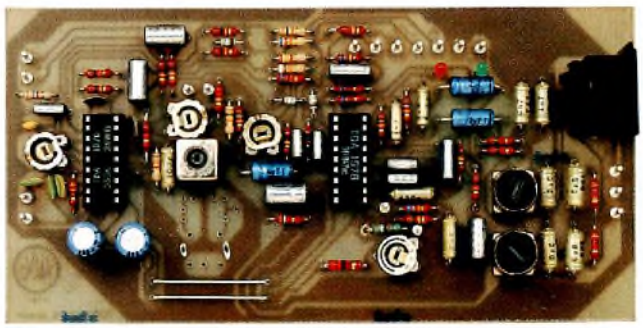


Fig.4 Output from the signal-level detector

kHz. Its polarity is immaterial because the detune/noise detector automatically receives the absolute value. Since capacitors C_1 and C_2 can be considered to be open-circuit to d.c., the d.c. voltage at pin 8 is passed via R_8 to the input of the detune/noise detector at pin 10. The detune/noise detector therefore generates a muting control voltage at pin 11 which is proportional to the extent of detuning. This control voltage is passed, via potential divider R_3/R_6 to the input of the mute drive circuit at pin 3 of the TDA 1578A. In addition to controlling the mute attenuator, the mute drive circuit also activates a mute indicator driver to control a LED connected to pin 1. This indicator lights when the muting is less than 1 dB to indicate correct tuning. In practice, the MPX outputs from the f.m. demodulator at pins 8 and 9 of the TDA1576 are not pure d.c. but also contain the modulation of the received signal (up to 53 kHz for stereo transmissions) and, in some cases, interference components which can extend up to about 200 kHz, dependent on the bandwidth of the i.f. amplifier. Since the detune/noise detector functions as a peak detector for a.c. inputs, the high-frequency interference must be allowed to reach its input but, to avoid modulation-dependent muting, the low-frequency modulation must not reach its input. One input of the detune/noise detector is therefore internally connected to the f.m. demodulator output and the other input is externally connected via pin 10. This arrangement allows a band-stop filter, which provides 20 dB attenuation between 3 Hz and 80 kHz, to be interposed between the outputs from the f.m. demodulator and the inputs to the detune/noise detector. The 3 Hz lower limit of the stopband is set by series network R_7/C_1, and the upper 80 kHz limit is set by parallel network R_8/C_2. The detune/noise detector therefore operates at full sensitivity for f.m. demodulator output signals of less than 3 Hz (detuning) or between 80 kHz and 200 kHz (interference), but its sensitivity is reduced by 20 dB for f.m. demodulator output signals within the frequency range 3 Hz to 80 kHz (modulation).



The f.m. channel (without front-end) for the economy version of the hi-fi radio

Pin 11 of the TDA1576 also serves as an input to a mute attenuator in the TDA1576. This muting facility is not used for hi-fi stereo radios. It is used in mono f.m. radios to allow muting which is solely dependent on signal strength. It is activated when the voltage at pin 11 is less than 0.7 V.

The a.m. channel

The TDA1072 performs all the a.m. channel functions required between the aerial and the audio amplification stages of a radio. Its low distortion handling of a wide dynamic range of input signals and its many additional features make it suitable for use in the circuit shown in Fig.5 which is variable-capacitor tuned over the medium waveband (510 kHz to 1620 kHz) and is used in both the economy and the high-performance version of the radio.

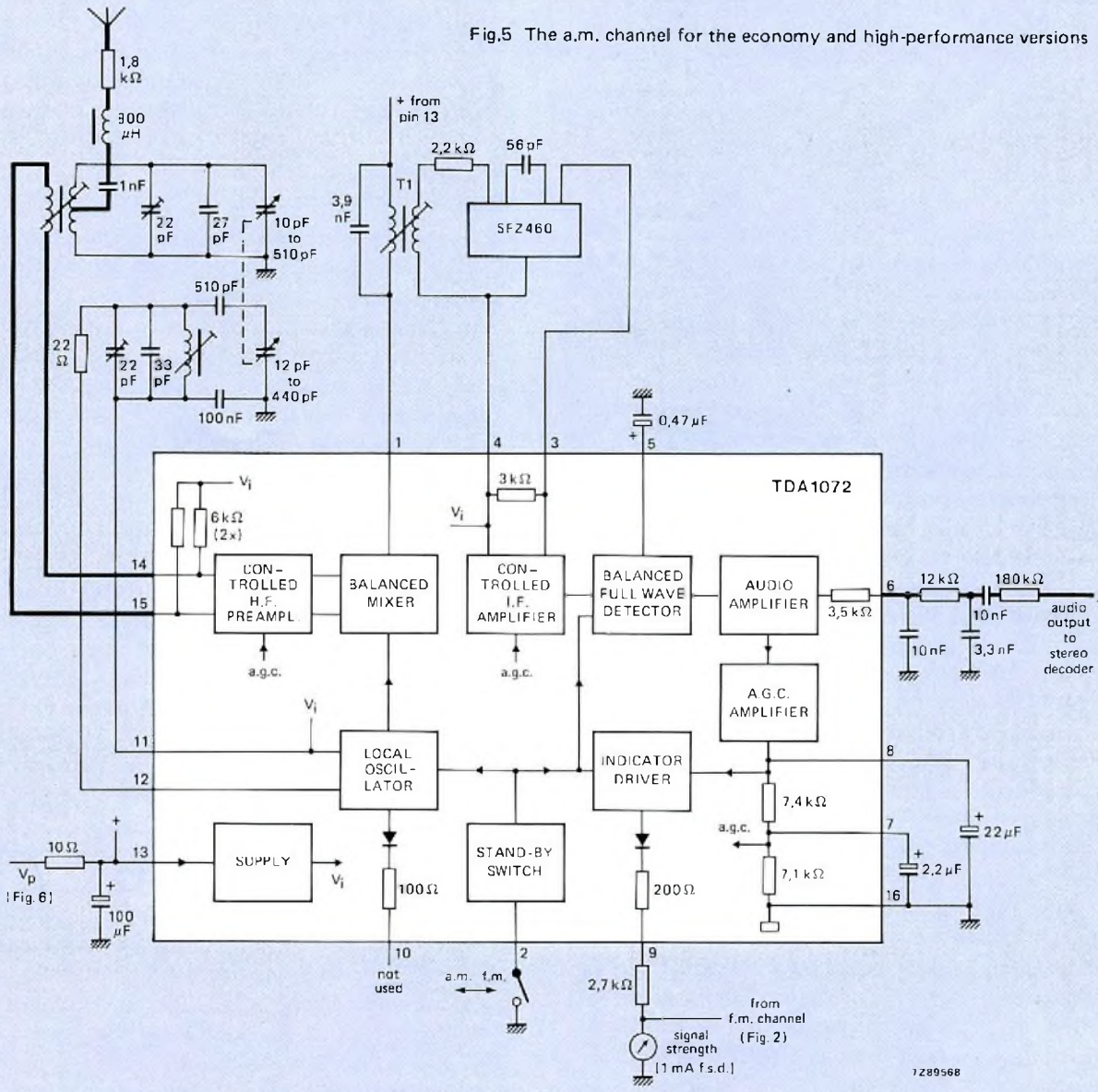
The aerial input is coupled to the h.f. preamplifier at pins 14 and 15 by a single-tuned LC circuit. Input signals of up to 1.3 V, modulated to 80% can be handled with less than 3% distortion and the distortion falls to 0.3% for input signals below 300 mV. This low distortion is mainly due to the use of a balanced full-wave detector with internal i.f. filter. The i.f. rejection is >60 dB over most of the medium waveband (510 kHz to 1620 kHz). The fully symmetrical mixer is essential to achieve this performance. For accurate mixing, it is desirable that the amplitude of the local oscillator signal should be independent of tuned frequency. The local oscillator output at pin 12 is therefore controlled at a typical level of 140 mV up to a frequency of 50 MHz.

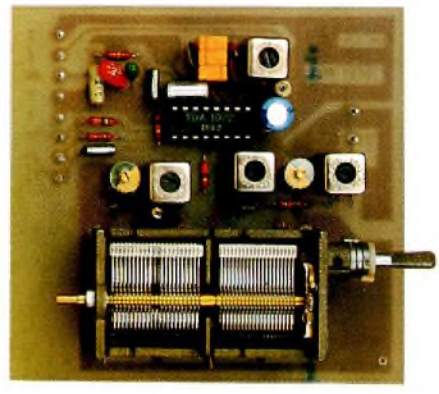
The i.f. selectivity is concentrated in a hybrid filter comprising a tuned LC circuit followed by a 2nd-order ceramic filter at the output from the mixer. The LC circuit prevents the intermodulation distortion which would occur if the radio were detuned during the reception of a strong signal. The a.g.c. loop contains a 2nd-order filter comprising two internal resistors and two external capacitors connected to pins 7 and 8. The filter component values are chosen to reduce harmonic distortion of low-frequency modulation without causing too much delay of the a.g.c. The starting levels of the a.g.c. for the three controlled stages (r.f. preamplifier and two i.f. stages) are determined internally and are therefore independent of the spreads of external components. The a.g.c. control range is 90 dB for an audio output level change of 6 dB.

A buffered d.c. output which is a logarithmic function of aerial input voltage is available for driving a signal strength meter at pin 9 from which up to 2 mA may be drawn. With an input of 500 mV between pins 14 and 15, the typical signal strength output at pin 9 is 2.8 V. The TDA1072 is switched on and off (a.m./f.m. band selection) by an internal standby switch activated by connecting pin 2 to the common return.

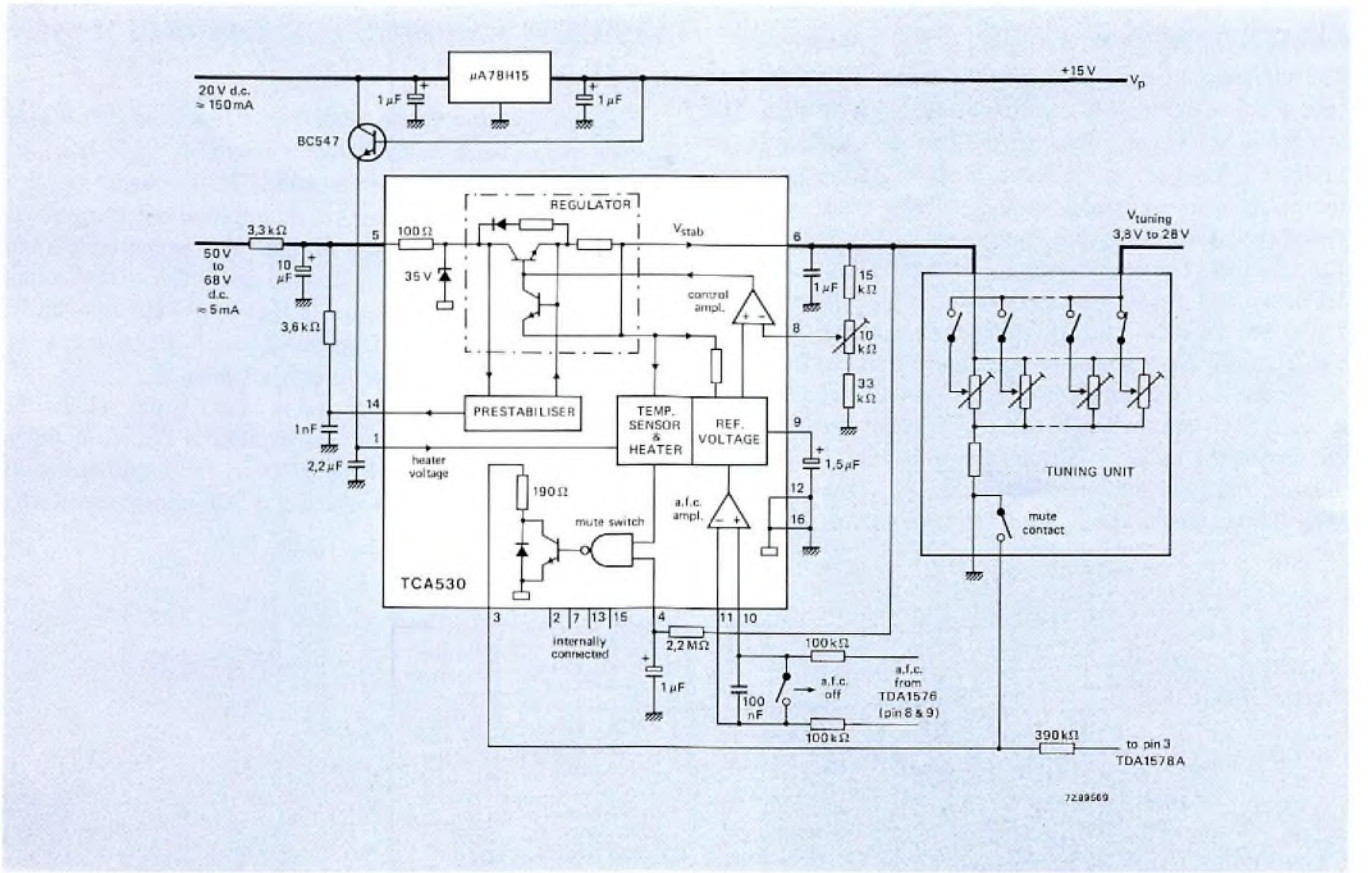
The output from pin 6 is passed through a 2nd-order low-pass RC filter which limits the demodulated signal to the audible range.

Fig.5 The a.m. channel for the economy and high-performance versions





The a.m. channel for the economy and high-performance versions of the hi-fi radio



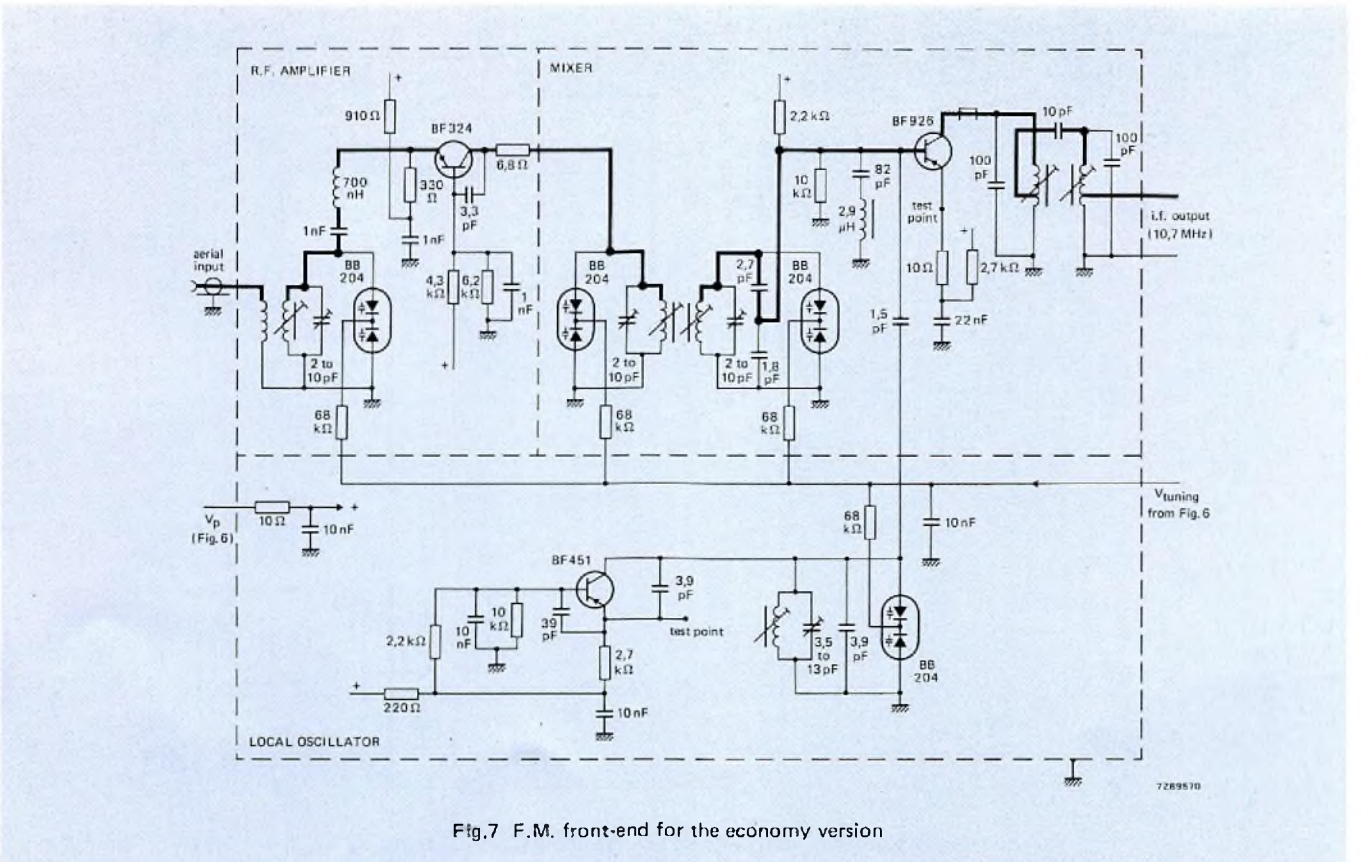


Fig.7 F.M. front-end for the economy version

The power supply

The circuit of the power supply for radios with electronic tuning but without a PLL synthesiser is shown in Fig.6. The integrated voltage stabiliser TCA530 which incorporates an internal voltage reference diode provides a constant level, temperature-compensated tuning voltage with superimposed a.f.c. for the variable-capacitance tuning diodes in the f.m. channel. The circuit also incorporates an internal crystal heater and a muting switch which inhibits the audio output from the radio until the temperature of the crystal of the TCA530 has stabilised. The duration of the muting is prolonged by the time-constant of the RC combination connected to pin 4. The 15 V d.c. supply for the integrated circuits of the radio is derived from a μA78H15 voltage regulator, the output from which is passed to the electronic smoothing circuits built into the TDA1576 and TDA 1578A.

CIRCUIT VARIANTS FOR THE HI-FI RADIOS

F.M. front-ends

The variable-capacitance diode tuned f.m. front-end for the economy version of the radio is shown in Fig.7. It covers the v.h.f. band 87.5 MHz to 108 MHz. The aerial signal is fed, via an input filter, to the r.f. amplifier operating in the common-base mode. Due to the high operating current (4 mA) of this transistor, its gain is so high that the coupling to the input and the output tuned-circuits can be loose, resulting in good large signal handling characteristics, low noise and good repeat spot suppression.

The variable-capacitance diode tuned front-end for the high-performance version of the radio is shown in Fig.8. The use of a dual-gate MOSFET as an r.f. amplifier results in a noise figure of 4 dB which is a 2 dB improvement over

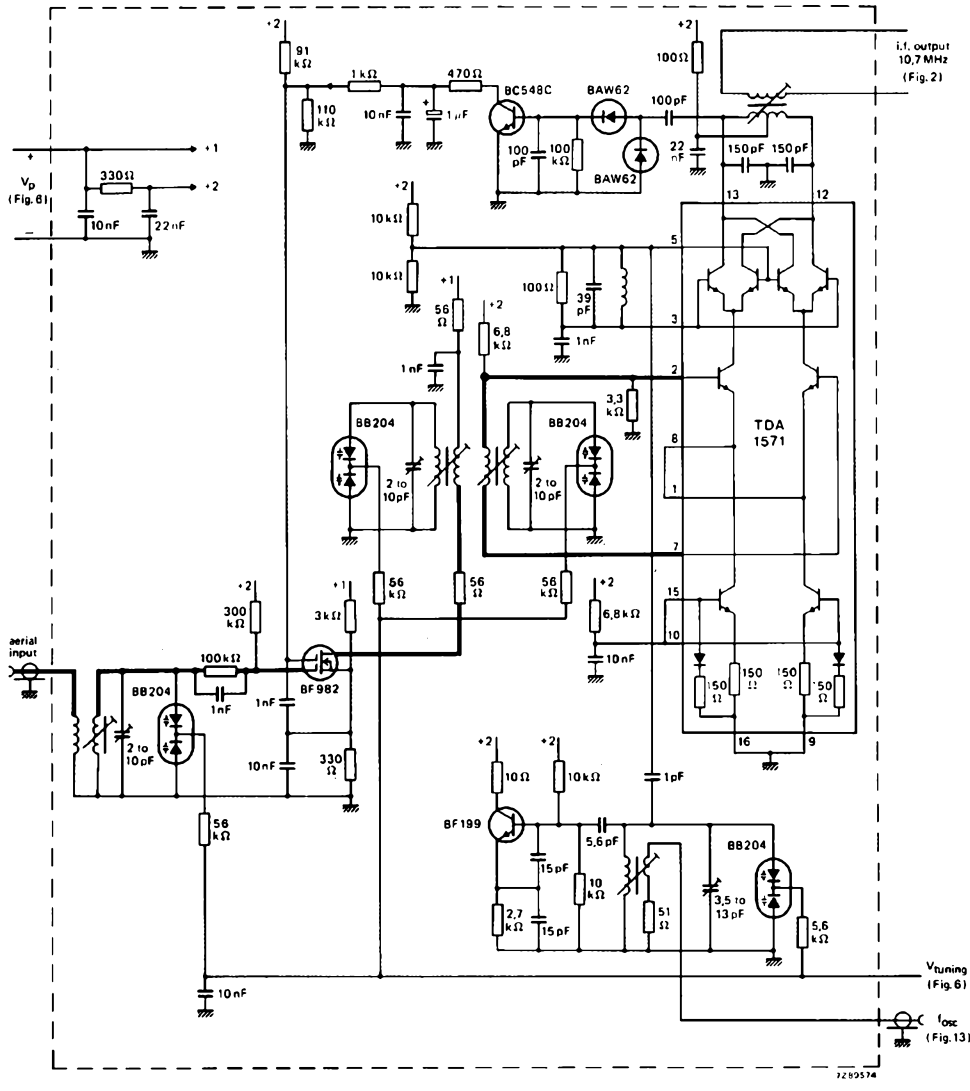


Fig.8 F.M. front-end for the high-performance version

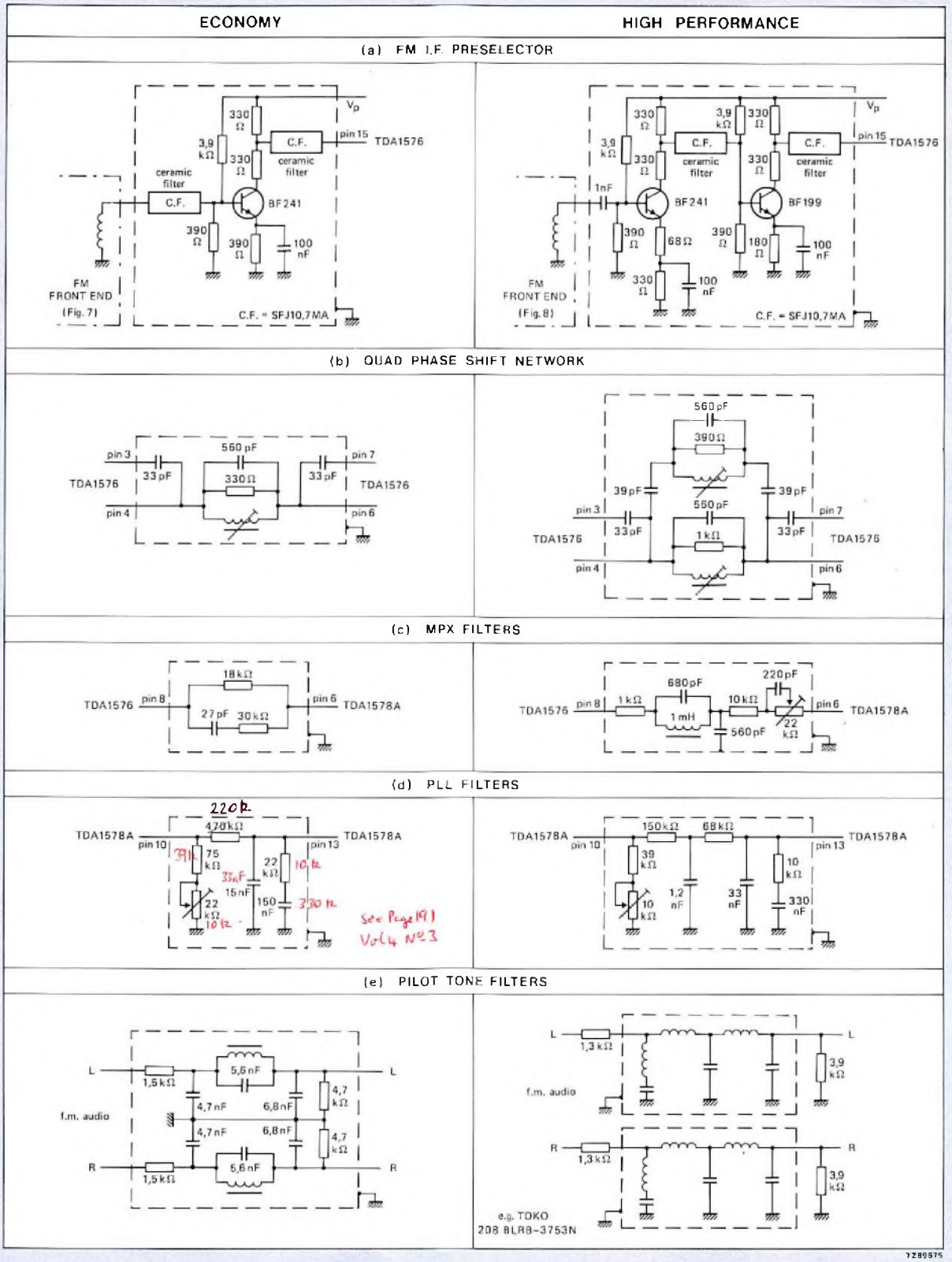


Fig.9 Circuit variants (a) i.f. preamplifiers
(b) quadrature phase-shift networks for the f.m. demodulator
(c) MPX filters
(d) PLL filters
(e) pilot tone filters

the economy front-end. To improve the large signal handling capability, a.g.c. is applied to the r.f. amplifier and an integrated balanced mixer TDA1571 is used with loose oscillator coupling via a wideband resonant circuit between pins 3 and 5.

F.M. i.f. preamplifiers

In both versions of the radio, an i.f. preamplifier as shown in Fig.9 (a) compensates for the insertion loss of the ceramic filter which couples the f.m. front-end and the input to the limiting i.f. amplifier in the TDA1576. The two-stage preamplifier for the high-performance version of the radio improves the limiting, and therefore the a.m. suppression, even during the reception of weak signals. Although the preamplifier increases the noise level of the overall i.f. amplifier, this is reduced again by the muting system in the TDA1576/TDA1578A combination.

Quadrature phase-shift networks for the f.m. demodulator

The modulation of the received f.m. signals is accurately recovered in the TDA1576 by a symmetrical quadrature demodulator which requires inputs with a 90° phase relationship. The necessary phase shift is provided by a single-tuned or double-tuned LC circuit as shown in Fig.9 (b). For the single-tuned LC circuit, the THD of the radio is inversely proportional to the square of the overall Q of the phase-shift network. For the double-tuned LC circuit, the THD is a function of the Q and the kQ factor between the two tuned circuits. The audio output of the f.m. channel is also a function of the Q. The single-tuned economy version network has a Q of 10 and the double-tuned high-performance version has a Q of 15. As shown in Fig.10, the THD of the high-performance radio in the centre of the i.f. passband is lower than that of the economy version and it increases less as a function of detuning. The higher Q network also results in a 3.5 dB increase of audio output from the demodulator of the high-performance radio with a consequent improvement of the signal-to-noise ratio.

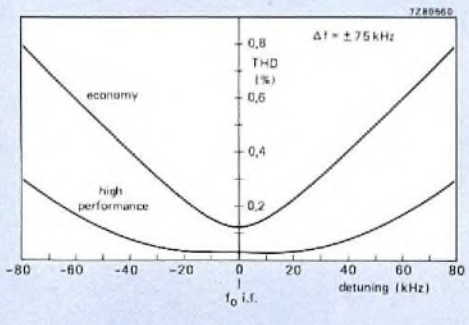


Fig.10 Distortion as a function of detuning of the f.m. channel

MPX filters

The MPX filters shown in Fig.9 (c) are connected to the output from the f.m. demodulator in the TDA1576. The filter for the high-performance version of the radio attenuates the fifth harmonic of the residual stereo subcarrier (5 x 38 kHz = 190 kHz) which could otherwise mix with a signal in an adjacent channel 200 kHz from the desired signal and cause audible interference. It is a second-order LC type which also incorporates an RC network for adjustment of the phase of the stereo MPX signal relative to that of the transmitted stereo subcarrier so that optimum stereo channel separation is obtained. The MPX filter for the economy version of the radio is an RC network which provides fixed correction of the phase of the stereo MPX signal.

PLL filters

The PLL filters shown in Fig.9 (d) are connected to the TDA1578A. They determine the bandwidth of the feedback loop of the PLL 76 kHz oscillator and provide facilities for setting its frequency. The filters attenuate intermodulation products caused by mixing of the pilot tone with the modulation of the received signal. Since these products occur at 19 kHz − f_{mod} and $2f_{mod}$ − 19 kHz, they can fall within the audible frequency spectrum. The performance of the PLL filter for the economy version of the radio is shown in Fig.11, and that for the high-performance version is shown in Fig.12.

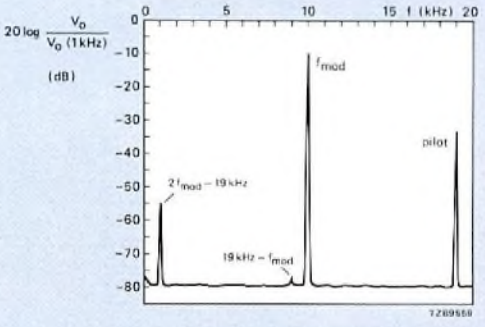


Fig.11 Pilot tone intermodulation (economy version)

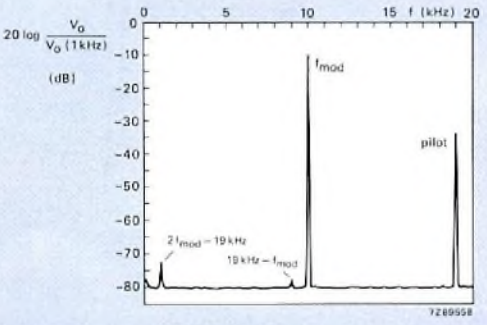


Fig.12 Pilot tone intermodulation (high-performance version)

Pilot tone filters

The stereo decoder TDA1578A provides 32 dB attenuation of the 19 kHz pilot tone and 50 dB attenuation of the 38 kHz stereo subcarrier. Although the residual components of these signals at the decoder output are beyond the audible frequency range, they can give rise to audible interference if mixed with signals from other sources such as the bias oscillator of a tape or cassette recorder. The pilot tone filters shown in Fig.9 (e) therefore provide additional attenuation at 19 kHz and 38 kHz. The filter for the economy version of the radio provides 32 dB additional attenuation at 19 kHz and 15 dB at 38 kHz. The filter for the high-performance version provides 26 dB additional attenuation at 19 kHz and 50 dB at 38 kHz.

Microcomputer-controlled radio or tuner

Figure 13 shows how the high-performance version of the radio can be modified for microcomputer control. The tuning system uses a phase-locked loop to maintain stable, accurate tuning of the a.m. and f.m. channel. The a.m.

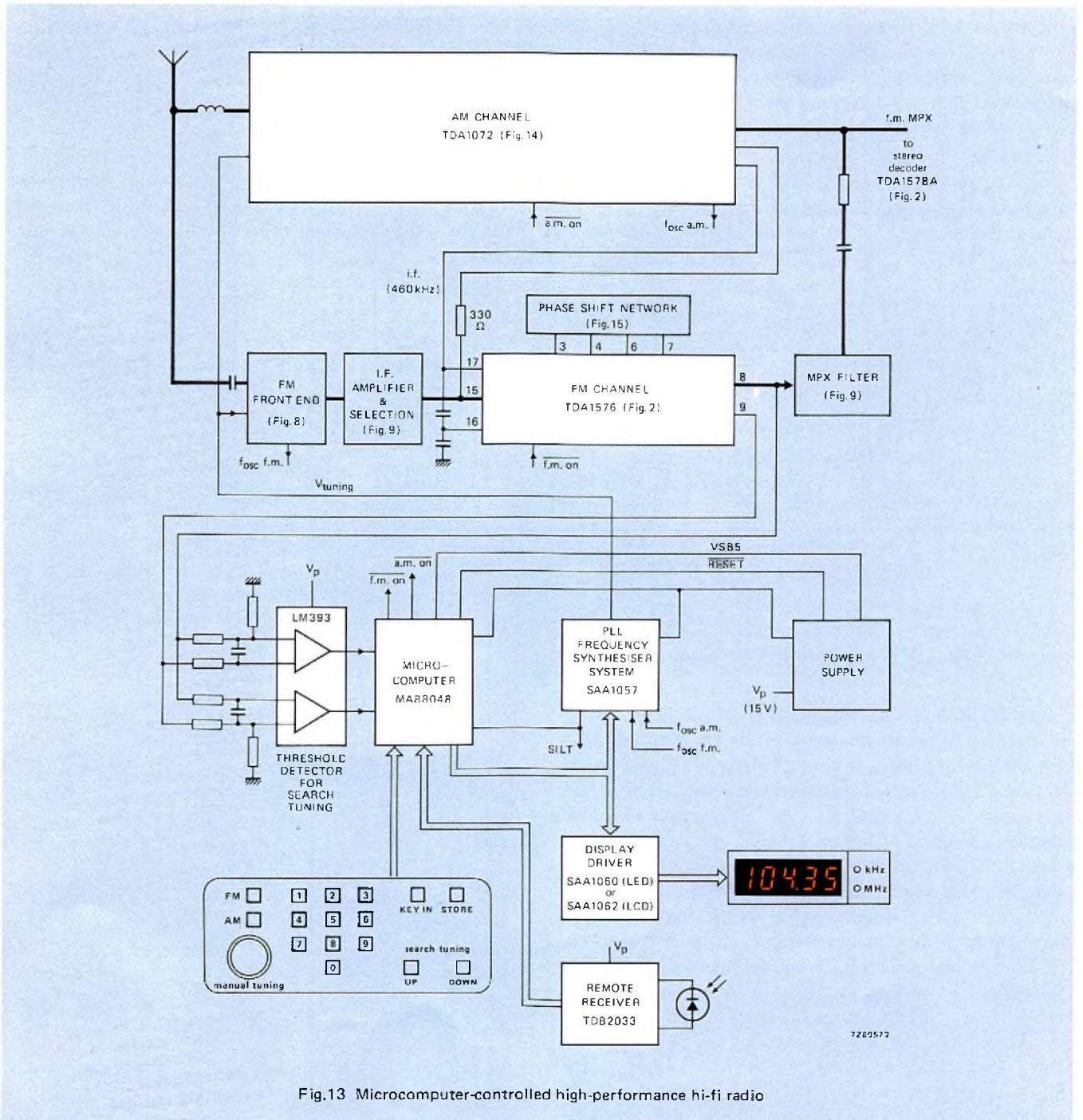


Fig.13 Microcomputer-controlled high-performance hi-fi radio

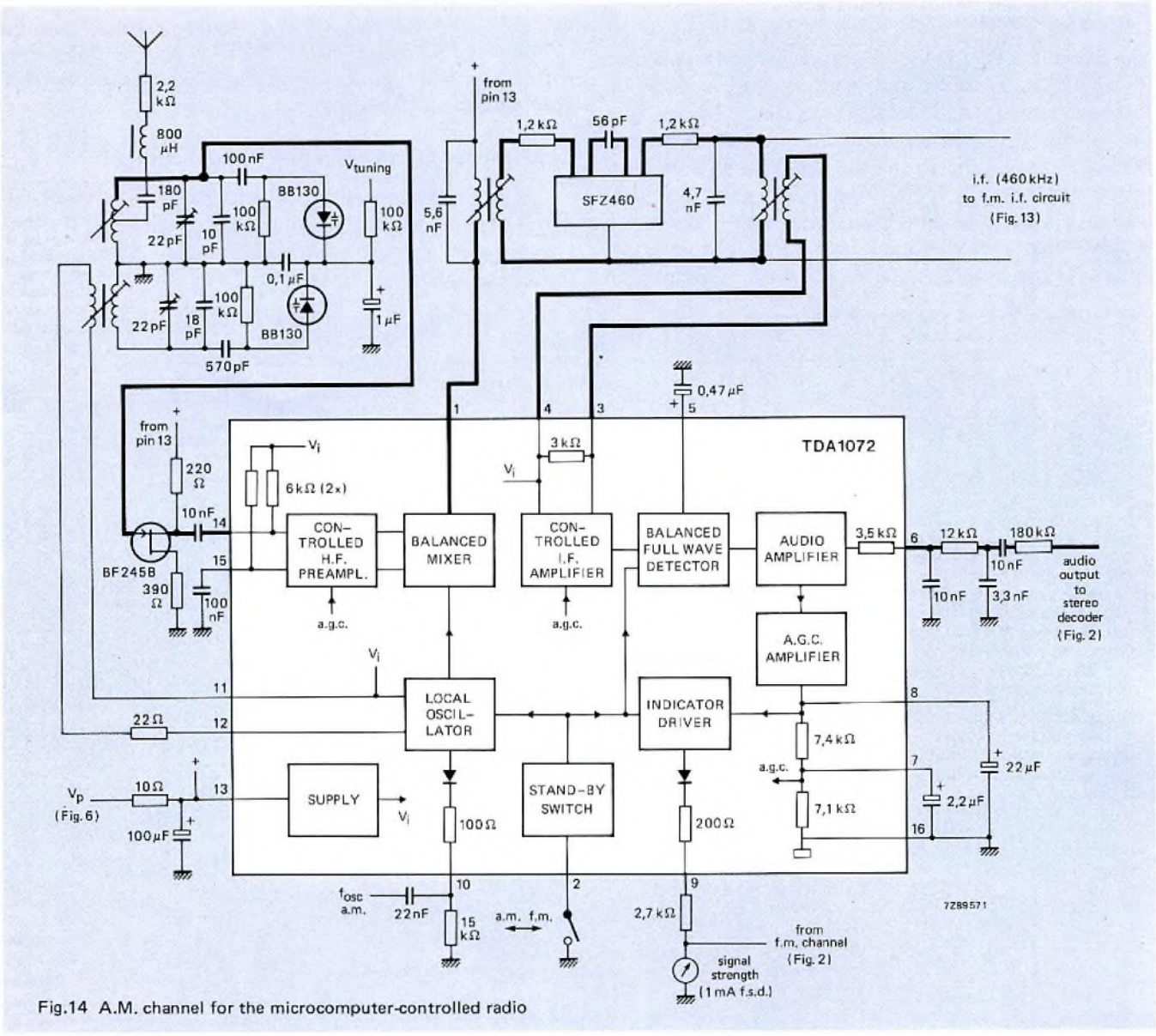


Fig.14 A.M. channel for the microcomputer-controlled radio

channel TDA1072 with variable-capacitance diode tuning for this radio is shown in Fig.14. In Fig.13, the local-oscillator output from the a.m. channel TDA1072 is passed to a frequency divider with a programmable division ratio in the PLL frequency synthesiser SAA1057. The output from the divider is compared with a crystal-controlled reference frequency. The result of the comparison, which represents any tuning error, is amplified and filtered before it is used to modify the tuning voltage applied to the variable-capacitance diodes in the f.m. front-end or in the a.m. channel. The listener can change the tuned frequency by keying-in the required broadcast frequency, or by manual or search tuning. These commands cause the microcomputer to calculate the appropriate division ratio for the programmable divider after adding or subtracting the i.f. The stop pulses required when a station is detected during search tuning are generated in a very simple manner for both reception chan-

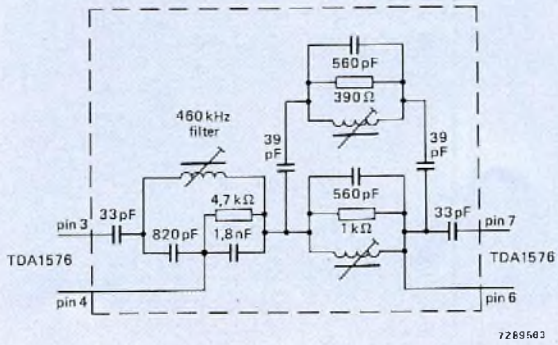
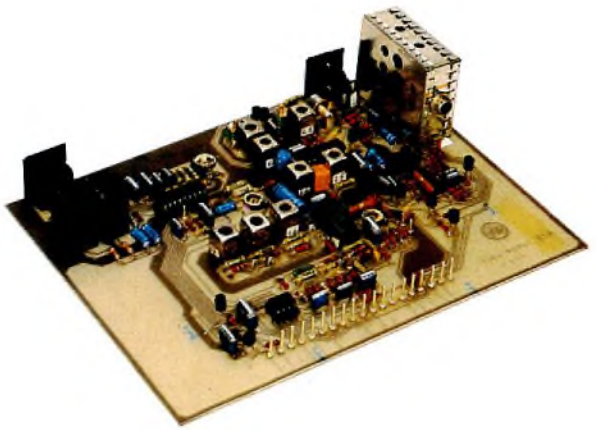


Fig.15 Demodulator filters for the microcomputer-controlled radio

nels by using the TDA1576 as a balanced phase demodulator for both a.m. and f.m. For this purpose, the TDA1576 demodulator circuit incorporates tuned circuits which are resonant at the i.f. of the a.m. and f.m. channels. These tuned circuits are shown in Fig.15. During a.m. or f.m. search tuning, the TDA1072 and/or TDA1576 is switched on by the microcomputer and the zero crossing of the S-curve at the output of the phase demodulator in the TDA 1576 is located by the LM393 threshold detector to identify the correct tuning point. If a.m. is being received, the TDA1576 is then switched off by the microcomputer and normal reception continues via the a.m. channel TDA1072.



The complete high performance hi-fi radio for microcomputer control

PERFORMANCE OF THE RADIOS

This section gives the performance of all three versions of the hi-fi radio. The headings above the performance figures are version 1 = economy version, version 2 = high performance version, 3 = microcomputer-controlled version.

General

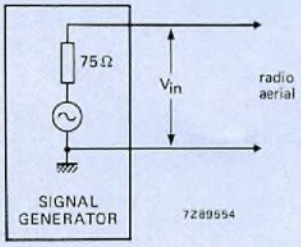
Supply voltage (d.c.)	15	V
Ambient temperature	25	°C
F.M. frequency range	87.5 to 108	MHz
A.M. frequency range	510 to 1620	kHz
F.M. i.f.	10.7	MHz
A.M. i.f.	460	kHz
F.M. aerial input impedance (asymm.)	75	Ω

F.M. characteristics

f_o = 98 MHz, Δf = ±40 kHz, f_{mod} = 1 kHz unless otherwise stated. Generator impedance 75Ω.

	version 1		version 2 & 3	
Input voltage for				
−3 dB limiting without muting	0.7	μV	0.5	μV
−3 dB limiting with muting	2.2	μV	2.2	μV
mono				
(S + N)/N = 26 dB	0.9	μV	0.7	μV
= 46 dB	2.2	μV	2	μV
stereo (channel separation >32 dB)				
(S + N)/N = 46 dB	20	μV	18	μV
Input voltage				
for stereo lamp on	5	μV	5	μV
for 40 dB channel separation	20	μV	18	μV

Stereo channel separation				
for V_{in} >100 μV	45	dB	50	dB
Mono (S + N)/N for V_{in} = 1 mV	73	dB	75	dB
Capture ratio	1.6	dB	1.3	dB
A.M. suppression				
at V_{in} = 1 mV	>50	dB	>50	dB
Total harmonic distortion for stereo				
with Δf = ±40 kHz	0.15	%	0.08	%
with Δf = ±75 kHz	0.2	%	0.12	%
I.F. bandwidth B_{3dB}	190	kHz	190	kHz
Adjacent channel selectivity S_{300}	70	dB	70	dB
Image rejection	72	dB	72	dB
I.F. suppression	>96	dB	>96	dB
Repeat spot suppression				
RSS 2	82	dB	92	dB
RSS 3	>100	dB	>100	dB
Double beat suppression				
DBS 1 and 3	80	dB	98	dB
DBS 2	75	dB	91	dB
Oscillator pulling				
at V_{in} = 1 V	5	kHz	300	Hz
Suppression of spurious responses				
19 kHz pilot tone	64	dB	66	dB
38 kHz stereo subcarrier	>65	dB	>100	dB
Audio bandwidth				
(− 3 dB)	15 Hz to 15.5	kHz	15 Hz to 16	kHz
(− 1 dB)	25 Hz to 14.4	kHz	25 Hz to 15.5	kHz
De-emphasis	50	μs	50	μs



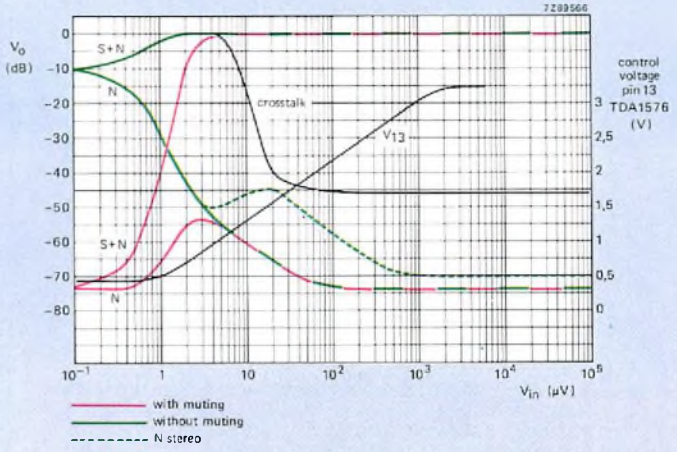
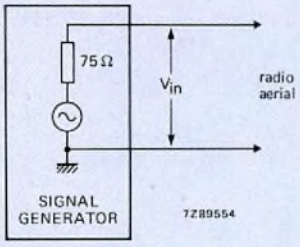


Fig.16 Performance of the f.m. channel of the economy version of the hi-fi radio



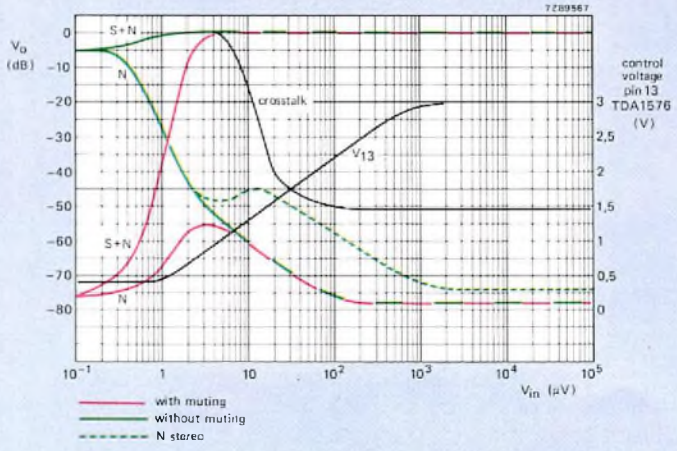
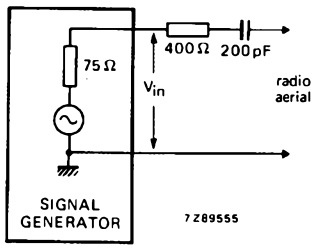


Fig.17 Performance of the f.m. channel of the high-performance version of the hi-fi radio

A.M. characteristics

f_o = 1 MHz, m = 0.3, f_{mod} = 400 Hz unless otherwise stated. Dummy aerial as shown in Fig.18 and 19.

	version 1 & 2		version 3	
Input voltage				
for (S + N)/N = 6 dB	7	μV	7	μV
= 26 dB	80	μV	80	μV
= 46 dB	1.2	mV	1.2	mV
A.G.C. range	90	dB	90	dB
Audio output voltage				
for V_{in} = 2 mV	350	mV	350	mV
R.F. signal handling capability				
at m = 0.8, THD = 3 %	1.3	V	300	mV
Total harmonic distortion				
over most of the a.g.c. range, m = 0.8	0.5	%	0.5	%
R.F. bandwidth B_{3dB}	18	kHz	18	kHz
I.F. bandwidth	3.9	kHz	3.9	kHz
Image rejection				
tuned frequency = 510 kHz	50	dB	50	dB
= 1 MHz	46	dB	46	dB
= 1.62 MHz	40	dB	40	dB
Adjacent channel selectivity S_9	35	dB	37	dB



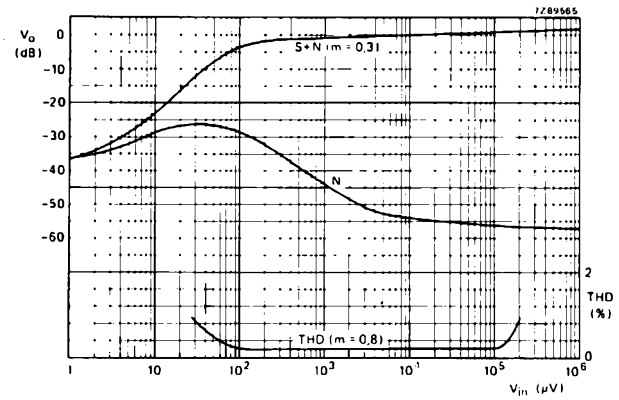
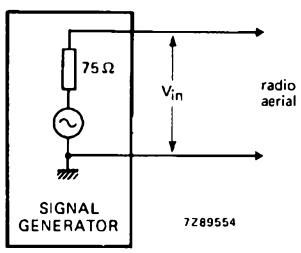


Fig.18 Signal-to-noise ratio and distortion for the a.m. channel of the economy and high-performance versions of the hi-fi radio



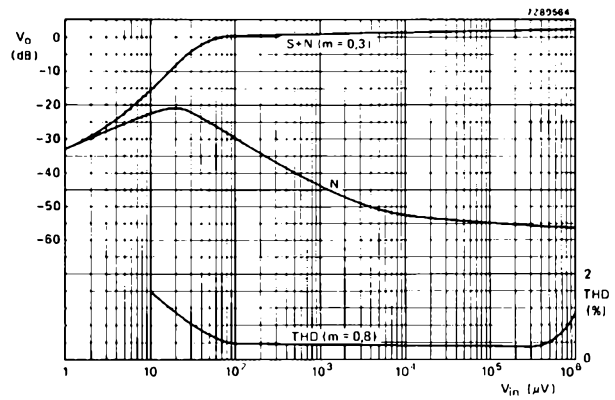


Fig.19 Signal-to-noise ratio and distortion for the a.m. channel of the microcomputer-controlled version of the hi-fi radio

ACKNOWLEDGEMENT

The authors wish to acknowledge the assistance given by their many colleagues during this project. Particular thanks are due to Bahne Peter Bahnsen and Wolfgang Schulze of the Valvo application laboratory and Hans Heinrich Feindt of the Valvo IC sales department.

Not long ago it took upwards of a hundred ICs to implement even a minimal CRT display terminal. Using a new set of four LSI chips to control the fundamental functions it can now be done with just fifteen. An intelligent terminal with 'all the bells and whistles' takes only a few more.

Integrated circuits for data-graphic displays

A. GOLDBERGER and J. L. GOODHART

Microprocessors and LSI have had a dramatic impact on the implementation and capabilities of alphanumeric CRT terminals. The first generation of CRT terminals were little more than 'glass teletypes'. Current designs, implemented with microprocessors, are characterised by an abundance of sophisticated features that were previously not economically feasible: a universal hardware design that can adapt to different user requirements simply by changing software or firmware; programmability to provide end users with the flexibility to execute specialised routines; and local intelligence and storage which off-loads the host CPU by permitting data manipulation and verification at the terminal site.

Just as the impact of microcomputers has been felt in the functional capabilities of terminals, advances in semiconductor technology have revolutionised the hardware implementation. Designs that previously consisted of 100 to 200 ICs can now be realised with a few dozen MSI and LSI devices. The majority of the LSI manufacturers' effort with respect to CRT terminals has been concentrated in the 'CRT controller' area. These circuits provide the character timing, display addressing, and sync generation functions required by all terminals. However, these controllers need to be supported by many other external circuits to implement a complete terminal.

A set of four LSI chips recently introduced by Signetics, when combined with standard CPUs, memories and TTL, can comprise a complete CRT terminal in just 15 device packages. Previous minimum-parts-count terminal designs were based on a CRT controller chip and required almost 40 ICs.

The new LSI chip set developed by Signetics consists of the 2670 display character and graphics generator, the 2671 programmable keyboard and communications controller, the 2672 programmable video timing controller, and the 2673 video and attributes controller. When incorporated in a CRT terminal, they help provide many important features, even for minimum chip-count designs. For example, a display format containing 24 or 25 character rows is always available. So too are 96 ASCII alphanumeric characters, 32 special symbols, block and thin-line graphics, a cursor, three operating modes, five visual attributes and an RS-232 compatible serial interface.

PARTITIONING

In a typical microcomputer-based CRT terminal (Fig.1), the CPU examines inputs from the data-communications line and the keyboard and places the data to be displayed in a display buffer memory (RAM), which holds the data for a single or multiple screenload (page) or for a single character row. Intelligent terminals start with the same base, but have additional circuits to provide more features and capabilities.

The major function of the timing and sync generation block in Fig.1 is to generate the horizontal and vertical timing signals required to produce the raster on the CRT. Other functions include the generation of display memory addresses in synchronism with the CRT scan and in accordance with a defined format (characters per row, scan lines per row, and rows per screen), generation of a cursor signal at the appropriate scan position, and generation of blanking signals during flyback.

In its simplest form, the I/O interface block provides an interface to a keyboard to identify the key depressed and a serial communications link, normally operating in an asynchronous mode, between the terminal and the host computer. Although these functions could be programmed through the terminal CPU system, removing them to intelligent controllers unburdens the CPU, allowing it to provide additional features at little extra cost.

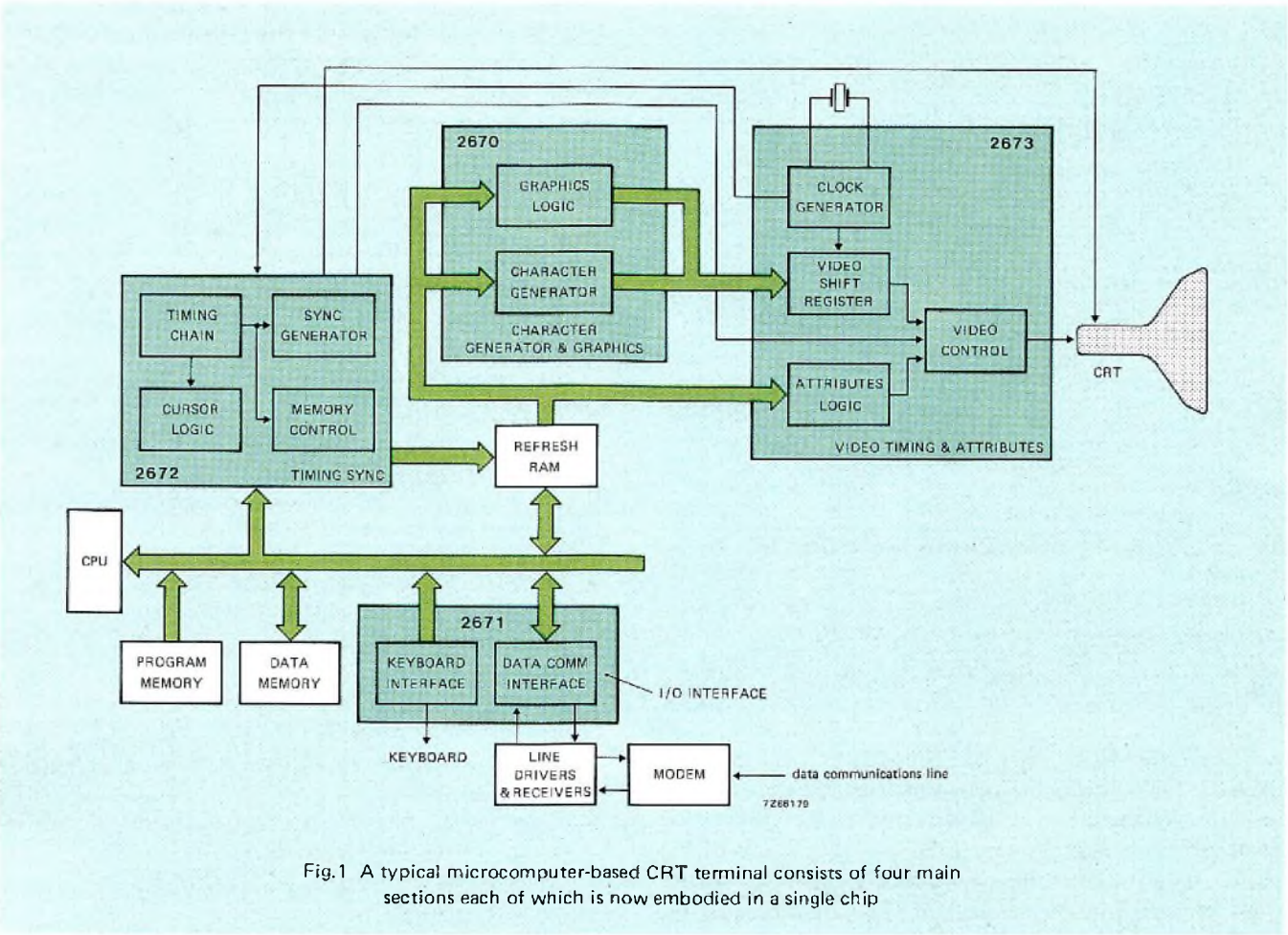


Fig.1 A typical microcomputer-based CRT terminal consists of four main sections each of which is now embodied in a single chip

The character generator and graphics logic circuits convert the data stored in the display memory to the line-by-line dot patterns required to display it on the CRT.

The video timing and attributes section of Fig.1 contains the high speed (dot rate) circuits necessary to convert the parallel data from the character generation and graphics logic circuits to the serial video stream required by the CRT. It also includes circuits to add visual display attributes such as blinking, high/low intensity, reverse video, and underlining to the video stream.

The Signetics chip set consists of four devices whose functions correspond closely to the four major CRT-terminal blocks just described. The circuits have been partitioned so that each chip can be used independently of the others. Several alternative methods of implementing the display memory interface are provided so that the hardware can be tailored to the system requirements. The circuits provide a full complement of programmable capabilities and minimise support circuitry.

2672 TIMING CONTROLLER

The 2672 video timing controller is a programmable device designed for use in raster-scanned CRT terminals and display systems. It generates the vertical and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT. Also, the 2672 provides addressing to a user-specified display buffer memory domain and controls the CPU-display buffer interface for various buffer configuration modes. Programmable features include screen format (characters/row, rows/screen, scan lines/row), horizontal and vertical timing parameters, cursor type (block or underline) and blink rate, interlaced or non-interlaced operation, and single or double height characters.

The 2672 can produce interrupts based upon several internal conditions. By using these interrupts, or by polling the equivalent status register, display features such as non-consecutive buffer addressing (for split-screen operation), multiple cursors, horizontal and vertical scrolling, and smooth vertical scroll are implemented.

One of the 2672's key features is its support of four common display buffer memory interface configurations; the independent, transparent, shared, and row-buffer modes. The first three modes use a single or multiple-page RAM and differ primarily in the means used to transfer display data between the RAM and the CPU. The row buffer mode makes use of a single row buffer (which can be a shift register or a small RAM) that is updated in real time to contain the appropriate display data.

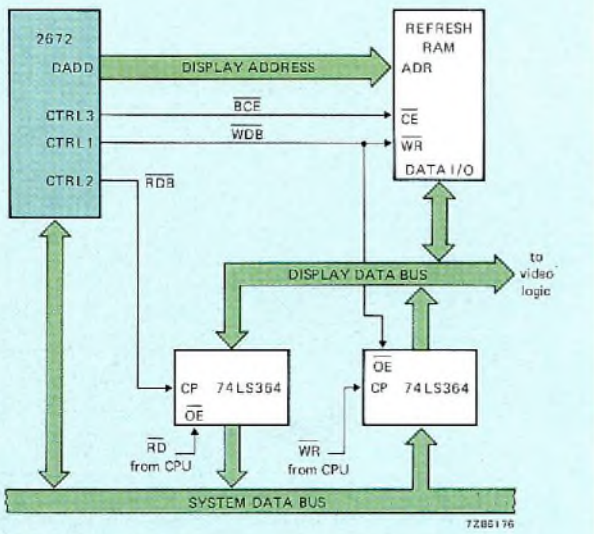


Fig.2 The 2672 supports four common display buffer memory interface connections. Here it functions in the independent buffer mode for transferring data between the CPU and display memory via a bidirectional latched port

The CPU-to-RAM interface configuration for the independent mode (Fig.2) transfers data between the CPU and display memory via a bidirectional latched port. It is controlled by the 2672's read data buffer signal, write data buffer signal, and buffer chip enable signal. This mode provides non-contention operation that needs no address multiplexers. The CPU does not address the memory directly; the read or write operation is performed at the address contained in the 2672's cursor address register or the pointer address register (as specified by the CPU). The 2672 enacts the data transfers during blanking intervals to prevent visual disturbances of the displayed data.

The CPU manages the data transfer by supplying three commands to the 2672:

- read/write at pointer address
- read/write at cursor address (with optional increment of address)
- write from cursor address to pointer address.

Table 1 details the operating sequences for a write-to-memory and a read-to-memory operation. Loading the same data into a block of display memory is accomplished via the write-from-cursor-to-pointer command as outlined in Table 2. Similar sequences can be implemented on an interrupt-driven basis using the READY interrupt output from the 2672 to inform the CPU that a previously requested command has been completed.

Two timing sequences are possible for the read/write-at-cursor/pointer commands. If the command is given during the active display window (defined as first scan line of the first character row to the last scan line of the last character row), the operation takes place during the next horizontal flyback interval. If the command is given during the vertical flyback interval, or while the display has been commanded blanked, the operation takes place immediately.

TABLE 1
2672 operational sequences

Write-to-memory-operation:

1. The CPU loads the data to be written into the display memory into the interface latch.
2. The CPU writes the destination address into the 2672's cursor or pointer registers.
3. The CPU checks the 2672's RDFLG status bit to assure that any previous operation has been completed.
4. The CPU issues a write-at-cursor-with/without-increment or a write-at-pointer command to the 2672.
5. The 2672 negates RDFLG, outputs the specified address, and generates control signals to perform the requested operation. Data is copied from the interface latch into the memory.
6. The 2672 sets its RDFLG status to indicate that the write operation is completed.

Read-from-memory operation:

1. The CPU writes the source address into the 2672's cursor or pointer registers.
2. The CPU checks the 2672's RDFLG status bit to assure that any previous operation has been completed.
3. The CPU issues a read-at-cursor-with/without-increment or read-at-pointer command.
4. The 2672 negates RDFLG, outputs the specified address, and generates control signals to perform the read operation. Data is copied from the memory to the interface latch and the 2672 sets its RDFLG status to indicate that the operation is completed.
5. The CPU checks the RDFLG status to see if the read is completed.
6. The CPU reads the data from the interface latch.

TABLE 2
2672 write-from-cursor-to-pointer operation

1. The CPU loads the data to be written into the display memory into the interface latch.
2. The CPU writes the beginning address of the memory block into the 2672's cursor address register and the ending address of the block into the pointer address register.
3. The CPU checks the RDFLG status bit to assure that any previous operation has been completed.
4. The CPU issues a write-from-cursor-to-pointer command to the 2672.
5. The 2672 negates RDFLG and outputs block addresses and control signals to copy the data from the interface latch into the specified block of memory.
6. The 2672 sets its RDFLG status to indicate that the block write is completed.

Glossary of abbreviations used in the illustrations

ABLANK	blank attribute
ABLINK	blink attribute
ACD	attribute control display
AFLAG	attribute flag
AMODE	attribute mode
ARVID	reverse video attribute
AUL	underline attribute
BACK	bus acknowledge
BCE	buffer chip enable
BEXT	bus external control
BKGND	background intensity
BLK CUR	blank cursor
BREQ	bus request control
BLANK	screen blank
CA	character address
CBLANK	composite blank
CC	character clock control
CCLK	character clock
CE	chip enable
CPU	central processor unit
CR/LF	automatic carriage return/line feed
CS	chip select
CSTROBE	character strobe
CTRL	handshake control
CTS	clear to send
CURSOR	cursor timing
D	data input (output)
DADD	display address
DB	data bit
DCLK	dot clock
GM	graphics mode
HDX/FDX	half duplex/full duplex
HSYNC	horizontal sync
INTA	interrupt acknowledge
INTR	interrupt request
IR	initialisation register
KC	keyboard column scan
KR	keyboard row scan
KRET	key return
LA	line address
LL	last line
LNZ	line zero
LPL	light-pen line
ODD	odd field
OE	output enable
ON/LOC	on-line/local
PBREQ	processor bus request
POP/SOFT	scrolling mode select
PRTY	parity bit
RD	read strobe
RDB	read data buffer
REPEAT	repeat key (15 strokes/s)
RTS	request to send
RxC	receiver clock
RxD	receiver data
SCD	selected character disable
SHIFT	shift key
TTLVID1	non-highlighted video
TTLVID2	highlighted video
TxD	transmitter data
UART	universal asynchronous transmitter & receiver
VAC	video and attributes controller
VSYN	vertical sync
WDB	write data buffer
WE	write enable
WR	write strobe
XCTS	clear to send extension
XINTR	external interrupt
XRxD	receiver data, extension
50/60	50 Hz/60 Hz

For the write-from-cursor-to-pointer operation, the 2672's BLANK output is asserted automatically and remains asserted until the vertical retrace interval following completion of the command. The memory fill rate is one location per two character times, plus a small amount of overhead time.

In the shared and transparent buffer modes, the display buffer RAM is a part of the CPU memory domain and is addressed directly by the CPU. Both modes use the same hardware configurations with the CPU accessing the display buffer via three-state drivers (Fig.3). The processor bus request control signal (PBREQ) informs the 2672 that the CPU is requesting access to the display buffer. In response to this request, the 2672 raises bus acknowledge (BACK) until its bus external output (BEXT) has freed the display address and data busses for CPU access. BACK, which can be used as a hold input to the CPU, is then lowered to indicate that the CPU can access the buffer.

In the transparent mode, the 2672 delays the granting of the buffer to the CPU until a vertical or horizontal blanking interval, thereby causing minimum disturbance of the display. In the shared mode, the 2672 will blank the display and grant immediate access to the CPU.

When implemented in the row buffer mode (Fig.4), the 2672 halts the CPU and direct-memory accesses the next row of character data from the system memory to the row buffer memory during the first scan line (line 0) of each character row. The 2672 then releases the CPU and displays the row buffer data for the programmed number of scan lines. The bus request control signal (BREQ) informs the CPU that character addresses and the memory bus control signal (MBC) will start at the next falling edge of BLANK.

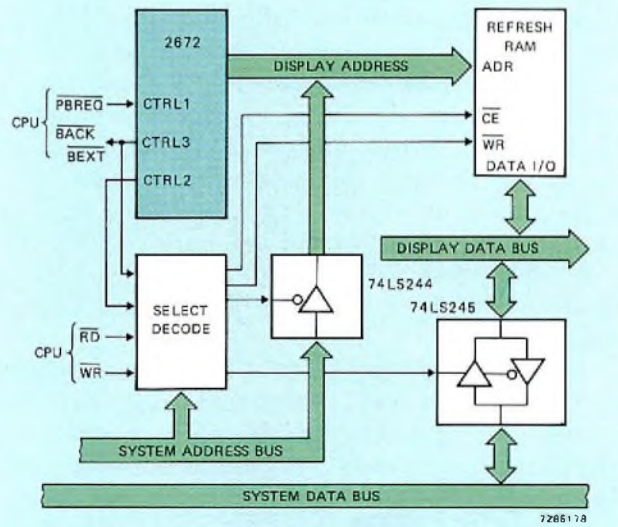


Fig.3 Both the shared and transparent buffer modes use this 2672 hardware configuration with the CPU accessing the display buffer via three-state drivers

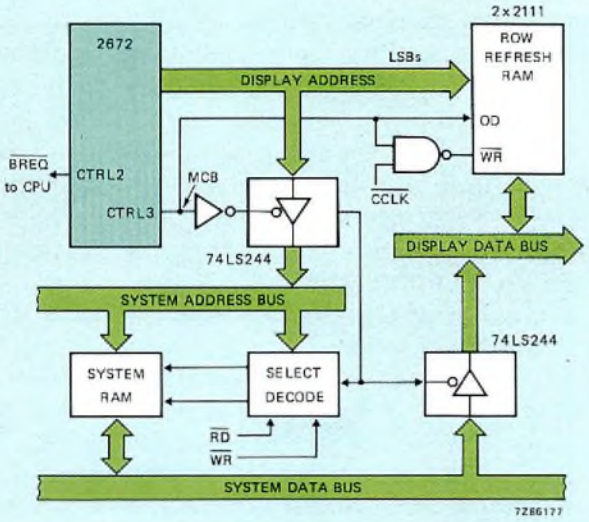


Fig.4 With hardware implemented in the row buffer mode, the 2672 halts the CPU and direct-memory accesses the next row of character data during the first scan line (line 0) of each character row

The CPU must release the address and data buses before this time to prevent bus contention. After the row of character data is transferred to the CPU, BREQ returns high to grant memory control back to the CPU.

2671 KEYBOARD AND COMMUNICATIONS CONTROLLER

The 2671 programmable keyboard and communications controller is a versatile keyboard interface and also functions as an asynchronous communications controller. The keyboard controller section provides scanning, debounce, and encoding for mechanical or capacitive keyboards. It can handle up to 128 keys, with any of four programmable rollover modes. A mask-programmable ROM supplies four levels of key encoding, corresponding to the separate shift and control input combinations. An eight-bit keyboard status register transmits status information to the CPU. Programmable features include rollover mode, scan rate and debounce time, coded or uncoded operation, and automatic repeat operation.

The communications sections of the 2671 is a universal asynchronous receiver and transmitter (UART). The receiver accepts serial input data and converts it to parallel-data characters. Simultaneously, the transmitter accepts parallel data from the CPU data bus and outputs it in serial form.

Received data is checked for parity and framing errors, and break conditions are flagged. Character lengths can be programmed as 5, 6, 7, or 8 bits (not including parity, start, or stop bits). An internal baud rate generator operating from an external clock or directly from a crystal can be used to derive one of 16 receive and/or transmit clocks. An eight-bit communications status register provides status information to the CPU.

The 2671 has an interrupt mask register that selectively enables keyboard and communications status bits to generate interrupts. Upon receipt of an interrupt acknowledge, a mask-programmable prioritised interrupt vector will be fed to the data bus, reflecting the source of the interrupt. Interrupt sources can also be determined by reading an interrupt register.

2670 CHARACTER AND GRAPHICS GENERATOR

The 2670 is a mask-programmable line-select display character and graphics generator. It contains 128 10 x 9 characters placed in a 10 x 16 matrix, and can shift characters that normally extend below the baseline (j, y, g, p, and q); effectively, the nine active lines are lowered within the matrix to compensate for the character's position.

Seven bits of an 8-bit address code are used to select one of the 128 available characters. The eighth bit acts as a chip-enable signal. Each character is defined by a pattern of logic 1s and 0s stored in a 10 x 9 matrix. When a specific 4-bit binary line address code is applied, a word of 10 parallel bits appears at the output.

Lines can be sequentially selected, providing a 9-word sequence of 10 parallel bits-per-word for each character selected by the address code inputs. As the line address inputs are sequentially addressed, the 2670 will automatically place the 10 x 9 character in one of two pre-programmed positions on the 16-line matrix with the positions defined by the 4-line address inputs. One or more of the 10 parallel outputs can be used as control signals to selectively enable functions such as half-dot shift.

The 2670 contains latches to store the character address and line address data. A control input is provided to inhibit character data output for certain groups of characters. The 2670 also includes a graphics capability, wherein the 8-bit character code is translated directly into 256 possible user-programmable graphic patterns. Thus, the 2670 can generate data for 384 distinct patterns (characters); 128 defined by the mask-programmable ROM plus 256 that are user-programmable.

2673 VIDEO TIMING AND ATTRIBUTES

The 2673 video and attributes controller is designed for raster-scanned CRT terminals and display systems. It contains a high-speed video shift register, field and character attributes logic, attribute latch, cursor format logic and half-dot shift control, and can be programmed for a light or dark screen background.

The 2673's visual attribute capabilities are reverse video, character blank, blink, underline, highlight, and light pen

strike-through or optional graphics. Each attribute has a separate control input which is latched internally when the AFLAG input is asserted. A second control input (AMODE) determines whether the attributes apply for only one character time (character mode) or remain valid until a new set of attributes is loaded (field mode). The attributes are double buffered on a row-by-row basis internally so that field attributes can extend across character row boundaries, eliminating the need to start each row with an attribute set.

The horizontal dot frequency is the basic timing input element to the 2673. Internally, this frequency is divided down to provide a character clock output for system synchronisation. Ten bits of dot data are parallel loaded into the video shift register on each character boundary. The video data are shifted out on three outputs at the dot frequency. The video output is a three-level signal representing low, medium, and high intensities. The three intensities are also encoded on two TTL-compatible video outputs (pins 29 and 30).

CRT TERMINAL FEATURES AND OPERATION

Only 15 IC packages are required for a minimum chip count CRT terminal using the new Signetics LSI chip set. The complete implementation includes all keyboard encoding and RS-232 level conversion for the serial interface (Fig.5). Despite this low chip count, the terminal provides many important features including:

- A display format containing 24 or 25 character rows and 80 characters per row.
- A character format consisting of a 7 x 9 dot matrix character in a 9 x 12 character block, 96 ASCII alphanumeric characters, 32 special symbols, block graphics, and a line-drawing character set.
- A cursor capable of underline or block cursor operation and optional blinking.
- A non-encoded keyboard that has 128 keys (maximum), including cursor control keys and a numeric keypad.
- An RS-232 compatible serial interface that has full or half duplex capability, 16 baud rates with internal baud rate generator, and character or block transmission options.
- Three operating modes; normal, transparent (displays graphic and control characters), and page or scroll with optional smooth scroll.
- Five visual attributes; blink, reverse video, highlight, underline, and non-display.

To minimise hardware requirements, this design uses the 2672's independent buffer mode. The dual port interface to the 2K x 8 display buffer is via a Signetics 8X31 bidirectional latch such as the 74LS374 if the CPU is not required to read the contents of the RAM.

The 2672, responding to commands from the CPU, completely controls data transfers between the CPU and display memory and avoids display interference by performing the display memory accesses only during blanking intervals. For massive display updates (clear, screen, load form, etc.), the 2672 is instructed to blank the display and service the data transfer immediately and continuously. An interrupt from the 2672 informs the CPU when an operation is completed.

The 2672 addresses the display buffer memory, which contains both characters and attribute data. Software identifies an attribute byte by setting bit 7 of the byte to a logic 1. The RAM data outputs are applied to the 2670, which provides the character dot data information, and to the 2673.

The 2673 is hard-wired to operate in the field-attributes mode for this application. An attribute character occupies a screen position but is not displayed unless the 2673's ACD input is asserted. When bit 7 on the RAM data bus is 1, the attribute byte is latched into the 2673, beginning a new attributes field. Since the attributes are double-buffered in the 2673, only one byte (at any character position) is required to specify a field.

The bipolar 2673 serialises the dot data from the 2670 into a 17.5-MHz data stream for the monitor. Two TTL-level video outputs provide three levels of video; black, white, and grey.

The 2671 provides the asynchronous data communications link at one of 16 selectable baud rates. The 2671 addresses a 74159 4-to-16 decoder to drive a 16 x 8 matrix keyboard. Key depressions are detected on the KRET input from a 74LS151 8-to-1 multiplexer. Each key depression is debounced, encoded according to the states of the SHIFT and CONTROL inputs, and presented to the CPU. Repeat and typomatic (auto-repeat) functions are processed automatically by the 2671.

The operating program for this terminal is contained in the internal ROM of the 8049 microcomputer which also provides the RAM required by the system program. Since the majority of the terminals's features are tailored by firmware, the ROM size can be internally or externally increased to support additional functions. Signetics will make available a pre-programmed 8049 microcomputer containing the operating firmware for this terminal.

Buffer memory allocation and scrolling

The minimum chip count terminal's 2 Kbytes of available buffer memory are allocated as follows (all addresses are in hexadecimal):

- 0000 to 004F, display data for row 25, status line
- 0050 to 007F, not used
- 0080 to 07FF, display data for rows one to 24.

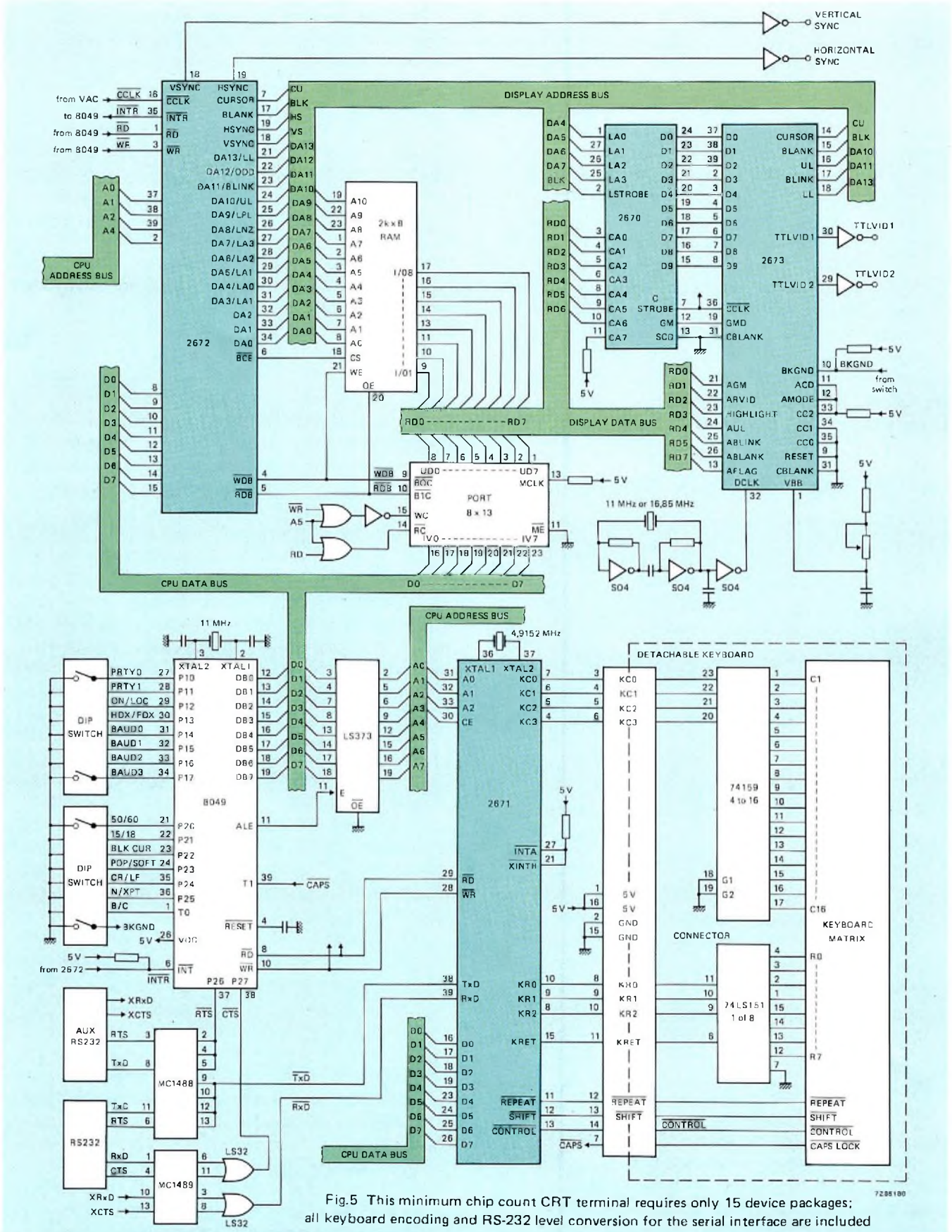


Fig.5 This minimum chip count CRT terminal requires only 15 device packages; all keyboard encoding and RS-232 level conversion for the serial interface are included

The 2672's display-buffer-first-address and display-buffer-last-address registers are loaded with the values 0080 and 07FF respectively, causing this part of the RAM to act as a circular buffer. Here is how the display data is initially organised in the RAM:

0080 to 00CF, row 1 data

00D0 to 011F, row 2 data

–

07B0 to 07FF, row 24 data

0000 to 004F, row 25 data (status line)

When a scroll operation is required, the CPU changes the value in the 2672's screen-start register from 0080 to 00D0. This effectively shifts the displayed data up one row. Upon reaching the specified last buffer address (which is now the last character in row 23), the 2672 automatically changes the addressing sequence to resume starting at 0080 for the 24th row. The display data is now organised:

00D0 to 011F, row 1 data

0120 to 016F, row 2 data

–

07B0 to 07FF, row 23 data

0080 to 00CF, row 24 data

0000 to 004F, row 25 data (status line)

The CPU can clear the previous data in 0080 to 00CF so that a blank row appears in the 24th position.

The status line (row 25) data is kept in a separate section of RAM to eliminate moving the data whenever the scrolling operation just described occurs. Thus, the 2672 must be instructed to change its addressing sequence at the beginning of the 25th row. This is accomplished with the 2472's split-screen-row-interrupt capability.

The split-screen-interrupt-row register, IR10, is initialized to issue an interrupt at the beginning of row 24. The CPU responds to this interrupt by changing the value in the screen start register to 0000. The 2672 then uses this value as the starting address of the next (25th) row, causing the status line to be displayed in that position. The CPU must re-load the screen-start register – before the vertical blanking interval ends – with the correct value for the first character to be displayed on the screen.

Basic software considerations

The software for a microcomputer-based CRT terminal is closely tied to the system hardware configuration and its characteristics. If interrupt-driven operation is desired, the system hardware/software design must be capable of prioritising the interrupts so that the system will correctly service interrupts from different sources.

In a typical system, there are three interrupt sources: the keyboard, the communications interface, and the video timing controller. (The latter must usually be assigned the highest priority since failure to service its interrupt promptly may result in visible perturbations of the display.) The keyboard and datacomm interrupts can, in most cases, absorb some time delay before they are serviced since they include one or more data buffer levels.

After application of power, the terminal's microprocessor first performs a five-part system initialisation routine:

- clear the microcomputer's scratchpad RAM
- initialise the CRT controller for the desired screen format, monitor timing parameters, cursor parameters, and display-start address
- clear the CRT display by loading a non-display-code (usually an ASCII space, 20 hex) into the buffer memory
- initialise the keyboard and serial interfaces
- read any mode switches (e.g., full or half duplex, baud rate, cursor type, etc.) and set system parameters as required.

The processor can now enable its interrupts and wait in a loop until an interrupt is received. When this happens, the processor first determines the source of the interrupt and then performs the required system operation.

An interrupt from the CRT timing controller usually indicates that some information is required for proper screen refresh operation. For example, the 2672 may issue a split-screen interrupt to indicate that a new address must be loaded into its screen-start registers if the next character row is to be displayed from other than the next sequential address in memory. The CPU must service this interrupt within a finite time in order for the display to operate correctly.

An interrupt from the keyboard interface may be a displayable character or a control function. Displayable characters are usually transmitted to the host computer and also put into the buffer memory for display on the terminal. Certain control characters, such as cursor-control keys or keyboard-error codes, cause only local actions, while others require transmission to the host.

An interrupt from the data communications interface may also be a displayable character or a system-control character. In either case, the microprocessor must determine the type of character and perform the necessary system operation.

Because the terminal's 8049 microcomputer provides only a single interrupt level, a totally interrupt-driven software design can not be used. The single interrupt level is assigned to the 2672 to service the split-screen interrupt just described and implement the smooth-scroll feature. The keyboard and datacomm functions are serviced by polling the 2671's status register. Both the keyboard interface and UART receiver are double-buffered in the 2671, preventing overrun even if they are not serviced immediately.

At system reset, the 8049 interrupts are disabled, data memory and display memory are cleared to 0's, and both the 2672 and 2671 are master-reset through software commands. The system option switches are then read and stored and the 2672 and 2671 internal registers are initialised for the selected operation. Finally, the initial data for the status line is loaded, the 2672, UART, and keyboard are enabled, and the CPU interrupt is enabled.

The program then enters a loop where the 2671 is checked for keyboard or UART entries. If an entry has occurred, the character is fetched and stored in a software-controlled first-in-first-out (FIFO) memory, which is eight bytes deep, for both receiving or transmitting characters.

There are two FIFOs, and if either has an entry, the program proceeds to a chracter recognition routine which checks for the type of character (displayable or control) and the appropriate handling subroutine (ESC sequence, control sequence, cursor control, character display, etc.) is called. If both FIFOs are empty, the polling routine checks the option switches for any changes since reset entry. If changes are present, the system is reconfigured as necessary.

The need for FIFO's results from the clear row function required when a scroll is performed. Although the 2672 includes a clear-from-cursor-to-pointer command that can be used to clear a block of memory rapidly, the display is temporarily blanked during this operation, causing undesirable flashes. Instead, the program does the clear row function by a repetitive loop using the write-at-cursor-and-increment command.

Since the write occurs only once per scan line during the active display window, a worst-case total of about 80 scan line times is required to execute the routine. This limits the maximum received character rate to about one per 80 scan lines or 240 characters per second (2400 baud). To overcome this limitation, the 2671 is also polled each time through the clear-line-subroutine loop, and any entries from the receiver or keyboard are stored in the appropriate FIFO.

Since the FIFOs are eight deep, eight characters can be received in the same time, increasing the theoretical maximum baud rate to 19200. (Other program limitations reduce this to 9600 baud.) However, this does not increase the rate at which scroll function characters (such as a line feed) can be received. Each character of this type must be followed by "fill" characters if data rates higher than 2400 baud are used.

An interrupt from the 2672 will occur when the display scan reaches the row count programmed in its split-screen address register (row address 23 for the 24th row). In response to the interrupt, the CPU loads the screen-start registers with the address of the status line (0000) and enables the 2672's line-zero interrupt. This causes another interrupt when the status line display begins. At this time, the CPU reloads the screen-start register with the proper address to begin the next display frame and disables the line-zero interrupt.

SOFT SCROLLING AND TIMING CONSIDERATIONS

If scrolling is required, the screen-start register value is incremented by 80 (cutting off the top row) and the effective bottom row is cleared to nulls. When soft scrolling is selected, additional functions are performed during the interrupt routines. To begin this operation, the line-zero-interrupt routine adds ten lines to the normal vertical "back porch". This causes the next active screen display to begin ten scan lines later than normal and gives the effect of the display moving up two scan lines (12 lines per character row minus 10) instead of jumping up all 12 character lines at once.

However, if nothing else were changed, the bottom of the display would move down ten lines. Thus, during the row-24 interrupt, the number of scan lines per character row is changed to two (12−10), causing only the first two scan lines of that row to be shown. The next line-zero interrupt (at row 25) restores the lines-per-row count back to 12, which keeps the whole status line showing. During this interrupt, the value added to the vertical back porch is changed to eight scan lines. The display moves up two more scan lines and at the next row-24 interrupt, four scan lines are shown. The process is continuous, providing the soft-scan effect over the entire display (except for the status line), smoothly scrolling at a rate of one row each six frames, or every tenth of a second.

Another design phase task required by the terminal is selecting a suitable monitor and then calculating the 2672's register values that provide suitable monitor drive signals. Begin by calculating the required horizontal scan frequency.

Each character is contained in a 9-dot by 12-line field. Since there are 25 display rows, there will be 12 x 25, or 300 active scan lines. Next, add some scan lines for the vertical flyback (typically 5 to 10% of the active scan lines). For a screen refresh rate of 60 Hz, the horizontal frequency = 60 x 300 x 1.1 = 18 900 Hz.

A Motorola monitor appears to do the job. Its major timing specifications are:

- horizontal frequency, 18.72 kHz ±500 Hz
- horizontal flyback, 8 μs (max)
- horizontal sync width, 4 μs (min)
- vertical frequency, 50/60 Hz
- vertical flyback, 750 μs (max)
- vertical sync width, 50 μs (min).

Monitoring timing definitions are detailed in Fig.6.

The Table 3 worksheet is used to compute the required timing and associated 2672 register values. Some rough guesses are required initially and several reruns through the worksheet will usually be required to arrive at final values. For example, the character clock period must be known to select the horizontal front porch (HFP), horizontal sync

width (HSYNC), and horizontal back porch (HBP) values. An initial approximation of the character period would be:

- horizontal period = 1/18 900 = 52.9 μs
- horizontal active = total − blank = 52.9 − 10 = 42.9 μs
- character period = 42.9/80 ≈ 0.53 μs.

TABLE 3
CRT timing worksheet

1.	Horizontal character block (number of dots)	9	
2.	Vertical character block (number of scan lines)	12	(IR0)
3.	Vertical refresh rate, Hz	60	
4.	Characters per row	80	(IR5)
5.	Character rows per screen	25	(IR4)
6.	Total active video scan lines (step 2 X step 5)	300	
7.	Vertical front porch (number of scan lines)	4	(IR3)
8.	Vertical back porch (number of scan lines)	12	(IR3)
9.	Vertical flyback interval (step 8 + 3)	15	
10.	Total scan lines per frame (add steps 6, 7, and 9)	319	
11.	Horizontal rate, kHz (step 3 X step 10)	19.14	
12.	Horizontal front porch (character time units)	5	
13.	Horizontal sync width (character time units)	8	(IR2)
14.	Horizontal back porch (character time units)	9	(IR2)
15.	Horizontal flyback interval (step 13 + 14)	17	
16.	Total character time units in one horizontal scan line (add steps 4, 12, 13, and 14)	102	
17.	Equalising constant ([step 16/12] − [2 X step 13])	35	(IR1)
18.	Character clock rate, MHz (step 16 X step 11)	1.95228	
19.	Character period, μs (1/step 18)	0.512	
20.	Scan line period, μs (step 19 X step 16)	53.27	
21.	Dot clock rate, MHz (step 18 X step 1)	17.57052	

parameter	specified	actual
Horizontal rate, kHz	18.72	19.14
Horizontal flyback time, μs	8	8.7
Horizontal sync width, μs	4	4.1
Vertical rate, Hz	50-60	60
Vertical flyback time, μs	750	784
Vertical sync width, μs	50	157

In calculating horizontal timing, an approximate ratio of 1:2:2 for HFP:HSYNC:HBP is recommended.

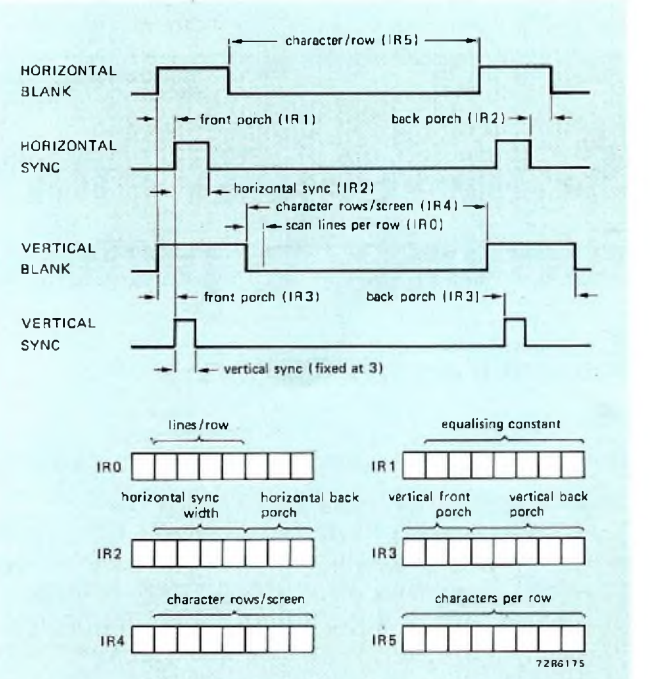


Fig.6 The minimum-chip-count terminal's 8049 microcomputer provides only a single interrupt level. Access to the keyboard and communication routines occurs through polling. A totally interrupt-driven software design with multi-level interrupts, as shown here, cannot be used

Demonstration model of an intelligent display terminal controller using the described integrated circuits

ACKNOWLEDGEMENT

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After a quarter century of development the shadowmask picture tube has reached a point at which further refinement of its electron optics promises only marginal improvement of picture quality. Thanks to the present excellence of the electron optics, however, it is now possible to take advantage of a simple, long-known circuit technique for enhancing the sharpness of the picture.

Scan-velocity modulation increases tv picture sharpness

G. HAENEN and H. SIMONS

Modulating the scan velocity in a tv receiver in accordance with variations in the video signal is not new. Long known as a means of increasing picture sharpness, scan-velocity modulation (or SVM) could be used to maximum advantage only with the introduction of the latest high-performance picture tubes such as 30AX. Before then, the improvements in picture quality offered by SVM were overshadowed by those arising from improved electron-gun and deflection-coil design.

Now, however, picture-tube design has advanced so far that attention has again turned towards SVM as a means of providing just that bit extra in picture quality. To this end, two new deflection-yoke assemblies – the AT1261 and AT1271 – incorporating an auxiliary coil for SVM are now available for 30AX colour picture tubes. All that is needed to operate with these new yokes is some simple driving circuitry, preferably in modular form, and slight changes to existing circuitry.

Before describing this, however, let's consider how scan-velocity modulation works.

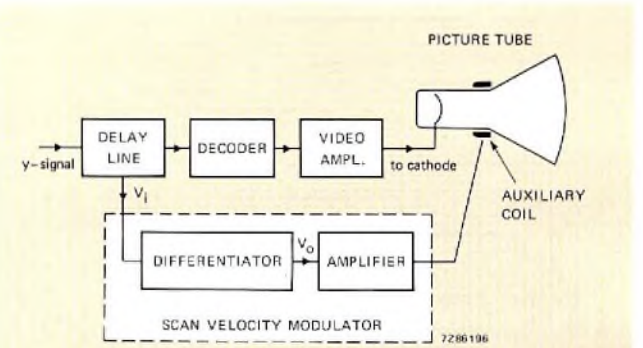


Fig.1 Block diagram showing the basic SVM setup

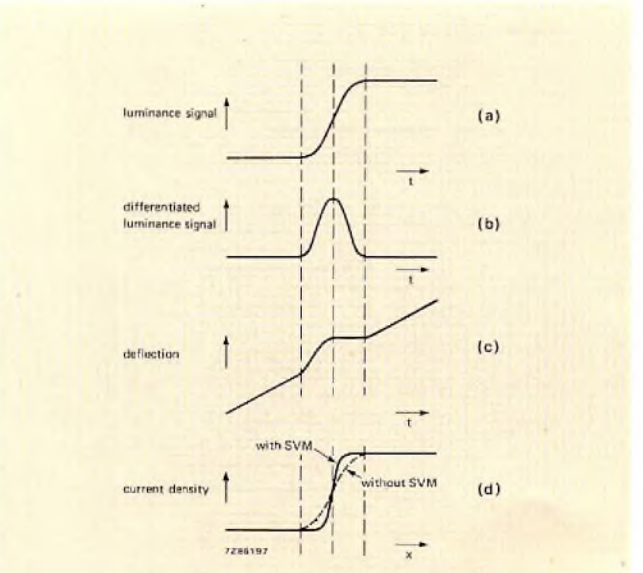


Fig.2 (a) Signal tapped from the luminance delay line;
(b) Output signal from the differentiator;
(c) Line deflection as a function of time;
(d) Current density on the screen

SVM CONCEPT

Figures 1 and 2 illustrate the basic idea behind SVM. A signal (V_i) representative of the intensity profile across the picture – the luminance signal for example (Fig.2(a)) – is differentiated (Fig.2(b)) and passed to an auxiliary deflection coil. This coil modulates the horizontal deflection field and hence the scan velocity (Fig.2(c)) to accentuate changes in picture intensity (Fig.2(d)). In this way, positive and negative-going intensity changes in the tv picture are sharpened.

The improvement that can be attained is demonstrated by Fig.3 which compares the tv picture produced by a 30AX picture tube operating in conventional mode, with that produced by the same tube with SVM.

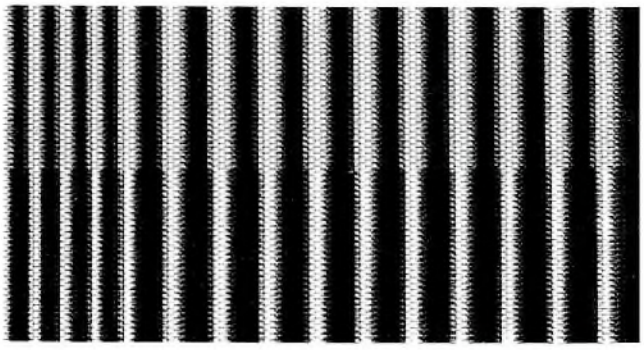


Fig.3 Test pattern (to scale) produced by a 30AX tube operating in conventional manner (top) compared with that produced in the same tube using SVM

SVM MODULE

Figure 4 shows the basic circuit of the SVM module, and Fig.5 the print board. The demodulated luminance signal, without the chrominance and sound signals, is taken from a tap on the luminance delay line, and passes via an emitter-follower to the differentiator – a simple RC network. The differentiated signal passes to a two-stage preamplifier, and then to a class B output stage a.c. coupled to the auxiliary deflection coil.

The output signal is proportional to the strength of the luminance signal. For weak video signals the a.g.c. will amplify the background noise, which would then be accentuated by the SVM circuit. Moreover, high amplitude pulses in the luminance signal might overload the output stage, causing damage to the output transistors and, at the very least, deterioration of picture quality. The module therefore incorporates a clipping circuit to limit the output signal from the differentiator.

For periodic changes in signal intensity, e.g. of the form $V_i = A \sin \omega t$, where A is the amplitude of the luminance signal and ω is its angular frequency, the output signal will be $V_o = RC\omega A \cos \omega t$. The output signal will therefore increase with increasing ω, so that high-frequency changes in picture intensity will be more greatly affected. Experience indicates, however, that high-frequency changes need to be accentuated less. For this reason, the differentiator/pre-amplifier combination is designed to introduce a high frequency roll-off (at about 3.5 MHz). Moreover, the RC product of the differentiator is chosen to provide a response only over a limited frequency range, so that low frequency changes remain unaffected.

Note: the demodulated luminance signal is the obvious choice for SVM in view of the simplicity it provides. Ideally, transients in the red, green and blue channels should be dealt with separately, but this would require more complicated circuitry.

TELETEXT RECEPTION

The rise and fall times of the digitally produced teletext signals are already so fast that there is little need for SVM

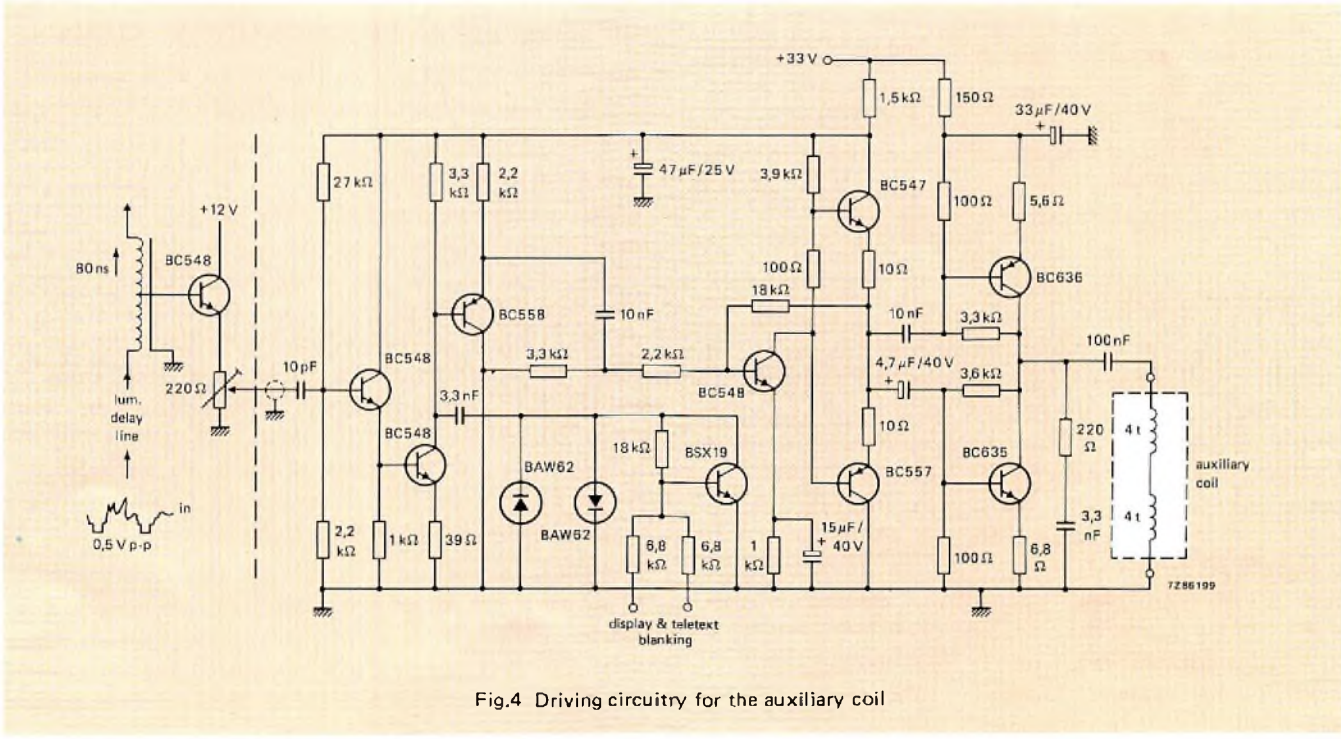


Fig.4 Driving circuitry for the auxiliary coil

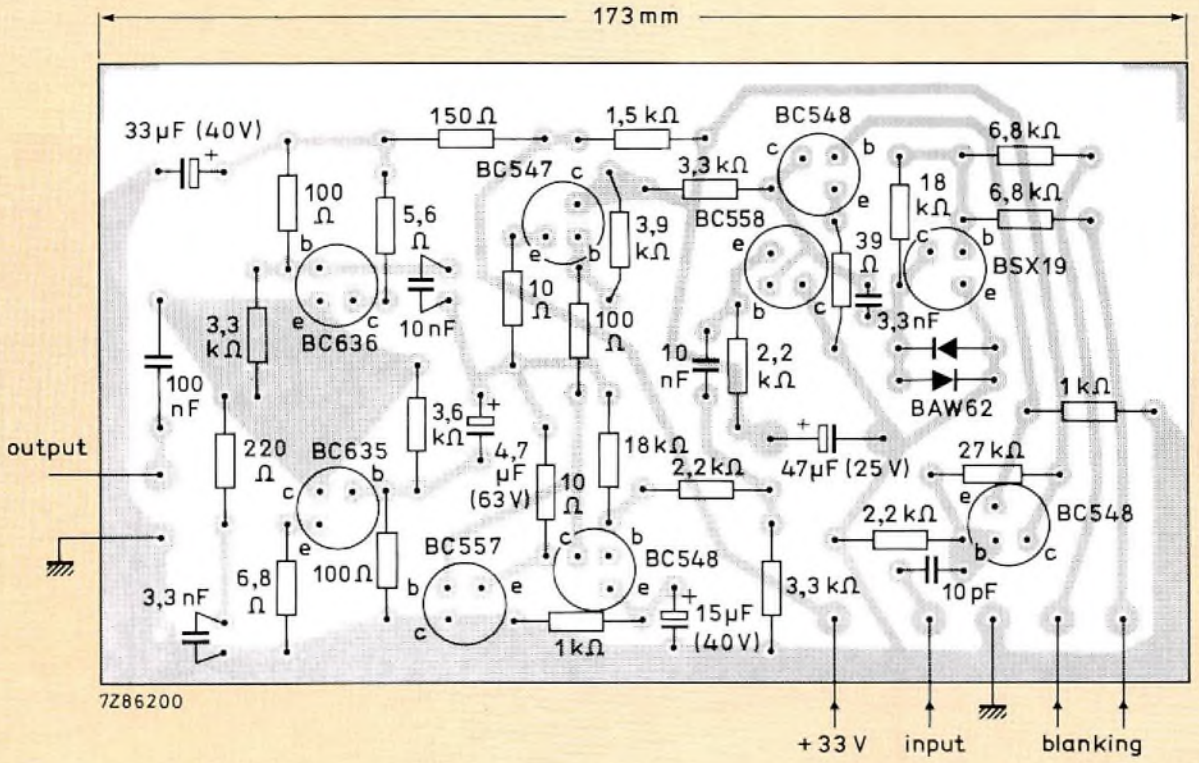


Fig.5 Print board for the SVM module

during teletext reception. Moreover, the SVM system described here only responds to the luminance signal derived from normal programme reception, so if operated during teletext reception, the system would superimpose this signal on the teletext picture. During teletext reception therefore, the SVM module can be switched off by the application of a blanking pulse.

AUXILIARY COIL

The auxiliary coil is recessed in the inner surface of the deflection coil former. Figure 6 shows its construction. It comprises two series-connected subsidiary windings, each of four turns printed on foil. Each subsidiary winding subtends an angle of 120° to minimize its influence on beam convergence.

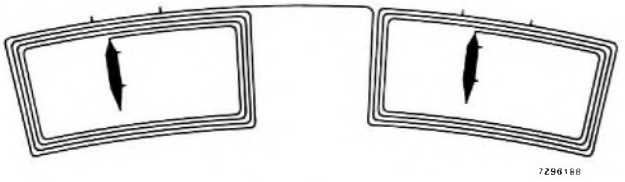


Fig.6 Auxiliary coil

CONSEQUENCES FOR EXISTING SYSTEMS

Adapting a current receiver design to SVM necessitates certain modifications to existing circuitry, as well as the use of a new deflection yoke.

Signal delay. For proper operation of the SVM circuit, signals passing to the auxiliary coil must coincide with those that pass to the picture tube cathode via the video decoder and preamplifier. This may necessitate modifying the delay lines in current systems.

For example, in a typical receiver using a 30AX picture tube, the transit time of the luminance signal from the output of the luminance delay line to the picture tube cathode is about 100 ns. The total delay produced by the SVM system is about 180 ns, so the luminance delay line should be provided with a tap for the SVM system at a distance corresponding to 80 ns from its output.

Position of the 4.43 MHz chrominance trap. In conventional tv receivers, the 4.43 MHz trap filtering the chrominance signal is located on the output side of the luminance delay line. This trap must now be connected to the input of the luminance delay line to ensure that the SVM module receives a filtered luminance signal.

Supply for the SVM module. The SVM module can be driven directly by the 33 V supply of the vertical deflection circuit. To facilitate this the module has an additional smoothing circuit to reduce the effects of frame ripple.

Module connections. The SVM module has two connectors: a two-pin connector for connecting the module to the auxiliary coil, and a five-pin connector for the input signal, the teletext blanking signal and the supply.

Note: for maximum stability and to minimise radiation, the emitter-follower circuit at the input of the differentiator must be as close as possible to the tap on the delay line. For this reason it is not located in the SVM module.

SUMMARY

The use of SVM can produce significant improvements in tv picture quality, and can do so at little extra cost. All that is needed is a new deflection yoke assembly incorporating the auxiliary coil, plus some slight addition to the existing circuitry.

The table gives the specifications of the SVM system.

System specifications

Auxiliary coil:	
inductance	3.5 μH
resistance	2.5 Ω
East-west sensitivity	
at screen centre	2.2 mm/A
at ends of horizontal axis	4.5 mm/A
Supply voltage	33 V
Supply current:	
average test picture	20 mA
cross-hatch picture	27 mA
noisy picture	50 mA
Power dissipation:	
average test picture	0.7 W
cross-hatch picture	0.9 W
noisy picture	1.5 W
Mains interference:	max. increase of mains interference level less than 10 dB with test picture generator PM5544.
Sensitivity:	with test pattern produced by PM5544 generator, a video input voltage of 80 mV produces a maximum output current of 600 mA p-p in the auxiliary coil.

With cathode-ray tubes becoming as common a feature of the office landscape as the ficus and the filing cabinet, data systems designers need to acquaint themselves better with these still-indispensable survivors of the pre-solid-state era. Good display terminal design rests on good understanding of the relations between character size, definition and packing density; screen size, luminance and contrast; and the effects of ambient lighting.

Cathode-ray tube requirements for data-graphic displays

Data-graphic displays can take advantage of cathode-ray tube technology that has benefited from three decades of television. A typical display might have a capacity of about 2000 characters, each sited in a cell of, say, 126 elements, making a total of 250 000 elements. The elements must be uniformly spaced and capable of being selectively lit. They are addressed by scanning the electron beam of the CRT, a process which is simple to implement, flexible in use, and tolerant of many errors. The system employed almost universally is the raster-generated display, similar to that used in tv receivers. Field frequency determines refresh rate, and the number of lines required for the display of information determines the ratio of line frequency to field frequency. The diameter of the electron beam sets the size of the elements.

The system possesses great flexibility. It is fairly easy to alter the scanning frequency to change the number of addressable sites. Adjustment of scan amplitude varies the size of the display within the boundaries of the useful screen area. The brightness of the display can be adjusted by changing the bias voltages applied to the CRT.

By its nature the system is very tolerant of certain errors. For instance, the luminance of the screen may vary by as much as 20% between the centre and the corners, but the transition is gradual and hardly perceptible. However, in a display consisting of individual elements (LEDs for example), a change in brightness between two neighbouring elements of 3% could not be tolerated and they would have to be matched to within 1%. Similarly, a departure from linear scan of several percent, provided it is gradual, can easily be accepted.

The following classification based on the amount of data displayed has been in use for some time and applies equally to monochrome and colour displays.

Basic display: about 40 characters per row and 1000 characters per screen. The rows are written parallel to the longer axis of the screen (tv or postcard format). Teletext, viewdata, and home computers are typical examples.

Half-page display: about 80 characters per row and 2000 characters per screen. As in the case of basic displays, tv format is used. This type of display is intended for administrative applications, word processors, home computers, etc.

Full-page display: at least 5000 characters in rows parallel to the shorter axis of the screen. The application is primarily word processing.

In most cases, the display is viewed by one person at a distance of about 0.4 m, which fixes the sizes of the characters. The size of CRT needed depends on the total number of characters to be displayed. For example, basic-displays use 9 in and 12 in tubes, half-page displays use 12 and 15 in tubes, and full-page displays use 15 in and larger tubes. Communal viewing – for instance, announcement displays in airports, railway stations, hotels, etc. – may demand 20 and 26 in tubes, and large projection installations may be required in special applications.

DISPLAY AREA

Character matrix and character cell

In raster-generated displays, each character is formed on a matrix of dots by unblanking the electron beam to 'bright-up' the required dots. A character matrix of 5 x 7 dots has been used in many displays but a recent trend is towards a 7 x 9 matrix for better legibility (Ref.1). Spaces between adjacent characters ensure that they remain individually

legible. An additional two or three rows of dots are made available to allow for descenders when lower case letters are required. If the text has to cover languages other than English, provision must be made for diacritical marks. For some languages, special letters must be formed; Far-Eastern languages are particularly demanding in this respect (Ref.2).

The character matrix is placed in a larger character cell to provide for these contingencies. For instance, in teletext systems the 5 x 7 character matrix occupies a 6 x 10 character cell as shown in Fig.1. In a modern 80 character/row display, the 7 x 9 character matrix may occupy a 9 x 14 character cell. This allows two spaces between characters in the horizontal direction, two lines between rows of characters, and three lines for descenders.

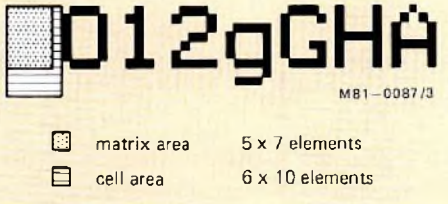


Fig.1 Alphanumeric characters used in teletext

Fig.2 Composition of teletext graphics

Graphic displays

There are two distinguishable types of graphic display which are sometimes referred to as character graphics and dot graphics. Character graphics employ character cells similar to those used to construct alphanumeric characters. Examples of graphic 'characters' as used in teletext are shown in Fig.2; these can be used to construct bar charts, graphs, maps, etc. Characters depicting suits of playing cards, chess pieces, etc. can be used for games and in personal computers.

Addressing every dot of the display individually (dot graphics), gives much better pictorial representation and greater flexibility but vastly increases the demand on the data display store.

Useful screen area

A little detail lost at the edge of a tv picture is unlikely to be missed but no information may be lost from a data display. For that reason the area assigned to a data display is smaller than the useful screen area. There are no fixed

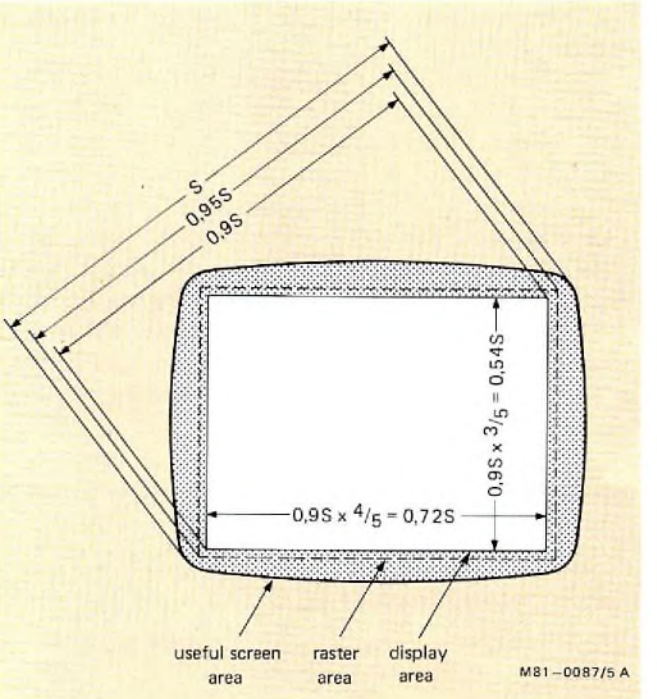


Fig.3 Suggested allocation of screen area

rules about this, but the relation shown in Fig.3 is a good rule of thumb. Here the information is confined to a rectangular area with an aspect ratio of 3:4 whose diagonal is 90% of the useful screen diagonal S quoted in the published data of the tube. The horizontal measure, H, of this area is

$$H = 0.9S \times 4/5 = 0.72S$$

and the vertical measure, V, is

$$V = 0.9S \times 3/5 = 0.54S$$

Table 1 lists V and H for four commonly used tube sizes.

TABLE 1
Screen dimensions in mm

tube type	width	height	diagonal(S)	H	V
M24-300	198	149	228	164	123
M31-330	254	201	292	210	158
M31-320	257	195	295	212	159
M38-328	292	227	352	253	190

FREQUENCY AND TIMING

Raster formation

Line scan is normally horizontal and field scan vertical. The number of lines, N, in the raster determines the ratio of the horizontal and vertical deflection frequencies, f_h and f_v.

For a non-interlaced raster $f_h/f_v = N$, and for an interlaced raster $f_h/f_v = N/2$.

The choice of deflection frequencies poses conflicting requirements. To minimise the bandwidth and system logic speed required, it is desirable to keep f_h as low as possible for a given value of N, but the lower limit of f_v is set by flicker. Setting f_v at or just above mains frequency eases some difficulties with hum and stray magnetic fields, but to avoid flicker the present tendency is toward frequencies as high as 100 Hz. Interlacing halves the horizontal deflection frequency required for a given number of lines, but because of the closeness at which data displays are usually watched an interlaced raster is not so unobtrusive as it is in television. Increasing f_v to eliminate interlace jitter conflicts with the aim of keeping bandwidth and system logic speed low; choosing a long persistence phosphor leads to some loss of resolution.

Scan waveform timing

The flyback factor p is a commonly quoted parameter of timebase circuits and is defined as

$$p = \tau_f/T$$

where τ_f is the flyback time and T the period. Typical values might be $p_h = 0.16$ for the line timebase and $p_v = 0.04$ for the field timebase. The ratio q of blanking time τ_b to the period can be similarly defined as

$$q = \tau_b/T$$

Because the raster area is made larger than the display area (see Fig.3) to allow for spreads in flyback time, non-linearities of scan at the beginning and end of scan, and any positional drift, the blanking time is longer than the flyback time; q_h is usually about 0.21 and q_v about 0.08. The time available for writing information τ_w is

$$\tau_w = T(1 - q)$$

Because blanking and flyback ratios differ from one display to another, a logic circuit designed to work with one display will not necessarily work with another having the same deflection frequencies.

Bandwidth and clock frequency

In the equations that follow,

m_h = number of elements in a character cell in the horizontal direction

m_v = number of elements in a character cell in the vertical direction

C_h = number of characters per row

C_v = number of rows per page

Non-interlaced operation is assumed.

The number of scanned lines n_v occupied by text is:

$$n_v = m_v C_v = N(1 - q_v)$$

where N is the total number of lines in a raster; therefore

$$N = \frac{m_v C_v}{1 - q_v}$$

Substituting this for N in the relation $f_h = Nf_v$ gives

$$f_h = \frac{m_v C_v f_v}{1 - q_v}$$

The time required to write one row of character elements is

$$\tau_{wh} = \tau m_h C_h$$

where τ is the duration of one element. Then, since $\tau_{wh} = T_h(1 - q_h)$ and $T_h = 1/f_h$,

$$\tau = \frac{1 - q_h}{f_h m_h C_h}$$

Although it is desirable to have as short an element bright-up rise time as possible, experience indicates that acceptable results are produced when the rise time τ_r is one-third of the pulse duration time τ. Thus,

$$\tau_r = \frac{\tau}{3} = \frac{1 - q_h}{3 f_h m_h C_h}$$

The relation between the rise time and the 3 dB bandwidth B_3 is given by

$$B_3 \approx \frac{1}{3\tau_r} = \frac{f_h m_h C_h}{1 - q_h}$$

The clock frequency for the logic is $1/\tau$.

CONTRAST, LIGHT OUTPUT, AND BEAM CURRENT

If the room in which a display is situated has illumination of E lux, and the reflectivity of the surfaces near the display is r_s, then the luminance of these surfaces, in candela per square metre, is

$$B_s = r_s E/\pi \qquad (1)$$

A similar situation applies to the picture tube when the phosphor is not excited and the ambient light is reflected from it with a reflectivity r_p. However, to reach the phosphor the light has to pass through the faceplate (transmission T_g) and, on reflection, return through the faceplate (Fig.4). Therefore, the luminance of the phosphor screen due to external illumination E is

$$B_E = r_p T_g^2 E/\pi$$

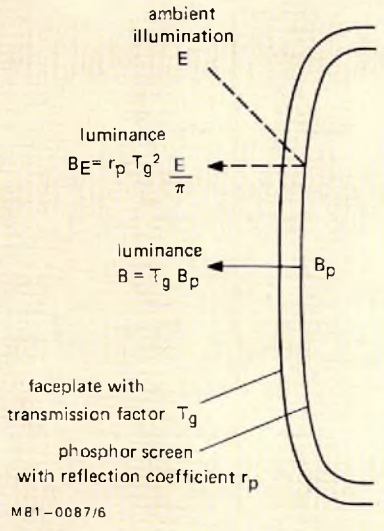


Fig.4 Ambient illumination, screen luminance, and contrast

In the absence of external illumination, if the screen is excited by the electron beam to produce a luminance B_p, then the luminance after passage through the faceplate is

$$B = T_g B_p$$

With no external illumination, the contrast C of the picture tube is high (about 100), but in the presence of ambient illumination it falls to

$$C = \frac{B + B_E}{B_E} = 1 + B/B_E = 1 + \frac{\pi B}{r_p T_g^2 E} \qquad (2)$$

This equation illustrates an important aspect of picture tube operation. To improve contrast, the ratio B/E must be increased, either by increasing B, by reducing E, or both. The contrast can also be improved by reducing T_g. Since a reduction in the glass transmission factor affects B, the overall improvement is approximately proportional to $1/T_g$. Reducing the reflectivity r_p of the screen is another way of improving contrast. The black matrix used in colour picture tubes and pigmented phosphors are examples of this.

In illumination engineering, the aim is to provide uniform illumination over a working area so that the eye does not have to adapt to differences of luminance as it focuses on different objects. This implies that the peak brightness of a display should be about equal to the brightness of the surroundings; that is, $B = B_S$. Substituting in Eq.2 for π/E from Eq.1, gives

$$C = 1 + \frac{r_s B}{r_p T_g^2 B_S}$$

For C = 10, which is a good value of contrast, and on the assumption that $B/B_S = 1$,

$$T_g = \frac{1}{3}\sqrt{\frac{r_s}{r_p}}$$

In practice, the reflectivity of the phosphor screen is about 0.8, and the reflectivity of surrounding surfaces about 0.6; thus $T_g = 0.289$. This explains why a twin-panel tube with an overall value of $T_g = 0.28$ gives a better display than a monopanel tube ($T_g \simeq 0.5$), particularly in the presence of high ambient illumination.

To ensure that $B = B_S$ at high levels of ambient illumination, say 500 lux, Eq.1 sets B at 96 cd/m^2 with $T_g = 0.289$ for optimum contrast. This corresponds to 164 cd/m^2 on a monopanel tube. The values of brightness often specified are 100 cd/cm^2 for twin-panel tubes and 170 cd/m^2 for monopanel tubes. Twin-panel tubes are clearly more suitable than monopanel tubes at ambient illumination around 500 lux.

To obtain an estimate of the required beam current and video drive, consider a 15 in tube with a display area 25 cm x 19 cm. This means that at a specified screen luminance of 170 cd/cm^2 the total luminous flux is 25.4 lm. If the tube has a faceplate transmission factor of 0.5, the total luminous flux of the phosphor screen must be 50.8 lm. The quoted luminous efficiency of P31 phosphor is 45 lm/W, so, assuming this is used, the power input to activate the full phosphor screen at the necessary peak brightness to meet the 170 cd/m^2 specification will be 1.13 W. At an e.h.t. of 17 kV, this implies a beam current of 68 μA. Assuming the worst-case conditions, that is, the tube is an end-of-manufacturing-spread specimen with respect to cut-off (110 V) and is operated at the highest permissible value of V_{g2}, the required video drive is 26 V.

RESOLUTION AND SIZE

Line and dot resolution

The light-intensity distribution of an aberration-free cathode-ray tube spot is approximately gaussian. The boundaries of the spot are therefore not clearly defined but its diameter d will be taken as twice the standard deviation (2σ) of a gaussian distribution. This corresponds to points at 60% of maximum and conforms with the 'merging raster' method of resolution assessment in which resolution is stated as the number of lines per screen height at which the lines merge. When the spot is scanned into a line, the luminance profile of the line remains gaussian (Ref.3).

The contrast between the peak brightness of the lines of a raster and 'peak darkness' between the lines is known as small-area contrast k,

$$k = \frac{B_{max}}{B_{min}}$$

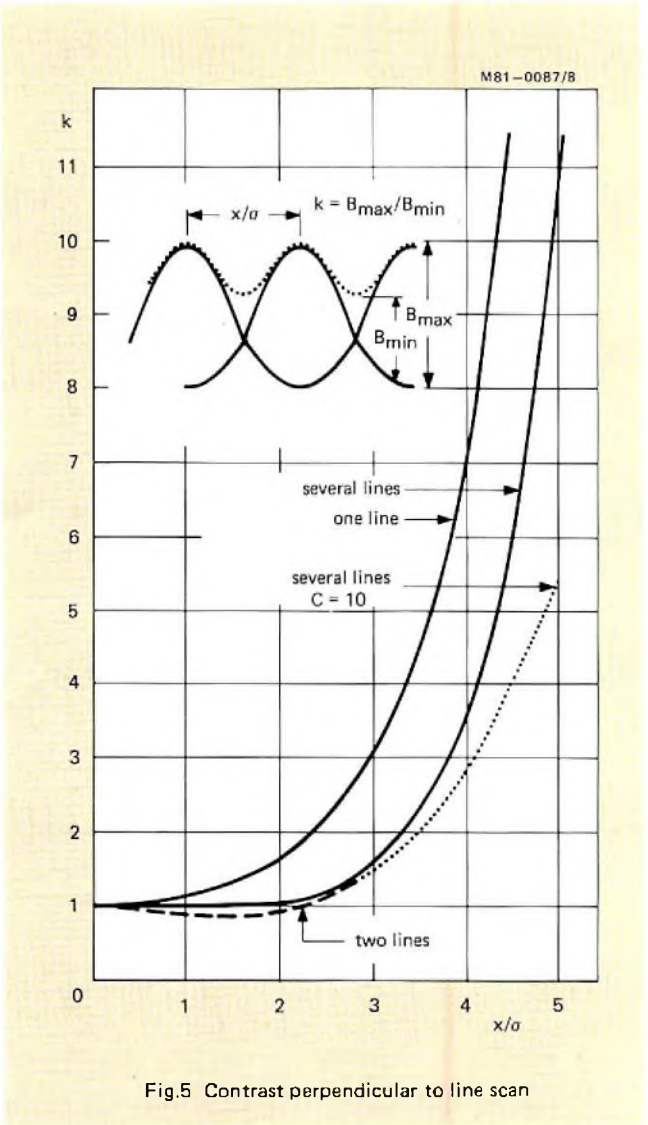


Fig.5 Contrast perpendicular to line scan

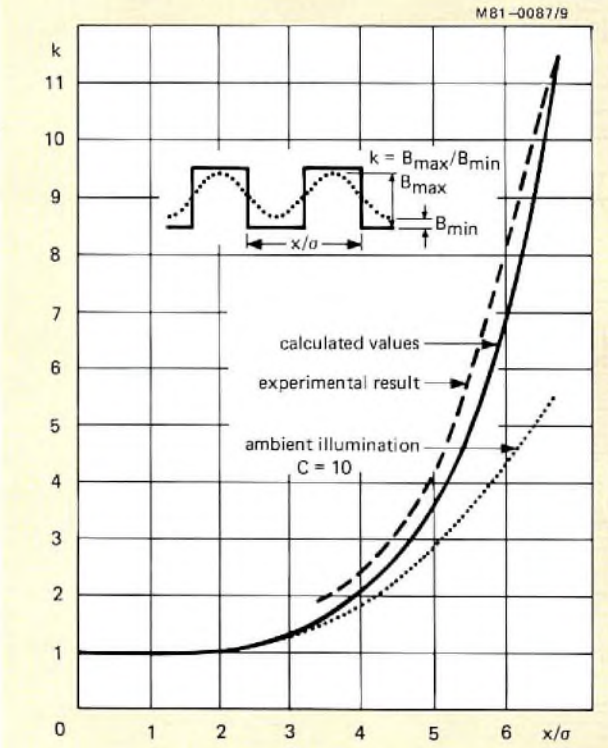


Fig.6 Contrast parallel to line scan

The increase of contrast with separation between lines is shown in Fig.5, where x is the spacing between the lines, and x/σ the normalised spacing (Ref.4). At $x/\sigma = 2$ (merging raster conditions), $k = 1.03$, which is just sufficient to enable the eye to distinguish the lines.

Ambient illumination affects the value of small-area contrast. This is shown by the dotted curve for $C = 10$ in Fig.5. Using this value of large-area contrast, it possible to show that the resultant small-area contrast k' is

$$k' = \frac{C}{1 + (C - 1)/k}$$

The foregoing applies to resolution in the direction perpendicular to the scanned lines. In the direction parallel to the scanned lines, the spot velocity has to be taken into account. The results of calculations based on a squarewave modulation of spatial period x/σ are compared with experimental values in Fig.6. As before, the presence of ambient illumination ($C = 10$) is detrimental.

The question now arises, what is an acceptable value of k' in a working situation? The eye can just distinguish separate lines at $k' = 1.03$. A large-area contrast of 10 is comparable to that of good newspaper printing and has already been assumed as suitable for data displays. Small-area contrast is that between neighbouring letters like H, M, N (one dot spacing), or inside the eye of the letter e. The latter represents the worst case. It is reasonable to accept $k' = 4.50$ for the worst case, and thus $x/\sigma = 6$ (Fig.6). As ambient illumination decreases, the value of k' increases.

In terms of a character matrix, contrast has meaning if one of any two neighbouring dots is white and the other black. The width of two dots of character matrix is thus required to be $x/\sigma = 6$. As the line separation d under 'merging raster' conditions is equal to 2σ, the width of two dots of character matrix under the same conditions should be equivalent to three lines of raster; that is,

$$d = \frac{2}{3} \times \text{width of a character matrix dot.}$$

Character element size and tube size

Legibility requirements are usually stated in terms of character height, height-to-width ratio, spacing between rows of characters, etc. (Ref.5). Information generally available suggests that for good visibility the angle subtended at the eye by a character element of size a should be about 3 minutes of arc (Ref.1). At a viewing distance of 400 mm, that corresponds to a = 0.35 mm.

Tube size is determined by the number of characters to be displayed. The number of elements displayed horizontally is $m_h C_h$, hence the width of the written area can be approximated by $H = am_h C_h$. The corresponding screen diagonal is H/0.72.

Alternatively, the screen size can be specified on the basis of the number of rows required if that is the governing consideration.

RESOLUTION OF A COLOUR TUBE

A monochrome display has three degrees of freedom: width, height, and luminance. Colour adds two more: hue and saturation. The shadowmask screen of a colour tube is built up either of dots or vertical stripes (Fig.7) and when the three guns are operative to display white, at least three elements of the screen are excited at the same time. It is from these 'building bricks' that elements of resolution must be built.

Obviously, the more triads that can be allocated per element of resolution (or per dot of a character matrix) the better are the final results. However, it is of interest to know the minimum number of triads which will give an acceptable display on the screen. It should be noted that the choice of triad system is not entirely open, since there is a trend towards self-converging systems which require an in-line arrangement of electron guns and preclude the delta configuration shown in Fig.7(a).

If one triad of a striped screen (Fig.7(c)) is allocated per element of resolution, the system would work well only if the holes of the shadowmask lined up with the elements of the character matrix (Fig.8(a)), a situation which is impossible to ensure. In the worst case the boundaries between the elements of the character matrix could coincide with the centres of the shadowmask holes (Fig.8(b)), with complete loss of contrast.

To overcome this difficulty and to ensure adequate differentiation between the elements of character matrix, it is found necessary to allocate at least three phosphor triads per two elements of character matrix (Fig.9); for a striped screen this can be expressed as $3p_S = 2a$. With a = 0.35 mm, $p_S = 0.23$ mm and is independent of tube size.

It is of interest to note that existing 14 in colour tv pictures tubes just meet this criterion when displaying teletext information, and the resulting display is judged as being satisfactory.

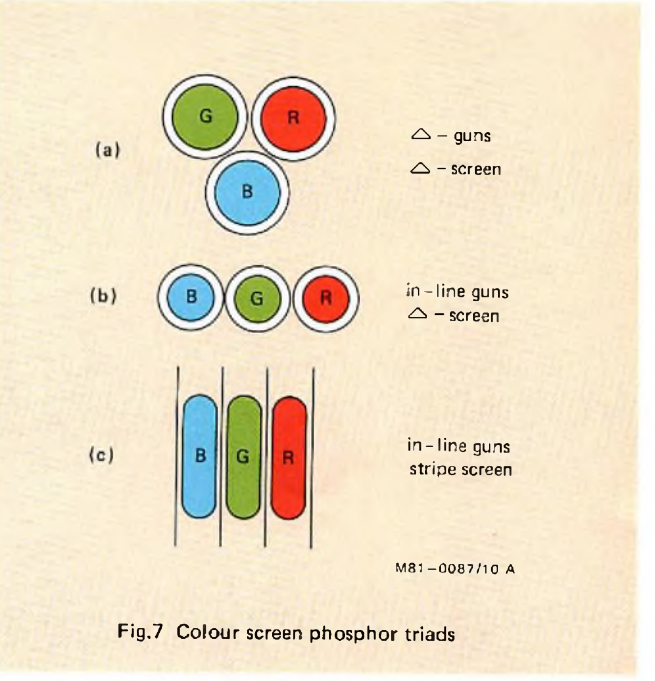
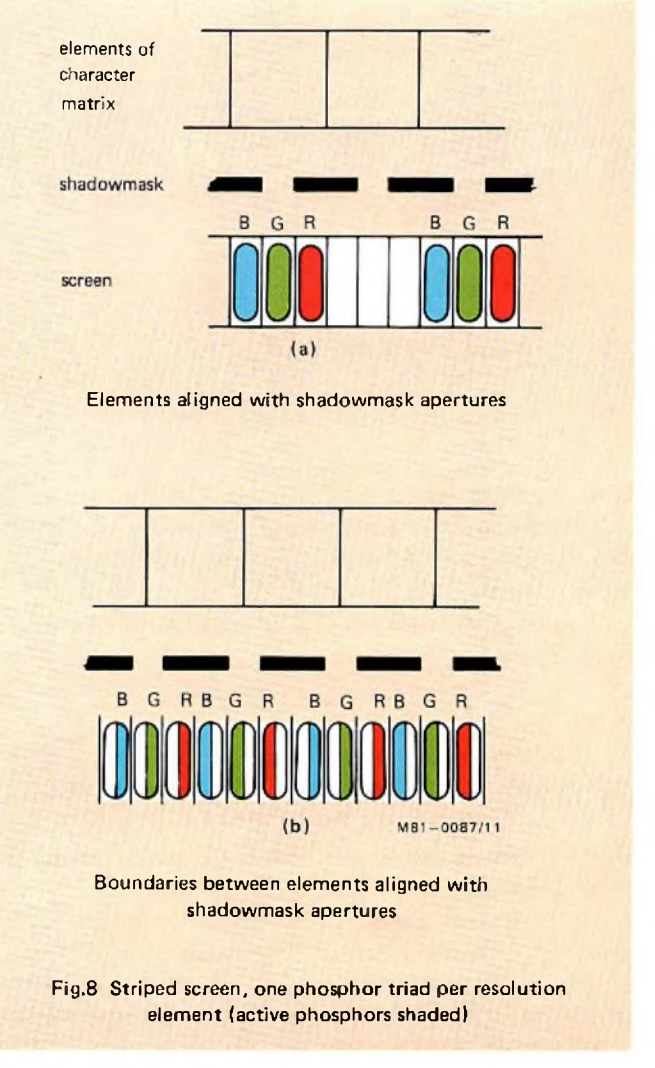


Fig.7 Colour screen phosphor triads



Elements aligned with shadowmask apertures

Boundaries between elements aligned with shadowmask apertures

Fig.8 Striped screen, one phosphor triad per resolution element (active phosphors shaded)

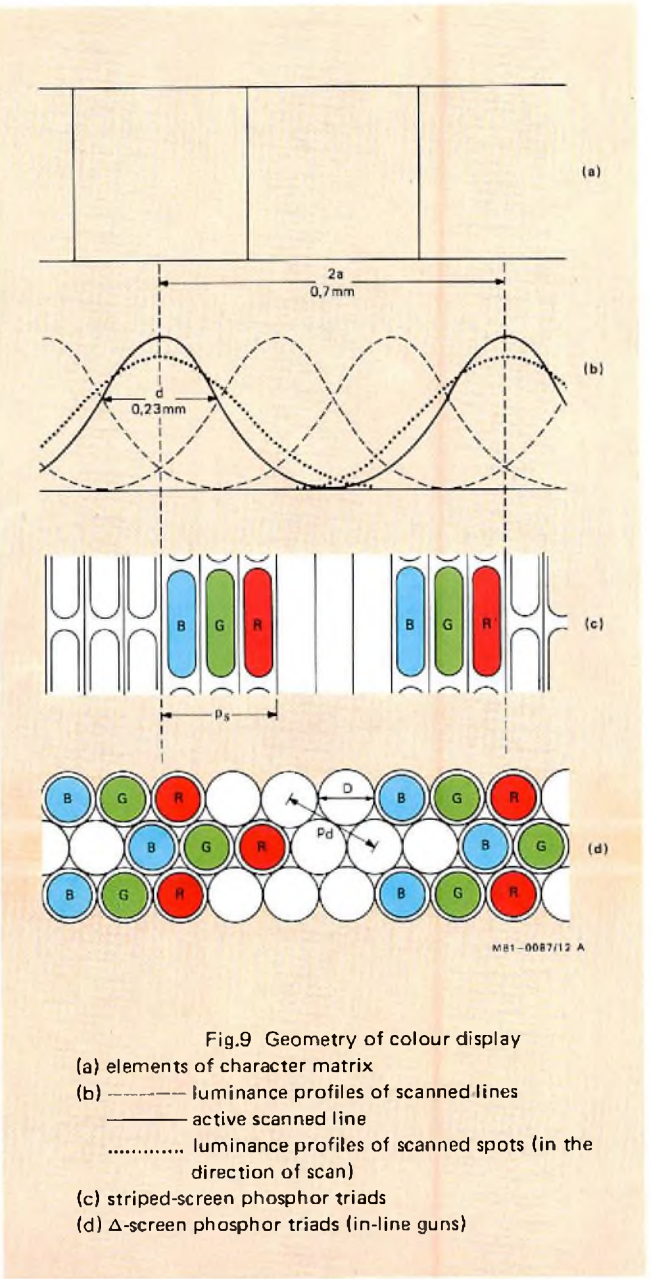


Fig.9 Geometry of colour display
(a) elements of character matrix
(b) ——— luminance profiles of scanned lines
——— active scanned line
..... luminance profiles of scanned spots (in the direction of scan)
(c) striped-screen phosphor triads
(d) Δ-screen phosphor triads (in-line guns)

The minimum allocation for an in-line Δ-screen system is shown in Fig.9(d). This can be expressed as six phosphor dots per two elements of character matrix; that is, $6D = 2a$, where D is the dot diameter.

Now, the pitch p_d of a Δ-screen is the distance between the centres of the nearest two dots of the same colour. A simple calculation shows that $p_d = D\sqrt{3}$. Thus the minimum requirement in terms of pitch is $p_d = a/\sqrt{3}$. Thus, with $a = 0.35$ mm, $p_d = 0.20$ mm.

Table 2 lists the results of corresponding calculations for the three main types of electron-gun/screen combination.

Fig.9 summarises the geometrical requirements of striped and delta screens, based on the merging raster definition of resolution and a line spacing such that $3d = 2a$. The widening of the line due to spot velocity (in the direction of line scan) is shown by the dotted curves. For $a = 0.35$ mm, the results can be summarised as follows:

$d = 0.23$ mm

$p_s = 0.23$ mm

$p_d = 0.20$ mm

Because of uncertainties related to the limits of visibility, the shape of the line-width profile, the rise time of the video signal, personal preferences, etc., the accuracy of the calculations is not great. Nevertheless, they can be used as a guide in dimensioning a colour display system.

TABLE 2
Limiting requirements of colour screens

electron-guns screen	Δ Δ	in-line Δ	in-line striped
minimum requirements per two elements of resolution	4.5 D	6 D	$3p_s$
maximum value of pitch	0.77 a	0.577 a	0.667 a
for a = 0.35 mm:			
maximum value of pitch (mm)	0.269	0.202	0.233
maximum value of D (mm)	0.156	0.117	0.078

SAMPLE CALCULATION

Consider a monochrome display having 28 rows of 80 characters each. The character matrix is 7 x 9, and the character cell 9 x 14. Assume non-interlaced operation at 50 Hz. The total number of scanned lines is then,

$$N = \frac{m_v C_v}{1 - q_v} = \frac{14 \times 28}{1 - 0.08} = 426$$

and the scan frequency is

$$f_h = N f_v = 426 \times 50 = 21.3 \text{ kHz}$$

Thus, the scan period is $\tau_h = 46.95\ \mu s$.

From the typical values given earlier:

line flyback time $\tau_h \times p_h = 46.95 \times 0.16 = 7.51\ \mu s$

field flyback time $\tau_v \times p_v = 20 \times 0.04 = 0.8$ ms

line blanking $\tau_h \times q_h = 46.95 \times 0.21 = 9.86\ \mu s$

field blanking $\tau_v \times q_v = 20 \times 0.08 = 1.6$ ms.

The duration of one display element is:

$$\tau = \frac{1 - q_h}{f_h m_h C_h} = \frac{1 - 0.21}{21\,300 \times 9 \times 80} = 51.51 \text{ ns}$$

and the rise time is $\tau_r = \tau/3 = 17.2$ ns.

TABLE 3
Calculated values for several data-graphic display systems; $f_V = 50$ Hz, non-interlaced raster

parameter	class of display				
	basic*	half-page		full-page	
format	horizontal	horizontal	horizontal	vertical	horizontal
characters per row, C_h	40	80	80	80	120
number of rows, C_v	24	24	28	68	58
total number of characters	960	1920	2240	5440	6960
character matrix	5 X 7	5 X 7	7 X 9	7 X 9	7 X 9
character cell	6 X 10	6 X 12	9 X 14	9 X 14	9 X 14
dots per row, $m_h C_h$	240	480	720	720	1080
active lines, $m_v C_v$	240	288	392	952	812
total number of dots	57 600	138 240	282 240	685 440	876 960
display diagonal (mm)	117	233	350	466	526
nearest tube size (monochrome)	9 in	12 in	15 in	20 in	22 in
useful screen diagonal S (mm)	228	295	352	473	530
line width (mm)	0.34	0.30	0.23	0.24	0.23
resolution (lines)	430	660	970	1300	1400
line frequency, f_h (kHz)	15.6	15.6	21.3	51.7	44.1
total line duration (μs)	64.0	64.1	46.9	19.3	22.7
line flyback time (μs)	12	10.3	7.5	3.1	3.6
active line duration (μs)	40	50.6	37	15.3	17.9
line system, non-interlaced	312	312	426	1034	882
duration of one element, τ(ns)	166	106	51.5	21.2	16.6
rise time, τ(ns)	55.5	35	17.2	7.1	5.5
3 dB bandwidth (MHz) (= clock frequency)	6.0	9.5	19.4	47.1	60.3
nearest colour tube (in-line)	14 in	14 in	14 in	20 in	22 in
required pitch, p_S (mm)	0.50	0.33	0.22	0.24	0.23

* This system is based on teletext and viewdata.

The 3 dB bandwidth $B_3 = 1/\tau = 19.4$ MHz, which is also the clock frequency for the logic circuitry.

Based on the number of characters per row, the horizontal measure of the display area is

$$H = 0.35 \times 9 \times 80 = 252 \text{ mm}$$

corresponding to a screen diagonal of 252/0.72 = 350 mm.

Based on the number of rows, the vertical measure is

$$V = 0.35 \times 14 \times 28 = 137.2 \text{ mm}$$

corresponding to a screen diagonal of 137.2/0.54 = 254 mm.

Thus, the number of characters per row is the governing requirement, and it can be met by a 15 in monochrome tube (S = 352 mm). The line width should be 0.234 mm (2a/3) at a screen brightness of 170 cd/m^2. The useful screen height of a 15 in tube is 227 mm, so the tube should be able to resolve 970 lines (227/0.234).

The results of calculations for several display systems are listed in Table 3.

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Recently introduced GTO thyristors make it possible to construct mains-driven series-resonant power supplies (SRPS) which are more efficient than switched-mode power supplies and also cause minimal mains pollution. This article describes the theory of operation of the SRPS and presents ten methods of connecting a load to the circuit.

Introduction to the series-resonant power supply

E. B. G. NIJHOF and H. W. EVERS

There has long been a need for a smaller and more efficient alternative to the transformer/rectifier/series-stabiliser circuit for deriving a constant, easily-isolated d.c. supply from the mains. The development of high-voltage switching transistors, such as our BUX80 series, has allowed the construction of SMPS circuits which go a long way toward meeting this need but are still far from providing the ideal answer to the problem. The main drawbacks of the SMPS, when it is supplied from the 220 V/240 V mains, are limited efficiency due to switching losses and dissipation in dV/dt limiting RC networks, mains pollution and r.f.i. due to the generation of near-rectangular current waveforms, difficult transformer design, and the need for a complex control circuit to ensure continued operation with an open-circuit or short-circuit load. A circuit that overcomes these drawbacks is the series-resonant power supply (SRPS) which incorporates an inverter in which a semiconductor switch maintains sinusoidal oscillation in a series-resonant LC network. Although the high-frequency sinusoidal currents generated in an SRPS allow it to be made compact and efficient, with far less mains pollution and r.f.i. than the SMPS, its use has so far been restricted to low-voltage power supplies due to the lack of a suitable low-loss, high-voltage semiconductor switch.

Our recently introduced range of GTOs (gate turn-off Thyristors described in Ref. 1, 2 and 3) with their high VA ratings, fast switching and simple, transistor-like drive, now allow the construction of SRPS circuits which can operate from a rectified mains input and will undoubtedly replace the SMPS for controlled mains power conversion in applications such as television sets, industrial drives, fluorescent lighting systems, microwave and inductive cookers. The SRPS is also suitable for controlling the speed of d.c. series-wound motors in domestic appliances, and for reducing harmonic distortion in the mains supply by acting as a buffer between the mains and a d.c. power supply. The main advantages of the SRPS are:

- It is a more than 90% efficient power converter.
- It causes minimal mains pollution because the mains input current can be made sinusoidal 50 Hz in phase with the mains voltage.
- It can be built with a single, easily-designed, inductive element (transformer) which also provides mains isolation.
- It continues to operate with the output short-circuit. It also continues to supply a well-stabilised output when it is not connected to a load.
- It can be made self-starting and does not therefore need a small 50 Hz transformer to supply the control circuit for the GTO.

Survey of GTOs for SRPS

type number	V_{DRM} (V)	I_{TCRM} (A)	$I_{T(AV)}$ (A)	case
BT157	1500	10	2.2	TO-220
	1300	10	2.2	TO-220
BTW58	1500	25	6.5	TO-220
	1300	25	6.5	TO-220
	1000	25	6.5	TO-220
BTW59*	1500	50	12	TO-238
	1300	50	12	TO-238

* With isolated base.

PRINCIPLES OF SRPS OPERATION

Figure 1 is the basic circuit of an SRPS, the operating principle of which depends on sinusoidal alternating current generation in the $L_1C_1C_O$ circuit. For guaranteed self-oscillation, there are two conditions regarding the values of the components. The inductance of L_S must be at least ten times that of L_1, and the value of C_O must be at least twice that of C_1. The operation of the circuit will first be described without a load connected to V_O and with a very brief conduction period for the GTO. This will be followed by a description of the circuit operation under similar conditions but with a longer conduction period for the GTO. Since the behaviour of the SRPS is complex (it sometimes functions as a fourth-order network), a complete analysis of the circuit is only possible with the aid of a computer; these theoretical descriptions are therefore only intended to give a basic understanding of the circuit operation and are followed by plots of the current and voltage waveforms derived by computer analysis of the basic circuit. The article concludes with a description of ten methods of connecting a load to the SRPS.

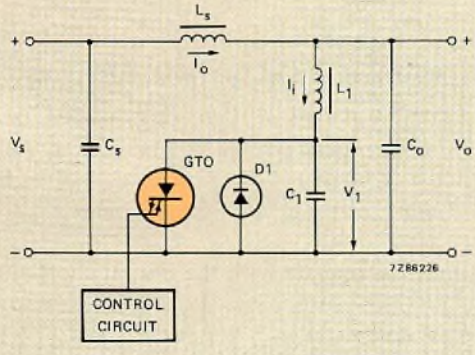


Fig.1 Basic SRPS circuit

Unloaded circuit with brief GTO conduction period

The waveforms for this mode of operation are given in Fig.2. Since $L_S \gg L_1$, and I_O is very small, the influence of L_S and I_O on the circuit behaviour can be disregarded for this simplified description.

In the steady state, with the GTO turned off, C_1 is charged to V_S. Assume that the GTO is turned on for the very short time necessary to just discharge C_1. Further assume that current I_1 is negligible during this brief on-time of the GTO. When the GTO is switched off, current I_1 oscillates sinusoidally about zero at the resonant frequency of

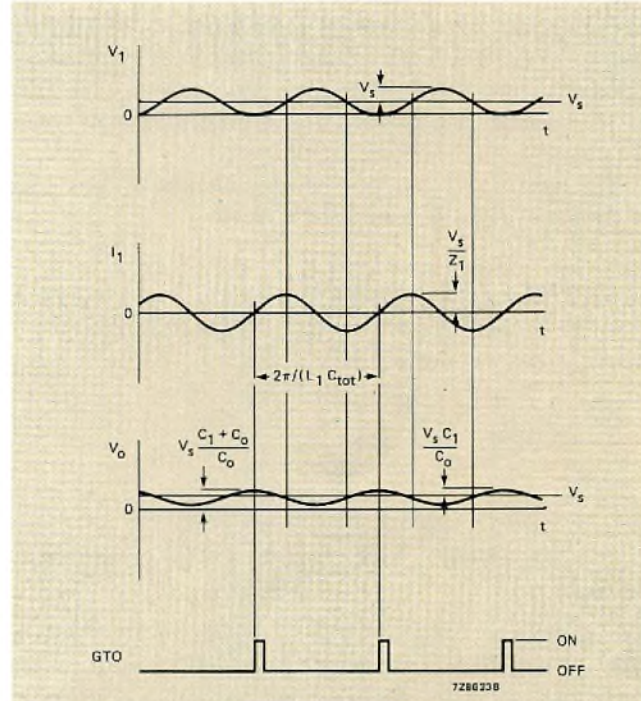


Fig.2 Waveforms of the basic SRPS for the shortest possible conduction time for the GTO

the circuit comprising L_1 together with C_O and C_1 in series:

$$\omega = \frac{1}{\sqrt{(L_1 C_{tot})}}$$

where

$$C_{tot} = \frac{C_1 C_O}{C_1 + C_O}$$

The peak oscillatory current is the supply voltage divided by the impedance of the resonant circuit (Z_1),

$$\hat{I}_1 = \frac{V_S}{Z_1} = V_S \sqrt{\frac{C_{tot}}{L_1}} \qquad (1)$$

which has an instantaneous value

$$I_1 = \frac{V_S}{Z_1} \sin \omega t$$

For stable self-oscillation of the circuit, the minimum level of V_1 must just reach zero during each cycle. The instantaneous value of V_1 is therefore given by

$$V_1 = V_S (1 - \cos \omega t)$$

$$\hat{V}_1 = 2V_S \qquad (2)$$

the a.c. component of which is

$$\hat{V}_{1\,a.c.} = \hat{V}_1 - V_S = V_S$$

This voltage therefore oscillates sinusoidally between 0 V

and $2V_S$ and has an average value equal to the supply voltage (V_S). Since the average value of the oscillatory current I_1 must therefore be zero, it is apparent that, as is to be expected, power is not drawn from the supply when the output from the circuit is unloaded.

The ratio V_O/V_1 is determined by the ratio of the values of C_1 and C_O. The peak value of V_O is

$$\hat{V}_O = V_S + \frac{\hat{V}_1 C_1}{2C_O} = V_S \frac{C_1 + C_O}{C_O}$$

the a.c. component of which is

$$\hat{V}_{O\,a.c.} = \hat{V}_O - V_S = V_S \frac{C_1}{C_O} \qquad (3)$$

Unloaded circuit with longer GTO conduction period

The waveforms for this mode of operation are given in Fig.3. If the conduction period of the GTO is made longer than that necessary to just discharge C_1, considerable current due to I_O and the discharge of C_O is flowing in L_1 at the turn-off instant. This value of I_1 will be denoted I_{off}. The peak oscillatory current V_S/Z_1 from equation (1) will now increase, in proportion to the ratio I_{off} to V_S/Z_1, by a factor

$$M = \sqrt{\left[\left(\frac{I_{off} Z_1}{V_S}\right)^2 + 1\right]}$$

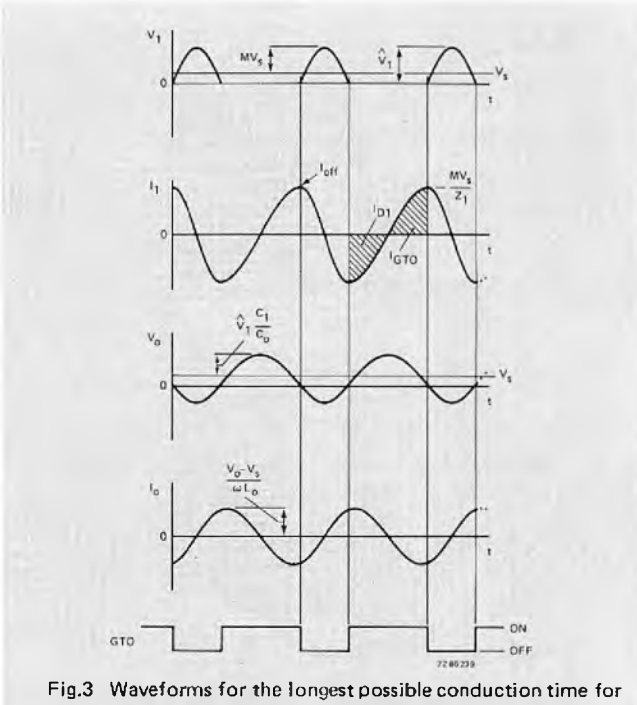


Fig.3 Waveforms for the longest possible conduction time for the GTO and V_1 = 1200 V max, V_S = 300 V, C_1 = 10 nF, C_O = 22 nF, L_O = 10 mH, L_1 = 1 mH, M = 3

The peak current through L_1 will therefore be

$$\hat{I}_1 = \frac{MV_S}{Z_1} \qquad (4)$$

The peak voltage across C_1 in Eq.(2) was V_S above its average value V_S. The rise of V_1 above V_S will now increase by the multiplying factor M, which gives

$$\hat{V}_1 = V_S + MV_S = V_S (M + 1) \qquad (5)$$

the a.c. component of which is

$$\hat{V}_{1\,a.c.} = MV_S$$

Solving Eq.(5) for the maximum multiplying factor in terms of the supply voltage and the maximum allowable peak voltage across the GTO gives

$$M_{max} = \frac{\hat{V}_1}{V_S} - 1 \qquad (6)$$

The a.c. component of the output voltage is $\hat{V}_{1\,a.c.}$ multiplied by the ratio C_1/C_O, which gives

$$\hat{V}_{O\,a.c.} = \frac{\hat{V}_{1\,a.c.}\, C_1}{C_O} = \frac{MV_S\, C_1}{C_O} \qquad (7)$$

Voltage control range of the basic SRPS

Assuming that V_S is the rectified mains voltage (300 V) and that the maximum peak voltage permitted across the GTO ($\hat{V}_1$) is 1200 V, then from Eq.(6) the maximum multiplying factor is 3 and, from Eq.(4), the maximum peak current through L_1 is

$$\hat{I}_1 = \frac{3V_S}{Z_1} \qquad (8)$$

Comparing Eq.(1) and (8) shows that the peak current through L_1 increases threefold when the conduction period of the GTO is increased to the maximum allowed by the permitted peak voltage across the GTO ($\hat{V}_1$). Comparing Eq.(2) and (5) shows that, with M = 3, the peak voltage across the GTO increases from $2V_S$ = 600 V to $4V_S$ = 1200 V when the conduction period of the GTO is changed from minimum to maximum. Comparing Eq.(3) and (7) shows that, with C_1/C_O = 0.5, the control range for the a.c. component of V_O is

$$V_{O\,a.c.}\ min = 0.5\ V_S = 150\ V$$

$$V_{O\,a.c.}\ max = 1.5\ V_S = 450\ V$$

The circuit can therefore be used as a power converter with its output voltage controllable over a 3:1 range by varying the conduction period of the GTO.

Alternatively, for a lower supply voltage such as V_S = 100 V, and the same maximum peak voltage $\hat{V}_1$ = 1200 V, the maximum multiplying factor from Eq.(6) is 11. Solving

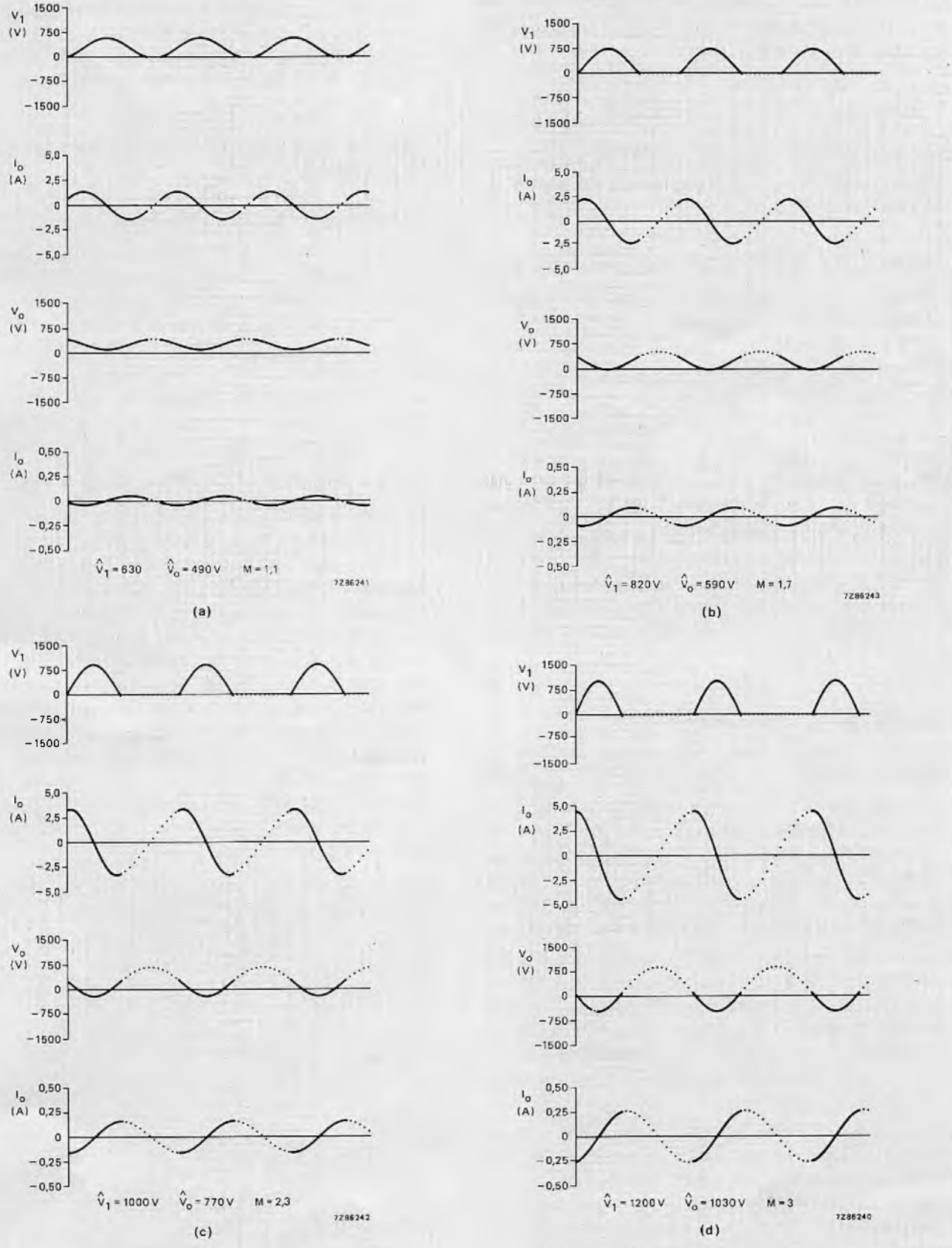


Fig.4 Computer plots of the waveforms in the circuit of Fig.1 with $V_s = 300$ V d.c., $L_o = 10$ mH, $L_1 = 1$ mH, $C_o = 20$ nF, $C_1 = 10$ nF. The dotted sections are the conduction period of the GTO, which is the maximum allowed by the V_1 specification

Eq.(2) and (5) for V_S shows that the variation of supply voltage (V_S) that can be compensated by variation of the conduction period of the GTO is:

$$V_{S\,min} = \frac{\hat{V}_1}{M+1} = 100\,V \qquad V_{S\,max} = \frac{\hat{V}_1}{2} = 600\,V$$

The SRPS output voltage can therefore be stabilised against a 6:1 d.c. supply voltage variation by varying the conduction period of the GTO.

Computer plot of the SRPS voltage and currents

As shown in Fig.4, a computer program has been used to plot the exact time functions for I_O, I_1, V_O and V_1 with V_S = 300 V d.c. and components values L_S = 10 mH, L_1 = 1 mH C_O = 20 nF and C_1 = 10 nF. The computer plots have been made for peak values of V_O of 490 V, 590 V, 770 V and 1030 V. Subtracting V_S = 300 V from these figures gives the a.c. component of V_O, which is about 190 V, 290 V, 470 V and 720 V respectively. This shows that the available output voltage control range for V_S = 300 V and V_1 max. = 1200 V is at least 3.8:1 instead of 3:1 as calculated in Eq.(3) and (7). This is due to the fact that the voltages across the capacitors in the oscillatory circuit are almost 180° out of phase so that the voltage division between them is not directly proportional to their values. The plots also indicate that the operating frequency decreases as the conducting time of the GTO is increased.

Extracting power from the SRPS

There are three basic methods of extracting power from the SRPS. They are:

- From capacitor C_O, via a diode, to an output electrolytic capacitor. Since the output voltage V_O a.c. is superimposed on the input d.c. level V_S, the voltage across the electrolytic capacitor will always exceed V_S. The circuit is therefore an up-converter and its main use is as a buffer between the mains and a d.c. power supply unit.
- From capacitor C_O via a capacitor which blocks the d.c. component of V_O so that pure a.c. is available at the output. This circuit is suitable for driving resistive loads and fluorescent lighting tubes. If the output from the blocking capacitor is rectified in a voltage doubler circuit, this type of SRPS is suitable for controlling the speed of a series-wound d.c. motor.
- By replacing inductor L_S with a transformer. This arrangement gives the best performance because it gives very good mains isolation and the load can be correctly matched to the SRPS by adjustment of the turns ratio of the transformer. This type of circuit can drive resistive or rectifier loads and can also be used as a supply for fluorescent tubes. For rectifier loads, however, the leakage inductance of the transformer must be made very low; for example, by using sandwiched windings. The final part of this article shows how inductor L_1 can be integrated with the transformer to overcome this problem and create an SRPS with a single inductive component.

PRACTICAL SRPS CIRCUITS WITHOUT MAINS-ISOLATION

Direct-coupled SRPS up-converter

The circuit of this type of SRPS is given in Fig.5. Diode D_O half-wave rectifies V_O and feeds the resultant half-sinewaves to output electrolytic C_O. Since the average value of V_O is V_S, the rectified half-sinewaves at the output are superimposed on the d.c. input voltage and the d.c. output voltage must necessarily exceed this level. The circuit is therefore an up-converter. The percentage of the total output power which has to be converted by the series-resonant circuit is $(V_O - V_S)/V_O$. For V_S = 200 V (average voltage of full-wave rectified 220 V mains) and $V_{O\,a.c.}$ = 500 V, this amounts to only 60 % of the total output power. This, together with the inherent high efficiency of the SRPS (about 95 % at V_S = 200 V d.c.), allows the circuit to feed some current to the load, even when the input voltage is as low as 10 % of the output voltage. For $V_{O\,a.c.}$ = 500 V to 600 V, the full-wave rectified mains input need not therefore be smoothed and can be obtained directly from a bridge rectifier followed by a low value decoupling capacitor (a few μF). This arrangement results in an SRPS up-converter with a well-stabilised d.c. output with a low level of superimposed 100 Hz ripple. Since the 50 Hz mains current flowing via the bridge rectifier without a high value smoothing capacitor is sinusoidal, the circuit can convert unlimited power without exceeding the limits of mains harmonic generation specified for domestic equipment in CENELEC specification EN 50 006.

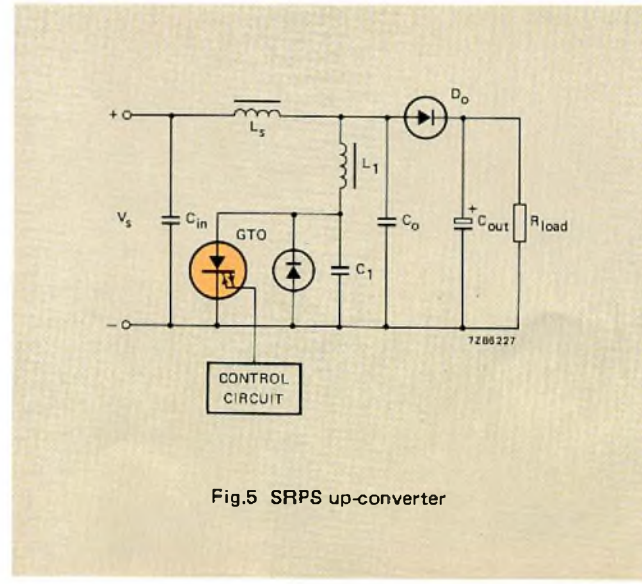


Fig.5 SRPS up-converter

The foregoing considerations indicate that the main use for this type of SRPS is for reducing mains distortion by acting as a buffer between the a.c. mains supply and a 500 V to 600 V d.c. power supply of more than 500 W.

Capacitively-coupled SRPS circuits

In capacitively-coupled SRPS circuits, the d.c. component of voltage V_O is blocked by a capacitor between C_O and the output rectifier. The circuit is given in Fig.6 which shows three methods of rectifying the a.c. component V_O.

Circuit 1. In circuit 1 of Fig.6, the a.c. component of V_O is rectified in a voltage doubler circuit that applies a positive d.c. voltage to the load. Like the previously described up-converter, this circuit works best with a d.c. output of more than 500 V, but has the added advantage that it is immune to output short-circuit. The main use of circuit 1 is speed control of a series d.c. motor connected as shown in Fig.7. Since inductor L_S has now been replaced by the series-connected armature and field windings of the motor, the SRPS has an effective input voltage of V_S minus the back e.m.f. Since the back e.m.f. is proportional to the current through the motor at a given speed, it is not necessary to use a high value capacitor to smooth the rectified mains input. The current flowing in the 50 Hz mains can therefore be made sinusoidal so that mains pollution is minimal. The range of back e.m.f. must not exceed about 75 % of supply voltage V_S so that the SRPS can still supply a reasonable amount of current when the motor is running at full speed.

Circuit 2. Circuit 2 of Fig.6 is similar to circuit 1 except that the output rectifier/voltage doubler is connected to provide a negative d.c. output voltage. The possible uses for this circuit are few.

Circuit 3. Circuit 3 of Fig.6 is again similar to circuits 1 and 2 except that the output is bridge-rectified. Since the bridge rectifier provides half the average output voltage of a voltage doubler rectifier, the minimum peak value for the d.c. output can be reduced to about 250 V. A disadvantage of the circuit however, is that the output is floating with respect to the return line of the input voltage.

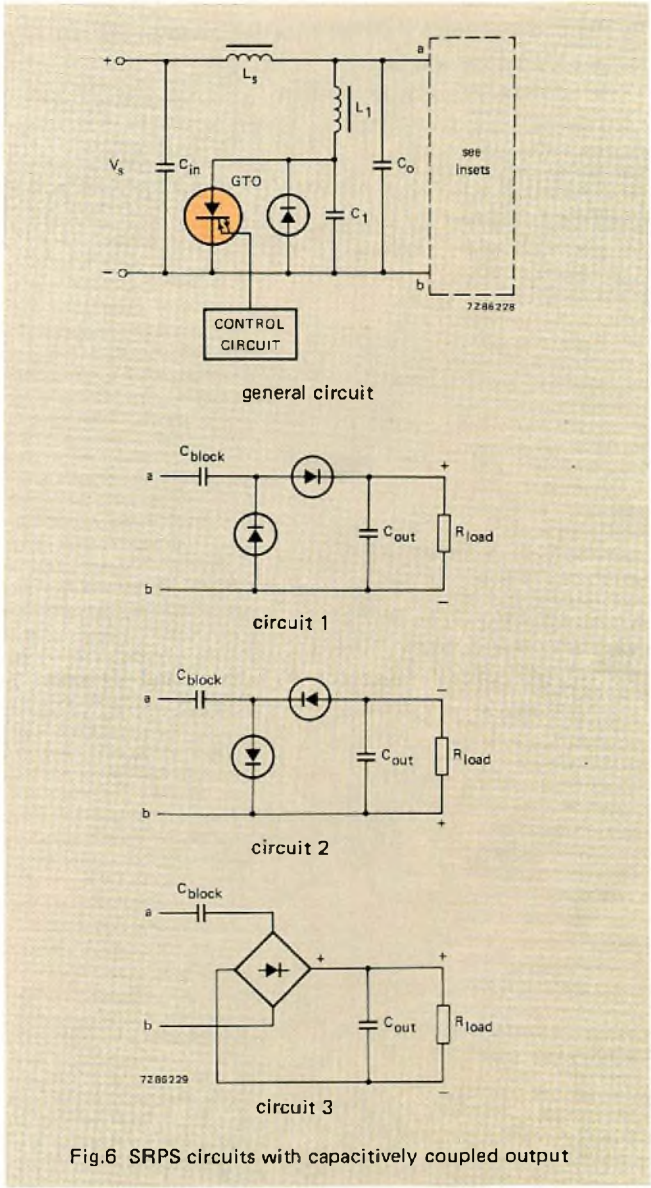


Fig.6 SRPS circuits with capacitively coupled output

SRPS CIRCUITS WITH MAINS ISOLATION

Since capacitor C_{in} has a much higher value than C_O, C_O is effectively in parallel with L_S so that V_O appears across this inductor. If mains isolation is required, L_S can therefore be replaced by a transformer with output rectifier connected to the secondary winding (Fig.8). The manner in which the rectifier and transformer are connected then determines the mode of operation, i.e. power transferred to the load

- when the current in the primary winding of the transformer is positive (forward mode, circuit 1)
- when the current in the primary is negative (flyback mode, circuit 2)
- when the current in the primary is positive and when it is negative (forward flyback mode, circuit 3).

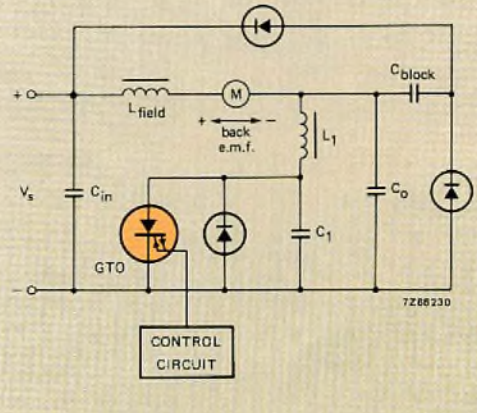


Fig.7 SRPS with capacitively coupled output controlling the speed of a d.c. series-wound motor

In circuit 3, a bridge rectifier can also be used with an untapped secondary winding.

In addition to driving rectifier loads via a transformer with low leakage inductance, these circuits with transformer-coupled output are also suitable for driving a resistive load or a load that behaves like a voltage source, for example, a fluorescent lamp or a magnetron in a microwave cooker. The best performance is obtained with a d.c. output of about 300 V.

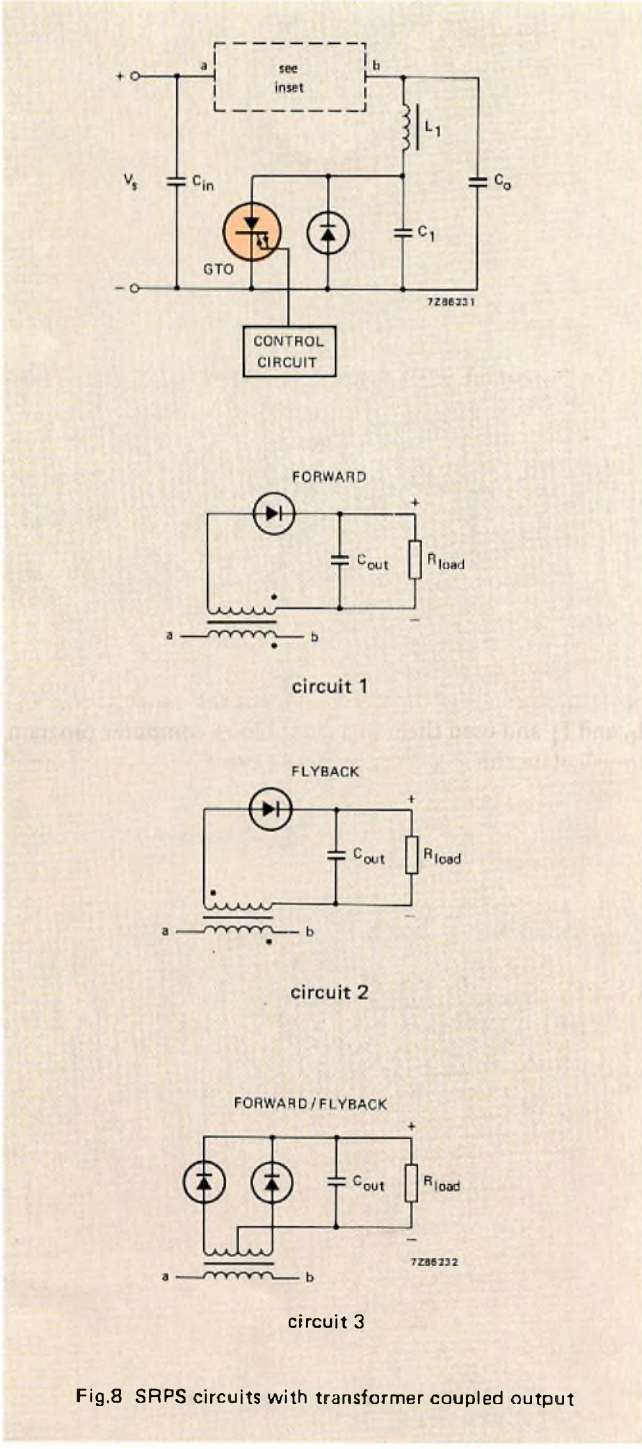
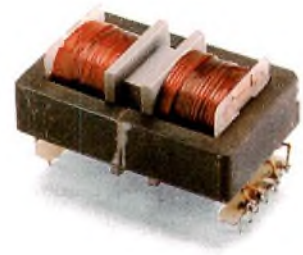


Fig.8 SRPS circuits with transformer coupled output

SRPS with a single inductive component (transformer)

In the circuits shown in Fig.8, inductor L_1 is rather bulky because, at operating frequencies of about 50 kHz, the flux swing in the core is quite large. It is therefore necessary to use a large core to prevent saturation and consequent overheating due to hysteresis losses. The core heating problem can be completely overcome by constructing the output transformer in such a manner that L_S is formed by the primary self-inductance and magnetising inductance of the transformer, and L_1 is formed by the primary and secondary leakage inductances. The flux swing of the transformer core is then quite small and the hysteresis losses are low.

Figure 9 shows how inductor L_1 can be integrated with the output transformer. Firstly, since C_{in} is a much higher value than C_O, C_O is effectively in parallel with the primary winding of the transformer and can therefore be connected in this position. Secondly, if the value of C_O is multiplied by the square of the turns-ratio of the transformer, it can be connected in parallel with the secondary winding. Finally, since there is now no connection to the junction of L_S and L_1, L_1 can be integrated with the output transformer. This final step is clarified by the equivalent T-circuit of the transformer given in Fig.10. Since a requirement for guaranteed self-oscillation of the SRPS is that the value of L_S is at least ten times that of L_1, the minimum coefficient of coupling for the transformer is $\geqslant 0.8$. A transformer with sufficient leakage inductance can easily be constructed on a pair of ferroxcube U-cores with the primary wound round one pole and the secondary wound round the other. If the external magnetic field with this type of construction is too great (for example, in a television receiver), the primary and secondary windings can be stacked on the gapped centre pole of a pair of E-cores. Experiments have shown that when this type of transformer is installed in a working SRPS and positioned within 4 cm of the deflection coils of a 26-inch CTV set with a 30AX deflection system, there is no perceptible distortion of the raster. If the transformer is positioned within 4 cm of the most sensitive part of the tube (cathode, grid 1 and 2 area), the maximum distortion of the raster is 1 mm.



Typical construction of a mains-isolated SRPS output transformer in which the leakage inductance is used for L_S. This transformer is for a 150 W to 200 W power supply operating at a frequency of 30 – 40 kHz

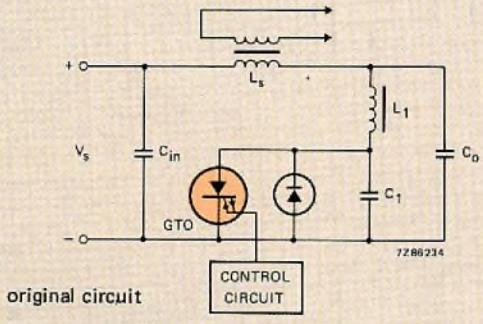
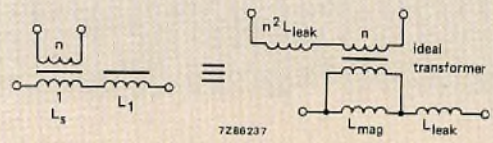


Fig.9 The three stages of integrating inductor L_1 with the output transformer of an SRPS



Approximate relations in the equivalent circuit ($L_s \geqslant 10L_1$)

$L_1 = 2L_{leak}$

$L_s = L_{mag}$

Fig.10 Transformer equivalent T-circuit with ideal transformation

An important advantage of the SRPS with a single inductive element is that it is inherently immune to a short-circuited output. It is therefore self-starting, even with zero volts across the output capacitor, so it is not necessary to use a separate 50 Hz transformer to provide a supply for the GTO control circuit.

The single-transformer SRPS can be used in any of the modes of operation illustrated in Fig.8 and can provide controlled power for all the previously mentioned types of load. Because the design of SRPS circuits is complex, we have calculated the time functions for the variables V_O, V_1, I_O and I_1 and used them in a closed-loop computer program to calculate the steady-state conditions for any set of input conditions. The computer program has also been used to construct a set of five universally-applicable graphs as a design aid for SRPS circuits.

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2. Woodworth, A., *Understanding GTO data as an aid to circuit design*, Electronic Components and Applications, Vol. 3, No. 3, May 1981.
3. Burgum, F. J., *Basic GTO drive circuits*, Electronic Components and Applications, Vol. 3, No. 4, August 1981.

Quality line

Collaboration is the key

Even where component quality is at a proven high level, quality potential cannot be fully realised by an OEM in isolation. Especially with more complex components, the quality realisable in finished equipment is heavily dependent on application conditions. Unsatisfactory performance may be due to dependence on component parameters that are not specified by the manufacturer, or not guaranteed, or not even tested for.

Here, the only solution is in-depth collaboration between component manufacturer and OEM. Together, they can often establish an economic solution for making component specification and testing compatible with the requirements of the application.

Quality in design: 123-series solid-aluminium capacitors

The 123-series of small, axial, solid-aluminium tubular capacitors offer the same CV product density as solid tantalum types but without their inherent disadvantages: life is not prematurely limited by internal changes. These new capacitors are produced by a development of the same technilogy used for the 121-series, whose established high quality gained the approval of CECC, FAO/FTL, CNES/Aerospatiale (Ariane), and British Telecom.

Intended primarily for industrial and professional applications where long life and high reliability are essential, 123-series capacitors meet the long-life requirements of IEC 384-4 and the climatic requirements of IEC 68-55/125/56. CECC type-approval is pending.

Factory testing of solid aluminium capacitors yields a reject level (process average) of $\leqslant 0.007\%$ (70 ppm) with a failure rate of $\leqslant 0.05 \times 10^{-6}$/h.

Experience shows that rejects due to poor solderability or loose leads should not exceed 10 ppm. The reject level due to lack of required function should also not exceed 10 ppm. Failure rate during the constant-failure period should not exceed 0.01×10^{-6}/h. A detailed failure-rate model is available. Detailed information about testing of 123-series capacitors is available as a separate Technical Publication.

Quality proven: 122-series solid-aluminium capacitors-stability and reliability in miniature

122-series solid-aluminium capacitors in miniature, single-ended epoxy envelopes are designed for long-life in industrial and other critical applications. Both in size and performance, they are fully equivalent to comparable tantalum types. They meet the long-life requirements of IEC 384-4 and fulfil the climatic requirements of IEC 68 55/125/56. They are available approved to NEN CECC 30 302-002.

Their stability and reliability have been evaluated against PTT requirements by a rigorous, 4 year endurance-test programme. Endurance tests of 37 240 h duration were carried out on 300 components covering most capacitance values and working voltages. After more than 11 million component-hours testing, only 5 capacitors were found to exceed the leakage-current specification: and only one of these had to be removed from test. Capacitance, tan δ, and impedance stabilities were all good.

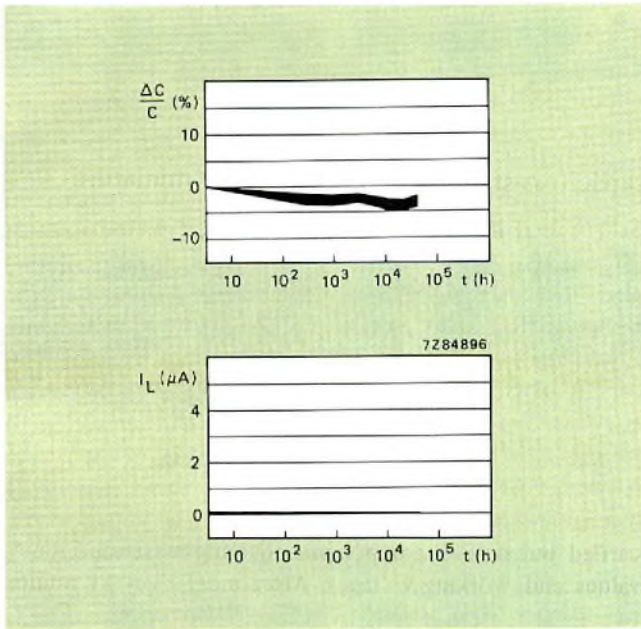
The sample tested was divided into batches of 10 capacitors. Tests were carried out under a variety of operating conditions: ambient temperatures of 70 °C and 85 °C;

122-series solid aluminium capacitor

operating voltages of 0 V, 0.75U_R and 1.1U_R. Operation at 1.1U_R was intended to explore the stability margin available when the capacitors were operated at rated operating voltage U_R.

Examples of capacitance and leakage current stability are given in the accompanying graphs. The change in capacitance for 4.7 μF, 25 V capacitors is shown in the upper graph. The lower one shows the leakage current during the test for 1.5 μF, 25 V capacitors. Both tests were carried out at 1.1 U_R and 85 °C.

The full leakage-current results show evidence of a self-healing mechanism in these component. More detailed information about these tests is available as a separate Technical Publication.



Improvement measurement method guarantees cerdip moisture level

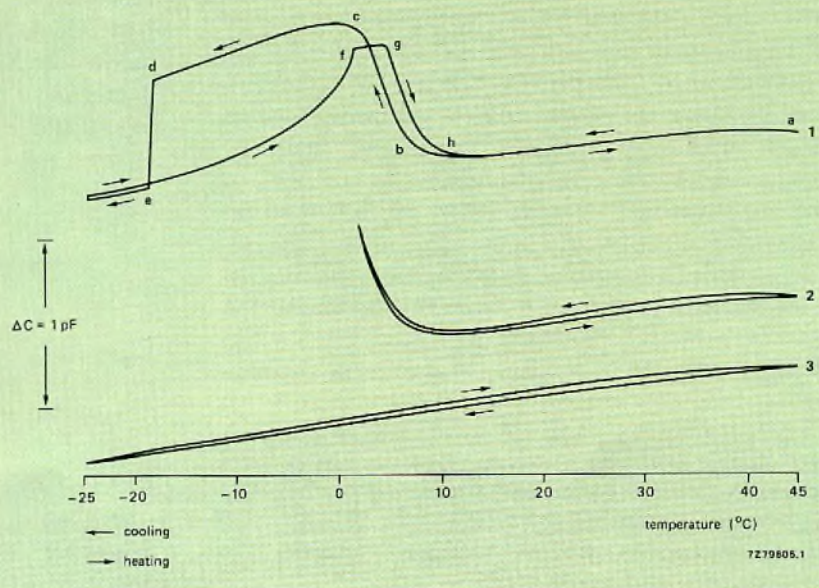
Standard methods of moisture detection and measurement are not suitable for the routine testing of passivated ICs in hermetic packages that is an essential element of effective quality control. The three alternative Procedures of MIL-STD-883B, Method 1018, are either destructive or require the incorporation of a moisture sensor within the IC package. The new method

- is applicable to all passivated devices
- is non-destructive
- takes about 10 minutes
- requires only simple equipment.

Thus, ICs in cerdip can now be supplied with a guaranteed maximum moisture content, established by 100% measurement.

In essence, the new method entails cooling the IC through its dewpoint, as in MIL-STD-883B, Method 1018, but now dewpoint is detected by the change in capacitance between adjacent die metallisation tracks caused by the precipitation of water. The curves shown are recordings of capacitance as a function of temperature (indicated by the forward voltage of a diode in the IC). The virtual coincidence of the heating and cooling cycle curves demonstrates the reproducibility of the method, which has been confirmed by an exhaustive evaluation programme.

For exceptionally long-life applications, moisture levels in the package cavity should be below 3000 parts per million by volume (ppmv), which corresponds to a dewpoint of −20 °C. We are able to supply our LOCMOS ICs in cerdip packages with a measured cavity dewpoint below −40 °C (moisture level less than 500 ppmv) as specified in MIL-STD-883B.



Capacitance variations measured between adjacent tracks of a LOCMOS IC reveal the presence of water vapour in the package cavity. Curve 1: a-b, water vapour; condensation takes place at b, the dew point; c-d, supercooled water; freezing takes place between d and e. As the sample warms, the ice melts between e and g; evaporation takes place from g to h. Curve 2 is a recording taken from the same IC as curve 1, but cooling was stopped and heating commenced at c. Curve 3 shows the behaviour of a sample whose dew point is below −25 °C.

Research news

Desk-size digital file stores million and a half pages

Megadoc, a storage and retrieval system developed by Philips' Research Laboratories, promises to revolutionise document handling. Using digital-optical recording technology which is an outgrowth of the video long-playing record, Megadoc can store in the floor space of an office desk a file that would otherwise occupy some fifty cubic metres. And from the million and a half pages such a file may contain it can retrieve and display any desired page within five seconds.

Under the control of a Philips P857 minicomputer, Megadoc deals with all aspects of document handling; recording, classification, storage, sorting, retrieval, distribution and duplication. It can accept input pictorially for recording and reproduction with either of two degrees of resolution. The prototype system displays only in black and white, but the potential for halftone and colour exists.

The compactness of the system is due to the bulk storage of documents on digital-optical recording discs. Each disc consists of a metal rim and hub supporting a pair of closely spaced glass plates having on their facing surfaces a tellurium film and a 40 000-turn spiral groove. Each turn of the groove is divided into 128 separately addressable segments and each segment has an information capacity of 1024 bits, making a total of $40\,000 \times 128 \times 1024 \approx 5 \times 10^9$ bits per side, or 10^{10} bits per disc. This is equal to the capacity of 24 nine-track magnetic tapes 730 metres long recorded at 640 bits per centimetre. The information density is about a hundred times that of a floppy disc

Information is written in by a laser which burns holes corresponding to binary digits in the tellurium film. In reading the recorded information, reflection from the film signals the presence or absence of holes (binary 0s and 1s). The disc rotates at 4 revolutions per second, and any segment of any turn can be accessed, on average, in 250 milliseconds.

Sixty-four discs housed in individual cassettes occupy a storage module from which they can be selectively extracted for reading or writing. Several storage modules, together with transport mechanisms and one or more disc readers or read/write units, comprise a filing 'jukebox' under the control of a Signetics microprocessor.

For existing documents the input to the system is from a scanner which translates a page into a digital signal. The principal element of the scanner is a linear array of 1728 photodiodes that resolves a page width into eight picture elements (pixels) per millimetre. The page is scanned lengthwise by traversing the optical system associated with the array. At high resolution the page length is resolved into 7.7 lines per millimetre, giving a total of $1728 \times 7.7 \times 297 = 3\,951\,763$ pixels for an A4 page; standard resolution gives 3.85 lines per millimetre, or 1 975 881 pixels per page. Either way the scanning time is one second, so the data rate approximates 4 Mbit/s for high resolution, 2 Mbit/s for standard resolution. Charges developed across the photodiode array are transferred to a shift register and converted to voltages corresponding to the grey-scale values of the pixels. A discriminator converts the voltages above and below a set threshold to binary digits corresponding to white and black.

The number of bits per page can be reduced by using a compression algorithm. The modified Huffman code gives an average compression factor of 10.

Text can also be entered from the keyboard of a word processor, up to a maximum of fifty 80-character lines per page. Using the 7-bit ASCII code plus a parity bit this requires only 32 000 bits per page. Whether entered from the page scanner or a word processor, each encoded page goes to an 8 Mbit capacity integrated-circuit buffer memory with an input and output speed of 4 Mbit/s.

Bits per page for different modes of entry

		compressed
word processor (ASCII plus parity bit)	32×10^3	–
pictorial, high resolution	4×10^6	4×10^5
pictorial, standard resolution	2×10^6	2×10^5

Internal data transfers are made via a switching network controlled by a Signetics 2650 microprocessor under the direction of the central P857 minicomputer. Serial bit

Internal transfers of data and instructions are made via a switching network controlled by a Signetics 2650 microprocessor under the direction of the P857 minicomputer. Serial bit streams entering the network are converted to parallel 8-bit bytes which can be transferred simultaneously between as many as six pairs of peripherals. These include not only page scanners, keyboards and buffer stores, but also video display units, data companders, telex terminals, and modems for connecting the system to a telephone network.

The register of documents lodged in the bulk store is kept in two moving-head magnetic disc memories connected to the P857 minicomputer. With a capacity of 40×10^6 bytes each, they can store a total of 100 000 document descriptions. Descriptive features that can be used for search and retrieval include document number, author, title, date, date of entry, number of pages, and key words.

A complete Megadoc work station consists of a page scanner, a video display unit and a keyboard. With the aid of the page scanner and keyboard an operator can enter incoming documents and their descriptions into the system and direct their distribution to the persons concerned. The addressees can review them at their convenience by activating their own video display units and enquiring via their keyboards whether there is incoming material for their attention. The video display units decode the digital signals received and display each page full size, black on white. The frame frequency is 47 Hz, which is fast enough to prevent flicker even at high brightness, and an internal refresher memory retains the display of a selected page for as long as the user may require. If he requires a hard copy he can request one via his keyboard.

The three main activities included in the Megadoc programming provide for:

- recording documents in the bulk store and distributing incoming documents to users of the system (mailbox function)
- tracing and retrieving stored documents on the basis of descriptive information supplied by a user
- selecting peripheral units for transmitting and receiving documents, and activating the switching network programs to effect the required transfers.

The special software created for Megadoc consists of two program packages. One governs the user-related parts of the activities mentioned above. The other governs operation of the switching network and the transfer of documents between peripherals. The standard software supplied with the P857 minicomputer permits different activities to proceed simultaneously under the supervision of a monitoring program which allocates computer time and memory capacity on the basis of priority and urgency.

Pages called up on the Megadoc screen are displayed full size, black on white. A refresher memory in the cabinet beneath the desk-top keeps them on display for as long as the user requires

Philips Technical Review, Vol. 39, No. 12, 1982, contains a detailed article on Megadoc from which this Research News item is abstracted.

These notes report activities of Philips research laboratories and do not imply commercial availability of any product embodying the described results. For further information, written application should be made to the Publicity Department, Philips Research Laboratory, Eindhoven, The Netherlands

Abstracts

Fast turn-off asymmetric silicon controlled rectifiers (ASCR)

The asymmetric silicon controlled rectifier is a development of the conventional thryristor combining high forward-blocking capability with low losses and fast switching performance. This article compares the construction of the ASCR and the conventional thyristor, and describes the device data for two currently available ASCRs: the BT155 and the BTW63. The use of the device data is illustrated by the selection of ASCRs for a pulse-width modulation inverter.

Intergrated circuits for hi-fi radios and tuners

The design flexibility provided by a set of integrated circuits for h.f. signal processing allows the same combination to be used in hi-fi radios, tuners and music centres with different standards of performance. The functions of the ICs are discussed in detail, and three versions of a complete radio are shown: an economy version, a high-performance version, and based on the latter, a microcomputer-controlled hi-fi tuner with frequency synthesiser, search tuning, digital frequency display and remote control. Subsequent articles will deal with other ICs in a range of more than forty for use in hi-fi radios.

Integrated circuits for data-graphic displays

A set of four new VLSI circuits reduces the number of ICs required in a data-graphic display from 40 to 15. The new circuits include a display-character and graphics generator, a programmable keyboard communications controller, a video timing controller and a video attributes controller, and they are so partitioned that each can be used independently of the others. The display provides for 96 ASCII alphanumeric characters plus 32 special characters, as well as line and block graphics; operating features include split-screen, multiple cursors, horizontal and vertical scrolling, reverse video, character blank, blink, underline and highlight, and light-pen strike-through.

Scan-velocity modulation increases TV picture sharpness

Two new deflection yokes for use with 30AX picture tubes – the AT1261 and AT1271 – sharpen the TV picture by modulating the scan velocity in accordance with variations in the luminance signal. The new yokes have auxiliary coils that modulate the horizontal deflection field, driven by a signal proportional to the derivative of the demodulated luminance signal. The special driving circuitry has facility for teletext blanking, allowing it to become inoperative during teletext reception, and requires only slight modification to existing circuitry to incorporate it into current receivers.

Cathode-ray tube requirements for data-graphic displays

Data-graphic displays can take advantage of picture tube and associated components and circuit technology that has benefited from three decades of television. However, the requirements for high-density alpha-numeric displays differ in certain important respects from those of television, and the difference must be taken into careful account not only in the design of the display components but also in how they are applied.

Introduction to the series-resonant power supply (SRPS)

The main advantages of series-resonant power supplies are low switching losses, no need for an R–C snubber, simple output transformer design, low mains pollution and wide range of input voltage. These advantages together with a power conversion efficiency of more than 90%, and consequent small size make the SRPS an attractive alternative to SMPS in many applications. The article explains the operating principle and presents eight possible circuit configurations.

Schnelle asymmetrische Thyristoren

Asymmetrische Thyristoren stellen eine Weiterentwicklung herkömmlicher Thyristoren dar. Sie zeichnen sich durch hohe Vorwärts-Sperrspannung, niedrige Verluste und kurze Schaltzeiten aus. In diesem Artikel werden der Aufbau eines asymmetrischen mit dem eines herkömmlichen Thyristors verglichen und die Kenndaten der gegenwärtig verfügbaren asymmetrischen Thyristoren BT155 und BTW63 erläutert. Am Beispiel eines mit Impulsbreiten-Modulation arbeitenden Inverters wird gezeigt, wie die Auswahl eines asymmetrischen Thyristors auf Grund der Kenndaten erfolgen kann.

Integrierte Schaltungen für HiFi-Radios and Tuner

Die Entwurfsflexibilität einer Familie von integrierten Schaltungen für die HF-Signalverarbeitung ermöglicht es, eine solche Gruppe von Schaltungen in HiFi-Steuergeräten, Tunern und HiFi-Kompaktanlagen unterschiedlicher Leistungsklassen einzusetzen. Die Funktionen derartiger integrierter Schaltungen werden im einzelnen erörtert und drei Versionen eines kompletten Rundfunkempfängers vorgestellt: eine ökonomische Version, eine Version hoher Leistungsfähigkeit und, basierend auf der letzteren, ein durch Mikrocomputer gesteuerter HiFi-Tuner mit Frequenz-Synthesiser, Suchlauf, digitaler Frequenzanzeige und Fernsteuerung. In nachfolgenden Artikeln werden in einer Reihe von über 40 Schaltungen auch noch andere integrierte Schaltungen für den Einsatz in HiFi-Radios behandelt.

Integrierte Schaltungen für Datensichtgeräte

Eine neue Familie aus vier LSI-Schaltungen reduziert die Anzahl integrierter Schaltungen, die ein Datensichtgerät benödigt, von 40 auf 15. Die Schaltungsfamilie umfasst einen Zeichen-/Grafik-Generator, einen programmierbaren Tastatur-Encoder mit serieller Schnittstelle, eine programmierbare Video-Steuer-schaltung sowie eine Zeichendarstellungsart-Steuerschaltung. Die Funktionen sind so über die Schaltungen verteilt, dass jede Schaltung unabhängig von den übrigen eingesetzt werden kann. Es sind 96 alpha-numerische ASCII-Zeichen sowie 32 Sonderzeichen darstellbar, ausserdem auch Block- und Strich-Grafik-Elemente. Die Betriebsmöglichkeiten umfassen Bildschirmaufteilung ("split screen"), Mehrfach-Kursor, horizontaler und vertikaler Bilddurchlauf ("scroll"), Positiv- und Negativ- Darstellung, Zeichenaustastung, Blinken, Unterstreichen, doppelte Helligkeit und Lichtgriffel-Einsatz.

Erhöhung der Bildschärfe im Fernseh-Empfänger durch Ablenkgeschwindigkeitsmodulation

Zwei neue Ablenkeinheiten für 30AX-Bildröhren – die Typen AT1261 und AT1271 – sind für die Erhöhung der Bildschärfe durch Ablenkgeschwindigkeitsmodulation geeignet, die von Änderungen des Leuchtdichtesignals abgeleitet wird. Die neuen Ablenkeinheiten haben eine Zusatzwicklung zur Modulation des Horizontal-Ablenkfeldes, die von einem Signal gesteuert wird, welches durch Differentiation des Leuchtdichtesignals gewonnen wird. Die Modulationsschaltung kann bei Videotextbetrieb abgeschaltet werden, sie erfordert nur geringe Änderungen der bestehenden Schaltung für den Einbau in die laufende Geräteserie.

Anforderungen an Bildröhren für Datensichtgeräte

Datensichtgeräte können auf der Erfahrung aufbauen, die in drei Jahrzehnten Fernsehen mit Bildröhren, den zugehörigen Komponenten und der Schaltungstechnik gemacht wurden. Die Anforderungen an hochauflösende alphanumerische Displays unterscheiden sich jedoch in bestimmten wichtigen Punkten von denen an Fernsehbildröhren; die Unterschiede müssen gewissenhaft beachtet werden, nicht nur beim Entwurf der Display-Komponenten sondern auch in der Art der Anwendung.

Serienresonanz – Netzteile

Die Hauptvorteile von Serienresonanz-Netzteilen sind: niedrige Schaltverluste, nicht erforderliche RC-Schutzbeschaltung, einfacher Ausgangstransformator, geringe Netzrückwirkung sowie grosser Eingangsspannungsbereich. Diese Vorteile, zusammen mit einem Umwandlungswirkungsgrad von über 90% und kleinen Abmessungen machen Serienresonanz-Netzteile zu einer attraktiven Alternative zu Schaltnetzteilen. Der Artikel erklärt die Wirkungsweise von Serienresonanz-Netzteilen und gibt acht Einsatzmöglichkeiten an.

Thyristors rapides asymétriques

Le thyristor asymétrique ou ASCR (Asymmetrical Silion Controlled Rectifier) a été spécialement développé pour offrir, par rapport au thyristor conventionnel, tout á la fois, une tension de blocage en direct élevée, de faibles pertes et une grande rapidité de commutation. Cet article compare les constructions des thyristors asymétrique et conventionnel et expose les caractéristiques de deux ASCR actuellement disponibles: les séries BT155 et BTW63. L'utilisation de ces caractéristiques est illustré dans le cas d'une réalisation d'onduleur à commande par impulsions à largeur modulable.

Circuits intégrés pour récepteurs radio et tuners hi-fi

La souplesse de conception qu'offre l'emploi d'un jeu de circuits intégrés pour le traitement de signaux H.F. permet d'employer un même jeu dans des récepteurs radio, tuners et chaînes haute fidélité à caractéristiques fonctionnelles d'un niveau de qualité différent. Les fonctions des circuits intégrés sont exposées en détail et trois versions d'un récepteur radio complet sont présentées: une version économique, une version de haut de gamme et, sur la base de cette dernière, un tuner hi-fi piloté par microcalculateur avec synthétiseur de fréquence, recherche automatique des émetteurs, affichage numérique de fréquence et télécommande.

Circuits intégrés pour visualisation graphique de données

Grâce à un jeu de quatre nouveaux circuits intégrés à très grande échelle (VLSI), le nombre nécessaire de circuits intégrés d'un appareil de visualisation graphique de données a pu être réduit de 40 à 15. Les nouveaux circuits comprennent un générateur de caractères et de graphiques, un contrôleur de communications programmable à clavier, un contrôleur de synchronisation des fonctions vidéo et un contrôleur d'effets vidéo, et ils sont cloisonnés de telle sorte que chacun puisse être utilisé indépendamment des autres. L'appareil offre la possibilité de visualiser 96 caractères alphanumériques ASCII, plus 32 caractères spéciaux, ainsi que des graphiques linéaires et modulaires.

La modulation de vitesse de balayage accroît la netteté des images de télévision

Deux nouvelles unités de déviation destinées aux tubes 30AX – AT1261 et AT1271 – améliorent la netteté de l'image en modulant la vitesse de balayage en fonction des variations du signal de luminance. Ces nouveaux déviateurs sont équipés de bobines auxiliaires parcourués par un courant proportionnel à la dérivée du signal de luminance qui module le champ de déviation horizontale. Le circuit de commande spécial est équipé d'un dispositif de suppression qui le rend inopérant pendant la réception d'émissions de télétexte, dispositif qui peut être incorporé à des récepteurs déjà en service, moyennant une légère modification des circuits existants.

Caractéristiques exigées des tubes cathodiques pour visualisation graphique de données

La visualisation graphique de données peut tirer profit de la technologie des tubes-image et des composants et circuits associés, technologie qui a profité de trois décennies de télévision. Toutefois, les exigences de la visualisation alphanumérique à haute densité diffèrent sous certains aspects importants de celles de la télévision, et il faut soigneusement tenir compte des différences, non seulement dans la conception des composants, mais aussi dans la manière de les employer.

Introduction à l'alimentation résonante-série (SRPS)

Les principaux avantages des alimentations résonantes-série sont de faibles pertes de commutation, l'absence de la nécessité d'un réseau ralentisseur R–C, la simplicité de conception du transformateur de sortie, la faible pollution du secteur et l'étendue de la gamme de tensions d'entrée. Ces avantages, associés à un rendement de conversion de puissance de plus de 90% et, par suite, à la petitesse de ses dimensions, font du SRPS une solution de rechange intéressante pour le SMPS dans de nombreuses applications. L'article explique le principle de fonctionnement et présente huit configurations possible du circuit.

ASCRs de bloqueo rápido

El rectificador asimétrico controlado de silicio (ASCR) es un desarrollo del tiristor convencional, que combina la elevada capacidad de bloqueo directo con bajas pérdidas y rápidas características de conmutación. Este artículo compara la construcción del ASCR y del tiristor convencional y describe las características de dos ASCRs disponibles: el BT155 y el BTW63. El uso de los datos del dispositivo se ilustra mediante la selección del ASCR para un inversor de la modulación de anchura de los impulsos.

Circuitos Integrados para radios y sintonizadores de alta fidelidad

La flexibilidad de diseño producida por un conjunto de CI's para el proceso de señal Hi-Fi permite que una misma combinación pueda ser usada en radios de Hi-Fi, sintonizadores y centros musicales, con diferentes standards de ejecución. La funciones de los circuitos integrados se examinan con detalle y se ofrecen tres variedades completas de una radio. Una versión económica, en versión de alto rendimiento, y basado en esta última, un sintonizador de Hi-Fi controlado por microordenador con un sintetizador de frecuencia, búsqueda automática de sintonía, visualizador de frecuencia digital y control remoto.

Circuitos Integrados para visualizadores gráficos de datos

Un grupo de cuatro nuevos circuitos VLSI, reduce el número de CI's requeridos en un visualizador de datos de 40 hasta 15. Los nuevos circuitos incluyen un display caracter y un generador de gráficos, un controlador programable de comunicaciones, un controlador de secuencias de video y un controlador de atributos de video divididos de tal forma que unos pueden ser usados independientemente de los otros. El display está provisto de caracteres alfa-numéricos ASCII, más 32 caracteres especiales, así como gráficos de líneas y de bloque: las características de funcionamiento incluyen pantalla dividida, cursores múltiples, arrollamiento horizontal y vertical, video inverso, borrado de caracteres, parpadeo.

Modulación de la velocidad de exploración incrementa la nitidez de la imagen

Dos nuevos yugos de deflexión para utilización en los tubos 30AX – AT1261 y AT1271 – dan mayor nitidez a la imagen TV, modulando la velocidad de exploración de acuerdo con las variaciones en la señal de luminancia. Los nuevos yugos, tienen bobinas auxiliares que modulan el campo de deflexión horizontal excitando mediante una señal proporcional a la derivada de la señal de luminancia demodulada. La especial circuitería de excitación tiene posibilidad de borrado de teletexto, permitiéndole que permanezca inoperante durante la recepción del teletexto y puede ser incorporado en los receptores normales con solo una ligera modificación de la circuitería existente.

Requerimiento en un tubo de Rayos Catódicos para un visualizador gráfico de datos

Los tubos empleados en los visualizadores gráficos de datos y su circuitería se han aprovechado de la experiencia de los tubos de imagen y componentes asociados, durante tres décadas de televisión. No obstante, los requerimientos de la alta densidad de los displays alfa-numéricos, difieren en ciertos importantes aspectos de los de televisión. Estas diferencias deben ser tomadas en cuenta cuidadosamente, no solo en el diseño de los componenetes del display sino también en cuanto a aplicación.

Introducción a las fuentes de alimentación resonantes SRPS

Las ventajas más importantes de las fuentes de alimentación resonantes son las bajas pérdidas en conmutación, no precisan de filtro RC, simple diseño de transformador de salida, baja polución de red y amplia gama de tensiones de entrada. Estas ventajas unidas a una eficiente conversión con un rendimiento del 90% y consecuentemente su pequeño tamaño, hace del SRPS una atractiva alternativa de las fuentes de alimentación conmutadas en diversas aplicaciones. El artículo explica el principio de funcionamiento y se dan ocho posibles configuraciones de circuito.

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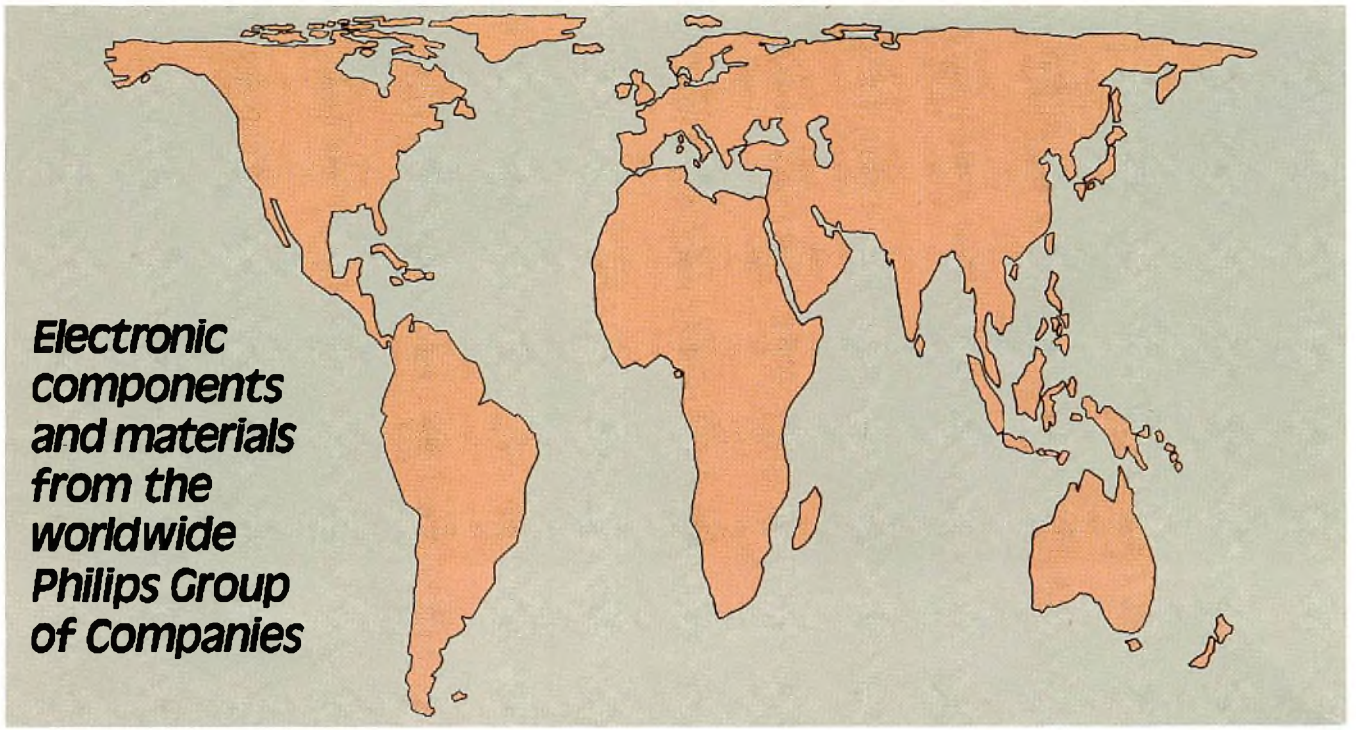

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