Electronic components & applications

Vol. 3, No
November 198

ISSN 0141–6219

Electronic components & applications

Volume 3, No. 1 November 1980

A remarkable characteristic of music is its ability to evoke nostalgia. Nostalgia for the time of its composition, for the composer, or performer, or for the occasion we first heard it played. But in his professional capacity, at least, no nostalgia assails the designer of audio reproduction equipment. His thoughts are directed toward the future. Toward the perhaps mythical lure of ideal audio reproduction. In this issue we have an article that will bring the myth somewhat closer to reality. The article concerns a new semiconductor laser for use with the video long player and its audio counterpart the compact audio disc. For audio, the introduction of the compact disc will remove all the noise and distortion currently associated with discs and styli. Myth and reality are steadily merging, but where are we heading? Nostalgia is a compelling force. Will it drive the audio buff of the future to demand circuits that restore the very imperfections we have striven so long to eradicate?

Contents

CQL10 semiconductor laser for information readout

The new *digital-optical* (DO) disc stores information digitally as a series of pits in a spiral track. To read out the information an optical scanning system directs a light beam at the track as the disc rotates, and by means of a photodiode, generates an electrical signal from the variation in reflected light intensity produced by interference between incident and reflected beams. Its very high information density makes the DO disc particularly attractive in video and audio applications (for example the new *VLP* system and the *compact disc*) as well as in more general data storage applications.

For an acceptable signal-to-noise ratio the light source must have a radiation density of about 2500 W/(sr.cm^2).

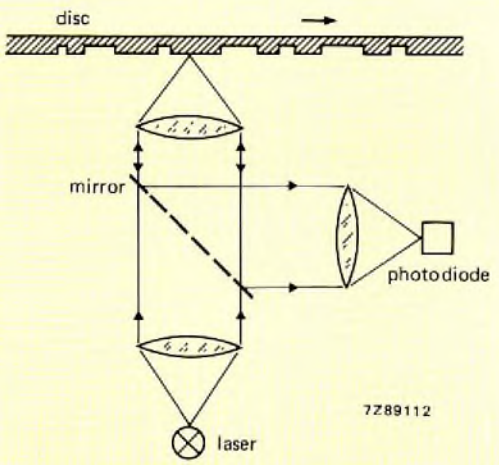

Fig.1 Optical system for read-out from the track of pits on a digital-optical disc

Only a laser can meet this requirement. Present DO systems use helium-neon lasers as the light source, but these have the disadvantage of being rather large (about 20 cm long) and of requiring a 1500 V supply.

In this article we describe a new semiconductor laser, the CQL10, based on AlGaAs. The CQL10 is about 1 cm long and requires a supply of only 2 to 3 V. It produces a beam whose wavelength (780 nm) remains constant even at ambient temperatures as high as 60 °C (an essential requirement in compact disc systems), and whose coherence length is relatively short so that noise produced by external feedback effects is virtually absent. Finally, the CQL10 is more efficient than the helium-neon laser and in volume production it is likely to be significantly cheaper.

LASER ACTION IN THE CQL10

Figure 2 shows a section through the CQL10 crystal. A GaAs substrate supports four layers, one (layer 4) of pure GaAs, and three (layers 1, 2 and 3) in which some of the Ga is replaced by Al: 46% in layers 1 and 3, 16% in layer 2. The amount of substituted Al in each layer determines its energy gap. With a current I flowing in the direction shown the energy levels take the form shown in Fig.3, and layer 2 effectively becomes an energy *well* for electons migrating from layer 1 and holes migrating from layer 3. So electrons and holes collect in layer 2 and *population inversion* arises with excess electrons in the conduction band and holes in the valence band.

Photons of the correct frequency ν ($h\nu = E_{g2}$, Fig.3) stimulate electron/hole recombination within layer 2.

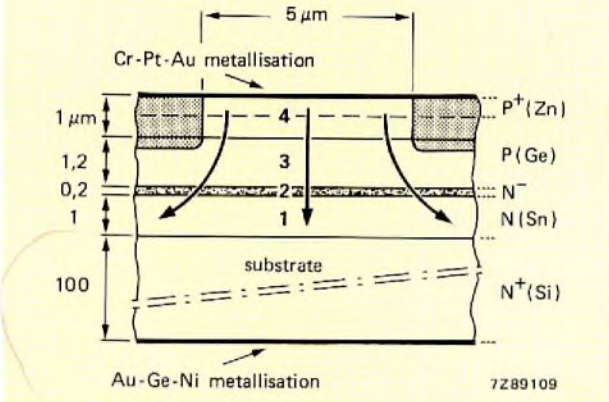

Fig.2 Cross-section through the CQL10 laser crystal. Layer thicknesses are given on the left and conduction type and dopant are given on the right. Layer 2 is undoped but residual impurities make it weakly n-type. A strong Zn diffusion makes layer 4 very strongly p-type (degenerate). Proton implantation in the upper layers (dark grey area) turns them into insulators except for a 5 μm strip. Heavy doping of the substrate and the upper layer permits good electrical contact between the crystal and the metallised layers (Cr-Pt-Au and Au-Ge-Ni)

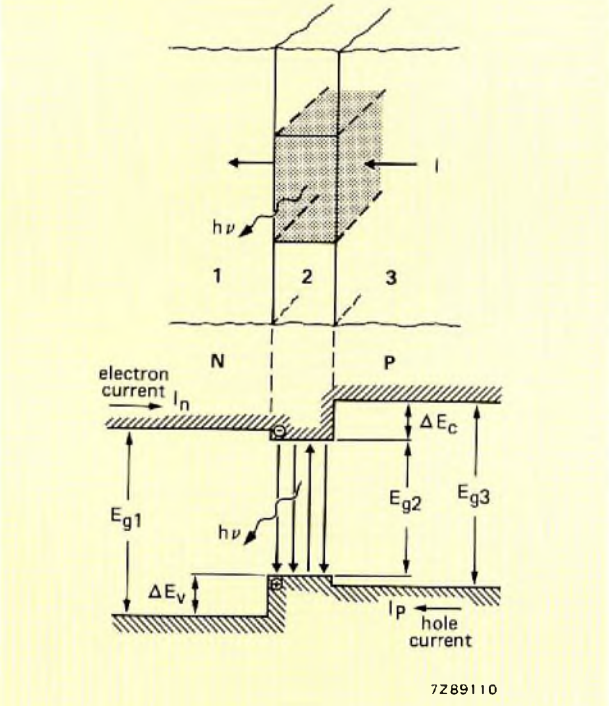

Fig.3 Simplified energy-level diagram for the CQL10 crystal with a large current I flowing in the *3 – 1* direction. The energy barriers ΔE_v and ΔE_c trap electrons and holes in layer 2 leading to a population inversion which in turn leads to an increase in *stimulated emission*

These *stimulated recombinations* are accompanied by emission of coherent photons, so a light wave passing through the layer is amplified. Internal reflection at the layer boundaries confines the photons to layer 2 and with partially reflecting mirrors (crystal cleavage planes) located at each end to provide optical feedback, the layer behaves as a resonator.

Stimulated emission increases with current I. Above a threshold current I_{th} the amplification is sufficient to overcome internal losses and losses at the mirror surfaces. The resonator then starts to oscillate and *laser action* starts with the emission of an intense beam of coherent light.

Below I_{th} stimulated emission is strongly attenuated. Electrons and holes still recombine *spontaneously*, however, with the emission of incoherent photons, and the device behaves merely as an LED.

To assure precisely defined current flow within layer 2, proton implantation of layers 3 and 4 (as indicated in Fig.2) limits the conduction region to a 5 μm strip.

LASER ASSEMBLY

Figure 4 shows the laser assembly. The copper assembly block supports the laser crystal and acts as a heatsink.

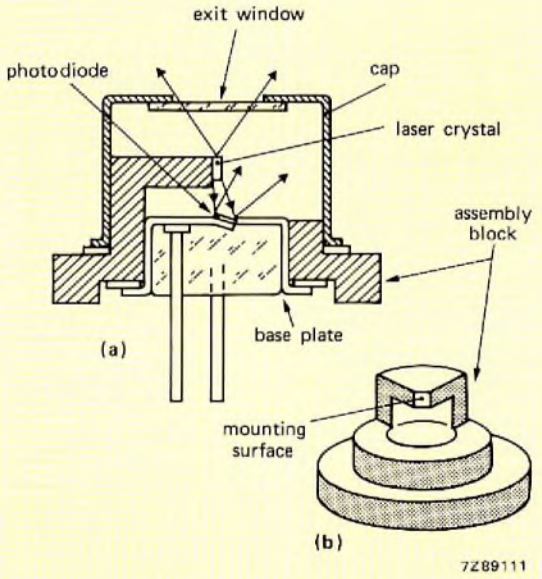

Fig.4 (a) CQL10 envelope. The laser beam leaves the envelope via a glass window in the cap. The envelope is hermetically sealed and filled with dry nitrogen to protect the laser crystal; (b) the assembly block is made of oxygen-free copper. The laser crystal is soldered to the mounting surface with the active layer (layer 2) as close as possible to the block for maximum cooling

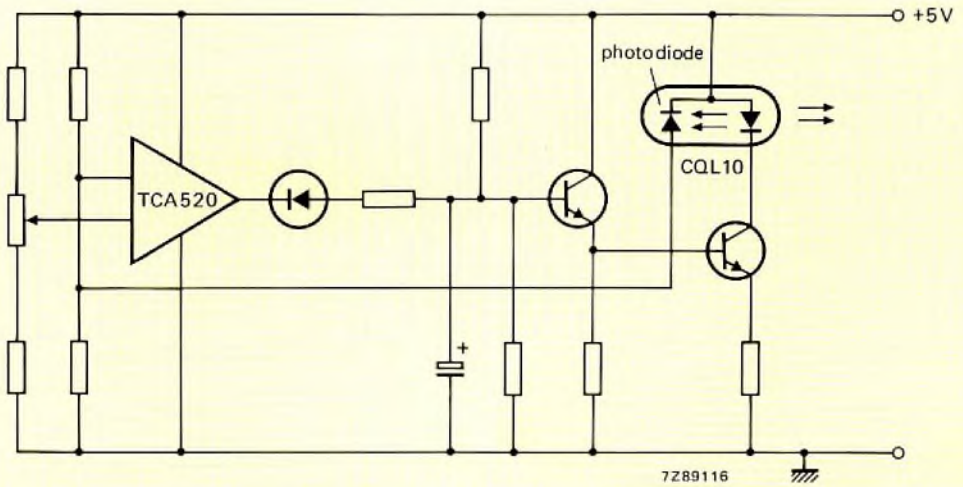

Fig.5 Feedback network incorporating a photodiode for stabilising the light flux from the laser. The photodiode controls the supply current to correct for variations in light flux

Two slots in its base permit accurate positioning of the assembly on installation. The envelope is filled with dry nitrogen to protect the crystal, and its external surfaces are gold plated as a protection against oxidation.

A feedback network (Fig.5) incorporating a photodiode stabilises the optical power from the laser. The photodiode is located in the reverse laser beam (Fig.4) and is tilted relative to the optical axis to prevent reflected light from adversely affecting the laser action.

Semiconductor lasers deteriorate with age, the threshold current increasing and the light-output/current characteristic becoming less steep. The rate of deterioration depends strongly upon the operating temperature, a rise of 30 K, for example, reducing the life by a factor of 15. Provided the temperature is kept under control, however, ageing effects will be minimal. At an *ambient* temperature of 30 °C and at a light level of 5 mW, the CQL10 can reasonably be expected to operate for at least 10 000 hours with no noticeable deterioration.

THE CQL10 IN OPERATION

The CQL10 laser beam has a wavelength of 780 nm. Although longer than that of the helium-neon laser currently used for scanning *VLP* discs (i.e. 630 nm) it is nevertheless satisfactory for all DO applications.

Figure 6 shows the light-output/current characteristics of the CQL10. Above the threshold current (at which the laser begins to oscillate) light output increases sharply. Laser action is strongly temperature dependent, a temperature rise of 30 K leading to a 30% increase in I_{th}. The crystal, or at least the active layer (layer 2) must therefore be kept as cool as possible. Otherwise the laser may go into *thermal runaway* with light output falling sharply and most of the energy being converted into heat.

Figure 7 shows the light output L as a function of the angle α to the optical axis. The CQL10, unlike the helium-neon laser, has a strongly divergent and astigmatic exit beam. This is caused by refraction at the exit aperture, and can be easily corrected with a suitable lens system.

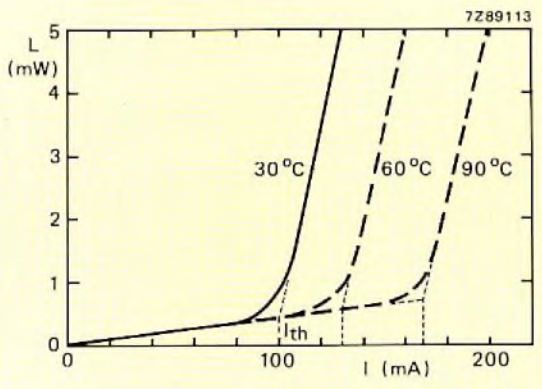

Fig.6 Light output L versus current I for the CQL10. Above the threshold current I_{th} light output increases sharply and laser action begins. The behaviour is strongly temperature dependent, a rise of 30 K producing a 30% increase in I_{th}

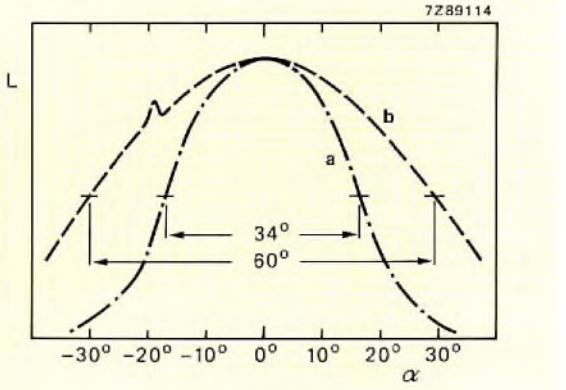

Fig.7 Light output L as a function of the angle α to the optical axis of the laser; (a) for radiation in the plane of the active layer, and (b) for radiation in the plane perpendicular to it. The peak at −20° is caused by reflection at the photodiode. The beam is strongly divergent and astigmatic; in the plane of the active layer the maximum spread is 34°, perpendicular to the active layer the maximum spread is 60°

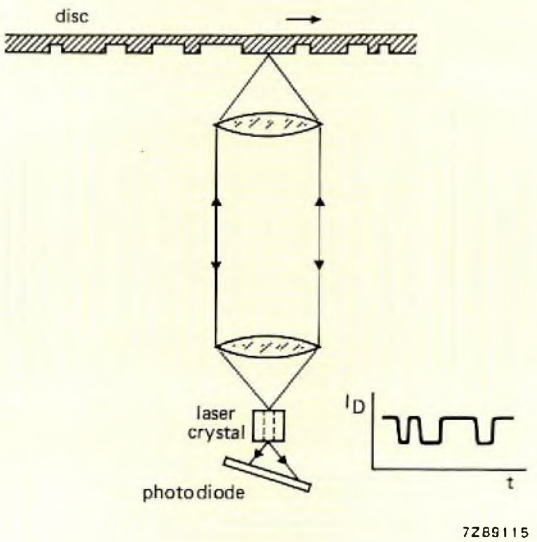

Fig.8 Information read-out using the laser itself as the detector. The disc reflects light back to the exit aperture of the laser crystal. The laser reacts by increasing its emitted power. Reflected light fluctuations are then reproduced in the photodiode current I_D

INFORMATION READOUT USING OPTICAL FEEDBACK

In the conventional scanning system (Fig.1), a mirror diverts the reflected beam to a detector, i.e. a photodiode, which then provides the output signal. We can, however, use the laser itself as the detector. Simply by directing the reflected beam back to the exit aperture of the laser, we produce a feedback effect in which the emitted power varies with changes in reflected light intensity. We can detect these variations in emitted power using the photodiode already incorporated in the CQL10 (Fig.4). This method of information readout (Fig.8) is still at an experimental stage and we cannot say at present whether or not it will become generally accepted. In anticipation that it will, however, the CQL10 already uses photodiodes that are fast enough to match the speed of information readout in the DO system.

ACKNOWLEDGEMENT

This article is based on one by J. C. J. Finck, H. J. M. van der Laak, and J. T. Schrama that appeared in Philips Technical Review, Vol. 39, 1980.

Analogue control system for a.c. motor with PWM variable speed drive

W.B. ROSINK

This article describes an analogue control system which has been developed for use with our Pulse-Width Modulation (PWM) variable speed drive for three-phase a.c. motors. The article is the fourth in a series, previous articles being listed in Refs.1, 2, and 3. Reference 1 gives a general introduction to our PWM drive system, Ref.2 describes a specially developed inverter circuit, and Ref.3 describes an LSI circuit, type HEF4752V, developed specifically for signal generation in PWM drive systems.

The three-phase a.c. motor is remarkable for its simplicity of construction. This simplicity is in contrast to the comparatively complex requirements of a control system for an a.c. motor operating under variable speed and load conditions. The features needed by such a system will be determined by three factors: the inherent operating characteristics common to all a.c. motors, the method of speed variation employed, and the particular control requirements needed by the motor user. The control system described in this article has been designed to meet the requirements of the majority of users, but without being excessively complex. Alternative system designs of greater or lesser refinement are of course possible. The detailed description of the design and operation of the analogue control system is preceded by a review of the operating characteristics of a.c. motors, and the relevant features of our PWM variable speed drive.

THE A.C. MOTOR

The three-phase a.c. induction (asynchronous) motor consists of a wound stator connected to a three-phase a.c. supply, and a squirrel-cage rotor with no external connections. The stator currents produce a rotating magnetic flux, with a speed of rotation (synchronous speed) n_s given by:

$$n_s = \frac{f_s}{p} \times 60 \text{ rev/min}, \qquad (1)$$

where f_s is the stator supply frequency, and p is the number of pole-pairs in the stator. The rotating stator field induces an e.m.f. in the rotor conductors, and since the conductors are short-circuited, this results in rotor currents. Motor torque is produced by the interaction of the stator flux and the rotor currents, the torque contribution T of each rotor conductor being proportional to the product of the in-phase component of the rotor current and the air-gap flux; that is:

$$T \propto I_r \cos\theta_r \phi, \qquad (2)$$

where I_r is the rotor current, $\cos\theta_r$ the rotor power factor, and ϕ the air-gap flux per pole.

In order that rotor currents may be induced, the rotor speed n_r must be different from the synchronous speed. This speed difference is called slip, and is usually expressed as a fraction of the synchronous speed; that is:

$$s = \frac{n_s - n_r}{n_s}. \qquad (3)$$

The speed of the rotor relative to the stator field is $(n_s - n_r)$, and the frequency of the rotor e.m.f., f_r, is therefore given by:

$$f_r = \left(\frac{n_s - n_r}{n_s}\right) f_s,$$

or:

$$f_r = sf_s. \qquad (4)$$

For constant flux, the magnitude of the rotor e.m.f., and therefore I_r, is proportional to s, so that as load is added to an induction motor, additional torque is produced by an increase in fractional slip. Since the rotor impedance is low, a small increase in slip produces a large increase in rotor current, the full-load slip being typically 3 to 5%. When rotor current flows, there is a corresponding increase in stator current.

Provided that the fractional slip is small, torque will increase with increasing slip. However, as the slip increases, the frequency of the rotor e.m.f. will increase (see Eq.4) so that rotor reactance will rise, together with the phase angle θ_r. With increasing slip, the motor torque therefore reaches a maximum and then falls. This maximum value is called the pull-out torque, and the motor will stall if this peak value is exceeded. Controlled operation of the speed drive therefore requires that slip variations do not exceed the limit defined by the pull-out torque.

The variation of torque with fractional slip for a typical squirrel-cage motor of the standard type is shown in Fig.1. This curve has been extended into the generator mode, where the rotor speed is greater than the synchronous speed. In this region, the motor converts mechanical energy into electrical energy which is partially absorbed by the power converter system, or returned to the supply. The generator mode occurs when the load drives the motor at super-synchronous speeds, as in crane drives. It can also occur in a variable-frequency system when the supply frequency is rapidly reduced.

Under direct-on-line starting conditions, the fractional slip is unity, so that the rotor frequency and reactance are both high. This implies a high motor current at a low power factor so that the starting torque is low (see Eq.2). By increasing the rotor resistance, the power factor can be increased and starting torque improved (see Fig.1). However, under running conditions the motor will then operate at reduced efficiency due to high I^2R losses. In practice, rotor design is a compromise between the needs of starting performance and efficiency, and while there are ways of reducing this conflict, such as the double-squirrel-cage design, starting performance remains a potential weakness of the induction motor when operated under constant-frequency conditions.

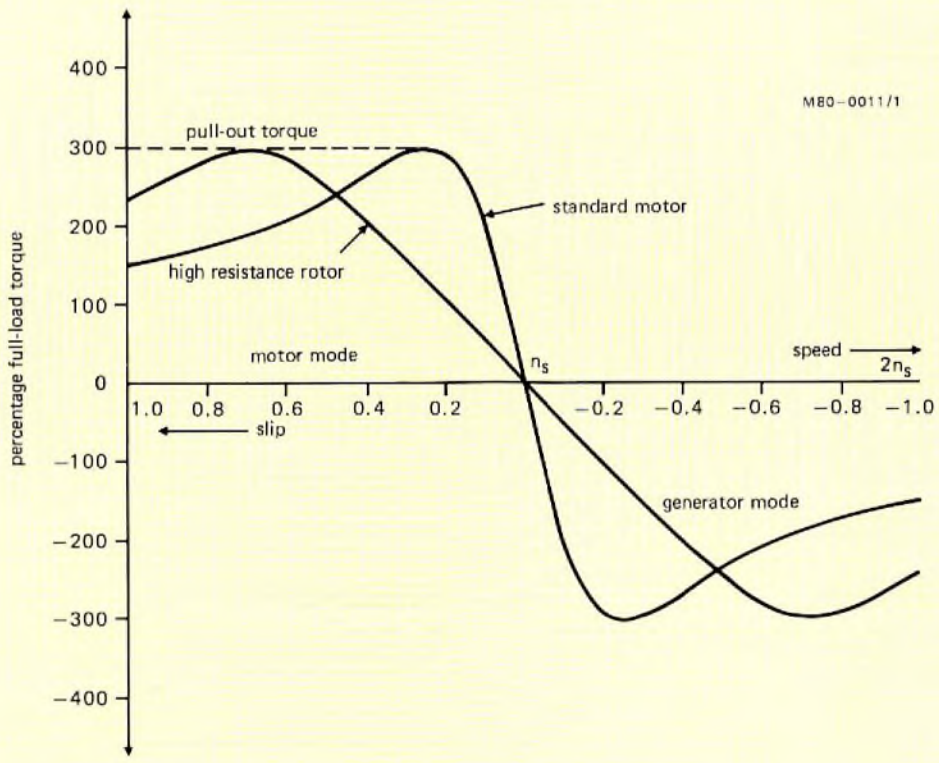

Fig.1 Variation of torque with slip for a standard squirrel-cage motor, and a motor with a high resistance rotor

PWM DRIVE FOR A.C. MOTORS

From Eq.1 it can be seen that varying the input frequency to the stator will result in a corresponding change in the synchronous speed. Since under normal operating conditions the rotor speed is only a few percent less than the synchronous speed, this provides a method of continuously changing the motor speed. To maintain constant full-load torque, the air-gap flux must be held constant, and this requires an applied voltage which must be varied in linear proportion to the input frequency. The speed/torque characteristics for an induction motor operating under constant flux and variable frequency are shown in Fig.2.

Our PWM drive system (see Ref.1) is designed to provide this type of variable speed constant-torque operation. A block diagram of the system is shown in Fig.3. The three-phase mains input is connected to the bridge rectifier via an interference filter. The d.c. voltage V_{Cb} is smoothed by a capacitor input filter (a choke input filter may be used for higher powers), and then applied to the inverter. The outputs from the three phases of the inverter consist of sinewave-weighted pulse-width-modulated waveforms at the selected carrier frequency; this gives sinusoidal motor currents with low harmonic content. The form of the inverter output waveforms is determined by the timing of the trigger pulses, generated by the PWM IC, HEF4752V. This IC forms the central feature of the PWM drive system, and the analogue control section effects changes in the motor performance solely by varying the inputs to the IC.

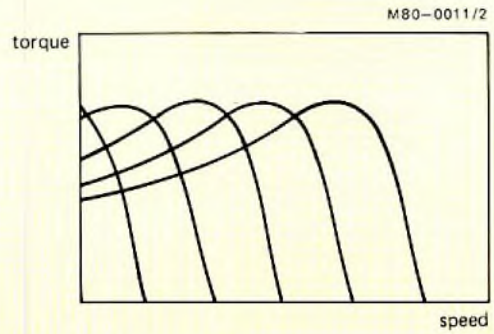

Fig.2 Induction motor speed/torque characteristics under constant flux and variable input frequencies

The operation of the IC is defined by a digital signal CW, which controls the direction of motor rotation, and four clock inputs FCT, VCT, RCT, and OCT. The four clock inputs have the following functions.

- FCT (Frequency Clock Trigger). This determines the stator frequency, thereby controlling the motor speed.
- VCT (Voltage Clock Trigger). This determines the stator frequency/voltage ratio.
- RCT (Reference Clock Trigger). This sets the inverter maximum switching frequency.
- OCT (Output Clock Trigger). This sets the minimum pulse-width allowable.

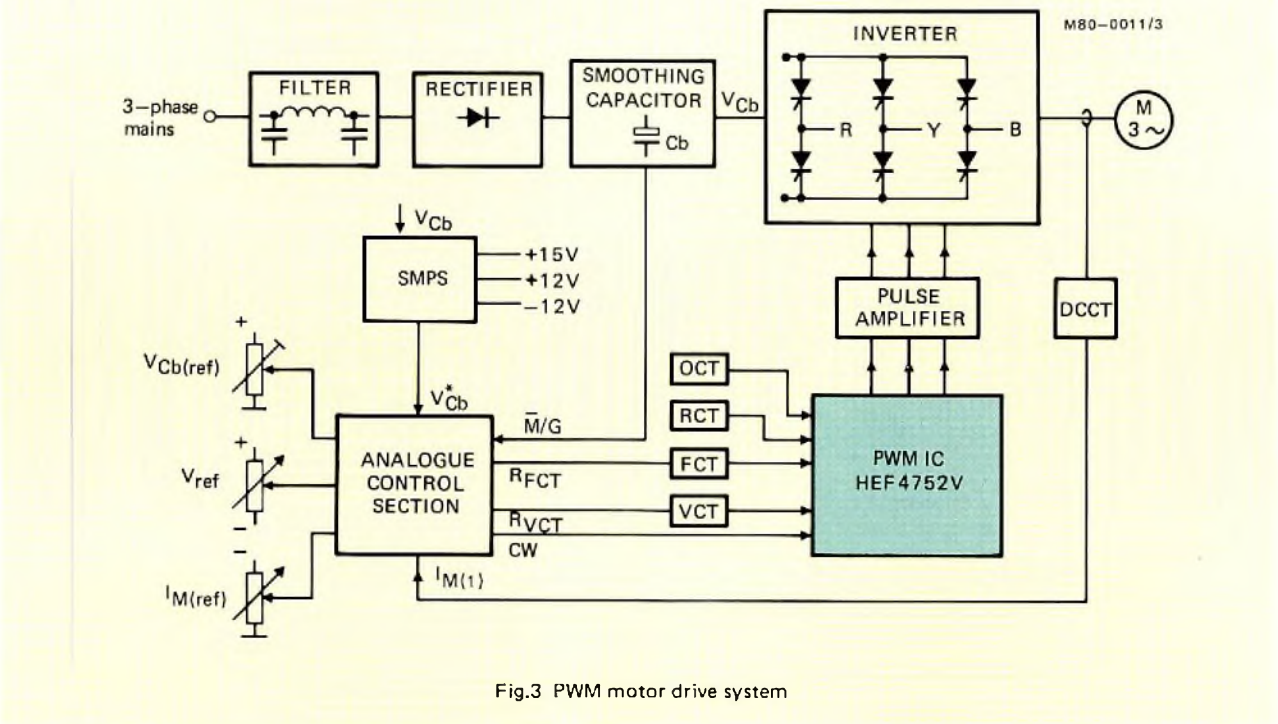

Fig.3 PWM motor drive system

The clock inputs of FCT and VCT are determined by wide-frequency-range voltage-controlled oscillators (VCOs), while the clock inputs of RCT and OCT are fixed for a given application, and can be controlled by VCOs or fixed oscillators.

The analogue control section produces three outputs: the digital signal CW, and voltage reference signals R_{FCT} and R_{VCT} for the VCOs of FCT and VCT. There are six inputs to the analogue control section: three are feedback signals, and three are potentiometer settings. The three feedback signals are: a voltage V^{*}_{Cb} which is proportional to the voltage across the smoothing capacitor, the motor current signal $I_{M(1)}$, sensed by a D.C. Current Transformer (DCCT) in the motor current lines, and a digital signal $\overline{M}/G$, derived from the power rectifier/filter circuit, indicating whether the motor is in the motor mode or generator mode. The potentiometer settings V_{ref}, $I_{M(ref)}$, and $V_{Cb(ref)}$ respectively set the motor speed, limit motor current in the motor mode, and limit the d.c. voltage in the generator mode. A fuller explanation of the function of the various input/output signals, is given in the next section.

ANALOGUE CONTROL SECTION

The analogue control section is designed to ensure safe and effective speed control under variable load and variable speed conditions. It provides the following facilities.

- Bidirectional control of motor speed from zero up to twice nominal speed, with fast response.
- Adjustment of maximum motor current up to about 140% of the nominal value.
- Adjustment of acceleration and deceleration time during motor speed variation.
- Limitation of motor current and voltage to protect the inverter, and to keep the motor operating within the specified slip range.
- Adjustable slip correction to improve speed regulation with load variation.
- Adjustable IR compensation to increase the starting torque.
- Protection circuits to ensure safe switch-on/switch-off performance.

The control section can be subdivided into four separate, but interrelated, circuits: the start/stop circuit, the speed reference circuit, the current/voltage control circuit, and the IR-compensation circuit. Each of these four circuits will now be considered in turn.

Start/stop circuit

Strictly speaking, the start/stop circuit is peripheral to the analogue control section represented as a block in Fig.3. However, it provides a number of important functions essential to the safe operation of the drive system, and a brief description of its operation is therefore given. A block diagram showing the essential features of the start/stop circuit, and its position in the total drive system is shown in Fig.4.

The circuit protects the system against adverse start/stop conditions, and provides the reset signal for the PWM IC. After switch-on, the three-phase rectifier

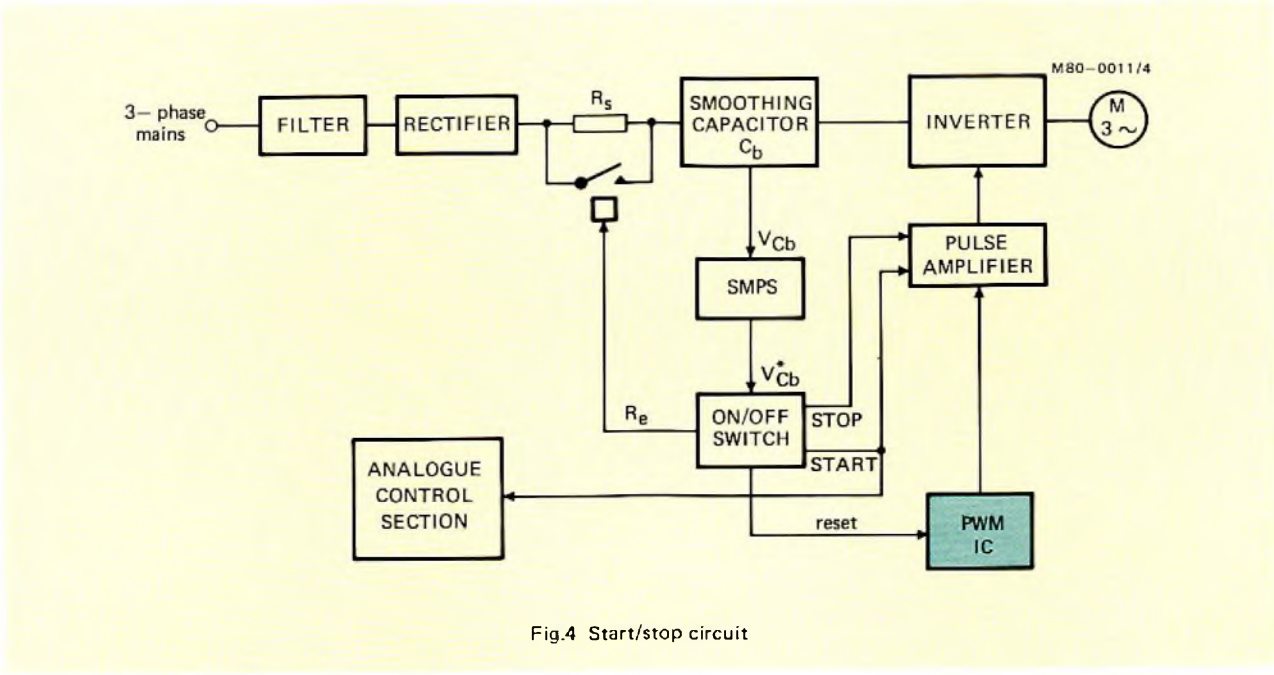

Fig.4 Start/stop circuit

charges the smoothing capacitor C_b via a limiting resistor R_s, protecting the rectifier diodes against inrush currents. When V^*_{Cb} exceeds 80% of its nominal value, the signal R_e closes the relay which short-circuits R_s. After a delay, determined by the action of a ramp generator, the PWM IC is reset. With the IC reset, the START signal goes HIGH, and the start procedure is complete.

When the mains supplies are disconnected, the capacitor C_b starts to discharge. When V^*_{Cb} is at 80% of its nominal value, the STOP signal goes HIGH, inhibiting the inverter action. Below this level, the commutation currents of the inverter are too low for safe commutation of the motor currents. The STOP signal remains HIGH until C_b has discharged. Figure 5 shows the various signals associated with the start/stop procedure.

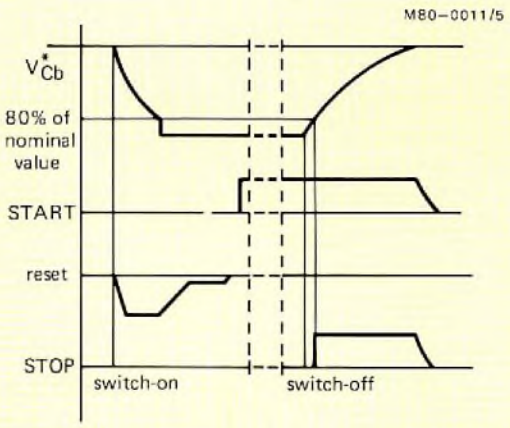

Fig.5 Start/stop signals

Speed reference circuit

The rate at which the speed of a motor can be changed is limited by the inertia of motor and load, and the available motor torque. As the stator frequency is altered, there is an inevitable lag in the response of the rotor, resulting in an increase in slip. Unless some limitation is placed on

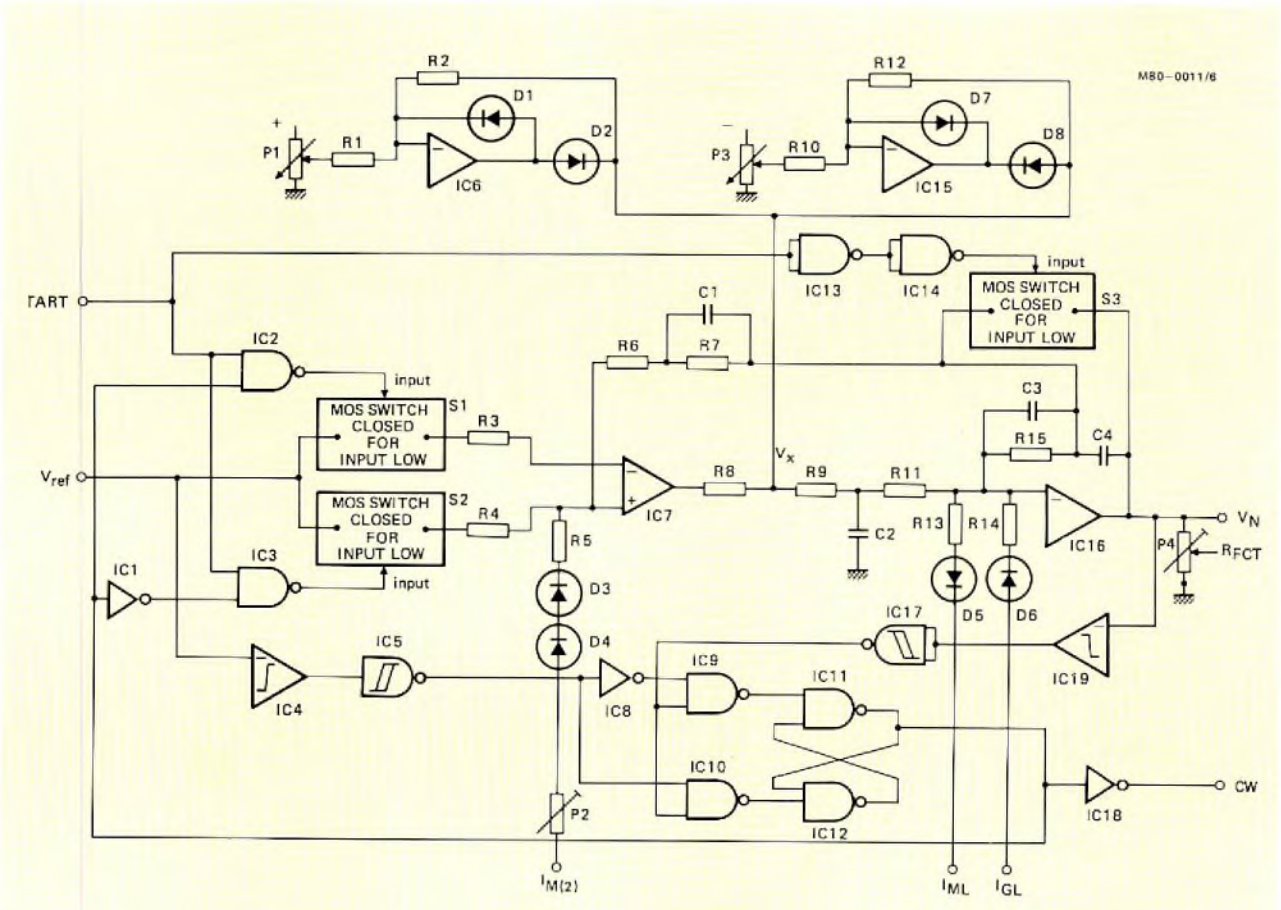

Fig.6 Speed reference circuit

the rate at which the stator frequency can change, the increase in slip can result in the pull-out torque being exceeded and the motor stalling. The speed reference circuit gives bidirectional speed variation together with control over the maximum rates of increase (acceleration control), and decrease (braking control) in the stator frequency.

A simplified circuit diagram is shown at Fig.6. The motor speed is determined by the potentiometer setting V_{ref}. This can be changed from −10 V to +10 V, changing the motor speed from maximum clockwise to maximum counter-clockwise. The speed signal output V_N is derived from V_{ref} via a comparator IC_7, and an integrator IC_{16} to give $V_N = -k|V_{ref}|$. A stepwise variation of V_{ref} results in a linear increase or decrease of the output signal V_N. The rate of variation of V_N can be adjusted via the accelerate/decelerate limiting potentiometers P_1 and P_3. The output V_N is grounded as long as the START input is low. The voltage output R_{FCT}, proportional to V_N, controls the frequency of the FCT clock, which in turn sets the inverter output frequency and hence determines the motor speed. The third output CW, controls the direction of rotation of the motor. Inputs I_{ML} and I_{GL} protect the inverter against overload conditions, while input $I_{M(2)}$ gives improved speed regulation for large load variations. The action of these three inputs is considered in detail under the discussion of the current and voltage control circuit.

Circuit operation

The influence of changes in input signals V_{ref} and START, on the output signals V_N and CW is shown in Fig.7. The features of the circuit operation which give rise to the results of Fig.7 are now considered.

At t_0 START is LOW, V_{ref} is positive, and CW is HIGH. The outputs of IC_2 and IC_3 will therefore be HIGH, so that MOS switches S_1 and S_2 will be open and no reference signal is supplied to the comparator IC_7. The output of IC_{14} will be low, so that MOS switch S_3 is closed and capacitor C_4 short-circuited. The speed output signal V_N is then zero.

At t_1 START now goes HIGH, together with the output of IC_{14}, so that S_3 is opened. The output of IC_3 goes LOW, S_2 is closed, and V_{ref} is supplied to the non-inverting input of comparator IC_7. The output of IC_7 is positive and the integrator IC_{16} ramps to a negative value. The slope of the integrator output voltage is determined by voltage V_x, resistors R_9 and R_{11}, and capacitor C_4; that is:

$$\frac{dV}{dt} = -\frac{V_x}{C_4(R_9 + R_{11})} \qquad (5)$$

As described below, the value of V_x can be limited by potentiometers P_1 and P_3 to give maximum rates of deceleration and acceleration respectively.

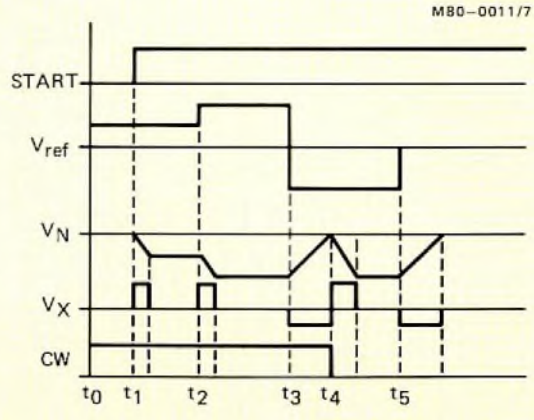

Fig.7 Input/output signals of the speed reference circuit

At t_2, V_{ref} is increased and V_N ramps to a more negative value.

At t_3 the input voltage V_{ref} is now reversed to a negative value, the output of IC_7 goes negative, voltage V_x is negative, and the integrator IC_{16} begins to ramp up. This implies a decelerating motor. The change in sign of V_{ref} causes the reference polarity detector IC_4 to switch the output of IC_5 from HIGH to LOW.

At t_4 the output of IC_{16} now reaches a slightly positive value, and the reference polarity detector IC_{19} switches the output of IC_{17} from LOW to HIGH. The flip-flop, IC_{11} and IC_{12}, now set via IC_9, and the output of IC_{11} goes HIGH so that CW goes LOW. With the CW signal LOW, the output of IC_3 goes HIGH and S_2 is opened, and the output of IC_2 goes LOW and S_1 is closed. This transfers the V_{ref} signal from the non-inverting to the inverting input of IC_7. This action ensures that the output of IC_7 is positive whenever the motor is accelerating, irrespective of the direction of rotation. The output V_N now ramps down to a value determined by the setting of V_{ref} at t_3.

At t_5, V_{ref} is set at zero, the output of IC_7 goes negative, and V_N ramps up to zero, bringing the motor to rest.

Limitation of the rate of speed variation

The maximum rate of speed variation is limited by controlling the maximum positive and negative values of V_x. The maximum positive value $V_{x(max)}$ is determined by the setting of potentiometer P_3 and the inverting operational amplifier IC_{15}; that is:

$$V_{x(max)} = -V_{p3}\,\frac{R_{12}}{R_{10}}, \qquad (6)$$

where V_{p3} is the voltage set by potentiometer P_3. Similarly, the maximum negative value of V_x is determined

by potentiometer P_1 and the inverting operational amplifier IC_6.

Suppose that the motor is accelerating; V_x will be positive. If V_x exceeds $V_{x(max)}$, then diode D_8 will conduct clamping V_x to $V_{x(max)}$. If V_x exceeds the preset maximum negative value while decelerating, then diode D_2 will conduct, clamping V_x to the maximum negative value. In this way independent control of acceleration and deceleration is obtained.

Current and voltage control circuit

The purpose of this circuit is to provide the I_{ML}, I_{GL}, and $I_{M(2)}$ signals for the speed reference circuit. As explained above, I_{ML} and I_{GL} limit the motor current and applied voltage to below the maximum capacity of the inverter, while $I_{M(2)}$ provides a degree of speed stabilisation under large loads. The protection of the inverter is considered first.

Inverter protection

In considering the problem of inverter protection, it is necessary to examine the requirements of the motor and generator modes separately.

In the *motor* mode, high motor currents will result if the required motor torque is too high, or the rate of acceleration is excessive. Both situations will give rise to high positive slip with correspondingly high currents. Motor current is controlled by *reducing* the synchronous speed so that the slip is also reduced.

In the *generator* mode, high motor currents can arise under braking conditions, or when the load drives the motor. In both cases, the motor speed can exceed the synchronous speed, giving negative slip. If this negative slip value is high, motor current will become excessive. By *increasing* the synchronous speed the slip is reduced and the motor current brought under control. There is a further complication in the generator mode, since the design of the control section does not allow for the return of energy to the supply; instead, any energy generated by the motor is initially stored in the smoothing capacitor. Without some limitation on the rate at which energy is fed to this capacitor the applied voltage could exceed the voltage rating of the inverter. To ensure that this voltage does not exceed a preset maximum value, the circuit reduces the synchronous speed at a slow enough rate so that power generation is just compensated by the power losses of the inverter and motor. In practice, limiting braking torque in this way still provides a fast braking action, even with large load inertia.

A circuit diagram is shown at Fig.8. The circuit has three input signals $I_{M(1)}$, $\overline{M}/G$ and V^*_{Cb}. The output signals are I_{ML}, I_{GL} and $I_{M(2)}$. Signal I_{ML} is the current limiting signal in the motor mode, while I_{GL} is the current limiting signal in the generator mode.

To reduce motor current in the motor mode, I_{ML} is driven negative. Diode D_5 of Fig.6 then conducts, so that the negative value of V_N is reduced, thus the synchronous speed falls and the slip is reduced. For excessive motor current conditions in the generator mode, I_{GL} is driven positive. Diode D_6 of Fig.6 then conducts, the negative value of V_N is increased, the synchronous speed rises, and the slip is again reduced.

The switch between I_{ML} and I_{GL} is controlled by the input $\overline{M}/G$. Signal $\overline{M}/G$ is LOW for the motor mode and HIGH for the generator mode. With $\overline{M}/G$ set LOW, the output of IC_3 (Fig.8) is HIGH. This clamps the output of IC_7 (Fig.8) negative, so that diode D_6 (Fig.6) inhibits the I_{GL} signal. With $\overline{M}/G$ HIGH, the output of IC_6 (Fig.8) is HIGH, keeping I_{ML} at a high level so that diode D_5 (Fig.6) inhibits the I_{ML} signal.

The measured motor current signal $I_{M(1)}$, sensed by the DCCT in the motor current lines, is amplified and filtered by IC_1 (Fig.8) and smoothed by capacitor C_2 to suppress the sampling ripple frequency of the measuring circuit. The output of IC_1, signal $I_{M(2)}$, is then supplied to the current limiting control amplifier IC_5, where it is compared with the current reference signal for the motor mode $I_{M(ref)}$. This circuit works as a 3-term error amplifier with proportional-integral-derivative control action. The proportional gain of the circuit is given by R_{18}/R_{11}. The crossover frequencies for the differential action are determined by the values of R_{11}, R_{12}, and C_7, while the crossover frequencies for the integral action are given by C_8, R_{17}, and R_{18}. The use of the differential network gives an optimal response for the current-limiting signal and prevents overshoot. By varying the setting of potentiometer $I_{M(ref)}$, the maximum motor current for the motor mode can be adjusted from 70% up to 140% of the nominal motor current. Current limiting below 70% can cause instabilities, because the motor current cannot be decreased below the magnetising current.

Control of motor current in the generator mode is achieved by supplying the $I_{M(2)}$ signal to the second error amplifier IC_2, where it is compared with the pre-adjusted reference signal $I_{G(ref)}$. As soon as $I_{M(2)}$ exceeds $I_{G(ref)}$, which sets the current limit level in the generating mode, the output of IC_2 goes negative. This signal is fed to a unity-gain inverting amplifier, IC_7, and then the resulting positive signal I_{GL}, is supplied to the speed reference circuit where it increases the synchronous speed, under current limit conditions in the generating mode.

To limit the applied voltage in the generator mode, the negative V^*_{Cb} signal, which is proportional to the voltage across the smoothing capacitor, is supplied to a third error amplifier IC_4, and compared with the adjustable maximum reference value $V_{Cb(ref)}$. For V^*_{Cb}

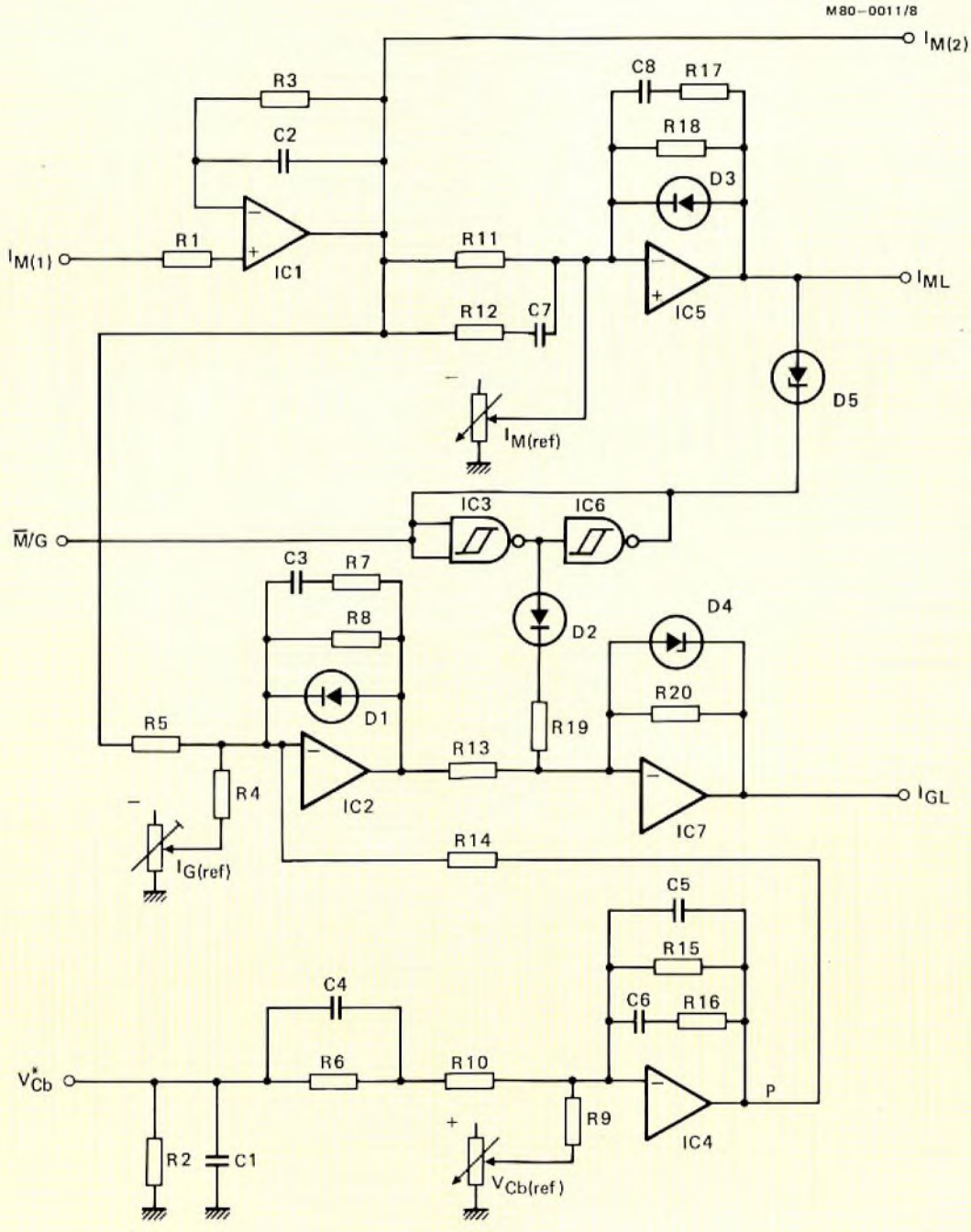

Fig.8 Current and voltage control circuit

greater than $V_{Cb(ref)}$ the output signal P of IC_4 goes positive. This signal is supplied to the input of IC_2, where it effectively reduces the current reference level for the generator mode until the regenerative power is just equal to the power losses in the inverter and motor. The response of the current and voltage control circuit under variable speed conditions is shown in Fig.9. The lower trace of Fig.9b shows the change in synchronous speed following a stepwise variation in the V_{ref} input of the speed reference circuit. It shows a fast speed response, with an acceleration time of 0.8 seconds, and a braking time of one second. The motor current is limited to a peak value of 8 A on acceleration, and to a peak value of 7 A on braking (lower trace Fig.9a). The maximum voltage on braking is 700 V (upper trace Fig.9a).

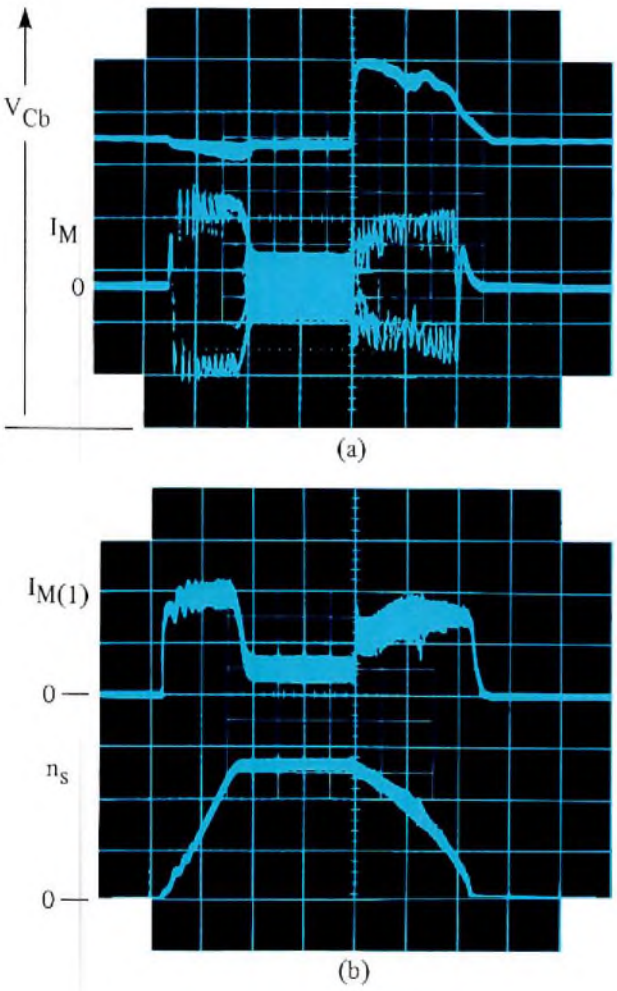

Fig.9 Current and voltage waveforms during speed change conditions
(a) upper trace – supply voltage V_{Cb} (100 V/division)
lower trace – motor current I_M (5 A/division)
(b) upper trace – DCCT output $I_{M(1)}$ (corresponds to I_m of approximately 3.5 A/division)
lower trace – synchronous speed (approximately 700 rev/min per division)
time scale: 0.5 s/division

Slip correction

Under increasing motor torque, the slip will increase, so that for a fixed synchronous speed the motor speed falls. The output of IC_1, signal $I_{M(2)}$, which is proportional to I_M, may be used to give improved speed regulation under variable load conditions.

The $I_{M(2)}$ signal is supplied to the non-inverting input of IC_7 (Fig.6) where its effect is to make V_N more negative, thus giving a higher synchronous speed and in turn a higher motor speed. The degree of slip correction can be varied with potentiometer P_2 (Fig.6).

The effectiveness of this technique of speed regulation is reduced for low-power standard asynchronous motors, where the magnetising current is a significant proportion of the load current. However, even with motors of this type, the speed deviation from the no-load to full-load condition can be reduced by 50 to 80%.

IR – compensation

With a variable frequency drive system, the motor is started at a low input frequency and then brought-up to the desired operating speed by a steady increase in frequency, and a motor voltage proportional to this frequency. In this way, the high motor currents, and low power factor associated with starting a fixed frequency system are avoided. However, the low input frequency will also result in a low applied motor voltage.

At low frequencies the voltage drop across the stator resistance is, therefore, relatively large when compared with the applied voltage. These high IR losses will result in a low air-gap flux, and consequently a low starting torque. If a high starting torque is required, it can be achieved by increasing the applied voltage at low frequencies.

The value of the applied voltage at a given input frequency is determined by the VCT clock input of the IC. Reducing the frequency of this clock will increase the applied voltage for a given input frequency, while increasing the clock frequency has the opposite effect. A full discussion of the relationship between the VCT clock and input frequency is given in Ref.3. The frequency of the VCT clock is determined by its voltage reference signal R_{VCT}, so that IR-compensation requires the modification of R_{VCT} for low input frequencies.

A circuit to obtain this modification is shown at Fig.10. The circuit has a single input, the negative speed signal V_N derived from the speed reference circuit, and a single output R_{VCT}. For values of V_N which are less negative than the value given by:

$$V_N = V_{p1} \frac{R_1}{R_3} , \qquad (7)$$

where V_{p1} is the voltage set by potentiometer P_1, the circuit decreases the negative value of R_{VCT}, while for

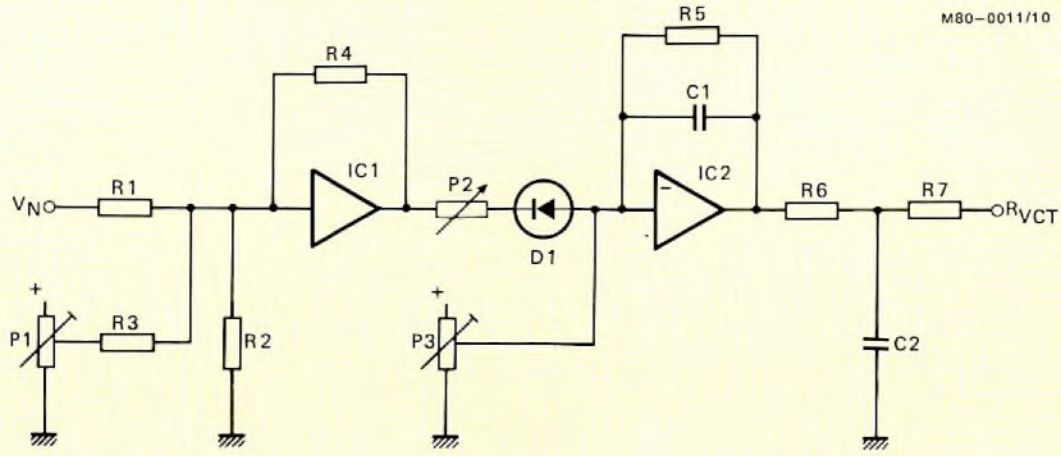

Fig.10 IR-compensation circuit

values of V_N which are more negative than the value defined by Eq.7, the output signal R_{VCT} is adjusted by potentiometer P_3 to obtain the nominal rated motor voltage. Equation 7 therefore defines the region of IR-compensation. For V_N as given by Eq.7, the output of IC_1 is zero, while for less negative values the output of IC_1 becomes increasingly negative, driving the output of IC_2 and thus R_{VCT} less negative. For more negative values, the output of IC_1 is blocked by diode D_1. Within the region of IR-compensation, the influence of V_N on R_{VCT} can be adjusted with potentiometer P_2. Figure 11 shows the effect of IR-compensation on the average applied voltage V_{AV}, and illustrates the roles of the three potentiometers P_1, P_2, and P_3.

The next article in this series will describe the D.C. Current Transformer (DCCT), which is used to sense the motor current.

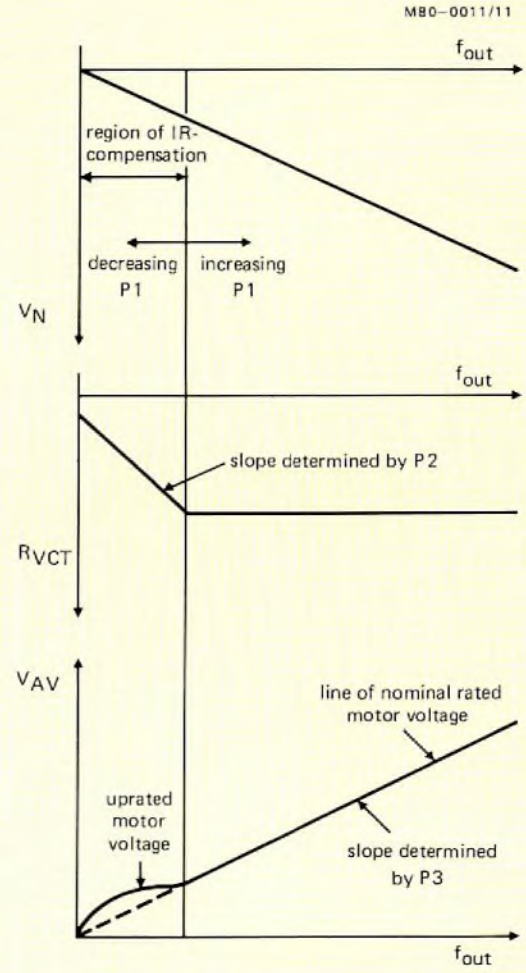

Fig.11 Signals for IR-compensation

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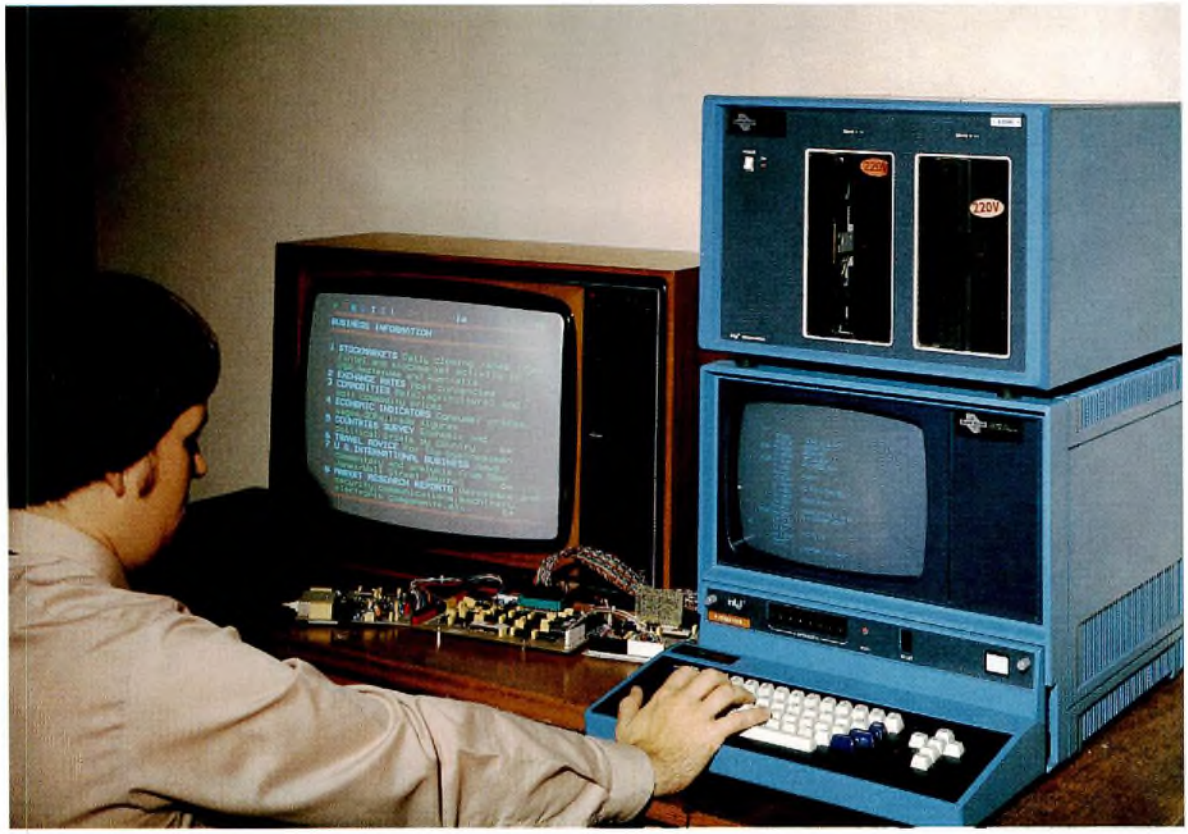

The television receiver is the display medium for viewdata systems, providing access to a library of computer stored data, which is transmitted via a telephone line. The world's first public viewdata service, Prestel, was developed by the British Post Office. Prestel is now available in three European countries – shortly increasing to five – and also in Hong Kong. Similar viewdata services are under intensive development throughout the world, and it is clear that the next few years will see a dramatic expansion in the availability of viewdata.

Our new LSI circuit, type SAA5070, is a microprocessor peripheral, designed for application in the latest generation of viewdata decoders. For microprocessor based systems of this type, software development represents a major part of the total design effort.

The SAA5070 chip has a very high circuit density, so that the IC package count for basic viewdata acquisition is reduced to only four chips. The SAA5070 provides all the features that are essential for a basic viewdata system, as well as a comprehensive range of additional features that can be adopted as required. Since all features are under the control of the microprocessor software, the SAA5070 can be used in a wide variety of system designs, and has the flexibility to cope with future changes in viewdata specifications.

Two features of the SAA5070 are of particular interest: modem operation at 1200/1200, facilitating communication between viewdata terminals, and a tape recorder modem using a 'Kansas City' system which is very tolerant of speed variations. A comprehensive description of the IC will be given in an article appearing in the next issue of ECA, and additional technical information will shortly be available.

Highlight handling with diode-gun Plumbicon* tubes

A. FRANKEN and W. LOHUIS

Television scenes frequently contain highlights that are much brighter than the average scene illumination. Such highlights cannot be fully read out by the electron beam of the camera tube, and this results in the annoying effects of highlight *blooming* and *comet tailing* in the television picture. By increasing the beam current it is of course possible to reduce these effects significantly, but this also reduces resolution and increases lag. The problem of highlight handling has, however, been solved effectively in two ways.

The first solution came about 10 years ago with the development of the anti-comet-tail (ACT) gun (Ref. 1,2), the principle of which is shown in Fig.1. The ACT gun neutralises highlights by increasing beam current during flyback only (Fig.2), the remainder of the charge pattern then being read out in the normal way. ACT guns are now used in several types of Plumbicon tube (e.g. 25 mm XQ1080 and XQ1500, and 30 mm XQ1520).

The second and more recent solution came with the development of dynamic beam control (DBC), alter-

* Registered trademark for television camera tubes

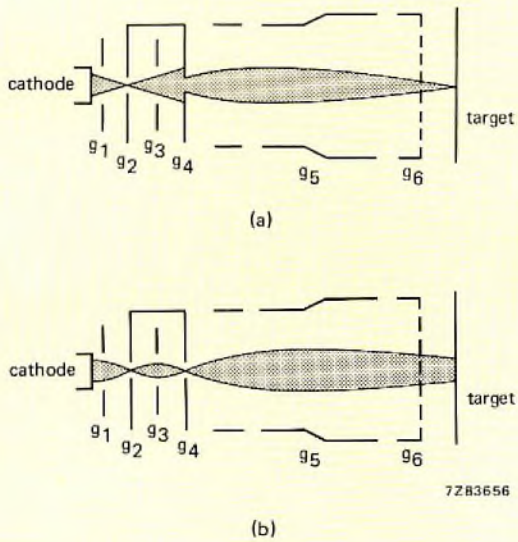

Fig.1 ACT electron gun with electron beam (a) during forward scan and (b) during flyback

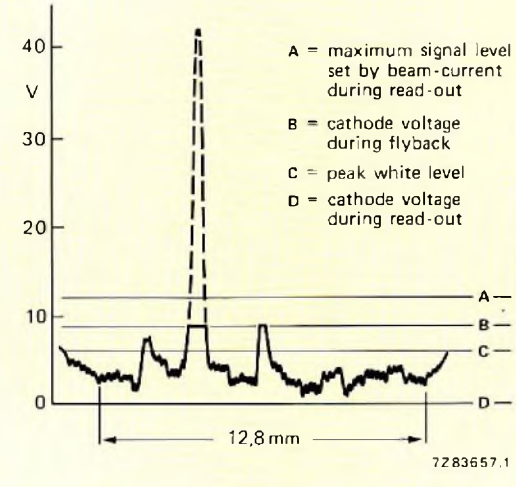

Fig.2 Voltage excursions V on the target layer of a Plumbicon tube. To read out the highlight during flyback, the ACT gun increases the beam current by raising V_{g1} and lowering V_{g3}. It also raises the cathode voltage to prevent the entire charge pattern being read out during flyback

natively known as comet-tail suppression (CTS). With DBC, beam current during forward scan increases only when a highlight is encountered. The wide beam-current excursions required for DBC effectively limit its use to camera tubes with large beam reserve. The new range of diode-gun Plumbicon tubes (Ref. 3, 4) which are characterised by very high slope (Fig.3) and large beam reserve are therefore ideal for this purpose.

This article describes the use of DBC in the diode-gun Plumbicon tubes, and briefly compares DBC with ACT.

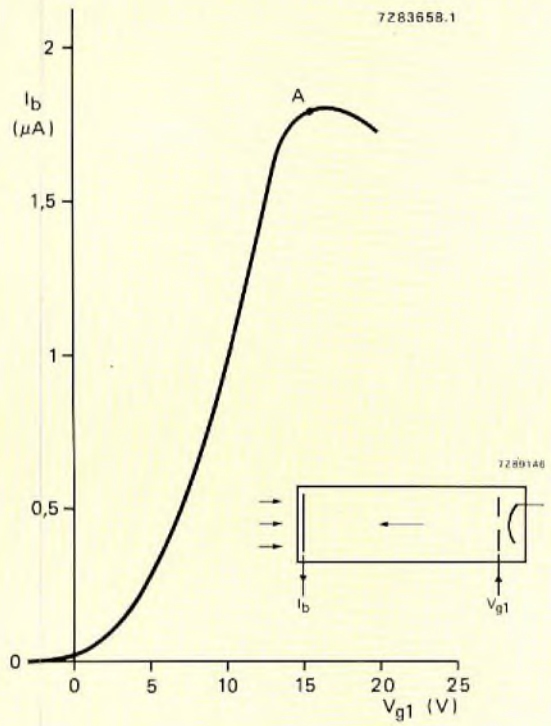

Fig.3 Beam current I_b of an XQ2427 diode-gun Plumbicon tube (measured with highly illuminated target) as a function of grid voltage V_{g1}. The diode-gun tubes are characetised by very high I_b/V_{g1} slope and large beam reserve, so they are ideally suited to DBC

The DBC concept

Figure 4 illustrates the principle of DBC. Signal current I_s varies according to the intensity profile across the target as it is scanned by the electron beam. When the beam encounters a highlight, the sharp rise in I_s is detected by a feedback network which then increases control grid voltage V_{g1}, so raising the beam current I_b to the required level to fully read out the hightlight.

The high slope of the diode-gun characteristic, besides providing the large beam reserve needed for DBC, significantly reduces the risk of oscillation in the feedback network.

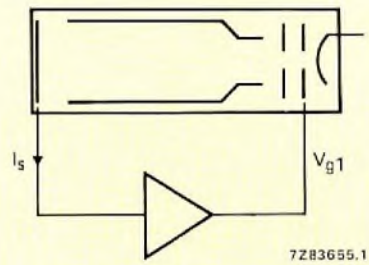

Fig.4 In the DBC system beam current I_b during forward scan increases only when a highlight is encountered. The system uses a feedback network that responds to sharp rises in signal current I_s by increasing V_{g1} and hence I_b

Operating principles

DBC makes use of the current range below saturation, i.e. below point A in Fig.3. Figure 5 illustrates the operation of a DBC circuit. The video signal from the preamplifier is fed to the video amplifier and to a threshold circuit, T, which compares the actual signal strength with a preset value defining the highlight threshold. Signals exceeding this threshold pass to the DBC amplifier and then to grid g_1.

To further reduce the risk of oscillation the DBC amplifier may have a limited bandwidth (1.5 MHz), and the feedback network includes a limiter, L, to keep the output voltage of the DBC amplifier within the required control range of the tube characteristics (i.e. voltage excursions $\Delta V_{g1} \leqslant +10\,V$ in the XQ2427 Series, $\leqslant +7\,V$ in the XQ2070 Series).

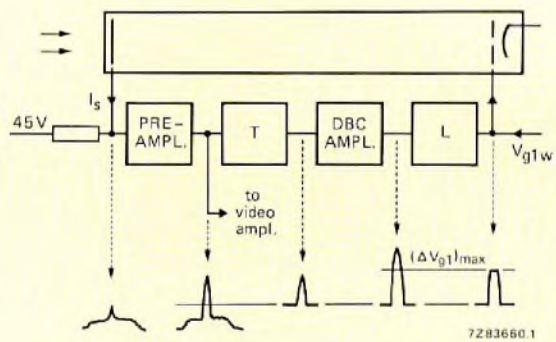

Fig.5 Block diagram of a typical DBC system. T, threshold circuit; L, limiter; V_{g1w}, normal operating voltage of the camera tube

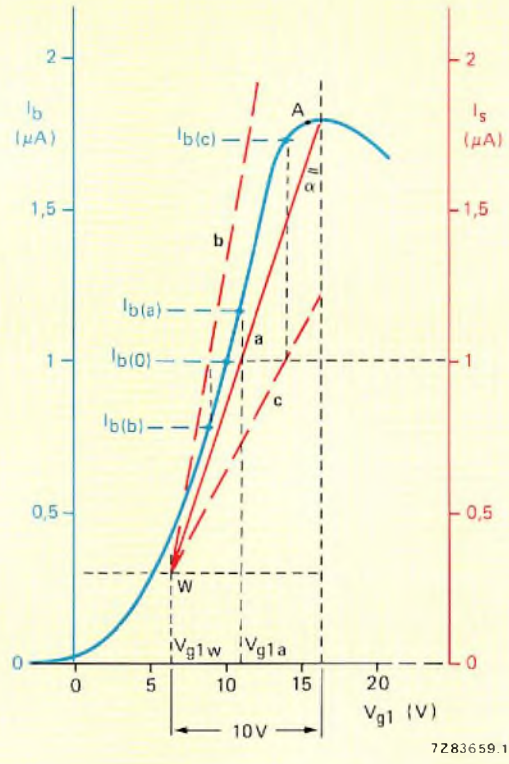

Fig.6 Beam current (blue) versus control grid voltage for a typical XQ2427 Plumbicon tube. The DBC system makes use of the range below saturation (point A), so voltage increases ΔV_{g1} are limited to a maximum of 10 V above normal operating voltage V_{g1w}. The I_s/V_{g1} slope of the DBC amplifier is given by line a (red), so a highlight signal of, say, 1 μA will cause the control grid voltage to increase to V_{g1a}, which in turn produces a beam current $I_b(a)$

DBC amplifier characteristics

Figure 6 shows the beam-current versus grid-voltage characteristic of a typical diode-gun Plumbicon tube (XQ2427) and the signal-current versus grid-voltage characteristic of the DBC amplifier. Ideally the slope of the DBC amplifier characteristic should precisely match the I_b/V_{g1} characteristic of the tube. The changes ΔV_{g1} in grid voltage accompanying a highlight occurrence would then follow exactly the blue curve of Fig.6, and I_b would increase by just the right amount to read out the highlight. So, in Fig.6, a highlight resulting in a signal current of say 1 μA would be just read out by the beam current $I_b(0)$.

In practice, however, such precise matching will itself lead to instabilities due to slight variations in the beam acceptance of the target. A practical compromise is to use an amplifier with the slope given by line *a* in Fig.6. A 1 μA signal current will then produce a beam current $I_b(a)$ slightly greater than that required to fully read out the highlight.

An amplifier with a slope given by line *b* would produce a beam current $I_b(b)$ somewhat less than that required to read out the highlight; an amplifier with a slope given by line *c* would produce a beam current $I_b(c)$ far greater than required, so although the highlight would be fully read out, the large beam current would inevitably lead to beam defocusing and loss of stability (which may show itself as a series of horizontal bands in the TV picture).

The amplifier slope is defined in Fig.6 by tan α. For the XQ2427 series of tubes tan α = 7 V/μA; and for the XQ2070 series tan α = 4 V/μA.

DBC in colour cameras

Figure 7 shows three ways in which DBC can be incorporated into a TV colour camera.

The set-up shown in Fig.7(a) requires three separate DBC systems since each tube is controlled independently. In Fig.7(b), a single DBC system in the green channel controls all three camera tubes. A drawback of this set-up is that it cannot respond to red and blue highlights. Figure 7(c) overcomes this drawback by employing a single DBC amplifier that receives highlight signals from each channel via a gating circuit. This set-up can read out highlights independently of colour, and since it uses only one DBC amplifier the risk of oscillation is considerably reduced.

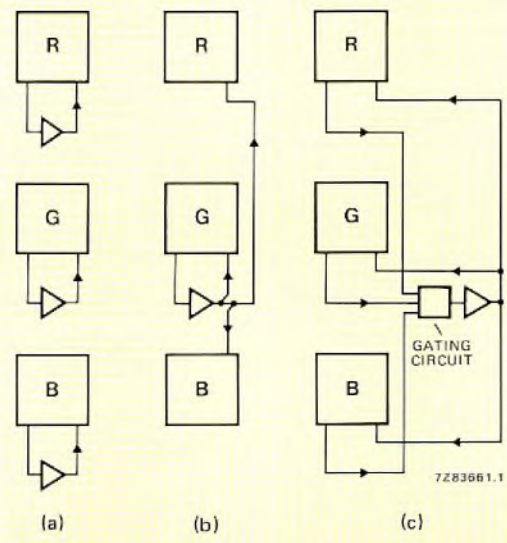

Fig.7 Three circuit configurations for a colour camera with channels R (red), G (green) and B (blue)

Instead of using one of the above systems, it might seem simpler merely to arrange for the beam current to rise to maximum whenever the signal current exceeds a threshold value (e.g. 0.3 μA). However, although this would simplify the electronic circuitry, the high beam current (which would occur even with low intensity highlights) would considerably increase the risk of instabilities.

DBC compared with ACT

The ACT gun, by neutralising highlights during flyback, avoids large voltage excursions during forward scan, so that beam bending and blooming effects are kept to a minimum. In contrast, DBC allows highlights to produce fairly large voltage excursions, but, nevertheless, the large beam current produced by DBC still keeps beam bending and blooming effects small.

ACT requires more complex circuitry than DBC, and moreover, may cause highlight currents as high as 50 μA to be fed to the video preamplifier (during flyback) compared with a maximum of only 2 to 3 μA with DBC.

Finally, compared with ACT, the DBC circuit is more compact and uses less power, important for small portable cameras as used in ENG and EFP.

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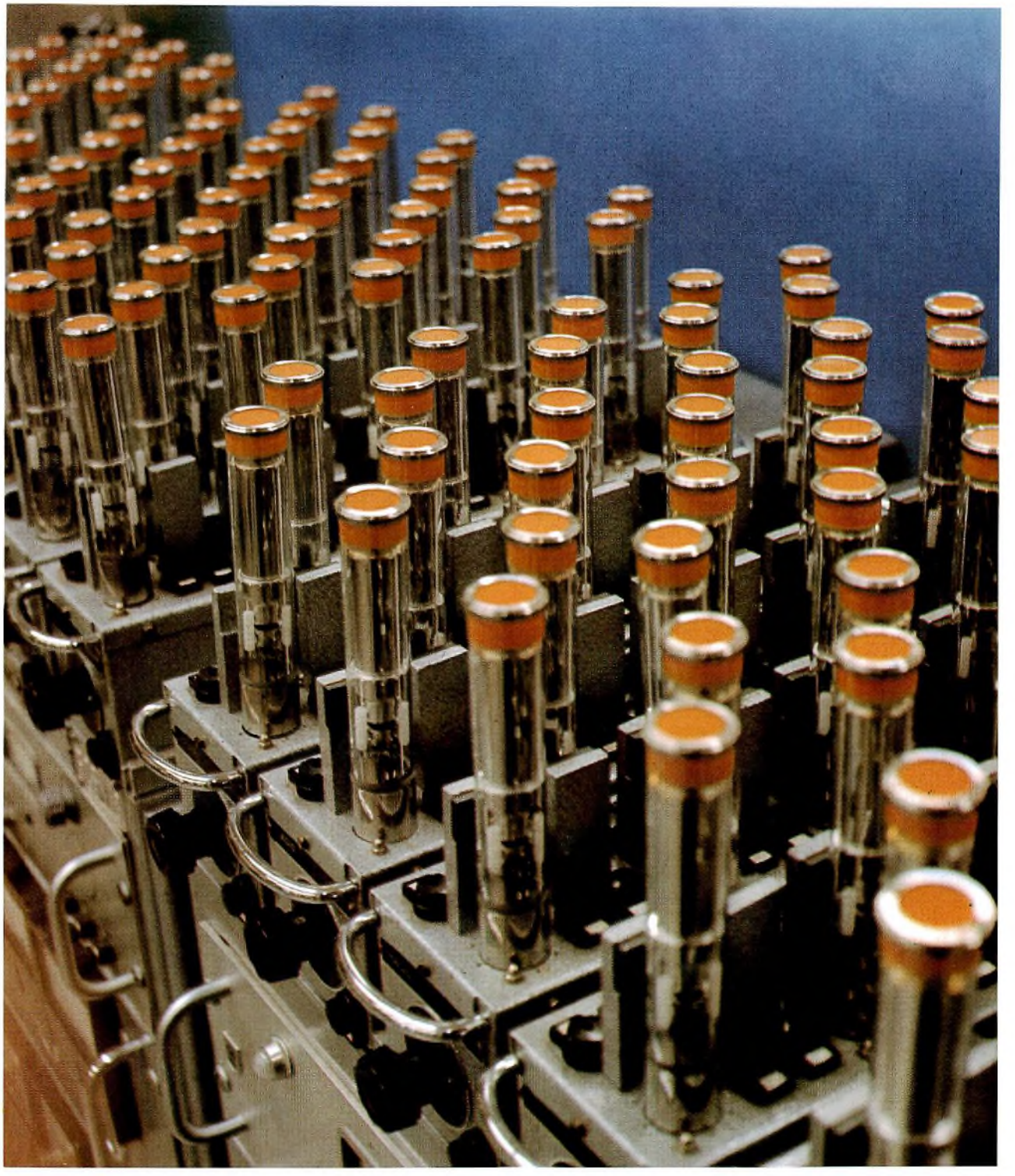


Beam current, an important parameter of camera tubes, depends to a large extent on cathode emission. Here, in one of the last stages of manufacture, the cathodes of a battery of Plumbicon tubes are undergoing a rigorously controlled programme of activation to achieve and stabilise the specified emission characteristics. The stability of these characteristics is an important factor contributing to the effectivenes and comparative simplicity of DBC.

Part 1 – Performance equations

Ceramic permanent magnets for d.c. motors

H. J. H. VAN HEFFEN

During the last fifteen years, the use of ceramic strontium-ferrite permanent magnets in low-voltage d.c. motors has increased enormously. Indeed, both economic and technical considerations make permanent-magnet motors of this type virtually mandatory for automobile windscreen-wiper, fan, and other low-power drives. Ceramic permanent-magnet motors are now being developed or are in use as starter motors, in domestic appliances such as washing machines, and for both high and low-voltage industrial applications. As a consequence, world production of d.c. motors with ceramic permanent-magnets is approaching 200 million units.

The growth in the use of ceramic magnets in motors is due not only to their low cost, but also to the performance of the newer anisotropic materials developed especially for motor applications. High values of intrinsic coercivity can be realised in materials that can easily be formed into magnets of the shapes most suitable for d.c. motors.

This article reports the results of a study carried out on the relationships between the characteristics of the magnetic material, the specification of the motor, and the volume of magnetic material required. This study was based on existing treatments of the magnetic aspects of d.c. motor design as given in the literature. The motor model used as a basis for calculation was chosen such that common, basic design formulae could be used without modification. The main results yielded by the study are:

- That the motor constant C_m (the product of the total flux through the rotor and the number of active conductors) depends only on the ratio of the working torque to the stall torque and not on their absolute values. A factor C has been introduced for this ratio, and a simple method of estimating the value of C_m derived.
- That the product of the total magnetic flux through the rotor and the effective back m.m.f. due to the stall current is equal to one quarter of the product of the winding angle and the stall torque due to that stall current. This rule makes possible the determination of the maximum stall torque obtainable with a given set of magnets.
- For each grade of ceramic magnet material, a quality factor Q_d for motor applications can be calculated that depends on the values of remanence, intrinsic coercivity and a recoil factor.
- That the minimum volume of the permanent magnets in a d.c. motor must be

$$V_f = f_m G/Q_d$$

where G is a geometric factor and f_m a motor factor that includes stall torque and winding angle.

- That the specific magnet volume

$$V_{f(s)} = G/Q_d$$

which is the volume per unit stall torque and unit winding angle, is the most suitable criterion for comparing grades of ceramic magnet material.

PERMANENT-MAGNET D.C. MOTORS

All symbols for quantities used in this article are listed in the table; as far as possible, the recommendations of IEC Publication 27 have been followed. All quantities are expressed in SI base units.

List of symbols

Note: all quantities are expressed in SI base units unless otherwise indicated.

symbol	*unit*	*definition*
a	–	number of parallel paths in the rotor
A_s	m^2	magnet area normal to the direction of magnetisation
B	T	induction
B_m	T	induction in the magnet at the working point
Bp	T	induction in the magnet at an arbitrary point P on the demagnetisation curve
B_r	T	remanence
C	–	torque ratio
C_m	V_s	motor constant
d	m	distance between rotor surface and inner wall of housing
d_s	m	thickness of magnet in direction of magnetisation
d_t	m	tooth width
D_a	m	rotor diameter
D_c	m	diameter of conductor on rotor
D_{ih}	m	inside diameter of housing
D_{is}	m	inside diameter of segments
D_{oh}	m	outside diameter of housing
D_{os}	m	outside diameter of segments
E	V	e.m.f. of power supply
E_b	V	voltage dropped across brushes
E_c	V	back e.m.f. from rotor
f	–	flux-loss correction factor
f_1	–	flux-loss correction factor for losses due to the rotor
f_2	–	flux-loss correction factor for losses due to segment overhang
f_m	Nm rad	motor factor
F	A	magnetomotive force
g	–	number of rotor slots
G	–	segment-geometry factor
H	A/m	magnetic-field strength
H_{cJ}	A/m	intrinsic coercive force
H_m	A/m	field strength due to a magnet at its working point
H_p	A/m	field strength due to a magnet at an arbitrary working point
H_{pn}	A/m	effective armature reaction at speed n
I_n	A	motor current at speed n
I_0	A	motor stall current
ℓ_r	m	rotor length
ℓ_s	m	segment length along the motor axis
M_{gn}	Nm	torque generated by a motor at speed n
M_{g0}	Nm	torque generated at n = 0 (stall)
M_n	Nm	stall torque
n	rev/s	motor shaft speed
p	–	number of stator pole pairs
P	W	power consumed
P_{gn}	W	power generated by rotor at speed n
P_{DR}	W/m^2	specific rotor dissipation
P_n	W	motor output power at speed n
q	–	reluctance factor for rotor iron
Q_i	–	quality number for rotor iron
Q_d	N/m^2	quality factor of a ceramic magnet materia
R	Ω	resistance
R_a	Ω	rotor resistance
R_b	Ω	brush resistance
R_c	Ω	connecting wire resistance
R_e	Ω	total resistance external to motor
R_i	Ω	internal resistance of power supply
S_n	A/m^2	current density at speed n
S_0	A/m^2	current density at stall
t	°C	temperature
V_f	m^3	minimum volume of stator magnets
V_{fs}	m^2/Nrad	minimum specific volume of stator magnet
w	–	number of conductors per rotor slot
Z	–	number of active rotor conductors
α	rad	angle subtended by a stator segment magne
α'	rad	active winding angle
γ_0	–	reversibility factor of magnet material
δ	m	airgap between magnet and rotor
$\eta(n)$	–	overall motor efficiency at speed n
$\eta_e(n)$	–	motor electrical efficiency at speed n
$\eta_m(n)$	–	motor mechanical efficiency at speed n
Φ	Wb	magnetic flux per stator pole pair
Φ_{tot}	Wb	total magnetic flux
τ_{HcJ}	%/°C	temperature coefficient of H_{cJ}
τ_{Br}	%/°C	temperature coefficient of remanence
μ_0	H/m	permeability of free space
μ_{rec}	–	relative recoil permeability

Calculation model

Permanent-magnet motors are made in a number of forms that can be classified according to

- motor construction
- stator construction
- rotor construction
- arrangement of the magnet system
- method of winding
- method of commutation.

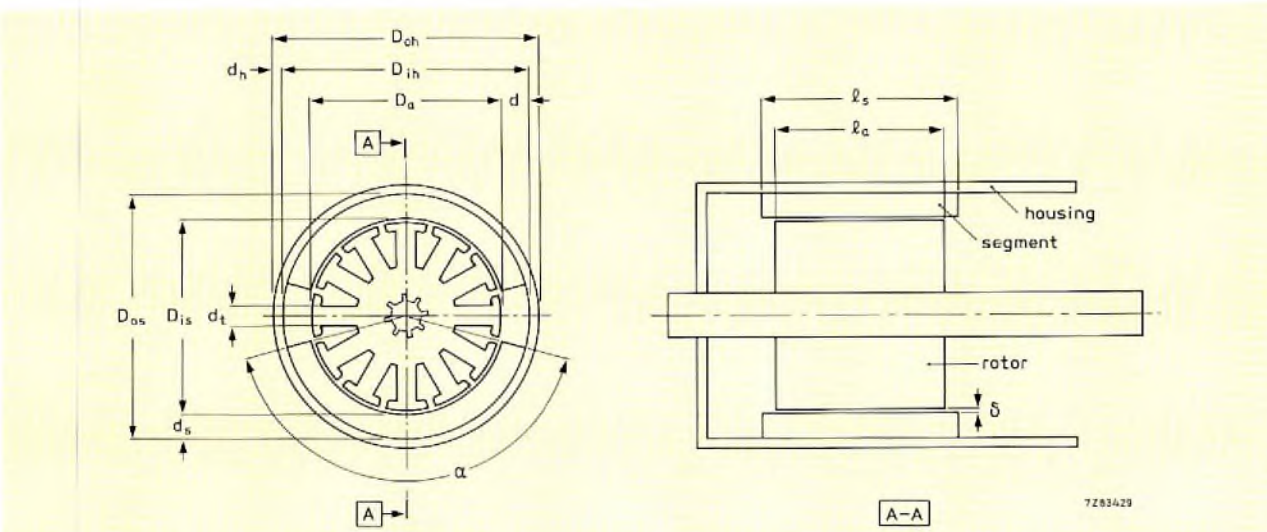


Fig.1 General arrangement of the design of permanent-magnet motor used as a calculation model

To simplify analysis, discussion will be mainly restricted to what might be termed the classic design of motor shown in outline in Fig.1. This comprises a cylindrical housing with an even number of segment magnets (giving an integral number of pole pairs) attached to its inner wall. These magnets are segment-shaped in transverse section and have cylindrical inner and outer walls with plane ends normal to their axes. They are not fitted with pole pieces and are treated during manufacture to obtain a radial preferred direction of magnetisation.

The rotor is laminated and has slots that accommodate the windings parallel to its axis. Single-lap winding is employed so that the winding angle is equal to the magnetic angle.

Current is applied to the commutator by an even number of brushes (an integral number of parallel circuits). Brush width is equal to or smaller than that of the commutator sections. Brushes are positioned so that no neutral line is coincident with a polar angle.

Power for the motor is supplied by a source of voltage E and internal resistance R_i. Supply-lead resistance, including any series resistor, is R_c.

In the following discussion, the term 'permanent-magnet motor' always refers to a model of this form.

Basic relationships

Three basic design relationships relate the characteristics of a d.c. motor to its magnetic requirements. That for the torque

$$M_{gn} = pZ\Phi\, I_n/(2\pi a) \qquad (1)$$

that for the back e.m.f.

$$E_c = npZ\Phi/a \qquad (2)$$

and that for the transverse field generated by the armature (the armature reaction)

$$H_{pn} = \frac{I_n Z\alpha'}{8\pi adq}. \qquad (3)$$

These expressions apply where the magnetic field due to the stator intersects the rotor slots at an angle of $\pi/2$ and where the number of active conductors over pole-angle α is $\alpha' z/2\pi$. These conditions apply in the model shown in Fig.1.

Figure 2 shows the equivalent electrical circuit of the model and power supply. One of two expressions may be used to relate the circuit voltages: either

$$E - E_c - E_b = I_n(R_a + R_c + R_i) \qquad (4)$$

or

$$E - E_c = I_n(R_a + R_b + R_c + R_i). \qquad (5)$$

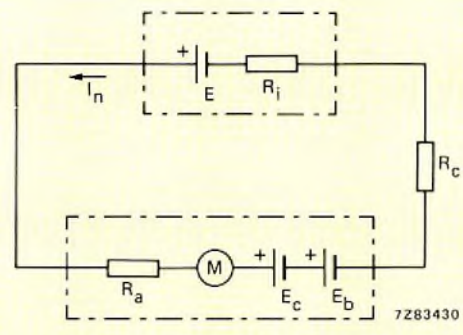


Fig.2 Equivalent electrical circuit of the permanent-magnet motor discussed in this article

Equation (4) is used where the voltage drop across the brushes themselves is fairly constant, as is usually the case at high current and low speed. Equation (5) is used where the brushes behave resistively, which is the case at low currents and high speed. For the motor model used here, eq. (4) is preferred since the voltage drop due to the brushes is fairly constant over the whole working range of the motor.

If resistances R_c and R_i are treated as a single external resistance R_e, eq. (4) simplifies to

$$E - E_c - E_b = I_n(R_a + R_e). \quad (6)$$

The motor constant

In permanent-magnet d.c. motors, the rotor flux remains constant at a given temperature provided that saturation does not occur in the magnetic circuit due to the reverse field generated on starting. It follows from this that the term

$$pZ\Phi/a$$

in eq. (1) and (2) has a constant value at any given temperature and can, thus, be regarded as the motor constant

$$C_m = pZ\Phi/a. \quad (7)$$

Then, eq. (1) reduces to

$$M_{gn} = C_m I_n/(2\pi) \quad (8)$$

and eq. (2) reduces to

$$E_c = nC_m. \quad (9)$$

Mechanical efficiency

Torque M_n available at the motor shaft is smaller than the generated torque M_{gn} due to mechanical losses. Taking the mechanical efficiency of the motor as $\eta_{m(n)}$

$$M_n = M_{gn}\eta_{m(n)}. \quad (10)$$

Together with eq. (8) this yields

$$M_n = \eta_{m(n)} I_n C_m/(2\pi). \quad (11)$$

The mechanical efficiency is limited by frictional losses in bearings and brushes and by viscous losses due to the air, together with hysteresis and eddy-current losses. All these depend wholly or partly on the rate of rotation. Thus, when the motor is at rest, the mechanical efficiency is unity and

$$M_0 = I_0 C_m/(2\pi). \quad (12)$$

Dividing eq. (12) by eq. (11) yields

$$M_n/M_0 = \eta_{m(n)} I_n/I_0. \quad (13)$$

Rearrangement of eq. (6) gives

$$I_n = \frac{E - E_b - E_c}{R_a + R_e}$$

and, since at $n = 0$, $E_c = 0$,

$$I_0 = \frac{E - E_b}{R_a + R_e} \quad (14)$$

we can write

$$\frac{M_n}{M_0} = \eta_{m(n)} \frac{E - E_b - E_c}{E - E_b} \quad (15)$$

If we define a torque ratio C such that

$$C = M_n/M_0 \quad (16)$$

and substitute eq. (9) in eq. (15) we find

$$C_m = \frac{(\eta_{m(n)} - C)(E - E_b)}{\eta_{m(n)}\, n} \quad (17)$$

Mechanical losses in a motor are determined by measurement. For calculating C_m, a value of $\eta_{m(n)}$ is taken based on experience, allowance being made for hysteresis and eddy-current losses, especially at high speeds. These iron losses can be calculated approximately using empirical formulae together with a quality figure Q_i for the iron rotor laminations quoted by the supplier.

When designing a motor starting from the calculated value of C_m it is extremely important that the value of $\eta_{m(n)}$ used should be as accurate as possible.

Since the power delivered by the motor at speed n is

$$P_n = 2\pi n M_n \quad (18)$$

and the power generated by the motor is

$$P_{gn} = 2\pi n M_{gn} \quad (19)$$

it is evident that

$$P_n = \eta_{m(n)} P_{gn}. \quad (20)$$

Electrical efficiency

At any given speed, the mechanical power generated by a motor is less than the electrical power

$$P = I_n E \tag{21}$$

consumed by the motor due to electrical losses. Where the electrical efficiency is $\eta_{e(n)}$,

$$P_{gn} = \eta_{e(n)} P. \tag{22}$$

Overall efficiency

It follows from eq. (20) and (22) that

$$P_n = \eta_{m(n)} \eta_{e(n)} P. \tag{23}$$

Thus, the overall efficiency of a motor is

$$\eta_{(n)} = \eta_{m(n)} \eta_{e(n)} \tag{24}$$

and

$$P_n = \eta_{(n)} P. \tag{25}$$

Electrical losses are due to voltage drops and resistances in the electrical circuit of the motor, as shown in Fig.2. The losses in the circuit external to the motor are $I_n^2 R_e$ and those inside the motor are $I_n E_b + I_n^2 R_a$. From eq. (22).

$$\eta_{e(n)} = P_{gn}/P_n$$

$$= \frac{P - (I_n^2 R_e + I_n E_b + I_n^2 R_a)}{P}$$

$$= \frac{I_n E - I_n (I_n R_e + E_b + I_n R_a)}{I_n E}$$

$$= \frac{E - E_b - I_n (R_e + R_a)}{E}$$

$$= E_c/E. \tag{26}$$

Which, together with eq. (9) yields

$$\eta_{e(n)} = n C_m / E \tag{27}$$

and this, with eq. (17) yields

$$\eta_{e(n)} = (\eta_{m(n)} - C)(E - E_b)/(\eta_{m(n)} E). \tag{28}$$

Equations (24) and (28) together yield the overall efficiency

$$\eta_{(n)} = (\eta_{m(n)} - C)(E - E_b)/E. \tag{29}$$

Since C, E, and E_b generally form part of the motor specification, the overall efficiency is thus determined by the mechanical efficiency $\eta_{m(n)}$.

Heat dissipation

The power lost in the motor is converted into heat which must be transferred to the surroundings.

Rotor dissipation $I_n^2 R_a$ takes place mainly through the air flow on the rotor surface $\pi D_a \ell_a$ (heat transfer at the ends of the rotor is neglected). The rotor dissipation per unit area is

$$P_{DR} = \frac{I_n^2 R_a}{\pi D_a \ell_a}. \tag{30}$$

It is evident that, to keep the motor temperature within safe limits, there will be a maximum allowable value for P_{DR}. This value depends on the construction of the motor and the provision made for cooling: open or closed construction, fan or no fan. It follows from eq. (30) that the value permissible for P_{DR} could determine the minimum rotor volume.

Reverse field

The total motor flux

$$\Phi_{tot} = p\Phi \tag{31}$$

is supplied by the stator magnets. These must be capable of withstanding the reverse field H_{pn} developed by the rotor without irreversible demagnetisation. This reverse field is maximum when the motor is stalled, that is, when current is applied but the rotor is not turning. The reverse magnetomotive force acting on the magnet poles due to the stall current is, from eq. (3)

$$F = H_{p0}\, d \qquad (\mu_r = 1) \tag{32}$$

$$= \frac{I_0 \alpha' Z}{8\pi a q}. \tag{33}$$

Temperature effects

The characteristics of a permanent-magnet motor vary with temperature due to

- the temperature dependence of the stator magnets
- the temperature dependence of the resistances
- the temperature dependence of the mechanical losses and, thus, $\eta_{m(n)}$.

Thus, a motor rated at a given temperature (usually 20 °C) will have different characteristics at another temperature. The change in characteristics depends on the change in the properties of the components.

Since the properties of the stator magnets vary with temperature, the total flux in the motor also varies with temperature. If the total flux at 20 °C is $\Phi_{tot(20)}$ then

$$\Phi_{tot(t)} = \Phi_{tot(20)} \left\{ 1 + \frac{\tau_{Br}(t - 20)}{100} \right\}. \qquad (34)$$

Since the motor constant defined in eq. (7) is

$$C_m = \frac{pZ\Phi}{a}$$

it follows from eq. (34) that

$$C_{m(t)} = C_{m(20)} \left\{ 1 + \frac{\tau_{Br}\,(t - 20)}{100} \right\} \qquad (35)$$

The effect of changes in resistances with temperature on the stall current is given by

$$I_{0(t)} = I_{0(20)} \frac{R_{a(20)} + R_{c(20)} + R_{i(20)}}{R_{a(t)} + R_{c(t)} + R_{i(t)}} \qquad (36)$$

and, therefore,

$$F_{(t)} = F_{(20)} \frac{R_{a(20)} + R_{c(20)} + R_{i(20)}}{R_{a(t)} + R_{c(t)} + R_{i(t)}} \qquad (37)$$

Furthermore, it follows from eq. (35) and (36) that

$$M_{0(t)} = M_{0(20)} \frac{R_{a(20)} + R_{c(20)} + R_{i(20)}}{R_{a(t)} + R_{c(t)} + R_{i(t)}} \times$$

$$\times \left\{ 1 + \frac{\tau_{Br}\,(t - 20)}{100} \right\} \qquad (38)$$

Resistances R_a, R_c and R_i do not neccessarily have the same temperature dependence. Resistances R_a and R_c, where R_c is due to wiring, will generally be of copper and their temperature dependence can be determined using the temperature coefficient for copper.

The temperature behaviour of resistance R_i depends on the type of power supply used. For example, the resistance of a battery increases as its temperature falls. Since, however, the resistance of the copper leads decreases with decreasing temperature, the sign of the temperature coefficient of M_0 will depend on which effect predominates.

It follows from eq. (11) that

$$M_{n(t)} = \frac{1}{2\pi}\, \eta_{m(n)(t)}\, I_{n(t)}\, C_{m(t)} \qquad (39)$$

where, from eq. (4) and (9)

$$I_{n(t)} = \frac{E - E_b - nC_{m(t)}}{R_{a(t)} + R_{c(t)} + R_{i(t)}} \qquad (40)$$

Equation (39) shows that the temperature dependence of $\eta_{m(n)}$ must be known before that of M_n can be determined. However, the effect of temperature on $\eta_{m(n)}$ depends, at least in part, on motor design and can usually be found only by experiment.

THE MAGNETIC CIRCUIT

Basic arrangement

Figure 3 shows the essential features of the magnetic circuit of a permanent-magnet motor. The rotor is treated as a solid iron cylinder without slots whose axial length is equal to that of the stator magnets.

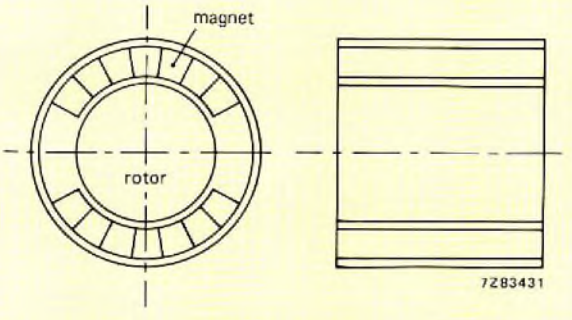


Fig.3 Simplified magnetic circuit of the permanent-magnet motor of Fig.1

The anisotropic, ceramic magnet material used for the stator magnets has a demagnetisation curve in which the portion above the knee approximates a straight line, Fig.4. Operation on this part of the curve is reversible; its slope can be considered to have constant permeability

$$\mu_{rec} = \frac{\mu}{\mu_0} = \frac{\tan\beta}{\mu_0} = \frac{B_r - B_p}{\mu_0 H_p} \qquad (41)$$

where B_p and H_p are the coordinates of any working point P on the straight portion above the knee. Rearrangement of eq. (41) gives

$$H_p = (B_r - B_p)/(\mu_0 \mu_{rec}). \qquad (42)$$

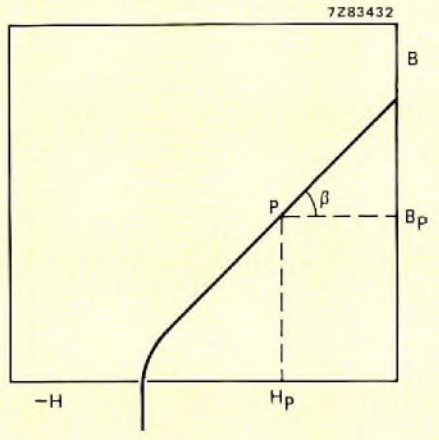


Fig.4 Characteristic demagnetisation curve of an anisotropic ceramic permanent-magnet showing the working point

Calculation of motor flux

Method

In the system of Fig.3, the stator magnets do not have a single working point; rather, there is a band of working points: each part of each magnet operates under slightly different conditions with a slightly different load line. Figure 5 shows the demagnetisation curve of Ferroxdure 380; shaded triangle $P_1 0 P_1$ defines the limits of the spread of load lines for the magnets of a typical motor. Point P ($\bar{B}_m$,$\bar{H}_m$,) is the mean working point which depends on the type of magnetic material, on the radial thickness of the magnets, and on the air gap between rotor and stator:

$$\bar{B}_m = B_r/(1 + \mu_{rec}\delta/d_s) \qquad (43)$$

and from eq. (42),

$$\bar{H}_m = (B_r - \bar{B}_m)/(\mu_0\mu_{rec}). \qquad (44)$$

Rearrangement of eq. (43) yields

$$\bar{B}_m = B_r d_s/(d_s + \mu_{rec}\delta) \qquad (45)$$

which, with eq, (44) gives

$$\bar{H}_m = \frac{B_r\mu_{rec}\delta}{\mu_0\mu_{rec}(d_s + \mu_{rec}\delta)} = \frac{B_r\delta}{\mu_0(d_s + \mu_{rec}\delta)} \qquad (46)$$

Since, for most motor designs, $0.05d_s < \delta < 0.15d_s$, and for anisotropic grades of Ferroxdure ceramics, $\mu_{rec} \approx 1.07$, the value of μ_{rec} in the term

$$1/(d_s + \mu_{rec}\delta)$$

may be taken as unity with an error of less than 1% (but its dimension must not be forgotten). Making this assumption, eq. (45) becomes

$$\bar{B}_m = d_s B_r/d \qquad (47)$$

and eq. (46)

$$\bar{H}_m = \delta B_r/\mu_0 d \qquad (48)$$

within 1% for the magnetic circuit of Fig.3. The total flux supplied by the stator magnets should then be

$$\Phi'_{tot} = \bar{B}_m A_s p = B_r A_s p d_s/d \qquad (49)$$

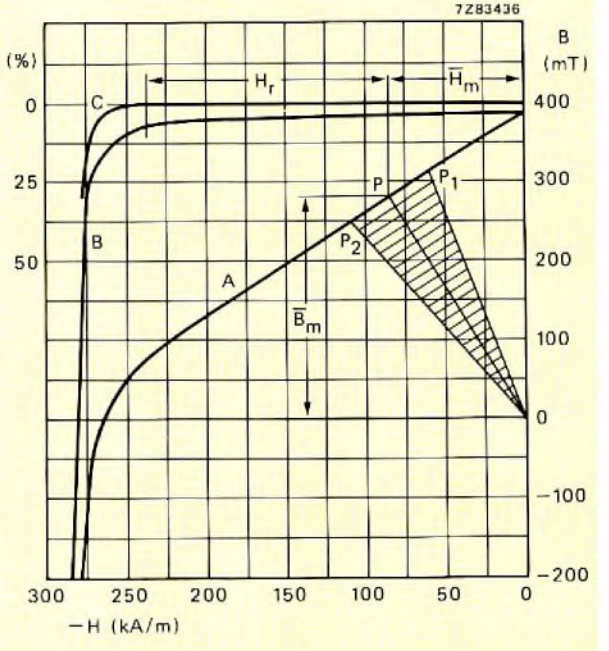


Fig.5 Curve A is the induction and curve B the intrinsic demagnetisation characteristic of Ferroxdure FXD 380 at 20°C. Curve C is the percentage demagnetisation as a function of the applied reverse field. The maximum reverse field that can be tolerated by magnets of this material is H_r. Thus, a mean working point P should be chosen such that $H_r + \bar{H}_m = 0.83H_{cJ}$ ($\gamma_0 = 0.83$) in order that permanent demagnetisation cannot occur

Correction factors

Measurement generally reveals that the flux through the rotor of a given design of permanent-magnet motor is less than that given by eq. (49) by a factor

$$f = \Phi_{tot}/\Phi'_{tot}$$

or, with eq. (49)

$$\Phi_{tot} = fB_r A_s p d_s/d. \qquad (50)$$

There are, in fact, two main causes of the shortfall in flux; thus,

$$f = f_1 f_2. \qquad (51)$$

Correction factor f_1 allows for the fact that the rotor of a permanent-magnet motor is not a solid cylinder but is fabricated from slotted laminations. Its value for most rotor designs has been found to lie between 0.9 and 0.95. This value also allows for losses due to stray flux.

Correction factor f_2 is required for motor designs in which the axial length of the stator magnets is more than about 1.15 times that of the rotor. Values of f_2 have been determined and are given in Ref.2.

Volume of magnet material

The total flux in permanent-magnets motors is supplied by a quantity of permanent-magnet material of total volume

$$\begin{aligned} V_f &= 2p\ell_s\alpha\pi(D_{os}^2 - D_{is}^2)/8\pi \\ &= p\ell_s\alpha(D_{os} - D_{is})(D_{os} + D_{is})/4 \\ &= p\ell_s\alpha d_s(D_{is} + d_s) \\ &= p\ell_s\alpha d_s D_{is}(1 + d_s/D_{is}). \end{aligned} \qquad (52)$$

Since

$$A_s = \alpha D_{is}\ell_s/2 \qquad (53)$$

then

$$V_f = 2pd_s A_s(1 + d_s/D_{is}). \qquad (54)$$

Substituting eq. (54) in eq. (50) yields

$$\Phi_{tot} = \frac{fB_r V_f}{2d(1 + d_s/D_{is})} \qquad (55)$$

which, for the total flux as a function of temperature, becomes

$$\Phi_{tot(t)} = \frac{fB_{r(t)} V_f}{2d(1 + d_s/D_{is})} \qquad (56)$$

neglecting the thermal expansion of the magnet material.

Demagnetising field

The starting current of a permanent-magnet motor generates a m.m.f. which, in turn, gives rise to a reverse field across the stator magnets of maximum value

$$H_{po} = F/d. \qquad (57)$$

To prevent permanent demagnetisation of the magnets, this field should not exceed the permissible value of H_r for the grade of magnet material used (Fig.5). That is,

$$H_r = \gamma_0 H_{cJ} - H'_m \qquad (58)$$

where $\gamma_0 H_{cJ}$ is the range of demagnetising field over which the operation of the material remains reversible. The value of γ_0 depends on the material: most grades of Ferroxdure have a γ_0 value of about 0.83 (Ref.3).

The value of H'_m to be used in eq. (58) must be considered carefully; it is found in practice that the most appropriate value is, in fact, that calculated with eq. (48). Thus

$$H_r = \gamma_0 H_{cJ} - \frac{\delta B_r}{\mu_0 d}. \qquad (59)$$

The reverse field H_a due to the rotor must not be greater than this value of H_r, or

$$F \leqslant d\left(\gamma_0 H_{cJ} - \frac{\delta B_r}{\mu_0 d}\right). \qquad (60)$$

Moreover, it is essential to ensure that permanent demagnetisation cannot occur over the whole operating-temperature range of the motor:

$$F_{(t)} \leqslant d\left(\gamma_0 H_{cJ(t)} - \frac{\delta B_{R(t)}}{\mu_0 d}\right). \qquad (61)$$

Temperature coefficients of the magnet material

The effect of temperature on the stator magnets is given in terms of the temperature coefficients of B_r and H_{cJ}.

For Ferroxdure anisotropic ceramic materials, these are

$$\tau_{Br} = -0.2\%/^{\circ}C \qquad (62)$$

$$\tau_{HcJ} \approx [0.19 + 0.17B_r/(\mu_0 H_{cJ})] \quad \%/^{\circ}C \qquad (63)$$

(Ref.4). These figures should be used with eq.(61) to check that the stator magnets cannot permanently be demagnetised over the operating temperature range of the motor.

Figure 6 shows the effect of temperature on the grades of Ferroxdure usually used in permanent-magnet motors. The maximum reverse m.m.f. that can be tolerated by these materials is plotted as a function of d in Fig.7.

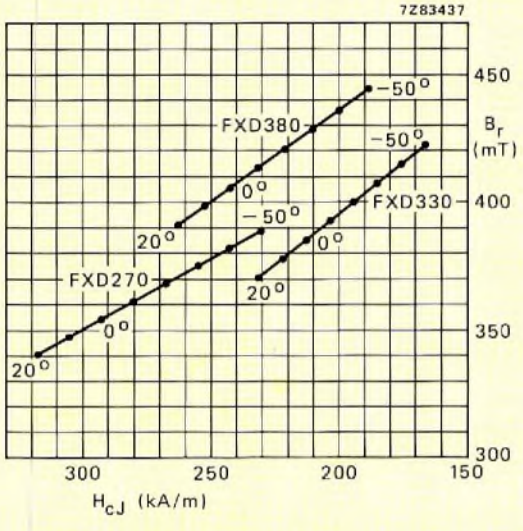


Fig.6 Combinations of B_r and H_{cJ} for a number of grades of anisotropic Ferroxdure as a function of temperature

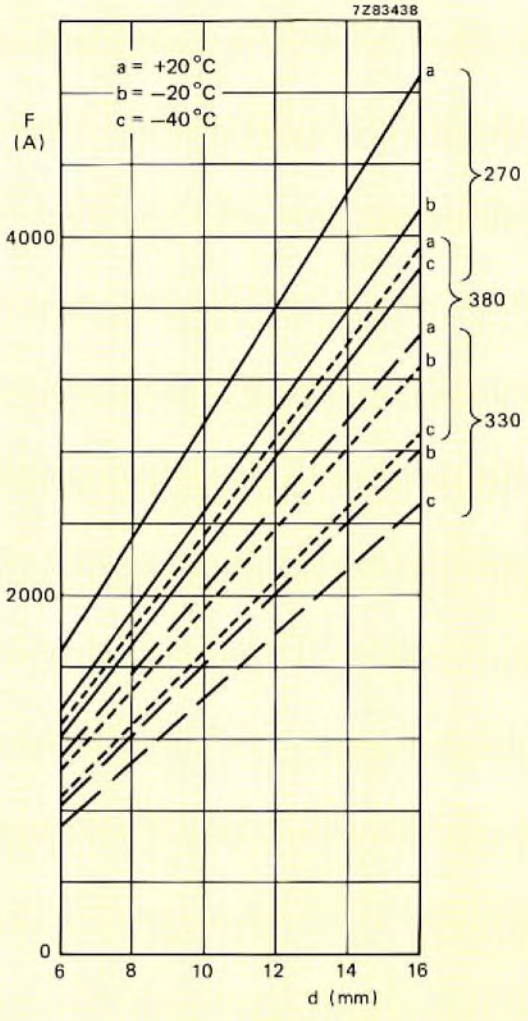


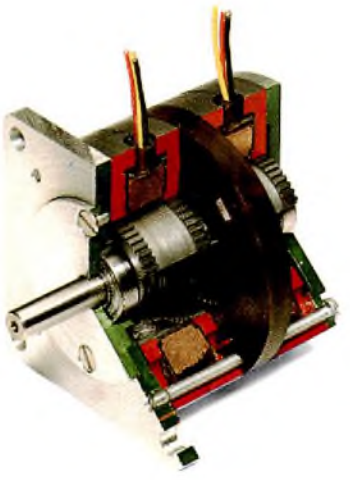
Fig.7 The maximum value of applied m.m.f., F, as a function of dimension d for several grades of Ferroxdure at various temperatures

Part 2 of this article, to be published in E.C.&A. Vol 3 No. 2, will consider the application of the foregoing analysis to specific motor design parameters and magnetic materials.

New hybrid stepper motor design

B. H. A. GODDIJN

Technological progress in industry over the last decade, especially the application of digital electronics, has produced substantial growth in the demand for stepping motors. As well as increased demand from the computer industry, other industries, formerly unrelated to stepping motor techniques, have found new ways to improve their products with the aid of stepping motors. Nevertheless, stepping motor development has not kept pace with the technological changes that have increased demand, but has instead been concentrated on reducing cost.



Cutaway hybrid stepping motor (size 23) showing the features of the new design. The motor has ring coils and a ceramic ring permanent-magnet located in the stator

There is now an urgent need for stepping motors in a wide range of small step angles, and for smaller motors. The design described here uses a new concept to meet today's requirements. Fundamentally different to the three types of motor on the market (permanent magnet, variable reluctance and hybrid), the new design is free from their restrictions on step angle. The components of the motor are simple and few; manufacture can be highly automated.

In short, the advantages of the new motor concept are:

- a wide range of step angle and motor size
- holding torque better than that of existing hybrid motors
- simple construction; motor is easy to mass produce and uses an inexpensive grade of magnet.

EXISTING TYPES OF STEPPING MOTOR

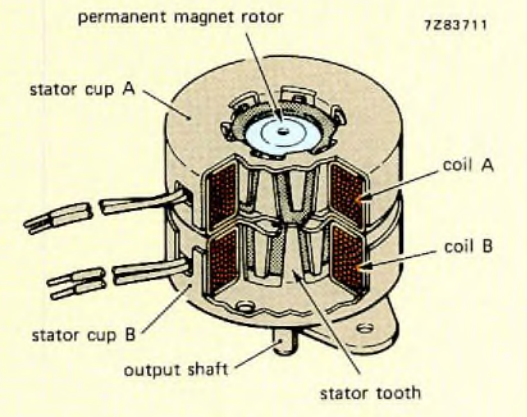
Many variations are available, but there are only three basic types of stepping motor. A brief look at their construction and operation reveals certain inherent limitations.

True permanent magnet stepping motor

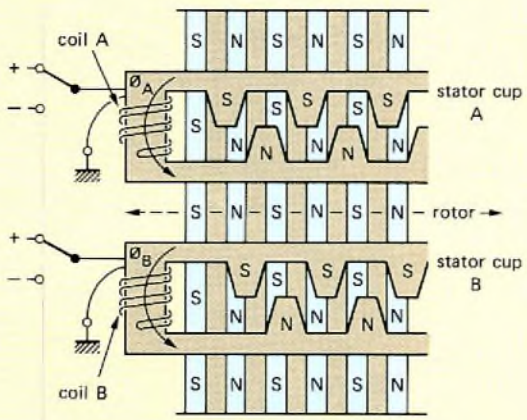
The distinguishing feature of this type of motor is the use of a cylindrical, ceramic, permanent magnet in the rotor assembly. This magnet is radially magnetised with several poles; the stator has an equal number of wound poles.

Figure 1 shows an industrial type. The motor has sheet metal stator cups with punched-out teeth surrounding a radially polarised permanent magnet rotor. Centre-tapped bifilar-wound ring coils determine the polarity of the stator teeth. Changing the direction of the current through the coils produces a rotating magnetic field which exerts a force on and advances the rotor.

This design is simple and inexpensive. Its limitation is the number of poles that can be magnetised on the circumference of the rotor. Because the number of poles determines the step angle, only large angles are feasible. Enlarging the magnet to accommodate more poles is unpractical because its effect on moment of inertia (which for a cylinder increases as the fourth power of the diameter) reduces starting torque below acceptable levels.



(a)



STEP	COIL A	COIL B
1	+	+
2	+	−
3	−	−
4	−	+
1	+	+

clockwise rotation

counter-clockwise rotation

7Z83712

(b)

Fig.1 Permanent magnet stepping motor (2-phase). (a) Construction. (b) Operating principle. The coils are energised in a 4-step switching sequence, see Table. Interaction between rotor and stator poles makes the rotor move ¼ pole pitch at every step in the sequence

Variable reluctance stepping motor

The variable reluctance motor has no permanent magnet. It uses only coil excitation; reluctance forces move the rotor. A practical motor has a single or multi-stack laminated stator which has several wound poles. Longitudinal slots in the stator accommodate the windings. A soft iron toothed rotor is used; this is cylindrical in the single-stack motor and consists of several discs in the multi-stack motor, see Fig.2.

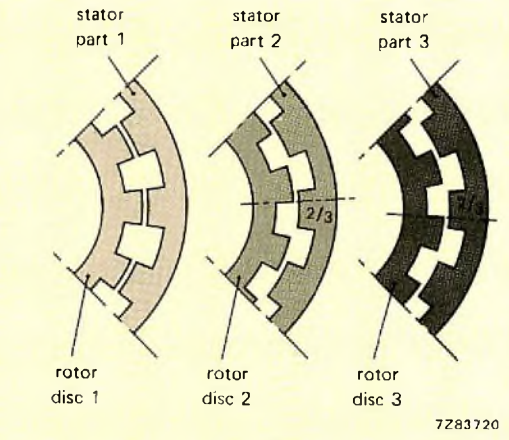
The multi-stack motor has the same number of stator parts as rotor discs (usually three or five); all have the same number of teeth. Each stator part corresponds to one phase. The teeth of the stator parts are in line, those of the rotor discs offset from each other by a distance depending upon the number of phases (thus, one third of a tooth pitch for three phases).

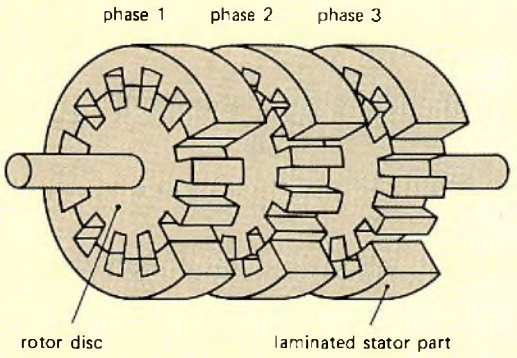
The single-stack stator has separate windings for each phase. The number of rotor teeth is less than the number of stator teeth, so that only one pair of stator poles and a corresponding pair of rotor poles can be aligned per phase.

Phases are energised in sequence – radially for single-stack motors, axially for multi-stack motors. The rotor moves to the position of least reluctance, for each set of energised windings.

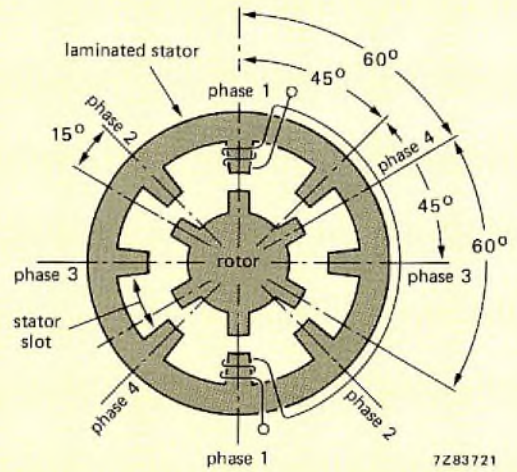
Because the rotor does not incorporate a permanent magnet, its diameter can be small, giving low moment of inertia. When lightly loaded, these motors have very high slew rates.

The variable reluctance motor also has drawbacks. Only a limited range of step angles is possible with the single-stack type, because the wound stator construction limits the number of poles that can be arranged around the stator circumference. Multi-stack motors suffer from a low torque to stator volume ratio compared with hybrid motors and require sophisticated drive circuits because they have almost no inherent damping. Neither type has detent torque when de-energised, which is often a disadvantage.





(a)



(b)

Fig.2 Variable reluctance stepping motors. (a) Industrial multi-stack motor (3-phase). Position shown is with phase 1 energised. (b) Industrial single-stack motor (4-phase). The motor shown has four pairs of stator poles at 45° intervals and three pairs of rotor poles at 60° intervals. This gives a 15° step angle. Position shown is with phase 1 energised

Conventional hybrid stepping motor

The hybrid motor produces torque by reluctance forces, like the variable reluctance motor. What differentiates the two is the type of excitation used. In the variable reluctance motor, excitation is solely by means of a coil; in the hybrid motor, excitation is by permanent magnet in conjunction with a coil.

Figure 3 shows the basic design which gives a step angle of 90°. To obtain smaller step angles, the number of stator and rotor poles is increased (Fig.4). However, the range of step angles is limited by the number of poles which can be arranged around the stator and the number of teeth on each.

There are ways around the step angle problem (e.g. 5 or 8-phase or multiple stator motors), but they bring new complications and performance usually suffers.

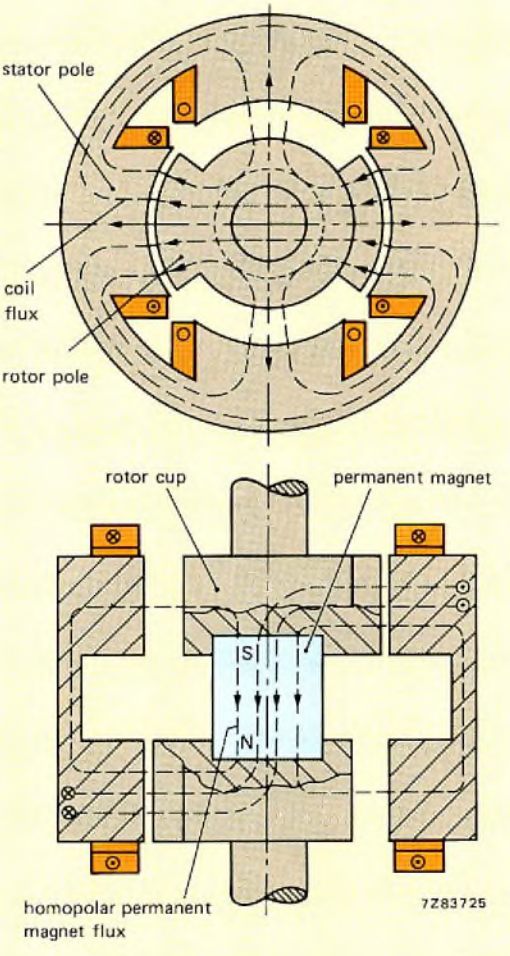


Fig.3 Conventional hybrid stepping motor. The motor produces torque by means of reluctance forces. It uses permanent magnet excitation in conjunction with coil excitation. Energising two coils increases the flux in two stator poles which causes the rotor poles to align under the energised stator poles. By energising both pairs of coils alternately and in both directions, the rotor will rotate in steps of 90°

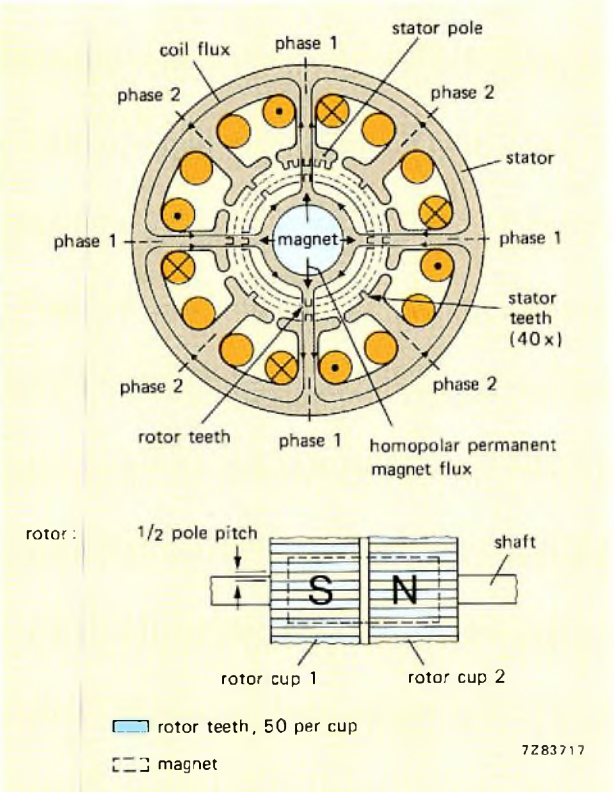


Fig.4 Industrial hybrid stepping motor with eight stator poles for 1.8° step angle. The number of teeth that can be accommodated per stator pole and the need for two pole pairs per phase limit the range of step angles possible

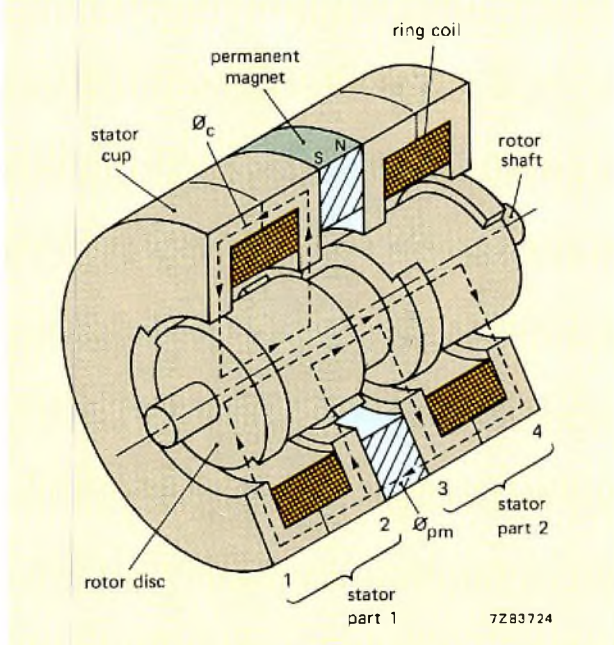


Fig.5 New ring-coil hybrid stepping motor, showing the paths of the permanent-magnet flux ϕ_{pm} and coil flux ϕ_c for one coil excitation mode. For this mode ϕ_c adds to ϕ_{pm} in disc 1 and subtracts from it in disc 2. Discs and cups 1 to 4 are here shown with only one tooth for clarity

NEW HYBRID STEPPING MOTOR

Construction

Figure 5 shows the construction of the motor, which has been made simple by using ring coils for the stator windings. The stator is in two parts joined by a permanent magnet (a thin ring of Ferroxdure 370). Each stator part consists of two magnetically conducting cups with teeth, and a ring coil. One cup corresponds to one pole in the conventional hybrid motor. The rotor consists of a shaft on which four toothed discs are mounted. Rotor discs are solid iron; stator cups sintered iron.

Each stator part represents one phase, and the motor uses only *one pole pair per phase*. Discs and cups have the same number of teeth uniformly distributed around their circumferences. The teeth of the stator cups are in line; those of the rotor discs offset in a pattern set by the energising sequence of the ring coils. When the teeth of disc 1 are in line with the teeth of the stator cups, the teeth of discs 2, 3 and 4 are respectively 180, 90 and 270 electrical degrees offset from the stator teeth, see Fig.5.

Operation

Completely different to other hybrid stepping motor designs is the positioning of the magnet in the stator package; therefore, the flux paths are also different.

Referring to Fig.5, the permanent magnet passes a flux from one stator part to the other, via the rotor. Depending on the initial rotor position, the flux through disc 1 will be larger than that through disc 2, or vice versa. However, the sum of the fluxes through the two discs remains constant. The same holds for discs 3 and 4. Because the sum of the fluxes is independent of rotor position, the rotor has no preferred position.

When a coil is excited, a flux flows from one stator cup through two rotor discs to the other cup of the same stator part. The permanent magnet acts as a large air gap to this flux, thus the two stator parts are almost magnetically separate. The flux due to excitation of the coil increases the flux due to the permanent magnet in one disc and cup, and decreases it in the other. The rotor moves to align the teeth of the rotor disc where the flux was increased with the teeth of the stator cups. When the two coils are excited alternately and in both directions, thereby increasing the flux in each disc in turn, the rotor revolves in steps of a quarter of a tooth pitch.

Freedom of step angle

The main weakness of the conventional hybrid motor is the limited choice of step angle imposed by the stator design. Thus, manufacturers are unable to offer many desirable step angles.

A popular number of characters on a daisy wheel printer is 96. This requires a 3.75° step angle for single

stepping, or a 1.875° step angle for double stepping. There is no feasible solution using the conventional hybrid motor concept. Step angles of 3.75°, 1.875° and many others pose no problem with the new design, because the number of teeth per stator cup, which determines step angle, can be increased or decreased one tooth at a time, resulting in only four steps more or four steps less per revolution. This gives tremendous scope in step angle, see Table 1.

Freedom of motor size

The rotor of the new motor has no magnet inside. Thus, the rotor diameter can be altered with no effect on the field strength in the air gap. Very small rotors can be used to reduce rotor inertia for special applications.

In the conventional hybrid motor the magnet is in the rotor. High quality magnets (Alnico, Ticonal) are needed because the available space in the rotor is limited. Miniaturisation below motor size 23 is not feasible unless stronger, even more expensive, rare-earth magnets are used to obtain sufficient flux in the air gap.

Performance

The first motors we have made using the new design are size 23 with a step angle of 1.8°. They are direct replacements for many existing 1.8° hybrid stepping motors.

Figure 6 shows the pull-out torque as a function of stepping rate of the new motor and Table 2 gives the brief specification.

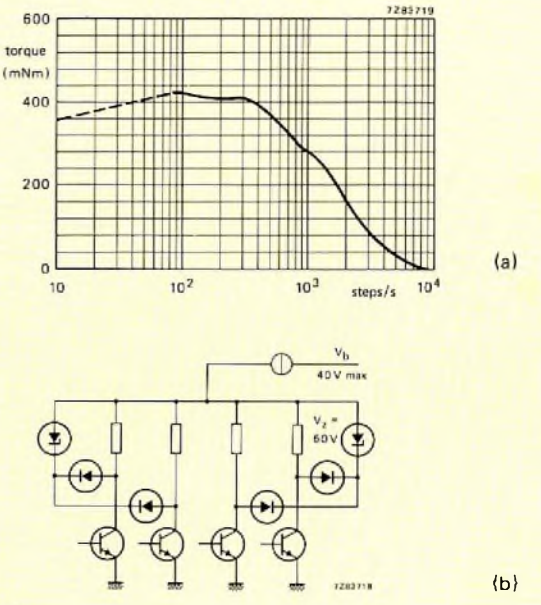


Fig.6 (a) Pull-out torque as a function of stepping rate for the size 23 motor with 1.8° step angle with unipolar constant-current drive (b)

TABLE 1
Some of the step angles possible with the new hybrid motor design

number of teeth per stator cup	steps/rev.	step angle (degrees)
64	256	1.41*
52	208	1.73*
51	204	1.76*
50	200	1.8
49	196	1.84*
48	192	1.875
32	128	2.81*
24	96	3.75
2	8	45
1	4	90

* approximate value.

TABLE 2
Brief specification of the size 23 stepping motor with 1.8° step angle

Power consumption (motor only)	8.7 W
Number of phases	4
Step angle	1.8°
Step angle tolerance (non cumulative)	±5%
Max. working torque	380 mNm
Holding torque	500 mNm
Max. pull-out rate	see Fig.6
Resistance per coil (at 20 °C)	4.3 Ω
Inductance per coil	14 mH
Current per coil	1 A
Insulation according to CEE 10	class III
Insulation resistance at 500 V d.c.	>2 MΩ
Rotor inertia	100 gcm²
Max. radial force on bearings	50 N
Max. axial force on bearings	20 N
Mass	0.6 Kg

Measured with unipolar constant-current drive, $V_{b\,max}$ = 40 V, V_Z = 60 V.

All values are provisional.

In principle, the new motor has a very high static torque to volume ratio compared with conventional hybrid motors. This is due to the use of ring coils and a single pole pair per phase. The practical motor compromises static torque with dynamic performance suitable for a variety of digital servo functions.

Figures of merit

As we have seen, the new motor uses only one pole pair compared with the two pole pairs of the conventional hybrid motor. In addition, permanent magnet excitation is completely different due to the position of the magnet in the stator.

To study the effect of the number of pole pairs and the permanent magnet excitation on the static and dynamic performance of an idealised hybrid motor, we shall introduce several figures of merit (q). The first is: $q_1 = T/V$ where T is the motor torque (hybrid torque) and V the motor volume. The ratio of torque to motor volume is the main criterion of static performance.

Note, motor torque consists of hybrid torque, detent torque and reluctance torque. Here, we assume that the hybrid torque of a motor is many times larger than the detent and reluctance torque.

Because the motor must not be thermally overloaded when attaining a large torque, we introduce $q_2 = T/I^2R$ where I is the excitation current and R the resistance per phase. The criteria q_1 and q_2 are closely related. With increasing copper volume q_1 decreases and q_2 increases.

The dynamic performance of a motor, shown in pull-out and pull-in curves and the single-step response, is determined by the electrical parameters: self-inductance, resistance and rotational e.m.f., and by the mechanical parameters: moment of inertia of the rotor and friction. The effect of friction on performance is negligible.

The coils of a motor convert electrical energy, supplied by the motor drive circuit, into magnetic energy. A certain amount of electrical energy has to be supplied simply to maintain the magnetic field in the motor. The smaller this energy is, the more is available to produce torque. Thus, $q_3 = T/I^2L$, where L is the self-inductance of the motor, indicates the magnetic energy necessary to produce the torque.

The final figure of merit $q_4 = T/J$ shows the effect of the moment of inertia of the rotor (J) on the dynamic performance.

In assessing the effect upon performance of the number of pole pairs and the permanent magnet excitation, we assume that the rotor geometry is unchanged.

Effect of the number of pole pairs

A hybrid stepping motor produces maximum torque when the magnetic potential difference across the airgap due to coil excitation is equal to that due to the permanent magnet. Each pole pair has the same number of ampere-turns in order to produce the desired magnetic potential across the airgap. Therefore, for a fixed copper volume, the copper volume per pole pair is inversely proportional to the number of pole pairs, p, and the current density is proportional to p.

If a motor is designed so that the copper length is minimised, then the copper length per pole pair is inversely proportional to $p^{1/2}$ (since the pole surface is inversely proportional to p).

Because the copper volume per pole pair is inversely proportional to p and copper length per pole pair is inversely proportional to $p^{1/2}$, the copper cross-section per pole pair is proportional to $p^{1/2}$. Therefore, the resistance per pole pair is independent of the number of pole pairs. Hence, the I^2R losses of the stator coils are directly proportional to the number of pole pairs. If, as is the case in a conventional hybrid stepper motor with its wound stator, the copper length consists of the coil sides and the coil overhangs, the losses will rise even faster with increasing p. When the coil overhangs are short compared with the coil sides, the losses in the stator coils are proportional to p^2, thus q_2 is very dependent on the number of pole pairs, and $q_2 \sim p^{-a}$, where a is between 1 and 2.

Enlarging the copper volume reduces the I^2R losses and increases q_2. It does not affect the magnetic energy produced by the phase coils, the torque or moment of inertia. Thus, q_3 and q_4 are independent of the number of pole pairs.

Effect of permanent magnet excitation

The magnetic potential difference across the air gap, U_g, is equal to the sum of the contributions from the permanent magnet and from the coil excitation. U_g is limited by the saturation of the iron rotor and stator. If we assume that the iron has an infinitely large permeability as long as the iron does not saturate (see Fig.7), then:

$$U_{g\,max} = B_{sat}\, g/\mu_o$$

where

B_{sat} is the saturation value of the magnetic flux density in the iron,
g is the airgap length,
μ_o is the permeability of air.

If the motor is excited so that the iron just fails to saturate

$$U_{g\,max} = \alpha_1 U_{pm} + \alpha_2 F_c$$

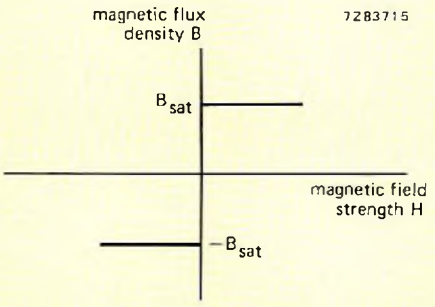


Fig.7 Idealised B-H curve of the rotor and stator

where

U_{pm} is the magnetic potential difference of the permanent magnet outside the magnet,
F_c is the m.m.f. of the excitation coil,
α_1, α_2 are dimensionless constants accounting for design variables.

The torque expressed in terms of the coil m.m.f. is

$$T = \frac{\alpha}{\alpha_1} F_c (U_{g\,max} - \alpha_2 F_c) \frac{dP_\lambda}{d\theta}$$

where

P_λ is the permeance of one tooth pitch,
θ is the rotor angle,
α is a dimensionless constant accounting for design variables.

In the new motor, the volume of the motor depends only slightly on that of the permanent magnet. In the conventional hybrid motor, the permanent magnet is located in the rotor, therefore the stator volume of the motor is unchanged when a different size of magnet is used. Thus, q_1 is almost completely determined by the variation of torque:

$$q_1 \sim F_c(U_{g\,max} - \alpha_2 F_c).$$

For a constant copper volume and airgap geometry, the I^2R losses are approximately F_c^2. We can now express q_2 in terms of the permanent magnet and coil excitation:

$$q_2 \sim \frac{F_c (U_{g\,max} - \alpha_2 F_c)}{F_c^2} = \frac{U_{g\,max} - \alpha_2 F_c}{F_c}.$$

The energy necessary to maintain the magnetic field produced by coil excitation is also proportional to F_c^2, therefore:

$$q_3 \sim \frac{U_{g\,max} - \alpha_2 F_c}{F_c}.$$

The moment of inertia of the rotor only depends upon the size of the magnet if the magnet is located in the rotor. In any event, the contribution of the magnet to the moment of inertia is small, because the magnet is not at the periphery of the rotor. Therefore, figure of merit q_4 is almost identical to q_1.

Results

Figure 8 shows q_1, q_2 and q_3 as functions of m.m.f. of the excitation coil. The curves show that a small deviation of q_1 from its optimum gives a large variation of q_2 and q_3. It is possible to choose the copper volume so that q_1 increases as q_2 decreases, or vice versa. Increasing the permanent magnet excitation increases q_2 and q_3 sharply, but decreases q_1 only slightly. If in addition the copper volume is reduced, q_1 and q_2 are practically unchanged whereas q_3 increases sharply.

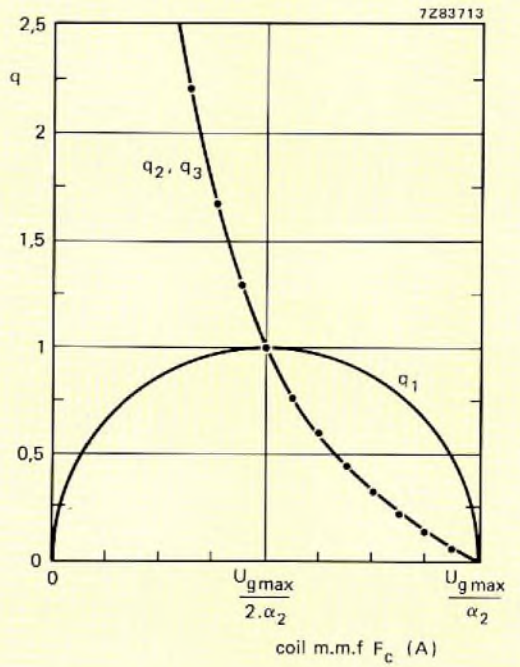


Fig.8 Figures of merit of a hybrid stepping motor as functions of coil excitation

REFERENCE

GODDIJN, B. H. A., 'Static performance of a hybrid stepping motor with ring coils', 1980 Ph.D. thesis, University of Technology, Eindhoven.

Serial I/O with the MAB8400 series microcomputers

A. P. M. MOELANDS

A microcomputer with a mask-programmed memory is a general purpose device with a dedicated function that is specified by the contents of its ROM. The increasing use of microcomputers in domestic and industrial apparatus, where much of the task is control rather than computation, has lead to the requirement for modification of some of the hardware functions of these devices.

The 8400 series* has been developed from the well-known 8048/8021 devices, to provide microcomputers with additional dedicated functions suited to control applications. Architecture and pin layout of the 8400 series are similar to the 8021 microcomputer, while the instruction set is based upon that of the 8048 microcomputer. The 8400 series comprises a range of functionally identical devices offering a variety of ROM and RAM capacities to suit the application.

Serial input/output

Use of serial data communication between devices greatly reduces the number of connections required, leading to simpler circuit layout and economies in connector size and printed circuit board area. One of the special functions of the 8400 series, the Serial Input/Output (SIO) interface has been designed to eliminate the heavy processing load imposed upon a normal microcomputer performing serial data transfer. The SIO interface can be seen in the block diagram of the 8400 in Fig. 1.

Whereas a normal microcomputer must regularly monitor the serial data bus for the presence of data, the 8400's SIO interface detects, receives and converts the serial data stream to parallel format without interrupting the execution of the current program. Only when the complete byte has been received is an interrupt sent to the microcomputer, which can then read the data byte in a single instruction. Likewise, for transmission, the SIO interface performs the parallel to serial conversion and subsequent serial output of the data while the microcomputer continues with execution of its programmed tasks.

The design of the 8400's SIO system allows any number of 8400 devices to be interconnected by the two-line serial bus. Furthermore, the ability of any two devices to communicate, without the slightest interruption of the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to messages prefixed with its own address or the 'general call' address. The address recognition procedure is performed by the interface hardware so that operation of the microcomputer need only be interrupted when a valid address has been received. This results in a significant saving of processing time and memory space compared with a conventional microcomputer employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcomputers, direct data transfer without addressing can be performed.

The 8400 serial input/output system also provides simple mechanisms for implementation of master/slave operation of devices, acknowledgement of data

* Detailed information on the MAB8400 series can be found in a separate Technical Publication.

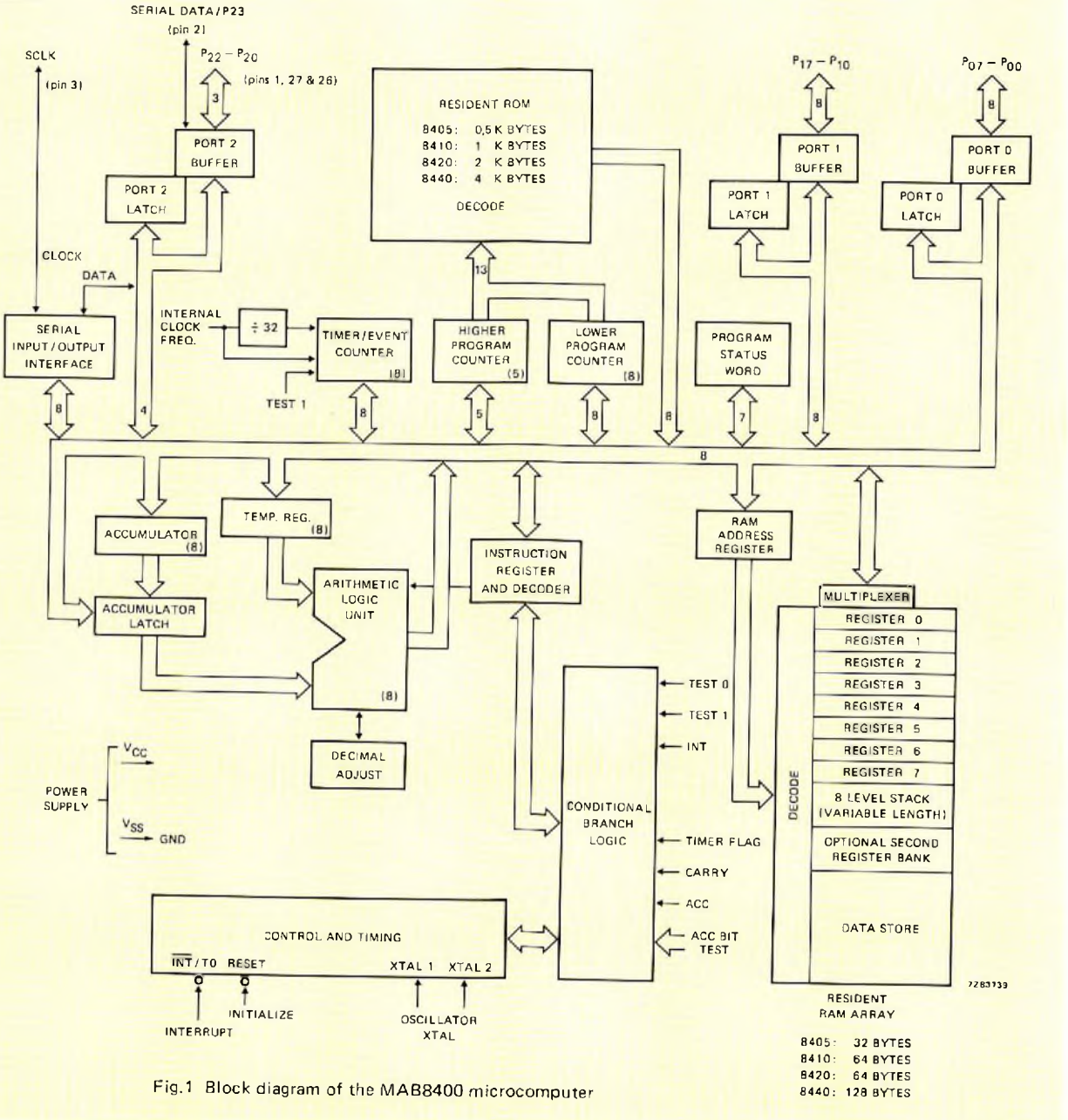


Fig.1 Block diagram of the MAB8400 microcomputer

reception and an asymmetrical clock signal for use with conventional microcomputer systems. When multimaster systems are used, an arbitration procedure is automatically invoked, thus preventing two or more devices from continuing simultaneous transmission.

Serial data bus

The 8400 serial interface has been designed to work with a serial bus consisting of two bi-directional lines: one for data signals and one for clock signals. A protocol has been defined to allow reliable and efficient operation of this bus:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is High. Changes in the data line while the clock line is High will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: both data and clock lines remain High.

Start data transfer: a change in the state of the data line, from High to Low, while the clock line is High defines the *start* condition.

Stop data transfer: a change in the state of the data

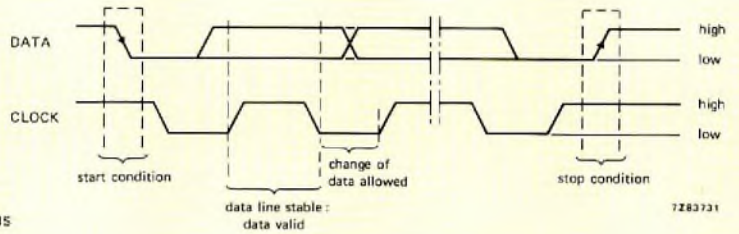


Fig.2 Data transfer sequence on the serial bus

line, from Low to High, while the clock line is High, defines the *stop* condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Figure 2 illustrates the sequence of events involved in data transfer on the serial bus. Each data transfer is initiated with a start condition and terminated with a stop condition; the number of data bits transferred between the start and stop conditions is not limited.

Serial I/O interface

A block diagram of the 8400 serial I/O interface is shown in Fig. 3. The clock line of the serial bus has the exclusive use of pin 3, while the data line shares pin 2 with I/O signal P23 of port 2. Consequently, only three I/O lines are available for port 2 when the SIO interface is enabled.

Communication between the microcomputer and the interface takes place via the internal bus of the microcomputer and the Serial Interrupt Request line. Four registers are used to store data and information controlling the operation of the interface:

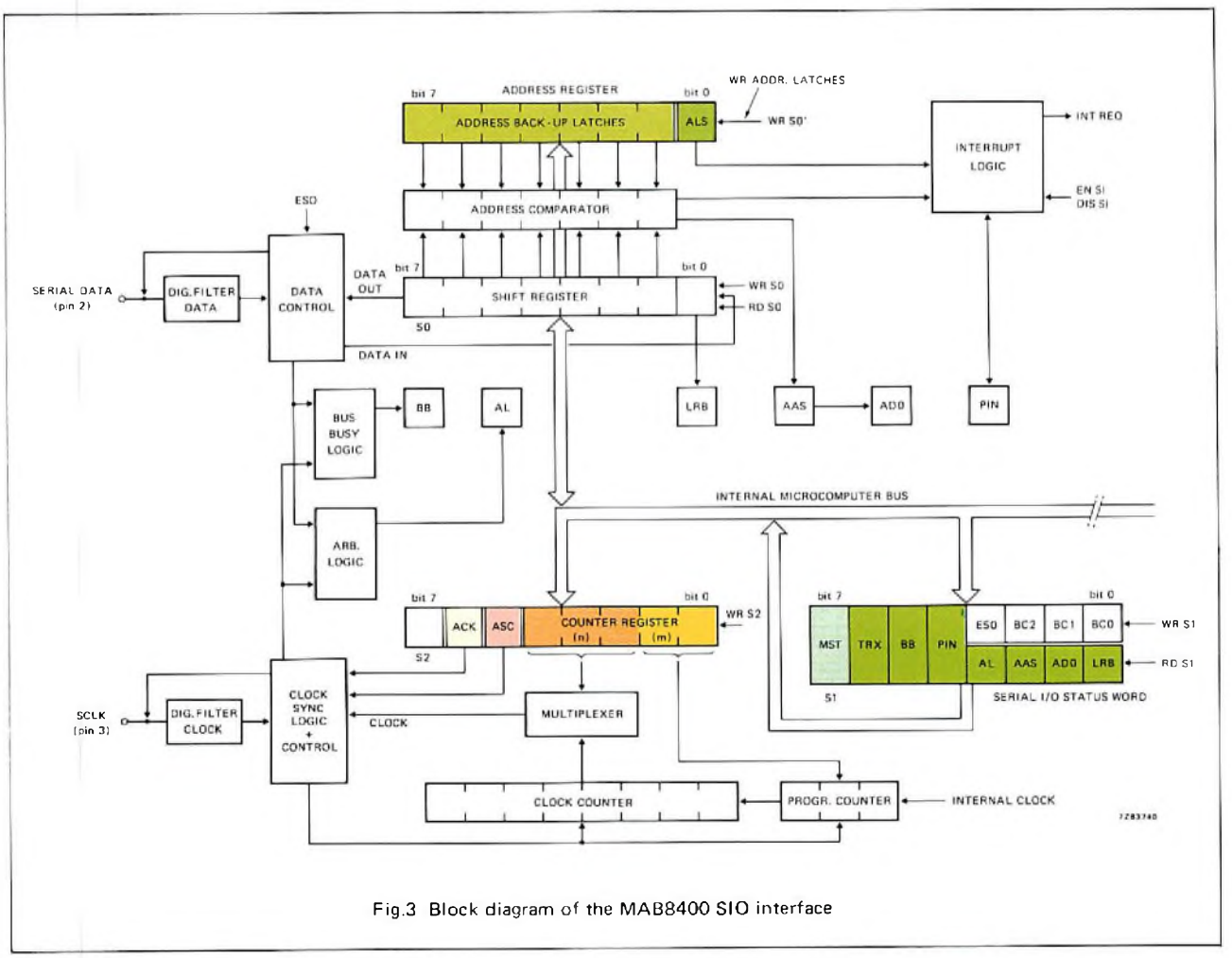


Fig.3 Block diagram of the MAB8400 SIO interface

- data shift register S0
- SIO interface status word S1
- clock control word S2
- address register.

Data shift register S0

S0 is the shift register used to perform the conversion between serial and parallel data format. Data to be transmitted is loaded in S0 by the microcomputer and shifted out serially, most significant bit first. Data received on the serial bus is shifted into S0, most significant bit first. After transmission of a complete byte or reception of a complete data byte, the specific address, or the general address, a pending interrupt is generated.

Status word S1

S1 provides information for the microcomputer about the state of the interface and stores interface control information from the microcomputer. The bit allocation of S1 is shown in Fig. 4. Note that bits 0-3 are duplicated: the control bits in these positions can only be written by the microcomputer, while the interface status bits can only be read.

MST and TRX

MST (master) controls the operation of the interface as a master or slave device:

MST = 1, master device
MST = 0, slave device.

TRX determines the direction of the data transfer:

TRX = 1, transmit data
TRX = 0, receive data.

Table 1 summarises the operating modes resulting from the four combinations of MST and TRX. A slave receiver is a device that receives both data and clock signals from a master transmitter. A slave transmitter is a device that

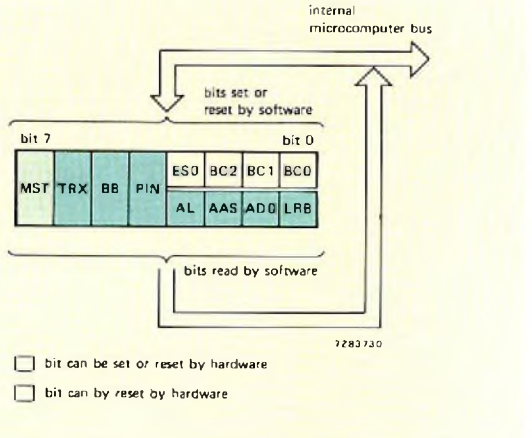


Fig.4 Bit allocation of the SIO status word, S1

TABLE 1
Operating modes of the SIO interface

MST	TRX	MODE
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

has been addressed by a master transmitter, with a request to transmit data. The slave transmitter then transmits its data in accordance with the clock signal provided by the master receiver. (The master transmitter enters the master receiver mode to receive the data from the slave transmitter). A master transmitter is the only mode of operation in which a data transfer sequence can be initiated by the start conditions.

BB: Bus Busy

The Bus Busy flag indicates the status of the bus. Whenever a start condition is detected on the bus, the Bus Busy flag is set. It is reset by detection of a stop condition on the bus. In the master transmitter mode, the Bus Busy flag is used for the generation of start and stop conditions. Should a device attempt to generate a start condition while the flag is set, the Arbitration Lost (AL) flag will be set and a pending interrupt will be generated. The start condition will not be generated.

PIN: Pending Interrupt Not

PIN = 0 indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled. The pending interrupt is cancelled whenever data is read from or, written to, register S0. A pending interrupt is generated whenever a complete byte has been transmitted, the bus arbitration procedure is lost, a complete data byte is received or a valid device address is detected.

ESO: Enable Serial Output

The ESO flag enables/disables the SIO interface:

ESO = 1, the SIO interface is enabled
pin 2 is assigned the function of the serial data line.

ESO = 0, the SIO interface is disabled
pin 2 is assigned the function of I/O signal P23
the address register can be loaded by writing to S0.

ESO is set or reset by software but cannot be read.

BC0, BC1 and BC2

BC0, BC1 and BC2 form a counter for the number of bits in the byte to be received or transmitted. The counter can be set, but not read, by the microcomputer. The content of the counter indicates the number of bits/byte, with the exception that the value zero indicates an eight-bit byte. To eliminate the risk of spurious clock pulses affecting the counter while the bus is free, generation or reception of a start condition causes the counter to be reset. This has the result that the first byte of a transfer will always consist of eight bits.

AL: Arbitration Lost

The Arbitration Lost flag is set by hardware when the SIO interface, as a master transmitter, loses a bus arbitration procedure. The interface then automatically enters the receiver mode to check if it is being addressed by the device that won the arbitration procedure. A pending interrupt will always be generated after reception of the byte during which arbitration was lost. When the microcomputer reads the status word, the Arbitration Lost flag will indicate that the required transmission did not take place. The Arbitration Lost flag will be reset when the pending interrupt is cleared (PIN = 1).

AAS: Addressed As Slave

The Addressed As Slave flag is set by hardware when the interface detects either its own specific address or the general call address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode. It is reset at the same time as the pending interrupt is cleared.

AD0: Address Zero

The Address Zero flag is set by hardware after detection of the general call address when the interface is operating in the address recognition mode. The general call address consists of a byte of eight zeros. The AD0 flag is reset when the bus becomes free after a stop condition.

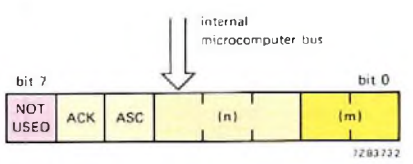


Fig.5 Bit allocation of the clock control register, S2

LRB: Last Recieved Bit

This will contain either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Clock control register S2

Clock counter control

The five least bits of S2 are used to program the serial clock counter. The serial clock signal is derived from the internal clock of the microcomputer, which is one third of the frequency generated by the crystal clock circuit. When a 4.43 MHz crystal is used, the frequency of the serial clock may be programmed within the range 720 Hz to 100 kHz, using two dividing factors m and n. As can be seen in Fig.5, bits 0 and 1 are used to specify the required value of m according to Table 2, while bits 2, 3 and 4 are used to specify the value of n according to Table 3. The frequency of the serial clock signal can be determined from the equation.

$$f_{SCLK} = \frac{f_{crystal}}{3\ m\ n}$$

ACK: Acknowledge

For operation in the acknowledgement mode, both transmitter and receiver must have ACK = 1. The master device will then generate an extra clock pulse after each complete byte, as shown in Fig. 6. During the extra clock pulse, the transmitting device holds the data line High and the receiving device acknowledges by pulling the data line Low. The transmitting device stores the received acknowledgement signal in the LRB bit of S1.

TABLE 2
Specifications of the dividing factor m

register S1 bit 1	bit 0	m
0	0	5
0	1	6
1	0	7
1	1	8

TABLE 3
Specification of the dividing factor n

register S1 bit 4	bit 3	bit 2	n
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

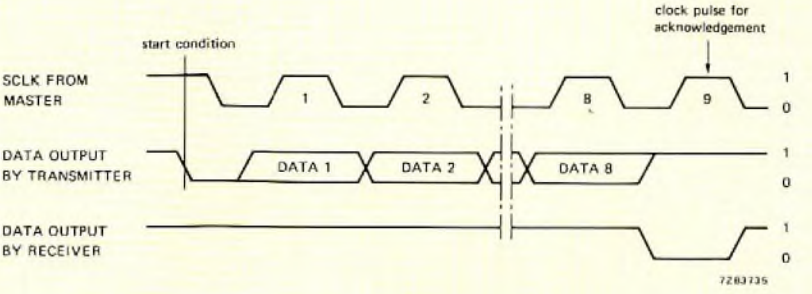


Fig.6 Acknowledgement: an extra clock pulse is generated during which the receiver pulls the data line LOW

ASC: Asymmetrical Clock

ASC = 1 causes the clock generator to generate a serial clock with a Low to High ratio of 1:3. In this case, the dividing factor n must be 128, so that bits 4, 3 and 2 of S2 must be set to 1, 1, 0 respectively. The clock frequency is then given by the equation:

$$f_{SCLK} = \frac{f_{crystal}}{384\,n}$$

Address register

The address register contains the 7-bit address back-up latches and the ALS flag, as shown in Fig.7. The address latches hold the specific address allocated to the device, while the ALS (Always Selected) flag is used to enable/disable the address recognition mode.

ALS = 1, the SIO interface will respond to all messages, regardless of address.

ALS = 0, the SIO interface will respond only to messages containing its own address or the general address. In this mode, the least significant bit of the first byte received performs the function of read/write command (write = 0). When an interface detects its own address or the general call address, it automatically sets the TRX bit of the status word to the value of the received read/write command. The general call address (eight zeros) is thus a seven-zero address with the read/write command always zero.

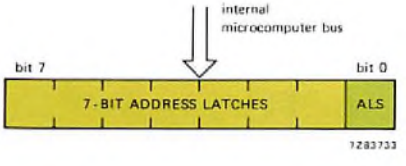


Fig.7 Address register in the SIO interface

The address register can only be loaded from the internal bus of the microcomputer when the SIO interface is disabled (ESO = 0). Under this condition, a MOV S0,A instruction will move the contents of the accumulator to the address register instead of S0, as would normally be the case.

Interrupt Logic

The interrupt logic can be enabled by an EN SI instruction, or disabled by a DIS SI instruction. When the logic is enabled, generation of a pending interrupt will result in a Serial I/O interrupt to the processor. An SIO interrupt causes the processor to execute the instruction at location 5 of its memory; the instruction is typically a jump to the beginning of the routine that handles SIO interrupts. When the logic is disabled, pending interrupts can still be serviced, as the PIN signal can be read from the SIO status word. However, the vectored interrupt will not occur.

Pending interrupts

The first pending interrupt in a transfer sequence is generated when:

- a complete byte (data or address) has been transmitted
- the general call address is received
- the specific own address is received
- eight bits have been received and ALS = 1
- an arbitration procedure is lost and a complete byte is received.

Subsequent pending interrupts will be generated after the completion of each byte.

Once a pending interrupt has been generated, the clock line will be held Low until the interrupt is cancelled. This means that there will be a delay between bytes dependent on the interrupt processing time of the devices taking part in the transfer. Only when the clock line is released by all devices concerned, can transfer of the next byte be started.

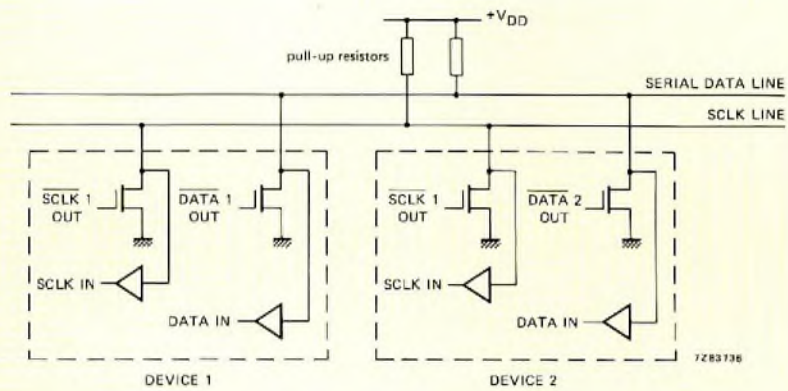


Fig.8 Bus outputs have open drain configuration

Serial I/O operations

From the foregoing descriptions, it can be seen that once a device has generated a start condition, all Bus Busy flags in the system are set and no other device can initiate a transfer until the first device leaves the bus free. However, it is possible that two or more devices give a start condition almost simultaneously, so that none detects the start condition of the other(s). An arbitration procedure has therefore been designed into the interface so that only one device gets control of the bus.

Arbitration procedure

Figure 8 shows the open drain configuration of the serial bus outputs of the 8400 which gives the bus lines the wired AND property. This means that a Low level will overrule a High level on the line. The arbitration procedure uses the data presented on the serial data line by the competing transmitters. When a transmitter senses that a High signal it has presented on the line has been overruled by a Low signal, it switches to the slave receiver mode, sets the AL flag and generates a pending interrupt at the end of the byte. Figure 9 shows the arbitration procedure between two devices. The arbitration procedure will give priority to the device that transmits the serial data stream with the lowest binary value. Should two or more devices send identical first bytes, arbitration will continue on the subsequent bytes. If the data streams are identical, an arbitration result is not necessary.

Clock synchronisation

Under normal conditions, only one master device will generate a clock signal. During the arbitration procedure, however, there are two or more master devices and the clocks must be synchronised so that the data outputs can be compared. The wired AND property of the clock line means that a device that first generates a low period of the clock line will overrule the other devices. At this High to Low transition, the clock generators of the other devices will be forced to start generation of their own Low period. The clock line will then be held Low by the device with the longest Low period, while the other devices that finish their low periods must wait for the clock line to be released before starting their High periods. A synchronised signal on the clock line is thus obtained, where the slowest device determines the length of the Low period and the fastest the length of the High period. An illustration of clock synchronisation is given in Fig. 10.

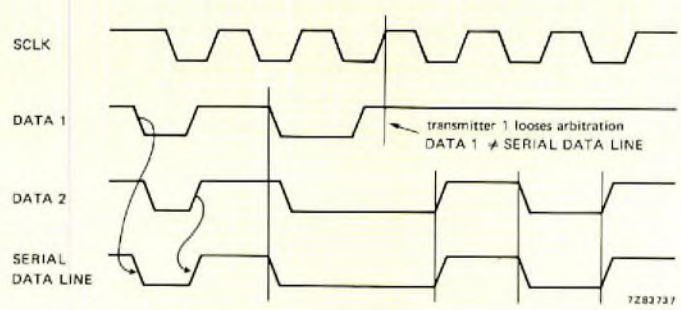


Fig.9 Arbitration procedure between two master transmitters

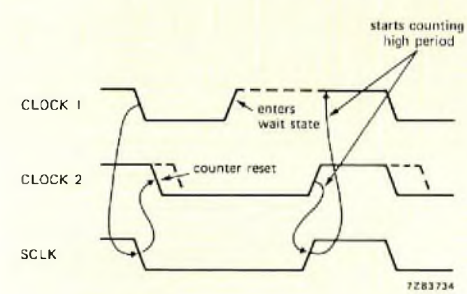


Fig.10 Synchronisation of clocks during the arbitration procedure

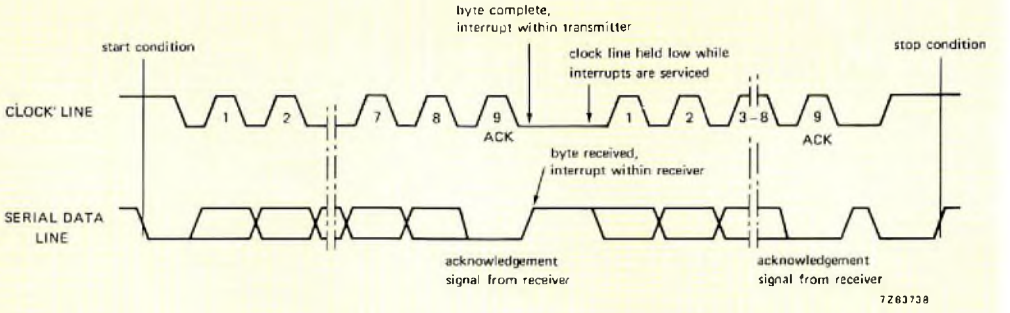


Fig.11 Transfer of two bytes without address recognition, in acknowledgement mode

Transfer modes

The 8400 SIO system has three basic transfer modes:
- transfer without address recognition
- transfer with address recognition
- transfer with asymmetrical clock.

Use of the acknowledgement procedure can be specified (ACK = 1 in both devices) with each of these three modes, giving a total of six options.

Transfer without address recognition

Transfer without address recognition is illustrated in Fig. 11. After reception or transmission of a complete byte, a pending interrupt will be generated, causing a serial interrupt request to the microcomputer if the interrupt logic is enabled. While the pending interrupt has not been serviced, the slave receiver will hold the clock line Low to indicate that it is not yet ready to continue with the subsequent data bytes. The receiver will service this interrupt by presetting the bit-counter in S1 and reading the data from S0. The transmitter will service the interrupt by presetting the bit-counter in S1 and writing data to S0. The pending interrupts are cancelled by the action of reading or writing data to or from S0. The transfer sequence is terminated by a stop condition from the master device, immediately following the last data byte.

Transfer with address recognition

In this mode, a master device can send a 7-bit slave address and read/write command bit or the general address of eight zeros as the first byte. The ALS flag of all devices should be set to zero. When a slave address is sent, only the device with that address will respond. The TRX bit of S1 will be set to the value of the read/write command bit such that the device becomes a slave receiver or a slave transmitter. The clock line will be held Low until the interrupts have been serviced in both master and slave, after which data will be shifted into, or out of, the slave's shift register under control of the clock signal from the master device. When the master has addressed a slave with the command to transmit (least significant bit of byte = 1), the TRX bit in the master device will be reset so that the device enters the master receiver mode. After the first address byte any number of subsequent bytes may be transferred in the same way as described for transfer without address recognition.

When a general address is sent, all devices will enter the slave receiver mode and wait for data bytes from the master transmitter.

Transfer with asymmetrical clock

With a High to Low ratio of 3:1, the asymmetrical clock allows a microcomputer more time per clock period for sampling the data line, making the timing of this action less critical. Furthermore, because the clock line will often be used to generate interrupts, the reduced Low period will allow the microcomputer more processing time, as the microcomputer will be forced into the interrupt handling program all the time that the clock line is Low. Otherwise, the asymmetrical clock mode is the same as transfer without address recognition.

TABLE 4
8048 instructions not supported by the 8400 family

ANLD	P, A	–
CLR	F0	JNI
CLR	F1	MOVD A, P
CPL	F0	MOVD P, A
CPL	F1	MOVP3 A, @ A
ENTO	CLK	MOVX A, @ R
JF0		MOVX @ R, A
JF1		ORLD P, A

Instructions for serial I/O

The 8400 family uses the instruction set of the 8048 microcomputer, minus the instructions listed in Table 4. Five new instructions have been defined for use with serial I/O:

MOV A,S_n
MOV S_n,A
MOV S_n, # data
EN SI
DIS SI

Details of these instructions are given in Table 5.

Developments within the MAB 8400 series

The 8400 series has been designed for use in consumer equipment, where the reduction in the total number of connections has an important bearing on product cost. Other ICs are being developed to provide a useful range of peripheral functions, such as text-handling, display drivers and serial-operated memories. An inter-IC bus has been developed to simplify the use of these peripheral circuits. Further articles in the series will describe typical applications of the 8400 series and these peripherals.

TABLE 5
New instructions for serial I/O

mnemonic	op-code hex	bytes/ cycles	description of operation	function
MOV A, S_n	0C	1/2	Move contents of SIO register n to Accumulator	(A) – (S0)
	0D			(A) – (S1)
MOV S_n, A	3C	1/2	Move Accumulator contents to serial /IO register n	(S0) – (A)
	3D			(S1) – (A)
	3E			(S2) – (A)
MOV S_n, # data	9C	2/2	Move immediate data to serial I/O register n	(S0) – data
	9D			(S1) – data
	9E			(S2) – data
EN SI	85	1/1	Enable serial I/O interrupt	
DIS SI	95	1/1	Disable serial I/O interrupt	

Acknowledgement

The author wishes to thank Mr. H. Schutte and Dr. V. Timm for their contributions to this article.

Frequency synthesiser using LSI devices

P.R. BRENNAND and B. MURRAY

The two LSI ICs HEF4750 and HEF4751 described in a previous article (Ref.1) are designed to be used as the basis of programmable high-performance frequency-synthesiser circuits which are straightforward to design and construct. This article describes the design and construction of a phase-locked loop frequency synthesiser operating over a frequency range of 154 to 156 MHz and suitable for mobile radio applications. A brief design specification is given in Table 1 and measurements made on the circuit are given later in the article. The reader is referred to Ref.1 for background information.

TABLE 1

Frequency synthesiser specification

Frequency range	154 to 156 MHz
Channel spacing	12.5 kHz
Modulation bandwidth (± 1 dB)	0.3 to 4 kHz
Modulation sensitivity	200 mV (r.m.s.) for 3 kHz deviation
Loop bandwidth	500 Hz

COMPONENTS OF A PHASE-LOCKED LOOP FREQUENCY SYNTHESISER

Figure 1 shows the main parts of a phase-locked loop frequency synthesiser. The frequency synthesiser functions by comparing a divided-down stable crystal reference ($f_r = f_{xtal}/M$) with a signal derived from the output signal (f_o) by the main divider circuit. The division ratios of both the main divider (N) and the reference divider (M) are controlled by switching circuits to facilitate switching from one frequency to another. The output frequency is defined by the expression:

$$f_o = f_{xtal}N/M.$$

The error output from the phase comparator controls the voltage-controlled oscillator (VCO) frequency. The characteristic of the loop filter determines the response of the phase-locked loop. The modulating signal is applied at two points on the loop for reasons that will be discussed later.

154 TO 156 MHz FREQUENCY SYNTHESISER

Figure 2 relates the phase-locked loop of Fig.1 to the functions provided by the HEF4750 and the HEF4751 ICs. Two prescaler stages are necessary to ensure that the signal at the input of the HEF4751 is within the acceptable frequency range of the IC. The crystal oscillator frequency chosen is 10 MHz which means, as will be shown later, that the reference divider has to provide a division ratio of 200; well within the range of the HEF4750. A channel spacing of 12.5 kHz is specified and this determines the frequency of the universal divider output signal (and hence the reference frequency).

Universal divider and prescalers

Figure 3 illustrates the configuration of the main divider and prescalers used in the frequency synthesiser. The HEF4751 operates up to a maximum input signal frequency of 9 MHz and, as the maximum phase-locked loop output frequency is 156 MHz, some frequency division is necessary between the VCO output and the

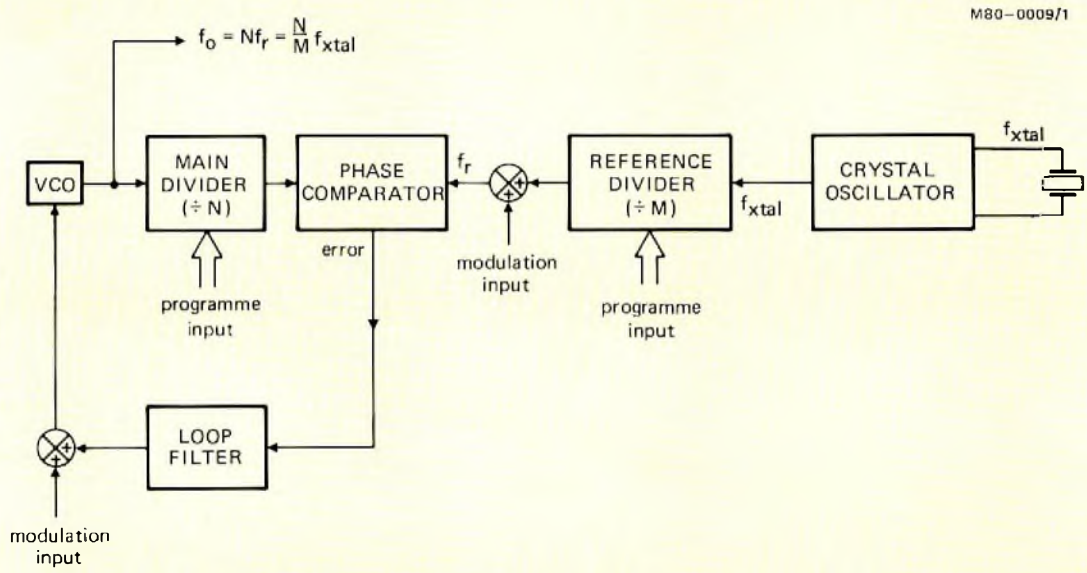


Fig.1 Basic frequency synthesiser

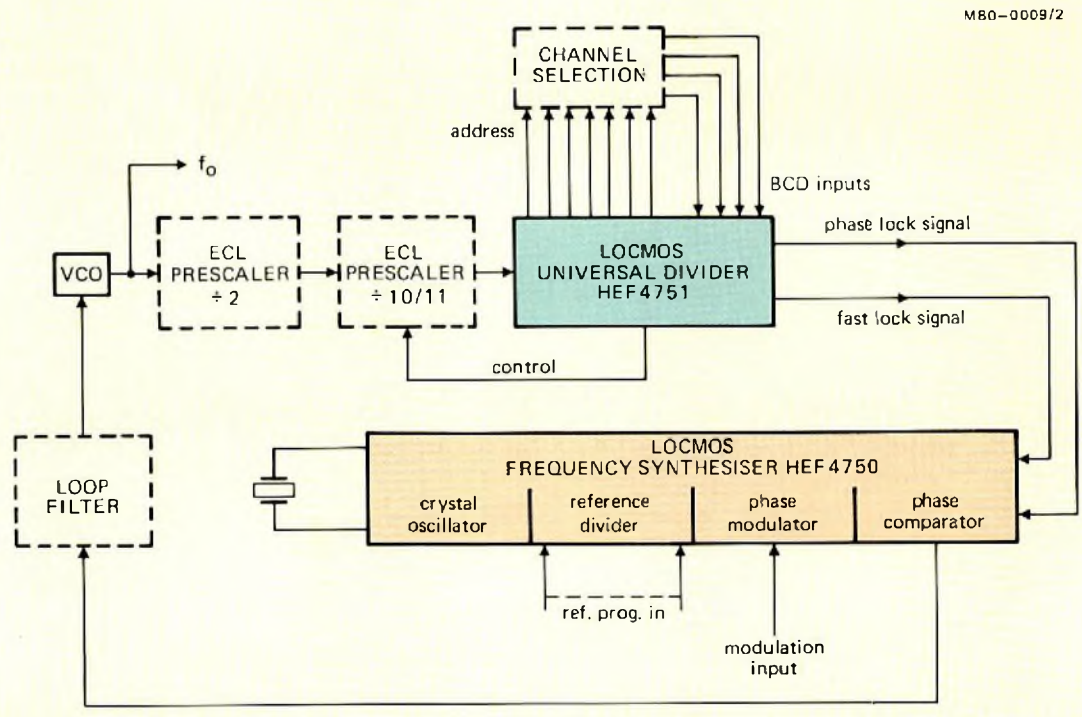


Fig.2 The HEF4750/HEF4751 frequency synthesiser system.

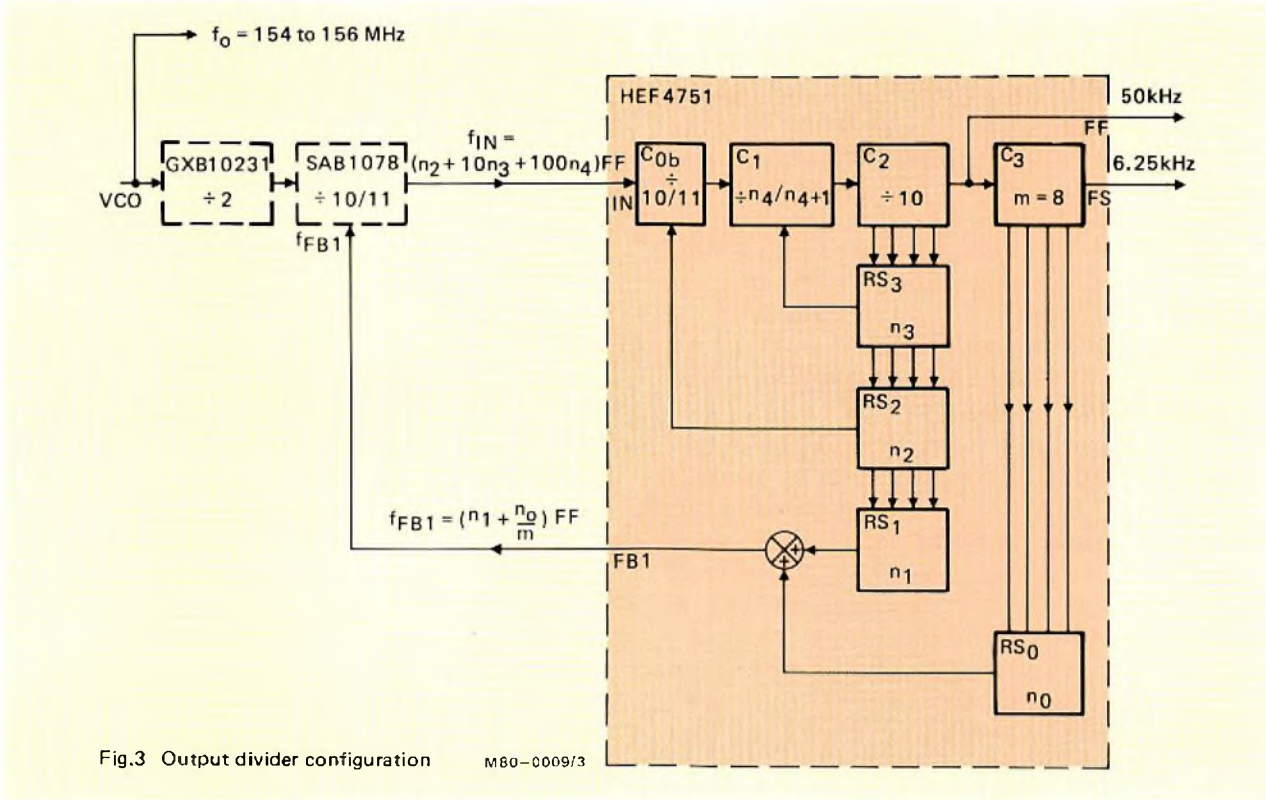


Fig.3 Output divider configuration M80–0009/3

HEF4751 input. The ECL prescaler stages shown give a division ratio of two followed by a dual modulus division ratio of 10/11. This limits the maximum input frequency to the HEF4751 to 7.8 MHz. The period of this frequency (128 ns) is suitable for the set-up requirements of the SAB1078 IC used as the ÷10/11 prescaler.

The slow output frequency (FS) of the HEF4751 universal divider is usually dictated by the specified channel spacing and any fixed divider stages that may be present between the VCO output and the HEF4751. For instance, with the configuration in Fig.3, the VCO output frequency f_o is related to FF by the expression:

$$f_o = 2\left(\frac{n_0}{m} + n_1 + 10n_2 + 10^2 n_3 + 10^3 n_4\right) FF. \quad (1)$$

Without the fixed divide-by-two stage shown (GXB10231), the relationship would be:

$$f_o = \left(\frac{n_0}{m} + n_1 + 10n_2 + 10^2 n_3 + 10^3 n_4\right) FF. \quad (2)$$

In the case of Eq.2, the lowest increment by which the VCO output frequency f_o can be changed is FF/m (= FS) and thus the frequency FS is the channel spacing enabled by the set-up. In the case of Eq.1, the lowest increment by which f_o can be changed is 2FF/m and the channel spacing is 2FS. A general expression for FS is:

$$FS = \frac{\text{channel spacing}}{p},$$

where p is the fixed division ratio preceding the HEF4751. As the channel spacing specified is 12.5 kHz, FS is required to be 6.25 kHz. The fast frequency output FF of the HEF4751 is thus set to 50 kHz, so the final division stage with a modulus of 8 generates the 6.25 kHz output (Fig.4).

The division ratio of the main divider is programmed into the HEF4751, decade-by-decade, during a sequence

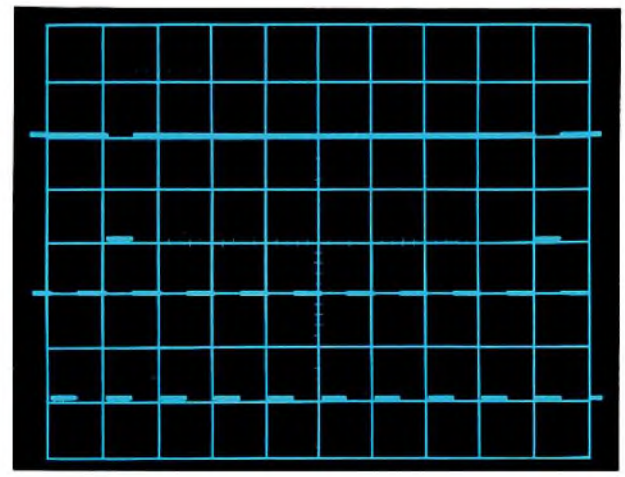


Fig.4 Universal divider outputs:
Upper trace FS, lower trace FF
Horizontal scale: 20 μs/division
Vertical scale: 5 V/division

of seven programme input periods (D_0 to D_6) triggered by the application of a programme-enable input to the device. A switching arrangement comprising binary-coded decimal thumbwheel switches can be used to set up the division ratio data; this has the advantage that it is easy for the selected frequency to be displayed on the thumbwheel switches.

The 100 MHz and 10 MHz decades are fixed at 1 and 5 so the device can be permanently wired to have the constants 1 and 5 input as division ratio data during the appropriate programme input period. The data for the 1 MHz and 100 kHz decades and the appropriate channel is set up on the BCD switches.

The programme input circuitry and the circuitry interfacing the ECL ÷10/11 prescaler with the LOCMOS universal divider is shown in the circuit diagram of the frequency synthesiser digital board, Fig.5. (For reasons discussed later, the frequency synthesiser is constructed on four boards: the digital board, the loop filter board, the modulation board, and the voltage-controlled oscillator (VCO) board.) The programme inputs to the universal divider (A_0 to A_3 and B_0 to B_3) are active in their LOW states and are read in as a series of seven parallel 2 X 4-bit inputs. Each of the seven programming intervals are signified by a 0 V signal at one of the outputs D_0 to D_6. During intervals D_0 to D_2, the data set up on the thumbwheel switches (S2) is applied to the programme inputs, and during D_3 to D_6, the fixed data determined by the diode connections between outputs D_3 to D_6 and the programme inputs is read in.

With FF = 50 kHz and FS = 6.25 kHz, five decades of programmability are required (two of which are fixed) and so the internal prescaler must be used. The significance of each decade can be seen from Fig.3 and is shown in Table 2. A frequency of 155.7375 MHz would, for example, be set by programming $n_4 = 1$, $n_3 = 5$, $n_2 = 5$, $n_1 = 7$ and $n_0 = 3$. The programme inputs to n_4, n_3 (and n_6 and m) are wired and the thumbwheel switch sets n_2, n_1, and n_0 to 5, 7, and 3, to give 5 MHz, 700 kHz, and 37.5 kHz respectively.

Reference divider

The reference divider comprises a prescaler with a modulus of 1, 2, 10, or 100 and a divider which can be set to divide by any number between 1 and 1024. All the necessary circuitry is contained in the HEF4750 IC and the correct division ratio (200) is shown set in the circuit diagram (Fig.5). Pins D_0 and D_1 of the HEF4750 are connected to the 10 V rail to give the prescaler a modulus of 100 and the divider circuit following the prescaler is programmed by the binary number connected to pins A_0 to A_9. Connecting pin A_1 to the 10 V rail and the rest to 0 V assigns a division ratio of two to this circuit so that the overall division ratio of the reference divider is 200.

TABLE 2

Universal divider input (Fig.5)

Programme period	Significance	Input data source	Input range A	Input range B	Destination	Stored value
D_0	12.5 kHz	switch	0000–0111		N_0	0–7
D_1	100 kHz	switch	0000–1001		N_1	0–9
D_2	1 MHz	switch	0100–0110		N_2	4–6
D_3	10 MHz	wired	0101		N_3	5
D_4	100 MHz	wired	0001		N_4	1
D_5	not used					
D_6	half-channel offset and internal prescaler facility	wired	1000	0011*	m	8

*The data entered into the IC at data input B during the address period D_6 determines the programming of the internal prescaler (C_{0b}, Fig.3) and the use of the half-channel offset facility described in the published data. The IC is permanently wired as shown in Fig.5 so that the B input during the D_6 period is:

B_0 and B_1 at '0' – half-channel offset not used;

B_2 and B_3 at '1' – C_{0b} set to divide by 10/11.

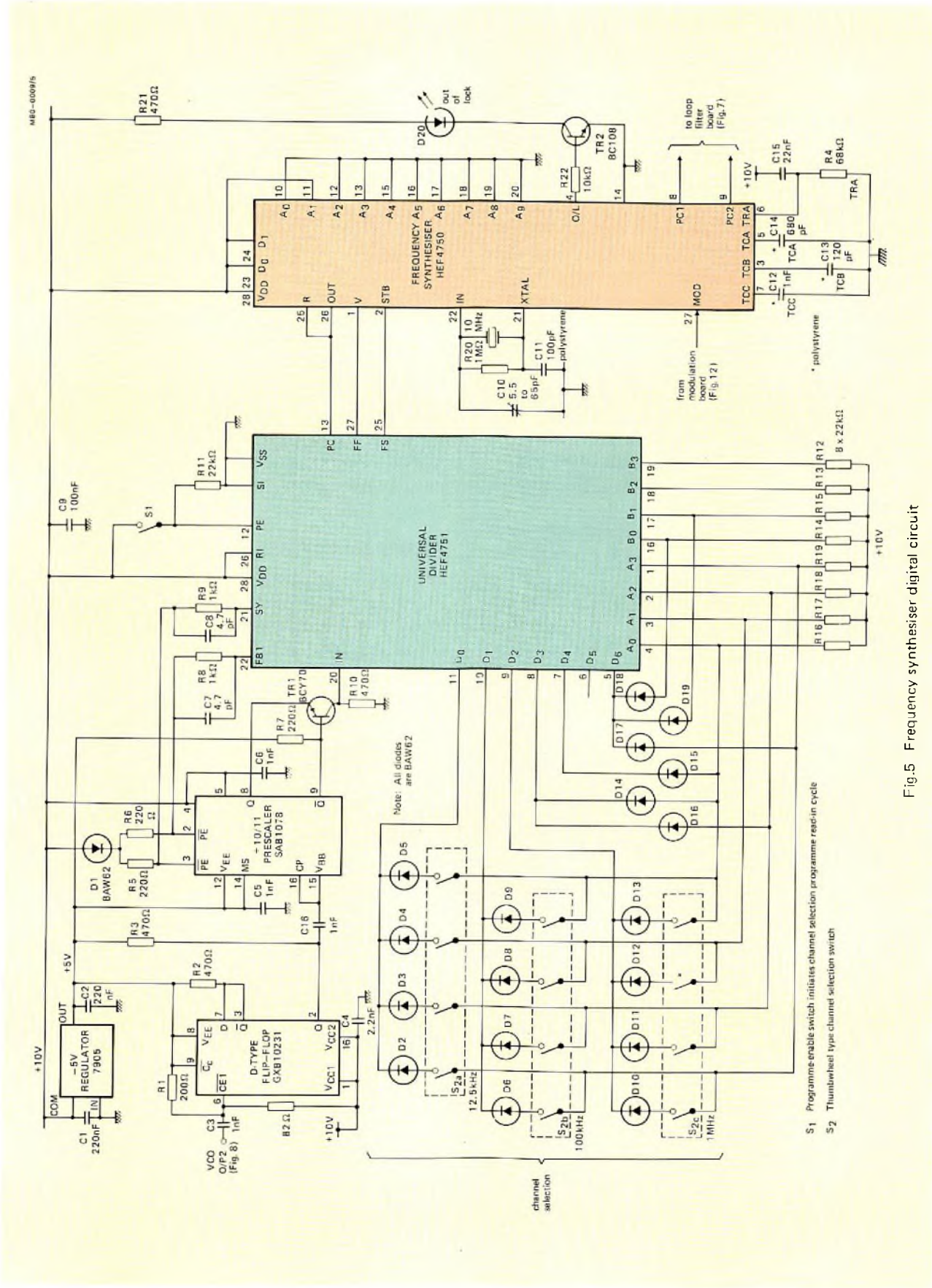


Fig.5 Frequency synthesiser digital circuit

Phase comparators and loop filter

The main phase comparator PC1 in the HEF4750 uses a sample-and-hold technique. The gain K_ϕ is fixed by the resistor at pin 6 (TRA) and the capacitor at pin 5 (TCA) and is determined by the following expression.

$$K_\phi = \frac{120(V_{DD} - V_{SS} - 3.2)}{TRA.\ TCA.\ FS}\ V/cycle,$$

where TRA is in ohms, and TCA is in farads. A gain of about 3 kV/cycle has been found ideal for most applications and TRA is typically about 68 kΩ. As FS is 6.25 kHz, TCA will be 680 pF (nearest preferred value) for this application. The 22 nF capacitor at pin 6 of the HEF4750 in Fig.5 decouples TRA to ensure good noise immunity.

Capacitor TCC is the hold capacitor for the sample-and-hold circuit. The main consideration when choosing TCC is that it is a low leakage type and that, when combined with its driving impedance of about 700 Ω, it does not cause excessive phase shift which could lead to loop instability. A value of 1 nF is chosen. The modulation capacitor TCB is discussed later.

The two phase comparators are designed to be used with an inverting second-order filter of the type shown in Fig.6.

The component values are governed by the following equations:

$$R_1 C_1 = \frac{3K_V K_\phi}{N\omega^2}, \qquad (3)$$

$$R_2 C_1 = \frac{3}{\omega}, \qquad (4)$$

$$R_4 C_2 = \frac{1}{3\omega}, \qquad (5)$$

where K_V is the coarse VCO gain in Hz/volt, K_ϕ is the phase comparator gain (3 kV/cycle), N is the total division ratio of the main divider, that is, f_o/FS, and ω is the loop bandwidth in radians/second.

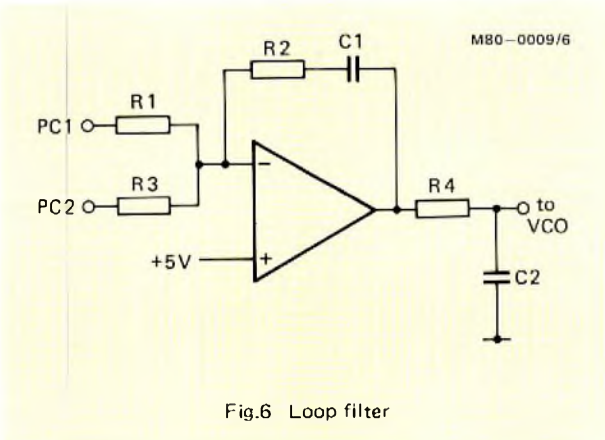


Fig.6 Loop filter

To cover the frequency range required, a coarse VCO gain of 300 kHz/V is chosen. The loop bandwidth is $\pi \times 10^3$ radians/sec and N, the division ratio is:

$$N = \frac{155 \times 10^6}{6.25 \times 10^3} = 24\,800.$$

Hence

$$R_1 C_1 = 11\ ms, \qquad R_2 C_1 = 954\ \mu s,$$
$$R_4 C_2 = 106\ \mu s.$$

The capacitors C_1 and C_2 are chosen as 100 and 10 nF respectively and the above equations indicate that preferred values of 110 kΩ, 10 kΩ, and 10 kΩ can be selected for resistors R_1, R_2, and R_4 respectively.

Figure 7 shows the circuit diagram of the loop filter board. Resistor R_3 should be between one-tenth and one-hundredth of the value of R_1 for a satisfactory performance and a good settling time. A value of 10 kΩ is selected. It is useful to be able to adjust R_2 slightly for optimum system performance, and therefore a 22 kΩ potentiometer is used.

Voltage-controlled oscillator

The voltage-controlled oscillator (VCO), shown in Fig.8, is a simple Hartley oscillator with varicap diode tuning. It uses a BFR84 dual-gate MOSFET as the active device. Coarse and fine control inputs are applied to BB105B varicap diodes. The 'fine' varicap diode is referenced to the positive supply so its control voltage is decreased to increase the resonant frequency of the tuned circuit. The gains of the two control inputs are:

$$\text{coarse gain} \simeq 300\ kHz/V$$

$$\text{fine gain} \simeq -10\ kHz/V.$$

The coil (L_4) is tapped at a point which gives a turns ratio of about 1.5, the tap being near the earthed end of the coil. This is found to be the best compromise satisfying the conflicting requirements of maintaining reverse bias on the varicap diodes, and obtaining the maximum signal-to-noise ratio by having the highest possible signal amplitude in the tuned circuit. The g_2 gate of the BFR84 is biased to 5 V and must be well decoupled at high frequencies.

The output is taken from a small drain resistor to a two-stage buffer, TR_2 and TR_3, which drives the ECL prescaler. Two stages of buffering provide good isolation from the input impedance changes of the prescaler, which can otherwise result in unwanted modulation sidebands appearing at the synthesiser output.

The frequency synthesiser output is also fed from the drain resistor via a single-stage buffer (TR_4) to provide an output power of approximately 1 mW into 50 Ω.

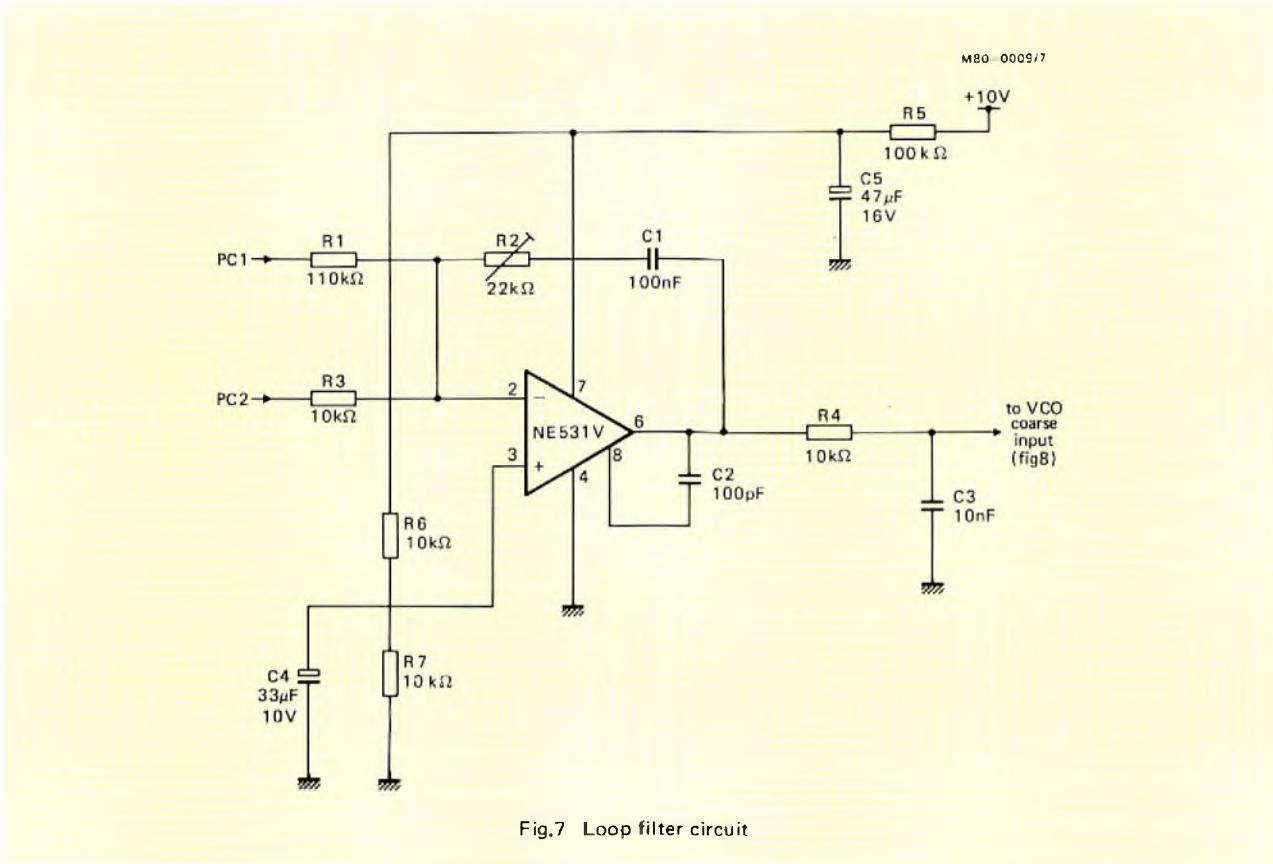


Fig.7 Loop filter circuit

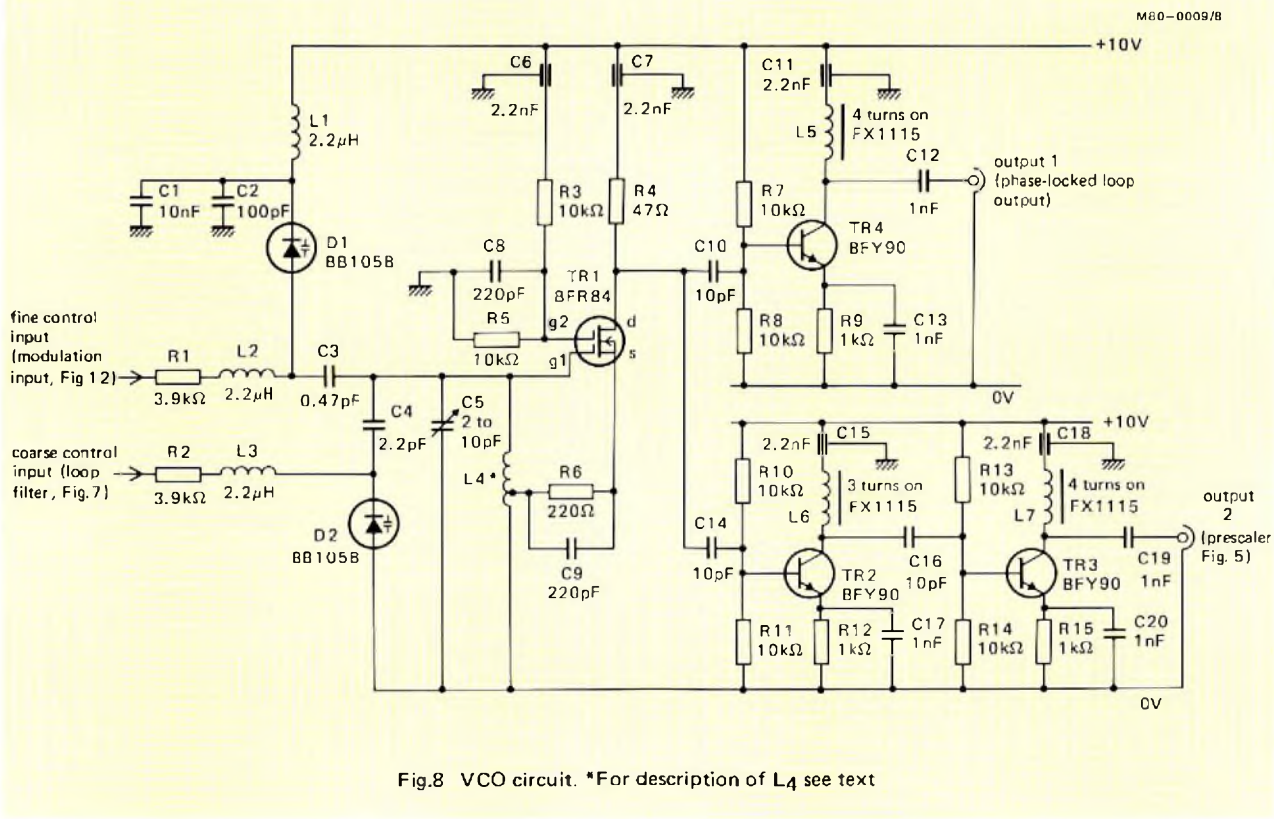


Fig.8 VCO circuit. *For description of L_4 see text

FREQUENCY MODULATION

HEF4750 phase modulator

The HEF4750 IC has an on-chip phase modulator which can be used to frequency or phase modulate the r.f. output of a synthesiser. It applies a voltage-controlled delay to the edge of the input at pin 1 (V) before it is input to the phase comparator. Its operation is illustrated in Fig.9 and is briefly described in the following paragraph.

When a negative-going edge is applied to pin 1 of the HEF4750, the D-type latch is set, generating a V′ pulse for the IC logic and switching the comparator input switch to the position shown. The constant-current source charges capacitor TCB to produce a positive-going ramp at TCB and the positive comparator input. Waveforms are shown in Fig.10. The ramp starts at V_{SS} (0 V) and causes the comparator to change state when it reaches a voltage equal to $(V_{MOD} - V_S)$. The D-type latch is cleared when the comparator changes state, terminating the V′ pulse to the IC logic and resetting the comparator input switch. Capacitor TCB is immediately discharged to 0 V so that the circuit is reset to the start condition. The rising edge of the V′ pulse is used as the active edge for the phase comparator and the technique produces linear phase modulation. The gain of the phase modulator is determined by the slope of the ramp on TCB, and is given by:

$$K_{pm} = \frac{\text{TCB. TRA. FS}}{27\,(V_{DD} - V_{SS} - 3.2)} \text{ cycles/V.} \qquad (6)$$

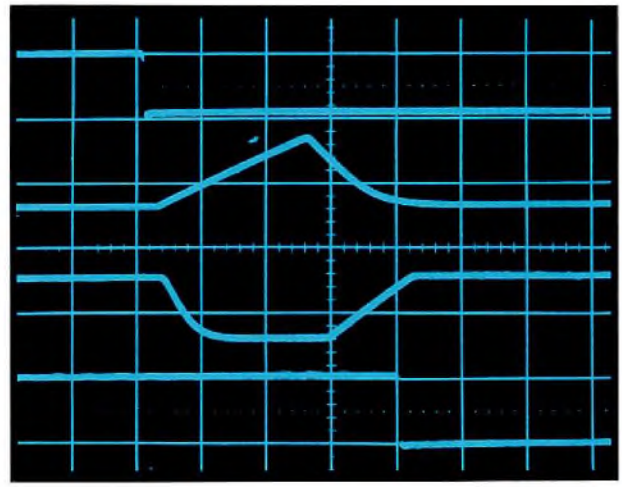


Fig.10 HEF4750 locked-state waveforms. From top to bottom: V, TCB, TCA, R. Horizontal scale: 200 ns/division

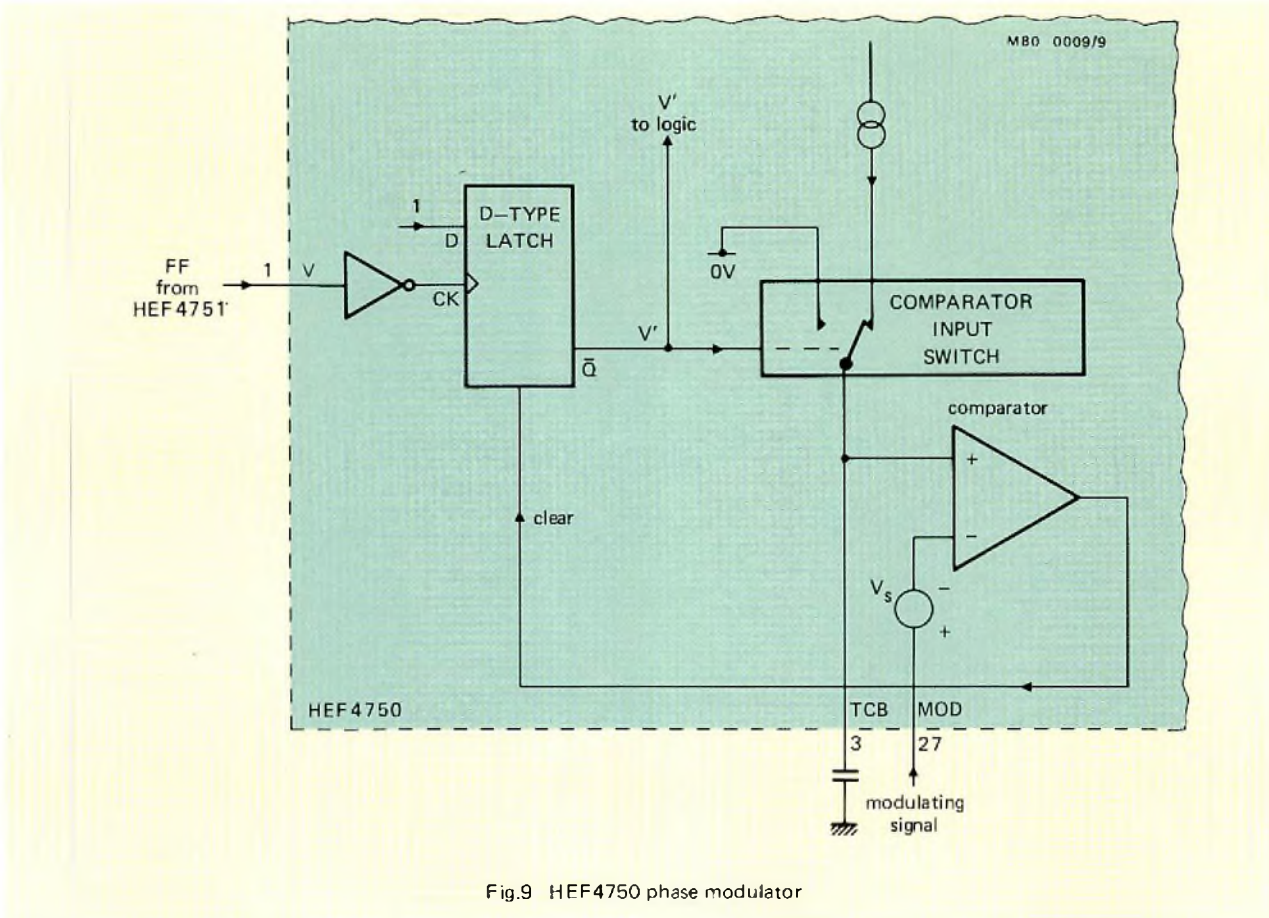


Fig.9 HEF4750 phase modulator

Two-point modulation

Applying frequency modulation to a single point on a phase-locked loop frequency synthesiser characterises the modulation sensitivity with either a high-pass or low-pass response, depending upon the point at which the modulation is applied. It also causes the generation of spurious signals which, in a mobile radio system, occur in adjacent channels. This latter effect is due to the sampling action of the comparator operating in the presence of a modulating signal. A flat frequency response is obviously desirable and the suppression of spurious signals is necessary to meet statutory requirements. A method of two-point modulation described in Ref.2 overcomes these problems; it gives an essentially constant modulation sensitivity and suppresses spurious signals. The technique is briefly discussed in the following paragraphs to explain the operation of the modulation input circuits in the frequency synthesiser described.

If a modulating signal is applied to the phase modulator input (MOD) of the HEF4750 the phase comparator converts the difference in phase between the modulated output of the phase modulator and the phase-locked loop output signal to an error voltage which is applied to the VCO. The error signal modulates the VCO output but the low-pass loop filter between the phase comparator and the VCO attenuates the error signal and reduces the modulation sensitivity at high frequencies.

Applying the modulation of the VCO itself, via the fine control input, would seem to be the answer but the action of the loop corrects the frequency of the output signal and thus counteracts the modulation. The low-pass loop filter now has the reverse effect. As it attenuates high-frequency signals from the phase comparator, the correcting action of the loop reduces modulation sensitivity at low frequencies and the modulation sensitivity has a high-pass characteristic.

A two-point modulation technique suggests itself as a method of counteracting one effect with the other; the arrangement shown in Fig.11 is used in the circuit under discussion. The transfer functions of the input networks (K_x and K_y) have to be calculated so that the resultant phase difference across the phase comparator input caused by the modulating signal $V_m(s)$ is zero. The other constants in Fig.11 are:

K_f, fine VCO gain,

N, main divider division ratio,

K_{pm}, phase modulator gain.

The additional factor, s, accounts for the fact that it is the frequency, not the phase, of the VCO, which is proportional to the control voltage.

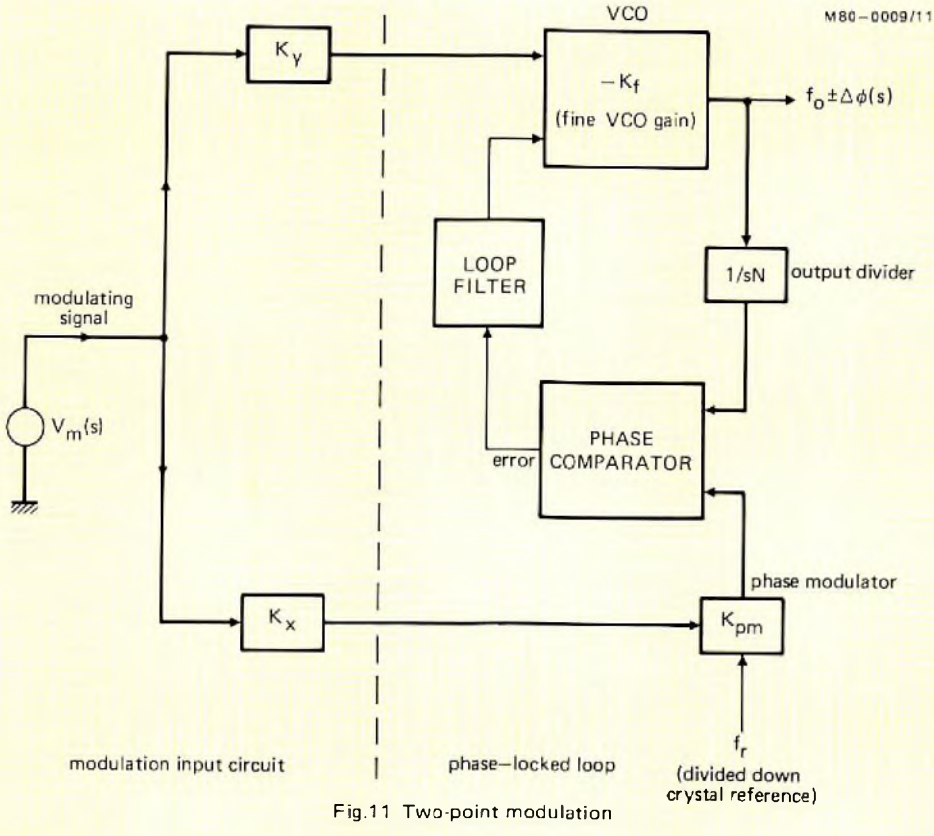


Fig.11 Two-point modulation

It is easy to see from Fig.11 that the following condition must be realised to achieve zero phase difference at the phase comparator input:

$$-\frac{K_y K_f}{sN} = K_x K_{pm},$$

or

$$\frac{K_x}{K_y} = \frac{-K_f}{sNK_{pm}}. \quad (7)$$

If K_x and K_y are single-section low-pass and high-pass RC filters with transfer functions:

$$K_x = \frac{1}{1+sT} \text{ (low-pass)},$$

$$K_y = \frac{sT}{1+sT} \text{ (high-pass)},$$

where T is the filter time-constant, then:

$$\frac{K_x}{K_y} = \frac{1}{sT}.$$

The characteristic of the network is that of a pure integrator. As the right-hand side of Eq.7 is negative, an inversion is required in either the K_x or K_y path. The K_x path contains the inversion in the circuit under discussion and this characterises the frequency synthesiser with inverted frequency modulation (increasing the modulating voltage decreases the r.f. frequency). Non-inverted frequency modulation is obtained with the inversion in the K_y path. Often this is of no consequence, but there may be some applications in which there is a specification for one or the other of the two methods.

Equation 7 can be written as:

$$\frac{1}{T} = \frac{-K_f}{NK_{pm}}. \quad (8)$$

When this is satisfied, the modulation transfer function is simply $-K_fK_y$, and so the modulation frequency response has a high-pass characteristic with a −3 dB frequency of:

$$f_{(-3\text{ dB})} = \frac{1}{2\pi T}.$$

The frequency synthesiser discussed here is designed to be less than 1 dB down at 300 Hz, and so a value of T = 1.2 ms is chosen. The modulation sensitivity is $|K_y|K_f$, and this should be chosen to meet the requirements of the particular application, bearing in mind that no more than about 500 mV r.m.s. should be applied at the phase modulator input (the MOD pin of the HEF4750). A sensitivity of 10 kHz/V was obtained by setting the fine VCO gain to this value and designing the high-pass K_y section to have unity gain. Other systems may require gain or attenuation in the K_y path to achieve the necessary value of sensitivity. It is, however, good practice to keep the value of K_f fairly low to maintain good linearity.

The remaining variable concerned with 'balancing' the input to the phase comparator is K_{pm}. This can be varied by changing the value of TCB but as too high a value will degrade the noise performance, it is better to make the gain of the K_x section variable. In any case, an adjustment must be provided to enable the exact balance to be set up. Whatever form this adjustment takes, it must provide a means of altering the relative gains of the K_x and K_y sections, and should allow variation of the calculated value of relative gains in either direction. Writing Eq.8 as:

$$\frac{NK_{pm}}{T} = -K_f, \quad (9)$$

and taking,

TCB = 120 pF,
TRA = 68 kΩ,
FS = 6.25 kHz,
N = 24 800 (at 155 MHz),
T = 1.2 ms,

Eq.6 gives K_{pm} as 0.28×10^{-3} and thus the left-hand side of Eq.9 = 5.78 kHz/V. As already mentioned, the modulation sensitivity $|K_y|K_f$ selected is 10 kHz/V, achieved by choosing the high-pass (K_y) filter to have unity gain and setting the fine VCO gain K_f to 10 kHz/V. The difference between the left-hand side of Eq.9 and the selected value of K_f is compensated by assigning a gain of 1.75 to K_x.

The implementation of this design could take many forms, subject to the requirement that the phase modulator input pin, MOD on the HEF4750, is biased to about 6 V, and that the VCO fine-control input is biased at about half the supply voltage. The configuration shown in Fig.12, using an operational amplifier in each input circuit, provides a versatile means of setting up the necessary gains and d.c. conditions. Arrangements with fewer components are possible, but careful design is necessary to avoid extraneous phase shifts and setting-up problems. Certainly with the circuit shown the setting-up procedure is very simple – a large modulating signal at a frequency close to the natural frequency of the loop (about 500 Hz) is applied, and the 100 kΩ preset potentiometer is adjusted to give a minimum signal amplitude on the PC1 pin of the HEF4750. The only point to note is that, if the synthesiser has a fine adjustment available on its frequency reference (in this case the trimmer in the crystal oscillator), then this must be set up first. Varying FS will affect the phase modulator gain, K_{pm} (see Eq.6), and this in turn will disturb the balance of Eqs.8 and 9 unless f_{xtal} and thus FS is set up first.

Theoretically, the balance condition holds for only

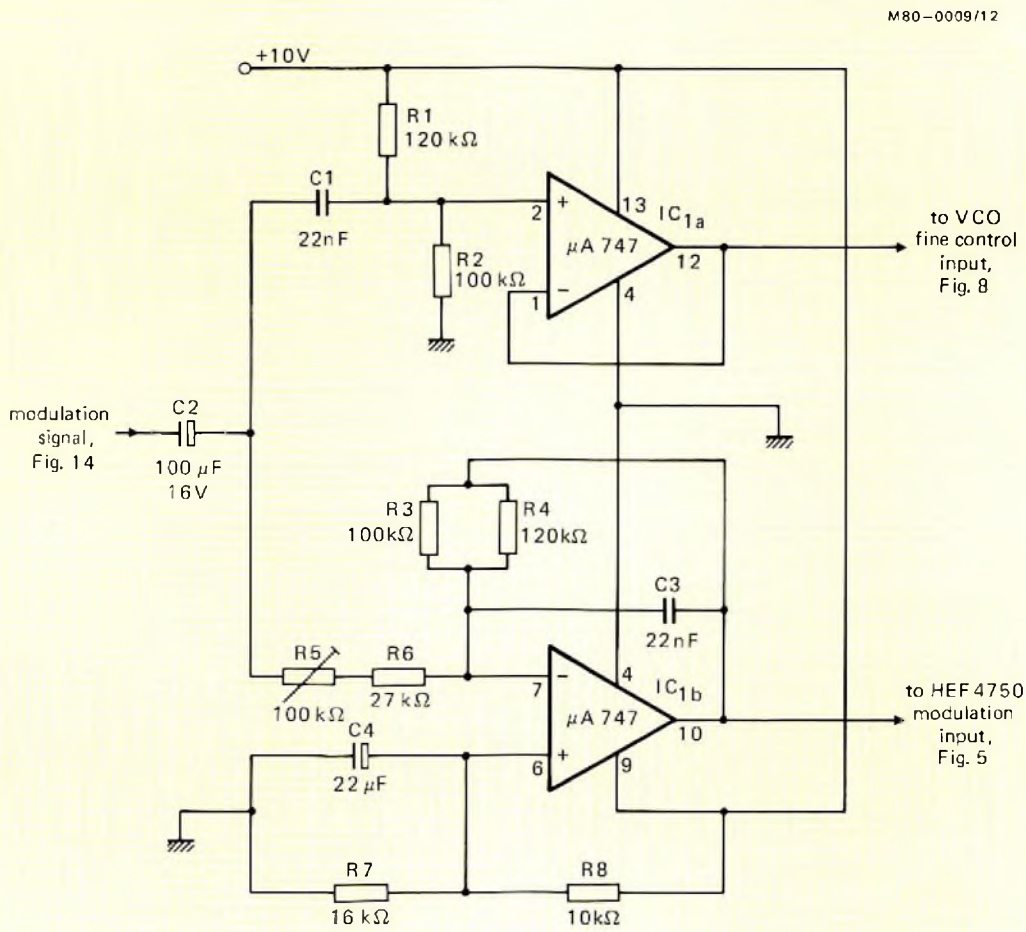


Fig.12 Modulator circuit

one value of division ratio, implying that the system goes out of balance if the r.f. frequency is changed. In practice, however, this variation is offset by the varying value of the fine VCO gain K_f. As the r.f. frequency is increased (by increasing the division ratio) then the capacitance of the main varicap diode is reduced to increase the tuned circuit resonant frequency. The fine varicap diode is therefore 'swamped' less by the main one, and the value of K_f is increased. By varying the ratio of coarse and fine VCO gains, the effect of division ratio variation can be almost completely eliminated.

The curves in Fig.13 were obtained from the circuit shown in Figs.5, 7, 8, 12, and 14, and illustrate the excellent results obtained. Figure 13a shows the flat modulation frequency response, while Fig.13b shows the audio spectrum of the demodulated r.f. output of the synthesiser when it is modulated at a frequency of 1 kHz and a constant amplitude of ±3 kHz peak deviation. The cancellation of spurious signals generated by sampling is good, the residual spurii probably being due to a mismatch between the values of time-constant T in the K_x and K_y paths. An additional adjustment could be incorporated to account for this at the expense of greater complexity in the setting-up procedure. The modulation distortion is also shown plotted against frequency (Fig.13c). It is constant at a value of about 1.5% (governed by the fine linearity) except at low frequencies where the phase modulator introduces some additional distortion.

CONSTRUCTION

The HEF4750 and HEF4751 LSI circuits not only greatly simplify frequency synthesiser design but they also make the construction of the circuit far more

Fig.13a Modulation sensitivity against modulation frequency plotted relative to 0 dB level of 3 kHz deviation at 1 kHz; r.f. frequency = 155 MHz

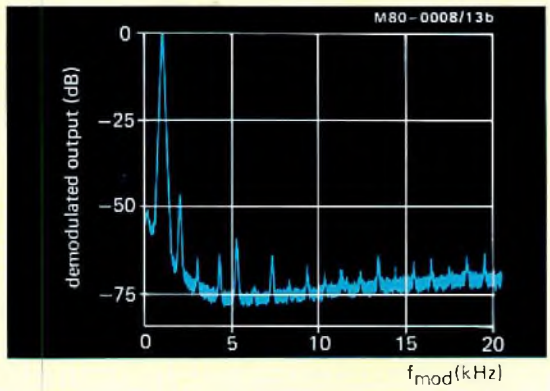


Fig.13b Demodulation spectrum plotted relative to 0 dB level of 3 kHz deviation at 1 kHz; r.f. frequency = 155 MHz

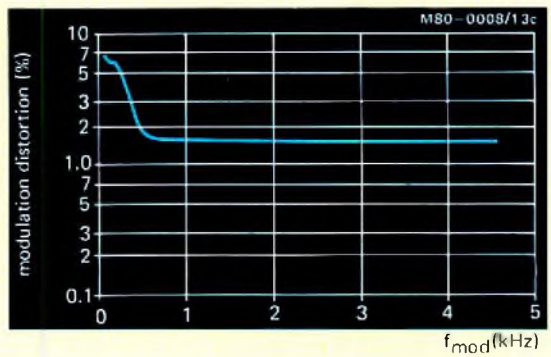


Fig.13c Demodulation distortion against modulation frequency

straightforward. The layout of the system is not critical but certain precautions must be taken for optimum performance. Efficient decoupling of the power supplies is most important and this is why the synthesiser circuit uses four separate printed-wiring boards (Fig.14). Earth plane construction is advisable for components working at v.h.f., and therefore the VCO and digital boards are double-sided with an earth plane on the upper side. The VCO and loop filter boards are best mounted in a screened box with screened leads used for all interconnections. This considerably reduces the stray pick-up of signals (especially 6.25 kHz and 50 kHz).

The layout of the modulation circuitry is not critical, and in the prototype, normal single-sided printed-wiring board was used. The complete synthesiser was mounted on an earthed aluminium base board together with the thumbwheel switches for the binary-coded decimal programme input and the programme-enable switch. This further reduces stray pickup.

MEASUREMENTS

Measurement of noise and spurii

The noise and spurious signal levels can be examined by feeding the synthesiser output directly to a v.h.f. spectrum analyser. In general, however, the measurement of a high-performance frequency synthesiser will require more sophisticated techniques. The arrangement shown in Fig.15 uses a low-frequency spectrum analyser to obtain better resolution. The synthesiser output is mixed with a high quality local oscillator signal to give a 10.7 MHz output. This is fed via a narrow bandpass crystal filter (±3.75 kHz) to the spectrum analyser. If the synthesiser frequency is changed by one channel, the mixer output will be outside the filter passband and the analyser gain can be increased by about 40 dB, allowing examination of the noise level and reference frequency sidebands in the adjacent channel.

The results of such a measurement are shown in Fig.16 and show the synthesiser to exhibit an adjacent channel noise level of −120 dB/Hz and reference frequency sidebands of −88 dBC.

Measurement of lock time

Measuring the lock time of the synthesiser requires the use of a storage oscilloscope or facilities to switch the synthesiser continuously between two frequencies. The latter approach was chosen and the switching unit shown in Fig.17 was constructed to perform the switching function.

A pulse generator running at approximately 100 Hz is

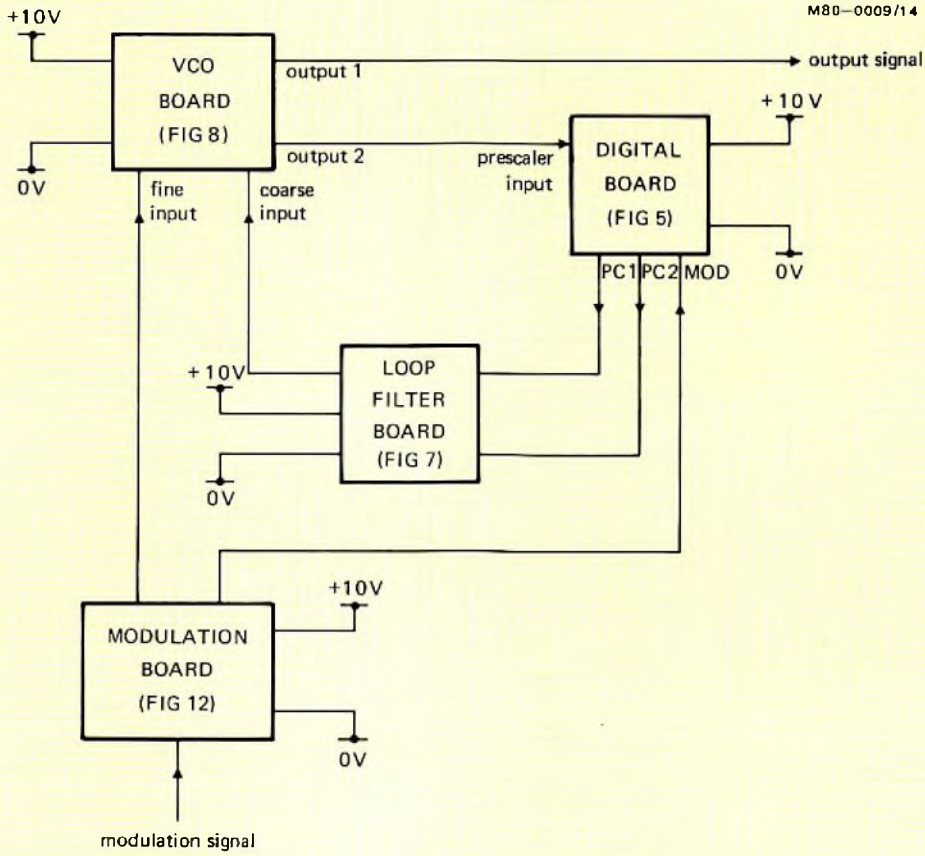


Fig.14 Frequency synthesiser board interconnections

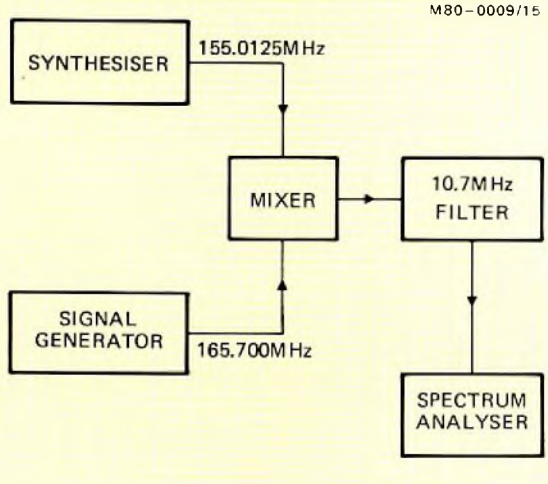


Fig.15 Measurement of noise and spurii

used to clock the programme-enable pin on the HEF4751. The 100 Hz signal is divided down to 50 Hz by a suitably connected D-type latch, and enabled on to data line A_0 by a tri-state buffer whenever address line D_2 goes low. Thus data line A_0 is alternately high and low at consecutive active periods of the address line D_2. The synthesiser is set to a frequency of 154 MHz so that it is switched between 154 MHz and 155 MHz by the alternating input at A_0. The synthesiser output is mixed with a signal of 165.7 MHz, so that as the synthesiser comes into tune at 155 MHz, the mixer output comes within the passband of the 10.7 MHz filter. The filter output therefore has an envelope shape which depends on the difference between the instantaneous synthesiser frequency and 155 MHz. The time required for the synthesiser to lock can be measured by triggering the oscilloscope with the appropriate latch output. Figure 18 shows frequency jumps of 1 MHz, 100 kHz, and 12.5 kHz. The upper trace shows the filter output and the lower trace shows the state of the out-of-lock output from the IC.

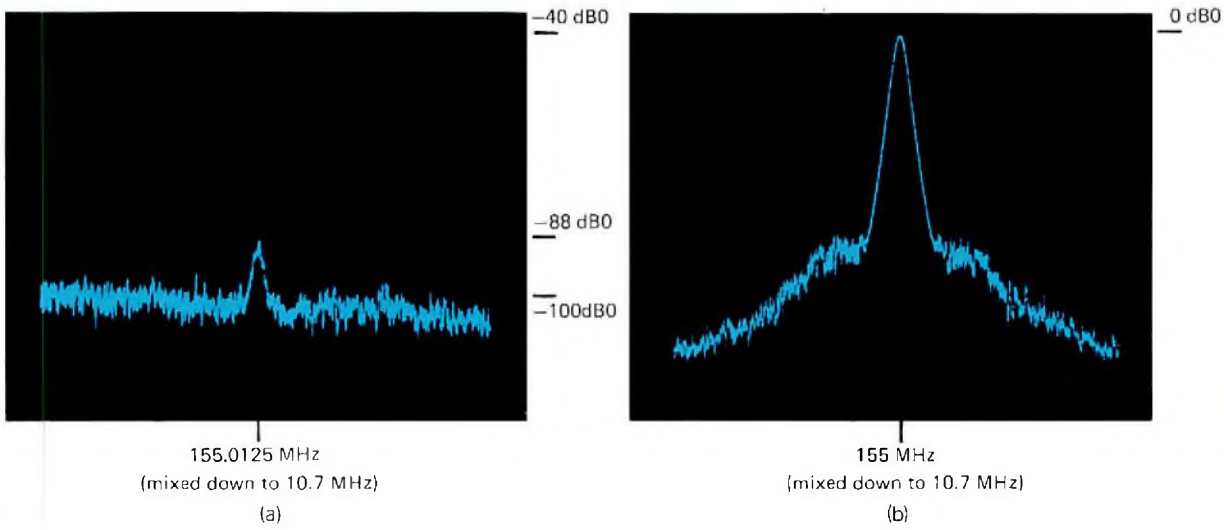


Fig.16 Noise and spurii: (a) adjacent channel noise level (b) on channel spectrum

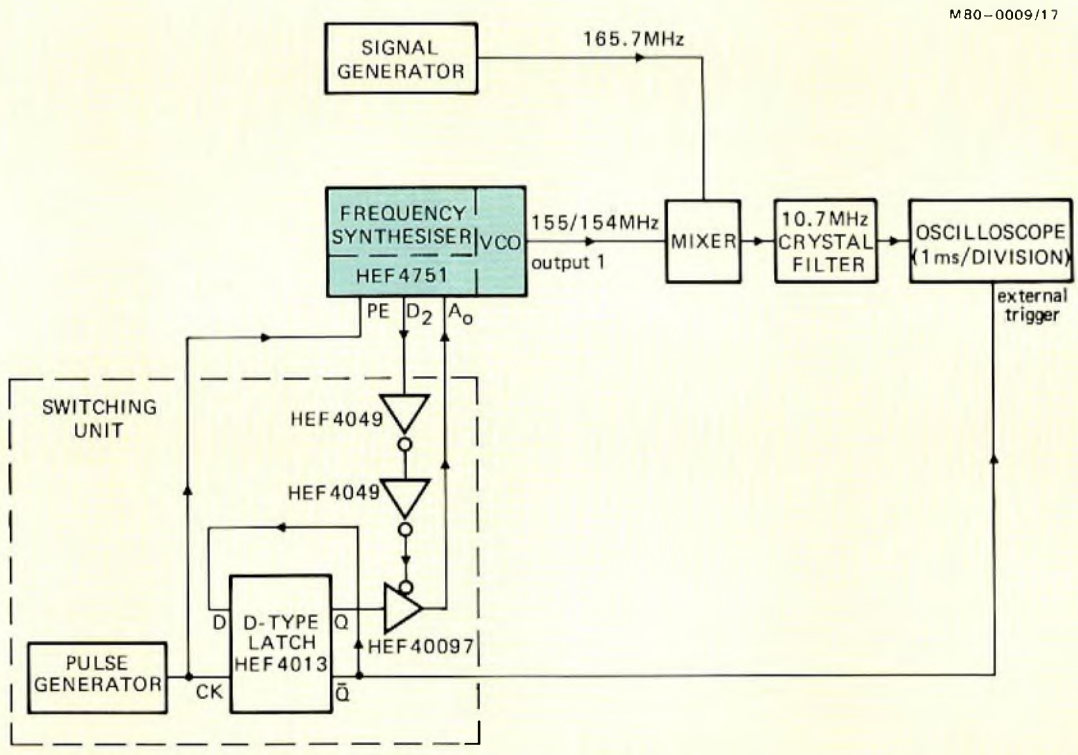


Fig.17 Measurement of lock time for 1 MHz jump

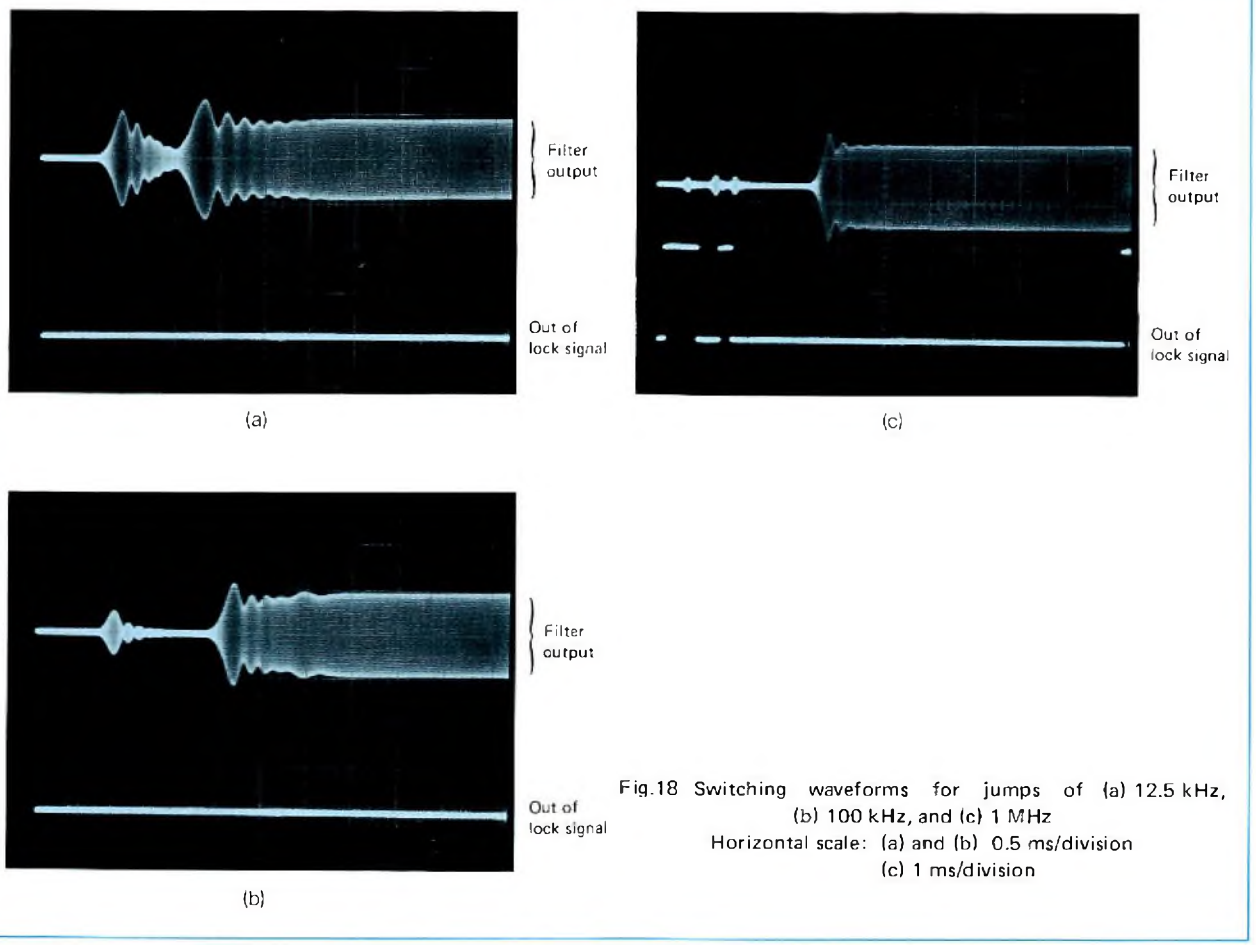


Fig.18 Switching waveforms for jumps of (a) 12.5 kHz, (b) 100 kHz, and (c) 1 MHz
Horizontal scale: (a) and (b) 0.5 ms/division
(c) 1 ms/division

PERFORMANCE

Table 3 summarises the overall performance of the frequency synthesiser.

TABLE 3

Frequency synthesiser performance

Noise at ± 12.5 kHz in 1 Hz bandwidth	−120 dBC
Discrete spurious signals at ± 12 kHz	−88 dBC
Switching time for 1 MHz change	4 ms
Modulation bandwidth at 3 kHz deviation	0.3 to 4 kHz ±1 dB
Modulation distortion at 3 kHz deviation	1.5%
Total current consumption	200 mA at 10 V

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1. GILES, T.G., 'Versatile LSI frequency synthesiser system', Electronic Components and Applications, Vol.2, No.2, February 1980, pp.91-105.
2. SCOTT, R.I.H. and UNDERHILL, M.J., 'FM modulation of frequency synthesisers', IERE Conference on Land Mobile Radio, Lancaster (UK), September 1979.

Abstracts

Semiconductor laser for information readout

The CQL10 semiconductor laser comprises essentially three GaAs layers in each of which Al replaces some of the Ga: an active layer with 16% replaced, sandwiched between two layers with 46% replaced. The laser produces a divergent light beam whose wavelength (780 nm) remains constant even at ambient temperatures as high as 60 °C. Designed for use in digital-optical readout systems, the CQL10 is smaller and more efficient than the conventional helium-neon laser, and requires a supply of only 2 to 3 V.

Analogue control system for a.c. motor with PWM variable speed drive

This article, the fourth in a series, describes a control system for use with pulse-width modulation variable speed drive for a.c. motors. The system provides a wide range of facilities meeting the requirements of most users but avoiding excessive complexity.

Highlight handling with diode-gun Plumbicon tubes

To read out highlights in a televised scene, dynamic beam control (DBC) increases the camera-tube beam current whenever a highlight is encountered. DBC is effectively limited to camera tubes with large beam current reserve, so the new range of diode-gun Plumbicon tubes, which are characterized by very high slope, are ideal. The highlight handling ability of DBC is comparable with that of the ACT (anti-comet-tail) Plumbicon, and its simple, low-power circuitry makes it ideally suited to ENG and EFP.

Ceramic permanent magnets for d.c. motors

The interdependence of the electrical, magnetic and mechanical characteristics of the most common form of permanent-magnet motor is analysed using classical motor design formulae. The expressions derived relate motor performance at various temperatures to the volume and magnetic properties of the stator magnets.

A new hybrid stepping motor design

Owing to the way the stator of a conventional hybrid stepping motor is wound, manufacturers can offer only a limited range of step angles. A new design using ring coils permits a range of step angles and motor sizes far beyond those possible using exisitng hybrid motor concepts. The permanent magnet is located in the stator and the motor uses only one pole pair per phase, giving a very high torque-to-volume ratio.

Frequency synthesiser using LSI devices

Two LSI devices described in a previous article (HEF4750 and HEF4751) form the basis of a high-performance, phase-locked loop frequency synthesiser which is programmable and can be switched throughout the range 154 to 156 MHz with a 12.5 kHz channel spacing.

Serial I/O with MAB8400 series microcomputers

The first of a series about special aspects of the MAB8400 series microcomputers, this article describes the function and operation of the on-chip serial input/output interface. The 8400 series microcomputers are developed from the proven 8048/8021 devices to provide microcomputers with additional dedicated functions suited to the consumer-electronics market.

Halbleiter-Laser zum Auslesen von Informationen

Der Halbleiter-Laser CQL10 besteht im wesentlichen aus drei GaAs-Schichten, bei denen jeweils ein Teil des Galliumarsenids durch Aluminium ersetzt ist. Der Laser erzeugt einen divergenten Lichtstrahl, dessen Wellenlänge (780 nm) bei Umgebungstemperaturen bis hin zu 60°C konstant bleibt. Der für die Anwendung in optodigitalen Lesesystemen vorgesehene Halbleiter-Laser CQL10 ist kleiner als ein konventioneller Helium-Neon-Laser und besitzt einen höheren Wirkungsgrad.

Ein System zur kontinuierlichen Drehzahlregelung von Induktionsmotoren mittels Impulsbreiten-Modulation

Dieser Artikel, der vierte einer Serie, beschreibt ein Antriebssystem für Induktionsmotoren, bei dem die Drehzahlregelung durch Impulsbreiten-Modulation vorgenommen wird. Mit diesem System lassen sich ohne übermässigen Aufwand die Anforderungen der meisten Anwender erfüllen.

Spitzlichtverarbeitung durch Plumbicon-Röhren mit Dioden-Elektronenstrahlsystem

Das Verarbeiten von Spitzlichtern in einer Fernseh-Szene kann mit Hilfe von Strahlstromsteuerung (DBC, Dynamic Beam Control) vorgenommen werden. Bei diesem Verfahren wird der Strahlstrom stark erhöht, sobald ein Spitzlicht auftritt. Das DBC-Verfahren ist Kameraröhren mit hoher Strahlstromreserve vorbehalten wie der neue Reihe von Plumbicon-Röhren mit Dioden-Elektronenstrahlsystem. Die Spitzlichtverarbeitung mit DBC ist vergleichbar mit der des ACT (anti-comet-tail)-Plumbicons; ferner ist das Verfahren aufgrund seiner einfachen, wenig Leistung beanspruchenden Schaltung ideal für ENG- und EFP-Anwendungen geeignet.

Keramische Permanentmagnete für Gleichstrommotoren

Die gegenseitige Abhängigkeit der elektrischen, magnetischen und mechanischen Kenngrössen der üblichen Dauermagnetmotoren wird mit Hilfe der klassischen Motor-Konstruktionsformeln analysiert. Die abgeleiteten Ausdrücke setzen das Motorverhalten bei verschiedenen Temperaturen in eine Beziehung zum Volumen und zu den magnetischen Eigenschaften der Statormagnete.

Eine neue Hybrid-Schrittmotor-Entwicklung

Da der Stator der herkömmlichen Hybrid-Schrittmotoren eine durchgezogene Wicklung enthält, lassen sich derartige Motoren nur mit einem begrenzten Schrittwinkelbereich herstellen. Der neue, mit Ringspulen arbeitende Motor übertrifft bezüglich Schrittwinkelbereich und Motorabmessungen die Möglichkeiten der herkömmlichen Hybrid-Motoren bei weitem.

Frequenz-Synthesizer mit hochintegrierten Halbleiterschaltungen

Zwei in einem früheren Artikel beschriebene hochintegrierte Halbleiterschaltungen (HEF4750 und HEF4751) bilden die Basis für einen besonders leistungsfähigen PLL-Frequenz-Synthesizer, der programmierbar ist und sich im Frequenzbereich von 154 MHz bis 156 MHz in Schritten von 12.5 kHz (Kanalabstand) durchschalten lässt. Der Entwurf und die Schaltungsausführung des Frequenz-Synthesizers und des Modulators werden beschrieben und deren Eigenschaften in Form von Massergebnissen angegeben.

Serielle Datenein- und ausgabe bei der Mikrocomputer-Familie MAB8400

Dieser erste einer Reihe von Artikeln über die besonderen Eigenschaften der Mikrocomputer-Familie MAB8400 beschreibt die Funktion und Arbeitsweise des auf dem Chip befindlichen Interfaces zur seriellen Datenein- und ausgabe. Die Mikrocomputer der Familie MAB8400 sind eine Weiterentwicklung der bewährten Mikrocomputer 8048 und 8021 und haben zusätzliche Eigenschaften die sie für Anwendungen in der Konsum-Elektronik besonders geeignet machen.

Laser à semiconducteur pour la lecture des informations

Le laser à semiconducteur CQL10 comprend essentiellement trois couches de Ga(1 – x)Al(x)As: une couche active avec x = 0.16 prise en sandwich entre deux couches pour lesquelles x = 0.46. Le laser produit un faisceau lumineux divergent dont la longueur d'onde (780 nm) reste constante même pour des températures ambiantes atteignant 60 °C. Conçu pour les systèmes de lecture numérique/optique, le CQL10 est plus petit et plus efficace que le laser classique à l'hélium-néon, et ne nécessite qu'une alimentation de 2 à 3 V.

Système de commande analogique pour moteur à courant alternatif avec variateur de vitesse à modulation par impulsion de largeur variable

Quatrième d'une série, cet article décrit un système de commande pour des moteurs à courant alternatif utilisant un variateur de vitesse à modulation par impulsion de largeur variable. Le système offre, sans trop de complexité, des possibilités multiples qui répondent aux impératifs de la plupart des utilisateurs.

Analyse de zones suréclairées à l'aide de tubes Plumbicon à canon diode

Pour analyser correctement les zones suréclairées d'une scène télévisée, le contrôl dynamique de faisceau (DBC) augmente le courant de faisceau du tube de la caméra chaque fois qu'une plage lumineuse se présente. L'application du contrôle dynamique est en fait limitée aux tubes disposant d'une vaste réserve de courant de faisceau, et la nouvelle gamme de tubes Plumbicon à canon à diodes, caractérisés par une pente très élevée, conviennent donc parfaitement. Le contrôle dynamique de faisceau (DBC) présente des propriétés de traitement des zones suréclairées comparables à celles du tube Plumbicon ACT (anti-comet-tail), et son circuit simple à faible consommation le destine parfaitement à des applications de reportage ENG et EFP.

Aimant permanent céramique pour moteurs à courant continue

L'interdépendance des caractéristique électriques, magnétiques et mécaniques du moteur à aimant permanent du type le plus courant est analysée à partir des formules d'étude classique des moteurs. Les expressions qui en résultent relient les performances du moteur, pour diverses températures, au volume et aux propriétés magnétiques des aimants du stator.

Un moteur pas-à-pas hybride d'un nouveau type

Compte tenu du mode de bobinage du stator dans un moteur pas-à-pas hybride classique, les fabricants ne peuvent offrir qu'une gamme limitée d'angles de pas. Une nouvelle conception reposant sur des bobines toroïdales permet d'obtenir une gamme d'angles de pas et de tailles de moteur nettement supérieure à celle que permettait l'utilisation des concepts existants de moteurs hybrides.

Synthétiseur de fréquence utilisant l'intégration à grande échelle

Deux dispositifs intégrés LSI décrits dans un article précédent (HEF4750 et HEF4751) constituent la base d'un synthétiseur de fréquence à boucle à blocage de phase à haute performance; ce synthétiseur est programmable et peut être commuté sur toute la gamme de 154 à 156 MHz avec un écart entre deux canaux de 12.5 kHz.

Interfaces d'entrée/sortie série avec les micro-ordinateurs de la série MAB8400

Premier d'une série consacrée aux aspects particuliers des micro-ordinateurs de la série MAB8400, cet article décrit le fonctionnement et l'utilisation de l'interface d'entrée/sortie série "mono plaquette". Les micro-ordinateurs de la série 8400 sont développés à partir des dispositifs éprouvés 8048/8021 pour obtenir des micro-ordinateurs pourvus de fonctions spécialisées supplémentaires parfaitement adaptées au marché électronique grand public.

Laser semiconductores para leer información

El laser semiconductor CQL10 contiene esencialmente tres capas de GaAs en cada una de las cuales el Al sustituye al Ga: una capa activa con un 16% sustituido entre dos capas con el 46% sustituido. La inversión de la población, esencial para emisión simulada, tiene lugar en la capa activa, la cual actua efectivamente como una trampa electrón/hueco. El laser produce un haz de luz divergente cuya longitud de onda (780 nm) permanece constante incluso a temperaturas ambientes del orden de 60 °C. Diseñado para utilizarlo en sistemas de lectura óptico-digital, el CQL10 es más pequeño y más eficiente que el laser convencional de helio-neón, y requiere una alimentación de sólo 2 a 3 V.

Sistema de control analógico para un motor de c.a. con velocidad variable por modulación de anchura de impulsos

Este artículo, el cuarto de una serie, describe un sistema de control para utilizarlo con motores de c.a. con velocidad variable por modulación de anchura de impulsos. El sistema proporciona un amplio margen de posibilidades que cumplen sin excesiva complejidad los requisitos de la mayoría de usuarios.

Tratamiento de puntos brillantes con tubos Plumbicón

Para eliminar puntos brillantes en una escena televisada, el control dinámico de la haz (DBC, Dynamic Beam Control) hace que aumente la corriente de haz del tubo de cámara siempre que se encuentre con un punto brillante. El control dinámico de haz está efectivamente limitado en tubos de cámara con gran reserva de haz, de modo que los tubos de la nueva gama, que se caracterizan por una pendiente muy elevada, son ideales. La eficacia del tratamiento de los puntos brillantes del DBC puede compararse a la del ATC (anticola de cometa), y su circuitería sencilla de baja potencia lo hace muy adecuado para los fines ENG y EFP.

Imanes permanentes cerámicos para motores de c.c.

Para analizar la interdependencia de las características eléctricas, magnéticas y mecánicas del tipo más corriente de imán permanente usado en motores se recurre a las fórmulas ya conocidas para el diseño de un motor. Las expresiones establecidas ponen el rendimiento del motor, a diferentes temperaturas, en función del volumen y propiedades magnéticas de los imanes del estator.

Un nuevo diseño de motor paso a paso híbrido

Debido a que el estator de un motor híbrido paso a paso convencional está bobinado, los fabricantes pueden ofrecer solamente una gama limitada de ángulos de paso. Un nuevo diseño que utiliza bobinas en anillo, permite un márgen de ángulos de paso y tamaños de motor muy por encima de los que son posibles con los conceptos de motor híbrido existentes.

Sintetizador de frecuencia con dispositivos LSI

Dos dispositivos LSI, que fueron descritos en un artículo anterior, (HEF4750 y HEF4751) constituyen la base de un sintetizador de frecuencia de largo enclavado en fase (PLL) que es programable y puede ser conmutado en el margen de 154 a 156 MHz con una separación de canales de 12.5 kHz.

E/S en serie con microordenadores de la serie MAB8400

Es el primero de una serie de artículos sobre los aspectos especiales de los microordenadores de la serie MAB8400. Describe la función y operación del acoplamiento de entrada/salida en serie incorporado en el chip. Los microordenadores de la serie 8400 están desarrollados a partir de los dispositivos ya conocidos 8048/8021, para ofrecer microordenadores con funciones específicas adicionales adecuadas para el mercado de la electrónica de consumo.

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Printed in The Netherlands