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"Mr Watson, come here, I want you."

Little more than a century stands between Bell's first, faint, room-to-room call and this 27 metre satellite tracking antenna at Burum in Friesland that now relays thousands of telephone conversations a day between two continents. Anticipating tomorrow's needs, advances in telephone technology are reaching not only out into space to expand network capacity, but also back into the home and local exchange to improve convenience, speed, and service. This issue of EC&A takes note of two developments in step with that trend. The carbon microphone that has been a feature of the subscriber's set since the inception of public telephone service is overdue for retirement; the article beginning on page 150 announces an electret replacement compatible with existing lines. And the article beginning on page 175 describes an integrated circuit that puts the convenience of pushbutton dialling within reach of subscribers connected to exchanges not yet converted to fully electronic dialling.

Contents

Inverter circuit for a PWM motor speed control system

F. J. BURGUM and E. B. G. NIJHOF

This article describes an inverter circuit developed specifically for use in Pulse-Width Modulation (PWM) speed control systems for three-phase a.c. motors. The article is the second in a series. The first article (Ref.1) gave a general introduction to our PWM speed control system. This system uses the technique of sinewave-modulated pulse-width modulation, and employs a purpose-designed LSI circuit type HEF4752V for signal generation. With the exception of the introductory article, each article in the series will concentrate on one particular aspect of the system.

The inverter is a major advance on previous inverter designs, and has the following advantages.

- It places the lowest possible stress on the thyristors and diodes, limiting the peak voltage on these devices to not more than 10% above the supply voltage. This means that low-voltage thyristors and diodes can be used for a relatively high-voltage supply.
- Full commutation capability is available at any time. There are no starting problems, and no special triggering sequence is required to prime the inverter.
- No delay is necessary between successive commutations. The minimum pulse width is therefore equal to the commutation cycle time, and a high modulation depth is possible.
- It is highly efficient. A high switching frequency is possible, only a small amount of the commutation energy is lost, and there are no circulating currents.
- It does not need reverse-blocking thyristors. ASCRs can therefore be used, and since there are no reverse-recovery losses, efficiency will be increased.
- The commutation energy does not vary with the load current.

CIRCUIT DESCRIPTION

The complete inverter consists of three identical phases, one for each of the outputs R, Y, and B. A complete circuit diagram of a single phase is shown in Fig.1, and a photograph of a typical assembled circuit is shown in Fig.2. The main thyristors Th_1 and Th_2 control the power throughput of the inverter, while main diodes D_1 and D_2 carry reactive and regenerative currents from the load to the supply. The main thyristor is commutated off by triggering the appropriate commutation thyristor: Th_3 for main thyristor Th_1, and Th_4 for main thyristor Th_2. When Th_3 is triggered, commutation current flows in the commutation circuit Th_3, L_1, C_5, and D_3. Similarly, components Th_4, L_2, C_6, and D_4 make up the commutation circuit for Th_2.

RC snubber networks R_1C_1, R_2C_2, R_3C_3, and R_4C_4 limit the rate of rise of reapplied voltage to the thyristors after they have been turned off. Inductor L_3 limits the rate of rise of on-state current of the main thyristors. The rate of rise of on-state current in the commutation thyristors is limited by the commutation inductors L_1 and L_2. Resistor-diode networks D_5, D_7, R_6 and D_6, D_8, R_5 limit the maximum charge on the commutation capacitors C_5 and C_6, and the peak voltage on the commutation thyristors Th_3 and Th_4. Charging resistors R_7 and R_8 ensure that the commutation capacitors are charged when first applying voltage to the d.c. supply.

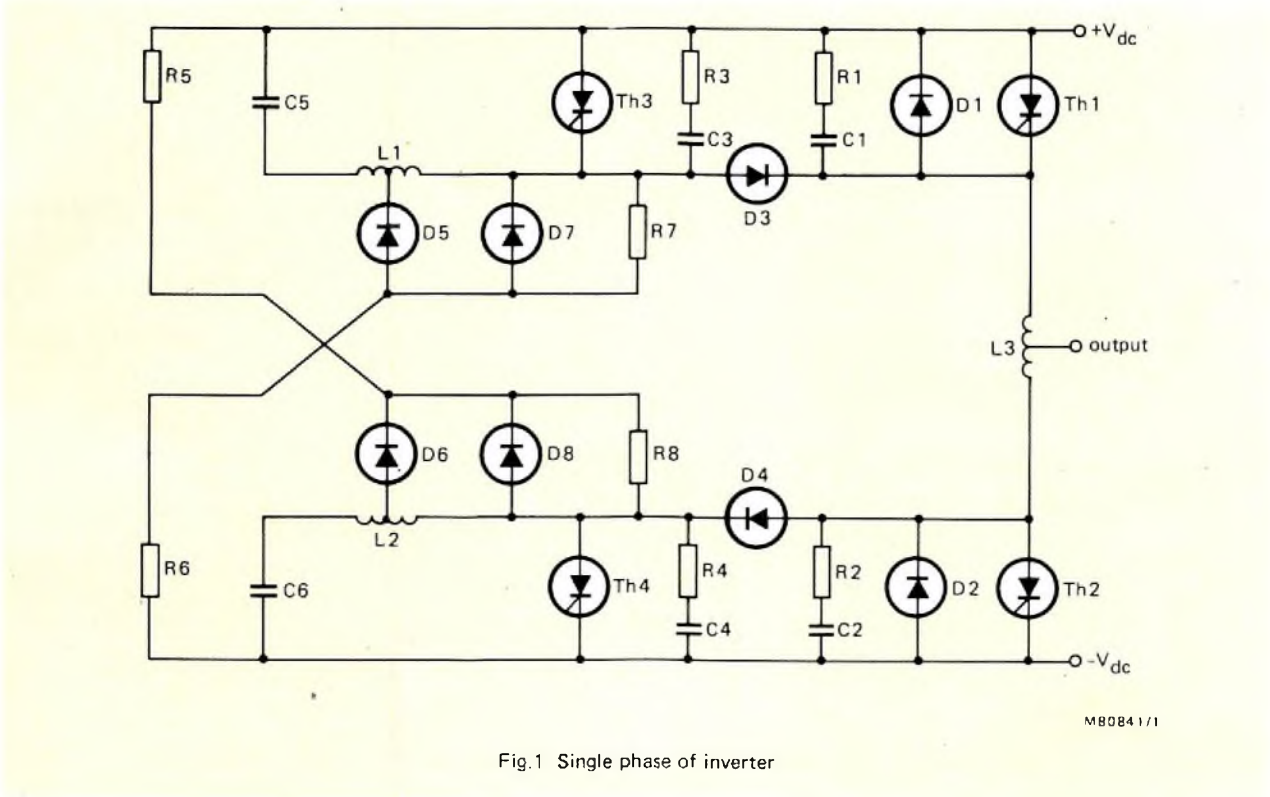

Fig.1 Single phase of inverter

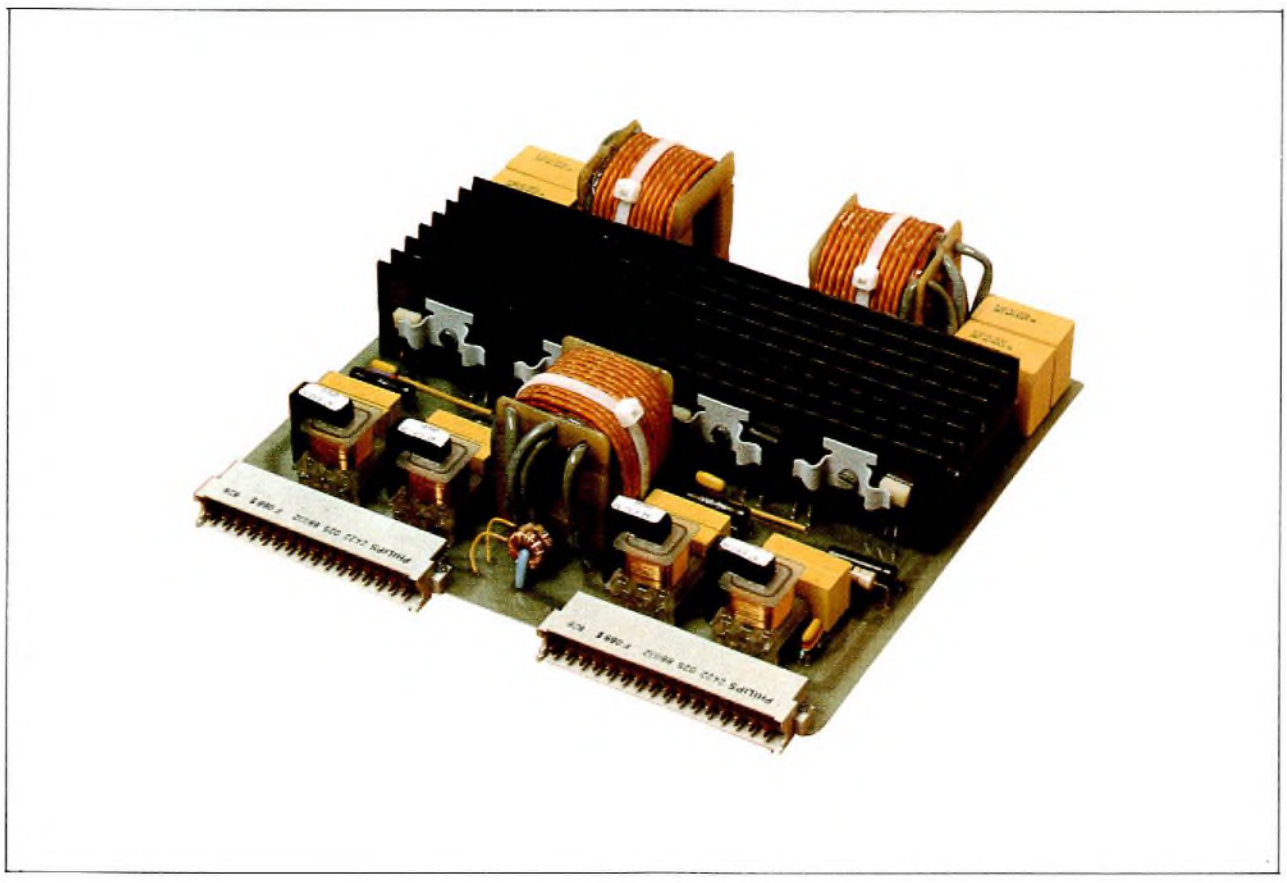

Fig.2 Single phase of typical inverter with thyristors clip-mounted on the heatsink

The triggering of the four thyristors in the phase is controlled by an external PWM IC, the trigger pulses being fed via isolating pulse transformers (not shown in Fig.1). A detailed description of the operation of this circuit is given in Ref.1.

INVERTER DESIGN EQUATIONS AND WORKED EXAMPLE

The design method described here is suitable for a wide range of motor sizes and voltages, but a worked example is given for an inverter suitable for driving a 4 kW 380 V motor.

The maximum voltage that the inverter can provide to the motor is determined by the mains supply voltage. In general, a motor may be used which has a rated voltage less than or equal to the mains supply voltage. For an a.c. supply voltage of V_{ac} line-to-line, the average d.c. line voltage of the three-phase rectified supply is given by:

$$V_{dc(nom)} \simeq V_{ac} \times \sqrt{2} \times \frac{3}{\pi}.$$

This allows an output fundamental r.m.s. voltage of:

$$V_{o(rms)} \leqslant 1.1 \times \frac{V_{dc(nom)}}{\sqrt{2}},$$

$$= 1.05\, V_{ac}$$

at maximum modulation (quasi-squarewave).

The design process falls into the following parts: inverter specification, selection of the main thyristors and diodes, commutation thyristors and diodes, passive commutation components, snubber and dI/dt components for damping and voltage-clipping circuits, and the selection of the heatsinks for the power semiconductors. A flowchart for the design process is given in Fig.3, and Table 1 gives a complete list of the symbols used in this article.

Input data

The following input data must be provided at the start of the inverter design exercise.

$V_{dc(min)}$. The lowest d.c. supply voltage at which correct commutation of peak inverter output current is required.

$V_{dc(nom)}$. The highest continuous value of d.c. supply voltage. This is used for calculating inverter losses.

$V_{dc(max)}$. The transient peak voltage to which the supply voltage is allowed to rise during regenerative braking.

$I_{m(max)}$. The maximum motor r.m.s. line current. This is determined by the required peak motor output power. The inverter must be rated for continuous $I_{m(max)}$, and not for the nominal motor current, since the thermal time-constants of the inverter semiconductors and heatsinks are considerably less than the thermal time-constants of the motor.

$f_{s(max)}$. The maximum required inverter switching frequency. The choice of this value depends on the trade-off between excessive motor ripple current and losses, which occur with low $f_{s(max)}$, and excessive inverter losses which occur with high $f_{s(max)}$. Typical values of $f_{s(max)}$ lie in the range 500 to 1500 Hz.

$T_{amb(max)}$. Maximum ambient air temperature. This is required for heatsink calculations.

Input data – example

$V_{dc(min)}$

Assuming a European three-phase mains supply, 380 V r.m.s. ±10%, then when rectified the minimum d.c. voltage at minimum a.c. supply voltage is given by:

$$V_{dc(min)} \simeq 380 \times 0.9 \times \sqrt{2} \times \frac{3}{\pi},$$

$$= 462\ V.$$

$V_{dc(nom)}$

The nominal continuous d.c. supply voltage is given approximately by:

$$V_{dc(nom)} \simeq 380 \times \sqrt{2} \times \frac{3}{\pi},$$

$$= 513\ V.$$

$V_{dc(max)}$

The peak d.c. supply voltage at maximum a.c. supply is obtained from the peak a.c. supply voltage $V_{ac(pk)}$. The value of $V_{ac(pk)}$ is given by:

$$V_{ac(pk)} \simeq 380 \times 1.1 \times \sqrt{2},$$

$$\simeq 591\ V.$$

Under regenerative braking conditions, the d.c. supply voltage rises above $V_{ac(pk)}$. Assuming a permitted rise of 150 V, then $V_{dc(max)}$ is given by:

$$V_{dc(max)} = 591 + 150,$$

$$\simeq 750\ V.$$

$I_{m(max)}$

Assume that a 4 kW 380 V motor is to be used at 50% transient overload. The nominal line current for such a motor varies between motor manufacturers, but the

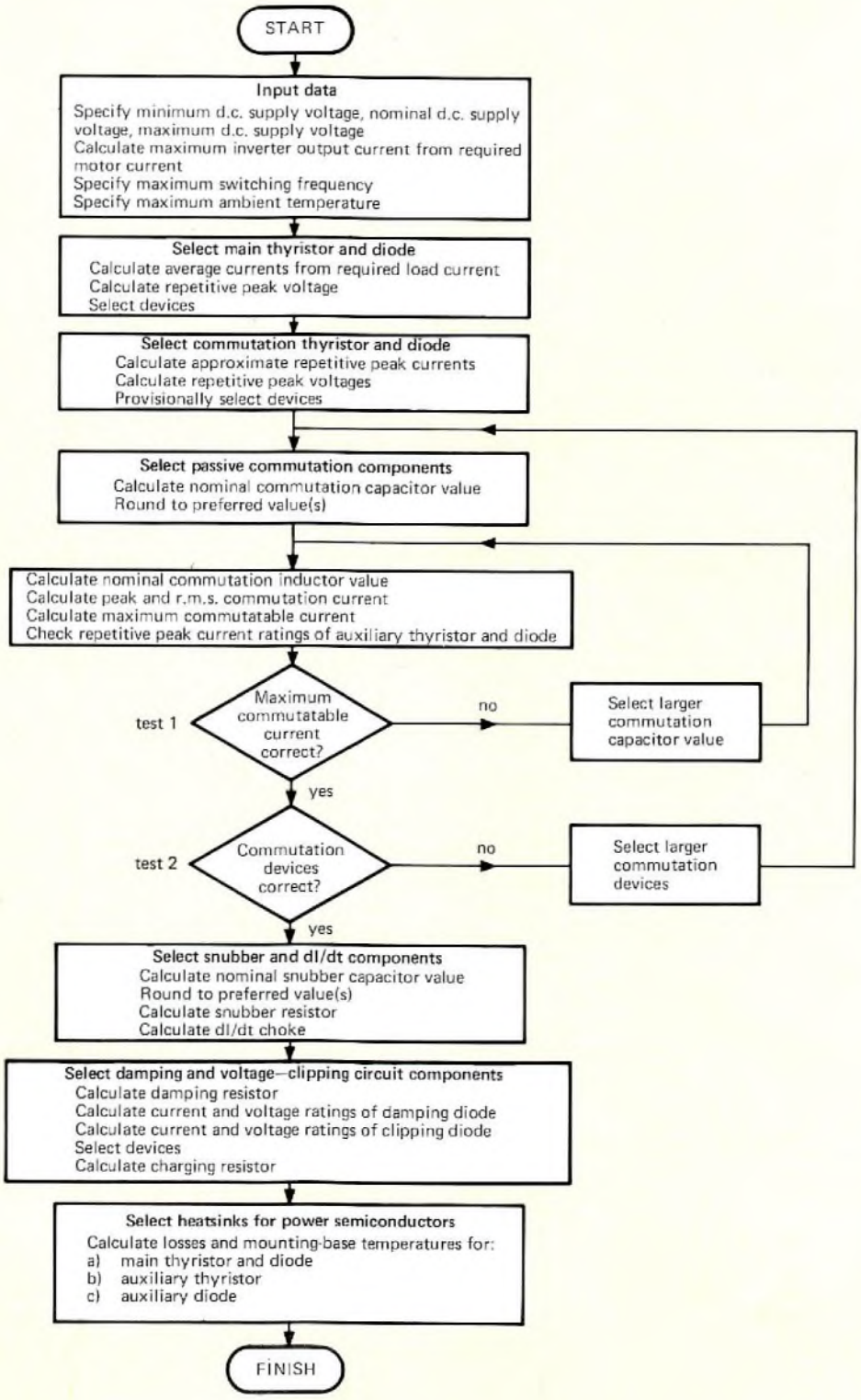

Fig.3 Flowchart of the design process

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TABLE 1 List of symbols

Symbol	Definition
a	form factor
C_3	snubber capacitor across auxiliary thyristor Th_3
C_5	rounded value of commutation capacitor of Th_1
$C_{5(min)}$	minimum value of commutation capacitor of Th_1
$C_{5(nom)}$	nominal value of commutation capacitor of Th_1
C_5'	optimum value of commutation capacitor of Th_1
D_5	damping diode for commutation circuit of Th_1
D_7	clipping diode for commutation circuit of Th_1
dI_T/dt	rate of rise of thyristor on-state current
dV_D/dt	rate of rise of thyristor off-state voltage
F_R	ripple factor of output current
$f_{s(max)}$	maximum inverter switching frequency
I_c	commutation current
$I_{c(pk)}$	peak commutation current
$I_{c(rms)}$	r.m.s. value of commutation current
I_D	rated leakage current of diode
$I_{F(av)}$	average forward current through diode
I_{FRM}	repetitive peak forward current through diode
$I_{m(max)}$	maximum r.m.s. value of motor line current
$I_{o(pk)}$	peak output current of inverter
I_s	current through snubber components
I_T	thyristor on-state current
$I_{T(av)}$	average forward current through thyristor
I_{TRM}	repetitive peak forward current through thyristor
$I_{T(rms)}$	r.m.s. on-state current through thyristor
L_1	optimum value of commutation inductor of Th_1
$L_{1(max)}$	maximum value of commutation inductor of Th_1
$L_{1(min)}$	minimum value of commutation inductor of Th_1
P_{off}	off-state power loss for thyristors and diodes
P_{on}	on-state power loss for thyristors and diodes
P_{R3}	power dissipated in snubber resistor R_3
P_{R6}	power dissipated in damping resistor R_6
P_{R7}	power dissipated in charging resistor R_7
P_{sw}	switching loss for thyristors and diodes
P_{tot}	total power loss for thyristors and diodes
R_3	snubber resistance across auxiliary thyristor Th_3
R_6	damping resistor for commutation circuit of Th_1
R_7	charging resistor for commutation circuit of Th_1
$R_{th(h-a)}$	thermal resistance of heatsink
$R_{th(j-h)}$	thermal resistance between junction and heatsink
$R_{th(j-mb)}$	thermal resistance between junction and mounting-base
$R_{th(mb-h)}$	thermal resistance between mounting-base and heatsink
r_F	diode forward current slope resistance
r_T	thyristor forward current slope resistance
$T_{amb(max)}$	maximum ambient air temperature
T_h	temperature of heatsink
$T_{j(max)}$	maximum junction temperature for thyristors and diodes
T_{mb}	temperature of mounting-base
t_q	thyristor turn-off time
$t_{q(A)}$	auxiliary thyristor turn-off time (as defined in Fig.5)
$t_{q(M)}$	main thyristor turn-off time (as defined in Fig.4)
t_{rr}	diode reverse-recovery time
V_{ac}	a.c. supply voltage
$V_{ac(pk)}$	peak a.c. supply voltage
V_{ak}	thyristor anode-to-cathode voltage
$V_{(BR)R}$	diode reverse breakdown voltage
$V_{dc(max)}$	transient peak value of d.c. supply voltage
$V_{dc(min)}$	minimum value of d.c. supply voltage
$V_{dc(nom)}$	highest continuous value of d.c. supply voltage
V_{DRM}	repetitive peak off-state forward voltage across thyristor
$V_{F(0)}$	diode forward-current knee voltage
$V_{o(rms)}$	output fundamental r.m.s. voltage
V_R	maximum continuous reverse voltage of diode
V_{RRM}	repetitive peak reverse voltage across diode
V_s	voltage across snubber components
$V_{T(0)}$	thyristor forward-current knee voltage
$\Delta T_{(h-a)}$	temperature difference between heatsink and air

worst-case value is about 9.3 A r.m.s. Assuming 50% overload, $I_{m(max)}$ is therefore given by:

$$I_{m(max)} = 9.3 \times 1.5,$$

$$= 14 \text{ A r.m.s.}$$

$f_{s(max)}$

If the PWM IC HEF4752V is used to produce trigger-pulses for the inverter, then the number of inverter output pulses per motor line current fundamental period is one of the series 15, 21, 30 . . . . . 168, (see Ref.1). At maximum modulation, which, for 50 Hz rated motors, occurs when the fundamental frequency of the motor line current is in the range 42 to 45 Hz, the number of pulses per period will be either 15 or 21. The value of $f_{s(max)}$ is taken to be 1 kHz, and therefore the inverter switching frequency at maximum modulation is 45 × 21 = 945 Hz.

$T_{amb(max)}$

For this example, the maximum temperature is assumed to be 50°C.

Selection of main thyristor and diode

The main thyristor and diode are selected initially on the basis of current ratings $I_{T(av)}$ and $I_{F(av)}$ respectively, and peak voltage ratings V_{DRM} and V_{RRM}. For the voltage ratings, a safe design figure is:

$$\text{main thyristor } V_{DRM} = \text{main diode } V_{RRM} =$$

$$= V_{dc(max)} + 50. \qquad (1)$$

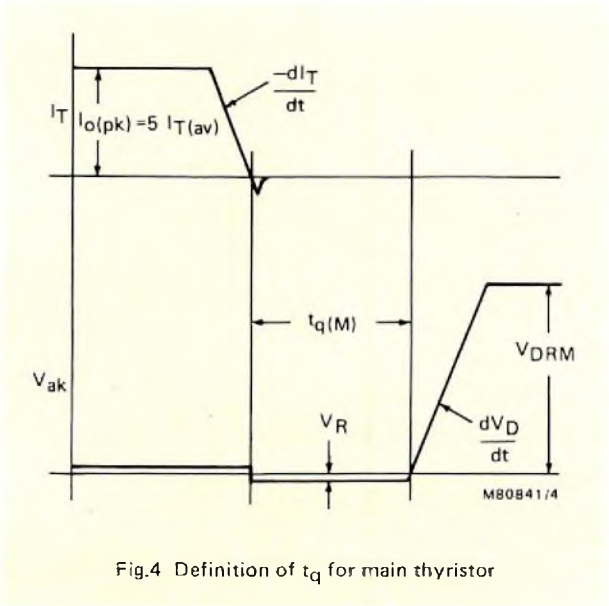

Fig.4 Definition of t_q for main thyristor

For the current ratings, we can assume that the worst-case thyristor current is approximated by a half-wave rectified sinewave, so that:

$$I_{T(av)} \simeq I_{m(max)} \times \frac{\sqrt{2}}{\pi}. \qquad (2)$$

The average diode current $I_{F(av)}$ is also given by Eq.2. However, whereas the repetitive peak current of the thyristor is the peak load current, the repetitive peak current of the diode is the sum of the peak load current and the peak commutation current at maximum supply voltage.

The following approximations can be used until the commutation circuit has been designed, when more accurate values may be calculated to check the selection of the main thyristor and diode:

$$I_{TRM} \simeq 5 \times I_{T(av)} \qquad (3)$$

for the main thyristor, and:

$$I_{FRM} \simeq 20 \times I_{T(av)} \qquad (4)$$

for the main diode. The choice of main thyristor is also restricted by the limits on the turn-off time t_q, and the post-commutation rate-of-rise of reapplied voltage dV_D/dt. It is an advantage to have t_q as short as possible to minimise the size of the commutation components, and dV_D/dt as high as possible to minimise the losses in the snubber circuits.

If the value of t_q published in the data is to be used in the commutation circuit design, then it must be specified under the correct conditions. These include turning off from I_{TRM} (approximately $5 \times I_{T(av)}$) at a high dI_T/dt, applying only a small reverse blocking voltage V_R (the forward voltage drop of one diode), and with a high reapplied dV_D/dt after t_q, see Fig.4. In the rest of this article, the main thyristor turn-off time measured under these conditions is denoted by $t_{q(M)}$. The diode must be of the fast soft-recovery type.

Selection of main thyristor and diode – example

From Eq.1:

$$\text{thyristor } V_{DRM} = \text{diode } V_{RRM} = 750 + 50,$$

$$= 800 \text{ V}.$$

From Eq.2:

$$I_{F(av)} \simeq I_{T(av)} \simeq 14 \times \frac{\sqrt{2}}{\pi},$$

$$= 6.3 \text{ A}.$$

From Eqs.3 and 4:

$$I_{TRM} \simeq 5 \times 6.3 = 32 \text{ A};$$

$$I_{FRM} \simeq 20 \times 6.3 = 126 \text{ A}.$$

A good thyristor for this application, chosen from our range of fast high-voltage types, is the BT155N. This has a $t_{q(M)}$ of 9 μs, measured under the correct current conditions, and a dV_D/dt of 500 V/μs. A suitable diode is the BYW19-1000. This has the correct $I_{F(av)}$ and I_{FRM}, and is of the fast soft-recovery type with t_{rr} = 450 ns.

Selection of commutation thyristor and diode

The selection of the commutation thyristor and diode depends chiefly on V_{DRM}, V_{RRM}, I_{TRM}, and I_{FRM}. The voltage ratings V_{DRM} and V_{RRM} are the same as those of the main thyristor and diode, see Eq.1. I_{TRM} is the peak of the first half-cycle of the commutation current, and I_{FRM} is the peak of the second half-cycle of the commutation current. Until the design of the commutation circuit is complete, approximate values of I_{TRM} and I_{FRM} may be obtained by considering the commutation circuit design in terms of the inverter peak output current $I_{o(pk)}$. If the motor line current were a perfect sinewave, r.m.s. value $I_{m(max)}$, the peak inverter output current would be $\sqrt{2} \times I_{m(max)}$. However, because of the finite switching frequency of the inverter, the sinewave has a ripple current superimposed, so that:

$$I_{o(pk)} = I_{m(max)} F_R \sqrt{2}, \qquad (5)$$

where F_R is a ripple factor, typical value 1.4.

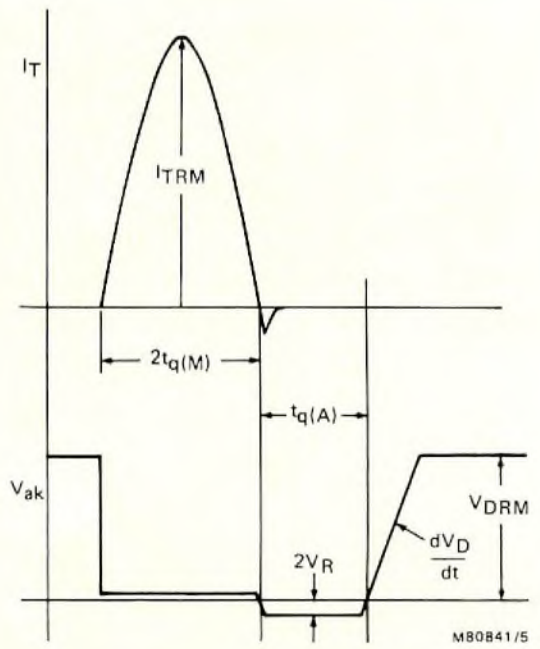

Fig.5 Definition of t_q for commutation thyristor

It can then be shown that for commutation components having ±10% tolerances, an accurate estimate of the repetitive peak current is:

$$I_{TRM} \simeq 2.0 \times I_{o(pk)} \times \frac{V_{dc(max)}}{V_{dc(min)}} \qquad (6)$$

for the thyristor, and:

$$I_{FRM} \simeq 1.8 \times I_{o(pk)} \times \frac{V_{dc(max)}}{V_{dc(min)}} \qquad (7)$$

for the diode.

The auxiliary thyristor turn-off time $t_{q(A)}$ is given by:

$$t_{q(A)} \leqslant 1.5\, t_{q(M)}. \qquad (8)$$

The value of $t_{q(A)}$ should be measured under the conditions shown in Fig.5; that is, with a current pulse having a width of $2t_{q(M)}$ and a peak value of I_{TRM}, and with a rate of rise of reapplied voltage dV_D/dt the same as that of the main thyristor. The auxiliary diode must again be a fast soft-recovery type.

Selection of commutation thyristor and diode – example

From Eq.5, and assuming F_R = 1.4:

$$I_{o(pk)} = 14 \times 1.4 \times \sqrt{2},$$
$$= 27.7 \text{ A}.$$

From Eq.6:

$$I_{TRM} \simeq 2.0 \times 27.7 \times \frac{750}{462},$$
$$= 90 \text{ A}.$$

From Eq.7:

$$I_{FRM} \simeq 1.8 \times 27.7 \times \frac{750}{462},$$
$$= 81 \text{ A}.$$

From Eq.8:

$$t_{q(A)} \leqslant 1.5 \times 9,$$
$$\leqslant 13.5\ \mu\text{s}.$$

As in the case of the main thyristor and diode, V_{DRM} and V_{RRM} are both 800 V.

A good choice of thyristor for this application would be the BT155P, and a good choice of diode, the BYW19-1000.

Selection of passive commutation components

Both main thyristors will have identical commutation circuits. The equations formulated in this section are for Th_1.

The commutation current waveform is approximately one cycle of a damped sinewave; see Fig.6. The second

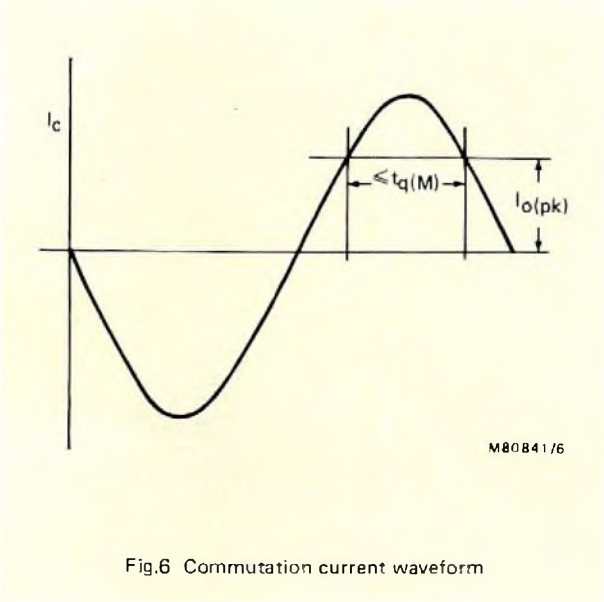

Fig.6 Commutation current waveform

half-cycle must support the load current for a time greater than the main thyristor turn-off time $t_{q(M)}$ under the worst-case combination of d.c. supply voltage, load current, component tolerances, and commutation circuit losses.

The worst-case supply voltage and load current are $V_{dc(min)}$ and $I_{o(pk)}$ respectively. A typical value of the commutation circuit Q-factor might be 20, and we will assume a worst-case value of Q = 15. The worst-case condition for the commutation capacitor is the smallest value that the capacitor can take. For a capacitor with a nominal value $C_{5(nom)}$ and ±10% tolerance, a value of $C_{5(min)} = 0.9\ C_{5(nom)}$ should therefore be assumed in the calculations. The effect of the tolerance on the value of the commutation inductor is shown in Fig.7. Commutation component values are minimised if correct commutation is just obtained at both maximum and minimum tolerances on the inductor. That is, the two current curves in Fig.7 for $C_{5(min)}$, $L_{1(min)}$ and $C_{5(min)}$, $L_{1(max)}$ both pass through the corners of the rectangle defined by $I_{o(pk)}$ and $t_{q(M)}$.

Assuming commutation component tolerances to be ±10%, and the commutation circuit Q-factor (including losses in the semiconductors) to be 15, it can be shown that the optimum capacitor value C_5' is given by:

$$C_5' \simeq 1.2 \times \frac{I_{o(pk)} \times t_{q(M)}}{V_{dc(min)}} \pm 10\%. \qquad (9)$$

A suitable capacitor, or combination of capacitors, should be chosen from a range which can handle high peak and high r.m.s. currents and voltages. Suitable capacitors are film-foil types such as those from our 357 series. If rounding of the value of C_5' is necessary, it should preferably be rounded up. If downward rounding is necessary, then this should be by one or two percent only.

The optimum inductor value L_1 is given by:

$$L_1 \simeq 0.32 \times V_{dc(min)} \times \frac{t_{q(M)}}{I_{o(pk)}}, \qquad (10)$$

and if the rounded value of C_5' is denoted by C_5 then:

$$I_{c(pk)} \simeq 1.1 \times V_{dc(max)} \sqrt{\left(\frac{C_5}{L_1}\right)}, \qquad (11)$$

and the r.m.s. commutation current is given by:

$$I_{c(rms)} \simeq 1.6 \times V_{dc(nom)} \sqrt[4]{\left(\frac{C_5^3}{L_1}\right)} \times \sqrt{(f_{s(max)})}. \qquad (12)$$

Note that the $I_{c(pk)}$ value, defined by Eq.11, gives a more accurate value of I_{TRM} for the commutation thyristor than does the approximation of Eq.6. If the commutation thyristor selected from Eq.6 does not have sufficient I_{TRM}, then a device with a higher I_{TRM} characteristic must be used (see test 2 in Fig.3).

The capacitor peak-to-peak voltage is $2\ V_{dc(max)}$, and the r.m.s. voltage is $V_{dc(nom)}$. The actual peak output current which can be commutated is given by the smaller of the following two values:

$$I_{o(pk)} = 0.855 \times V_{dc(min)} \cos\left\{\frac{t_{q(M)}}{1.8\sqrt{(L_1 C_5)}}\right\}\sqrt{\left(\frac{C_5}{L_1}\right)},$$

or: (13)

$$I_{o(pk)} = 0.769 \times V_{dc(min)} \cos\left\{\frac{t_{q(M)}}{1.98\sqrt{(L_1 C_5)}}\right\}\sqrt{\left(\frac{C_5}{L_1}\right)}.$$

Should the peak commutatable current be insufficient, a larger commutation capacitor will be required (see test 1 in Fig.3).

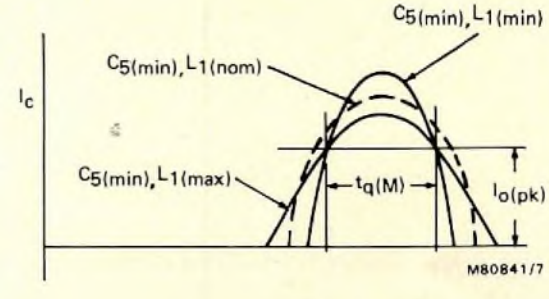

Fig.7 Effect of inductor tolerances on second half-cycle of commutation current

Selection of passive commutation components – example

For the BT155N thyristor, with $t_{q(M)} = 9\ \mu s$, we have from Eq.9:

$$C_5' \simeq \frac{1.2 \times 27.7 \times 9 \times 10^{-6}}{462}\ F,$$

$$= 0.647\ \mu F \pm 10\%.$$

A possible combination of preferred values might be three 0.15 μF capacitors in parallel with two 0.1 μF capacitors, giving $C_5 = 0.65\ \mu F$. With a peak-to-peak voltage of 1500 V and an r.m.s. voltage of 513 V, suitable types would be the 357 81154 and the 357 81104, both from our range of 1500 V d.c. film-foil capacitors.

From Eq.10:

$$L_1 \simeq 0.32 \times 462 \times \frac{9 \times 10^{-6}}{27.7}\ H,$$

$$= 48\ \mu H \pm 10\%.$$

From Eq.11:

$$I_{c(pk)} \simeq 1.1 \times 750 \sqrt{\left(\frac{0.65}{48}\right)},$$

$$= 96\ A,$$

and from Eq.12:

$$I_{c(rms)} \simeq 1.6 \times 513 \sqrt[4]{\left\{\frac{(0.65 \times 10^{-6})^3}{48 \times 10^{-6}}\right\}} \times \sqrt{1000},$$

$$= 7.1\ A\ r.m.s.$$

From Eq.13 the peak commutatable current is given by:

$$I_{o(pk)} = 0.855 \times 462 \times \cos\left\{\frac{9}{1.8\sqrt{(48 \times 0.65)}}\right\} \times \times \sqrt{\left(\frac{0.65}{48}\right)},$$

or

$$I_{o(pk)} = 0.769 \times 462 \times \cos\left\{\frac{9}{1.98\sqrt{(48 \times 0.65)}}\right\} \times \times \sqrt{\left(\frac{0.65}{48}\right)},$$

$$= 28.4\ A,$$

which is more than the initial required value of 27.7 A.

Selection of snubber and dI/dt components

The RC snubber connected across each auxiliary thyristor forms a damped resonant circuit with the commutation components. During the time interval in which the V_{ak} of the auxiliary thyristor is rising, the equivalent circuit of the snubber can be represented as shown in Fig.8, where the component numbers are identical to the component numbers in Fig.1. Voltage V_s is the voltage across the snubber, which is the V_{ak} of the thyristor.

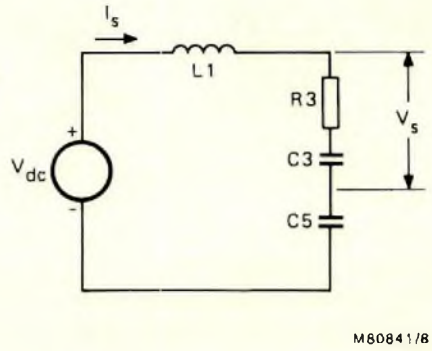

Fig.8 Equivalent circuit during snubber operation

The initial conditions for the circuit of Fig.8 may be taken as $V_s = 0$, $I_s = 0$. By solving the circuit equations, dV_s/dt can be found as a function of time. For a given snubber capacitor C_3, we can then calculate the value of R_3 for which dV_s/dt is minimised.

Putting parameter $X = R_3 \sqrt{\left\{\frac{C_3 C_5}{L_1(C_3 + C_5)}\right\}}$,

it can be shown that dV/dt is minimised for X = 0.53, when:

$$\left.\frac{dV_s}{dt}\right|_{max} \simeq 0.9 \times V_{dc} \sqrt{\left(\frac{C_3 + C_5}{L_1 C_3 C_5}\right)},$$

assuming ±10% tolerance on all components.

The value of C_3 to give the required maximum dV_s/dt at maximum supply voltage may thus be obtained from:

$$\frac{C_3 C_5}{C_3 + C_5} \simeq 0.81 \times \frac{V^2_{dc(max)}}{L_1 \left(\frac{dV_s}{dt}\right)^2}. \qquad (14)$$

and we have, for X = 0.53:

$$R_3 \simeq 0.53 \sqrt{\left\{\frac{L_1(C_3 + C_5)}{C_3 C_5}\right\}}. \qquad (15)$$

As in the case of C_5, any rounding of C_3 should preferably be in the upward direction.

The peak voltage on the snubber capacitor is approximately $V_{dc(max)}$, and the d.c. voltage is $V_{dc(nom)}$. The maximum possible power dissipated in the snubber resistor is given by:

$$P_{R3} \simeq C_3 V^2_{dc(nom)} f_{s(max)}. \qquad (16)$$

In the case of the snubbers across the main thyristor, the inductor L_1 in the circuit of Fig.8 is replaced by the dI/dt-limiting inductor L_3 in Fig.1. This inductor limits

the rate of rise of on-state current when the load current commutates from one main diode to the opposite main thyristor. If this dI/dt choke is made equal in value to the commutation choke L_1, and the main thyristor snubbers are the same as the auxiliary thyristor snubbers, then all four thyristors in the phase will have the same dI/dt and reapplied post-commutation dV_D/dt. The r.m.s. current in the dI/dt choke is rather higher than in the commutation choke, but at a lower frequency; the peak current in the dI/dt choke is rather less than in the commutation choke. In many applications, it is more economic to use identical designs for both the dI/dt and commutation chokes.

The reverse recovery currents of the main and auxiliary diodes can put an initial value of I_s into the equivalent circuit shown in Fig.8. This produces a reapplied voltage which has an initial rate-of-rise greater than the design value. However, the reverse-recovery time t_{rr} of the fast diodes is typically only half the total voltage rise time, so that the reverse recovery only affects the dV/dt at lower voltages, where the thyristors are less sensitive to dV/dt.

Selection of snubber and dI/dt components — example

For the BT155N and BT155P thyristors, characterised at a reapplied dV_D/dt of 500 V/μs, we have from Eq.14:

$$\frac{C_3C_5}{C_3+C_5} \simeq \frac{0.81 \times 750^2}{48 \times 10^{-6} \times (500 \times 10^6)^2}\ \text{F},$$

$$= 38.0\ \text{nF}.$$

With $C_5 = 0.65\ \mu\text{F}$, then:

$$C_3 = \frac{650 \times 38.0}{650 - 38.0}\ \text{F},$$

$$= 40\ \text{nF} \pm 10\%.$$

The suggested value is therefore $C_3 = 47$ nF. With a peak-to-peak voltage of 750 V and a d.c. voltage of 513 V, a capacitor from our 357 series 1000 V range should be chosen. Type 357 71473 would be suitable.

From Eq.15:

$$R_3 = 0.53 \times \sqrt{\left(\frac{48 \times 10^{-6}}{38 \times 10^{-9}}\right)},$$

$$= 19\ \Omega:$$

and from Eq.16:

$$P_{R3} \simeq 47 \times 10^{-9} \times 513^2 \times 1000,$$

$$= 12.4\text{W},$$

so that R_3 might be rated at 18 Ω 15 W.

These values of R_3 and C_3 apply to all four snubbers in each phase. The dI/dt choke is the same as the commutation choke; see Eq.10.

Selection of components for damping and voltage clipping circuits.

An equivalent circuit for the inverter when the snubber capacitors have just reached full charge after commutation is shown in Fig.9. The load current I_o flows in the auxiliary diode D_3. At the end of commutation, the inductor L_1 was left carrying this load current. Without damping, this energy would be transferred to the commutation capacitor C_5, causing it to be charged to a voltage higher than the d.c. supply. To prevent this, the commutation circuit is critically damped by the resistor R_6 and the diode D_5 shown in Fig.9. The diode is connected to the centre-tap of the choke so that it receives a peak reverse voltage equal to 1.5 times the d.c. supply, while the junction of C_5 and L_1 rises to twice the d.c. supply.

For critical damping, taking into account the turns ratio between the two halves of L_1, we have:

$$R_6 \simeq 0.5 \times \sqrt{\left(\frac{L_1}{C_5}\right)}. \qquad (17)$$

The current waveform in D_5 and R_6 takes the form of a pulse after each commutation is completed. If the pulse is assumed to be a half-sinewave, the following approximations are obtained:

$$P_{R6} \simeq 0.03 \times C_5 \times V^2_{dc(nom)} \times f_{s(max)} \qquad (18)$$

for the loss in R_6, and:

$$I_{FRM} \simeq I_{o(pk)} \sqrt{2}, \qquad (19)$$

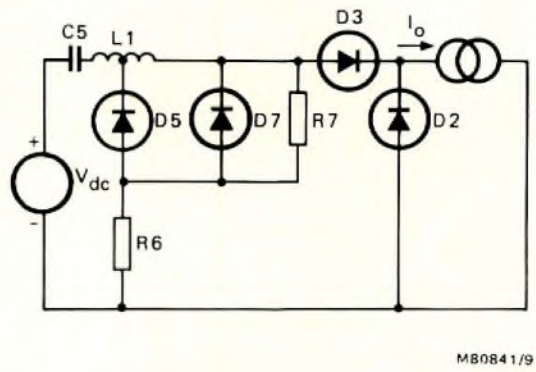

Fig.9 Equivalent circuit after commutation

$$I_{F(av)} \simeq 2\sqrt{2} \times I_{o(pk)} \times \sqrt{(L_1 C_5)} \times f_{s(max)}. \quad (20)$$

$$V_{RRM} \simeq 1.5\, V_{dc(max)}. \quad (21)$$

for the damping diode D_5.

In addition to the damping diode, in applications where the V_{DRM} of the auxiliary thyristors is a limiting parameter, the peak voltage on the auxiliary thyristors may be clipped by the addition of the diode D_7 in Fig.9. This removes the voltage transient caused by the reverse recovery of the auxiliary diode D_3. Diode D_7 may be rated as follows:

$$I_{FRM} \simeq 0.5 \times \frac{V_{dc(max)} \times t_{rr}}{L_1}. \quad (22)$$

$I_{F(av)}$ is very small, and:

$$V_{DRM} \simeq V_{dc(max)} + 50\ V. \quad (23)$$

The last component in the circuit is a high-value resistor R_7, in parallel with D_5 or D_7. This ensures that the commutation capacitors are charged on first applying voltage to the d.c. supply. A suitable time-constant for the charging of the commutation capacitor is in the range 0.1 to 0.5 s.

Selection of components for damping and voltage clipping circuits – example

The value of the damping resistor R_6 is given by Eq.17:

$$R_6 \simeq 0.5 \times \sqrt{\left(\frac{48 \times 10^{-6}}{0.65 \times 10^{-6}}\right)},$$

$$= 4.3\ \Omega.$$

From Eq.18:

$$P_{R6} \simeq 0.3 \times 0.65 \times 10^{-6} \times 513^2 \times 1000,$$

$$= 5.1\ W.$$

Thus a 4.3 Ω 6 W or a 3.9 Ω 6 W resistor should be used.

For the damping diode D_5, we have from Eq.19:

$$I_{FRM} \simeq 27.2\sqrt{2} = 39\ A;$$

from Eq.20:

$$I_{F(av)} \simeq 2\sqrt{2} \times 27.7 \times \sqrt{(48 \times 10^{-6} \times 0.65 \times 10^{-6})} \times 1000,$$

$$= 0.44\ A;$$

and from Eq.21:

$$V_{RRM} = 1.5 \times 750 = 1125\ V.$$

A possible choice for the damping diode D_5 is therefore the BYW56. This has $I_{FRM} = 50$ A, $I_{F(av)} = 2$ A, and a controlled avalanche breakdown $V_{(BR)R}$ between 1100 V and 1600 V.

For the voltage clipping diode D_7, we have from Eq.22:

$$I_{FRM} \simeq 0.5 \times \frac{750 \times 450 \times 10^{-9}}{48 \times 10^{-6}},$$

$$= 3.5\ A;$$

and from Eq.23:

$$V_{DRM} = 750 + 50 = 800\ V.$$

A BYW55 or BYW56 diode is therefore suitable.

The value of the charging resistor R_7 is determined from the time-constant and the value of the commutation capacitor:

$$R_7 = \frac{0.1}{0.65 \times 10^{-6}}\ \Omega,$$

$$= 153\ k\Omega,$$

so that a 150 kΩ resistor is used; and

$$P_{R7} = \frac{513^2}{150 \times 10^3},$$

$$= 1.8\ W.$$

Selection of heatsinks for power semiconductors

The devices in the inverter which require heatsinks are the main thyristor, main diode, auxiliary thyristor, and auxiliary diode. If the devices can be isolated from the heatsinks, then there are no restrictions on the number of devices which can share a common heatsink. If the devices cannot be isolated, then the circuit imposes restrictions on the minimum number of heatsinks which must be used. Each main thyristor can share a heatsink with its anti-parallel main diode. Each auxiliary device is assumed to have its own heatsink.

Because the main thyristor and main diode cannot conduct simultaneously, the main heatsink need only be rated for the maximum thyristor loss. This is true partly because the $T_{j(max)}$ of the thyristors is generally less than the $T_{j(max)}$ of the diodes.

To design the main heatsink, the various contributions to the main thyristor loss must be calculated. The largest contribution is the on-state loss. The thyristor worst-case current waveform can be considered to be a half-wave rectified sinewave, with an average value given by Eq.2:

$$I_{T(av)} \simeq I_{m(max)} \times \frac{\sqrt{2}}{\pi}.$$

and an r.m.s. value:

$$I_{T(rms)} \simeq \frac{I_{m(max)}}{\sqrt{2}}. \quad (24)$$

The form factor of the worst-case current waveform is therefore:

$$a = \frac{I_{T(rms)}}{I_{T(av)}} = \frac{\pi}{2}.$$

If the device published data includes a power loss curve (which will include the off-state losses), then the form factor may be used to determine the power loss. Otherwise, the I_T/V_T characteristics may be approximated by a straight line with a 'knee' voltage $V_{T(O)}$ and a slope resistance r_T. Then the on-state loss is given by:

$$P_{on} \simeq V_{T(O)} \times I_{T(av)} + r_T \times I^2_{T(rms)}; \quad (25)$$

and the off-state loss is given by:

$$P_{off} \simeq 0.5 \times V_{dc(nom)} \times I_D,$$

where I_D is the rated leakage current of the device at $T_{j(max)}$.

The third contribution is the turn-on switching loss P_{sw}. In some cases the device data contains a turn-on loss nomogram which may be used to determine P_{sw}. The dI/dt used in the nomogram is approximately $V_{dc(nom)}/L_1$. Where a nomogram is not given, the switching loss must be estimated as a fraction, typically 15%, of the on-state loss. For switching frequencies of the order of 1 kHz, this is a reasonable approximation.

The total power loss is:

$$P_{tot} = P_{on} + P_{off} + P_{sw},$$

and given the thermal resistance of the device from junction to heatsink (including the preferred mounting method), the rated $T_{j(max)}$ of the thyristor, and the desired maximum ambient air temperature $T_{amb(max)}$, then the temperature difference between the heatsink and the ambient air temperature may be determined from:

$$\Delta T_{(h\text{-}a)} = T_{j(max)} - P_{tot} \times R_{th(j\text{-}h)} - T_{amb(max)}. \quad (26)$$

The required thermal resistance of the heatsink is then given by:

$$R_{th(h\text{-}a)} = \frac{\Delta T_{(h\text{-}a)}}{P_{tot}}. \quad (27)$$

Once the heatsink temperature, $T_{j(max)} - P_{tot} \times R_{th(j\text{-}h)}$, has been calculated, the junction temperature of the diode may be checked to ensure that it does not exceed $T_{j(max)}$.

The other devices needing heatsinks are the auxiliary thyristors and diodes. The auxiliary thyristor current waveform consists of half-sinewave pulses at a low duty cycle, with:

$$I_{T(av)} \simeq 1.9 \times V_{dc(nom)} \times C_5 \times f_{s(max)}, \quad (28)$$

and:

$$I_{T(rms)} \simeq 1.2 \times V_{dc(nom)} \sqrt[4]{\left(\frac{C_5^3}{L_1}\right)} \times \sqrt{(f_{s(max)})}, \quad (29)$$

giving a form factor:

$$a = \frac{0.63}{\sqrt[4]{(L_1 C_5 f^2_{s(max)})}}.$$

This auxiliary thyristor form factor is usually much larger than the values used as parameters in the power dissipation curves in published data. The power dissipation must therefore be found from the device I_T/V_T curve or by calculating the knee voltage $V_{T(O)}$ and slope resistance r_T from the power dissipation curve at lower form factors. The on-state loss can then be calculated as for the main thyristors.

As the device spends most of the time blocking forward voltage, the off-state current losses are given approximately by:

$$P_{off} \simeq V_{dc(min)} \times I_D. \quad (30)$$

Switching losses may again be found from the nomogram in published data or by estimation; a reasonable value is 50 to 150% of the on-loss P_{on}.

The auxiliary diode waveform is similar to that of the auxiliary thyristor:

$$I_{F(av)} \simeq 1.7 \times V_{dc(nom)} \times C_5 \times f_{s(max)}, \quad (31)$$

and:

$$I_{F(rms)} \simeq 1.1 \times V_{dc(nom)} \sqrt[4]{\left(\frac{C_5^3}{L_1}\right)} \times \sqrt{\{f_{s(max)}\}}. \quad (32)$$

and has the same form factor as the auxiliary thyristor. Losses for the auxiliary diode may therefore be calculated by the same method as that used for the auxiliary thyristor, except that the off-state losses must be multiplied by a factor of 0.5.

Selection of heatsinks for power semiconductors – example

For the main thyristor, we have from Eqs.2 and 24:

$$I_{T(av)} \simeq 14 \times \frac{\sqrt{2}}{\pi} = 6.3 \text{ A};$$

and:

$$I_{T(rms)} \simeq \frac{14}{\sqrt{2}} = 9.9 \text{ A}.$$

The form factor is therefore:

$$a = \frac{9.9}{6.3} = 1.57.$$

From the BT155 published data, this gives a loss, including off-state losses, of 11 W. The switching loss is estimated at 1.5 W, 15% of the on-state loss, giving $P_{tot} \simeq 12.5$ W.

From data, $T_{j(max)} = 110°C$, $R_{th(j\text{-}mb)} = 2.0°C/W$, $R_{th(mb\text{-}h)} = 0.3°C/W$ (with heatsink compound and no insulation), and therefore assuming $T_{amb(max)} = 50°C$, we have from Eq.26:

$$\Delta T_{(h\text{-}a)} = 110 - (2.3 \times 12.5) - 50,$$

$$= 31°C;$$

and from Eq.27:

$$R_{th(h\text{-}a)} = \frac{31}{12.5},$$

$$= 2.5°C/W.$$

We can now check the junction temperature of the diode. For the same current the BYW19 loss is 10.1 W, so that with switching (reverse-recovery) losses estimated at 1 W, $P_{tot} = 11$ W. BWY19 data gives $R_{th(j\text{-}mb)} = 4.5°C/W$ and $R_{th(mb\text{-}h)} = 1.5°C/W$. The maximum value of T_h is 50 + 31 = 81°C, so that the maximum junction temperature that the diode can reach is 81 + 11 × 6 = 147°C. This is less than the $T_{j(max)}$ of 150°C quoted in the data, so that the heatsink design is satisfactory.

For the auxiliary thyristor, we have from Eqs.28 and 29:

$$I_{T(av)} \simeq 1.9 \times 513 \times 0.65 \times 10^{-6} \times 1000,$$

$$= 0.63 \text{ A};$$

and:

$$I_{T(rms)} \simeq 1.2 \times 513 \times \sqrt[4]{\left\{\frac{(0.65 \times 10^{-6})^3}{48 \times 10^{-6}}\right\}} \times \sqrt{(1000)},$$

$$= 5.35 \text{ A}.$$

The form factor is therefore:

$$a = \frac{5.35}{0.63} = 8.5,$$

which is not on the power loss curve in the published data.

From the $P_{tot}/I_{T(av)}$ curve for a = 1.1, $V_{T(O)}$ is estimated at 1.3 V and r_T at 30 mΩ. From Eq.25, this gives:

$$P_{on} \simeq (1.3 \times 0.63) + (0.03 \times 5.35^2).$$

$$= 1.68 \text{ W}.$$

From Eq.30, with rated leakage current of 1.5 mA:

$$P_{off} \simeq 513 \times 1.5 \times 10^{-3} = 0.8 \text{ W};$$

and P_{sw} may be estimated at 1.5 W. The total power loss P_{tot} is therefore 4.0 W.

Using $T_{j(max)}$, $T_{amb(max)}$, and $R_{th(j\text{-}h)}$ as above, we obtain:

$$\Delta T_{(h\text{-}a)} = 51°C,$$

and therefore:

$$R_{th(h\text{-}a)} = 12.8°C/W.$$

From Eqs.31 and 32 the auxiliary diode currents are:

$$I_{F(av)} = 0.57 \text{ A},$$

$$I_{F(rms)} = 4.9 \text{ A}.$$

From the $P/I_{F(av)}$ curve in the BYW19 data, for a form factor a = 1.57, we can estimate:

$$V_{F(0)} = 1 \text{ V and } r_F = 40 \text{ m}\Omega.$$

Thus the forward dissipation is:

$$P_{on} = (1.0 \times 0.57) + (0.04 \times 4.9^2) = 1.5 \text{ W};$$

and:

$$P_{off} = 0.5 \times 513 \times 0.6 \times 10^{-3} = 0.15 \text{ W}.$$

Reverse-recovery losses at $dI/dt = 513/(48 \times 10^{-6})$, that is 11 A/μs, are from the nomogram about 0.2 W. Thus the total loss $P_{tot} = 1.85$ W.

Using the published $T_{j(max)} = 150°C$, $R_{th(j\text{-}mb)} = 4.5°C/W$, and $R_{th(mb\text{-}h)} = 1.5°C/W$, then:

$$T_{mb} = 150 - 1.85 \times 4.5 = 141.7°C.$$

This is higher than the published data maximum mounting-base temperature of 125°C, so that for $P_{tot} = 1.85$ W, we must use:

$$\Delta T_{(mb\text{-}a)} = 125 - 50 = 75°C,$$

giving:

$$R_{th(mb\text{-}a)} = 40.5°C/W.$$

Therefore:

$$R_{th(h\text{-}a)} = 39°C/W.$$

The next article in this series will describe the purpose-built PWM LSI circuit.

REFERENCE

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Mains pollution caused by domestic appliances

Part 3 - Voltage fluctuation and flicker

H. W. EVERS

Perceptible changes in electric light intensity are known as *flicker*. These changes, the result of voltage fluctuation of the mains due to load switching, can give rise to irritation.

In this article we shall consider flicker both from an annoyance and from an electrical viewpoint. We shall also consider the recommendations of CENELEC (European Committee for Electrotechnical Stanardization) with regard to flicker, and the ways in which flicker can be evaluated or measured. Recent contributions made by the IEC (International Electrotechnical Commission) will be discussed, and the article will conclude with some aspects of equipment design concerned with minimizing flicker in domestic appliances. We shall begin our discussion, however, by listing the major causes of flicker in both the industrial and the domestic field.

Flicker is caused by the switching of high power industrial appliances such as large motors and welding equipment, and of domestic appliances such as dish washers, washing machines, refrigerators and electrical heating installations. In addition, the increasing use of electronic control (e.g. burst firing) as a means of power regulation has led in recent years to a significant increase in flicker, so that the problem is now too great to ignore. As a result CENELEC has set down limits on the maximum permissible flicker that may be produced by a domestic appliance. In most European countries manufacturers are obliged to comply with these limits; this usually means designing anew since the problem of flicker cannot in general be solved by adapting designs currently in use.

TYPES OF VOLTAGE FLUCTUATION

Voltage fluctuation of the mains supply can take many forms depending upon the nature of the appliance and the mode of control. Figure 1 provides two illustrations of voltage fluctuation. The induced flicker is determined by the voltage change ΔV and is given as a percentage of the nominal mains voltage.

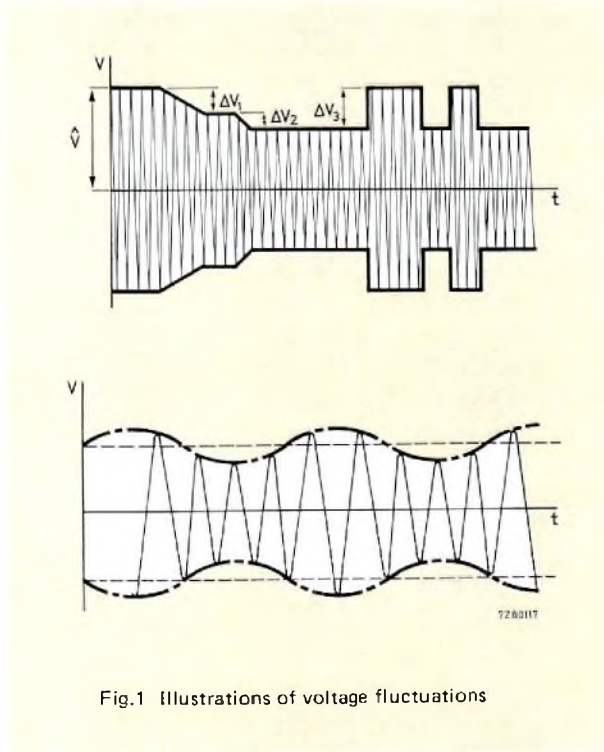


Fig.1 Illustrations of voltage fluctuations

In general, four types of voltage fluctuation can be identified, designated types (a) to (d) in Fig.2. These range from completely regular rectangular voltage changes (a), through irregular voltage changes composed either entirely of step changes (b) or of a mixture of step and random changes (c), and finally to completely random voltage changes (d). The table shows the major causes of these different types of fluctuation.

TABLE
Major causes of flicker

voltage fluctuation type	major causes
(a)	heaters, cookers, boilers etc.
(b)	washing machines, switching of multiple loads
(c)	motor starting, transformers, welding apparatus
(d)	electronically controlled motor-speed appliances e.g. washing machines

TOLERANCE LEVELS – THE FLICKER CURVE AND FLICKER-DOSE

Although the effects of flicker are subjective, much work has been done in an attempt to quantity them. The results of this work are summarized by the *flicker curve* shown in Fig.3. This curve indicates, as a function of the voltage changes per unit time, the maximum voltage variation that can be tolerated before discomfort is experienced. The curve dips at about 20 changes per second, the frequency at which sensitivity to flicker is greatest.

The flicker curve has been adopted by CENELEC as its standard (EN 50 006) for evaluating flicker. For an appliance to comply with the standard, the flicker it induces in the mains must lie on or below this curve.

The irritating effect of flicker is cumulative, so that a distrubance that passes unnoticed over a short period may become intolerable over a longer one. The degree of irritation, known as the *flicker-dose*, is proportional to the duration of the disturbance and to the square of the voltage variation. Figure 4 is a graph of flicker-dose tolerance threshold based on the flicker caused by a 10 Hz sinusoidal modulation of the 50 Hz supply. The solid line, which corresponds to a relative voltage fluctuation of 0.3%, defines the limit for indefinite tolerance at this frequency. A fluctuation greater than 0.3% produces a line of steeper gradient and will, in general, be experienced as intolerable. However, the threshold can be exceeded briefly, as indicated by the broken lines, provided the average fluctuation remains below it.

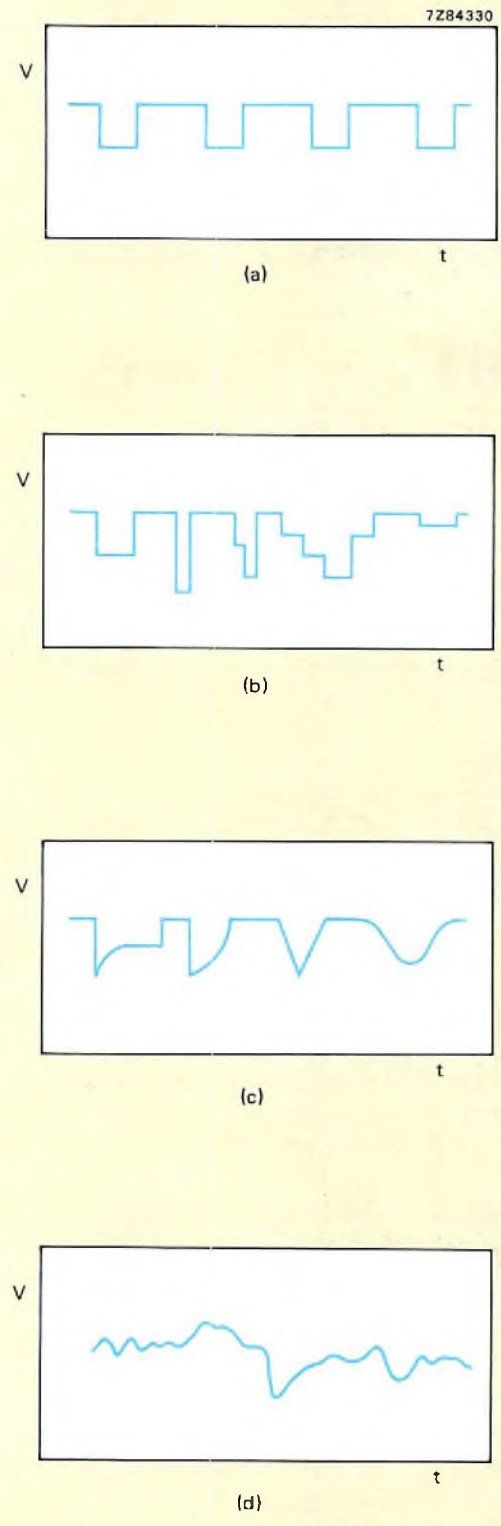


Fig.2 Voltage fluctuations can be divided into four major types

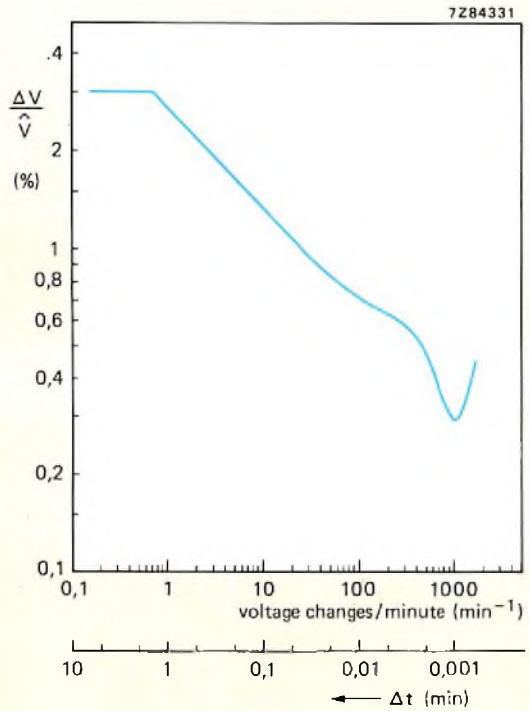


Fig.3 The flicker curve; relative voltage variation as a function of voltage changes per unit time, defining the threshold of unacceptable irritation embodied in the CENELEC recommendations. The lower scale gives the rest-time Δt, which is the minimum time needed for the memory of a voltage change to have faded

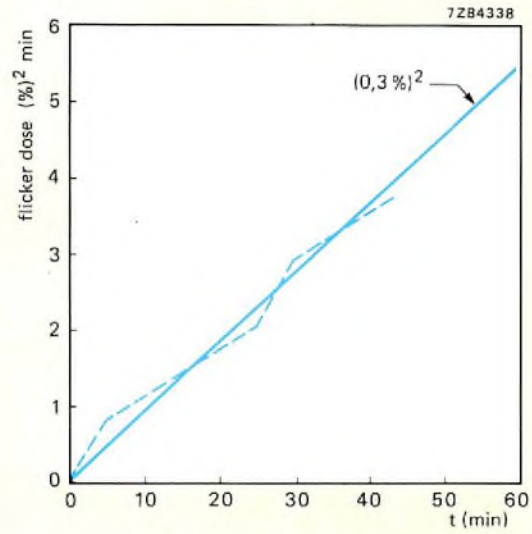


Fig.4 Flicker dose tolerance threshold for a persistent 10 Hz sinusoidal voltage variation

EVALUATING AND MEASURING FLICKER

To discover whether or not an appliance complies with the CENELEC Standard the flicker it induces in the mains must be determined. In many instances, particularly at lower frequencies, this can be calculated. At frequencies above about 120 alternations per minute, however, and in the case of type (d) fluctuations, a *flicker meter* must be used.

Calculating flicker

Type (a) fluctuations

These are the easiest to deal with since they are completely regular with constant amplitude. For example, consider a 1 kW heater controlled between 10% and 100% by means of burst-firing. We can easily calculate the relative voltage change ΔV/V. Taking the mains voltage V as 220 V, and the mains impedance as 0.4 Ω (present day CENELEC reference impedance neglecting the reactive part), then ΔV/V = 0.83%. From the flicker curve we find that this voltage change must not occur more often than 50 times per minute if the device is to comply with the CENELEC Standard. The maximum permitted switching frequency of a 1 kW resistive load controlled by burst-firing is therefore 25 cycles per minute (or about 0.4 Hz).

Type (b) fluctuations

This type of fluctuation, in which the amplitude and frequency both vary, presents a more difficult problem. To deal with it the IEC has proposed a method based on the principle that given two stimuli (i.e. light intensity changes), provided the time between them is long enough, only the last is remembered. The time between the stimuli must be long enough for the memory of the first to have faded; the minimum time for this to occur is known as the *rest-time* Δt.

Using this principle, for each relative voltage change $\Delta V/V$ we can use the flicker curve to find a rest-time Δt within which no further change should occur if the CENELEC Standard is to be observed. Over a specified observation time T containing, say, n voltage changes, these rest-times must satisfy the condition that:

$$\sum_{i=1}^{n} \Delta t_i \leqslant T$$

This is illustrated graphically in Fig.5. T, which may be the repetition period of the waveform, must by convention lie between 5 and 15 minutes and must contain at least 10 voltage changes.

Provided the above condition holds, the flicker is considered tolerable even if the limit is exceeded for brief periods within the observation time.

As an example, suppose a load produces the waveform shown in Fig.6, in which 10 voltage changes occur

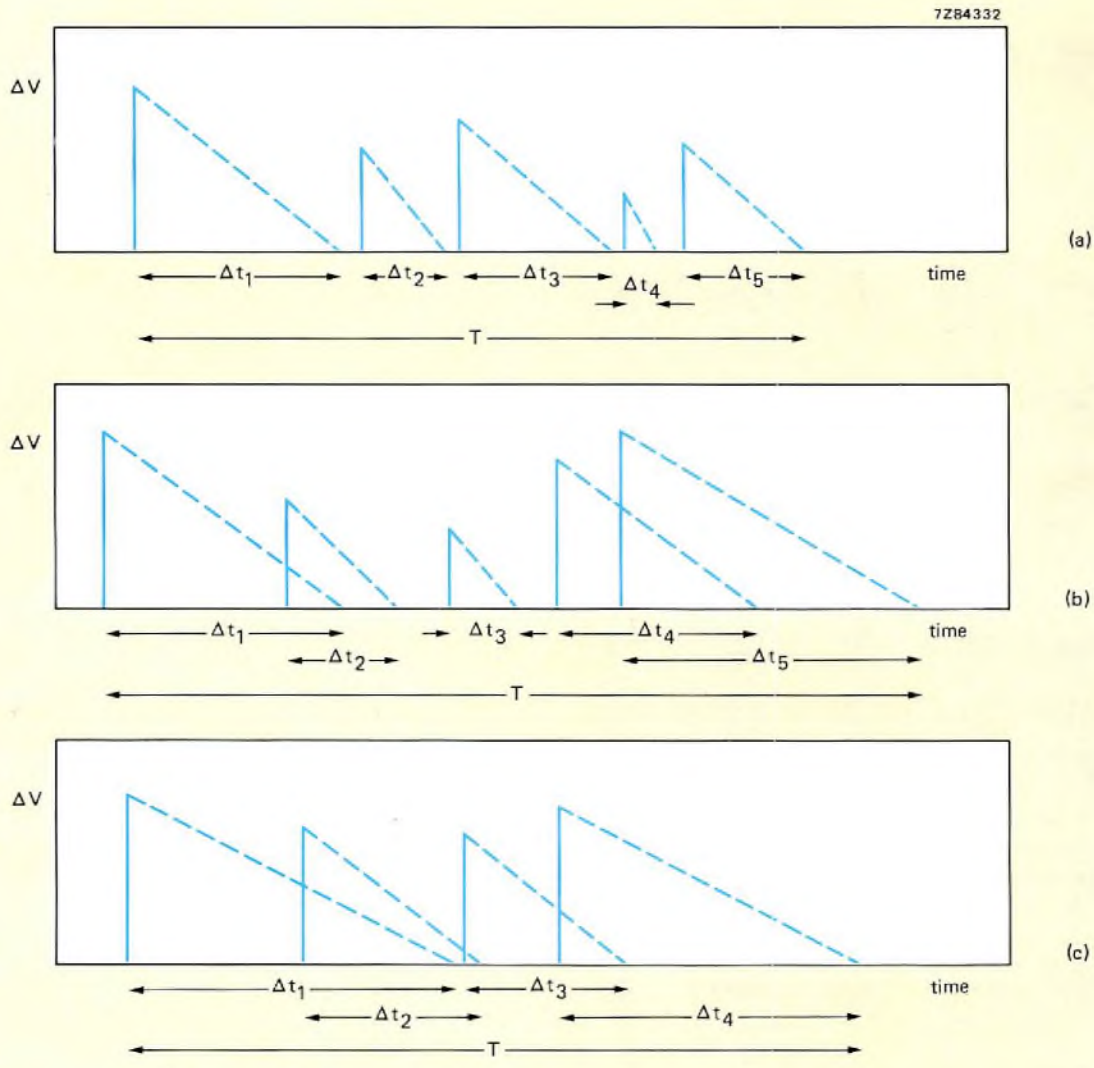


Fig.5 For each voltage change there is a rest-time Δt within which no further voltage change should occur if the CENELEC Standard is to be observed. A voltage change occurring within the rest-time of a previous change may, however, still be permitted if it is followed by a suitably long recovery time.
(a) Permitted voltage changes: $\Delta t_1 + \ldots + \Delta t_5 < T$;
(b) Borderline case: permitted only if $\Delta t_1 + \ldots + \Delta t_5 \leqslant T$;
(c) Forbidden voltage changes: $\Delta t_1 + \ldots \Delta t_4 > T$

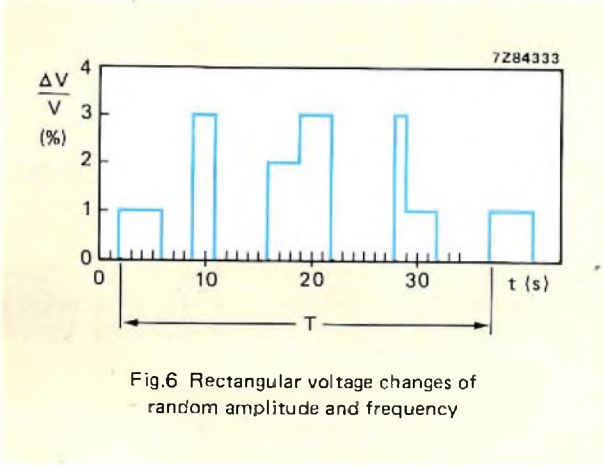


Fig.6 Rectangular voltage changes of random amplitude and frequency

in a 30 second period. The rest-times found from Fig.3 add up to about 375 seconds, so that the waveform must not be repeated within this time if the CENELEC Standard is to be observed.

Type (c) fluctuations

In these fluctuations, the non-rectangular voltage changes are represented by step functions as shown in Fig.7, the waveform then being treated in the same manner as type (b) fluctuations. This method does, however, give pessimistic results, so that an appliance judged unacceptable may still comply with the CENELEC Standard. This can be checked by a direct measurement using a flicker meter.

Direct measurement of flicker

A direct flicker measurement using a flicker meter is needed in the case of type (d) fluctuations and in all instances where calculation gives uncertain results.

One of the first flicker meters to receive CENELEC approval is based on a system developed by EDF (Electricite de France) and described briefly in EN 50 006. This computes the flicker dose from a direct measurement and indicates visually whether or not the CENELEC limit has been exceeded. The disturbed supply voltage is first fed into a filter system that effectively normalizes the signal to the frequency of maximum sensitivity (i.e. about 10 Hz). The normalized signal is then squared and integrated to produce an output proportional to the flicker-dose.

FGH (Forschungs-Gemeinschaft für Hochspannungs- und Hochstromtechnik E.V. Germany) have recently developed a flicker meter in which the disturbed supply voltage is first fed into an equalizing network comprising a system of 12 filters having centre frequencies ranging from 0.7 to 28 Hz, and insertion losses inversely related to the flicker curve. The equalized signal then

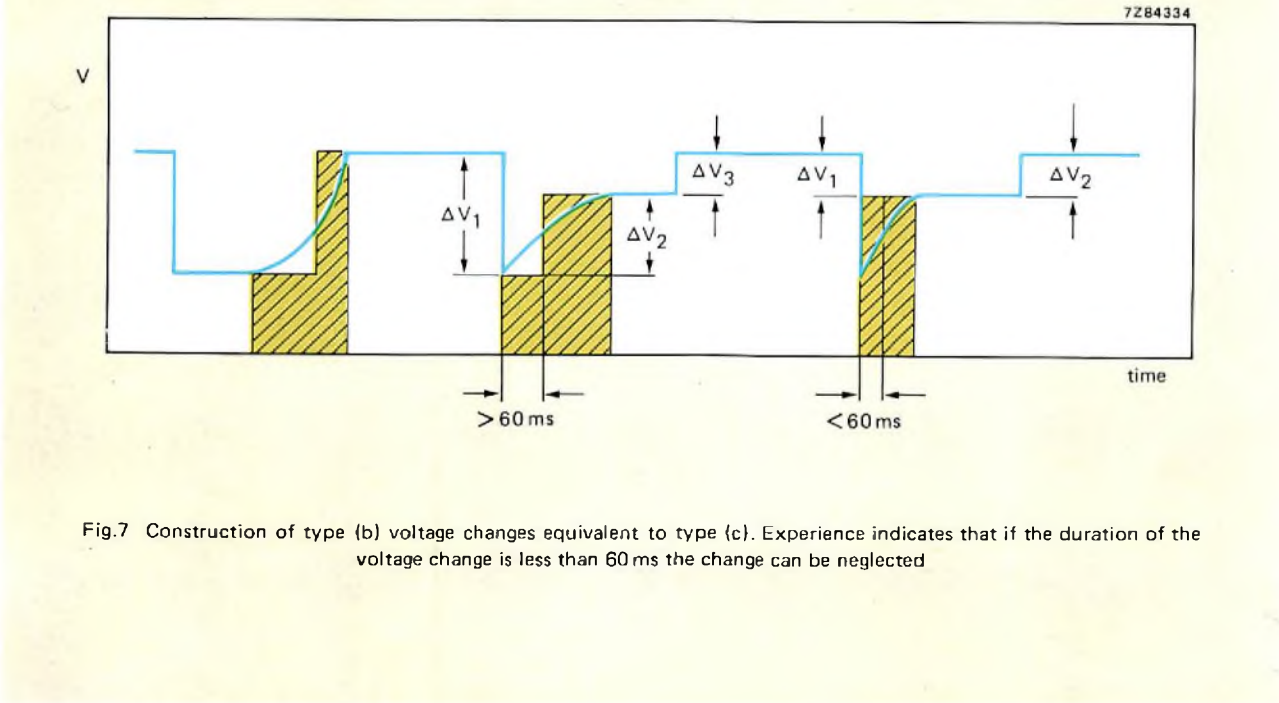


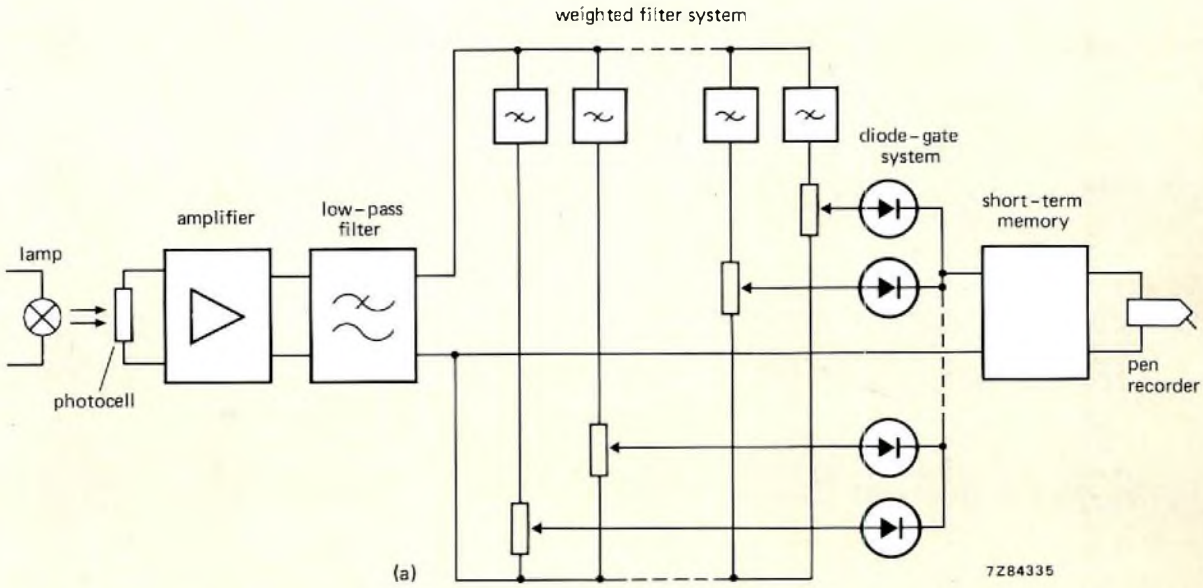
Fig.7 Construction of type (b) voltage changes equivalent to type (c). Experience indicates that if the duration of the voltage change is less than 60 ms the change can be neglected

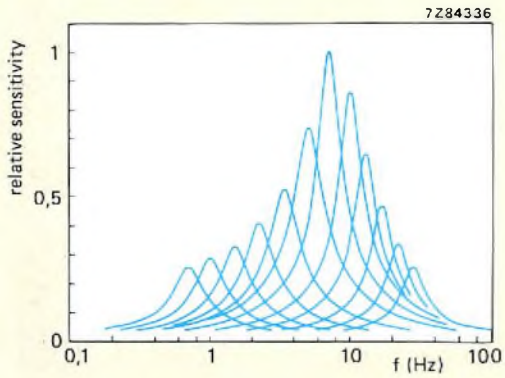
passes to a diode-gate system that taps the highest amplitude continuously present and directs it to a recording device (e.g. a pen-recorder). Equalizing the signal simplifies the task of deciding whether or not the CENELEC limit has been exceeded. A basic block diagram of the system is shown in Fig.8a; Fig.8b shows the frequency responses of the filters.

DESIGNING FOR FLICKER AVOIDANCE

We have already given some examples of control by burst-firing in which the irritation due to flicker can be avoided by judicious choice of switching frequency. This method is very effective wherever long time-constants are involved, as in panel heaters, ovens and boilers. For electronic motor speed control, switching frequencies in the 5 to 20 Hz region (i.e. the region of maximum sensitivity) are best avoided completely.

High-power heating systems with relatively short time-constants, such as hot-air ovens and magnetron ovens, present a more difficult problem. In such systems a compromise between maintaining smooth control and complying with the CENELEC Standard is not easy to obtain. The problem can be solved effectively by the wider use of electronic control within the supply system itself. Below we describe a typical solution employing an h.f. power inverter in the control of a microwave oven.





(b)

Fig.8 (a) Basic block diagram of the flicker meter developed by FGH Germany;
(b) Centre frequencies and insertion losses of the filters

Power control of microwave ovens

In the conventional power module for a microwave oven, the h.t. voltage (4 kV) is generated by a 50 Hz transformer having high leakage inductance. If burst-firing is used to control the power, the triggering points should preferably occur at periodic maxima of the supply voltage to avoid excessive inrush currents. The system does have a number of disadvantages, notably: flicker induced in the mains supply, low efficiency, unstabilised power output and the need for a large and heavy transformer.

These disadvantages can be overcome by using a high-frequency power-inverter as the supply. A basic circuit of such a supply is shown in Fig.9. The circuit employs a centre-tapped load with thyristors as switching elements. The switching frequency is set above the audio range to allow the use of a smaller transformer with a ferrite core.

To regulate power output, use is made of the zener-like magnetron behaviour, in which output current and power are highly dependent upon anode voltage. Small changes in anode voltage are therefore sufficient to produce wide variations in output power. Moreover, mains voltage variations are accompanied by changes in output current; these are suppressed by means of a feed-back control circuit, thus ensuring that output power remains relatively constant.

The system effectively behaves as an up-inverter which means that the h.t. magnetron voltage is relatively unaffected by variations in input voltage. This ensures that the supply presents a reasonably constant impedance to the mains, providing the bonus of greatly reduced harmonic distortion.

Smooth power control with a complete absence of flicker is attainable for magnetron currents between 35 and 280 mA.

The use of h.f. inverters is, of course, not confined solely to the magnetron oven, and they can be used to equal advantage in the control of other devices such as inductive cooking and motor control appliances.

As a final remark we should mention that the use of h.f. inverters can cause r.f. interference in the mains, but this can be avoided by the use of suitable filter networks.

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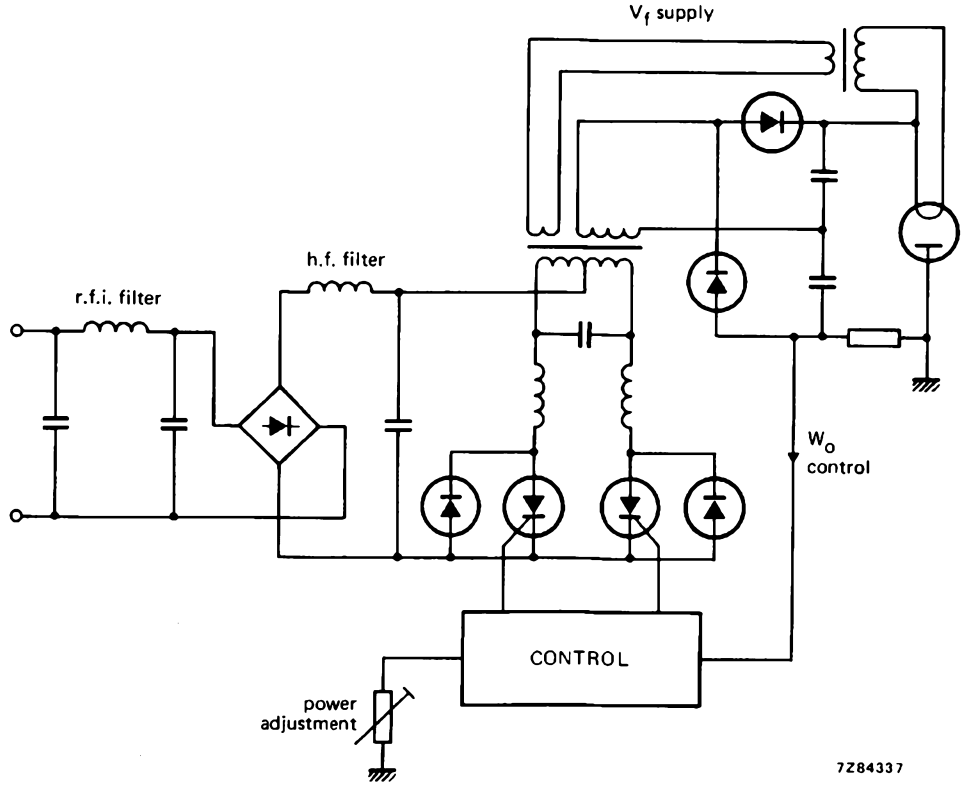

Fig.9 Basic diagram of an h.f. power inverter used as the supply of a magnetron oven

Electret microphone for telephony

A. J. REES and E. I. VÁRSZEGI

The overwhelming majority of the world's telephones use carbon microphones which, despite serious shortcomings, have now been in production for over a hundred years. Their continued use is due to their low production costs, and to the fact that they do not require an amplifier in the telephone. However, recent advances in microphone technology, and the production of cheap, reliable solid-state amplifiers, have largely negated the advantages of the carbon transmitter. Maintenance costs have risen sharply, so that there is now a strong demand for the replacement of the carbon microphone by a more reliable and technically superior device.

There are a number of different transducers which are potential replacements for the carbon microphone. The British Post Office (BPO) is currently conducting field trials to identify suitable linear replacements for its existing carbon microphone, transmitter inset No.16. Several different types of microphone will be tested in this trial, although the majority are likely to have an electret transducer. The electret microphone is particularly well suited to replace the carbon microphone. It is very reliable, cheap to produce, of high quality, and the subject of proven production technology.

In this article, the operation, construction, and characteristics of the electret microphone are considered, with particular reference to its use in telephony. The article begins by describing the operation of the carbon microphone and examining the arguments for its replacement. This is followed by an explanation of the operation of the electret microphone, and the construction and long-term performance of our electret capsule is described in detail. The desirable characteristics of a microphone suitable for telephony are then discussed, and the design of an appropriate amplifier considered. The article concludes by reviewing future changes in the telephone system which may result from the use of linear microphones.

CARBON MICROPHONE

The construction of a modern carbon telephone microphone is shown in Fig.1. Loosely-packed carbon granules are contained between carbonised metal electrodes. The rear electrode is fixed, and the front electrode attached to the diaphragm. Variations in sound pressure on the diaphragm change the area of contact between the granules, thereby altering the resistance, and modulating the transverse current. It is a self-amplifying transducer, as the electrical power out is considerably greater than the acoustical power going in.

Apart from its attractions as a power amplifier, the carbon microphone has the additional advantages of being reasonably robust, cheap, and easy to manufacture. The main disadvantages include high noise, non-linearity, instability of characteristics and, when compared with more modern microphones, a high failure rate. All of these disadvantages can be attributed to the physical properties of the carbon granules, especially the tendency of the granules to deterioriate with age and use. However, extensive development and the careful control of materials and manufacture have produced a microphone in which these disadvantages are kept to reasonable levels. As a part of this development process, the characteristics of the modern carbon microphone have been tailored to match the transmission elements of the

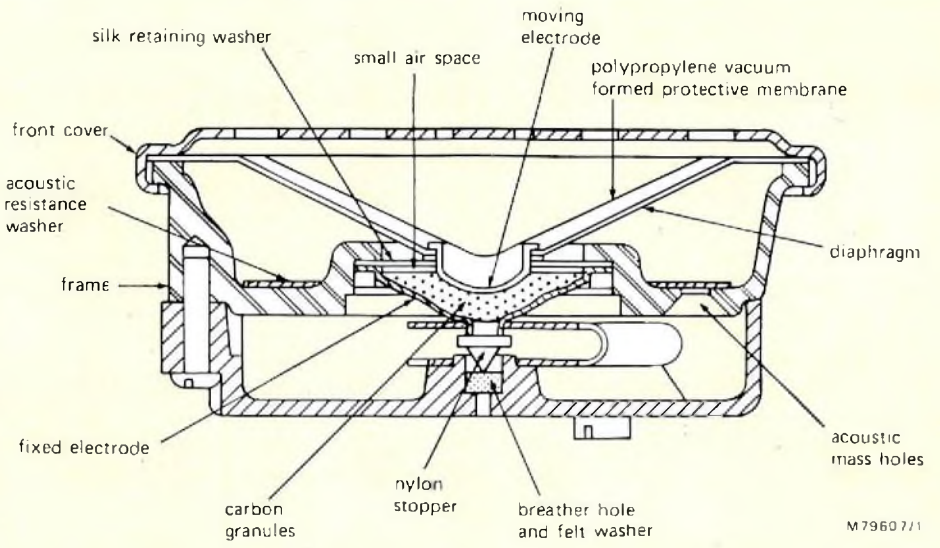

Fig.1 Structure of a modern carbon microphone

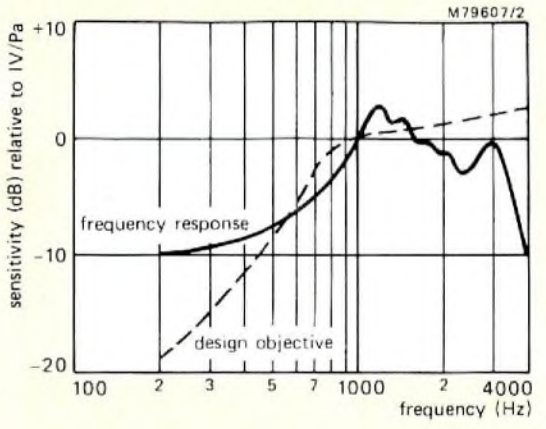

Fig.2 Typical frequency response of carbon microphone, and design objective for maximum intelligibility

telephone system, in particular the line and exchange relays, and to give a frequency response which is compatible with the requirements of maximum intelligibility (see Fig.2).

Despite this satisfactory process of development, the past fifteen years have seen many attempts to introduce alternative types of microphone, both for new telephone designs and as direct replacements for existing carbon types. Many different types of transducer have been proposed, and in some instances, placed in service. However, the combined cost of the transducer and the necessary electronic amplifier has always been significantly greater than the self-amplifying carbon microphone. Because of this cost penalty, replacements for the carbon microphone have yet to find widespread use.

Two factors are likely to change this situation: increasingly high maintenance costs which offset the initial cost advantage of the carbon microphone, and the production of cheap polymer foil transducers. Such transducers require amplification, but given the demonstrated reliability of electronic components and assembly methods, they should have lower long-term costs than the carbon transmitter with its permanent maintenance penalties. There is therefore a good economic argument for introducing a replacement unit for substitution in existing telephones.

In addition to the direct financial benefits, there will be less easily quantifiable gains due to consistent transmission performance, fewer faults, and improved audio quality. Looking more to the future, the introduction of a microphone with highly consistent transmission performance, should assist the maintenance of well-toleranced levels throughout the national network.

ELECTRET MICROPHONE

There is no perfect microphone for telephony, but of the types currently being considered to replace the carbon transmitter, the electret is the most strongly favoured. Its advantages include: simplicity of construction, low costs, relatively high output, low diaphragm mass, easy

control of parameters, and mechanical robustness. In addition, microphones of this type have now been in production for over ten years so that extensive knowledge exists on their long-term mechanical and electrical reliability.

The electret microphone can best be understood as a development of the capacitor microphone. A capacitor microphone consists basically of a thin electrically-conducting membrane stretched closely in front of an insulated metal backplate to form the two plates of an electrical capacitor. If the capacitor is charged, any movement of the diaphragm due to acoustic pressure varies the potential difference between the plates in sympathy with the variations in capacitance. Microphones of this type are of very high quality, and are used as precision measuring microphones and in broadcasting and recording applications. However, they do require a stable polarising voltage and an impedance-matching network to step down the very high output impedance, typically several hundred megohms. Impedance matching is now achieved using an FET (Field Effect Transistor) source-follower circuit, while the development of polymer electrets has eliminated the need for the polarising voltage.

An electret is a material which can retain electrical charge. It can be thought of as the electrical analogy of a permanent magnet. In the electret microphone, the diaphragm is formed from an electret polymer film. Since the film is permanently charged, a polarising voltage is unnecessary. In modern electret microphones, charge densities equivalent to a polarising voltage of 300 V are readily achieved.

Electret capsule

The construction of our electret capsule is illustrated in Fig.3, and an exploded view of the capsule is shown in Fig.4. The electret diaphragm has a diameter of 10 mm, and the capsule has an effective capacitance of 15 pF. The diaphragm is Teflon-FEP, metallised on the upper surface. During assembly, the electret foil is stretched and then glued to a metal ring so that it remains under tension. The acoustic back volume provides compliance against the movement of the diaphragm. A source-follower amplifier (FET) is included in the capsule, to give the required reduction in output impedance.

We have been manufacturing electret capsules for more than ten years. During this period, over ten million capsules have been produced for use in tape decks alone. Figure 5 shows several microphones, all containing the electret capsule. With the exception of the mobile microphone, the microphones shown in Fig.5 are of Hi-Fi standard. Figure 6 shows the frequency response for the Hi-Fi omnidirectional type. It indicates excellent frequency/sensitivity characteristics, and shows clearly the good acoustic performance of the capsule. In addition to microphones, we also produce electret headphones. These have an area of charged foil of about 75 mm in diameter.

Quality of polymer electrets

Recent developments in polymer technology have made it possible to produce high-quality polymer electrets. By using fluorcarbon polymers and charging the foil negatively, electrets of particularly high stability can be

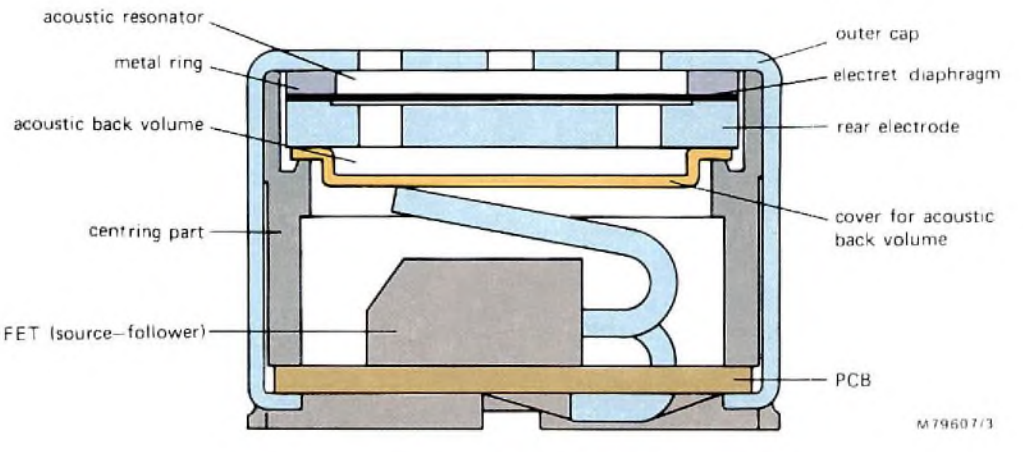

Fig.3 Structure of electret capsule

Fig.4 Exploded view of electret capsule

Fig.5 A selection of electret microphones

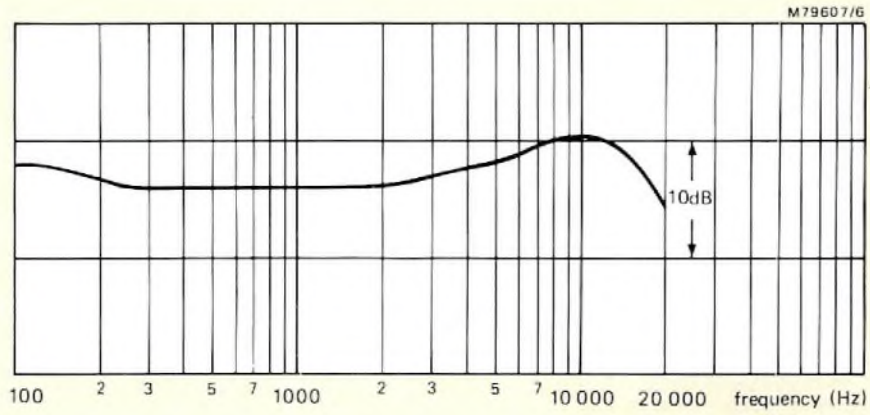

Fig.6 Frequency response of an omnidirectional electret microphone

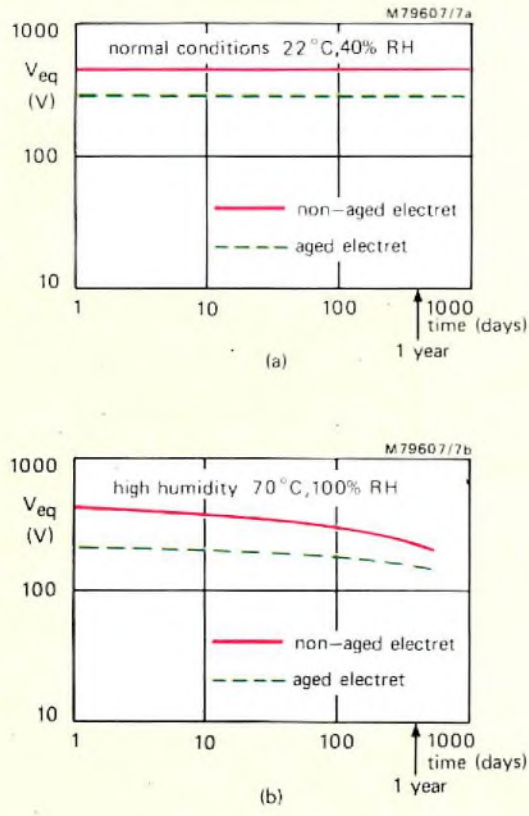

Fig.7 Long-term stability of Teflon-FEP electrets:
(a) under normal temperature and humidity conditions
(b) under severe temperature and humidity conditions

obtained. The foil in our electret capsules is charged by a corona-discharge process. In this process, the foil is placed in a corona-discharge and the electrons are driven into the foil by an electric field. Figure 7 illustrates the charge stability characteristics obtained by this method. Charge density is measured in equivalent volts (V_{eq}); that is, the potential that would exist between the diaphragm and the back electrode if the foil was in a capsule. A charge density of 7 nC/cm^2 gives a V_{eq} of 100 V. The results shown in Fig.7a were obtained for normal temperatures and humidities, while for Fig.7b the temperature was 70°C and the relative humidity 100%. Even in tropical conditions no electret would be exposed to conditions as severe as these. The two solid lines represent the behaviour of ordinary electrets, and the broken lines the behaviour of electrets subject to a special pre-ageing process where the charge is stabilised by heat treatment. Even without ageing, the stability of the electrets is remarkable. For normal temperature and humidity the charge density of an untreated electret drops by only 5% in three years, while under conditions of extreme humidity and temperature it drops by 50%. This performance is improved by the ageing process; in particular the stability of the electrets towards moisture.

The thermal stability of Teflon-FEP foil electrets is illustrated in Fig.8. Again, results are given for aged and non-aged electrets. The charge on the untreated electret does not decay before a temperature of 160°C has been reached, while for the aged electret the charge is still stable at 200°C.

From the experimental results presented in Figs.7 and 8 it is clear that fluorcarbon foil electrets, charged by a corona-discharge method, have excellent charge retaining properties. At normal temperature and humidity, the charge is retained almost indefinitely, while even under extremeley adverse conditions the rate of charge loss is still slow.

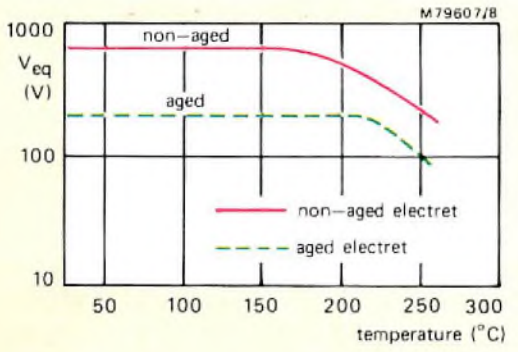

Fig.8 Thermal stability of Teflon-FEP electrets

Assembly and testing of electret capsule

The assembly sequence and testing procedures for the electret capsule are set out in Fig.9. A special thermal discharge test is used to check the quality of incoming foil. The foil is charged, and then heated at a constant rate while V_{eq} is measured. Typical results for this test are shown in Fig.10. If V_{eq} falls before a specified temperature is reached, the foil is rejected. Prior to the assembly of the complete capsule, the FET is attached to the PCB, and the foil glued to the metal ring to form the diaphragm. The diaphragm is then given a special heat treatment to improve the mechanical properties of the foil. The assembly of the complete capsules is auto-

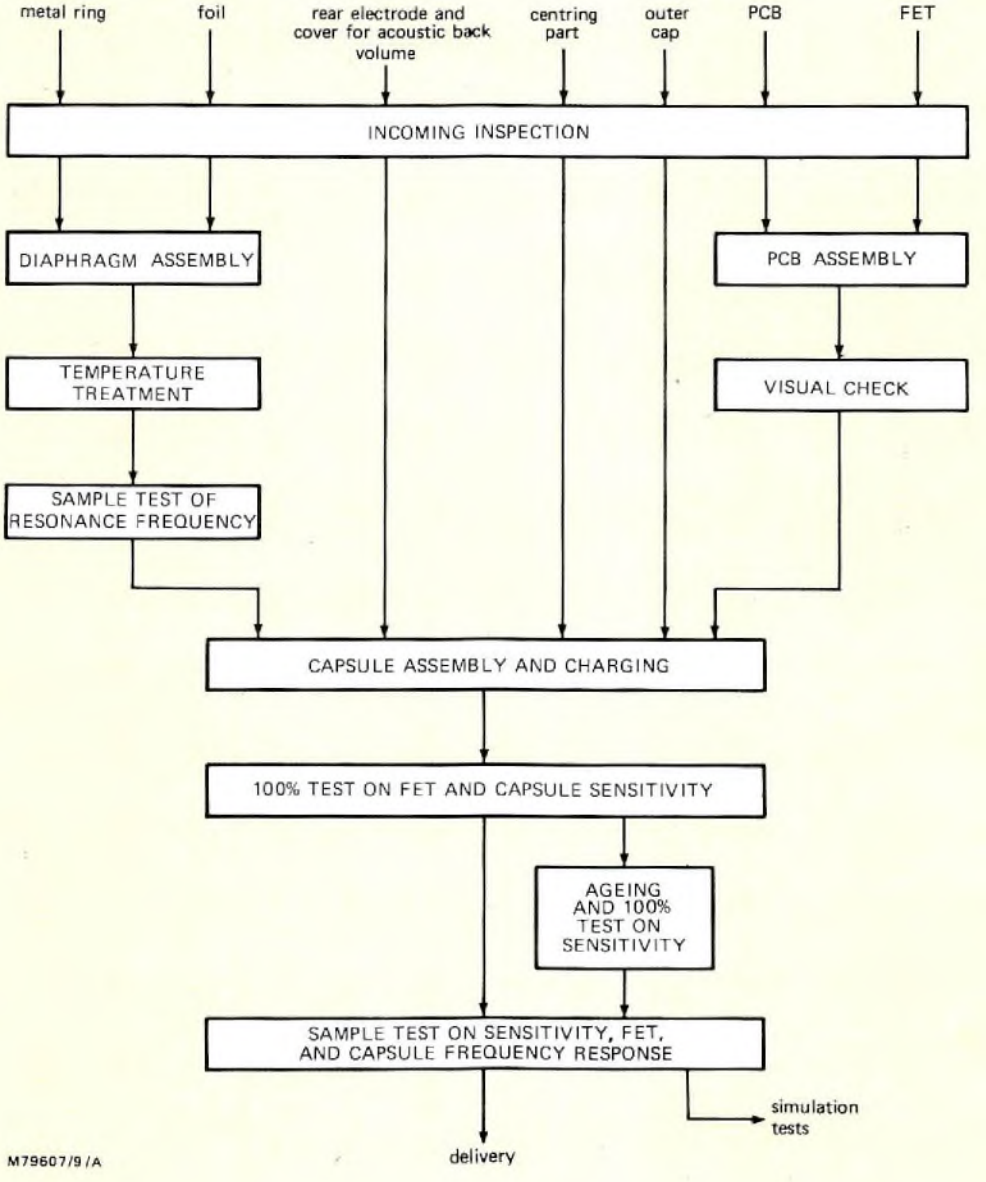

Fig.9 Electret capsule production process

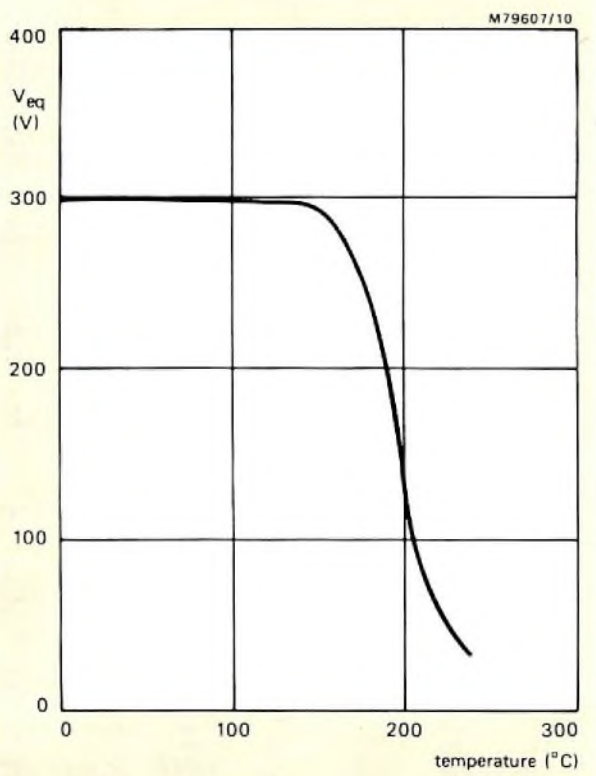

Fig.10 Thermal discharge test of Teflon-FEP foil (non-aged foil)

mated, and a detail of the machine used in this process is shown in Fig.11.

The foils are charged during the capsule assembly. When charged, capsules are liable to attract dust and positive ions which will mask the negative charge. To overcome these difficulties, the electrets are charged so that the charged surface is facing downwards.

After assembly, but on the machine, all capsules are tested for FET performance and sensitivity. For capsules needing to meet special requirements, assembly is followed by a thermal-ageing process. Since this can affect the charge concentration, the test of sensitivity is then repeated. As a part of the quality control procedure, samples of completed capsules are tested for sensitivity at 1 kHz, FET performance, and frequency response. The test of sensitivity and FET performance is shown in Fig.12.

Production samples are regularly subjected to a series of simulation tests to ensure a consistent performance from the production process. The details of these tests are set out in Table 1. Any significant variation in performance produced by these tests indicates a change in production quality level.

Long-term performance of electret capsule

The long-term acoustical performance of the electret capsule is shown in Fig.13. This figure shows variations

TABLE I
Simulation test

Test	Conditions	Purpose
Drop test	10 times onto a concrete surface from a height of 1 m	Exposes mechanical weakness in capsule
Cold storage test	−25 °C for 96 hours	Exposes mechanical and acoustical weakness
Heat storage test	+55 °C for 96 hours	Exposes mechanical and acoustical weakness
Damp heat cycling	21 cycles, upper temperature 45 °C (IEC 68 Db)	Reveals tendency to corrosion
Damp heat steady state	10 days, 42 °C, 95% RH	Reveals tendency to corrosion
Industrial atmosphere	48 hours H_2S and 48 hours SO_2	Checks stability of contact resistance
Bump test	3000 bumps, peak acceleration 40 g (IEC 68 Eb)	Exposes mechanical weakness
Vibration functional test	Three directions, 30 minutes per direction, peak acceleration 5 *g* (IEC 68 Fc)	Exposes mechanical weakness
Thermal shock test	Five cycles, −25 to +55 °C	Exposes mechanical and acoustical weakness

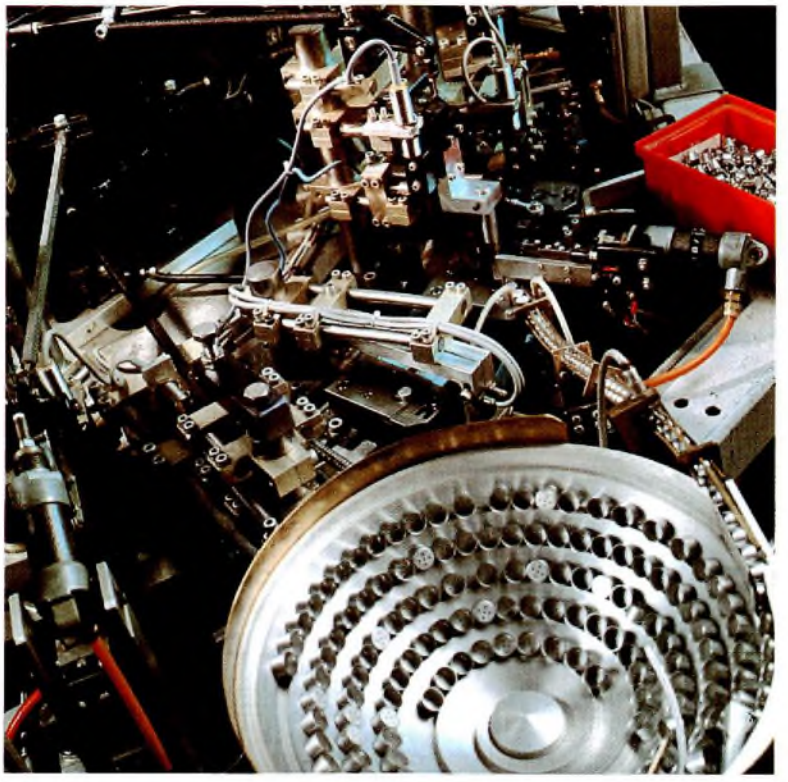

Fig.11 Detail of automatic assembly of electret capsule

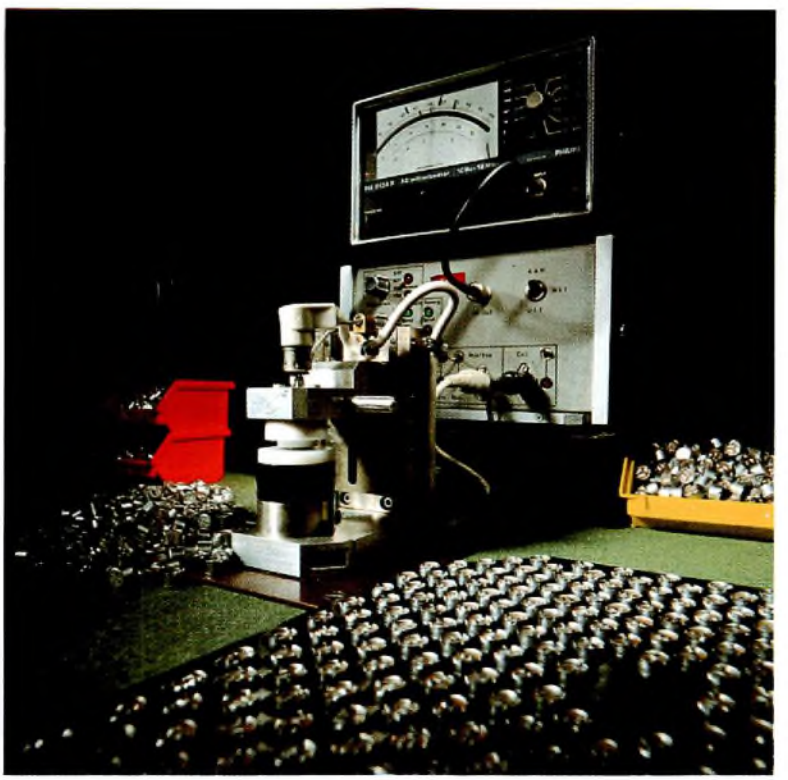

Fig.12 Quality control test of sensitivity and FET performance

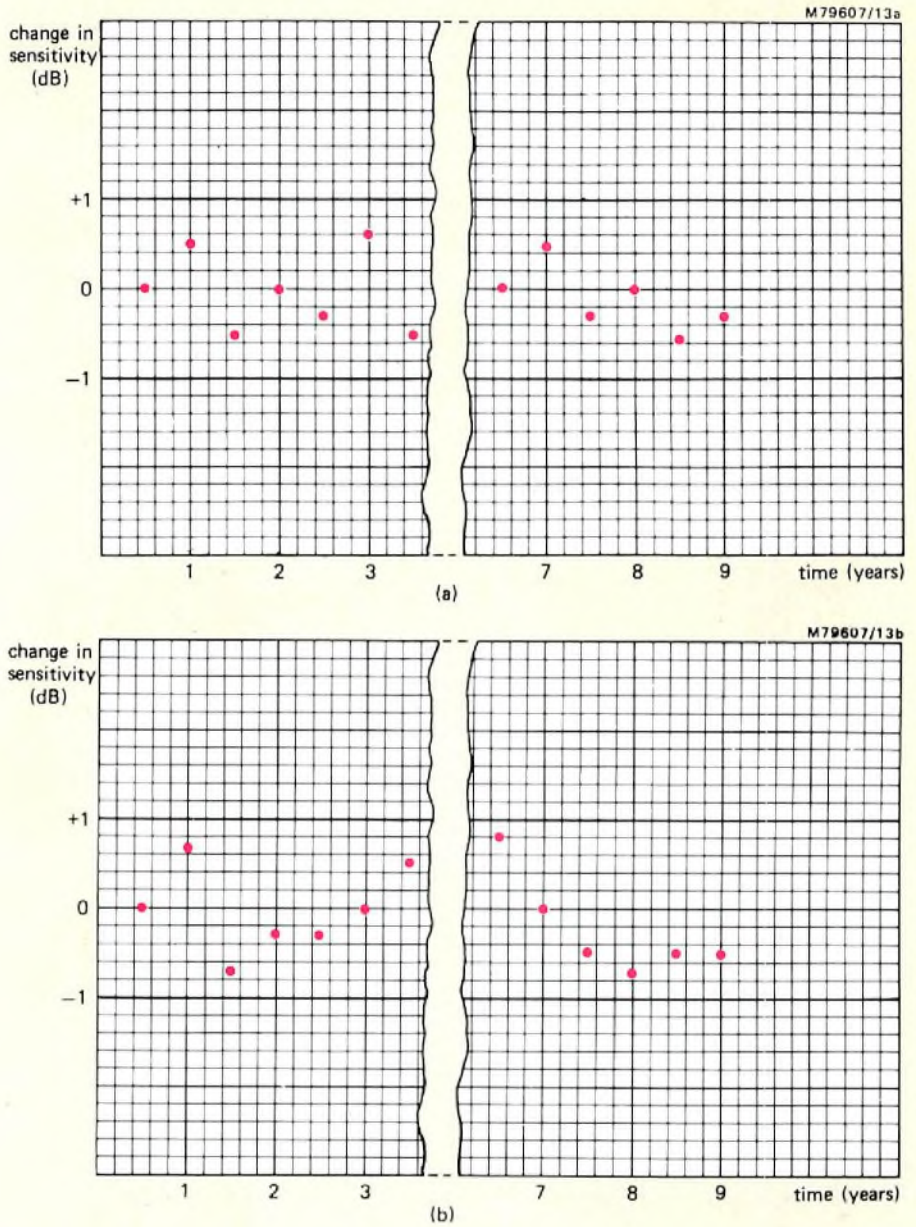

Fig.13 Long-term sensitivity of electret capsules (measuring accuracy ±0.5 dB in an anechoic room): (a) normal conditions (b) tropical conditions

in sensitivity for a group of capsules stored for a total of nine years. For Fig.13a the capsules were stored under normal conditions, while for Fig.13b they were stored under tropical conditions: 95% RH; twenty-four hour temperature cycle, upper temperature 45°C. As with the data on the charge stability of the foil, Figs.7 and 8, these graphs indicate the remarkable consistency in the performance of the capsule.

DESIRABLE CHARACTERISTICS OF A REPLACEMENT LINEAR MICROPHONE

In practice, the performance characteristics required by a microphone intended to replace the carbon transducer will vary for different national telephone organisations. These variations will reflect the different states of development in national network transmission and signalling plans. For example, where high maintenance

costs justify a linear microphone as a direct replacement of the carbon transmitter, then a close mechanical and electrical correspondence between the linear replacement and the original transmitter will be required. New telephone designs, on the other hand, could significantly alter the mechanical and electrical requirements of the microphone. Because of these wide potential variations in microphone requirements, it is not possible to give a single detailed specification for a linear replacement microphone. However, the significant performance factors will be common to all types, and these are considered below.

Line current

Line current is determined by the central battery supply voltage, the relay hold-in current, and by the length of the subscriber loop. Typical values will be in the range 15 to 100 mA.

Supply voltage

To limit dissipation, and heat generation within the handset, the voltage drop caused by line current through the transmitter should be as low as possible. However, as the telephone usually has only two connections, the supply voltage must be large enough to ensure that the electronic amplifier remains in the linear region even on peak signals, and with line current at a minimum. The voltage drop will increase as line current increases, reaching a maximum when line current is a maximum. Clearly, this maximum voltage drop must limit dissipation to an acceptable level, but the practical minimum voltage drop across the microphone will then be determined by the amplifier working conditions and necessary additional components. In summary these are:

1) Bias on the FET (where an electret microphone is used).
2) Bias at the coupling to the telephone line (where conventional resistive coupling is used). This bias voltage must be greater than the peak a.c. voltage.
3) A bridge rectifier in the line circuit; this ensures that the microphone can operate from line currents of either polarity.
4) A resistor and semiconductor suppressor diode; this provides protection from line current surges and transients.

As a result of the above factors, a d.c. operating voltage of between 4 and 8 V, at the extremes of line current, should be expected.

Stress

This can take three forms: electrical, mechanical, and environmental. Probably the most significant form of electrical stress will arise from internal dissipation in the event of line current surges and transients. The severity of the conditions applied to the transmitter will depend on other aspects of the telephone design, such as the wound component anti-side tone circuit. In addition, to obtain type approval, it may be necessary to submit linear microphones to transient voltages in the order of a few kilovolts.

It is difficult to be specific about the need for a microphone to withstand mechanical stress, but dropping a handset or telephone accidently in the home, or possibly deliberately in a public installation, will generate high impulsive accelerations, possibly more than 1000 g.

The required level of resistance to environmental stress is likely to be dependent on the procedures for type approval. With new technologies it is difficult to devise tests which reflect the real-life operating conditions, but for a new microphone, operation in a temperature range of -10 to 50°C with a relative humidity of 85% is likely to be a typical operational range.

Sensitivity

The requirement for transmitter sensitivity is likely to be in the range 200 to 500 mV/Pa, at 1 kHz, with design objectives varying for different telephone authorities. Sensitivity measurements are commonly made as a function of frequency using an artificial mouth and a specified load such as an artificial line. The development of standards of sensitivity for ensuring good speech intelligibility has been a long and complex process (see Ref.1). It has required a study of both human and technical factors: nominal loudness of speech, positioning of the microphone, transmission impairments, background noise, and receiver characteristics. Much of this development process has included extensive subjective investigations.

For a number of reasons, such as the prediction of transmission levels, it is necessary to control the output impedance of the microphone. Dynamic output impedances of less than 100 Ω would be a typical requirement.

Frequency response

The useful frequency response of a linear microphone for telephony should closely approximate to the well-known standard for intelligible communication (see Fig.2). The required frequency range is 300 Hz to 3.4 kHz. Low-frequency and high-frequency roll-off should be provided with some pre-emphasis between 1 and 3 kHz.

Tolerances and stability of characteristics

A linear microphone would be required to have narrower initial tolerances, and negligible degradation with use under adverse environmental conditions, when compared with the carbon transmitter.

Non-linear distortion

Again this is a performance feature where the linear microphone would be expected to show considerable advantage over the carbon transmitter. However, high standards are not required and 1 to 5% total harmonic distortion, at normal speech levels, should be acceptable. An alternative amplitude distortion specification requires sensitivity to be substantially constant over the expected SPL range, possibly up to 2 Pa.

Noise

A linear microphone should have a lower noise level than a carbon transmitter, although a perceived noise increase in the carbon transmitter can have the advantage of giving an early warning of failure. At present, there are numerous additional sources of noise in a typical connection, and a figure for total tolerable noise power in a subscriber line is typically specified at below –60 dBm.

Stability and electromagnetic interference

The amplifier of a linear microphone would be required not to oscillate at any frequency, under any combination of terminating impedances. In addition, the microphone should not respond to unwanted electrical signals on the line, or radiate signals. To meet these requirements, the microphone will need careful screening and decoupling at the connection to the telephone line.

AMPLIFICATION

Figure 14 shows the design of a discrete semiconductor amplifier which, together with our electret capsule, can form a microphone suitable for telephony. The assembled circuit, together with the electret capsule, is shown in Fig.15. The resistors shown are the normal preferred values. However, by changing R_1 to 102.7 kΩ, R_4 to 449 kΩ, R_{10} to 21.4 kΩ, and R_{11} to 89 kΩ, the per-

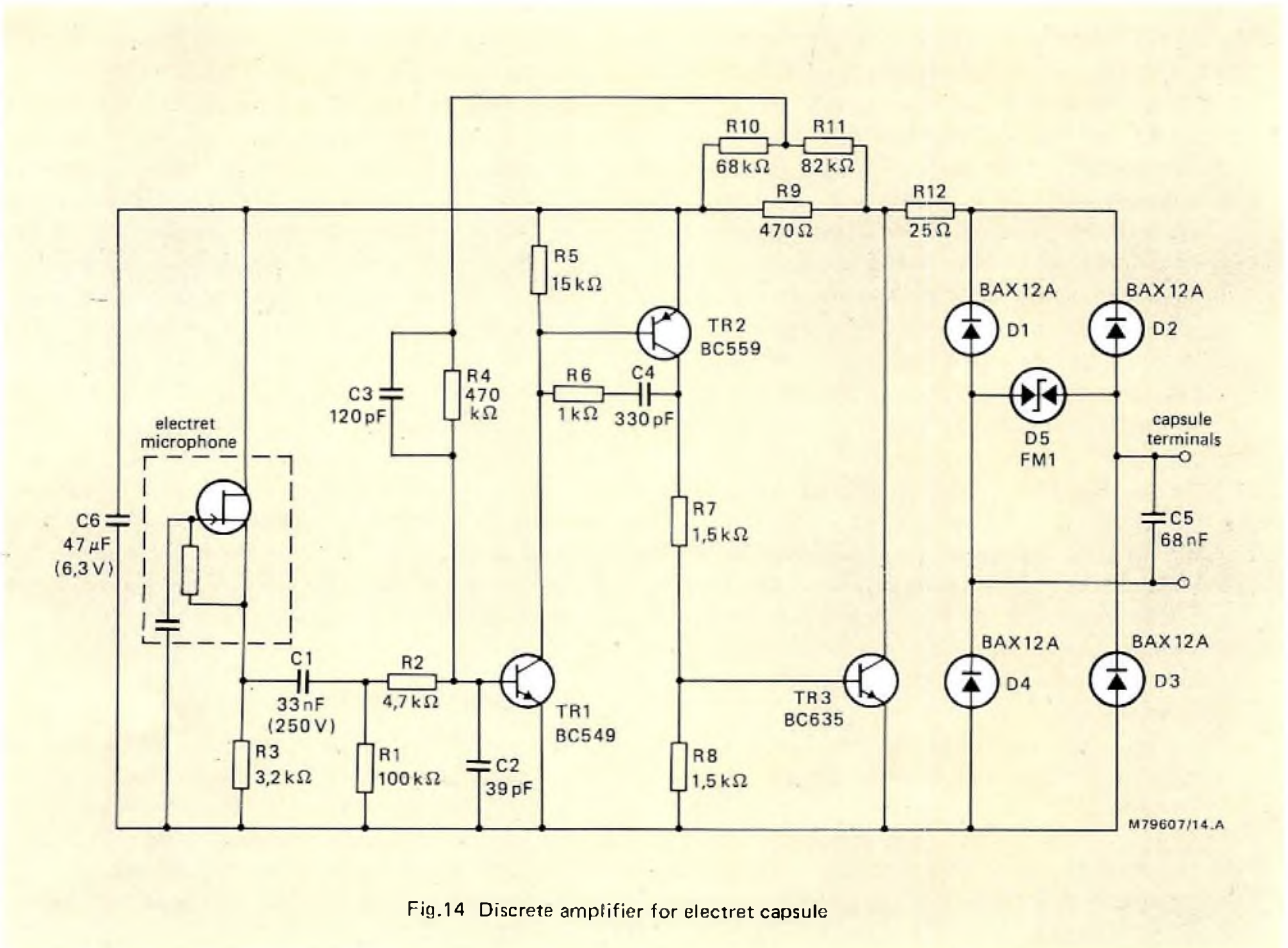

Fig.14 Discrete amplifier for electret capsule

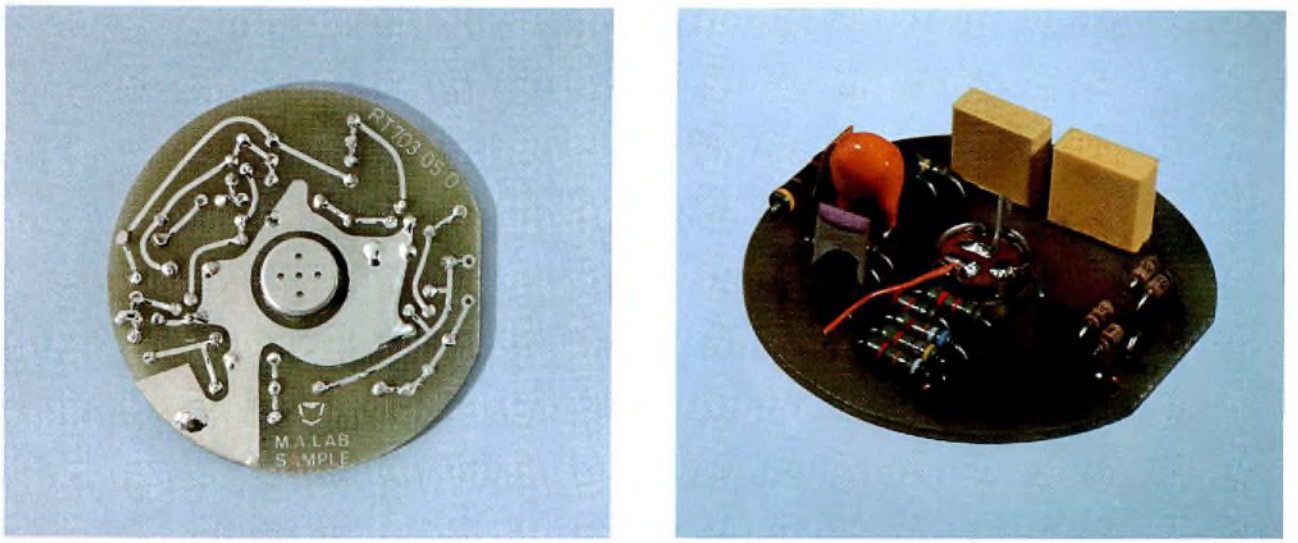

Fig.15 Assembled discrete amplifier and electret capsule:
(a) front view; (b) rear view

formance of the amplifier in combination with the electret capsule provides a suitable replacement for the BPO transmitter inset No.16. The circuit was also designed to illustrate the feasibility of incorporating thick-film technology, for example a resistor network trimmed at the final assembly.

Circuit details

The amplifier, as shown in Fig.14, is of conventional design except in that the d.c. power input and the a.c. output signal use the same connections. The stabilisation of bias conditions and audio-frequency gain is achieved by d.c. and a.c. feedback. It can be shown that the resistor R_1 controls the d.c. adjustment, but has negligible effect on a.c. gain, while R_{10} may be varied to adjust gain with negligible effect on the d.c. bias.

The low-frequency roll-off is determined by capacitor C_1, together with R_2, and the output resistance of the FET source-follower. The high-frequency roll-off is determined by C_3 and R_4, but will also depend on the acoustic design of the electret encapsulation within the transmitter inset.

Sensitivity to r.f.i. is reduced by the inclusion of C_2 at the base of TR_1. Stability is controlled by C_2, the local feedback network C_4R_6, and the capacitor C_5 placed across the telephone line.

Amplifier performance

Details of the performance of the amplifier are summarised below. Design details and nominal and toleranced performance have been established by computer, with subsequent experimental verification.

D.C. conditions

Figure 16 shows the variation of voltage drop with line current, with the amplifier connected to the electret capsule. This figure shows good agreement between the predicted and measured results, within 90 mV at 100 mA.

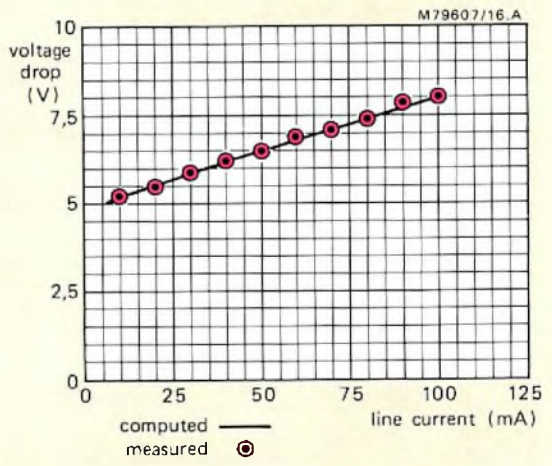

Fig.16 Microphone voltage drop as a function of line current

Gain and frequency response

Computer prediction of the gain of the amplifier itself as a function of the frequency is shown in Fig.17. It should be noted that when combined with the electret capsule in the transmitter inset, the degree of high-frequency roll-off will be increased because of acoustic filtering. Computer analysis shows the variation of gain caused by the h_{fe} of the three transistors to be less than 0.3 dB at 1 kHz, 50 mA line current, and the variation with line current to be less than 0.3 dB between 15 and 100 mA.

The predicted variation of gain with the value of R_{10} is shown in Fig.18. The agreement between predicted and measured performance is within 0.6 dB at 1 kHz, 50 mA.

The predicted a.c. output impedance of the amplifier at 50 mA line current is shown in Fig.19. The output impedance is substantially resistive.

Noise

The psophometrically-weighted noise voltage across a 100 Ω load resistor has been measured as −83.2 dBV. The measurement was made with the amplifier input terminated by 1 kΩ representing the FET output impedance.

Harmonic distortion

Figure 20 shows the total harmonic distortion measured into a 100 Ω load at line currents of 15 and 50 mA.

Stability

The stability parameters of the amplifier have been computed over a wide frequency range and checked experimentally. Computer analysis predicts that the amplifier gain will fall to 0 dB at about 500 kHz for all values of R_{10}, with a further reduction to −76 dB at 10 MHz. The loop phase margin is calculated to be more than 75° for resistive loads between 100 Ω and 100 kΩ.

These results have been confirmed experimentally, but such experimental performance does assume good component layout to prevent local feedback within the amplifier itself.

FUTURE DEVELOPMENTS

This article has demonstrated that the electret microphone is highly suitable for use in telephony. Initially, it will be introduced primarily as a replacement for existing

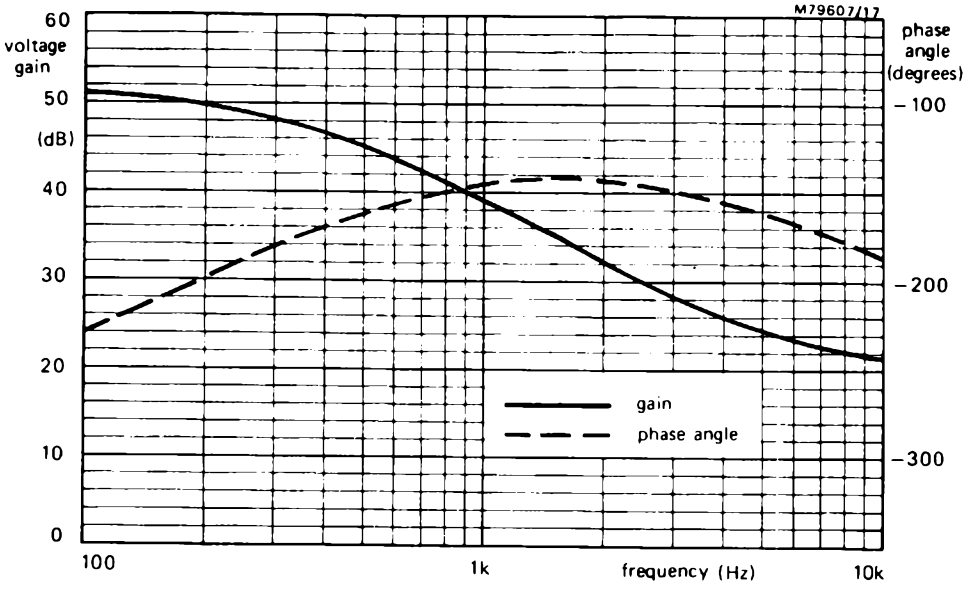

Fig.17 Amplifier voltage gain and phase angle as a function of frequency

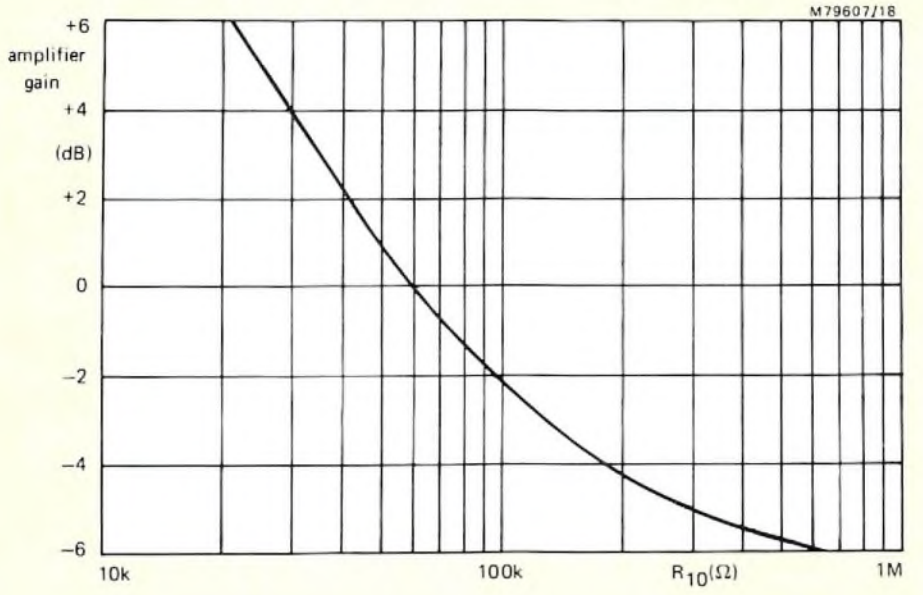

Fig.18 Amplifier gain as a function of R_{10}

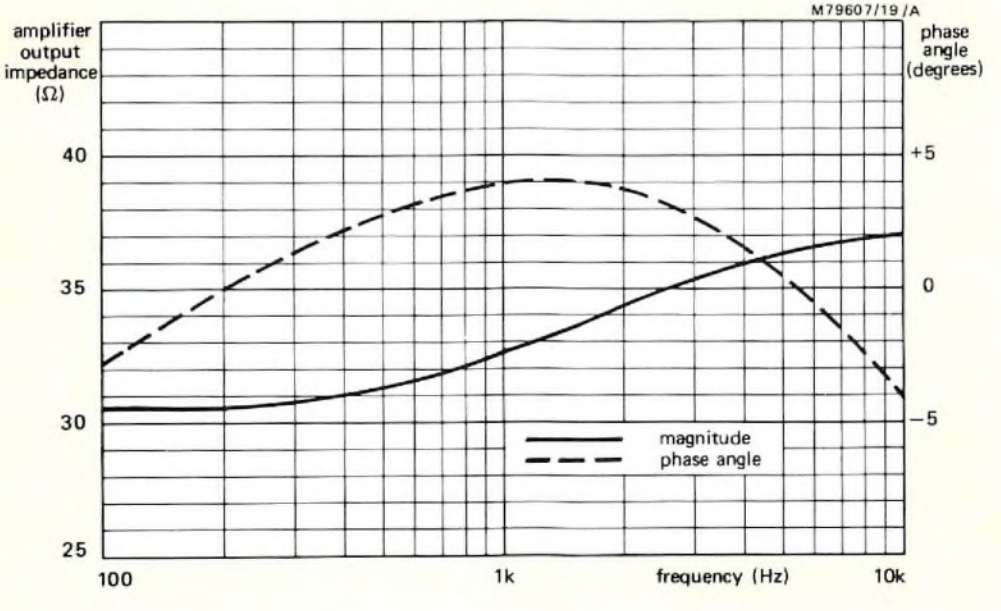

Fig.19 Amplifier output impedance and phase angle as a function of frequency

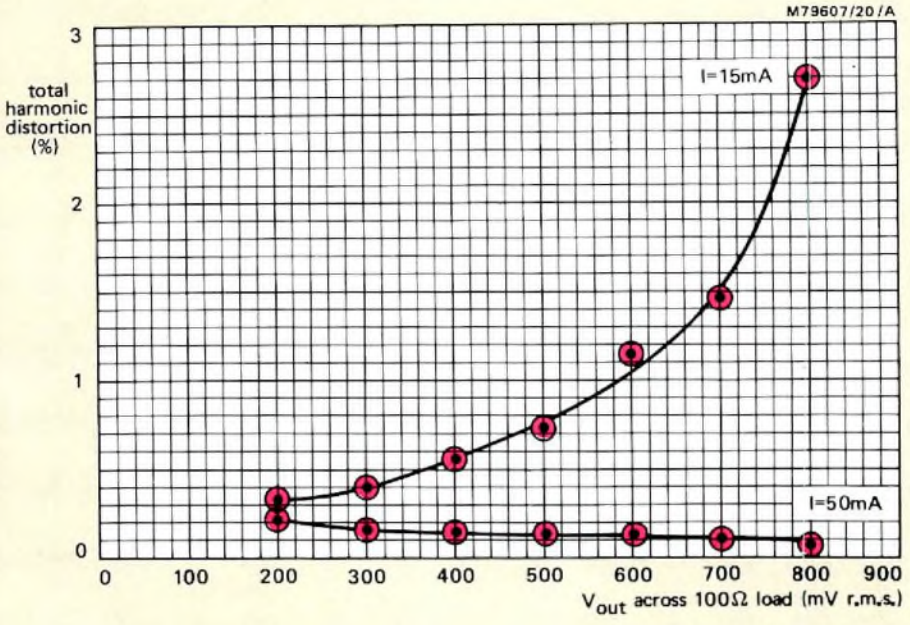

Fig.20 Total harmonic distortion as a function of output voltage

carbon transmitters. During the early stages of this replacement programme, the discrete amplifier may be retained, but once production quantities are sufficient, it will be superseded by an IC amplifier.

In parallel with this replacement process, electret microphones will also be introduced in new telephone designs. In line with existing trends, these new designs will have an increasing IC content. Eventually, it can be expected that the whole of the transmission circuit will be integrated, together with such functions as line interrupt dialling, two-tone dialling and automatic compensation for line length. The cost of providing the microphone amplifier in these new telephones will be minimal, since it will be incorporated within a larger multi-purpose IC.

For the next few years, it can be expected that the majority of electret microphones will be used as replacements for carbon transmitters. However, by the mid 1980s, use in new telephones is likely to be equally important, and thereafter will become the major application.

The microphone itself has some development potential. A likely line of development is to increase the physical dimensions of the device, thereby increasing the capacitance. For a given sensitivity, this would improve the noise performance of the device, and also reduce the difficulties of interfacing with the following amplifier.

ACKNOWLEDGEMENT

We would like to acknowledge the contribution made to this article by the members of the Telephone Group of the Mullard Application Laboratory, Mitcham, UK, who were responsible for the design and evaluation of the discrete amplifier.

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Application note

Asymmetric J-FET improves radio performance

Junction-gate Field Effect Transistors are now commonly used as r.f. amplifiers and mixers in radios because their nearly square-law transfer characteristic (V_{GS}/I_{DS}) results in lower intermodulation and distortion than is achievable from bipolar transistors with their exponential transfer characteristic. Moreover, their minimum noise figure is lower and, in low-current applications such as portables and car radios, the associated circuitry can be simpler and less dependent on supply voltage variations because biasing components are not necessary. For maximum gain and minimum noise, the common-source configuration is preferred. In this configuration, however, the inherent high feedback capacitance between the drain and substrate of a symmetric FET may cause instability. Although stability can be regained by using two FETs in a cascode circuit, such an arrangement results in increased complexity and noise, and it also requires a higher supply voltage.

Our new asymmetric n-channel J-FET type BF410 provides an inexpensive solution to the problem by combining low feedback capacitance with low h.f. noise. Furthermore, the forward transfer characteristic of the BF410 approximates a square-law over a much wider range of gate-source voltages than any other available FET. It can therefore handle larger input signals without causing undue non-linear distortion or intermodulation. These qualities make the BF410 particularly suited for use in the aerial and mixer stages of all classes of a.m. and f.m. radios and tuners.

CONSTRUCTION

The asymmetric construction of the BF410 is compared with that of a symmetric FET in Fig.1. The symmetric FET consists of a p^+p substrate upon which there is a low-resistivity channel region into which the drain, source and gate are diffused. The gate is connected, via a deep p^+ diffusion, to the substrate which forms the lower gate-channel junction. Since the structure is symmetrical, interchanging the source and drain connections causes little or no change of the electrical properties. With this construction, the desirable square-law transfer characteristic is only approached over a small portion of the gate-source voltage range. The feedback capacitance (C_{rs}) consists of the sum of the capacitance between drain and gate (minor part) and the capacitance between drain and substrate (major part).

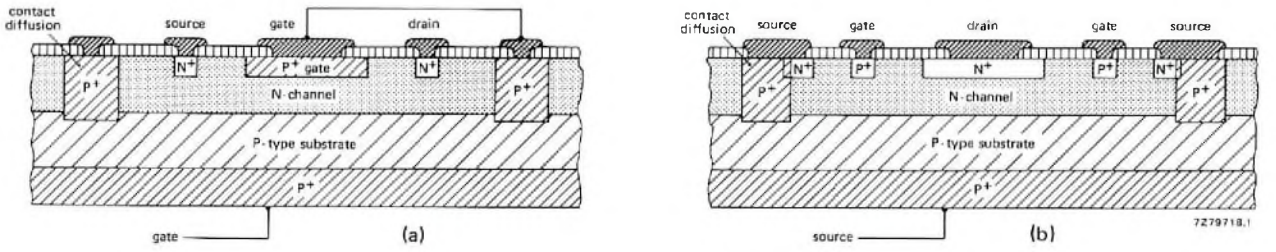


Fig.1 Cross-section of (a) a symmetric FET (e.g. BF256) and (b) an asymmetric FET

In the asymmetric BF410 construction, the substrate has a sub-region with a lower doping concentration than the channel region it adjoins. This prevents the diffusion of impurities. Since the source is connected, via a deep p^+ diffusion, to the substrate, the structure is asymmetrical and the source and drain can no longer be interchanged. These two constructional alterations considerably extend the range of gate-source voltages over which the transfer characteristic closely approximates a square-law but would normally halve the forward transfer conductance. This, however, is easily compensated by increasing the width of the gate. The feedback capacitance is smaller than that for the symmetric FET because it consists solely of the capacitance between drain and gate.

CHARACTERISTICS

For a FET with an ideal square-law transfer characteristic, the dependence of I_D on V_{GS} in the pinch-off region can be described by:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

where I_{DSS} is the drain current at $V_{GS} = 0$, and V_P is the pinch-off voltage.

The forward transfer conductance (g_{fs}) of this ideal FET can be derived from the previous equation as follows:

$$g_{fs} = \frac{dI_D}{dV_{GS}} = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) = -\frac{2}{V_P}\sqrt{I_{DSS}I_D}$$

This expression shows that g_{fs} has a linear dependence on V_{GS} and $\sqrt{I_D}$.

Figure 2 shows that the relationship between V_{GS} and g_{fs} is more linear for the BF410 than it is for a typical symmetrical J-FET such as the BF256. This is further exemplified by the second derivitive of I_D with respect to V_{GS}, which is shown as the parameter β in Fig.2. Ideally, β should remain constant during V_{GS} variations. Although this is not entirely so for either type of FET, Fig.2 shows that β is less dependent on V_{GS} for the BF410 than it is for the symmetric FET. The main differences between the electrical parameters of the BF410 and the symmetric BF256 are given in Table 1. Table 2 lists some of the most important electrical parameters of the BF410.

The BF410 is available in four selections of I_{DSS} as follows:

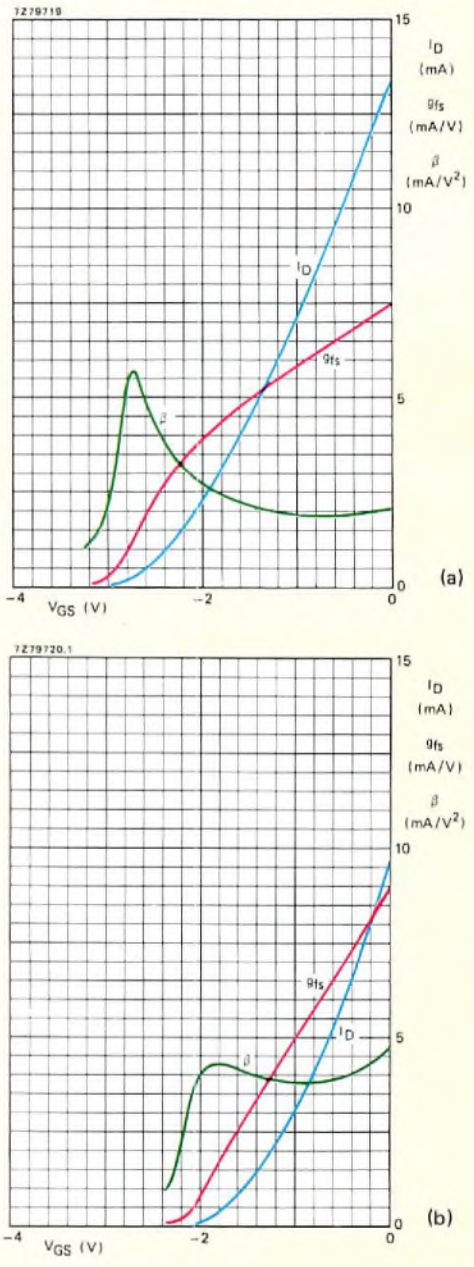


Fig.2 Plots of I_D, g_{fs} and β against V_{GS} for (a) the BF256 symmetric FET and (b) the BF410 asymmetric FET. The plots for g_{fs} and β illustrate clearly the superior square law transfer characteristic of the BF410

type number	I_{DSS} *(mA)*
BF410A	0.7 to 3
BF410B	2.5 to 7
BF410C	6 to 12
BF410D	10 to 18

The A, B and C versions are recommended for r.f. amplifiers in the f.m. section of high-class portables, car radios

and mains-powered radios respectively. The D version is recommended as a mixer for mains-powered radios and car radios.

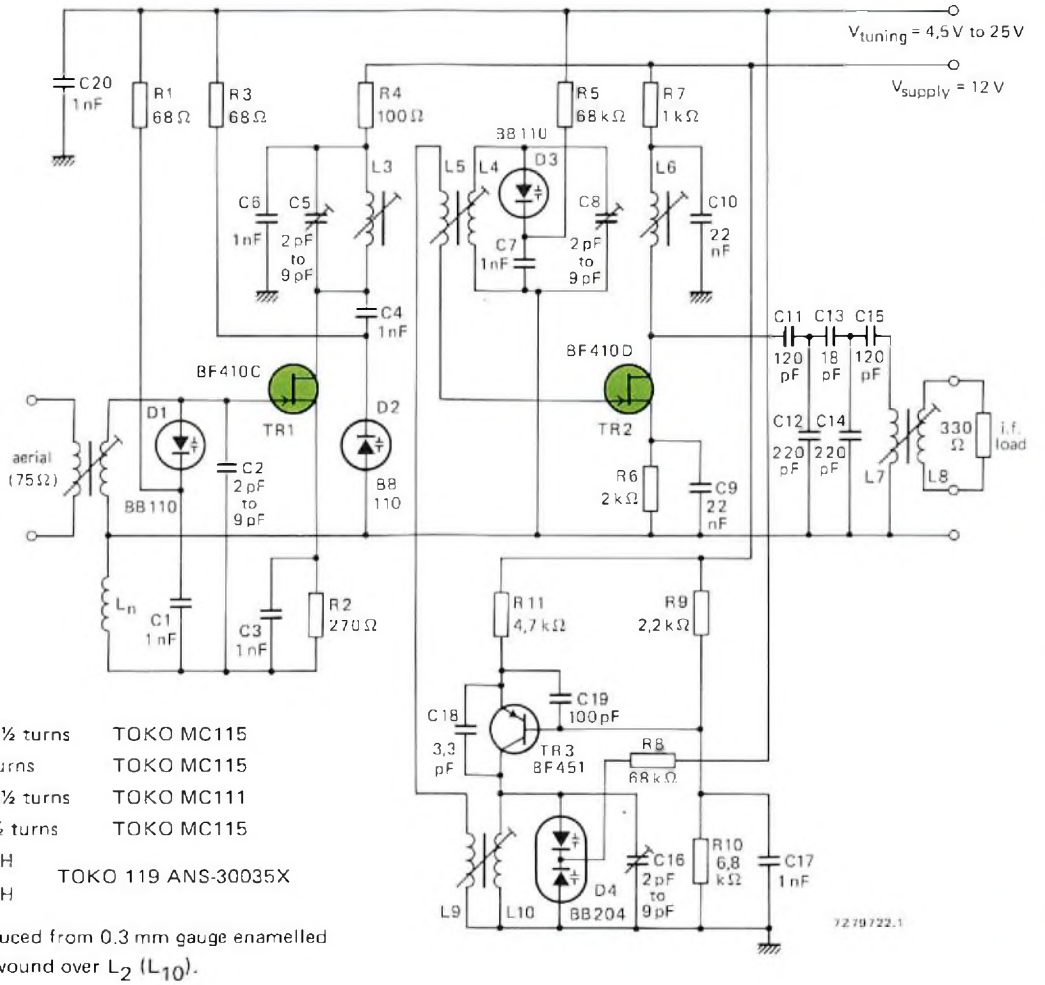
The BF410 is also available in microminiature versions for thick-film applications. These versions are in SOT-23 encapsulations and have the type numbers given on page 168.

TABLE 1
Typical BF410 and BF256 parameters

parameter	BF410	BF256
I_{DSS} (mA)	6.5	6.5
input capacitance C_{is} (pF)	3.0	3.8
output capacitance C_{os} (pF)	2.0	1.2
feedback capacitance C_{rs} (pF)	0.3	0.75
transfer admittance Y_{fs} (mA/V)	7.4	5.2
output conductance g_{os} (mA/V)	0.06	0.04

TABLE 2
Important electrical parameters of the BF410

drain-source voltage V_{DS}	>20 V
maximum drain current I_{Dmax}	30 mA
maximum power (up to T_{amb} = 75 °C)	300 mW
drain current I_{DSS} (at V_{GS} = 0 V, V_{DS} = 10 V)	0.7 to 18 mA
transfer admittance Y_{fs} (at I_{DSS}, and f = 1 kHz)	
A-type	>2.5 mA/V
B-type	>4 mA/V
C-type	>6 mA/V
D-type	>7 mA/V
feedback capacitance C_{rs} (at V_{DS} = 10 V)	<0.4 pF (typically 0.3 pF)
input capacitance C_{is} (at f = 1 MHz)	<5 pF
noise figure F at optimum source admittance (f = 100 MHz)	1.5 dB



$L_1 L_2^*$ = 1½/3½ turns TOKO MC115
L_3 = 3½ turns TOKO MC115
L_4/L_5 = 3½/2½ turns TOKO MC111
L_9/L_{10}^* = ¾/3½ turns TOKO MC115
L_6 = 2.8 μH
L_7/L_8 = 2.8 μH
TOKO 119 ANS-30035X

* L_1 (L_9) produced from 0.3 mm gauge enamelled copper wire wound over L_2 (L_{10}).

Fig.3 Circuit diagram of an FM tuner for a mains-powered radio

TO-92 variant	*SOT-23*
BF410A	BF510
BF410B	BF511
BF410C	BF512
BF410D	BF513

APPLICATIONS

The BF410 in a Mains-Powered f.m. Tuner

Figure 3 is the circuit diagram of the high-frequency section of a mains-powered f.m. tuner with variable-capacitance diode tuning. The r.f. amplifier is a BF410C and the mixer is a BF410D.

The r.f. stage

For circuit simplicity, the gate of the BF410C is directly connected to the secondary winding of the aerial transformer. This obviates the use of additional coils or components for providing a capacitive tap on the aerial transformer secondary winding. To achieve maximum gain and minimum noise, the common-source configuration is chosen for the BF410C. A bypassed bias resistor is connected in the source to reduce the I_{DS} spread. The r.f. stage is coupled to the mixer stage by double-tuned bandpass filter L_3/L_4.

For minimum noise in the r.f. stage, the input conductance G_S must be about 1 mA/V. Since the conductance of the aerial tuned circuit is only about 0.18 mA/V, the aerial must make the major contribution to G_S. However, this means that, if the aerial is disconnected, feedback may cause the stage to become unstable. Although this can be cured with a neutrodyne circuit in which the output tuned circuit is tapped, this would reduce the gain of the stage. The Rice method of neutralisation is therefore used in which the input tuned circuit is tapped. As shown in Fig.4, the neutralisation circuit isolates the input of the r.f. stage from its output by connecting input and output to opposite corners of an LC bridge network. The bridge is balanced and the circuit neutralised when $C_{os}/C_{rs} = L_a/L_n$. It has been found that the ratio C_{os}/C_{rs} remains reasonably constant at a value of about 8 in spite of a spread in the value of C_{os} and C_{rs}. Since the total inductance of the input tuned circuit must be $L_a + L_n = 88$ nH, it follows that the value of L_n must be 88 nH/9 ≈ 9.8 nH. Similarly, the value for L_a must be 9.8 nH × 8 = 78.4 nH. Since the required value for L_n is so small, it is formed by a track on the printed-wiring board thus avoiding the expense of a tapping on L_2.

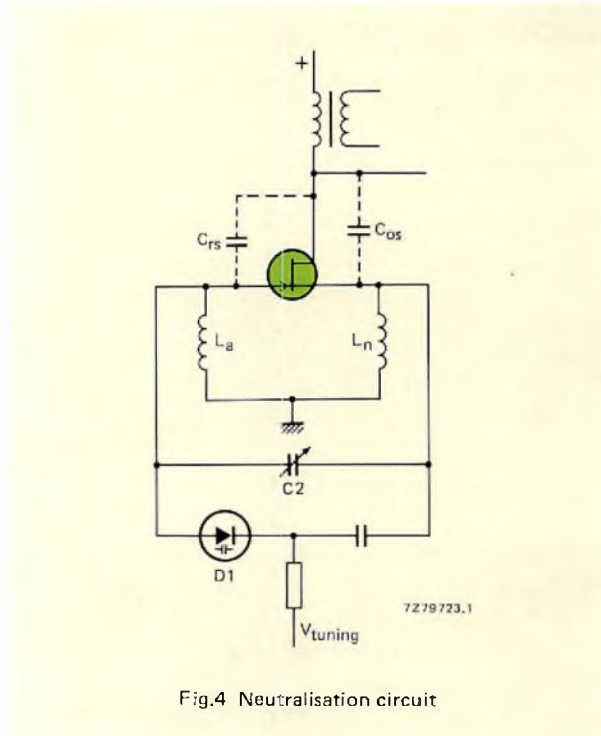


Fig.4 Neutralisation circuit

TABLE 3
Influence of L_n on Y parameters and stability factors for a typical BF410-C

parameter	without neutralisation (L_n = 0 nH)	with neutralisation (L_n = 9 nH)	with neutralisation (L_n = 10 nH)
Y'_{is} (mA/V)	0.06 + 18.5j	0.69 + 20.5j	0.78 + 20.7j
Y'_{fs} (mA/V)	$5e^{-10j}$	$5.6e^{-10j}$	$5.6e^{-10j}$
Y'_{rs} (mA/V)	$0.2e^{-90j}$	$0.054e^{-77j}$	$0.037e^{-68j}$
Y'_{os} (mA/V)	0.06 + 1.5j	0.10 + 1.5j	0.10 + 1.5j
s_1 (without aerial)	0.15	1.66	2.31
s_2 (with aerial)	0.54	2.83	3.79

The influence of neutralisation on Y parameters

Since the introduction of the neutralisation circuit influences the parameters of the r.f. stage, the parameters have been calculated without L_n, with $L_n = 9\,nH$ and with $L_n = 10\,nH$. The stability factor was also calculated with and without an aerial. For the purpose of these calculations, the capacitance of the trimmer capacitor C_2 and of the variable-capacitance diode D_1 were added to the input capacitance of the FET. The results of the calculations are given in Table 3. From Table 3, the ratio C_{OS}/C_{rs} is $1.5/0.2 = 7.5$. With this capacitance ratio, the value of L_n should be $88/8.5 = 10.3\,nH$. However, Table 3 shows that a high enough stability factor ($s_2 \approx 3$) is obtained with $L_n \approx 9.5\,nH$.

The mixer and local-oscillator

For maximum frequency stability, the conventional variable-capacitance diode tuned local-oscillator uses a bipolar transistor BF451 operating at an emitter current of 0.5 mA at $V_{CE} = 10\,V$. The oscillator has an output of 0.5 V which provides a good compromise between high conversion gain in the mixer and low radiation from the oscillator. The output from the oscillator is inductively coupled to the gate of the mixer via L_{10}, L_9 and L_5.

To achieve maximum conversion transconductance, a 2 kΩ resistor in the source of the mixer biases the stage so that the peaks of the 0.5 V local-oscillator signal just reach the pinch-off voltage. The amplified aerial signal is inductively coupled to the gate of the mixer via double-tuned bandpass filter L_3, L_4 and L_5. The 10.7 MHz i.f. output is limited to a bandwidth of 300 kHz by the filter in the drain of the mixer.

Performance of the tuner

The performance figures for the f.m. tuner are given in Tables 4 and 5. The double-beat suppression figures in Table 5 were measured with $f_1 = 94.35\,MHz$ and $f_2 = 98.63\,MHz$.

TABLE 4
Tuner performance at various frequencies

frequency	90	97.5	105	MHz
transducer gain	15.7	17.7	19.0	dB
noise figure	4.5	4.0	3.9	dB
repeat spot suppression*	77	77	78	dB
image rejection	74	72	68	dB
ΔV_{supply} for $\Delta f_{osc} = 20\,kHz$	±0.4	±2.4	±0.7	V
V_{aerial} for $\Delta f_{osc} = 20\,kHz$	0.28	1	0.2	V
osc. voltage on aerial	0.6	0.8	1.6	mV
osc. voltage on gate of mixer		0.5		V
i.f. 3 dB bandwidth		300		kHz

* Reference level 10 μV e.m.f. 75 Ω.

TABLE 5
Double beat suppression

f (MHz)	90.07	91.14	102.91
DBS (dB)	77	73	77

Battery-powered applications

When the BF410A or BF410B is used in high-class portable radios or car radios, it can often be used without biasing components as shown in Fig.5. The BF410 circuit then requires three resistors and two capacitors fewer than the equivalent bipolar circuit. The gain of the BF410 circuit is then more independent of supply voltage reduction than that of the bipolar circuit. For example, the gain remains almost unchanged if the battery voltage is halved.

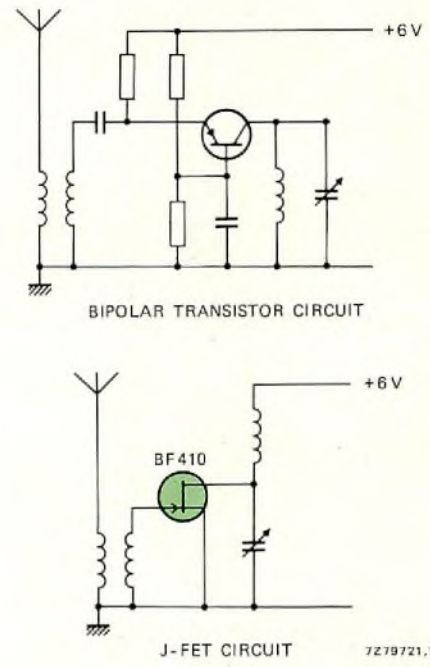


Fig.5 Two r.f. input stages showing the simplicity of the FET circuit compared with that of the bipolar transistor circuit.

Digital control of radio and audio equipment

Part 7 - RTS tuning controls and the microcomputer

W. HESSE and U. SCHILLHOF

In EC&A Vol. 1, No. 4 we introduced the Radio Tuning System (RTS) and described how the tuning voltage is generated using programmable frequency divider SAA1059 and PLL frequency synthesiser SAA1056. In EC&A Vol. 2, No. 1, the control position and frequency displays for RTS were described. This article continues the theme by presenting one of the many methods by which a microcomputer can control the tuning functions of the RTS in an a.m./f.m. radio.

One of the main advantages of RTS is its modular construction from a series of LSI circuits, all of which are microcomputer compatible. This allows a wide variety of control systems to be constructed to suit the individual requirements of manufacturers or different classes of equipment. The number of control facilities available to the user and the sequence in which the user-commands are executed depend entirely on the type of microcomputer used and on the program stored in its ROM. This article describes a basic tuning control system using an 8048 microcomputer together with an HEF4720 LOCMOS RAM for storing user-variable data. The software for the microcomputer was primarily developed for laboratory evaluation of the RTS. In due course, we will develop more RTS microcomputer programs to meet the specific requirements of radio manufacturers.

THE BASIC RTS

In the basic microcomputer-controlled RTS shown in Fig.1, a phase-locked loop maintains stable, accurate tuning of the a.m. and f.m. broadcast bands. The local-oscillator signal from the tuner is passed to a frequency divider with a programmable division ratio. The output from the divider is compared with a stable reference frequency. The comparator output, which represents the tuning error, is then amplified and filtered before being used to modify the tuning voltage for the local-oscillator, thereby completing the control loop. The listener changes the tuned frequency by keying-in the required broadcast frequency or by manual or search tuning. These commands cause the microcomputer to calculate the appropriate division ratio after compensating for the i.f. of the tuner.

The tuned frequency ($f_{osc} - f_{i.f.}$) is displayed in a 4½-digit, 7-segment LED numeral indicator. Two additional LEDs indicate whether the displayed frequency is in kHz (a.m.) or MHz (f.m.). The frequency and kHz/MHz indicators are driven by an SAA1060 LED display interface circuit controlled by the microcomputer bus.

Variable functions such as preset tuning data and i.f. offset data are stored in a LOCMOS RAM HEF4720. A rechargeable back-up battery makes this memory non-volatile. Preset programme numbers and selected wave-

Laboratory model of an a.m./f.m. tuner incorporating the RTS described in this article

band are indicated by LEDs which can be driven by an Output Port EXpander (OPEX) SAA1061 or by another SAA1060 operating in the static mode. The same i.c. controls the waveband switching in the tuner. The SAA1060 and SAA1061 are pin and function compatible for static displays.

The 1K×8 program memory of the 8048 microcomputer allows the construction of a very versatile and easy to operate radio tuning system.

THE MICROCOMPUTER PROGRAM

Operating facilities provided by the program

The versatility and ease of operation of the RTS is entirely determined by the software mask-programmed into the 1K×8 program ROM of the microcomputer. The system evaluation program, on which this article is based, provides the following facilities:

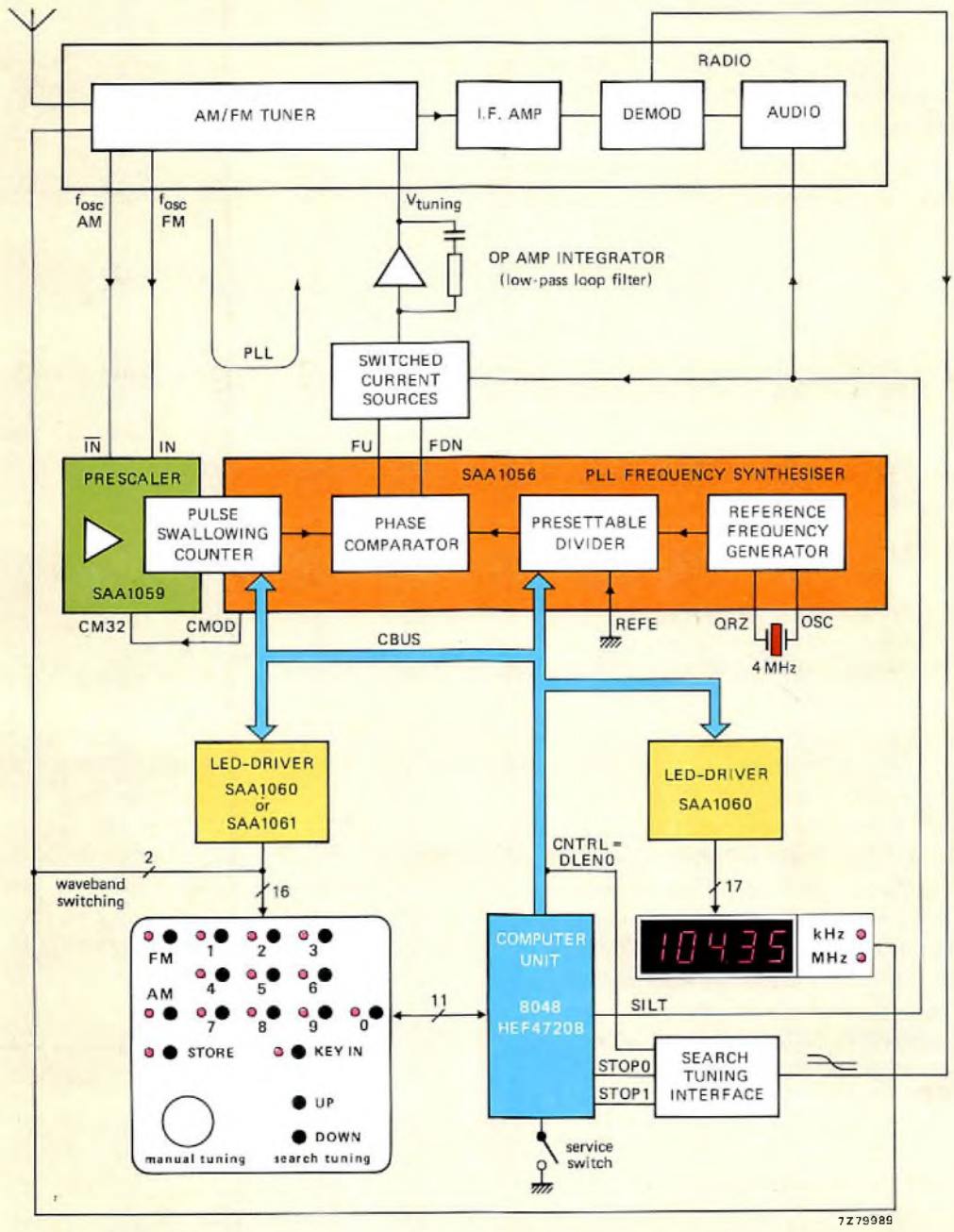


Fig.1 A basic microcomputer-controlled RTS. The manual tuning can be controlled via up/down, slow/fast pushbuttons or via a shaft-position encoder rotated by a tuning knob

- When the tuner is switched on, it returns to the operational and display state that existed at the time of switching off.
- The wavebands can be manually selected with two pushbuttons. On changing the waveband, the system automatically tunes to the frequency that was previously tuned on the selected waveband.
- A station can be tuned by pressing a key-in pushbutton and then entering the required frequency with ten data entry pushbuttons. The previously tuned programme is not interrupted during this procedure and the new frequency is not tuned until the key-in pushbutton is pressed a second time. If an invalid frequency is entered, the system tunes to the upper or lower band limit.
- A station can be tuned with a manual tuning knob or up/down slow/fast pushbuttons. The angular position of the tuning knob is converted into up/down tuning pulses for the microcomputer by a shaft-position encoder.
- Bidirectional search tuning of the f.m. band with muting of interstation noise and automatic stop on reaching a station satisfying pre-determined criteria. This mode is initiated by pressing a search-up or search-down pushbutton. The system automatically returns to the opposite end of the band when the search reaches the upper or lower frequency limit.
- The frequencies of up to ten stations can be stored for subsequent preselection. The preset frequencies can be freely selected from either waveband according to the wishes of the listener. The waveband of the preset station is automatically selected when the frequency is recalled.
- A service switch is provided for adjusting the i.f. offset frequency so that the system can be matched to tuners with a range of a.m. and f.m. intermediate frequencies. The nominal intermediate frequencies are 460 kHz for a.m. and 10.7 MHz for f.m. The system is adapted for other intermediate frequencies by operating the service switch (not accessible to the listener). The i.f. is then displayed on the frequency indicator. The i.f. can be altered by operation of the manual tuning control after which the new frequency is automatically stored in the external memory. The limits of adjustment are 10.56 MHz to 10.87 MHz for f.m. and 448 kHz to 479 kHz for a.m.

The sequence of the main program

The main part of the system evaluation program shown by the flow chart of Fig.2 is initiated when the tuner is switched on. If the program were to step sequentially through all 1024 instructions in the resident ROM of the microcomputer, the program execution would be slow and inefficient. The program therefore incorporates a number of conditional jumps and instructions to call subroutines. In some cases, these subroutines call other subroutines. For clarity, the subroutines are not shown in Fig.2.

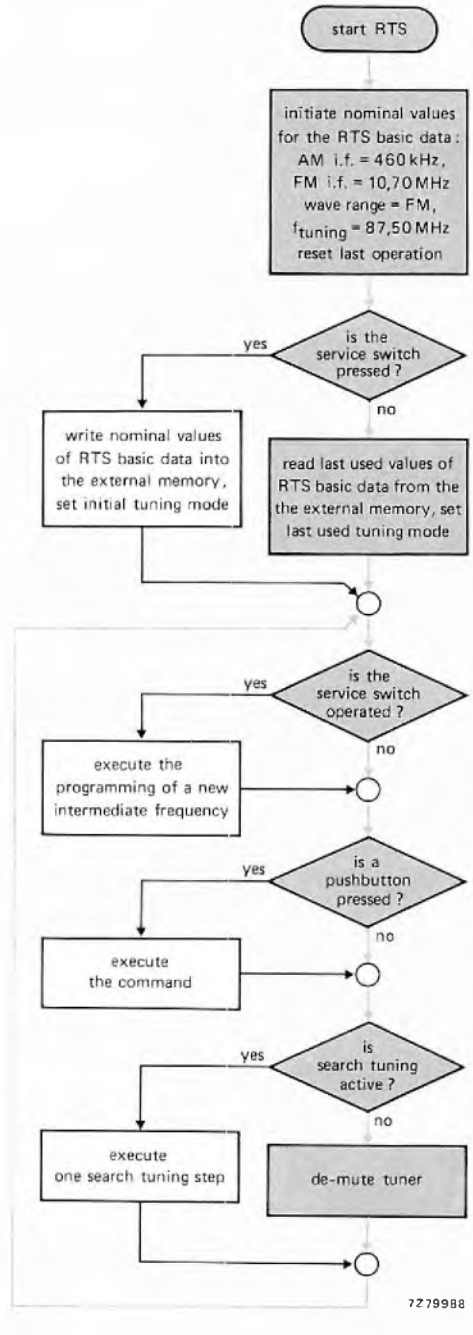


Fig.2 Flow chart for the main part of the computer program used to evaluate the RTS

When the RTS is switched on, the last key operation is reset, the tuner is muted and nominal values for the RTS basic data are transferred from the ROM to the RAM in the microcomputer. These nominal values are:

a.m. intermediate frequency:	460 kHz
f.m. intermediate frequency:	10.7 MHz
waveband:	f.m.
tuned frequency:	87.5 MHz

The next operation depends on whether or not the service switch is operated. If it is not, the data that was stored in the external memory at the time of switching off are read out and the tuned frequency and displays are set to the state that existed when the tuner was last used. If no further pushbuttons are operated, the tuner is de-muted and the remaining part of the program then forms a loop which is repeatedly processed until a pushbutton is pressed or the manual tuning knob is rotated.

If the external memory contains invalid data because the back-up battery has expired or has been replaced during servicing, the service switch must remain closed whilst the tuner is being switched on. The nominal values for the RTS basic data are then written into the external memory. When the tuner has switched on, it operates on 87.5 MHz but the nominal value for the i.f. for the f.m. band (10.7 MHz) is displayed. If necessary, the tuning control can be used to program new intermediate frequencies for f.m. and a.m. When the service switch is opened again, normal operation of the tuner ensues.

As an example, the repetitive processing of the main loop of the program can be halted by selecting a preset programme (e.g. programme 5) by pressing one of the data entry pushbuttons 0 to 9. The program then branches from the main loop after the second circulation and executes the key command as follows:

- The tuner is muted.
- The selected programme number and associated programme number indicator data is stored in the external memory. This allows the microcomputer to tune to the selected programme if the tuner is switched off and subsequently switched on again.
- The preset frequency associated with pushbutton 5 is read out of the external memory.
- The selected waveband is decoded and the frequency data is checked against the limits of the decoded waveband.
- The preset programme number and waveband data are loaded into the programme number and waveband display driver SAA1060 or SAA1061. This IC lights the LED indicator associated with pushbutton 5 and, if necessary, switches the waveband in the tuner and changes the a.m./f.m. display.
- The PLL dividing number for the selected preset frequency is calculated by the microcomputer and loaded into the shift register of the synthesiser SAA1056.
- The microcomputer converts the selected preset frequency into 7-segment display data and loads it into the frequency display driver SAA1060.
- After 300 ms, the tuner is de-muted and the program returns to the main loop.

To simplify the operating procedure for the RTS, the sequence of the microcomputer program and the position of the return addresses have been selected so that some functions have priority over others. For example, if the search tuning is operative, the program returns to the start of the main loop after executing each frequency increment of the search. Search tuning is therefore discontinued if any other pushbutton is pressed.

The data transfer between the microcomputer and its peripherals is transmitted in serial form as required by all of the integrated circuits of the RTS.

THE COMPUTER UNIT

The circuit diagram of a typical RTS computer unit using an 8048 microcomputer and an HEF4720 external memory with rechargeable back-up battery is given in Fig.3. The unit is made fail-safe during supply voltage interruption as follows.

The 5 V stabilised supply Vp5 and power available signal POW are derived from a separate stabilised supply unit. When the RTS is switched on, POW goes HIGH after the 5 V supply has stabilised. If the input voltage to the stabiliser is interrupted (e.g. due to mains drop-out), POW goes LOW (<1 V) about 15 ms before the 5 V output from the stabiliser starts to decrease. This turns-off TR_2, thereby causing TR_2 to conduct and reset the microcomputer at its $\overline{\text{RESET}}$ input. Because TR_2 is turned off, the tuner is muted (SILT = HIGH) and TR_3 conducts, thereby connecting the write address and write enable inputs of the external memory to the common rail via diodes and turning off TR_5. The HIGH level at the collector of TR_5 disables the external memory at its Chip Select input $\overline{\text{CS}}$.

If the supply interruption occurs during memory access, TR_1 holds TR_2 conducting during the data transfer which will always be completed before the 5 V supply strarts to fall because the memory access time is only about 10 ms.

Transistors TR_6 to TR_{13} separate the address inputs of the memory from non-operated switches of the push-button matrix, thereby minimising radiation from the unit.

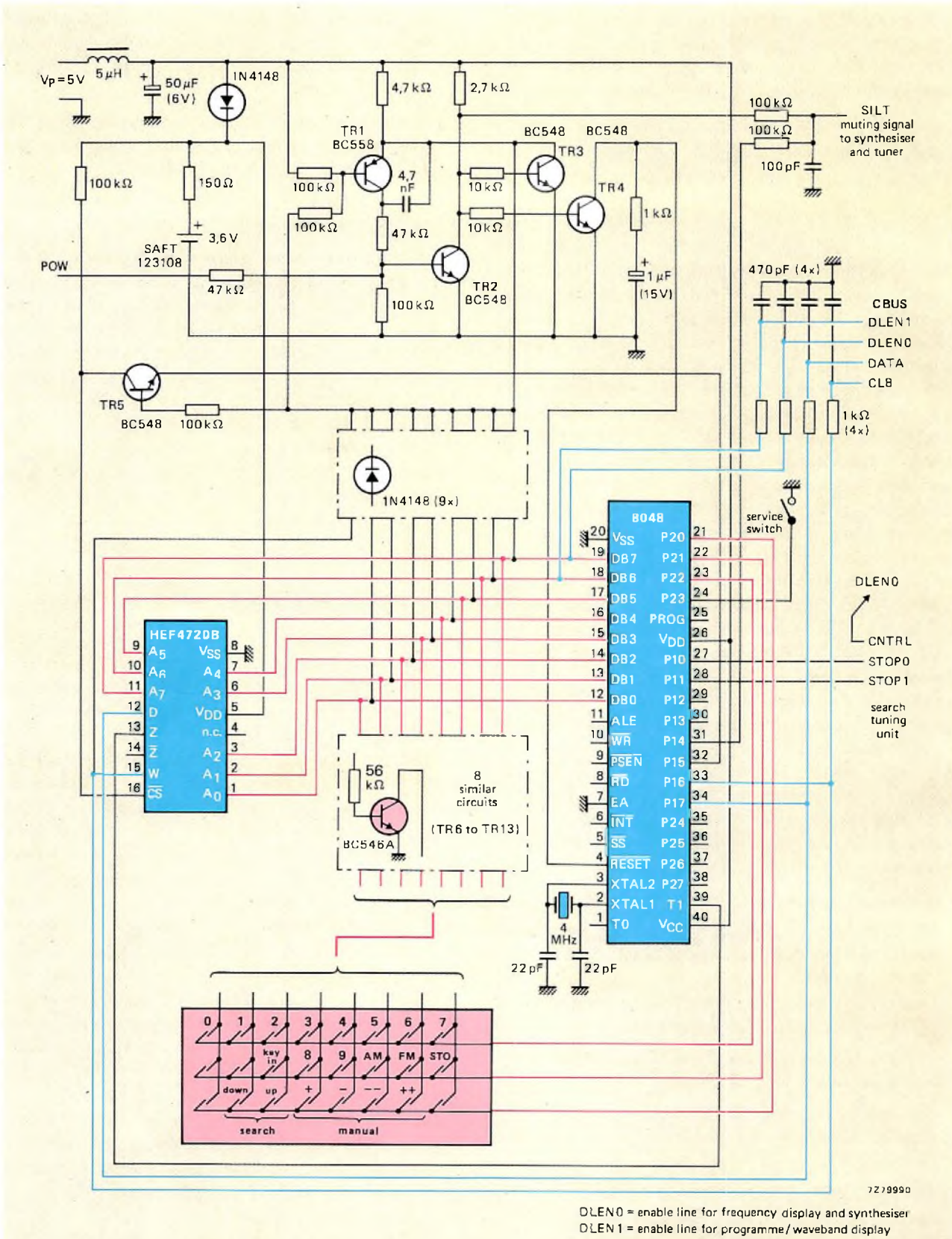


Fig.3 Circuit of the computer unit

Interrupted current-loop dialling for pushbutton telephones

J. FASSER and A. M. HODEMAEKERS

The traditional telephone dial interrupts the line current at a rate of ten times a second, thereby generating a train of current pulses for each dialled digit. Since the pulses are generated during the return of the dial, a new digit cannot be dialled until the previous one has been pulsed out. The method is therefore slow. To speed it up, and thereby make more efficient use of the exchange facilities, modern telephone exchanges incorporate decoders which can accept dialling signals from telephone sets with pushbutton keyboards and two-tone dialling circuits (see Electronic Components and Applications Vol. 1, October 1978).

Since many subscribers now prefer a pushbutton telephone, there is also a requirement for a circuit which can convert pushbutton keyboard entries into streams of correctly-timed line current interruptions, thus allowing pushbutton telephones to be used with exchanges not yet equipped with two-tone decoders. Either of the new integrated circuits MH320 and MH323 can be used for this purpose.

When a telephone number is dialled via a keyboard, it is possible to enter the digits faster than they may be transmitted for interrupted-current-loop dialling. The MH320 and MH323 therefore incorporate a RAM for storing the entered digits before they are transmitted as an accurately-timed stream of dialling pulses. Since the RAM can retain up to 23 digits after the call has been completed, the previously dialled number can also be automatically redialled by pressing a single pushbutton (#) on the keyboard. When the handset is replaced on the cradle after a call, the circuit automatically assumes a static standby mode of operation during which the normal 40 μA current consumption is reduced to about 1 μA and a back-up supply ensures retention of the memory contents. This back-up supply can be provided from the telephone lines via a high-value resistor bridging the cradle contacts; from a rechargeable battery, or from a temporary charge held by an electrolytic capacitor.

For the last seventy years, rotary electro-mechanical telephone dials have been faithfully dialling numbers by interrupting the current in the telephone lines. The much heavier traffic that must be handled by modern exchanges has resulted in the introduction of a much faster dialling system using combinations of two audio frequency tones generated by electronic pushbutton telephones. Meanwhile, integrated circuits MH320 and MH323 merge the old with the new by allowing pushbutton telephones to be used with exchanges not yet equipped with decoders for two-tone dialling

The main difference between the MH320 and the MH323 is that the MH323 also incorporates an automatic access pause system. If, during the original dialling sequence, the subscriber pauses to await a trunk exchange access tone, this system, if enabled, will regenerate the access pause as a pre-determined interval during any subsequent automatic redialling of the number. One or two access pause codes can be automatically stored for redialling in this way. Alternatively, the automatic access pause storage system can be inhibited and any number of access pause codes manually stored for redialling by pressing the access pause pushbutton (★) during the access pause(s) in the original manual dialling sequence. If required, the access pauses in the automatic redialling sequence can be prematurely terminated on hearing the access tone by pressing the redial pushbutton (#) for a second time. This entry is then decoded as an access pause reset. Automatically regenerated access pauses can also be shortened or lengthened under the control of an additional tone recogniser circuit.

The following main features are common to both integrated circuits:

- Operation from 2.5 V to 6 V supply.
- Typical current consumption of only 40 μA during a call.
- When the handset is replaced, the Chip Enable input detects the line current interruption after 1.6 dialling pulse periods. The circuit then assumes a static standby mode of operation during which the current consumption is reduced to a typical level of 1 μA.
- The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix.
- High input noise immunity. Keyboard entries are not accepted until they have been debounced on the leading edge. Further keyboard entries are inhibited until the previous entry has been debounced on the trailing edge.
- If a back-up supply is provided, numbers with up to 23 digits can be automatically redialled by operation of a single pushbutton on the keyboard. If the original number contained more than 23 digits, it will have been transmitted but the redialling facility is then disabled.
- The normal dialling pulse frequency of 10 Hz with a mark/space ratio of 2:3 can be increased to 932 Hz for test purposes. The pulse timing is controlled by an on-chip 3.58 MHz oscillator with external crystal. The system can also be synchronised with clock pulses from an external source.
- Hold facility allows inter-digit period to be lengthened under the control of external equipment.
- All inputs (except Chip Enable) are internally pulled up or down to the inactive state when they are not being driven.
- All inputs are internally protected against electrostatic charges.
- Up to two fixed-duration access pauses can be automatically stored for redialling if the subscriber includes access pauses in the original dialling sequence. Alternatively, any number of access pause codes can be stored for redialling if the subscriber presses the access pause pushbutton (★) during the original manual dialling sequence. During redialling, the access pause(s) can be prematurely terminated by pressing the redial pushbutton (#) again, or they can be shortened or lengthened by an external tone recogniser operating in conjunction with the hold facility.
- The period after which a line current interruption causes operation in the standby mode can be set to 1.6 or 3.2 dialling pulse periods.
- The dialling pulse frequency can be set to 10 Hz, 16 Hz, 20 Hz or 932 Hz (test frequency).
- The mark/space ratio of the dialling pulses can be set to 2:1 or 3:2.
- The access pause can be set to one of two durations.

CLOCK PULSE GENERATION AND PULSE TIMING

The integrated circuits incorporate a 3.58 MHz crystal-controlled oscillator followed by a frequency divider. In the MH320, the division ratio can be externally set to provide one of two clock pulse frequencies. In the MH323, one of four clock pulse frequencies can be selected. The divider is followed by a timing counter which generates one dialling pulse for every thirty clock pulses. In the MH320, the mark/space ratio of the dialling pulses is fixed at 3:2. In the MH323, it can be externally set to 3:2 or 2:1.

If required, the crystal input pin can be driven from an external source to provide dialling pulse frequencies that are not normally available. In the MH323 the clock pulses are available at an output pin. This pin can be forced from an external source to provide dialling pulse frequencies that are not normally available.

The pulse timing for the two integrated circuits are given in Tables 1, 2 and 3.

FUNCTIONAL DESCRIPTION OF THE DIALLING SYSTEM

The following functional description is based on the block diagram given in Fig.1 and follows the usual sequence of making a telephone call.

TABLE 1
Clock pulse and dialling pulse frequencies (f_{osc} = 3.58 MHz)

freq. selection input F01	F02	f_{DP} (Hz)	T_{DP} (ms)	f_{CL} (Hz)	T_{CL} (ms)
LOW	HIGH	19.42	51.5	582.6	1.72
HIGH	HIGH	15.54	64.4	466.1	2.15
LOW	LOW	10.13	98.7	303.9	3.30
HIGH	LOW (test mode)	932.20	1.073	27965	0.036

Coloured figures apply to MH323 only.

f_{DP} = dialling pulse frequency
T_{DP} = dialling pulse period
f_{CL} = clock pulse frequency
T_{CL} = clock pulse period

TABLE 2
Dialling sequence intervals with fixed duration

clock start-up time (typical):	t_{on}	4 ms
prepulse duration (typical):	t_d	$10T_{CL}$
initial data entry time (min):	t_i	$t_{on} + 4T_{CL}$
initial data entry time (max):	t_i	$t_{on} + 5T_{CL}$
subsequent data entry time (min):	t_e	$4T_{CL}$
subsequent data entry time (max):	t_e	$5T_{CL}$

For T_{CL}, see Table 1.

TABLE 3
Dialling sequence intervals with selectable duration

function	control input		state of control input HIGH	LOW
Dialling pulse mark/space ratio	M/S			
break time (mark):		t_b	$18T_{CL}$	$20T_{CL}$
make time (space):		t_m	$12T_{CL}$	$10T_{CL}$
mark/space ratio:		$t_b:t_m$	3:2	2:1
Inter-digit pause selection	IDP			
inter-digit pause:		t_{id}	$9T_{DP}$	$8T_{DP}$
Reset delay selection	RDS			
reset delay:		t_{rd}	$3.2T_{DP}$	$1.6T_{DP}$
Access pause duration	APD			
access pause:		t_{ap}	$64T_{DP}$	$32T_{DP}$

Coloured figures apply to MH323 only.

For T_{CL} and T_{DP}, see Table 1.

Operating modes

The integrated circuits have three modes of operation which will be frequently referred to during the functional description. They are:

The static standby mode during which the Chip Enable (CE) input is LOW and the handset is on the cradle so that the telephone set is disconnected from the line by the cradle contacts. The previously dialled number remains stored in the RAM for possible redialling as long as a back-up supply maintains the level of V_{DD} above V_{DDO}. In this mode, the normal current consumption of 40 μA is reduced to 1 μA to minimise the current drain from the back-up supply. The Read Address Counter (RAC) is set at its starting position. The clock pulse

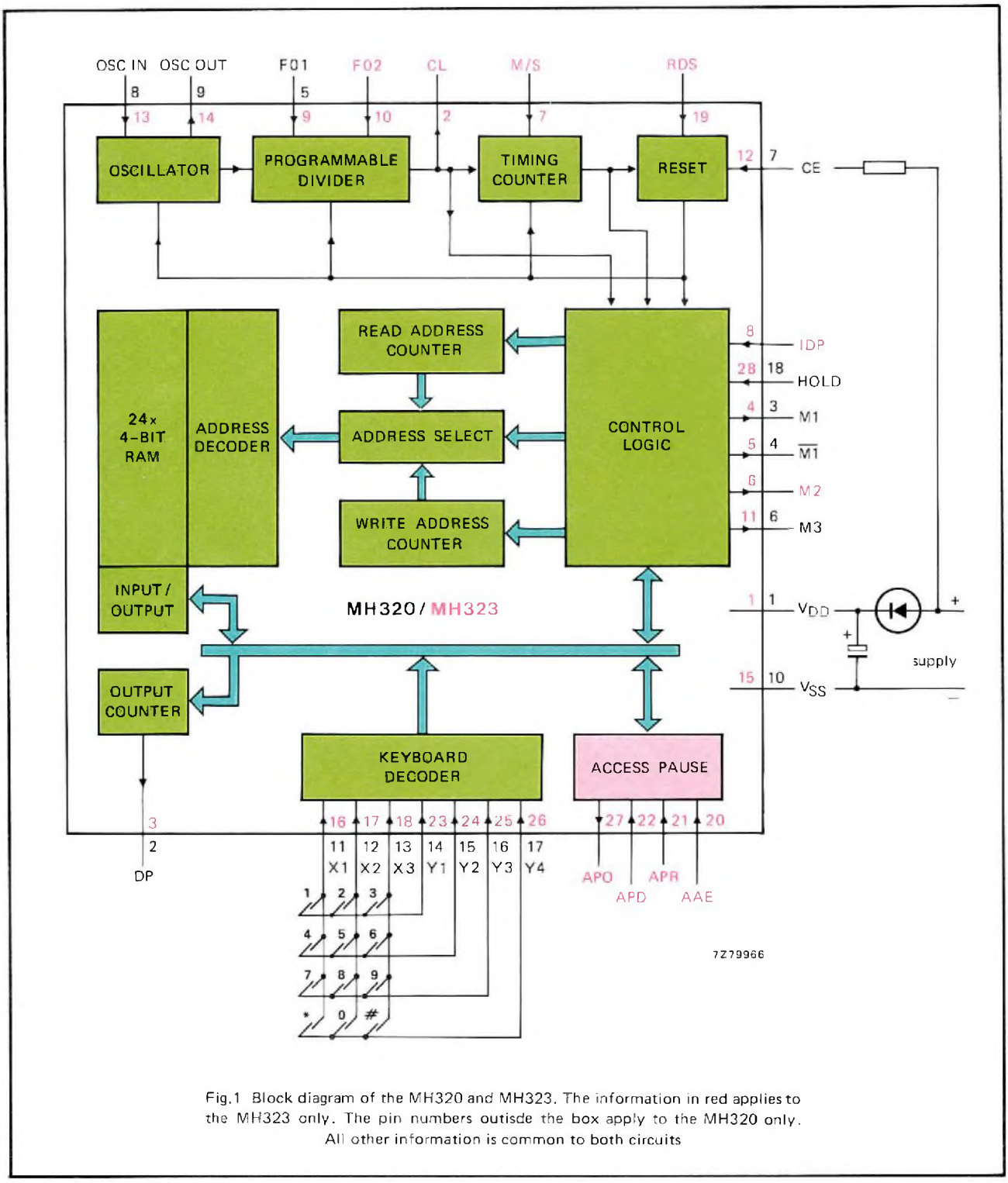


Fig.1 Block diagram of the MH320 and MH323. The information in red applies to the MH323 only. The pin numbers outisde the box apply to the MH320 only. All other information is common to both circuits

generator and keyboard decoder are disabled. The Write Address Counter (WAC) contents equals the number of digit codes stored in the RAM.

The conversation mode during which CE is HIGH because the handset has been lifted. The muting output M1 is inactive so that speech or dialling tones can be heard. Keyboard entries can be accepted.

The dialling mode starts after the first keyboard entry either initiates an automatic redialling sequence or enters the first digit of a new number for storage in the RAM. The previously stored or newly entered keycodes are read from the RAM and regenerated as correctly-timed dialling pulses at output DP. In this mode, the telephone is muted because output M1 goes HIGH after the first pushbutton operation.

Initiating a telephone call

A telephone call can be initiated under either of the following two conditions:

– The supply to the integrated circuit is derived from the telephone lines via the cradle contacts. A timing diagram for this situation is given in Fig.2.

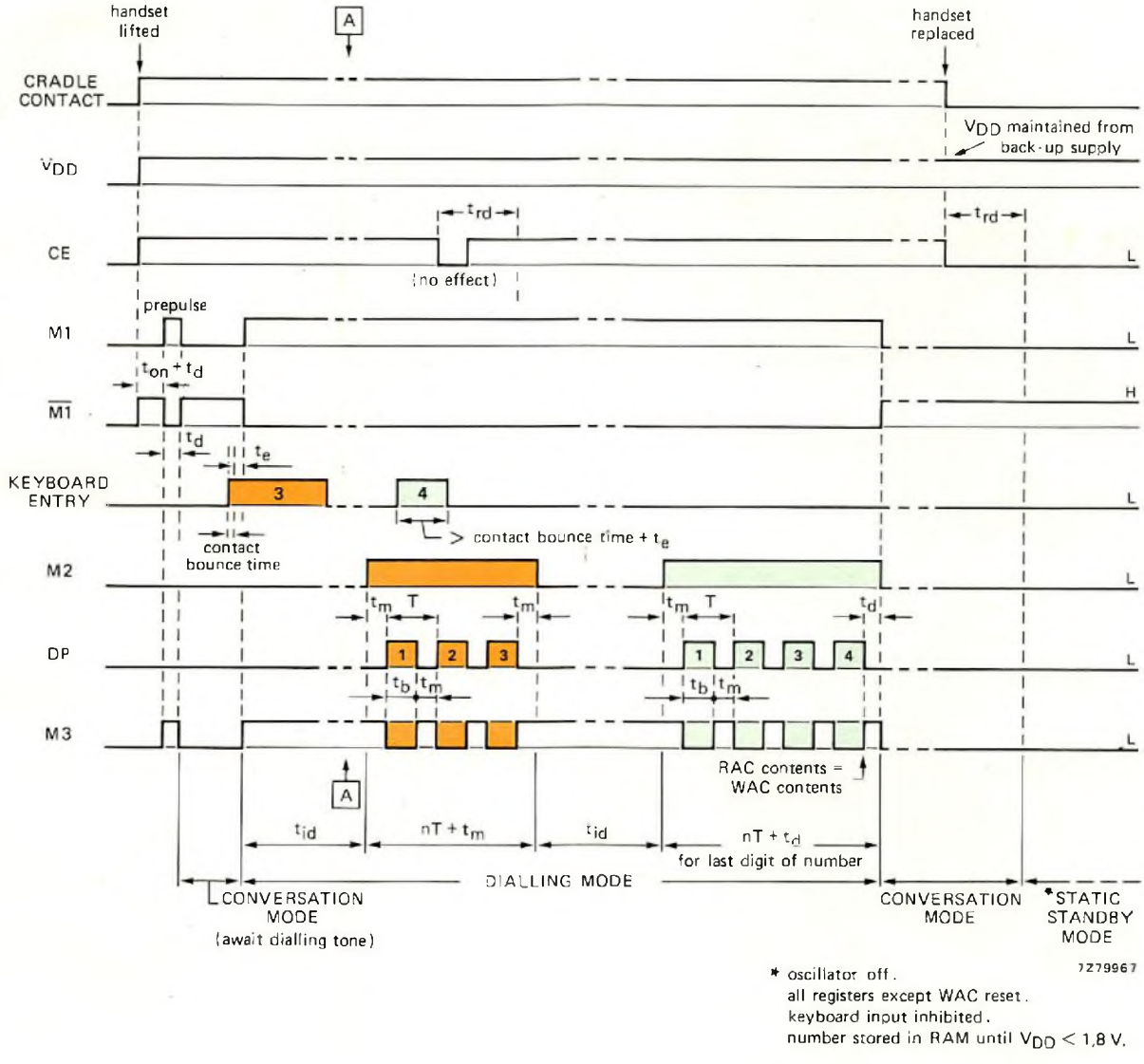


Fig.2 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts)

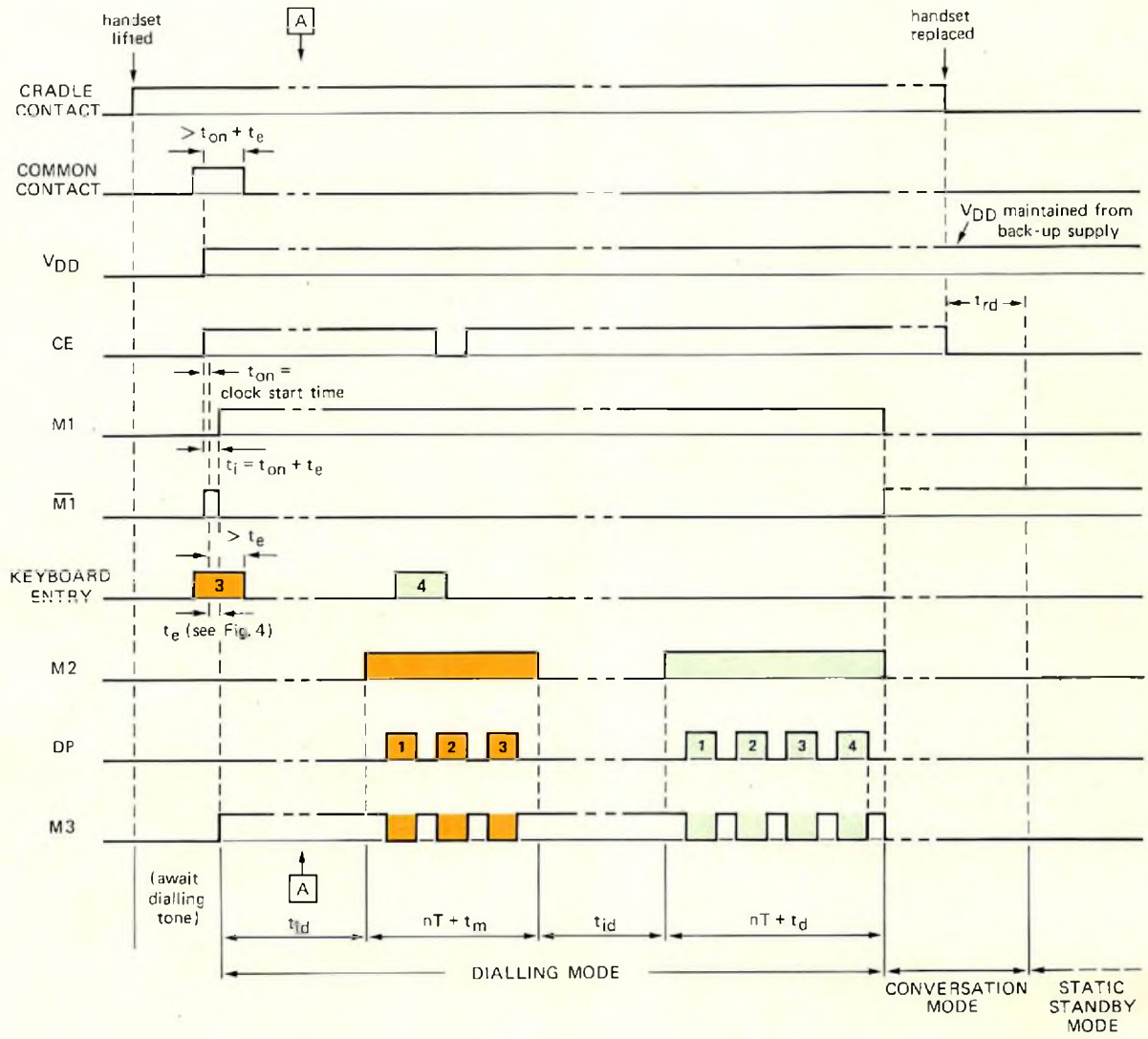


Fig.3 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. When the pushbutton is released, the supply to V_{DD} and CE is maintained by the muting circuit controlled by output M1. See Fig.2 for pulse timings after point A.

– The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact. A timing diagram for this situation is given in Fig.3.

In Fig.2, when the handset is lifted, the supply to V_{DD} and CE is provided via the cradle contacts. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at outputs M1 and M3. This prepulse ensures that, if a polarised muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

In Fig.3, when the handset is lifted, the circuit is in the static standby mode with the level of V_{DD} dependent on the level of the back-up supply. Since M1 is LOW, the telephone is de-muted so that the subscriber can await the dialling tone. When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can then be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

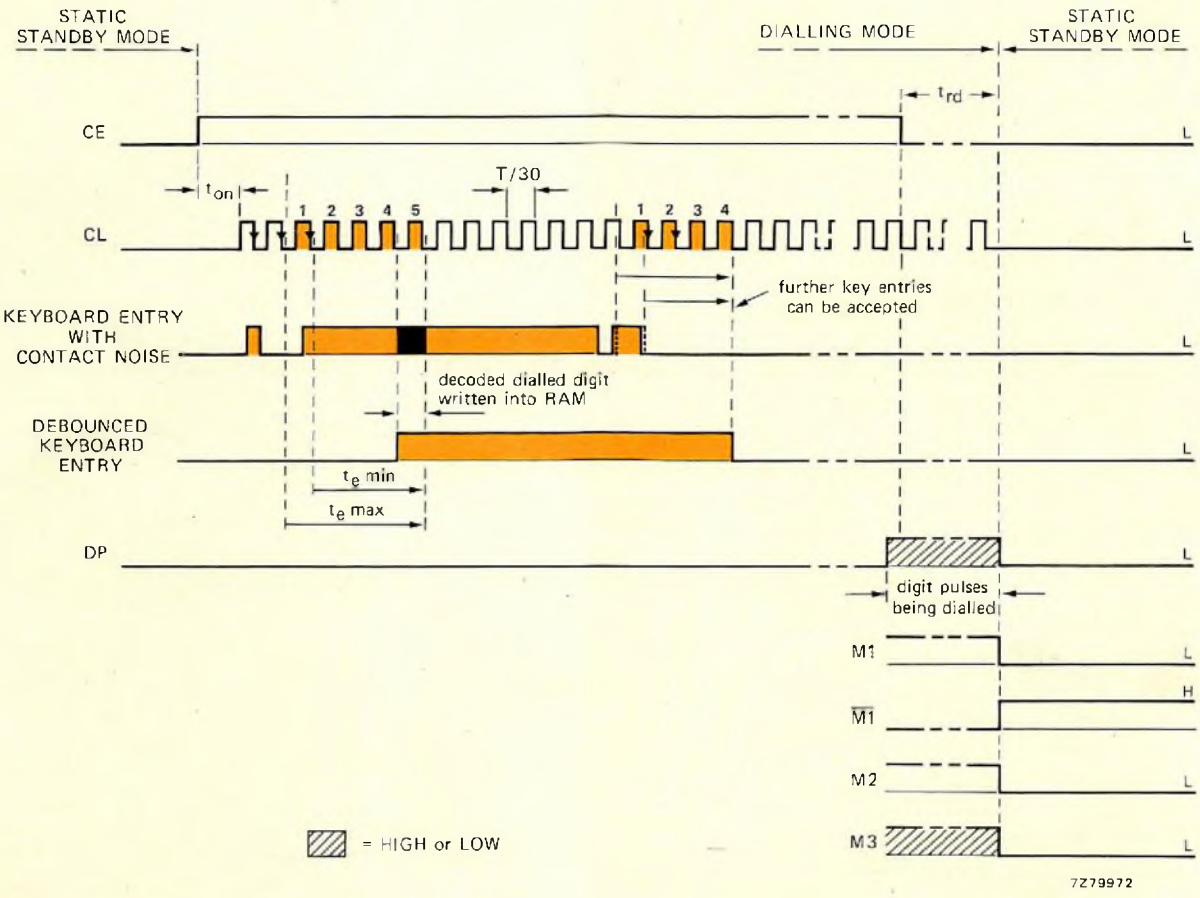


Fig.4 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses

Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 keyboard matrix (with or without common contact) as shown in Fig.1. An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig.4.

Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the RAC is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding

keycode is written into the first RAM location, and the WAC is then incremented by one. Subsequent keyboard entries each cause the WAC to be incremented by one after each keycode has been written into the RAM. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycodes replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

Memory recall for redialling

If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. After each keycode has been recalled, the RAC is incremented by one. Since the WAC has not been reset since the last number was written into the RAM, the WAC and RAC contents will be equal when all of the stored keycodes have been recalled from the RAM. The circuit will then revert to the conversation mode after 10 clock pulses (t_d).

If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the MH323.

Dialling sequence

The dialling sequence will be described with the aid of Fig.2. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode and the subscriber awaits the ringing tone and completes the call.

The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1.6 or 3.2 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1.8 V. Shorter interruptions of CE (e.g. dialling pulses superimposed on CE) do not have any effect. If a back-up supply is not used (no automatic redialling facility), a capacitor must be connected between V_{DD} and V_{SS} to ensure that the line current interruptions caused by the dialling pulses do not interrupt the supply voltage to the circuit.

Hold function

As shown in Fig.5, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in the RAM. No further keycodes will be read from the RAM and converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

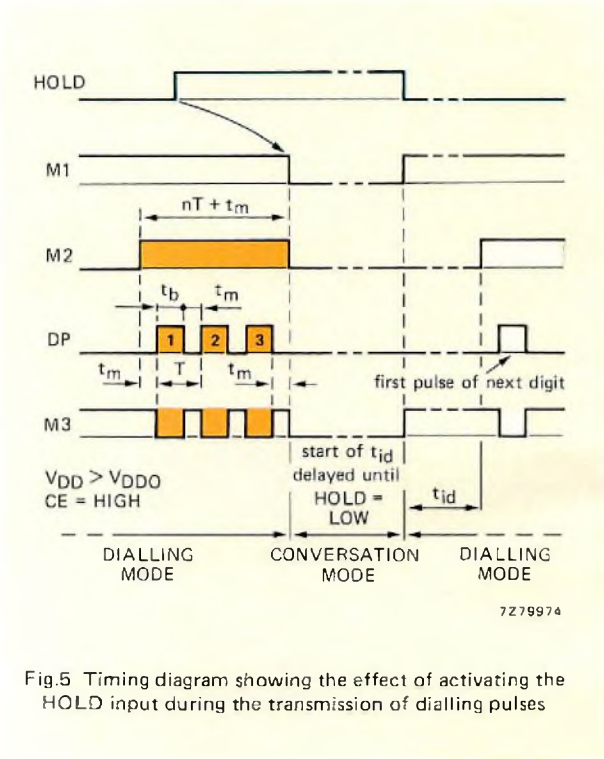


Fig.5 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses

ACCESS PAUSE GENERATION

As previously explained, M1 goes LOW and the circuit assumes the conversation mode when all of the previously entered digits have been pulsed out as indicated by the equality of the contents of the WAC and the RAC. This is the point at which the subscriber awaits the access tone when making a trunk call and then, after hearing the tone, makes further keyboard entries. In the MH320, the subsequent keyboard entries will be decoded and written into the RAM but, during redialling, the access pause will be regenerated as the standard inter-digit pause of eight dialling pulse periods.

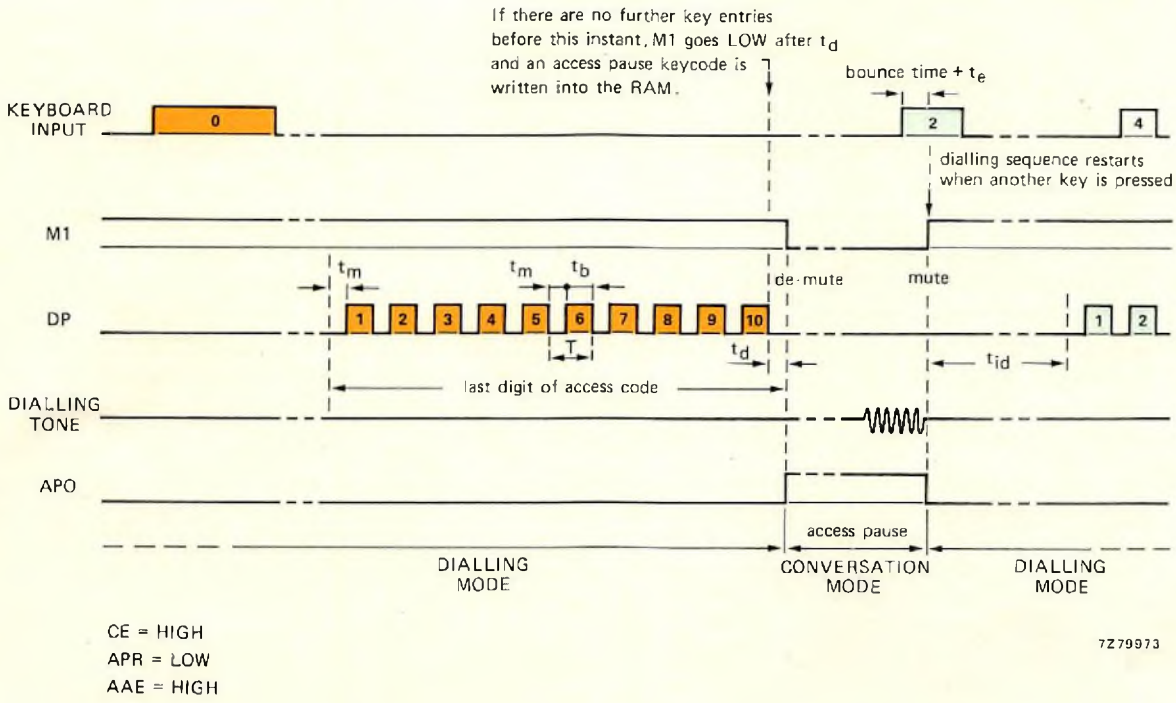


Fig.6 Dialling sequence showing how, in the MH323, an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed

Automatic regeneration of access pauses inserted by delayed key entry

In the MH323, M1 goes LOW and the circuit assumes the conversation mode in the same manner as that just described when all the entered digits have been pulsed out (Fig.6). However, if the Access Pause Reset (APR) input is set LOW, and the Automatic Access pause Enable (AAE) input is set HIGH, an access pause code will be automatically written into the RAM when M1 goes LOW. The circuit then remains in the conversation mode until the next keyboard entry restarts the dialling sequence. During redialling, if the Access Pause Output (APO) is connected to the HOLD input, the access pause will be regenerated as a fixed duration period (t_{ap} = 32 or 64 dialling pulse periods depending on the state of Access Pause Delay input APD). If necessary, this period can be prematurely terminated, when the access tone is heard, by pressing the redial (#) pushbutton again (Fig.7a). At the end of the access pause M1 will go HIGH again so that the circuit assumes the dialling mode and the re-dialling sequence continues, starting with an inter-digit pause. Up to two access pauses can be entered into the RAM in this manner.

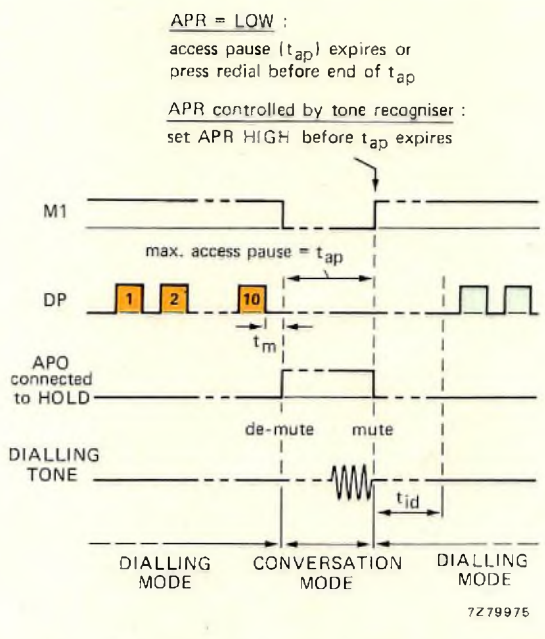


Fig.7(a) Three methods of prematurely terminating an access pause during a redialling sequence.

Automatic regeneration of access pauses inserted with access pause (*) pushbutton

In some cases, it may be undesirable for delay between keyboard entries to automatically cause an access pause code to be written into the RAM. This can be avoided in the MH323 if the APR and AAE inputs are both held LOW. In this case, when the subscriber has entered the trunk exchange code and is awaiting the access tone, an access pause code will not be written into the RAM unless the access pause (#) pushbutton is pressed. As before, the access pause will only be regenerated during redialling if the APO output is connected to the HOLD input. The number of access pauses that can be inserted in this manner is only limited by the capacity of the RAM (digits + access pauses $\leqslant 23$).

Automatic early termination of access pause with tone recogniser

Figure 7(b) shows a circuit for automatically terminating an access pause with a tone recogniser. In this circuit, as soon as an access pause code is read from the RAM during redialling, APO goes HIGH and simultaneously activates the HOLD input of the MH323 and enables the tone recogniser. When the access tone is received, the tone recogniser sets APR HIGH for at least 10 μs, thereby terminating the access pause so that the redialling sequence can continue.

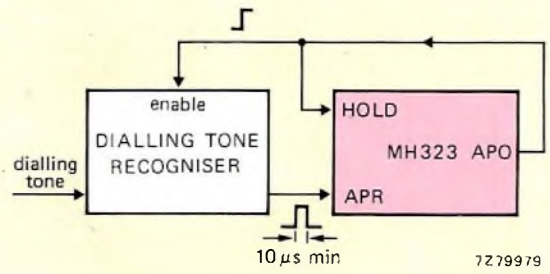


Fig.7(b) Circuit for automatic termination of an access pause during redialling by using a tone recogniser to set APR to HIGH for more than 10 μs

Shortening or lengthening an access pause with a tone recogniser

Figure 7(c) shows a circuit for automatically shortening or lengthening an access pause under the control of a tone recogniser. In this circuit, as soon as an access pause code is read from the RAM during redialling, APO goes HIGH and sets the output from the tone recogniser to HIGH. This HIGH level activates the HOLD input of the MH323, thereby setting the circuit to the conversation mode. If the access tone is received within the access pause period t_{ap}, it resets the tone recogniser which then sets HOLD to LOW and the redialling sequence continues. If the access tone is not received within the access pause period, APO goes LOW but this has no effect because the tone recogniser maintains the HOLD input of the MH323 HIGH until the access tone is received.

INTERFACING THE MH323 WITH A STANDARD PUSHBUTTON TELEPHONE

As previously explained, the MH320 and MH323 allow pushbutton telephones to be used in conjunction with exchanges which are not yet equipped with two-tone dialling decoders. They will therefore be used in the following two ways:

– In conventional telephone-sets as a replacement for the electro-mechanical rotary dial.

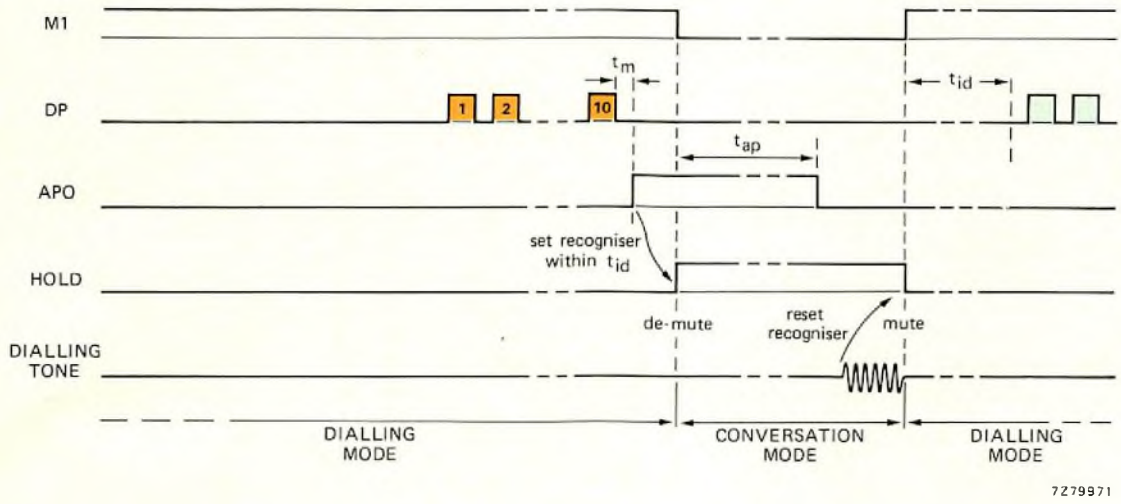
– In all-electronic telephone-sets specifically designed for use in conjunction with exchanges not yet equipped with two-tone dialling decoders.

Since it is envisaged that the majority of the integrated circuits will be used for the first application, the interface circuit for an all-electronic telephone will not be further discussed in this article.

Interface circuit design criteria

1. Since the dialling system will most often be used with conventional telephone circuits, the installation of the dialling circuit will be simplified if the interface circuit connects directly to the three terminals normally used for the rotary dial (terminals C, D and E in Fig.8(a)).

2. Since the integrated circuit must receive a supply voltage of the correct polarity, a rectifier diode bridge must be connected between the dialling circuit and the telephone lines as a guard against telephone line connection reversal.



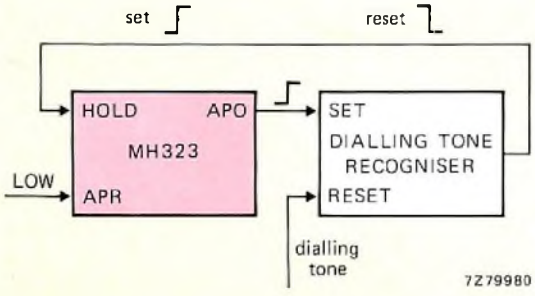


Fig.7(c) Prolonging an access pause during redialling until the dialling tone is recognised

3. If the muting contacts of the rotary dial were to be replaced with an electronic circuit, the muting circuit, and therefore the telephone circuit, would also have to be supplied via the polarity guard diode bridge. In this case, point 1 could not be achieved. The interface circuit must therefore incorporate an electro-mechanical muting relay. Since such a relay requires more operating current than the minimum available from the telephone lines ($\approx$15 mA), it must be a polarised type with two stable positions. It can then be energised from a charged capacitor via a two-pole changeover transistor switch controlled by outputs M1 and $\overline{M1}$ from the integrated circuit.

4. If the automatic redialling facility is not required, the circuit of Fig.8(b) should be used. In this arrangement, either the telephone circuit or the dialling circuit is connected *directly* to the telephone lines dependent on whether the muting relay is in the 'conversation' or 'dialling' position.

5. If the automatic redialling facility is required, the supply to the integrated circuit must be maintained when the handset is replaced on the cradle. This can be achieved as follows:

   a. By bypassing the cradle contacts with a resistor so that the required current ($\approx 1\,\mu$A) can be derived from the telephone lines.

   b. By using a rechargeable battery.

   c. By using the charge held by an electrolytic capacitor (limited redialling memory retention time).

If option (a) were used, condition 1 could not be satisfied. Option (b) is rejected by most Post Office authorities on the grounds of cost and diminished reliability. In most cases, a charged capacitor will therefore be used to provide the back-up supply for the RAM when using the automatic redialling facility.

6. If the automatic redialling facility is required, the circuit of Fig.8(b) would limit the available redialling time because the line current is not available for charging the back-up supply capacitor until the common contact of the keyboard is closed. For this reason, the circuit of Fig.8(c) is more suitable. In Fig.8(c), the value of the back-up supply capacitor can be increased because the line current becomes available as soon as the handset is lifted from the cradle. However, in this circuit, the impedance of the dialling circuit (typically 11 Ω in series with 68 μF) remains connected in series with the telephone circuit in the conversation mode of operation.

7. Protection against lightning-induced surges of up to 2 kV on the telephone lines can be provided by connecting a Voltage-Dependent Resistor (VDR) across the input to the bridge rectifier.

8. The line switching transistor may have to be protected against excessive collector current and power dissipation caused by residual lightning-induced surges after the action of the VDR (250 V to 300 V).

9. The integrated circuit must be protected against line voltages exceeding the maximum V_{DD} specified for the circuit.

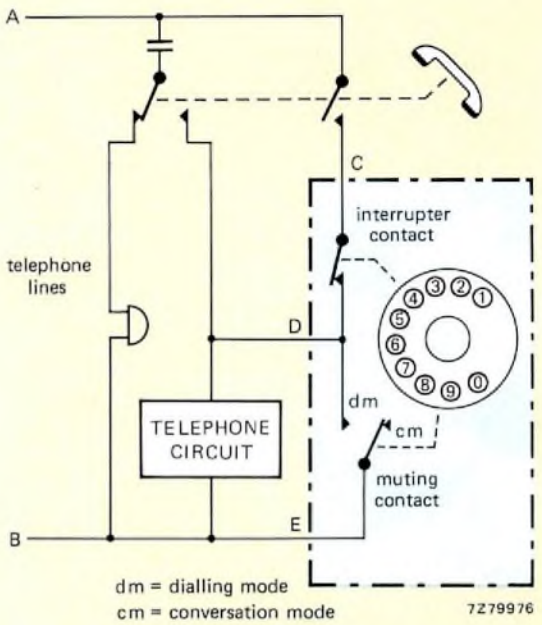


Fig.8(a) A conventional telephone with rotary electromechanical dial

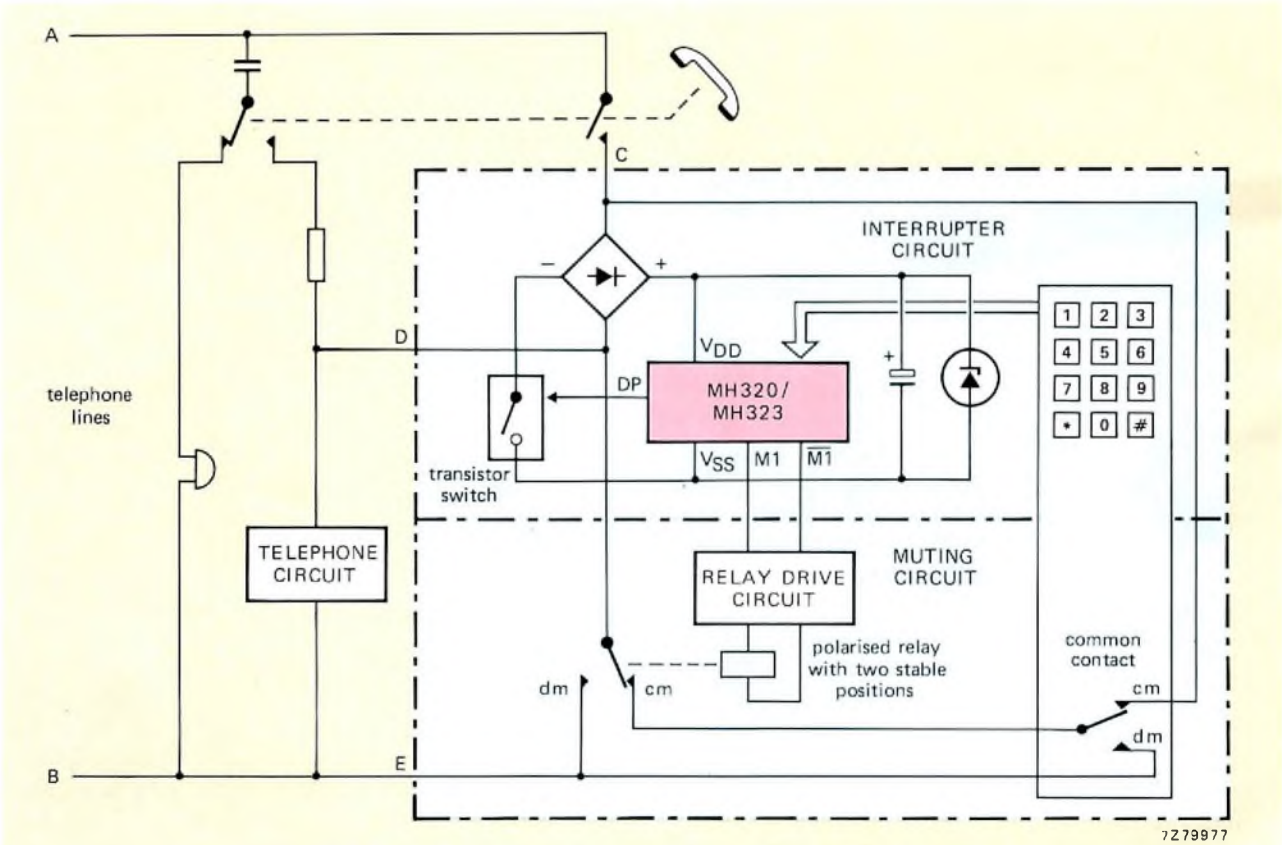


Fig.8(b) The most suitable interface circuit if the redialling facility is not required

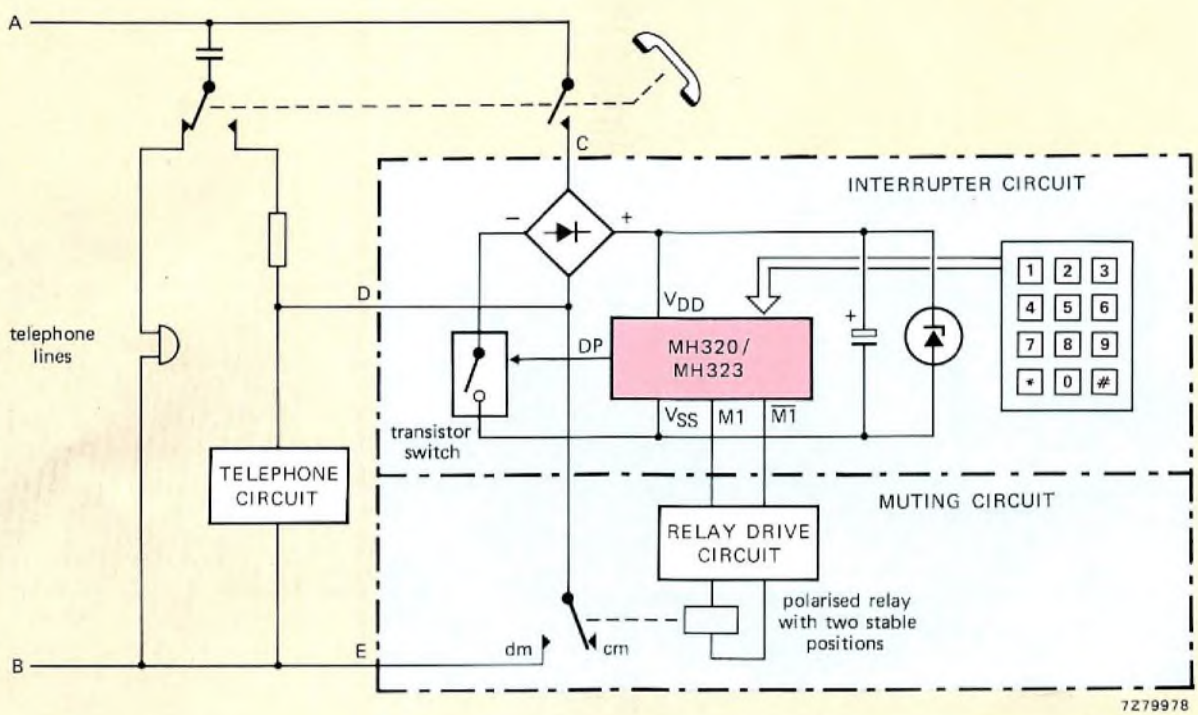


Fig.8(c) The most suitable interface circuit if the redialling facility is required

Examples of interface circuits

The circuit diagram of a telephone-set without an automatic redialling facility is given in Fig.9. The circuit diagram of a telephone-set with an automatic redialling facility and an automatic access pause system is given in Fig.10. Both of these circuits satisfy all of the design criteria.

The circuits of Fig.9 and Fig.10, and the circuit of an all-electronic telephone-set for interrupted current-loop dialling, will be described in a series of Technical Notes.

Brief specification for the circuit of Figure 9

All of the following figures are typical values. The circuit withstands 2 kV pulses generated by the circuit published in West German specification FTZ 10/700.

DP	TR_1	I_{line}	V_{in}
LOW	ON	15 mA	4 V
LOW	ON	75 mA	5.6 V
HIGH	OFF	50 μA	$V_{exchange}$ (48 V)
HIGH	OFF	175 μA	90 V

Brief specification for the circuit of Figure 10

All of the following figures are typical values. The circuit withstands 2 kV pulses generated by the circuit published in West German specification FTZ 10/700. Using a 1000 μF electrolytic capacitor for the back-up supply results in a start-up time of 70 ms after lifting the handset, and a redialling memory retention time of sixteen minutes. The impedance in series with the telephone circuit during the conversation mode of operation is 11 Ω in series with 68 μF.

DP	TR_1	I_{line}	V_{in}
LOW	ON	15 mA	4.6 V
LOW	ON	75 mA	6 V
HIGH	OFF	50 μA	$V_{exchange}$ (48 V)
HIGH	OFF	175 μA	90 V

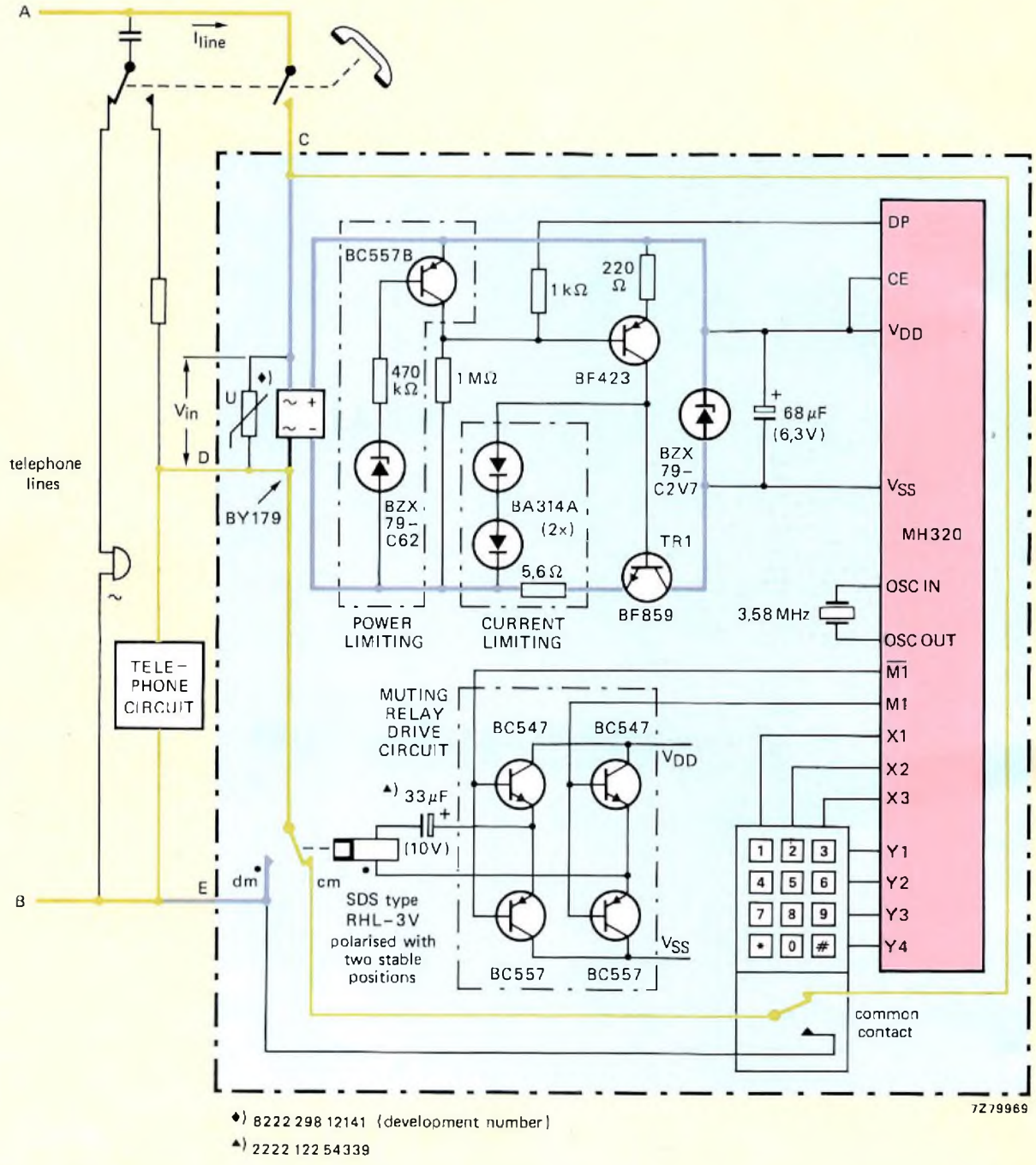


Fig.9 Circuit of a telephone-set without an automatic redialling facility

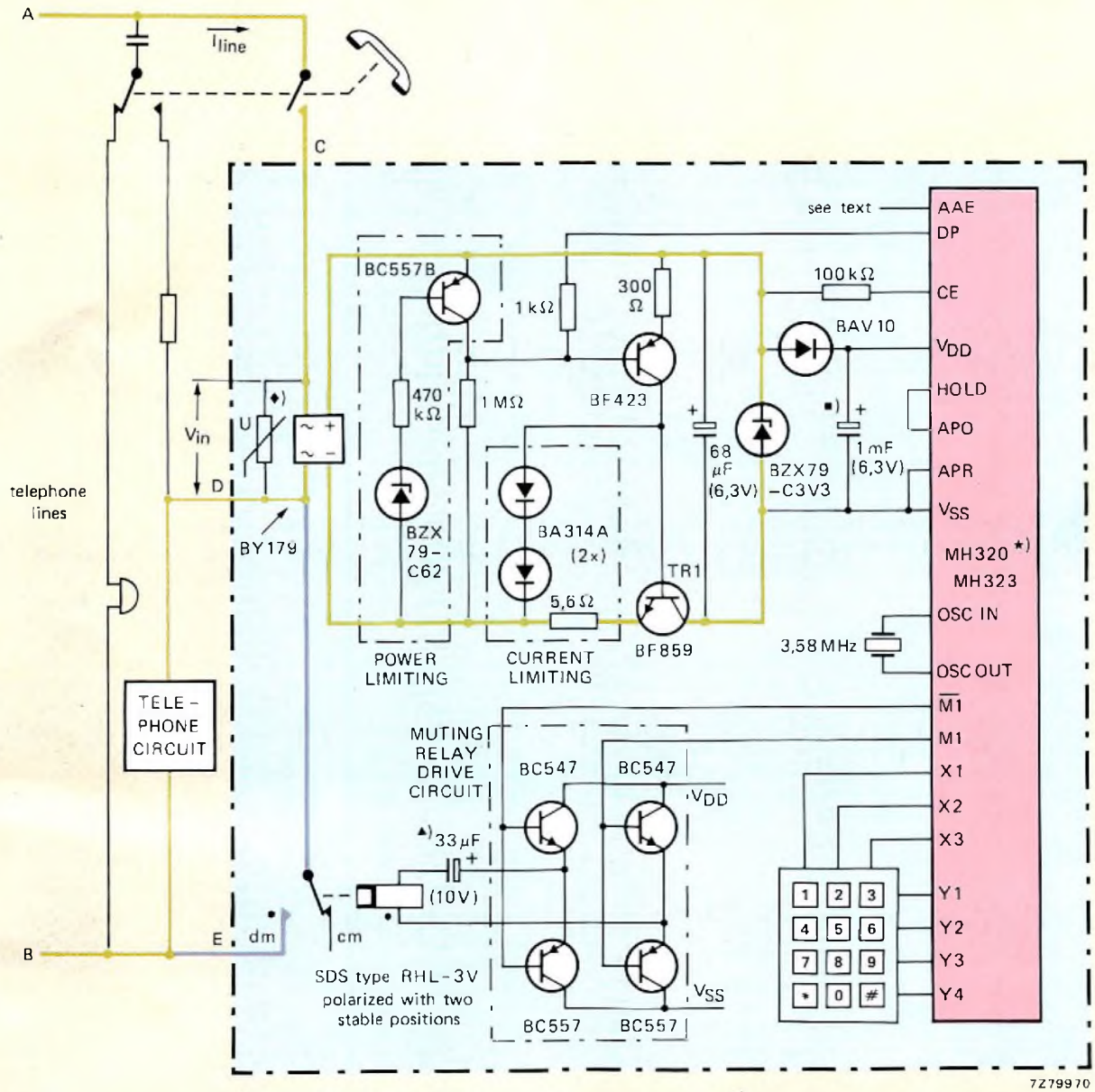


Fig.10 Circuit of a telephone-set with an automatic redialling facility. If the MH323 is used for this circuit, the automatic access pause system is also available

Abstracts

Inverter circuit for PWM motor speed control system

This article describes an inverter circuit which has been developed specifically for use in Pulse-Width Modulation (PWM) three-phase motor speed control systems. The advantages of the circuit over previous designs are considered and the design method is described in detail. As an example, the design of an inverter suitable for driving a 380 V/3 kW motor is given. The article is the second in a series describing our PWM speed control system.

Mains pollution caused by domestic appliances

Part 3 – Voltage fluctuation and flicker

Perceptible changes in electric light intensity are known as flicker. These changes, which can produce visual irritation, are caused by voltage fluctuation of the mains due to load switching. This article discusses flicker from an annoyance and from an electrical point of view, having particular regard for the recommendations of CENELEC and the work of the IEC. The ways in which flicker can be calculated and measured are described, and some advice is given on how to reduce the effects of flicker by suitable choice of switching frequency and equipment design.

Electret microphone for telephony

Increasing maintenance costs together with recent advances in microphone technology have led to a strong demand for the replacement of the telephone carbon microphone. This article describes an electret microphone which is particularly suited as a replacement for the carbon transmitter. The construction of the electret capsule is described in detail, and the long-term stability characteristics of charged polymer films are discussed. The desirable operating characteristics of a telephone microphone are considered, and the article concludes by describing a discrete amplifier for use with the electret capsule.

Digital control of radio and audio equipment

Part 7 – RTS tuning controls and the microcomputer

This article explains how the Radio Tuning System (RTS) described in earlier articles is microcomputer controlled. The described system is based on an 8048 microcomputer with software mainly intended for evaluation and demonstration of the RTS. A brief description of the main loop of the microcomputer program is given, and a step-by-step explanation of how a preset programme is recalled is included. The article concludes with a complete circuit diagram and a description of the power down protection.

Interrupted-current-loop dialling circuits for pushbutton telephones

Since the introduction of two-tone dialling systems in some modern telephone exchanges, many subscribers have a preference for pushbutton telephones. The integrated circuits MH320 and MH323 allow pushbutton telephones to be used with exchanges not yet equipped with two-tone dialling decoders. The article fully describes the dialling system and gives two typical application circuits which can be connected to the telephone terminals normally used by a rotary dial.

Inverterschaltung zum Betrieb eines Motors mit Drehzahlregelung durch Pulsbreiten-Modulation

Dieser Artikel beschreibt eine Inverterschaltung, die speziell für den Betrieb eines Dreiphasen-Motors entwickelt wurde, dessen Drehzahlregelung durch Pulsbreiten-Modulation erfolgt. Der Entwurf dieser Schaltung wird ausführlich behandelt und der Vorteil dieser Schaltung gegenüber vorangegangenen Entwürfen herausgestellt. Als praktisches Beispiel folgt der Entwurf eines Inverters, der für den Betrieb eines 380 V/3 kW-Motors ausgelegt ist. Es ist dieses der zweite Artikel einer Serie, welche unser System der Drehzahlregelung mittels Pulsbreiten-Steuerung behandelt.

Das Entstehen von Netzstörungen durch Haushaltsgeräte

Teil 3 – Spannungsschwankungen und Flackererscheinungen

Wahrnehmbare, als 'Flackern' bezeichnete Änderungen der Beleuchtungsstärke können zu einer Gereiztheit führen. Sie werden durch Netzspannungsschwankungen ausgelöst, die ihre Ursache im Schalten von Lasten haben. Dieser Artikel behandelt das Flackern sowohl in Hinblick auf die verursachte Belästigung als auch in elektrischer Hinsicht unter besonderer Berücksichtigung der CENELEC- und IEC-Empfehlungen. Es wird beschrieben, wie das Flackern gemessen und berechnet werden kann. Ausserdem werden Ratschläge gegeben, wie sich die Auswirkungen des Flackern durch die Schaltfrequenz und den Geräteentwurf verringern lassen.

Ein Elektret-Mikrofon für das Fernsprechwesen

Zunehmende Wartungskosten führten in Verbindung mit jüngsten Fortschritten in der Mikrofontechnik zu einem starken Interesse, das Telefon-Kohlemikrofon zu ersetzen. Dieser Beitrag beschreibt ein Elektret-Mikrofon, das sich insbesondere als Ersatz für den Kohlemikrofon-Sender eignet. Der Aufbau der Elektret-Kapsel wird im Detail beschrieben, und die Eigenschaften geladener Polymer-Filme im Hinblick auf die Langzeitstabilität werden diskutiert. Die für ein im Telefon eingesetztes Mikrofon erwünschten Betriebseigenschaften werden betrachtet. Der Beitrag schliesst mit der Beschreibung eines diskret aufgebauten Verstärkers, an dem die Elektret-Kapsel betrieben werden kann, ab.

Digitale Steuerung von Rundfunk- und NF-Geräten

Teil 7 – RTS-Abstimmsteuerung und der Mikrocomputer

Der vorliegende Beitrag erklärt, wie das in früheren Artikeln beschriebene RTS-System mikrocomputergesteuert wird. Das beschriebene System basiert auf einem Mikrocomputer 8048, dessen Software hauptsächlich auf die Demonstrierung von Funktionstüchtigkeit und Eigenschaften der RTS-Systems zugeschnitten ist. Der generelle Ablauf des Mikrocomputerprogramms wird kurz beschrieben, wobei eine Schritt-für-Schritt-Erklärung für die Vorgänge beim Abruf einer gespeicherten Station eingeschlossen ist. Der Artikel schliesst mit einer Gesamtschaltung der Mikrocomputer-Peripherie und einer Beschreibung der Netzspannungsüberwachung ab.

Wählerschaltungen mit Stromunterbrechungsschleife für Tastentelefone

Set Einführung von Zweiton-Wählersystemen in modernen Fernsprechvermittlungen bevorzugen viele Teilnehmer Tasten-Telefonapparate. Mit Hilfe der integrierten Schaltungen MH320 und MH323 ist es möglich, Tasten-Telefonapparate zu verwenden, auch wenn die Vermittlung noch nicht mit Zweiton-Wähler-Decodern ausgestattet ist. Der Artikel behandelt ausführlich das Wählersystem und zwei typische Anwendungsschaltungen, die an die Anschlussklemmen für eine normale Wählerscheibe angeschlossen werden können.

Circuit onduleur pour un système de régulation de vitesse de moteur à modulation par impulsions de largeur variable

Cet article décrit un circuit onduleur spécifiquement étudié en vue de l'emploi dans des systèmes de régulation de vitesse de moteurs triphasés à modulation par impulsions de largeur variable. Les avantages de ce circuit par rapport aux réalisations précédentes sont considérés et la méthode de conception est décrite en détail. La conception d'un onduleur convenant pour la commande d'un moteur de 380 V/4 kW est donnée à titre d'exemple. Cet article est le second d'une série consacrée à la description de notre système de régulation de vitesse à modulation par impulsions de durée variable.

Un circuito inversor para un sistema de control de velocidad de motores por modulación de anchura de impulsos

Este artículo describe un circuito inversor que ha sido específicamente diseñado para utilizarlo en sistemas de control de velocidad de motores trifásicos por modulación de anchura de impulsos. Se examinan las ventajas del circuito sobre los diseños anteriores y se describe con detalle el método de diseño. Como ejemplo se da el diseño de un inversor adecuado para excitar un motor de 4 kW, 380 V. Este artículo es el segundo de una serie que describe nuestro sistema de control de velocidad por modulacion de anchura de impulsos.

Pollution du secteur par les appareils domestiques

3ème partie – Fluctuations de tension et papillotement

On donne le nom de papillotement aux variations perceptibles de l'intensité de l'éclairage électrique. Ces variations, qui sont susceptibles d'être gênantes, sont causées par des fluctuations de la tension secteur résultant d'opérations de commutation en charge. L'article traite du papillotement au point de vue de la gêne et au point de vue électrique, eu égard en particulier aux recommandations du CENELEC et aux travaux de la CEI. Les méthodes de calcul et de mesure du papillotement sont décrites et des conseils sont donnés sur la manière de réduire les effets par un choix judicieux de la fréquence de commutation et de la conception du matériel.

Contaminación de red causada por aplicaciones domésticas

Parte 3 – Parpadeo y fluctuación de tensión

Los cambios perceptibles en la intensidad de la luz eléctrica son conocidos como parpadeo. Estos cambios, que pueden producir fuertes irritaciones, son causados por la fluctuacion de la tension de red debida a conmutaciones de la carga. Este artículo estudia el parpadeo desde un punto de vista eléctrico y de la molestia que ocasiona, prestando particular atención a las recomendaciones de CENELEC y al trabajo de la IEC. Se describen los caminos a seguir para el cálculo y medición del parpadeo, y se dan algunos consejos sobre la forma de reducir los effectos de parpadeo mediante la elección adecua da de la frecuencia de conmutación y un diseño cuidadoso del equipo.

Microphone téléphonique à électret

L'accroissement des coûts d'entretien, associé aux progrès récents de la technologie des microphones, s'est traduit par une forte demande de remplacement du microphone téléphonique à charbon. Le présent article décrit un microphone à électret particulièrement approprié à cette fin. La construction de la pastille à électret est décrite en détail et les caractéristiques de stabilité à long terme des films de polymère chargés sont analysées. Les caractéristiques fonctionnelles souhaitables d'un microphone téléphonique sont considérées et l'article se conclut par la description d'un amplificateur discret destiné à être employé avec la pastille à électret.

Un microfono electret para telefonía

El aumento de los costos de mantenimiento junto con los recientes avances en la tecnología de micrófonos, han conducido a un fuerte deseo de sustituir el micrófono de carbón del telefono. Este artículo describe un micrófono electret que es particularmente adecuado para sustituir al transmisor de carbón. Se describe con detalle la construcción de la cápsula electret y se estudian las características de estabilidad del dieléctrico polarizado. Se consideran las características deseables de funcionamiento de un micrófono telefónico, y el artículo concluye describiendo un amplificador discreto para ser utilizado con la cápsula electret.

Commande digitale d'équipment radio et audio

7ème partie – les commandes d'accord RTS et le micro-ordinateur

Cet article explique comment le système RTS d'accord sur émetteur de radio déjà décrit dans des numéros précédents est piloté par micro-ordinateur. Le système décrit est basé sur un microordinateur 8048 dont le logiciel est principalement destiné à l'évaluation et la démonstration du système RTS. Une brève description de la boucle principale du programme du micro-ordinateur est donnée, ainsi que la manière dont un programme préétabli est rappelé. L'article se termine par le schéma complet d'un circuit et une description de la protection contre les pannes d'alimentation.

Control digital de equipos de radio y audio

Parte 7 – Controles de sintonia RTS y el microordenador

Este artículo explica la forma de controlar por microordenador el sistema de sintonía de radio (RTS) descrito en anteriores artículos de EC y A. El sistema descrito está basado en un microordenador 8048 con software realizado particularmente para, la evaluación y demostración del RTS. Se da una breve descripción del bucle principal programa del microordenador, y se incluye una explicación paso a paso de como se vuelve a llamar un programa preestablecido. El artículo concluye con un esquema completo del circuito y una descripción de la protección contra una bajada en la alimentación.

Circuits de sélection à boucle de courant interrompu pour postes téléphoniques à clavier

Depuis l'introduction de systèmes de sélection à deux tonalités dans certains centraux téléphoniques modernes, de nombreux abonnés manifestent une préférence pour les postes à clavier. Les circuits intégrés MH320 et MH323 permettent d'employer ces derniers conjointement avec des centraux non encore équipés de décodeurs de sélection à deux tonalités. L'article contient une description complète du système de sélection et de deux circuits d'application types, qui peuvent être connectés à des terminaux téléphoniques normalement associés à un cadran rotatif.

Circuitos de llamada de lazo de corriente interrumpida para teléfonos de teclado

Desde la introducción de sistemas de llamada telefónica de dos tonos en algunas de las centrales telefónicas modernas, muchos abonados prefieren teléfonos de teclado. Los circuitos integrados MH320 y MH323 permiten utilizar teléfonos de teclado con centrales no equipadas todavía con decodificadores de llamada de dos tonos. El artículo describe totalmente el sistema de llamada y da dos circuitos típicos de aplicación que pueden ser conectados a los terminales del teléfono de disco normalmente utilizado.

Authors

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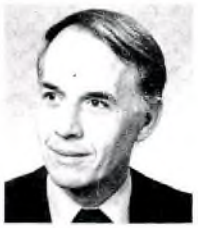

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ERRATA

Volume 2, No. 1, November 1979, *Segment field magnets for large electric motors.*

page 60 — The graph published for FXD380 is incorrect; the correct graph is printed below.

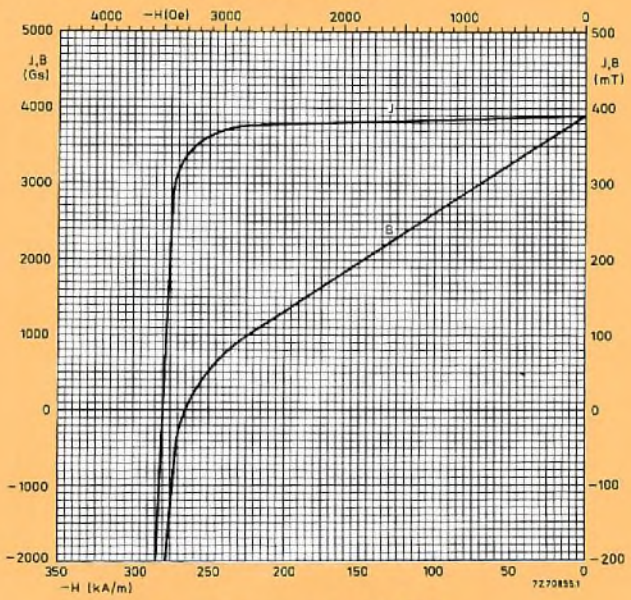

Fig.1(c) B-H and J-H curves for FXD380

Volume 2, No. 2, February 1980, *Introduction to PWM speed control system for 3-phase AC motors.*

page 72, Table 1 — Footnote should read 'd.c. supply voltage source' (not 'a.c. supply voltage source').

page 74, Fig.14 — Choke should be labelled 'L_2'.

page 74, right-hand column — First equation should read:
$I_{cp} = V_{Cb} \sqrt{(C_1/L_2)}$.

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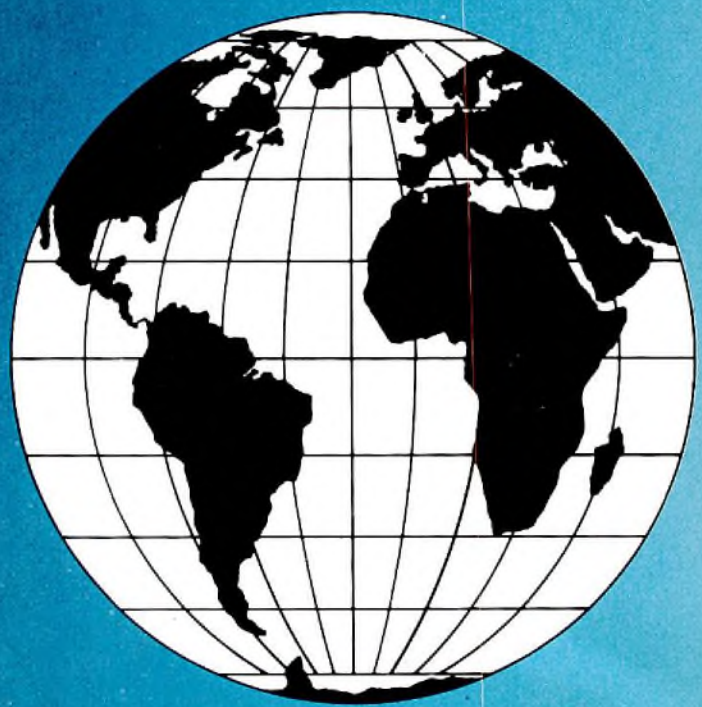

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