GTE LENKURT

DEMODULATOR

SEPTEMBER 1974

PCM OVER MICROWAVE PART I

The traditional approach to transmission of digital information has been with cable as the transmission medium, but the increased demand for digital microwave systems has led to a number of developments in the transmission of PCM over microwave radio.

The transmission of PCM (pulse code modulation) over microwave radio is particularly desirable when the geography of an area or some other obstacle impedes or prevents the accomplishment of cable plant. For example, PCM over microwave radio may be useful in situations where a body of water must be crossed to complete the communication path, where it is necessary to extend low-capacity trunks in rural areas, and where there is a requirement for temporary low-capacity trunks for special service or telephone restoration.

Recent developments at GTE Lenkurt have led to the introduction of equipment capable of multiplexing two T1-type PCM signals (each comprised of 24 PCM voice channels), and coding and shaping these in such a way that transmission over any frequency-modulated microwave radio is technically feasible. This type of equipment is thus capable of transmitting 48 PCM channels over one radio. By employing cross-polarized operation, which uses two radios on the same radio frequency (one radio using a vertically-polarized antenna system, the other a horizontally-polarized), this same equipment has the capability of utilizing the radio spectrum to transmit 96 PCM voice channels per radio channel.

An example of a hypothetical PCM-over-microwave system is shown in the simplified block diagram in Figure 1. The major components of the system are the digital multiplexer, the microwave radio baseband equipment, and the microwave radio transceiver. The input to the system is provided by two 24-channel D1, D2, or D3-type PCM terminals operating over a T1 line, or by any other type of equipment capable of producing a 1.544 Mb/s bipolar bit stream. The combination of any two 1.544 Mb/s channel banks can be used to meet subscriber, exchange, toll connecting, and intertoll applications, as well as low- or high-speed data transmission.

The Digital Multiplexer

The digital multiplexer combines two 1.544 Mb/s digital inputs into a 3.156 Mb/s signal, which is then converted to "modified duobinary" format for application to the radio baseband assembly. The modified duobinary output signal from the multiplexer is applied to the radio baseband equipment, where it is combined with voice-frequency order wire and alarm and continuity pilot signals. The composite signal is then level-coordinated and fed to the FM transmitter. The process is reversed in the receive portion of the system. Figure 2 shows the digital multiplexer in block diagram form. Low speed input and output signals to the multiplexer are designated DS1, which means "digital signal at the first level," and refers to the 1.544 Mb/s bipolar line signal from T1-type equipment such as channel banks, data terminals, and repeatered lines.

The transmit portion of the multiplexer synchronizes and interleaves the two asynchronous, bipolar input signals into a single bit stream, which is then scrambled, encoded, and converted to a modified duobinary waveform for application to the baseband equipment.

The receive portion of the multiplexer accepts a signal from the radio baseband assembly. It filters the received signal, blocks the radio pilot frequency, and decodes and descrambles the signal. The signal is then demultiplexed and desynchronized into two separate 1.544 Mb/s streams. Two new bit streams are then produced that are identical to those applied at the transmit end.

Synchronization

The bit rate of the asynchronous T1 lines coming into the multiplexer is a nominal 1.544 Mb/s; that is, each T1 line may have a bit rate that is sometimes higher, and sometimes lower, than the desired 1.544 Mb/s. This results in a continual shift in phase between the two T1 lines, which prevents the direct interleaving of bit streams into a single bit stream at twice the frequency. In addition, instantaneous frequency changes (timing jitter) that may occur in an individual T1 bit stream also prevent synchronization of the two T1 bit streams. To handle both of these problems, an eight-cell elastic store is included in the synchronizer portion of the "syndes" (synchronizer-desynchronizer) unit (see Figure 3). Each syndes extracts a clock (timing pulses) from the incoming data, and slices the data to convert it from a bipolar format to unipolar format (ones and zeros).

In the synchronizing process, after the DS1 streams have been converted to unipolar format, dummy or "stuffed" pulses are inserted, where needed, into each incoming T1 pulse stream, thus bringing the bit rate of each up to some common value before multiplexing. Each T1 pulse stream is written into the elastic store by means of the write clock derived from the incoming T1 pulse stream. Taking a simplified example, if the DS1 data coming into the synchronizer is at 1.544 Mb/s, the clock or timing pulses that are extracted from the data will be at 1.544 MHz. A synchronous T1 pulse stream is read out of the elastic store by means of a local 1.5458-MHz clock that is common to both synchronizers. The common clock rate of 1.548 MHz is a critical frequency, since too high a frequency would cause bits to be read before they actually appeared, and too low a frequency would result in an occasional loss of a bit. Since data must be written into the elastic store before it can be read, the read clock must operate at a faster rate than the write clock (1.544 MHz).

The read clock cannot be allowed to overtake the write clock to the extent that it attempts to read a bit that isn't yet present in the store. (This event is called "spilling" the elastic store.) To prevent this occurrence, the phase comparator (which compares the phase of the write clock with that of the read clock), through associated control circuitry, slows up the read clock by inhibiting readout for one time slot, and stuffs a dummy pulse into the synchronous pulse stream. This maintains the proper output bit rate and allows the write clock to again precede the read clock, thus keeping the elastic store at least partially full. Any bits inserted by stuffing are removed during the demultiplexing operation.

The Transmit Common Unit

The transmit common unit provides pulse stuffing for both syndes. Each stuffed bit is identified by a complex framing scheme which allows recogni-

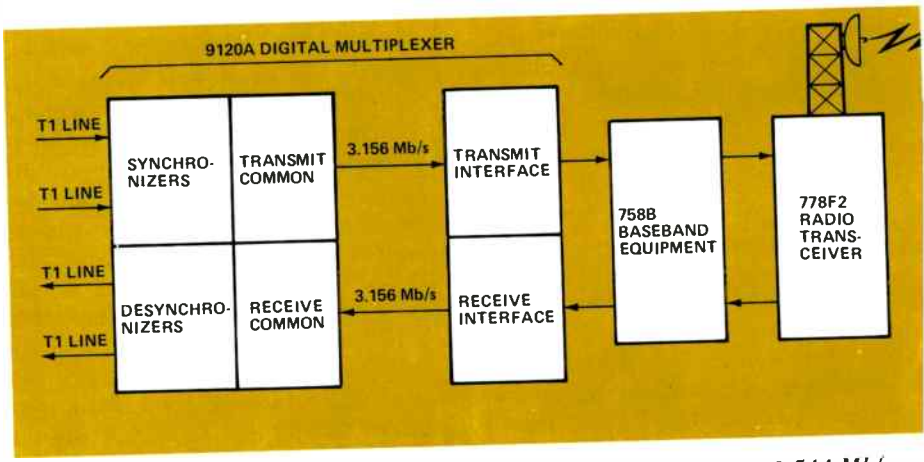


Figure 1. Block diagram of a PCM-over-microwave system with two 1.544-Mb/s inputs.

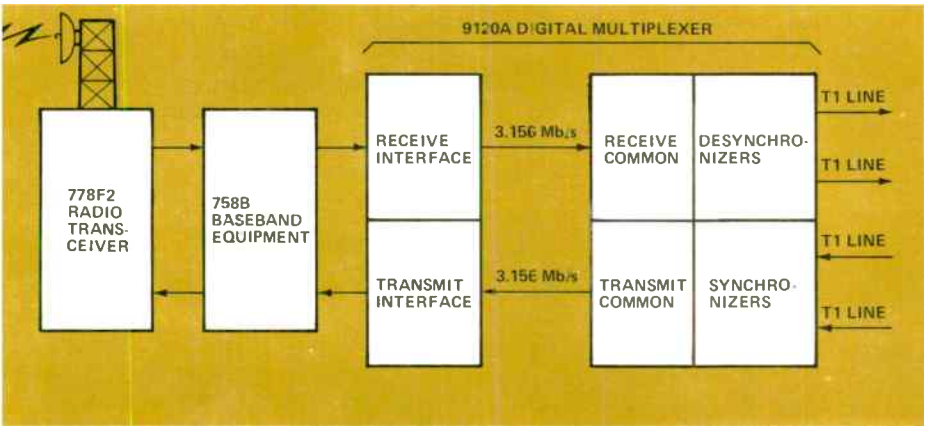
tion of the stuffed bits at the receive end so that they may be eliminated from the bit stream. The transmit common unit provides control bits (including framing bits) as well as stuffing bits. The framing bits, which are added to the data stream at precise intervals, are actually a form of bookkeeping: they keep track of which bits belong to T1 line A, and which to T1 line B.

The output from the syndes is two bit streams of ones and zeros at the same clock rate (1.5458 MHz). The transmit common unit interleaves the two bit streams, adds control bits, and clocks out a bit stream of 3.156 Mb/s; this is slightly more than twice the bit stream frequency (1.544 Mb/s) due to the addition of control bits and stuffed bits.

Demultiplexing

The receive common unit performs the opposite functions of the transmit common unit. The 3.156-Mb/s signal enters the receive common unit, where the framing bits are removed and monitored. The overall condition of the transmission medium may be determined by monitoring the framing bits. The information bits constitute totally random data, but the insertion of framing bits guarantees a point of reference at a specific location. If the framing bits are repeatedly not in the prescribed location, synchronization is momentarily lost, and the multiplexer initiates a resynchronizing process.

The receive common unit monitors the incoming 3.156-Mb/s signal, examining incoming control bits for a predetermined pattern. The receive common circuitry removes the stuffing and control bits, then splits the remaining bit stream into two 1.544-Mb/s streams. Each bit stream is then applied to the desynchronizer portion of the appropriate syndes (see Figure 3), where it is retimed with a phase-locked loop through another 8-cell elastic store to eliminate the gaps caused by the bits removed at the receive end. At this point the bit streams are again asynchronous, and the original data at the input of the multiplexer is reproduced at the output of the demultiplexer.



To review, two asynchronous (different frequency) bit streams have been interleaved into a single bit stream at slightly more than twice the nominal bit rate of 1.544 Mb/s. Pulse-stuffing synchronization is used to bring the bit rate up to 3.156 Mb/s for output to the transmit interface unit. At the far end, just the opposite process takes place to reproduce the data.

Transmit Interface Unit

The transmit interface unit converts the binary (ones and zeros) 3.156-Mb/s signal to one suitable for application to the baseband portion of the radio. If the binary signal were to be applied directly to the radio transmitter, the resulting radio signal would occupy more than the maximum allowable bandwidth (3.156 MHz) for a 2-GHz system. One major objective for the interface unit is thus to compress the incoming data so that the radio signal will not exceed 3.156-MHz of bandwidth. Careful system design is necessary to meet this objective, since the compression of data to fit within the required bandwidth must be accomplished without an objectionable increase in error rate during deep

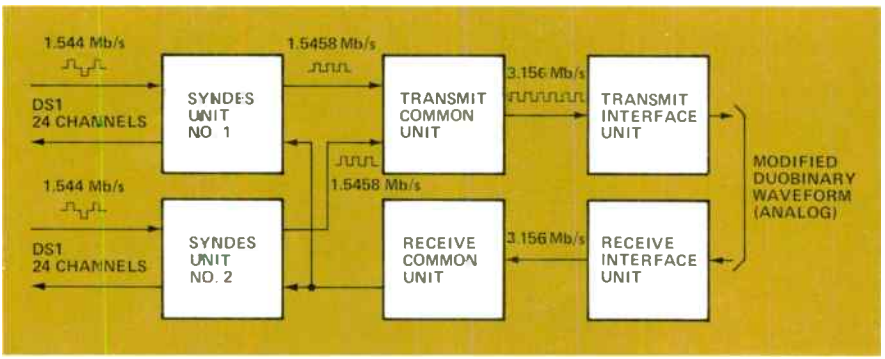


Figure 2. The digital multiplexer processes two DS1 inputs for application to microwave baseband equipment.

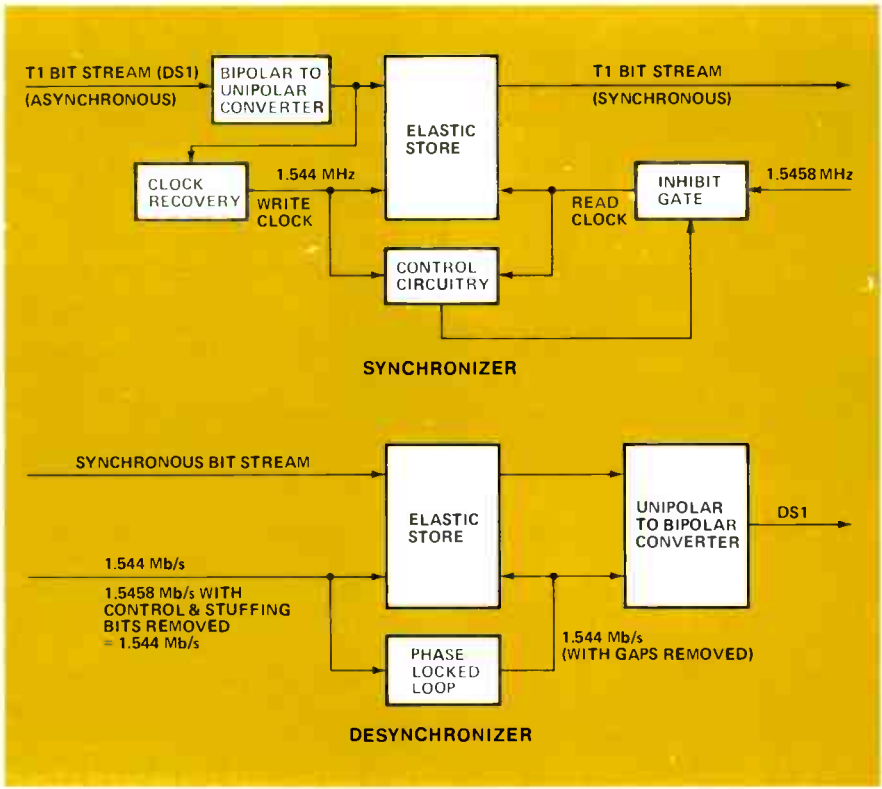


Figure 3. Synchronization and desynchronization take place in the syndes portion of the digital multiplexer.

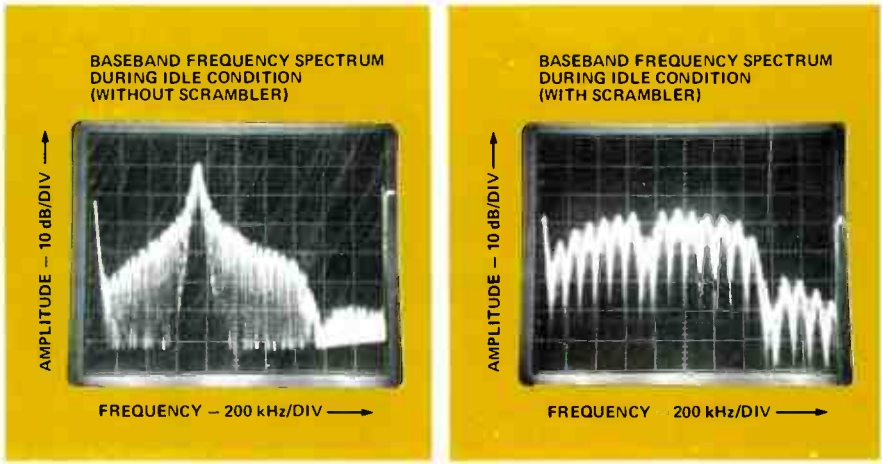


Figure 4. Scrambling is necessary during idle conditions to prevent the occurrence of power concentration at discrete frequencies.

atmospheric fades. The transmit interface unit also removes dc and low-frequency components so that an order-wire signal can be transmitted with the main body of data.

Scrambling

The sequence of events which takes place in the transmit interface unit after the two incoming DS1 signals are converted into a single 3.156 Mb/s stream is scrambling, conversion to modified duobinary encoding waveform, and filtering. There are two inputs to the transmit interface: a clock from the transmit common unit at 3.156 MHz, and data from the transmit common unit at 3.156 Mb/s. The main reason for scrambling the binary signal is to eliminate discrete frequency components during idle conditions. An idle condition may exist, for example, during the very early hours of the morning when perhaps all 48 channels are not in use, except for the transmission of framing bits. During this idle period, repetitive frequency patterns constituting a heavy concentration of system power at particular frequencies are likely to occur: such power concentrations can cause interference in other radio channels in the vicinity. Scrambling eliminates this condition by creating a continuum of power over all the channels in the system during idle conditions. The even distribution of available power over the entire allocated frequency spectrum reduces interference to nearby radio channels. Figure 4 shows a comparison of idle-condition output spectrums with and without a scrambler in the system. The scrambling process consists of combining the data entering the transmit interface unit with a pseudo-random bit sequence generated by a conventional feedback shift register.

An important consideration in the design of an overall transmission is the inclusion of a voice-frequency order wire in the radio baseband equipment; how this is achieved, while conforming to certain bandwidth requirements, will be the starting topic of the next Demodulator.

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