VISUAL INFORMATION SYSTEMS

MODEL VTF TITLEFILE SYSTEM

INSTRUCTION MANUAL VOLUME II

MAINTENANCE INSTRUCTIONS AND
SPARE PARTS LIST

VISUAL ELECTRONICS CORPORATION

SECTION V
SERVICE AND REPAIR

GENERAL

This section contains information necessary to aid the maintenance technician in servicing and repairing the Titlefile. Included in the section are service and repair hints, detailed circuit descriptions, schematics, logic and timing diagrams, and signal listings.

SERVICE

The only periodic servicing necessary to assure efficient operation of the Titlefile is cleaning of the magnetic tape head, and tape cleaner.

> CAUTION: Under all circumstances, avoid contact with tape. Ascertain that the spring-loaded cartridge lid is closed at all times when the cartridge is not in the tape unit.

Cleaning of Tape Head

Use any commercially available aerosol magnetic tape head cleaner and a clean, soft, lint-free cloth. Gently wipe heads dry after spraying on cleaner. Wipe a second time to eliminate any residue. This procedure should be performed approximately once a week.

Cleaning of Tape Vacuum Cleaner

Using a clean, soft, lint-free cloth, moistened with tape head cleaner, gently wipe surface of tape vacuum cleaner. Wipe with dry cloth to eliminate any residue. This procedure should be performed approximately once a week.

Tape Loop Replacement

If the tape is damaged in any way, return the entire tape cartridge to Visual Electronics Corporation for tape loop replacement.

REPAIR

Repair of the Titlefile must be considered as two operations: isolation of the malfunctioning component, and part replacement.

TROUBLE ISOLATION

In order to provide a starting point for the maintenance technician, the following test procedures should be performed. When the desired result is not obtained in any test step, begin checking the circuitry associated with that function for an indication of malfunction. Table 5-1 lists the required tools and test equipment for trouble isolation. If, for any reason, the Titlefile performs as desired for all the test checks, yet still malfunctions during operation, start signal tracing at the circuit or component in which the indication of malfunction occurs. Schematic and logic diagrams are included to aid in trouble isolation.

Table 5-1.
SPECIAL TOOLS AND TEST EQUIPMENT

Name	Type
Oscilliscope	*Tektronix Model 459
Multimeter	*Simpson Model 260
Wire Wrap Unit	*Gardner-Denver
Gun	Model 14-XA2-3
Bit	Part No. 507063
Sleeve	Part No. 507100-482
Unwrapping Tool	*Gardner-Denver, Part No. 505244-481
Display Control Unit	Visual Model 990
Display Control Keyboard	Visual Model 995
Video Display Unit	*Conrac Monitor
Integrated Circuit Extractor	*Augat, Part No. 114-1

*as listed or equivalent.

Pre-Turn-On Procedure

The following checks shall be performed prior to turn-on of the Titlefile system.

1) TAPE UNIT. Check tape heads and cartridge receptor for foreign matter; clean with magnetic tape head cleaner if required.

2) CABLING. Check that all cables are properly connected and secured.

Voltage Checks

Energize the system and check the following power supply outputs, using the multimeter.

\+ 5 volts dc ± 5% at TB2-1 of Controller
\- 9 volts dc ± 5% at TB2-5 of Controller
\+ 20 volts dc ± 5% at TB3-1 of Controller
\- 20 volts dc ± 5% at TB3-2 of Controller
\+ 200 volts dc ± 5% at TB3-4 of Controller

Interface Unit

Check for proper transfer of data between the DCU and Titlfile as follows:

A) DATA OUTPUT. All data output lines are negative logic and must be 0 volts $^{+0.25\ v}_{-0\ v}$ for logic 1 and +5 volts $^{+0\ v}_{-0.25\ v}$ for logic 0. All other outputs are positive logic (+5 volts = logic 1; 0 volts = logic 0).

B) OUTPUT SIGNAL DESIGNATIONS. The following signals are given the listed signal names on the logic diagrams. To check any signal voltage, refer to the signal list for the circuit module and pin number of the signal origin point.

Signal	J3 Pins	Signal Name
Data Lines 1-8	1-8	BOUT1 - BOUT8
Strobe	9	STROUT
Crawl	10	CRWOUT
Roll	11	ROLOUT
Fast Roll	15	HIGH
Fast Crawl	18	HIGH

Signal	J3 Pins	Signal Name
Character Request	31	CHAREQ
Fast Load	34	FASTLOAD
Circuit Ground	19-27	GND

C) DATA INPUT. Data input lines are negative logic; all other inputs are positive logic.

D) INPUT. Signal Designations.

Signal	J4 Pins	Signal Names
Data Lines 1-8	1-8	BIN1 - BIN8
Data Ready Strobe	9	DRSIN
Data Request	11	DATREQ
Record Mark	33	RECMRK
Circuit Ground	19-29	GND

Control Keyboard

Check operation of the control keyboard as follows:

A) ADDRESS KEYS. Set multimeter to 10 V scale, and connect positive lead to VCC. Connect the negative side to the appropriate connector pin as noted below. Press the key associated with that pin. The meter should indicate 5 volts each time a key is pressed.

CAUTION: High voltage (200 volts) at pins J1-24 and J1-25.

Key	J1 Pins	Key	J1 Pins
Zero	10	4	04
1	01	5	05
2	02	6	06
3	03	7	07

Key	J1 Pins	Key	J1 Pins
8	08	Clear	26
9	09		

B) FUNCTION KEYS. With the multimeter connected as in A) above, connect negative lead to pins noted for the function keys and press appropriate key. Meter should indicate +5 volts.

Key	J1 Pins	Key	J1 Pins
Record	45	Crawl	48
Read	46	Erase	31
Roll	47	High	50

C) NIXIE READOUT. Ground the BCD leads in the unit, tens and hunderds "Nixies"; the display lights should read all zeros. (J1 pins 11-16, 36-41.)

Remote Keyboard

If the Titlefile system contains a Remote Keyboard, repeat the checks given for the control keyboard on the Remote Keyboard.

Integrated Circuit Signal Tracing

When tracing signals in the logic assembly and a signal failure is detected, replace the circuit generating the signal. If this does not correct the condition, check the circuit receiving the signal and the interconnecting wiring.

NOTE: To prevent static electricity damage to MOS chips, tie all leads together when the MOS chip is removed from the circuit.

DETAILED CIRCUIT DESCRIPTIONS

The following paragraphs provide detailed circuit descriptions of the Titlefile circuits. They are keyed to the schematic and logic diagrams provided in this section. A list of signal names, origin points and destinations, and signal functions, is also provided in this section.

In order to follow signal flow through the logic diagrams, the following should be remembered. All references to signal origin points and destinations in the origin signal list are given as two sets of numbers separated by a slash. Example: $\overline{\text{UNLRST}}$, from S6-10/9-8B to H7-6/9-6C. The S6 refers to the gate generating the signal; -10 refers either to the pin at which the signal appears, or to the output pin. 9-8B is the sheet and area on the diagram in which the gate is located (thus gate S6 is in sheet 9, at location 8B). All the circuit diagrams are sheets of Figure 5-1.

Tape Address Generation and Control Circuits

Addresses are selected by entering the appropriate three digits on the Address Control Keyboard. The signals generated by pressing the keys of the keyboard are $\overline{\text{ONE}}$, $\overline{\text{TWO}}$, $\overline{\text{THREE}}$, $\overline{\text{FOUR}}$, $\overline{\text{FIVE}}$, $\overline{\text{SIX}}$, $\overline{\text{SEVEN}}$, $\overline{\text{EIGHT}}$, $\overline{\text{NINE}}$ and $\overline{\text{ZERO}}$; these signals are routed to the decimal-to-binary decoder, illustrated in Figure 5-1, sheet 1 (gates A1-8, B1-6, B1-8, A2-3). The output of the decimal-to-binary decoder is in the form of signals B1, B2, B4 and B8; different combinations of these signals are generated to represent the different numbers entered on the keyboard. For example, the number six is represented by B2 and B4; seven is represented by B1, B2 and B4. In this manner, every decimal digit entered into the decoder is given a four-bit binary representation.

From the decimal-to-binary decoder, each four-bit number is routed to the address encoder, which is a series of shift registers illustrated in Figure 5-1, sheet 6; the shift registers generate the signals that locate the address on the magnetic tape. The first digit of the three-digit address represents the magnetic tape track number; this digit is shifted through the shift registers to the track register (H8).

The output of the track register is routed to the track decoders (C5 and C8), which convert the binary-coded digit to the appropriate (decimal) control signal; the control signal is then applied to the read/write control circuits, which enable the selected recording head.

The remaining shift registers are the 'tens' register (F8), an adder (C6), and the 'units' register (M10). The function of the adder is to "carry"; when the 'units' register reaches a count of nine, the adder increments the 'tens' register on the following count. Similarly, when the 'tens' register reaches a count of nine, the track register is incremented by the adder. The second and third digits of the address are the 'tens' digit and the 'units' digit, respectively; these are stored in the 'tens' register and the 'units' register.

The configuration of the address track is as follows: the first address is recorded near the splice in the magnetic tape loop. Each address comprises a series of eight zeros, followed by sixteen ones, followed by an eight-bit address.

The first address is 00. After the address there is a series of 34 zeros, after which the pattern is repeated: eight zeros, followed by sixteen ones, etc. Spacing is such that one hundred individual addresses are recorded on the address track.

The tape loop is normally stationary. When IC is generated, GO is produced (D5-8, sheet 1) and allows one revolution of the tape. Depression of either the READ or the RECORD switch generates a corresponding mode signal; these are RETM (retrieve from magnetic tape - F1-9) and STORM (store on magnetic tape - F1-12) illustrated in Figure 5-1, sheet 2. When either of these signals appear, they cause BUSY to be generated (B5-6); BUSY causes GO to start the tape loop (D5-8, sheet 1), and initiates a delay of approximately 200 milliseconds (E4-8, sheet 2), to allow tape loop speed stabilization.

At the end of the delay, the signal produced at H1-13 goes low; the contents of the address track are routed to the read logic (A7-8, A7-11, B8-3, H4-12) in the form of the READBK signal (S4-8), illustrated in Figure 5-1, sheet 4. As soon as a zero is read from the address track, ZSEEN (zero seen) is generated (H1-9). ZSEEN causes ONETST (ones test) to be generated (J6-1), which allows a counter (N6) to begin counting ones (sheet 7). The sixteenth one counted DEC 15 (J8-6), causes PRCOMP (permit compare - F2-12) and COMPFF (compare flip-flop - F2-9) to be set. PRCOMP remains set for one character time, during which the test for character equality is carried out. Refer to Figure 5-1, sheet 2. During this test, the 'units' and 'tens' shift registers are connected together as a closed loop (F8-10 to M10-1, M10-10 to F8-1), to the exclusion of the adder. All the data in the two registers is shifted through in serial form; this stream is tapped at the output of the 'tens' register, in the form of the signal ARSRD. ARSRD is routed to the comparison network (E2-6, 8, 11); in the comparison network, ARSRD is compared with the signal being read from the address track. In the event that the comparison is unsuccessful, ZSEEN remains set, and the process can begin again at the next address read from the tape. If, however, the comparison is successful, $\overline{\text{COMPFF}}$ (F2-8) goes low; the low $\overline{\text{COMPFF}}$, in turn, allows the SCOMPR (successful compare - H2-12) flip-flop to be set. Refer to Figure 5-1, sheet 2. SCOMPR resets ZSEEN (E1-4), thus halting the search-and-compare operation; SCOMPR also sets either WRTENA (write enable - F3-12) or RDCNT (read count - F4-12), according as the initial mode selected was STORM or RETM. WRTENA enables the recording operation; RETM enables the read playback operation (illustrated in Figure 5-1, sheet 3).

Read Buffer

Filling of the read buffer is initiated by the LOAD signal. In the roll and crawl modes, data from the magnetic tape is loaded into the MOS shift registers (Figure 5-1, sheet 9). At the end of the first line period, as given by ENLINE, the T-register is full, and contains 2 (or 3) 8-bit characters. At this time, a flip-flop (L3-9) is set, generating the signal TFULL (T-register full); data continues to enter the registers during the second line, and to shift out of the T-register into the M-register. Detection of the second ENLINE indicates the M-register is full; a flip-flop (L3-12) is set, generating the signal MFULL. A CNTUP (count up) signal is generated (at gate L6-8), and data continues to enter the MOS registers; as the third line enters the T-register, the first line enters the V-register. The next ENLINE generates another CNTUP (L4-4), which, together with MFULL, sets VFULL (K1-9). The first cycle of LOAD always lasts for three line periods, during which time the line counter is advanced from its initial condition (00) to the 02 condition. Reset of LOAD is effected by ENDPGE (end of page), which resets READ.

Each LOAD cycle lasts for approximately 10 milliseconds; during any given LOAD cycle, a CHAREQ (character request) signal will be generated by the DCU; CHAREQ and VFULL generate REQNLD (request unload) at M6-8 (sheet 9). The REQNLD signal enables the J input of a flip-flop (H7-1), which, at the time of the next CLKN (clock narrowed) synchronization signal sets the UNLOAD flip-flop (H7-9). The UNLOAD flip-flop can be set only if the VFULL signal is set; under normal conditions, once the V-register fills, it should empty after the end of the message. During each unload operation, one character is transmitted from the V-register into the input/output network. UNLOAD causes UNLOAD 1 to be generated (L10-13), which increments counter N2-12. On the eighth count, the outputs of N2 are nanded to give RCDTST (K9-8); when this signal goes low (on the ninth count) it triggers a one-shot oscillator (N1-8) which produces RCTSPD. Since DLOUT is low, RCTSPD causes RCSTR (Roll/Crawl Strobe) to be generated (P6-10). RCSTR, in turn, generates STROUT (strobe out) at D6-6 (sheet 5), which instructs the DCU to accept the output of the I/O network. STROUT must be at least a 2 microsecond pulse.

Magnetic Tape Read/Write Electronics

The writing circuitry (Figure 5-2) is common to all of the data tracks. The track to be written into is selected by a switching circuit, which allows a +20 volt source to be connected to the center tap of the recording head winding corresponding to the desired track. There are eight switching circuits, corresponding to the eight data tracks. The selection circuits are also enabled during the read operation; this establishes a zero reference potential on the center tap of the recording head, preventing undesired noise from being picked up.

The selected track signals TRK00 through TRK07, from the Tape Address Generation and Control Circuits, are routed to their respective switching circuits. The following discussion relates to the TRK00 switching circuits; the operation of the remaining seven circuits is exactly similar to that of the TRK00 circuit.

The track signal TRK00 controls transistor Q7A, keeping the transistor in the non-conducting state as long as TRK00 is not selected; Q7A conducts when TRK00 is selected; $\overline{\text{TRK SEL}}$ appears on the collector of Q7A, and is used to control the read amplifiers. The base of transistor Q8A is resistence-coupled to the collector of Q7A, while the emitter of Q8A is connected, through a protective diode, to a constant current soucre. The collector of Q8A is connected to the center tap of the recording head corresponding to physical track 1; thus, when $\overline{\text{TRK SEL}}$ is present, Q8A conducts.

If the constant current source is energized, current will be supplied to the center tap of the recording head. Once a constant current source is connected to the recording head, data recording can begin. The constant current source is energized by the $\overline{\text{WRITE}}$ signal. When the write operation is initiated, the input signal is grounded, and the collector of Q1 "goes high". Q2 is thus de-energized, and the voltage at its collector begins to drop; as it drops, it biases Q3 (connected as a diode), completing the voltage divider consisting of R6 and Q3. The voltage divider establishes a base potential for Q4, which supplies a constant current to recording head selection circuit transistor Q8A.

Actual writing of data is performed by the circuit consisting of transistors Q5 and Q6, common to all the recording heads. The output of this circuit is routed to the recording heads through two isolating diodes. The transistors are enabled by the WD and $\overline{\text{WD}}$ signals causing the flux transitions necessary for recording data on the magnetic tape; one transition per data bit for each logic zero, and two transitions per data bit for each logic one. During the read operation, both transistors are enabled; the isolation diodes are thus grounded, to prevent them from contributing noise to the read signal.

Each recording head has a tape read pre-amplifier associated with it. The two outputs of the recording head are routed into the input section of a differential amplifier. The input network consists of two resistors, two diodes and a capacitor. The function of the diodes is to limit excursion during the write operation, while the capacitor acts as a frequency limiter. In addition, a resistor and a capacitor are connected between the track select signal ($\overline{\text{TRK SEL}}$) and ground; thus, when a track is not selected, the voltage at diode CR6A is routed to the inverting side of the amplifier input. The amplifier output is thereby forced to its extreme negative value, reverse-biasing output CR7A; the recording head reading circuitry is thus effectively removed from additional amplification stages. Since only one track is selected at any time, only one input junction will be at ground potential.

In the selected circuit, diode CR6A is reverse-biased, preventing biasing current and noise from being applied to the operational amplifier input network.

The second stage of amplification is common to all tracks. Coupling capacitor recovery from track or read/write switching is less than 50 milliseconds; guard circuitry is included in the logic to prevent these transients from affecting the data. The amplifier output represents the derivative with respect to time of the flux changes; this output is routed to an operational amplifier, connected as a differentiator. The output of the differentiator is routed through a clipping circuit, and applied to a Schmitt trigger circuit. The output of the Schmitt trigger is a replica of the input WD signal; this signal is fed to an output buffer transistor, Q15, and to transistor Q14.

The signal $\overline{\text{AREAD}}$ is fed into the base of Q14, through a resistance network; this signal brackets the transition from the address track to the data tracks, forcing the Schmitt trigger to reset, and holding it there until the signals become stable. The output buffer transistor is connected to the read buffer input (Figure 5-1, sheet 9).

Input/Output Network (6)

Output data may enter the input/output network (Figure 5-1, sheet 5) from either the MOS shift registers [in the roll or crawl modes as signal SR (L8-12, sheet 9)] or from the tape read/write electronics in the form of signal READ 1 (in the normal read mode). If the Titlefile is wired for 32-character lines, the roll and crawl modes are inoperative. Both sources provide serially-coded characters, which must be converted to parallel-coded characters by the I/O network, for transmission to the DCU. Data is applied (via A10-8) to the I/O network shift register (C1-11, 15; C2-11, 15; C3-11, 15; C4-11, 15), bit by bit; each bit is shifted through the register to the next flip-flop as each additional bit comes in. Clocking of the shift register is accomplished during the write operation by the internally-generated CLOCK signal, and during the read operation, by the SPKDL (sprocket delay) address track synchronization signal (A10-11; D1-8; E10-8).

All flip-flops of the shift register have a common forced state, initiated by the WRTCLR signal (B10-8; D1-6). The "1" outputs of the flip-flops in the shift register, corresponding to seven bits of the output word, are applied to nand gates (B10-6, B7-8, B9-8, E10-12, E10-6, and B9-11).

The output of the flip-flop corresponding to the fifth bit of the output word is connected to an inverter (A8-12). The outputs of the gates and the inverter are fed to the DCU, which strobes them in as a single parallel-coded character.

Characters are received from the DCU in parallel form; each of the character's eight bits is applied to a nand gate (B8-6, B8-8, B8-11, A9-3, A9-8, A9-11, B9-3). The outputs of the input nand gates are connected to the forced-reset inputs of the shift register flip-flops; thus, the state of each flip-flop reflects the state of the corresponding input bit. CLOCKA and WRITE signals (A10-11) toggle the shift register, which has a constant input; the input is shaped by the flip-flops as it is shifted through the register, and routed as REG H to an output circuit where it is gated with WRITE and CLOCK (D3-6). The output of this gate clocks a flip-flop (H4-8), which generates $\overline{\text{WRTDAT}}$; $\overline{\text{WRTDAT}}$ is gated with WRTENA (S4-3) to produce WRTDAT, which goes to the tape read/write electronics.

Read/Write Control Electronics (7)

Pressing the READ switch on the address control keyboard causes the RETM (retrieve from magnetic tape) signal to be generated; (see Figure 5-1, sheet 3) this signal is applied to the J-input of a flip-flop (F4-14) in the read control electronics.

When the tape address generation and control circuits have located the selected address on the tape, the SCOMPR (successful compare) signal is generated. This signal toggles the input flip-flops (F3-1, F4-1) of the read/write control electronics, generating the RDCNT (read count) signal; RDCNT is applied to a flip-flop (F4-7, which, when clocked with DEC07 (decode 7) and SPKDL, produces the READ signal. The setting of READ switches the track select circuits from the address track to the track indicated by the decoder (C8), which is connected to the most significant digit register of the address register. Address selection then proceeds in the manner described in the paragraphs relating to address generation and control.

After the address has been located, the READ1 signals being produced as a result of signals being read from the tape are routed to the C1-15 flip-flop in the I/O shift register (via A10-1); the entire register is clocked by SPKDLA. When the clock causes DEC07 - the eighth bit-time - to be generated, STROUT (strobe out) is sent to the DCU; on receipt of this signal, the DCU accepts the character that is in the I/O register, and the cycle begins again.

Pressing the RECORD switch on the address control keyboard causes the STORM (store on magnetic tape) signal to be generated. STORM is routed to the J-input (F3-14) of the first flip-flop in the write section of the write control electronics.

As in the read operation, the input flip-flop is clocked by SCOMPR, generating WRTENA (write enable.

WRTENA shifts control of the operation to an internal crystal-controlled clock; this is necessary to ensure the data is recorded at the correct address, because reading of the address on the address track and recording cannot take place at the same time.

The second flip-flop (F3-9) in the write section of the write control electronics is controlled by the output of the internal clock (CLOCKA); this flip-flop ensures a smooth transition from the control of the address track to the control of the internal clock. The third flip-flop (H3-12) in this section is toggled by DEC15, which is generated after sixteen bit-times have elapsed, generating WRITE. WRITE (via J3-12, D4-1, D2-4) produces WRTCLR (see sheet 5), which forces the setting of all eight flip-flops of the input/output shift register; WRITE also causes (D2-4) DATREQ (data request) to be generated, routed to the DCU. The DCU responds, within six microseconds, with a flow of data to the input/output circuits of the Titlefile.

As each character is written on tape, data requests (D5-3) are transmitted to the DCU. At DEC07, which is the eighth bit-time, a character counter (N5 or P2) is advanced; the character counter causes ENLINE to be produced after the last count, (on the 25th or 33rd count) which blocks the data requests to the DCU.

In both the read and write operation, ENLINE (see sheet 8) and either WRITE or RETM, with DEC07 are combined to produce ENDPGE (end of page - M5-10); in the WRITE operation, this initiates a sequence in which WRITE and WRTENA are shut off for approximately 70 microseconds, during which the head circuitry can "recover" from the write operation, and control is switched back to the address track. The address flip-flop (H2-9) (see sheet 3) produces ADDRFF, causing the address in the address register to be incremented by one; ADDRFF is set for one character time, the completion of which causes $\overline{\text{PROEND}}$ (E7-6) to be generated if line 15 or RECMRK is high. $\overline{\text{PROEND}}$ terminates the write or the read operation [by producing TERM (B5-3, sheet 2)], clearing the flip-flops involved in writing or reading. (Strapping the Titlefile for 12-line page operation, as described in Section II, consists of holding LINE C high. LINE 15 is then produced on the twelfth line count.)

The roll and crawl modes of operation are described in the paragraphs discussing the read buffer. The roll and crawl operations are inoperative when the Titlefile is wired for 32-character lines.

Pressing the ROLL or the CRAWL switch on the address control keyboard initiates a flow of CHAREQ signals from the DCU (see sheet 3); however, the DCU will set up blank characters, until the READ switch on the address control keyboard is pressed. Pressing the READ switch initiates the normal search operation; generation of SCOMPR (H2-12, sheet 2), causes RDCNT to be set (F4-12, sheet 3).

One character time later, with the generation of DEC07, READ is produced (F4-9); $\overline{\text{READ}}$ goes low, resetting RDCNT. ROLL or CRAWL produce R/CRET, which, together with ALTIN, enable the generation of LOAD (H6-12, sheet 8). ENLINE generates CNTUP (L6-8) at DEC07 (sheet 9); this initiates the loading of the read buffer. Thus, in the roll and crawl modes, data is read from the tape into the read buffer, rather than into the I/O circuit.

Function Control Circuits

The two major function control circuits are the system clock (sheet 1) and the sprocket-detection circuit (sheet 4). The system clock is a self-contained, crystal-controlled multivibrator, which oscillates at a frequency of 1.18 megahertz; it produces the signal OSC; the frequency of OSC is divided by eight to give CLOCK, which is used throughout the system for timing when it is impossible to read from the address track (e.g. during the write operation).

The sprocket-detection circuit is fed the READBK signal (E8-1) from the magnetic tape read/write circuitry; when READBK goes low, E8 generates RDGATE (read gate) for a time T1 (see timing diagram, Figure 5-3). When RDGATE goes low, E9 produces ONERST (ones reset) for a time T2. Two Schmitt triggers (H9-11, 12), connected in series with an inverter separating them, are triggered by ONERST. After a time T4, the Schmitt triggers fire, producing SPKDL (sprocket delay); SPKDL has duration T5. SPKDL is the major timing signal used in the Titlefile; it is used to clock all operations.

Tape Capstan and Drive Motor Adjustment

If, during repair of the tape unit, it becomes necessary to remove or replace either the tape drive motor or capstan, perform the following adjustment when assembling the unit.

1) Place a tape cartridge in the tape receptor and slide capstan on motor shaft. Do not tighten setscrew.

2) Mount the drive motor and capstan frame assembly and tighten bolts enough to hold motor in position. Slide motor as far from cartridge end of mount as possible.

3) Position the capstan wheel so that it is aligned with the cartridge driver. Tighten the capstan setscrew.

4) Move motor and capstan assembly toward cartridge until capstan wheel contacts cartridge driver. Make sure that contact pressure is not too great or binding will occur. Tighten motor bolts, locking motor in position.

Signal Names And Origins

In order to follow signal flow through the logic diagrams, the following should be remembered. All references to signal origin points and destinations in the origin signal list (Table 5-2) are given as two sets of numbers separated by a slash. Example:-UNLRST, from S6-10/9-8B to H7-6/9-6C. The S6 refers to the gate generating the signal; -10 refers either to the pin at which the signal appears, or to the output pin. 9-8B is the sheet and area on the diagram in which the gate is located; thus gate S6 is in sheet 9, at location 8B. All the circuit diagrams are sheets of Figure 5-1.

Table 5-2.
SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
ADDRFF	H2-9/3-C3	B7-5/3-E4 F5-6/6-C4 L7-5/9-E5 N7-14/8-D3	Allows address mode.
-ADDRFF	H2-8/3-C3	B5-12/2-E1 E6-6/3-D6 J9-13/7-B4 K3-11/7-B2	
ADONE	D9-10/6-A2	C6-11/6-B3 D10-11/6-C2	Increments address by one.
ADTRAK	D9-4/6-C7	A8-5/6-C7 C5-12/6-B7	Selects address track.
-ADTRAK	A8-6/6-C7	S00-11	
-ADVP	K8-10/8-B2	K8-12/8-A3 L8-1/8-C2	Signifies end of character when Titlefile is in either read or write mode.
-AFP	H5-13/7-D8	D1-1/5-C1 D3-10/5-D2 K3-2/7-C7	Pulse advance in read mode; allows PREMBL for operation of super-third mode.
ALSCMP	P5-10/9-D5	A7-5/2-C6	Permits successful compare of operator-entered address with tape address.
ALTIN	S9-12/9-B1	L5-10/9-A2 L9-12/9-B2 M9-9/8-B7	Allows tape data to be entered when buffers are empty in roll or crawl mode.

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
ALWLD	N3-13/8-B7	H6-14/8-B7	Allows flip-flop H6 to load.
AREAD	S8-8/4-B2	S00-35	Provides one character delay from tape when Titlefile is in read mode.
-AREAD	S8-6/4-C3	H9-14/4-B6	
ARSRD	F8-10/6-B4	D8-3/6-C5 E2-9/2-B6 H8-5/6-B6 H10-1/6-D7 M10-1/6-B2	Most significant first digit of sector address.
-ARSRD	D8-4/6-C5	E2-4/2-C6	
A1	D8-6/6-D3	M10-2/6-B2	Binary bits 1, 2, 4, 8 for selection of address in address register.
A2	D8-8/6-E3	M10-3/6-B2	
A4	D8-10/6-D6	M10-4/6-B2	
A8	D8-12/6-E6	M10-5/6-B2	
BIN1	P00-18	B8-4/5-A2	Data input from DCU to shift register.
BIN2	P00-19	B8-9/5-A3	
BIN3	P00-20	B8-12/5-A3	
BIN4	P00-21	A9-1/5-A4	
BIN5	P00-22	A9-4/5-A5	
BIN6	P00-23	A9-9/5-A5	
BIN7	P00-24	A9-12/5-A5	
BIN8	P00-25	B9-1/5-A7	
BITA	N6-12/7-A6	C7-15/7-A7 N6-1/7-A6	Bit counts; counts data bits for proper timing and transfers.
BITB	N6-9/7-A6	C7-14/7-A7	
BITC	N6-8/7-A6	C7-13/7-A7	

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
BITD	N6-11/7-A6	H5-5/7-B6 J9-4/7-C7	Bit counts; counts data bits for proper timing and transfers.
BKUNLD	L7-3/9-D5	F7-7/5-E5 L2-12/5-D2 M2-1/9-E5	Allows line to unload in roll and crawl modes.
-BKUNLD	M2-12/9-E5	F5-14/5-D5 K9-5/9-C5 L7-2/9-D5	
BOUT1	B10-6/5-A2	R00-6	Data output from shift register to DCU.
BOUT2	B7-8/5-A3	R00-7	
BOUT3	B9-6/5-A4	R00-8	
BOUT4	A8-12/5-A4	R00-9	
BOUT5	B9-8/5-A5	R00-10	
BOUT6	E10-12/5-A6	R00-11	
BOUT7	E10-6/5-A7	R00-12	
BOUT8	B9-11/5-A7	R00-13	
BUSY	B5-6/2-D1	A5-5/2-D2 D5-12/6-B1 E4-3/2-E1 L10-5/1-A1 L10-8/6-E1	Signifies that Titlefile is in the write or read mode.
-BUSY	A5-6/2-D2	A3-5/2-C1 D5-9/1-C2 F1-7/2-C2 F1-14/2-B2	
B1	A1-8/1-A1	B2-2/1-B2 J4-1/6-D2	Data output from keyboard to address register.
B2	B1-6/1-B1	B2-3/1-B2 J4-2/6-D2	
B4	B1-8/1-B1	B2-5/1-B2 J5-1/6-D5	

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
B8	A2-3/1-C1	B2-6/1-B2 J5-2/6-D5	Data output from keyboard to address register.
-CADR	K10-13/2-A2	L10-9/6-D1 P5-2/2-A4	Clears address register to zero.
-CARYFF	F5-8/6-C4	D10-3/6-A3 D10-8/6-C1	Allows address to carry to next location.
CCTSEL	P1-12/7-E3	F6-1/8-B4	Selects either 24 or 32 character lines.
CHARA	N15-12/8-A4	N5-1/8-A4	Character count.
CHAREQ	P00-14	M2-3/9-E2 N4-1/9-E1 N4-13/9-E1 N4-14/9-E1	Character request from DCU. (Timing in roll or crawl mode for data acquisition.)
CHA24D	N5-8/8-A5	P1-4/7-E3	Signifies end of 24 character line.
CHA32D	P2-13/7-A5	P1-5/7-E3	Signifies end of 32 character line.
-CLCHOP	K4-8/2-A5	B3-1/2-D3 K2-2/6-E4	Signal to clear address register.
CLEAR	A2-11/1-C3	A3-10/2-B4 B2-9/1-B4	Signal from keyboard used to develop a termination.
-CLEAR	P00-31	A2-12/1-C3	
CLKDBL	M7-8/1-C6	L1-5/1-D6	Clock doubled.
-CLKDBL	L1-6/1-D6	D3-5/5-C4 J3-13/5-C4	
CLKN	M8-13/9-D4	H7-1/9-C4 K9-2/9-C5 M9-2/9-A3 S7-11/9-D7	Clock narrowed; used for proper strobe timing in both roll and crawl modes.
-CLKN	S7-10/9-D5	L10-12/9-D7	
CLKQUD	M7-9/1-C6	M9-1/9-A3	Clock quadrupled.
CLOCK	M7-11/1-C6	L1-13/1-D6	Basic timing signal for controller (75 KHZ).

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
-CLOCK	L1-12/1-D6	J3-2/5-C4 K5-1/1-D6 K5-2/1-D6 K5-4/1-D6 K5-5/1-D6 M8-11/9-D4	Basic timing signal for controller (75 KHZ).
CLOCKA	K5-6/1-D1	A3-9/2-B4 A10-13/5-C1 D3-4/5-C4 E3-11/3-A6 F3-5/3-A5 J7-5/3-A5 N3-6/5-E2 P5-15/2-D4 S5-7/9-D4 S5-8/9-D4 S5-9/9-D4 S9-10/5-E3	Clock pulse amplified to clock basic timing circuits in controller.
-CNTDWN	M9-6/9-D4	L4-5/9-D6 M6-12/9-D2 S7-1/9-D3	Character count for proper buffer emptying in roll and crawl modes.
CNTUP	M5-8/9-D4	P5-3/9-D2	Character count for proper buffer loading in roll and crawl modes.
-CNTUP	L6-8/9-D1	L4-4/9-D6 M5-9/9-D2	
-COMPFF	F2-8/2-B8	E1-8/2-D7	Signifies comparison in progress of operator-entered address with tape address.
COUT	C6-14/6-C3	A5-13/6-C4 F5-7/6-C4	Carry output bit of address adder.
-COUT	A5-12/6-C4	F5-10/6-C4	
-CRAWL	P00-35	B4-8/2-C4 J2-3/2-C4	Crawl signal from keyboard to controller to enter crawl mode.
CRET	B4-10/2-C4	B3-13/2-C4 K4-13/7-C6	Allows controller to read in crawl mode.
-CRET	B3-12/2-C4	B5-10/2-C5	

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
CRWOUT	J2-4/2-C4	P00-16	Crawl command to DCU.
-CURHME	K3-6/7-D7	B7-10/5-A3 B10-4/5-A2	Cursor home.
-CURUP	K6-6/7-D7	B7-9/5-A3 B9-9/5-A5 B9-12/5-A7 B10-1/5-A2	Cursor up.
DATREQ	D2-6/5-C7	A6-3/5-C7 R00-2	Data request to DCU for data in normal read mode.
DEC00	S7-8/5-E3	S9-9/5-E3	Decoded counts in controller for proper timing and strobing.
-DEC00	C7-1/7-A7	D4-2/5-C5 S7-9/7-A7	
-DEC01	C7-2/7-A7	B7-1/3-E3 D9-9/6-C2 J1-4/6-C2	
DEC02	J8-8/7-E5	K3-4/7-D7 K6-2/7-D6	
-DEC02	C7-3/7-A7	J7-12/7-A5 J8-9/7-E5 K6-5/7-D7	
-DEC03	C7-4/7-A7	D10-9/6-C1 J1-1/6-A2 J1-5/6-C2 J7-13/7-C5	
-DEC04	C7-5/7-A7	J9-10/7-C5	
-DEC05	C7-6/7-A7	J1-2/6-A2 J9-11/7-C5	
-DEC06	C7-7/7-A7	B7-13/3-E3 P1-1/7-E3	

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
DEC07	J8-4/7-B7	A7-4/2-D6 F2-3/2-A8 F2-10/2-B8 F4-5/3-B3 H2-3/2-B8 H2-10/3-C3 J9-3/7-C7 L6-5/8-C7 L6-10/9-D1 M3-9/4-B1	Decoded counts in controller for proper timing and strobing.
-DEC07	C7-9/7-A7	D4-6/5-D1 J8-3/7-B7 K8-3/8-B2 P1-2/7-E3	
DEC15	J8-6/7-C7	F2-7/2-B8 F2-14/2-A8 H3-1/3-A4	
-DEC23	J8-10/7-C5	J9-9/7-C5	
-DE2345	J8-12/7-C5	B7-2/3-E3 K2-3/7-D4	
DLOUT	D4-13/5-E5	D2-9/5-E6 F7-14/9-D3 M8-3/9-C4	Delete output to DCU for timing in roll and crawl modes.
DRSA	N3-4/5-E2	A9-2/5-A4 A9-5/5-A5 A9-10/5-A5 A9-13/5-A5 B8-5/5-A2 B8-10/5-A3 B8-13/5-A3 B9-2/5-A7 N3-3/5-E2	Signal from controller to DCU signifying that the controller is ready to accept data from DCU.
DRSIN	R00-4	D2-11/5-E1	
D1	M10-13/6-B2	C6-10/6-B3 F10-1/6-D7 J1-9/6-C1	Output from address register to first Nixie tube. (Least significant digit.)

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
D10	F8-13/6-B4	F10-5/6-D7 H8-2/6-B6	Output from address register to second Nixie tube.
D100	H8-13/6-B6	C5-15/6-B7 C8-15/6-A7 H10-2/6-D7 J4-9/6-D2	Output from address register to third Nixie tube. (Track selection.)
D2	M10-12/6-B2	C6-8/6-B3 F10-2/6-D7	Output from address register to first Nixie tube. (Least significant digit.)
D20	F8-12/6-B4	F10-6/6-D7 H8-3/6-B6	Output from address register to second Nixie tube.
D200	H8-12/6-B6	C5-14/6-B7 C8-14/6-A7 H10-3/6-D7 J4-4/6-D2	Output from address register to third Nixie tube. (Track selection.)
D4	M10-11/6-B2	C6-3/6-B3 F10-3/6-D7	Output from address register to first Nixie tube. (Least significant digit.)
D40	F8-11/6-B4	F10-7/6-D7 H8-4/6-B6	Output from address register to second Nixie tube.
D400	H8-11/6-B6	C5-13/6-B7 C8-13/6-A7 H10-4/6-D7 J5-9/6-D5	Output from address register to third Nixie tube. (Track selection.)
D8	M10-10/6-B2	C6-1/6-B3 F8-1/6-B4 F10-4/6-D7 J1-10/6-C1	Output from address register to first Nixie tube. (Least significant digit.)
D800	H8-10/6-B6	H10-5/6-D7 J5-4/6-D5	Output from address register to third Nixie tube. (Track selection.)
-ECSTR	J7-3/7-A3	D6-10/7-A4 E2-2/2-A6	Strobe signal generated after successful comparison of address has been made.
-EIGHT	P00-9	A2-1/1-C1	Data bit eight from keyboard.
EIPCLK	K2-12/6-D3	F8-8/6-B4 H8-8/6-B6 M10-8/6-B2	Clock signal used for shifting of address register.

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
ENDPGE	M5-10/3-C7	E3-4/3-B4 H3-5/3-A5 H6-3/8-B7	End of page signal to stop data transfer.
ENDTRG	E5-8/3-C2	E6-11/3-C5 H2-7/3-A3 J7-2/7-B4	End of transmission in write mode.
ENDTRP	A4-8/3-A7	E5-1/3-C2	End of write or read.
ENLINE	F6-9/8-C4	K6-10/8-C2 K8-11/8-A3 L6-2/8-D7 L6-9/9-D1	End of line; used for proper timing of either 24 or 32 character lines.
-ENLINE	F6-8/8-C4	D5-2/5-C6	
-ENWREN	E3-8/3-A6	A4-9/3-A7	Signifies end of wiring.
ERASE	B3-8/2-B4	A2-10/2-B4 L10-6/2-A1	Allows erasing of video display.
-ERASE	P00-36	A4-5/2-A1 B3-9/2-B3	
-ERASEA	A2-8/2-B4	B9-4/5-A4 B10-2/5-A2 B10-12/5-A1 D6-2/5-D3 E10-1/5-A6 E10-3/5-A7	
-ETRTRM	E6-13/3-C5	F3-2/3-A2 F3-6/3-A3 F4-6/3-B3 H3-6/3-A5	Signifies end of transmission and resets write flip-flops.
-FIVE	P00-6	A1-3/1-A1 B1-10/1-B1	Data bit five from keyboard.
-FOUR	P00-5	B1-9/1-B1	Data bit four from keyboard.
FSTLD	K1-12/1-B7	R00-21	Blanks video screen momentarily during normal read mode. (Eliminates video flashes.)

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
F9A	F9-3/2-A3	C9-9/2-A3 F9-2/2-A3	Enabling signal to permit "and" operation of gate F9.
F9B	F9-6/2-A3	F9-5/2-A3	
GENCLR	B3-2/2-D3	A5-1/2-D4 N2-2/9-C8	Clears MOS buffer.
-GENCLR	A5-2/2-D4	B5-1/2-E5 B10-9/5-C1 F2-2/2-A8 H2-2/2-D8	
GO	D5-8/1-C2	S00-33	Starts tape loop.
H9A	H9-3/4-B6	C9-10/4-B7 H9-2/4-B6	Enabling signal ta permit "and" operation of gate H9.
H9B	H9-6/4-B5	C10-9/4-B5 H9-5/4-B5	
-IC	R10-14/1-C2	A2-13/1-C3 D5-10/1-C2	Initial clear.
-INACLK	A7-3/3-E5	D10-5/6-C3 K2-13/6-D3	Increments address clack.
INCADR	A8-4/3-E5	A7-1/3-E5 J4-5/6-D2 J4-10/6-D2 J5-5/6-D5 J5-10/6-D5	Enables output of address register to select address.
-INCADR	B7-6/3-E4	A8-3/3-E5 D5-13/6-B1 D9-8/6-A2	
-KB/CLR	B2-10/1-B4	A4-1/2-A1 P6-5/2-A5	Keyboard clear from address keyboard.
KBSTR	A3-12/1-B3	A3-3/2-C1 B2-8/1-B4	Keyboard strobe.
KYCLR	B3-6/2-A4	K10-1/2-A4 P3-6/2-A5 P5-1/2-A4	Keyboard clear.

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
LDP	P6-2/2-A5	A3-4/2-C1 P6-3/2-A6	Load pulse; allows read and write command flip-flops.
-LDP	P6-4/2-A6	B2-12/2-B1 B4-3/2-C1	
LDTWO	K10-9/9-D2	B6-1/9-D5 B6-9/9-D6 S10-2/9-D7	Allows the loading of two lines of data from tape to MOS registers in roll or crawl mode.
LINEA	N7-12/8-D3	L4-1/8-C3 N7-1/8-D3	Line counts of page used for timing.
LINEB	N7-9/8-D3	L4-2/8-C3	
LINEC	N7-8/8-D3	P1-3/7-E3	
LINED	N7-11/8-D3	L5-13/8-D3	
LINE15	L1-10/8-D4	D2-13/5-C2 E6-2/3-D5	
LOAD	H6-12/8-B7	H6-6/9-C1 H6-7/9-C1 L3-7/9-B7 L5-9/9-A2	Allows the loading of data into the read buffers.
-LOAD	H6-13/8-B7	B6-5/9-D6 B6-10/9-D6 J8-1/8-B7 P9-15/8-B2 S10-5/9-D8	
LOADA	J8-2/8-B7	L6-13/9-D1 L7-12/9-A1 M2-9/9-A3 M3-1/9-A5 S10-3/9-D7	LOAD signal amplified.
LOLINE	J6-4/7-C2	K2-11/7-D6	Tape track command when Titlefile is in super-third operation.
L1	F10-14/6-D7	P00-10	Nixie tube decodes from address register.

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
L10	F10-10/6-D7	P00-37	Nixie tube decodes from address register.
L100	H10-13/6-D7	R00-1	
L2	F10-13/6-D7	P00-11	
L20	F10-9/6-D7	P00-38	
L200	H10-12/6-D7	R00-5	
L4	F10-12/6-D7	P00-12	
L40	F10-8/6-D7	P00-39	
L400	H10-11/6-D7	R00-14	
L8	F10-11/6-D7	P00-13	
L80	H10-14/6-D7	P00-40	
L800	H10-10/6-D7	R00-15	
MFULL	L3-12/9-B7	K1-7/9-D8 L2-9/9-C2 M6-4/9-B3 S9-2/9-B1	Signifies M-register is full.
-MFULL	L3-13/9-D7	B6-2/9-D5 B6-4/9-D6 J6-9/9-E4 K4-1/9-E4 P5-4/9-D2	
MO1	R4-4/9-B4	S2-4/9-A4	Enables loading of M-register.
MO2	R5-4/9-B5	S2-6/9-A4	Enables unloading of M-register.
-NDTEST	D8-2/5-D2	L2-11/5-D2 L5-4/5-E4	Two microsecond pulses generated at the end of each character during read mode.
-NINE	P00-30	A1-5/1-A1 A2-2/1-C1	Data bit nine from keyboard.
NORMRT	B4-13/2-D6	A8-1/5-C2 K2-10/7-D6 M8-8/8-E2	Allows Titlefile to operate in normal read mode.

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
N4A	N4-3/9-E1	N4-2/9-E1 P3-12/9-E1	Enabling signal to permit "and" operation of gate N4A.
-ONE	P00-2	A1-1/1-A1	Data bit one from keyboard.
ONERST	E9-8/4-B4	A7-12/4-D1 H6-5/9-C1 H9-1/4-B6 H9-7/4-B5 H9-8/4-B5 H9-9/4-B5	Permits reading of first 16 ones from tape.
-ONERST	E9-6/4-B4	L10-3/9-C2 S6-11/9-B6	
ONETST	J6-1/7-A2	J3-5/7-A3 J3-9/7-B4	
ONRSTD	H9-11/4-B5	A8-9/4-B6 S6-12/2-B6	Signal used to generate the sprocket pulse.
OSC	M5-4/1-D4 N8-5/1-C5	M7-14/1-C6	Oscillator output to clock circuits (1.18 MHZ).
-PCSTR	J3-6/7-A3	D6-9/7-A4 E2-1/2-A6	Strobe signal generated after first eight zeros preceeding sector address are read from tape.
PGLNCT	P1-14/7-E3	L5-2/8-D3	Allows selection of either 12 or 15 line operation.
PRCOMP	F2-12/2-A8	J6-3/7-A2	Permits strobe signal generated after successful comparison has been made.
-PRCOMP	F2-13/2-A8	D9-2/6-C1 J1-12/7-A1	
PREMBL	J2-10/7-C8	D3-9/5-D2 K3-3/7-D7 K6-4/7-D7	Permits operation of super-third mode.
-PREMBL	K3-12/7-C7	E10-2/5-A6 E10-4/5-A7 J2-11/7-C8	

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
-PROEND	E7-6/3-D6	B5-2/2-E5 K10-2/2-A2	Signifies that address has been incremented by one and terminates read and write operations.
PSTWRD	H3-9/3-A5	E1-11/3-B6 E3-9/3-A6	Signifies end of last character written on tape.
R/CRET	B5-8/2-C5	A5-9/2-C6 B4-11/2-D6 M9-10/8-B7	Allows Titlefile to enter roll mode.
-R/CRET	A5-8/2-C6	E6-8/3-D5 K1-14/1-B7 M6-2/9-D5	
RCDLTS	S5-12/9-D3	F7-1/9-D3 L7-9/9-C3	Roll and crawl mode pulse signals used to set up proper timing for data transfer.
RCDTST	M5-12/9-C6	N1-2/9-B7	
-RCDTST	K9-8/9-C6	M5-13/9-C6	
-RCENSR	F7-8/5-E5	H1-14/2-D3 K4-2/9-E4	
RCSTR	M8-1/9-C4	M9-5/9-D4 P6-11/9-C4	
-RCSTR	P6-10/9-C4	D6-4/5-D3 H7-2/9-C4	
RCTSPD	N1-8/9-B7	L7-10/9-C3 S5-1/9-C3 S5-13/9-C3 S5-14/9-C3 S6-8/9-B8	
-RCTSPD	N1-6/9-B8	L5-3/5-D4	
RDCNT	F4-12/3-B2	F4-7/3-B3 K1-1/1-B7 M3-10/4-B1 M6-1/9-D5 N3-9/8-B6	Read count; allows reading of read flip-flop.

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
-RDCNT	F4-13/3-B2	K3-9/7-B2 K4-5/8-B7	Read count; allows reading of read flip-flop.
RDGATE	E8-8/4-B2	H4-14/4-C3	Signifies the reading of data from tape at a 9.7 microsecond pulse rate.
-RDGATE	E8-6/4-B3	E8-2/4-B3 E9-3/4-B4	
-RDSHFT	E10-8/5-D1	D1-13/5-C1 D4-5/5-D1	Signifies data being read on basic timing pulse rate of controller.
READ	F4-9/3-B3	A10-2/5-B1 D9-5/6-C7 E3-3/3-B4 E10-9/5-D1 H6-2/8-B7 J6-11/8-A2	Allows Titlefile to enter read mode.
-READ	F4-8/3-B3	F4-2/3-B2 K3-10/7-C2	
-READAT	S00-1	S4-12/4-A1 S4-13/4-A1	Signifies data from tape.
READBK	S4-8/4-A2	A7-9/4-C1 E8-1/4-B2	
-READBK	P00-33	A4-4/2-A1 B4-2/2-C1	
READ1	H4-12/4-C3	A7-13/4-D1 A10-1/5-B1 E1-3/2-E3 E2-5/2-C6 J3-3/7-A3 L7-13/9-A1	Allows Titlefile to read the first 16 ones from tape to allow the compare strobe.
-READ1	H4-13/4-C3	A7-10/4-C1 E2-10/2-B6 J3-10/7-B4	
RECMRK	F5-12/5-D5	E6-3/3-D5 P00-26	Record mark; stops data transfer.
-RECMRK	F5-13/5-D5	A6-4/3-D5	

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESCRIPTION	FUNCTION
-RECORD	P00-32	A4-2/2-A1 B2-11/2-B1	Output record command from keyboard.
REGA	C1-15/5-B2	B10-5/5-A2 C1-9/5-B3	Shift register data used to and from DCU.
-REGA	C1-14/5-B2	C1-12/5-B3 D4-12/5-E5 S10-12/5-D3	
REGB	C1-11/5-B3	B7-11/5-A3 C2-4/5-B3 D7-2/5-D4	
-REGB	C1-10/5-B3	C2-16/5-B3	
REGC	C2-15/5-B3	B9-5/5-A4 C2-9/5-B4 D7-3/5-D4	
-REGC	C2-14/5-B3	C2-12/5-B4	
REGD	C2-11/5-B4	A8-13/5-A4 C3-4/5-B5 D7-4/5-D4	
-REGD	C2-10/5-B4	C3-16/5-B5	
REGE	C3-15/5-B5	B9-10/5-A5 C3-9/5-B6 D7-5/5-D4	
-REGE	C3-14/5-B5	C3-12/5-D6	
REGF	C3-11/5-B6	C4-4/5-B6 D7-6/5-D4 E10-13/5-A6	
-REGF	C3-10/5-B6	C4-16/5-B6	
REGG	C4-15/5-B6	C4-9/5-B7 D7-11/5-D4 E10-5/5-A7	
-REGG	C4-14/5-B6	C4-12/5-B7	

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
REGH	C4-11/5-B7	B9-13/5-A7 B3-2/5-C4	Shift register data used to and from DCU.
REQNFF	H7-12/9-C4	K9-1/9-C5	Signifies presence of REQNLD.
REQNLD	M6-8/9-E3	H7-14/9-C4	Pulse of approximately 30 microseconds, to request to unload a line in roll or crawl mode.
RETM	F1-9/2-C2	F4-14/3-B2 H5-2/7-E4 H5-14/7-E4	Retrieve from tape; signifies Titlefile is in read mode.
-RETM	F1-8/2-C2	B4-6/2-B4 B4-9/2-C4 B4-12/2-D6 B5-5/2-D1 L4-13/8-C6	
-ROLL	P00-34	B4-5/2-B4 J2-1/2-B4	Roll signal from keyboard to controller to enter roll mode.
ROLOUT	J2-2/2-B4	P00-15	Roll command to DCU.
RRET	B4-4/2-B4	B3-11/2-B4	Allows controller to read in roll mode.
-RRET	B3-10/2-B4	B5-9/2-C5	
SAMPLE	S7-12/9-E4	L9-10/9-B2	Timing pulse used when unloading MOS registers.
-SAMPLE	L9-3/9-A3	S7-13/9-E4	
SCOMPR	H2-12/2-D8	E1-5/2-E2 F3-1/3-A2 F4-1/3-B2 F5-1/7-E4 K3-13/7-C7 N3-8/8-C7	Indicates successful comparison of operator-entered address with tape address.
-SCOMPR	H2-13/2-D8	H10-10/5-C1 J1-13/7-A1 J9-5/7-C7	

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATIONS	FUNCTION
-SEVEN	P00-8	A1-4/1-A1 B1-5/1-B1 B1-13/1-B1	Data bit seven from keyboard.
SHFTA	N2-12/9-C8	K9-10/9-C6 N2-1/9-C8	Shift bits used to set up RCDTST.
SHFTB	N2-9/9-C8	K9-12/9-C6	
SHFTC	N2-8/9-C8	K9-13/9-C6	
-SIX	P00-7	B1-4/1-B1 B1-12/1-B1	Data bit six from keyboard.
SPKDL	H9-12/4-B6	A8-11/4-B7	Sprocket delay pulse used as basic timing signal initiated from reading of address track.
-SPKDL	A8-10/4-B7	D9-3/6-C1 K5-9/4-C7 K5-10/4-C7 K5-12/4-C7 K5-13/4-C7 P9-7/4-C7	
SPKDLA	K5-8/4-C7	A7-2/3-E5 D3-13/5-D2 E3-5/3-B4 E10-11/5-D1 H1-5/2-E4 H2-1/2-C8 H2-5/3-C3 J3-4/7-A3 J3-11/7-B4 J7-1/7-A3 J7-9/7-B3 J9-1/7-B4	
SPKDLE	L2-4/9-E2	L5-11/9-A2 M2-11/9-A3 M3-13/9-A5	Timing pulse used when loading MOS registers.
SR	L8-12/9-A8	A10-4/5-B1	Data signal output from MOS register.
-SR	R8-2/9-A7	L8-13/9-A8	

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
STORM	F1-12/2-B2	F3-14/3-A2 K6-1/7-D6 M8-9/8-E2	Store on tape; signifies Titlefile is in read mode.
-STORM	F1-13/2-B2	B5-4/2-D1 K3-5/7-D7	
-STRLD	A3-6/2-C1	K2-1/6-D3	Initializes clock signal used to load address register.
STROUT	A6-2/5-D3	A6-1/5-D3 R00-3	Strobe pulse to enable data to be transmitted to DCU.
S5A	S5-3/9-E1	P4-10/9-E1 S5-2/9-E1	Enabling signal to permit "and" operation of gate S5A.
S5B	S5-6/9-D4	P4-9/9-D4 S5-5/9-D4	Enabling signal to permit "and" operation of gate S5B.
TERM	B5-3/2-E5	A5-3/2-D6 E1-6/2-E2 E1-12/3-B6 E6-12/3-C5 S6-9/9-B8 S7-3/2-E6 S7-5/2-E6	Terminate; clears flip-flops upon completion of either read or write mode.
-TERM	A5-4/2-D6	F1-2/2-B2 F1-6/2-C2 F5-2/5-D5	
-TERMA	S7-4/2-E6	K1-6/9-D8 L3-2/9-D7 L3-6/9-D7	Termination signal amplified.
-TERMB	S7-6/2-E6	F7-6/5-E5 H2-6/3-C3 H4-2/4-C3 K1-2/1-B7 K7-12/7-B5 M2-13/9-E5 S9-3/8-B3	Termination signal amplified.
TFULL	L3-9/9-B7	P5-11/9-D5 S9-1/9-B1	Signifies that T-register is full.

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
-TFULL	L3-8/9-D7	J6-8/9-D2 L2-8/9-C2 S10-6/9-D7	Signifies that T-register is full.
-THREE	P00-4	A1-2/1-B1 B1-2/1-B1	Data bit three from keyboard.
-TK00	C5-1/6-B7	S00-3	Output signals from controller which selects tape track.
-TK01	C5-2/6-B7	S00-4	
-TK02	C5-3/6-B7	S00-5	
-TK03	C5-4/6-B7	S00-6	
-TK04	C5-5/6-B7	S00-7	
-TK05	C5-6/6-B7	S00-8	
-TK06	C5-7/6-B7	S00-9	
-TK07	C5-9/6-B7	S00-10	
TO1	R2-4/9-B3	S1-4/9-A3	Enables loading of T-register.
TO2	R3-4/9-B3	S1-6/9-A3	Enables unloading of T-register.
-TRAKD0	C8-1/6-A7	P10-1/7-C1	Track decodes used in super-third operation.
-TRAKD1	C8-2/6-A7	P10-2/7-C1	
-TRAKD2	C8-3/6-A7	P10-3/7-C1	
-TRAKD3	C8-4/6-A7	P10-4/7-C1	
-TRAKD4	C8-5/6-A7	P10-5/7-C1	
-TRAKD5	C8-6/6-A7	P10-6/7-C1	
-TRAKD6	C8-7/6-A7	P10-7/7-C1	
-TRAKD7	C8-9/6-A7	P10-8/7-C1	
-TWO	P00-3	B1-1/1-B1	Data bit two from keyboard.

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
ULOAD1	L10-13/9-C7	K9-9/9-C6 L8-3/9-B2 N2-14/9-C8	Signifies unload data command to MOS registers.
-ULOAD1	L8-4/9-B2	D1-12/5-C1 M1-1/9-B2 M1-12/9-B4 M4-9/9-B5	Signifies unload data command to MOS registers.
UNLOAD	H7-9/9-C6	A10-5/5-B1 L9-9/9-B2	
-UNLOAD	H7-8/9-C6	K9-4/9-C5 L9-2/9-A1 L10-11/9-C7	
-UNLRST	S6-10/9-B8	H7-6/9-C6	Allows unload of MOS registers.
VFULL	K1-9/9-D8	F7-2/9-D3 H7-7/9-C6 K10-6/9-D2 M2-5/9-E2 M6-5/9-B3 P5-13/9-D5 S9-13/9-B1	Signifies that V-register is full.
-VFULL	K1-8/9-D8	M3-2/9-A5 M4-4/9-C5	
VO1	R6-4/9-B6	S3-4/9-A6	Enables loading of V-register.
VO2	R7-4/9-B6	S3-6/9-A6	Enables unloading of V-register.
WRITE	H3-12/3-A4	A10-12/5-C1 D3-1/5-C4 H3-7/3-A5 J3-1/5-C4 J6-12/8-A2 S9-11/5-E3	Allows Titlefile to enter write mode.
-WRITE	H3-13/3-A4	L4-12/8-C6 S00-34	
-WRTCLK	J7-6/7-B3	D6-12/7-A4	Basic timing pulse of Titlefile when in write mode.

Table 5-2. (Cont'd.)

SIGNAL NAMES AND ORIGINS

SIGNAL NAME	ORIGIN	DESTINATION	FUNCTION
-WRTCLR	D2-4/5-C7	B10-13/5-C1	Pulse to clear all write flip-flops.
WRTCNT	F3-9/3-A3	H3-14/3-A4 J7-4/7-B3	Allows write flip-flops when Titlefile is in write mode.
WRTDAT	S4-3/5-C5	S00-21	Signifies data to tape.
-WRTDAT	H4-8/5-C5	S4-2/5-C5 S00-2	
WRTENA	F3-12/3-A2	D9-6/6-C7 F3-7/3-A3 H4-6/5-C5 S4-1/5-C5	Allows Titlefile to enter write mode.
-ZERO	P00-1	A3-1/1-B3	Data bit zero from keyboard.
-ZSEEN	H1-8/2-E4	J6-2/7-A2	Signifies the presence of eight zeros before address on tape; allows address compare.

Table 5-3.

ADDRESS CONTROL KEYBOARD WIRING

SIGNAL	FROM	TO	COLOR
-ZERO	PC1-13	J1-10	BLK
"	PC1-14	KB0-1	BLK
-ONE	PC1-15	J1-1	BRN
"	PC1-16	KB1-1	BRN
-TWO	PC1-17	J1-2	RED
"	PC1-18	KB2-1	RED
-THREE	PC1-19	J1-3	ORN
"	PC1-20	KB3-1	ORN
-FOUR	PC1-21	J1-4	YEL
"	PC1-22	KB4-1	YEL
-FIVE	PC1-23	J1-5	GRN
"	PC1-24	KB5-1	GRN
-SIX	PC1-25	J1-6	BLU
"	PC1-26	KB6-1	BLU
-SEVEN	PC1-27	J1-7	VIO
"	PC1-28	KB7-1	VIO
-EIGHT	PC1-29	J1-8	GRAY
"	PC1-30	KB8-1	GRAY
-NINE	PC1-31	J1-9	WHT
"	PC1-32	KB9-1	WHT
-CLEAR	PC1-33	J1-26	BLK/WHT
"	PC1-34	KBCLR-1	BLK/WHT
-READ	PC1-3	J1-46	RED/WHT
"	PC1-4	SW4-4	RED/WHT
-ROLL	PC1-5	J1-47	ORN/WHT
"	PC1-6	SW6-1	ORN/WHT
-CRAWL	PC1-7	J1-48	YEL/WHT
"	PC1-8	SW5-1	YEL/WHT
-ERASE	PC1-9	J1-31	GRN/WHT
"	PC1-10	SW1-4	GRN/WHT
-RECORD	PC1-1	J1-45	BRN/WHT
"	PC1-2	SW3-4	BRN/WHT
HIGH	PC1-11	J1-50	BLU/WHT
"	PC1-12	SW7-1	BLU/WHT
RECORD ALLOW	SW2-4	SW3-2	GRAY/WHT
+200VDC	PC1-41	J1-24	GRAY/WHT
"	PC1-42	SW8-1	GRAY/WHT
"	PC1-43	SW8-2	GRAY/WHT
DEL200	J1-25	SW8-6	GRAY/WHT
+5VDC	J1-21	PC1-40	VIO/WHT
"	PC1-40	SW1-A	VIO/WHT
"	SW1-A	SW2-A	VIO/WHT
"	SW2-A	SW3-A	VIO/WHT
"	SW3-A	SW4-A	VIO/WHT

Table 5-3. (Cont'd.)

ADDRESS CONTROL KEYBOARD WIRING

SIGNAL	FROM	TO	COLOR
+5VDC	SW4-A	SW5-A	VIO/WHT
"	SW5-A	SW6-A	VIO/WHT
"	SW6-A	SW7-A	VIO/WHT
L1	J1-11	M1-B	BRN
L2	J1-12	M1-C	RED
L4	J1-13	M1-D	ORN
L8	J1-14	M1-A	YEL
L10	J1-15	M2-B	GRN
L20	J1-16	M2-C	BLU
L40	J1-36	M2-D	VIO
L80	J1-37	M2-A	WHT
L100	J1-38	M3-B	BLK/WHT
L200	J1-39	M3-C	BRN/WHT
L400	J1-40	M3-D	RED/WHT
L800	J1-41	M3-A	ORN/WHT
LAMP CONT.	SW1-4	SW1-B	BLK
"	SW1-2	SW2-B	BLK
"	SW3-2	SW3-B	BLK
"	SW4-4	SW4-B	BLK
"	SW5-4	SW5-B	BLK
"	SW6-4	SW6-B	BLK
"	SW7-4	SW7-B	BLK
DELGND	J1-19	SW8-5	BLK
GND	SW1-2	PC1-37	BLK
"	J1-50	PC1-38	BLK
"	SW8-3	PC1-39	BLK
"	SW8-4	PC1-40	BLK
"	SW1-2	SW2-2	BLK
"	SW2-2	SW4-2	BLK
"	SW4-2	SW5-2	BLK
"	SW5-2	SW6-2	BLK
"	SW6-2	SW7-2	BLK
"	SW8-4	KB0-2	BLK
"	KB0-2	KB1-2	BLK
"	KB1-2	KB2-2	BLK
"	KB2-2	KB3-2	BLK
"	KB3-2	KB4-2	BLK
"	KB4-2	KB5-2	BLK
"	KB5-2	KB6-2	BLK
"	KB6-2	KB7-2	BLK
"	KB7-2	KB8-2	BLK
"	KB8-2	KB9-2	BLK
"	KB9-2	KBCL-2	BLK

Table 5-4.

CONTROLLER LOGIC WIRING

SIGNAL	FROM	TO	SIGNAL	FROM	TO
-ZERO	P00-1	J5-10	L80	P00-40	J5-37
"	J5-10	J6-10	"	J5-37	J6-37
-ONE	P00-2	J5-1	CHAREQ	P00-14	J3-31
"	J5-1	J6-1	ROLOUT	P00-15	J3-11
-TWO	P00-3	J5-2	CRWOUT	P00-16	J3-10
"	J5-2	J6-2	BIN1	P00-18	J4-1
-THREE	P00-4	J5-3	BIN2	P00-19	J4-2
"	J5-3	J6-3	BIN3	P00-20	J4-3
-FOUR	P00-5	J5-4	BIN4	P00-21	J4-4
"	J5-4	J6-4	BIN5	P00-22	J4-5
-FIVE	P00-6	J5-5	BIN6	P00-23	J4-6
"	J5-5	J6-5	BIN7	P00-24	J4-7
-SIX	P00-7	J5-6	BIN8	P00-25	J4-8
"	J5-6	J6-6	RECMRK	P00-26	J4-33
-SEVEN	P00-8	J5-7	GND	P00-28	CH.GND
"	J5-7	J6-7	"	P00-29	J5-43
-EIGHT	P00-9	J5-8	"	J5-43	J4-19
"	J5-8	J6-8	"	J4-19	J3-19
-NINE	P00-30	J5-9	"	P00-27	R00-23
"	J5-9	J6-9	L100	R00-1	J5-38
-CLEAR	P00-31	J5-26	"	J5-38	J6-38
"	J5-26	J6-26	L200	R00-5	J5-39
-READ	P00-33	J5-46	"	J5-39	J6-39
"	J5-46	J6-46	L400	R00-14	J5-40
-ROLL	P00-34	J5-47	"	J5-40	J6-40
"	J5-47	J6-47	L800	R00-15	J5-41
-CRAWL	P00-35	J5-48	"	J5-41	J6-41
"	J5-48	J6-48	DATREQ	R00-2	J4-11
-ERASE	P00-36	J5-31	STROUT	R00-3	J3-9
"	J5-31	J6-31	DRSIN	R00-4	J4-9
-RECORD	P00-32	J5-45	BOUT1	R00-6	J3-1
"	J5-45	J6-45	BOUT2	R00-7	J3-2
L1	P00-10	J5-11	BOUT3	R00-8	J3-3
"	J5-11	J6-11	BOUT4	R00-9	J3-4
L2	P00-11	J5-12	BOUT5	R00-10	J3-5
"	J5-12	J6-12	BOUT6	R00-11	J3-6
L4	P00-12	J5-13	BOUT7	R00-12	J3-7
"	J5-13	J6-13	BOUT8	R00-13	J3-8
L8	P00-13	J5-14	+5VDC	R00-20	J5-21
"	J5-14	J6-14	"	J5-21	J6-21
L10	P00-37	J5-15	FASTLOAD	R00-21	J3-34
"	J5-15	J6-15	-READAT	S00-1	J7-1
L20	P00-38	J5-16	WRTDAT	S00-2	J7-13
"	J5-16	J6-16	-TK00	S00-3	J7-3
L40	P00-39	J5-36	-TK01	S00-4	J7-4
"	J5-36	J6-36	-TK02	S00-5	J7-5

Table 5-4. (Cont'd.)

CONTROLLER LOGIC WIRING

SIGNAL	FROM	TO	SIGNAL	FROM	TO
-TK03	S00-6	J7-6	GND	TB4-3	J7-18
-TK04	S00-7	J7-7	"	J7-36	CH.GND
-TK05	S00-8	J7-8	+5VDC	R00-20	J5-21
-TK06	S00-9	J7-9	"	J5-21	J6-21
-TK07	S00-10	J7-10	"	TB3-1	J7-21
-ADTRAK	S00-11	J7-11	+20VDC	TB4-1	J7-19
-WRTDAT	S00-21	J7-12	-20VDC	TB3-2	J7-20
-WRITE	S00-34	J7-14	HIGH	J3-15	J3-18
-AREAD	S00-35	J7-15	"	J3-18	J5-50
GO	S00-33	J7-16	"	J5-50	J6-50
GND	S00-40	J7-17	DELGND	J5-19	J6-43
"	S00-23	J7-2	DEL200	J5-24	J6-25

Table 5-5.

READ/WRITE AMPLIFIER BOARD WIRING (TAPE UNIT)

SIGNAL	FROM	TO	COLOR
TRAKD1	P1-28	TK1-S	BRN
"	P1-27	TK1-F	GRN/WHT
"	P1-9	TK1-C	BRN/WHT
TRAKD2	P1-31	TK2-S	RED
"	P1-30	TK2-F	GRN/WHT
"	P1-12	TK2-C	RED/WHT
TRAKD3	P1-25	TK3-S	ORN
"	P1-24	TK3-F	GRN/WHT
"	P1-6	TK3-C	ORN/WHT
TRAKD4	P1-14	TK4-S	YEL
"	P1-13	TK4-F	GRN/WHT
"	P1-32	TK4-C	YEL/WHT
TRAKD6	P1-22	TK6-S	BLU
"	P1-21	TK6-F	GRN/WHT
"	P1-3	TK6-C	BLU/WHT
TRAKD7	P1-2	TK7-S	VIO
"	P1-1	TK7-F	GRN/WHT
"	P1-20	TK7-C	VIO/WHT
TRAKD8	P1-11	TK8-S	BLK
"	P1-10	TK8-F	GRN/WHT
"	P1-29	TK8-C	BLK/WHT
TRAKD9	P1-8	TK9-S	WHT
"	P1-7	TK9-F	GRN/WHT
"	P1-26	TK9-C	BLK
ADTRAK	P1-5	5-ADD-S	GRN
"	P1-4	5-ADD-F	GRN/WHT
"	P1-23	5-ADD-C	BLU/WHT
GND	P1-37	G3	BLK
-READAT	P2-1	$\overline{RD}$	RED/WHT
GND	P2-2	G1	BLK
-TK00	P2-3	$\overline{00}$	BRN
-TK01	P2-4	$\overline{01}$	RED
-TK02	P2-5	$\overline{02}$	ORN
-TK03	P2-6	$\overline{03}$	YEL
-TK04	P2-7	$\overline{04}$	BLU
-TK05	P2-8	$\overline{05}$	VIO
-TK06	P2-9	$\overline{06}$	BLK
-TK07	P2-10	$\overline{07}$	WHT
-ADTRAK	P2-11	$\overline{AT}$	GRN
-WD	P2-12	$\overline{WD}$	BLK
WD	P2-13	WD	WHT
-WRITE	P2-14	$\overline{WR}$	YEL/WHT
-AREAD	P2-15	$\overline{AR}$	GRN/WHT
GO	P2-16	GO	GRN
GND	P2-17	G2	BLK

Table 5-5. (Cont'd.)

READ/WRITE AMPLIFIER BOARD WIRING (TAPE UNIT)

SIGNAL	FROM	TO	COLOR
GND	P9-1	G	BLK
+20V DC	P9-2	+20V	RED
+5V DC	P9-3	+5V	BLU
-20V DC	P9-4	-20V	YEL
SW	TB2-1	PC1-SW	GRN
"	TB2-2	PC1-SW	RED
GO	TB2-3	PC1-GO	GRN
+5V DC	TB2-4	PC1- +5	BLU

SIGNAL CROSS REFERENCE

	INPUTS		OUTPUTS		
SIGNAL	FROM	TO	SIGNAL	FROM	TO
BUSY	B5-6/2-D1	L10-5/1-A1	B1	A1-8/1-A1	J4-1/6-D2
-BUSY	A5-6/2-D2	D5-9/1-C2	B2	B1-6/1-B1	J4-2/6-D2
-CLEAR	P00-31	A2-12/1-C3	B4	B1-8/1-B1	J5-1/6-D5
-EIGHT	P00-9	A2-1/1-C1	B8	A2-3/1-C1	J5-2/6-D5
-FIVE	P00-6	A1-3/1-A1	CLEAR	A2-11/1-C3	A3-10/2-B4
		B1-10/1-B1	-CLKDBL	L1-6/1-D6	D3-5/5-C4
-FOUR	P00-5	B1-9/1-B1			J3-13/5-C4
-NINE	P00-30	A1-5/1-A1	CLKQUD	M7-9/1-C6	M9-1/9-A3
		A2-2/1-C1	-CLOCK	L1-12/1-D6	J3-2/5-C4
-ONE	P00-2	A1-1/1-A1			M8-11/9-D4
-R/CRET	A5-8/2-C6	K1-14/1-B7	FSTLD	K1-12/1-B7	R00-21
RDCNT	F4-12/3-B2	K1-1/1-B7	GO	D5-8/1-C2	S00-33
-SEVEN	P00-8	A1-4/1-A1	-KB/CLR	B2-10/1-B4	A4-1/2-A1
		B1-5/1-B1			P6-5/2-A5
		B1-13/1-B1	KBSTR	A3-12/1-B3	A3-3/2-C1
-SIX	P00-7	B1-4/1-B1			
		B1-12/1-B1			
-TERMB	S7-6/2-E6	K1-2/1-B7			
-THREE	P00-4	A1-2/1-A1			
		B1-2/1-B1			
-TWO	P00-3	B1-1/1-B1			
-ZERO	P00-1	A3-1/1-B3			

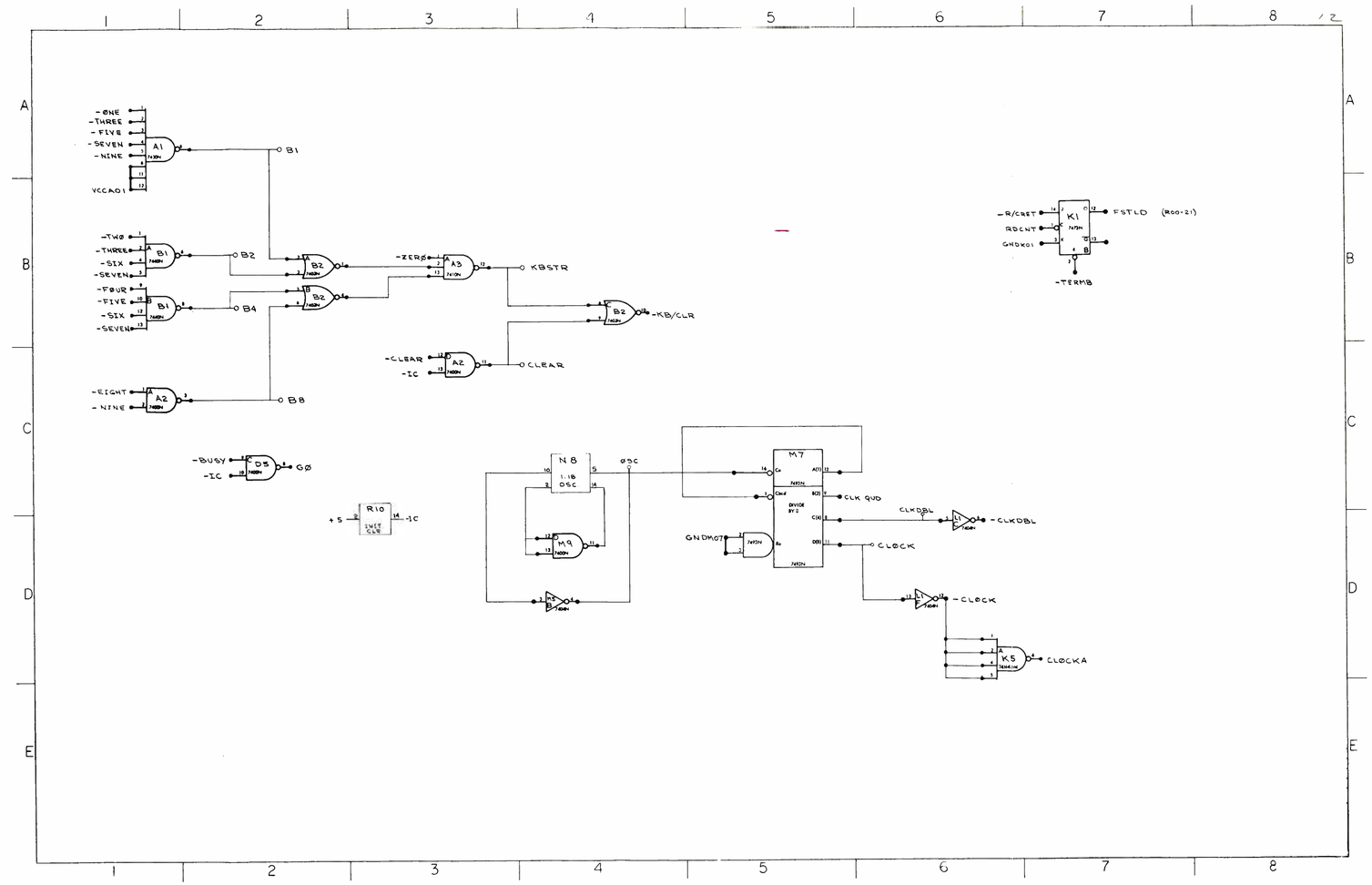


Figure 5-1. Titlefile Logic Diagram (sheet 1 of 9). Keyboard Control and Clock.

SIGNAL CROSS REFERENCE

	INPUTS			OUTPUTS	
SIGNAL	FROM	TO	SIGNAL	FROM	TO
-ADDRFF	H2-8/3-C3	B5-12/2-E1	BUSY	B5-6/2-D1	D5-12/6-B1, L10-5/1-A1
ALSCMP	P5-10/9-D5	A7-5/2-C6			L10-8/6-E1
ARSRD	F8-10/6-B4	E2-9/2-B6	-BUSY	A5-6/2-D2	D5-9/1-C2
-ARSRD	D8-4/6-C5	E2-4/2-C6	-CADR	K10-13/2-A2	L10-9/6-D1
CLEAR	A2-11/1-C3	A3-10/2-B4	-CLCHOP	K4-8/2-A5	K2-2/6-E4
CLOCKA	K5-6/1-D1	A3-9/2-B4	CRET	B4-10/2-C4	K4-13/7-C6
		P5-15/2-D4	CRWOUT	J2-4/2-C4	P00-16
-CRAWL	P00-35	B4-8/2-C4	-ERASEA	A2-8/2-B4	B9-4/5-A4, B10-2/5-A2
		J2-3/2-C4			B10-12/5-A1, D6-2/5-D3
DEC07	J8-4/7-B7	A7-4/2-D6			E10-1/5-A6, E10-3/5-A7
		F2-3/2-A8	GENCLR	B3-2/2-D3	N2-2/9-C8
		F2-10/2-B8	-GENCLR	A2-2/2-D4	B10-9/5-C1
		H2-3/2-B8	NORMRT	B4-13/2-D6	A8-1/5-C2, K2-10/7-D6
DEC15	J8-6/7-C7	F2-7/2-B8			M8-8/8-E2
		F2-14/2-A8	PRCOMP	F2-12/2-A8	J6-3/7-A2
-ECSTR	J7-3/7-A3	E2-2/2-A6	-PRCOMP	F2-13/2-A8	D9-2/6-C1, J1-12/7-A1
-ERASE	P00-36	A4-5/2-A1	R/CRET	B5-8/2-C5	M9-10/8-B7
		B3-9/2-B3	-R/CRET	A5-8/2-C6	E6-8/3-D5, K1-14/1-B7
-KB/CLR	B2-10/1-B4	A4-1/2-A1			M6-2/9-D5
		P6-5/2-A5	RETM	F1-9/2-C2	F4-14/3-B2, H5-2/7-E4
KBSTR	A3-12/1-B3	A3-3/2-C1			H5-14/7-E4
ONRSTD	H9-11/4-B5	S6-12/2-B6	-RETM	F1-8/2-C2	L4-13/8-C6
-PCSTR	J3-6/7-A3	E2-1/2-A6	ROLOUT	J2-2/2-B4	P00-15
-PROEND	E7-6/3-D6	B5-2/2-E5	SCOMPR	H2-12/2-D8	F3-1/3-A2, F4-1/3-B2
		K10-2/2-A2			F5-1/7-E4, K3-13/7-C7
-RCENSR	F7-8/5-E5	H1-14/2-D3			N3-8/8-C7
-READBK	P00-33	A4-4/2-A1	-SCOMPR	H2-13/2-D8	H10-10/5-C1, J1-13/7-A1
		B4-2/2-C1			J9-5/7-C7
READ1	H4-12/4-C3	E1-3/2-E3	STORM	F1-12/2-B2	F3-14/3-A2, K6-1/7-D6
		E2-5/2-C6			M8-9/8-E2
-READ1	H4-13/4-C3	E2-10/2-B6	-STORM	F1-13/2-B2	K3-5/7-D7
-RECORD	P00-32	A4-2/2-A1	-STRLD	A3-6/2-C1	K2-1/6-D3
		B2-11/2-B1	TERM	B5-3/2-E5	E1-12/3-B6, E6-12/3-C5
-ROLL	P00-34	B4-5/2-B4			S6-9/9-B8
		J2-1/2-B4	-TERM	A5-4/2-D6	F5-2/5-D5
SPKDLA	K5-8/4-C7	H1-5/2-E4	-TERMA	S7-4/2-E6	K1-6/9-D8, L3-2/9-D7
		H2-1/2-C8			L3-6/9-D7
			-TERMB	S7-6/2-E6	F7-6/5-E5, H2-6/3-C3
					H4-2/4-C3, K1-2/1-B7
					K7-12/7-B5, M2-13/9-E5
					S9-3/8-B3
			-ZSEEN	H1-8/2-E4	J6-2/7-A2

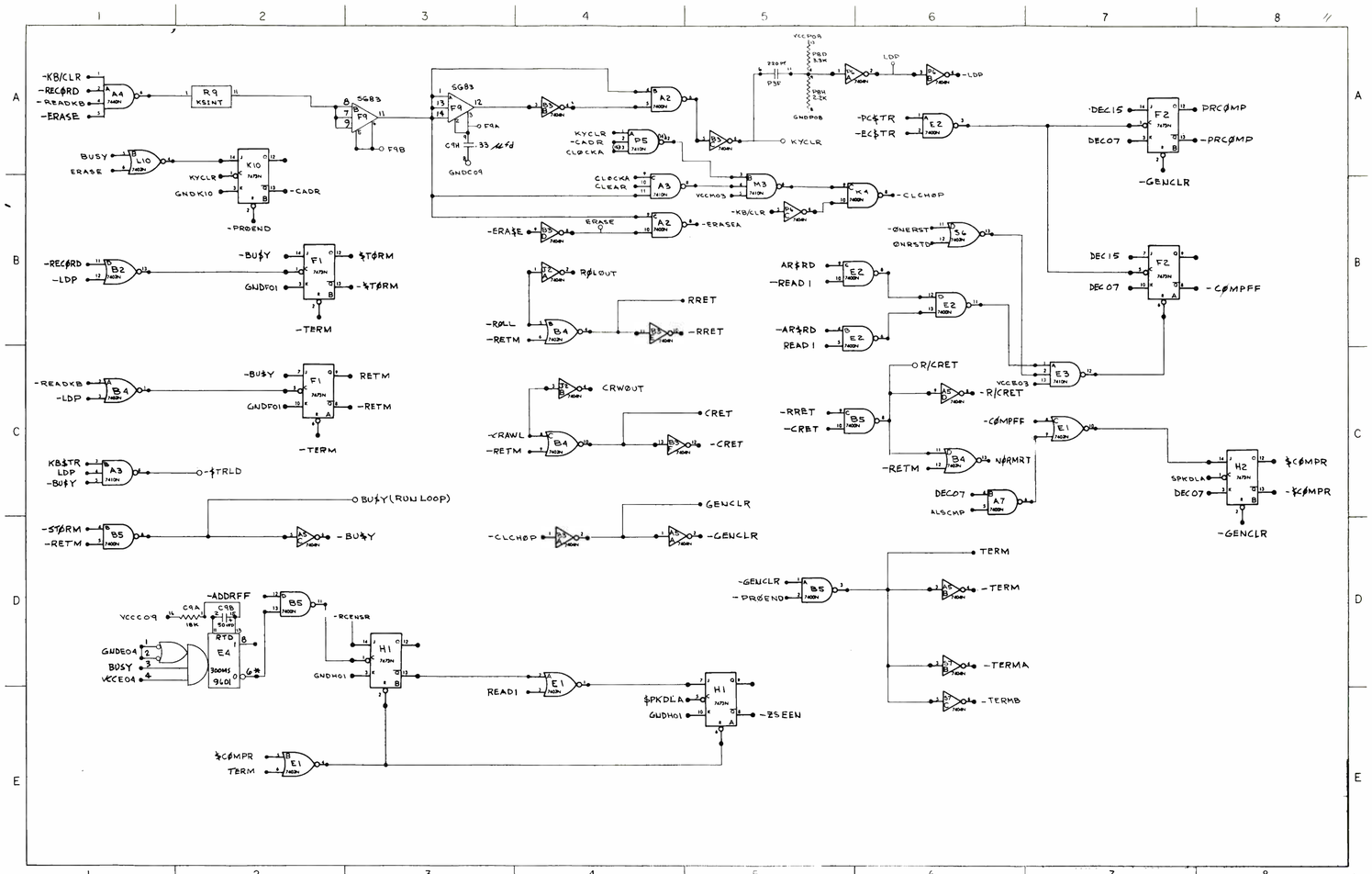


Figure 5-1. Titlefile Logic Diagram (sheet 2 of 9). Keyboard Control.

SIGNAL CROSS REFERENCE

	INPUTS			OUTPUTS	
SIGNAL	FROM	TO	SIGNAL	FROM	TO
CLOCKA	K5-6/1-D1	E3-11/3-A6	ADDRFF	H2-9/3-C3	F5-6/6-C4
		F3-5/3-A5			L7-5/9-E5
		J7-5/3-A5			N7-14/8-D3
-DEC01	C7-2/7-A7	B7-1/3-E3	-ADDRFF	H2-8/3-C3	B5-12/2-E1
-DEC06	C7-7/7-A7	B7-13/3-E3			J9-13/7-B4
DEC07	J8-4/7-B7	F4-5/3-B3			K3-11/7-B2
		H2-10/3-C3	ENDPGE	M5-10/3-C7	H6-3/8-B7
DEC15	J8-6/7-C7	H3-1/3-A4	ENDTRG	E5-8/3-C2	J7-2/7-B4
-DEC2345	J8-12/7-C5	B7-2/3-E3	-INACLK	A7-3/3-E5	D10-5/6-C3
-R/CRET	A5-8/2-C6	E6-8/3-D5			K2-13/6-D3
RECMRK	F5-12/5-D5	E6-3/3-D5	INCADR	A8-4/3-E5	J4-5/6-D2
-RECMRK	F5-13/5-D5	A6-4/3-D5			J4-10/6-D2
RETM	F1-9/2-C2	F4-14/3-B2			J5-5/6-D5
SCOMPR	H2-12/2-D8	F3-1/3-A2			J5-10/6-D5
		F4-1/3-B2	-INCADR	B7-6/3-E4	D5-13/6-B1
SPKDLA	K5-8/4-C7	A7-2/3-E5			D9-8/6-A2
		E3-5/3-B4	-PROEND	E7-6/3-D6	B5-2/2-E5
		H2-5/3-C3			K10-2/2-A2
STORM	F1-12/2-B2	F3-14/3-A2	RDCNT	F4-12/3-B2	K1-1/1-B7
TERM	B5-3/2-E5	E1-12/3-B6			M3-10/4-B1
		E6-12/3-C5			M6-1/9-D5
-TERMB	S7-6/2-E6	H2-6/3-C3			N3-9/8-B6
			-RDCNT	F4-13/3-B2	K3-9/7-B2
					K4-5/8-B7
			READ	F4-9/3-B3	A10-2/5-B1
					D9-5/6-C7
					E10-9/5-D1
					H6-2/8-B7
					J6-11/8-A2
			-READ	F4-8/3-B3	K3-10/7-C2
			WRITE	H3-12/3-A4	A10-12/5-C1
					D3-1/5-C4
					J3-1/5-C4
					J6-12/8-A2
					S9-11/5-E3
			-WRITE	H3-13/3-A4	L4-12/8-C6
					S00-34
			WRTCNT	F3-9/3-A3	J7-4/7-B3
			WRTENA	F3-12/3-A2	D9-6/6-C7
					H4-6/5-C5
					S4-1/5-C5

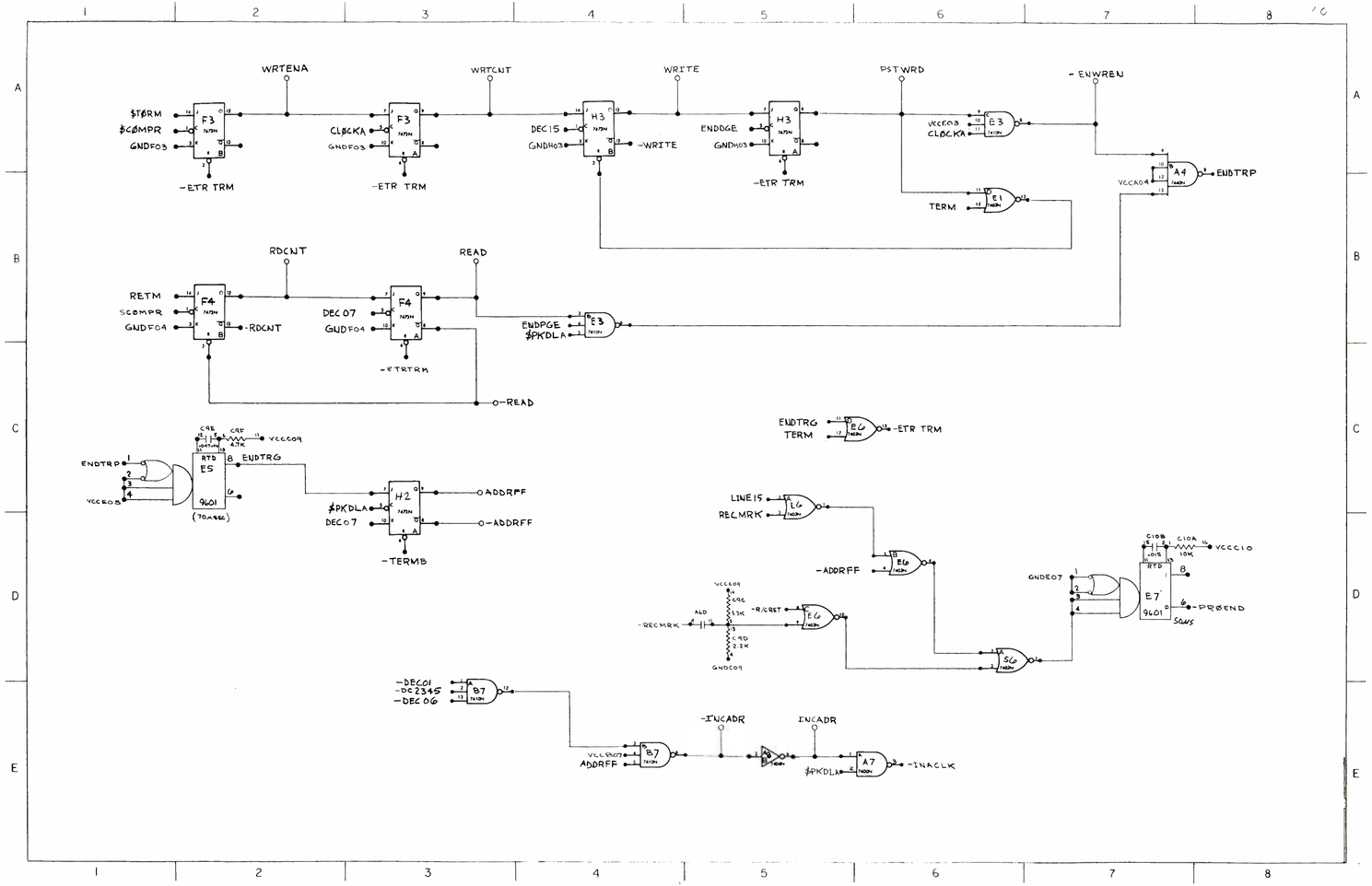


Figure 5-1. Titlefile Logic Diagram (sheet 3 of 9). Write Control and Read Control.

SIGNAL CROSS REFERENCE

INPUTS			OUTPUTS		
SIGNAL	FROM	TO	SIGNAL	FROM	TO
DEC07	J8-4/7-B7	M3-9/4-B1	AREAD	S8-8/4-B2	S00-35
RDCNT	F4-12/3-B2	M3-10/4-B1	ONERST	E9-8/4-B4	H6-5/9-C1
-READAT	S00-1	S4-12/4-A1	-ONERST	E9-6/4-B4	L10-3/9-C2
		S4-13/4-A1			S6-11/9-B6
-TERMB	S7-6/2-E6	H4-2/4-C3	ONRSTD	H9-11/4-B5	S6-12/2-B6
			READ1	H4-12/4-C3	A10-1/5-B1
					E1-3/2-E3
					E2-5/2-C6
					J3-3/7-A3
					L7-13/9-A1
			-READ1	H4-13/4-C3	E2-10/2-B6
					J3-10/7-B4
			-SPKDL	A8-10/4-B7	D9-3/6-C1
			SPKDLA	K5-8/4-C7	A7-2/3-E5
					D3-13/5-D2
					E3-5/3-B4
					E10-11/5-D1
					H1-5/2-E4
					H2-1/2-C8
					H2-5/3-C3
					J3-4/7-A3
					J3-11/7-B4
					J7-1/7-A3
					J7-9/7-B3
					J9-1/7-B4

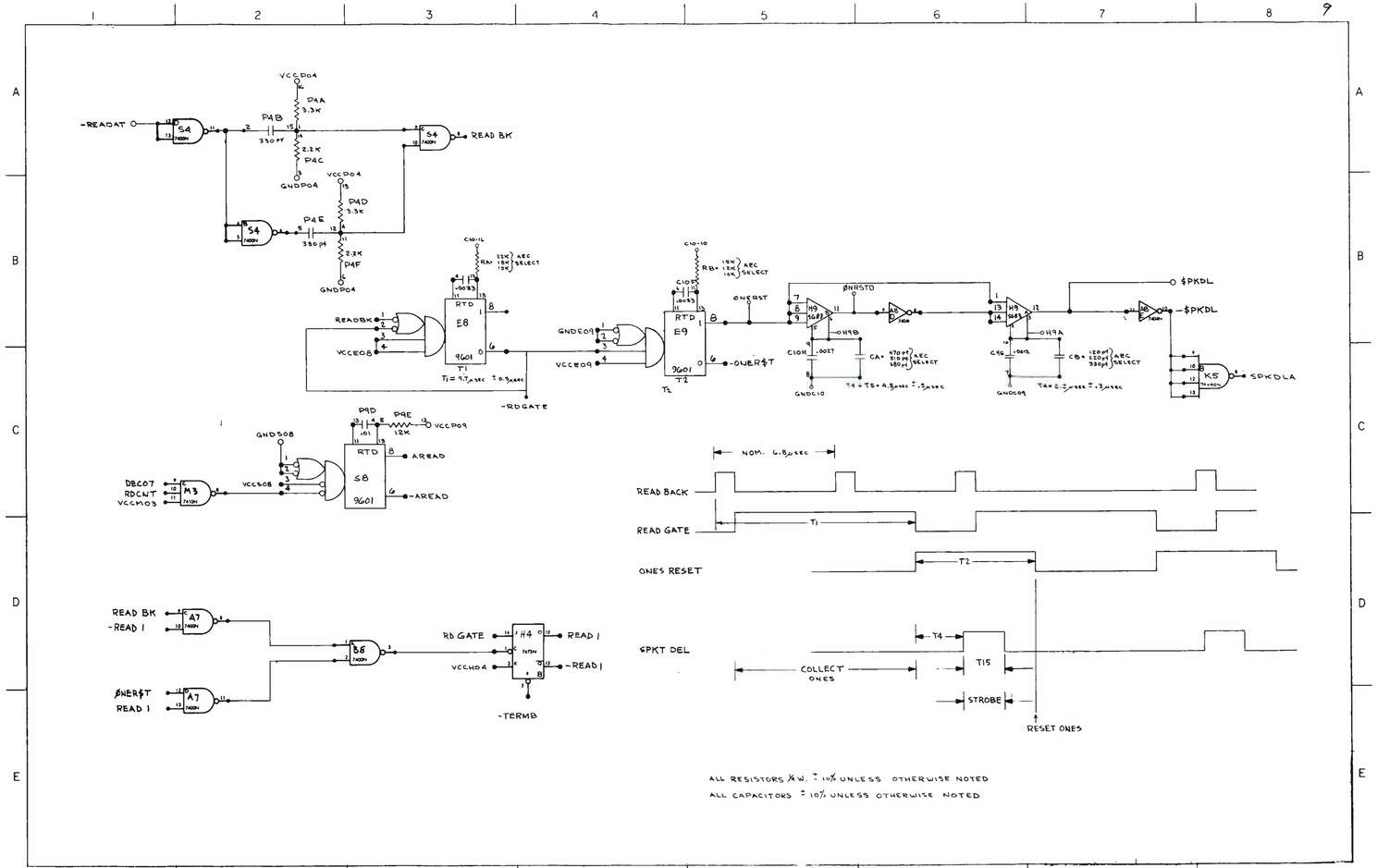


Figure 5-1. Titlefile Logic Diagram (sheet 4 of 9). Read Control.

SIGNAL CROSS REFERENCE

SIGNAL	INPUTS FROM	INPUTS TO	SIGNAL	OUTPUTS FROM	OUTPUTS TO
-AFP	H5-13/7-D8	D1-1/5-C1, D3-10/5-D2	BOUT1	B10-6/5-A2	R00-6
BIN1	P00-18	B8-4/5-A2	BOUT2	B7-8/5-A3	R00-7
BIN2	P00-19	B8-9/5-A3	BOUT3	B9-6/5-A4	R00-8
BIN3	P00-20	B8-12/5-A3	BOUT4	A8-12/5-A4	R00-9
BIN4	P00-21	A9-1/5-A4	BOUT5	B9-8/5-A5	R00-10
BIN5	P00-22	A9-4/5-A5	BOUT6	E10-12/5-A6	R00-11
BIN6	P00-23	A9-9/5-A5	BOUT7	E10-6/5-A7	R00-12
BIN7	P00-24	A9-12/5-A5	BOUT8	B9-11/5-A7	R00-13
BIN8	P00-25	B9-1/5-A7	DATREQ	D2-6/5-C7	R00-2
BKUNLD	L7-3/9-D5	F7-7/5-E5, L2-12/5-D2	DLOUT	D4-13/5-E5	F7-14/9-D3
-BKUNLD	M2-12/9-E5	F5-14/5-D5			M8-3/9-C4
-CLKDBL	L1-6/1-D6	D3-5/5-C4, J3-13/5-C4	-RCENSR	F7-8/5-E5	H1-14/2-D3
-CLOCK	L1-12/1-D6	J3-2/5-C4			K4-2/9-E4
CLOCKA	K5-6/1-D1	A10-13/5-C1, D3-4/5-C4	RECMRK	F5-12/5-D5	E6-3/3-D5
		N3-6/5-E2, S9-10/5-E3			P00-26
-CURHME	K3-6/7-D7	B7-10/5-A3, B10-4/5-A2	-RECMRK	F5-13/5-D5	A6-4/3-D5
-CURUP	K6-6/7-D7	B7-9/5-A3, B9-9/5-A5	STROUT	A6-2/5-D3	R00-3
		B9-12/5-A7, B10-1/5-A2	WRTDAT	S4-3/5-C5	S00-21
-DEC00	C7-1/7-A7	D4-2/5-C5	-WRTDAT	H4-8/5-C5	S00-2
-DEC07	C7-9/7-A7	D4-6/5-D1			
DRSIN	R00-4	D2-11/5-E1			
-ENLINE	F6-8/8-C4	D5-2/5-C6			
-ERASEA	A2-8/2-B4	B9-4/5-A4, B10-2/5-A2			
		B10-12/5-A1, D6-2/5-D3			
		E10-1/5-A6, E10-3/5-A7			
-GENCLR	A5-2/2-D4	B10-9/5-C1			
LINE15	L1-10/8-D4	D2-13/5-C2			
NORMRT	B4-13/2-D6	A8-1/5-C2			
PREMBL	J2-10/7-C8	D3-9/5-D2			
-PREMBL	K3-12/7-C7	E10-2/5-A6, E10-4/5-A7			
-RCSTR	P6-10/9-C4	D6-4/5-D3			
-RCTSPD	N1-6/9-B8	L5-3/5-D4			
READ	F4-9/3-B3	A10-2/5-B1, E10-9/5-D1			
READ1	H4-12/4-C3	A10-1/5-B1			
-SCOMPR	H2-13/2-D8	H10-10/5-C1			
SPKDLA	K5-8/4-C7	D3-13/5-D2, E10-11/5-D1			
SR	L8-12/9-A8	A10-4/5-B1			
-TERM	A5-4/2-D6	F5-2/5-D5			
-TERMB	S7-6/2-E6	F7-6/5-E5			
-ULOAD1	L8-4/9-B2	D1-12/5-C1			
UNLOAD	H7-9/9-C6	A10-5/5-B1			
WRITE	H3-12/3-A4	A10-12/5-C1, D3-1/5-C4			
		J3-1/5-C4, S9-11/5-E3			
WRTENA	F3-12/3-A2	H4-6/5-C5, S4-1/5-C5			

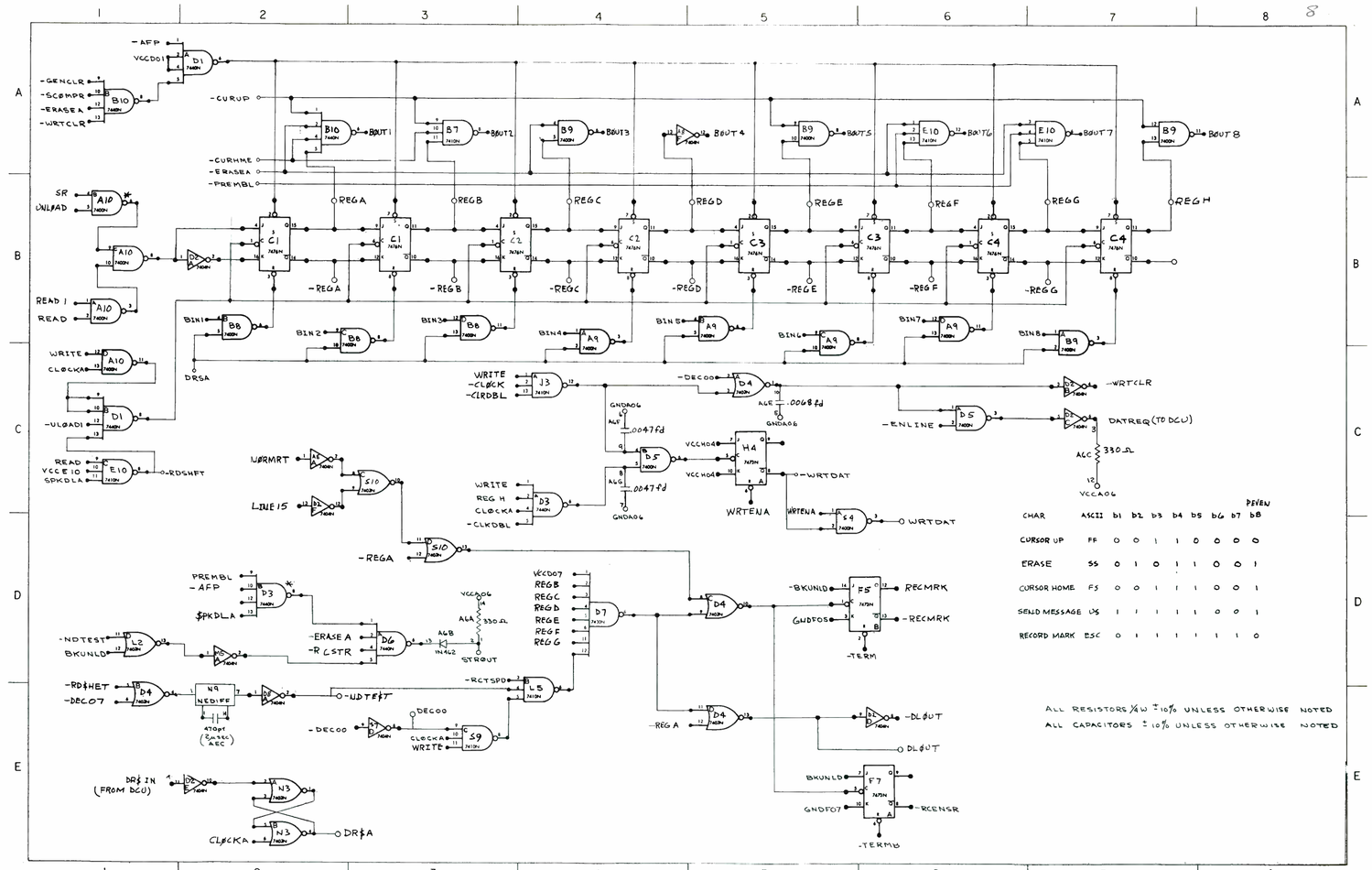


Figure 5-1. Titlefile Logic Diagram (sheet 5 of 9). Input/Output Control.

SIGNAL CROSS REFERENCE

INPUTS			OUTPUTS		
SIGNAL	FROM	TO	SIGNAL	FROM	TO
ADDRFF	H2-9/3-C3	F5-6/6-C4	-ADTRAK	A8-6/6-C7	S00-11
BUSY	B5-6/2-D1	D5-12/6-B1	ARSRD	F8-10/6-B4	E2-9/2-B6
		L10-8/6-E1	-ARSRD	D8-4/6-C5	E2-4/2-C6
B1	A1-8/1-A1	J4-1/6-D2	L1	F10-14/6-D7	P00-10
B2	B1-6/1-B1	J4-2/6-D2	L10	F10-10/6-D7	P00-37
B4	B1-8/1-B1	J5-1/6-D5	L100	H10-13/6-D7	R00-1
B8	A2-3/1-C1	J5-2/6-D5	L2	F10-13/6-D7	P00-11
-CADR	K10-13/2-A2	L10-9/6-D1	L20	F10-9/6-D7	P00-38
-CLCHOP	K4-8/2-A5	K2-2/6-E4	L200	H10-12/6-D7	R00-5
-DEC01	C7-2/7-A7	D9-9/6-C2	L4	F10-12/6-D7	P00-12
		J1-4/6-C2	L40	F10-8/6-D7	P00-39
-DEC03	C7-4/7-A7	D10-9/6-C1	L400	H10-11/6-D7	R00-14
		J1-1/6-A2	L8	F10-11/6-D7	P00-13
		J1-5/6-C2	L80	H10-14/6-D7	P00-40
-DEC05	C7-6/7-A7	J1-2/6-A2	L800	H10-10/6-D7	R00-15
-INACLK	A7-3/3-E5	D10-5/6-C3	-TK00	C5-1/6-B7	S00-3
		K2-13/6-D3	-TK01	C5-2/6-B7	S00-4
INCADR	A8-4/3-E5	J4-5/6-D2	-TK02	C5-3/6-B7	S00-5
		J4-10/6-D2	-TK03	C5-4/6-B7	S00-6
		J5-5/6-D5	-TK04	C5-5/6-B7	S00-7
		J5-10/6-D5	-TK05	C5-6/6-B7	S00-8
-INCADR	B7-6/3-E4	D5-13/6-B1	-TK06	C5-7/6-B7	S00-9
		D9-8/6-A2	-TK07	C5-9/6-B7	S00-10
-PRCOMP	F2-13/2-A8	D9-2/6-C1	-TRAKD0	C8-1/6-A7	P10-1/7-C1
READ	F4-9/3-B3	D9-5/6-C7	-TRAKD1	C8-2/6-A7	P10-2/7-C1
-SPKDL	A8-10/4-B7	D9-3/6-C1	-TRAKD2	C8-3/6-A7	P10-3/7-C1
-STRLD	A3-6/2-C1	K2-1/6-D3	-TRAKD3	C8-4/6-A7	P10-4/7-C1
WRTENA	F3-12/3-A2	D9-6/6-C7	-TRAKD4	C8-5/6-A7	P10-5/7-C1
			-TRAKD5	C8-6/6-A7	P10-6/7-C1
			-TRAKD6	C8-7/6-A7	P10-7/7-C1
			-TRAKD7	C8-9/6-A7	P10-8/7-C1

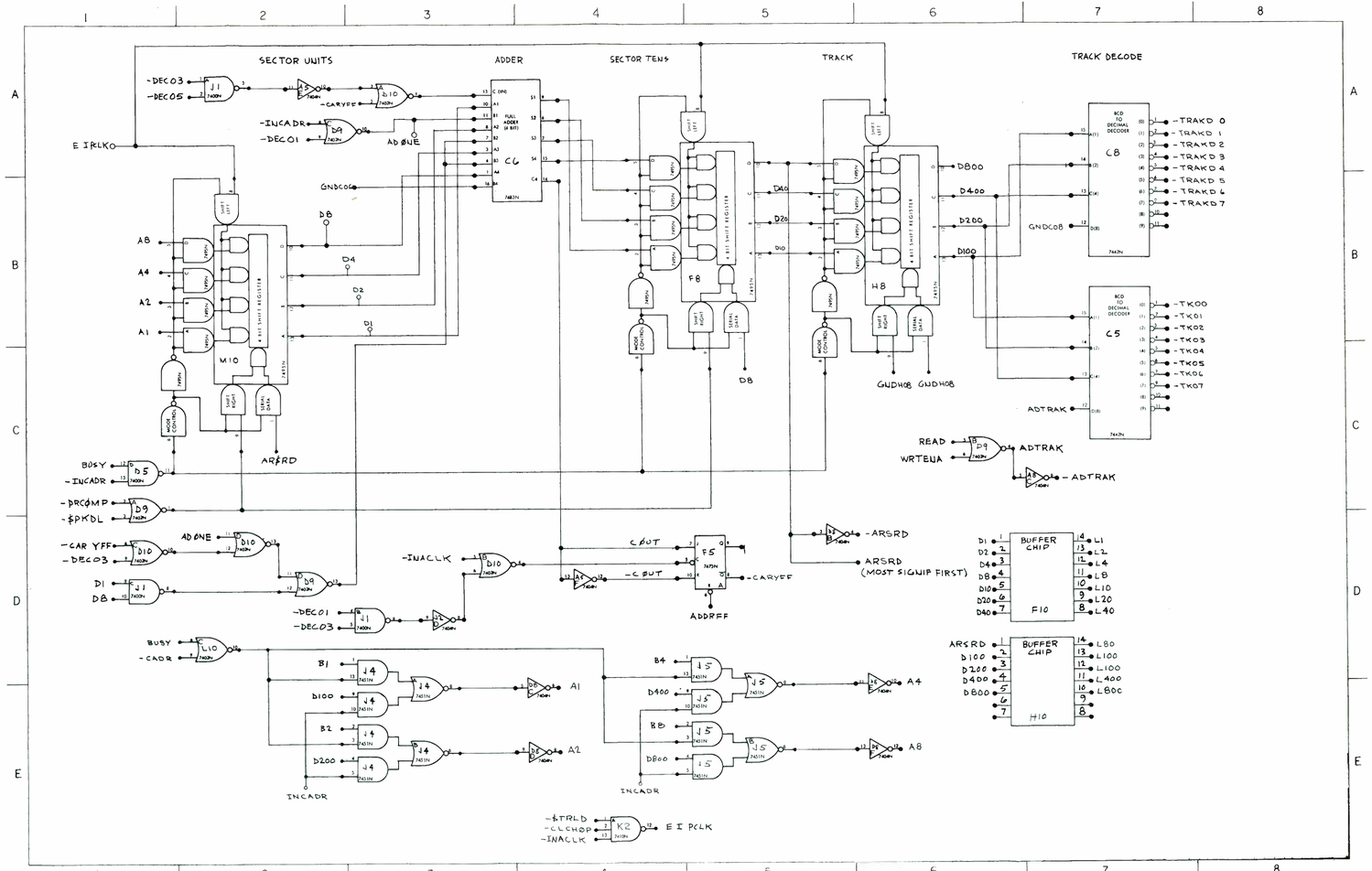


Figure 5-1. Titlefile Logic Diagram (sheet 6 of 9). Address and Track Select Control.

SIGNAL CROSS REFERENCE

	INPUTS			OUTPUTS	
SIGNAL	FROM	TO	SIGNAL	FROM	TO
-ADDRFF	H2-8/3-C3	J9-13/7-B4	-AFP	H5-13/7-D8	D1-1/5-C1
		K3-11/7-B2			D3-10/5-D2
CHA24D	N5-8/8-A5	P1-4/7-E3	CCTSEL	P1-12/7-E3	F6-1/8-B4
CRET	B4-10/2-C4	K4-13/7-C6	-CURHME	K3-6/7-D7	B7-10/5-A3
ENDTRG	E5-8/3-C2	J7-2/7-B4			B10-4/5-A2
LINEC	N7-8/8-D3	P1-3/7-E3	-CURUP	K6-6/7-D7	B7-9/5-A3
NORMRT	B4-13/2-D6	K2-10/7-D6			B9-9/5-A5
PRCOMP	F2-12/2-A8	J6-3/7-A2			B9-12/5-A7
-PRCOMP	F2-13/2-A8	J1-12/7-A1			B10-1/5-A2
-RDCNT	F4-13/3-B2	K3-9/7-B2	-DEC00	C7-1/7-A7	D4-2/5-C5
-READ	F4-8/3-B3	K3-10/7-C2	-DEC01	C7-2/7-A7	B7-1/3-E3
READ1	H4-12/4-C3	J3-3/7-A3			D9-9/6-C2
-READ1	H4-13/4-C3	J3-10/7-B4			J1-4/6-C2
RETM	F1-9/2-C2	H5-2/7-E4	-DEC03	C7-4/7-A7	D10-9/6-C1
		H5-14/7-E4			J1-1/6-A2
SCOMPR	H2-12/2-D8	F5-1/7-E4			J1-5/6-C2
		K3-13/7-C7	-DEC05	C7-6/7-A7	J1-2/6-A2
-SCOMPR	H2-13/2-D8	J1-13/7-A1	-DEC06	C7-7/7-A7	B7-13/3-E3
		J9-5/7-C7	DEC07	J8-4/7-B7	A7-4/2-D6
SPKDLA	K5-8/4-C7	J3-4/7-A3			F2-3/2-A8
		J3-11/7-B4			F2-10/2-B8
		J7-1/7-A3			F4-5/3-B3
		J7-9/7-B3			H2-3/2-B8
		J9-1/7-B4			H2-10/3-C3
STORM	F1-12/2-B2	K6-1/7-D6			L6-5/8-C7
-STORM	F1-13/2-B2	K3-5/7-D7			L6-10/9-D1
-TERMB	S7-6/2-E6	K7-12/7-B5			M3-9/4-B1
-TRAKD0	C8-1/6-A7	P10-1/7-C1	-DEC07	C7-9/7-A7	D4-6/5-D1
-TRAKD1	C8-2/6-A7	P10-2/7-C1			K8-3/8-B2
-TRAKD2	C8-3/6-A7	P10-3/7-C1	DEC15	J8-6/7-C7	F2-7/2-B8
-TRAKD3	C8-4/6-A7	P10-4/7-C1			F2-14/2-A8
-TRAKD4	C8-5/6-A7	P10-5/7-C1			H3-1/3-A4
-TRAKD5	C8-6/6-A7	P10-6/7-C1	-DEC2345	J8-12/7-C5	B7-2/3-E3
-TRAKD6	C8-7/6-A7	P10-7/7-C1	-ECSTR	J7-3/7-A3	E2-2/2-A6
-TRAKD7	C8-9/6-A7	P10-8/7-C1	-PCSTR	J3-6/7-A3	E2-1/2-A6
WRTCNT	F3-9/3-A3	J7-4/7-B3	PGLNCT	P1-14/7-E3	L5-2/8-D3
-ZSEEN	H1-8/2-E4	J6-2/7-A2	PREMBL	J2-10/7-C8	D3-9/5-D2
			-PREMBL	K3-12/7-C7	E10-2/5-A6
					E10-4/5-A7

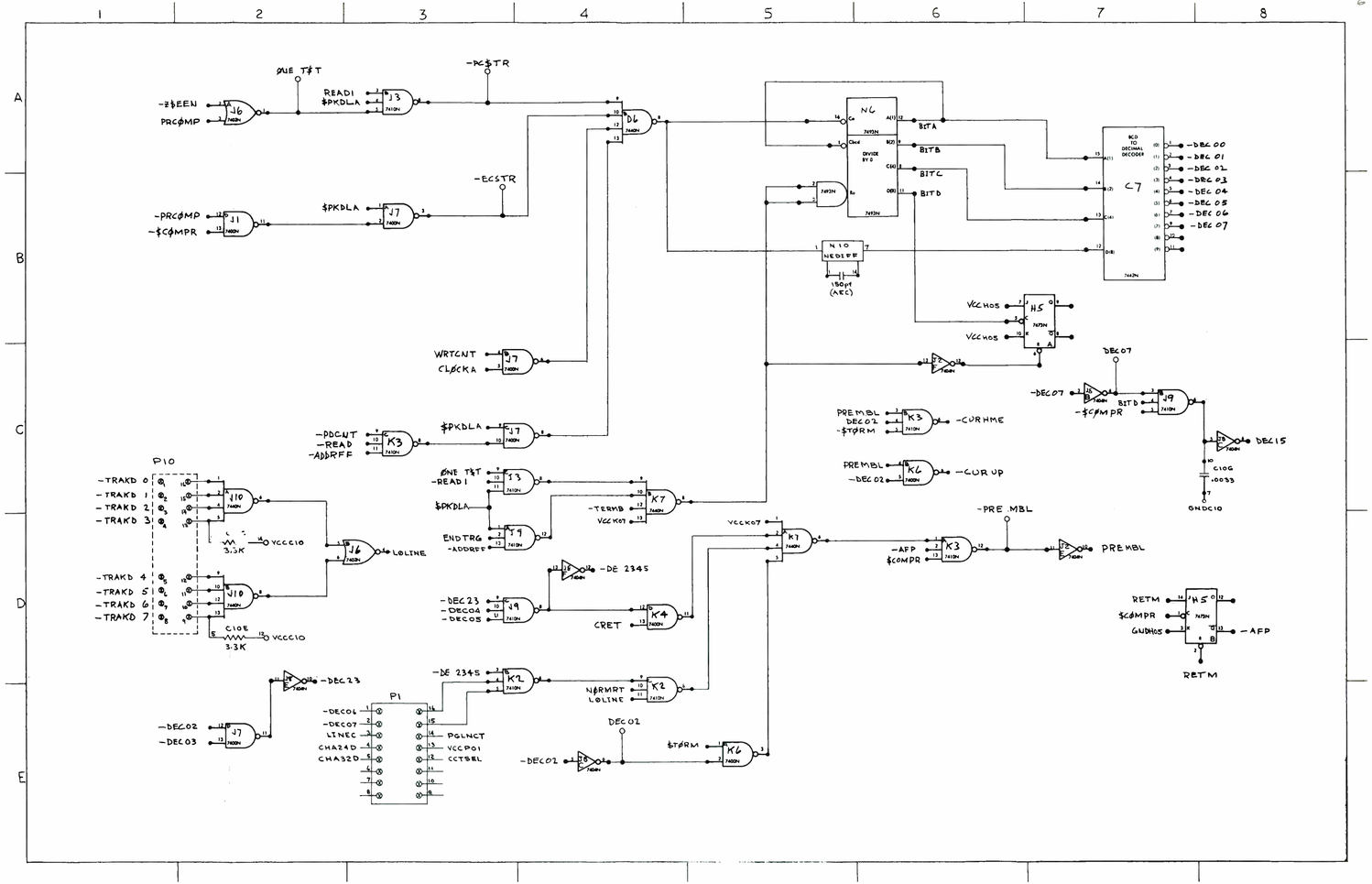


Figure 5-1. Titlefile Logic Diagram (sheet 7 of 9). Bit Count Control.

SIGNAL CROSS REFERENCE

	INPUTS			OUTPUTS	
SIGNAL	FROM	TO	SIGNAL	FROM	TO
ADDRFF	H2-9/3-C3	N7-14/8-D3	CHA24D	N5-8/8-A5	P1-4/7-E3
ALTIN	S9-12/9-B1	M9-9/8-B7	-ENLINE	F6-8/8-C4	D5-2/5-C6
CCTSEL	P1-12/7-E3	F6-1/8-B4	LINEC	N7-8/8-D3	P1-3/7-E3
DEC07	J8-4/7-B7	L6-5/8-C7	LINE15	L1-10/8-D4	D2-13/5-C2
-DEC07	C7-9/7-A7	K8-3/8-B2			E6-2/3-D5
ENDPGE	M5-10/3-C7	H6-3/8-B7	LOAD	H6-12/8-B7	H6-6/9-C1
NORMRT	B4-13/2-D6	M8-8/8-E2			H6-7/9-C1
PGLNCT	P1-14/7-E3	L5-2/8-D3			L3-7/9-B7
R/CRET	B5-8/2-C5	M9-10/8-B7			L5-9/9-A2
RDCNT	F4-12/3-B2	N3-9/8-B6	-LOAD	H6-13/8-B7	B6-5/9-D6
-RDCNT	F4-13/3-B2	K4-5/8-B7			B6-10/9-D6
READ	F4-9/3-B3	H6-2/8-B7			S10-5/9-D8
		J6-11/8-A2	LOADA	J8-2/8-B7	L6-13/9-D1
-RETM	F1-8/2-C2	L4-13/8-C6			L7-12/9-A1
SCOMPR	H2-12/2-D8	N3-8/8-C7			M2-9/9-A3
STORM	F1-12/2-B2	M8-9/8-E2			M3-1/9-A5
-TERMB	S7-6/2-E6	S9-3/8-B3			S10-3/9-D7
WRITE	H3-12/3-A4	J6-12/8-A2			
-WRITE	H3-13/3-A4	L4-12/8-C6			

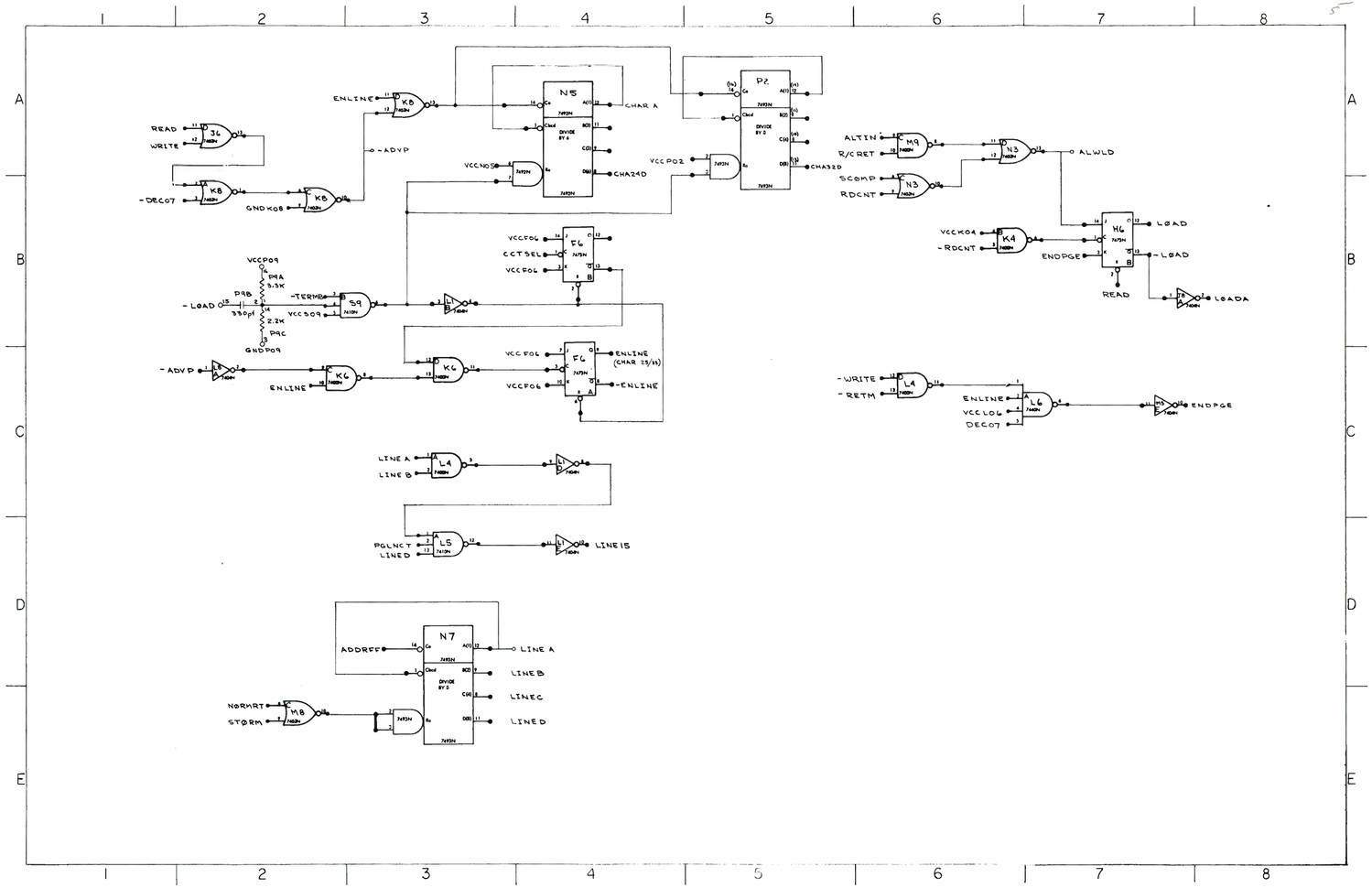


Figure 5-1. Titlefile Logic Diagram (sheet 8 of 9). Character Count Control.

SIGNAL CROSS REFERENCE

INPUTS			OUTPUTS		
SIGNAL	FROM	TO	SIGNAL	FROM	TO
ADDRFF	H2-9/3-C3	L7-5/9-E5	ALSCMP	P5-10/9-D5	A7-5/2-C6
CHAREQ	P00-14	M2-3/9-E2	ALTIN	S9-12/9-B1	M9-9/8-B7
		N4-1/9-E1	BKUNLD	L7-3/9-D5	F7-7/5-E5
		N4-13/9-E1			L2-12/5-D2
		N4-14/9-E1	-BKUNLD	M2-12/9-E5	F5-14/5-D5
CLKQUD	M7-9/1-C6	M9-1/9-A3	-RCSTR	P6-10/9-C4	D6-4/5-D3
-CLOCK	L1-12/1-D6	M8-11/9-D4	-RCTSPD	N1-6/9-B8	L5-3/5-D4
CLOCKA	K5-6/1-D1	S5-7/9-D4	SR	L8-12/9-A8	A10-4/5-B1
		S5-8/9-D4	-UNLOAD1	L8-4/9-B2	D1-12/5-C1
		S5-9/9-D4	UNLOAD	H7-9/9-C6	A10-5/5-B1
DEC07	J8-4/7-B7	L6-10/9-D1			
DLOUT	D4-13/5-E5	F7-14/9-D3			
		M8-3/9-C4			
ENLINE	F6-9/8-C4	L6-9/9-D1			
GENCLR	B3-2/2-D3	N2-2/9-C8			
LOAD	H6-12/8-B7	H6-6/9-C1			
		H6-7/9-C1			
		L3-7/9-B7			
		L5-9/9-A2			
-LOAD	H6-13/8-B7	B6-5/9-D6			
		B6-10/9-D6			
LOADA	J8-2/8-B7	L6-13/9-D1			
		L7-12/9-A1			
		M2-9/9-A3			
		M3-1/9-A5			
		S10-3/9-D7			
ONERST	E9-8/4-B4	H6-5/9-C1			
-ONERST	E9-6/4-B4	L10-3/9-C2			
		S6-11/9-B6			
-R/CRET	A5-8/2-C6	M6-2/9-D5			
-RCENSR	F7-8/5-E5	K4-2/9-E4			
RDCNT	F4-12/3-B2	M6-1/9-D5			
READ1	H4-12/4-C3	L7-13/9-A1			
TERM	B5-3/2-E5	S6-9/9-B8			
-TERMA	S7-4/2-E6	K1-6/9-D8			
		L3-2/9-D7			
		L3-6/9-D7			
-TERMB	S7-6/2-E6	M2-13/9-E5			

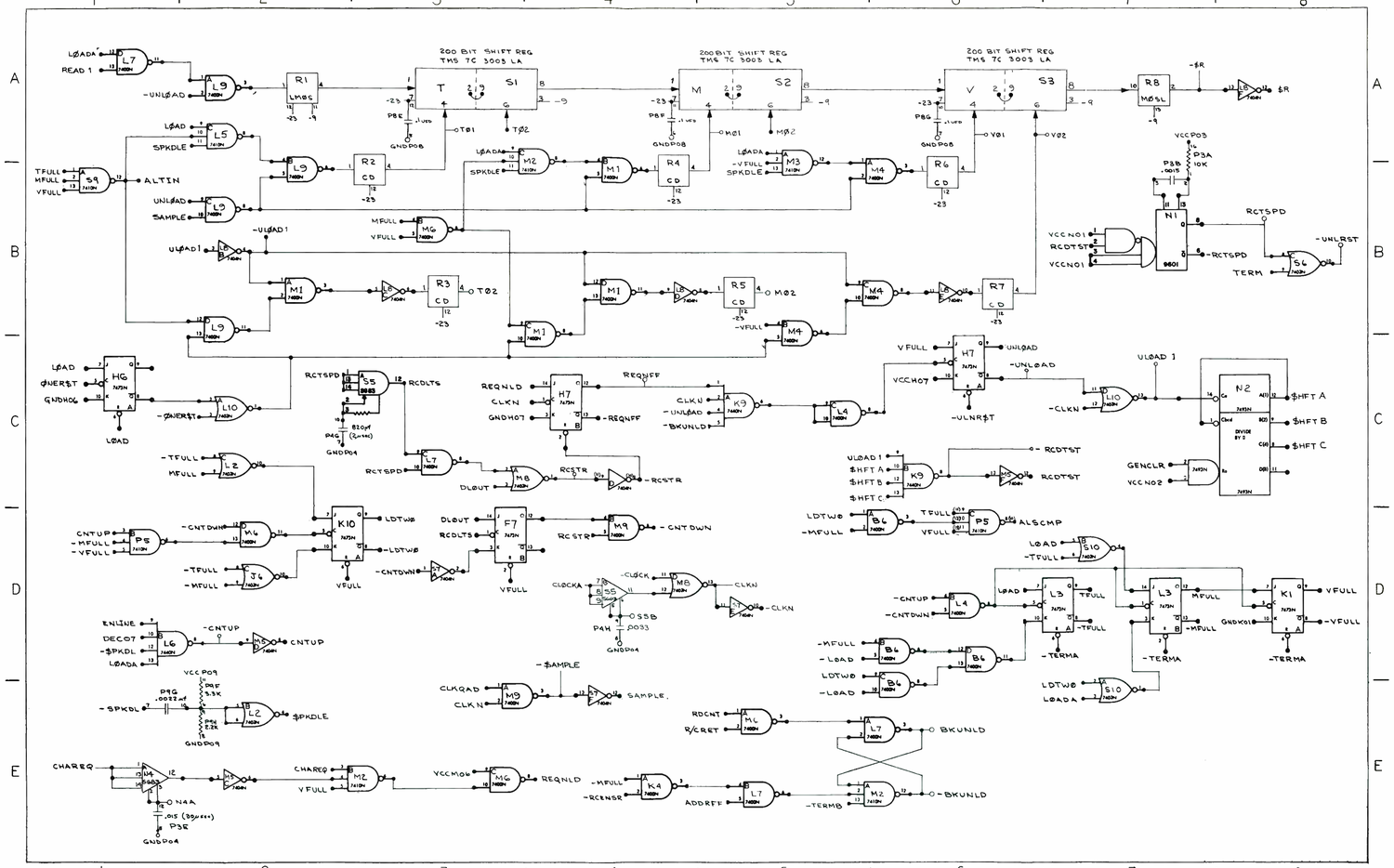


Figure 5-1. Titlefile Logic Diagram (sheet 9 of 9). Roll/Crawl Control.

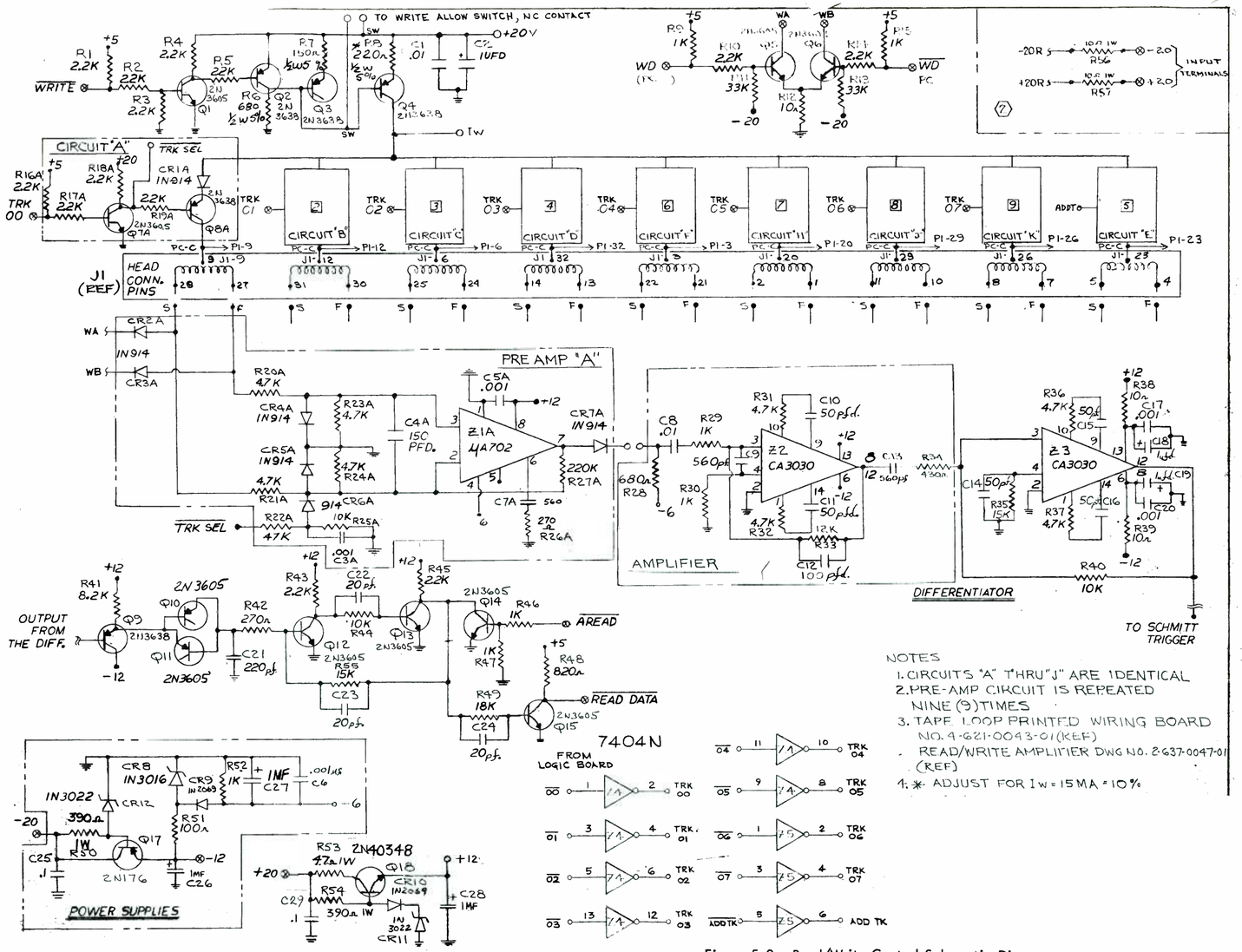
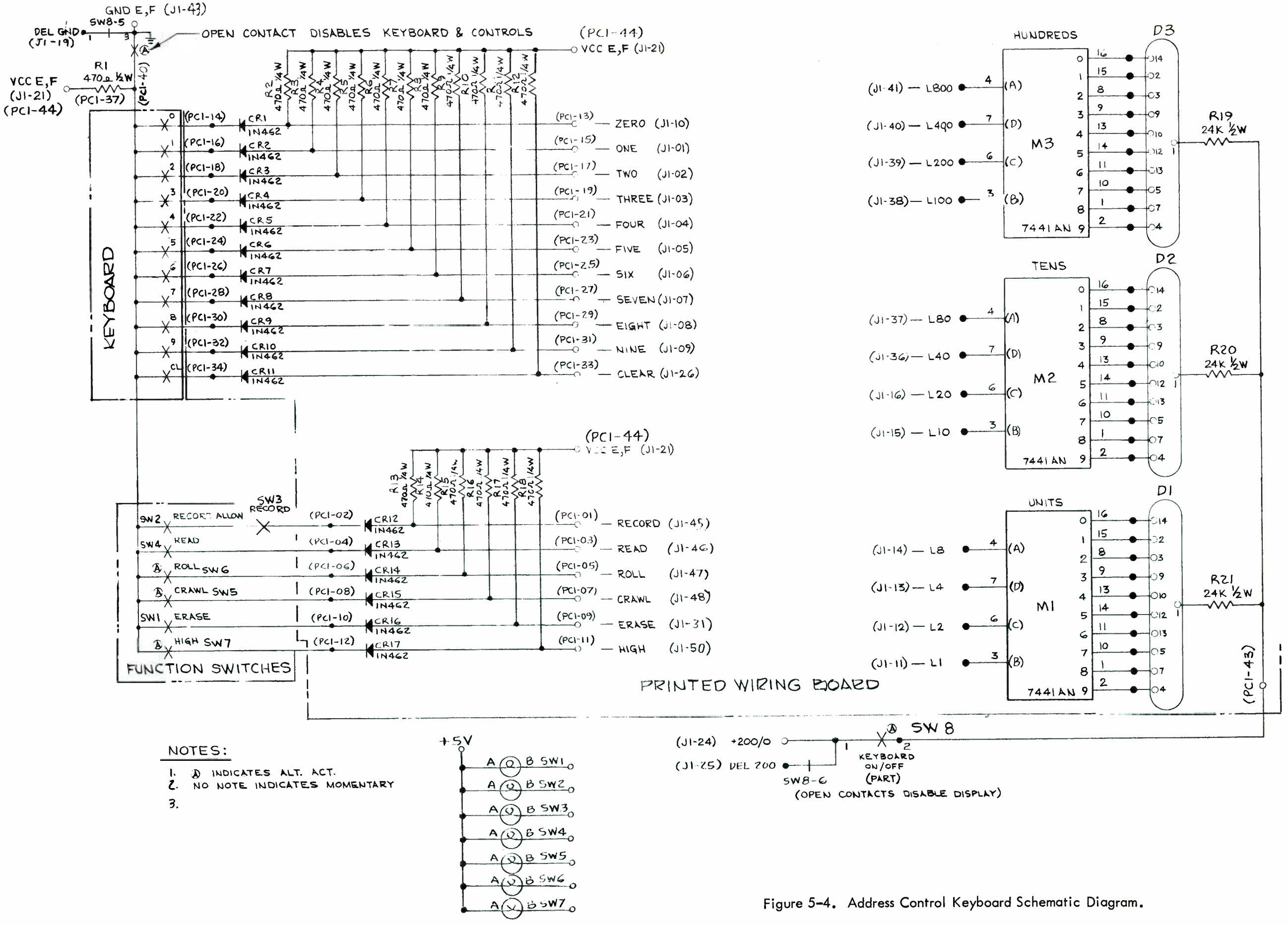


Figure 5-2. Read/Write Control Schematic Diagram.



NOTES:

1. Ⓐ INDICATES ALT. ACT.
2. NO NOTE INDICATES MOMENTARY
3.

Figure 5-4. Address Control Keyboard Schematic Diagram.

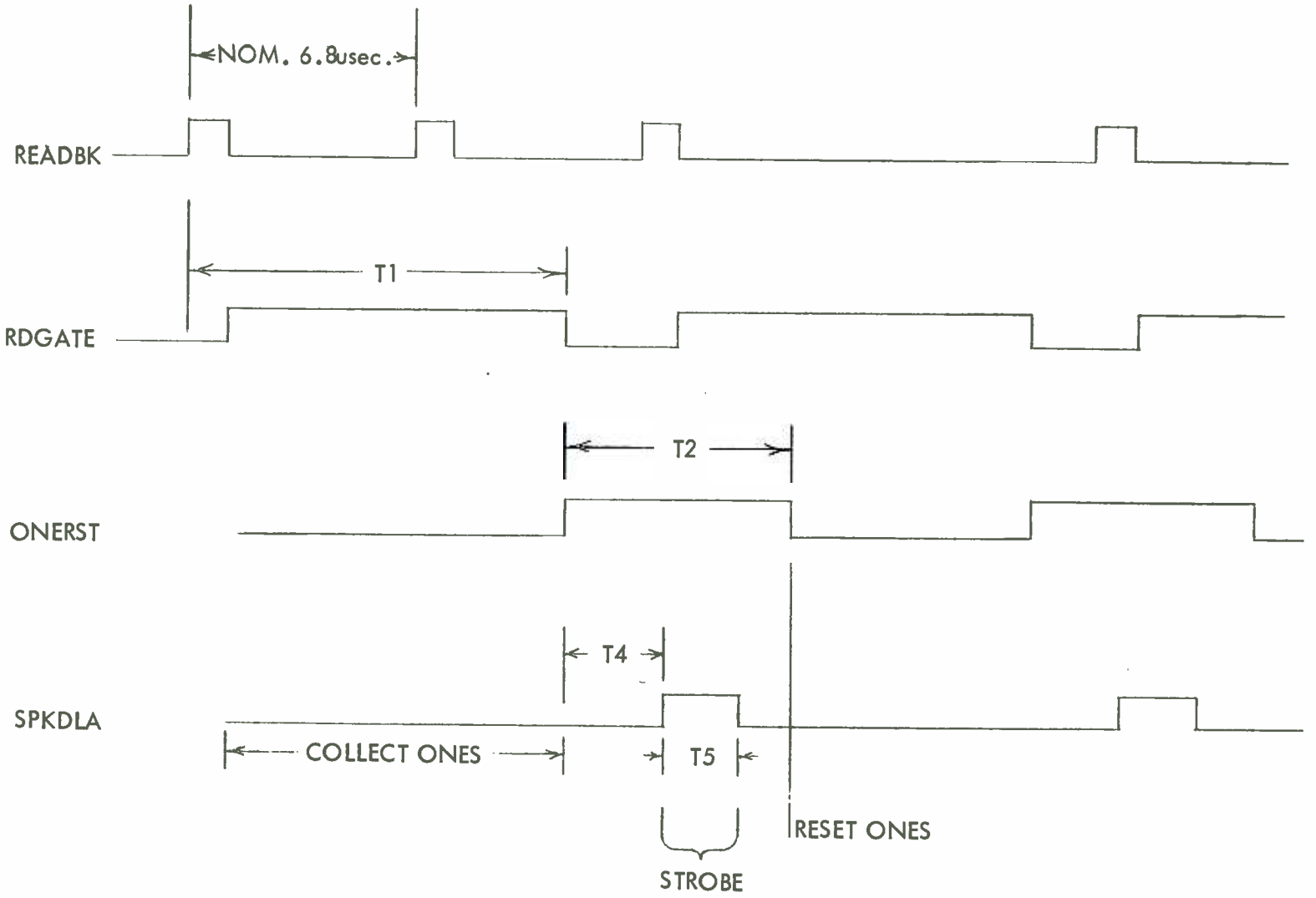


Figure 5-3. Timing Diagram.

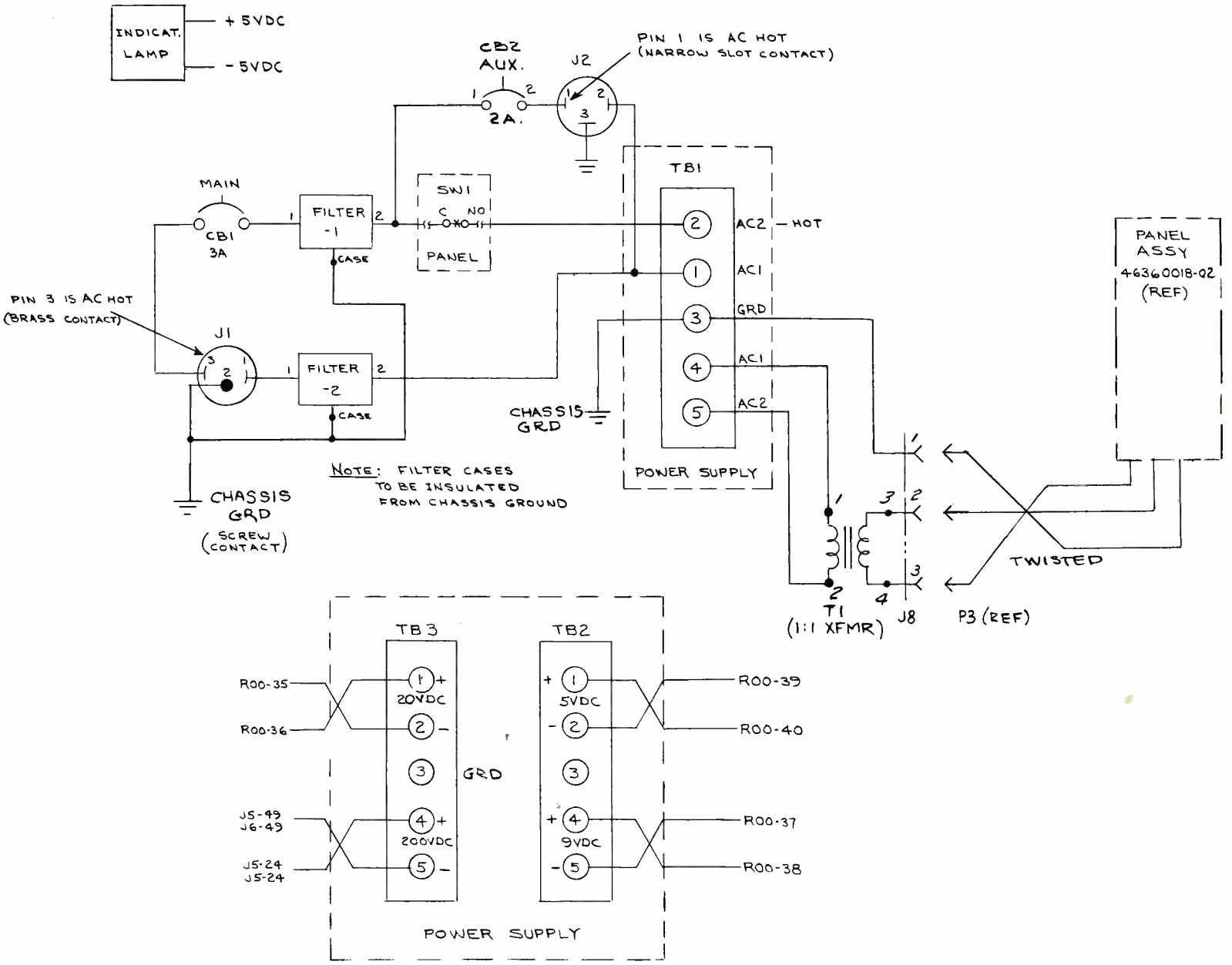


Figure 5-5. Logic Controller Power Distribution Wiring Diagram.

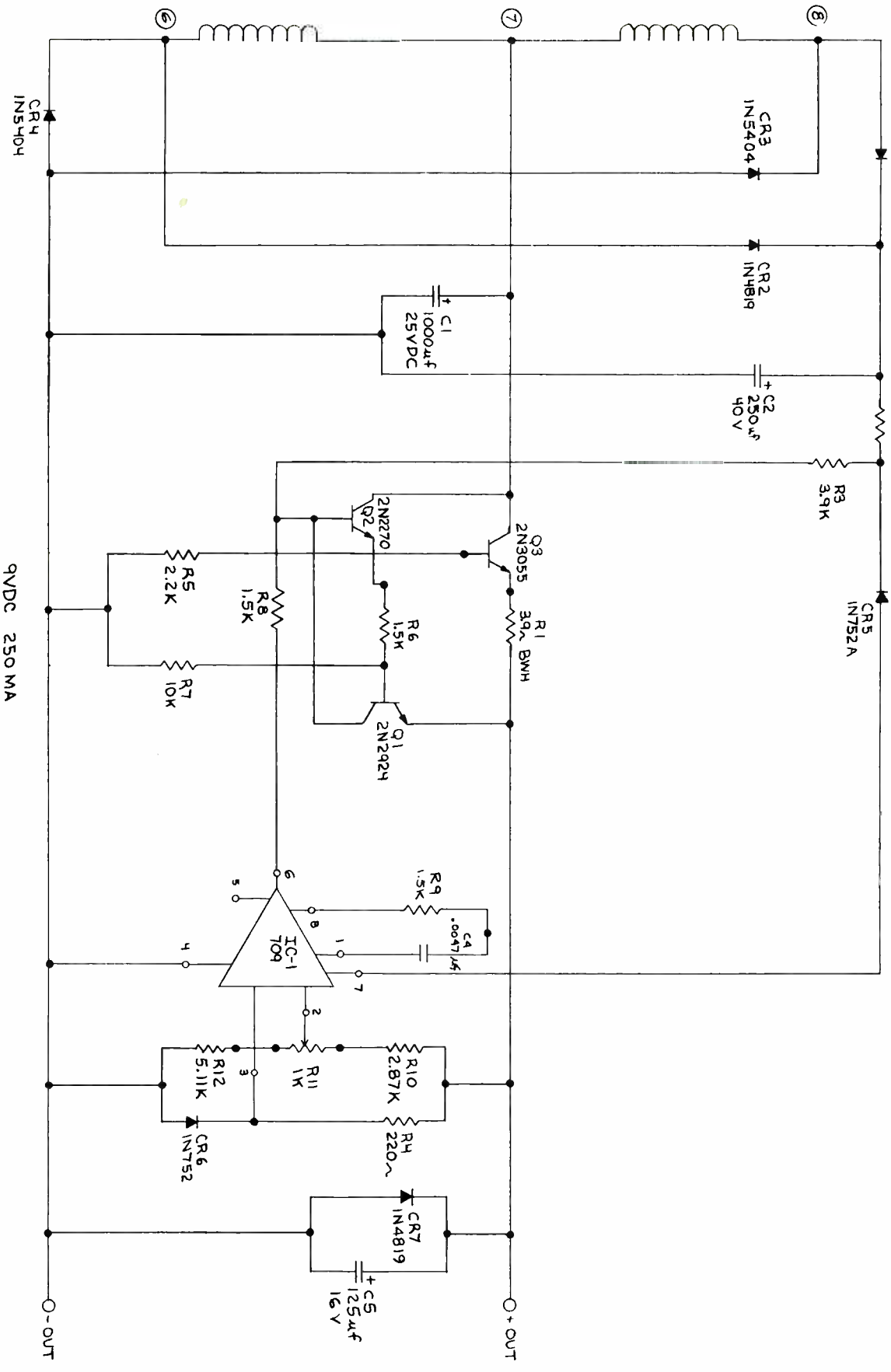


Figure 5-6. Power Supply Schematic Diagram (sheet 1 of 5).

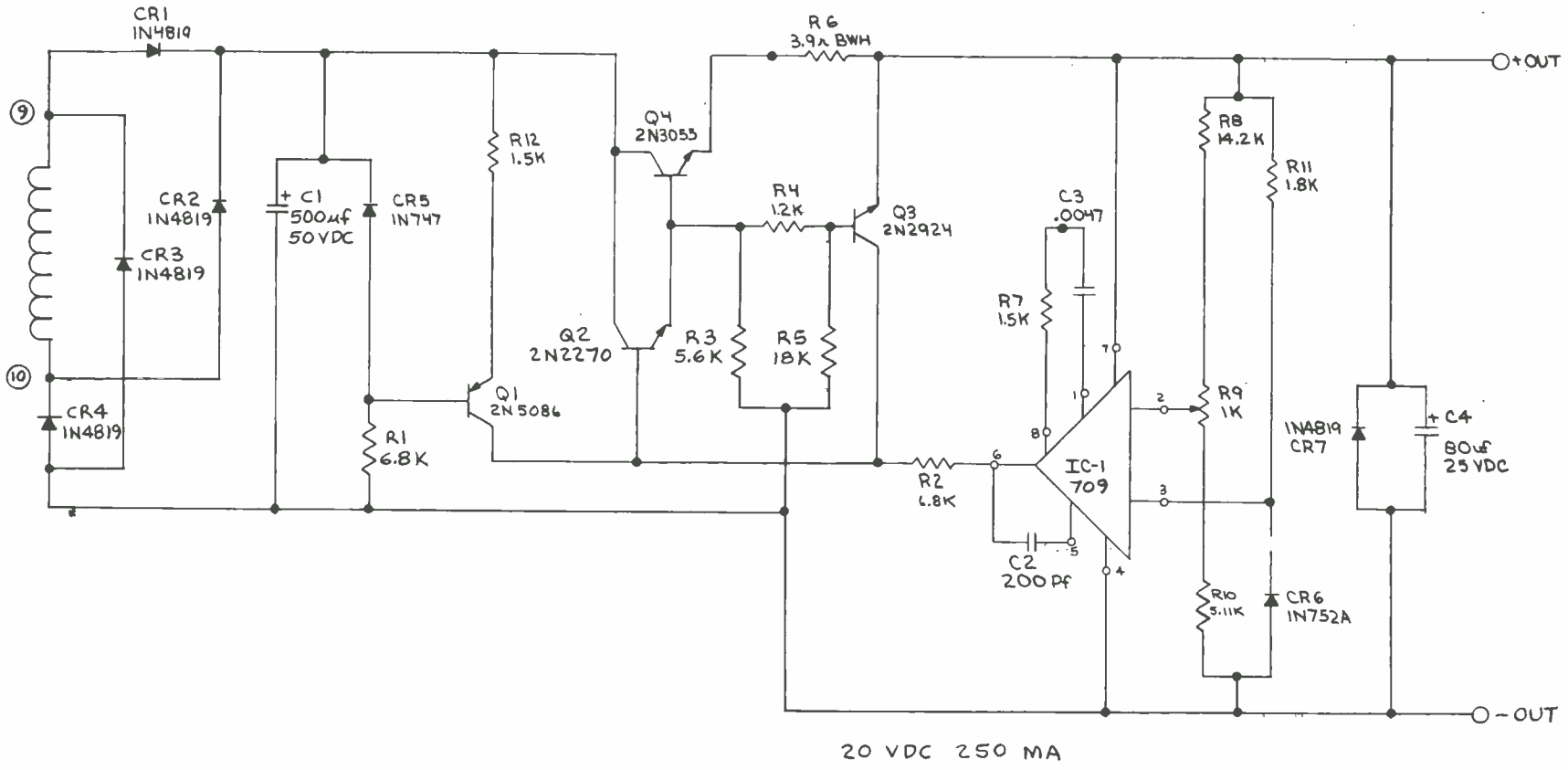


Figure 5-6. Power Supply Schematic Diagram (sheet 2 of 5).

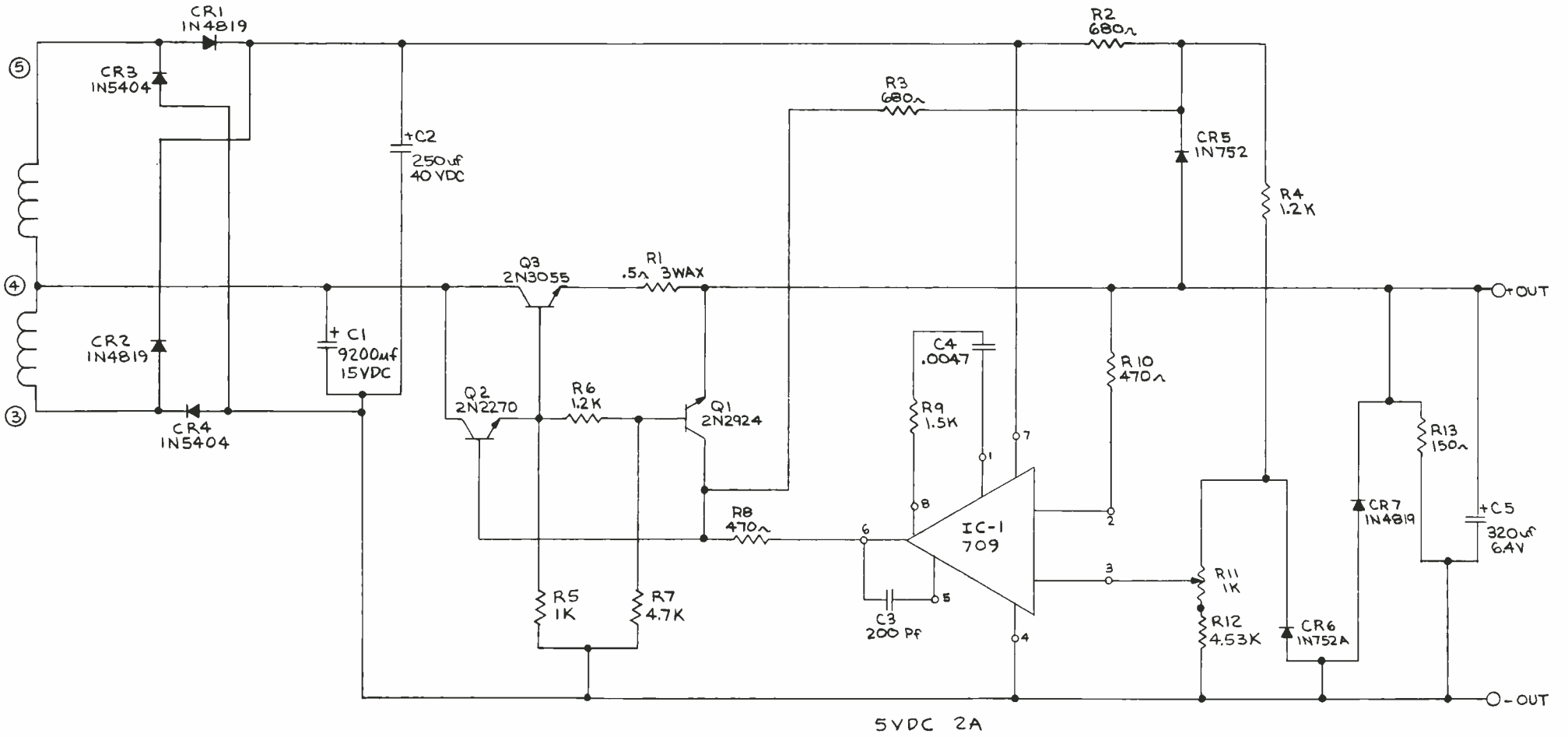


Figure 5-6. Power Supply Schematic Diagram (sheet 3 of 5).

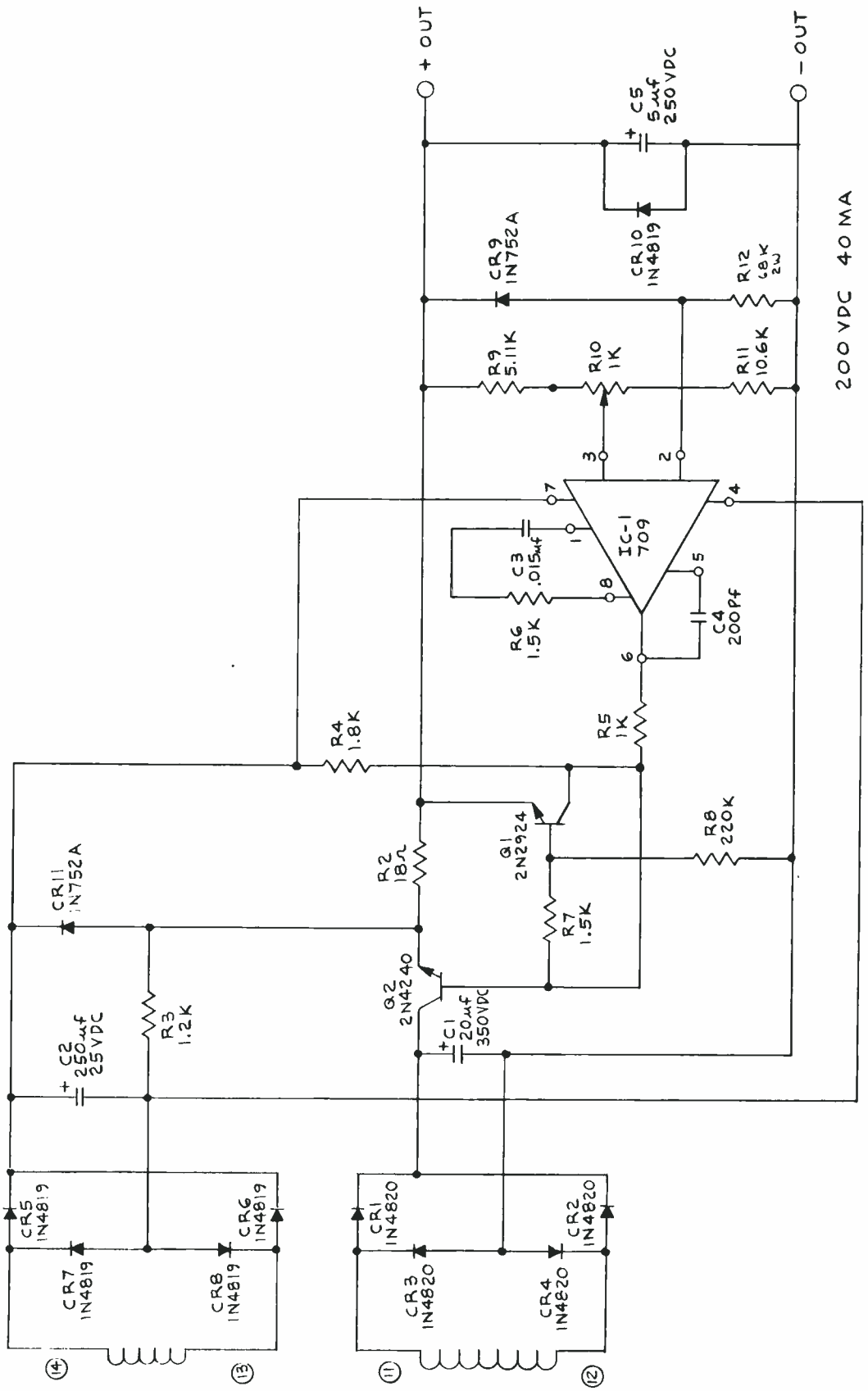


Figure 5-6. Power Supply Schematic Diagram (sheet 4 of 5).

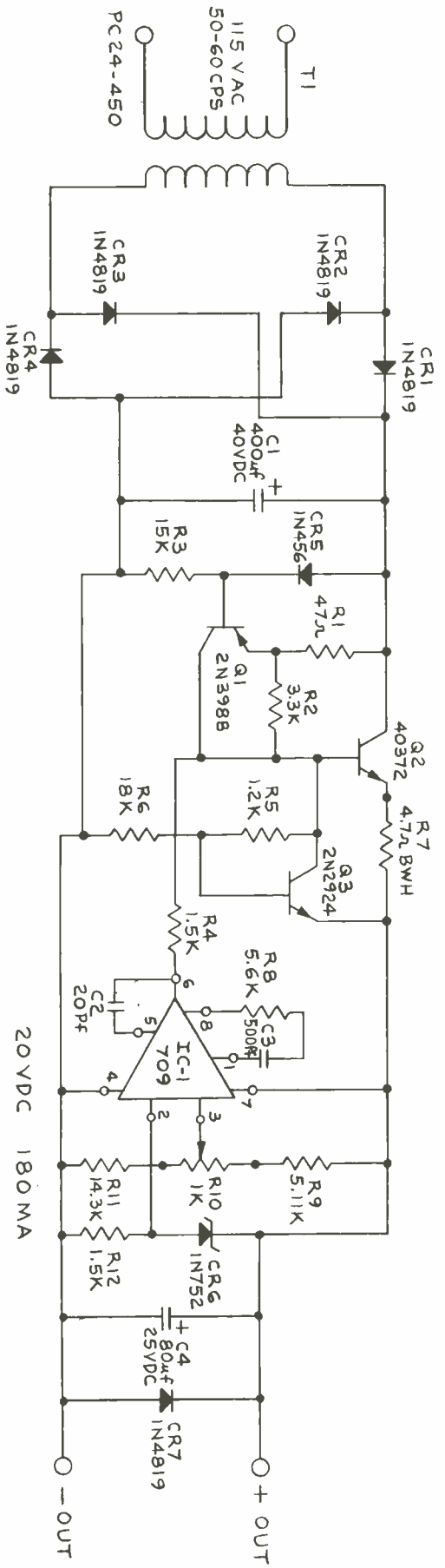


Figure 5-6. Power Supply Schematic Diagram (sheet 5 of 5).

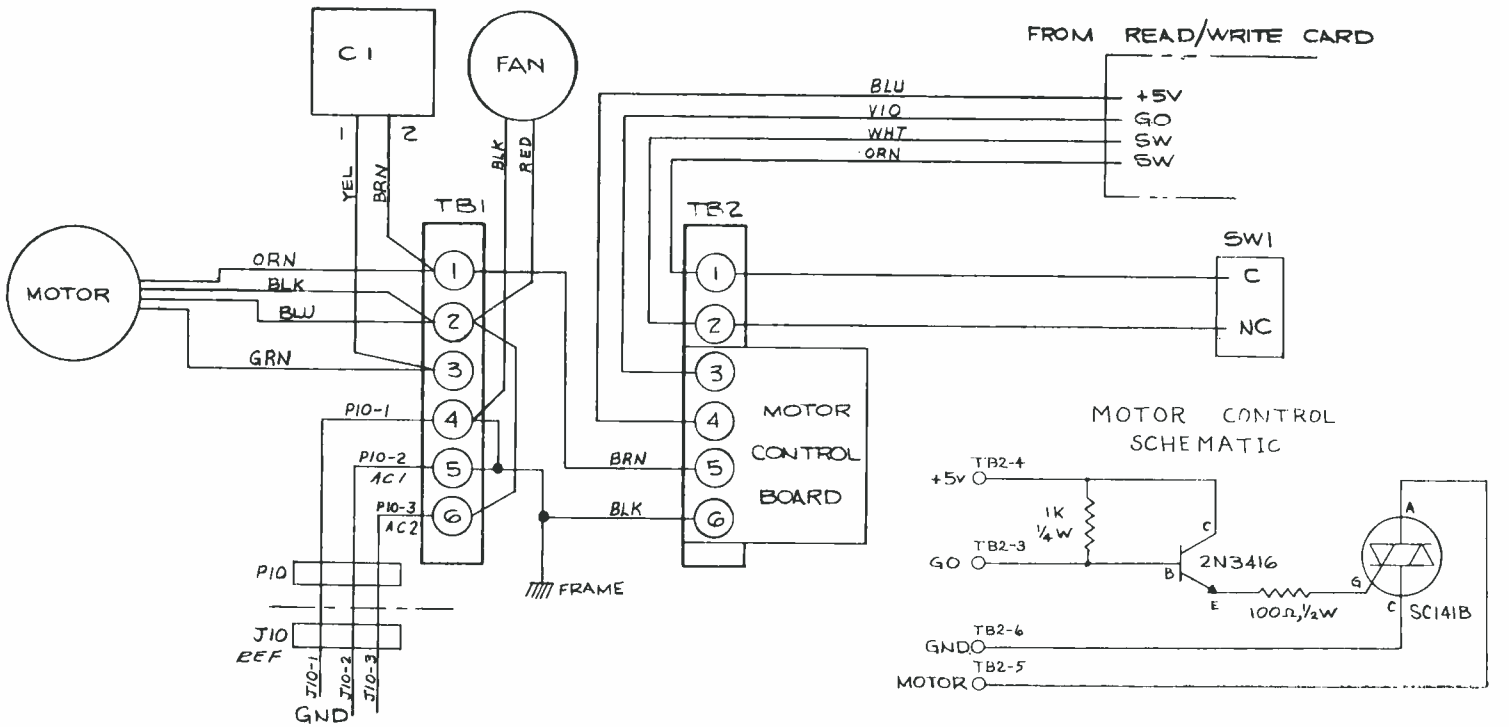


Figure 5-7. Tape Unit Wiring Diagram.

SECTION VI
REPLACEMENT PARTS LIST

GENERAL

The following tables contain the descriptions, manufacturers, and part numbers of replacement parts for the Titlefile. The tables are divided into three groups: Address Control Keyboard, Logic Controller, and Tape Unit. Each part listed is keyed, by an index number, to a component location illustration.

Address Control Keyboard

Tables 6-1 through 6-3 list the replacement parts of the Address Control Keyboard. These parts are illustrated in Figures 6-1 through 6-3.

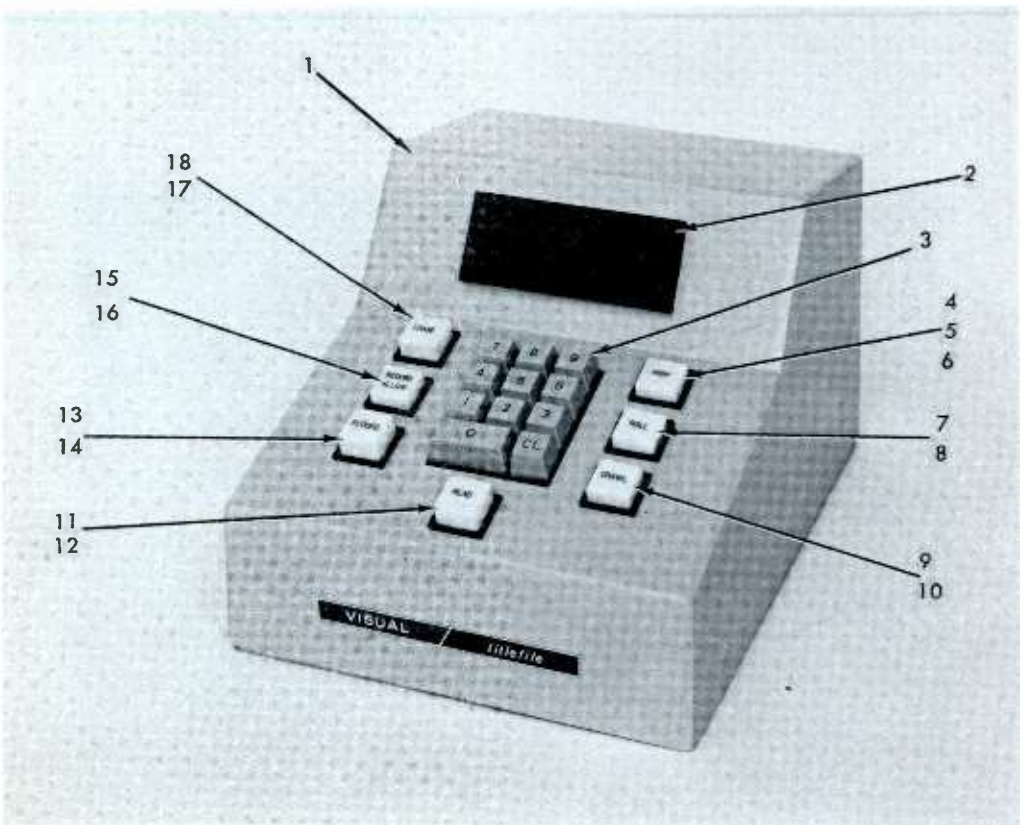


Figure 6-1. Address Control Keyboard.

Table 6-1.

ADDRESS CONTROL KEYBOARD PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Keyboard Case	Compat	4-640-0047-01
2	Bezel Assembly	Burroughs	BWB4-35000
3	Switch	Alco Switch	SB-033
4	Lamp	General Electric	345
5	Switch	Clare/Pendar	56-1182PL41W1-L
6	Button	Compat	2-460-0016-03
7	Switch	Clare/Pendar	56-1182PL41W1-L
8	Button	Compat	2-460-0016-02
9	Switch	Clare/Pendar	56-1182PL41W1-L
10	Button	Compat	2-460-0016-05
11	Switch	Clare/Pendar	1053L41W1-L
12	Button	Compat	2-460-0016-04
13	Switch	Clare/Pendar	1053L41W1-L
14	Button	Compat	2-460-0016-01
15	Switch	Clare/Pendar	56-1182PL41W1-L
16	Button	Compat	2-460-0016-06
17	Switch	Clare/Pendar	1053L41W1-L
18	Button	Compat	2-460-0016-00

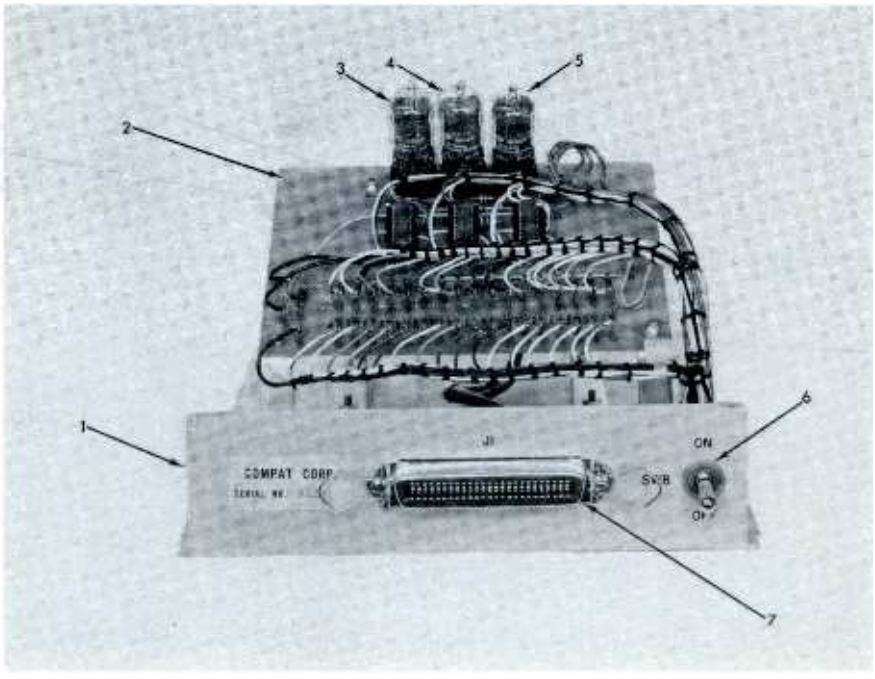


Figure 6-2. Address Control Keyboard.

Table 6-2.

ADDRESS CONTROL KEYBOARD PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Keyboard Base	Compat	3-450-0074-01
2	P.C. Board Assembly (see Fig. 6-3)	Compat	3-621-0044-01
3-5	Nixie Indicator Tube	Burroughs	5440
6	Switch	Cutler-Hammer	7564-K6
7	Connector	Amphenol	57-40500

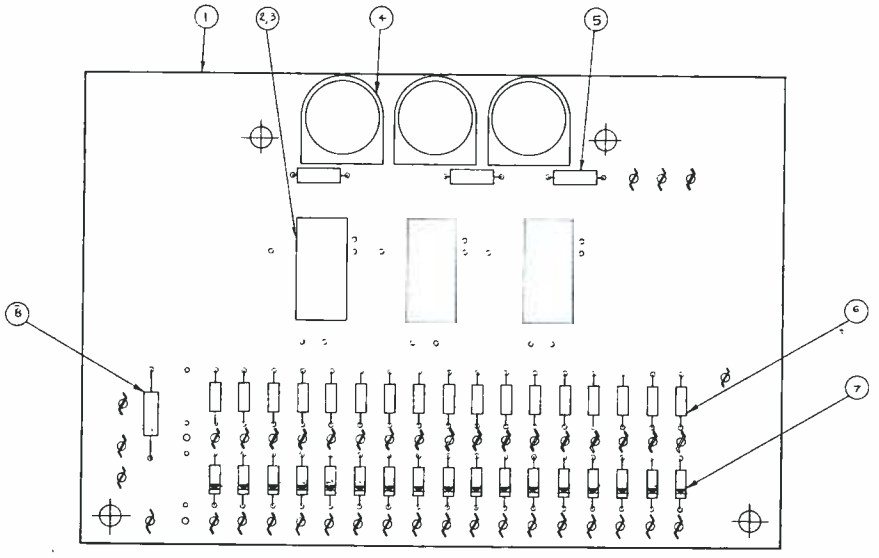


Figure 6-3. Address Control Keyboard P.C. Board Assembly.

Table 6-3.

ADDRESS CONTROL KEYBOARD P.C. BOARD ASSEMBLY PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Printed Circuit Board	Compat	3-473-006-01
2	Integrated Circuit	Texas Instruments	SN7441AN
3	Socket	Augat	316AG5D-3R
4	Socket	Burroughs	SK-196
5	Resistor	24 K ohms, 1/2W, 10%	
6	Resistor	470 ohms, 1/2W, 10%	
7	Diode	1N462	
8	Resistor	470 ohms, 1/4W, 10%	

Logic Controller

Tables 6-4 through 6-23 list the replacement parts of the Logic Controller. These parts are illustrated in Figures 6-4 through 6-23.

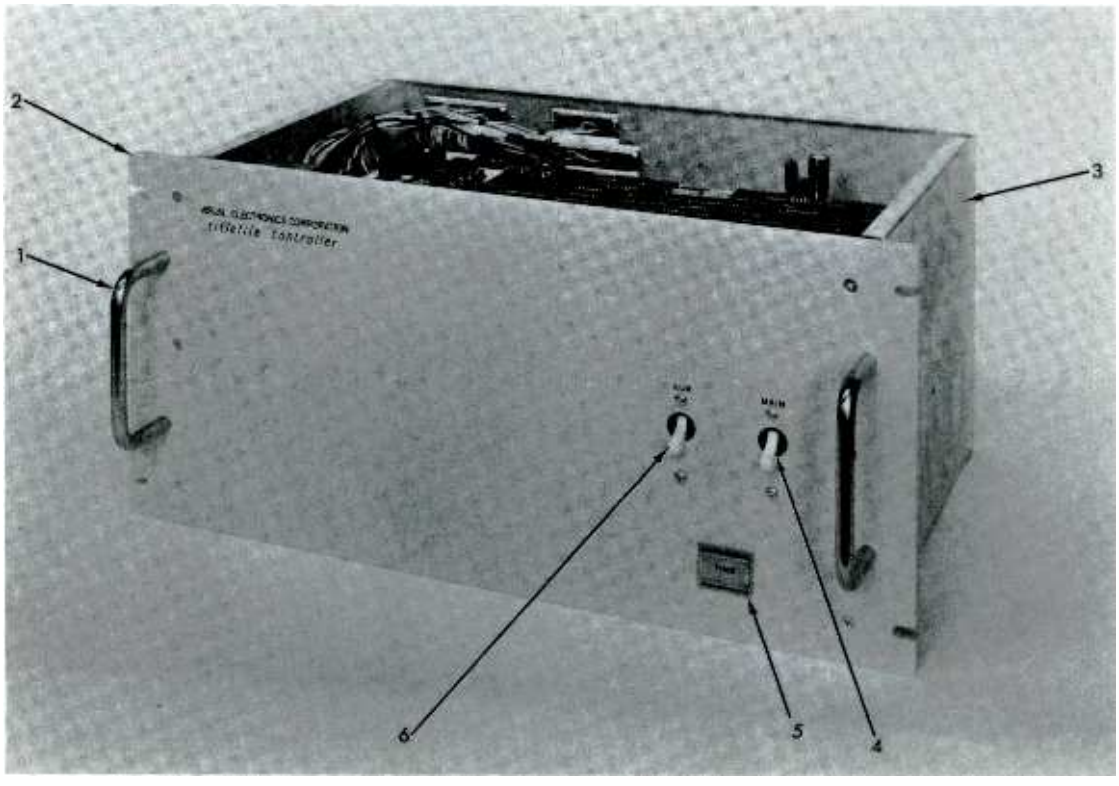


Figure 6-4. Logic Controller.

Table 6-4.
LOGIC CONTROLLER PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Handle	Amaton	1055655-1032-7
2	Front Panel	Compat	4-440-0085-01
3	Chassis Assembly (see Fig. 6-6)	Compat	4-640-0045-01
4	Circuit Breaker	Heinemann	JA1A3-2-2
5	Switch	Unimax	1121314151647181
6	Circuit Breaker	Heinemann	JA1A3-3-2

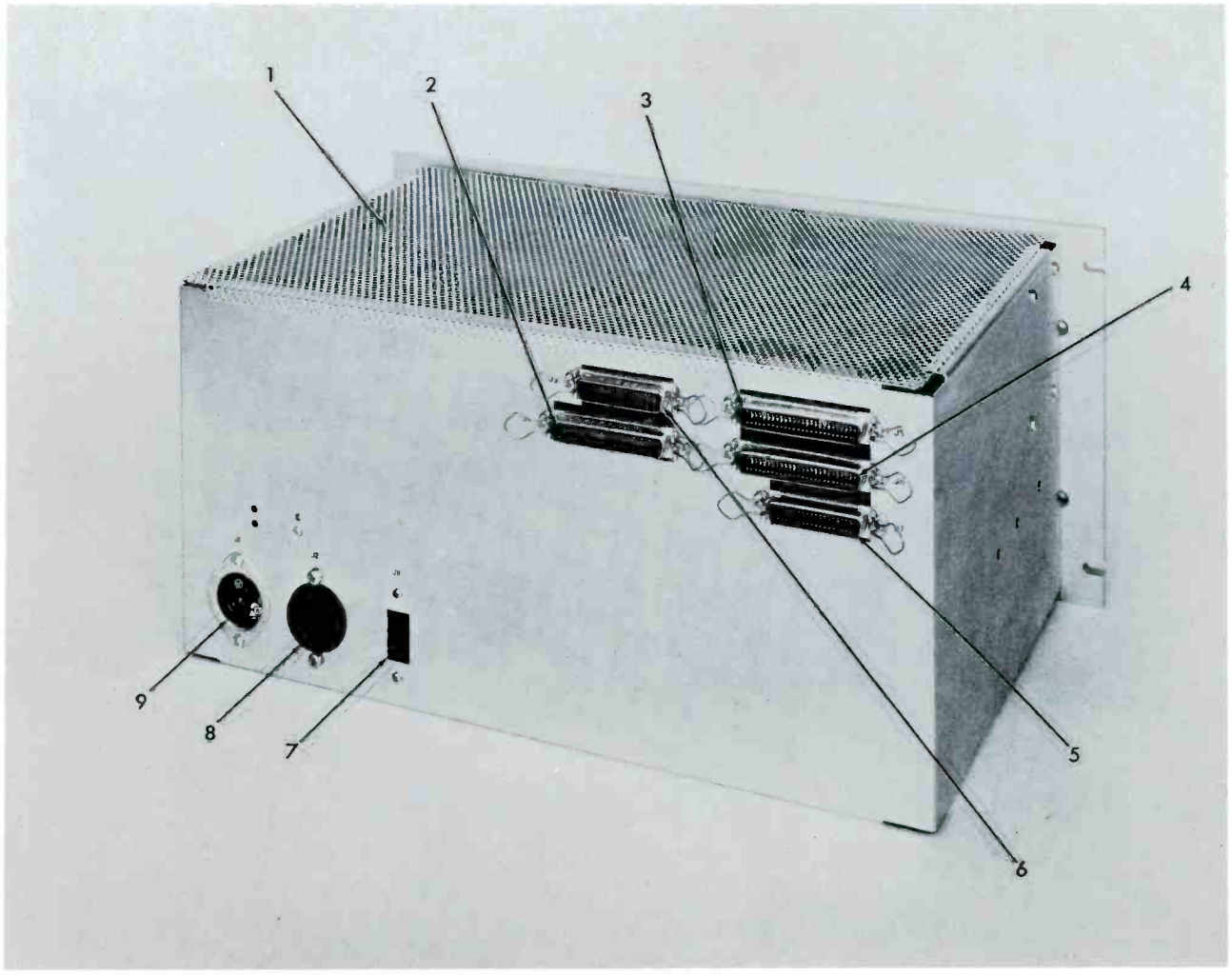


Figure 6-5. Logic Controller, Rear View.

Table 6-5.
LOGIC CONTROLLER PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Controller Chassis Cover	Compat	4-440-0094-01
2-4	Connector	Amphenol	57-40500
5,6	Connector	Amphenol	57-40360
7	Connector	Cinch	S303FP
8	Connector	Hubbell	5258
9	Connector	Hubbell	7486

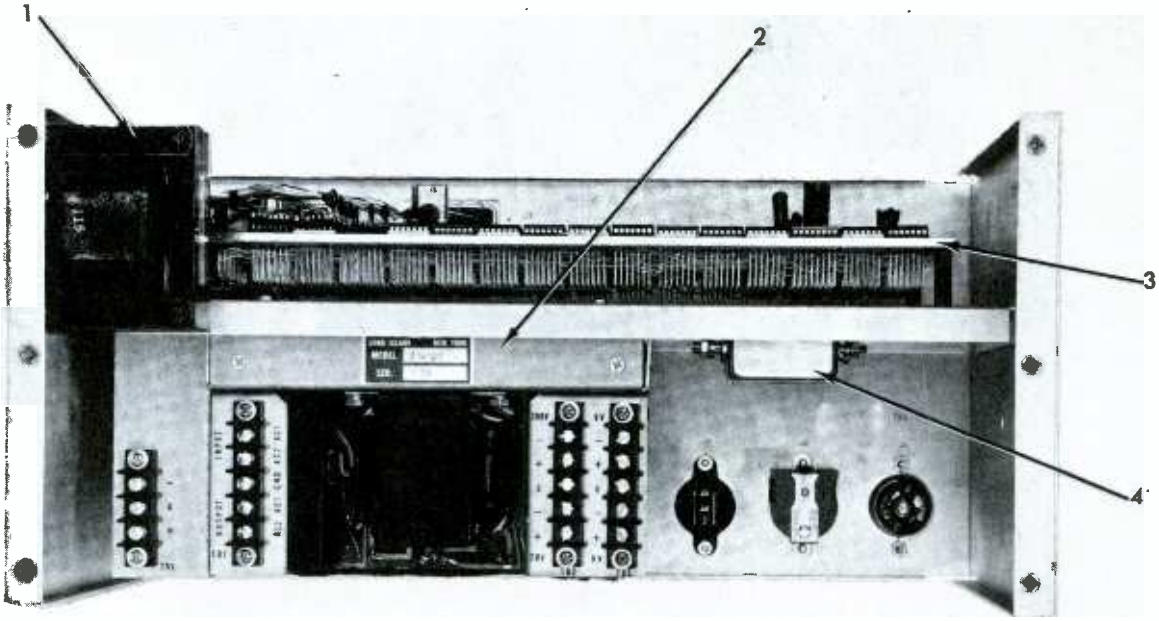


Figure 6-6. Logic Controller Chassis.

Table 6-6.
LOGIC CONTROLLER CHASSIS PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Transformer	Sig. Xfmr	120-05
2	Power Supply	Voltex	3-280-0014-01
3	Logic Board Assembly (see Fig. 6-7)	Compat	3-638-0001-01
4	R.F. Filter	All Tronics	400D65HP12

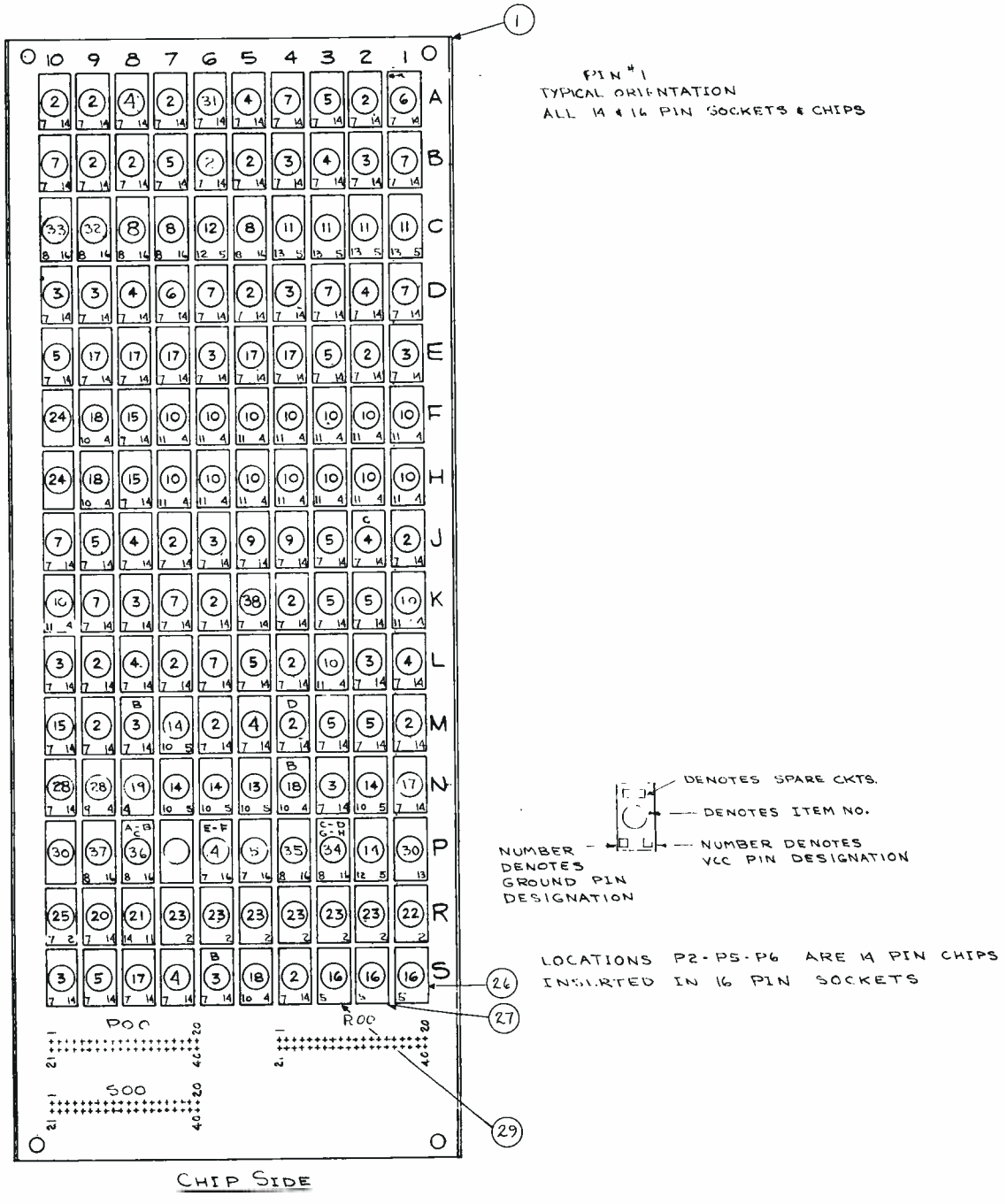


Figure 6-7. Logic Board Assembly.

Table 6-7.

LOGIC BOARD ASSEMBLY PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Tape Loop Logic Board	Compat	3-550-0012-01
2	Integrated Circuit	Texas Instruments	SN7400N
3	Integrated Circuit	Texas Instruments	SN7402N
4	Integrated Circuit	Texas Instruments	SN7404N
5	Integrated Circuit	Texas Instruments	SN7410N
6	Integrated Circuit	Texas Instruments	SN7430N
7	Integrated Circuit	Texas Instruments	SN7440N
8	Integrated Circuit	Texas Instruments	SN7442N
9	Integrated Circuit	Texas Instruments	SN7451N
10	Integrated Circuit	Texas Instruments	SN7473N
11	Integrated Circuit	Texas Instruments	SN7476N
12	Integrated Circuit	Texas Instruments	SN7483N
13	Integrated Circuit	Texas Instruments	SN7492N
14	Integrated Circuit	Texas Instruments	SN7493N
15	Integrated Circuit	Texas Instruments	SN7495N
16	Module Assembly (see Fig.6-8)	Compat	2-637-0069-01
17	Integrated Circuit	Fairchild	TTuL9601
18	Integrated Circuit	Sylvania	SG83
19	Osc.Chip (see Fig.6-9)	Compat	3-623-0002-01
20	Key Stroke Integrator (see Fig.6-10)	Compat	2-637-0034-01
21	Level Converter (see Fig.6-11)	Compat	2-637-0035-01
22	Level Converter (see Fig.6-12)	Compat	2-637-0036-01
23	Clock Driver (see Fig.6-13)	Compat	2-637-0037-01
24	Buffer Chip (see Fig.6-14)	Compat	2-637-0038-01
25	Initial Clear Circuit (see Fig.6-15)	Compat	2-637-0039-01
26,27	Connector Shell	Amphenol	1-86148-1
28	Neg.Edge Differentiator (see Fig.6-16)	Compat	2-637-0042-01
29	Connector Shell	Amphenol	1-86148-1
30	Adapter Plug	Augat	8136-29G2
31	Plug-In Module RC/7 (see Fig.6-17)	Compat	2-637-0062-01
32	Plug-In Module RC/8 (see Fig.6-18)	Compat	2-637-0063-01
33	Plug-In Module RC/9 (see Fig.6-19)	Compat	2-637-0064-01
34	Plug-In Module RC/10 (see Fig.6-20)	Compat	2-637-0065-01
35	Plug-In Module RC/11 (see Fig.6-21)	Compat	2-637-0066-01
36	Plug-In Module RC/12 (see Fig.6-22)	Compat	2-637-0067-01
37	Plug-In Module RC/13 (see Fig.6-23)	Compat	2-637-0068-01
38	Integrated Circuit	Texas Instruments	SN74H40N

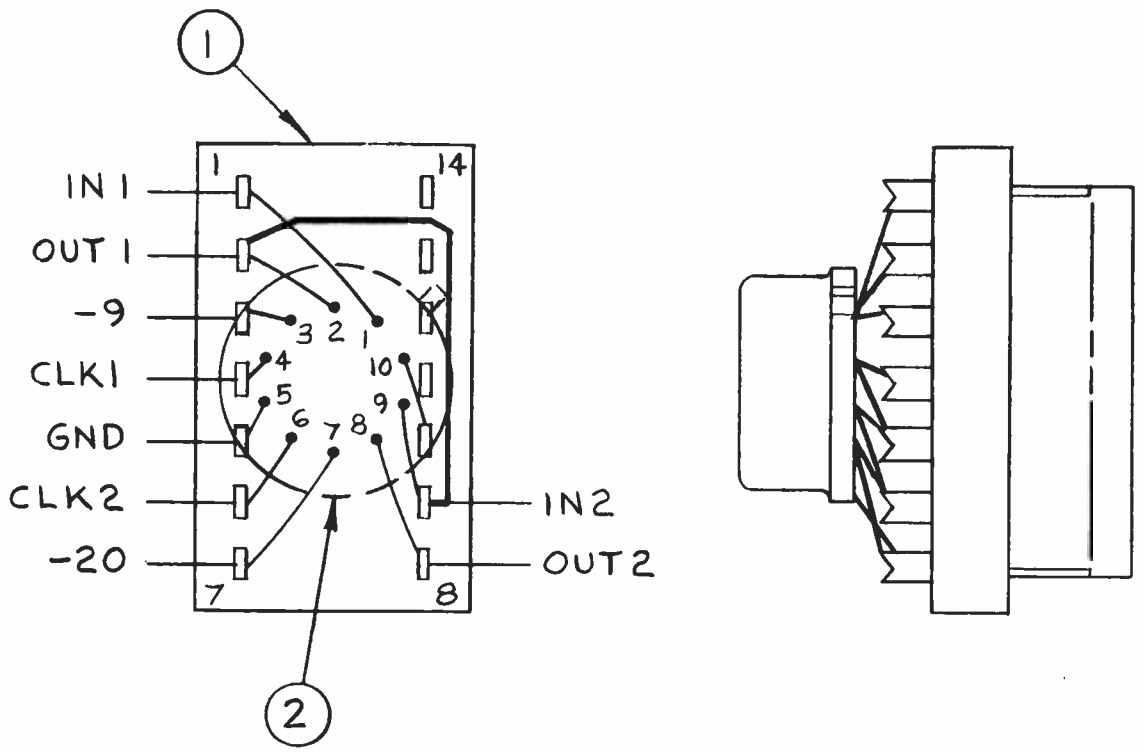


Figure 6-8. Module Assembly.

Table 6-8.
MODULE ASSEMBLY PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Texas Instruments	IC-D14DC-7518
2	Integrated Circuit	Texas Instruments	TMS7C3003LA

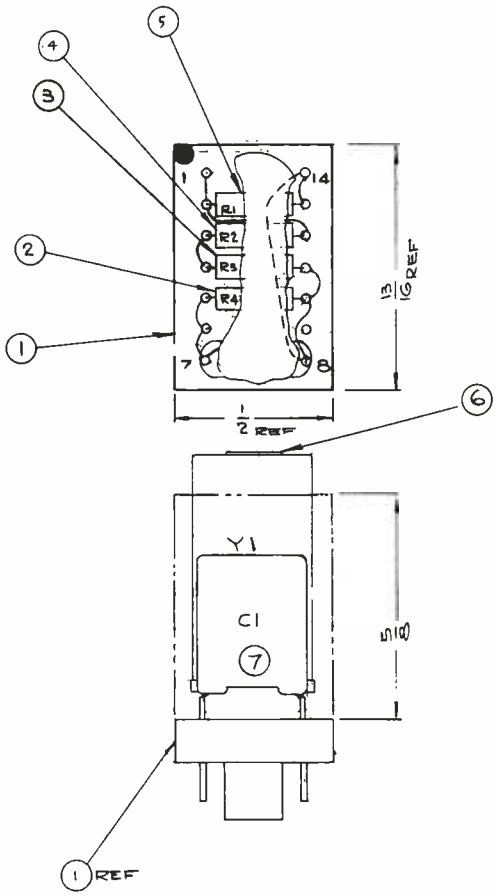


Figure 6-9. Oscillator Chip Assembly.

Table 6-9.

OSCILLATOR CHIP ASSEMBLY PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Connector	Texas Instruments	MPC-20
2	Resistor	2 K ohms, Y4W, 5%	
3,4	Resistor	1.5 K ohms, 1/4W, 5%	
5	Resistor	2 K ohms, 1/4W, 5%	
6	Crystal	1.18MHZ, 1%-Hunt	HC-G Can
7	Capacitor	0.047 uf, 10V-IEC	EM470-03

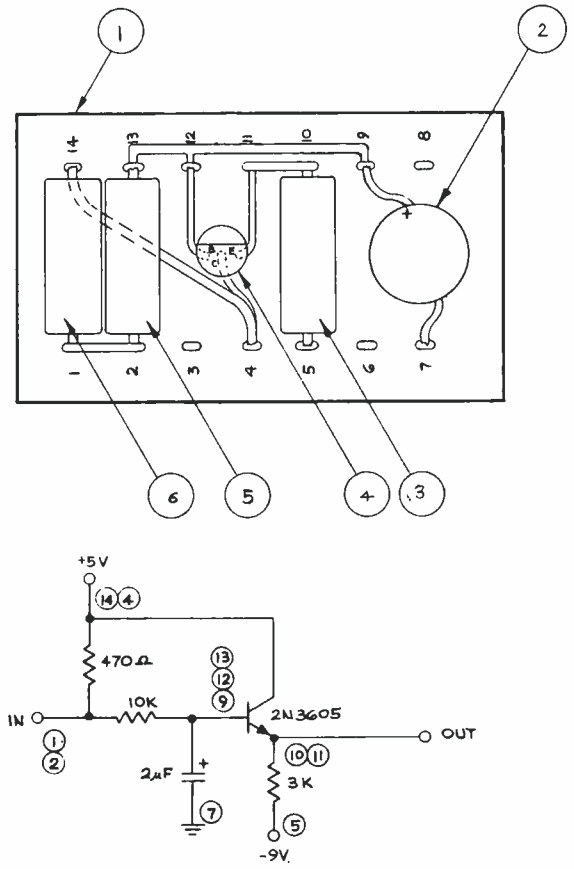
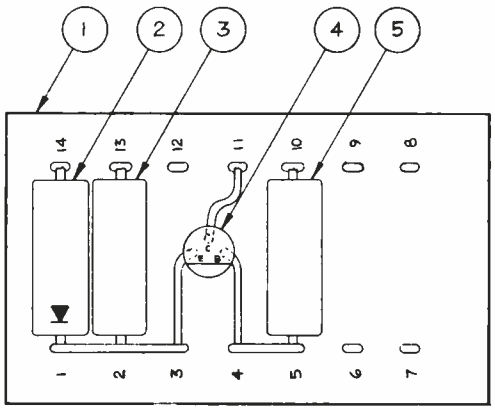


Figure 6-10. Key Stroke Integrator.

Table 6-10.

KEY STROKE INTEGRATOR PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Texas Instruments	IC-014DC-7518
2	Capacitor	2 uf, 25V-IEC	PCW002PA25
3	Resistor	3 K ohms, 1/4W, 5%	
4	Transistor	2N3605	
5	Resistor	10 K ohms, 1/4W, 5%	
6	Resistor	470 ohms, 1/4W, 5%	



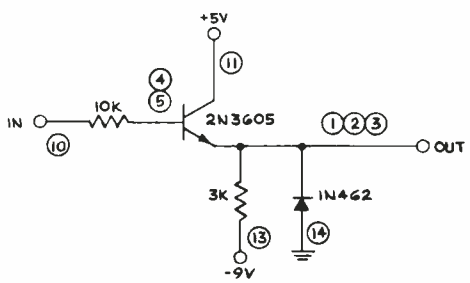


Figure 6-11. Level Converter.

Table 6-11.
LEVEL CONVERTER PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Texas Instruments	IC-014DC-7518
2	Diode	1N462	
3	Resistor	3 K ohms, 1/4W, 5%	
4	Transistor	2N3605	
5	Resistor	10 K ohms, 1/4W, 5%	

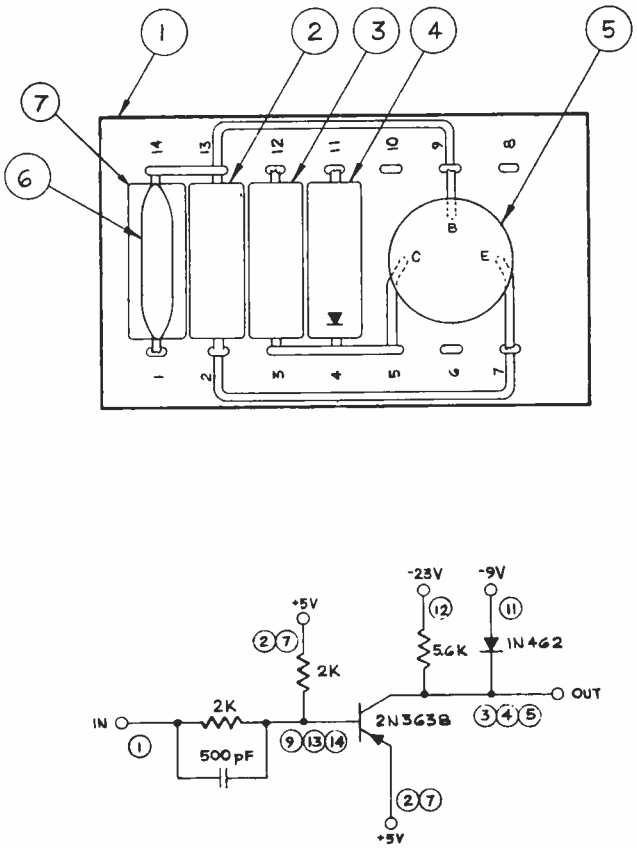


Figure 6-12. Level Converter.

Table 6-12.
LEVEL CONVERTER PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Texas Instruments	IC-014DC-7518
2	Resistor	2 K ohms, 1/4W, 5%	
3	Resistor	5.6 K ohms, 1/4W, 5%	
4	Diode	1N462	
5	Transistor	2N3638	
6	Capacitor	500 pf, 10V-Centralab	DD-501
7	Resistor	2 K ohms, 1/4W, 5%	

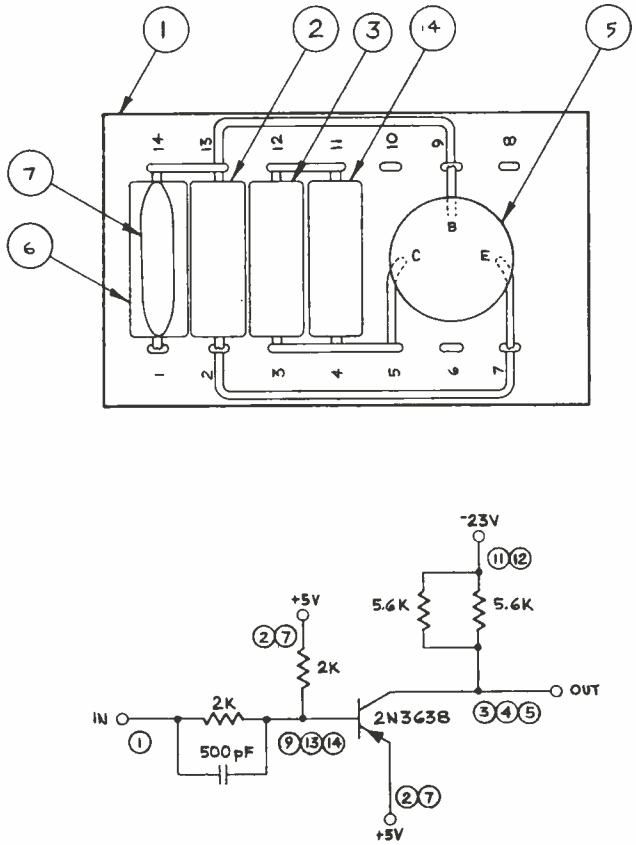


Figure 6-13. Clock Driver.

Table 6-13.

CLOCK DRIVER PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Texas Instruments	IC-014DC-7518
2	Resistor	2 K ohms, 1/4W, 5%	
3,4	Resistor	5.6 K ohms, 1/4W, 5%	
5	Transistor	2N3638	
6	Resistor	2 K ohms, 1/4W, 5%	
7	Capacitor	500 pf, 10V-Centralab	DD-501

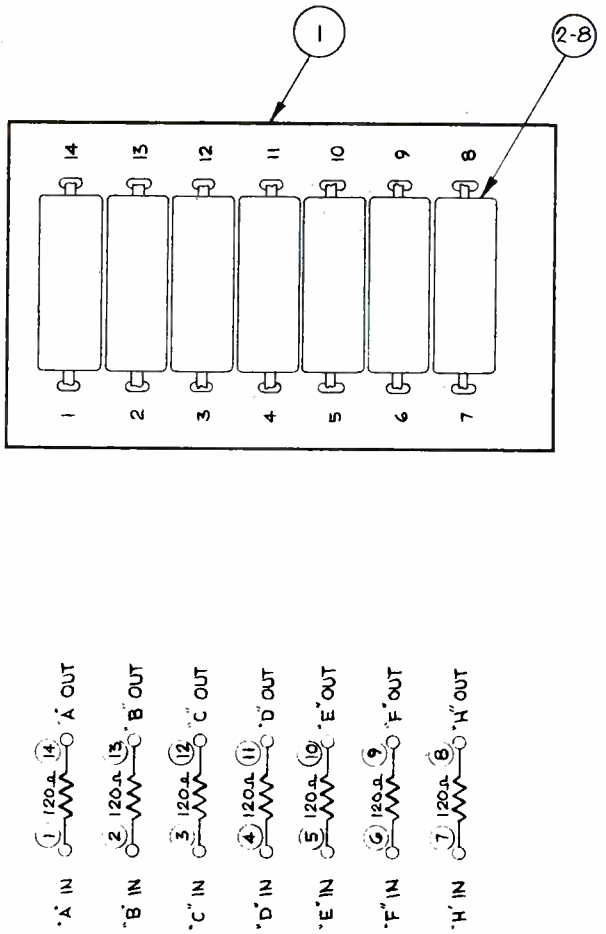


Figure 6-14. Buffer Chip.

Table 6-14.

BUFFER CHIP PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Texas Instruments	IC-014DC-7518
2-8	Resistor	120 ohm, 1/4W, 5%	

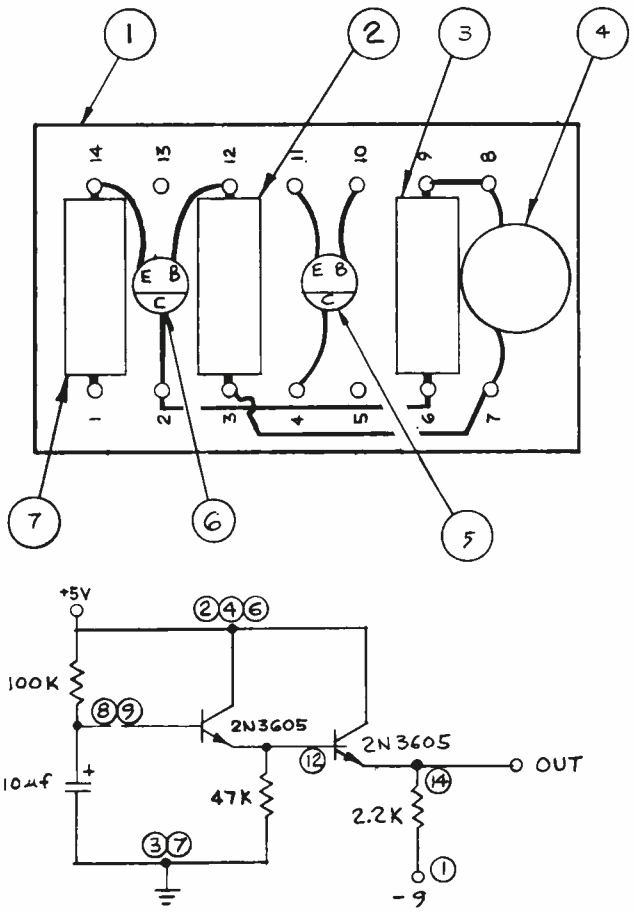


Figure 6-15. Initial Clear Circuit.

Table 6-15.
INITIAL CLEAR CIRCUIT PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Texas Instruments	IC-014DC-7518
2	Resistor	47 K ohms, 1/4W, 5%	
3	Resistor	100 K ohms, 1/4W, 5%	
4	Capacitor	10 uf, 15V-IEC	PCW010PB15
5,6	Transistor	2N3605	
7	Resistor	2.2 K ohms, 1/4W, 5%	

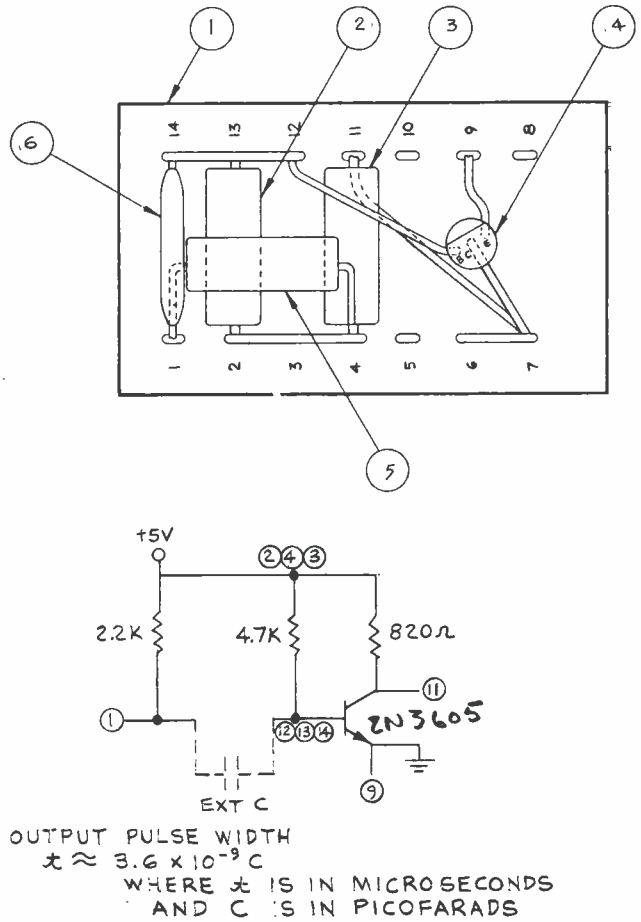
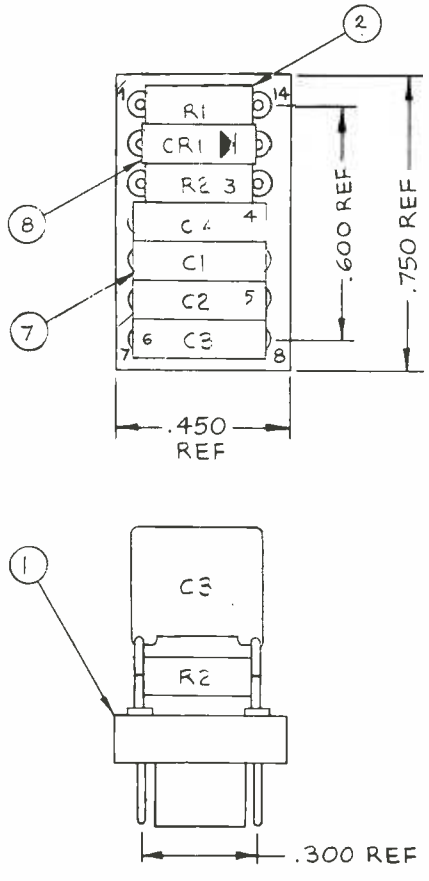


Figure 6-16. Neg. Edge Differentiator.

Table 6-16.

NEG. EDGE DIFFERENTIATOR PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Texas Instruments	IC-014DC-7518
2	Resistor	4.7 K ohms, 1/4W, 5%	
3	Resistor	820 ohms, 1/4W, 5%	
4	Transistor	2N3605	
5	Resistor	2.2 K ohms, 1/4W, 5%	
6	Capacitor	0.001 uf, 10V-IEC	EM10-05



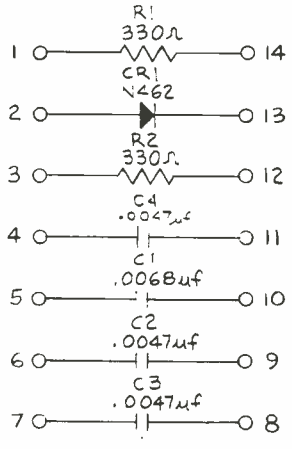


Figure 6-17. Plug-In Module RC/7.

Table 6-17.

PLUG-IN MODULE RC/7 PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Texas Instruments	IC-014DC-7518
2,3	Resistor	330 ohms, 1/4W, 5%	
4-6	Capacitor	0.0047 uf, 10V-IEC	EM47-05
7	Capacitor	0.0068 uf, 10V-IEC	EM68-05
8	Diode	1N462	

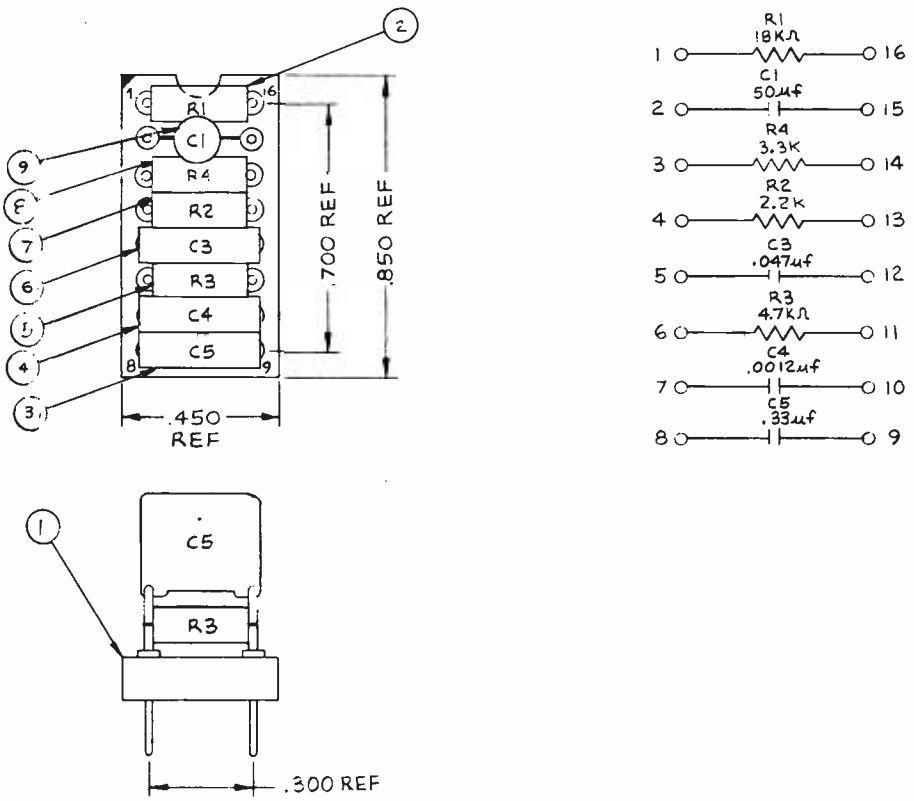


Figure 6-18. Plug-In Module RC/8.

Table 6-18.

PLUG-IN MODULE RC/8 PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Texas Instruments	IC-014DC-7518
2	Resistor	18 K ohms, 1/4W, 5%	
3	Capacitor	0.33 uf, 10V-Sprague	HY-327
4	Capacitor	0.0012 uf, 10V-Sprague	5GA-D12
5	Resistor	4.7 K ohms 1/4W, 5%	
6	Capacitor	0.047 uf, 10V-IEC	EM470-03
7	Resistor	2.2 K ohms, 1/4W, 5%	
8	Resistor	3.3 K ohms, 1/4W, 5%	
9	Capacitor	50 uf, 6V-IEC	PCW050PA6

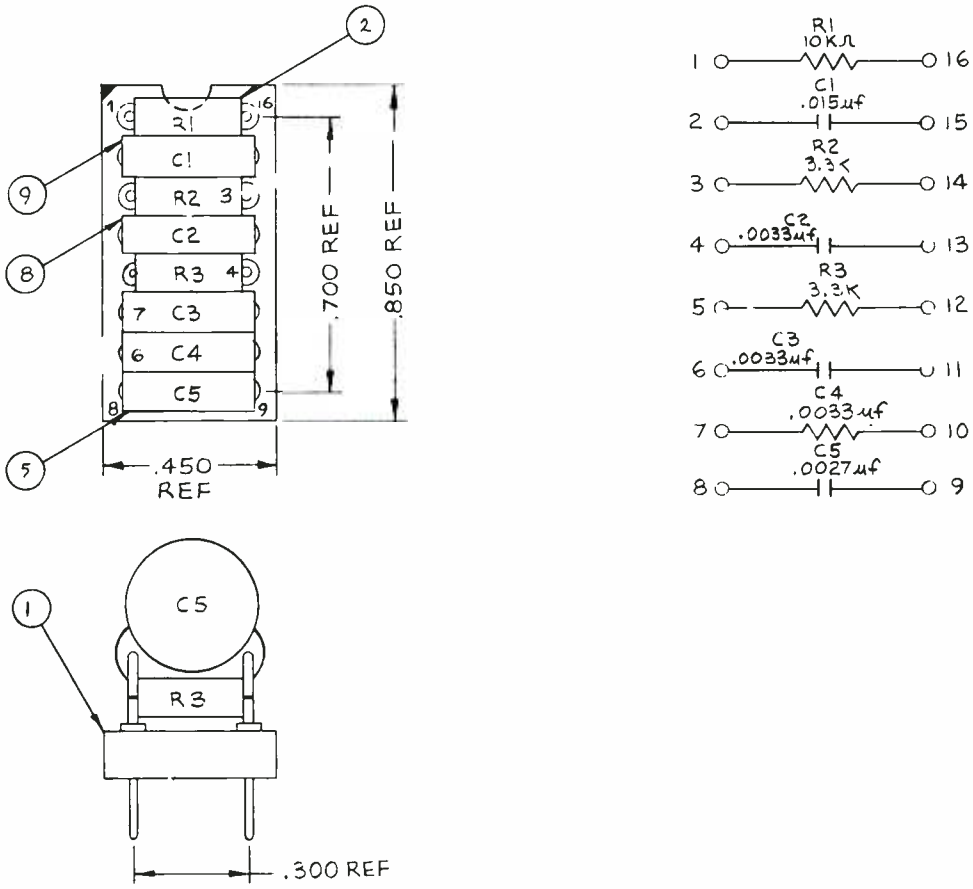


Figure 6-19. Plug-In Module RC/9.

Table 6-19.
PLUG-IN MODULE RC/9 PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Augat	8136-29G2
2	Resistor	10 K ohms, 1/4W, 5%	
3,4	Resistor	3.3 K ohms, 1/4W, 5%	
5	Capacitor	0.0027 uf, 10V-Sprague	SGA-D27
6-8	Capacitor	0.0033 uf, 10V-IEC	EM33-05
9	Capacitor	0.015 uf, 10V-IEC	EM150-03

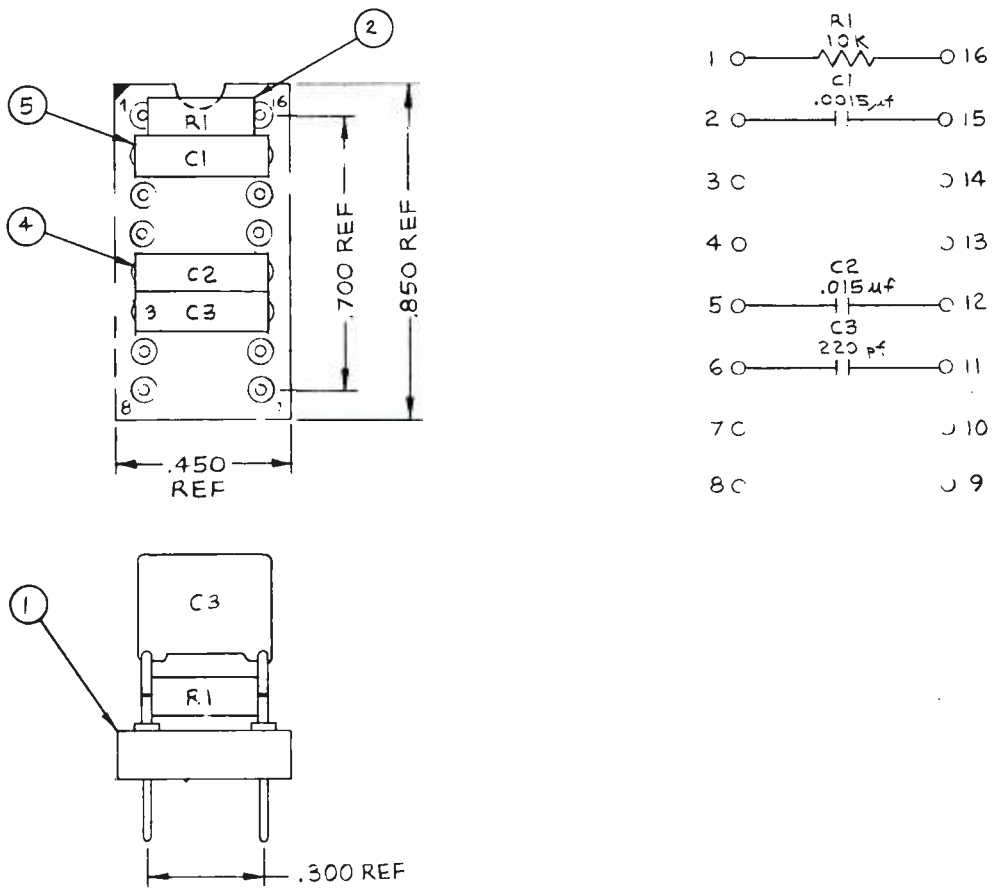


Figure 6-20. Plug-In Module RC/10.

Table 6-20.

PLUG-IN MODULE RC/10 PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Augat	8136-29G2
2	Resistor	10 K ohm, 1/4W, 5%	
3	Capacitor	220 pf, 10V-Centralab	DD-221
4	Capacitor	0.015 uf, 10V-IEC	EM150-03
5	Capacitor	0.0015 uf, 10V-IEC	EM15-05

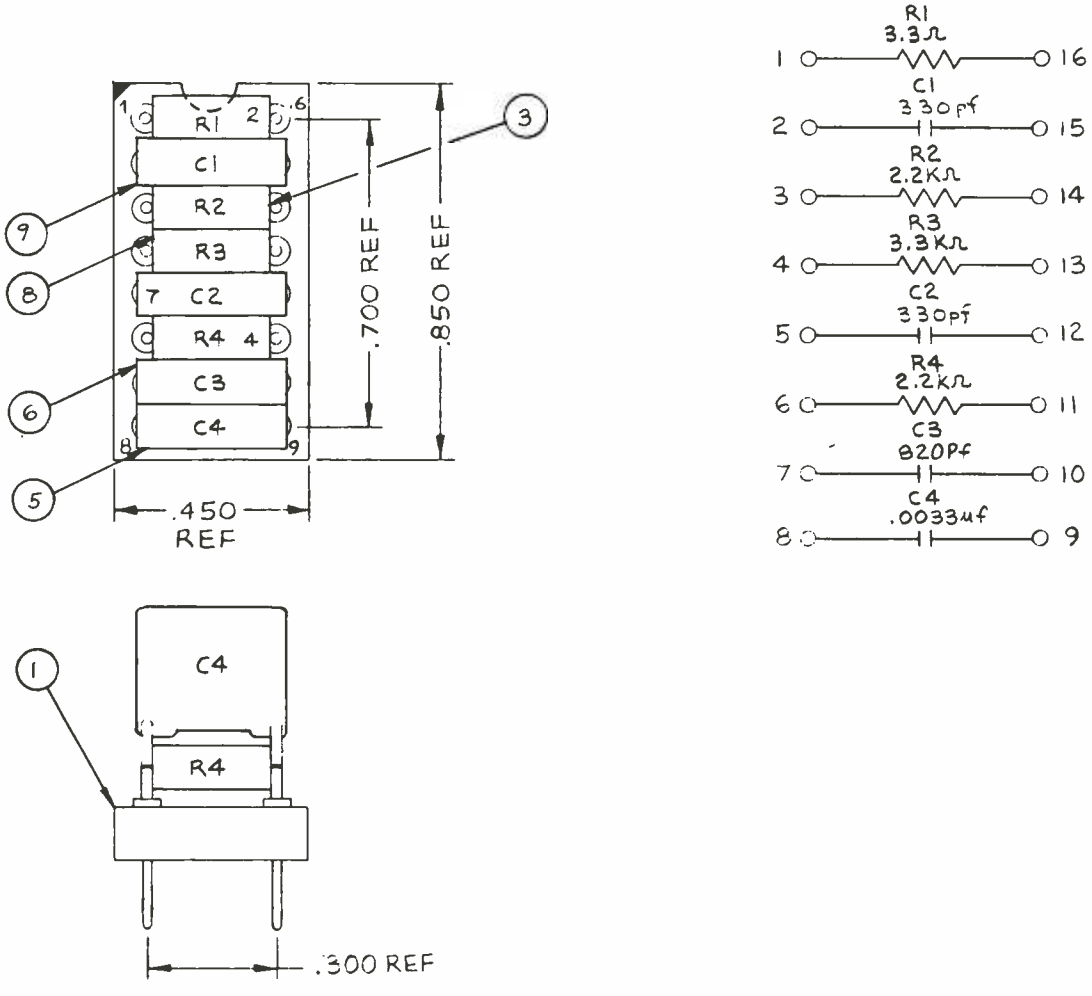


Figure 6-21. Plug-In Module RC/11.

Table 6-21.

PLUG-IN MODULE RC/11 PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Augat	8136-29G2
2,8	Resistor	3.3 K ohm, 1/4W, 5%	
3,4	Resistor	2.2 K ohm, 1/4W, 5%	
5	Capacitor	0.0033 uf, 10V-IEC	EM33-05
6	Capacitor	820 pf, 10V-Centralab	DD-821
7,9	Capacitor	330 pf, 10V-Centralab	DD-331

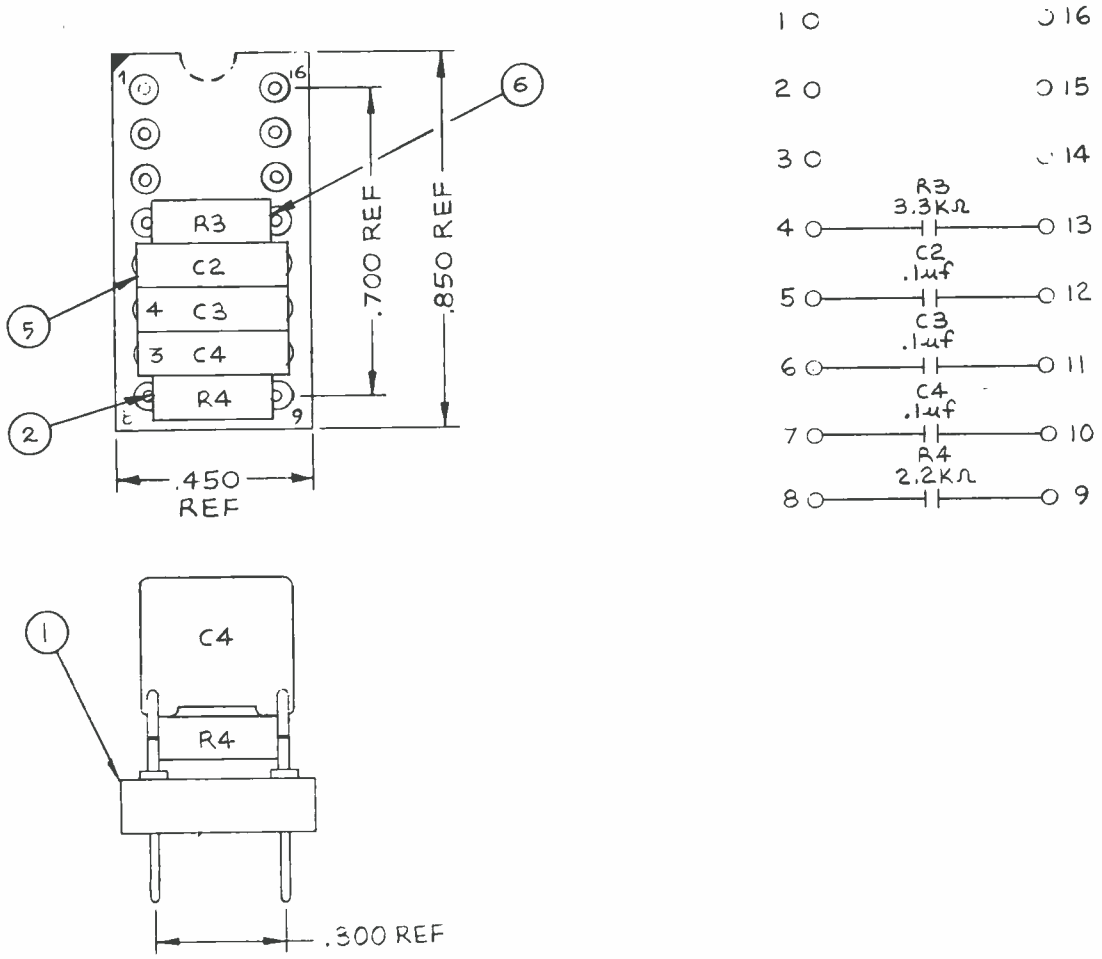


Figure 6-22. Plug-In Module RC/12.

Table 6-22.

PLUG-IN MODULE RC/12 PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Augat	8136-29G2
2	Resistor	2.2 K ohms, 1/4W, 5%	
3-5	Capacitor	0.1 uf, 10V-IEC	EM1000-03
6	Resistor	3.3 K ohms, 1/4W, 5%	

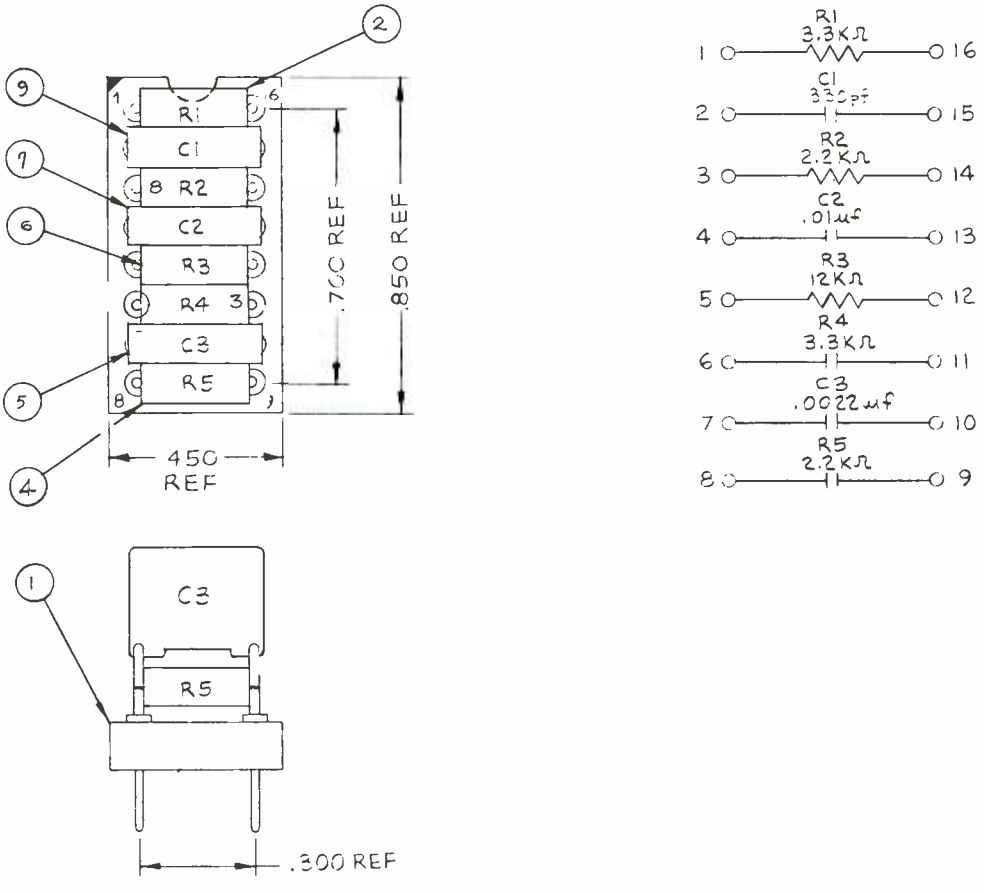


Figure 6-23. Plug-In Module RC/13.

Table 6-23.
PLUG-IN MODULE RC/13 PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Adapter Plug	Augat	8136-29G2
2,3	Resistor	3.3 K ohms, 1/4W, 5%	
4,8	Resistor	2.2 K ohms, 1/4W, 5%	
5	Capacitor	0.0022 uf, 10V-IEC	EM22-05
6	Resistor	12 K ohms, 1/4W, 5%	
7	Capacitor	0.01 uf, 10V-IEC	EM100-03
9	Capacitor	330 pf, 10V-Centralab	DD331

Tape Unit

Tables 6-24 through 6-28 list the replacement parts of the Tape Unit. These parts are illustrated in Figures 6-24 through 6-28.

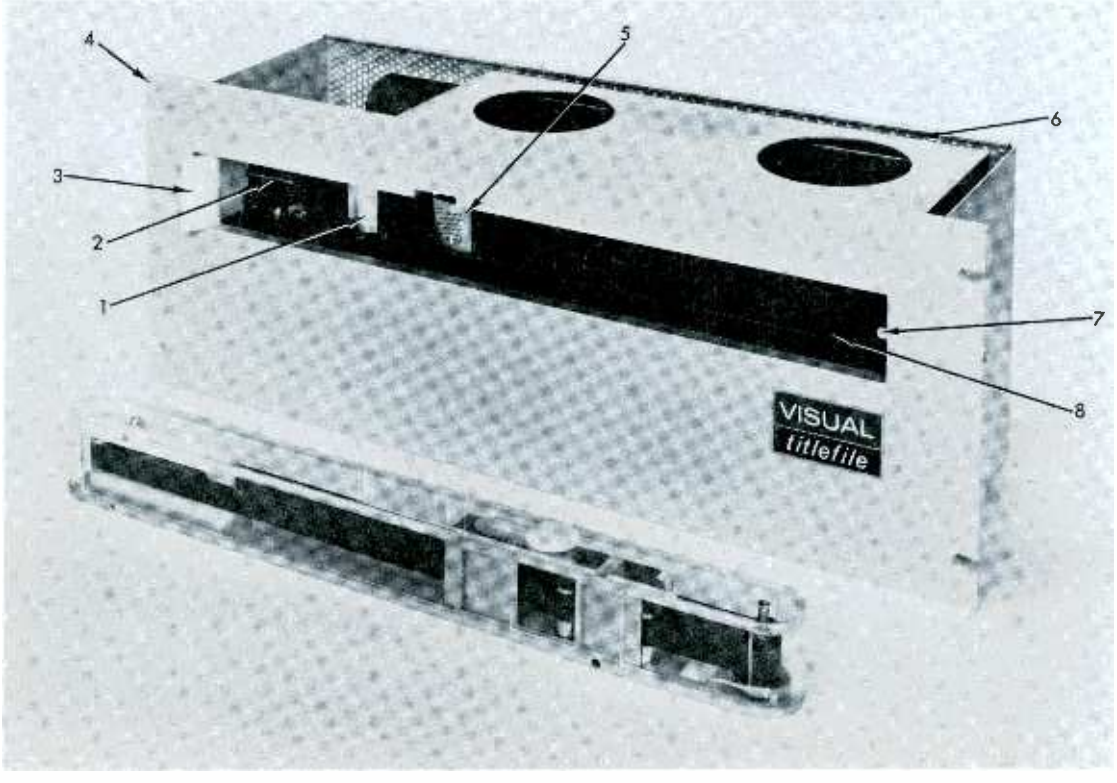


Figure 6-24. Tape Unit, Front View.

Table 6-24.
TAPE UNIT PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Head Assembly	Compat	4-610-0040-01
2	Plunger	Compat	1-440-0108-01
3	Latch Assembly	Compat	2-640-0051-01
4	Front Panel	Compat	4-420-0007-02
5	Cleaner Assembly	Compat	3-640-0049-01
6	Mag Tape Cover	Compat	4-640-0057-01
7	Plunger	Compat	1-440-0109-01
8	Actuator	Compat	1-440-0117-01

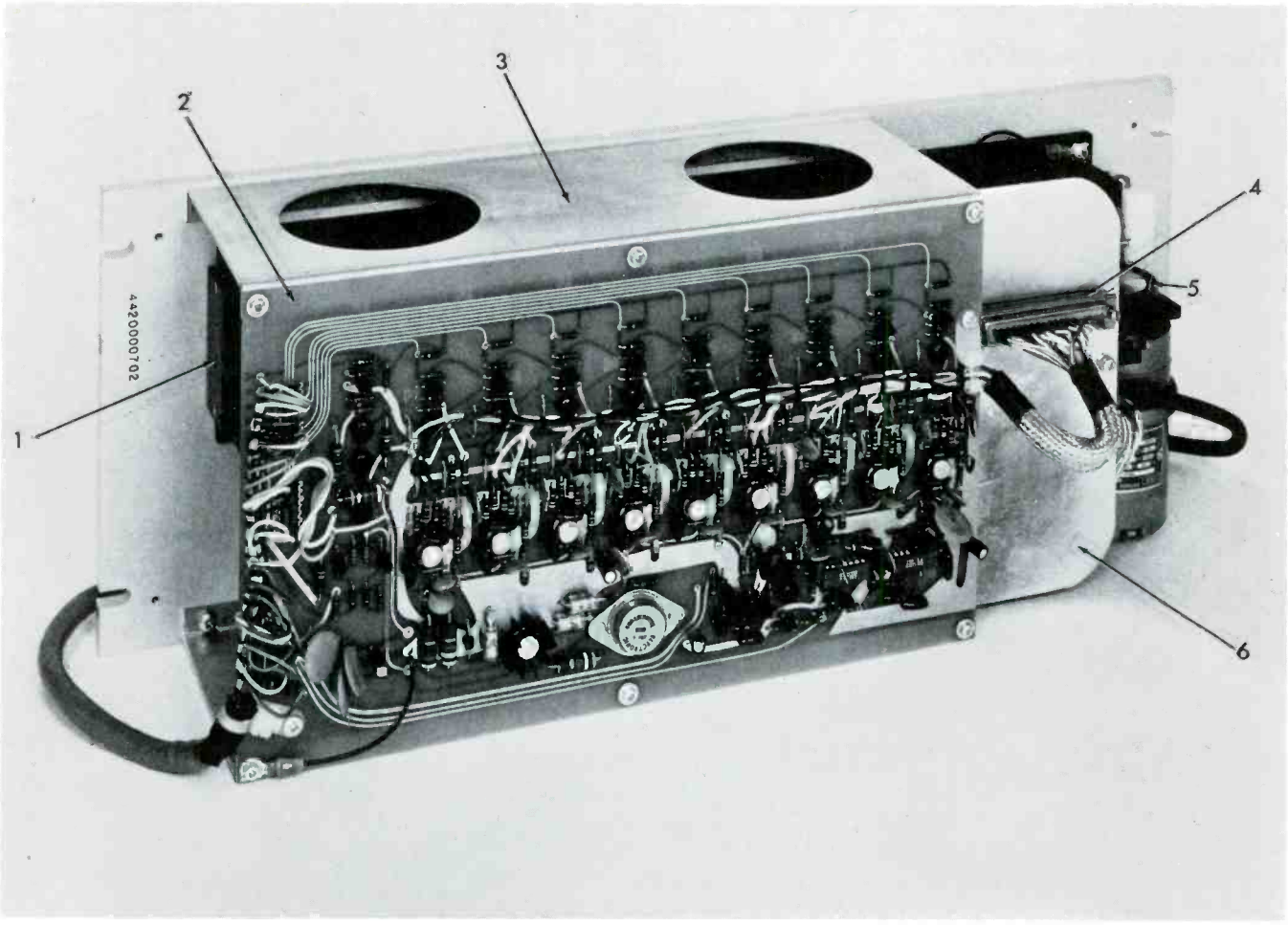


Figure 6-25. Tape Unit, Rear View.

Table 6-25.
TAPE UNIT PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	End Plate	Compat	1-440-0107-01
2	Read/Write Amplifier Assembly (see Fig.6-27)	Compat	2-637-0047-02
3	Card Bracket	Compat	4-450-0079-01
4	Receptacle	Cannon	DC37-P
5	Capstan Assembly	Compat	2-640-0054-06
6	Card Shield	Compat	3-450-0078-01

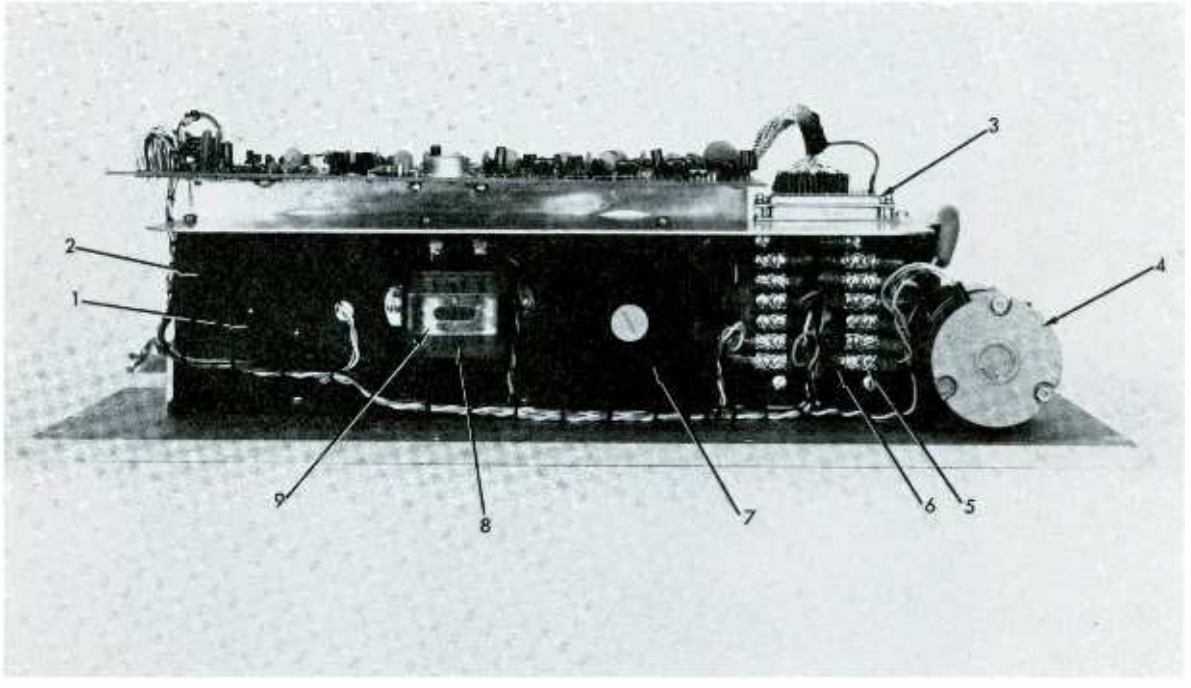


Figure 6-26. Tape Unit, Bottom View.

Table 6-26.
TAPE UNIT PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Switch	Micro Switch	V3-1101-D8
2	Frame	Compat	4-440-0123-01
3	Connector	Cannon	DC37-S
4	Motor	Elinco	FBSHFNE583
5	Barrier Strip	Kulka	600A-6
6	Marker Strip	Kulka	MS600A-6
7	Motor Control Assembly (see Fig.6-28)	Compat	2-621-0047-01
8	Rotron Fan	Sprite	SP2A2
9	Capacitor	Sprague	OV-2020
10	Mounting Bracket	Sprague	OVC-1

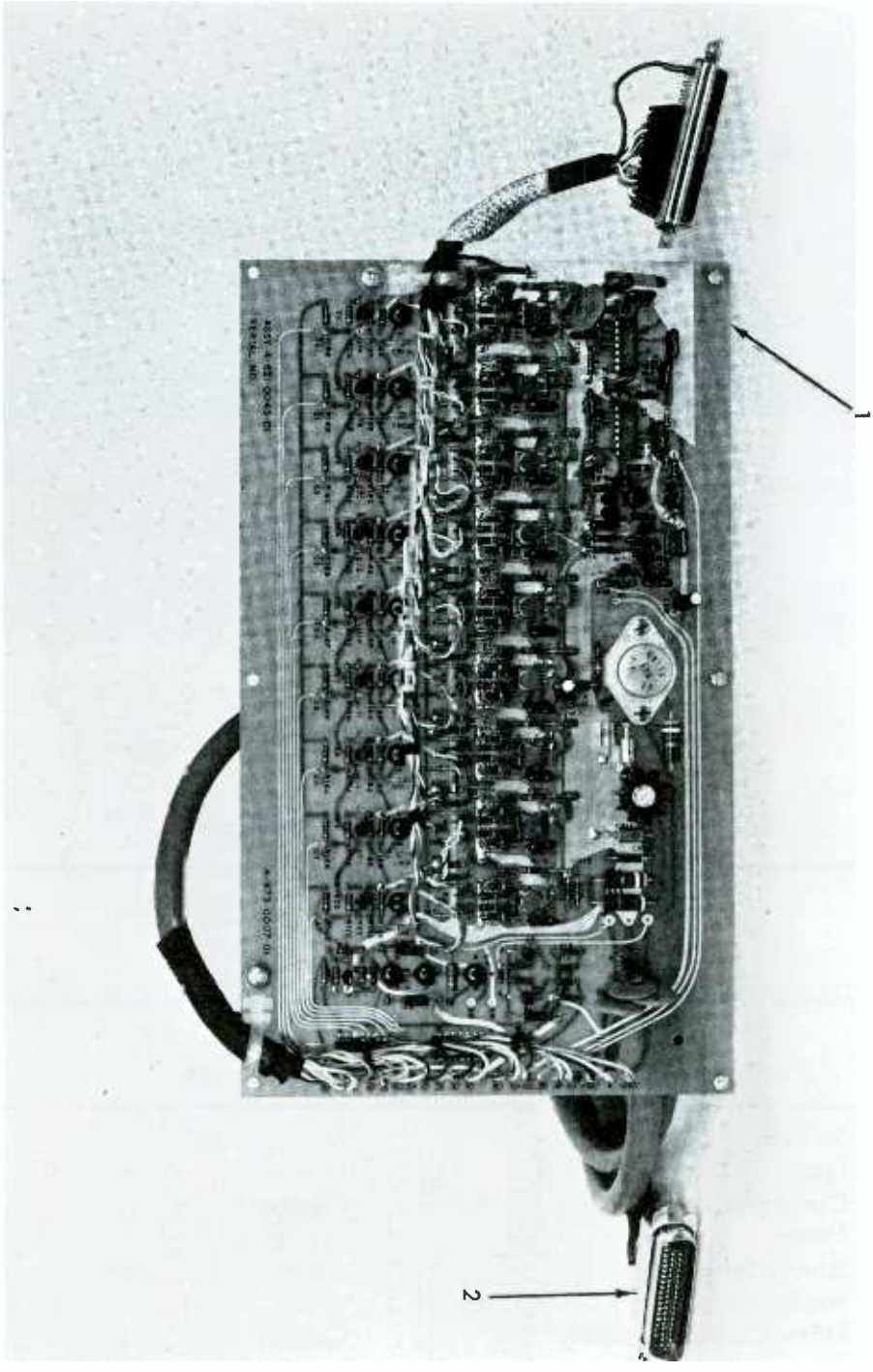


Figure 6-27. Read/Write Amplifier Assembly.

Table 6-27.

READ/WRITE AMPLIFIER ASSEMBLY PARTS LIST

Reference Designation	Description	Manufacturer and Part No.
1	P.C. Board	Compat 4-473-0007-01
2	Connector	Amphenol 57-30360
C1, C8	Capacitor, 0.01 uf, 100V	
C2, C18, C19 C26, C27, C28	Capacitor, 1 uf, 50V	IEC PCX-1GA50
C3A-C3K, C5A-C5K, C6, C17, C20	Capacitor, 0.001 uf, 100V	
C4A-C4K	Capacitor, 150 pf, 500V	DM15-1515
C7A-C7K, C9,	Capacitor, 560 pf, 500V	DM15-561J
C13, C10, C14, C15, C16	Capacitor, 50 pf, 500V	DM15-500J
C12	Capacitor, 100 pf, 500V	DM15-101J
C21	Capacitor, 220 pf, 500V	DM15-221J
C22, C23, C24,	Capacitor, 20 pf, 500V	DM15-200J
C25, C29	Capacitor, 0.1 uf, 50V	Centralab CK-104
CR1A-CR1K, CR2A-CR2K, CR3A-CR3K, CR4A-CR4K, CR5A-CR5K, CR6A-CR6K, CR7A-CR7K	Diode	General Electric 1N914
CR8	Diode, Zener	Motorola 1N3016
CR9, CR10	Diode	I.R. 1N2069
CR11, CR12	Diode, Zener	Motorola 1N3022
Q1, Q5, Q6 Q7A-Q7K, Q10-Q15	Transistor	General Electric 2N3605
Q2-Q4, Q8A-Q8K, Q9	Transistor	Fairchild 2N3638
Q17	Transistor	RCA 2N176
Q18	Transistor	RCA 2N40348
	Heat Sink	Wakefield NF2D7
R1-R5, R10, R14, R16A-R16K, R17A-R17K, R18A-R18K, R19A-R19K, R43, R45	Resistor	2.2 K ohms, 1/4W, 5%
R6	Resistor	680 ohms, 1/2W, 5%
R7	Resistor	150 ohms, 1/2W, 5%
R8	Resistor	220 ohms, 1/2W, 5%

Table 6-27. (Cont'd.)

READ/WRITE AMPLIFIER ASSEMBLY PARTS LIST

Reference Designation	Description	Manufacturer and Part No.
R9, R15, R29, R30 R46, R47, R52	Resistor	1 K ohms, 1/4W, 5%
R11, R13	Resistor	33 K ohms, 1/4W, 5%
R12	Resistor	10 ohms, 1/2W, 5%
R20A-R20K, R21A-R21K, R23A-R23K, R24A-R24K, R31, R32, R36, R37	Resistor	4.7 K ohms, 1/4W, 5%
R22A-R22K	Resistor	47 K ohms, 1/4W, 5%
R25A-R25K, R40, R44	Resistor	10 K ohms, 1/4W, 5%
R26A-R26K, R42	Resistor	270 ohms, 1/4W, 5%
R27A-R27K	Resistor	220 K ohms, 1/4W, 5%
R28	Resistor	680 ohms, 1/4W, 5%
R33	Resistor	12 K ohms, 1/4W, 5%
R34	Resistor	430 ohms, 1/4W, 5%
R35, R55	Resistor	15 K ohms, 1/4W, 5%
R38, R39	Resistor	10 ohms, 1/4W, 5%
R41	Resistor	8.2 K ohms, 1/4W, 5%
R48	Resistor	820 ohms, 1/4W, 5%
R49	Resistor	18 K ohms, 1/4W, 5%
R50, R54	Resistor	390 ohms, 1W, 5%
R51	Resistor	100 ohms, 1/4W, 5%
R53	Resistor	47 ohms, 1W, 5%
Z1A-Z1K	Integrated Circuit	Fairchild uA702
Z2, Z3	Integrated Circuit	RCA CA3030
Z4, Z5	Integrated Circuit	Texas Instruments 7404N

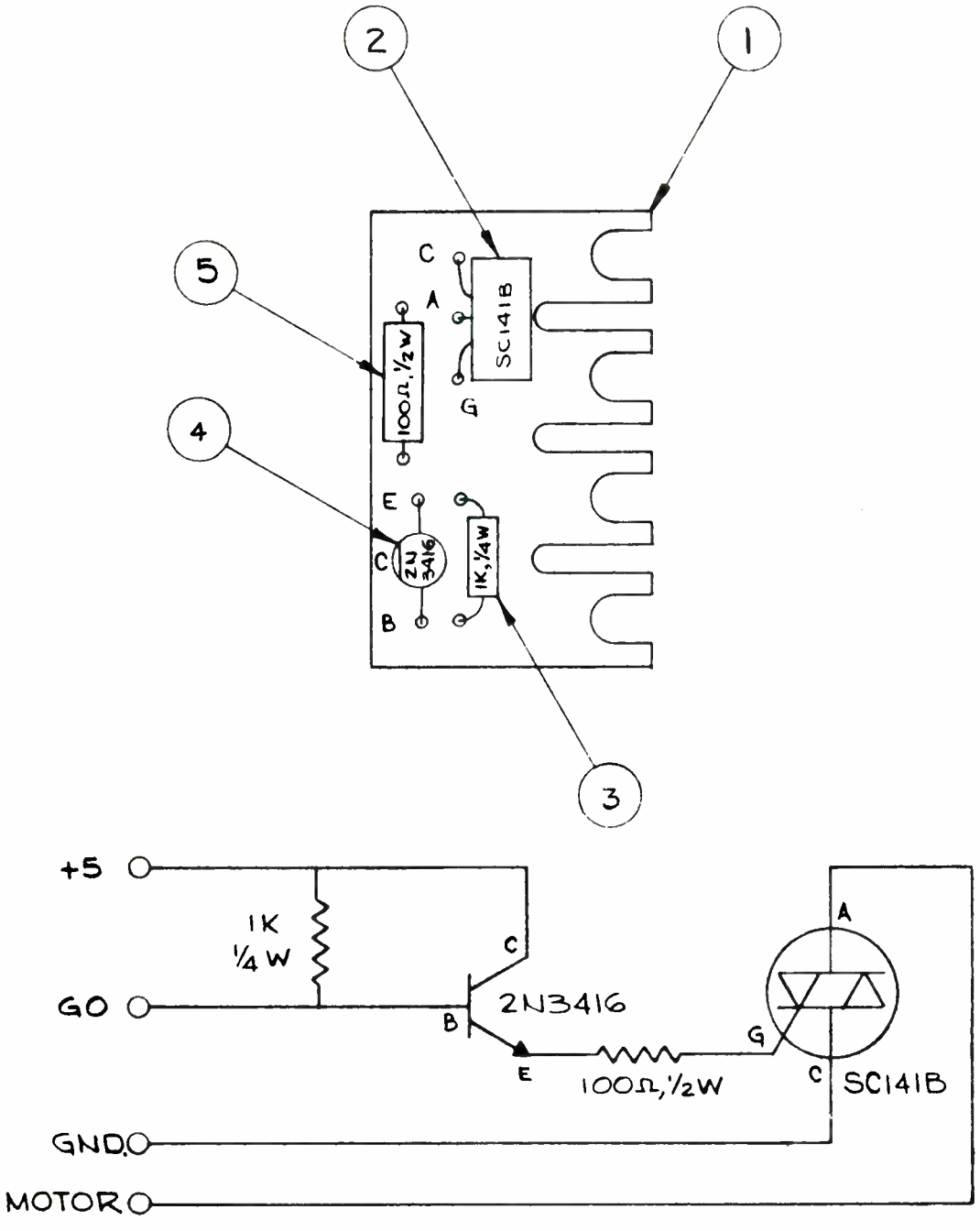


Figure 6-28. Motor Control Assembly.

Table 6-28.
MOTOR CONTROL ASSEMBLY PARTS LIST

Index No.	Description	Manufacturer	Part No.
1	Printed Circuit Board	Compat	2-473-0008-01
2	Triac	General Electric	SC141B
3	Resistor	1 K ohms, 1/4W, 5%	
4	Transistor	2N3416	
5	Resistor	100 ohms, 1/2W, 5%	