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BYTE

the small systems journal

In the Queue

BYTE March 1979
Volume 4, Number 3

Foreground

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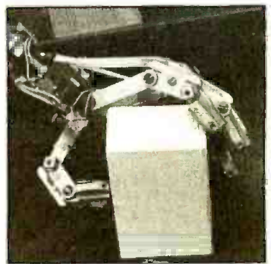

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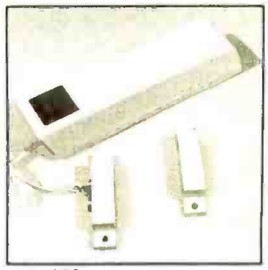

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Background

Nucleus

Cover Art:
THROUGH THE TRAP DOOR
by Robert Tinney.

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Editorial

Don't Overlook LISP

John R Allen
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Los Gatos CA 95030

*Most programming languages do very little to reinforce the creative process of algorithm discovery and creation. They are more concerned with the execution of already constructed algorithms. This month's guest editorial by John R Allen elaborates on this idea and discusses the relative merits of LISP, along with some general philosophy about personal computing. . . .*CPM

Pascal has reached critical mass; it has flashed through the mainframe, minicomputer, and now the microcomputer field. It has much to support its popularity; however, it represents but one point of view about computing.

This discussion offers a contrasting position, as "personified" by LISP. I will discuss not relative expressive power or syntax, but rather that the forces and attitudes which shaped the languages (and the kinds of problems which the languages address) represent diverse views of computation. In the 1969 Software Engineering Conference, Niklaus Wirth (creator of Pascal) said:

> *I would like to discuss the trend towards conversationality in our tools. There has been, since the development of timesharing and on line consoles, a very hectic trend towards development of systems which allow the interactive development of programs. Now this is certainly nice in a way, but it has its dangers, and I am particularly wary of them because this conversational usage has not only gained acceptance among software engineers but also in universities where students are trained in programming. My worry is that the facility of quick response leads to sloppy working habits and, since the students are going to be our future software engineers, this might be rather detrimental to the field as a whole.*

Wirth was addressing programming development in particular, but the question of "sloppy work habits" has a broader connotation. Many industrial and educational personnel still question the viability of interactive composition of any kind of text. Supposedly on line composition is wasteful and inefficient; one should carefully think out the text, writing it out in longhand or by typewriter, then revise and amend, cut and

Continued on page 212

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Articles which are accepted are purchased with a rate of up to $50 per magazine page, based on technical quality and suitability for BYTE's readership. Each month, the authors of the two leading articles in the reader poll (BYTE's Ongoing Monitor Box or "BOMB") are presented with bonus checks of $100 and $50. Unsolicited materials should be accompanied by full name and address, as well as return postage.■

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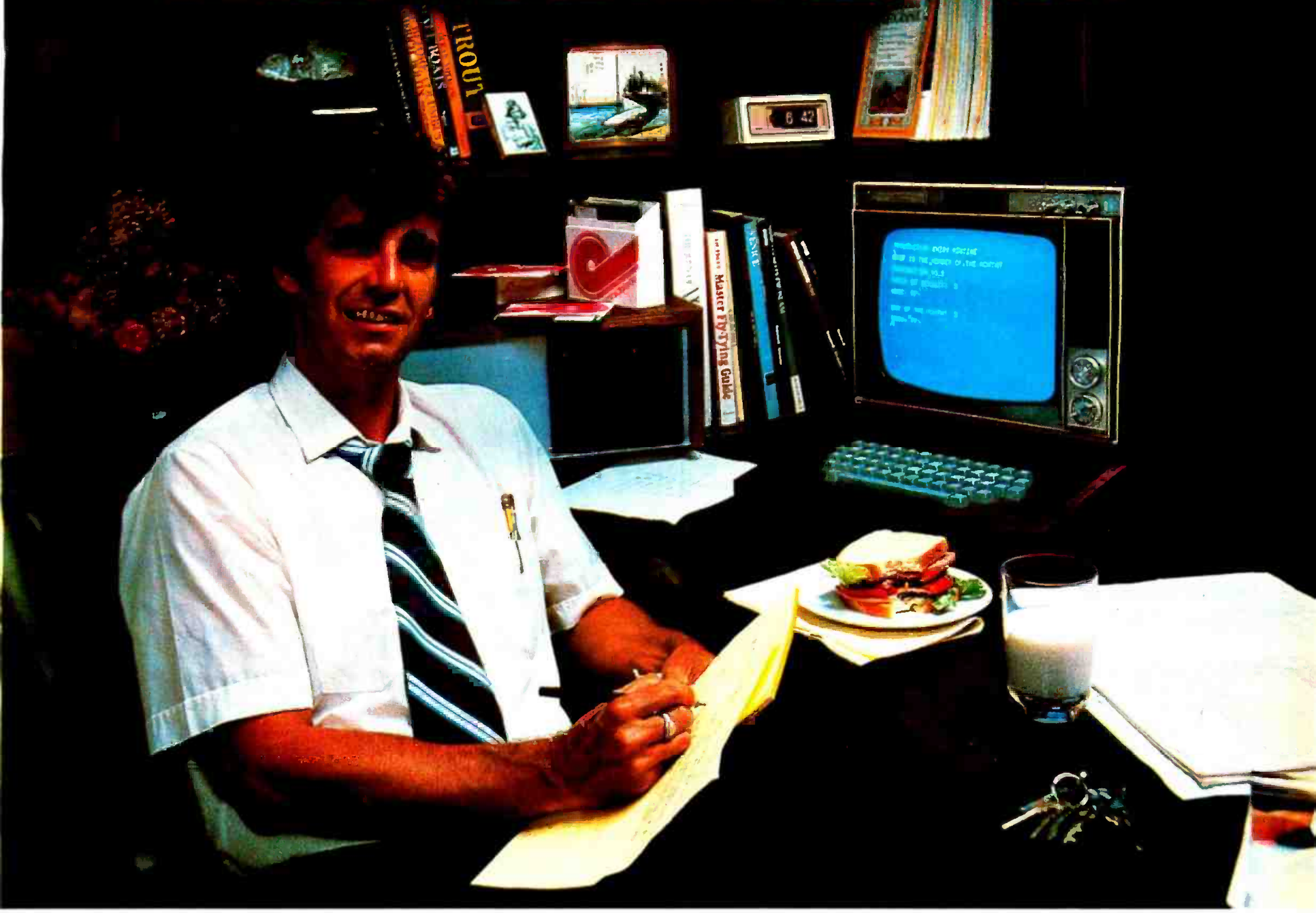

"After working all day with the computer at work, it's a kick to get down to Basic at home. And one thing that makes it more fun is my Shugart minifloppy™. We use Shugart drives at work, so when I bought my own system I made sure it had a minifloppy drive.

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For a list of manufacturers featuring Shugart's minifloppy in their systems, circle reader response number.

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*Both systems require a video monitor, modified TV or RF converter and home television for operation. Ohio Scientific offers the AC-3 combination 12" black and white TV/monitor for use with either system at $115.00 retail.

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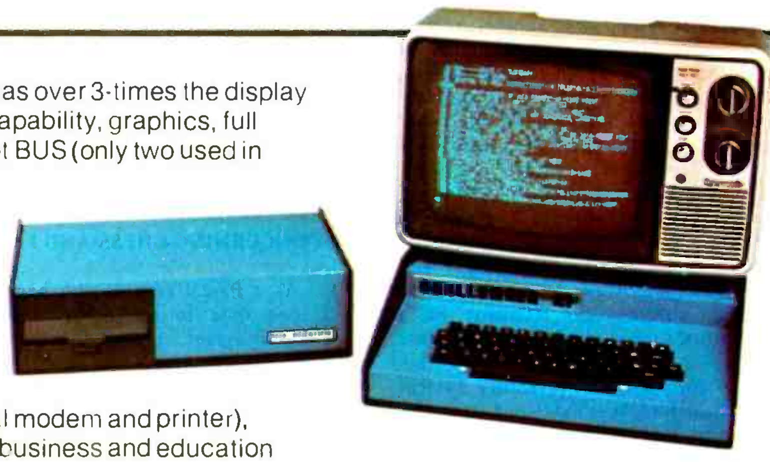

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Letters

OF KITCHENS AND COMPUTERS

As a data processing professional of twelve years experience, I have come to have great respect for the principle: "Don't make things more complicated than they are." In particular, this means don't put applications on a computer if they are more easily done some other way, no matter how much you like computers. I refer in particular to Richard Shuford's "Proposal for a Kitchen Inventory System, or Don't Byte the Wand that Feeds You" (December 1978 BYTE, page 184).

An automated food inventory and ordering system might be ideal for a restaurant. Feeding large numbers of people means ordering large amounts of food; the cost of running out of an item, or of overstocking perishables is relatively high. The home kitchen, on the other hand, deals with small quantities of a virtually unlimited number of items. Impulse buying is frequent, and will cause menus to change. The cost of mistakes is fairly small. Automatic reordering is fraught with danger — just when you *finally* use up the last can of cheddar cheese soup (bought in a moment of madness), *shazam;* four more appear.

My own kitchen inventory system works just fine. It is made out of a piece of paper from a legal pad, with the words CHOPIN LISZT (sorry about that) printed across the top, affixed to the door of my refrigerator with a bar magnet. The input device is a number two pencil.

There are thousands of applications which lend themselves to automation very well, and many where nothing else will do — but a computerized shopping list isn't one of them. For computers and computerists to gain the respect (and avoid the enmity) of the rest of the world, we need to be simplifiers, not complicators. So please, don't make things any more complicated than they are!

Bob Brown
Medical Association of Georgia
938 Peachtree St NE
Atlanta GA 30309

The kitchen inventory system may not be every family's cup of tea. My own buying habits are regular enough that the system may help; perhaps yours are not. Impulse purchases do not necessarily disrupt the system. The user may simply choose not to scan a product which is not to be restocked.

In a related communication, Mr Brown advises us that a reprint of "The Characteristics and Decodability of the Universal Product Code" which appeared in the IBM Systems Journal, *volume 14, number 1, is available as form G321-5002 for $0.50 from IBM's General Systems Division offices*. . . .RSS

COMPUTER HUMOR

Perhaps your readers will enjoy the following bit of doggerel. Every once in a while my husband Pat comes up with a good one like the one below:

Count Dracula's micro, it seems,
Would trouble his diurnal dreams.
What he felt was, you see,
Inferiority,
For it got all its bytes without screams.

Leah O'Connor
6315 W Raven
Chicago IL 60646

CONCERNING CHESS AND PASCAL

As a Pascal fanatic who had waited a long time to run across a readable chess program, I was thoroughly delighted to find that the excellent theoretical article "Creating a Chess Player" by Peter Frey and Larry Atkin (October 1978 BYTE, page 182) was to be followed by a complete Pascal listing that put the principles into practice. Having said that, may I be allowed to voice a few minor reservations?

First, although the authors are in general admirably clear about separating machine dependent and machine independent code, I feel they should have made clear that the contorted treatment of bit boards results from a machine dependent implementation restriction: in CDC Pascal, sets may not have more than 59 elements, so that a bit board must be represented as two sets of 32 elements. Other implementations, such as UCSD Pascal, do not have this restriction, so that the bit board manipulations which form the backbone of the program may be represented much more naturally. Thus, IORRS (INRS, INRS, IMRS) could become simply INRS := INRS + IMRS.

Secondly, I find that the program does not exploit Pascal's self-documenting potential as much as it might, because the authors chose a cryptic naming convention instead of using mnemonics. After ten hours of intensive study,

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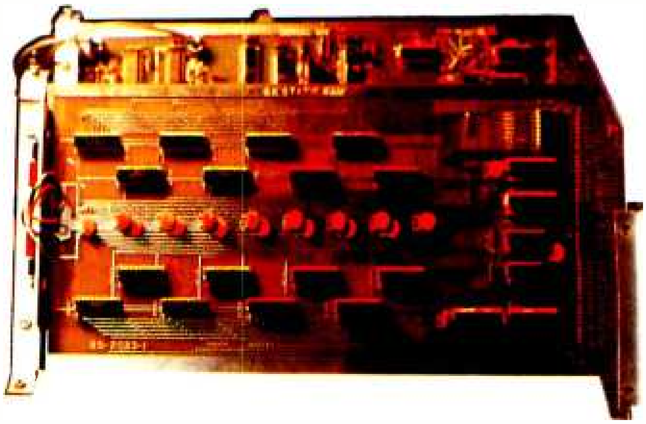

Photo 1: The H8 programmable memory board.

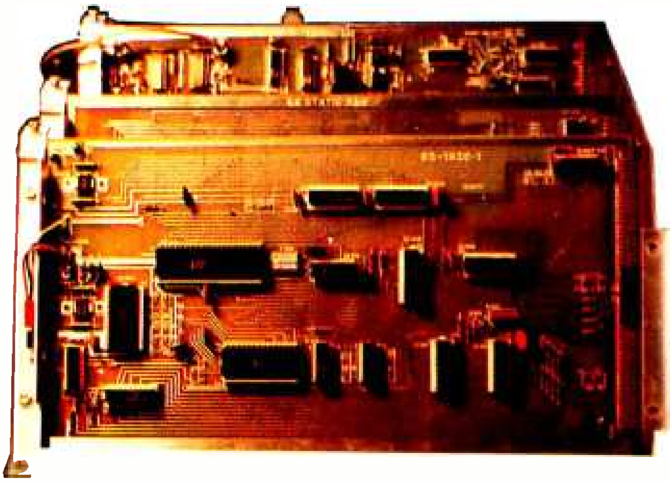

Photo 2: The H8 processor board in position in the chassis.

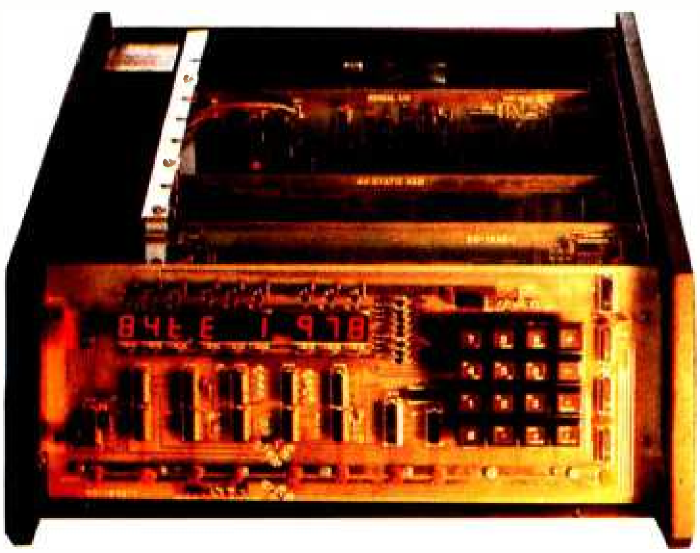

Photo 3: Assembled H8 ready for testing.

Building

Dr Paul R Poduska
21G Hampshire Dr
Nashua NH 03060

In response to growing public interest in microcomputing during the past several years, a number of microcomputer kits have been marketed.

The Heathkit H8 microcomputer represents a departure from the S-100 bus design mainstream. It has the full instruction set capabilities of other 8080A systems as well as an innovative, user oriented front panel control subsystem and a 10 position mother board; yet it does not use the type of large power supply found in some larger systems.

It was the kind of design I was hoping for. I was seriously considering the purchase of a computer for some time, and prior to the introduction of the H8, I almost did buy one. But I had a hunch that the Heath Company might resolve some of the design drawbacks that discouraged me from buying other 8 bit kits.

What follows are my experiences, thus far, of building, testing, and running this computer kit. By the time you've finished reading this article you should have a good feel for what the H8 is, what it can do, and how it compares with other kits on the market. In addition, I'll give you a few pointers and short programs that will enable you to take advantage of some of the H8's many features.

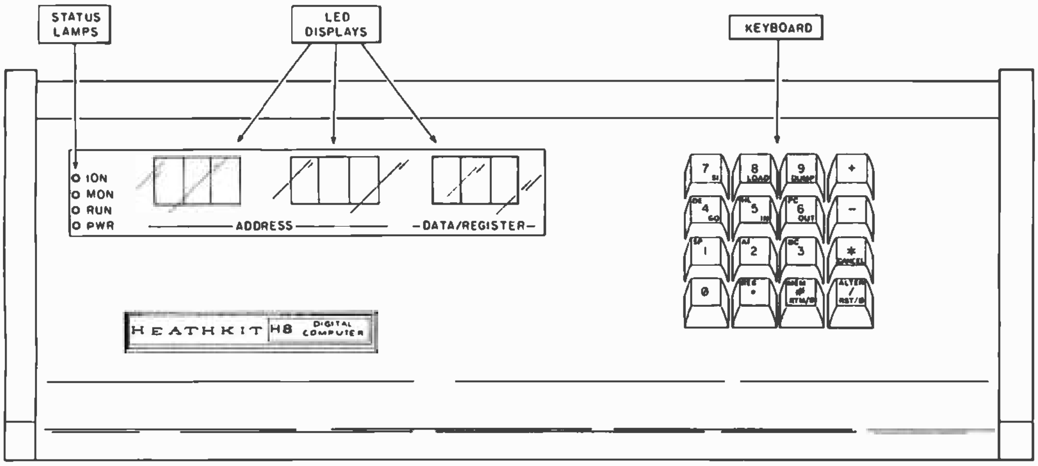

Figure 1: The Heath H8 front panel. Many of the 16 keys are multifunctional. The panel allows quick entry of data and programs into the computer. Drawn from a diagram courtesy of Heath Company.

the Heath H8 Computer

Unpacking and Building

My first few evenings with the H8 kit were leisurely spent getting acquainted with the materials and manuals. Opening the 22 lb carton, the first thing that caught my eyes was a loose slip of paper with a notice on it. It warned me to review all of the manuals supplied with the kit before putting anything together, and that if I found it to be too complicated for my knowledge and skill level, I could return it to the Heath Company for a full refund. I know of no other computer kit manufacturer who includes that kind of built-in consumer protection from the outset.

The next items were the sets of manuals and an attractive 3 ring binder to store them in. I had assembled Heathkits before and knew how thorough their documentation has always been; and I had seen some mediocre documentation provided by other companies in the computer kit industry. I found 503 pages worth of assembly and operating manuals which were far superior to any that I had seen on the market.

In all fairness, I don't feel that this point can be overemphasized. Building a microcomputer is not like building a stereo or piece of test equipment. The technology and associated hardware of a computer are unique in many ways. You may have assembled and tested electronic kits before, but unless you've also assembled digital equipment, you probably won't be an expert on this type of hardware. If you ever need to troubleshoot your computer kit, much of your previous knowledge about *conventional* analog electronics won't be of use. Therefore, *it is important that you know what you are assembling and how to do so correctly.* You don't have to be an electronics wizard to build and operate the H8. Your chances of building a computer kit that works the first time you turn on the power are nearly 100 percent with an H8, due in part to the support services that the manufacturer provides.

After the first few evenings of studying the manuals, I found a reasonably undisturbed space and, with tools in hand, began the first stage of assembly.

The Chassis

Chassis assembly consists of installing the power supply, frame, and several accessories, including a small cone speaker. The frame is made out of heavy sheet metal on the top, bottom and back panel, and structured foam on the sides. The bottom is covered with rows of small holes necessary for the H8's convection cooling system. The ample 10 A power supply is located

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A Map of the TMS-9900 Instruction Space

Henry Melton
2511 Dovemeadow
Austin TX 78744

Organizing One's Approach to a Machine with $2^{15.95}$ Legal Instructions

Now that the TMS-9900 16 bit computer is being marketed to the computer experimenter, some easy way to handle its 63,480 individual op codes at a level of "hand assembly" is going to be necessary. The standard method of programming the 16 bit machine involves higher level languages, or at the very least, a good symbolic assembler. The op codes of an 8 bit machine are smaller in number and can be fairly easily memorized by a machine level programmer confined to the limited resources of hand assembly. But nearly every instruction on the TMS-9900 has to be *constructed*, calculated from the instruction's format, depending on the selected options of the moment. That is the essence of the machine's power, but it makes building and analyzing programs at a machine language level difficult. The charts in this article should help simplify the matter.

The first of the op code maps (figure 1) is an expansion of the first byte of a 16 bit instruction. The second map (figure 2) is a detail of the first rank of figure 1. Notice that the most significant digits of the op codes go down and the least significant digits go across the charts. Each block contains the mnemonic of the instruction, the format type of that instruction, and the number of variations (ie: the number of different instructions that the mnemonic represents).

For example, the instruction MOV, for MOVE WORD, has a source and a destination word address, with one of four addressing codes for each, referenced to one of the 16 registers in the workspace for each. That gives 16 times 4 times 16 times 4, or 4096 possible individual instructions. Let's take a specific example. Suppose you come across a C835 instruction in a hexadecimal program dump. You look up that code on the op code space map (figure 1 in this case). It lies in the block for instruction MOV, with an instruction format of I. Comparing C835 with format I in table 1, you find that:

Base op code	=	1100.
Address mode of destination	=	10.
Destination operand register	=	0000.
Address mode of source	=	11.
Source operand register	=	0101.

Since the destination is indexed, the word following the C835 is an address, and thus part of the instruction. The index register, however, is 0000 and the zero register isn't allowed for index mode. Thus the following address *is* the destination address without address modification. If it had been one of the other registers, the following word would have been *added* to the register value to form the indexed address. The addressing mode for the source is register 5, indirect and autoincremented. The source operand's address is in register 5. Once the operand is fetched, the address value in register 5 is incremented by 2 (since it was a word instruction and the 9900 addresses specify *bytes*). Thus the end result of the instruction is that this source operand is moved to the immediate address specified by the word following C835.

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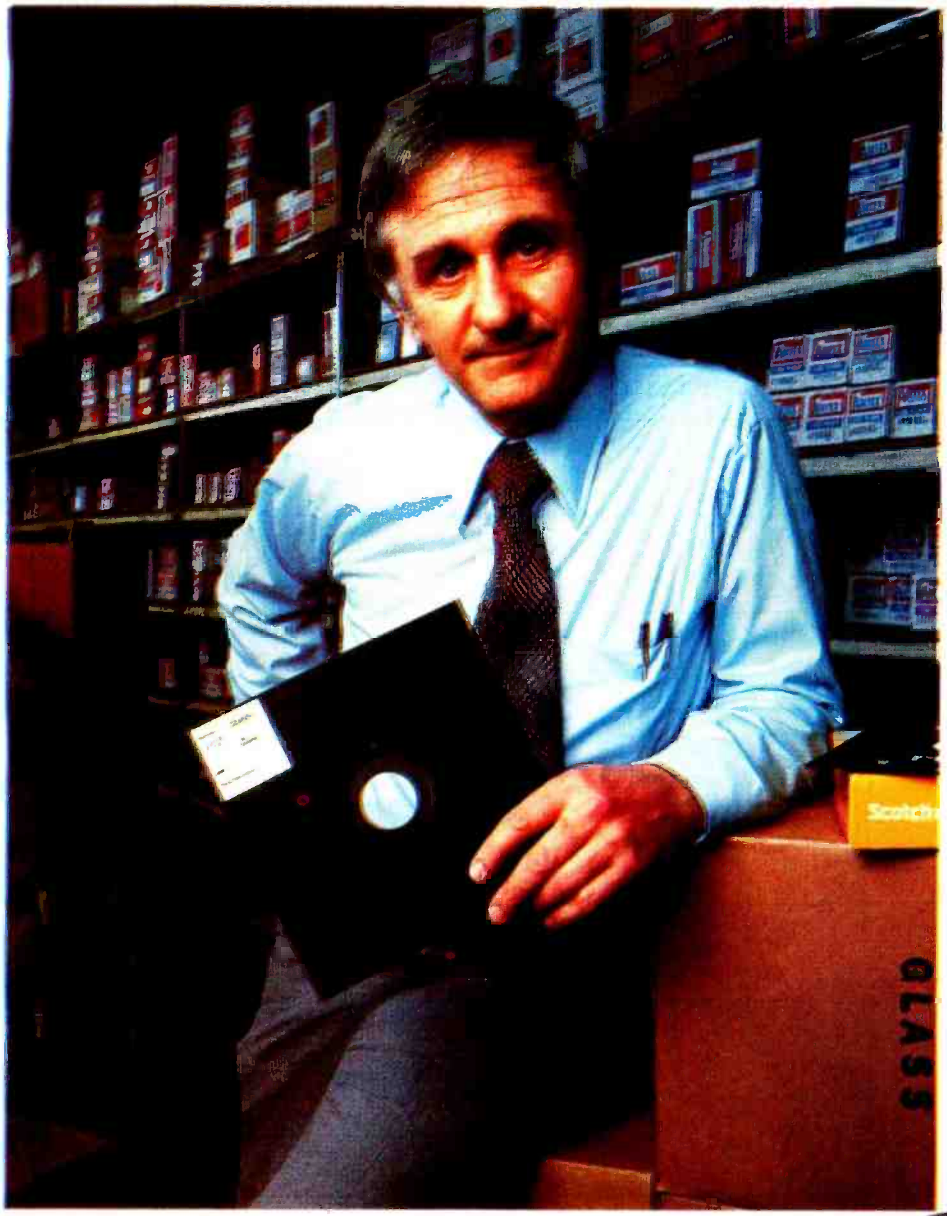

Don Stone, Vice-President, Mass. Auto Supply Company, Inc., Boston, Mass.

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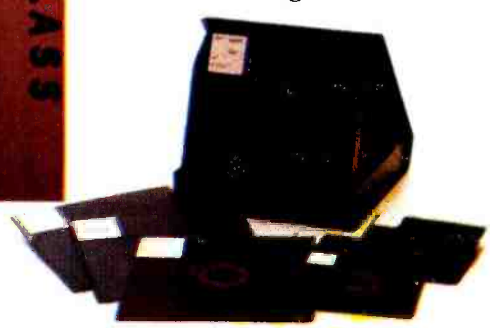

3M

Key

JLE	–	Mnemonic
II	–	Tape
256	–	Number of possible op codes

Figure 1: General map of all TMS-9900 instructions. This map covers operation codes from 00XX to FFXX hexadecimal, with reference to the detail of table 2 for op codes from 00XX to 0FXX. In interpreting a machine dump in hexadecimal, the first step is to look up a 2 byte operation code in this table, or in figure 2.

	0XX	1XX	2XX	3XX	4XX	5XX	6XX	7XX	8XX	9XX	AXX	BXX	CXX	DXX	EXX	FXX
0	See figure 2															
1	JMP II 256	JLT II 256	JLE II 256	JEQ II 256	JHE II 256	JGT II 256	JNE II 256	JNC II 256	JOC II 256	JNO II 256	JL II 256	JH II 256	JOP II 256	SBO II 256	SBZ II 256	TB II 256
2	COC III 1024				CZC III 1024				XOR III 1024				XOP IX 1024			
3	LDCR IV 1024				STCR IV 1024				MPY IX 1024				DIV IX 1024			
4	SZC I 4096															
5	SCZB I 4096															
6	S I 4096															
7	SB I 4096															
8	C I 4096															
9	CB I 4096															
A	A I 4096															
B	AB I 4096															
C	MOV I 4096															
D	MOVB I 4096															
E	SOC I 4096															
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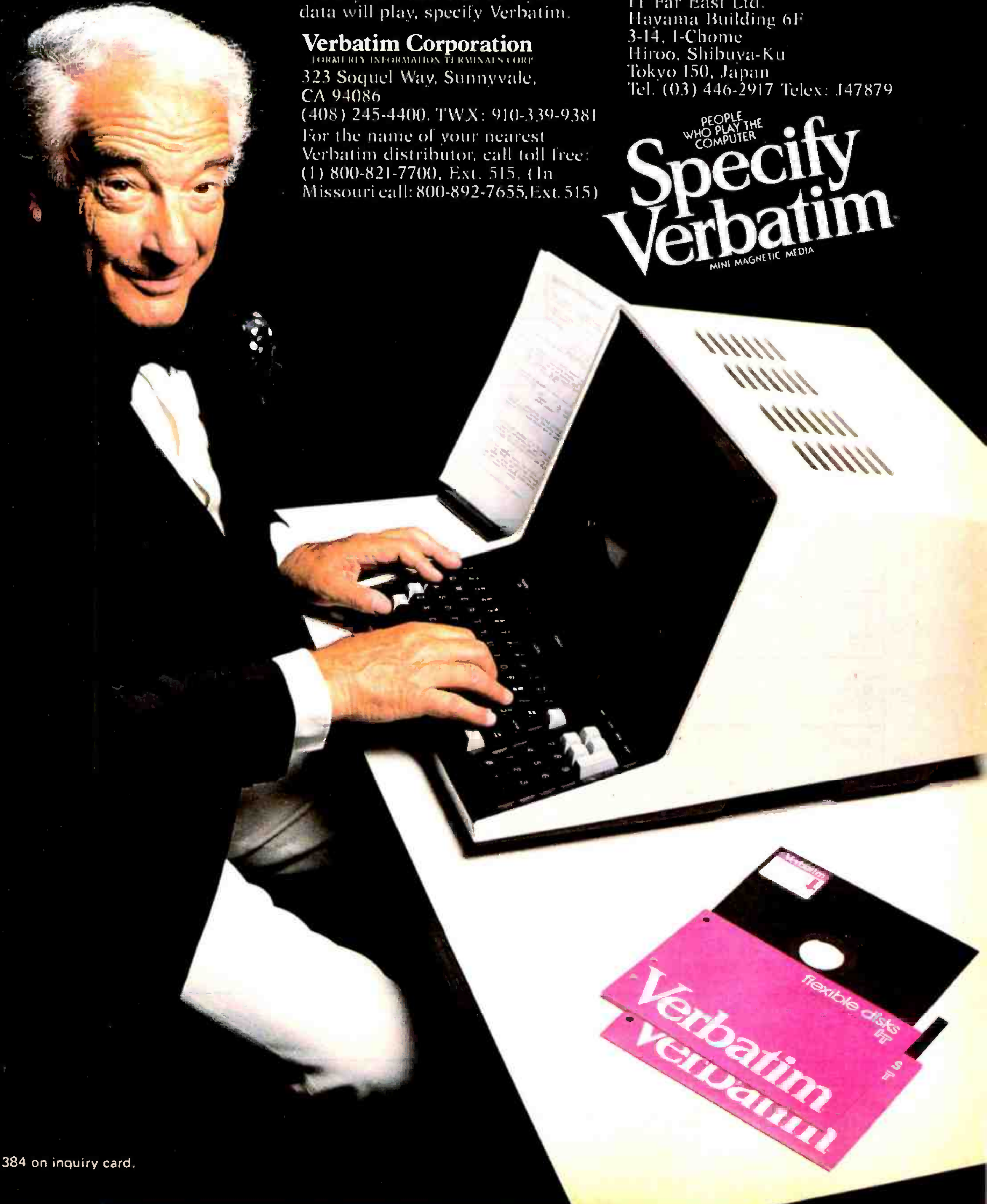

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Figure 2: For operation codes 00XX to 0FXX, the details of interpreting a hexadecimal dump can be further understood with the aid of this map. Once the format is determined, refer to table 1 for details of formats V, VI, VII and VIII.

	0X	1X	2X	3X	4X	5X	6X	7X	8X	9X	AX	BX	CX	DX	EX	FX
00	Illegal op codes															
01	Illegal op codes															
02	LI VIII 16		AI VIII 16		ANDI VIII 16		ORI VIII 16		CI VIII 16		STWP VIII 16		STST VIII 16		LWPI VIII 1	
03	LIMI VIII 1				IDLE VII 1		RSET VII 1		RTWP VII 1		CKON VII 1		CKOF VII 1		LREX VII 1	
04	BLWP VI 64				B VI 64				X VI 64				CLR VI 64			
05	NEG VI 64				INV VI 64				INC VI 64				INCT VI 64			
06	DEC VI 64				DECT VI 64				BL VI 64				SWPB VI 64			
07	SETO VI 64				ABS VI 64				Illegal op codes							
08	SRA V 256															
09	SRL V 256															
0A	SLA V 256															
0B	SRC V 256															
0C	Illegal op codes															
0D	Illegal op codes															
0E	Illegal op codes															
0F	Illegal op codes															

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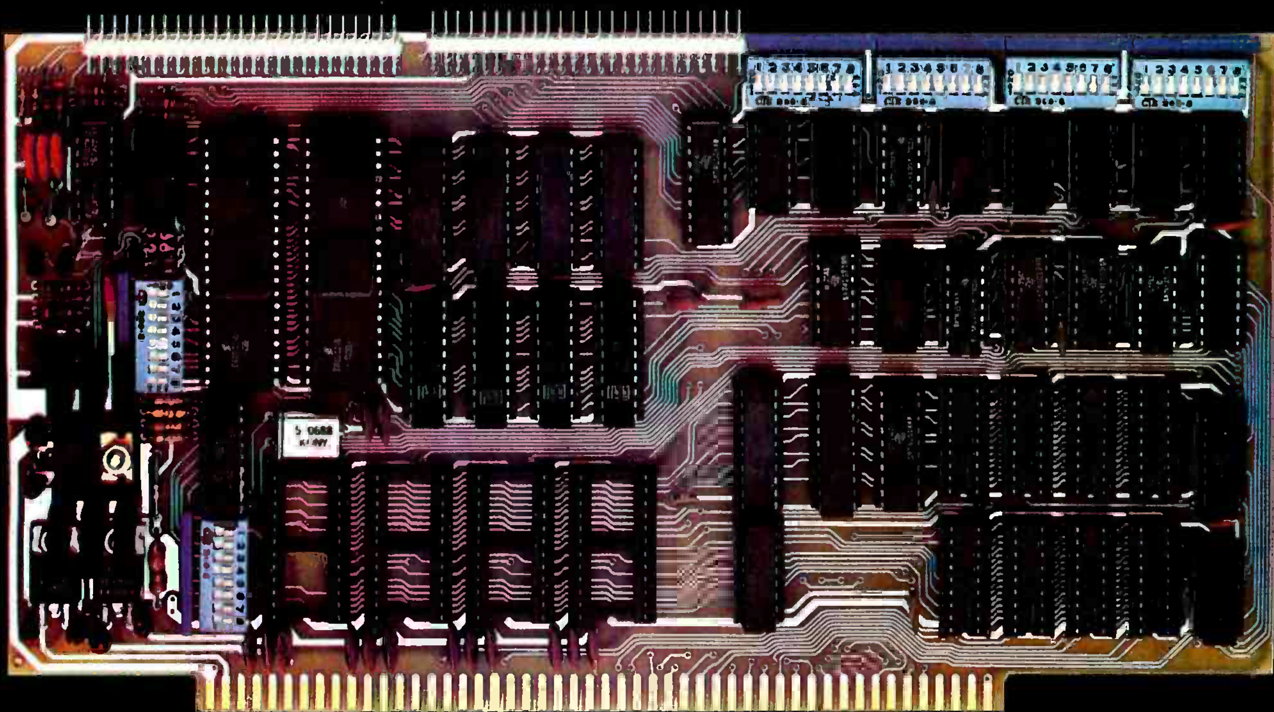

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Table 1: *Instruction formats of the TMS-9900. This table details the fields of the TMS-9900 instructions and is used in decoding a machine dump once the instruction type has been determined from the two maps of tables 1 and 2.*

Bit Number

Type	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	Number
I	Op code			B	Td		D				Ts		S				4096
II	Op code								Displacement								256
III	Op code						D				Ts		S				1024
IV	Op code						C				Ts		S				1024
V	Op code								K				W				256
VI	Op code										Ts		S				64
VII	Op code											N					1
VIII	Op code											N	W				1 or 16
IX	Op code						D				Ts		S				1024

B — Byte or word operation (1=byte)
D — Destination operand register
S — Source operand register
W — Workspace register
Td — Address mode of destination operand
Ts — Address mode of source operand
C, K — Bit or shift count
N — Unused bits of the instruction. Set to zero.

Address Modes

Td or Ts

00 Workspace register
01 Workspace register indirect
10 Indexed memory
11 Workspace register indirect, autoincrement

Hexadecimal modifiers for the Td (format I) and Ts (formats I, III, IV, VI and IX) fields. To generate an operation code reflecting the given addressing mode, add the hexadecimal values listed in this table:

Addressing Mode	Td	Ts
Workspace register	0000	0000
Workspace register indirect	0400	0010
Indexed memory (symbolic)	0800	0020
Workspace register indirect with autoincrement	0C00	0030

Shifted register or count values for D (formats I, III and IX), C (format IV) and K (format V) fields. In constructing operation codes for these formats, the modifiers for the register or count values indicated are added to the base op code from table 4:

Register or Count	D (C)	K
0	0000	0000
1	0040	0010
2	0080	0020
3	00C0	0030
4	0100	0040
5	0140	0050
6	0180	0060
7	01C0	0070
8	0200	0080
9	0240	0090
10	0280	00A0
11	02C0	00B0
12	0300	00C0
13	0340	00D0
14	0380	00E0
15	03C0	00F0

Table 2: Going the other way; this list of the complete TMS-9900 instruction set shows the format and semantics of each operation possible with the machine. The base operation code, in hexadecimal, is modified by arithmetic addition of appropriate codes for details of the instruction as shown in table 1. Thus for example, to generate the code for comparing bytes between two absolute memory addresses this table gives a base op code of 9000 with format I. For the destination address field, a modifier of 800 is added, and for the source address field a modifier of 020 is added, yielding a net instruction value of 9820 for comparing two bytes at arbitrary memory addresses. Information for this table is taken from appendix E of the January 1976 reissue of the TI Model 990 Computer and TMS-9900 Microprocessor Assembly Language Programmer's Guide, *document manual number 943441-9701, eliminating operations not applicable to the TMS-9900.*■

TMS-9900 Alphabetical Instruction List

Mnemonic	Format	Hexadecimal Base Op Code	Semantics
A	I	A000	Add words
AB	I	B000	Add bytes
ABS	VI	0740	Absolute value
AI	VIII	0220	Add immediate
ANDI	VIII	0240	AND immediate
B	VI	0440	Branch
BL	VI	0680	Branch and link
BLWP	VI	0400	Branch and load workspace pointer
C	I	8000	Compare words
CB	I	9000	Compare bytes
CI	VIII	0280	Compare immediate
CKOF	VII	03C0	Clock off
CKON	VII	03A0	Clock on
CLR	VI	04C0	Clear operand
COC	III	2000	Compare ones corresponding
CZC	III	2400	Compare zeros corresponding
DEC	VI	0600	Decrement by one
DECT	VI	0640	Decrement by two
DIV	IX	3C00	Divide
IDLE	VII	0340	Computer idle (ie: no operation)
INC	VI	0580	Increment by one
INCT	VI	05C0	Increment by two
INV	VI	0540	Invert
JEQ	II	1300	Jump if equal
JGT	II	1500	Jump if greater than
JH	II	1B00	Jump if high
JHE	II	1400	Jump if high or equal
JL	II	1A00	Jump if low
JLE	II	1200	Jump if low or equal
JLT	II	1100	Jump if less than
JMP	II	1000	Jump unconditional
JNC	II	1700	Jump if carry off
JNE	II	1600	Jump if not equal
JNO	II	1900	Jump if no overflow
JOC	II	1800	Jump if carry on
JOP	II	1C00	Jump if odd parity
LDCR	IV	3000	Load communication register
LI	VIII	0200	Load immediate
LIMI	VIII	0300	Load interrupt mask immediate
LREX	VII	03E0	Load or restart execution
LWPI	VIII	02E0	Load workspace pointer immediate
MOV	I	C000	Move word
MOVB	I	D000	Move byte
MPY	IX	3800	Multiply
NEG	VI	0500	Negate
ORI	VIII	0260	OR immediate
RSET	VII	0360	Computer reset
RTWP	VII	0380	Return with workspace pointer
S	I	6000	Subtract word
SB	I	7000	Subtract byte
SBO	II	1D00	Set CRU bit to one
SBZ	II	1E00	Set CRU bit to zero
SETO	VI	0700	Set word to ones (FFFF)
SLA	V	0A00	Shift left arithmetic
SOC	I	E000	Set ones corresponding, word (OR)
SOCB	I	F000	Set ones corresponding, byte (OR)
SRA	V	0800	Shift right arithmetic
SRC	V	0B00	Shift right circular
SRL	V	0900	Shift right logical
STCR	IV	3400	Store communication register
STST	VIII	02C0	Store status
STWP	VIII	02A0	Store workspace pointer
SWPB	VI	06C0	Swap bytes
SZC	I	4000	Set zeros corresponding, word ($\overline{S}$ AND D)
SZCB	I	5000	Set zeros corresponding, byte ($\overline{S}$ AND D)
TB	II	1F00	Test CRU bit
X	VI	0480	Execute word as an instruction
XOP	IX	2C00	Invoke extended operation
XOR	III	2800	Exclusive OR

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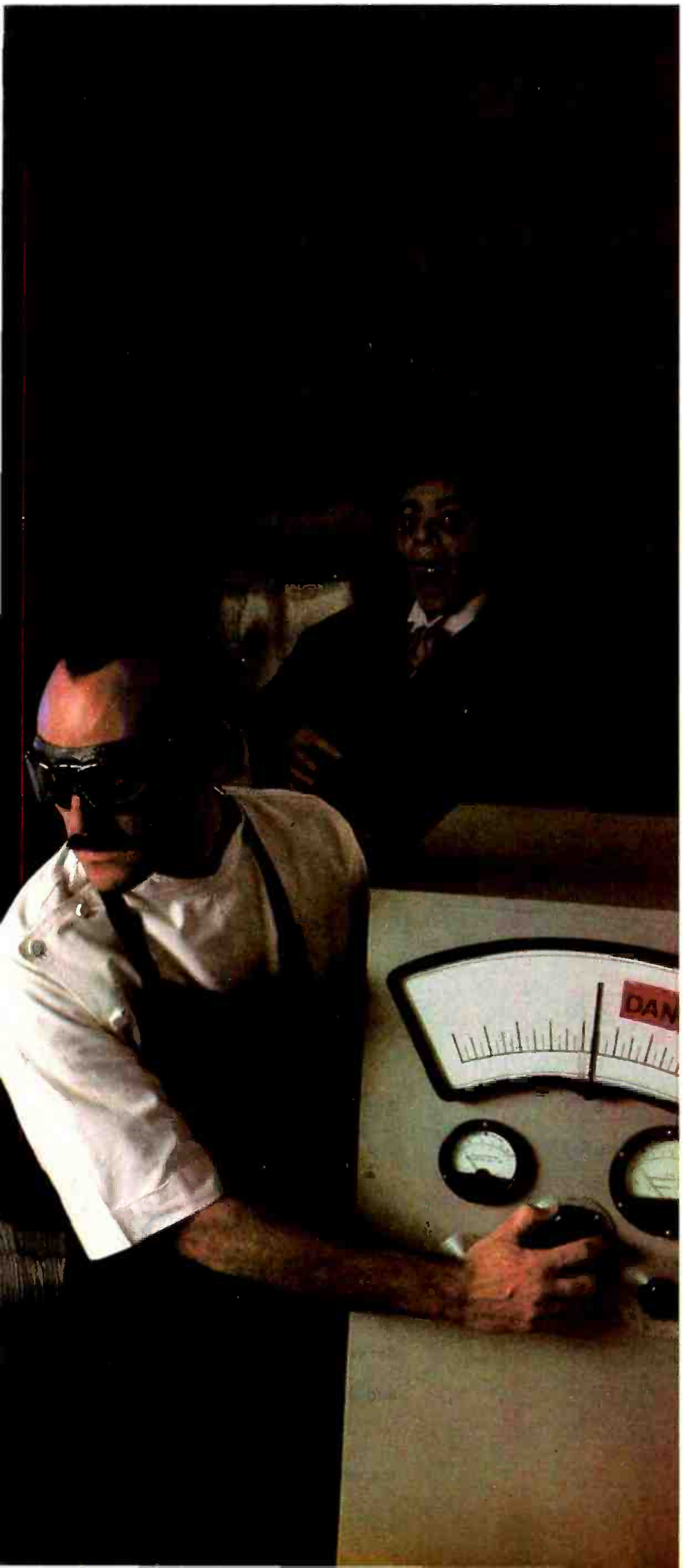

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Race Car for the SR-52

Race Car is a game of skill written for the Texas Instruments SR-52 programmable calculator, in which the player maneuvers a car around a race track drawn on graph paper. The object of the game is to drive the car from the start to the finish line in the best possible time without leaving the track. The program calculates the coordinates of the car based on steering, throttle and brake information entered by the driver. Players can choose to go left, straight or right (relative to the driver's seat), and to accelerate, brake or cruise. Each time the player makes a move, 1 second of time elapses.

For each move, the program calculates the X and Y coordinates of the car's new position and the elapsed time. The player simply plots the car's position and makes the new move based on the present position. Using different colored pens, two or more players can race on the same track and compete for the best finishing time.

The program moves the coordinates of the car during the 1 second time interval based on a velocity vector constructed by the player's decisions. Left and right steering increments are fixed at +15° and −15°, respectively. For example, if you go left, the velocity vector is rotated +15° from its present direction. The acceleration and deceleration constants are +1 division per second^2 and −1 division per second^2. If you wish to accelerate, the magnitude of the velocity vector is increased by one and the distance traveled during that move will be one division farther than the previous move. If you decide to cruise, the magnitude of the velocity vector remains constant and the distance traveled during that move will be the same as the previous move.

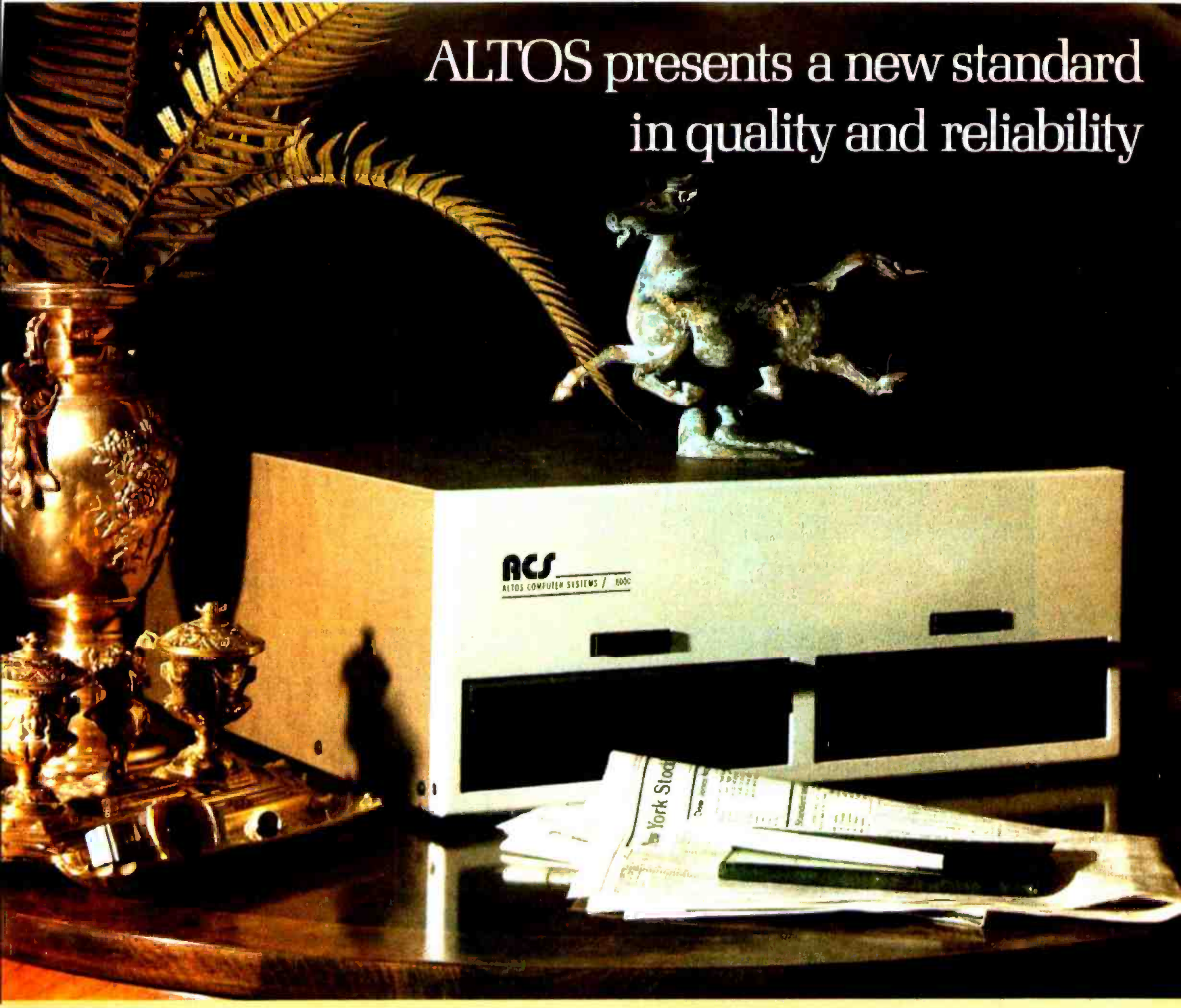
Text continued on page 30

Listing 1: The Race Car program, written for the SR-52.

Loc	Keys						Commentary
000	*LBL	*C'	STO	0	1		Store XX.YY.
005	INV	*D.MS	INV	*D.MS	*fix	0	Mask off YY and store XX.
011		*D.MS	INV	*fix			
014		STO	0	3			
017	+/–	+	RCL	0	1	=	Get XX.YY, mask off XX
023		x	1	0	0	=	and store YY.
028		STO	0	4	0	HLT	
033	*LBL	*D'	STO	0	5		Store the starting angle.
038		0	INV	*fix	HLT		
042	*LBL	*E'	RCL	0	3		Initialize X position.
047		STO	0	6			
050	RCL	0	4	STO	0	7	Initialize Y position.
056	RCL	0	5	STO	0	8	Initialize velocity angle.
062	0	STO	0	9			Set velocity magnitude
066		STO	1	0			and elapsed time = 0.
069	GTO	*A'					
071	*LBL	A	1	5			Increment velocity angle

Listing 1, continued:

Loc	Keys						Commentary
075		SUM	0	8			by 15 degrees for left turn.
078		0	INV	*fix	HLT		
082	*LBL	B	1	5	INV		Decrement velocity angle
087		SUM	0	8			by 15 degrees for right turn.
090		0	INV	*fix	HLT		
094	*LBL	D					Increment velocity magnitude
096	1	SUM	0	9	GTO	C	by 1 for acceleration.
102	*LBL	E					Decrement velocity magnitude
104	1	INV	SUM	0	9		by 1 for brake.
109	*LBL	C	1	SUM	1	0	Increment elapsed time.
115	RCL	0	9	STO	0	0	Convert velocity vector
121		RCL	0	8	*P/R		to rectangular coordinates.
125	SUM	0	7	RCL	0	0	Readjust X and Y coordinates.
131		SUM	0	6			
134	*LBL	*A'	RCL	0	7		Convert Y coordinate to
139		SBR	*1'	STO	1	1	integer value.
144	RCL	0	6				Convert X coordinate to
147		SBR	*1'				integer value.
149	+	.	0	1	x		Combine X and Y coordinate
154		RCL	1	1	+	.	and elapse time and
159		0	0	0	0	1	display result.
164		x	RCL	1	0	=	
169		*fix	5	HLT			
172	*LBL	*B'	RCL	0	9	=	Display magnitude of
178		INV	*fix	HLT			velocity vector.
181	*LBL	*1'	STO	0	1		Subroutine to convert
186		INV	*D.MS	INV	*D.MS		real number to integer form.
190	*fix	0	*D.MS				Mask off fractional part
193		INV	*fix	STO	0	2	of real number to convert
198		+/–	+	RCL	0	1	to integer.
203		=					
204	–	.	5	=	*ifpos	*2'	If fractional part of
210		RCL	0	2	*rtn		real number is greater than
214	*LBL	*2'	RCL	0	2		0.5, then add 1 to integer
219	+	1	=	*rtn			value.



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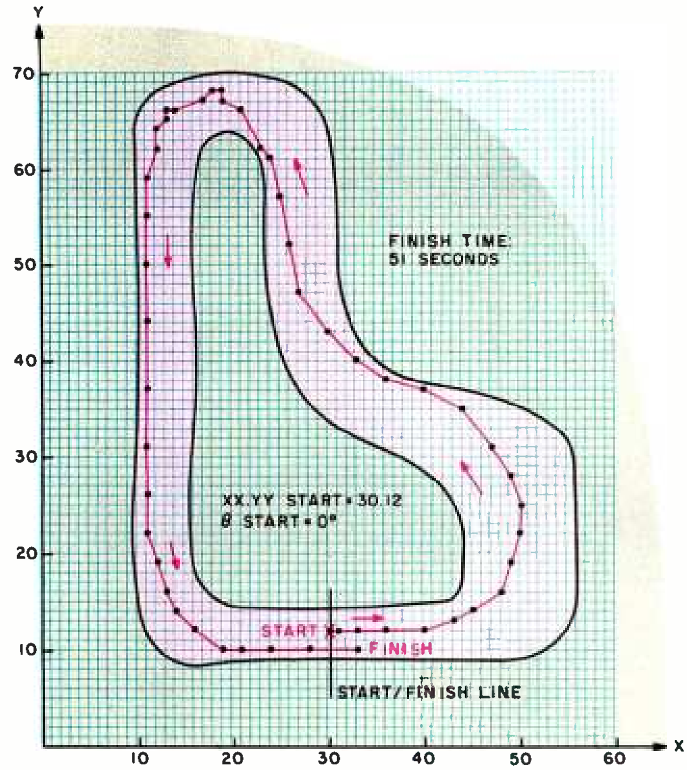

Figure 1: A typical route for one player in the game of Race Car, written for the Texas Instruments SR-52 programmable calculator. Players must stay within the bounds of the track (which is arbitrarily drawn on graph paper) or risk disqualification. Increments of change to acceleration and steering are deliberately restricted in order to make the game more challenging, but players have free choices within these limitations.

Text continued from page 26

Remember that you are steering the race car as if you were sitting in the driver's seat, so don't confuse your left and right directions. The degree of difficulty can also be set in the layout of the race track. Hairpin turns and straightaways will test your skill and make the game exciting. I've had hours of fun racing with my friends and family; I hope you will, too.■

User Accessible Labels:

A = Left	A' = X.YT
B = Right	B' = Vel
C = Cruise	C' = X.Y Start
D = Accel	D' = θ Start
E = Brake	E' = Init

Register Utilization:

00 = P/R conversion
01 = Work area
02 = Work area
03 = Initial X coordinate
04 = Initial Y coordinate
05 = Initial veclocity angle
06 = X coordinate
07 = Y coordinate
08 = Angle of velocity vector
09 = Magnitude of velocity vector
10 = Elapsed time
11 = Work area
12 = Work area

Race Car Operating Instructions

1. Draw the race track on a suitable piece of graph paper, preferably ten divisions to the inch. Figure 1 shows an example of a typical race track. The race track must be located in the area bound by the lines X=0, X=100, Y=0 and Y=100. It is a good idea to leave space between the edge of the race track and the boundaries, since the car might leave the track. Select the combination start and finish line on the track and the initial direction of the car.
2. Enter sides A and B of the program.
3. Set the D/R switch to D.
4. Enter the starting coordinates of the car in the form XX.YY, where XX is the initial X coordinate and YY is the initial Y coordinate. Both numbers must be positive integers between 0 and 100. Press *C'.
5. Enter the initial direction of the car. This is a positive angle in degrees measured from the positive X axis to the initial direction of the car. This angle should equal n x 15°, where n = 0, 1, 2, 3, . . . , 23. Press *D'.
6. Press *E' to initialize the game. The initial X and Y coordinates will be displayed in the form XX.YY000.
7. Select the direction in which you will steer the car.

   Press A to steer left. Zero will be displayed.
   Press B to steer right. Zero will be displayed.

   If you want to go straight, skip this step and proceed to step 8.
8. Select the throttle and brake conditions.

   Press C to cruise.
   Press D to accelerate.
   Press E to brake.

   The position of the car and the elapsed time will be displayed in the form XX.YYTTT, where:

   XX = X coordinate of the car.
   YY = Y coordinate of the car.
   TTT = Elapsed time in seconds.
9. Repeat steps 7 and 8 for each move. If the car should leave the track, the player is disqualified. Once the car passes the finish line, the winning time is read from the display.
10. To display the magnitude of the velocity vector, press *B'. To return the display back to XX.YYTTT, press *A'.
11. To play a new game on the same race track, press *E'.

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Part 2: Using Files

File Management

In part 1 we discussed the concept of the file. In part 2 we conclude with some practical techniques for using files.

Getting a list of the files on your system is a task you probably perform often. Table 6 is a sample directory (which also appeared in part 1 as table 4a). Notice the command string used to produce the table just above the directory itself. In table 6 the first asterisk is the *prompt*, the computer's signal to enter a command. The letter Q is the Query command, used to produce file directories. The next asterisk is a *wild card* name instead of the file name: it means "give me (a list of) all the files on this device." Finally there is a software switch, /1, specifying floppy disk drive number 1.

Depending on the operating system, wild card characters can also be used. The PerSci controller, for example, allows a command string like:

Q FIL???.MPK/1

which means:

> List [Q] all files on drive number 1 whose extension (version) is MPK, and whose file name begins with the letters FIL, regardless of what the next few letters are.

This article was produced on a text editor and for convenience the different parts were given different file names: FILFIG.MPK held the list of figures; FILCAP.MPK held the figure captions; FILAR1, FILAR2, etc, held text proper. The extension .MPK identified the files as belonging to me. Thus the command string above would produce a directory listing of all files holding parts of this article.

Using Defaults

If parts of a command string are omitted the operating system automatically inserts a proper type of specification chosen from a preprogrammed list. This preprogrammed list is called the system default specification or just defaults. If the /I is left off the microcomputer command string in table 6, that system would automatically search for the files on floppy disk drive 0, which happened to be the default device when the directory was made.

Defaults are used as a convenience not just in specifying file devices but also in file names. Large and small timesharing systems usually assign to each user some identifying code number, referred to by terms like account number, user ID, or programmer number. This number is incorporated into the file name, to associate a particular file with a particular user. A common system default lets a user omit this part of the file specification when the user is referencing his or her own files.

Another useful and common kind of default provides extensions to the file name according to the program that produced the file. For example, data files created in Multiuser BASIC have a default extension beginning with .D. Other data files might have an extension .DAT; FORTRAN files could have default extensions .FOR; input files for a macroassembler could be expected to have the extension .MAC; and that assembler might produce binary object files with a default extension of .OBJ.

File Names

T S Eliot understood the complexities of a similar subject when he wrote, in *Old Possum's Book of Practical Cats*, that:

> "The Naming of Cats is a difficult matter.
> It isn't just one of your holiday games;

Table 6: Floppy disk directory generated by microcomputer. This table is repeated from part 1 of this article.

```
k
*Q*/1
FILES 08-09 09 771219
TEXTPROC.TDL   01-01   0023   0022   064   771219   771219
BIGRUMP.TDL    01-24   0074   0073   033   771219   771219
BASIC.TDL      04-20   0065   0064   001   771219   771219
EDIT.TDL       07-07   0023   0022   001   771219   771219
IODRIVER.EEN   08-04   0005   0004   051   771219   771219
```

(a)

Position		Significance
FILE NAME	1	determines access for all users in same group
	2	determines access for all other users
	3 thru 6	no special significance
•	•	separates name and extension
EXTENSION	7	B → BASIC program; D → data file
	8	group identifier
	9	positions 8 and 9 together form the user's ID

(b)

Character	Meaning
6	read, run and update (only useful for virtual arrays)
7	read and run
8	run only
9	run only, but allows program to perform any privileged file operation
any other character	— for group library file, your group, or a public library file: read and run — any other file: no access

Table 7: A multiuser file protection system. Table 7a summarizes the significance of position in the file name. If position 9 is blank, it is assumed to be a group library file. If positions 8 and 9 are blank, a public library file is assumed. Table 7b shows the characters in file names that affect file access when they are used in positions 1 and 2. The number 8 causes the user's storage area to be erased when the program terminates.

You may think at first I'm as mad as a hatter
When I tell you, a cat must have THREE DIFFERENT NAMES."

As it is with cats, so it is with files. First, it's good to give a file a family (or group) name. The extension is one place for this, and some of the default extensions make good group names. Properly chosen extensions or family names will allow the use of wild card file names and thus greatly accelerates getting directories of groups of files.

Old Possum can help with the other two names. "First of all," he says, "there's the name that the family use daily." These should be "sensible, everyday names" such as Spacewar, Mastermind, Payroll, Heatplan or Help. They can be plain or fancy, but they must be descriptive. Often these everyday names actually refer to a system of programs, perhaps linked together. The user may not even be aware of this linkage and might refer to this system of programs by its everyday name. "Run the Help program" one user might advise another, without considering or needing to consider that this is really a collection of programs, subprograms and data files.

Finally, a file:

"... needs a name that's particular,
A name that's peculiar, and more dignified. ..."

If each file on a device does not have a unique name there will be serious problems. Further, computer operating systems put stringent restrictions on file names, restrictions necessary if the operating system is to efficiently handle requests dealing with files. A common restriction is the one on the number of characters in a file name. In TDL's 8 K BASIC, names must be one character. DEC's RT-11 permits six characters, the PerSci controller allows eight, and the latter two provide for additional extensions. Thus keeping the name particular and peculiar requires some thought.

File Protection Systems

Another consideration in choosing a particular and peculiar file name is how it fits into the local file security system. As soon as more than one person begins using a computer system there should be some way of controlling access to files. A simple way is to have users keep their files on their own cassettes or disks. But when user A creates a splendid new program and user B borrows A's cassette to copy the program, problems begin.

It is painful to remember how many times I thought the file I wanted to erase was on drive 0, and the good version was on drive 1.

Physically controlling your media gives good file security, but we often loan out our tapes and disks. Write protecting the media or device helps also, but is often impossible, inconvenient or overlooked. Carefully chosen file names are a further protection. There are several degrees of file access which can be controlled in part on many systems by the file name. These degrees of access might be:

RUN: allows executing the file.
READ: allows copying or listing the file.
UPDATE: allows modifications to the file.

Table 7 partially describes the way to

Note: "Using Files" concludes the 2 part series, "Files on Parade." The table and listing numbering is continued from part 1.

Table 8: Representative file transfer commands from several processors.

Command	Controlling Program	Computer	What Is Being Done
OLD BAGELS	BASIC (most versions)	Micro, PDP-11, etc	The program Bagels is copied from secondary memory (disk) to primary memory.
SAVE B	TDL 8K BASIC	Micro	A program called B is transferred to cassette tape.
L BASIC.TDL/1	PerSci Disk Operating System	Micro	The TDL BASIC interpreter is loaded from floppy disk drive 1 into memory.
SY:9BAGEL.B= CT0:BAGELS.MPK	RT-11 Peripheral Interface Program	PDP-11	A version of Bagels on cassette drive 0 is copied onto the system disk, where it is given the name 9Bagel, and the extension .B.

choose names in Multiuser BASIC to control user access. When working with several files at once, on different devices or media, it is good practice to use procedures similar to those in table 7, and to make sure your file names are uniquely chosen. Mastermind might now have to be called 7MASTR.BAS, but it will still be there tomorrow after others finish using it today.

So choose your file names well. Many times I have seen a programmer who has created a file and is about to name it. He sits in front of his terminal:

> " . . . in profound meditation,
> The reason, I tell you, is always the same:
> His mind is engaged in a rapt contemplation
> Of the thought, of the thought, of the thought of his name:
> His ineffable effable
> Effanineffable
> Deep and inscrutable singular Name."

[All quotations from "The Naming of Cats," Old Possum's Book of Practical Cats, *by T S Eliot, Harcourt, Brace, New York, 1939.]*

Operation \ Computer	Microcomputer (PerSci DOS)	Minicomputer (DEC RT-11, PIP)
FILE DELETION	D BAGELS.MPK/1 (delete BAGELS.MPK from floppy drive #1)	CT1: *.MPK/D (delete all files with extension .MPK from cassette drive #1)
DIRECTORY SQUISH	G /1 ("Gap" drive 1)	SY:/S (Squish the system disk)
RENAME	N 9BAGEL.B BAGELS.B	BAGELS.B=9BAGEL.B/R (rename 9BAGELS)

Table 9: Comparison of some microcomputer and minicomputer file housekeeping functions. DEC uses the term squish *rather than* pack.

Manipulating Files

There are many file operations besides the assembling of directories that are performed at the command level. Most of these operations fit into the general framework of moving a file from one place (device, library, etc) to another. The transfer can be represented symbolically as:

DESTINATION: FILENAME.
EXTENSION ←SOURCE: FILENAME.
EXTENSION.

Copying a file from one floppy disk to another, listing a file on a terminal, and moving a file from cassette to primary memory are examples of file transfer. The specific commands vary greatly from system to system, and, even within a system, from one language or utility tool to another. Table 8 illustrates a small selection of these commands.

Deleting a file is also a kind of file transfer; the file is moved to "nowhere." On a directory device, the directory reference to the deleted file is usually removed; the file itself is probably still on the medium and can often be recovered if its absolute location is known.

Another file transfer operation, the media *pack*, eliminates gaps on disks and tape due to deleted files, and packs together the remaining files to make room for more. A disk can usually be packed without the use of a second disk drive, but cassettes often require repacking on another medium.

Finally, renaming a file can be thought of as a file transfer within the symbolic format above. The destination and source do not change, but the file name and extension do. Table 9 compares typical minicomputer and microcomputer pack, delete and rename operations.

Function	Multiuser BASIC Implementation
assign a status; assign a mode; assign a channel	10 OPEN "9VISR0. B53" FOR OUTPUT AS FILE #2
write on a file	20 PRINT #2: L$
read information from a file	30 INPUT #2: A, B1, T3
test for end of file	40 IF END #2 THEN 100
move data pointer within the file	50 RESTORE #2
make the file permanent; deassign the channel; change the file status	60 CLOSE #2

Table 10: Types of program file control statements. The line numbers used in the examples are to emphasize that these are statements within a program.

File Control

In addition to the file manipulations previously described, there are several kinds of file control statements designed to be part of an application program. Instead of a file handling operation happening in response to a command from the keyboard, using perhaps the monitor system or operating system commands, this second kind of file control happens in response to a program statement. Again, the specific format varies from language to language; unfortunately it also seems to vary within a language like BASIC from manufacturer to manufacturer. However the functions performed in response to these statements are fairly standard. Table 10 is a summary of these functions, with examples from BASIC.

Assigning a unique channel, or data path, to each active file is one way for the operating system to allow simultaneous (or at least parallel) access to several files. Obviously this is necessary in a timesharing system, but it is also convenient for a single user reading text from one file, editing it, and then writing it into an output file. In the first example in table 10, the file 9VISR0 is assigned to channel number 2. (The maximum number of channels will depend on the system configuration.)

The file status can be open or closed. Here again the requirements vary from system to system, and within systems according to file access types. The PerSci disk operating system, for example, allows *stream* access regardless of file status. But stream access usually happens at command level. *Relative* access, used for data base applications, requires a file status of open to store or retrieve file data.

The file mode requirements (input or output) depend on access type too. For this function, though, the distinction is clearer. Once random access files are open, the mode does not usually need to be specified because individual bytes can be changed without touching other parts of the file. However sequential files must be updated as a unit, and therefore a sequential file must generally be set into either input or output (read or write) mode. Remember that input and output refer to the direction of information flow relative to the processor, and not to the storage medium: information comes into the processor from the disk; information goes out of the processor to the disk.

Testing for the end of a file and moving a data pointer within a file are operations characteristic of sequential access files. A random access file has a fixed length, so presumably one knows where the end of it is. Similarly, since individual bytes of a random access file are directly addressable, it is unnecessary to move a data pointer. In practice these functions are performed by program logic statements.

Some kinds of files are more rugged than others; they stand up better to programmer or user abuse. Aborting an information transfer to a sequential file in the midst of the transfer can cause the loss of the whole file, for example. The close command, for both access types, puts a lock on the file door and frees up a data channel, too. Other BASIC program statements (such as CHAIN, END) will often do the same thing. Good programming practice is to do it explicitly, with statements such as CLOSE.

Explicit file initialization is also good practice. Random access files, occupying a specific part of a disk, could contain information left on the disk by a previous program. (Recall that file deletion usually means that the directory entry, not the file itself, is deleted.) At the other end of the line, it is wise to erase a file containing sensitive information when its usefulness is over. These operations can all be done with file control statements in programs.

Programming Techniques Using Files

Whole articles, even whole books, are written to discuss file programming techniques. This final section is not meant to be that comprehensive. Rather, it is a quick dip into the programmer's bag of tricks—a look at some of the methods used to deal with the limitations of smaller systems. The em-

```
100 PRINT 'TYPE THE LETTER CORRESPONDING TO YOUR CLASS:'
110 PRINT '      A--PRACTICAL BIOLOGY, PER. A'
120 PRINT '      B--PRACTICAL BIOLOGY, PER. B'
130 PRINT '      C--BISCI'
160 PRINT '      E--PRACTICAL BIOLOGY, PER. E'
170 PRINT 'CLASS'; \ INPUT S$
200 PRINT 'TYPE THE NUMBER OF THE OPTION YOU NEED:'
210 PRINT '      1-ENTER SCORES FOR WHOLE CLASS'
220 PRINT '      2-ENTER SCORES FOR SOME STUDENTS'
230 PRINT '      3-LIST STUDENTS WHO HAVE COMPLETED A GIVEN ITEM'
240 PRINT '      4-LIST STUDENTS WHO HAVEN'T COMPLETED A GIVEN ITEM'
250 PRINT '      5-DISPLAY SCORES PROFILE FOR AN INDIVIDUAL STUDENT'
260 PRINT '      6-DISPLAY PROFILE FOR A SELECTED GROUP OF STUDENTS'
270 PRINT '      7-DISPLAY CUMULATIVE TOTALS FOR ALL STUDENTS'
280 PRINT '      8-LIST OR MODIFY STUDENT NAMES OR ITEM HEADERS'
290 PRINT '      9-CREATE BACKUP FILES'
300 F$='9VISRO.B8'+S$ \ CHAIN F$
```

Listing 2: BASIC code for an option choice menu. When the option is chosen, the required code is chained into main memory by line 300.

phasis is on techniques available in versions of BASIC that support named files which can be called from secondary memory devices such as cassettes or floppy disks.

Shortening Program Size

For student programmers at Sanborn Regional High School, where I teach, and especially for students with grandiose plans and unprivileged user numbers, the most frustrating error message is PTB, which means the *program* is *too big.* There are three file related approaches to this problem that we urge on the students—approaches that fit into our push for modular program design.

First, for programs that have a linear logical flow, we encourage breaking the program into small segments that can be connected by CHAIN statements. A CHAIN statement such as

110 CHAIN "WUMPS2.BAS"

erases the program currently in main memory (perhaps called WUMPUS.BAS), and replaces it with the program file WUMPS2.BAS. Variables whose values are needed in the second, or chained-to, segment, can be declared in a COMMON statement in the first segment. A typical usage of the CHAIN statement is to segment some long game. The first segment might request information from the user: "Do you want instructions?" If yes, instructions are given; if no, there is a branch directly to the end of segment 1. In either case, the logical flow reaches the end of the first segment, where there is a CHAIN statement to a program file that contains the code for the main body of the game.

A second method works well for application programs that give the user a choice of options. This method puts the *menu* of choices in one program file and each of the various options, or "meals," in separate program files. Listing 2 shows the code for a typical option menu. The menu file and the meals files could be connected by CHAIN statements or by OVERLAY statements.

The OVERLAY statement calls a named program file from secondary memory and "lays it on top of" the program currently in memory. Suppose the original program has a line 100. After the OVERLAY statement in the original program is executed, line 100 in memory will be the one from the overlay file. A line with a number either in the original program or in the overlay file, but not in both, will always be in memory after the overlay.

For the multiple branch logical flow characteristic of the menu and meal method, the decision to use CHAIN or OVERLAY to connect the program files usually depends on how much logic and code can be shared by the various meals. If several of the options utilize the same set of subroutines, or if the options access the same set of data files, it makes sense to use overlay files. Then, in lines that will not be overlaid, the original program can hold the shared subroutines or statements opening and closing the shared data files. If the meals are quite disjoint, and there is little need to pass information back and forth, chaining the segments will increase the modularity of the code.

In either case the goals are to keep the modules small and the interface between them independent of the module used. Smaller segments fit into more machines and are easier to understand. The interface should allow adding options or replacing an option with an improved version without having to modify all of the other options. This plug-in quality facilitates writing code that is easy to change and easy to use.

Data Files

The third technique for using files to achieve modular program design is to separate the data from the program operating on it. An example is the payroll program mentioned in part 1. Another application is to the tutorial, drill and practice, and testing programs used in computer assisted instruction. A common type of program in this group is one that gives a multiple choice quiz. Variety can be added by putting a large bank of questions and accompanying choices in a data file. The main program can then pick five or ten numbers randomly and call

Circle 357 on inquiry card.

```
120 REM *** OPEN DATA FILE
130 OPEN 'GRIPE.D22' AS FILE VF1$(20)=250
140 REM  ***  NUMBER OF GRIPES = N
145 N=VAL(VF1(0))
160 PRINT 'WHAT IS THE NUMBER OF THE GRIPE YOU WISH TO DELETE';
170 INPUT D
180 VF1(D)=''
190 FOR K=D+1 TO N
200 VF(K-1)=VF(K)
210 NEXT K
250 REM  ***  RESET N AND SAVE UNDER VF(0)
260 N=N-1
270 VF1(0)=STR$(N)
```

Listing 3: Using a virtual array with Multiuser BASIC. This allows the user to think he is using an array when actually there is a random access device which is holding the bulk of the information.

out the questions and choices matching those numbers to make up a particular test from the file. Using essentially the same kind of programming, the words for the computer's side of a game like Hangman can be kept on a data file.

A slightly more sophisticated method is to use one master program to administer several different multiple choice tests. The user might supply the name of the test, and the program would open the data file containing the appropriate bank of questions. The first word of the data file might hold information about how many questions are in the file, how many choices per question, how many questions comprise a test, etc. The same master program can handle many different question and answer banks.

Still another type of program can extract information from more than one data file to construct a question. For example, a quiz on chemical formulae can be designed by randomly taking one element name (calcium, aluminum, sodium, . . .) from one file, and another (chloride, sulfide, sulfate, . . .) from a second file.

A common feature of these examples is that space-eating dimensioned arrays are avoided by keeping the data in files, and calling and using only a few elements at a time from a file. When new data is called out, it can be given the same variable name as the previous small group of data. Virtual arrays stored in random access files can be thought of as extensions of this technique. As listing 3 shows, the items in the file can be addressed as if they were part of a dimensioned array in memory. However no dimension statement is necessary in the program, and the programmer has the best of both approaches: access and update as if the variables were in main memory, but space utilization corresponding to their actual storage on files, an ideal arrangement for a data base.

Files as Buffers

Finally, one more data file technique deserves mention: using files as buffers, as temporary collection boxes for string or numeric information. The names of the elements for the chemistry tutorial and the text for a Help program are examples of data stored in files on a relatively permanent basis. In contrast to this kind of use, files can provide transient storage for data. They might be used as extra workspace for calculations or manipulations like sorts or holding intermediate results.

Perhaps the chemistry tutorial program creates three problems for the student to do at home using random numbers. A file could contain the answers to those problems, to be accessed once the next day when the student checks his or her answers against those in the file. The answers would then be erased.

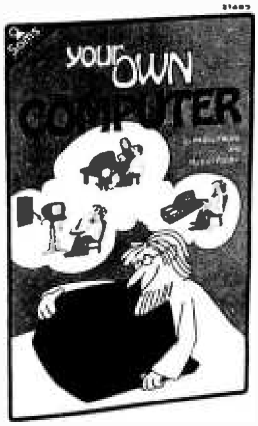
The list of books or equipment loaned to friends can be placed in the buffer file of a home information program, with items removed from the file as they are returned. Buffer files can also be used to hold messages taken by a computer interfaced to an automatic answer phone modem, or by a computerized suggestion box (a gripe file), or to hold mail in a computer conference.

Sometime there will be a secondary program to examine, modify, and erase these buffer files. At our high school, for instance, a secondary program reads the gripe file and removes meaningless or obscene comments before the file is posted on the bulletin board.

A Qualification

This article, an introductory tutorial, has skimmed the surface of the concept of files. The richness of file structures and the power of the many techniques have led to varied implementations, only a few of which are illustrated here. Readers are urged to study the manuals for the systems they use both to learn the capabilities of those systems and to find the exact syntax for the techniques described in this article. With respect to file structures and types, microcomputer systems in particular are closer to the Tower of Babel end of the spectrum than they are to any monolithic standard. Now is the time to write about files, to learn about files and to build file systems.■

Book Reviews



Your Own Computer

by Mitchell Waite and Michael Pardee
Howard Sams Co Inc
Indianapolis IN, 1977
80 pages
$1.95

The last three books I read were *Passages, Star Wars* and *Your Own Computer.* You see, in between the second and third books a rather futuristic friend loaned me a copy of BYTE, saying, "You won't believe this!"

I didn't. A computer in every home? In department stores? Right now? Being a writer with a science fiction orientation, I was shocked and simultaneously exalted to find that companies were already selling all kinds of low cost home computers, and that perhaps I could buy and use one.

After devouring BYTE in less than two hours, I called my friend and asked him if he knew of any books that explained these personal computers in simple terms, something a nontechnical person like me could understand.

Two days later I went to the local computer store and picked up a copy of *Your Own Computer,* a book that has completely changed my viewpoint about the future of technology. I thanked the universe for being so kind, told my friend, "May the force be with you," and hid myself away for the next day to learn what this home computer thing was all about.

In the preface, the authors informed me that the invention of the personal computer is the most historic event since the automobile, television and transistor combined. This book was designed to remove the the stigma of complexity and mystery that surrounds computers, and would probably be my first investment on the road to acquiring my own computer. That made me rather suspicious from the start. How do they know I'll like computers? I might hate them, but I'll admit I was interested.

Chapter 1 was quite interesting. Called "Introduction," it defined what computers

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We're ComputerLand, the #1 computer store chain in the U.S. What's meaningful about that fact is, that ComputerLand has been chosen by more people as having what they've been looking for. And, since you're looking, let us tell you what you'll find, when you visit a ComputerLand store.

You'll find a product line that's continually evaluated to provide you with the widest and best selection in quality, brand name microcomputers anywhere. You'll find an enthusiastic and knowledgeable staff able to interpret all the equipment specifications, in terms of how they apply to you, and in a way you'll understand. You'll find demonstration areas where you can get a firsthand experience of running a computer yourself.

COMPUTERS FOR BUSINESS

You'll find educational materials to give you a total insight into the world of microcomputers.

You'll find a fully equipped service department to provide whatever assistance is required to keep your computer running in top-notch condition. You'll find computer user's clubs to join, where you can share ideas with people as enthusiastic as yourself. And, with each new visit, you'll find excitement—from the people you deal with, the equipment they offer, and from your own ever-growing personal involvement.

Enough about us. How about what computers do. To attempt to describe all the things your computer might do, would be to describe your imagination. So instead, we'll briefly list some of the many things for which small computers are already being used.

In business, the advent of the versatile and compact microcomputer has put the benefits of computing within reach of small companies. With systems starting at less than $6000, the businessman can computerize things like accounting, inventory control, record keeping, word processing and more. The net result is the reduction of administrative overhead and the improvement of efficiency which allows the business to be managed more effectively.

COMPUTERS FOR THE HOME

In the home, a computer can be used for personal budgeting, tracking the stock market, evaluating investment opportunities, controlling heating to conserve energy, running security alarm systems, automating the garden's watering, storing recipes, designing challenging games, tutoring the children . . . and the list goes on.

In industry, the basic applications are in engineering development, process control, and scientific and analytical work. Users of microcomputers in industry have found them to be reliable, cost-effective tools which provide computing capability to many who would otherwise have to wait for time on a big computer, or work with no computer at all.

COMPUTERS FOR INDUSTRY

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for the average consumer were like, and where they evolved (a natural evolution of big computers, the further miniaturization of electronic components due to the space race, the development of large scale integration [LSI] by the semiconductor makers, the pocket calculator, the digital watch and the TV game).

Chapter 2, called "Personal Computer Applications," goes into just what personal computers can do for you. Applications for the home, business, classroom and just plain fun are explained, using cartoons for punctuation.

What really impressed me was that one computer could do so many different things. The examples that turned me on the most were: "In the Office," where the computer would automatically display my next appointment while it balanced the company's books; and "Organizing Your Hobby," where the computer would maintain a cross file of my photography collection. I was definitely getting turned on.

The next chapter, "Program for Your Computer," made it clear that it takes a great deal of concentrated thought to write computer programs, and that I probably wouldn't need to know much about programming, since thousands of people were already available to do the programming for me. However, I would need to learn to communicate my needs to a programmer if I wanted to do something special with my computer that wasn't already available from a manufacturer, or someone else. Still, I was assured that most of the programs I would ever want would be furnished by the people who sold me the computer; so the pressure to learn programming apparently was off. That's good because then I began to see a computer as just another consumer product, rather complex but still quite manageable.

In the next chapter, "Nuts and Bolts," I learned what kinds of things make a computer tick. Computers have many hookup parts and equipment. In a way, they are a lot like cameras. Just as camera owners buy lenses and other attachments to enhance the power of their equipment, computer owners may purchase "peripherals" to beef up their systems and give them more flexibility.

Although the authors promised to give me enough information to enable me to walk into any computer store and not be snowed by the equipment, I felt rather rained upon during one such visit. The range of products offered in these computer stores is amazing. I didn't see any two computers that looked, worked, or even cost the same. However, after I finally started talking to the store owner, I was very glad that I had read the chapter about nuts and bolts. Each time he would show me a particular computer system, I would say something like, "Does it have a software front panel?", or "How much memory and read only memory is there in the minimum system?" My questions seemed to elicit surprise, and I found the owner gleefully explaining everything in fine detail.

One of the nicest things about the nuts and bolts chapter was that I learned about the most often used computer I/O devices: keyboards, video displays, front panels, Teletypewriters, cassette tape mass storage, floppy disk mass storage, etc. Photographs of each device were included.

The final chapter in the book, entitled "Getting Started," explains how one goes about taking the next logical step in understanding, or perhaps even buying, a personal computer. Like the others, this chapter is illustrated with our friendly computer enthusiast trying his luck at learning more about personal computers by going to conventions, reading books and magazines such as BYTE, visiting computer clubs, and of course going to a store.

For me one of the most useful parts of the book was the appendix called "Glossary of Computer Buzz Words." Here I quickly learned the meanings of the crazy words used by computer people. I read the entire glossary from A to X; it was very interesting. Each word was defined and then used in a typical sentence. I memorized a few of these buzz words and used them on the computer store owner. For example, while he showed me a computer game called Star Trek that didn't seem to be working right, I informed him that perhaps his "buffer had overflowed." All I got was a chuckle, and then a sigh.

Well, I finished the book and can honestly say that for someone who previously knew nothing about computers, I really got my money's worth. Besides learning that computers are here to stay, I discovered that the future of home computing is changing fast and furiously. Although delaying my purchase for a few years may save me a lot of money, it will also mean I'll miss out on a whole lot of fun and excitement.

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A Microprocessor for

Part 3:

Terry Ritter and Joel Boney
Motorola Inc
3501 Ed Bluestein Blvd
Austin TX 78721

Photo 1: Processing. Photosensitized wafers are exposed with a particular mask pattern using ultraviolet light. The entire environment is otherwise ultraviolet-free.

Photo 2: Breadboard debug. The gate level TTL model of the processor involves ten boards of 80 to 120 integrated circuits each. Many of the required 10,000 connections will be wrong. The system must be tested to find and correct construction and logic errors.

Crowds are not unusual; here we have Don Tietjen, Katy Miller, James Tietjen, Steve Messinger (almost hidden), Mike Shapiro and Bill Keshlear.

Clock Speed

In part 3 we conclude our discussion of the Motorola 6809 processor with some thoughts on clock speed, timing signals, condition codes and software design philosophy for the 6809.

We expect that our logic and circuit design cohorts will be able to get significant production at a 2 MHz bus rate (and possibly faster) with the 6809. But this value alone means next to nothing as a figure of processor merit (we did consider using a very high frequency on chip oscillator so we could win the clock rate race, but decided at the last minute that a resonant cavity would not be acceptable to most users).

Other processors use an internal state machine to implement the required internal operations. These processors frequently require multiple states and multiple clock edges to implement operations which are done in one cycle on 6800 class processors.

The 6800 class machines are all random logic machines with multiple dynamic sequencers. This method of microprocessor design selects a different set of engineering trade-offs as opposed to the state machine approach. In particular, less critical timing is necessary, but suspending the processor for a long time is difficult. We provide two external methods of stopping the machine: $\overline{\text{DMAREQ}}$ (which has a maximum asynchronous latency of 1.5 bus cycles, and which will recover the bus from DMA (direct memory access) periodically to allow the dynamic microprocessor to perform a refresh cycle) and $\overline{\text{HALT}}$ (which has a maximum latency of 21 cycles, but releases this bus completely).

Signals

The 6809 processor will be made in two versions: the on chip clock version (for small systems) and the off chip clock version (with extra signal lines for additional processor status information). This will allow a cost-effective utilization of pins for each proposed market.

The bus timing signals are E and Q. E is

the Revolution: The 6809

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and Joel Boney

Final Thoughts

the same as on 6800 systems (previously called Ø2), a square wave clock with a period equal to one bus cycle. Q is the quadrature clock, and leads E by one quarter bus cycle. Good addresses should be available from the processor on the leading edge of Q; data is latched (by the processor or selected memory or peripheral) on the trailing edge of E.

Two signals are used for clock control in the on chip clock version. $\overline{\text{DMAREQ}}$ halts the processor internally (and puts the output lines of the processor in the high impedance state using three state circuitry) but allows E and Q to continue to run to provide system clocks for a DMA transfer. MREADY being low extends a memory access in increments of the high frequency oscillator period until MREADY is brought high.

If BA=0 (the processor is running) BS=1 means that a vector fetch is occurring (IACK). This signal can be used to develop vector-by-interrupting-device hardware that transfers control directly into the desired interrupt handler without polling.

Two signals are available in the off chip clock version to assist in multiprocessor systems. The last instruction cycle (LIC) pin is high during the last execution cycle of any instruction, thus giving bus arbitration a head start. BUSY is high during read modify write, (from the read through to modify) to indicate that memory exclusion is required. Exclusion is required in multiprocessor systems.

Condition Codes

The 6809 condition code flags are the same as those used in the 6800 (N, Z, V and C), and are affected similarly by most operations. Some exceptions are the double byte operations, since the flags are always set to represent the result of the entire operation, whether single or double byte. (This is implied by the fact that both data length operations have the same root mnemonics).

While very simple in concept (the condition flags being mere by-products of arithmetic and logic unit [ALU] operations), their use with various data representations

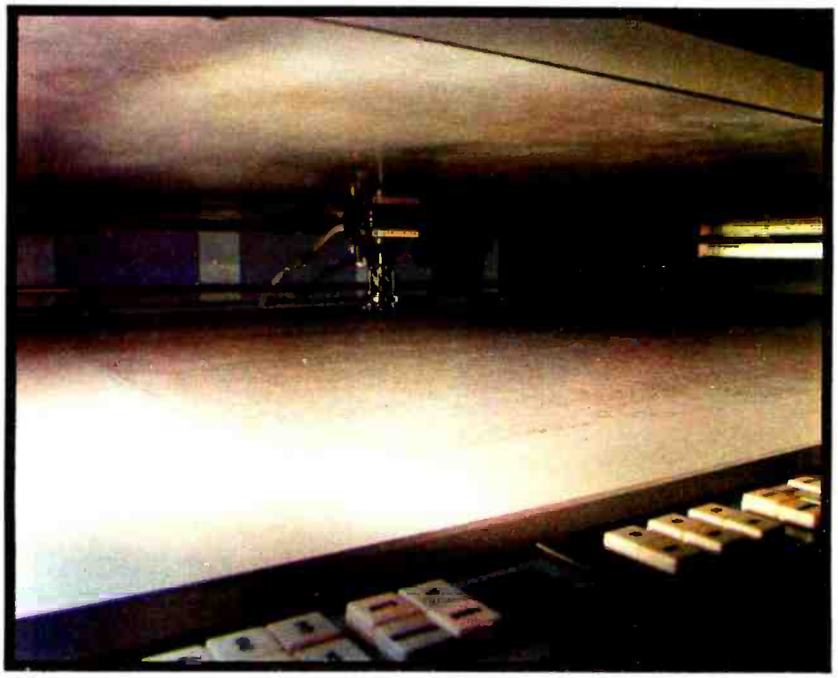

Photo 3: Plotting the circuit layout. Huge precision plotters display the computer data base which will become the chip. The layout plot is then checked by circuit engineers both for proper interconnection and exact transistor sizing. Any problems thus uncovered will be repaired by editing the data base.

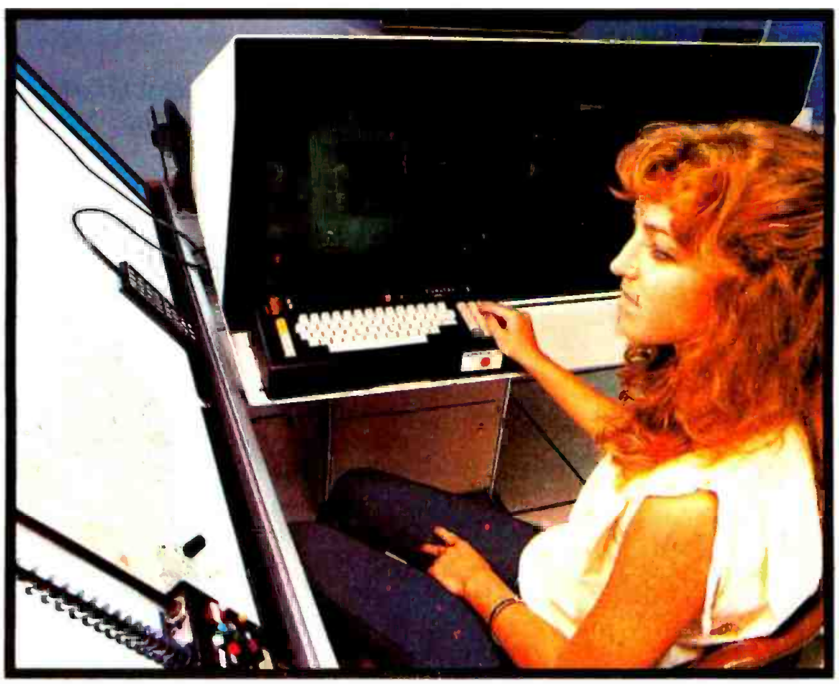

Photo 4: Digitizing. Computer aided design (CAD) technician Lisa Fink enters a cell layout into the data base. The cursor on the light table is used to transfer precision measurements to the computers. An already digitized cell is shown on the video display.

Photo 5: Diffusion. Into the furnace goes another batch of wafers in the process of becoming integrated circuits. Operating near 1000° C, the quartz liner glows incandescent.

and the rich set of conditional branch conditions can seem quite complex. First, we will define the flags as follows.

N: set if and only if the most significant bit of the result is set (this would be the 2's complement "sign" bit).

Z: set if and only if all bits of the result are clear (the result is exactly 0). set

V: if and only if the operation causes a 2's complement overflow. Notice that the expression $(N \oplus V)$ will give the correct sign, even if the sign is not properly represented in the result.

C: set if and only if the operation causes a carry from the most significant bit (for ADD, ADC) *or*,

set if and only if the operation does not cause a carry from the most significant bit of the arithmetic and logic unit (for subtract-like operations – SUB, SBC, CMP – carry flag represents a borrow) *or*,

set according to rules for rotate or shifts *or*,

set if and only if bit 7 of the result is set (for MUL).

- Notice that the C flag is not the simple result of the carry in the 8 bit arithmetic and logic unit, but depends on the type of operation performed.
- Notice also that the carry flag represents a borrow after subtract-like operations. This was done on the 6800, for convenience.

Next, let's define the use of the branches. Simple conditional branches:

Test	True	False
Z=1	BEQ	BNE
N=1	BMI	BPL
C=1	BCS	BCC
V=1	BVS	BVC

Signed conditional branches:

Test	True	False
$\overline{(N \oplus V)} \wedge \overline{Z}=1$	BGT	BLE
$\overline{(N \oplus V)}\ \ =1$	BGE	BLT
Z=1	BEQ	BNE
$\overline{(N \oplus V)} \vee Z=1$	BLE	BGT
$\overline{(N \oplus V)}\ \ =1$	BLT	BGE

Unsigned conditional branches:

Test	True	False
$\overline{C} \wedge \overline{Z}=1$	BHI	BLS
$\overline{C}=1$	BHS	BLO
$\overline{Z}=1$	BEQ	BNE
$C \vee Z=1$	BLS	BHI
C=1	BLO	BHS

Note: The unsigned branches are not, in general, useful after INC, DEC, LD, ST, TST, CLR or COM.

And finally, the flag results of known conditions of comparison are as follows.

After SUB, SBC, CMP:

If register is less than memory value (2's complement values) $(N \oplus V)=1$.
If register is lower than memory value (unsigned values) C=1
If register is equal to memory value (signed or unsigned) Z=1.

Because some instructions do not (and should not) affect carry, only the equal and not equal branch tests (BEQ, BNE) are useful after these instructions (INC, DEC, LD, ST, TST, CLR, COM) operate on unsigned values. When operating on 2's complement

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values, all signed branches are correctly available.

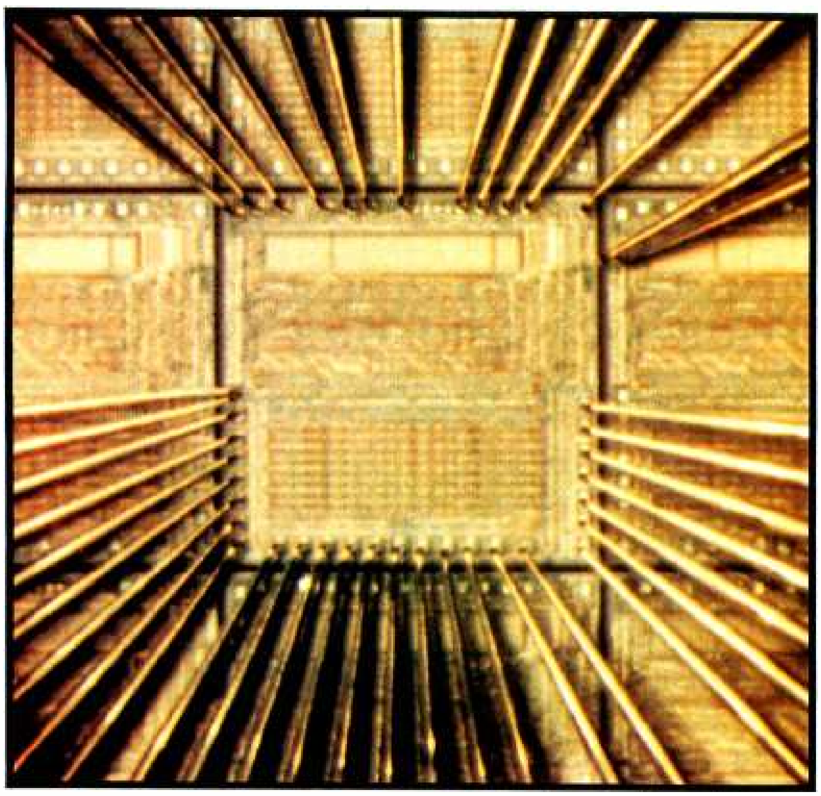
Some Software Design Philosophy

The design of successful software differs from other types of engineering design in that good software can be easily changed, but is exceedingly unforgiving. The creation of working software involves intimate contact with *quality*.

Any program, working or unworking, is a representative of the philosophy of *truth*; the machine will execute the program, good or bad. Only applicable programs are useful, however, and utility is where we encounter quality. Many individuals indoctrinated into a society founded upon truth can scarcely understand why such truthful programs do not work, for isn't one truth just as good as another?

Any program that is to be fixed or changed must be analyzed: the written code must be read and understood. Reading is a problem — most computer languages are very difficult to read simply because so many options are possible from each statement. Finding the coherent design of a program is nearly impossible when, as it is being read, thousands of options exist. It is the paradox of programming that a disciplined, restricted, structured programming language gives programmers greater freedom to understand their programs.

Photo 6: Wafer probe. Each circuit is separately checked while still on the wafer. This equipment automatically steps to the next chip after any bad result or when all tests are good. A production 6800 is shown.



Consider the analysis of programs: any program segment having multiple conditional branches that cannot be separated must be analyzed for all possible conditions of input data before we can be assured that the program will operate correctly.

Program segments having branch paths that cross may be impossible to analyze rigorously due to the combinatorially larger number of paths that the program may execute. Where control structures are always properly nested, crossed branch paths cannot occur and analysis is easier.

Programming structures which have basically one entry point and one exit are easily detached from surrounding code and are easier to understand and test. This is the fundamental tenet of structured programming.

Every attempt should be made to code in modules. Modules are self-contained entities (usually subroutines) which allocate and deallocate their own local storage. Naturally, the actual code should be heavily commented to allow a reader to understand what is being attempted. But one mark of a good module is that it contains a header block which fully describes *all* aspects of the inputs to the module and results from it. This description should be so detailed as to allow the module to be totally recoded from this information alone. We hope that the description was arrived at *before* the module was written. It is a mark of good software design that the actual coding is but a minor part of the project; it occurs after all modules have been completely described. The finished modules should be individually tested for all possible input values, and should demonstrate that error handlers will operate when a supposedly invalid input value occurs. Modules which are recoded at a later date must pass the original tests.

Software in the Revolution

The microprocessor revolution is fueled by continual technical advancement that produces hardware with ever higher capability and ever lower cost. Yet, it is a requirement of the revolution that software be written to make that cheap hardware *do* anything.

Most present microprocessor software is custom software written for a specific project. Project specific software is rarely published, partly in the (unreasonable) hope of maintaining trade secret protection, and partly because finished project software is rarely of publication quality. Commercial software is rare for a number of reasons:

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there must be a market for the (machine specific) software before the investment in program development is made, but the customer base may not exist until good programs are available. It is also difficult to consider investing in software that can be so easily copied (stolen) and used.

The copying problem is not new; musical reproductions have long coexisted with the possibility of consumer recording and reproduction for a close circle of friends. This occasionally happens, but it is usually too much bother to tape the music you want (assuming that the original product is available at a reasonable cost). Software should be distributed as a reasonably priced physical product that is useful to a broad consumer base.

This is an old idea, but it just hasn't worked. The problem is not in the idea, but in the second generation microcomputer architectures which limit the applicability of any particular program read only memory. The 6809 microprocessor is designed specifically — through the use of position independent code, stack indexing, and indirect addressing — to allow the creation of standard program read only memories. This creates a market opportunity for a brand new standard software industry. We knew this when we included these features; you're welcome, entrepreneurs!

Summary

We wrote this series of articles not only to disclose the 6809 but mainly to put down in print the rationale and reasoning behind the 6809. It would have benefited us if the designers of the 6800 had documented their rationale. We would also like to think we have stimulated some interest in the personal computing community for solutions to the software problem and for the study of computer architecture. The big challenge for architects in the next decade and beyond will be to design computers that can effectively utilize the huge number of devices — 1,000,000 transistors by 1985 — that semiconductor technology will be able to put on one 25 mm^2 piece of silicon.

No computer is designed in a vacuum, and we would like to thank all of our customers and the people at Motorola who gave us valuable input. Special thanks go to the dozens of people — too many to enumerate — who have been or are still actively involved in the design, implementation and production of the MC6809. Without their individual talents and dedication to what seemed to be impossible tasks and impossible schedules, the MC6809 could not have been realized.■

Event Queue

March 3-4, Micro-Expo '79, Texas A and M University Memorial Student Ctr, College Station TX. Sponsored by The Texas A and M Microcomputer Club, the activities at the third annual Micro-Expo '79 will include exhibits by dealers and hobbyists, a programming contest, and a computer chess tournament, as well as seminars on topics of interest to both the novice and the experienced computer enthusiast. Contact Larry Brown at (713) 693-5748 or Scott Edwards at (713) 845-5531.

March 10-11, Personal Computer Fair, Pacific Science Ctr, Seattle WA. The fair will acquaint people with personal, home and hobby computer applications. Visitors will see a variety of nontechnical demonstrations and have numerous opportunities for hands-on experimentation. Contact Susan Stocker, Pacific Science Ctr, 200 Second Av N, Seattle WA 98109.

March 17, The Computer Faire, Delaware State College, Dover DE. This faire will deal with current technology of computers for the classroom and personal use. Contact Lynda Baker, New Castle County School District Area II, Henry B duPont Middle School, Benge and Meeting House Rds, Hockessin DE 19707.

March 19-20, Microcomputers: Operating Principles, Hardware and Software Seminar, Holiday Inn, Palo Alto CA. Polytechnic Institute of New York and the Institute for Advanced Professional Studies are presenting this 2 day seminar for engineers, programmers, and technical managers involved with selection of microprocessors and design of microprocessor-based systems. The seminar will cover the underlying concepts governing microprocessor operation, architecture, and systems design. Microcomputer elements and their interrelationships will be discussed, emphasizing features important in determining whether a particular microcomputer will be suitable for a given task. Contact Prof Donald D French, Institute for Advanced Professional Studies, 1 Gateway Ctr, Newton MA 02158, (617) 964-1412.

March 19-21, Federal DP Expo Conference and Exposition, Sheraton Park Hotel, Washington DC. This fifth annual government show will feature computer related hardware, software and service.

Continued on page 76

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Cryptography in the Field

Part 1: An Overview

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Senior Consulting Engineer
General Electric
Court St, Bldg 4, Rm 38A
Syracuse NY 13201

Cryptography could be described as the science or art of transforming messages into forms that render them unintelligible to outsiders. This is an old and fascinating field and the interested reader could hardly do better than to read a most remarkable book on this subject by David Kahn called *The Codebreakers.*

A few definitions are needed before proceeding. *Plaintext* is the message to be put into secret form. The message, after cryptographic transformation, is known as a *cryptogram*. An authorized individual who is privy to the secrets of the system is said to *decode* or *decipher* the message when converting the cryptogram to plaintext. *Cryptanalysis* is the science or art of extracting the meaning of a cryptogram without the key. *Cryptology* is the science or art encompassing both cryptography and cryptanalysis.

A code is a cryptographic transformation in which no fixed relationship is maintained between the number of symbols in the plaintext and the corresponding cryptographic transformation or *codetext*. An example of a code is shown in table 1. To encode a message the plaintext word or phrase is found in an alphabetical listing in the encoding section and the corresponding codetext group (in this case 5 digit numbers) is entered into the cryptogram. Note that commonly used words (eg: ballistic) may have more than one codetext equivalent. These are known as *homophones*. There may also be codetext groups that have no plaintext equivalent; these are known as *nulls*. The coding clerk is encouraged to select at random from a group of homophones and also to throw in an occasional null in an effort to frustrate the work of the cryptanalyst.

In the decoding section, the codetext groups appear in their numerical order. The security of a code is enhanced when the codetext numerical order is scrambled relative to the plaintext alphabetical order. When this is done the codebook contains separate encoding and decoding sections. Such codes are known as *2 part* codes. The resulting codetext is often given a further cryptographic transformation (encipherment); the overall process is then known as *superencipherment*.

In many applications, a cipher is preferred to a code. A cipher is a cryptographic transformation in which a fixed relationship is maintained between the number of plaintext symbols and the number of symbols in the resulting cryptographic transformation (ciphertext). An example of a simple cipher would involve replacement of each plaintext letter by the next letter in alphabetical order. Plaintext A becomes ciphertext B, plaintext B becomes ciphertext C, etc. Some feeling for the difference between codes and ciphers may be obtained by noting that linguists are often assigned to break codes while mathematicians handle the ciphers.

This article deals mostly with field ciphers, of which there are two main classifications: substitution and transposition. In the former, new symbols are substituted for the plaintext symbols to form the ciphertext. In the latter, the original symbols are

Encoding			Decoding	
plaintext	codetext	nulls	codetext	plaintext
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
BALANCE	78452	17593	17590	AFTERBURNER
BALANCE SHEET	43987	43874	17591	DETACHED
BALL	15638	12958	17592	UNLIKELY
BALLAST	28457	84355	17593	(NULL)
BALLISTIC	12953		17594	JAMMING
BALLISTIC	87465		17595	STATUTE OF LIMITATIONS
BALLISTIC	72589		17596	BALLOON
MISSILE			.	.
BALLOON	17596		.	.
.	.		.	.
.	.			
.	.			

Table 1: A simple 2 part code example. The encoding section is alphabetically arranged and the decoding section is numerically arranged. To further frustrate the efforts of anyone intercepting the message, nulls are frequently used (a null is a portion of ciphertext having no plaintext equivalent).

plaintext alphabet:	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
ciphertext alphabet:	P	A	T	R	I	C	Z	L	O	N	K	B	D	E	F	G	H	J	M	Q	S	U	V	W	X	Y

Table 2: This relatively simple cryptographic procedure can be used as a field cipher. First the plaintext alphabet is written, then the ciphertext is written underneath it. The message is coded by using the ciphertext alphabet in place of the plaintext alphabet. The former is arrived at by using a keyword. In this case, the keyword Patricia Zlotnik is written followed by the unused letters of the alphabet. No letters are allowed to repeat.

retained but the order of appearance is scrambled to prevent disclosure of meaning.

Field Ciphers

Field ciphers are traditionally relatively simple cryptographic procedures which can be implemented readily in the field using only pencil and paper. The definition of *pencil and paper* is updated here to include the ubiquitous electronic pocket calculator. Common to these systems is the use of an easily remembered word or phrase which serves as a *key* in the cryptographic process. In the illustrative examples that follow we will use as a demonstration keyphrase:

PATRICIA ZLOTNIK

and as a demonstration message:

MAY UP BID PRICE TWENTY
PERCENT ON TRACT ONE ONLY.

In one form of a monoalphabetic substitution, the key is first written by eliminating repeated letters, followed by the remainder of the alphabet in order as shown in table 2. By substitution from this table, M becomes D, A becomes P, etc. The following cryptogram results for the demonstration message:

D P X S G	A O R G J
O T I Q V	I E Q X G
I J T I E	Q F E Q J
P T Q F E	I F E B X

The ciphertext is represented here in the standard form used by cryptographers, in groupings of five characters. The ciphertext should be read across both columns rather than across one (eg: the ciphertext in this example would be DPXSGAORGJOTIQV).

The cryptogram purposely does not preserve word groupings. How good is this cipher? It is both unbreakable and worthless. If the only message ever sent is the single 3 letter word:

CAT

then the cryptogram:

TPQ

is beyond rational cryptanalysis. On the other hand, even very light usage (such as the demonstration message) allows simple frequency analysis to begin the destruction of the cipher. The fact that the letter I has been used to replace the plaintext E will not remain a mystery for long. By any practical measure, monoalphabetic ciphers of this type are clearly useless.

Useless or not, one can present a superficially convincing argument for monoalphabetic substitution. It could be correctly noted that there are approximately 4×10^{26} possible plaintext to ciphertext alphabet equivalents using this system. (This, of course, is the number of permutations possible in a 26 character alphabet.) Therefore, even if a fast computer could be found that would check, say, one billion trial solutions per second, it would still take over ten billion years to exhaust all the possibilities. These are impressive but totally meaningless statistics. Presenting the cryptanalyst with a large number of possibilities is a necessary but not a sufficient condition for cryptographic success.

Improved security may be obtained by the use of polyalphabetic ciphers, which may be demonstrated using the Vigenère tableau of table 3. (The Vigenère tableau is named after the French cryptographer Blaise de Vigenère who popularized the

ciphertext alphabet designator	plaintext alphabet: A B C D	– – – – –	X Y Z
A	A B C D	– – – – –	X Y Z
B	B C D E	– – – – –	Y Z A
C	C D E F	– – – – –	Z A B
D	D E F G	– – – – –	A B C
.	. . . .		
.	. . . .		
.	. . . .		
X	X Y Z A	– – – – –	U V W
Y	Y Z A B	– – – – –	V W X
Z	Z A B C	– – – – –	W X Y

Table 3: The Vigenère tableau is used to generate a polyalphabetic cipher. To encipher, the plaintext message is first written out. Then the keyword is repeatedly written on top of the plaintext. The ciphertext is obtained by selecting the letter which is at the intersection of the plaintext alphabet column and the keyword character row.

key:	P	A	T	R	I	C	I	A	Z	L	O	T	N	I	K	P	A	T	R	----
plaintext:	M	A	Y	U	P	B	I	D	P	R	I	C	E	T	W	E	N	T	Y	----
ciphertext:	B	A	R	L	X	D	Q	D	O	C	W	V	R	B	G	T	N	M	P	----

Table 4: An example of the encryption process using the Vigenère tableau shown in table 3.

method although he did not invent it.) This table is bordered by the plaintext alphabet at the top and ciphertext alphabet designators at the left. The ciphertext alphabets in the body of the table are merely rotations of the normal alphabet. Enciphering is done by writing the key phrase repeatedly over the plaintext and enciphering each plaintext character by the corresponding keyphrase alphabet designator. In the example shown in table 4, letter M is enciphered from alphabet P, letter A is enciphered from alphabet A, letter Y from T, etc. By switching alphabets in this way we frustrate the simple frequency analysis which was so effective in the previous cipher example. Clearly, any given plaintext letter (such as E) has a different ciphertext equivalent in each of the different alphabets.

The cryptanalyst can attack this system by searching for the repeating key length (in this case 15). Once the keylength is established, he or she will rearrange the ciphertext in matrix form in which the row length is equal to the keylength. The columns of this matrix each involve the same ciphertext alphabet. Frequency analysis by columns soon reveals the specific key used and the whole structure then collapses.

One ploy sometimes used to frustrate the cryptanalyst is to use a coherent running key. The key could be taken from a readily available book, for example. By this method, the repetitions of the key are eliminated and the cryptanalyst is forced to work harder for a solution, which he or she can get, given enough cryptogram material and time.

A very significant advance in cryptography was introduced by a concept which may be generally described as *autokey*. In this system, the plaintext itself is used as the key. A given plaintext character selects the alphabet for encipherment of the next plaintext character, and so forth. One of the problems of using autokey is that the key and the recovered plaintext are one and the same. Thus the system tends to self-destruct after the first error. The error propagation properties of autokey are often cited as the reason for not using this technique in field ciphers.

Transposition Ciphers

An important cipher class is the transposition cipher. As the name implies, the meaning of the message is hidden because the order of the characters is scrambled in the ciphertext. To demonstrate transposition, we again call upon our friend Patricia, but this time her name is written out completely to form the keyphrase. The letters in the keyphrase are then numbered according to alphabetical order. When two or more identical letters exist, they are sequentially numbered from left to right. When this is done, there results a scrambled set of integers from 1 to the number of characters in the keyphrase (in this case 15). The message is then written under these column designators in rows of keyphrase length. An example for the demonstration key and message is shown in table 5.

Once this is done, the ciphertext is read out in column order: ANC, DCN, BEE, etc. When put in the standard 5 letter groups, the cryptogram becomes:

```
ANCDC  NBEEP
PNIRO  TTWRR
NYENI  TMEAU
YOYTT  COPEL
```

Since the deciphering clerk knows both the key and message lengths, he or she can quickly determine the length of each column in the original matrix. The cryptogram is then copied in column form and the message read out by rows. Multiple transpositions are often done using the same or different keyphrases. Null cells in the transposition matrix are sometimes used to strengthen the cipher.

Substitution ciphers replace characters but leave them in their original positions. The cryptanalyst can use this invariant to advantage. Transposition destroys the order but does not hide the content. Combinations of transposition and substitution can provide complementing strengths to produce very effective ciphers.

key:	P	A	T	R	I	C	I	A	Z	L	O	T	N	I	K
column order:	11	01	13	12	04	03	05	02	15	08	10	14	09	16	07
	M	A	Y	U	P	B	I	D	P	R	I	C	E	T	W
	E	N	T	Y	P	E	R	C	E	N	T	O	N	T	R
	A	C	T	O	N	E	O	N	L	Y					

Table 5: A transposition table arranged for the keyword Patricia Zlotnik and the example message "May up bid price twenty percent on tract one only." In the transposition method, the keyword is first written out and numbered in alphabetical order. The message is then written in columns under the keyword. The resulting columns are read out in numerical order to produce the ciphertext.

Playfair Cipher

It is interesting to consider briefly an

K	X	J	E	Y	U	R	E	B	E	X	E	L	W	A	O	H	W	U	W
Z	W	E	H	E	W	R	Y	T	U	Y	Z	M	W	I	H	O	M	N	E
H	E	Y	F	S	K	R	E	H	E	O	B	T	F	W	M	S	S	P	I
G	O	Y	F	I	W	T	T	T	U	A	J	L	U	O	E	A	O	N	G
O	L	K	S	Y	C	A	J	P	O	O	O	F	C	M	F	E	X	T	T
B	O	T	E	I	Z	O	N	T	X	C	W	C	F	Z	Y	I	P	T	F
B	Y	B	N	T	G	O	N	E	Y	E	O	B	H	M	W	E	M	O	C
C	U	Z	W	R	G	D	S	O	N	S	A	W	C	Z	S	N	Y	N	W
S	X	B	O	U	Y	W	R	H	E	M	G	X	E	L	H	E	Z	C	U
B	A	A	H	Y	U	S	E	D	Q	F	N	Z	Y	L	N	S	B	T	B

Table 6: The two messages shown here were sent by coastwatchers in the South Pacific during World War II. The first message uses "ROYAL NEW ZEALAND NAVY" as the key and the second message uses "PHYSICAL EXAMINATION." These messages follow the Playfair cipher rules except that letter pairs, when falling in a digraph, were left unenciphered.

important contribution to cryptography made by Charles Wheatstone of electrical measurement fame. Reference is made here to the famous Playfair cipher (named, ironically, after the man who enthusiastically promoted Wheatstone and his idea). The ciphertext alphabet is written as in the monoalphabetic example but is reformatted to a 5 by 5 square with I,J occupying the same cell and used interchangeably. Our demonstration key would yield:

P	A	T	R	I/J
C	Z	L	O	N
K	B	D	E	F
G	H	M	Q	S
U	V	W	X	Y

Enciphering is done by letter pairs with the following four rules:

- If the plaintext pair falls in the corners of a *square*, use as the ciphertext the other two corner characters taken in corresponding row order.
- If the plaintext pair falls in the same row, take as the ciphertext the characters immediately to the right of each plaintext character in order. Consider each row to have cylindrical continuation so that the character to the right of the last character in a row is the first character of that row.
- If the plaintext pair falls in the same column, take as the ciphertext the character immediately below each plaintext character in order. Consider each column to have cylindrical continuation so that the character below the last character in a column is the first character in that column.
- Encipher double letters by inserting an X between the letter pair in the plaintext.

Deciphering merely reverses the above procedure. We have here one of those operations that is quicker to execute than to explain. Using the demonstration keyword square and the demonstration message yields:

```
H T U V A   K T F A I
P N D R X   D L I U I
Q O O K L   I N C R I
P Z R L O   F N C N W
```

This digraphic substitution procedure can be very effective considering its relative simplicity. The reasons for this may be seen from the fact that while there are only 26 characters in the alphabet, there are 676 digraphs (combinations of two letters). The highest letter frequencies are 12% (E) and 9% (T). The highest digraph frequencies are 3¼% (TH) and 2½% (HE). The cryptanalyst thus faces many more entities with a much more uniform frequency distribution in the Playfair than in the character-for-character processing examples given previously.

The Playfair can, of course, be broken, and had the Japanese done this in World War II for the two cryptograms in table 6, the course of contemporary American history might have been radically changed. These cryptograms were sent by coastwatchers in the South Pacific. There is no clear call to action as far as the first message is concerned. However, the reader must surely agree that the second message required immediate action. This is especially true since the Japanese had adequate vessels and troops in the area to resolve the matter without difficulty. Both messages follow the Playfair rules except that letter pairs, when falling in a digraph, were left unenciphered. Even though these messages were (apparently) not deciphered and acted upon, military history is replete with examples in which the course of events was dramatically changed by poor cryptographic practice or by brilliant cryptanalysis. (These messages are taken from the Kahn reference which contains fascinating stories of this type.)

Vernam Cipher

The only cipher generally accepted as being absolutely secure is the invention of an American, Gilbert S Vernam. His system is known in the trade as the onetime key or onetime pad. Some perspective on the contribution made to cryptography by this man may be gained by noting that his system, for which patents were filed in 1918, is the standard system used today, 61 years later, on the Washington to Moscow hot line. Vernam's work involved Exclusive OR operations with a random binary key. An equivalent set of operations is presented

encipher

key:	15(P)	0(A)	19(T)	17(R)	8(I)	–	–	–
plaintext:	+12(M)	+0(A)	+24(Y)	+20(U)	+15(P)	–	–	–
ciphertext:	1(B)	0(A)	17(R)	11(L)	23(X)	–	–	–

decipher

ciphertext:	1(B)	0(A)	17(R)	11(L)	23(X)	–	–	–
key:	−15(P)	−0(A)	−19(T)	−17(R)	− 8(I)	–	–	–
plaintext:	12(M)	0(A)	24(Y)	20(U)	15(P)	–	–	–

Table 7: When all letters of the alphabet are numbered sequentially, messages may be enciphered and deciphered by adding together the numerical values of the plaintext and the keyword (modulo 26) to obtain the ciphertext. The deciphering process is performed by subtraction.

here except that a different base for the residue arithmetic is used.

Return now to table 3. Let the letters of the alphabet be replaced by the numbers 0 through 25. That is, A = 0, B = 1, C = 2, . . ., Y = 24, Z = 25. When this is done it will be immediately noted that in numerical form each of the ciphertext alphabets is equal to the plaintext alphabet plus the value of the ciphertext alphabet designator, modulo 26. In residue arithmetic all numbers lie in the range of 0 to 1 minus the base value. The base is repeatedly added to or subtracted from any arithmetic result until this range is achieved. For example, alphabet D (value 3) equivalents are obtained by adding 3 to the plaintext or alphabet A values. Once this numerical format is established, tables such as that of table 3 are no longer needed, since encipherment and decipherment may be done as shown in table 7 by simple addition and subtraction. The arithmetic used in this case is modulo 26.

Vernam realized that under heavy traffic loads substitution ciphers all broke down via the Achilles heel of the key, be it repeating keyphrase, coherent running key, or autokey. His solution to the problem was to generate a truly random key, make two or more copies, and arrange for the used key to be destroyed at both ends of the system after first use. In some cases the key is in paper tape format and a knife is provided at the exit position of the paper tape reader so that the keytape is destroyed automatically as soon as it is read (ie: a onetime tape). In other cases the key is written on pads of paper (digits 0 thru 9, base 10 system) and the sheets of the pad are torn off and destroyed as soon as each is used (ie: a onetime pad).

Trap Door Operations

The bulk of the open literature in the field of cryptography today takes us chronologically to the end of World War II. The state of cryptographic art at that time was represented by the mechanical and electromechanical cipher machines. Some punch card sorting mechanization for cryptanalysis is also occasionally referenced. The security curtain has since fallen, and quite obviously that curtain hid a revolution in cryptography brought about by solid-state digital data processing technology. Until very recently this concrete curtain quietly separated two coexisting computer user groups. The emergence of large commercial data networks and the need for preserving the privacy of data in transmission and storage has resulted in cryptographic work on both sides of that curtain. Topics such as the one reviewed in this section have apparently opened an uneasy dialog between these two groups.

Residue arithmetic, as used by Vernam and demonstrated in the simple example of the previous section, plays a key role in some recent cryptographic techniques that have been disclosed. In these techniques the encryption key (which can be made public) is comprised of a pair of positive integers (E,N). The message is first converted by any consistent means to some integer number M between 0 and N-1. The encryption process is then:

$$C = M^E \text{ (modulo N)} \qquad (1)$$

The message number M is raised to the power E, the result is divided by N and the *remainder* forms the ciphertext number C, which represents the cryptogram. (In one published example, E = 9007 and N is 129 decimal digits in length. This is residue arithmetic with a vengeance!)

The deciphering key (which is kept secret) involves two integer numbers (D,N), and the decryption process is:

$$M = C^E \text{ (modulo N)} \qquad (2)$$

The ciphertext value C is raised to the power D, division by N is then done, and the *remainder* is the original message number M. This can be converted back to alphanumeric format for final delivery.

A 3 step process is used to generate N, D and E.

- Generate two random prime numbers P,Q (of the order of 100 decimal digits each in a practical system) and let N = PXQ. Thus N is typically a 200 decimal digit composite number.
- Select number D to be relatively prime to (P-1) X (Q-1). Any prime number greater than both P and Q is a possible selection.
- Select an E value such that the product E X D equals unity, modulo the product (P-1) X (Q-1).

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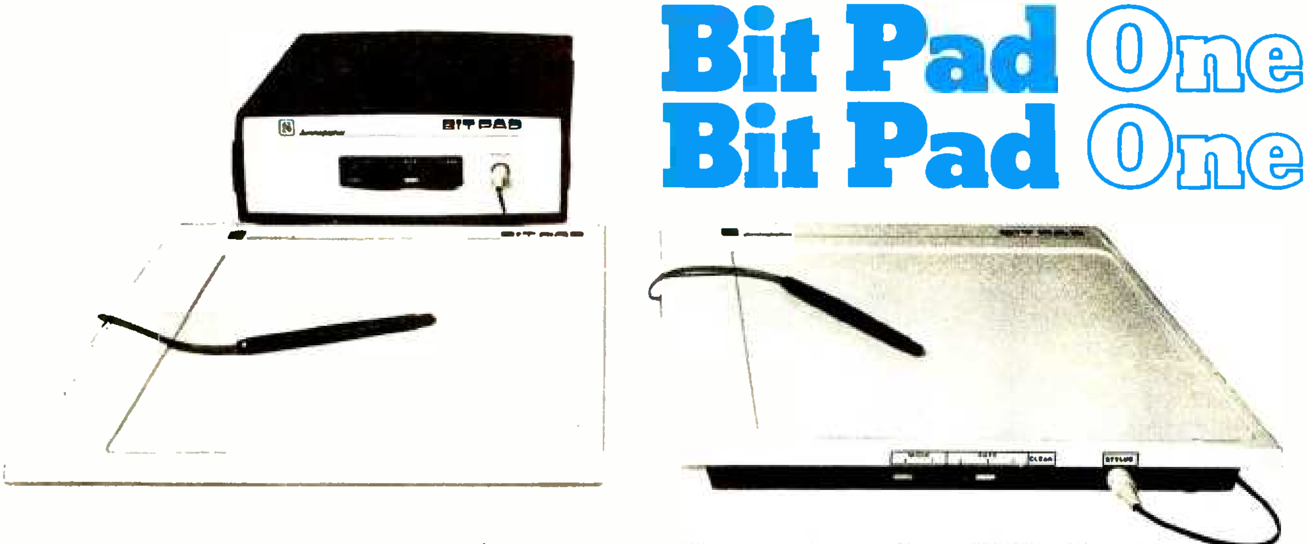

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This cryptographic process is novel in that knowledge of the enciphering process (E,N) does not reveal the deciphering process (D,N). The terms *one-way* and *trap door* have been applied to such operations. This is to be compared to the cryptographic processes we have been discussing in which knowledge of the key allows one to go in either direction between plaintext and ciphertext with equal ease. Consider now two parties to a transaction: a customer C and a bank B. Let Ec and Eb be the (public) encryption processes of the customer and bank, respectively. Let Dc and Db be the (secret) corresponding decryption processes.

The customer may take a funds transfer order T in plaintext and apply his secret *decoding* operation to it to produce Dc(T). This transformation may be converted by anyone back to T by applying the public Ec operation. For transmission to the bank, however, the customer encrypts Dc(T) by applying the bank's (public) encryption operation Eb. Thus

$$Eb[Dc(T)]$$

is transmitted to the bank. Interception of the message at this point may be tolerated since only the bank can decipher the Eb operation. Once this is done the bank has Dc(T) to which the bank may easily apply the customer's public encryption operation, Ec, to obtain the plaintext T. That is:

$$T = Ec(Dc(T))] \qquad (3)$$

is done at the bank.

Three important features are to be noted. First, the data was protected in transit by the bank Eb operation. The bank is sure of the sender's identity from equation (3) because only c knows the *backward* Dc operation which was applied to T. Also the bank cannot alter T after receipt since Dc(T) stands as verification. The bank cannot produce a Dc(T') to correspond to some altered T' funds transfer order.

The security of these systems is dependent to a great extent on the computational difficulty of factoring the compound number N. It is claimed that this procedure is *computationally infeasible* for sufficiently large values of N using the best algorithms and the fastest computers. (The presentation in this section follows very closely material recently published by R L Rivest and his associates at MIT.)

In part 2 of this article I will discuss program Crypto which performs substitution and transposition. This part shows how a calculator can be converted to a field cipher machine of significant capability.■

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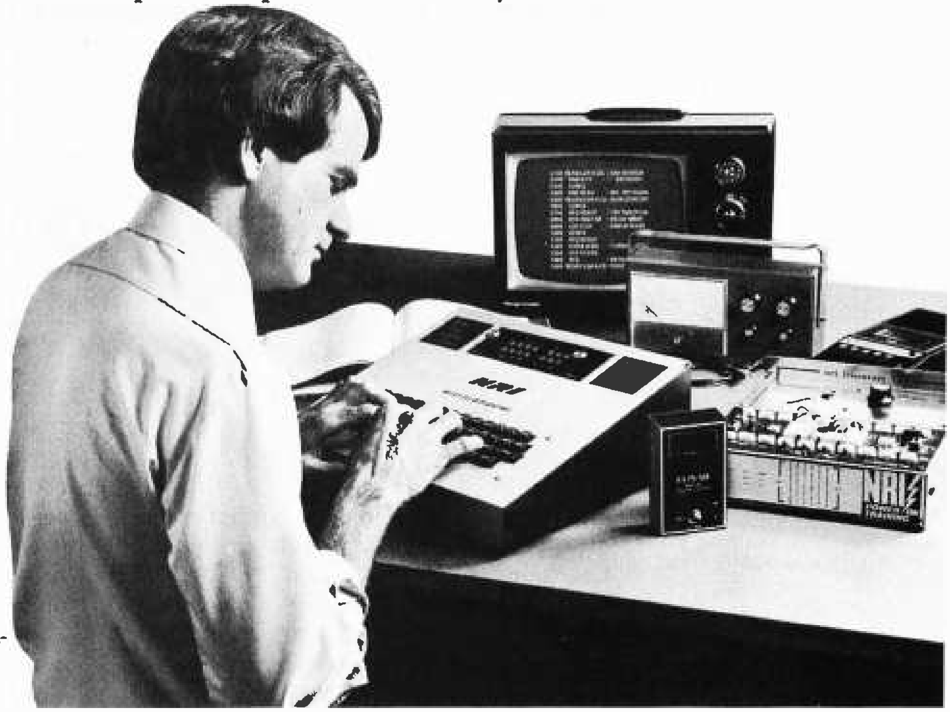

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The Standard Data Encryption Algorithm

Part 1: An Overview

Robert V Meushaw
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Recently, I have seen many articles describing new commercial encryption equipment using the Standard Data Encryption Algorithm. There have also been recent announcements of integrated circuits, like the Intel 8294, which implement the standard. The Standard Data Encryption Algorithm has been published by the National Bureau of Standards for use in the protection of computer data. The algorithm is described in FIPS Publication 46, available from the US Department of Commerce. After months of being bombarded with publicity regarding the encryption method, it finally struck me that I had found a perfect project for my KIM. The challenge became to implement the algorithm with the basic memory provided and to achieve sufficient processing speed to make it practical for use by others. Along the way, I hoped to investigate the advantages and disadvantages of the 6502 in performing the necessary tasks.

Cryptography Basics

Cryptography involves the use of a scheme to transform intelligible text into an unintelligible form and to later recover the original text. The transformation process is known as *encryption* and the recovery process is known as *decryption*. Cryptographic techniques have been used for centuries to allow individuals to communicate without fear of outsiders discovering what they are saying. The individuals who communicate generally possess a cryptographic *key* which controls the encryption and decryption process. Unless someone knows the key used to encrypt the data, he or she will not be able to correctly decrypt the data. The number of possible keys is usually made so large that it is impractical to try decrypting the data using all key possibilities. It must be clear that the critical factor in protecting the data is the secrecy of the key used.

The cryptographic technique employed in the Standard Data Encryption Algorithm is known as a *codebook*. In this case, a 64 bit block of data is transformed to a corresponding 64 bit block of data known as a *cipher*. Each time a particular set of data is provided as input, the same cipher will result: assuming the same key is used. The Standard Data Encryption Algorithm uses a 56 bit key to control the encryption. As mentioned before, this was chosen to give a large number of possible keys (ie: 2^{56}). Some estimates have been made that it would require, on the average, approximately 2500 years on a general purpose computer significantly faster than a CDC 7600 to examine all 2^{56} (ie: 7.2×10^{16}) possible keys in order to determine the particular key used to encrypt a block of data.

Restrictions

The National Bureau of Standards position on the implementation of the Standard Data Encryption Algorithm is that software implementations are not in compliance with the standard. The standard, however, applies to use on federal systems, not private computers. If you have any reservations concerning your intended use of this method, check the applicable regulations.

Algorithm Overview

A very simple diagram of the operations involved in the encryption algorithm is shown in figure 1. The input (plaintext) is first subjected to an initial permutation operation, which reorders the bits. Most of the work of the encryption is done in the box labeled product transformation. Details of this transformation will be described later. The block transformation is a simple exchange of the left and right 32 bits of data. The last step is a permutation operation which is the inverse of the initial permutation operation. The output of this step is the *ciphertext*.

In case you're wondering where the key comes in, it is the controlling factor in the product transformation. Note also the relationship of the initial permutation to its inverse. The fact that they are inverses means that if you perform an operation using a function and then reorder again using the inverse of the function, the result will be the original word. Of course the same thing occurs if the inverse and then the function is applied to the word. Tables 1a and 1b show the permutation tables for the initial permutation and its inverse. The permutation operation should be interpreted as follows: proceeding from left to right, bit 1 of the permuted word is bit 58 of the input, bit 2 of the permuted word is bit 50 of the input, etc. I was originally confused about the numbering scheme chosen for the bits, since I was accustomed to bits being numbered 0 thru 7 going from right to left. The correspondence between the Standard Data Encryption Algorithm numbering scheme and typical computer numbering is depicted in figure 2.

Algorithm Operation

A more detailed diagram of the encryption algorithm is provided in figure 3. The basic operations are quite straightforward. What is shown is basically an expansion of the product transformation box from figure 1.

Let's look at the basic operations involved after the initial permutation. The 64 bits of permuted input are split into two groups of 32 bits each, called left (L) and right (R). The subscripts on L and R indicate the iteration of the algorithm. The first thing that occurs is the generation of K1. K1 is known

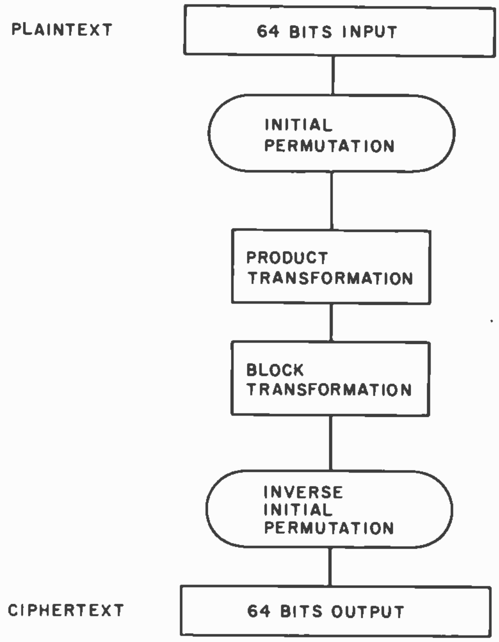


Figure 1: An overview of the Standard Data Encryption Algorithm.

(1a)

58	50	42	34	26	18	10	2
60	52	44	36	28	20	12	4
62	54	46	38	30	22	14	6
64	56	48	40	32	24	16	8
57	49	41	33	25	17	9	1
59	51	43	35	27	19	11	3
61	53	45	37	29	21	13	5
63	55	47	39	31	23	15	7

(1b)

40	8	48	16	56	24	64	32
39	7	47	15	55	23	63	31
38	6	46	14	54	22	62	30
37	5	45	13	53	21	61	29
36	4	44	12	52	20	60	28
35	3	43	11	51	19	59	27
34	2	42	10	50	18	58	26
33	1	41	9	49	17	57	25

Table 1: Permutation tables for the initial and inverse initial permutation (1a and 1b respectively). The initial permutation table is read as follows: bit 1 of the input goes to bit 58 of the output, bit 2 of the input goes to bit 50 of the input, etc.

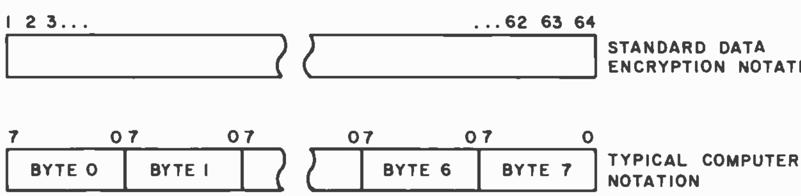
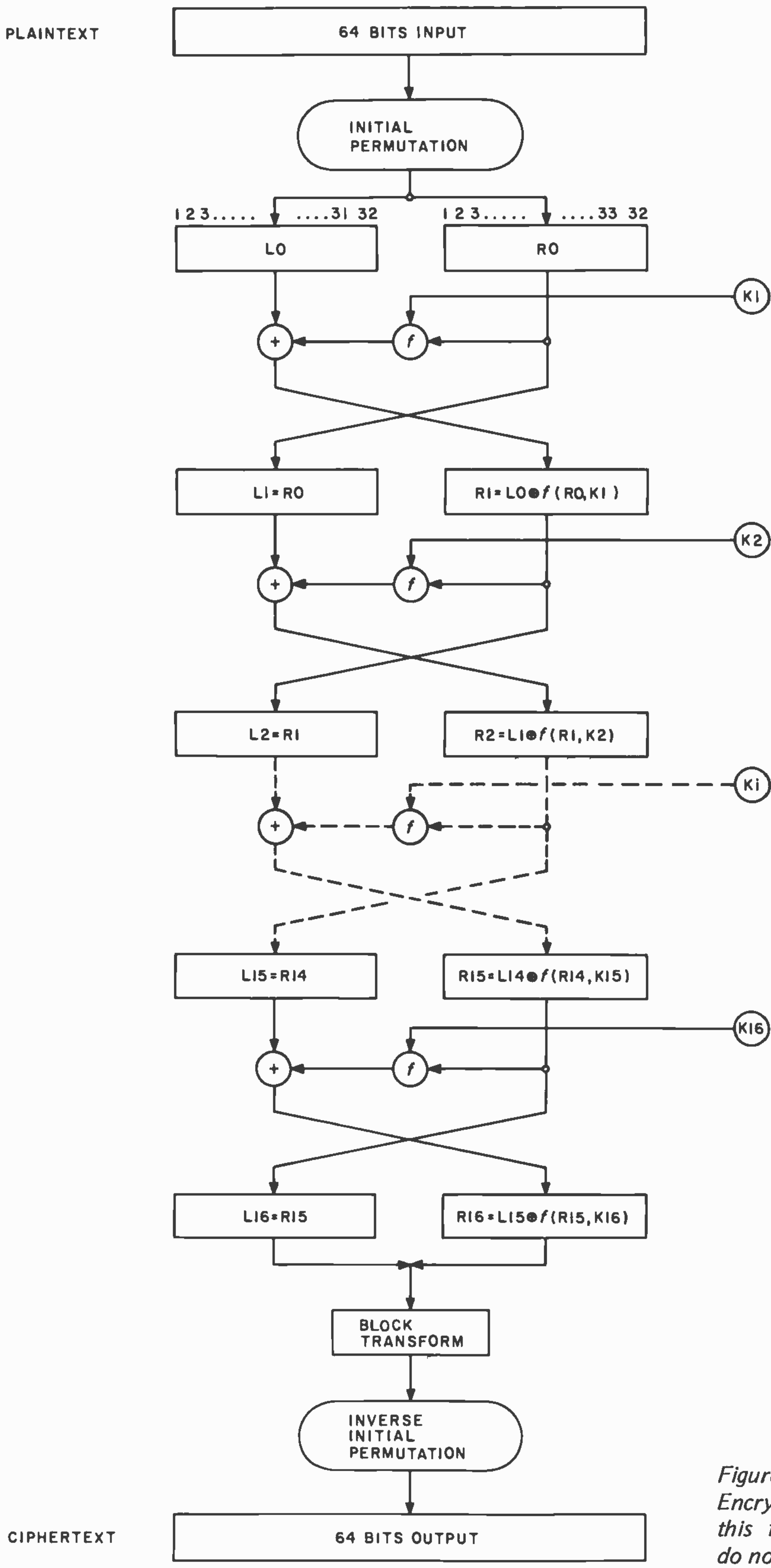


Figure 2: Corresponding numbering between the Data Encryption Standard and typical microcomputer bit numbering.



as the *subkey*, and is generated directly from the encryption key. In fact, each Ki is generated from the key. Don't worry yet about exactly what each Ki is or where it comes from — that will soon be explained. A function, f(R0, K1), is now generated using K1 and R0 as inputs (again, the details will be explained shortly). The next operation is the modulo 2 addition (ie: exclusive OR) of f(R0, K1) to L0. Therefore, L0 ⊕ f(R0, K1) replaces the old L0. Finally, the current leftmost 32 bits are exchanged with the current rightmost 32 bits. This completes one iteration of the algorithm and involves all the basic operations. To complete the product transformation, the steps above are repeated as shown in figure 3. The encryption process is completed by performing the block transformation and the inverse initial permutation operation.

An important fact about the modulo 2 addition step is that it is reversible. This reversibility allows the decryption process to recover the original plaintext. In fact, as I will show, you can use the same algorithm steps to do the decryption as you used for encryption.

Something for Nothing?

In case my arguments of the simplicity of the Standard Data Encryption Algorithm haven't convinced you, I should point out that it wouldn't be fair to expect 2500 years of protection from an algorithm which wasn't somewhat involved. Figures 4a and 4b provide illustrative examples of the encryption and decryption processes. I have used only two iterations in the product transformation, but the principle is the same for 16 iterations. Note in particular how the same algorithm is used for decryption, except that the subkeys are applied in reverse sequence. In figure 4b, the results of each transform are shown after the modulo 2 addition. For example, the first transform results of L1 are obtained by computing R2 ⊕ f(L2, K2) = [L1 ⊕ f(R1, K2)] ⊕ f(R1, K2) = L1. Remember how modulo 2

Figure 3: A detailed operation of the Standard Data Encryption Algorithm encryption process. Note that this flow diagram (and the following flow diagrams) do not use standard flowchart symbology.

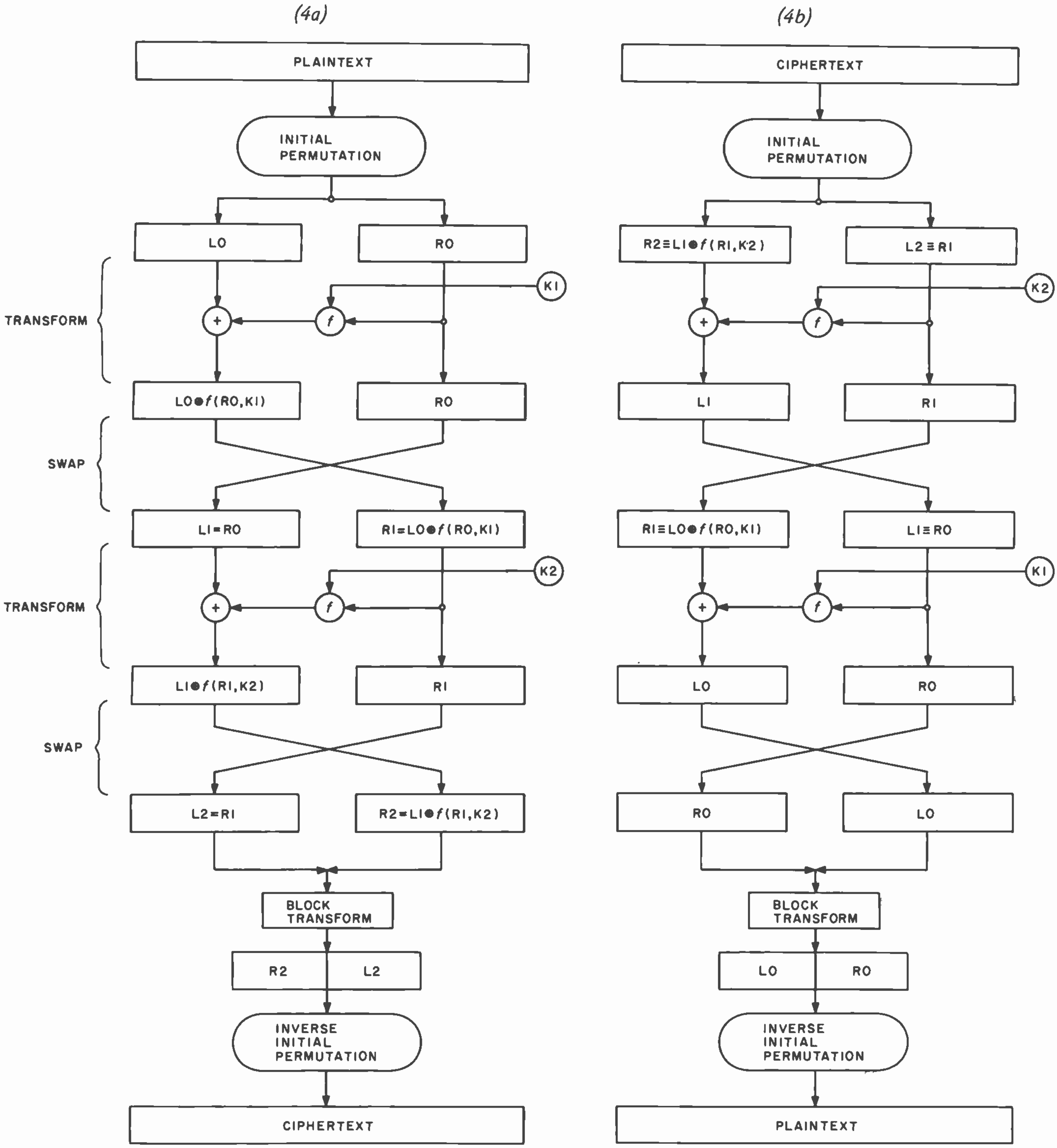


Figure 4: A simplified encryption and decryption process using the Standard Data Encryption Algorithm. Figure 4a shows a plaintext message being processed into a ciphertext and figure 4b shows the inverse process. Although only two iterations of transformation and swapping are shown, 16 are actually performed.

addition works. Following the decryption through figure 4b, you can see how the encryption steps are reversed. The result is the original plaintext.

Algorithm Details

In order to program the encryption algorithm, it is necessary to understand the details of two operations that I have alluded to. The first is the generation of the subkeys K1, K2, . . . K16; the second is the generation of the function f (R,K).

Subkey generation is depicted in figure 5. The process starts with the 64 bit key that you provide for the encryption. Actually, only 56 of these bits are used; the remaining eight can be used as parity bits. The first transformation of the key is called permuted choice 1. Permuted choice 1 permutes the 56 bit key and also regroups it into two 28 bit words, called C0 and D0. The generation of subkey K1 is done by circular shifting both C0 and D0 left and then permuting

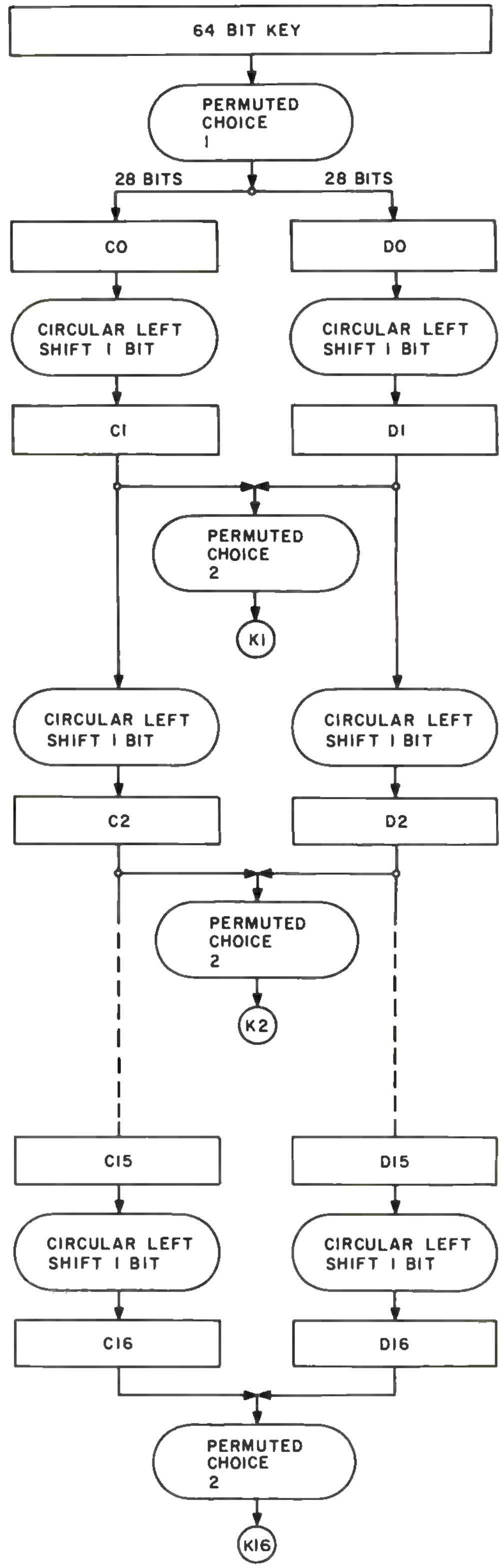


Figure 5: A process flow diagram showing how subkeys K1 thru K16 are produced from a single key.

Table 2: Tables for using permuted choice 1 and permuted choice 2 (table 2a and 2b respectively). The permuted choice 1 table (table 2a) is used to develop C0 and D0 from the key. Bits 8, 16, 24, 32, 40, 48, 56, and 60 of the key are not used. The permuted choice 2 table (table 2b) is used to develop subkey Ki from Ci and Di.

(2a)

64 Bit Key

57	49	41	33	25	17	9
1	58	50	42	34	26	18
10	2	59	51	43	35	27
19	11	3	60	52	44	36

63	55	47	39	31	23	15
7	62	54	46	38	30	22
14	6	61	53	45	37	29
21	13	5	28	20	12	4

C0
28 Bits

D0
28 Bits

(2b)

Ci
28 Bits

Di
28 Bits

14	17	11	24	1	5
3	28	15	6	21	10
23	19	12	4	26	8
16	7	27	20	13	2
41	52	31	37	47	55
30	40	51	45	33	48
44	49	39	56	34	53
46	42	50	36	29	32

Subkey Ki
48 Bits

Iteration Number	Number of Circular Left Shifts
1	1
2	1
3	2
4	2
5	2
6	2
7	2
8	2
9	1
10	2
11	2
12	2
13	2
14	2
15	2
16	1

Table 3: A summary of the number of left circular shifts applied to Ci and Di at each iteration of subkey generation.

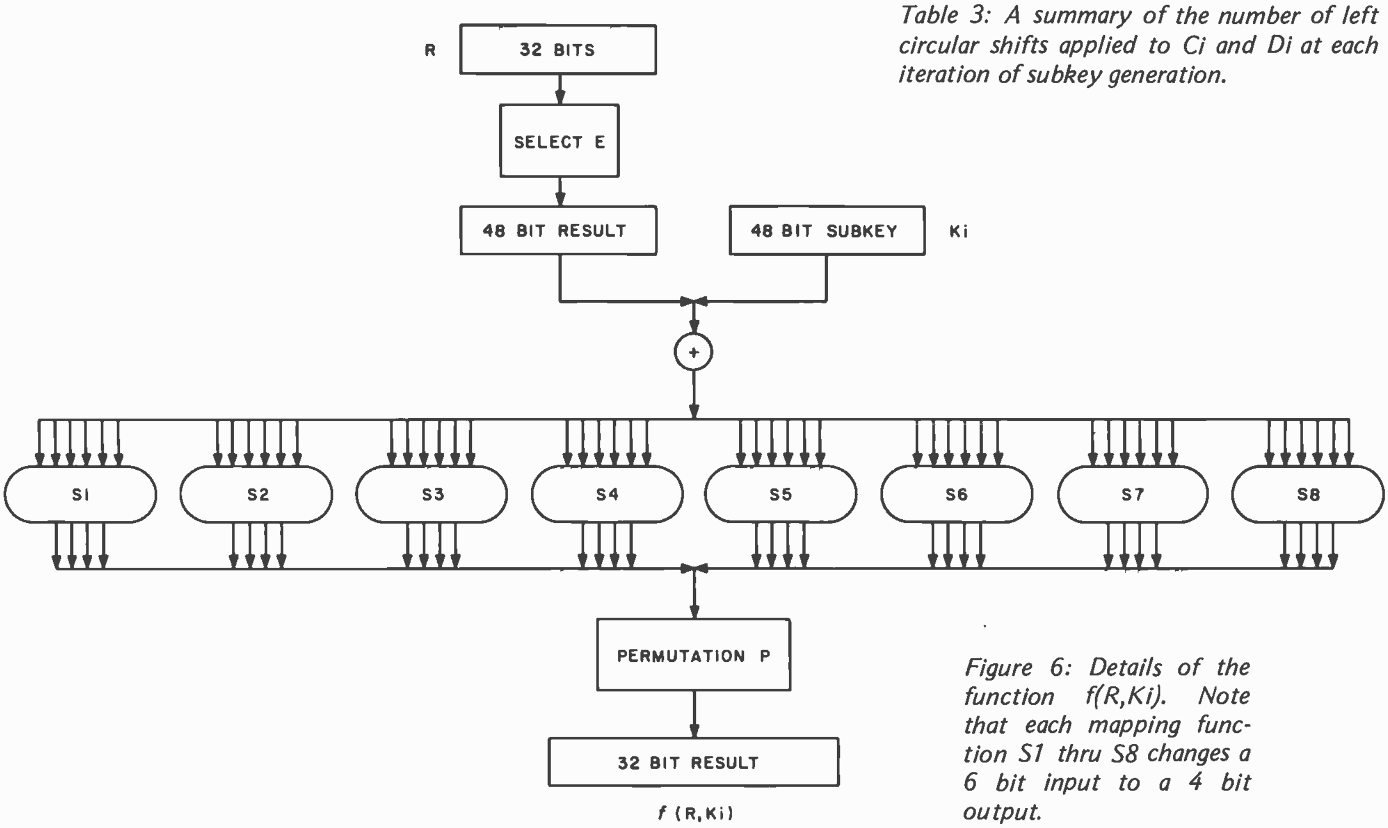


Figure 6: Details of the function f(R,Ki). Note that each mapping function S1 thru S8 changes a 6 bit input to a 4 bit output.

C1 and D1 using permuted choice 2 to form a 48 bit subkey. Permuted choice 1 and permuted choice 2 are shown in tables 2a and 2b. Each successive subkey is generated in the same way: by shifting Ci and Di left (by one or two bits) and then using permuted choice 2. Table 3 shows the number of left shifts to be applied to Ci and Di for each iteration in the subkey generation.

Once K1, K2, . . ., K16 have been generated, it is not necessary to generate them again until the key is changed. The same set of subkeys is used for each encryption and decryption operation shown in figures 4a and 4b.

The final operation to understand is f (R,K), depicted in figure 6. The first operation is called select E. This is really a permutation operation similar to the initial permutation operation previously discussed, except that the result has more bits than the input. Table 4 shows the select E permutation table. The 48 bit result of this operation is then added modulo 2 to the subkey. This result is reduced to a 32 bit result using a set of mapping functions known as S1, S2, . . .,S8. These are used as shown in figure 6. Each group of six bits, going left to right, is mapped into a 4 bit word using a distinct mapping function. The mapping functions are shown in figure 5, and an example of how they are used is shown in figure 6. The six bits input to each S mapping function are used to generate a row address and column address as shown. The selected matrix entry is converted from its

S_1

14	4	13	1	2	15	11	8	3	10	6	12	5	9	0	7
0	15	7	4	14	2	13	1	10	6	12	11	9	5	3	8
4	1	14	8	13	6	2	11	15	12	9	7	3	10	5	0
15	12	8	2	4	9	1	7	5	11	3	14	10	0	6	13

S_2

15	1	8	14	6	11	3	4	9	7	2	13	12	0	5	10
3	13	4	7	15	2	8	14	12	0	1	10	6	9	11	5
0	14	7	11	10	4	13	1	5	8	12	6	9	3	2	15
13	8	10	1	3	15	4	2	11	6	7	12	0	5	14	9

S_3

10	0	9	14	6	3	15	5	1	13	12	7	11	4	2	8
13	7	0	9	3	4	6	10	2	8	5	14	12	11	15	1
13	6	4	9	8	15	3	0	11	1	2	12	5	10	14	7
1	10	13	0	6	9	8	7	4	15	14	3	11	5	2	12

S_4

7	13	14	3	0	6	9	10	1	2	8	5	11	12	4	15
13	8	11	5	6	15	0	3	4	7	2	12	1	10	14	9
10	6	9	0	12	11	7	13	15	1	3	14	5	2	8	4
3	15	0	6	10	1	13	8	9	4	5	11	12	7	2	14

S_5

2	12	4	1	7	10	11	6	8	5	3	15	13	0	14	9
14	11	2	12	4	7	13	1	5	0	15	10	3	9	8	6
4	2	1	11	10	13	7	8	15	9	12	5	6	3	0	14
11	8	12	7	1	14	2	13	6	15	0	9	10	4	5	3

S_6

12	1	10	15	9	2	6	8	0	13	3	4	14	7	5	11
10	15	4	2	7	12	9	5	6	1	13	14	0	11	3	8
9	14	15	5	2	8	12	3	7	0	4	10	1	13	11	6
4	3	2	12	9	5	15	10	11	14	1	7	6	0	8	13

S_7

4	11	2	14	15	0	8	13	3	12	9	7	5	10	6	1
13	0	11	7	4	9	1	10	14	3	5	12	2	15	8	6
1	4	11	13	12	3	7	14	10	15	6	8	0	5	9	2
6	11	13	8	1	4	10	7	9	5	0	15	14	2	3	12

S_8

13	2	8	4	6	15	11	1	10	9	3	14	5	0	12	7
1	15	13	8	10	3	7	4	12	5	6	11	0	14	9	2
7	11	4	1	9	12	14	2	0	6	10	13	15	3	5	8
2	1	14	7	4	10	8	13	15	12	9	0	3	5	6	11

Table 5: Matrices for the selection functions S1 thru S8. Each Si maps a 6 bit input into a 4 bit output.

Table 4: The Select E permutation table. The output contains more bits than the input in order to match length of subkey.

Input to Select E 32 Bits

32	1	2	3	4	5
4	5	6	7	8	9
8	9	10	11	12	13
12	13	14	15	16	17
16	17	18	19	20	21
20	21	22	23	24	25
24	25	26	27	28	29
28	29	30	31	32	1

Output from Select E 48 Bits

Table 6: Illustration of the use of S1 mapping function. The middle four bits of input give the column index. The first and last bits are the row index. The binary value of the selected table entry is output.

0 1 000 1 Input to S1

Column Number

Row Number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
00	14	4	13	1	2	15	11	8	3	10	6	12	5	9	0	7
01	0	15	7	4	14	2	13	1	10	6	12	11	9	5	3	8
02	4	1	14	8	13	6	2	11	15	12	9	7	3	10	5	0
03	15	12	8	2	4	9	1	7	5	11	3	14	10	0	6	13

10 10 Output from S1

Output from S1 thru S8
32 Bits

16	7	20	21
29	12	28	17
1	15	23	26
5	18	31	10
2	8	24	14
32	27	3	9
19	13	30	6
22	11	4	25

f(Ri, Ki)
32 Bits

Table 7: Table for permutation P.

decimal representation to binary. A final 32 bit permutation, P, is then performed as shown in figure 6 to give the output f (R,K). Table 7 shows this permutation table.

This completes the details of the Standard Data Encryption Algorithm and should allow you to develop your own implementation. My particular implementation for the 6502 on the basic KIM-1 is given in part 2. It should provide you with some interesting insights into program optimization.■

Continued from page 53

March 19-21, Modern Integrated Circuits, George Washington University, Washington DC. This course is structured to meet the needs of engineers, scientists, and technical managers who desire a better understanding of the latest technological advances in the area of integrated circuits. As such it examines all aspects of integrated circuit technology, starting from fundamental principles of construction and operation, to the most recent devices, their characteristics and specifications. A significant part of the course deals with the application of integrated circuits in linear and digital systems. Specific topics to be covered include detailed design examples of circuits using operational amplifiers and active filters, as well as computer arithmetic units, registers, and memories. Contact George Washington University, Continuing Engineering Education Program, Washington DC 20052.

March 19-21, Project Management for Computer Systems, Atlanta GA. This seminar is designed for the computer oriented professional responsible for the development and implementation of complex EDP systems. The seminar will illustrate techniques for planning, implementing, installing, and controlling projects. Contact The University of Chicago, Center for Continuing Education, 1307 E 60th St, Chicago IL 60637.

March 21-23, Microcomputer Hardware and System Design Seminar, Holiday Inn, Palo Alto CA. Polytechnic Institute for New York and the Institute for Advanced Professional Studies are presenting this 3 day seminar for engineers, programmers and technical managers with a working knowledge of digital hardware design and familiarity with the underlying concepts governing microprocessor operation, architecture, and systems design. This seminar will cover the operation, architecture, instruction set, and design techniques for 8 bit microprocessors. Contact Prof Donald D French, Institute for Advanced Professional Studies, 1 Gateway Ctr, Newton MA 02158, (617) 964-1412.

March 25-28, Expo '79 Los Angeles Marriott, Los Angeles CA. Expo '79 is held in conjunction with the 16th Numerical Control Society Annual Meeting and Technical Conference. Contact Numerical Control Society, 1800 Pickwick Av, Glenview IL 60025, (312) 724-7700.

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March 26-28, Minicomputers and Distirbuted Processing, New York NY. This seminar will examine the uses, economics, programming and implementation of minicomputers. Current hardware and software will also be evaluated. Contact The University of Chicago, Center for Continuing Education, 1307 E 60th St, Chicago IL 60637.

March 26-30, Data Base Concepts and Design, AMA Management Center, Chicago IL. Sponsored by the American Management Associations, this course will feature practical information to help the participant understand structure, concepts, design, software, and management. Contact American Management Associations, 135 W 50th St, New York NY 10020, (212) 586-8100.

March 27-29, The Midwestern Computer Expo, McCormick Pl, Chicago IL. Exposition by the leading vendors of data processing equipment and services. Contact Lee Mulder, The Caravan Group, 60 Austin St, Newton MA, (617) 964-4550.

April 3-5, Specifications of Reliable Software, Hyatt Regency Hotel, Cambridge MA. This conference is sponsored by the IEEE Computer Society. Contact Douglas T Ross, Softech Inc, 460 Totten Pond Rd, Waltham MA 02154, (617) 890-6900.

April 5-6, Computers in Ophthalmology, St Louis MO. This is a course in application of computers to ophthalmic patient care and clinical reseach. Sessions dealing with data bases, automated patient testing, artificial intelligence, and image processing are being planned. Contact Robert Greenfield, DSc, Biomedical Computer Laboratory, Washing University School of Medicine, 700 S Euclid Av, St Louis MO 63110.

April 5-6, 1979 Computer Users Conference, East Texas State University, Commerce TX. The theme of this conference will be "Educating in a Computer Society." Contact Henrietta Gale, conference coordinator, Dept of Computer Science, East Texas State University, Commerce TX 75428.

April 9-11, Data Processing Operations Management, Miami FL. This seminar will emphasize the management skill and techniques applicable to the data processing operations function. The curriculum is designed toward practical, applied management techniques to provide a sounder understanding of the ways of managing data processing operations more effectively. Contact The University of Chicago, Center for Continuing Education, 1307 E 60th St, Chicago IL 60637.

April 9-12, Interface '79, McCormick Pl, Chicago IL. This is the seventh annual conference and exposition on data communications and computers. Contact The Interface Group, 160 Speen St, Framingham MA 01701.

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April 16-20, Data Communication Systems and Networks, George Washington University, Washington DC 20052. See March 5-9, Washington DC.

April 23-26, Middle Eastern Electronic Communications Show and Conference, Bahrain Exhibition Ctr, Bahrain. The exhibition will consist of companies marketing communication systems, products, and services. Contact Gerry Dobson, MECOM '79, Arabian Exhibition Management, 11 Manchester Sq, London W1M 5AB.

April 23-27, Data Base Concepts and Design, San Francisco CA. See March 26-30, Chicago IL.

April 24-26, Electro/79 Show and Convention, New York Coliseum and American Hotel. Contact William C Weber Jr, general manager, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo CA 90245.

April 30-May 2, First Annual International Conference on Computer Capacity Management, Washington DC. This conference is sponsored by the Institute for Software Engineering. Contact the Institute for Software Engineering, POB 637, Palo Alto CA 94302.

May 7-11, Data Base Concepts and Design, Kansas City KS. See March 26-30, Chicago IL.

May 15-17, Micro/Expo 79, Centre International de Paris, Paris FRANCE. Contact Sybex Inc, 2020 Milvia St, Berkeley CA 94704.

May 15-17, First Education Computer Fair, Detroit Plaza Hotel, Detroit MI. This fair will be held in conjunction with 1979 Association for Educational Data Systems 17th Annual Convention. The theme of the fair will be the use of microprocessors in education. Contact Bruce G Alcock, Riverdale Country School, W 253 St and Fieldston Rd, Bronx NY 10471.

May 15-18, 1979 Association for Educational Data Systems 17th Annual Convention, Detroit Plaza Hotel, Detroit MI. The convention program will focus on computer applications, computer resources, computer related curriculum, application development methodologies, and futures. Exhibits, user group meetings and vendor sessions will also be offered. Contact Arthur W Daniels Jr, 31202 Dorchester, Madison Heights MI 48071.

May 21-24, Eighth Annual Incremental Motion Control Symposium, Ramada Inn, Urbana IL. Contact Dr B C Kuo, POB 2772, Station A, Champaign IL 61820.

Northeast Personal and Business Computer Show, Hynes Auditorium, Boston MA. See BYTE's Bits, page 224, for information concerning change from previously published date.■

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APPENDIX A

Vol. III

Billing, Inventory, Payroll, Risk, Schedule 2, Shipping, Stocks, Switch

Vol. IV

Bingo, Bonds, Bull, Enterprise, Football, Funds 1, Funds 2, Go-Moku, Jack, Life, Loans, Mazes, Poker, Popul, Profits, Qubic, Rates, Retire, Savings, SBA, Tic-Tac-Toe

Vol. V

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APPENDIX B

Vol. VI

- **Ledger** — Maintains Company accounts and generates financial reports. Includes routines for: Pyrl, Inv, Depr, A/R, A/P.

Vol. VII

- **Chess** — Designed to challenge the average player, fairly comprehensive. Great fun for all, offers a unique opportunity for beginners in need of an opponent.
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- **Wdproc** — Wordprocessing for lawyers, publishers, writers, etc. Write, store, and change from rough draft to final copy in a variety of formats.
- **Utility** — Disk utility program with memory testing.

Vol. VIII

- **1040-Tax** — Taxpayers return, itemized deductions or standard
- **Balance** — Reconciles bank statements
- **Checkbook** — Balances your checkbook
- **Inst1 o 78** — Computes real cost on bank financed items; cars, boats, etc.
- **Deprec 2** — Computes depreciation, 4 methods, any time period

APPENDIX C — FAVORITE PROGRAM CONVERSIONS

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Preview of the Z-8000

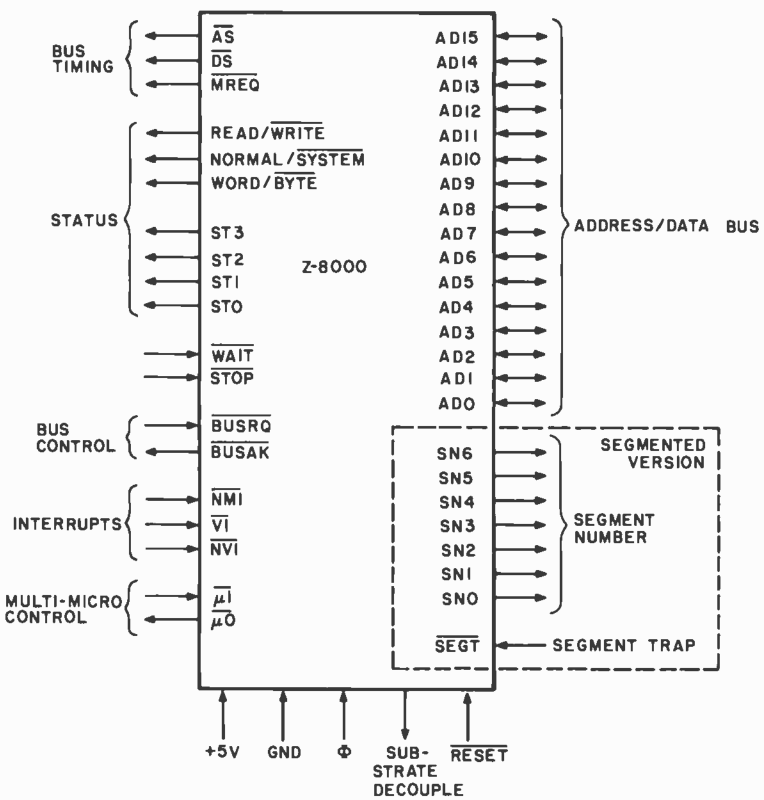
All figures in this article are courtesy of Zilog.

The Z-8000 (shown in figure 1) is Zilog's new entry in the field of 16 bit processors. It is a single chip processor with more raw processing power than many popular minicomputers. Benchmarked against the popular PDP-11 family, the Z-8000 is between the 11/45 and the 11/70 in speed for many simple instructions. The processor also introduces several sophisticated minicomputer hardware techniques such as memory management, separate system/user operation modes, separate memory space for data, stack contents and code, and long word instructions. The remainder of this review will offer a very brief description of the Z-8000 so that future thinking personal computer experimenters can begin planning applications for it.

Architecture

The Z-8000 is a general register machine with 1 and 2 address instructions, faintly reminiscent of a PDP-11. It comes in two varieties: segmented or nonsegmented, in reference to the memory management capability which will be discussed later. I will discuss only the segmented processor

Figure 1: Pin diagram of Zilog's new Z-8000 16 bit processor. The device is both fast and versatile, with over 110 instructions in its instruction set. The Z-8000 is availáble in two versions: segmented and unsegmented. The segmented version uses an outboard auxiliary integrated circuit called a memory management device to provide memory segment mapping or relocation and memory protection (the memory in the Z-8000 is divided into 64 K byte blocks called sections).



AD_{15}–AD_0	Address/data (inputs/outputs, active high, 3 state). These multiplexed, address/data lines are used both for I/O and to address memory.
$\overline{AS}$	Address strobe (output, active low, 3 state) indicates addresses are valid.
$\overline{BUSAK}$	Bus acknowledge (output, active low). A low on this line indicates the processor has relinquished the bus.
$\overline{BUSRQ}$	Bus request (input, active low). This line must be driven low to request the bus from the processor.
$\overline{DS}$	Data strobe (output, active low, 3 state). This line times the data in and out of the processor.
$\overline{MREQ}$	Memory request (output, active low, 3 state) is a timing signal that eases the interface to dynamic memories.
$\overline{\mu I}$	Multimicro in (input, active low) tests for the state of the multimicroprocessor request.
$\overline{\mu O}$	Multimicro out (output, active low).
$\overline{NMI}$	Nonmaskable interrupt (input, active low).
$\overline{NVI}$	Nonvectored interrupt (input, active low).
Φ	System clock is a transistor-transistor logic level clock input.
$\overline{RESET}$	Reset (input, active low) resets the processor.
$R/\overline{W}$	Read/write (output, low = write, 3 state) provides early status information for a read or write cycle.
SA_6–SA_0	Segment number (outputs, active high, 3 state).
$\overline{SEGT}$	Segmentation trap (input, negative edge triggered).
ST_3–ST_0	Status (outputs, active high). These lines specify the following statuses: memory request, stack pointer request, instruction fetch first word, instruction fetch subsequent words, internal operation or halt, VI acknowledge, NVI acknowledge, NMI acknowledge, I/O reference, refresh, segmentation I/O, set bootstrap, reset bootstrap.
$\overline{STOP}$	Stop (input, active low) single steps instruction execution.
$\overline{VI}$	Vector interrupt (input, active low).
$\overline{WAIT}$	Wait (input, active low) tells the processor that the memory or I/O device is not ready for data transfer.
$W/\overline{B}$	Word/byte reference (output).
$N/\overline{S}$	Normal/system mode (output).

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since the nonsegmented processor is a functional subset of the former. Nonsegmented mode is a software selectable option in the segmented processor.

The processor has sixteen 16 bit registers which are logically subdivided (figure 2) into sixteen 8 bit registers, eight 32 bit registers and four 64 bit registers. All of the 8 and 16 bit registers are available as general purpose accumulators. Fifteen of the 16 bit registers are available as index registers. Registers 14, or 14 and 15 serve as stack pointer depending on the segmentation mode in effect. There are two sets of these registers to provide for separate system and user stacks. There is a 64 bit status register which contains the program counter and various flags. There is also a rate programmable refresh counter for servicing dynamic memories.

There are seven discrete data types recognized by the Z-8000. In ascending order of size they are bits, BCD (binary coded decimal) digits (4 bits), bytes (8 bits), words (16 bits), long words (32 bits), byte strings (8n + 8 bits), and word strings (16n + 16 bits). The string types consist of sequential bytes or words preceded by a word count. Strings may be accessed in either ascending or descending address order. Bytes are the smallest directly addressable data type. Bits and binary coded decimal are dealt with using special instructions such as SET B (set bit), and DAB (decimal adjust).

One of the most unusual features of this processor is the large memory space. The segmented Z-8000 has 24 address lines yielding 16,777,216 directly addressable bytes. The system and the user may both have their own memory, as may program code, data, and data stack, for a grand total of 96 M bytes of on line memory. The memory is arranged in 64 K byte blocks called segments. An outboard support integrated circuit, called the memory management unit (MMU), is available to provide, transparently to the user, segment mapping or relocation and memory protection. To access this mountain of memory, there are eight addressing modes, illustrated in figure 3.

The Z-8000 has over 110 different instructions, many of which have several possible addressing modes. The instruction set is summarized in table 1. There are many

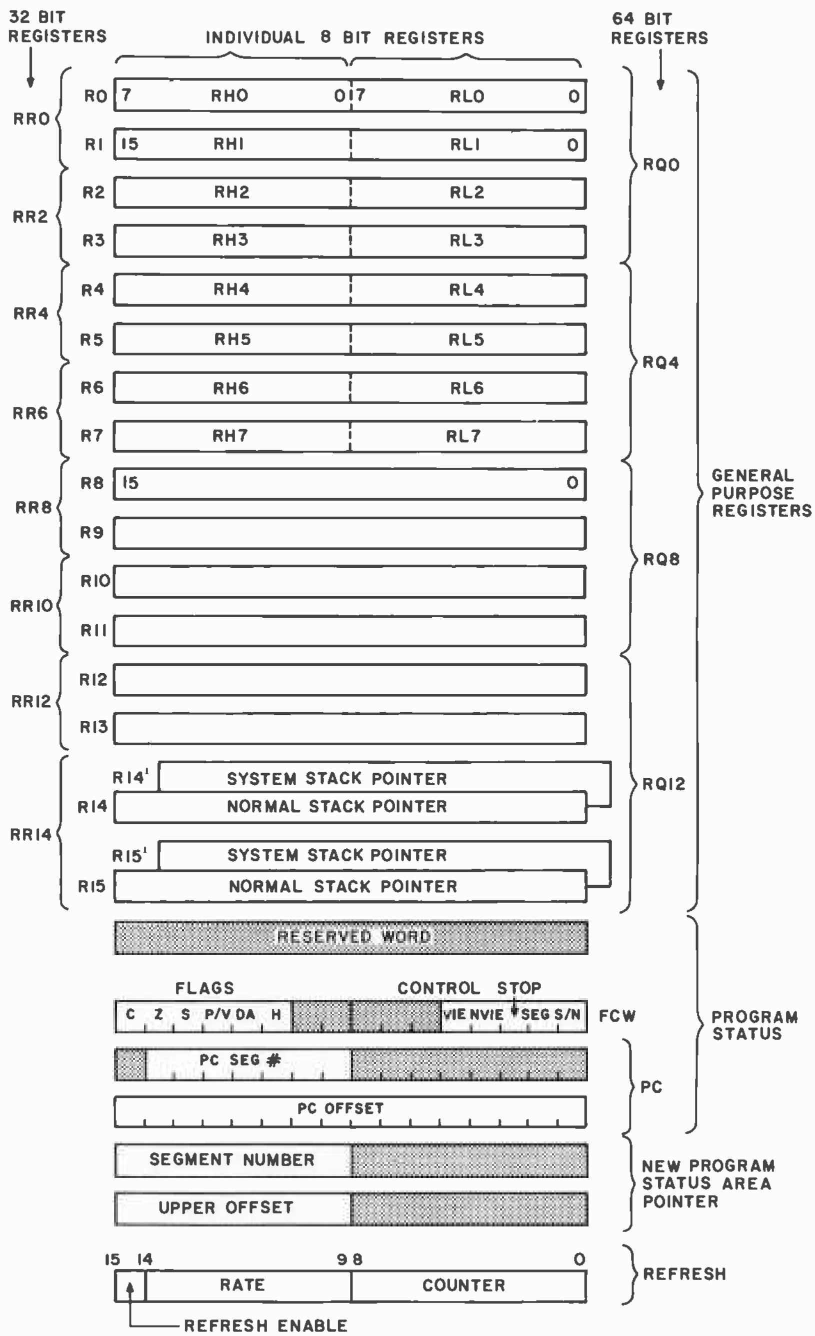
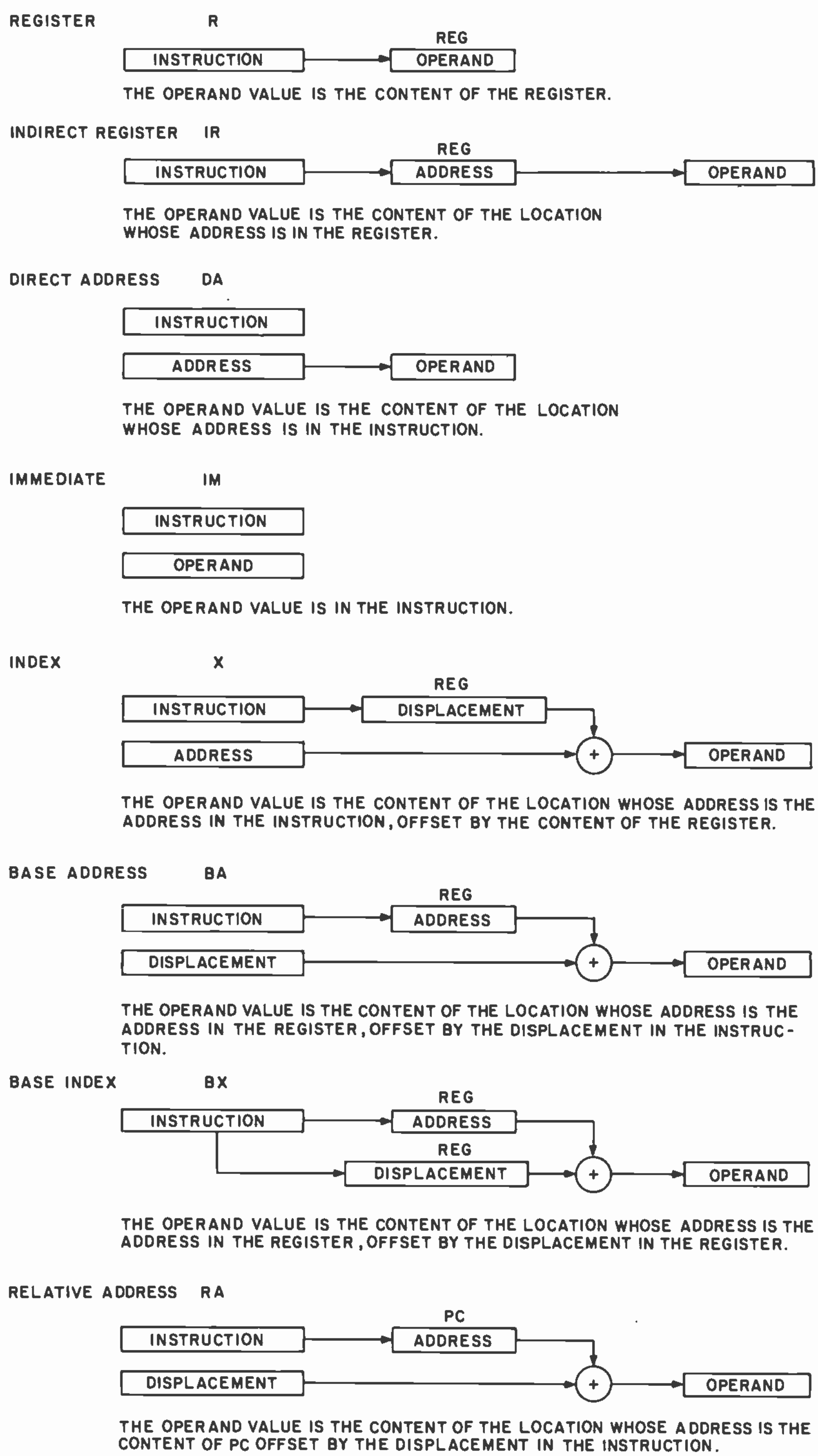
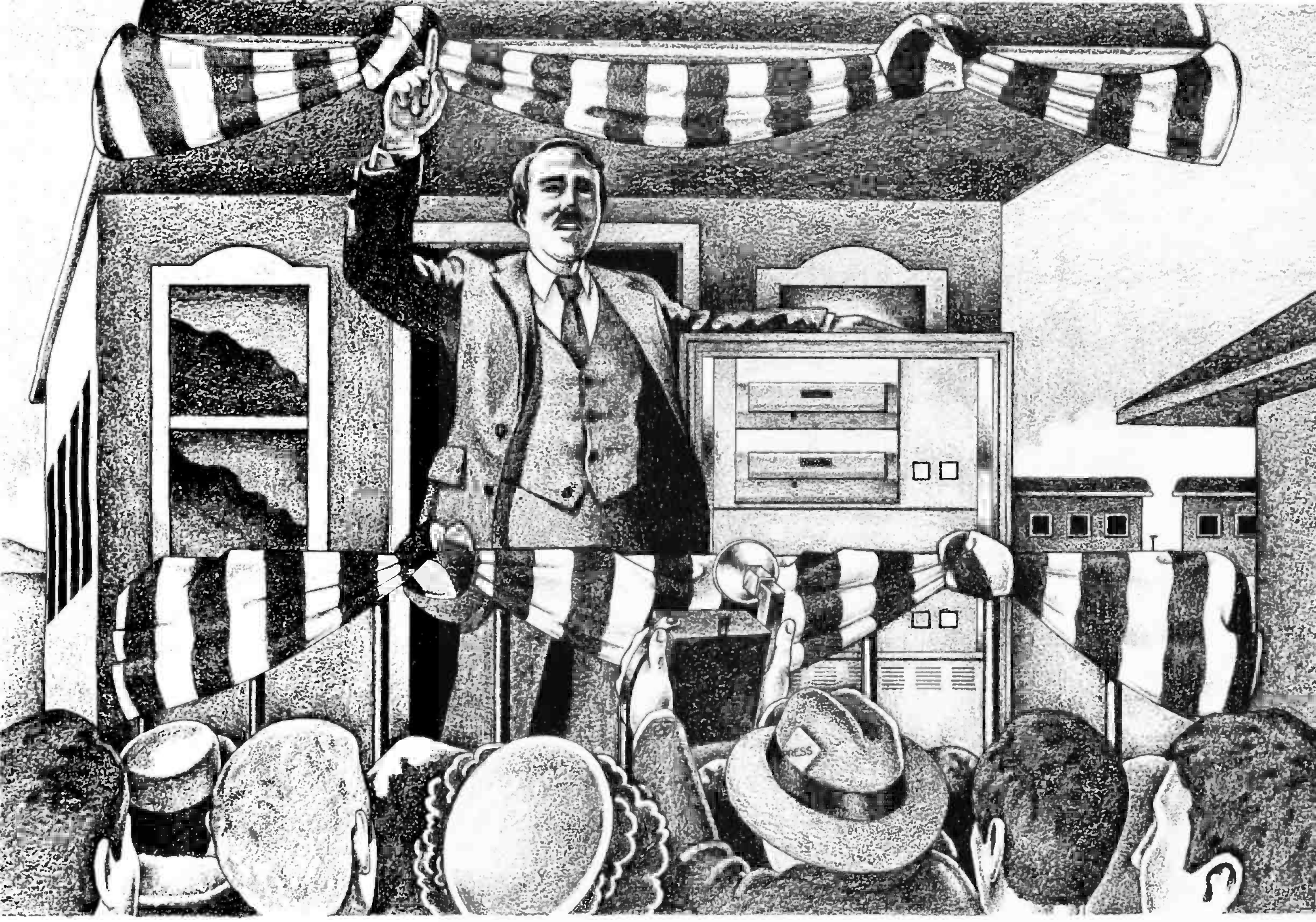


Figure 2: Z-8000 registers. The Z-8000 has sixteen 16 bit registers logically subdivided into sixteen 8 bit registers, eight 32 bit registers, and four 64 bit registers. The 8 and 16 bit registers are available as general purpose accumulators, and 15 of the 16 bit registers are available as index registers.

powerful instructions which are not usually seen in microcomputers. Not many microcomputers or small minicomputers have extended precision multiply and divide, or translate, increment, and repeat. There are string comparison operations and block move operations. The decrement and jump-on-nonzero instruction of the Z-80 has been extended to allow any word or byte length register as an index counter. There is also a system call instruction which performs a software interrupt to the operating system. This is a very convenient means of communication between the user and system. There are other so-called traps that imitate an interrupt to the operating system. They are used to preserve software integrity, and occur when there is an illegal memory or instruction reference, or when a user mode program attempts to execute a privileged or I/O (input/output) instruction. A parti-

Figure 3: Z-8000 addressing modes.





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cularly interesting subset of instructions concerns the use of a pair of pins on the Z-8000 packaged called μI and μ0. These pins, and the instructions which govern them, allow for the combination of Z-8000 into efficient multi-processor or network systems. The only regrettable lack I've noticed thus far is the absence of memory-to-memory instructions.

Performance, in terms of execution speed, is a major factor in the selection of a processor. In table 2, I have tabulated the approximate speed of several common processors for simple tasks. Obviously, the Z-8000 is way out in front, competing very favorably with a popular medium sized minicomputer whose processor's cost is more than two orders of magnitude greater. The Z-8000's speed and memory make it the best thing yet for personal applications which involve number crunching. I can easily imagine it as the heart of a personal FORTRAN or

Text continued on page 91

Memory Management

Memory management, as the name implies, is a clever technique to handle large amounts of memory in a flexible fashion. In most computer systems, this management requires the large memory to be broken up into smaller (eg: 64 K byte) chunks. Each program or task residing in memory is assigned into its own unique chunk or segment. In general, segments may vary in length, but a program residing in a particular segment may not exceed that segment in length. Often a program will not need to directly address a vast amount of memory, and if a particular application program or set of programs will fit into segments, then management can be used. Management provides three main advantages in the Z-8000:

1. Since programs are constrained to fit in 64 K bytes or less, a 16 bit address is sufficient instead of the 24 bits required to address 16 M bytes. This obviously leads to a more compact and efficient code.
2. Programs residing in segments are mapped into what is known as logical or virtual address space. Virtual addresses are simply the addresses of locations in a segment from hexadecimal 0000 to FFFF. They are called virtual because they are relative only to the start of their segment and need not bear any relation to the actual physical addresses in the memory circuitry. Programs in segments are thus totally relocatable, needing only to inform the memory management device of the physical starting address of the particular segment. Figure 4 demonstrates this principle. Note that consecutive segments need not appear consecutively mapped into physical memory and also that segments may overlap physical memory.
3. Segmenting easily provides for memory protection. Since the memory management device knows the length of each segment, any attempt by a user task to access physical memory outside of its segment causes a segment violation and a software interrupt to the operating system. This is very useful when running a timesharing system or debugging a new program.

The memory management device works simply by adding a constant base address for each segment to any memory references issued by that segment. The device in the Z-8000 also checks a number of conditions such as system versus user state, code versus data, read write versus read only, and valid base address in addition to the segment size. If any mismatches or faults occur, the operating system is informed.

Table 1: Summary of the Z-8000 instruction set, slightly condensed.

The instruction set table is somewhat abridged due to space considerations. For example, almost all data manipulation type instructions (ie: data transfers, or arithmetic) have associated forms for the handling of byte length and long word length operands. The mnemonic for an alternate length operand is created by appending a B (for byte) or an L (for long word) to the standard op code mnemonic. For example, a byte length COMPARE (CP) would be CP B = CPB. The symbols and abbreviations used in this table are defined as follows:

Operands	Addressing Modes	Miscellaneous
b - bit number	BA - base address	← - is replaced by
CC - condition code	BX - base index	@ - indirect
CTLR - a control register	DA - direct address	R_n, R_n+1 - register pair
dst - destination	IM - immediate	
FLGR - flag register	IR - indirect register	
int - any interrupt enable bit	R - register	
n - a small integer	RA - relative address	
src - source	X - index	

Loads and Exchanges

Op code	Operands	Operation	Addressing Modes
CLR	dst	Clear dst← 0.	R,IR,DA,X
EX	R,src	Exchange temp← src src← R R← temp.	R,IR,DA,X
LD	R,src	Load src to register R← src.	R,IR,DA,X,IM, BA,BX,RA
LD	dst,R	Load register to dst dst← R.	IR,DA,X,BA, BX,RA
LD	dst,IM	Load to memory immediate dst← IM.	IR,DA,X
LDA	R,src	Load address The address is computer from src and stored in R.	DA,X,BA,BX,RA
LDM	R,src,n	Load multiple memory to registers Load n registers starting at register R from location starting at src (n=1 to 16).	IR,DA,X
LDM	dst,R,n	Load multiple register to memory Load n words starting at dst from n registers starting with R (n=1 to 16).	IR,DA,X
POP	dst,IR	Pop dst← IR (autoincrement).	R,IR,DA,X
PUSH	IR,src	Push (autodecrement) IR← src.	R,IR,DA,X,IM

Arithmetic

Op code	Operands	Operation	Addressing Modes
ADC	R,src	Add with carry R← R + src + carry.	R
ADD	R,src	Add R← R + src.	R,IR,DA,X,IM
CP	R,src	Compare R − src Flags are affected.	R,IR,DA,X,IM
CP	dst,IM	Compare memory with immediate dst − IM.	IR,DA,X
DAB	dst	Decimal adjust Decimal adjust of dst.	R
DEC	dst,n	Decrement by n dst← dst − n (n is 1 to 16).	R,IR,DA,X
DIV	R,src	Divide (signed) R_{n+1}← (R_n, R_{n+1})/src R_n← remainder.	R,IR,DA,X,IM
EXTS	dst	Extend sign Extend sign of R_{n+1} to R_n.	R
INC	dst,n	Increment by n dst← dst + n (n is 1 to 16).	R,IR,DA,X
MULT	R,src	Multiply (signed) (R_n, R_{n+1})← (R_{n+1})*src.	R,IR,DA,X,IM
NEG	dst	Negate dst← 0 − dst.	R,IR,DA,X
SBC	R,src	Subtract with carry R← R − src − carry.	R
SUB	R,src	Subtract R← R − src.	R,IR,DA,X,IM

Logical

Op code	Operands	Operation	Addressing Modes
AND	R,src	And R← R AND src.	R,IR,DA,X,IM
COM	dst	Complement dst← NOT dst.	R,IR,DA,X
OR	R,src	Or R← R OR src.	R,IR,DA,X,IM
TEST	dst	Test dst OR 0.	R,IR,DA,X
TCC	CC,dst	Test condition code Set lower bit of register if CC is true, reset otherwise.	R
XOR	R,src	Exclusive or R ← R XOR src.	R,IR,DA,X,IM

Program Control

Op code	Operands	Operation	Addressing Modes
CALL	dst	Call subroutine Autodecrement SP @ SP ← PC PC ← dst.	IR,DA,X
CALR	dst	Call relative Autodecrement SP @ SP ← PC PC ← PC + dst Range +4094 to −4096 bytes.	RA
CPBJR	R,IM,CC,dst	Compare and jump relative R −IM. If CC is true PC ← PC + dst Range +254 to −256 bytes Flags are not affected.	RA
DJNZ	R,dst	Decrement and jump on nonzero R ← R − 1 If R≠0 PC ← PC + dst Range 0 to −256 bytes Flags are not affected.	RA
IRET		Interrupt return PS ← @ SP Autoincrement SP.	–
JP	CC,dst	Jump conditional If CC is true PC ← dst.	IR,DA,X
JR	CC,dst	Jump conditional relative If CC is true PC ← PC + dst Range +254 to −256 bytes.	RA
RET	CC	Return conditional If CC is true PC ← @ SP Autoincrement SP.	–
SC	n	System call Push instruction Autodecrement SP @ SP ← Old PS PS ← New system call PS (N=0 to 255).	–

Table 1, continued:

Bit Manipulation

Op code	Operands	Operation	Addressing Modes
BIT	b,dst	Test bit static Z flag ← NOT dst_b.	R,IR,DA,X
BIT	R,dst	Test bit dynamic Z flag ← NOT dst_R.	R
RES	b,dst	Reset bit static dst_b ← 0.	R,IR,DA,X
RES	R,dst	Reset bit dynamic dst_R ← 0.	R
SET	b,dst	Set bit static dst_b ← 1.	R,IR,DA,X
SET	R,dst	Set bit dynamic dst_R ← 1.	R
TSET	dst	Test and set S flag ← sign of dst dst ← All "1s."	R,IR,DA,X

Rotate and Shift

Op code	Operands	Operation	Addressing Modes
RLDB	R,src	Rotate digit left.	R
RRDB	R,src	Rotate digit right.	R
RL RLB	dst,n	Rotate left by n n is 1 or 2.	R
RLC	dst,n	Rotate left through carry by n n is 1 or 2.	R
RR	dst,n	Rotate right by n n is 1 or 2.	R
RRC	dst,n	Rotate right through carry by n n is 1 or 2.	R
SDA	dst,R	Shift dynamic arithmetic Shift dst by content of R Left or right depending on sign Range +31 to −32.	R
SDL	dst,R	Shift dynamic logical Shift dst by content of R Left or right depending on sign Range +31 to −32.	R
SLA	dst,n	Shift left arithmetic by n n is 1 to size of data element.	R
SLL	dst,n	Shift left logical by n n is 1 to size of data element,	R
SRA	dst,n	Shift right arithmetic n is 1 to size of data element.	R
SRL	dst,n	Shift right logical by n n is 1 to size of data element.	R

Block Transfer and String Manipulation

Op code	Operands	Operation	Addressing Modes
CPD	Rx,src,Ry,CC	Compare and decrement Rx − src Autodecrement src Ry ← Ry − 1.	IR
CPDR	Rx,src,Ry,CC	Compare, decrement and repeat Rx − src Autodecrement src Ry ← Ry − 1 Repeat until CC false or R = 0.	IR
CPI	Rx,src,Ry,CC	Compare and increment Rx − src Autoincrement src Ry ← Ry − 1.	IR
CPIR	Rx,src,Ry,CC	Compare, increment and repeat Rx − src Autoincrement src Ry ← Ry − 1. Repeat until CC false or Ry=0.	IR
CPSD	dst,src,R,CC	Compare string and decrement dst − src Autodecrement dst and src R ← R − 1.	IR
CPSDR	dst,src,R,CC	Compare string, decrement and repeat dst − src Autodecrement dst and src R ← R − 1 Repeat until CC false or R=0.	IR
CPSI	dst,src,R,CC	Compare string and increment dst − src Autoincrement dst and src R ← R − 1.	IR
CPSIR	dst,src,R,CC	Compare string, increment and repeat dst − src Autoincrement dst and src R ← R − 1 Repeat until CC false or R=0.	IR
LDD	dst,src,R	Load and decrement dst ← src Autodecrement of dst and src R ← R − 1.	IR
LDDR	dst,src,R	Load, decrement and repeat dst ← src Autodecrement of dst and src R ← R − 1 Repeat until R=0.	IR
LDI	dst,src,R	Load and increment dst ← src Autoincrement of dst and src R ← R − 1.	IR
LDIR	dst,src,R	Load, increment and repeat dst ← src Autoincrement of dst and src R ← R − 1 Repeat until R=0.	IR
TRDB	dst,src,R	Translate and decrement dst ← src (dst) Autodecrement dst R ← R − 1.	IR
TRDRB	dst,src,R	Translate, decrement and repeat dst ← src (dst) Autodecrement dst R ← R − 1 Repeat until R=0.	IR
TRIB	dst,src,R	Translate and increment dst ← src (dst) Autoincrement dst R ← R − 1.	IR
TRIRB	dst,src,R	Translate, increment and repeat dst ← src (dst) Autoincrement dst R ← R − 1 Repeat until R=0.	IR
TRTDB	src1,src2,R	Translate and test decrement R0 ← src2 (src1) Autodecrement src1 R ← R − 1.	IR
TRTDRB	src1,src2,R	Translate and test, decrement and repeat R0 ← src2 (src1) Autodecrement src1 R ← R − 1 Repeat until R=0 or R0≠0.	IR
TRTIB	scr1,src2,R	Translate and test increment R0 ← src2 (src1) Autoincrement src1 R ← R − 1,	IR
TRTIRB	src1,src2,R	Translate and test, increment and repeat R0 ← src2 (src1) Autoincrement src1 R ← R − 1 Repeat until R=0 or R0≠0.	IR

Input Output

Op code	Operands	Operation	Addressing Modes
IN	R,src	Input R ← src.	IR,DA
IND	dst,src,R	Input and decrement dst ← src Autodecrement dst R ← R − 1.	IR
INDR	dst,src,R	Input, decrement and repeat dst ← src Autodecrement dst R ← R − 1 Repeat until R=0.	IR
INI	dst,src,R	Input and increment dst ← src Autoincrement dst R ← R − 1.	IR
INIR	dst,src,R	Input, increment and repeat dst ← src Autoincrement dst R ← R − 1 Repeat until R=0.	IR
OUT	dst,R	Output dst ← R.	IR,DA
OUTD	dst,src,R	Output and decrement dst ← src Autodecrement src R ← R − 1.	IR
OTDR	dst,src,R	Output, decrement and repeat dst ← src Autodecrement src R ← R − 1 Repeat until R=0.	IR

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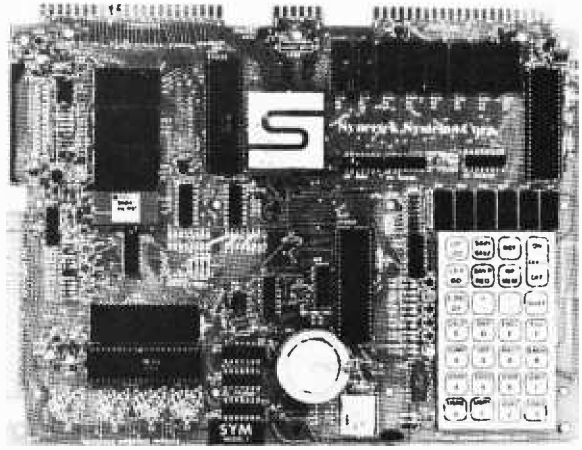

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VAK-2 16K RAM Board with only 8K of RAM (½ populated)	**$239.00**
VAK-3 Complete set of chips to expand above board to 16K	**$175.00**
VAK-4 Fully populated 16K RAM	**$379.00**

VAK-5 2708 EPROM PROGRAMMER

This board requires a +5 VDC and ±12 VDC, but has a DC to DC multiplyer so there is no need for an additional power supply. All software is resident in on-board ROM, and has a zero-insertion socket.

VAK-5 2708 EPROM Programmer **$269.00**

VAK-6 EPROM BOARD

This board will hold 8K of 2708 or 2758, or 16K of 2716 or 2516 EPROMs. *EPROMs not included.*

VAK-6 EPROM Board **$129.00**

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This board allows you to create your own interfaces to plug into the motherboard. Etched circuitry is provided for regulators, address and data bus drivers; with a large area for either wire-wrapped or soldered IC circuitry.

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*KIM is a product of MOS Technology

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Circle 315 on inquiry card.

Table 1, continued:

OUTI	dst,src,R	Output and increment dst ← src Autoincrement src R ← R − 1.	IR
OTIR	dst,src,R	Output, increment and repeat dst ← src Autoincrement src R ← R − 1 Repeat until R=0.	IR
SINB	R,src	Special input R ← src.	DA
SINDB	dst,src,R	Special input and decrement dst ← src Autodecrement dst R ← R − 1.	IR
SINDRB	dst,src,R	Special input, decrement and repeat dst ← src Autodecrement dst R ← R − 1 Repeat until R=0.	IR
SINIB	dst,src,R	Special input and increment dst ← src Autoincrement dst R ← R − 1.	IR
SINIRB	dst,src,R	Special input, increment and repeat dst ← src Autoincrement dst R ← R − 1 Repeat until R=0.	IR
SOUTB	dst,src	Special output dst ← src.	DA
SOUTDB	dst,src,R	Special output and decrement dst ← src Autodecrement src R ← R − 1.	IR
SOTDRB	dst,src,R	Special output, decrement and repeat dst ← src Autodecrement src R ← R − 1 Repeat until R=0.	IR
SOUTIB	dst,src,R	Special output and increment dst ← src Autoincrement src R ← R − 1.	IR
SOTIRB	dst,src,R	Special output, increment and repeat dst ← src Autoincrement src R ← R − 1 Repeat until R=0.	IR

Processor Control

Op code	Operands	Operation	Addressing Modes
COMFLG	flag	Complement flag Any combination of flags Z, C, V, P, S.	—
DI	int	Disable interrupt Any combination of NVI,VI.	—
EI	int	Enable interrupt Any combination of NVI,VI.	—
HALT		HALT.	
LDCTL	CTLR,src	Load to control register CTLR← src.	R
LDCTL	dst,CTLR	Load from control register dst← CTLR.	R
LDCTLB	FLGR,src	Load to flag byte FLGR← src.	R
LDCTLB	dst,FLGR	Load from flag byte dst← FLGR.	R
LDPS	src	Load program status PS← src.	IR,DA,X
MBIT		Test μI Z← μI.	—
MREQ	dst	Multimicro request.	R
MRES		Reset μ0 μ0← 0.	
MRLSE		Multimicro release.	—
MSET		Set μ0 μ0← 1.	
NOP		No operation.	
RESFLG	flag	Reset flag Any combination of flags Z, C, V, P, S.	—
SETFLG	flag	Set flag Any combination of flags Z, C, V, P, S.	—

Z-8000 Peripheral Support Circuits

Name	Function
Z-MBU	Microprocessor buffer unit for high speed elastic buffering between processors, and processors and peripherals. Organized in a 256 by 8 bit FIFO (first in first out) configuration. Can be used to interface Z-Bus systems to most other microprocessors.
Z-FIFO	First in first out buffer memory provides expansion of the Z-MBU to 16 bit words and any depth.
Z-CIO	Counter/timer and parallel I/O circuit contains three counter/timers and three parallel ports. Two of the parallel ports are eight bits wide and provide four handshaking modes, including IEEE-488 instrument bus protocol. The third port is four bits wide. The counters are all 16 bits wide.
Z-SIO	Serial I/O circuit contains two independent full duplex synchronous/asynchronous receiver/transmitters (USARTs). Each data channel contains full modem controls, programmable clock generator, and parity or CRC error code generation and checking.
Z-UPC	Universal peripheral controller is a Z-Bus compatible version of Zilog's new Z-8 8 bit microcomputer on a chip. It includes 124 general purpose registers, 2 K of masked read only memory, an internal UART, and two counter/timers.
Z-Bus RAM	There are two versions of these programmable memory circuits which directly interface to the Z-Bus. Both are organized as byte-wide structures to reduce the complexity of small, local memory design. 1. 4 K by 8 pseudostatic programmable memory has internal and transparent refresh circuitry. Its access time is in the range of 200-300 ns. 2. 2 K by 8 fully static programmable memory has access times below 150 ns.

Table 2: Comparison of the Z-8000 to several popular processors in the performance of several simple tasks.

Task	Z-8000[1]	8080A-1[2]	Z-80A[3]	LSI-11[4]	PDP 11/45[5]
Load Byte (Register to Register) (A register in Z-80, 8080)	0.75	1.6	1.0	2.95	0.90
Load Word (Memory to Register) (to HL in Z-80, 8080)	2.25	5.12	4.0	5.6	2.86
Add (16 bit)	2.25	9.61[6]	5.25[7]	6.3	2.86
Multiply (16 bit)	17.50	–	–	27 – 64	5.64

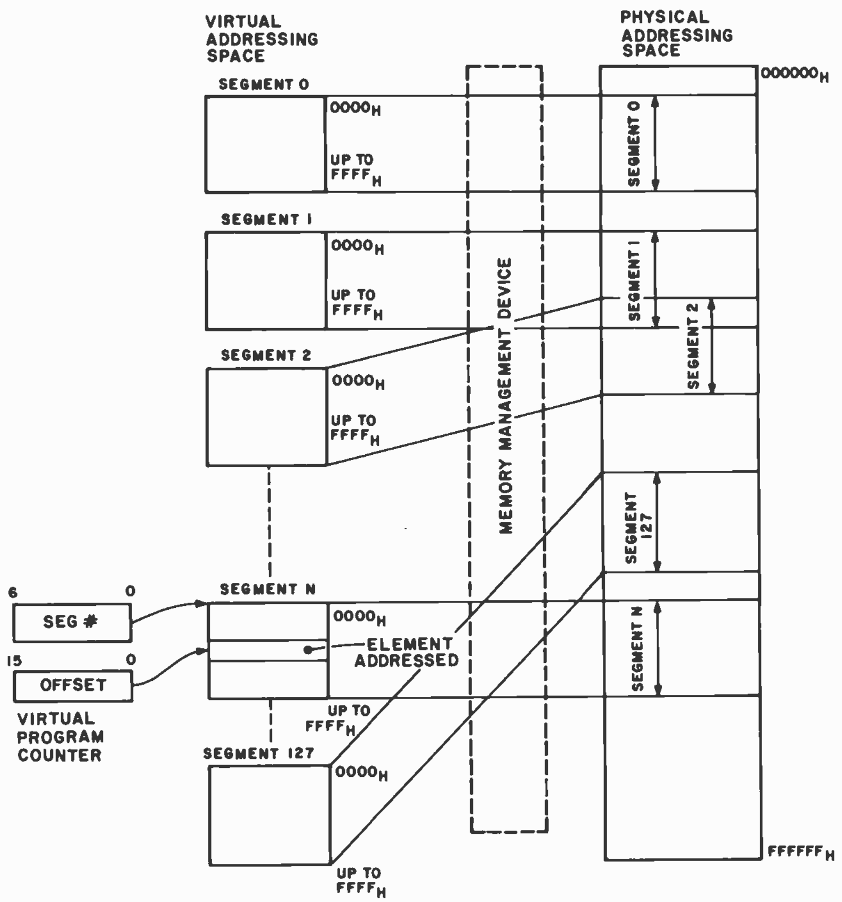
Notes:

1. 4 MHz clock, no memory wait, no refresh; data from Zilog Z-8000 advance specification, April 1978.
2. 3.125 MHz clock, no memory wait, no refresh; data from *Intel 8080 Microcomputer System Users Manual*, 9/75.
3. 4 MHz clock, no memory wait, no refresh; data from *Z-80 Reference Manual*.
4. 4 K byte onboard memory disabled: data from *LSI-11/PDP 11/03 Processor Handbook*, 1975-1976.
5. 11/45 with 8 K byte core stacks, even bytes; data from *PDP 11/04/34/45/55 Processor Handbook*, 1976-1977.
6. BC←(nn) LD BC, (MEM)
   HL←HL+BC ADD HL,BC.
7. HL⇄DE XCHG
   HL⇄(nn) LHLD (MEM)
   HL←HL+DE DAD D.

Text continued from page 84

APL machine which could run large application packages such as SPICE for circuit analysis or SPSS for statistics, and solve dynamics equations on line for real time graphics simulations like lunar lander, or very large chess playing programs.

According to sources at Zilog, the Z-8000 and its memory management device support chip will soon be available in large quantity. The Z-8000 is compatible with the already available Z-80 family of support chips such as the SIO (serial I/O), the CTC (timers), and the PIO (parallel I/O), etc. A new series of extended support chips for the Z-8000 is also in the works. So far five LSI peripheral devices and a new memory family have been announced. The text box on opposite page contains a brief description of these new devices. The usual line of microprocessor support products including single board computers, evaluation boards and development systems will also be available. Although details are not available as I write this, the system bus structure will probably be oriented toward high performance multiprocessor systems. As for software, Zilog has announced a disk based development system and the PLZ, BASIC, COBOL, FORTRAN languages. Also there is a Z-80-to-Z-8000 translator. I expect a real time, multitasking and multiprocessing operating system to be available soon in order to take advantage of this processor's many resources.■



(b) SEGMENTED ADDRESSING SPACE

Figure 4: Logical to physical address translation using the memory management device. The Z-8000 allows the programmer to make use of virtual memory addresses, which are simply the addresses of locations in a memory segment from hexadecimal 0000 to FFFF. Virtual addresses are relative only to the start of their segment and need not bear any relation to physical addresses in memory. The clever use of virtual memory techniques can yield high-powered programming results.

Programming Quickies

Inverse Trig Functions

Alan R Miller
New Mexico Tech
Socorro NM 87801

All except the very smallest BASIC interpreters provide sine, cosine, tangent and inverse tangent functions. None, that I am aware of, have the inverse sine or inverse cosine functions. These two functions are very simple to generate using the inverse tangent function. Lines 10 and 20 of listing 1 contain the definition of the inverse sine and inverse cosine, respectively. Lines 30 to 80 contain a driver function for demonstration purposes.■

Listing 1:

```
10 DEF FNSN (X) = ATN (1/SQR(1/(X*X)−1))
20 DEF FNCS (X) = ATN (SQR(1/(X*X)−1))
30 PRINT "A     ";"ARC SIN"," SIN","ARC COS","COS"
40 INPUT "ARC"; A
50 B=FNSN(A)
60 C=FNCS(A)
70 PRINT A; B, SIN(B),C,COS(C)
80 GOTO 40
```

Machine Language Puzzler

Christopher Strangio
CAMI Research
43 Bailey Rd
Watertown MA 02172

Odd Tones

The following program is entered and run:

(For the 6800 processor)

```
L3:  MVI A, #X
L2:  MVI B, #A8 (hex)
L1:  DCR B
     JNZ L1
     DCR A
     OUT 00


     JNZ L2
     JMP L3
```

(For the 8080 processor)

```
L3:  LDAA #X
L2:  LDAB #A8 (hex)
L1:  DECB
     BNE L1
     DECA
     STAA @FF00 (assume port 0 is
                 this location as a
                 simple output latch)
     BNE L2
     BRA L3
```

By connecting a small speaker (in series with a 220 ohm resistor) between the least significant bit of port 0 and ground, we hear a tone. However, for X equal to an odd number, an audible blip is heard periodically, while for X equal to an even number, no blip is heard at any time. Why is a blip heard for odd Xs only? Try these programs or simply analyze the waveforms, then turn to page 178 for an answer.■

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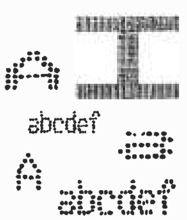

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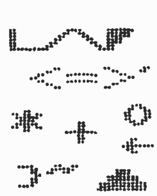

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AaBb
CcDd
EeFf

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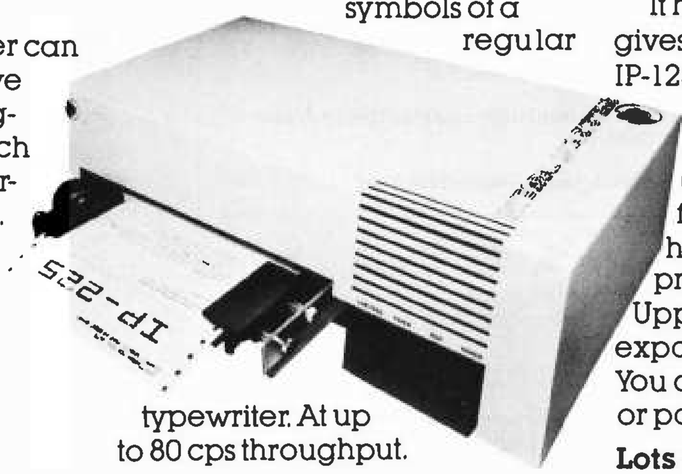

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*Some of these advantages require extra-cost options.

Circle 173 on inquiry card.

Designing with Double Sided Printed Circuit Boards

David Lamkins
DBL Electronics
83 Morgan Cir
Amherst MA 01002

Materials Required for Layout Design
Pencils: Red, Blue and Black
Eraser and Pencil Sharpener
Tracing Vellum
Grid
Printed Circuit Design Template
Light Table
Large Scratch Paper Pad
Your Schematic, Integrated Circuit Pinout Data, etc
Scotch Magic Transparent Tape

Table 1: Materials required for printed circuit board layout.

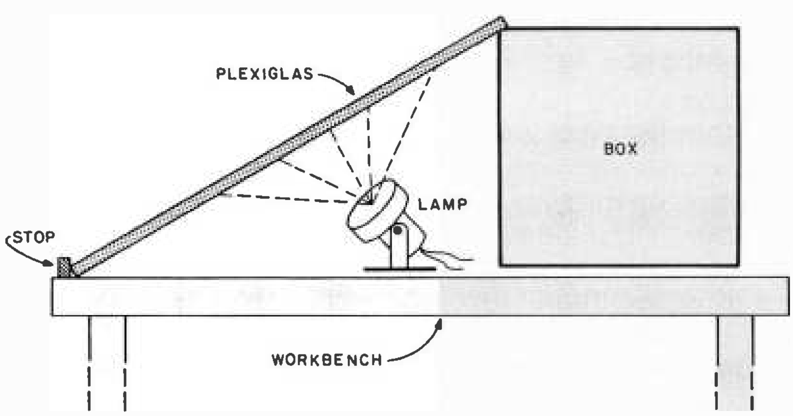

Figure 1: The author's design for a homebrew light table used for drawing printed circuit board layouts. A sheet of Plexiglas or other clear plastic illuminated by a lamp is used as the drawing surface.

Magazines for electronic hobbyists sometimes run articles about do-it-yourself printed circuit layout and construction. Unfortunately I never saw an article which presented a unified printed circuit design strategy for large and very large systems (eg: a board with 20 or more integrated circuits).

Consequently, when the time came for me to design the printed circuit boards for a system involving more than 900 semiconductors, with greater than 60 percent of that count being integrated circuits, I didn't know where to begin.

Determination is the prime motive force in a project that large, so I went ahead and started. Along the way I took notes about what I learned. Using the methods I developed, you should be able to design double sided printed circuits for your own behemoth kluge without undue anger or frustration.

To undertake a large printed circuit project, you should be properly equipped. Simple "pen and ink on grid paper" techniques may be adequate for small boards, but on a larger layout, even with only 20 integrated circuits, you will have an absolute minimum of almost 300 integrated circuit leads. Try drawing that many pads on 0.1 inch centers, not to mention interconnecting traces and associated components, and you will end up in a sobbing heap on your workshop floor.

Table 1 lists the materials necessary to the initial design of your printed circuit layout.

The black pencil will be used to delineate components and pads on your drawing. The red pencil is used to mark conductor runs for the solder side of the board, while the blue pencil marks runs on the component side. A necessary adjunct to the pencils is the eraser and pencil sharpener. Most likely, neither will see as much use as the pencils themselves, but both should be close at hand.

The tracing vellum should be good quality. You will not appreciate tears or holes as a result of the erasing you will be doing.

A grid is essential to good planning. Grids are precision printed on dimensionally stable Mylar and are available in a variety of styles. Your selection will depend largely on the scale to which you draw your design. The most commonly used scales are 4x, 2x, and 1x. The 4x and 2x scales find wide use commercially, where use of automated manufacturing techniques requires extremely tight tolerances on component positioning. The other advantage of a larger scale is reduced eyestrain. For our purposes, the 1x scale is probably best since materials cost is lowest and the need for photoreduction facilities is alleviated. Therefore, your grid should have 20 lines per inch to allow component placement to the nearest 0.05 inch. You might find a grid with 10 lines per inch adequate, but many lead spacings do not fit exactly on a 0.1 inch grid, and you will quickly tire of trying to visually approximate the halfway mark.

The printed circuit design template helps you draw resistors, capacitors, diodes, transistors, integrated circuits, trimmers and edge fingers accurately and repetitively. Be sure you get the 1x size.

A light table is necessary to light your grid from the back and make the grid lines visible through the vellum. Commercial light tables are available, but they are not inexpensive. A homemade substitute can be as simple as a piece of Plexiglas leaning against a box on a table with an incandescent or fluorescent desk lamp providing the illumination (see figure 1). Should you use an incandescent lamp, a low wattage is recommended to minimize heating of the grid.

A pad of scratch paper should be kept handy for sketching of trial layouts, quick computations, doodles, etc.

I use Scotchbrand Magic transparent tape; it is the only readily available tape I have found that will hold the grid and artwork in place on the light table without oozing or creeping due to the heat of the light.

These materials along with your schematic and related pertinent data are all you need to lay out a printed circuit board.

Table 2 outlines the layout strategies I follow in order of execution by heading, and in order of relative importance by subheading.

Initially, you should study your schematic to identify functional groups of components. Carry this out to as detailed a level as you are able. The procedure will enhance your understanding of the circuit in general as well as the interrelations among subcircuits and the correspondence between circuits and components that influence your design. Additionally, you may be able to define critical areas at this time, such as the need for shielding, isolation, or heat removal. Be sure that all unused logic inputs and nonstandard supply pinouts are explicitly included in your schematic.

- **Divide circuit into functional groups.**
- **Define board interface.**
- **Calculate board size.**
- **Trial position integrated circuits.**
  1. Locate analog circuitry close to interface.
  2. Group components by functional groups.
  3. Arrange circuits symmetrically around shared integrated circuits.
  4. Arrange functional groups to minimize number of interconnects.
- **Position other Components.**
  1. Keep analog traces short with inputs separated from outputs.
  2. Provide supply bypassing at each linear and TTL integrated circuit and at any other circuitry sensitive to supply noise or circuitry generating fast edges.
- **Don't crowd components.**
- **Route traces.**
  1. Shortest runs first.
  2. Runs local to functional group.
  3. Inter-group runs.
  4. Runs to interface.
  5. Power runs last.

  } Avoid blocking power and ground pins.
- **Check spacings.**

Table 2: Some printed circuit board layout strategies.

Your board interface is a definition of how signals connect to and from the printed circuit board. The interface may be configured as edge connections, solder pads for single leads or ribbon cable, a special connector, or any combination of these. Your system's physical design may place constraints on the locations of the interface connections. If your system is so large that a single board implementation is impractical, or if your system is being constructed modularly, you should define macrofunctions or subsystems into which your overall system can be partitioned. First, define a system by which individual boards can be interconnected. Then, treating each partition as a complex component, define any requirements for shielding, isolation, or heat removal. You may want to consider using a printed circuit backplane or mother board to make system interconnections (see figure 2). The mother board is a good place to locate your power supply and front panel controls if you want a truly modular system.

Now calculate the board size. An ab-

About the Author

David Lamkins is a twenty-three year old consultant in the analog and digital electronics field, and has been working since 1974 on a digital electronic music system. David's hobbies also include playing the guitar and reading science fiction.

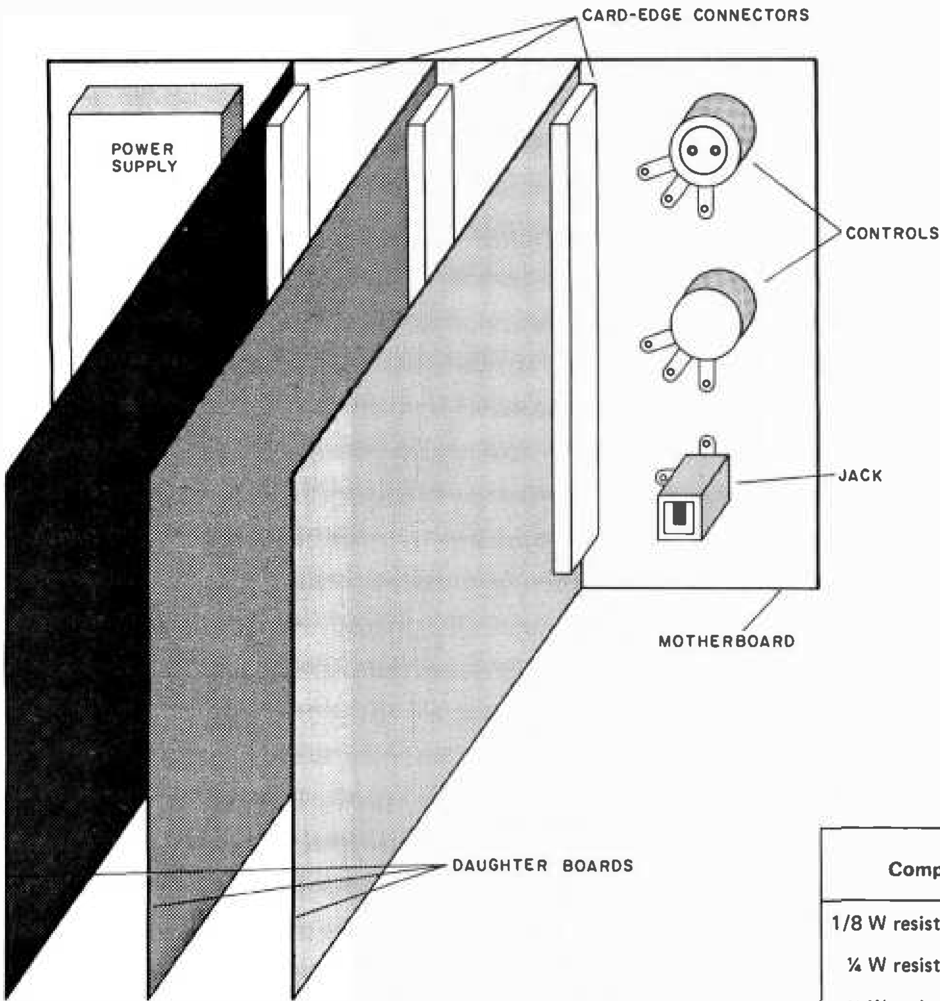

Figure 2: A typical arrangement of printed circuit boards used for large circuit designs. Several "daughter" boards are shown plugged into a "mother" board. The latter is used to facilitate board interconnections and reduce wiring to a minimum.

Table 3: Average printed circuit board areas taken up by commonly used electronics components.

Component Type	Board Area (Square Inches)
1/8 W resistor	0.075
¼ W resistor	0.09
½ W resistor	0.14
1 W resistor	0.27
2 W resistor	0.44
RN55 precision resistor	0.12
Signal diode (D035)	0.06
Power diode (D07)	0.09
Small disk capacitor (CK60-61)	0.06
Large disk capacitor (CK62-64)	0.16
TO-18	0.09
TO-5	0.16
TO-66	0.64
TO-3	1.0
14 lead DIP	0.18
16 lead DIP	0.21
24 lead DIP	0.66
28 lead DIP	1.9
40 lead DIP	2.34
.156 inch connector finger	0.06

solute minimum figure can be obtained by calculating the total area occupied by components (table 3). In practice, you will never achieve this minimum figure with a double sided board, but it is helpful to know how much component area you have. A more realistic figure to start with is 2 to 3 square inches per integrated circuit, tending toward the higher side if the board has many discrete components, large passive components, or a large number of edgeboard IO pins. If the board is constrained to be a certain size, you will have to try to make it all fit, although it could be very difficult if you have much less than 2 square inches per integrated circuit.

Now, take a sheet or two from your scratch pad and sketch a few trial arrangements for your integrated circuits. There are several things you should strive for. Most important is to locate any analog circuitry close to its associated board interface. This minimizes any adverse effects due to coupling or feedback that could be caused by long analog lines. Next is the arrangement of components by functional groups. If a multi-

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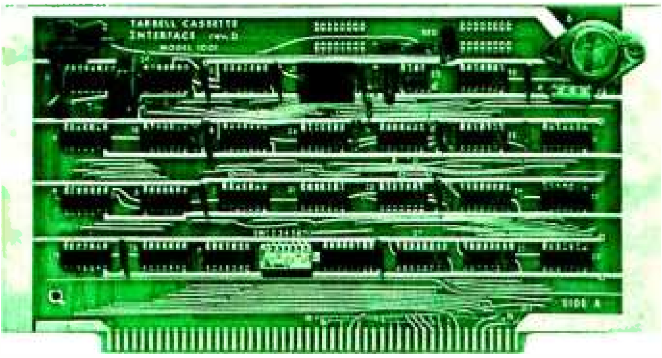

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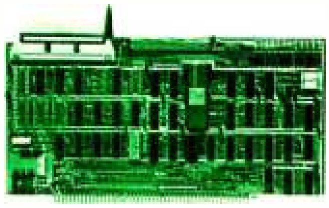

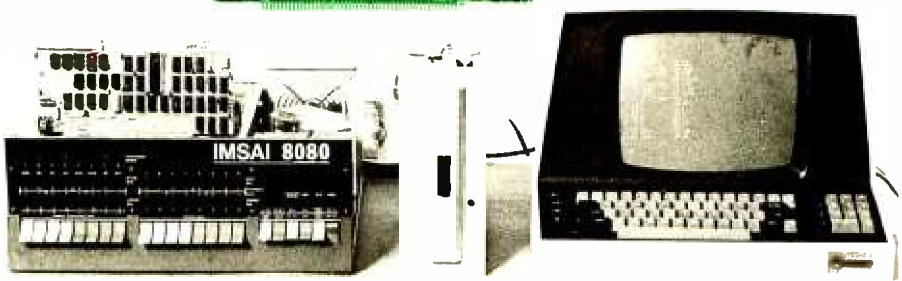

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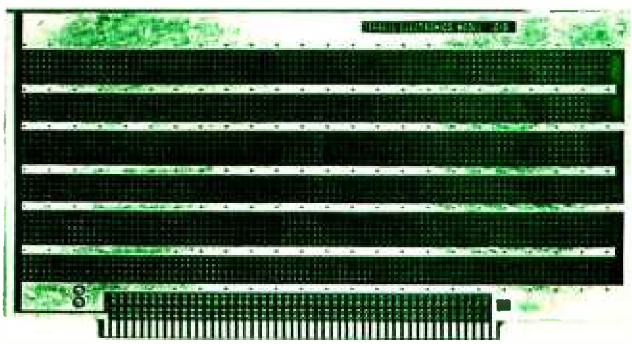
Model 1010



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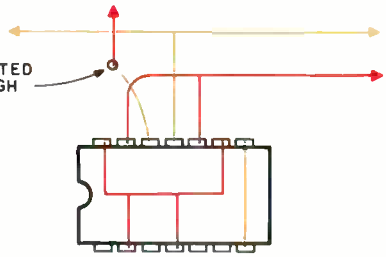

Figure 3: Typical routing of conductors on a two sided printed circuit board. Contrasting colors are used to show wire runs on the respective sides of the board. Note the use of the dedicated through-hole.

section integrated circuit is shared by two or more functional groups, try to arrange these groups close to the shared integrated circuit. It is often advantageous to make use of the symmetrical layout of many multisection integrated circuit pinouts. Functional groups should be arranged relative to each other to minimize the number and length of interconnections between groups. If a lot of lines go to an edgeboard connector, try to leave a clear route for them.

Tape the grid to the light table, then tape a sheet of vellum over the grid and proceed to lay out the board. Begin by defining the edges of the board in black pencil. Next, using black pencil and the template, locate the integrated circuits on the board using your best trial sketch as a guide. Leave plenty of space around the integrated circuits, because interconnections can consume a lot of board space.

Try to arrange the integrated circuits in a consistent XY grid to maximize the open paths a trace can follow from here to there. Leave plenty of room around the edges of the board; some of the longer traces are most easily routed there.

Still using template and black pencil, position the discrete components. In analog circuitry, maintain short signal leads and separation between input and output of high gain stages. Be sure to provide adequate bypassing: One bypass capacitor per integrated circuit is not too much. Don't crowd components. Keep in mind that you may need access to integrated circuit pins for servicing, and leave room to adjust trimpots. Also, keep important test points out in the open. Avoid locating small components out of sight below larger, overhanging components, and don't allow components or groups of components to block access to integrated circuit pins. During this process, you may find you'll have to move things around somewhat to fit everything where you want it. This may require some erasing.

Now comes the difficult part. Using red and blue pencils and eraser, draw the traces on the vellum. Red is used for solder-side runs and blue for component-side runs. Trying things out on scratch paper can save you much erasure.

The shortest traces will be those interconnecting the pins of a single integrated circuit to one another. Do these first. Use red whenever possible to minimize the number of component-side runs. You should be able to get this far without creating any connections that start on one side of the board and finish on the other side (except via a hole used for a component lead). The next longest runs will be interconnections within a functional group: Do these next. If possible, avoid blocking access to integrated circuit power and ground pins.

Next should be runs connecting functional groups together, followed by runs to the edge-board interface, if used. Somewhere along the way you'll have to start using dedicated through-holes to run signals past areas that are blocked in completely (see figure 3). Depending on the complexity of your circuit, you shouldn't really need more than one or two through-holes per integrated circuit on the board.

As you proceed, you'll want to keep track of the connections made. I usually do this by numbering the integrated circuits on the layout, then marking them on the schematic to correspond. As I make a connection, I mark a slash through the lead on the schematic. For circuitry that uses identical sections repeatedly, I simply copy the first section as required.

The last connections are power and ground to the integrated circuits. The practice of saving these connections until last is uncommon, but it reduces drastically the number of dedicated through-holes on a larger board. It's easier to route two or three runs through a jungle of interconnections than it is to individually reroute each trace of that same jungle to go around two or three power runs. At any rate, the power runs should be heavy enough for the type and amount of logic being used. When working with TTL integrated circuits, be aware that some formidable current transients are coupled to ground; be sure to beef up that trace accordingly. CMOS at low speeds is relatively immune to power supply noise.

In routing some of the longer traces, you may think that access to some places is blocked by runs on both sides of the board. In such a case group all the interconnections in one area on one side of the board and move them in one direction; then move the interconnections on the opposite side of the board in that area in the other direction. You now have a clear space between the two

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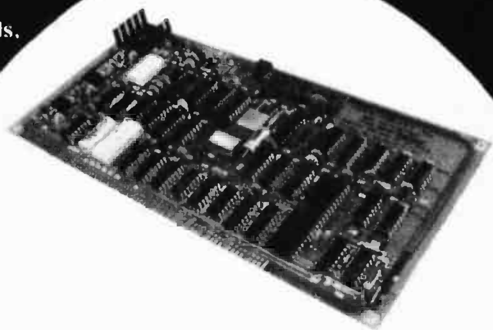

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Table 4: Materials required to construct a printed circuit board artwork master.

Mylar sheets
Black donut pads

- 0.093 inch (essential)
- 0.075 inch and 0.111 inch (helpful)
- (Other sizes per personal preference)

Black drafting Tape

- 0.015 inch, 0.040 inch, 0.062 inch suggested

Integrated Circuit lead pattern stick-ons
Targets
Drafting pen
PC design template } From table 1
Grid } From table 1
Light table } From table 1
Scotch Magic transparent tape } From table 1

groups for routing your connection via a dedicated through-hole (see figure 4a & 4b). At this point, you probably don't want to erase and move all those lines. I use a shorthand method to indicate this rearrangement (see figure 4c).

Once all the traces are drawn in place, make sure you have enough room to route traces through the crowded spots. Signal traces can be as narrow as 0.015 inch, in fact, you will find this width very easy to work with because tape in this width is extremely flexible. Spacings of 0.050 inch between conductors are easy to achieve. Avoid, if possible, running conductors closer than 0.1 inch to pads where no connection is intended. Leave at least 0.1 inch between a trace and the board edge. If you find you will have too little room for traces in a given area, calculate how much related components will need to move and mark the distance and direction on the vellum.

Congratulations! You now have a design that will be the basis of your tape-on-Mylar artwork master. Table 4 lists those materials necessary for the preparation of the artwork master.

Mylar drafting film comes in sheets and rolls. The price advantage of buying in roll form is slight and the curl of sheets cut from a roll is a nuisance at best.

Black donut pads come 500 to a pack. The 0.093 inch size will work for almost everything, but it's nice to have 0.075 inch pads on hand for the finer leads of transistors and diodes plus 0.111 inch pads to connect lead wires to the board.

I use three tape widths for most of my designs. The 0.015 inch width finds the greatest use. Power and ground runs usually use 0.040 inch or 0.062 inch widths.

Integrated circuit patterns are worth every penny for the time they save. If your requirements are modest, buy just one pack of 16 lead DIP patterns. These can be cut down to make 14 or 8 lead DIP patterns, and they can be split down the middle and arranged to make 24, 28, or 40 lead DIP patterns. Round 8, 10, or 12 lead TO-5 patterns can be accommodated by bending the device leads to fit DIP spacing. I find the 0.075 inch round pad style most suitable. Check the catalogs of the sources listed at the end of this article; many styles are available.

Targets come 250 per package, and, although expensive, are absolutely essential to assure accurate alignment of the three or four layers of artwork.

A drafting pen is used with the printed circuit design template to make an assembly drawing of your board. It will cost about $7.50 at an art supply store and is truly a joy to own.

Remove your vellum layout sheet from the light table and keep it nearby. Securely tape a Mylar sheet over the grid. Locate two targets in diagonally opposite corners of the Mylar and carefully align the centers with a grid intersection. The targets may be located inside or outside of the board area. If located within the board area, they can

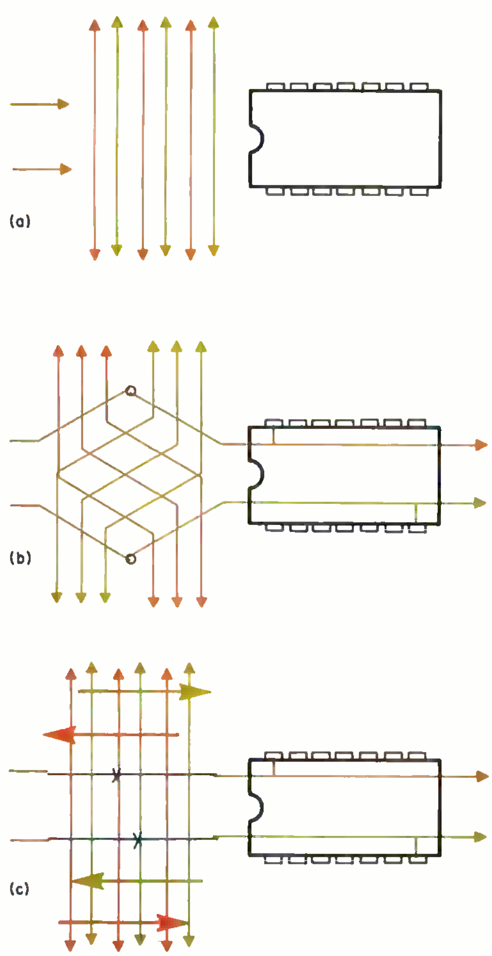

Figure 4: Figure 4a illustrates a common printed circuit board problem. The designer wishes to run conductors across a group of existing perpendicular conductor runs. Figure 4b shows how the problem can be solved by using a two sided printed circuit board with two through-holes. Figure 4c is a shorthand notation for the configuration shown in figure 4b. As before, contrasting colors indicate conductors on the respective sides of the board.

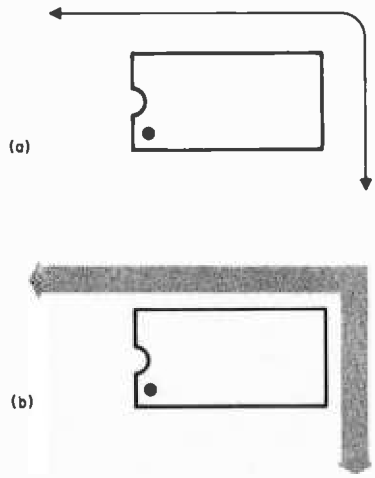

Figure 5: Two techniques for applying drafting tape around corners. Figure 5a shows the preferred method for narrow traces; figure 5b shows the technique for wide traces.

0.075 inch pad	#71 drill
0.093 inch pad	#64 drill
0.111 inch pad	#55 drill
0.125 inch pad	1/16 inch drill

Table 5: Recommended drill sizes for drilling standard printed circuit board pad holes.

double later as mounting holes. Define the board edges with short pieces of tape at the board's corners.

Now, working with a ruler marked in tenths of an inch and your vellum layout, transfer the component and through-hole locations to the Mylar using donut pads and stick-ons. Be sure to take into account the shifts notated as the last step of the layout preparation. Once all the components and through-holes appear as pad groups on the Mylar, align the vellum over the Mylar and check for missing or misplaced pads. This sheet now contains all the component pads that will appear on both sides of the board. Remove the vellum.

Tape a second sheet of Mylar directly over the first. Align targets with those on the first sheet. Using black tape, transfer all the lines appearing in red on the vellum to this sheet of Mylar. Take heed of any notes on the vellum to shift traces from their indicated positions. Narrow tapes are best routed directly with gentle corners where necessary. Wider tapes do not curve as easily and require cut corners for sharp bends (see figure 5). This sheet now contains all traces located on the solder side of the board. There are no pads on this sheet. The same procedure is followed using a third Mylar sheet and the blue lines for the component side traces.

For the sake of completeness, you should now make an assembly drawing on a fourth layer of Mylar sheet. This is done using the template by inking the component outlines aligned with their respective pads. The component designation or value should be included within or beside the outline using pen and ink or dry transfer lettering.

Your master artwork is now complete and should be rechecked for accuracy.

To make negatives of solder-side and component-side artwork for use in photographically etching your board, simply align the Mylar sheet containing only pads with either of the sheets containing only traces before making a contact negative. The details of the negative-producing operation are well covered in the hobbyist magazines, and most local electronics stores sell printed circuit board etching kits.

You now have a negative for each side of your printed circuit board. Before coating your board with photoresist, pick two holes near diagonally opposite corners and accurately transfer their locations to the laminate. Use a very small drill to make these two holes. You now have reference points by which you can align the negative on each side of the board. The board is now photo etched on both sides.

All that remains is to drill the holes, mount the components, and solder the leads. Table 5 shows recommended drill sizes for various sizes of pads. When mounting components, crimp the leads flat against the solder side. Dedicated through-holes are stuffed with a short piece of wire crimped to the board on both sides. Solder leads on both sides of the board where necessary for through-board connections. As an alternative to soldering on both sides, you can crimp eyelets in the holes or get someone to process your board with plated through-holes.

Well, that's all there is to it. Now you can put that very large project of yours on a printed circuit board. (The very first printed circuit board I ever designed had 26 integrated circuits, 144 resistors, 44 capacitors, 28 transistors, 30 diodes, and 23 indicators. I completed the master artwork using the techniques I have just described in less than 40 hours.) A homebrew double sided printed circuit board may be just the solution you're looking for.■

Sources of printed circuit board artwork supplies:

1. Bishop Graphics Inc.
   20450 Plummer St
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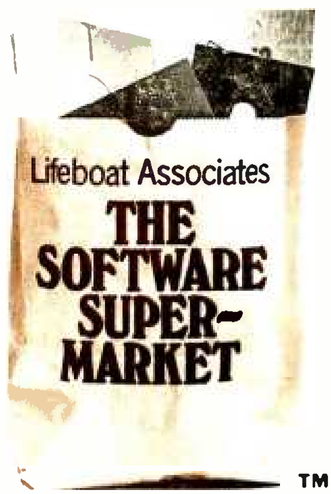

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INTEL, TEXAS INSTRUMENTS AND IBM MAKE MEMORY NEWS. Intel has again beat its competitors to the marketplace with a new product. This time it is the 32 K byte programmable read only memory, called the 2732, following in the footsteps of the 2716 and the 2708. It is pin compatible with the 2716 16 K erasable byte read only memory, and is organized as 4 K by 8 bit words. It has a 450 ns access time and operates from a single 5 V power supply. Further, a separate chip-enable input reduces power dissipation by 80 percent (from 150 mA to 30 mA) when the device is not selected. The single unit price is $147.30 and drops to $91.65 in quantity. Intel claims the 2732 is now available in production quantities.

Texas Instruments has been sampling their new 64 K bit dynamic programmable memory (TMS-4164) since last fall to selected customers and expects to be in quantity production by the last quarter of this year. Motorola also recently began sampling their 64 K bit programmable memory and hopes to be in production by year-end (initial price is $130).

IBM, at a recent International Electron Devices meeting, disclosed that they had made an experimental MOS gate with channel lengths of 1.3 to 1.0 micrometers. This represents a significant breakthrough in very large scale integrated (VLSI) circuit technology. Using this technology it is now possible to build a 256 K bit memory part. Further, IBM reports that these devices have switching times of 230 picoseconds, which is three to four times faster than previous MOS circuits, and dissipate one tenth the power.

BUBBLE MEMORIES INCREASING IN AVAILABILITY. Texas Instruments and Rockwell are currently the only two manufacturers of bubble memories and their maximum size devices are only 256 K bits. National Semiconductor is expected to start sampling their 256 K device later this year. Also, look for Intel to enter the market before year-end. However, prices are still very high, compared to disk storage technology, and production is still very limited. Don't look for their use in microcomputers until the early 1980s, when bit capacity is up in the megabyte size and competition develops. Currently, bubble memories are being used in applications where the electro-mechanical disk systems are not rugged enough.

FLOPPY DISK IMPROVEMENTS COMING. Floppy disks are going to be with us for some time to come. It is expected that next year will see the introduction of 5 to 10 M byte floppy disks due to higher track density. This will be made possible by having the disk supply its own track positioning data and by improvements in media technology, allowing for narrower tracks. 5 inch floppies will be expanded to the 1 to 2 M byte range, per disk.

Projections for 1980 are that bubble memory will drop to 0.1 cent per bit while disk will cost 0.0001 cent per bit. Further, projections are for bubble memory prices to drop to only 0.02 cent per bit by 1985.

In the meantime, floppy disks, first introduced in 1973, saw sales of close to 270,000 units last year with sales for this year expected to be over 350,000.

FLAT SCREEN TERMINALS ARE COMING. General Telephone and Electronics (GT&E) has announced that they are far along in development of a flat screen display using cathodoluminescence. They are working on it jointly with Lucitron Inc. GT&E predicts that the display will be in production by 1981 at the latest. A color display, using the same technique, is also being developed. The system will permit large displays, up to 50 inches (127 cm, measured diagonally) and approximately three inches thick. The Lucitron panels use a "self-scanning" system which does not require complex drive circuitry. The initial display panels will be used for computer terminals, with television type displays, providing good gray scale, following a year or two later.

APL ON A MICROCOMPUTER FOR $2000 AVAILABLE SOON. APL buffs waiting patiently for a home APL system will finally get their dream. Alan Rose, of Scientific Time-Sharing Corp, considered one of the APL authorities, reports that he and a small company called Quark will soon introduce a microcomputer system dedicated to APL. It will run the full APL language, as implemented by IBM and Scientific Time-Sharing Corp. It will be easily expandable in I/O and peripheral mass storage and will execute two to four times faster than the IBM 5100 APL machine. The unit, which will use the Intel 8086 16 bit processor, will contain its own keyboard and display and can be used in either a stand-alone mode or as an intelligent APL terminal to a host system. The best news is that the system price will start at only $2000. Look for availability this summer.

Although several "tiny APL" interpreters have been brought out for microcomputers, and IBM has a micro-APL in their 5100 desktop computer, these implementations have left a great deal to be desired. Vanguard Systems in Austin TX has available an excellent Z-80 APL interpreter which we understand will be licensed soon to one or more computer manufacturers. Microsoft had advertised their version of APL for some time, but as far as we know have not started delivery yet.

FCC TAKING ACTION ON RADIATING COMPUTERS AND GAMES. After severe interference problems that occurred with Citizen's Band radio interference on television sets, the FCC sought to regulate devices which employ radio frequency modulators. This is also the case with computers and electronic games that are connected to standard television sets via radio frequency modulators. Manufacturers are required to submit their units to the FCC for approval and licensing. Passing the standards appears quite difficult and so far only a few units have obtained approval. Several manufacturers have gotten around the problem by providing only video signal output, which means that the user must use a video monitor or TV set with special video input. Some manufacturers have ignored the FCC regulations and sold unlicensed units.

Recently the FCC served a cease-and-desist order on some personal computer system owners because of interference on neighbors sets. The FCC is also talking about imposing marketing sanctions on those companies who fail to meet interconnect qualifications.

PERSONAL COMPUTERS GOING GREAT IN EUROPE. Sales of personal computer systems are going great on the Continent. The Germans report that sales are soaring. An estimated 4000 PETs were sold in 1978, primarily to home users. Commodore is manufacturing the PET in England. Tandy also reports greater than expected sales, but has not disclosed figures. Tandy started selling the TRS-80 last summer through 340 stores. In Germany the TRS-80 (Level I) sells for $935 compared to $595 in the states. The Apple computer is being handled by ITT, who reports excellent sales. The TRS-80 and Apple are manufactured in the USA. Things will change this year as Seimens, one of the largest European electronics manufacturers, will soon announce their own personal computer system.

Interestingly, one of the major sales outlets for personal computer systems has become department stores. Several US department stores have tried selling personal computer systems but have withdrawn.

MICROPROCESSOR MAKERS MOVE INTO COMPUTER SYSTEMS BUSINESS. Integrated circuit manufacturers are going into competition with their customers, the computer systems manufacturers. Texas Instruments was one of the first. They have been selling complete minicomputer systems for several years now. Additionally, they have seen selling 16 bit systems using their 9900 processor and now also will soon introduce a personal computer system using the 9900.

National Semiconductor is now selling a large system to replace IBM-370s and will soon offer for sale a microprocessor version of the DEC PDP-11 16 bit computer system. Also, Fairchild will soon sell a system that is compatible with the Data General NOVA computer system.

Zilog late last year introduced their system using the Z-80. It is a business-oriented system and has a full complement of computer languages, including BASIC, FORTRAN and COBOL; business application software packages are also offered. A Z-8000 based system is expected in the fall.

Intel is rumored to be working on a very powerful data base system using an associative processor to handle searching, inserting, deleting, etc, among an array of storage devices and host interfaces. The system will utilize a 16 bit processor and CCD memory that will represent a breakthrough in data base computer technology. Introduction is expected in 1980.

TANDY REVAMPS ITS COMPUTER MARKETING. Early last year Tandy opened a computer store in its Fort Worth TX building complex and also issued a computer catalog. The store and the catalog carried the Radio Shack TRS-80 and a wide variety of products ranging from the IMSAI 8080 to the Video Brain computers. Tandy considered it an experiment. The TRS-80 accounted for 80 percent of the sales. Now Tandy has decided on a new marketing approach. They have already opened five computer stores (Richardson, Dallas and Fort Worth TX, and New York City and Washington DC) and plans to open others soon in Tampa, Atlanta, San Francisco and Los Angeles. Each store will have a classroom and repair facilities.

Further, the stores will carry only three different computer systems. The TRS-80, Tandy-10 and Tandy-150 systems. The Tandy-10 is made for Tandy by Digital Data Systems (DDS) and will have a base price of $8995. Using an 8080, it will have a video display, keyboard, 48 K bytes of programmable memory, two 8 inch floppy disk drives, BASIC and a disk operating system similar to CP/M. The initial order placed by Tandy with DDS was reportedly for 250 systems. The Tandy-150 will be assembled by Tandy and use a Computer Automation 16 bit processor. Starting at $21,995, it will include a 10 M byte hard disk.

Sol Libes
ACGNJ
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Springfield NJ 07081

...And the future

THE BYTE BOOK OF COMPUTER MUSIC combines the best computer music articles from past issues of BYTE Magazine with exciting new material—all written for the computer experimenter interested in this fascinating field.

You will enjoy Hal Chamberlin's "A Sampling of Techniques for Computer Performance of Music", which shows how you can create four-part melodies on your computer. For the budget minded, "A $19 Music Interface" contains practical tutorial information—and organ fans will enjoy reading "Electronic Organ Chips For Use in Computer Music Synthesis".

New material includes "Polyphony Made Easy" and "A Terrain Reader". The first describes a handy circuit that allows you to enter more than one note at a time into your computer from a musical keyboard. The "Terrain Reader" is a remarkable program that creates random music based on land terrain maps.

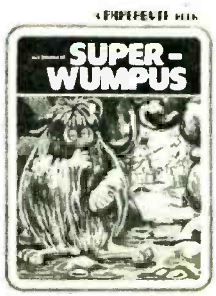
Other articles range from flights of fancy about the reproductive systems of pianos to Fast Fourier transform programs written in BASIC and 6800 machine language, multi-computer music systems, Walsh Functions, and much more.

For the first time, material difficult to obtain has been collected into one convenient, easy to read book. An ardent do-it-yourselfer or armchair musicologist will find this book to be a useful addition to the library.

NEW

ISBN 0-931718-11-2
Editor: Christopher P. Morgan
Pages: approx. 128
Price: **$10.00**

SUPERWUMPUS is an exciting computer game incorporating the original structure of the WUMPUS game along with added features to make it even more fascinating. The original game was described in the book **What To Do After You Hit Return,** published by the People's Computer Company. Programmed in both 6800 assembly language and BASIC, SUPERWUMPUS is not only addictively fun, but also provides a splendid tutorial on setting up unusual data structures (the tunnel and cave system of SUPERWUMPUS forms a dodecahedron). This is a **PAPERBYTE™** book.



ISBN 0-931718-03-1
Author: Jack Emmerichs
Pages: 56
Price: **$6.00**

TINY ASSEMBLER 6800, Version 3.1 is an enhancement of Jack Emmerichs' successful Tiny Assembler. The original version (3.0) was described first in the April and May 1977 issues of BYTE magazine, and later in the **PAPERBYTE™** book **TINY ASSEMBLER 6800 Version 3.0.**

In September 1977, BYTE magazine published an article entitled, "Expanding The Tiny Assembler". This provided a detailed description of the enhancements incorporated into Version 3.1, such as the addition of a "begin" statement, a "virtual symbol table", and a larger subset of the Motorola 6800 assembly language.

All the above articles, plus an updated version of the user's guide, the source, object and PAPERBYTE™ bar code formats of both Version 3.0 and 3.1 make this book the most complete documentation possible for Jack Emmerichs' Tiny Assembler.

ISBN 0-931718-08-2
Author: Jack Emmerichs
Pages: 80
Price: **$9.00**

A walk through this book brings you into **Ciarcia's Circuit Cellar** for a detailed look at the marvelous projects which let you do useful things with your microcomputer. A collection of more than a year's worth of the popular series in BYTE magazine, **Ciarcia's Circuit Cellar** includes the six winners of BYTE's On-going Monitor Box (BOMB) award, voted by the readers themselves as the best articles of the month: **Control the World** (September 1977), **Memory Mapped IO** (November 1977), **Program Your Next EROM in BASIC** (March 1978), **Tune In and Turn On** (April 1978), **Talk To Me** (June 1978), and **Let Your Fingers Do the Talking** (August 1978).

Each article is a complete tutorial giving all the details needed to construct each project. Using amusing anecdotes to introduce the articles and an easy-going style, Steve presents each project so that even a neophyte need not be afraid to try it.

NEW

ISBN 0-931718-07-4
Author: Steve Ciarcia
Pages: approx. 128
Price: **$8.00**

is right now!

BASEX, a new compact, compiled language for microcomputers, has many of the best features of BASIC and the 8080 assembly language—and it can be run on any of the 8080 style microprocessors: 8080, Z-80, or 8085. This is a **PAPERBYTE™** book.

Subroutines in the **BASEX** operating system typically execute programs up to five times faster than equivalent programs in a BASIC interpreter—while requiring about half the memory space. In addition, **BASEX** has most of the powerful features of good BASIC interpreters including array variables. text strings, arithmetic operations on signed 16 bit integers, and versatile IO communication functions. And since the two languages, BASEX and BASIC, are so similar, it is possible to easily translate programs using integer arithmetic data from BASIC into BASEX.

The author, Paul Warme, has also included a BASEX Loader program which is capable of relocating programs anywhere in memory.

NEW

ISBN 0-931718-05-8
Author: Paul Warme
Pages: 88
Price: **$8.00**

PROGRAMMING TECHNIQUES is a series of **BYTE BOOKS** concerned with the art and science of computer programming. It is a collection of the best articles from BYTE magazine and new material collected just for this series. Each volume of the series provides the personal computer user with background information to write and maintain programs effectively.

The first volume in the Programming Techniques series is entitled **PROGRAM DESIGN.** It discusses in detail the theory of program design. The purpose of the book is to provide the personal computer user with the techniques needed to design efficient, effective, maintainable programs. Included is information concerning structured program design, modular programming techniques, program logic design, and examples of some of the more common traps the casual as well as the experienced programmer may fall into. In addition, details on various aspects of the actual program functions, such as hashed tables and binary tree processing, are included.

ISBN 0-931718-12-0
Editor: Blaise W. Liffick
Pages: 96
Price: **$6.00**

SIMULATION is the second volume in the Programming Techniques series. The chapters deal with various aspects of specific types of simulation. Both theoretical and practical applications are included. Particularly stressed is simulation of motion, including wave motion and flying objects. The realm of artificial intelligence is explored, along with simulating robot motion with the microcomputer. Finally, tips on how to simulate electronic circuits on the computer are detailed.

ISBN 0-931718-13-9
Editor: Blaise W. Liffick
Pages: approx. 80
Price: **$6.00**
Publication: Winter 1979

RA6800ML: AN M6800 RELOCATABLE MACRO ASSEMBLER is a two pass assembler for the Motorola 6800 microprocessor. It is designed to run on a minimum system of 16 K bytes of memory, a system console (such as a Teletype terminal), a system monitor (such as Motorola MIKBUG read only memory program or the ICOM Floppy Disk Operating System), and some form of mass file storage (dual cassette recorders or a floppy disk).

The Assembler can produce a program listing, a sorted Symbol Table listing and relocatable object code. The object code is loaded and linked with other assembled modules using the **Linking Loader LINK68.** (Refer to **PAPERBYTE™** publication **LINK68: AN M6800 LINKING LOADER** for details.)

There is a complete description of the 6800 Assembly language and its components, including outlines of the instruction and address formats, pseudo instructions and macro facilities. Each major routine of the Assembler is described in detail, complete with flow charts and a cross reference showing all calling and called-by routines, pointers, flags, and temporary variables.

In addition, details on interfacing and using the Assembler, error messages generated by the Assembler, the Assembler and sample IO driver source code listings, and **PAPERBYTE™** bar code representation of the Assembler's relocatable object file are all included.

This book provides the necessary background for coding programs in the 6800 assembly language, and for understanding the innermost operations of the Assembler.

ISBN 0-931718-10-4
Author: Jack E. Hemenway
Pages: 184
Price: **$25.00**

to order books see next page .....

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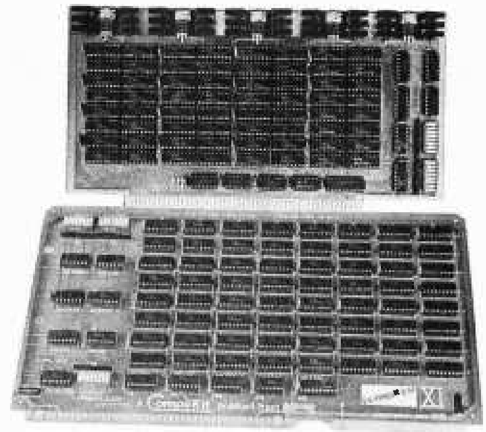

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Designing a Robot from Nature

Part 2: Constructing the Eye

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1(a)

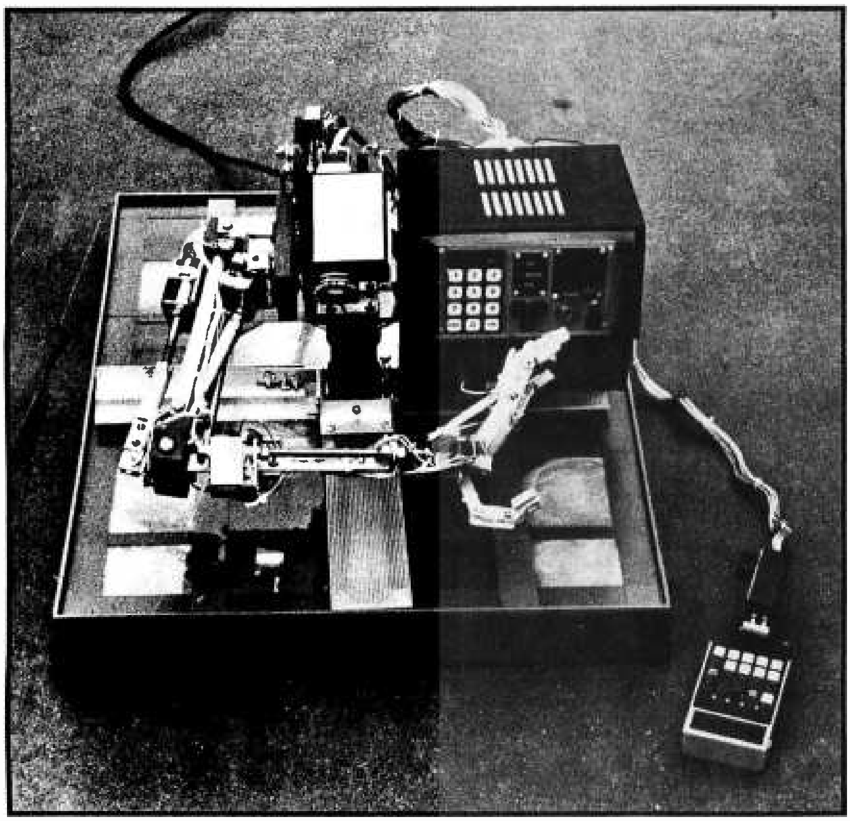


Photo 1: The author's NELOC (neural logic cyberanimate). The manipulator arm (with five degrees of freedom) and the 8008 computer (at upper right) are shown. The object resembling a TV camera is actually a sustained contrast detector used to obtain a rough image of the object to be grasped (see photos 4a and 4b and figure 7). Just below and to the right of the sustained contrast detector is a small box called the net convexity detector (see photo 5), which detects the direction of motion of an LED mounted on the hand of the manipulator and feeds this information into the homebrew computer. Photos 1(b), 1(c), and 1(d) show the arm in action.

The first piece of hardware to be built in my system was the manipulator. From the start it was obvious that a tongue-manipulator concept would be impractical; I chose remote operator control over the manipulator arm because I wanted to program manipulator motion by "teaching," and also to assist the system during its operation if necessary.

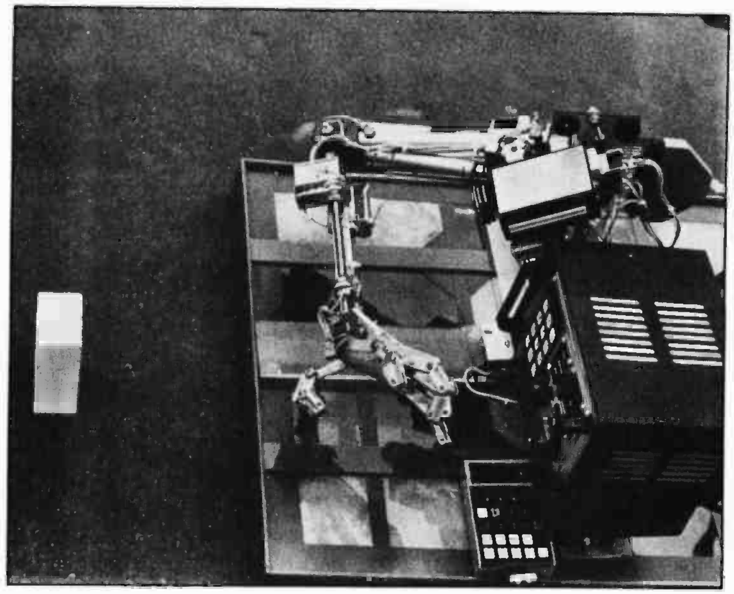
The manipulator I designed was roughly modeled after a human arm, with regard to its actions and dimensions. The manipulator is capable of five degrees of freedom, making it suitable for control by the motion of joints in a remote operator's arm. The prototype arm was originally designed to be pneumatically operated, but electric motors were substituted for convenience during testing. The motors (which accurately simulate the actions of pneumatic pistons and their servo valves) are electro-optically controlled. To start a motor or open a valve, the optocoupler connecting the motor or valve to the circuit's ground must be activated. Next, the forward or reverse coupler must be illuminated, connecting the motor or valve to a positive or negative voltage source, thereby causing the motor or air piston to extend or retract its portion of the manipulator. The only feedback devices located on the arm are two microswitches located just before the limit of travel of each joint. These microswitches provide either a full extension or full retraction signal for each joint. There is also a set of tactile sensor switches located in the fingertips of the device. Even though this manipulator may appear to have little in common with the frog, almost every facet of its design has been mentioned, in one form or another, in the previous (see February 1979 BYTE, page 12) analysis. The optoisolators, for instance, resemble the neuromuscular junctions in function, being the point where control signals leave the processing system and enter the motive system. The switches in the joints approximate the neuromuscular spindles. The tactile switches resemble the innervated capsules in the skin. And the entire manipulator itself is a folding, prehensile device, as is the frog's tongue.

Net Convexity Detector

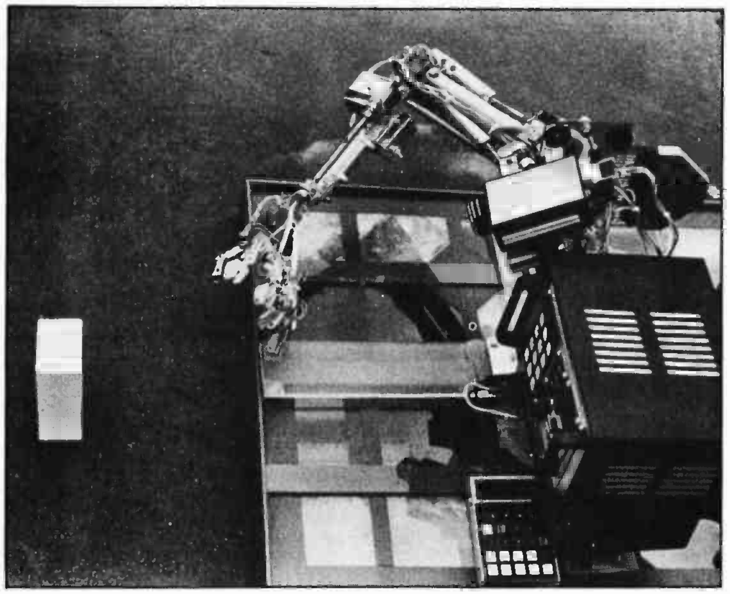
Other structures developed for the turret system more closely resemble their biological counterparts. To monitor the motion of the manipulator more closely, my system requires a device that can track the motion of the arm. A matrix of net convexity detectors proved more than adequate for the task. By monitoring a small bright spot of light either reflected from a retroreflector or emitted from a brilliant LED (light emitting diode) source located on the manipulator, the net convexity detectors can easily monitor the motion of the manipulator. The net convexity detectors built for the turret system utilize the concepts of receptor geometry, weighting (for processing), and output suppression for size discrimination.

Building a small matrix of net convexity detectors could involve the use of possibly hundreds of sensors and many processing devices, but since I was not concerned with building an accurate model of the net convexity detector in the frog's retina, I could trade off various design features. For example, I deduced that 20 is the minimum number of receptors required to define motion on at least four axes. The geometry of these receptors has to be in a matrix of four columns by five rows with the high sensitivity receptor occuring in the fifth row, third column (see figure 6 and boxed text at end of article). In the frog, a net convexity detector may have up to 100 receptors in its receptor field, allowing the frog to precisely monitor the angle of the insect's trajectory, but to duplicate this would require the use of a monolithic digital sensor of photodiodes if the system were to be portable. Even a 4 by 5 matrix would require a 1 inch square surface to contain all of the detectors. This means that four net convexity detectors would require a 2 by 2 inch imaging surface — impractical both in terms of size and optics. Another serious problem was scanning and processing the information from the photoelectric devices.

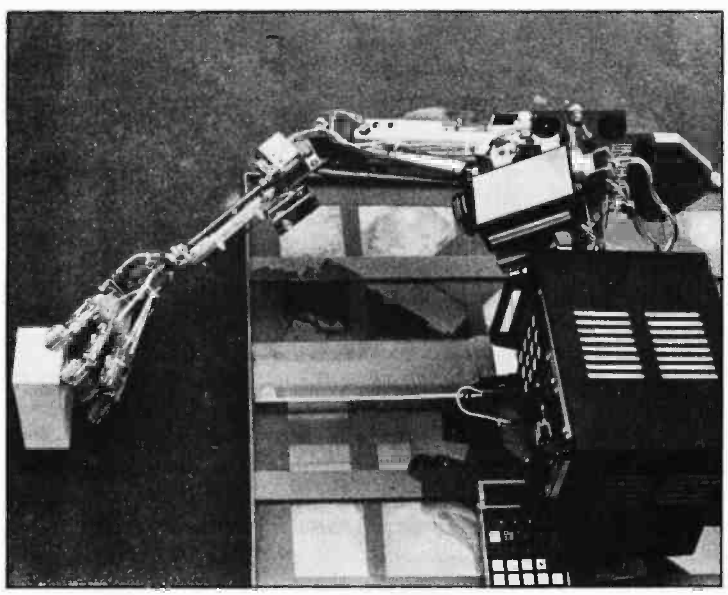
Text continued on page 119



1(b)



1(c)



1(d)

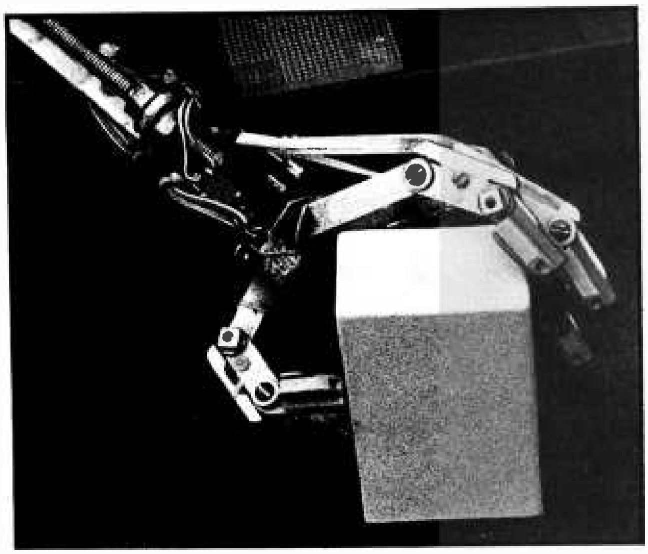


Photo 2: Close-up of the manipulator's hand.

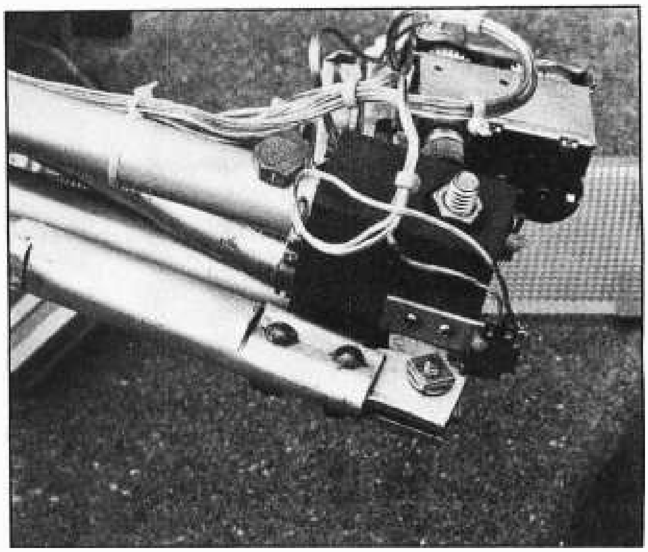


Photo 3: Elbow of the manipulator.

Sources of Parts

A few items mentioned are available only from single sources:

National Semiconductor 650 calculator modules are available from Poly Packs, POB 942, South Lynnfield MA 01940.

The best sheet plastic and cement I have found for hobby use can be purchased from Plastruct Inc, 61 Monterey Pass Rd, Monterey Park CA 91754.

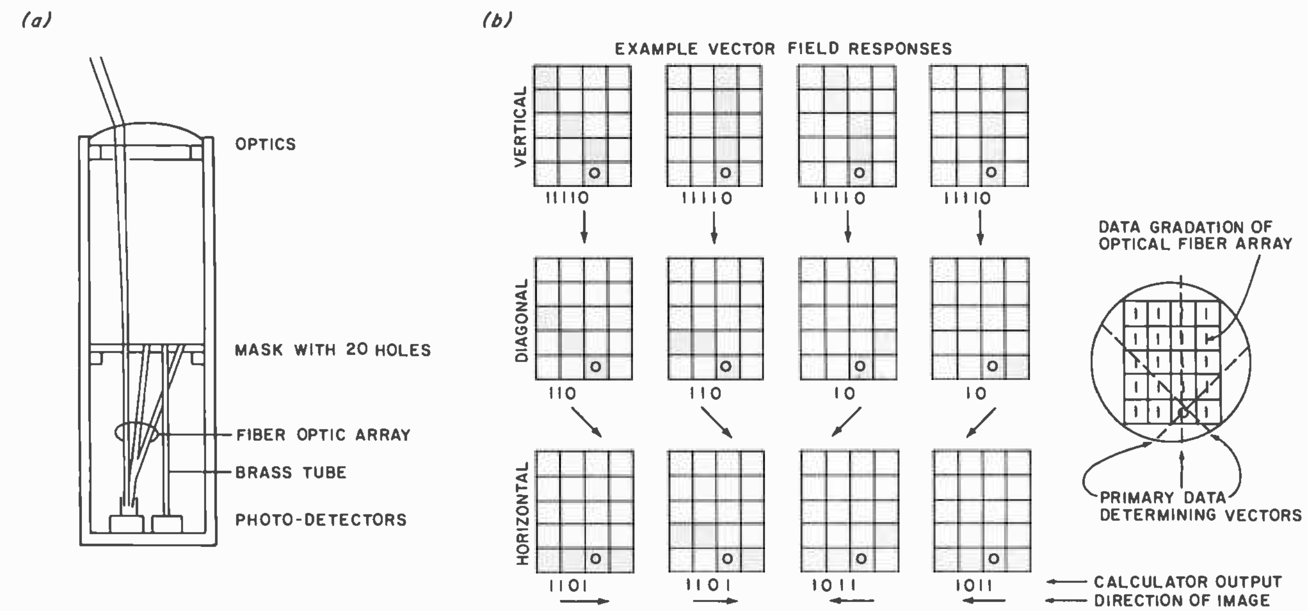
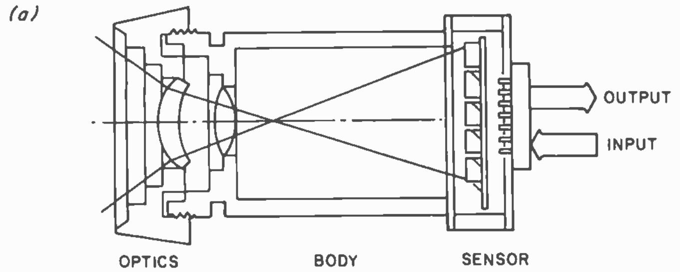


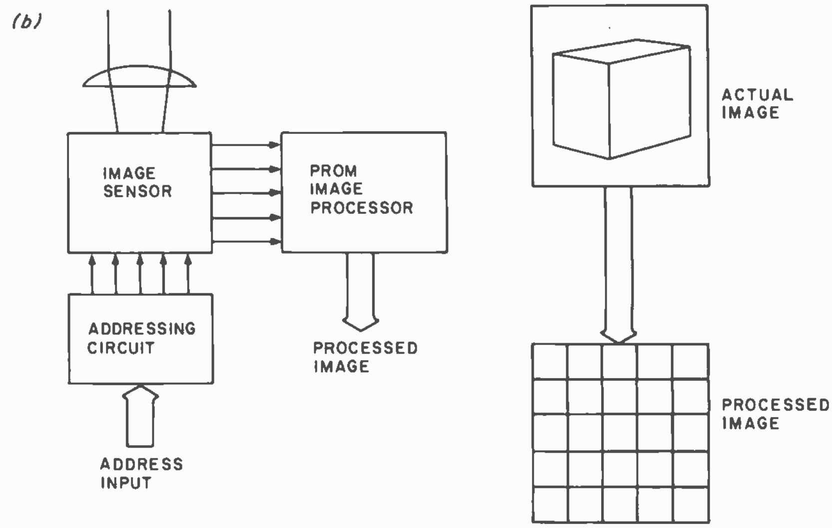
Figure 6: Shown at (a) is a sectional view of the net convexity detector, used to determine the motion vector of the manipulator arm. Light entering the lens passes through one of 20 holes in a 4 by 5 array at any instant of time, and impinges on one of a corresponding set of phototransistors. 19 of these photo-darlingtons (the low sensitivity detectors) activate the 1 key of a calculator module. The remaining photo-darlington activates the 0 key; its off-center location is used to uniquely determine the arm's direction of travel. (The final version of the unit does not use fiber optics bundles, except inside the brass tube. See figure 9 and accompanying text box.) At (b) are some examples of typical vectors passing over the retina, along with the corresponding calculator outputs.


Helios II

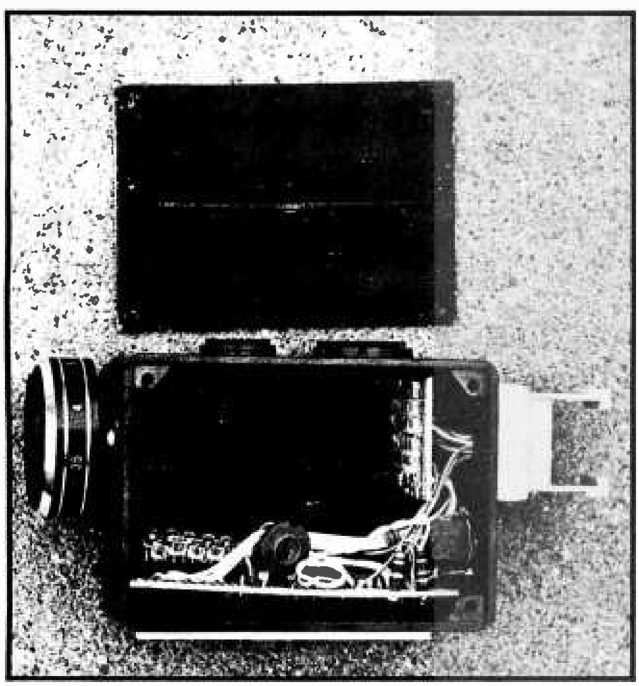


The figure numbering sequence for this article has been continued from part 1 (February 1979 BYTE, page 12).

Figure 7: Details of the sustained contrast detector. At (a) is a cross section of the unit, which resembles a television camera; (b) is a simplified block diagram of the system. The sustained contrast detector is used to obtain a rough image of the object to be grasped by the manipulator.



4(a)



4(b)

Photo 4: Interior of the sustained contrast detector. Shown at (a) is the lens (at left), the array of phototransistors (at right), and the associated electronics. 4b shows the 4 by 5 prototype array (compare with final version in figure 7).

Text continued from page 115

I solved both problems by using a simple 6 digit, 4 function calculator integrated curcuit, the National Semiconductor MM 50736. Before I began work on the neural logic cyberanimate, I had experimented with this device and found it to be compatible with photo-darlington transistors 2N5777 thru 2N5780. With the photo-darlington transistors as input devices, the calculator circuit could register pulsations of light from a diffused LED source more than two feet away. Clearly this device was capable of detecting bright objects at short distances. Additionally, it was possible to use the data processing nature of the calculator circuit to assign different values to the receptors and, based on these values, produce two distinct output signals. The weighted inputs were made simply by attaching one photo-darlington amplifier to the calculator circuit where the 1 switch of the keyboard would normally be connected, and a second photo-darlington to what would normally be the 0 position.

The two types of output signals are the results of the data which the photo-darlingtons receive. Note that there are only two photo-darlingtons connected to the calculator circuit in figure 6, yet I had previously stated that the minimum configuration for the net convexity detector was a matrix of 20. This is because I used fiber optic pipe for "receptors" and the photo-darlington devices as detectors. Figure 6b shows the arrangement of the optical fibers. 19 fibers have a value of 1 (they are equivalent to the low sensitivity receptors). All 19 of these fibers are fused to the photo-darlington that has a numerical value of 1. The remaining fiber is fused to the 0 value photo-darlington (to simulate the high sensitivity receptor). The completed device can detect and record the trajectory of a small moving penlight flashlight at a distance of 4 feet (well beyond the extended length of the manipulator); obviously, if the object's path does not cross the high sensitivity detector, the data is invalid.

Sustained Contrast Detector

Another structure derived from my analysis is a sustained contract detector (figure 7). This device is a spinoff of a previous electro-optic project. But without the analysis of the frog's eye I would never have considered this application. The sensor consists of a matrix of five rows by five columns of photo-darlington transistors (see photo 4). The columns of the sensor are scanned by TTL (transistor-transistor logic) devices controlled by the computer. The 5 row output is fed into a programmable read only memory that serves two functions. First, the logic voltage level on the address lines of the programmable read only memory sets the on/off contrast levels for the sensors, thus eliminating the gray scale conversion problem. Second, the programmable read only memory is encoded with a truth table that can vertically reduce

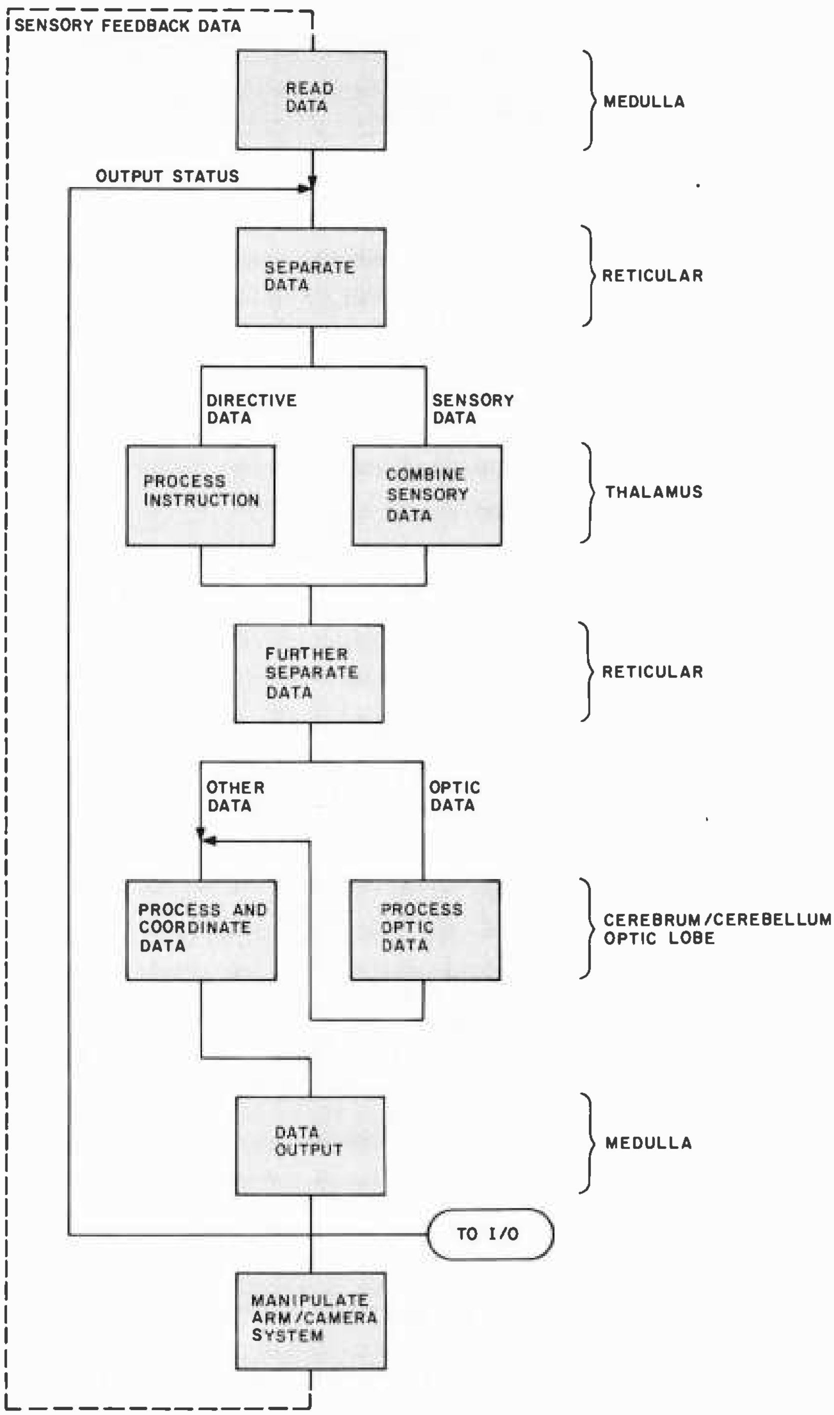


Figure 8: Simplified system flowchart, showing parallel functions in the brain.

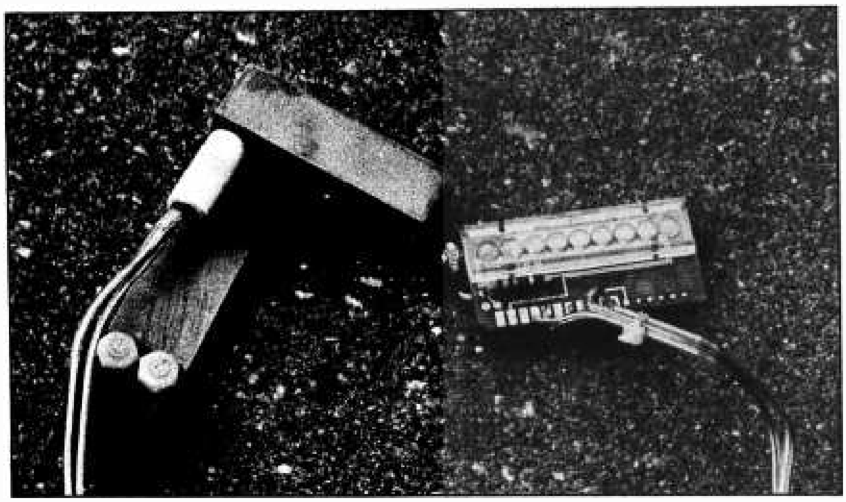


Photo 5: The net convexity detector, shown with the National Semiconductor NS 650 calculator module (connecting wires not fully visible). The calculator module used in the final version is an MM 50736, which has no readout. The NS 650 is useful for readers who will not be interfacing the unit to a computer immediately, since it does have a readout.

a high contrast image line by line with the computer's assistance. The image reduction process will horizontally outline an image and vertically dimension it (see figure 7 and photos 4a and 4b), enabling the computer to gauge the dimensions of objects within reach of the manipulator.

Finally, there was the design of the processing system. By designing all of the most external appliances first, I hoped to further define some of the required characteristics of the neural logic cyberanimate. The purpose of my processing system (including the computer program, preprocessing, and postprocessing elements) as stated before, is to locate, classify, and manipulate objects specified by control instructions. To accomplish this, the system first has to be able to recognize the command instructions that specify the location of the object to be manipulated and what is to be done with it. Next, the system has to use measurements of pressure and reflected light from the environment made by the sensory instruments. Once in the processing system, this information has to be recognized and labeled. Incorrect or unnecessary measurements will then be eliminated. The filtered measurements will then be combined according to their information content (ie: optical and mechanical data relating to the position of the manipulator would be combined, etc). The combined data, whether optical, optical-mechanical, or mechanical, is then processed according to its type. Optical data is reduced to information pertaining to object size and location. Optical and mechanical information processing describes the location and position of the manipulator. Processed mechanical information relates manipulator position and contact with an object. Based on the results of this processing, the system then has to grasp and move the object as specified by the command instructions. Following this, the system notifies the command system.

The processing system uses an 8008 processor (not the best choice, but one which was chosen for expediency since I already owned one) interfaced to a series of 8223 programmable read only memories used to decode gray scale images, fire the LEDs in the optocouplers, and perform the various other tasks in the system.

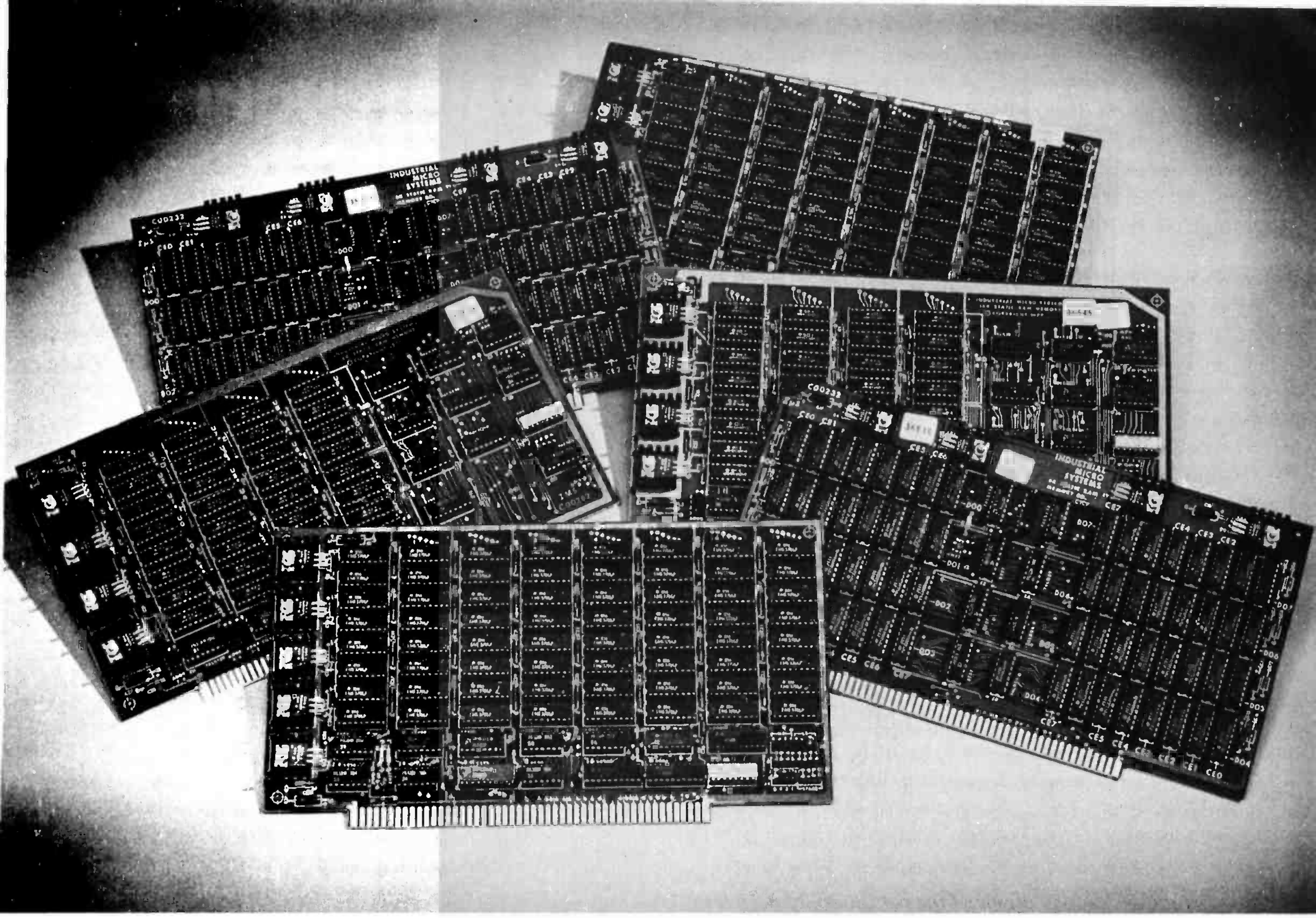
The algorithm for the NELOC system is diagramed in figure 8. Notice in the algorithm that sections of the program perform functions similar to those discussed in the cyberanimetric analysis of the brain. For example, monitoring, filtration, and suppression of sensory data, which are reticular functions, are performed in the program. Also in the algorithm are routines that combine sensory data, process and coordinate it, and control the input and output of data-functions that simulate those of the frog's brain. Another routine placed in the algorithm accepts instructions from the I/O and converts them into a form that can be used by the rest of the program. This routine makes it possible to control the system by external command.

During its trial operation, the neural logic cyberanimate performed quite well. With electric motors driving the manipulator arm, it took the system about 60 seconds to find and manipulate a test object. The most impressive feature of the system's operation is its ability to resolve the position of the manipulator and the test object.

Conclusion

During the design and construction of the NELOC system I encountered no major design problems because, from the start, it was possible to determine what portions of the system would be difficult to design or construct, and, therefore, I could budget my time and money accordingly. The benefits of clearly defining the organization of the system before designing the hardware are obvious. I put about 120 hours into the research, design, and construction of the prototype neural logic cyberanimate. If I had tried to develop these structures without the cyberanimetric philosophy, it would probably have taken much longer to design a net convexity detector or a reticular system.

Of course the NELOC system itself represents the equivalent of only a very thin neurological slice through a simple organism. By no measure is the neural logic cyberanimate intelligent, but I believe this design philosophy could be useful for designing systems beyond the simple servo system.



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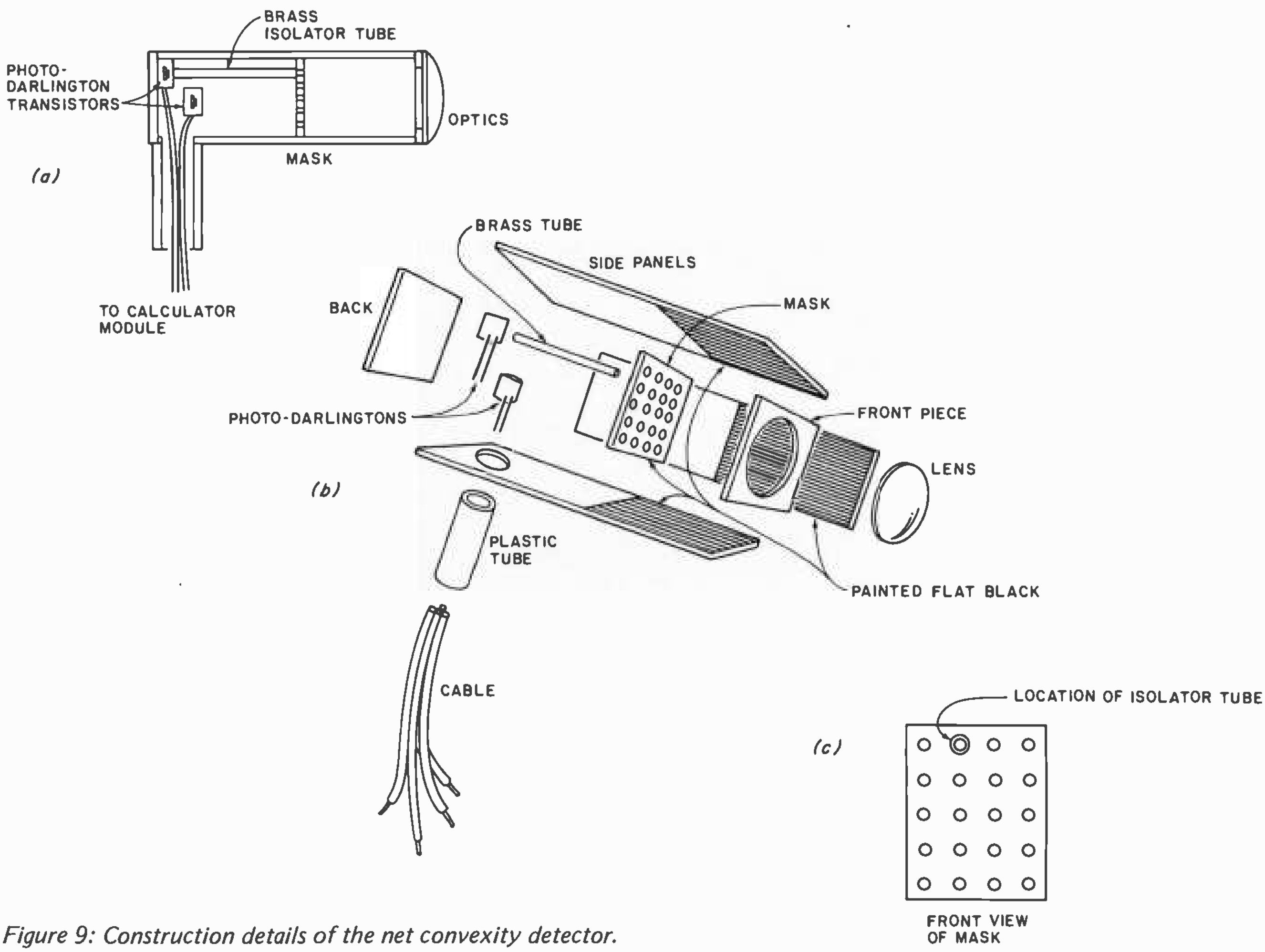

Figure 9: Construction details of the net convexity detector.

Building the Net Convexity Detector

The net convexity detector used in my system is a good example of how a calculator circuit can be used for noncalculator application. As illustrated in figure 9, the net convexity detector is a very simple device. The whole idea behind the circuit's operation is that the sensory head can, in effect, push the right keys on the calculator in response to the motion of an image that is a certain size and brightness. As explained previously, the purpose of the net convexity detector is primarily to define angle and direction of a small bright object. In this design, a mask is used as a template to gauge the diameter of an image. If a bright, moving image is small enough to illuminate only one hole of the template at a time, the calculator will register its movement as a series of numbers. If the image is too large, and illuminates more than one hole at a time, the calculator will display only one number that, in terms of a trajectory, would mean nothing.

To build the net convexity detector it is first necessary to build the sensor head. Figure 9b is an exploded view of the sensor. In the construction of the sensor it is necessary to use a lens that forms a focal point at a distance no shorter than 25 mm. Next a case is constructed from sheet plastic. This case should be at least twice as long as the focal point of the lens and must be able to hold a mask containing a 4 by 5 matrix of holes. The simplest way to make the mask is to use a piece of unclad perforated circuit board with holes 2.5 mm on center. Just cut a corner of the board off so the piece will have four by five holes. The mask must then be secured in the case so it will be at the lens's focal point. The inside of the forward end of the case must now be painted flat black. Two end pieces are cut, one is drilled to accommodate the lens and is glued to the front of the case. Next, a 4 lead cable is brought through a hole drilled in the end of the case. A short piece of plastic tube is glued over this hole and filled with epoxy to block light. Two photo-darlingtons are attached to this cable. Notice in figure 9 how a length of brass tube is aligned with one of the photo-darlingtons. This tube must be located in the second column of the first row for the sensor to work properly. This tube carries the image to the 0 value darlington only. The tube must be carefully glued to the mask and the darlington by a very small amount of epoxy glue. The photo-darlington and epoxy joint are then painted black. Before attaching the back of the case, make sure that the 1 value photo-darlington is in the center of the case.

After the sensor has been completed, it is a simple matter to complete the circuit. A National Semiconductor calculator module, the NS 650, has all of the solid state electronics for a calculator, including a 6 digit display. By adding a battery, switch, and the sensor head (see figure 10), the circuit is finished.

To test the circuit, use a small penlite type flashlight, moving it in board circles at a distance of 3 feet away from the sensor. Many 1s and a few 0s should fill the display until the calculator indicates an overflow. If you move the light source on a straight vector that crosses the hole to the isolated darlington you will get a certain readout. Figure 6b shows all of the possible fields of vectors, the direction that the object must be traveling, and the output that should be displayed by the calculator. All other combinations are illegal.

Although the net convexity detector is a very simple device, it must be built very precisely. All surfaces should be flush, parallel, or perpendicular. Optics should be carefully aligned and all seams should be checked for light leaks.■

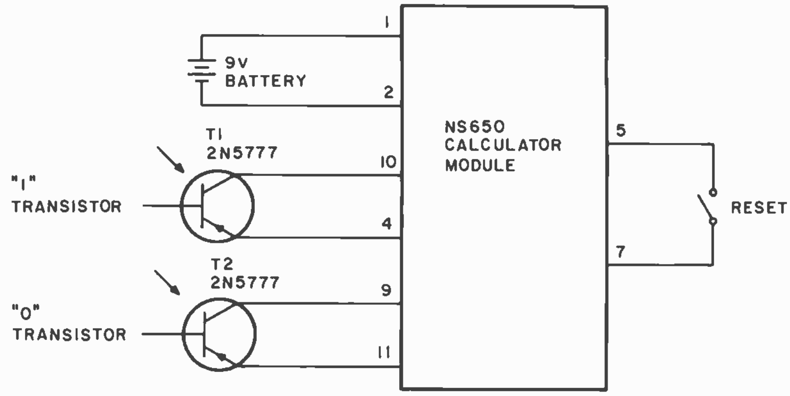

Figure 10: Circuit for the net convexity detector (pins numbered left to right as in the orientation in photo 5).

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Continued from page 13

along the entire back panel as well as the lower back corner of the mother board (5 VDC voltage regulators are on each circuit board). With two exceptions, everything went together easily, and exactly as presented in the assembly manual.

The first problem occurred when I attempted to install the self-retaining nuts in the side panels. For one thing, it can be very difficult to press these nuts into the very sturdy composition board unless they are gently tapped with a hammer. In addition, the part numbers for one of the nuts on the left side panel as illustrated in the assembly manual didn't correspond to the associated detail pictorial in the illustration booklet.

The only other problem I encountered during this stage of assembly was the installation of the side panels. Access to the side panel self-retaining nuts at the bottom rear corner of the chassis was obstructed by the previously installed screws and nuts that hold the rubber feet to the bottom of the chassis. My solution was to turn the chassis onto the side panel to be attached and insert and tighten the remaining screws to the appropriate panel.

The Mother Board

The mother board consists of two sections: a portion of the power supply, and ten rows of paired 25 pin plugs used later for connecting circuit boards and cables to the system bus. The installation of the plugs can be tedious. If you have not had much soldering experience, practice before you begin this board.

The most challenging part of the mother board assembly process is soldering some 500 pins which form the connectors for the individual boards of the system. The remainder of the board consists of a few capacitors, resistors, and diodes. There are, however, two instructions whose sequence should probably be reversed. Specifically, you are instructed to solder two electrolytic capacitors to the board and then secure each to the board with a self-locking cable tie. Reversing this sequence insures that no strain will be placed upon the soldered capacitor leads by the cable ties when they are tightened. The finished board is installed on the righthand side panel of the chassis after the twisted pair of 18 V leads from the power supply transformer are connected to the board. I had no trouble obtaining the proper resistance and power supply test readings outlined in the manual, and proceeded to the next step of assembly.

Front Panel Circuit Board

The H8 front panel control system has many features which make using the H8 a pleasure. One of these is the multifunction console keypad that provides users with direct, easy-to-use commands to operate the H8 without a terminal (see figure 1). Another feature is the 7 segment LED (light emitting diode) display system that displays a variety of system status information in an easy to read format not found on many larger 8 bit systems. We'll take a closer look at this unique system later, but first let's consider its assembly.

The entire assembly procedure is very straightforward. However, it is during the assembly of this board that a second rather tedious subassembly construction activity is encountered. In particular, it is necessary to prepare the cables that run from the board to the first row of plugs on the mother board and between the front panel and processor boards. The instructions and illustrations for this stage of construction are excellent and, if they are followed exactly, you should have no problems. The work performed on the cables is rather delicate, requiring the same amount of care and patience needed while assembling the mother board. One construction hint: you are instructed to mount four single element LEDs on the upper left side of the board. Make sure that each LED is mounted at exactly the same height as the others (0.25 inches from the board to the base of each LED). This can be easily accomplished by cutting a piece of 0.25 inch wire and using this as a spacer placed underneath each LED between the pairs of LED leads prior to soldering each to the board.

The Processor Board

Another feature of the H8 is the processor board, which comes preassembled. This is a real advantage because many of the problems that computer kit builders encounter are caused by mistakes made during assembly or installation of the processor board (see photo 2).

With assembly of the circuit boards and chassis complete, all that remains is to install the components. Of course, the H8 does not come with other boards that are necessary to have a functioning computer, such as extra memory and an

I/O (input/output) board. These are options the user purchases when buying an H8 (and most other computers, for that matter).

The Memory Board

If you want to use your H8 without external devices, the H8-1 memory board is the only other board you will need. The H8-1 is a 4 K byte programmable memory board which can be extended to a full 8 K by installing the optional H8-3 memory chip set. This board is easy to assemble, and not much more need be said about it — nothing, that is, except a short story about a mistake I made which also points to another nice feature of the H8.

Briefly, it happened like this: I was assembling the H8's circuit boards with extreme care, paying particular attention to the quality of the instructions and illustrations and making notes in my manuals I might want to use later. On the evening I started putting the memory board together, friends dropped over, and because the board looked so simple to put together, I decided to put part of it together while we relaxed and chatted. As a result of my divided attention, I installed a 14 pin IC socket in a 16 pin socket location.

One of my visitors was just beginning to get interested in computers (which was part of my reason for doing some of the assembly while company was around) and I showed her the partially completed board. She looked at it, asked a few questions, and then said, "What are those holes for by the end of that socket?"

I turned a bit red — I had blundered in the middle of a demonstration. Well, for the next 45 minutes we struggled to remove the socket, clean out the solder that was plugging the holes in the board and refit another socket. The H8 as well as its accessory kits come with sockets for all of the ICs including the 7 segment displays. If you ever need to replace an IC, you won't have to struggle with unsoldering it and cleaning off the board. And you won't have to pay extra for the socket sets when you buy the kits. The finished board is shown in photo 2.

The H8-5 SIO Board

If you want to connect your H8 to a console terminal or use the system software stored on cassette tape, you'll also want the H8-5 serial I/O and cassette interface board. It took quite a while to assemble because of its relatively high component density, but it presented no construction problems.

Testing and Alignment

After assembling the basic H8 system, you are instructed to perform three programmable test routines as well as an alignment of the cassette interface. The first test routine is a short program entered in machine code through the front panel keypad. The routine performs a general check of the H8 and at its end-of-run displays several messages on the front panel LEDs (ie: YOUR H8 . . . IS UP AND . . . RUNNING). If the test routine does not execute properly, the reader is directed to an extensive trouble-shooting flowchart that is ten pages in length and very clearly written. I had no trouble at this point and proceeded to the next test routine.

The second of the two routines is a memory test routine. It is also entered in machine code through the front panel keypad. The program performs a thorough test of every memory location on any 4 K or 8 K byte memory board by storing and retrieving consecutive octal values from 000 through 377 in every memory location. If an incorrect value is detected during a compare operation, the program halts, sounds an audio alert, and displays the expected (rather than observed) contents of the location where the test failed. The address where the test fails and the actual (or observed) contents of memory at that location can both be displayed on the LEDs by displaying the contents of the HL register pair and the accumulator, respectively. If no problems are encountered during execution of this routine, it will continue to repeat the test cycle until stopped by the user. Everything worked fine for me as I watched the memory content values go sailing by in the display.

The last task to be performed is the alignment of the cassette interface on the cassette I/O board. The procedure consists of setting the two variable resistors on the board to the correct positions as indicated by the readout on an on board single element LED test lamp. This LED also comes in handy later for troubleshooting the H8's circuitry. The adjustments were quite tricky to make, but after two tries and a number of test loads of software cassette tapes, it worked very well. Had it not worked, I could have referred to another trouble-shooting flowchart to locate the problems.

But everything did work. I proceeded to play around with the keypad commands, becoming familiar with what made my H8 "tick." Finally it was time to install the front panel cover and the louvered metal chassis cover. I connected the serial I/O cable to my H9 video terminal and was ready to do the final test routine for the serial I/O channel on the serial I/O board. It consists of setting up the USART (universal synchronous/asynchronous receive/transmit device) assigned to this channel and transmitting and receiving characters to and from the terminal. I was amazed at how easy it was to do I/O routines from the front panel. The final test was completed, so I left my system for awhile to return to the H8 operating manual and software manual set.

The Benton Harbor Bus

The Benton Harbor Bus represents a departure from the S-100 bus, which has become one of the "standards" of the microcomputer industry. The H8 system bus uses only 50 lines, compared with the 100 lines of the S-100. Since the S-100 was designed early in the history of the microcomputer industry, it incorporates bus lines which are no longer needed or which have been replaced by more recent system control hardware.

Manufacturing costs are kept down by not having to machine an edge connector tongue, not using gold plated edge connectors, and replacing the expensive 100 pin socketing system of the S-100 with much less expensive plug and socket sets which are assembled by the user.

Another feature found on the H8 is its convection cooling system. This system has been designed so that power supply voltage decreases slightly every time a circuit board is added to the mainframe. As more boards are added, the proportional amount of heat dissipation from each circuit board regulator also decreases. It is for this reason that you are instructed to "locate circuit boards in alternating positions for improving ventilation." When the time comes to add boards to the unoccupied alternating rows of plugs on the mother board, the effective heat dissipation will be low enough to position boards adjacent to one another. To improve upon this scheme, all circuit boards are installed on a slant to facilitate the convection cooling process. The end result is a quiet running machine which does not require the added cost of a fan to keep component temperatures down.

Costs are also kept down by the size of the H8's power supply. I saved a lot of money by not buying an 8 bit machine with a large power supply. The fact is that you pay dearly for every extra and often unused ampere that a power supply delivers. In this regard, the H8 delivers a full 10A, which is sufficient to operate all of the boards that the chassis can hold — up to seven in addition to the front panel and processor boards. It is also switch-selectable for operation on either 110 or 220 VAC, an advantage for European users. It also includes a switch for normal or low level line voltages, which may come in handy in case of a brownout — you'll need a separate generator for a blackout.

Split-Octal Notation

Before going on to discuss the firmware that coordinates many H8 operations, we should first describe the type of machine language code notation used by the H8. The H8 uses a number system called split octal, a modification of straight octal that is well suited to 8 bit computers like the H8. It is also well suited for the H8 display system, as you will see.

Split-octal notation is identical to octal notation except that the two most significant bits of each pair of data bytes are represented by one arabic numeral. In this scheme 377 is the highest value that can be represented by one 8 bit byte (ie: word) of data. Thus:

$$3\ 7\ 7 = \underbrace{1\ 1}_{3}\ \underbrace{1\ 1\ 1}_{7}\ \underbrace{1\ 1\ 1}_{7}.$$

And, the highest value that can be represented by two 8 bit bytes of data would be 377.377. The H8 defines 1 K bytes of memory as 003.377 bytes and 8 K bytes of memory as 037.377 bytes. The H8 is designed to reserve certain portions of memory for the system monitor and later system expansion as shown in the H8 memory map (see figure 2).

PAM-8, the Front Panel Monitor

The functions and features discussed above are tied together by another H8 feature — the front panel monitor — which resides in 1 K bytes of read only memory on the processor board. It also controls such activities as initializing the system during power-up, coordinating tape loads and dumps, communication with the Console Driver routine (part of every Heathkit software package), processing restart and clock interrupt vectors, and processing user defined interrupt requests.

H8 Software

Someone once said a computer system is no better than the software that comes with it. This is as true for large computers as it is for microcomputers. The H8 software packages are intended to function as an integrated system. They include TED-8, a line oriented text editor; HASL-8, a machine language assembler; BUG-8, a machine language debugger; and Benton Harbor BASIC, Heathkit's version of the popular interactive programming language created many years ago at Dartmouth College. Let's see what they're all about.

Common Elements

Each of these software packages contains a console driver routine that enables the H8 to communicate with a user's console terminal (Teletype, video display terminal, etc) and a cassette or paper tape transport. It occupies 355 decimal bytes of programmable memory in each software product from locations 040.100 through 041.144. Thus, all of the console driver routines are available to users for special purpose modifications as well as for use in user designed software which would benefit from using the same I/O routines, including I/O port assignment. It is responsible for processing console terminal interrupts, setting up and reading USART (universal synchronous-asynchronous receiver-transmitter) modes, commands and statuses, processing control characters (such as CTL-C, CTL-Q, and CTL-S), reading and writing single characters, and processing character strings in the 28 character type-ahead buffer. During interrupt processing, the console driver interacts with the PAM-8 system monitor. The entire listing of the console driver routine in assembly language is provided in an appendix to the software manuals. As in the case for the monitor, the console driver routine and all other software for the H8 were developed for Heath by Wintek. The Heath Company cannot (under contract with Wintek) provide any listings other than the partial listings presented in the software manuals, and "cannot provide consultation on user developed programs or modified versions of Heath software products." However, with a homebrew disassembler or memory dump routine and the partial listings provided, you might not have too much difficulty in generating your own unofficial versions of the source codes.

Another common element to all Heath software products is the software configuration procedure that must be performed before any software distribution tape is loaded into the H8. The procedure provides opportunities for the user to adapt each software package to his or her own needs. A list of program configuration parameters is presented to the user, who can then define items such as BKSP, which allows the user to define which key will be used to control the backspace function, HIGH MEMORY, which allows the user to specify that section of high memory that he or she does not want used by the system program, and LOWER CASE, which allows the user to select either upper and lower case or upper case only I/O to the terminal.

A third element common to all Heath software products is command completion. The feature allows the user to enter the first letter(s) of a program command, whereupon the software routine, in conjunction with the console driver, will print out the remainder of the command. For example, a text editor allows the PRINT command to be evoked by typing P, and the system responds with RINT, completing the command. The problem is that, if one is a fast

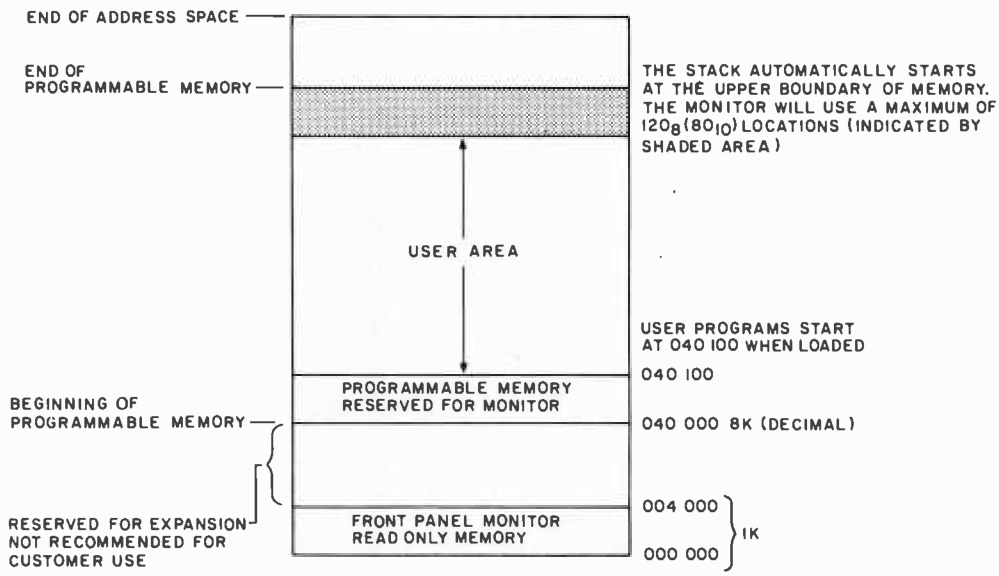
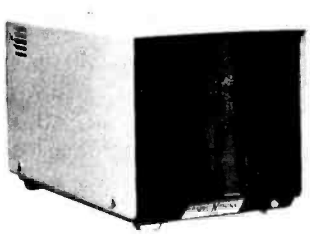


Figure 2: The H8 memory map.



typist or has used computer terminals before, one tends to enter too many beginning characters and thereby cause an error. For example, I still haven't gotten used to typing just P to evoke the print command. So what happens? I type out the entire command, PRINT, and the result is PRINT RINT. The problem is even more bothersome because the command completion for some of the same commands is different for different software. Using the text editor (the above example), typing just P evokes the RINT completion; using BASIC, a PR evokes the INT completion.

TED-8, the Heath Text Editor

A text editor turns the user's terminal into a typewriter of sorts with the added capability to store what is typed into memory, and to edit the contents once stored. It is essential for writing assembly language programs and for preparing various kinds of texts, such as newsletters and reports, for personal use.

TED-8 is a line oriented text editor that occupies approximately 4.3 K of user memory. It has commands for loading and dumping both files and individual records, searching for character strings, clearing the text buffer, replacing and deleting lines, specifying range statements which control the number of lines upon which commands will operate, creating new text, and editing existing text in the buffer. It also includes a TAB command to facilitate the writing of assembly language programs, a wide variety of range commands, and a USE command that provides the user with a current number-of-lines count and memory usage information.

In my opinion, TED-8 is a reasonably good small system text editor with considerable flexibility. It is, however, somewhat inconvenient to use, especially when one needs to edit a particular line but does not know the exact line number and must therefore either count the lines (an inconvenience if there's a lot of text to cover) or write and execute an often lengthy expression to specify the character string in the line that is to be edited. Some of this could have been avoided if a line numbering system had been included, which could be stripped off at the end of editing.

Another problem is that the text editor and assembler are interdependent in some situations but must each be loaded separately into memory. This makes repeated editing and execution for program testing a real chore. I would have liked to see these programs (TED-8 and HASL-8) put together as one package, or have been provided with a dedicated linking loader as part of the

PAM-8 monitor that would enable me to load both programs into memory. Aside from these two disappointments, I am pleased with the general capabilities of TED-8. For the small amount of memory it occupies, it is relatively powerful.

HASL-8, the Heath Assembly Language

HASL-8 is a 2 pass assembler which effectively means that you must load (playback) your source program (created by TED-8) twice before the assembly of the source program can be executed. (You can see how often you may have to load and unload, rewind and playback cassette tapes if you are editing and testing even a moderately sized assembly language program.) The output of HASL-8 is object code which is the machine language for the computer. In addition, a source listing of your program is generated, which includes not only the text of your original program but also the addresses which correspond to specific assembly language and machine language instructions (op codes). The Heath assembly language resides in slightly less than 8 K bytes of user memory and supports a complete set of operators, tokens, and pseudo opcodes (assembler directives), including in the latter a large set of pseudo ops for error detection and control of listings.

When a configured version of HASL-8 is started, the user must first answer a series of questions regarding the desired page size, interpage gap size, listing port, whether or not to produce a binary image of the source program in memory, and whether or not to save a binary image on tape. The program then requests input of the source program from tape, makes a second pass after the tape is rewound, assembles the object program, and dumps out a listing at the console terminal. The listing includes single character error codes in the far lefthand margin, and run summary data at the end of the listing (number of statements listed, remaining free bytes in user memory, and the number of errors detected). HASL-8 does not process macros or provide a cross-reference listing of user labels and associated addresses, both of which would be a nice improvement in a subsequent version. It is a fairly average assembler for its size, but should be adequate for most general purpose assembly language programming. Its documentation is very good, as is the documentation for all of the software products from Heath.

BUG-8, the Heath Console Debugger

BUG-8 is one of the best software packages that comes with the H8. Residing in any

3 K bytes of memory, it provides the user with powerful tools for writing, editing and debugging machine language programs from a console terminal in octal, decimal or ASCII format. It interacts with the PAM-8 monitor and uses many of the PAM-8 routines. With BUG-8 running as a full console monitor, you can do any of the following:

- examine the contents of any memory locations;
- change the contents of memory locations;
- examine the contents of any processor register;
- change the contents of any processor register;
- start program execution;
- perform single step execution of a program;
- set program breakpoints;
- clear program breakpoints;
- load and dump programs from OR to tape.

The command format used in BUG-8 is short, which makes using BUG-8 a real pleasure (the same kind of feature would be very desirable as a configuration option for TED-8).

Benton Harbor BASIC and Extended BASIC

When you purchase an H8 kit, you are supplied with Heath's 8 K byte, Benton Harbor BASIC. In addition, Heath has also marketed two versions of Extended BASIC (versions 10.01.02 and 10.02.01) which provide the user with functions for string manipulation and a number of other useful features. Version 10.02.01 of Extended BASIC also enables the user to load and dump variables, program text, and both text and variables. This latest version is a significant improvement over the earlier version of Extended BASIC in that it allows the user to pass variables from one program to the next.

There has been quite a bit of discussion about the relative execution speed of various versions and brands of BASIC that are on the market. However, the benchmark tests for Heath BASICs that have appeared in the small systems literature have been performed only under somewhat restricted circumstances. In particular, the H8 real time clock was not enabled when Extended BASIC benchmark tests were published, which by omission and implication exaggerates the speed of the 8 K byte version of BASIC. Now, speed isn't the only criterion in evaluating a higher level language's performance, but to provide you with a more balanced perspective on this issue, I give you the following benchmark comparisons between the two versions of Extended BASIC and the 8 K BASIC that comes with the kit.

A modified benchmark algorithm developed by J G Letwin (a software engineer for Heath) was used to conduct all of the tests. All timings were accomplished using the H8 real time clock via the POKE and PEEK commands. Table 1 presents the comparative data for execution time of various functions in milliseconds. The real time clock was enabled for all tests. The algorithm I used is as follows:

```
110 B=1.1:C=1.5 (numeric constants)
120 POKE 8219,0:POKE 8220,0 (set clock = 0)
130 FOR I=1 TO 2000 (2000 iterations)
140 (line for each test function)
150 NEXT I
160 Y=PEEK (8219)+(PEEK (8220)*256)
    (read run time)
170 X=(correction factor for "A=B")
180 T=((Y/500-X)/2000 (time in ms)
190 PRINT "T= ";T,"Y=";Y (output)
32767 END
```

The argument at line 180 computes the time for execution of one operation of the function supplied at line 140 by dividing total time in milliseconds (Y) by 500, subtracting the time for the identity statement A=B, and then dividing by the total number of iterations (2000). Line 140 contains the function being benchmarked across each version of BASIC (for example, 140 A=SIN(B), 140 A=SQR(B)). The POKE and PEEK commands are placed immediately before and after the test routine to be timed, respectively, thus holding any time required to execute these commands constant and to a minimum.

Table 1: Comparison of execution times for three Heath BASICs for various common functions, operators, and the FOR/NEXT statement. All times are in milliseconds, with the real time clock enabled.

FUNCTION/ OPERATOR/ STATEMENT	8 K BASIC (Version 05.01.00)	Extended BASIC (Version 10.01.02)	Extended BASIC (Version 10.02.01)
A=B	14.9	15.7	15.8
ABS	1.2	1.2	1.2
+	1.9	2.7	2.5
–	2.2	3.0	2.7
INT	2.3	2.0	2.0
RND	2.4	2.4	2.4
PEEK	3.5	3.3	3.2
*	4.3	3.3	3.1
/	5.2	5.9	5.7
FOR/NEXT	5.4	5.5	5.5
POKE	14.5	13.8	13.7
COS	18.3	15.0	14.6
SIN	19.3	15.7	15.3
EXP	22.1	17.3	17.0
LOG	27.2	21.8	22.0
ATN	29.2	24.9	24.3
SQR	47.8	15.7	15.3

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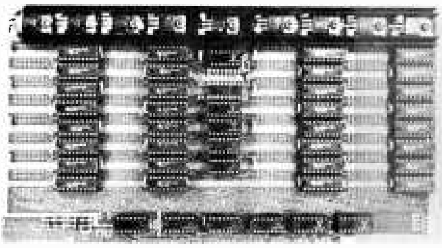

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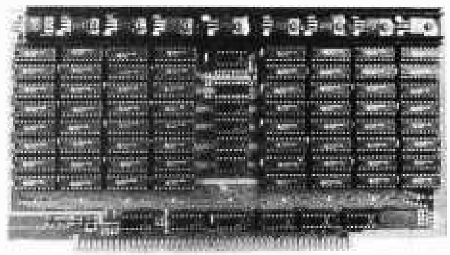

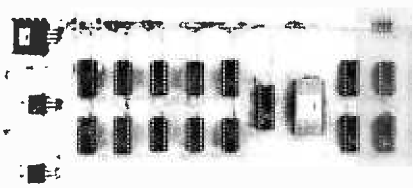

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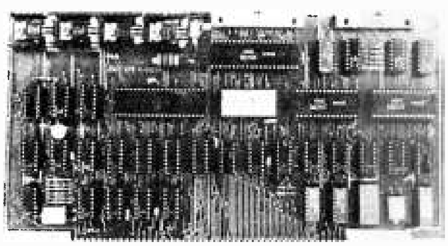

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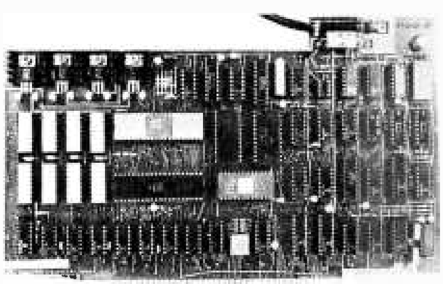

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What can we glean from all these timings? For one thing, the 8 K basic BASIC is generally slower than either of the Extended BASICs. The differences in execution times between the three versions is not really significant for the arithmetic functions. On the other hand, the transcendental functions run faster in Extended BASIC. The differences between the versions are most evident when the SQR function timings are compared. It appears that for arithmetic applications, such as those used in most financial accounting, the user can get by very well without using Extended versions. On the other hand, those who plan to do engineering or scientific applications software development should give serious consideration to using only the Extended versions. All of the versions will operate approximately 10 to 15 percent faster if the real time clock is disabled, which might be a further incentive for the scientific programmer to use only the latest version (10.02.01) of Extended BASIC.

Aside from timing benchmarks, there are many other criteria to consider when reviewing a higher level language like BASIC. Since I cannot possibly cover all of them in this article, I'll select the ones which are probably of most interest to many readers. Let's start with the command and function types of the three versions.

8 K Benton Harbor BASIC contains most of the commands and functions found in many commercial brands of BASIC for small systems. It has a set of editing facilities, immediate and program command modes, and a full set of relational operators. It also has additional commands, including PEEK, POKE, SEG (for controlling the H8 LED displays), PAD (for utilizing the H8 control keypad while running BASIC), and several commands for loading and dumping programs. Most 8 K BASIC functions can use variables in addition to constants within their arguments, which makes programming more flexible. This version of BASIC does not provide functions for manipulating string variables.

In contrast to 8 K BASIC, both versions of Extended BASIC have a variety of functions for handling string variables. In addition, such commands as BUILD, DELETE, LINE INPUT and CONTROL make program development easier. Each version makes use of the FREE command, which prints out memory allocation data for the user. The latest version of Extended BASIC also includes commands for differentiated loading and dumping of program text and variable as well as LOCK/UNLOCK commands for file protection. Both versions display the type of data being loaded or dumped on the H8 front panel LED displays. As the data in table 1 indicates, the latest version is quite fast. Additional refinements, such as incorporating PRINT USING, OCTS and DECS (for octal to decimal, and decimal to octal conversion), and file handling commands that could be executed in program mode (such as PUT and GET), would have been useful. In addition, a special INPUT command that suppresses the carriage return/line feed would also have been useful formatting the terminal display during INPUT, as would a more flexible RUN command to specify a file/program name for storing and executing one of several programs stored in user memory. This can be accomplished now using a combination of the GOTO and CONTINUE commands. However, this procedure prevents the use of identical variable names in different programs unless such variables are reinitialized before each execution, or the variable values of a previously executed program are to be used as *global* variables in subsequent programs in memory.

A Few Pointers

The following section includes some suggestions about using the real time clock for program run timing, displaying output using user defined patterns or character messages on the LEDs, and using the audio feedback system for any number of interesting projects. By combining and augmenting some of the following techniques, you can use your H8 as a daytime clock, alarm clock, device controller timer, and even a (rather crude) music synthesizer.

Among the applications software packages available from Heath for the H8 are a Space War program and a set of games programs. The Space War game, which requires 24 K bytes of memory is a sophisticated version of Star Trek. It has excellent displays, a full range of commands, and some surprises for those of you who dream of cruising the galaxy. Finally, the games set, which comes on one cassette tape, contains a variety of interesting games, including Craps, Nim, Hexapawn, Tic Tac Toe, Orbit, Hamrabi, and Derby, all stored in machine language and executable without first loading the BASIC interpreter into memory.

In addition to the above applications software, the Heath Company is also planning to market some business software in the not too distant future. This source of applications programs will be supplemented by the software that will become available from the Heath user's group (HUG), which is presently reviewing and cataloging hundreds of programs that are being donated to HUG by users. Software from HUG will be available to HUG members at a nominal cost and will be announced in the HUG magazine *REMark* as contributed programs become available.

The H8 Real Time Clock

Every 2 ms the H8 generates a level 1 interrupt which is then used to service the front panel and update the real time clock. The clock or "tick counter" is located in two bytes of user memory at locations 040.034 and 040.033 and is called TICCNT. Both the high order byte (040.034) and low order byte (040.033) of the counter can be displayed on the H8 LEDs using the following short assembly language program which can be executed in memory with the assembler (HASL-8) resident:

```
074.000                    ORG  074000A
074.000 041 033 040        LIX  H,040033A
                           LOW ORDER BYTE
074.003 116 DISPLAY        MOV  C,M
                           LOAD LOW BYTE
074.004 054                INR  L
                           NEXT BYTE
074.005 106                MOV  B,M
                           LOAD HIGH BYTE
074.006 055                DCR  L
                           RETURN POINTER
074.007 303 003 074        JMP DISPLAY
                           NEXT BYTES
074.012                    END  074000A
```

Be sure to set the front panel to display the BC register pair before running the program.

The BASIC timings described earlier accessed the TICCNT memory locations by using the PEEK function and POKE command. Using these commands, it is possible to create a program run timer for programs that run up to approximately two minutes. Unfortunately, after this time TICCNT will start all over again instead of continuing to increment third and fourth memory locations, which would have provided a very convenient built-in extended range timer. You will need to allocate additional bytes in memory for a higher order counter in order to extend the clock range.

H8 Display Control

As discussed earlier, the H8's front panel is an integral part of the entire system and can be used for many operations even while using a console terminal. One of the advantages of this design is that the LED display can be accessed and controlled by the user either through the front panel or through a program being run from a terminal. Much of this is made possible by accessing the monitor control cells and flags stored in memory.

As an example, the assembly language program in listing 1 provides you with complete control of the display updating. First the display update control bit in the user definable memory flag .MFLAG is set to 002 to disable display update. The displays are then loaded with the desired bit pattern, in this case the pattern "XrunningX" (where X = blank). The user accessible memory cells for each LED bit pattern are in memory locations 040.013 through 040.023. The temporary bytes for storing the pattern for this display are in locations 071.000 through 071.010. Each byte in the temporary area is, in progression, loaded into the corresponding byte in the monitor LED memory bytes. To modify the display, change the bit patterns in the temporary area. Add additional temporary bit pattern tables and a table reference and transfer routine to display more than one front panel message.

The H8 Horn

The audio feedback system that is part of the H8 has other practical uses. The audio tone can be turned on from a running program that stores the octal value 160 in the front panel hardware control cell CTLFLG located at 040.011. If an attempt is made to do this from the front panel without going through a program, the front panel will be disabled before the operation is completed. The tone can be turned off by restoring CTLFLG to its normal octal value of 360.

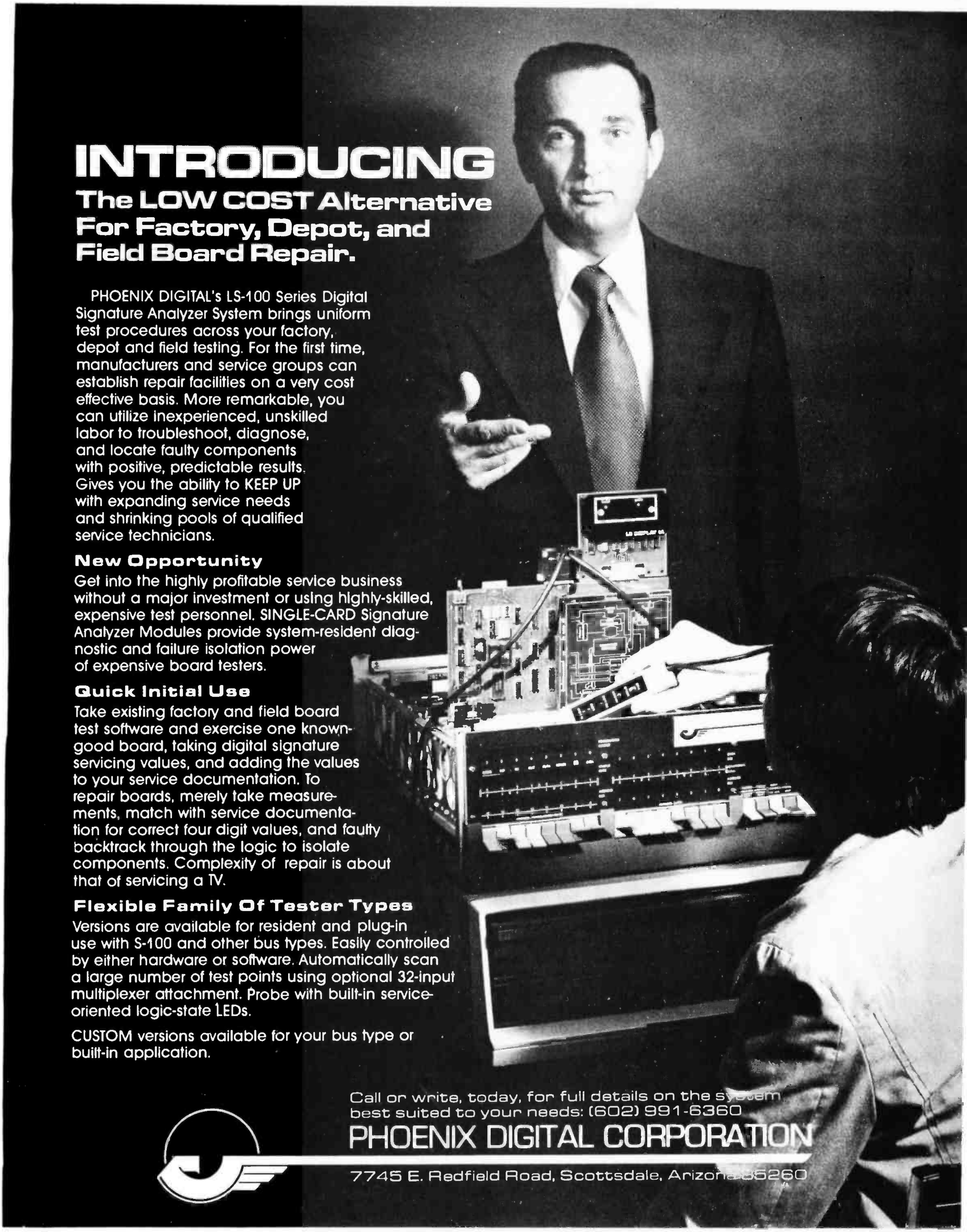
Here is an interesting BASIC routine to generate an audio beep sequence with timing that follows a sine curve. Change the value of X to vary the timing curve. (Note: line number 3 is written in multiple statement form to structure the program to run as fast as possible.)

```
1  X=1
2  A=8201: B=120: C=208: D=20
3  J=J+X: POKE A,B: POKE A,C:
   FOR I=X TO SIN(J)*D+D: NEXTI: GOTO 3
4  END
```

Split-Octal to Decimal Conversion

It is often useful to be able to quickly convert split octal bytes to their decimal equivalents. The following routine does this. It can be located as a temporary program in BASIC while other programs are being developed or executed. Be sure to use line numbers that do not conflict with those in the program you are using. (Note: input N if done.)

```
010   REM OCTAL TO DECIMAL CONVERSION
020   PRINT: INPUT "A=?";N
```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```
071.000                          ORG   071000A
071.000  377                     DB    377A       LED PATTERN 1
071.001  235                     DB    235A       LED PATTERN 2
071.002  203                     DB    203A       LED PATTERN 3
071.003  221                     DB    221A       LED PATTERN 4
071.004  221                     DB    221A       LED PATTERN 5
071.005  363                     DB    363A       LED PATTERN 6
071.006  221                     DB    221A       LED PATTERN 7
071.007  240                     DB    240A       LED PATTERN 8
071.010  377                     DB    377A       LED PATTERN 9
                         *
                         *
071.011  041 010 040             LXI   H,040010A  POINTER TO .MFLAG
071.014  076 002                 MVI   A,002A     (A)=OFF CONSTANT
071.016  167                     MOV   M,A        DISABLE LED UPDATE
071.017  041 000 071 DISPLAY     LXI   H,071000A  PATTERN TBL POINTER
071.022  021 013 040             LXI   D,040013A  LED TABLE POINTER
071.025  176         LOADIT      MOV   A,M        (A)=BIT PATTERN
071.026  353                     XCHG             (H)=LEDPT, (D)=DISPT
071.027  167                     MOV   M,A        DISPLAY IT
071.030  353                     XCHG             (H)=DISPT, (D)=LEDPT
071.031  043                     INX   H          NEXT PATTERN BYTE
071.032  023                     INX   D          NEXT LED
071.033  067                     STC              SET CARRY=1
071.034  077                     CMC              SET CARRY=0
071.035  076 024                 MVI   A,024A     (A)=COMPARE CONSTANT
071.037  273                     CMP   E          (A)<(E)
071.040  322 025 071             JNC   LOADIT     NEXT PATTERN/LED
071.043  303 011 071             JMP   DISPLAY    REINITIALIZE
071.046                          END   071011A
```

Listing 1: An 8080 assembly language program to allow the user to control the LED (light emitting diode) readouts on the front panel of the H8 computer.

```
030   IF N > 377 GOTO 100
040   IF N=0 GOTO 110
050   A=INT(N/100): IF A >3 GOTO 90
060   B=INT ((N/10)-(A*10)). IF B > 7 GOTO 100
070   C=N-((A*100)+(B*10)): IF C > 7 GOTO 100
080   Q=C+(8*((8*A)+B))
090   PRINT: PRINT "A=";N;"D=";Q: GOTO 20
100   PRINT: PRINT "ERROR! USE ONE
      SPLIT-OCTAL INPUT BYTE!"
110   GOTO 20
120   END
```

Heath Support Services

Regarding the servicing of digital systems like the H8, Heath's present approach is to do most repairs at regional centers or at the factory in Benton Harbor MI until such time as each local store can either provide additional in service training for existing technicians or add on additional technical staff. Some stores that are not regional centers, such as the Heathkit Electronic Center in Peabody MA, have service technicians who are capable of performing most of the necessary digital equipment repair jobs. All Heath products are warranted for a 90 day period from date of delivery. If replacement parts are needed, some parts can be obtained through local stores; the remainder must be ordered from the factory. I have used the replacement parts service and found it to be most adequate.

Another area of support services is the Heath Users Group (HUG). Owners of Heath computers can pay a yearly membership fee to join HUG which is administered in St Joseph MI. HUG supplies users with a variety of services including contributed software, membership information, and newsletters. HUG is an important component of the overall services provided by Heath and is growing rapidly. HUG members who are interested in forming local or regional users groups should feel free to contact HUG manager Robert Furtaw for additional information and assistance.

A third area of support services is new system products. The design of the H8 lends itself to upgrading and expansion in many ways, which Heath is already taking advantage of. I have also heard they're considering a number of designs for interfacing the H8 to their excellent line of ham radio gear, which should be of considerable interest to ham operators who are also interested in RTTY (radio teletypewriter). Likewise, I wouldn't be surprised if Heath introduces sophisticated video game boards to interface to their television sets, and household controllers to interface with some of their home oriented equipment.

Final Thoughts

Aside from these items, the possibilities are many. Digital to analog/analog to digital converters, video drivers, speech recognition systems, EROM (erasable read only memory) boards, upgraded firmware monitors, firmware versions of existing and future software, printers, modems, intruder entry detection devices, graphics boards, and perhaps even bubble or CCD (charge coupled device) memory boards are just a few of the many possible products that Heath might market.■

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A Stepping Motor Primer

Part 2: Interfacing and Other Considerations

Paul Giacomo
51 Farmington Chase
Farmington CT 06032

Interface Circuitry

Part 1 of this article ("A Stepping Motor Primer," February 1979 BYTE, page 90) described the theory of operation of the stepping motor. Part 2 concludes the discussion with a description of how to interface stepping motors to microcomputers. The interface can be accomplished in several different ways. The most common methods are to either decode the control sequence in software, outputting it to a parallel port with buffers and connecting the output of the buffers to the drive transistors, or use the output ports of the computer to feed into an external decoder that will sequence the drive. Since personal preference and individual application dictate how much or how little of this will be in the program, I will first describe a hardware version for a 4-phase, full-step drive, then describe how to transfer it to software.

Let us assume that two control lines from an input/output (IO) port are used to control the stepper. One line is for direction and the other is for a step command. The program can then control the speed of the motor by controlling the frequency of pulses on the control line. Figure 17 shows a simple interface circuit. The control lines coming from an output port are buffered and sent over a cable to this circuit, which is in close proximity to the motor. (Avoid high voltage and current spikes near the processor.) The first thing to be done is to clean up the signals and then feed them into an up-down counter. The counter determines in which of the four excitation stages the motor is to be. The outputs of the counter are fed into a decoder section that activates the driver transistors at the correct time.

There is a 16 pin integrated circuit available (SAA 1027) through North American Philips Corporation that can do all of this, as well as including the drive transistors, for under $10. The program needed for the system is now fairly simple. What must be done is to select the direction of travel and then pulse the step line the correct number of pulses at the desired stepping speed. *Ramping* the speed of the motor is discussed in the following section.

The software version of this system would use four lines of parallel port interfacing directly with the drive transistors, with the excitation sequence stored in the program. To advance the motor, the program either increments to the next sequence pattern and outputs it for forward, or decrements the pattern and outputs it for reverse. Again, the speed of the motor is determined by how fast the patterns are outputted.

Although not covered in this article, there are drives available that allow one to input to the drive the number of steps to travel and then activate the go line. The drive automatically ramps the motor up in speed and then stops at the number of steps set beforehand. These drives are known as preset indexers. Another type of drive uses a voltage level to control an oscillator for the stepping speed.

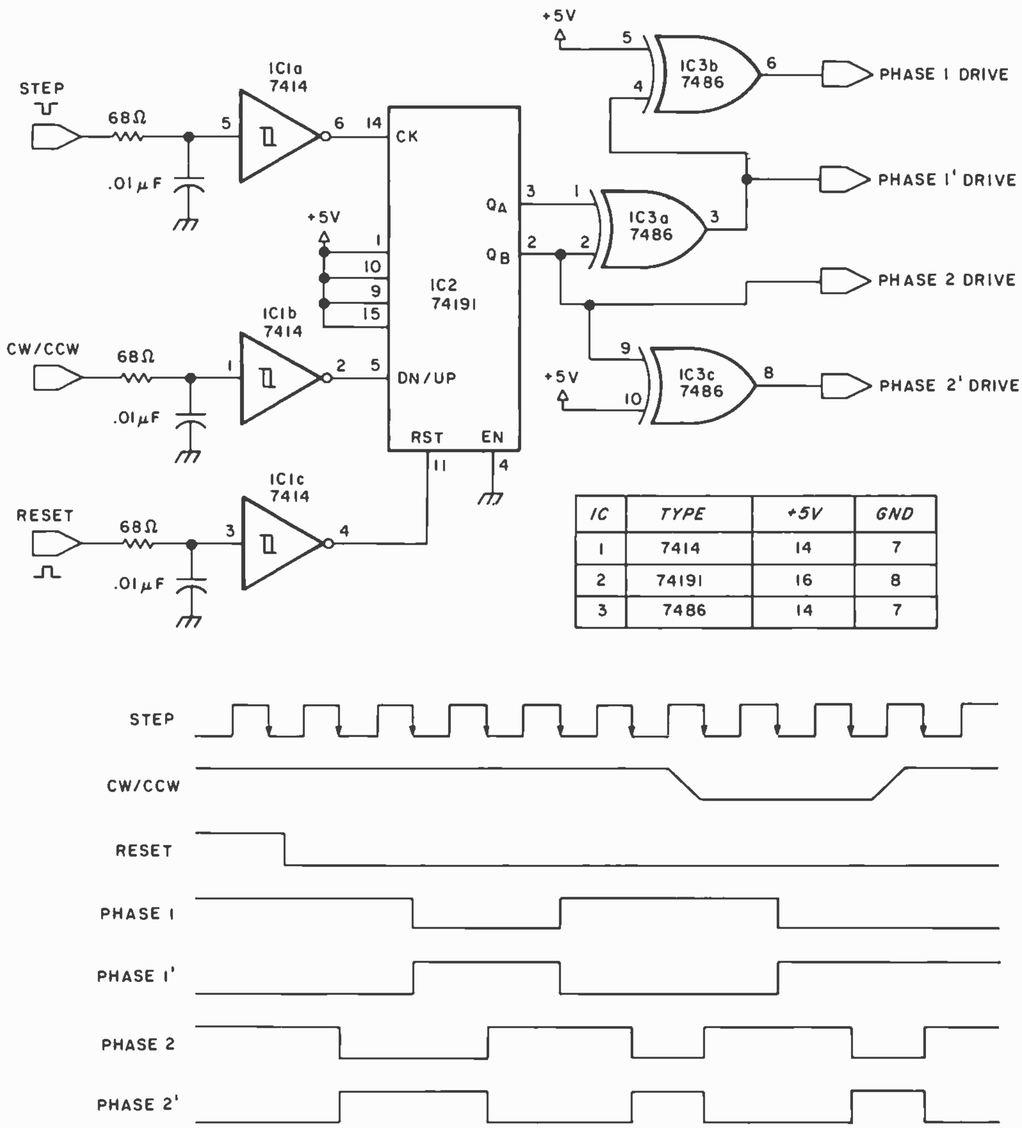
Behavior of Motors in Operation

Like any other motor, the stepper cannot instantly start and stop at full speed and maximum load and still be expected to end at the correct position.

When a motor takes a step, it behaves in a manner similar to that of a fiberglass pole with a weight on one end, as shown in

Note:

The figure numbering sequences used in this installment continues the sequence begun in part 1. Also, part 1 includes a glossary of terms and a reference list.



IC	TYPE	+5V	GND
1	7414	14	7
2	74191	16	8
3	7486	14	7

Figure 17: Hardware version of step sequence generation for a 4 phase full stepping motor.

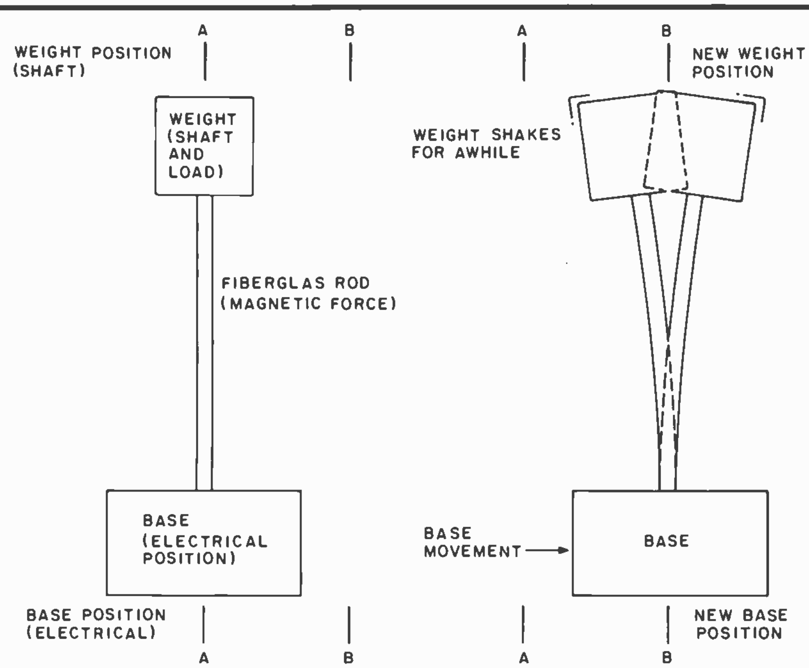


Figure 18: Analogy to single step movement in a stepping motor. When the base (electrical position) is suddenly moved to a new position, the fiberglass rod (magnetic force) pulls the suspended weight (shaft and load) along with the base. Because the fiberglass rod is flexible, the weight causes it to shake for a while before stopping. The inertia of the shaft and load in the stepping motor's case is the mass that makes the weight oscillate for a time.

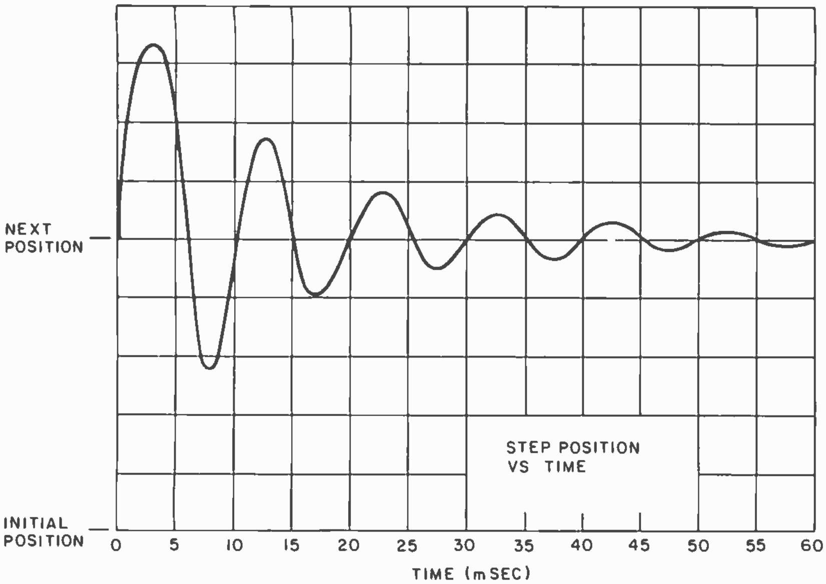


Figure 19: Step position versus time for a typical stepping motor. The actual frequency of oscillations and time to decay is different for every motor and load combination.

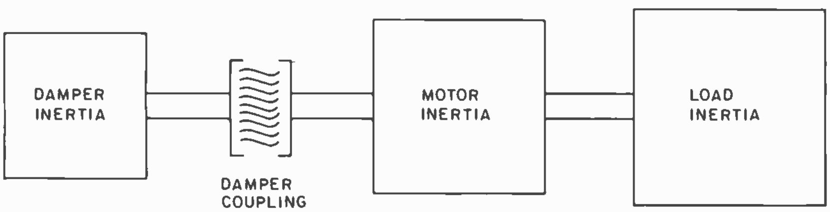


Figure 20: Simplified diagram of inertial damping used to reduce overshoot of a motor.

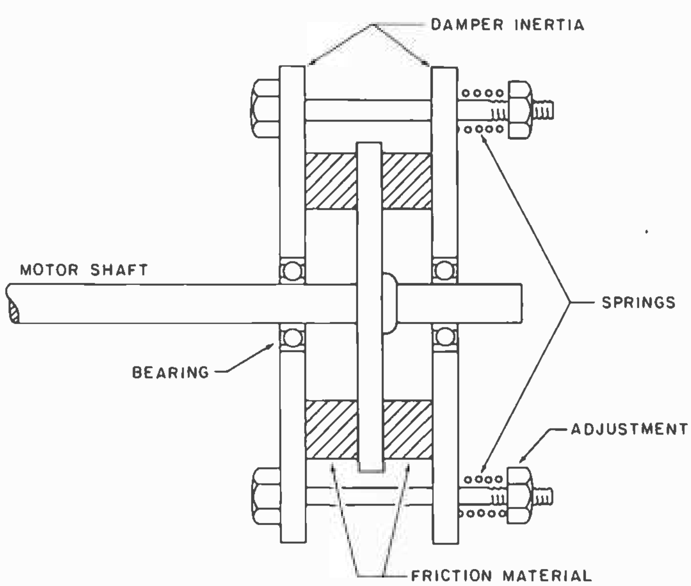


Figure 21: Example of a friction coupled inertia damper.

figure 18. When the electrical position is advanced one step, the magnetic force tries to pull the shaft and load to the next mechanical position. Depending on the drive, inertia of the load, and friction on the load, the shaft will bounce back and forth (oscillate) around the next mechanical position (like the weight on the end of the fiberglass pole) until it has dissipated its energy. Figure 19 is a graph showing position versus time for one step of a motor. This overshoot of the shaft may not be a problem in a low inertia, high friction system, but can cause troubles in a high inertia system with low friction.

To reduce the overshoot some form of damping must be added, the easiest being friction damping. This consists of adding friction to the motor shaft, which opposes any kind of motion and provides energy dissipation during oscillation. Although this method is easy and inexpensive, it reduces the available torque from the motor. This also affects the performance and the final position accuracy of the system.

Another type of damping is known as inertia damping (sometimes referred to as *Lanchester* damping), which is the most commonly used method for mechanical damping. A simplified diagram of this type is shown in figure 20. This type of damper is constructed with a coupling that is somewhat loose and slips like an automobile clutch that is not fully engaged. The coupling will try to bring the damper inertia to the same speed as the motor shaft. When the speeds are equal, there is no friction between the damper and motor, so the damper is inactive. This type of damper does not affect the final position accuracy but reduces the acceleration and deceleration rate of the system. These dampers are much more expensive than the simple friction damper. The inertia of the damper (which is related to the size and weight) has the largest effect on the amount of damping, and must be selected for the particular application.

Two common ways that coupling can be made are by friction or by using a viscous fluid similar to oil. Figures 21 and 22 give examples of friction and viscous coupling dampers, respectively. The friction damper has a disk attached to the shaft and two other disks, or bearings, that are free to rotate on the shaft. By adjusting the springs, the amount of friction between the free disks and the mounted disk can be changed. The viscous damper consists of a cylindrical case attached to the motor shaft with another cylinder that is free to rotate inside the case. Fluid inserted between the two

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cylinders acts as the coupling. By changing the viscosity of the fluid, the amount of damping can be adjusted.

Another damping method uses the control circuit to electronically damp the mechanical oscillations. This is accomplished by giving the motor a quick reverse, then forward pulse, just as it were about to stop at the final position. Although inexpensive, it requires tuning of the pulses to the load, and the motor will be sensitive to fluctuations in load and friction. For this reason, this type of damping is not suggested for most personal computing applications.

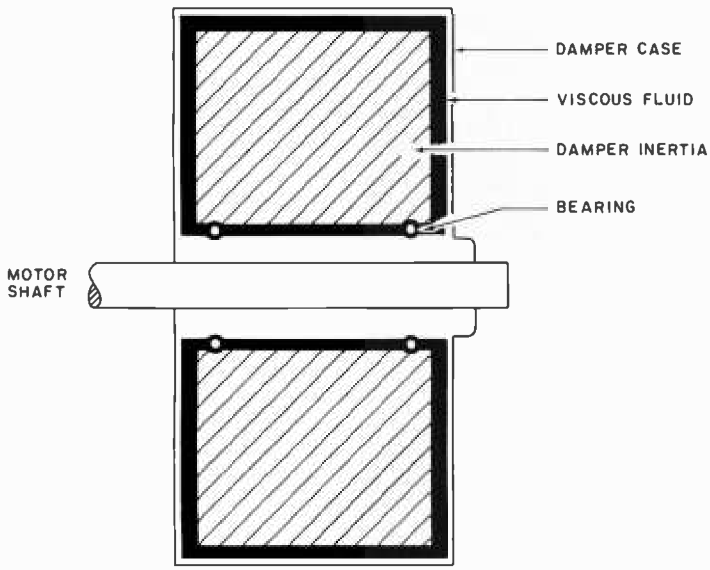

Figure 22: Example of a viscous fluid coupled inertia damper.

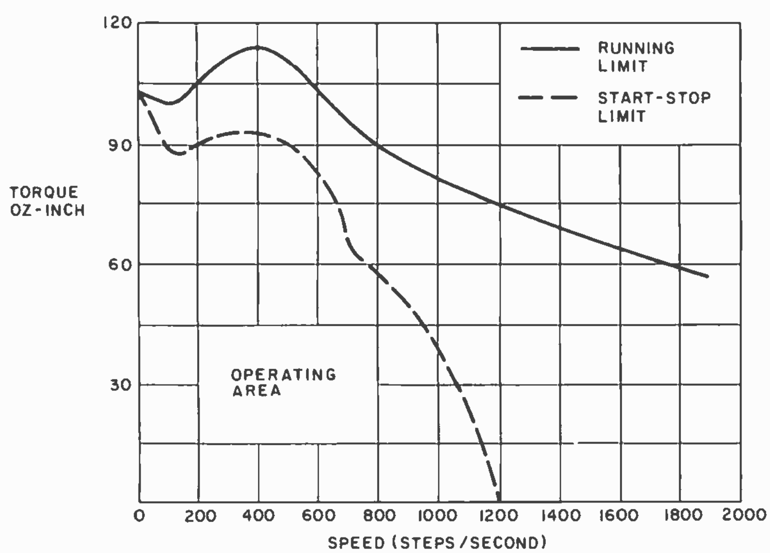

Figure 23: Typical speed versus torque curve for a medium power stepping motor. The solid line represents the maximum speed-torque combination that the particular motor and drive combination is capable of producing. The dotted curve shows the maximum speed-torque combinations that can be achieved and still start and stop without gradual acceleration or deceleration.

Since the motor cannot normally start and stop at high speeds, some form of acceleration and deceleration must be used. This quickly becomes obvious if the inertia is too large for the initial speed attempted. The motor will make noise and the computer will sequence through the steps, but the motor will not run. Fortunately, this will not harm the motor. To correct this situation, provided that the motor and drive combination is capable of that speed, the motor must start at a speed low enough to turn the shaft and then gradually accelerate to the desired speed. If the acceleration is too fast, the motor will lose synchronism and stop running. To stop the motor, it should be decelerated or it will continue to turn even after the pulses have stopped. As a rule, the deceleration rate can be faster than the acceleration rate.

An operating parameter exhibited by all stepping motors that should be noted is resonance. Every motor has a particular speed at which it has difficulty running. This is called its primary resonance, and it is usually located somewhere between 50 and 150 steps per second. An unloaded motor, when run at its resonance, will have very little torque and may sputter, make noise, stop turning or run backwards. This will not hurt the motor, but it will make the system do a lot of strange things.

To lessen the effects of resonance, a number of things may be done. More friction could be provided by damping, or the drive could be made to deliver less power. The best solution, however, would simply be not to run at that particular speed. When ramping up or down in speed, acceleration through resonance is possible as long as it is only for a few pulses.

The characteristics mentioned above can be found for every motor by examining the motor's speed versus torque curve. Figure 23 shows a typical curve. One point to remember about the graphs is that the curve represents a particular motor with a particular drive, so it is only a rough approximation for a motor with a personally designed drive. The bottom of the graph usually represents the speed of the rotor in steps per second. The side scale shows the torque that the motor can produce. The curve usually shows the maximum torque that can be applied and still start and stop without error. Notice the sag in the curves at low speed. This is where the resonance is located. Under certain conditions, the sag can be very sharp, going down to almost no torque and then back up to several hundred ounce-inches of torque in only 20 to 30 steps per second.

It should be kept in mind that if there is less current in the main drive than what is

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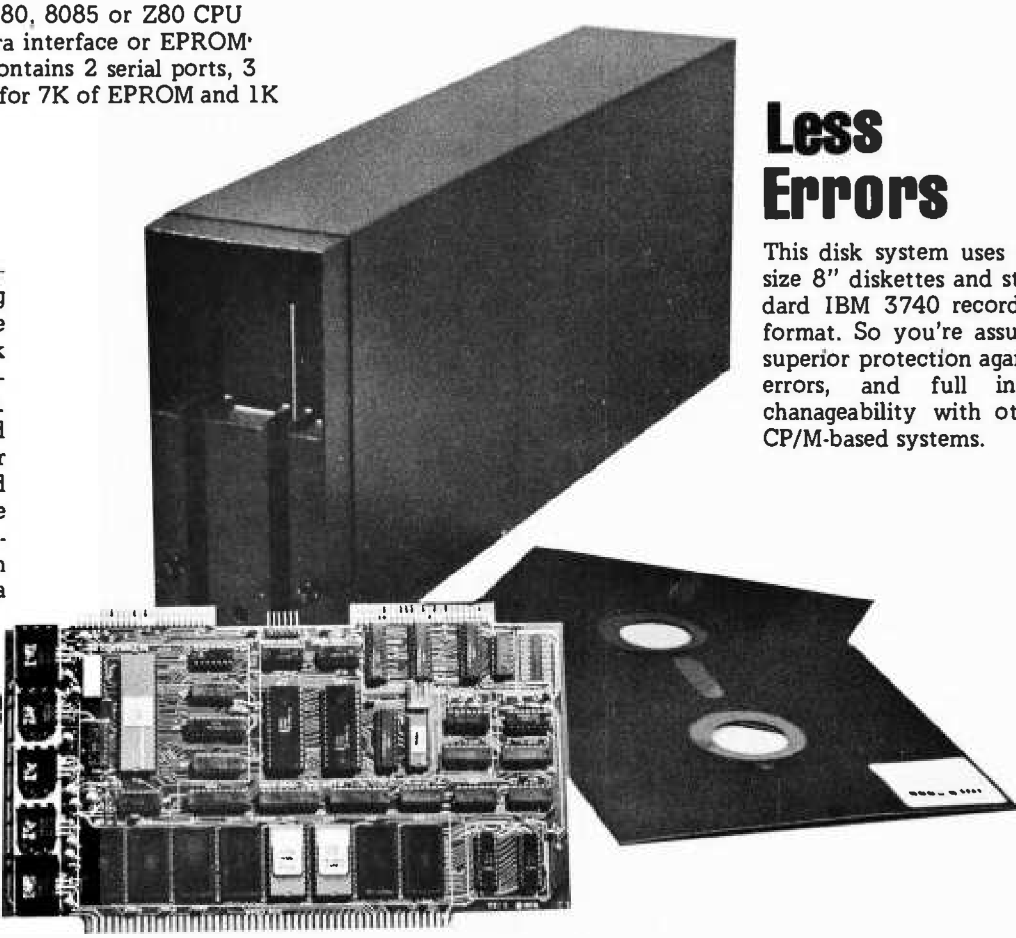

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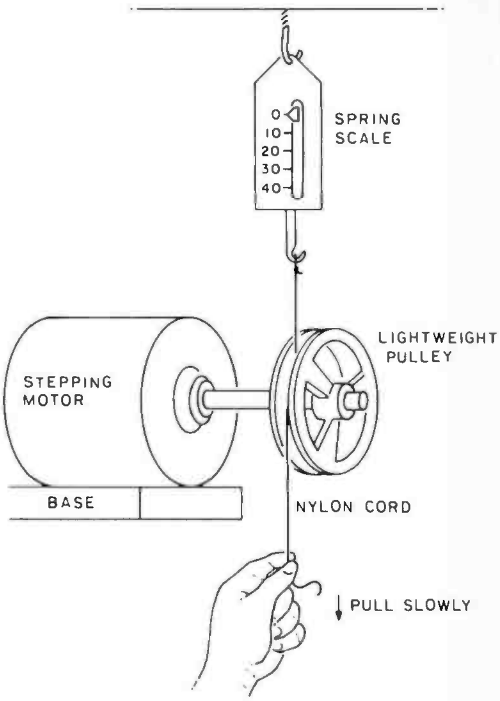

Figure 24: Spring scale torque measurement. The torque of a stepping motor at a set speed is measured by pulling slowly on the nylon cord wrapped around the pulley until the motor stalls. The reading on the scale times the pulley radius gives the maximum load torque the motor can run with at that speed. The amount of turns around the pulley varies with the pulley and cord. For a 3/32 inch (0.25 cm) diameter cord and aluminum pulley, two or three turns works best. By measuring the torque at several speeds, it is possible to make a special torque curve for the motor and drive.

The following list contains various sources from which stepping motors and pertinent literature may be obtained.

Manufacturers:

Superior Electric Co, Middle St, Bristol CT 06010.

Sigma Instruments Inc, Motion Control Div, 170 Pearl St, Braintree MA 02184.

North American Philips Control Corp, Cheshire Industrial Park, Cheshire CT 06410.

Warner Electric Brake, MCS Div, Beloit WI 53511.

Computer Devices of California, 11901 Burke St, Santa Fe Springs CA 90670.

Singer Co, Kearfott Div, 1150 McBride Av, Little Falls NJ 07424.

Berger-Lahr, Jaffrey NH 03452.

Surplus Stepping Motors and Equipment:

AST/Servo Systems Inc, 930 Broadway, Newark NJ 07104.

Some Stepping Motor Calculations

The following formulas are commonly used in stepping motor calculations.

Distance = $s = \frac{1}{2}at^2 + v_o t + c$ where
- s = distance (inches or cm)
- a = acceleration (inch per second²)
- t = time (seconds)
- v_o = velocity, initial (feet per second or meter per second)
- c = constant.

Velocity (linear) = $v\ at + v_o$ where
- v = velocity (inch per second or meter per second)
- a = acceleration
- t = time
- v_o = velocity, initial.

Velocity (angular) = $\omega = v/(r\pi)$ where
- ω = angular velocity (radians per second)
- v = linear velocity (inch per second or meter per second)
- r = radius (inches or meters)

ω = (RPM) N/60 where
- RPM = revolutions per minute
- N = number of steps per revolution
- ω = angular velocity in steps per second.

(Similarly, the speed in revolutions per minute is RPM = ω 60/N.)

Torque = T = Fd, where
- d = radius from pivot point to force
- F = force applied or restraining force, ie: friction, weight, load (ounces or newtons).

The relationship between torque and rotary motion is:

$T = J(\omega/t)$ where
- T = torque (ounce-inches or newton-meters)
- J = moment of inertia (ounce-inch-seconds² or newton-meter-seconds²)
- ω = angular velocity (radians per second)
- t = time (seconds)

To use the equation with J in units of ounce-inches², multiply the inertia by 1/384 (ounce being a unit of mass in this case, instead of a unit of force as used above).

$T = J(\omega/t)(1/384)$

The moment of inertia for a rotating disk (pulley, gear, etc) is:

$J = Wr^2/2$ where
- J = moment of inertia
- r = radius of disk
- W = weight of disk

L/R Time Constant

The ratio of the inductance to resistance of a winding is used to determine the buildup or decay of current in a stepping motor. The basic equation which represents current flowing in a stepping motor is as follows:

$$I = I_{ss}\left(1 - e^{\frac{t}{-(L/R)}}\right)$$

where
- I = instantaneous current (amps)
- I_{ss} = steady state current in winding (amps)
- e = natural exponent = 2.718
- t = time (seconds)
- L = inductance in winding (henries)
- R = total resistance in the current path (ohms)

By examining the formula closely, it can be seen that the instantaneous current will reach its steady state value much sooner if the ratio of inductance to resistance is decreased. The result is that the motor will react faster to input signals, which will increase system performance.

shown for rated current, the curve will be shifted below the rated curve. A speed versus torque curve of the motor to be used will help to make the design much easier, and without unexpected disasters. By trying to operate safely below the curve, and observing the design rules, no unforeseen problems should be experienced with the system.

Once the motor has been selected and the drive fully completed, the next logical step is to make a speed versus torque curve of the motor and drive combination. This is important for a number of reasons. First, the speed versus torque curve obtained is the actual response of the motor and drive combination rather than a representative curve provided by the manufacturer. Second, it becomes a reference to compare against if any changes in the drive are made to alter its performance. Another reason for obtaining a curve is that it gives the experimenter a hands-on feel of the behavior of the stepping motor. (See text box for a detailed method of finding the torque of a stepping motor.)

I hope the information presented in these two articles will inspire you to use the versatile stepping motor for your own applications.■

Obtaining the Torque Curve: A Practical Technique

A simple technique for obtaining the curve is through the use of a spring scale (small fishing scale will serve the purpose) and a thin nylon cord. In this system, a cord suspended from a spring scale is wrapped several times around the motor shaft (or a lightweight pulley on the shaft) and is used to apply a frictional torque on the motor (see figure 24). Changing the size of the pulley will provide several ranges of torque. To find the torque, the motor is run at a constant speed and the free end of the cord is pulled very slowly. As friction builds up, the scale will begin to move. At the point where the motor stops turning, the value on the scale times the radius of the shaft (pulley) gives the maximum torque for that speed. This should be repeated several times to get the correct reading. This is repeated for several different speeds. The typical speed points taken start at 50 steps per second and proceed in increments of 50 steps per second up to 250 steps and then every 200 steps per second thereafter. Other points to find are the maximum torque point, maximum speed no torque point and resonance points. When enough points are taken to get an idea of the curve (about 10 to 15), the points are plotted on regular graph paper and a "best fit" curve is drawn through the points.

Warning: *Be careful at low speeds, because the motor can run backwards when it is "jerked" out of synchronism and wind the cord around the shaft in the reverse direction (your finger can get wrapped in there in larger motors). A thin nylon cord is preferable because of its strength. A point to remember is that this is a frictional load and that the shaft (pulley) and cord will heat up when trying to dissipate the energy.*

Ciarcia's Circuit Cellar

Build a Computer Controlled Security System for Your Home: Part 3

Steve Ciarcia
POB 582
Glastonbury CT 06033

There are many security systems on the market. From the simple $10 door buzzers which signal forced entry to elaborate professionally installed Rollins and ADT systems, their purpose is singular: give the occupant advance warning of an emergency condition. Protection of property is a secondary benefit of the more sophisticated alarms. Ultimately it is the overall complexity of the security system that defines how much coverage is attained in each of these areas.

Forced entry, prowler, and fire detection are but three possible events for which people buy alarms. A $15 smoke alarm alerts the occupants, who rush out of the house in the nick of time but stand watching the house burn because they didn't have time to call the fire department. Similarly, a prowler breaks into a home when the family is out. He has grown accustomed to the regular pattern of timer controlled lights after observing the house for a few nights and immediately disables the alarm horn upon entry. Had the occupants been home they of course would have been alerted to the break-in, but that was not the thief's intention.

To provide full protection, the ultimate security system should discourage intrusion, monitor all potential emergency situations and have the intelligence to initiate a preset series of actions should the alarming event ever occur. Combining all these elements into a single computer controlled security system is the subject of this and the two preceding articles (January 1979 BYTE, page 56; February 1979 BYTE, page 162). With the control system proposed and developed in this series, the user will have more of a process control computer than a burglar alarm. Except for the detection of the alarming event itself, a system designed to discourage intrusion and automatically respond to certain situations cannot be configured solely as a passive detection unit. The programs which this computer executes either in response to timed events or sensor inputs amount to a process control situation.

The computer controlled security system outlined in these three articles has the capability (presuming you have wired the same output controls as I have) to detect cars or people approaching a residence and track them by sequentially turning on flood lights aimed to cover the perimeter of the house, or give an audible warning in daylight situations. It can also control the power to AC appliances (TV, lights, stereo, etc) either to simulate occupancy or provide the luxury of remote control. This same software allows preset responses to water and temperature sensors for the control of wood heating, water circulating stoves or simply to turn on a pump in the basement. Should any perpetrator be ignorant enough to break in even after sufficient warning, the system has all the usual bells and whistles, an automatic telephone dialer, a hidden video tape recorder to obtain evidence, and, finally, a separate communications link to your neighbor.

The first article presented a general outline of the control system, the types of inputs available, and proposed responses. The second article described the hardware modifications to the SDK-85 computer used as the controller and provided an extensive description of the control and data acquisition software. With these three articles, more advanced readers should have enough information to configure a similar control computer using any microprocessor.

The final installment in the series presents examples of discrete input sensors to monitor temperature, moisture, motion, fire, and smoke. To allow the computer to make the proper response to such inputs, designs for flashing lights, strobes, siren, and AC remote control interfaces are also detailed. Finally, just to alleviate any lingering apprehensions over what appears to be a complex software algorithm, we will trace the flow of an alarm input as it is processed by the security system and demonstrate the versatility of table-driven software in this application.

The Alarm System Is Only as Good as Its Input Sensors

The SDK-85 has 38 bits of parallel I/O (input/output). In this application 18 of these bits have been set aside to control outputs, while the remaining 20 are used solely for input. Because the computer is composed of TTL (transistor-transistor logic) circuitry, any input to it must also be TTL compatible. It is a further requirement that all signals be discrete in nature. That is, they change state from a 1 to a 0 or a 0 to a 1 level when the set point is attained. Analog inputs are not beyond the capabilities of the software, but no analog to digital interface has been built into the system.

Analog Input Sensors

Temperature and voltage are important analog parameters which any sophisticated alarm system requires if it is to monitor freezer or furnace room temperature and brownout conditions. The circuit of figure 1 can be used to read temperature setpoints. IC1 is a special integrated circuit having an output voltage proportional to temperature.

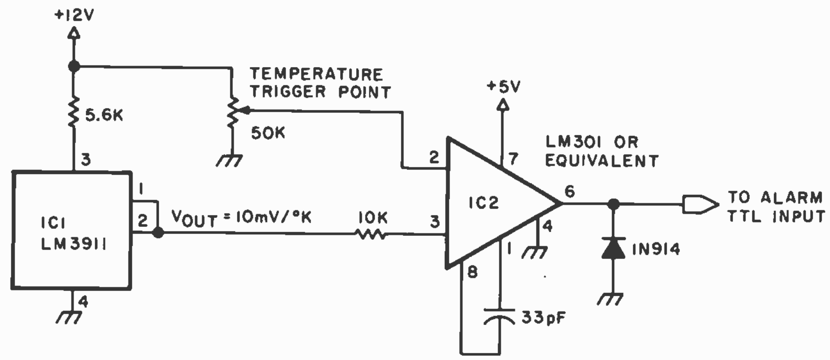

Figure 1: Temperature setpoint indicator circuit. IC1 is a special integrated circuit whose output voltage is proportional to temperature. The circuit feeds into an Intel SDK-85 single board computer, which accepts only TTL (transistor-transistor logic) level inputs. Op amp IC2 is used as a computer to convert the output accordingly.

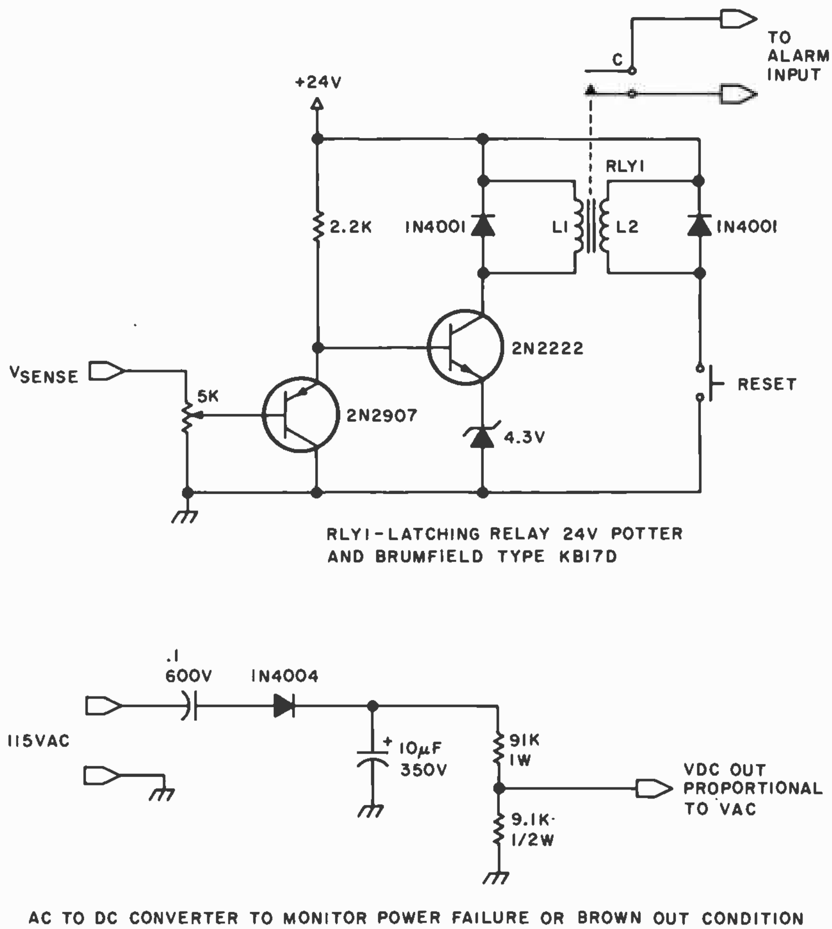

Figure 2: Circuit which can be used to monitor any DC voltage between 0 and 24 V. A latching relay is used to latch on when a voltage transient occurs.

Since the SDK-85 can respond only to TTL inputs, op amp IC2, configured as a comparator, changes logic levels when the output of IC1 equals the setting of the temperature trigger pot. IC2 is powered by a 5 V power supply so that the output is TTL compatible. If a multiple array of temperature transducers is to be constructed, use an LM339 quad comparator instead of four LM301s to reduce wiring complexity. Another analog circuit, shown in figure 2, can be used to monitor any DC voltage between 0 and 24 V. It could be used to monitor the battery backup supply to the computer or some other important parameter. Since voltage fluctuations are often significant and desirable to catch, the circuit uses a latching relay to keep it in the set condition once triggered. If that is not a desirable feature, then replace RLY1 (relay 1) with a nonlatching type. A relay should continue to be used, however, because it isolates the computer from the monitored voltage sources.

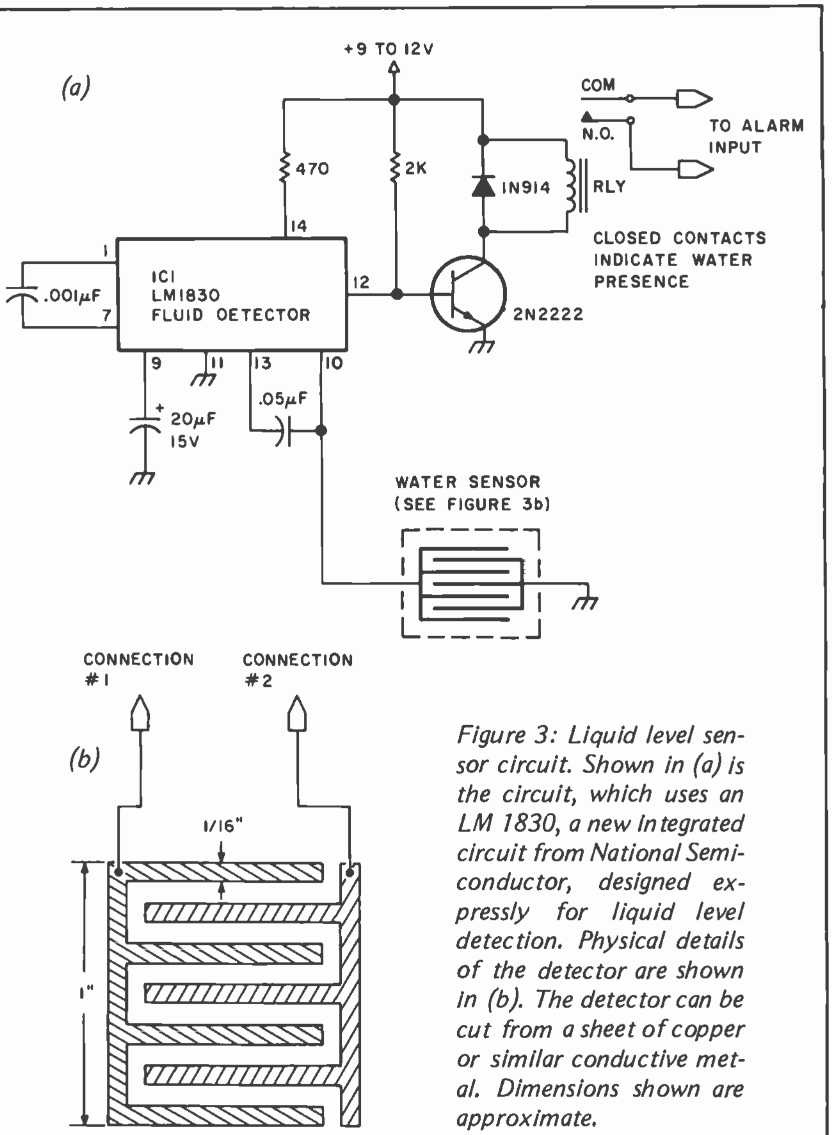

Figure 3: Liquid level sensor circuit. Shown in (a) is the circuit, which uses an LM 1830, a new Integrated circuit from National Semiconductor, designed expressly for liquid level detection. Physical details of the detector are shown in (b). The detector can be cut from a sheet of copper or similar conductive metal. Dimensions shown are approximate.

Discrete Input Sensors

Actually, all inputs to the computer are discrete, and this need not be a separate category. The outputs from the sensors are primarily contact closures for a reason I'll explain later. Some of the important ones worth considering are liquid level or moisture, smoke and fire, and ultrasonic and infrared interrupted beam motion detectors.

A liquid level sensor suitable for detecting basement flooding so that a sump pump can be turned on is illustrated in figures 3a and 3b. This circuit uses a new integrated circuit from National Semiconductor specifically

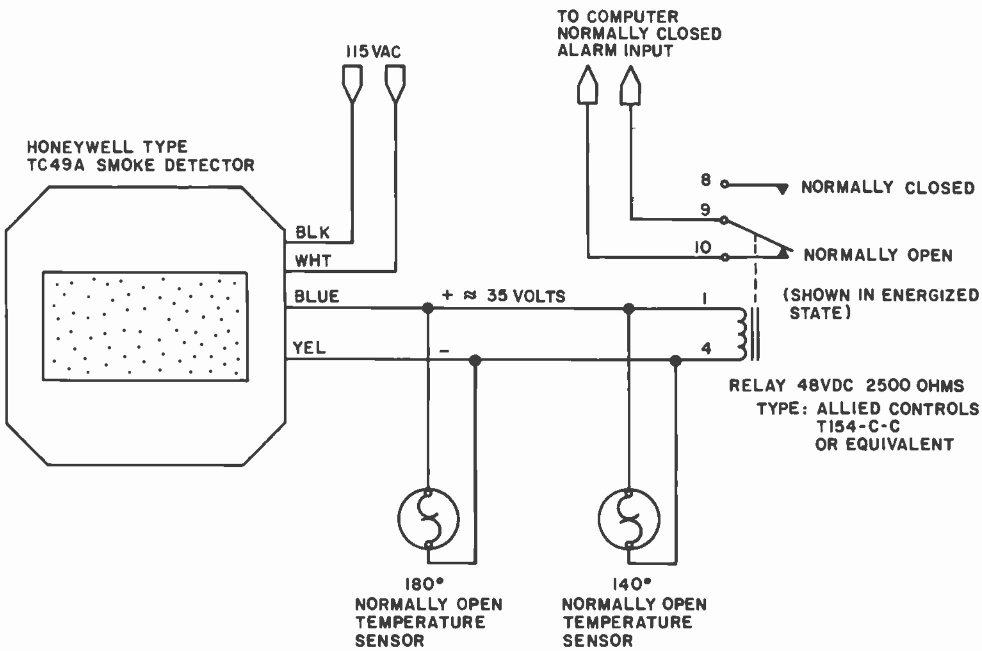

Figure 4: Commercial smoke detector with additional temperature sensors and data acquisition output added. Additional sensors may be added in parallel.

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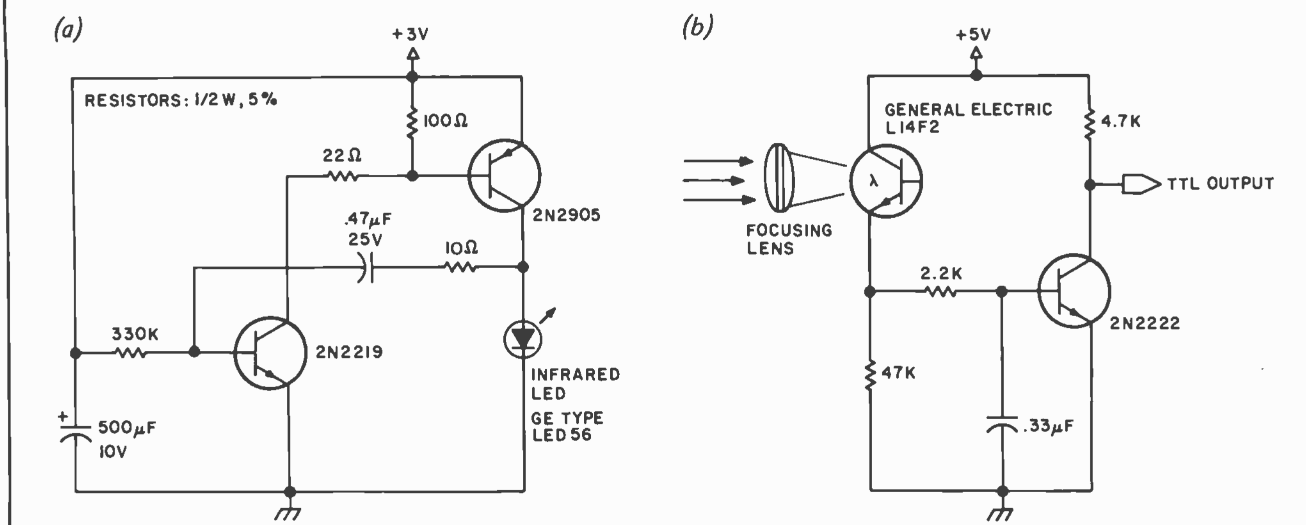


Figure 5: Intrusion alarm infrared transmitter and detector. Shown in (a) is a low voltage pulsed LED (light emitting diode) transmitter; the light beam receiver with optional focusing lens is shown in (b). The lens extends the range of the unit from approximately 10 to 50 feet. Anyone or anything breaking the beam will alert the security system.

designed for this purpose. As configured, the relay contacts will close in the presence of water or condensing moisture. The circuit is extremely sensitive and can be used with practically any conductive liquid.

Probably the most important sensors on the security system are the ones that detect fire and smoke. A commercially available ionization type smoke detector, shown in figure 4, has been configured to interface to the computer. The AC powered TC49A by Honeywell is ideally suited for this purpose, since it is designed for parallel attachment to other sensors. In this instance any number of normally open temperature sensors can be attached between the blue and yellow output leads of the device. Should any of these sensors or the smoke detector itself detect an alarm condition, the 35 V normally present on these wires will drop 2 V. The relay which had previously been in an energized state will open, signaling the event to the computer. Protection must be provided during power failures, however, so that the computer (which has an emergency supply) does not detect a false alarm. If the program which scans the smoke alarm also checks the power failure sensor, positive results should be obtained. In any case it is always a good idea to have a battery powered smoke detector also within the residence.

Note that the majority of sensor designs presented in this article can be used independently. The device normally activated when the sensor signals an alarm condition can be attached and directly controlled through another parallel set of relay contacts. An example would be the water detector that automatically turns on the sump pump. Requiring the computer to receive the signal, process the control record, and turn on an AC powered pump would be a waste of wire. The computer need know only that the high water mark has been reached to notify the residents on the display panel: it does not have to control it as well. Before you string a mile of wire through the house, consider what functions really need "computer" rather than "local" control.

The two remaining special input sensors are related in purpose. Both are used to detect an object or person passing between two points, and both use interrupted beam sensing techniques. One is an infrared light beam and the other is ultrasonic. The light beam circuit is shown in figure 5 and the ultrasonic circuits are illustrated in figure 6. The range of the infrared unit is about 10 feet without a lens and as much as 50 feet with proper ambient light shielding and a focusing lens. No focusing was tried on the ultrasonic unit, but 25 feet was easily achieved.

Testing and alignment of the ultrasonic transmitter can be tricky, while the infrared is simply a mechanical alignment consideration. First, the transmitter must be tuned to resonance. The nominal frequency of the ultrasonic transducers can be 34 to 42 kHz; they should be bought in pairs. An oscilloscope should be put across the transducer in the transmitter circuit when power is applied. Coils T1 and T2 should then be adjusted to produce the greatest amplitude across the transducer. The usual value is about 30 V peak-to-peak and the frequency should be the nominal F_0 listed for the part.

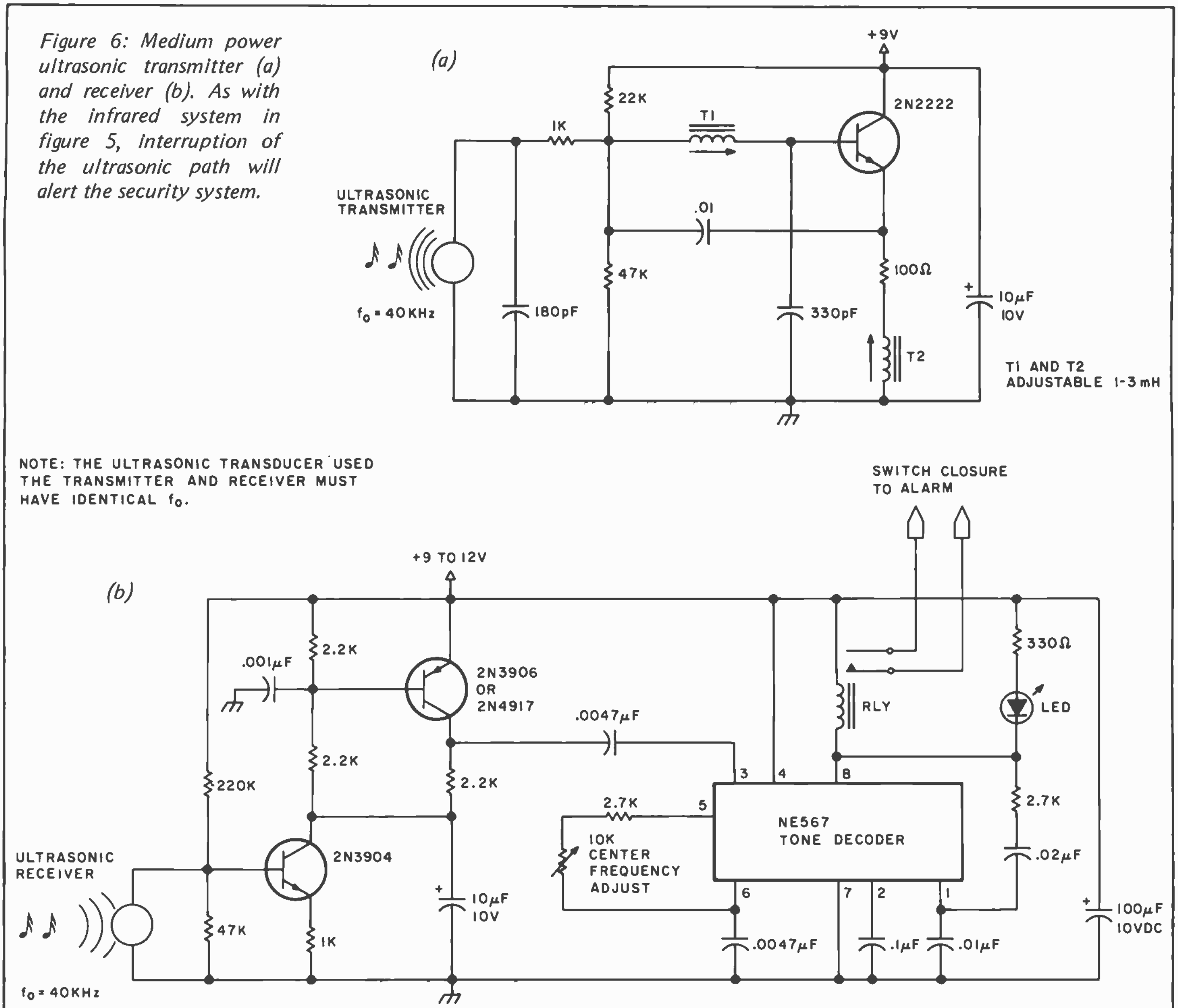
Once the transmitter is tuned, place it about 2 feet in front of the receiver. Adjusting the center frequency adjustment pot should cause the relay to pull in and the LED (light emitting diode) to light. The transmitter and receiver can now be placed across a driveway or large room.

Wireless Inputs

So far we have only discussed input sensors which are directly wired to the connectors of the SDK-85 computer. If a reed switch were attached to the garage door a wire must be run from it to the computer. In a larger house this can amount to a lot of wire and can extend system construction time. One possible solution is to use a wireless transmitter and receiver between the computer and remote points within the house.

Homebrew wireless transmitters, while cheap, suffer from a lack of reliability. They are not being considered for this application because there is a commercial unit available which is both cost effective and reliable. The particular device is the Norelco Home Patrol wireless burglar alarm system available in most discount stores for about $200. It consists of a receiver, four contact-closure-activated transmitters, and a smoke

Figure 6: Medium power ultrasonic transmitter (a) and receiver (b). As with the infrared system in figure 5, interruption of the ultrasonic path will alert the security system.



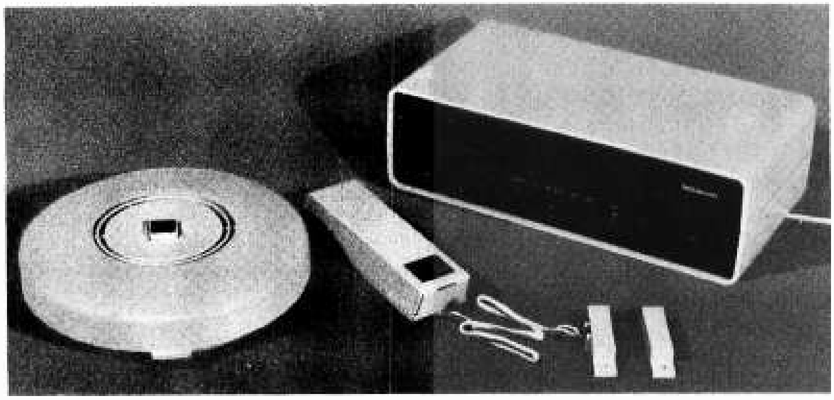


Photo 1: Norelco wireless alarm system. The three components from left to right are: wireless smoke detector, wireless door sensor, and master receiver.

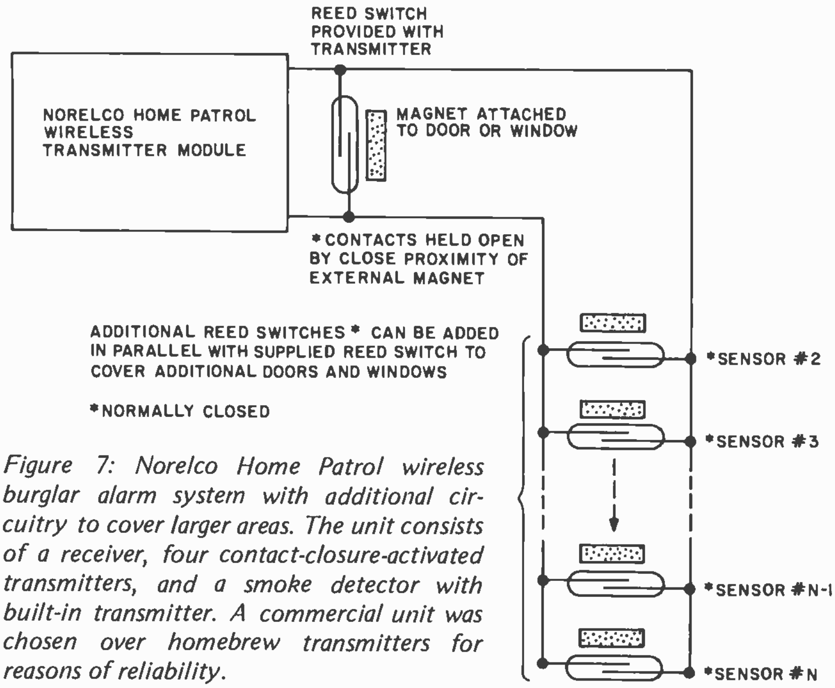
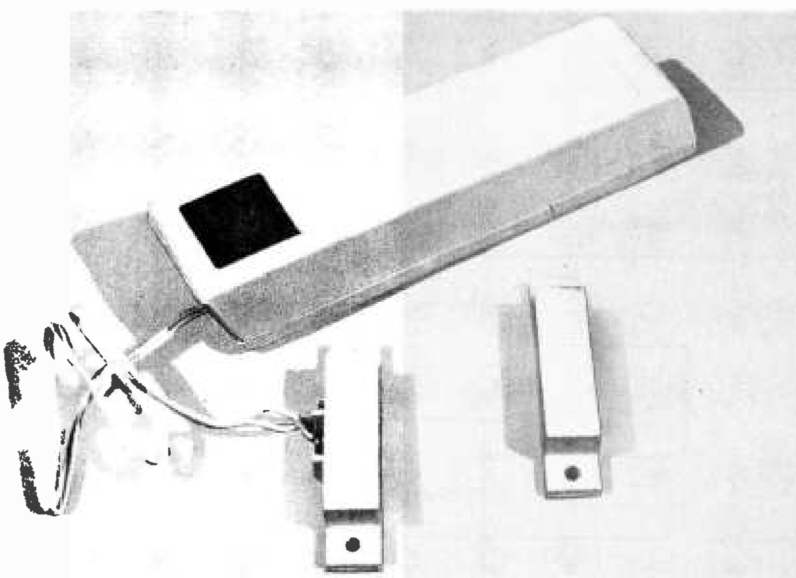


Figure 7: Norelco Home Patrol wireless burglar alarm system with additional circuitry to cover larger areas. The unit consists of a receiver, four contact-closure-activated transmitters, and a smoke detector with built-in transmitter. A commercial unit was chosen over homebrew transmitters for reasons of reliability.



detector with built-in transmitter. Photo 1 shows the components of the system and figure 7 details how each of these separate transmitters can be expanded to cover a wider area.

The Norelco receiver has four separate output channels designated as fire, intrusion, car, and miscellaneous. Transmitters are supplied for intrusion and fire only — transmitters for the other two channels must be purchased separately. Photo 2 shows one of these devices.

Photo 3 shows the output connections of the receiver and figure 8 illustrates the type of interface which must be constructed to convert the 0 and −15 V Norelco receiver outputs to be TTL compatible. Only then can the security system be aware of these remote alarm inputs.

Security System Outputs

Once an alarm condition has been detected or the event processor activated, the security system responds accordingly. Whatever the cause, the output will be a TTL change of state which can be used to drive a mechanical or solid-state relay. Typical output interfaces are warble alarms, high intensity flashers, and strobe lights. They are shown in figures 9, 10 and 11, respectively.

AC output control can be handled in either of two ways: solid-state or mechanical relays. While solid-state relays are definitely the more modern approach, it is very difficult to find control panels incorporating them which are understandable to electricians or which meet local electrical codes. Rather than fight the system it was easier to install a readily available relay control panel as shown in photo 4. The two cabinets on the right are relay cabinets, and the one on the left is the regular breaker box. Each relay enclosure contains six relays. The left relay enclosure controls the six outside light circuits and the righthand enclosure remotely controls six wall outlets around the house. The relays are DC input and can either be controlled directly from the computer or manually from scattered points around the house. Each of the 12 relay outputs requires a separate cable to the outlet or light to be controlled. This is not an inexpensive control method, but it does meet the code and is a convenience once installed.

Two other details left to be considered are the emergency power supply to the com-

Photo 2: Single wireless transmitter with one read switch attached to it. Multiple reed switches can be attached in parallel to cover a wider area, as described in the text.

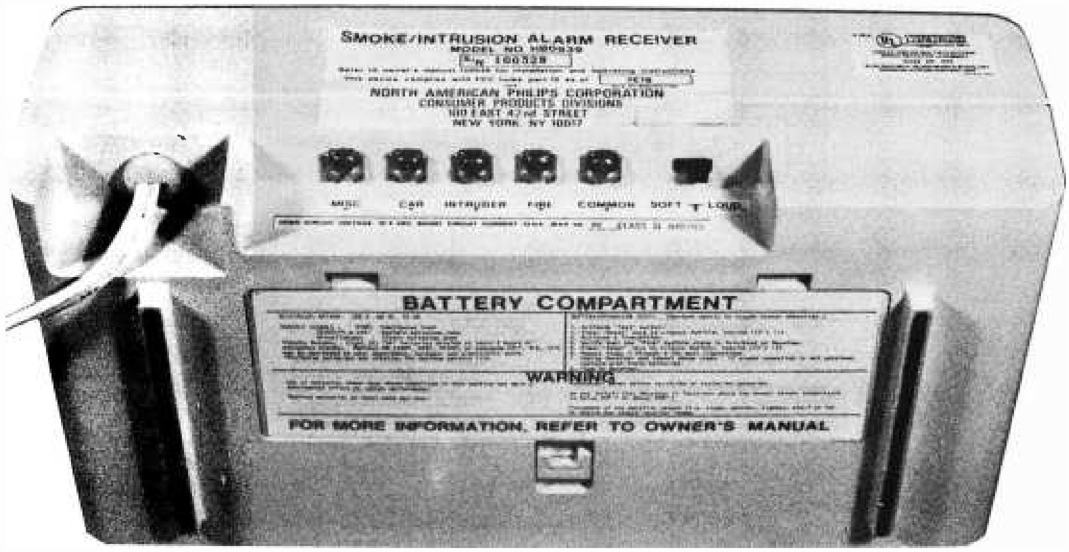


Photo 3: Output connections of the Norelco receiver. Using the circuit described in figure 8, the outputs of the Norelco receiver can be easily interfaced to the computer. There are four distinct output channels of the Norelco unit. As purchased in its basic form it comes with transmitters for fire and intrusion only.

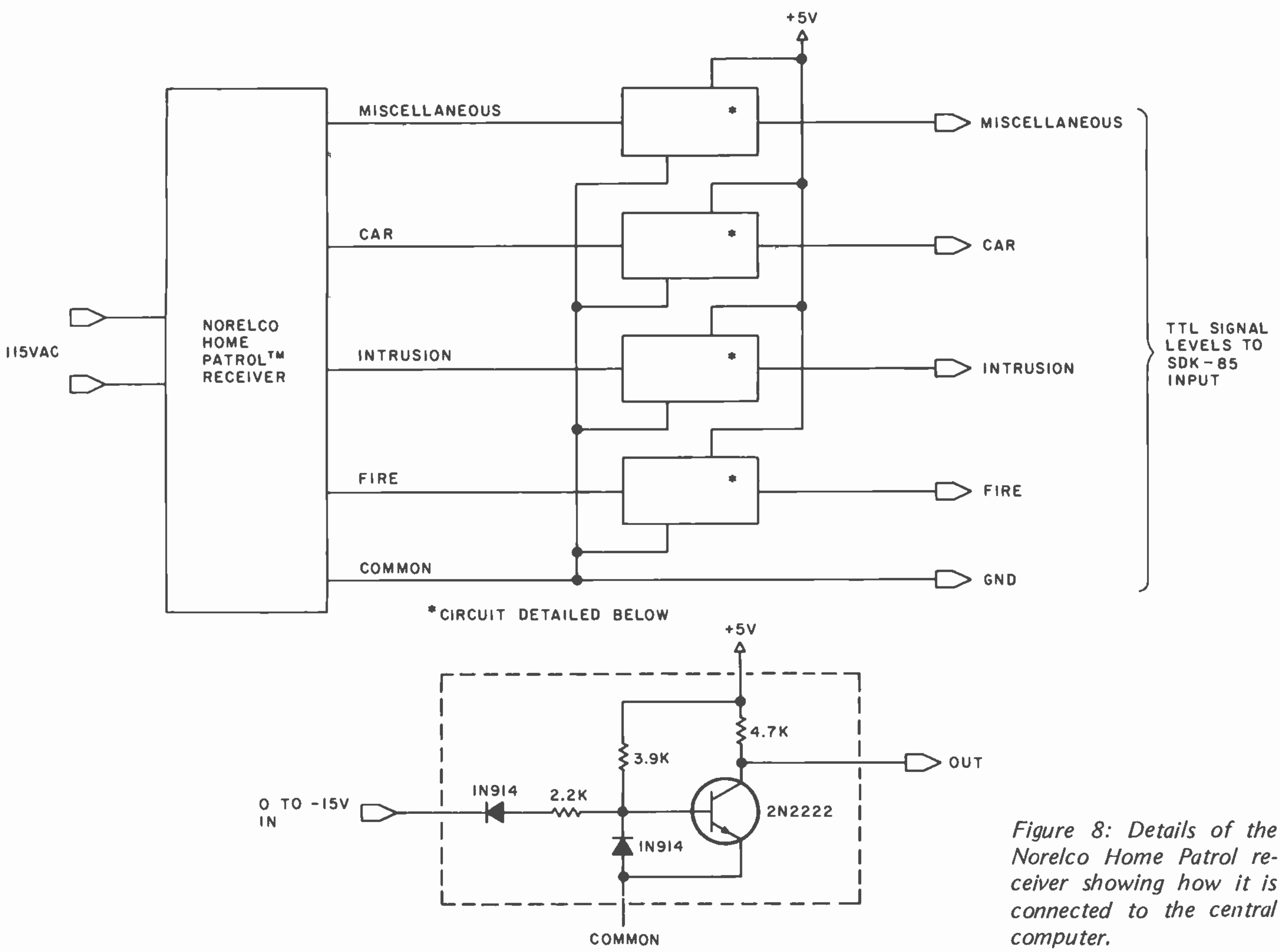


Figure 8: Details of the Norelco Home Patrol receiver showing how it is connected to the central computer.

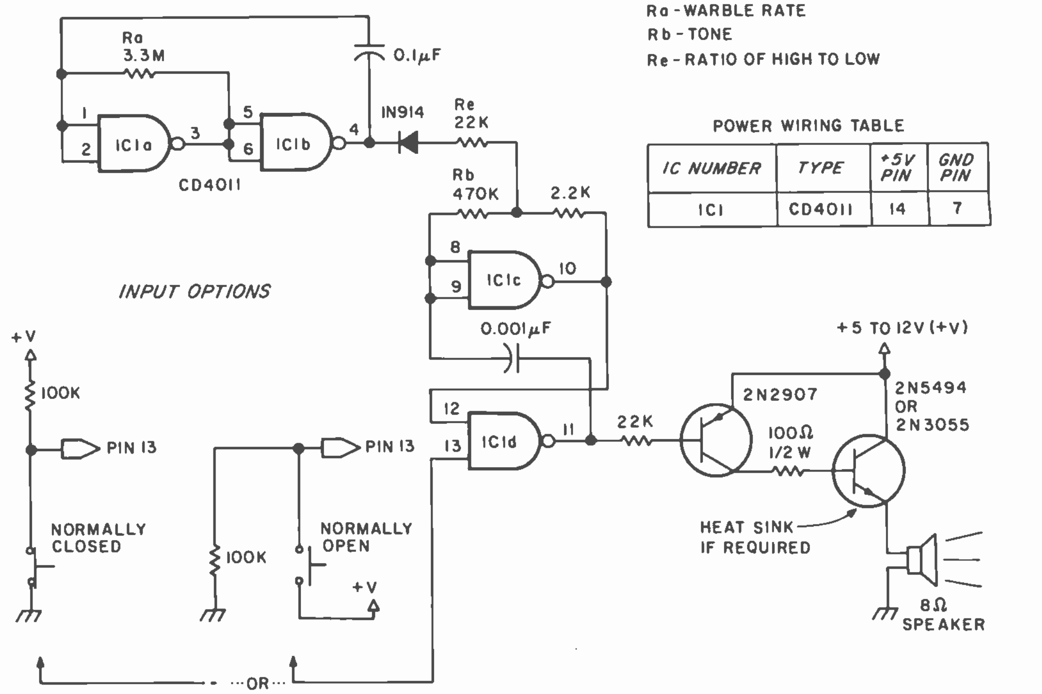


Figure 9: CMOS warble alarm.

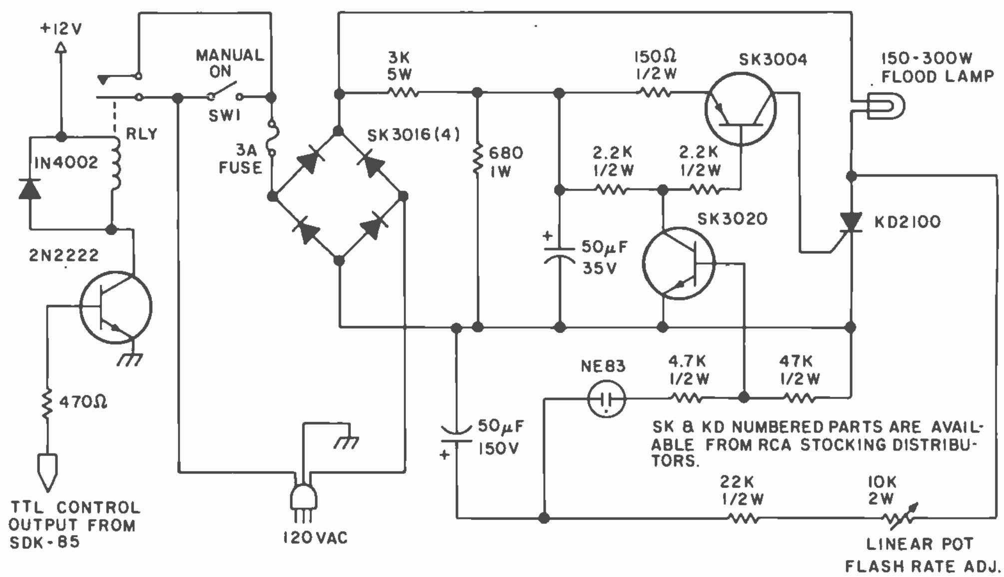


Figure 10: 115 VAC incandescent lamp flasher.

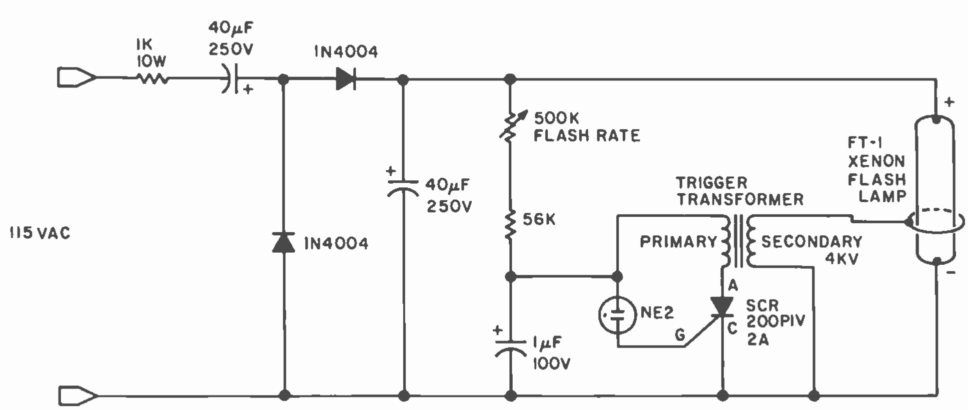
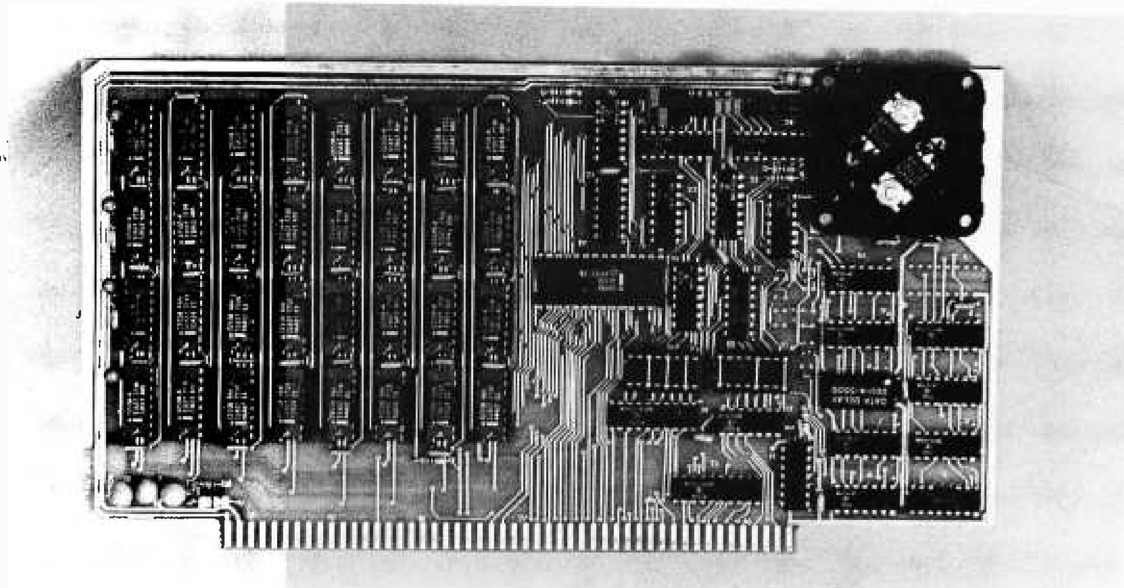


Figure 11: 115 VAC Xenon strobe light. Parts for this circuit are available from Chaney Electronics, 2010 W Dartmouth Unit # 8, Englewood CO 80110.



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Wait states generated	None
Maximum DMA rate	1 Mhz

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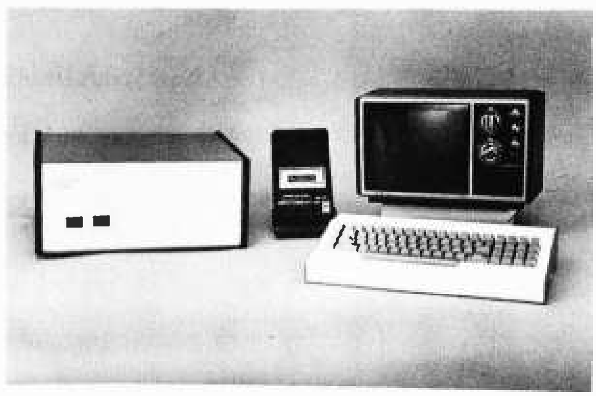

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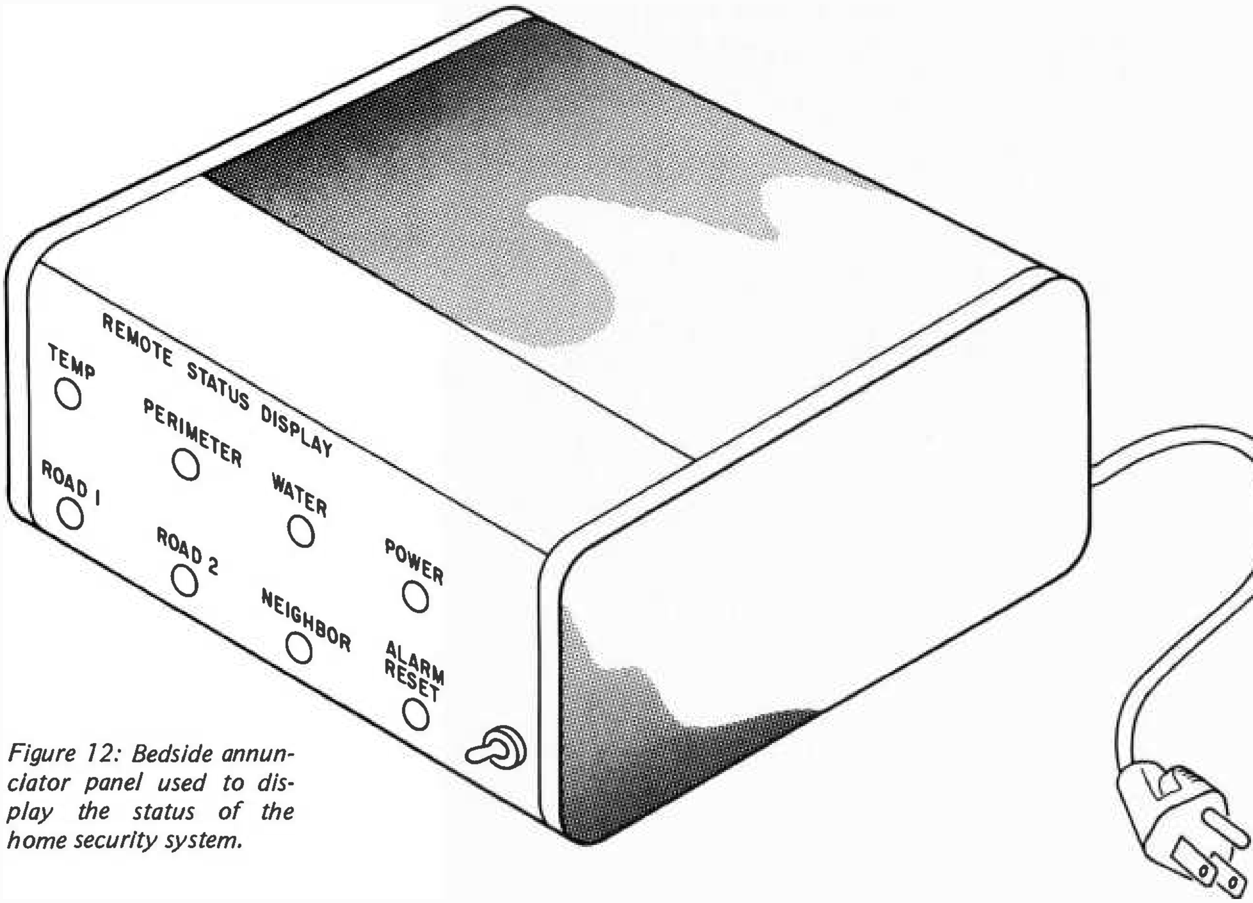


Figure 12: Bedside annunciator panel used to display the status of the home security system.

puter and the display panel located in the bedroom.

The Alarm Status Display Panel

The purpose of the alarm status display panel is to provide the resident with a graphic representation of the status of the security system. Figure 12 is a sketch of a simple annunciator (the picture was omitted because the control panel I finally built bears no resemblance to the purpose we are discussing, and might be confusing since it contains numerous additions to the basic concept).

The circuit (see figure 13) is simply a BCD (binary coded decimal) to decimal decoder driver which is multiplexed by a 3 bit output from the SDK-85. The computer sequentially sends out the codes for the particular lights to be lit. This is done repeatedly and with sufficient speed so that they appear constant. If the annunciator panel is more than 50 feet from the computer, the user may want to consider the addition of the line drivers also described.

Emergency Power Supply

Should power ever be lost in the residence, it is important to maintain the security system in an active mode. To do this a 12 V automobile battery is used to power the computer *all the time*. The SDK-85 5 V power is derived from the 12 V through a regulator. The EROM (erasable read only memory) can be either a single +5 V unit such as a 2716; or, if using a 2708, the −12 V can be derived using one of the circuits outlined in my article "No Power for Your Interfaces? Build a 5 W DC to DC Converter" (October 1978 BYTE, page 22). The requirements of such a power supply are maintenance of the 12 V on the battery, recharging the battery as it needs it, and also providing standby power to critical sensors and alarms.

Tracing an Activated Alarm Condition: An Example

Part 2 of this series (February 1979 BYTE, page 162) emphasized the software of our computerized home security system. To adequately complete the description of this design, it is necessary to include an example which illustrates the use of table driven software. Included is a listing of the digital scan module and various response modules which should aid in understanding.

Suppose one of the functions of the system is to respond to a smoke and fire detector. First, assume that the sensor in question is wired into the least significant bit (bit 0) on port 0. Response to this sensor is on a reset-to-set (0 to 1) transition, and that on a set-to-reset (1 to 0) transition no action is to be taken. As detailed in part 2 of this series, the initial state change is detected by DIGSCN (the digital scan module) which uses the information contained in XFVE (the sensor state transfer table) to initiate the processing of a digital event. If you recall, the sensor state transfer table is comprised of four byte records, with one record being required for each digital input:

Sensor State Transfer Record

Bytes 0 and 1: event record address for reset-to-set transition plus active/inactive flag (bit 7);
Bytes 2 and 3: event record address for set-to-reset transition plus active/inactive flag (bit 7).

The smoke and fire detector connected to bit 0 input uses the first record in the sensor state transfer table to initiate the required responses. Since no action is required for a set-to-reset transition, bytes 0 and 1 are set equal to hexadecimal FF. This makes such a transition inactive (active/inactive flag = 1). We do, however, want to process a smoke and fire alarm. Therefore, bytes 2 and 3 must contain the address of the event record associated with the alarm. For this example let us assume that the address of the event record used to process this alarm is at hexadecimal 4214 (therefore byte 2 of the transfer record will equal hexadecimal 14 with byte 3 being equal to 42):

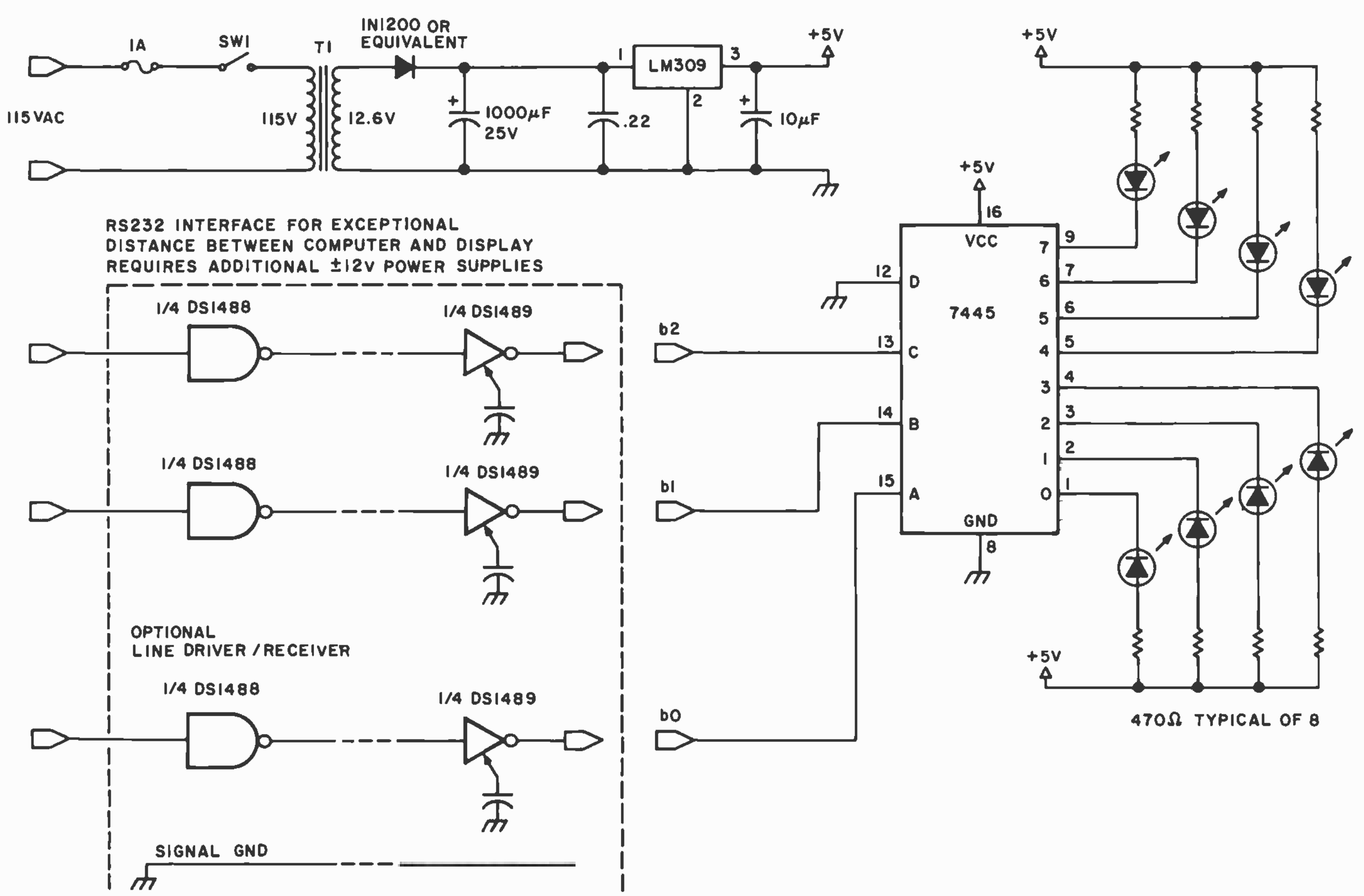
Sensor State Transfer Record for Smoke and Fire Alarm

Byte 0 = FF;
Byte 1 = FF;
Byte 2 = 14;
Byte 3 = 42.

To summarize, the digital scan module detects the transition of the smoke and fire sensor from a reset to a set state. Using the information contained in the sensor state transfer table, the system processes the event by first extracting the address of the event record associated with this alarm and then activating EVPRO (the event processor module).

EVRREC (the event record), which is used by the event record processor, contains the indices to the various response records associated with this alarm. As you may recall, one of the features of this system is its ability to associate several responses to

Figure 13: Driving circuitry for the annunciator panel (see figure 12). A BCD (binary coded decimal) code from the computer is converted to decimal by IC7445 to drive the LEDs on the panel, which are driven sequentially with sufficient speed so they appear to be lit constantly. An optional RS-232 interface for driving the circuit at some distance from the computer plus a 5 V power supply are also shown.



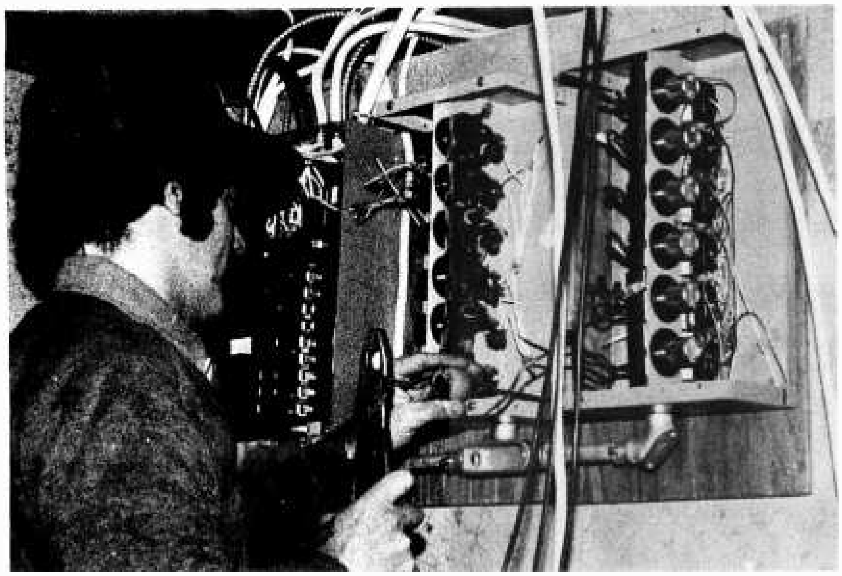


Photo 4: Electrician Vince Sadosky installing "Touch Plate" control system. Each enclosure (of the two on the right) contains six 15 A latching relays. The relay is a pulse on/pulse off type in which the control pulse can come from either a manual pushbotton panel in the kitchen or from the computer.

a single event. The event record is the mechanism which accomplishes this as follows:

Event Record Format

Byte 0: number of responses associated with record;
Byte 1: relative index of response record i;
Byte 2: relative index of response record j;

•
•
•

Byte n: relative index of response record z.

Initially the response might be to activate the autodialer notifying the police and fire departments of the predicament. But before doing that, let us take a few seconds to check for a false alarm and, if possible, verify the situation. This can be accomplished with the following responses to the alarm. First we do want to initiate the autodialer. So, our first response will be the initiation of a 60 second delay of the autodialer. Next, since we may be in the bedroom and unable to hear the alarm itself, we will initiate an audible alarm – and, so that we can tell the location of the alarm, we will display the location of the alarm on the annunciator panel.

These functions will require an event record containing the indices of the following responses:

- Delay timer activation for the 60 second delay.
- Application task response for driving the annunciator.
- Digital output response for activating the audible alarm.

In this example it is assumed that the response indices are 0, 1, and 2, respectively. The event record for this event will therefore be four bytes in length as follows:

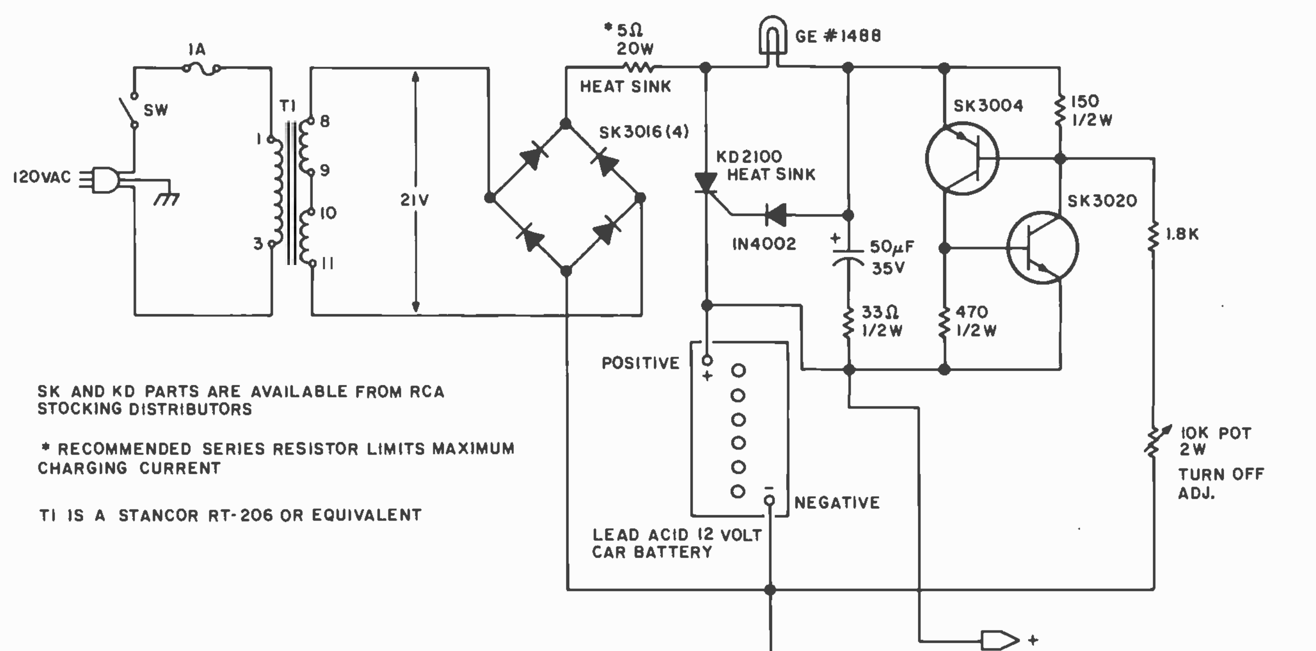


Figure 14: Automatic charger circuit for the 12 VDC car battery computer backup power supply.

Listing 1: Selected 8080/8085 subroutines for the home security system.

```
ZERO    EQU     0
ONE     EQU     1
P1      EQU     0               *PORT 1
P2      EQU     1               *PORT 2
P3      EQU     2               *PORT 3
*
* THE FOLLOWING AREAS ARE TO BE LOCATED IN RAM
*
TEMP1   DB      0
TEMP2   DB      0
TEMP3   DB      0
PORT1   DB      0               * CURRENT INPUT DATA FOR PORT 1
PORT2   DB      0               * CURRENT INPUT DATA FOR PORT 2
PORT3   DB      0               * CURRENT INPUT DATA FOR PORT 3
PROT1H  DB      0               * PREVIOUS INPUT STATE FOR PORT 1
PORT2H  DB      0               * PREVIOUS INPUT STATE FOR PORT 2
PORT3H  DB      0               * PREVIOUS INPUT STATE FOR PORT 3
OPORT   DS      3               * OUT PUT PORT STATUS
DIGIND  DB      0               *DIGITAL INPUT BIT PROCESSING INDEX
XFVE    DS      500             *SENSOR STATE TRANSFER TABLE
EVRREC  DS      3000            *EVENT RECORD FILE
TODREC  DS      1000            *TIME OF DAY RECORD FILE
TIMREC  DS      1500            *DELAY TIMER RECORD FILE
RESREC  DS      1500            *RESPONSE RECORD FILE
DIGREC  DS      360             *DIGITAL OUTPUT RECORD FILE
*
*THE FOLLOWING MODULES REPRESENT THE MODULES
* REQUIRED FOR PROCESSING THE  OCCURRANCE OF
* A DIGITA EVENT.  THESE MODULES WOULD RESIDE IN PROM
*
*
* THE DIGITAL SCAN MODULE READS THE DIGITAL
* INPUTS. COMPARES THE CURRENT STATE WITH THE PREVIOUS
* STATE AND IF DIFFERENT INITALIZES THE PROCESSING
* OF THE STATE CHANGE.  UPON CUMPLETUON OF THE DIGITAL
* INPUT PROCESSING THE HISTORY STATE
* OF THE DIGITAL INPUTS IS UPDATED AND THE
* NEXT SCAN INITIATED
*
DIGSCN  IN      P1              *INPUT PORT 1
        STA     PORT1
        IN      P2              *INPUT PORT 2
        STA     PORT2
        IN      P3              *INPUT PORT 3
        STA     PORT3
        MVI     A,0             *RESET DIGITAL PROCESSING INDEX
        STA     .DIGIND
*
* ISOLATE BIT FROM HISTORY AND CURRENT DIGITAL STATE
*
DIGI1   LDA     DIGIND          *GET PROCESSING INDEX
        CPI     8D              *INDEX .GT.9
        JC      DIG4            *JUMP IF INDEX=0-7
        CPI     16D             *INDEX.LT.16
        JC      DIG3            *JUMP IF INDEX =08-15
*
* PROCESS THIRD PORT
*
        LXI     H,PORT3         *HL=PORT3 DATA ADDRESS
        LXI     D,PORT3H        *DE=PORT3 HISTORY ADDRESS
DIG2    CALL    COMBIT          *GO COMPARE BIT
        CPI     0               *IF A=0 NO CHANGE
        JNZ     DIGPRO          *IF A=U /R 2 GO PROCESS STATE CHANGE
DIG22   LDA     DIGIND          *INCREMENT PROCESS INDEX
        CPI     25D             *ALL INPUTS PROCESSED
        JNZ     DIGI1           *JUMP IF NOT
        JMP     DIGSCN          * GO RESTART SCAN
*
* PROCESS SECOND PORT
*
DIG3    LXI     H,PORT2         *HL=PURT 2 DATA ADDRESS
        LXI     D,PORT2H        *DE=PURT 2 HISTROY ADDRESS
        JMP     DIG2
*
* PROCESS FIRST PORT
*
DIG4    LXI     H,PORT1         *HL=PURT 1 DATA ADDRESS
        LXI     D,PORT1H        *DE=PORT1 HISTORY ADDRESS
        JMP     DIG2
*
* IF A= 1 PROCESS A SET STATE
* IF A=2 PROCESS A RESET STATE
* DIGIND CONTAINS THE RELATIVE INDEX INTO
* THE SENSOR STATE TRANSFER VECTOR TABLE
*
DIGPRO  STA     TEMP1
        LXI     H,XFVE          *HL=BASE ADDRESS
        LDA     DIGIND
        DCR     A
        RLC                     *DIGIND*4
```

Event Record for Smoke and Fire Alarm

Hexadecimal Address	
4214 = 3	number of responses;
4215 = 0	response record indices for event.
4216 = 1	
4217 = 2	

The event processor will process the entries in the event record sequentially, extracting the response record index and activating RESPRO (the response record processor). Using this index the response processor will obtain RESREC (the indicated record from the response file) and direct the activation of the appropriate subprocessors, which contain the following information:

Byte 0 = response type:
- 0 = digital output;
- 1 = application module;
- 2 = delay activation;
- 3 = delay deactivation;
- 4 = time-of-day activation;
- 5 = time-of-day deactivation.

Bytes 1 and 2 = module address of record index.

For our example the records will be as follows:

Response File

Record 0	Byte 0 = 2 Byte 1 = 0 Byte 2 = 1	second delay timer record;
Record 1	Byte 3 = 1 Byte 4 = 0F Byte 5 = 2C	address of annunciator application module;
Record 2	Byte 6 = 0 Byte 7 = 0 Byte 8 = 0	first digital output record.

The first record processed causes DELINT (the delay module) to activate the second record in TIMREC (the delay timer file). These records contain the delay time (in seconds) and address of the event record to be activated when the directed delay has timed out:

Delay Time Record

Bytes 0 and 1: active flag plus remaining time;
Bytes 2 and 3: number of seconds to delay;
Bytes 4 and 5: address of event record.

In our example this record (prior to activation) will appear as follows:

Bytes 0 and 1: 80, 0 = record inactive;
Bytes 2 and 3: 0, 3C = 60 second delay;
Bytes 4 and 5: 18, 42 = event record at hexadecimal 4218.

After the delay has been initiated, the event processor will notify the response processor to initiate the second response.

Listing 1, continued:

```
         RLC
         MOV     C,A
         MVI     B,ZERO
         DAD HL,BC
         LDA     TEMP1
         CPI     2
         JZ      DIGP1          *JUMP IF SET TO RESET
         INX     H
         INX     H
DIGP1    LDAX    DE             *DE=TRANSFER VECTOR
         CPI     80H            *IS HIGH ORDER BIT SET
         JNC     DIG22          *JUMP IF RECORD INACTIVE
         LDAX    DE
         MOV     L,A
         INX     DE
         LDAX    DE
         MOV     H,A
         CALL EVPRO             *PROCESS EVENT RECORD
         JMP     DIG22
*
* COMBIT ISOLATES AND COMPARES THE DATUM BIT
* IN THE CURRENT AND HISTORICAL DIGITAL INPUT
* STATE TABLES
*
* HL=CURRENT DATA ADDRESS
* DE=HISTORY DATA ADDRESS
*
COMBIT   LDAX    D              *A=HISTORY DATA
         CMP     M              *COMPARE HISTORY TO CURRENT
         JZ      COM5           *JUMP IF CURRENT=HISTORY
*
* NO COMPARE  ISOLATE BIT
*
         MVI     A,1            *SET MASK=1
         JMP     COM2
COM1     CPI     0              *SHIFT COUNT=0
         JZ      COM4           *JUMP IF SHIFT COUNT=0
         RLC     A              *SHIFT MASK BIT
COM2     STA     TEMP2          *SAVE MASK
*
* GET CURRENT STATE BIT
*
         MOV     B,M            *B=CURRENT DATA
         ANA     B              *A=CURRENT STATUS BIT
         STA     TEMP3          *TEMP3=CURRENT BIT STATUS
         XCHG
         MOV     B,M
         LDA     TEMP2
         ANA     B
         MOV     B,A            *B=HISTORY BIT
         LDA     TEMP3          *A=CURRENT BIT
         CMP     B              *COMPARE BITS
         JZ      COM6           *RETURN IF EQUAL
*
* CURRENT .NE. HISTORY
* UPDATE HISTORY STATE
*
         CPI     0              *IS BIT RESET
         JNZ     COM3           *JUMP IF BIT SET
* RESET HISTROY STATE
         LDA     TEMP2          *GET MASK
         CMA                    *COMPLIMENT MASK
         XCHG
         ANA     M
         MOV     M,A            *STORE HISTORY
         INR     A
         STA     DIGIND
         MVI     A,2
         RET
*
* SET HISTORY STATE
*
COM3     LDA     TEMP2          *GET MASK
         ORA     M              *A=NEW HISTROY
         MOV     M,A            *STROE NEW HISTORY
         LDA     DIGIND
         INR     A
         STA     DIGIND
         MVI     A,1
         RET
*
COM5     LDA     DIGIND
         ADD     8D
         STA     DIGIND
COM4     MVI     A,0            *A=0
         RET
COM6     XCHG
         LDA     DIGIND
         INR     A
         STA     DIGIND
```

Listing 1, continued:

```
        LDA     TEMP2
        JMP     CONT
*
* THE EVENT RECORD PROCESSOR OBTAINS THE INDEX
* OF THE RESPONSE RECORD FROM THE EVENT RECORD
* CALCULATES ITS ADDRESS
* AND CALLS THE RESPONSE RECORD PROCESSOR
*  EVENT RECORD ADDRESS IS IN H/L
EVPRO   MVI     A,ONE           *SET INITIAL INCEX
        PUSH    AF              *SAVE INDEX
        PUSH    HL
EVPR1   INX     HL              *INCREMENT RECORD ADDRESS
        PUSH    HL              *SAVE RECORD ADDRESS
        MOV     A,M             *A=RELATIVE RESPONSE RECORD INDEX
        CALL    RESPRO          *CALL EESPONSE RECORD PROCESSOR
        POP     HL              *GET EVENT RECORD ADDRESS
        POP     DE              *GET INITIAL RECORD ADDRESS
        POP     PSW             *A=GET INDEX
        INR     A               *INCREMENT INDEX
        XCHG                    *HL=INITIAL ADDRESS
        MOV     B,M             *B=NUMBER OF RECORDS TO PROCESS
        XCHG
        PUSH    DE              *SAVE INITIAL RECORD ADDRESS
        CMP     B               *HAVE ALL RESPONSE RECORDS BEEN PROCESSED
        JZ      EVPR2           *JUMP IF MORE TO PROCESS
        POP     HL              *REMOVE BASE ADDRESS OF RECORD FROM STACK
        RET
EVPR2   POP     DE
        INR     A
        PUSH     PSW
        PUSH    DE
        JP      EVPR1           *GO PROCESS NEXT ENTRY IN RECORD
*
* THE RESPONSE RECORD PROCESSOR OBTAINS THE
* RESPONSE TYPE FROM THE RECORD AND TRANSFERS CONTROL
* TO THE APPROPRIATE RESPONSE MODULE
* ON ENTRY A=RESPONSE RECORD INDEX
*
RESPRO  MOV     L,A
        MVI     H,ZERO           *HL=RESPONSE INDEX
        MOV     B,H
        MOV     C,L
        DAD     DE
        DAD     DE
        DAD     DE              *HL=RESPONSE INDEX*3
        XCHG
        LXI     HL,RESREC
        DAD     DE              *HL=RESPONSE RECORD ADDRESS
        MOV A,M                 *A=RESPONSE TYPE
        ADD     A
        INX     HL              *HL=ADDRESS OF NEXT DATA ITEM IN RECORD
        XCHG                    *DE=ADDRESS OF NEXT DATA ITEM IN RECORD
        MOV     C,A
        MVI     B,ZERO
        LXI     HL,RESTAB
        DAD     BC              *HL=TABLE ADDRESS
        MOV     C,HL
        INX
        MOV     B,HL            *BC=ADDRESS OF RESPONSE MODULE
        PUSH    BC
        XCHG
        INX     HL
        MOV     E,M
        RET                     *GO TO RESPONCE SUBPROCESSOR
RESTAB  DW      DIGOUT
        DW      APPL
        DW      DELINT
        DW      DELDAC
        DW      TODACT
        DW      TODDAC
*
* THE DIGITAL OUTPUT SUBPROCESSOR EXTRACTS
* THE PORT/MASK/AND DIRECTIVE INFORMATION FROM
* THE INDICATED RECORD AND OUTPUTS THE NEW VALUE
* DE CONTAINS THE RECORD INDEX
*
DIGOUT  LXI     HL,DIGREC       *SET DIGITAL OUTPUT RECORD ADDRESS
        DAD     DE
        DAD     DE
        DAD     DE              *HL=OUTPUT RECORD ADDRESS
        PUSH    HL              *SAVE OUTPUT RECORD ADDRESS
        MOV     A,M             *A=PORT
        DCR     A
        MOV     C,A
        MVI     B,ZERO
        LXI     HL,OPORT        *HL=OUTPUT PORT BASE ADDRESS
        DAD     BC              *HL=ADDRESS OF PORT DATA
        MOV     A,M             *A=OUTPUT PORT CURRENT STATE
        POP     HL
        INX     HL              *HL=MASK ADDRESS
```

This time it determines that the response required from record 1 is to call the application module located at hexadecimal address 2C0F. This information is transmitted to APPL (the application task initiator subprocessor) by the response processor, which transfers control. In our particular example this application module will cause the display panel to flash the location of the sensor giving the alarm. Upon completion of this function the application module returns control to the event record processor.

Next, the event record processor transfers the index of response record 2 to the response processor. Recognizing that a digital output is to be initiated, the processor extracts the index of DIRREC (the digital output record), 0 in this example, and initiates DIGOUT (the digital output subprocessor).

The function of this subprocessor is to activate the audible alarm. A 3 byte record is used to effect the actual output:

Digital Output Record

Byte 0 = output port;
Byte 1 = bit isolation mask;
Byte 2 = 0 for reset (off); 1 for set (on).

In our case let's assume that the audible alarm has been connected to bit 5 on output port 3 and must be set to a logic 1 to sound the alarm. This requires a digital output record as follows:

Audible Alarm Output Record

Byte 0 = 3;
Byte 1 = 20;
Byte 2 = 1.

Using this information bit 5 on output port 3 is set and the alarm horn is turned on. Processing this final response causes the event processor to return to the digital scan module, which will continue monitoring the state of all the digital inputs.

The intent of this example is to show how the system works when attached to the real world. While this example does not cover all the functions one might associate with a smoke or fire alarm, it does serve to illustrate how the various tables are structured. What you can do with such a system is limited only by your imagination. As stated earlier in this series, the system can be structured to perform many of the discrete tasks associated with the control and monitoring of the home or office, as well as protecting your property against intruders. So let your imagination take command and have fun. Next month: musical toys.■

Listing 1, continued:

```
         ANA      M
         PUSH     PSW               *SAVE MASKED STATE
         INX      HL
         MOV      A,M               *GET SET/RESET DIRECTIVE
         DCX      HL
         CPI      ONE
         JZ       DIGSET            *GO TO SET FUNCTION
         POP      BC                *B=NEW OUTPUT STATE
DIGOU1   DCX      HL                *HL=PORT ADDRESS
         MOV      A,M               *A=OUTPUT PORT
         STA      DIGOUT2+1         *SAVE PORT NUMBER IN OUTPUT INSTRUCTION
         MOV      A,B               A=OUPUT DATA
DIGOU2   OUT      THREE
         MOV      C,M               *C=PORT
         MOV      B,ZERO
         LXI      HL,OPORT
         DAD      BC
         MOV      M,A               *SAVE NEW STATE IN MEMORY
         RET
DIGSET   MOV      A,M               *A=MASK
         CMA
         POP      BC                *C=MASKED VALUE
         ORA      B                 *A=NEW OUTPUT STATE
         MOV      B,A
         JP       DIGOUT1
*
* VECTORS TO APPLICATION TASK
* DE CONTAINS MODULE ADDRESS
*
APPL     PUSH     DE                *SAVE ADDRESS ON STACK
         RET                        *EXIT TO APPLICATION MODULE
*
* DELINT ACTIVATES THE DELAY RECORD WHOSE
* RECORD INDEX IS IN DE
*
DELINT   LXI      HL,DELREC         *SET BASE ADDRESS
         DAD      DE
         DAD      DE
         DAD      DE
         DAD      DE
         DAD      DE
         DAD      DE                *HL=DELAY RECORD ADDRESS
         MOV      A,M               *GET ACTIVE FLAG
         ANI      80H               *IS ACTIVE FLAG RESET ,ACTIVE<
         RZ                         *RETURN IF RECORD IS ACTIVE %RESET<
         INX      HL
         INX      HL                *HL=TIMER ACTIVATION VALUE
         MOV      A,M               *A=TIMER VALUE
         DCX      HL
         DCX      HL
         MOV      M,A               *SET VALUE IN RECORD
         RET
*
* DELDAC DEACTIVATES THE DELAY RECORD
* WHOSE INDEX IS N DE
*
DELDAC   LXI      HL,DELRES         *SET BASE ADDRESS
         DAD      DE
         DAD      DE
         DAD      DE
         DAD      DE
         DAD      DE
         DAD      DE
         MVI      A,ZERO
         MOV      M,A               *RESET ACTIVE FLAG
         RET
*
* TODACT ACTIVATES THE TOD RECORD
* WHOSE RECORD INDEX IS IN DE
*
TODACT   LXI      HL,TODREC         *SET BASE ADDRESS
         DAD      DE
         DAD      DE
         DAD      DE
         DAD      DE
         DAD      DE
         MVI      A,7FH             *ACTIVATION MASK
         ANA      M                 *SET RECORD ACTIVE
         MOV      M,A
         RET
TODDAC   LXI      HL,TODREC         *SET BASE ADDRESS
         DAD      DE
         DAD      DE
         DAD      DE
         DAD      DE
         MVI      A,80H             *DEACTIVATION MASK
         ORA      M                 *SET RECORD INACTIVE
         MOV      M,A
         RET
```

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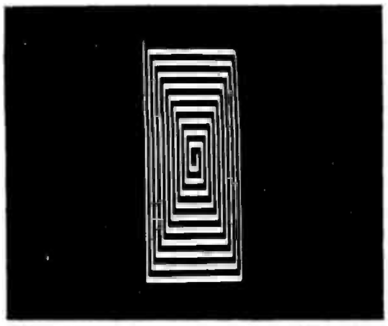

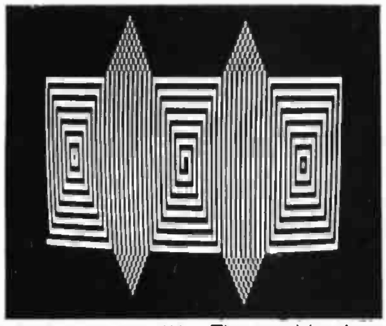

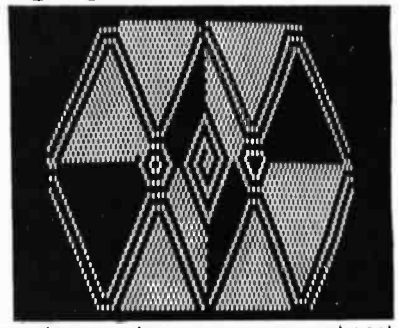

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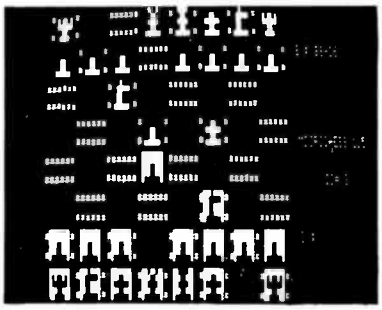

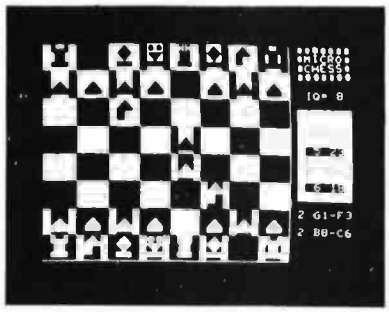

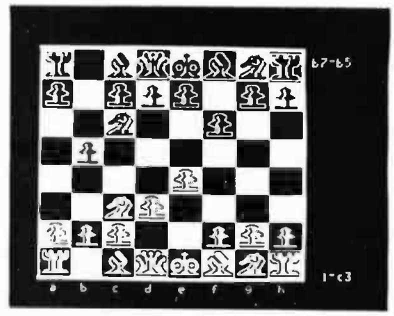

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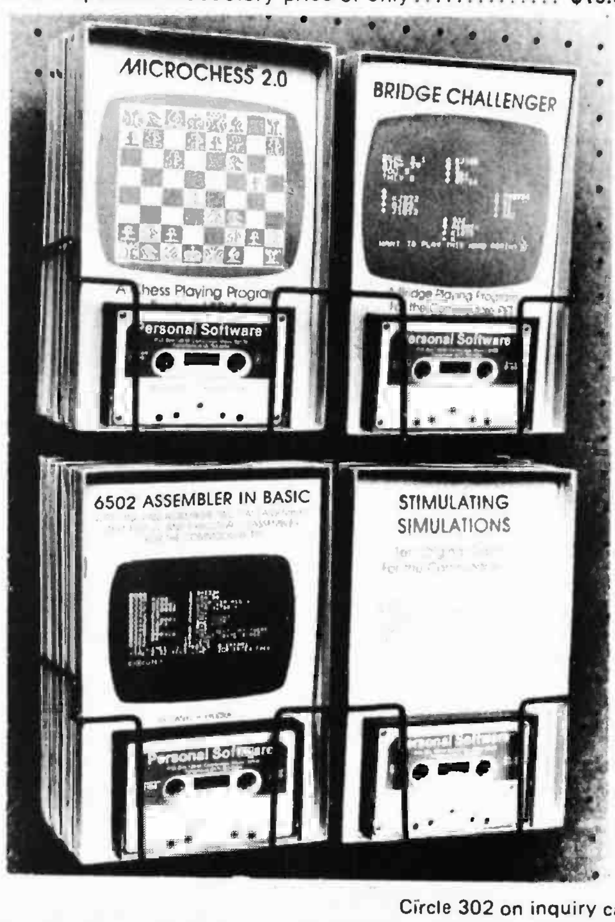

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Common Mistakes Using Warnier-Orr Diagrams

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Langston Kitch and Associates
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Topeka KS 66607

Editorial Note. . .

Since publishing David Higgins' first two articles on Warnier-Orr diagramming techniques, we have received a number of letters from people expressing the message (paraphrased) "if I have this or that self-documenting structured programming language, why should I use Warnier-Orr techniques? After all, if a program in my language is logically equivalent to the Warnier-Orr structure, and it is directly executable, I see no need for an extra layer of documentation."

A very real answer to this objection is that it is correct. There is no point to using Warnier-Orr techniques if you properly use a language such as PASCAL which, having structured programming constructs built in, allows long descriptive names for variables and procedures, and as a result can support self-documenting code.

But most currently used languages in personal computing do not easily support self-documenting code and modern concepts of structured programming. The usefulness of the Warnier-Orr methodology is that it provides a disciplined way of imposing such structure on a language such as BASIC, FORTRAN or assembly language. In effect, the Warnier-Orr discipline is a programming language which is intended for hand translation into one of the existing unstructured languages. . . CH

In my opinion, one of the best program and system design methods is the Warnier-Orr structured systems design approach, which I described previously ("Structured Program Design," page 146, October 1977 BYTE; "Structured Programming with Warnier-Orr Diagrams," page 104, December 1977 and page 122, January 1978 BYTE). This article is being presented because of the interest expressed in this subject, and because a lot of people will be trying these techniques for the first time. Newcomers to this methodology often have many questions about their work, and want to know whether or not what they are doing is correct. The purpose of this article is to outline a few of the more common mistakes that beginners make when using this technique.

Philosophical Errors

Many first time users of the Warnier-Orr diagrams tend to make mistakes which are so similar that they are worth examining. The biggest and most common mistakes tend to be a direct result of what we can call philosophical errors; not really a misuse of the techniques so much as a misunderstanding of the techniques. The most common error stems from the fact that many computer programmers tend to be obsessed with the desire to write some kind of code at the very beginning of the design process. This problem usually manifests itself in any or all of the following three ways:

- Trying to code the program while designing it (called the design-a-little, code-a-little approach).
- Relying too heavily on language restrictions and considerations while doing logical design.
- Skipping the design phase altogether because:
  - a) the program is "too easy" or
  - b) the programmer is "too smart."

Any of the above practices will destroy most if not all of the effectiveness of the Warnier-Orr methodology *[or any other structured programming methodology for that matter. . . CH]*. It will certainly cause you to waste a great deal of time.

If you try to use the first technique, the design-a-little, code-a-little approach, you will probably be in for quite a bit of erasing or retyping when you have to change the design because you coded yourself into a corner that you can't design your way out of. Your program will tend to be twice as long as it should have been and half as efficient. You will probably be in for a lot of debugging runs while trying to put back into the code everything that you left out when you changed the design. As you can see, this technique just naturally generates problems.

The second technique described above is a common mistake that veteran programmers almost always seem to make: relying too heavily on the program language they will be using while doing the program design. Consider the two examples of program

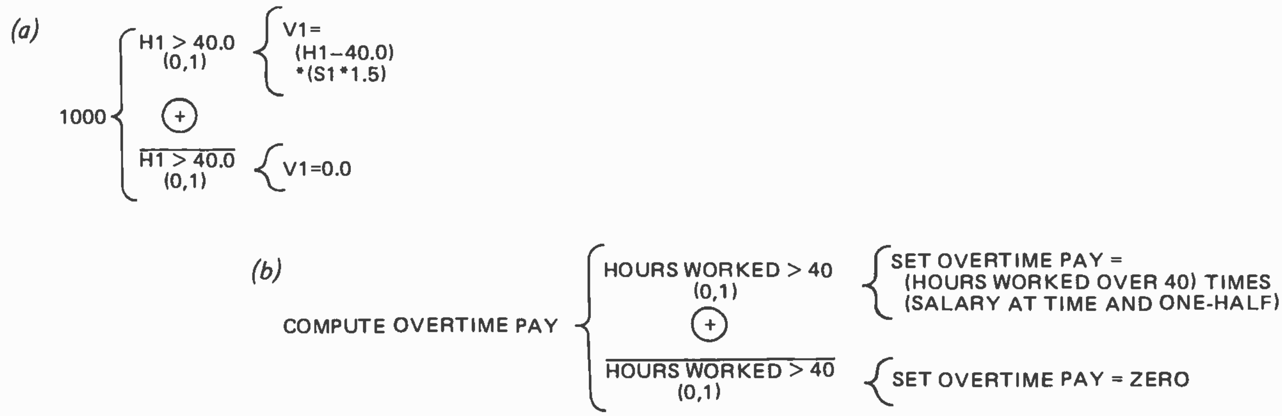

Figure 1: DOs and DON'Ts of Warnier-Orr diagramming. Figure 1a looks like actual program code and should not be used when trying to logically design a program. Figure 1b shows the correct method. The entire diagram contains only logical statements which could be coded into any computer language.

designs shown in figure 1. Both figures 1a and 1b are diagrams of the same process: computation of overtime wages. The diagram in figure 1a however seems to be the type that veteran programmers will almost always try to draw. Note its heavy stress on the language aspect of the function. It almost looks like part of a BASIC program cut out and pasted on a diagram. Contrast that diagram with the one of figure 1b which correctly details the logical process being performed. You can see that if figure 1a was the only documentation for this particular procedure, you would probably not be able to tell what that piece of code was supposed to be doing. You might have some idea because this program seems to have semimeaningful field names from which you might deduce some purpose. All we can tell for sure from figure 1a is that some part of the program is going to crunch a couple of numbers. What numbers it is going to crunch and just what for are anyone's guess. On the other hand, it is impossible to misunderstand what the process diagrammed in figure 1b is doing. It is very easy to read and comprehend because it shows the logical side of the procedure.

This stress of the logical over the physical while designing with the Warnier-Orr diagrams is essential to their correct usage. Designing as in figure 1a serves absolutely no purpose as far as understanding the process that is being described and is essentially worthless as far as documentation is concerned. Even though you might be able to tell what that diagram does the day you draw it, you probably won't be able to understand it in six months. Someone else who wants to use your documentation might never understand it.

As long as we're on the subject of documentation, I might mention that through the development period of this technique, many people were concerned that the diagrams might become too far removed from the actual code, which would render them useless as effective documentation. They worried that since the diagrams depicted the logical side of the problem, they had little or no relevance to the physical (real world) side. Those fears were easily put aside with two diagramming and coding conventions, as follows:

- Physical mileposts on the Warnier-Orr diagrams.
- Logical symbol tables in the programs.

Thus, when we actually wrote code that looked like that of figure 1a, we would tie it to the logical figure 1b by adding the following to the diagram.

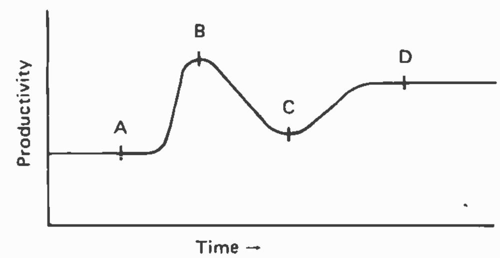

Figure 2: Typical productivity curve of programmer being introduced to Warnier-Orr diagram methodology.

This would be included in the program itself by using comment statements:

```
      .
      .
      .
1000 REM     COMPUTE OVERTIME PAY
1001 REM        HFLD      = HOURS WORKED
1002 REM        OVTFLD  = OVERTIME PAY
1003 REM        SALFLD   = SALARY
      .
      .
      .
```

This allows us to have a very clear and concise, one to one mapping between the logical diagram and the physical code. References between the two diagrams are quite easy. If, for instance, you want to know what a particular section of code is supposed to be doing, you need only to look it up on the logical diagram. Similarly, if you want to find out which part of the program is carrying out a particular logical function, you have the location information at your fingertips. This is excellent documentation in the event that you or someone else might someday want to make a modification to your code.

The third common philosophical error, that of skipping the design phase altogether, is a real problem to most newcomers. In fact, if you look at a typical productivity curve for a programmer who is introduced to the Warnier-Orr diagrams, it generally looks something like the curve in figure 2.

A currently productive programmer producing work at a constant rate up until the time the Warnier-Orr techniques are introduced (point A), will typically show an initial burst of very high productivity (point B). This is usually followed by a slump (point C) where the programmer sinks back to or just above his previous level of work. Eventually, he will climb back up to a new, higher level of work (point D), where he will usually stay. This peculiar slump at point C seems to be primarily due to the fact that since the programmer has begun to feel comfortable with the new technique and has had some initial success with it, he begins to feel confident enough to try to do the work without doing the diagrams first. He soon realizes that the quality of his work has dropped off and starts to do the diagrams once again, this time for good, and his work level rises up to a new, higher level that will remain fairly constant.

Apparently, the only way to get new people to avoid this temptation is to forewarn them that it does tend to happen, so that if and when they find themselves on the downhill side of the productivity curve, they can recognize the trap in time to escape the worst of it.

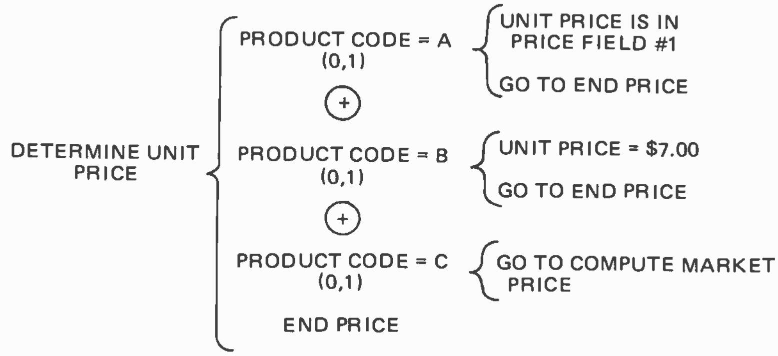

Figure 3: Example case statements making use of logically illegal GOTO statements. When a set of statements is finished the diagram will logically fall through all of the other exclusive ORs, ⊕, and arrive at the END PRICE section. Thus no GOTO need be shown.

So much for the philosophical errors. There are also a few common technical errors that people make, and we'll look at those next.

Technical Errors

For a lot of people who are just starting to program and may be unfamiliar with structured programming techniques, some of the diagramming methods may seem to be a bit uncomfortable. One of the most often seen technical errors is the attempted use of a GOTO statement on the diagram. The case statement shown in figure 3 illustrates this problem.

Two of the occurrences of the GOTOs in figure 3 are incorrect and the other is ambiguous. The GOTOs in "PRODUCT CODE = A" and in "PRODUCT CODE = B" are unnecessary and incorrect. The default logical linkages will see to it that the appropriate steps are executed. The GOTO at "PRODUCT CODE = C" is unclear. If it is supposed to mean that we are to cease execution of this process and jump to the procedure "COMPUTE MARKET PRICE" to begin processing, then its usage is incorrect. If on the other hand it means that "COMPUTE MARKET PRICE" is a common utility routine and is described elsewhere in the system, then the GOTO is misleading. Instead, we should have written:

```
PRODUCT CODE = C   { COMPUTE MARKET PRICE
      (0,1)        {                    . . . SEE PAGE #3,
```

if the process was expanded on a different page of the diagram; or something like the words ". . .SEE ABOVE" or ". . .SEE BELOW" if that process appears elsewhere on the same page. The GOTO is a physical entity to be used at execution and is not a logical relationship, so it does not belong on

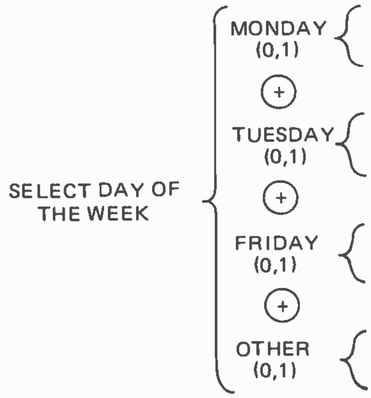

Figure 4: Example of a case statement with processes that are mutually exclusive and mutually independent.

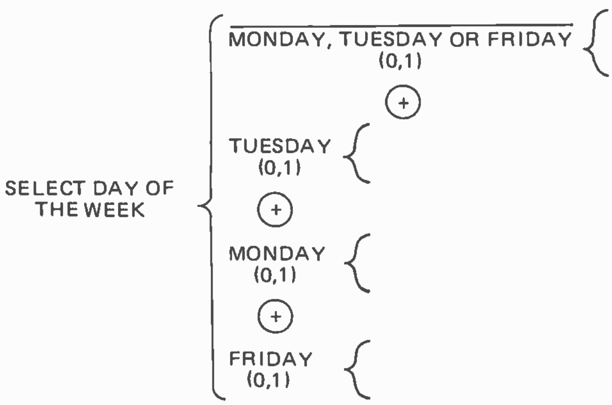

Figure 5: When a case statement has mutually independent and mutually exclusive statements, the statements may be rearranged into any order without changing the logic of the diagram.

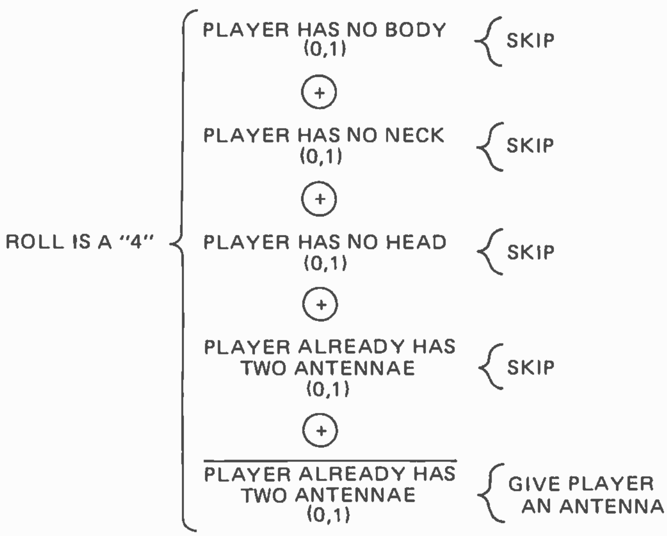

Figure 6: Although this is a working Warnier-Orr diagram, the case statements are not mutually independent.

```
IF 'player has no body'
   THEN . . .
ELSE IF 'player has no neck'
   THEN . . .
ELSE IF 'player has no head'
   THEN . . .
ELSE IF 'player has two antennae'
   THEN . . .
ELSE 'give player one antenna'
```

Listing 1: Typical if-then-else structure for Warnier-Orr diagram of figure 6.

a logical Warnier-Orr diagram.

Another common technical mistake is one that is a little harder to catch, and is one that even professionals with this technique will make if they aren't careful. Consider the case statement shown in figure 4.

Note that in this case statement, not only are the processes outlined mutually exclusive (only one of the cases is true), but they are also mutually independent. That is, their order within the case statement does not matter. It would be just as correct for me to have written the diagram as shown in figure 5.

In an earlier article "Structured Program Design" (Oct 77 BYTE), the game of BUG was outlined. In the game, a die is rolled for each player and each number of the die corresponds to a part of the bug's body; the player finishing his bug first wins the game. If a player rolls a 4 for instance, he is entitled to one antenna. But he must have already acquired a body, a neck and a head in that order before he can receive an antenna. He needs a total of two antennae if he is to complete a bug.

Many people would try to code that process as a case statement as in figure 6. The process in figure 6 certainly looks correct, and indeed, if you code it as a case statement, as in listing 1, it will even run correctly.

However, this process is not a case statement. It is more properly called a pseudo-case statement, because each of its cases is mutually dependent. The cases cannot be reordered within the statement without destroying its logic. Notice that rearrangement of the case statement diagram as shown in figure 7 does not work at all. This arrangement will give the player an antenna anytime a four is rolled, until he has two antennae, regardless of whether or not he already has a body, a neck or a head. A more correct logical interpretation of the case structure we want is shown in figure 8.

You might also notice that since the bug must have a body before it can have a neck (and a neck before it can have a head) if we

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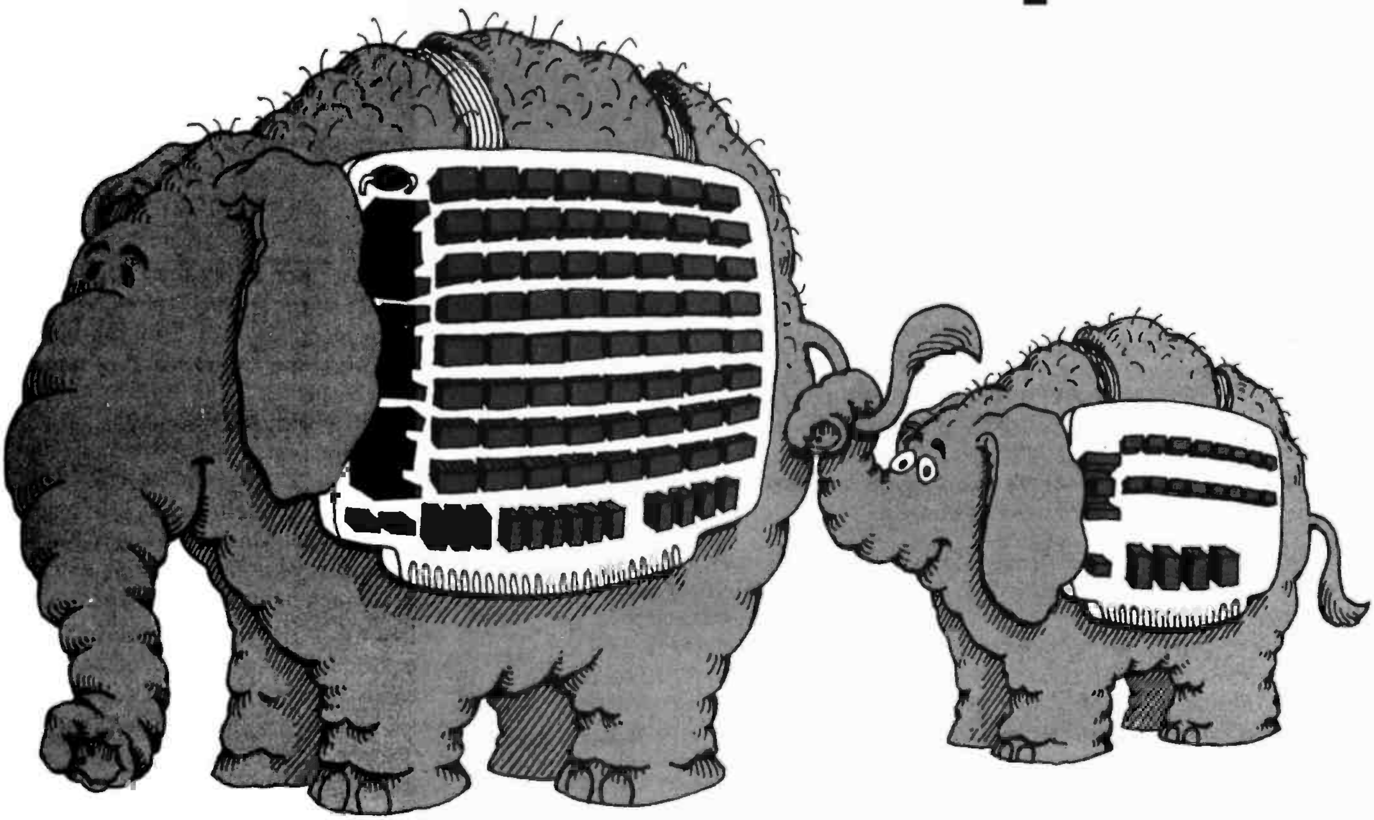

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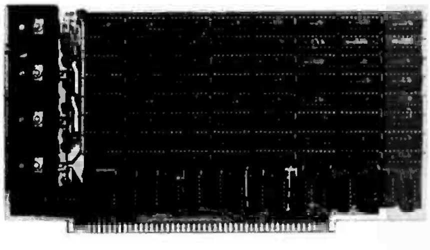

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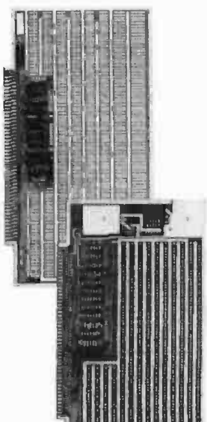

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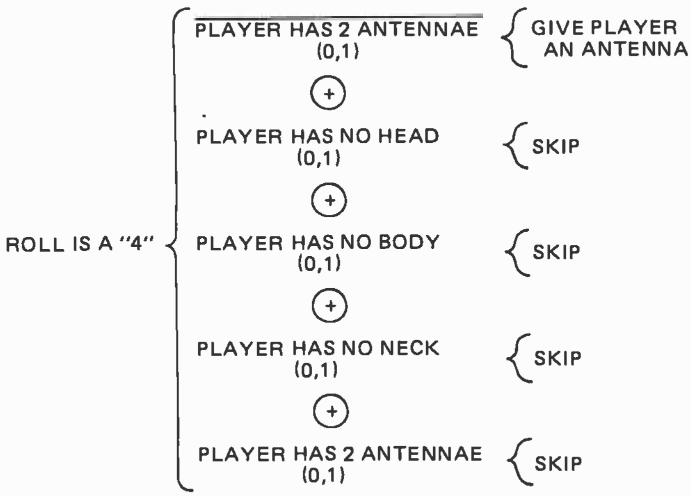
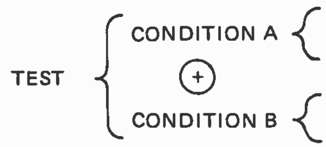


Figure 7: When the statements in figure 6 are rearranged as shown, it can be seen that the program fails to work as desired.

merely check for the presence of the head, we will be indirectly checking for the neck and the body, so that figure 9 is an equivalent structure.

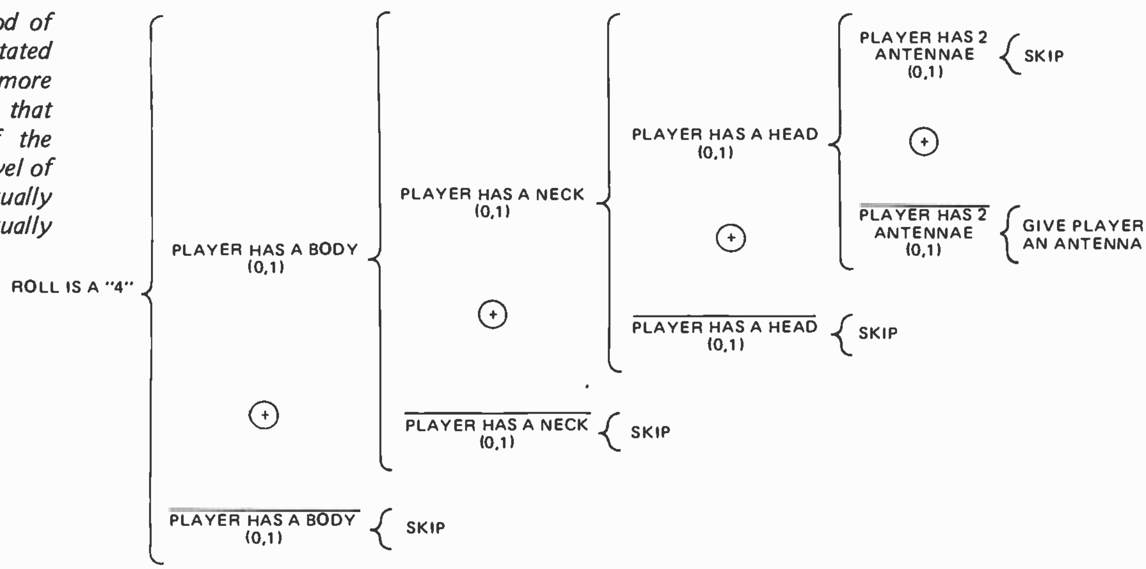
Another common technical error is the misuse or lack of use of the (0,1) notation in conjunction with the exclusive OR, ⊕. Many times, people will simply write:



By this they often imply the (0,1) notation with the use of the symbol ⊕ alone. Actually, this is not incorrect; in fact, for most people familiar with the diagrams, this notation seems to be just as clear. But for users not quite familiar with the Warnier-Orr diagrams it is probably best to go ahead and include the (0,1).

To conclude, I'll reiterate a point made in an earlier article: Understanding a Warnier-Orr diagram is very easy; creating one from scratch is much harder than it looks.■

Figure 8: This method of approaching the stated "bug" problem is more logically correct than that of figure 6. All of the statements at each level of the diagram are mutually exclusive and mutually independent.



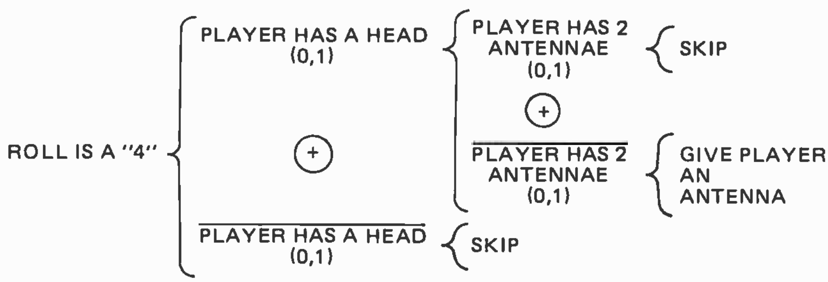


Figure 9: Since a bug must have a head in order to have an antenna, and a body and neck to have a head, the search process can be shortened by just checking for the presence of a head.

Solution to Machine Language Puzzler

(See page 92)

The waveforms shown in figure 1 depict the voltage waveform being applied to the speaker from the least significant bit of port 0 for each case.

When the outer loop constant (in A) is decremented to 00, the accumulator is reinitialized with #X. If X is even, only an imperceptible discontinuity in the waveform results owing to the execution time of 2 more instructions. If #X is odd, however, the waveform contains *one extra* half cycle, and a blip is heard. Every time A is reinitialized with an odd X, the waveform phase is changed by 180°.■

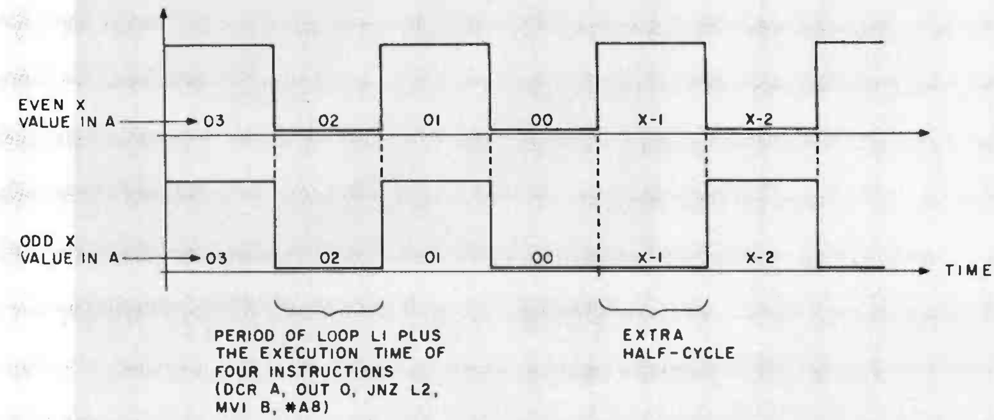


Figure 1: Voltage waveform appearing at the least significant bit (LSB) of port 0 for each case in the problem.

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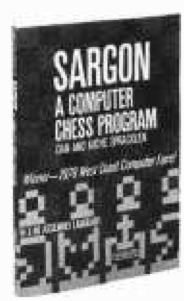

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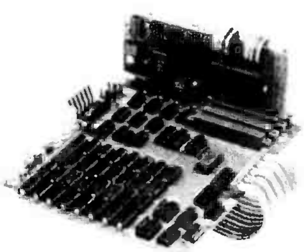

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Technical Forum

A Search for Vector Graphics

Mitchell Gilberg
c/o Coles, POB 610
Natchez MS 39120

I am a subscriber and avid reader of BYTE, and I have a problem I hope you can help me solve. I am trying to find some information on a particular type of video graphic display and whether it is currently available on any personal computers. Unfortunately, I don't know a technical name, so I'll have to attempt a cumbersome nontechnical description. What I want is to be able to draw one dimensional lines between defined endpoints, and to move the lines continuously across the screen.

Let me give you an example. Suppose an application I want to display is an aircraft instrument panel. The altimeter might look something as shown in figure 1. With the relatively common raster scan grid the altimeter would look as shown in figure 2.

One problem here is that in order to have enough detail to read the instruments, they would have to be too big to get an entire instrument panel on the screen. Another is that "lines" are not continuous. They are approximations that frequently lose their original shape when rotated between horizontal and vertical. Also, small displacements are lost if they aren't large enough to cause a quantum jump between plot grid points.

With high density noncolor graphics, you gain the ability to create a more detailed drawing, but motion becomes impractical. To show increasing altitude on the altimeter above, you must calculate a new location for each point on the rotating indicator and set and reset the corresponding bits in memory. That might represent several hundred calculations for each degree of rotation. Also, the indicator will not move as a unit. That is, it "warps" point by point, as shown in figure 3.

Figure 3.

In the past, I have used a Tektronix 4010 storage tube. This particular device allows plotting graphics as lines between endpoints. That is, your program specifies a starting and ending point for a line segment, and you can then "draw" a line between the points. So, for rotation of the altimeter, you need only calculate the positions of three points, and connect them with line segments. The line segments are always continuous, never warped. However, the Tektronix stores the line until the entire screen is erased, so you can draw detailed diagrams although true motion is impossible. You must erase the entire screen and redraw it at the new position—a process which takes several seconds for complex diagrams.

Let me now try to describe what I need. The display must be able to define lines as the Tektronix does, so that line movements are done by simply recalculating the endpoint locations. But, it must also allow for moving the line without having to recreate the entire drawing— or, if it must recreate the entire drawing, it must recreate it fast enough so that you don't see an erase and redraw action. (I have seen this type of display in only two places, both of which were in 25 cent video arcade games, and both of which were a Space War game. The games were similar in that they both showed spaceships which moved continuously through space, able to turn through any angle.)

If you or any of your readers can tell me who makes this type of display, or how it works, or if it's even feasible to do with personal computers that are available today, I would certainly appreciate it.■

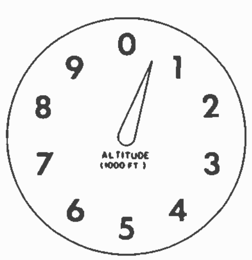

Figure 1.

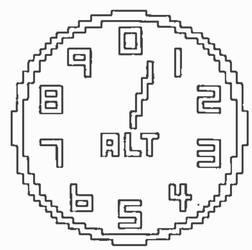

Figure 2.

We cannot help specifically in this reply, but can point you in the right direction: you are looking for a vector *display, where an XY oscilloscope with blanking is driven from a list of XYZ coordinate triples. (The Z* axis *simply indicates an intensity for the line of 0 or 1.) An example of this was found in Steve Ciarcia's article, "Make Your Next Peripheral a Real Eye Opener," (November 1976 BYTE, page 78). Steve's design is not, to our knowledge, currently being manufactured, so you will have to build it yourself. . . .*CH

Technical Forum

Filling 6800 Op Code Holes

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Table 1: A table of "holes" in the 6800 op code space. Analyzing the holes involves tabulating the effect of each instruction on the condition code register, computing the number of machine cycles for each instruction, and most importantly, finding suitable applications for these instructions.

Instruction Length	Hex Code	Label	Commentary
1	00	NOP	
1	02	NOP	
1	03	NOP	
1	04	NOP	
1	05	NOP	
1	12	SBA-1	A←A – (B+1).
1	13	SBA-1	Same as 12.
1	14	NBA	A←A AND B
1	15	NOP	
1	18	DAA	No effect on carry bit?
1	1A	ABA	No effect on carry bit.
1	1C	ABA+1	A←A + (B+1). No effect on carry or half-carry bits.
1	1D	ABA	A←A + B. No effect on half-carry bit.
1	1E	TBA	Same as 17.
1	1F	TBA	Same as 17, plus carry bit is set to 1.
2	21	BRA r	Same as 20.

When looking at a reference chart for the Motorola 6800 processor, one may notice many nonimplemented op codes. It is possible that these codes, when properly explored, can lead to interesting operations of the processor. I could not resist the challenge to do this and have spent many frustrating hours trying to understand the strange results obtained. By dint of perserverance, I eventually worked my way through every one, producing table 1. I have not yet made a study of the complete effect of each operation on the condition code register, although some were obvious along the way.

It is interesting to note that four of the op codes (hexadecimal 87, 8F, C7 and CF) actually modify the program, conveniently skipping one program step in the process. This jumped over step could contain a branch or jump instruction, so that if the modified part of the program is immediately followed by a branch back to the skipped over instruction we would have the possibility of an approximately 65,536-way branch, depending on the result of some calculation in either of the accumulators or the index register. Of course, any program using this self-modifying feature can only be implemented in programmable memory. Committing it to read only memory would automatically render it unchangeable.

Three codes (hexadecimal 3D, 9D and DD) cause the 6800 to continuously increment the address bus with both the valid memory address (VMA) and read write (RW) lines held high, but the microprocessor does not act on the instructions it reads along its route. Perhaps they can be used in the form of some direct memory access instruction with a hardware halt to the process by activating RESET.

It would be interesting to find out if all 6800s follow the patterns in my table, or if the results are specific to my individual unit. Remember, these instructions worked in my processor but may not necessarily work in yours. The best course of action is to use my table as a base and then double check your own processor.

REFERENCES

1. Jessop, Paul M, "The Motorola 6800 Instruction Set," January 1978 BYTE, page 84.
2. Wheeler, Gerry, "Undocumented M6800 Instructions," December 1977 BYTE, page 46.

Table 1, continued:

1	38	RTS	Same as 39 followed by 34; ie: RTS followed by reset of stack pointer to original setting plus 1.
1	3A	RTI	Same as 3B followed by 34s; ie: RTI followed by reset of stack pointer to original setting plus 1.
1	3D	DMA	Program counter continuously increments address bus. VMA and RW lines go high.
1	41	CPZ A	Compare register A with zero. Leaves register A unchanged, but sets NZVC according to result of the compare with zero.
1	42	COM A	Same as 43.
1	45	CPY A	Copies least significant bit of register A into carry bit. Leaves register A unchanged. Sets overflow bit (V) according to $V=N\bar{C} + \bar{N}C$. Sets zero bit (Z) if either register A or B is zero. Could be used (by following with BCS) to branch on register A equal to an odd number.
1	4A	DEC A	Same as 4A.
1	4E	NOP	
1	51	CPZ B	Compare register B with zero. Similar to 41 above.
1	52	COM B	Same as 53.
1	55	CPY B	Copies least significant bit of register B into carry bit. Leaves register B unchanged. Remarks similar to 45 above.
1	5B	DEC B	Same as 5A.
1	5E	NOP	
2	61	NEG X	Same as 60.
2	62	COM X	Same as 63.
2	65	LSR X	Same as 64.
2	6B	DEC X	Same as 6A.
3	71	NEG e	Same as 70.
3	72	COM e	Same as 73.
3	75	LSR e	Same as 74.
3	7B	DEC e	Same as 7A.
2	83	SB1 A#	A←(A) — (immediate+1).
1	87	ST2 A	PC+2←(A). Stores contents of register A at current program counter plus two and advances to program counter plus 3.
1	8F	ST2 S	PC+2, PC+3←SP. Stores current value of stack pointer at program counter plus two and three and advances to program counter plus four.
2	93	SB1 A d	A←(A) — [(memory direct)+1]. Adds one to contents of referenced memory, subtracts result from register A and stores result of subtraction in register A. Leaves memory contents unchanged.
1	9D	DMA	Same as 3D above.
2	A3	SB1 A X	A←(A) — [(memory indexed)+1]. Similar to 93 above.
3	B3	SB1 A e	A←(A) — [(memory extended)+1]. Similar to 93 above.
2	C3	SB1 B#	B←(B) — (immediate+1).
1	C7	ST2 B	PC+2←(B). Similar to 87 above.
3	CC	CPX #	Same as 8C.
2	CD	BSR r	Same as 8D.
1	CF	ST2 X	PC+2, PC+3←IX. Stores current value of index at program counter plus two and three and advances to program counter plus four.
2	D3	SB1 B d	B←(B) — [(memory direct)+1]. Similar to 93 above.
2	DC	CPX d	Same as 9C.
1	DD	DMA	Same as 3D above.
2	E3	SB1 B X	B←(B) — [(memory indexed)+1]. Similar to 93 above.
2	EC	CPX X	Same as AC.
2	ED	JSR X	Same as AD.
3	F3	SB1 B e	B←(B) — [(memory extended)+1]. Similar to 93 above.
3	FC	CPX e	Same as BC.
3	FD	JSR e	Same as BD. ■

Technical Forum

Let's Be PALs: Some Comments on BBC Teletext

R G Silson
Near Station
TRING
Herts HP23 5QX
ENGLAND

E John Dehaven (April 1978 BYTE, page 152) is a little out of date regarding British TV standards. In 1936 the world's first high definition television station started regular broadcasts from Alexandra Palace, London ENGLAND. The transmission used 405 lines with AM sound and synchronized to the 50 Hz power lines. After the war the system was extended to cover the whole country on VHF.

With the introduction of color, a new UHF network was set up which now has around 1000 transmitters. The color system uses a 625 line phase alternation line (PAL) system with FM sound. *[In the PAL color system, the subcarrier derived from the color burst is phase inverted from one line to the next to minimize possible transmission hue errors. . .CM]* No new 405 sets have been available for many years. Official policy has been to delete the 405 line system as soon as practical since all channels are duplicated on UHF. The problem is that many small communities in hilly areas find UHF reception very poor and a local UHF transmitter is not always economic.

In Britain the whole 50 Hz power system is synchronized by high voltage links, but transmitters are no longer tied to it. This change is perhaps unfortunate since some sets show a moving band, at the difference frequency, up or down the screen. This is usually faint but noticeable to the critical.

There is no need to modify the latest British color sets. They include high quality video display unit facilities to receive the new Teletext transmissions. All 625 channels now transmit digital data on unused picture lines giving up to 800 pages on each channel (more with special arrangements as below). A standard format of 24 lines, each with 40 characters, is used, with odd parity 8 bit bytes for each character. Each page is numbered (100 to 899) and the whole series is transmitted in sequence each 15 seconds or so. Some pages (eg: page 100) give general or special indexes to other pages which carry all kinds of information from news to recipes, sports to weather maps, etc. A digital

Circle 231 on inquiry card.

clock is given on the top line of each page, exact to the second.

A small key pad is provided. Keying a page number selects that page from the stream and stores it in the set for display as required. Normally only one page is stored but this is limited by economics alone. Storage may be for seconds or weeks if necessary. Extra pages above the basic 800 are obtained by using sets of pages with the same page number, and cycling them over several minutes, or even once per day. The keypad has extra buttons that permit normal picture display, Teletext display and combined display. It also has clock time setting switches that allow a page to be selected at a given time and stored to be displayed at leisure.

To use the set as a personal video display unit, one merely needs to input serial bytes in the published standard Teletext format via a spare channel. Superb facilities are available, all controlled by the data. Characters are of a high standard since they are generated as video signals by the Teletext unit with an equivalent bandwidth of about 14 MHz. The whole ISO-7 ASCII set is available with upper and lower case. Additionally, there are 64 graphics characters (permitting maps and other displays). These are in a 3 by 2 rectangle using one of six bits to give all possible on or off combinations. A duplicate upper case permits legends within the graphics.

The Teletext unit has direct control of the three color guns, permitting all characters to be displayed as black, white, red, green, yellow, blue, magenta or cyan in almost any combination, against a background of a chosen color. Any or all of the characters may be flashed on and off to attract attention.

A special control character may be used to open and close a box in the normal picture. The box may be of any size or shape and in any position on the screen. This facility is normally used for subtitles and news flashes, but could allow part of the screen access to the personal computer while the family watches a normal program on the rest of it. The store is continually updated by incoming new or repeat data but, if required, the whole page may be erased before a new page is started.

Overall, this set seems to have a high potential of usefulness. This may increase in the future since several control characters are still spare. In Britain this video display unit is also being standardized for telephone data so that all possible digital information services may use the household television, giving a minimum total cost. One wonders what the limit is going to be. ■

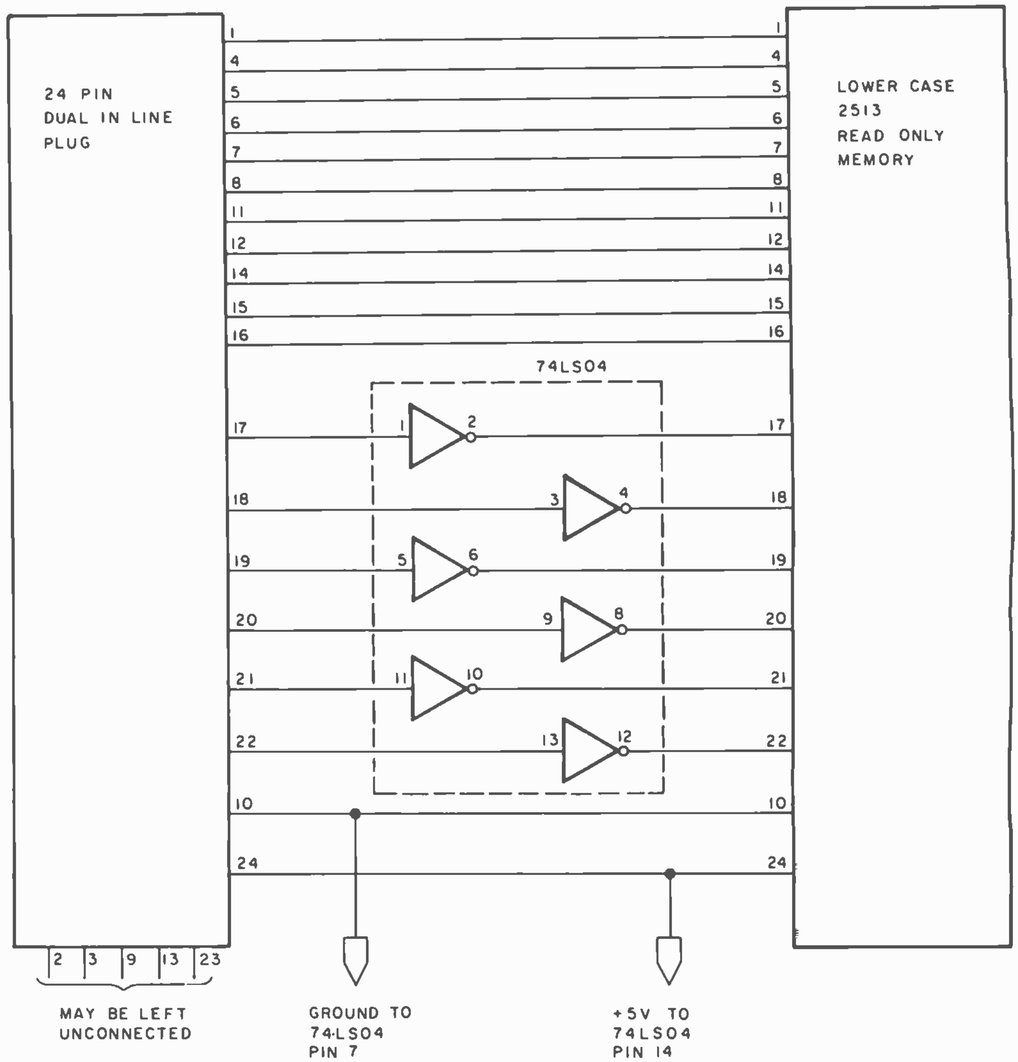
Adding Lowercase Display to the ADM-3A

A W Walker
1914 Ridgewood Dr
San Diego CA 92139

The scenario: you wanted a good quality, versatile video display, so you stretched the budget to the limit to buy a "dumb" terminal kit. After it's all together, you're showing off the result of your assembly skills when someone innocently asks "Does it have lowercase?" Well no, it doesn't, actually. You ask around, and find there is a way, but at $89, the kit from Lear Siegler doesn't quite fit the constraints. So a short expedition into the innards of the ADM-3A should be helpful; after all, one should only need a bit more of a character generator read only memory to do the trick. Lo and behold, the designers at Lear Siegler have even provided the socket, so let's see what fits into it. The ADM-3A maintenance manual explains nicely on page 6-11 that "the lowercase read only memory is a custom masked part" whose distinguishing attribute is that "all of the address lines. . . are inverted." Well, just how unusual is that custom read only memory? After some experimentation and further delving into the mysteries of the schematics, it appears that all one has to do is turn over the six character address bits, use a readily available lowercase 2513 for about $9.95 and be on the air. An easy way to invert six bits might be with a 74LS04 transistor-transistor logic (TTL) integrated circuit.

To avoid any modifications to the

Figure 1: Modifications that must be made to the existing ADM-3A to produce lower case characters.



ADM-3A, I built my lowercase adapter on a 24 pin dual-in-line plug that inserts into the existing lowercase read only memory socket (location L14) in the terminal. On top of the plug I mounted a small piece of 0.1 by 0.1 inch (0.254 by 0.254 cm) perforated board with sockets for the added lowercase 2513 and the 74LS04 inverter. Using this assembly method requires fairly careful consideration to avoid interference with the cabinet top or other components. For more compact assembly, the perforated board and sockets might be omitted with the new read only memory mounted directly on the plug and the inverter glued in place upside down on top. Since all but six of the read only memory's pins are connected directly to those of the plug, adequate support is available. The remaining six pins needing inversion can be bent out for appropriate connection to the 74LS04.

Regardless of the final mounting and installation method chosen, the required wiring is given in figure 1. Note that two additional 2102-1 memories are required, which plug into locations J11 and H11 to store the uppercase/lowercase data bit on characters stored in the display memory. The total cost of materials for my unit is $14.25, and it can be built for less depending upon your junkbox, where you shop for parts, and the method of construction.

Once installed in the ADM-3A, and assuming the UC DISP-U/L DISP at the inside rear of the unit is set to U/L DISP with the LC EN-UC switch at the left of the keyboard set at LC EN, the result is a full 95 character terminal display including the 26 lowercase letters and five additional symbols as shown in table 1. Note that, since the characters are still only generated with a 5 by 7 dot matrix, the lowercase letters with descenders, such as g, j, p, q and y, do not actually display the descenders below the writing line, but instead are elevated so as to allow the characters, including descenders, to be displayed within the 5 by 7 matrix. This technique results in a very acceptable low cost upper and lowercase display. My customized ADM-3A has been in service quite satisfactorily for more than eight months.■

Bits 4321 \ 765	110	111
0000	`	p
0001	a	q
0010	b	r
0011	c	s
0100	d	t
0101	e	u
0110	f	v
0111	g	w
1000	h	x
1001	i	y
1010	j	z
1011	k	{
1100	l	|
1101	m	}
1110	n	~
1111	o	DEL

Table 1: Additional characters added to the ADM-3A by the modification shown in figure 1.

Password Protection for Your Computer

R Jordan Kreindler
USC Eastern Regional Office
5510 Columbia Pike
Arlington VA 22204

Is your computer available via the telephone? Do you plan to leave it in a public area but want to limit its use? Will your system be used in a school environment where access must be controlled?

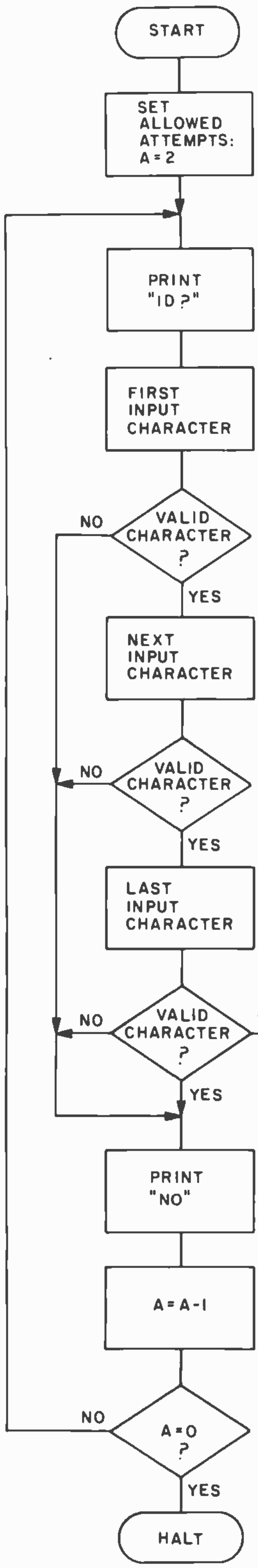
If the answer to any of the above questions is "yes," this article should interest you.

A Simple Password Procedure

One way to restrict system access is by lock and key. An easier method is to set up a password requirement. The flowchart in figure 1 is one way of implementing a password subroutine. This figure shows a simple method for checking a 3 character password. Each character of the password is checked immediately after it is entered. Upon detection of an illegal character, "NO" is printed. As shown, the user is allowed two attempts to enter the correct password. If both attempts fail, the system halts.

Number of characters in password	Number of possible passwords
3	46,656
4	1,679,616
5	60,466,176
6	2,176,782,336

Table 1: Possible password combinations using upper case letters and digits.



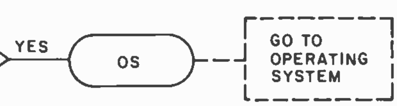


Figure 1: A simple password approach.

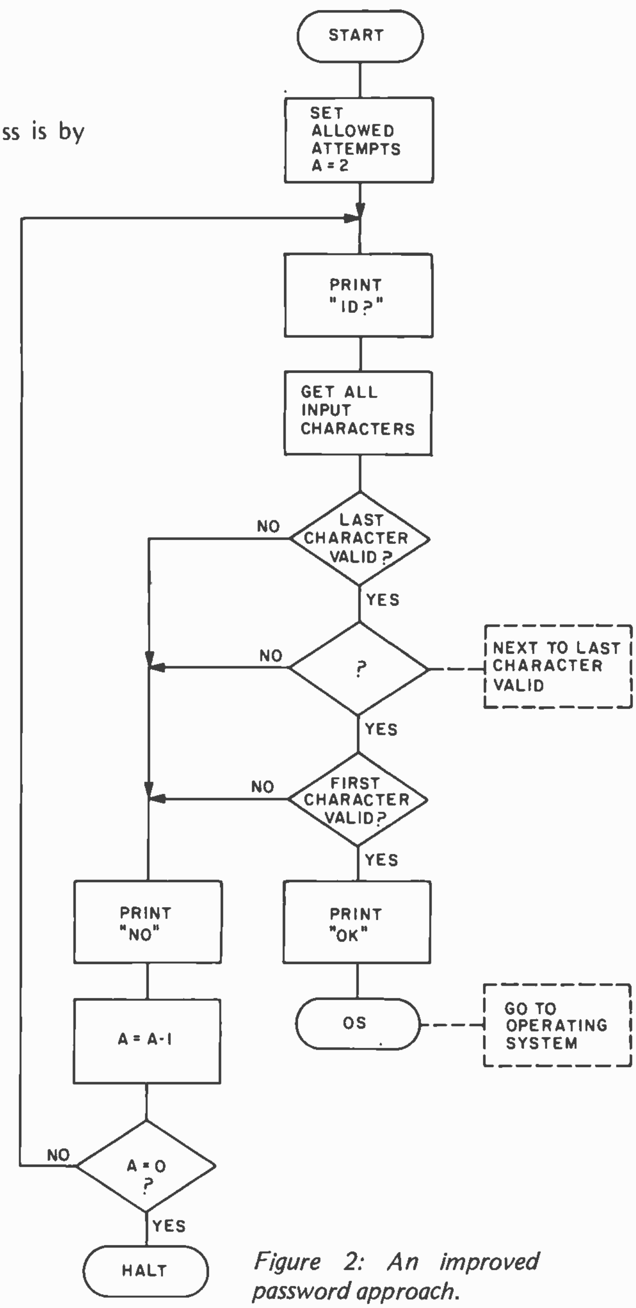


Figure 2: An improved password approach.

Assume that the 26 upper case letters and the 10 digits will be used to establish a password. For the algorithm in figure 1, a user could try, in order, all 36 characters to find the correct first character. After the first character is identified, the user could follow the same procedure to find the second character. Once the second character is found, the procedure could be repeated to find the third.

With this system, there are 36 + 36 + 36 = 108 different possible passwords. This is too few combinations for adequate security.

An Improved Password Procedure

A better procedure is shown in figure 2. Here, a 3 character password is also used. However, in this method all characters are entered before the password is checked. Thus, a failing password yields little information. The user can't tell which of the characters is incorrect. All that is known is that the combination tried was incorrect.

With this procedure, there are 36 X 36 X 36 = 46,656 possible passwords. This should be an acceptable level of security. If additional security is desired, the password can be expanded beyond three characters. Table 1 shows the number of different possible passwords in these situations. This table was developed with the assumption that only upper case letters and digits would be used in a password.

The program in listing 1 is an 8080/Z-80 coding of the algorithm in figure 2. The program as shown uses the password YES. It has been implemented on a North Star Horizon Computer. The following comments should allow this program to be modified for other systems (all numbers shown are in hexadecimal; DOS stands for disk operating system):

Statement	Comment
CALL 200D	Calls the DOS output routine. Outputs the character in the B register.
CALL 2900	Calls the DOS character input subroutine.
JMP 270F	Jumps to the DOS to allow normal system access.
MVI E, 53 MVI E, 45 MVI E, 59	Establishes the password as "YES." These three statements are where you establish your own password.

A password subroutine is easy to implement and requires little computer memory. However, it increases the security of your system.■

Listing 1: An 8080/Z-80 assembler listing of the improved algorithm for a 3 character password. This program is written for the password YES.

```
2969                    ;*****************************************
2969                    ;*                                       *
2969                    ;*     PROGRAM NAME :ID                  *
2969                    ;*     PROGRAMMER   :R. J. KREINDLER     *
2969                    ;*     DESCRIPTION  :THIS PROGRAM        *
2969                    ;*     ALLOWS THE USER TO ESTABLISH      *
2969                    ;*     A THREE CHARACTER ID(PASSWORD)    *
2969                    ;*     TO CONTROL SYSTEM ACCESS          *
2969                    ;*                                       *
2969                    ;*****************************************
2969                                         ;*
2969                    ;DEFINE STORAGE LOCATIONS FOR INPUT CHARS
2969                                         ;*
2969            LOC1:   EQU 29CCH
2969            LOC2:   EQU 29CDH
2969                                         ;*
2969                    ;ESTABLISH NUMBER OF TRYS
2969                                         ;*
2969 16 02      ID:     MVI  D,02H           ;SET ATTEMPTS TO TWO
296B 06 0D      IDETR:  MVI  B,0DH           ;PLACE "CR" IN B
296D CD 0D 20           CALL 200DH           ;PRINT "CR"
2970 06 0A              MVI  B,0AH           ;PLACE "LF" IN B
2972 CD 0D 20           CALL 200DH           ;PRINT "LF"
2975 06 49              MVI  B,49H           ;PLACE "I" IN B
2977 CD 0D 20           CALL 200DH           ;PRINT "I"
297A 06 44              MVI  B,44H           ;PLACE "D" IN B
297C CD 0D 20           CALL 200DH           ;PRINT "D"
297F 06 3F              MVI  B,3FH           ;PLACE "?" IN B
2981 CD 0D 20           CALL 200DH           ;PRINT "?"
2984 06 20              MVI  B,20H           ;PLACE " " IN B
2986 CD 0D 20           CALL 200DH           ;PRINT " "
2989                                         ;*
2989                    ;OBTAIN THE THREE INPUT CHARACTERS
2989                                         ;*
2989 CD 00 29           CALL 2900H           ;GET INPUT CHAR
298C 32 CC 29           STA  LOC1            ;STORE CHAR AT ADDRESS LOC1
298F CD 00 29           CALL 2900H           ;GET NEXT INPUT CHAR
2992 32 CD 29           STA LOC2             ;STORE IT AT LOC2
2995 CD 00 29           CALL 2900H           ;GET LAST INPUT CHAR
2998                                         ;LEAVE IT IN A
2998                    ;COMPARE INPUT TO VALID ID IN REVERSE ORDER
2998                                         ;*
2998 1E 53              MVI  E,53H           ;PLACE "S" IN E
299A BB                 CMP  E               ;COMPARE WITH LAST CHAR IN
299B C2 BD 29           JNZ TRYS             ;NO MATCH GO TO TRYS
299E 3A CD 29           LDA  LOC2            ;PLACE 2ND CHAR IN A
29A1 1E 45              MVI  E,45H           ;PLACE "E" IN E
29A3 BB                 CMP  E               ;COMPARE WITH 2ND INPUT CHAR
29A4 C2 BD 29           JNZ  TRYS            ;NO MATCH GO TO TRYS
29A7 3A CC 29           LDA  LOC1            ;PLACE 1ST INPUT CHAR IN A
29AA 1E 59              MVI  E,59H           ;PLACE "Y" IN E
29AC BB                 CMP  E               ;COMPARE WITH 1ST INPUT CHAR
29AD C2 BD 29           JNZ  TRYS            ;NO MATCH GO TO TRYS
29B0                                         ;*
29B0                    ;IF ID VALID PRINT "OK" & GIVE SYSTEM ACCESS
29B0                                         ;*
29B0 06 4F      OK:     MVI  B,4FH           ;PLACE "O" IN B
29B2 CD 0D 20           CALL 200DH           ;PRINT "O"
29B5 06 4B              MVI  B,4BH           ;PLACE "K" IN B
29B7 CD 0D 20           CALL 200DH           ;PRINT "K"
29BA C3 0F 27           JMP  270FH           ;GIVE ACCESS TO SYSTEM
29BD                                         ;*
29BD                    ;IF INPUT INVALID PRINT "NO"
29BD                                         ;*
29BD 06 4E      TRYS:   MVI  B,4EH           ;PLACE "N" IN B
29BF CD 0D 20           CALL 200DH           ;PRINT "N"
29C2 06 4F              MVI  B,4FH           ;PLACE "O" IN B
29C4 CD 0D 20           CALL 200DH           ;PRINT "O"
29C7                                         ;*
29C7                    ;TEST NUMBER OF INPUT TRYS
29C7                                         ;*
29C7 15                 DCR D                ;REDUCE D BY 1
29C8 C2 6B 29           JNZ  IDETR           ;IF D NOT 0 TRY AGAIN
29CB                                         ;*
29CB                    ;IF ALL ALLOWED TRYS FAIL THEN HALT
29CB                                         ;*
29CB 76         HALT:   HLT
*
```

The Power of the HP-67 Programmable Calculator, Part 1

Robert C Arp Jr
POB 1268
Minden NV 89423

Photo 1: The HP-67, one of the sophisticated pocket calculator products which represent the small end of the personal computing hardware range.

Introduction

This article is not a simple product review. Rather, it is the presentation of a complex programming example designed to illustrate the exploitation of a computing system composed of the HP-67 and its accessories, and worksheets that reduce the task of programming the *calculator* to a systematic exercise. The HP-67 is a pocket-sized version of the HP-97. The built-in thermal printer of the HP-97 is the major difference between the calculators. The HP-67 is shown in photo 1.

In addition to the HP-67, there are other sophisticated programmable calculators available at price levels which attracted consumers to the first scientific calculators in 1972 and the years following. I purchased my HP-35 early, and until the introduction of the HP-67 I considered it to be the finest calculator ever manufactured.

I must admit that I was intrigued by the features of the SR-52 when it was introduced. However, three of the Hewlett-Packard features force me to vote for the HP-67: choice of display format (fixed decimal, scientific and engineering; all with number of digits control), reverse Polish notation (RPN), and my previous experience with Hewlett-Packard. (Since 1972 I have experienced zero down time with the HP-35. Therefore, I am properly impressed with HP quality.)

Although I expect to see calculators with more memory capacity and some increase in programming capability in the future, I think the HP-67 represents a plateau of sophistication that will satisfy the needs of a large percentage of users. The HP-67 has 26 data storage registers, 224 steps of program memory (each step can hold as many as three keystrokes), unconditional and conditional branching, three levels of subroutines, four flags, 20 labels, indirect addressing, and, if that isn't enough, it accepts magnetic cards that record data or programs. In addition, each of the 35 keys control up to four separate operations, and, of course, it is completely portable with the rechargable battery pack.

Learning to Use the HP-67

Table 1 is a list of cautions which should be memorized before using the HP-67. These simple rules will allow maximum utility with minimum misery. After memorizing these rules, read Appendix B of the HP-67 handbook before attempting to use the calculator.

The HP-67 is a very powerful computer. One should not expect to memorize the *Owner's Handbook and Programming Guide* with a cursory reading. (The handbook is almost 3/4 inch thick.) Its contents should be digested in two stages: After acquiring your HP-67, read the handbook leisurely for two or three days, performing calculations when necessary. Next, design programs that require as many functions as possible, referring to the handbook often.

In addition to the *Owner's Handbook and Programming Guide*, the HP-67 is accompanied by a "Standard Pac" of programs which includes:

- 15 prerecorded magnetic cards containing programs for problems common to business, science and engineering, a diagnostic program and an abrasive cleaning card.
- 24 blank magnetic cards.
- *Standard Pac Handbook.*

The *Standard Pac Handbook* contains a description of each of the standard programs, instructions for running the programs, example problems, program listings and explanations of important programming techniques. As part of learning to use the HP-67, an owner should be sure to read this handbook. Pay particular attention to any programming techniques you might be able to utilize.

Application pacs (which include business decisions, statistics, mathematics, electrical engineering, clinical lab, nuclear medicine, mechanical engineering, and surveying) contain about 20 prerecorded program cards apiece and a handbook containing a description of the programs with relevant equations, instructions for running the programs, example problems and program listings.

All prerecorded cards in the pacs have printed mnemonics which substitute for the instructions after a few familiarization runs. The mnemonics include input variables, keys to be pressed and outputs to be expected. A full explanation of the mnemonic symbols for the magnetic cards may be found on page vi of the *Standard Pac Handbook* and in each *Application Pac Handbook*.

Table 1: A list of precautions for prospective users of the Hewlett Packard HP-67 and HP-97 programmable calculators.

1. Always have a battery pack installed in calculator.
2. Connect the calculator to the charger using the following steps: a. Turn HP-67 off. b. Connect charger to calculator. c. Plug charger into power outlet. d. Turn HP-67 on.
3. Disconnect the charger from the calculator using the following steps: a. Turn HP-67 off. b. Unplug charger from power outlet. c. Disconnect charger from calculator.
4. Leave the W/PRGM-RUN switch in the RUN position except when programming or recording a program.
5. Check each program of the Standard Pac and your Application Pacs as soon as you receive the Pacs. Don't wait until the need occurs to discover an error.
6. Store partially completed programs on two blank cards. Don't trust yourself with only one copy.
7. If any difficulty is experienced when removing a program card from the window slot, press down on the card with a pencil's eraser and slide the card out of the slot.
8. If the motor begins to sound as if it is laboring, a pass or two of the abrasive cleaning card may clear up the problem. Remember, also, that a fully discharged battery pack must be charged for five minutes before a card can be read.

Key Functions

All of the HP-67 Key Functions are discussed briefly on pages 8 thru 13 of the *Owner's Handbook and Programming Guide*. The mathematical key functions are discussed in detail in the first 120 pages of the guide. Following this is a complete description of the programming key functions. Card reader operations and the appendices take up the rest of the guide.

Many of the mathematical and programming functions are self-explanatory by their designations. Examples of these, which would be familiar even to those people unfamiliar with Hewlett-Packard calculators, are ÷, X, +, −, π and $\sqrt{x}$. Experienced users should recognize ENTER, CHS, EEX and CLX. After brief explanations, it is easy to remember the function of most unfamiliar keys by their abbreviations: STK = stack review, ABS = absolute value, INT = integer portion, FRAC = fractional portion, RND = round off, STO = store, and RCL = recall.

32 of the keys may be used as a single stroke function, or they may be preceded by one of three prefix keys (two stroke function) and, occasionally, they may be followed by another function key (three stroke function). These 32 keys are used to provide 116 functions (five are redundant), but because the key designations closely describe the functions performed, they are easily memorized. I also found the mathematical functions listed in table 2 to be especially useful.

Functions I Would have Appreciated

The programming functions of the HP-67

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certainly allow the writing of complex programs. Yet, I would ask for the following additional features:

- I would like to be able to clear registers R0 thru R9 with one or two keystrokes, without clearing registers A thru E and I. (Pressing f CL REC clears primary storage registers R0 thru R9 plus A thru E and I.)
- I would like to be able to perform direct storage register arithmetic upon the contents of all registers. (Storage register arithmetic can be performed directly upon the contents of registers R0 thru R9 only. *Indirect* storage register arithmetic can be performed upon the contents of any storage register.)
- I would like to be able to directly address all storage registers. (Registers R0 thru R9 and registers A thru E and I can be addressed directly, while registers RS0 thru RS9 can be addressed indirectly or by pressing f P≷S.)

Most Appreciated Features

Personally, I think the most powerful HP-67 functions are the five program editing and manipulation functions. These five functions are nonrecordable operations that assist you in altering and correcting your programs.

The SST (single step) function may be used while either programming or running a program. When SST is pressed (with the W/PRGM-RUN switch set to W/PRGM) the calculator moves to and displays the next step of program memory. This allows you to view each step of the program without execution. If SST is pressed while the W/PRGM-RUN switch is set to RUN, the calculator displays the next step of program memory, and, when you release the SST key, the calculator executes the instruction loaded in that step. This operation is especially useful when debugging a program.

When the W/PRGM-RUN switch is set to W/PRGM, the h BST operation causes the calculator to move to and display the previous step of program memory. If the W/PRGM-RUN switch is set to RUN, pressing BST, after h has been pressed and released, causes the calculator to display the contents of the previous step of program memory. When BST is released, the original contents of the X register are displayed, the calculator having executed no instructions.

The GTO.nnn operation permits you to jump to any location in program memory for editing, additions or corrections to a program. When GTO. is pressed, followed by a three digit step number, the calculator transfers execution so that the next operation or instruction will begin at that step number (this happens whether the W/PRGM-RUN switch is set to W/PRGM or to RUN). No instructions are executed.

When the W/PRGM-RUN switch is set to W/PRGM, a press of h DEL will erase the instruction at the current step of program memory, and all subsequent instructions in program memory move upward one step. (Note: Any time an instruction is inserted between existing instructions in a program, all subsequent instructions in program memory move downward one step. Thus the HP-67 has a true insertion capability.)

Programming the HP-67

A program for the HP-67 is nothing more than a listing of the keystrokes necessary to perform the desired calculations manually, plus the labels to define the beginning and ending of the program, loops and subroutines. The listing may be prepared using a worksheet such as that shown in figure 1. The form shown is page 1 of a set of five with preprinted program steps from 1 thru 224.

When creating programs, remember that any solution that gives the correct outputs may be a suitable program. There is no *one* correct program for any problem. Emphasis, when programming, must only be placed on *time*. The *time* spent in programming must be compared to the *time* involved in running the program and the number of *times* the program will be used. It would be silly to spend days modifying a program with a running time of 30 minutes so that it could be run in 20 minutes if the program is to be used only two or three times.

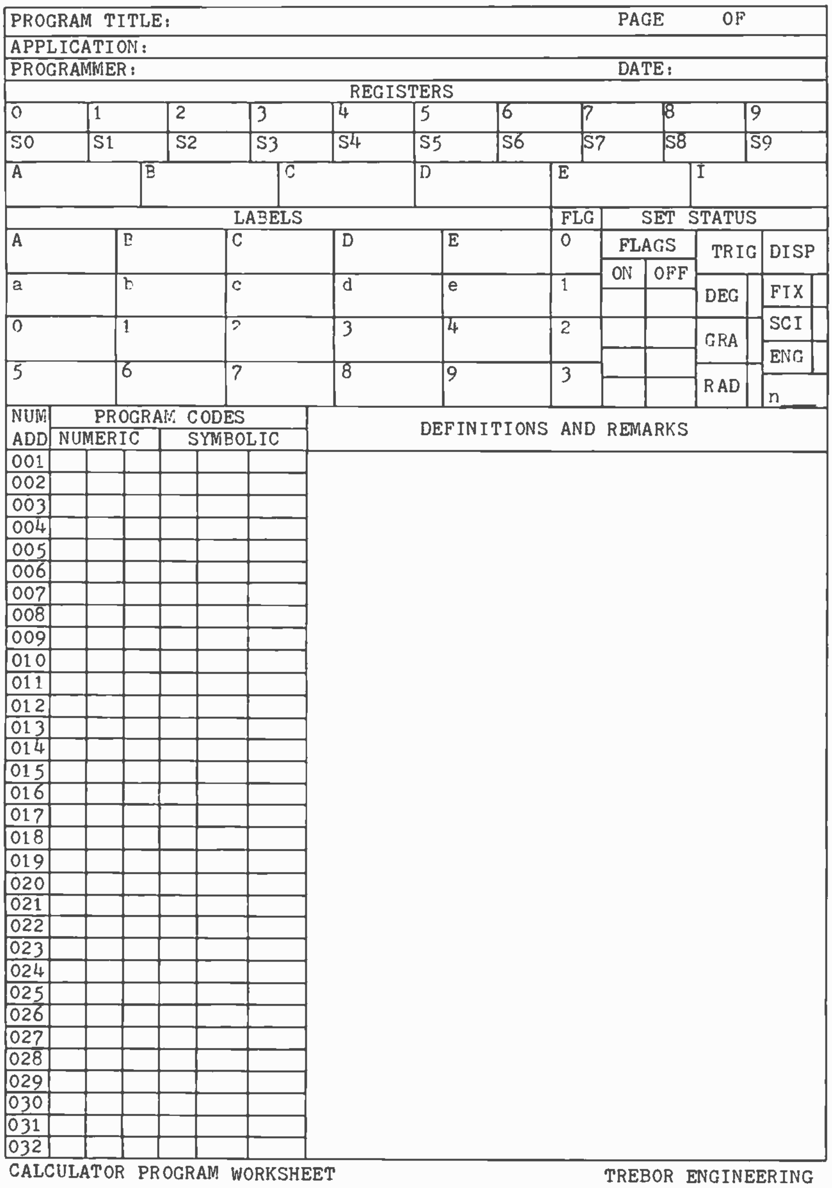
In addition, programming is a personal art. Spend enough time creating your programs to satisfy your own artistic fastidiousness. Of course, you are limited to the available memory. However, the example to be discussed illustrates that very complex

Table 2: Some useful mathematical functions available on the HP-67 and HP-97 programmable calculators.

Function Name	Definition
P	Rectangular to polar coordinates conversion
R	Polar to rectangular coordinates conversion
LSTx	Recalls number displayed before the previous operation
R	Converts degrees to radians
D	Converts radians to degrees
DEG	Sets decimal degrees mode for trigonometric functions
RAD	Sets radians mode for trigonometric functions
GRD	Sets grads mode for trigonometric functions
H.MS	Converts decimal hours or degrees to hours, minutes and seconds, or degrees, minutes and seconds
H.MS+	Adds hours, minutes and seconds (or degrees, minutes and seconds) in the Y register to those in the X register

problems can be handled with 224 steps of program memory. Furthermore, don't forget that data may be stored on the magnetic cards, and this memory is limited only by the number of blank cards you purchase.

The guide (and probably every other publication which discusses programming) suggests that a flowchart be drawn for each program. A flowchart breaks down a program into small groups of instructions which can be handled more easily than the entire program. In addition, flowcharts can be used as documentation for the program. I cannot argue with this reasoning because it seems logical. I can only say that I personally find flowcharts worthless when they are drawn, and I can, within the limits of my capabilities, write a program while another programmer is fooling around with the flowchart.


PROGRAM TITLE: PAGE OF
APPLICATION:
PROGRAMMER: DATE:

REGISTERS

0	1	2	3	4	5	6	7	8	9
S0	S1	S2	S3	S4	S5	S6	S7	S8	S9
A	B	C	D	E	I				

LABELS / FLG / SET STATUS

					FLG	FLAGS ON	FLAGS OFF	TRIG	DISP
A	B	C	D	E	0				
a	b	c	d	e	1			DEG	FIX
0	1	2	3	4	2			GRA	SCI
									ENG
5	6	7	8	9	3			RAD	n

NUM ADD	PROGRAM CODES NUMERIC			PROGRAM CODES SYMBOLIC			DEFINITIONS AND REMARKS
001							
002							
003							
004							
005							
006							
007							
008							
009							
010							
011							
012							
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027							
028							
029							
030							
031							
032							

CALCULATOR PROGRAM WORKSHEET TREBOR ENGINEERING

Figure 1: An example of the author's calculator program sheet used to write a program for the HP-67 which solves up to nine equations in nine unknowns.

I certainly do suggest, however, that you try the flowchart approach to programming, but don't be surprised if you find it easier to tackle the program directly. For documentation, I believe that comments with the program and the run instructions are more valuable than any flowchart, especially a year or two after the program is written.

While creating a program, a review of the "Function Key Index" every now and then will keep the full repertoire of the HP-67 fresh in your mind. This is important if you want to take advantage of the many mathematical, branching and looping functions available. Also, since there are usually many ways to accomplish a desired series of steps, spend a moment or two thinking of the various possibilities. For example, if a conditional test must be executed, would g X=Y, f X=0, f DSZ, f ISZ, g DSZ(i) or g ISZ(i) fit best in your program? Each of these functions are designed to be used in slightly different ways, yet all of them may be used to test for zero.

When g X=Y and f X=0 are used, the calculator branches around the next instruction if the question asked by the conditional is not true; f DSZ and f ISZ decrement or increment the contents of the I register unless its contents are zero, and, if the number in the I register has become zero, program execution skips the next step just like a false conditional instruction; g DSZ(i) and g ISZ(i) decrement or increment the contents of the storage register addressed by the current number in the I register unless the contents of the addressed register are zero, and, if the number in the addressed register has become zero, one program step is skipped.

These functions, as well as the many other programming functions, are fully explained in the guide. Since it is not my desire to reprint the guide, I will not dwell upon these explanations. I would, however, like to mention two other types of choices that must often be made.

One of these choices is whether to branch forward or to branch backward. A backward branch, which is usually executed faster, becomes necessary when all labels have been used for other purposes. But any correction to the program after the backward branch has been added may necessitate a correction to the number stored in the I register. (It is the number stored in the I register which causes the jump.)

The other choice is whether or not a subroutine should be used to accomplish the functions performed by a group of keystrokes used more than once during program

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execution. Because of the run time needed to search for the subroutine and the discontinuity in the program which results, I recommend not using subroutines unless it is absolutely necessary to save space in memory to accommodate a program which would otherwise have more than 224 steps.

I have seen commercial programs so riddled with subroutines that the programs had to be completely rewritten at enormous expense after the programmers were replaced. Of course, you would not want to punish yourself this way. When you own the calculator, you don't pay for computer time or memory. It costs you the same to run a 224 step program as it does a five step program.

As I have stated above, the guide covers all programming operations thoroughly. There is one operation I found difficult to implement. I am referring to the g MERGE function, but now that I have performed the function successfully, I can't imagine the cause of the difficulty I experienced.

The g MERGE function allows data or programs from magnetic cards to be merged with data or programs in the calculator. When a program from a card is merged with one in the calculator, steps 000 thru nnn of the original program are preserved. This function permits you to add to or alter a program that is already loaded in the calculator.

In fact it is possible to include the g MERGE instruction immediately preceding the h PAUSE instruction in a program and to load a program or data from a magnetic card into the calculator while a program is running. Not mentioned in the guide is the fact that when a program is loaded during a pause in a running program an h RTN immediately following the h PAUSE will be overwritten by the first step of the merging program and execution of the new program will begin immediately after it is loaded.

Card Reader Operations

One of the primary reasons the HP-67 is such a versatile calculator is its ability to store information on magnetic cards and to retrieve this information at a later time. Therefore, I would like to stress the following points concerning this operation:

- When storing the contents of the registers on a data card, always pass side 1 of the card through the card reader first, then side 2, if necessary. This insures that any nonzero data in the secondary registers will always be stored on side 2 of the card.
- When it is necessary to restore data from only one side of a magnetic card into the calculator, pass the side of the card which contains the data through the card reader. Then, when crd is displayed, press CLX.
- Accidents may occur that will destroy the program or data on a card, therefore, if the information to be stored is important or extensive, do yourself a favor and store it on two cards.
- Identify the information on your magnetic cards with a #2 pencil. When necessary, the cards can be easily erased.
- When inserting the leading edge of a card to be read into the card reader automatically during a pause, remember that the program must actually be running when you insert the leading edge. Be sure to insert the tip of the card far enough into the card reader.■

Next month's concluding installment of this article features an example program showing how the HP-67 can be used to solve simultaneous network equations for an electrical network.

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SPECIFICATIONS

DISPLAY

SCREEN CAPACITY, CHARACTERS	2000
CHARACTERS PER LINE	80
NUMBER OF LINES	25
SCREEN	P4 phosphor (white)
TUBE SIZE(DIAGONAL)	12 inches (30.4 cm)
VIEWING AREA	54 square inches (137.1 cm)
CHARACTER SIZE	0.20" high x .08" wide (5.08 mm high x 2.03 mm wide)
REFRESH RATE	60 Hz (50 Hz available)
SCAN METHOD	Raster
CHARACTER GENERATION	5 x 7 character in an 8 x 10 dot matrix
CURSOR	Blinking block

MEMORY

TYPE	Random Access Memory
CAPACITY	2000 characters

OPERATOR CONTROLS

POWER ON/OFF SWITCH	On rear of unit
BRIGHTNESS CONTROL	On rear of unit

POWER REQUIREMENTS

Model 501 – 115 volts, 60 Hz, 100 watts nominal
Model 502 – 230 volts, 50 Hz, 100 watts nominal

INTERFACE

DATA FORMAT	
DATA BITS	7 serial, asynchronous
DATA BIT 8	1, 0 or deleted
PARITY	Odd, even or deleted with error displayed as DLE
STOP BITS	1 or 2
DATA TRANSFER RATE	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 BAUD

STANDARD FEATURES

INVERSE VIDEO	Operator or software selectable
TRANSMIT MODES	Half or full duplex (switch selectable)
DATA ENTRY	Top or bottom line
END OF LINE BELL	Switch selectable
CURSOR POSITIONING	X–Y
CURSOR ADDRESS	Load and read
DISPLAYABLE CHARACTERS	126 (including space)
CURSOR CONTROLS	Up, down, left, right, home, return
AUTOMATIC ROLL–UP	Switch selectable
AUTO CARRIAGE RETURN AND LINE FEED	Switch selectable
MONITOR MODE	Special "Monitor" Mode allows display of control codes (first two columns) of ASCII Code Chart).

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Computer Assisted Flight Planning

The production of flight plans is a task that lends itself well to computer solution. It is a time-consuming and repetitious job involving numeric manipulation and output formatting, just the sort of thing that computers do accurately and quickly. The drawback has been, of course, that computer facilities have not been made available to pilots in a way that allows timely production of flight plans. To be useful, flight plans must reflect accurate route and weather data, and so cannot be produced too far in advance. The solution, of course, is that the increased availability of computing facilities made possible by the microprocessor makes automated flight planning practical even for private pilots.

The heart of any flight planning system consists of three calculations. Indeed, anything else the system may provide is really the option of the system's designer. The first necessity is a true air speed calculation. Without going into too much detail, airplanes fly with "indicated" air speeds, but flight plans need "true" air speeds for their calculations. The formula used in my program is:

$$\text{true air speed} = \text{indicated air speed} \times [.971 + \text{temp} \times ((.017 + \text{INT}(\text{altitude} / 50.1) \times .002)/10) + \text{altitude} / 10 \times (.02 + \text{INT}(\text{altitude} / 50.1 \times .00035)]\ .$$

This formula provides accuracy within 1 knot up to altitudes of 15,000 feet. The error is somewhat greater than that above 15,000 feet, but might be considered acceptable up to 20,000 feet. For private sector flying this formula should provide excellent accuracy and reasonable simplicity. Another simpler formula is usable up to altitudes of 8,000 feet:

$$\text{true air speed} = \text{indicated air speed} \times (\text{temp} \times .002 + \text{altitude} / 10 \times .018 + .971).$$

There are formulae which purport to give absolute accuracy at all altitudes, but those that I am familiar with are extremely cumbersome and time-consuming.

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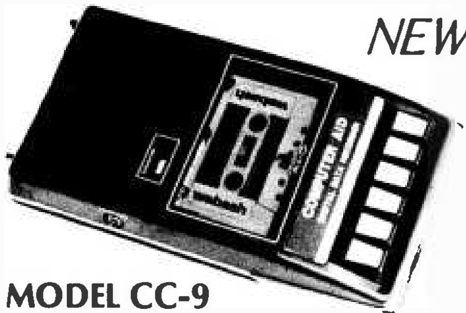

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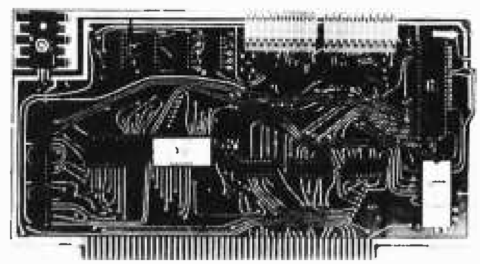

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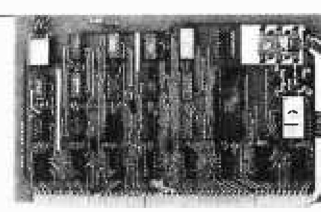

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The second necessary calculation is drift. Drift is the measure of how many degrees off your intended course the wind will blow you if you let it. My program uses a one pass wind solution that gives the drift and ground speed after going through the formula just once. This particular solution has the disadvantage of requiring the use of an inverse sine ($\sin^{-1}$) in the calculation. The one pass drift formula is:

$$\text{drift} = \sin^{-1}\left[\frac{\text{wind velocity} \times \sin(\text{course} - \text{wind direction} - 180)}{\text{true air speed}}\right]$$

It is possible to substitute an inverse tangent calculation for the inverse sine. This substitution is:

$$\sin^{-1}(Y) = \tan^{-1}(Y/\mathrm{SQRT}(1 - Y^2)).$$

The one pass ground speed formula is the third of the three necessary calculations. This formula will not work for direct head winds or tail winds. These conditions must be handled separately. In this program, I detected these situations prior to the drift calculation to save the extra step. The one pass ground speed formula is:

$$\text{ground speed} = \frac{\sin(180 - \text{course} + (\text{wind direction} + 180) - \text{drift}) \times \text{true air speed}}{\sin(\text{course} - (\text{wind direction} + 180))}$$

The special cases of direct head or tail winds are easy to handle. In either case the drift is 0. For head winds (course − wind direction = 0), the ground speed will be equal to true air speed minus wind velocity. For tail winds, ground speed will be equal to true air speed plus wind velocity.

An alternative to the one pass system is a *two pass* system. In this case the course is applied to the formula initially to obtain an estimate of the drift. This in turn is applied to the course to get a heading. The heading is then used in the formula to obtain the actual drfit and ground speed. This routine is equally accurate and has the advantage that it requires no functions more sophisticated than sine and cosine. In an extreme case the sine and cosine functions could be obtained by reading a table.

As I said earlier, any output beyond these three basic pieces of information is at the discretion of the system's designer. I use a similar system to produce flight plans for low altitude and high-speed routes, which I fly as a C-130 instructor navigator. That system uses fixed route data stored on disk and produces precise ETAs (estimated times of arrival) and includes a lot of ancillary output information concerning altitudes,

high obstructions along each leg, and detailed descriptions of each turn point.

This program, however, is intended to fit the most general case; readers can tailor it to their own needs more easily if what they start with is not too cluttered. The program accepts basic header data and then information concerning each leg of the

Listing 1: Sample program of the flight program. The typical output from the program is also shown.

```
DATE (YY,MM,DD): 78,06,20

THIS FLIGHT PLAN GOES FROM: LITTLE HOCK
                        TO: NEW OHLEANS
PILOT'S NAME: TITUS PUHDIN
ACFT TYPE:
PROPOSED TAKE-OFF TIME: 1200



LEG # 1
THIS LEG GOES FROM LITTLE HOCK TO [MEMPHIS ]
                                  [        ]
MAG COURSE: 072
LEG DIST: 111
ALTITUDE (X100): 50
TEMP AT ALT (C): 22
IND AIR SPEED: 120
WIND (DDD,VV): 210,15
DO YOU HAVE ANOTHER LEG TO ENTEH? YES


LEG # 2
THIS LEG GOES FROM MEMPHIS TO [GHNWOOD ]
                              [        ]
MAG COUHSE: 186
LEG DIST: 97
ALTITUDE (X100): 50
TEMP AT ALT (C): 22
IND AIR SPEED: 120
WIND (DDD,VV): 230,10
DO YOU HAVE ANOTHEH LEG TO ENTEH? YES


LEG # 3
THIS LEG GOES FROM GHNWOOD TO [JACKSON ]
                              [        ]
MAG COURSE: 177
LEG DIST: 50
ALTITUDE (X100): 50
TEMP AT ALT (C): 22
IND AIR SPEED: 120
WIND (DDD,VV): 230,10
DO YOU HAVE ANOTHEH LEG TO ENTER? YES


LEG # 4
THIS LEG GOES FROM JACKSON TO [MCCOMB  ]
                              [        ]
MAG COURSE: 177
LEG DIST: 79
ALTITUDE (X100): 50
TEMP AT ALT (C): 22
IND AIR SPEED: 120
WIND (DDD,VV): 230,10
```

route. It allows 25 individual legs, and prints a formatted flight plan of fairly simple design.

The program is based on magnetic information (magnetic courses and magnetic winds). This is simple and direct because the end product is supposed to be a magnetic (compass) heading. A more formal solution can be made based on true information (true courses and true winds) by applying magnetic variation. A typical program run is shown in listing 1.■

The Nybbles Library is an inexpensive means for BYTE readers to share some interesting but specialized forms of software. These programs are written by readers with small computers and printer facilities, and are therefore designed for particular systems. The algorithms and programming techniques in these programs can be directly used by readers with similar equipment, or can serve as an inspiration for improvisation on computers of different characteristics.

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Continued from page 6

paste, until the document is finished or the author is exhausted. To me, that is inefficiency! Of course, many computer text editors are not well suited to creative composition, being little more than teletypewriter editors. Even with many display editors one still has to resort to hard copy for effective editing. That is the nub of our problem: most display editors are line oriented and run on "glass teletypewriters." The latter were derived from hard copy terminals, which were in turn derivatives of keypunches—certainly an old way of thinking about text production. If the display media are truly utilized, however, a quantum improvement in editing facilities can result: information can be presented as in a "video book," complete with rapid random access paging and on screen cutting and pasting.

Given such a tool, creative composition becomes a joy. Freedom of expression is improved; the ideas flow freely from mind to screen. A phenomenon of egoless composition results; the author does not have to measure the content of a passage against the agony involved in its creation. As a result, the author is more willing to modify and polish the document, even experimenting with major revisions in order to present the topic in its best light. What is truly exciting is that the technology for such editing systems is now of modest cost; one need only break with the past ways of thinking about editors.

What does this have to do with our subject? There is a strong analogy between the editing task and the programming task. We must examine the programming task the same way we looked at editors. Alas, most of us still program on "virtual keypunches." We may even use one of these excellent display editors to create our card deck, but we create a linear string of characters and throw the completed program at a compiler; given that there are no syntax errors, we try to run the program, probably debugging with dumps, print statements, or debuggers which give us information in terms of the compiled code. If an error is found, we return to the editor to modify the source, recompile, and try again. Given these conditions, sloppy work habits are inevitable. In fact, the *conditions* are sloppy.

Editing Programs

Now we are at a critical point in programming: do we build a better "programming keypunch," or do we look for a programmer's tool analogous to the display editor? I would opt for the latter, and would claim that the paradigm of LISP programming is the appropriate model from which we should begin.

First, let's examine the conservative "keypunch" approach. The traditional edit-compile-debug cycle is improved by a display editor, operating with a compiler that can return the user to the editor upon indication of a syntax error, pointing at the source statement that caused the error. A quick edit, and the syntax check cycle begins again. However, once the program is compiled, we are still at the mercy of primitive debugging techniques. One solution is to require that the user specify more information about the program, indicating expected behavior of program modules with the assumption that the compiling phase can be made more knowledgeable, and check the consistency of the expectations against the realities present in the user's encoded algorithms. This reassures us that the code which gets to the debug portion of the cycle does operate as expected. In general these user expectations are difficult to express, and checking their consistency is even more problematic. Syntactic consistency checks based on simple properties of the programmer's variables can be checked in a reasonably straightforward manner. Such properties are called type structures. The compiler checks each occurrence of an identifier to ensure that it always has the same type; with simple variables, this involves checking such things as "Is it an integer?", "Is it a Boolean operator?" with procedures the compiler checks to make sure that the programmer's calls are consistent in the number of arguments supplied and the types of the parameters. Such consistency is important, but it usually requires that the programmer supply declarations throughout the program segments, specifying the type structure information of each and every identifier. This approach offers a short-term payoff in an increased probability that the generated code will perform as expected. But then, there's still the strong possibility that the programmer's errors are not so transparent that type checking can detect them. One approach is to improve the consistency phase, strengthening the compiler's ability to detect inconsistencies between expectations and reality. This requires that programmers express more and more of their expectations along with their algorithms; a program verification system results. Such a system would guarantee that the expectations expressed were consistent with the written algorithm. The debugging problem vanishes, but is replaced with a specification task that may be as difficult to accomplish as the debugging.

AI and Programming Expectations

What about programs whose expectations are not easily formulated? The primary example is artificial intelligence programming: often it is only the final algorithm itself which expresses the expectation. The creative programming process is driven by a partially understood phenomenon; the programming effort is to capture as much of that phenomenon as possible. We program in a world of great uncertainty, much like driving a car. We may have a reasonably detailed roadmap, but the path may involve traffic lights, accidents, and detours. We do not return home and restart every time we encounter an unexpected situation; we correct on the fly and continue. I feel that much of modern computation has this exploratory character of artificial intelligence.

What about programs which contain issues involving more than correctness? For example, it would be difficult to express the specifications of a text editor in terms of static conditions. To be sure, certain aspects of editors involve correctness, but usability is equally important. An experimental process is involved which requires modification and iteration. In fact the editor *exists* for modification. If we made no typing errors we would not need an editor. For example, when we discover an error in a text file, we don't erase the whole file and retype it—we edit the error and keep the result. However in the traditional debugging paradigm, when we discover a run-time error, we throw away all the computation, edit the file, and restart. If that computation has taken several hours (or even minutes) to elicit the bug, it will be most painful to restart.

Most programming involves a deeper issue than debugging: it involves modifiability. Programs are always being modified because we change our expectations. Debugging is only a very minor component of the problem of program modification. Therefore, as we progress to more and more complex programming tasks, programming modification will take on a more fundamental role. Don't try to stamp out program modification as a manifestation of human frailty and error; it is a fundamental ingredient of our field. Cater to modification at the innermost levels of our programming systems. Assembly language continues to dominate systems design not because of inate masochism, but because of modifiability. There is a close (but low level) match between the language, the debugger, and the execution device. Any language that expects to dethrone machine language must offer an equally compelling environment.

"Modifying a Blank Screen"

One artificial intelligence researcher has characterized programming as "debugging a blank piece of paper." To that I would add: *programming is modifying a blank screen*. Get the machine into the programming process as soon as possible, but it must be done right. In that context we will see a rise in productivity comparable to that experienced in the editing task when a true display editor is used. We can expect egoless programming and good work habits to evolve naturally. With such tools the promise of structured programming can become a reality. That is, it is the *activity* of programming that involves the structuring. One should not expect to find structure in a program anymore than one can look at the final board positions of a chess game and tell whether that game was played by Masters or amateurs. Imagine programming systems whose "moves" involve stepwise refinement of partially elaborated programs; imagine the transcript of those keystrokes as comparable to the recording of moves in the chess game. The transcript of the program development would be available for analysis by programming students and teachers. Such a system would truly support structured programming. Current practice does not support such activity. We are forced to submit character strings to our language systems, even though our methodology tells us to compose in terms of structure. Until that disparity is resolved we should expect little improvement in the software problem.

Most programming languages do very little to reinforce the creative process of algorithm discovery and creation. They are more concerned with the *execution* of already constructed algorithms. This is a natural outgrowth of their ancestry: a numerical computation era in which the emphasis was placed on minimizing computer time at the expense of programmer time. Also, the programming problems of that day involved the transcription of well-specified numerical algorithms into an equally precise programming language. Times and economics have changed. The problems are more complex and no longer as well-specified as those of numerical analysis. Now computers are cheap and programmers are expensive; we need techniques to speed the development of correct programs. Certainly the verification efforts are aimed in this direction, but verification typically is an after-the-fact reconciliation of a completed algorithm with some descriptive specification of its behavior. We need languages that support the creative and exploratory phases of program development. Of course, one may question this. In the Computing Surveys, Wirth writes:

> . . . *It is therefore entirely possible that in the future a more interactive mode of operation between compiler and programmer will emerge, at least for the very sophisticated professional. The purpose of this interaction would not, however, be the development of an algorithm or the debugging of a program, but rather its* improvement under invariance of correctness. [Wirth's emphasis].

I most definitely agree with the emphatic phrase; we must develop such program transformation systems. However, it is equally important to improve the program development phase.

Exploratory programming, which is the hallmark of artificial intelligence and which, to a very large extent, occurs in the creative stages of any programming task, is best done with an untyped interactive language like LISP. Strong typed languages like Pascal only confuse and obfuscate the formulative stages.

LISP's basic unit is an expression, meaning that every LISP construct computes a value. LISP tends to emphasize the applicative nature of algorithms, using "function application" as its basic computational notation and using recursion to express the control aspects of the process; recent research has indicated that many common recursive schemes can be *executed* in an iterative fashion. That is, the evaluation mechanism need not involve the usual stack oriented overhead. One should not confuse the recursive notation with the evaluation mechanism.

The basic unit of Pascal is a statement, rather than an expression. That is, Pascal's units tend to be executed for *effect* rather than *value*. It is interesting that John Backus, the "father" of FORTRAN, has spent considerable time in recent years studying and advocating applicative languages, turning from the more traditional imperative, statement oriented languages like FORTRAN, ALGOL, and Pascal. In his Turing lecture, Backus writes:

> *This world of statements is a disorderly one, with few useful mathematical properties. Structured programming can be seen as a modest effort to introduce some order into this chaotic world, but it accomplishes little in attacking the fundamental problems created by the word-at-a-time von Neumann style of programming, with its primitive use of loops, subscripts, and branching flow of control.*

Of course things are not all that black and white. Pascal has applicative aspects and LISP has imperative aspects. The difference is again one of emphasis and philosophy: the expression versus the statement. The difference has a mighty influence on the language design: expressions lead to calculator-like interactions; statements lead to computer-like programs. Wirth, in the Computing Surveys, writes:

> *We must recognize the strong and undeniable influence that our language exerts on our way of thinking, and in fact defines and delimits the abstract space in which we can formulate—give form to—our thoughts.*

Computing Attitudes

That is a critical point, true in natural language as well as in programming languages. In fact, the problem goes deeper than programming language. One's attitude about computation is deeply connected with the human interface problem. Those who grew up with batch oriented computation have a quite different frame of reference from that of a person who has experienced truly interactive access.

These attitudes permeate the whole computing approach. If one is to interact with a calculator, then we must expect to present expressions and receive values; that implies an immediacy which is antithetical to type structures. So too is interactive design; the interactive creation and running of partially specified programs is difficult to reconcile with language processors that expect total information about all program segments and identifiers.

By now many of you are sure that I am preaching total heresy, advocating a return to the old days of hack and patch programming. I am definitely not. Rather, I am advocating the development of programming systems that incorporate the ideas of structured stepwise development of programs—systems in which the interactive *development* is as flexibly supported as the interactive *debugging* of modern LISP systems. We must do for programming what the page oriented display has done for editing. But such systems are only half the software problem. We must dramatically improve the way people think about programming. Computer programming is probably the most difficult and challenging enterprise mankind has ever undertaken. Until programming methodologies are supported by the programming tools, and until programmers are expected to spend as much time perfecting their craft as professional engineers and poets, we should expect little improvement in software quality.

We must put a stronger emphasis on the education of programmers, rather than restrict the expressive powers of the languages. Consider the tools of a more traditional craftsman: in the hands of an amateur those tools can be deadly, whereas the craftsman can develop exquisite objects. We do not propose that all tools be dulled appropriately so that the amateurs cannot do themselves injury! We educate them in the proper use of, and respect for, the instruments and expect that the craftsman's tool remain sharp. The emphasis is properly placed on the individual. Do not confuse education with the mass-merchandizing of armies of programmers whose competence is sealed in a cautious, uncreative world of dull tools. The artificial intelligence community is the craft of the tool builder; their tools are the sharpest and most incisive of the computer field. It is this kind of tool which should appeal to the personal computer person. It is not the elegance of BASIC which has made it the standard personal computer language; it is BASIC's interactive nature, allowing quick experimentation with programming ideas, that accounts for its longevity. This interactive flavor can be grafted onto a Pascal-like language, but it is much more difficult to do this successfully. In the process one either compromises the tenets of the language (extensions) or compromises the resulting system.

"Wild West" Computing

The essence of personalized computing has been sort of the "wild west" attitude: open, undisciplined, but creative and lusty as hell. You are a very healthy sign; today, a modest personal computer has more power and flexibility than that available in a professional installation 20 years ago. Each of you has molded your system according to your desires and economic constraints. But freedom is expensive; systems and programs become one of a kind. Enter compatibility and, unless you are careful, exit individuality. Clearly these problems are not solely the province of personal computing; the manufacturers feel the same pressures. So the real question is: can we bring discipline and order to programming without curtailing the creativity?

Personal computer users need not give up the interactiveness of BASIC to gain the structure and portability which Pascal is advertising; LISP offers both. BASIC's longevity, indeed strength, lies in its "friendliness." That is a critical ingredient of an interactive programming language. I guarantee that if BASIC were available only in the traditional batch oriented environment, its popularity as a personal computer language would not have occurred. Similarly with LISP or Pascal. That is, it is the total environment in which a language is situated that is important. The UCSD experience with Pascal illustrates this point well. The real question then is: can we do better?

LISP is *not* a special purpose list processing language. A modern LISP system has more flexible data handling facilities than other more recent languages. For example, MACLISP's data types include arbitrary precision numbers, very flexible record structures (called property lists), strings, arrays, list structure, and even procedures. One attribute which leads to LISP's elegance and economy of expression is that all of these data types are available as values of programming constructs. Thus LISP procedures may take procedures as values, return procedures as values, or create arrays which are returned as value.

Lest you suspect that such generality implies inefficiency, note that LISP has been used as the systems programming language for the MIT LISP machine. All system software is written in LISP even to the level of the algorithms that place the characters on the screen. Even the microcode is written in LISP. LISP compilers can be as good as those of any other language. In one experiment, the MACLISP compiler was tested against a FORTRAN compiler on some purely numerical examples. The LISP compiler's code was better both in terms of space and time.

Might not such generality lead to sloppy programming techniques? Note again that a language is a tool, and is only as effective as its user. I would rather sharpen the user than dull the tool. In terms of user aids, LISP excels. A modern LISP system is an integrated programming environment incorporating editors, debuggers, and compilers. Some LISP packages include sophisticated error recovery modules, allowing the user to undo computations or explore alternative computations. The integration of these "programmer's assistants" with modern display techniques has begun. The results are quite impressive. The flexibility of these systems is due in large part to LISP's unique representation of programs as data structures. As a result, it is easy to write programs which manipulate programs. Note that language editors, debuggers, compilers, and program transformations systems like those advocated by Wirth (above) all fall into this category.

One also hears dreadful rumors about LISP's syntax (Lots of Irritating Single Parentheses). First, the regularity of the notation and the simple syntax more than make up for any initial inconvenience. However, these syntactic difficulties can also be stifled directly. It is quite simple to supply LISP with an ALGOL like sugared input and output. Such parsers and unparsers are simple LISP programs.

The above discussion has hinted at a very important aspect of LISP: LISP *is* a machine language. In the traditional machine, instructions reside in memory locations just as data does. It is the access path of the processor that determines how the contents of a location are to be interpreted. Access by the program counter implies an instruction fetch; other access implies a data fetch—so too in LISP. Data and program are stored identically; both are presented to the machine in a simple syntax of lists. The LISP CPU (central processing unit), called *eval*, accesses LISP memory either to fetch code or data. Instead of the linear sequential representation of traditional machines, LISP has a tree-like storage scheme. One very exciting area of investigation involves architectures for LISP-like machines.

Finally, it is often assumed that LISP demands large expensive computers for its implementation. That, too, is not true: there are versions of LISP for the Z-80, 8080, 6800, F8, LSI-11, and even a version in BASIC. Certainly the machine size will limit the range of feasible applications; but that is true of any language. The new class of microcomputers is particularly exciting. They will open up many new areas—including artificial intelligence study—for the personal machine. The new machines will support very substantial implementations of LISP.

It is particularly important to influence the personal computer advocate now, given the growth in computing power and the cries for compatibility, discipline, and standardization. The DOD-1 language effort is but the latest manifestation of this attitude. I do not believe that this legislative approach is healthy. I believe that LISP offers a healthy alternative to the current choices of programming languages for personal computation.■

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Clubs and Newsletters

Southeastern Michigan Computer Organization Sponsors TRS-80 Group

SEMCO (the Southeastern Michigan Computer Organization) sponsors a TRS-80 special interest group for Radio Shack TRS-80 enthusiasts. Meetings are for the beginning hobbyist and computer expert alike. The main objective is to share ideas on programming, troubleshooting and new or compatible TRS-80 products. This group meets the first Saturday of every month from 6 to 9 PM. The location is the Bryant Branch Library, Michigan Av and Mason St, Dearborn MI 48124.

Northwest Computer Society

The Seattle chapter of the Northwest Computer Society meets at the Pacific Science Center on the first and third Thursday of each month at 7:30 PM. The first meeting of the month is normally held in room 200 on the east side of Science Center Court. This meeting usually features a formal presentation by a speaker or speakers. The second meeting of the month is normally held in the math room at the southeast corner of Science Center Court. This meeting is usually more informal with freewheeling discussion and problem solving. Call the recorded information line at (206) 284-6109 or write to POB 4193, Seattle WA 98104.

South Florida Computer Group

The South Florida Computer Group has two chapters, one in Miami and the other in Ft Lauderdale. Members can attend meetings at both chapters and visitors are welcome. The Miami chapter meets the first Monday of every month at the Papanicolaou Cancer Research Institute, 1155 NW 14 St, Miami. The Ft Lauderdale chapter meets the second Tuesday of every month at the Social Annex Building, Holiday Park (behind the Parker Playhouse). Both chapters have a $5 a year membership fee which includes their monthly newsletter, *I/O*. For more information about this group, write to Robert Lief, Papanicolaou Cancer Research Institute, 1155 NW 14 St, Miami FL 33136.

Australian 9900 Users Group

The Australian 9900 Users Group is a relatively new club concerned with the 9900 family of devices and applications for process control and business data processing. They have both Texas Instruments and Technico equipped members and would welcome contact with overseas correspondents. Presently, they do not have meetings but operate by direct contact or by correspondence between members. Contact Barry Day, 43a Osborne Rd, Lane Cv, NSW 2066, AUSTRALIA.

Melbourne Australia Computer Club

We have heard from Andrew Stewart, correspondence secretary of MICOM (the Microcomputer Club of Melbourne). The club meets the third Saturday of every month at Railway Modellers' Hall, Wills St, Glen Iris, Victoria. The dues are $7.50 per year, which includes a monthly newsletter and quarterly magazine. MICOM can be contacted at POB 60, Cantebury, Victoria 3126, AUSTRALIA.

North London Hobby Computer Club

A press release has come our way informing us of a recent meeting of the North London Hobby Computer Club. At this particular meeting, held at the Polytechnic of North London, over 200 members and guests listened to a talk given on the present situation in personal computing. After the talk, three user groups were formed: a PET user group; a business user group; and another group of individuals interested in homebrew activities. The club is planning a series of lectures, and hopes to publish a regular monthly newsletter. For more information, contact Robin Bradbeer, Dept of Electronics and Communications Engineering, Polytechnic of North London, Holloway Rd, London N7 8DB, ENGLAND.

Circle 1 on inquiry card.

Attention: TDL Users

An exchange of information among users of TDL (Technical Design Labs) equipment and software is being started by Dr John R Cameron, POB 1517, Palo Alto CA 94301. If you would like to correspond with others who have similar interests, send descriptions of any and all Z-80/TDL related hardware and software to Dr Cameron. He asks that you enclose a brief summary (typed, single spaced) of your offerings and wishes, with your return address. Whatever material you wish to disseminate may be enclosed, or give prices and availability for commercial offerings. A users survey is also being compiled, so you may wish to describe your system and its applications. For copies of other users' summaries and information of general interest, send $3 to Dr Cameron at the above address.

New Computer Group in Battle Creek MI Area

Called the Battle Creek Area Microcomputer Club, this group consists largely, but not exclusively, of TRS-80 owners. Meetings are on alternate Thursdays at 7 PM and include software swapping, hardware topics, tutorials, etc. Both professionals and beginners are welcome. For detailed information, contact Jeff Stanton, 8587 Q Dr N, Battle Creek MI 49017.

Pittsburgh Area Computer Club Members Compete for Monthly Babbage Award

PACC (the Pittsburgh Area Computer Club) is currently meeting every third Sunday at 11 AM in the community room of the Northway Mall. They normally have a 2 hour general session, followed by a formal meeting with a speaker. This in turn is followed by another general session in which the various user groups meet. During the formal meeting the monthly Babbage is awarded to the "best in its class." Members and guests are invited to bring their systems, share their ideas and vie for the Babbage prize. Contact PACC, 400 Smithfield St, Pittsburgh PA 15222.

Space Coast Microcomputer Club Celebrates Second Birthday

Ray Lockwood, president of the Space Coast Microcomputer Club, called us with information about his computer group. The club recently celebrated its second birthday and boasts a membership of approximately 100. They meet every fourth Thursday at 7:30 PM at the Merritt Island Public Library, 315 Inlet Av, Merritt Island FL. The membership fee of $5 includes the club's newsletter. Ray tells us there is club interest, but not exclusively, in 8080 and Z-80 systems. If you wish further information, he can be reached at (305) 452-2159.■

BYTE's Bits

Call for Papers

The 17th annual meeting of the Association of Computational Linguistics will be held August 11 thru 12, 1979, on the campus of the University of California, San Diego, at La Jolla CA. Papers are being solicited on linguistically and computationally significant topics, including theoretical and methodological problems of computational linguistics (eg: mathematical foundations, software tools); computational semantics (eg: linguistic semantics, deductive logic, artificial intelligence); automatic syntactic parsing and synthesis of natural languages; computational lexicography and stylistics (eg: concordances and statistical studies); speech recognition and synthesis, graphemics (ie: character recognition); automated terminology dictionaries, machine translation and machine aided translation. Authors wishing to present a paper should submit five copies of an extended abstract (not to exceed 1000 words) by April 1 1979 to: Dr Norman Sondheimer, Sperry Univac, POB 500, M S 2G3, Blue Bell PA 19424, (215) 542-5896.■

Boston is Having a Huge Small Computer Show

Hynes Auditorium in Boston is the site of the Northeast Computer Show. The show originally scheduled to be held April 6, 7 and 8, 1979 has been changed to September 28, 29 and 30, 1979. The Northeast Computer Show will be a total spectrum presentation for the trade and public. There will be two separate sections to the show: a small business system section and a personal computing section.

The personal computing section will feature microcomputers, small computer systems, business opportunities, electronic and video games, career and employment opportunities, education exhibits, free seminars and lectures. Exhibitors will display the latest in personal computing hardware and software, computerized music synthesizers, computer amusements, computer generated art, graphics, and animation. Dozens of free lectures and seminars will be given by internationally recognized speakers for all categories and levels of enthusiasts including introductory classes.

The admission fees to the show are $5 for adults, $4 for college and high school students. For more information write or call: Northeast Exposition, POB 678, Brookline Village MA 02147, (617) 522-4467.■

Tektronix Microprocessor Design and Development Lab Workshops

Tektronix Inc is offering a series of microprocessor design and development lab workshops. Two different types of workshops are available: one lasts five days for those who want exposure to basic microprocessor design and organization, as well as experience in design development and testing. The other is a 3 day workshop for those already experienced in microprocessor design who wish more intensive training in developing and testing a design using the Tektronix 8002 Microprocessor Development Lab. Both workshops will provide a practical, hands-on, results oriented learning experience. The purpose of the workshop is to help the attendee grow as a professional designer. For a complete listing of dates and locations, write to Tektronix Inc, POB 500, Beaverton OR 97077.■

International Date Standard

Software system writers may be interested in the international standard for writing numeric dates. In 1971 the International Organization for Standardization adopted Recommendation 2014, which provides for a system of descending order when writing numeric dates on any letter or document. If numbers only are used, the first day of July in the year 1979 should be written 1979-07-01. The hyphen is preferred as a separator, rather than the period, slant, or space.

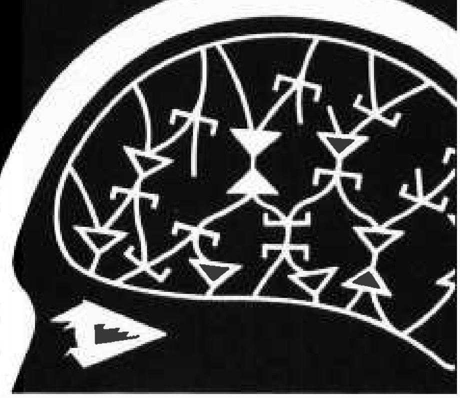
If the month is given in alphabetic form, one can write the date in any order (eg: 1 July 1979, July 1 1979, or 1979 July 1). No ambiguity results when a 4 character year field is used.

A related document, Recommendation 2015, sets up a standard for the numbering of weeks. It is recommended that for business and commercial purposes, Monday be regarded as the first day of the week. Furthermore, the week should always be seven days in length. A week which is divided by the turn of the year should be attached to the year containing a majority of days in that week.

ANSI (the American National Standards Institute) is the member organization representing the United States. Correspondence should be directed to ANSI, 1430 Broadway, New York NY 10018.■

Sargon Reproduced

We have been informed by Matt Mihovich of the Hayden Book Company



that the Sargon chess program described in recent issues of BYTE is no longer directly available from the authors. It is now marketed by the Hayden Book Company in book and tape (TRS-80, Level II) formats. The book retails for $14.95 and the tape for $19.95. Contact Hayden at 50 Essex St, Rochelle Park NJ 07662.■

New Computer Chess Champion

At the Computer Chess Championship held at the 1978 ACM (Association for Computing Machinery) meeting this past December, a new champion emerged from the Swiss system tournament. The program *Belle*, developed at Bell Laboratories, edged out defender Chess 4.7, the program developed by Slate and Atkin at Northwestern University. The Belle program runs on a Digital Equipment Corp PDP-11 with special hardware to generate moves, and a new device to evaluate positions using high speed hardware.

Of interest to microcomputer users is the relatively good performance of the Sargon program, written by Dan and Kathe Spracklen. It managed a good enough performance for a tie for third place, although the Swiss system leaves controversy concerning its exact ability.

Still waiting in the wings is Slate and Atkin's newest effort, Chess 5.0. At this writing, this version is not ready for competition. The rewritten program uses the venerable FORTRAN language.■

Association for Women in Computing

It has been announced that the AWC (Association for Women in Computing) was founded on December 5 1978 in Washington DC. The purposes of AWC are:

- to promote communication among women in computing;
- to further the professional development and advancement of women in computing;
- to promote the education of women and girls in computing.

Membership in AWC is open to all persons interested in the purposes of the association regardless of sex, race, religion, or national origin. To obtain further information and/or a membership application, contact Anita Cochran, 5A137 Bell Laboratories, Murray Hill NJ 07974.■

Automated Shopping List

During the past Christmas season, an interesting computer application was demonstrated at the Mall of New Hampshire in Manchester. The Digital Equipment Corp retail store there set up three DECstation 78 computer systems for use by shoppers. Each system executed a program for an automated shopping list. Each user answered four questions about a gift recipient, and the computer selected appropriate gifts from a data base contained on floppy disks. The selections were printed out in the form of a list of 20 suggestions.

The data base was created from gift selections submitted by the various stores in the mall in each of the several categories. An exemplar of a gift suggestion list is reproduced here. The list is specified as being appropriate for a female, 18 years of age or older, in the price range of $20 to $50, in the category of general presents.

It is estimated that over 1000 people per day used the system. The DEC store has received many inquiries about the system, and no doubt many such systems will appear in other locations. The program used in the system was written in the DIBOL language. The processor unit in the DECstation 78 is a microcomputer version of the venerable PDP-8.■

MERRY CHRISTMAS FROM THE DIGITAL STORE!
OUR COMPUTER HAS PROCESSED YOUR DATA AND SUGGESTS THE FOLLOWING GIFTS:

STORE	DESCRIPTION OF GIFT	PRICE
WEATHERVANE	PLAYGIRL SHOULDER BAG	23.00
FILENE'S	E LAUDER PVT COLLECTION 1/2 OZ	45.00
KARTEN'S	PORCELAIN FIGURINES	50.00
BRAZIL CONTEMPO	LIMITED PRINTS	50.00
GREAT EXPECTATIONS	GIFT CERTIFICATE FOR PERMANENT	25.00
LONDON HARNESS COMPANY	AUTHENTIC SCRIMSHAW	25.00
THE GREAT INDOORS	TEA SET	23.50
SCANDINAVIAN DESIGN	IMPORTED BASKETS	25.00
PHOTO CORRAL	800G SL1K TRIPOD	26.95
JOY OF COOKING	COPCO COOKWARE	22.95
TARRANT'S CUTLERY SHOWCASE	KING'S ARMS 2PC CARVING SET	37.50
SEARS ROEBUCK AND CO.	DIGITAL CLOCK RADIO	44.95
LAMP AND SHADE WORLD	STAINED GLASS TIFFANY LAMP	49.99
C.B. PERKIN'S TOBACCO SHOP	PARKER CUBE TABLE LIGHTER	29.95
QUALITY PETS	COMPLETE DOG GROOMING KIT	26.99
FABRIC GALLERY	STUFFED CHILDREN TOYS	25.00
BROOKSTONE	BRASS FIRST MATE'S LAMP	37.50
ABUNDANT LIFE WOODSTOVES	CAST IRON TEA KETTLE	29.95
LECHMERE SALES	GE DIGITAL SCALE	39.88
BREWSTER GLASSMITH	HANDMADE GLASS SEWING MACHINE	22.50

THANK YOU FOR SHOPPING AT THE MALL OF NEW HAMPSHIRE

Continued from page 10

I am just reaching the point where I can remember that TH is a search mode and ZA is the number of characters in a word. This is particularly regrettable in a program with avowedly pedagogical purposes. I shall refrain from belaboring the similar confusion caused by the program's use of GOTOs.

Finally, I am sorry that the authors did not comment generally on the memory requirements for the program, its performance, and the question of high versus low level languages for competitive chess programs. Still, it is an exciting series and I look forward to adapting the program when my Western Digital Microengine arrives.

David A Mundie
104-B Oakhurst Cir
Charlottesville VA 22903

ATTENTION ATARI EXPERTS

I am getting started in home computing. I have an Atari video computer with interchangeable game cartridges and controls. Is it possible to modify this so that I can write small programs on it? If anyone has done this, I would appreciate being sent some directions on how to do it. (I have some experience in putting electronic kits together.)

If these modifications are not feasible, does there exist a plug-in cartridge for playing chess? It seems to me that the 12 key keyboard or the 10 pin connector could be made to handle chess functions. I would appreciate help and advice from your readers.

Paul Rensink
POB 247
Ashton IA 51232■

DIGICAST: A CORRECTION AND AN OPINION

I would like to make a couple of corrections to the otherwise fine article by A I Halsema regarding "The Digicast System" in January 1979 BYTE, page 100.

- The explanation offered for the functioning of the standard FM Multiplex transmission and reception system needs clarification. What is commonly referred to as the stereo pilot signal is a signal sent to the FM tuner at 19 kHz from center frequency, which acts as an *on-off* switch for the tuner's demultiplexing section. In the presence of the 19 kHz pilot, the tuner will attempt to combine the difference signal being sent in the 38 kHz band with the summary monaural signal to derive two channels [algebraically, $(L + R) \times (L - R) = (L^2 - R^2)$]; in the absence of the pilot, the monaural signal is fed to both preamplifier channels.
- I highly doubt that, in practice, one could realize a full 6 M bit data rate on a UHF television channel where the full channel bandwidth is only 6 MHz total. The realities of broadcast transmission and reception would probably yield a service operating at less than half this frequency (I would guess 2.0–2.5 M bps tops).

Neil D Weiser
81 Horton St
Stamford CT 06902

CAN OUR READERS HELP?

I would appreciate information concerning any suppliers of an IBM compatible Magnetic Card II reader which may be interfaced to a microcomputer which uses the S-100 bus.

Ray Menzies
3/545 St Kilda Rd
Melbourne 3004
AUSTRALIA

Any BYTE reader with appropriate information is requested to correspond with Mr Menzies.

TEXT EDITOR

Your editorial "On the Virtues of Writing Editors" (November 1978 BYTE, page 6) prompted this letter to the editor. It seems that we have been reinventing the same wheel. I began writing my text editor about nine months ago—after becoming sufficiently frustrated with the Teletype-oriented editor purchased when I first got my system running. I have actually intended to write this letter since I read your earlier editorial asking for a better text processing system. However, I have been busy completing my doctorate during the period when the program was being developed so other things have also occupied my time. Many of your ideas were incorporated into my program. Here is a description of my editor.

Videowriter is a video display oriented text editor. I wrote it for the most common hobbyist systems (16 lines of 64 characters) but it is easily modified for other page lengths, and can be modified for other page widths (it is very easily modified for the Sorcerer size screen). It is an expandable program designed to have extra features added on as desired by the user. A complex split screen video driver for a memory mapped video display and a keyboard input routine using three flashing cursors are incorporated into Videowriter so that support software external to the program is not needed.

The screen is divided into a text display area and a command and message

display area. The text area is the bottom 13 lines of the screen. A flashing cursor indicates the position at which the next operation in the text buffer will occur. This cursor changes to different figures for either the text input mode or the command mode so the operator can tell at a glance which mode is in effect. The cursor can always be moved at will—left, right, up, and down. Left and right movement stop at the end of the line, and the cursor can move to any of the 13 text lines displayed. If the operator attempts to move the cursor off the top or bottom of the screen, text is scrolled onto the screen (scroll down or scroll up) form the text buffer. A direct one-to-one correspondence is always maintained between the screen text cursor position and the text buffer pointer position. To illustrate the use of the cursor, imagine that you are entering text and notice a misspelled word several lines up on the page. Without changing operating modes, move the cursor up to the line containing the error and then over to the wrong letter, positioning the flashing cursor over the error. Touching the delete key (or any other key so defined at assembly) removes the letter and the line beyond the cursor moves back one place. Now simply type in the letter or letters desired. The line moves to the right to make room. If the line becomes too long for the screen width it is split into two parts at the cursor position, and you continue entering on the same line. If you come to the end of the screen line an automatic carriage return and line feed is executed. If you were part way through a word at the end of the line the entire word will be entered on the next text line, and you simply keep typing. When a letter is entered in the last position on the screen line the cursor wraps around to the start of the next line to signify that that is where the next letter will go. A cursor-left from this "65th" position will move back up to the last line entered just as if the cursor was actually on the same line (in the text buffer it is). The cursor *always* indicates where the next insertion or deletion will occur. The operator does not need to enter a carriage return at the end of the line—this is done automatically.

Text lines in the text buffer are terminated by a single carriage return character. Actual line length varies from the single carriage return up to 64 text characters and a carriage return. This buffer arrangement is the most memory conservative arrangement that I could easily implement. Any byte (hexadecimal 00 to FF) can be entered into the text buffer.

Videowriter features user set, variable tab stops that work exactly like tab stops on a typewriter. 16 tab stops are allowed—and they can be set at any line position.

The top line of the screen is used for messages from the editor to the operator. If more tabs are entered into a line than there are tab stops set in the tab stop buffer the message TAB STOP NOT SET appears in the upper left corner of the screen and the system's bell is sounded. Similar messages annouce other user errors and undefined conditions.

The command mode of operation allows the operator to manipulate the text through the execution of command strings. Commands are all single letter entries (upper or lower case) made on the third line of the screen. Command characters do not have to be separated by a delimiter, but a delimiter $ is used to separate groups of commands. Each group delimited by a $ will be repeated as a loop according to the number preceeding the group on the command line. For example:

9999asdf$23ERT$h$121K$$

will be interpreted in the following way.

1. Execute the commands A, S, D, and F; and repeat 9999 times.
2. Do E, R, T 23 times.
3. Do one H; execute L and K commands.
4. Stop.

After the command string is entered on line 3, the two dollar signs $$ signal the start of execution. The line is first moved up to line 2, and then the commands are actually read from the video memory and executed. If the operator makes an error another command string can be entered on line 3 with the previous string still visible on line 2. Existing line 2 command strings can be repeated, and line 3 command entries can be deleted singly or the entire line can be erased. The command line cursor indicates where the next command line entry will go. A text cursor indicates where the next command will have effect in the text buffer. For example, the delete command will delete characters starting at the current text cursor position.

There are two types of commands. The 26 single letter commands are reserved for use on the command line as described above. These commands are decoded in sequence and a vector is found in a table. The user can place any vector in this table and the editor will then call the user's routine. A number of immediate commands are implemented using the set of ASCII control characters. A control E initiates the text enter mode. A control C halts execution of any command mode string (if the user has written it into the routine!) and returns to the command mode with a *BREAK* message and a bell. Control R deletes the entire line 3 command string entry. A control X returns to the monitor or operating system. The control Z command causes the next character entered from the keyboard to be entered into the text buffer, regardless of any assigned function of the character.

Videowriter is constructed in two parts. The core program does the housekeeping for the features described above (except for the delete command). None of the 26 single letter commands is used by the core program. (Control T initiates the tab set or clear routine.) All of the immediate commands are processed by the core program. Text buffer entry or delete, cursor positioning, screen scrolling, and keyboard entry are managed by the core. Decoding of the 26 single letter commands, command line execution and loop control is done by the core, and control is passed to the vector in the command vector lookup table. Undefined commands return control to the command processing routine.

The other half of Videowriter is a user expandable set of extension routines vectored to by the core program. The user's routine does not need to save any registers or the stack pointer position, but the address on the stack when the extension routine is called must be saved. This is the return address to the command processor. Input and output routines are obvious candidates for the extension routines, since these routines must be tailored to the user's individual disk or tape system. The normal editor functions to search for strings, substitute strings, delete text blocks, copy blocks, move blocks, etc, are implemented in the extension routines.

The character delete routine is a good example. The single letter D or d causes one character to be deleted from the text buffer. D100 will delete a block of 100 characters. 100D will delete 100 characters one at a time, with the results displayed on the screen after each deletion. 30D100 will delete 30 blocks of 100 characters each. The D\ command simply searches from the current pointer position toward the end of the text, looking for a special stop character in the text buffer. Text is then deleted from the cursor to the stop flag, or to the end of text if no flag is set.

The 0\ command outputs from the buffer from the cursor to the stop flag or end of text, and the 0 command saves the entire buffer. The move command moves a block, from the cursor to the stop flag, to a position marked in the buffer by a special flag. The function requires only one byte more than the original buffer size, regardless of the size of the block moved. Copy works similarly except that the original block is not destroyed. It appears that there will be about ten unused command vector positions left in the command vector table for the addition of user functions. These could be used to implement text output processing extensions.

It is my intention that Videowriter be used by simply pointing the cursor and then performing the function doing it without having to count lines or places, etc. All changes to the text buffer are displayed. It has always seemed obvious to me that this is an absolute requirement for a text editor, but I have never seen another program that does as much for the operator as Videowriter. Since no one else had what I considered to be a "decent" editor, I wrote it myself!

Of course, the current implementation of Videowriter doesn't satisfy me completely. It has one major drawback which must be fixed—the more text between the cursor position and the end of text the slower it runs (block transfers are slow). If text is being entered with 16 K bytes of text following the cursor, a fast typist can enter characters faster than Videowriter can put them into the buffer. This will be fixed by using a line input buffer so that no more than 64 characters will be moved at each entry until the line is full. Nested command loops will be added, probably before you receive this letter. This will allow true macrocommand loops to be entered and executed.

Only two simple routines are needed to allow nested command loops, with no changes to the current command processing scheme. Currently, only 9999 iterations of each loop are allowed, but this will be changed to allow 65535 passes. That should be enough to satisfy anyone! I want to add a display at the upper right corner of the screen to show the workspace remaining. The tab set and clear routine must be modified to display the position number of each tab stop. And, finally, I eventually want to add a separate command buffer so that huge macrooperation can be executed. The command buffer contents will be saved and loaded just like the text buffer. These are all changes to the core program, and should take another month or two at the most.

Do you like it? Do you have any suggestions for further additions or modifications? If you do I would certainly appreciate your opinions. Of course it isn't complete (as I would like it) now, but it works—and, of course, I am using Videowriter to write this letter! Virtually all of the extensions need rewriting to speed them up. I forgot to mention one point: Videowriter was assembled in TDL's pseudo-8080-like, Z-80 mnemonics. Since most of the op codes are 8080 op codes, rewriting for the 8080 will be simplified. I have machine reproducible flow diagrams for all of Videowriter which are fairly compact—more so than flowcharts.

I will appreciate any comments. Videowriter will soon be running on several other systems so I can get other opinions.

Phillip Hays
Apt 46
825 NW 23rd St
Corvallis OR 97330■

R Travis Atkins
67 Greenend Av
Middletown RI 02840

What Is an Interrupt?

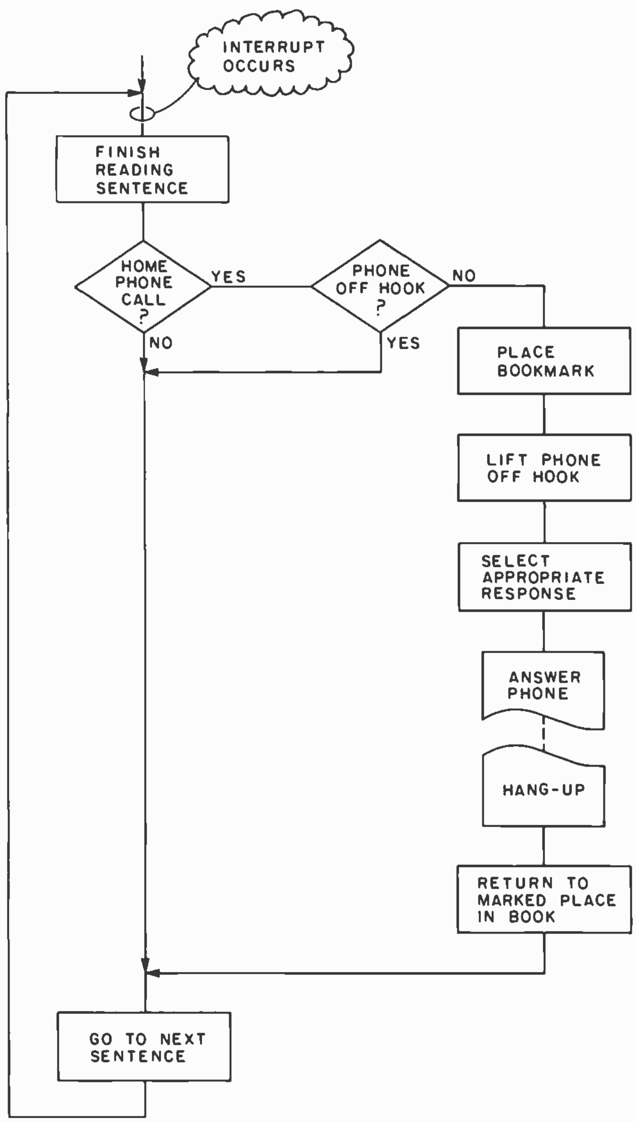


Figure 1: One example of a way to handle a human being's interrupt processing in response to a ringing bell. The ringing bell is like a signal on a multiple source interrupt line of a computer. The first object is to identify the source of the interrupt. If processing is done, the state of the interrupted process (reading a book here) is saved (with a bookmark) while the phone is answered. After the phone call, the reading of the book may be resumed at the place of the bookmark, restoring the original process.

Busy work! It's a terrible thing to inflict on people or computers. Wait loops in input or output operations are busy work for computers, and unless you learn how to tap your computer on the shoulder when you need it, it will probably spend most of its time doing busy work.

As hobbyists, we are always concerned about squeezing the greatest value out of our investments. We want our computers to run as efficiently as possible. Since it is likely that we will be involved in designing and building some of our own IO devices, we should develop an understanding of the concept of interrupts. To efficiently program peripherals for IO purposes it is often necessary to use interrupts.

This article introduces the basic concepts of interrupts, defines the terminology that applies to interrupt mechanisms, and describes the processing events that must occur during the time from the receipt of an interrupt to the return from that interrupt.

Concepts

An excellent example of interrupt processing is the system used in telephones. Let's see why.

We know when someone is trying to call us because the telephone rings. But consider how much time would be wasted if we had to periodically pick up the receiver to see if anyone was on the telephone if the phone had no bell. This periodic method is called *polling;* it works well for telethons and radio talk shows. However, it's not the best method for normal home telephone installations. Assume you receive an average of one or two phone calls a day at home. Imagine yourself as a processor and the callers as the IO requests from a keyboard. The order of magnitude differences in this example are about the same as with your processor and its IO. The bell on your telephone is, of course, an *interrupt.* It is an

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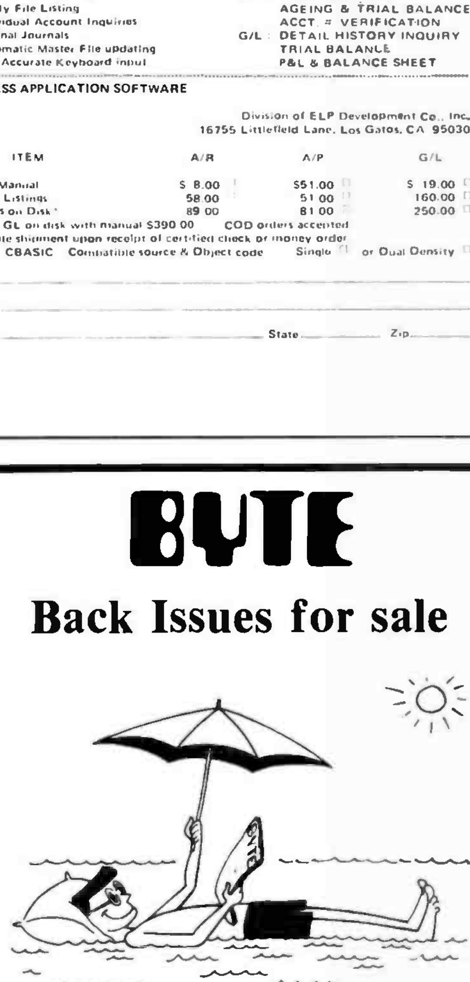

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excellent way to resolve the asynchronism and speed differentials of the telephone communications system. Interrupts can resolve the same fundamental mismatches for computers as well.

Terminology

Let's carry this analogy a little further to introduce the terminology that refers to variations of the basic interrupt concept.

If your phone is ringing, and you are about to process an interrupt, what are your reactions? How does your interrupt processing work?

More than likely, you will perform a sequence of actions precisely analogous to those your microprocessor performs when it receives an interrupt. Figure 1 is a flowchart of the typical procedure we would run through for a telephone interruption. It consists of both the *housekeeping* chores of switching from the background task you were doing, reading, to the interrupt task, answering the phone, and back again in an orderly and complete fashion, as well as the interrupt handler itself.

In the computer an interrupt is a special control signal that is sent to your microprocessor when a given asynchronous event, such as a switch closure, or an IO ready signal, is detected by your system. It is the mechanism by which your processor is forced to take note of that exceptional event.

The interrupt causes your processor to transfer control to a set of instructions known as the *interrupt handler.* The interrupt handler is nothing more than a precoded contingency plan in the form of a subroutine that may be called at any time in response to an interrupt signal. What you do in this subroutine is limited only by the software capabilities of your processor.

In microprocessors, interrupt processing is basically a software technique with varying degrees of hardware support depending on your particular processor and system. The term *vectored interrupt* refers to a simple method of reacting to an interrupt. The processor is sent to the interrupt handler which will lead the processor through steps to determine the source of the interrupt, initiate appropriate actions and return to the point of interruption. The *vector* is simply the starting address of the interrupt handler, and is supplied either externally or internally, depending upon your particular processor's hardware.

Microprocessor integrated circuit designers who seek to minimize the hardware requirements in their processors often assign a fixed location or set of locations in the processor's address space to hold the vector(s). The 6800 processor uses this approach, as does the Texas Instruments TMS-9900. Other processors such as the 8080 receive their vectors directly from external sources, a method which usually involves more system hardware.

The built-in process that occurs in your microprocessor chip is usually limited to saving the program counter and the processor's status register, masking subsequent interrupts, and then *transferring control* to your interrupt handler (loading the program counter with the interrupt handler's starting address). The task of determining where the interrupt came from is left to the interrupt handler itself. In the simplest case, where you have only one device tied to an interrupt line, the origin of the interrupt is implied. Since we may at some time have more devices than we have separate interrupt lines, we should also know how to make a more sophisticated system capable of handling many devices.

To see how multiple interrupts are handled, consider another analogy. Assume you had just settled back into your easy chair after finishing with the telephone interruption, when suddenly a pair of hands covers your eyes and a voice says, "Guess who?" You've been interrupted again, and you don't know which of your 12 children it is, so you will have to save your place again, and begin by saying, "Is that you Olen?". . ."No.". . ."Is it you Travis?". . . "No.". . ."Is it you Mary Ellen?". . .etc, until you get a positive response. In much the same way, several devices can use a single common interrupt line to your processor so that, once the interrupt handler is initiated, it can interrogate all the devices to see which one sent the interrupt signal. To accomplish this, it is customary to have a *device status register* in the microprocessor's address space for each individual device. The data in this location indicates the device's current status: busy or ready.

Now suppose this game of guess-who is very popular with your children, and they are all playing it on you, some much more often then others. Your best strategy would probably be to adopt an ordering scheme *to optimize* the handling of these many interruptions. This simply means that you would guess the names of the children who were the most frequent players first, and check the least likely ones last. Similarly, in interrupt processing you should arrange the order of checking the device status registers of your IO units from the most frequent source of interrupts to the least frequent. By ordering your interrupt servicing this way, you can add significantly to the efficiency of your system.

By now you've probably realized that the idea of letting multiple devices share one interrupt line is problematical: two devices may want to interrupt the processor at the same time. In terms of our analogy, all 12 of your children may want to play the guess-who game with you at the same time. The way to handle this situation is to say, "Hold it! I will play the game with each of you. . .but only one at a time." By doing this you act on one interrupt while you *mask out* the rest.

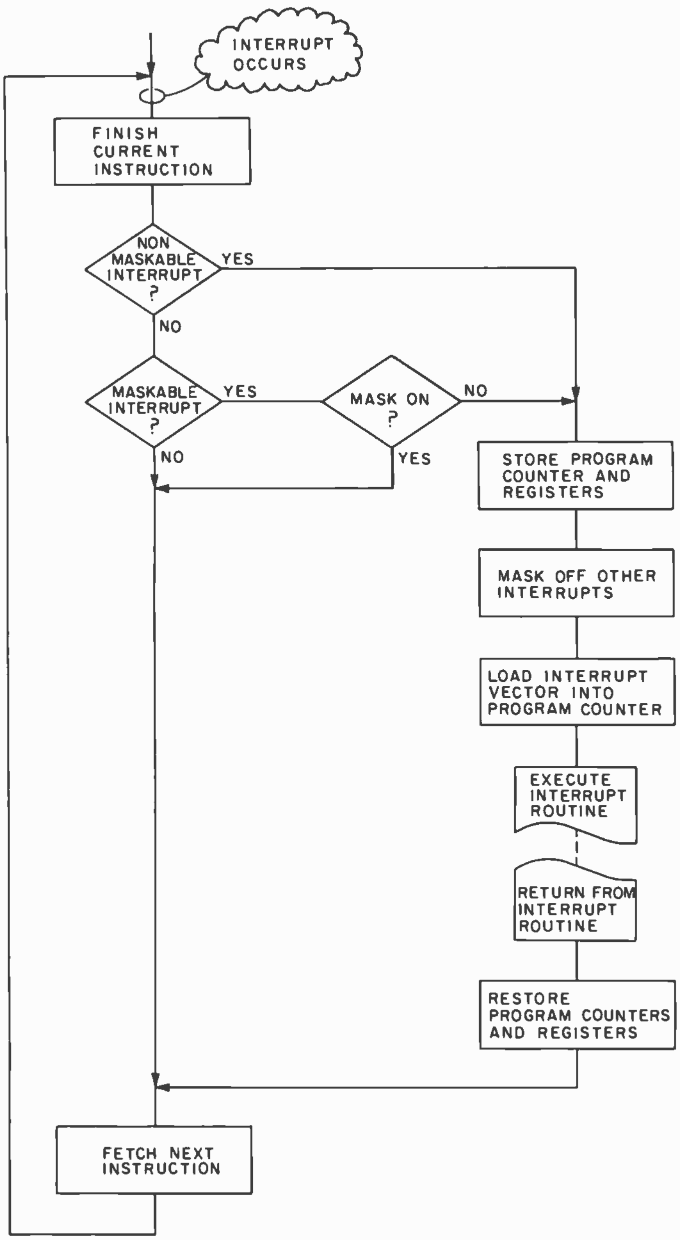

Figure 2: Analogous to the human interrupt processing of figure 1, the typical computer's interrupt processing activities are shown by this chart. The differences between the two figures (1 and 2) are largely in the activities described in each box; the form of the processing logic in this particular set of examples is nearly identical.

The concept of *maskable interrupts* is incorporated in many of today's processors. There is usually a mask bit or bits used to block or *mask* the interrupt signal from the processor. This masking is frequently part of the built-in process on your microprocessor chip to protect the function of saving critical information, such as the program counter and status register, from subsequent interrupts. Once masked out, your system's design will determine if a subsequent interrupt will be held pending or lost. Interrupts that are kept pending are often referred to as *queued interrupts.* Sometimes circuitry external to the processor chip itself is used to give the pending interrupts an order of priority in much the same way as you might tell your children to line up in the order of youngest to oldest to play the guess-who game. The *N level priority* interrupt capabilities that are mentioned as features of microprocessor systems refer to this type of interrupt queuing. A higher priority interrupt that arrives after several low priority ones will usually bump the lower priority interrupts down in the queue.

For those cases where an interrupt must get the processor's attention right away, a *nonmaskable interrupt* is usually also provided in the chip's structure. This control line is for a very high priority function of your choice, which can override the maskable interrupts even if they are in progress. This is valuable for very high speed IO, such as a floppy disk unit, and for hardware emergencies such as fire or power loss routines. Your system reset is usually a nonmaskable interrupt.

Mechanisms

Now that you have a feel for the terminology, let's take a look at the mechanisms and processing that are common to all interrupt routines. Figure 2 is a typical flowchart of the functions necessary to accomplish the transfer of control from the background processing to the interrupt handler and return. You may think of this as putting the background process "on hold" while the interrupt is processed and recommencing the background process when it returns. The background process is not affected by what has happened; thus the interrupt processing is completely transparent to the background process and may be executed at any time without fear of disturbing it. The only definite change is

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Table 1: The following list of responsibilities must be jointly met by both the programmer and the system being programmed, if interrupts are to be properly handled. The key item to remember is that when the interrupt occurs, the critical data values which determine the state of the machine *must be saved so that at the end of the interrupt process, the original process can be resumed "as if the interupt never happened."*

- Sensing an interrupt signal and determining appropriate response.
- Setting the mask to protect the processor from subsequent interrupts.
- Note where you are by saving the program counter and status register.
- Transferring processor control by loading the program counter with the interrupt vector address.
- Executing the interrupt handler which may:

  save accumulator(s).
  save index register(s).
  save pointers(s).
  search for interrupt source.
  satisfy device request.
  restore pointer(s).
  restore index register(s).
  restore accumulator(s).
  clear the interrupt mask.

- Resume normal processing by restoring the program counter and the processor status register.

that the background processing will slow down somewhat because the processor has to take extra time to service the interrupt(s). As a result, any real time clocking in the system will be offset by that interrupt processing time.

The joint responsibility of the processor and you, the interrupt routine programmer, is to insure that the background process is not disturbed. These responsibilities are simply stated in table 1.

Within the interrupt handler it is not always necessary to save all of the working registers for every interrupt, but you must at least save and restore every register used in your routine.

Deciding when to remove the interrupt protection (clear the mask) is your responsibility. The key is to pick a point which comes after the saving of the critical registers. The mask shouldn't be removed in the middle of your interrupt routine unless the routine is *reenterable.* Reenterancy is a term that refers to software routines that find new memory locations to store their working data each time that they are reentered before they have been exited. The significance of this is that if you clear the mask and a subsequent interrupt arrives, stops your current interrupt processing, and begins to use the same interrupt routine you were just using, you must ensure that it doesn't destroy your current working data. The safest procedure is to stay masked throughout the interrupt processing until you become experienced with the reentry software techniques. Figure 3 shows the division of these interrupt processing duties for a typical microcomputer system.

If your processor's monitor was supplied by the manufacturer, there is much to be learned from studying its interrupt handler section. Look for the methods used to accomplish the basic steps we have outlined above, then write your own simple interrupt handler, modify the interrupt vector to point to your routine instead of theirs, and execute your interrupt handler.

Once you have done this successfully, you will have developed an appreciation of how the modern digital computer, large or small, services the requests of so many peripheral devices seemingly simultaneously. Understanding interrupt driven processing, which is the central concept of computer operating systems, will help you to grasp the awesome power that lies within your own personal computing system. ■

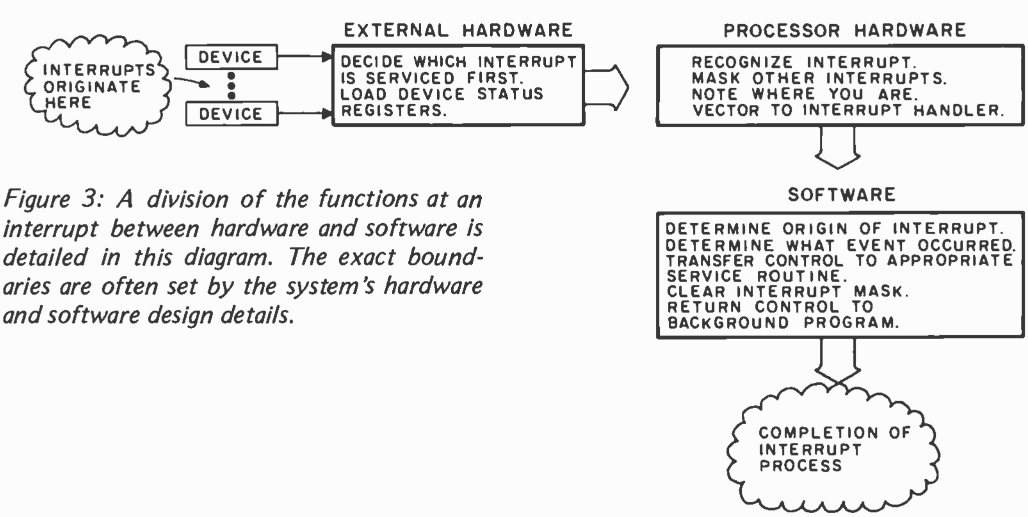

Figure 3: A division of the functions at an interrupt between hardware and software is detailed in this diagram. The exact boundaries are often set by the system's hardware and software design details.

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History of Computers

Keith S Reid-Green
Technical Staff
David Sarnoff Research Ctr
Princeton NJ 08540

The 650 was the most popular IBM computer during the 1950s until it was supplanted by the 1401 at the end of the decade. The machine was used widely by small banking, accounting and insurance companies which did not require the capabilities of the relatively powerful 705, and it is safe to say that IBM's current share of the commercial data processing market got its initial impetus from the successful marketing of the 650. However, the sophisticated personal computer user of today wouldn't give a passing glance to a machine of its capabilities.

The original 650 consisted of three units: the power supply, console and card reader/punch. Later modifications allowed for the addition of an on line printer and magnetic tape units, but the original 650 was strictly cards in and cards out. A tabulating machine such as the 407 was therefore required to produce printout, but this system was not satisfactory from financial and ecological points of view, since punching cards as an intermediate step to a printed page is very wasteful. The really bad news, however, was storage. Either 1000 or 2000 10 digit decimal words could be stored on a magnetic drum in bands of 50 words, each band having its own read head. Since the drum rotated at 12,500 revolutions per minute, average access time (half a revolution) was a little less than one hundredth of a second, or in modern terms 9,600,000 ns.

The problem of rotational delay could have been a serious detriment to processing speed except for a very clever assembly program. Modern computers using random access memory are programmed on the assumption that, in the normal course of execution, instructions are stored in consecutive locations. Had this been the case on the 650 it would have reduced processing speed to roughly one instruction per drum revolution, or 12,500 program steps per minute, because the processor was not fast enough to process an instruction in less time than it took for the next instruction to pass under the drum's read heads. However, instructions consisted of an operation code and two addresses; a data address and a next instruction address. Theoretically, the programmer could organize an optimum way to store the finished program so that the completion of each instruction coincided with the arrival of the next instruction under a read head. Since execution times varied from one instruction type to another, it was very difficult to optimize a program by hand.

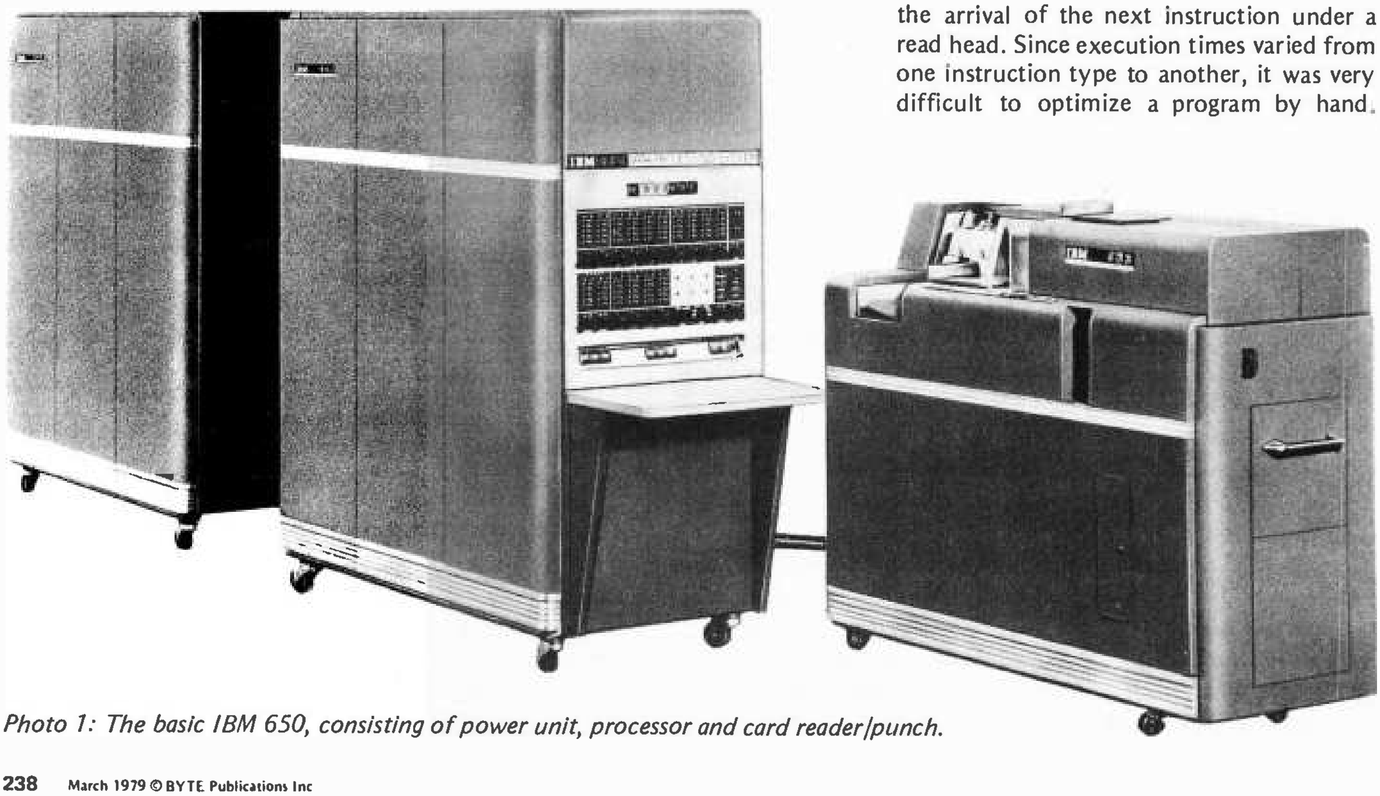


Photo 1: The basic IBM 650, consisting of power unit, processor and card reader/punch.

The IBM 650

Fortunately, the SOAP assembler (SHARE optimum assembly program) did a pretty good job of optimizing the object programs it produced.

The instruction execution process was accomplished through a minimal number of registers (see figure 1). An instruction was brought from the drum to the program register, where the operation code and data addresses were passed on to the 2 digit operation register and 4 digit address register. If necessary, the data word specified by the address register was brought to the distributor, where it may have been used in conjunction with the lower or upper accumulators (the accumulators were logically considered as a 20 digit number separated into upper and lower halves). Then the instruction address was moved from the program register to the address register in order to process the following instruction.

Validity checking of numbers took place whenever they were transferred among registers or to the drum. Digits were stored in biquinary form, requiring seven binary bits per digit, in which one of two bits represented either 0 or 5 and one of the remaining five bits represented 0, 1, 2, 3 or 4. The sum of the two "on" bits could therefore represent the digits 0 thru 9 and the validity check ensured that exactly one bit of the pair and one of the group of five was "on."

Given the other constraints of the 650, the instruction set was reasonably complete, including read and punch, branching, add, subtract, multiply and divide, shifting and even a table lookup instruction. Routines

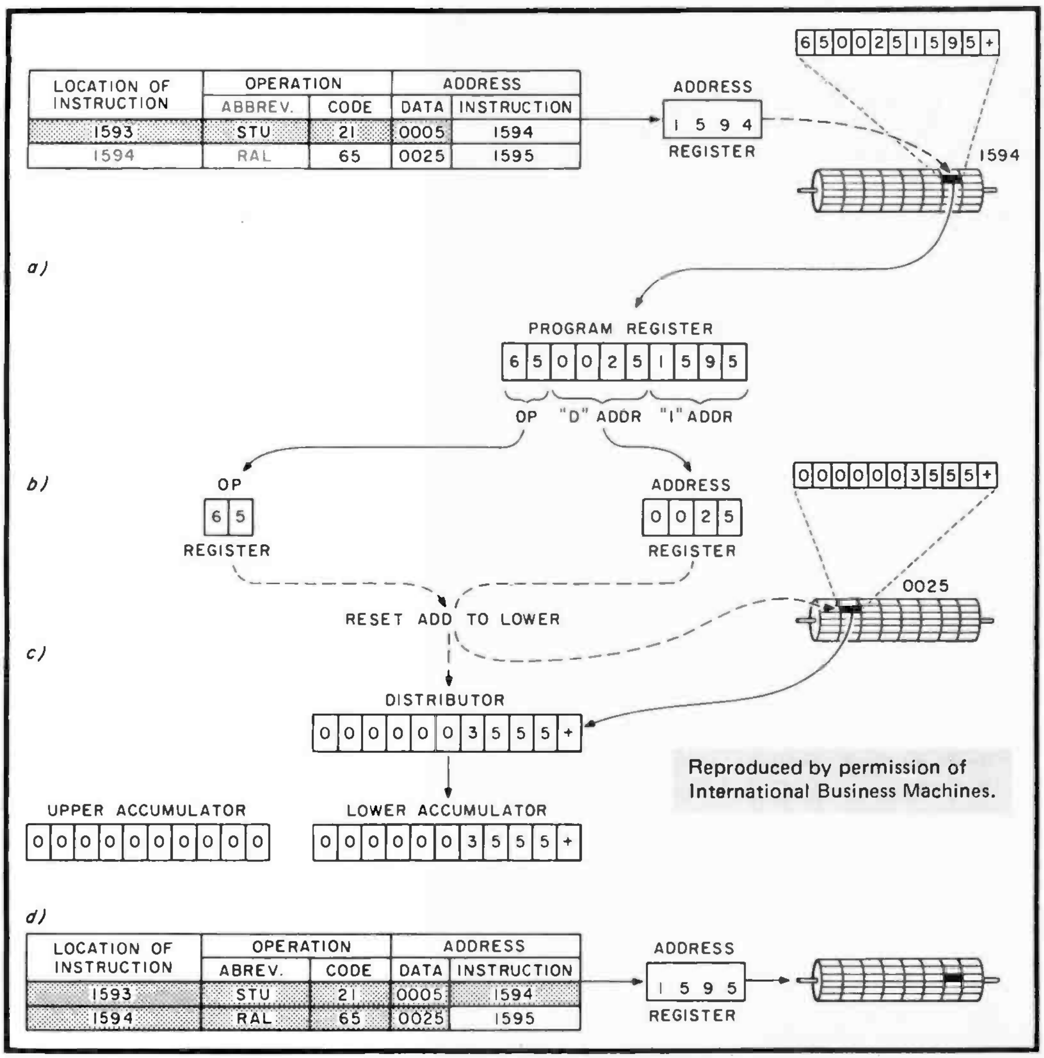


Figure 1: The instruction execution cycle of the IBM 650.

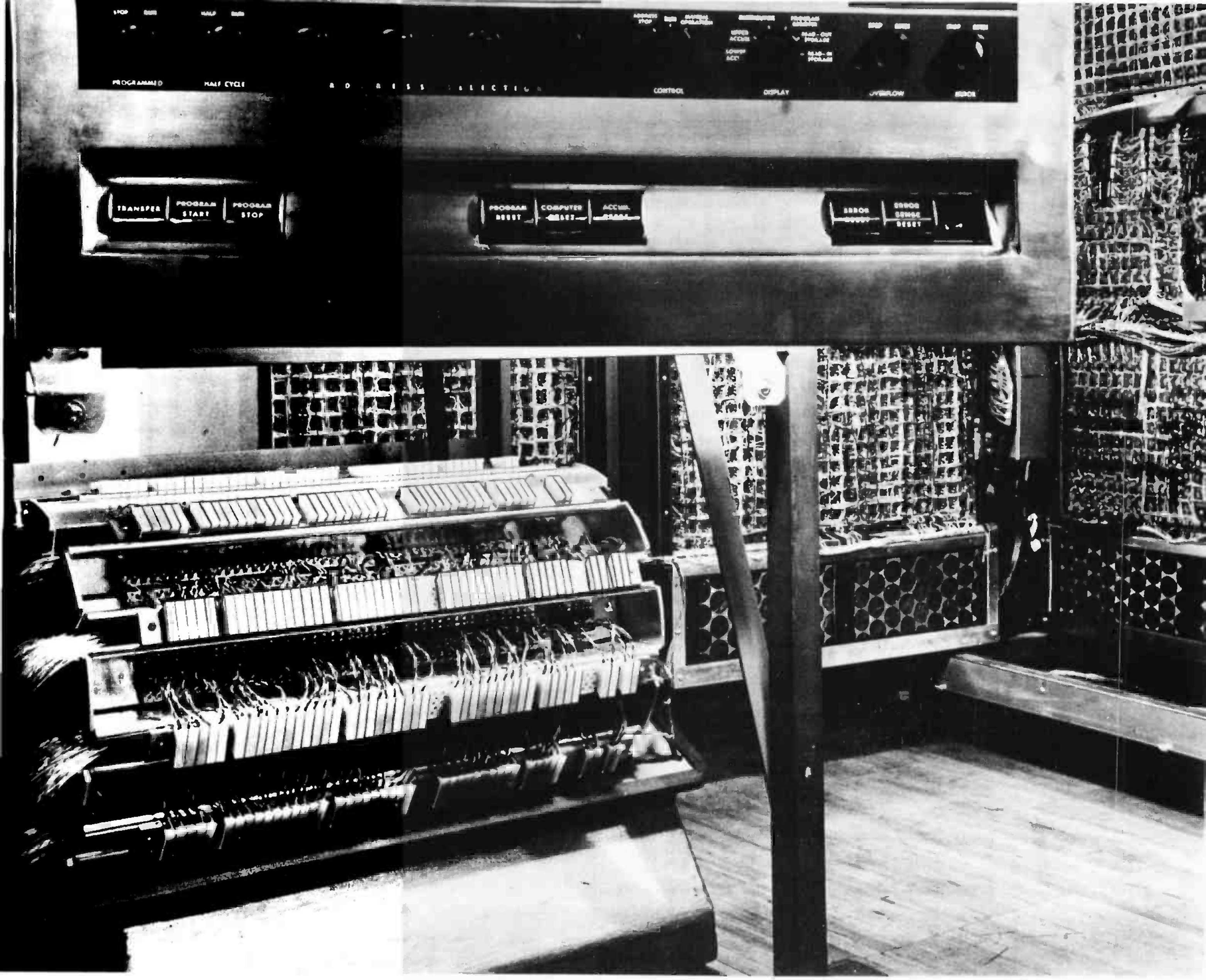


Photo 2: The magnetic drum memory showing positioning of the read heads.

to simulate floating point were available through the SHARE user group, but they were slow in operation. In most cases it was preferable to assume decimal point positions and to use shift instructions to align them before adding.

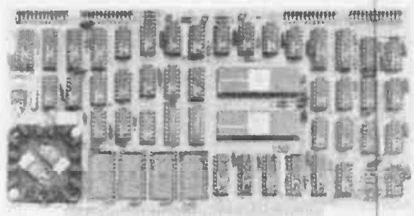
Input and output were restrictive and clumsy due to reliance on punched cards. Even in the later days of the 650 when magnetic tapes were available, flexibility was not greatly increased. Since tape was faster than the drum, a core memory buffer of 120 words was used, and all tape records were of this length.

The biggest problem of all was the small memory. 2000 10 digit words cannot be equated exactly with, say, 8 K bytes. While five alphabetic characters could be stored in one 650 word, each number and each instruction took up a full word. In a personal computer having a 16 bit word, a program of 2000 instructions takes less than 4 K bytes. It would have completely filled the memory of the 650.

Given all these failings, why was the 650 so popular? Because it was the only minicomputer that IBM made at that time. Although Burroughs built the 205 at about the same time, no company except IBM had established itself as a viable computer manufacturer (in 1959 IBM had about 90% of the computer market). Furthermore, the 650 was seen as a natural replacement for punched card calculators like the 602, which were used in conjunction with the so-called electric accounting machines, sorters, collators and tabulators, to handle payroll and accounting problems. Clearly, at a rate of $600 per hour, the 704 or 705 could not be used by smaller businesses. The 650 cost about $50 per hour, which nowadays is a preposterous rate for such low computing power, but in the 1950s was the only answer to the computing needs of small businesses.■

What's New?

4 MHz Single Card Computer



Cromemco's Single Card computer features the Z-80 processor and S-100 bus architecture. The card offers 4 MHz operation, 8 K bytes of on board 2716 programmable read only memory and 1 K bytes of static programmable memory. It also provides an RS-232 (or 20 mA current loop) serial interface with programmable transmission rates up to 76,800 bps, 24 bits of bidirectional parallel input and output (I/O), five programmable timers and vectored interrupts. Only a power supply and programmable read only memory software are required for operation. The Single Card computer can also be the core of an expandable S-100 bus system that can include additional memory, I/O, or even floppy disk drives as required.

Cromemco's Z-80 Monitor and 3 K byte Control BASIC are available in 2716 read only memory for use with the Single Card computer. With these two memories, the computer can be used immediately without any additional memory or I/O. The Monitor has 12 comments to aid in program development. The 3 K byte Control BASIC has 36 commands and functions and can directly access I/O ports and memory locations, and call machine language subroutines.

The Single Card computer is available in kit form for $395 and assembled and tested for $450. The Monitor and Control BASIC are available in two read only memories for $90. For additional information contact Cromemco Inc, 280 Bernardo Av, Mountain View CA 94040.■

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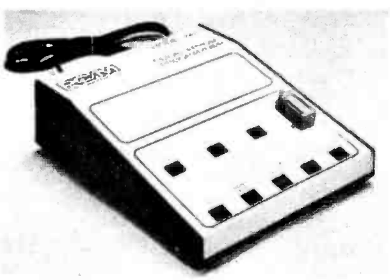
Intelligent Programmer for Intersil Ultraviolet Memory Chips



Pacific Cyber/Metrix Inc has announced availability of its new Model 660 programmer for the 6603 and 6604 4 K bit CMOS ultraviolet erasable read only memory integrated circuits from Intersil Inc.

The Model 660 programmer has been designed specifically for programming the 6603 and 6604 devices. The programmer contains a microprocessor and 4096 bit programmable memory and can be operated stand alone from its front panel or interactively with a video or Teletype terminal through the programmer's built-in RS-232 or 20 mA current loop interfaces. The Model 660 can also communicate with a computer for automated on line programmable read only memory programming.

Built-in features include a full complement of editing capabilities for loading and checking the programmable memory buffer or 660X erasable read only memory, ability to accept all popular paper tape formats, firmware for programmable read only memory copying and verifying, and a front panel erase check capability. Programming time is typically half of that required for similar N channel device programmers.

The Model 660 is priced at $645. Contact Pacific Cyber/Metrix Inc, 3120 Crow Canyon Rd, San Ramon CA 94583. ■

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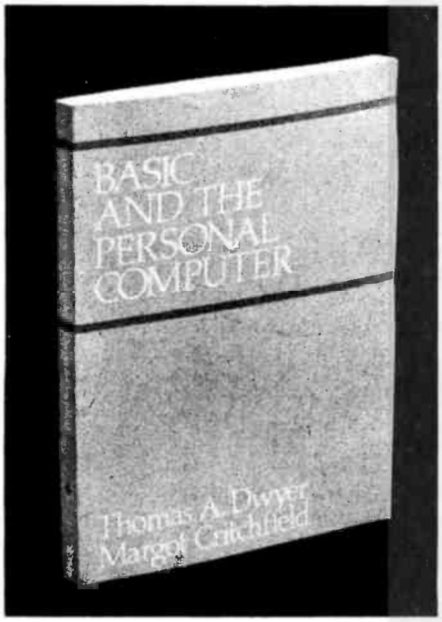
What's New?

SOFTWARE

New Book Explores Varied Facets of Personal Computing



BASIC and the Personal Computer by Dwyer and Critchfield discribes the uses of personal computers, then explains how to make these ideas become a reality by using the power of interactive computer programming. It features examples that cover a wide range of applications possible with personal computers.

Topics include microcomputer hardware, programming in BASIC and extended BASIC, computer graphics, word processing, data structures, sorting algorithms, computer games, computer art, simulations, business applications, color graphics and the use of special interface devices.

The book requires no previous experience with computing. The text is integrated with a large number of original illustrations that clarify both beginning and advanced concepts.

This 438 page softbound book is published by Addison-Wesley Publishing Co Inc, Reading MA 01867 for $12.95.■

Circle 630 on inquiry card.

Software Package for the North Star Disk System

The Program Utility Package (PUP) includes assembler and BASIC programs to enhance the usability of the North Star BASIC language. These programs use the input and output routines provided by the North Star disk operating system and the user. The package includes: CREF which is an assembler program producing a sorted cross reference of variable and function usage by line number; SMAP is an assembler program which produces a sorted map of line reference by GOSUB and GOTO; FLIST is an assembler program to produce a formatted BASIC program listing; MEMTEST is an assembler program which performs multiple memory diagnostics on user specified memory ranges; HEXMON is a BASIC program to load or list memory in hexadecimal. Each displayed line of 16 bytes of hexadecimal data also has the ASCII equivalents printed.

This package consists of six programs on a library diskette, 16 pages of documentation, and a diskette folder. The price of PUP is $25, with program listing available for an additional $7. For further information, contact Business Computer Systems, 216 Collier Dr, Springfield IL 62704.■

Circle 631 on inquiry card.

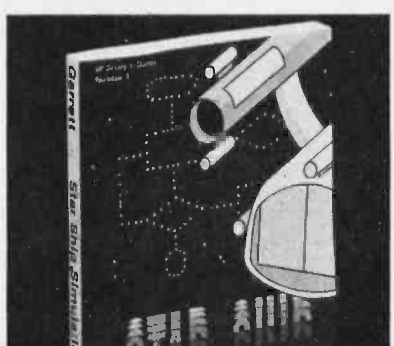
The Complete Star Ship: A Simulation Project

Star Ship Simulation by Roger Garrett explains the methods used in approaching the design of a software simulation. Readers become familiar with the techniques by which any large programming task can be implemented and learn how to attack a program in a straightforward, structured manner.

The first half of the book gives the reader a working knowledge of system design and program structure, and the last half deals with the actual development and implementation of the Star Ship simulation project. Details are given for every major function aboard a star ship as well as the intelligence of enemy and friendly space craft.

The 122 page book is priced at $6.95 and is available from Dilithium Press, 30 NW 23rd Pl, Portland OR 97210.■

Circle 632 on inquiry card.



Assembly Language Development System for 8080 or Z-80

PDS is an assembly language development system for 8080 or Z-80 microcomputers with at least one disk drive. PDS includes a unified assembler and editor, a macro-assembler combining the features of a relocating linking loader, a string-oriented text editor, and a trace debugger and disassembler.

The assemblers favor the Intel instruction mnemonics, treating the Z-80 superset as a logical and syntactical extension. The debug module features breakpoint or single step execution of programs with trace display of all register contents, flag status, a memory window, and the mnemonics of the instruction just executed and the next instruction to be executed.

Source modules are available for floating point arithmetic, floating point IO, trigonometric functions, numerical and alphabetic sorting, matrix inversion, fast Fourier transform and a full function expression evaluator.

The price is $99. For further information, contact Allen Ashley, 395 Sierra Madre Villa, Pasadena CA 91107.■

Circle 633 on inquiry card.

Micropolis CP/M System Upgrade

The Micropolis CP/M System Upgrade gives the Micropolis disk owner the full capacities of the CP/M disk operating system while retaining full access to Micropolis' operating system.

The CP/M System Upgrade allows the Micropolis disk owner to directly load and start CP/M and automatically execute a program at system start-up. Other features include dynamic disk space allocation and reclamation, random access on all files, high speed disk read and write and full compatibility with all other CP/M systems and software.

For further details, contact the Computer Mart of New Jersey, 501 Rt 27, Iselin NJ 08830.■

Circle 634 on inquiry card.

Word Processor for the Commodore PET

Connecticut microComputer has announced a word processor program for the Commodore PET. This program permits composing and printing of letters, flyers, advertisements, manuscripts, articles, etc, using the PET and an RS-232 printer.

Script directives include line length, left margin, centering and skip. Edit commands allow the user to insert lines, delete lines, move lines, change strings, save onto cassette, load from cassette, move up, move down, print and type.

The word processor program addresses an RS-232 printer through a Connecticut microComputer printer adapter. The program can be purchased for $29.50 from Connecticut microComputer, 150 Pocono Rd, Brookfield CT 06804.■

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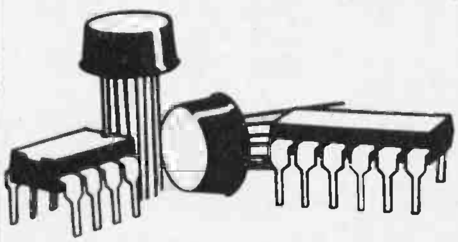

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SOLDERTAIL STANDARD (TIN)

14 pin ST	$.27	.25	.24	28 pin ST	$.99	.90	.81
16 pin ST	.30	.27	.25	36 pin ST	1.39	1.26	1.15
18 pin ST	.35	.32	.30	40 pin ST	1.59	1.45	1.30
24 pin ST	.49	.45	.42				

SOLDERTAIL STANDARD (GOLD)

8 pin SG	$.30	.27	.24	24 pin SG	$.70	.63	.57
14 pin SG	.35	.32	.29	28 pin SG	1.10	1.00	.90
16 pin SG	.38	.35	.32	36 pin SG	1.65	1.40	1.26
18 pin SG	.52	.47	.43	40 pin SG	1.75	1.59	1.45

WIRE WRAP SOCKETS (GOLD) LEVEL #3

8 pin WW	$.39	.38	.31	22 pin WW	$.95	.85	.75
10 pin WW	.45	.41	.37	24 pin WW	1.05	.95	.85
14 pin WW	.39	.38	.37	28 pin WW	1.40	1.25	1.10
16 pin WW	.43	.42	.41	36 pin WW	1.59	1.45	1.30
18 pin WW	.75	.68	.62	40 pin WW	1.75	1.55	1.40

1/4 WATT RESISTOR ASSORTMENTS – 5%

ASST. 1	5 ea.	10 OHM 12 OHM 15 OHM 18 OHM 22 OHM	27 OHM 33 OHM 39 OHM 47 OHM 56 OHM	50 PCS	$1.75
ASST. 2	5 ea.	68 OHM 82 OHM 100 OHM 120 OHM 150 OHM	180 OHM 220 OHM 270 OHM 330 OHM 390 OHM	50 PCS	1.75
ASST. 3	5 ea.	470 OHM 560 OHM 680 OHM 820 OHM 1K	1.2K 1.5K 1.8K 2.2K 2.7K	50 PCS	1.75
ASST. 4	5 ea.	3.3K 3.9K 4.7K 5.6K 6.8K	8.2K 10K 12K 15K 18K	50 PCS	1.75
ASST. 5	5 ea.	22K 27K 33K 39K 47K	56K 68K 82K 100K 120K	50 PCS	1.75
ASST. 6	5 ea.	150K 180K 220K 270K 330K	390K 470K 560K 680K 820K	50 PCS	1.75
ASST. 7	5 ea.	1M 1.2M 1.5M 1.8M 2.2M	2.7M 3.3M 3.9M 4.7M 5.6M	50 PCS	1.75

ASST. 8R Includes Resistor Assortments 1-7 (350 PCS.) $9.95 ea.

$5.00 Minimum Order – U.S. Funds Only
California Residents – Add 6% Sales Tax

Spec Sheets – 25¢
1979 Catalog Available—Send 41¢ stamp

NEW 1979 Catalog

Jameco ELECTRONICS

PHONE ORDERS WELCOME (415) 592-8097

MAIL ORDER ELECTRONICS – WORLDWIDE
1021 HOWARD AVENUE, SAN CARLOS, CA 94070
ADVERTISED PRICES GOOD THRU MARCH

TELEPHONE/KEYBOARD CHIPS

AY-5-9100	Push Button Telephone Dialler	$14.95
AY-5-9200	Repertory Dialler	14.95
AY-5-9500	CMOS Clock Generator	4.95
AY-5-2376	Keyboard Encoder (88 keys)	14.95
HD0165	Keyboard Encoder (16 keys)	7.95
74C922	Keyboard Encoder (16 keys)	9.95

ICM CHIPS

ICM7045	CMOS Precision Timer	24.95
ICM7205	CMOS LED Stopwatch/Timer	19.95
ICM7207	Oscillator Controller	7.50
ICM7208	Seven Decade Counter	19.95
ICM7209	Clock Generator	6.95

NMOS READ ONLY MEMORIES

MCM6571	128 X 9 X 7 ASCII Shifted with Greek	13.50
MCM6574	128 X 9 X 7 Math Symbol & Pictures	13.50
MCM6575	128 X 9 X 7 Alphanumeric Control Character Generator	13.50

MISCELLANEOUS

TL074CN	Quad Low Noise bi-fet Op Amp	2.49
TL494CN	Switching Regulator	4.49
TL496CP	Single Switching Regulator	1.75
11C90	Divide 10/11 Prescaler	19.95
95H90	Hi-Speed Divide 10/11 Prescaler	11.95
4N33	Photo-Darlington Opto-Isolator	3.95
MK50240	Top Octave Freq. Generator	17.50
DS0026CH	5Mhz 2-phase MOS clock driver	3.75
TIL308	.27" red num. display w/integ. logic chip	10.50
MM5320	TV Camera Sync. Generator	14.95
MM5330	4½ Digit DPM Logic Block	5.95
LD110/111	3½ Digit A/D Converter Set	25.00/set

LITRONIX ISO-LIT 1
Photo Transistor Opto-Isolator (Same as MCT 2 or 4N25)
2/99¢

SN 76477
SOUND GENERATOR
Generates Complex Sounds
Low Power - Programmable
3.95 each

TV GAME CHIP AND CRYSTAL
AY-3-8500-1 and 2.01 MHZ Crystal (Chip & Crystal Includes score display, 6 games and select angles, etc. **7.95/set**

EXAR

XR205	$3.40			XR2242CP	1.50
XR210	4.40			XR2264	4.25
XR215	4.40			XR2556	3.20
XR320	1.55	JE2206KA	14.95	XR2567	2.99
XR-L555	1.50	JE2206KB	19.95	XR3403	1.25
XR555	.39	XR1800	3.20	XR4136	1.25
XR556	.99	XR2206	4.40	XR4151	2.85
XR567CP	.99	XR2207	3.85	XR4194	1.45
XR567CT	1.25	XR2208	5.20	XR4202	3.60
XR1310P	1.30	XR2209	1.75	XR4212	2.05
XR1468CN	3.85	XR2211	5.25	XR4558	.75
XR1488	1.39	XR2212	4.35	XR4739	1.15
XR1489	1.39	XR2240	3.45	XR4741	1.47

DIODES

TYPE	VOLTS	W	PRICE	TYPE	VOLTS	W	PRICE
				1N4002	100 PIV	1 AMP	12/1.00
				1N4003	200 PIV	1 AMP	12/1.00
1N746	3.3	400m	4/1.00	1N4004	400 PIV	1 AMP	12/1.00
1N751	5.1	400m	4/1.00	1N4005	600 PIV	1 AMP	10/1.00
1N752	5.6	400m	4/1.00	1N4006	800 PIV	1 AMP	10/1.00
1N753	6.2	400m	4/1.00	1N4007	1000 PIV	1 AMP	10/1.00
1N754	6.8	400m	4/1.00	1N3600	50	200m	6/1.00
1N757	9.0	400m	4/1.00	1N4148	75	10m	15/1.00
1N759	12.0	400m	4/1.00	1N4154	35	10m	12/1.00
1N959	8.2	400m	4/1.00	1N4305	75	25m	15/1.00
1N965	15	400m	4/1.00	1N4734	5.6	1w	28
1N5232	5.6	500m	28	1N4735	6.2	1w	28
1N5234	6.2	500m	28	1N4736	6.8	1w	28
1N5235	6.8	500m	28	1N4738	8.2	1w	28
1N5236	7.5	500m	28	1N4742	12	1w	28
1N5242	12	500m	28	1N4744	15	1w	28
1N5245	15	500m	28	1N1183	50 PIV	35 AMP	1.60
1N456	25	40m	6/1.00	1N1184	100 PIV	35 AMP	1.70
1N458	150	7m	6/1.00	1N1185	150 PIV	35 AMP	1.70
1N485A	180	10m	5/1.00	1N1186	200 PIV	35 AMP	1.80
1N4001	50 PIV	1 AMP	12/1.00	1N1188	400 PIV	35 AMP	3.00

SCR AND FW BRIDGE RECTIFIERS

C36D	15A @ 400V	SCR(2N1849)	$1.95
C38M	35A @ 600V	SCR	1.95
2N2328	1.6A @ 300V	SCR	.50
MDA 980-1	12A @ 50V	FW BRIDGE REC.	1.95
MDA 980-3	12A @ 200V	FW BRIDGE REC.	1.95

TRANSISTORS

C106B1	.50			2N3904	4/1.00
MPSA05	.30	2N3055	.89	2N3905	4/1.00
MPSA06	5/1.00	MJE3055	1.00	2N3906	4/1.00
TIS97	6/1.00	2N3392	5/1.00	2N4013	3/1.00
TIS98	6/1.00	2N3398	5/1.00	2N4123	6/1.00
40409	1.75	PN3567	3/1.00	PN4249	4/1.00
40410	1.75	PN3568	4/1.00	PN4250	4/1.00
40673	1.75	PN3569	4/1.00	2N4400	4/1.00
2N918	4/1.00	MPS3638A	5/1.00	2N4401	4/1.00
2N2219A	2/1.00	MPS3702	5/1.00	2N4402	4/1.00
2N2221A	4/1.00	2N3704	5/1.00	2N4403	4/1.00
2N2222A	5/1.00	MPS3704	5/1.00	2N4409	5/1.00
PN2222 Plastic	7/1.00	2N3705	5/1.00	2N5086	4/1.00
2N2369	5/1.00	MPS3705	5/1.00	2N5087	4/1.00
2N2369A	4/1.00	2N3706	5/1.00	2N5088	4/1.00
MPS2369	5/1.00	MPS3706	5/1.00	2N5089	4/1.00
2N2484	4/1.00	2N3707	5/1.00	2N5129	5/1.00
2N2906	4/1.00	2N3711	5/1.00	PN5134	5/1.00
2N2907	5/1.00	2N3724A	.65	PN5138	5/1.00
PN2907 Plastic	7/1.00	2N3725A	1.00	2N5139	5/1.00
2N2925	5/1.00	2N3772	2.25	2N5210	5/1.00
MJE2955	1.25	2N3823	1.00	2N5449	3/1.00
2N3053	2/1.00	2N3903	5/1.00	2N5951	3/1.00

CAPACITOR CORNER

50 VOLT CERAMIC DISC CAPACITORS

	1-9	10-99	100-		1-9	10-99	100-
10 pf	.05	.04	.03	.001µF	.05	.04	.035
22 pf	.05	.04	.03	.0047µF	.05	.04	.035
47 pf	.05	.04	.03	.01µF	.05	.04	.035
100 pf	.05	.04	.03	.022µF	.06	.05	.04
220 pf	.05	.04	.03	.047µF	.06	.05	.04
470 pf	.05	.04	.035	.1µF	.12	.09	.075

100 VOLT MYLAR FILM CAPACITORS

.001mf	.12	.10	.07	.022mf	.13	.11	.08
.0022	.12	.10	.07	.047mf	.21	.17	.13
.0047mf	.12	.10	.07	.1mf	.27	.23	.17
.01mf	.12	.10	.07	.22mf	.33	.27	.22

+-20% DIPPED TANTALUMS (SOLID) CAPACITORS

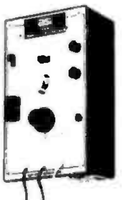
.1/35V	.28	.23	.17	1.5/35V	.30	.26	.21
.15/35V	.28	.23	.17	2.2/25V	.31	.27	.22
.22/35V	.28	.23	.17	3.3/25V	.31	.27	.22
.33/35V	.28	.23	.17	4.7/25V	.32	.28	.23
.47/35V	.28	.23	.17	6.8/25V	.36	.31	.25
.68/35V	.28	.23	.17	10/25V	.40	.35	.29
1.0/35V	.28	.23	.17	15/25V	.63	.50	.40

MINIATURE ALUMINUM ELECTROLYTIC CAPACITORS

Axial Lead				Radial Lead			
.47/50V	.15	.13	.10	.47/25V	.15	.13	.10
1.0/50V	.16	.14	.11	.47/50V	.16	.14	.11
3.3/50V	.15	.12	.09	1.0/16V	.15	.13	.10
4.7/25V	.15	.13	.10	1.0/25V	.16	.14	.11
10/25V	.15	.13	.10	1.0/50V	.16	.14	.11
10/50V	.16	.14	.12	4.7/16V	.15	.13	.10
22/25V	.17	.15	.12	4.7/25V	.15	.13	.10
22/50V	.24	.20	.18	4.7/50V	.16	.14	.11
47/25V	.19	.17	.15	10/16V	.14	.12	.09
47/50V	.25	.21	.19	10/25V	.15	.13	.10
100/25V	.24	.20	.18	10/50V	.16	.14	.12
100/50V	.35	.30	.28	47/50V	.24	.21	.19
220/25V	.32	.28	.25	100/16V	.19	.15	.14
220/50V	.45	.41	.38	100/25V	.24	.20	.18
470/25V	.33	.29	.27	100/50V	.35	.30	.28
1000/16V	.55	.50	.45	220/16V	.23	.17	.16
2200/16V	.70	.62	.55	470/25V	.31	.28	.26

Circle 200 on inquiry card.

Transistor Checker



— Completely Assembled —
— Battery Operated —

The ASI Transistor Checker is capable of checking a wide range of transistor types, either "in circuit" or out of circuit. To operate, simply plug the transistor to be checked into the front panel socket, or connect it with the alligator clip test leads provided. The unit safely and automatically identifies low, medium and high-power PNP and NPN transistors. Size: 3¼" x 6¼" x 2"
"C" cell battery not included.

Trans-Check $29.95 ea.

Custom Cables & Jumpers

DB 25 Series Cables

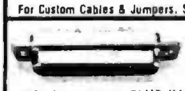
Part No.	Cable Length	Connectors	Price
DB25P-4-P	4 Ft.	2-DP25P	$15.95 ea.
DB25P-4-S	4 Ft.	1-DP25P/1-25S	$16.95 ea.
DB25S-4-S	4 ft.	2-DP25S	$17.95 ea.

Dip Jumpers

DJ14-1	1 ft.	1-14 Pin	$1.59 ea.
DJ16-1	1 ft.	1-16 Pin	1.79 ea.
DJ24-1	1 ft.	1-24 Pin	2.79 ea.
DJ14-1-14	1 ft.	2-14 Pin	2.79 ea.
DJ16-1-16	1 ft.	2-16 Pin	3.19 ea.
DJ24-1-24	1 ft.	2-24 Pin	4.95 ea.

For Custom Cables & Jumpers, See JAMECO 1979 Catalog for Pricing

CONNECTORS



25 Pin-D Subminiature

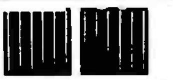
DB25P (as pictured)	PLUG (Meets RS232)	$2.95
DB25S	SOCKET (Meets RS232)	$3.50
DB51226-1	Cable Cover for DB25P or DB25S	$1.75

PRINTED CIRCUIT EDGE-CARD

.156 Spacing-Tin-Double Read-Out — Bifurcated Contacts — Fits .054 to .070 P.C. Cards

15/30	PINS (Solder Eyelet)	$1.95
18/36	PINS (Solder Eyelet)	$2.49
22/44	PINS (Solder Eyelet)	$2.95
50/100 (.100 Spacing)	PINS (Wire Wrap)	$6.95
50/100 (.125 Spacing)	PINS (Wire Wrap) R681-1	$6.95

Solar Cells 2x2cm

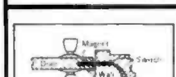


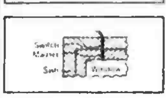
- 0.4 volts
- 100mA
- 41 MW

Can be added in series for higher voltage or parallel for higher current.

#SC 2x2 $1.95 ea. or 3/$5.00

Magnetically Activated Switch

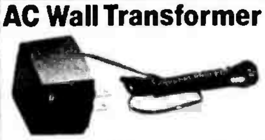




The 9250-0002 is a single pole normally closed switch. When the magnet is engaged, the circuit is open. This switch is only suitable for use in non-magnetic doors and windows.

#9250-0002 2/$1.00

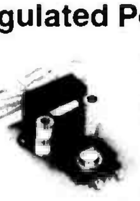
AC Wall Transformer



Ideal for use with clocks, power supplies or any other type of AC application.

Part No.	Input	Output	Price
AC 250	117V/60Hz	12 VAC 250mA	$3.95
AC 500	117V/60Hz	12 VAC 500mA	$4.95

Regulated Power Supply



- Uses LM 309K
- Heat sink provided
- P.C. board construction
- Provides a solid 1 amp @ 5V
- Includes components, hardware and instructions
- Sizes: 3-1/2" x 5" x 2" high

JE200 $14.95

INSTRUMENT/CLOCK CASE

This case is an injection molded unit that is ideal for uses such as DVM, COUNTER, or CLOCK cases. It has dimensions of 4½" in length by 4" in width by 1-9/16" in height. It comes complete with a red bezel.

PART NO: IN-CC $3.49 each

MICROPROCESSOR COMPONENTS

8080A/8080A SUPPORT DEVICES

8080A	CPU	$ 9.95
8212	8-Bit Input/Output	3.25
8214	Priority Interrupt Control	5.95
8216	Bi-Directional Bus Driver	3.49
8224	Clock Generator/Driver	3.95
8226	Bus Driver	3.49
8228	System Controller/Bus Driver	5.95
8238	System Controller	5.95
8251	Prog. Comm. I/O (USART)	7.95
8253	Prog. Interval Timer	14.95
8255	Prog. Periph. I/O (PPI)	9.95
8257	Prog. DMA Control	19.95
8259	Prog. Interrupt Control	19.95

6800/6800 SUPPORT DEVICES

MC6800	MPU	$14.95
MC6802CP	MPU with Clock and Ram	24.95
MC6810API	128X8 Static Ram	5.95
MC6821	Periph. Inter. Adapt (MC6820)	7.49
MC6828	Priority Interrupt Controller	12.95
MC6830L8	1024X8 Bit ROM (MC68A30-8)	14.95
MC6850	Asynchronous Comm. Adapter	7.95
MC6852	Synchronous Serial Data Adapt	9.95
MC6860	0-600 bps Digital MODEM	12.95
MC6862	2400 bps Modulator	14.95
MC6880A	Quad 3-State Bus Trans. (MC8T26)	2.25

MICROPROCESSOR CHIPS—MISCELLANEOUS

Z80(780C)	CPU	$19.95
Z80A(780-1)	CPU	24.95
CDP1802	CPU	19.95
2650	MPU	19.95
8035	8-Bit MPU w/clock, RAM, I/O lines	19.95
P8085	CPU	19.95
TMS9900JL	16-Bit MPU w/hardware, multiply & divide	49.95

SHIFT REGISTERS

MM500H	Dual 25 Bit Dynamic	$ .50
MM503H	Dual 50 Bit Dynamic	.50
MM504H	Dual 16 Bit Static	.50
MM506H	Dual 100 Bit Static	.50
MM510H	Dual 64 Bit Accumulator	.50
MM5016H	500/512 Bit Dynamic	.89
2504T	1024 Dynamic	3.95
2518	Hex 32 Bit Static	4.95
2522	Dual 132 Bit Static	2.95
2524	512 Static	.99
2525	1024 Dynamic	2.95
2527	Dual 256 Bit Static	2.95
2528	Dual 250 Static	4.00
2529	Dual 240 Bit Static	4.00
2532	Quad 80 Bit Static	2.95
2533	1024 Static	2.95
3341	Fifo	6.95
74LS670	4X4 Register File (TriState)	1.95

UART'S

A-Y-5-1013	30K BAUD	5.95

MICROPROCESSOR MANUALS

M-Z80	User Manual	$7.50
M-CDP1802	User Manual	7.50
M-2650	User Manual	5.00

ROM'S

2513(2140)	Character Generator(upper case)	$9.95
2513(3021)	Character Generator(lower case)	9.95
2516	Character Generator	10.95
MM5230N	2048-Bit Read Only Memory	1.95

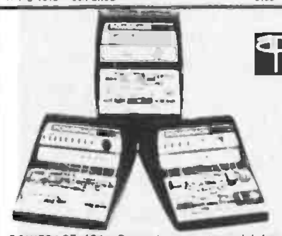
RAM'S

1101	256X1	Static	$1.49
1103	1024X1	Dynamic	.99
2101(8101)	256X4	Static	3.95
2102	1024X1	Static	1.75
21L02	1024X1	Static	1.95
2111(8111)	256X4	Static	3.95
2112	256X4	Static MOS	4.95
2114	1024X4	Static 450ns	9.95
2114L	1024X4	Static 450ns low power	10.95
2114-3	1024X4	Static 300ns	10.95
2114L-3	1024X4	Static 300ns low power	11.95
5101	256X4	Static	7.95
5280/2107	4096X1	Dynamic	4.95
7489	16X4	Static	1.75
74S200	256X1	Static Tristate	4.95
93421	256X1	Static	2.95
UPD414 (MK4027)	4K	Dynamic 16 pin	4.95
UPD416 (MK4116)	16K	Dynamic 16 pin	14.95
TMS4044-45NL	4K	Static	14.95
TMS4045	1024X4	Static	14.95
2117	16,384X1	Dynamic 350ns (house marked)	9.95
MM5262	2KX1	Dynamic	4/1.00

PROM'S

1702A	2048	FAMOS	$5.95
TMS2516 (2716)	16K*	EPROM(Intel 2716)	49.95
	*Requires single +5V power supply		
TMS2532	4KX8	EPROM	89.95
2708	8K	EPROM	10.95
2716 T.I.	16K**	EPROM	29.95
	**Requires 3 voltages, —5V, +5V, +12V		
5203	2048	FAMOS	14.95
6301-1(7611)	1024	Tristate Bipolar	3.49
5330-1(7602)	256	Open C Bipolar	2.95
82S23	32X8	Open Collector	3.95
82S115	4096	Bipolar	19.95
82S123	32X8	Tristate	3.95
74186	512	TTL Open Collector	9.95
74188	256	TTL Open Collector	3.95
74S287	1024	Static	2.95

NEW!! IN STOCK... POWERACE



ALL-CIRCUIT EVALUATORS WITH POWER

- 1680 solderless, plug-in tie points... will hold up to 18 14-pin DIP's
- Breadboard elements accept all DIP sizes... including RTL, DTL, TTL and CMOS devices. TO-5's and discretes with leads up to .032" dia.
- All connections to/from switches, indicators, power supplies and meters are made via solderless, plug-in, tie-point blocks on control panels
- Interconnect with any solid 20 to 30 AWG wire.
- Breadboard elements are mounted on ground planes... ideal for high-frequency and high-speed low-noise circuits
- Short-circuit-proof fused power supplies
- Operate on 110 to 130 VAC at 60 Hz
- Space-age compact styling and high-grade components permit convenient, organized and quick prototyping
- All models are 7.5" wide 11.5" deep and 4.0" high (rear) 0.75" high (front) and weigh approx. 2.5 lbs.

POWERACE 101 -General purpose model for prototyping all types of circuit.
#923101 $ 84.95

POWERACE 102 -Complete digit prototyping lab with built-in logic probe
#923102 $114.95

POWERACE 103 -Triple-output power supply for prototyping both linear and digit circuits.
#923103 $124.95

B&K PRECISION 3½-Digit Portable DMM

- Overload Protected
- 3" high LED Display
- Battery or AC operation
- Auto Zeroing
- 1mv, 1Va, 0.1 ohm resolution
- Overange reading
- 10 meg input impendence
- DC Accuracy 1% typical

Ranges: DC Voltage 0-1000V
AC Voltage 0-1000V
Freq. Response 50-400 HZ
DC/AC Current 0-100mA
Resistance 0.10 meg ohm
Size 6 x 4.4 x 2

Model 2800
$99.95

Comes with test leads, operating manual and spare fuse

Accessories:

AC Adapter 8C-28	$9.00
Rechargeable Batteries BP-26	20.00
Carrying Case LC-28	7.50

CSC 100 MHz 8-Digit Counter

CONTINENTAL SPECIALTIES CORPORATION

- 20 Hz-100 MHz Range
- 6" LED Display
- Crystal-controlled timebase
- Fully Automatic
- Portable — completely self-contained
- Size — 1.75" x 7.38" x 5.63"
- Four power souces, i.e. batteries, 110 or 220V with charger 12V with auto lighter adapter and external 7.2-10V power supply

MAX-100 $134.95

ACCESSORIES FOR MAX 100:

Mobile Charger Eliminator
use power from car battery — Model 100 — CLA $3.95

Charger/Eliminator
use 110 V AC — Model 100 — CAI $9.95

New CSC Mini-Max 6 Digit 50MHz Frequency Counter

- Guaranteed frequency range of 100 Hz to 50 MHz
- Full 6 digit display with antiglare window
- Fully automatic-range, polarity, slope, trigger, input level switching not required.
- Lead-zero blanking—All zeros to the left of the first non-zero digit are blanked. Kilo Hertz and Mega Hertz decimal points automatically light up when the unit is turned on.
- Built in input overvoltage protection.
- Use 9V Battery or 110/220V power.
- Complete with mini antenna.
- Lightweight — Only 8oz.

MINI-MAX $89.95

Accessories For Mini-Max

Part No.	Description	Price
MM-A4	Antenna	$ 3.95
MM-CS	Carrying case	5.95
MM-IPC	Input cable with clip leads	3.95
MM-AC2	110V adapter	9.95
MM-AC3	220V adapter	9.95

$5.00 Minimum Order – U.S. Funds Only
California Residents – Add 6% Sales Tax

Spec Sheets – 25¢
1979 Catalog Available—Send 41¢ stamp

NEW 1979 Catalog

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ADVERTISED PRICES GOOD THRU MARCH

The Incredible "Pennywhistle 103"

$139.95 Kit Only

The Pennywhistle 103 is capable of recording data to and from audio tape without critical speed requirements for the recorder and it is able to communicate directly with another modem and terminal for telephone "hamming" and communications. In addition, it is free of critical adjustments and is built with non-precision, readily available parts.

Data Transmission Method	Frequency-Shift Keying, full-duplex (half-duplex selectable).
Maximum Data Rate	300 Baud.
Data Format	Asynchronous Serial (return to mark level required between each character).
Receive Channel Frequencies	2025 Hz for space; 2225 Hz for mark.
Transmit Channel Frequencies	Switch selectable: Low (normal) = 1070 space, 1270 mark, High = 025 space, 2225 mark.
Receive Sensitivity	−46 dbm accoustically coupled.
Transmit Level	−15 dbm nominal. Adjustable from −6 dbm to −20 dbm.
Receive Frequency Tolerance	Frequency reference automatically adjusts to allow for operation between 1800 Hz and 2400 Hz.
Digital Data Interface	EIA RS-232C or 20 mA current loop (receiver is optoisolated and non-polar).
Power Requirements	120 VAC, single phase, 10 Watts
Physical	All components mount on a single 5" by 9" printed circuit board. All components included.

Requires a VOM, Audio Oscillator, Frequency Counter and/or Oscilloscope to align.

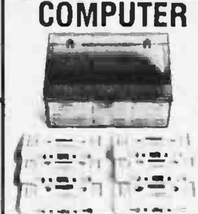
TRS-80 16K Conversion Kit

Expand your 4K TRS-80 System to 16K. Kit comes complete with:
* 8 each UPD416 (16K Dynamic Rams)
* Documentation for conversion

TRS-16K $115.00

Special Offer - Order both your TRS-16K and the Sup'R' MOD II Interface kit together (retail value $144.95) for only $139.95

COMPUTER CASSETTES



- 6 EACH 15 MINUTE HIGH QUALITY C-15 CASSETTES
- PLASTIC CASE INCLUDED 12 CASSETTE CAPACITY
- ADDITIONAL CASSETTES AVAILABLE #C-15-$2.50 ea

CAS-6 $14.95
(Case and 6 Cassettes)

SUP 'R' MOD II

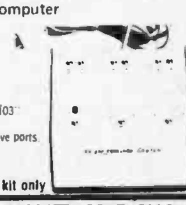
UHF Channel 33 TV Interface Unit Kit

Wide Band B/W or Color System
* Converts TV to Video Display for home computers, CCTV camera, Apple II, works with Cromeco Dazzler, SOL-20, TRS-80, Challenger, etc.
* MOD II is pretuned to Channel 33 (UHF).
* Includes coaxial cable and antenna transformer.

MOD II $29.95 Kit

RS-232 CONTROL CENTER

Plug in your modem, computer prom programmer, terminal, printer, etc. and selectively control data flow.



- Same Contour as "Pennywhistle 103"
- Totally self-contained
- Includes 2 master ports and 3 slave ports

PART NO.
RS-232CC $89.95 kit only

CASSETTE CONTROLLER

Ideal for use with the TRS 80 and others.
"Plug/Jack interface to any computer system requiring remote control of cassette functions"
The CC100 controls cassette motor functions, monitors tape location with its internal speaker and requires no power. Eliminates the plugging and unplugging of cables during computer loading operation from cassette.

#CC-100
$29.50

63-Key Unencoded Keyboard

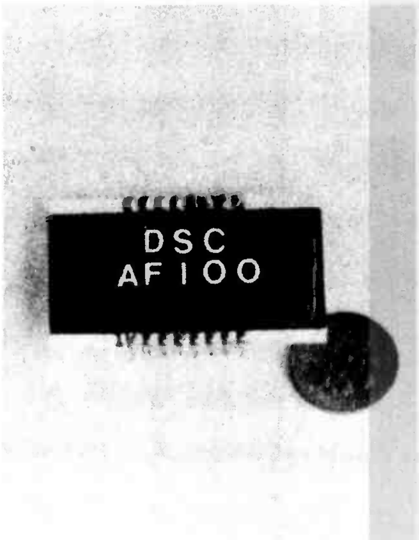
This is a 63-key, terminal keyboard newly manufactured by a large computer manufacturer. It is unencoded with SPST keys, unattached to any kind of PC board. A very solid molded plastic 13 x 4" base suits most application. IN STOCK $29.95/each

Hexadecimal Unencoded Keypad

19-key pad includes 1-10 keys, ABCDEF and 2 optional keys and a shift key. $10.95/each

Circle 200 on inquiry card.

Speech Synthesis Integrated Circuit from TI



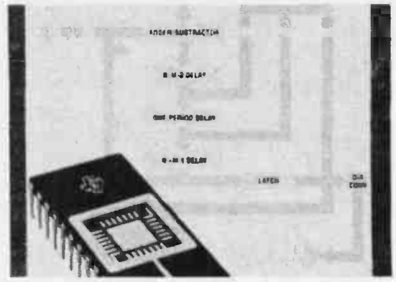
A significant new speech synthesis monolithic integrated circuit has been developed by Texas Instruments Inc, POB 5012, Dallas TX 75222. The circuit, along with two 128 K byte dynamic read only memories, each with the capacity to store over 100 seconds of speech, and a special version of the TMS1000 microcomputer, serve as the main electronics for a new talking learning aid called Speak and Spell, for ages seven and up.

Speech encoding is achieved through pitch-excited linear predictive coding (LPC). LPC is a technique of analyzing and synthesizing human speech by determining from original speech a description of a time varying digital filter modeling the vocal tract. This filter is then excited by other periodic or random inputs. An 8 bit digital to analog converter on the chip transforms digital information processed through the filter into synthetic speech.

Codes for 12 synthesis parameters (ten filter coefficients, pitch, and energy) serve as inputs to the synthesizer chip. These codes are stored in read only memory and, once decoded by on chip circuitry, represent the time varying description of the LPC synthesis model. The LPC speech synthesizer is an advanced design 10 stage lattice filter which has an integrated array multiplier, an adder coupler to the multiplier output and various delay circuits coupled to the adder output.■

Circle 568 on inquiry card.

Dual Tone Separation Filter Integrated Circuit



The Model AF-100 dual tone separation filter integrated circuit provides channel isolation between the low frequency group tone (DTMF) frequencies 697 Hz thru 941 Hz and the high frequency group tone frequencies 1209 Hz thru 1633 Hz. It is intended for applications in which dual tone separation is required, eg: touch tone decoders, transceivers, modem interfaces, etc.

Contained in a 16 pin dual-in-line package, the dual resistance capacitance active filter chip features 30 dB minimum separation between high and low group tones, 1.5 dB maximum in-band deviation, dual and single power supply operation ±12 VDC at 2.5 mA each.

The Model AF-100 is priced at $32. For further information write to Data Signal Corp, 40-44 Hunt St, Watertown MA 02172.■

Circle 569 on inquiry card.

Circle 170 on inquiry card.

NEW IN STOCK

The EW-2001 A "Smart" VIDEO BOARD KIT At A "Dumb" Price!

A VIDEO BOARD + A MEMORY BOARD + AN I/O BOARD – ALL IN ONE!

- STATE OF THE ART TECHNOLOGY USING DEDICATED MICROPROCESSOR I.C.
- NUMBER OF I.C.s REDUCED BY 50% FOR HIGHER RELIABILITY ■ MASTER PIECE OF ENGINEERING ■ FULLY SOFTWARE CONTROLLED

Priced at ONLY **$199.95** Basic Software Included

SPECIAL FEATURES:

- S-100 bus compatible
- Parallel keyboard port
- On board 4K screen memory (optional)* relocatable to main computer memory
- Text editing capabilities (software optional)
- Scrolling: up and down through video memory
- Blinking characters
- Reversed video
- Provision for on board ROM
- CRT and video controls fully programmable (European TV)
- Programmable no. of scan lines
- Underline blinking cursor
- Cursor controls: up, down, left, right, home, carriage return
- Composite video

*Min. 2K required for operation of this board.

DISPLAY FEATURES:

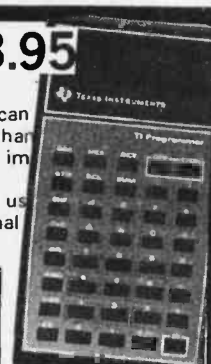
- 128 displayable ASCII characters (upper and lower case alphanumeric, controls)
- 64 or 32 characters per line (jumper selectable)
- 32 or 16 lines (jumper selectable)
- Screen capacity 2048 or 512
- Character generation: 7 x 11 dot matrix

OPTIONS:

Sockets	$10.00
2K Static Memory (with Sockets)	$45.00
4K Static Memory (with Sockets)	$90.00
Complete unit, assembled and tested with 4K Memory	$335.00
Basic software on ROM	$20.00
Text editor on ROM	$75.00

DEALER INQUIRIES WELCOMED

TI PROGRAMMER $53.95



Hexadecimal. Octal. Decimal.
Enter a number in base 8, 10, or 16. TI Programmer can quickly convert to either of the other bases. Rapidly han arithmetic in all three bases giving you more time for im ant programming or troubleshooting tasks.
Ideal for use with any size computer. TI Programmer us integer "two's complement" arithmetic in hexadecimal octal bases.

$44.95 DATA CHROM

Large, easy-to-read 8-digit liquid crystal display.
Clock mode displays time, day, date, and AM/PM.
Stopwatch mode displays hours, minutes, seconds and tenths of seconds up to 9-59-59.9.
Economical—you'll get typically 12 months normal operation on a single set of batteries.
Attractive—comes in brown vinyl wallet folder with insert pockets for business cards. Makes a neat addition to your personal or business accessories.
24-hour alarm.
Stopwatch records and displays lap and total elapsed times.
Up to one-tenth of a second accuracy.

ASCII KEYBOARD KIT $74.00

Additional Improvements: Double Size Return Key Control Characters Molderd on Key Caps

- Power: +5V 275mA
- Upper and Lower Case
- Full ASCII Set
- 7 or 8 Bits Parallel Data
- Optional Serial Output
- Selectable Positve or Negative Strobe, and Strobe Pulse Width
- 2 Key Roll-Over
- 3 User DEfineable Keys
- P.C. Board Size: 17-3/16" x 5"

OPTIONS:

Metal Enclosure Painted Blue and White	$27.50
18 Pin Edge Cqn.	$ 2.00
I.C. Sockets	$ 4.00
Serial Output Provision (Shift Register)	$ 2.00
Upper Case Lock Switch for Capital Letters and Nos.	$ 2.00
Assembled (on Sockets) and Tested	$90.00

APPLE II I/O BOARD KIT

Plugs Into Slot of Apple II Mother Board

18 Bit Parallel Output Port (Expandable to 3 Ports)
1 Input Port
15mA Output Current Sink or Source
Can be used for peripheral equipment such as printers, floppy discs, cassettes, paper tapes, etc.

1 free software listing for SWTP PR40 or IBM selectric

PRICE:
1 Input and 1 Output Port for $49.00
1 Input and 3 Output Ports for $64.00
Dealer Inquiries Invited

SHIPPING: $3.50

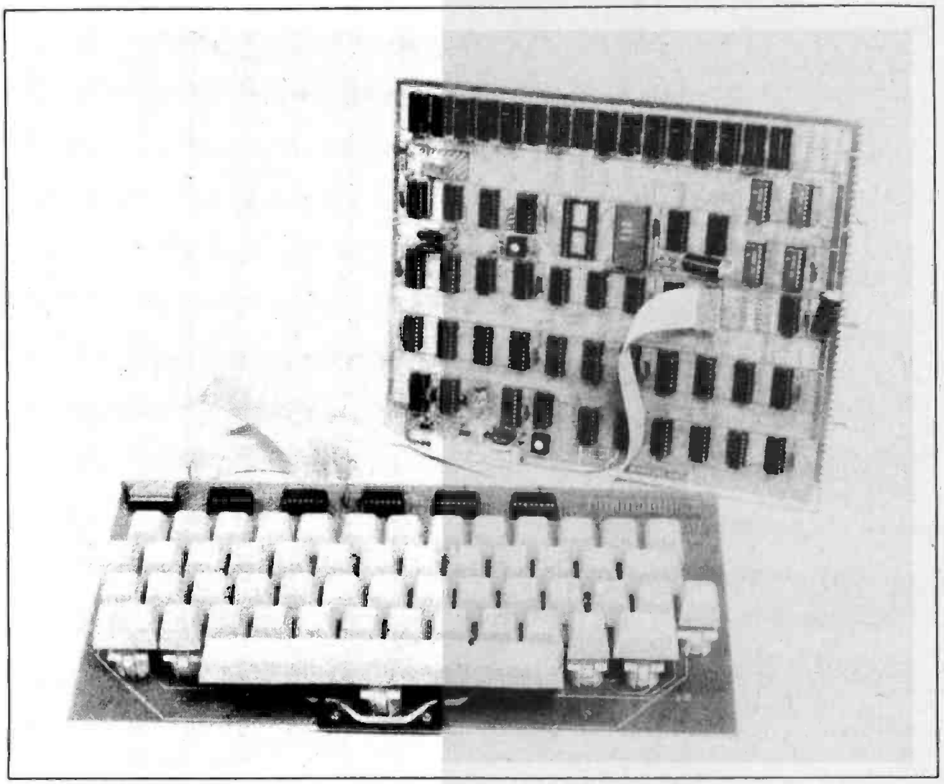
California residents add 6% sales tax

ELECTRONICS WAREHOUSE Inc.

1603 AVIATION BLVD. Dept.
REDONDO BEACH, CA. 90278
TEL. (213) 376-8005
WRITE FOR FREE CATALOG
Minimum Order: $10

VISA master charge

Fully Assembled Video Display Interface for Ohio Scientific Systems



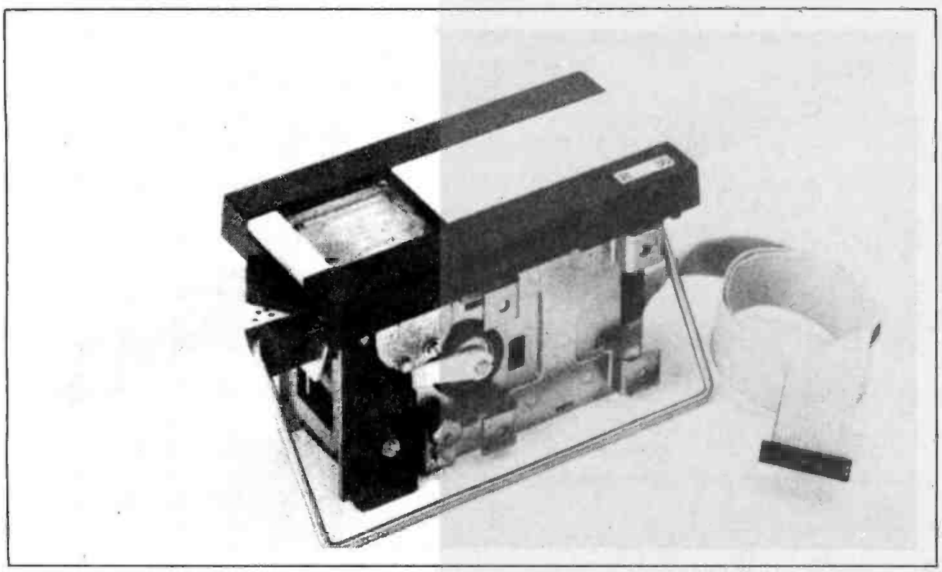
Ohio Scientific is offering the video display interface from its Challenger IIP as a fully assembled accessory for any OSI system. The 540 video display features a 32 row by 64 column display of the standard 64 character ASCII font in 5 by 7 dot matrix form. Standard features include programmable formatting of the display for 32 by 32 or 32 by 64. The 32 by 32 mode is useful for video animation since it provides square character cells. The video board also features a keyboard port which can be used with a standard ASCII keyboard of OSI's new programmable keyboard. The 540 optionally supports a graphics character generator which features lower case and about 170 special characters for plotting and gaming.

All systems using the 540 incorporate OSI's new 542 programmed keyboard. This fully programmable keyboard system is capable of upper and lower case and auto repeat on all characters. The keyboard also features up to five levels of shifting to allow many special single keystroke commands and direct single keystroke graphics. The keyboard has provisions for character editing and supports special formats for video games.

The Model 540 video board is available as an add-on option for any OSI system as a CA-11 for $249. The graphics character generator option retails for $29. Contact Ohio Scientific, 1333 S Chillicothe Rd, Aurora OH 44202.■

Circle 559 on inquiry card.

Tape Punch Handles Paper and Mylar Tapes



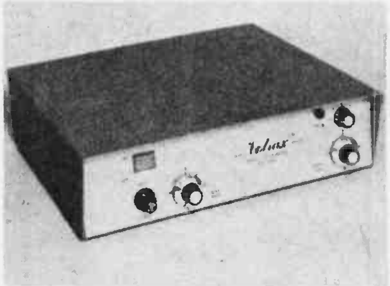
This low cost tape punch, which handles paper or Mylar tape, has been introduced by GNT Automatic Inc, 440 Totten Pond Rd, Waltham MA 02154. The GNT 36 tape punch is designed to handle oiled and dry paper tape and all types of Mylar and Mylar foil tapes without adjustment. Easily integrated into a wide variety of equipment, the unit measures 2.4 by 4.7 by 3 inches (6.10 by 11.94 by 7.62 cm).

Providing a die block life of 150 million characters, the GNT 36 punches up to 50 characters per second. With an allowable back tension of about 5 ounces, the bidirectional unit accommodates 5, 6, or 8 hole tape widths, selectable by the user. A second version of the GNT 36 punches up to 75 characters per second.

The GNT 36 tape punch is priced at $495. Contact GNT Automatic Inc, 440 Totten Pond Rd, Waltham MA 02154.■

Circle 560 on inquiry card.

Interface This Electronic Voice System to Your Computer



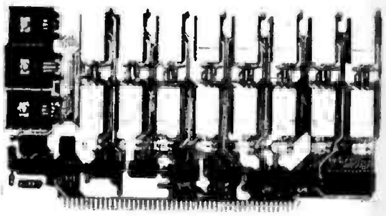
The Votrax VS-6.4 is an improved model of the VS-6 which produces electronically synthesized human speech from digital data. In the VS-6.4 two circuit boards have been changed to obtain improved voice quality. For those who wish to convert their VS-6 equipment, retrofit boards are available. Software is unaffected by the change.

The Votrax VS-6.4 electronic voice system is flexible and operationally simple. A complete range of interface types and options make it compatible with most conventional computer and communications equipment, and it can be used over telephone lines or paging systems.

For further information contact Votrax, 500 Stephenson Hwy, Troy MI 48084.■

Circle 561 on inquiry card.

16K EPROM CARD-S 100 BUSS



$59.95 KIT

OUR BEST SELLING KIT!

USES 2708's!

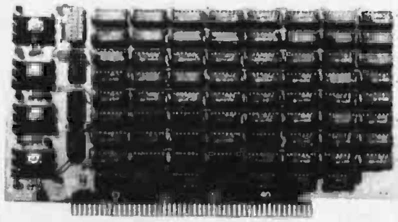
Thousands of personal and business systems around the world use this board with complete satisfaction. Puts 16K of software on line at **ALL TIMES!** Kit features a top quality soldermasked and silk-screened PC board and first run parts and sockets. All parts (except 2708's) are included. Any number of EPROM locations may be disabled to avoid any memory conflicts. Fully buffered and has WAIT STATE capabilities.

OUR 450NS 2708'S ARE $8.95 EA. WITH PURCHASE OF KIT

ASSEMBLED AND FULLY TESTED ADD $25

8K LOW POWER RAM KIT-S 100 BUSS

250 NS SALE!



ADD $5 FOR 250NS!

$129 KIT

Use 21L02 450 NS RAMS!

Thousands of computer systems rely on this rugged, work horse, RAM board. Designed for error-free, NO HASSLE, systems use.

KIT FEATURES:

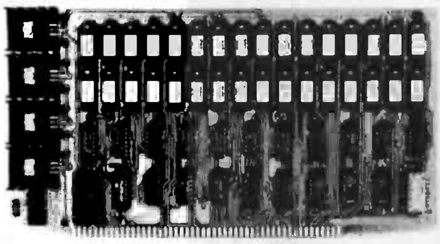
1. Doubled sided PC Board with solder mask and silk screen layout. Gold plated contact fingers.
2. All sockets included.
3. Fully buffered on all address and data lines.
4. Phantom is jumper selectable to pin 67.
5. FOUR 7805 regulators are provided on card.

Blank PC Board w/Documentation $29.95
Low Profile Socket Set...13.50
Support IC's (TTL & Regulators) $9.75
Bypass CAP's (Disc & Tantalums) $4.50

ASSEMBLED AND FULLY BURNED IN ADD $30

16K STATIC RAM KIT-S 100 BUSS

$295 KIT



FULLY STATIC, AT DYNAMIC PRICES

WHY THE 2114 RAM CHIP?

We feel the 2114 will be the next industry standard RAM chip (like the 2102 was). This means price, availability, and quality will all be good! Next, the 2114 is FULLY STATIC! We feel this is the ONLY way to go on the S-100 Buss! We've all heard the HORROR stories about some Dynamic Ram Boards having trouble with DMA and FLOPPY DISC DRIVES. Who needs these kinds of problems? And finally, even among other 4K Static RAM's the 2114 stands out! Not all 4K static Rams are created equal! Some of the other 4K's have clocked chip enable lines and various timing windows just as critical as Dynamic RAM's. Some of our competitor's 16K boards use these "tricky" devices. But not us! The 2114 is the ONLY logical choice for a trouble-free, straightforward design.

KIT FEATURES:

1. Addressable as four separate 4K Blocks.
2. ON BOARD BANK SELECT circuitry. (Cromemco Standard!). Allows up to 512K on line!
3. Uses 2114 (450NS) 4K Static Rams.
4. ON BOARD SELECTABLE WAIT STATES.
5. Double sided PC Board, with solder mask and silk screened layout. Gold plated contact fingers.
6. All address and data lines fully buffered.
7. Kit includes ALL parts and sockets.
8. PHANTOM is jumpered to PIN 67.
9. LOW POWER: under 2 amps TYPICAL from the +8 Volt Buss.
10. Blank PC Board can be populated as any multiple of 4K.

BLANK PC BOARD W/DATA—$33
LOW PROFILE SOCKET SET—$12
SUPPORT IC'S & CAPS—$19.95
ASSEMBLED & TESTED—ADD $30
2114 RAM'S—8 FOR $69.95

60 Hz CRYSTAL TIME BASE

$4.95 (Complete Kit)

Uses MM5369 CMOS divider IC with high accuracy 3.579545 MHZ Crystal. Use with all MOS Clock Chips or Modules. Draws only 1.5 MA. All parts, data, and PC Board included.

100 HZ CRYSTAL TIME BASE

$5.95 (Complete Kit)

Same as above, except it uses a special MM5369. Perfect for frequency counter time bases, etc. Also use with MOSTEK MK50397 timer chip.

16K DYNAMIC RAM CHIP

16K X 1 Bits. 16 Pin Package. Same as Mostek 4116-4. 250 NS access. 410 NS cycle time. Our best price yet for this state of the art RAM. 32K and 64K RAM boards using this chip are readily available. These are new, fully guaranteed devices by a major mfg. **VERY LIMITED STOCK!**

8 FOR $89.95

NOT ASSOCIATED WITH DIGITAL RESEARCH OF CALIFORNIA, THE SUPPLIERS OF CPM SOFTWARE.

2708 EPROMS

450 NS!

Now full speed! Prime new units from a major U.S. Mfg. 450 N.S. Access time. 1K x 8. Equiv. to 4-1702 A's in one package.

~~$15.75 ea.~~ **$9.95** ~~4 FOR $50.00~~

PRICE CUT

NATIONAL SEMICONDUCTOR JUMBO CLOCK MODULE

MA1008A BRAND NEW!

$6.95

2 FOR $13

(AC XFMR $1.95)

FEATURES

- FOUR JUMBO ½ INCH LED DISPLAYS
- 12 HR REAL TIME FORMAT
- 24 HR ALARM SIGNAL OUTPUT
- 50 OR 60 Hz OPERATION
- LED BRIGHTNESS CONTROL
- POWER FAILURE INDICATOR
- SLEEP & SNOOZE TIMERS
- DIRECT LED DRIVE (LOW RFI)
- COMES WITH FULL DATA

ASSEMBLED! NOT A KIT!

ZULU VERSION! We have a limited number of the 24 HR Real time version of this module in stock. #MA1008D — $9.95

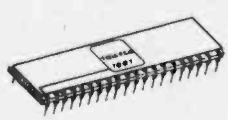
PERFECT FOR USE WITH A TIMEBASE.

COMPARE AT UP TO TWICE OUR PRICE!

MANUFACTURER'S CLOSEOUT!

WESTERN DIGITAL UART

TR1602A. PIN FOR PIN SUB FOR AY5-1013 AND TMS6011.
FOR SERIAL I/O



$2.99 EACH

SURPLUS SPECIAL

SALE!

1N4148 DIODES. SILICON. Same as 1N914. New, factory prime, Full Leads.
100 FOR $2
1000 FOR $17.50

New! REAL TIME Computer Clock Chip

N.S. MM5313. Features BOTH 7 segment and BCD outputs. 28 Pin DIP. $4.95 with Data

Z-80 PROGRAMMING MANUAL

By MOSTEK, or ZILOG. The most detailed explanation ever on the working of the Z-80 CPU CHIPS. At least one full page on each of the 158 Z-80 instructions. A MUST reference manual for any user of the Z-80. 300 pages. Just off the press. **$12.95**

COMPUTER PARTS

Z-80	- 19.95	8212	- 2.25
Z-80A	- 24.95	8255	- 6.95
8080A	- 6.95	2111AL-4	- 2.25
8080A-2	- 8.95	2708	- 9.95

"THE COLOSSUS" FAIRCHILD SUPER JUMBO LED READOUT

A full .80 inch character. The biggest readout we have ever sold! Super efficient. Compare at up to $2.95 each from others!

YOUR CHOICE

FND 843 Common Anode
FND 850 Common Cathode **$1.49 ea** (6 for $6.95)

Digital Research Corporation

(OF TEXAS)

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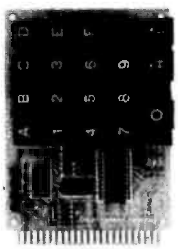
TERMS: Add 30¢ postage, we pay balance. Orders under $15 add 75¢ handling. No C.O.D. We accept Visa, MasterCharge, and American Express cards. Tex. Res. add 5% Tax. Foreign orders (except Canada add 20% P & H. 90 Day Money Back Guarantee on all items.

HEX ENCODED KEYBOARD
E.S.

This HEX keyboard has 19 keys, 16 encoded with 3 user definable. The encoded TTL outputs, 8-4-2-1 and STROBE are debounced and available in true and complement form. Four onboard LEDs indicate the HEX code generated for each key depression. The board requires a single +5 volt supply. Board only $15.00 Part No. HEX-3, with parts $49.95 Part No. HEX-3A. 44 pin edge connector $4.00 Part No. 44P.



E.S. TRS-80 SERIAL I/O

• RS-232 compatible • Can be used with or without the expansion bus • On board switch selectable baud rates of 110, 150, 300, 600, 1200, 2400, parity or no parity odd or even, 5 to 8 data bits, and 1 or 2 stop bits. D.T.R. line. Board only $19.95 Part No. 8010, with parts $59.95 Part No. 8010A, assembled $79.95 Part No. 8010C. No connectors provided, see below.

EIA/RS-232 connector Part No. DB25P $6.00, with 8', 8 conductor cable $10.95 Part No. DB25PS.

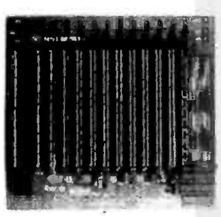
3' ribbon cable with attached connectors to fit TRS-80 and our serial board $19.95 Part No 3CAB40.

S-100 BUS ACTIVE TERMINATOR *

Board only $14.95 Part No. 900, with parts $24.95 Part No. 900A

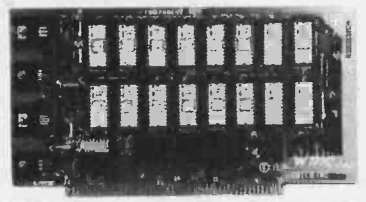
9 AND 13 SLOT MOTHER BOARDS
WMC inc.

All traces are reflow solder covered and both sides are solder masked. The connectors used on these boards are the IMSAI™ type (.125" between pins, .250" between rows). Spacing between connectors is .750". All lines, except power and ground, have a passive RC network termination available. There is a kluge area available that will accept two 40 pin sockets and one 36 pin socket. The circuitry for supplying three separate regulated voltages to the kluge area is contained on the board. Part No. QM8-12 $40 bare, $105 kit, $120 assembled. Part No. QM8-9 $35 bare, $90 kit, $105 assembled.



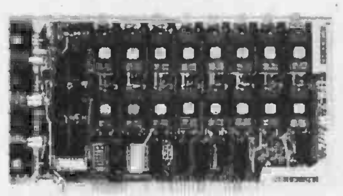
4K EPROM
WMC inc.

This board is designed to operate with any speed or power 1702A. Addressable in 4K byte increments and can be configured to occupy either 2K or 4K segments. It can be populated one memory chip at a time. Bare board $30, board with parts $200, assembled $230. Part No. EPM-1



16K OR 32K EPROM
WMC inc.

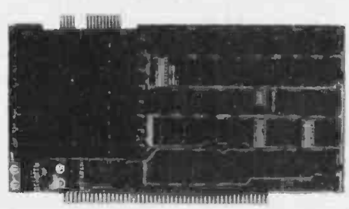
Designed to operate with any speed or power 2708 or single voltage (+5V) 2716. Addressable in 4K increments and can occupy multiples of 4K. It can be populated one memory chip at a time. Has bank addressing and Phantom Disable. The board comes with an exclusive software program that can be placed in a 2708 or 2716 that will, when used in conjunction with a RAM memory board, check out every line on the EPM-2. Bare board $30, board with parts with 2708 $455, assembled $485. Board with parts with 2716 $1,225, assembled $1,255. Part No. EPM-2



PIICEON

65K DYNAMIC RAM

Main memory for microcomputers, intelligent terminals, business systems, medical systems, and OEM systems. • High density random access memory 48K bytes or 64K bytes • Fully buffered • S-100 bus compatible • Low power (dynamic memory) • Transparent refresh • Digital delay line techniques for reliable operation • Multiple boards allowed using hardware or software controlled bank select • "Phantom" signal for RAM/ROM overlap • All boards are fully tested prior to shipment. Operating System test and extensive bit pattern testing. • Works directly in 8080A processors or Z-80 environment at 2MHz • Currently used by industry • 1 year warranty. Only available assembled and tested with 48K $1,250 Part No. 48K, or with 65K $1,475 Part No. 65K

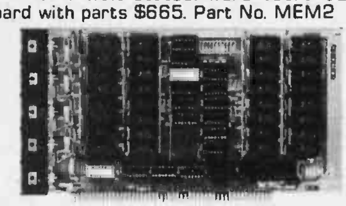


8080A CPU (With Eight Level Victor Interrupt Capability)
WMC inc.

Uses the 8080A and the 8224 clock chip. The crystal frequency used is 18 MHz and the vector interrupt chip is the 8214. The board will function normally without the interrupt circuitry. When the interrupt circuitry is built up, the board will respond to eight levels of interrupts. Designed to be a plug-in replacement for the IMSAI CPU board and will work in other computers with the appropriate modifications made to the ribbon cable connector pin out from the front panel. The board will work in systems without a front panel if the system has a PROM board that simulates the functions of the front panel. Bare board $30, with parts $185, assembled $220. Part No. CPU-1

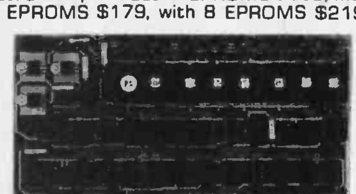
16K STATIC RAM
WMC inc.

Operates with any speed or power 2114. All input and output lines are fully buffered. Addressable in 4K byte increments. If the system has a front panel, the board will allow itself to be protected. If there is no front panel, the board will not allow itself to be protected. The board has Bank Address capability, Phantom Disable, MWRITE, and selectable wait states. Bare board $30, board with parts $665. Part No. MEM2



8K EPROM
PIICEON

Saves programs on PROM permanently (until erased via UV light) up to 8K bytes. Programs may be directly run from the program saver such as fixed routines or assemblers. • S-100 bus compatible • Room for 8K bytes of EPROM non-volatile memory (2708's). • On-board PROM programming • Address relocation of each 4K or memory to any 4K boundary within 64K • Power on jump and reset jump option for "turnkey" systems and computers without a front panel • Program saver software available • Solder mask both sides • Full silkscreen for easy assembly. Program saver software in 1 2708 EPROM $25. Bare board $35 including custom coil, board with parts but no EPROMS $139, with 4 EPROMS $179, with 8 EPROMS $219.



To Order: Mention part number, description, and price. In USA, shipping paid for orders accompanied by check, money order, or Master Charge, BankAmericard, or VISA number, expiration date and signature. Shipping charges added to C.O.D. orders. California residents add 6.5% for tax. Outside USA add 10% for air mail postage and handling, no C.O.D.'s. Checks and money orders must be payable in US dollars. Parts kits include sockets for all ICs, components, and circuit board. Documentation is included with all products. Prices are in US dollars. No open accounts. To eliminate tariff in Canada boxes are marked "Computer Parts." Dealer inquiries invited. 24 Hour Order Line: (408) 226-4064

* Circuits designed by John Bell

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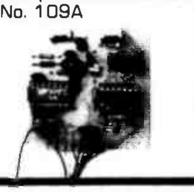
MODEM⁂

● Type 103 ● Full or half duplex ● Works up to 300 baud ● Originate or Answer ● No coils, only low cost components ● TTL input and output-serial ● Connect 8 Ω speaker and crystal mic. directly to board ● Uses XR FSK demodulator ● Requires +5 volts ● Board only $7.60 Part No. 109, with parts $27.50 Part No. 109A

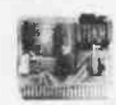


APPLE II⁂ SERIAL I/O INTERFACE

Baud rate is continuously adjustable from 0 to 30,000 ● Plugs into any peripheral connector ● Low current drain. RS-232 input and output ● On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even ● Jumper selectable address ● SOFTWARE ● Input and Output routine from monitor or BASIC to teletype or other serial printer ● Program for using an Apple II for a video or an intelligent terminal. Also can output in correspondence code to interface with some selectrics. ● Board only $15.00 Part No. 2, with parts $42.00 Part No. 2A, assembled $62.00 Part No. 2C

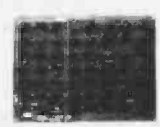
UART & BAUD RATE GENERATOR⁂

● Converts serial to parallel and parallel to serial ● Low cost on board baud rate generator ● Baud rates: 110, 150, 300, 600, 1200, and 2400 ● Low power drain +5 volts and -12 volts required ● TTL compatible ● All characters contain a start bit, 5 to 8 data bits, 1 or 2 stop bits, and either odd or even parity. ● All connections go to a 44 pin gold plated edge connector ● Board only $12.00 Part No. 101, with parts $35.00 Part No. 101A, 44 pin edge connector $4.00 Part No. 44P



T.V. TYPEWRITER

● Stand alone TVT ● 32 char/line, 16 lines, modifications for 64 char/line included ● Parallel ASCII (TTL) input ● Video output ● 1K on board memory ● Output for computer controlled curser ● Auto scroll ● Non-destructive curser ● Curser inputs: up, down, left, right, home, EOL, EOS ● Scroll up, down ● Requires +5 volts at 1.5 amps, and -12 volts at 30 mA ● All 7400, TTL chips ● Char. gen. 2513 ● Upper case only ● Board only $39.00 Part No. 106, with parts $145.00 Part No. 106A



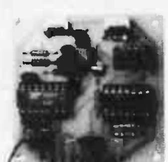
T.V. INTERFACE

● Converts video to AM modulated RF, Channels 2 or 3. So powerful almost no tuning is required. On board regulated power supply makes this extremely stable. Rated very highly in Doctor Dobbs' Journal. Recommended by Apple ● Power required is 12 volts AC C.T., or +5 volts DC ● Board only $7.60 part No. 107, with parts $13.50 Part No. 107A

(Illegal where prohibited by law.)

TAPE⁂ INTERFACE

● Play and record Kansas City Standard tapes ● Converts a low cost tape recorder to a digital recorder ● Works up to 1200 baud ● Digital in and out are TTL-serial ● Output of board connects to mic. in of recorder ● Earphone of recorder connects to input on board ● No coils ● Requires +5 volts, low power drain ● Board only $7.60 Part No. 109, with parts $27.50 Part No. 109A



To Order: Mention part number, description, and price. In USA, shipping paid for orders accompanied by check, money order, or Master Charge, BankAmericard, or VISA number, expiration date and signature. Shipping charges added to C.O.D. orders. California residents add 6.5% for tax. Outside USA add 10% for air mail postage and handling. no C.O.D.'s. Checks and money orders must be payable in US dollars. Parts kits include sockets for all ICs, components, and circuit board. Documentation is included with all products. Prices are in US dollars. No open accounts. To eliminate tariff in Canada boxes are marked "Computer Parts." Dealer inquiries invited. 24 Hour Order Line: (408) 226-4064

⁂ Circuits designed by John Bell

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QUEST Cosmac Super Elf Computer $106.95

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The **Super Elf** includes a **ROM** monitor for program loading, editing and execution with **SINGLE STEP for program debugging** which is not included in others at the same price. With **SINGLE STEP** you can see the microprocessor chip operating with the **unique Quest address and data bus displays before, during and after** executing instructions. Also, CPU mode and instruction cycle are shown on several LED indicator lamps.

An RCA 1861 **video graphics** chip allows you to connect to your own TV with an inexpensive video modulator to do graphics and games. There is a **speaker system** included for writing your own music or using many music programs already written. The speaker amplifier may also be used to drive relays for control purposes.

A 24 key **HEX keyboard** includes 16 HEX keys plus **load, reset, run, input, memory protect, memory select, monitor select** and **single step.** Large, on board displays provide output and optional **high and low address.** There is a 44 pin standard connector for PC cards and a 50 pin connector for the **Quest Super Expansion Board.** Power supply and sockets for **all** IC's are included in the price plus a detailed 90 page instruction manual.

Many schools and universities are using the Super Elf as a course of study. OEM's use it for training and research and development.

Remember, other computers only offer Super Elf features at additional cost or not at all. Compare **before you buy. Super Elf Kit $106.95, High address option $8.95, Low address option $9.95. Custom Hardwood Cabinet** with drilled and labelled front panel **$24.95. NiCad Battery Backup Kit $4.95.** All kits and options also come completely assembled and tested.

Questdata, a 12 page monthly software publication for 1802 computer users is available by subscription for $12.00 per year. New 100 page software manual Vol.1 $4.95.

Tiny Basic for ANY 1802 System

Cassette $10.00. On ROM Monitor $38.00. Super Elf owners. 30% off. **Object code listing or paper tape with manual $5.50.**
Original ELF Kit Board $14.95.

Super Expansion Board with Cassette Interface $89.95

This is truly an astounding value! This board has been designed to allow **you** to decide how you want it optioned. **The Super Expansion Board comes with 4K of low power RAM** fully addressable anywhere in 64K with built-in memory protect and a **cassette interface.** Provisions have been made for all other options on the same board and it fits neatly into the hardwood cabinet alongside the **Super Elf.** The board includes slots for **up to 6K of EPROM (2708, 2758, 2716 or TI 2716) and is fully socketed ($12.00 value).** EPROM can be used for the monitor and Tiny Basic or other purposes.

A 1K Super ROM Monitor $19.95 is available as an on board option in 2708 EPROM which has been preprogrammed with a program loader/editor and error checking multi file cassette read/write software, (relocatible cassette file) another exclusive from Quest. It includes register save and readout, block move capability, and video graphics driver with blinking cursor. The Super Monitor is written with subroutines allowing users to take advantage of monitor functions simply by calling them up. Improvements and revisions are easily done with the monitor. If you have the **Super Expansion Board and Super Monitor** the monitor is up and running at the push of a button.

Other on board options include **Parallel Input and Output Ports with full handshake.** They allow easy connection of an ASCII keyboard to the input port. **RS 232 and 20 ma Current Loop** for teletype or other device are on board and if you need more memory there are two S-100 slots for static RAM or video boards. A Godbout 8K RAM board is available for $135.00. **Parallel I/O Ports $9.85, RS 232 $4.50, TTY 20 ma I/F $1.95, S-100 $4.50. A 50 pin connector set** with ribbon cable is available at $12.50 for easy connection between the **Super Elf and the Super Expansion Board.**

The **Power Supply** for the Super Expansion Board is a 5 amp supply with + 8v ± 18v + 12v − 5v. Regulated voltages are ±5v & +12v $29.95. −12 volt optional. Deluxe version Includes the case at $39.95.

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INTEGRATED CIRCUITS

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7400N	.17
7402N	.17
7404N	.19
7409N	.23
7410N	.17
7414N	.63
7420N	.17
7422N	1.39
7430N	.20
7442N	.50
7445N	.69
7447N	.60
7448N	.69
7450N	.17
7474N	.29
7475N	.49
7485N	.88
7489N	2.00
7490N	.43
7492N	.43
7493N	.43
7495N	.69
74100N	.90
74107N	.29
74121N	.34
74123N	.59
74125N	.39
74145N	.69
74150N	.95
74151N	.69
74154N	1.00
74157N	.69
74161N	.87
74162N	.67
74163N	.87
74174N	.96
74175N	.90
74190N	1.15
74192N	.87
74193N	.85
74221N	1.55
74298N	1.65
74365N	.66
74366N	.66
74367N	.66

74LS00 TTL	
74LS00N	.25
74LS02N	.25
74LS04N	.25
74LS05N	.25
74LS08N	.25
74LS10N	.25
74LS13N	.40
74LS14N	.90
74LS20N	.25
74LS22N	.25
74LS28N	.41
74LS30N	.25
74LS33N	.39
74LS38N	.30
74LS74N	.35
74LS75N	.47
74LS90N	.51
74LS93N	.51
74LS95N	1.89
74LS107N	.35
74LS112N	.35
74LS113N	.35
74LS132N	.72
74LS136N	.35
74LS151N	.67
74LS155N	.67
74LS157N	.67
74LS162N	.91
74LS163N	.91
74LS174N	.95
74LS190N	1.06
74LS221N	1.95
74LS258N	.67
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LM320K-12	1.35
LM320K-15	1.35
LM320T-5	1.60
LM320T-8	1.60
LM320T-12	1.50
LM320T-15	1.60
LM324N	1.15
LM339N	1.55
LM340K-5	1.10
LM340K-8	1.10
LM340K-12	1.10
LM340K-15	1.10
LM340K-24	1.10
LM340T-5	1.10
LM340T-8	1.10
LM340T-12	1.10
LM340T-15	1.10
LM340T-18	1.10
LM340T-24	1.10
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LM382	1.60
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LM733N	.87
LM741CH	.35
LM741N	.25
LM747H/N	.62
LM748N	.35
LM1303N	.82
LM1304	1.10
LM1305	1.27
LM1307	2.00
LM1310	2.75
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CD4013	.36
CD4014	.86
CD4015	.86
CD4016	.36
CD4017	.94
CD4018	.94
CD4019	.21
CD4020	1.02
CD4021	1.02
CD4022	.86
CD4023	.21
CD4024	.75
CD4025	.21
CD4026	1.51
CD4027	.36
CD4028	.79
CD4029	1.02
CD4030	.21
CD4035	1.02
CD4040	1.02
CD4042	.71
CD4043	.63
CD4044	.63
CD4046	1.67
CD4049	.36
CD4050	.36
CD4051	1.13
CD4060	1.42
CD4066	.71
CD4068	.40
CD4069	.40
CD4070	.40
CD4071	.21
CD4072	.21
CD4073	.21
CD4075	.21
CD4076	1.75
CD4078	.40
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74C10	.28
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74C923	5.50
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8T23	3.10
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8T28	2.75
8T97	1.69
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6850	12.95
6502	12.50

IC SOCKETS

Solder Tin Low Profile PIN	1 UP	PIN	1UP
8	.15	22	.30
14	.18	24	.35
16	.20	28	.42
18	.27	36	.58
20	.29	40	.57

3 level wire wrap gold
14 pin 25
2 level 14 pin ww 20

WIRE WRAP LEVEL 3

PIN		PIN	
14	.25	24	.86
16	.33	28	1.00
18	.57	40	1.23

UART/FIFO	
AY5-1013	5.50
AY5-1014	7.50
3341	6.95

PROM	
1702A	3.95
N82S23	2.95
N82S123	3.50
N82S126	3.75
N82S129	3.75
N82S131	3.75
N82S136	8.75
N82S137	8.75
2708	10.50
DM8577	2.90
8223	2.90
2716T1	22.50
2716 Intel	48.00

CRYSTALS	
1 MHz	4.50
2 MHz	4.50
4 MHz	4.25
5 MHz	4.25
10 MHz	4.25
18 MHz	3.90
20 MHz	3.90
32 MHz	3.90
32768 MHz	4.00
1.8432 MHz	4.50
3.5795 MHz	1.20
2.0100 MHz	1.95
2.097152 MHz	4.50
2.4576 MHz	4.50
3.2768 MHz	4.50
5.0688 MHz	4.50
5.185 MHz	4.50
5.7143 MHz	4.50
6.5536 MHz	4.50
14.31818 MHz	4.25
18.432 MHz	4.50
22.1184 MHz	4.50

CONNECTORS	
44 pin edge	2.00
100 pin edge	4.50
100 pin edge WW	4.50

KEYBOARD ENCODERS	
AY5-2376	$12.50
AY5-3600	13.50
74C922	5.50
74C923	5.50
HD0165-5	6.95

IC Test Clips	1	10
Red	.55	.47
Black	.55	.47

Keyer 8043 14.50
comp. w/spec./sock.

TRANSISTORS	
2N1893	.40
2N2222A	.18
2N2369	.30
2N2904A	.20
2N2907A	.25
2N3053	.40
2N3638	.25
2N3643	.25
2N3904	.18
2N3906	.18
2N3055	.69
2N4400	.25
2N4401	.75
2N4402	.20
TIP31	.60
TIP33A	1.00

CLOCK MODULES Complete alarm clocks ready to hook up with transformer and switches. Very compact with .50" and .84" digits.

MA1002A, C or E .50"	8.95
102P3 Transformer	2.25
MA1010A, C or E .84"	11.95
102P2 Transformer	2.25
Special transformer and six switches when purchased w/module	2.95
MA1003 car module .3" green fluor. display	15.95

RESISTORS ¼ watt 5%
10 per type .03 1000 per type .012
25 per type .025 350 piece pack
100 per type .015 5 per type 6.75

KEYBOARDS	
56 key ASCII keyboard kit	$62.50
Fully assembled	72.50
53 key ASCII keyboard kit	55.00
Fully assembled 65.00 Enclosure	14.95

LEDS	
Red TO18	.15
Green, Orange, Yellow TO18	.20
Jumbo Red	.20
Green, Orange, Yellow Jumbo	.25
Cliplite LED Mounting Clips	8/$1.25

(specify red, amber, green, yellow, clear)

CONTINENTAL SPECIALTIES in stock
Complete line of breadboard test equip.
MAX-100 8 digit Freq. Ctr. $128.95

OK WIRE WRAP TOOLS in stock
Portable Multimeter $18.00

DIGITAL THERMOMETER $48.50
Batt. oper. General purpose or medical 32°–230°F. Disposable probe cover ±.2° accuracy. Comp. Assy. in compact case. Switches from F° to C°.

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4K EPROM Kit	114.95
I/O Board Kit	44.50
Extender Board w/connector	12.50
Video Interface board kit	125.00
16K EPROM board kit w/o PROMS	74.50
16K Static RAM board kit	395.00
North Star Floppy Disk Kit	$665.00
Additional Drive Kit	415.00

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PC board	7.50
Switches Mom. Pushbutton	.27
3 pos. slide	.25
Encoder HD0165-5	6.95
3 Digit Universal Counter Board Kit Operates 5–18 Volt DC to 5 MHz typ. .125" LED display	10.50
Voice actuated switch	.50
Paratronics 100A Logic Analyzer Kit	$224.00
Model 10 Trigger Expander Kit	$229.00
Model 150 Bus Grabber Kit	$369.00

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12 Volt 300 ma transformer	1.25
12.6V CT 600 ma	3.75
12V 250 ma wall plug	2.95
12V CT 250 ma wall plug	3.50
24V CT 400 ma	3.95
10V 1.2 amp wall plug	4.85
12V 6 amp	12.95

DISPLAY LEDS			
MAN1	CA	.270	2.90
MAN3	CC	.125	.39
MAN72/74	CA/CA	.300	1.00
DL704	CC	.300	1.25
DL707/DL707R	CA	.300	1.00
DL727/728	CA/CC	.500	1.90
DL747/750	CA/CC	.600	1.95
DL750	CC	.600	1.95
FND359	CC	.357	.70
FND500/507	CC/CA	.500	1.35
FND503/510	CC/CA	500	.90
FND800/807	CC/CA	800	2.20
3 digit Bubble			.60
4 digit bubble			.80
DG8 Fluorescent			1.75
DG10 Fluorescent			1.75
5 digit 14 pin display			1.00
NSN69 9 digit display			.60
7520 Clairex photocells			.39
TIL311 Hex			9.50

COMPUTER GRADE CAPS			
1600	mfd	200V	4.50
2000	mfd	45V	2.50
3200		50V	2.50
5500		25V	2.50
5800		40V	3.00
6100		40V	3.00
6100		50V	3.00
7700		50V	2.50
8000		55V	2.50
9400		65V	3.00
10000		20V	2.50
12000		30V	3.50
35000		25V	5.00
55000		25V	5.00
82000		15V	6.00
160000		10V	6.00

Auto Clock Kit $15.95
DC clock with 4-.50" displays. Uses National MA-1012 module with alarm option. Includes light dimmer, crystal timebase PC boards. Fully regulated, comp. instructs. Add $3.95 for beautiful dark gray case. Best value anywhere.

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Video computer with games and graphics. Fully assem. and test. **$249.00**

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Indoor and outdoor. Switches back and forth. Beautiful. 50" LED readouts. Nothing like it available. Needs no additional parts for complete, full operation. Will measure −100° to +200°F, tenths of a degree, air or liquid. Very accurate. $39.95
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Opens shorted cells that won't hold a charge and then charges them up, all in one kit w/full parts and instructions. $7.25

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Ultraviolet, assembled $34.50

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CT7015 direct drive chip displays date and time on .6" LEDS with AM-PM indicator. Alarm/doze feature includes buzzer. Complete with all parts, power supply and instructions, less case.

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Prescaler kit to 350 MHz $19.95

1978 IC Update Master Manual
1978 IC Update Master Manual $19.50. Complete IC data selector, 2175 pg. Master reference guide. Over 42,000 cross references. Free update service through 1978. Domestic postage $3.50. Foreign $5.00. 1979 IC Update available late Jan. $35.00.

Stopwatch Kit $26.95
Full six digit battery operated. 2–5 volts. 3.2768 MHz crystal accuracy. Times to 59 min., 59 sec., 99 1/100 sec. Times std., split and Taylor. 7205 chip, all components minus case. Full instructions.

D Connectors RS232
25 Pin Subminiatures

DB25P	2.95	DE9P	1.50
DB25S	3.95	DE9S	1.95
Cover	1.50	DA15P	2.10
RS232 Complete Set	6.50	DA15S	3.10

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8K Static RAM Kit	$135.00
16K Static RAM Kit	265.00
24K Static RAM Kit	423.00
32K Dynamic RAM Kit	310.00
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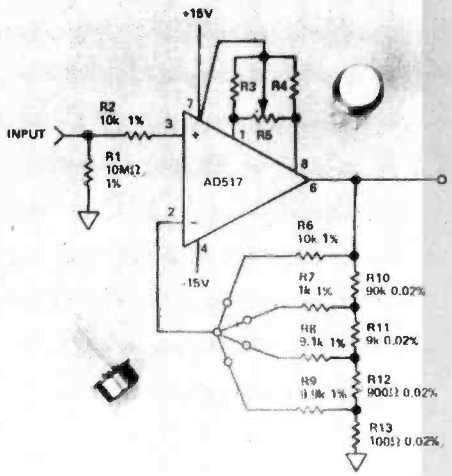
Free 32 Page Short Form Guide from Analog Devices



This new *Short Form Guide* contains a complete listing of Analog Devices' line of more than 400 products for precision measurement and control, including digital to analog, analog to digital, voltage to frequency and frequency to voltage converters; sample and hold amplifiers; multiplexers, switches and references; operational amplifiers, instrumentation amplifiers and isolation amplifiers; computational circuits; root mean square to DC converters; analog input and output subsystems for microcomputers; data acquisition subsystems; temperature transducers; digital panel instruments; and power supplies. Products are listed with basic specifications and prices. Contact Analog Devices, Rt 1 Industrial Park, POB 280, Norwood MA 02062.■

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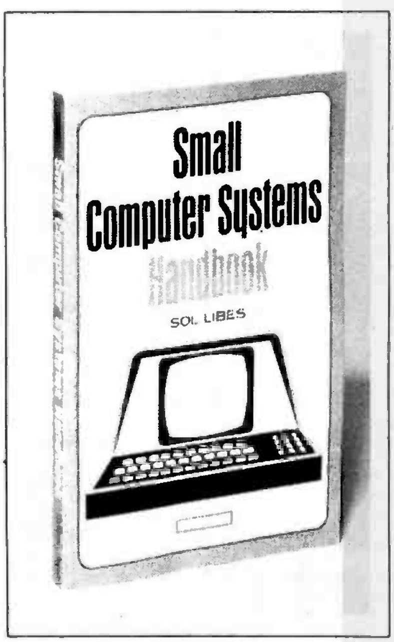
Small Computer Systems Handbook by Sol Libes



Small Computer Systems Handbook by Sol Libes is written for those new to the field of personal computers. The emphasis throughout is on important practical knowledge that the small computer user should have to be able to intelligently purchase, assemble and interconnect components, and to program the microcomputer.

This guide provides background in digital logic fundamentals, number systems, and computer hardware and software basics. Only a minimal amount of electronics is required. The book offers an introduction to programming on the machine level, and with higher level languages such as BASIC.

The various applications of small computers are described, such as maintaining financial records, storing records, controlling appliances, typewriting, sales analysis and inventory control.

This 197 page book is priced at $8.45 and is published by Hayden Book Company Inc, Rochelle Park NJ 07662.■

Circle 564 on inquiry card.

PET Magazine on Cassette

Program is a new monthly magazine recorded on cassette and intended for use by 8 K byte Commodore PET computer owners. Subscribers will receive a standard magazine format for video display on side 1 of the cassette, with pages of articles, applications, sources of hardware and software, availability of peripherals, programming hints, etc. The reverse side contains three or more games, household and business programs, etc. The subscription rate is $27 per year. For further information contact *Program*, POB 461, Philipsburg PA 16866.■

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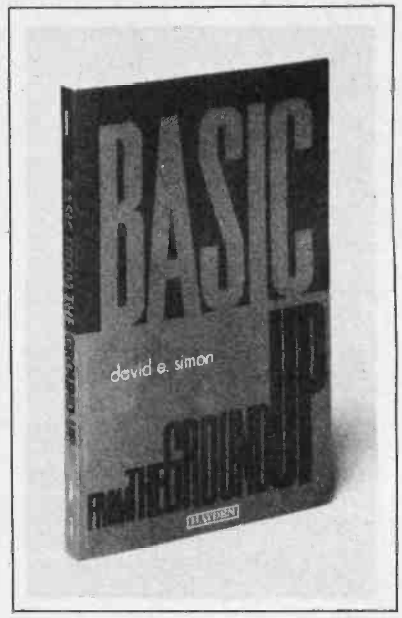
For Newcomers to the Computer Field



BASIC From the Ground Up by David E Simon assumes the reader knows nothing about computers. All the statements of BASIC are detailed as well as what goes on inside the computer when programming. The book covers at least one version of each of the BASIC statements along with some of their variations. *BASIC From the Ground Up* is 232 pages long and is priced at $8.95. Contact Hayden Book Company Inc, 50 Essex St, Rochelle Park NJ 07662.■

Circle 563 on Inquiry card.

Free Information on Commodore PET

Are you having difficulty locating information on the Commodore PET computer? New England Electronics Company, 248 Bridge St, Springfield MA 01103, has available free of charge a PET information package as well as a software and hardware products directory. The information package includes specifications on the PET 2020 printer, PET service and warranty information and other pertinent data concerning the PET.■

Circle 565 on inquiry card.

Catalog Features Personal Computing

Introduction to Personal Computing is a composite of companies providing personal computing hardware and software to the marketplace. Included are profiles of 69 companies and an overview of their product offerings. It also includes the names and addresses of various computer related publications. This 72 page catalog is available for $25 ($5 handling charge if payment does not accompany the order). New Jersey residents should include 5% sales tax. For further information contact Alltech Publishing Company, 212 Cooper Center, N Park Dr and Browning Rd, Pennsauken NJ 08109.■

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THE PET CONNECTION

Networks Bidirectional RS-232 Interface

Single Port	$240.00
Dual Port	$280.00
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Networks Modem for PET

Attaches to DAA	$320.00
Cabinet	$ 35.00

PET with 8K user memory	$795.00
Second Cassette drive	$99.95
RS-232 Printer Adapter — assembled board	
With power supply case & connector	$169.00
Beeper — PET controlled 'beep'	$24.95
Video Buffer — add a conventional monitor	$29.95

EXPANDAPET — Economical 16K memory expansion for the PET (incl 1 daughter bd) $485
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Hams! Add a PET to your rig.

Computerize your station with Microtronics' M-65 Ham Interface and included software. You simply plug the unit into your PET and you're ready to display, transmit and receive either CW or RTTY at rates up to 100 WPM

ASSEMBLED KITS
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This peripheral from Commodore gives you the ability to use one tape deck for input and one for output, copy files, etc.

SELECTRIC-BASED TERMINAL FOR PET

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We have interfaced our TC-71 to the PET. Use with the IEEE-488 bus as a printer or with the VIA User Port for bidirectional I/O. Ideal for Word Processing applications.

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This is a completely refurbished Teletype KSR-33 terminal ready to attach to your PET's interface to use as a printer

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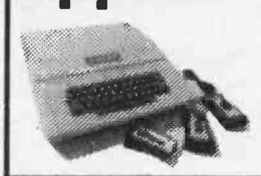
apple II



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- Z-80 Processor
- Full-size ASCII keyboard
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Single board

VIDEO TERMINAL by XITEX

16 Ln x 64 chr display, 128 printable characters, software UART (ASCII or Baudot), 3 serial interfaces & cassette I/O, true composite video, TTL compatible, easy power connection.

Assembled & tested **NOW $187**

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A full capability terminal completely assembled with a 90 day warranty for less than you'd pay for a kit.

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Model 3 8K RAM $1,495.
Model 4 16K RAM $1,795.
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- Beautiful 128 x 128 color graphics
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Top-quality printing terminal with RS-232, PTTC code. Includes desk. 130 char line. ASCII version employs 6802 for code conversion. See our catalog for details.

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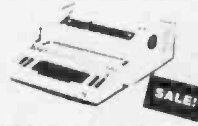

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45 Day delivery Normally $199 NOW **$169**
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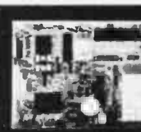

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NCE/Compumart Inc. breaks the price barrier with a new 300 baud RS-232C acoustic coupler. For only $159 you get an assembled, tested stand alone unit which accepts the standard telephone handset for full or half duplex operation. Complete with power supply and carrier detect light, the unit is housed in an attractive case for desk top use.

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INTERACT Model One

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Best of all you get over $294 worth of free cassettes including:

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STRIP — WRAP — UNWRAP

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MOS LSI INSERTER

Tool is crome plated ABS for excellent static dissipation.
Tool has ground lug for connection to grounding strap.

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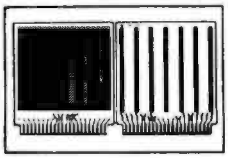
P.C. BOARD



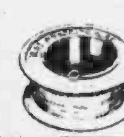
The 4 x 4.5 x 1/16 inch board is made of glass coated EPOXY Laminate and features solder coated 1 oz. copper pads. The board has provision for a 22/44 two sided edge connector, with contacts on standard .156 spacing. Edge contacts are non-dedicated for maximum flexibility.

The board contains a matrix of .040 in. diameter holes on .100 inch centers. The component side contains 76 two-hole pads that can accommodate any DIP size from 6-40 pins, as well as discrete components. Typical density is 18 of 14-Pin or 16-Pin DIP's. Components may be soldered directly to the board or intermediate sockets may be used for soldering or wire wrapping.

Two independent bus systems are provided for voltage and ground on both sides of the board. In addition, the component side contains 14 individual busses running the full length of the board for complete wiring flexibility. These busses enable access from edge contacts to distant components. These busses can also serve to augment the voltage or ground busses, and may be cut to length for particular applications.

Hobby Board	H-PCB-1	$4.99

REFILL ROLL OF WIRE



Wire for wire-wrapping AWG-30 (0.25mm) KYNAR® wire, 50 ft. roll, silver plated, solid conductor, easy stripping.

30-AWG Blue Wire 50ft Roll	R 30B-0050	$1.98
30-AWG Yellow Wire 50ft Roll	R 30Y-0050	$1.98
30-AWG White Wire 50ft Roll	R 30W-0050	$1.98
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Fast • Reliable • Economical

- No more cutting & stripping by hand
- Good, clean, uniform strip
- Cheaper than using bulk wire

PRECUT WIRE — BULK WIRE

#30 Kynar stripped 1" on each end. Lengths are overall. Colors: Red, Blue, Green, Yellow.

	100	500		100	500
2½ in.	.78	2.40	6½ in.	1.15	4.05
3 in.	.82	2.60	7 in.	1.20	4.25
3½ in.	.86	2.80	7½ in.	1.25	4.45
4 in.	.90	3.00	8 in.	1.29	4.65
4½ in.	.94	3.21	8½ in.	1.32	4.85
5 in.	.98	3.42	9 in.	1.36	5.05
5½ in.	1.02	3.65	9½ in.	1.40	5.25
6 in.	1.06	3.85	10. in.	1.45	5.51

WIRE KITS

#1 $6.95 (2.2 ¢/ft.)

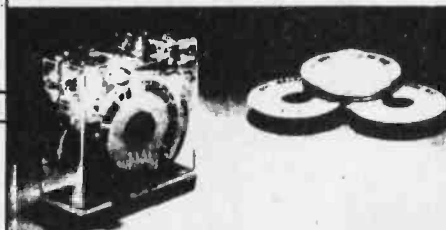
250	3"	100	4½"
250	3½"	100	5"
100	4"	100	6"

#2 $19.95 (1.9 ¢/ft.)

250	2½"	250	5"
500	3"	100	5½"
500	3½"	250	6"
500	4"	100	6½"
250	4½"	100	7"

1-250 ft. Roll

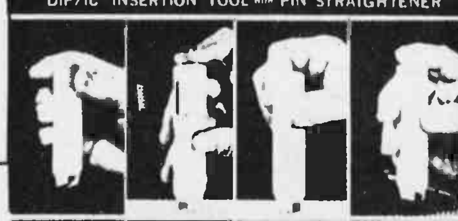
TRI-COLOR WIRE DISPENSER



WD - 30 - TRI $5.95
R - 30 - TRI 3 color refill $3.95

- With 50 ft. ea. of RED, WHITE, BLUE wire
- Cuts the wire to length
- Strips 1" of insulation
- Refillable

DIP/IC INSERTION TOOL with PIN STRAIGHTENER

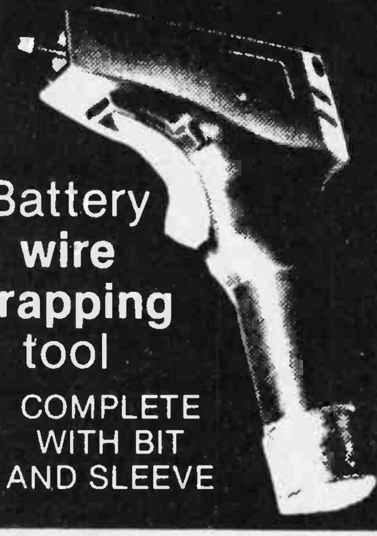


STRAIGHTEN PINS — RELEASE — PICK UP — INSERT

14-16 Pin Dip IC Inserter	INS-1416	$3.49

NEW

HOBBY-WRAP Model BW-630



Battery wire wrapping tool

COMPLETE WITH BIT AND SLEEVE

WIRE DISPENSER

- With 50 ft. Roll of AWG 30 KYNAR® wire-wrapping wire.
- Cuts the wire to length.
- Strips 1" of insulation.
- Refillable

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Yellow Wire	WD-30-Y	$3.95
White Wire	WD-30-W	$3.95
Red Wire	WD-30 R	$3.95

WIRE-WRAPPING TOOL

For .025" (0,63mm) sq. post "MODIFIED" wrap, positive indexing, anti-overwrapping device.

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For AWG 30	BW-630	$34.95*
For AWG 26-28	BW-2628	$39.95*

Bit for AWG 30	BT-30	$3.95
Bit for AWG 26-28	BT-2628	$7.95

*USE "C" SIZE NI CAD BATTERIES (NOT INCLUDED)

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The EX-1 Extractor is ideally suited for hobbyist or lab engineer. Featuring one piece spring steel construction. It will extract all LSI, MSI and SSI devices of from 8 to 24 pins.

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LM4A 4 dig .03% DC
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  Tilt stand option .... $ 3.50
- Leather case $20.00

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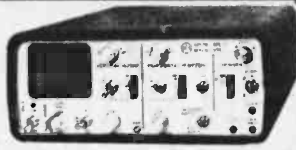

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PROBE 1¢
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S100 WWG 50/100 Cont .125 ctrs 3 LEVEL WIRE WRAP .025" sq posts on .250 spaced rows GOLD plated

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$4.00	$3.75	$3.50

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Other Popular Edge Connectors

R644-G 22/44 Cont. .156 ctrs PIERCED SOLDER EYLET tails. GOLD plated

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R644-3 22/44 Cont. .156 ctrs WIRE WRAP tails GOLD

1-4	5-9	10-24
$4.00	$3.75	$3.50

CG-1 IMSAI Style Card Guides 5/$1.00
ATTN: OEM's and Dealers, many other connectors available call for quotation

3 LEVEL GOLD WIRE WRAP SOCKETS

Sockets purchased in multiples of 50 per type may be combined for best price.

	1-24	25-49	50-99	100-249	250-999	1K-5K
8 pin*	.41	.38	.35	.31	.27	.23
14 pin*	.39	.38	.36	.32	.29	.27
16 pin*	.43	.42	.39	.35	.32	.30
18 pin	.63	.58	.54	.47	.42	.36
20 pin	.80	.75	.70	.63	.58	.53
22 pin*	.90	.85	.80	.70	.61	.57
24 pin	.90	.84	.78	.68	.63	.58
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40 pin	1.50	1.40	1.30	1.20	1.04	.89

All sockets are GOLD 3 level closed entry *End and side stacable. 2 level, Solder Tail, Low Profile, Tin Sockets and Dip Plugs available. CALL FOR QUOTATION

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- Solder mask with solder windows on etched circuits to avoid accidental short circuits
- Mounts 11 receptacles with 100 contacts (2 rows) on .125 centers with .250 row spacing, vector part number R681-2, or mounts 10 receptacles plus interconnections to smaller mother board for expansion
- Includes etched circuits and instructions for option of active, pull-up, or floating terminations
- Large buses +5V and GND (10 AMPS), ± 12V or 16V (7 AMPS). Current ratings are per MIL STD 275 with 10°C rise
- Fits in Vector-pak enclosures
- Fits in IMSAI 8080 microcomputer as expander board.

8803
MOTHER BOARD FOR S100 BUS MICRO-COMPUTERS

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Price: **$29.50**

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Card Extender has 100 contacts 50 per side on .125 centers-Attached connector-is compatible with S-100 Bus Systems. $25.83
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1/16 Vector BOARD
.042 dia holes on 0.1 spacing for IC's

Phenolic PART NO.	SIZE	PRICE 1-9	10-19
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64P44	4.5x6.5"	$1.79	$1.61
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169P44	4.5x17"	$4.52	$4.07
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Sockets are End & Side stackable, closed entry

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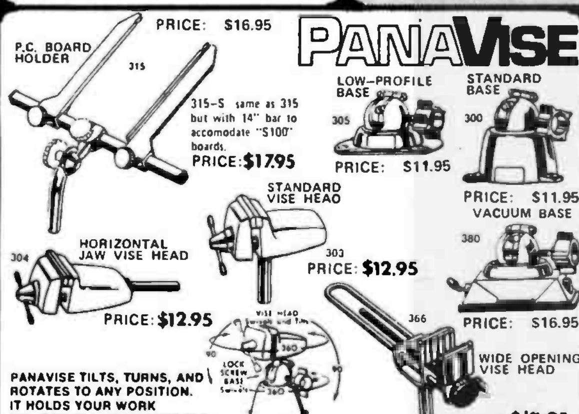

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IMSAI CARD GUIDES:	0.19 ea.	5 pcs.	0.16 ea.

CROMEMCO S-100: Cont./Ctrs. .125" Row Spacing, .250"

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OTHER CONNECTORS AVAILABLE

.100" Contact Ctrs., .140" Row Spacing.

22/44 Dip Sold.	$2.30 ea.	5 pcs.	$2.10 ea.
25/50 Sold. Eye.	2.95 ea.	5 pcs.	2.75 ea.
40/80 Sold. Eye.	4.80 ea.	5 pcs.	4.50 ea.
43/86 Dip Sold.	4.90 ea.	5 pcs.	4.70 ea.
43/86 Sold. Eye.	4.90 ea.	5 pcs.	4.70 ea.

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6/— Sgle. Row (PET)	$1.00 ea.	5 pcs.	$0.90 ea.
22/44 Sold. Eye. (KIM)	1.90 ea.	5 pcs.	1.80 ea.
22/44 Dip Sold. (KIM)	1.90 ea.	5 pcs.	1.80 ea.
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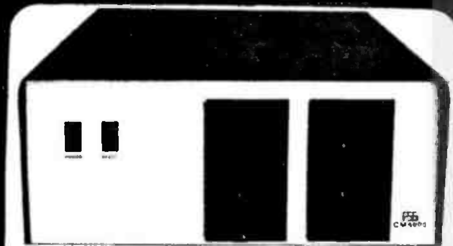
Memory Madness Memory Madness Memory Madness

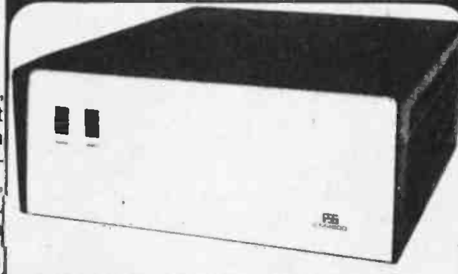
PROBLEM SOLVER SYSTEMS, INC.



CM5000 COMPUTER MAINFRAME

Includes cabinet, 18 amp power supply, S-100 compatible STREAKER-12® (12-slot motherboard), and dual-disk provision with disk power supply. The CM5000 is fan-cooled, has AC line filter to eliminate EMI, and is fully-assembled and factory-tested. Power and reset switches are located on front panel.

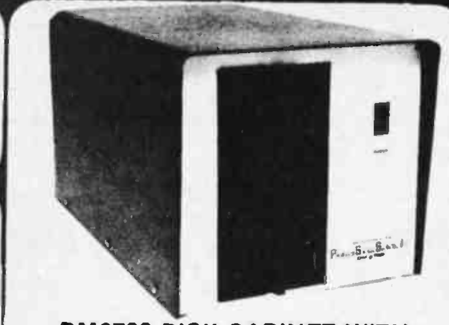
~~$549.00~~* $495.00



CM4800 COMPUTER MAINFRAME

Includes cabinet, 30 amp power supply, and the S-100 compatible STREAKER-22® (22-slot motherboard). The CM4800 is fan-cooled, has AC line filter to eliminate EMI, and is fully-assembled and factory-tested. Power and reset switches are located on front panel. OPTION: Model CM4800D—includes provision for floppy disk power supply. Also available: Model CM4900—with 18 amp power supply and STREAKER-12® (12-slot motherboard)

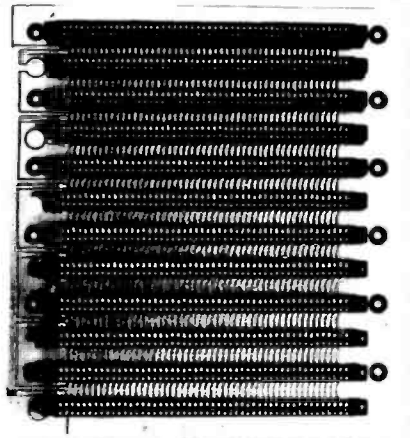
~~$549.00~~* $495.00



DM2700 DISK CABINET WITH POWER SUPPLY

Accepts either PerSci or Shugart mini-floppy disks. Includes data cable and AC line filter to eliminate EMI. Operates from 100 to 125 volts or 200 to 250 volts, 50 or 60Hz. Fully assembled and tested at factory. (Disk drive not included). OPTION: Model DM2700S—Includes Shugart Series 800 minifloppy disk.

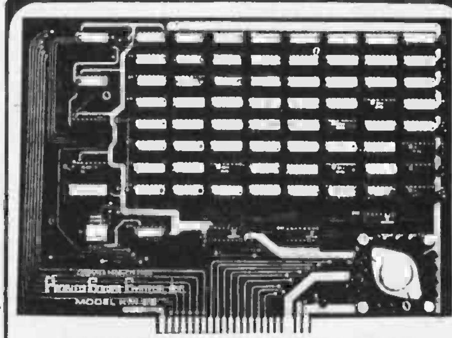
~~$249.00~~* $225.00



STREAKER® MOTHERBOARDS

- In 7, 12, and 22-slot versions • S-100 compatible
- Connectors have bifurcated, gold-plated contacts
- Ground plane surrounding each signal
- Compatible with Imsai chassis
- Power connections compatible with power supplies in PSS's CM4800, CM5000, and CM5200 Computer mainframes.
- Fully-assembled and tested at factory
- No isolation hardware required for mounting.

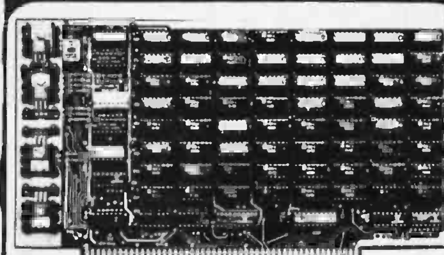
Streaker 12	~~$99.00~~	$89.00
Streaker 22	~~$159.00~~	$147.00



KM8B / KIM-4® COMPATIBLE

- KIM® compatible, 8K x 8 bit static RAM
- Can be connected directly to KIM-1®
- Plugs directly into KIM-4® motherboard • 2MHz
- Addressable in 8K steps
- Allows expansion of KIM® computer up to 65K of memory
- Memory protection activated / deactivated by DIP Switch
- Buffered address and data lines
- Operates from either an unregulated 8 volt or a regulated 5 volt power supply
- All IC's mounted in low-profile sockets
- Assembled, tested, burned-in at factory.

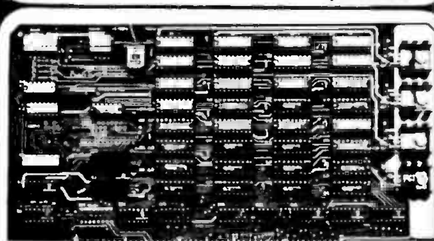
~~$179.00~~ $162.00



RAM 8 ~~$199.00~~ $179.00

- S-100, 8K x 8 bit static RAM
- 4MHz
- Addressable in 8K steps
- Memory protection in 1K increments, from bottom board address up or top down
- Memory protection activated / deactivated by large, easily accessible switch
- May deactivate up to six 1K segments of board by use of jumpers to create "holes" for other devices
- DIP switch selectable wait states
- Phantom line jumper
- Schmitt trigger-buffered I/O lines
- All IC's mounted in low-profile sockets
- Assembled, tested, burned-in at factory.

OPTION: RAM8B—2MHz ~~$179.00~~ $162.00



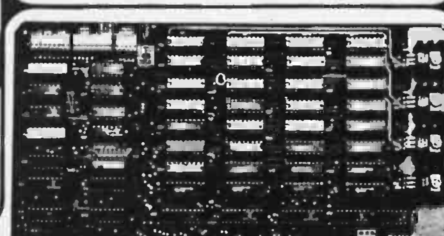
RAM 16 ~~$449.00~~ ~~$372.00~~ $339.00

- S-100, 16K x 8 bit static RAM • 4MHz
- Addressable in 4K steps
- Memory protection in 1K increments, from bottom board address up or top down
- Memory protection activated / deactivated by large, easily accessible switch
- May deactivate up to six 1K segments of board by use of jumpers to create "holes for other devices
- DIP switch selectable wait states
- Phantom line DIP switch
- Bank-select for expansion beyond 65K of memory
- Schmitt trigger-buffered I/O lines
- All IC's mounted in low-profile sockets
- Assembled, tested, burned-in at factory

OPTION: RAM16B—2MHz

~~$429.00~~ $339.00

*Please include sufficient funds to cover cost of shipping of Mainframes.



RAM 65 ~~$495.00~~ $395.00 BANK SELECTABLE

- S-100, 16K x 8 bit static RAM • 4MHz
- Addressable in 4K steps
- Memory protection in 1K increments, from bottom board address up or top down
- Memory protection activated / deactivated by large, easily accessible switch
- May deactivate up to six 1K segments of board by use of jumpers to create "holes" for other devices
- DIP switch selectable wait states
- Phantom line DIP switch
- Features bank selection by I/O instruction using any one of 256 DIP switch-selectable codes—allows up to 256 software-controlled memory banks.
- Schmitt trigger-buffered I/O lines • All IC's mounted in low-profile sockets
- Assembled, tested, burned-in at factory

OPTION: RAM65B—2MHz

~~$459.00~~ $389.00

*Please include sufficient funds to cover cost of shipping of Mainframes.

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OEM and institutional inquiries invited

Memory Madness Memory Madness Memory Madness

What's New?

CALCULATORS

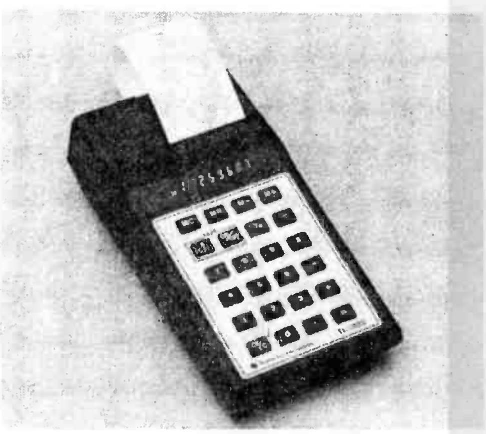
New 10 Digit Desktop Calculator from Sharp

This new desktop, 10 digit business calculator featuring an item counter and grand total key has been introduced by Sharp Electronics Corp, 10 Keystone Pl, Paramus NJ 07652.

The new 4½ pound QS-1702 offers calculating and printing on standard roll paper. A 1 touch grand total key accumulates individual calculations. Specially designed minus equal and plus equal keys make the QS-1072 ideal for applications that require fast calculation. A constant add mode selector facilitates dollars and cents calculations. A 1 touch percent key, non-add and subtract total key for printing dates and codes, an item counter switch with a plus and minus and plus/only calculation and a fixed and floating decimal point selector are other major features of the QS-1702 calculator.■

Circle 532 on inquiry card.

Handheld Printer and Display Calculator

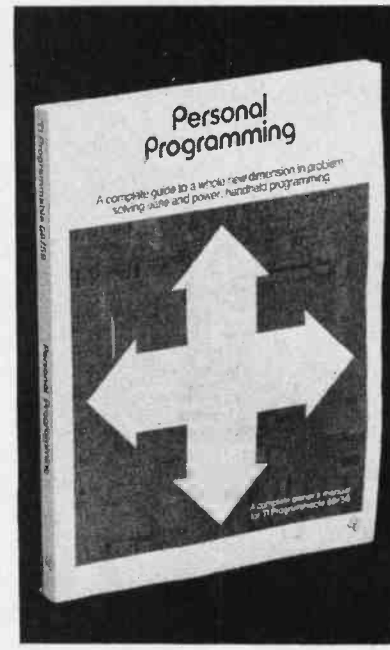


This rechargeable handheld printer and display calculator has been introduced by Texas Instruments Inc, POB 53, Lubbock TX 79408. The TI-5025 features a thermal printer and a large vacuum fluorescent display that can be used without the printer to conserve paper. The unit provides four basic functions as well as percent and 4 key memory. The TI-5025 operates with the same number entry system used in other TI handheld calculators. The thermal printer has fewer parts than impact printers, providing reliable, quiet, ribbonless operation.

The unit is priced at $80 and comes with a charger and adapter, thermal paper and carrying case. Thermal paper rolls are available in packages of three for $0.99.■

Circle 533 on inquiry card.

Operator's Manual for Texas Instruments Programmable 58 and 59 Calculators



Personal Programming is written for owners of the Texas Instruments programmable 58 and 59 calculators. This manual gives a guided tour of keyboard basics, display control, algebraic functions, conversions, and statistical function on keys; a step by step discussion of programming as well as advanced programming; and a detailed analysis of all calculator keys showing the full operating limits of the machines in various calculating situations.

The price of this manual is $12.95 plus tax and $1 for shipping. For further information contact Texas Instruments Inc, POB 2500, Lubbock TX 79408.■

Circle 534 on inquiry card.

wirewrap

PRECUT WIRE

#30 WIRE KITS

#1 $7.95

250	3"	100	4½"
250	3½"	100	5"
100	4"	100	6"

#2 $19.95

250	2½"	250	5"
500	3"	100	5½"
500	3½"	250	6"
500	4"	100	6½"
250	4½"	100	7"

#3 $24.95

500	2½"	500	4½"
500	3"	500	5"
500	3½"	500	5½"
500	4"	500	6"

#4 $44.95

1000	2½"	1000	4½"
1000	3"	1000	5"
1000	3½"	1000	5½"
1000	4"	1000	6"

Choose One Color or Random Assortment:
Red, Blue, Green, Yellow, White, Orange, Black.

* #26 Prices on Request

#30 Kynar stripped 1" on each end. Lengths are overall.
Colors: Red, Blue, Green, Yellow, Black, Orange, White.
Wire packaged in plastic bags. Add 25¢/length for tubes.

In.	100	500	1000	5000
2½	1.04	2.98	5.16/K	4.67/K
3	1.08	3.22	5.65/K	5.06/K
3½	1.13	3.46	6.14/K	5.46/K
4	1.18	3.20	6.62/K	5.87/K
4½	1.23	3.95	7.12/K	6.25/K
5	1.28	4.20	7.61/K	6.62/K
5½	1.32	4.48	8.10/K	7.03/K
6	1.37	4.72	8.59/K	7.43/K
6½	1.60	5.37	9.84/K	8.48/K
7	1.66	5.63	10.37/K	8.91/K
7½	1.73	5.89	10.91/K	9.33/K
8	1.78	6.15	11.44/K	9.79/K
8½	1.82	6.41	11.97/K	10.19/K
9	1.87	6.76	12.51/K	10.62/K
9½	1.92	6.93	13.04/K	11.05/K
10	1.99	7.26	13,57/K	11.48/K
Addl. In.	.15	.60	1.20/K	1.00/K

EDGE CARD CONNECTORS

44 pin Solder Tall	$1.95	$17.50/10	ALL are Gold
100 pin Solder Tall	$3.95	$35.00/10	100 pin are IMSAI
100 pin Wire Wrap	$3.95	$35.00/10	spacing.

WIRE WRAP TOOLS

HOBBY WIRE WRAP TOOL

BW 630 (Back Force)	$34.95
BT 30 Extra Bit	2.95
BT 2628 #26 Bit	7.95
Batteries & Charger	11.00

FREE Wire Kit # 1 ($7.95 Value)

INDUSTRIAL WIRE WRAP TOOL

BW 928	$49.95*
BW 928BF (Back Force)	52.95*
#30 Bit & Sleeve	29.50
#26 Bit & Sleeve	29.50
Batteries & Charger	11.00

FREE Wire Kit #1 ($7.95 Value)

ELECTRICAL INDUSTRIAL WIRE WRAP TOOL

EW 7D	$85.00*
EW 7D BF (Back Force)	92.90*
#30 Bit & Sleeve	29.50
#26 Bit & Sleeve	29.50

FREE Wire Kit #1 ($7.95 Value)

*Industrial Tools do not include Bit & Sleeve
Spring Loaded bit on Back Force models.

INTERCONNECT CABLES

Ribbon cable connectors for connecting boards to front panels, or board to board.

	SINGLE ENDED			DOUBLE ENDED		
	14 pin	16 pin	24 pin	14 pin	16 pin	24 pin
6"	1.24	1.34	2.05	2.24	2.45	3.37
12"	1.33	1.44	2.24	2.33	2.55	3.92
24"	1.52	1.65	2.63	2.52	2.76	4.31
48"	1.91	2.06	3.40	2.91	3.17	5.08

OK PRODUCTS

WD 30	50 ft. Wire Dispenser Red, White, Blue, or Yellow	$3.75
WD-30-TRI	TRI Color Dispenser	5.50
R-30-TRI	Refill for TRI Color	3.75
INS 1416	14 & 16 pin Insertion Tool	3.25
MOS 40	40 pin Insertion Tool	7.50
EX-1	IC Extractor Tool	1.49
H-PCB-1	Hobby PC Board	4.99
WSU 30	Hand Wrap/Unwrap/Strip Tool	6.25
WSU 30M	Same as WSU30 with Modified Wrap	7.50

SOLDERLESS BREADBOARDS

SK 10 $16.50

2.2" x 6.5"

FREE #22 Precut wire over 100 pieces

MB10 $18.95

SK10 mounted on board W74 Binding Posts & Rubber Feet

WIRE WRAP SOCKETS

	1-9	10-24	25-99	100-249	250-999
8 pin*	.40	.36	.34	.31	.27
14 pin*	—	.39	.37	.34	.32
16 pin*	—	.42	.40	.36	.34
18 pin*	.70	.60	.55	.50	.45
20 pin	.90	.80	.75	.65	.62
22 pin*	.95	.85	.80	.70	.65
24 pin	.95	.85	.80	.70	.65
25 pin strip	1.25	1.15	1.00	.95	.90
28 pin	1.25	1.15	1.00	.95	.90
40 pin	1.65	1.45	1.35	1.20	1.10

Gold 3-Level Closed Entry Design   *End & Side Stackable
2-Level Sockets Available

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$34.95

NEW

- Compatible with all Logic Families
- 10 Nsec pulse response

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Dealer Inquiries Invited

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California Digital

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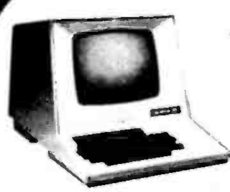
Hazeltine 1400



cost effective

CRT TERMINAL

$735 plus shipping

The Hazeltine 1400 Vidio Display Terminal is designed to optimize interactive real-time operations. The interface is capable of either local or remote connection through an EIA RS232-C interface at baud rates that are switch selectable up to 9600 baud.

- All 128 ASCII Codes
- 64 Displayable Characters
- 24 Lines; 12 inch Screen
- 80 Characters per Line
- Self Diagnostic Test

Immediate Delivery

S-100 Mother Board

Quiet Buss

$29.95

8803-18

18 slot

IMSAI

The Quiet Buss from California Industrial is quality engineered. No short cuts have been taken to produce this mother board. Active termination circuitry prevents noise and crosstalk. Manufactured from extra heavy FR-4 epoxy glass.

TELETYPE MODEL 43

Even if we have to give them away, we're going to ship more 43's in 1979 than the aggregate of all our competitors.

Model 43AAA (TTL)

EACH	3	10	25
$925.	875.	850.	825.

RS-232 Interface "K" Add $75.00 plus shipping

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SA800-R Floppy Disk Drive

The most cost effective way to store data processing information, when random recall is a prime factor. The SA800 is fully compatible with the IBM 3740 format. Write protect circuitry, low maintenance & Shugart quality.

$449.50

$29.95 BOX of 10 DISKETTES

Verbatim. APPLE/TRS-80 Mini - Soft sector

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your choice

DB25P male plug & hood

or

DB255 female

$3.95

Qty.	fe.	male	hd.
10	3.45	2.45	1.15
25	3.15	2.25	1.05
100	2.85	1.90	.95
500	2.25	1.60	.85
1K	1.97	1.37	.73

Edge Connectors

GOLD 100 PIN IMSAI/ALTAIR

Imsai solder .125x.250	$4.95	3/$10.00
Imsai w/w .125centers	$4.95	3/$13.00
Altair soldertail .140 row	$5.95	3/$15.00
SPECIALS		
22/44 Kim eyelet .156"	$1.95	3/$5.00
25/50 solder tab .156"	$1.09	3/$2.00
36/72 wide post w/w .156	$1.95	3/$5.00

SPERRY UNIVAC KEYBOARD

$24.88

The famous Sperry Univac 1710 Hollerith keyboard assembly is now available from California Industrial for only $24.88. The ideal computer input device for accountants and mathematicians. The numeric keys are placed on the lower three rows to resemble a ten key adding machine. This format allows one handed numeric data entry. Original cost was $385. Used but guaranteed in excellent condition. Complete with documentation.

World Power TRS-80 Interface

MSIOa I/O Modual	$129.95
MCCa master control	$149.95
RSBa S-100 interface	$289.95
EPR80a Eprom prog.	$159.95
EPR100a Eprom prog.	$159.95

Data sheet available upon request

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COLOR • GRAPHICS • SOUND

$1024 PLUS SHIPPING

Mfg. Sug. Retail.... $1195

Scotch Certified Digital CASSETTES

TEN for $41

50+ $3.85

Won't drop a BIT!

$5.50

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- 8 inch Soft (IBM)
- 8 inch 32 sector
- Mini Soft sec.
- Mini 10 sector
- Mini 16 sector

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APPLE RS-232

Serial Interface $59.95

Interfaces Apple II to Teletype or other serial printer.

ELECTRONIC SYSTEMS

DigiCast A/V-100

R.F. MODULATOR

$29.95 Broadcast both audio and vidio on your existing color television. Recommended for the Apple II.

Extender Board

Mullen $34.95

Facilitates design and troubleshooting of all S-100 microsystems. Includes logic probe along with high-low and pulse LED display.

Also available, the Mullin CB-1 controller board $88.

S-100 PROTOTYPE BOARD

$19.98

GP100-Maximum design versatility along with standard address decoding and buffering for S100 systems. Room for 32 uncommitted 16 pin IC's, 5 bus buffer & decoding chips, 1 DIP address select switch, a 5 volt regulator and more.

WW100-Wire wrap breadboard, similar to the GP100. Allows wire wrap of all sizes of sockets in any sizes of sockers in any combination. An extra regulator position for multiple voltage applications.

MEMORY

TRS-80 / APPLE II $65

16k memory (8) 4116's

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To obtain the best pricing on memory we have made volume commitments to our suppliers, which in turn affords us the opportunity to sell these circuits at the most competitive prices. Please contact us if you If you have a demand for volume state of the art memory products.

STATIC	1-31	32-99	100-5C	-999	1K+
21L02 450nS.	1.49	1.19	1.05	.95	.89
21L02 250nS.	1.69	1.49	1.45	*	*
2114 1Kx4 450	6.95	6.50	6.25	6.00	5.75
2114 1Kx4 300	8.95	8.50	8.00	*	*
4044 4Kx1 450	5.95	5.50	5.00	*	*
4044 4Kx1 250	9.95	9.50	9.00	*	*
4045 1Kx4 450	8.95	8.50	8.00	*	*
4045 1Kx4 250	9.95	9.50	9.00	*	*
5257 low pow.	7.95	7.50	7.05	6.75	6.45

SPECIAL CIRCUITS

Z80A 4 MHz.	24.95	AY5-1013A UART	4.95
8080A CPU	9.95	Floppy Disc Controllers	
8085	22.50	WD1771 single D.	39.95
8086 Intel 16 bits	*	WD1781 Double D	65.00
TMS9900 16 bits	49.95	WD1791 D/D 3740	*

EPROMS		1-15	16-63	64+
1702A	2K	4.95	4.50	4.00
2708	8K	9.95	9.50	9.00
2716	16K	19.95	*	*
2532	32K	*	*	*

Attention TRS-80 Owners

$650

WORD PROCESSING TERMINAL

LAWYERS, BUSINESSMEN..... This terminal, when properly interfaced to your computer, allows you the flexibility of generating computerized error free correspondence. Gives your clients and business associates the impression that each letter was personally typed for the recipient. Compose your correspondence and "Fill-in" forms on your computer, edit on your screen and when your text is letter perfect instruct your computer to print an error free copy on your terminal.

The heart of this terminal is the durable IBM Selectric Typewriter. If maintenance is ever required, the World Wide network of IBM service centers is at your disposal. The terminal is functional as a regular office typewriter when not performing computer work.

Over the next several months 150 of these terminals will be removed from service, returned to the manufacturer, inspected and brought into perfect condition. Last Spring we offered for sale two-hundred Diablo printers. Within three weeks every unit was sold. Don't pass this opportunity to purchase a word processing terminal at an excellent price.

Selectric Terminal $650 (FOB Los Angeles). Shipping to the East coast aprox. $35. Combined TRS-80 interface and power supply available. Documentation will be supplied to those individuals who want to do their own custom interfacing.

Sorry, but credit cards will not be accepted on this purchase.

Thumbwheel switch

Ten position BCD

$1.39 ea.

10	50
$1.19	.89

CAPACITORS

ELECTROLYTICS

	ea.	10	50
80,000/10v.	3.95	3.49	2.95
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1000/15v axial	$.55	.49	.45
.1 disc	$.12	.09	.07
.01 disc	.06	.05	.04

MINIATURE SWITCHES

your choice

$.98

10	50	100	1k
$.88	.81	.73	.66

SPDT Miniature Toggles

7101 C&K	ON-NONE-ON
7107 jbt	ON-OFF(mnt.ON)
7108 CK	ON-(moment. ON)
Rocker JBT	DPDT
Rotary	3P-4-Pos.
Rotary	3P-6-Pos.
Push B (N.O.)	$.39ea. 4/$1

DIP Switch

$1.49 ea.

10	25	100	1K
$1.29	1.15	.97	.83

specify 7 or 8 pos.

SPST

DISCOUNT Wire Wrap Center

IC SOCKETS

pin	wire wrap ea.	25	50	low profile ea.	25	50
8	—			17¢	16	15
14	37¢	36	35	18	17	16
16	38	37	36	19	18	17
24	99	93	85	36	35	34
40	169	155	139	63	60	58

Soft. $.98

KYNAR WIRE WRAP

500	1,000	11,000
$9.	$15.	$105.

wire wrapping tool

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OK HOBBY WRAP-30 wire wrap & strip tool

$5.45

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All merchandise sold by California Digital is premium grade. Sorry, no COD's. Orders are shipped the same day received. California residents add 6%. Foreign orders add 10%. Orders over $25, when accompanied by payment, are shipped at our expense. Otherwise, please add $2.

VISA master charge

Circle 39 on inquiry card.

Ham Interface for the PET Microcomputer

The M-65 is a complete Morse code and radioteletypewriter (RTTY) system for the PET microcomputer. The hardware consists of a printed circuit board which plugs into a jack on the radio equipment and the PET user port. No external power is required. Both input and output circuits are optically isolated from the PET, minimizing radio frequency interference and spurious voltages. The board has a built-in side tone oscillator which connects to the speaker or headphone.

The software consists of two computer programs: Morse and RTTY, which are supplied on one audio cassette. Both programs are written in BASIC with machine language subprograms, and each requires 8 K bytes of programmable memory.

The M-65 is available in kit form for \$69.95 or fully assembled and tested for \$99.95. Contact Microtronics, 5943 Pioneer Rd, Hughson CA 95326.■

Circle 653 on inquiry card.

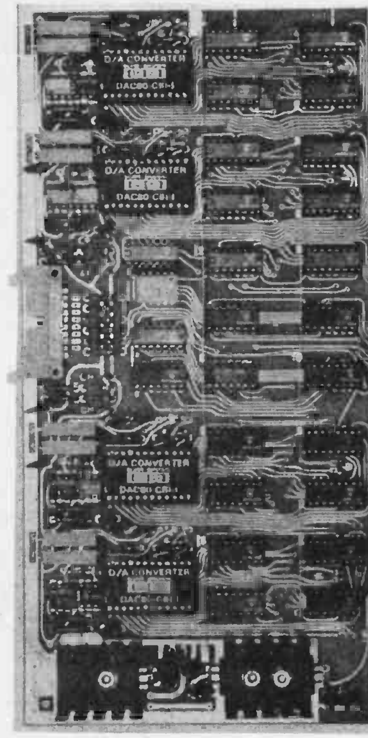
S-100 Bus Compatible 4 Channel Digital to Analog Converter

This 4 channel digital to analog converter is available for use with Z-80 or 8080/8085 processors. The S-100 bus compatible digital to analog board has 12 bit resolution and uses plug-in hybrid digital to analog converters with ±0.5 least significant bit accuracy. Power requirements are compatible with S-100 bus voltages: +8 V at 338 mA, +18 V at 122 mA, and −18 V at 156 mA.

The output is 10 V or 20 V full scale (strap selectable). The output range may be ±5 V, ±10 V, 0 to +10 V, or 0 to −10 V. An inversion strap is also provided for decreasing output with increasing input. Output current is 10 mA. Independent gain and offset adjustments are provided. Input coding may be either binary or 2's complement. Conversion speed is 3 μs typical, and the converter slew rate is 20 V per μs typical.

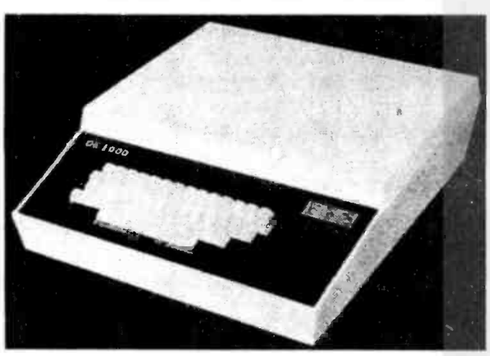
The price is \$495. Contact California Data Corp, 3475 Old Conejo Rd, Suite C10, Newbury Park CA 91320.■

Circle 654 on inquiry card.



New Terminal Outputs Composite Video

The OE 1000 terminal is designed to interface to any microcomputer that has



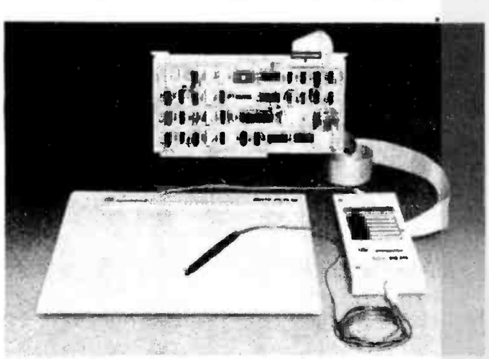
a 300 bps serial data output port. It operates in the full duplex mode with either 20 mA current loop or RS-232 voltage swing. The OE 1000 outputs composite video for use with a modified television or a video monitor. The screen format is 16 lines by 64 characters. It has an upper and lower case mode or Teletype mode keyboard and will display 96 ASCII characters and 32 special characters. The OE 1000 has full cursor control, automatic scroll, erase to end of line, erase to end of screen, and clear screen.

The terminal is available as a kit for \$275 or assembled for \$350. Contact Otto Electronics, POB 3066, Princeton NJ 08540.■

Circle 655 on inquiry card.

Digitizer for Small Computer Systems

Summagraphics has announced a new version of its Bit Pad, the digitizer for



small computer systems. The new Bit Pad configuration is Intel Multibus compatible. The Bit Pad can now be plugged into the Multibus along with Single Board Computers (SBC), memory and input/output (I/O) boards, peripherals and controllers.

All electronics are located on one SBC card. Operational control and status indication is provided from a small handheld console. The system also includes an 11 by 11 inch (27.94 by 27.94 cm) Bit Pad tablet and a date input stylus.

The basic Multibus Bit Pad configuration is priced at \$625. For further information contact Summagraphics, 32 Brentwood Av, POB 781, Fairfield CT 06430.■

Circle 656 on inquiry card.

PerSci's New 4 Headed Voice Coil Floppy

A 4 headed flexible disk drive has been introduced by PerSci Inc, 12210 Nebraska Av, W Los Angeles CA 90025. The Model 299 diskette drive interfaces to 8080, 6800 and Z-80 systems, as well as minicomputers.

The Model 299 is a dual-headed, dual diskette drive, reading and writing both sides of two 8 inch diskettes. Data can be encoded in single or double density in IBM compatible soft sectored formats or expanded hard and soft sectored formats on IBM Diskette I, II, IID or equivalent media. The drive will store up to 1 M byte of data in IBM type format, 1.6 M bytes unformatted single density and up to 3.2 M bytes in unformatted double density encoding.

The operational tolerances required to achieve dual head, dual drive double density data handling are provided by PerSci's voice coil positioning system for an average seek time of 33 ms (including 0 settle time), five to seven times faster than stepper motor positioned drives. A full stroke 76 track seek is performed in 100 ms. The speed and the capacity of the drive are achieved while maintaining industry standard data reliability figures of 1 in 10^9 soft errors and 1 in 10^{12} hard errors.

The Model 299 features electric autoload and can be unloaded by remote software control. Optical write protect secures the file.

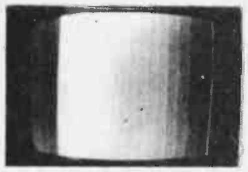
The price is \$1595 in single unit quantities.■

Circle 657 on inquiry card.

SOLID STATE SALES. . . *Announces a Breakthrough in Computer Technology*

A PICTURE MAY BE TAKEN BY OUR CAMERA, STORED IN A COMPUTER IN REAL TIME AND THEN DISPLAYED ON A CRT AT AN AFFORDABLE PRICE

VIDEO COMPUTER PROCESSING SYSTEM



GRAY LEVELS

THIS REMARKABLE VP-1 COMPUTER/ INTERFACE KIT HAS THE FOLLOWING:

FEATURES

- IT PRODUCES COMPOSITE VIDEO OUTPUT IN A 128 × 128 MATRIX FROM A DIRECT MONITOR CONNECTION USING 8K OF MEMORY
- THE SYSTEM USES A STANDARD S 100 BUSS
- WILL NOT TIE UP COMPUTER SOFTWARE WHEN NOT ADDRESSED
- IT DISPLAYS CONTINUOUSLY WHEN NOT ADDRESSED
- IT MAY PRODUCE PSEUDO COLOR AND/OR GRAPHICS (UP TO 16 GREY LEVELS, 4 BIT BINARY)

THE CAMERA WILL TAKE BETWEEN 15 AND 100 FRAMES/SECOND. THE CAMERA CONNECTS TO THE PROCESSOR WITH SEVEN LINES. THIS INCLUDES VIDEO AND TIMING SIGNALS

APPLICATIONS

- CONTINUOUS SURVEILLANCE
- INSPECTION OF MOVING PARTS WITH PROPER STROBING
- VISUAL GRAPHIC INPUT TO A COMPUTER
- CHARACTER OR PATTERN RECOGNITION
- PICTURES MAY BE TAKEN DIRECTLY FROM A TV WITHOUT ELECTRICAL CONNECTIONS
- THE INTERFACE KIT MAY BE USED SEPARATELY AS A 128 × 128 16 LEVEL GRAPHIC DISPLAY

OUR VP1 VIDEO SYSTEM CONSISTS OF THE FOLLOWING KITS:

- CCD 202C SOLID STATE VIDEO CAMERA KIT (CASE INCLUDED) . $399.00
- VP-1 COMPUTER/VIDEO INTERFACE KIT (3 BOARDS) $599.00
- ASSEMBLED 8K MEMORY BOARD (OPTIONAL) $235.00

THIS VIDEO COMPUTER KIT CAN WORK WITH THE GE, REDICON, OR ANY OTHER 128 × 128 SENSOR CAMERA

REGULATED POWER SUPPLIES

POWER SYSTEMS # PS1111
115-230V 50/60 cy. in 5v DC at 35A out.
6"x 16¾"x 15¼" 26 lbs. shipping weight $85.00

POWER SYSTEMS # PS1106
115-230V 50/60 cy. in 12v DC at 15A out
5"x 16¾"x 5" 19 lbs. shipping weight. $75.00
(OV PROTECT)

C/MOS (DIODE CLAMPED)

4001	.18	4019	.37	4049	.35	74C74	.45
4002	.18	4020	.90	4050	.35	74C83	1.15
4006	.95	4021	.90	4053	1.10	74C86	.40
4007	.18	4022	.90	4055	1.25	74C93	.75
4009	.37	4023	.18	4066	.70	74C151	1.40
4010	.37	4024	.75	4071	.18	74C160	1.05
4011	.18	4025	.18	4076	.97	74C161	1.05
4012	.18	4027	.37	4520	.70	74C174	1.05
4013	.29	4028	.80	74C00	.22	74C175	1.05
4014	.75	4029	.95	74C02	.22	74C192	1.20
4015	.75	4030	.33	74C04	.24	74C193	1.20
4016	.29	4035	.97	74C08	.22	74C901	.48
4017	.90	4042	.65	74C10	.27	74C902	.48
4018	.90	4046	1.35	74C73	.65	74C914	1.70

1488 RS232 INTERFACE	$1.40	UPD410 1 4K STAT. RAM	8.95
1489 RS232 INTERFACE	1.75	4116	11.50
2508 TRI STATE STAT. SR	1.35	5280/2107B 4K DYN RAM	3.40
2513 CHARAC. GEN. UP.	6.75	TMS 4050L	3.95
2516 HEX 32 BIT SR	2.20	5204 4K PROM	4.95
2522 STATIC SHIFT REG	1.95	82S23	1.95
2708 8K EPROM (450 ns)	8.60	82S129	3.25
TMS 3409 NC 80 BITS DYN S.R.	1.35	AY5 1013 UART	6.75
2716 (TI)	35.95	TR1 602B	4.95
2102-1 (450 ns)	.99	8700C TELEDYNE 8 BIT AD CONVERT	9.25
21L02-1 (450 ns)	1.25	PT 1482 B PSAT	6.95
MM5270 4K x 1 DYN	3.45	8080A	7.75
MK4008P	1.95	8212	2.25
2101-1 256 x 4 STATIC	2.45	8216	2.25
2111-1 256 x 4 STATIC	3.45	8224	2.95
2112-1 256 x 4 STATIC	2.75	8251	4.50
2114 4K STAT. RAM (450 ns)	8.50	8255	5.50
2107 16K DYN RAM	8.95		

8130 — 3.50 8830 — 3.50 8837 — 2.25
8131 — 3.50 8834 — 2.25 8838 — 2.25

CRYSTALS $3.45 ea.
4.000 MHz
5.000 MHz
6.000 MHz
8.000 MHz
10.000 MHz
20.000 MHz

RIBBON CABLE FLAT (COLOR CODED) #30 WIRE
26 cond. - .50/per foot
40 cond. - .75/per foot
50 cond. - .90/per foot

CTS 206-8 eight position dip switch $1.60
CTS-206-4 four position dip switch $1.45
LIGHT ACTIVATED SCR's TO 18, 200V 1A $ .70

SILICON SOLAR CELLS
2¼" diameter .4V at 500 ma $4.00

LED READOUTS
FND 359 C.C. .4" $ .50
FCS 8024 4 digit C.C. 8" display $5.95
FND 503 C.C. .5" $ .85
FND 510 C.A. .5" $ .85
DL-704 .3" C.C. $ .85
DL-704 C.A. .3" $ .75
DL 747 C.A. .6" $1.25
HP3400 .8"CC $1.95
HP3405 .8"CA $1.95

PRINTED CIRCUIT BOARD

4-1/2"x6-1/2" SINGLE SIDED EPOXY BOARD 1/16" thick, unetched $.60 ea. . . . . 5/$2.60

7 WATT LD-65 LASER DIODE IR $8.95

2N 3820 P FET $ .45
2N 5457 N FET $ .45
2N2646 UJT $ .45
ER 900 TRIGGER DIODES 4 $1.00
2N 6028 PROG UJT $ .65

MINIATURE MULTI-TURN TRIM POTS
100, 1K, 2K, 5K, 10K, 20K, 50K, 200K, 1Meg, 2Meg, $.75 each 3/$2.00

CHARGED COUPLE DEVICES
CCD 201C 100x100 Image Sensor $95.00
CCD 202C 100x100 Image Sensor $145.00

VERIPAX PC BOARD $4.00
This board is a 1/16" single sided paper epoxy board, 4½"x6½" DRILLED and ETCHED which will hold up to 21 single 14 pin IC's or 8,16 or LSI DIP IC's with busses for power supply connector.

FP 100 PHOTO TRANS . . . . $ .50
RED, YELLOW, GREEN or AMBER LARGE LED's .2" . . . . 6/$1.00
TIL-118 OPTO-ISOLATOR . . . . $ .75
MCT-6 OPTO ISOLATOR . . . . $ .80
1 WATT ZENERS: 3.3, 4.7, 5.1, 5.6, 9.1, 10 12, 15, 18, or 22V . . . . 6/$1.00
MCM 6571A 7 x 9 character gen ... $10.75

Silicon Power Rectifiers

PRV	1A	3A	12A	50A	125A	240A
100	.06	.14	.30	.80	3.70	5.00
200	.07	.20	.35	1.15	4.25	6.50
400	.09	.25	.50	1.40	6.50	9.50
600	.11	.30	.70	1.80	8.50	12.50
800	.15	.35	.90	2.30	10.50	16.50
1000	.20	.45	1.10	2.75	12.50	20.00

SAD 1024 a REDICON 1024 stage analog "Bucket Brigade" shift register. $14.95

IN 4148 (IN914) 15/$1.00

RS232 CONNECTORS
DB 25P male $2.25
DB 25S female $2.95
HOODS $1.00

REGULATORS

309K . . . . . . $ 1.10
723 . . . . . . $ .50
LM 376 . . . . $ .60
320T-5, 12, 15 or 24 . . . . $1.10
340K-12, 15 or 24V. . . . $1.10
340T-5, 6, 8, 12 15, 18 or 24V $1.10
78 MG $1.35
79 MG $1.35

TRANSISTOR SPECIALS

2N6233-NPN SWITCHING POWER $ 1.95
MRF-8004 a CB RF Transistor NPN $ .75
2N3772 NPN Si TO 3 $ 1.00
2N1546 PNP GE TO-3 . . . . $ .75
2N4908 PNP Si TO 3 $ 1.00
2N5086 PNP Si TO 92 4 $ 1.00
2N3137 NPN Si RF . . . . $ .55
2N3919 NPN Si TO 3 RF $ 1.50
2N1420 NPN Si TO 5 . . . . 3/$ 1.00
2N3767 NPN Si TO 66 $ .70
2N2222 NPN Si TO 18 5/$ 1.00
2N3055 NPN Si TO-3 $ .50
2N3904 NPN Si TO 92 6/$ 1.00
2N3906 PNP Si TO 92 6/$ 1.00
2N5296 NPN Si TO-220 $ .50
2N6109 PNP Si TO 220 $ .55
2N3638 PNP Si TO 5 5/$ 1.00
MPSA 13 NPN Si. . . . . 4/$ 1.00

TTL IC SERIES

		7446	.08	74153	.61
		7447	.58	74154	.94
7400	.15	7448	.68	74155	.58
7401	.16	7450	.18	74157	.56
7402	.15	7472	.25	74158	.65
7403	.16	7473	.28	74161	.55
7404	.18	7474	.28	74162	.80
7405	.18	7475	.45	74163	.56
7406	.22	7476	.30	74164	.85
7407	.24	7480	.31	74165	.95
7408	.18	7483	.65	74170	1.68
7409	.18	7485	.87	74173	1.20
7410	.16	7486	.28	74174	.95
7411	.18	7489	1.25	74175	.85
7412	.18	7490	.42	74176	.75
7413	.36	7491	.58	74177	.75
7414	.60	7492	.43	74180	.65
7416	.22	7493	.43	74181	1.90
7417	.25	7494	.67	74190	1.00
7420	.18	7495	.65	74191	.85
7425	.30	7496	.65	74192	.70
7426	.22	7497	.90	74193	.79
7427	.28	74107	.28	74194	.80
7430	.16	74121	.30	74195	.60
7432	.22	74122	.40	74196	.86
7437	.22	74123	.45	74197	.80
7438	.22	74125	.40	74273	.55
7440	.18	74126	.40	74298	.90
7441	.70	74148	1.10	74363	.62
7442	.45	74150	1.00	74391	1.75
7445	.65	74151	.61	74325	1.50

DATA CASSETTES 1/2 HR $ .95

14 pin headers 3/$1.00

MM 5387AA new clock chip which will directly drive LED's 12/24 hrs., 1 supply & alarm $5.95

NO. 30 WIRE WRAP WIRE SINGLE STRAND 100' $1.40

ALCO MINIATURE TOGGLE SWITCHES
MTA 106 SPDT . . . . $ .95
MTA 206 DPDT . . . . $ 1.70
MTA 206 P-DPDT CENTER OFF $ 1.85
MSD 206 P-DPDT CENTER OFF LEVER SWITCH . . . . $ 1.85

Full Wave Bridges

PRV	2A	6A	25A
100			1.30
200	.75	1.25	2.00
400	.95	1.50	3.00
600	1.20	1.75	4.00

DIP SOCKETS

8 PIN .17 24 PIN .35
14 PIN .20 28 PIN .40
16 PIN .22 40 PIN .60
18 PIN .25

SANKEN AUDIO POWER AMPS

Si 1010 G 10 WATTS . . . . $ 7.80
Si 1020 G 20 WATTS $15.70
Si 1050 G 50 WATTS $28.50

TANTULUM CAPACITORS

22UF 35V	5/$1.00	6.8UF 35V	4 $1.00
47UF 35V	5 $1.00	10UF 10V	$ .25
68UF 35V	5 $1.00	22UF 25V	$ .40
1UF 35V	5 $1.00	15UF 35V	3/$1.00
2.2 UF 20V	5 $1.00	30UF 6V	5/$1.00
3.3UF 20V	4 $1.00	47UF 20V	$ .35
4.7UF 15V	5/$1.00	68 UF 15V	$ .50

74LS SERIES

74LS00	.23	74LS132	.70
74LS02	.23	74LS138	.70
74LS03	.23	74LS139	.70
74LS04	.25	74LS151	.85
74LS05	.25	74LS153	.85
74LS08	.25	74LS155	.68
74LS09	.25	74LS156	.68
74LS10	.23	74LS157	.68
74LS11	.23	74LS160	.90
74LS13	.44	74LS161	.90
74LS14	.80	74LS162	.90
74LS15	.23	74LS163	.90
74LS20	.23	74LS168	1.05
74LS21	.23	74LS169	1.05
74LS22	.23	74LS170	1.40
74LS26	.29	74LS173	1.20
74LS27	.29	74LS174	1.00
74LS28	.29	74LS175	1.00
74LS30	.23	74LS181	2.20
74LS32	.29	74LS190	1.10
74LS37	.28	74LS191	1.10
74LS38	.28	74LS192	.89
74LS40	.23	74LS193	1.10
74LS42	.65	74LS195	.80
74LS47	.73	74LS196	.60
74LS51	.25	74LS197	.80
74LS54	.25	74LS241	2.50
74LS73	.35	74LS257	.88
74LS74	.36	74LS258	.89
74LS75	.50	74LS259	1.35
74LS76	.36	74LS265	.30
74LS85	.80	74LS266	.39
74LS86	.35	74LS279	.70
74LS90	.50	74LS290	.60
74LS92	.50	74LS293	.68
74LS93	.50	74LS365	.60
74LS109	.35	74LS366	.60
74LS112	.35	74LS368	.60
74LS113	.35	74LS375	.70
74LS114	.35	74LS386	.35
74LS125	.45	74LS390	1.45
74LS126	.45	74LS670	2.00

LINEAR CIRCUITS

LM 101	.75
LM 301/748	.25
LM307	.30
LM 308	.75
LM 311	.75
LM 318	1.20
LM 324	.70
LM 339	1.10
LM 358	.70
LM 370	1.15
LM 377	1.60
LM 380	.95
LM 382	1.25
LM386	.80
LM 387	1.25
LM 537	2.50
LM 553	2.50
LM 555	.39
LM 556	.85
NE540L	2.25
560	2.00
565	.95
566	1.10
567	1.10
703	.90
733H	.75
592H	.95
709	.25
710	.35
741C or V	.25
747	.50
LM 1310	2.50
1456	.95
1458	.50
3900	.40
8038CC	3.90
791	1.95
LF356H	1.20

TRIACS / SCR'S

PRV	TRIACS 1A	TRIACS 10A	TRIACS 25A	SCR'S 1.5A	SCR'S 6A	SCR'S 35A
100	.40	.70	1.30	.40	.50	1.20
200	.70	1.10	1.75	.60	.70	1.60
400	1.10	1.60	2.60	1.00	1.20	2.20
600	1.70	2.30	3.60		1.50	3.00

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Circle 340 on inquiry card.

Early-Bird Specials...

Circle 296 on inquiry card.

Daisy Wheel Printers

•**SELECTRIC I/O TERMINALS** (by GTE/Information Systems). Both ASCII & IBM code versions with microcomputer interface software & hardware (RS-232 connector.) Cassette drive models permit up to 2400 baud data transfer rate as well as off-line data storage, use as memory typewriter, & use as data entry device for office personnel familiar with Selectric typewriters but not computers. Wide-carriage, interchangeable type spheres; optional built-in modem. All units cleaned, adjusted & warranted.

- Model 5541 (IBM Correspondence code) $695.00
- Model 5550 (corres. code, built-in cassette drive) $1195.00
- Model 5560 (ASCII code, built-in cassette drive) $1295.00

•**IBM SELECTRIC 725 TYPEWRITER I/O** w/solenoids switches & magnet driver PCB (from GTE/IS terminal) plus instructions for 8080 printer-driver interface hardware & software.

- a) Typewriter mechanism complete, cleaned & adjusted $375.00
- b) Case from terminal & power supply (+24V, ±12V, +5V @5A) . . $ 75.00
- c) a & b plus output ASCII interface to mCPU 8-bit parallel port . $600.00

•**POS 103/202 *"MIX or MATCH"* MODEM:** BELL 103 and/or BELL 202 FREQUENCIES: Unique POS control design permits use in one housing of both Bell-compatible 103 (0 – 300 baud) and 202 (0 – 1200 baud) modem modules originally made by VADIC Corp. for a telephone company subsidiary. FEATURES: RS-232 serial interface, auto-answer, auto-dial, LED display, telephone line interface via acoustic coupler, manual DAA, or auto-answer DAA (sold separately.) FULLY ADJUSTED; no special tools required; 3,000 mile range over standard dial-up telephone lines.

- –POS 103 MODEM (with Auto Answer, Auto Dial) $179.95
- –POS 202 MODEM (Half-Duplex with Reverse Channel) $249.95
- –POS 202 MODEM (Half-Duplex w/Rev. Ch., Auto-Answer) $279.95
- –POS 103/202 MODEM (Auto-Answer, Auto-Dial) $399.95

•**DIABLO HYTYPE I** Model 1200 Printer Mechanism: used, complete and operational. Requires power supply, case & mCPU interface. 15 day return privilege – no other warranties. LIMITED QUANTITY! $750.00

- –6' Ribbon cable & connector for printer Main Logic PCB $10.00
- –14-pin Winchester connector & 18" power supply cable $5.00
- –"As-is" spare printer PCB's for parts (Logic, Heat Sink, Control): ea. $20.00

•**NEW TAPE DRIVE CONTROLLER for Microcomputer:** POS Version II tape drive controller is now available, permitting the 8080 or Z-80 owner to read and write standard IBM NRZ1 format tapes (as well as ASCII tapes) with the Ampex Model TMX tape drive described below. Controller is sold only with tape drive, comes complete with connector cables to CPU and software listing in 8080 assembly language (specify 2MHz or 4MHz system.)

- –Ampex TMX tape drive (used) with Version II Controller $1500.00

•**AMPEX MODEL TMX TAPE DRIVE:** Ideal for microcomputerist who wants backup mass storage or access to IBM-type systems via standardized 2400 series ½" mag tape. Specs: 9-track, NRZ1 standard, 800 BPI, 12"/sec., 1200 ft. reels (11 megabyte capacity.) Drive is like new & comes with 8-bit CPU controller diagram (requires only 11 I/C's) & mCPU interface instructions.

Prices: Drive & Documentation $750.00
Controller & cable for mCPU, assembled & tested $250.00

•**DIGITAL CASSETTE DRIVE** (from GTE/IS Terminal): 1800 baud, 6"/sec: AC motor; fwd/rewnd circuitry plus tape head, no read/write electronics $25.

•**FORMS TRACTORS**, Moore Variable width "Form A-Liner" for print terminals:

- a) Model 565P for 15" Carriage IBM Selectrics (new): $50.00
- b) Model K81 for QUME or DIABLO Hytype I or II printers (new): $90.00

•**POWER SUPPLIES** for Disk Drive, mCPU, tested under load shown:

- –No. 519 (w/fan & AC cord): +5V reg., ±12V reg., +24V, @5A (10 lb.) . . $29.95
- –LAMBDA No. LMEE5 w/OV protect: +5V reg. @ 25A (35 lb.) $59.95

NO RISK! 15 DAY APPROVAL ON ALL MAIL-ORDERS

Full documentation included PLUS Interface instructions where indicated. All equipment is shipped insured FOB Palo Alto within 14 days after check clears or COD order is received. Prices may change without notice.

PACIFIC OFFICE SYSTEMS, INC.
2600 El Camino Real, Suite 502
Palo Alto, Calif. 94306
(415) 321-3866

Call or write for details, quantity prices, catalog. 15 day return privilege PLUS 90 day no charge replacement of defective parts. All orders shipped from stock. No back orders, no substitutions. M/C & VISA accepted.

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10 Watt · 20 Watt · 30 Watt · 50 Watt
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- Multi-purpose linear amplifiers for comercial and industrial applications.
- Less than 0.5% harmonic distortion at full power level.
- ½ dB response from 20 to 100,000 Hz.
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- Rugged, compact and lightweight packages.
- Built-in current limiting for SI-1050G and efficient heat radiating construction.

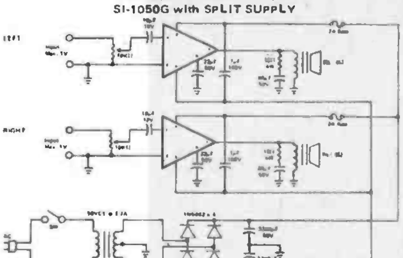
SANKEN Series SI-1000G Amplifiers are self-contained power hybrid amplifiers designed for Hi-Fi, stereo, musical instruments, public address systems and other audio applications. The amplifiers have quasi-complementary class B output. The circuit employs flip-chip transistors with high reliability and passivated chip power transistors with excellent secondary breakdown strength. Built-in current limiting is provided for SI-1050G and all devices can be operated from a single or split power supply.

Power Amplifier			* Matching Transformer	
P/N	Power	Price	P/N	Price
SI-1010G	(10W)	$ 6.95	TR10	$ 7.90
SI-1020G	(20W)	$13.95	TR20	$10.90
A-SI-8	(Socket for above)			.95
SI-1030G	(30W)	$19.00	TR30	$12.90
SI-1050G	(50W)	$27.80	TR50	$17.90
A-SI-10	(Socket for above)			.95

*Note: One Transformer can power two Sanken audio amplifier modules.

Data Sheet with application Notes–$ .50

TYPICAL CONNECTIONS
SI-1050G with SPLIT SUPPLY



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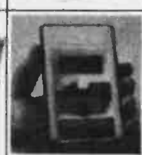

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1858LD	5.65	1858LE	1.45
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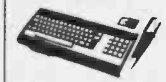

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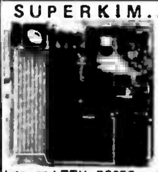

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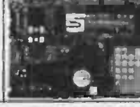

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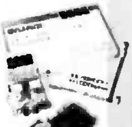

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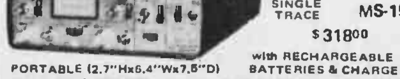

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Circle 11 on inquiry card.

Unclassified Ads

FOR SALE OR TRADE: Interdata Model 1 minicomputers. One complete and working, another lacking one board. 10 K core memory. $400 or best offer. Gary Sawyer, 3952 Ash St, Irvine CA 92714, (714) 559-0243.

HELP: We have a SwTPC terminal (TV II) and would like to use it as a character generator for our TV studio. To do this, the terminal has to be synchronized externally. Can anyone send plans or ideas to do this by either stripping the present sync and adding the new, or by rebuilding portions of the terminal to accept external synchronization? Ken Pavlicek, Lyons Township High School, 4900 Willow Springs Rd, Western Springs IL 60558.

FOR SALE: TRS-80, LEVEL I, 4 K complete with video, power pack, cassette recorder, keyboard, original carton, manuals, and software. Perfect condition, I pay the freight. $490. Mark Baiada, 271 Winding Ln, Cinnaminson NJ 08077. Call collect (609) 829-9310 after 6 PM.

FOR SALE: One Anderson Jacobsen 841 Terminal with 6 bit EBCO code 10 CPS. IBM Selectric keyboard. Good Condition. $1000 FOB truck. Alan C Page, Green Diamond Forestry Service Inc, Blue Meadow Road, Belchertown MA 01007.

FOR SALE: 64 22 pin 3 level tin wire wrap sockets, $8 per 16. 58 TMS-4060 4 K programmable memory chips, $15 per 29 (bought surplus from Honeywell; never used but not guaranteed). Money order or cashier's check. James Phillips, 3435 N 75th Dr, Phoenix AZ 85033, (602) 849-6937.

FOR SALE: Heathkit H11 large scale integration computer with 4 K memory; serial and parallel interface, plus extended arithmetic chip. H10 paper reader/punch up and running and factory tested. Asking $1900 and I will ship. Jim Thebeault, Rt 12 Box 94, Mansfield OH 44903, (419) 468-4700.

FOR SALE: Viatron Cassette decks, dual heads and motors, excellent foundation unit for mass storage system. Good documentation with all schematics. $70 for pair or $38 single units. Money order or certified check. Shipped post paid. V Caggia, 15 Lovell Dr, Wanaque NJ 07465, (201) 835-2477.

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FREE: Software and blank diskettes with the purchase of the minifloppy with the best cost/performance ratio available, the Micropolis Macrofloppy. Normally $835 for drive, S-100 controller, cables, and blank diskettes new; the first check or money order over $750 takes a factory assembled and tested system (only two months old and working beautifully, with the software and blanks added as a bonus). Contact David or Robert Mason, 503 Timber Ter, Houston TX 77024, (731) 681-3427 after 7 PM.

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FOR SALE: September 1975 thru September 1976 BYTE. Best offer over $75, all other BYTEs to date. Make offer, C Ernst, 215 E Costilla Av, Littleton CO 80122, (303) 794-5667.

FOR SALE: High quality terminal priced to sell, QUME (300Q), rebuilt and reconditioned ASCII, RS232, 55 characters per second, over 70 software commands, super graphics, still in warranty. $2250. Pat Reynolds, 4903 Hirsch, Houston TX 77026, (713) 674-8367.

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FOR SALE: Heath H8, 16 K memory, two H8-5s, cassette, extended BASIC; up and running. $900 or best offer. Ten new 8 inch disks, make offer. Andy Thornburg, RR2, Thompsonville IL 62890, (618) 627-2166.

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FOR TRADE: Famous 8080 FORTRAN MITS disk version for 8080 COBOL or MITS timesharing BASIC. Manuals available. K R Roberts, 10560 Main St, Suite 515, Fairfax VA 22030.

FOR SALE: Video display terminals; industrial quality display terminals with ASCII keyboard; 12.5 MHz display bandwidth; pictures available. Comes complete ready to plug in at $215 plus shipping. Works great with S-100, Digital Group and other boards. Also available with other options such as 16 by 64 character generation logic, composite (TV) video input, or customized to your specifications. S Stoddard, 12 Kathy Dr, Poquoson VA 23662, (804) 868-7682.

FOR SALE: Technico TMS-9900 processor, 16 bit, with 2 K programmable memory, 2 K read only memory (monitor and Assembler), 2 K erasable programmable memory and programmer. Documentation, manuals and cables. Factory tested, never used. $275. S J Huber, 318 Steven Ct, Benicia CA 94510, (707) 745-8089.

FOR SALE: 8 K PET commodore with second tape cassette unit, games, manuals, as new. $695. John Clarke, 13609 Luscern, Dunlap IL 61525, (309) 243-7584.

SACRIFICE: New Univac type 079 incremental printer. Still in packing crate. Adjustable 132 column tractor feed. 30 characters per second. Hinged top with glass window enclosure and stand. Mechanism alone cost $1800. Three cases fanfold paper. $575 plus shipping. Do not phone. Write for details and picture. David Krivoshik, 18 Newcomb Pl, Elizabeth NJ 07202.

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DIGITAL USERS: Repair, trade, buy, and assemble Digital Group equipment. For more information, write: Michelle, POB 30098, Boulder CO 80307.

FOR SALE: Heath H9 terminal fully assembled, checked out (by Heath), and operational, $500. I will deliver to eastern MA or southern NH. Otherwise add shipping. Lawrence Woods, 12 Patten St, Watertown MA 02172.

FOR SALE: Two Shugart SA-400 Minifloppy disk drives; includes manual. $275 each or both for $500. J Lightsey, 339 Deer Trail Rd, Boulder CO 80302, (303) 443-7888.

FOR SALE: Two SSM 450 ns 8 K programmable memory boards, assembled and running, (S-100), $80 each. One SSM 450 ns 4 K programmable memory board, assembled and running, (S-100), $60. First money order or cashier's check takes it, all others returned. I pay shipping. Vance Navarrette, 2057 S W Leewood Ln, Aloha OR 97005.

XITAN USERS: Information exchange group formed to facilitate finding each other and sharing our work. Send a short description of your applications and any hardware tips or software you wish to exchange or sell to Dr John R Cameron, POB 1517, Palo Alto CA 94301. Enclose $3 if you wish to receive copies of others' offerings.

FOR SALE: Used computer equipment — three General Automation 16/220 computers, controllers; three GE Terminet 310 line printers; three Hazeltine 1500 video terminals; six Diablo Hy-Term Printers 1620-3. Relate best offer to Mr Ralph P Price, Sun Information Services, 656 E Swedesford Road, Wayne PA 19087, (215) 293-8242.

FOR SALE: PET 8 K. Reasonable offer considered. R White, 5752 N Milwaukee Av, Chicago IL 60646.

FOR SALE: New Noval 765 microcomputer system in a desk including dual Shugart 400 minifloppy drives, controller, Z-80 processor with 32 K programmable memory and 16 K read only memory, built-in 12 inch high resolution (256 by 256) graphics videoterminal, keyboard, and built-in 32 column dot matrix printer. System cost $5990, asking $3990. Included are seven programmed minifloppy diskettes plus operator's manuals with diskette operating system on read only memory, and Extended BASIC on diskette. Esther Robinson, 16689 Mt Cachuma Cir, Fountain Valley CA 92708, (714) 554-3914.

FOR SALE: Heathkit H-11 16 bit computer with 12 K memory and serial and parallel interfaces. Heathkit H-9 video terminal. Both fully assembled and tested. Needs only paper tape or floppy disk unit to complete system. Cannot complete — need money for graduate school tuition. Will sell at kit price. Fred Graefe, 309 Harrison Av, Roselle NJ 07203, (201) 245-4930.

FOR SALE: Complete KIM-1 System; BASIC board; 3 K programmable memory, 1 K erasable programmable memory, PIA I/O (input/output), video I/O, Hefty power supply, chassis, mother board, plug-in 44 connector boards, ASCII keyboard, cables. Extra 6502, PIA's available. $225 or best offer. Bill Carlquist, 6253 Hollywood Blvd, Suite 202, Hollywood CA 90028, (213) 461-4643.

WANTED: TRS-80 computers wanted. Any condition, any quantity. Immediate cash. Also for sale; DEC PDP8 e, f, m; also all peripherals. K2DCY. POB 632; W Caldwell NJ 07006, (201) 226-9185.

FOR SALE: Processor Technology VDM-1, $130 plus postage. KIM-4 mother board, $85 plus postage. Bruce McIntire, 807 Bejay Pl, San Pedro CA 90731, (213) 831-1844.

TRADE: Star Trek program, TRS-80 BASIC I or II, source code. Well tested and documented. Send your program to Daniel Napoli, 112 N Walnut St, Beacon NY 12508.

FOR SALE: Processor Technology (GPM) general purpose memory module with ALS-8, SIM-1 and TXT-2 read only memories. All in good working condition. Complete with hardware and ALS-8 manuals. $275 or best offer. Joe Hartnett, 2323 N Woodlawn, Wichita KS 67220.■

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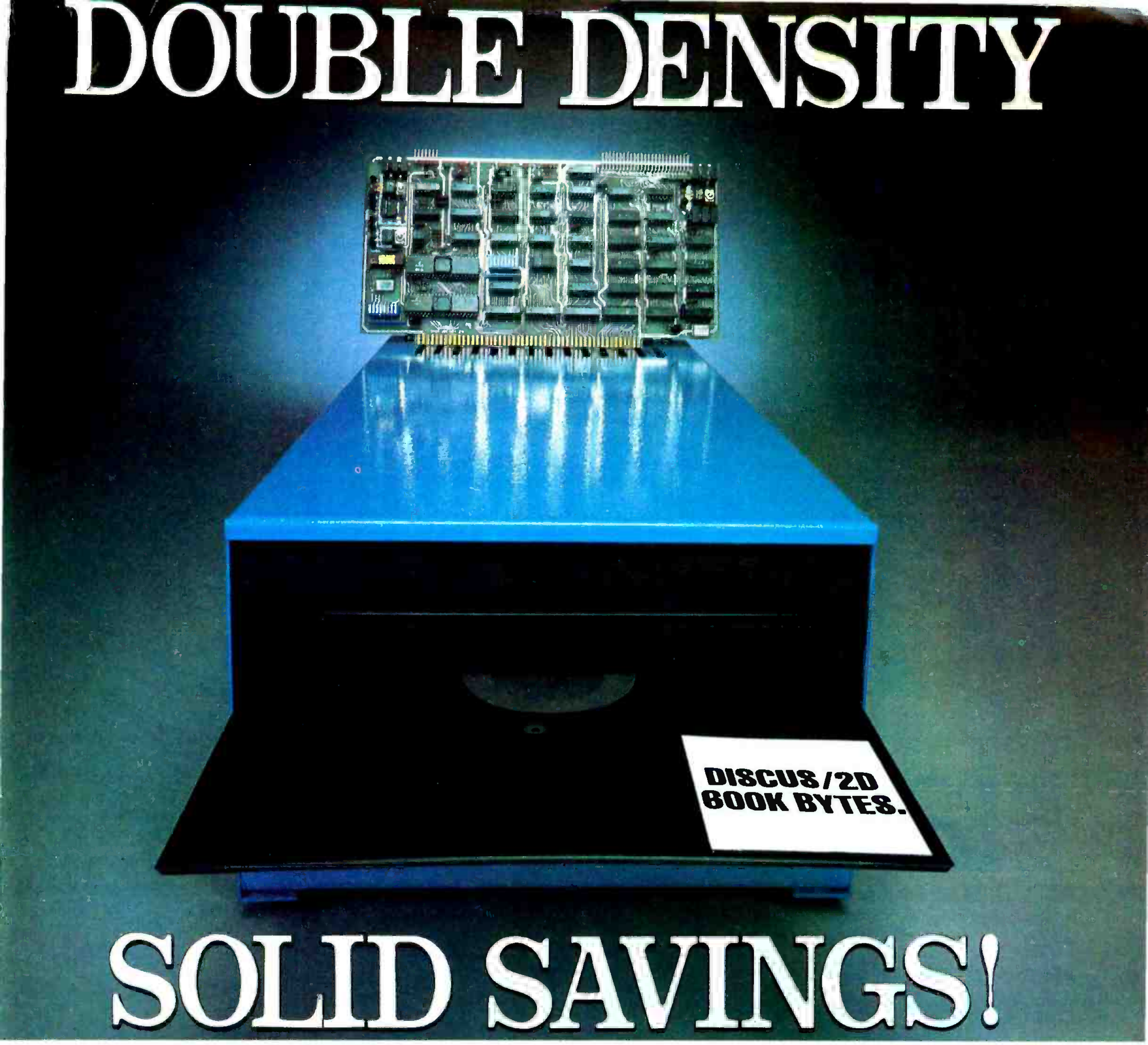
A Lively Bomb Response

The first and second place winners of the December 1978 BOMB were "Some Facts of Life" by David J Buckingham (page 54) and "Life With Your Computer" by Justin Milliun, Judy Reardon, and Peter Smart (page 45). These articles placed 2.17 and 1.21 standard deviations above the mean. First and second prizes of $100 and $50 will be sent to the authors.

Third place went to "Fast Fourier Transforms on Your Home Computer" by William D Stanley and Steven J Peterson (page 14), followed by "Chess 4.7 versus David Levy" by J R Douglas (page 84).■



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