COMMUNICATIONS QUARTERLY

THE JOURNAL OF COMMUNICATIONS TECHNOLOGY

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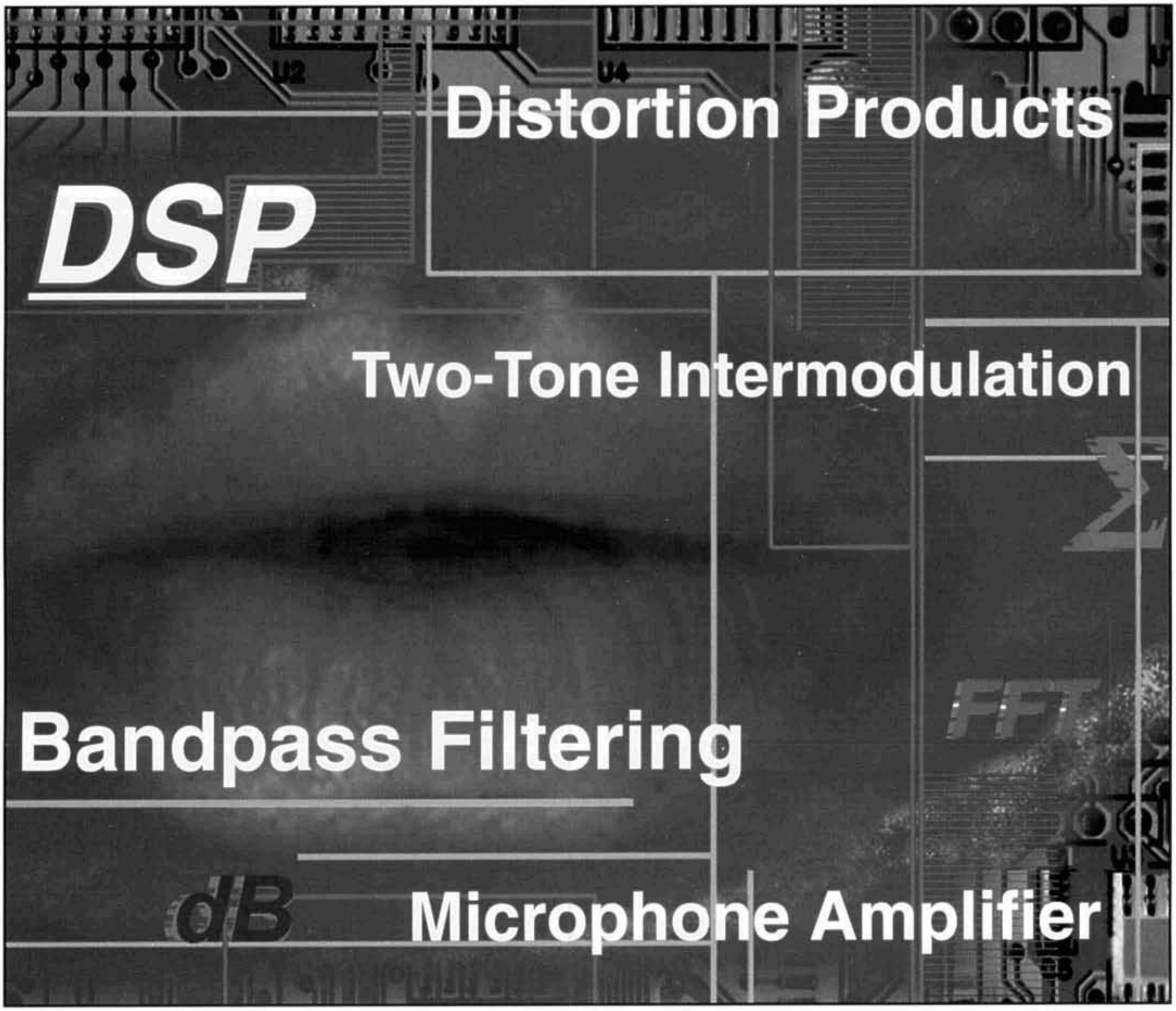

- Build a Logarithmic Audio Speech Processor for a More Effective SSB Transmitter
- Modern Receiver Design with an Eye toward DSP Techniques
- Single-chip DDS Technology Opens Complex Technique to Amateur Radio Population
- Continuous Duty Battery Charger for Any Size Lead-Acid Battery System
- Modeling and Understanding Small Beam Series—The Popular ZL Special
- Build a 5- to 850-MHz Spectrum Analyzer with Low-cost TV Tuners

ISSN 1053-9433

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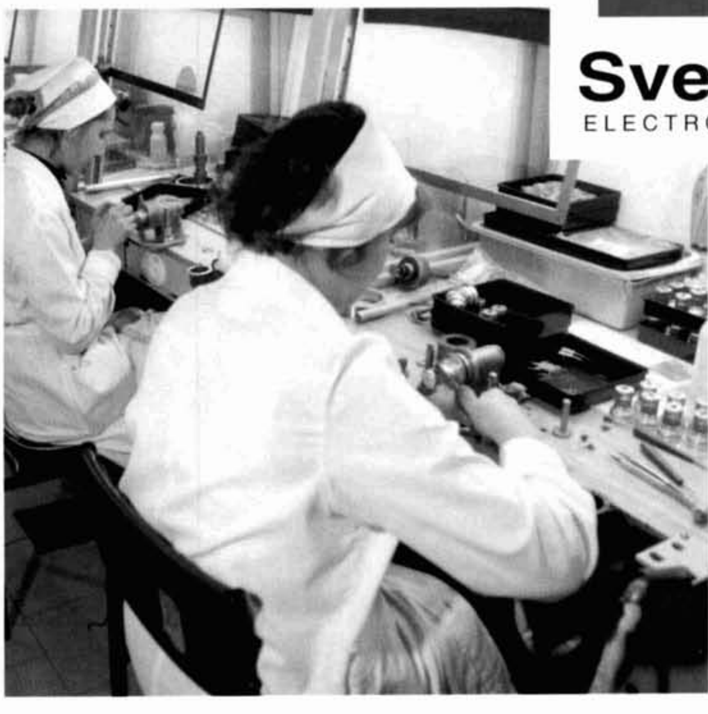

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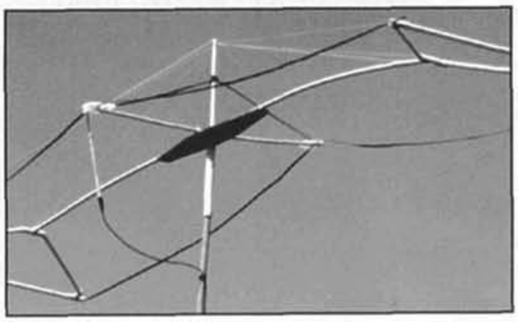

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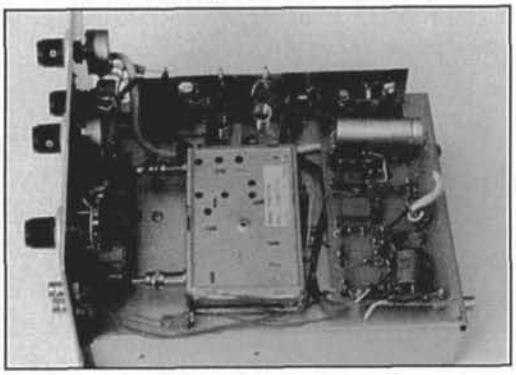

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On the Cover: A logarithmic audio speech processor can improve the effectiveness of your SSB transmitter. Bill Sabin, *WØIYH*, has developed a compromise between complexity, performance, and cost. For all the details see "A Logarithmic Audio Speech Processor," beginning on page 9.

EDITORIAL

Junk Science and Amateur Radio

Last night I watched a great show produced by ABC News, called "Junk Science: What You Know That May Not Be So," hosted by John Stossel. Of course, I sniggered a bit about the ABC News tag. It seems a lot of the news we hear today revolves around "what the news sources know that may not be so" theme.

A few tidbits from the show

Did you know there's a government agency that sends out tons of pamphlets which try to convince the public that *everyone* should severely limit or eliminate salt in their diets. By doing so, the agency contends, they can lower their incidence of heart attack *and* live longer. When Stossel confronted the head of this agency with contradictory data from nine prominent physicians from major hospitals and research centers, the gentleman refused to back down on his claims *even though he could not offer convincing proof.* It appears the *real* truth is that only those afflicted with maladies like hypertension should limit salt intake. It's just not necessary for the rest of us.

Remember cold fusion? In March 1989, at a Salt Lake City press conference, chemists B. Stanley Pons and Martin Fleischmann announced that they had achieved cold fusion—setting the scientific community on its ear. Pons and Fleischmann went on to claim that they had performed this feat at the University of Utah using a simple tabletop apparatus and just a few dollars in materials. This alleged discovery spun off two camps: skeptics, who summarily dismissed the whole idea, and enthusiasts, who continue to *attempt* to prove Pons' and Fleischmann's claims.

Even a Nobel Prize winner

Finally, there was the claim made by Nobel Prize Winner Linus Pauling. He was convinced that taking Vitamin C could prevent or cure the common cold. Unfortunately, research revealed that while Vitamin C can ease the nasal congestion and other symptoms of the common cold, it doesn't cure it. Only time can do that. So, here was a highly respected scientist, who was heavily invested in his own piece of junk science. It just goes to show that the promises of junk science can lure anyone.

Junk disciples

Like other forms of science, amateur radio has its *junk* disciples. Most often these guys are heavily invested in an experiment gone wrong (they just don't know it) concerning an antenna, a feed system, an equipment modification, etc. Anyone of us could be puttering around in our shacks, fiddling with something on the bench, and "discover" something we're sure no one has ever encountered before. That's exciting, and that's what ham radio experimentation is all about, but here's where the process goes awry.

Suppose we loose our objectivity about this discovery and begin sharing it with our ham friends—before determining whether our hypothesis is correct. We may be guilty of disseminating junk science, and, just like other types of junk science, what we know may not be so. The idea may sound good, it may look good on paper, it may even appear to work; but if it's not based on careful scientific study, we can't be sure it's really legitimate. I can think of many instances in our hobby where such ideas have gotten into mainstream via magazine, Internet newsgroups, or over the airwaves. I've been editing amateur radio magazines for 10 years, and I know I've been caught a time or two by an idea that sounded incredibly interesting and innovative, but that lost its luster in the bright light of day.

A challenge

My challenge to all of us as we start a new year is to look at our own amateur radio *science* with a more critical eye. If you read something you think may be bogus, or based on a lack of evidence, call the author (or editor) and ask for verification. When you see something on one of the amateur radio newsgroups or hear something on the air, put on your skeptic's hat and mount a challenge. If you make a discovery, document your work and try to have it peer-reviewed before you disseminate it via the amateur press, newsgroups, radio clubs, etc.

Finally, no matter what side of the fence you're on, try to handle any challenges or confrontations calmly, but with panache. Sniping and flaming does not a dialogue create. Yes, we want to debunk the junk scientists in our ranks; but it's important to do it with *style*!

Terry Littlefield, KA1STC
Editor

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Questions about the ultimate noise bridge

Dear Editor:

I have been unable to understand the "Ultimate Noise Bridge" circuit in the Summer 1996 issue. I find three problems:

1. The noise generator is built in a "floating" box to ensure equal noise currents at A' and C', yet the box is AC grounded to the outer box 1 by the 0.01 and 15 μF capacitors.
2. The receiver output RX appears to be grounded to the outer box.
3. As you know, there is no such thing as a 9-volt NiCd battery. There is the six-cell NiCd, with a plateau voltage of only 7.2 volts and the seven-cell battery with a plateau voltage of 8.4 volts. Most 9-volts are of the six-cell construction. The Varta and Saft have seven cells. Will either work in the circuit, or must you use the higher voltage, seven-cell version?

I enjoy *Communications Quarterly*. It is outstanding in this era of beginner-oriented magazines. Don't ever let anyone tell you that it is too technical. They miss the point entirely!

Ruddy Ellis, W4LNG
Atlanta, Georgia

Cosmic cousins

Dear Mr. Hyder:

This is in response to your letter to *Communications Quarterly*, dated June 14, 1996. I regret that I have been unable to respond sooner. Your letter raises some very valid points; but in addressing them, I come to different conclusions that you did.

I fully agree that the vast distances between the stars preclude two-way communications with our cosmic neighbors. But does this negate the value of simplex transmissions? All my life I have been receiving one-way communications which have enhanced my being—from Moses, Aristotle, Shakespeare, and George Bernard Shaw. Because I cannot engage them in a dialogue, is the communication any less valid?

You are absolutely right about the challenges of decoding a communication from a race with which we have nothing biologically in common. But translation and interpretation aside, the mere confirmation of the existence of other civilizations can have a profound impact on humanity. If, because we have at least all physical law in common, we do manage to interpret some of the intercepted transmissions, I would consider that a bonus. But existence of proof alone is, in my opinion, still worth the price of admission.

Some in SETI may indeed be looking for a father figure. I prefer to think more along the lines of finding a brother figure, or a distant cousin. Though I've never personally met my cousins in Europe, though we do not speak the same language, I still feel there is a bond between us. Why should it be otherwise with our cosmic cousins.

Finally, Frank Drake's speculations as to the nature of alien civilizations are just that—speculations. But about the nature of photons, we need not speculate. They are indeed the fastest spaceships known to man, and stand a far better chance of traveling between the stars than do alien visitors, be they benevolent or malevolent. Further, they are the substance of ham radio communications, and we hams are in a unique position to exploit them for the good of all humanity.

Paul Shuch, Ph.D., N6TX
Executive Director
The SETI League, Inc.

Triode/tetrode efficiency comparison

Dear Editor:

Thanks to W6MTF for calling my attention to an oversight in my article "4CX400A Russian Tubes for the MLA-2500 Amplifier" (*Communications Quarterly*, Summer 1996). **Table 1** is an apples-to-oranges comparison of the performance of the 4CX400A tetrode to the 8875 triode. As W6TMF points out, the Eimac 8875 data presented in my article was taken at 432 MHz. As he states, transit-time effects at 432 MHz will reduce efficiency, so the comparison is unfair.

When comparing Svetlana 4CX400A published data to the correct Eimac HF data, the Svetlana tube still has higher efficiency than the Eimac tube because of the unique Russian secondary emission inhibiting geometry in the 4CX400A; however, the difference is less dramatic than shown in the article.

My thanks to W6TMF for finding the oversight and to *Communications Quarterly* for the opportunity to set the record straight.

Bob Alper, W4OIW/6
Product Manager
Svetlana Electron Devices
Portola Valley, California

Thumbs up for Caddock Electronics' Kool-Tab MP850 resistors

Dear Rick,

I was intrigued by your "Quarterly Devices" column of Summer 1995, page 73, because the users of Svetlana tetrodes wish to use the passive input circuit which you covered in your "Quarterly Devices" column of Summer 1993, page 90. Since you published that article, the passive input circuit for tetrode circuits has become quite popular because it substantially reduces the component count in linear amplifiers. It has also proved to be rock stable and neutralization is not required.

A problem for the builder is the supply of 50-watt, 50-ohm resistors. That is why your article on power-film resistors was so interesting. The Caddock Electronics line of tab-mount devices (Kool-Tab MP850) power-film resistors neatly fill the need for compact, low-inductance and high-power resistors for passive grid input circuits for full-power amateur radio linear amplifiers.

George Badger, W6TC
President
Svetlana Electron Devices
Portola Valley, California

A few corrections

Dear Editor:

I must have failed to send you the latest draft of the letter about the 4CX400 article. Please be aware of several errors I made.

On line on page 4 right column.

"A look at Eimac's published data shows the 8877 <u>anode</u> voltage used in **Table 1** is actually the absolute maximum allowable operating voltage, <u>2200</u>, volts."

(That was a copy error. Note that it was correct in my text.)

The following were my sole responsibility. Regretfully, I understood the early draft was wrong and failed to correct it.

Page 5. The grid resistance formulas should be

$$Rg = \frac{Eb^2}{2Pd}$$

where Eb is the <u>total</u> dc grid bias and also

$$Rg = \frac{Eg}{Ipk}$$

The correct grid L-pad series input resistance is about 18 Ohms, and the grid's parallel resistance about 32 Ohms, for 100 watts of drive and -35 volts bias with no feedback or loss. In a practical circuit these values would have to be adjusted slightly.

Thanks,

Tom Rauch, W8JI
Conyers, Georgia

Reader takes exception

Dear Editor:

In reference to W4OIW's article concerning the 4CX400A, W8JI's letter in the Fall 1996 issue makes some valid points relative to specifications and operating conditions. I must take exception to W8JI's statements concerning the screen supply and control grid circuitry.

Shunt regulators thrive on high impedance sources and in fact prefer a current source. The 10k resistor in series with Q1 has almost no effect on the regulation as long as Q1 remains out of saturation. It does greatly reduce the dissipation in Q1's collector. The impedance seen by the screens is very low due to the shunt negative feedback around Q1. Negative screen current in excess of a few milliamps could cause failure of the Zener string feeding the base of Q1 with the failure a short time later of the 100-Ohm resistor in Q1's emitter. At that point control of the screen voltage would be lost. My preference for screen voltage regulation would be two 200V, 50W Zeners in series from screen to ground. The 2500-Ohm rheostat in series with the source along with the tripler's poor regulation should keep the screen dissipation within reason.

I'm not sure where Mr. Rauch was going with his math. An AB1 amplifier needs only a peak driving voltage equal to the grid bias. Therefore with 35V bias a single tone sine wave of about 24V would be necessary. 24V across 50 Ohms requires about 11.5W. A simple divider takes care of higher powers. The divider should have a total resistance of 50 Ohms and a tap located such that 35V peak appears at the grid.

While I would have done some things differently, I found Mr. Alper's article both interesting and thought provoking.

Gerald S. Bower, AB6BO
Templeton, California

W4OIW/6 replies

Dear Mr. Bower:

Thank you for a copy of your 18 December 1996 letter to the Editor of *Communications Quarterly*. Your courtesy to copy Mr. Tom Rauch, as well as myself, is sincerely appreciated.

Enclosed is a copy of my letter response of 25 November 1996 to Mr. Rauch and a copy of his 1 December, 1996, comments to me. It is somewhat apparent, at least to me, that he did not read with an open mind or possibly did not wish to understand my letter to him. This conclusion was drawn in conjunction with his analysis of the screen grid regulator and drive requirements, and repetition of questions that were answered in my letter of 25 November. The denigrating of "on-the-air" testing was not completely justified. While certainly not as controlled as laboratory tests, "on-the-air" testing is a valuable addition to static tests because, as Mr. Rauch indicated, syllabic laboratory testing is anything but standardized.

Thank you again for the copy of your letter and for taking the interest and the time to write *Communications Quarterly*. Terry Littlefield, KA1STC, Editor of *Communications Quarterly*, advised me on 26 December her plans to publish correspondence on this subject in the Spring 1997 issue.

B.-N. "Bob" Alper, W4OIW/6
Portola Valley, California

"The Monster Antennas"—A huge hit

Bill Byron, W7DHD, sent along copies of these letters he received after his article "The Monster Antennas" appeared in our Spring 1996 issue. Congratulations for an FB job, Bill!

Dear OM:

Just a short note to express my admiration for your truly excellent article "The Monster Antennas" in the spring 1996 issue of *Communications Quarterly*.

Your article was beautifully researched, written, and illustrated—a rarity in this days of inarticulate engineers!

Archibald C. Doty, K8CFU, Director
Radio Club of America, Inc.
Fletcher, North Carolina

Dear Bill:

Thanks for sending the copy of *Communications Quarterly* with your paper on "The Monster Antennas." I thought it came out very well and is an article you can be proud to have authored. I don't know of anyone else who could have done so well in dealing with the topic. You seem to have found your second calling in writing about history of communication technology. Have you selected your next topic yet?

Dr. James Brittain, Professor Emeritus
History of Technology Department
Georgia Tech
Hendersonville, North Carolina

Dear Mr. Byron:

My word, what an outstanding article you wrote for *Communications Quarterly*. I thoroughly enjoyed it. It was fantastic reading and I didn't want it to end. Please accept my sincere thank you for all the painstaking effort that you went through to write it. Is there any possibility you'll be writing more about "The Monster Antennas?" I hope so.

Dick Weber, K5IU
Prosper, Texas

Dear Mr. Byron:

As one of the four RCA engineers who were continuously involved with the Jim Creek station from the proposal stage to the final factory acceptance tests, I certainly enjoyed reading your article in the spring 1996 issue of *Communications Quarterly*.

The personnel involved were John C. Watler, project leader and system design; John W. Sanborn, power and control; Charles D. Mulford, mechanical engineer; and myself, general RF design. Antenna design was subcontracted to J.L. Finch at RCA Communications. At the completion of the factory phase of this project, I left RCA to move to California in August 1950. As a consequence, I lost all touch with VLF design and moved into other programs.

While I was still living in New Jersey, I visited the alternator station at Tuckerton, New Jersey, which was quite an experience. In later years, I attended an IRE symposium on long haul communication at Honolulu about 1958 and visited the station at Lualualei, Oahu, which was built by GE in the 30s. It was not in service at the time.

Your excellent review of the various antennas for VLF certainly was interesting to read and revived some fond memories of people that I worked with in years past and, for that, I thank you.

O.B. Dutton, KM6PJ
Ventura, California

Dear Bill:

I greatly enjoyed your Monster Antenna article in the spring 1996 *Communications Quarterly*. I have always been interested in this subject. I do remember the Radio Central Antennas on Long Island, which we passed many times during the 1930s.

I have never seen any of the OMEGA antennas pictured. OMEGA operated near 12 kHz. One in Norway was described. It was on an island in the middle of a fjord. The flat top was suspended between mountains on each side of the fjord. Many long cables were laid into the fjord to get good contact with the sea water. OMEGA and LORAN C will be shut down within a few years because GPS has made all other forms of electronic navigation obsolete.

The Motorola engineering library had a copy of *VLF Engineering* (at my request) and I enjoyed reading it.

Harry Hyder, W7IV
Tempe, Arizona

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SL-11R	•	•	7	11	2 5/8 × 7 × 9 3/4	12
SL-11R-MC		•	7	11	5 3/4 × 7 1/4 × 9 3/4	13
SL-11R-GE	•		7	11	5 3/4 × 7 × 9 3/4	13
SL-11R-RA		•	7	11	4 3/4 × 7 × 9 3/4	13
SL-11R-EFJ		•	7	11	5 1/8 × 7 1/4 × 9 3/4	13
SL-11MG		•	7	11	5 1/8 × 7 1/18 × 9 3/4	13
SL-15R	•	•	12	15	2 5/8 × 7 × 9 3/4	13
SL-15R-GE	•		12	15	5 1/8 × 7 5/8 × 9 3/4	14
SL-15R-RA		•	12	15	4 3/4 × 7 1/4 × 9 3/4	14
SL-15R-EFJ		•	12	15	5 1/8 × 7 1/18 × 9 3/4	14

RS-L SERIES

• POWER SUPPLIES WITH BUILT IN CIGARETTE LIGHTER RECEPTACLE

MODEL		Continuous Duty [Amps]	ICS* [Amps]	Size [IN] H × W × D	Shipping Wt. [lbs]
RS-4L	•	3	4	3 1/2 × 6 1/8 × 7 1/4	6
RS-5L	•	4	5	3 1/2 × 6 1/8 × 7 1/4	7

RM SERIES

MODEL RM-35M

• 19" RACK MOUNT POWER SUPPLIES

MODEL	Continuous Duty [Amps]	ICS* [Amps]	Size [IN] H × W × D	Shipping Wt. [lbs]
RM-12A	9	12	5 1/4 × 19 × 8 1/4	16
RM-35A	25	35	5 1/4 × 19 × 12 1/2	38
RM-50A	37	50	5 1/4 × 19 × 12 1/2	50
RM-60A	50	55	7 × 19 × 12 1/2	60
• Separate Volt and Amp Meters				
RM-12M	9	12	5 1/4 × 19 × 8 1/4	16
RM-35M	25	35	5 1/4 × 19 × 12 1/2	38
RM-50M	37	50	5 1/4 × 19 × 12 1/2	50
RM-60M	50	55	7 × 19 × 12 1/2	60

RS-A SERIES

MODEL RS-7A

MODEL	Colors Gray	Colors Black	Continuous Duty [Amps]	ICS* [Amps]	Size [IN] H × W × D	Shipping Wt. [lbs]
RS-3A		•	2.5	3	3 × 4 3/4 × 5 3/4	4
RS-4A	•	•	3	4	3 3/4 × 6 1/2 × 9	5
RS-5A		•	4	5	3 1/2 × 6 1/8 × 7 1/4	7
RS-7A	•	•	5	7	3 3/4 × 6 1/2 × 9	9
RS-10A	•	•	7.5	10	4 × 7 1/2 × 10 3/4	11
RS-12A	•	•	9	12	4 1/2 × 8 × 9	13
RS-12B		•	9	12	4 × 7 1/2 × 10 3/4	13
RS-20A	•	•	16	20	5 × 9 × 10 1/2	18
RS-35A	•	•	25	35	5 × 11 × 11	27
RS-50A	•		37	50	6 × 13 3/4 × 11	46
RS-70A	•		57	70	6 × 13 3/4 × 12 1/8	48

RS-M SERIES

MODEL RS-35M

MODEL	Continuous Duty [Amps]	ICS* [Amps]	Size [IN] H × W × D	Shipping Wt. [lbs]
• Switchable volt and Amp meter				
RS-12M	9	12	4 1/2 × 8 × 9	13
• Separate volt and Amp meters				
RS-20M	16	20	5 × 9 × 10 1/2	18
RS-35M	25	35	5 × 11 × 11	27
RS-50M	37	50	6 × 13 3/4 × 1	46
RS-70M	57	70	6 × 13 3/4 × 12 1/8	48

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MODEL VS-35M

• Separate Volt and Amp Meters • Output Voltage adjustable from 2-15 volts • Current limit adjustable from 1.5 amps to Full Load

MODEL	Continuous Duty [Amps] @13.8VDC	@10VDC	@5VDC	ICS* [Amps] @13.8V	Size [IN] H × W × D	Shipping Wt. [lbs]
VS-12M	9	5	2	12	4 1/2 × 8 × 9	13
VS-20M	16	9	4	20	5 × 9 × 10 1/2	20
VS-35M	25	15	7	35	5 × 11 × 11	29
VS-50M	37	22	10	50	6 × 13 3/4 × 11	46
VS-70M	57	34	16	70	6 × 13 3/4 × 12 1/2	48
• Variable rack mount power supplies						
VRM-35M	25	15	7	35	5 1/4 × 19 × 12 1/2	38
VRM-50M	37	22	10	50	5 1/4 × 19 × 12 1/2	50

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William E. Sabin, *WØIYH*
1400 Harold Drive, S.E.
Cedar Rapids, Iowa 52403
e-mail: <sabinw@crpl.cedar-rapids.lib.ia.us>

A LOGARITHMIC AUDIO SPEECH PROCESSOR

Improve the effectiveness of your SSB transmitter

The communications effectiveness of an SSB transmitter may be improved significantly if the weaker components of speech can be emphasized relative to those that are stronger. Normal speech has more than a 20-dB dynamic,[1] which isn't good from a weak-signal communications standpoint. Most SSB transmitters are capable of delivering a higher *average* power level for a given maximum PEP rating.

IF clipping provides one good method of speech processing, but it involves modifying the internal signal path circuitry of the SSB exciter. This can be difficult and tricky, often to the point of not being worthwhile. Other methods use audio processing, which can be performed in an external unit ahead of the microphone input. Audio *compressors* with fast attack (2 or 3 milliseconds) and long decay time (1 or 2 seconds) don't offer enough improvement in weak component enhancement. Audio speech *clipping* with very fast attack and recovery time (without memory) works somewhat better, but has a tendency to produce a

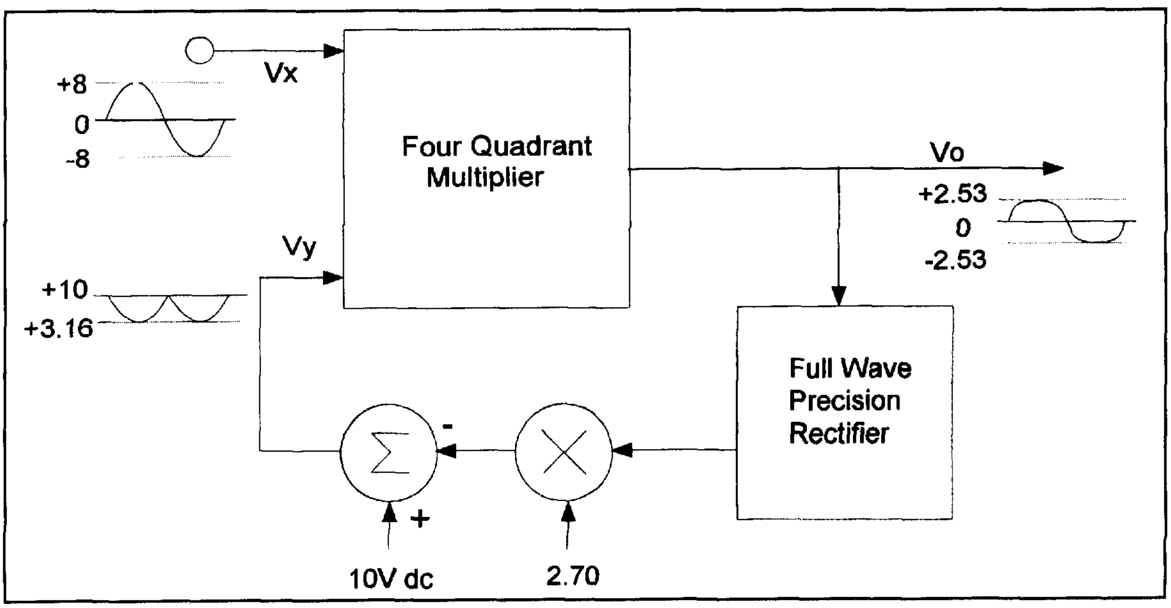

Figure 1. Block diagram.

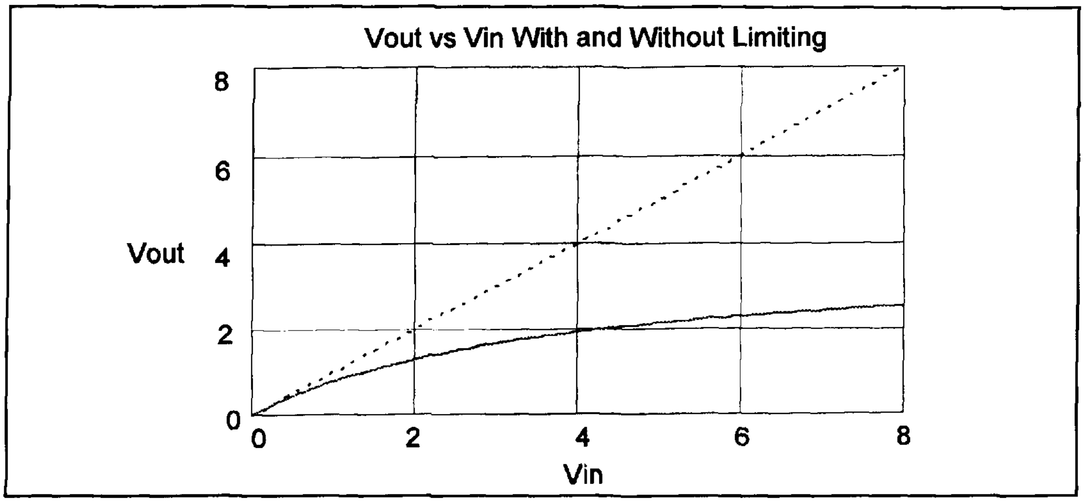

Figure 2. Plot of v_o versus v_x.

considerable amount of harmonic distortion. This is unpleasant to listen to and tends to detract from the improvement. Another approach is to translate the audio to IF, clip, and translate back to audio, then into the mic jack. This is a good method and has been used a lot because it produces less harmonic distortion than audio clipping.

Some audio processors combine compression and clipping. The compressor compensates for variations in the speaker's voice level and presents a more constant level into the clipper circuit. Unfortunately, the *total* audio amplification may become so large that during speech pauses, background noise and breath sounds are highly exaggerated. Matched amplitude *compandor* pairs at the transmitting and receiving ends are used commercially to restore the speaker's original voice range at the receive end. Lincompex is another commercial system that does this.

Some amateurs use other advanced and complicated methods, such as the "split-band" and those that employ DSP. I felt that a simpler and less expensive approach would be very desirable for my purposes.

I'll describe a simple "soft limiting" method that's quite effective. It produces less distortion

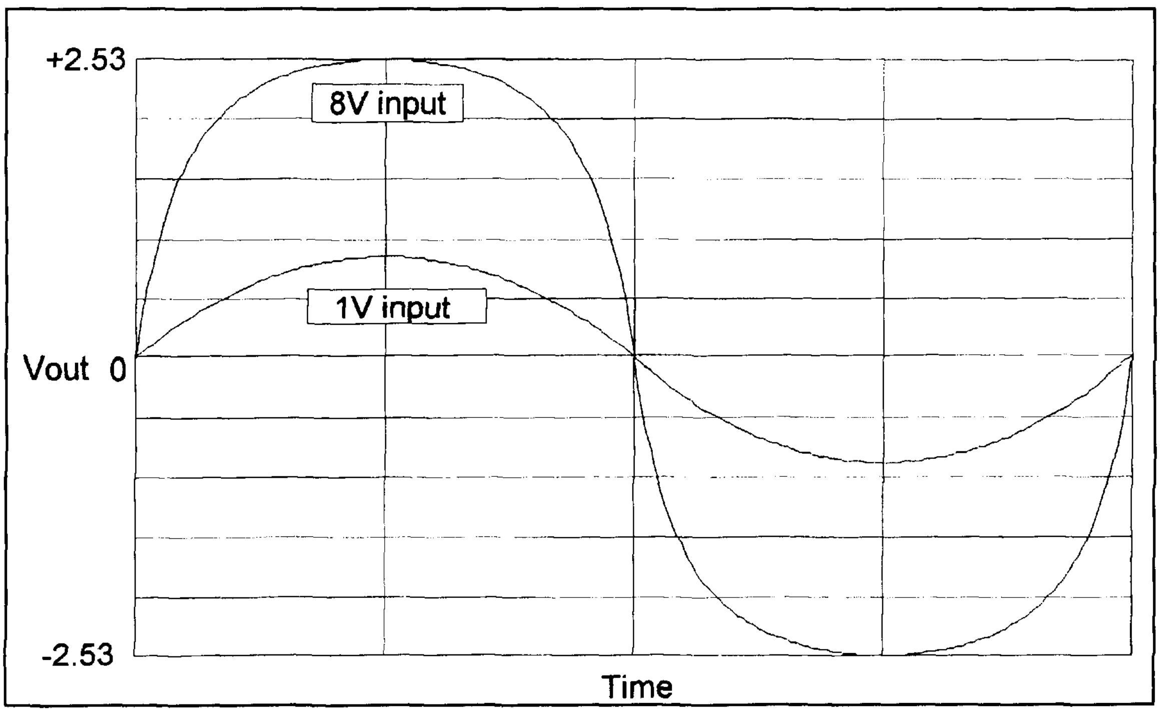

Figure 3. Response of the multiplier to a small sine-wave signal and a maximum-level signal.

than audio clipping and is more pleasing to the listener. A roughly similar approach was described in the amateur literature by Schleicher (a telephone company engineer) a long time ago.[2] We'll adapt that approach to modern precision ICs. I haven't added compression ahead of the limiter, but have used a simple and effective method of monitoring speech level. The main exercise is to create a "system design" and tie the ICs together to obtain the desired response. The result is a *compromise* between complexity, performance, and cost that may be attractive to many experimenters (I found it so).

Soft-limiting

The block diagram of **Figure 1** shows the basic principles used in the soft-limiter. The multiplier is an Analog Devices AD633JN high-precision, low-cost four quadrant multiplier chip. The relationship for this multiplier is:

$$v_o = \frac{vx \bullet vy}{10} \tag{1}$$

The signal input is v_x and, if v_y=10 volts DC, the gain from v_x to v_o is 1.0. If v_y is reduced to 3.16 volts, the gain is reduced to 0.316. Assume that v_x is a positive-going voltage. Then in **Figure 1**, v_o is also positive-going and is multiplied by 2.70, subtracted from 10.0 volts, and then applied to the *y* terminal. If we place this value of v_y in **Equation 1**, we get:

$$v_o = \frac{v_x \bullet (10 - 2.70\, v_o)}{10} \tag{2}$$

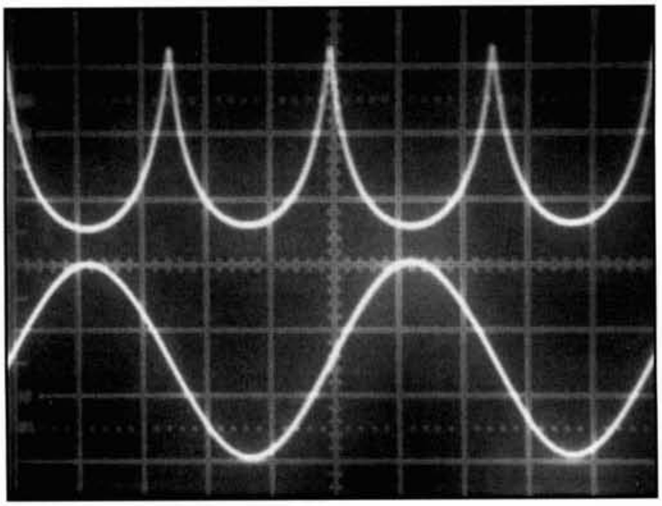

Photo A. Oscilloscope waveforms.

When we solve this for v_o we get:

$$v_o = \frac{v_x}{1 + 0.270\, v_x} \tag{3}$$

Figure 2 plots v_o versus v_x for both the case with and without feedback. We see that for an 8-volt input to v_x, v_o is reduced from 8 to 2.53 volts, a gain reduction of 10 dB. In other words, there is 10 dB of amplitude limiting. A plot of gain in dB versus v_x is approximately linear, so I call this a "logarithmic" processor; although this isn't *exactly* correct, it is within 0.5 dB.

A problem arises if v_x is a negative-polarity input. This would cause v_o in **Equation 3** to

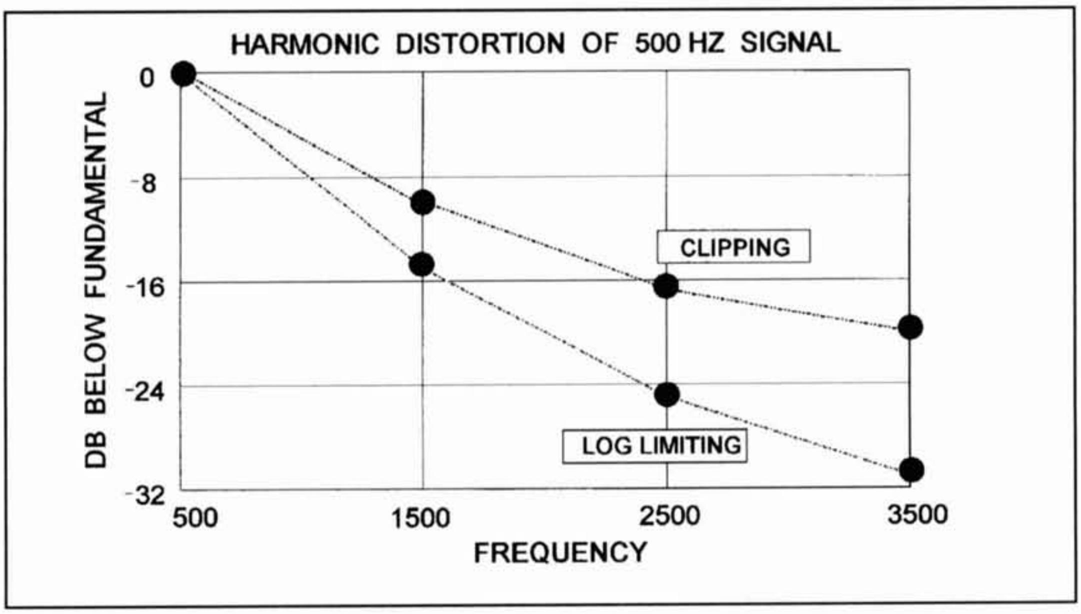

Figure 4. Harmonic distortion as a function of amplitude for a 500-Hz tone.

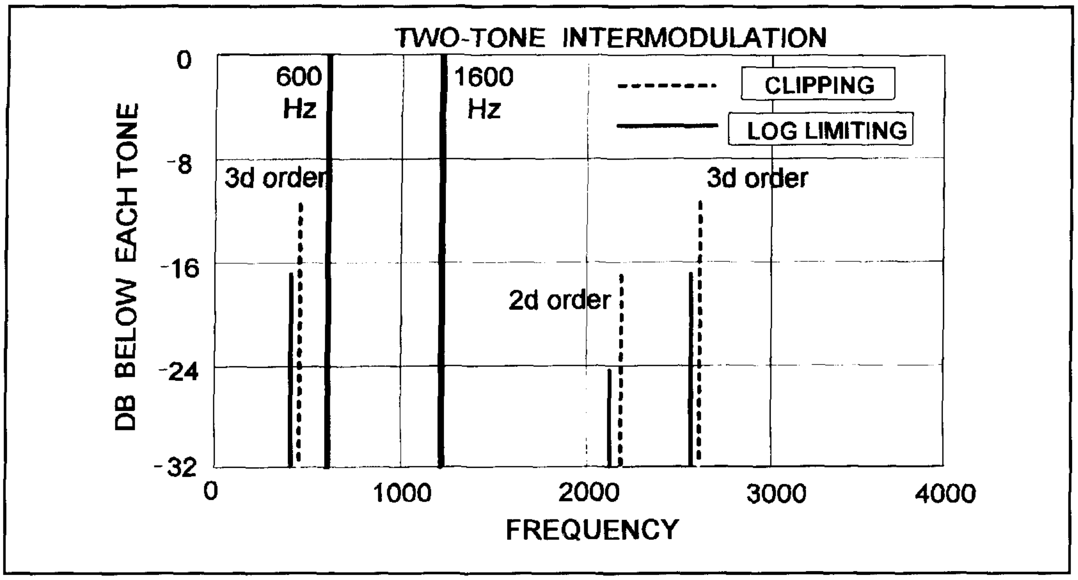

Figure 5. Comparison of second and third-order two-tone IMD products for tones at 600 and 1600 Hz.

increase. To fix this, **Equation 3** is modified as shown in **Equation 4**:

$$v_o = \frac{v_x}{1 \pm 0.270\, v_x} \tag{4}$$

The plus sign is used for positive v_x and the minus sign for negative v_x. We accomplish this in circuitry by full-wave rectifying v_o within the feedback loop, using op-amp precision rectifiers.

Using this method, the computer simulation of **Figure 3** shows the response of the multiplier to a small sinewave signal and a maximum-level signal. As the small signal gets larger, its appearance approaches that of the large signal. This rounding at high levels should be compared to the sharp corners in a hard-clipped or "sliced" signal processor. The actual circuit waveforms look exactly like these.

This rounded waveform has a special advantage in an SSB system. An audio waveform with sharp corners produces unwanted *peaks* in the output of an SSB modulator. This phenomenon is due to a mathematical principle called the Hilbert Transform effect. These peaks, unless restrained by ALC, can cause splatter in the PA. The restraint caused by the ALC, in turn, reduces the "talk power." The problem is reduced considerably by the AF and IF filters in the SSB transmitter, but a 1 or possibly 2 dB reduction of talk power is still possible. Smoothing the corners in the manner shown here helps reduce this problem. Note that this shape is independent of frequency: the waves at 250 and 3500 Hz have the same appearance.

A brief word of explanation about the Hilbert

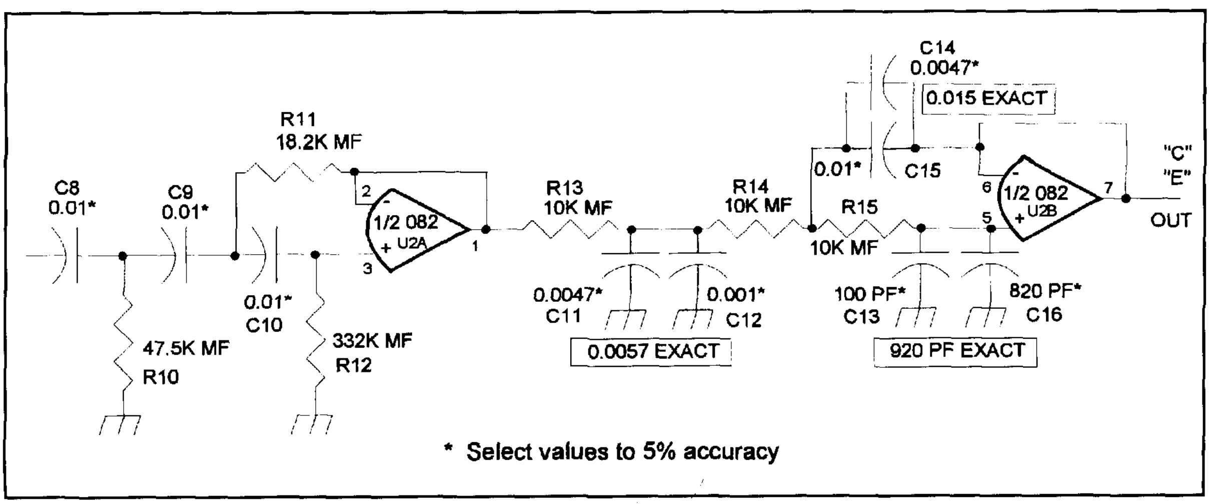

Figure 6. Bandpass filter schematic.

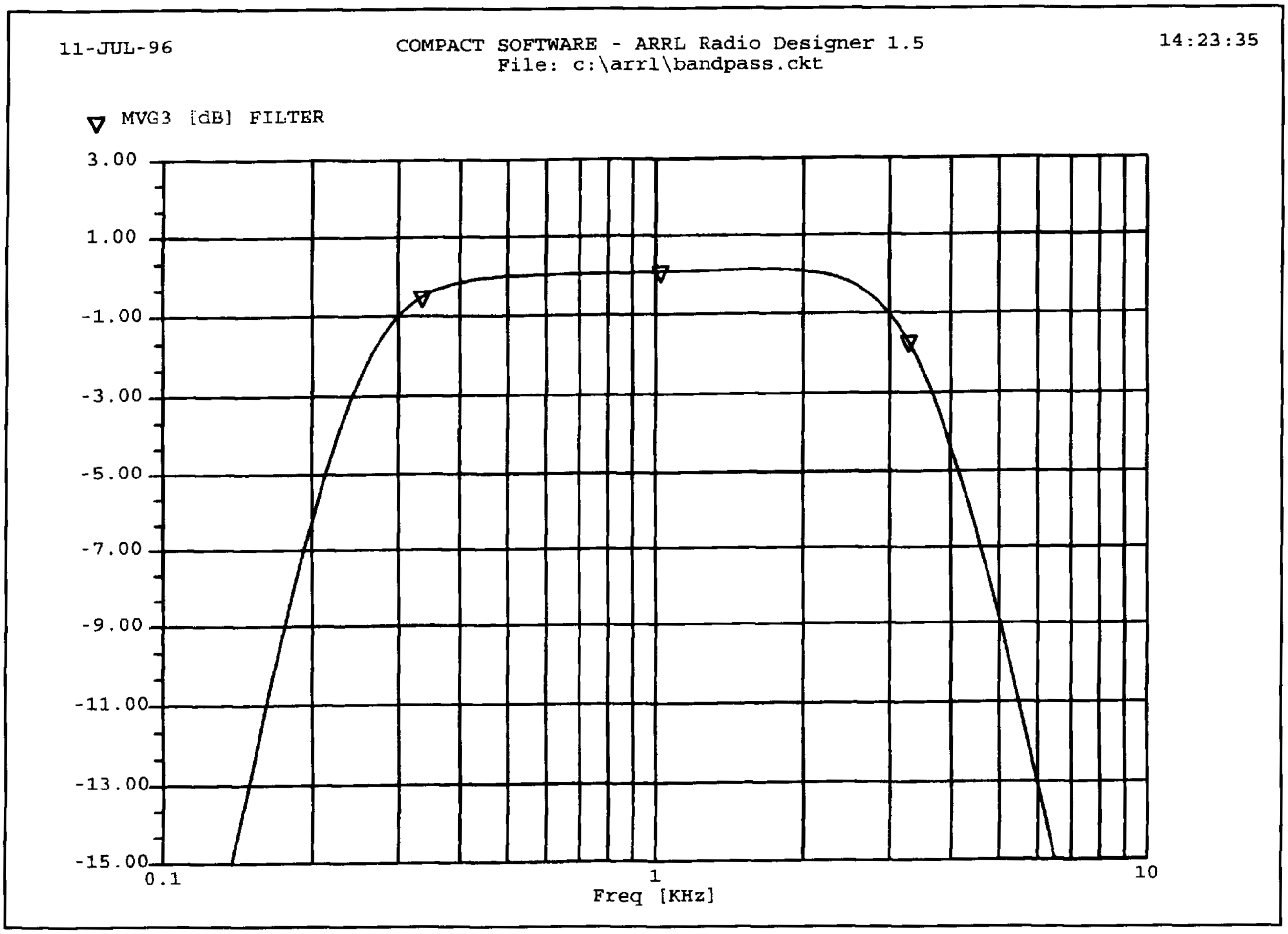

Figure 7. Bandpass filter frequency response.

transformation. It causes each frequency component in a signal waveform to be retarded 90 degrees. This produces a distortion of the waveform and, if the original wave is square, the peaks become very large. This isn't the same thing as nonlinear distortion, as no new frequencies are introduced. The Hilbert transformer is a linear circuit.

Photo A is a dual trace (chopped mode) wideband oscilloscope picture of v_x and v_y for a large

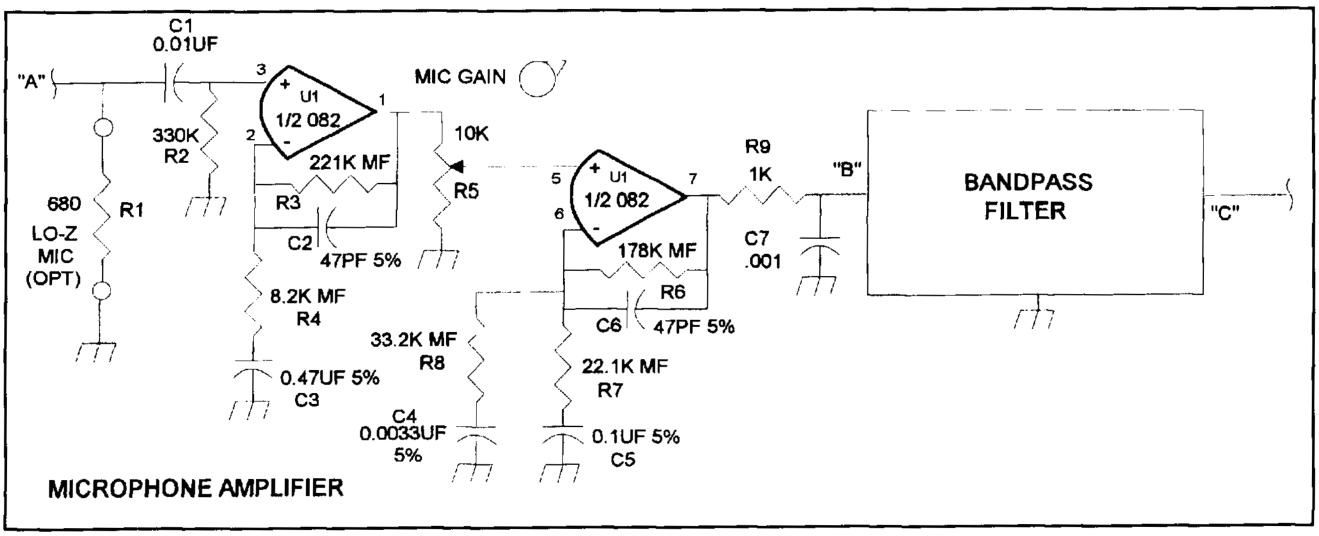

Figure 8. Op-amp microphone amplifier.

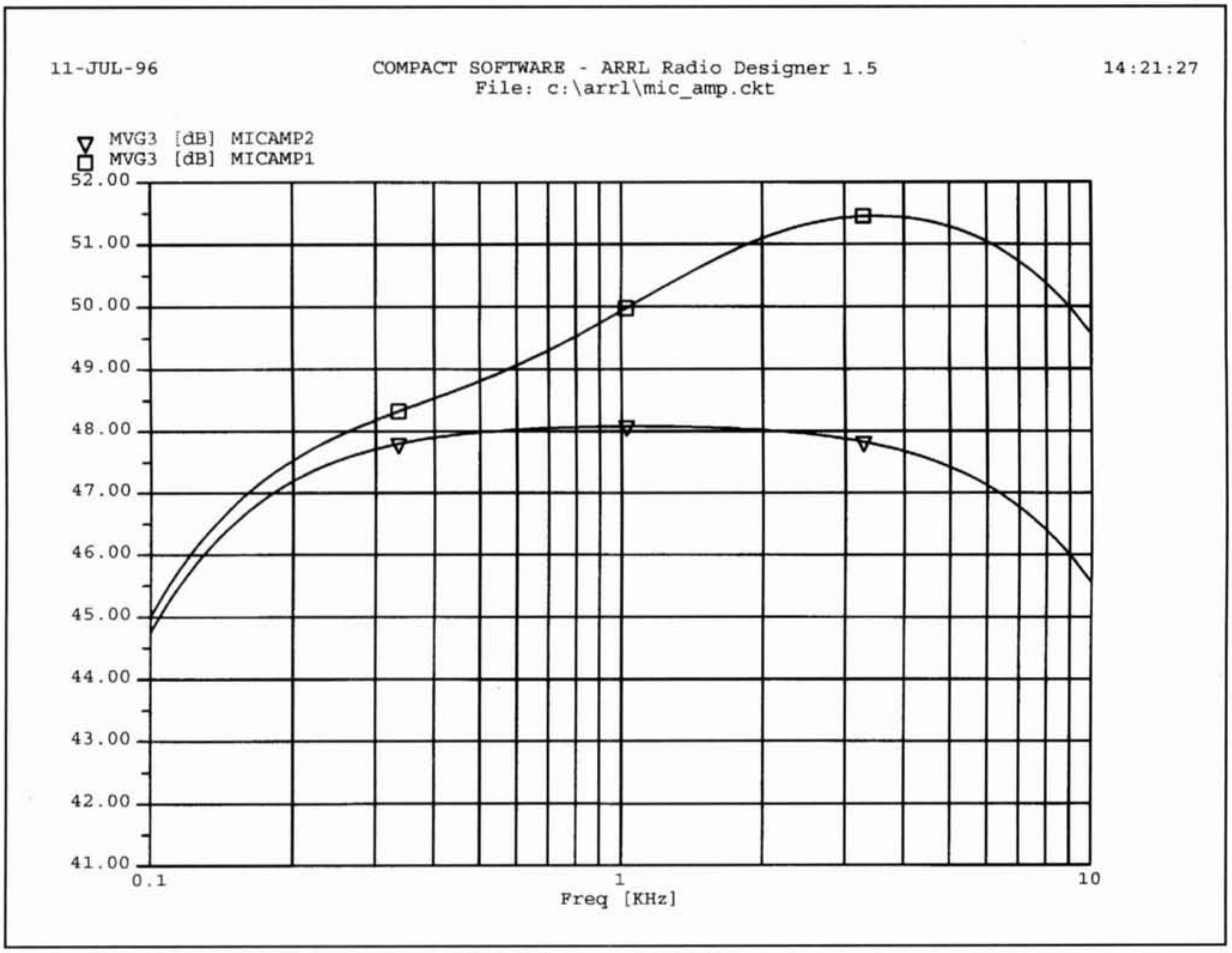

Figure 9. Microphone amplifier frequency response with and without pre-emphasis.

Photo B. Front panel.

v_x. Note that v_x and v_y are in very close phase and that v_y has very sharp corners at the 10-volt level. These things are important and require a wide bandwidth in the multiplier *and* in the feedback loop of **Figure 1**. The circuitry used is more than adequate for speech frequencies.

Distortion products

The other main attraction of the soft-limiting approach is that harmonic and intermodulation products are lower than in the audio frequency hard limiter/clipper type circuitry often used. **Figure 4** plots harmonic distortion as measured in both cases as a function of amplitude for a 500-Hz tone. For the hard limiter case, the circuitry was temporarily modified (using two reversed diodes) to perform this type of processing. Because of waveform symmetry, the even harmonics are very small and only the odd harmonics are shown. Note the difference in the way the higher harmonics fall off.

Figure 5 compares second-order and third-

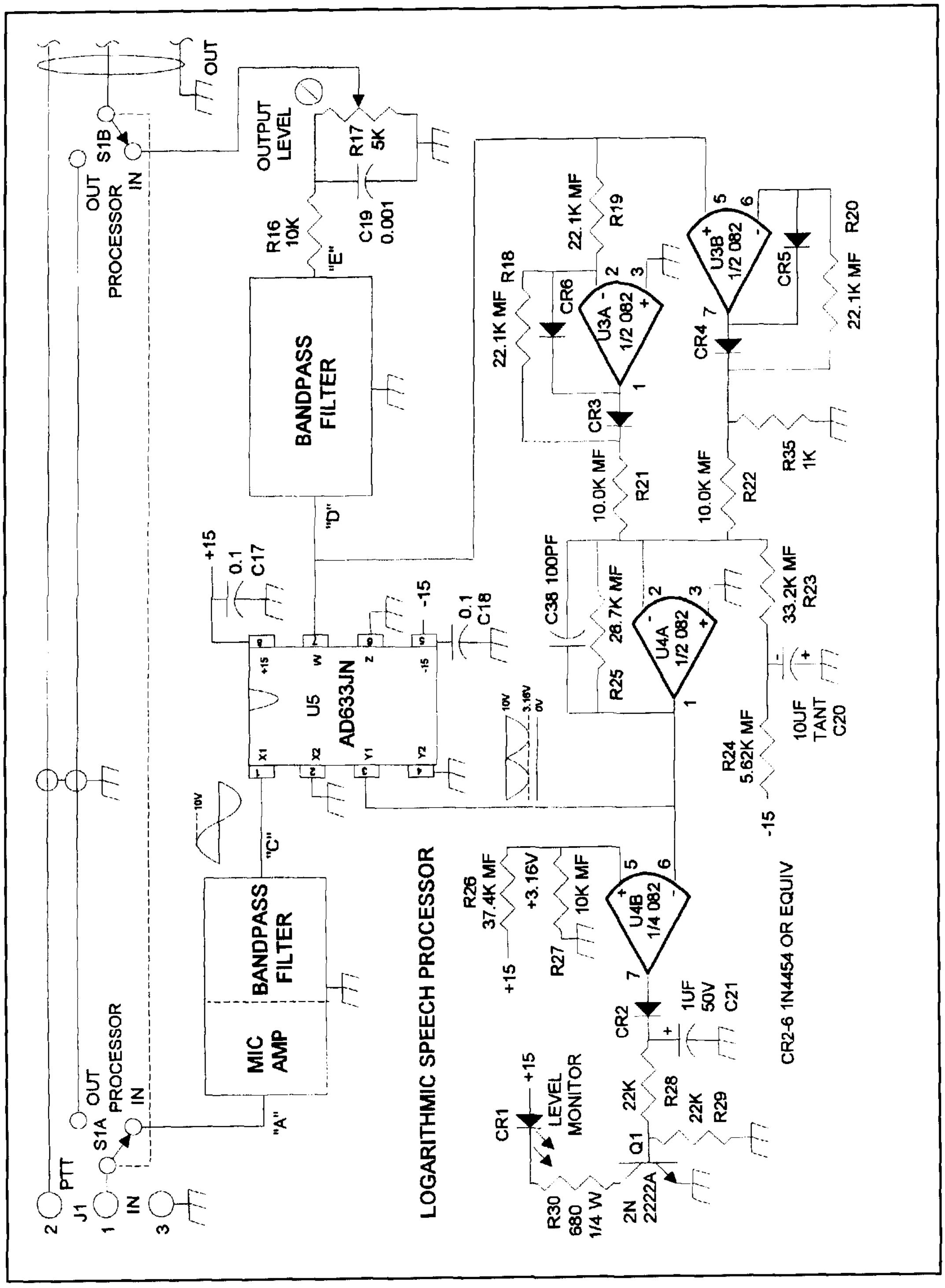

Figure 10. Overall schematic and the peak level detector.

order two-tone intermodulation products for tones at 600 and 1600 Hz. The peak instantaneous value of the two-tone signal is 8 volts into the x input of the multiplier. The soft-limiter approach is better, especially at higher amplitudes. Two-tone intermod tests are important because frequently, and for brief periods, the voice signal resembles a two-tone signal. I used an HP302A Wave Analyzer in my home lab to obtain this data.

Bandpass filtering

There are two identical bandpass filters, one ahead of and one after the limiter. The schemat-

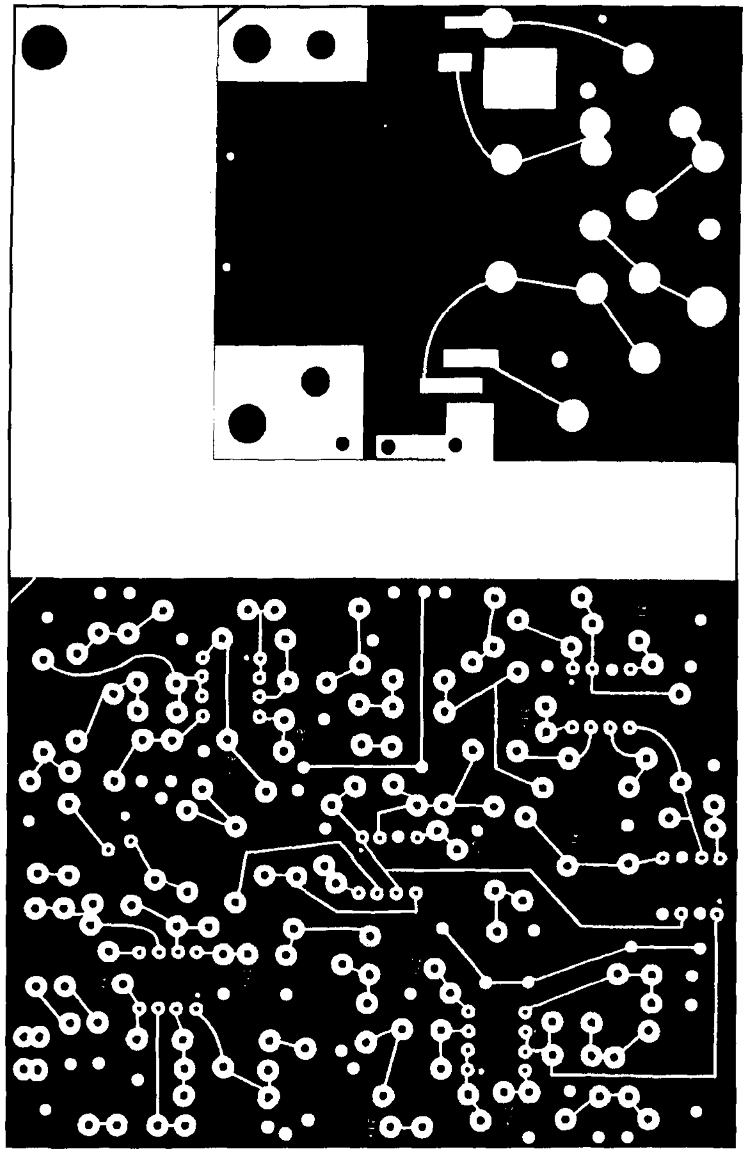

Figure 11. Masks for processor and power supply boards (trace side).

ic for these is shown in **Figure 6**. A third-order highpass and third-order lowpass, each with the Butterworth response, are used and the frequency response of each filter is shown in **Figure 7**. The filter *ahead* of the limiter decreases limiter-produced distortion products by reducing speech components below 250 Hz and above 3500 Hz. The filter *after* the limiter reduces high and low-frequency distortion products generated by the limiter. This latter selectivity augments, to some extent, the SSB filter in the transmitter—especially in its transition band region. It also helps to improve the Hilbert problem mentioned previously.

There is an effect, called the "repeaking effect," that's produced by the output filter. When a flattened waveform from the limiter is filtered, the peak value of the filtered waveform is slightly greater than the peak value of the input waveform. This is predicted by the Fourier series analysis of the input waveform and is actually observed. The result is that the overall limiting is about 9, and not 10, dB.

The schematic suggests 1 percent metal film resistors; capacitor values or combinations of values are within 5 percent of the exact values shown (see the **Parts List**). It's advisable to follow these suggestions, so the cascade of two filters will have a good overall response. The capacitors may be hand-picked CK05 ceramic types for processor units used at normal room temperatures; there's no need to buy large, expensive capacitors. The types described as X7R have better temperature stability and are preferred. A good digital C meter is one of my most important pieces of lab gear for experimental work.

Microphone amplifier

Figure 8 is the op-amp microphone amplifier. My microphone, an Electro-Voice 607 (noise canceling), is a high-impedance type that delivers about 100 mV peak instantaneously on strong voice peaks, as seen on a scope. To obtain 8-volt peaks with the mic gain pot at 1/2, a voltage gain of 160 is needed. The op amps use a +/-15 volt supply and deliver +/-8 volts peak output easily. In the schematic, R8 and C4 provide about 3 dB of high frequency pre-emphasis, which has been found to be desirable.[1]

The frequency response of the mic amp with and without this pre-emphasis is shown in **Figure 9**. It helps to emphasize the weaker high frequency components and augments the speech processing. If more or less mic gain is desired, change R2. Follow the same guidelines for resistor and capacitor values as described for the bandpass filters. The microphone itself should be of high quality and have a flat voice-frequency response (with no peaks or troughs).

The system

Figure 10 shows the overall schematic and the peak level detector. U4B compares v_y with

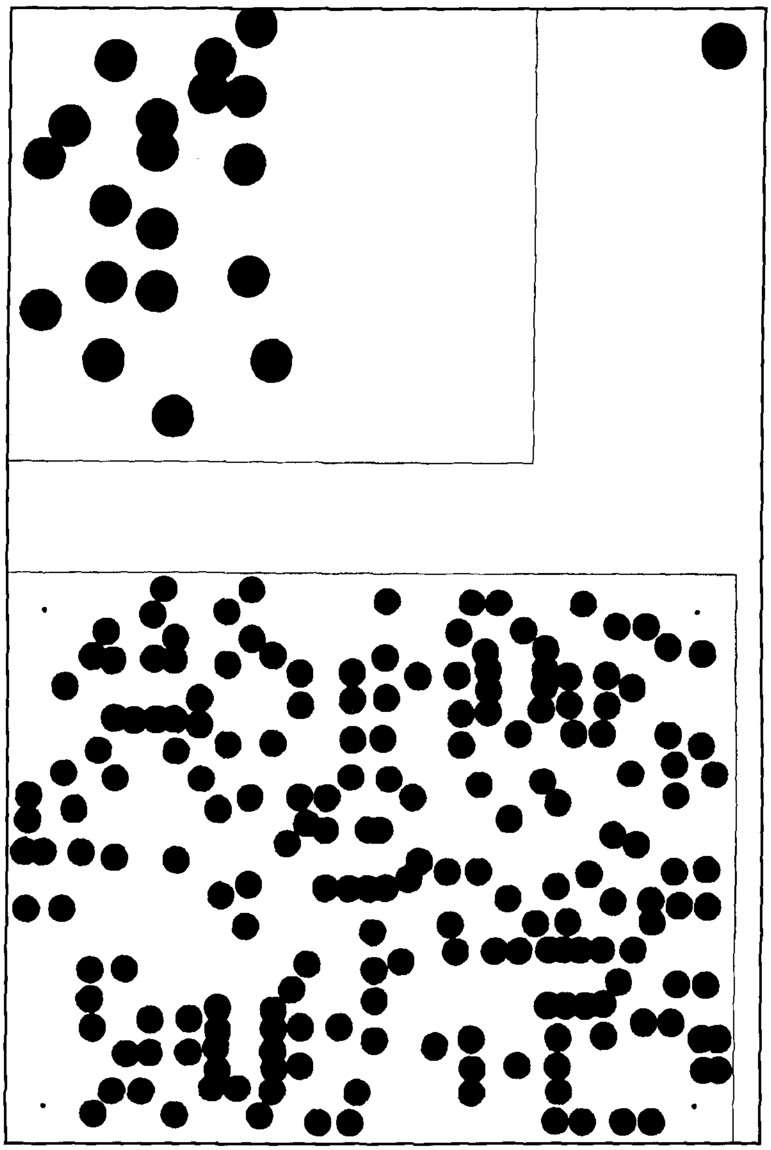

Figure 12. Masks for processor and power supply boards (component side).

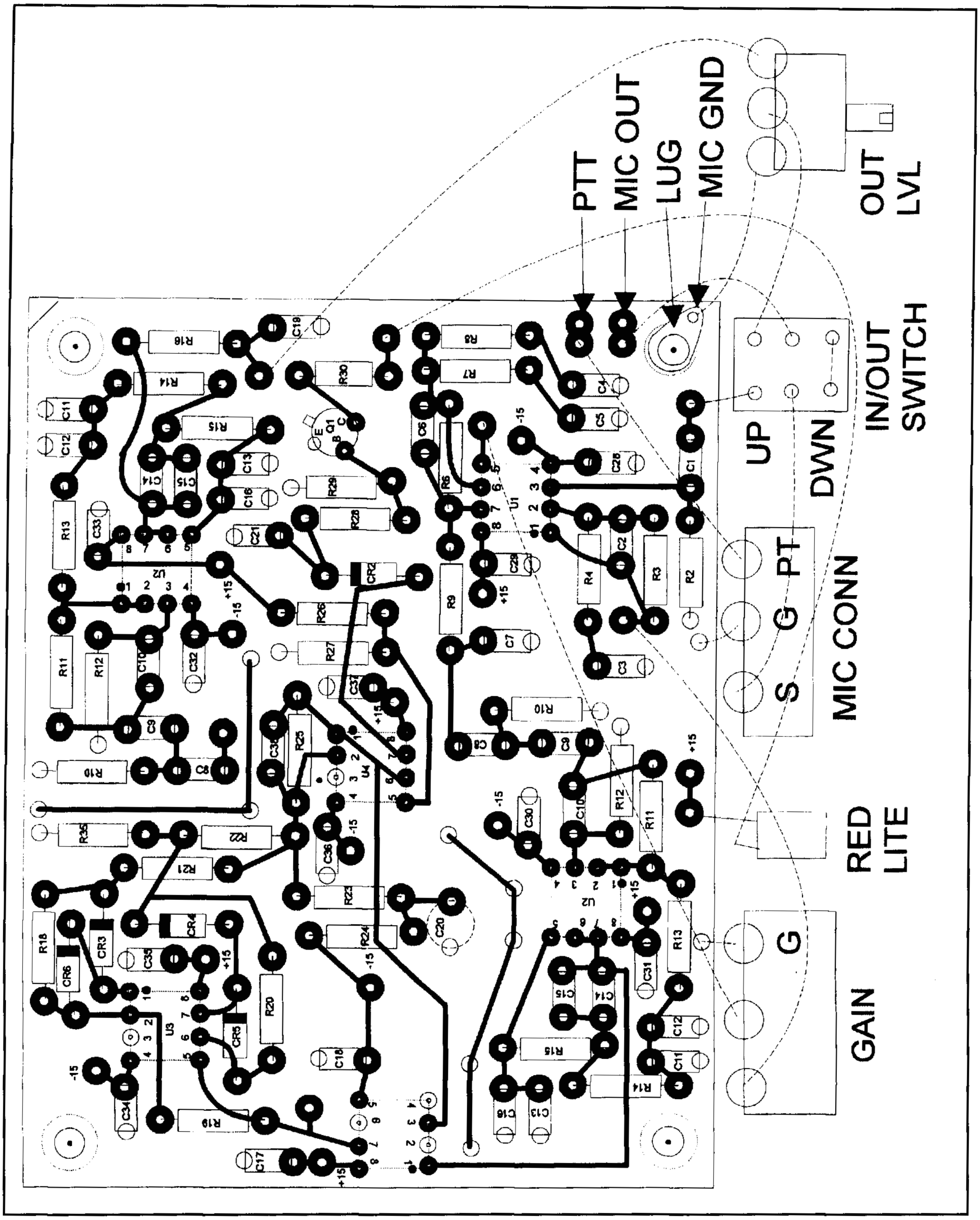

Figure 13. Trace side of processor board.

3.16 volts. If v_y drops below that level on voice peaks, the red LED flickers occasionally, accurately indicating the 10-dB limiting point. This simple approach has been very satisfactory, and the exact value of maximum processing is not at all critical.

Note from **Equation 4** that if v_x exceeds +/-14.5 volts (a 5.2 dB increase over +/-8 volts), the maximum soft-limiting is then 13.8 dB; v_o increases 1.3 dB (from +/-2.53 to +/-2.95 volts) and, beyond that point, hard clipping begins. There's about 4 dB (13.8 to 10.0) processing "headroom" after the red light comes on. Transmitter ALC should be able to protect the

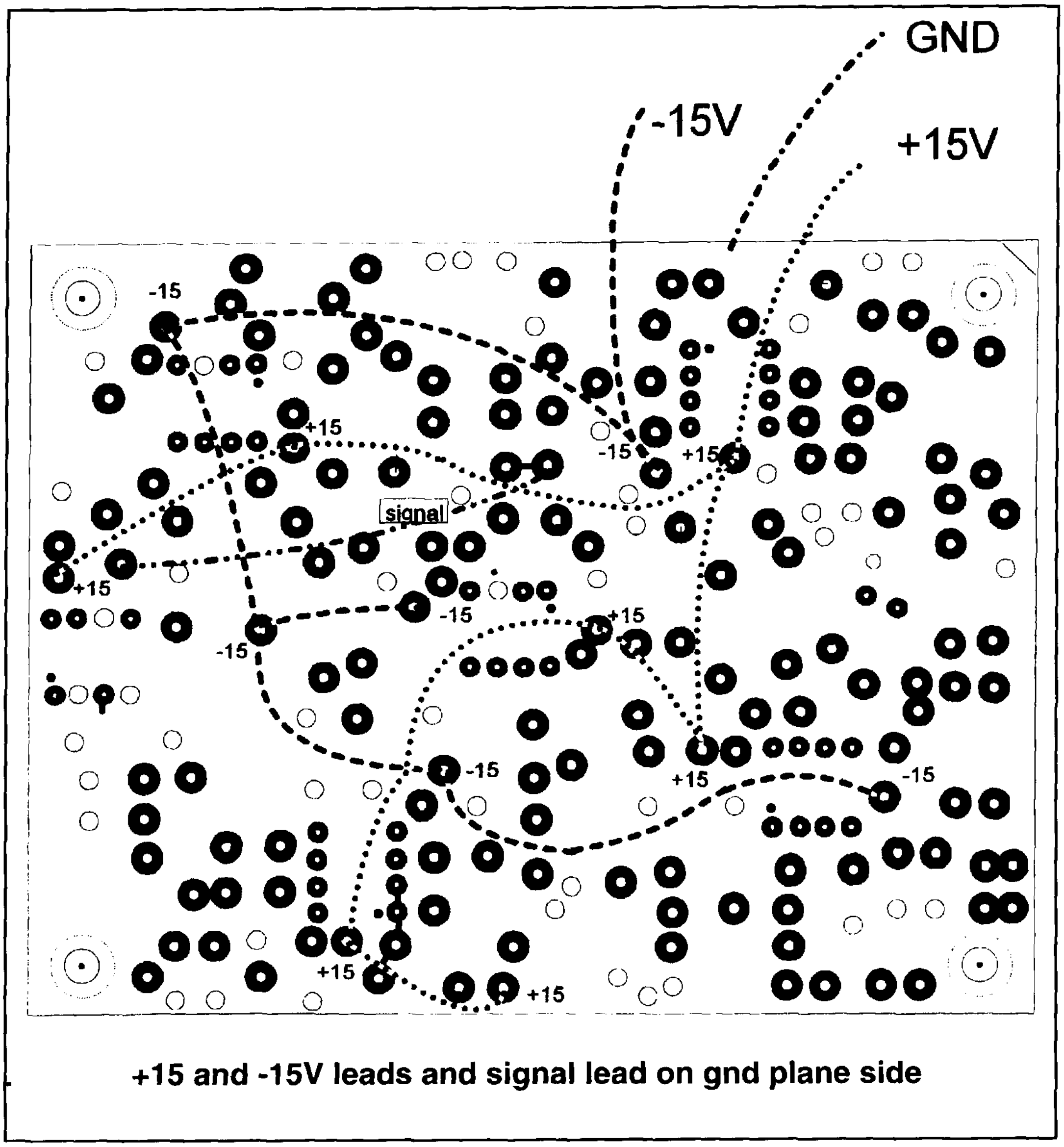

Figure 14. Ground place side of processor board showing +15 and -15 volt leads, and signal lead.

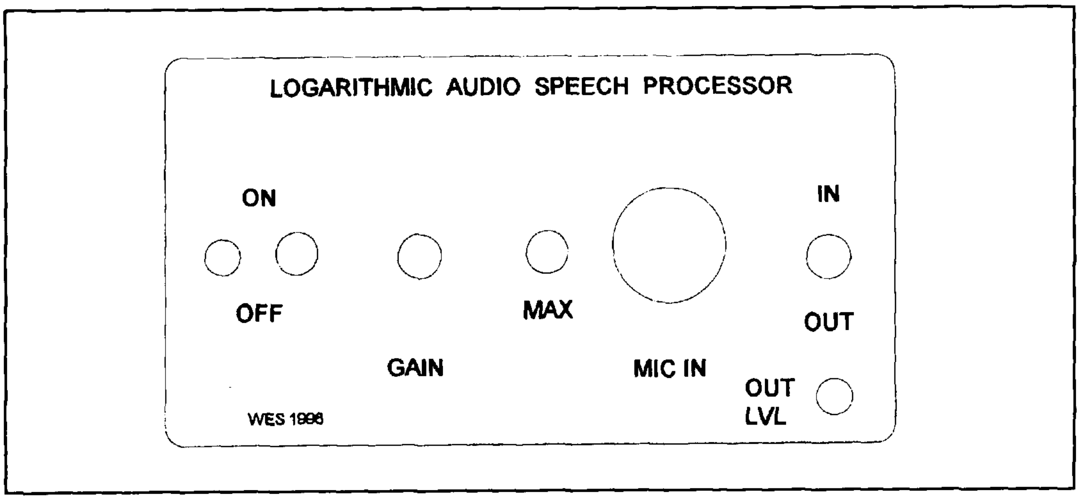

Figure 15. Front panel template.

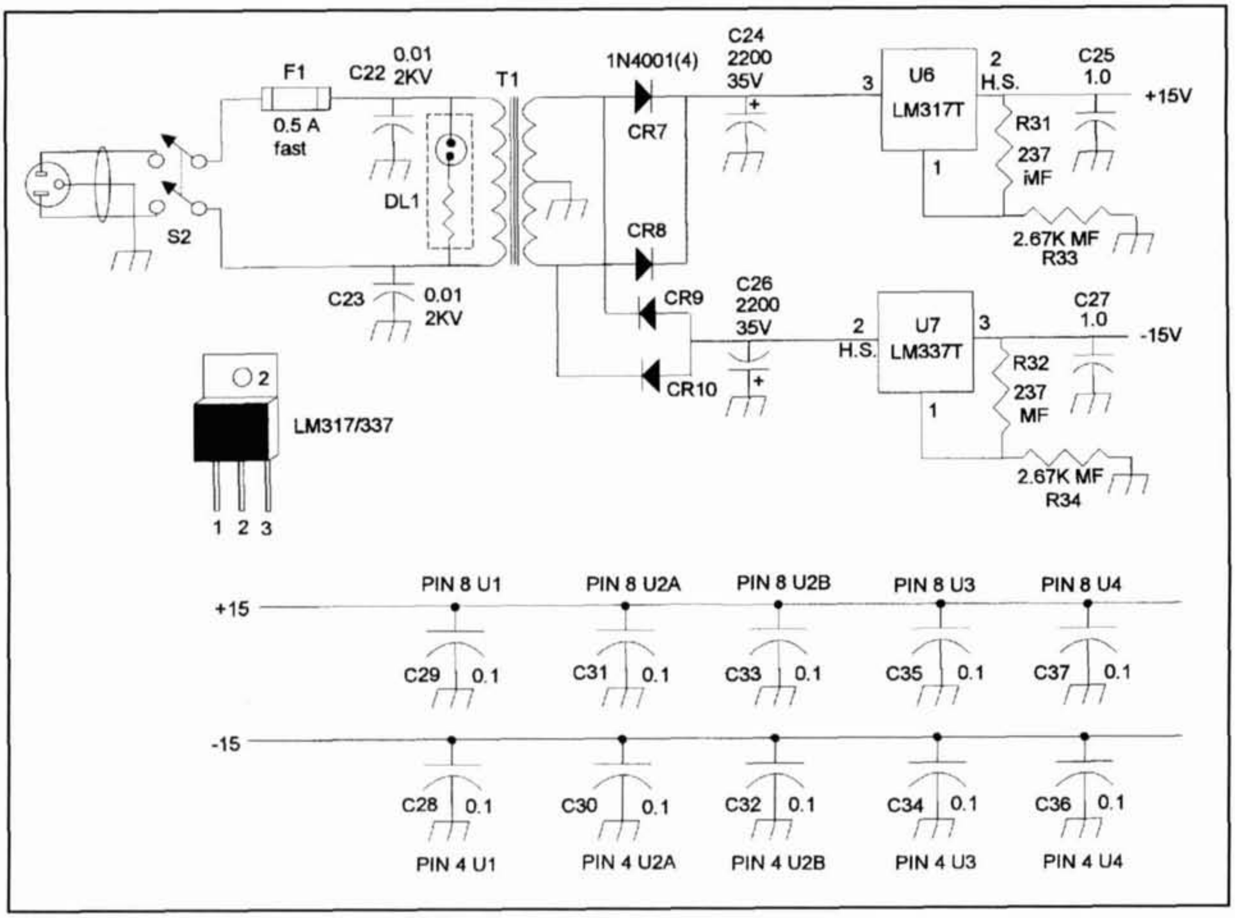

Figure 16. Power supply.

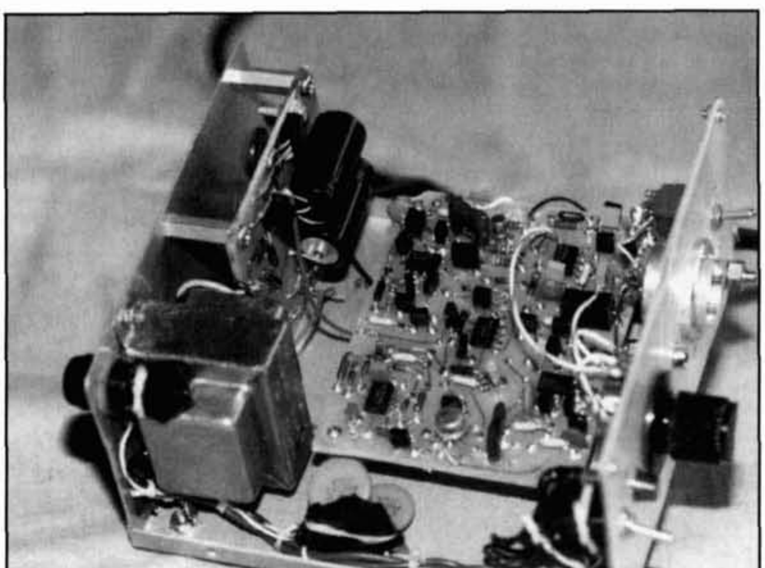

Photo C. Internal construction.

PA linearity with this additional 1.3 dB of signal, but the *processor* distortion will increase a few dB in this "overdrive" condition. These are the system considerations for this circuit.

Potentiometer R17 is screwdriver adjustable, and it is used to obtain identical output levels when the processor is switched in and out (red light flickering occasionally).

Photos B and **C** show the front panel and the internal construction. Masks for the processor and power supply boards are shown in **Figures 11** and **12**. **Figure 13** is the component side of the processor board; **Figure 14** is the ground plane. The cabinet was purchased from RadioShack and the front panel template is shown in **Figure 15**. The power supply in **Figure 16** provides regulated +15 and -15 volts. These regulators guarantee precise performance and hands-off operation. Parts placement is shown in **Figure 17.** For safety, use a three-wire line cord with a grounded chassis and be sure to tape up all exposed 120 volts AC circuitry. Use the microphone connector of your choice.

You may etch your own boards using the masks printed here, or you may purchase them from FAR Circuits. The price for a set of boards is $13 plus $2 shipping per order. Visa or MasterCard orders are welcome for a $3 service charge. To order boards for this project, contact FAR Circuits, 18N640 Field Court, Dundee, Illinois 60118.

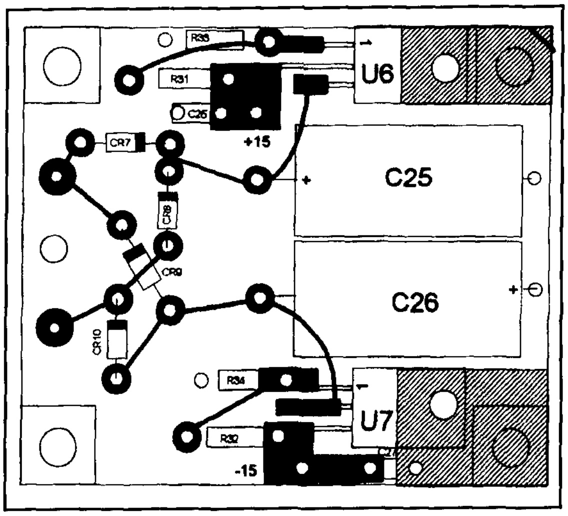

Figure 17. Power supply parts placement.

Adjustments

With the processor switched out of operation, talk into the mic and adjust the transmitter for correct operation that's both clean and at the correct power level. Observe the ALC meter. Now switch in the processor and, while talking, adjust the processor mic gain until the red LED blinks frequently on voice peaks. Then set the screwdriver-adjust output pot until the ALC level is approximately the same as before. A peak-reading RF wattmeter or an oscilloscope (that's what I use) is very useful for ensuring the right PEP level. Double check the out-of-band cleanliness to make sure there are no hidden problems, such as an ALC that's not working properly.

I think the overall effect, with an accurately measured 10 dB of soft-limiting, frequency pre-emphasis, and multiple bandpass filtering is very good. On-the-air comments, contest performance, and my own listening tests verify the cleanliness and effectiveness of this simple approach. A frequent comment is that the other operator's S-meter kicks up an S-unit or more. Depending on the dynamic response of the AGC and the S-meter (and also its calibration) at the receive end, this suggests the increase in average power due to speech processing.

There's always the temptation to use *more* processing (more is better, right?). I find this totally unnecessary and counterproductive. If the processing is pushed too much, the benefits of this simple approach will quickly erode. ■

REFERENCES

1. Sabin and Schoenike, *Single-Sideband Systems and Circuits*, Second Edition, Chapter 7, McGraw Hill, 1995.
2. Schleicher, "A Passive Limiter," *QST*, December 1966.

Parts List

Component	Description	Part Number
C1	0.01 µF	
C8(2),C9(2), C10(2),C15(2)	0.01 µF 5%	
C2,C6	47 pF	
C3	0.47 µF 5%	
C4	0.0033 µF 5%	
C5	0.1 µF 5%	
C7(2),C19	0.001 µF	
C11(2)	0.0047 µF 5%	
C12(2)	0.001 µF 5%	
C13(2),C38	100 pF 5%	
C14(2)	0.0047 µF 5%	
C16(2)	820 pF 5%	
C17,18,28-37	0.1 µF/50 volt	
C20	10 µF tantalum	RS 272-1436
C21	1.0 µF 55 volt	
C22,C23	0.01 µF 2 kV AC line	RS 272-160
C24,C26	2200 µF 35 volt	RS 272-1020
C25,C27	1.0 µF 50 volt	
CR1	Red LED	RS 276-068
CR2-6	1N4454 or equivalent	
CR7-10	1N4001 or equivalent	
DL1	Neon panel light	RS 272-708
F1	Fuse holder	RS 270-362
Fuse	1/2 A fast blow	RS 270-1047
J1/P1	Mic jack/plug	Newark 39F014/013
Q1	2N2222A	
R1	not used	
R2	330 k	
R3	221 k metal film	
R4	8.2 k metal film	
R5	10 k pot	RS 271-1721
R6	178 k metal film	
R7	22.1 k metal film	
R8	33.2 k metal film	
R9,R35	1 k	
R10(2)	47.5 k metal film	
R11(2)	18.2 k metal film	
R12(2)	332 k metal film	
R13(2),R14(2), R15(2),R27,R21, R22	10 k metal film	
R16	10 k	
R17	5 k mini pot, screwdriver adjustable	
R18,R19,R20	22.1 k metal film	
R23	33.2 k metal film	
R24	5.62 k metal film	
R25	26.7 k metal film	
R26	37.4 k metal film	
R28	22 k	
R29	22 k	
R30	680	
R31,32	237 metal film	
R33,34	2.67 k metal film	
R36	Not used	
S1	DPDT toggle	
S2	DPST AC switch	
T1	25.2 CT 450 mA	RS 273-1366
U1,U2(2),U3,U4	TL082	RS 276-1715
U5	AD534LH (Alternative AD633JN)	
U6	LM317T	RS 276-1778
U7	LM337BT	
Cabinet	3 x 5-1/4 x 5-7/8	RS 270-253

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MODERN RECEIVER DESIGN

Including Digital Signal Processing

Traditional radios, both receivers and transceivers, use analog parts that are bulky, expensive, subject to manufacturing tolerances, and require alignment during production. The number-crunching power of digital processing allows the replacement of many of these analog functions and moves the digital portions toward the antenna.

Efforts to implement digital signal processing (DSP) in communications equipment, specifically HF and VHF types, date back to before 1980. Then, the number-crunching capabilities were insufficient for the requirements of analog parts. In those days, microprocessors were too power hungry, expensive, and mostly found in state-of-the-art designs for validation of the principles of the approach. (A survey of the state-of-the-art in what today is called "*software*" radios appears in my book *Communication Receivers: Principles and Designs.*)[1]

Today, a number of manufacturers supply sufficiently powerful digital signal processors. The two best known are the Texas Instrument TSM 3232 series and the Motorola 56002. There are, however, subtle differences between these processors. The key difference is the availability of floating point arithmetic versus integer calculations, which determines price and power consumption. Many commercial/military and radio amateur transceivers rely

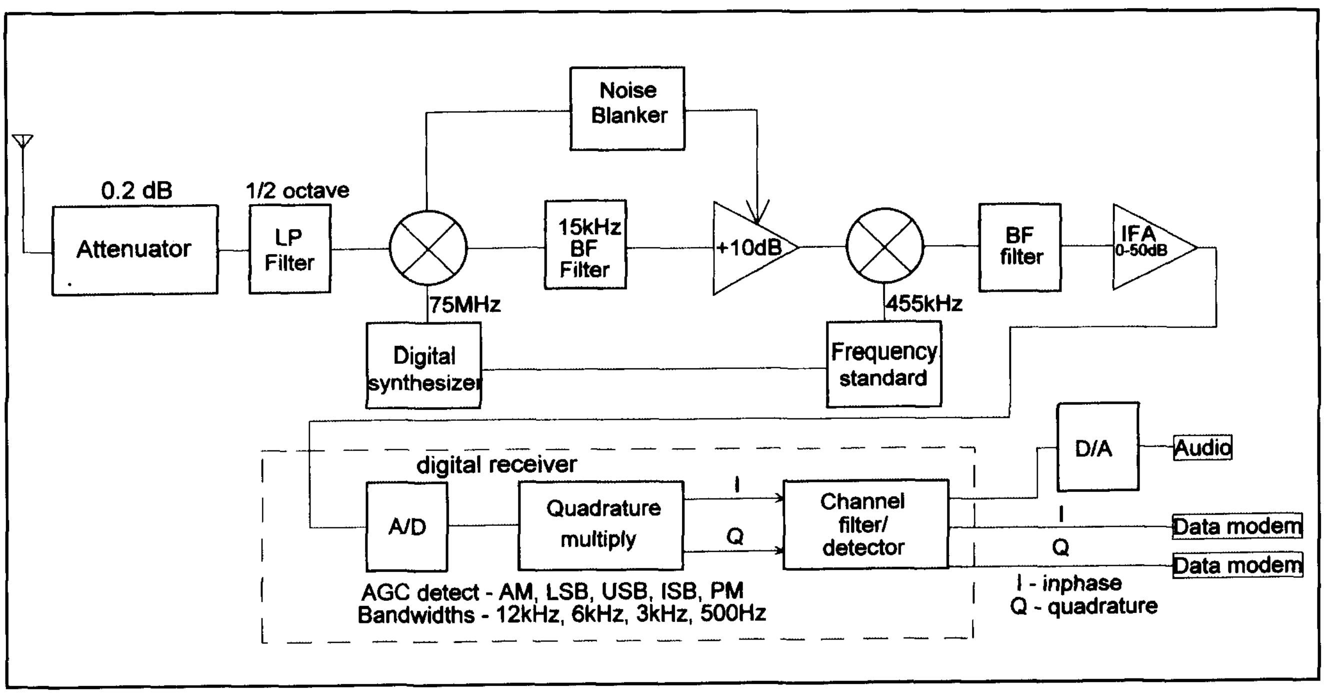

Figure 1. Block diagram of typical modern HF radio. Digitally implemented portions within dashed lines.

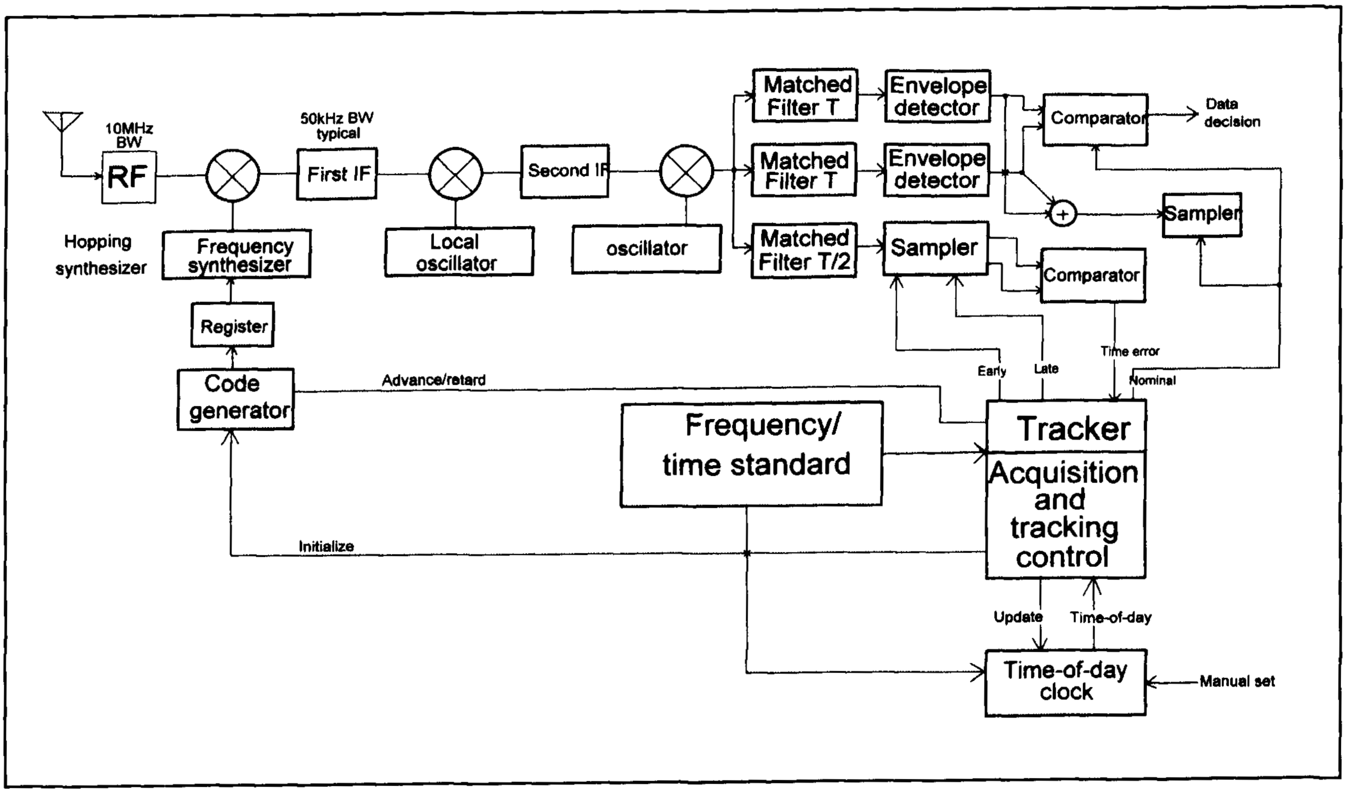

Figure 2. Typical HF receiver block diagram.

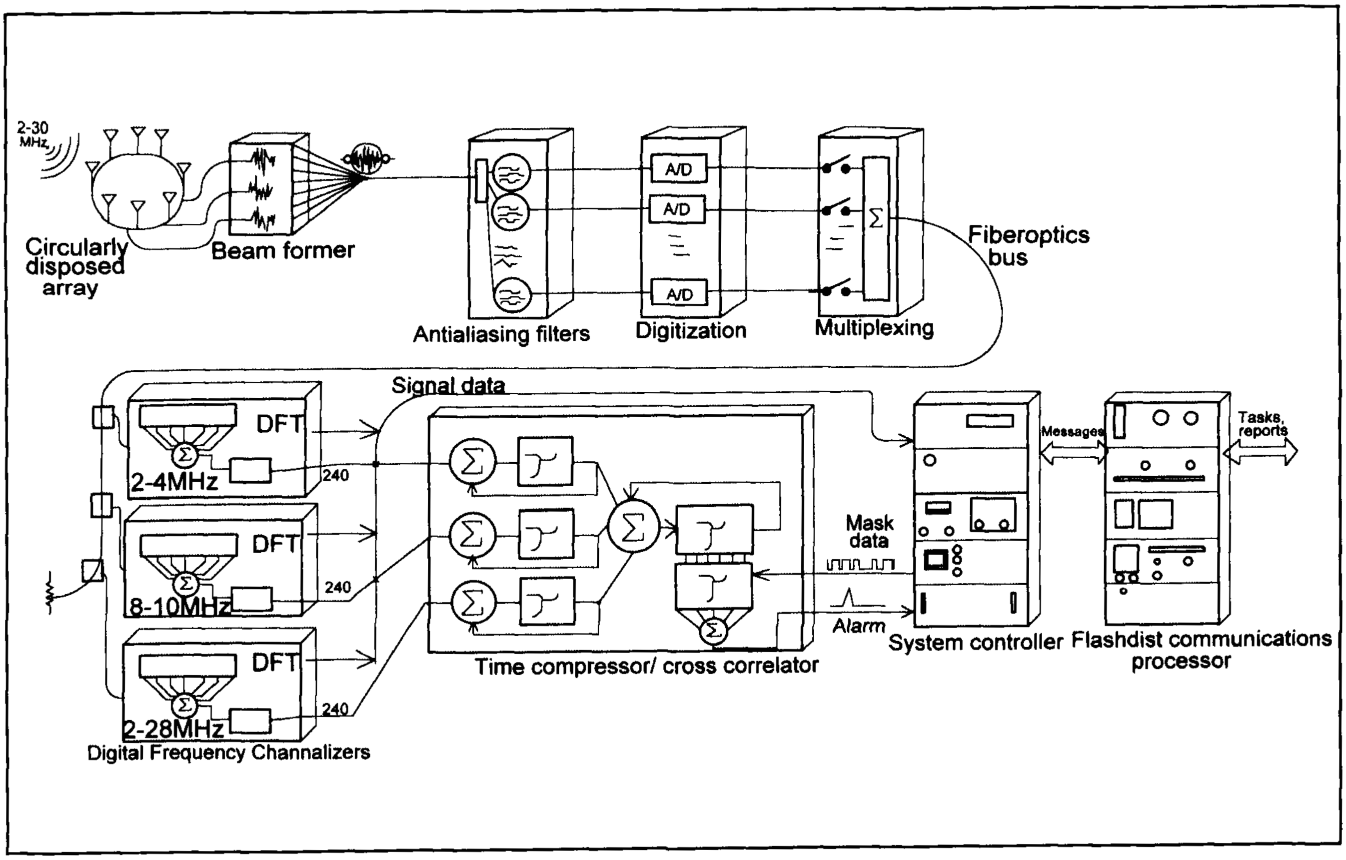

Figure 3. Block diagram of complete surveillance system.

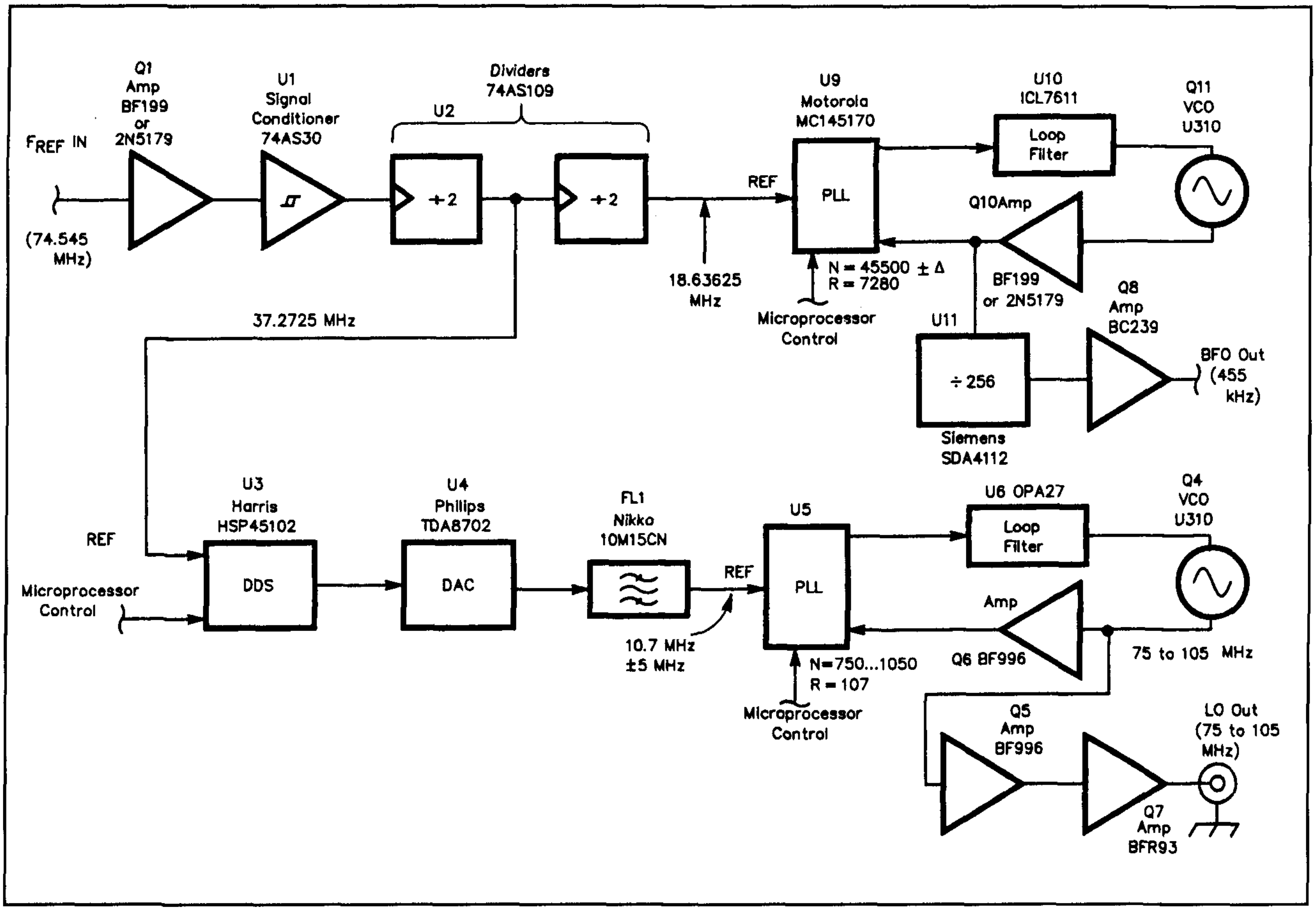

Figure 4. High-performance hybrid synthesizer for shortwave receivers.

mostly on the Motorola DSP chip. It comes in different flavors relative to computation speed.

I would like to discuss the few remaining problems in the hardware area, which determine the high performance capabilities of these transceivers, and to look at software solutions (DSP). Previous publications and advertisements have shown me that there is sufficient confusion concerning DSP, specifically in the use of DSP in IF or audio frequencies or a combination of both. Here the main differences in the applications seem to be the design and construction of high-performance IF filters and the use of DSP for "*cleaning up*" the signals. This cleanup goes back to the principle of echo cancellation in software and takes advantage of correlation techniques that remove unwanted signals and/or enhance those that are wanted.

Basic block diagram

As far as DSP is concerned, there is little difference between transmitters and receivers because the basic architecture allows bidirectional use. For this reason, I will concentrate on the receive path only, but will point out that the equivalent problems/solutions are relevant in transmit as well.

Figure 1 shows the block diagram of a modern HF radio. For various reasons, such as number crunching, the last IF is now 25 kHz or less, and the number of intermediate IF analog stages must be minimized. This is not only true with ham equipment, but also within military uses, such as frequency hopping, since the architecture becomes more complicated. It is apparent from **Figure 2** that the architecture of frequency hopping radios goes beyond the purpose of this paper, but some of the control mechanisms and number-crunching capabilities are consistent with this. In general, modern radios are not only used for point-to-point communications, but also for radio monitoring. Based on the complexity of the signals, the actual radio can become quite complex. **Figure 3** shows a complete surveillance system that can be easily expanded in frequency range. It does not require much imagination to envision the software requirements needed to collect all the data.

The transition for existing radios like the Rohde & Schwarz EK 890 to DSP-based radios like the EK 895 is performed by replacing the conventional analog IF section and the audio

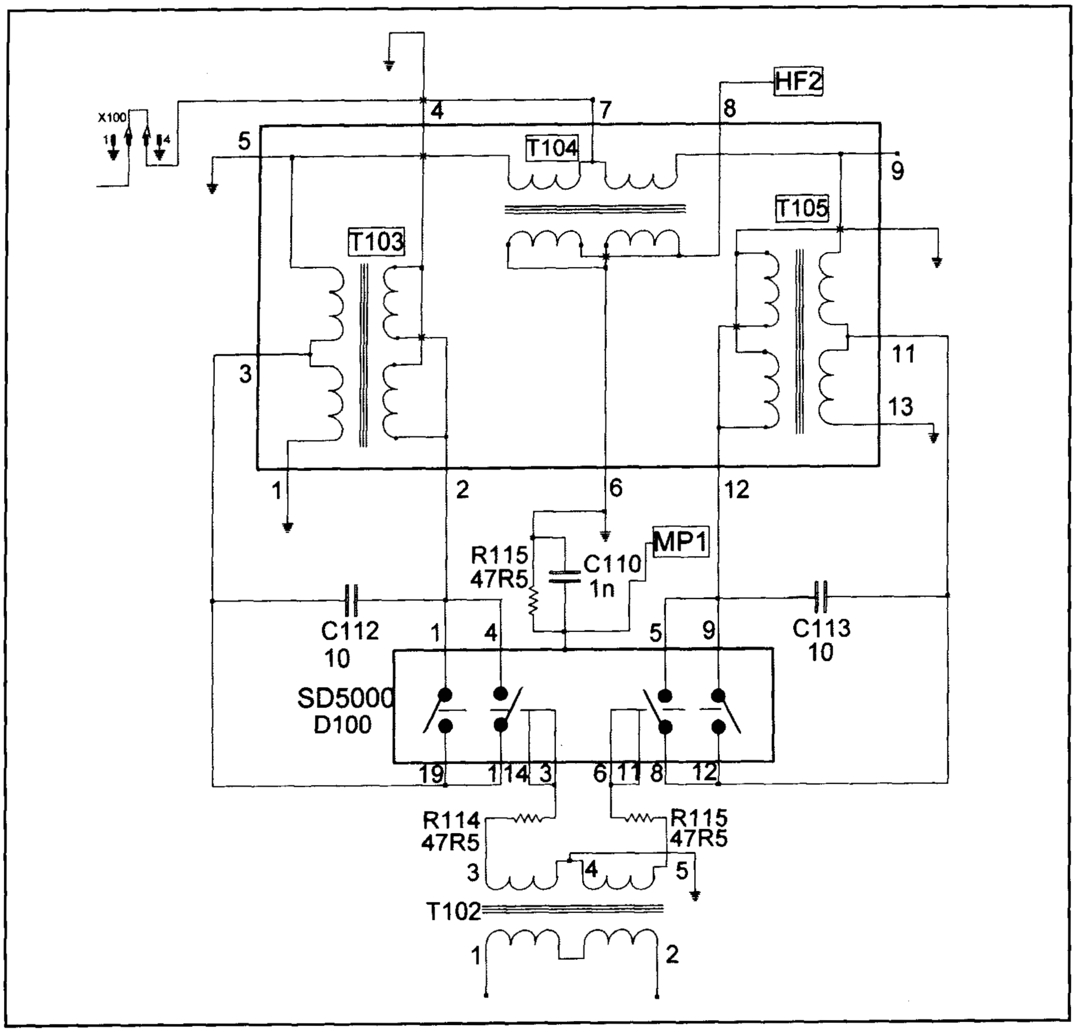

Figure 5. High intercept point mixer using FET switches.

portion with the appropriate DSP. In the EK 895, the performance increase in the DSP area is more dramatic than the catch up in the hardware area in the front end. The weakest links are the input filter switching, the input mixer and its roofing filter (it's too wide for cost reasons—narrow filters cost three to five times more), and the synthesizer.

Table 1. Receiving bandwidths in Hertz.

3 dB	60 dB
+/-25	+/-75
+/-75	+/-150
+/-150	+/-225
+/-300	+/-430
+/-500	+/-770
+/-750	+/-990
+/-1050	+/-1600
+/-1200	+/-1760
+/-1350	+/-1900
+/-1550	+/-2100
+/-3000	+/-4200
+/-4000	+/-5200

The jury is still out on whether direct digital signal (DDS)-based synthesizers are better or whether one should use the fractional division synthesizer approach. In the case of multimode transceivers, it is possible to apply fast modulation to the fractional division N synthesizer, but care must be taken not to violate some of the patents around this area. **Figure 4** shows a synthesizer, which I published recently.[2] Its phase noise requirements are quite sufficient compared to shortwave dynamic requirements.

MOS switches in mixers have also improved the dynamic range. The schematic in **Figure 5** shows a quad circuit with a measured 3rd order intercept point of 40 dBm or better, with a 2nd order intercept point of 77 to 80 dBm, and an insertion loss of about 6.5 dB. Its upper frequency limit of about 100 MHz is determined by the actual physical construction and the capacitance of the MOS transistors.

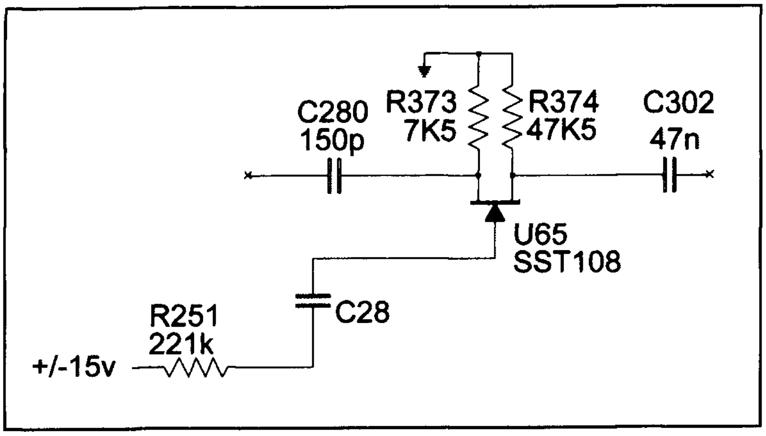

Figure 6. Improved filter switching system using JFETs

Motorola is working on LD MOS devices for power applications that show high power output up to 40 watts at 1 GHz. It is now possible that a side scaled-down version of the transistor would allow a quad-mixer design that can be operated above 1300 MHz. The roofing filter, which is driven by the mixer, is also in the critical path for radio amateur applications with FM capabilities. This filter is generally found to be too wide and deteriorates the performance. A +/- 5 kHz filter is still too expensive for ham equipment, but the commercial users with their narrowband frequency modulation (NBFM) applications take advantage of it. This is the last headache for users of ham equipment, and it would be nice to have a retro-fit available. Radios with multiple IFs operating in CW mode show severe in-band intermod products.

The final headache, so to speak, remains the input filters' switching mechanism. For low loss, relays are the best choice; however, for more affordable applications, a novel technique using JFETs has heavily biased switches with essentially no DC supply voltage.

Figure 6 shows the simple gating arrangement. The only complication that arises for the designer has to do with the generation of a positive and negative voltage to bias the gate. Companies such as Maxim manufacture small inexpensive DC-to-DC converters and, therefore, single power supply radios can be updated easily. Having shown intermod performance that is better than the mixer, the diodes are transparent in the design.

DSP and the radio

As outlined in the introductory paragraphs, digital signal processing, which is really performed by a complex chip set, is used both in the IF and the audio. In order to sound modern and "*jump*" on the bandwagon, many companies have incorporated the DSP in the audio area with limited performance increase.

The first truly affordable *all* DSP transceiver is Kenwood's TS-870. It is a combination of well-established techniques and moves the input frequency from a first IF of 73.5 MHz to 8.8 MHz, 455 kHz, and finally down to about 11 kHz. In high-end transceivers, like the Rohde & Schwarz XK2100, the second IF jumps down 25 kHz directly. This can be established by using an image reject mixer. Such a scheme avoids the close-in intermodulation distortion (IMD) problems. **Figure 7** contains a more detailed block diagram of a digital SSB receiver as mentioned in **Reference 3**. After review, it becomes apparent that the digital portion of the receiver starts at the A to D converter and the overall performance is highly dependent upon this converter.

The Rohde & Schwarz XK2100's block diagram illustrates the following properties: The gain from the antenna to the input of the A to D converter is 48 dB with an AGC (automatic gain control) range (analog) of about 34 dB. The A to D converter has an impedance input point of 15 k, so part of the gain is due to the impedance transformation from 50 ohms to 15 k. The A to D converter part of the DSP system is a 16-bit device with a 96-dB signal-to-noise ratio from 5 volts peak-to-peak input maximum voltage down. The A to D converter operates at a 3.2 MHz reference sampling frequency externally and then internally reduces this to 100 kHz sampling.

These types of A to D converters are also referred to as Sigma (Σ) Delta (Δ) converters, which consist of a system wherein high accuracy is obtained at relatively slow sampling rates. This is accomplished by grossly oversampling with a 4-bit A to D converter or higher in a feedback loop. At the same time, the requirements of the analog anti-aliasing filter are considerably relaxed. The associated low-pass filter needs to be only half of the sampling frequency and, therefore, is 50 kHz.

By using a mixing process that occurs due to undersampling, we can translate the channels to a baseband with a narrower decimating filter. This decimating process is dependent on the actual bandwidth. As the bandwidth becomes narrower, the sampling moves from 25 to 12.5 to 6.25 kHz and ultimately down to 1.78 kHz. This sampling frequency is reduced to maintain the same amount of number crunching and, therefore, the same delay.

While maintaining a 16-bit arithmetic, the filter types chosen still have up to 20 mS delay to calculate. Such a system will be difficult for ARQ operation. The type of filters calculated by the DSP system are called FIR (finite impulse response) filters. **Figures 8** and **9** show their characteristic appearance. Rather than going into the noise floor, these filters

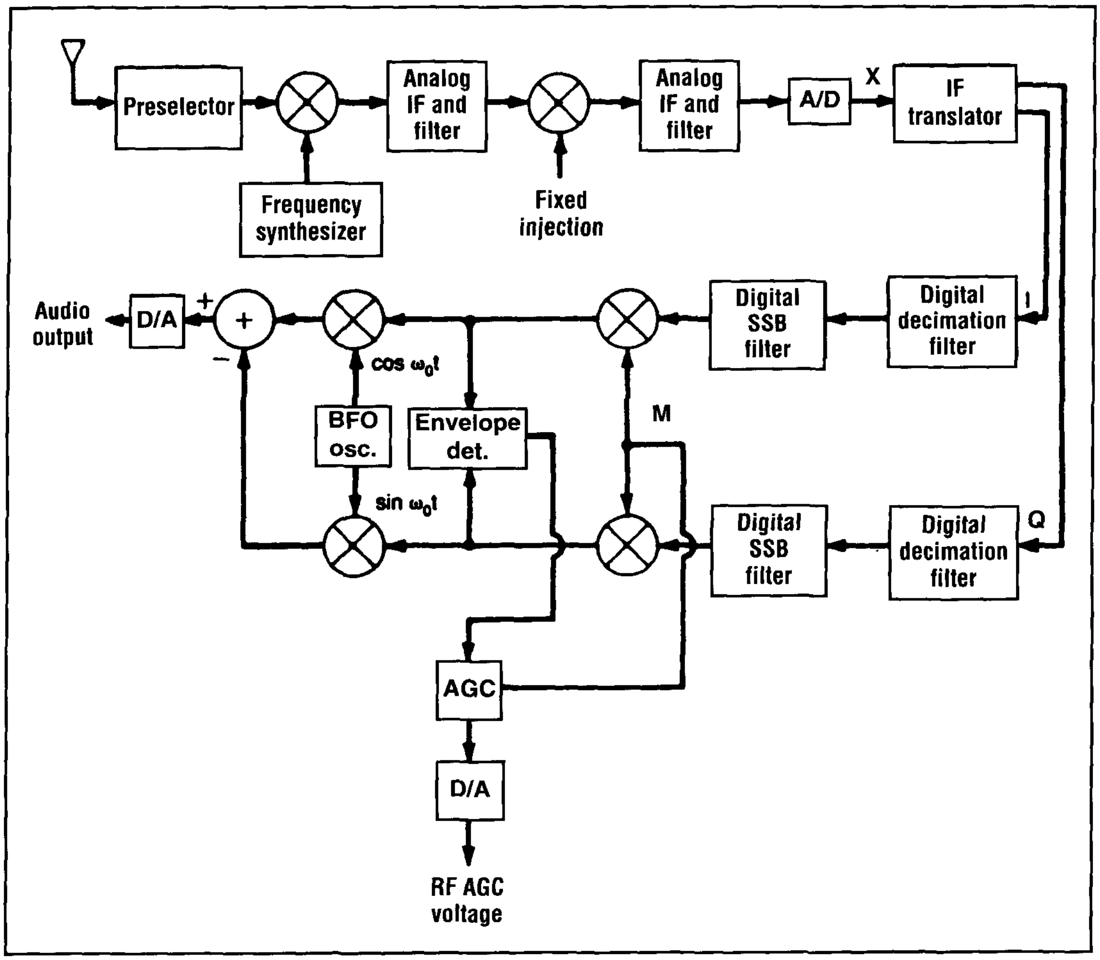

Figure 7. Block diagram of a digital SSB receiver.

have a stop-band ripple typical for these types of digital filters. A more dramatic presentation of this is shown in **Figure 10**.

The use of FIR filters allows for the design of arbitrary selectivity curves and orders as high as the 100th. The main advantages these DSP filters offer is that the time delay is absolutely flat and constant with varying frequencies.

It is practically impossible to build such filters in analog form. As to the ringing noticed in CW, there are two causes. One is due to the reduced bandwidth and the other is due to group delay distortion. These particular types of FIR filters do not add any ringing; therefore, for a given bandwidth, the FIR filter rings less than a conventional filter.

Another problem can also occur if the skirts are made steeper than necessary. There is certain splatter or bandwidth emissions from all amplitude-modulated signals, and because one seldom has the task of removing only a constant carrier (this is done at a different place than the DSP), excessive shape factors only punch holes into noise producing a sinusoidal voltage output much like ringing. **Table 1** is a useful selection of bandwidths and shape factors for receivers.

The DSP unit not only provides the selectivity, but also handles the automatic gain control. For these types of systems, dual-loop AGC is required. The analog portion of the AGC, which is wrapped around the input stage, takes over after the input signal reaches sufficiently high levels. This threshold is typically set between 1 and 5 mV.

Some noise calculations

The "digital" S/N ratio:

$$\left(\frac{Ps}{N0q}\right) = -1.25 + 10 \bullet \log(\mathrm{Fs}) + 602 \bullet b$$

where:
F_s = A to D sample rate
b = number of bits

$= -1.25 + 10 \bullet \log(25E3) + 602 \bullet 16$
$= -1.25 + 44 + 96.32$
$= 139$ dB

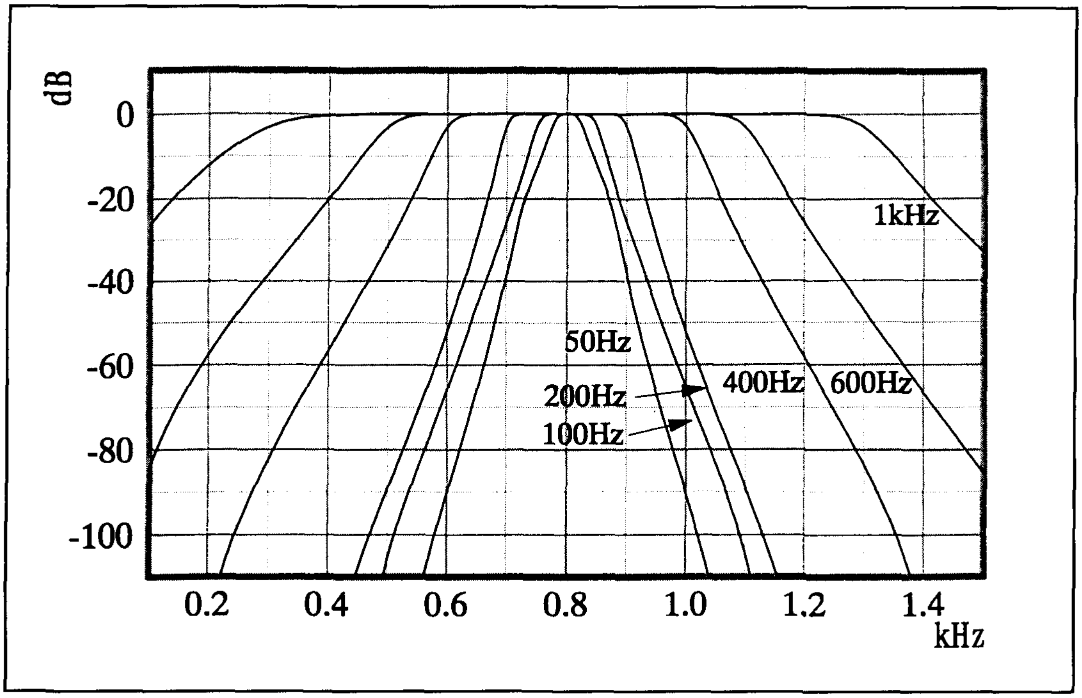

Figure 8. CW filter width.

This is the theoretical maximum signal to quantization noise density ratio. It is somewhat similar to the signal-to-noise ratio using sinusoidal waveforms.[4]

If our A to D converter has 5 volts P_P then,

$$N_q = \frac{(V_{p\text{-}p})^2}{12 \bullet 2^{32}} = \frac{25}{12 \bullet 4.3E9}$$

$$= 484\text{E} - 12 \text{ Watts}$$

From this equation, $U^2/R = N$, we solve:

$$U = \sqrt{50 \bullet 23E - 12}$$

$$= 34\ \mu\text{V or}$$

$$= 95\ \mu\text{VP\_P}$$

The noise figure can be expressed as:

$$F = 1 + \frac{(VP\_P)^2}{6KTR_S F_S} \quad \text{with}$$

where:
K = Boltzman's constant (1.38E-23),
T = Room temperature degrees Kelvin (300)
R_s = Generator impedance of the A to D converter (15 k)
F_s = Sample frequency of A to D converter (25E3)

Therefore:

$$F = 1 + \frac{(95\text{E} - 6)^2}{6 \bullet 1.38\text{E} - 23 \bullet 300 \bullet 153\text{E}3 \bullet 253\text{E}3} = 970$$

$$F = 10 \bullet (970) \approx 30 \text{ dB}$$

To determine the analog gain, we solve the Friis formula for VG_1:

$$F_{TOT} = F_{input} + \frac{F_2 - 1}{VG_1} \quad \text{with}$$

where:
F_{input} = noise factor of the input stage
F_2 = noise factor of the A to D converter
VG_1 = voltage gain of the preamp system

We solve this for VG_1 with the understanding that we want a total noise factor of equal to or better than 10. Assuming that the input storage noise figure is 3 dB, we now obtain:

$$10 = 3 + \frac{970}{x}$$

Solving this for x results in:

$$x = \frac{970}{7} = 138.57 \text{ or } 42.8 \text{ dB}$$

This is the required voltage gain to match the prescribed noise figure. Recall that we had

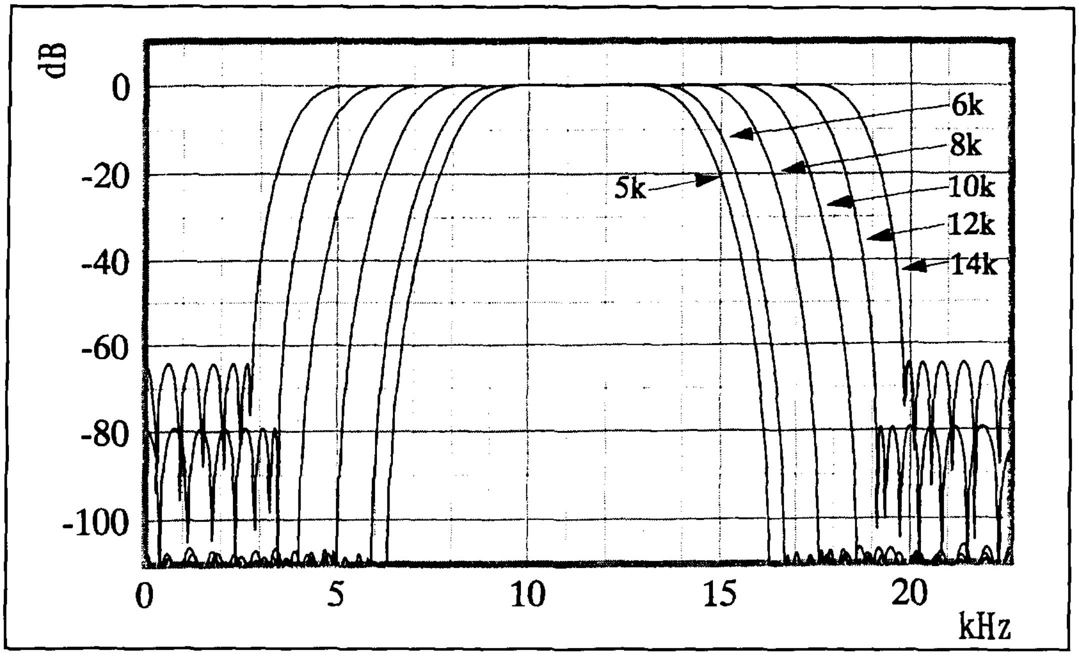

Figure 9. AM/FM filter width.

already set the preamplifier gain to 48 dB, allowing for a safety margin towards tolerance and differentiating between sinusoidal and quantization noise.

Noise cancellation

Besides providing superb selectivity in filters, the other attractive feature of DSP is its ability to deal with correlated and uncorrelated signals. The DSP processors either at RF or IF levels or at audio frequencies can compare signals and determine whether or not they are: not correlated, slightly correlated, or totally correlated. Such adaptive filters were developed for echo cancellation in long distance telephone lines. In the book *Introduction to Adaptive Filters*[5] by Simon Haykin, these methods are well described. The DSP can detect certain classes of signals and subtract them from a wide frequency band, thereby effectively canceling signals. This is done in the time domain. The opposite is possible, or noncorrelated signals can be removed, enhancing the correlated signals. Modern noise reduction techniques and automatic notch filters are a combination of both.

Given the number of adaptive filters, we can distinguish between a) adaptive noise canceler; b) adaptive self-tuning filter; c) canceling periodic interference without an external reference source; d) adaptive line enhancer; e) system modeling; and f) linear combiner. Regardless of whether the noise reduction algorithm is the Widrow-Hoff Least Mean Square (LMS) algorithm, or the Discrete Fourier Transform (DFT)-based "spectral subtraction" algorithm, DSP noise reduction works by finding the most significant spectral lines in a signal and then forming bandpass filters around the strongest energy concentrations. The particular algorithm only determines how this is accomplished. To understand adaptive noise reduction, it helps to think about filters in a different way.[6]

A very nice write-up on this topic is found in "Using the LMS Algorithm for QRM and QRN Reduction."[7] For those of you who are not radio amateurs, QRM refers to interference adjacent to the wanted signal and QRN refers to noise static. The various DSP units presently available on the market operate in either frequency or time domain. Because of the transformation, some of them require extensive number crunching, and the products by JPS, which generally receive high marks, transform the information from the time domain into the frequency domain and back. This method is called "spectral subtraction." The resulting delay from this can be several hundred mS.

Without going into details on how to design those, I would like to present some pictures that deal with the noise reduction itself.

Figure 11 shows a spectrum from zero (0) to 4 kHz with a wanted signal around 1.5 kHz and two interfering signals—one at 1 kHz and one at 3 kHz. After activating the auto-notch, the interfering signals are significantly reduced as is shown in **Figure 12**. The DSP-based filtering can be performed at the AF (mostly) and the IF (hopefully). The IF filtering requires significantly more number crunching. **Figure 13** shows the automatic notch filter rather than

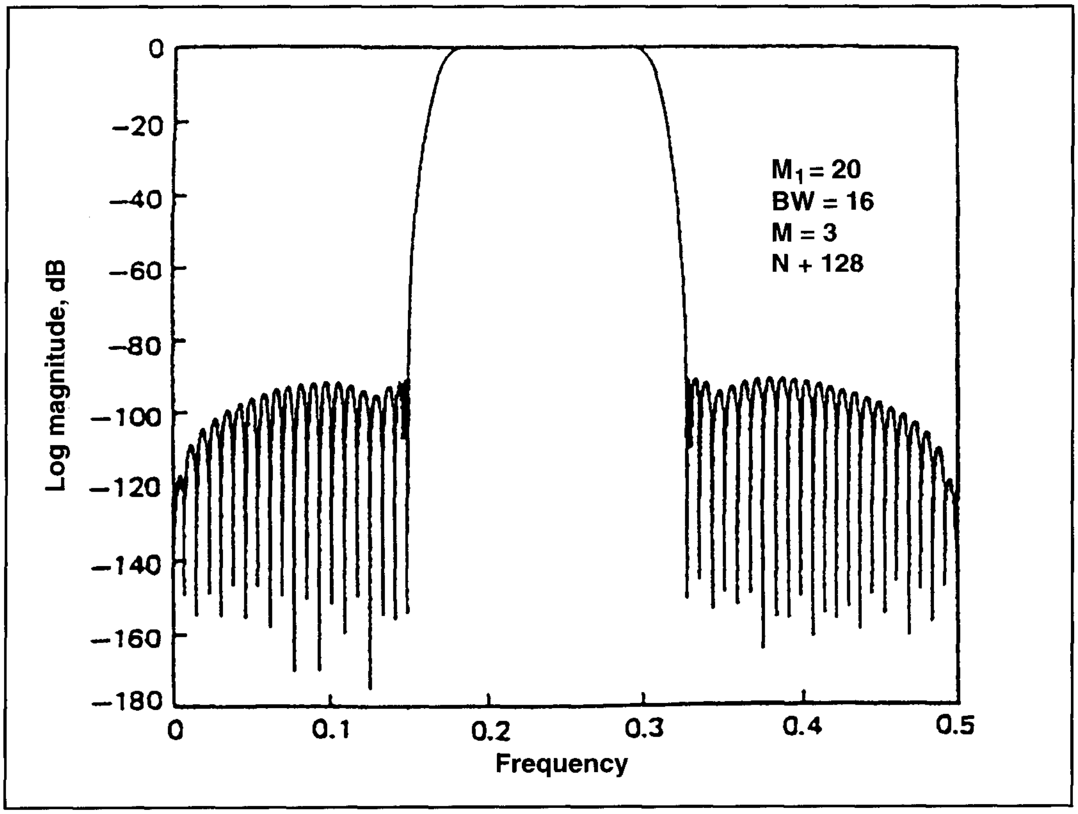

Figure 10. More dramatic presentation of the characteristic appearance shown in Figures 8 and 9.

beat cancellation done via DSP at the IF level. **Figure 14** illustrates the effect of the automatic notch filter compared with an analog version, such as the Kenwood TS 950SDX. The TS-870 is the first unit that allows beat cancellation in the audio and auto-notch in the IF.

Depending on the signal type, these systems have different levels of effectiveness. The required number crunching is significant, and the Kenwood engineers told me they were not able to provide noise reduction and notch filter simultaneously. **Figure 15** shows the general diagram of the adaptive filter used in the TS-870; **Figure 16** is the block diagram of the correlation method used for noise improvement. Finally, **Figure 17** shows the signal-to-noise ratio as a function of the various adaptive filters or correlation match system. I predict the next generation of DSP radios will need to have more computation power to deal with this situation.

Spectral Subtraction

Spectral subtraction is another way to reduce the noise in voice signals. The technique accomplishes much the same thing as the LMS algorithm, but in a different way.

Up to this point, all of the DSP algorithms we have discussed work by processing a series of numbers that represent the signal waveform as a function of *time*. Spectral subtraction, on the other hand, works by processing a series of numbers that represent the *frequency content* of our input signal.

To do this, DSPs use a relatively complex mathematical operation (called a transform) to change the signal representation from the *time domain* to the *frequency domain*.

For example, what comes out of an analog-to-digital converter is a series of numbers that represent the audio voltage in time increments at 0 μs, 100 μs, 200 μs, etc. The transformation operation yields a series of numbers that indicate signal energy in *frequency* increments at 300 Hz, 320 Hz, 340 Hz, etc., up through 3000 Hz, or more.

A complementary inverse transform returns the frequency data to a time-domain signal. If we do the time-to-frequency transform and follow it immediately with the frequency-to-time (inverse) transform, we get our original signal back.

Spectral subtraction is a three-step process:

1. Transform signal to frequency domain.
2. Process frequency domain data.
3. Inverse transform back to time domain.

This process repeats for successive short segments (a fraction of a second) of audio.

It relies on two assumptions:

1. Voice-frequency energy is concentrated in a small number of frequencies, and

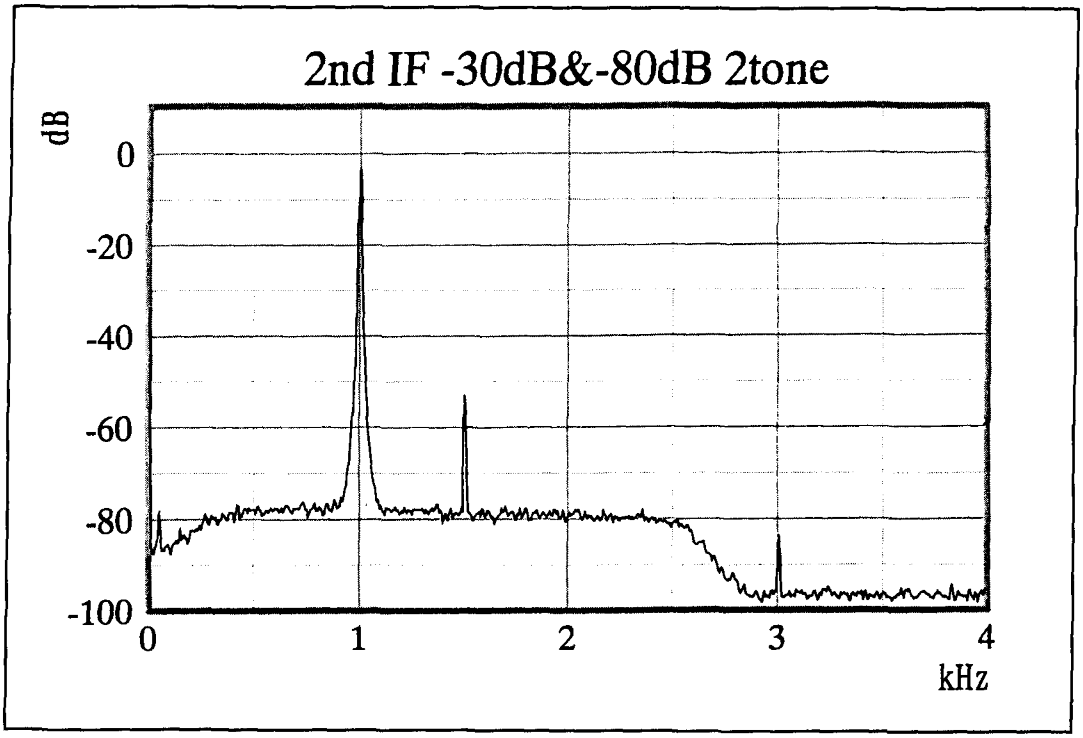

Figure 11. Wanted signal of 1.5 kHz in the presence of 1 and 3-kHz interfering signals.

2. Noise energy is uniformly distributed throughout the audio spectrum.

Using spectral subtraction algorithms we try to determine the "noise floor" of a signal. The process assumes that any frequency domain value at or below the noise floor is noise and sets the energy at that frequency to zero. Conversely, it considers the signal above the noise floor to be voice components and allows them to pass.

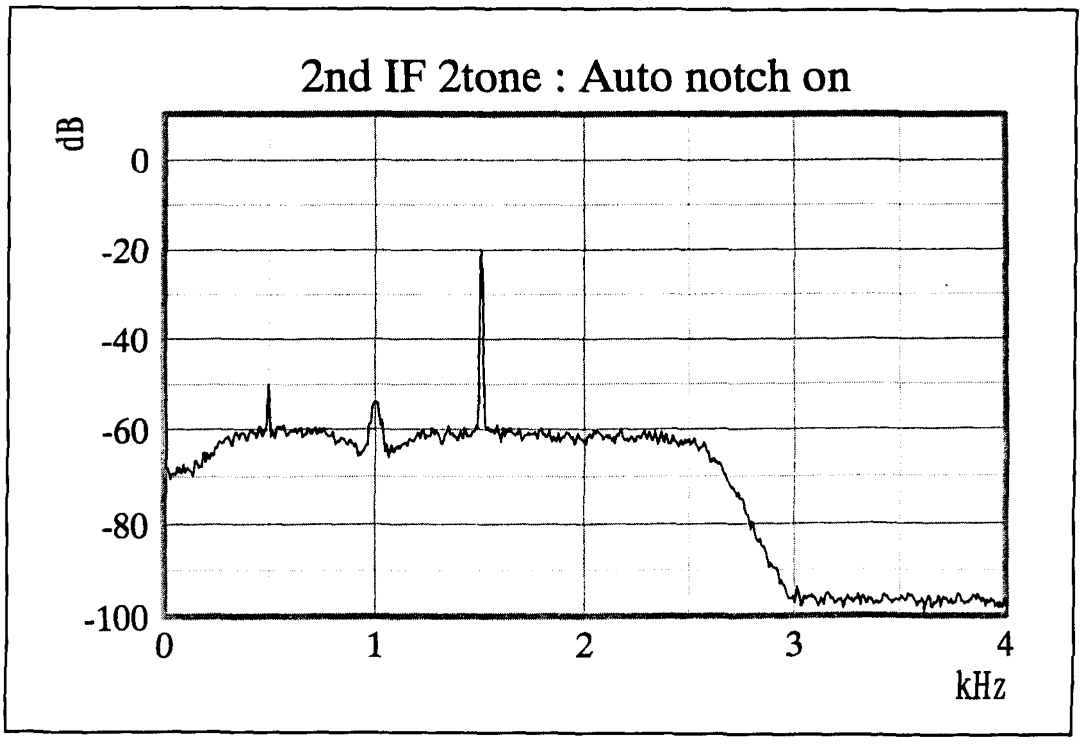

Figure 12. DSP removed interfering signals at 1 and 3 kHz shown in Figure 11. These automatic multi-tone notches/beat cancellations provide up to 50 dB attenuation.

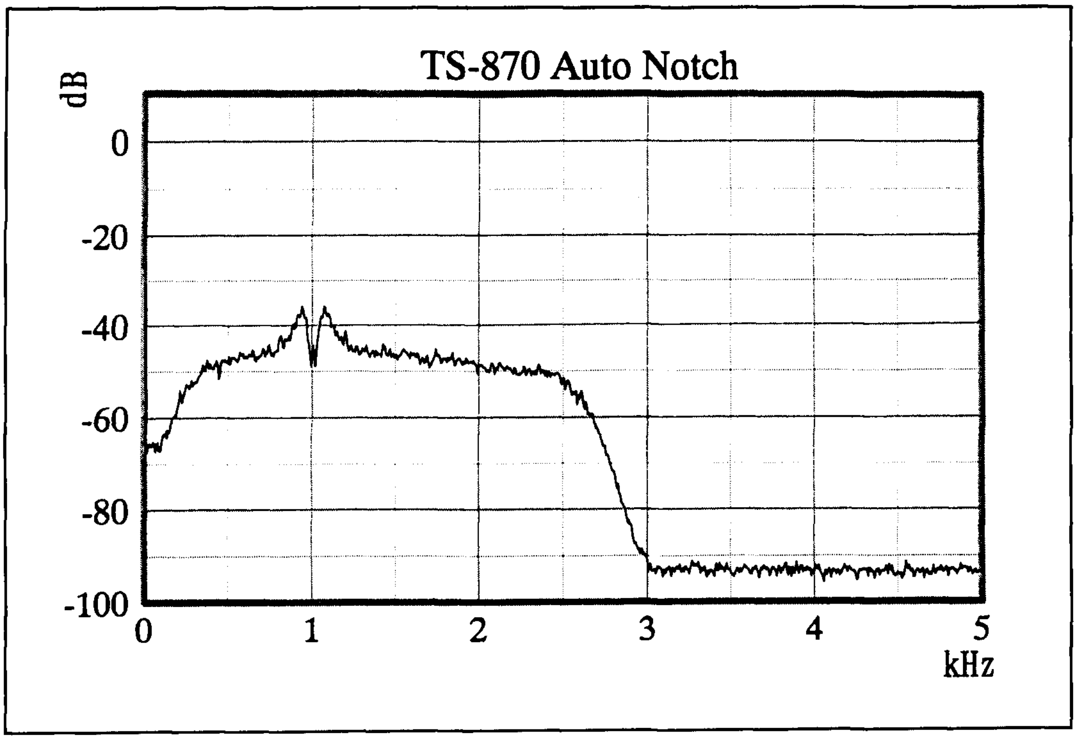

Figure 13. TS-870 auto notch (IF). Note the single beat rejection at 1 kHz.

Some amateur DSPs use spectral subtraction for noise reduction, but the algorithm has several disadvantages.

1. It takes a substantial amount of time to perform the forward and inverse transforms. The resulting delay through the DSP (a fraction of a second) can create an annoying "electrical backlash." The delay makes it difficult to rapidly tune receivers because the audio and dial position are not synchronized. The delay also

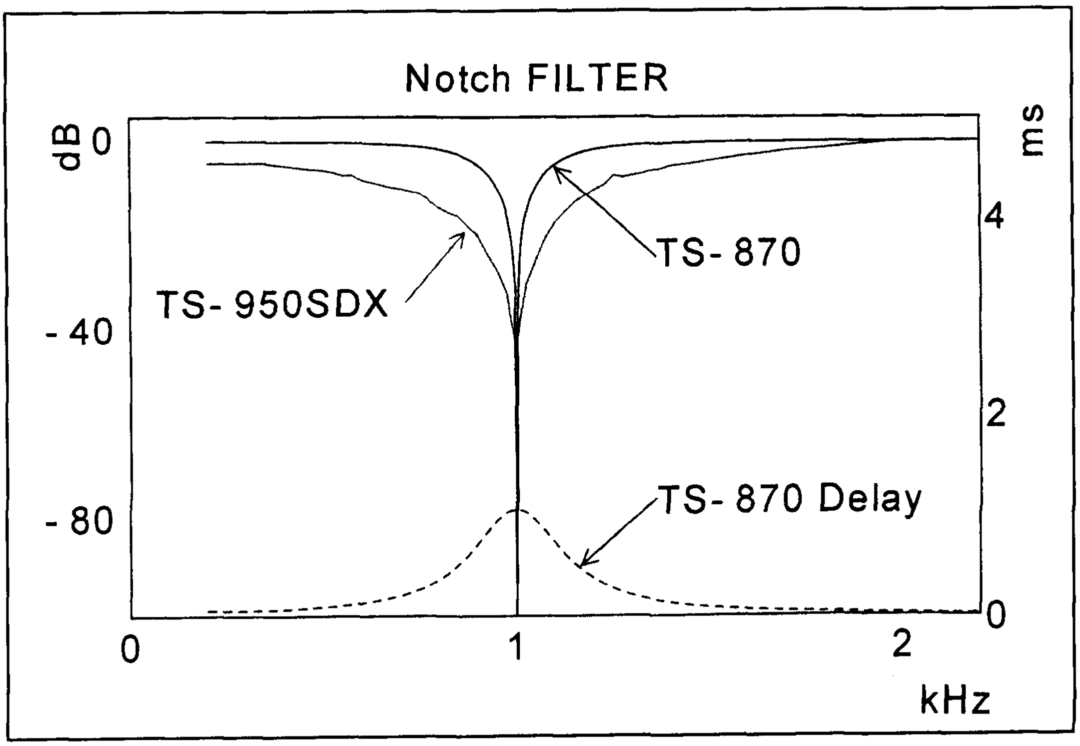

Figure 14. Automatic notch filter done in DSP. Can be done at IF (preferably) or at AF (typically). IF notch filter for multi-tones requires more computational power.

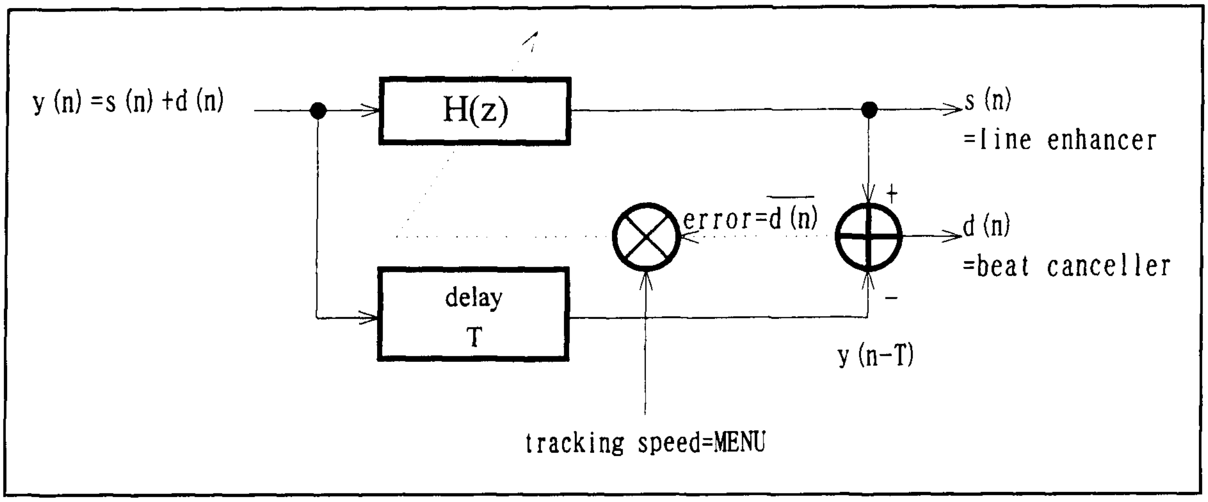

Figure 15. Block diagram of the adaptive filter used in the TS-870.

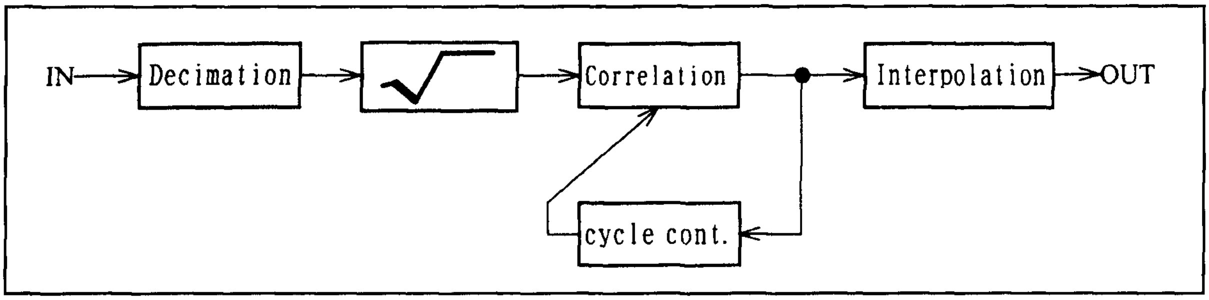

Figure 16. Block diagram of the correlated method used for noise improvement.

makes rapid contest exchanges impossible.

2. Spurious audio "tones" result when noisy signals are processed in some implementations. These appear as seemingly random beeps at random frequencies and are caused by the algorithm's imperfect ability to distinguish between signal and noise in the frequency domain.

3. Spectral subtraction requires much more DSP computing power than the LMS algorithm. All algorithms have their disadvantages; yet, under some conditions, spectral subtraction may provide the best performance. The JPS NIR-12 DSP, for example, provides *both* spectral subtraction and LMS noise reduction (which JPS refers to as *adaptive peaking*). The user can choose the best noise reduction method for each situation.

The above is a verbatim description as taken from **Reference 6**.

Noise blankers

Another useful application of DSP, although not really demonstrated in ham equipment, is noise blanking. Noise blanking is typically achieved by analyzing the incoming signal. If the rise or decay times are faster than either the human voice or transceiver switching, it is detected and the receiver is blanked during this time period.

Impulse noise blankers are based on the principle of opposite modulation. In effect, a stage in the signal path is modulated, so the signal path is blanked by an AM process for the duration of the interference. It is also possible to use an FM method in which the signal path is shifted to a different frequency range. The latter procedure[8] uses the attenuation overlap of IF filters in a double superheterodyne receiver. The second oscillator is swept several kilohertz from the nominal frequency for the duration of the interference, so the gain is reduced to the value of the ultimate selectivity in accordance with slope of the filter curves.

This method is especially advantageous as the switching spikes, which often accompany off-on modulation, should not be noticeable. However, when using a high-speed (wide bandwidth) FM modulator, components can appear within the second IF bandwidth from the modulation. The most stringent limitation of this method is the requirement for two identical narrowband filters at different frequencies along

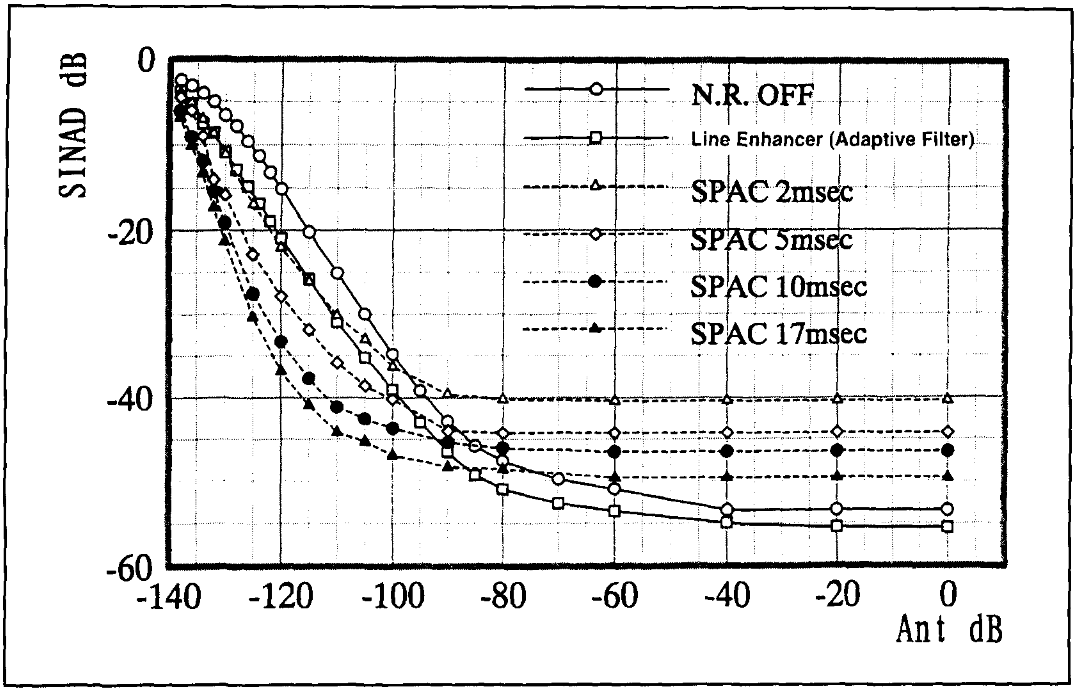

Figure 17. Signal-to-noise ratio as a function of the various adaptive filters or correlation match system.

with an intermediate mixer. Thus, the concept is limited to a double conversion superheterodyne receiver with variable first oscillator.

When using an AM method, two types of processing are possible:

1. The interference signal is tapped off in parallel at the input of the systems and increased to the trigger level of a blanker by an interference channel amplifier having a pass bandwidth that is far different from the signal path. A summary of such techniques is given in **Reference 9**. This method is effective only against very wideband interference because noticeable interference energy components must fall into the passband range to cause triggering. This method will not be effective in the case of narrowband interference, such as radar pulses, which are within or directly adjacent to the frequency range to be received.

2. The interference signal is tapped off from the required signal channel directly following the mixer.[10,11] It is then fed to a fixed-frequency second IF amplifier, where it is amplified up to the triggering level. Because there is danger of crosstalk from the interference channel, it is advisable to use a frequency conversion in the interference channel. Thus, interference amplification occurs at a different frequency than the signal IF. Attention must be paid when using this method to ensure that there are no switching spikes generated during the blanking process that can be fed back to the interference channel tap-off point. Otherwise there would be danger of pulse feedback. The return attenuation must, therefore, exceed the gain in the interference channel between the tapping point and the blanker.

The blanker must be placed ahead of the narrowest IF filter in the signal path. It must be able to blank before the larger components of the transient have passed this filter. We must assure a small group delay in the interference channel by using a sufficiently broad bandwidth and a minimum of resonant circuits. It is desirable to insert a delay between the tap-off point and the signal path blanker, so there is sufficient time for processing the interference signal. If this is done, it is not necessary to make the interference channel excessively wide, while still assuring the suppression of the residual peak.

Figure 18 is the block diagram of a superheterodyne receiver with this type of impulse noise blanker. **Figure 19** illustrates its operation in the presence of a strong interfering radar pulse. An essential part of the blanker is the use of a gate circuit that can operate linearly over a wide dynamic range. **Figure 20** shows such a gate, using multiple diodes. The circuit is driven by the monostable flip-flop, which is triggered by the noise channel.

Figure 21 is a schematic of a noise blanker circuit designed following these principles. When the noise channel is wider than the signal channel, this type of noise reducer can also have problems from the interfering signals in the adjacent channels.

In analyzing the recently published circuits

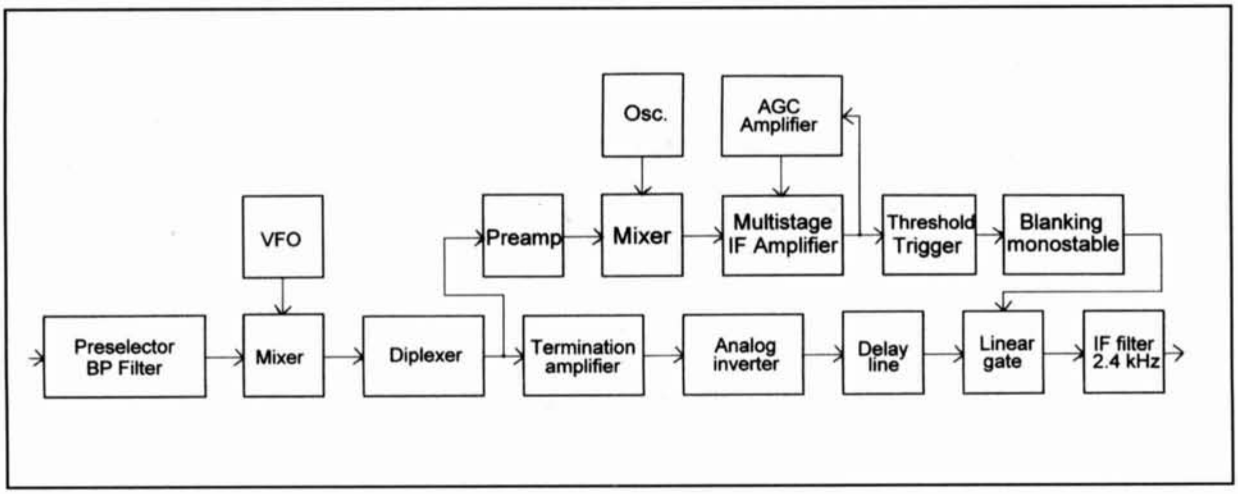

Figure 18. Block diagram of a superheterodyne receiver with blanker.

Table 2. Digital VLF-HF Receivers EK895/EK896.

Frequency range	10 kHz to 30 MHz	
Resolution	1 Hz	
Frequency drift	-10 to 45°C	aging/year
Frequency standard	$5x10^{-7}$	$1x10^{-6}$
Oven-controlled frequency standard	$1x10^{-7}$	$1x10^{-7}$
External frequency standard	1/5/10 MHz, 0.2 to 1 V_{RMS}	
Antenna input	BNC connector, 50 Ω	
VSWR	<3	
Max. input voltage (≤ 30 MHz)	100 V EMF	
Oscillator reradiation into 50-ohm termination	≤10 µV	
Demodulation modes	CW/MCW (A1A, A1B, A2A, A2B) FAX1 (F1C) AM/AME (A3E, H2A, H2B, H2E) USB/LSB (R2A, R3E, J2A, J3E) ISB (B8E) FSK/AFSK (F1A, F1B), F6 (F7B) FAX2 (F3C), FM (F3E) DATA LINK acc. to MIL STD 188-203-1A (on request)	
IF bandwidth in Hertz (standard values)		
	3 dB	60 dB
	+/-75	+/-150
	+/-150	+/-225
	+/-300	+/-430
	+/-500	+/-770
	+/-750	+/-990
	+/-1050	+/-1600

(Continued) →

	+/-1200	+/-1760
	+/-1350	+/-1900
	+/-1550	+/-2100
	+/-2000	+/-3400
	+/-2400	+/-3700
	+/-3000	+/-4200
	+/-4000	+/-5200
Quasicontinuous bandwidth	128 steps, 100 Hz to 8 kHz (optional)	
Sensitivity (for S/N=10dB, f=0.1 to 30 MHz)		
A1A (CW)	0.4 μV EMF (-121 dBm), BW=300 Hz	
J3E (SSB), J7B	1.0 μV EMF (-113 dBm), BW=2.7 kHz	
H3E (AME), 1 kHz, m=60%	2.7 μV EMF (-104 dBm), BW=6 kHz	
	with preamplifier, f=0.2 to 30 MHz	
A1A (CW)	0.2 μV EMF (-127) dBm), BW=300 Hz	
J3E (SSB), J7B	0.4 μV EMF (-121 dBm), BW=2.7 kHz	
H3E (AME), 1kHz, m=60%	1.0 μV EMF (-113 dBm), BW=6 kHz	
Immunity to interference, nonlinearities		
Intermodulation (1.5 to 30 MHz; $\Delta f \geq 30$ kHz; interfering signal 0 dBm)		
IP_2	>60 dBm (typ. 70 dBm)	
IP_3	>30 dBm (typ. 35 dBm)	
Crossmodulation (0.1 to 30 MHz, interfering signal 5 V EMF (+21 dBM); $\Delta f \geq 30$ kHz; m = 0.3; f= 1 kHz; signal level 10 mV EMF (-33 dBm)	≤1 dB signal attenuation	
Blocking (0.1 to 30 MHz); interfering signal 6.3 V EMF (+23 dB); $\Delta f \geq 30$ kHz; signal level 1 mV EMF (-53 dBm) m = 0.3; f= 1 kHz;	≥1 dB signal attenuation	
Desensitization (interfering signal 300 mV EMF; $\Delta f \geq 30$ kHz; signal level 30 μV EMF; bandwidth 3.1 kHz)	≥20 dB SINAD	
Inherent spurious signals (f>100 kHz)	<-113 dBm (nominal -124 dBm)	
Image frequency rejection	>90 dB	
IF rejection	>90 dB	
Weighted S/N ratio for 1 mV EMF	>46 dB SINAD	
Gain control	automatic (AGC), manual (MGC), or remote (DGC)	
AGC error	≤3 dB (1 μV to 1 V EMF)	

Current measurements show IP2 of more than 100 dBm and IP3 typically 42 dBm between 5 MHz and 20 MHz. It assumes the digital binary pre-selector (EK896 or XK2100)

and their transceivers, it becomes quite obvious that companies—for cost-saving reasons—are not going to the extreme in having two independent receivers. By analyzing the attack/decay times, a decision based upon this process, and gating the signal in particular, has been found to be a solution.

It is apparent that this process can be duplicated in DSP in the IF stage. The first true implementations of this technique are also

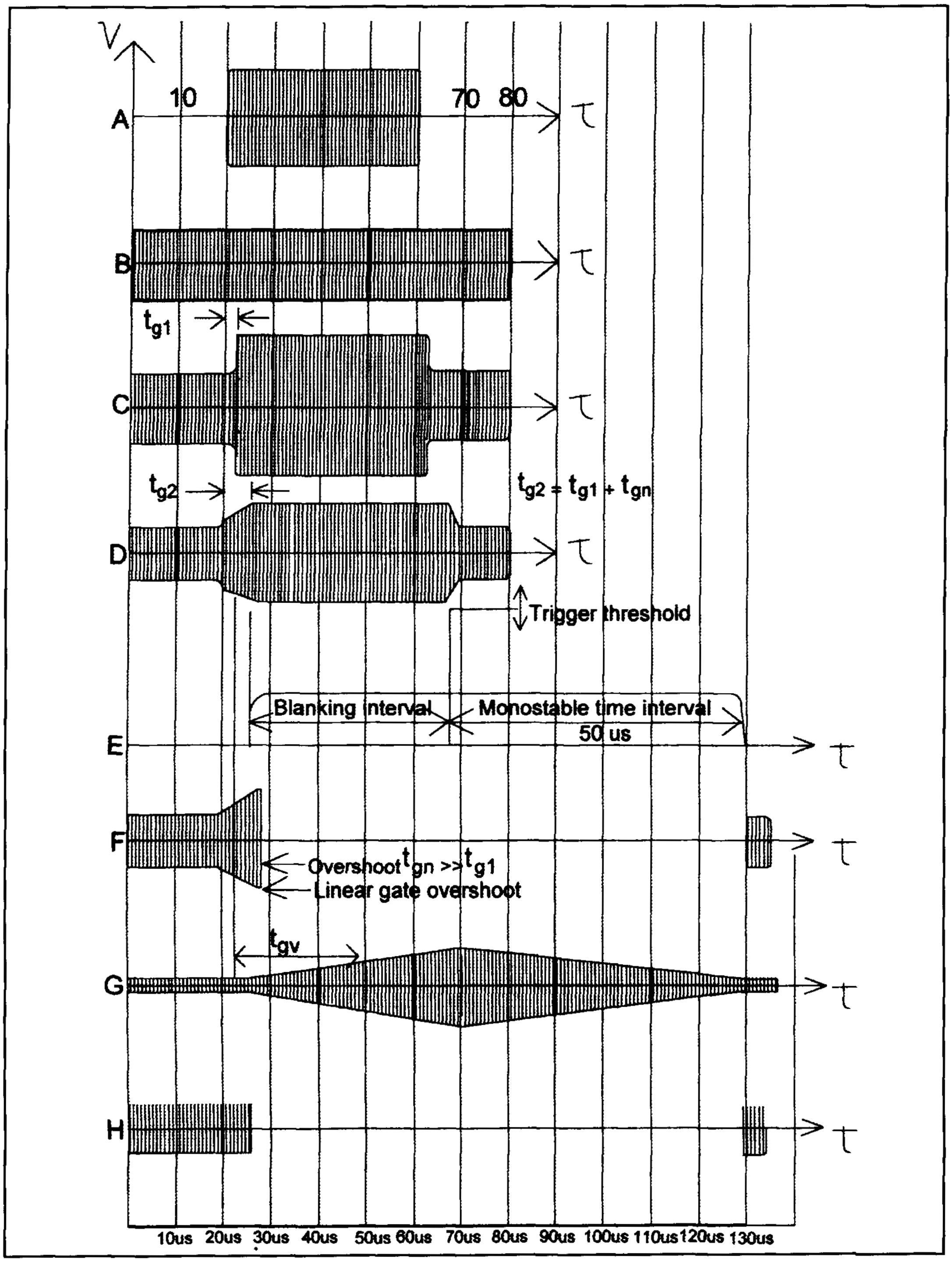

Figure 19. Waveform sketches illustration operation of noise blanker. (a) Interfering radar noise pulse 40 µs, (b) desired signal, (c) interference and signal after diplexer, (d) noise channel output signal, (e) blanking monostable output, (f) linear gate output, (g) delayed version of linear gate input signal, (h) delayed version of linear gate output signal at main channel.

found in the XK2100 and in the EK895/96. Research is currently underway to determine whether or not the attack/decay times can be evaluated based on some adaptive methods.

Table 2 shows the performance of a typical modern DSP-based VLF-HF receiver.

Summary

This short paper provides an overview regarding "*leftovers*" in the area of RF hardware problems and an insight into the use of DSP, both for filtering and noise cancellation.

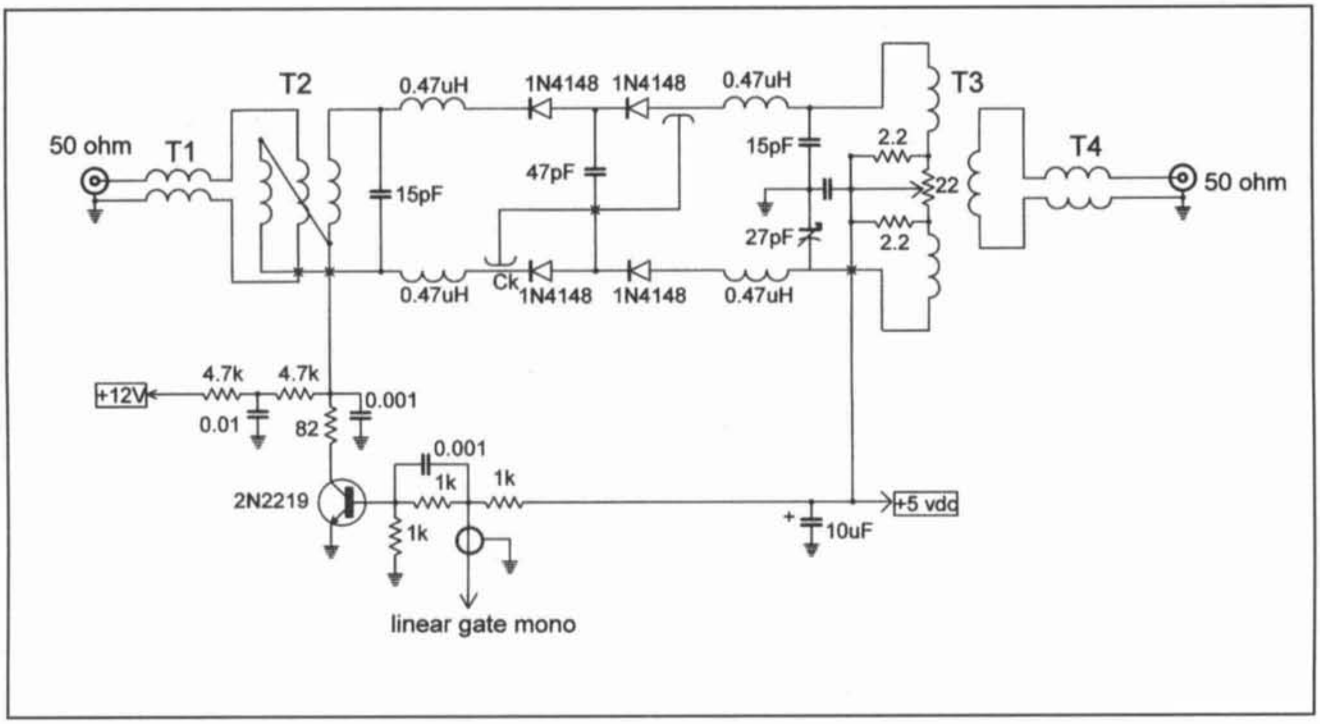

Figure 20. Schematic diagram of blanker gate with high dynamic range.

The current, most advanced of these units, which combines all the available techniques, is the Rohde & Schwarz XK2100 (see **Photo A**). As I write this, I have two mail boxes with such units installed in the United States and two in Germany, which are used for Pactor II, and take full advantage of all filtering. **Photo B** shows my Florida ham station at Marco Island,

Photo A. My ham station using both the analog (IC-781) and digital (XK2100) systems KA2WEU/4, Marco Island, Florida.

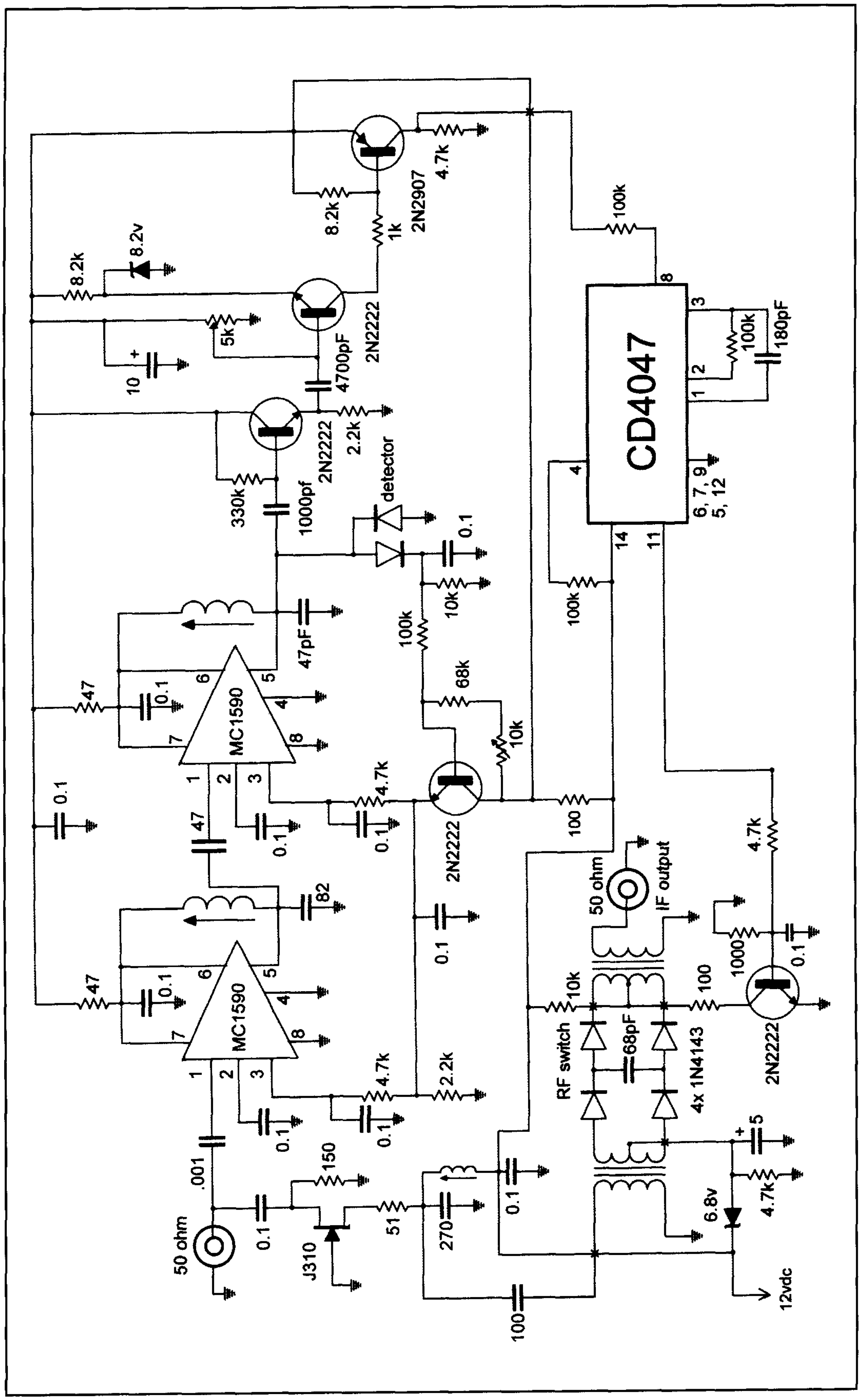

Figure 21. Schematic diagram of an analog noise blanker circuit.

Photo B. Eight-element, log-periodic antenna atop the Cap Marco Merida Condominium, Marco Island, Florida (160 feet or 50 meters above ground level). It is connect to ham station KA2WEU/4 located in the penthouse below.

using both the analog (IC-781) and digital (XK2100) systems. In **Photo C**, you see a 12-story building situated on the Gulf of Mexico on Marco Island, Florida, with an eight-element, log-periodic antenna sitting atop, which is connected to my ham station in the penthouse. The antenna is 160 feet or 50 meters above the Gulf of Mexico.

Acknowledgments

I am particularly grateful to Yukio Kawana, Chief Engineer of the Amateur Product Division, Kenwood Corporation, who provided me with intimate details regarding their system, and Department II of Rohde & Schwarz, RF Communications Division—in particular Messers. Korsmeier, Träger, Hackl, and Wachter. ■

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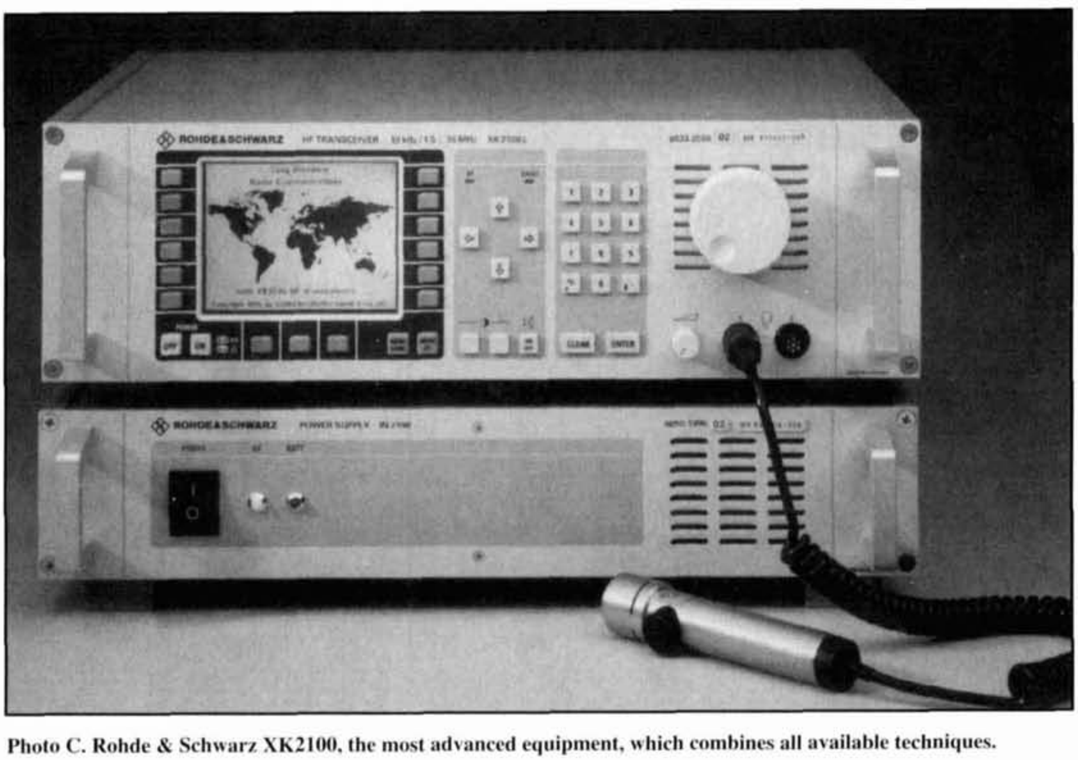

Photo C. Rohde & Schwarz XK2100, the most advanced equipment, which combines all available techniques.

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DIRECT DIGITAL SYNTHESIS

On a PC platform

The recent introduction of single-chip Direct Digital Synthesis (DDS) synthesizers has opened up this once complex technique to a broader segment of the amateur radio population. DDS chips make audio and radio frequency generation possible to resolutions better than one 2X 10^{-3} Hz and at frequencies approaching the Nyquist maximum of *fo*/2 or 25 MHz with a 50-MHz clock.

The unit described here is designed around the Analog Devices AD7008 and was built on an IBM AT format printed circuit card (ISA bus) shown in **Photo A**. The synthesizer card will operate in any properly designed ISA bus computer with a vacant, full-length, 8-bit slot. All power for the synthesizer is derived from the host PC. A stand-alone microcontroller bus interface is included in the board's design should you want to incorporate the DDS unit into a stand-alone, non-PC application.

Objectives

The original objective was to design, construct, program, and implement a low-cost signal generator for use in a commercial six-tone multi-frequency shift-keyed data encoder. However, the finished product has many other uses, such as:

- signal generator from 0.01 Hz to Nyquist maximum,
- multi-octave sweep signal generator,
- phase contiguous FSK generator,
- radio frequency VFO to control older transmitters, receivers, and transceivers,

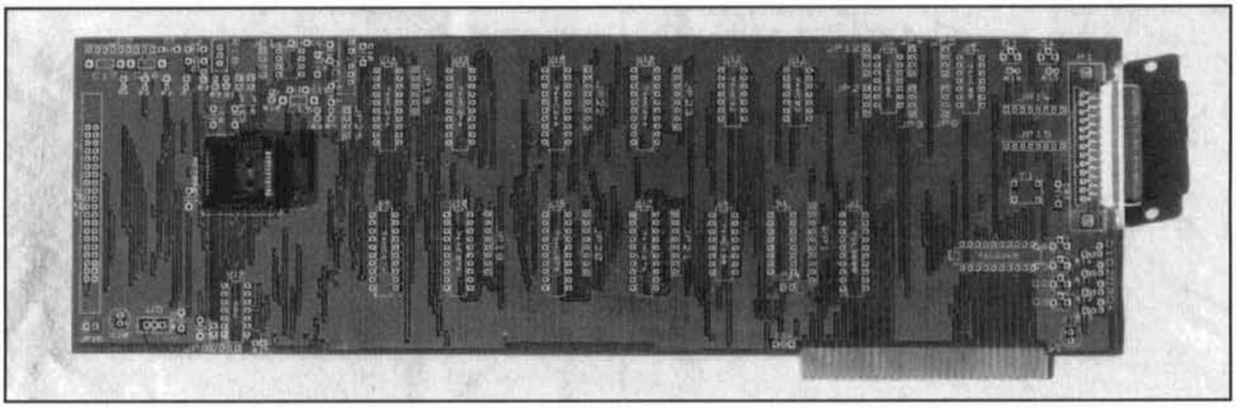
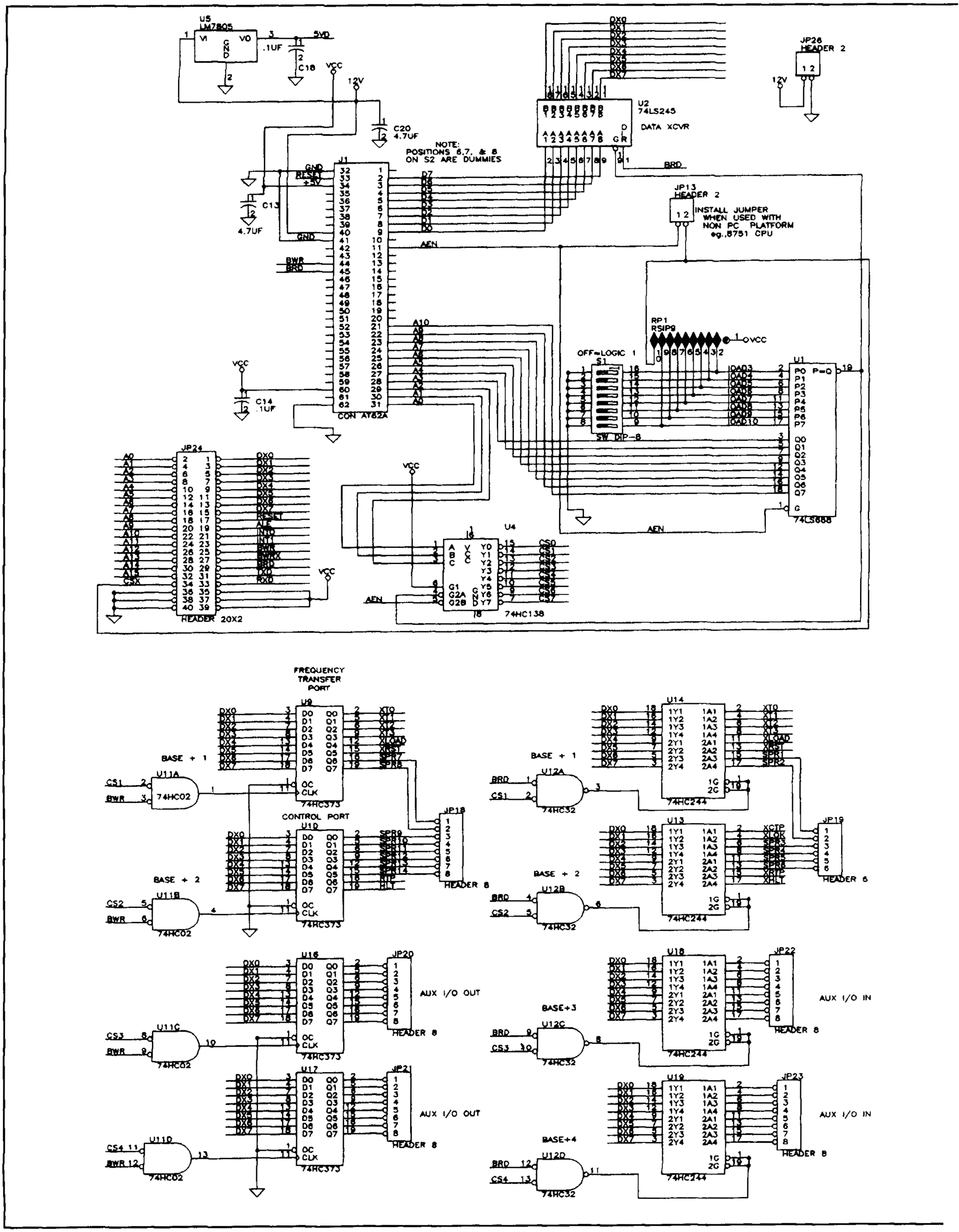


Photo A. Bare board with reference parts location.


U5
LM7805
C18
C20
4.7UF
NOTE:
POSITIONS 6,7, & 8
ON S2 ARE DUMMIES
J1
CON AT62A
U2
74LS245
DATA XCVR
JP26
HEADER 2
JP13
HEADER 2
INSTALL JUMPER
WHEN USED WITH
NON PC PLATFORM
eg.,8751 CPU
RP1
RSIP9
OFF=LOGIC 1
S1
SW DIP-8
U1
74LS688
C13
4.7UF
C14
.1UF
JP24
HEADER 20X2
U4
74HC138
FREQUENCY
TRANSFER
PORT
U9
74HC373
BASE + 1
U11A
74HC02
CONTROL PORT
U10
74HC373
BASE + 2
U11B
74HC02
JP18
HEADER 8
U14
74HC244
U12A
74HC32
U13
74HC244
U12B
74HC32
JP19
HEADER 6
U16
74HC373
JP20
AUX I/O OUT
HEADER 8
U11C
74HC02
U17
74HC373
JP21
AUX I/O OUT
HEADER 8
U11D
74HC02
U18
74HC244
JP22
AUX I/O IN
HEADER 8
BASE+3
U12C
74HC32
U19
74HC244
JP23
AUX I/O IN
HEADER 8
BASE+4
U12D
74HC32

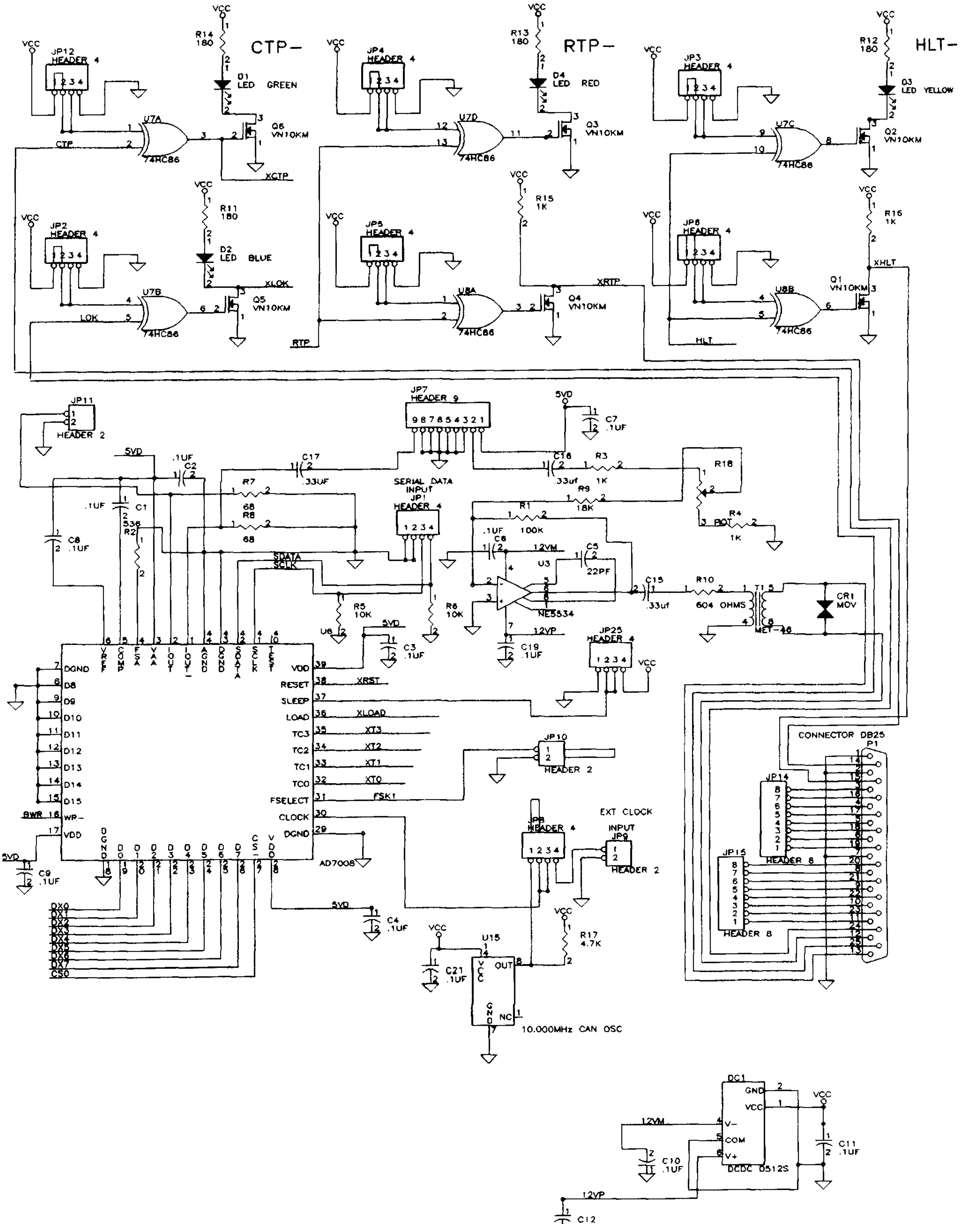


Figure 1. The schematic diagram.

1	I OUT--	12	D12	23	D4	34	TC2
2	IOUT	13	D13	24	D5	35	TC3
3	V_{AA}	14	D14	25	D6	36	LOAD
4	FS ADJUST	15	D15	26	D7	37	SLEEP
5	COMP	16	WR--	27	CS--	38	RESET
6	V_{REF}	17	V_{DD}	28	V_{DD}	39	V_{DD}
7	DGND	18	DGND	29	DGND	40	TEST
8	D8	19	D0	30	CLOCK	41	SCLKA
9	D9	20	D1	31	FSELECT	42	SDAT
10	D10	21	D2	32	TC0	43	DGND
11	D11	22	D3	33	TC1	44	AGND

Figure 2. AD7008 PLCC pin definitions. Taken from Analog Devices Application note C1791-18-4/93 (Rev 0) page 4.

- complex waveform generator capable of concurrent amplitude, frequency, and quadrature modulation via computer control,
- moderate noise component local oscillator for new radio designs,
- platform for DDS software development to support future, stand-alone DDS projects,
- primary delta reference source for low-noise phase lock loop (PLL) systems,
- nearly unlimited programmed frequency signal source for receivers, transmitters, and transceivers, and
- automated signal generator for bench testing.

Additional features

The board contains additional features, which ease the integration of the DDS function with external applications (see the schematic in **Figure 1**). These include:

- three general purpose TLL-compatible 8-bit output ports,
- three general purpose TLL-compatible 8-bit input ports,
- onboard crystal reference oscillator for non-critical DDS applications,
- general purpose line amplifier pad-out with isolated DC-DC converter power to minimize PC power bus noise contribution to the unit's signal-to-noise budget,
- generic passive filter pad-out area,
- a generic microcontroller interface connector for stand-alone applications,
- status LEDs for software debugging,
- standard DB-25 connector for both DDS signal output and selected bit level I/O,
- external reference clock selection, and
- Bit Serial interface to DDS for dedicated controller software development and testing.

The Analog Devices AD7008 synthesizer chip

Analog Devices introduced their 7008 single DDS synthesizer chip in 1994. This chip was a first in that all components for accepting binary frequency values and generating sinewave signals were cast into a single plastic package (see **Figure 2** and **Photo B**). You need only send a few bits of mode and control information to the chip followed by a 32-bit phase accumulator value to generate a discrete sinewave signal. Calculation of the phase accumulator value and the actual frequency of the output signal is based on the formula:

fclock * fo/2x10E32 **(1)**

where *fclock* is the reference oscillator, and *fo* is the desired output frequency. The result of this calculation is a 32-bit binary value sent byte-sequentially to the AD7008 data port address. The AD7008 is composed of the following functional areas (see **Figure 3**):

- control bit interface logic block,
- data bus logic block,
- dual phase accumulator registers,
- command and mode resisters,
- special function and modulation registers I and Q,
- sequence logic,
- sine ROM,
- digital-to-analog converter,
- gain control block, and
- serial data mode and frequency set interface logic.

How does it work?

Direct digital synthesis is predicated on several assumptions: the first is that any alternating current signal can be represented by a minimum of two waveform samples per signal period (the Nyquist sample minimum). The more bits that can be developed per signal period, the better the representation of the desired waveform prior to any low-pass filtering.

The DDS system takes advantage of Nyquist mathematics and produces accurate waveforms by representing the desired sinewave signal with a binary sample quantity of 10 bits. Close observation of the waveform coming from the unfiltered output shows tiny steps in amplitude along the time axis. The output waveform shape is determined by the device's lookup ROM table. In the AD7008, the ROM table contains binary values that represent a sinewave function. Therefore, as the phase accumulator transfers its contents to the address bus of the sine ROM, the ROM output binary value drives an on-chip digital-to-analog converter. This, in turn, produces a stepped sinewave signal with step intervals equal to the step value in the phase accumulator.

How is the unit put together?

Analog Devices has eliminated most of the guesswork by integrating the entire process into a functional block. You must, however, exercise some care in circuit layout and power decoupling to minimize the effects of external noise sources. To this end, the circuit board uses under-chip decoupling capacitors or integrated socket-capacitors wherever possible. A completed board appears in **Photo C**.

The dilemma of analog and digital signal grounds is minimized via the use of large copper pour zones around all logic areas and onboard analog functions. Primary power distribution on the board also takes advantage of copper pour zones where routing permits. Power from the PC bus connector is either decoupled or post regulated with three terminal regulators. Where low noise requirements must be met, an optional isolated DC-DC inverter module can be installed to produce the ±12 volts DC sources for the onboard post amplifier.

The DDS chip mounts in a 44-pin Plastic Leaded Chip Carrier (PLCC) socket. The remaining integrated circuits can be soldered directly onto the board, but under-chip bypass capacitors must be used to minimize digital noise on the board's power distribution bus. Sockets with built-in bypass capacitors should be of the milled pin variety to ensure the unit's long-term reliability. The design, however, is amenable to hand wiring, as the unit was initially breadboarded on an AT protoboard and was operated without any noticeable instability or noise problems.

Connecting and communicating with the PC

The PC interface is from an Intel applications note (see **Figure 4**). Data to and from the board's assets are buffered to the AT bus via a 74LS245 bidirectional bus transceiver. An 8-bit board address comparator, 74LS688 compares a switch pack for a card base address (block of 8) and enables the card's various I/O units when satisfied. A 74HC138 decodes the lower three bits of the address bus and provides unique chip select signals for the AD7008 and auxiliary input/output port logic. Additional nand/nor logic is used to generate the final I/O strobes to the 74HC373 output ports and 74HC244 input ports.

How are connections made to the unit from the outside?

Primary DDS output signals are brought off the printed circuit card through a right-angle DB-25 connector (see P1 in **Photo A**). Auxiliary digital input and output ports, along with

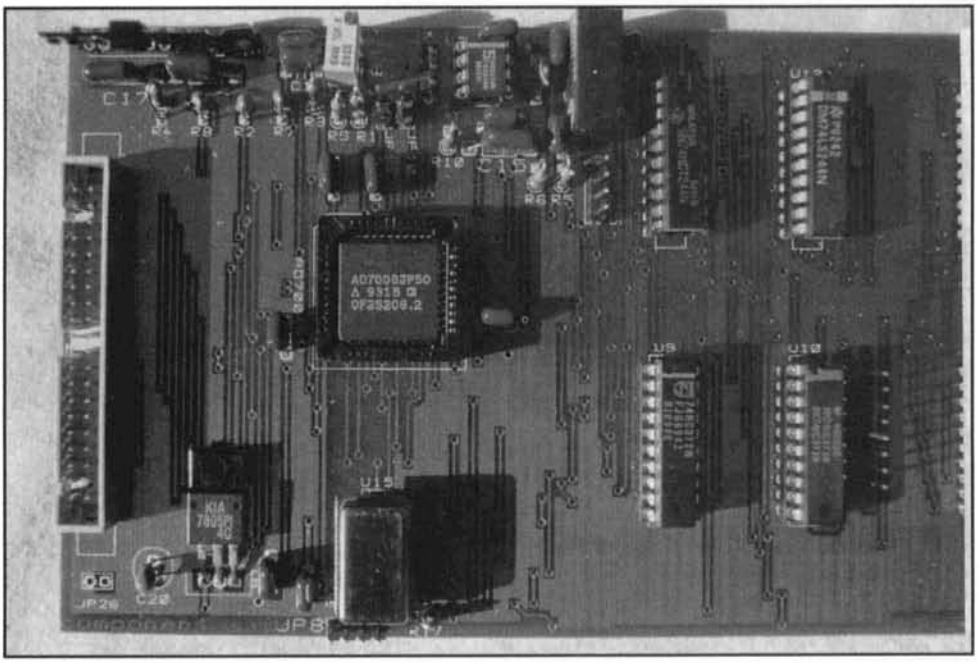


Photo B. The heart of the DDS board. Note the AD7008 mounted in a PLCC socket.

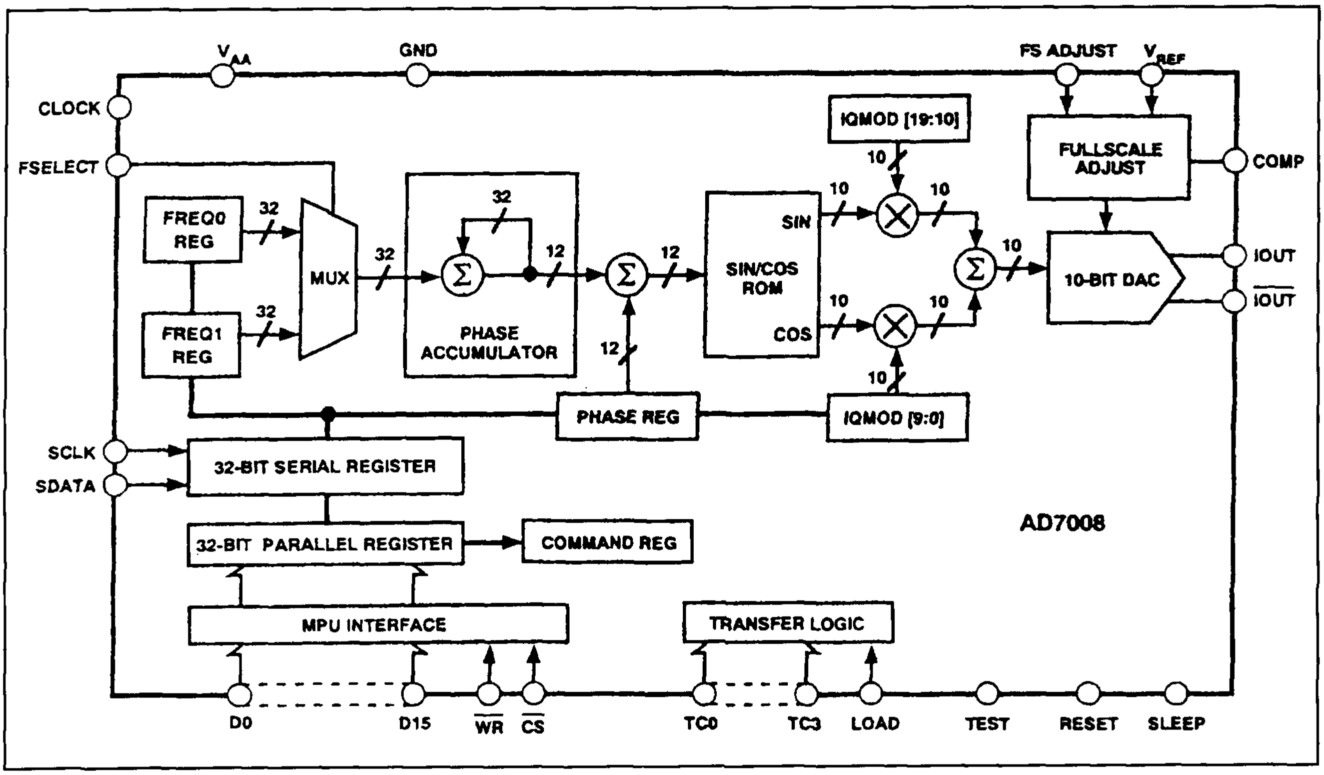


Figure 3. AD7008 functional block diagram. From Analog Devices Data Applications note C1791-18-4/93 (Rev 0).

optional reference clock signaling, are brought off the card via single-in-line-square post headers. Onboard exclusive OR gates and power MOSFET drivers have been incorporated into selected output control port pins to provide direct relay coil drive (less than 30 volts DC) and for software-independent configuration of bit logic levels. You must, however, provide back EMF spike diodes across any driven relay coil to prevent damage to the driver device.

A complete microcontroller bus connector is available for your dedicated controller applications. The data bus, address bus, memory read/write, and auxiliary control signals are patterned after the Intel 8051 microcontroller. The interface, however, is generic in that a number of different microcontroller chips could be adapted to drive the DDS chip as well as the general purpose I/O ports (see **Figure 5**).

Resolution versus accuracy

The onboard crystal oscillator may be bypassed in favor of an external clock source. The external clock signal must conform to standard TTL levels. The maximum external clock frequency is 50 MHz. The onboard crystal oscillator is an integrated, metal-can crystal oscillator assembly (U15 in **Photo B**). For most noncritical applications, the simple onboard oscillator will do quite well. In moderately stable temperature environments, the absolute frequency of the onboard crystal oscillator can be measured with an accurate frequency counter. That measured frequency can be inserted into the phase assimilator calculation and can correct, in software, any firm error attributable to the reference oscillator—a software derived free lunch.

How is the unit calibrated?

A principal factor to consider in the quest for the last digit of accuracy is the dilemma of finding an accurate calibration source. The most common frequency calibration sources are the National Institute of Standards and Technology (NIST) high-frequency broadcasts via radio station WWV. The good news is that high-frequency broadcasts from WWV on 2.5, 5, 10, 15, and 20 MHz can be received by almost any inexpensive shortwave receiver. A simple zero-beating of the DDS output at any of these frequencies will facilitate calibration. The bad news is that errors introduced by high-frequency propagation anomalies reduce WWV high-frequency accuracy to approximately 0.1 parts per million. This will lead to an error of approximately ±2.5 Hz at the DDS maximum output frequency of 25 MHz (50-MHz reference clock assumed). Sixty kilohertz broadcasts from WWV may be used to enhance the accuracy of the calibration process, but noise-free reception in many areas of the country is often problematic.

On the other hand, high-quality frequency counters can provide accuracies approaching a few parts per 100 million. Still, this degree of accuracy is only obtainable if the frequency counter has been calibrated against either a primary source or a recently calibrated transfer standard. For many radio amateur high-frequency applications and VFO substitutions, an accuracy of a few parts in 10 million will usually suffice.

How pure is the DDS signal?

The primary spurious components in the DDS process are alias signals. The alias derivation process can lead to some extended calculations and a modest amount of hair pulling. But, in its simplest form, the effects of alias signals can be minimized if DDS signals are not generated at, or even near, the theoretical Nyquist maximum of *fo/2*.

A rule of thumb suggests that the maximum DDS signal frequency should not exceed one third of the reference clock. This would permit signal generation up to 16.65 MHz with a 50-MHz reference clock. The addition of brick-wall low-pass filters to the DDS may permit the generation of signals beyond the one third guideline; however, the incremental increase in frequency coverage may be offset by the filter's implementation cost. Passing the DDS signal through a modest LC low-pass filter will reduce alias signals and spurious noise by approximately 60 to 70 dbsr. This level of purity is satisfactory for signal generators, sweep generators, and most transmitting applications; but close-in spurious noise or birdies are strong enough to limit the use of a DDS system as a local oscillator in high-performance receiver designs. There is, however, a mechanism that will minimize alias problems and, at the same time, mitigate phase noise common to simple PLL signal generation.

Combining DDS and PLL to minimize alias and phase noise components

The fundamental flaw in simple PLL systems is that a small frequency step puts a strong demand on the filter associated with the PLL comparator error signal. If the filter time constants are large enough to smooth out the error ripple, the response time to make a frequency step will be too long to be practical. If the loop time constant is made short enough to facilitate a reasonable response time to frequency change, the residual ripple on the error signal will cause the voltage-controlled oscillator (VCO) to produce numerous close-in sidebands—commonly referred to as phase noise. In a receiver mixer, the phase noise acts like a multitude of secondary local oscillators resulting in what would have been out-of-band signals appearing as increased noise in the desired receiver passband.

Some PLL designs incorporate VCOs that operate at 10 to 100 times the desired frequency to produce a larger frequency step increment, thereby minimizing the phase noise near *fo*. The VCO signal is then divided or heterodyned down to the desired frequency. The process works, but the added complexity in both analog and digital circuitry is costly.

The dilemma of PLL time constants, spectral purity, and loop response times can be mitigated by inserting the output of a DDS generator in place of the PLL fixed reference. The phase comparison is now performed with signals in the RF range, rather than signals in the near subaudible. The VCO will still respond to the PLL comparator error signal, but, because the comparison is made at frequencies in the kilohertz or megahertz range, the error loop filters can be extremely sharp, with no noticeable response delays.

The alias problem is also mitigated because the VCO would normally run at 10 or even 100 times the DDS frequency. Therefore, a spectrally pure DDS signal ranging from 3 to 6 MHz could control a VCO running in the 30 to 60 MHz range and perform the local oscillator function for an upconverted superheterodyne receiver. The upconversion scheme would also enhance image rejection. The DDS, in combination with a simple but well designed PLL, would provide the following:

- frequency resolution to less than 1 Hz at 60 MHz,

2	**Data 7**	**22**	**Address 9**	**32**	**GROUND**
3	**Data 6**	**23**	**Address 8**	**33**	**RESET**
4	**Data 5**	**24**	**Address 7**	**40**	**+12v**
5	**Data 4**	**25**	**Address 6**	**41**	**GROUND**
6	**Data 3**	**26**	**Address 5**	**44**	**Bwrite**
7	**Data 2**	**27**	**Address 4**	**45**	**Bread**
8	**Data 1**	**28**	**Address 3**	**60**	**VCC**
9	**Data 0**	**29**	**Address 2**	**62**	**GROUND**
11	**AEN-notdma**	**30**	**Address 1**		
21	**Address 10**	**31**	**Address 0**		

Figure 4. Applicable AT BUS pin definitions.

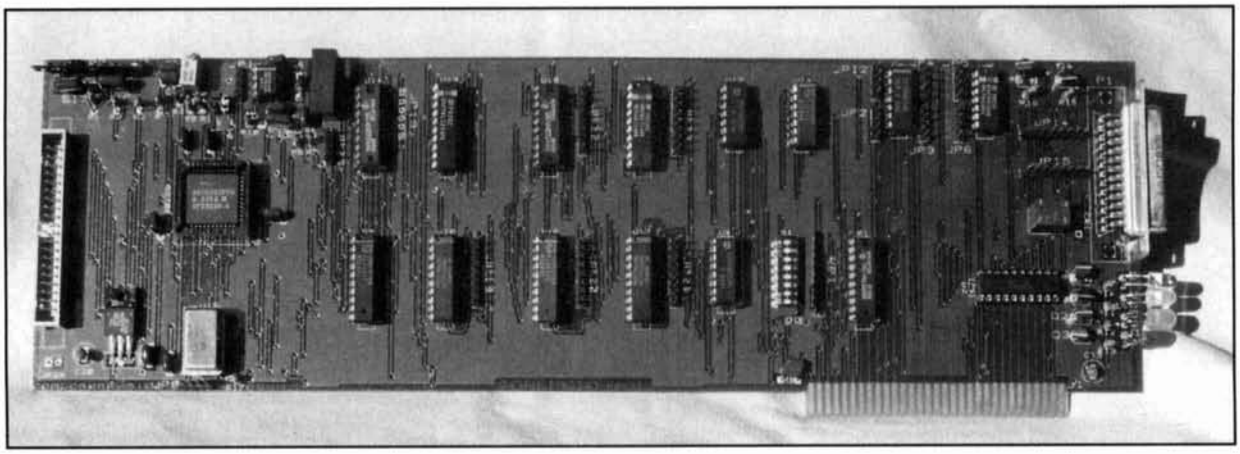


Photo C. The fully stuffed board.

- RF generation without the penalty of significant alias signals or close-in phase noise,
- frequency stability determined mainly by the DDS reference clock,
- frequency accuracy determined by the reference clock, but correctable in software,
- automated frequency setting versus time and event,
- nearly unlimited frequency memories,
- candidate for frequency hopper spread-spectrum local oscillators, and
- remote control of radio system's frequency via computer data link.

Software requirements

Software development may be accomplished using a variety of PC-based program languages, including: Borland Turbo C®, GWBASIC®, or Assembly Language. Test software referenced in this article was developed with Borland Turbo C.

Talking to the AD7008 internals

Communication with the AD7008 internals can be done in a 8/16 bit parallel mode or clocked bit-serial. The 8-bit paralleled mode was chosen over the simpler clocked bit-serial to ensure rapid frequency and modulation updates in future applications. The clocked bit-serial mode requires that all data (32 bits) and some control information be shifted into the device with every frequency change.

The parallel loading process is accomplished in four PC I/O write cycles (see **Figure 6**). Eight-bit parallel data was chosen over the 16-bit option to maintain compatibility with early 8088-based personal computers. The software listing references all applicable control and data

1	**DX0 (DATA)**	**11**	**DX5**	**21**	**INT0**	**31**	**TXD**
2	**A0 (ADDRESS**	**12**	**A5**	**22**	**A10**	**32**	**A15**
3	**DX1 (data)**	**13**	**DX6**	**23**	**INT1**	**33**	**RXD**
4	**A1**	**14**	**A6**	**24**	**A11**	**34**	**CHIP SELX**
5	**DX2**	**15**	**DX7**	**25**	**BWR (WRITE)**	**35**	**VCC**
6	**A2**	**16**	**A7**	**26**	**A12**	**36**	**GROUND**
7	**DX3**	**17**	**RESET**	**27**	**BWRX(SPEC)**	**37**	**VCC**
8	**A3**	**18**	**A8**	**28**	**A13**	**38**	**GROUND**
9	**DX4**	**19**	**ALE**	**29**	**BRD (READ)**	**39**	**VCC**
10	**A4**	**20**	**A9**	**30**	**A14**	**40**	**GROUND**

Figure 5. Microcontroller bus definition. Notes: (1) BWRX is a protected write from microcontroller, (2) CHIP SELX is a predecoded chip select, (3) TXD is microcontroller UART transmit, and (4) RXD is microcontroller UART receive.

<----------------32-Bit Parallel Assembly Registry---------------->				
			A BYTE	D7-D0 <<A BYTE
		A BYTE	B BYTE	D7-D0 <<B BYTE
	A BYTE	B BYTE	C BYTE	D7-D0 <<C BYTE
A BYTE	B BYTE	C BYTE	D BYTE	D7-D0 <<D BYTE

Figure 6. Eight-bit parallel loading sequence. Taken from Analog Devices Application note C1791-18-4/93 (Rev 0) page 4.

registers in the AD7008 (**Figures 7, 8,** and **9**). Complex modulation modes are addressed in the Analog Devices data sheet, which can be downloaded from the Analog Devices Web Server on the Internet.

Driving the DDS board from the PC keyboard

The test program, DDS.EXE, was written by David Sipe, KD6QFZ (see **Listing 1**). It may be used freely, in whole or part, by anyone who wishes to do so. No warranty is expressed or implied. Use at your own risk. Files included in the archive are:

DDS.C—The C source code. This was compiled using Borland C++v3.1. It will also compile under Borland C v2.0 without modification. All code is contained in this file. Only the header and library files supplied with the above mentioned compilers are needed with the source file for a successful compile.

DDS.EXE—The DOS executable file has been compiled using the small memory model, but should compile in any other memory model without modification.

DDS.TXT—This is a document file.

Program information and default values

- Output frequency *(f0) = 0,*
- Source clock *(fs) = 50 MHz* on startup unless other specified on command line.
- This value was selected because it didn't cause a conflict with cards in my computer. This may not be true of your machine,
- Step = 1 Hz on startup unless specified on command line,
- Frequency steps are 1 Hz, 5 Hz, 10 Hz, 25 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz, and
- Desired output frequency should not exceed *fs/3* and is limited to *fs/2*.

Command line parameters

- C<frequency in Hz> specifies *fs* other than default,
- P<portbase>portbase = a hex value to use other than default portbase of 240h,
- S<frequency in Hz> specified starting value for step other than the default must be a value listed above, and
- Note that command line parameters are NOT case sensitive.
  Example: dds c32000000 p248 s25

This specifies a source clock of 32 MHz at a portbase address of 248h. The initial step value is 25 Hz.

Menu options

- UpArrow—Increments *fo* by the step value,
- DownArrow—Decrements *fo* by the step value.

Source Reg.	TC3-TC2		Dest. Reg.	TC1 TC0
Parallel Assembly Reg	0 0	Transfer Parallel Assembly Reg. to Command Reg	Freq 0 Reg	0 0
Parallel Assembly Reg	1 0	Transfer Parallel Assembly Reg. to Selected Dest Reg	Freq 1 Reg.	0 1
Serial Assembly Reg.	1 1	Transfer Serial Assembly Reg to Selected Dest. Reg	Phase Reg.	1 0
			I Q Mod Reg	1 1

Figure 7. Source and destination registers. From Analog Devices Application note C1791-18-4/93 (Rev 0) page 6.

```
/* Test code for AD7008 DDS

Source clock (Fs) = defaults to 50 Mhz on startup unless specified on command line

Portbase = defaults to 240h on startup unless specified on command line

Step = defaults to 1 Hz on startup unless specified on command line. Selectable frequency Steps
are 1Hz, 5Hz, 10Hz, 25Hz, 100Hz, 1KHz, 10KHz, 100KHz, and 1MHz.

Desired output Frequency (Fo) should not exceed Fs/3, and is limited to Fs/2.

Command line parameters:
      C<freqency in Hz> specifies Fs other than default
      P<portbase> specified as a hex value to use other than default portbase of 240h
      S<freqency in Hz> specified starting value for step other than the default. Must be a value
      listed above. If not, the next lower value will be substitued.

Program menu options:
UpArrow     - Increments Fo by the step value
DownArrow   - Decrements Fo by the step value
PageUp      - Increments Fs by the step value
PageDown    - Decrements Fs by the step value
LeftArrow   - Decrements the step value to the next lower value
RightArrow  - Increments the step value to the next higher value
Home        - Sends the most recent Fo to the DDS
End         - Sends Fo = 0 Hz to the DDS
Del         - Resets the DDS
F1          - Increments the portbase by 8
F2          - Decrements the portbase by 8
F3          - Toggles the Red LED On/Off
F4          - Toggles the Yellow LED On/Off
*/
/* Includes*/
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <conio.h>
#include <dos.h>
/* General programs */
#define EVER        ;;
#define MAXCLOCK    51000000.0
#define DEFCLOCK    50000000.0
#define NUMSTEPS    9   /* max number of selectable step frequencies */
/* Keyboard return codes */
#define ESC         0x1b
#define ENTER       0x0d
#define UPARROW     0x4800
#define DOWNARROW   0x5000
#define LEFTARROW   0x4b00
#define RIGHTARROW  0x4d00
#define PGUP        0x4900
#define PGDN        0x5100
#define HOME        0x4700
#define END         0x4f00
#define INSERT      0x5200
#define DEL         0x5300
#define PLUS        0x2b
#define MINUS       0x2d
#define STAR        0x2a
#define SLASH       0x2f
```

```
#define F1          0x3b00
#define F2          0x3c00
#define F3          0x3d00
#define F4          0x3e00
#define F5          0x3f00
#define F6          0x4000
#define F7          0x4100
#define F8          0x4200
#define F9          0x4300
#define F10         0x4400
/* Port addresses */
#define ASMREG      0x240
/* Command stobes */
#define RESET       0x20
#define LOAD        0x10
/* Control bits */
#define TC0         0x01
#define TC1         0x02
#define TC2         0x04
#define TC3         0x08
/* Destination Registers */
#define FREQ0       0x00
#define FREQ1       0x01
#define PHASE       0x02
#define IQMOD       0x03
/* Source Registers */
#define PAR2CMD     0x00
#define PAR         0x08
#define SAR         0x0c
/* Lights */
#define RED         0x40
#define YEL         0x80
/* Function prototypes */
void cmdline(int ac,char *av[]);
unsigned int getkey(void);
unsigned long calc_ph_acc(unsigned long f);
void write_phaseaccum(unsigned long ph_acc,int dest);
void reset_dds(void);
void xfer(int dest);
void lights(int cmd);
/* Global Variables modified dymamically during program execution */
unsigned long step;             /* the frequency change step in Hz */
int stepnum = 0;                /* step pointer */
unsigned long freq = 0L;        /* the output freqency in Hz */
unsigned long phaseaccum = 0L;  /* 32bit phase accumulator value sent to DDS */
/* global variables modified either from command line or interactively */
double fclock = DEFCLOCK;       /* source fclock frequency */
/* port addresses for DDS board */
unsigned par = ASMREG;          /* parallel assembly register */
unsigned control = ASMREG + 1;  /* tranfer and control register */
unsigned aux1 = ASMREG + 2;     /* auxilliary control register #1 - lights */
unsigned aux2 = ASMREG + 3;     /* auxilliary control register #2 */
unsigned aux3 = ASMREG + 4;     /* auxilliary control register #3 */
/* global variable used as constants */
unsigned long steplist[NUMSTEPS]={ 1L,5L,10L,25L,100L,1000L,10000L,100000L,1000000L };
double twoto32nd = 4294967296.0;;
void main(int ac,char *av[])    /* will add command line parms later */
{
  unsigned long f;
  unsigned ch;
  int i,t;
```

```
double tclock;
step = steplist[stepnum];  /* initial step */
/*init();*/ /* set all variables to default values */
if(ac > 1)  /* if any command line parameters, use them */
cmdline(ac,av); /* parse and decode command line */
clrscr();
for(EVER)
{
 gotoxy(1,1);
 clreol();
 printf("Output Frequency = %ld     Freqency Step = %ld\n",freq,step);
 clreol();
 printf("PortBase = %Xh    Source Clock = %1.1f\n",par,fclock);
 printf("\nLEFT and RIGHT arrows adjust Step,\n");
 printf("UP and DOWN arrows adjust Freq by step\n");
 printf("PGUP & PGDN adjust Clock by step\n");
 printf("HOME - Send most current Freq\n");
 printf("END - Stop Freq output\n");
 printf("DEL - Reset DDS\n");
 printf("F1 - Increment portbase address by 8\n");
 printf("F2 - Decrement portbase address by 8\n");
 printf("F3 - Toggle RED led\n");
 printf("F4 - Toggle YELLOW led\n");
 printf("ESC - Exit program\n");
 ch = getkey();
 switch(ch) /* Selects user function by keypress */
 {
  case RIGHTARROW:  /* increment step */
   if(++stepnum < NUMSTEPS) /* still in range? */
    step = steplist[stepnum]; /* set the new step value */
   else
    stepnum—; /* else restore step pointer */
   break;
  case LEFTARROW:  /* decrement step */
   if(—stepnum >= 0) /* still in range? */
    step = steplist[stepnum]; /* set the new step value */
   else
    stepnum++; /* else restore step pointer */
   break;
  case UPARROW:  /* increment freq by step */
   f = freq + step;
   if(f <= fclock/2L)  /* Not > fclock/2, else do nothing */
   {
    freq = f; /* save the new frequency */
    phaseaccum = calc_ph_acc(freq);
    write_phaseaccum(phaseaccum,FREQ0);
   }
   break;
  case DOWNARROW:  /* decrement freq by step */
   if(freq >= step)  /* must have room to dec, else do nothing */
   {
    freq -= step; /* update to the new frequency */
    phaseaccum = calc_ph_acc(freq);
    write_phaseaccum(phaseaccum,FREQ0);
   }
   break;
  case PGUP:  /* increment clock by step */
   tclock = fclock + (double)step;
   if(tclock < MAXCLOCK)
    fclock = tclock;
   break;
```

```
      case PGDN:  /* decrement clock by step */
        tclock = fclock - (double)step;
        if(tclock >= 0.0)
          fclock = tclock;
        break;
      case HOME:  /* write most recent freq value to dds */
        phaseaccum = calc_ph_acc(freq);
        write_phaseaccum(phaseaccum,FREQ0);
        break;
      case END:  /* write '0' freq value to dds */
        write_phaseaccum(0L,FREQ0);
        break;
      case F1:  /* increment base port address by 8 */
        par += 8;              /* PAR port address */
        control = par + 1;     /* Control register address */
        aux1 = par + 2;        /* Aux Control register address */
        aux2 = par + 3;        /* Aux Control register address */
        aux3 = par + 4;        /* Aux Control register address */
        break;
      case F2:  /* decrement base port address by 8 */
        par -= 8;              /* PAR port address */
        control = par + 1;     /* Control register address */
        aux1 = par + 2;        /* Aux Control register address */
        aux2 = par + 3;        /* Aux Control register address */
        aux3 = par + 4;        /* Aux Control register address */
        break;
      case F3: /* toggle red light */
        lights(RED);
        break;
      case F4: /* toggle Yellow light */
        lights(YEL);
        break;
      case DEL: /* reset */
        reset_dds();
        break;
      default:
        break;
    }
    if(ch == ESC) /* exit program */
      break;
  }
  return;
}
/*---------------------------------------------------------------------------
FUNCTION NAME:  cmdline()
DESCRIPTION: Parses and interprets the command line parameters
REQUIRES:     The command line variables.
RETURNS:      nothing
COMMENTS:     Sets global variables with values that override
              default values for Source clock frequency, port
              base address, and the step frequency.
---------------------------------------------------------------------------*/
void cmdline(int ac,char *av[])
{
  int i;
  int a;        /* temp variable to keep track of command line parameters */
  char *p;      /* temp pointer to command line parameters */
  a = ac - 1;
  while(a > 0)
  {
    p = av[a];      /* point to parameter string */
```

```
    switch(p[0]) /* use first character to identify */
    {
     case 'C':  /* Source clock frequency both upper and lower */
     case 'c':  /* case so not case sensitive */
       p++; /* increment the pointer past the switch value */
       fclock = atof(p);
       break;
     case 'P':  /* base port address, in hex on cmd line */
     case 'p':
       p++;
       sscanf(p,"%lx",&par);
       break;
     case 'S':  /* Starting step value in decimal */
     case 's':
       p++;
       sscanf(p,"%ld",&step);
       i = NUMSTEPS - 1;
       while(i >= 0)  /* check against all legit values */
       {
        if(step >= steplist[i])
        {
         stepnum = i;           /* save the pointer */
         step = steplist[stepnum]; /* and closest legit value */
         break;  /* done, short circuit while loop */
        }
        i—; /* decrement for next test */
       }
       break;
     default:
       break;
    }
   a—;  /* decrement to look at next parameter */
  }
  return;
}
/*------------------------------------------------------------------------
FUNCTION NAME:  getkey()
DESCRIPTION:    Waits for a keystoke and then reads the key pressed.
REQUIRES:       nothing
RETURNS:        The value of the keypress.
COMMENTS:       Reads the keystoke, determines if it is a normal key
          or and extended key. If it is a normal key, letter,
          number, etc, the first getch() returns the ASCII value
          of the key, an unsigned int value from 0x01 to 0xff. This
          value is returned by the getkey function. If the keypress
          is and extended key, a second call to getch() returns the
          scan code of the extened key. This value is shifted to the
          upper byte of the integer and returned as a multiple of
          256. For example, F1 returns 0x3b00, F2 returns 0x3c00.
------------------------------------------------------------------------*/
unsigned int getkey(void)
{
      unsigned int ch;
      ch = getch();
      if(ch == 0)
         ch = getch() << 8;
      return(ch);
}
/*------------------------------------------------------------------------
FUNCTION NAME:  calc_ph_acc()
DESCRIPTION:    Calculates the 32 bit phase accumulator value representing
```

```
                        the desired output frequency for the DDS chip
REQUIRES:               The desired output frequency as an unsigned long int.
RETURNS:                The phase accumulator value as an unsigned long int
COMMENTS:               Floating point is used to eliminate errors caused
        when integer values would be turncated during the
        divide operations.
-------------------------------------------------------------------------*/
unsigned long calc_ph_acc(unsigned long fl)
{
 double f;
 f = (double)fl;
    return( (unsigned long)((twoto32nd/fclock)*f) );
}
/*-------------------------------------------------------------------------
FUNCTION NAME:  write_phaseaccum()
DESCRIPTION:    Writes the 32 bit phase accumulator value to the
                parallel assembly register in the AD7008.
REQUIRES:       The 32 bit phase accumulator value an unsigned long int.
RETURNS:        nothing
COMMENTS:       Breaks the 32 bit phase accumulator value into four
          bytes. Each byte is sequentially written the the
          parallel assembly register as it is parsed from the
          32 bit word. The most significant byte is done first,
          followed by the next most significant until the least
          significant is done last. After the fourth byte is
          written, the xfer() function is called to transfer
          the value to the frequency register, thus generating
          the desired output frequency.
-------------------------------------------------------------------------*/
void write_phaseaccum(unsigned long ph_acc,int dest)
{
      int i = 4;
      gotoxy(1,20);
   clreol();
      printf("phase_acc = %lxh\n",ph_acc);
      while(i—)
      { /* start with MSB and send 4 bytes in decreasing significance */
    outp(par,((int)(ph_acc >> (i*8)))&0xff);
      }
      xfer(PAR|dest); /* now transfer from the PAR to the FREQ register */
      return;
}
/*-------------------------------------------------------------------------
FUNCTION NAME:  xfer()
DESCRIPTION:    Transfers the 32 bit phase accumulator value from the
                source register to the destination register in the AD7008.
REQUIRES:       An integer value with the 4 bit command specifying the
                source and destination registers.
RETURNS:        nothing
COMMENTS:       The first output writes the 4 bit command to the
          latch on the transfer control bus of the AD7008.
          This is done prior to insure that the data on the
          transfer control bus is stable prior to the load
          strobe. The second ORs in the load strobe bit, thus
          strobing the LOAD term on the AD7008. The third again
          writes the 4 bit command to insure the data on the bus
          remains after the strobe.
-------------------------------------------------------------------------*/
void xfer(int cmd)  /* cmd=4 bit cmd, source and dest reg */
{
 outp(control,cmd&0xff);          /* write command (cmd) */
```

```
 outp(control,(LOAD|cmd)&0xff); /* now with the load (transfer) bit */
 outp(control,cmd&0xff);        /* hold command after load bit drops */
 return;
}
/*-----------------------------------------------------------------------
FUNCTION NAME:  reset_dds()
DESCRIPTION:    Resets the AD7008 to power up defaults.
REQUIRES:       nothing
RETURNS:        nothing
COMMENTS:
-----------------------------------------------------------------------*/
void reset_dds(void)
{
 outp(control,RESET & 0xff);
    outp(control,0x00);
    return;
}
/*-----------------------------------------------------------------------
FUNCTION NAME:  lights()
DESCRIPTION:    Toggles either the red or yellow LED on/off
REQUIRES:       An integer value specifying which LED to toggle
RETURNS:        nothing
COMMENTS:       Reads the current state of the latch controlling
           the specified LED. Then writes a value toggling the
           latch to the opposite state.
-----------------------------------------------------------------------*/
void lights(int cmd)
{
      char old;
      old=inp(aux1); /* read the current status */
      if(cmd && old && 0xff) /* already set? */
           outp(aux1,(~cmd)&old&0xff); /* then clear it */
      else
           outp(aux1,(cmd|old)&0xff);  /* else set it */
      return;
}
```

Register	Size	Reset State	Description
COMMAND REG	4 bits CR3-CR0	All Zeroes	Command Register. This is written to using the parallel assembly register
FREQ 0 REG.	32 Bits, DB31-3B0	All Zeroes	Frequency Select Register 0. This defines the output Frequency, when FSELECT = 0, as a fraction of CLOCK frequency
FREQ 1 REG.	32 Bits, DB31-DB0	All Zeroes	Frequency Select Register 1. This defines the output frequency, when FSELECT = 1, as a fraction of the CLOCK frequency
PHASE REG	12 BITS DB11-DB0	All Zeroes	Phase offset register. The contents of this is added to the output of the phase accumulator
I Q Mod Reg.	20 Bits DB19-DB0	All Zeroes	I and Q Amplitude Modulation Register. This defines the amplitude of the I and Q signals as 10-bit two complement binary fractions. DB[9:0] is multiplied by the quadrature (sine component and DB[9;0] is multiplied by the IN-Phase (cosine) component.

Figure 8. AD7008 control registers. Taken from AD7008 DDS Modulator Applications Note C1791-18-4/93 (Rev 0) page 7.

Parts List

Source Codes: A=Allied
D=Digikey
J=Jameco
M=Mouser
N=Network

Item	Qty	Reference	Value	Source
1	15	C1, C2, C3, C4, C6, C7, C8, C9, C10, C11, C12, C14, C18, C19, C21	.1UF	D, J, M
2	1	C5	22PF	D, J, M
3	2	C13, C20	4.7UF	D, J, M
4	2	C15, C16	.33uf	D, J, M
5	1	C17	.33UF	D, J, M
6	1	CR1	MOV	D, J, M
7	4	D1, D2, D3, D4	LED	D, J, M
8	1	DC1	DCDS O512S	M
9	1	J1	P/O PC Board	
10	9	JP1, JP2, JP3, JP4, JP5, JP6, JP8, JP12, JP25	HEADER 4	D, J, M
11	1	JP7	HEADER 9	D, J, M
12	5	JP9, JP10, JP11, JP13, JP26	HEADER 2	D, J, M
13	7	JP14, JP15, JP18, JP20, 21, JP22, JP23	HEADER 8	D, J, M
14	1	JP19	HEADER 6	D, J, M
15	1	JP24	HEADER 20X2	D,J,M
16	1	P1(short reach PCB right angle)	CONN. DB25	D,J,M
17	6	Q1, Q2, Q3, Q4, Q5, Q6	VN10KM	D, J, M
18	1	R1	100K	D, J, M
19	1	R2	536	D, J, M
20	4	R3, R4, R15, R16	1K	D, J, M
21	2	R5, R6	10K	D, J, M
22	2	R7, R8	68	D, J, M
23	1	R9	18K	D, J, M
24	1	R10	604 OHMS	D, J, M
25	4	R11, R12, R13, R14	180	D, J, M
26	1	R17	4.7K	D, J, M
27	1	R18 (10K app. Specific)	POT	D, J, M
28	1	RP1 (10k)	RS1P9	D, J, M
29	1	S1	SW DIP-8	D, J, M
30	1	T1 (see *ARRL Handbook* 1:1 50 Ω)	Application Specific	
31	1	U1	74LS688	D, J, M
32	1	U2	74LS245	D, J, M
33	1	U3	NE5534/LM6131	D, J, M
34	1	U4	74HC138	D, J, M
35	1	U5	LM7805	D, J, M
36	1	U6	AD7008	D, J, M
37	2	U7, U8	74HC86	D, J, M
38	4	U9, U10, U16, U17	74HCT373	D, J, M
39	1	U11	74HC02	D, J, M
40	1	U12	74HC32	D, J, M
41	4	U13, U14, U18, U19	74HCT244	D, J, M
42	1	U15	50 MHz OSC	D, J, M

Milled IC sockets with built-in bypass capacitors are available from Mouser Electronics under the Mil-Max brand. Mouser stock numbers: 575-493314 (14 pin), 575-493316 (16 pin), and 575-493320 (20 pin).

CR0	=0	**Eight Bit Databus. Pins D15-D8 are ignored and the parallel assembly register shifts eight places left on each write. Hence four successive writes are required to load the 32-bit parallel assembly register**
	=1	**Sixteen-Bit databus. The parallel assembly register shifts 16 places left on each write. Hence two successive writes are required to load the 32-bit parallel assembly register, Figure xxx**
CR1	=0	**Normal Operation**
	=1	**Low Power Sleep Mode. Internal Clocks and DAC current sources are turned off**
CR2	=0	**Amplitude Modulation Bypass. the output of the sine LUT is directly sent to the DAC**
	=1	**Amplitude Modulation Enable. I Q modulation is enabled allowing AM or QAM to be performed**
CR3	=0	**Synchronizer Logic Enabled. The FSELECT, LOAD, and TC3-TC0 signals are passed through a 4-stage pipeline to synchronize them with the CLOCK frequency, avoiding metastability problems**
	-1	**Synchronizer Logic Disabled. The FSELECT, LOAD, and TC3-TC0 signals bypass the synchronization logic. This allows for faster response to the control signals**

Figure 9. Command register bits. Taken from AD7008 DDS Modulator Applications Note C1791-18-4/93 (Rev 0) page 7.

- PageUp—Increments *fo* by the step value,
- PageDown—Decrements *fs* by the step value,
- LeftArrow—Decrements the step value to the next lower value,
- RightArrow—Increments the step value to the next higher value,
- Home—Sends the most recent *fo* to the DDS and is useful after adjusting *fs* to send new phase accumulator value to DDS,
- End—Sends *fo* = 0 Hz to the DDS,
- Del—Resets the DDS,
- F1—Increments the portbase by 8,
- F2—Decrements the portbase by 8,
- F3—Toggles the Red LED On/Off, and
- F4—Toggles the Yellow LED On/Off.

The finalities

The basic DDS board can be used in a variety of applications. The additional I/O ports provide for control of external hardware. Items such as antenna selection, band switching relays, and mode of transmission changes are just a few of the possibilities. Through software development, complex modulation schemes are also possible. Accurate and phase contiguous FSK signals can be generated by manipulating the FSELECT bit in the DDS control port. Another attractive capability of the DDS board is its ability to enhance older radio performance. With some restrictions, the DDS board may be used as a stabilized replacement for the Collins 312B5 external VFO. The venerable Heathkit DX100 can take on rocklike stability with a simple DDS interface board to raise the injection voltage to vacuum tube levels.

Tests were run using the DDS board with a Heath SB-104A transceiver. The NE5534 operational amplifier was replaced with a National LM76181 current mode device with a gain setting of five. The DDS signal (unfiltered 4-volt P-P) was inserted into the SB-104A's external VFO jack. On-air tests were encouraging. Frequency stability was excellent. A 24-hour worst case drift of 4 Hz was noted. All SB-104A crystal oscillators and sideband selection oscillator errors were accounted for in software. The end result was digital frequency control accurate to a few Hz with tuning steps ranging from 1 Hz to 1 kHz—quite an improvement over the Heath VFO. In-depth off-air analysis hasn't been compiled at this time, but no increase in receiver noise or spurious responses were noted during the on-air tests.

Specific application schemes for other radios are beyond the scope of this article, but the success of the Heath SB-104 test is encouraging. Numerous ham radio transmitters, receivers, and transceivers use variable local oscillators in ranges less than 10 MHz and would be candidates for a Digital Frequency Oscillator (DFO).

Building information

Those interested in building their own DDS board will find the components needed for this project in the **Parts List**. For pc board information, contact <rmmiller@IX.netcom.com> or <dsipc@calweb.com>. ■

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A CONTINUOUS DUTY BATTERY CONTROLLER

Charge any size lead-acid battery system, gelled electrolyte, or liquid

Under emergency conditions, battery power is often the best possible source of immediate energy to run communications equipment. It's quiet, portable, ready to use, and compact. Gelled-electrolyte cells are available from surplus suppliers and at flea markets. These cells are often "pulls" from companies that replace cells in their equipment on a routine basis (say, every two years), so a good power back-up system is always ready to meet emergency demands. Typically, these cells haven't been abused and are in excellent condition, with many years of use left in them.

Keeping batteries ready for use can be a burdensome task without a proper charging system. A standard department store charger is often nothing more than a bulk charging system that dumps a large current into the battery until

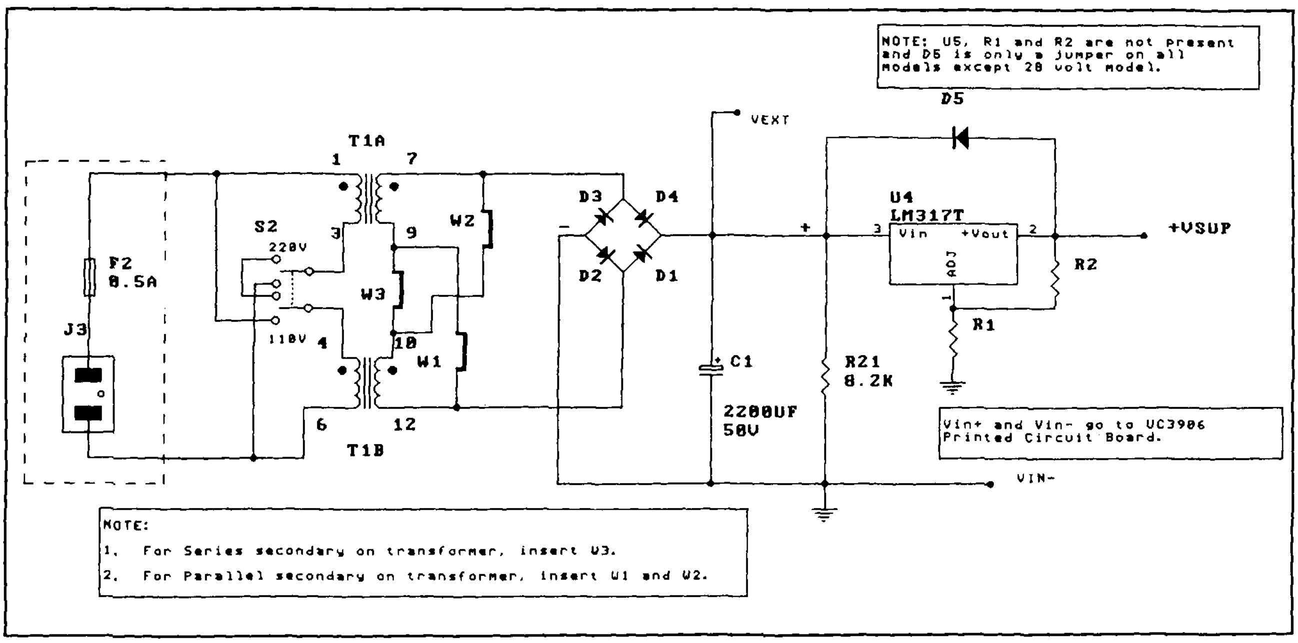

Figure 1. Battery controller power supply schematic.

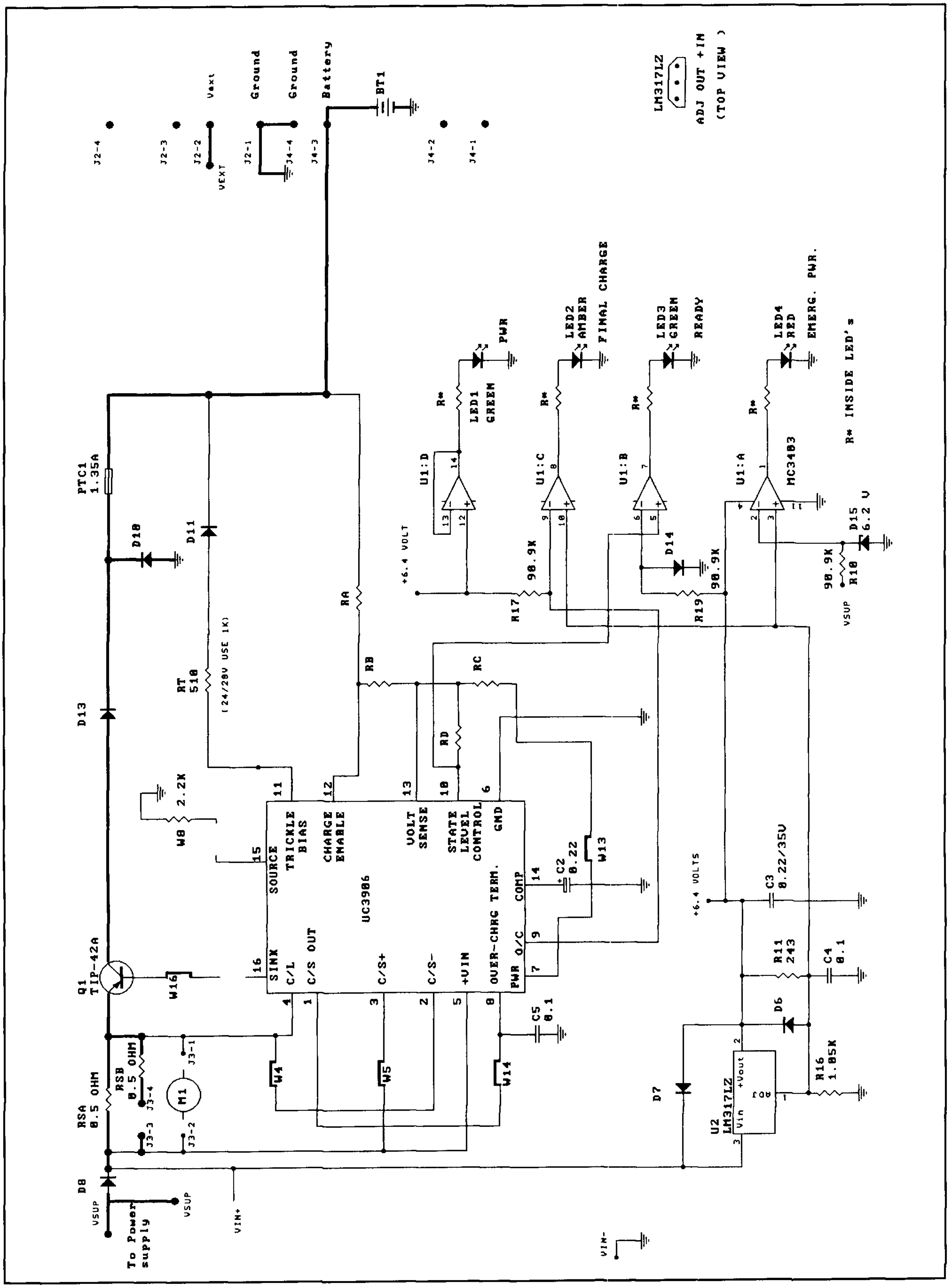

Figure 2. Battery controller schematic.

it's somewhere near fully charged. This is fine in situations demanding a quick charge, as when a battery is needed to jump start an automobile, but can be very destructive to the battery if used as a continuous duty charger.

I'll describe a controller you can use to charge and maintain any lead acid battery system from 6 to 28 volts, regardless of size. A battery charger is usually a simple circuit—basically nothing more than a bulk charger. A controller, on the other hand, is a precision device that carefully controls the battery's charge state. The printed circuit board system described handles currents of up to 1 amp and, with a few offboard components, can control even larger currents.

How big should the battery be?

Many amateur operators shy away from battery power, believing it's for QRP operators. Nothing could be further from the truth! Batteries can store substantial power, and a 100- or 200-watt station can easily be powered by lead acid cells. In most cases, an automobile-sized battery is sufficient to power a typical transceiver and a few accessories.[1]

How big should the controller be?

The key here is usage. If you're very active, perhaps using RTTY or AM for long periods, the demands on the controller will be high. If you operate SSB or CW just a few hours a day, a 1-amp controller will return power to the battery at about a 14-watt per hour rate, which means the battery should be fully recovered in about 6 hours.

What is a "Smart Charger" and do I really need one?

A "Smart Charger" can monitor and satisfy a battery's needs. This type of charger is a controlled loop (controller) using feedback from the battery to maintain proper charge under all conditions—including maximum bulk charging, overcharge, and float voltage rates. A well-designed controller should include the following: reverse battery protection, trickle-charging for severely discharged batteries, temperature compensation, and low-voltage disconnection of the battery when it's dangerously low and the source of charging power is absent. My charger meets all these requirements.

The Smart Charger is an around-the-clock sentry for those who haven't the time to monitor a station battery constantly. More primitive chargers can work; however, particularly with gelled electrolyte batteries, you'll pay a price in battery life and performance.

Table 1. Values needed for various voltages.

Battery Voltage (volts)	XFMR Voltage (VAC)	RA kohms	RB kohms	RC kohms	RD kohms
6	8–11	69.8	16.9	43	392
12	15–18	200	16.9	43	499
14	16–20	243	16.9	43	511
24	24–28	453	16.9	43	549
28	28–32	549	16.9	43	549

There are two popular methods for charging lead acid batteries: dual level floating voltage charging or dual step charging. The floating voltage approach tracks battery voltage during charging and, at a preselected voltage, transitions the charging current by reducing or increasing it as needed. The advantage of the floating voltage charger is that it can charge practically any lead acid battery—regardless of size—because it uses voltage information common to all lead acid batteries, whether liquid or gelled electrolyte.

The dual step current approach switches the charging currents based on those that the battery draws during charging. The dual step current charging method is only feasible if you know the size and type of battery ahead of time, because it depends on the current requirements of the specific battery. A dual step current charger may be used to charge strings of batteries by controlling the charge rate in one of the batteries in the series, provided all the batteries are of a like type and size. One common application is electric car battery charging.

My controller is a dual level floating voltage charger. However, the printed circuit board, with jumper changes, can be configured for duty as either type.

Circuit description

Refer to the schematic in **Figure 1**, starting at the input on the left and working towards the right. Any good amateur radio design should have a power supply capable of operation on either 110 or 220 volts AC and 50 or 60 Hz. This circuit uses onboard switch S2 and transformer T1 to meet this requirement. The secondary has three jumpers so the secondaries can be wired in parallel or series, depending on the output voltage required. An offboard ON/OFF switch, S1, may be used if desired. A bridge rectifier, D1-D4, converts the AC to DC.

The filter capacitor, C1 (2200 µF), provides more smoothing than is really necessary.

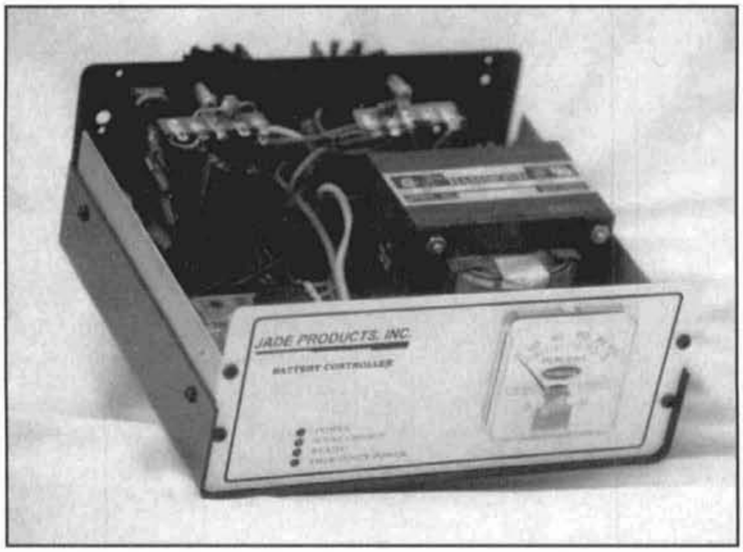

Photo A. Front view of controller shows four LEDs, current meter, and larger power transformer inside. This is the 5-amp controller.

Resistor R21 provides a small bleeding current that drops the supply voltage to almost zero volts in about 20 seconds, so the loss-of-power circuitry can detect that the power is gone. At this point, Vext comes in and can operate as an external source of power, such as a solar panel. If you use solar power and have a diode in series with the panel current, the line current can be used simultaneously. The source with the higher voltage will supply the charging current.

Voltage regulator U4, an LM317T, is used only in the 24- and 28-volt charging configurations to keep supply voltages below 40 volts. This is the maximum voltage rating for the UC3906 controller IC (see **Figure 2**). R1 and R2 provide the voltage regulator setpoints and D5 provides transient protection for the regulator. R1, R2, U4, and D5 aren't used for the 6- to 14-volt regulators, and D5 is replaced with a jumper.

Diode D8 keeps the battery current from reaching the power supply when the power drops off. This reduces back-drain current that results from leaving the battery and running it down prematurely when the power quits.

RSA and RSB are the current sense resistors. The ever-popular Unitrode UC3906[2] controller chip holds the current through the sense resistors to a 0.25-volt drop. The maximum charge rate is determined by the voltage drop across them. RSB is brought out to a connector. An external switch may be used to switch between high and low current ranges. If only RSA is in the circuit (0.5 ohms) the current is:

Imax = 0.25 V / RSA
0.5 amp = 0.25 / 0.5

Switching RSB in parallel reduces the parallel resistance to 0.25 ohms, doubling the current to 1.0 amp. Other resistor values may be used; however, the etch on the board is only capable of 3 amps of current and the transformer is only capable of 1 amp of current. An offboard transformer or DC supply would be needed with currents greater than 1 amp.

The sense resistors provide a convenient point for measuring the charging. Because the voltage drop across the sense resistor combination will never be greater than 0.25 volts at maximum current, a 250-mV meter (M1) will show maximum current rate, regardless of the current setting. Using this approach, the meter will indicate 100 percent current, whether the current is 1.0 amp or some other value.

The UC3906 is capable of charging a battery at up to a 25 mA rate, but this is inadequate for most applications. Pass transistor Q1, a TIP42A, supplies a more practical rate of charge. IC pin 16 provides base current to Q1 to control the current passing through it; this is determined by the sense current in RSA and RSB.

Diode D9 keeps power going to the controller when the power source is absent. This is important during a power failure, or, should you be using solar charging, at night or when the sun is behind the clouds. During this time the power comes from the battery that's being charged, but the current is only a few mA. Of course, you can eliminate D9 and shut the charger down entirely when there's no power, which means the low-voltage disconnect circuits won't be functional.

D11 and D13 prevent the battery from discharging through the charger when power is unavailable. Diode D10 provides a short circuit path to ground when a battery is connected backwards, causing heavy flow through PTC1, a positive temperature coefficient device. With heavy currents of over 1.35 amps, the PTC acts like a fuse and goes open. Once the backwards battery is removed, the device cools and allows current to flow again. In essence, the PTC is an automatically resetting fuse.

Resistor RT sets the controller trickle current. Any current up to 25 mA is allowed. A trickle current brings the battery up to a minimum voltage before bulk charging begins. Resistors RA, RB, RC, and RD are voltage-sensing resistors, and set the various points for the charging curve. **Table 1** lists the values needed for various voltages.

Pin 7 of the UC3906 is an internal transistor open collector. The sensing resistors are connected to ground through pin 7 when the transistor is turned on. Whenever the UC3906 detects that the power supply voltage is too low, it will cause pin 7 to go open and disconnect the sense resistors from the ground reference. This off state, in conjunction with the

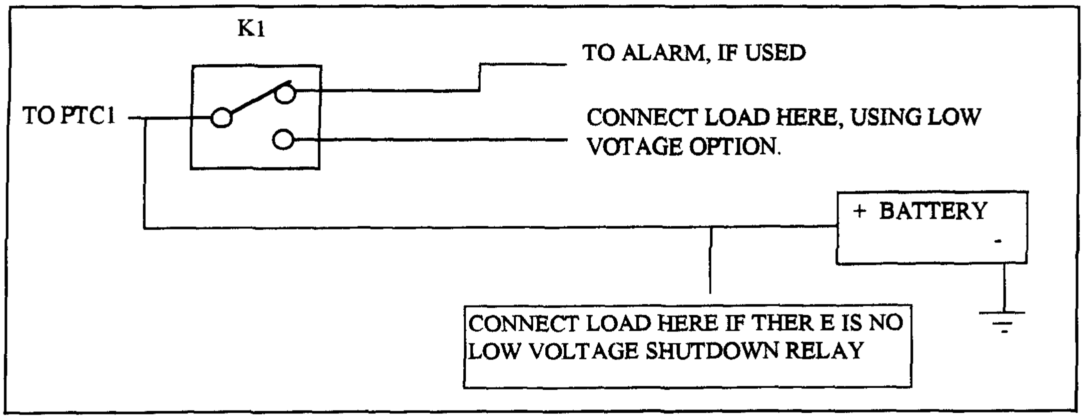

Figure 3. Possible connections for low-voltage option.

reversed diodes elsewhere in the circuit, limits reverse-trickle currents from the battery to a few μA when the power is off and the battery is still connected to the controller. If diode D9 is used in the circuit, the LEDs can draw several mA each, if on. This isn't a problem if long term power outages aren't expected.

Pin 8 is the over-charge terminate input. It tells the charger that the battery is completely charged. As configured in this design, the input signal comes from pin 1—which is the current sense amplifier output. When the amplifier determines that the battery current has dropped to a sufficiently low state, it switches the controller to the final state of charge, a floating state. Capacitor C5 filters pin 8, preventing it from responding to transients that could prematurely end the charge cycle. One note to builders: the current between pins 1 and 8 is only about 10 μA. After soldering, make sure all residue is washed off. Even trace amounts of resin can act as a resistance to other points and cause some very strange symptoms.

Capacitor C2 is a compensation capacitor to keep things stable. For most applications, 0.22 μF is quite adequate.

Jumpers W8 and W9 are used to configure the drive arrangement. In this application, W9 is empty and W8 is a 22-k resistor. Those interested in other variations of the driver circuits should refer to the Unitrode Application Notes.

U2 is a voltage regulator, set to 6.4 volts by R11 and R16, used to create a supply for the indicator circuitry. The quad op-amp, U1, an MC3403, is used as a logic circuit to drive the LED package. The op-amp output has a drop of about 1.4 volts from the supply voltage, so it's at 5 volts when the output is high. The LED package has an internal resistor for each LED that sets it to operate at 5 volts. R* is that resistor. **Photo A** shows the LEDs on the front of the controller.

LED1 (green) indicates that power is available. The power can be from any source; i.e., the batteries (if D9 is in circuit), the power line, or an external input. The indicator simply shows that power is available from some source.

LED2 (amber) indicates that the battery is approaching the fully charged state and will go into float state next. On smaller batteries this state may only last an hour or less; on larger batteries it could last for many hours; and with very large batteries, a day or more.

LED3 (green) indicates the battery is fully charged. It will stay on until the battery is discharged to about 90 percent of full charge. If the battery is used while in this state, the controller will replace the energy without going through a complete charge cycle. If the battery drops below 90 percent, the controller will switch to the bulk charge state, and a complete charge cycle will commence.

LED4 (red) indicates that all sources of external power are down, and the controller is now getting its power from the battery. This LED doesn't light immediately; it comes on after about 20 seconds without external power. Op-amp U1A senses supply voltage on pin 2 and is held to 6.2 volts when it is present. Pin 3 is at 5.15 volts and is the reference voltage of regulator U2. When the Vsup voltage drops below the 5.15 reference, LED4 lights.

Low-voltage shutdown circuit

If the battery is to be left unattended with its load attached, it's useful to have a battery-disconnect circuit. If the battery reaches dangerous discharge levels, it may be damaged and need to be replaced. This circuit offers two possible battery disconnection methods (**Figure 3**).

Relay K1 is used to disconnect the battery in a low-voltage state. Transistor Q2 is a switch that turns the relay on or off. Let's examine a situation where a battery is discharged and the

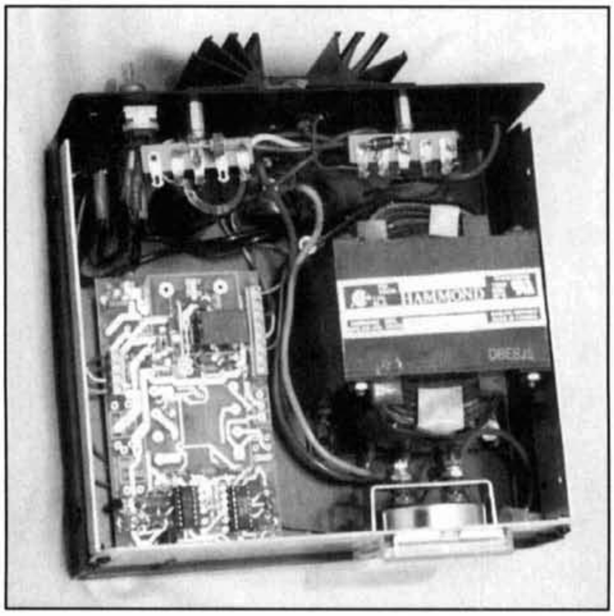

Photo B. Battery controller designs place great demands on the heatsink, shown here mounted on the back of the controller box.

power is off. Initially, the relay is assumed to be in the normally closed position with the contact connected to the DC out terminal. If desired, a very low current alarm device can be connected here to warn of the situation, or the signal can be used to trigger an alarm on a remote radio, etc.

The power comes on. If the battery is very low, below 10.5 volts in the case of a 12-volt system, the UC3906 senses this and put out a trickle voltage on pin 11. This, in turn, starts a trickle charge to the battery to bring it up to 10.5 volts—where bulk charging can commence. Assume for the moment that jumper W17 is in place and MOSFET Q5 isn't present. The voltage on pin 11 then also drives transistor Q3, which turns on and pulls the drive to Q2 low, so Q2 can't turn on and the relay stays off.

When battery voltage reaches the bulk charge state, the trickle voltage turns off. The Vin signal on R4 turns on Q2 and the relay pulls in, connecting the battery to the load. Bulk charging now begins.

If you use MOSFET Q5 instead of W17, the battery won't be connected to the load until the "ready" state is reached. You must decide which scenario you preferred, as you can't use both W17 and Q5 in the circuit at the same time.

The battery charges until the float state is reached. If the power source is eliminated, the system continues to run off battery power. If jumper W17 is used, the battery continues to discharge until the trickle voltage is reached again. The trickle voltage comes on and fires Q3, which causes the relay to disconnect. The controller now loses all power and shuts down until power returns.

If you build this circuit without the low-voltage disconnect components (**Table 2**), the load is connected directly to the battery. If you use the low-voltage circuit, connect the load to the DC out connector (**Figure 3**).

This circuit can be used as a low-voltage shutdown circuit without the charging capability. Such a circuit might be useful in a recreational vehicle or in a situation where a very high-current charger already exists and a disconnect circuit is needed. Relay K1 can be used to drive an offboard solid-state relay with much greater current capability.

When do I need a greater than 1-amp controller?

Stations that use SSB or CW as their primary operating mode can be quite efficient; however, stations using FM, RTTY, or repeaters can put very high demands on their energy source. Repeaters, particularly during emergencies, may perform "around the clock" duty. A 50-watt repeater can easily draw 10 to 15 amps from a 12-volt power source. Quick recovery for this type of service demands a controller that provides at least 5 amps, assuming the battery is at least 50 A/H, preferably larger.

Heat and battery charging

Regular power supply designs must always take heat dissipation into consideration, but battery controller designs place even greater demands on the heatsink (**Photo B**). Because the output voltage for a 12-volt battery can be as low as 10.5 volts, and the power supply section can be as high as 18 volts under load, the heatsink must dissipate as much as 40 watts at a 5-amp load! This is a substantial amount of heat to dissipate without a fan. Fortunately, a lead-acid battery won't stay at the 10.5-volt point for very long and, if it's in good condition, will reach close to 12.0 volts in a very short time. However, there will still be 30 watts of heat to dissipate. Only build as much battery controller as is needed to save wasted energy. In most cases, 5 amps is sufficient.

Let's look at a specific 5-amp controller, with suggestions to support larger versions.

Power supply section

A rule of thumb for battery charging is to use 1000 µF for every amp of current needed. For 5 amps, a 5000-µF capacitor in the filter section will suffice. In this controller, I use a 6800 µF capacitor. At 5 amps, the diode bridge dissipates nearly 6 watts; the two diodes in the path to the

Table 2. Low-voltage Option Components

Designator	Item	Source
K1	Relay	Potter-Brumfield T-70 series. (Select relay and R3 for voltage used.)
R7	90.9 k	
R4,R5,R6	9.09 k	
Q2,Q3	2N3904	general purpose transistor
Q5	BS170	Jade Products
D12	1N4148	general purpose diode

battery dissipate an additional 6 watts. This loss must be considered when arriving at the transformer's power capability. Consequently, when using capacitive input filters, it's wise to choose a transformer capable of approximately twice the current needed (see **Figure 4**)!

Pass transistor selection

Unitrode controller chip UC3906 is capable of driving up to 25 mA. Five amps is 200 times this current. Most standard power transistors don't have near a Beta (gain) of x200. There's a family of transistors with two transistors in one package that multiply their gain; these are known as Darlington Pairs. The Darlington Pair I've chosen for Q1 is the MJ900. Its Beta is in the thousands, even at these current levels, and it can handle the very high junction temperatures of high-current charging. With ambient temperatures of 29 degrees C, the case temperature of the pass transistor can approach 90 degrees C. This is well within the capabilities of the transistor; however, as with any design, the lower the temperature, the better. For high reliability and continuous duty, a fan is beneficial (see **Figure 5**).

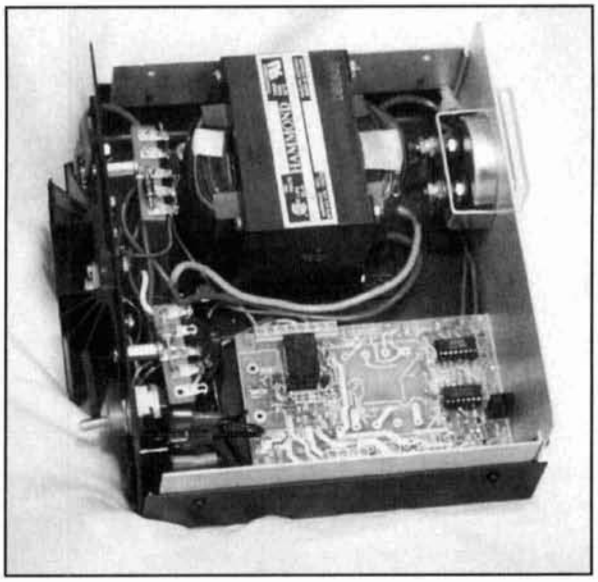

Photo C. Inside view of the 5-amp controller. Large power components mount along terminal strips along the back wall.

At these gains you must be concerned about stability, as it's possible for the controller to oscillate. The capacitor at pin 14 of UC3906 will compensate adequately under these conditions.

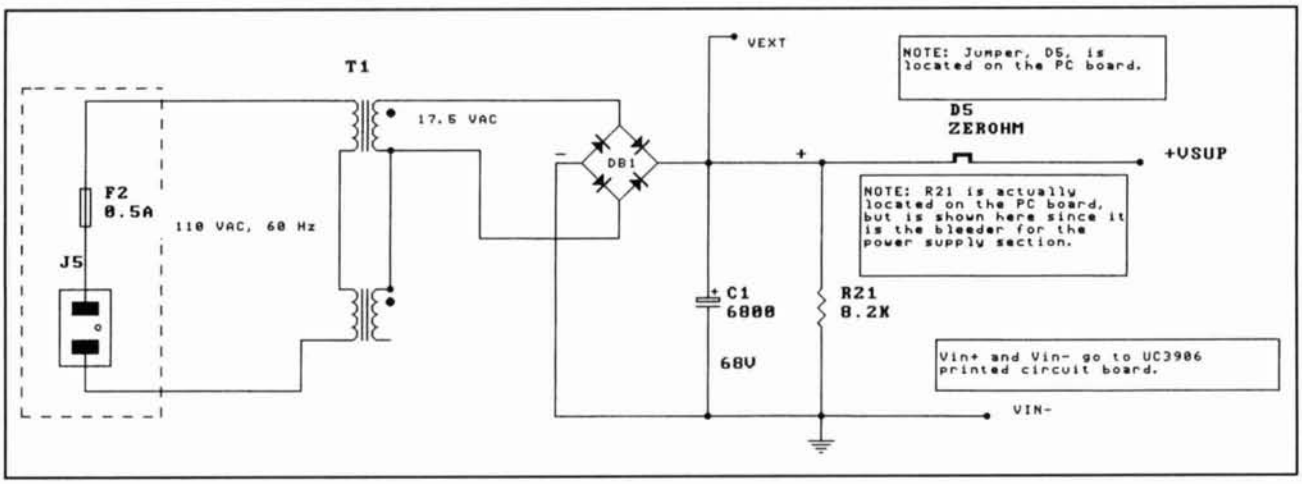

Figure 4. Five-amp controller supply.

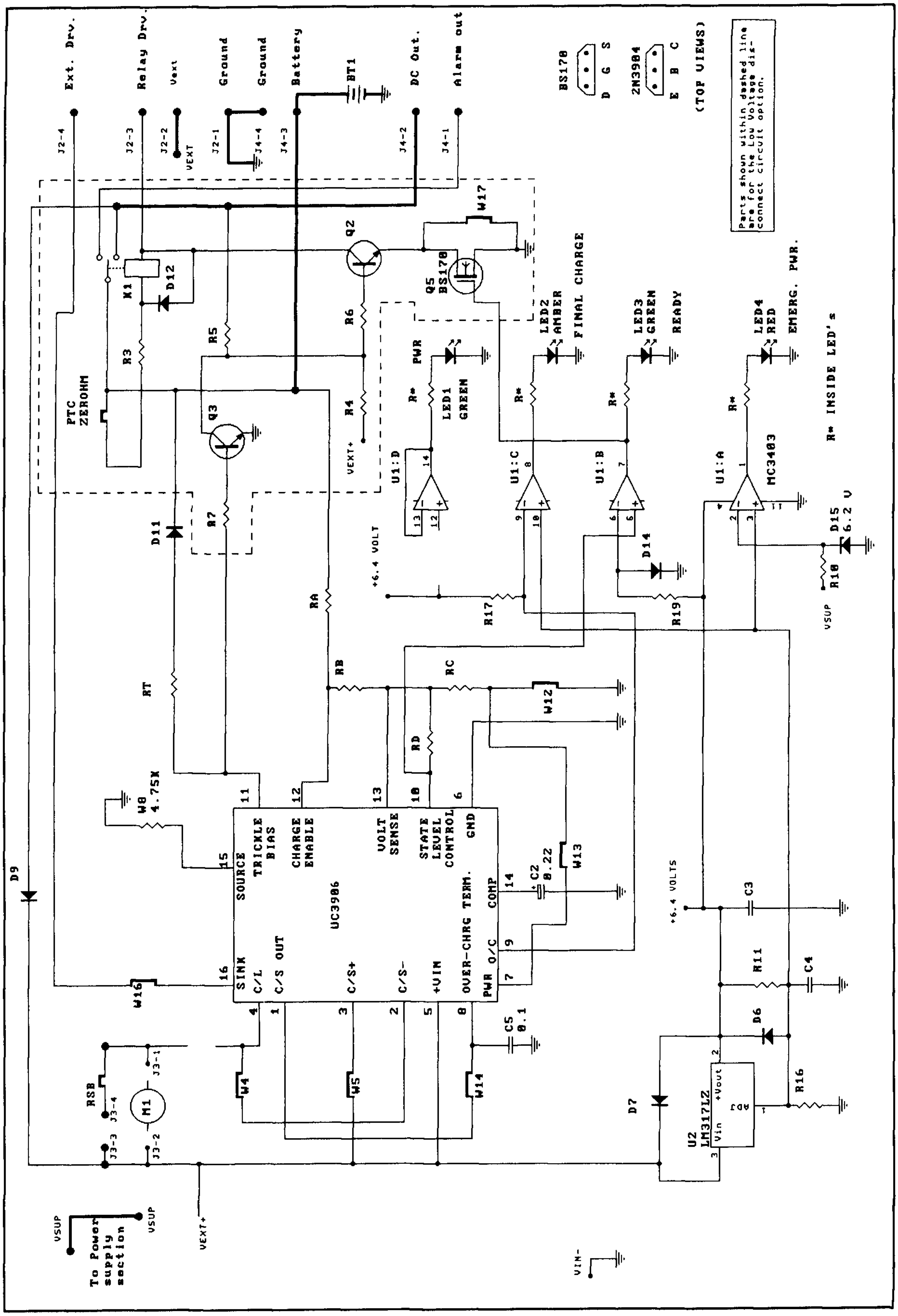

Figure 5. Five-amp pc board.

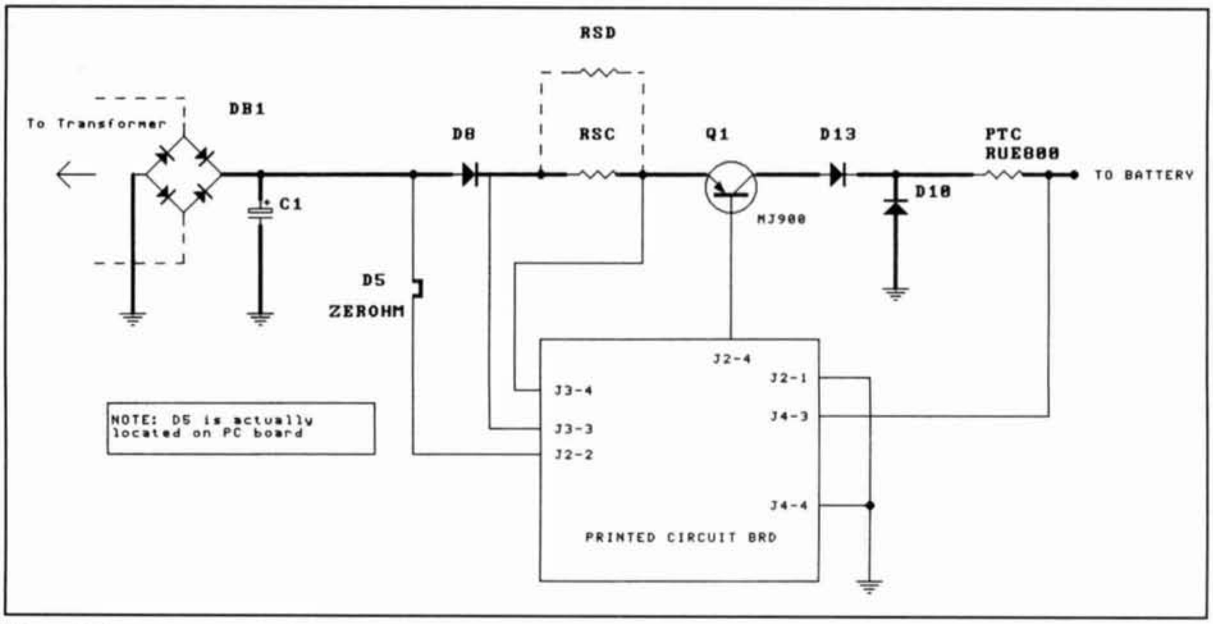

Figure 6. Five-amp terminal strip.

The printed circuit board described earlier isn't capable of handling these higher currents directly. For this reason, some of the parts that were "onboard" the 1-amp controller are now mounted offboard. Wires connect them for the 5-amp design. The diodes, pass transistor, wires, and PTC for high-current charging mount along the back wall of the controller on terminal strips (**Photo C**). In this case, the PTC is rated at 8 amps at room temperature and operates at around 6 amps under normal charging temperatures (see **Figure 6**).

Low-voltage shutdown circuit

Although I've already discussed the theory of the low-voltage shutdown circuit, a few comments about using it at higher currents are warranted. In situations where an unattended battery system could possibly discharge below a safe point, it's recommended you have a shutdown circuit to disconnect the battery. My pc board has an onboard relay (see **Photo D**) that disconnects the battery from the load under such conditions. The relay can handle load currents of up to 2 amps. For larger loads, use the relay output to drive an offboard solid-state relay.

This particular low-voltage shutdown circuit is advantageous because it can be added later, after the circuit is up and running and without changes to the original circuit. Many shutdown circuits require you to break the current path and make many modifications to the original circuit to accommodate the shutdown circuit.

The low-voltage shutdown circuit is particularly useful for those who use automobile or motorcycle lead-acid batteries in fixed station amateur use. Unlike batteries specifically designed for deep cycle usage, the standard auto battery is more susceptible to damage under these conditions. Even though deep cycle batteries, such as those used in forklifts and golf carts, have become less expensive in recent years, the department store automobile battery is a bargain. The low-voltage shutdown circuit will prevent "deep cycling" from occurring and prolong battery life.

Higher currents

The most difficult part in designing a high-current controller lies in providing proper cooling of the pass devices. For very high

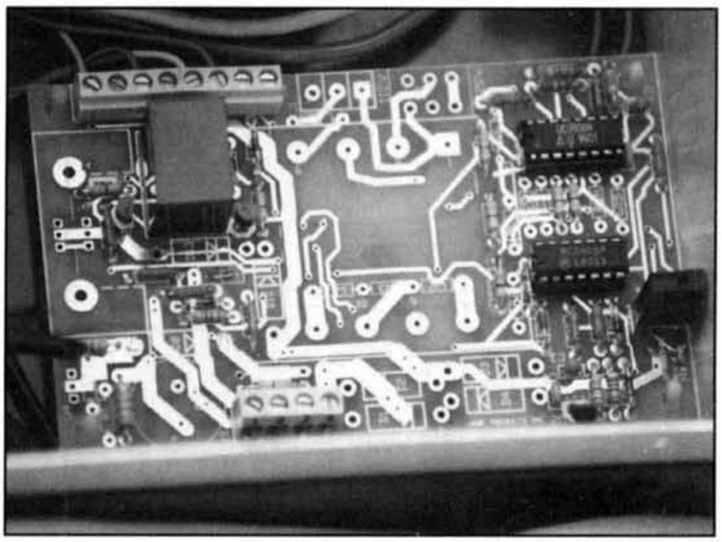

Photo D. PC board with terminal strips, using screws to connect wires. The large black "block" is the low-voltage shutdown relay. The tall block next to the ICs is the four-position LED holder.

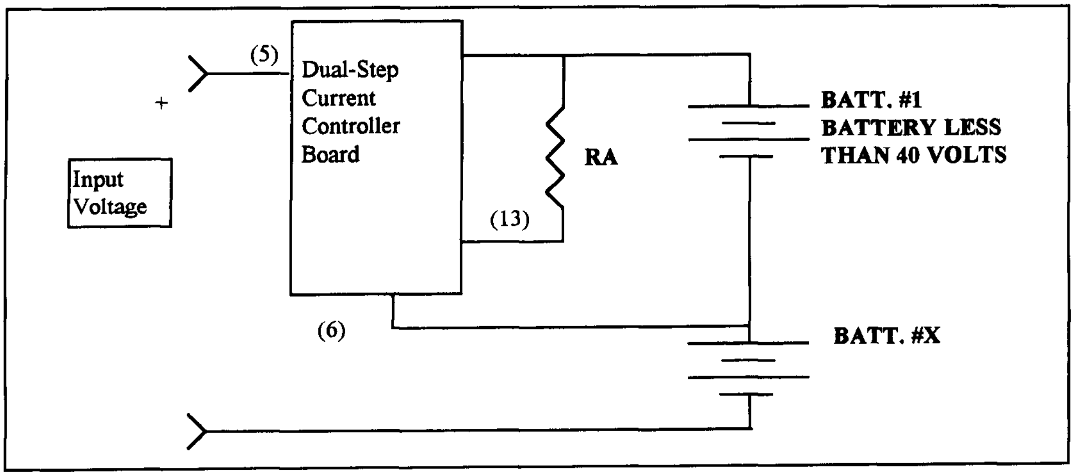

Figure 7. Possible connection for charging high-voltage battery arrangements with a lower voltage dual-step current controller board.

currents, you can use forced air cooling or you can submerge the heatsink in a motor oil bath; the voltages involved will not be affected by the oil. But use Teflon™-coated wire in this case, because motor oil can damage many standard insulations.

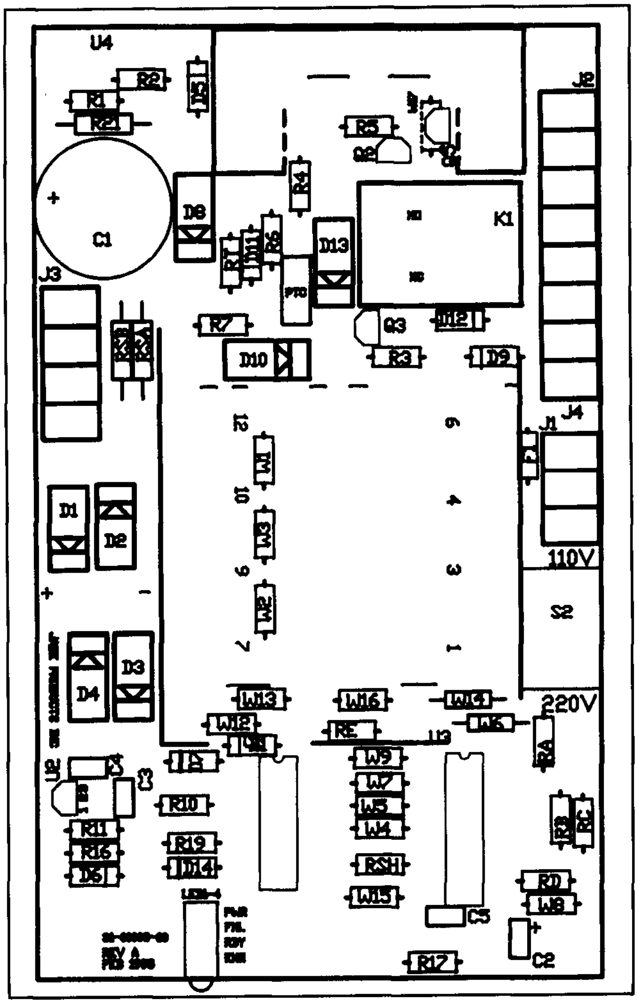

Figure 8. Top overlay.

Conductor size must be considered when dealing with very high currents. A no. 20 wire can safely handle 5 amps of current over short distances (i.e., several inches) without substantial voltage drop. Pay particular attention to long runs of wire or cable from the controller output to the battery. The voltage drop over many feet of wire can be substantial. If long wires are necessary, use a separate wire to connect the top of resistor RA directly to the battery. This will overcome the high-current drop in the charging cable and give the sense resistor a proper measurement of the voltage at the battery (the sense current is only about 50 µA).

Dual-step current controller

This design offers potential for the electric automobile, or other situations where a high-voltage battery supply is needed. A power supply section can be designed to supply over 100 volts. The controller board can be "floated" so the controller section charges an individual battery or group of cells at 12 or 24 volts, and the 96-volt battery system is charged by the current controlled in the lower-voltage section. In essence, the current to charge battery #1 is carried through the other batteries in the series (see **Figure 7**). Under these conditions, the batteries must all be the same type and size. The Unitrode Application Notes provide more information about dual-step current controllers.

Parallel battery charging

Lead acid batteries—gelled electrolyte, in particular—can be charged in parallel. All the cells should be of like size and condition. It's wise to put some sort of small resistance in series with each battery for better equalization during bulk-charge mode. A 0.10-ohm resistor

Parts List, 1-amp Controller

Complete kits, including enclosure, meter, pc board, transformer, and all other parts are available from JADE PRODUCTS, Inc. See ads in *QST*, or call 1-800-JADE PRO (1-800-523-3776).

Individual parts are also available from JADE PRODUCES, Inc., or as indicated below.

All resistors are 1/4 watt, 1 percent, unless otherwise noted.

Designator	**Item**	**Source**
PC board	Part no. 31-00004-00	Jade Products, Inc.
R21	8.2 k, 1 W, 5%	Jade or Mouser
RT	510 ohms (for more than 20 volts use 1 k)	
PTC1	RUE135	Ray-Chem, available from Sager or Jade
D5,D6,D7 D9,D11,D14	1N4148, general purpose diode	
R11	240 ohm, 5%	
R1	6.65 k	
RSA,RSB	0.5 ohm, 1/2 W	
D1-D4, D8 D10,D13	1N5401, 3-amp silicon rectifier	
F1	3/4 amp Pico fuse	
R10,R19 R17	90.9 k	
R16	1.05 k	
C1	2200 μF/50 volts	
C2,C3	0.22 μF/100 volts	
C4,C5	0.1 μF/100 volts	
LED1-4	LEDs: 2 green, 1 amber, 1 red.	Individuals or single package from Jade
Q1	TIP-42A Power transistor, TO-220	
Heatsink	20 W	Digi-Key or Jade
Heatsink	3 W 24/28 volts only	Digi-Key or Jade
U1	MC3403 quad opamp	
U2	LM317LZ progressive voltage regulator	
U3	UC3906	Jade or Active Electronics
U4	LM317T progressive voltage regulator	
J2,J3,J4	4-terminal screw-type terminal strip, pc mount 0.100 inch	Mouser or Jade
J1	3-terminal screw-type terminal strip, pc mount 0.100-inch centers	Mouser or Jade
T1	Transformer For 12 or 14-volt battery, 16 VAC; for 24 or 28-volt battery, 28 VAC; for 6-volt battery, 10 VAC	Digi-Key or Jade

is more than sufficient, but don't forget about the heat lost in that resistor—it can get quite warm if it's too low a wattage. The charging setpoints will be affected slightly, but probably not seriously enough to justify changing the programming resistors in the controller. Using this method, a bank of batteries can be kept ready to go, all maintained by one controller. This is justification for one high-current controller, rather than a series of smaller ones.

Safety

As is true with any power system, certain precautions are necessary. Battery power sys-

Parts List, 5-amp Controller

Complete kits, including the enclosure, meter, pc board, transformer, and all other parts are available from JADE PRODUCTS, Inc. See ads in *QST*, or call 1-800-JADE PRO (1-800-523-3776).

Individual parts are also available from JADE PRODUCTS, Inc., or as indicated below.

All resistors are 1/4 watt, 1 percent, unless otherwise noted.

Designator	Item	Source
PC board	Part no. 31-00004-00	Jade Products, Inc.
R21	8.2 k, 1 W, 5%	Jade or Mouser
RT	510 ohm	
PTC	RUE800	Ray-Chem, available from Sager or Jade
D5,D6,D7	1N4148 general purpose diode	
D9,D11,D14		
R11	240 ohm, 5%	
R1	6.65 k	
RSA,RSB	0.1 ohm, 1 W	
DB1	10-amp rectifier	Jade, Mouser
D8,D13	6-amp silicon rectifier	
D10	1N5401 4-amp silicon rectifier	
F1	5-amp fuse	
R10,R19	90.9 k	
R17		
R16	1.05 k	
C1	6800 μF/63 volt	
C2,C3	0.22 μF/100 volt	
C4,C5	0.1 μF/100 volt	
LED 1-4	2 green, 1 amber, 1 red	Individuals, or single package from Jade
Q1	MJ900 Power Transistor, TO-3	
Heatsink	50 W	Digi-Key or Jade
U1	MC3403 quad opamp	
U2	LM317LZ progressive voltage regulator	
U3	UC3906	Jade or Active Electronics
J2,J3,J4	4-terminal screw-type terminal strip, pc mount 0.100-inch	Mouser or Jade
J1	3-terminal screw-type terminal strip, pc mount 0.100-inch centers	Mouser or Jade
T1	Transformer: for 12- or 14-volt battery, 16–18 VAC	Jade or Mendelson

tems have two unique situations that deserve special attention.

First and foremost, these systems are very high-current sources of energy. You must be careful to place the batteries and all associated wiring in such a way as to avoid shorts between the positive and negative terminals. Large battery systems have enough energy stored to easily melt large wrenches and screwdrivers. Fuses and good-quality circuit breakers are a must. Always connect the positive battery terminal first to prevent accidental shorting of tools to the ground bussing.

Second, when performing high rates of

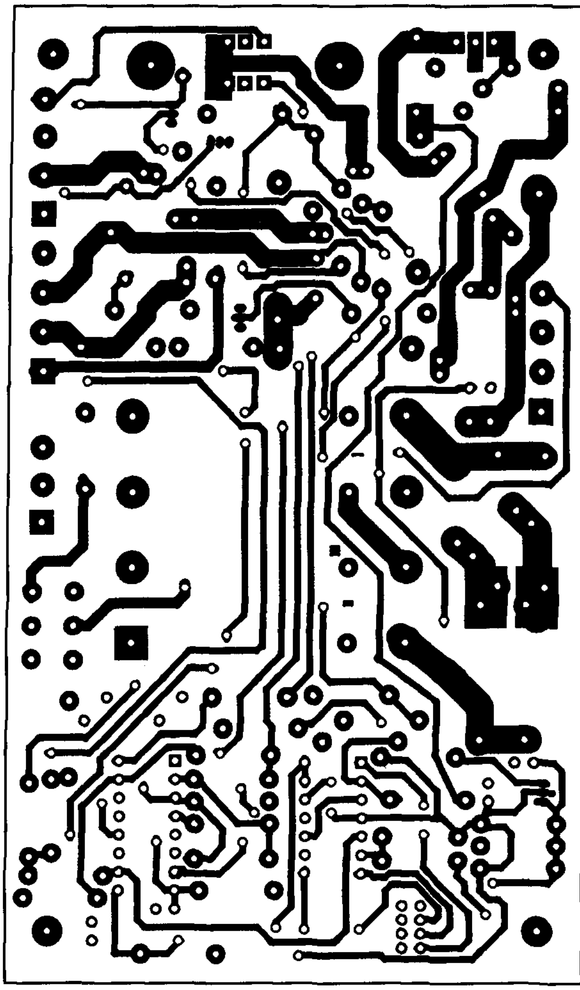

Figure 9. PC board bottom layer.

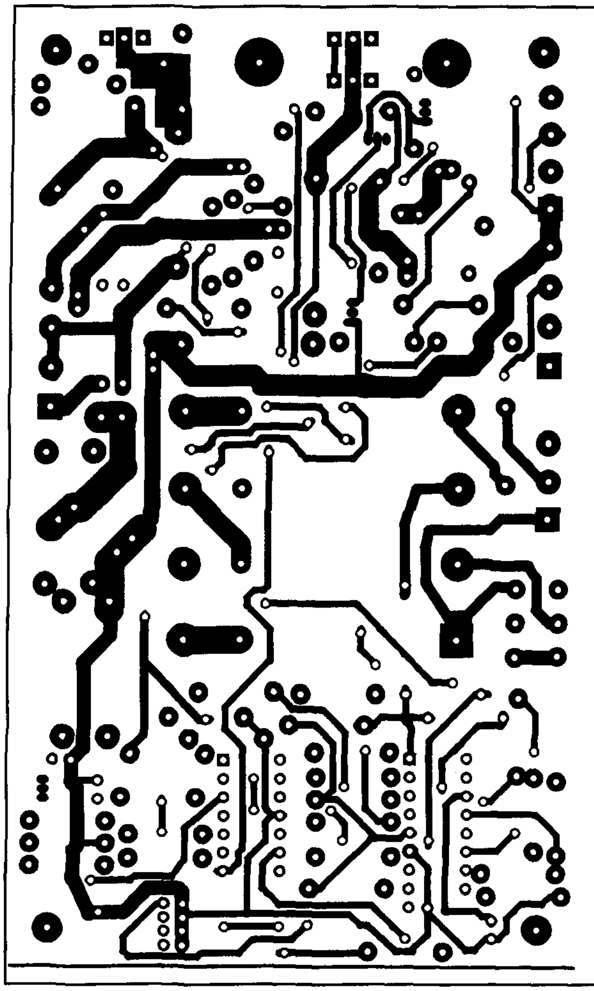

Figure 10. PC board top layer.

charging, provide proper ventilation—especially for vented batteries. High charging rates can create gases that must be ventilated. These gases are not only dangerous, they tend to eat up cloth in furnishings and curtains. Usually, when charging at rates of 1 amp or less, this isn't a particular concern.

Construction notes

A double-sided board for this charger is available from Jade Products, Inc. Jade also offers a complete parts kit. You can also make your own boards using the pc art found here. **Figure 8** is a pictorial parts layout for the pc board. **Figures 9** and **10** are one-to-one artwork for the bottom and top views of the board. The **Parts Lists** provide component information for both the 1- and 5-amp version of the controller and ordering information for boards and kits.

Conclusion

Battery power can be substantial, and can offer the average amateur user plenty of energy if proper planning and charging schedules are maintained. It can be a real joy to have the main power go out in a storm and have the station keep on "going and going and going."

Thanks

Special thanks to Warren Dion, N1BBH, for his encouragement and to Jane, KA1FUN, for her support and abilities in making this controller a reality. ■

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MODELING AND UNDERSTANDING SMALL BEAMS: PART 5

The ZL Special

When George Prichard (ZL3MH, later ZL2OQ, now deceased) introduced two-element horizontal phased arrays in 1949, they promised to overcome all the shortcomings of early homebrew Yagis.[1] Preliminary experimental results by F.C. Judd, G2BCX, who dubbed the antenna the "ZL Special" in honor of Prichard's work, seemed to indicate gains as high as 7 dBd and front-to-back ratios as high as 40 dB.[2] Moreover, the antenna was relatively simple to construct. Two half-wave elements, separated by about 45 degrees relative to the frequency of choice and connected by a phasing transmission line with a half twist, would produce an array phased 135 degrees with maximum gain and a deep null to the rear. **Figure 1** shows the general outline of the antenna, which uses either straight or folded dipoles.

The variability of success in replicating the claimed results has been exceeded only by the variety of explanations of what makes a ZL Special work. Moxon and Lewallen have pointed out that the success of any phased array depends, not upon shifting the impedance of an element, but upon establishing correct current

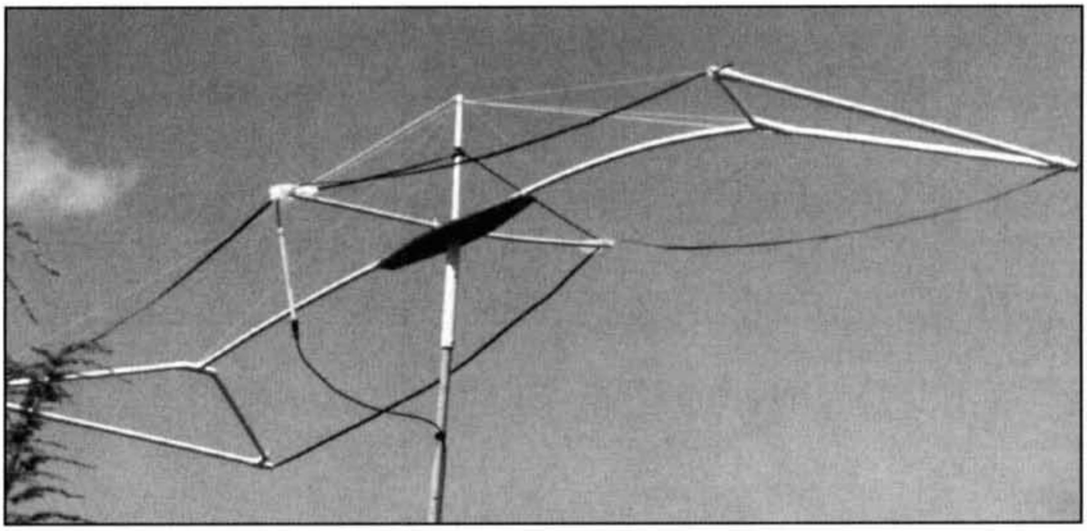

Photo A. Single mast support system has inner arms of Schedule 40 PVC and outer triangular sections of PR 315 PVC.

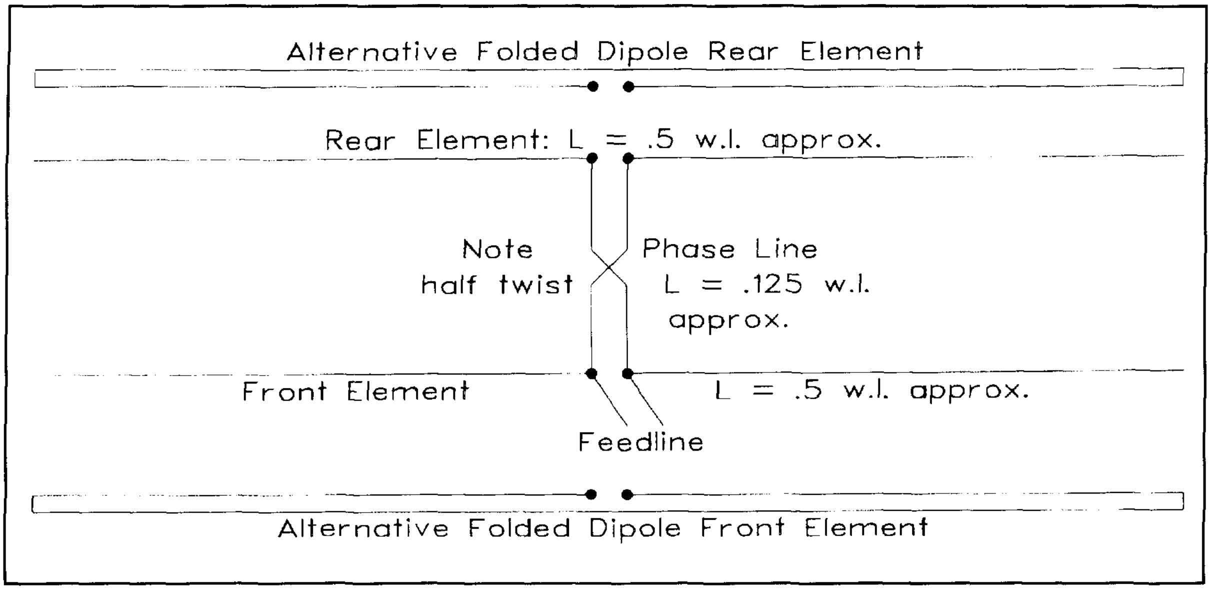

Figure 1. The basic construction of a ZL Special horizontal 2-element phased array.

magnitude and phase angle relationships between the two elements. Indeed, Moxon found that successful ZL Specials were more likely the result of accident than engineering—although Lewallen succeeded in designing replicable and reliable equal-length element models using "twinlead" for service as "Field Day Specials."[3]

It would be very easy to lose ourselves in the history of misconceptions regarding the ZL Special within the amateur community. Let's look instead at a (not THE) conception of the ZL Special that permits one to design an antenna that works as predicted. The design technique involved combines data supplied by antenna modeling programs, such as NEC and MININEC, with further algebraic analysis to produce an accurate model of both the geometric and the phasing dimensions of the ZL Special problem.

The background for ZL Special analysis

We can reduce the ZL Special problem to an orderly series of propositions and explanations.

1. *The significant reason for phasing two horizontal half-wavelength elements is front-to-back ratio, not gain.* Two phased half-wavelength horizontal elements will not significantly exceed the gain of a two-element Yagi. For reference, the performance figures of the modified W6SAI beam appear in **Table 1**. Although two-element Yagis with higher gain are possible, they sacrifice even the modest front-to-back ratio of the Orr beam.

The rationale for designing a phased array is to improve the front-to-back ratio of the antenna for QRM reduction. Phasing promises, in the abstract, to produce a deep rear null, while preserving the gain obtainable with a two-element Yagi. **Figure 2** compares the plots (35 feet above real ground) of the reference Yagi and a modestly well-designed ZL Special.

2. *We may think of the ZL Special as a "-45 degree" antenna.* Traditionally, we considered the ZL special as two parallel horizontal elements connected by a short (about 45 degree) phaseline with a half twist. Thinking in impedance terms, where all values reappear every half wavelength, we subtracted the half-twist line from 180 degrees to obtain 135-degree phasing. However, we can make two modifications to this traditional view.

First, we may think of the antenna in terms of current phase shifts rather than impedance phase shifts. Current magnitude-phase combinations occur only once per wavelength along a transmission line. Although full-length, 135-degree lines will achieve the desired phasing for well-designed models, a 45-degree length of phaseline with a half twist is not the equivalent of a 135-degree line with respect to current.

Second, for modeling purposes, we may move the half twist of the phase line anywhere along the line—including the point of junction with the rear element. In modeling terms, this move means twisting the element. In practical terms, if the front element is modeled in increasing length values (for example, from -8 feet to +8 feet), then the rear element is modeled in decreasing values (for example, from +8 feet to –8 feet). The two elements are 180 degrees out of phase and connected by an untwisted 45-degree length of phaseline.

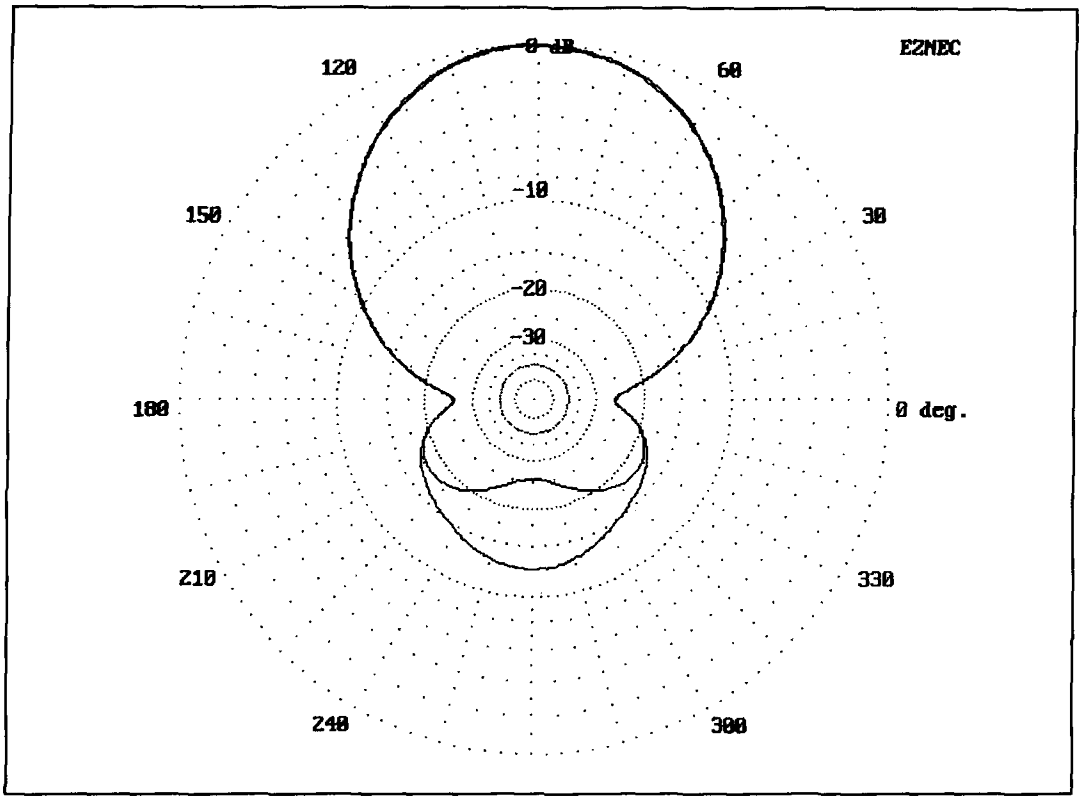

Figure 2. Comparison of azimuth plots for the reference Yagi and a ZL Special at 28.5 MHz, 35 feet above real medium earth.

With respect to the front element, the rear element is ideally current-phased –45 degrees (or 315 degrees). The model will now return correct values for calculating voltage and current along the phaseline, with no change in the impedance transformation. However, impedance transformation is largely incidental to understanding the ZL Special.

3. *For any two close-spaced, near-resonant elements, there is a value of current magnitude and phase for each element that will yield a deep null to the rear.* The values of current phase relative to the front element are roughly proportional to the spacing between elements. **Figure 3** shows the results of modeling half-wavelength elements for maximum front-to-back ratio. The precise angles required by the front and rear current depend to some degree

Wide-Band 2-Element Yagi Performance

	Antenna Dimensions	**Driven Element Length**	**Reflector Length**	**Element Spacing**	**Material Aluminum**
	DE + Ref	16.0'	17.5'	4.3'	1" dia.
Free Space:					
Frequency (MHz)	28.00	28.25	28.50	28.75	29.00
Gain (dBi)	6.7	6.5	6.3	6.1	5.9
F-B ratio (dB)	10.3	11.0	11.2	11.0	10.6
Impedance (R±jX)	24 - 17	28 - 8	32 + 1	36 + 9	40 + 18
35' over real medium earth:					
Frequency (MHz)	28.00	28.25	28.50	28.75	29.00
Gain (dBi)	12.1	11.9	11.7	11.5	11.4
F-B ratio (dB)	11.7	12.5	12.5	11.9	11.1
Impedance (R±jX)	26 - 18	30 - 9	34 + 0	38 + 8	42 + 16

Table 1. Performance characteristics in free space and at 35 feet over real medium earth of a wide-band 2-element Yagi using a driven element and a reflector.

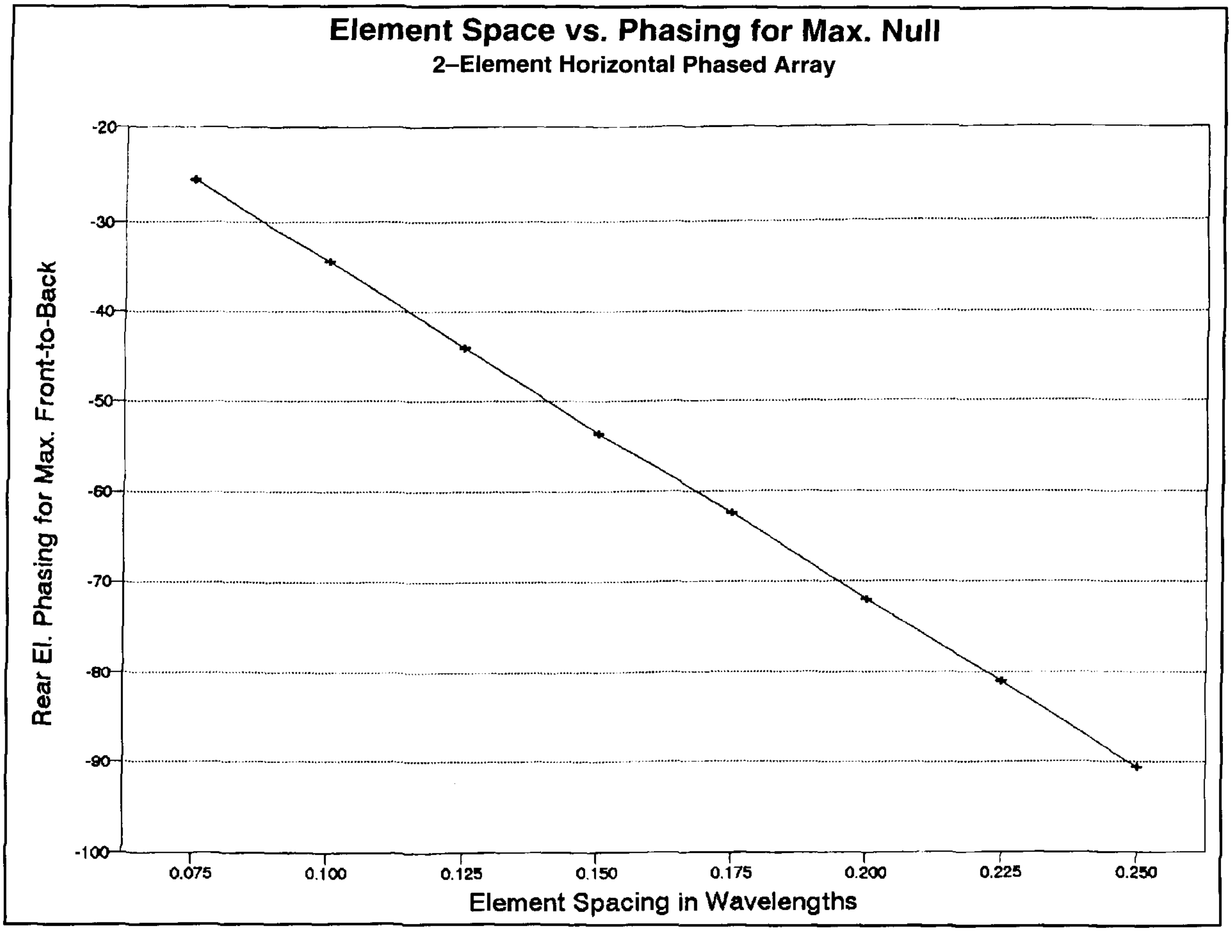

Figure 3. Graphic representation of the relationship between ZL Special element spacing and the phase angle required for maximum front-to-back ratio.

on the antenna geometry and may vary slightly from those graphed.

The graph dispels the idea that the two-element horizontal phased array is in any sense either a 135-degree or a –45-degree antenna. Within reason, there is a continuum of usable spacings and phasings. Consequently, the rationale for using wide-spaced planar folded dipoles for elements is lacking, and computer models detect no advantage for that geometry.

Figure 3 also indicates why many hams obtain usable results from casually designed ZL Specials—even those somewhat off the critical marks. **Figures 4** and **5** graph the results of modeling phased arrays at increasing departures from the optimal current phasing and the optimal current magnitude (relative to a front element current value of 1 at 0 degrees). If we arbitrarily set 20 dB front-to-back ratio as the minimum mark of an improved two-element array relative to the standard Yagi, then ZL Specials may depart considerably from optimal values and still meet the criterion.

4. *NEC and MININEC models using separate front and rear element sources are "forced" and may not be amenable to phaseline construction.* By judiciously arranging the antenna geometry (element length, diameter, and spacing) and the relative current magnitudes and phase angles, we may obtain a deep rear null in many antenna models. In general, such antennas rarely translate into arrays that work with phasing lines of the ZL Special sort.

Virtually any forced or two-source model can be built successfully under the condition that each element can be supplied with the correct magnitude and phase angle of current. Perhaps the only practical way to achieve this goal is through a lumped-constant network.

5. *Horizontal two-element phased arrays with phaselines are heavily interactive at all points of measurement.* Basic antenna geometry consists of the element diameters and their lengths (both absolute and relative to each other) and the spacing between elements. Slight variations in any parameter yield different values (magnitude and phase angle) of voltage, current, and impedance at the element feedpoints. The rear element values undergo transformation along the phaseline, depending upon

the characteristic impedance and the velocity factor of the transmission line used. The phaseline front terminal values combine with the front-element values to produce a feedline matching situation.

NEC and MININEC 2-source models calculate the feedpoint values of magnitude and phase angle for voltage, current, and impedance for each element. Moreover, for available transmission lines—and for those one might build—we know the characteristic impedance and the velocity factor. Therefore, it's possible to analyze proposed ZL Special designs to evaluate their feasibility and likely performance and to adjust the design to a level of satisfactory performance. The following procedure permits some precision in the design process.

Analyzing ZL Special designs

The analysis of two-element phased arrays with phaselines is a stepped procedure that uses the values of voltage and current magnitude and phase provided by a two-source model derived from NEC or MININEC analysis.[4] **Table 2** lists the meanings of the terms in the equations below as a handy reference. Most two-source models used to obtain values for the following analysis will normally designate the Element 1 current as 1 at a phase angle of 0 degrees and the Element 2 current as a set of values optimized by trial. The magnitude of the rear element current will be close to 1 and the phase angle will be close to the value corresponding to the element spacing, as found in **Figure 1**. Alternatively, one may use a front element current value of 0.5 and a correspondingly adjusted rear element current close to 0.5.

1. For any antenna geometry that yields a "perfect" ZL Special, the voltage at the front element feedpoint is identical to the voltage at the input end of the phaseline connected to the rear element. We may use this fact as a starting point in our analysis of the antenna design, as it provides the necessary third term (in addition to the values of voltage and current at the rear element feedpoint) for calculating either the characteristic impedance of the phaseline or its length, where the other is given. The basic formula for calculating the voltage along a lossless transmission line is given by **Equation 1**:

$$E_{in} = E_L \cos\left(2\pi \frac{\ell}{\lambda}\right) + jI_L Z_o \sin\left(2\pi \frac{\ell}{\lambda}\right)$$

where E_L and I_L are the rear element feedpoint values, E_{in} is the front element feedpoint voltage value, and the parenthetical expressions represent the phaseline length. We may simplify calculations by precalculating the line length into radians to obtain ℓ_r.[5]

Equation Terms

E_{fr}	Voltage at the front element; appears as Element 1 voltage in modeling program outputs; corresponds to E_{in} in general equations for transmission lines
I_{fr}	Current at the front element; appears as Element 1 current in modeling program outputs
E_{rr}	Voltage at the rear element; appears as Element 2 voltage in modeling program outputs; corresponds to E_L in general equations for transmission lines
I_{rr}	Current at the rear element; appears as Element 2 current in modeling program outputs; corresponds to I_L in general equations for transmission lines
Z_{rr}	Impedance at the rear element feedpoint
I_{in}	Current at the input end of the phasing transmission line; corresponds to I_{in} in general equations for transmission lines
E_{fp}	Feedpoint voltage, equals E_{fr} in "perfect" models of ZL Specials
I_{fp}	Total current at the antenna system feedpoint
Z_{fp}	Impedance at the antenna system feedpoint
R_{fp}	Resistive component of the feedpoint impedance, Z_{fp}
X_{fp}	Reactive component of the feedpoint impedance, Z_{fp}
I_{r2}	Recalculated rear element current
ℓ_f	Length in feet
ℓ_m	Length in meters
ℓ_d	Length in electrical degrees
ℓ_r	Length in radians
Z_O	Characteristic impedance of the phaseline
VF	Velocity factor of the phaseline

Note: Each term for E, I, and Z will have an associated phase angle, θ.

Table 2. Terms of equations used in the analysis of horizontal 2-element phased arrays using phaselines.

Because we cannot calculate the line length and Z_O simultaneously, we must assume one or the other. Letting the line length equal the element spacing is most convenient. We can always set up a small utility program in BASIC to step the calculation through several plausible values of line length, each of which will require a different Z_O. We must also make a judicious guess as to the likely velocity factor of the line. In general, if the proposed ZL Special design uses straight dipoles, use a figure in the 0.67 to 0.7 range, as the phaseline will likely have a low Z_O. If the design uses folded dipoles, an

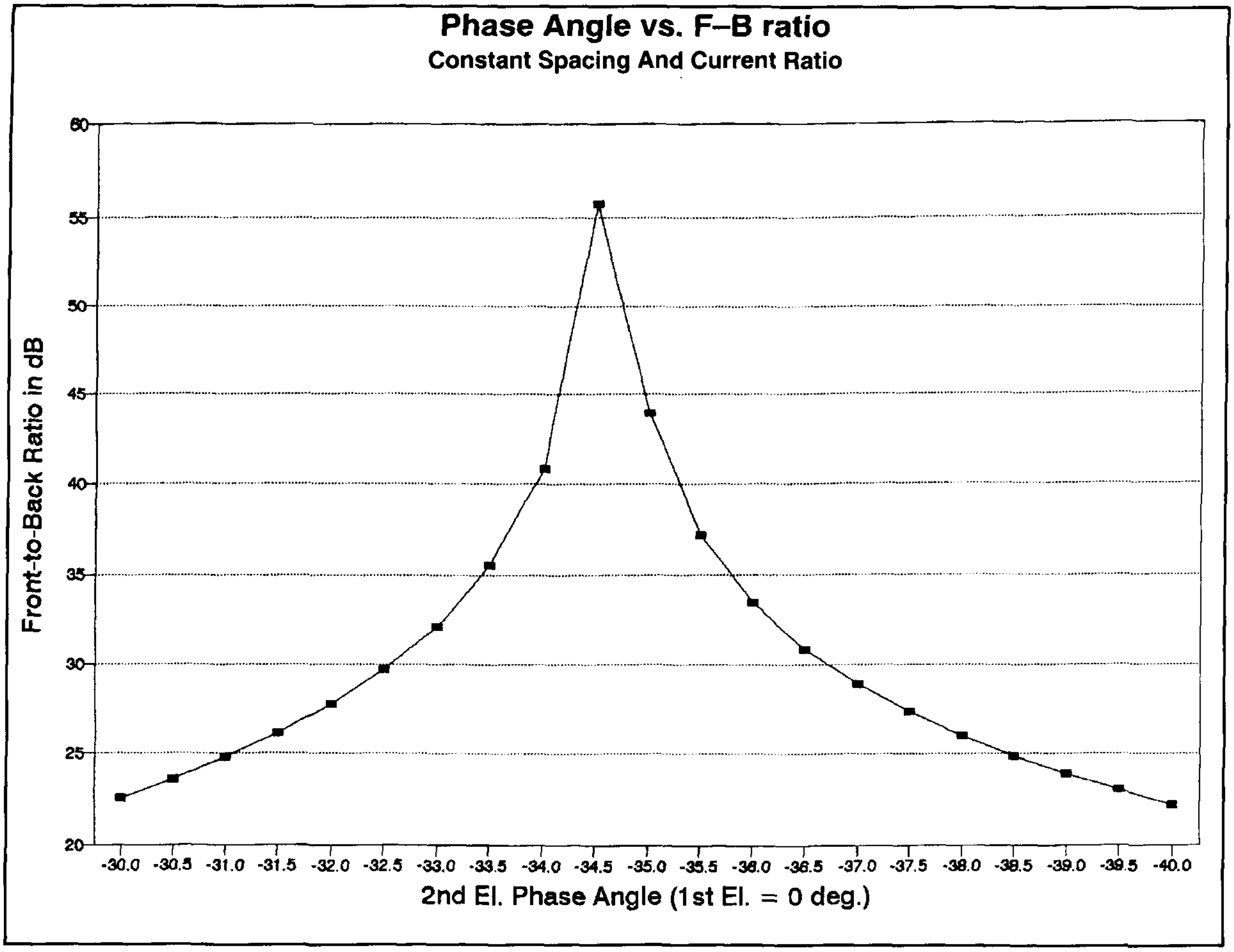

Figure 4. Front-to-back radio versus phase angle for two-element arrays.

initial velocity factor of 0.8 will serve because the range of the phaseline Z_O will be from about 150 to 350 ohms.

If we select ℓ_r and VF, rewrite the terms for front and rear element values, and solve for Z_O, we obtain **Equation 2**:

$$Z_o = \frac{E_{fr} - E_{rr}\cos\ell_r}{jI_{rr}\sin\ell_r}$$

If the array design is "perfect," it will require a phaseline with line length ℓ_r and the characteristic impedance, Z_O, in order to provide the correct phase and magnitude shift of current to the rear element.

2. To understand the conditions at the antenna feedpoint, we must also know the current at the input end of the phaseline. We may obtain this value from the standard equation for calculating the current along a transmission line (written here in terms of front and rear elements):

$$I_{in} = I_{rr}\cos\ell_r + j\,\frac{E_{rr}}{Z_o}\sin\ell_r$$

The value of current obtained, along with its phase angle, will also be crucial in evaluating the proposed array design.

3. For the array, if perfect, the total current at the feedpoint is the sum of currents in the two branches—namely, the front element and the phasing line input end, or:

$$I_{fp} = I_{fr} + I_{in}$$

This equation, of course, is for a vector sum.

The phase angle of the total feedpoint current represents in "perfect" models the appropriate source current phase angle to obtain a forward element current phase angle of 0 degrees and a rear element current phase angle of the value obtained from the original model. If fed with a current at 0 degrees phase angle, the antenna forward element will show a phase angle shifted in the positive direction by the amount of the phase angle of I_{fp}, with the rear element current shifted positive by the same amount. The net difference between forward and rear element current phases will remain the same.

4. We may obtain the feedpoint impedance from the front element voltage and the feed-

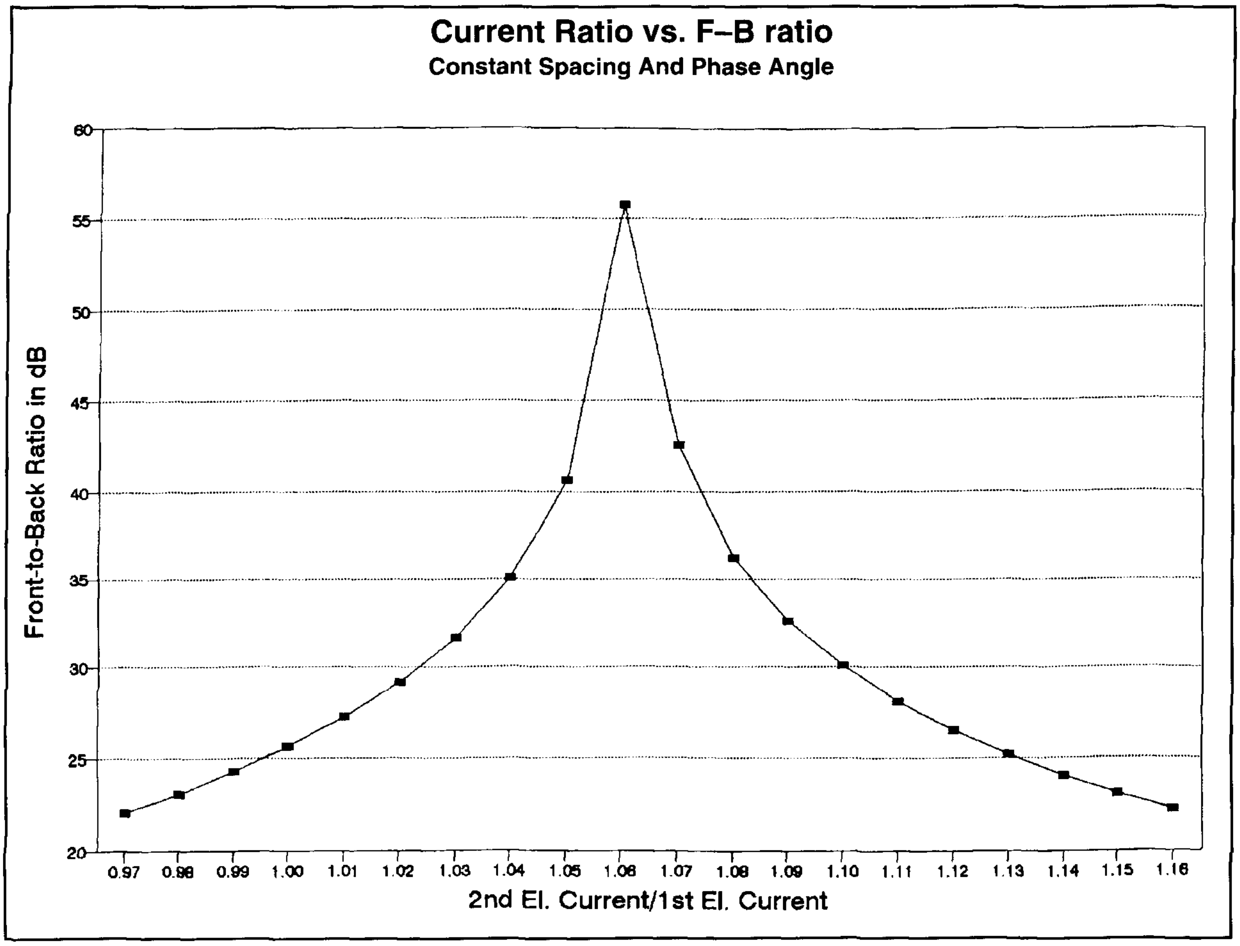

Figure 5. Front-to-back ratio versus current ratio at element feedpoints for two-element arrays.

point current, along with values for the resistive and reactive components:

$$Z_{fp} = \frac{E_{fr}}{I_{fp}} \qquad R_{fp} = Z_{fp}\cos\theta_{Zfp} \quad X_{fp} = Z_{fp}\sin\theta_{Zfp}$$

The calculation of Z_{fp} is, again, a matter of vector division involving the subtraction of I_{fp}'s phase angle from the phase angle of E_{fr}. R_{fp} and X_{fp} provide the values of resistance and reactance to be matched to the feedline for the system.

5. The preceding steps provide the crucial data for a "perfect" phased array. To test the design's feasibility, simply recalculate the rear element current, I_{r2}, using the calculated value of I_{in} and Z_O, along with E_{fr}. Use the standard equation (with the terms rewritten for the present problem).

$$I_{r2} = I_{in}\cos\ell_r - j\,\frac{E_{fr}}{Z_o}\sin\ell_r$$

If the model's chosen geometry is perfect, then this calculation will simply return the current magnitude and phase angle of I_{rr}. Anything less than perfect will show a divergence between I_{r2} and I_{rr}, especially with respect to the phase angle.

Evaluating ZL Special designs

The calculations above provide a significant body of data by which to evaluate the feasibility of a proposed ZL Special design. **Table 3** describes seven models for which **Table 4** provides selected results. The results appear in three groups. The first data group comes from two-source models and provides the current magnitude and phase relationship between the elements, along with the models' projected front-to-back ratio. The second data group comes from calculations in accord with the equation just described, listing the output Z_O, the return current phase (and its difference from the design value), and the calculated feedpoint impedance. The last data group comes from applying the basic antenna model to a version of NEC capable of handling transmission lines

Test Models of ZL Specials

Name	El. Type	Front El. L_{ft}	Rear El. L_{ft}	El. Spacing L_{ft}
Folded Dipole Models				
Short	1" Cu	15.36'	15.68'	3.86'
Off Z	1" Cu	16.06'	16.80'	4.31'
1"	1" Cu	16.16'	16.16'	4.27'
3/8"	3/8" Cu	16.26'	16.26'	4.27'
Straight Dipole Models				
#12	#12 Cu	16.42'	16.42'	3.46'
5/8"	0.625" Al	16.04'	16.04'	3.46'
3/4"	0.75" Al	16.00'	16.00'	3.46'

Notes: Cu = copper; Al = aluminum. Folded dipole element type dimension = width of the folded dipole; straight dipole element type dimension = element diameter. The 1" folded dipole approximates the use of 450-Ω ladder line as the element, while the 3/8" folded dipole approximates the use of 300-Ω twinlead as the element.

Table 3. Test models of ZL Specials discussed in text.

within the model.[6] Using one or more values for the phaseline Z_O, the data group provides the projected front-to-back ratio and the feedpoint impedance. All the antennas were modeled over real medium earth using NEC's more accurate ground modeling capabilities.

The "Short" model represents a casual design I found in the literature. Although model calculations indicate a promising phaseline Z_O of about 269 ohms, which suggests the use of 300-ohm twinlead for both the elements and the phaseline, notice the phase differential between the design figure and the return calculation. In general, any difference greater than ±4 degrees or so is likely to bring disappointment. Moreover, as the phase differential between the design value and the return calculation increases, the feedpoint impedance values grow more inaccurate. Compare the calculated value with either of the test models to the right, noticing the subpar front-to-back figures along the way.

Perhaps what made this model attractive was the wide-band low SWR of the antenna. Frequency sweeping the 300-ohm phaseline model indicated that the antenna would show an SWR below 2:1 for over a MHz of 10 meters. Unfortunately, horizontal two-element phased arrays cannot be adequately designed by reference to SWR. Feeding the assembly must be the last design step, not the first.

The model named "Off Z" demonstrates another problematic situation. The two-source model and the calculations show that the design is quite feasible and capable of good performance, as indicated by the tiny 0.07-degree phase differential. However, the 194-ohm characteristic impedance of the recommended phaseline is uncommon, to say the least. Attempting to execute this model using the nearest common transmission line (300-ohm twinlead) as the phaseline results in a serious degradation of performance. Phaseline Z_O should be within approximately 10 percent of the calculated value for reasonably successful array performance. Unless you can build a short length of your own transmission line, many good ZL Special models must be set aside as impractical.

The two models we've evaluated so far used elements based upon Yagi theory: the rear element should—in a driven element-reflector design—be somewhat longer than the forward element. This mode of thinking is detrimental to ZL Special design. The remaining models in the group all use equal element lengths as a starting point. There are good reasons on occasion to alter the length of either (or both) the forward or the rear element, but those reasons have virtually nothing to do with the considerations crucial to Yagi design. We shall look at some design alterations after examining the better models on the list.

The 1-inch and 3/8-inch folded dipole models required care in selecting the current magnitude and phase angle for the rear element, while the straight dipole models were more quickly settled by letting the current ratio between elements be 1:1. Use of 0.5 A as the current value permits a more rapid correlation of values with

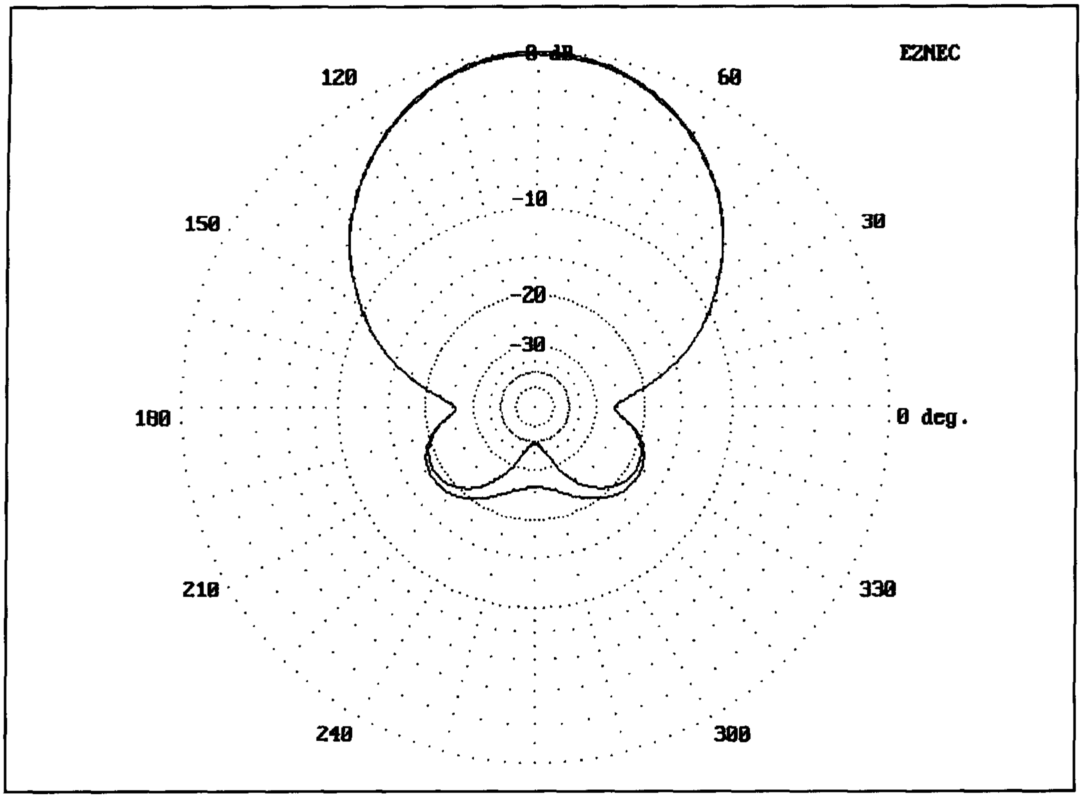

Figure 6. Comparative azimuth patterns for equal-length element and "improved" versions of the 5/8-inch straight dipole ZL Special (35-feet above real medium earth).

those of the NEC transmission line models using a source current value of 1 A. In actuality, the total antenna current for the antenna system is slightly higher than 1 A, because the phaseline transforms not only the current phase angle, but its value as well.

Both folded dipole models show similar results, despite their different lengths. Although the figure varies slightly as the length-to-diameter ratio changes, the folded dipole elements for a ZL Special should be about 2.44 percent shorter than a single self-resonant folded dipole at the frequency of interest. The #12 straight dipole model used elements only about 2 percent shorter than a self-resonant single dipole, while the tubular elements required a little under 2.9 percent shortening.

The 1-inch folded dipole model is interesting because it demonstrates the fall-off in performance (front-to-back ratio) as the phase differential between the design value and return calculation value increases. Although 30 dB is a respectable ratio, it's down nearly 10 dB from the two-source model with only a 1.74-degree phase differential. Greater attention to the rear element current phase angle would likely have resolved the difference, but also resulted in a different phaseline Z_O value. Compare this model to the 3/8-inch model for a closer correlation of all relevant values.

In practical terms, the differential is moot, as 330-ohm twinlead is not common. Both antennas promise very good performance with a 300-ohm phaseline, if a figure of 25 to 27 dB for the front-to-back ratio can be considered very good. Compared to the reference Yagi, the figure certainly represents an improvement that may be both detectable and desirable. Note that the phaseline meets the ±10 percent criterion mentioned earlier.

Feeding a ZL Special that utilizes folded dipoles and equal-length elements presents little problem. The resistive component of the feedpoint impedance presents a reasonable match to 50-ohm coax. The remnant inductive reactance can be canceled by the use of either a capacitive stub or a pair of capacitors—each with half the reactance value—in series with the two sides of the feedline at the feedpoint junction.[7] Indeed, it is characteristic of well-designed ZL Specials using equal-length elements to have similar numerical values for the resistive and reactive components of the feedpoint impedance; in other words, for the feedpoint impedance to have a phase angle approaching 45 degrees inductive.

Similar results can be obtained from straight dipoles and 72-ohm nominal twinlead. The three models differ only in the wire size used, with consequential differences in element

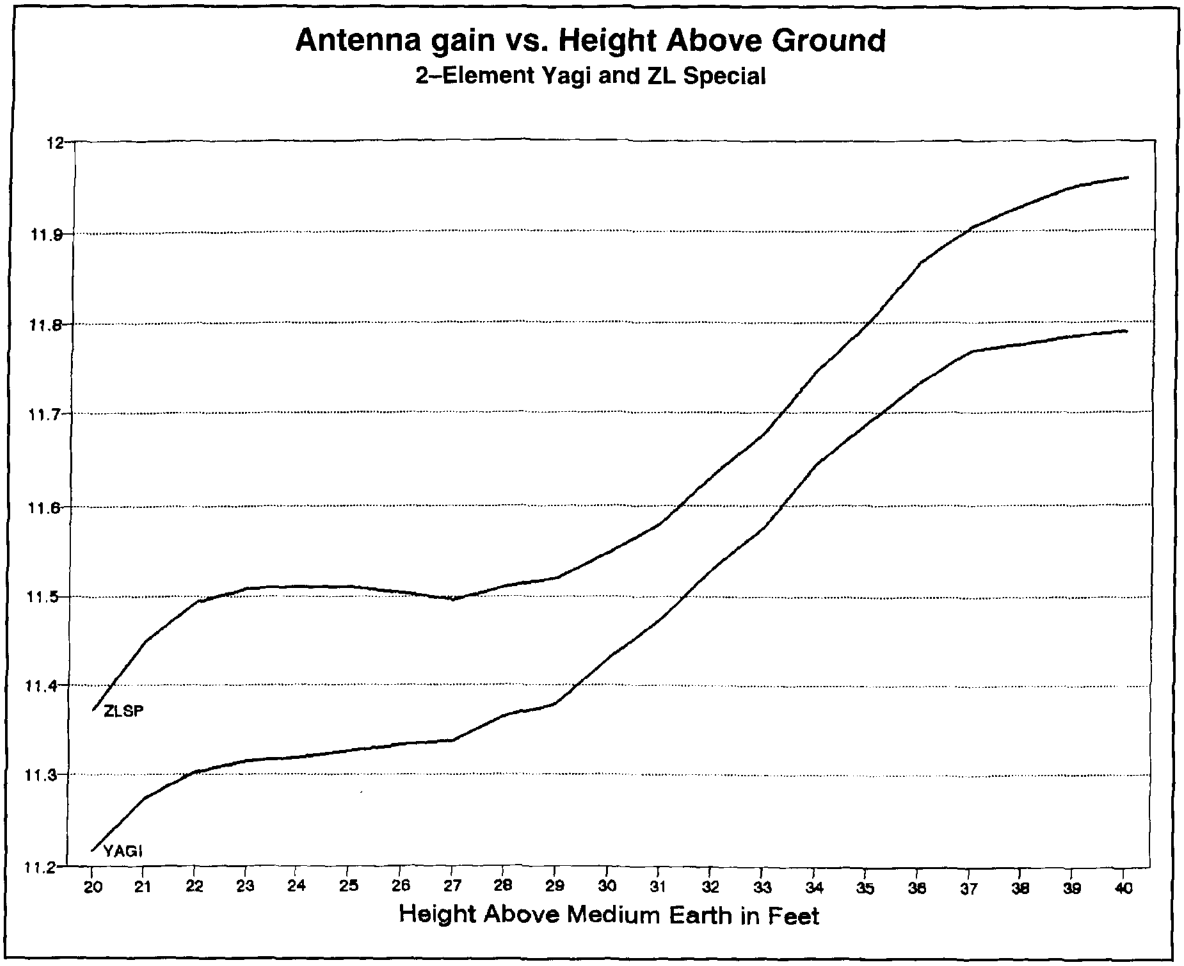

Figure 7. Yagi and ZL Special gain versus height above ground from 20 to 40 feet over real medium earth.

length. The calculated phaseline Z_O of 66.7 to 67 degrees departs from the twinlead impedance by only about 6 percent, and the transmission-line models of the antennas verify antenna performance. Unfortunately, the very low feed-point impedances require careful attention to both design and construction to minimize losses. A 71-ohm twinlead or a 75-ohm coax stub something over 4 feet long provides the required match to 50-ohm coax. Either a capacitive stub or a parallel capacitor is used to cancel the remaining reactance, which will be in the range of 150 to 200 ohms.

Improving ZL Special performance

One straightforward means of improving ZL Special performance is to construct a phaseline with a characteristic impedance and velocity factor that agrees with calculations, after fully optimizing a two-source model of the desired antenna. However, most builders will be limited to altering the antenna geometry in accordance with the available transmission lines. In general, there are only two methods of achieving this goal.

First, you may change the spacing. Unfortunately, element spacing is insensitive to change. Raising the required characteristic impedance of the phaseline for the straight dipole models demanded shortening the spacing to approximately 2.5 feet. Lowering the required line impedance of the folded dipole models demanded an increase in spacing to around 7 feet. Neither move seems very attractive mechanically.

Second, you may change the ratio of element lengths. Each model with equal-length elements was initially optimized with respect to element length for maximum front-to-back ratio. Only the ratio of element lengths remains to be changed in pursuit of a geometry that requires a phasing line of the desired characteristic impedance. The rule of thumb is this: to decrease the required Z_O, make the front element shorter than the rear element. To increase the required phasing line Z_O, make the front element longer than the rear element. The

Table 4. Some modeling and calculation results using test models described in Table 3.

Modeling and Calculation Results with Test Models

Model	< Two-Source Data		>	< Calculations				>	< Test Model Results			>
Name	**I @ El. 1**	**I @ El. 2**	**F-B (dB)**	**Zo Ω**	**Rtn I El. 2**	**Ph. Dif.**	**R**	**jX**	**Zo**	**F-B (dB)**	**R**	**jX**
Folded Dipole Models												
Short	0.5/0°	0.49/-38.7°	41.89	268.9	-63.61°	24.91°	55.8	-48.9	268.9	12.80	29.5	-18.1
									300	12.46	35.3	-12.8
Off Z	0.5/0°	0.49/-42.7	44.95	194.4	-42.63°	0.07°	52.3	36.3	194.4	45.38	52.4	36.3
									300	17.95	74.9	56.2
1"	0.5/0°	0.5/-42.9°	39.52	330.2	-41.16°	1.74°	40.8	53.4	330	30.12	43.3	51.3
									300	25.64	37.8	44.9
3/8"	0.5/0°	0.49/-42.7°	44.16	330.1	-42.69°	0.01°	42.0	42.7	330	44.19	42.0	42.6
									300	27.60	36.6	36.4
Straight Dipole Models												
#12	0.5/0°	0.5/-34.75°	29.61	66.9	-35.44°	0.69°	6.7	6.6	71	27.17	7.1	5.8
5/8"	0.5/0°	0.5/-34.75	26.06	67.0	-36.19°	1.44°	7.1	7.7	71	26.63	7.2	8.8
3/4"	0.5/0°	0.5/-34.75	25.66	66.7	-36.57°	1.82°	7.2	7.5	71	25.46	7.2	8.8

See Notes, Table 3.

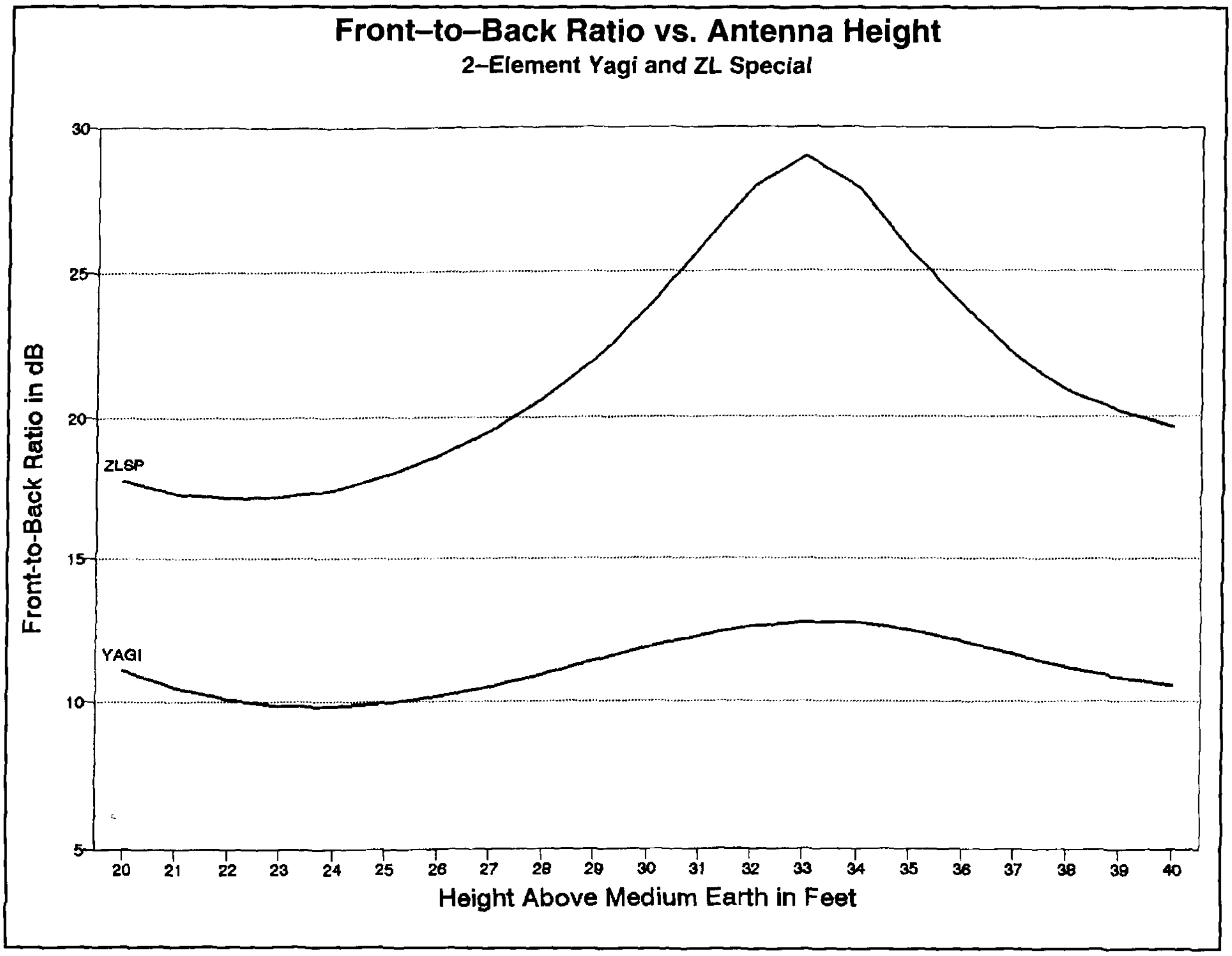

Figure 8. Yagi and ZL Special front-to-back ratio versus height above ground from 20 to 40 feet over real medium earth.

adjustments will be small if the original antenna requires a phaseline Z_O within 10 percent of the desired value. In addition, either or both elements may require adjustment.

Table 5 catalogs four improved models. Note that the folded dipole models have front elements slightly more than an inch shorter than the rear. Not shown are the new design values of rear element current magnitude and phase, which will change as the element-to-element ratio changes.

The straight dipole models show the reverse effect: to raise the required Z_O from 67 to 71 ohms, the rear element must be slightly shorter than the front element, with a consequential change in rear current magnitude and phase relative to the front element current. Because the curves approaching the maximum possible front-to-back ratio are steepest above 30 dB or so, very small changes in element dimensions produce large changes in front-to-back ratio.

Having shown that, and how it's possible to refine ZL Special performance by adjusting the antenna geometry, we must consider whether such a measure is worthwhile for the average home builder. **Figure 6** superimposes two of the straight dipole antenna patterns—one for equal-length elements, the other improved. Although there is some improvement in the overall front-to-rear pattern (taking into account the entire region from 180 to 360 degrees), the improvement isn't large compared to the initial improvement over the reference two-element Yagi.

Moreover, achieving the absolute maximum rear null in fixed construction may be beyond the building and measurement capabilities of most hams. Indeed, phased arrays with equal-length elements may have advantages that offset their slightly reduced front-to-back performance. Such an array is reversible if we attach, to both elements, ladder line feeders that are a multiple of a half-wavelength (adjusted for the velocity factor). One feeder is attached to the line to the transceiver, the other left open as an indefinitely large impedance that doesn't significantly affect antenna operation.

However, carefully pruning a ZL Special for maximum null at the design frequency does center the front-to-rear pattern within a desired frequency span. For a front-to-back null of over 40 dB, the front-to-back ratio degrades uniformly above and below the center frequency. On 10 meters, the front-to-back ratio is better than 25 dB 25 kHz each side of the design center and about 20 dB 50 kHz each side of the design center. Less careful pruning will likely improve the front-to-back ratio in one direction from the center frequency, but degrade it in the other down to about 15 dB.

Construction and placement notes

All the antennas in this analysis have been modeled at 35 feet above medium or average ground. More than many antennas, ZL Specials require modeling over real ground, rather than the construction of free space models, because they are somewhat sensitive to ground effects. This applies most especially to the array's front-to-back ratio.

Figures 7 and **8** graph the gain and front-to-back ratio, respectively, of the ZL Special (the 5/8-inch diameter straight dipole model), with comparable values for the reference Yagi provided as a standard. The gain curves are quite parallel. Their spacing is a graphing convenience; the difference in values makes little, if any, operational difference. However, the excursions in front-to-back ratio for the ZL Special are many times those for the Yagi. The curves are based on a single configuration for each antenna. While the Yagi shows a relative constancy of performance, the variability of the ZL Special's front-to-back ratio suggests that optimizing it for the anticipated height of use is in order.

As a further indication that Yagis and ZL Specials operate according to quite different principles once we move beyond the mutual coupling of elements, the correlation of feedpoint impedance and other parameters differs for the two antennas. ZL Special front-to-back peaks and nulls tend to correspond with peaks and nulls in the reactive component of the feedpoint impedance. For driven-element-reflector Yagis, the front-to-back peaks and nulls correspond with their counterparts in the resistive component of the feedpoint impedance. By way of contrast, to the degree they are detectable, gain peaks and nulls show a reverse correspondence.

There's little that anyone can add to the construction of ZL Special, whether using straight dipoles or folded dipoles. Straight dipoles lend themselves to the use of rotary beam techniques. One caution is required: do not permit metal antenna structural elements (such as a boom or mast) to disturb the balance of the currents in the phaseline. Moreover, the sum of 45 years of ZL Special construction wisdom dic-

Some Improved Test Models

Name	Type Wire	Front El. Lft	Rear El. Lft	El. Spacing (feet)	< ZoΩ	Calculations Rtn I El. 2	Ph. Dif.	R	jX >	< Zo	Test Model Results F-B (dB)	R	jX >
Folded Dipole Models													
1"	Cu	16.06'	16.16'	4.27'	300.2	-42.79°	0.01°	41.3	39.8	300	47.54	41.2	39.8
3/8"	Cu	16.23'	16.34'	4.27'	299.8	-42.53°	0.07°	41.4	38.0	300	43.20	41.5	38.0
Straight Dipole Models													
5/8"	Al	16.10'	15.98'	3.46'	71.0	-34.69°	0.31°	6.4	9.0	71	38.39	6.5	8.9
3/4"	Al	15.98'	15.78'	3.46'	71.2	-33.95°	0.80°	5.7	7.3	71	34.17	5.9	7.1

See Notes, Table 3.

Table 5. Modeling and calculation results using improved test models.

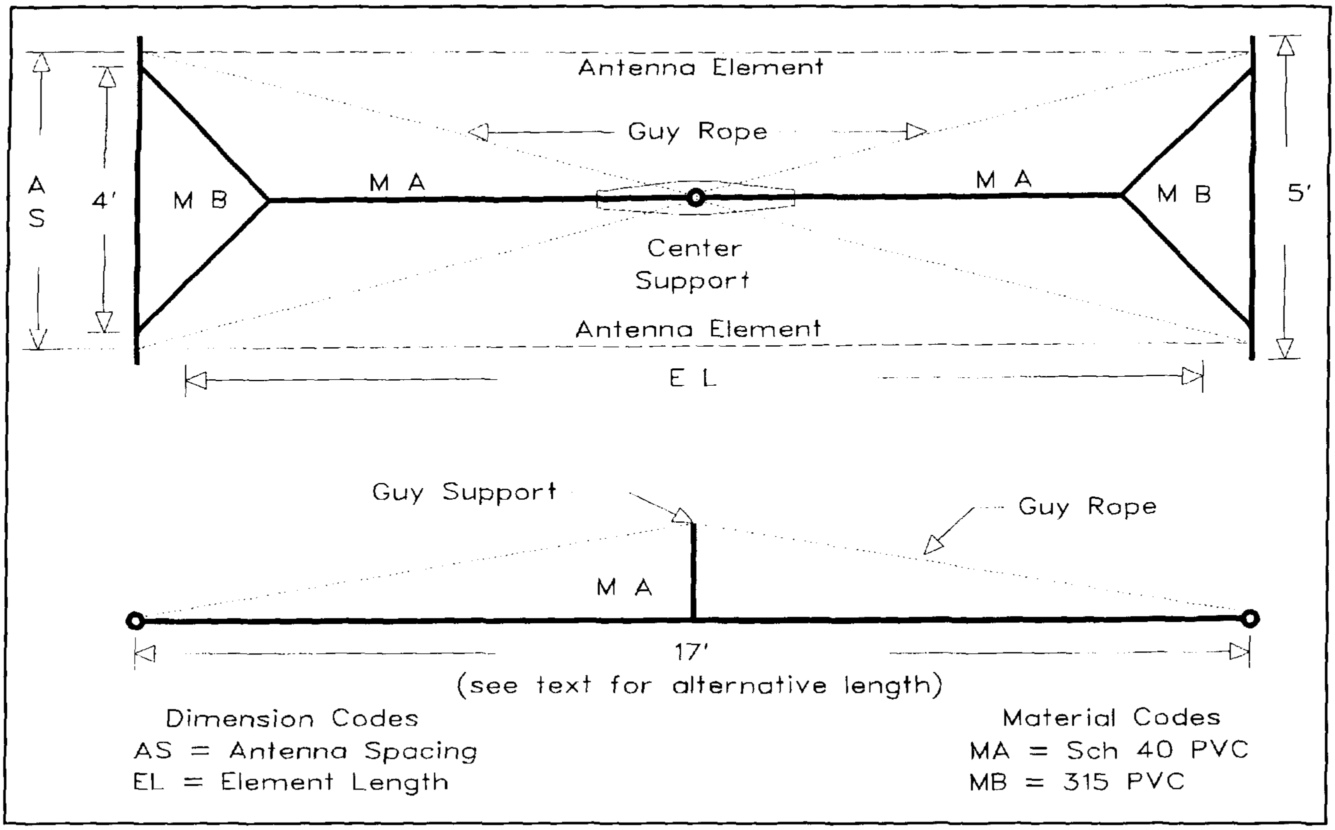

Figure 9. General sketch of a single-mast support structure for testing wire ZL Specials.

tates that we use parallel feedline, not coax, for the phaseline. A mixture of wood, PVC, and similar construction materials for the structural assembly can leave your twinlead phaseline unaffected. Unfortunately, the demise of 70-ohm twinlead as an easily obtained commodity has made the straight-dipole version of the ZL Special an endangered—if not an extinct—species of the antenna. What remains to build are twinlead folded dipole versions.

Use caution when buying materials for a folded dipole ZL Special. Belden 8230, the standard 300-ohm twinlead for many amateur applications, has #20 stranded conductors and a nominal velocity factor of 0.80. It is the basis for the models and the test antenna studied here. Many common local sources of supply for twinlead no longer carry equivalents of this transmission line. The foam lines they do carry often have no listed velocity factory, and it's unlikely that the figure will be 0.80. Velocity factor is important chiefly in the physical length of the phasing line, which is perhaps the most critical factor in building a ZL Special.

Decades ago, when bamboo was cheap, taping 300-ohm twinlead to support elements permitted folded dipole versions of the ZL Special to approximate rotary beam configurations. More recently, the idea of fixed beam installations, whether in an attic or in the field, has regained popularity—if for no other reason than necessity in today's tighter ham quarters. A twinlead ZL Special, following W7EL's lead, makes a good Field Day Special, because it rolls up into a small ball for transport. Elevated at the ends and pointed roughly toward the main body of hams to be worked, the antenna outperforms dipoles by a good measure. Coastal hams can use a single feedline version, while midwestern operators may opt for a reversible version.

As a test bed for validating modeling figures, I built the single-mast support system shown in **Figures 9, 10,** and **11** and **Photo A**. With inner arms of Schedule 40 PVC and outer triangular sections of lighter PR 315 PVC, the assembly permitted me to place practically no metal in the vicinity of the antenna elements or the phase line. Support arms for the center connections to each folded dipole are optional. If you use them, lightweight 1/2-inch nominal CPVC is recommended. All junctions are glued.

Although the assembly is a good bit more rigid than it appears at first sight, I don't recommend it for a permanent installation. The guys don't stabilize the structure in all axes and certain twisting motions are possible in high winds. In lighter winds, the structure is quite stable. Thus, it is adaptable to short-term portable operations if some of the junctions are only press-fitted into the couplings.

Those who wish to hang the elements from their ends might use the 17-foot length, because a 10-meter two-element phased array is just over 16 feet long. My own final version of the support system was about 15 feet, 9 inches long. The ends of each front-to-back arm were slit, with the twinlead pressed in place. A pair of holes punched in the insulation of the twinlead permitted the use of a cable tie to hold the element in place. The short ends sticking out beyond the limits of the structure were self-supporting and easily accessed for pruning.

The antenna tested was the improved 3/8-inch model in **Table 5**. The insulation on twinlead elements requires about 1 to 2 percent shortening (relative to the models) of the elements for resonance at 10 meters. (Note: the velocity factor of a transmission line used as a radiating antenna element isn't the same as the velocity factor of the material used as a transmission line. As a radiator, twinlead is just another type of insulated wire.) The final lengths for the test frequency of 28.5 MHz and a height of slightly more than 20 feet were 16 feet and 16 feet, 1 inch using Belden 8230. Feedpoint series capacitors are 300 pF in each leg of the feedline on the antenna side of a choke balun. Because the impedance at resonance is in the neighborhood of 40 ohms resistive, the lowest SWR doesn't necessarily indicate the frequency of the null, which will be at a slightly lower frequency. If heights other than 20 to 35 feet are used, these test numbers may be somewhat different.

Once pruned, the antenna worked as predicted, within the coarse methods available for tests. Point-to-point contacts established a front-to-back ratio at the design frequency that rivaled the Moxon rectangle. Performance held up across the first MHz of 10 meters, both in terms of anticipated front-to-back ratio and in terms of an SWR bandwidth within 2:1 limits. Unless one has a very special operating need, the extra work of obtaining a "perfect" null would not likely show up, as it is frequency specific and flattens rapidly with excursions away from the design frequency.

One ZL Special variant is especially apt for attic use (assuming the broad surface faces the best QSOs). W9BRD bent the ends of straight dipoles toward each other and phase fed the resultant assembly.[8] **Figure 12** shows the general outline of the antenna. The original design used equal-length elements and a system of volt-

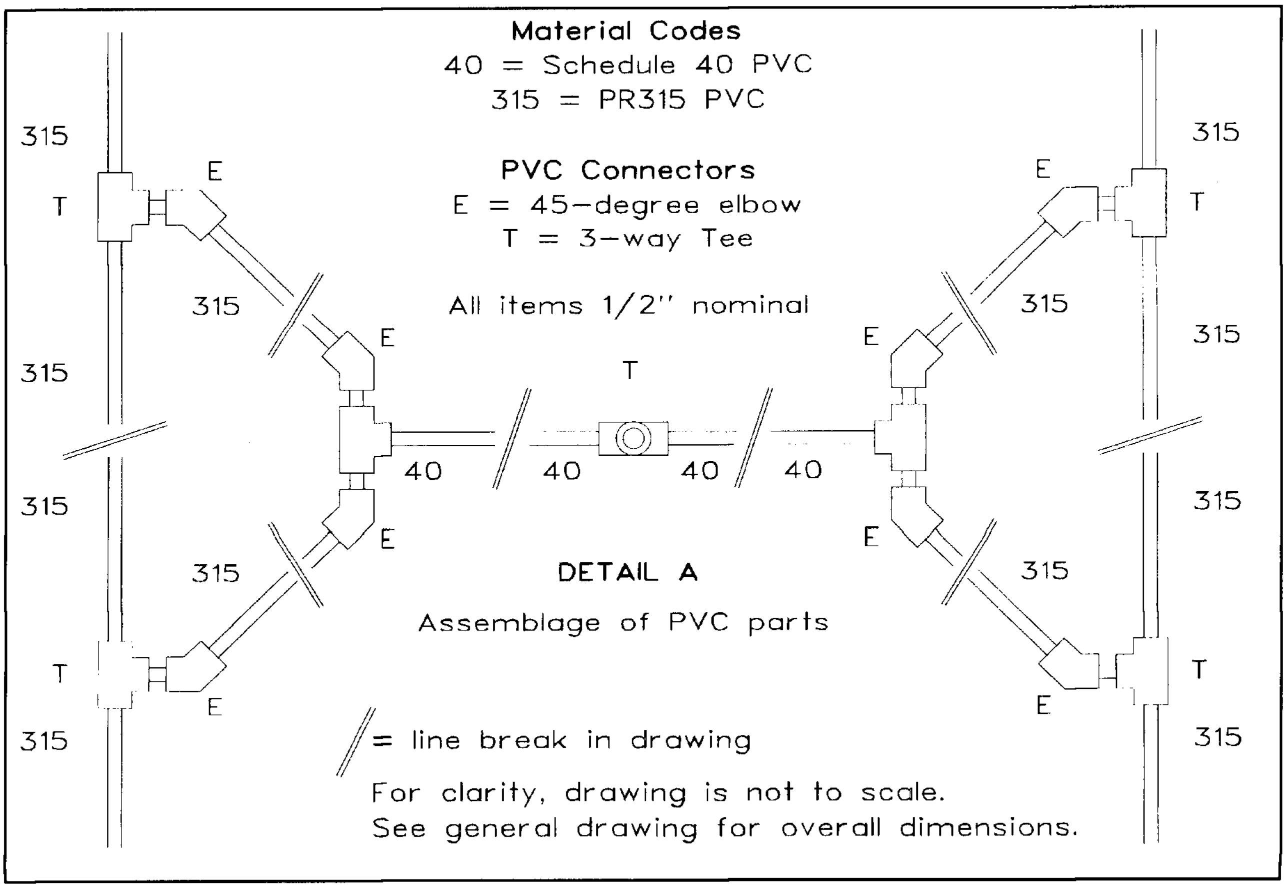

Figure 10. Detail A of the support structure, showing the combination of PVC materials used in its construction.

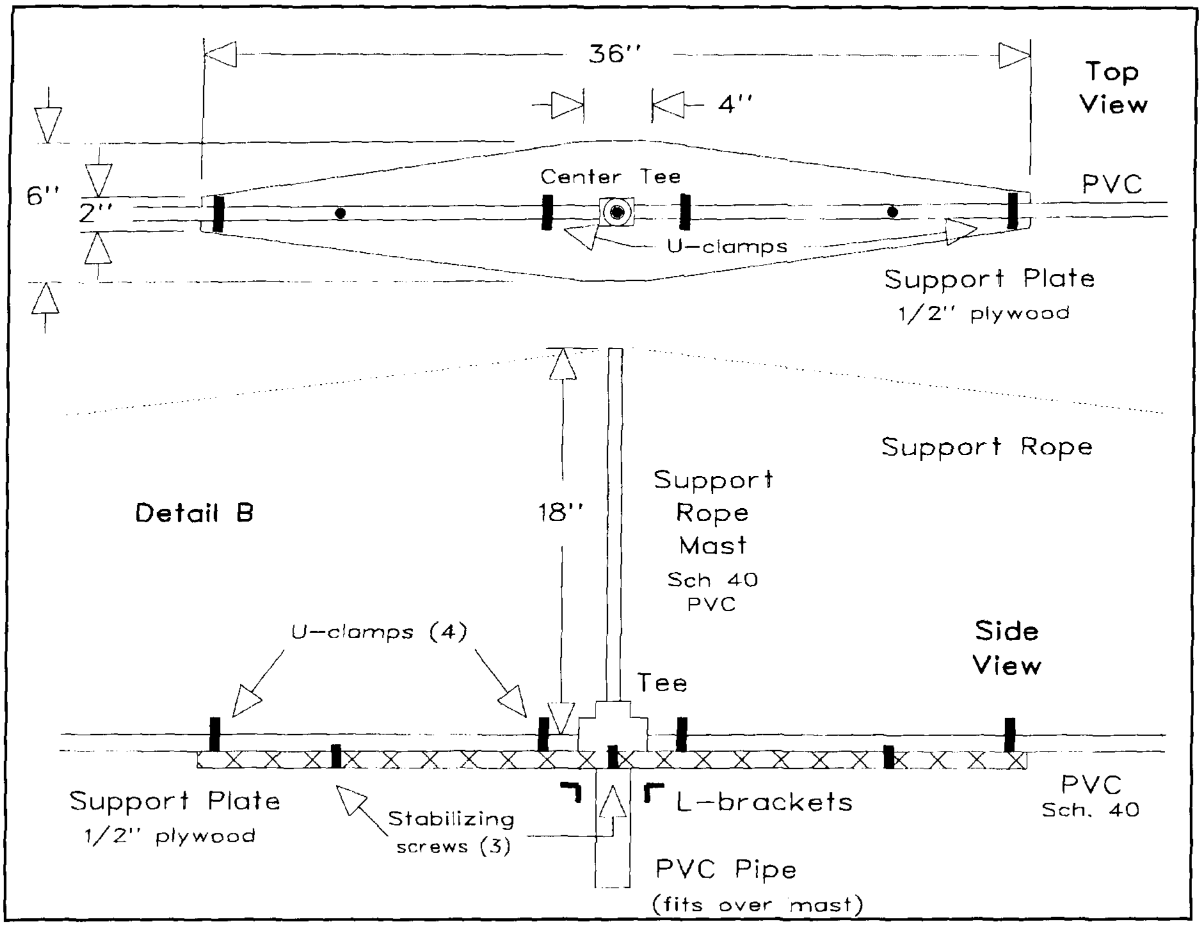

Figure 11. Detail B of the support structure, showing the center plate and mast connection.

age feeding a transmission line segment between the element ends on one side. The dimensions shown are for a modified version using #18 wire unequal length elements and a 71-ohm phasing line. The resulting feedpoint impedance is 33 + j45 ohms—a tolerable match for coax once the inductive reactance is canceled.

Figure 13 shows the pattern at both 20 and 35 feet above real medium earth for the 'BRD Zapper. Relative to a model with linear elements, the closed geometry of the 'BRD Zapper costs a little under 0.5 dB of gain. At the higher elevation, the worst rear lobe is down over 25 dB. At 20 feet (perhaps an average attic height), the front-to-back ratio drops to about 20 dB, although further refinement of the geometry may restore much of the dimple in the most rearward direction. Perhaps the only competitive small parasitical antenna in this respect is the Moxon rectangle. In fact, either antenna would make a good fixed beam for attic use, and the Moxon would be easier to build because it requires no phase line. The best reason for noting the 'BRD Zapper here is to demonstrate that the geometry of horizontal two-element phased arrays isn't exhausted by straight and folded dipoles.

In fact, this analysis of ZL Specials hasn't even come close to exhausting the possibilities for horizontal two-element phased arrays. The lure of indefinitely deep rear nulls is likely to keep the creative juices flowing in many a ham builder. Hopefully, this exploration into modeling and analyzing ZL Specials has added to a better understanding of the process. The operation of ZL Specials can be understood in terms of the voltages and currents at the terminals of each element and along the transmission line used to establish correct phasing. A combination of modeling and calculation makes the performance of a proposed version of the ZL Special far more predictable than was thought in the past. My hat is off to all those early experimenters who made workable ZL Specials while laboring under a limiting set of assumptions. That is a testimony to persistence of trial and error efforts.

Notes

Special thanks to Elaine Richards, News and Features Editor for PW Publishing Ltd., publishers of *Shortwave Magazine* and *Practical*

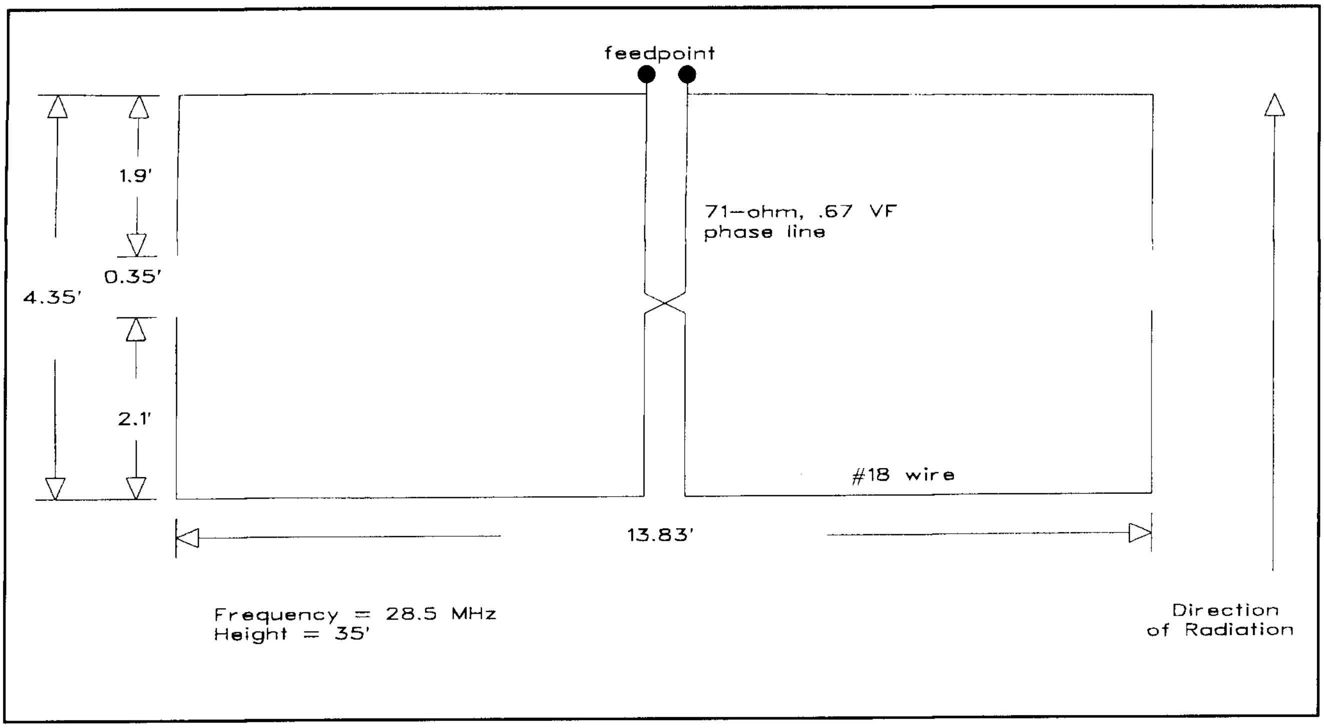

Figure 12. General configuration of the 'BRD Zapper ZL Special.

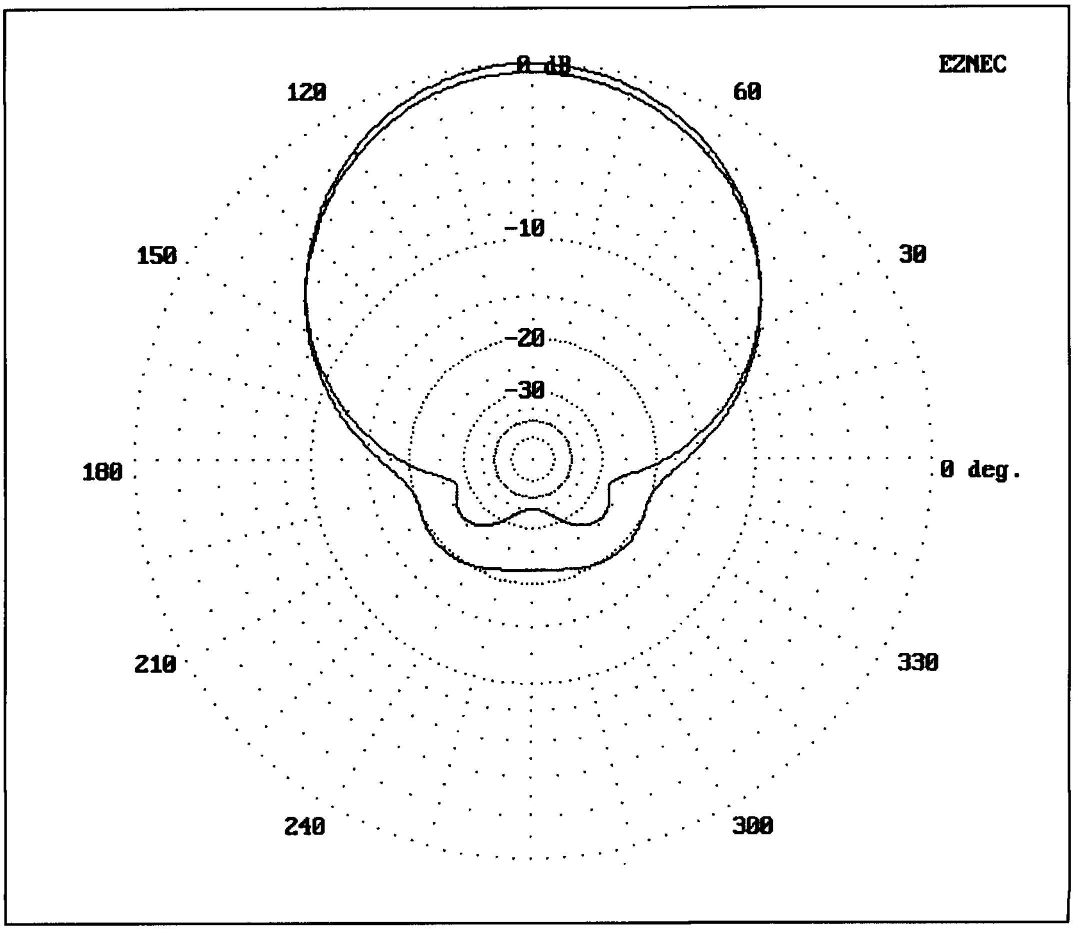

Figure 13. Azimuth patterns of the 'BRD Zapper at 28.5 MHz, 20 and 35 feet over real medium earth.

Wireless, for her kindness in supplying me with copies of articles on the ZL Special appearing in those journals. My thanks also go to Brian Egan, ZL1LE, for providing copies of ZL Special articles appearing in *Break-In*, and to Bridget DiCosimo of the ARRL for finding similar materials that have appeared in *QST*.

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1. Prichard, "A New Driven Array," *Break-In*, May 1949, pages 13–14; "Two Beams for the Price of One," *Break-In*, July 1949, pages 15–17; "Some Notes on the Driven Arrays," *Break-In*, September 1949, pages 5–7; and "Further Experimentation with the '3MH' Beam," *Break-In*, December 1949, page 13. ZL3MH credits two U.S. hams, W5LHI and WØGZR, for supplying him with the basic idea for the array, which was apparently developed commercially just prior to World War II. I have been unable to uncover the identities of the two hams who inspired Prichard. However, see the appended bibliography for some fascinating reading on the history of the ZL Special and its workings.
2. Judd, "The ZL Special," *Shortwave Magazine*, July 1950, pages 337–339.
3. Moxon, *HF Antennas for All Locations*, RSGB, 1982, pages 77, 222; and Lewallen, "Try the 'FD Special' Antenna," *QST*, June 1984, pages 21–24.
4. Similar results might be obtained by using any two of the three value sets, as E, I, and Z are interrelated. However, the use of E and I provides a very straightforward set of calculations. Also, concern for graphical outputs from NEC and MININEC often obscures the fact that these programs are precise calculational programs. The limits on the accuracy of the models produced relative to "real" antennas is a separate issue (or set of issues).
5. Supplementary equations for calculating line lengths, along with expansions of the equations in the text for use with complex E and I values are given in Appendix 1.
6. The modeling programs used for this analysis were ELNEC 3 and EZNEC 1.
7. I owe this idea to Roy Lewallen, W7EL, who has implemented it with success. See Lewallen, "Try the 'FD Special' Antenna," *QST*, June 1984, pages 21–24.
8. Newkirk, "The 'BRD Zapper: A Quick, Cheap, and Easy 'ZL Special' Antenna," *QST*, June 1990, 28–29.

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12. Newkirk, "The 'BRD Zapper: A Quick, Cheap, and Easy 'ZL Special' Antenna," *QST*, June 1990, pages 28–29.
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18. Prichard, "The 'ZL Special' Beams, *Break-In*, May 1961, pages 129–130.
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Appendix: Using the ZL Special Equations

Using the equations given in the main text for the ZL Special requires that we expand them to account for the fact that each voltage, current, and impedance may be a complex number—that is, a magnitude with a phase angle. As a convenience to anyone who might wish to put these calculations into a utility computer program, the following expansions are provided, along with some additional calculations of casual interest in the analysis of horizontal two-element phased arrays.

First, the rear element values of E_{rr} and I_{rr}, along with their associated phase angles, yield the impedance at the rear element, Z_{rr}:

$$Z_{rr} = \frac{E_{rr}}{I_{rr}} \qquad \theta_{Zrr} = \theta_{Err} - \theta_{Irr}$$

where Z_{rr} is the rear element feedpoint impedance and θ_{Zrr} is its associated phase angle. Obtaining this figure allows one to determine the impedance phase change along the phaseline as a matter of interest.

The use of **Equation 2** in the text requires that we first convert the physical length of the phaseline, initially identical to the spacing between elements, into radians. This is a standard two-step process that begins with the conversion of the physical length into an electrical length in degrees:

$$\ell_d = \frac{1.2f\ell_m}{VF} \quad or \quad \ell_d = \frac{.366f\ell_f}{VF}$$

where ℓ_d is the length of the line in degrees, f is the frequency in MHz, VF is the velocity factor of the line, and ℓ_m and ℓ_f are the initial lengths in meters and feet, respectively.

Converting degrees into and out of radians requires the familiar equations,

$$r = \frac{\pi\ell_d}{180} \quad and \quad \ell_d = \frac{180\ell_r}{\pi}$$

where ℓ_r is the electrical length in radians.

Equation 2 in the text yields a value of Z_O that produces the desired change of current phase with an incidental change of magnitude:

$$Z_o = \frac{E_{fr} - E_{rr}\cos\ell_r}{jI_{rr}\sin\ell_r}$$

Expanded to account for the complex numbers involved, it becomes:

$$Z_o = \frac{E_{fr}\cos\theta_{Efr} + jE_{fr}\sin\theta_{Efr} - E_{rr}\cos\theta_{rr}\cos\ell_r - jE_{rr}\sin\theta_{rr}\cos\ell_r}{jI_{rr}\cos\theta_{rr}\sin\ell_r - I_{rr}\sin\theta_{rr}\sin\ell_r}$$

Gathering real and imaginary terms in the numerator allows one to split the equation into its parts. However, because the denominator is also complex, inverting the parts allows further subdivision. Each real and imaginary subdivision pair may be recombined by vector addition. Reinverting and using vector addition once more produces the final result, the Z_O of the phaseline.

Calculating the current at the input end of the phaseline, given the phaseline Z_O, is straightforward:

$$I_{in} = I_{rr}\cos\ell_r + j\frac{E_{rr}}{Z_o}\sin\ell_r$$

This equation expands into the following form:

$$I_{in} = I_{rr}\cos\theta_{Irr}\cos\ell_r - \frac{E_{rr}}{Z_o}\sin\theta_{Err}\sin\ell_r + j\,(I_{rr}\sin\theta_{Irr}\cos\ell_r + \frac{E_{rr}}{Z_o}\cos\theta_{Err}\sin\ell_r)$$

where the real and imaginary parts of the equation are recombined by vector addition.

Z_{in}, the impedance at the input end of the phaseline, may be obtained from E_{fr} and I_{in} by the same calculation method used to find Z_{rr}. The difference in the phase angle for the two impedances is the total impedance phase angle change for the phaseline.

Because the total feedpoint current is a vector sum; that is,

$$I_{fp} = I_{fr} + I_{in}$$

the magnitude and phase angle of I_{fp} are determined from:

$$I_{fp} = \sqrt{(I_{fr}\cos\theta_{Ifr} + I_{in}\cos\theta_{Iin})^2 + (I_{fr}\sin\theta_{Ifr} + I_{in}\sin\theta_{Iin})^2} \qquad \theta_{Ifp} = \arctan\frac{I_{fr}\sin\theta_{Ifr} + I_{in}\sin\theta_{Iin}}{I_{fr}\cos\theta_{Ifr} + I_{in}\cos\theta_{Iin}}$$

Precalculation of various recurrent terms can simplify programming of such equations.

Determination of the feedpoint impedance, resistance, and reactance are self-explanatory from the equations in the main text, with the addition of one item:

$$Z_{fp} = \frac{E_{fr}}{I_{fp}} \qquad \theta_{Zfp} = \theta_{Efr} - \theta_{Ifp} \qquad R_{fp} = Z_{fp}\cos\theta_{Zfp} \qquad X_{fp} = Z_{fp}\sin\theta_{Zfp}$$

The recalculation of I_{r2}, the rear element current magnitude and phase angle, via the standard formula,

$$I_{r2} = I_{in}\cos\ell_r - j\frac{E_{fr}}{Z_o}\sin\ell_r$$

requires an expansion similar to that for calculating input current from load current, with some appropriate sign changes along the way. Expanded, the equation is:

$$I_{r2} = I_{in}\cos\theta_{Iin}\cos\ell_r + \frac{E_{fr}}{Z_o}\sin\theta_{Efr}\sin\ell_r + j\,(I_{in}\sin\theta_{Iin}\cos\ell_r - \frac{E_{fr}}{Z_o}\cos\theta_{Efr}\sin\ell_r)$$

The equation requires completion in the same manner as the calculation of I_{in}.

I hope this appendix will assist a few readers. Those who wish precision beyond the capabilities of average home construction may replace the lossless transmission line formulas with those for lossy lines. Terman's *Radio Engineer's Handbook* and Johnson's *Antenna Engineering Handbook* provide ready references.

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BUILD A 5- TO 850-MHz SPECTRUM ANALYZER

Low-cost TV tuners make this project a snap!

A spectrum analyzer can be a useful and helpful tool. It lets you look at any part of the RF spectrum and see at a glance just what signals are there. Normally, a good used or new spectrum analyzer would run over a thousand dollars—placing it out of the reach of most pocketbooks. But, by using commonly available varactor-tuned TV tuners, you can put one together with ease!

A major cost component is represented by the CRT display section. If you already have a good shop scope with DC coupling and XY inputs, you have half of a spectrum analyzer already in hand. By adding a CATV tuner and a UHF TV tuner, along with some simple support circuitry, you can cover from 5 to 850 MHz in two bands! The block diagram is shown in **Figure 1**. Either tuner can be selected, and its output amplified by the 62-MHz IF strip and detected. The detected signal feeds the vertical (Y) input of the scope. The tuners are swept across their tuning range by a sawtooth waveform generator that's also used to drive the scope horizontal (X axis) input.

More about TV tuners

Photo A shows a typical CATV tuner module. These devices can be found surplus at very low cost. You can also salvage suitable tuners from discarded cable-ready TV sets that have electronic tuning. In **Figure 2**, I show a block diagram depicting what goes on inside one of the CATV tuners. The input signal first passes through a high-pass filter with a cutoff at 40 MHz. A low-pass filter limits signals above

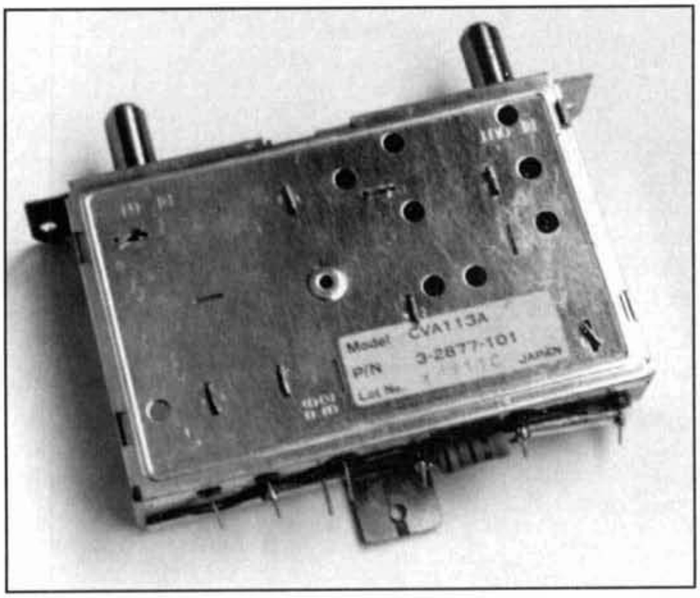

Photo A. A typical CATV tuner has F connectors for RF input and output. Power requirement is +12 volts 75 mA.

500 MHz. The internal VCO is used to up-convert signals in this passband to a fixed first IF at 612 MHz. A second fixed LO down-converts the IF to an output on TV channel 3.

Removal of the input high-pass filter will allow operation down to as low as 5 MHz. Simply take out two small coils and three chip capacitors. A coupling capacitor replaces the high-pass filter section (see **Figure 3**). The VCO that drives the first mixer is varactor tuned by a tuning voltage of from 2 to 20 volts. This was originally tuned by a PLL system, and a divide-by-256 ECL prescaler chip in the mod-

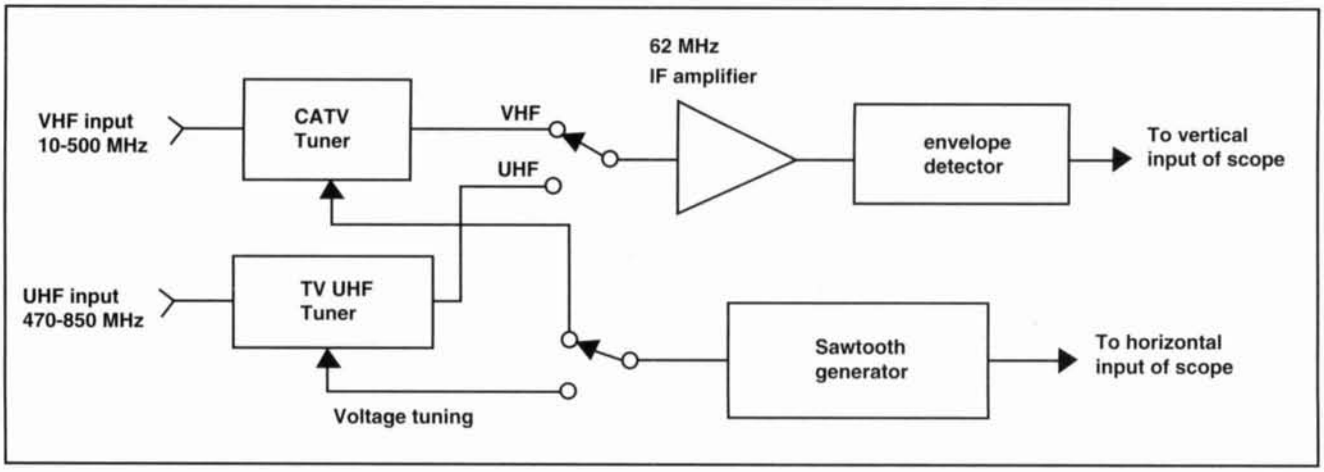

Figure 1. Block diagram of the spectrum analyzer.

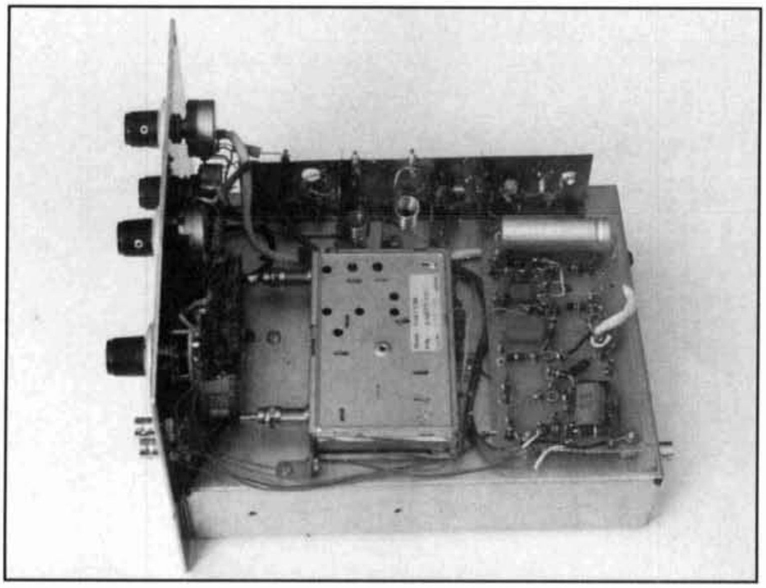

Photo B. The author's spectrum analyzer is built on a 7 x 9 x 2-inch chassis. The power supply is underneath and sweep circuits are on the circuit board at the right. The IF strip runs along the top and the two high-Q air-wound coils, L2 and L3, are clearly visible.

ule was used to drive the divide-by-N portion of the PLL. However, the prescaler isn't used; it's left in the tuner.

Editor's note: CATV tuners used by cable boxes are designed for negative voltage power supplies and also use negative-going tuning voltages—CATV tuners such as the Jerrold 400 or 450 series cannot be used in this analyzer!

My UHF tuner has a bipolar RF stage, mixer, and local oscillator. All three stages are tunable and tracked by varactor diodes. The input coupling loop is for 300-ohm line. By reducing this to one turn, a better match is had for 50-ohm lines. Enough turns were removed from the mixer output coil to raise its frequency from the normal TV IF of 43 to 62 MHz, or channel 3. Other than a minor alignment touchup, these are the only modifications needed for the UHF tuner.

To keep things simple, no further frequency conversion stages are used after the tuners; that is, the IF runs straight through at 62 MHz. I felt this reduced the likelihood of generating spurious signals in the analyzer. As it is, there are no

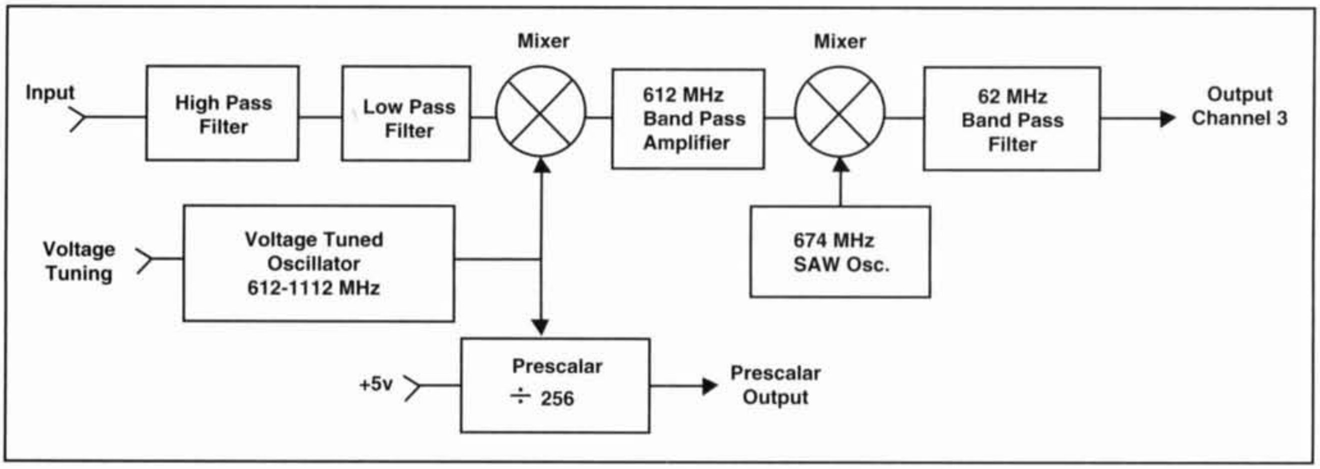

Figure 2. Block diagram of a CATV tuner.

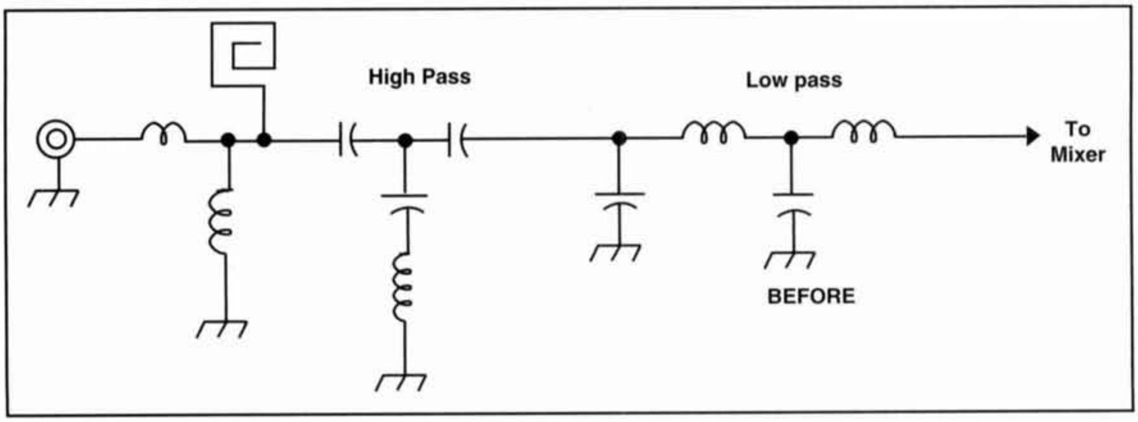

Figure 3. Before and after configuration of the CATV converter front end. The high-pass 40-MHz filter components are removed and replaced with a 1 nF capacitor to extend the frequency response down through HF.

spurious blips anywhere within the analyzer range. Using Hi-Q coils, with light loading, in the IF stages yielded a passband with a 3-dB bandwidth of 180 kHz. This may seem overly broad, but for most ham applications it's entirely satisfactory. You might be able to improve the resolution using crystal or SAW filters, but this would increase the complexity and cost of this project. The lack of an RF stage in the CATV module, and the broad IF bandwidth, limits the sensitivity of the analyzer to about 3 µV—signals weaker than this are lost in the "grass" (noise above the analyzer display baseline).

Figure 4 shows the complete analyzer circuit diagram. **Photos B** and **C** show the exterior and interior views of my completed analyzer. The sawtooth waveform generator has an 80 Hz repetition rate. Transistors Q1 and Q2 perform this function. This scan rate is high enough to avoid flicker but low enough that rise time isn't a problem. The sawtooth waveform is amplified by the op amp, U1. It was nesessary to use an FET-input op amp because of the high impedance level of the sawtooth oscillator circuit. The output of U1 provides a voltage swing of +2 to +20 volts when scan width control, R1, is set for maximum sweep. This sawtooth is then combined with a variable DC voltage, from the center frequency control, R2, so any part of the RF spectrum can be examined in detail. The TV tuner modules have a fairly linear tuning voltage-to-frequency curve. **Photo D** illustrates linear tracking up to approximately 400 MHz. The discrepancies above 400 to 500 MHz could have been compensated for by using op-amp drivers with nonlinear diode feedback schemes. But, again, the results are livable for my applications.

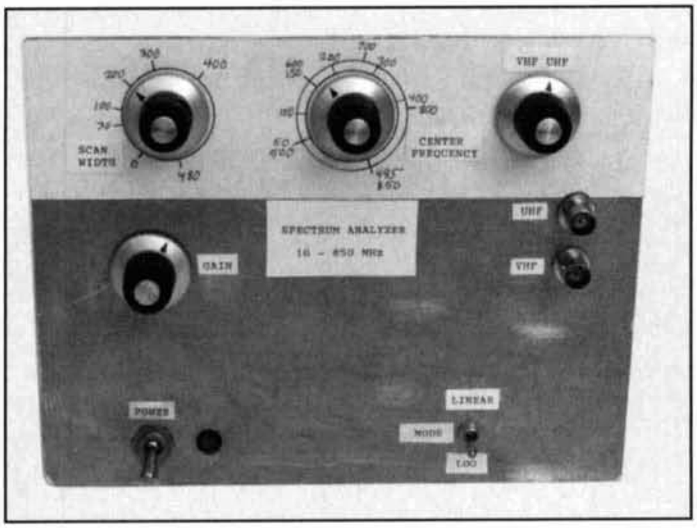

Photo C. The front panel measures 8-1/4 x 6-1/2 inches. The center frequency control has two scales—one calibrated for VHF and one for UHF.

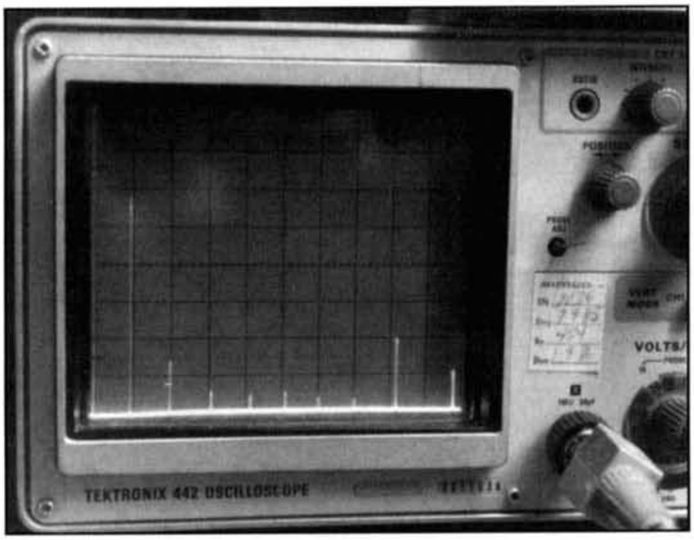

Photo D. This shows the harmonic structure of a 50-MHz crystal-controlled oscillator coupled to a step-recovery diode harmonic generator. Note that the spacing of the harmonics is quite uniform from zero up to almost 400 MHz, but the sweep rate falls off at higher frequencies as evidenced by wider spacing between harmonics.

IF strip

The IF strip uses three dual-gate MOSFETS, Q5, Q6, and Q7. Total gain from IF input to

Coil data.
L1: 7 turns no. 24 enamel wire, close wound on 1/4-inch OD slug-tuned coil form.
L2: 6 turns no. 14 wire, 0.4-inch ID, 1/2-inch long, air wound.
L3: Toroid core, wound for 0.32 μH inductance.

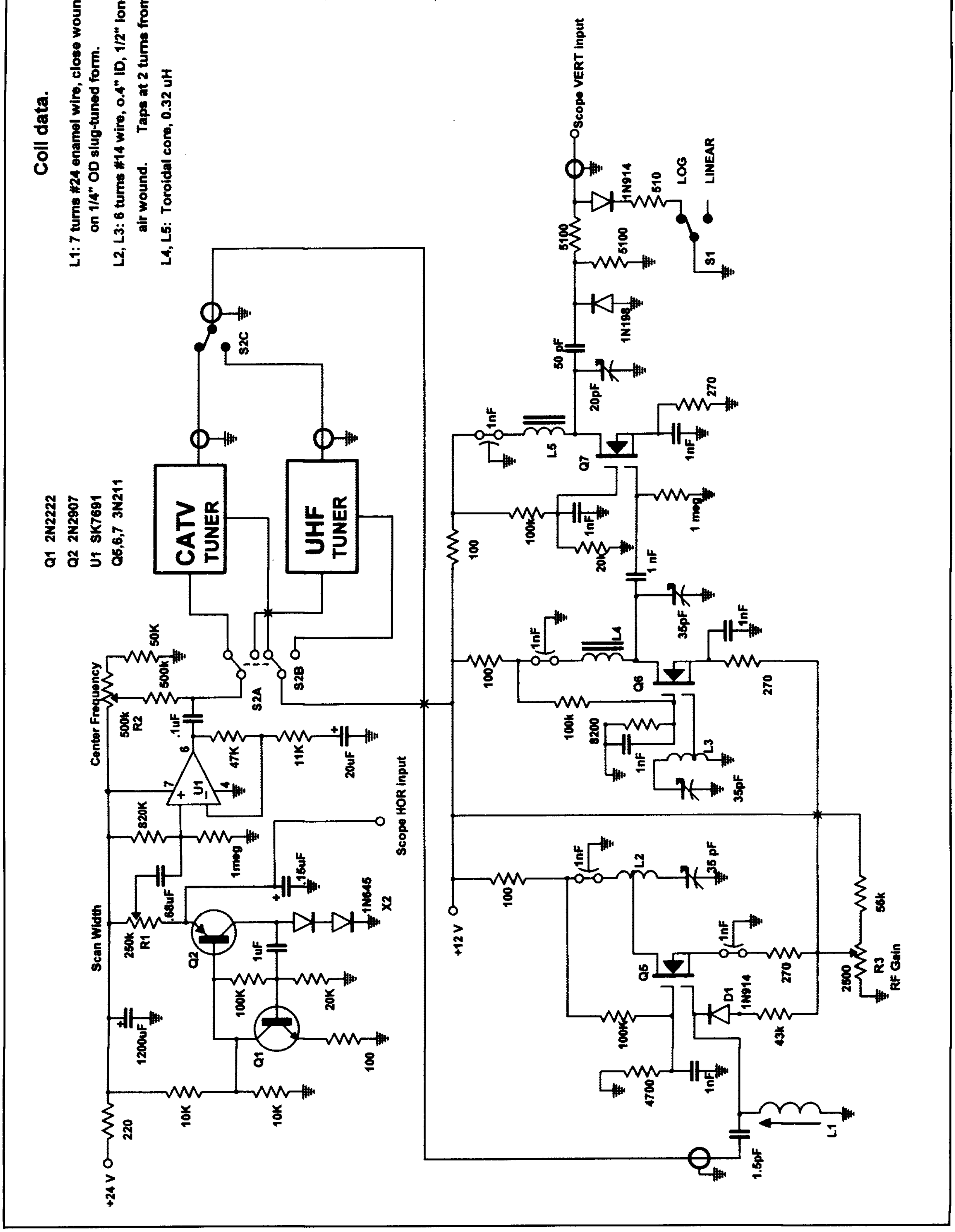

Figure 4. Complete circuit and part values for the spectrum analyzer.

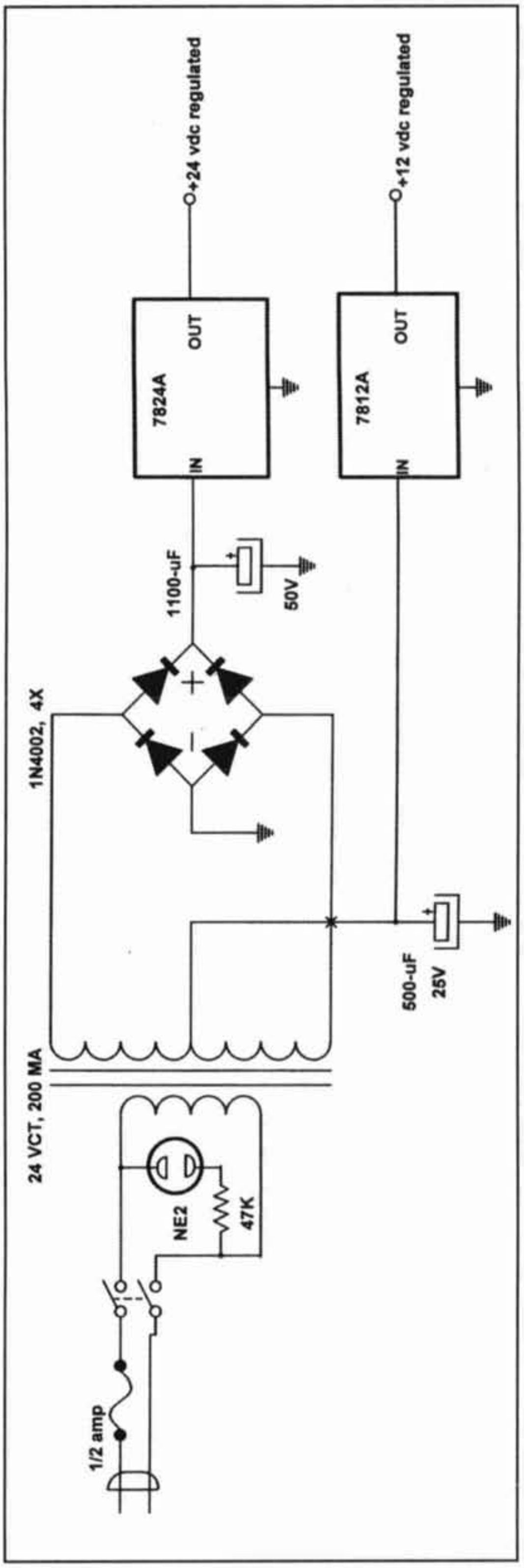

Figure 5. The power supply provides both 12 and 24 volts regulated from one small transformer.

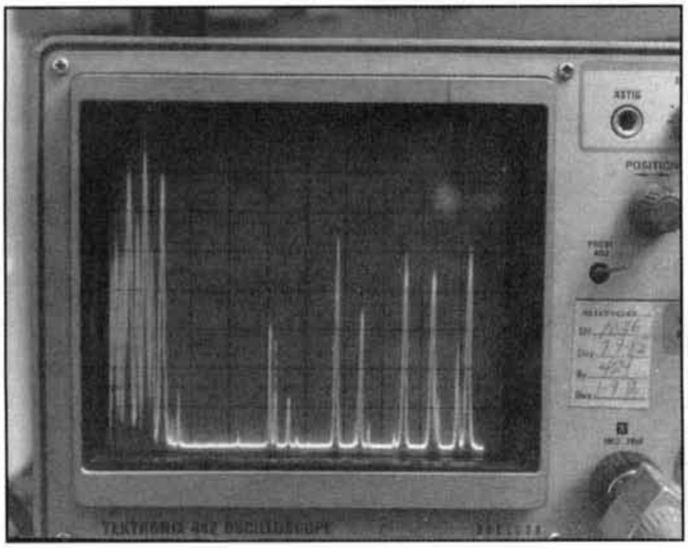

Photo E. This shot of the RF spectrum at the author's QTH was obtained by connecting the VHF input of the spectrum analyzer to a broadband antenna. The sweep is approximately zero to 80 MHz with 50 MHz at the center of the screen. The signals on the left are HF skywave signals. Note that the MUF cuts off at about 18 MHz. The strong signal just to the right of center is the video carrier of channel 2. Next is the sound carrier of channel 2, and the subsequent strong signal is the video barrier of channel 4. This is followed by a couple of communications signals in the 72 to 76-MHz band, which are followed by the video carrier of channel 5.

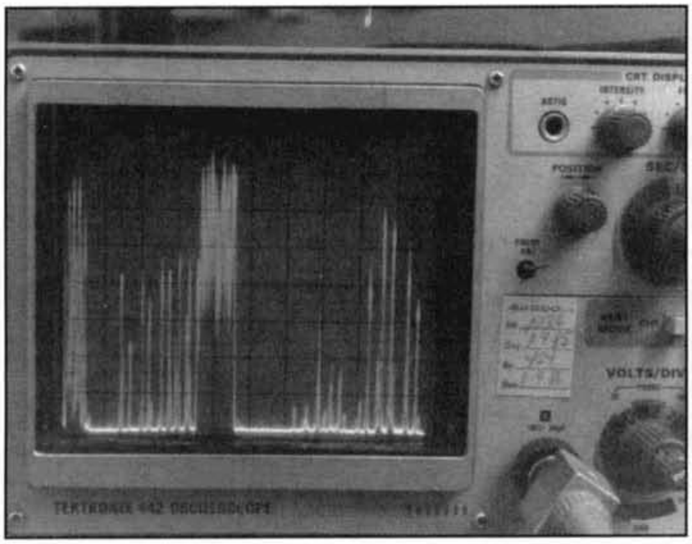

Photo F. This scan is from zero to 230 MHz and shows all the VHF TV channels plus many communications signals. The part that's saturated with signals, just to the left of center, is the FM broadcast band.

DC output is about 75 dB. The two high-Q coils, L2 and L3, form a two-pole filter and provide most of the selectivity. It was necessary to tap Q5 and Q6 down on these coils to maintain a high Q. It was also necessary to place a shield between the two coils to reduce the coupling. If there's too much coupling, you end up with a double-hump response curve. Because of the high Qs of L2 and L3 (about 250), optimum coefficient of coupling is very small. RF toroids were used for L4 and L5; this avoids stray magnetic fields, but solenoidal coils could also be used if shielding is adequate.

The IF assembly is built on a 1-1/2 by 7-inch section of pc board. Each amplifier is individually shielded. The liberal use of feedthrough capacitors helps to maintain the needed isolation. With 75 dB of in-line gain, you need at least 7 dB of isolation between the input and output. Isolation also affects the skirt selectivity! Any spectrum analyzer will have a large blip at a zero frequency. At this point, the LO reaches the first IF frequency and saturates the analyzer. The skirt bandwidth of this "blip" determines the lowest observable signal. (Editor's note: The baluns used in the construction of the diode mixers may also play a role here.)

RF gain control R3 provides a control range of more than 70 dB, while maintaining good linearity in the IF stages. As the arm of R3 nears the 56-k resistor, the DC source voltage of Q5 and Q6 increases—reducing the gain of those stages. Additionally, as the voltage on the arm of R3 nears 1/2 volt, diode D1 begins to conduct, shunting the input signal to prevent overloading of the Q5 IF stage.

The detector is a simple germanium diode! Techies may use a Schottky device here, but the results will remain the same. Capacitor C1 and resistor R4 determine the detector time constant—about 1/4 µsec for the values shown.

A reasonably logarithmic response results from switching in diode D2, providing a log response over a 40-dB range. There are better methods, but this offers simplicity and is adequate for my needs. **Photos E** and **F** show off-air signals received on two different scan ranges.

The analyzer power supply is shown in **Figure 5**. A center-tapped 24-volts AC transformer provides the needed 24 volts DC and 12 volts DC regulated outputs. The 24-volt supply filtering is especially critical, because it's used for developing the tuner varicap tuning voltages.

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Edited by Peter Bertini, K1ZJH
Senior Technical Editor

In this issue of "Tech Notes," we feature just one article on the attenuators by Chris Fagas, WB2VVV. These nifty little gadgets have many applications in RF, HF, VHF, and UHF projects. Mounted in small boxes, they'll even serve as inexpensive VHF "Fox Hunting" adjustable attenuators. I'm sure you'll find many additional uses for these handy devices!
—Pete, K1ZJH

Adjustable 50-ohm Attenuators Make Level Matching Easy Between RF Stages

These nifty little attenuators have many applications.

Chris Fagas, WB2VVV

This approach to 50-ohm attenuators is usable almost anytime such a device, which can be tweaked to its final attenuation value in the operating circuit, is needed between stages.

Although this little-known technique has been used by many in the past, very little time and effort has been spent to date in understanding the performance characteristics that can be attained through it.

By carefully choosing component values, the response of this simple pi-network resistive attenuator (**Figure 1**) can be optimized to provide:

1. An appropriate range of attenuation;
2. A smooth response over the desired range.

Measurements

All of the examples discussed here will yield input and output VSWR with respect to 50 ohms of under 2:1 (return loss over 9.5 dB), even over their maximum adjustment range.

This low theoretical input/output VSWR has been calculated in the following tables and graphs (**Figures 2** through **4**) without taking component inductive/capacitive reactance into account. This is simply a matter of individual circuit execution, with an understanding that these reactances will become more bothersome at higher frequencies. In my experiences under 30 MHz, little regard for neat execution is necessary to achieve excellent performance. However, at higher frequencies more careful attention should be directed towards component choices and cleaner execution.

I used the Wiltron S331 Vector Network Analyzer to create the circuit plots from 25 to 330 MHz in the minimum, median, and maximum attenuation settings. These show the VSWR and Smith Chart of these settings over this frequency range. The Scalar Network Analyzer plots of the circuit from 300 kHz to 1300 MHz in the minimum, median, and maximum attenuation settings were created using the Hewlett Packard HP8711B. These plots show two channels for these settings over this frequency range. Channel number 1 is transmission loss, or loss through the circuit. Channel number 2 is return loss, or the delta between energy put into the circuit and energy

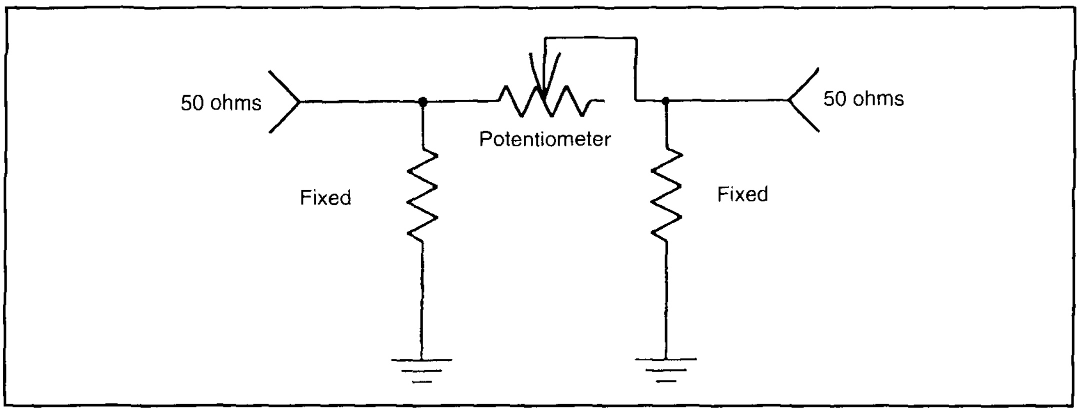

Figure 1. Pi-network resistive attenuator.

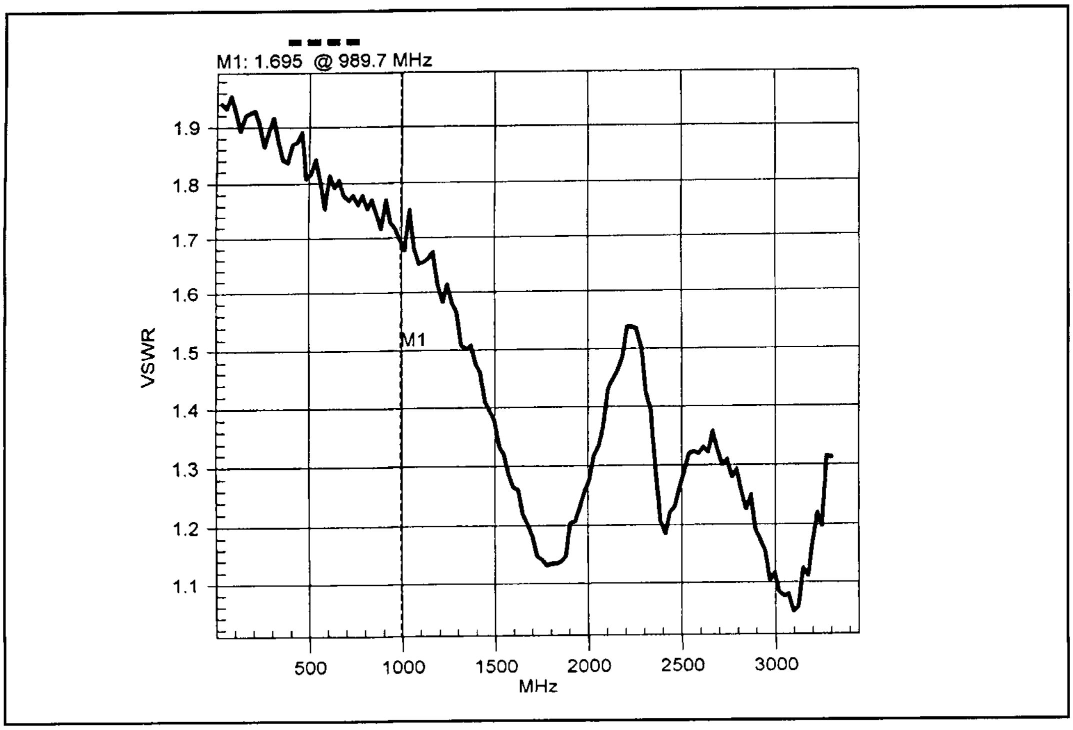

Figure 2. (A) VSWR (Reflection) of minimum attenuator setting (approximately -3 dB).

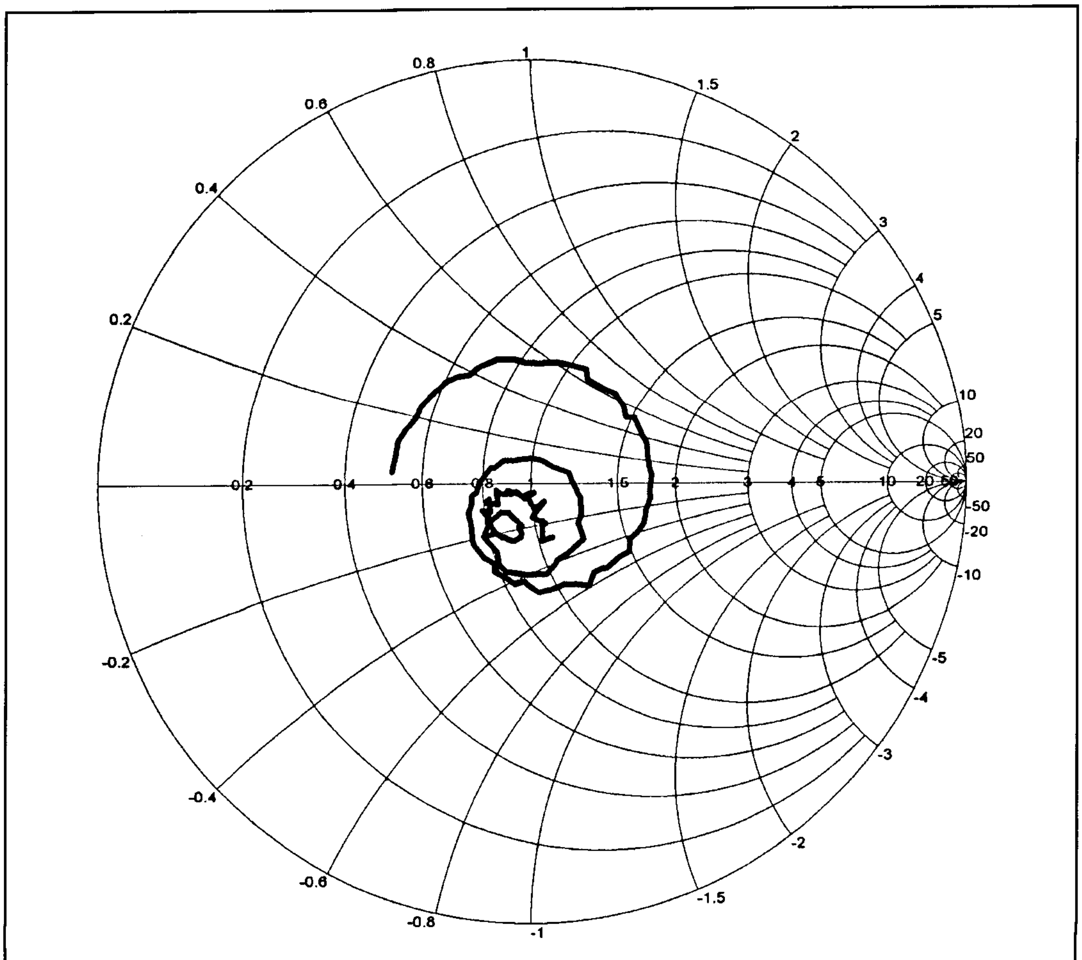

Figure 2. (B) Smith Chart plot.

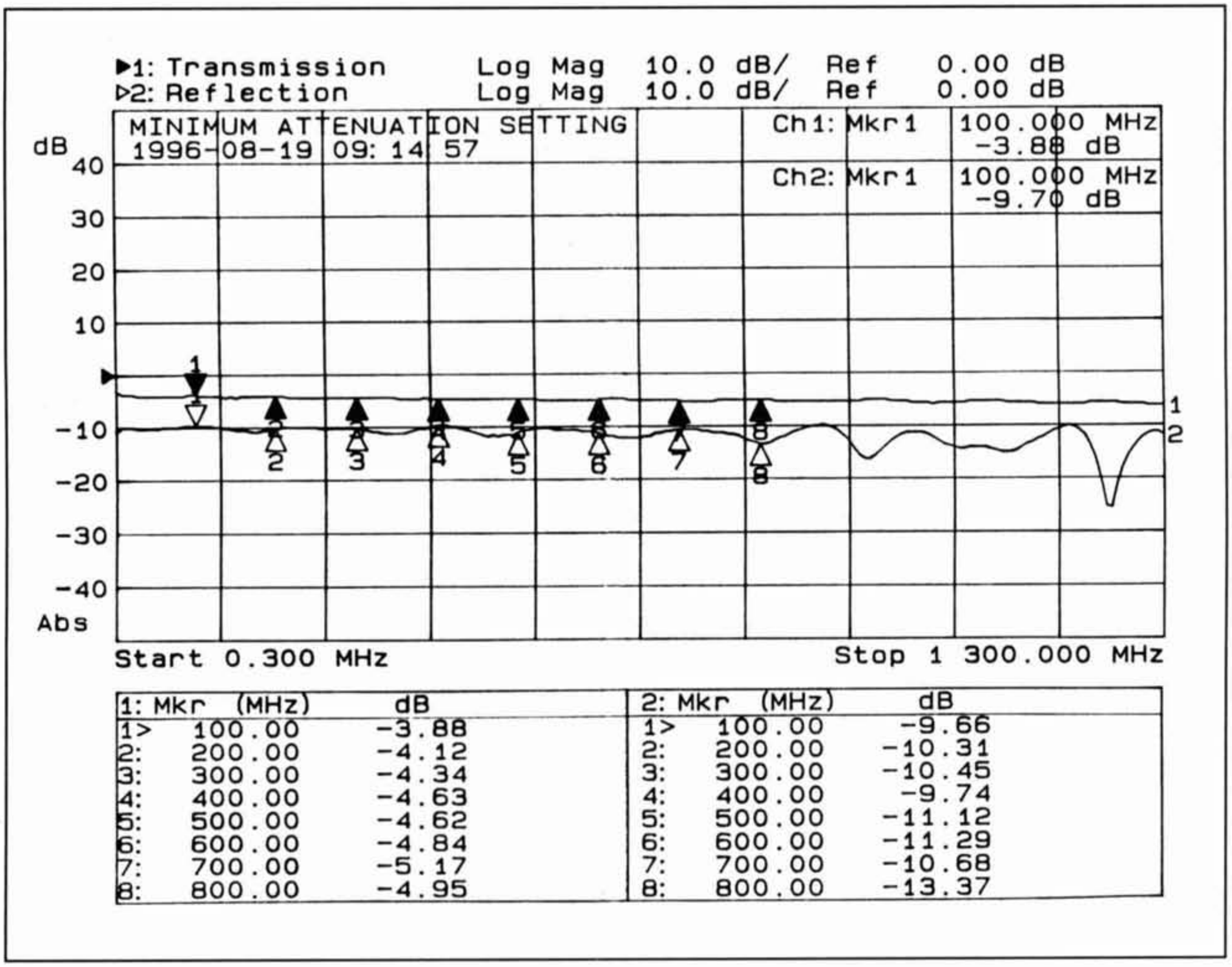

Figure 2. (C) Network analyzer plot of the circuit.

reflected by the circuit (for reference, 6 dB of return loss equals a VSWR of 3:1, 9.6 dB of return loss equals a VSWR of 2:1, and 14 dB of return loss equals a VSWR of 1.5:1).

Figures 5 through **8** show that 100-ohm fixed resistors yield the greatest adjustment range in this circuit. Standard carbon composition or metal-oxide fixed resistor legs to ground will generally yield excellent results. At higher frequencies, you'll need to keep all leads very short and neat for acceptable performance. At even higher frequencies, surface-mount chip resistors might be necessary to attain acceptable performance. Wirewound resistors must be avoided because of excessive inductance.

The choice of potentiometer is quite similar; again, wirewound varieties must be avoided. Unfortunately, this means that most of the high-quality, panel-mount, multi-turn potentiometers aren't usable because they're of the wirewound variety. However, many composition potentiometers are available in both the panel-mounted and on-the-board "trimmer"

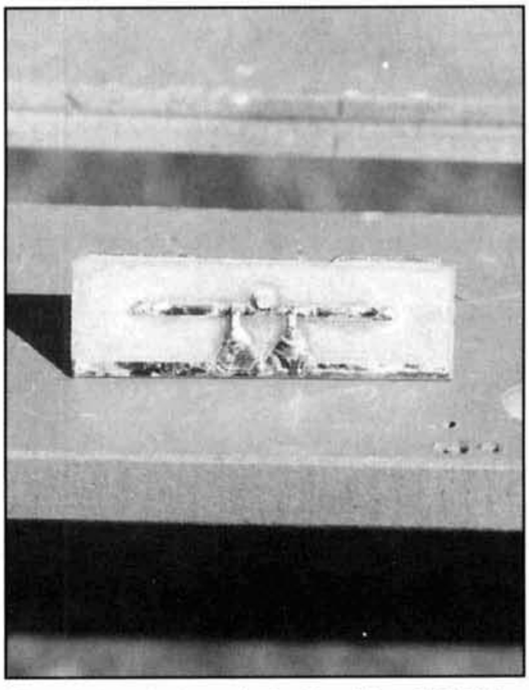

Photo A. Actual microstrip circuit usable to 1000 MHz.

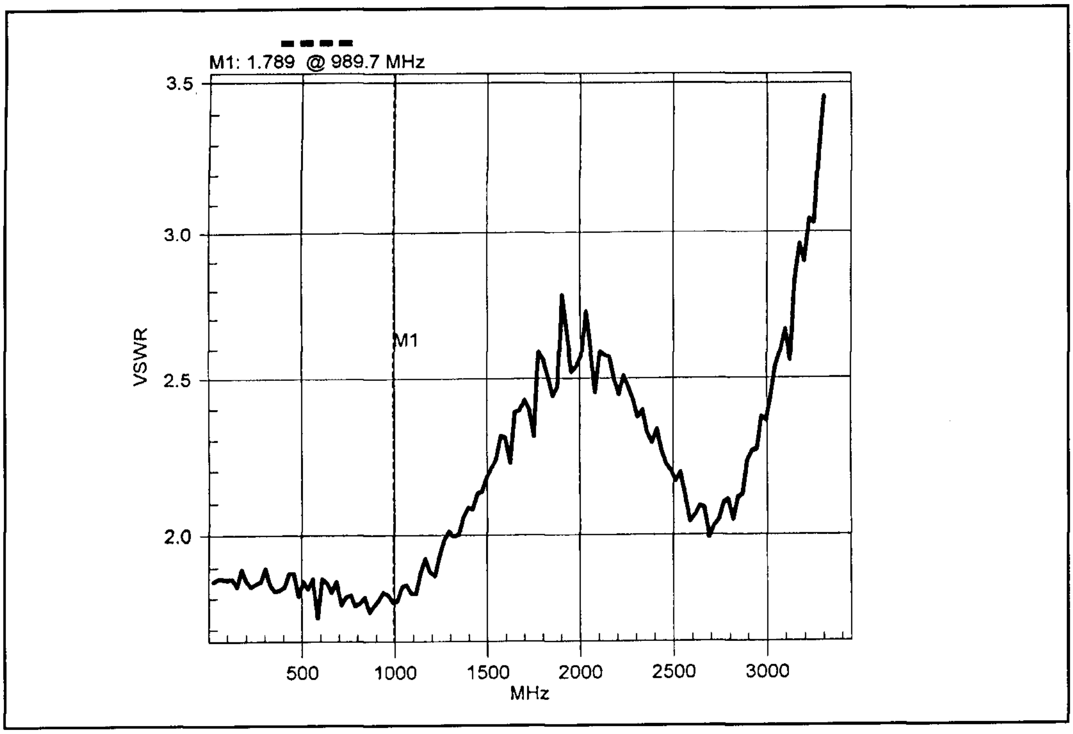

Figure 3. (A) VSWR (Reflection) of median attenuator setting (approximately -30 dB).

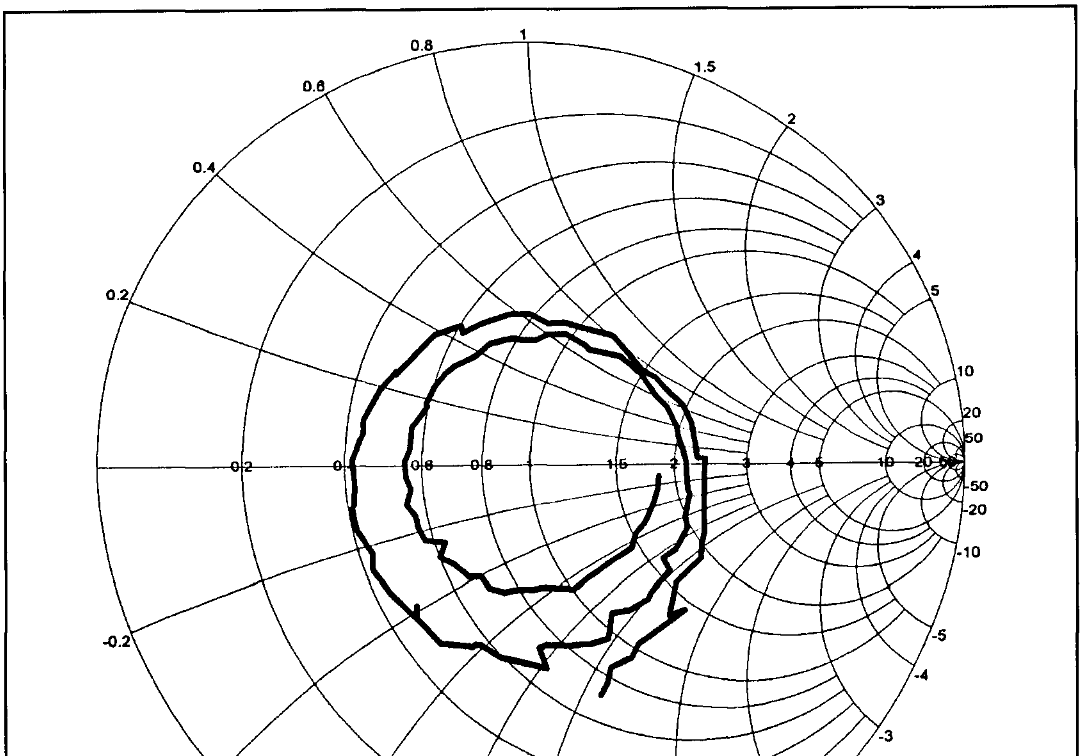

Figure 3. (B) Smith Chart plot.

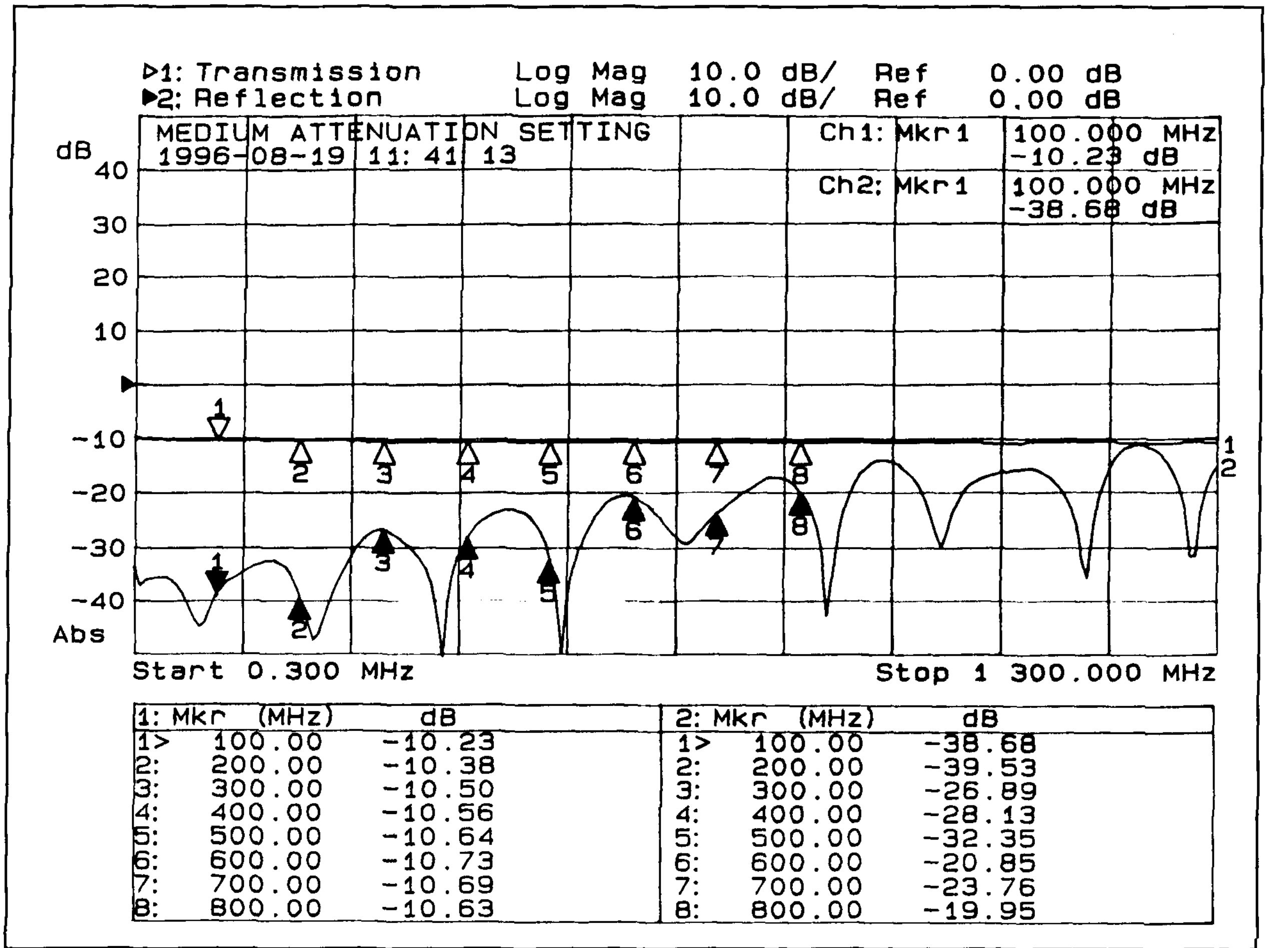

Figure 3. (C) Network analyzer plot.

style. Also, surface-mount "trimmer" potentiometers will push the upper frequency limit of the circuit even higher.

A Test Fixture

As an example, I made a test fixture with a surface-mount 5-k potentiometer installed on a 50-ohm microstrip, which I cut onto a small piece of glass epoxy FR4 double-sided board stock (**Photo A**). I used fixed value 100-ohm surface-mount chip resistors from the microstrip to a low impedance ground. I then tested this circuit on a network analyzer and was pleased to note excellent performance up to 1000 MHz.

For a lower frequency application at 28 MHz, I used a standard composition 1-k panel-mounted potentiometer on the side of a diecast box, with fixed value 100-ohm composition resistors to a grounding tab on the bottom of the box. The leads of the fixed resistors were left full size. The dressing of the mini-coax leads from the input and output BNC connectors on the opposite side of the box to the potentiometer weren't particularly neat or direct. However, the performance of this circuit was excellent to 100 MHz.

Circuit Applications

Applications in which I have successfully used this circuit, with various styles of execution, are as follows:

A. Panel mounted within a diecast box to allow smooth 28-MHz IF transmitter drive control for a transverter-based UHF system. A high-power amplifier is used with the moonbounce/terrestrial system, and a means of controlling drive is necessary during amplifier tuning. In addition, full transmit power isn't necessary for terrestrial communications, and this circuit allowed the 432-MHz RF output power to be easily adjusted from 10 watts to 1.5 kW (approximately 22 dB).

B. Board mounted and following an 850-MHz low noise amplifier, or LNA (preamplifier), which was to be used ahead of a spectrum analyzer. This allowed an accurate setting of

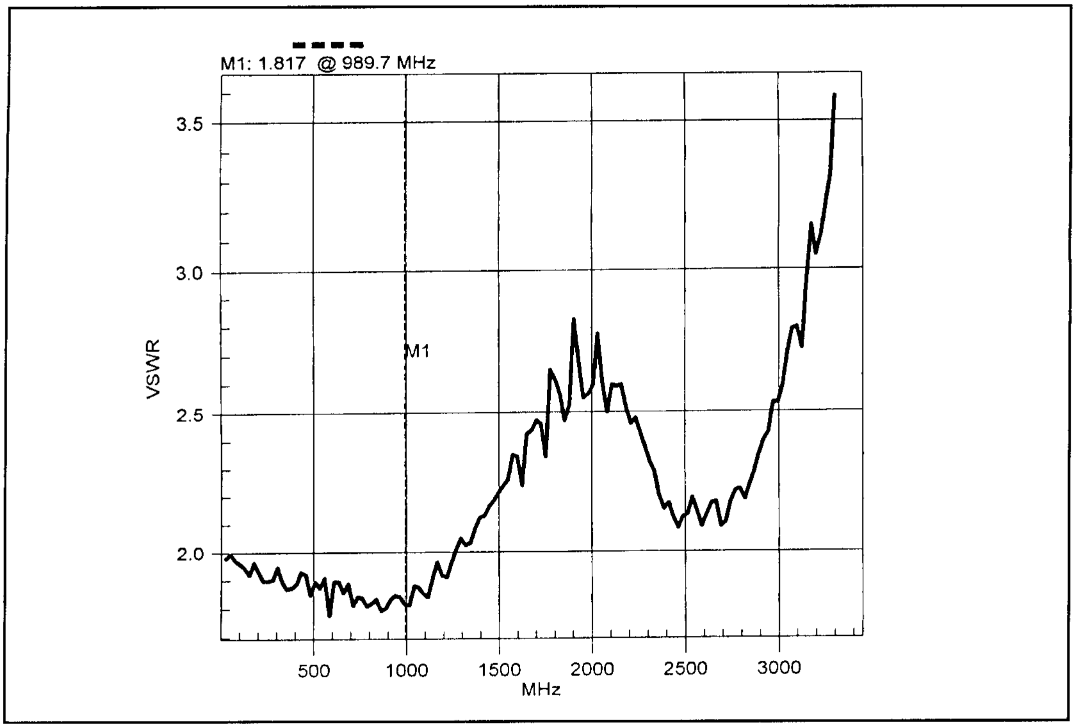

Figure 4. (A) VSWR (Reflection) of maximum attenuator setting (approximately -36 dB)

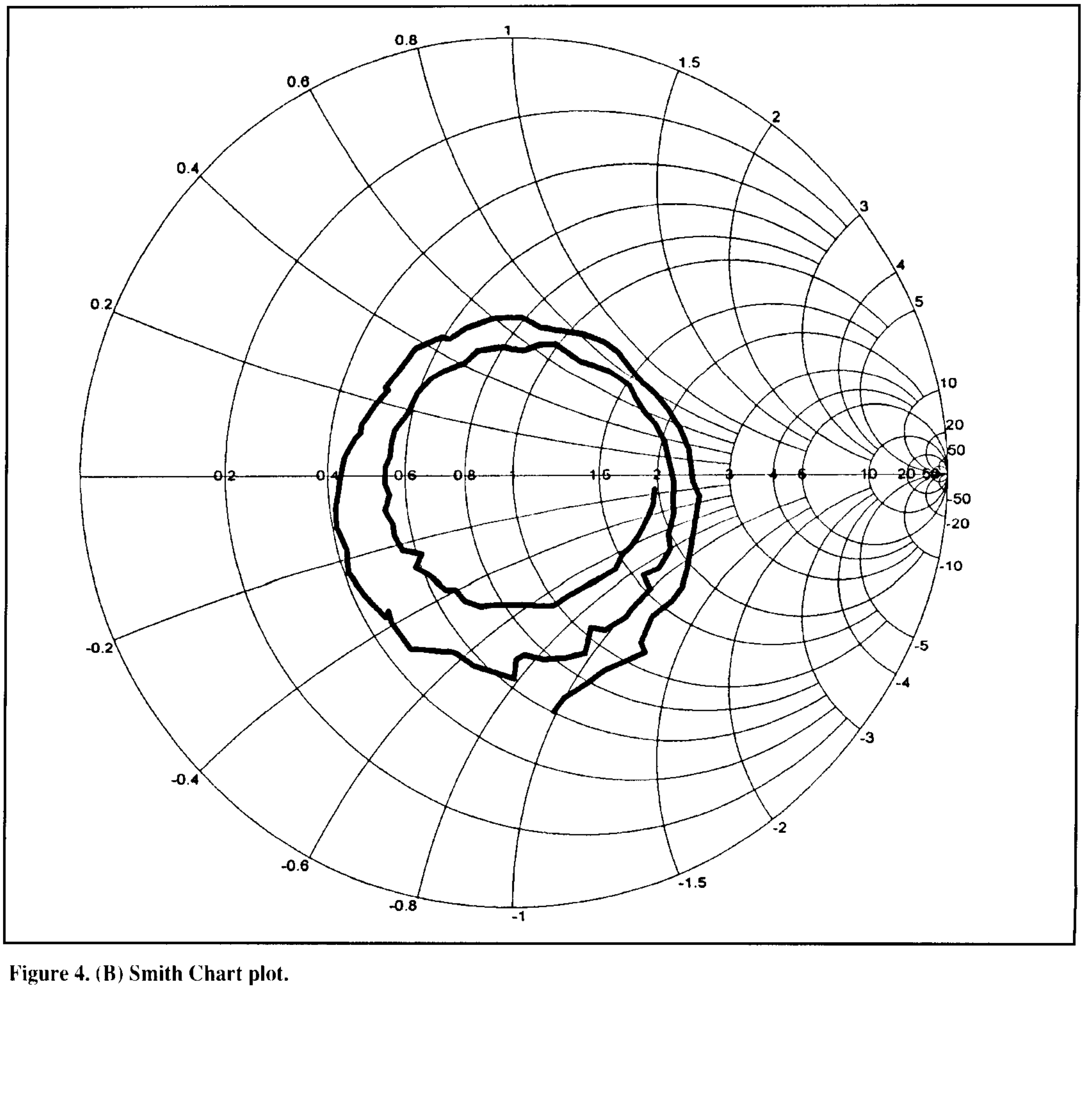

Figure 4. (B) Smith Chart plot.

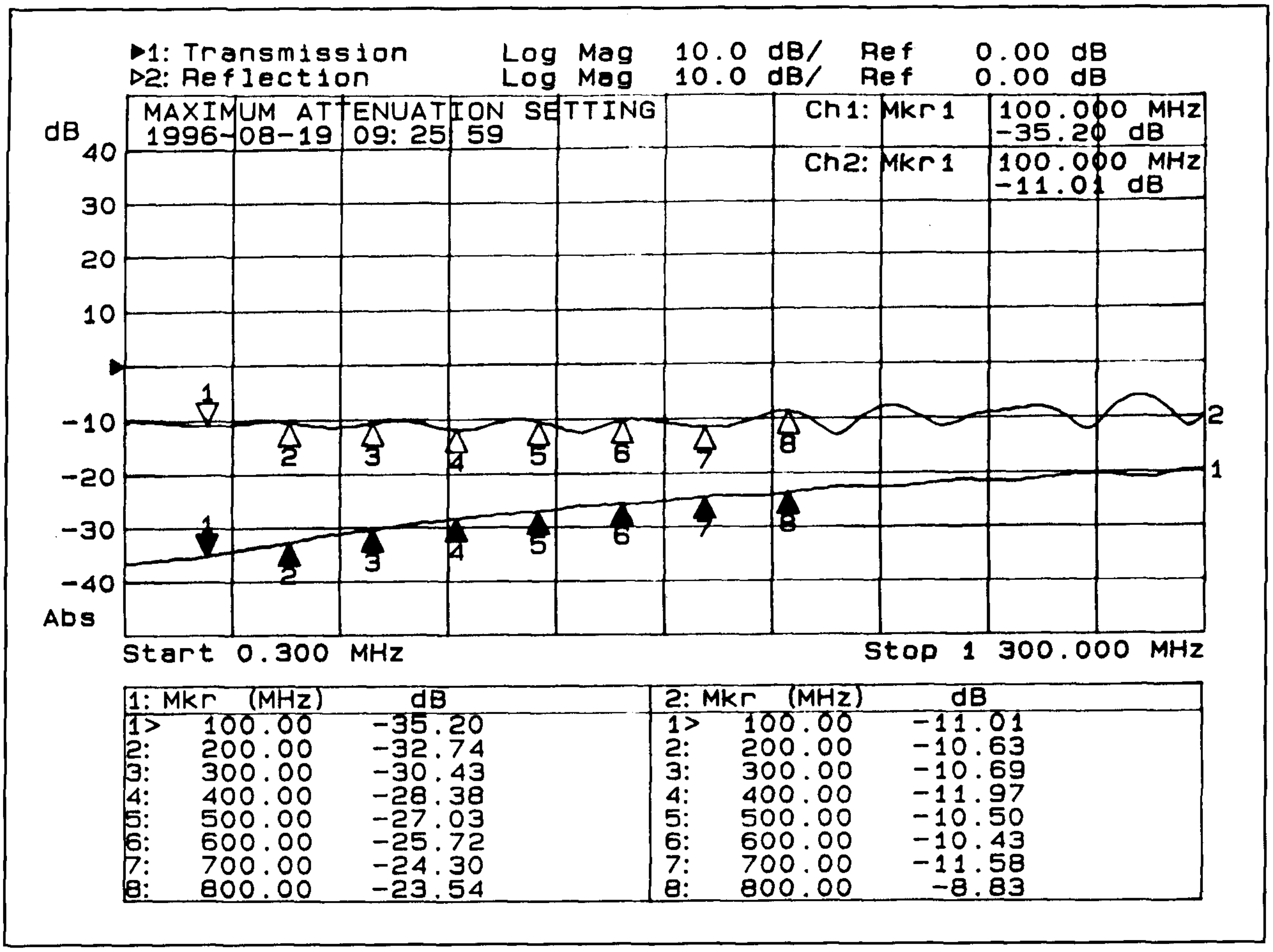

Figure 4. (C) Network analyzer plot.

the system gain for noise floor measurements and calculations.

C. Board mounted between stages in HF, VHF, and UHF receivers to allow redistribution of gain for improvement in strong signal handling capability. This allows for the shifting of gain within the receiver for best strong signal handling while connected to the appropriate test equipment.

D. Board mounted and following a masthead preamplifier in order to avoid overloading a VHF receiver with excessive gain. This allowed the preamplifier's gain to be tweaked on the tower, once it was installed and tested, to take into account the feedline loss of the entire system.

E. Panel mounted and following a second-stage VHF preamplifier to allow adjustment in weak-signal receive system gain, this provided for changing antenna noise temperatures based on antenna position and time of day.

F. Panel mounted in small boxes as inexpensive VHF "Fox Hunting" adjustable attenuators.

Components for a practical attenuator

As a starting point, 100-ohm fixed resistors to ground with a 1, 2, or 5-k potentiometer will yield a very practical adjustable attenuator.

In **Figure 5**, you'll see that extraordinary adjustment range is possible via these potentiometer values. In addition, these potentiometer values tweak quite smoothly over their entire range. Potentiometer values over 5 k adjust extremely quickly and, as a result, are much coarser, albeit they allow for even greater range. This too is illustrated in **Figure 5**. It should be very clear that a tradeoff exists between adjustment range and smoothness. You must decide what it is that you need in your circuit.

When you're selecting potentiometers, you might also have a choice between linear and log varieties. Each has its own advantage based on the tradeoff you make between the adjustment range and the smoothness.

Good luck using these very practical adjustable attenuators. They've served me well!

Pi-Network Resistive Attenuator 100 ohm Fixed Resistors to Ground			
Pot Value ohms	**Attenuation dB**	**VSWR x:1**	**Reflection Coefficient**
0	3.01	2	0.333
5	3.78	1.8	0.287
10	4.46	1.65	0.246
25	6.19	1.36	0.152
50	8.37	1.1	0.048
75	10.07	1.04	0.02
100	11.46	1.14	0.067
150	13.69	1.29	0.128
200	15.44	1.4	0.167
250	16.89	1.48	0.193
350	19.21	1.59	0.227
450	21.03	1.66	0.247
550	22.54	1.71	0.261
650	23.82	1.74	0.271
750	24.93	1.77	0.279
1000	27.22	1.82	0.292
1500	30.52	1.88	0.305
2500	34.77	1.92	0.316
5000	40.65	1.96	0.325
10000	46.61	1.98	0.329
100000	66.54	2	0.333

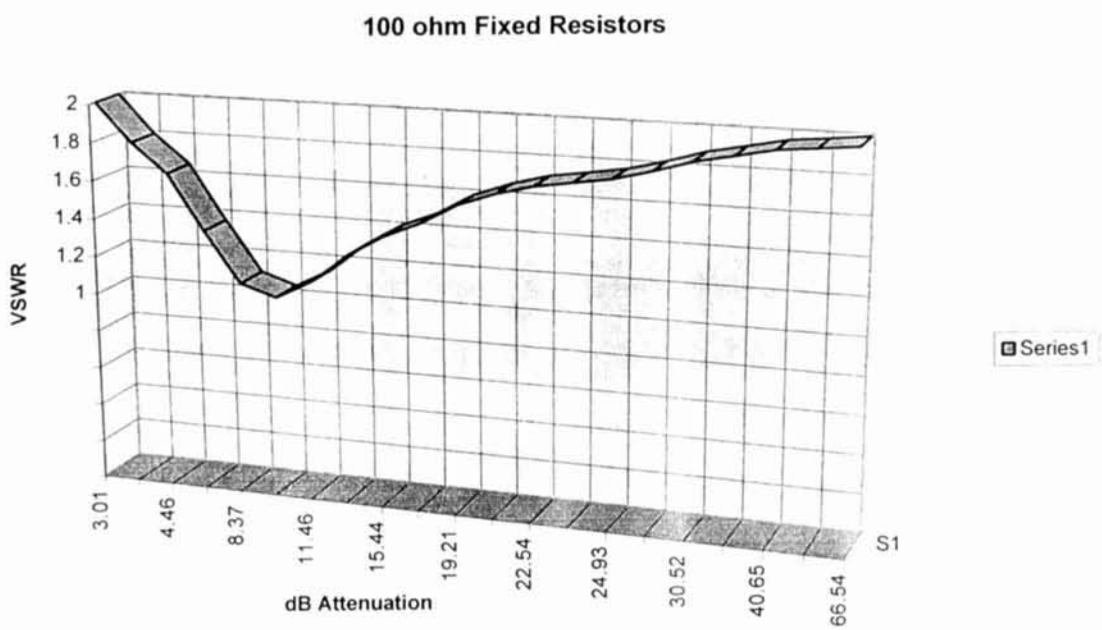

Figure 5. Pi-network resistive attenuator, 100-ohm fixed resistors to ground.

Pi-Network Resistive Attenuator 150 ohm Fixed Resistors to Ground			
Pot Value ohms	**Attenuation dB**	**VSWR x:1**	**Reflection Coefficient**
0	2.22	1.67	0.25
5	2.88	1.51	0.203
10	3.47	1.39	0.162
25	4.98	1.13	0.063
50	6.92	1.11	0.05
75	8.45	1.29	0.125
100	9.72	1.43	0.179
150	11.76	1.67	0.25
200	13.39	1.84	0.295
250	14.74	1.97	0.327

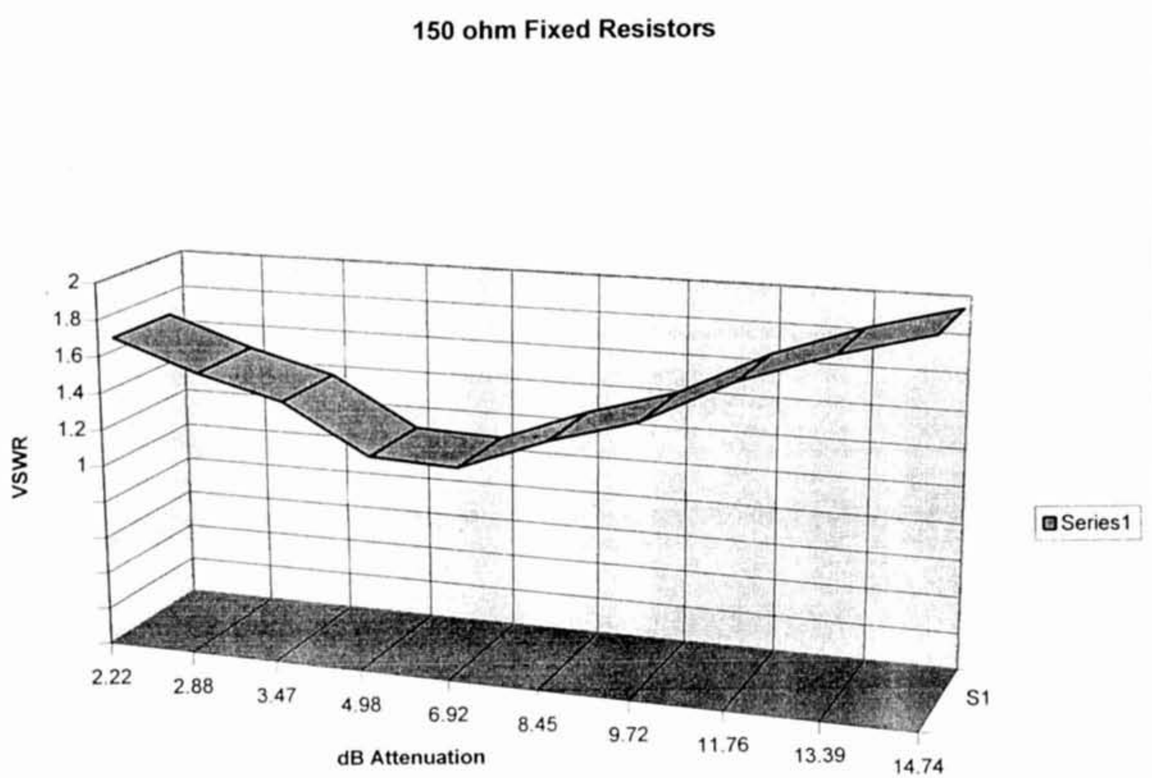

Figure 6. Pi-network resistive attenuator, 150-ohm fixed resistors to ground.

Pi-Network Resistive Attenuator 220 ohm Fixed Resistors to Ground			
Pot Value ohms	**Attenuation dB**	**VSWR x:1**	**Reflection Coefficient**
0	1.63	1.45	0.185
5	2.21	1.32	0.138
10	2.74	1.21	0.096
25	4.1	1.01	0.006
50	5.87	1.28	0.125
75	7.26	1.52	0.205
100	8.42	1.72	0.264

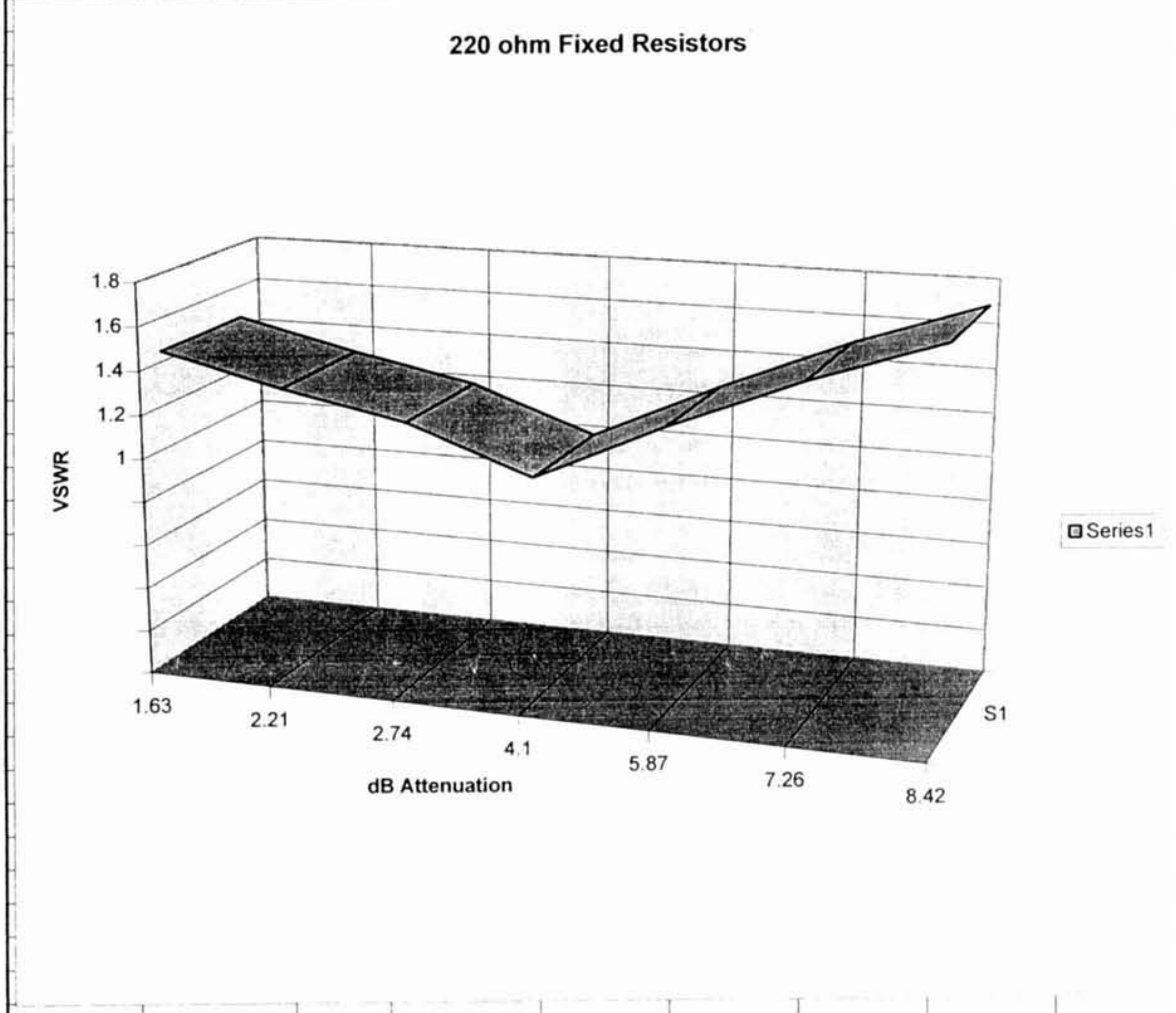

Figure 7. Pi-network resistive attenuator, 220-ohm fixed resistors to ground.

Pi-Network Resistive Attenuator			
1000 ohm Fixed Resistors to Ground			
Pot Value ohms	**Attenuation dB**	**VSWR x:1**	**Reflection Coefficient**
0	0.41	1.1	0.048
5	0.87	1	0
10	1.28	1.09	0.043
25	2.35	1.35	0.15
50	3.73	1.78	0.28

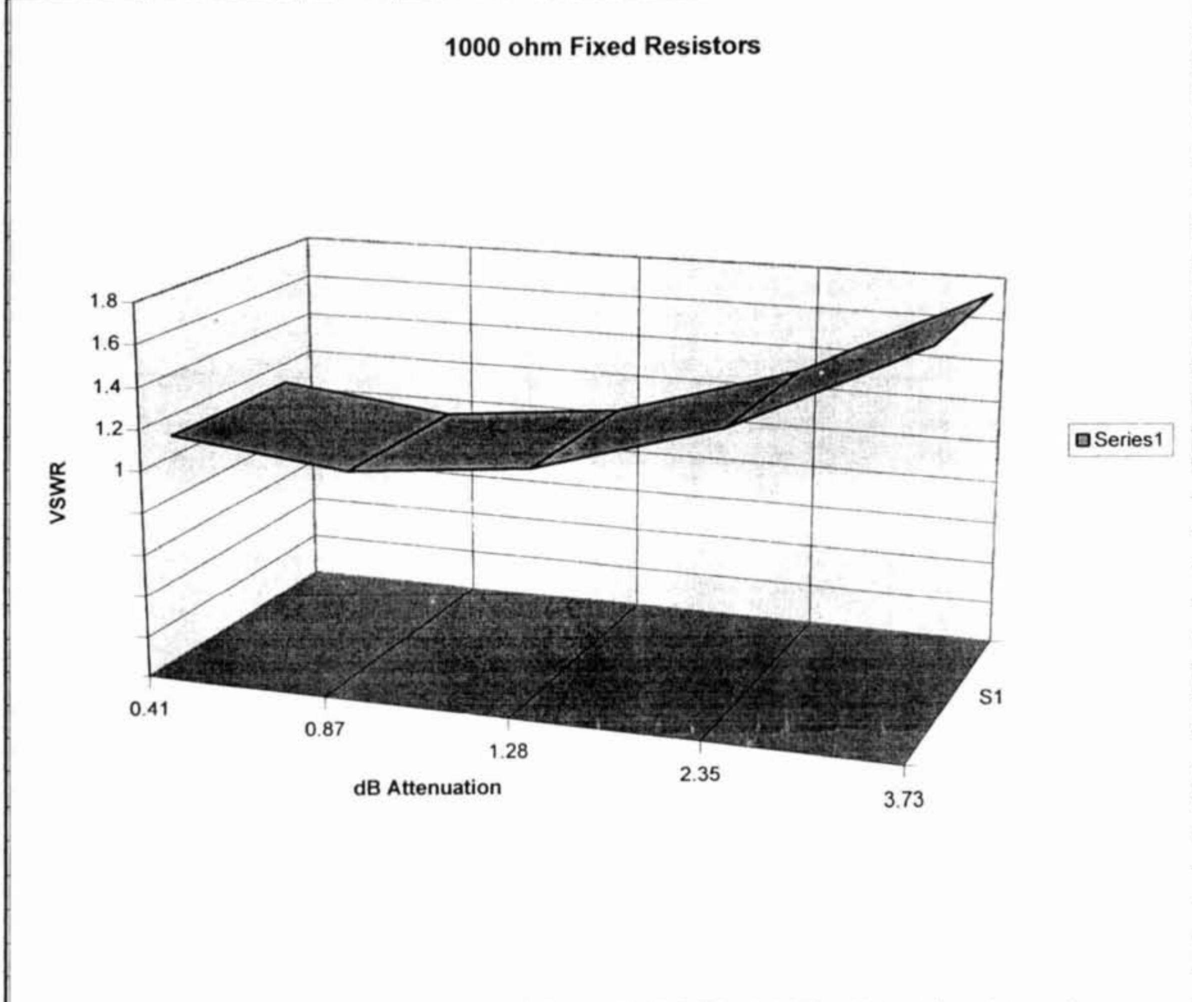

Figure 8. Pi-network resistive attenuator, 1000-ohm fixed resistors.

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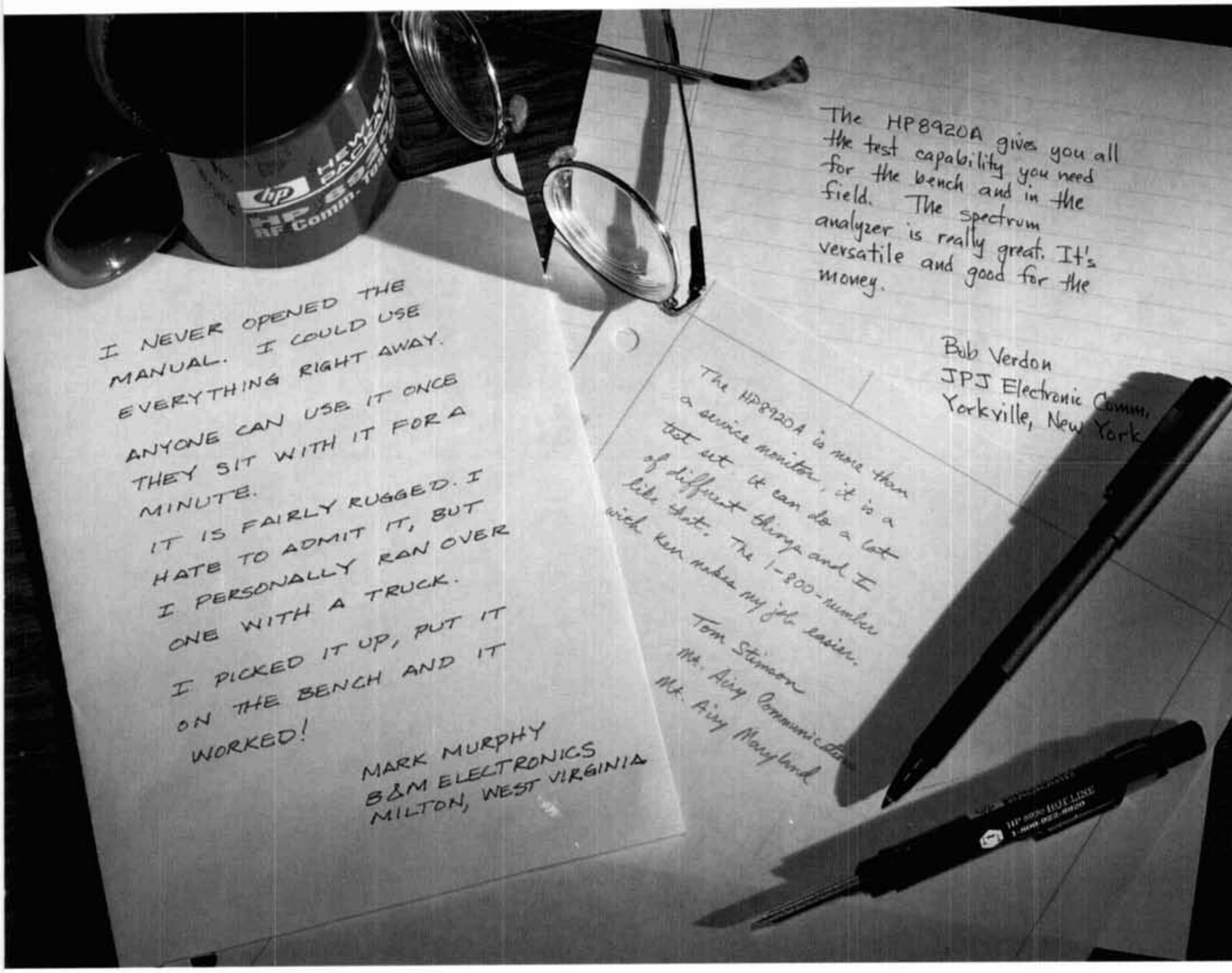

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