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Fall 1996

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Svetlana
ELECTRON DEVICES

3CX2500A3
3CX2500F3
3CX2500H3
3CX3000A7
3CX3000F7
3CX6000A7/YU148
3CX10,000A3
3CX10,000A7
3CX10,000H3
3CX15,000A3
3CX15,000A7
3CX15,000H3
4CX250B
4CX250BC
4CX250BM
4CX250BT
4CX250R
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4CPX800A
4CX1500A
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4CX1600U
4CX3500A
4CX5000A
4CX5000R
4CX7500A
4CX10,000D
4CX15,000A
4CX15,000J
4CW10,000A
4X150A/7034
5CX1500A
5CX1500B
572B
5U4G
6AS7G
6BM8
811A
833A
8560AS
EF86
EL34
EL509/6KG6
SV572-3
SV572-10
SV572-30
SV572-160
SV6550C
SV6L6GC
SV811-3
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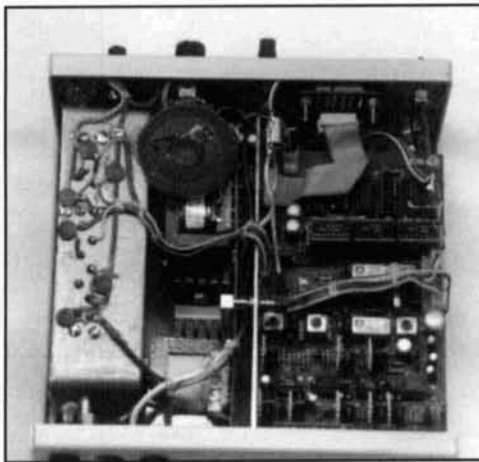
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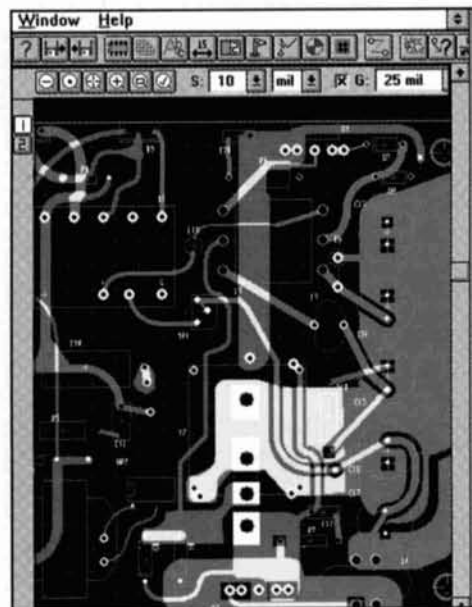
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On the Cover: Boundary scan technology lets designers detect board level defects—often to the IC pin level. To find out how the nature of modern high-density pc board and component testing is changing, see "Boundary Scan Technology," beginning on page 9. Cover photo and article by Bryan Bergeron, NUIN.

EDITORIAL

From On-Air Ragchew to Online Chat: Hams and the Internet

A curious (some would say ominous) change is afoot. Many, many hams are passing over their radios in favor of their computers and are doing their ragchewing online rather than on the air.

What's the attraction?

If you're into the technical side of amateur radio, the numerous online nets and chat sessions on radio topics can provide the mental stimulation often lacking on the bands today. Just about every subject of interest to radio amateurs has a meeting place online. There's the homebrew group, the equipment group, and the DX net to name a few.

It's great to see how many of the most well-known hams meet at the antenna news group, for instance, where members discuss such topics as coax, baluns, and the best antenna designs. Conversations are generally polite, although they can become pretty heated when vastly divergent views are expressed. Discussions die down for a time and then rekindle as members put forth new theories.

Why not on the air?

But why not have these same conversations on-the-air? After all, the original premise of amateur radio was to provide a vehicle for experimentation and research, as we followed in the footsteps of early pioneers like Marconi, deForest, and Armstrong. What's wrong with the old ways?

Have you tried to have a serious technical discussion on the air, lately? It's tough. The airwaves are filled with guys discussing their medical problems, calling their buddies from hunting camp, maintaining schedules with other amateurs, etc.

It's not exactly a great climate for the sharing of ideas, is it? Those who want a little more substance in their technical diet, now know they can find it on the net.

The end of ham radio?

Does the proliferation of the online radio chat signal the demise of ham radio as we know it? Probably, but this change is not a death knell! After all, these online-hams *are* discussing amateur radio. They're still working to learn better ways to put more metal in the air, build or modify equipment, improve their stations, or perfect their contest techniques.

When computers first came on the scene, many of us said, "No way will I have one of those things in my shack!" Years later, we've traded our Commodores for Pentiums so we can run antenna optimization and circuit design programs. We have our *Callbooks* on CD-ROM and keep track of our contest QSIs using special logging programs. And, we use all these aids to help us *on the air*.

Radio still has its place

Amateur radio still provides a very important service both here and abroad. Radio enables us to provide support during natural and manmade disasters and communications for community events. (In the worst conditions, a CW signal is still the only one that gets through.) The ham community offers the disabled a way to join the world and provides company to those who must travel the roads late at night. And, by talking to astronauts on the Space Shuttle and cosmonauts on Mir, our children can experience the wonder of voices through the ether—just like our earliest radio explorers.

Given all that radio still provides, it's doubtful that computers will pull all the hams from the airwaves any time soon. Online radio groups are simply adjuncts to those on the air. I, for one, am not going to worry until these hams stop talking radio and start talking computer networking!

Terry Littlefield, KA1STC
Editor

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TECHNICAL CONVERSATIONS

Not excited about SETI

Dear Editor:

I have never been able to get excited about SETI ("SETI Made Simple," Spring 1996).

It is not that I doubt the possible existence of other intelligent beings in space, but it would seem that because of the vast distances involved, any possibility of two-way communication is unlikely.

If we did receive some kind of message, could we ever understand it? These beings certainly went through a very different evolutionary process than we did, and their thought patterns might be incomprehensible to us. We have not yet deciphered ancient Etruscan, which was spoken by human beings like us right here on Earth.

I have read many articles on SETI over the years, but I had never read Dr. Drake's book.* I got a copy from the library and found it very interesting. Some of Dr. Drake's speculations on the possible nature of alien civilizations are pretty far out.

I sometimes think that what SETI is really looking for is a father figure out in space who will tell us how to solve our earthly problems of nuclear weapons, overpopulation, and destruction of the environment.

Of course, we know the solutions to these problems. We just lack the will to solve them.

**Harry R. Hyder, W7IV
Tempe, Arizona**

**Is Anyone Out There*, Frank Drake and Dave Sobel.

Reader says article fell short

Dear Editor:

The Summer 1996 article "4CX400A Russian Tubes for the MLA-2500 Amplifier," by Bob Alper (product manager, Svetlana), fell short of properly representing the 8875's true performance. It also fell short in several other important technical areas. Readers not fully experienced with the operation and design of tetrode amplifiers should be advised to avoid making this conversion as published.

While page 29 (**Table 1**) contains data extracted from Eimac's 8875 typical operation tables, the data is not an accurate representation of Eimac's typical operating guidelines. **Table 1** is a worst-case mixture of several unrelated type parameters. This table lists the 8875's anode voltage as 2200 volts, while anode current is specified to be 500 mA. **Table 1** gives the incorrect impression that an 8875 would typically be operated with 1100 watts

input while delivering 505 watts output, with an efficiency of 46 percent and a dissipation of 595 watts.

A look at Eimac's published data shows the 8875 analog voltage used in **Table 1** is actually the *absolute maximum* allowable operating voltage, 2220 volts. The 8875 plate current was extracted from another absolute maximum—the single tone IVS rating. This incorrectly extracted data inflates the plate input power of the 8875.

On the other hand, power output was extracted from 432-MHz specifications. This provides the lowest possible output power for the 8875. When an input power well beyond the actual maximum input power is combined with reduced UHF power output, any tube can be made to "appear" as a very poor performer.

In reality the 8875, at 30 MHz, delivers 587 watts with a plate input of 500 mA at 2000 volts. Efficiency is 59 percent, not **Table 1's** incorrect value of 46 percent.

While tetrodes have their advantages, they also have pitfalls. In fairness to both builders and other amateurs sharing bands with tetrode users, we should all be aware of potential problems associated with amateur use of these grid-driven tetrodes.

Tetrode amplifiers demand much greater design and operating skill than more simple grounded grid triode amplifiers. Even the best tetrode PA designs can become horrible performers if the PA is slightly overdriven or underloaded. Tetrodes are quicker to distort and splatter when mistuned or overdriven. Tetrodes are extremely sensitive to screen regulation and control grid current.

Tetrodes are easy to drive and Svetlana tetrodes are inexpensive, but grounded grid triodes are much more tolerant of operating and design errors.

Dynamic and long-term screen grid voltage regulation must be excellent, or the tetrode will cause distortion. This distortion can fail to surface in conventional two-tone tests, where the low frequency syllabic amplitude variations of speech are not included. With improper circuit design, a tetrode can appear "clean" in a casual on-the-air or two-tone test, but if supply voltage, drive power, or loading change, a "clean" signal can quickly become an IMD nightmare.

The desired characteristics of a shunt-type tetrode screen regulator are straightforward. It must have excellent regulation with changing load currents. This includes load variation rates extending from very long time intervals to fractions of a millisecond. Regulator dynamic impedance should be a small fraction of the lowest expected screen grid impedance. The screen

supply must remain stable with changes in temperature, line voltage, and power supply loading.

The screen supply shunt regulator shown on page 34 fails to meet any of these requirements. It is powered from a weak voltage tripler circuit. It is operated from an inadequately designed winding on the same transformer that supplies anode current. Even worse, the unstable voltage shunt regulation device (Q1) is applied through a 10,000-ohm resistor. The 10,000-ohm resistor destroys regulation, and also allows negative screen current to “lift” the supply (exactly what we don’t want). There is no screen over current protection, and the screen supply is not interlocked with anode or bias supplies. Finally, the schematic on page 35 shows the electrolytics connected backwards.

The control grid circuit is also improperly designed. The grid swamping resistor is located near the input relay, even though proper placement dictates it be placed as close as possible to the tube’s grid terminals. If the user intends to drive the amplifier with a 10-watt PEP or larger exciter, he’s destined for problems. Virtually every exciter on the market suffers from ALC response time shortfalls. Inherent ALC or power control response time limitations cause the leading edge of speech to overshoot the average power setting. Reducing the output of a modern solid-state exciter to 10 watts not only will increase splatter from ALC overshoot, it often reduces IMD performance of solid-state exciters by moving operation away from factory design values.

It isn’t very difficult to correct the grid circuit. The correct formula for the grid resistor in a AB1 amplifier (neglecting intentional or unintentional feedback) is found by the following:

$$R_g = 2Pd/E_b^2$$

Where Pd is actual drive power available at the grid and Eb is 1/2 grid bias.

The correct resistance for 100 watts of excitation with 35 volts of bias is 1.53 ohms. This assumes grid and other losses are negligible (in most cases some experimentation may be required). It isn’t surprising a 50-ohm grid resistor allows this amplifier to be driven with a 10-watt exciter. Fifty ohms is the correct value for 3 watts of grid excitation (no feedback)!

An L pad may be the best solution, allowing 50-ohm exciter termination and proper drive levels. In this case, resistance values are determined by finding the peak current available with a 50-ohm load, and using this current value to calculate L pad resistances. The formula would be:

$$I_{pk} = 1.414 \sqrt{Pd/50}$$

and

$$R_g = E_g/2I_{pk}$$

Where Eg is the full grid bias. The series input resistor is found from:

$$R_s = 50-R_g$$

In the case of a 35-volt bias tube and a 100-watt exciter, Rg would be around 10 ohms and Rs around 40 ohms. The exciter would “see” 50 ohms and the tube would be stabilized by the 10-ohm grid swamping resistor, and 100 watts of drive could be safely applied without distortion of ALC overshoot problems. In the event circuit losses prove more drive is needed, the resistor ratio can be modified.

With proper control grid and screen supply circuitry and careful attention to operation, the 4CX400A would be a good choice to replace expensive 8875s. The circuit presented, however, is an IMD disaster waiting to happen.

**Tom Rauch, W8JI
Conyers, Georgia**

On surface mount construction

Dear Editor:

Brad Thompson, AA1P’s letter in the summer 1996 issue raises some points.

Surface mount isn’t anything hams should be afraid of. This is just another generation of technology, like all the others we’ve been through in the last 40 years, and it’s nowhere near as big a jump as the transistors we were supposedly never going to embrace. (“Hams will always be tube men”—remember that?) As usual, there are benefits and drawbacks, and a little relearning to do.

He’s right about us seldom needing the degree of miniaturization that SMT allows. However, miniaturization isn’t the reason why so much hardware is going surface mount. It’s cheaper. In a lot of cases, SMT designs just work a whole lot better, too. The reason is that shortening up the conductors drastically reduces strays.

For instance, the inductance of a typical pin in a DIP package is around 10 nanohenries, from the bonding pad on the chip to the solder joint on the pc board. For a SOIC, it’s more like 3.5 nH. This makes a heck of a difference if you’re trying to make logic run fast, or build a nontemperamental UHF circuit. In the first generation of really fast CMOS logic ICs, it turned out that the peak current through the ground and V_{CC} pins when driving a reasonable capacitive load was so high, and rose so fast, that the transient voltage developed across the pin inductance was more than the noise margin. [Remember, V=-L(di/dt).] This was the infamous “ground bounce”—even if the board had a rock-solid ground plane, the so-called “ground” pad *on the chip* would jump like a kangaroo. So, if the IC had more than one output, the outputs that weren’t switching would

transmit big glitches to their loads. Texas Instruments attacked the problem by assigning multiple pins to ground and V_{CC} , and moving them from the corners of the package to the center, all to get the stray inductance down. But in the end, the industry abandoned through-hole packages for fast logic.

Similarly, it just isn't possible to get the series inductance of a bypass capacitor nearly as low with leads as with a naked chip. Making the parts very small also shortens the interconnecting tracks, bringing down not only the track inductances, but also the capacitances between nearby runs. A lot of runs get short enough to be treated as simple conductors instead of transmission lines, too.

Now, what's it like to work with SMT? Not all that bad. I had to learn to design with this stuff a couple of years ago, when I went to work for Modutec, Inc. of Manchester, New Hampshire, a company that makes digital panel meters.

As you'd expect, the right tools make it a lot easier to work with these little parts. A lighted bench magnifier helps a whole lot. A hot-air rework station would be ideal if you can find one second hand, but we get by in the lab quite well with decent tweezers and a temperature-regulated soldering iron with an assortment of small tips. Solder wick comes in handy for loosening multi-pin parts; so does a collection of desoldering tips (which can be homemade).

Disadvantages of surface mount? Well, the biggest problem I've run into so far is that some of the critical components needed for high-precision analog instruments just don't exist in SMT form. Sometimes it's because there isn't enough demand to interest a component manufacturer; sometimes it's because nobody's figured out how to make the thing, and sometimes it's because it's flat-out impossible. That's when we figure out the sneaky workarounds we don't tell our competitors about.

Breadboarding with SMT parts? We do it sometimes, usually mixed with through-hole parts on perfboard. It calls for #30 bus wire and Teflon™ sleeving, and no-clean rosin-core solder.

I think the time isn't too far away when hams will routinely work with surface mount. It's just going to take some time and familiarization, and the availability of low-cost tools.

**John A. Carroll, AB1Z
Nashua, New Hampshire**

Correspondence from Cornell,
WB3JZO

Dear Cornell:

About a year and a half ago, in an issue of *Communications Quarterly* ("Build a High-

Performance, Low-Profile, 20-Meter Beam, spring 1993, page 84), I ran across your article about the 20-meter shortened Yagi. Because I am a DXer and absolutely cannot put up a tower on my property. I decided that it might be perfect for my situation and built it last spring. Having used it now for almost a year, I am quite impressed with it. It's up on a 40-foot guyed mast hidden between some trees in the back yard. Third contact with it was Rolf, XV7SW, in Hanoi....Now I'm up to about 275 countries worked in less than a year and a half. Because I needed an antenna project for this summer and am having more and more trouble breaking the pileups as the new ones get harder and harder to come by, I decided I wanted more out of the antenna and would like to add a third element to it.

I was wondering if you had ever played with the idea of a third element on this design, and whether you might have any constructive suggestions for adding a third element. I imagine that the matching scheme will have to be changed, but rather than trying to guess and check or figure it out, I thought I would write you for any suggestions.

If you can offer any help, please let me know. Thanks and 73.

**Tom Schwabel, N2WLG
Clarence, New York**

Dear Mr. Schwabel:

I have no specific suggestions regarding upgrading the two-element shortened Yagi to a three-element array. I never contemplated this because my antenna was intended as the best performer for the size, and the size was the most important feature. Then came the outstanding performance that you noted.

Judging by the amount of time it took me to design and implement the current antenna, I would think that it would take an effort to maximize it for a three-element version, despite how simple it may look after it is done. If you are interested in pursuing such a project, I recommend that you take a good look at the book *Yagi Antenna Design* by James Lawson published by ARRL. Only then, would I pursue a new design.

For your information, my antenna has been recently competing favorably against some five and seven-element arrays into the YO-land from my QTH here in Arizona. While the two-element shortened beam cannot totally compete, repeated tests indicate signal reports of only one or two S-units under these large arrays. Not bad for such a small array mounted on a chimney. Good luck with the project.

**Cornell Drentea, WB3JZO
Tucson, Arizona**

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SL-11R	•	•	7	11	2 5/8 x 7 x 9 3/4	12
SL-11R-MC	•	•	7	11	5 3/4 x 7 1/4 x 9 3/4	13
SL-11R-GE	•	•	7	11	5 3/4 x 7 x 9 3/4	13
SL-11R-RA	•	•	7	11	4 3/4 x 7 x 9 3/4	13
SL-11R-EFJ	•	•	7	11	5 1/8 x 7 1/4 x 9 3/4	13
SL-11MG	•	•	7	11	5 1/8 x 7 1/8 x 9 3/4	13
SL-15R	•	•	12	15	2 5/8 x 7 x 9 3/4	13
SL-15R-GE	•	•	12	15	5 1/8 x 7 5/8 x 9 3/4	14
SL-15R-RA	•	•	12	15	4 3/4 x 7 1/4 x 9 3/4	14
SL-15R-EFJ	•	•	12	15	5 1/8 x 7 1/8 x 9 3/4	14

RS-L SERIES



- POWER SUPPLIES WITH BUILT IN CIGARETTE LIGHTER RECEPTACLE

MODEL	Continuous Duty [Amps]	ICS* [Amps]	Size [IN] H x W x D	Shipping Wt. [lbs]
RS-4L	3	4	3 1/2 x 6 1/8 x 7 1/4	6
RS-5L	4	5	3 1/2 x 6 1/8 x 7 1/4	7

RM SERIES



MODEL RM-35M

- 19" RACK MOUNT POWER SUPPLIES

MODEL	Continuous Duty [Amps]	ICS* [Amps]	Size [IN] H x W x D	Shipping Wt. [lbs]
RM-12A	9	12	5 1/4 x 19 x 8 1/4	16
RM-35A	25	35	5 1/4 x 19 x 12 1/2	38
RM-50A	37	50	5 1/4 x 19 x 12 1/2	50
RM-60A	50	55	7 x 19 x 12 1/2	60

• Separate Volt and Amp Meters

RM-12M	9	12	5 1/4 x 19 x 8 1/4	16
RM-35M	25	35	5 1/4 x 19 x 12 1/2	38
RM-50M	37	50	5 1/4 x 19 x 12 1/2	50
RM-60M	50	55	7 x 19 x 12 1/2	60

RS-A SERIES



MODEL RS-7A

MODEL	Colors		Continuous Duty [Amps]	ICS* [Amps]	Size [IN] H x W x D	Shipping Wt. [lbs]
	Gray	Black				
RS-3A	•	•	2.5	3	3 1/4 x 5 3/4 x 5 3/4	4
RS-4A	•	•	3	4	3 3/4 x 6 1/2 x 9	5
RS-5A	•	•	4	5	3 1/2 x 6 1/8 x 7 1/4	7
RS-7A	•	•	5	7	3 3/4 x 6 1/2 x 9	9
RS-10A	•	•	7.5	10	4 x 7 1/2 x 10 3/4	11
RS-12A	•	•	9	12	4 1/2 x 8 x 9	13
RS-12B	•	•	9	12	4 x 7 1/2 x 10 3/4	13
RS-20A	•	•	16	20	5 x 9 x 10 1/2	18
RS-35A	•	•	25	35	5 x 11 x 11	27
RS-50A	•	•	37	50	6 x 13 3/4 x 11	46
RS-70A	•	•	57	70	6 x 13 3/4 x 12 1/8	48

RS-M SERIES



MODEL RS-35M

MODEL	Continuous Duty [Amps]	ICS* [Amps]	Size [IN] H x W x D	Shipping Wt. [lbs]
RS-12M	9	12	4 1/2 x 8 x 9	13
RS-20M	16	20	5 x 9 x 10 1/2	18
RS-35M	25	35	5 x 11 x 11	27
RS-50M	37	50	6 x 13 3/4 x 11	46
RS-70M	57	70	6 x 13 3/4 x 12 1/8	48

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• Separate volt and Amp meters

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	@13.8VDC	@10VDC	@5VDC			
VS-12M	9	5	2	12	4 1/2 x 8 x 9	13
VS-20M	16	9	4	20	5 x 9 x 10 1/2	20
VS-35M	25	15	7	35	5 x 11 x 11	29
VS-50M	37	22	10	50	6 x 13 3/4 x 11	46
VS-70M	57	34	16	70	6 x 13 3/4 x 12 1/2	48

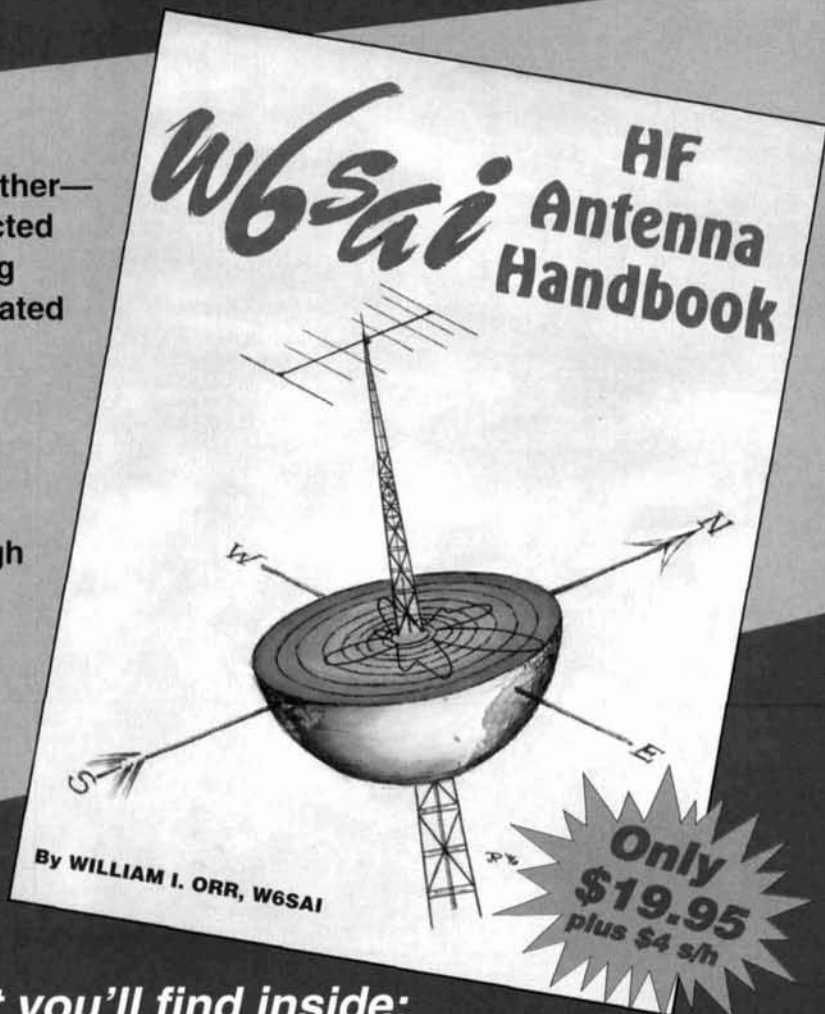
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VRM-50M	37	22	10	50	5 1/4 x 19 x 12 1/2	50

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BOUNDARY SCAN TECHNOLOGY

*Addressing the challenge of testing
complex components and circuits*

Despite the romantic image of simpler times in days gone by, complexity is a fundamental and necessary part of modern life. We live in a society with more people, a greater hunger for information and communications, and an ability to feed this hunger by developing technologies at an exponential rate. Look at the trend in communications technology. We've moved from equipment based on massive power supplies, a few vacuum tubes, resistors, and capacitors to portable, battery-powered, microprocessor-controlled units containing thousands of transistor junctions in the form of high-density ASICs.

Of course, the down-side of this complexity is that there's simply more to go wrong—even when reliability is a goal. In the world of electronics, designing for reliability once focused on criteria like expected component or equipment life, as expressed in maximum mean time between failure (MTBF). However, with the increasing density and complexity of ICs and other components, emphasis has shifted to automated design verification, designing for testing (DFT), and automated testing techniques. Strategies based on logic modeling are being developed to make the verification of complex circuit designs more manageable. Similarly, automated testing equipment (ATE) has become an industry unto itself. ATE techniques—including X-ray and infra-red inspection of components and boards, robotic probing of circuit boards, and microprocessor-controlled evaluation of components and PC boards—are now commonplace.

Automated testing technologies have made it possible for relatively naive users to at least

identify faulty electronic components and systems, even though they may not understand (or want to understand) the low-level circuitry. The self-test feature found in many desktop printers is a case in point. By providing users with a self-test feature, printer manufacturers not only equip them with a means of quickly identifying the source of a printing problem (e.g., is the printer or the print driver at fault?), but also reduce the number of technical support calls and needless printer returns.

In a move akin to that made by the printer industry, many IC manufacturers have provided designers with a type of self-test feature that can be used to simplify the testing of complex circuits. However, conventional internal tests, which isolate ICs from surrounding circuitry and exercise their internal logic, are costly to create—especially in complex ICs. In addition, such tests don't assist in detecting defects at all levels within the circuit; e.g., at the board level. One of the most exciting advances in automated testing, and one that was originally developed to detect board-level defects, is called boundary scan. Boundary scan technology provides designers with a means of detecting board-level defects, often down to the level of the IC pin. Follow along for a discussion of how this exciting technology is changing the nature of modern, high-density PC board and component testing.

Component and board testing

Before the introduction of multi-chip modules, surface mount components, and ultra-high

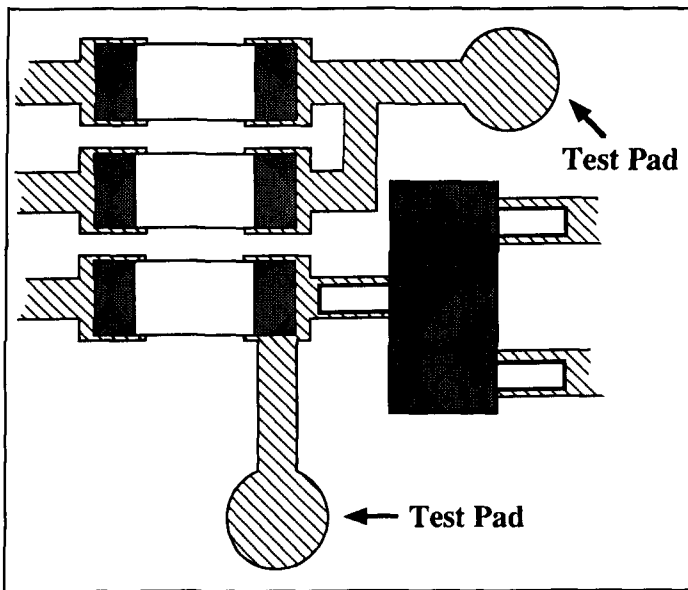


Figure 1. Providing test points for physical access limits maximum circuit board density. As illustrated here, the leads of surface mount (SMT) components are often too small to be probed manually, requiring that space consuming test pads be laid down on the pc board.

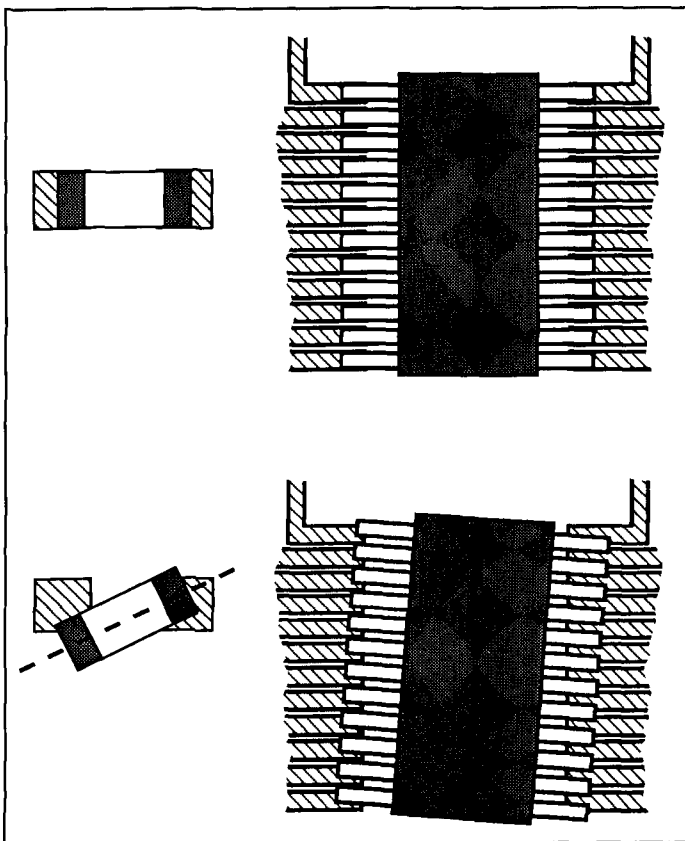


Figure 2. One of the challenges of working with modern, high-density components is the accuracy with which components must be placed and soldered. Whereas simple SMT components, such as SMT resistors (left) have a relatively high tolerance to placement inaccuracies, high-density, high contact count SMT ICs must be very accurately mounted to avoid multiple shorts and opens on the pc board.

density IC packaging, testing usually involved the use of multimeters, oscilloscopes, frequency counters, and similar manually operated instruments. Special IC clip-on probes, meters with sample-and-hold features, and even meters with audio announcement of measurements have been developed in an attempt to make the measurement task less arduous. However, the leads used with many surface mount IC designs are either not accessible (e.g., hidden from view) or simply too fine and densely packed to be probed by even the most skilled technician. Look at a modern multi-chip module, composed of a dozen VLSI chips, with over a hundred hair-thin edge-connectors and you'll appreciate the difficulty of identifying, much less manually probing, surface-mount IC leads.

Automated testing jigs, in which machine-operated probes simultaneously test the 64, 128, or more leads of a single IC are useful when the IC leads are physically accessible. However, it often isn't merely a question of a steady hand and micro-fine probe; you can't test a pin that's hidden under the body of an epoxy-coated, multi-pin microprocessor, an add-on daughter board, or other IC.

Of course, getting to a particular IC pin is just a small part of the testing challenge. There isn't much you can do with the signals from a particular pin on a microprocessor or other complex IC, unless you have a means of storing and analyzing the data. It's an almost impossible challenge for most of us to troubleshoot our modern transceivers with only a signal diagram and conventional tools. Microprocessor-controlled testing equipment, with a means of storing and analyzing complex data interactions, is a must for serious analysis of modern digital circuit boards.

Even when automated probing and measurement systems are available, circuit board designers are often faced with the need to sacrifice density (and therefore the minimum circuit trace length and overall device size) to accommodate physical access. The measurement problem isn't limited to ICs in complex digital systems; circuit board designers are often forced to provide test pads for boards densely populated with both conventional and surface-mount components (see **Figure 1**).

The challenge of testing isn't limited to troubleshooting problems that arise during the normal operating life of a device. Automated construction and soldering techniques, while making high-density circuit board construction both efficient and cost-effective, is not trouble free. As illustrated in **Figure 2**, a common problem in PC board manufacturing is the misalignment of SMT components. Although construction materials and techniques have been developed to address these challenges, there remains the

need to routinely assess the quality and functionality of boards as they roll off of the production line.

One solution to the access and testing dilemma has been to develop a means of testing components and connections electronically, with signals routed into and out of the pc board through edge connectors. Computer manufacturers, defense contractors, and other specialty fields have used electronic testing for several decades. However, until recently the electronics' industry as a whole couldn't apply or benefit from these proprietary technologies. In fact, these techniques were often viewed as a strategic advantage for the company that developed a means of electronically testing their components and boards.

Enter the Joint Test Action Group (JTAG) support for IEEE Standard 1149.1, "IEEE Standard Test Access Port and Boundary-Scan Architecture," adopted in 1990. This standard defines the architecture and functionality of test circuitry that can be incorporated in digital IC designs. By adding the on-board silicon required to conform to the standard, IC manufacturers have made it possible for circuit board manufacturers and designers to use standardized, electronic testing routines in evaluating the components and interconnections used on their boards. Boundary scan is meant to complement, not replace, conventional in-circuit testing and inspection of digital circuits.

Today there are hundreds of boundary scan compliant devices on the market, available from dozens of IC manufacturers. Digital ICs from any vendor can be used on a given circuit board with no change in the testing strategy, as long as the ICs support the boundary scan standard. In addition to simplifying the physical access problem, components adhering to the boundary scan standard support computer-controlled functionality testing, allowing a complete suite of tests to be developed in software. As described below, boundary scan techniques are equally applicable at the component, circuit board, and system levels.

Boundary scan

Exactly what is boundary scan, and how does it work? As suggested by the name, boundary scan test circuitry is placed around (that is, along the boundary of) the device logic of an IC—just inside the inside the I/O pins. The term *scan* refers to the test circuitry's function as a serial shift register during testing (a shift register is a digital storage circuit in which data are shifted from one position in a chain to adjacent positions on application of each clock pulse). The boundary scan standard defines boundary scan latches or scan cells at each IC

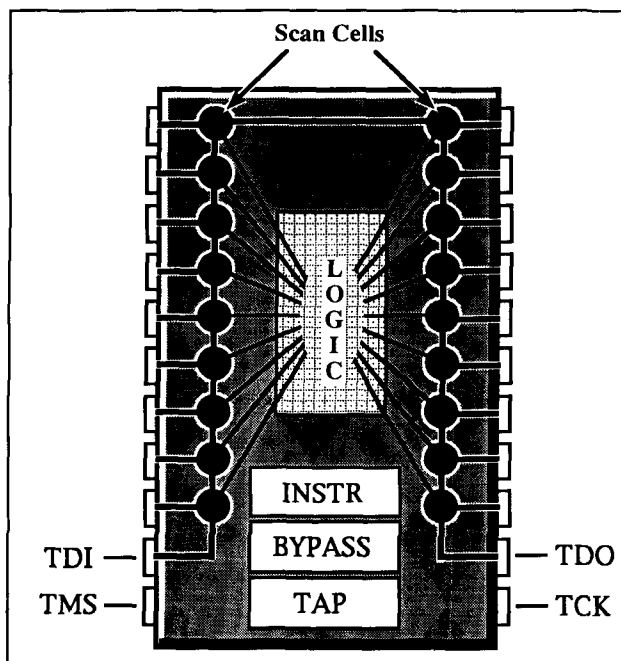


Figure 3. A functional view of a boundary scan compliant IC. Boundary scan cells, which are located on the boundary of the internal IC logic (LOGIC), are connected to each other in series, as well as in parallel with corresponding IC pins. Silicon dedicated to boundary scan operations include an Instruction Register (INST), a Test Access Port Controller (TAP), and a Bypass Register (BYPASS). Four pins are dedicated to boundary scan operation: Test Data In (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK). An optional fifth pin, Test Reset (TRST), is not shown.

I/O port. As shown in **Figure 3**, a series of these cells forms a shift register. The standard also defines a Test Access Port Controller (TAP), composed of four dedicated leads, that provides control for the IC test modes, and access to the scan cells.

As **Figure 3** shows, dedicated boundary scan pins include a Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select (TMS) pins. The TDI pin provides access to the string of scan cells, while the TDO pin allows data to pass out of the string, on to the next IC, or on to a data recorder for analysis. The TCK pin is used to control when data is shifted through the scan cells, and when the TMS pin communicates with the TAP Controller. An optional fifth pin, the Test Reset (TRST) pin, allows the component's test logic to be reset independently of the IC's internal system logic. An Instruction Register and Bypass Register complement the logic contained within the TAP controller and the scan cells. The Bypass Register provides a signal short cut, effectively bypassing the scan cells.

Boundary scan in action

A scan cell can be considered a single-bit (0

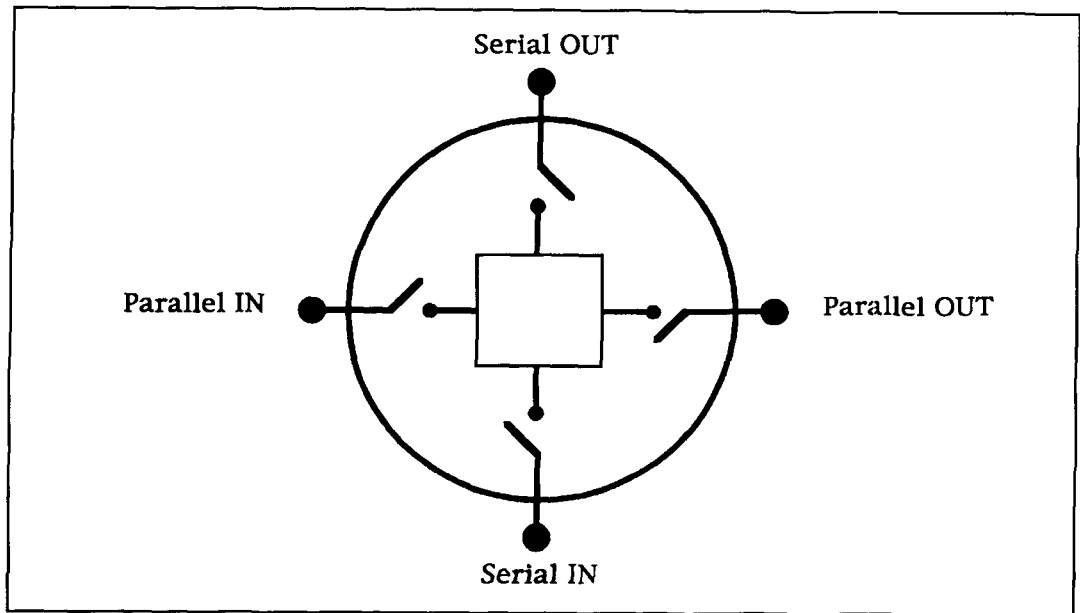


Figure 4. Scan cell operational description. Individually, scan cells can be thought of as 1-bit registers (e.g., capable of storing a “0” or “1” value), with two possible input ports and two possible output ports. Collectively, the scan cells can operate as a serial shift register.

or 1) memory device with two sets of switches (see Figure 4). When an IC is in a normal operating mode, these switches are configured so the data simply pass from the parallel input to the parallel output of each cell (see Figure 5A). In

this configuration, the boundary scan components shouldn't effect circuit operation. However, when used in the test mode, the scan cells can accept data from their serial or parallel inputs and pass these through their serial out-

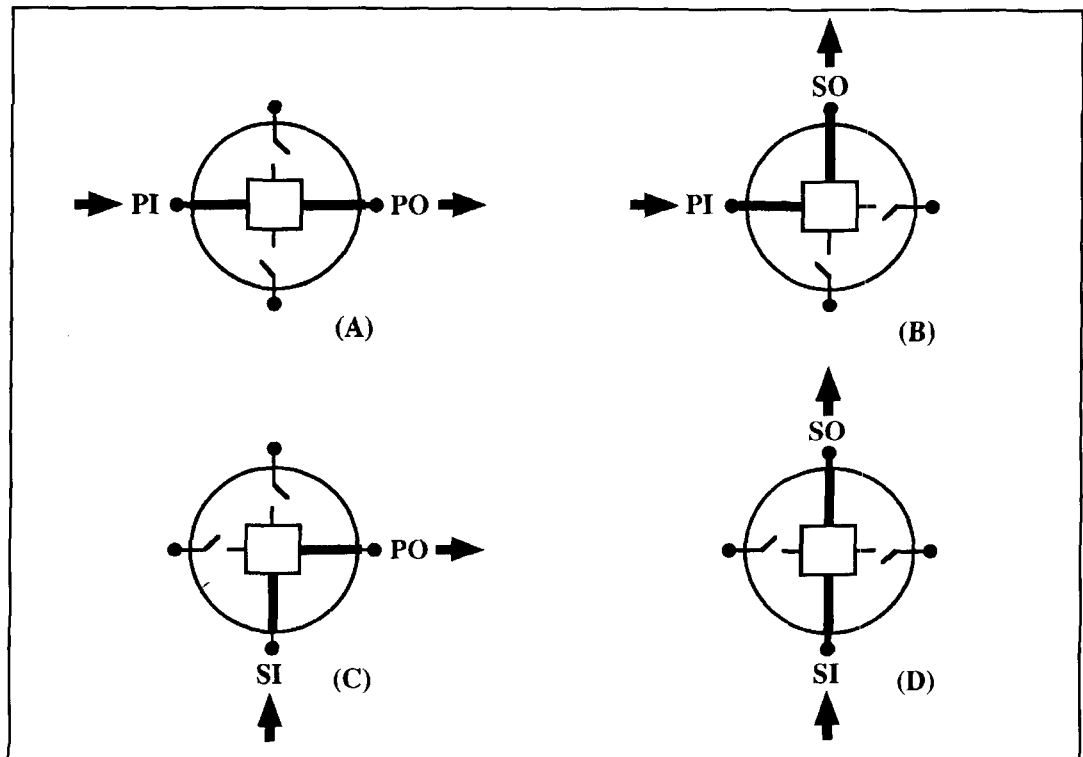


Figure 5. Four possible scan cell operational modes. (A) Parallel pass-through. (B) Parallel-to-serial shift register. (C) Serial shift register to parallel. (D) Straight serial shift register. In operation, scan cells can be configured to use the parallel and serial paths in a variety of combinations, allowing data to be moved where it's needed for testing. PI - Parallel In. PO - Parallel Out. SI - Serial In. SO - Serial Out.

puts, along the shift register. That is, data can be shifted serially around the boundary of the IC logic—the so-called scan path (see **Figure 6**).

Because the data can be shifted through parallel and serial paths in combination—e.g., the parallel inputs to the scan cells can be captured and serially shifted out of the component—any combination of input and output data can be created. For example, the parallel input data to an IC can be captured, converted to a serial string, and shifted around and out via the TDO pin (see **Figure 7**). Conversely, serial data from the shift register can be converted to parallel data on the IC output pins (refer to **Figure 8**). Yet another option is to completely bypass an IC altogether by using the Bypass Register (see **Figure 9**). In this way, a particular IC can be isolated and tested without the time penalty imposed by having to move data into, around, and out of other ICs in the boundary scan path. Regardless of the boundary scan features used, the main concept is that the internal logic of an IC can be ignored or “faked” by placing data on its input and output pins via boundary scan techniques.

At the circuit board level, several ICs are usually interconnected with each other and with other components, often in complex configurations. Regardless of how the application-specific leads of the ICs are interconnected, the scan cells of individual ICs are wired in series, with the TDO pin of one IC leading to the TDI pin of another. In contrast, the TCK and TMS pins are usually connected in parallel (see **Figure 10**). The parallel wiring of the TCK and TMS pins allows all boundary scan components on a pc board to be manipulated simultaneously.

A mixed world

Despite the widespread and enthusiastic acceptance of the boundary scan standards, only about 20 percent of current circuit board production is *completely* boundary-scan compliant. The other 80 percent of circuit boards contain noncompliant ICs that have either been in production for years or have very limited production runs. With the older ICs, there's pressure to stay with the *original packaging*, both to satisfy space requirements and minimize costs. Adding boundary scan capabilities to an existing IC design usually requires the switch to a larger package to accommodate the additional four or five pins. Also, it may not be economically feasible for manufacturers to expend the money and time required to add boundary scan capabilities to an IC design that may be near the end of its useful life. Similarly, it would be difficult to recoup boundary scan engineering costs on a limited production run of custom ICs. For these and other reasons,

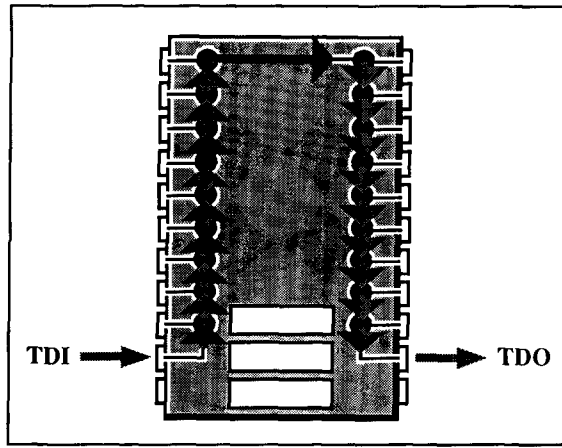


Figure 6. A boundary scan device with scan cells configured to act as a series shift register. Test data is passed around the boundary of the IC logic, along the scan path, from the TDI (Test Data In) pin to the TDO (Test Data Out) pin.

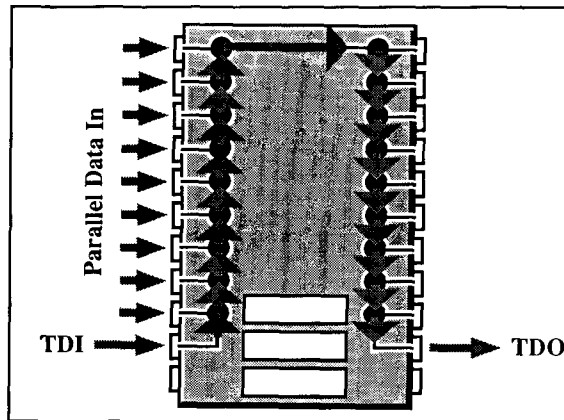


Figure 7. Using scan cells in a combination of operational modes makes complex tests possible. For example, the cells on the input side of an IC (left) can be configured as parallel-to-serial shift registers (*Figure 5B*) to capture the data on the input pins. By reconfiguring the cells as straight serial registers (*Figure 5D*), these values can then be serially sifted out of the IC through the TDO pin.

there will probably always be conventional, noncompliant ICs to contend with.

Although the presence of conventional ICs can complicate the testing of boundary-scan compliant ICs on the same pc board, the testing challenge is less arduous when there is full physical access to conventional components and their signal leads. In these cases, standard in-circuit tests, either under manual or robotic control, can usually be easily supplemented with automated boundary scan tests.

Working with a board populated with both congenital and boundary scan ICs is far more complex when there is only partial physical access to conventional ICs. In situations where

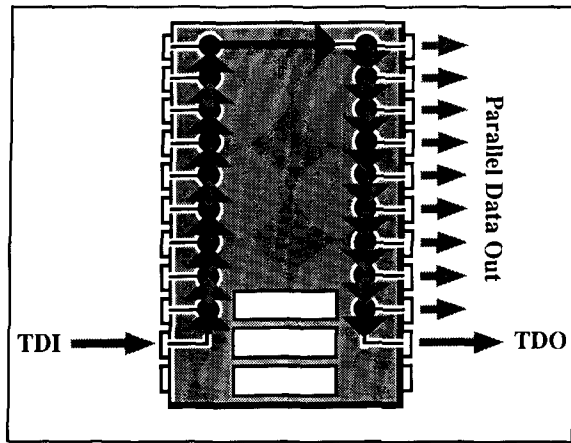


Figure 8. Serial data fed to the TDI pin can be shifted serially around the boundary of the IC logic and then output as parallel data by manipulating scan cell operation. Data are first moved along through straight serial shift registers (Figure 5D) and then moved from the serial shift register to parallel outputs (Figure 5C). Compare with Figures 6 and 7.

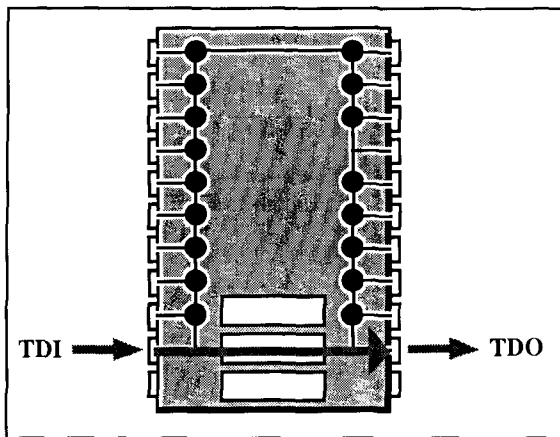


Figure 9. The Bypass Register can be used to bypass the scan cell serial shift register. This technique can be used to isolate chips from the test path, and to speed the test cycle.

a large number of conventional IC pins are simply unavailable for direct measurement. boundary scan tests can be devised that identify potential shorts between conventional and boundary scan ICs. Such tests are nontrivial to design, as they must eliminate all possible sources of ambiguity in the boundary scan test. Fortunately, automatic test generation (ATG) software is available to assist designers in creating appropriate boundary scan tests.

Detection capabilities

Overall, the goal of boundary scan technology is to provide an automated, electronically controlled means of detecting and identifying shorts, opens, correct component placement,

and component functionality. The specific boundary scan test used is a function of the circuit complexity, the nature of the ICs to be tested, the proportion of boundary scan compliant and noncompliant ICs on the pc board, the type of fault suspected, and the extent of physical access available for conventional probing and testing. Most faults can be described as either opens or shorts.

Opens—Opens can be the result of faulty traces, faulty soldering, or misalignment of components on the circuit board. **Figure 11** illustrates a possible test configuration for identifying opens in the IC signal path, from the scan cells to the circuit traces in the immediate vicinity of the IC. Data input via tester driver/sensor probes on the IC input leads can be verified by capturing the data with the corresponding scan cells. A discrepancy between the tester probe and scan cell values suggests an open. For example, one would expect a "1" on the driver probe to result in a "1" on the corresponding scan cell. A "0" on the scan cell would indicate an opening between the probe and the scan cell. Similarly, the state of the IC output pins, as set by boundary scan techniques, can be compared to the actual output measured by a sensor probe.

Figure 12 illustrates the ease with which opens can be detected between boundary scan compliant ICs, despite the lack of any direct physical access. Because all inter-IC signals are under the control of the boundary scan test, verifying signal path integrity is as simple as comparing the output data of one IC with the input of another.

As shown in **Figure 13**, boundary scan techniques can also be used to detect opens in circuits with a mixture of both compliant and noncompliant ICs, as long as physical access to noncompliant ICs is available. Again, driver probe values on signal traces would be expected at corresponding scan cells. Note that in situations where IC output data conflicts with driver probe data (e.g., IC output is "0" and driver probe value is "1"), the driver probe level predominates. In this way, single open traces, multiple opens to the same node, and multiple open pins on the same device (e.g., due to misalignment during the soldering process) can be diagnosed to the pin level.

Shorts—Shorts, which represent the most common fault in high-density circuitry, may result from solder bridges between closely spaced pins, misalignment of components during soldering, or defects in the circuit board manufacturing process. On a board populated with strictly boundary-scan compliant ICs, shorts can be identified without any physical access to the signal paths (see **Figure 12**). For example, two IC output pins can be set to dif-

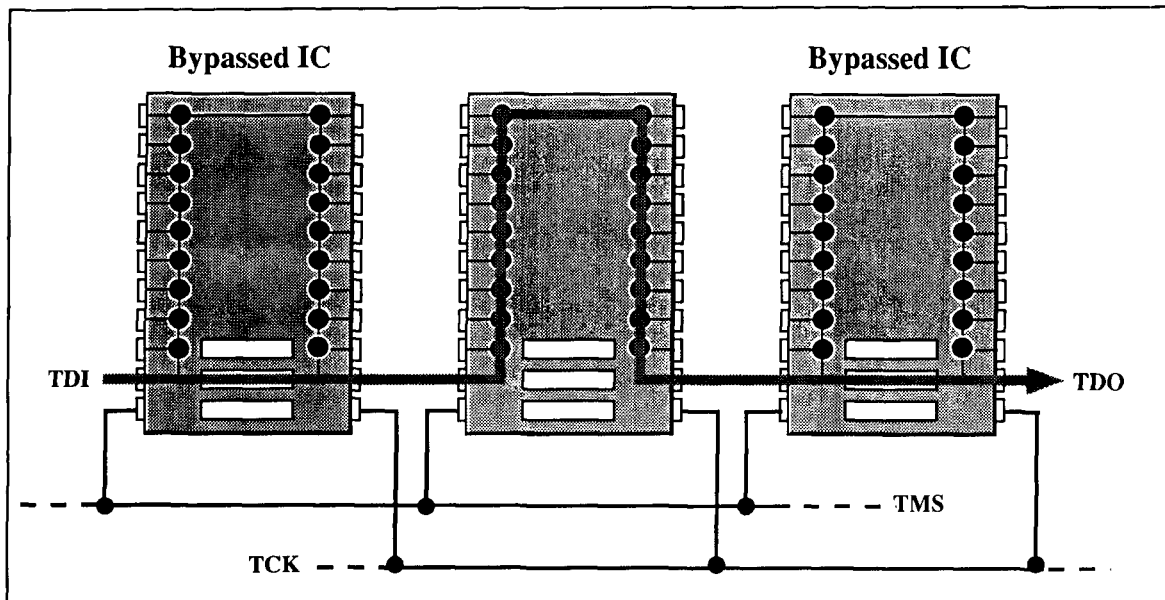


Figure 10. A possible test scenario in which two chips are bypassed (left and right), while one is under test (center). Note that both the Test Clock (TCK) and Test Mode Select (TMS) lines are wired in parallel.

ferent values—e.g., “0” and “1”—and the integrity of these values can be verified on the input pins of a second IC. Identical values on the input pins would suggest a short.

The magnitude of the potential short problem becomes apparent when you consider that, for a board with N nodes, there are $N(N-1)/2$ possible shorts—and a typical board might have 1000 or more nodes. The probable number of shorts is, in practice, somewhat less than the formula suggests, because it assumes that it is possible for any node in a circuit to be sorted to every other node in the circuit. This is a good figure to keep in mind, given that it’s often difficult to determine, even with visual inspection,

which traces are close enough at all points on a circuit board for a possible short to occur.

Boundary scan descriptive language

The boundary scan standards, as set forth by the IEEE in 1990, define component architecture requirements. However, it is only through the use of a standard language, the Boundary Scan Description Language (BSDL), that we can describe, and computers can read, how the boundary-scan circuits of a device are to be used. The language, which reads something

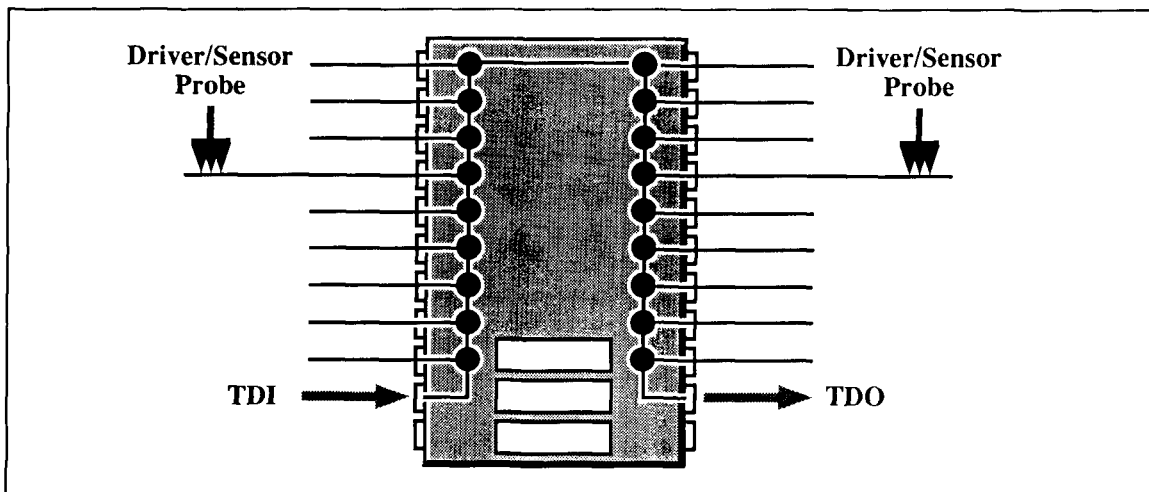


Figure 11. Faulty IC connections (opens), whether from defects in the IC pin, IC-to-solder pad joint, or the IC solder pads themselves, can be easily detected by using boundary scan techniques in conjunction with traditional testers. Only two tester probes (one on the input and one on the output side of the IC) are shown for clarity.

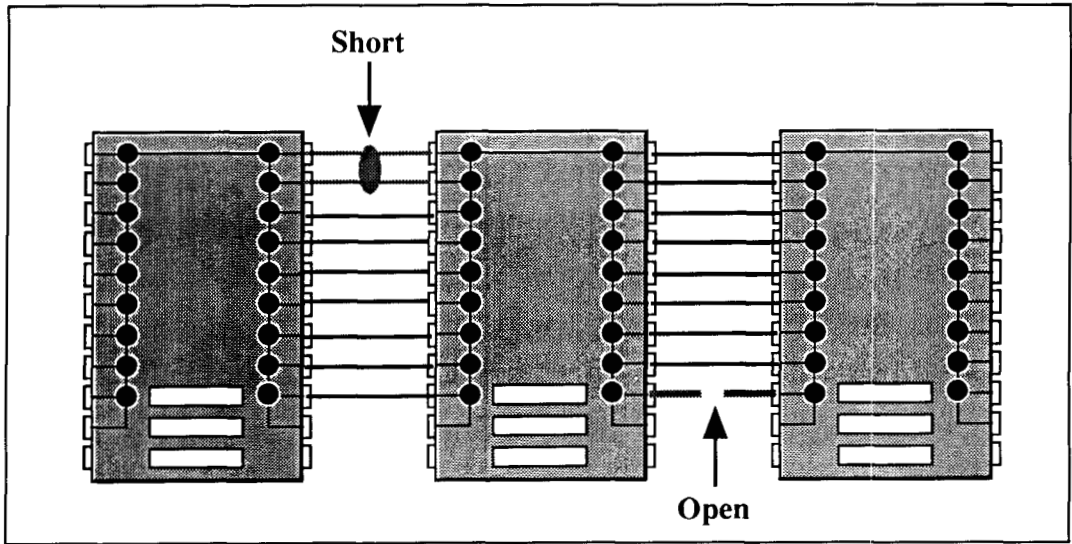


Figure 12. Boundary scan tests can detect shorts (left) and opens (right) between boundary scan devices, without any physical access to signal leads.

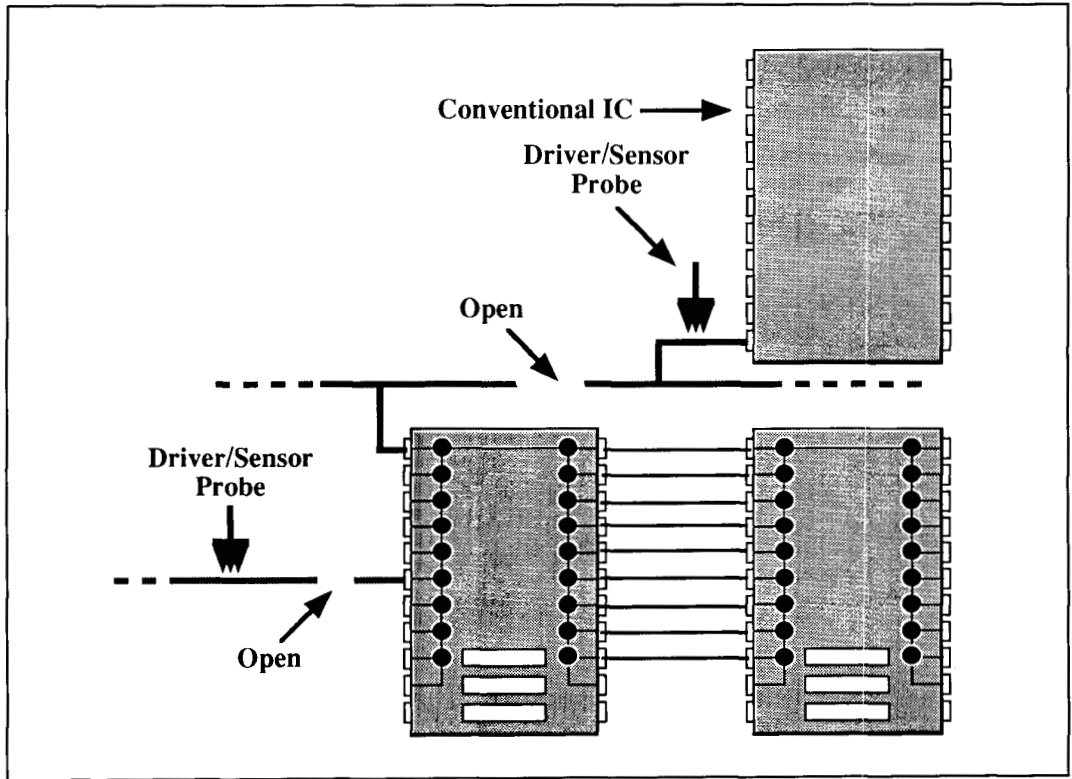


Figure 13. Open traces on the pc board between conventional and boundary scan devices can be detected with a combination of traditional and boundary scan tests.

like C, describes a number of parameters—including the pin-out, boundary-scan cell types, boundary-scan order, register length, instructions, control cell locations, control cell values, and I/O pin control cell. The more important instructions, EXTEST, INTEST, RUNBIST,

BYPASS, SAMPLE, PRELOAD, and HIGHZ are outlined in more detail below.

EXTEST—allows you to control the logic value at each output pin and observe the logic value at each input pin. EXTEST instructs the TAP Controller to capture input values, shift

them serially through the shift register, and update the output pins to the values held in the scan cells.

INTEST—isolates the IC from the circuit board, and provides a means of assessing the IC's internal system logic. Like EXTEST, INTEST uses a combination of capture, shift, and update operations, but uses them to apply data to, and observe output from, the internal system logic. Compared to conventional test methods, INTEST can be extremely slow, because every input pattern to be tested must be input serially. However, INTEST provides a mechanism for checking the internal logic without physical access to IC signal paths.

RUNBIST—instructs the IC to run a built-in diagnostic test. Of course, the IC manufacturer must have implemented such a test for this instruction to be useful.

BYPASS—moves test data directly from the TDI pin to the TDO pin, bypassing the shift register. This command is useful in isolating a particular IC, and in simplifying and speeding up test execution.

SAMPLE—samples the input pins' state while the IC is in its normal operating mode.

PRELOAD—allows initial logic values to be loaded prior to an INTEST or EXTEST instruction.

HIGHZ—sets all outputs to a high impedance state. This command is useful in providing in-circuit isolation.

Of course, it's the availability of software tools that make the design of boundary scan tests that rely on these low-level calls manageable. Fortunately, a number of vendors and IC manufacturers have devoted considerable energy toward developing easy-to-use boundary scan software tools.

Discussion

Boundary scan is one of the hottest and most promising technologies available for circuit board designers. However, despite its many advantages, boundary scan isn't perfect. For example, there's the overhead imposed by the need for extra silicon associated with boundary scan operations. IC yield tends to decrease with the addition of circuitry dedicated to boundary scan, simply because there's more that can go wrong. In addition, extra silicon and the associated test pins require larger package sizes (recall that boundary scan generally requires four and sometimes five dedicated pins). Finally, the addition of boundary scan capabilities to a device translates into increased design time, increased component cost, and a potential decrease in device performance. Not only must the boundary scan logic be properly designed

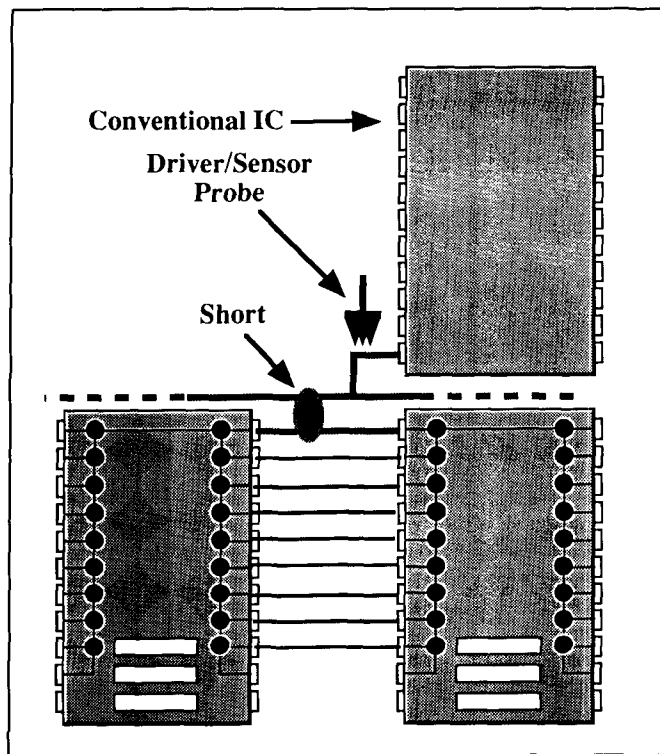


Figure 14. When testing for shorts between boundary scan and conventional ICs, a tester driver/sensor probe must be used on the conventional device leads.

and tested, but the added silicon can sometimes degrade IC performance.

Despite these limitations, boundary scan testing represents the most important new technology for board-level testing. And, like any technology, it will certainly continue to evolve to meet the needs of future designers.

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QUARTERLY DEVICES

PC Designer

There's a lot of fantastic PC-design software around these days, and most of it has enormous capability. Unfortunately, for the electronics student, experimenter, or prototype designer, the complexity and extended learning curve associated with many of these programs may prove too time consuming to be practical. In addition, RF designers may not be motivated to learn a CAD system heavily weighted toward laying out digital circuitry. In short, for some applications, simpler is better.

CAD made easy

PC Designer from Niche Software is an intuitive Windows-based program from the UK that enables experimenters to generate high-resolution, double-sided printed circuit artwork without mastering the protocol and complexities that go with a full-blown CAD package. PC

Designer runs on any 386-or-better PC running Windows and may be loaded from a single 3-1/2 inch disc or downloaded directly from Niche via the Internet. For undecided shoppers, a demo package is also available online.

I've been using this program for nearly a year and can attest to the fact that PC Designer is easy to master. The documentation package is simple enough: it consists of three typewritten pages, with additional support provided by a built-in HELP menu. PC Designer is highly visual and screen driven—almost anyone can boot it up and start laying out simple boards in a matter of minutes. It *does* take a little practice to master using a mouse or trackpoint for laying down pads and tracks, but this soon becomes second nature for most users.

A typical PC Designer screen is shown in **Photo A**. The program's *menu bar* provides access to a number of set-up options and general program functions. However, the real key to the program's utility is the on-screen *button bar* located just below the menu bar. This allows you to perform several short-cut operations. For example, you can select from four preset track widths and four preset pad sizes with a click of the mouse. The size specifications for each track and pad selection are either user-defined via a menu, or set to a program default (your choice). Footprints for several common IC-DIPs (Dual In Packages)—plus a menu-configured custom IC package—are also accessible via the button bar.

For additional selections, you can use the button bar to turn on a menu containing a number of predrawn footprints for transistors with various package styles, edge connectors, common SMT parts, and even a "bullet" to mark board corners or drilled mounting holes. (If a footprint isn't provided off menu, it can usually be constructed using tracks.) The button bar also turns on the program's *rubber banding* function, which allows you to mark several

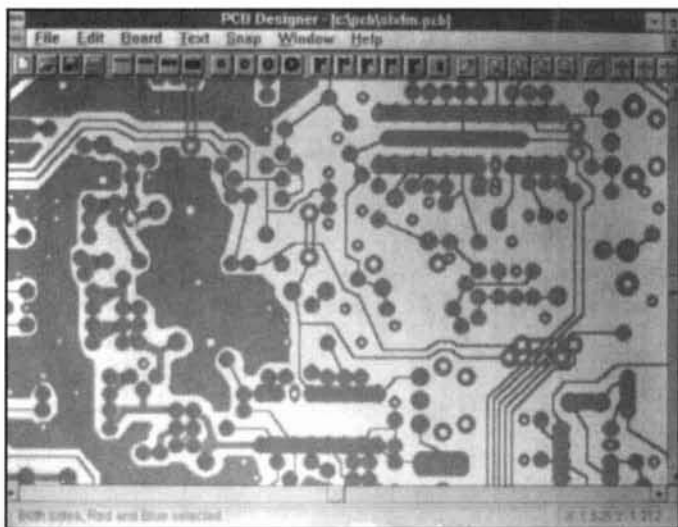


Photo A. A typical PC Designer screen.

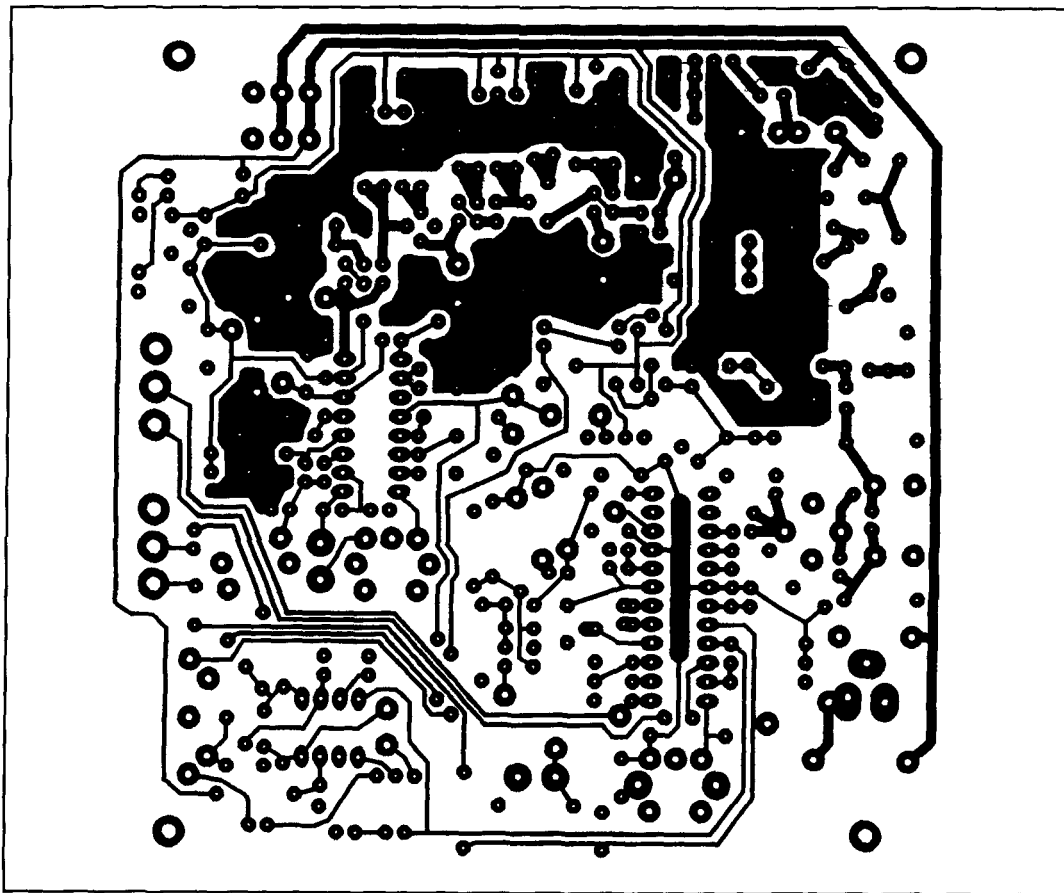


Figure 1. Sample layout.

components at one time to either move or erase as a block.

In one sense, building a pc board layout with PC Designer is like building a layout the old-fashioned way—with donut-pads and tapes on grid paper or acetate. You don't have to wade through parts libraries. All of the commonly used circuit board elements are close at hand (on the button bar), and you can lay down pads individually—to whatever spacing standard you prefer to use. At the same time, PC Designer is far superior to the old method because the computer eliminates all of the guesswork, cutting, and mess associated with adhesive-backed pads and tape...not to mention the expense! On-screen grid markers and several snap-to-grid resolutions make pad placement and track spacing easy and accurate. The program also provides a running on-screen display of your cursor position relative to the last pad placement. If you want your next pad positioned 0.8 inch up and 0.1 inch over from the last entry, you can move the cursor to the exact spot and lay it down by the numbers. PC Designer allows you to work at the x1, x2, or x4 magnification level, so you can select the appropriate resolution for the type of work you are doing—or zoom in on

a targeted area for close inspection. Other helpful features include automatic track bending and the ability to add text. The best feature of all, however, has to do with board revisions and layout mistakes. If anything goes down incorrectly, it is very, very easy to fix!

Doing RF layouts

I've found PC Designer especially helpful for RF layouts. As a rule, I set up a couple of track sizes that are convenient for pad interconnections, and then I select two wider track widths for building land areas (see **Figure 1**). Because track length and width are easy to control, it's also possible to lay out accurate striplines and printed inductors. For two-sided work, solder-side features are displayed in red and component-side features in blue. You can view both sides of the board in color, simultaneously. However, when working, the inactive side becomes underlaid in a gray halftone. For two-sided RF-style boards, I work up the component side as a negative, assigning white area as foil and blue as relief. This saves the work of building extensive land areas—and makes posi-

tioning relief areas over solder-side pads very easy. The solder side is then reversed to a matching negative during printout.

Printing out

PC Designer will work with virtually any graphics-compatible printer, although ink jet or laser printers generate better camera-ready art. Be sure to use high-quality paper made for the type of printer you're using. My HP DeskJet™ delivers very sharp camera-ready results usable for even finely detailed surface-mount layouts. A laser printer is probably most desirable for printing directly onto a transparency. Several menu-selected printout options are available, including masks and proofs, reverses and negatives, and x1 or x2 sizing. Drawings are in a Windows Metafile format that may be exported to other documents or moved into a paint program for visual enhancement.

Limitations

Although you can accomplish a great deal with this program, it would be unrealistic to equate PC Designer with a full-blown CAD package. For example, while a two-sided prototype pc board may require only two screens for etching, a manufactured version of the same board would require several more, including solder masks, a drilling template, and a parts-

placement screen. Add in the standardization requirements for automated production, a need for coordinated schematic, artwork, and parts-list documentation, plus interface with a computerized inventory control system, and the case for a full-grown CAD package (along with the services of a specialist to run it) becomes pretty strong. But, for many of us who simply like to "build stuff," those concerns aren't really germane. If your only goal is to make a good-looking circuit board, and you don't have time to learn a new profession to do it, PC Designer might prove an excellent choice.

Purchasing information

PC Designer is available from Niche Software (UK), 12 Short Hedges Close, Northleach Cheltenham, GL54 3PD. The price per copy is 49 pounds, payable via Access, MasterCard, Visa, Visa Delta, and AMEX. As a special offer to *Communications Quarterly* readers, Niche is offering a special price of 39 pounds for Internet-based orders *only* until December 31, 1996. All special orders will be delivered via the Net. Interested parties should order the program from: <SpecialOffer@Niche.demon.co.uk>. You may also order via FAX at +44 1432 357 113, or call Niche at +44 1432 355 414. Niche also has a new parts compiler program and user-friendly schematic program in the works. ■

PRODUCT INFORMATION

New RF Signal Generators from Tektronix

Tektronix, Inc. has announced the SME06 and SMT06 RF signal generators. Both are considered to be cost-effective stimulus solutions for measurements in the 6 GHz range. The SMT06 is a general-purpose model and the SME06 is designed to produce a full slate of digital modulation signals. The SME06 is designed to meet the evolving needs of the new class of 5.7 GHz digital communication equipment.

The SME06 and SMT06 are the latest members of the Rohde & Schwarz (Germany) family of RF and microwave signal generators. They are marketed and supported in the United States and Canada by Tektronix under an alliance formed with Rohde & Schwarz in 1993. The instruments are part of a full line of digital wireless test products offered by Tektronix.

Both models serve the requirements of wireless communications component and system designers and manufacturers who must test products ranging from discrete amplifiers to

board-level assemblies to base stations. The SME06, when equipped with the DM Coder option, provides a host of digital modulation schemes including GSM, DCS 1800, PCS 1900, DECT, PDC, FLEX™, and more. It supports 25 prevailing modulation standards and it offers all the standard analog modulation schemes.

The SMT06 is a general-purpose 6.0 GHz RF signal generator aimed at the needs of wireless communications components and systems, radar, electronic warfare, and electromagnetic compatibility testing. It is equipped to cover the entire range of analog receiver measurements, with AM, broadband FM, and phase modulation, plus options that include pulse modulation, a function generator, and a low frequency generator. The SMT06 is suitable for both benchtop engineering use and manufacturing test applications.

For more information, call 1-800-426-2200 (when prompted, press 3 and ask for code number 512); or visit the Tektronix web site at <http://tek.com.Measurement>.

AN IF AND 80-dB LOG AMP FOR SPECTRUM ANALYZERS

*Modernize your older commercial or
homebrew unit*

Serious "basement RF engineers" often attend hamfests looking for the ultimate bargain spectrum analyzer. My luck at these gatherings hasn't been as good. I know excellent analyzers, like those based on the HP 141T and Tek 7000 series mainframe units, are becoming affordable. However, my upstairs workshop is quite small. My ham station, computer work area, and a sprinkling of antique radios fill the space. There just isn't room for one of those big old dinosaurs!

Several years ago, I reviewed the A&A Engineering spectrum analyzer for *Ham Radio* magazine.¹ This low-cost kit was based on a *QST* article by Al Helfrick, K2BLA.² It used a Jerrold CATV module, and the remaining RF sections were built around a single Motorola MC3356 IC. Unfortunately, the instrument's dynamic range was restricted to 50 dB at best—the limits of the RSSI output of the MC3356. Even so, it was a well-balanced match between the Jerrold module and the MC3356 chip. Still, the 50-dB dynamic range remained a serious drawback for most RF work. Once input signals exceeded this limit, the analyzer overloaded—resulting in serious distortion of the displayed signals. There was no headroom!



Photo A. The modified A&A Engineering spectrum analyzer and companion Tek 604 display make a dynamite combination!

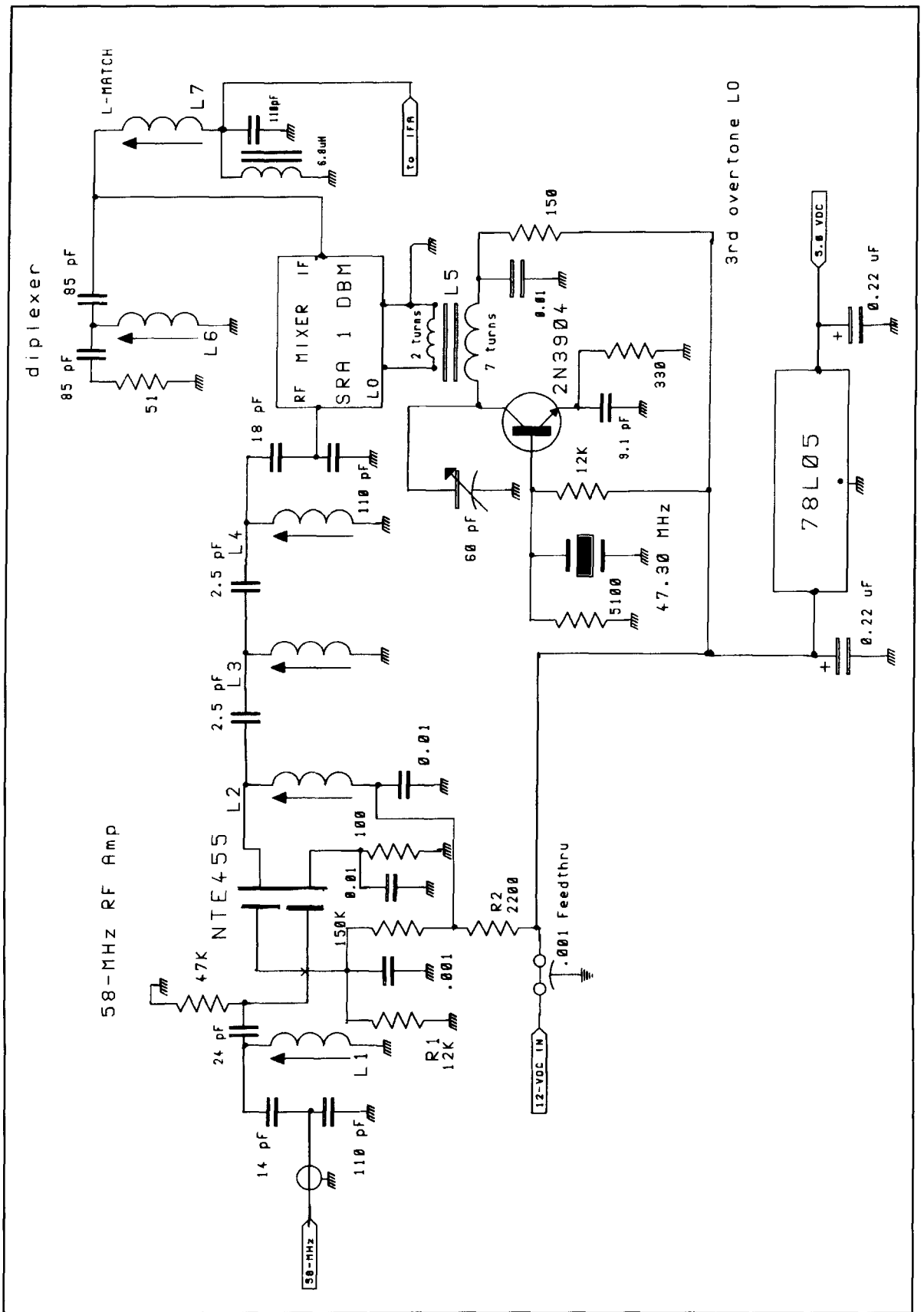


Figure 1A. The 58-MHz stage, 47.3 LO, and the MiniCircuits SRA 1-DBM stage. Note that 0.001 feedthrough capacitors are on the wall of the Hammond enclosure.

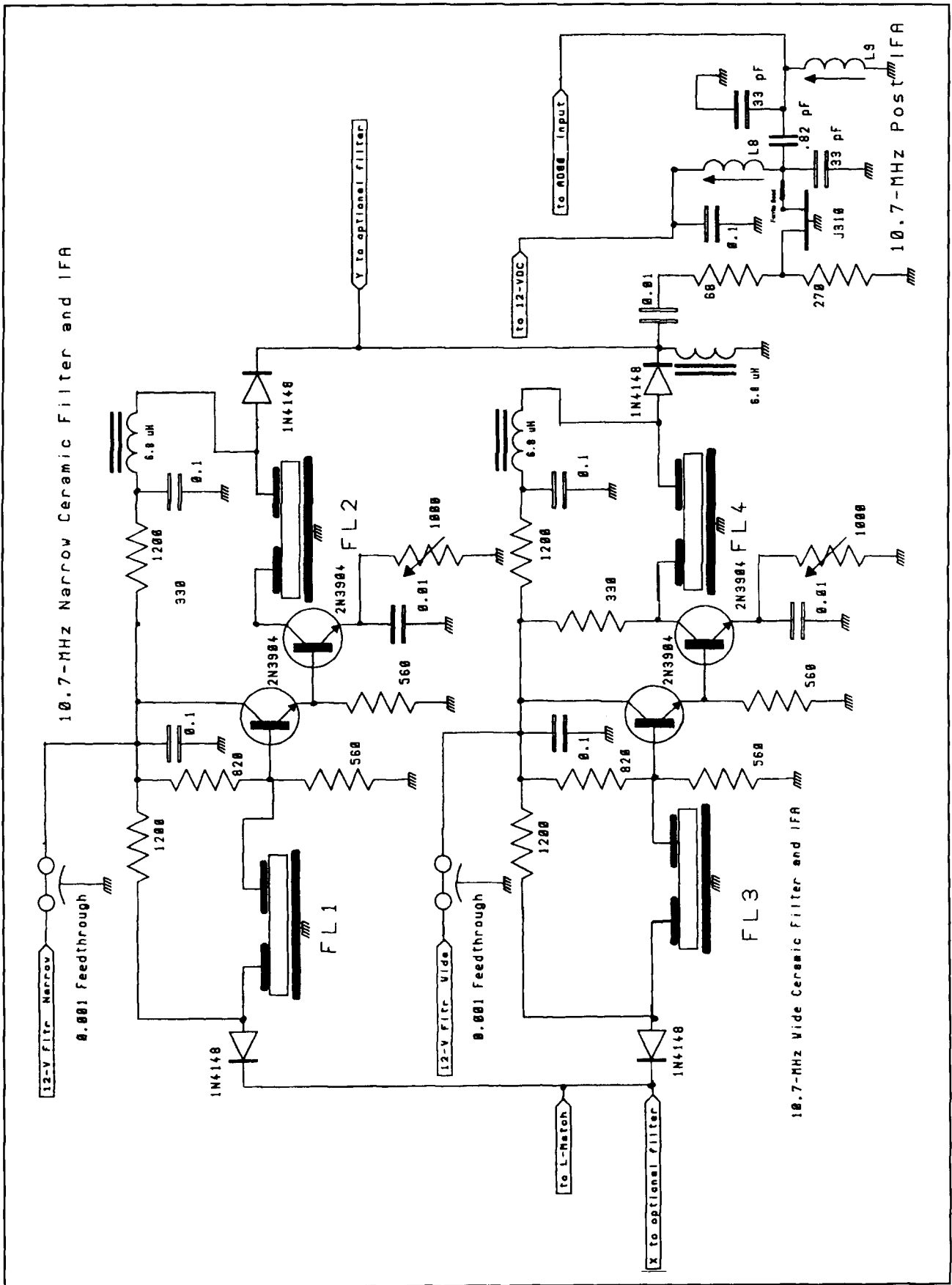


Figure 1B. Wide and narrow IF amplifier stages, followed by a J310 IFA stage.

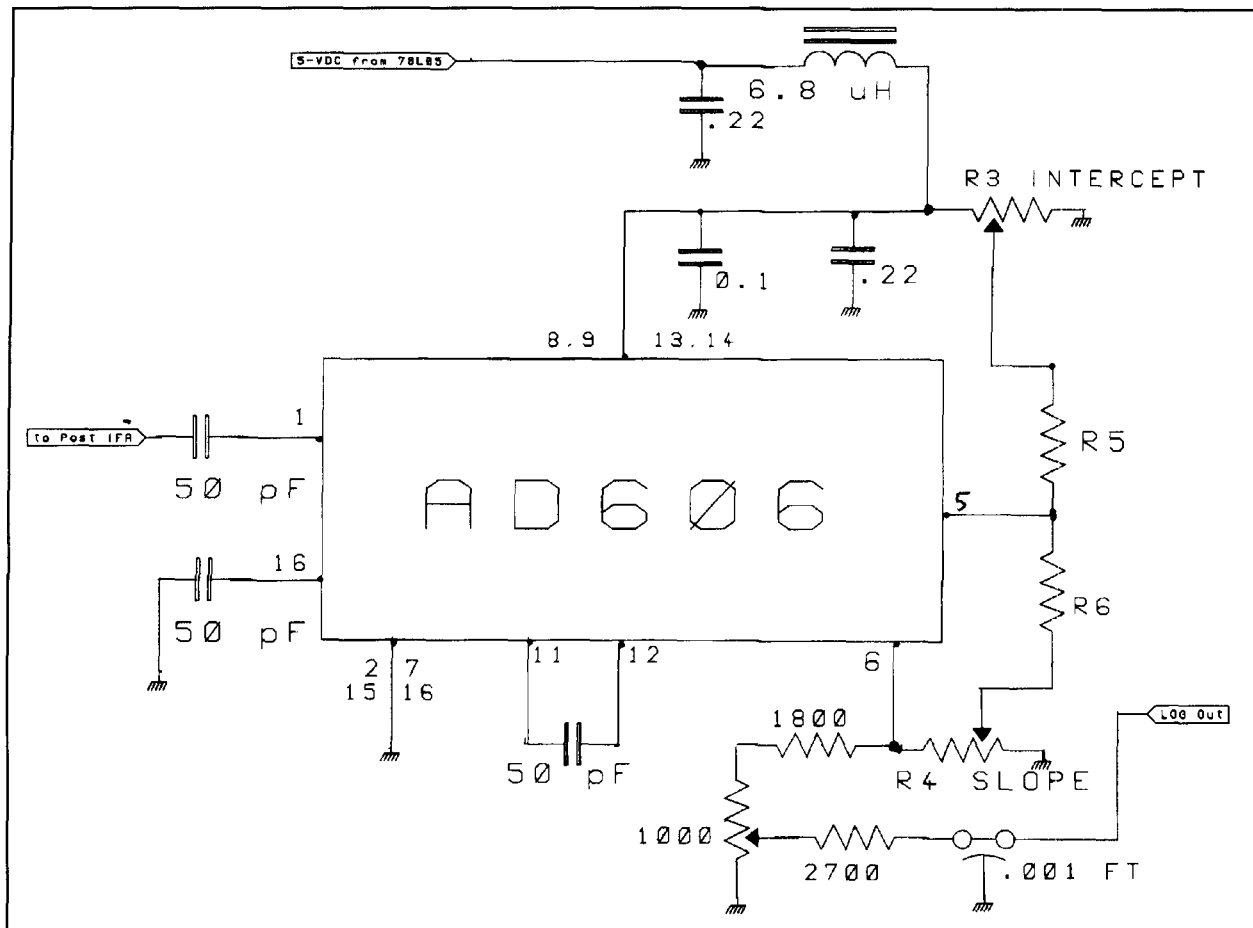


Figure 1C. The AD606 log amplifier section. Intercept and slope pots aren't used in this application, but are provided for on the FAR Circuits board.

Since 1985, newer FM IF chips with better RSSI outputs have become available. But rather than reinvent the wheel and use one of those devices, I decided to start from scratch and chose a newer chip designed specifically for log amp service: the Analog Devices AD606.

I designed and built a high-dynamic range IF system and log amp that delivers at least 70 dB (typically 75 to 80 dB) of calibrated dynamic range on screen. My goal was to build a general-purpose spectrum analyzer. I'm mostly interested in searching for transmitters involved in IMD equations, measuring transmitter harmonics, and looking for spurious transmitter emissions. This unit isn't intended for single-sideband signal analysis or other demanding narrow bandwidth signal work.

I had intended to design a new analyzer from the ground up. My first step was to devise a simple IF section and a good log amplifier—the heart of such a unit. Once that was done, I used my A&A Engineering spectrum analyzer as a test bed to prove my design. The results were so encouraging that I'm not considering any further work on a newer analyzer at this time.

If you're interested, I've provided details on

how to interface the new IF and log amp to the A&A Engineering spectrum analyzer. I've also included modifications to the Jerrold CATV module that provide greater dynamic range and eliminate internally generated spurs.

The IF system and log amplifier

Figures 1A through 1D show the IF and log amp schematic. Photo A shows an assembled IF and log amp pc board. The drilled, plated, and silkscreened pc board is available from FAR Circuits. Pricing and ordering information is given in Table 1.

The silkscreen parts placement is provided in Figure 2. Photo B shows an assembled FAR Circuits pc board.

58-MHz RF stage

The RF input to the board is designed for 58 MHz and 50 or 75 ohms—making this project compatible with most CATV or TV tuner-based analyzer designs.

Several CoilCraft coil kit assortments³ great-

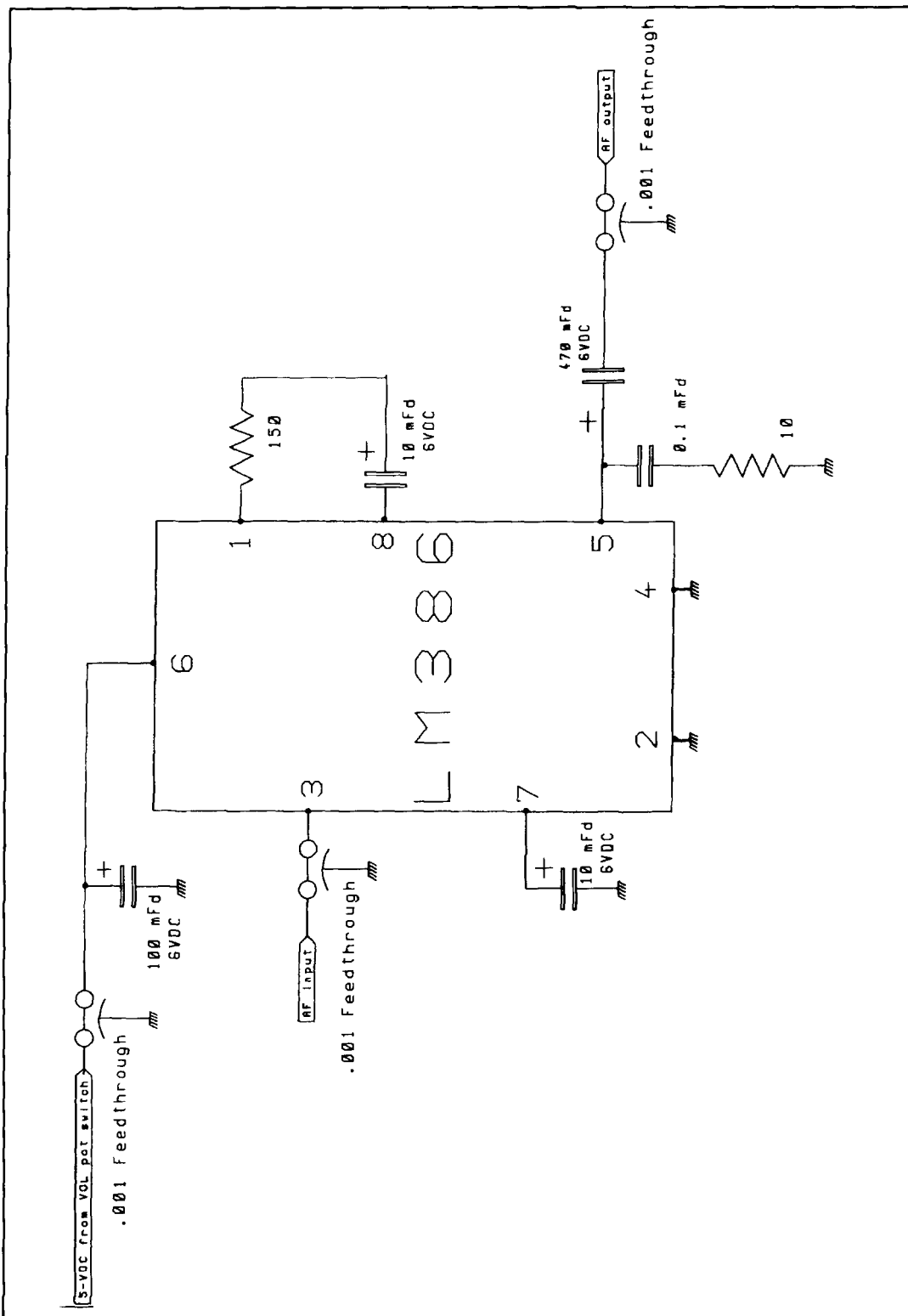


Figure 1D. W6UCM's audio amplifier stage allows demodulation of FM or AM signals.

ly simplified the breadboard design stages of this project. You can obtain RF inputs other than 58-MHz, and out of the tuning range of the coils used, with different value coils and padding capacitors. Another trick is to use

either high or low side LO injection. This allows for a greater range of RF input frequencies, while still using third-overtone crystals.

Because some CATV downconverter modules are designed for a Channel 3 TV IF at 61.5

Coils	
L1,L2,L3,L4	CoilCraft 142 10 J 08S 0.32 to 0.42 μ H, shielded
L5	T-37-2 toroid primary: 7 turns no. 26 AWG secondary: 2 turns no. 26 AWG
L6	Coilcraft 150 05 J 08S 0.09 to 1.23 μ H, shielded
L7	Coilcraft SLOT 10 3-03 1.5 to 2.0 μ H, shielded
L8, L9	Coilcraft SLOT 10 3-06 1.5 to 6.0 μ H, shielded
DBM	MiniCircuits SRA-1 7-dBm LO

*An etched, drilled, and plated circuit board for this project is available from FAR Circuits, 18N640 Field Court, Dundee, Illinois 60118. Phone: (708) 426-2431 after 6 p.m. CST. The price per board is \$6. Shipping and handling for 1 to 2 boards is \$1.50.

Table 1. Parts list for FAR circuits board*

MHz, the tuning range of the 58-MHz RF stages should accommodate this IF with small changes in the resonating capacitors. (The IF for Channel 2 is 55.5 MHz; well within the tuning range of the RFA stages with small capacitance changes, and of the LO tank circuit.)

You may prefer to use IFs in the 40- or 70-MHz range. This lets you use economical off-the-shelf SAW filters for additional filtering before the final mixer stage. Because the AD606 is rated to 50 MHz, it can be used as part of an inline IF section operating directly on a Channel 2 or 3 IF, or a 45-MHz TV video IF, without any conversion schemes.

The parts list in **Table 1** provides the CoilCraft part number and the inductance ranges needed for a 58-MHz IF. The capacitor values used for coupling and tuning the 58-MHz stages are critical. The table also gives my coil values.

First RF stage

The first RF stage uses a low-noise dual-gate UHF MOSFET—setting the noise figure for the IF, overcoming the losses of the passive DBM stage following it. There are four lightly coupled 58-MHz stages. These provide adequate blowby protection and prevent any undesired off-frequency products produced in the Jerrold (or other) analyzer front end from reaching the mixer input. They, and the other

tuned circuits at 10.7 MHz, also provide selectivity to reject strong signals that may fall on unwanted spurious responses occurring in the ceramic IF filter stop-bands.

Pre-IF 58-MHz bandpass filter

The Jerrold 450 CATV module generated some spurious responses on either side of the displayed signal when strong signals exceeded the analyzer's dynamic range. I added a three-section 58-MHz preselector to eliminate the problem, locating it inside the Jerrold CATV module used in the Helfrick/A&A Engineering spectrum analyzer. It may also be mounted externally in a small shielded enclosure.

Stage gain

While the 58-MHz stage gain may appear excessive for use ahead of a mixer, I noticed no overload problems. Also, this RF amplifier precedes a passive mixer stage in the Jerrold, which probably has several dB of conversion loss, so some gain is needed here. You may increase gain by reducing the values of the 2.5-pF coupling capacitors used between the tuned output stages. Note that this will result in instability (regenerative) problems if you use a values that's too low.

I chose parts values to reduce the stage gain from its maximum setting, which allowed the analyzer to "recover" 3 or 4 dB of signal range over the original breadboard design. Excessive stage gain caused excessive "grass" levels on the display baseline, and raised the baseline by a few dB (noise floor). More gain may be obtained by either changing the gate 2 bias resistor (R1) from 12 to 27 k, or by reducing the drain resistor (R2) from 2.2 to 1 k.

Optional IF gain control

I decided to include a variable IF gain control. To do so, I removed resistor R1 and, in its place, ran a 10-k resistor from the gate 2 side to a 0.001-pF feedthrough on the Hammond enclosure. I mounted a 25-k pot on the front panel. This let the gate 2 bias resistor vary from 10 to 37 k, providing 15-dB of control over the RF stage gain.

Helfrick's IF attenuator is actually a calibrated 10-turn pot that controls the Y axis positioning. One-dB indications allow for accurate comparative signal level readings, placing a lot of faith in the accuracy of the log output of the MC3356! This control is handy for positioning the scope's baseline or the 0-dB reference graticule when switching between IF filters, or following adjustment of the IF gain control.

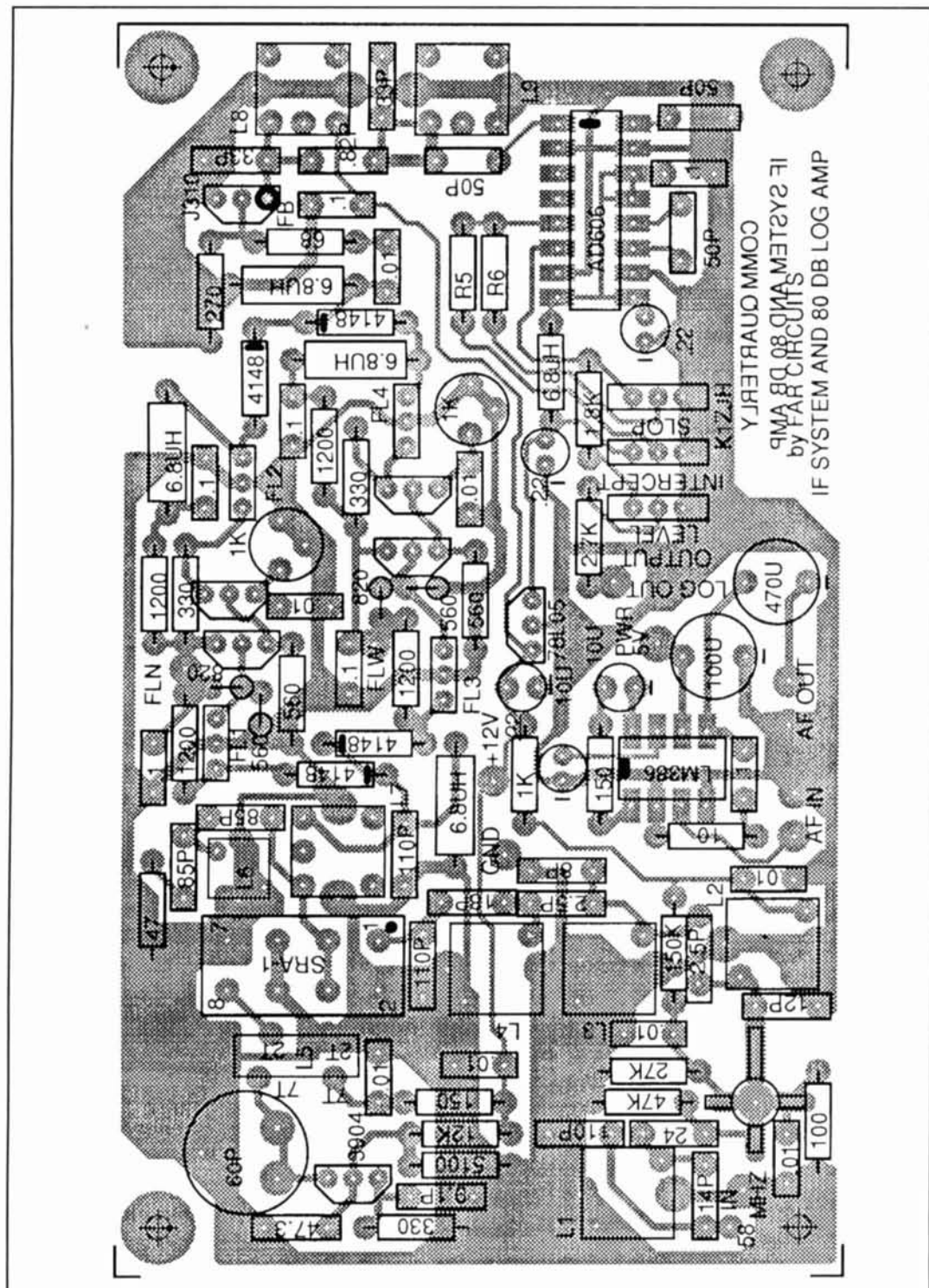


Figure 2. Parts side "silk screen" view of FAR Circuits pc board.

Note the optional -40 dBm reference signal level modification.

First mixer and LO

The first mixer and LO contain a passive diode double-balanced mixer (DBM). You can

use almost any +7-dBm LO DBM with a footprint and characteristics similar to the MiniCircuits Labs SRA-1. Mixer loss is about 6 dB. There is capacitive matching between the output of the 58-MHz stage and the 50-ohm RF input port on the DBM.

Because of the 10.7-MHz IF, I used a 47.3-MHz LO signal for the 58-MHz RF input.

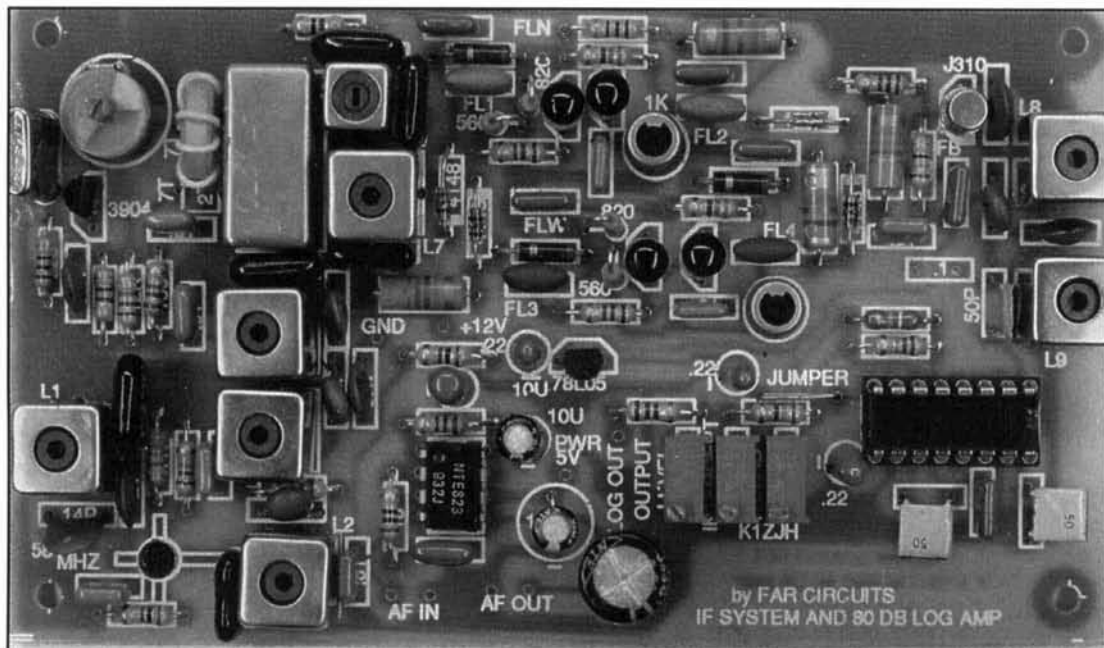


Photo B. FAR Circuits pc board assembled and ready for installation. This picture is of a slightly earlier version. Photo by Frank Maggiore, Maggiore Electronic Labs.

The toroid and trimmer capacitor provide a wide oscillator frequency range if another RF frequency is desired. I tried slug-tuned coils, but their tuning ranges were too restrictive.

The crystal is a high-quality third-overtone type. I used a commercial grade crystal, "cut" to Motorola KXN6207 (for the MT-500 Motorola portable radio receiver) specs. The 2N3904 oscillator provides the desired +7-dBm drive to the mixer (measured on a terminated Boonton 92 millivoltmeter). If more LO drive were available, I would have considered a fixed 3-dB pad at the mixer LO port for termination.

LO tuning

Tune the oscillator by finding the point where it breaks into oscillation, when starting at a maximum capacitance setting. The ideal point lies just slightly beyond this point. An RF probe held in the field of the toroid will indicate a maximum reading here. Be sure the oscillator restarts reliably at this setting when power is removed and reapplied.

First IF

As I mentioned, the IF is at 10.7 MHz. The mixer's IF output is 50 ohms—terminated at the image and LO frequencies via a simple high-pass filter, composed of coil L6, two 85-pF capacitors, and a termination resistor (47 or 51 ohms, 1/4 watt). An L-match network (coil L7 and a 100-pF capacitor) transforms the 50-ohm mixer output to 330 ohms—the imped-

ance of the ceramic IF filters. These filters have considerable loss, up to several dB depending on the filter bandwidth. The first IF filter loss adds directly to the average 6 or 7 dB conversion DBM loss. Thus, filter losses play a large part in determining the overall display range. I obtained better gain distribution when I tried a gain "make-up" IF stage between the mixer and first filter. This also helped improve the mixer stage noise figure. (It was omitted in the final design for simplicity.)

This and other design tradeoffs were a direct result of my desire to power this board directly from the A&A spectrum analyzer power supply.

Because the A&A supply has little reserve power, I deleted any unnecessary active stages. The A&A power supply uses a 78L12 12-volt regulator with a limited 100-mA output rating. The transformers also run near their maximum continuous ratings.

IF filters

The A&A analyzer has two IF selectivity positions. The narrow 15-kHz BW uses a two-pole crystal filter; the wider 330-kHz BW uses a ceramic filter. A single stage of IF filtering was used for the 50-dB range of the original instrument. I found using a single IF filter resulted in grossly inadequate stop-band suppression and off-resonance spurious responses when the dynamic range was increased much over 50-dB!

It would be easy to incorporate several selectivity positions, considering the variety of low-cost ceramic filters. **Table 2** lists a number

Bw Freq. @3db	Ins. Loss (Max.)	Spurious Response (9-12 MHz)	Impedance
280KHz	6dB	30dB	330Ω
230 KHz	6dB	35dB	330Ω
180KHz	7dB	40dB	330Ω
150KHz	10dB	40dB	330Ω
110KHz	10dB	30dB	330Ω

Table 2.

of TOKO ceramic 10.7-MHz filter styles available from DigiKey. Table 3 highlights the characteristics of the harmonic-mode Murata ceramic filters.

These have bandwidths that almost rival two-pole crystal filter performance. The trade-off for sharper bandwidths is greater insertion losses. The Murata harmonic mode ceramic filters are covered in Reference 4.

I decided that two selectivity positions using low-cost ceramic filters would be adequate for most applications. The crystal filters required additional matching networks, and I had problems achieving the desired passband responses when I tried them in earlier prototypes. In this design, two IF filters are used for each selectivity selection, and each selectivity position has its own dedicated two-stage RC coupled IF amplifier with an input and output ceramic filter. This is the heart of the 10.7-MHz IF amplifier stage.

Diode switching selects the IF amplifier and filters. Common 1N4148 or 1N914 silicon high-speed switching diodes performed as well as PIN diodes, and I used them in the final design. Low-speed power diodes, like the 1N4001, would probably work, but I suspect they would require much higher forward biasing currents. The RC-coupled IF amplifier stages are untuned and provide 330-ohm input and output terminations for the ceramic filters. Using the filter bandwidths indicated, the IF has a swept response that's very symmetrical and clean, with a single response peak, over the 80-dB plus scope display.

The IF stage transistors in my prototypes were CS5088s. However, the 2N3904s or NTE 123AP transistors are good substitutes.

Wide IF Filter: 180-kHz

You'll need a wide BW filter to use the A&A analyzer's 450-MHz scan setting. I installed a

pair of 180-kHz BW TOKO ceramic filters here. When using video filtering with either the 20- or 50-MHz-per-division scanwidth settings, wider values (330 kHz) are preferable to avoid attenuating the displayed signals. Otherwise, you must use a storage scope and a slow sweep rate. The narrow width "blips" produced by sharper filters are also much harder to see.

Narrow IF filter—30-kHz

The narrow IF bandwidth was another trade-off in filter choices. I chose the narrow BW Murata 10.7 volt for the input and output IF filters. If Murata filters aren't available, try using two of the narrow 110-kHz BW TOKO filters. Two narrow Murata 10.7-volt filters worked well and provided a nice sharp response, but their combined insertion losses were a bit excessive. While the Murata filters aren't quite as good as crystal two-pole filters, they are adequate for most needs.

Optional broadband filter—500-kHz

Figure 3 shows a small off-board LC filter I built to provide a bandwidth twice that of the 180-kHz TOKO types—somewhere between 300 and 500-kHz BW. Its swept waveform is more triangular than the sharper-skirted ceramic filters, making it better suited for use with wider scanwidths and video filtering. (This circuit doesn't fit on the FAR Circuits pc board.)

The broadband filter was an afterthought. Repeatability isn't guaranteed. It's best to add this circuit after you've enclosed the FAR Circuits board and have it debugged and working as intended.

The circuit is built around three 7-mm 10.7-MHz IF transformers (violet color code)

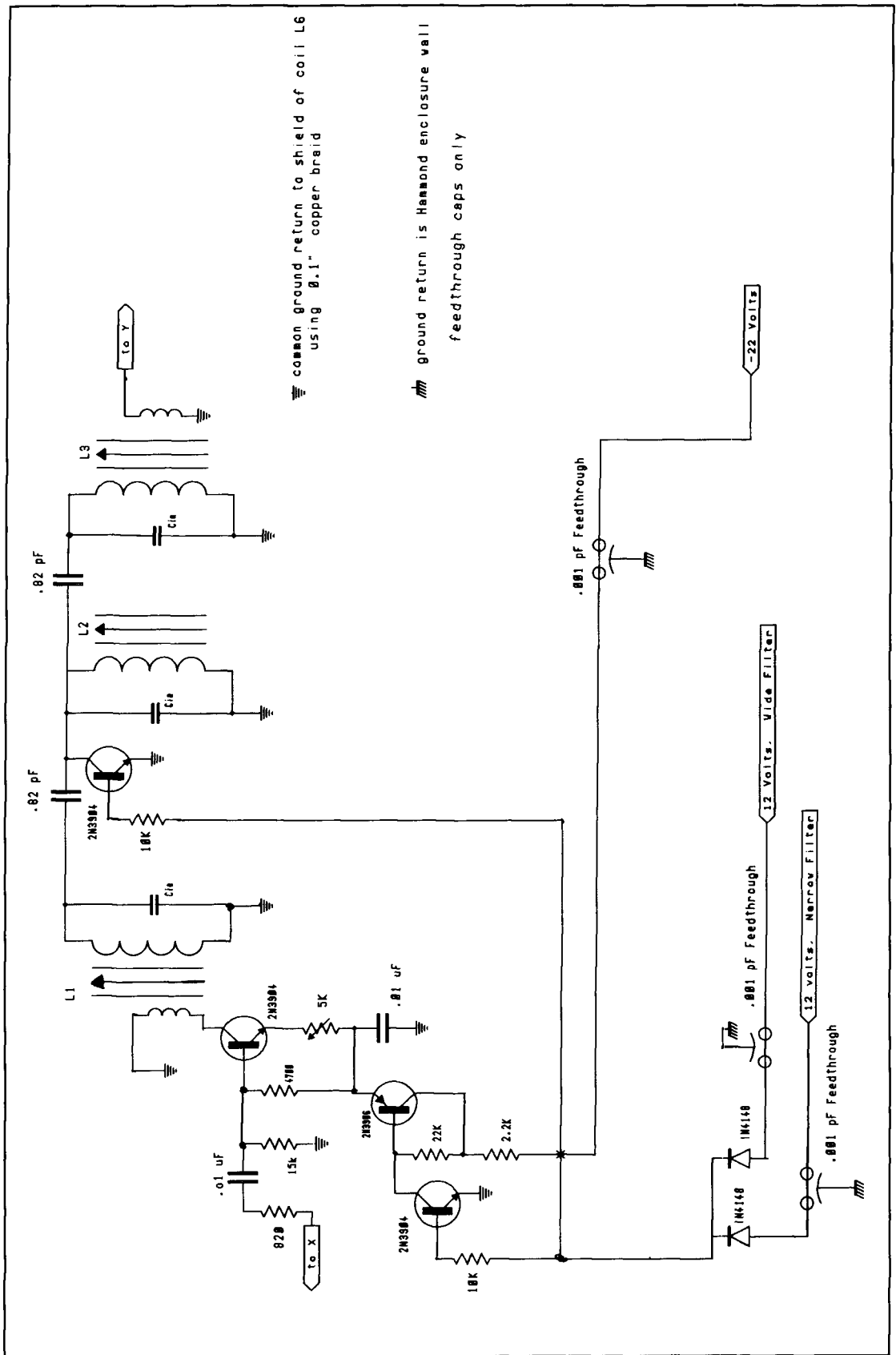
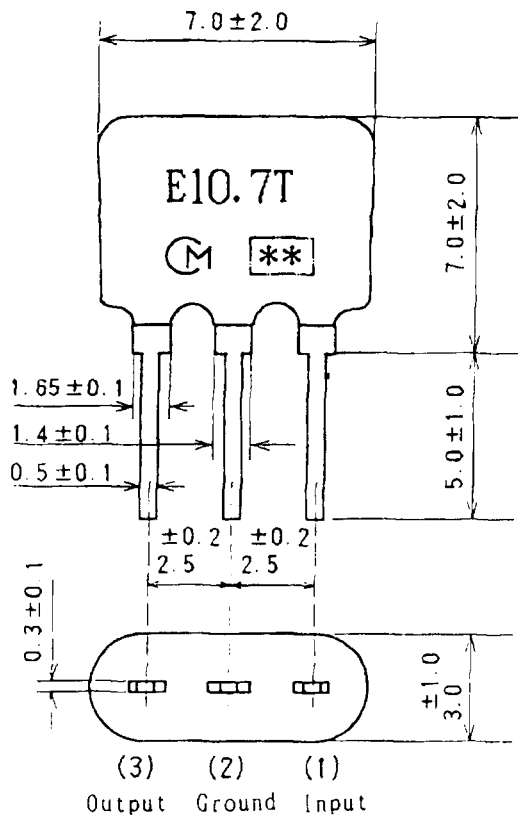


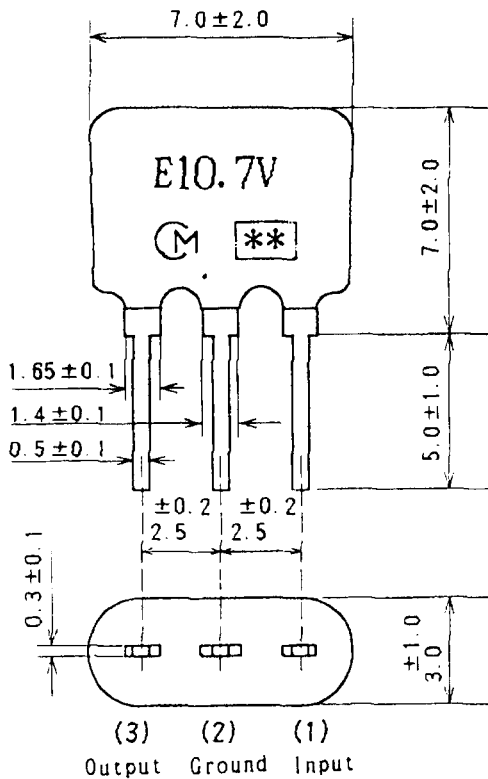
Figure 3. Optional "broad" selectivity IF stage is built "cordwood" fashion off the main FAR Circuits board. Note the only short length of 0.1-inch RF braid back to the FAR Circuits board. The 0.001 feedthroughs are located on the Hammond enclosure wall.



Specification of Ceramic Filter

Type: SFE10.7MT

- | | | |
|--|---|---|
| 1. Nominal Center Frequency (f_n) | : | 10.700 MHz |
| 2. 3 dB Bandwidth | : | $f_n \pm 25$ kHz min.
Total 60 kHz min. |
| 3. Selectivity at $f_n \pm 100$ kHz | : | 20 dB min. |
| 4. Insertion Loss | : | 6.5 ± 2.5 dB |
| 5. Spurious Response (within 9 MHz to 12 MHz) | : | 30 dB min. |
| 6. Ripple (within 3 dB Bandwidth) | : | 1.0 dB max. |
| 7. Temperature Coefficient of Center Frequency | : | ± 20 ppm/ $^{\circ}$ C max. |
| | | Temperature Range: -20° C to $+80^{\circ}$ C |
| 8. Input and Output Impedance | : | 330 ohms |
| 9. Withstanding Voltage | : | 50 Vdc max. 1 minute max. |



Specification of Ceramic Filter

Type: SFE10.7MV5

- | | | |
|--|---|---|
| 1. Nominal Center Frequency (f_n) | : | 10.710 MHz |
| 2. 3 dB Bandwidth | : | $f_n \pm 13$ kHz min. |
| 3. 20 dB Bandwidth | : | 135 kHz max. |
| 4. Insertion Loss | : | 6.0 ± 2.0 dB |
| 5. Spurious Response (within 9 MHz to 12 MHz) | : | 35 dB min. |
| 6. Ripple (within 3 dB Bandwidth) | : | 1.0 dB max. |
| 7. Temperature Coefficient of Center Frequency | : | ± 20 ppm/ $^{\circ}$ C max. |
| | | Temperature Range: -20° C to $+80^{\circ}$ C |
| 8. Input and Output Impedance | : | 330 ohms |
| 9. Withstanding Voltage | : | 50 Vdc max. 1 minute max. |

Table 3.



Photo C. A&A engineering front panel before modifications. Photo courtesy A&A Engineering.

whose cans are seam-soldered together. The components are built onto the structure using point-to-point wiring. The coil shield cans act as ground returns. This filter assembly's RF and DC ground return is connected to coil can L6 on the IF board using a short length of 0.1-inch desoldering braid. Do not connect grounds to the Hammond enclosure. The assembly should be mounted next to, but not touching, the Hammond enclosure sidewall using insulating silicone adhesive.

The 0.82-pF capacitors provide light coupling between the coils. Unlike the other IF amps, this stage runs off the -22 volt power supply in the A&A Engineering analyzer. An



Photo D. A&A front panel after modifications. Note addition of two SMA jacks above the RF IN BNC fitting on the left. The bottom SMA supplies a calibrated -40-dBm 47.3-MHz reference signal. The upper SMA fitting is for a future tracking generator project. It supplies the divide-by-256 output from the Jerrold prescaler. To the right of the display bezel is the new IF gain control. To the right of the SCAN WIDTH control is the volume control and a jack for using an external speaker or headphones.

emitter gain pot lets you set the gain to match that of the other IF amps. This stage's input and output impedances are relatively high, so they can be directly connected to the 6.8- μ H chokes used for the DC return paths of the switching diodes used for the two onboard IF amps.

Filter tuning is performed so the three coils peak at the same point as the wide ceramic filters. Note that mistuning the last IF transformer will distort the ceramic filter responses. This coil must be set to the same center frequency as the ceramic filters to reflect a high-impedance termination at resonance!

The amplifier is disabled by a 2N3904 that acts as a shunt across the high-impedance winding of the center IF bandpass filter. The 12-volt feed to either the narrow or wide filter is diode-or'ed to the base of the 2N3904 when either of those stages is selected. As a result, the transistor is driven into heavy conduction, effectively killing the amplifier output. This alone doesn't provide enough isolation, so a 2N3904 and 2N3906 are used to remove the -22 volt power to the broadband IF stage whenever the wide or narrow ceramic filter IF amps are selected.

To allow selection of the broad filter position, I replaced the original double-throw (on-on) IF filter selector switch on the A&A front panel with one that has a center detent (on-off-on) position. The broad filter is activated in the switch center position.

Gain balancing

In his *QST* design, Helfrick provided compensation for the increased losses when he chose the higher selectivity filter position. I included a 1-k trimmer resistor in the emitter return of each IF stage to allow for gain control. In theory, you set each pot for best gain (as indicated by maximum upward deflection of a signal in the analyzer display.) The stage with the highest gain (i.e., lower loss filters) can then be adjusted to reduce its level to that of the other IF stage using more lossy filters. This keeps the analyzer readings the same when different filters are selected. Gain reduction must be implemented by increasing the trimmer resistance setting for best bias stability.

Post IF amplifier

A grounded-gate J-FET amplifier follows the selected IF stage. Its input impedance is optimized to yield best swept results (symmetry, single response peak) for the 330-ohm impedance of the ceramic filters.

I tried several different J-FETs, all with identical results. (Although I specify a J310, a

Items available from A&A Engineering (limited quantities)

450-RFM 450-MHz RF module with modification information and part	\$75
450-RFM RF module without modification information or parts	\$55
119-PCB power supply board	\$20
119-KIT board and parts	\$70
117-PCB spectrum analyzer main circuit board	\$30

Display boards are no longer available. Jerrold modules may come with either Channel 2 or Channel 3 output, depending on what's available.

Other small components may be available. Call or write: A&A Engineering, 2521 West LaPalma, Unit K, Anaheim, California 92801. Phone: (714) 952-2114; fax: (714) 952-3280.

Table 4.

2N4416 should also work). Besides providing a small amount of gain, this stage also drives the two lightly coupled high-impedance 10.7-MHz tuned stages preceding the log amplifier input. A small ferrite bead is placed over the drain lead to discourage VHF parasitics.⁵

The AD606 log amplifier

At the core of this project is Analog Device's AD606 log amplifier IC, discussed in "Quarterly Devices".⁶ Early log-amp designs involved summing the outputs of several limited-range cascaded log amps constructed with discrete components. This required considerable power and pc board real estate.⁷

Because the AD606 is a CMOS device, and an expensive one at that (around \$30 in small quantities), use care when handling. It's the only socketed component on the board and shouldn't be inserted until after all wiring and initial testing is completed. I recommend a high-quality machined-pin low-profile socket. Note that an on-board 78L05 regulator supplies the 5 volts for the AD606; verify that no more than 5 volts is present at the chip socket before inserting the AD606. (I lost two to soldering iron leakage currents caused by an intermittent ground return in my soldering station's remote power supply—a rather expensive lesson in handling CMOS devices!)

With over 80 dB of dynamic range, circuit board layout is *critical*. Stray RF, especially from the 47.3-MHz LO, can easily reach the AD606 input, resulting in considerable loss of dynamic range. I got a good demonstration of this effect during the open "dead-bug" construction used in prototyping! Careless wire placement often resulted in an upward shift of the display baseline, with a corresponding loss of dynamic range. I was able to observe strong

foreign broadcast signals, falling within the bandpass of the 10.7-MHz IF, on evenings with good HF propagation. The two lightly coupled 10.7-MHz tuned stages, made up by L8 and L9 and associated capacitors, help keep stray signals from reaching the AD606. Very light coupling is adequate (note that I use a 0.82-pF capacitor for coupling between L8 and L9).

The Hammond 1590P cast-aluminum enclosure is an excellent size for the FAR Circuits board and will fit inside the A&A enclosure after some layout changes are made in that unit.

The pc board must be housed in a shielded enclosure with 0.001-pF RF feedthrough capacitors used for all power leads, audio signals, and the log output signal. An SMA or SMB bulkhead connector is needed for the RFA input signal. The AD606 will respond to signals from LF well into the VHF range.

Remember, shielding is important. As a test, set the LO so the crystal isn't oscillating and watch the scope display. (First, remove the RF connector feeding the RFA stage.) If the baseline drops more than a few dB, you may have a serious problem with stray RF radiation reaching the AD606 inputs. With over 80-dB dynamic range, the chip is a very sensitive "receiver"!

I strongly advise you use the FAR Circuits board. It represents about three redrafts to eliminate RF ground loop problems. The first board drove the scope baseline to the -50-dB mark, due to RF leakage from the 47.3-MHz oscillator reaching the AD606 log-amp chip. This shouldn't have surprised me: the log action begins with signals as low as -75 dBm (about 120 μ V) at the input pin of the AD606! The final board revision has only one ground foil return to the metal enclosure via the metal standoff near the 58-MHz RF amplifier stage.

The board must be mounted in a suitable RF-tight enclosure; the Hammond 1590P is ideal. Make sure no ground leads are connected

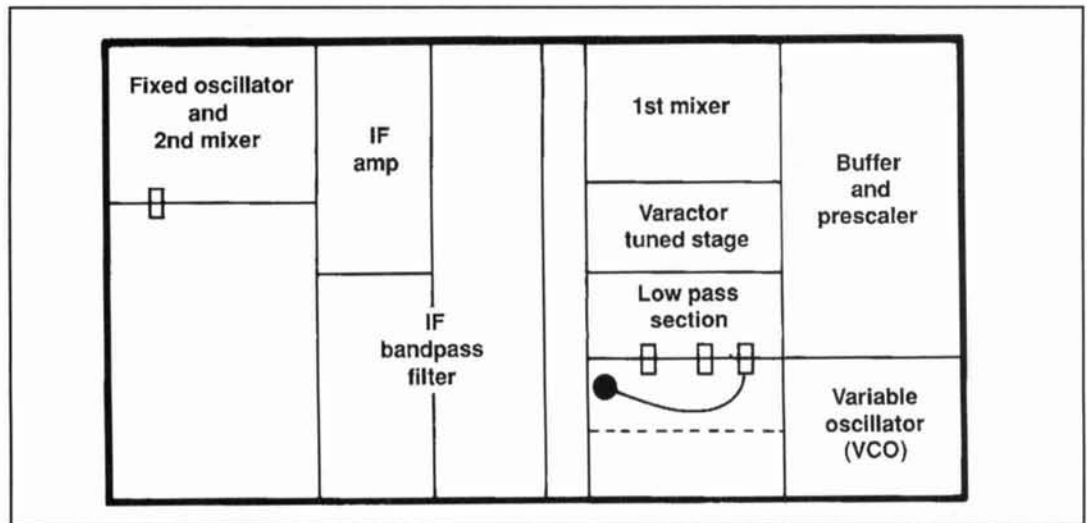


Figure 4. Internal layout of the Jerrold CATV modules. Optional 58-MHz bandpass filter may be mounted in the chamber adjacent to the "fixed oscillator and second mixer" compartment. All signals to and from the Jerrold module are done using SMA or SMB fittings.

to the board, except for the coax lead to the SMA connector for the 58-MHz RF input. All leads from the board, except for the coax, should be further decoupled using high permeability ferrite beads on the leads going to the feedthrough capacitors. I used five beads on each lead. The ferrites serve two functions. First, they help keep stray RF from entering and leaving the enclosure. Second, they break up a source of unwanted ground loops. If you

don't have beads, use 6.8- μ H molded chokes between the board terminations and feedthrough capacitors.

Before I installed the beads, simply touching a short piece of 0.1-inch braid between the shield can for either L8 or L9 and the adjacent Hammond wall caused the baseline to rise by 25 dB! After installing the beads, the baseline shift was only 10 dB. The 47.3-MHz crystal should also be grounded to the pc board. Most crystal manufacturers supply this pigtail upon request when you order.

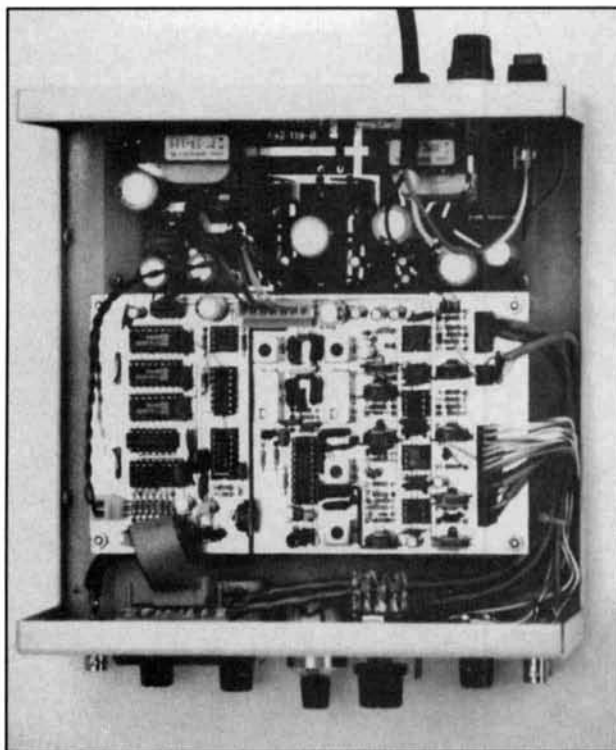


Photo E. A&A analyzer before modifications. Photo courtesy A&A Engineering.

Weird birdies

One strange birdie caught me by surprise. It appeared at repetitive 8-MHz tuning intervals across the tuning range, but only on the center of the screen. The IF filters had no effect on its width or duration, nor did the scanwidth control. Indeed, it appeared as a single "blip," center screen, even with the scanwidth set to 0!

I finally noticed this birdie only showed up when the LM386 audio amp was powered. I had tapped into the A&A 5-volt supply that fed the counter circuits. The birdie was generated in the digital counter logic, and coupled into the Hammond enclosure via the 5-volt power. A small 0.05 ceramic cap across the 0.001-pF 5-volt power feedthrough stopped the nonsense.

More notes on improving the dynamic range

I found strapping together the cans of coils, L2, L3, L4, L6, and L7, and the metal can of the DBM, provided an additional -3 dB decrease in the analyzer baseline. I used

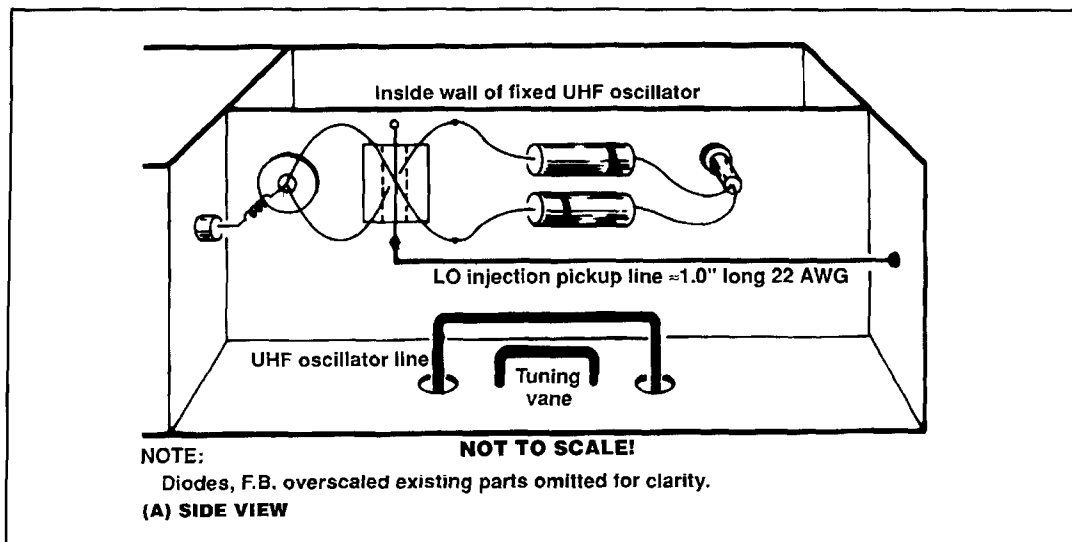


Figure 5A. A glance at the inner sidewall of the fixed oscillator compartment shows the pictorial layout of the new balanced mixer.

0.1-inch copper desoldering braid. DO NOT connect the braid to the enclosure or any other point! You may try extending the braid from the DBM can to the bottom sidewall of the Hammond enclosure while viewing the display.

If the baseline drops, connect it permanently to a solder ground lug. This lowered my baseline by another 0.5 dB, or so. Local oscillator leakage was no longer detectable at this point.

Remember, there is little you can do to increase the upper end, but anything that results in a lowering of the baseline level is recovered dynamic range.

Intercept and slope

These controls are covered in the AD606 application notes.⁸ While the FAR Circuits

board has provisions for including trim pots (R3, R4) for control of the intercept and slope, I didn't use them here. Thus, values for R3, R4, and associated resistors R5 and R6 aren't given. Typical values are supplied in the AD606 notes if you wish to include these controls. These four resistors aren't installed on the FAR Circuits board.

Log output setting

An output level pot (R7) is provided to set the log output signal to the level for which your analyzer was designed. It lets the log output be set to match the RSSI levels of the MC3356 Motorola chip this board replaces in the A&A analyzer. Excessive log-signal levels to the A&A will lead to misalignment of the A&A

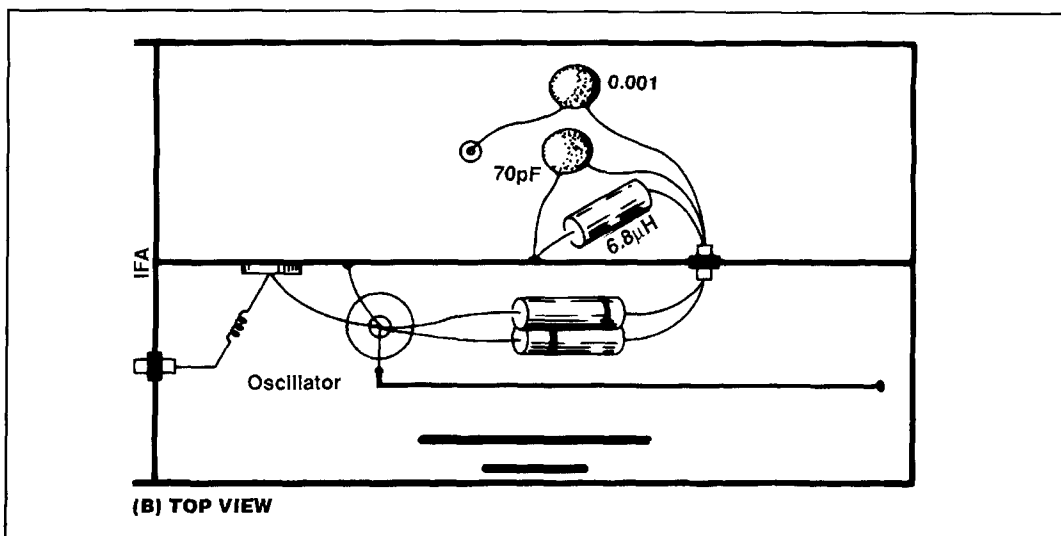


Figure 5B. Another view of the new mixer, looking down into the compartment. Note the positioning of the new LO pickup line for second mixer LO injection.

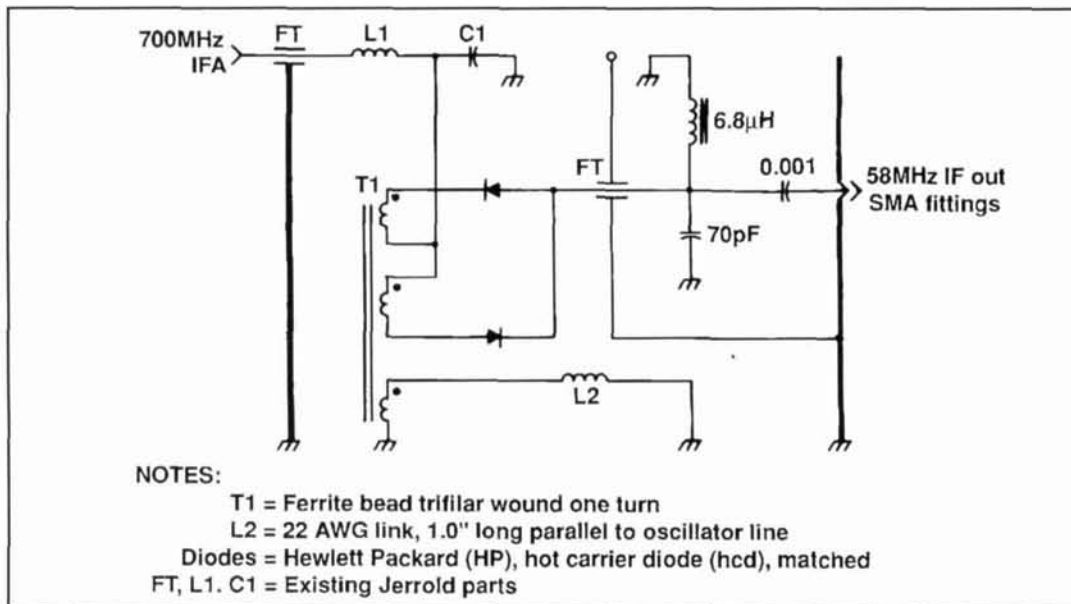


Figure 5C. Schematic of the new balanced mixer. The 6.8 µF choke and 70-pF capacitor are in the next compartment and are connected with short leads. The optional 58-MHz bandpass filter may be installed between the FT capacitor and the SMA fitting in this compartment.

vertical output pot (RE) and result in retrace line or retrace interval "ghosts" of displayed signals becoming visible on screen. This analyzer drives the baseline off screen (downwards) during retrace; it is not blanked during

retrace. The A&A analyzer also provides the horizontal sweep signal to an X-Y capable scope. The log amplifier may drive a scope display directly—if your design provides for retrace blanking.

I've added a 1000-pF video filter capacitor (actually a feedthrough capacitor through the aluminum box enclosure) to reduce on-screen noise. It has minimal effect on the faster scan rates and is used primarily for RF bypassing. The A&A video filter has far greater effect.

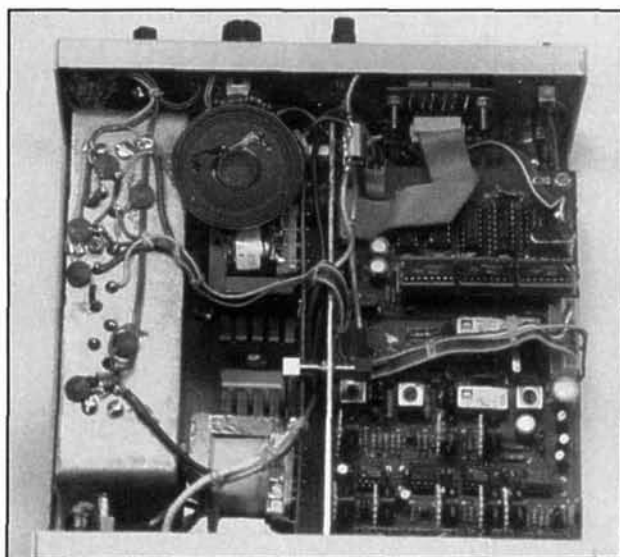


Photo F. A peek inside shows the new layout for the major internal assemblies. The main board is turned 90 degrees and mounted to the far left. The power supply is now mounted vertically in the center of the enclosure. To the left of the power supply is the Hammond die-case box, which houses the new IF and log amplifier sections. The numerous 0.001 feedthrough capacitors and additional 0.05 disc capacitors are visible on the Hammond wall. Although not visible, the Jerrold module is piggybacked beneath the main circuit board mounted 180 degrees around from the original position. The new 1024 µs crystal-controlled generator is also visible. Note the strip of three ICs piggyback-mounted on the main A&A board. One chip is in a wire-wrap socket whose pins connect to a chip socket on the main board.

RF alignment

All RF stages are peaked for greatest signal amplitude on the analyzer display. Note that L2, L3, and L4 may give false initial peak settings. Go through the alignment procedure several times to ensure these stages are properly peaked. As a final touch, adjust the 58- and 10.7-MHz coils *slightly* for more symmetrical filter response—especially at the crest of the filters and for the skirts at the -70 dB points. The settings of L6 in the high-pass filter and for L7 aren't critical; use the factory designations. If you include the optional IF gain control, set it to the most frequently used gain setting for final alignment.

Setting the scope display

Perform these steps with an accurate step attenuator and signal generator in order to verify the proper setting of the log output level and the 0 dB scope graticule point, in addition to the vertical scope positioning control. Select

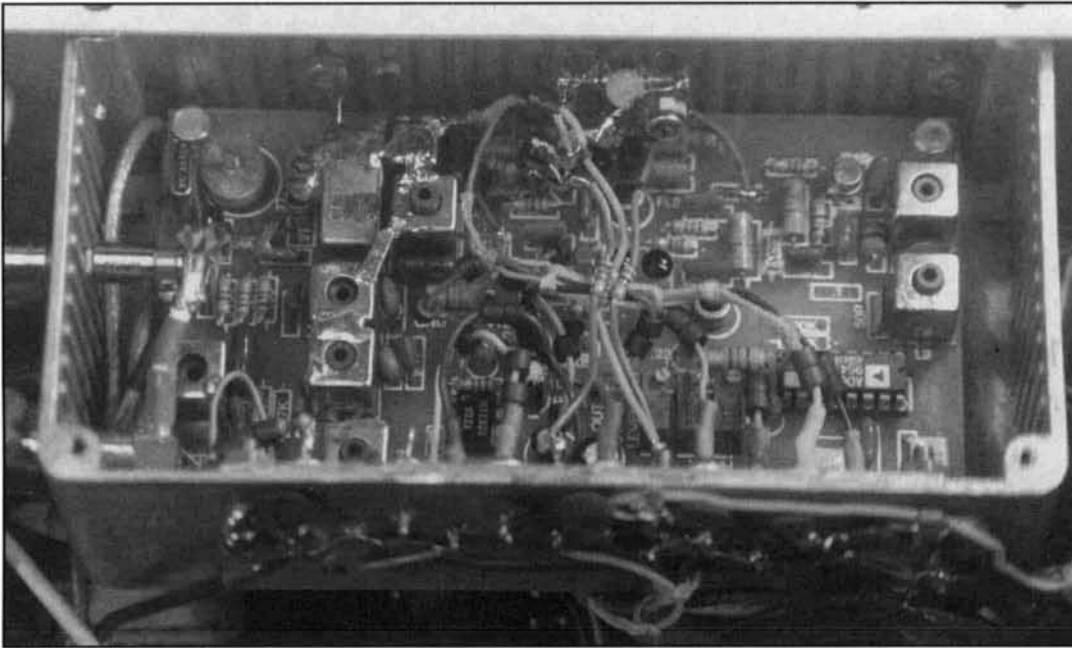


Photo G. The FAR Circuits pc board mounted in the Hammond box. The added 0.1-inch braid strapping between coil shields is visible. The reference level pick-up coil at the lower right is nestled against the LO toroid coil. Note the generous use of ferrite beads on all leads entering the Hammond enclosure. The optional "broad" bandwidth IF amp is visible on the lower center bottom wall of the Hammond box. The ground return for this module goes directly to the FAR Circuits pc board.

the wide filter and turn on the video filter. The 0-dB marking on my display corresponds to an input level of from -10 to -25 dBm—depending on the IF gain setting. I usually set the gain so the 0-dB marking corresponds to a -20-dBm input signal.

Adjust a signal from a signal generator to show signs of gain compression at the 0-dB scope Y axis graticule marking, then reduce it by 3 or so dB. The ideal point results in a 10-dB increase in signal strength from the -10-dB scale, which provides a display within 0 to -1 dB of the 0-dB graticule mark. Signals above the 0-dB marking will be going into gain compression and displayed nonlinearly; but, they should drive the crest of the signal "off the CRT display."

Starting at the -10 dB graticule mark, each 10 dB reduction in signal strength should fall within a 1/2 dB of the corresponding graticule marks down to -60 dB. The -70 dB signal should be close, but may be off by 3 dB or so, depending on the IF filters selected and the IF gain setting. Signals at the -70-dB point will be somewhat "noisy," especially if the video filter is off.

The -70- to -80-dB range is usable, but the -80-dB mark will fall above the bottom scope graticule line. A signal 10 dB under the -70-dB marking should be about 1/4 above the -80-dB marking and above the baseline noise. Signals at -90 dB (about 3- μ V for my A&A analyzer) should be just barely visible above the baseline noise. A new Y axis line should be added to the

scope graticule to show the proper -80-dB calibration point. After the -70-dB level, the log amplifier performance falls off. The AD606 device is specified for an 80-dB-log range, but that level of performance is difficult to achieve in any multiple conversion scheme.

If you don't select the video filter, the baseline "grass" will limit the analyzer to about a 70-dB range. The display range, including non-linear areas, may reach 90 dB. With the A&A video filter disabled and high IF gain settings, the noise spectra (baseline grass) will cover up to or above the -70-dB graticule, limiting the analyzer to about a 70-dB range. With the video filter off, you should be able to get at least 80 dB on screen, although some interpolation will be needed under -70 dB. This is a respectable figure for a homemade analyzer.

The LM386 audio stage

Many inexpensive spectrum analyzers can't monitor signals. I considered adding an FM discriminator to the limiter outputs provided by pins 7 and 8 of the AD606, but Stas, W6UCM, of A&A Engineering suggested an easier and cheaper method he uses in export models of the A&A spectrum analyzer.

Stas pointed out that the IF filter skirts could be used to "slope detect" signals. I tried his suggested LM386 audio circuit and it worked surprisingly well. The A&A analyzer (actually,

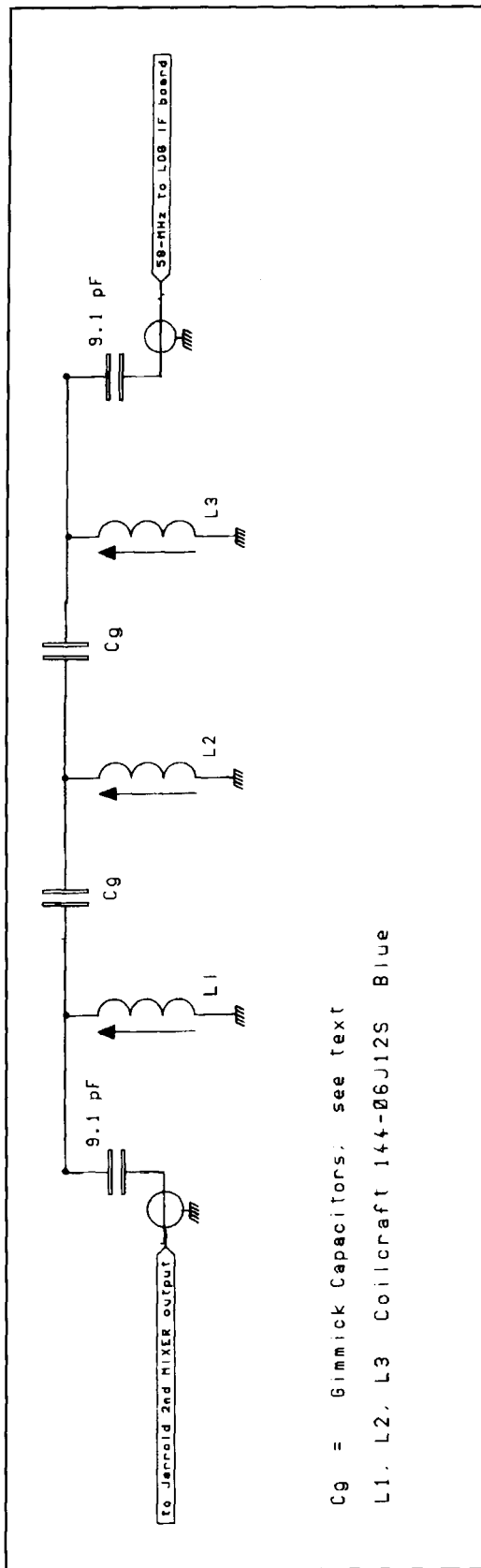


Figure 6. Schematic of the 58-MHz bandpass filter. Coils L1, L2, and L3 are "gimmicks" made up of 1/2-inch capacitor leads in close proximity.

the free-running UHF oscillators in the Jerrold CATV model) are quite stable, allowing you to monitor FM broadcast stations for hours once the analyzer warms up. The recovered audio was better than expected using this sort of detection. Even music reproduction was acceptable—certainly no worse than that of a cheap \$10 FM portable! The LM386 audio stage is included on the FAR Circuits pc board (see Figure 1D).

FM audio recovery

With the analyzer set for 0 swept, adjust the analyzer tuning to place the input signal on the slope of the IF bandpass curve. The log output signal will then supply demodulated FM audio. The wider filters work well for wideband FM, like that used in TV or FM broadcasting, while the narrower (25 kHz or less) filters do well for narrowband FM detection. There's still some AC modulation on the Jerrold VCO due to the proximity of the power transformers. A loud hum is normal on narrowband FM signals.

AM audio recovery

Log amplifiers are a "natural" for demodulating AM signals. In this mode, I set the analyzer to the crest of the signal and then for 0 sweep, which made it easy to monitor AM stations on HF shortwave, AM broadcast, and the aircraft bands. The analyzer is accurate only to about 5 MHz, due to the limitations of the first Jerrold mixer. However, it will still receive signals in the AM broadcast band. It was interesting to "watch" the demodulated video signal from WFSB Channel 3 in Hartford. The sync pulses and video waveform were quite clear. With the video filter in line, the color burst signal was plainly visible. Signal characteristics seen in the frequency domain can also be viewed in the time domain!

If you include the audio amp stage, use a 25 k or higher audio taper pot between the log output and the audio stage. This will load the output of the AD606 slightly, and the log output pot will need to be retouched. (Remember, connect the high side of the pot to log output!)

An external and baffled 4- to 8-ohm speaker sounds best. I mounted a small speaker internally for portable use, but I use a larger speaker at home. The audio amplifier is intended to run on 5 volts. In the A&A unit, 5 volts is available from either of the two regulated 5-volt supplies. An off/on switch on the pot lets you turn off the audio amp when not in use.

Another useful feature of the audio amp is that it lets you "hear" signals that appear, without watching the CRT. If the audio stage is left

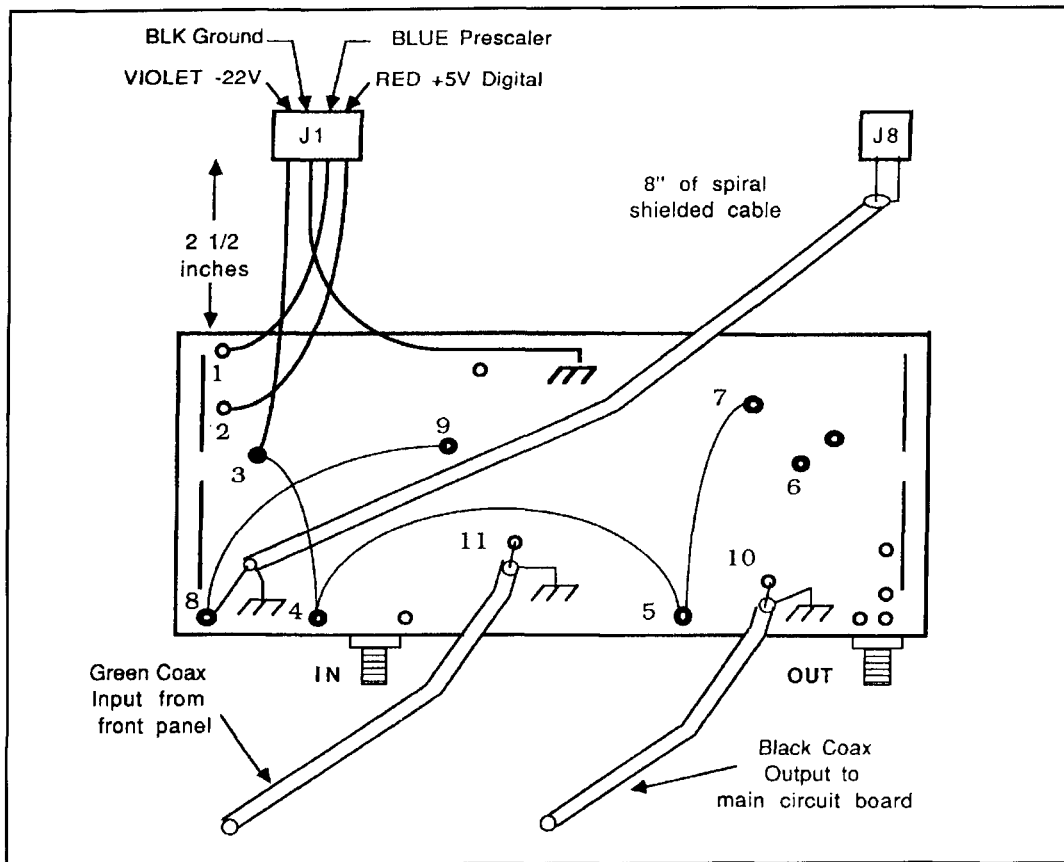


Figure 7. Tantalum capacitors with parallel disc capacitors are mounted at points 3, 4, 5, and 7 (marked with an "X") for additional filtering of the -22 volts DC supply feeds. The 5-volt feed to point 2 (marked with a "Y") is also treated in the same manner. Observe polarity! Short leads are a must.

on, you'll hear signals appearing within the scan limits as "pops" through the speaker as they're scanned over. With a few hours warm up, the Jerrold CATV module is exceptionally stable—even though it relies on two unlocked UHF LOs! I was able to monitor the Canadian time signals from CHU on 3.33 MHz for several hours in the narrow filter position without having to retune!

Parts selection

While I've specified CoilCraft coils, you may substitute TOKO or other brands. I've given the inductance ranges in **Table 1** for this reason. The low-value capacitors I chose are disc ceramics or dipped micas, but you may use either style. If you find a particular value hard to find, try the next size smaller standard value; i.e.; use a 33-pF to replace a 34-pF value. Remember, the tuning range of these coils is limited. All bypass caps from 0.001 through 0.22 are either ceramic monolithic or disc capacitors. Miniature tantalums may be used for the higher 0.22 μ F values. Almost all the resistor values are available in the Radio Shack

271-312A 1/4-watt resistor assortment. The FAR Circuits pc board is laid out for pots with footprints similar to the Bourns 3296 series 25-turn trimpot.

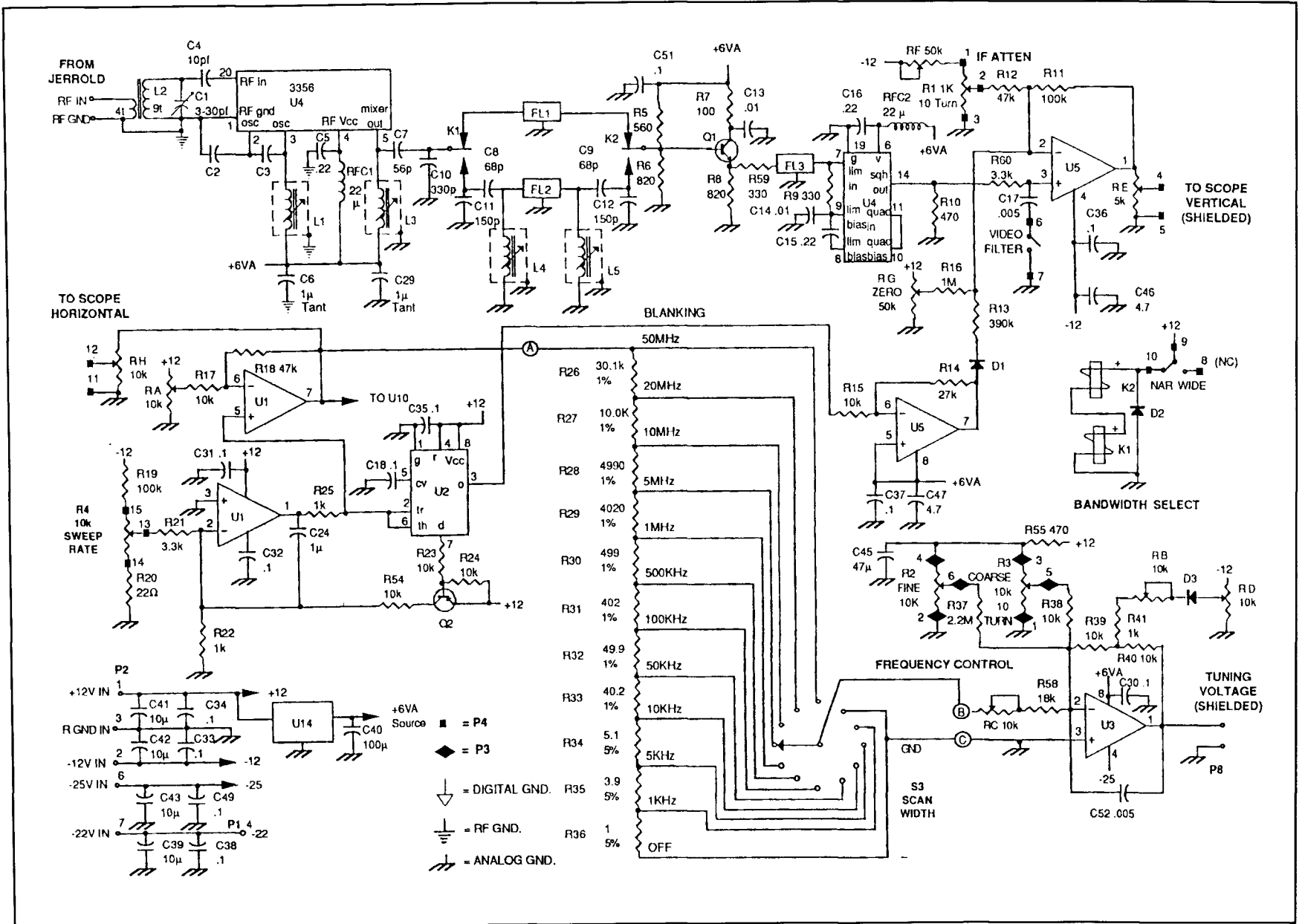
The IF stage gain adjustment pots are single-turn Weston 567 or Bourns 3329H series trimmers, available from discount surplus houses.

Choice of CRT displays

I use a Tektronix model 604 X-Y monitor with my analyzer. Having a dedicated display sure beats tying up my bench Tek 465 scope! Also, it was a hassle to set up the 465 scope for X-Y operation and the vertical and horizontal gain and positioning controls each time I needed to use the spectrum analyzer. Use of a 100-MHz scope can lead to stray RF pickup in the Y amplifier when working around strong RF fields.

The Tek 604 six-inch CRT is quite impressive! The large screen allows more accurate readings with a lot less eyestrain. These units show up surplus or at ham fleamarkets, often at bargain prices. I got my first at a ham auction for \$10. One note: the BNC fittings on the TEK

Figure 8. Linear circuitry for the A&A version of the Helfrick design.



604 aren't grounded. I noticed some AC ripple riding on the baseline until I connected the cable shields to chassis ground on the X and Y amplifier pc boards.

You might also keep your eyes open for the Tek 603 X-Y scope. This model has a storage-type CRT. Make sure the CRT phosphor is suitable for spectrum analyzer use and has medium or long persistence. My second 604 had a short persistence CRT—not very good for the slower scan rates! The Tek units also have provisions for Z input, which is useful for retrace or baseline blanking. I suspect the A&A analyzer could provide for this with slight modification. (Pin 3 of U2 looks like a likely starting point.)

Note that the variable gain settings for these displays are internal and that there are internal switches for high or low sensitivity settings on the X and Y channels.

Interfacing to the Helfrick/A&A spectrum analyzer

Let's start the interface process with modifications to the A&A spectrum analyzer and Jerrold 450 CATV module.

There are several appealing things about the Helfrick/A&A Engineering spectrum analyzer. Since its publication in *QST* in November 1989, there have been many copycat designs using TV tuners or CATV converters. Few, however, approach the professional features offered in Helfrick's layout.

Helfrick's analyzer allows a full scan from almost 0 to 500 MHz. Varactor diode nonlinearities are compensated for and result in a true correlation between frequency and graticule markings over the entire CRT display at the maximum 500-MHz scan dispersion. A three-digit LED display shows the analyzer center frequency. Several calibrated scan widths from 0 to 50 MHz per division are provided. Two bandwidth positions, selectable video filtering, adjustable sweep rates, and coarse and fine frequency controls round off the list of features.

Once the limited dynamic range problems are overcome, the analyzer is quite a performer for the investment. My only serious complaint is that A&A Engineering never offered an internal RF attenuator scheme. I use outboard variable attenuators with my unit, in addition to Rick Littlefield's -30-dB signal tap for transmitter testing.⁹

Now, on to the modifications. I suspect this IF and log amp board will work with other units, like those offered by Science Workshop, but I'm not prepared to offer advice on these units.

The necessary changes will involve substan-

tial modifications to the internal layout of the A&A analyzer, and some internal rework to the RF sections of the Jerrold CATV module. If you're not experienced in UHF techniques, I suggest you don't attempt any internal modifications to your Jerrold module.

These modules up-convert the CATV TV channels to a fixed IF in the lower UHF range. This IF has a combined bipolar amplifier and bandpass filter stage. A second mixer stage, with a fixed UHF LO, downconverts the IF to the desired TV Channel 2, 3, or 4 VHF IF to feed a television. Each stage of the module has its own individual compartment. A special spring shield and top cover plate provide shielding. **Figure 4** shows the important internal sections of the Jerrold modules.

It's easier to start with a unit that's working and calibrated! Unfortunately, the original *QST* design used a now-obsolete Jerrold model 400 CATV module with an upper frequency limit of 400 MHz. The current A&A spectrum analyzer is built around the Jerrold 450. This module uses a higher first IF (551 versus 516 MHz) and a VCO that operates at a slightly higher frequency and with greater range. Consequently, it required a redesign of the original Helfrick frequency counter scheme that calculates and displays the center scan frequency of the spectrum analyzer. To upgrade to the Jerrold 450, order a complete information package from A&A Engineering. This will provide the circuit changes needed to modify Helfrick's counter circuit to accommodate Jerrold's 450 CATV module. Coverage of the Jerrold 450 converter is out-moded by today's expanded CATV channels: newer modules reach well above the 450-MHz range.

Although, A&A is dropping the spectrum analyzer from their product line, they still offer boards, Jerrold CATV modules, and all other parts. **Table 4** lists the major assemblies and current pricing. For smaller components, you'll need the entire 5-page parts list. The display pc board is no longer available.

Read first, cut and chop later!

Read through the entire modification procedure before you begin! In some cases, you'll need to make up all new wiring harnesses, which will require new cable connectors. You'll do some drilling and major relocation of the A&A analyzer components, and you'll fabricate a metal bracket to allow for the relocation of the power supply assembly.

Is it worth all the work?

Two-tone tests showed that, for signals separated by only 2 MHz (and thus within the pass-

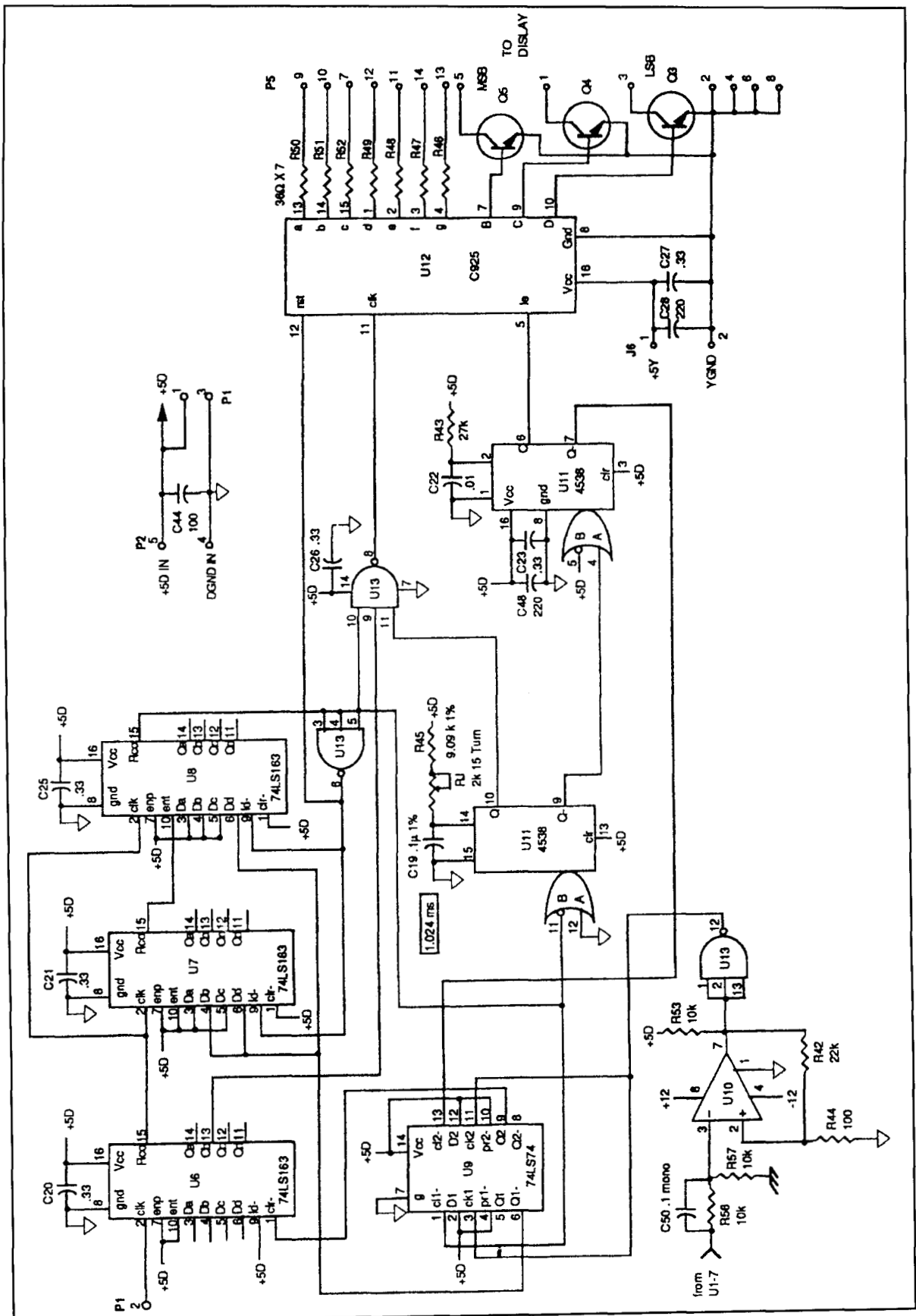


Figure 9. Digital end of the A&A analyzer. New counter design accommodates the newer Jerrold 450 module and also adds several corrections to the original QST design.

band of the first IF filter), the dynamic range of the instrument is in excess of 65 dB (third order products referenced to the input signals.) Due to the wide bandwidth of the Jerrold's 551-MHz first IF bandpass filtering—which for its original purpose must pass a 6-MHz bandwidth TV signal—signals separated by more than 12 MHz will have better IMD performance. At 20 MHz separation, the third order IMD products weren't visible with the two signals set at the 0-dB graticule. Other spurious signals, however, will appear throughout the analyzer range when signal levels are above the -10-dB scope graticule.

Some rework of the first IF stage (less gain, better device, sharper filtering) would probably improve matters. It would be hard to obtain a worthwhile improvement in selectivity for a 550-MHz IF that relies on LC technology. Arithmetic selectivity limitations make it far easier to achieve sharp LC bandpasses for IFs much lower in frequency.

Sometimes it's tempting to drop another 10 dB or so when looking for signals under those at the -20-dB log scale—especially for weak harmonics in the baseline noise. Be careful! If you attempt to force the analyzer when there are other strong signals, such as transmitter harmonics 50 dB below the carrier, they may mix internally and generate IMD products that fall on the higher order harmonic frequencies. This, in turn, may mask the readings you're trying to make. Always use the 1-dB RF attenuator steps to verify whether you're viewing an IMD product or true signal when forcing the analyzer. A true signal will follow 1-dB attenuator steps directly. An IMD product will change by 3 dB for every 1-dB RF input attenuator step. You can't use the IF gain control for this check.

The revised Helfrick analyzer is superior to most incorporated in high-end service monitors found in two-way radio service shops (the HP8920 may be an exception to this claim!). Some Cushman and IFR service monitors only offer a maximum dispersion of 10 MHz per division for a limited 100-MHz display. And, unlike analyzers using BWO or YIG LOs, the unit is easy and cheap to repair (the Jerrold 450 module is well under \$100!—see **Table 4**).

Jerrold CATV module modifications

Here's how to modify an assembled A&A Engineering spectrum analyzer:

Determine the exact center frequency of the first IF stage by injecting a strong signal from a UHF signal generator. Keep it under the maximum input rating specified by A&A Engineering to avoid damage to the first mixer

stage. Carefully sweep from 545 to 560 MHz, and note the exact center frequency of the first IF stage of the Jerrold CATV module. (This is for the Jerrold 450 CATV module. Earlier modules use a lower IF on 516 MHz.) Use a sensitive UHF counter with a short probe antenna inserted into the alignment "peephole" (over the fixed LO oscillator section) in the cover. You may cover this with a strip of copper tape. Note the exact frequency of the oscillator. Only insert the probe far enough to achieve a stable count. Once the modifications are finished, you may need to reset the oscillator frequency if the second mixer mods cause a frequency shift. This is done via a small tuning vane near the oscillator tuned line, which can be moved in or out to adjust the oscillator tuning. Insert a small insulated tuning tool through the cover to perform the adjustment.

The Jerrold second LO should be at 606 or 612 MHz depending on whether the IF output was designed for Channel 2 or 3. The first IF should have an Fc of 551 MHz. My Jerrold has a measured second LO of 612 MHz and a first IF centered at 554 MHz; thus, my IF board is setup for a 58-MHz RF input.

The Helfrick design had a variable free-running oscillator in the third LO (part of the MC3356) to compensate for variations in the actual IF output from the Jerrold CATV module. My IF board uses a stable crystal oscillator (47.3 MHz for my Jerrold) to supply the third LO. You must either order the correct crystal frequency or set the Jerrold's second LO carefully for a 58-MHz IF output.

This assumes that shifting the LO frequency doesn't move you out of the Jerrold's first 551-MHz IF's several MHz-wide passband. Before proceeding, carefully align the A&A, or your homebrew *QST* version, so it meets the original specs. I allow for some overscan, about 10 percent when setting the horizontal (X axis) sweep width on the A&A. This provides for some adjustment to align the center frequency to the center graticule marking via the horizontal positioning control on the scope.

Before and after

Photo C is the original A&A Engineering front panel. **Photo D** shows the panel after the addition of the controls for the IF gain and volume control, along with the addition of SMB fittings for the internal 47.3 MHz -40-dBm reference and the Jerrold's prescaler output. The prescaler output is for a planned outboard tracking generator.

A&A's original internal layout appears in **Photo E**. To make room for the Hammond enclosure, the main pc board is removed and all attached cables are disconnected. The Jerrold

CATV module is detached from the main pc board and the power supply board is removed. Set these assemblies aside for now.

Photo F shows how everything fits back into the box after the modifications are completed. Note that the main A&A board has been turned 90 degrees, and the power supply is now mounted vertically on a new bracket. The Hammond box is at the far right of the A&A enclosure. **Photo G** shows the FAR Circuits board inside the Hammond box.

Reaching 500 MHz

The Jerrold model 450 CATV module used in current versions of the A&A Engineering spectrum analyzer allows coverage from about 5 to 450 MHz. By carefully moving the varicap diode position on the VCO tuned line and/or the tuning vane near the oscillator, coverage to 500 MHz can be squeezed out of most modules. This is desirable, as the full scope CRT is now used when the 50-MHz per division scan width is used. My analyzer will go to 520 MHz, but signals at that point are severely attenuated by the low-pass filtering. If you adjust your Jerrold to go to 500 MHz, you'll also need to adjust (spread the coil windings) the low-pass filter on the Jerrold module input to allow for the higher frequency coverage. Because the first IF is at 551 MHz, some compromise of spurious 551-MHz RF input signal rejection may result. Also, my analyzer sensitivity falls off by several dB before the 500-MHz point is reached.

SMA or SMB connectors are a must!

The Jerrold RF input is now routed through either an SMB or SMA connector (a BNC fitting is too large). The pigtailed and spiral wrapped "coaxial" cable supplied with the Jerrold is grossly inadequate for the increased dynamic range and sensitivity of the modified unit! Signals as low as 3- μ V are visible. Also, the exposed BNC chassis connector used on the A&A front panel must be replaced with a fully shielded unit. I was surprised how many strong FM stations I "received" without an antenna before these mods were done. Signals as low as 3 μ V are visible with the new IF section. In my prototypes, harmonics of the 47.3-MHz oscillator made a nice comb presentation on the analyzer display—due to stray pickup from inadequate shielding.

New balanced second mixer

The first mixer in the Jerrold CATV module is a double-balanced diode built on a section of pc

board using discrete components. The second mixer uses only a single-ended diode. **Figures 4 and 5A through C** show how I replaced this with a balanced diode mixer for improved dynamic range. The diodes are a matched pair of Hewlett Packard hot-carrier diodes.

The transformer core for the balanced diode mixer was salvaged from a low-cost Channel Master TV signal splitter rated from 54 through 900 MHz. A VHF-UHF TV antenna balun may also provide a suitable core. A single hole bead is used here; some baluns may yield a dual-hole core. The ferrite bead-sized core was stripped of all windings. These were replaced with "single-turn" pigtail windings made from color-coded enamel magnet wire.

The leads are only long enough to allow for ground connections, connecting to the diode leads, and connecting to the new pickup line for LO signal injection. **Figures 5A, B, and C** provide construction and parts placement details. Keep things as symmetrical as possible.

The new mixer components are mounted on the inside wall of the CATV module in the second LO compartment (keep the mixer close to the metal wall). With the exception of the ground connections and new LO pickup line, connections to the new mixer are supplied by leadless ceramic capacitors or standoffs already present in the compartment. The LO pickup line, constructed out of tinned no. 20 bus wire, is installed for mixer injection. See **Figures 5A and B** for placement.

IF signal output

The Jerrold CATV module has a compartment section housing the post IF amplifier. Later models have a pin-diode attenuator for TriMode descrambling of protected pay channels. A&A Engineering modifications involve stripping all these components and replacing them with a tunable band-pass filter.

The 58-MHz preselection filter

While I didn't use the two-stage A&A filter, I did add a three-stage LC bandpass filter to improve the rejection of spurious signals falling near the 58-MHz IF. **Figure 6** shows my filter, constructed of CoilCraft coils and ceramic capacitors. The coupling capacitors are "gimmicks" and are nothing more than 1/2-inch lengths of component leads covered with insulating heatshrink. The proximity of the leads controls the degree of coupling—about 1/16-inch separation is sufficient.

The CoilCraft cans are seam-soldered together. Then the assembly is tack-soldered by the coil can tops to the bottom 58-MHz of the

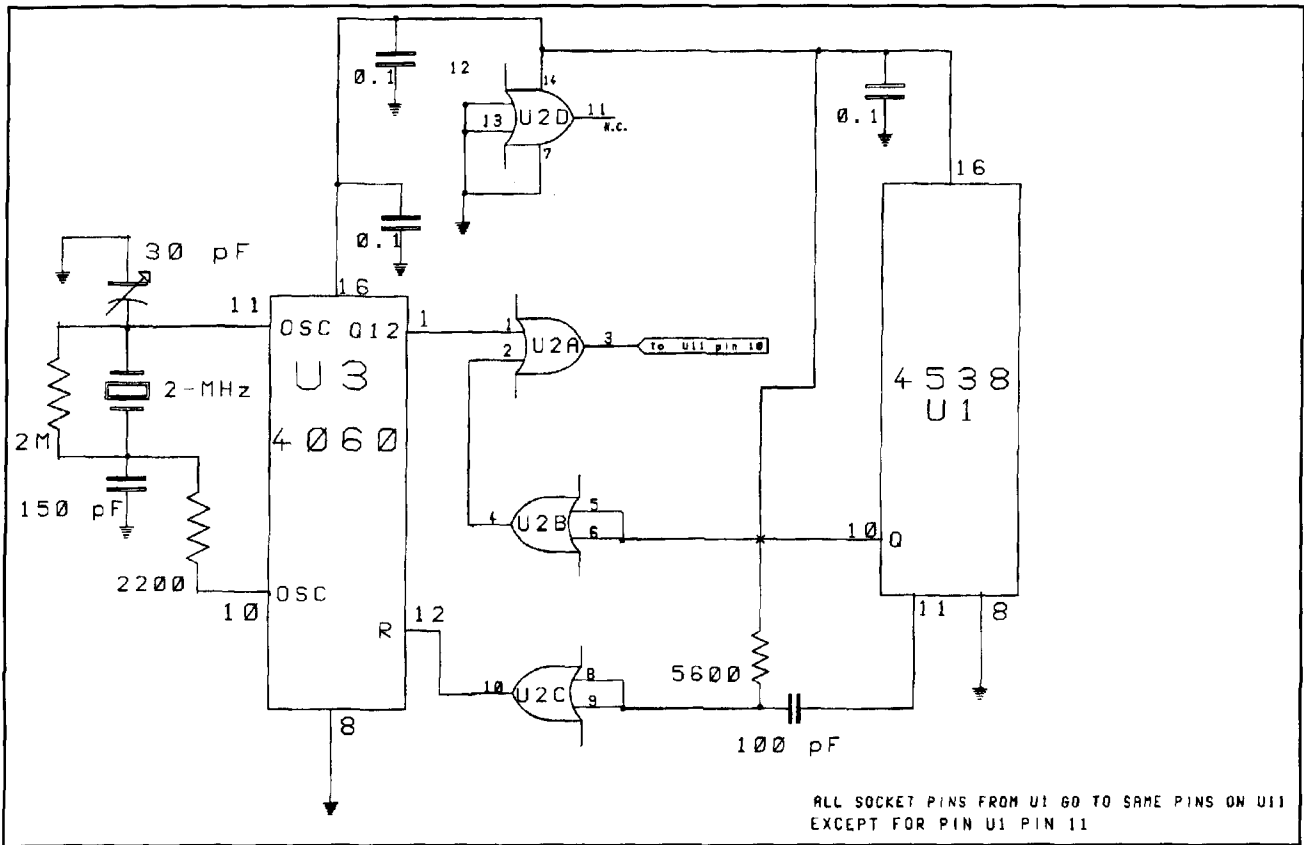


Figure 10. The W6UCM crystal-controlled 1024- μ s generator greatly improves the counter accuracy. Note that chip U1 essentially “piggy backs” over the old U11 on the main A&A board. All pins, except for pin 11, go “straight through” to the U11 socket.

Jerrold module. Next, the coils are adjusted from the bottom, with slugs favoring this tuning direction. If you’re careful, you may drill tuning holes in the Jerrold to access the coil slugs for alignment. The coil leads and capacitors must be bent over, as there’s little clearance to the top metal shield. Signals from this point are carried by high-quality miniature coax and SMB fittings until they reach the RF input on the pc board.

The preselector may be housed external to the Jerrold in a small minibox using SMA or SMB fittings. However, the 68-pF capacitor and associated RF choke should be left in the IF section of the Jerrold module, at the point where the second mixer output enters this compartment.

Bye, bye birdies!

Helfrick noted that the lower end of the HF range of his analyzer contained some internally generated birdies emanating from the Jerrold module. These were livable in his design, but become very noticeable with the new IF section and improved sensitivity. I found the birdies were the result of inadequate HF interstage isolation due to the nature of the VHF range feedthroughs used by Jerrold.

Ceramic 0.0022 bypass capacitors are installed at the fixed -22 volt power feeds to the Jerrold module (refer to Figure 7). These points are marked with an “X,” and 0.22- μ F 25-volt miniature tantalums are also added here (use very short leads). Observe the polarity for the tantalum—this is a positive ground! For some extra decoupling, I also added ferrite beads on the -22-volt interconnecting leads between the feedthrough’s junction points on the Jerrold module.

The 5-volt feedpoint for the Jerrold prescaler and LO amplifier section is treated with the addition of a parallel tantalum and disc capacitor combination. This is a positive voltage feedpoint, so observe polarity! A 0.005 disc and 0.22 tantalum are used here (see point “Y” of Figure 7).

Don’t add extra filtering to the VCO tuning and tracking filter voltage inputs on the Jerrold. Also, don’t add filtering to the prescaler output connection. Use good quality RG-174 or miniature TeflonTM coax from the prescaler output to the A&A circuit board, with short exposed center leads. Achieving a good tight RF fit of the cover, metal RF spring shield assembly, and the module is more important than ever.

These modifications dramatically reduce the

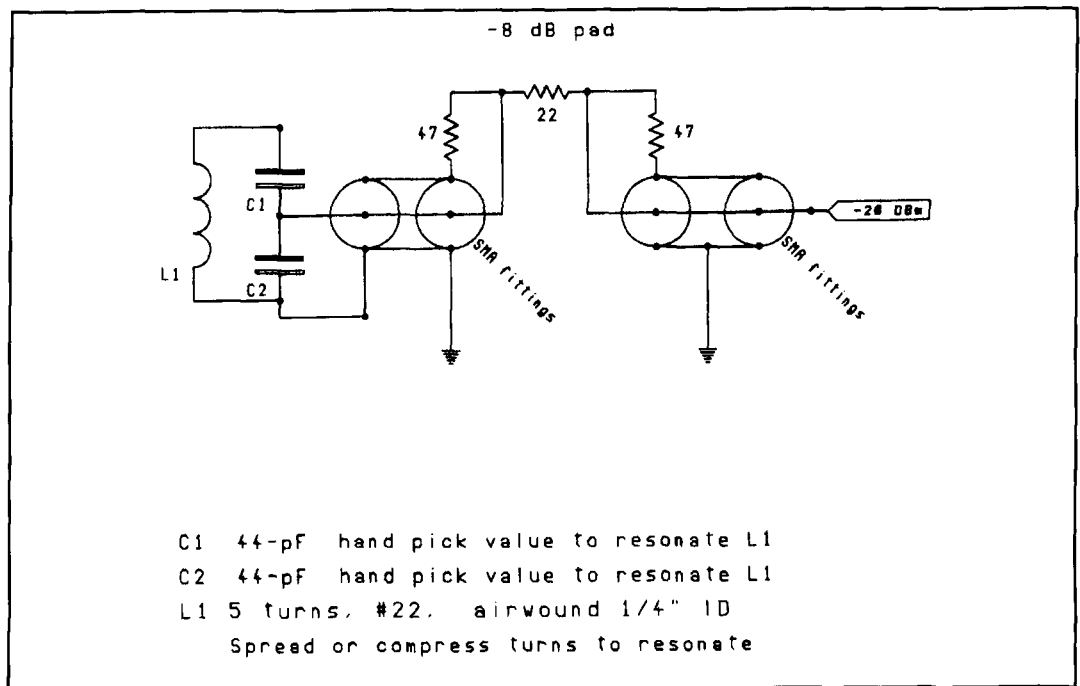


Figure 11. Sampling the 47.3-MHz crystal LO allows a convenient and accurate dBm and frequency reference.

amplitude and number of spurious signals in the lower HF range (and throughout the entire 500-MHz coverage) to an almost unnoticeable level. You may wish to try these mods even if you elect not to make any other changes to your unit. Of course, some birdies are inevitable when signals approach the 0-dB mark (-20 dBm.)

We're now done with the Jerrold module. Put it aside, but don't reattach it to the A&A main circuit board yet.

A&A circuit board changes

The A&A Engineering schematics are reproduced in **Figures 8** and **9**. **Figure 8** shows the analog sections; **Figure 9** the digital and counter sections.

Remove IC U4, the Motorola MC3356 (see **Figure 8**). To further conserve power, remove transistor Q1. Remove relays K1 and K2, or cut the 12-volt DC feed to their respective windings.

Connect a short length of RG-174 or miniature Teflon coax to pin 14 of the solder side of the IC socket for U and tie its shield to ground. The other end will be terminated at the log output feedthrough capacitor (0.001 μ F) on the Hammond 1590P box. Locate and remove R10, a 470-ohm resistor used from pin 14 of U4 to ground; locate and remove R5, a 560-ohm base biasing resistor for Q1.

Temporarily reattach the Jerrold module to the A&A board, but reverse its mounting 180

degrees from what the A&A instructions show. The reason? The orientation between the power transformers and the Jerrold module is critical. Make sure it's correct or the magnetic field will modulate the swept Jerrold first LO, and this modulation will appear on signals when you use the sharper IF filters and narrow dispersion scans. You'll probably find that the RG-174 cable to the connector for P8, and the four wires that go to the connector for P1, are now too short and need to be replaced with longer wires. I would suggest reordering new plugs and pins from A&A rather than trying to reuse the old connectors.

New power supply mounting bracket

Now, you must fabricate an L bracket from aluminum, large enough to mount the power supply on edge in the center of the A&A enclosure as shown in **Photo H**. The mounting lip of the L bracket that attaches to the chassis should be at least 1-inch wide. This will allow two of the four standoffs used to mount the main pc board to hold the power supply bracket in place. As a result, the power supply board is mounted on the side opposite the L bracket mounting lip. Fabricate and drill the L bracket as needed. Mount the board using short standoffs. Make sure the clearance is sufficient for the AC line voltages. Use insulating plastic if needed.

Carefully position the main pc board, the

power supply and its support bracket, and the Hammond 1590P as shown in **Photo I**. Mark and drill four holes for the four main board standoffs and power supply bracket. On final assembly, shim the two outside standoff with washers to offset the thickness of the power supply bracket.

Drill two holes that allow clearance for 6-32 screws through the A&A enclosure and the bottom side of the Hammond 1590P box. These screw holes will let you secure the Hammond box to the enclosure. There are some existing holes in the A&A you can use; one is for a front rubber foot mounting screw. I suspect the Hammond material is thick enough to permit using a 6-32 tap instead of nuts for mounting.

Find a center point between the A&A factory logo and the "VERT" BNC connector on the A&A front panel, and drill a hole for the miniature 25-k audio pot. Mount the optional IF gain control pot in similar fashion at a point that's equidistant between the display bezel and scan-width control.

Mark and drill four holes in the Hammond box, so the FAR Circuits pc board can be mounted using 4-40 hardware and 1/2-inch metal standoffs. Drill holes to mount, inline, seven 0.001- μ F feedthrough capacitors for the 12-volt DC input, 5-volt DC audio supply voltage, log amp output, AF audio in, AF audio out, wide filter select, and narrow filter select connections. (Note that the clearance from the Hammond enclosure to the A&A cover is very tight.) I used solder-mount feedthrough capacitors mounted on a brass strip—with holes that aligned with those drilled through the Hammond enclosure wall. The brass strip mounts inside the enclosure, so only about 1/16

of an inch of the capacitor leads protrude above the outer wall.

Provide a few solder lugs on the feedthroughs for ground connections. Drill a hole for and mount an SMA or SMB double female bulkhead for the 58-MHz signal input. Temporarily mount the pc board in the Hammond box, and wire the board to the feedthrough capacitors. You *must* use shielded coax and a connector to connect from the SMA or SMB fitting to the RF input on the pc board. Ferrite beads must be placed on the other leads to improve RF filtering and break up ground loops. Mount the pc board, connector, and feedthrough caps and finish all wiring inside the Hammond box. You can now install it in the A&A enclosure. (See the earlier notes regarding ground loops and this boards.)

With the box in place, and the main board and power supply also temporarily in place, most of the interconnecting cables and connectors are now too short. Make up new cabling for the power supply connectors and for the cables coming from the front panel controls and jacks. The ribbon cable from the digital display should be reusable. Don't reverse one of the DIP headers on this cable, or you'll destroy the expensive CMOS display driver. Also, when wiring up the new cables, note that the wiring for the IF bandwidth "Narrow/Wide" toggle switch no longer goes to the main pc board. The AC connections to the power supply board will also need to be redone. I suggest you order all new connectors and socket pins from A&A rather than trying to reuse the old ones.

Once the new cables are finished, remount everything permanently in the A&A housing. Add a pigtail hookup wire from a 5-volt regula-

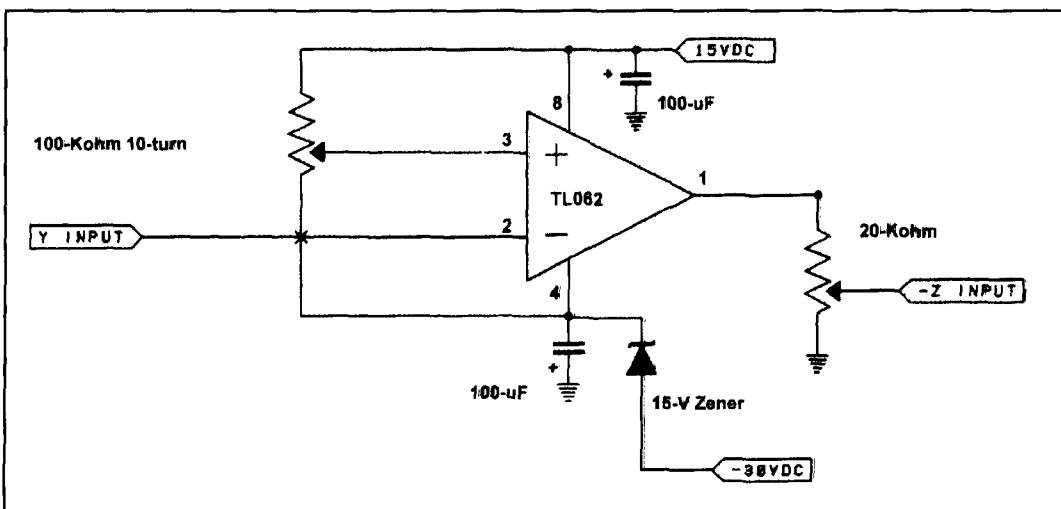


Figure 12. Variable baseline clipper. Simple op-amp comparator is built on a section of perfboard and mounted in the Tek 604 display monitor. The 15 and -30 volts DC are taken from the Tek 604 power supply. Pin 2 of the TL062 is connected to the monitor Y input; the opamp output from pin 1 goes to the -Z input of the Tek 604. The 20-k pot sets the blanking level "intensity"; the 10-turn 100-k trimpot sets the point at which the clipper blanks the baseline.

tor on the A&A power supply and from the 12-volt output of the 78L12 regulator. Connect the 12-volt lead directly to the feedthrough cap used for the 12-volt DC feed to the IF board. Next, connect the 5-volt pigtail to one side of the audio pot power switch. The other side connects to the audio amp power input (5 volts) feedthrough capacitor. The center arm of the IF bandwidth toggle ties into the 12-volt feedthrough capacitor. The wide and narrow filter connections on the toggle switch go to the appropriate IF bandwidth selection feedthroughs on the Hammond box. Connect the free end of the RG-174 cable from the main pc board (pin 14 of U4 connection made earlier) to the feedthrough used for the "LOG OUTPUT" signal of the AD606.

Connect a short piece of shielded audio cable from the "log output" feedthrough to the high-side arm of the audio pot. Use the shield to supply the low-arm ground return back to the BNC fitting ground solder lug. Connect the arm of the pot, again with shielded wire, to the "AF-INPUT" feedthrough. Also, ground the shield to the solder lug provided. You'll need a miniature oval speaker (transistor radio type) if you want audio monitoring. You can epoxy a small speaker inside the A&A cover so it fits over the rear ventilation holes. The speaker leads connect to ground and to the "AF-OUT" feedthrough capacitor. Otherwise, use a small earphone jack mounted on the rear panel for an external speaker or headphones. A larger external speaker provides higher fidelity.

Improving the counter accuracy

Helfrick's frequency counter scheme determines the center scan frequency of the analyzer LO and relies on the long-term accuracy of a free running 1.024-ms one shot. Some overseas users of the A&A Engineering analyzer have complained about temperature drift problems associated with the counter display one-shot circuit. While I never felt this was a serious problem, A&A has been including the modification shown in **Figure 10** in export models. It greatly improves the accuracy of the counter display. The circuit can be built on a small section of perfboard using just three ICs are used. One of them, the 4538 (chip U11), removed from the A&A main board, is now used for U1 on the new add-on board (refer to **Figure 10**). The 4060, IC U3, is a 2-MHz crystal oscillator and a divide-by 2048-counter (2 to the 11th power), which yields an output of 976.56 Hz. This has a period of 1.024 ms. In my unit, I needed a crystal frequency of 2.025 MHz because I had retuned the Jerrold IF to a slightly different frequency.

Only pin 11 of U11 isn't carried directly to

U1 on the add-on board. This lets you use a wire-wrap 16-pin DIP IC socket for U1, the 4538, on the perfboard to mate with the U11 socket. Wire-wrap pin 10 is cut short so it doesn't reach the socket for U11 on the A&A board. The cut-off lead is used for the flying lead from pin 3 of U2, a 4001, to U11 socket pin 10.

Pot RJ on the A&A board is set to produce a pulse greater than 1024 μ s; a good value is 1500 μ s. The 1500- μ s pulse from pin 11 on the old U11 socket now does two things: it fires U1 and resets U3 (4060). The 4060 begins its count-down from 2 MHz, and the resulting 1024- μ s pulse passes through gate U2A, which is set for a 1500- μ s window. The counter is then reset. This circuit board is visible in **Photo F**.

Optional level and frequency standard

Figure 11 provides details of a feature I recently added to my analyzer. This is another cut-and-try modification that provides a calibrated -20-dBm reference signal on 47.3 MHz. It does two things. First, it lets you set the original Helfrick counter frequency display accurately. Second, it lets you make accurate signal level readings from the relative dB graticule scales using the IF gain control to calibrate the analyzer display.

An SMB bulkhead fitting is installed near the 47.3-MHz oscillator in the Hammond enclosure. A small pick-up coil (5 turns no. 22 enamel, 1/4-inch ID) is used to pick up stray radiation from the field near the toroid coil. This pick-up loop is tuned and matched to the 50-ohm line feeding to the Jerrold using fixed value miniature ceramic trimmers. The coil is resonated by spreading or compressing its turns. Some cut-and-try experimentation is needed here. The coil and resonating capacitors are attached to a very short coaxial pigtail from a right-angle SMB fitting inside the enclosure.

I obtained the best signal levels by placing the coil near the "cold" end of the toroid primary winding. The pick-up coil orientation is critical. *Do not* attempt to place another secondary winding on the toroid for this purpose! Once you've reached the desired signal level (-20 dBm after the 8-dB pad) fix the coil in position with silicone adhesive. If the analyzer baseline is affected by this mod (upward shift due to 47.3-MHz energy reaching the AD606), some further experimentation is needed.

Terminate the analyzer input with a 50-ohm pad when making critical measurements or the RF input impedance won't be well defined. An internal -8-dB pad (allowing use of common 47 and 22-ohm resistors) is placed inline with the

-20 dBm reference signal to present a 50-ohm termination to the analyzer RF signal input. The reference signal SMB jack is just above the BNC RF input fitting (see **Photo D**).

Final steps

Assuming your analyzer was calibrated before we began, all you need to do is align the new IF and log section, as outlined in the first section of this article. Set the log output trim resistor to correspond to the original output levels of the MC3356. *Do not adjust the FE trimmer on the A&A circuit board to make these corrections. Use the 1-k log output pot on the new IF board to calibrate the 10-dB log steps to align with the Y axis display markings instead!* Set the scope vertical input (Y axis) to 50-mV per division and for DC coupling. Then set the horizontal (X) input to DC coupling and 1 volt per division. If you're using a Tek 604, preset its inputs to correspond to these settings using an audio signal generator and calibrated shop scope for reference. The 604's Y amplifier should be set to the high gain setting.

At this point, you may wish to go back and retouch the settings of other alignment pots on the A&A main board—especially if you increased the analyzer range to reach 500 MHz. Once you're happy with everything, mark the new -80-dB graticule on the scope display. Make sure the AD606 slope and log output levels are properly set before scribing any new lines! If you have a steady hand, I suggest you make your own custom scope graticule overlay using a sharp drafting pencil, some graph paper (blue ink doesn't photo copy), and a good drafting ruler. Once you have a viable graticule design on paper, use high-temperature copier transparency film to reproduce your artwork on a copier. Most copy or print centers will do this for a nominal fee.

Baseline variable clipper

Figure 12 is an afterthought added internally to my Tek 604 monitor. An IC voltage comparator allows the display to be partially or fully dimmed for signals falling below a preset level. Mine is set to partially dim the display for signals at or below the -75 dB level.

I added this circuit for a simple reason. The display intensity varies greatly depending on

the writing speed of the electron beam. Because the scan speed is fixed, when signals are encountered the electron beam must "detour" from its X axis scan to write in the Y plane at a faster rate of travel—shortening the amount of time the electron beam has to illuminate any point in the signal display area. When using the wider scan dispersions, the displayed signals become fairly dim while the baseline remains quite bright. The natural tendency is to turn up the brightness to compensate, but this usually results in the display being over-driven, causing signals near the baseline to become "fuzzy" and out of focus.

The baseline clipper allows for a more uniform display brilliance and helps protect the CRT from long-term "burn-in" at the scope baseline. There's some interaction between the monitor's intensity setting and the setting for the op amp output.

Future plans

What's next? Hopefully, a tracking generator for use on this or other analyzers, incorporating CATV modules equipped with internal divide-by-256 prescalers. Sharp-eyed readers will note an SMB fitting is already in place in the upper left-hand corner of my front panel for this purpose!

Acknowledgments

My sincere thanks Stas, W6UCM, of A&A Engineering and Fred Reimers of FAR Circuits.

I dedicate this article to the memory of Frank Maggiore of Maggiore Electronic Labs, who became a silent key this past spring. ■

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A STABLE OSCILLATOR

Try this straightforward design

This stable oscillator is a “throw-together” proposition with a cookbook design recipe. The design procedures here are straightforward, and are presented along with parts selection criteria. What results is an oscillator whose stability is almost entirely limited by the stability of the resonator.

There are many types of oscillators, but all must address three common concerns. These are: (1) an amplifier suitable for the frequency, (2) a feedback network that provides the necessary phase-shift and phase-shift change with respect to frequency, and (3) impedance matching. An amplifier “suitable for the frequency” includes phase shift through the amplifier, gain at the operating frequency and ability to control the gain of the amplifier, and sensitivity of the device parameters at the operating point. The feedback network must provide positive feedback only at the desired operating frequency. Impedance matching is usually required when coupling the feedback network into and out of the amplifier.

The common oscillator uses an amplifier with a nominal 180 degrees of phase shift between input and output, so the feedback network must provide an additional 180 degrees of change. The Colpitts oscillator and its variants use a pi network to provide the phase shift and impedance matching, while a few oscillators use two amplifiers to produce 0 degrees of shift. The Butler oscillator, in one configuration, uses an emitter follower and a common-base amplifier to produce 0 degrees of phase shift. The Franklin oscillator uses two cascaded grounded cathode amplifiers, each providing 180 degrees of phase shift, to produce an overall 0 degree change. In these two-stage oscillators, the feedback network provides 0 degrees of phase shift at the operating frequency. Two-stage amplifiers can have higher open-loop gain that can be trad-

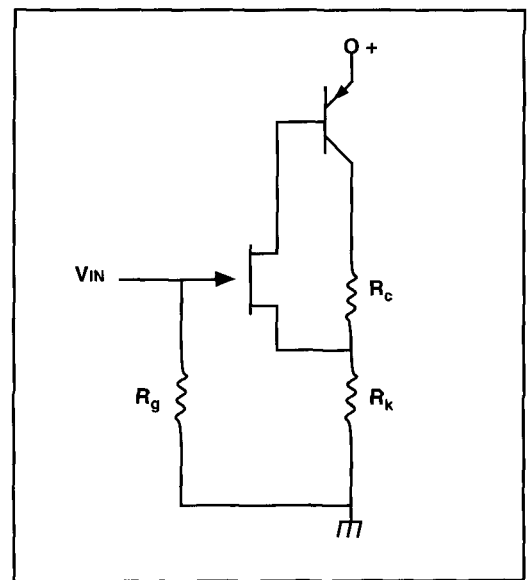


Figure 1. A hybrid amplifier can offer excellent operating point stability.

ed for losses involved in stabilizing the amplifiers and isolating the resonator from the amplifier and from the output load.

When large, expensive vacuum tubes ruled the electronics world, circuit designs emphasized reduction of the tube count. The design rules have changed with present-day semiconductors, because the active devices are inexpensive and small. In fact, in monolithic linear ICs, transistors are so inexpensive they're used as resistors. Today there's little advantage to be gained in minimizing transistor counts if it requires a significant increase in the number of passive components required.

The amplifier shown in **Figure 1** uses an N-channel JFET amplifier DC coupled to a PNP base junction transistor (BJT) amplifier to pro-

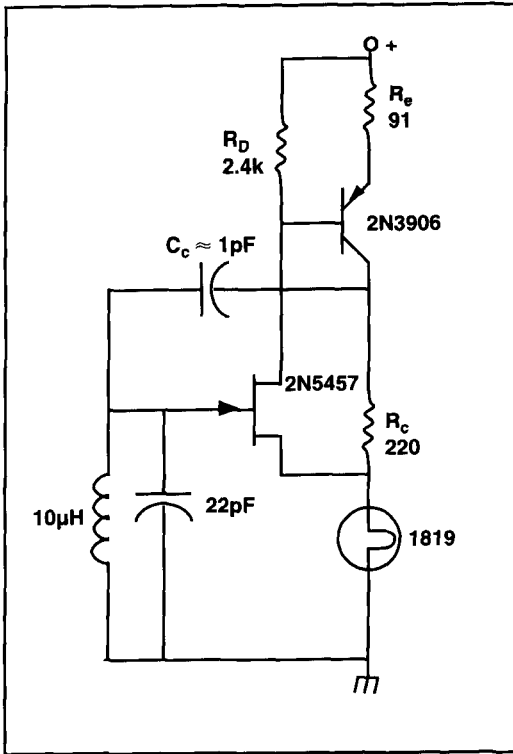


Figure 2. An oscillator can take advantage of the stability of the hybrid amplifier.

duce an amplifier with 0 degrees of phase shift. This amplifier can be viewed as a source follower whose input is from gate to ground, and whose output is from source to ground. In a source follower, the source voltage is in phase with the gate voltage and the voltage gain is less than one. The 100 percent negative feedback leads to great stability in the operating point and also increases the input impedance of the amplifier while lowering the output impedance.

The voltage gain (output signal to input signal) of a simple source follower can be expressed as:

$$VG_{sf} = G_{fs} \times R_k / (G_{fs} \times R_k + 1)$$

where:

G_{fs} = forward transconductance, dI_D/dV_g

R_k = resistance source to ground

In Figure 1, the BJT multiplies the G_{fs} of the JFET by its current gain (h_{fe}). Therefore, the effective transconductance of the pair is:

$$G_m = G_{fs} \times h_{fe}$$

The gain of the pair is then:

$$VG_{sf} = G_m \times R_k / (G_m \times R_k + 1)$$

In a FET, the drain current is nearly indepen-

dent of the supply voltage when the drain to source voltage is greater than $V_{pinch-off}$, and in a BJT, collector current is nearly independent of collector voltage when collector to emitter voltage is greater than a few volts.

Therefore, in Figure 1, the value of resistor R_c is small enough that emitter-to-collector voltage is always several volts. The collector current, then, is dependent only on the base current supplied by the FET.

The current in R_k is $(I_D + I_C)$, and the voltage at the source of the FET can be expressed as:

$$e_k = R_k \times (I_C + I_D)$$

The voltage at the BJT collector can be expressed as:

$$e_c = R_c I_C + R_k (I_C + I_D)$$

The oscillator shown in Figure 2 uses the basic amplifier of Figure 1 with components selected for operation at 10 MHz. The LC resonator at the JFET gate is resistive at parallel resonance and produces 0 degrees of phase shift. The 1-pF coupling capacitor, C_c , between the collector and the gate, isolates the resonator from the output. The 1-pF capacitance can be provided by a "gimmick," two short insulated wires twisted together, or a high value 1/4-watt composition resistor. The end-to-end capacitance of the resistor plus circuit strays will probably be about 1 pF. The value of the resistor isn't critical if it's large compared to the shunting reactance; that is, greater than 150 k.

The gate-to-ground impedance of the JFET is very high and stable, and presents little loading on the resonator. When the source lead inductance is zero, the input impedance of the JFET is a capacitance that can be expressed as:

$$C_i = C_{gd} + C_{gs}(1-A)$$

where:

C_{gd} = capacitance gate to drain

C_{gs} = capacitance gate to source

A = voltage gain of the source follower

While both C_{dg} and C_{gs} vary somewhat with operating voltage, C_{dg} is smaller initially and has a smaller voltage coefficient. The negative feedback provided by R_k mitigates changes in C_{sg} . The result is improved frequency immunity to operating voltage changes.

In any oscillator, the AC loop gain must be greater than one if oscillations are to start, but the loop gain must be reduced to exactly one after the oscillations build up. The loop gain is the product of the amplifier gain and the coupling coefficient, C_f , between the collector and

the gate. The coupling coefficient, C_f , can be expressed as:

$$C_f = Z_t / (Z_t + X_{cc})$$

where:

Z_t = the impedance of the tank at parallel resonance (including C_i above)

X_{cc} = the reactance of the coupling capacitance

Z_t is determined by the Q of the resonator and the reactance of L or C. Z_t may be expressed as:

$$Z_t = 6.28 \times f \times Q \times L = Q / (6.28 \times f \times C)$$

where:

f = the frequency in Hertz (10 MHz)

C = the tank capacitance in Farads (25 pF), including C_i

L = the inductance of the coil (10 μ H)

Q = principally, the Q of the coil

When a crystal is used as the resonator, Z_t is on the order of 10^{12} ohms, and the coupling efficient is practically unity.

To oscillate, the gain of the amplifier must be equal to or greater than $1/C_f$. If the gain is greater than $1/C_f$, the amplitude of oscillations will build up until the amplifier either saturates or cuts off. For stable oscillations, the gain of the amplifier must be exactly equal to $1/C_f$.

The amplifier gain is determined by G_m , R_c , and R_k . In conventional oscillations, amplifier gain control is achieved by changing the bias on the amplifier that varies G_m . While this is a convenient method of controlling gain, it comes at the cost of changing the operating point of the amplifier and requires matching the gain control time constant to the resonator Q. The shift in operating voltages compromises performance, and inappropriate bias time constant can even lead to intermittent oscillation. In this oscillator, the gain is controlled by changing R_k in response to changes in power dissipated in R_k —or in effect, output levels. Changes in R_k alter the feedback with minimal change in operating point.

The circuit in **Figure 2** uses an incandescent lamp for R_k . There are two major advantages in using a variable resistor (the lamp) to control the amplifier gain. First, the gain change is accomplished with a quasi passive component and the amplifier's operating point isn't changed. Second, because the operating point of the amplifier doesn't change, the amplifier can be operated in class A with corresponding low distortion. Operating class A also implies that loading on the resonator doesn't change during the cycle. An increase in rms voltage

across the lamp, which acts as R_k , causes its resistance to increase and reduces R_c/R_k , which reduces the amplifier's gain. A drop in voltage across the lamp causes R_k to decrease. This, in turn, increases R_c/R_k and the amplifier's gain.

The nominal value of R_k and the output voltage of the oscillator relates to the lamps that are available. A lamp's voltage/current relationship is generally given as:

$$I_{spec}/I_{op} = (V_{spec}/V_{op})^{0.55}$$

where:

I_{spec} = the manufacturer's specified nominal current at the specified voltage

I_{op} = the current at the operating voltage, V_{op}

The resistance of the lamp at the operating voltage can be obtained by manipulating this equation to produce:

$$R_{op} = (V_{op}/I_{des}) \times (V_{des}/V_{op})^{0.55}$$

The number 1819 lamp is a reasonable, usually available lamp choice. The 1819 is specified at 28 volts and 0.04 amps, which represents a resistance of 700 ohms. However, when the voltage is reduced to 1.5 volts, the current is 8 mA and the operating resistance, R_{op} , is 188 ohms. Under the operating conditions in the oscillator, the voltage across the lamp is DC with the RF voltage superimposed. The effective, or rms, values will be greater than the average (DC) value. For example, when the DC voltage is 1.5 volts and the RF voltage is 1.0 V_p , the rms voltage is calculated to be 1.66 volts.

The published characteristics of a JFET may provide a rough guide in selecting a JFET type, but more exact values are needed for a specific design. The necessary parameters* can be obtained empirically using simple instruments. For example, a multimeter, a 6-volt battery, and a 22-ohm resistor are all that are required to determine the needed parameters. For an N-channel JFET, the drain is connected to the positive side of the battery, the gate is connected to the negative side, and the 22-k resistor is connected between the source and the negative side. Measure the drain current, I_D , and the voltage across the resistor, V_{gs} . To find I_{DSS} , short the resistor and measure drain current I_{DSS} . With I_D , I_{DSS} , and V_{gs} known, the values of V_{off} , and G_{fs} can be computed for any particular value of I_D . According to Evans in "Designing With Field Effect Transistors," the forward transconductance, G_{fs} , is related to other parameters as:

$$G_{fs} = (2 \times I_{DSS}/V_{off}) \times (1 - V_{gs}/V_{off})$$

*These DC measurements may not reflect the high-frequency performance.

where:

I_{DSS} = drain current with gate shorted to the source

V_{off} = gate-to-source voltage needed to reduce drain current to zero

V_{gs} = voltage gain to source

and

$$I_D/I_{DSS} = (1 - V_{gs}/V_{off})^2$$

$$V_{off} = V_{gs}/[1 - (I_D/I_{DSS})^{0.5}]$$

G_{fs} can also be stated as:

$$G_{fs} = 2 \times I_D / (V_{off} - V_{gs})$$

The data sheet for the 2N5457 shows these typical values:

$$I_{DSS} = 3 \text{ mA}$$

$$I_D = 0.1 \text{ mA at } V_{gs} = 2.5 \text{ volts}$$

Based on these values, the value for V_{off} is calculated to be:

$$V_{off} = 2.5 / [1 - (0.1 \text{ mA} / 3 \text{ mA})^{0.5}] = 3.06 \text{ volts}$$

A similar process can yield the h_{FE} of a PNP BJT. First, connect the emitter to the positive

side of the battery. Then connect the collector to the negative side, and a potentiometer between the emitter and the collector. Now, connect the arm to the base. Adjust the pot for the desired collector current, approximately 10 mA.

Measure base current, I_b , and calculate h_{FE} :

$$h_{FE} = I_c / I_b$$

The data sheet for the 2N3906 specifies a typical $h_{FE} = 100$ at I_c , or approximately 10 mA.

The design of the 10-MHz oscillator shown in **Figure 2** is straightforward after the active devices have been selected. In the following example, the typical values provided in the data sheets are used. V_{off} is calculated to be 3.06 volts and the FET should be operated with $V_{gs} = V_{off}/2$, $V_{gs} = 1.5$ volts, for highest power output with low distortion.

The oscillator shown in **Figure 2** uses a 2N5457 JFET, a 2N3906 BJT, and a no. 1819 incandescent lamp. The FET typical values are: $I_{DSS} = 3$ mA, $V_{off} = 3.05$ volts. The BJT is specified to have $h_{FE} = 100$ at 10 mA of collector current.

The design steps are as follows:



1. Calculate I_D at $V_{gs} = 1.5$ volts: $I_D = I_{DSS} \times (1 - V_{gs}/V_{off})^2 = 0.78 \text{ mA}$
2. Calculate G_{fs} at $I_D = 0.78 \text{ mA}$: $G_{fs} = 2I_D / (V_{off} - V_{gs}) = 1.00 \times 10^{-3} \text{ S}$
3. Calculate the lamp operating voltage, V_{op} , assuming $V_{pk} = 1$ volt, $V_{DC} = 1.5$ volts. $V_{rms} = 1.66$ volts
4. Calculate the lamp resistance when $V_{op} = 1.66$ volts: $R_{lamp} = V_{op} / I_{spec} \times (V_{spec} / V_{op})^{0.55} = 196 \text{ ohms}$
5. Calculate lamp operating conditions: $I_{op} = I_{ck} + I_D$, where I_{ck} is the portion of I_c flowing in the lamp. Given $R_k = 196$ and $V_{op} = 1.66$: $I_{ck} = V_{op} / R_k = 8.47 \text{ mA}$. $I_{op} = I_{ck} + I_D = 8.47 \text{ mA} + 0.78 \text{ mA} = 9.25 \text{ mA}$
6. Determine I_c given $h_{FE} = 100$ and assumed $I_{load} = 3.5 \text{ mA}$: $I_c = I_{ck} + I_{load} = 9.25 \text{ mA} + 0.78 \text{ mA} = 12.8 \text{ mA}$
7. Calculate I_b needed to produce $I_c = 12.8 \text{ mA}$: $I_b = I_c / h_{FE} = 0.128 \text{ mA}$
8. Assume a desirable value of $E_e = 1.11$ volts. Calculate R_e for the required $E_e = 1.11$ volts:
 $R_e = 1.11 \text{ volts} / 12.8 \text{ mA} = 87 \text{ ohms}$
9. Calculate base input resistance, R_b : $R_b = h_{FE} \times R_e = 8700 \text{ ohms}$
10. Calculate R_D to produce required I_B for an assumed base/emitter voltage, $V_{BE} = 0.6$ volts
 $R_D = (E_e + V_{BE}) / (I_D - I_B) = 1.71 \text{ volts} / 0.652 \text{ mA} = 2.62 \text{ k}$
11. Calculate the effective $h_{FE} = h_{eff}$: $h_{eff} = I_c / I_D = 12.8 \text{ mA} / 0.78 \text{ mA} = 16.4$
12. Calculate G_m and $V_{G_{sf}}$: $G_m = G_{fs} \times h_{eff} = 1.0 \times 10^{-3} \times 16.4 = 16.4 \times 10^{-3}$,
 $V_{G_{sf}} = G_m \times R_k / (G_m R_k + 1)$ $V_{G_{sf}} = 0.762$
13. Calculate C_f : $C_f = Z_f / (Z_f + X_{cc}) \approx 25.4 / (25.4 + 15.9) = 0.615$
14. Calculate required amplifier gain, V_{G_a} : $V_{G_a} = 1 / C_f = 1 / 0.615 = 1.63$
15. Calculate R_c : $V_{G_a} / V_{G_{sf}} = 2.14 = (R_c / R_k) + 1$
 $R_c = (2.14 - 1) \times 196 = 223 \text{ ohms}$
16. Calculate RF voltage at the collector: $e_c = V_{kpk} \times (R_c / R_k + 1)$, where V_{kpk} is the peak RF voltage across R_k . $1.0 \text{ volt } e_c = 1.0 V_{kpk} \times 2.14 = 2.14 V_p = 1.51 V_{rms}$
17. Calculate the load resistance with the assumed $I_L = 3.5 \text{ mA}$: $R_L = E_L / I_L = 1.51 / 0.0035 = 431 \text{ ohms}$
18. Calculate the power in the load: $P_L = I_L \times E_L = 3.5 \text{ mA} \times 1.51 \text{ volts} = 5.3 \text{ mW}$

To resonate with 25 pF (22 pF fixed plus 3 pF FET gate capacitance) at 10 MHz requires an inductance of 10.1 μ H. An inductor of this value can be purchased or wound at home. While it's beyond the scope of this article to present the development of stable inductors or temperature compensation of resonant circuits, suffice it to say that the inductance of a coil varies with temperature as a result of changes in dimensions with temperature and changes in current distribution in the wire. Optimum stability will be obtained with a single layer air-cored wound on a ceramic, quartz, or glass form. It should be noted that inductors wound with copper wire don't normally have a retraceable temperature coefficient. That is, the inductance won't return to the same inductance after heating or cooling because the dimensions will be minutely different. This lack of retraceability presents severe problems in precise temperature compensation with capacitors. Inductance variations of several parts per million per $^{\circ}$ C are common with normal coil construction techniques. However, a glass or ceramic form is dimensionally stable and a winding with the wire under tension will conform to the coil form. Coating with Q-dope will also help hold the turn spacing. For a first-cut 10 μ H coil, 28 turns of no. 22 enameled wire close wound on a 1.75-inch diameter form will be in the ballpark.

This oscillator is pretty close to a "throw together" circuit. The design is straightforward and doesn't require demanding operating voltages or depend on critical parts except in the tank circuit and C_{cc} . The components shown in **Figure 2** are the nearest 5 percent parts, so tolerances may accumulate and require some minor tweaking. There's no mystery to making the tweaks: DC conditions can be checked by

shorting the FET gate to ground and measuring the DC voltage across the lamp. The voltage across the lamp can be increased by increasing R_D . When the lamp voltage is 1.5 volts, remove the short on the gate and the circuit should oscillate. If the circuit doesn't oscillate, the value of C_{cc} is too small for the actual tank Q. More C_{cc} than necessary will be provided by 0.25 inch of insulated wire twisted together. Trim the gimmick so the RF voltage at the output is about 1.5 volts. A tighter twist or longer length will increase the RF output. The gimmick isn't mechanically stable, so a dab of Q dope or clear glue (Duco Cement) will be needed to hold the gimmick's shape.

Note that, in general, oscillators designed with excessive positive feedback have lower noise, but poorer frequency stability than oscillators with minimum positive feedback. Weakly oscillating circuits with minimum positive feedback may not have enough excess gain at "turn on" to start reliably and may require a shock of voltage to get started. As a result, weakly oscillating circuits generally oscillate on frequency, or they don't oscillate at all. Also, the voltage feedback may not be very large compared to the internal thermal noise and consequently cannot suppress the internal noise. This results in an oscillator output with high noise. The design presented here overcomes many of these compromises because of the large range of feedback control offered by the lamp used for R_k .

The FET/BJT hybrid amplifier with an incandescent lamp for the source resistance makes a very versatile circuit. It offers automatic adaptive biasing that maintains an essentially constant output level. Because the lamp is operated at very low voltage, its life expectancy is similar to that of the transistors or resistors. ■

PRODUCT INFORMATION

New Mobile Transceiver from Standard

Standard Radio's new C5900DA is a dual display FM mobile transceiver with back-lit microphone and display that covers 50, 145 and 440 MHz bands. The radio comes with 160 memories, 80 each side, and can be upgraded to 400, 200 each side, with an accessory memory chip CMU161. The memory chip can also be used to up and down load the 160 memories to another C5900DA. Seven Hyper memories are provided, in addition to the normal memories, for quick selection of most used frequencies. The transceiver also features a snap-off front panel that permits mounting the radio in

the trunk or under the front seat. Another feature of the C5900DA is the ability to DTMF control the radio from an HT. The CTCSS encode/decode board is built in, and DTMF allows auto-dialing with 12 memories, six per side. Other features include a programmable TX time-out timer, auto power-off, and automatic opposite band mute. Power output is 45W on 6, 50W on 2, and 35W on 70 cm, 3W and 10W selectable.

For more information, contact Standard Radio at P.O. Box 48480, Niles, IL 60714; phone 312-763-0081; fax 312-763-3377; or on the World Wide Web at <http://www.stdradio.com>.

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Antennae Exotica—Genetics Breeds Better Antennas

By Nathan “Chip” Cohen, N1IR

2 LedgeWood Place
Belmont, MA 02178

Summary: Applying Darwinian “natural selection” to the concept of antenna design optimization. Using a genetic algorithm, software antenna models can be refined to the point where less desirable characteristics are reduced or eliminated.

Fall 1996, pages 55-60.

Please contact the author for additional information.

FROM A J TO A ZEPP

The truth and its consequences

After weeks of reading the mail on area repeaters, I noticed discussions frequently turned to J-poles. A number of J-pole design variations circulated (copper tubing, 450-ohm ladder line, TV twin-lead, etc.), and each stressed the need for careful measurement. It seemed a mystique was associated with tuning these antennas.

Research

I decided to research the subject and began by analyzing a known design. The J-pole's reputation has taken a beating as hams have attempted to construct models from 300-ohm TV twin-lead. Many are convinced that a match of 1.5:1 or better is impossible and recommend 450-ohm ladder line. Even successful experimenters think TV twin-lead designs can't be easily reproduced. Nevertheless, many have built J-poles from TV twin-lead for a number of excellent reasons.

The end game

A half-wave center-fed dipole appears as a low impedance (approximately 73 ohms), easily matched to commercial coaxial transmission lines with characteristic impedances of 50 to 75 ohms. If antenna length is increased beyond a half wavelength, the feedpoint impedance also increases. This trend continues as the length approaches a full wavelength. If the conductor were infinitely thin, the impedance would rise to infinity. The impedance is lower (on the order of 3500 ohms for 12 gauge wire at 146 MHz) for reasonable conductor sizes of 0.001 wavelengths in diameter. This is well-illustrated in Chapter 20 of *The Radio Handbook* in a graph of impedance versus wavelength with respect to conductor size.¹

If we relate this to the J-pole, the center-fed full-wavelength dipole can be viewed as a pair

of half-wave dipoles fed in phase at the ends. Considering the wire gauge used (20 gauge) in the manufacture of TV twin-lead, we might anticipate that the J-pole's end-fed dipole will exhibit a feedpoint impedance somewhat greater than 3500 ohms, but less than infinity.

I haven't found quantitative works on the feedpoint impedance of an end-fed radiator, other than the feedpoint impedance of a ground-mounted vertical.² Here, the impedance appears to be approximately half that of a center-fed dipole. Assuming this is also true for an end-fed vertical mounted above ground, we might anticipate the impedance of an end-fed dipole to be greater than 1750 ohms.

I ran an ELNEC³ simulation of an end-fed vertical dipole to check my prediction. I varied wire size and height above ground and observed the changes. The results appeared to vary slightly around 7000 ohms.

Using dimensions from a 450-ohm ladder-line design described by Lew McCoy, W1ICP, in the July 1994 issue of *CQ* magazine,⁴ I performed a source-to-load evaluation to obtain an estimate of the load impedance he saw. It was around 5000 ohms. I assumed a perfect match at 146 MHz (mid-band) and a velocity factor of 0.88 for the 450-ohm ladder-line Lew used in his design.

I chose 5000 ohms as the target feedpoint impedance for my analysis and design. I figured this value should be achievable based on my analysis of W1ICP's design. I reasoned that if 5000 ohms wasn't quite right, I could compensate by shortening the length of the half-wave dipole element slightly.

Choosing 7000-ohms would put the design at risk if I were unable to achieve the higher value in practice. I made a number of assumptions when evaluating W1ICP's design. The 5000-ohm value appeared a reasonable expectation for the load impedance, allowing some margin of error during construction.

This exercise established that the J-pole was

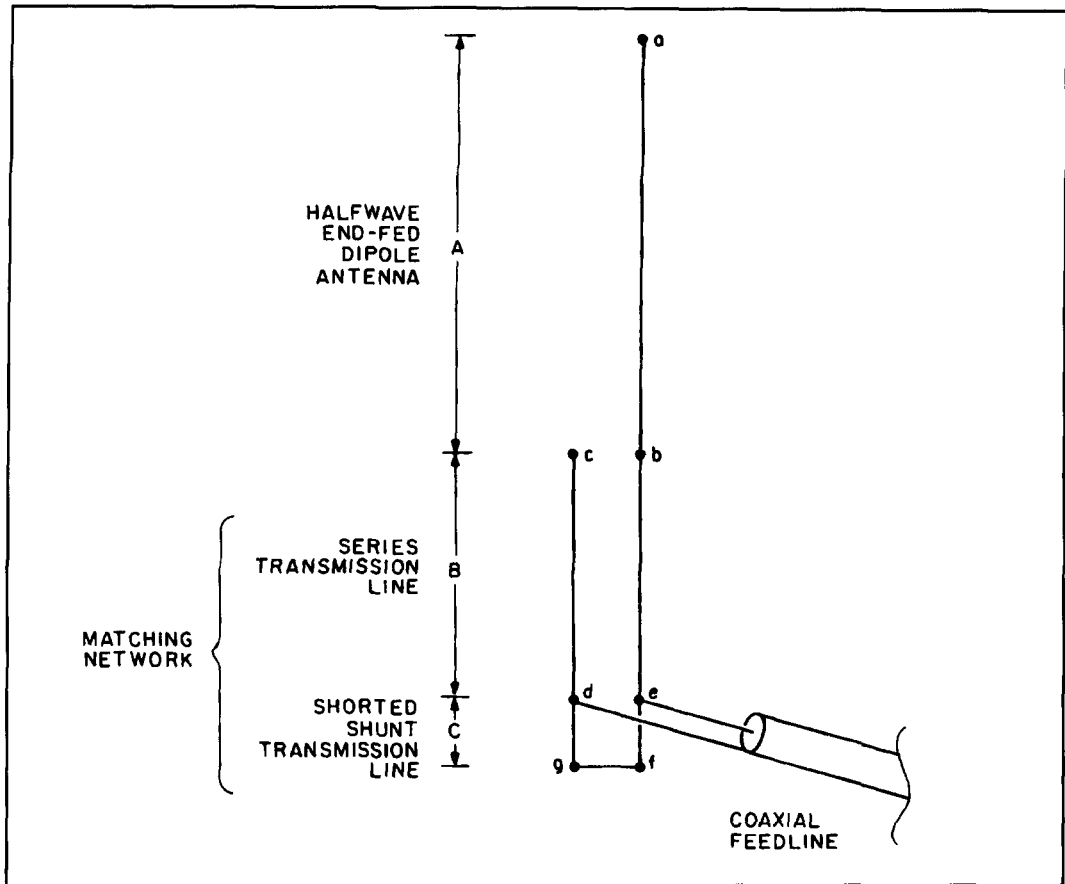


Figure 1. The three components of a J-pole: (A), series transmission line (B), and shunt transmission line (C). The component sections are on the left, the J-pole is on the right.

an end-fed half-wave dipole with a very high feedpoint impedance. I could now move ahead and match this impedance to a 50-ohm feedline.

Gotta match?

Transmission line matching is predictable, repeatable, and practical at VHF and UHF frequencies. Yet this aspect of the J-pole is the least understood, as evidenced by the universal technique of tuning by “adjusting the tap.” The myth that J-poles require great care during building and tuning likely has its roots here.

Transmission line theory: bridging the gap

Quarter wavelength sections of transmission line are common circuit elements for matching. They effectively convert open circuits to short circuits, and vice versa. This is the result of standing waves created by the termination of any transmission line of arbitrary impedance in a short or open circuit at exactly 90 electrical degrees along its length.

There are a number of texts that cover the properties of transmission lines in detail.^{5,6,7} Here, however, I’ll review only that behavior relevant to the J-pole.

Doing it the hard way

The objective is to produce a near open circuit (i.e., a high impedance) at the frequency where the end-fed dipole is a half wavelength. Do this, and the antenna will be matched. A short at one end of a quarter-wave section of transmission line appears as an open circuit (high impedance) at the opposite end. This means a shorted quarter-wave transmission line may be used to match the high feedpoint impedance of an end-fed dipole. Once this is done, the feedline must be attached at an appropriate point along the line to produce a match to the characteristic impedance of that line (50 ohms for RG-58).

Let’s get real

Let’s look at how the J-pole is constructed from a slightly different perspective. We can do

this with respect to the source or the load. It's easier to start from the load and work back to the source, which aligns with the design approach presented here.

We'll begin with load assumptions. At this point, all we need to know is that the load impedance is nonreactive and 5000 ohms. Maximum current flows in nonreactive circuits, implying a pure resistance. This repeats periodically at half wavelength intervals along any conductor of arbitrary length, whether or not it's intended to be a radiator.

Select a transmission line for matching the antenna to the feedline. (I prefer 300-ohm TV twin-lead.) The goal is to match the antenna to an impedance of $50+j0$ ohms. By expressing the impedance in cartesian form, we can work with real and imaginary components independently.

Enter the Smith chart

The Smith chart is an invaluable tool for performing transmission line calculations. For more information on its use, see **References 8 and 9**.

In **Figure 1**, the half-wave end-fed dipole, section (a,b), has a dimension of (A). The bottom of this section (b) is the antenna feedpoint, with a terminal impedance of $5000+j0$ ohms.

The dipole end is connected to one terminal (b) of the transmission line matching section (B). This may seem awkward, but terminal (c) is 180 degrees out-of-phase with terminal (b) and serves as a virtual return to properly terminate the transmission line matching section.

At interface (b,c) in **Figure 1**, we're attempting to terminate a 300-ohm transmission line into 5000 ohms—a mismatch of 16.67:1.

The Smith chart is normalized to 300 ohms (**Figure 2**) to permit graphing of 300-ohm transmission line elements. Dividing the real and imaginary components of the impedances we wish to work with by 300, yields the coordinates on the normalized chart. Conversely, both the real and imaginary components of any coordinate pair read off the chart must be multiplied by 300 to obtain the actual impedance.

Begin by plotting the nonreactive source and load impedances on the $j0$ axis (the horizontal line crossing the center of the chart). The 5000-ohm load is normalized and plotted in **Figure 2** as $(16.67+j0)$. The source is referenced at the end of the feedline where it connects to the J-pole; i.e., (d,e) in **Figure 1**. The business end of the feedline is driven by a transmitter with a 50-ohm source impedance. It's necessary to terminate both ends of the feedline at its characteristic impedance for maximum power transfer from source (transmitter) to load (antenna.)

The antenna feedpoint, which when matched exactly equals the feedline impedance at this

point, is normalized and plotted in **Figure 2** as the equation $0.167+j0$.

We want to use 300-ohm transmission line to transform the load impedance from 5000 to 50 ohms. A process called navigating around the Smith chart provides a path that connects the load to the source. All operations follow contour lines to move from point to point. Lines of constant VSWR are described by circles centered on the chart, with a radius that represents the VSWR (equivalently expressed as reflection coefficient). These contour lines, constructed only when needed (using a compass), are normally omitted from the chart.

Returning to **Figure 1**, we see that a section of 300-ohm transmission line (b,c,d,e) is series-connected between the load (dipole) and the source (feedline). Because the length is physically short, we assume it to be lossless; we need only consider how the reactance of the load appears as it's observed along the length of the line. Specifically, we must look at the connection to the coaxial feedline or "tap"—identified as (d,e) in **Figure 1**.

The contour representing the change is a circle centered on the chart with a radius equal to the load mismatch. The VSWR value of 16.67 defines the radius of the circle drawn in **Figure 2**.

In **Figure 1**, another section of 300-ohm transmission line (d,e,f,g) is connected across the feedline (d,e) and shorted at the opposite end (f,g). A section of transmission line shorter than a quarter wavelength is used to simulate a shunt inductor. Its inductance (and, therefore, its reactance) increases with increasing length. More precisely, its inductive susceptance decreases with increasing length. Beyond a quarter wavelength, it appears capacitive. We now have a slightly different problem.

Figure 2 is an impedance plot and the lines of reactance represent contour paths of series-connected, rather than shunt or parallel-connected, components. A minor adjustment to the Smith chart shows how easily the J-pole is matched.

Figure 3A represents admittance, the reciprocal of impedance. Now, the Smith chart is quite literally turned upside down. All numerical values change to become the reciprocal of their impedance counterparts. Even the terminology changes. The reciprocal of resistance is conductance; the reciprocal of reactance is susceptance, and the units are in mhos.

The conversion process involves rotating the impedance chart 180 degrees while leaving the coordinate positions unchanged (i.e., an open circuit remains to the right and a short to the left). Because flipping the chart also moves the plotted coordinates, they must be replotted.

The trick is to place a compass at the center of the chart, extend the compass to each point,

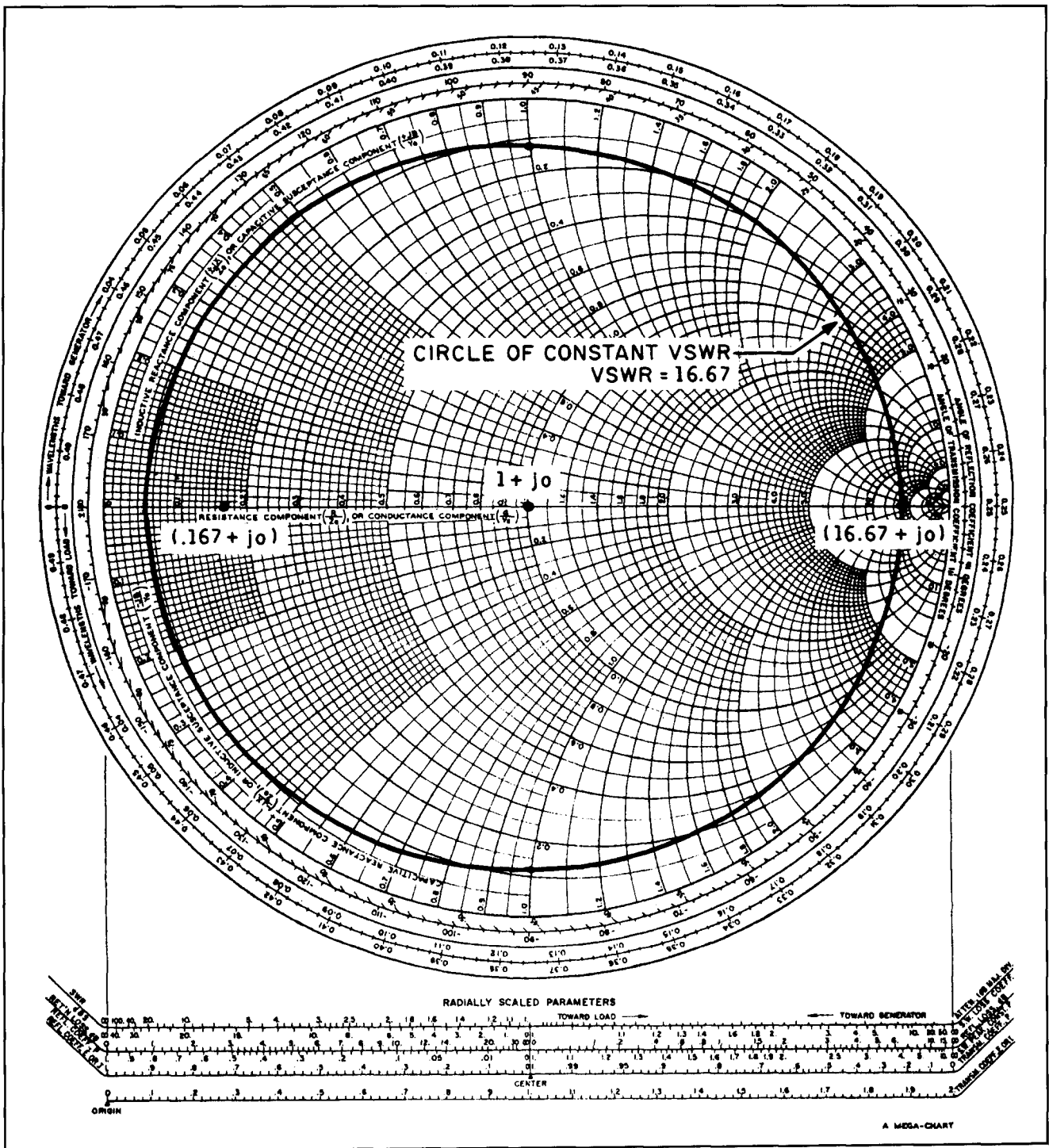


Figure 2. Smith chart normalized to 300 ohms, with plot of J-pole VSWR contour of 16.67 to 1 and normalized 50-ohm source impedance at $0.167 + j0$.

then locate and mark the points at the exact distance but diametrically opposite the center. The plotted coordinates will then appear in the same orientation on both charts (Figures 2 and 3A).

The result in Figure 3A is now in normalized units of mhos. Because we were working with a chart normalized to 300 ohms, the admittance chart becomes normalized to $1/300$ or 3.33 millimhos ($0.003 + j0$ mhos).

The circle of constant VSWR is unchanged by the conversion from impedance to admittance coordinates and is again drawn in Figure 3A.

The mystery solved

With the load and source identified on an admittance chart, two operations disclose how a match is achieved for the J-pole.

The effect of the shorted transmission line section, plotted as an inductive susceptance, must trace a line of constant conductance equal to the conductance of the source. The locus of points that describe the line of constant conductance equal to the conductance of the feedline is shown in **Figure 3A**. This locus and the constant VSWR circle intersect at two points. The necessary condition for matching to the real axis with a shorted stub requires that these two lines intersect in the $-j$ region. An open stub (capacitive susceptance) will match an impedance in the $+j$ region to the real axis.

Moving along the transmission line (**Figure 1**, points b,c,d,e), away from the load (dipole) and toward the feedline, the admittance follows the circle of constant VSWR (**Figure 3A**) clockwise until it intercepts the line of constant conductance at $6-j7.96$ where the feedline is connected (**Figure 1**, points d,e).

The resultant capacitive susceptance must be canceled by an inductive susceptance equal in magnitude to achieve a pure resistance (reactance free) match to the feedline.

A shorted length of 300-ohm transmission line (**Figure 1**, points d,e,f,g) provides the inductive susceptance required to complete the match. It's that simple!

Figure 3B clarifies the two maneuvers. Y_{ant} represents the load (antenna) admittance. Y_f represents the feedline admittance.

A J-pole constructed using the computed dimensions will accurately define the correct position of the "tap," making adjustments about this point inappropriate.

It's extremely important to know the velocity factor of the transmission line used for the matching elements to determine the series and shunt transmission line segment lengths.

Revelation one

If the length of the series section of transmission line is added to that of the shorted stub, the sum is greater than an electrical quarter wavelength. It's commonly believed that the J-pole is matched with a tapped quarter-wave matching stub.

Revelation two

Using the analysis method given, we see that VHF/UHF J-poles are more easily matched with 300-ohm TV twin-lead than with higher impedance open-wire ladder lines.

Figure 4, normalized for 600-ohm transmission line, shows a plotted constant VSWR contour (VSWR = 8.33) for the same dipole (0.12 mhos normalized), and a locus of constant conductance for 50-ohm feedline (12 mhos nor-

malized). Note that the contours fail to intersect. In this situation, the antenna can't be matched using the simple network described. Popular opinion supports the contradictory notion of "the higher the impedance the better."

The maximum impedance, the place where the two lines intersect, is found by computing the square root of the product of the feedline and antenna feedpoint impedances (500 ohms in this case.) A quarter wavelength of 500-ohm transmission line would precisely match 5000 ohms without a stub of any length (shorted or otherwise).

J-poles fabricated from open wire, 450-ohm transmission line appear to be favored over 300 ohm twin-lead. For the 300-ohm case presented, I assumed a load impedance of 5000 ohms (based on W1ICP's design). Analysis based on 450-ohm transmission line demonstrates that it's not as forgiving of errors. For example, if the actual antenna impedance is less than 4000 ohms, the contour pair won't intersect and matching won't be straightforward. Actual antenna impedance would need to fall below 1800 ohms to create a condition not easily matched with 300-ohm twin-lead. Therefore, the choice of 300 ohms provides a greater margin of error than higher impedances. If the actual antenna impedance were significantly greater than 5000 ohms, the margin of error would improve in both cases with 300 ohms maintaining the greater margin.

More research is needed to accurately quantify the feedpoint impedance for various lengths and gauges of wire and tubing configured as end-fed radiators. Although it's clear that 300 ohm twin-lead is superior to higher impedance lines, the results aren't sufficient to draw conclusions on the accuracy of the assumed antenna feedpoint impedance.

By "adjusting the tap," the center conductor of the feedline could attach to the matching section at a slightly different height (higher or lower on the matching section) than the braid (shield). This procedure, along with some adjustment of the antenna length, would introduce a third transmission line section in the model (by virtue of its lack of symmetry). Perhaps, in this way, one can compensate by introducing a small (but significant) shunt resistance to achieve a match. This would introduce loss and reduce antenna efficiency, but not dramatically. If this is how high-impedance ladder lines are made to work, the adjustment of the "tap" would be critical.

I suspect ladder line is favored for its physical attributes. J-pole designs dictate adjustment of the tap to obtain good VSWR. This trial and error process is easily accomplished in the open wire segments of ladder line.

The solid dielectric along the length of twin-

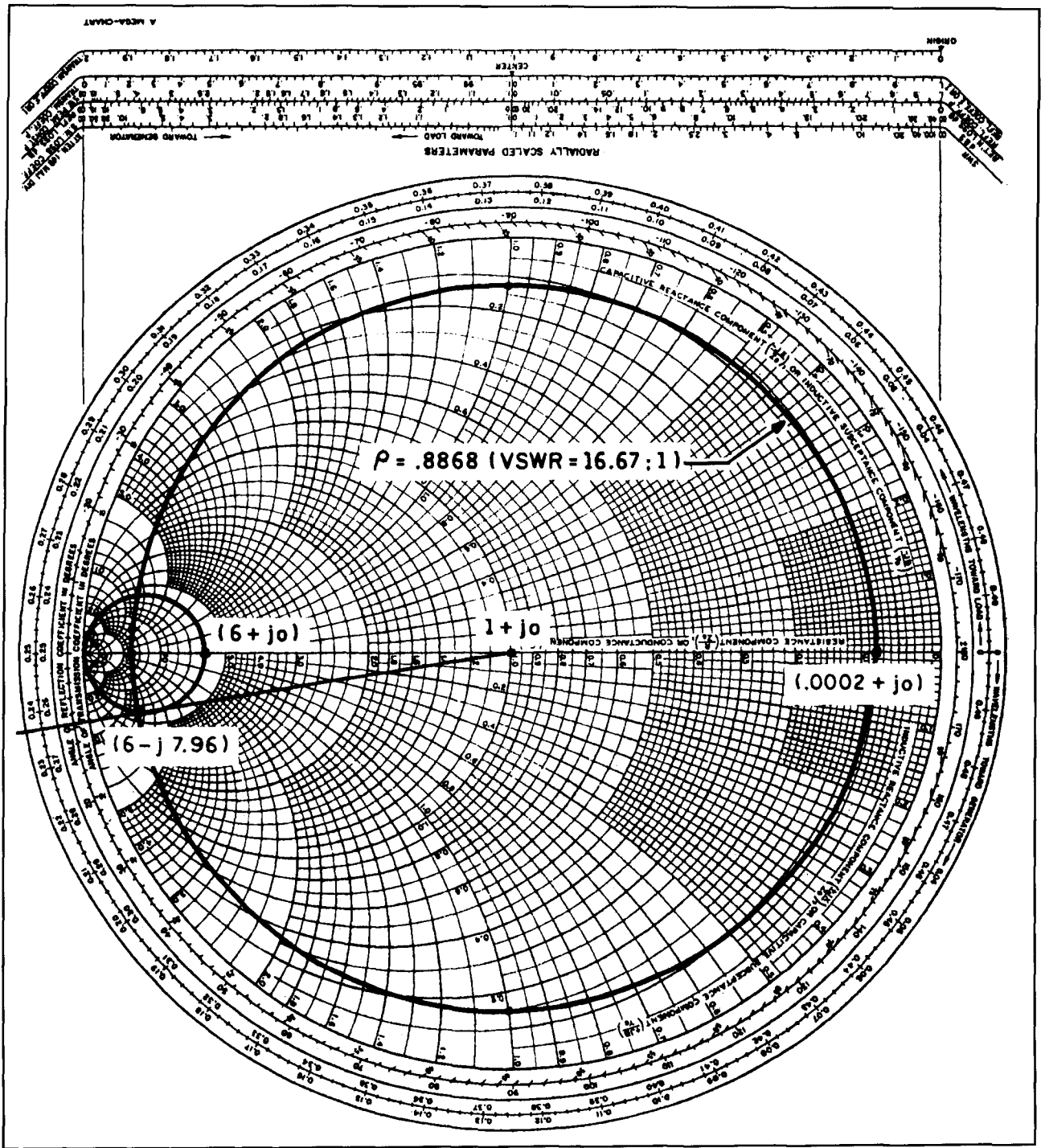


Figure 3. (A) Smith chart of Figure 2 in terms of normalized admittance (the reciprocal of impedance), with the source conductance contour ($6+j0$) added.

lead makes it difficult to adjust the feedline tap. It's also difficult to perform many iterations before it begins to look ugly.

Revelation three: 6:1

To answer questions about the impedance of J-poles designed with tubing materials, I select-

ed a few designs to determine the J-pole's "stub" impedance. In every case, the spacing-to-diameter ratio was between 2.4 and 3.0—placing the impedance of the transmission line sections at 188 to 214 ohms, respectively. Larger diameter elements (tubing versus wire) result in lower feedpoint impedances as well, perhaps below 5000 ohms.

By varying the diameter of the constant

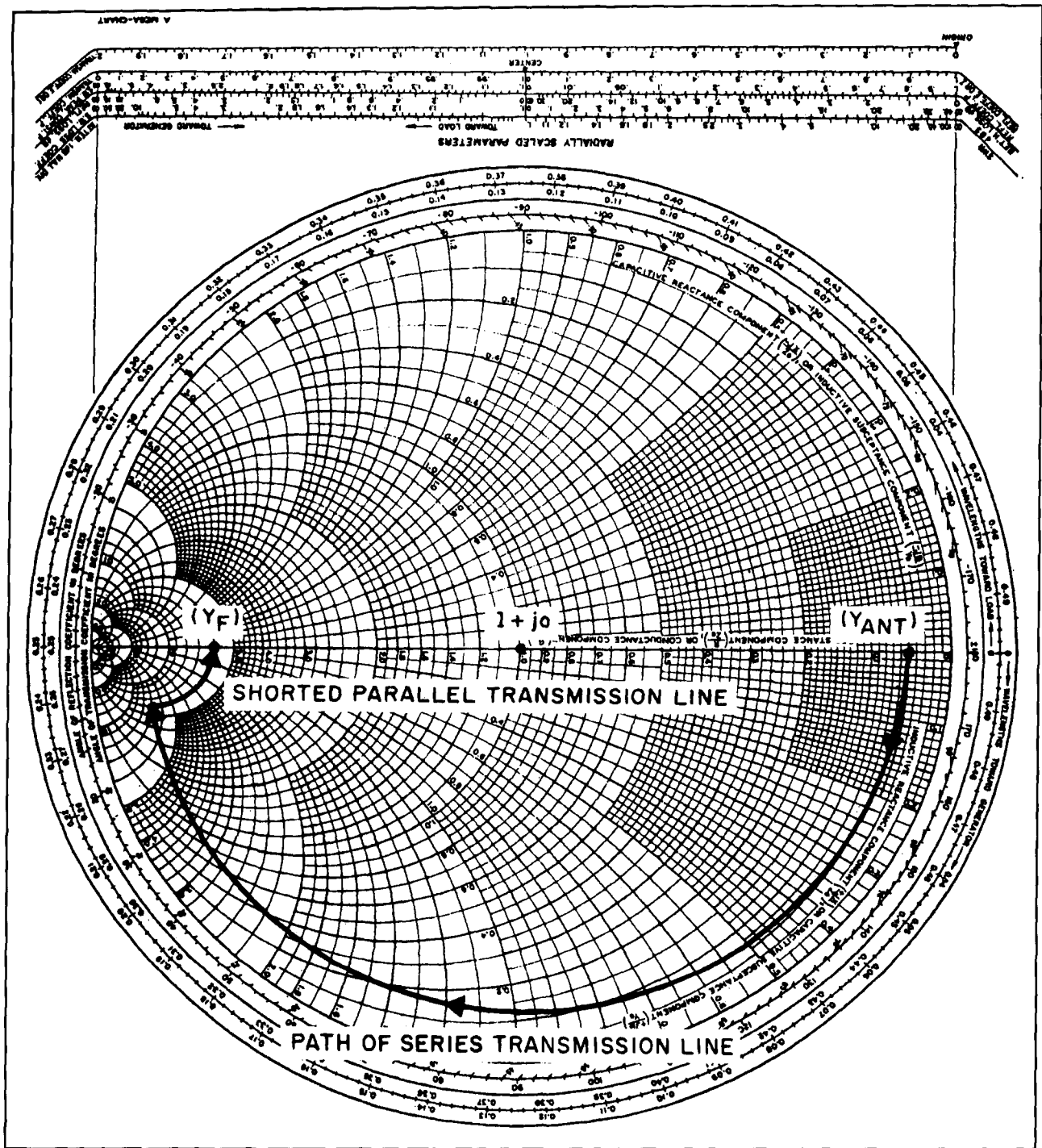


Figure 3(B). Contours representing the maneuvers required to match a J-pole.

VSWR circle, I was able to illustrate the effect caused by increasing or decreasing the antenna load impedance assumption.

The optimum transmission line for matching 5000 ohms to 50 ohms appears to be about 300 ohms. This is illustrated by plotting the contours in Figure 3A for normalized values of 200 and 450 ohms. A radial drawn tangent to the contour of constant conductance (equal to

the feedline conductance) is tangent at a point very close to the intersection of the VSWR contour. If 200-ohm transmission line were used, the contour lines would intersect more to the left. For 450-ohm transmission line, the intersection would occur more to the right.

Errors in assumed antenna feedpoint impedance (change in diameter of VSWR circle) result in little change to the computed length of

the top matching section. A good match is nearly guaranteed, with the risk of a slight VSWR degradation caused by the bottom section length error.

For 200 ohms, the length of the top section is more critical; for 450-ohms, the length of the lower section is more critical. Interestingly enough, the total overall length doesn't change significantly for either case, given that both have equivalent velocity factors. It's likely this attribute leads to the success of the iterative "tap" adjustment. The adjustment becomes increasingly critical with a rise in transmission line impedance.

Conductors of 300-ohm parallel transmission lines with a 6:1 spacing-to-diameter ratio in air would seem to be optimal for tubing versions of the J-pole—although this is not observed. Smaller ratios reduce the characteristic impedance of the transmission line and may be arbitrary to some extent to match 5000 ohms to 50 ohms. Closer spacings simplify fabrication; the trade-off is a reduction in ease of adjustment. Three-hundred-ohm transmission lines simply yield designs that are easier to tune.

The closer spacing afforded by lower impedance transmission lines provides tighter coupling between the parallel conductors and less radiation. This supports their direct connection to coaxial cable feedlines without introducing a balun.

Revelation four

To adjust the J-pole, simply tune the dipole element to resonance. This is the same procedure used to tune center-fed dipoles, inverted vees, verticals, etc. You can choose whether to adjust the tap or vary the length of the dipole element. Both operations are easily performed on designs constructed from tubing. The latter is simpler and more precise on designs using twin-lead or ladder line and, thus, is the recommended procedure.

Revelation five: the closer it gets, the better it looks

Parallel transmission lines properly terminated in their characteristic impedance, efficiently transfer power and suffer minimal radiation loss. They are balanced because fields created by current propagating out one of the conductors are matched by fields created by the return current propagating in on the adjacent conductor. Both are referenced to, and therefore balanced against, a common (earth) ground return.

As the conductors get closer together, the opposing fields cancel more effectively, and the

transmission line radiates minimally. To achieve this: 1) lower the frequency in which the transmission line is used (i.e., a given physical spacing is a proportionally smaller electrical distance); or 2) decrease the physical spacing of the parallel conductors.

Total field cancellation is purely theoretical. To cancel completely, the parallel conductors would need to occupy the same space.

An obvious benefit of 300-ohm twin-lead over higher impedance ladder lines is that the former radiates less at any given operating frequency due to its closer conductor spacing. The feedline is therefore less susceptible to RF currents induced by the fields surrounding the twin-lead. If used in a properly designed and matched network, the chances for unwanted feedline currents are further suppressed. It appears that TV twin-lead is an optimal choice.

A balancing act

The J-pole is designed with a balanced feed. Coaxial cable is unbalanced in that the field surrounding the center conductor (used as a single wire transmission line) is contained by the shielding properties of the outer braid, which also serves as the ground return reference. It uses the inside surface of the shield as the return signal path. The effectiveness of the shield determines the loss properties of the cable, with poor quality varieties exhibiting severe radiation as well as resistive (heat) losses.

When interfacing balanced and unbalanced transmission lines, there's always some danger that something will go awry. If not matched perfectly, antenna currents will flow along the outside surface of the coax cable's shield, producing "hot spots" along its length. These act as parasitic (power stealing) radiators that generally serve no useful purpose, but can degrade or enhance the antenna's performance (directivity) through destructive or constructive interference. In general, the energy is absorbed or otherwise dissipated. Whether routed through conduit, behind walls, or under carpets, the coax is generally not well positioned to be effective or beneficial as a parasitic radiator.

To cancel these effects, place a balun or a common mode RF choke at the point where the feedline connects to the antenna. These devices electrically isolate the feedline's outer conductor from reflected energy that would otherwise radiate from the feedline.

A purist would certainly use a balun on his J-pole, considered sound engineering practice for any balanced-to-unbalanced transition. However, a good match keeps feedline currents to a minimum. Small currents induced on the feed-

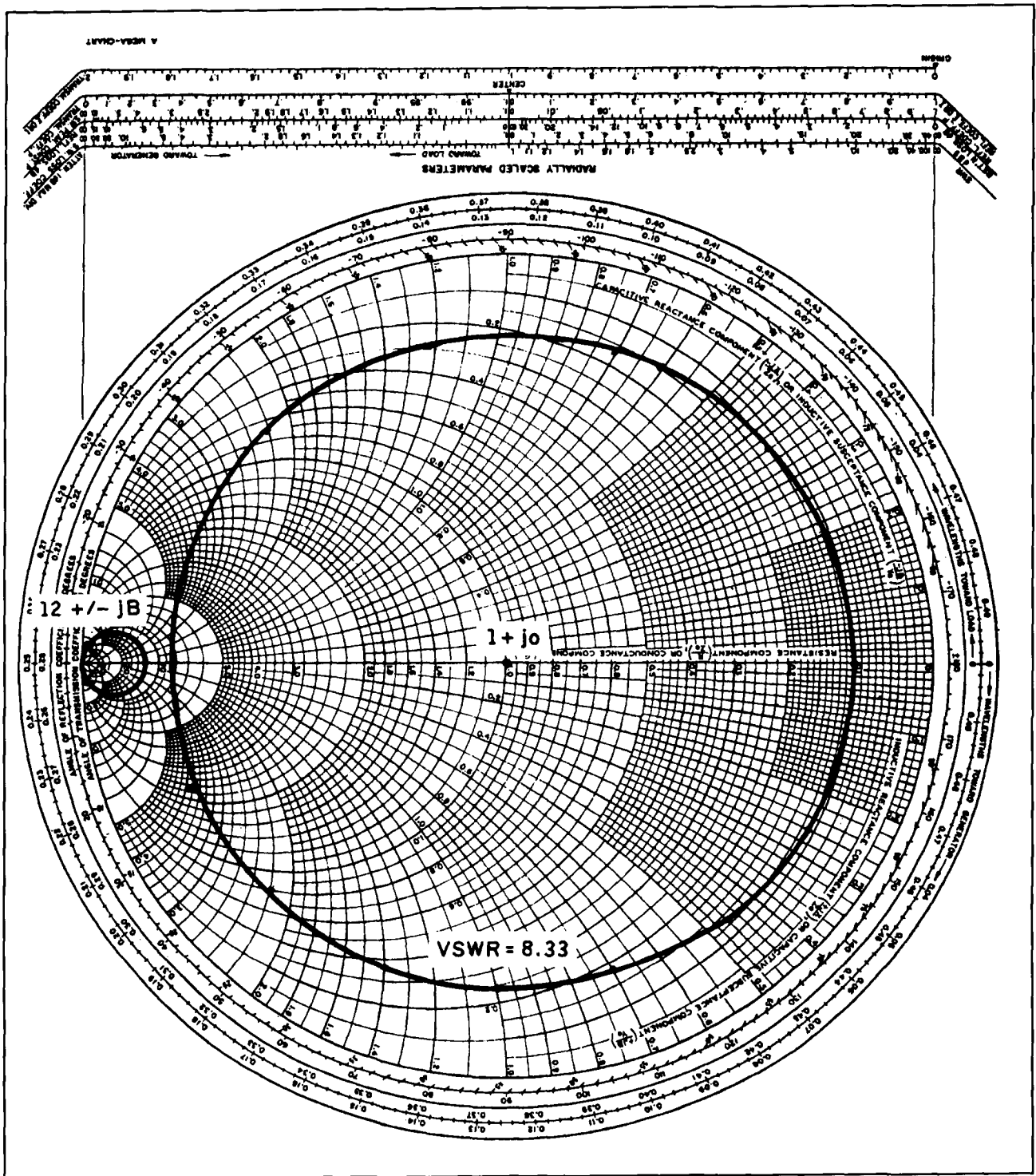


Figure 4. Smith chart with admittances normalized for matching attempt with 600-ohm transmission line.

line are sacrificed as a mismatch loss with little if any pattern distortion. Both effects are negligible. For example, 1.5:1 VSWR produces a mismatch loss that reduces the effective radiated power by less than 0.2 dB (about 4 percent). At 100 percent efficiency, this small amount of

parasitic energy will do little to alter J-pole performance, but could significantly alter the front-to-back ratio or sidelobe rejection of a directive array. Remember, even a well-designed balun introduces loss and adds complexity to the design.

I did experiment with the feedpoint to determine whether it made a difference if the center conductor were connected to the short or long leg of the J-pole. I anticipated a negligible effect. The VSWR changed slightly, but I could net it back with a minor adjustment to the length of the half-wave dipole element. I concluded that this is attributable to my inability to connect the stub at exactly the same points when reversing the connections.

Wandering about the shack in the vicinity of the feedline produced more perceptible VSWR fluctuations with the center conductor connected to the short leg, **Figure 1** (d). Fluctuations were slight when the center conductor was connected to the long leg, **Figure 1** (e). In that configuration, the J-pole appears to exhibit the best behavior with respect to unwanted feedline currents.

Reflected current on the short (unconnected) leg is controlled solely by the accuracy of the matching network construction, which is tightly controlled in the design procedure described. The reflected current on the leg connected to the dipole element is a function of any residual mismatch to the antenna as well, which is also subject to errors in the assumptions. Of course if a balun were used, the antenna feedpoint connections would be on the balanced side of the transformer, and the way in which the J-pole is connected would make no difference.

The same but not equal

It's widely accepted that, because voltage goes to zero in a short circuit, the shorted end of a transmission line is electrically at zero potential, or virtual ground. In theory, voltage goes to zero at a single point at the midpoint of the shorted end of the transmission line. It seems reasonable that this point can be connected to any convenient earth ground reference. This is only true, however, if the shorted section of the transmission line is an exact multiple of a quarter wavelength. In fact, this short is at the electrical (and physical) midpoint of the feed, where the current (and voltage) is phase shifted by 90 degrees. It's best modeled as the centertap of an inductor shunted across the feedline terminals.

Many recommend this for roof- and tower-mounted applications. The J-pole then doubles as a lightning rod and serves as a low impedance shunt of static energy at levels considerably below strike potential during electrical storms. This creates a cone of protection with the tip of the J-pole at the apex; but it's extremely important to maintain a very low impedance connection to an earth ground. Avoid connections to cold water pipes inside

the house, and don't connect dissimilar metals (e.g., copper and aluminum).

As a short circuit across the antenna terminals, the shorted matching stub protects against static discharges via the antenna port if you fail to disconnect your antennas when you finish operating. However, this would be inadequate protection against nearby or direct strikes.

Grounding the J-pole shorting bar places it at the same electrical potential as the braid side of the feedline coax. Although both points are at zero potential (voltage), the currents are out-of-phase with each other by 90 degrees. To be electrically equivalent, both voltages and currents must be equal in phase and amplitude.

Figure 1 illustrates how forcing the coaxial braid (d) and the shorting bar (f,g) to a common reference inhibits ground current from flowing in the J-pole conductor between points (d) and (g). Consequently, the shorted stub at the base of the J-pole (d,e,f,g) can't behave as a balanced transmission line. Current flowing on the side connected to the center conductor (e,f) attempts to induce an equal and opposite current component on the side connected to the shield (g,d), but needs to create a potential difference between points (g) and (d) to do so. This requirement conflicts with keeping them at the same potential, destroying the balance in the line.

The conductors that make up the shorted stub, (e,f) and (g,d), are in parallel and proximity to one another and establish an RF current return path to the feedline at (d). Current flowing in (e,f), upon finding a parallel return to earth ground, creates a ground loop. RF current is induced in the earth return and the outside of the feedline shield. This condition can be corrected by introducing a balun where the feedline connects to the antenna.

J-poles constructed from plumbing hardware are often shown with the feedline routed through the center of the tubing to isolate or shield it from the radiating portion of the antenna. This technique is effective at keeping RF from conducting along the outside of the feedline shield, but it's not a balun. Electrically connecting the shorting bar to an earth reference forces two points on the J-pole to the same electrical potential and establishes the ground loop.

If an earth reference isn't required, the J-pole will work well without a balun. Routing the feedline coax through the tubing center will reduce feedline currents adequately.

Slowing down a bit

Radio waves propagate along a transmission line more slowly than in free space or air. The difference in the propagation speed is the

velocity factor: it varies as a function of the dielectric properties of the material used in the construction of the transmission line. Velocity factor is critical for accurate computation of the electrical characteristics of transmission line circuit elements (i.e., inductance, capacitance, or phase rotation). The accuracy with which velocity factor is known is perhaps the sole nemesis of most J-pole designs. It appears to be the design parameter most often ignored, although it's easy to measure.

Revelation six: caveat emptor

I contacted a popular U.S. manufacturer of television twin-lead products for an estimate of velocity factor tolerance in the manufacturing process, and made another revealing discovery. Their large selection of 300-ohm TV twin-lead products varies widely in dielectric properties and physical construction. Physical variations range between flat solid versions (generally the lowest cost varieties) to solid jacketed low-loss foam. Varieties also differ in the construction of the region between the conductors (e.g., ladder line versus solid fill).

The dielectric constant of a given "recipe" of insulating materials may be of some nominal value (0.66 or 0.82 for solid versus foam varieties, respectively). The density of the material and the combinations of dielectrics used, all contribute to the velocity factor.

My most significant discovery was that velocity factor is neither known nor controlled in any of this particular manufacturer's products. One company engineer stated that their manufacturing focuses on controlling only the impedance and loss properties. He recommended I perform my own measurements. Consequently, you'd be well advised to measure the velocity factor of any transmission line you plan to use for antenna matching.

Sensitivity to errors in velocity factor drops with decreasing transmission line impedance. The proof lies in plots of three test cases on a Smith chart for impedances of 200, 300, and 450 ohms, which introduce plus and/or minus 1 percent changes in velocity factor for each case.

This may explain why bygone-era J-pole designs are closer to 200 ohms. At the price of a slight increase in sensitivity to errors in antenna feedpoint impedance, sensitivity to velocity factor is reduced.

J-poles from ladder line have proven successful because open ladder line has a velocity factor close to air. Such designs are more forgiving when this parameter has been ignored.

Awareness of the importance of velocity factor, the use of a reasonable antenna tuning procedure, and a balun (if earth ground referencing

is necessary) are all we need to guarantee reliable and repeatable success.

Revelation seven: two surprises

I was advised to anticipate velocity factor variations of a few (perhaps as much as 5) percent from batch to batch—much larger variations when switching between vendors, for any given transmission line style. To test the consequences, I introduced a 5-percent error in the parameter and was unable to achieve a match. I also confirmed this analytically.

To validate the design model on HF (an ended Zepp), I recently purchased twin-lead using the exact RadioShack part number of the material I purchased in Maryland six or more years earlier. The measured velocity factor was exactly equal to my old batch, within plus or minus 0.1 percent.

Recalling that the vendor I consulted informed me that only impedance and loss parameters are controlled in their products, I was surprised by the "coincidence." Velocity factor is hardly a critical parameter for consumer television antenna installations, so it's unlikely RadioShack's supplier makes any attempt to control it.

A quick review of transmission line equations reveals that the phase constant of any given line is a direct function of the velocity factor, which is the phase constant modified by the dielectric properties of the medium. The phase constant sets the conductor spacing-to-diameter-ratio. This, itself, must be held uniform and constant along the length of the transmission line to maintain the constant L/C ratio that establishes the characteristic impedance of the line.

My inference from this observation is that a tightly controlled characteristic impedance (independent of loss) must, by necessity, maintain tight control over velocity factor. This seems plausible, as conductor diameter and spacing are more easily held constant than varied by some criteria, to establish a line of uniform characteristic impedance during the manufacturing process.

This observation suggests that those who wish to procure TV twin-lead from RadioShack and build a J-pole should be able to do so with reasonable confidence. The velocity factor of "Super Low-Loss Foam TV Twin-Lead Cable" (RadioShack No. 15-1174) is 0.769.

Velocity factor for a given brand and style of twin-lead need be determined only once. As long as nothing is changed, the number should remain valid. Velocity factor is somewhat independent of frequency, and the construction of J-poles on other bands can be scaled with good

success. Accuracy improves at longer wavelengths, however, because of the increased resolution in the measurements of both frequency and physical length.

A small, but measurable, increase in velocity factor may be observed at HF where conductor separating is a smaller fractional wavelength and the influence of dielectric material between them is reduced. The twin lead used in my experiments exhibited a velocity factor of 76.5 percent at 146 MHz and 76.9 percent at 28 MHz.

Get a load of this!

Packaging twin-lead in PVC for mechanical rigidity, creates a plethora of mounting options and expands the utility of this version of the J-pole. Not unexpectedly, the electrical characteristics are modified by the PVC's dielectric properties, which lowers the resonant frequency of the antenna and the velocity factor of the matching elements. As for the stub length, simply determine the velocity factor for twin-lead installed in the material you want to use, then proceed with the design as in the open air case.

I ignored the contribution of PVC and observed no negative side effects aside from a reduction of about 4 MHz in antenna resonance. A slight shortening of the dipole brought it back to 146 MHz. No special installation effort was required, no recalculating, no adjustment of the "tap," and no perceptible change in performance. This testimony to the J-pole's tolerance of fabrication errors shows how easily the design can be "cloned."

Two for the price of one

An antenna tuner in place of the shorted transmission line stub would produce the familiar end-fed Zeppelin or Zepp.¹⁰ This antenna is another universally misunderstood design. The G5RV is a center-fed derivative only loosely related to the end-fed J-pole.

A 450- to 500-ohm ladder line section exactly one quarter wavelength long would match the end fed dipole in this example exactly. No tuner or shorted stub would be required. This would be the minimum or root form of the Zepp. Unless operation is only desired over a narrow bandwidth, a 1:1 balun is recommended.

A balanced tuner permits use of the antenna over a wide range (often several bands). This is why that configuration of the Zepp is most

common. Significant feedline radiation is expected when operating on frequencies where the "random wire" isn't an exact multiple of half a wavelength.

In general, end-fed Zepps, unlike center-fed dipoles, are suitable for multiband operation on both even and odd frequency multiples. Avoid feedline lengths that approach half-wave multiples at one or more of the desired operating frequencies. Such a condition would be difficult to tune; the impedance presented to the tuner would approach several thousand ohms. End-fed designs are also installation versatile.

Does it perform?

Because it is a half-wave radiator, the performance of a J-pole should be exactly equal to that of any properly designed, matched, and tuned half-wave dipole—regardless of how it's fed. In addition, half-wave vertical antennas don't require a ground plane or counterpoise as do quarter-wave designs. As a result, radiation efficiency and the angle of elevation can be more easily controlled.

Build your own

Now that you know all the particulars, why not build your own J-pole or Zepp? The appendix provides the design procedure you need to construct the antenna of your choice with or without the Smith chart.

Acknowledgements

Thanks to Dick Lodwig, W2KK, Chet Burroughs, KE4QNG, my peers on the Internet, and my wife, Marie.

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Appendix A: Designing a J-pole

Use this procedure to design a J-pole or fixed tuned end-fed Zepp antenna with or without a Smith chart. A "normalization" process is included. This adds a couple of steps, but provides results that can be directly applied to a Smith chart.

Getting started

The procedure requires a number of input parameters or reasonably close estimates. I used a feedpoint impedance of 5000 ohms as an estimate for the impedance of an end-fed dipole element for my analysis and experiments. This value is likely an upper limit and will be high if large conductors, like copper tubing, are used.

I chose a velocity factor of 0.769 because I used "Super Low-Loss Foam TV Twin-Lead Cable" (RadioShack No. 15-1174) in my experiments. This parameter is quite critical and you should measure it if unknown.

I've simplified impedance and admittance calculations whenever possible by ignoring the complex component when it is zero (i.e. +/- j0).

The calculations

1. Normalize the antenna impedance to the stub transmission line impedance:

$$ZP = ZA/Z0 \quad (A1)$$

Where:

ZP = the antenna impedance ZA normalized to the stub impedance Z0.

2. Calculate the antenna reflection coefficient, rho, using **Equation A2**. This describes the constant VSWR circle on the Smith chart.

$$RHO = (ZP-1)/(ZP+1) \quad (A2)$$

Where:

RHO = the antenna reflection coefficient with respect to the matching stub impedance.

3. Convert the feedline impedance to normalized admittance. (Note: admittance is the reciprocal of impedance.)

$$YF = Z0/ZF \quad (A3)$$

Where:

YF = the feedline admittance 1/ZF normalized to the stub admittance 1/Z0
ZF = the characteristic impedance of the coaxial feedline

Z0 = the characteristic impedance of the transmission line used for the matching network, to which all calculations are normalized

The feedline admittance may now be expressed as $YF = G + j0$ mhos in its complex form.

4. Calculate the normalized capacitive susceptance at the point where the circle of constant antenna reflection coefficient (constant VSWR calculated in step 2) intercepts the line of constant conductance equal to the feedline admittance calculated in step 3.

$$B = \text{SQR}((RHO * RHO * (YF + 1) * (YF + 1) - (YF - 1) * (YF - 1)) / (1 - RHO * RHO)) \quad (A4)$$

Where:

B = the capacitive susceptance that appears when looking at the feedline end of the series transmission line before connecting the shorted stub element.

The equation yields two roots that differ only in sign. The negative root represents the capacitive susceptance to be canceled by the shorted stub.

The conductance calculated in step 3, along with this susceptance, defines the admittance (Y), which is plotted on a normalized admittance chart as:

$$Y = YF - jB \text{ mhos}$$

Where:

YF = the real component of the admittance
B = the imaginary component of the admittance preceded by a -j to indicate a negative or capacitive susceptance.

5. Calculate the inductive reactance of the shorted stub required to cancel the susceptance from step 4 using **Equation A5**.

$$X2 = 1/B \quad (A5)$$

Where:

X2 = the normalized reactance of the shorted stub section. (Note: this is the negative of the capacitive reactance we wish to cancel.)

6. Calculate the electrical length (L2) of the shorted transmission line (stub).

$$L2 = \text{ATN}(X2) * (180/3.14159) \quad (A6)$$

Where:

L2 = The length of the shunt (bottom) transmission line matching section in degrees.

7. Calculate the impedance (Z) at the intersection of the antenna reflection coefficient (rho) and the line of conductance equal to the feedline admittance (YF). This is the reciprocal of the admittance (Y) from step 4 and requires taking the reciprocal of a complex number. The steps are shown to demonstrate how this operation is performed mathematically.

$$\begin{aligned} R &= YF/(YF*YF+B*B) \\ X1 &= B/(YF*YF+B*B) \end{aligned} \quad (\text{A7})$$

Where:

R = The real part of the impedance ($Z = R+jX$) at the intersection of the rho and G contours.

X1 = The imaginary part of the impedance at the intersection of the rho and G contours.

This is the inductive reactance for which the shorted stub must be designed.

8. Calculate the electrical length of the top transmission line section. This is the length of transmission line required to rotate the antenna impedance (along the line of constant VSWR) to the coordinates of Y.

$$L1 = 90 - (\text{ATN}(X1) * (180/3.14159)) \quad (\text{A8})$$

Where:

L1 = the length of the series (top) transmission line matching section in degrees.

Up until now, we haven't yet considered the frequency or band of operation for which the antenna is being designed. You can build your J-pole (or Zepp) for any band you wish. By saving the calculations made thus far, you may simply scale the results to the frequency of your choice.

9. Calculate the physical length of each section of the J-pole to complete the design. The velocity factor must be used when calculating the physical length of the transmission line sections (B and C in **Figure 1**). The dimensions have been normalized to MHz, inches, and degrees in **Equation A9 A-C**.

$$\text{DIPOLE} = 5606/F \quad (\text{A9-A})$$

Where:

F = Design center frequency in MHz.

Note: The constant 5606 is 95 percent of the speed of light in inches for half a wavelength at 1 MHz.

Now, refer to **Equation A9-B in Section B in Figure 1**.

$$\text{SERIES} = 32.78 * V * (L1/F) \quad (\text{A9-B})$$

Where:

L1 = The computed electrical length in degrees

of the series transmission line matching section
V = The velocity factor of the transmission line used for performing the match.

F = Design center frequency in MHz.

Note: The constant 32.78 is the speed of light in inches/degree/MHz.

Continue using **Equation A9-C in Figure 1**.

$$\text{SHUNT} = 32.78 * V * (L2/F) \quad (\text{A9-C})$$

Where:

L2 = The computed electrical length in degrees of the shunt transmission line matching section

10. Strip the insulation from one end of the transmission line to be used for the J-pole at a length slightly greater than its width. Twist the bare wire ends together snugly, and generously solder the connection. This is the short-circuited end (bottom) of the J-pole.

11. Measure from the short the distance C calculated in step 9. Carefully remove only enough insulation on the edges of each side of the transmission line to bare a 1/16-inch length of the conductors. Take care not to nick the wires. Generously tin the exposed areas with solder. This is where you attach the 50-ohm coax feedline.

12. Once again, measure from the short-circuited end (bottom) of the J-pole a distance that is the sum of distances B and C calculated in step 9. Carefully cut through the conductor (on one side only) of the transmission line at this point, and once again a 1/4 inch farther. Remove the conductor material from the 1/4-inch-long section of transmission line just severed. This is the top of the short (left) side of the "J." You may remove the entire length of wire above the cut, but it's not required.

13. Again measure, from the bottom, a distance that's the sum of all three distances (A, B, and C) calculated in step 9. Cut the antenna off at this length to complete the J-pole.

14. Carefully separate the shield and center conductor at one end of the feedline coax cable, snugly twist the shield into a pigtail, and tin with solder. The lead lengths shouldn't exceed the width of the J-pole transmission line. This allows for a stable and reliable connection. A 10- to 15-foot-length of RG-58 makes a convenient and portable assembly. Rooftop- and tower-mounted J-poles require longer runs. Keep the feedline as short as possible at VHF and UHF to minimize losses. Where maximum height is desirable, use a low loss coaxial cable for the feedline.

15. Solder the shield of the coaxial feedline to the feedpoint location exposed and tinned in step 11, on the short (left) side of the J-pole.

16. Solder the center conductor of the feed-

line to the remaining feedpoint location, and trim excess leads that may be exposed at the connections to keep the area free from parasitics.

17. Inspect all connections for sound electrical and mechanical integrity. Using vinyl electrical tape or shrink tubing, secure the coax to the twin-lead from just above the feedpoint to just below the shorted matching stub.

18. Attach an RF connector to the other end of the coaxial cable to complete the fabrication.

19. Tune the J-pole as you would any other resonant wire antenna. Measure the VSWR and

shorten the length of the dipole element in small increments until you achieve a near 1:1 match. To avoid accidentally trimming the antenna too short, adjust the length of the dipole by first folding back the dipole element against itself at the top. Once you determine the correct length, trim away the excess length.

For a BASIC program that performs the calculations described here, send a no. 10 SASE to: *Communications Quarterly*, P.O. Box 465, Barrington, New Hampshire 03825.

PRODUCT INFORMATION

The AD1843 SoundComm® Codec from Analog Devices

Analog Devices has announced production of their multimedia codec that supports audio, V.34 modem, fax and video signals simultaneously. The AD1843 SoundComm® codec supports up to four simultaneous sample rates, allowing it to synchronize and unify audio, modem, fax and video signals. The device addresses the need for a single, low-cost audio and communications front end in PCs where sound cards, fax/modems, multimedia and telephony applications are converging. The codec gives add-in card manufacturers a way to combine, on one card, a range of sound, fax, and modem functions that can run concurrently.

On-chip resources include two ADC's, four DAC's, modem, audio, and resampler digital filters, three digital phase lock loops, seven stereo analog inputs, four stereo analog outputs, stereo headphone driver, bit and conversion clock outputs. The AD1843 can sample an audio signal at one of several rates while locking that audio to an external MPEG clock, NTSC-horizontal, PAL-horizontal, or modem-terminal sync signal. The AD1843 operates from one 24.576-MHz clock or crystal source, and its inputs can be programmed on-the-fly to any sample frequency between 4 and 54 kHz to within 1-Hz resolution. The clock phase may be advanced or delayed in increments of 0.12 degrees.

The AD1843 serial port can be used with any DSP that provides a multichannel Time Division Multiplexed (TDM) serial port or a Pentium™ class microprocessor with a bus interface ASIC. Signals are included to allow multiple AD1843 codecs to operate in a daisy-chain configuration for professional-level audio applications where as many as six or eight channels of output are needed.

For more information, contact Analog Devices, Inc., Three Technology Way, Norwood, MA 02062; phone 617-461-3881; fax 617-821-4273.

Squel-Stopping Silent-Plug® from Switchcraft®

Switchcraft's Silent-Plug® has a circuit-closing device that prevents annoying hums, squeals and pops from occurring when the plug is inserted or removed from the jack. The Silent-Plug features a switch near the base of the plug finger that, when depressed at the time the plug is completely inserted and released when withdrawn from the jack, prevents audio feedback. The Silent-Plug is a two-conductor 1/4 inch plug that accepts cable up to .370" in diameter and is available with screw terminals or solder lug and cable clamp. The one-piece tip rod assembly also insures plug quality and durability. The one or two-piece nickel-plated brass handle is shielded and supplied with a mylar tube for protection. Red or black plastic handles are available on special order.

For more information or product literature, call 312-792-2700 ext. 243.

New Spectrum Analyzer for Digital Communications

Hewlett-Packard Company has introduced a high-performance spectrum analyzer that provides the frequency and dynamic range for high-speed digital-communication applications.

The new spectrum analyzer, HP 8562E, allows manufacturing and R&D engineers to test network components with state-of-the-art performance at frequencies required for digital-communication networks. The HP8562E spectrum analyzer's 13.2 GHz frequency range covers the 12.75 GHz and 12.5 GHz spur-search ranges specified by leading standards organizations in Europe and the United States. The increase in dynamic range is a full 6 dB more than previous HP spectrum analyzers in this frequency range.

For further information, contact Hewlett-Packard Company, Direct Marketing Organization, P.O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059.

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QUARTERLY COMPUTING

NTE's WinBoard and WinDraft

Who hasn't wished for simple software that would let them compose camera-ready schematics and pc board layouts in a small workshop environment? I've searched long and hard to find a program that works for me.

A few years ago, I was given an opportunity to purchase a registered commercial CAD software package for creating schematics and pc board layouts. The software normally sold for

over \$1,000 and was being offered to hams for \$300. The catch was that, at this price, there would be no direct factory support other than from the person selling the discounted version of the software. And, at the time, there were no manuals available!

The demo disk allowed for limited experimentation with the program on a 30-day trial basis. Alas, my vision of CAD schematic software (some sort of computer-based

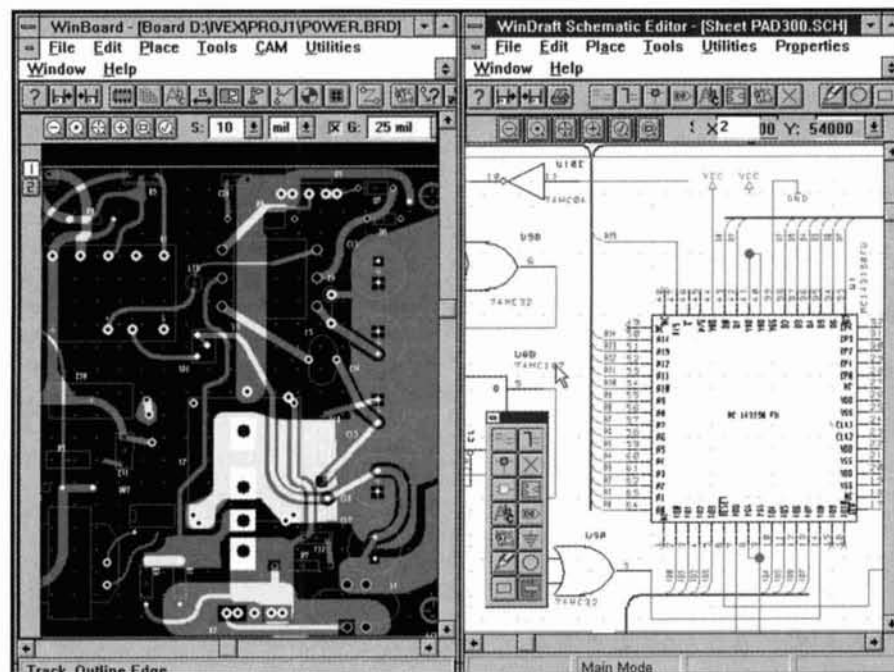


Photo A. Abridged computer screen renditions of IVEX WinBoard (left) and IVEX WinDraft (right). The secondary toolbars across the top of the screen may be "hidden," permitting more screen display work area. In the WinDraft screen, the "Floating Icon" display may be dragged and dropped into any screen location, or turned off. This WinDraft schematic highlights how the program handles multiple signal buses easily.

“Etch-a-Sketch”) was vastly different from what was available in the real world. Trying to learn the program via long-distance telephone calls soon proved an expensive and frustrating experience. The seller told me that he was able to train a friend to use the software after a week of instruction. Needless to say, I passed on his offer and continued my search for a user-friendly program.

Enter NTE

NTE Electronics, Inc., is well known for its extensive line of replacement electronic components. When I learned they were adding *WinDraft* and *WinBoard* to their product line, I was eager to sample what was promised as user-friendly and easy-to-learn software!

WinDraft operating system requirements

WinDraft, the schematic capture program, requires a high-speed 486DX or Pentium-based computer system running Microsoft's Windows 95 with 8-megs of RAM or Windows NT-based system. Windows 3.1x holdouts will need a MicroSoft program, Win32s, to run the 32-bit WinDraft application software. A copy of Win32s is available from the IVEX BBS, FTP, or World Wide Web sites. Your Windows environment must be stable and free of GPFs to use this software reliably.

For best results, your video board should support the 800 by 600 and 16-color SVGA mode, best viewed on at least a 15-inch high resolution monitor. The programs will run in VGA mode in a pinch. I've used the programs on several test machines with 14-inch monitors. The IVEX software does let you “zoom” in and out of specific areas—making life a bit easier for those of us with 14 or 15-inch monitors. But for CAD work, the bigger the monitor screen, the better! As with any Windows software, a comfortable mouse or trackball is needed. This software requires very little keystroking. Most of the work is done via toolbar selection and from fixed and floating icon sets (see **Photo A**).

WinBoard will run under Windows 3.x, Windows 95, or Windows NT and doesn't require 32-bit access. Together, both programs need at least 30 megs of free hard drive space. Each program is supplied on two 1.44 3-1/2 inch floppies.

Naturally, the end products of this software reflect the quality and resolution of the system's printer. Both programs support dot matrix, ink jet, PostScript, laser, or Windows-supported pen plotters such as HP-GL. I even tried an inexpensive (currently about \$148 with discount pricing) Epson Color Stylus IIs with

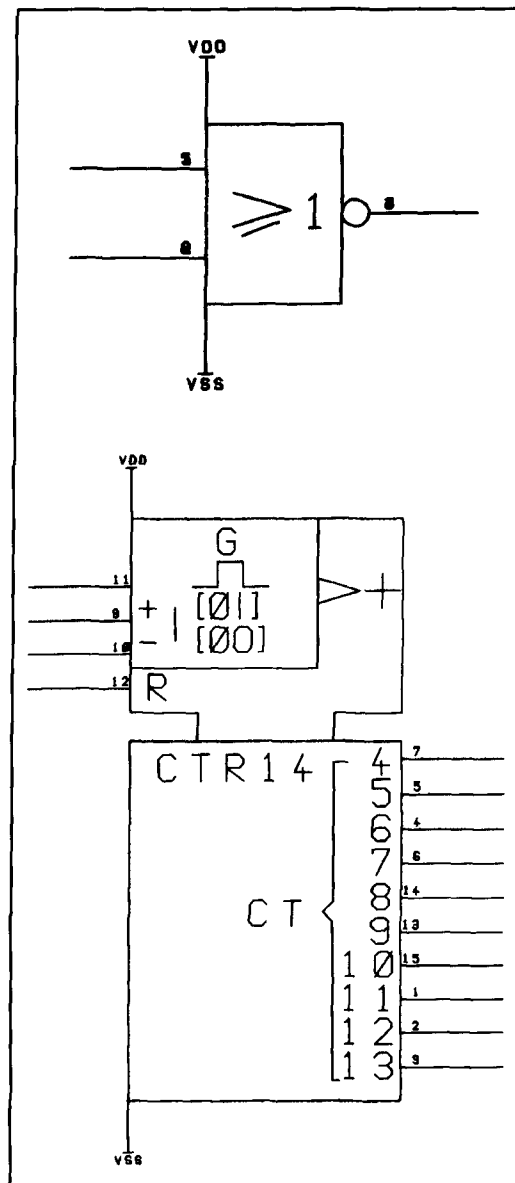


Figure 1. These devices from IVEX's WinDraft CMOS part library will do the job, but weren't what I expected. (A) shows a CMOS 4001 quad NOR gate and (B) is a 4060 oscillator counter IC. More conventional renditions may be created easily using the WinDraft parts editor.

720x720-dpi resolution. It produced camera-ready schematic artwork or pc board transparencies, although it was rather slow at the higher print resolutions. The Epson IIs can take up to 15 minutes to do an 8-1/2 by 11-inch schematic. Several years ago, you'd have paid dearly for a printer or pen plotter that would handle CAD/CAM software. Today you have several reasonably priced options.

IVEX Design International

WinBoard and WinDraft are products of IVEX Design International. I was surprised to

learn that IVEX demos these products as uncrippled shareware. The restriction in the shareware versions is a 100-pin limitation for either program. The pin count roughly translates to the number of terminals on a device. For example, a CD4001 CMOS gate in a 14-DIP package would have a pin count of 14 pins. I was able to do quite a bit of work using the 100-pin shareware versions. The 220-pin versions should be able to handle most ham designs without problems.

Thirty-day factory support is offered for shareware and pin-limited registered versions, while unlimited pin registered owners receive lifetime technical support. After the first call, and once the 30-day limit is reached, shareware or limited-pin registered users may be charged *by-the-minute* for factory technical assistance.

Normally, registration is done in 100-pin increments; each 100-pin increase costs \$50. Either program can also be purchased with no pin limitations for \$495. IVEX refers to the *unlimited-pin* versions as WDPX and WBPX. But remember, though, 8 megs of RAM may not be able to handle these versions. Each registration upgrade buys you a new password, not more software. The software limitations are keyed to the password supplied by IVEX. You pay only for what you need. NTE's price for either program is \$29.95—quite a bargain because the password for 200 pins also supplied. You can e-mail IVEX and receive an additional free 20-pin password upgrade (for a total of 220 pins). Upgrades are handled through IVEX.

As you increase the pin capacity of your program, you may find it beneficial to add more RAM to your computer. NTE is adding specially packaged 350-pin versions of WinDraft and Windboard for \$99. These packages also include the "Getting Started" manual. Because IVEX does the actual packaging, the latest software versions are always being shipped.

Manuals

Most of the material in the manuals is available in either program's on-screen help section and may be printed out as needed. Hitting the F1 key brings up the entire table of contents, allowing you to quickly select the reference area where help is needed. The manuals may be ordered from IVEX directly. Three are offered: one each for the WinDraft and WinBoard programs, and a more general User's Guide for "Getting Started and Tutorial" information.

The printed manuals are \$25 each, and the User's Guide is fairly small at only 76 pages. But for the CAD novice, they are a "must have" to get anywhere! The WinBoard and WinDraft manuals are spiral bound and will lay

flat when opened. The complete text of the latest manual editions may be downloaded without charge from IVEX on their Internet Web page and printed out on your printer.

Factory support

Before I'm tempted to say anything less than favorable about this software, I must comment on the excellent technical support provided by the folks at IVEX. In all honesty, my first impulse upon test-driving WinDraft for an evening was to return it and forget the review.

What changed my mind? First, I had wisely invested in the manuals, and upon their arrival followed the example exercises closely. Things began to make sense at that point. But more importantly, by reading the manuals, or using the online help first, I was able to get started and actually do something! When I needed to call IVEX for help, both the support person and I were in a better position to understand one another!

There are several ways to obtain technical assistance (see **Table 1**). Perhaps the easiest and fastest (and most costly!) method is to dial the factory help line directly. A wiser choice would be to look in the manuals first. And, if you don't have the manuals, the online help screens contain nearly all the same information. Online help is available when you're creating a sheet or pc board layout. You needn't exit from the work in progress to access the help screens. I advise that you read all of the material offered in the various IVEX window icons!

Browsing the program, you'll find undocumented features, lists of known bugs, and even a tutorial to help you begin. You may also call IVEX's BBS for the latest software and library upgrades, technical hints, and to interact with other IVEX software users. There's no charge for BBS access. Technical help is also available via e-mail at <help@ivex.com> via AOL, CompuServe, and other services. Their Internet World Wide Web page is <<http://www.ivex.com>> and provides access to tech notes, application notes, how-to sections, the manuals, and all of the available parts libraries. As a registered user, I have also been receiving regular e-mailings from IVEX dealing with the most commonly received calls for assistance. This is a nice touch. You'll find all of the notices already sent on the their Web site. Note that NTE isn't able to answer technical questions regarding this software.

I had numerous chances to try all of these support options. Alas, initial access to the IVEX Web page using AOL was a painfully slow experience. Fortunately, AOL access to Web sites has improved recently. Direct long-distance calls for support always resulted

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Technical support: (503) 531-9443
24-hour BBS: (503) 645-0576
FAX: (503) 629-4907
e-mail: info@ivex.com
e-mail, tech support: help@ivex.com
Internet WWW: http://www.ivex.com
Anonymous ftp: ftp://ftp.ivex.com

Test platforms:

Cyrix P166 system, 32 megs EDO RAM,
Matrox Millenium 2-megs WRAM PCI,
SCSI-II 2.9 gig HD, Windows '95 operating
system, Epson Stylus Pro, 15-inch SVGA
monitor.

AMD 486DX80 system, 8 megs RAM,
420-meg EIDE HD, Cirrus Video VLB with 1
meg video RAM, Windows 3.1/WIN32S,
Epson Stylus IIs, 14-inch SVGA monitor.

AMD 486DX100 system, 16 megs RAM,
210-meg EIDE HD, Trident VLB with 1 meg
video RAM, Windows 3.1/WIN32s, NEC
2200 Pinwriter.

Table 1. Support information for WinDraft and WinBoard.

in quick access to a technician. In those rare instances where they couldn't immediately answer a question, they would promise a quick reply via e-mail. As promised, an e-mail response was always in my electronic mailbox by the next working day.

A nice e-mail feature is that it lets attach a troublesome file to permit the factory folks to see first hand what problems you're having. E-mail inquiries were also promptly answered by the next working day.

If there's any advantage the IVEX software has over other competitive offerings, it has to be reflected by the quality and dedication of the people I've dealt with when I needed help. This, plus their generous 30-day no-cost support for unregistered or limited users, gives these products a Four Star, No Risk rating in my book! IVEX also offers a 90-day return period for their products purchased direct from the factory!

IVEX continually upgrades the software, and

they are very upfront and honest about listing any known fatal software glitches—offering advice on how to get around them until the next software upgrades are available for downloading. This is an example that I wish other software manufacturers would follow. All too often, I've been stuck with expensive software that doesn't work as advertised and is unreturnable once the shrink wrap is removed.

I must confess I have a long way to go to master or fully appreciate all that these programs have to offer. There's a considerable learning curve for those new to CAD programs. For most of us, this is a whole new technology with its own unique vocabulary. The manuals could stand some improvement in numerous areas; they sometimes left questions unanswered for the novice user. For example, in both WinDraft and WinBoard, I often became confused and lost when it came to recovering from blunders. I'd find myself wondering: "How can I change my one-sided board layout to double-sided once I've already started the layout? How do I lay down pads for wire jumpers?" (This question was answered subsequently in a general e-mail from the factory. You first have to create a library of pads.) If you have previous experience with similar CAD programs, like OrCAD or CIRCAD, you'll probably feel right at home with *WinBoard* and *WinDraft*.

You'll be happy to know that these programs can import OrCAD libraries or schematics. I advise that beginners try WinDraft first. Once you achieve mastery of this program, you'll find that the WinBoard software makes more sense.

Parts libraries

Key to using WinDraft, which will also affect your ability to generate pc boards in WinBoard from a WinDraft netlist, is the ability to make up your own parts libraries. The WinDraft parts libraries not only define how a component appears on the schematic, but also its physical characteristics and electrical pin assignments. While the number of libraries offered by IVEX is always growing, it's unreasonable to expect that every linear or RF device will appear in a library of parts, or in the form we wish to use! For example, **Figures 1A** and **B** show IVEX parts library representations for the CMOS 4001 quad NOR gate and a 4060 oscillator counter IC. While these may be someone's ideal schematic representations of these parts, they bear no similarity to what's shown in my factory data books for these devices. But remember, many of these libraries are contributed by other users and then distributed by IVEX as a free service to their customers.

You may create new or modify existing parts to fit your needs with the help of WinDraft's parts editor. A recent excursion to the IVEX BBS netted user-contributed libraries of Motorola's microprocessor line and many of their discrete components.

Some pitfalls

While in WinDraft, I tried using a library part for a common multisection linear IC. Although I was able to lay down each schematic representation of the quad package, each package repeated the Vcc and grounds on pins 4 and 8! This was something I didn't want to appear on the schematic, and it also caused nonfatal ERC warnings concerning these unassigned pins when running netlist. While this is a quick fix for those "in the know" who perform some quick parts library editing, it's a formidable task for the novice.

IVEX software is aimed at the commercial user, or those of us with a need to do this sort of work at home or in a small shop. If the software lacks anything, it is that the WinBoard program has no autorouter or automatic parts placement functions. Then again, it doesn't cost \$30,000 either. For those who need autorouting, IVEX is licensed to distribute the Spectra autorouter program. Prices start at about \$650 for 1000-pin autorouting capabilities. I can't

give you a feel for its performance, as I didn't review this product.

WinDraft will read in OrCAD schematics and libraries and uses industry standard formats for EDIF and ASCII in/out. WinDraft comes complete with Electronics Rules Checking (ERC) for finding and flagging unused inputs and invalid connections on your sheets. The program will produce a summary listing of all parts used on a schematic in a Bill of Materials (BOM). WinBoard will read in netlists from WinDraft, OrCAD, Tango, Protel, and other CAE programs. It has industry standard outputs for Gerber photo plot, NC Drill, and Bill of Materials. The WinBoard package also features Design Rules Check (DRC) and Pick&Place.

Pick&Place produces up to six output reports for controlling the grouping for through-hole components, SMD components on the solder or component board sides, and adhesives on either side. These files are used by Pick&Place automated insertion machines during the manufacturing process.

Don't let the preceding list of features scare you away if you're a neophyte to CAD/CAM! If you don't understand most of the terminology, chances are you don't need to and won't use such advanced features for some time. I was able to generate many of the schematics shown in this issue's "80-dB Log Amplifier and IF System" article after a few days of experimenting with WinDraft! ■

PRODUCT INFORMATION

AudioFLEX Snake Cables from Belden

Belden Wire & Cable Company has announced a new line of super-flexible, non-kink multiple-pair audio cables which exhibit a low level of microphonic or triboelectric noise. Brilliance® AudioFLEX Snake Cables provide better performance to traditional analog, remote field-deployable broadcast cabling applications. Typical uses for these cables include connecting multiple audio channels in low-level and high-level componentry such as console board equipment for recording studios, radio and TV stations, post production facilities, and sound system installations.

The cables feature Belden's French Braid Double Shield, a double spiral (double serve) bare copper shield tied together by one braided strand. The cable produces lower levels of microphonic or triboelectric noise than conven-

tional braid or single and double spiral shields. It provides for a lower DC loop resistance than a single spiral shield, for lower attenuation.

There is a choice of 2, 4, 6, 8, 12, 16, 24, or 32 pairs of high strand count (41 x 40) 24 AWG bare copper conductors with polyolefin insulation. The pairs are individually shielded and jacketed, so they can be split out of the overall jacket as needed and still maintain their mechanical integrity. The pair jackets are made of PVC and are numbered and color-coded with non-repeating colors for easy identification. The overall jacket is a matte finished, super flexible black PVC.

To obtain additional information on Belden Brilliance® AudioFLEX Snake Cables or other Belden cables, contact Belden Wire & Cable Co., P.O. Box 1980, Richmond, IN 47375; phone 1-800-BELDEN-4.

BASIC SYNTHESIZERS AND HOW THEY WORK

*A guided tour through the maze of
modern synthesizer circuitry and
techniques*

Synthesizers appear in virtually all new receivers and transceivers today. They appear in one form or another, and they offer tremendous advantages over other forms of local oscillator. This is particularly true now that large parts of these synthesizers can be contained within a single integrated circuit.

As a result of the use of synthesizers, we have come to expect many facilities. These include very good frequency stability, accurate frequency setting, multiple memories, remote setting of the frequency, and scanning.

There are many more facilities which would not be possible, if it were not for the use of synthesizers. Yet, the circuitry behind these now common systems, present many challenges to the designer.

There are many ways of achieving the required result. However, if the cost is to be kept to a minimum without compromising the performance, then the designer's job is made more difficult.

Analog methods

Initially, analog methods were used for synthesizing signals. Analog techniques involved taking a signal, dividing it in frequency, and then mixing this signal with others generated in the same way.

As you can imagine, this required very good filtering if it were to be successful, and the levels of spurious signals were to be low enough. Because of the design constraints, these early synthesizers were very expensive, and they were only used in specialist applications.

Another method is to store the shape of the waveform in a memory, then read out various points on it which are then converted into an analog form. This type of synthesis is known as direct digital synthesis (DDS).

The DDS technique is now finding its way into some of the more expensive amateur rigs. However, the form of synthesizing which has been almost universally accepted today, is based around the phase locked loop (PLL).

Phase locked loop

The phase locked loop, which is at the heart of most of today's synthesizers, is basically a form of servo system. It consists of a number of basic building blocks, as shown in **Figure 1**.

The basic operation of the loop is quite simple. The phase of the two signals entering the phase detector is compared, and an error voltage is generated, according to the phase difference between the two signals.

This error voltage is then filtered, and is used to control the frequency of the oscillator. This

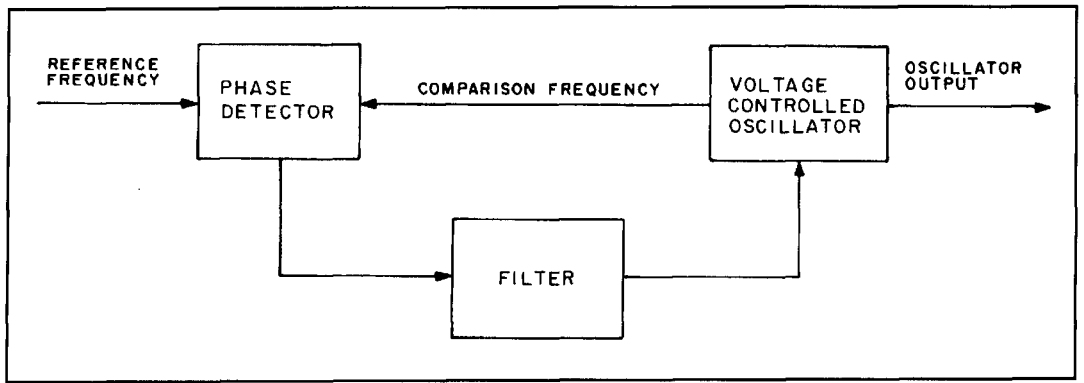


Figure 1. A block diagram of a basic phase locked loop (PLL).

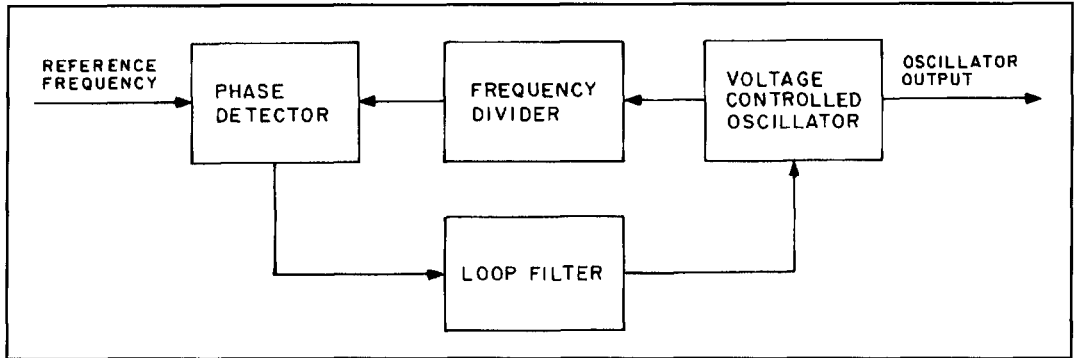


Figure 2. Block diagram of a basic synthesizer using a divider.

is done in such a way, that the phase difference between the signals entering the phase detector is reduced.

Phase difference reduced

Eventually a point is reached when the phase difference is reduced to such a degree that it remains constant. This means that the phase difference between two signals is not changing.

This is significant because there can only be a frequency difference between two signals if the phase difference is changing. It means that when the loop has reached this state, the frequency of the reference or incoming signal is exactly the same as the voltage controlled oscillator.

There may seem little point in generating a

signal at exactly the same frequency as one which already exists. However, there are a number of uses for a PLL—even in its basic form.

Widely known use

The first and most widely known use of the phased locked loop is in the demodulation of a frequency modulated signal. In the role as a demodulator, the incoming signal is fed into the loop as the reference.

The loop will then act, so that the voltage controlled oscillator (VCO) will follow the instantaneous frequency of the signal. In doing this, the VCO has to move up and down in frequency, and it will require a varying tune voltage. It's this tune voltage which is buffered,

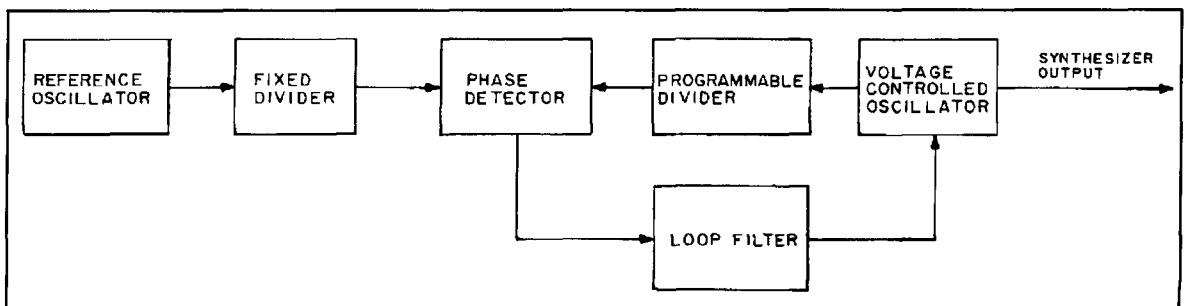


Figure 3. A basic synthesizer, with the reference oscillator frequency divided.

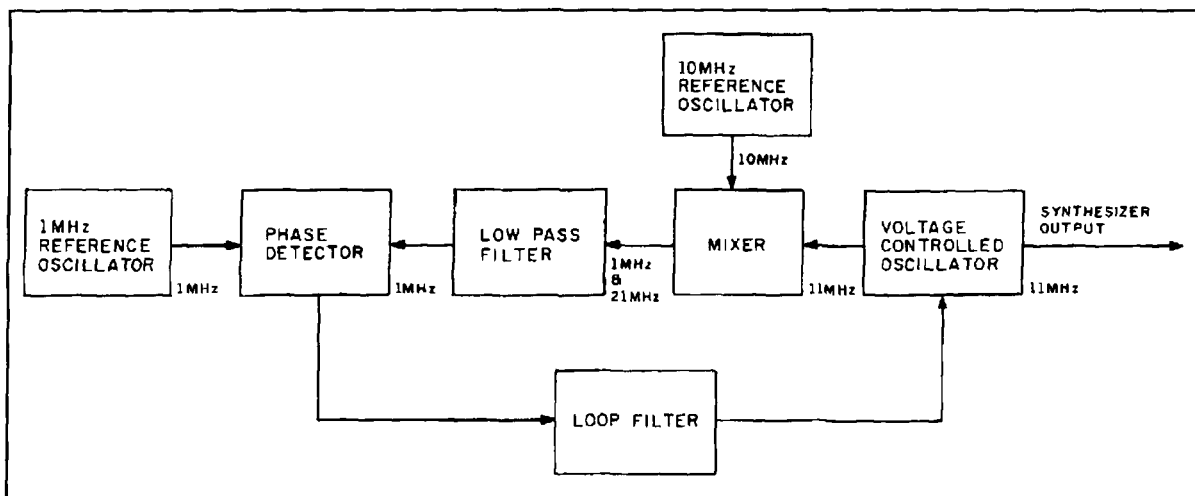


Figure 4. A synthesizer using a mixer in the loop.

and then used as the demodulated output.

Other uses of PLLs are wide and varied. Sometimes they are used to give a constant signal, when the reference is interrupted for one reason or another.

This can be done by making the time constants in the filter long, so that the tune voltage and hence the VCO frequency, is stored when the reference is not present. One common use for this method is found in televisions for use in the color demodulation circuitry.

In the PAL TV system employed in the UK and elsewhere, a color reference burst is given at the beginning of each line. A reference oscillator is then needed to store the phase information for the rest of the line, until it can be resynchronized at the beginning of the next line. Naturally PLLs are ideal for this application.

Further ingredient

In order to turn a PLL into a synthesizer, a further ingredient is needed. This is obtained by placing a divider into the loop as shown in **Figure 2**, so the VCO can be maintained at a different frequency to that of the reference.

To see how this works, I'll use the example when the divider is set to two. The phase detector will still have two signals entering, and it will generate an error voltage. This will be dependent upon the phase difference it sees between these two frequencies. In turn, the error voltage will cause the frequency of the VCO to tune to a frequency, which makes the two inputs to the phase detector the same.

For this to be true, the VCO must be operating at twice the reference frequency. Similarly, if the divider is set to divide by three, then the VCO must oscillate at three times the reference frequency, and so on for other division ratios.

With these conditions, the synthesizer can

step in frequency, by an amount equal to the reference frequency entering the phase comparator. In most practical applications, fairly small steps are needed.

Transmitter example

Let's take a 144-MHz FM transmitter as a typical equipment example using a synthesizer. The synthesizer will need to have step size of 25 kHz, if it's to be able to cover all the necessary channels.

It's not easy to develop a reference oscillator with the required stability at 25 kHz. To overcome this problem, it is usual to have a crystal oscillator. This will run at a much higher frequency, possibly 1 or 5 MHz.

The higher frequency is then divided down by a fixed amount. This is shown in **Figure 3**, and it provides the much lower frequency signal for the phase comparator. You'll also see that the division ratios for the divider may have to be quite large in some instances.

With the 144 MHz transmitter, if it's to operate over (for example) the range 145 to 146 MHz, with a phase comparison frequency of 25 kHz, then the divider will have to operate over the range 5800 to 5840.

Not the only way

Using a digital divider is not the only way of using a PLL in a synthesizer. It's also possible to place a mixer into the loop, as shown in **Figure 4**.

The effect of a mixer is quite different, but every bit as useful. This is because it essentially adds a frequency offset into the loop.

The way in which a mixer acts in the loop can be reasoned in exactly the same way as the divider. Again, the effect of the loop is to try to

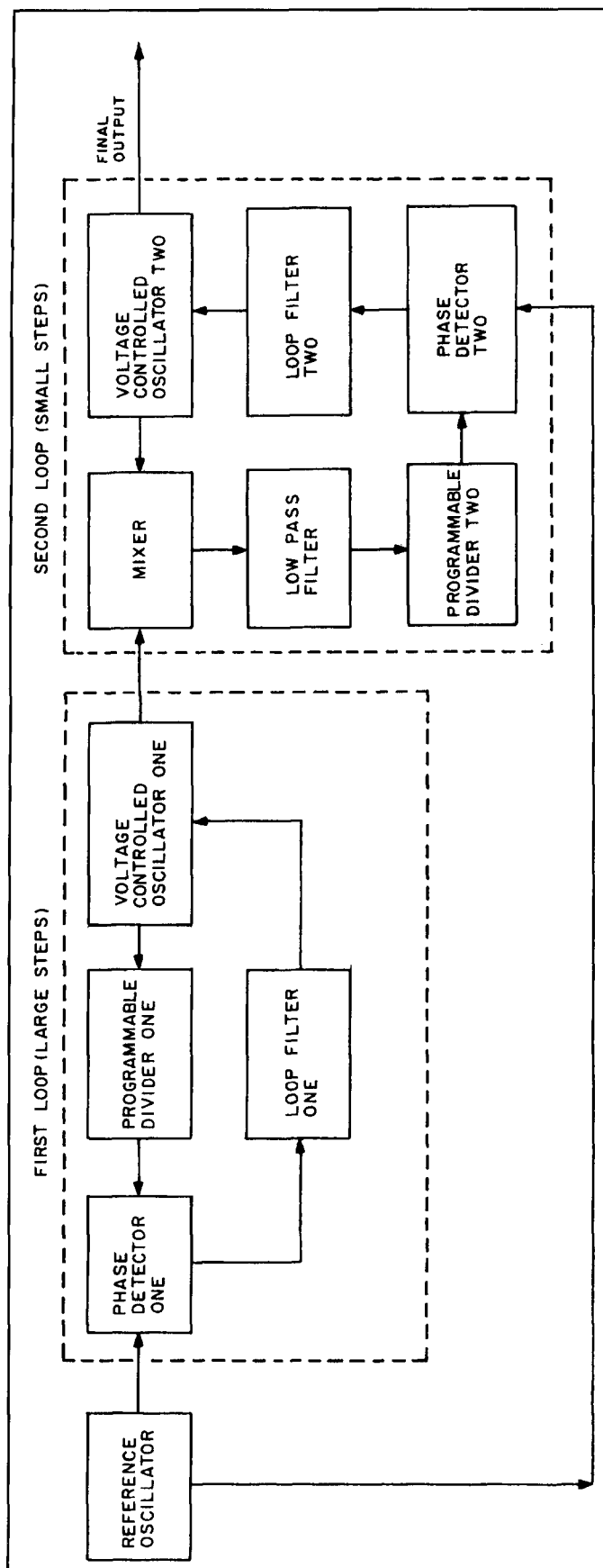


Figure 5. A two-loop synthesizer (see text).

reduce the phase difference between the two signals entering the phase detector.

Eventually, there will be a small and steady phase difference between them. In turn, this means that the frequency of these two signals is the same.

External signal

So, if an external signal is fed into the mixer in the loop, then the VCO will have to run at a frequency which is the sum of the reference and the external signal. To put some figures into the block diagram, take the example of a reference signal of 1 MHz and an external signal of 10 MHz.

For the loop to be in lock, both signals entering the phase detector must be at 1 MHz. In turn, this means that the output from the mixer must be at 1 MHz.

For the loop to be in lock, the oscillator must be running at a frequency of either 9 or 11 MHz. Normally, the oscillator is made to run on the high side of the external oscillator.

The oscillator would be prevented from trying to "lock" onto the image, by restricting the range or "steering" it. In the example I've provided, you can see that if the frequency of the reference oscillator is raised by 1 kHz, then the frequency of the VCO will have to increase by the same amount for the loop to remain in lock.

Similarly, if the reference falls by 1 kHz, the VCO frequency will fall. The same is also true if the external oscillator frequency is varied.

This form of loop is very useful. For example, the frequency of a stable low frequency oscillator (which could even be another synthesizer) can be transferred to a much high frequency.

There are advantages with this technique. It's much easier to have a low frequency synthesizer, with small frequency steps, than making a single loop version with the same steps.

A mixer could be used, but the use of a PLL is much better. This is because a PLL gives much lower levels of spurious signals, and the filtering is much simpler.

In fact the filter (**Figure 4**), is a simple low-pass type. If a mixer was used, a more complicated and expensive bandpass filter would be needed. The use of a PLL offers a wide variety of options to the designer, as he may not just use the second loop in this basic form.

More than one loop

There are many ways in which synthesizers can be made up with more than one loop. The way it's done, will depend upon factors like the use of the synthesizer, its frequency range, and other specifications which may be important.

An example of how a multi-loop synthesizer

can be made up is shown in **Figure 5**. From the diagram, you'll see that comparatively small steps can be achieved without the need for excessively large division ratios in any one loop.

This approach can pay large dividends in several features of the loop, and most noticeably in terms of the phase noise performance which is often very important. By extending the principle shown in **Figure 5**, it's possible to include more loops and achieve even smaller steps.

In fact, many top-of-the-range synthesizers will have up to 10 loops or possibly more. However, synthesizers like these are usually only found in specialized signal generators costing many thousands of pounds.

Loop filter

Having looked at synthesizers in terms of their overall block diagrams, it's worth taking a closer look at the contents of some of the circuits. One of the most important sections of any synthesizer is the loop filter.

The loop filter will govern many of the features of the synthesizer, but it need only contain very few components. One of the obvious functions of this filter is to remove any leakage of the phase detector reference signals on the tune line. A typical loop filter is shown in the diagram of **Figure 6**.

If these signals appear at the input to the VCO, they will give rise to sidebands at the output of the loop. These sidebands will be at an offset from the carrier, equal to the reference frequency as shown in **Figure 7**.

Another important feature of the filter, is that it governs the stability of the whole loop. By assuring proper design of the filter, the loop will remain stable and have a large degree of margin in hand.

However, if the filter components are not chosen correctly, then it's possible for the whole loop to become unstable. If this happens, the tune line will be seen to have a large oscillation on it, giving rise to a wide band frequency modulated signal. When this occurs, the feedback path is around the whole loop, and no single stage is oscillating.

Phase noise

The filter also contributes to the phase noise characteristic of the synthesizer. The reason for this is that noise emanating from different parts of the circuit affect the loop differently, depending upon the filter.

From all this, it can be seen that the choice of the loop filter is very important. As you can imagine with so many features of the synthesizer affected by it, the choice of the filter can be

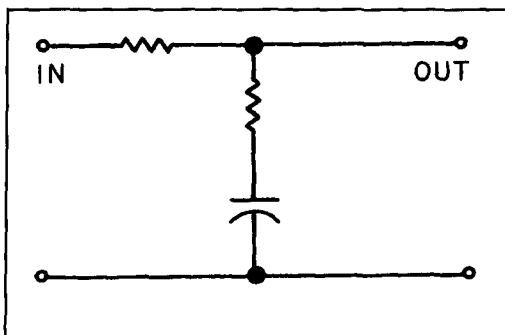


Figure 6. A basic loop filter (see text).

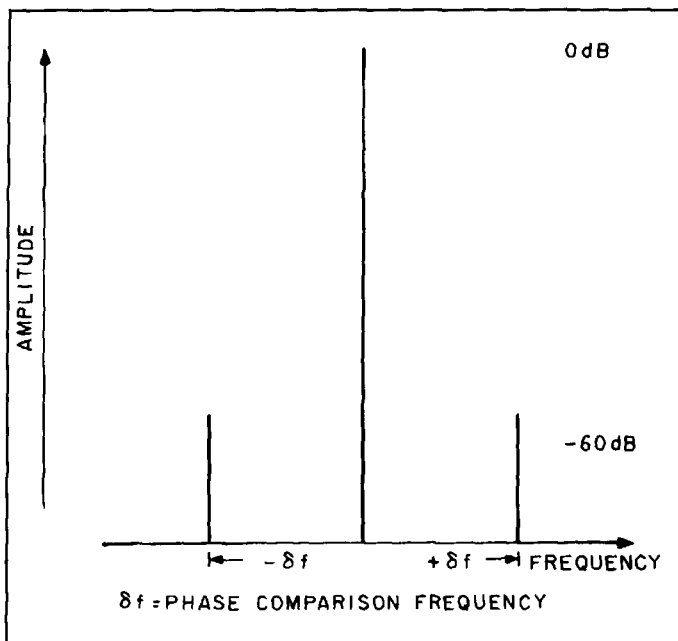


Figure 7. Sidebands at the output of the loop (see text).

something of a compromise. But this is a part of the designer's challenge!

Phase detector

The phase detector is another important circuit block within the synthesizer. There are several different types which vary in complexity, as well as performance.

The simplest type is a mixer. The two signals to be compared are fed into it, and the difference signal comes out.

When the loop isn't in lock, and the two signals are on different frequencies, a signal equal to the difference frequency appears on the tune line. However, when the loop is in lock, the mixer generates a voltage proportional to the phase difference.

Although mixers work well as phase comparators, and are often used at high frequencies where many other types can't work, their operation does have some drawbacks. The main

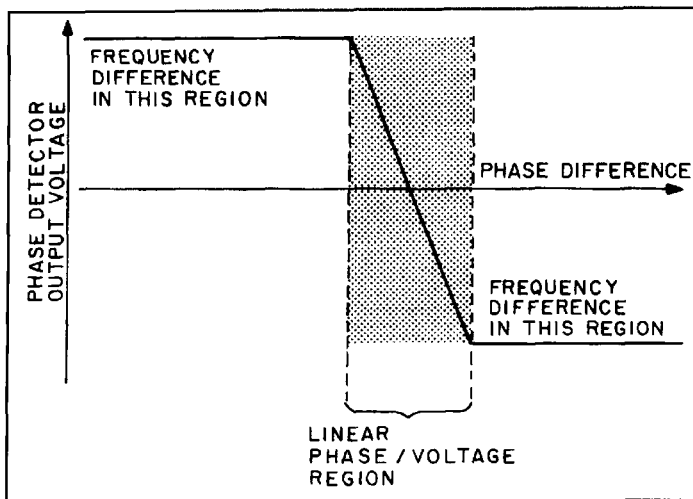


Figure 8. When there is a frequency difference, a fixed voltage is generated (see text).

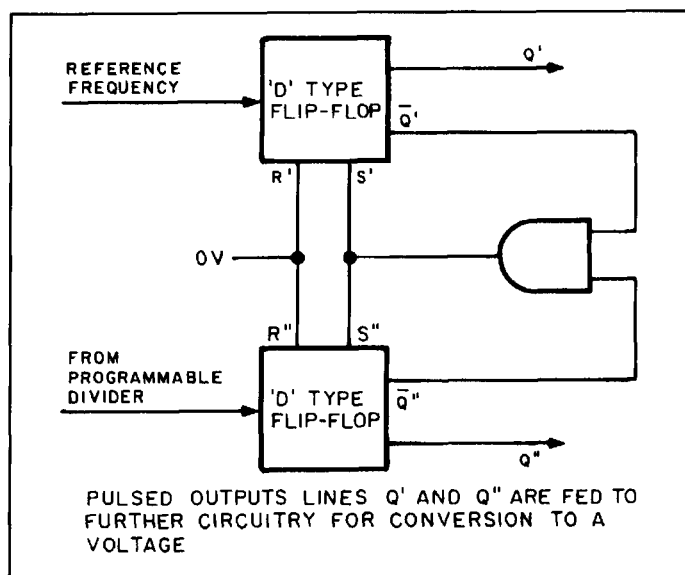


Figure 9. A "dual-D" type phase detector.

problem is seen when the loop is not in lock, and a difference frequency is being generated.

If the difference frequency is outside the passband of the loop filter, no error voltage will be seen on the tune line to the VCO, and the loop will not lock. Then, the loop will only lock when the frequency difference between the VCO and the frequency it should lock onto is less than the passband of the loop filter.

In fact, the range over which the loop will come into lock is known as the capture range. Fortunately, other types of phase detector exist which overcome this problem.

Error voltage

Essentially, the alternatives generate an error voltage which is proportional to the phase

error, when there's no frequency difference. However, when there is a frequency difference, they will generate a fixed voltage, as shown in **Figure 8**.

There are many types of circuit which will fulfill this requirement, and they use digital techniques. The simplest is an OR gate, but the one which has possibly found the most widespread use is in the "dual-D" type phase detector, as in **Figure 9**.

Voltage controlled oscillator

The design of the voltage controlled oscillator (VCO) in any synthesizer is very important. This is because the circuit will have to meet quite stringent requirements.

Meeting the required frequency range, with the available tuning voltage often presents problems. In addition, the phase noise characteristics are always important.

Unfortunately, there are always other requirements. This means that the design of the oscillator is seldom easy!

Although there are many different designs for oscillators, the most commonly used is the standard Colpitts. This is seen whenever a variable frequency oscillator is needed.

In order to make it tune according to the tuning voltage applied, the standard variable capacitor is replaced by a varactor diode arrangement. Normally, this is a couple of diodes, as shown in the back-to-back arrangement in **Figure 10**.

In this arrangement, the series resistor R1 is to provide radio frequency (RF) isolation, so that the oscillator is not affected by the tune line. Its value can be quite high, possibly 10 k or more. This is because the diodes are reverse biased and they don't draw any current.

Although a choke may seem to be a better solution, here this is not always the case. This is because the choke will be reactive, and it could introduce undesirable spurious responses and resonances into the circuit.

The programmable divider

The programmable divider is an integral and important part of the design of any synthesizer. Essentially, it's a circuit whose division ratio is set by a number of programming lines on the integrated circuit (IC).

However, when division ratios become very large, there may not be enough lines available. This can be overcome in a number of ways.

Some synthesizer ICs have their programming data entered in a serial fashion. Others can be connected directly to a microprocessor data bus, and have several bytes of data entered one after another.

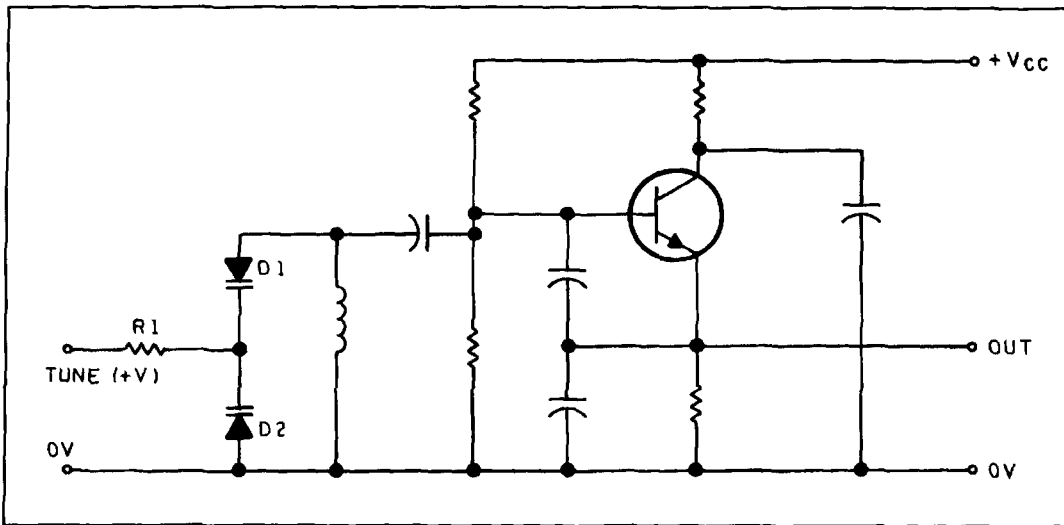


Figure 10. A voltage-controlled oscillator, tuned by a varactor diode.

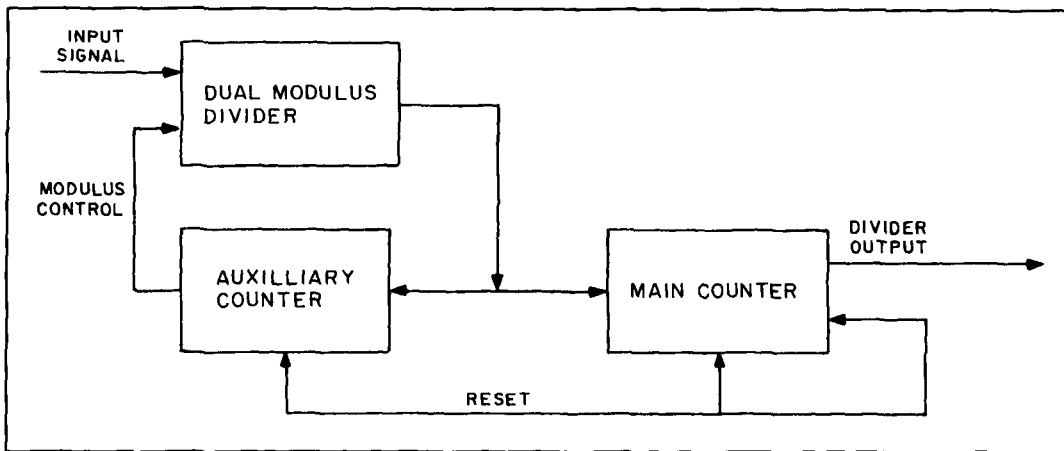


Figure 11. A "swallow counter" (see text).

In fact, this ability for the frequency of a synthesizer to be controlled by a processor, is one of the reasons for their success. Unfortunately, there are a number of problems with the use of programmable dividers.

Too slow

The main problem is simply that the dividers are too slow. They can't operate fast enough. Although fixed dividers can operate very much faster, the fact that a divider is programmable, means that there's much more circuitry inside and it's slower.

There are a number of ways of overcoming this problem. The first and most obvious is to place a fixed divider or prescaler in front of the programmable divider.

This is fine up to a point, because the divider increments in multiples equal to the division

ratio of the prescaler. In turn, this means that the step size is increased in the same ratio as the division ratio of the prescaler.

In other words, if a prescaler had a division ratio of four, and the phase detector frequency was 25 kHz, then the step size with the prescaler in circuit would be 100 kHz. This is obviously not satisfactory in most cases.

Swallow counter

To overcome the divider difficulty, a more complicated circuit often called a "swallow counter," employing a dual modulus divider, can be used. Essentially, a dual-modulus counter is a prescaler which can switch between two division ratios such as 10 and 11.

Generally speaking, a circuit similar to the block diagram shown in **Figure 11** is used. As before, there's a main counter after the

prescaler, but there's also an auxiliary counter, which controls the division ratio of the dual modulus counter.

By using this system, it's possible to count in steps equal to the phase comparison or reference frequency. The auxiliary counter is set to a division ratio less than the main one.

Initially, the dual modulus counter will be set to divide by one of its ratios, and its output will be fed into both of the other counters, which in turn will start to divide. The first counter to have a change in its output state will be the auxiliary counter, and this will change the division ratio of the dual modulus counter.

This alters the rate at which pulses enter the main counter. The overall effect of the three

counters is to give a counter which increments in single steps rather than multiples.

Although the operation of this system may seem a little complicated, it operates very satisfactorily and it's widely used in synthesizers operating over a few megahertz.

Summary

Frequency synthesizers are a part of the amateur radio scene. Whether you love or hate them, it can't be disputed that they offer many advantages over other systems for generating stable and controllable frequencies. I hope that now that we've taken a closer look, you'll be a bit more familiar with the modern synthesizer.

PRODUCT INFORMATION

QUALCOMM Introduces Low Power 2.0 GHz Phase-Locked Loop Frequency Synthesizer

QUALCOMM Incorporated has announced its new Q3236 Phase-Locked Loop (PLL) Frequency Synthesizer, a high speed, low power, single-chip solution for high performance communications systems. The Q3236 combines low power consumption and ultra-low phase noise to allow communications engineers to customize their designs.

The Q3236 can be used in a variety of applications including cellular and paging base stations, frequency hopping systems, digital radios and modems, lab instrumentation and local oscillators for Very Small Aperture Terminals (VSAT), Direct Broadcast by Satellite (DBS), Global Positioning Systems (GPS), and radar. The Q3236 requires less than 0.6 Watts of nominal power and has an operating speed of up to 2 GHz. It has three programmable control interface options including direct parallel, 8-bit bus and serial loading. Included on the chip is a high gain linearized phase/frequency detector operating to 100 MHz and divide-by 10/11 dual-modulus prescaler with

programmable feedback divider. These features allow PLL designs to have small Voltage-Controlled Oscillator (VCO) division ratios to optimize synthesizer phase noise performance.

Using a single +5 Volt power supply, the Q3236 contains all of the necessary elements, with the exception of the VCO and loop filter components, to build a PLL Frequency Synthesizer operating from UHF through L-Band. The Q0410 and Q0420 PLL evaluation boards are also available for either fixed demonstration or custom prototyping.

For more information, contact QUALCOMM Incorporated, 6455 Lusk Boulevard, San Diego, CA 92121; phone 619-587-1121; fax 619-452-9096.

HP Expands its HP 8648 Family of Signal Generators

Hewlett-Packard Company has introduced their low-cost, 4 GHz synthesized model that gives designers and manufacturers an affordable way to test new, higher-frequency RF communication-system components.

This new signal generator offers a frequency coverage of 9 kHz to 4 GHz, and can be used for general-purpose receiver testing, personal communication systems, wireless local area networks and fixed-radio access. The 8648D signal generator is also available with an optional variable-modulation generator which expands audio-band testing by adding variable 10 Hz to 20 kHz modulation with different shapes, including triangle, square and sawtooth.

For further information, contact Hewlett-Packard Company, Direct Marketing Organization, P.O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; or call 1-800-452-4844 ext. 1491; or on the World Wide Web at <http://www.hp.com>.



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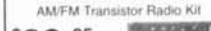


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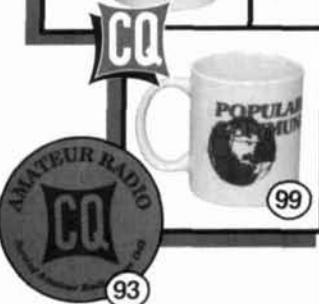
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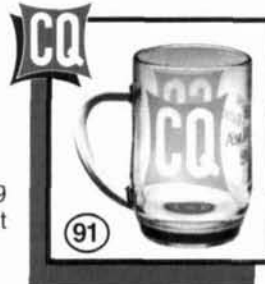


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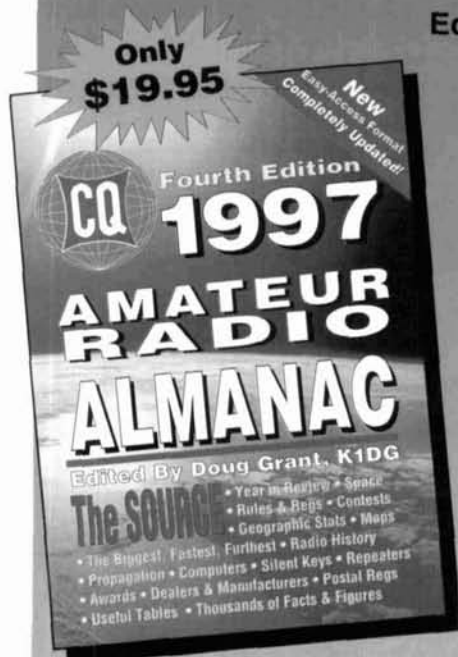


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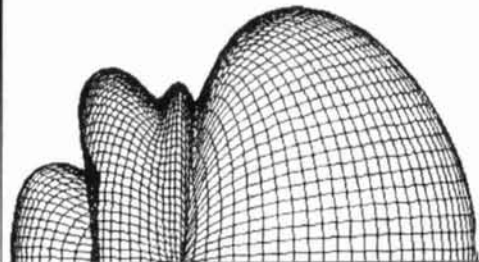
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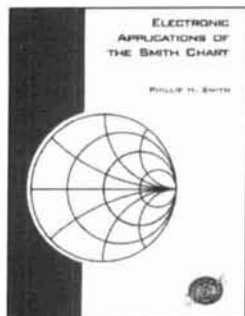
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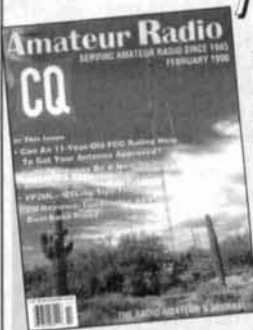
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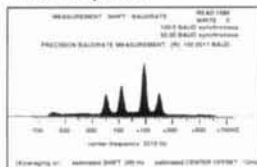
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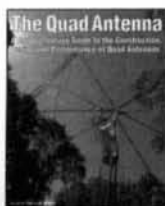
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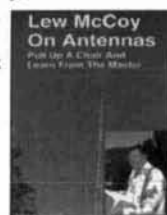


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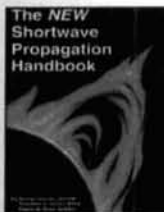


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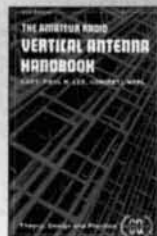
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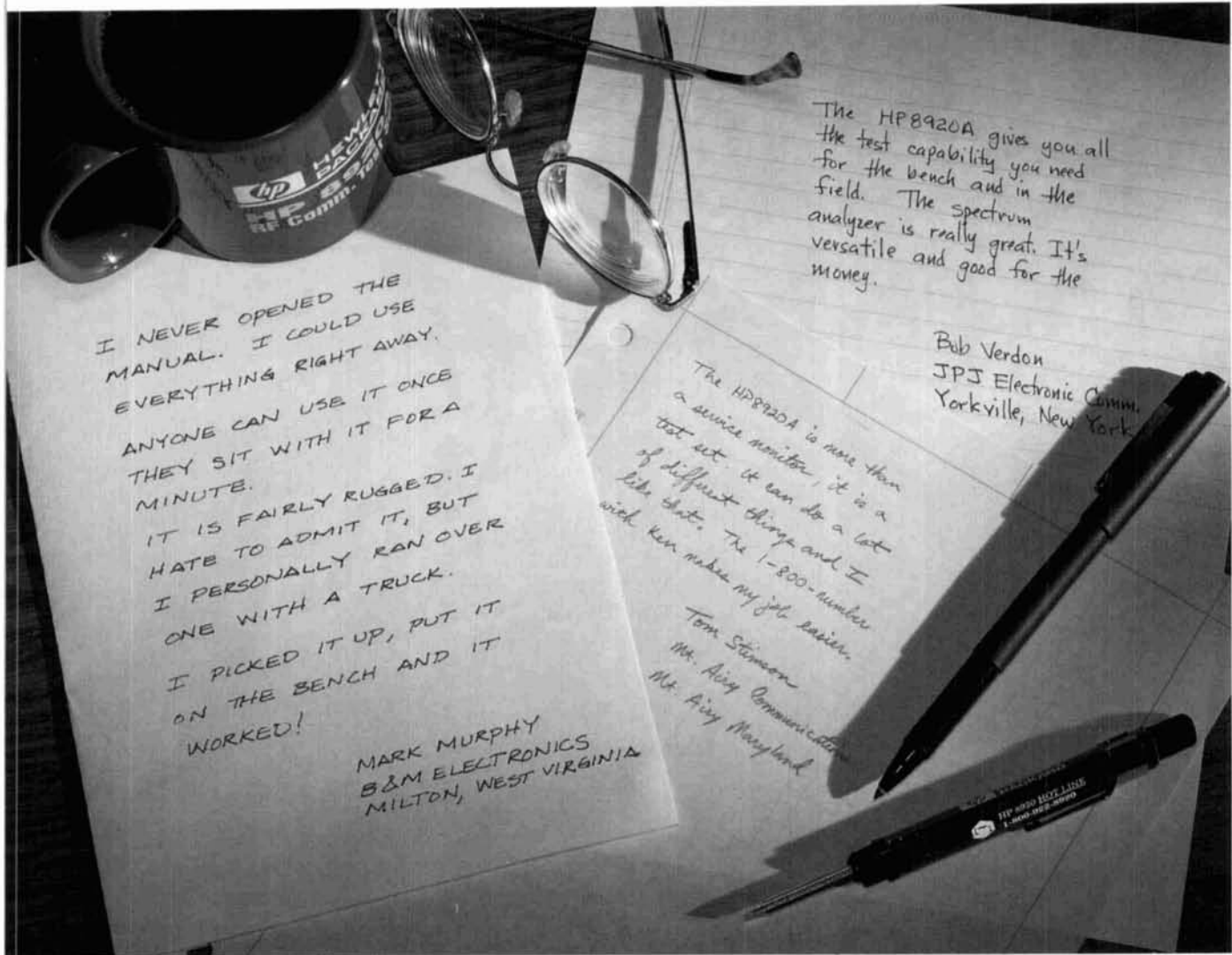
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