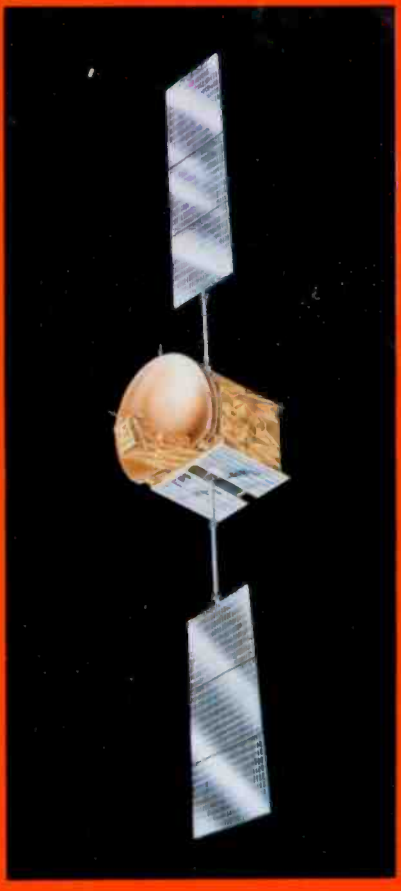
# RCA Review



Improving Reliability

June 1984

Volume 45, No. 2

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A hermetically sealed leadless chip package is shown on the left on our cover with the lid on and without the lid with an IC in place. This type of high-reliability device is extensively used in military and aerospace applications. Shown on the right is an advanced Satcom satellite of the type discussed by Mancino and Slusark in their paper on communications satellite reliability.

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RCA Review

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## Contents



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# Foreword to Special Issue on Reliability

The cost-effective achievement and verification of reliability objectives is of vital and continuing importance in maintaining a leadership position in electronics. Accordingly, successful electronic companies apply major efforts toward assessing and improving product reliability, as well as performance, quality and safety. High product reliability is achieved by understanding the manufacturing process, and by use of suitable designs, materials, processes, and tests to insure that the product will meet or exceed the requirements of the application.

This issue of RCA Review contains seven invited papers on various aspects of the reliability of electronic components and systems. These papers, written by technical specialists in their fields, are expected to be primarily of interest to other technical specialists concerned with the effects of designs and manufacturing technology on electronic device and equipment reliability. The articles provide information on reliability of integrated circuits ranging from plastic-encapsulated ICs for commercial applications to high-reliability ICs for military and aerospace systems. They also include a discussion of techniques for attaining high reliability in a satellite communications electronic system in which a 10-year design life is required.

The topics included in this issue represent a small fraction of the total RCA effort on improving the reliability of products. As might be expected, the subjects selected reflect, to some extent, the interests of the guest editor.

The contributions of a large number of RCA personnel to the preparation of this special issue are gratefully acknowledged, including the scientists, engineers and associates who performed the experimental studies, and also those who assisted in the preparation and editing of the manuscripts. The efforts of those who served as technical reviewers of the manuscripts are also very much appreciated.

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# Reliability Characterization of High-Speed CMOS Logic ICs

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**Abstract**—Information is presented on the reliability testing of new high-speed CMOS devices known commercially as QMOS. The reliability characterization of the early development product is discussed and data is presented on more than 10,000 plastic-packaged devices tested under accelerated stress conditions during and after product qualification. The data generated demonstrate a final plastic-packaged product with exceptionally good reliability as compared with the more mature LSTTL technology. Data is also presented to show excellent stability under extreme mechanical and environmental stresses.

## 1. Introduction

The RCA high-speed CMOS technology, introduced in 1983 and known commercially as QMOS, includes an extensive line of products that are pin compatible with many existing bipolar 54/74 LSTTL and CMOS 4000-series digital-logic types. The new devices provide replacements for the most popular LSTTL devices in existing designs and also offer low-power all-CMOS designs for new digital systems. The two series (HC and HCT) of CMOS high-speed-logic integrated circuits are based on 3-micron minimum feature size and self-aligned, polysilicon-gate technology; the structure is illustrated in Fig. 1.

HCT-series devices are direct, drop-in replacements for 54/74-series LSTTL devices, and can be intermixed with any TTL devices. They operate at the same speed as LSTTL devices (eight nanosecond typical gate propagation delay) and, simultaneously, offer the classical CMOS advantages, such as low power dissipation, low power consumption (1/2000 that of LSTTL in the quiescent state), wide

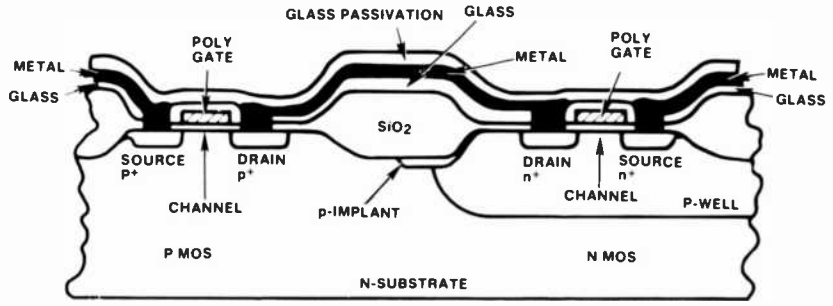


**Fig. 1**—Basic structure of high-speed CMOS logic devices.

operating-temperature range ($-40$°C to $+85$°C for plastic-package types), noise immunity twice that of LSTTL at 5V, and improved output-drive capability. The HC-series devices operate at CMOS logic levels and are ideal for all-CMOS designs.

As with any new technology, the reliability of high-speed CMOS logic had to be demonstrated. This paper discusses the reliability characterization of the early developmental product, and presents data on more than 10,000 plastic-packaged devices tested under accelerated stress conditions during and after final product qualification. The results show conclusively that the high-speed CMOS technology is a reliable one, even when compared to the mature LSTTL products.

## 2. Reliability Characterization During Product Development

A number of reliability studies were conducted during the early stages of product development in order to characterize the device structure and process from a reliability standpoint. The stress tests used to perform these studies were accelerated significantly above normal application conditions to uncover all possible device limitations that could adversely effect the reliability of the product. Once detected, these limitations were addressed and corrected prior to full-scale factory introduction.

One limitation, which was observed in early samples under accelerated static bias-life conditions, was a positive shift in p-channel threshold voltage $V_{TP}$. The increase in $V_{TP}$ over time for three different accelerated bias-life temperatures is shown in Fig. 2. The bias circuit for the developmental type used to generate these results is diagrammed in Fig. 3. Fig. 4 shows an Arrhenius plot of these

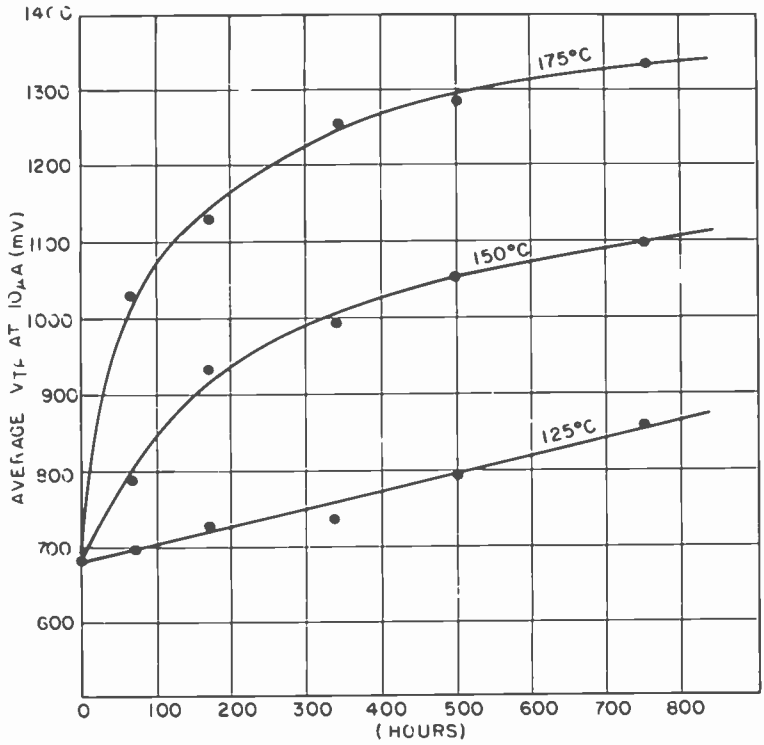


**Fig. 2**—Plot of average $V_{TP}$ shift over time on static bias-life test at 6V for three temperature conditions ($N$ = 20 per cell).

data for a 200-mV change in $V_{TP}$. The estimated activation energy is 1.05 eV. This value was determined from the slope of the line and is the energy that characterizes the temperature dependence of the reaction rate of the $V_{TP}$ shift mechanism.

Shifts in threshold voltage $V_T$ have been known to occur under bias at elevated temperatures in MOS devices.[1–7] They are caused primarily by movement of charge in the oxide at or near the silicon/oxide interface. These shifts can cause a degradation in circuit timing that can adversely affect device performance.

Several mechanisms are identified with this phenomenon. Perhaps the best known is mobile ion contamination.[2,3] Ions trapped within the gate oxide (or entering it from the surrounding areas) can drift, under conditions of bias voltage and high temperature, and disturb the balance of charge at the silicon-oxide interface. This mechanism is normally controlled through the use of clean processing and phosphorus gettering techniques. Another well-

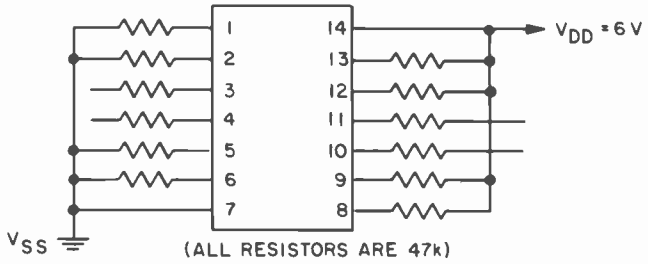


**Fig. 3**—Static bias-life circuit for RCA developmental test vehicle TA11405 (quad 2-input NAND gate). 1,2,5 and 6 tied to ground ($V_{SS}$) and inputs 8,9,12 and 13 tied to $V_{DD}$ = 6V.

known mechanism is the so-called slow-trapping instability.[2,5] Although the precise cause of this mechanism is still uncertain, it has been attributed to hole-trapping in the oxide or to field-induced dissociation of an additional Si bond in partially ionized Si atoms near the silicon-oxide interface. It has been shown that this mechanism can be controlled through high-temperature oxide-annealing steps.[3,5] Other mechanisms identified with $V_T$ instability include

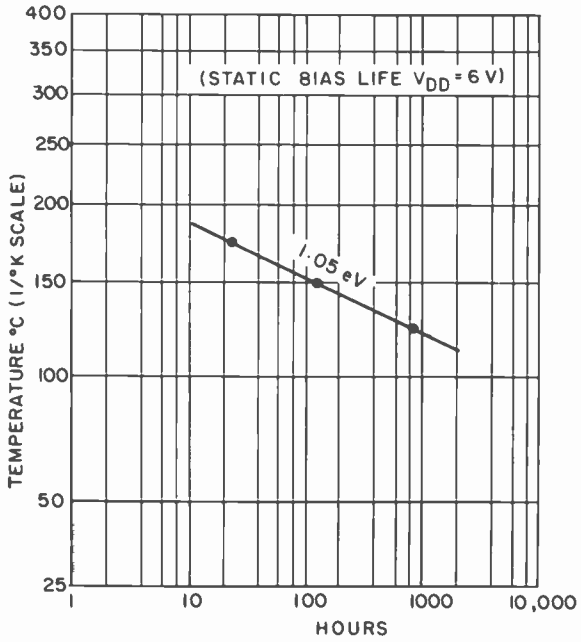


**Fig. 4**—Time to average $\Delta V_{TP}$ = +200 MV for plastic molded device. Activation energy is 1.05 eV.

surface-charge spreading and hot-electron injection.[2] Last, $V_T$ instability has been found to be accelerated by the diffusion of moisture and/or impurities from the epoxy plastic package material.[1,6]

Experiments conducted on the developmental high-speed CMOS devices tended to incriminate package-related impurities as the main cause of the observed $V_{TP}$ instability. Tests were conducted on epoxy-molded devices (using two different molding compounds), ceramic-packaged devices with epoxy-mounted pellets, and ceramic-packaged devices with AuSi eutectically-mounted pellets (no epoxy present). The same pellet lot was used in each case. A plot of the $V_{TP}$ shift as a function of time and package variants is shown in Fig. 5 for a test temperature of 175°C. The figure shows that the AuSi-mounted pellet (no epoxy) in the hermetic ceramic package was very stable in comparison to similar pellets mounted in several epoxy-package variants; this result indicates that the presence of the epoxy in some way affected the $V_{TP}$ stability.

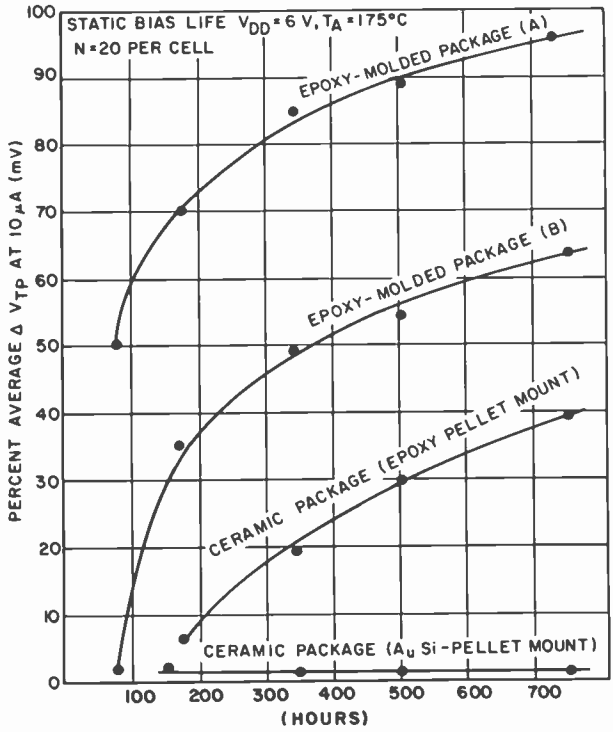


**Fig. 5**—Plot of percent average $V_{TP}$ shift versus time at 175°C for four package variants using the same pellet lot.

It should also be noted that a pellet epoxy-mounted in a ceramic package exhibited less $V_{TP}$ shift than either of the pellets in the epoxy-molded packages but significantly more shift than a pellet mounted in the ceramic package with a nonepoxy technique. Gas mass-spectrographic analysis of the internal package environment revealed a moisture content in the order of 40,000 ppm, indicating probable moisture outgassing of the epoxy mounting material. The difference in rate of $V_{TP}$ shift between the two molding compounds was attributed to possible differences in the moisture and/or impurity levels of each.

It is of interest to note that the activation energy of 1.05 eV, presented earlier, is similar to that reported by M. Noyori, et al[7] for moisture-induced $V_T$ instability. In a paper by L. Gallace[1] and another by M. Noyori,[6] data are presented which strongly suggest that the $V_T$ shifts observed in plastic-encapsulated, PSG-passivated, polysilicon-gate CMOS devices is caused by diffusion of moisture from the epoxy molding material.

$V_{TP}$ instability was eliminated through the use of a high-temperature silicon nitride ($Si_3N_4$) layer deposited over the polysilicon gate, a technique that has been used successfully in other polysilicon-gate technologies.[1] The $Si_3N_4$ layer provides a barrier to the diffusion of moisture and ionic contaminants, and is currently used in all RCA high-speed CMOS devices. Data demonstrating the stability of plastic-molded high-speed CMOS devices employing the high-temperature nitride barrier layer are shown in Fig. 6. A second method that demonstrated excellent results in preventing $V_{TP}$ shifts, but one that has not yet been used in production, involves the use of a plasma-enhanced silicon nitride overcoat. This overcoat is employed in place of the phosphosilicate glass (PSG), or over a layer of PSG, and eliminates the need for the $Si_3N_4$ barrier layer. Fig. 7 demonstrates the stability of both silicon nitride methods relative to the instability of product without a nitride layer.

## 3. Reliability Data from Production Samples

Once the design rules, wafer-fabrication process, and assembly process were finalized, the high-speed CMOS technology was ready to be qualified from a reliability standpoint prior to full-scale factory introduction. The reliability test plan used for the basic technology qualification, completed in May, 1983, is shown in Table 1. These tests were continued on production samples as new types were introduced. To date, 49 high-speed CMOS types, amounting to a total

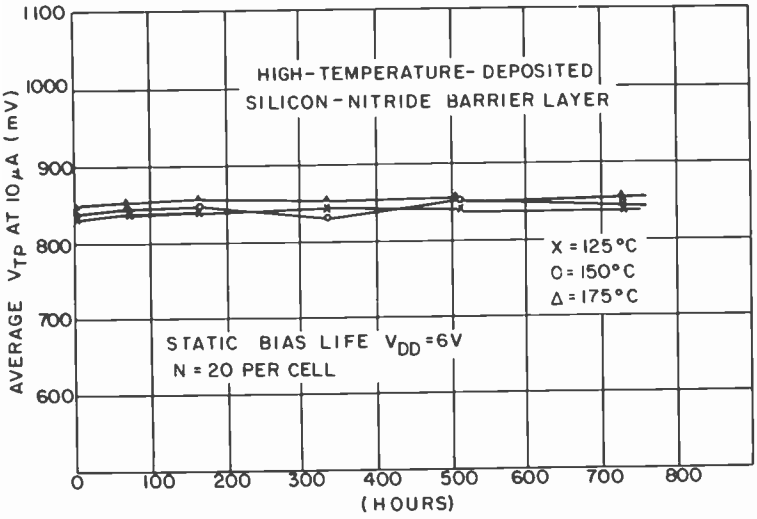


**Fig. 6**—Plot of average $V_{TP}$ versus time, demonstrating the stability resulting from the use of the high-temperature-deposited nitride ($Si_3N_4$) barrier layer at accelerated temperatures in the epoxy-molded package.

of 10,731 devices, have undergone reliability evaluation. The test results are discussed in the sections that follow.

## 3.1 Life-Test Results

Life tests are performed at elevated temperatures and maximum-rated voltage in order to accelerate time-dependent failure mechanisms related to conditions of temperature and electrical stress. Life testing is the principal method used in predicting the failure rates of components in actual field applications.

Results of accelerated static bias-life tests, as performed at temperatures of 125°C, 150°C, and 175°C, are given in Table 2. The maximum specified temperature rating for these devices in the plastic dual-in-line package is 85°C. Thus, the tests performed are significantly in excess of this rating. The static test biases the devices in the off condition, so that no current flows from $V_{DD}$ to ground ($V_{SS}$). The resulting electric field accelerates leakage-current mechanisms associated with a concentration of mobile ions in and under the various dielectric layers. Leakage-current mechanisms are considered the most prevalent life-related mechanisms in MOS technology devices. Other mechanisms, such as time-depen-

Table 1—High-Speed CMOS Technology Qualification:* Accelerated Reliability Test Matrix

| Test | Condition | Minimum Duration | Sample Size | Accept Failure Number |
|---|---|---|---|---|
| Static Life | 125°C, $V_{DD}$ = 6V | 1000 Hrs | 50 | 1 |
| Accel. Static Life | 150°C, $V_{DD}$ = 6V | 1000 Hrs | 50 | 1 |
| Accel. Static Life | 175°C, $V_{DD}$ = 6V | 168 Hrs | 80 | 1 |
| Dynamic Life | 125°C, $V_{DD}$ = 6V | 1000 Hrs | 50 | 1 |
| Temp/Humidity/Bias | 85°C/85% RH/6V | 1000 Hrs | 20 | 0 |
| Temp/Humidity/Bias | 93°C/98% RH/6V | 240 Hrs | 20 | 0 |
| Pressure Cooker | 15 psig, 121°C | 192 Hrs | 25 | 0 |
| Thermal Shock | −65°C to +150°C | 1000 Cyc | 50 | 1 |
| Temperature Cycle | −65°C to +150°C | 1000 Cyc | 50 | 1 |
| Storage Life | 150°C | 1000 Hrs | 20 | 0 |

* Approval of technology was based on meeting the above criteria on a minimum of three production lots.

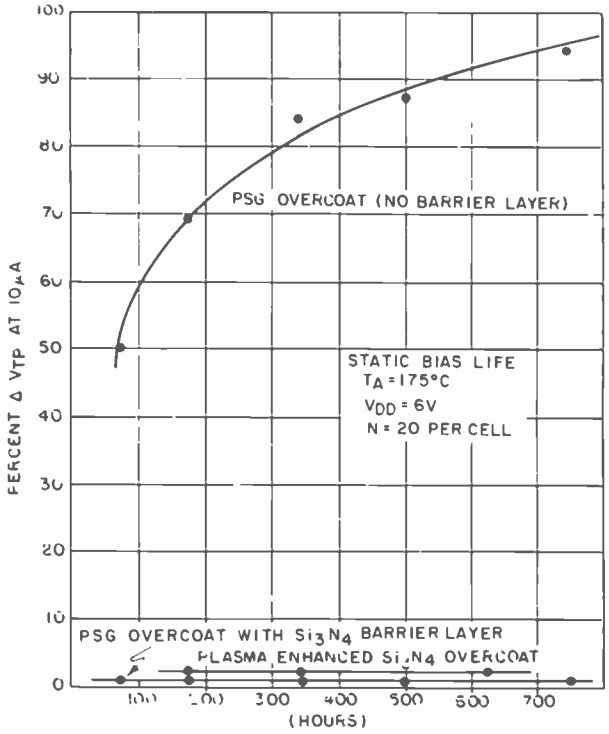


**Fig. 7**—Plot of percent average $V_{TP}$ shift over time at 175°C for the two silicon nitride systems versus product without $Si_3N_4$ in the epoxy-molded package.

Table 2—Static Bias Life Test

| *Test Conditions:* $T_A$ = 125°C, $V_{DD}$ = 6V | | | | | | |
|---|---|---|---|---|---|---|
| Lots | Quantity | Hours | | | | |
| 31 | 1753 | 168 | 500 | 1000 | 1500 | 2000 |
| Quantity Per Downtime | | 1753 | 1750 | 1702 | 921 | 861 |
| Outside Specification* | | 3† | 0 | 0 | 0 | 1† |
| Total Device-Hours = 2,617,504 | | | | | | |
| *Test Conditions:* $T_A$ = 150°C, $V_{DD}$ = 6V | | | | | | |
| Lots | Quantity | Hours | | | | |
| 6 | 385 | 168 | 500 | 1000 | 1500 | 2000 |
| Quantity Per Downtime | | 385 | 385 | 385 | 267 | 267 |
| Outside Specifications* | | 0 | 0 | 0 | 0 | 0 |
| Total Device-Hours = 652,000 | | | | | | |
| *Test Conditions:* $T_A$ = 175°C, $V_{DD}$ = 6V | | | | | | |
| Lots | Quantity | Hours | | | | |
| 35 | 3039 | 168 | 336 | 500 | | |
| Quantity Per Downtime | | 3039 | 356 | 116 | | |
| Outside Specification* | | 5† | 0 | 0 | | |
| Total Device-Hours = 589,384 | | | | | | |

* Criticized to data-sheet limits
† Parametric drift (bake recoverable)

dent dielectric breakdown and slow-trapping instability,[7] can also be accelerated by this test.

The dynamic life-test data are shown in Table 3. This test stresses the devices in the on condition with an ac signal applied to the inputs. Like the static bias-life test, this test also accelerates mobile-ion movement, but to a lesser degree. The dynamic life test is more effective in detecting imperfections in the metallization and oxide layers than the static test, and more nearly simulates actual application conditions.

The ten parametric-drift failures observed on the combined tests were primarily leakage-current related, and recovered within specification limits after a 150°C, 24-hour bake. This bake-recovery effect suggests that this phenomenon is attributed to a mobile-ion

**Table 3—Dynamic Life Test**

Test Conditions: $T_A$ = 125°C, $V_{DD}$ = 6V

| Lots | Quantity | Hours | | | | |
|---|---|---|---|---|---|---|
| 20 | 1189 | 168 | 500 | 1000 | 1500 | 2000 |
| Quantity Per Downtime Outside Specification* | | 1189<br>1† | 1189<br>0 | 1189<br>0 | 457<br>0 | 457<br>0 |
| Total Device Hours = 1,646,000 | | | | | | |

* Criticized to data sheet limits.
† Parametric drift (bake recoverable).

condition. The established activation energy for this mechanism[8] is in the neighborhood of 1.0 to 1.4 eV.

Based on these results, an activation energy value of 1.0 eV was assumed for predicting the failure rate at the lower temperatures. These predictions are shown in Fig. 8 as a function of temperature and in Table 4 for both the maximum-rated temperature of 85°C and nominal-use condition of 55°C. The calculated 85°C failure rate (%/1000 at 60% UCL) for the LSTTL technology is 0.008; for high-speed CMOS devices from RCA and two other major manufacturers, the failure rates are 0.0019, 0.0086, and 0.0039, respectively. These values were calculated by extrapolation of published test data[9–11]

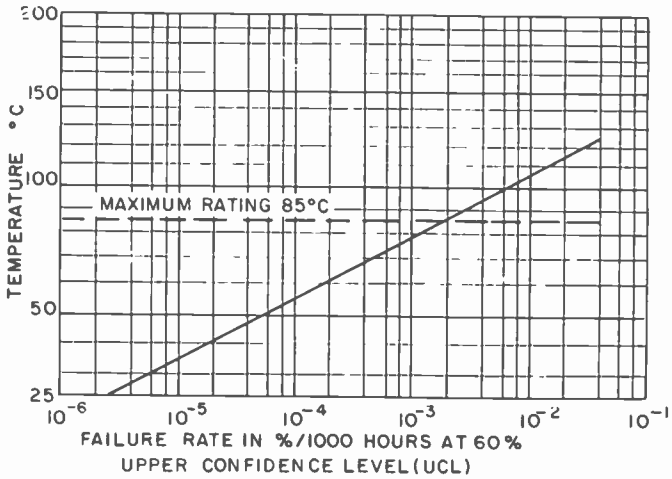


**Fig. 8**—Plot of failure rate versus temperature for plastic-molded high-speed CMOS logic based on 1.0-eV extrapolation of accelerated-test data.

Table 4—Failure Rate Estimation at Maximum-Rated (85°C) and Nominal Use (55°C) Temperature (Activation Energy = 1 eV is Assumed)

| Condition | Total Devices Tested | Devices Outside Spec. | Equivalent Device Hrs | | Failure Rate %/1000 Hrs @ 60% UCL | |
|---|---|---|---|---|---|---|
| | | | 85°C | 55°C | 85°C | 55°C |
| Static | 5177 | 9 | $5.5 \times 10^8$ | $1.0 \times 10^{10}$ | .0019 | .0001 |
| Dynamic | 1189 | 1 | $4.2 \times 10^7$ | $8.1 \times 10^8$ | .0047 | .0002 |
| Combined | 6366 | 10 | $6.0 \times 10^8$ | $1.08 \times 10^{10}$ | .0019 | .0001 |

using an activation energy of 1.0 eV. As can be seen, the RCA failure rates derived from the data presented in this paper compare very well with LSTTL and extremely well with the product of other suppliers of high-speed CMOS ICs. The product used to develop the failure rates in Table 4 received no burn-in or stress-test screening to remove possible infant failures prior to being subjected to life testing. Thus, these failure rates are for commercial-grade product.

In addition to the life tests described above, a nonbiased high-temperature-storage test was performed at 150°C on 130 devices. This test stresses the devices from the standpoint of temperature alone. No failures were encountered on this test in a 1,000-hour period.

## 3.2 Moisture-Test Results

Moisture tests are conducted to determine the susceptibility of the plastic-packaged device to moisture penetration. The primary path of moisture ingress is at the lead-frame/plastic interface. Once moisture reaches the chip surface in the presence of certain contaminants, an electrolytic cell can form, resulting in corrosion of the aluminum. The two stress tests commonly used to evaluate the moisture capability of plastic-encapsulated devices are temperature-humidity-bias (THB) and pressure-cooker tests.

In the THB test, devices are placed in a chamber under rated bias-voltage at a specified relative humidity and temperature. The bias condition is static rather than dynamic to assure that little or no power is dissipated by the device under test; dissipation can cause a temperature rise in the chip above that of the ambient. Temperatures significantly above the ambient can drive moisture away from the chip surface, reducing the intended stress. The test conditions most often used in the industry consist of a temperature of 85°C, a relative humidity (RH) of 85%, bias voltage in accordance

Table 5—Temperature-Humidity-Bias Test (THB)

| Test Conditions: $T_A$ = 85°C, RH = 85%, $V_{DD}$ = 6V | | | | | |
|---|---|---|---|---|---|
| Lots | Quantity | Hours | | | |
| 11 | 218 | 168 | 500 | 1000 | 7000 |
| Quantity Per Downtime | | 218 | 218 | 218 | 20 |
| Outside Specifications* | | 0 | 0 | 0 | 0 |

* Criticized to data-sheet limits

with the maximum rating, and a test duration of 1,000 hours; this is commonly referred to as an "85/85" test. The data obtained under the 85/85 conditions are shown in Table 5. No corrosion-related failures have occurred on this test, with one sample tested to 7,000 hours.

In addition to the 85/85 test, a more accelerated, shorter-duration THB test performed at 93°C and 98% RH was employed (93/98 test); this test provides a 4.5 acceleration over the 85/85 test.[12] The data shown in Table 6 are for a 93/98 test duration of 216 to 240 hours, which is approximately equivalent to 1,000 hours of 85/85 testing.

Pressure-cooker testing involves placement of the devices just above the water level in a pressure-cooker chamber. A pressure of 15-psi above normal atmospheric pressure is then applied. This pressure corresponds to a relative humidity of 100% (saturated steam) and a temperature of 121°C inside the chamber. The pressure-cooker test provides a method of rapidly forcing moisture into the package and, in this respect, is more accelerated than the THB test. The mechanisms brought out by this test are similar to those of THB, except that the bond-pad area (rather than the inboard metallization) tends to be the primary area affected. Extensive data

Table 6—Accerated Temperature-Humidity-Bias Test (THB)

| Test Condition: $T_A$ = 93°C, RH = 98%, $V_{DD}$ = 6V | | |
|---|---|---|
| Lots | Quantity | Hours |
| 18 | 430 | 216 – 240 |
| Outside Specification* | | 3† |

* Criticized to data-sheet limits
† Parametric drift (no corrosion)

Table 7—Pressure-Cooker Test

Test Conditions: 15 psi, 121°C

| Lots | Quantity | Hours | | | | |
|---|---|---|---|---|---|---|
| 23 | 1182 | 48 | 96 | 144 | 192 | |
| Quantity Per Downtime | | 1182 | 1182 | 1182 | 1007 | Total |
| Outside Specification* | | 1 | 2 | 1 | 3 | 7† |

* Criticized to data-sheet limits
† Parametric drift (no corrosion)

collected on this test, and displayed in Table 7, show no corrosion-related failures.

## 3.3 Thermal-Cycling Results

Because of the differences in the thermal-expansion properties of the materials used in the construction of the molded plastic package, sudden and extreme changes in temperature can produce stress within the package. This stress can affect the bond-wire integrity and crack the die or glass protect layer. However, with improvements in the manufacture of plastic-packaged devices over recent years, susceptibility to these types of failure modes has been significantly reduced, if not eliminated, particularly under application conditions. These improvements have been accomplished through the use of better plastics, which provide a closer thermal match to the package materials, and fully automated assembly processing.

One test used to characterize the capability of a device to withstand extreme thermal-cycling stress is thermal shock. To induce thermal shock, devices are submerged in an inert, hot (150°C) fluorocarbon liquid for a specified time, and then immediately transferred to a cold (−65°C) fluorocarbon liquid for an equal period of time. These conditions represent an acceleration of stress significantly beyond application levels. The data in Table 8 show that only two parametric drift failures (noncatastrophic) occurred in over 1,300 devices started on this test.

The second thermal-test method employed is temperature cycling. In this method, devices are transferred from hot-air (150°C) to cold-air (−65°C) chambers, instead of liquid baths as in the thermal-shock test. In addition, the cycle duration (20 to 30 minutes) is longer than that used in the thermal-shock test. The data in Table

Table 8—Thermal Shock Test

Test Conditions: $T_A$ = −65°C to +150°C, liquid-to-liquid, 10-sec transfer, MIL-STD 883, Method 1011.2

| Lots | Quantity | Number of Cycles | | | | |
|---|---|---|---|---|---|---|
| 33 | 1320 | 200 | 500 | 1000 | 1500 | 2000 |
| Quantity Per Downtime | | 1320 | 1020 | 870 | 75 | 50 |
| Outside Specifications* | | 0 | 0 | 2† | 0 | 0 |

* Criticized to data-sheet limits and hot continuity (125°C).
† Parametric drift

9 show that no failures were detected until the downtime following 1,000 cycles, which apparently approximates the point at which bond-wire wearout begins. The fact that no failures occurred prior to this number of cycles assures product capability under normal application conditions, which are significantly less severe than those used during testing.

## 4. Conclusion

The data presented in this paper demonstrate the effect of the extensive testing of high-speed CMOS product at stress levels significantly greater than the conditions the product would meet in typical applications. More than 10,000 fully qualified production samples were examined and the resulting data shows that high-speed CMOS devices possess a high standard of reliability, a standard that compares very favorably with that of the widely used, more mature LSTTL products and with the reliability figures of other high-speed CMOS suppliers.

Table 9—Temperature Cycle Test

Test Conditions: $T_A$ = −65°C to +150°C, air-to-air chambers, 20 to 30 minute dwell time, MIL-STD 883, Method 1010.3

| Lots | Quantity | Number of Cycles | | |
|---|---|---|---|---|
| 29 | 1085 | 200 | 500 | 1000 |
| Quantity Per Downtime | | 1085 | 755 | 480 |
| Outside Specification* | | 0 | 0 | 5† |

* Criticized to data-sheet limits and hot continuity (125°C).
† Continuity

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# Dielectric Integrity of the Gate Oxide in SOS Devices†

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**Abstract**—Circuits fabricated in CMOS/SOS are very attractive for applications that require complex, high-density designs and that have special performance requirements, such as speed and radiation tolerance. In the case of an isolated-mesa SOS technology, the dielectric integrity of the channel oxide can be a key reliability issue, especially as device size and oxide thickness are reduced. In this paper dielectric integrity is described in terms of gate-oxide leakage current and catastrophic breakdown. The significance of the island edges and certain process modifications in the determination of channel-oxide dielectric integrity are discussed in detail. It is suggested that high-temperature processes enhance dielectric integrity because of a mechanism associated with stress relief and viscous flow in silicon dioxide. Various topographical modifications that increase dielectric integrity are described. Based upon the characterization of large arrays of SOS structures with oxides as thin as 35 nm, it is believed that the intrinsic dielectric integrity of SOS devices will not be a limitation to further development of the technology.

## 1. Introduction

For many years now, it has been recognized that the integrity of the gate oxide in MOS devices is a key issue for both yield and reliability of integrated circuits. Random-access memories, because of their very large total gate area, are the circuits most sensitive to this failure mechanism, and as early as 1976 it was suggested[1] that oxide breakdown can be the primary failure mode of a RAM. The

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reliability aspects of gate-oxide dielectric integrity are perhaps more critical than the yield issue, because of the need to design appropriate tests that will accelerate rates of potential failure mechanisms in circuits. With the continuing trend toward increases in circuit complexity and decreases in the size of devices, gate oxides will be required in the future to withstand even higher electric fields than those of today; hence, the need to understand the factors that dominate the dielectric integrity of the gate oxide in an MOS technology will become more important.

In the work described here, characterization of the dielectric integrity of the gate oxide in various CMOS/SOS processes was done. The purpose of the investigation was two-fold: to assess the merits of certain process variations from the viewpoint of reliability goals and to further enhance the understanding of the factors that control dielectric integrity in SOS structures. Only isolated-mesa processes were investigated, primarily because the RCA production processes are of this type. A major motivation for this work was the discovery that the dielectric integrity of the channel oxide in devices made with a low-temperature SOS process is not as good as that in devices made with processes that include post-oxidation temperatures near 1050°C. Because the use of low temperatures is critical for the fabrication of radiation-hardened circuits,[2] which are now in volume production, and for high-density circuits with device dimensions near 1 μm, a further study of dielectric integrity was deemed to be timely.

Because of some of the unique topographical features associated with SOS devices, the issue of dielectric integrity in SOS technology has been of special interest for many years. Transmission electron microscopy has been used[3] to characterize the topographical structure of selectively-etched, oxidized silicon islands; features such as the very sharp corner at the top of the island and the reduced oxide thickness on the sidewall near top and bottom of the island are certainly potential problems with respect to dielectric integrity of the channel oxide. During the past few years, various approaches, including a variety of quasi-planar schemes, have been considered to enhance the dielectric integrity in SOS devices, and a recent review[4] provides an overview and bibliography of the work in this area. Although planar-type SOS structures do offer a significant improvement in dielectric integrity over that found in isolated-mesa structures,[5,6] the planar structure, because of the parasitic sidewall transistor with a thick oxide, does not appear to be suitable for the fabrication of circuits in one of the major areas of application for SOS technology, radiation-hardened systems. Therefore, this work

was limited to an investigation of process variations within the constraint of an isolated-mesa technology.

It should be noted that problems associated with the topology of silicon devices and dielectric integrity are not unique to SOS technology. For example, the thin gate oxide, near the isolation region, produced in selective oxidation processes in bulk silicon technology has been a subject of concern for many years[7,8] and is still an issue today.[9] Furthermore, there is no evidence to suggest that the fundamental physical mechanisms associated with the dielectric integrity of the channel oxide in SOS devices are any different from those associated with devices in bulk silicon.

After some remarks with regard to test structures and characterization methods, this paper describes the results obtained from a variety of experiments. These experiments were designed to enhance our understanding of the role edges play in the determination of dielectric integrity and to attempt to produce topographical modifications favorable to the enhancement of dielectric integrity in an isolated-mesa SOS structure. The fast-ramp characterization technique employed during this work was found to be a very good indicator of the viability of the various process modifications. A number of processes that offer a dielectric integrity enhanced over that produced by the straightforward, KOH-based, selective island-etching process were developed during the period of this investigation. A particular dry island-etching process was found to be easily implementable in a factory environment. Present reliability data[10] demonstrate that the process is suitable for the fabrication of high-density, CMOS/SOS RAMs with a 50-nm-thick channel oxide, and the results presented here indicate that devices with oxides at least as thin as 35 nm can be made with present technology.

## 2. Test Structures

The devices used in this study were fabricated with variations of a self-aligned, $n^+$ polysilicon-gate, CMOS/SOS process. The initial thickness of the silicon films was 0.6 μm. Structures with feature sizes in the range from 5 to 1.5 μm were examined. Included among the process variations were different maximum process temperatures after growth of the channel oxide, various thicknesses of the channel oxide, and modifications of the topography of the silicon islands. Channel oxides were grown in pyrogenically-generated steam. As mentioned above, all test structures were of the isolated-mesa type.

A variety of test structures were characterized. Primary emphasis was given to the measurement of the dielectric integrity of large arrays of transistors in parallel, so that a large number of devices could be sampled. On some wafers, arrays of various sizes were available, and as many as 5000 devices could be simultaneously stressed. In most cases, however, an array with 480 transistors was used. All the arrays consisted of n-channel, edge-type transistors; that is, the polysilicon gate forms a continuous path over the channel oxide on the sidewalls and the top of the mesas. As discussed below in more detail, what is really being characterized is the dielectric integrity of the oxide near edges in such SOS structures.

Characterization of the dielectric integrity of both edge-type and edgeless single transistors was also done. Hence, it is possible to determine more clearly the effects associated with the edges of the silicon islands. The characteristics of the edgeless transistors are also important, because input protection devices in circuits contain transistors of this type. The presence of a large number of single devices also makes possible a detailed characterization of time-dependent breakdown phenomena, but this is the subject of another study.[11]

## 3. Characterization Methods

A variety of techniques for the characterization of dielectric integrity in device structures are known. At least three methods are commonly used: current measurements in response to a ramped voltage, breakdown measurements in response to a stepped-voltage pulse, and time-dependent breakdown measurements. Each of these methods has its merits, which, to some extent, represent a trade-off between convenience of the measurement and the accumulation of basic information. In view of the purposes of this investigation, primary emphasis was given to the ramped-voltage measurement and, to a lesser extent, to measurements with a stepped-voltage signal. Both of these measurements are reasonably convenient for the purpose of evaluation of the effects associated with a process experiment. In bulk silicon devices it was shown,[12] furthermore, that a direct relationship exists between catastrophic breakdown as measured by a ramped-voltage test and the information obtained from the analysis of time-dependent breakdown data. Recent data obtained from SOS devices shows this same relationship.[11]

The ramped-voltage characterization technique offers the possibility of measurement of the current flow through the oxide during

the test, and we believe that, in some cases at least, the characteristics of the pre-breakdown current may be as important as the magnitude of the catastrophic breakdown voltage. It was found, for example, that there is no fixed relationship between the catastrophic breakdown voltage and the onset of gate leakage current in variant SOS structures; in many cases, it was observed that pre-breakdown leakage-current characteristics could be affected without changing the voltage at which catastrophic failure occurred. Furthermore, much evidence to suggest that the ultimate failure of thin oxide films is directly related to charge injection and trapping has accumulated during the past few years,[13–15] and such effects will become much more significant as channel oxides are scaled-down in thickness. The measurement of pre-breakdown current-voltage characteristics also makes possible at least speculation about the mechanism of breakdown and allows one to examine the role of charge trapping in the oxide. A final, important point with regard to the significance of the pre-breakdown current-voltage characteristics is that the reproducibility of these characteristics was found to be a very sensitive indicator of process reproducibility and consistency. In contrast, the value of gate voltage at which catastrophic breakdown of the channel oxide in an array occurs tends to be much more variable.

Measurement of the current-voltage characteristics was done simply by the application of a voltage ramp between the gate and the source and drain of the devices. Current was measured with a logarithmic current detector. A typical ramp rate was about $10^6$ V/cm-sec, which was chosen primarily because this value is in the fast-ramp range where the current-voltage characteristics tend to be independent of the ramp rate; with slower ramp rates, the measured currents are strongly dependent upon the ramp rate. This dependence of current on the applied ramp rate is presumably due to charge trapping in the oxide, and this subject is discussed later.

During the early part of this work, the effect of the polarity of the gate-bias sweep was investigated to determine if a worst-case bias condition existed; if so, measurements could then be concentrated upon the weaker condition. A large number of single transistors, edge and edgeless of both n and p types, were characterized. For devices with edges, it was always found that higher currents and slightly lower breakdown voltages were associated with a positive gate bias, and there was a tendency for n-channel devices to break down at voltages slightly smaller than those of p-channel devices. In the case of edgeless transistors, it was observed that the weaker condition was associated with a negative gate bias. These

observations are what one would expect in view of the topographical features of the SOS devices and the fact that electrons are the primary charge carrier in the silicon–silicon-dioxide system when carrier injection is done by the method used in this work. For devices with edges, the sharp upper edges of the silicon island are the regions with the highest electric field, and electron injection from these edges would be favored by a positive gate bias. In the absence of edges, the rougher interface is probably that of the polysilicon-oxide, and electron emission from the polysilicon is then favored for a negative bias on the gate. Based upon this information, the majority of the later measurements were concentrated upon positive-bias data obtained from n-channel devices and arrays. In a later section, some specific data will be presented to further illustrate the effect of the bias polarity on the dielectric integrity of thin oxides.

A typical measurement procedure, therefore, was to sweep an n-channel device with a positive bias until catastrophic failure occurred. During the low-voltage portion of the sweep, the charging current of the device capacitance is measured, and the magnitude of that current is used as an indicator to show that the entire array is being stressed.

In general, measured values of gate voltage have not been converted to electric fields for the presentation of the data, because of the complex structure of the SOS devices. As mentioned earlier, it is well-known that the channel oxide tends to be significantly thinner near the top and bottom of the sidewalls of the silicon islands. Furthermore, as discussed below, the data show that the dielectric integrity of the structures is determined by the sidewall topography. Hence, there is no straightforward method to calculate the electric field that is relevant to the measured dielectric integrity in the SOS devices, and the oxide thickness values associated with the data must be considered as nominal values which are only correct for the oxide layer on the top of the silicon islands.

## 4. Basic Phenomena

In this section, the fundamental phenomena associated with the dielectric integrity of the channel oxide in an isolated-mesa SOS process are described. Emphasis is given to the consistent behavior of very large arrays and to the effects associated with the sidewalls of the epitaxial silicon islands. The data show clearly that the edges of the islands determine both the gate oxide conduction and breakdown characteristics.

## 4.1 Characteristics of Large Arrays

Fig. 1 shows typical characteristics obtained from the application of a fast voltage ramp to seven different arrays. Gate leakage current versus gate voltage is shown for arrays varying in size from a single device to 5000 devices in parallel. Stated differently, the dielectric integrity of SOS structures containing from two to 10,000 edges is measured. All of the arrays are contained within one test chip. With the exception of the single device, the transistors in these arrays have a nominal gate width of 7.6 μm and a gate length of 5 μm; the single device has a gate width 3.3 times larger than that of the transistors in the arrays, and has the same gate length as in the array devices. In the fabrication of these arrays, the silicon islands were formed with a KOH-based etchant, the 74-nm-thick channel oxide was grown at 900°C, and all processing steps after the growth of the channel oxide were done at temperatures not exceeding 950°C.

The characteristics of Fig. 1 illustrate a number of points. One can observe that the charging current and the gate leakage currents scale directly with the size of the arrays, and this latter point will be illustrated more precisely below. In contrast, the voltage at which catastrophic failure occurs tends, with the exception of the single device, to be random and independent of the number of transistors in the array. This random behavior of the voltage at which destructive breakdown occurs can be considered a positive attribute of a process, as it suggests that circuit complexity can be increased without a significant reliability risk associated with dielectric failure due simply to the existence of a larger number of devices in the circuit. In spite of the randomness of the value of gate voltage at which catastrophic breakdown occurs, the magnitudes of the gate leakage currents were found to be very consistent. To within the sensitivity of the logarithmic current scale of the characteristics, it is generally not possible to find a measurable difference in the currents in a particular array on any one wafer. This observation seems to suggest that gate leakage currents are uniformly distributed throughout the arrays.

Some array characteristics obtained from structures fabricated with wet-etched silicon islands exhibit the changes in slope near 13 V shown in Fig. 1. Such a characteristic, which indicates a reduced rate of increase of current with voltage, suggests that, even with the fast ramp rate used, charge trapping in the channel oxide may have an effect on the measured currents. The effect of charge trapping in the oxide is shown more clearly in Fig. 2; here, the characteristics of arrays after the application of a gate voltage stress of

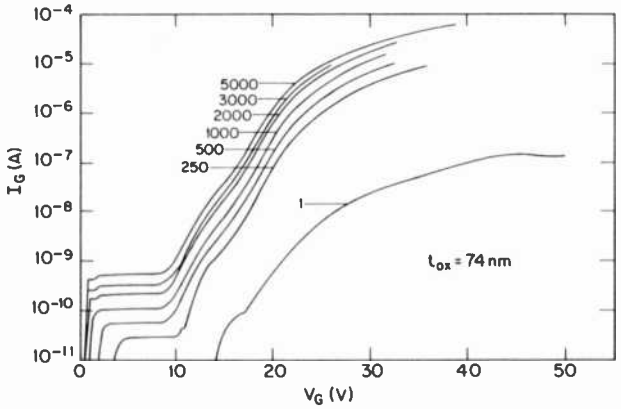



**Fig. 1**—Family of fast-ramp characteristics from arrays containing from 1 to 5000 isolated-mesa, SOS transistors. The islands were wet-etched, the channel oxide was 74-nm thick, and a low-temperature process was used. The ramp rate was $10^6$ V/cm-sec.

+25 V for two minutes are shown. It can be seen that subsequent to the stress the leakage currents are much reduced, and the onset of gate leakage currents above the displacement current level is shifted by 10 V. The voltage at which catastrophic failure occurs appears not to have been affected by the voltage stress. Other effects, such as the decay of gate leakage currents with time, associated with charge trapping in the oxide were also observed. As suggested by earlier work,[16] the results discussed here are consistent with a model based upon a reduction in local electric field near the region of the cathode due to negative charge trapping in the oxide.

A more detailed analysis of the gate leakage currents was done,

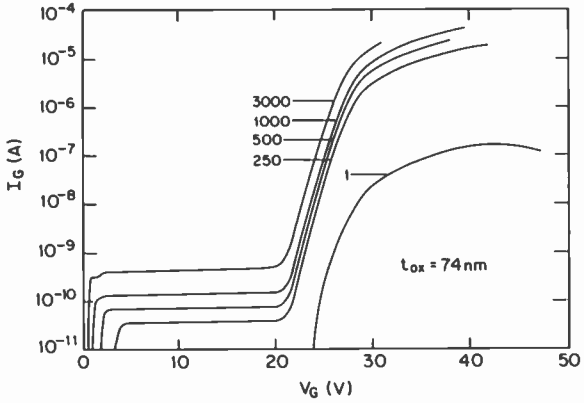



**Fig. 2**—Family of fast-ramp characteristics from arrays, as in Fig. 1, after a +25-V, 2-min stress.

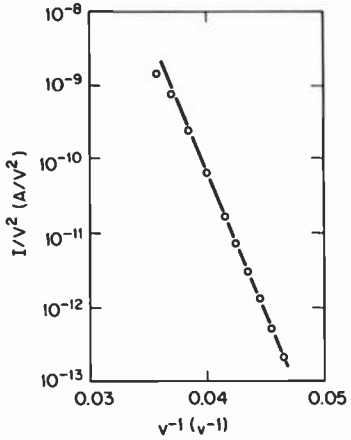



**Fig. 3**—Fowler-Nordheim plot obtained from an array of 250 transistors after a +25-V,2-min stress.

and it was found that the array characteristics could only be fit to a Fowler-Nordheim type of plot[17] such as shown in Fig. 3. Illustrated is the characteristic of an array of 250 transistors after the application of a voltage stress. The measured values of voltage have not been converted to units of electric field because, as discussed in more detail below, the carrier injection within the individual transistors is not believed to be uniform. The deviation of the points from the straight line at high values of voltage is believed to be an artifact of the measurement, because, at the high current levels associated with the higher values of voltage, the ramp rate produced by the ramp generator is reduced.

To further illustrate the relationship between gate leakage currents and the size of an array of transistors, data from fast-ramp characteristics of the types shown in Figs. 1 and 2 were extracted and plotted to explicitly show the effect of the array size. In Fig. 4 gate leakage current at a particular gate voltage is plotted versus the number of transistors in the array for both a stressed and an unstressed group of arrays. In general, it was found, as Fig. 4 suggests, that the data from stressed arrays could be plotted as a straight line with a slope very close to unity, whereas there was a tendency for data from unstressed arrays to fall along a line with a slightly smaller slope. Data of the type shown in Fig. 4 can probably be taken as an indicator of a low defect-density process; the linear characteristic suggests that at least 5000 transistors whose gate-oxide leakage behavior is no worse than that of a single transistor can be made.

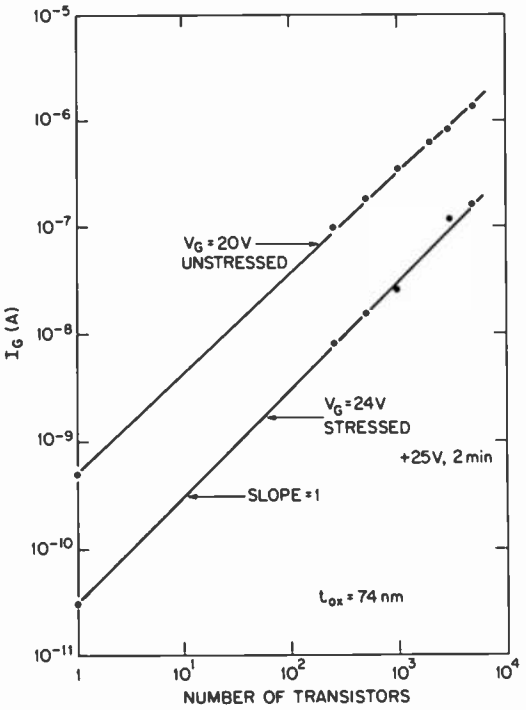



**Fig. 4**—Gate leakage current, at a particular gate bias, versus the number of transistors from array characteristics.

## 4.2 Role of Island Sidewalls

As indicated earlier, it has been generally realized that the dielectric integrity of an isolated-mesa, SOS structure is controlled by the topographical features associated with the edges of the silicon islands, and Fig. 4 illustrates this concept very clearly. Recall that the single transistor whose gate leakage current is plotted has a gate width 3.3 times larger than each single device in the arrays; that is, the single device has the same gate length but 3.3 times the gate area of the individual devices in the arrays. That the leakage current in the single device scales with the currents in the arrays shows that gate leakage currents are determined not by the total gate area but by the gate length, which corresponds to the length of the island edge under the gate.

The important role of the island edges in the determination of the dielectric integrity of SOS structures can be illustrated by another observation. It was found that charge injection into the gate oxide could be used to preferentially increase the threshold voltage of the

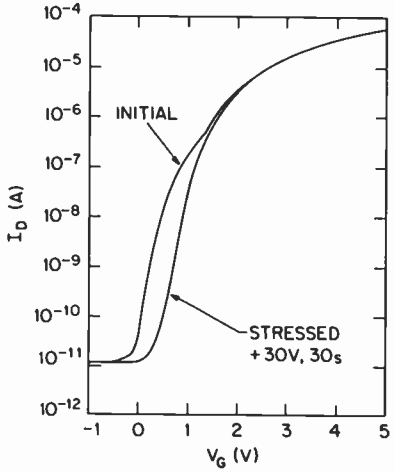



**Fig. 5**—Gate-transfer characteristics from an n-channel transistor before and after a gate stress.

parasitic, sidewall transistor in n-channel devices without affecting the top-of-the-mesa device, and this effect is illustrated in Fig. 5. Shown are logarithmic gate-transfer characteristics of an n-channel SOS transistor before and after the application of +30 V to the gate with respect to the source and drain for 30 seconds. The pre-stress characteristic shows the current due to the well-known, parasitic, sidewall device in the subthreshold region. With the positive gate bias stress, the current due to the parasitic transistor is totally suppressed, presumably because the threshold voltage of the sidewall device is increased by the trapping of injected electrons. However, the characteristic of the top-of-the-mesa transistor is unaffected. Although there may be some difference between the trap concentrations in the oxide on the sidewall and on the top of the mesa, the observed suppression of the parasitic device due to a gate bias is certainly consistent with the idea that the island edges determine the dielectric integrity of isolated-mesa SOS structures.

The importance of the island edge in the determination of channel-oxide dielectric integrity can further be illustrated by a comparison of fast-ramp characteristics obtained from edgeless and edge-type transistors. Typical current-voltage curves from single transistors whose gate oxide is 75-nm thick are shown in Fig. 6. The difference in both the catastrophic-breakdown voltage and the voltage at which gate conduction begins are quite dramatic. The onset of gate conduction above the displacement current level is increased by almost 40 V in the absence of edges. In the case of

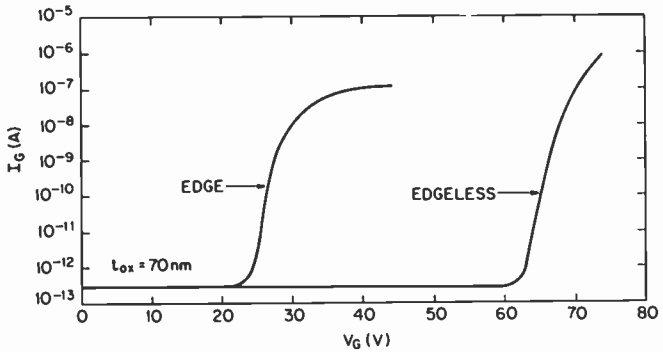



**Fig. 6**—Fast-ramp characteristics of single edge-type and edgeless transistors.

catastrophic failure, the absence of edges leads to about a 75% increase in the voltage at which the gate oxide ruptures. The breakdown of the edgeless device at 74 V is in all likelihood the intrinsic breakdown of the oxide, since with this gate bias, the maximum field is about 10 MV/cm. In the case of 75-nm-thick oxide films on bulk silicon, maximum field strengths are reported[18,19] to be in the range from 9.5 to 11 MV/cm. Based upon data of this type, we believe that silicon dioxide films grown on SOS are inherently no weaker than those grown on bulk silicon.

## 4.3 Effect of Measurement Temperature

A limited amount of data to assess the effect of temperature on dielectric integrity was taken. Both arrays and single devices were characterized. All of the data suggest, as one might expect, a very weak dependence of both breakdown voltage and gate leakage current on temperature, and in some cases, the inherent variability of the data among the devices made it difficult to clearly establish an effect associated with temperature. The trend of the temperature-dependent characteristics can be illustrated by the data obtained from one wafer; fast-ramp curves at three temperatures were taken from many single transistors. Fig. 7 shows both the variations and the average values of catastrophic failure and gate leakage current at 25 V from the fast-ramp curves. The variability in the data make analysis difficult, although it can be noted that the average values exhibit a remarkably linear relationship with temperature: with increasing temperature the catastrophic-breakdown voltage decreases by perhaps 3 V per 100°C and gate leakage current increases by about 0.4 nA per 100°C.

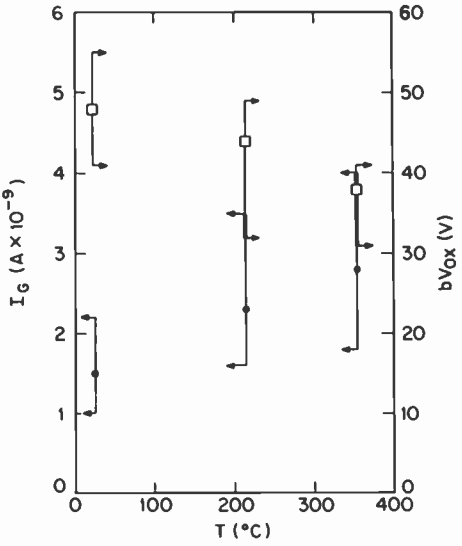



**Fig. 7**—Effect of measurement temperature on gate leakage current at 25 V and on catastrophic breakdown voltage from single, edge-type, n-channel transistors.

One might attempt to fit the leakage current data to the relationship between temperature and Fowler-Nordheim currents:[20]

$$J(T) = J(0)\frac{x}{\sin x},$$

in which $x$ is a complex function of temperature, barrier height, and electric field. The large error bars in Fig. 7 bring the data within the range of such a functional relationship, but the data cannot justify this relationship in detail.

The weak dependence of dielectric integrity on temperature serves to emphasize the increasing importance of the use of tests at voltages significantly above the anticipated operating voltage of a device during reliability investigations. With the trend to ever-decreasing channel oxide thicknesses, the importance of such testing and analysis becomes more significant.

## 5. Process Variations

For any topographically-distinct, SOS island structure, one might expect that the thickness of the channel oxide is the major determinant of dielectric integrity, and data are presented below to illustrate the effect of the oxide thickness on breakdown and gate leakage currents. In addition, in the case of wet-etched islands at

least, significant differences in dielectric integrity were found to be associated with differences in processing temperatures, and, in particular, it was discovered that processes in which the temperature of the wafer never exceeds about 1000°C after the growth of the channel oxide produce devices whose dielectric integrity is reduced over that found in devices fabricated with a high-temperature process. This latter issue is of special significance because of the need to reduce processing temperatures for the fabrication of short-channel and radiation-hardened devices.

## 5.1 Process-Temperature Effects

To characterize the effect of temperatures associated with wafer processing on the dielectric integrity of SOS structures, arrays of transistors made with three different processes were analyzed. All the devices had silicon islands that were wet-etched in a KOH-based solution. In all cases, also, the growth of the channel oxide was done at 900°C. What was varied was the temperature of certain processing steps subsequent to the growth of the channel oxide and the deposition of the polysilicon gate material. Three maximum, post-oxidation temperatures were selected: 850°C, 950°C, and 1050°C. The two extremes represent, respectively, the RCA radiation-hardened[2] and the RCA commercial SOS processes. In some cases, it was possible to include more than one maximum temperature within one wafer-lot, so that the effect of possible lot-to-lot variability in the island-etching, which is a batch process, would be minimized.

The results obtained from our investigation of process temperature effects are illustrated by the data of Figs. 8 and 9. Shown in Fig. 8 for the three processes is the relationship between array size and the median values of gate voltage at which 0.5 μA of gate leakage current flowed in response to a stepped-voltage test. Each data point of Fig. 8 represents a minimum of 35 measurements and as many as 130 measurements. Clearly, the dielectric integrity of large arrays of devices made with the highest temperature process is superior to that of devices made with the two lower temperature processes, and the difference, in terms of gate voltage, is as much as 10 V. It should be remarked that the major cause of the scatter in the data in Fig. 8 is the test condition itself; since testing was done in voltage increments of 2 V, the uncertainty in the gate voltage at failure is somewhere in the two-volt interval below the measured value. This uncertainty in the measurement probably accounts for the differences in the data for the two low-temperature

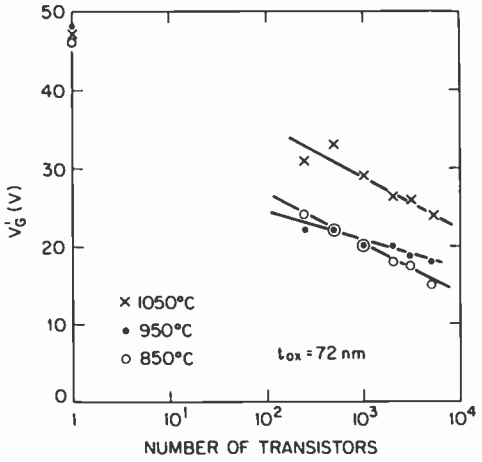



**Fig. 8**—Effect of processing temperature on dielectric integrity in arrays. Plotted is the median value of gate bias at which 0.5 μA of gate current was detected in response to a stepped-voltage test.

processes. In contrast to the data from the large arrays, there is no significant difference in the behavior, shown in Fig. 8, of the single transistors. However, the data from the single devices cannot be interpreted in the same way as the data from the arrays, because, as can be seen from Fig. 1, the test had to force the single devices to catastrophically fail, whereas the arrays were still in the regime of gate leakage current prior to failure. Because the point of catastrophic failure tends to be somewhat variable, as illustrated by Fig. 7, speculation about the similarity of the data points representing the single devices in Fig. 8 is probably not warranted.

Fast-ramp measurements consistent with the data of Fig. 8 are shown in Fig. 9. Curves are shown for arrays of 500 transistors made with a 1050°C and 950°C process. Both a higher gate leakage current and a lower breakdown voltage occur in the arrays made with the lower temperature process, and it can be observed that the voltage difference between the two characteristics at a current of 0.5 μA agrees closely with the data in Fig. 8. A significant difference in the consistency of the fast-ramp characteristics among the different process was also found: the value of gate voltage at which breakdown occured was very reproducible among different arrays for devices made with the high-temperature process, whereas, the breakdown voltage tended to be variable among arrays made with the low-temperature processes. In all cases, however, the gate leakage characteristics were very uniform from array to array for any one process.

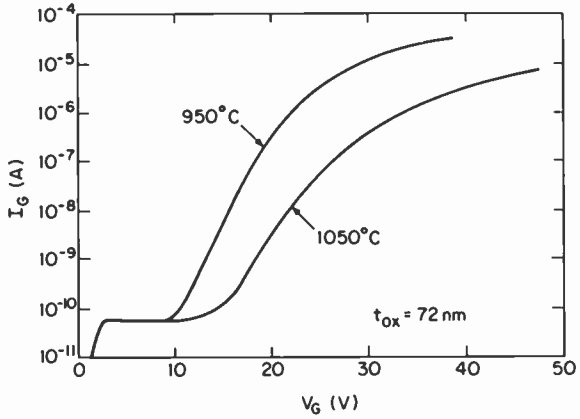



**Fig. 9**—Fast-ramp characteristics from arrays of 500 transistors to illustrate the effects associated with a 950°C and a 1050°C process.

The observed relationship between dielectric integrity and process temperature permits some speculation about the mechanism responsible for the differences. For this purpose it is important to note that the process temperatures varied were those associated with process steps after the growth of the channel oxide; in all cases, the growth of the channel oxide was done at one temperature, 900°C. Therefore, it seems unlikely that the effect of temperature is associated with topographical modifications, such as have been described[21] when silicon is oxidized at different temperatures. More likely, it seems, there is a healing mechanism which occurs after the growth of the channel oxide. The data indicate that the healing process occurs at temperatures somewhere above 950°C, and that it becomes significant at 1050°C. This observation is quite consistent with the onset of viscous flow and stress relief in silicon dioxide films; it has been reported[22–24] that significant flow and stress relief in silicon dioxide occurs at about 975°C. We believe, therefore, that in high-temperature processes a healing mechanism associated with stress relief in the channel oxide occurs that improves the dielectric integrity at the edges of the silicon islands.

## 5.2 Effect of Channel Oxide Thickness

To investigate the role that the thickness of the channel oxide plays in the determination of dielectric integrity, arrays were fabricated with various oxide thicknesses. To illustrate the results of this investigation, data from one particular lot of wafers made with the 1050°C process are shown in Fig. 10. The data plotted are the measured gate voltage values at which 0.5 μA of gate leakage current

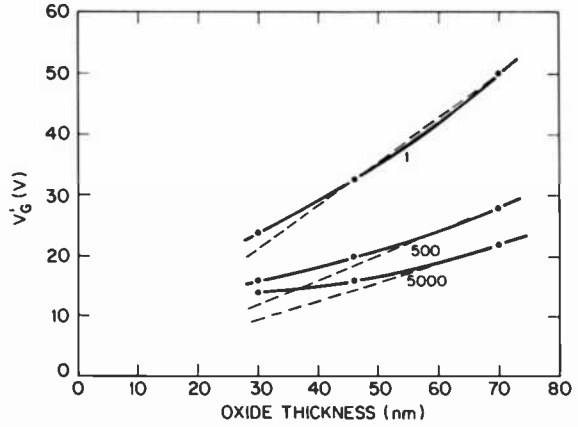



**Fig. 10**—Median gate bias at 0.5 μA versus oxide thickness for three sizes of arrays made with the 1050°C process.

flowed in single transistors and in arrays of two sizes in response to a stepped-voltage test. The data obtained from arrays of other sizes were similar. Just as in the case of the data in Fig. 8, it should be noted that the single device had to be forced to fail catastrophically to measure 0.5 μA during testing, whereas the arrays presumably had not yet broken down at the test current. This supposition is supported by Fig. 11, which shows data obtained from arrays of 500 transistors in a number of different ways; shown with the data transposed from Fig. 10, are data obtained from fast-ramp characteristics at three different conditions. The gate voltage at which 0.5 μA flowed during the fast ramp is seen to agree closely with the data from the stepped-voltage measurement, and the gate voltage at which catastrophic failure occurred is much higher than the value corresponding to 0.5 μA of gate leakage current.

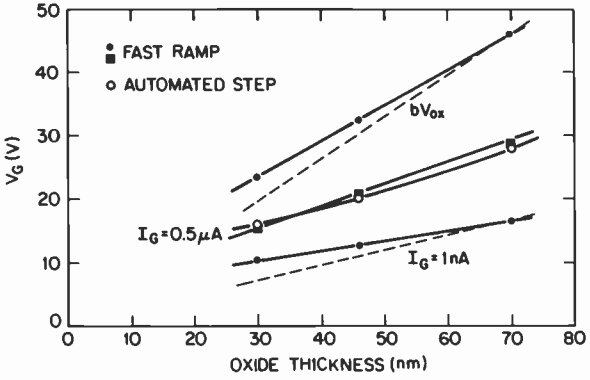



**Fig. 11**—Gate bias under various conditions from fast-ramp characteristics and the automated-step test from 500-transistor arrays with three oxide thicknesses.

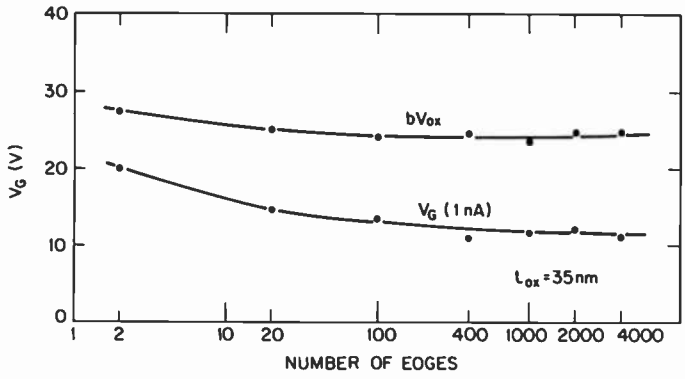



**Fig. 12**—Mean values of positive gate bias for catastrophic breakdown and at 1 nA from arrays of edges fabricated with a low-temperature, 35-nm-oxide, dry-etched-island process.

The data of Figs. 10 and 11 suggest that dielectric integrity is increased as the thickness of the channel oxide is reduced. The dashed lines are linear extrapolations from the data points representing the devices with the thickest oxide, and in all cases the gate bias values representing the devices with thinner oxide films are significantly higher than the extrapolated values. Such an increase in dielectric breakdown field with decreasing oxide thickness is well-known for oxides grown on bulk silicon, and, in fact, the 20% enhancement of $bV_{ox}$ associated with the devices with the 30-nm oxide is very close to the percentage enhancement reported[18,19] for 30-nm-thick oxide films compared with 70-nm films on bulk silicon. The data of Fig. 11 also indicate that the onset of gate leakage current scales less rapidly than reductions in oxide thickness. These observations suggest again that there is no reason to expect to find differences in the fundamental issues that influence the reliability of oxide films in either bulk silicon or SOS technologies.

More extensive data for thin oxides were obtained from wafers containing large arrays of edges. These arrays consist not of transistors but simply of polysilicon lines crossing a matrix of holes in epitaxial silicon. Outside the polysilicon, the epitaxial material is heavily doped. The nominal gate area is the same in all of the arrays. In Fig. 12 typical data from devices with a 35-nm-thick oxide are shown to illustrate how the voltage of catastrophic failure and the bias at which 1 nA of gate leakage current flows are related to the total number of edges. The devices whose characteristics are shown were made with a low-temperature process, and the silicon islands were formed by a dry etching process. As illustrated earlier, the data of Fig. 12 also show that the bias at which gate oxide

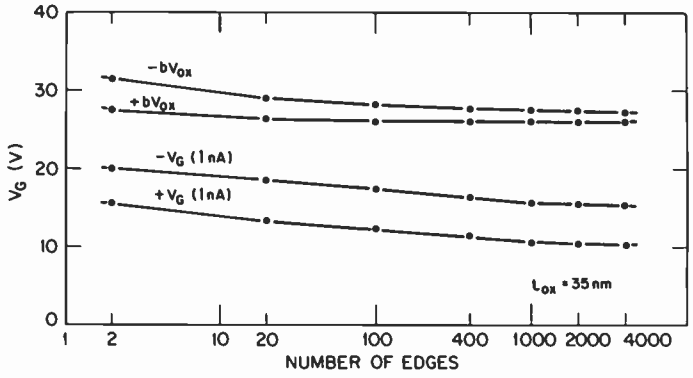



**Fig. 13**—Mean values of gate bias, for both polarities, for catastrophic breakdown and at 1 nA from arrays of edges; processing was the same as for the arrays of Fig. 12, except that the gate was a tantalum silicide bilayer structure.

breakdown occurs is only a weak function of the number of edges; hence, the intrinsic behavior of island edges should not be a limitation to the dielectric integrity of very high-density SOS circuits with channel oxides on the order of a few tens of nanometers thick.

## 5.3 Silicide Gate Material

The fabrication of high-performance, high-density circuits with device dimensions on the order of a micrometer requires the use of a high-conductivity gate material, and a bilayer structure consisting of $n^+$ polysilicon with a refractory-metal silicide on top is commonly used. Although it might seem unlikely that such a gate structure would affect the dielectric integrity of the underlying gate oxide, data was presented[25] to indicate that the lower layer of polysilicon must, in some cases, be as thick as 200 nm to avoid a penalty in dielectric integrity. Other publications have not reported such a dependence of dielectric integrity on polysilicon thickness, and it has been suggested[26] that the method of formation of the silicide is an important variable.

To investigate the issue of dielectric integrity in structures with a bilayer gate, arrays of the type discussed in relation to Fig. 12 were analyzed. In this case, the devices had a tantalum-silicide–polysilicon gate structure in which the underlying polysilicon was 300-nm thick. The silicide was formed by cosputtering. The thickness of the gate oxide was again 35 nm. Data obtained from a sample of eight wafers are summarized in Fig. 13; the points rep-

resent the mean values obtained from the sampling of arrays on every wafer, and data for both polarities are shown.

For the case of a positive gate-bias sweep, a comparison between Figs. 12 and 13 suggests that the silicide process has no impact on the dielectric integrity of the channel oxide. The mean values of gate breakdown voltage differ at most by 2.5 V, which is probably within the statistical noise, and, in fact, the devices with the silicide gate exhibit the larger values. Although we have not investigated the effect of a variation of the polysilicon thickness, the results reported here are consistent with published information.[25,26]

Fig. 13 also shows explicitly the effect of the polarity of the gate-bias sweep on the measurements. As indicated earlier, positive bias applied to the gate of an isolated-mesa SOS structure is the polarity for which the channel oxide is dielectrically the weaker, and this fact is clearly shown by the data. In the case of the gate bias at which 1 nA of leakage current flows, the data are unambiguous, and the consistency of the difference for all of the arrays serves to emphasize again the reproducibility of gate leakage characteristics in a well-defined process. The data representing catastrophic failure are less clear, especially as the array size becomes large. However, as will be described later, conduction and breakdown in channel oxides in SOS devices are not always closely coupled.

Data from edgeless devices were also obtained from these eight wafers. The mean values of the catastrophic breakdown voltage $bV_{ox}$ are $+40$ V and $-35$ V; the voltages $V_g$ at which 1 nA flowed for both polarities are $+27$ V and $-22$ V. As indicated earlier, a negative gate bias represents the weaker situation in edgeless SOS devices, presumably because the oxide-polysilicon interface is rougher than the oxide–epitaxial-silicon interface.

Recall that the special test structures utilized to generate the data of Figs. 12 and 13 are arrays of equal total gate area. Hence, even more convincing data of the type shown in Fig. 4 can be obtained to show that the sidewalls of isolated-mesa SOS structures dominate the dielectric integrity of devices. In Fig. 14 measured values of gate leakage current from one set of arrays at a gate bias of 15 V are plotted as a function of the number of edges. Again, one sees a nearly linear relationship between gate leakage current and the number of edges.

Based upon the data presented in this section, we see no impediment to the fabrication of reliable, high-density, thin-oxide circuits in an isolated-mesa SOS technology. A well-defined, high-conductivity, bilayer gate process does not negatively impact dielectric integrity, and gate oxides at least as thin as 35-nm can be used.

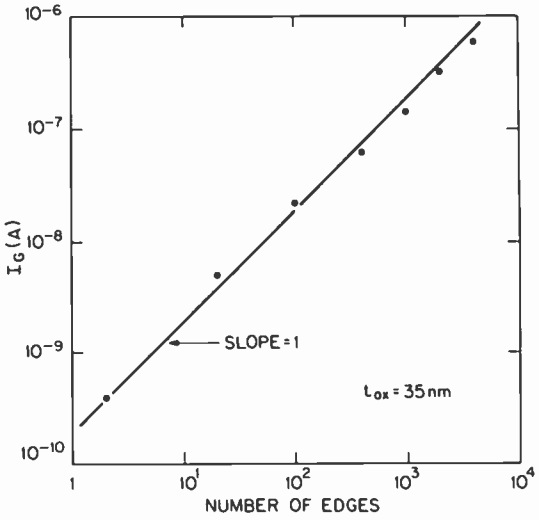



**Fig. 14**—Gate leakage current at 15 V versus the number of edges from equal-area arrays with the silicide gate.

## 6. Topographical Modifications

Thus far data has been presented to show that an isolated-mesa SOS process can produce very uniform and reproducible characteristics associated with dielectric integrity of the channel oxide. As the earlier literature indicates, the presence of the edges of the silicon islands is the most important factor which controls both the onset of gate leakage current and the catastrophic breakdown of the oxide. A particularly important observation, not heretofore mentioned in the literature, is the significant penalty in dielectric integrity associated with the processing of SOS wafers at low temperatures.

Because processes for the fabrication of radiation-hardened and short-channel devices require the use of low temperatures, interest was focused upon an investigation of techniques to topographically modify the island edges. Of particular interest was suppression of gate leakage current which, in view of recent suggestions,[13–15] may be more intimately related to long-term reliability than is the gate breakdown voltage as measured by the methods reported here. In this section, the results of a number of experiments directed toward alteration of the SOS island structure are described.

For the most part, the data to be presented are based upon test and control experiments done within wafer lots. In most cases each cell of the experiment consisted of from three to six wafers, but for

the laser contouring experiments, portions of each wafer were exposed to the laser. The control devices were fabricated by the conventional, KOH-based, wet etching process. Because the process modifications to be described were exploratory in nature, the primary characterization technique employed was the fast-ramp measurement of an array of transistors. It was noted that the relative behavior of arrays is equivalent to that of single devices; that is, the improvement or degradation of dielectric integrity associated with a particular process could be found in the characteristics of either a large array or a single, edge-type transistor. It was not, in general, possible to obtain large quantities of data for statistical analysis. Instead, what will be presented are fast-ramp characteristics that are typical of those obtained from arrays made with the various processes in their final state of development. It is not necessarily the case, therefore, that the data represent the best results that might be achieved if further refinements to the processes were investigated.

## 6.1 Local Oxidation

A process in principle similar to a local oxidation process in bulk silicon technology was developed for the formation of SOS islands. In this process, the etch mask for the silicon islands consists of a thin oxide film and a 100-nm-thick layer of silicon nitride. After island etching in the KOH-based solution, the wafers are subjected to an oxidation in steam at 900°C; this oxidation step grows 200 nm of oxide on a bulk (100)-oriented wafer. After the local oxidation step, the oxide and nitride films are removed so that only the bare silicon islands remain on the substrate. Processing then continues in the usual way. The channel oxide was grown to a thickness of 70 nm, and post-oxidation process temperatures were limited to a maximum of 875°C. This local oxidation process is, in principle, straightforward, and does not involve additional masking levels.

For the purpose of evaluation, arrays consisting of 480 transistors in parallel were subjected to the ramped-voltage test. Fig. 15 shows curves representing the typical characteristics of the test and control devices. A significant suppression of gate leakage currents is apparent, and over a wide range of gate bias, the local oxidation process reduces the current by more than two orders of magnitude. The magnitude of gate bias at which catastrophic failure occurred is, on average, unaffected by the local oxidation process. So, in summary, a local oxidation process, which presumably alters the shape of the top edge of the silicon island, can at the least produce devices

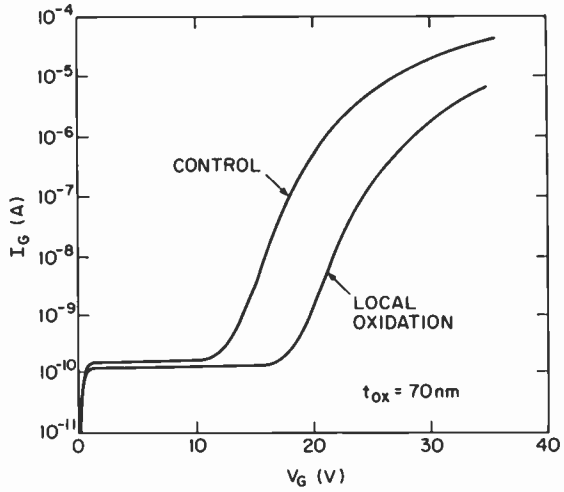



**Fig. 15**—Fast-ramp characteristics of arrays of 480 transistors made with the wet-etched-island process and with the local-oxidation process. The processing was done at low temperatures and the channel oxide is 70-nm thick.

with significantly reduced gate leakage currents over a wide range of gate bias conditions.

## 6.2 Double-etched Island

Based upon an earlier suggestion,[27] an attempt was made to define an island etching process that would remove the sharp and possibly reentrant edge at the top of the silicon islands. This process differs from the basic, wet-etched island process in that after the usual island etch, the oxide mask is partially etched to expose a narrow portion of the top of the silicon island and the silicon is again etched. The time of the second etch is approximately one-fourth the time required to etch the basic island structure. This procedure should produce a ledge on the sidewall of the island, and such a structure is illustrated by the SEM view of Fig. 16. This double-etching process clearly eliminates any possibility of a sharp, reentrant edge at the top of the island. As a variant of this twice-etched island process, a dry-etching process was also used for the first etch of the silicon. It was our experience that the reproducibility of a double-etching process is not good, most likely because of problems associated with reproducibility of the structure after the oxide etch. There appeared to be significant variations from wafer-to-wafer in the time required to etch the oxide mask to expose the portion of the silicon that would

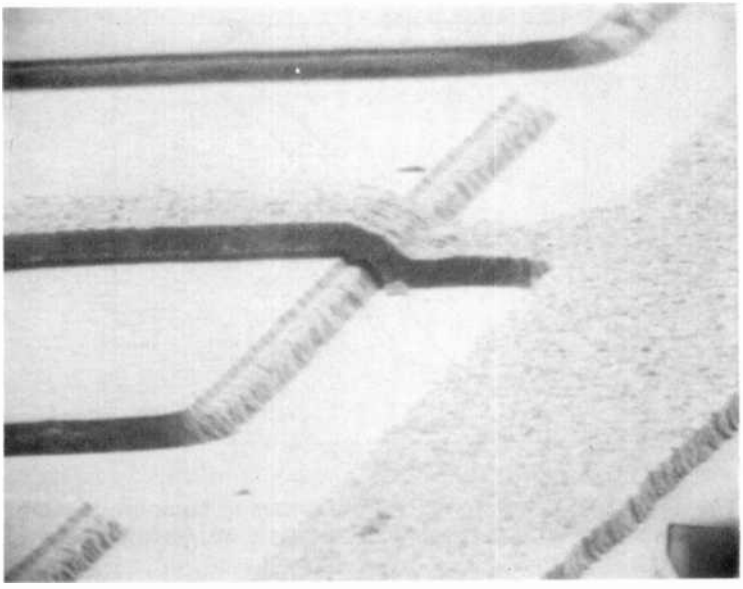


**Fig. 16**—SEM of island structure produced by the double-etched-island process.

form the ledge. Consistent results and island profiles such as those illustrated in Fig. 16 were not obtained with batch processing.

The types of fast-ramp characteristics obtained from arrays on wafers processed with the twice-etched island processes are illustrated in Fig. 17. In all cases, the contouring of the top edge did reduce gate leakage currents, but the effect on catastrophic-breakdown voltage was less well-defined. In the case of the double wet-etching process, gate breakdown voltage was generally reduced over that associated with the control and the dry-wet processes. This reduction is difficult to understand from the viewpoint of the structure produced, and may perhaps be due to the introduction of defects at some point in the process. On the basis of this work, it seems unlikely that a twice-etched island process would be viable for production requirements.

## 6.3 Sacrificial Oxidation

A number of experiments were done to determine if the growth and removal of an oxide layer could alter the dielectric behavior of devices. For these experiments silicon islands were etched in the usual way. After formation of the islands, the remaining oxide mask was stripped from the islands and an oxide layer was grown. This second

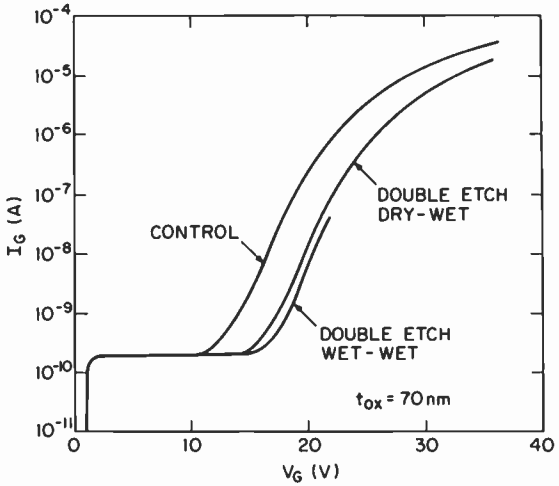



**Fig. 17**—Fast-ramp characteristics from arrays to compare two different twice-etched processes with the basic wet-etched process.

oxide film was then removed, and processing continued in the usual fashion. Based upon previous TEM results it was predicted[3] that such a sacrificial oxide must be grown to a thickness in excess of 100 nm, and it was found that, as measured on a bulk (100)-oriented wafer, the minimum thickness required to affect the dielectric integrity of devices is about 200 nm. The sacrifical oxides investigated were grown in steam at two temperatures, 900°C and 1100°C.

Consistent characteristics were obtained from fast-ramp measurements when the sacrificial oxide was grown to about 300 nm, and Fig. 18 illustrates typical characteristics of arrays. The lower-temperature oxidation process produces arrays with reduced gate leakage currents and with oxide breakdown voltages very similar to those of the control devices. In contrast, the higher-temperature process has very little effect on gate leakage currents and produces devices with breakdown voltages lower than those of the control arrays. These characteristics associated with the two processes were seen consistently in both arrays and single edge-type transistors. The data presented here seem to be in opposition to what one might expect based upon a recent study[21] of the oxidation of corners formed in silicon wafers; in Ref. [21], high-temperature oxidations are shown to create edge profiles with less sharp corners than those created by oxidation at low temperatures. In the absence of TEM profiles of our device structures, it is not possible to speculate about the results obtained here. It is of interest to note that the experiments described here were initiated prior to the publication of Ref.

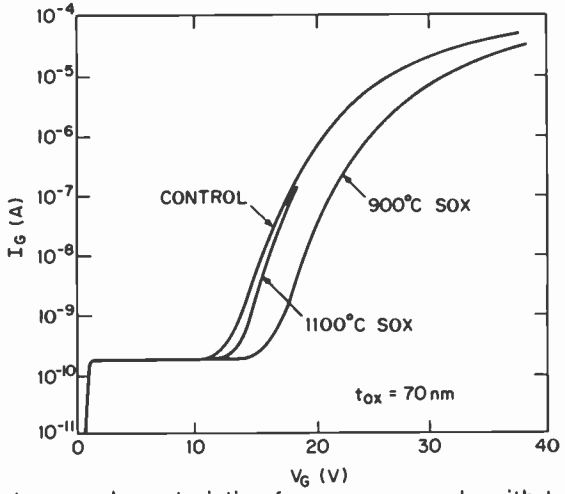



**Fig. 18**—Fast-ramp characteristics from arrays made with two sacrificial oxidation processes compared with the baseline process.

[21]; had this not been so, it is very possible that the lower temperature process, which produced the better results, would not have been attempted.

## 6.4 Implant-Damaged Material

An attempt was made to contour the top edge of the silicon islands by heavily damaging the material near the interface between the epitaxial film and the oxide etch mask prior to the etching of the islands. It was hoped, for example, that the damaged silicon would etch faster near the edge of the oxide mask, and in this way minimize the tendency to form a sharp or reentrant edge. For this experiment, wafer processing was done in the usual way, except that just prior to the definition of the oxide etch mask, the wafers were implanted with argon ions to a dose of $2 \times 10^{15}$ cm$^{-2}$. The implantations were done through the 70-nm-thick initial oxide film and two energies were chosen, 70 keV and 130 keV. The 70-keV implantation would be expected to create an implanted profile with the peak in the concentration at the silicon–silicon-dioxide interface, and the higher energy implantation would locate the maximum argon concentration about 35 nm further into the silicon. Hence, in one case a damaged zone was created that probably overlaped both the oxide and the silicon, and in the other case, the damaged zone was more concentrated in the silicon.

Array characteristics obtained from devices are shown in Fig. 19,

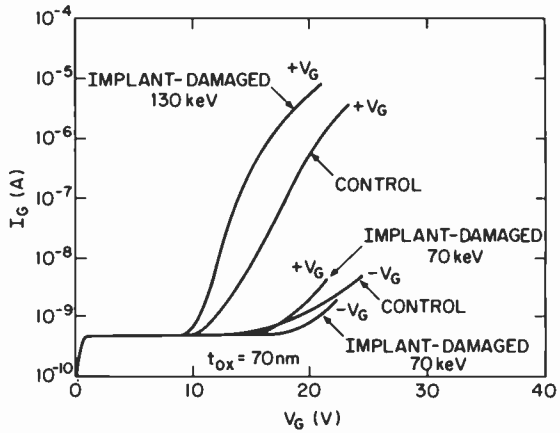



**Fig. 19**—Fast-ramp characteristics of arrays to illustrate the effect of implantation damage on dielectric integrity.

and the contrast in the results is quite dramatic. The deeper implantation degraded the oxide dielectric integrity and the more shallow implantation enhanced the characteristic. Note also that the 70-keV implantation not only reduced leakage currents but also tended to minimize the polarity dependence of the fast-ramp curves. This latter observation is strongly suggestive of a significant reduction in the sharpness of the edge of the silicon island. It is not possible to conclude anything about the effect of the damage implantation on the catastrophic failure voltage of the channel oxide from this experiment, because, as shown in Fig. 19, both the test and control devices exhibited low breakdown voltages.

The improvement in dielectric integrity created by the lower energy implantation suggests at least two mechanisms that could explain the presumed reduction in edge sharpness: a damage-induced enhancement of the nominally low etch rate of the oxide in the etching solution of the islands and a damage-enhanced etch rate of the silicon near the top of the film. In either case there would be a tendency to enhance the etching of the silicon at the position where the upper corner of the island is formed, and hence the formation of a sharp or reentrant edge would be less likely. Both of these mechanisms are consistent with reports that the etch rate of silicon dioxide[28] and silicon[29] can be increased by ion-bombardment damage.

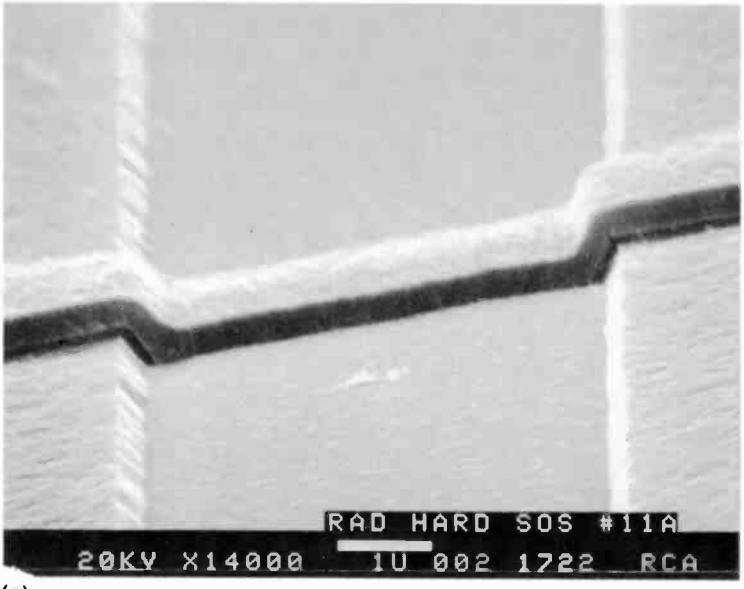
## 6.5 Laser-Contoured Islands

A more drastic approach to the formation of smooth contours on

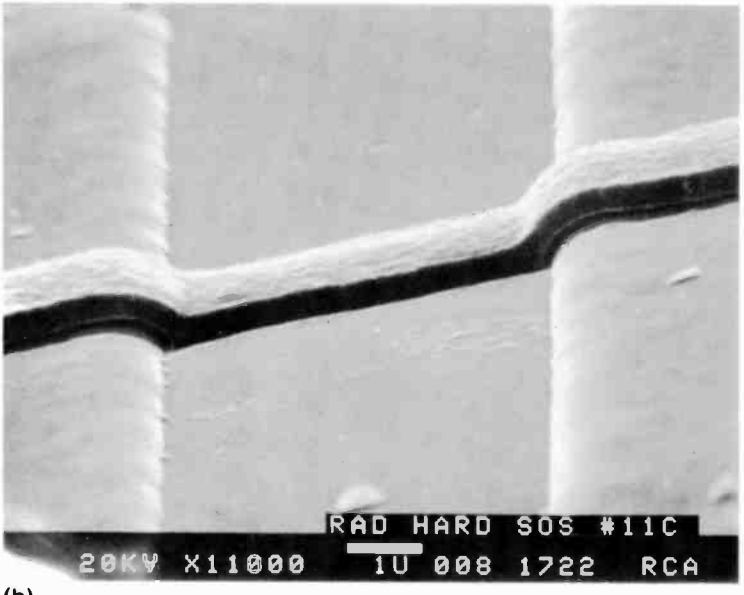
silicon islands is to melt the surface of the silicon, and a demonstration of this approach by use of a laser was described in 1979.[30] In that work a ruby laser was used, and the relationship between power density and the degree of edge rounding was shown. This early work was extended to include the fabrication of SOS devices for the evaluation of the electrical properties of transistors and arrays. For these experiments SOS wafers were exposed to the output of a pulsed, frequency-doubled, Nd:YAG laser just before the growth of the channel oxide; at this point in the process, only bare islands of silicon are present on the sapphire substrate. Halves of wafers were exposed at three different energy densities: 0.1 J/cm$^2$, 0.2 J/cm$^2$, and 0.3 J/cm$^2$. To illustrate the physical effect of the laser treatment, Fig. 20 shows SEM views of silicon islands with the polysilicon gate. Fig. 20(a) represents the structure produced by the wet-etching process, and Fig. 20(b) shows islands from the laser-treated portion of the same wafer. In the case of irradiation at 0.3 J/cm$^2$ illustrated, melting of the entire sidewall down to the sapphire appeared to have taken place. With this sort of sidewall structure, one might anticipate an effect on the dielectric integrity of the channel oxide.

To illustrate the fundamental effects of the laser treatment on dielectric integrity, Fig. 21 shows some typical fast-ramp characteristics. In general, it was found that the laser irradiation tended to reduce gate leakage currents, due presumably to contouring at the top corner of the silicon islands. At the lower energy densities, however, there was a clear tendency to degrade the breakdown voltage. At the highest energy irradiation the best results were obtained: gate leakage currents were reduced by many orders of magnitude and there appeared to be a slight enhancement to the catastrophic breakdown voltage of the channel oxide. This enhancement in breakdown voltage averaged-out to be about 5 V in one lot, but such an increase was not seen in a later lot.

To further describe the consequences of the laser treatment, Fig. 22 illustrates the effect of the polarity of the voltage ramp on the measurements. One observes that the strong polarity dependence of the typical control device characteristic is very much reduced by the laser irradiation; this suggests that the sharp corner of the island has been eliminated, such that electron emission from the epitaxial silicon and the polysilicon are not too different. Data to further substantiate the conclusions drawn from the fast-ramp characteristics are shown in Fig. 23, which presents a summary of data obtained from an automated stepped-voltage test. Recall that what is plotted is the value of gate bias at which 0.5 μA of gate leakage




(a)




(b)

**Fig. 20**—Scanning electron micrographs of island structures: (a) wet-etched and (b) wet-etched and exposed to laser irradiation at 0.3 J/cm$^2$.

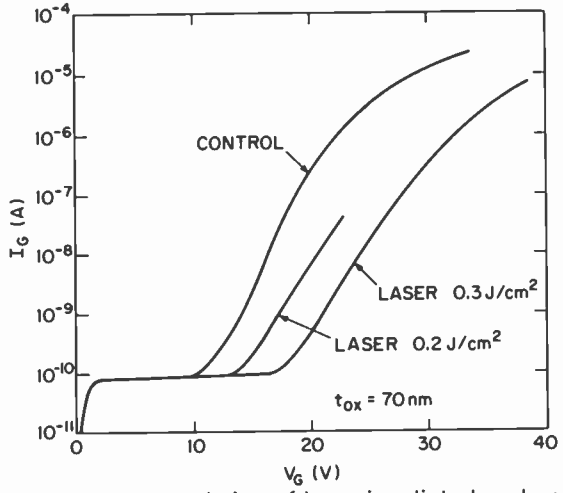



**Fig. 21**—Fast-ramp characteristics of laser-irradiated and control arrays.

current is detected, so that the data for the array of 500 devices in Fig. 23 can be compared with the characteristics at that current in Fig. 21. As seen, the agreement is reasonably good. The significant reduction in gate leakage current is, we believe, an important attribute to be associated with the use of a laser in the processing of SOS devices. In addition, at least some data suggest that an increase in dielectric breakdown voltage may be achievable.

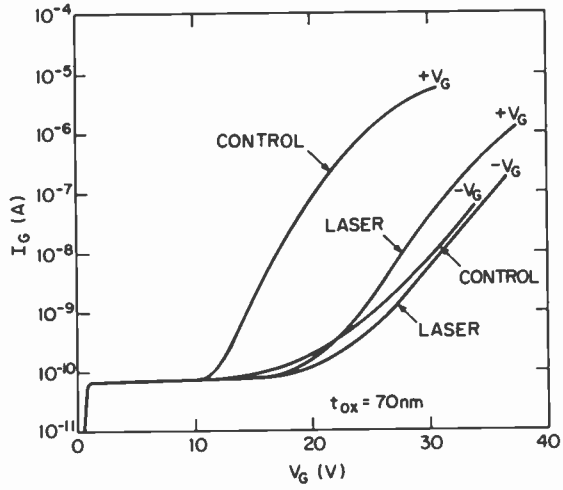



**Fig. 22**—Fast-ramp characteristics of both polarities from arrays laser-irradiated at 0.3 J/cm$^2$ and from untreated arrays.

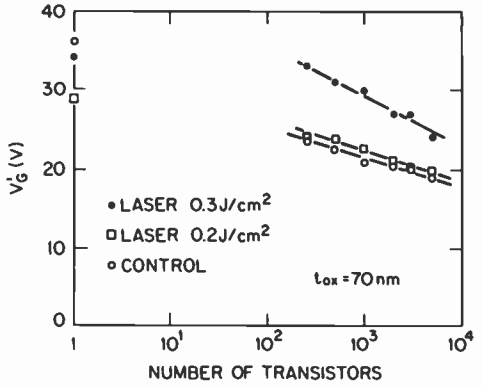



**Fig. 23**—Median gate bias at 0.5 μA versus the number of devices in the array from laser-treated and control arrays.

## 6.6 Dry-Etched Islands

In comparison with a wet-etching process for the fabrication of SOS islands, it was suspected that a dry-etching process would offer a number of advantages, some of which were described earlier.[31] In particular, for the purposes of this investigation, it was anticipated that a more consistent and reproducible island-edge contour could be defined. A number of approaches to the use of dry processing for the formation of SOS islands were considered, and processes for the fabrication of both vertically-walled and tapered islands were developed. As suggested by a previous publication,[32] it was found that a major criterion in the selection of a dry process for the definition of a silicon surface that will become part of an active MOS device is minimization of surface roughness. One particular process was found to consistently produce an enhanced dielectric integrity as measured by the suppression of gate leakage current, and Fig. 24 illustrates a typical fast-ramp characteristic obtained from an array made with this dry-etching process compared with the typical characteristic obtained from an array made with wet-etched islands. As observed with most other process modifications, however, there was no significant increase in the breakdown field strength of the array.

A particular advantage of the dry-etching process over others described in this paper is its relative simplicity. Other than the actual island-etching step, wafer processing does not differ from the processing associated with the wet-etched islands. It has been found that the dry-etching process can be easily implemented in a production environment, and that yields are quite satisfactory.[33] If required, it may well be possible to further enhance the dielectric integrity of devices made with the dry-etching process by use of one

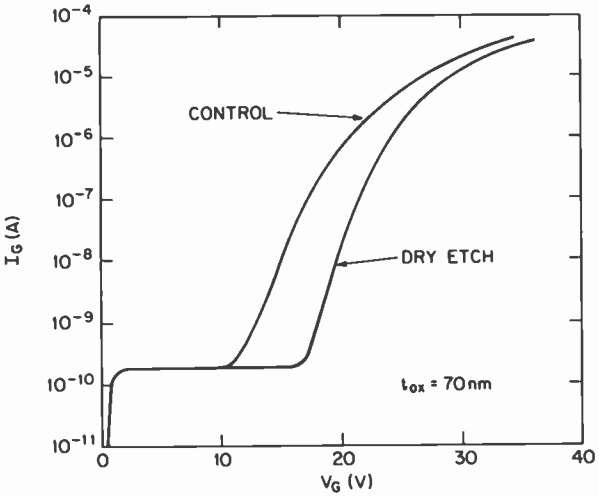



**Fig. 24**—Fast-ramp characteristics from arrays in which the islands were wet etched and dry etched.

of the techniques discussed earlier. Most of the methods used to contour the wet-etched SOS islands could also be applied to the dry etching process.

## 7. Summary and Conclusions

In this work we have attempted to elucidate some of the fundamental issues associated with the dielectric integrity of the channel oxide in an isolated-mesa SOS technology. Although channel-oxide dielectric integrity is not a fundamental limitation to the fabrication of SOS devices with current processes, it is expected that this issue will become more important (just as it has in bulk silicon technology) in advanced, thin-oxide, low-temperature processes. Of particular importance is the observation that there is a definite penalty in dielectric integrity associated with processes in which wafers with the channel oxide present are not exposed to temperatures above about 975°C. A healing mechanism associated with stress relief and viscous flow of the oxide is clearly absent in low-temperature processes, and the importance of such hydrodynamic considerations in oxidation processes was recently described in detail.[34] For this reason, a number of techniques to enhance the dielectric integrity of the channel oxide were investigated.

The data presented here show clearly, as have past studies, the important role of the island sidewalls in the determination of dielectric integrity. In the absence of sidewalls, it was found that

oxides grown on SOS material are dielectrically equivalent to oxides grown on bulk silicon. The presence of the island sidewall, however, produces approximately a 40% decrease in the gate breakdown voltage of a single transistor. The significance of the island sidewall was also demonstrated by the gate-leakage-current characteristics obtained from both arrays and single devices. In the case of arrays, it was shown that gate leakage currents scale directly with the number of edges rather than with the area of the gate, and a linear relationship between current and array size was found in arrays containing as many at 10,000 edges, which was the largest array available. This latter observation is, we believe, an indicator that gate-oxide integrity is not a fundamental limitation to the fabrication of high density, SOS circuits.

As described, gate-oxide leakage currents in SOS devices tend to be strongly dependent upon the polarity of the applied bias. The higher currents are always associated with a positive gate bias, and this suggests that the primary conduction mechanism is electron emission from the silicon island, presumably at the sharp upper edge. This supposition is supported by the results of experiments in which attempts were made to alter the contour of the island sidewalls; without exception it was found that gate leakage currents could be significantly affected by process variations directed toward changing the topography at the top edge of the island. Not only were gate leakage currents made smaller, but the sensitivity to polarity was reduced.

At the present time, very limited information concerning the exact physical structure created by the various experiments is available. Although extensive SEM work was done, it was our experience that the typical resolution available is not sufficient to provide much useful information. It was found, in fact, that one particular island structure which looked smooth and had tapered sidewalls produced devices with very high leakage currents and low breakdown voltages. Later TEM studies[35] revealed that the sidewalls were very rough and irregular, but on a scale which precludes resolution with a SEM. These observations emphasize the importance of electrical measurements, and our experience suggests that SEM views are of limited usefulness for the study of the effects of topographical modifications on dielectric integrity of SOS devices.

In contrast to the experimental results, which showed that oxide leakage currents could be affected by topographical modifications, the various processes had, with the possible exception of the highest-energy laser treatment, no significant effect on the catastrophic breakdown voltage of the devices. As the experiments were

directed primarily toward shaping the top edge of the island, it is very possible that oxide breakdown occurs at the bottom of the sidewall. The channel oxide is known[3,4] to be thin near the interface between the silicon and the sapphire, and, furthermore, it is not likely that the experiments, with the exception of the one laser treatment which appeared to have melted the silicon on the sidewall from top to bottom, affected the profile of the island sidewall near the bottom. Previous investigations also suggest that the bottom edge of the island is the critical area that determines gate oxide breakdown; planar processes[5,6] produce devices with higher breakdown voltages than isolated-mesa processes and isolated-mesa structures[36] with a very shallow sidewall angle with respect to the substrate surface have been shown to be superior to structures with steep sidewalls. In summary, it appears that the properties of both the top edge and the bottom edge of isolated-mesa SOS structures are important issues.

As indicated earlier, the gate leakage currents in SOS devices are, in general, strongly dependent upon the polarity of the gate bias; between the two polarities, currents can differ by more than three orders of magnitude. In contrast, the gate voltage at which destructive failure occurs is only weakly dependent upon the polarity of the gate bias. These observations are consistent with current flow controlled by the electric field at the cathode and breakdown determined by a local electric field, independent of polarity, in the oxide layer.

Based upon the research described here, the reliability data presented elsewhere,[10] and a detailed characterization of other device properties, dry etching has become the method of choice for the definition of silicon islands in all low-temperature and high-density SOS processes. Data indicate that the isolated-mesa SOS technology can be scaled to small dimensions and thin oxides without a significant reliability risk associated with the intrinsic dielectric integrity of the channel oxide. Circuits with 35-nm-thick oxides and 1.25-μm silicided gates are now in pilot production, and the data presented here suggest that no special problems are associated with these features. In the coming years we expect further reductions in device dimensions and corresponding increases in circuit density and complexity.

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# Reliability of CMOS/SOS Integrated Circuits

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**Abstract**—Reliability data for silicon-gate integrated circuits of various types are summarized. Included are failure rates for devices ranging from plastic-encapsulated commercial products to high-reliability hermetically-sealed integrated circuits for military and aerospace applications. Data are presented on devices fabricated by the original CMOS/SOS silicon-gate process and on devices prepared by advanced processes. These include lower wafer-process temperatures and improved wafer-processing techniques that permit thinner gate dielectrics and smaller feature sizes. Because they have fewer possible failure modes, CMOS/SOS integrated circuits have demonstrated a reliability at least equal to that achieved by bulk-MOS ICs.

## Introduction

Complementary-MOS integrated circuits based on the silicon-on-sapphire technology (CMOS/SOS) offer many advantages,[1-15] in-

cluding high circuit density, very high speed, low power dissipation during high-speed operation, substrate isolation, wide operating-voltage range, freedom from latchup, designability, scalability, and testability. CMOS/SOS has been the technology of choice for a number of advanced applications, and integrated circuits based on silicon-on-sapphire (SOS) technology are being fabricated in a number of organizations.

Presently available SOS ICs have benefited from improvements in SOS substrates, designs, materials, processes, and in-process controls, and thus both yield and reliability are superior to those of devices fabricated a number of years ago. New process improvements have been evaluated and applied to developing SOS devices.

The potential advantages of silicon-on-sapphire dielectrically isolated integrated circuits for radiation-hardened applications have been recognized for some time.[16–23] Techniques have been developed that further improve the radiation hardness of silicon-gate CMOS/SOS integrated circuits.[24–30]

The CMOS/SOS technology has many features that have reliability implications. Examples include freedom from the possibility of field inversion, freedom from the possibility of punchthrough or of parasitic lateral bipolar-transistor action between adjacent devices, freedom from the possibility of four-layer parasitic device latchup, freedom from problems due to vertical metal-spiking across source/drain junctions, no need for a grown field oxide, and the possibility of input-protection circuits that cannot be implemented in bulk-CMOS technologies. These CMOS/SOS-technology advantages become increasingly significant as integrated circuits are scaled to smaller dimensions.

An additional advantage of a dielectric-isolation technology is that it is easier to fabricate higher-voltage and radiation-hardened circuits because there is no possibility of field inversion, or of punchthrough to adjacent devices or to the edge of a well. By contrast, bulk-MOS processes involve a tradeoff between field-inversion voltage and avalanche-breakdown voltage. Ion implantation is used for bulk-MOS devices to increase field-inversion voltage; it is applied using a pattern that masks the channel region but allows overlap with the subsequently ion-implanted source and drain regions. This overlap is essential to achieve high-density circuits. Only SSI and MSI CMOS circuits can provide the space for a separate channel-stop diffusion that is located some distance away from source and drain regions.

The ability to fabricate integrated circuits that function at higher voltages than the intended application voltage has significant re-

liability implications, as it permits burn-in of circuits at high applied voltages, which in turn results in effective screening of failure mechanisms that are greatly accelerated by voltage but relatively insensitive to temperature. Two examples of failure mechanisms that are very effectively screened by high-voltage tests are time-dependent dielectric breakdown of gate oxides and hot-electron effects in short-channel MOS transistors. If CMOS/SOS integrated circuits are burned-in at 125°C and 11 V, for example, and are subsequently used in an electronic system under conservative conditions, such as 7 V at 55°C, both temperature and voltage acceleration factors can be applied to the calculation of estimated failure rate under usage conditions. If an electric-field acceleration factor of 0.06 mV/cm applies,[31] 11 V constitutes an acceleration factor of approximately three orders of magnitude compared to 7 V.

## Background

CMOS/SOS integrated circuits are produced in a pilot manufacturing line in the Government Systems Division, Solid State Technology Center (SSTC) in Somerville, N. J., and in the Solid State Division production line in Palm Beach Gardens (PBG), Florida. The SSTC pilot line has fabricated, packaged and delivered approximately 20,000 CMOS/SOS integrated circuits per year for the last four years.

Factory production of CMOS/SOS ICs was started in 1977, and production deliveries were made in 1978. By the end of 1983, more than four-million packaged CMOS/SOS integrated circuits had been produced. In 1982, CMOS/SOS microprocessors, A/D flash converters, and radiation-hardened LSI circuits were introduced. In 1983, radiation-hardened 4-kbit RAMs were introduced, and the feasibility of a 16-kbit radiation-hardened RAM was demonstrated.

## CMOS/SOS Processes

CMOS/SOS integrated circuits use an all-ion-implanted,[32] self-aligned, silicon-gate process, with n+ polycrystalline silicon gates for both p-channel and n-channel transistors. The basic silicon-gate CMOS/SOS process is shown in Fig. 1. Advanced processes are introduced that reflect current main-stream trends in MOS integrated circuit technology. The CMOS/SOS I silicon-gate process employs wet-chemical etching to pattern 0.6-μm-thick heteroepitaxial silicon-on-sapphire islands, 1000-Å gate oxides, and 5-μm feature sizes. The process reduces the tendency for gate-oxide thinning at

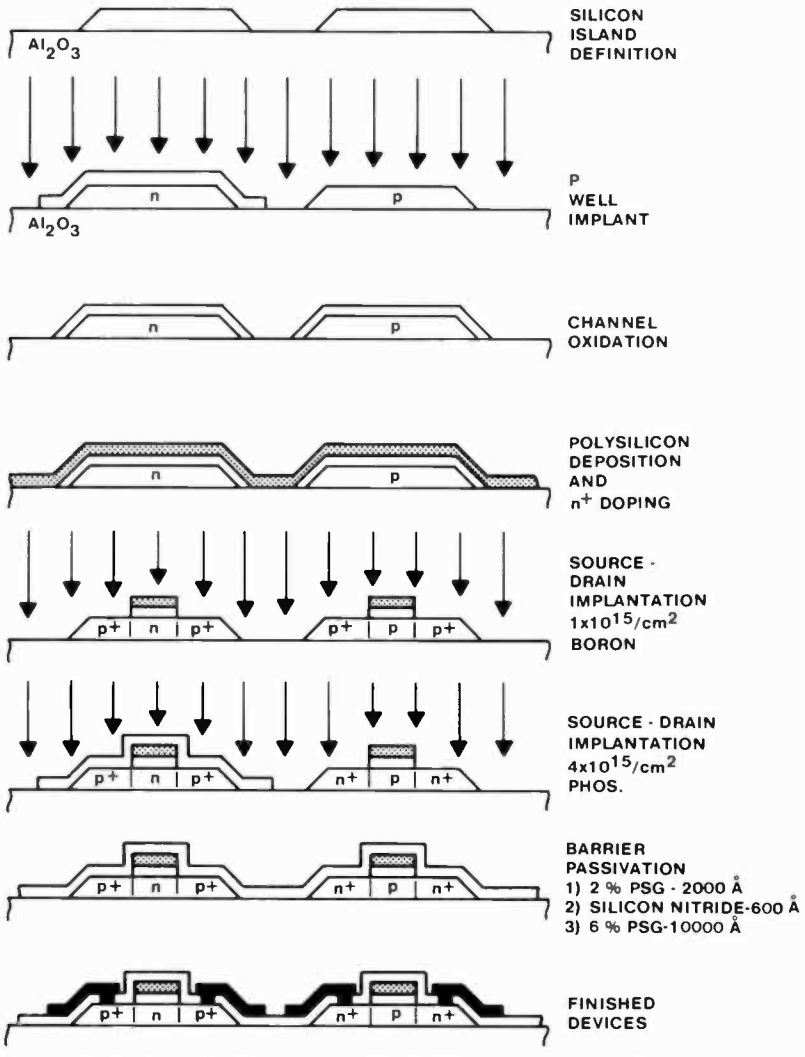


**Fig. 1**—Self-aligned silicon-gate CMOS/SOS process outline.

epitaxial silicon-island edges and, thus, provides high gate-oxide integrity. Passivation is provided by sequential deposition of a 0.2-μm-thick layer of 2% P-PSG, a 0.06-μm-thick layer of high-temperature-deposited silicon nitride ($Si_3N_4$), and a 6% P-PSG (or BPSG) thermally flowable layer.[33] The present processes thus provide for alkali-ion gettering of $SiO_2$ regions under the $Si_3N_4$ layer; the films are a barrier to the ingress of alkali, moisture, or other contaminants into gate-oxide regions.

## CMOS/SOS Integrated-Circuit Failure Rates

Much information has already been published on the reliability of various types of CMOS/SOS integrated circuits.[33–47] In this paper, we present recent data on the reliability of CMOS/SOS integrated circuits manufactured by RCA. Available data range from failure rates of plastic-encapsulated, commercial, CMOS/SOS integrated circuits to failure rates of high-reliability, hermetically-sealed ICs and high-performance 1-k and 4-k static RAMs. Data are also available on failure rates of CMOS/SOS RAMs during spacecraft-component burn-in and during in-flight satellite usage. Portions of the data reported have been summarized at recent technical meetings.[48–52]

## Reliability of CMOS/SOS I integrated Circuits—SSTC Pilot Line

Data on results of burn-in and static-life tests have been compiled for CMOS/SOS integrated circuits fabricated in the pilot line in SSTC. During the 1982–1983 time period, a total of 2,719 integrated circuits fabricated in SSTC by the CMOS/SOS I process (5-μm feature size, 1000-Å gate oxide) were processed through static burn-in at 125°C and 10V for 168 hours. Devices were tested at room temperature before the 168-hour static burn-in and then retested at high, low, and room temperature. Of the 2,719 devices tested after burn-in, 55 devices failed at high, low, or room-temperature, for a 98% burn-in yield. (The failed devices include those that did not initially function at high and low temperatures, as well as devices that degraded or became functional failures during the burn-in test.)

Integrated circuits that were screened by the above-described burn-in were subjected to a static-life test at 10 V at 125°C for 1000 hours.[52] Of 385 integrated circuits tested, there were no failures. The calculated failure rate for screened SOS I integrated circuits is 0.24%/1000 hours at 125°C, at a 60% confidence level. The extrapolated failure rate at 55°C (60% confidence level), calculated using a thermal activation energy of 1.0 eV, is 0.0005%/1000 hours (5 FITs).

## Reliability of Plastic-Encapsulated CMOS/SOS I integrated Circuits

CMOS/SOS integrated circuits for commercial applications are usually manufactured in plastic-encapsulated packages. Cost and per-

formance are major considerations, but high reliability is even more important. High reliability is accomplished through in-process controls. Real-time indicators (RTIs) are used to monitor the reliability in high-volume commercial production. Highly accelerated temperature-humidity-bias tests, high-temperature operating life, and in some cases accelerated mechanical tests are used. RTIs are short-duration accelerated-stress tests used to detect specific failure mechanisms that affect product reliability. RTIs monitor the reliability level to see that it meets design specifications; their use also tends to raise the level of reliability. Since they are accelerated tests, they can rapidly show the differences in lot capability and provide processing feedback.

Reliability test data are obtained from the evaluation of standard products and new-design verification tests. The following reliability data represent a summary of static bias-life testing in the 1982–1983 time frame.[53] The plastic encapsulated devices include the 128 × 8-bit RAM, the 1-k × 4-bit RAM, a transcoder, and a custom game IC. These devices were tested to data-sheet limits and not subjected to prescreening stress conditions, such as high-temperature-bias aging or high-voltage dynamic testing. Table 1 summarizes the accelerated-stress-test data for these plastic-encapsulated circuits.

Field data from one automotive company using the 1-k CMOS/SOS RAM circuit at the rate of 100,000 devices per year indicated one failure for the past year. With 400 hours operating time per

Table 1—Static Bias Life-Test Summary (Plastic Package)

| Test Conditions | Duration (Hours) | Out of Specification | Comments |
|---|---|---|---|
| Bias Life, 125°C, 7V | 1000<br>2000 | 1/143<br>0/20 | Leakage @ 168 Hrs. |
| Bias Life, 150°C, 7V | 1000 | 0/20 | |
| Bias Life, 175°C, 7V | 1000 | 2/13 | 2 Single-Bit Errors |

| Total Units Tested | Total Units Rejected | Equivalent Device-Hours @ Temp. | Failure Rate† %/1000 Hrs. |
|---|---|---|---|
| 196 | 3 | $0.61 \times 10^6$ @ 125°C<br>$15.6 \times 10^6$ @ 85°C<br>$301 \times 10^6$ @ 55°C | 0.34 @ 125°C<br>0.026 @ 85°C<br>0.0014 @ 55°C |

† The failure rate for CMOS/SOS technology has been calculated to a 60% confidence limit, and extrapolated based on a 1.0 eV activation energy. The tests criteria were defined as the data sheet limits.

circuit per year, the results are equivalent to $4 \times 10^7$ device-hours with one failure, which corresponds to a failure rate of 0.004% per 1000 hours. This field failure rate is consistent with predicted device-failure rates obtained by extrapolation of accelerated life-test data.

## Reliability of CMOS/SOS I: High-Rel-Program Gate Arrays and Memories

CMOS/SOS integrated-circuit reliability data have been compiled during performance of the high-reliability program, which involves fabrication and packaging of gate universal arrays (GUAs) and memory devices by RCA Solid State Division. The program includes four types of 632-gate GUAs and a 1-k RAM; modified Class S screening is used. Burn-in and test includes a 240-hour dynamic burn-in, with functional exercising of devices during burn-in. With a 3% PDA, 92% of the GUA lots passed first burn-in, and 100% of the GUA lots passed with 240-hour re-burn-in. For the four CMOS/SOS types of TA11093 (632-gate GUAs) tested from 1981 until mid 1983, a total of 153 lots was dynamically burned-in at 125°C at 11 V for 240 hours. These lots contained a total of 3,839 devices, which were burned-in for 921,000 device-hours, with 48 parametric/delta post-burn-in failures and two inoperative failures. Of the 153 lots, 13 lots (335 devices) received a second 240-hour burn-in with no failure of any kind (80,400 device-hours).

Systems-level life testing has been performed at 5.5 V for the four gate arrays and one memory device by the user. To date 1,632,000 device hours have been recorded with no rejects.

## Failure Rates of Screened High-Reliability CMOS/SOS ICs

In this section, screening and accelerated-life-test data are reviewed for several CMOS/SOS ICs, including 1-k RAMs, 4-k RAMs,[54] processors, controllers, and gate universal arrays. All manufactured parts were subjected to visual, mechanical, and electrical screens patterned after MIL-M-38510/50 series CMOS specifications. A simplified device-screening flowchart is shown in Fig. 2

Table 2 is a life-test summary of screened units stressed at 125°C at 7 volts or greater. A total of 2,045 devices were stressed for over $2.5 \times 10^6$ device-hours and tested to data-sheet requirements. Two devices were out of specification for leakage current; there were no functional failures. Using an activation energy of 1.0 eV, this data extrapolates to 2.0 FITs at 5V, 55°C, for the case of the out-of-specification devices, or 0.7 FIT for no functional failures.

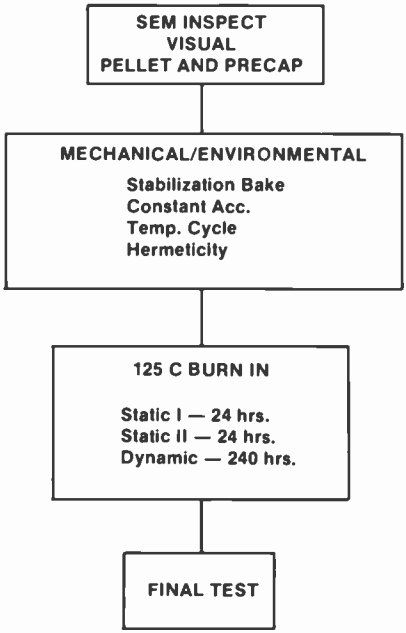


**Fig. 2**—Simplified device-screening flow chart.

In 1978, life-test results of 397 CDP1821 1-k RAMs were reported.[37] The barrier layer used for these RAMs consisted of sequentially-deposited layers of chemical-vapor-deposited $SiO_2$, $Si_3N_4$, and 6% P PSG reflow glass.

An additional group of 629 RAMs, fabricated by a modified CMOS/SOS I process, were life tested in 1982. The barrier layer was modified by the addition of 2% P to the CVD-$SiO_2$ layer.[33]

In 1983, devices of greater complexity, such as 4-k RAMs and processors, were fabricated with the CMOS/SOS II process. This lower-temperature thinner-oxide process is required for the increased performance specified for these parts. The 4-k RAMs are fabricated using a five-transistor memory-cell design and a buried-contact process.[54]

Many MIL specifications require control of the electrical parameters and monitoring of changes in those parameters ($\Delta$). Parameters, such as leakage current and output drive, are checked for changes. Table 3 shows the $I_{DD}$ distribution for a 1-k RAM, 1000-hour life tested at 7 V. The $I_{DD}$ changes were within the error of the measurement. These data are consistent with other parameters measured on many circuits. These parameters are defined in the CMM 5104/IRZ data sheet.[55]

Table 2—CMOS/SOS Life Test Summary for 125°C, $V_{DD} \geq 7$ Volts, Screened Units

| Type | SOS Process | Quantity | Device-Hours | Out of Specifications | |
|---|---|---|---|---|---|
| | | | | Leakage | Functional |
| 1821, 1k × 1 RAM | CMOS I (1978) | 397 | 752,000 | 1 | 0 |
| RAMS, Controller, Arrays | CMOS I (82–83) | 385 | 385,000 | 0 | 0 |
| 1821, 1k × 1 RAM | CMOS I (1982) | 629 | 706,000 | 0 | 0 |
| 1821, 1k × 1 RAM | CMOS II (1982) | 138 | 179,000 | 0 | 0 |
| 6P001 General Processor | CMOS II (1983) | 35 | 105,000 | 0 | 0 |
| 3P502 Controller | CMOS II (1983) | 45 | 45,000 | 1 | 0 |
| 632 Gate Universal Array | CMOS II (1983) | 25 | 31,000 | 0 | 0 |
| 1k × 4 RAM | CMOS II (1983) | 122 | 95,000 | 0 | 0 |
| 4k × 1 RAM | CMOS II (1983) | 269 | 262,000 | 0 | 0 |
| Total CMOS I and CMOS II | | 2,045 | 2,560,000 | 2 | 0 |
| Failure Rate % per 1000 Hours, 125°C, 7 V | | | | 0.12 | 0.035 |
| Rate Extrapolated to 55°C, 5 V (1.0 eV), Failures per $10^9$ Hour (FITs) | | | | 2.0 | 0.5 |

## Process Monitoring and Control

Process reproducibility and control are important requirements for reliable circuits. RCA has instituted process controls for all commercial and high-reliability CMOS/SOS products. These controls exceed the requirements of MIL/STD-883C, a MIL standard establishing the requirements for lot-acceptance testing of microcircuit wafers intended for Class S use. Table 4 lists some process controls that are a standardized part of the PBG production line and the requirements of MIL-STD-883C.

High-temperature/voltage stress of the gate oxide is another tool used to predict threshold stability during bias life. Fig. 3 shows a single inverter circuit that stresses the n and p gate oxide. Fig. 4 shows no threshold shift on the inverter after the gate oxide has been stressed in ceramic packages at 150°C and 7V for 500 hours.

Table 3—$I_{DD}$ Distribution for 1-k RAM Life Tested at 7 V

| | Descriptive Statistics | | |
|---|---|---|---|
| | 0 Hours | 500 Hours | 1000 Hours |
| Number of Devices | 77 | 77 | 77 |
| Mean (μA) | 69.36 | 66.94 | 69.40 |
| Std Dev. | 38.98 | 36.88 | 37.99 |
| Data Min. | 11 | 10.5 | 11 |
| Data Max. | 191 | 192 | 191 |
| Data Range | 180 | 181.5 | 180 |
| Standard Error of Mean | 4.44 | 4.20 | 4.33 |

Maximum Allowable $I_{DD}$ = 260 μA

These gates were stressed with an acceleration factor of $3 \times 10^3$ relative to 55°C usage (based on a 1.0-eV activation energy). Even with this large acceleration factor, there is no measurable sodium contamination.

In addition to the electrical stability required, Class S requirements include SEM examination of metal step coverage consistent with MIL-STD-883. The required step coverage is achieved by proper circuit design rules and by use of a reflow-glass process that contours all steps and contacts. A 6% P PSG reflow glass, fused at 1,050°C, provides excellent step coverage in CMOS I devices. Where lower reflow temperatures, such as 950°C or 850°C, are required, borophosphosilicate glass (BPSG) provides smooth surface topology.[56] Fig. 5 is an SEM photo of a 4-k RAM's contact metal over a flowed BPSG layer. The BPSG glass provides low-temperature reflow and, thus, permits excellent step coverage with the high-performance CMOS/SOS II process. All SOS parts consistently meet this MIL-STD SEM requirement.

## Tiros Spacecraft Reliability Data

The CMOS/SOS RAMs described in this paper have been used in spaceborne Tiros and Defense Meteorological Satellite memories since 1978. The RAMs operate at 5 V or 10 V with a maximum temperature of 30°C. In addition to in-orbit time, there is extensive testing at spacecraft levels. These data are summarized in Table 5. As of March 16, 1984, RAMs had operated more than 45-million hours with no failures.[57] Three soft errors were observed during a period of extensive solar-flare activity.This low failure rate is consistent with the inherent CMOS/SOS cosmic ray sensitivity of $<10^{-9}$ errors/bit/day.

Table 4—CMOS/SOS Process Inspection and Controls

| Process | Controlled Parameters | MIL Standards 976 and 883C Requirements |
|---|---|---|
| Epitaxial Wafer | Crystallinity; Thickness; Flatness | NHB-5300 |
| Photomasks | Laser inspection after specified usage | Defect level defined |
| Thermal Oxide | Thickness; CV shift ($V_T \leq 0.4$ V for 1000Å $SiO_2$) | |
| Polysilicon | Thickness, Grain Size | |
| Polysilicon Conductivity | 4-Point probe | |
| Ion Implant | Energy; Conductance of control chip | Controls and documentation required |
| Reflow Glass | Thickness; EDAX composition; Flow characteristics; SEM | Controls and documentation required |
| Al Metallization | Thickness (>8000Å, ±20% of design nominal, 6000Å min); CVBT shift (evaluate sodium concentration); Metal purity | |
| Passivation Overcoat | Thickness; Composition | |
| Electrical Wafer Acceptance Test on SOS Test Key | N and P threshold voltage; Source—drain breakdown voltage; transistor gain; Device leakage current; Contact resistance to Si islands and to polysilicon | MIL Std 976 |
| Thermal Stability | Controls at metal evaporation and oxide growth ($\Delta V_T \leq 0.4$ V normalized for 1000 Å oxide) | |
| SEM | All lots for military applications | Method 2018 required for class S only |
| Product Assurance | Quality control organization; Calibration; Process documentation | MIL-Std-Cp 45662 |

## Accelerated Stress Testing of Advanced CMOS/SOS Processes (SOS III)

In parallel with the development of CMOS/SOS processes capable of fabricating VLSI arrays with increasingly finer geometries, the reliability of arrays produced with these advanced processes is constantly monitored. Since 1981, a continuing study of the reliability of advanced short-channel CMOS/SOS arrays has been carried out.

Throughout 1982, the reliability studies were concerned with ar-

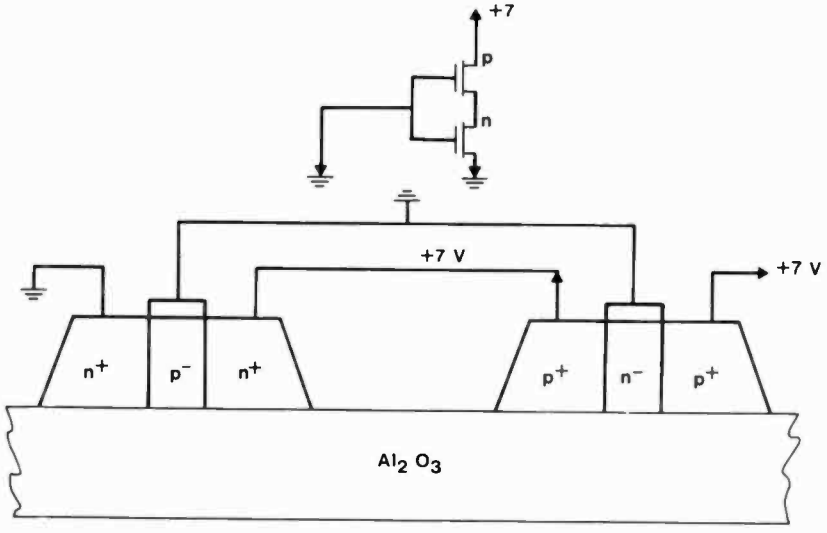


**Fig. 3**—Inverter bias circuit for accelerated life tests.

rays produced by the SOS III process.[52] This process uses 500 Å of gate oxide, a 3μm n+ polysilicon gate, negative photoresist, arsenic and boron source-drain implants, and a triple layer of chemical-vapor-deposited dielectric consisting of 2% PSG/$Si_3N_4$/6% PSG.

An arithmetic logic unit (ALU) containing approximately 1,300 transistors was the test vehicle used in the reliability studies. These arrays were fabricated, packaged, data logged, and stress tested. Throughout 1982, static-bias accelerated stress tests were per-

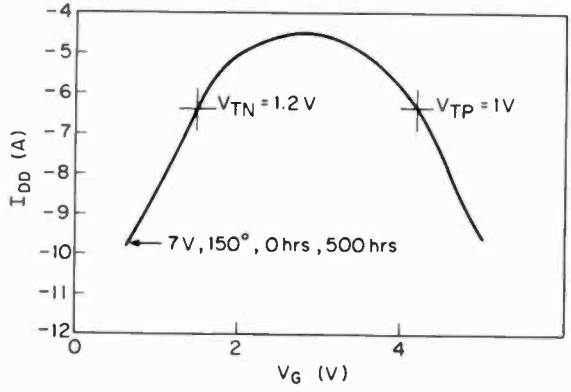


**Fig. 4**—Data from inverter bias circuit showing threshold stability after stress at 150°C at 7 V for 500 hours.

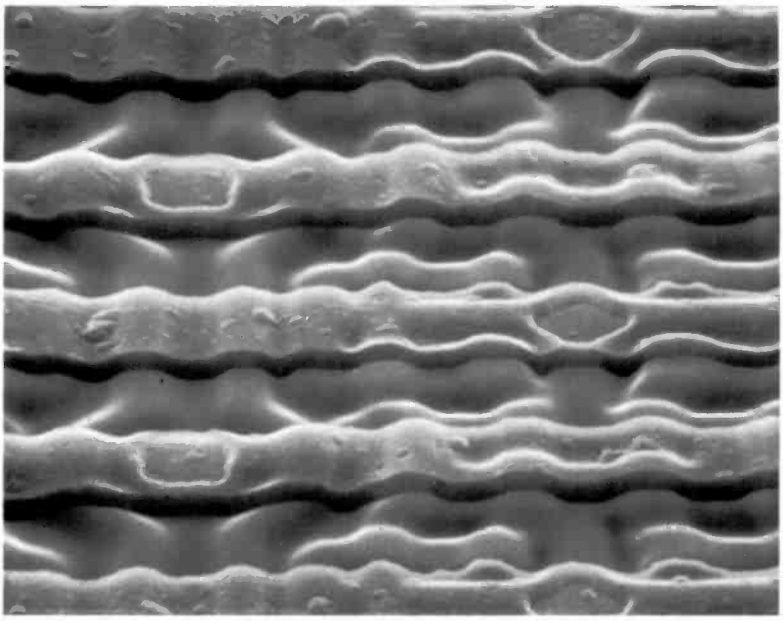

**Fig. 5**—SEM showing contact metal over a flowed BPSG layer for 4-k RAM (original magnification 2000×, 55°).

formed at 175°C and at 250°C with 6-volt bias on 52 ALU's representing three lots. The median time to failure for each sample was 2,600 hours and 170 hours, respectively. All the devices in these tests remained fully functional; the out-of-specification arrays exceeded an arbitrary limit of $I_{DD} = 100\ \mu A$.

An additional thirty-two ALUs were subjected to an accelerated stress test at 250°C and 6 V with the input terminals dynamically exercised. Several devices experienced increases in leakage current within the first twenty-four hours; however, there were no additional increases in leakage current, and all devices were functional when the test was terminated at 456 hours. A comparison of this result with those of the 175°C and 250°C static-bias tests shows that this result is consistent with a mobile alkali-ion drift, the most common MOS device failure mode. This observation, together with analysis performed on some of the devices that displayed increased leakage currents after accelerated life tests, confirm these mechanisms.

ALUs that were fabricated during the first quarter of 1983 with the SOS III process are being subjected to static-bias accelerated stress tests at 200°C and at 225°C with 6-V bias. Seventy-three

Table 5—DMSP and TIROS Meteorological Satellite, Spacecraft On-Orbit and Spacecraft Level Stress Testing (CDP 1821 1-k SOS RAM Survival Data)

| Spacecraft | Launch Date | Days as of 3/16/84 | Hours as of 3/16/84 | 1-k RAM Qty/SC | Part-Hours |
|---|---|---|---|---|---|
| DMSP 5D-2 S6* | 12/20/82 | 452 | 10,848 | 952 | 10,327,296 |
| DMSP 5D-2 S7 | 11/17/83 | 120 | 2,880 | 952 | 2,741,760 |
| TIROS-N | 10/13/78 | 464 | 11,136 | 306 | 3,407,616 |
| TIROS NOAA-E | 3/28/83 | 354 | 8,496 | 680 | 5,777,280 |

Spacecraft Level Testing = 22,794,960 Part-Hours
Total Part-Hours = 45,048,912, No Device Failures

* S6 exhibited three occurrences of parity errors between 21 and 58 days of operation. Source/location of errors could not be determined. Failures were not "hard".

arrays are currently on test. To date, the baseline devices at 225°C have accumulated 6,900 hours, with seven devices exceeding the leakage-current limit; the devices at 200°C have accumulated 5,500 hours, with 15 out-of-specification. Ten of these occurred early in the test (within the first 144 hours) and would have been screened out with a standard burn-in. Of these, three were nonfunctional, six were the result of increases in leakage current without loss of functionality, and one was the result of electrostatically induced damage attributed to mishandling. The remaining arrays categorized as out-of-specification suffered from increases in power-supply leakage current after they had been on test in excess of 2,000 hours.

The results of these accelerated stress tests are summarized in Table 6. Extended stress test times are required to produce approximately 75% failures in each test sample. The device hours accumulated by in-specification devices are extrapolated to the operating temperatures of 55°C, 85°C, and 125°C using an activation energy of 1.0 eV. The predicted failure rate at 55°C of 1.5 FITs is consistent with the CMOS/SOS database.

The technique of characterizing the reliability of a process by static-bias accelerated stress tests is being employed to demonstrate the viability of any new CMOS/SOS process. Now that the reliability baseline is established, this technique evaluates process variations by comparing the predicted reliability of the variant with that of the baselined process. A quick and accurate appraisal of a process variant is now possible for processes such as low-temperature LPCVD polysilicon gates,[58] reactive ion etching, or double-level metal.

## Discussion

Accumulated data show that the process sequence and controls used for CMOS/SOS circuit fabrication in both RCA's Palm Beach Gar-

Table 6—CMOS/SOS Static Bias Accelerated Stress Test

| Test Conditions | Duration (hours) | Out of Specifications | Comments |
|---|---|---|---|
| 175°C, 6V | 6500 | 25/31 | $I_{DD}$ in excess of 100 μA. Devices are functional at final test point. |
| 250°C, 6V | 240 | 15/19 | $I_{DD}$ in excess of 100 μA. Devices are functional at final test point. |
| 225°C, 6V | 6900 | 7/22 | $I_{DD}$ in excess of 100 μA. Devices functional at 4882-hour interim test, continuing on test. |
| 200°C, 6V | 5564 | 15/75 | $I_{DD}$ in excess of 100 μA. All but 3 devices functional, remainder continuing on test. |

| Total Units Tested | Out of Spec. Devices | Equivalent Device-Hrs | Failure Rate* in FITs |
|---|---|---|---|
| 147 | 62 | $86.1 \times 10^6$ (125°C) | 740 |
| | | $2.3 \times 10^9$ (85°C) | 28.6 |
| | | $43.0 \times 10^9$ (55°C) | 1.5 |

* Failure rates for the CMOS/SOS III technology have been calculated using a 60% confidence level and extrapolated based on 1.0 eV activation energy. All devices were processed and packaged at SSTC, using commercial assembly (no screening) and hermetic ceramic packages.

dens, FL, and Somerville, NJ, facilities produce devices that meet all commercial and military requirements for stability and reliability.

The most common failure mechanisms for all types of silicon-gate MOS integrated circuits are alkali-ion migration effects and time-dependent breakdown of thermally grown oxides. The predominant failure mechanism of CMOS/SOS integrated circuits during high-temperature bias-life testing has been parametric, an increase in $I_{DD}$ leakage, rather than functional, or catastrophic, failure. This type of failure is believed to be due to the motion of sodium ions in $SiO_2$ in an electric field and is characterized by an activation energy on the order of 1.0 eV.

In predicting IC reliability in accordance with MIL-HDBK-217 D[59] and Notice 1,[60] a learning factor ($\pi_L$) of 10 is used for new technologies. A $\pi_L$ of 1.0 is used when production conditions and controls have stabilized (after 4 to 6 months of continuous production). CMOS/SOS has been in production since 1978. The current RCA low-temperature CMOS/SOS wafer-fabrication process has been in production since August 1982; accordingly, a $\pi_L$ of 1.0 is considered appropriate for use in the prediction of reliability of all RCA CMOS/SOS integrated circuits.

A comparison of the observed failure rates of CMOS/SOS integrated circuits with data on failure rates of MOS integrated circuits based on bulk-silicon substrates[36,41,42,45,61–70] indicates that CMOS/SOS integrated-circuit reliability is comparable to that of devices fabricated by bulk-MOS technologies (CMOS, NMOS, PMOS).

## Conclusions

CMOS/SOS integrated circuits have been in volume production for more than five years. Initial devices were based on 5-μm feature sizes and 1000-Å gate oxide. Newer devices have evolved to smaller feature sizes and have used thinner gate oxides and lower processing temperatures to achieve performance advantages. The failure rate at 125°C, 7 V, is 0.1/1000 hours for screened parts; this number extrapolates to a failure rate for CMOS/SOS integrated circuits of one FIT at 55°C at 5 volts, to a 60% confidence level. Accelerated stress analysis of new high-performance circuits demonstrates a capability comparable to the production circuits. Analyses of failed devices from screened and plastic-encapsulated circuits indicate no new failure mechanisms attributable to the silicon-on-sapphire technology.

Analysis of field data in device applications, such as automotive and space, demonstrates low failure rates consistent with those predicted by the accelerated stress techniques reviewed in this paper.

Both the CMOS/SOS technology and the bulk-CMOS technology are evolving as design and wafer-processing trends are applied to achieve improved circuit performance and higher density. The advantages of the CMOS/SOS technology relative to the bulk-CMOS technology continue to be applicable as transistors in ICs are scaled to submicron dimensions.[71] Accordingly, it is predicted that the use of CMOS/SOS technology will continue to increase, particularly in those advanced applications in which designability, speed, density, and dielectric isolation are important.

## Acknowledgment

The authors gratefully acknowledge the contributions of D. R. Carley, who directed most of this effort, J. Hale for the data on plastic-encapsulated CMOS/SOS, and R. Nearhoof for the High-Rel Program results.

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# Reliability of Plastic-Encapsulated Integrated Circuits in Moisture Environments

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**Abstract**—An overview of the factors affecting the reliability of plastic-encapsulated ICs in moisture environments is presented. Particular attention is given to the moisture-related failure mechanism EMA (electrolytic metal attack). The package design and process steps and techniques developed at RCA (through identification of the proper analytical models, thorough engineering programs, and by the statistical design of experiments) are detailed. Particular attention was paid to eliminating chlorides and their sources. The nature and state of on-going plastic-package moisture-resistance programs and future expectations are described.

## Introduction

Plastic-encapsulated integrated circuits are the predominant devices used by electronic-system manufacturers, primarily because of their significantly lower cost and improved mechanical strength. The use of plastic materials brings with it certain reliability issues that must be resolved. The most important of these is the ability of a plastic package to resist various temperature and humidity conditions or, simply, its moisture resistance capability. This paper presents several advances in the wafer and assembly processes used by RCA that have resulted in increased reliability of the plastic package. The data reported are the result of more than sixty statistically designed experiments that were conducted to determine the significance of changes in the plastic-package system.

## Plastic Package System

In the design of any plastic package system for a semiconductor device, no single design factor is predominant. There is a tendency to believe that the entire issue is determined by the selection of plastic materials, that is, that a single plastic material will solve all problems in plastic-encapsulated-device reliability, but this is not true. Table 1 indicates the many factors involved in the design of packages for a plastic system, any one of which can be a complete study in itself. When designing a plastic package, all these factors must be considered as part of an experimental design because there can be an interaction between them.[1] Attempts to improve the plastic package by simply changing materials and formulations can cause more problems than they solve.

Fig. 1 illustrates the present RCA plastic system for most narrow body (0.250-inch) packages. The basic components of the plastic package are a lead frame on which the chip is mounted and wire bonded and the plastic case material that provides mechanical protection. By definition, the plastic package is nonhermetic but, prac-

Table 1—Plastic-System Package-Design Factors

| |
|---|
| Chip Design, Process, Junction Seal |
| Silicon Dioxide |
| Silicon Nitride |
| Metallization |
| Aluminum, Aluminum-Silicon |
| Gold |
| Passivation (over Metal) |
| CVD PSG (Chemical Vapor Deposited Phosphosilicate Glass) |
| Plasma-Deposited Nitride |
| Silicone Resin |
| Chip Mounting |
| Epoxy |
| Eutectic |
| Polyimide |
| Lead Frame or Header Material Connections |
| Wire |
| Plastic |
| Epoxy (Low Chloride, Low Stress) |
| Plastic Mechanical Strength |
| Plastic Thermal Stability |
| Plastic to Lead-Frame Adherence |
| Plastic Molding-System Requirements |
| Time |
| Temperature |
| Pressure |
| Post-Mold Cure |

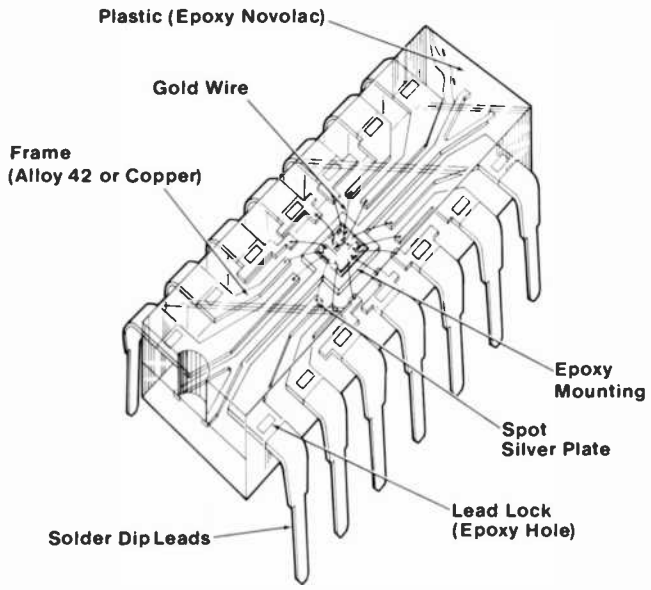


**Fig. 1**—RCA dual-in-line plastic (DIP) 14-lead package.

tically, due to the potential for chemical reaction of the circuit metallization, a degree of "hermeticity" is necessary to protect the chip.

Cost is the primary reason for the use of plastic packages; a hermetic package may cost three to ten times more than a plastic package. Moreover, the plastic-package components lend themselves to assembly by mechanized techniques, resulting in improved yields and quality and lower assembly costs by eliminating manual handling and operator error. In this study, 8-, 14-, and 16-lead packages were included (Fig. 2 shows the 14-lead package). Each package can pose different problems in designing for reliability. For example, the 8-lead package, because of size, has a different leadframe design, and the amount of material around the chip is less than that around the chip in packages of larger lead counts. Thus, when silicon devices fabricated by the same chip technology are put in different types of packages, reliability results for each can be different.

In the design of the plastic package, the chip size and its layout play an important role. If the chip is too large for the package, the walls surrounding the chip can be very thin, and the amount of plastic material available to protect the chip from the external environment can be inadequate. Obviously, this condition in itself can

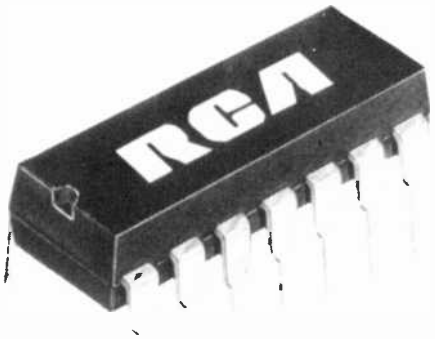


**Fig. 2**—Photograph of 14-lead dual-in-line plastic package.

result in a potential moisture problem, since the plastic material is the first line of defense.

In addition to the chip size and layout, consideration must be given to the lead-frame material, the chip-mounting method, the chip-to-frame interconnection, encapsulation materials, and lead finish. Also, because plastic packaging assembly is done in very high volume, automation of the assembly is a necessity. A mechanized system is needed, not only to produce the volume required, but to ensure consistent quality. Again, this mechanization allows a reduction of operator error and reduces handling of the product as it is being manufactured.

In 1982, RCA established a comprehensive mechanization program in Malaysia for the high-volume assembly of 8-, 14-, and 16-lead plastic packages.[2] In this manufacturing process, the wafers are mounted on a tape and then saw cut to separate them into individual chips. The sawed wafers are cleaned and the chips inspected. The chip matrix is then presented to a chip mounter which automatically mounts the chip on the lead frame prior to interconnection by fully automatic wire bonders. Since the bonders have a pattern-recognition function, all the operator has to do is to set up the machine once; it then runs continuously. The operator simply loads product and monitors the machine's performance. The wafers then go through the molding and the lead finishing equipment. Automatic solder dipping and automatic branding complete the mechanized system sequence.

Because the plastic package is nonhermetic, the most significant environmental factor affecting reliability is moisture.[3] (In a her-

metic package, the moisture environment is not a consideration; only the moisture sealed in the cavity during assembly is of concern.) Therefore, with a plastic package, as a first consideration, the moisture environment of the application and the moisture resistance of the package as defined by reliability test data must be related.

## Factors Affecting Moisture Resistance

Table 2 highlights the many variables that determine the ultimate moisture resistance of a plastic package. Of these, the device technology (e.g., bipolar versus CMOS) is a key one because of power dissipation[4] and the effect of this dissipation on reliability-test results. For example, when devices of two different technologies are placed on THB (temperature-humidity-bias) test in 85% relative humidity, and one, because of its technology, dissipates power in such a way that its junction temperature is perhaps 10 degrees greater than the ambient, the relative humidity at the chip surface of that device will actually be 58%, and not the 85% at the junction of the lower-power unit. Thus, bipolar devices, which dissipate more power than CMOS devices, sometimes yield better test data than

Table 2—Variables Influencing the Reliability of Plastic Packages In Moist Environments

| |
|---|
| Technology |
| Bipolar |
| CMOS |
| Design Layout |
| Chip Size |
| Metallization |
| Protect Layer |
| Packaging |
| Lead Frame Design |
| Lead Frame Base Material |
| Chip Mounting Method/Materials |
| Encapsulation (Plastic) Material |
| Molding System Parameters |
| Plastic Cure Schedule |
| Plating (Finish) of External Leads |
| Contaminants |
| Adhesion to Chip & Lead Frame |
| Application |
| Moisture Environment |
| Temperature |
| Applied Voltage |

CMOS devices under like conditions. In most humidity tests on linear bipolar devices, even when the power is reduced and an attempt is made to "cut-off" the devices by reverse-biasing, they will still dissipate milliwatts of power and change the test conditions.

Two important application-environment factors that influence moisture resistance are temperature and applied voltage. Fig. 3 indicates how failure rate changes as a function of voltage. A substantial improvement (approximately 5 to 1) can result from reducing the device voltage (from 18 volts to 5 volts). This phenomenon is significant with the latest CMOS silicon-gate technology, CMOSII (RCA's high-speed product, QMOS),[5] which is a 5 to 6-volt technology, compared to the 4000-series CMOS, which may be operated at up to 18 volts. The lower the voltage used in an application, the better the reliability that can be expected.

Other factors affecting moisture resistance include the protect layer over the metallization, the method of packaging, the materials used, the molding-system parameters, the lead-frame design, the adhesion of plastic to chip and lead frame, the contaminants in the system, the plastic cure schedule, and the finish of the external leads. All these factors influence the degree of moisture resistance of a package, that is, the degree to which the package prevents a

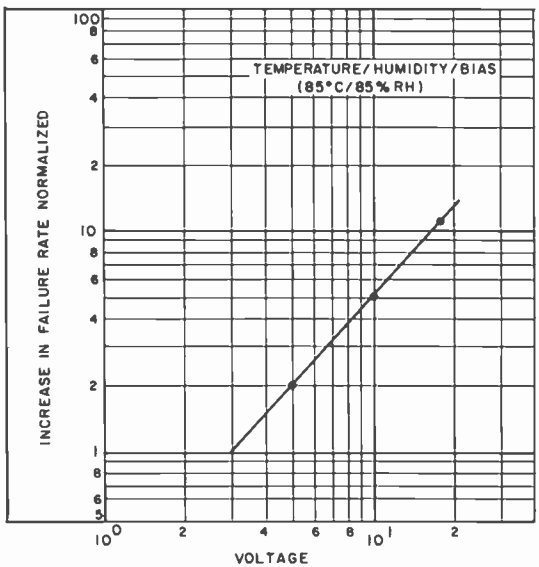


**Fig. 3**—Effect of voltage on the moisture mechanism for CMOS logic.

device from failing as the result of a mechanism triggered by the presence of moisture in the package. One of the most serious of these mechanisms is aluminum corrosion, a mechanism precipitated by the presence of contaminants and moisture in the package at final assembly or introduced in the application.

## Mechanism of Aluminum Corrosion

Three types of corrosion, or electrolytic metal attack (EMA), can take place in a plastic package: galvanic cell (dissimilar metals), concentration cell (Nernst equation), and ionic cell.[6] The amount of EMA that takes place is a function of the many factors listed in Table 3; a number of these factors must be present for EMA to occur. The abundance of these factors gives a good idea of why the attainment of plastic-package reliability is so difficult. From the time a plastic package is assembled to its final application, its lack of hermeticity leaves it "open" to exposure to a variety of adverse conditions.

One of the most severe of these conditions for the plastic package, and one of the main causes of corrosion, is the interaction of moisture with chlorides.[7] The package materials and processes in use today at RCA minimize the amount of chloride content, as is explained below, but chlorides may still be prevalent in many processes to which the package may be subjected after manufacture.

The problem begins with a tendency, during lead forming, for a separation to occur between the lead frame and plastic at the point where the leads enter the package body. This separation allows contaminants (e.g., chloride) to migrate along the wire, onto the chip, and then onto the exposed aluminum bond pads where the gold-ball bonds are made (Fig. 4). The interface of dissimilar metals, gold to aluminum, sets up an approximately 3-volt potential, and

**Table 3**—Factors Determining Amount of Corrosion of Integrated Circuit Metallization

| |
|---|
| pH of System |
| Metal |
| Encapsulation Material |
| Passivation Glass |
| Ionic Contamination |
| Temperature |
| Relative Humidity |
| Applied Voltage |
| Moisture Resistance of Package |

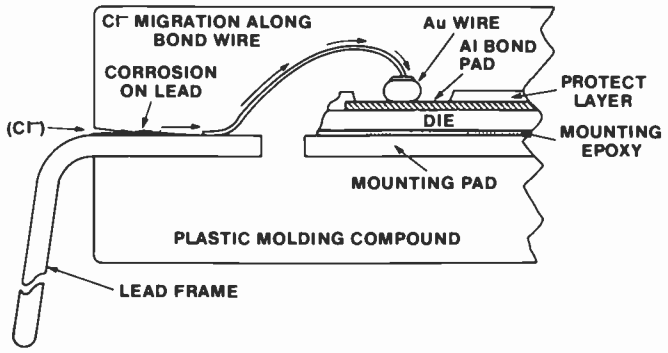


**Fig. 4**—Dual-in-line plastic-package—model of chloride-induced EMA. The path for $Cl^-$ ions is shown, with the primary area affected being Al bond pads.

in the presence of water and chloride, an EMA reaction can take place.

The equations for the EMA reactions involving chlorides are as follows.[8] Metallic aluminum and its alloys are normally protected from atmospheric conditions by a layer of passivating oxide. The oxide is dissolved in a moist environment from the adsorption of $Cl^-$ on the surface according to the reaction:

$$Al(OH)_3 + Cl^- \rightarrow Al(OH)_2Cl + OH^-.$$

After the surface oxide is dissolved, the exposed metallic aluminum then reacts with the chloride ion as follows:

$$Al + 4Cl^- \rightarrow [AlCl_4]^- + 3e^-.$$

The resulting complex alumino-chloride anion, $[AlCl_4]^-$, then reacts with water:

$$2[AlCl_4]^- + 6H_2O \rightarrow 2Al(OH)_3 + 6H^+ + 8Cl^-.$$

Basically, the chemical reaction described between the aluminum and the chloride is one that allows chloride to be continuously released into the system. This chloride is free to react as long as water is present.

Since 100% screening of all product for moisture resistance is impractical, the approach preferred is to eliminate the chlorides, more specifically, the sources of the chlorides and/or the means by which they enter a plastic package. The areas of investigation that have proved most fruitful, and that have led to actual improvements

in package fabrication techniques and reliability, are assembly-area soldering, lead-frame design, and plastic molding processes.

## Elimination of Chlorides

### Assembly-Area Soldering

In an assembly process, due to the possible presence of heavily oxidized areas on lead surfaces, and to assure a good solder bond, the first step of the soldering process is often a preclean, in HCl solution, for example, followed by fluxing with a material that contains approximately 90,000 ppm of chloride; only a few ppm are needed to cause corrosion. Soldering is then done at a temperature of 275°C, which results in a thermal shock to the plastic and, depending on package design, the possible creation of conditions that will allow initial entrance of chloride into the package. In an analysis of some EMA resulting from reliability testing, chloride was detected by electron probe microanalysis on the internal portion of the leads in the cross-hatched regions shown in Fig. 5.

The first task in improving the soldering process was, then, to eliminate the chloride. Table 4 shows a typical manual solder process and the data from an experiment comparing no fluxing and no soldering to fluxing and soldering. Units were exposed to very high humidity (98%) and very high temperature (93°C); moisture condensation can occur on the devices at these humidity-temperature conditions. When there was no soldering and no flux, no EMA was found. Where there was precleaning with HCl and/or a halide flux, there was EMA. With no preclean and a flux that had no chloride in it, no evidence of EMA was found. The latter method is now in use at RCA.

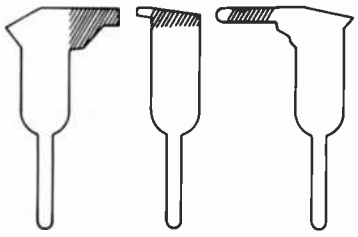

**Fig. 5**—Electron-probe microanalysis of integrated-circuit corrosion failures; areas indicating presence of chloride are highlighted.

Table 4—Results of Fluxing/Soldering Study

*Manual Solder Dip Process*

| | |
|---|---|
| 1. HCl Etch | 1:1 HCl/$H_2O$ at 50°C, 4 Minutes |
| 2. Cascade Rinse | $H_2O$ |
| 3. Fluxing | Halide Flux, 5 Seconds |
| 4. Solder Dip | 275°C, 5 Seconds |
| 5. Rinse | $H_2O$ 40°C, 2 Minutes |
| 6. Cascade Rinse | Cold $H_2O$, 2 Minutes, 3× |
| 7. Alcohol Bath | 1 Minute |
| 8. Air Dry | 40°C, 10 Minutes |

*Flux Solder Experiments*

A. Manual Solder Dip (CMOS CD4011B)—Results After 264 Hours* at 93°C/98% RH/18 V

| No HCl/No Flux (Steps 4–8) | HCl/Flux (Steps 1–8) | No HCl/Flux (Steps 3–8) | HCl/No Flux (Steps 1, 2, 4–8) |
|---|---|---|---|
| 0/15 | 4/15 (EMA) | 2/15 (EMA) | 1/15 (EMA) |

B. Non-Halide Flux (CMOS CD4049UB)—Results After 168 Hours* at 93°C/98% RH/18 V

| No Solder/No Flux No HCl Preclean | HCl Preclean Halide Flux | Non-Halide Flux |
|---|---|---|
| 0/10 | 5/10 (EMA) | 0/10 |

* Test approximately 4.5× more accelerated than 85/85 THB.

## Lead-Frame Design

Although a new manufacturing solder process (no HCl preclean and a chloride-free flux) was established, there was no guarantee that soldering processes used by a customer would not introduce a source of chloride contamination. Therefore, the moisture penetration of the package had to be improved.

As mentioned above, during forming of the leads, a small separation occurs between the leads and the plastic (Fig. 6), because there is no strong chemical bond between the plastic and the lead frame, i.e., the bond is primarily mechanical. A method was needed to more effectively lock the plastic to the lead frame and minimize separation. The DIP package in Fig. 1 shows a lead frame that provides an effective mechanical lock. The epoxy in the hole mechanically locks the plastic so that there is less separation when the lead forming takes place. By eliminating the sources of chloride and then using the lead-lock frame, the plastic package was made more impervious to moisture and contaminants.

Running of the standard industry temperature-humidity-bias (THB) test (85°C, 85% relative humidity), shows that improvement in the moisture resistance due to the lead-lock construction results in increasing the point at which the EMA starts from 200 to 500

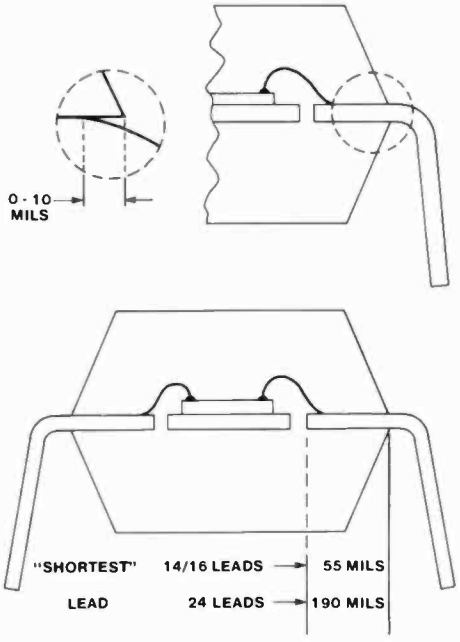


**Fig. 6**—Cross section showing separation between leads and plastic after leads are formed.

hours, as shown in Fig. 7. The contribution of the use of the lead-lock frame to improved package performance can then be determined as a part of the total reliability. This data is shown in Fig. 8, where cumulative results of temperature-humidity-bias tests comparing standard lead frames to lead-lock frames are given. All of these results were gathered under very accelerated test conditions.

## Plastic Molding Processes

An investigation was made of the plastic-package materials and molding processes.

With the objective of eliminating chlorides throughout the system, it is essential to choose a molding compound with as low a chloride content as possible. Table 5 shows the results of a study of a number of molding compounds, including several from domestic and Japanese suppliers.

There are many factors in the molding process besides molding compound that can affect a package's ultimate reliability, including

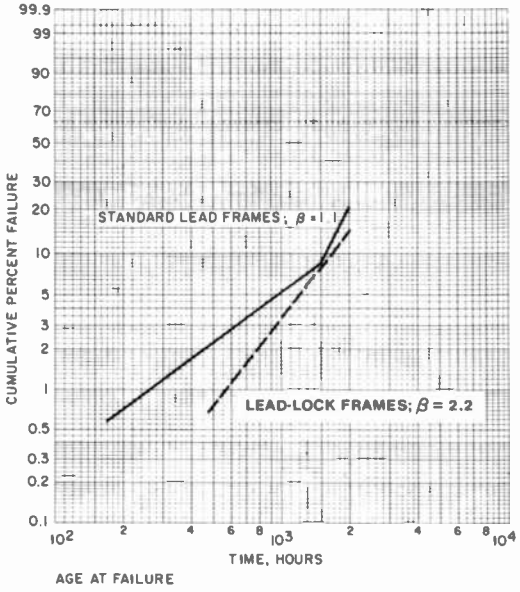


**Fig. 7**—Improvement in moisture resistance from using lead-lock frame. Data is for CMOS devices on THB of 85°C, 85% RH, 18 volts.

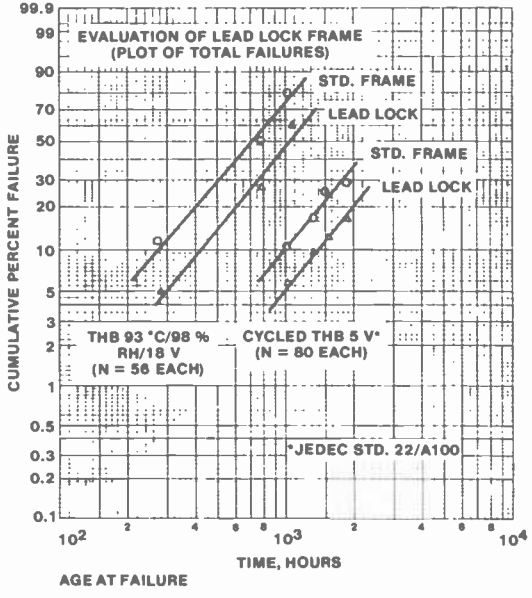


**Fig. 8**—Demonstration of improvement in temperature/humidity/bias test results for CMOS devices brought about by using lead-lock frames.

Table 5—CD4049UBE Molding Compound Study THB 85/85/18V

| | Domestic | | | Japanese | | | |
|---|---|---|---|---|---|---|---|
| Hours | A | B | C | A | B | C | D |
| 168 | 0/20 | 0/20 | 0/20 | 0/20 | 0/20 | 0/20 | 0/20 |
| 500 | 0 | 0 | 0 | 2 | 0 | 0 | 0 |
| 832 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1072 | 0 | 0 | 1 | 2 | 0 | 1 | 0 |
| 1572 | 0 | 2 | 0 | 0 | 1 | 2 | 0 |
| 2072 | 0 | 0 | 0 | 2 | 1 | 0 | 0 |
| 2572 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3072 | 0 | — | — | — | — | — | 0 |
| TOTALS | 0/20 | 2/20 (Open) | 1/20 (Open) | 7/20 (Open) | 3/20 (Open) | 3/20 (1 Open 2 Lkg.) | 0/20 |

transfer pressure and post-mold cure (discussed below). A relationship was found between these two variables during evaluation of the molding system. The effect of transfer pressure on the bias pressure-cooker (HAST) test was evaluated, and it was determined that, at a post-mold cure time of 16 hours, 1,000 psi transfer pressure provided improved moisture resistance over a pressure of 780 psi. The use of a post-mold cure of 16 hours yielded a significant improvement over no cure at all pressures, but the key factor apparent from this experiment was that the transfer pressure has to be 1,000 psi (Fig. 9). Thus, as shown in Fig. 10, transfer pressure alone does not provide the improvement, but it does provide a significant improvement when coupled with the 16-hour cure.

When plastic-material suppliers recommend a post-mold cure schedule, they typically do so with optimization of the material properties in mind, and not necessarily the effect of the schedule on the reliability of the packaged IC. Therefore, the effect of post-mold cure on moisture resistance of the packaged IC was investigated. The typical industry cure time varies from 4 to 8 hours. Investigations were made using post-mold cure times ranging from 4 to 32 hours.

Pressure cooker tests were run on 5,500 devices. The number of failures are shown in Fig. 11, which shows control-chart limits. If the data points are outside these limits, there is a 95% probability that the response to the conditions is different. Based on this information, the post-mold cure time was changed from 6 to 16 hours. The 85°C, 85% RH THB test shows the same results as the pressure cooker tests, namely, that 16 hours post-mold cure yields better results than a 6-hour cure.

In another experiment, it was determined that while 16 hours

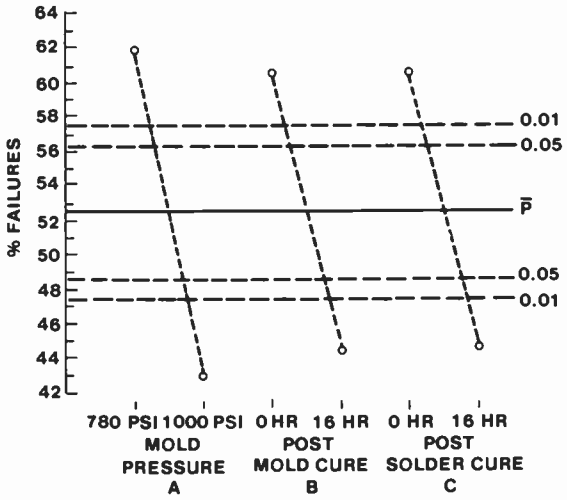


**Fig. 9**—Post-mold cure matrix for HAST test of CMOS devices at 145°C, 85% RH, 18 volts, 24 hours. Analysis of means main-effects chart for aperture mold.

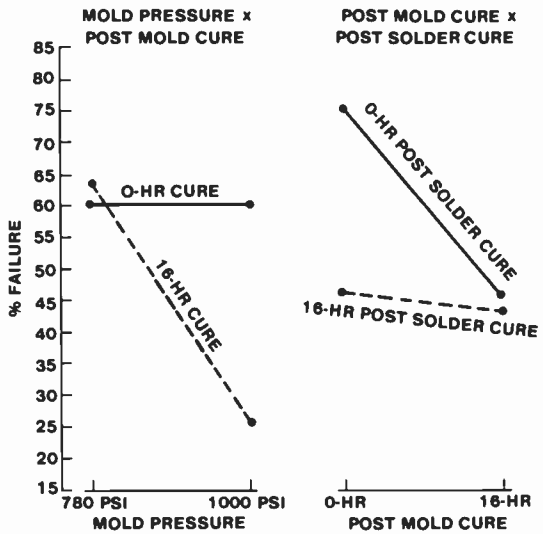


**Fig. 10**—Post-mold cure matrix for HAST test at 145°C, 85% RH, 18 volts, 24 hours. Significant two-factor interactions.

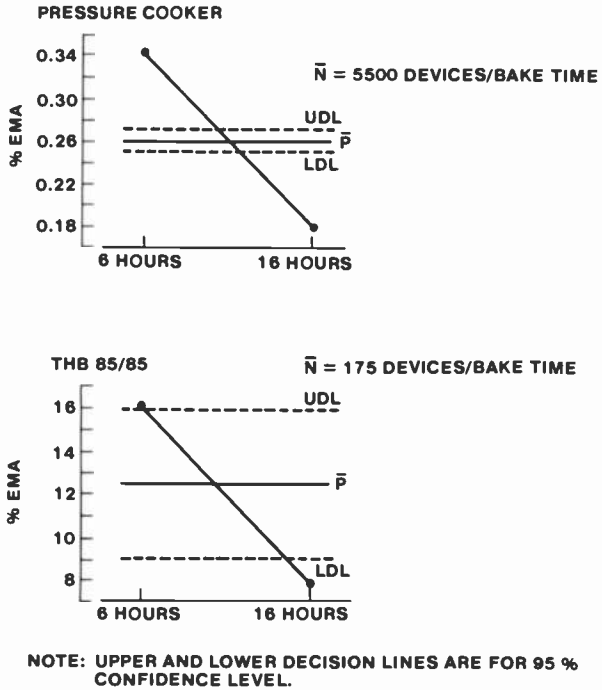


**Fig. 11**—Moisture-test results: 6-hour versus 16-hour post-mold bake at 175°C.

post-mold cure was significantly better than 0 hours, 32 hours was only slightly better than 16 hours (Fig. 12). The increment of improvement from 16 to 32 hours was not significant enough to justify the extra cost but, certainly, the extra cost for 16 hours over 0 or 6 hours is justified.

The reasons for improved reliability with increased cure time are not fully understood at this time. One theory postulates that the plastic may be more completely cured and is, perhaps, more stable, and another that the longer bake may neutralize a potential chemical reaction. It is recognized that all of the variables influencing post-mold cure must be studied together to identify any interactions, and that the significance of interactions can only be understood through sophisticated experimental design techniques followed by statistical analysis.

## Additional Evaluations and Experimental Results

In order to evaluate the many possible effects of a factory environ-

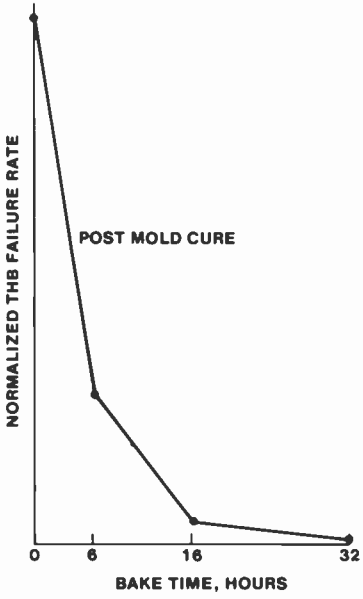


**Fig. 12**—Normalized THB capability as a function of 175°C post-mold bake time.

ment on plastic-package reliability, four different processes were set up in the manufacturing facility (Table 6). Product was assembled using these processes, and reliability tests were performed. When any process showed better, or worse, reliability results than another, the key variables could then be identified.

Table 7 shows the data from the 85°C, 85% RH THB testing. Line process 4 (available chlorides) show 14.5% failures, while processes 2 and 3 (no available chlorides) show 0% failures. Process 1, which was originally thought to be the best, did have some failures. One difference between this process and the other processes is that a pre-mold cleaning was performed. It is believed that this operation added some contaminants to the system. Since good engineering judgment would dictate the use of a preclean, the data provides an example of how not running the appropriate experiments in the actual factory environment can result in a wrong decision.

The latest CMOS silicon-gate technology, CMOSII (RCA's high-speed product QMOS),[5] was used to compare the two processes, chloride versus nonchloride (Table 8). There were 16% failures with the old chloride process compared to no failures on the new nonchloride process, a large improvement for the new process. The test used was

Table 6—Experimental Assembly Process Matrix

| | Process 1 | Process 2 | Process 3 (Standard) | Process 4 (Old Standard) |
|---|---|---|---|---|
| Pellet Inspect. | No Foreign Mat.<br>No Oxide Faults<br>No Discolored Bond Pads | Std | Std | Std |
| Pellet Mount. | Low Chloride | Low Chloride | Std | Std |
| Post Bond Inspect | No Rework | Real Time Process Control (RTPC) | RTPC | RTPC |
| Pre-Mold Clean | Freon TF | None | None | None |
| Molding Cmp. | Dom. Low $Cl^-$ | Dom. Low $Cl^-$ | Dom. Low $Cl^-$ | Domestic |
| Post-Mold Cure | 16 Hrs.@ 175°C | 16 Hrs. @ 175°C | 16 Hrs. @ 175°C | 6 Hrs. @ 175°C |
| Solder Dip Process: | | | | |
| | No HCl<br>Auto. Dip<br>Non-Halide Flux | No HCl<br>Auto. Dip<br>Non-Halide Flux | No HCl<br>Auto. Dip<br>Non-Halide Flux | HCl<br>Manual<br>Halide Flux |
| | No Rework | Rework (Non-Halide Flux) | Rework (Non-Halide Flux) | Rework (Halide Flux) |
| Auto-Brand | Std | Std | Std | Std |
| Final Test | Std | Std | Std | Std |

Table 7—Experimental Assembly Process Matrix—THB Data Base (85°C/85% RH/18V)

| Type | Data Code | Hours | Line 1 | | Line 2 | Line 3 | Former Std. Line 4 | |
|---|---|---|---|---|---|---|---|---|
| CD4049BE | 8314 | 1000 | 0/20 | | 0/20 | 0/20 | 8/20 | (7 EMA) |
| CD4059BE | 8314 | 1000 | 0/20 | | 0/20 | 0/20 | 3/20 | (EMA) |
| CD4076BE | 8318 | 1000 | 0/20 | | 0/20 | 0/20 | 2/20 | (Lkg) |
| CD4011BE | 8323 | 1000 | 0/20 | | 0/20 | 0/20 | 2/20 | (EMA) |
| CD4053BE | 8323 | 1000 | 0/20 | | 0/20 | 0/20 | 3/20 | (1 Lkg/ 2EMA) |
| CD4024BE | 8327 | 1000 | 0/20 | | 0/20 | 0/20 | 5/20 | (EMA) |
| CD4502BE | 8327 | 1000 | 1/20 | (EMA) | 0/20 | 0/20 | 1/20 | (EMA) |
| CD4051BE | 8332 | 1000 | 2/20 | (1 EMA, 1 PAR) | 0/20 | 0/20 | 2/20 | (EMA) |
| CD4049UBE | 8336 | 1000 | 1/20 | (Lkg) | 0/18 | 0/20 | 0/20 | |
| CD4011BE | 8336 | 1000 | 1/20 | (Lkg) | 0/20 | 0/20 | 6/20 | (EMA) |
| CD4011BE | 8340 | 1000 | 0/20 | | 0/20 | 0/20 | 0/20 | |
| | | | 5/220 (2.3%) | | 0/218 (0.0%) | 0/220 (0.0%) | 32/220 (14.5%) | |

Table 8—QMOS Chloride versus Nonchloride Assembly Process—THB Results for EMA

| Test | Hours | Chloride Process | Non-Chloride Process | Magnitude Improvement |
|---|---|---|---|---|
| THB 85°C/85%RH/6V | 1000 | 39/240 (16.3%) | 0/198 (0.0%) | >16× |
| Accelerated THB 93°C/98%RH/6V | 1000 | 119/180 (66.1%) | 8/160 (5.0%) | 13× |

the 85°C, 85% RH THB test. For the 93°C, 98% RH THB, the results were 66% and 5% for the old and new processes, respectively. With QMOS product, using the chloride-free soldering process, there are zero failures on the 85°C, 85% RH THB test, with one lot reaching 7000 hours without a failure (Table 9).

A 5,000-hour capability on 85°C, 85% RH THB qualifies that product to be used in some long-term (greater than 10 years) applications where hermetic product is normally used. Many hermetically sealed devices would have a problem passing 7,000 hours of 85°C, 85% RH THB without the package coming apart. If a cerdip package were run in the same test for 7,000 hours, conductive shorts would form on the outside of the package due to the leaching out of lead ions from the glass. In the future, plastic packages will be used in more and more applications previously employing hermetic packages because the plastic-package technology is reducing the differences in the package capabilities.

In the program described in this paper, the major effort was to remove chlorides from the package and assembly system and improve the basic moisture resistance of the plastic package. However, all wafer fabrication operations were also reviewed with the goal of

Table 9—QMOS—1983 Assembly Process THB 85°C/85% RH/6V

| Type | Hours | Sample Size | Failures |
|---|---|---|---|
| HC/HCT00 | 7000 | 20 | 0 |
| HC74 | 1000 | 18 | 0 |
| HC/HCT238 | 1000 | 20 | 0 |
| HC/HCT138 | 1000 | 20 | 0 |
| HC242 | 1000 | 20 | 0 |
| HC/HCT175 | 1000 | 20 | 0 |
| HCT74 | 1000 | 20 | 0 |
| HC/HCT251 | 1000 | 20 | 0 |
| HC243 | 1000 | 20 | 0 |
| HC/HCT04 | 1000 | 20 | 0 |
| | | 198 | 0 |

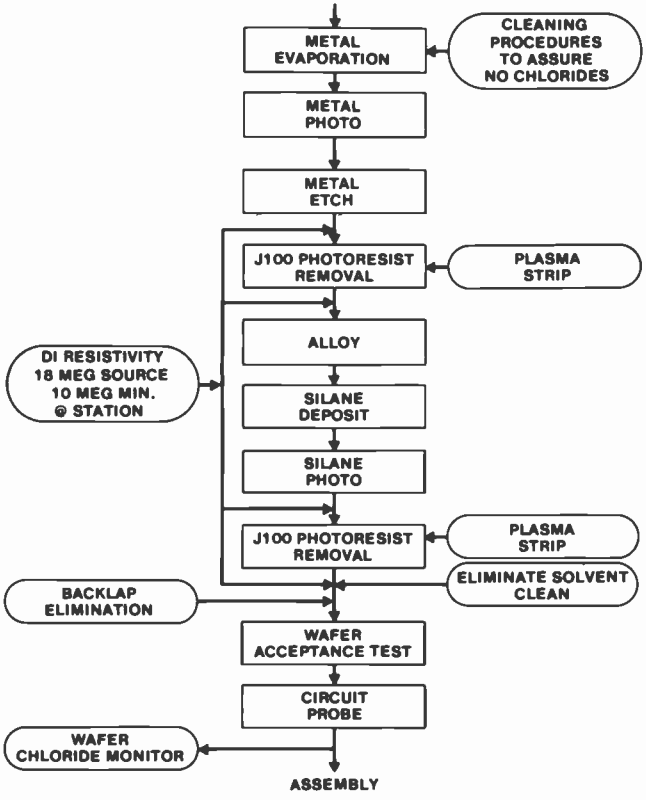


**Fig. 13**—Wafer fabrication process changes (oval boxes are changes).

eliminating chloride-bearing materials and processes. Figs. 13 and 14 show the wafer fabrication and assembly process steps (square boxes) and the changes made (rounded boxes). Based on the major parameters discussed in this paper, an improvement of over 25 times was realized (Fig. 15). This number is conservative; the actual improvement could be as high as 50 times.

Fig. 16 shows the improvements in plastic-packaged-CMOS moisture resistance over the last 10 years. The moisture resistance of plastic packages is measured by the 85°C, 85% RH THB test, the industry standard. In 1974, the plastic-packaged products were about 30% defective at 1,000 hours. Moreover, at that time, plastic was not used except in very benign applications. The impetus for improvement in 1974 was the first use of plastic-packaged devices in volume in automotive applications other than radio. The main reason for the improvement was the understanding and control of

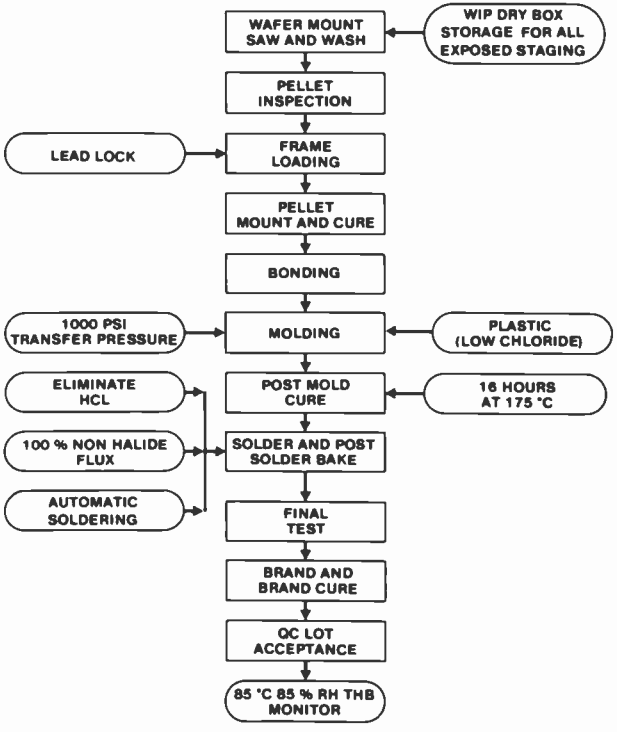


**Fig. 14**—Assembly process changes (oval boxes are changes).

phosphorous content in the CVD PSG protect layer. An even greater step-function improvement has been achieved in 1984 by the elimination of chloride from the plastic-package process.

## Failure Rates in Dry Ambients and Thermal Stress

Table 10 shows plastic-package failure rates for different technologies, and indicates the sample size, the actual test temperature, the voltage ratings, the equivalent device hours at 85°C, and the failure rates at various temperatures. For example, CMOS logic at 55°C has a very low failure rate (0.0008%/1000 hours) if moisture is not a factor. This finding is based upon high-temperature test data with no moisture.

There are also tests that quantify temperature-cycling capability (Table 11). The DIP, dual-in-line plastic package, has good temperature-cycling capability at −65°C to 150°C based on a sample of 17,000 devices (there were only two continuity failures). Thermal-

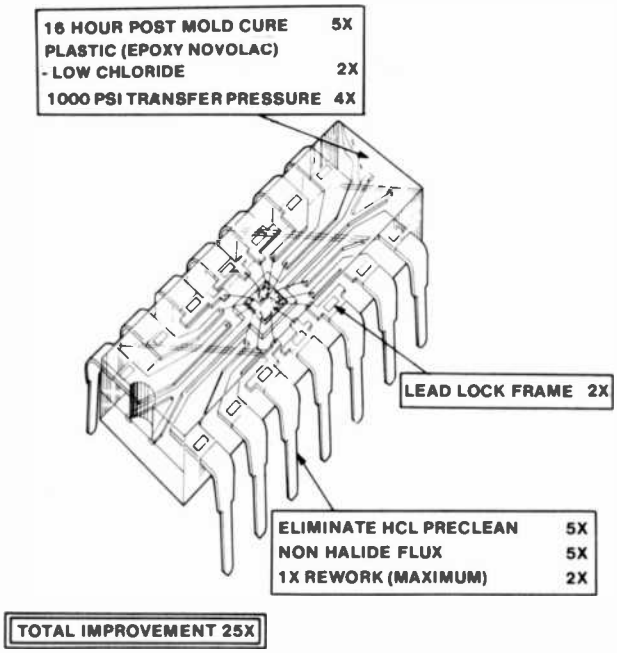


**Fig. 15**—RCA dual-in-line plastic-package improvement. The numbers show magnitude of improvement contributed by each of the major factors relative to reducing the occurrence of EMA.

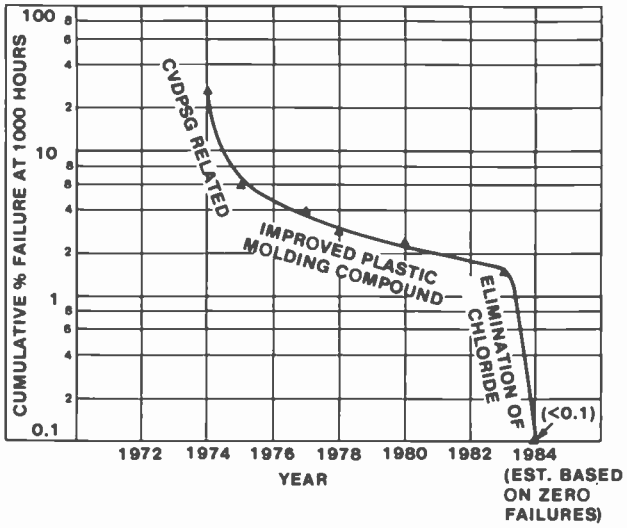


**Fig. 16**—Improvements over the past ten years in plastic-packaged-CMOS moisture resistance.

Table 10—Integrated Circuit Failure Rates Plastic Dual-In-Line Package

| Technology | Sample Size | Actual Test Temp | Voltage (Max Rated) | Equivalent[a] Device Hrs At 85°C | Failure Rate[a] %/1000 Hrs at 60% UCL | | |
|---|---|---|---|---|---|---|---|
| | | | | | 85°C | 70°C | 55°C |
| CMOS Logic | 1405 | 125°C–150°C | 18 | $9.7 \times 10^7$ | 0.015 | 0.0036 | 0.0008 |
| CMOSII (QMOS) | 2340 | 125°C–175°C | 6 | $2.7 \times 10^8$ | 0.003 | 0.0007 | 0.00015 |
| $C^2L$ LSI | 2985 | 125°C–175°C | 7 | $9.4 \times 10^7$ | 0.030 | 0.007 | 0.0015 |
| SOS LSI | 246 | 125°C–175°C | 7 | $2.1 \times 10^7$ | 0.020 | 0.005 | 0.0010 |
| CMOS I LSI | 1119 | 125°C–175°C | 6 | $9.1 \times 10^7$ | 0.034 | 0.008 | 0.0017 |
| CMOS II LSI | 279 | 125°C | 6 | $3.5 \times 10^6$ | 0.057 | 0.013 | 0.0029 |
| Bipolar | 8725 | 125°C[b] | 8–30 | $1.1 \times 10^8$ | 0.025 | 0.006 | 0.0013 |

[a] Extrapolated from actual test temperature, assuming a 1.0 eV activation energy.
[b] Dynamic life ambient test temperature is 85°C; device-hours based on an estimated average junction temperature of 125°C (calculated junction temperature of the range of types tested is between 100°C to 150°C).

shock data ( −65°C to 150°C, liquid-to-liquid) shows only one failure for continuity in 18,000 devices. Some of the small samples have gone to 9,000 cycles before the first failure occurred.

## Future Developments in Reliability Tests

Future programs include the study of new encapsulation materials, optimization of the molding parameters, investigation of chip protect layers, and consideration of some new metallization schemes. Every year, improvements are made in the reliability of plastic packages, not necessarily because of problems, but because of the increased demand for plastic products in ever more diversified applications. Accordingly, improvement programs will be continued while the present capability is monitored. Table 12 shows the volume of data collected in the monitoring of moisture resistance in the factory. These tests, which are pressure-cooker oriented, are now being replaced by 85°C, 85% RH THB testing in the factory.

Table 13 shows the different moisture-related reliability tests that are currently used to characterize plastic-packaged ICs. A correlation of each of these tests with the 85°C, 85% RH THB will be established. For example, Fig. 17 shows the correlation between the 85°C, 85% RH THB test, the 93°C, 98% RH THB test, and the cycled THB test. There is an approximately 5× difference in acceleration.

Table 11—Plastic Dual-In-Line Package (RAMP—1983)

| Technology | Cycles | Sample | Outside Specifications |
|---|---|---|---|
| | Temperature Cycle $T_A$ = −65°C to +150°C, Air-to-Air, Mil. Std, 883/1010.3 | | |
| CMOS Logic | 200 | 9,955 | 0 |
| | 1000 | 525 | 2 |
| | 1500 | 40 | 0 |
| | 3000 | 20 | 0 |
| Bipolar | 200 | 6,480 | 0 |
| | Total | 17,020 | 2 |
| | Thermal Shock $T_A$ = −65°C to +150°C, Liquid-to-Liquid, Mil. Std. 883/1011.2 | | |
| Technology | Cycles | Sample | Outside Specification |
| CMOS Logic | 200 | 11,411 | 0 |
| | 1000 | 415 | 0 |
| | 2000 | 160 | 0 |
| | 9000 | 60 | 1 |
| Bipolar | 200 | 6,580 | 0 |
| | Total | 18,626 | 1 |

The 85°C, 85% RH THB test is repeatable, but as product capability increases, the time needed to get results increases; hence, the need for a more accelerated test.

One increasingly popular test is the HAST (highly accelerated stress test),[9,10,11] which is a bias pressure-cooker test performed under nonsaturated conditions. HAST testing is becoming very pop-

Table 12—1983 Assembly Process Composite Summary of Moisture Test Data (Factory RVS and Pressure Cooker)

| Technology | Quantity Tested | Number EMA |
|---|---|---|
| | Malaysia Assembly | |
| CMOS | 33,582 | 1 |
| Bipolar | 64,990 | 2 |
| QMOS | 845 | |
| | Total 99,417 | 3 |
| | Taiwan Assembly | |
| Technology | Quantity Tested | Number EMA |
| LSI | 3,450 | 2 |
| CMOS | 7,640 | 0 |
| Bipolar | 39,406 | 4 |
| | Total 50,496 | 6 |

Note: RVS = Reliability Verification Sequence

Table 13—Moisture Test Matrix CMOS/Bipolar

| Test | Condition |
|---|---|
| 1. THB | 85°C/85% RH, $V_{DD}$ = Max. Rated |
| 2. THB Cycled | Same as (1), Except Cycled T On = 5 Minutes, T Off = 5 Minutes |
| 3. THB JEDEC 22A/100 | 98% RH, 30 – 60°C, $V_{DD}$ = 5V, Cycled T On = 5 Minutes, T Off = 5 Minutes |
| 4. HAST | 145°C/85% RH/$V_{DD}$ = Max. Rated |
| 5. Humidity Storage | 85°C/85% RH |
| 6. Humidity Storage | 50°C/85% RH |
| 7. Pressure Cooker | 15 PSIG, 121°C |
| 8. Pressure Cooker | 50 PSIG, 150°C |
| 9. RVS | Pressure Cooker (15 PSIG, 24 Hours) + Bias Life (85°C, Max. Voltage, 100 Hrs) |

ular, but the question of correlation to the 85°C, 85% RH THB test has not been settled. The failure-rate data indicates a correlation, but the results could be due to two different failure mechanisms. A physical analysis must always be done to prove that a correlation in mechanism exists.

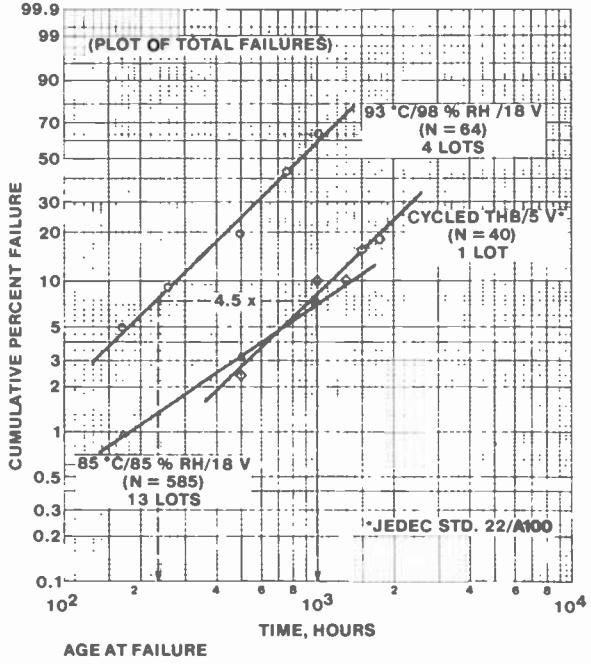


**Fig. 17**—A correlation, for CMOS devices, between the 85°C, 85% RH THB test, the 93°C, 98% RH THB test, and the cycled THB test.

Table 14—Development of One-Day THB Test (HAST[a] Method) to Correlate with 1000 Hours at 85°C/85% RH. Test to Be Used As a Real-Time Indicator in Factory Production

| Condition | MTF[b] (Hours) | Preliminary Estimate of Acceleration Over 85°C/85% RH/18V[c] |
|---|---|---|
| 155°C/85% RH/18V | 27 | 100 Times |
| 145°C/85% RH/18V | 50 | 55 Times |
| 135°C/85% RH/18V | 90 | 30 Times |

[a] Highly Accelerated Stress Test
[b] 50% failure point from Weibull plot of functional/continuity failures.
[c] Based on first approximation of the activation energy, which is 0.85 eV.

Based on the activation energy for the three points in Table 14 (which come from the Weibull plot in Fig. 18), the percent failure from one test-condition level to the next can be predicted. Physical analysis shows that the failure mechanisms are not identical, even though the data falls on a straight line. The purpose of establishing

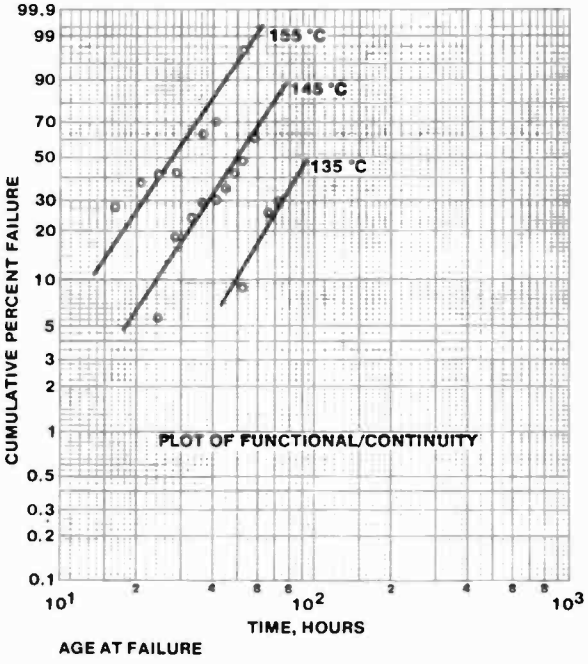


Fig. 18—Based on the activation energy and the data provided in this graph, the percent failure from one test condition level to the next can be predicted. Data is the result of HAST test: 85% RH, 18 volts, on CMOS devices.

an acceleration factor is to predict the mechanism occurring at some lower temperatures. However, in this case, as the temperature is decreased, more bond-pad failures occur (Fig. 19), and as the temperature is increased, more in-board failures occur (in-board means underneath the protect layer over the metal). Under the 85°C, 85% RH THB test, more bond-pad and less in-board failures occur. The HAST test results primarily in in-board failures, with a smaller percentage of the bond pads showing EMA. Changes in temperature cause the failure mechanisms to split; however, the failure mechanism is still evident. In either case, both bond-pad and in-board failures exist. They will be detected on either the HAST or the 85°C, 85% RH THB test, but the ratios of bond pads to in-board failures changes. A great deal of analysis has to be utilized with HAST testing.

In a recent evaluation of prediction techniques (Fig. 20), it was shown that the sum of temperature and humidity provides the acceleration factor over various temperature and humidity conditions.[12] When this data is plotted as log versus the sum of T and RH, it can be fitted to a straight line. Use of the straight line allows a prediction of what could happen under test conditions shown by the dotted line of Fig. 20. This model was originally proposed by Reich and Hakim[12] based on work done in the Panama Canal Zone

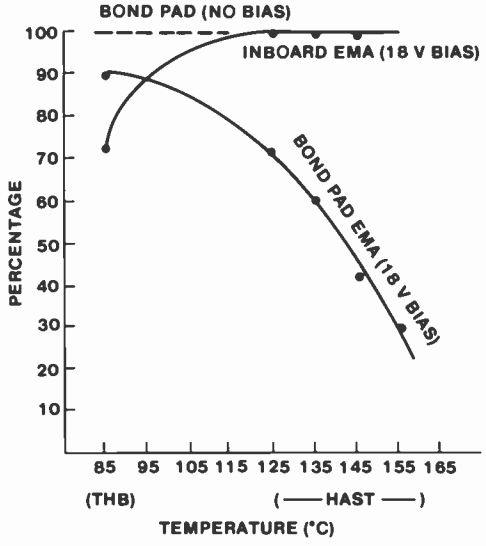


**Fig. 19**—Location of EMA as a function of temperature at 85% RH. Plot of percentage of bond pad versus inboard failures.

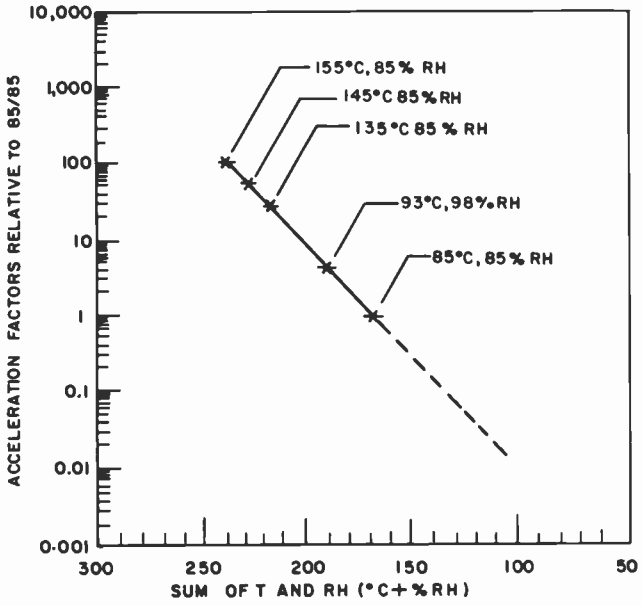


**Fig. 20**—Acceleration factors for CMOS devices relative to 85°C, 85% RH THB as a function of temperature and relative humidity.

(at 30°C, 90% RH). Lycoudes[3] later reported median life data from this model where, comparing results for the Panama Canal Zone conditions of 30°C, 90% RH (no contaminants in the environment) to results for 85°C, 85% RH, an acceleration factor of approximately 40 could be realized. Extrapolating the straight line of Fig. 20 to the 30°C, 90% RH conditions indicates a prediction of approximately a 30 times acceleration factor. This is not the ultimate in predicting reliability, but as techniques are improved with more reliability data, better predictions will be possible.

## Summary

The plastic package is the dominant form of packaging for integrated circuits in use today worldwide. It is mechanically stronger than its hermetic counterpart and more cost effective both in manufacturing and application.

Each year there is an improvement in the reliability of plastic-packaged ICs because of (1) the continuously increasing demand by the customer for plastic in more diverse, more hostile applications and (2) the introduction and use by the manufacturer of improved

materials, techniques, and processes. The information in this paper indicates the kind of reliability improvement that can be achieved with identification of proper models, thorough engineering programs, and statistical experimentation, and will provide the basis for the transition to the next level of plastic-package reliability.

## Acknowledgments

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# Moisture Control in Hermetic Leadless Chip Carriers With Silver-Epoxy Die-Attach Adhesive

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**Abstract**—This paper describes package design and process changes in the development of an improved system for controlling internal water-vapor levels below 5000 ppmv in hermetically-sealed leadless chip carriers with silver-epoxy attached silicon devices. It was shown by mass spectrometry that the silver-epoxy die-attach material releases water and unreacted monomers at about 300°C. Therefore, the high-temperature braze-seal design and process originally used in manufacturing was changed to a controlled-environment low-temperature seam-welded design. A high-temperature, pre-seal, furnace bake-out and epoxy cure process was also incorporated. Moisture levels measured for the new package and process are below the 1000 ppmv level.

## Introduction

High moisture levels were detected in the fabrication of devices for a critical high-reliability program. The product, CMOS/SOS devices, were assembled in leadless chip carriers (LCC) and die attached using DuPont 6838 silver-filled epoxy adhesive. A number of engineering tests and experiments were made, but only those results considered most significant are reported here.

Initial production of four universal gate arrays (UGAs) and one random-access memory (RAM), all of which contain CMOS/SOS de-

vices assembled in leadless chip carriers (LCC), commenced in the fourth quarter of 1980. The LCC packages were designed for braze seal using a nickel- and gold-plated Kovar lid with a Au/Sn brazing preform tack welded to the lid at each of the four corners. The assembled package and lid are pre-aligned in a jig and clamped together with spring tension clips. The clipped assembly is placed on a conveyor belt and passes through the furnace in a nitrogen atmosphere containing 20 ppmv (parts per million by volume) moisture at a maximum temperature of 310°–315°C (Fig. 1).

Initial water-vapor measurements on three production lots sealed from December 1980 to November 1981 ranged from 460 to 2250 ppmv. A 5000-ppmv moisture level is the allowable maximum for qualification to Mil-Std-883, Test Method 1018.2, Procedure 1.[2] These results were satisfactory and qualified production; however moisture measurements made on engineering tests processed during the March and April 1982 period of time ranged from 5000 ppmv to 15000 ppmv. Further moisture measurements made on the

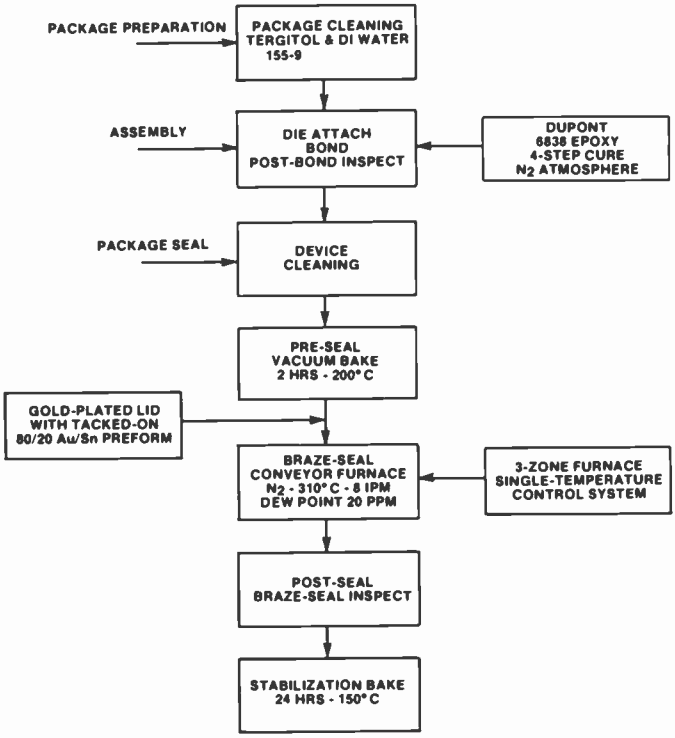


**Fig. 1**—Flow chart for braze-seal process with pre-seal vacuum bake.

product, after the production line was carefully checked and controlled, indicated some product with internal moisture levels greater than 5000 ppmv. Fig. 2 indicates the moisture level distribution of product made during this time. An engineering investigation into the cause of these inconsistencies was initiated.

## Analysis and Testing

One of the first series of tests run compared moisture levels for empty packages and packages containing the silver-epoxy die-attached devices (Table 1). The mass spectrometer results indicated a significant increase in $CO_2$ for the packages containing the silver-epoxy attached CMOS/SOS devices. The moisture levels, however, showed no significant differences. Hydrogen, which is generally present in hermetic packages due to the nickel- or gold-plating processes,[3] was significantly lower for the package containing the silver-epoxy attached devices.

It was clear therefore that the organic silver-epoxy die-attach material had an influence on the gases contained in the leadless chip carrier hermetic package. It was also evident that at the high temperature required to braze seal, additional degassing or moisture release could occur (Fig. 3).

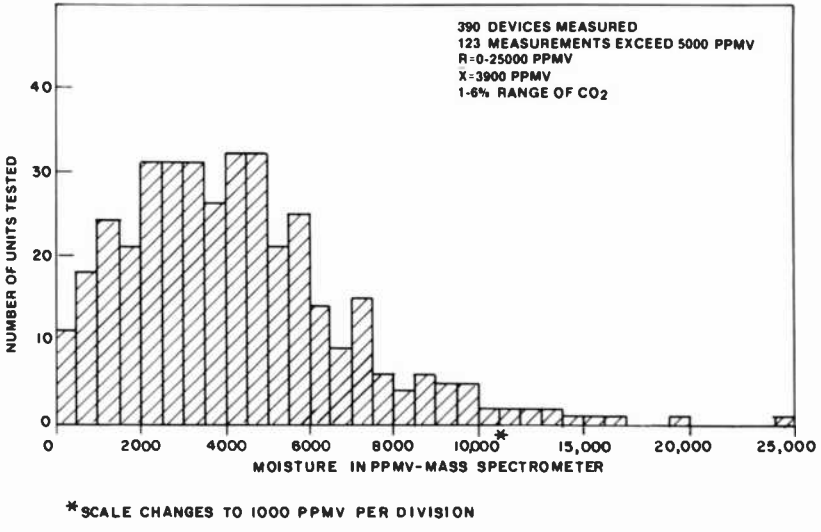


**Fig. 2**—Moisture-level distribution in early samples of devices made using braze-seal process.

Table 1—IC Package Ambient Analysis (MIL STD 883, Method 1018, Proc. 1): Empty Packages Versus Packages Containing Silver-Epoxy Attached Devices

| | Empty Packages | Packages with Standard Devices |
|---|---|---|
| 64-Pin Leadless | | |
| Moisture – ppmv | 300 – 1100 | 100 – 1700 |
| Hydrogen – ppmv | 2000 – 4500 | 300 – 800 |
| $CO_2$ – ppmv | 30 – 200 | 4000 – 7000 |
| 24-Pin Leadless | | |
| Moisture – ppmv | 400 – 2700 | 200 – 2000 |
| Hydrogen – ppmv | 100 – 3000 | 300 – 900 |
| $CO_2$ – ppmv | 200 – 300 | 3000 – 14,000 |

## Die-Attach Silver-Epoxy Mass Spectrometry Analysis[4]

A sample of cured silver-epoxy die-attach material was inserted into a mass spectrometer ion source by means of a pyrolytic probe, and the mass spectrometer was scanned from 10 to 600 a.m.u. once a second. The sample was heated at 200°C per minute to 1100°C. In this manner, identification of the evolved gases was made as the sample was heated. Two distinct regions were observed (Fig. 3). At about 300°C, unreacted monomers of the epoxy (epichlorohydrin and bisphenol A) were evolved, along with degradation products from these species, in particular water (Fig. 3). These data indicate that one source of moisture can come from the silver-epoxy die-attach material. It suggests that at the braze-seal temperature of 310°–315°C, the water released from the silver epoxy could be captured within the package cavity as the braze seal is made, resulting in packages with greater than 5000 ppmv moisture levels.[5]

## Pre-Seal High-Temperature Bake-Out and Epoxy Cure

A pre-seal furnace bake-out and epoxy cure step through the braze-seal furnace at 330°C was tested. This pre-seal high-temperature process was considered advantageous, since it would compensate for any insufficiencies in the pre-seal bake, would ensure the elimination of absorbed and condensed moisture from the package components, and would further out-gas the epoxy die-attach material and release some of the unreacted chemicals and water shown to be present by the mass spectrometry analysis (Fig. 3). This process could also be easily implemented in production.

Although a significant improvement in the distribution of moisture vapor content was made, this process did not consistently produce product below the 5000 ppmv of moisture required (Fig. 4).

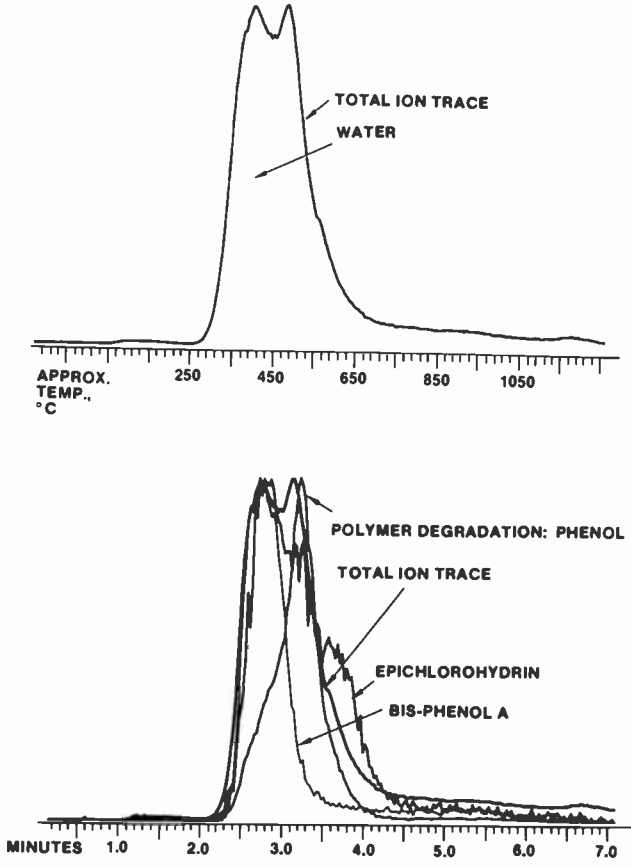


**Fig. 3**—Mass spectrometry analysis of silver epoxy versus temperature.

## Si/Au/Sn Preform for Moisure Control

The incorporation of an Si/Au/Sn alloy in a hermetic package was reported to reduce the high levels of moisture.[6] Preliminary tests were conducted by dropping a 0.35% Si/Au/Sn preform (0.070 × 0.070 × 0.001 inch) in the package with a silver-epoxy mounted chip and braze sealing with no other precautions taken to reduce moisture. The mass spectrometer moisture analysis results are shown in Table 2. For these tests, the moisture level for the control units measured 13,000 to 16,000 ppmv of moisture; the test packages containing the 0.35% Si/Au/Sn preforms measured only 125 to 135 ppmv moisture. Also, the hydrogen content of the packages containing the Si/Au/Sn increased to 5000–8000 ppmv, compared

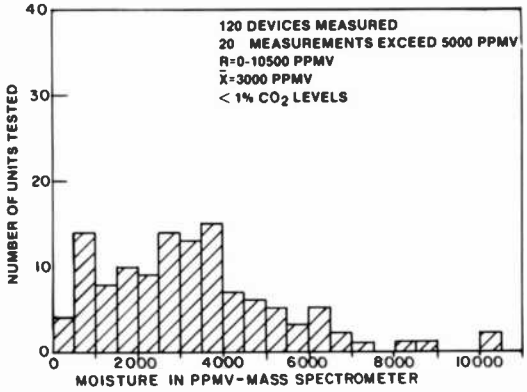


**Fig. 4**—Moisture-level distribution in sample of devices made using braze-seal process with pre-seal furnace bake.

to the control packages with 1700–1900 ppmv hydrogen. These results confirm the proposed mechanism of the reaction of the Si in the preform during the heat cycle,[6]

$$Si + 2\ H_2O = SiO_2 + 2\ H_2.$$

The use of a Si/Au/Sn preform inside a package with an epoxy-mounted die provided the silicon needed in the above reaction to produce a very dry package. Unfortunately, the method of placing the Si/Au/Sn preform inside the package and control of the related processing were not compatible with production processes.

Neither the Si/Au/Sn preform nor a Si/Au preform could be used as a die attach, since the device substrate is sapphire. All of the Si/Au/Sn experiments involved CMOS/SOS die and silver epoxy for die attach. The development of a process using the Si/Au/Sn approach to control moisture is considered possible. However, the results of the next series of experiments proved more satisfactory from a cost and implementation point of view, and work on the Si/Au/Sn preform approach was discontinued.

**Table 2**—IC Package Ambient Analysis (MIL STD 883, Method 1018, Proc. 1): Control IC Package Versus Package with Si/Au/Sn Preform Insert

| | Control | Si/Au/Sn Preforms |
|---|---|---|
| Moisture – ppmv | 13,000 – 16,000 | 125 – 135 |
| Hydrogen – ppmv | 1,700 – 1,900 | 5,000 – 8,000 |
| $CO_2$ – ppmv | 18,000 – 22,000 | 19,000 – 25,000 |

## Seam-Weld Seal

A modification of the braze-sealed package is required for seam welding. The top layer of ceramic is reduced in thickness to allow the weld ring to be brazed on top of it (Figs. 5 and 6). The gold plating is removed from the lid and the lid thickness is reduced to insure seam welding quality. The seam-weld sealing is controlled under dry-box conditions of less than 20 ppmv moisture and sealed at room temperature. Initial engineering weld-seal tests on 48-pin

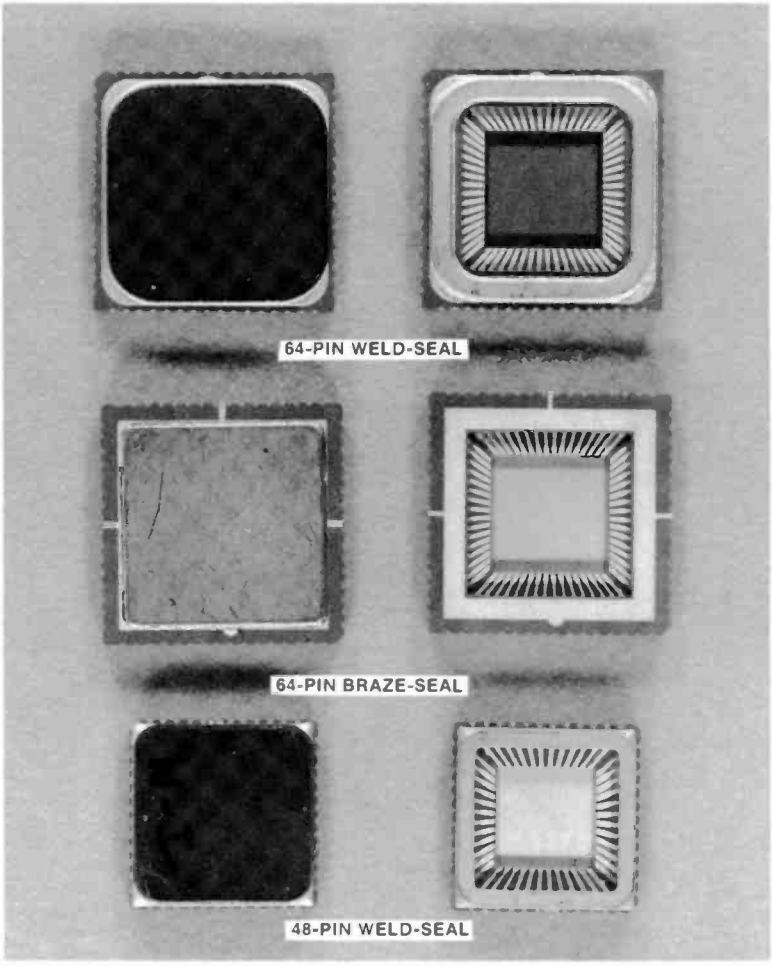


**Fig. 5**—Weld-seal and braze seal packages with and without lid attached. The 64-pin packages measure 0.720 inch square and the 48-pin package 0.560 inch square.

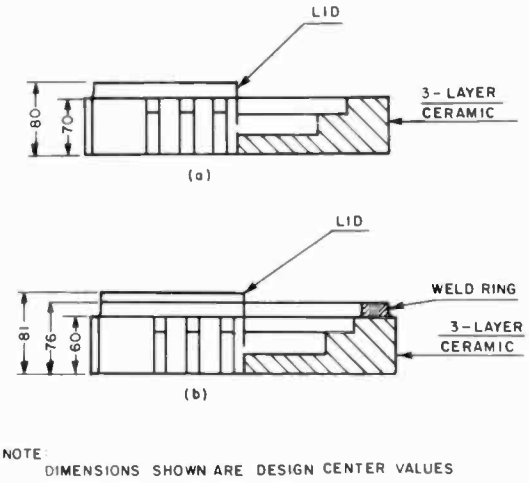


**Fig. 6**—Schematic of sections through braze-seal and weld-seal packages.

packages with silver-epoxy die attached measured between 0–410 ppmv for moisture.

The first series of tests with 24-pin and 64-pin weld-seal leadless packages compared the weld-seal process and pre-seal furnace bake with the braze-seal process and pre-seal furnace bake (Figs. 7 and 8). Moisture level analysis results are compared in Table 3 for the 64-pin leadless carriers. The results indicated a significant (10–20 times) reduction in moisture levels for the weld-seal ICs. Moisture levels of 100–300 ppmv for seam-welded ICs were measured versus 1700–2200 ppmv for the braze-seal product.

Based on these results, production was re-started with weld-seal packages. A total of 109 seam-welded IC's were measured for moisture (Fig. 9); 90% of the product was below 300 ppmv and 63% of the product was below 100 ppmv moisture, a significant and dramatic improvement over the pre-seal-bake braze-seal process (which as shown in Fig. 4, had approximately 16% of the product above the 5000 ppmv moisture levels).

## Seam-Weld Seals—Internal Moisture Analysis at High-Temperature Stress Conditions

A series of experiments were conducted for the seam-welded ICs to test changes in the ambient gases under temperature stress.

The first series of tests were to qualify the process, and tests were

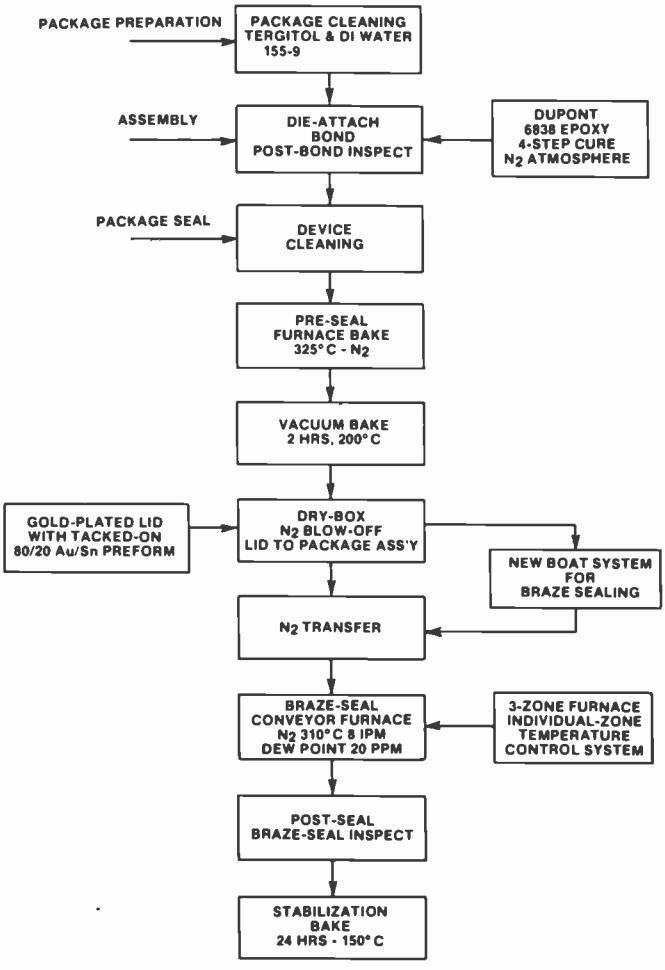


**Fig. 7**—Flow chart for braze-seal process with pre-seal furnace bake.

conducted at the highest temperature the devices would be subjected to in the application. Ten cycles from 25°C to 200°C were used to simulate the solder board-mounting process. The 64-pin seam-welded packages containing silver-epoxy attached CMOS/SOS devices (pre-seal furnace baked at 330°C) were analyzed for internal gases before and after the ten-cycle temperature stress (Table 3). Moisture levels of 100–300 ppmv were obtained before temperature stress and levels of 100–385 ppmv were measured after stress, indicating a stable system under this type of stress.

A series of tests were next conducted with 125°C, 230°C, and

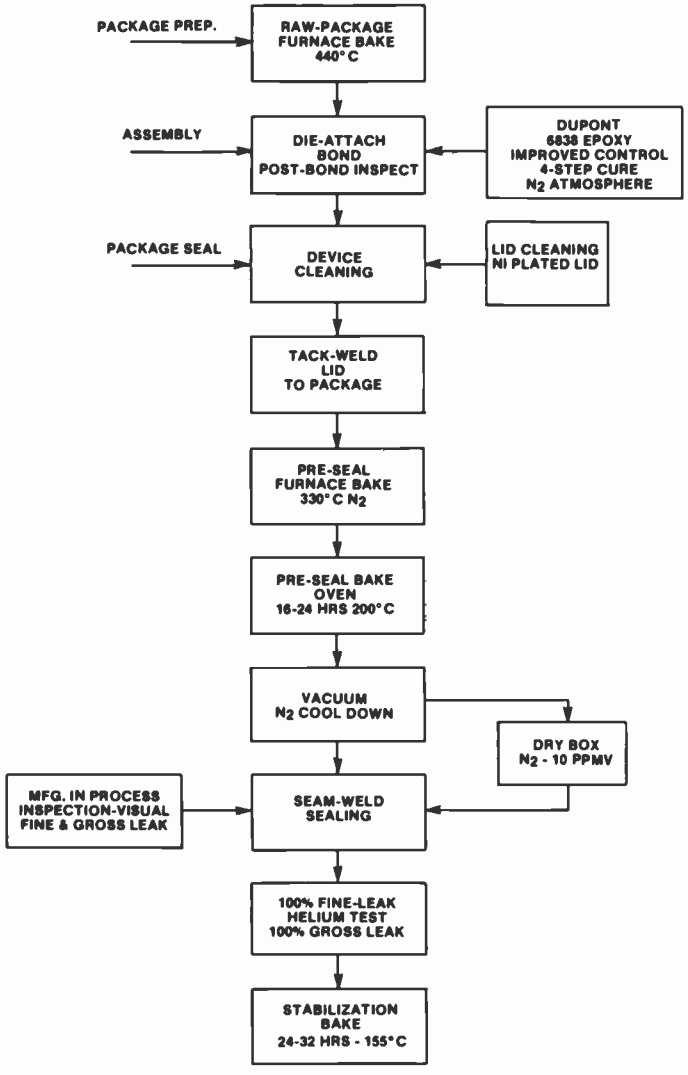


**Fig. 8**—Flow chart for weld-seal process with pre-seal furnace bake.

313°C post-seal bakes for these 64-pin leadless seam-weld ICs (Table 4). Moisture analysis was also made for seam-weld ICs before and after 125°C, 11 V, 240 hour burn-in.

Mass spectrometer results indicated that at temperatures above 200°C, significant changes in the ambient gases resulted (Table 4). Moisture increases from 70–80 ppmv moisture at 125° to 5000–9000 ppmv moisture at 313°C were observed. However no changes

Table 3—Moisture Level Tests for 64-Pin Packages: Weld-Seal Control Group, Braze-Seal Control Group, and Weld-Seal Group Subjected to Ten-Cycle Heat Stress Test*

| | | | | | |
|---|---|---|---|---|---|
| *Weld-Seal Control Group* | | | | | |
| Part Identification | H1 | H2 | H3 | H4 | H5 |
| Moisture – ppmv | 300 | 263 | 129 | <100 | 171 |
| Hydrogen – ppmv | ND† | ND | ND | ND | ND |
| $CO_2$ – ppmv | 1652 | 1609 | 1947 | 1972 | 1594 |
| *Braze-Seal Control Group* | | | | | |
| Part Identification | J1 | J2 | J3 | J4 | J5 |
| Moisture – ppmv | 2024 | 1738 | 1862 | 2163 | 1887 |
| Hydrogen – ppmv | 1.17 | 0.209 | 0.532 | 0.426 | 0.565 |
| $CO_2$ – ppmv | 3418 | 5784 | 8325 | 6755 | 6689 |
| *Weld-Seal After Ten-Cycle Heat Stress Test* | | | | | |
| Part Identification | E1 | E2 | E3 | E4 | E5 |
| Moisture – ppmv | <100 | 133 | 203 | 385 | 356 |
| Hydrogen – ppmv | ND | ND | ND | ND | ND |
| $CO_2$ – ppmv | 2332 | 2512 | 3353 | 3546 | 4572 |

* Data reported by Oneida Research Services, Inc. IC package Ambient analysis (per MIL-STD 883, Method 1018, Procedure 1).
† ND = none detected.

in internal moisture levels were observed for the 125°C temperature stresses after 240 hours.

## Discussion

It is shown that at approximately 300°C (Fig. 3), the silver-epoxy die-attach material chemically reacts, or decomposes, releasing water as a by-product of the reaction. It is this reaction and water release that makes it difficult to consistently obtain internal moisture levels of less than 5000 ppmv for the high-temperature braze-seal leadless chip carrier. The addition of the pre-seal high-temperature degassing, desorption, and cure bake process had an advantageous effect on moisture control (Fig. 4), although levels below 5000 ppmv were not consistently maintained.

The seam-weld sealing process yielded product with internal

Table 4—Moisture Analysis of Post-Seal Temperature Stressing 64-Pin Leadless Seam-Weld Seal

| | Moisture Level (ppmv) |
|---|---|
| 120°C – 16 Hours | 70 – 80 |
| 230°C – 3 Hours | 800 – 1,600 |
| 313°C – Furnace Bake – 3 Min. | 5,000 – 9,000 |

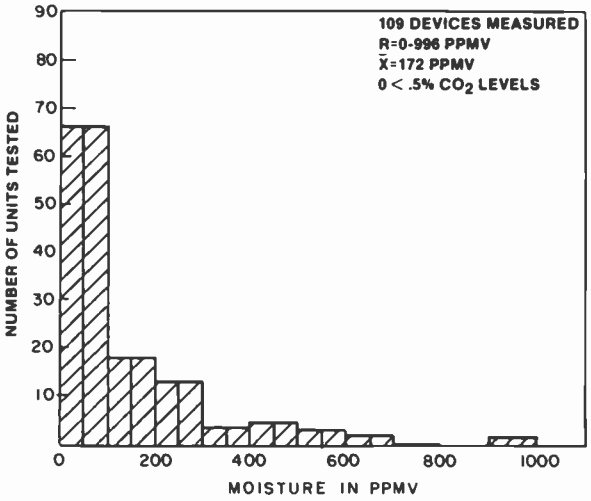


**Fig. 9**—Moisture-level distribution in sample of devices made using weld-seal process with pre-seal furnace bake.

moisture readings consistently below 1000 ppmv, and typically at 200 ppmv (Fig. 9). Weld-sealed silver-epoxy attached ICs, when subjected to post-seal temperatures above 200°C, show significant changes in the ambient gases, and increases in moisture content in the package.

## Conclusion

Internal moisture levels for silver-epoxy attached devices hermetically packaged in ceramic leadless chip carriers can be successfully controlled with the incorporation of (1) a high temperature 330°C pre-seal bake and (2) the conversion from a high-temperature braze-seal technique to a low-temperature seam-weld seal. These devices, when burned-in for 240 hours at 125°C, show no internal changes in moisture levels.

## Acknowledgments

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# Electrostatic Discharge: Mechanisms, Protection Techniques, and Effects on Integrated Circuit Reliability

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**Abstract**—Electrostatic discharge (ESD) was once considered a problem only for unprotected, insulated-gate field-effect transistors, but the ever shrinking geometries of all semiconductor devices have made them vulnerable to this phenomenon. ESD models and on-chip device protection techniques are reviewed, together with current evidence concerning latent defects and their effect on device reliability. A brief discussion on the importance of ESD controls in the assembly environment is also included, with an emphasis on realistic cost-effective measures. Finally, the impact of continued scaling on ESD vulnerability and protection structure limitations, are examined.

## Introduction

In 1982, it is estimated that the U.S. electronic industry scrapped over $5 billion worth of circuit boards.[1] Many believe that ESD was responsible for a large portion of this total, as their own in-house results show that static damage can account for 10 to 100% of the failures, depending on the device technology.[2] Much of the damage due to ESD occurs during device or equipment manufacture, and may go undetected by the operator if it is below the 3-kV threshold of feeling. However, many semiconductors can be damaged by discharges of 200 V or less,[3] and this level continually decreases as device geometries shrink.

Fortunately, most of the damaged devices are caught during testing, and the cost of yield loss, repair, or replacement, although not insignificant, is minimal. However, there is a growing body of evidence[4,5] that latent ESD-induced defects in devices are real. In

these devices the semiconductor structure has been damaged, but not sufficiently to cause an immediate malfunction. The device, board, or system passes testing and may even pass a limited burn-in, but it fails later. Also, there are devices that have been damaged by ESD and weakened; they continue to work well, until a small system electrical overstress (EOS) occurs. It may not be large enough to damage a normal device, but it is adequate to destroy the weakened unit.[23]

ESD handling precautions are absolutely essential at each stage of the manufacturing process and can go a long way towards reducing the number of defects and latent failures, but EOS in the equipment is still a hazard. Protecting against this problem can require extensive evaluation time and additional components, which add to the cost of the equipment and may even delay its introduction as a product, thus reducing the potential profit margins.

Although ESD is normally considered an MOS problem, shrinking geometries have made bipolar integrated circuits, long considered immune to ESD, almost as sensitive as unprotected MOS devices in some circuit configurations.

## ESD Models

### The Human-Body Model

The human ESD event begins with an individual acquiring an electrostatic charge through some mechanism, such as triboelectric charging or by contacting another charged object, such as a TV or VDU screen. If the charged person now moves toward an uncharged object, such as the pin of an IC, an ESD event occurs when the local electric field exceeds the dielectric strength of the air. A rapid discharge takes place, and inadequately protected devices can be destroyed.

The simplest human-body ESD circuit model is a series *LCR* circuit. The inductance is normally neglected in most models, but it does exist in all practical circuits, including the human individual, and has a limiting affect on the waveform risetime. The most commonly used *RC* components are 1.5 kilohm and 100 pF, which represent a standing individual with the discharge directly from the skin. In an assembly environment, the individual will frequently be seated close to a grounded work station holding a pointed metal object (which may be a component). Under these conditions, the capacitance can increase to 200–250 pF, and the resistance reduces to 500–300 ohms. The inductance remains virtually unchanged at

50–100 nH. The net effect is to increase the energy and the peak current seen by the component. Also, in practice, the human ESD event is not a single discharge, but a series of multiple discharges of successively lower voltages.[6] Multiple discharges occur because while the simple human-body model represents the surface capacitance and skin resistance, the real body has an additional bulk capacitance that is coupled to the skin capacitance via a high value resistance. In their paper, Hyatt, Calvin, and Mellberg suggest values of 100 kilohm and 650–1000 pF for these components. If the hand approaches the component slowly, the surface capacitor discharges rapidly through the skin resistance, and the arc is extinguished. The surface capacitor is then free to be recharged by the bulk capacitor through the high-value resistor. When the charge on the surface capacitor reaches sufficient voltage, the air is ionized and another discharge occurs. This process is repeated until the finger touches the component and the bulk capacitor is discharged.

Obviously, the full human-body model would be very difficult to duplicate in practice, and most specifications, such as MIL STD 883/38510 and DOD STD 1686, call for the surface *RC* components only and specify a maximum allowed rise time of 20 ns. It is unfortunate that no minimum rise time is specified, since some recent work at RCA[7] has shown that faster rise times, on the order of two to three nanoseconds, can result in a much lower failure threshold for some MOS protection networks.

## The Charged-Device Model

Speakman[8] has pointed out that the human-body model is not the only one of concern to semiconductor users; another is the charged device model. Further details of this potentially damaging ESD model are given in a paper by Bossard et al.[9] Basically, a device acquires a charge on its surfaces. This charge can be immobile, i.e., on the nonconductive parts, or it can be mobile, i.e., on conductive parts such as the lead frame. If one or more of the device pins now contacts a conductive surface, a very rapid, high-current, fast-rise-time discharge occurs that can degrade or damage dielectrics and junctions. To minimize potential damage from this cause, the charge on the device must be kept low, often to less than 100 volts. Unger et al,[10] and others, believe that this will be the major cause of future, ESD-related failures.

## The Field-Induced Model

Huntsman et al[11] have shown that a damaging potential can be

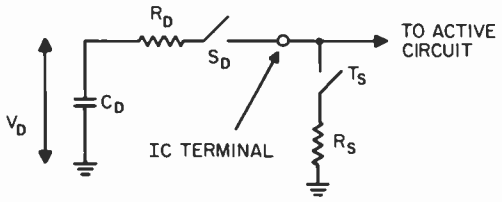


**Fig. 1**—Basic transient protection concept.

imposed on an ESD-sensitive, high-impedance device, such as a MOSFET, by bringing a highly-charged object into close proximity. Touching is unnecessary, as the induced voltage is a function of the capacitance division ratio between the device gate structure and the source-to-ground impedance. For devices to be damaged due to field induction, the charges have to be high and the device very sensitive. However, damage from this cause has been shown to exist and should not be ignored.

## Integrated Circuit Device Protection

### Basic Concepts

The basic concept of transient protection at the device pin is illustrated in Fig. 1. The discharge model consists of $C_D$, $R_D$, and $S_D$, and the protection structure of $T_S$ and $R_S$. When the switch $S_D$ closes, applying a transient to the IC terminal, $T_S$ must sense that transient and close, diverting the discharge current through $R_S$. If $R_S$ is zero, there is effectively no transient voltage at the IC terminal, and the active circuit is protected. As $R_S$ is increased, a transient voltage appears at the IC terminal and, at some critical level, the active circuit, or $R_S$, is damaged by the transient. $T_S$ can be bipolar, that is, capable of responding to positive and negative transients, or two unipolar devices can be used in parallel as shown in Fig. 2. If this method is used, the transient protection structure must protect the opposite polarity device as well as the active circuit against avalanche breakdown. Consequently, the avalanche voltage must be greater than the peak transient current multiplied by the 'on' resistance of the protecting structure.

Another problem that must be addressed is the time taken by the protection structure to turn on and reach its full low-impedance state. This can vary from about 1 ns for a forward biased, or zener, diode to 4 ns or longer for more complicated structures. During this time, the transient continues to rise, and can impose significant

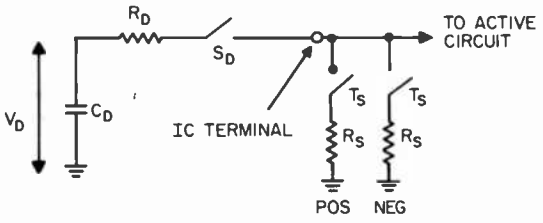


**Fig. 2**—Basic bipolar transient protection circuit.

voltages, albeit for a short time, on the active circuit. It is, therefore, essential that some additional filtering of the transient be used between the bond pad and the active circuit, particularly for MOS devices. Fig. 3 illustrates this arrangement.

Before deciding on a particular protection structure, it is necessary to evaluate the various stress levels to which the device will be subjected throughout its expected life. Some devices will only be required to survive ESD handling, whereas others may be expected to survive many EOS pulses without degradation. Wunsch and Bell[12] did some excellent early work on energy failure levels versus pulse width for semiconductor junctions. Speakman,[8] Pierce,[13] and others have since expanded this work, enabling protection structure designers to arrive at a first-order approximation of the likely failure level of a given structure.

## Bipolar Integrated Circuit Protection

RCA Consumer Electronics Division is a major user of bipolar ICs in a hazardous environment, a domestic TV receiver. A receiver can be subjected to transients from power lines, lightning, and picture-tube flashover. The latter is a severe requirement, as the energy-storage capacitor can be in excess of 2000 pF and peak discharge currents into the IC can be more than an order of magnitude greater than those obtained using the standard human-body ESD model.

Following considerable experimentation with various protection schemes, the dual polarity SCR protection network shown in Fig. 4

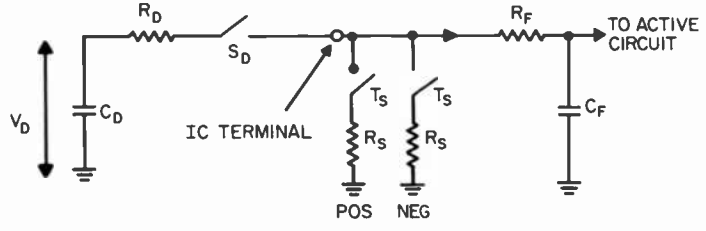


**Fig. 3**—Bipolar transient protection circuit including transient filter.

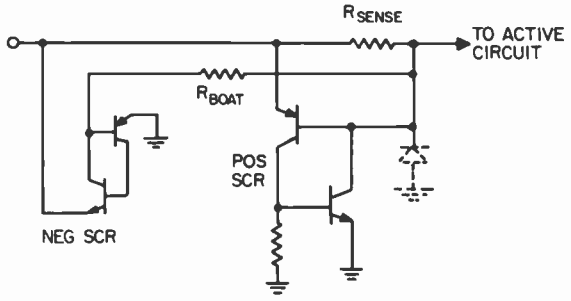


**Fig. 4**—SCR protection structure incorporating transient-current sense resistor.

was evolved. It incorporates a transient-current sense resistor which, in conjunction with the diffused pocket-to-substrate junction capacitance, also serves to limit the leading edge pulse seen by the active circuit. This structure has been used to protect devices to greater than 12 kV, using the human body ESD model, and to over 4 kV using a 2000-pF/500-ohm EOS model.[14] Fig. 5 shows the "multi-zap" failure characteristic of the structure when using a worst-case ESD model of 200 pF and 150 ohms. The high energy handling capability of this device is due to the negative 'on' resistance characteristic of plasma structures. Fig. 6 shows the 'on' resistance characteristic for the SCR protection device.

## MOS Integrated Circuit Protection

Various protection structures that have been used to protect MOS ICs are thick- and thin-oxide FETs, gated diodes, punchthrough devices, zener diodes, spark gaps and, parasitically, SCRs. Each

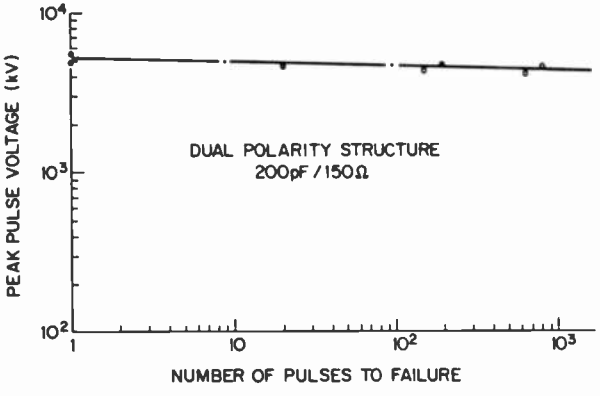


**Fig. 5**—"Multi-zap" failure characteristic.

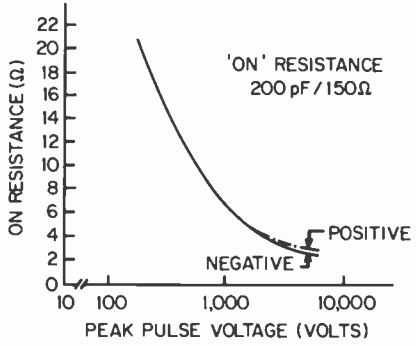


**Fig. 6**—'On' resistance versus peak pulse voltage.

technology seems to have its 'favorite' structure. However, Hulett[15] and others have shown that in nearly all cases it is the parasitic bipolar structure that provides the required protection.

A generic bulk CMOS input protection circuit is illustrated in Fig. 7. $D_1$ and $D_2$ are large-area diodes with direct connections to the $V_{DD}$ and $V_{SS}$ rails. $R_2$ is either a polysilicon or diffused resistor, which is used in conjunction with the input capacity of the inverter to limit the risetime and, hence, peak voltage at the gate of the first transistors. This circuit has been used to successfully protect 5-μm CMOS to "single-zap" ESD failure levels of greater than 4 kV.

The output buffer circuit also includes two clamping diodes to $V_{DD}$ and $V_{SS}$ as shown in Fig. 8. These diodes are actually formed parasitically, by the drain diffusions of the p and n MOS transistors. Two additional components are necessary to complete the full protection circuit: a diode and an SCR between $V_{DD}$ and $V_{SS}$. Both are formed parasitically during the normal manufacturing process and are essential to the safe handling of ESD transients between input and output terminals or between either terminal and $V_{DD}$ or $V_{SS}$. For example, if a positive pulse is applied to the input with respect to the output, the current will flow through $D_1$, the parasitic SCR, and $D_4$. If the parasitic SCR were not present, the current path could be through $Q_1$ source-to-drain punchthrough, a much weaker and, therefore, potentially catastrophic path. When used in a system, EOS transients are clamped to either the $V_{DD}$ or $V_{SS}$ rails by the

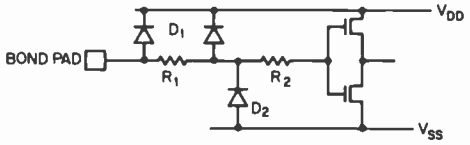


**Fig. 7**—Basic CMOS input protection circuit.

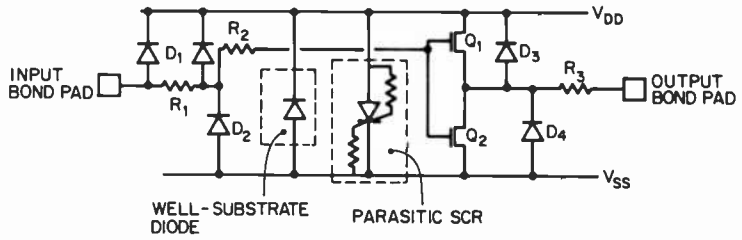


**Fig. 8**—Bulk CMOS output buffer circuit including parasitally formed components.

diodes. Since the $V_{DD}$ supply potential is well below the parasitic SCR trigger voltage, the latter plays no part in protecting the device once it is plugged into a system.

## Handling Precautions for Static-Sensitive Devices

Alert semiconductor manufacturers have been aware of the detrimental effects of ESD for a long time, and have established static-free assembly environments, coupled with worker training, parts shipping procedures, and containers. To maintain adequate protection and guarantee product integrity, all users of semiconductors should do likewise.

There have been many excellent papers dealing with handling precautions for static sensitive parts.[24–27] Some authors advocate a fully conductive environment, while others prefer one that is not capable of generating a static charge. Both schools of thought, however, agree that static controls must be complete throughout the entire receiving, fabrication, assembly, test, and shipping areas. Failure at any point could be catastrophic. Worker training and cooperation, which are essential in any operation, are vital where ESD is concerned, because parts can be damaged at static discharge levels well below the threshold of feeling.

There are two main rules to remember when creating a static-free working environment:

1. Treat or remove from the work area *ALL* static producing items.
2. Suitably ground everything and everyone that moves.

It is surprising how many factories exist where elaborate precautions are taken when inserting static sensitive devices, but nonsensitive devices are still brought to the line in untreated white polyfoam material, which is often charged to tens of kV. To combat this problem, many aerospace and automotive companies now require all parts, whether sensitive to static or not, to be shipped in non-

static or treated materials. Parts bins, intermediate shipping containers, work surfaces and tools should all be made of antistatic or conductive material, or be suitably treated with a topical antistat. Care must also be taken to protect against casual intruders such as foam coffee cups or plastic pocket books.

Moving objects are a particular problem, and it must be assumed that they will become charged sooner or later. *Everyone,* whether fixed or mobile, should wear and use a wrist strap. The type chosen should depend upon user preference (if you like it, you are more likely to wear it), but loose-fitting types should be avoided, as they can easily slip over sleeves and become ineffective. For the same reason, wrist straps should be checked for continuity at least once a day.

Carts and conveyer belts pose special problems, but they should not be ignored as they have been responsible for damage to many sensitive semiconductors. The use of conductive wheels, belts, and bearings solves the problem permanently, and they are virtually maintenance free.

In some circumstances, it is not possible to use conductive or antistatic materials. For these situations, high relative humidity has been employed, but this can prove to be expensive, particularly in cold, dry environments. Mykkanen[16] has shown that whole-room air ionization can be an alternative, and less expensive, approach. Cognizant semiconductor manufacturers are also turning to this technique to control particulate contamination, as well as static charges, in the wafer fabrication areas. Whole-room air ionization is an area where we can expect to see a lot of activity during the coming years.

Hansel[17] has shown that an interesting and beneficial side effect of worker participation in an active ESD program was a general improvement in product quality, and a reduction in non-ESD-related defects. Others[18–20] have shown that the initial investment can pay for itself in a very short time.

## Latent ESD-Induced Failures

There has been considerable conjecture over the question of whether latent ESD-induced failures are real or not. Indeed, much of the early evidence seemed to show the opposite, i.e., healing of damaged parts with time and temperature. However, McAteer[4] and Whitehead[5] have shown that there is indeed reason for concern. Although their work was done on different types of product, the resulting conclusions are basically the same.

Latent, ESD-induced, defects can be roughly divided into three categories:

(1) ESD damage is slight, with the part fully able to meet specification. There is a high probability that these parts will continue to function throughout their required life, and the damage may even anneal out with time and temperature.
(2) ESD damage is more severe. The part may still meet specification (just) or be slightly out of specification but still able to function in the system. There is a reasonable probability that many of these parts will fail prematurely. The others may remain unchanged, or even 'heal' during life.
(3) ESD damage is sufficient to cause the part to fail to meet specification, but it still functions in the system. (This assumes that the part was damaged after device testing, but before system/board check.) There is a high probability that a substantial number of these parts will fail prematurely.

The actual damage that occurs will vary, and depends upon a number of factors. Damage can be roughly divided into the following categories:

(1) Damage to the oxide, either charging or rupture.
(2) Metalization damage, either junction spiking or electrothermomigration (ETM), where a metalization filament bridges two or more junctions.
(3) Bulk silicon remelts. These are more EOS-related, are usually visible upon optical inspection, and will not be dealt with here.

Oxide charging changes the effective threshold voltage of MOS transistors and can even cause parasitic leakage paths between components on the chip. This type of damage will normally heal with time, and the healing can be accelerated by a biased, high-temperature bake. Oxide rupture normally results in a gate-to-channel/source/drain short or Schottky barrier diode formation. In mild cases, this type of failure may go undetected, with the part functioning normally, except for increased leakage. Consequently, it may escape normal testing procedures, resulting in a malfunction only at temperature extremes.

Alloy spiking and electrothermomigration of the junction have been well described by Wood[21] and DeChiaro[22] and reiterated by Whitehead.[5] The result is an increase in junction leakage. In cases of mild damage, the resulting filament may not affect normal system operation and may even 'fuse' if another overstress occurs. This type of 'healing' phenomenon is sometimes seen when step

stressing a device at successively higher levels of ESD. The evidence to date indicates that these types of defects are more likely to result in failure during life than not. There is also an indication that these parts may be more susceptible to system EOS transients than undamaged parts.[23]

## Future Considerations

The scaling of CMOS, as with any technology, causes new problems in the ESD protection area. Oxides are thinner, device geometries smaller and shallower, and devices faster. To protect these new circuits to the same level as the 4000B series CMOS parts, without degrading their potential speed, is a formidable challenge. To compound the problem, many custom VLSI circuits have a large number of I/O ports, which limits the area available for the protection circuit. So far, designers have been able to meet the challenge, but the day may not be far away when a trade-off between speed and ESD performance is necessary. This will place a greater emphasis on system protection and correct handling procedures during assembly.

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# Reliability in Communications Satellites

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**Abstract**—The reliability of complex communications satellites is discussed as well as the elements necessary to insure the specified life. Some of the these elements are novel to commercial communications satellite, and generally are found only in military satellites having very exacting reliability requirements. Also treated are some of the changes that have been implemented within the last decade to enhance reliability and increase life of space communications satellites.

## 1. Introduction

Modern commercial communications satellites cost approximately $50 to $100 million each to design, build, test and launch. Since current satellite designs do not have repair capability once launched, the system's design must have an inherent reliability and compensating provisions similar to the most demanding military systems for the satellite to be profitable. It is not unusual to require a commercial communications satellite to have a design life of ten years, with the additional requirement of a high predicted reliability at the seven or eight year point.

A number of techniques for commercial communications satellite programs implemented by RCA to achieve high reliability and long life are discussed in this paper. These methods and techniques are applicable to other similar applications where it is desired to have a program emphasizing reliability, long life, and reasonable costs.

## 2. Techniques Used to Achieve Inherent Reliability

To have a satellite system that is reliable over a long mission life, reliability requirements must be part of the inherent design. From a programatic viewpoint, this involves the following steps:

- Setting design goals for mission life and probability of achievement
- Performing reliability trade-off studies to select optimum design with redundancy
- Instituting design constraints to meet design goals, particularly end of life parameter degradation and derating requirements
- Planning
  Reliability program plan
  Parts and materials control plan
  Subcontractor and vendor control plan
- Monitoring of results

In the RCA Satcom program the above planning was defined as a series of reliability task elements which had to be performed during the design of the spacecraft. These elements were:

- Reliability Prediction
- FMECA (Failure Modes Effects and Criticality Analysis)
- Limited-Life Items
- Worst-Case Analysis
- Failure Reporting, Analysis and Corrective Action
- Parts, Materials, Processes Control

A description and purpose of each of these elements follows.

### 2.1 Reliability Prediction

The purpose of a reliability prediction is to determine the mission life potential of the design configuration, provide a basis for redundancy and trade-off analyses, and to optimize the design configuration for life-cycle cost. The proposed system design is configured into reliability block diagrams from which mathematical models may be formulated. The system's inherent reliability may then be calculated using failure rates of the constituent parts based on MIL-STD-217,[1] orbital experience of similar designs, or special testing.

The following example illustrates the wide variation in reliability that may occur with changes in the design configuration within a system. Suppose that the main element in a communications channel consisting of a traveling wave tube (TWT), its amplifier network and supporting circuitry has a typical failure rate ($\lambda$) of 3500 FITs (failures per $10^9$ hours of operation). Then the probability

of survival ($P_S$) for several representative configurations is as shown in Table 1.

The $P_S$ computations involve four types of reliability equations: the series exponential, the active redundancy equation, the standby redundancy equation, and a Monte Carlo simulation available on a computer program.[2]

*Example (a): Single Element for One Year*

Here the series exponential equation applies as follows for one year (8760 hours).

$$P_S = e^{-\lambda t} = e^{-(3500 \times 10^{-9} \times 8760)} = e^{-0.03066} = 0.96981. \quad [1]$$

*Example (b): Twenty Elements for One Year, All Active*

Here, the series exponential equation still applies but because there are 20 elements, the exponential term must be multiplied by 20:

$$P_S = e^{-n\lambda t} = e^{-(20 \times 3500 \times 10^{-9} \times 8760)} = e^{-0.6132} = 0.5416. \quad [2]$$

*Example (c): Twenty Elements On At All Times But Only Sixteen Required At Any Given Time*

This involves an active redundancy equation in which $n$ units of equal $\lambda$ are available and $(n\text{-}x)$ units are needed. If all elements have a 100% duty cycle, the $P_S$ is expressed by

Table 1—Reliability Comparison of Various Combinations

| Configuration | $P_S$ 1 Year | $P_S$ 10 Years | Remarks |
|---|---|---|---|
| A Single Element | 0.96981 | 0.73594 | $\lambda$ = 3500 Fits |
| 20 Elements: | | | |
| All 20 Required | 0.5416 | 0.0021 | |
| 16 of 20 Required | 0.9947 | 0.3592 | All active. |
| 16 of 20 Required | 0.9998 | 0.4567 | Four on standby which can switch to any failed unit. |
| 20 Elements, Four Groups of five, one standby per | 0.9696 | 0.1682 | $P_S$ for 16 Channels |
| Group, Switching only | 0.9992 | 0.4382 | $P_S$ for 15 Channels |
| within the Group permitted | 0.9999 | 0.5925 | $P_S$ for 14 Channels |
| 20 Elements, Two Groups of ten, two standby per | 0.9961 | 0.2967 | $P_S$ for 16 Channels |
| Group, Switching only | 0.9998 | 0.5585 | $P_S$ for 15 Channels |
| within the Group permitted | 0.9999 | 0.7630 | $P_S$ for 14 Channels |

$$P_S = \sum_{a=I}^{X} \binom{n}{a} (e^{-\lambda t})^{n-a} [1 - e^{-\lambda t}]^a, \qquad [3]$$

where $\binom{n}{a} = \frac{n!}{(n-a)!\,(a)!}$, $0! = 01$, and

$I$ is the minimum number of failures permitted (i.e., for $x = I$ one term of the binomial is obtained; for $I < x$ a summation of the applicable terms is obtained).

*Example (d): Sixteen Required At All Times, But Twenty Elements Used With Four On Standby (Inactive)*

This involves a standby redundancy equation in which the units of equal $\lambda$ are available and $m$ units are on standby. If the standby $\lambda$ is assumed to be zero and the duty cycle is 100%, then the $P_S$ is expressed by

$$P_S = e^{-(n-m)\lambda t} \sum_{a=1}^{m} \left[ 1 + \lambda t + \frac{(\lambda t)^2}{2!} + \ldots \frac{(\lambda t)^m}{m!} \right], \qquad [4]$$

where $m$ is the number of standby units and $n$ is the total number of units (active plus standby).

*Example (e): Twenty Elements Available Divided Into Groups With At Least One Standby Per Group Available (Illustration Is For Two Groups of Ten and Four Groups of Five)*

Here the mathematical equation is very complex and therefore a Monte Carlo simulation available on a computer program[3] was used in which the $P_S$ is estimated on a number of repeated trials. The number used depends on the accuracy desired. In Table 1 one thousand trials were used.

Table 1 illustrates several important considerations that must be taken into account during the reliability trade-off analysis. For both a relatively short-duration (one-year) mission and a long-duration (ten-year) mission, the table illustrates the effect upon the probability of a successful mission when a system has

(a) No redundancy capability
(b) Active redundancy
(c) Stand-by redundancy with the ability to switch on a replacement for *any* failed unit
(d) A group configuration with each group having standby redundancy, and with replacement switching available *within* the group.

Figure 1 shows the reliability block diagram of a typical communications subsystem. The figure depicts the communication payload for the Advanced Satcom, which was the first RCA communications satellite using solid-state power amplifiers (SSPAs) to replace traveling-wave-tube amplifiers (TWTAs). Note that this reliability model involves the use of reliability equations that range from a simple series reliability equation to the use of a Monte Carlo simulation.

To illustrate, items 1, 2, 3, 5, 6, 9, and 11 involve just series reliability, i.e.,

$$R = R_1 \cdot R_2 \cdot R_3^2 \cdot R_5^2 \cdot R_6^4 \cdot R_9 \cdot R_{11}.$$

Item 4 involves standby redundancy with $m$ standby units out of a total of $n$ units. In this case, $n = 4$ and $m = 2$. The general equation is expressed as

$$R = e^{-(n-m)\lambda t} \sum_{a=0}^{m} \left[ 1 + \lambda t + \frac{(\lambda t)^2}{2\,!} + \ldots \frac{(\lambda t)^m}{m\,!} \right]; \qquad [5]$$

$$R = e^{-2\lambda t} \left[ 1 + \lambda t + \frac{\lambda t^2}{2} \right]. \qquad [6]$$

Item 8 involves active redundancy in which $x$ failures are permitted in $n$ units of equal $\lambda$, i.e., $(n\text{-}x)$ are needed, which in this case is (4-1) or 3. This involves finding the reliability for just one EPC at a given period in time and then utilizing the binominal distribution equation to calculate the reliability of the $(n\text{-}x)$ combination required. The general equation is expressed as

$$R = \sum_{a}^{x} \binom{n}{a} (e^{-\lambda t})^{n-a} [1 - e^{-\lambda t}]^a,$$

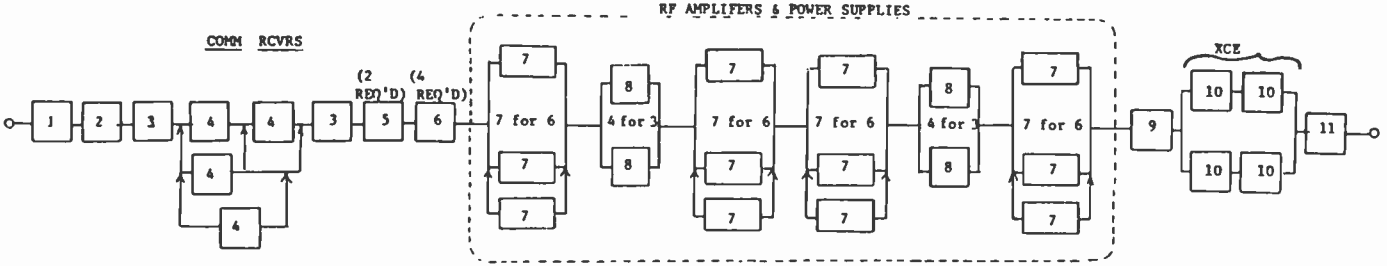
where $\binom{n}{a} = \dfrac{n\,!}{(n-a)\,!\,(a)\,!}$

and $a$ is an integer that varies from zero to $x$. For this specified case of one failure permitted,

$R = R_8^4 + 4R_8^3 Q_8$, where $Q_8 = 1 - R_8$.

Item 10 involves both series and parallel redundancy. For the series string, the reliability, is $R = R_{10} \cdot R_{10} = R_{10}^2$. When both strings are put together in parallel the reliability of the entire string, $R_T$, is

$$R_T = 1 - Q^2$$




| Block/Yr | Description | Failure Rate $10^{-9}$ | Duty Cycle % |
|---|---|---|---|
| 1 | Main Communications Antenna | 90 | 100 |
| 2 | Input Filters & Waveguides | 39 | 100 |
| 3 | Communication Receiver Coaxial Switch Matrix | 16 | 100 |
| 4 | Communications Receiver | 2044 | 100 |
| 5 | Hybrid Couplers (2 Required) | 20 | 100 |
| 6 | Input Isolators (4 Required) | 40 | 100 |
| 7 | SSPA/Atten/Switches/Filters/Etc. | 779 | 100 |
| 8 | Electronic Power Conditioners (EPC) | 1000 | 100 |
| 9 | RF MUX Manifold & Waveguides | 8 | 100 |
| 10 | SSPA Heaters | 1860 | 1 |
| 11 | Output Filters & Waveguide | 114 | 100 |

**Fig. 1**—Reliability block diagram of the advanced Satcom Communications Satellite.

where $Q = 1 - R_{10}^2$.

Item 7 involves four groups of seven SSPA's in which one failure is permitted per group, i.e., switching a replacement for a failed amplifier is only permitted within the group. In this case, the analysis can be readily calculated using Monte Carlo simulation techniques or by using equations giving an exact solution if one is not interested in knowing about additional failures within the group. The number of trials used depends on the accuracy desired, but normally 1000 trials suffice. After the reliability of one group is calculated for a given time period, it must then be raised to the fourth power to calculate the reliability for the four groups.

## 2.2 FMECA (Failure Modes, Effects, and Criticality Analysis)

An FMECA is a necessity on complex, nonrepairable systems and is a requirement on satellites procured by the Government.[4,5] Its purpose is to systematically evaluate potential failure modes and determine their effect on performance and mission life. The process can also identify which of the failures are single-point failures, i.e., failures whose occurrence can abort an entire function or even the entire mission. The analysis provides a basis for trade-offs, where to use fusing, and what items are to be highlighted during the test program. It can also be used to insure that a low probability of failure exists for any single-point failure that cannot be eliminated. FMECAs are routinely performed on all subsystems and systems associated with RCA commercial satellites.

An FMECA may be performed at a parts level, box level, or a systems level. One page of a FMECA for the C-Band SSPA is shown in Table 2. This is a portion of the FMECA which concentrates on the active devices and assembly techniques used in the construction of the SSPA. In addition to identifying single-point failures, it is useful in post-launch failure analysis to determine probable failure mechanisms in orbit. In this particular FMECA, the loss of gate voltage was identified as a possible failure mode with resultant catastrophic results. However, if the drain voltage can be automatically turned off with the loss of gate voltage, catastrophic failure may be averted. The SSPA can then be rebiased and placed in service with changed operating conditions that might be acceptable for certain services. This automatic cutoff was included in the bias design as a result of the FMECA.

Some additional benefits that resulted from the FMECA for the early RCA Satcom Program are (1) compensating provisions were

Table 2—Failure Mode, Effects and Criticality Analysis for 8.5 Watt Amplifier

| Item | Failure Mode | Possible Cause | Symptoms and Local Effects Including Dependent Failure | Existing Compensatory Provisions | Remarks and Recommendations |
|---|---|---|---|---|---|
| Isolator | Loss of Isolation, Increase of Insertion Loss | Ferrite Crack | Decrease or Loss of Signal Level, Gain | None | |
| | Change in VSWR | Loss of Terminating Resistor | Gain | | |
| Drain Supply | No Voltage | Part Failure | Loss of Signal | Redundant Units | |
| | Loss of Regulation | Part Failure | Decrease in Gain, Power Levels | Redundant Units | |
| Gate Supply | No Voltage | Part Failure | Loss of Gain, Power Level, Transistor Burnout | Redundant Units | If Gate Supply is lost, Drain Supply should be automatically turned off. |
| | Loss of Regulation | Part Failure | Variation in Gain, Power Levels | Redundant Units | |
| FLC-30 Output Stage | Loss of Output Power | Open | ~ 1/2 Power Level | None | |
| | Loss of Output Power | Short | ~ 1/2 Power Level | None | Bond Wires should fuse open in milliseconds if Drain Supply can handle surge. |
| FLC-15 Driver | Loss of Output Power | Open | ~ 1/3 Power Level | None | |
| | Loss of Output Power | Short | ~ 1/3 Power Level | None | Bond Wires should fuse open in milliseconds if Drain Supply can handle surge. |
| FLC-08, FLC-02 HFET-2201 | Loss of Output | Open | Loss of Signal | None | |
| Interstage Connection | Loss of Output | Lifting of Bond | Loss of Signal | None | |
| Coupler Bond Wire | Decrease in Output | Lifting of Bond Wire | Decrease in Output Signal | None | |
| Bypass Capacitor | Bias Circuit Oscillations | Opening of Capacitor | Loss of Signal | None | |

added during the design for a momentum wheel run away failure mode, which was highlighted by the FMECA, and (2) a fusing plan was developed for the satellite power supply system so that a gross short in one of the redundant boxes would not affect the other boxes.

## 2.3 Limited-Life Items

The purpose of a limited-life items study is to identify those items whose wear out region may fall within the time frame of mission life. The analysis is also used to identify what special controls are required for each identified limited-life item. These controls include serialization and lot control, time and cycle record keeping, special packaging, tolerance selection, design constraints on stress conditions, or even design modification.

Some of the benefits that resulted from the limited life items study and analysis are as follows:

*(a) Shielding of CMOS Devices for Protection Against Long Term Radiation Effects*

An analysis of the Satcom F1 orbit forecast that the radiation dosage that would be encountered by any part on the satellite would vary as shown in Fig. 2.[6] This figure shows the radiation dosage encountered in Rads(Si) as a function of mils of aluminum shielding. By doing a sector analysis, one can determine the amount of aluminum shielding available and the dosage encountered by parts in that section.

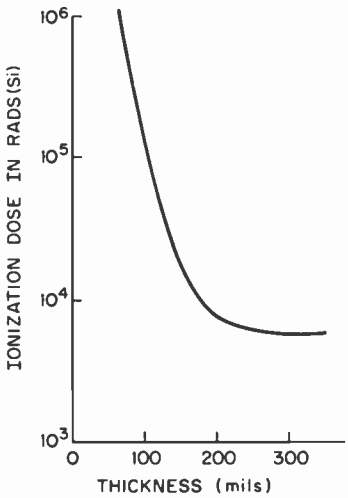



**Fig. 2**—Radiation dosage as a function of aluminum shielding thickness.

To illustrate, suppose the Command portion of the Satellite had an equivalent shielding of 140 mils of aluminum; then, the forecasted radiation dosage encountered during the mission life for the Command Subsystem would be in excess of $2 \times 10^4$ Rads(Si). Since radiation tests indicated that the CMOS parts manufactured in 1973 could only survive $1 \times 10^4$ Rads(Si) as used, they would have to be protected. This was done by adding 10 mils of lead to each CMOS device on Satcom F1. The 10 mils of lead is equivalent to increasing the aluminum shielding by 40 mils, so that now the forecasted dosage would be less than $1 \times 10^4$ Rads(Si), which is an acceptable level. On subsequent satellites in the series, the shielding efficiency was improved even further by using tantalum shields instead of lead.

*(b) Installation of the Flight Batteries Just Prior to Shipment and Use of "Work-Horse" Batteries During the Test Phase*

The life expectancy of a battery pack is greatly dependent on the conditions and environment of its application. For example, the life expectancy is greatly influenced by the surrounding temperature, the number of charge-discharge cycles, the depth of each discharge cycle, and the rate of charge during the charge cycle.[7] In prior analyses, it was found that even with the design controlling these factors, the battery pack could be a life-limiting item when long-duration (ten-year) missions were desired. A synchronous satellite such as Satcom F1 encounters 88 eclipses per year or 880 for a ten-year mission. The depth of discharge is typically in the range of 40 to 55%. For these reasons, it was decided that a new battery pack would be installed just prior to shipment.

## 2.4 Worst-Case Analysis

The purpose of a worst-case analysis is to assure that each circuit or function will perform adequately, both at the beginning of the mission and at the end of mission life. End-of-life (EOL) parameters must be determined for each part and then the circuits analyzed to ensure that the EOL parameters are compatible with mission life.

The study considers the worst combination of initial tolerance, degradation, and the effects of thermal, environmental, and radiation stresses. One page of a worst-case analysis of gain degradation is shown in Fig. 3 for the C-band SSPA used on the Advanced Satcom series of RCA commercial communications satellites. This amplifier has an EOL requirement of an output power of 8.5 watts (39.3 dBm). The beginning of life output power is specified to be 9.0 watts (39.6 dBm) nominal.

| Drop in Gain (dB) | Power Levels (dBm) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| 0 | -10.00 | 3.60 | -2.80 | 10.03 | 9.63 | 18.51 | 18.11 | 27.40 | 24.20 | 30.90 | 27.70 | 34.23 | 39.83 | 39.58 |
| -0.10 | -10.00 | 3.50 | -2.90 | 9.83 | 9.43 | 18.21 | 17.81 | 27.20 | 24.00 | 30.70 | 27.50 | 34.08 | 39.68 | 39.43 |
| -0.20 | -10.00 | 3.40 | -3.00 | 9.63 | 9.23 | 17.91 | 17.51 | 27.00 | 23.80 | 30.60 | 27.40 | 33.95 | 39.55 | 39.30 |

| Drop in Output Power | |
|---|---|
| Watts | dBm |
| 9.07 | 0 |
| 8.77 | -0.14 |
| 8.51 | -0.28 |

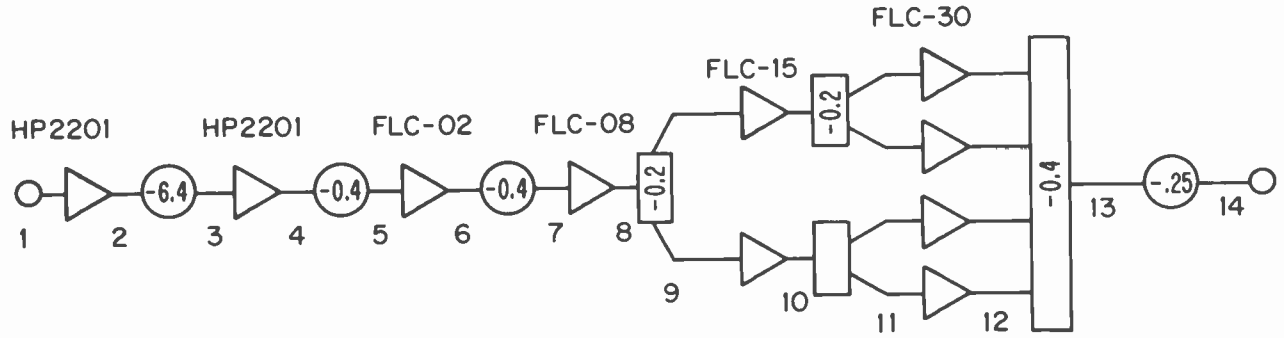



**Fig. 3**—C-Band solid-state-power-amplifier gain worst-case analysis. Assumptions: 4.0 GHz; −10 dB input; 6 dB chip attenuator between points 2-3.

A calculation is made of the results of 0.10 dB degradation in each of the active devices in the SSPA and its effect on output power. As seen in Fig. 3, a simultaneous 0.10 dB drop in gain of each of the active devices results in a decrease in the output power from 9.07 watts to 8.77 watts (39.58 dBm to 39.43 dBm). An 0.20 dB drop in gain results in an output power (8.51 watts) which just meets EOL requirements. This information is used to establish failure criteria for each part and hence its reliability requirement. This illustrates that the failure criteria for these devices is system dependent. A larger beginning of life margin would permit the use of devices with larger parameter changes as a function of life to meet EOL mission needs.

## 2.5 Failure Reporting, Analysis and Corrective Action

The purpose of failure reporting is to ensure that every test failure has been accounted for. Properly applied, it provides positive feedback and corrective action to prevent recurrent failures and spots trends early in the test program to improve design and reduce workmanship problems. A formal, closed-loop, in-house reporting system was applied to the Satcom Program with the inception of the test program.

This reporting system had many benefits both in the early Satcom F1 and in later spacecrafts. Some of the items discussed in Sec. 4 were benefits of this reporting and corrective action system.

## 2.6 Parts and Materials Control

The importance of a formal parts and materials program to satellite design cannot be over emphasized. The reliability of the satellite is directly influenced by the reliability or quality grade of the parts and materials used and how the design applies them. The parts and materials control program for a non-repairable long-life satellite must consider such things as:

(a) High quality parts and materials selected as standard or preferred types for the design to use.
(b) Control of all nonstandard parts and materials to ensure that they comply with mission objectives.
(c) Special testing, screening and inspection for space use.
(d) Design guidelines to place constraints on the designer for derating, end-of-life parameters, outgassing, radiation, and flammability requirements.
(e) A parts and materials application review and stress analysis.

From the inception of the Satcom F1 Program, a decision was made to use the best parts available consistent with cost and schedule. For the early Satcoms, microcircuits having a Class A MIL grade or Class A equivalents[8] were required. For the Advanced Satcoms, microcircuits having a JAN S MIL grade[9] or Class S equivalents were required.

Many benefits resulted from this formal program to control the use and application of the parts and materials. Many items whose qualification for space use was not documented were disallowed. The screening requirements (including lot qualification and sampled destruct physical analysis at incoming) became more stringent and were more uniformly enforced. Last, the application analysis was rigorously performed and enforced. This resulted in better thermal control, lower operating temperatures, and lower electrical stresses, with resulting longer life and better reliability.

## 3. Reliability Requirements of the Satcom Satellites

Each Satcom satellite had a reliability requirement based on a specified number of transponders being available at various intervals of orbital life. To validate the feasibility of the requirement, a prediction was performed for the Satcom F1 design in 1974 utilizing the techniques and methods of MIL-HDBK-217A. The vintage of the failure rates was also that of the then current MIL-HDBK-217(Rev A); however, an improvement was factored into the failure rates for any steps taken to upgrade the quality level of the parts, such as retest and remeasurement at incoming inspection. This was consistent with RCA's experience on other spacecraft programs at that time.

For ease of reliability assessment, the Satcom F1 satellite was partitioned into the following functional systems:

(a) Coast and Insertion
(b) Communications
(c) Command, Ranging, and Telemetry
(d) Power
(e) Attitude Control
(f) Propulsion
(g) Structures and Thermal

This approach permitted a direct comparison between individual functions and a means of evaluating the relative reliability contribution of the various functions or subsystems.

Due to the complexity of the calculations for the communications subsystems, where it was necessary to know the probability of how

many channels would be available in any given year of orbital life, a computer program[3] was successively improved and refinements added so that complex combinations could be evaluated with relative ease using Monte Carlo simulation techniques. This program was especially necessary for the Advanced Satcom which had many design refinements, including an availability of 28 transponders (24 active and 4 in standby). Without the computer program the calculations would have been extremely difficult, since the transponder arrangement was to have four groups of seven, with one standby spare in each group.

As in the case for Satcom F1, a reliability prediction was also performed for the design of the Advanced Satcom. The methods used were consistent with those contained in MIL-HDBK-217C. The Advanced Satcom was also subdivided into functional subsystems to evaluate the overall reliability. The reliability requirements for both Satcom F1 and the Advanced Satcom, along with the calculated values, are shown in Table 3.

## 4. Changes Adopted to Enhance Reliability Growth

An examination of Table 3 shows that the eight-year predicted lifetime for the Satcom satellites 20-channel availability improved from 0.515 for Satcom F1 to 0.766 for the Advanced Satcom. A number of significant improvements were incorporated to insure both longer life and greater reliability. Probably the most significant improvement in the C-Band communications has been the incorporation of the solid state power amplifier (SSPA) using a gallium arsenide FET to replace the TWTA. This change resulted in better packaging, reduced weight, and lower power consumption. Another change made in the communications subsystem was better utilization of reliability combinations. Satcom F1 had 24 transpon-

Table 3—Satcom Reliability Requirements Summary*

| Available Channel Conditions | Satcom F1 | | Advanced Satcom | |
|---|---|---|---|---|
| | 8 Years Requirement | Predicted | 8 Years Requirement | Predicted |
| 20 Ch Comm & Bus | 0.5 | 0.515 | 0.70 | 0.766 |
| 20 Ch Comm | — | 0.7301 | — | 0.964 |
| Bus Only | — | 0.7099 | — | 0.8004 |
| Coast & Insertion | — | 0.9933 | — | 0.9926 |

* Above figures include all telemetry functions

ders, while the Advanced Satcom has 28 transponders, 4 of which are in standby. These changes improved the predicted reliability for the communications subsystem from 0.7301 to 0.964 for the 20-channel availability situation. To further illustrate, a TWT has a commonly accepted failure rate of 1000 FITs, where FIT is one failure per $10^9$ hours. To this must be added the electronic power conditioner (EPC), which has a commonly accepted failure rate of another 1000 FITs. Thus for each channel, the sum of the TWT and the EPC totals 2000 FITs.

In contrast to this, an SSPA such as used on the Advanced Satcom Satellite has an equivalent failure rate of approximately 450 FITs (457 was actually used), exclusive of the EPC.

Each EPC also has a failure rate of 1000 FITs; however, the transponders were configured with two groups of four EPCs, of which only three per group are required for successful operation of any 24 of the 28 amplifiers. A switching matrix allows maximum benefit from this EPC and amplifier redundancy arrangement. A comparison of just the redundancy improvement is dramatic and is shown in Table 4.

The orbit performances for the SSPAs have lived up to the predicted reliability. As of this date 84 SSPAs are in orbit (72 are in service and 12 are inactive spares) on three Advanced Satcoms, and a total of over 560,000 operating orbital unit-hours have been accumulated.

Other changes were made to improve long term life, reliability, and performance:

(a) The battery subsystem was increased to be 17 ampere-hours per assembly instead of the 12 ampere hours used on Satcom F1.

Table 4—Comparison of TWT versus SSPA Reliability

| Item | (FITs) | Condition | Predicted Reliability (8 Years) |
|---|---|---|---|
| TWT, EPC | 2000 | 24/24*<br>24/28** | 0.0326<br>0.3896 |
| SSPA, EPC | 457, 1000 | 24/28** | 0.9115 |
| SSPA's Only | 457 | 24/28** | 0.9749 |
| EPC's Only (in SSPA Application) | 1000 | 3/4*** | 0.9749 |

* Twenty-four channels with no spare.
** Four groups of seven with six operating.
*** Only three of four required per group.

Three assemblies are used per spacecraft, with each assembly having two strings of eleven cells. The greater capacity was achieved by using larger cells.

(b) The torque motor drive on the solar array drive (SAD) was changed to a stepper motor. This change allowed operation with reduced power consumption.

(c) Previously, a single SAD driveshaft was used and it was offset from the center of gravity of the spacecraft. Later the SAD drive shaft was split and each shaft was located at the center of gravity. This configuration is less complex, uses less power, and has the added benefit of redundancy.

(d) A shaped beam was incorporated for the fixed antenna. This change allowed greater coverage with essentially the same antenna size.

## 5. Verification of Newly-Developed Complex Devices

Commercial communication satellites, for technical and competitive reasons, often utilize state-of-the-art devices and subsystems with little prior reliability history. For long-life high-reliability missions, the satellite manufacturer must perform special testing to both qualify and establish the reliability of these devices.

The Advanced Satcom C-Band satellite offers an example of this type of program. A decision was made to replace conventional TWTAs with advanced SSPAs. This required that a special testing program be instituted to establish the reliability of and qualify both GaAs FETs (for the SSPA transponder) and power MOSFETs (for the electronic power conditioner). These testing programs are described below.

### 5.1 GaAs FETs

The qualification of the GaAs devices proceeded in three steps: initial life test studies, stress tests, and flight model life tests.[10] At the conclusion of this testing, the reliability of the GaAs FETs was established and quantified. The failure modes and mechanisms of the devices were understood and a purchase specification was developed to assure reliable long-life devices.

The purpose of the initial testing was (a) to provide experience in the handling, assembling as amplifiers, and testing of these devices, and (b) to identify the failure mode of these devices. This information served as a basis for establishing specifications and screening procedures for the flight-qualified GaAs FETs. The initial tests on

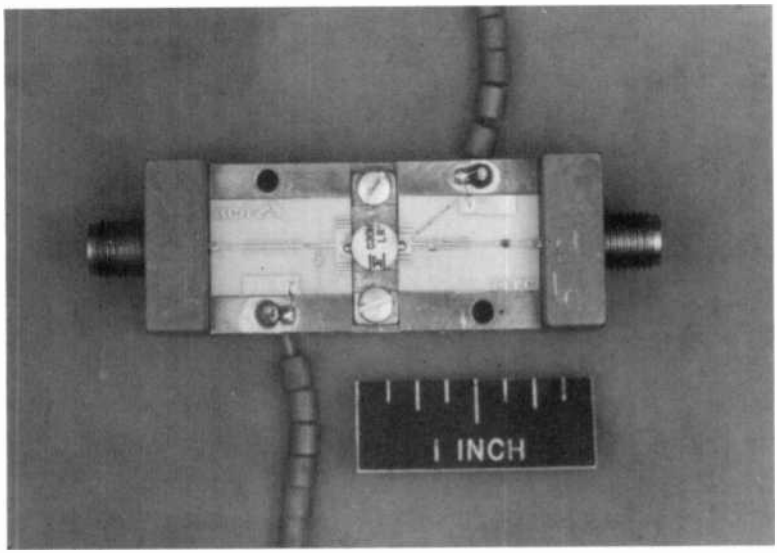



**Fig. 4**—Life-test amplifier module.

commercial-grade devices established that the failure mode was graceful in nature for these parts and that the failure mechanism was source-drain electromigration.

Before attempting a full flight-model life test, it was decided to stress test four GaAs FET devices assembled as amplifier modules to verify assembly techniques. The amplifier modules were stressed successfully for 48-hour intervals at ambient temperatures of 150°C, 165°C, and 175°C. There were no significant adverse effects to either the power output of the devices or the amplifier module components.

The flight-model lifetest consisted of the accelerated temperature testing of twenty-nine GaAs FET hermetically-sealed devices assembled as 2.5 watt amplifier modules. These devices were assembled as amplifiers using space-qualified techniques subject to review and inspection. Fig. 4 shows a device assembled as a life-test amplifier. A schematic of the amplifier components along with the bias circuit is shown in Fig. 5. The unique feature of this test is that the individual life-test amplifier modules are identical to those used in the flight module SSPA. In effect, we qualified the amplifier module for space use.

The life-test conditions are shown in Table 5. The test flow diagram for the life test is shown in Fig. 6. After mounting in the life-test fixture, the dc parameters were measured. The devices were then biased to 9.0 V and 500 mA under rf drive. The temperature of the test fixture was raised to the operating level and the drain

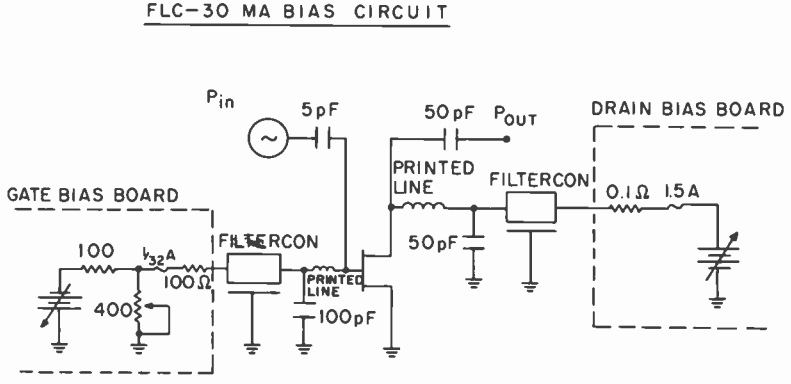



**Fig. 5**—FL-30 MA bias circuit.

current was adjusted in the range 425 to 500 mA (~1/2 of $I_{DSS}$) to bring the channel temperature to the desired level.

The lifetest was conducted until all the devices had failed. The failure mode was graceful in nature, with a gradual degradation of the device gain and output power. The failure mechanism was a complex migration-diffusion problem, in which Au from the device electrodes was determined to be entering the epitaxial GaAs and Ga from the epitaxial material was diffusing to the surface and combining with the Au to form AuGa hillocks. Additionally, Au was migrating along the source-drain fingers in a classical electromigration mode.[11]

A lifetest transistor is shown in Fig. 7. The buildup of Au material is evident at the tip of the source fingers as well as the depletion of Au in the drain finger. An Au hillock is shown in Fig. 8. These hillocks were determined to be AuGa by electron-probe microanalysis. As a result of these tests, it was estimated that the average failure rate over ten years was no greater than 2.0 FITs at an operating channel temperature of 85°C and a 60% confidence limit.

Table 5—Flight Model Life Test Conditions

| | Flight Model | Life Test |
|---|---|---|
| Channel Temperature | 190°C | 215°C |
| Number of Devices | 19 | 10 |
| RF Drive (4.0 GHz) | 27.5 dBm | |
| Drain Voltage | 9.0 V | |
| Drain Current | 425 to 500 mA | |

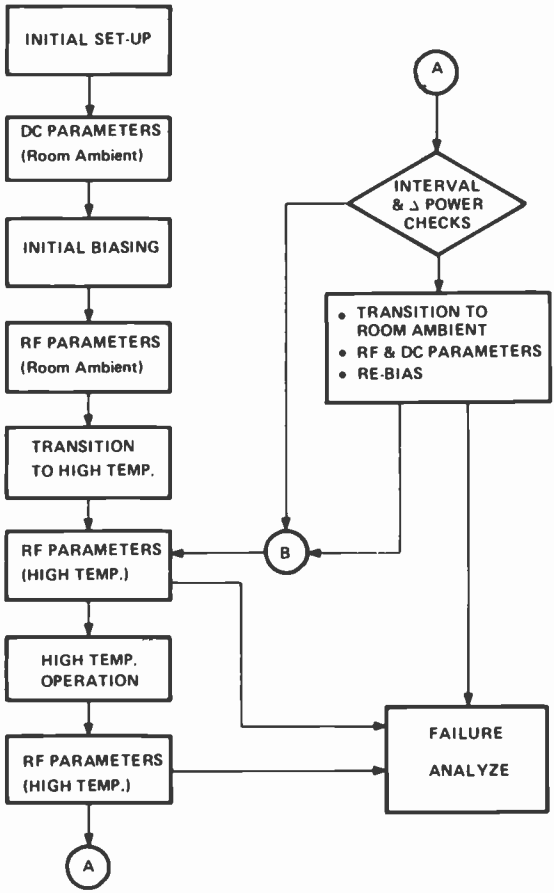



**Fig. 6**—Test flow chart.

## 5.2 HEXFETs

In addition to life testing, another type of special testing often required in satellite programs is the evaluation of radiation hardness. The HEXFET is a Si power VDMOS (vertical double-diffused MOS) field-effect transistor. An optical micrograph of a HEXFET is shown in Fig. 9. For reference, this device is approximately 0.25 inch on a side. The reliability of this device was a concern, and a special program similar to that for the GaAs FETs was undertaken. In addition, an extensive series of radiation tests was conducted to establish the radiation hardness of the device.

The HEXFET device structure is shown in Fig. 10. In operation, holes generated in the oxide by ionizing radiation collisions are

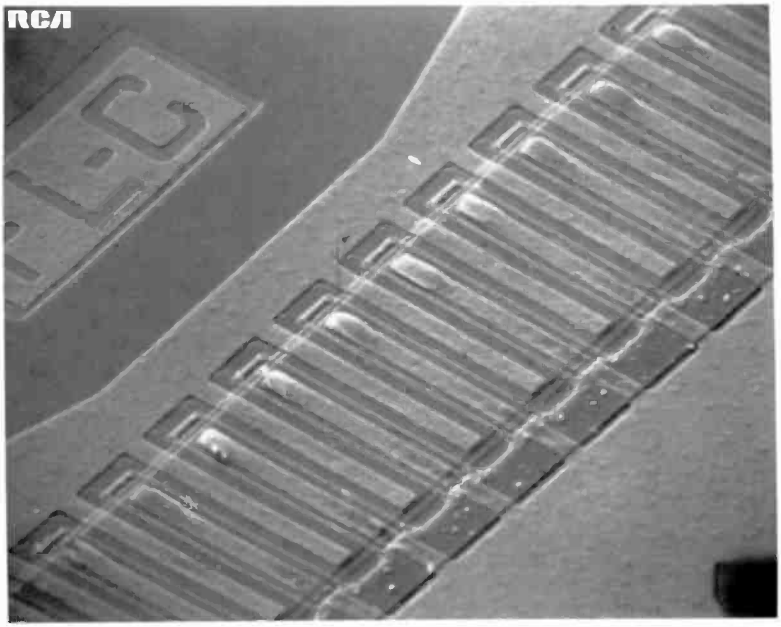



**Fig. 7**—Electromigration on a life-test transistor (original photo was 500× magnification).

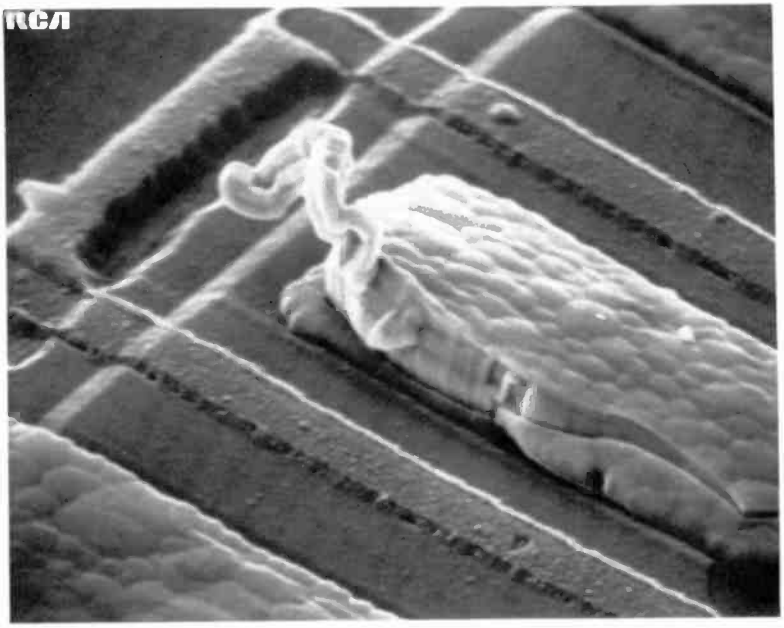



**Fig. 8**—Hillock growth (original photo magnification was 10,000×).

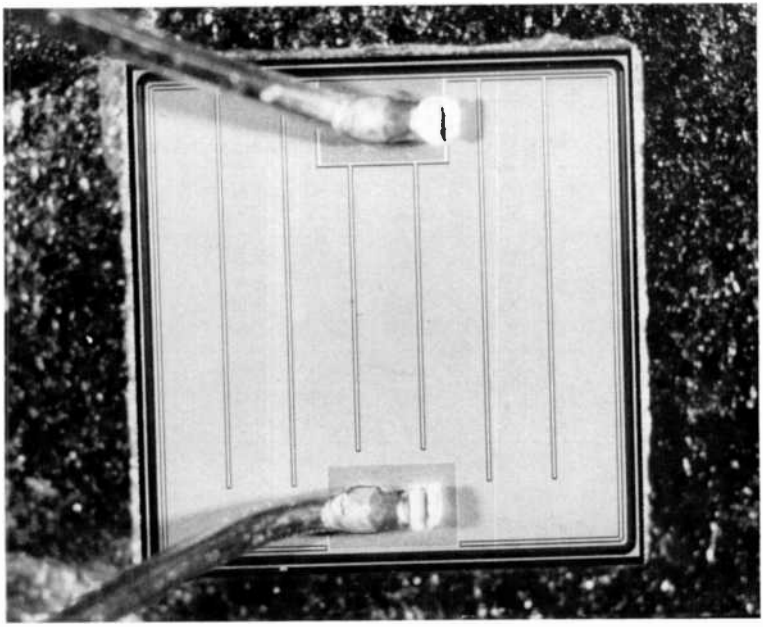


**Fig. 9**—HEXFET optical micrograph (chip is 0.25 inch/side).

driven under the influence of the gate electric field to the Si-$Si0_2$ interface. These holes are trapped at the interface and have the effect of reducing the gate threshold voltage for this n-channel enhancement-mode device. Eventually, the device fails to turn off.

The results of the radiation testing are shown in Table 6.[12] This data indicates that the radiation damage is independent of drain voltage and operating frequency but strongly dependent on gate

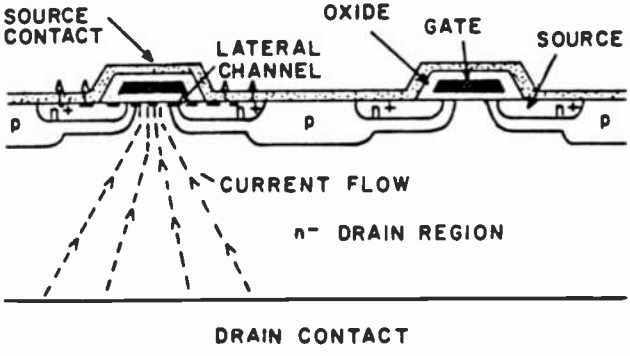



**Fig. 10**—HEXFET device structure.

Table 6—Threshold Voltage Shifts In Irradiated Devices

| Test Conditions | | | $\Delta V_T$ (Volts) After Irradiation to | | | Number of Devices | Initial Threshold Voltage (Volts) |
|---|---|---|---|---|---|---|---|
| $V_{GS}$ (Volts) | $V_{DS}$ (Volts) | Frequency (kHz) | 10 kRad(Si) | 25 kRad(Si) | 40 kRad(Si) | | |
| 18 | 80 | 50 | 1.19 | 2.63 | 3.85 | 2 | 3.71 |
| 18 | 30 | 50 | 1.23 | 2.72 | 3.92 | 4 | 3.63 |
| 14 | 80 | 50 | 1.11 | 2.37 | 3.44 | 6 | 3.82 |
| 14 | 45 | 50 | 1.08 | 2.39 | 3.47 | 6 | 3.73 |
| 14 | 45 | 10 | 1.08 | 2.43 | 3.58 | 6 | 3.85 |
| 14 | 30 | 10 | 1.16 | 2.52 | 3.68 | 4 | 4.00 |
| 10 | 80 | 10 | 0.80 | 1.91 | 3.05 | 6 | 3.81 |
| 10 | 45 | 10 | 0.83 | 1.99 | 3.01 | 7 | 3.76 |
| 10 | 30 | 10 | 0.97 | 2.19 | 3.30 | 6 | 3.99 |

voltage. The maximum allowable radiation dose for these devices was determined to be 40 kiloRads (Si). With this information, the device application was modified to lower the gate voltage to the minimum level allowable consistent with proper device operation. Additionally, since a synchronous satellite with a ten-year mission can accumulate up to $10^5$ Rads(Si) over its lifetime,[13] it was necessary to shield these devices to absorb a portion of the incident radiation.

## 6. Conclusions and Predicted Reliability Results

The techniques discussed have enabled sustained reliability growth

Table 7—Subsystems Reliability and Probability of Survival*

| Subsystem | Satcom F1 | | Advanced Satcom | |
|---|---|---|---|---|
| | 1 Yr. | 8 Yrs. | 1 Yr. | 8 Yrs. |
| Coast and Insertion | 0.9933 | 0.9933 | 0.9926 | 0.9926 |
| CR&T | 0.9967 | 0.9427 | 0.9984 | 0.9217 |
| Power | 0.9975 | 0.9226 | 0.9898 | 0.9182 |
| Attitude Control | 0.9983 | 0.9085 | 0.9992 | 0.9698 |
| Propulsion (RCS) | 0.9880 | 0.9083 | 0.9981 | 0.9800 |
| Structure and Thermal | 0.9990 | 0.9891 | 0.9991 | 0.9949 |
| Comm 20/24** | 0.9963 | 0.7300 | 0.9971 | 0.9639 |
| 24/24** | 0.6336 | 0.0256 | 0.971 | 0.616 |
| Entire System 20/24** | 0.9693 | 0.5147 | 0.9744 | 0.7656 |
| 24/24** | 0.6164 | 0.0180 | 0.9489 | 0.4892 |

* These numerics were taken from the original system predictions, which was conservative since it assumed all telemetry functions are required. If one were interested in the predicted reliability for just essential functions, then, the resultant reliability would be considerably higher.
** 20/28 and 24/28 for the Advanced Satcom.

in a complex communication satellite program. The techniques used are general and may be utilized wherever good initial reliability is required and reliability growth is desired with successive iterative designs. Table 7 shows the growth that is possible. At the eight-year point for an availability of at least 20 channels, the predicted reliability went from 0.51 to better than 0.76, a 50% growth. These predictions were conservative estimates of the reliability to be expected. The observed reliability has exceeded these predicted values.

## Acknowledgements

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## **Patents Issued to RCA Inventors**—First Quarter 1984

### January

**J. G. Aceti** Apparatus for Measuring the Dimensions of Delicate Parts (4,424,630)
**A. E. Bell and Y. Arle** Reversible Recording Medium and Information Record (4,425,570)
**S. L. Bendell** Electron Beam Alignment in Tube/Coil Assemblies (4,429,258)
**D. Botez** Constricted Double Heterostructure Semiconductor Laser (4,426,701)
**J. L. Bradshaw** Frequency-Controlled Variable-Gain Amplifiers (4,429,285)
**R. Brown and P. C. Jozwiak** Composition and Thickness Variation in Dielectric Layers (4,426,249)
**G. N. Butterwick** Photomultiplier Tube Having a Heat Shield With Alkali Vapor Source Attached Thereto (4,426,596)
**K. K. Chang** Deflection Yoke Integrated Within a Cathode Ray Tube (4,429,254)
**D. Chin, J. G. Henderson and R. J. Maturo** Signal-Seeking Tuning System With Signal Loss Protection for a Television Receiver (4,429,415)
**E. L. Crosby, Jr.** Strain Measurement (4,426,875)
**S. B. Deal and D. W. Bartch** Method of Making a Cathode-Ray Tube Having a Conductive Internal Coating Exhibiting Reduced Arcing Current (4,425,377)
**A. R. Dholakia** Flip-Flop Grinding Method (4,428,165)
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**R. A. Gange** Line Cathode Support Structure for a Flat Panel Display Device (4,429,251)
**P. E. Haferl** Variable Horizontal Deflection Circuit Capable of Providing East-West Pincushion Correction (4,429,257)
**L. A. Harwood and R. L. Shanley 2nd** Circuit for Linearly Gain Controlling a Differential Amplifier (4,426,625)
**L. L. Jastrzebski and J. Lagowski** Method for Determining Oxygen Content in Semiconductor Material (4,429,047)
**G. Katz** Method for Improving the Inspection of Printed Circuit Boards (4,427,496)
**J. K. Kim** Method of Making an Array of Series Connected Solar Cells on a Single Substrate (4,428,110)
**R. W. Kipp** Tracking Filter System for Use With a FM/CW Radar (4,429,309)
**T. F. Kirschner** Process for Improving Dimensional Stability of Video Disc Caddy (4,426,349)
**K. H. Knop** Semi-Thick Transmissive and Reflective Sinusoidal Phase Grating Structures (4,426,130)
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**S. A. Lipp and M. P. Adams** Method for Making a Dipolar-Deflecting and Quadrupolar-Focusing Color-Selection Structure for a CRT (4,427,395)
**S. A. Lipp** Focusing Color-Selection Structure for a CRT (4,427,918)
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**D. L. Sherwood** High-Speed Data Sorter (4,425,617)
**A. M. Smith** Fail Soft Tri-State Logic Circuit (4,425,517)
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**W. Truskalo** Television Receiver Power Supply Ferroresonant Load Circuit Provided With a Redundant Operating Capability (4,429,260)
**J. Tults and C. M. Wine** Arrangement Useful in a Phase-Locked Loop Tuning Control System for Selectively Applying an AFT Voltage in a Manner to Improve Loop Stability (4,426,734)
**L. J. Vieland and R. C. Alig** Color Picture Tube Having an Expanded Focus Lens Type In-Line Electron Gun With Improved Static Convergence (4,429,252)
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**L. K. White and M. Popov** Planarization Technique (4,427,713)
**H. A. Wittlinger** Differential Current Amplifier (4,429,283)

**February**

**A. Acampora** Arithmetic Circuits for Digital Filters (4,430,721)
**S. Berkman** Chemical Vapor Deposition of Epitaxial Silicon (4,430,149)
**F. Caprari and R. A. Geshner** Visual Defect Inspection of Masks (4,432,641)
**L. A. Cochran** Automatic Video Signal Peaking and Color Control (4,430,665)
**R. D. Faulkner and R. E. McHose** Electron Discharge Device Having a High Speed Cage (4,431,943)
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**M. Nowogrodski** Wheel Wear Measurement System (4,432,229)
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**L. N. Schiff** FM/TV Transmission System (4,434,440)
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**C. H. Strolle and T. R. Smith** Generating Angular Coordinate of Raster Scan of Polar-Coordinate-Addressed Memory (4,434,437)
**G. G. Tamer** Television Channel Indicator With Automatic On-Screen Display (4,430,671)
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**Y. Yarnitsky and S. Kaldor** Jig for Machining Stylus Blanks (4,433,794)

**March**

**S. L. Bendell and P. A. Levine** Low Noise CCD Output (4,435,730)
**G. N. Butterwick** Anode Structure for Photomultiplier Tube (4,439,712)
**L. A. Cochran** Dynamic Coring Circuit (4,437,124)
**A. R. Dholakia** Capacitive Playback Stylus (4,439,853)
**A. R. Dholakia** Capacitive Playback Stylus (4,439,855)
**F. C. Farmer, Jr. and D. P. Knight** Drive Level Control System for Testing Kinescopes (4,437,120)
**J. W. Fish** System for Controlling Indicators for Switches (4,437,094)
**W. E. Harlan** Dynamically Controlled Horizontal Peaking System (4,437,123)
**L. A. Harwood and R. L. Shanley 2nd** Television Receiver With Selectively Disabled On-Screen Character Display System (4,435,729)
**W. Hinn and M. B. Knight** Dual-Standard SECAM/PAL Color TV Receiver With Automatic Control of Operating Mode (4,438,451)
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**W. Kern** Structural Defect Detection (4,436,999)
**R. W. Kipp** Radar Ranging System for Use With Sloping Target (4,435,709)
**R. W. Kipp** FM-CW Radar Ranging System With Signal Drift Compensation (4,435,712)
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**M. Kumar and L. C. Upadhyayula** Variable Power Amplifier (4,439,744)
**L. J. Levin** Information Record With a Thick Overcoat (4,435,801)
**P. A. Levine and A. L. Limberg** Electrical Compensation for Misregistration of Striped Color Filter in a Color Imager With Discrete Sampling Elements (4,437,764)
**L. Louik and R. E. Ballard** Apparatus for Molding a Recorded Disc Having a Molded-In Center Hole (4,439,128)
**A. Mattei** Automatically Adaptive Transversal Filter (4,438,521)
**A. Mattei** Phase Locked Loop, as for MPSK Signal Detector (4,439,737)
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**J. J. Prusak and B. P. Patel** Apparatus for Separating a Replica from a Matrix (4,436,603)
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**M. H. Riddle and J. R. Orr** Protection Circuit for Memory Programming System (4,439,804)
**R. L. Shanley 2nd** Adjustable Coring Circuit Permitting Coring Extinction (4,438,454)
**R. W. Shisler and R. E. McVety** Desoldering Tool and Method of Desoldering Leadless Components (4,436,242)
**F. M. Sohn** Color Picture Tube Having Improved Temperature Compensating Support for a Mask-Frame Assembly (4,439,709)
**D. Stavitsky and E. A. Beres** Mold for Recorded Disc (4,437,641)
**I. T. Wacyk** Actively Controlled Input Buffer (4,437,024)
**C. P. Wu** Electromagnetic Radiation Annealing of Semiconductor Material (4,439,245)

## AUTHORS

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He is a founder member of the EOS/ESD Association and Technical Program Chairman for the 1985 EOS/ESD Symposium.

**Carl W. Benyon** graduated in 1962 from Trenton Junior College with the AS degree (cum laude) in Basic Engineering and in 1964 from RCA Institutes with a certificate in Electronics and Transistor Fundamentals. He later took courses in semiconductor device technology, physics, and vacuum technology at Rutgers University and in reliability engineering at RCA. Mr. Benyon joined RCA Laboratories, Princeton, NJ, in 1958 and has been involved in the study of semiconductor device problems including the bonding of leads, damage by bonding techniques, high-temperature contacts, liquid-phase epitaxial growth of semiconductors, radiation hardening of $Al_2O_3$ MIS devices, and advanced techniques in integrated-circuit manufacture. He has also worked on the ion-implantation doping of silicon-on-sapphire films for CMOS circuits and is engaged in reliability studies of SOS devices. Mr. Benyon has been directly involved in work at RCA's manufacturing facilities of the Solid State Division and Consumer Electronics.

Mr. Benyon received RCA Laboratories Outstanding Achievement Awards in 1974 and 1978. He has published several articles in his fields of interest and holds four U.S. patents. He is a member of the IEEE.

**Donald R. Carley** joined RCA after graduation from the University of Michigan with a BS degree in Physics. His first management position at RCA was manager of high-power, high-frequency transistor design. He held positions of increasing management responsibility in high frequency devices until 1971 when he transferred to the integrated circuits activity as Manager of MOS Integrated Circuits Engineering. In this position, he was responsible for all phases of RCA's CMOS engineering activity. In 1975 he became Manager of Application Engineering for Microprocessors where he was responsible for developing RCA's 1800 Series Microprocessor family. In 1978 he was promoted to the position of Manager of RCA's Integrated Circuit activity for Automotive. In December 1980, he was appointed to his present position as Manager of High Reliability Product Engineering for LSI devices.

Mr. Carley has been awarded five patents and has published over twenty papers. He received the 1965 David Sarnoff Individual Award for Outstanding Engineering.

**Richard Denning** received BS and MS degrees in Engineering from the Newark College of Engineering in 1947 and 1952, respectively. He holds the dual responsibilities of Staff Engineer in the Reliability Physics group of RCA Laboratories, Princeton, NJ, and of Manager, Reliability Technology Transfer for Quality Assurance, at RCA's Solid State Division (SSD), Somerville, NJ. He was appointed to these positions in 1980.

Mr. Denning joined SSD in 1956, as a Process and Type Engineer for the manufacture of germanium and silicon transistors. From 1958 to 1963, he held the positions of Engineering Leader, Engineering Manager, and Manufacturing Manager. He also was Program Manager for the Polaris R212 program. In 1964, he joined the Engineering Transistor Design Department where he was responsible for the design and development of high-frequency silicon transistors, high-speed silicon core-driver transistors, MOS devices, and high-voltage deflection transistors for color TV. In 1970, he became Program Manager for the Minute Man III power transistor program, including design, development, and production. In 1972, Mr. Denning was promoted to Manager, Power Transistor Design. He supervised the development of high-voltage ignition and horizontal-deflection transistors, power-switching transistors, epibase p-n-p and n-p-n power transistors, and Darlington devices. In 1975, Mr. Denning became Manager, Advanced Power Engineering, for the Solid State Technology Center at Somerville. He supervised the research and development of new power devices, including thyristors, rectifiers, power MOS transistors, and power monolithic circuits, before being appointed a Staff Engineer at the Laboratories.

In 1984, he shared a David Sarnoff Award for Outstanding Technical Achievement, RCA's highest honor, for his contributions to major reliability improvement in plastic-encapsulated integrated circuits. Mr. Denning has written several technical papers and holds a number of U.S. and foreign patients in the solid-state field. Mr. Dennings is a member of the IEEE.

**M. Patrick Dugan** received BEE and MEE degrees from the University of Detroit in 1969 and 1971 and an MS degree in mechanics and materials science from Rutgers University in 1979. He is currently completing the requirements for a PHD in mechanics and materials science at Rutgers University. Mr. Dugan was employed by the Singer Co. as a Senior Components Engineer in the Consumer Products Division before joining RCA Solid State Technology Center in 1980. Mr. Dugan works in the Quality Control and Reliability Engineering Department, where he is responsible for the complete reliability characterization programs for both bulk CMOS and CMOS/SOS as well as directing device analysis efforts.

He is the author or co-author of six publications and one U.S. patent disclosure.

**Larry J. Gallace,** Director, Product Assurance, Solid State Division, Sommerville, New Jersey, is a graduate of RCA Institutes (1958). He received the Bachelor degree in Mathematics in 1968 and the MS in Applied and Mathematical Statistics in 1971 from Rutgers University. Mr. Gallace joined RCA in August 1958, and has worked predominantly in the area of Reliability Engineering and Product Assurance. Mr. Gallace was a recipient of a 1968 RCA Engineering Achievement Team Award for silicon plastic power transistor engineering. In 1972, he was appointed Manager of the Reliability Engineering Laboratory for all solid state devices, which include integrated circuits and power devices. Since this time, he has been heavily involved in developing test methods for characterizing the reliability of CMOS devices. In 1947, Mr. Gallace was one of the recipients of the David Sarnoff Team Award for his contribution to the development of high-voltage power transistors for automotive ignition and other applications. In 1984, he was part of the David Sarnoff Team Award for improvements in reliability of plastic encapsulated integrated circuits.

Mr. Gallace has published a number of articles on the reliability of silicon devices in addition to teaching courses on reliability engineering methods.

**Leonard Gibbons** received the B.Eng.Sc. Degree in Electrical Engineering from the John Hopkins University in 1959, and the M.S. Degree in Electrical Engineering from Rutgers University in 1963. He joined RCA-Solid State in 1959. He has worked on the design, development, and pilot line assembly of GaAs special products and was the co-recipient of the division's 1962 Engineering Achievement Award. He established and managed the division's first solid-state applications engineering laboratory in Europe from 1969–1974. Since that time, he has managed several marketing and engineering departments including five and one-half years as Manager of the Divisional Reliability Engineering Laboratory. He is now Manager, Long-range Product Planning for standard IC products working on the strategic planning of new products.

Mr. Gibbons is a member of Tau Beta Pi and Eta Kappa Nu.

**Sheldon Gottesfeld** received a B.S. Degree in Mathematics and Statistics from Rutgers University in 1970 and an M.S. Degree in Applied Statistics from Rutgers University in 1975. He joined RCA Solid State Division in 1964 and has worked in the area of reliability characterization and quality control of rf transistors and hybrid devices, optical products, liquid crystal displays, heart pacemaker hybrid circuits, and discrete power devices. More recently, Mr. Gottesfeld has been a Section Manager of the Divisional Reliability Engineering Laboratory working on the reliability of integrated circuits.

**Vincent J. Mancino** graduated from Rutgers University with a BSEE in 1951 and later obtained an MBA from Drexel Institute of Technology. He also completed graduate level and special courses in Electrical Engineering, mathematics, and probability at the University of New Mexico, University of Pennsylvania, and Northeastern University. From 1951 to 1960, he was employed by RCA's Central Engineering group in what is now Government Systems Division, where he was engaged in Electromagnetic Compatibility studies. In 1960 Mr. Mancino joined Cornell-Dubilier, where he became Chief Engineer of the Filter Division and supervised the design and development of electromagnetic suppression components. Mr. Mancino joined RCA Astro-Electronics in 1963, where he is currently Manager of Reliability Engineering and supervises Parts Engineering, Materials Engineering, Failure Analysis, and Reliability Engineering activities and studies.

Mr. Mancino is a Senior Member of the IEEE Reliability and Electromagnetic Compatibility Societies, past Vice-Chairman of the IRE-RFI Technical Committee, past Chairman of the IRE-RFI Transmitter Subcommittee, past Vice Chairman of the Jersey Coast IEEE Reliability/Parts Section, and a Founder of the IRE Professional Group on Radio Frequency Interference, forerunner of the IEEE Electromagnetic Compatibility Society.

**Wesley Morris** received the B.S. degree majoring in Physics and Chemistry from the Florida State University in 1977. He joined the RCA Solid State Division, Palm Beach Gardens, Florida after graduation working on process development of the low-temperature SOS process. He has since worked on various aspects of IC manufacture including photolithography, diffusion, thin films, plasma etching, wet etching, device engineering and process development. In 1983, he received a Technical Excellence Award for his work.

**Robert W. Nearhoof** received his B.A. degree from Penn State University in 1952. He was selected for the RCA Specialized Training Program with the Receiving Tube Division at Harrison, New Jersey. He was permanently assigned to the Engineering Department of the Woodbridge Plant and worked for five years as a manufacturing process engineer. In 1957 he was promoted to Superintendent of Tube Manufacturing and Parts Preparation and served in this capacity until he was appointed Manager of Manufacturing in 1971. In 1974 he assumed the Plant Manager responsibilities for the offshore plant located in Belo Horizonte, Brazil, where he was responsible for Receiving Tube and Picture Tube Assembly Operations. In 1977 he joined the Solid State Division as Director of Operations and Manager of Solid State Manufacturing Operations in Belo Horizonte. In 1980 he returned to Somerville as Program Manager of the Westinghouse Matrix Program assigned to the Hi-Rel LSI Engineering Department. He has been responsible for leadless chip carrier package development and other Hi-Rel Programs.

**Maurice Rosenfield** is Manager of Package Development and Assembly Engineering for Integrated Circuits at the Solid State Division. Mr. Rosenfield, who holds a BSME from Northeastern University, joined the RCA Solid State Division in 1970 as a packaging engineer for the CMOS IC product line. His responsibilities included the package/assembly development of ceramic, frit, and plastic packages. In January of 1975, he was appointed Engineering Leader of the Assembly Technology and Package Development Group within the bipolar-IC product line. In 1978, his responsibilities were expanded to cover packaging and assembly needs for all integrated circuits.

Mr. Rosenfield has been cited in the 1984 David Sarnoff Team Award as a contributor to improved reliability of plastic-encapsulated integrated circuits.

**George L. Schnable** received a BS degree in Chemistry from Albright College in 1950, and MS and PhD degrees in Chemistry from the University of Pennsylvania, in 1951 and 1953, respectively. From 1953 until 1971, he was employed by Philco-Ford Corporation; in 1961 he became Manager of the Advanced Materials and Processes Department in the R&D Operation of the Microelectronics Division. In 1971, Dr. Schnable joined RCA Laboratories, Princeton, NJ, as Head, Process Research, in the Process and Applied Materials Research Laboratory. In 1977, he was named Head, Solid State Process Research. Since 1980, he has been Head, Device Physics and Reliability Research, in the Integrated Circuit Technology Research Laboratory. His research has been concerned with the fabrication technology and reliability of semiconductor devices.

Dr. Schnable holds 29 U.S. patents and has written more than 70 technical papers. He is listed in *American Men and Women of Science*. In both 1979 and 1983, Dr. Schnable received a David Sarnoff Award for Outstanding Technical Achievement. Dr. Schnable is a member of the American Chemical Society, the Electrochemical Society, the Franklin Institute, and Sigma Xi; a Senior member of the American Association for the Advancement of Science and the Institute of Electrical and Electronics Engineers; and a Fellow in the American Institute of Chemists.

**Walter Slusark** received the BA and BS degrees in Electrical Engineering from Rutgers University in 1969. He received the MS and PhD degrees from Rutgers in 1972 and 1976, respectively. Supported by the National Science Foundation, he investigated the optical and structural properties of thin Au-Cr films for his Master's thesis. His PhD dissertation dealt with the dielectric, transport, and switching properties of the transition metal oxide $Nb_2O_5$. Dr. Slusark joined the ITT Electro-Physics Laboratory in 1976 and engaged in the research and development of charge-coupled devices and their application to analog signal processing. In 1977, Dr. Slusark joined RCA Laboratories, Princeton, NJ. He has been concerned with GaAs-FET fabrication technology and its influence on device reliability. He is also responsible for a program of accelerated life testing and failure analysis of GaAs-FET devices at the Microwave Technology Center.

In 1981, Dr. Slusark was a corecipient of an RCA Laboratories Out-

standing Achievement Award for his contribution to the development of a space-qualified, solid-state power amplifier for the Advanced SATCOM satellite. He is the author of several technical publications and is a member of the IEEE, AVS, and Sigma Xi.

**Ronald K. Smeltzer** received a BS degree in Electrical Engineering from Bucknell University in 1964, and MS and PhD degrees in Electrical Engineering from Northwestern University in 1968 and 1970, respectively. As a Post-Doctoral Associate at Southern Methodist University in the Electrical Engineering Department from 1971 to 1972, he was responsible for specific technical activities and the coordination of group efforts in programs to prepare bulk crystals and epitaxial layers of compound semiconductors. In 1972 he was assigned as a Research Associate and Consultant to programs on silicon solar cells and compound semiconductor materials research and device preparation. From 1972 until 1974, as a Member of the Technical Staff at Texas Instruments, Inc., Dr. Smeltzer was Contract Program Manager for the development of the vertical multijunction solar cell. Technical activities in advanced silicon technology included the development of a new selective epitaxial deposition process and orientation-dependent etching techniques. When he was an Assistant Professor at Princeton University, Department of Electrical Engineering, from 1975 to 1978, his responsibilities included both research and teaching duties. His special research interest was new fabrication technologies for compound semiconductor devices. In 1978, he joined RCA Laboratories, Princeton, NJ, as a Member, Technical Staff in the Integrated Circuit Technology Research Laboratory. His activities are focused on process development and device analysis to enhance the radiation tolerance of CMOS circuits.

Dr. Smeltzer has published 17 articles in scientific journals, and is a member of the Electrochemical Society and the New York Microscopical Society.

**Harold S. Veloric** received the BA in Chemistry from the University of Pennsylvania in 1951 and the MS and PhD degrees in Physical Chemistry from the University of Delaware in 1952 and 1954, respectively. Dr. Veloric joined Bell Laboratories in 1954; there he worked on the development of various types of silicon diodes including power rectifiers, voltage-regulator diodes, computer diodes, and solar cells. In 1958 he joined RCA Solid State Division, where he worked on the design and development of high-frequency transistors for consumer and computer applications. In 1960, as Engineering Manager, he was responsible for the design and development of signal and switching transistors and, subsequently, for MOS engineering, device process development, and rf transistor engineering. From 1973 to 1976 he was a Member, Technical Staff, of the Microwave Technology Center at RCA Laboratories, working on technology developments for the microwave group. From 1976 to 1981 Dr. Veloric was Manager of the Materials and Processes Department for the Solid State Division. At present, Dr. Veloric is Program Manager in the Solid State Technology Center. He has authored more than 25 publications and has been awarded several U.S patents. He is a member of the Electrochemical Society and IEEE.