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New Process Technologies for Microelectronics

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New Process Technologies for Microelectronics

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New Process Technologies for Microelectronics

Foreword

Silicon is the touchstone of modern solid state technology, and an amazing diversity of devices and monolithic circuits has been fashioned of this elemental semiconductor. In large measure this variety stems from the *electrical* characteristics of silicon. Of equal importance, silicon is adaptable to a multiplicity of handling and processing techniques because of its unique *chemical* and *physical* properties. Good as present day processes are, improvements are constantly being sought. In fact, the devising and refining of novel methods for processing silicon is a major focus of contemporary solid-state research.

In December 1968, a special issue of the RCA Review devoted to new process technologies for microelectronics appeared. This second issue on the same topic is essentially a "continuation-in-part" that describes a number of additional technologies applicable to silicon processing. The majority of the articles are derived from research carried out in the Process and Applied Materials Research Laboratory of the David Sarnoff Research Center at RCA. Contributions by the Materials Research Laboratory and the Digital Systems Laboratory as well as two from the Solid State Division of RCA round out the issue.

The papers are arranged in the following order. First, a series of five papers dealing with aqueous etching and cleaning techniques for silicon is presented. These include discussions of the contamination of semiconductor surfaces by ionic impurities in common aqueous reagents, and methods of removing these contaminants. Also, the etching of vertical-wall grooves in silicon and the uniform thinning of silicon wafers by chemical etching is described. The next group of four papers involves a variety of techniques for metallizing devices. The processes employed are sputtering-evaporation, chemical vapor deposition, and electroless deposition from aqueous solution; the materials employed are, respectively, aluminum, tungsten, and nickel. The next series of three papers discuss MOS device processing. These include papers on new technology for preparing MOS and MNOS arrays, and recent advances in silicon-on-sapphire device preparation. A group of four articles on process control and defect characterization includes a monitoring technique for improved control of the epitaxial growth of silicon, a new integrating light-flux meter, and methods for

identifying imperfections in silicon and silicon dioxide layers. The issue concludes with two papers on special technologies, one concerns selective electroless plating from aqueous media and the other, a spin-off from silicon processing, describes glass-to-metal seals made possible by the use of a silicon nitride barrier layer.

The processing techniques described in these 19 papers are drawn from the classical disciplines of chemistry, physics, ceramics, metallurgy and electrical engineering. The contributions of each discipline are so commingled, however, that the processes may more aptly be described as derived from materials science. Though trained in one or another of the classical sciences, the authors have acquired broadened perspective by interacting with individuals representing other disciplines. The stimulation resulting from this contact leads to increased ingenuity and imagination in the solution of scientific problems, and is a principal factor in the development of the new technology that continues to revolutionize the electronics industry.

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Process and Materials Applied Research Laboratory

J. A. Amick, Head
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Cleaning Solutions Based on Hydrogen Peroxide for use in Silicon Semiconductor Technology

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Abstract—Hydrogen peroxide solutions at high pH are particularly effective for removing organic contaminants by oxidation; at low pH they are effective for desorbing metal contaminants primarily by complexing. The stability of these mixtures during usage and the effects of hydrogen peroxide depletion on the etching of silicon were measured as functions of resistivity type and doping concentration. These solutions are effective and simple to use, and have wide applications to the cleaning and preparation of silicon device wafers, quartz tubes, and implements employed in semiconductor processing.

1. Introduction

The increased demands on performance and reliability of silicon semiconductor devices and microcircuits in recent years have required the development of improved processing techniques. One key advance in modern solid-state technology is clean processing; contamination of sensitive device surfaces is minimized so that stability and reproducibility of device characteristics are greatly improved.

Hydrogen-peroxide-containing reagents have long been used to clean electron tube components,[1] but their use has not previously been described for the processing of semiconductor devices. The advantages and limitations of hydrogen-peroxide-containing solutions for silicon technology are pointed out, and their efficiency for removing contaminants has been determined by radioactive tracer[2,3] and MOS capacitance measurements.*

* Parts of this work were performed and reported under U. S. Government Contract AD-36-039-SC-86729 (ref. 4).

2. Types, Sources, and Effects of Surface Contaminants

Surface contaminants can be classified broadly as molecular, ionic, or atomic.

Typical molecular contaminants are natural and synthetic waxes, resins, and oils. These are typically present after the mechanical grinding, lapping, and polishing operations of wafers. They may also include grease from fingers and greasy films that are deposited when surfaces are exposed to room air or stored in plastic containers. Photoresists and organic solvent residues also fall into this category. Layers of such molecular impurities in contact with the substrate surface are usually held by weak electrostatic forces. Organic contaminants on silicon devices, especially on surface-sensitive MOS structures, may cause polarization[5] and ionic drift[6] due to the transport of protons.[7] Water-insoluble organic compounds tend to make semiconductor and oxide surfaces hydrophobic, thus preventing the effective removal of adsorbed ionic or metallic impurities. The elimination of molecular contaminants should therefore be considered the first step in a cleaning process.

Ionic contaminants are present after etching of wafers in HF-containing etchants or in caustic solutions, even after extensive rinsing in deionized water.[2] They may deposit on the silicon surface by physical adsorption or by chemisorption. The removal of chemisorbed ions is much more difficult than the removal of ions attached to the surface by physical forces, and a chemical reaction must generally be used to achieve desorption. Of the ionic contaminants, alkali ions are particularly harmful in that they may move under the influence of electric fields or at elevated temperatures, causing inversion layers, surface leakage, drifts during device operation, and other instabilities.[8] In the growth of epitaxial silicon layers, visible ionic and molecular residues from improper cleaning are reported to give rise to twinning, dislocations, stacking faults, and other crystal defects.[9]

Atomic contaminants present on silicon surfaces include heavy metals such as gold, silver, and copper. They originate from acid silicon etchants and are usually plated out in the form of metallic deposits.[3] The removal of this type of contaminant generally requires reactive agents that dissolve the metal and complex the ionic form to prevent redeposition from the solution. Atomic impurities, especially the heavy metals, can seriously affect minority-carrier lifetime, surface conduction, and other device parameters governing stability of the devices.[10-12]

Since a contaminated surface is likely to contain all three types of impurities, it is necessary to first remove the gross organic residues

masking the surface, then the residual organic materials, and finally the residual ionic and atomic contaminants. The gross organic residues from materials used in wafer-polishing operations may be removed by treatment with an organic solvent.*

3. New Cleaning Procedure

Two solutions, used sequentially, have been devised to remove any organic and inorganic contaminants remaining after solvent rinsing. Both solutions contain volatile reagents diluted with pure water. The exact compositions are not critical; some of the work discussed was done using slightly different compositions. However, the recommended compositions afford greater freedom in their application.

The first solution, typically 5-1-1 to 7-2-1 parts by volume of H_2O*-H_2O_2†-NH_4OH‡, was designed to remove organic contaminants that are attacked by both the solvating action of the ammonium hydroxide and the powerful oxidizing action of the peroxide. The ammonium hydroxide also serves to complex some group I and II metals such as Cu, Ag, Ni, Co and Cd.

The second solution consist of H_2O*-H_2O_2†-HCl†† in the typical proportions 6-1-1 to 8-2-1 by volume and was chosen to remove heavy metals and to prevent displacement replating from solution by forming soluble complexes with the resulting ions. The reagents used in these two solutions were chosen over other possible combinations because they are completely volatile. The cleaning action of the dilute HCl-H_2O_2 solution is similar to that of concentrated H_2SO_4-H_2O_2, or that of chromic–sulfuric acid mixtures, but is not as hazardous and presents no disposal problems.

---

* Rinses in hot trichloroethylene are most generally used and yield satisfactory results if overheating is avoided so that thermal decomposition of the solvent is minimized. Triethyl amine is commonly added to trichloroethylene as a stabilizer, i.e., it reacts with the hydrochloric acid formed by thermal decomposition of the solvent. The resultant triethyl amine hydrochloride may remain as a residue on the surface following a rinse in trichloroethylene. As much as 140 mg of residue has been isolated from 1000 ml of a typical batch of electronic grade trichloroethylene. Tetrachloroethylene stabilized with ethyl alcohol does not have this disadvantage and is a more effective degreasing solvent. Hot xylene is one of the most effective degreasing solvents; even halocarbon grease residues are readily removed from silicon wafers. However, it has the disadvantage of being flammable and toxic. Freon fluorocarbon solvents are also satisfactory, especially if vapor degreasing or carefully controlled ultrasonic agitation techniques are employed.

* filtered DI or quartz distilled H_2O

† 30% unstabilized H_2O_2

‡ 27% NH_4OH

†† 37% HCl

The hydrogen peroxide used in the cleaning solutions should be the unstabilized, electronic grade. Stabilized peroxide may contain non-volatile sodium phosphate and sodium stannate or amine derivatives as stabilizers. As mentioned, the compositions are not critical but the solutions of the approximate proportions given above have been found to be reliable, as well as simple to prepare and use.

Cleaning in either mixture is carried out at 75°C to 85°C for time periods of 10 minutes to 20 minutes, followed by a quench and rinse in running DI or quartz distilled water. As a final step, the wafers are "spun" dry and immediately transferred to an enclosure flushed with prefiltered inert gas. *Caution:* As both solutions are vigorous oxidizing agents and can evolve large quantities of gas even when cold, they must be kept in vented containers, or, preferably, mixed just before use.

4. Effectiveness of Contaminant Removal

Mechanically polished and precleaned bare and thermally oxidized silicon wafers were deliberately contaminated with typical organic water-insoluble materials, such as Apiezon wax, stearic acid, etc. They were rinsed with organic solvents and then cleaned with the ammonia–hydrogen peroxide solution only. Water spray tests[13] indicated that less than 1/10 monomolecular layer of hydrophobic organic contaminant remained.

The presence of surface contaminants, including water soluble organic compounds that can not be detected by the water spray test, can be determined by the more sensitive Capacitance-Voltage Bias Temperature Test (CVBT) on Metal-Oxide-Semiconductor (MOS) capacitors.[*,8,14,15] The capacitor is formed by thermally growing a thin oxide layer on a silicon wafer to be tested, then evaporating a metal contact. The CVBT characteristics of the capacitor are measured in an inert atmosphere using a biasing stress of 10^6 V/cm and a bias temperature of 300°C. The lateral displacement of the characteristic CV curve provides a measure of the mobile charge (a shift of 1.0 volt is equivalent to 2.1×10^{11} mobile charges/cm^2 for an SiO_2 thickness of 1000Å). The use of MOS capacitors as detectors for both organic and inorganic contaminants is fully established[7,14,15] by correlation of CV measurements with radiotracer analysis of deliberately contaminated MOS devices. The CVBT method as described was therefore utilized to test the effectiveness of our cleaning procedure for removing deliberately

* For example, Hofstein[7,14] demonstrated by CVBT techniques that contamination of MOS devices with alcohols can cause proton drift instability. Similar drifts caused by other organic contaminants were also observed by CVBT tests.[6]

introduced organic contaminants on MOS devices. These results are summarized in Section 5.

For inorganic contamination studies, silicon wafers and fused quartz samples were immersed in various solutions or etchants containing known quantities of specific ionic impurities "labeled" with radioactive ions of the same type. The quantities of radioactive impurities deposited and the amounts subsequently removed by cleaning treatments were determined by monitoring the radioactivity.[2,3] The efficiency of various acid hydrogen peroxide solutions for removing atomic contaminants including copper, gold, and chromium from silicon wafers and quartz surfaces is illustrated by the desorption curves presented in Figs. 1-4. For comparison, rinse curves for water, diluted hydrogen peroxide without acid, and diluted acid without hydrogen peroxide are also shown. These data were obtained by gamma-radioactivity measurements using Au^{198}, Cu^{64}, and Cr^{51} as radioactive tracers.

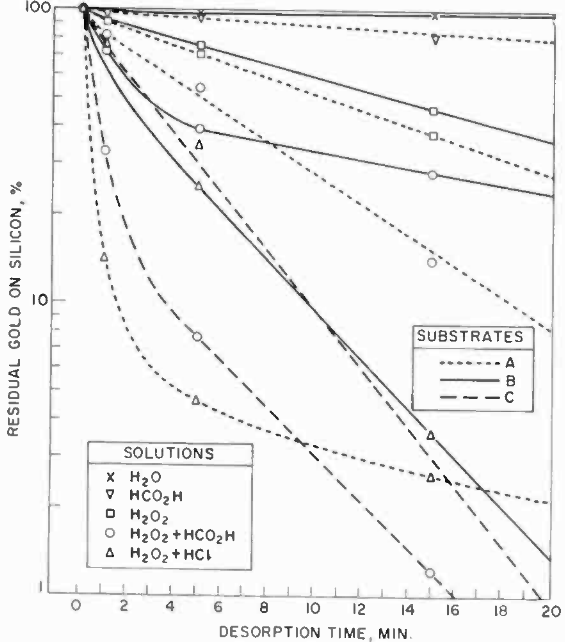
Curve A in Fig. 1 shows the results obtained with silicon wafers that had been etched in a HNO_3-HF mixture containing Au^{198}. The surface concentration on the etched silicon after quenching with deionized water followed by a 30-second water rinse was 7.3×10^{13} Au atoms/cm^2. Desorption at 90°C with an HCl-H_2O_2-H_2O mixture removed 97.4% of the gold in 15 minutes. For comparison, a solution consisting of 1 vol HCO_2H (formic acid),** 1 vol 30% H_2O_2, and 8 vol distilled H_2O removed 86% of the gold in the same time period. Used separately, the reagent components (diluted H_2O_2, diluted HCO_2H, distilled H_2O) removed only negligible quantities of the gold.

Silicon immersed in diluted HF had initially 2×10^{15} Au atoms/cm^2. After 15 minutes desorption in HCl-H_2O_2-H_2O, similar percentages of gold removed were found as for acid-etched silicon (Curve B, Fig. 1). Curve C in Fig. 1 shows the desorption for silicon previously etched in iodine-containing HF-HNO_3 etchant, resulting in an initial gold surface concentration of 3×10^{15} atoms/cm^2. In this case, the formic acid–hydrogen peroxide was more effective (98.8% removal) than the HCl-H_2O_2-H_2O mixture.

Fused quartz contaminated with Au^{198} from HNO_3, HCl, HF, and aqua regia, to an initial surface concentration of 10^{11} to 10^{12} Au atoms/cm^2 was decontaminated effectively with acid H_2O_2. A typical desorption curve is presented in Fig. 2. Similar results were obtained with quartz that had been immersed in the same acids but contained Cu^{64}.

** Formic acid can be used[3] instead of hydrochloric acid to lower the *p*H of the solution to attain metal complexing action; however, this system is generally less effective, partly because of consumption of hydrogen peroxide in the oxidative breakdown of the formic acid.

As seen from Fig. 3, acid hydrogen peroxide is very effective for desorbing copper from silicon. Over 99% is removed within the first 2 minutes of rinsing. Over 30 different desorption treatments involving combinations of complexing, chelating, and oxidizing agents have been tested for copper removal.[3] None was as effective as the acidic hydrogen peroxide. Water or hydrogen peroxide without added acid were quite ineffective.



Substrates:

Curve A (dotted line)—Si etched in $HNO_3 + HF + Au^{198}$; 100% $= 7.3 \times 10^{13}$ Au atoms/cm^2

Curve B (solid line)—Si immersed in 49% $HF + Au^{198}$; 100% $= 2.2 \times 10^{15}$ Au atoms/cm^2

Curve C—(dashed line)—Si etched in $HF + HNO_3 + I_2 + CH_3CO_2H + Au^{198}$; 100% $= 3.0 \times 10^{15}$ Au atoms/cm^2

Solutions:

× Deionized and distilled H_2O, 100°C

▽ 1 vol 90% HCO_2H + 9 vol H_2O, 90°C

□ 1 vol 30% H_2O_2 (unstabilized) + 9 vol H_2O, 90°C

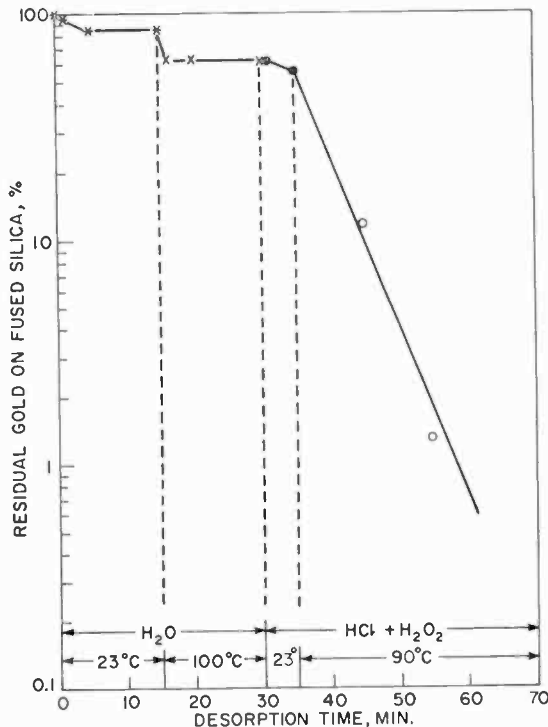
○ 1 vol 30% H_2O_2 + 1 vol 90% HCO_2H + 8 vol H_2O, 90°C

△ 1 vol 30% H_2O_2 + 1 vol 1N HCl + 8 vol H_2O, 90°C

Fig. 1—Desorption efficiency for gold labeled with Au^{198} from silicon surfaces with various solutions at 90°C.

Similar desorption curves for chromium on silicon are presented in Fig. 4. Diluted formic acid-H_2O_2 mixture at 90°C removed 93% of the chromium in 5 minutes. Less dilute solutions were more effective; HCl-H_2O_2 was not tested, but can be expected to be even better because of the high solubility of chromium in HCl.

The desorption of sodium was previously studied with Na^{22} and Na^{24} as tracers for the sodium ions. Aqueous solutions containing HCl were demonstrated to be highly effective in removing physically and chemically adsorbed sodium ions from silicon surfaces.[2]



Substrates:

Fused quartz etched in 49% HF + Au^{198}; 100% = 1.56×10^{12} Au atoms/cm^2

Solutions:

* Deionized distilled H_2O, 23°C

× Deionized and distilled H_2O, 100°C

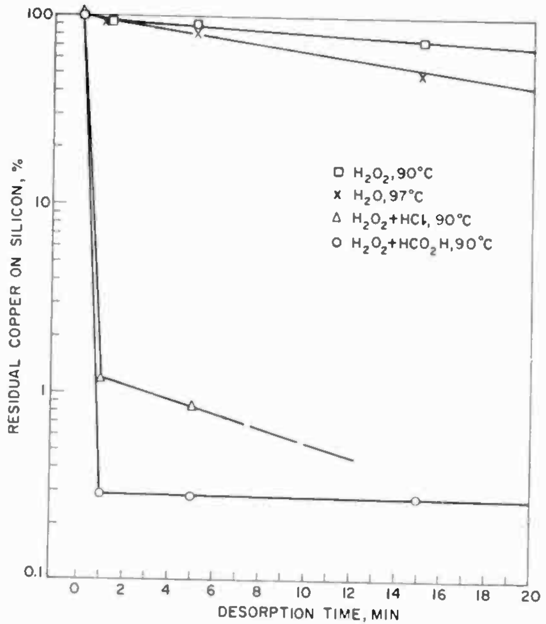
● 1 vol 30% H_2O_2 + 1 vol 1N HCl + 8 vol H_2O, 23°C

○ 1 vol 30% H_2O_2 + 1 vol 1N HCl + 8 vol H_2O, 90°C

Fig. 2—Desorption efficiency for gold labeled with Au^{198} from fused quartz under various conditions.

Considerably higher concentrations of the metals on silicon were used in these desorption studies than are normally present in silicon processing in order to determine the effectiveness of the cleaning mixtures. Although the rates of desorption are different for different metals, the following generalizations can be made on the basis of the results obtained. (1) Each of the single components (H_2O, H_2O_2, HCl, HCO_2H) used separately, regardless of the temperature, is relatively ineffective. (2) Elevated temperatures increase the oxidation potential of the acidic hydrogen peroxide system and the efficiency of desorption.

Radioactive-tracer studies have also demonstrated the importance of the acidic hydrogen peroxide treatment following an oxide removal step in aqueous HF or buffered HF. Heavy metal impurities are re-adsorbed by the silicon where it becomes exposed to these reagents, but can be effectively removed in the acid peroxide medium.



Substrates:

Si immersed in 49% HF + Cu^{64}; 100% = 1.5×10^{17} Cu atoms/cm^2 for □, ×, ○; for △, 100% = 3.3×10^{16} Cu atoms/cm^2

Solutions:

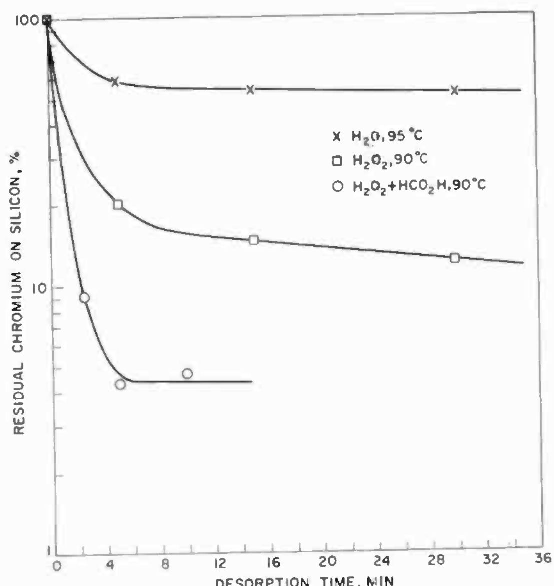
Explanations as for Fig. 1, except that H_2O temperature was 97°C

Fig. 3—Desorption efficiency for copper labeled with Cu^{64} from silicon with various solutions at 90°C.

The behavior of a number of other metals in acidic hydrogen peroxide can be predicted from data in the literature. The following metals are known to dissolve: silver,[16] nickel,[16] cobalt,[17] lead,[18,19] magnesium,[16] niobium,[20] tellurium,[21] and tungsten.[16]

It should be noted that the cleaning solutions are effective for surface contaminants only. If the contaminant is already distributed within an oxide layer, an etch back with dilute HF followed by cleaning in the acidic hydrogen peroxide mixture may be required to remove it. In a more pragmatic sense, silicon wafers that have undergone this cleaning treatment can be used for the routine growth of silicon epitaxial layers free from hillocks, bumps, spikes, etc. Furthermore, vapor-deposited SiO_2 layers deposit uniformly on the wafers, a fact previously correlated with surface cleanliness.[22]

Ellipsometry[23-25] was used to determine the oxide thickness of clean



Substrate:

Si immersed in 49% HF + Cr^{51}; 100% = 2.2×10^{14} Cr atoms/cm^2

Solutions:

Explanations as for Fig. 1 except that H_2O temperature was 95°C.

Fig. 4—Desorption efficiency for chromium labeled with Cr^{51} from silicon at 90°C.

Si surface.* Chemically/mechanically polished (111)-oriented silicon wafers (1-10 ohm-cm p-type) had an initial film thickness of 21 Å. After the cleaning treatment in the ammonia–hydrogen peroxide solution, the film thickness was 18 ± 1 Å; this thickness changed only slightly to 16 ± 1 Å on the subsequent acid-hydrogen peroxide treatment.[26] It can be concluded that no excessive surface oxidation takes place during these cleaning treatments.**

5. Experiments in the Electrical Performance of Devices

The effectiveness of the cleaning procedure was evaluated using MOS capacitors fabricated using these cleaning treatments.

CVBT tests on silicon wafers deliberately contaminated with methanol and cleaned in these solutions prior to metallization showed flat-band voltages and driftable charge levels identical to those of uncontaminated control samples.[27]

A statistical evaluation of MOS capacitors fabricated on reference ingot wafers cleaned with these solutions was also performed using CVBT testing. Over a nine-month test period, a 1100 and a 1200°C furnace was found to result in flat-band shifts arising from driftable charge of (average $\pm 1\sigma$ limit) 0.20 ± 0.07 volt, and 0.18 ± 0.09 volt, respectively.

6. Chemistry of Hydrogen Peroxide Solutions

6.1 General

The chemistry of hydrogen peroxide has been extensively studied.[16,28,29] It is a powerful oxidizing agent in both acidic and basic solutions. Dilute solutions at 50°C are most stable at a pH in the vicinity of 4.5 to 5.0, and are least stable at high pH's, decomposing to water and oxygen. Decomposition is catalized by traces of most heavy metals.

As cleaning agents, hot formic acid and hydrogen peroxide,[1] hot hydrogen peroxide and hydrochloric acid,[13] and cold hydrogen peroxide and ammonium hydroxide[30,31] have been used in a variety of applications. In all of these mixtures, the chemistry is considerably complicated by changes in the reagent concentration with time, and by the complexing nature of both the chloride and ammonium ions. For example, nickel and cobalt each form six different amines;[32] copper and zinc also form amine complexes. The potential–pH diagram shown in

---

* The refractive index of SiO_2 (1.48) was assumed for all films.

** For comparison, immersing the cleaned wafers in HF solution followed by water rinsing reduced the film thickness to 7 ± 1 Å; subsequent boiling for 15 or 30 minutes in deionized and distilled water led to a limiting film thickness of 31 ± 1 Å.[26]

Fig. 5 is thus highly idealized, but it illustrates the relative oxidizing powers of the cleaning solutions at room temperature. The measured *p*H ranges for the alkaline peroxide and acid peroxide solutions described in this paper are indicated.

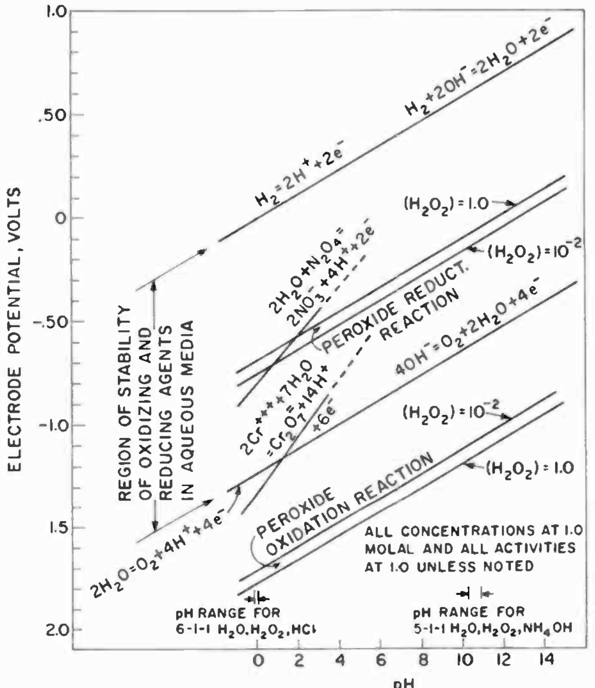


Fig. 5—Potential versus *p*H diagram for hydrogen peroxide solutions at 25°C.

Within the limits of solution stability and peroxide depletion (Section 6.2) the exact concentrations of reagents are not critical. However, if excess peroxide is used, the solutions tend to froth and overflow the container from the too rapid evolution of oxygen.

6.2 Stability of Hydrogen Peroxide Mixtures

These hydrogen peroxide solutions gradually decompose, losing their cleaning effectiveness. Their decomposition rates were determined by titration with a standard potassium permanganate solution. Half-lives of the alkaline and acidic solution[33] at room temperature are, respectively, 11 hours and 50 hours (Fig. 6) ; these half-lives decrease rapidly with increasing temperature. The relative hydrogen peroxide content

of the acidic solution was found to decrease by 98% in 30 minutes, and by 99.95% in 60 minutes, after the solution reached the operating temperature of 80°C.†

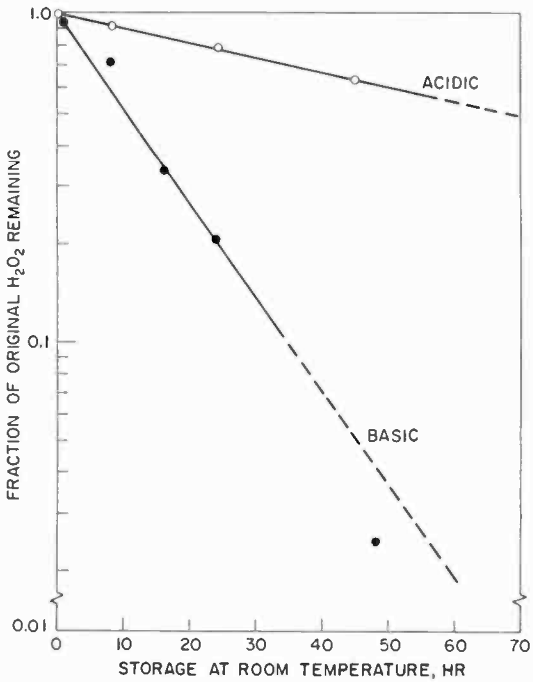


Fig. 6—Rate of decomposition of acidic and alkaline hydrogen peroxide as a function of storage time at 23°C.

To determine more precisely the shape of the decomposition curve during typical processing conditions, the peroxide content in 405 ml of alkaline solution heated in a beaker on a hot plate was monitored. After the beaker was placed on the hotplate the amount of peroxide remaining was determined as a function of time (Fig. 7). The half-life of the solution at 88-90°C was approximately 5 minutes, and the time for the concentration of peroxide to be reduced to the etching threshold* level for (111)-oriented silicon was approximately 40 minutes after the solution reached temperature. Since the recommended cleaning time is 10 to 20 minutes at 75-80°C, there is an adequate margin of safety if the initial peroxide concentration is at the recommended level.

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† It should be realized that the rates of decomposition can be affected by the presence of trace impurities.

* This is the etching threshold under the conditions recommended for cleaning silicon.

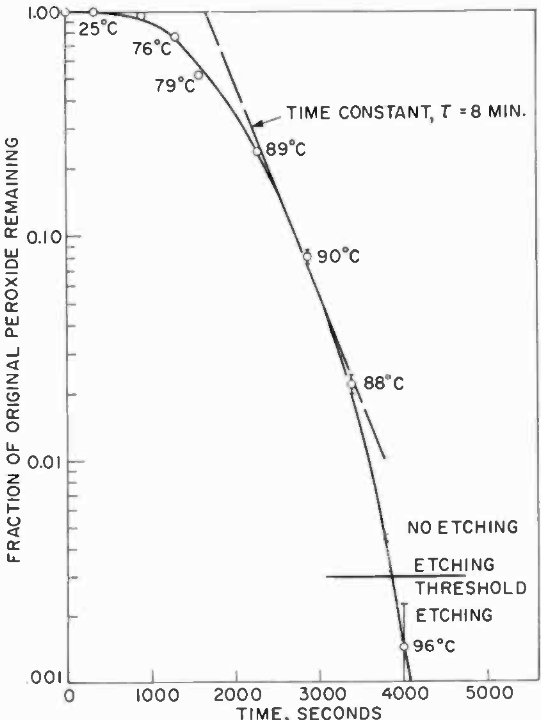

Fig. 7—Fraction of hydrogen peroxide remaining as a function of use time in H_2O_2-NH_4OH-H_2O cleaning solution (etching threshold indicated by horizontal line is for (111) and (100)-oriented silicon; value is approximate).

6.3 Effects of Hydrogen Peroxide Depletion

A bare silicon surface is readily attacked by even a weak base, such as ammonium hydroxide. However, when hydrogen peroxide is present, the surface is immediately passivated, presumably by the formation of a thin (<50 Å) continuous layer of hydrous oxide. This oxide layer is very resistant to chemical attack by ammonium hydroxide at the temperatures and concentrations used for cleaning.*

The etch rate of n- and p-type (111)-oriented chemically polished silicon has been determined in hydrogen-peroxide-free ammonium hydroxide solutions. Resistivity and types used were 0.25 ohm-cm and 20 ohm-cm p-type; 1 ohm-cm and 15 ohm-cm n-type. Etching was conducted in a Pyrex chamber immersed in a constant-temperature bath

* A complete equilibrium potential-pH diagram for the Si-H_2O system is given in Ref. [34].

and capped with a stoppered, water-cooled condenser to minimize loss of ammonia. Wafers were prepared for etching by growing 5000 Å of oxide in steam at 1000°C, by defining and etching a 1-cm-wide stripe along a diameter to expose a bare silicon surface, and by cleaning in H_2O-H_2O_2-NH_4OH solution. Each wafer was then given a 5 second dip in 5% HF, rinsed in distilled water, quartered, and transferred to the etching apparatus. This procedure was adopted to ensure that the

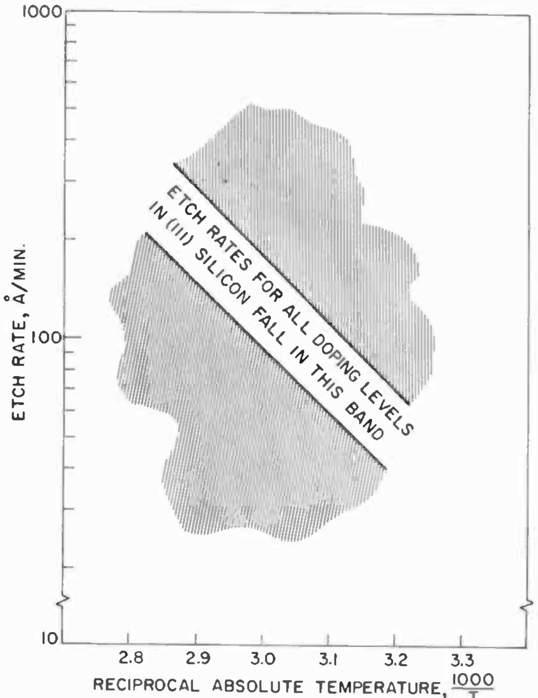

Fig. 8—Etch rate of (111)-oriented silicon in ammonium hydroxide solutions as a function of temperature.

bare silicon surface was covered by no more than a thin film of freshly formed hydrous oxide when the wafer quarters were placed in the etching solution. The samples were removed from the etch at prescribed time intervals and the oxide was stripped in buffered HF etch.

The depth of step formed in the silicon as a result of localized etching was measured with a Talysurf** surface profilemeter with an accuracy of better than ±2%. This technique was also used to deter-

** Talysurf Model 4, Rank Taylor Hobson, Leicester, England.

mine the thickness of the oxide films by measuring the step height formed from the top of the film to the substrate surface.

The observed etch rate values for 2N to 6N NH_4OH solutions fall into the broad band shown in Fig. 8 where the etch rate is plotted as a function of reciprocal temperature. Despite the precautions used to obtain an oxide-free surface, plots of step height versus time showed considerable scatter even on the four quadrants of the same wafer. These results may indicate that the oxide formed at room temperature offers some barrier to the attack of ammonium hydroxide on silicon, or that the chemical polishing had not completely removed the work-damaged surface and that the etch-rate variations reflect this. Within the limits of the experiment, there was no difference between the etch rates of n- and p-type silicon. There was no discernable etching of the oxide mask at any concentration or temperature used in this experiment. It should be noted that ammonium hydroxide etching of silicon is orientation sensitive; (100)-oriented material etches more rapidly than (111)-oriented material. As expected, no silicon etching effects have been observed in aqueous HCl or in the acidic peroxide solution.

6.4 Effects Of Fluoride Ion Additive

A common semiconductor processing operation is to either completely strip the surface oxide or to conduct limited etch-back in HF or buffered HF. A large number of fluoride ions are adsorbed during this kind of treatment.[2] If rinsing is inadequate, these fluoride ions could transfer to the ammoniacal cleaning solution producing a silicon etch.[35] As an extreme test of this type of contamination, the etch rates of both n- and p-type (111)-oriented epitaxial silicon in H_2O-NH_4F-H_2O_2 solutions were determined over a five-decade range in fluoride ion concentration. The solutions were prepared by adding aliquot amounts of aqueous ammonium fluoride solution (40% NH_4F by weight) to 5 ml of 30% unstabilized H_2O_2 and diluting with distilled water to a total volume of 30 ml. Each test solution was preheated on a hotplate for five minutes to bring the temperature to 75 ± 2°C, the wafer was added, and heating continued for 10 minutes to a final temperature of 80°C. The wafer preparation procedure was similar to that described in the previous section except that the HF dip was omitted. The thickness of the remaining oxide was measured, the oxide was then stripped in buffered etch, and the silicon etch-step height was measured on the Talysurf.

The observed variation of silicon and silicon dioxide etch rate with fluoride ion concentration are shown in Figs. 9 and 10. The silicon etch-rate curve has two distinct regions, one for low fluoride ion con-

centration and one at higher concentrations where the etch rate increases quite rapidly with increasing fluoride ion concentration. While the different regions are of considerable interest in the interpretation of the etching mechanism, the immediate practical significance of this curve is that peroxide solutions containing fluoride ion concentration

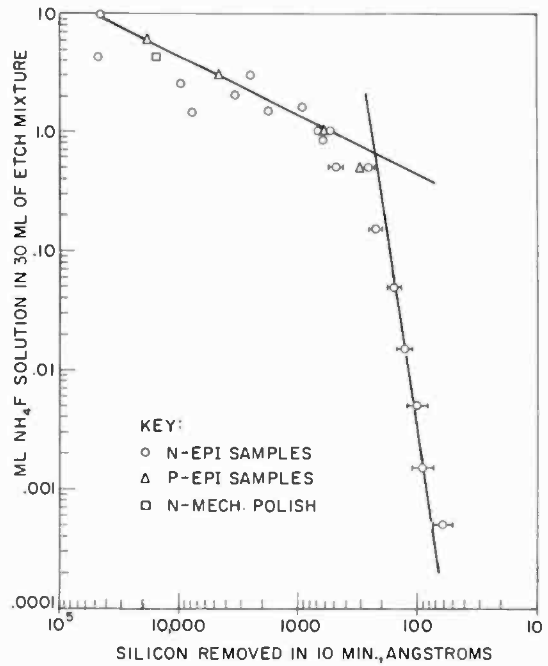

Fig. 9—Etch rate of (111)-oriented silicon in ammonium fluoride solutions (solution composition: 5 ml 30% H_2O_2, aliquot 40 wt % NH_4F solution, diluted with H_2O to total volume of 30 ml).

at the level that might be found by casual contamination during normal handling and processing have very low etch rates. This means that trace contamination of the H_2O_2-NH_4OH cleaning solutions with fluoride ion will not be a cause of etching of (111) oriented silicon wafers. A similar conclusion applies to (100) wafers. It follows that any fluoride ion that might be leached out of Teflon workholders will not cause any significant amount of etching. The oxide etch rate becomes appreciable only at the highest fluoride concentrations and is essentially zero at concentrations below 0.1 ml NH_4F per 30 ml solution.

A feature of both the ammonium hydroxide and the ammonium fluoride-hydrogen-peroxide solutions is that, although physically iso-

lated samples of n-type and p-type (111) oriented silicon will etch at nearly the same rate, adjacent n and p regions will etch at different rates. This differential etch rate may be illustrated by the change in relative heights shown in Fig. 11. This figure shows the surface levels before and after a 10-minute etch at 80°C in a 5-1 H_2O_2-NH_4OH solution; in Fig. 12 levels for treatment in 5-1-1 H_2O-H_2O_2-NH_4F solution are displayed.

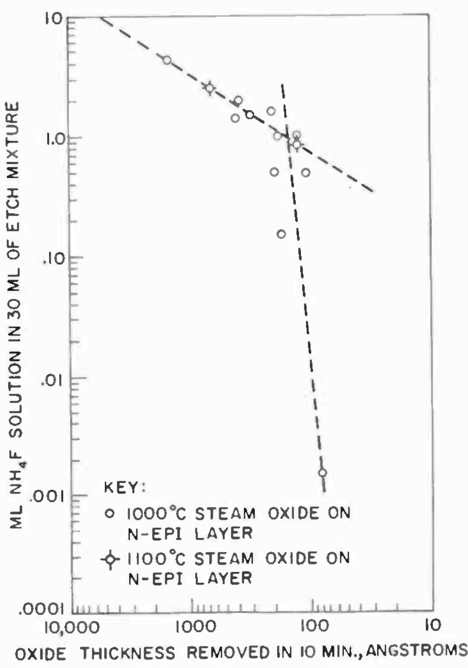

Fig. 10—Etch rate of thermally grown silicon dioxide in ammonium fluoride solutions (solution composition: same as for Fig. 9).

7. Summary and Conclusions

Two sequential cleaning solutions (H_2O-H_2O_2-NH_4OH, and H_2O-H_2O_2-HCl) have been devised for cleaning silicon surfaces to reduce organic and inorganic contaminants to the very low levels required for silicon device fabrication.

The solutions do not attack either silicon or silicon dioxide as long as sufficient hydrogen peroxide is present. If the hydrogen peroxide is depleted or if gross fluoride ion contamination is present, etching can occur.

The hydrogen peroxide depletion rate and the concentration de-

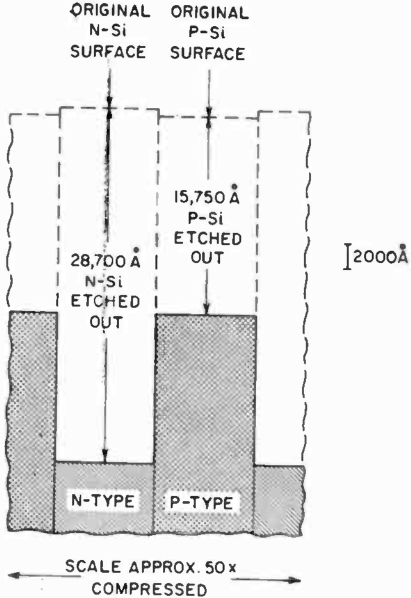

Fig. 11—Surface profiles of n- and p-type silicon regions before and after etching in ammonium hydroxide (conditions: 1 vol 27% NH_4OH + 5 vol H_2O, 10 min at 80°C).

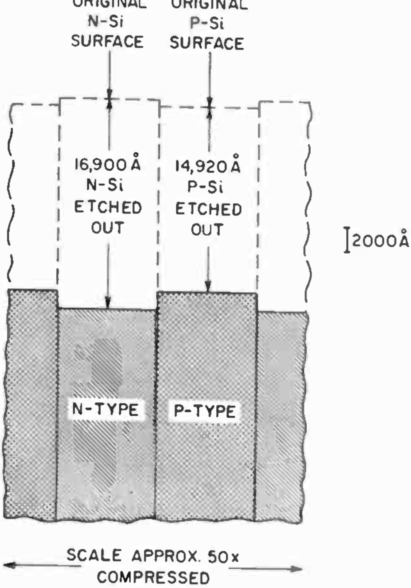

Fig. 12—Surface profiles of n- and p-type silicon regions before and after etching in fluoride hydrogen peroxide etch (conditions: 1 vol 40 wt % NH_4F + 1 vol 30% H_2O_2 + 5 vol H_2O, 10 min at 80°C).

pendence of the silicon etch rate in depleted hydrogen peroxide solutions or in fluoride ion contaminated solutions have been determined and found safe for the recommended cleaning conditions.

The chemical effectiveness of these solutions has been demonstrated by water spray tests and radiotracer analyses. Moreover, the ability of the cleaning procedure to remove electrically active impurities has been verified using CVBT measurements on MOS capacitors.

Acknowledgments

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Radiochemical Study of Semiconductor Surface Contamination

I. Adsorption of Reagent Components

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Abstract—The adsorption of reagent components on semiconductor surfaces was measured by radioactive tracer methods to assess the extent of surface contamination from typical reagent solutions used in solid-state-device processing. Substrates used were primarily silicon and germanium. Reagent solutions include NaOH, HF, HCl, HF-HNO_3-CH_3CO_2H mixtures, iodine-containing semiconductor etchants, and chromic-sulfuric acid. Radionuclides used as tracer ions are Na^{22}, Na^{24}, F^{18}, Cl^{38}, and I^{131}.

Adsorption of Na^+ ions by Si slices from dilute NaOH at 25°C was predominantly physical, Si increasing slowly with increasing NaOH concentration. In 0.1% NaOH, adsorption equilibrium was established in 1 hour, leading to 4×10^{13} Na^+/cm^2. An initial 60-second rinsing treatment in cold H_2O removed 63%, but continued rinsing desorbed Na^+ at decreasing rates. Hot water desorbed 99.5% within 2 minutes, lowering the surface concentration to below 0.004 monoionic layer.

Etching of Si wafers in 5% NaOH at 100°C led to 1×10^{14} Na^+/cm^2. Desorption with HCl reduced this layer to less than 0.0002 of one monolayer of Na^+ ions. In contrast to thermal SiO_2, pyrolytic SiO_2 sorbed large quantities of Na^+, probably due to its porous nature. On immersing in diluted HF, Si and Ge wafers adsorbed on the order of 10^{16} to 10^{17} F^-/cm^2. The major portion was desorbable by rinsing with cold water, but a fluoride residue of several monolayers remained. Fluoride in Si volatilized only partly at 1250°C. Etching of Si and Ge wafers in strong HF-containing etchants led to concentrations in the 10^{16} F^-/cm^2 range. Desorption of etched and water-rinsed wafers with acetone was extremely effective, reducing the adsorbate to a residual concentration of 10^{14} F^-/cm^2 in 30 seconds. Si etched in hot NaOH followed by immersion in dilute radioactive HCl adsorbed 1×10^{14} Cl^-/cm^2. Ge immersed directly in the HCl acquired 3×10^{14} Cl^-/cm^2. Metal surfaces adsorbed larger quantities, especially indium (10^{17} Cl^-/cm^2). Iodine from CP-4 type etch mixture contaminated both Si and Ge surfaces with 10^{13} to 10^{14} I_2 molecules/cm². The adsorbate on Ge could be desorbed readily with aqueous solutions, but Si required hot EDTA solution to lower the residue to 3% of the initial value in 5 minutes. A special etch containing only 1.9 mg/liter NaI led to uniformly adsorbed 10^{11} I_2/cm^2 on Si and 10^{12} I_2/cm^2 on Ge. Iodide ions from 1N NaI led to 10^{14} I^- ions/cm² Si or SiO_2. Treatments of Si in hot chromic-sulfuric acid, followed by cold water rinsing, resulted in absorbed chromium concentrations of less than 10^{14} atoms/cm².

1. Introduction

The electrical properties and the stability of semiconductor devices are strongly influenced by contaminants inadvertently introduced during the many processing steps required to fabricate the devices. Contaminants can originate from many sources—organic residues from photoresist polymers and solvents, gases or vapors from the ambient, and anions or cations from etch and rinse solutions. Of these contaminants inorganic ions are particularly detrimental to semiconductor devices.

The contamination of the semiconductor or oxide surfaces usually occurs as a result of physical or chemical adsorption, by electrolytic action, or by exchange of surface atoms with impurity ions in the solution. Some of the impurities deposited on the surface may be removed by suitable desorption treatments. Heating of oxide-coated semiconductor wafers at high temperatures during subsequent processing may cause diffusion of residual impurities to the oxide semiconductor interface. The extremely high fields that exist at p-n junctions during operation of the finished device can also give rise to surface migration of ionic impurities. The effects of these contaminants may become manifest in uncontrolled drifts of the semiconductor surface potential, changes in the minority-carrier lifetime at the surface, surface recombination velocity, and the formation of inversion or accumulation layers. These effects can lead to increased and erratic reverse leakage current in devices.

The effects on device performance of the following fast-diffusing contaminants have been studied extensively: gold,[1,2] copper,[1,3-5] iron,[1,5] manganese,[1,6] and sodium.[7-9]

Of the papers published concerning surface contamination from inorganic solutions, few discuss the situation under actual conditions of semiconductor device processing. Holmes and Newman employed electron diffraction to examine deposits on silicon and germanium surfaces etched in solutions to which various metals had been added.[10] Neutron-activation analysis was employed by Bemski and Struthers[11] and by Carlson[12] to detect gold on silicon. Several groups of workers determined sodium concentrations in silicon and silicon dioxide films by neutron-activation and radio-tracer techniques.[9,13-18] Radioactive tracers were also used by Larrabee[19] for measuring cationic impurity adsorption from solution on silicon surfaces, by Krembs and Schlacter[20] on germanium, and by Fowkes et al. on silicon dioxide films.[21] Adsorption of halide ions by germanium,[22] silicon,[23,24] and silicon dioxide[24] surfaces has also been measured by tracer methods.

Contamination studies with compound semiconductors have been

reported by Larrabee[25] who employed radiotracers in solutions, and by Kern[26] who investigated contamination of gallium arsenide from quartz crucibles during synthesis by means of neutron activation and gamma-ray spectrometry.

Radiochemical contamination studies with metal components on which transistors are mounted were published in a previous paper.[27] The results of the present work will therefore be confined primarily to semiconductor surfaces to assess surface contamination from solutions under conditions frequently encountered during device processing. This paper, Part I, describes contamination from reagent components; Parts II‡ and III*, will discuss contamination from trace impurities. Both acid and alkaline etch solutions of typical composition but "tagged" with radioactive tracers were used to measure the extent of deposition on the sample surfaces. Desorption data were analyzed to determine the mechanism and reversibility of impurity deposition.

2. Experimental Methods

2.1 Semiconductor and Silica Substrates

Variously doped silicon and germanium wafers cut from (111)-oriented single crystals were used. In a few instances, hyperpure silicon powder*** was used to increase the surface area, thus enhancing the analystical sensitivity. The wafers were either lapped, mechanically polished, or chemically polish-etched, as indicated in the tables. Before use, the wafers were degreased with hot organic solvents, nonionic surfactant solution, and finally rinsed with deionized and distilled water. Thermally grown or chemical-vapor-deposited silicon dioxide films, as well as plates of natural fused quartz** were also used. Impurity concentrations in the latter were published previously.[26]

2.2 Preparation of Radioactive Reagent Solutions

Pertinent nuclear data[28] of the radionuclides used as tracers are summarized in Table I. The isotopes and reagent solutions were prepared as follows:

Dilute radioactive sodium hydroxide containing Na^{22} was prepared in our laboratory from carrier-free $Na^{22}Cl$ in HCl solution.† Curie-

‡ RCA Review, Vol. 31, p. 234, June 1970.
* To be published in September 1970 issue of RCA Review.
*** Pigment Dept., E. I. DuPont de Nemours and Co. (Inc.), Wilmington 98, Del.
** Vitreosil, Trademark of Thermal American Fused Quartz Company.
† NSEC (Nuclear Science and Engineering Corporation, Pittsburgh, Pa.).

Table I—Pertinent Properties of the Radioactive Isotopes Used as Tracers

Isotope	Lifetime	Modes of Decay	Decay Energy (MeV)	Principle Radiations			
				Particle Energies (MeV)	Particle Intensities	Gamma Energies (KeV)	Gamma Intensities
$_{11}Na^{22}$	2.602 y	$\beta+$, EC	2.84*	0.54* EC*	89%* 11%*	AR 1275	99%*
$_{11}Na^{24}$	15.0 hr	$\beta-$	5.51	1.389	99 + %	1369 2754	100% 100%
$_{9}F^{18}$	109.7 min	$\beta+$, EC	1.65	0.635 EC	97% 3%	AR	
$_{17}Cl^{38}$	37.3 min	$\beta-$	4.91	4.81 2.77 1.11	53% 16% 31%	1600 2168	85** 100
$_{53}I^{131}$	8.070 d	$\beta-$	0.970	0.333 0.606	6.9% 90.4%	284 364 637	5.9% 79% 6.7%

Data compiled from Ref. [28], except * which are from the 45th Edition (1964).
Notes:

$\beta-$ = Negative beta emission
$\beta+$ = Positron emission
EC = Orbital electron capture
AR = 511 KeV photon associated with the annihilation of positrons in matter
** = Relative intensity
y = Year
d = Day

level quantities of radio sodium were prepared†† by thermal neutron activation of sodium hydroxide pellets by an ion-exchange treatment at a thermal neutron flux of 2.5×10^{13} n/cm² sec. The resulting $Na^{24}OH$ permitted the use of high specific radioactivities (curies per gram of sodium) with consequent increase in the analytical detection limit. Fluorine-18, prepared by reactions discussed previously,[27] was obtained in ionic form# in 0.1N NaOH with chloride ions as non-isotopic carrier. The prepurified solution was further refined by neutralizing with HF, concentrating by distillation, and passing through a Dowex-50 W-X8 cation exchange column in the H^+ form to remove the sodium ions. The eluate was then mixed with appropriate quantities of 49% HF. Chlorine-38 was prepared by thermal neutron activation of pure calcium chloride.* $CaCl_2$ was chosen as target material because no interfering gamma radioactivity is generated from either the calcium or the chlorine by the thermal (n, p) activation, or by possible fast neutron reactions; 100 mC Cl^{38} activity was generated and converted to 0.2N HCl by passing the radioactive $CaCl_2^{38}$ solution through a Dowex cation exchange column in the H^+ form. Iodine-131 was obtained as carrier-free, high-purity NaI^{131} solution.† Aliquots of the solution were added to standard iodine etch mixtures, yielding molecular iodine of the same chemical form as the normal iodine present in the etchants.

2.3 Sample Exposures

The substrates were immersed in the radioactive reagents in polyethylene beakers, usually with slight agitation. In the case of the acid etch mixtures, the nominal temperature is the starting temperature, but the exothermic etching reactions usually increased the temperature by several degrees during use. Samples were withdrawn from the etch bath with plastic-coated tweezers, except when etching in mixtures containing HF and HNO_3; here the etching was always terminated by rapidly diluting with deionized water.

2.4 Initial Rinsing of Samples

Following removal of the wafers from the etch bath, a series of water rinses was applied to remove droplets of radioactive etch solution that

†† RCA nuclear reactor facilities at Industrial Reactor Laboratories, Inc., Plainsborough, N. J.

Brookhaven National Laboratories, Upton, N. Y.

* RCA nuclear reactor facilities at Industrial Reactor Laboratories, Inc., Plainsborough, N. J.

† Oakridge National Laboratory, Oakridge, Tenn.

by the water rinses (minus drag-out) was 742 cpm, or 63% of the total Na+ initially present.

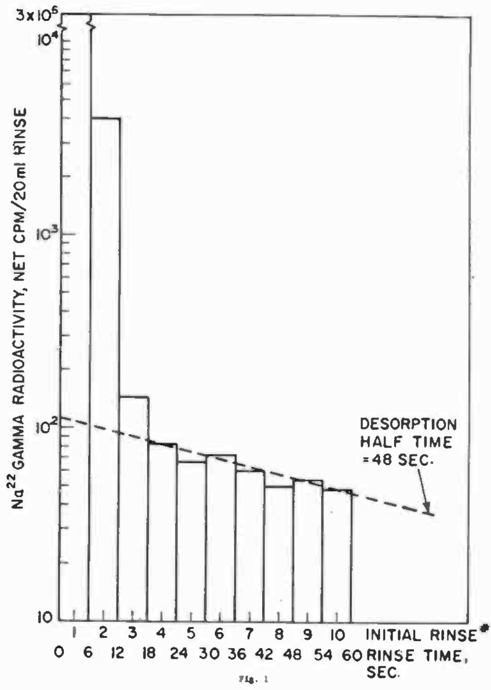

Fig. 1—Sodium-22 radioactivity in initial water rinses from $Na^{22}OH$-treated silicon. 20 ml deionized H_2O per 6-second-rinse from lapped silicon wafers that had been immersed in 0.03N $Na^{22}OH$ at 25°C. Desorption half-time = 48 sec.

The initial concentrations of Na+ adsorbed from 0.03N NaOH as a function of immersion time were measured by the above technique. The results, shown graphically in Fig. 2, indicate that adsorption equilibrium of 3.8×10^{13} Na^+/cm^2 is attained in approximately 1 hour. Na+ adsorption on mechanically polished* wafers with a mirror-like surface finish was only 30% lower than on lapped wafers, indicating that the true surface area of lapped wafers is reasonably close to their geometric area, as used in these calculations.

A limited number of data was obtained relating Na+ adsorption at 25°C to the NaOH concentration over the range 0.003 to 6N. The relation was found to follow a Freundlich-type adsorption isotherm. The quantity of adsorbed Na+ after the initial 60-second rinse sequence in-

* Polished with Linde Type A-5175 abrasive powder and felt wheel.

creased approximately 2½-fold for a 10-fold increase in the NaOH concentration.

Desorption with water beyond the initial 60 seconds of rinsing continued to decrease the Na^+ surface concentration rather rapidly, as seen from the typical desorption curves in Fig. 3. Water at 100°C was particularly effective, decreasing the initial concentration 200-fold within 2 minutes to a residual Na^+ quantity corresponding to 0.004 monoionic layer. The ease of removal of Na^+ from silicon indicates predominantly physical adsorption.**

Similarly, 6N (19%) HCl also removes Na^+ from a recently immersed surface at a much higher rate, as shown in the next section.

The importance of rinsing samples immediately following an etching treatment was demonstrated by the following experiment. Two

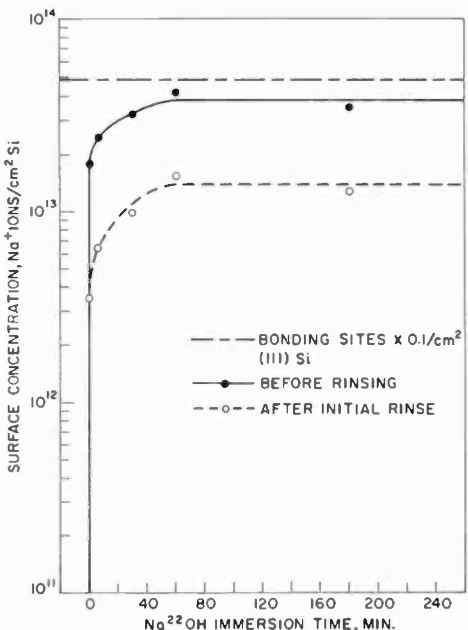

Fig. 2—Adsorption of Na^+ Ions on silicon from 0.03N $Na^{22}OH$ at 25°C as a function of immersion time. Upper curve shows adsorbed Na^+ prior to rinsing. Lower curve shows adsorbed Na^+ after 60 sec initial water rinse sequence.

** Since the substrate surface is covered with a thin layer of natural oxide, which in the presence of water will hydrate forming silanol groups ($\sim 8 \times 10^{14}$ Si-OH/cm²),[29] it can be expected that physical adsorption takes place primarily by electrostatic attraction of Na^+ and Na^+OH^- ions to the electrically charged hydroxylated silicon surface forming an ionic double layer structure.

silicon wafers were immersed in 0.04N NaOH followed by the initial 60-second rinse sequence, but they were then stored in room air for several weeks before continuing the desorption with 100°C-water or with 6N HCl (Fig. 3). This resulted in a considerably lowered desorption rate compared to samples that were stored for less than 24 hours, probably due to the growth of a surface oxide that tends to trap impurity ions.

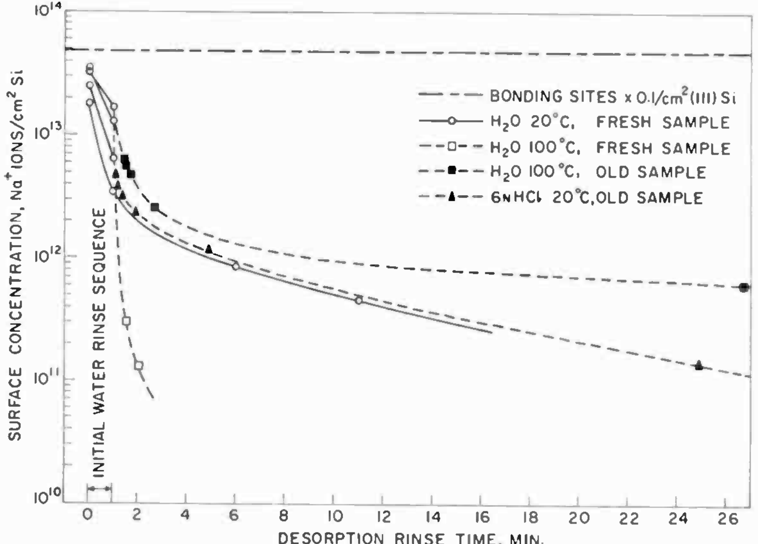

Fig. 3—Desorption of Na+ Ions from silicon with H_2O and HCl. Silicon wafers that had been immersed in 0.025N $Na^{22}OH$ followed by immediate initial rinsing in H_2O for 60 sec. Some samples (open symbols) were then desorption-treated as indicated within 24 hr. Other samples (solid symbols) were desorption-treated after several weeks of storage leading to inhibited desorption.

3.1.2 *Adsorption of Na+ Ions on Silicon from $Na^{24}OH$ at 100°C*

To assess sodium contamination during actual post-mount etching of silicon power transistors, various types of silicon wafers were prepared to simulate different doping and surface conditions. The wafers were etched for 60 seconds in 1.25N (5.0%) $Na^{24}OH$ at 95-100°C, followed by one of two special initial rinse treatments. These had been designed to simulate typical transistor processing conditions and to allow manipulation of the samples by remote control in the radiation hot cell. Initial rinse treatment "A" consisted of 3 immersions in cold deionized water for a total of 17 seconds in 330 ml per wafer to remove

all of the "drag-out" from the etch bath without appreciably lowering the adsorbed Na^+. In the alternative treatment "B", the etched wafers were immersed in 6N (19%) HCl for 15 seconds, using 60 ml per wafer; this was followed by 3 rinses in cold deionized water for a total of 15 seconds in 400 ml per wafer. All wafers were given a final dip in acetone to speed up drying in air. At this stage, the wafers were scanned with a Geiger–Mueller microprobe radiation detector that was connected to a counting rate meter to locate spots of high radioactivity. These sometimes occurred near the edge where the wafer was being held by the tweezers during the remote handling operations. Contaminated areas were carefully removed by scribing and breaking before accurate radioactivity measurement of the adsorbed Na^{24} commenced. The results are summarized in Table II.

The adsorbed Na^+ concentrations of the water-rinsed series ("A") are 5 times lower on the heat-treated silicon wafers (3.4×10^{13} Na^+/cm^2) than on all the others, which average 1.57×10^{14} Na^+/cm^2. The doping type, resistivity, and surface finish have no major influence on the quantity of Na^+ adsorbed.

Several additional etching and desorption experiments were conducted. Extending the etch time in the hot NaOH solution from 1 to 6 minutes did not increase the quantity of adsorbed Na^+ markedly, indicating that steady-state condition is established within the first minute of etching in hot caustic. This is reasonable, since silicon surface layers are continuously being removed by etching according to the equation

$$Si + 2NaOH + H_2O \rightarrow Na_2SiO_3 + 2H_2.$$

The initially water-rinsed silicon wafers were subjected to continued rinsing. Deionized water was used at a ratio of 1000 ml per wafer at a temperature of 20°C for rinse periods of 40 minutes. This additional water rinse descreased the Na^+ surface concentration listed in Table II to residual levels of about 10% of the value after the first water rinse ("A"). The sodium adsorbed on phosphorous-doped silicon required the entire 40 minutes of rinsing before it approached this concentration, whereas on boron-doped silicon this level was reached within 10 minutes. Representative desorption curves for each type are shown in Fig. 4. From this observation it appears that a phosphorus-doped silicon surface retains Na^+ more tenaciously than does one doped with boron.

The mean concentration on the initially acid-rinsed series ("B") was considerably lower: 6.5×10^{12} Na^+/cm^2. The average deviation

Table II—Adsorption of Sodium Ions on Silicon from Hot Sodium Hydroxide Solution (Na^{24} Used as Radioactive Tracer)

Adsorbent Wafer				Adsorbate	
Dopant	Resistivity Type	Resistivity (ohm-cm)	Preparation	Na+ ions/cm² after H_2O Initial Rinse "A"	Na+ ions/cm² after HCl Initial Rinse "B"
B	p	6.5-7.1	Lapped	2.68×10^{14}*	
B	p	6.5-7.1	Mechanically Polished	1.38×10^{14}**	1.00×10^{13}
B	p	6.5-7.1	Chemically etch-polished	1.83×10^{14}	0.62×10^{13}
B	p	6.5-7.1	Chemically etch-polished and heated 21 hr at 1300°C; HF etched	0.38×10^{14}	0.21×10^{13}
B	p	30†	Chemically etch-polished and boron diffused 21 hr at 1300°C; HF etched	0.36×10^{14}	0.55×10^{13}
P	n	0.12†	Chemically etch-polished and phosphorus diffused 30 min at 1200°C; HF etched	0.29×10^{14}	0.83×10^{13}
B	p	154	Lapped	0.78×10^{14}	
P	n	1.3-3.5	Lapped	0.59×10^{14}	0.55×10^{13}
P	n	1.3-3.5	Mechanically polished	$\sim 1.8 \times 10^{14}$	0.81×10^{13}

* Average of 4 analyses, mean error $\pm 0.78 \times 10^{14}$

** Average of 3 analyses, mean error $\pm 0.19 \times 10^{14}$

† Value in ohms/square.

Etching: 1 min in 1.25N (5.0%) NaOH at 95-100°C

Initial Rinsing "A": 3 immersions in deionized water at 20°C for a total of 17 sec and a total of 330 ml per wafer.

Initial Rinsing "B": 1 immersion in 6N (19%) HCl at 20°C for 15 sec, 60 ml per wafer, followed by 3 immersions in deionized water at 20°C for a total of 15 sec and 400 ml per wafer.

from this mean was only ±15%, regardless of the type of silicon surface. The individual values were up to 30 times lower than on the corresponding water-rinsed samples, which demonstrates the excellent efficiency of aqueous HCl for desorbing Na+ ions from silicon.

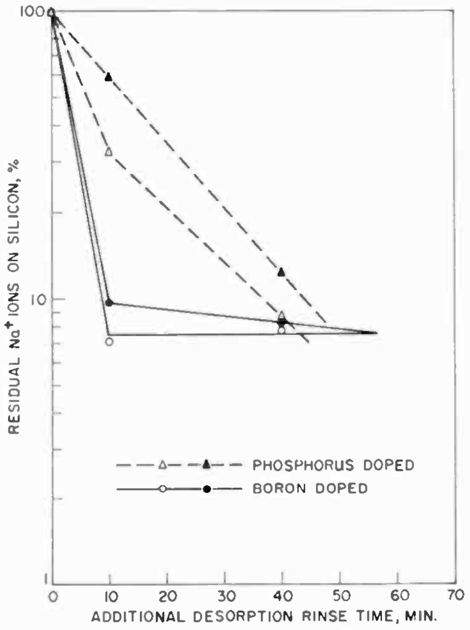

Fig. 4—Desorption of Na+ Ions from n-Type and p-Type Silicon with H_2O Phosphorus and boron doped wafers etched in 1N $Na^{24}OH$ at 100°C. Initially rinsed with H_2O (Table II); desorption rinsed with deionized H_2O, 20°C; 100% value = Na+ surface concentration after initial water rinse.

It was readily possible to lower the residual Na+ concentrations on the HCl-rinsed silicon wafers (Table II) still further by continued desorption treatment. A 5-minute immersion in an ultrasonically agitated water bath at 40°C lowered the Na+ levels on the average nearly 10-fold to 8×10^{11} Na+/cm². Alternatively, extending the HCl rinsing from 15 seconds to 2 minutes was even more effective, and resulted in a residual Na+ concentration below 5×10^{11} Na+/cm²; this quantity represents less than 0.00014 monoionic layer of Na+. While this is indeed a small quantity of contaminant, it must be remembered that the resulting electronic effects can be significant. Attalla et al.[30] reported that 1/10,000th of one monolayer of ionic impurity is capable of inverting the surface of 1 ohm-cm silicon. The desorption treatments should therefore be as exhaustive as practically feasible.

The desorption behavior suggests that the major portion of the sodium from hot NaOH is reversibly absorbed by electrostatic forces as noted in Section 3.1.1 for cold NaOH. However, a few percent appears to be strongly chemisorbed, requiring HCl or boiling H_2O for desorption. It is proposed that the chemisorption of sodium ions proceeds by exchange with the proton of the silanol group forming a ≡Si-O-Na surface.

3.1.3 *Adsorption of Na^+ Ions on Silicon Dioxide from $Na^{22}OH$ at 100°C*

A comparative adsorption experiment with SiO_2-coated silicon wafers was conducted by immersing the samples for 1 minute in NaOH (0.7N) at 100°C, followed by 60 seconds of water rinsing. Na^{22} was the tracer in these tests. Thermally steam-grown SiO_2 (1200°C, 1 micron thick film) retained less than 3×10^{13} Na^+/cm^2, whereas pyrolytically deposited SiO_2 (725°C, tetraethyl orthosilicate, 1 micron thick film)[31] retained 1.4×10^{16} Na^+/cm^2 geometric surface area. This large difference is probably due to the porosity of the undensified pyrolytic layer. Thermal SiO_2 and silicon immersed in cold NaCl solution are reported to have a much greater tendency of retaining Na^+ ions than SiO_2 deposited from SiH_4 or $SiCl_4$; however, in that work,[18] the Na^+ was found trapped by localized surface defects (on the silicon wafer, or the oxide film) and could not be removed by water rinsing. This appears not to be the case in the present work, as shown in the water desorption curve (Fig. 5). The residual level detectable after 10 minutes rinsing in deionized water at 100°C was 3×10^{13} Na^+/cm^2, a decrease of nearly 1000-fold. The distribution of sodium in thermally grown silicon dioxide layers on silicon has been reported in considerable detail[9, 13-18] and will not be discussed here.

3.2 Fluoride Ions from Hydrofluoric Acid Etchants

Five different etch compositions were prepared, all labeled with millicurie quantities of HF^{18}. Silicon and germanium wafers of different doping types, resistivities, and surface finishes were immersed in the radioactive etchants at 25°C for periods ranging from 10 seconds to 6 hours. All samples were subjected to an initial water-rinse sequence prior to measuring the F^{18} radioactivity: 5 rinses, each in 20 ml deionized water at 20°C for 6 seconds, followed by a dip in acetone for 6 seconds.

The rapid distintegration rate of F^{18} and the presence of small amounts of radioactive impurities made it difficult to perform the radio-

activity measurements. The experimentally determined life-time for the resolved F^{18} activity in the various etch solutions was within ±1.2% of the theoretical, and the F^{18} at the start of the measurements was 99.85% of the total gamma activity. The non-F^{18} activity was identified by gamma spectrometry, decay analysis, and chromatographic colorimetric analysis as Sb^{122}, Au^{198}, and Mo^{99}-Tc^{99m}; their adsorption behavior will be discussed in Part II* of this series. Electronic effects of adsorbed fluoride on silicon surfaces were described in the literature.[32, 33]

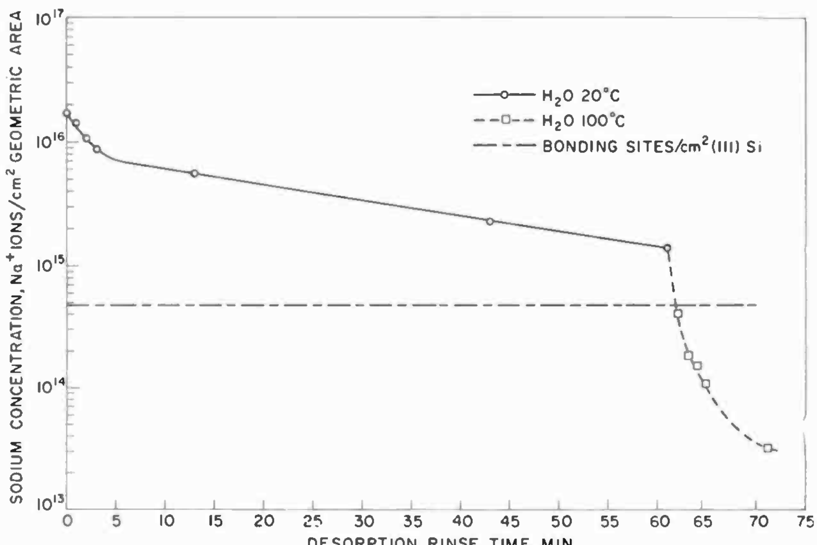

Fig. 5—Desorption of Na+ Ions from pyrolytic SiO_2 film with H_2O. Silicon wafer coated with pyrolytic SiO_2 film immersed in 0.7N $Na^{22}OH$ at 100°C followed by the indicated rinsing treatments.

3.2.1 *Adsorption of F^- Ions on Silicon from Aqueous HF^{18}*

Five silicon wafers, lapped on one side and mechanically polished on the other, that had been immersed 1N HF^{18} for 30 minutes and rinsed for 30 seconds, retained 4.6 to 7.7 × 10^{16} F^- ions/cm² regardless of the surface finish, the type of dopant, or the resistivity of the silicon. A summary of these and other data is presented in Table III. Diffusion doped wafers had 2 to 3 times higher concentrations for unknown reasons. A wafer freshly etched in HF-HNO_3 without F^{18} tracer adsorbed

* RCA Review, Vol. 31, p. 234, June 1970.

Table III—Adsorption of Fluoride Ions by Silicon from Dilute Hydrofluoric Acid (F^{18} Used as a Radioactive Tracer)

Reagent	Adsorbant Wafer					Immersion	Adsorbate
Solution Composition	Number of Wafers	Dopant	Resistivity Type	Resistivity (ohm-cm)	Preparation	Minutes at 23°C	F^- ions/cm²*
1.1N HF	3	B	p	4	lapped/polished	30	6.46×10^{16}
1.1N HF	1	Sb	n	0.007	lapped/polished	30	5.90×10^{16}
1.1N HF	1	B	p	160†	Chemically etch-polished and heated 21 hr at 1300°C; HF etched	30	5.88×10^{16}
1.1N HF	1	B	p	32†	Chemically etch-polished and boron diffused 21 hr at 1300°C; HF etched	30	2.18×10^{17}
1.1N HF	1	P	n	0.12†	Chemically etch-polished and phosphorus diffused 30 min at 1200° C; HF etched	30	1.16×10^{17}
1.1N HF	1	B	p	8	Freshly iodine-etched	30	2.58×10^{16}
1.1N HF	1	B	p	8	lapped	360	1.08×10^{17}

* After 30 seconds initial water rinsing plus a 6-second dip in acetone.
† Value in ohms/square.

3 times fewer fluoride ions from 1N HF^{18}; this appears to be caused by a slow rate of exchange between the adsorbed F^- ions and those in solution. A 6-hour exposure led to hardly double the concentration attained in 30 minutes, indicating a high initial rate of adsorption, similar to that observed for Na^+ from cold $Na^{22}OH$ (Fig. 2).

It will be shown later that acetone is an extremely effective desorbing agent for fluoride on etched silicon surfaces. There is no evidence, however, that the 6-second rinse in acetone following the initial rinse of the present HF-immersed samples removed a substantial quantity.

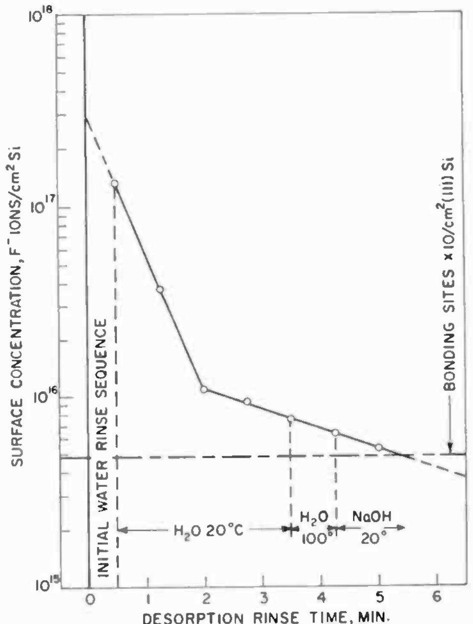

Fig. 6—Desorption of F^- Ions from silicon with H_2O. Silicon wafers immersed in 1N HF^{18} followed by initial water rinsing and the indicated desorption treatments.

Additional rinsing of the wafers with pure water at 20°C decreased the F^- concentration rapidly. As shown by the typical desorption curves in Fig. 6, 3 minutes additional rinsing led to a 94% decrease. Extrapolation of the exponential portion of the curve back to time "zero" (removal from the HF^{18} bath without rinsing) indicates an original F^- concentration of approximately 3×10^{17} F^-/cm^2; in other words, the initial 30-second water rinse removed about 60% of the original fluoride layers. Continued rinsing for 15 minutes reduced the adsorbate gradually to 5×10^{15} F^-/cm^2. The desorption behavior

indicates that the major portion of the fluoride ions is readily removable by water rinsing. However, as the monolayer concentration range is approached, the desorption with cold water proceeds at a much lower rate.*

The volatility of the fluoride adsorbate on silicon from HF^{18} was tested by heating wafers after the initial 30-second water rinse at 1250°C in an argon atmosphere for 30 minutes. At least 40% of the fluoride concentration was still present on the samples after this treatment.

3.2.2 *Adsorption of F^- Ions on Silica from HF^{18}*

Fused quartz that had been etched in dilute or concentrated HF^{18} and given the initial water rinse had a lower floride concentration than silicon, as would be expected from a continuously dissolving surface. Values after the initial rinse ranged in the low 10^{15} F^-/cm^2.

3.2.3 *Adsorption of F^- Ions on Silicon from HF^{18}-Containing Silicon Etchants*

In contrast to the essentially static conditions that prevail on immersing wafers in HF solutions,† which resulted in fairly uniform surface concentrations of fluoride, etching of wafers in strong acid etchants led to rather variable quantities of adsorbed fluoride ions. Silicon wafers etched in undiluted acid etchants, followed by "quenching" with distilled water plus a 30-second water rinse, exhibited adsorption levels in the range of 10^{16} F^-/cm^2. Dilution of the etchant with acetic acid led to lower surface concentrations, as seen from the typical values presented in Table IV. Acetone was found to be a highly effective desorbing agent for fluoride ions from etched silicon surfaces: a 30-second rinse decreased the F^- adsorbate by, typically, two orders-of-magnitude to a residual concentration of 5 to 10×10^{14} F^-/cm^2. This quantity corresponds approximately to the number of chemical bonding sites on a smooth (111)-oriented single-crystal silicon surface (4.8×10^{14} per cm^2).

3.2.4 *Adsorption of F^- Ions on Germanium from HF^{18}-Containing Solutions*

A summary of results is presented in Table V. As observed for silicon, the adsorption of fluoride ions from HF on germanium surfaces

* A residual value of 2×10^{14} F^-/cm^2 was reported[24] for silicon wafers that had been immersed in diluted HF followed by treatments with water at 95°C. However, the time periods of rinsing were not specified.

† Even in concentrated (48%) HF, the etch rate of n-type, 2 ohm-cm, (111)-oriented silicon at 25°C is only 0.3 Å/min.[34]

Table IV—Adsorption of Fluoride Ions by Silicon from Etch Mixtures (F^{18} used as Radioactive Tracer)

Reagent	Adsorbent Wafer					Immersion	Adsorbate
Solution Composition	Number of Wafers	Dopant	Resistivity Type	Resistivity (ohm-cm)	Preparation of Surface	Minutes at 23°C	F^- ions/cm²**
4 vol HF 49% + 8 vol HNO_3 70% + 9 vol CH_3CO_2H	4	B	p	8	lapped	1.0	9.7×10^{16} $\sim 1 \times 10^{15}$†
Iodine Etch*	3	B	p	8	lapped	1.0	1.8×10^{16} $\sim 5 \times 10^{14}$†
1 vol Iodine Etch* + 4 vol CH_3CO_2H	1	P	n	8	lapped	1.7	$\sim 9 \times 10^{15}$
1 vol Iodine Etch* + 4 vol CH_3CO_2H	1	P	n	8	polished	1.7	$\sim 3 \times 10^{15}$
1 vol Iodine Etch* + 4 vol CH_3CO_2H	1	B	p	8	lapped	1.7	$\sim 9 \times 10^{14}$
1 vol Iodine Etch* + 4 vol CH_3CO_2H	1	B	p	8	lapped	0.17	$\sim 4 \times 10^{14}$

* 1.00 vol HF 49.5%
1.00 vol HNO_3 70.5%
1.40 vol CH_3CO_2H 100%
0.22 vol H_2O (introduced with tracer)
0.24% Triton = ×100 nonionic surfactant (Rohm and Haas Co.)
0.15% Iodine Crystals

** After 30 seconds initial water rinsing.

† Additional 30 seconds rinse in acetone.

is not markedly affected by the dopant (Ga, In, Au) or the resistivity (0.001 to 8 ohm-cm) and is in the same concentration range as that for silicon. Germanium wafers etched in various etchants also acquired concentrations similar to those for silicon.

Table V—Adsorption of Fluoride Ions by Germanium (F^{18} Used as Radioactive Tracer)

Reagent	Adsorbent Wafer				Immersion	Adsorbate
Solution Composition	Dopant	Resistivity Type	Resistivity (ohm-cm)	Preparation of Surface	Minutes at 23°C	F^- ions/cm^2**
0.50N HF	Sb	n	0.25	polished	30	1.01×10^{16}
0.50N HF	Sb	n	0.25	etch polished	30	1.66×10^{16}
1.1N HF	Ga	p	0.001	lapped/ polished	30	9.30×10^{16}
1.1N HF	P(Au)	n	0.02	lapped/ polished	30	5.55×10^{16}
1.1N HF	In	p	8	lapped/ polished	1.0	5.12×10^{16}
4 vol HF 49% + 8 vol HNO_3 70% + 9 vol CH_3CO_2H	In	p	8	lapped/ polished	1.0	$\sim 6 \times 10^{14}$†
Iodine Etch	In	p	8	lapped	1.0	$\sim 5 \times 10^{14}$†

* 1.00 vol HF 49.5%
1.00 vol HNO_3 70.5%
1.40 vol CH_3CO_2H 100%
0.22 vol H_2O (introduced with tracer)
0.24% Triton = ×100 nonionic surfactant (Rohm and Haas Co.)
0.15% Iodine Crystals

** After 30 seconds initial water rinsing plus a 6-second rinse in acetone.

† Additional 24-second rinse in acetone.

3.3 Chloride Ions from Hydrochloric Acid

The substrates were immersed at 23°C in 0.2N HCl that had been "tagged" with HCl^{38}. After a 30-second initial rinsing sequence in water, as described for the fluoride experiments, the gamma ray spectrum of the radioactivity on each sample was measured and recorded automatically at high speed for later evaluation of the Cl^{38} net radioactivity.

3.3.1 *Adsorption of Cl^- Ions on Silicon from HCl^{38}*

Lapped, p-type silicon wafers were etched in 1.25N (5%) NaOH at 100°C for 60 seconds followed by direct immersion for 100 seconds in

the radioactive HCl^{38} to simulate transistor processing conditions. The wafers after the initial rinse had an average surface concentration of approximately 1×10^{14} Cl^- ions/cm^2.

Desorption tests were made using microcrystalline silicon powder to increase the analytical sensitivity. Powder samples that had been equilibrated in the HCl^{38} lost the activity extremely rapidly on batch rinsing with deionized water at 23°C. (The powder was separated from the fluoride by a brief centrifugation.) The surface concentration after the fifth wash, or a total of 9 minutes of rinsing, calculated from the Cl^{38} activity and the estimated surface area, was below 10^{14} Cl^-/cm^2, with evidence of additional decrease on continued rinsing. Clearly, the Cl^- ions from HCl on silicon are held only by relatively weak Van der Waals forces, so that desorption takes place rapidly with pure water at room temperature.

3.3.2 *Adsorption of Cl^- Ions on Germanium, Silica, and Metals from HCl^{38}*

Lapped, p-type germanium wafers immersed for 100 seconds in the 0.2N HCl^{38} adsorbed 3×10^{14} Cl^-/cm^2. Fused quartz plates immersed for 100 seconds attained a concentration less than 10^{15} Cl^-/cm^2.

Various metal parts were immersed for 60 seconds in 1.25N NaOH at 100°C followed by immersion for 100 seconds in the radioactive acid. The following surface concentrations were measured on these samples after the initial water-rinse: electroplated nickel 7.3×10^{14}; lead 4.6×10^{15}; electroplated indium 3.4×10^{17} Cl^- ions/cm^2. The adsorbate on the indium was strongly chemisorbed: The residual concentrations after rinsing in boiling water for 5 minutes was 66%, and after 40 minutes was still 16% of the initial value.

3.4 Iodine from Various Solutions

Etches containing molecular iodine isotopically "tagged" with I^{131}, were examined. Aqueous sodium iodide solution (NaI^{131}) containing the iodine in ionic form was also tested for comparison. The results are summarized in Table VI.

3.4.1 *Adsorption of Iodine on Silicon and Germanium from Standard Etch with I^{131}*

Etching of silicon wafers in standard iodine etch for 100 seconds followed by quenching with distilled water led to surface concentrations ranging from 4×10^{13} to 4×10^{14} I_2 molecules*/cm^2. The varia-

* The brown color of the etchant suggests that the iodine is present in molecular form; it is assumed that the adsorbate also consists of molecular iodine.

Table VI—Adsorption of Iodine by Silicon, Silica, and Germanium (I^{131} Used as Radioactive Tracer)

Reagent		Adsorbent Wafer			Immersion	Adsorbate	
Solution Composition	% Iodine	Material	Doping Type	Initial Surface	Minutes at 23°C	Distribution	Surface Concentration*
							I_2 Molecules/cm^2
Iodine Etch[a]	0.144	Si	p	lapped	1.7	uniform	4.15×10^{13}
Iodine Etch[a]	0.144	Si	p	lapped	1.7	uneven	4.70×10^{13}
Iodine Etch[a]	0.144	Si	p	lapped	1.7		3.44×10^{14}
Iodine Etch[a]	0.144	Si	p	lapped	1.7	some spots	3.73×10^{14}
Iodine Etch[a]	0.144	Ge	p	lapped	1.7	uniform	1.69×10^{14}
Iodine Etch[a]	0.144	Ge	p	lapped	1.7		2.69×10^{14}
Iodine Etch[a]	0.144	Ge	p	lapped	1.7	uniform	2.76×10^{14}
Special Etch[b]	0.00016	Si	p	lapped	1.7	uniform	4.52×10^{11}
Special Etch[b]	0.00016	Si	p	lapped	1.7	uniform	9.05×10^{11}
Special Etch[b]	0.00016	Ge	p	lapped	1.7	uniform	3.40×10^{12}
Special Etch[b]	0.00016	Ge	p	lapped	1.7	uniform	4.56×10^{12}
							I^- Ions/cm^2
0.010N NaI	0.127	Si	n	lapped/ polished	30	some pin-spots	2.87×10^{14}
0.010N NaI	0.127	SiO_2 (thermal)	on n-Si	vitreous	30	pin-spots	2.45×10^{14}
0.010N NaI	0.127	SiO_2 (pyrolytic)	on n-Si	vitreous	30	uniform	1.50×10^{14}

* After 30 seconds initial water rinsing plus dip in acetone.

(a) Composition as stated in Table III except that the iodine was added in form of NaI^{131} to insure isotopic hemogeneity.

(b) 1.00 vol HF 49.5%, 6.00 vol HNO_3 70%, 3.00 vol CH_3CO_2H 100%, 0.19 mg NaI per 100 ml

tion in these values appears to be caused by nonuniform distribution of adsorbate on the surface, as detected by autoradiography. The most effective of the desorbing agents shown in Fig. 7 was EDTA (ethylene diamine tetra acetic acid) solution at 95°C, which lowered the I_2 con-

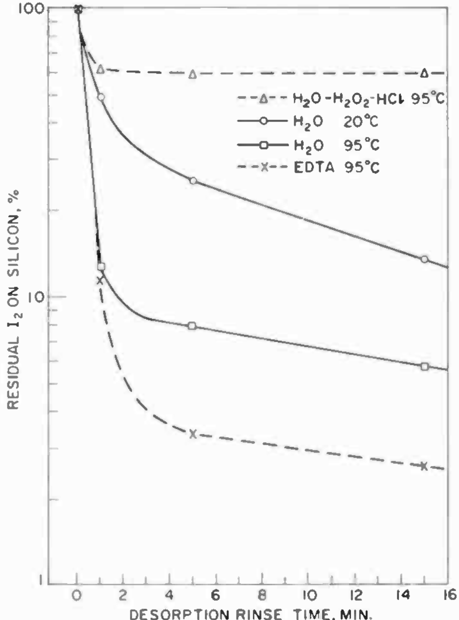

Fig. 7—Desorption of I_2 from etched silicon wafers with various solutions.
Substrate: Silicon etched in I^{131} containing iodine etch and given an initial water rinse. Surface concentration at this point $= 100\%$ (10^{13} to 10^{14} I_2/cm^2).
Desorbing Solution: H_2O, deionized; EDTA in H_2O, saturated solution; mixture of 1 vol 30% H_2O_2 + 1 vol 1N HCl + 8 vol H_2O.

centration to 3% of the initial value in 5 minutes. Germanium wafers treated similarly showed more reproducible and uniformly distributed surface concentrations of 1.7 to 2.8×10^{14} I_2/cm^2. Desorption proceeded much more readily than with the silicon, as seen from the plots in Fig. 8.

3.4.2 *Adsorption of Iodine on Silicon and Germanium from a Special Etch with I^{131}*

A mixture of HF-HNO_3-CH_3CO_2H containing 10^3 times less iodine than the preceeding etchant (section 3.4.1) led to uniform surface concentrations lower by about 50 to 100 times compared with the standard

etch, for both silicon and germanium. Again, germanium adsorbed a larger quantity than silicon.

3.4.3 *Adsorption of I^- Ions on Silicon and Silicon Dioxide from Aqueous NaI^{131} Solution*

For comparison with the etchants described above, the adsorption of iodine ions from a 0.010N (0.127%) NaI^{131} solution in distilled water

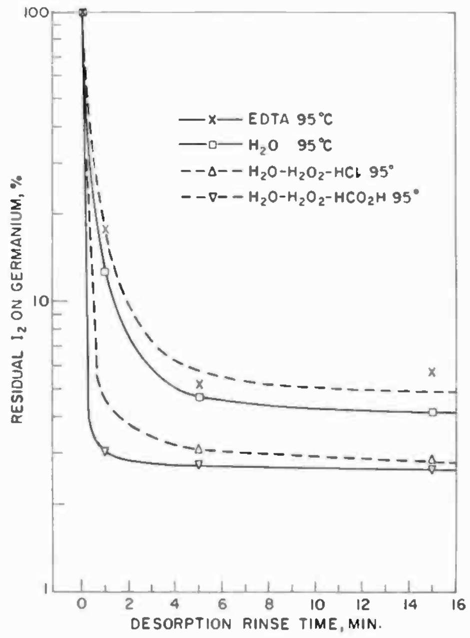

Fig. 8—Desorption of I_2 from etched germanium wafers with various solutions.
Substrate: Germanium etched in I^{131}-containing iodine etch and given an initial water rinse. Surface concentration at this point = 100% (1.7 to 2.7×10^{14} I_2/cm^2).
Desorbing Solutions: H_2O deionized; EDTA in H_2O, saturated solution; mixture of 1 vol 30% H_2O_2 + 1 vol 1N HCl + 8 vol H_2O; mixture of 1 vol 30% H_2O_2 + 1 vol 90% HCO_2H + 8 vol H_2O.

was tested for silicon wafers with and without silicon dioxide films. The surface concentration measured for the pyrolytic SiO_2 film[31] was 1.5×10^{14} I^-/cm^2 and the iodine was uniformly distributed. The concentration on the thermally grown SiO_2 film, and on the silicon substrate, averaged about twice this value, probably because of localized pin-spots of iodine seen with high-resolution autoradiographic techniques.

3.5 Chromium from Dichromate-Sulfuric Acid Solution

Solutions of dichromate ions in sulfuric acid are strong oxidants due to the hexavalent chromium ion, $Cr_2O_7^{-2}$. Heated, these solutions are often used to remove photoresist films and organic contaminants from silicon device surfaces.* It is therefore important to ascertain whether chromium contamination occurs under these conditions. The addition of Cr^{51} tracer to dichromate-sulfuric acid solution yielded an adsorbate radioactivity too low for reliable measurements because of the large isotopic dilution with the natural chromium isotopes. Emission spectrographic analysis with silicon powder was therefore employed to obtain an estimate of adsorption.

Five grams of silicon powder having a minimum surface area of 660 cm^2/g was mixed with 25 ml Chromerge-H_2SO_4 mixture and heated to fuming for 15 minutes, as customary for silicon wafers. The acid was then decanted, and the silicon washed thoroughly with cold deionized water, followed by settling and decantation. The last wash water showed negative tests for chromium-VI ions with benzidine reagent.[35] Original and final samples of the dried silicon powder were tested for chromium by emission spectrographic analysis using high-sensitivity photographic plates. No chromium could be detected in either sample. This result indicated a residual chromium concentration of much less than 10^{14} Cr ions/cm^2 of silicon, based on the estimated limiting sensitivity of the analytical method.

4.0 Conclusions

From the standpoint of device processing, the following conclusions can be derived.

1. Sodium contamination resulting from the etching of silicon devices in hot NaOH can be effectively reduced to below 0.001 monolayer by immediately rinsing with room-temperature deionized water, followed by rinsing in strong HCl for several minutes, and finally rinsing in pure water.
2. Immersing silicon or germanium wafers in aqueous HF, such as during oxide removal, results in physical adsorption of up to 10^{17} F^-/cm^2. The major portion can be readily removed by rinsing with cold deionized water, but appreciable quantities of strongly adsorbed fluoride remain even after 15 minutes of rinsing. Rinsing

* Commercial solutions, such as Chromerge (Registered trademark, Manostat Corp., New York, N. Y.) are particularly convenient to use: 25 ml Chromerge added to 9 lbs. H_2SO_4 98%.

with hot deionized water is necessary to speed up the desorption of the chemisorbed fluoride.

3. F^- contamination is also difficult to remove by heating. Exposing silicon wafers with adsorbed fluoride layers to typical diffusion temperature (1250°C) in dry ambient causes only partial volatilization of the fluoride.
4. Adsorbed F^- ions resulting from the etching of silicon or germanium wafers in HF-containing etchants are most effectively removed by rinsing with acetone for a few minutes.
5. Adsorption of chloride ions from HCl on silicon or germanium is very weak and the material can be readily removed by rinsing with deionized water at room temperature.
6. The remarkably large quantities of iodine adsorbed on silicon and germanium during etching in iodine containing etchants are best removed by rinsing with acetone, followed by treatment with hot EDTA solution.
7. Simple water rinsing of silicon wafers after treatment with hot chromic-sulfuric acid mixture effectively eliminates chromium residues.
8. In general, it should be kept in mind that contamination can be minimized by using reagents at low concentration and (generalizing the observations made with Na^+ adsorption) by proceeding immediately with rinsing treatments without allowing the wafers to dry between the rinses.

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Radiochemical Study of Semiconductor Surface Contamination

II. Deposition of Trace Impurities on Silicon and Silica

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Abstract—Surface contamination of silicon and silica by eight low-level-impurity elements was studied by radiochemical tracer techniques. Radionuclides used to label reagent trace constitutents are Au^{195}, Cu^{64}, Fe^{59}, Cr^{51}, Zn^{65}, Sb^{122}, Sb^{124}, Mn^{54}, and Mo^{99}. The deposition of these impurities from typical reagent solutions used in silicon device processing was investigated as a function of reagent composition, impurity concentration in solution, immersion time and temperature, condition of the adsorbent surface, and the presence or absence of chelating agents in the solutions. Various desorption treatments, e.g., rinses in water, acids, complexing reagents, and chelating compounds, were evaluted. To permit comparison of the quantities of the various impurities that deposit from reagent solutions, the data in this summary have been normalized to a constant impurity concentration of 4 ppm (w/v) per impurity expressed as atoms per cm^2.

Silicon wafers etched in mixtures of HF + HNO_3, with or without CH_3CO_2H or I_2, and containing just one specific radiotracer, showed surface concentration levels as follows: 10^{13} Au/cm^2, 10^{12} Cr/cm^2, 10^{11} Cu/cm^2, less than 10^{11} Mn/cm^2, and 10^{10} or less Fe/cm^2. These quantities represent small fractions of a monoatomic layer coverage of the silicon. For deposition from HF, the situation is considerably more severe since the surface oxide is dissolved without the silicon being etched, resulting in uninhibited electrochemical displacement plating. Surface concentrations of 3×16^{16} Cu/cm^2, 7×10^{14} Au/cm^2, 4×10^{14} Cr/cm^2, 1×10^{11} Fe/cm^2 are obtained with this reagent labeled with the corresponding ions. Sb and Mo also deposit, but not Zn ions, which are strongly complexed in HF.

Adsorption by silicon of trace metals from concentrated HNO_3, HCl or aqua regia is only 2-4 $\times 10^{12}$ Au or Cu/cm^2, and 3×10^{11} Fe/cm^2 because of the oxide film that protects the silicon in these acids. Washing of silicon wafers with hot deionized and distilled water containing radioactive copper led to similarly low levels if the preceding surface treatment produced an oxide layer. Silica provides an extreme example of this type adsorbent surface, leading to even lower levels of adsorption, including immersion in HF. However, oxide-stripped (in effect fluoridated) silicon adsorbs large quantities of metals from mineral acids or water.

Adsorption of metal ions from diluted H_2O_2 fluctuated, depending on conditions, but was generally high. Deposition from 5% NaOH under silicon etching condition (100°C) was 2×10^{16} Cu/cm^2, 6×10^{15}

Fe/cm^2, 1×10^{15} Au/cm^2, and 5×10^{13} Sb/cm^2.

The structure and finish of the silicon surface (other than oxide layers), the doping type and concentration, and the bath immersion time had negligible effects on the extent of impurity deposition. The resulting quantity of an impurity deposited versus the log of the impurity deposited was usually proportional to its concentration in solution and usually followed a straight-line log-log relation.

Attempts to inhibit impurity deposition on silicon by the addition of chelates to the reagent solutions were generally not successful. However, many chelating agents were able to remove deposited metals from the semiconductor surfaces. The most consistently excellent results were achieved by complexing dissolution in acidic H_2O_2. HCl was outstanding in its efficiency for desorbing Fe deposits.

1. Introduction

The results of radiochemical studies of semiconductor surface contamination by *components* of processing reagents were presented in part I of this series.[1] The present paper is concerned with inorganic *trace* contaminants in reagents commonly employed in the processing of silicon devices. A survey of the literature covering the subject matter of both parts was presented in the introduction of Part I, as was a brief discussion of sources of contaminants and their effects on the electrical performance of devices.

The present paper discusses results obtained using a number of radionuclides to follow the fate of trace impurities in reagents employed in semiconductor processing. These include gold-198, copper-64, iron-59, chromium-51, zinc-65, antimony-122 and 124, manganese-54, and molybdenum-99. Substrate materials include primarily silicon wafers; silica was examined only briefly. The concentration of specific impurities on these substrates was determined by conventional radiotracer techniques. Certain selected results of these investigations have previously been published.[2,3] Deposition of trace impurities under similar conditions on germanium and gallium arsenide will be presented separately as Part III.[4]

Desorption tests were made to explore the nature of the bonding and the chemical form of the impurity on the surface and also to indicate means for removing the contaminants. The most generally effective desorption treatment is based on complexing solutions containing hydrogen peroxide. The application of such reagents is discussed in detail in a separate paper.[5]

2. Experimental

2.1 Preparation of Radioactive Reagents

Important nuclear data[6] for the radionuclides used as tracers are summarized in Table 1.

Gold-198 was prepared by thermal neutron activation* of pure metal wire. The activated wire was first cleaned by etching in nitric acid, and then was dissolved in a minimum volume of hot aqua regia and diluted with distilled water. Small aliquots were added to the various reagent solutions to yield gold ion concentrations of 3 to 31 ppm. A small quantity of antimony-124 was also prepared by thermal neutron activation of the element.

Table 1—Pertinent Properties of the Radioactive Isotopes Used as Tracers

Isotope	Lifetime	Modes of Decay	Decay Energy (MeV)	Principle Radiations: Particle Energies (MeV)	Particle Intensities	Gamma Energies (KeV)	Gamma Intensities
$_{79}Au^{198}$	2.693d	$\beta-$	1.374	0.961	98.9%	412	99%
$_{26}Fe^{59}$	45.1d	$\beta-$		0.475 0.273	51% 48%	192 1099 1292	2.5% 56% 44%
$_{24}Cr^{51}$	27.8d	EC	0.752			320	9%
$_{30}Zn^{65}$	243.6d	$\beta+$, EC	1.353	0.325	1.54%	1116	50.6%
$_{51}Sb^{124}$	60.3d	$\beta-$	2.916	0.23 0.621 2.317	11% 50% 22%	603 646 1691	100%* 7.5% 51%
$_{51}Sb^{122}$	2.8d	$\beta-$ $\beta+$, EC	1.972 1.62	$\beta+$0.56 $\beta-$1.40 1.97	 63% 30%	AR 564 686	 70% 3.5%
$_{25}Mn^{54}$	303d	EC	1.379			835	100%
$_{29}Cu^{64}$	12.9 hr	$\beta-$ $\beta+$, EC	0.573 1.677	0.573 0.654	39.6% 19.3%	AR 1348	 0.6%

Data adapted from Ref. [6].
$\beta-$ = Negative beta emission
$\beta+$ = Positron emission
EC = Orbital electron capture
AR = 511 KeV photon associated with annihiliation of positrons in matter
d = day
hr = hour
* = relative intensity

* RCA facilities at the Industrial Reactor Laboratories, Inc., Plainsboro, N. J.

The copper-64 used in some experiments was prepared like the gold, except that the activated and purified wire was dissolved in a small volume of nitric acid. Reagents were prepared to yield copper ion concentrations of 0.01 to 109 ppm. A copper-64 preparation of high specific radioactivity (90 curies per gram of copper) was purchased† in form of $Cu(NO_3)_2$. It was used for preparing reagents with copper concentrations ranging down to 2 ppb.

Iron-59 with a specific radioactivity of 16 curies per gram of iron was obtained† in the form of purified $FeCl_3$. Alkaline etch solutions were centrifuged before calibration to remove traces of insoluble iron hydroxide. Chromium-51 was obtained† as $CrCl_3$ with a radiochemical purity of greater than 99% and having a specific radioactivity of 15 curies per gram of chromium. Aliquots of the original solution were directly added to the various reagent solutions to yield a chromium ion concentration of 2.5 ppm.

Zinc-65 was purchased** as $ZnCl_2$ at a purity of greater than 99%. The specific radioactivity was approximately 400 millicuries per gram of zinc. Manganese-54 was obtained** in carrier-free form as $MnCl_2$ with a radiochemical purity greater than 99%.

Molybdenum-99, antimony-122, and gold-198 were detected as trace impurities in the fluorine-18 preparations[1] and were used in studies of composite adsorption from mixtures.

Mineral acids of electronic-grade purity were used in all instances. Other reagents were typically of analytical grade purity. Impurity concentrations of various starting reagents were determined by emission spectrographic analysis with the results shown in Table 2. The composition of the reagent solutions and etch mixtures is listed in the tables included in this paper; two complicated formulations are in the Appendix.

2.2 Experimental Methods

The preparation of the semiconductor and silica substrates, the immersion treatment in the various etchants and reagent solutions, and the various techniques for the subsequent initial rinsing and the desorption treatments were all described in detail in Part I.[1] The techniques used in radioactivity measurements and calculations, gamma spectrometry, autoradiographic analysis, and life-time determination of the nuclides were also described there.

† Oakridge National Laboratory, Oakridge, Tenn.

** NSEC (Nuclear Science and Engineering Corporation, Pittsburgh, Pa.)

3. Results and Discussion

3.1 Contamination by Gold

Gold is a commonly occuring impurity that can seriously contaminate semiconductors surfaces, especially during etching in solutions containing hydrofluoric acid. The extreme position of gold in the electrochemical series suggests that deposition on semiconductor surfaces takes place primarily by an electrochemical displacement mechanism that

Table 2—Typical Impurity Concentrations in a Semiconductor Etch Mixture*

Impurity Element	Commercial Mixture A, ppm	Commercial Mixture B, ppm	Laboratory Mixture, ppm
Cr	0.2	0.2	0.1
Mn	0.08	0.02	0.05
Cu	0.06	0.2	0.08
Fe	1	1	2
Al	2	6	5
Ag	0.2	0.02	0.04
Mg	> 1	> 1	1
Ni	< 0.1	< 0.1	< 0.1
Pb	0.1	0.1	< 0.1
Na	not detected	1	1
Total	~ 5	~ 10	~ 9

* By chemical analysis of the following composition: 1 vol 49% HF
6 vol 70% HNO_3
3 vol 100% CH_3CO_2H

leads to metallic gold deposits. Surface concentrations on etched silicon on the order of 10^{14} Au atoms/cm^2 have been reported,[7] but much lower concentrations can be critical. Since gold has a comparatively high diffusion constant and a high solid solubility in silicon,[8] it may cause lifetime degradation on subsequent heating.[8,9] The assessment of contamination by gold under various typical chemical processing conditions is, therefore, particularly important.

Adsorption data for silicon under both etching and nonetching conditions at gold-ion concentrations of 3 to 31 ppm are presented in Table 3. Data for silica as adsorbents are summarized in Table 4. As previously,[1] semiconductor etchants containing HF were quenched with de-ionized water to stop the etching before withdrawing the wafer. All samples were initially rinsed in 5 portions of 20 ml deionized water for 6 seconds per rinse, followed by an additional 30-seconds rinse

Table 3—Deposition of Gold on Silicon (Au^{198} Used as Radioactive Tracer)

Reagent	Gold Solution		Adsorbent Wafer*			Immersion	Adsorbate
Solution Composition	Au ppm	Au ions/cm^3	Dopant	ohm-cm Resistivity	Wafers	min at 23°C	Au atoms/cm^2
49% HF	3.1	9.5×10^{15}	B	7	2	15	4.9×10^{14}
49% HF	6.2	1.9×10^{16}	B, P	1-9	2	30	2.1×10^{15}
HF 49% + 0.1% EDTA	6.2	1.9×10^{16}	P	3	1	30	1.2×10^{15}
HF 49% + 10% CM**	5.6	1.7×10^{16}	B	8	1	30	2.7×10^{15}
37% HCl	3.1	9.5×10^{15}	B	7	1	15	2.5×10^{12}
70% HNO_3	3.1	9.5×10^{15}	B	7	1	15	1.9×10^{12}
1 vol HNO_3 70% + 3 vol HCl 37%	3.1	9.5×10^{15}	B	7	1	15	1.4×10^{12}
70% HNO_3	6.2	1.9×10^{16}	P	3	1	30	1.2×10^{12}
7 vol HF 49% + 93 vol HNO_3 70%	6.2	1.9×10^{16}	B	8	1	15	7.4×10^{13}
Iodine Etch**	3.1	9.5×10^{15}	B	8	1	1.0	1.4×10^{13}
Iodine Etch**	6.2	1.9×10^{16}	B	8	1	1.0	2.0×10^{14}
Iodine Etch**	6.2	1.9×10^{16}	P	3	1	1.0	3.8×10^{14}
Iodine Etch**	31.0	9.5×10^{16}	P	6	1	1.5	3.0×10^{15}
1% $NaHSO_3$	15.5	4.7×10^{16}	P	3	1	30	6.9×10^{13}
1% H_2O_2	15.5	4.7×10^{16}	P	3	1	30	5.8×10^{15}
5% NaOH	10	3×10^{16}	B	7	1	1.0 at 100°C	3.3×10^{15}

* Surface finish on all wafers: lapped initially
** See Appendix for composition

sequence in acetone. The samples were then air-dried, and the gamma radioactivity was determined by scintilation counting.

The resulting surface concentrations are expressed in terms of the number of atoms (indicated by the symbol for the element) per cm^2 of geometric surface area, with no distinction between alternating chemical states of the deposited species. (This method is also followed in all subsequent discussions of other impurities).

Table 4—Deposition of Gold on Fused Silica (Au^{198} Used as Radioactive Tracer)

Reagent	Gold Solution		Immersion	Adsorbate
Solution Composition	Au ppm (added)	Au ions/cm^3 (added)	(Min. at 23°C)	(Au atoms/cm^2)
49% HF	31	9.5×10^{16}	15	1.6×10^{12}
37% HCl	31	9.5×10^{16}	15	5.9×10^{11}
70% HNO_3	31	9.5×10^{16}	15	1.7×10^{12}
Aqua Regia	31	9.5×10^{16}	15	4.8×10^{11}

Silicon wafers immersed for 15 minutes in concentrated HF containing 3 ppm* of gold acquired 5×10^{14} Au/cm^2 (Table 3). The difference between a lapped and a polished wafer surface was insignificant. The distribution of the gold on the polished wafer was examined by autoradiography and found to be uniform. Doubling the gold concentration and the immersion time yielded four times the surface concentration. Adsorption on fused silica was found to be 3 to 4 orders of magnitude lower under comparable conditions (Table 4), demonstrating the protective effect of a silicon oxide film as long as it covers the entire semiconductor surface during immersion. As soon as the oxide film has dissolved, the large electrochemical potential difference between the exposed semiconductor surface and the gold ions in the HF solution leads to rapid deposition of metallic gold. It should be pointed out, however, that even though the concentration adsorbed by silica was relatively low, the removal of that gold required hot HCl-H_2O_2 treatments.[5]

Ion-exchange resin studies showed that the gold in the concentrated HCl, HNO_3, and aqua regia solutions existed as the tetrachloro(III) acid, $H(AuCl_4)$. This stable anionic complex would be expected to associate weakly with the hydrated oxide covering the surface of the

* All concentrations stated as "ppm" in this paper are on a weight/volume basis.

silicon. Experimentally, we found that silicon wafers immersed in these solutions containing 3 or 6 ppm of gold adsorbed only $1\text{-}3 \times 10^{12}$ Au/cm^2. Silica surfaces immersed in the same acids but containing 31 ppm of gold attained a concentration of only $0.5\text{-}2 \times 10^{12}$ Au/cm^2 (Table 4). The adsorbates from HNO_3 and aqua regia on silica were so weakly bonded that merely rinsing in hot water for 15 minutes desorbed the deposit by a factor of 20, in the case of HNO_3, and by a factor of 50, in the case of aqua regia. Hot $HCl\text{-}H_2O_2$ solution was required to remove the gold deposit from the Au^{198} containing HCl solutions.[5]

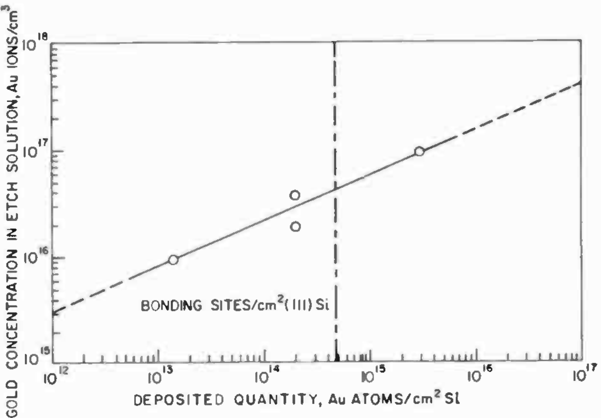

Fig. 1—Quantity of gold deposited on silicon from etchant as a function of gold solution concentration. $HF\text{-}HNO_3\text{-}CH_3CO_2H\text{-}I_2$ etch mixture containing Au^{198} as radioactive tracer. Number of bonding sites on (111) Si is indicated as a reference quantity.

From silicon etch mixtures containing concentrated HNO_3 and HF where a fresh semiconductor surface is continuously being exposed to the etchant, considerably less adsorption occured than from HF solutions of comparable concentration, leading to $0.1\text{-}4 \times 10^{14}$ Au/cm^2. The distribution of the adsorbate on one typical specimen was examined by autoradiography and was found to be uniform. The relationship between solution concentration and the resulting surface concentration is shown in Fig. 1, using the adsorption data from the iodine etch solution. The log-log plot of the data approaches a straight line that permits extrapolation to lower concentrations. A gold-ion solution concentration of 0.5 ppm, for example, can be expected to lead to a silicon surface concentration of 2×10^{11} Au/cm^2, the equivalent of 1×10^{-4} monoatomic layer of gold.

Chelating agents were added to some of the acid etchants to determine whether adsorption could be minimized. In most instances the

effects were negligible, possibly because of the destruction of the metal chelates in the extremely reactive, highly acid solutions. However, one example of successful inhibition was observed with iodine etch containing 8% of a special mixture of chelating additives (Table 3). The surface concentration of gold decreased by a factor of 25 for this mixture as compared with the etch free of chelating agents.

A comparison was made between aqueous solutions of 1% $NaHSO_3$ (sodium bisulfite) and 1% H_2O_2, both containing 16 ppm of gold. Because of the formation of the soluble complex sodium sulfitoaurate (III), the sodium bisulfite solution led to a surface concentration of only 7×10^{13} Au/cm², whereas the hydrogen peroxide yielded 6×10^{15} Au/cm².

Gold in NaOH solution should exist as the sodium salt of auric acid, Na_2HAuO_3 or $NaAuO_2$. Contamination of silicon would be expected by ionic adsorption and/or metallic deposition. One test conducted at 100°C with 5% NaOH containing 10 ppm of gold led to heavy (3×10^{15}/cm²) gold contamination.

No significant differences in contamination were generally found between n-type and p-type silicon in the 1 to 9 ohm-cm resistivity range, or between lapped and mechanically polished wafers.

Desorption tests were carried out with the silicon and silica samples treated in the acid solutions. Even strong nontoxic complexing agents such as oxalic acid, citric acid, formic acid, and EDTA (ethylene diamine tetra acetic acid) were largely ineffective in desorbing gold from the surface even at 90° to 100°C for 15 minutes. This is probably explained by the strong reducing action of these reagents for gold ions, which not only prevents desorption but tends to deposit additional gold ions as the metallic species. The most effective agent that can be used safely is acid hydrogen peroxide.[5]

3.2 Contamination by Copper

The degrading influence of copper on the lifetime of silicon devices and the thermal conversion effect of this fast-diffusing metal in semiconductors are well known. Next to sodium ions, copper is generally recognized as one of the most serious contaminants in silicon device processing. Contamination tests with Cu^{64} have been carried out for germanium[11,12] and III-V compound semiconductors[10] but no work has apparently been reported for silicon and fused quartz under typical device processing conditions except for the summaries published by the author.[2,3] The work presented in this section includes results on the deposition of copper from a large variety of reagent solutions and

from rinse water, as well as inhibition of adsorption by chelating additives, and the desorption of copper deposits with complexing and chelating agents.

The etching and initial rinsing treatments of the silicon wafers were conducted as described in the previous section on gold. The results have been summarized in Tables 5 to 7. The data for silicon are presented in Table 9.

3.2.1 Deposition of Copper on Silicon Using Cu^{64} as Tracer

Silicon wafers etched in typical mixtures containing HF, HNO_3, and CH_3CO_2H with or without iodine, to which 2 ppm of radio-active copper had been added, retained only 4×10^{10} to 7×10^{11} copper atoms per cm^2 (Table 5). This is the equivalent of less than 0.0004 monoatomic layer of copper, and is about 3 orders of magnitude less than the quantities of gold deposited under similar conditions (Table 3), probably due to the fact that copper, in contract to gold, is being redissolved by the extremely corrosive etch components. Rinsing of the etched silicon wafers with water at 100°C desorbed only 38% of the copper within 10 minutes, and further rinsing had no additional desorbing effects. As with the desorption of fluoride ions from silicon,[1] acetone at 20°C proved much more effective than hot water, removing 71% of the copper in 10 minutes, but additional rinsing did not further decrease this level.

Adsorbed copper on silicon from concentrated HCl, HNO_3, and aqua regia containing 7 ppm of Cu(II) ions was present to the extent of $3\text{-}4 \times 10^{12}$ Cu/cm^2. Similar concentration levels were measured for silicon immersed in 3% H_2O_2 at 100°C;* these adsorbates consisted usually of uniformly distributed copper plus dots of copper accumulation, as noted in Table 5.

Contamination of silicon by copper during etching with hot NaOH solution was tested using NaOH to which radioactive cupric ions had been added. Because of the trace concentrations involved, the slightly soluble copper(II) hydroxide, $Cu(OH)_2$, appeared to be completely dissolved in the etchant. Solutions containing 2 ppm of Cu^{64} led to 8×10^{15} Cu/cm^2. A 14-times higher Cu(II) solution concentration led to 4.6 times higher surface concentration (Table 5). Typical desorption curves for these adsorbates are presented in Fig. 2. The most effective of the complexing and chelating desorbents was a 0.1M aqueous solution of the pentasodium salt of diethylenetriamine penta-

* The H_2O_2 used throughout the work described in this paper was unstablized electronic grade reagent, free of additives.

Table 5—Deposition of Copper on Silicon (Cu^{64} Used as Radioactive Tracer)

Reagent	Copper Solution		Adsorbent Wafer		Immersion		Adsorbate	
Solution Composition	Cu ppm (added)	Cu ions/cm³ (added)	Dopant	Initial Surface	Duration (Min.)	Temp. (°C)	Cu atoms/cm²	Distribution
37% HCl	6.9	6.5×10^{16}	B	lapped	30	23	4.2×10^{12}	
70 % HNO_3	6.9	6.5×10^{16}	B	lapped	30	23	2.9×10^{12}	
Aqua Regia	6.9	6.5×10^{16}	B	lapped	30	23	3.1×10^{12}	
4 vol HF 49% + 8 vol HNO_3 70% + 9 vol CH_3CO_2H	2.1	2.0×10^{16}	B	lapped/polished	1.0	23	4.0×10^{11}	
4 vol HF 49% + 8 vol HNO_3 70% + 9 vol CH_3CO_2H	2.1	2.0×10^{16}	P	lapped	1.0	23	1.7×10^{11}	
4 vol HF 49% + 8 vol HNO_3 70% + 9 vol CH_3CO_2H	2.1	2.0×10^{16}	P	lapped	1.0	23	6.8×10^{10}	
Iodine Etch*	2.1	2.0×10^{16}	P	lapped	1.0	23	3.9×10^{10}	
Iodine Etch*	2.1	2.0×10^{16}	B	lapped	1.0	23	4.3×10^{10}	
Iodine Etch*	2.1	2.0×10^{16}	B	lapped	1.0	23	1.6×10^{11}	
Iodine Etch*	2.1	2.0×10^{16}	B	lapped/polished	1.0	23	1.0×10^{11}	
3% H_2O_2	2.1	2.0×10^{16}	B	polished	15	100	1.4×10^{12}	dots
3% H_2O_2	2.1	2.0×10^{16}	P	lapped/polished	15	100	2.9×10^{12}	uniform plus dots
3% H_2O_2	2.1	2.0×10^{16}	Sb	lapped/polished	15	100	2.7×10^{12}	
5% NaOH	2.1	2.0×10^{16}	B	lapped	1.0	100	7.8×10^{15}	uniform
5% NaOH	2.1	2.0×10^{16}	B	lapped	1.0	100	7.9×10^{15}	plus dots
5% NaOH	29	2.8×10^{17}	B	lapped	2.0	100	3.6×10^{16}	uniform

* See Appendix for composition

Table 6—Deposition of Copper on Silicon from Hydrofluoric Acid (CU^{64} Used as Radioactive Tracer)

Reagent		Copper Solution		Adsorbent		Immersion	Adsorbate	
Solution Composition	Inhibitor Additive	Cu ppm (added)	Cu ions/cm^3 (added)	Dopant	Initial Surface	Minutes at 23°C	Cu atoms/cm^2	Distri-bution
49% HF	none	2.1	2.0×10^{16}	B	polished	30	$1.6 \times 10^{15*}$	
49% HF	none	2.1	2.0×10^{16}	B	polished	30	$1.5 \times 10^{15*}$	uniform
49% HF	none	2.1	2.0×10^{16}	B	polished	45	$3.0 \times 10^{15*}$	
49% HF	none	2.1	2.0×10^{16}	P	lapped/ polished	40	$3.7 \times 10^{15*}$	uniform plus some dots
49% HF	none	6.9	6.5×10^{16}	B	polished	30	1.5×10^{16}	
49% HF	none	6.9	6.5×10^{16}	B	lapped	30	1.8×10^{16}	
49% HF	none	59	5.6×10^{17}	B	lapped	1.7	3.3×10^{16}	
49% HF	none	59	5.6×10^{17}	B	lapped	1.7	6.3×10^{16}	
49% HF	none	59	5.6×10^{17}	B	lapped	30	1.5×10^{17}	
49% HF	0.1% CM**	59	5.6×10^{17}	B	lapped	30	1.4×10^{17}	
49% HF	1% CM**	58	5.5×10^{17}	B	lapped	30	7.8×10^{14}	
49% HF	1% HCO_2H + 1% citric acid	58	5.5×10^{17}	B	lapped	30	5.0×10^{16}	
49% HF	1% EDTA-Na_2†	59	5.6×10^{17}	B	lapped	30	1.4×10^{17}	

* Solution/surface ratio only 0.4 ml/cm^2 Si which accounts for relatively low values.

** See Appendix for composition.

† Ethylenediamine tetra acetic acid disodium salt.

Table 7—Adsorption of Copper Ions from Water by Variously Treated Silicon Surfaces (Cu^{64} Used as Radioactive Tracer)

Copper Solution		Adsorbent Wafer			Immersion		Adsorbate	
Cu ppm (added)	Cu ions/cm^3 (added)	Dopant	Original Surface	Surface Preparation Prior to Immersion in H_2O-Cu^{64}	Temp. °C	Time (min.)	Cu atoms/cm^2	Distribution
0.00209	1.98×10^{13}	P	lapped	30 min 49% HF, H_2O rinsed	23	15	1.9×10^{12}	
0.0209	1.98×10^{14}	P	lapped	30 min 49% HF, H_2O rinsed	23	15	2.2×10^{13}	
0.209	1.98×10^{15}	P	lapped	30 min 49% HF, H_2O rinsed	23	15	1.9×10^{14}	
2.09	1.98×10^{16}	P	lapped	30 min 49% HF, H_2O rinsed	23	15	8.2×10^{14}	
2.09	1.98×10^{16}	P	lapped/ polished	30 min 49% HF, H_2O rinsed	100	30	1.6×10^{15}	uniform, but edges have higher concentration
2.09	1.98×10^{16}	B	lapped	1 min HF-HNO_3-CH_3CO_2H, H_2O rinsed	100	30	7.0×10^{13}	
2.09	1.98×10^{16}	B	polished	15 min 3% H_2O_2 100°C, H_2O rinsed	100	30	1.5×10^{13}	many dots, edges have higher concentration
2.09	1.98×10^{16}	P	lapped/ polished	15 min 3% H_2O_2 100°C, H_2O rinsed	100	30	5.4×10^{12}	uniform plus dots
2.09	1.98×10^{16}	B	lapped	15 min 70% HNO_3 100°C, H_2O rinsed	100	30	1.1×10^{13}	uniform plus dots, some localized heavy concentrations
2.09	1.98×10^{16}	B	polished	15 min 70% HNO_3 boiling, H_2O rinsed	100	30	1.5×10^{12}	many dots

acetic acid;** a 15-minute treatment decreased the copper deposit by 97%. Even more effective was the combination rinsing treatment consisting of HCl followed by an ultrasonic water rinse and, finally, by a 40-minute cascade rinse in deionized water at 100°C. The residue after this treatment was less than 1% of the initial, or 5.6×10^{13} Cu/cm^2. HNO_3 is capable of rapidly decreasing this residual concentration still further, but it obviously cannot be applied to mounted transistors because of metal corrosion.

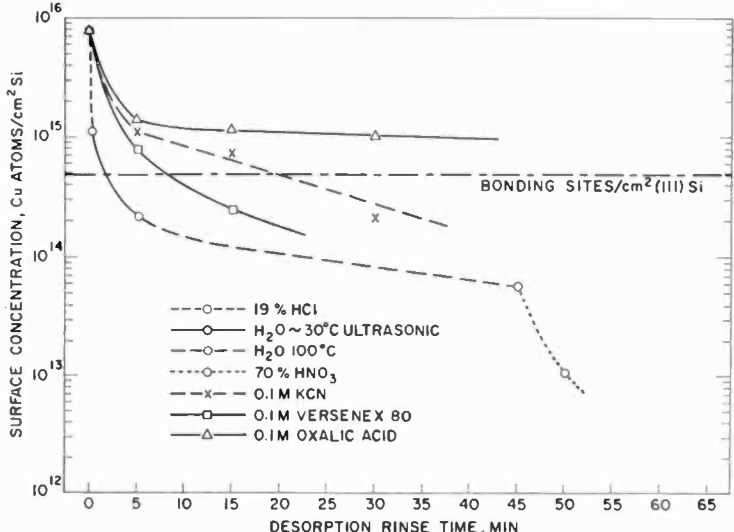

Fig. 2—Effectiveness of various agents for desorbing copper deposits from silicon. These adsorbates consisted of Cu^{64}-labeled Cu that had been deposited from hot 5% NaOH solution. Desorbing treatments were conducted at 23°C except for the water rinses (30°, 100°C).

The extent of contamination of silicon by copper from HF solutions is very great. It proceeds by electrochemical deposition leading to metallic copper even at low solution concentrations, as can be seen in Fig. 3. This graph shows the copper surface concentration on silicon (5 ohm-cm n-type, lapped/polished) as a function of solution concentration in 49% HF at room temperature after an immersion period of 30 minutes. The rate of deposition is very high initially (within the first 100 seconds) and decreases with increasing immersion time; this relation is shown in Fig. 4. Copper-free concentrated HF was used in these experiments as starting solvent; this HF

** Versenex 80, the Dow Chemical Company.

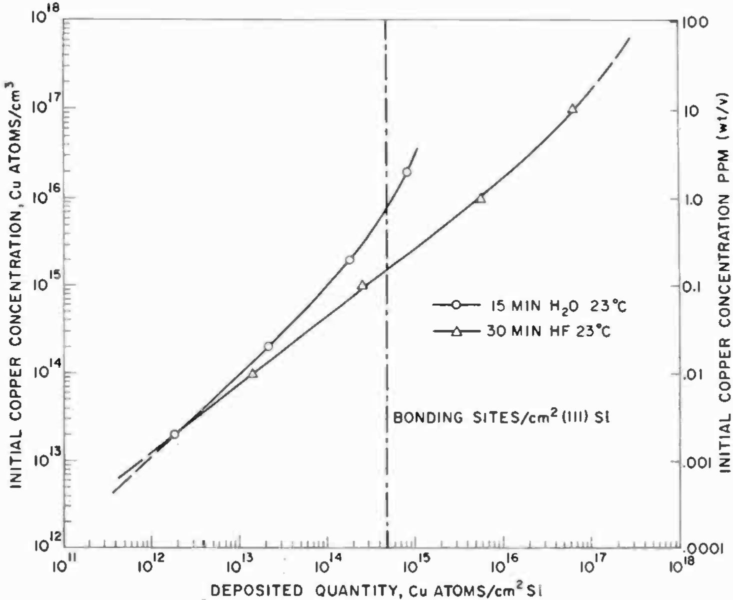

Fig. 3—Quantity of copper-deposited on silicon from HF and water as a function of copper solution concentration. The data for HF were obtained with specially purified copper-free 49% HF to which known quantities of Cu^{64} were added. The data for H_2O were obtained with deionized and distilled H_2O to which known quantities of Cu^{64} were added. Prior to immersion in this water, the wafers had been immersed in non-radioactive HF followed by rinsing in non-radioactive water.

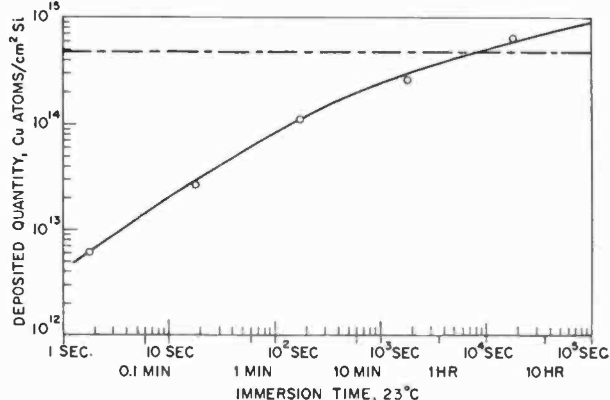

Fig. 4—Quantity of copper deposited on silicon from 49% HF as a function of immersion time. Concentrated HF with 0.1 ppm of radiocopper was used at a temperature of 23°C.

had been purified by filtration through a column of silicon powder by the technique published previously.[3] Known quantities (ppm weight/volume) of labeled cupric ions were then added to this purified reagent.

A summary of data for the deposition of radiocopper from concentrated HF, both pure and with the addition of various complexing and chelating agents, is presented in Table 6.* Inhibition of copper deposition by EDTA, citric acid, and formic acid additives to HF was negligible. A special mixture of chelating and surface active agents at a concentration of 1%, however, did decrease the deposition by a factor of 200. Extensive desorption studies of Cu^{64} from HF are discussed in the next Section.

Contamination by copper from rinse water was investigated by adding $Cu^{64}(II)$ ions to deionized and distilled water. Under these conditions the copper(II) can be expected to be complexed with oxygen forming a stable $[Cu(H_2O)_4]^{++}$ cation. The standard oxidation potential involving this compound indicates that electrochemical deposition onto silicon is possible, as is the case for all other copper reactions discussed here. In one series of experiments, silicon wafers that had been immersed in regular HF and rinsed with water were immersed in deionized and distilled water at 23°C to which 2 ppb to 2 ppm of radioactive copper had been added. The result is presented graphically in Fig. 3. The extent of copper deposition is remarkably high; this effect was certainly caused to a substantial extent by the fluoride ions that remained adsorbed[1] on the silicon during the preparatory HF treatment, thus enhancing the displacement plating.

In a second series involving Cu^{64}-containing rinse water, variously chemically treated silicon surfaces were exposed to the radioactive water at 100°C. These results are presented in Table 7. The elevated temperature approximately doubled the quantity of copper deposited at 20°C. Silicon pre-etched in $HF\text{-}HNO_3\text{-}CH_3CO_2H$ had 20 times less copper than silicon immersed in HF. This appears to be directly related to the lower fluoride concentration of etched silicon discussed in Part I of this work.[1] Silicon wafers pre-treated in oxidizing reagents all had distinctly lower copper surface concentrations than silicon that had been exposed to HF-containing reagents. Autoradiography revealed the presence of many locally concentrated areas (dots) of Cu^{64}; these might well represent pinholes and defects in the hydrous

* As indicated in Table 6, the ratios of the HF solution volume to silicon surface area in a few samples were such that the silicon depleted the copper in solution leading to relatively low quantities of adsorbed copper. Because of this stripping effect, accurate determinations of copper deposition require a large ratio of copper in solution to copper being deposited. This ideal condition could not be attained in the present study; the stated Cu/cm^2 values for HF should therefore be considered minimum values.

oxide film covering the silicon surface. These wet-chemically oxidized silicon surfaces approach the adsorption conditions observed for fused silica (Section 3.2.3).

3.2.2 Desorption of Copper Deposited on Silicon from Cu^{64}–Containing HF Solution

Silicon wafers that had been immersed in the radioactive 49% HF as described in the preceding sections were used for systematic desorption studies. Four initial concentration levels of deposited copper were chosen, ranging from 10^{17} down to 10^{15} Cu/cm^2. The samples were radiocounted, immersed in the desorbing solutions for the time and at the temperature specified in Table 8, dipped in acetone to facilitate drying, and recounted. The residual Cu^{64} surface concentrations were calculated as a percent of the initial value. These are listed in Table 8 for those agents that exhibited effectiveness. The most efficient formulations are those based on metal complexing with hot acidic hydrogen peroxide mixtures; with these copper desorption of better than 99% in 5 minutes was achieved. A more detailed discussion of these systems for use in silicon device technology is discussed in a separate paper.[5]

3.2.3 Adsorption of Copper on Fused Silica and Pyrex Glass Using Cu^{64} as Tracer

The contamination of fused quartz and Pyrex glass surfaces by copper from typical acids used to clean such containers in device processing

Table 8(a)—Desorption of Copper from Silicon with Various Complexing and Chelating Solutions.

Copper Concentration Levels:

Copper deposited from Cu^{64}-containing HF etchants resulting in the following initial (100%) surface concentrations:

Samples A: 1-2 × 10^{17} Cu atoms/cm^2
B: 3 × 10^{16} Cu atoms/cm^2
C: 2 × 10^{15} Cu atoms/cm^2

Reagent Solutions:

All solutions are in deionized and distilled water unless stated otherwise.

Ineffective Agents:

The following reagents (excluded from the table) were found ineffective or poorly effective for desorbing copper:

D.I. and distilled water (23°, 100°)
3% Hydrogen peroxide (23°, 90°)
Acetone (23°)
0.1 M Ethylene diamine tetra acetic acid disodium salt (23°)
1% Chelating mixture CM (23°)

was briefly examined. The samples were immersed for 15 minutes at 23°C in concentrated mineral acids to which 34 ppm radio-copper had been added. The etched samples were rinsed initially in three beakers of deionized water followed by one acetone rinse.

The data for fused silica are shown in Table 9. Even though a very high copper solution concentration was employed, the resulting concentration on the silica from HF was only 5×10^{12} Cu/cm^2, of which 85% could be desorbed by rinsing for 15 minutes with deionized water at 100°C. HNO_3 and aqua regia led to 1×10^{13} Cu/cm^2, of which 97 and

Table 8(b)—Desorption of Copper Deposited on Silicon

Desorbing Solution	Temp. °C	Cu^{64} Surface Concentration Level	Cu^{64} Residue (%) After			
			1 min	5 min	15 min	30 min
3% Hydrogen peroxide + 10% Formic acid	90	A	0.29	0.29	0.28	
3% Hydrogen peroxide + 10% Hydrochloric acid (1N)	95	B	1.2	0.85		
3% Hydrogen peroxide + 10% Acetic Acid	95	B	1.3	0.89		
10% Formic acid	90	A	44	8.6	0.80	
0.1M Potassium Cyanide	23	C		1.7	1.7	
0.1M Ethylene diamine tetra acetic acid disodium salt	90	A C	57	16 3.4	7.1 2.8	
1% CM (see appendix)	90	A	57	14	0.36	
0.1M Cupferon	90	C		4.1	3.3	
Sat. Ethylene diamine tetra acetic acid	90	A	72	36	0.10	
0.1M Monosodium N, N-di (β-hydroxy ethylene) glycine	90	C		4.6	4.0	
0.1M 8-Hydroxy quinoline in methyl alcohol	65	C		6.0	4.4	3.9
0.1M Pentasodium diethylene triamine penta acetate	90	C		4.9	4.7	
0.1M d-Tartaric acid	90	C		5.5	4.9	
0.1M Trisodium N-hydroxy ethyl ethylene diamine triacetate	90	C		6.7	5.3	
0.1M Oxalic acid	90	C		7.0	6.0	
0.1M Triethanol Amine	90	C		8.8	6.4	6.0
0.1M 2,4-Pentanedione in Methyl Alcohol	65	C		19	8.4	6.2

95%, respectively, could be desorbed in 15 minutes with 100°C water. HCl led to a slightly higher concentration, and the copper was adsorbed more strongly than from the other acids; only 60% could be removed after 15 minutes in 100°C water.

Table 9—Deposition of Copper on Fused Silica (Cu^{64} Used as Radioactive Tracer)

Reagent	Copper Solution		Immersion		Adsorbate
Solution Composition	Cu ppm (added)	Cu ions/cm³ (added)	Duration (Min.)	Temp. (°C)	Cu atoms/cm²
49% HF	34	1.1×10^{17}	15	23	4.6×10^{12}
37% HCl	34	1.1×10^{17}	15	23	2.1×10^{13}
70% HNO_3	34	1.1×10^{17}	15	23	1.1×10^{13}
Aqua Regia	34	1.1×10^{17}	15	23	1.1×10^{13}

Pyrex glass surfaces immersed under the same conditions in copper-containing HNO_3, aqua regia, and HCl retained 10 times less copper than the fused silica, about 1×10^{12} Cu/cm² (HF was not tested).

The very low degree of adsorption on these oxide and silicate surfaces, compared with semiconductor surfaces, and the relative ease of removal with hot water, suggests that the Cu(II) is adsorbed reversibly in ionic form. Following the usual cleaning of fused quartz furnace tubes with concentrated mineral acids, a thorough rinsing with hot deionized water should reduce copper contamination to negligible levels. Still better is immersion of the quartz or glassware in hot acidic H_2O_2 solution. This solution is capable of desorbing very effectively not only copper and other metal deposits,[5] but also gold, which cannot be removed by simple water rinsing (Section 3.1).

3.3 Contamination by Iron

Iron occurs in appreciable concentrations in "analytically pure" etch reagents, and the detrimental effects of iron in silicon devices are well known.[9,13,14] Concentrations are highest in sodium and potassium hydroxide, where levels up to 10 ppm are common. Sodium hydroxide solution is used for post-mount etching of some silicon power transistors and certain other silicon devices. The present radiochemical investigation was therefore centered primarily around iron contamination from this source.

The various reagents used in these studies were found to have the following initial iron impurity concentrations:

97% NaOH—2 ppm

HF-HNO_3-CH_3CO_2H etch mixture (4:8:10)—1 to 2 ppm

49% HF—1 ppm

70% HNO_3—0.2 ppm

CH_3CO_2H—0.2 ppm

37% HCl—0.1 ppm

Small aliquots of ferric chloride solution containing Fe^{59} were added to the reagents to yield total iron ion concentrations of 0.01 to 5 ppm. The iron in the original dilute HCl solution was present in the form of the acido-complex ion $(FeCl_4)^-$ which, on addition to NaOH, should form an amphoteric colloidal iron(III) oxide hydrate, such as $Fe_2O_3 \cdot H_2O$ or FeO(OH). The concentrations involved were such that the trace quantities of iron compound were largely soluble in the NaOH, forming sodium ferrate(III), $NaFeO_2$. Nevertheless, alkaline preparations were centrifuged before use to remove any hydroxide precipitates that might have been suspended in the solution.

All silicon wafers used as adsorbent were p-type, 6 to 8 ohm-cm resistivity, and (111) oriented. Following the etching treatments, all samples in the iron series described here were given an initial rinse sequence in 3 beakers of 20 ml deionized water each, followed by a methyl alcohol rinse. Each rinse duration was 5 seconds. The detailed experimental data and results are presented in Table 10.

3.3.1. Deposition of Iron on Silicon Using Fe^{59} Tracer

Silicon wafers immersed for 30 minutes in 19% HCl or 49% HF containing Fe^{59} showed low contamination levels of $1\text{-}3 \times 10^{11}$ Fe/cm^2. Diluted HF (0.5N) led to only 1/5 of this quantity. Silicon etched in HF-HNO_3-CH_3CO_2OH mixture had even lower concentrations (less than the radiochemical detection limit of 2×10^{10} Fe/cm^2, or 3×10^{-6} monolayer). The radioactive iron concentration in these acids ranged from 3.6 to 4.5 ppm.

Lapped silicon wafers etched for 1 minute in 5% (1.25N) NaOH solution at 100°C attained a smooth surface finish on which the iron was strongly adsorbed. The uniformity of the adsorbate distribution was poor in most cases, which may be a reason for the fluctuation in the data. The quantity of iron adsorbed by the silicon as a function of the iron concentration in the solution is shown in Fig. 5. The plot indicates that the solute/adsorbate relationship is roughly linear over at least three orders of magnitude. A solute concentration of 0.1 ppm leads to

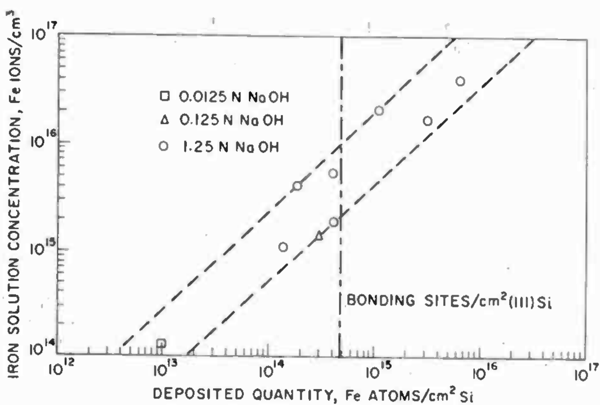

Fig. 5—Quantity of iron deposited on silicon from NaOH solutions at 100°C as a function of iron solution concentration. Fe^{59} was used as radioactive tracer in NaOH solutions of the concentrations indicated and for immersion periods of 1 min.

Table 10—Deposition of Iron on Silicon* (Fe^{59} Used as Radioactive Tracer)

Reagent		Iron Solution		Immersion		Adsorbate	
Solution Composition		Fe ppm (added)	Fe ions/cm³ (added)	Duration, Min.	Temp. °C	Fe atoms/cm²	Distribution
49% HF		4.5	4.9×10^{16}	30	23	1.3×10^{11}	
0.50N HF		3.6	3.9×10^{16}	30	23	2.6×10^{10}	
4 vol HF 49% + 8 vol HNO_3 70% + 9 vol CH_3CO_2H		4.0	4.3×10^{16}	1.7	23	$<2 \times 10^{10}$	
6.0N	HCl	3.7	4.0×10^{15}	30	23	2.8×10^{11}	
1.25N	NaOH	2.1	2.3×10^{16}	5.0	23	6.1×10^{13}	
0.0125N	NaOH	0.012	1.3×10^{14}	1.0	100	9.5×10^{12}	uniform
0.125N	NaOH	0.13	1.4×10^{15}	1.0	100	3.0×10^{14}	spotty
1.25N	NaOH	0.10	1.1×10^{15}	1.0	100	1.4×10^{14}	
1.25N	NaOH	0.18	1.9×10^{15}	1.0	100	4.2×10^{14}	spotty
1.25N	NaOH	0.37	4.0×10^{15}	1.0	100	1.9×10^{14}	
1.25N	NaOH	1.6	1.7×10^{16}	1.0	100	3.2×10^{15}	spotty
1.25N	NaOH	2.1	2.3×10^{16}	1.0	100	1.1×10^{15}	
1.25N	NaOH	3.7	4.0×10^{16}	1.0	100	6.4×10^{15}	spotty
1.25N	NaOH	0.5	5.4×10^{15}	1.0	100	4.1×10^{14}**	nearly uniform

* All adsorbents are lapped p-type Si wafers; 6-8 ohm-cm resistivity.
** Wafer etched in iodine etch before NaOH treatment.

an adsorbate concentration of about 1×10^{14} Fe/cm^2. The concentration of the NaOH does not appear to critically affect this relation. A wafer polish-etched in iodine etchant prior to treatment in the NaOH adsorbed iron to the same extent as the lapped wafers. The iron contamination resulting under nonetching conditions was tested by immersing a wafer in the solution at room temperature; 40 times less iron was adsorbed.

Desorption experiments with deionized water for silicon wafers etched in the hot NaOH solutions showed a low degree of iron removal; at 23°C a desorption half-time of 68 minutes was obtained. Treatment with iron complexing reagent solutions such as citric acid, or with metal chelating agents such as EDTA (ethylenediamine tetra acetic acid), had very little desorption action on the iron deposits. HCl, on the other hand, was found particularly effective in decreasing the iron surface concentration. As can be seen from the graph in Fig. 6, rinsing for 1 minute in 38% HCl diminished the contaminant by a factor of 10^4. Further rinsing in HCl had no effect on the residual iron layers of 6×10^{11} Fe/cm^2; diluted (19%) HCl was slightly less effective. Removal of the surface oxide with 49% HF diminished this residue an additional order of magnitude to below the detection limit. This indicates that practically all of the 6×10^{11} Fe/cm^2 was absorbed in the hydrated oxide layer covering the silicon.

Desorption for identically treated germanium is also shown in Fig. 6; this comparison indicates that the residual iron surface concentration is similar to that in silicon and does not depend markedly upon the initial surface concentration.

The following reaction mechanisms could account for the association of iron with silicon and germanium surfaces when etched in NaOH solution: (1) precipitation of colloidal iron oxide hydrate onto the sample surface; (2) physical adsorption of the $NaFeO_2$; (3) chemisorption of the $(FeO_2)^-$; and (4) electrochemical deposition as metallic iron.

Colloidal precipitation can be ruled out, since all solutions were thoroughly centrifuged for long periods of time before use, and contamination occurred with solutions of widely varying concentrations in an orderly fashion. Physical adsorption did not occur to a substantial extent, since the quantity of adsorbed iron decreased rapidly with decreasing temperature and the rate of desorption with water was low. The temperature dependence, the chemical behavior of the adsorbate, and the large electrochemical potentials between silicon and iron ions in alkali solution indicate that chemisorption and/or electrochemical deposition are the most likely mechanisms of deposition.

3.4 Contamination by Chromium Ions

Chromium occurs in etch reagents as another common trace contaminant and, therefore, deserves careful examination. In many instances its effects on devices are not as deleterious as sodium or copper ions. Because of their high oxidation-reduction standard potential, dichromate ions can, in fact, be beneficial for the device if introduced under controlled condition. For example, p-type silicon freshly etched in hot

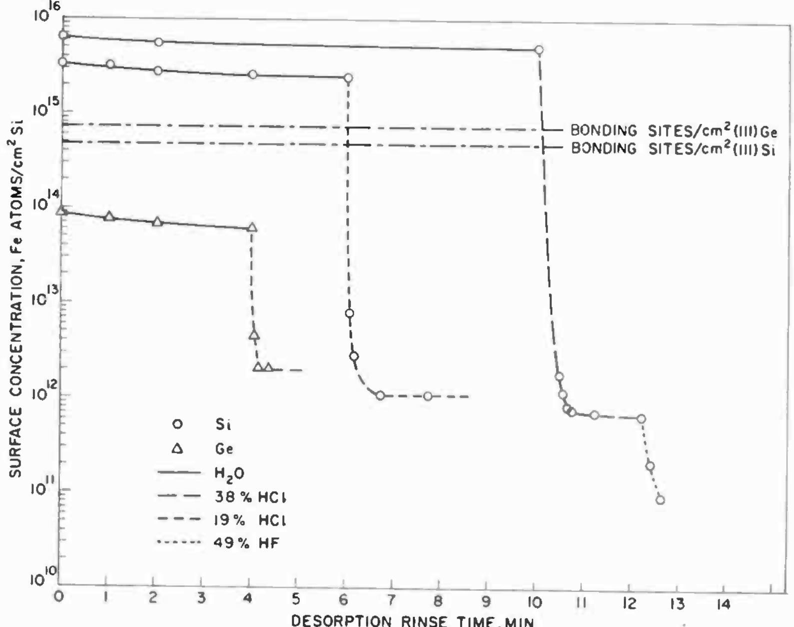

Fig. 6—Efficiency of various agents for desorbing iron adsorbates from silicon and germanium. Fe^{59} deposits from hot NaOH were used. All rinsing treatments were conducted at 23°C. Number of bonding sites for both Si and Ge are indicated for reference.

NaOH solution, followed by treatment with a dilute aqueous solution of sodium dichromate, can strongly adsorb dichromate ions, driving the p-type silicon to p^+-type. This can cause a decrease of the surface recombination velocity of the silicon and was demonstrated with diodes to reduce channel leakage at p-n junctions.[15,16]

The adsorption of chromium ions by silicon and germanium wafers from solutions of HF, mixtures of acid etchants,* and diluted hydrogen peroxide was examined in all solutions for a chromium ion concentra-

* Adsorption from chromic-sulfuric acid was discussed in Part I.[1]

tion of 2.5 ppm, with Cr^{51} serving as the labeling species. In the case of the acid etch mixture, this concentration represents a 12- to 25-fold excess over the chromium contamination normally present (Table 2). All the silicon wafers employed were (111) oriented, p-type, and of 3 to 9 ohm-cm resistivity. Following removal from the radioactive

Table 11—Deposition of Chromium on Silicon (Cr^{51} Used as Radioactive Tracer)

Reagent* + Cr^{51}	Adsorbent Wafer**		Immersion		Adsorbate	
Solution Composition	Initial Surface	Wafers Used	Duration Min.	Temp. °C	Cr atoms/cm²	Distribution
49% HF	polished/lapped	4	30	23	$2.21 \pm 0.32 \times 10^{14}$	uniform
49% HF + 1% CM†	lapped	1	30	23	4.5×10^{13}	localized dots
7 vol HF 49% + 3 vol HNO_3 70%	lapped	2	1.7	23	4.5×10^{12}	
7 vol HF 49% + 3 vol HNO_3 70% + 1% CM†	lapped	1	1.7	23	5.4×10^{12}	localized dots
Iodine Etch†	lapped	1	1.0	23	3.9×10^{12}	
3% H_2O_2	polished	1	15	23	8.7×10^{13}	localized dots
3% H_2O_2	polished	2	15	95	1.6×10^{15}	localized dots

* All solutions contain an added 2.3 ppm Cr; total Cr concentration is 3×10^{16} Cr ions/cm³.

** p-type Si; 5-9 ohm-cm resistivity.

† See Appendix for Compositions.

baths, all samples were rinsed initially by the usual 5 rinses of deionized water (20 ml per wafer, 6 seconds per rinse). This was followed by a 6-second dip in acetone to facilitate drying before commencing the radioactivity measurements and autoradiographic analysis. A summary of the experimental data is presented in Table 11.

3.4.1 Deposition of Chromium on Silicon Using Cr^{51} as Tracer

The chromium in HF solutions probably exists as a fluoride hydrate, such as the complex $[Cr\ (H_2O)_6]^{+3}[CrF_6]^{-3}$, which may be adsorbed by the silicon as the molecular species rather than as metallic chromium.

Silicon wafers immersed for 30 minutes in 49% HF attained, on the average, a concentration of 2×10^{14} Cr/cm^2. The addition of a mixture of surfactants and chelating agents to the tracer-containing acid reduced the surface chromium concentration by a factor of five. Less than 50% of these chromium adsorbates could be desorbed with deionized water, with or without surfactant addition at 95°C. Disodium ethylenediamine tetra acetate (Na_2EDTA) solution at 25°C, with and without surfactant, was also ineffective. However, acidic hydrogen peroxide at 90°C desorbed over 95% in 10 minutes.*

Silicon etched for 100 seconds in a mixture of Cr-containing HF-HNO_3 had an average surface concentration of 5×10^{12} Cr/cm^2. Additions of chelating and surface active agents to the etch did not prevent contamination. The same concentration was obtained in iodine etch; 60% of these layers could be removed by 5 minutes rinsing in cold water, but further rinses with hot water had no additional effect.

Immersing polished silicon wafers in 3% H_2O_2 containing 2.3 ppm of added Cr ions at 23°C for 15 minutes led to an average of 9×10^{13} Cr/cm^2, deposited as highly localized dots on the surface; whereas immersion at 95°C led to 2×10^{15} Cr/cm^2, similarly localized. The chemical composition of the adsorbate probably consists of a hydrated chromium oxide. The chromium ions in the H_2O_2 solution were certainly present in their original trivalent state, since oxidation to the hexavalent state requires the presence of strong acid or alkali in addition to hydrogen peroxide. Association of the chromium with the hydrated silicon oxide surface of the silicon was very strong and nearly irreversible. For example, disodium ethylenediamine tetra acetate solution at 25°C removed only 23% in 30 minutes. Immersion in HF resulted in removal of the surface oxide but of only 25% of the chromium deposits. Since the silicon oxide layers on and in which the chromium had been adsorbed was stripped by the acid, the chromium must have either remained as an insoluble residue or become redeposited on the oxide-free silicon surface. This observation shows that metal contaminants on or in silicon oxide surface layers can be transferred to the silicon surface when the oxide is stripped with HF, making this type of treatment rather critical, unless it is followed up by special treatment designed to dissolve and remove the metal impurities by complexing or chelating.

Adsorption of chromium compounds during etching of semiconductors in NaOH or KOH solutions was not investigated. A high degree of contamination can be predicted from the fact that addition of OH^-

* For a graphical presentation of these desorption curves see Ref. [5].

ions to a solution of Cr^{+3} ions results in the precipitation of chromic oxide hydrate, $Cr_2O_3 \cdot H_2O$. In addition, this precipitate is apt to contain absorbed alkali residues because of its colloidal nature. HCl forms soluble salts and should therefore remove most of the deposits, similar to its behavior in the desorption of iron deposits as discussed in the preceding section.

3.5 Contamination by Zinc

The adsorption of zinc ions from selected etch solutions was briefly investigated for silicon, silicon dioxide, and glass surfaces as adsorbents. The mechanism and extent of zinc deposition may serve as an example of a divalent metallic ion that exists in solution only with +2 oxidation state and, as will be shown, that exhibits weak and reversible adsorption behavior. This weak adsorption might be expected from the great tendency of zinc to form relatively stable complex ions, and from the standard electrochemical potential of the $Zn^o - Zn^+$ couple in acid solution, which is similar to that of the $Si(0) - Si(IV)$ couple.

3.5.1 Deposition of Zinc on Silicon Using Zn^{65} as Tracer

Aqua regia solutions containing additions of 1, 10, and 100 ppb of zinc tagged with zinc-65 were used as etchants. Silicon wafers were immersed in each solution for 60 seconds and then rinsed for 5 seconds each in three beakers of 20 ml deionized water per wafer. The radioactivity measurements indicated that the zinc adsorption was below 1×10^{10} Zn/cm^2. Several zinc complexes with chloride ions are known[17] that could account for the extremely weak adsorption behavior.

Similar experiments were made with 49%HF containing zinc-65. Again, the adsorption on silicon was very weak and readily reversible by water rinsing. The ZnF^+ complex that forms with F^- ions[17] is apparently responsible for preventing deposition.

3.5.2 Deposition of Zinc on Silicon Dioxide and Glass Surfaces

Pyrolytically deposited silicon dioxide films were etched in buffered HF solution tagged with zinc-65. Less than 1×10^{10} Zn/cm^2 were found. The same results were obtained for slides of soda-lime glass treated in the same manner.

The same negative results were observed for glass surfaces etched in radiozinc-containing 20% ammonium persulfate* indicating the oxide and glass surfaces adsorb less than 10^{-6} monoionic layer of zinc from the acidic reagents that were tested.

* Ammonium peroxydisulfate, $(NH_4)_2S_2O_8$.

3.6 Contamination by Antimony and Manganese

Both antimony and manganese introduce donor states into the conduction band edge in silicon. Antimony is a frequently used doping impurity in device technology. Manganese is known to be a rapidly diffusing element that reduces lifetime in silicon crystals.[8, 14, 18] A few experiments were carried out to examine the contamination levels that can be expected from these impurities during typical etching conditions.

3.6.1 Deposition of Antimony on Silicon Using Sb^{124} as Tracer

Sodium hydroxide solution was chosen as etchant mainly because traces of radioactive antimony had been detected previously on silicon wafers etched in neutron-activated NaOH during sodium contamination studies.[1]

A centrifuged solution 5% NaOH containing 1.4 ppm of antimony labeled with Sb^{124} was prepared. In these, lapped silicon wafers were etched at 95–100°C for 1 minute, followed by an initial water rinse sequence. A surface concentration of approximately 2×10^{13} Sb/cm^2 resulted; this is about 100 times less than observed for iron under the same conditions (Table 10).

Desorption with 19% HCl at 23°C decreased the adsorbed antimony to 33% of the initial value in 15 seconds, and 5.5% in 30 seconds. This residual quantity of 1×10^{12} Sb/cm^2 corresponds to 7×10^{-4} monolayer of antimony atoms.

3.6.2 Deposition of Manganese on Silicon Using Mn^{54} as Tracer

The difference between the standard oxidation potentials[19] for the Mn(0) – Mn(II) and the Si(0) – Si(IV) couples in acidic solutions is such that electrochemical deposition of manganese on silicon is not possible. One can therefore expect to encounter physical and hence easily reversible adsorption. This hypothesis is borne out by the experimental data.

$Mn^{54}Cl_2$ was added both in carrier-free form and with 0.1 ppm $MnCl_2$ as isotopic carrier to standard iodine etch solutions (composition as stated in the Appendix). Silicon wafers were etched in these solutions for 100 seconds, followed by a 30-second water rinse. A residual manganese concentration of less than 4×10^9 Mn/cm^2 of silicon was detected. In terms of monolayer quantities, this extremely low concentration is equivalent to less than 10^{-6} monoionic layer of manganese.

3.7 Deposition of Gold, Molybdenum, and Antimony from a Mixture

In the work discussed thus far, the fate of specific radioactive impurities has been examined one at a time. In reality, many types of impurities are being deposited simultaneously during semiconductor etching. Gamma-ray spectrometry makes it possible to examine several radioactive nuclides in a mixture, provided their gamma spectra are sufficiently different.

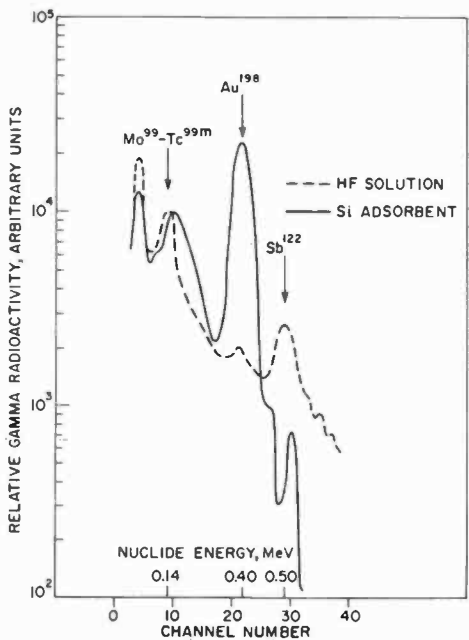

Fig. 7—Gamma radiation spectra of HF solution and silicon adsorbate. The relative distribution of radioactive molybdenum, gold, and antimony in the bath solution and in the resulting adsorbate on silicon is shown.

Gamma spectrometric analysis was carried out with a dilute (1N) HF solution containing gold-198, antimony-122, and molybdenum-99 (associated with technetium-99m). This solution had been used in fluorine-18 adsorption studies;[1] the residual radioactive impurities mentioned were identified after the flourine-18 activity had decayed. Although it was not possible to ascertain the absolute concentration of these impurities, comparative instrumental analysis of this HF solution and the adsorbates obtained from it led to some noteworthy results concerning the relative distribution of these impurities. These results are presented graphically in Fig. 7. The dashed curve shows the

gamma spectrum of the HF solution; the Mo^{99}-Tc^{99m} and the Sb^{122} pulse height peaks are readily visible, whereas the Au^{198} photon peak is minor. The solid curve was obtained from silicon wafers that had been immersed in this HF solution. The two spectra are normalized to give the same molybdenum-99 photon peak height to facilitate comparison. The relative distribution of the radioisotopes deposited on the silicon is seen to be different from that in the HF solution. The extremely high degree of accumulation of gold on the silicon is most striking. Antimony, on the other hand, is adsorbed by the silicon to a relatively small extent. It should be noted that these impurities were deposited in addition to flouride from HF plus other non-radioactive impurities.

4. Conclusions

1. Contamination of silicon surfaces by metallic impurities from reagent solutions is particularly severe in aqueous HF, which strips the protective layer of natural oxide without etching the semiconductor. The large difference between the oxidation potentials of the silicon and the metal ions in solution therefore becomes effective over the entire surface, leading to large quantities of electrochemically deposited Cu, Au, and Cr. The adsorption of Fe is much lower, and that of Zn is negligible.

2. Contamination of Si during etching in HF-HNO_3 containing etchants leads to somewhat smaller quantities of Au, 10-100 times less Cr, and 10^3-10^5 times less Cu than contamination from HF because of redissolution of the metal deposits. Mn ions become absorbed to a very low extent.

3. Adsorption of metal ions from concentrated mineral acids or from rinse water is low as long as the semiconductor is covered by a protective layer of oxide. Accordingly, adsorption on silica is also very low.

4. During etching of Si in hot NaOH solution, where the semiconductor surface is being dissolved, the contamination by Cu, Fe, and Au is very severe since the deposits accumulate. Contamination by Sb is much lower.

5. Inhibition of metal deposition by the addition of chelating agents to the solutions is generally not very effective.

6. Complexing by acidic H_2O_2 is the most effective method for removing metal contaminants including Au, Cu, Cr.

Acknowledgments

The author wishes to thank G. M. Loiacono for his competent technical assistance, R. F. Bailey for his help in preparing several of the radioactive isotopes by neutron activation, and G. Hornberger for the chemical analyses of reagents. Special thanks are due to A. Mayer for his critical reviewing of the original results, and to J. A. Amick for his helpful comments and suggestions on reading the manuscript.

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Appendix–Composition of Special Reagents

Iodine Etch

1.00 vol HF 49.5%

1.00 vol HNO_3 70.5%

1.40 vol CH_3CO_2H 100%

0.22 vol H_2O (introduced with tracer)

0.24% Triton – X100 nonionic surfactant (Rohm and Haas Co.)

0.15% Iodine Crystals

The ppm concentrations of radioactive impurities to this (and all other solutions) is on a weight/volume basis.

Chelating Mixture (CM)

This additive with chelating agents plus a surface active agent was designed primarily for use with HNO_3-containing etchants to inhibit the deposition of contaminants.

To prepare this formulation the following materials are emulsified by heating and mixing:

a) 20 ml Versenex 80, Dow Chemical Co.—(aqueous solution of pentasodium diethylenetriamine penta acetate).
b) 20 ml Versenol 120, Dow Chemical Co.—(aqueous solution of trisodium N-hydroxyethylene diaminetri acetate).
c) 10 g EDTA—(ethylenediamine tetra acetic acid).
d) 20 g Tergitol Nonionic NP 40, Union Carbide Co.—(nonyl phenyl polyethylene glycol ether).

The emulsion is cooled to room temperature and cleared by adding some HNO_3. The solution is then adjusted to 100 ml with deionized water.

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A New Technique for Etch Thinning Silicon Wafers

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Abstract—A novel technique for chemically thinning silicon wafers is described. Gas bubbles, rising from the bottom of the etching vessel, impinge on a float-mounted wafer in a random manner. When wafers are thinned with the apparatus and etch described, wafers having smooth, blemish-free surfaces, and a thickness uniformity of $\pm$ 0.1 mil, are obtained. A means of observing the light transmission through the wafer without removing it from the etch is also provided. This enables the end-point to be determined simply and accurately when wafers are being thinned to less than 1 mil.

Introduction

To fabricate certain semiconductor arrays, it is necessary that silicon wafers be uniformly thinned from a normal wafer thickness (5 to 10 mils) to 1 mil or less. Examples of such arrays are dielectrically isolated structures[1-4] and image sensor arrays.[5]

Normally, an isotropic acid etch (HF-HNO_3) is used for this purpose. However, during the etching, bubbles of gaseous reaction products such as NO_2 form on, and cling to, the surface, leading to nonuniform etching. To dislodge the bubbles, various agitation methods such as a rotating beaker have been used, but it is difficult to provide agitation and to control the flow pattern to give a uniform reduction in thickness over the entire wafer.

Described here is an etching apparatus and procedure that overcomes this problem by providing a completely random agitation, resulting in uniformly thinned blemish-free wafers when used with the isotropic etch developed for this purpose.

Apparatus

The appartus consists of a Teflon cylinder closed at the bottom and having a Teflon screen rigidly mounted just above the bottom. A suitable gas is bubbled up through the etching solution from beneath this screen, providing random agitation of the solution. The wafer to

be etched is waxed to the bottom of a Teflon cup, so that it floats just beneath the surface and the rising bubbles impinge upon it. The wafer holder bobs about randomly during etching.

Another feature of this apparatus is a protruding overhang on the etching chamber where the light transmission of the wafer can be observed so that the end point of the etching can be determined without removing the wafer from the etchant. Figs. 1 and 2 show a cross-sectional drawing and a photograph of this apparatus.

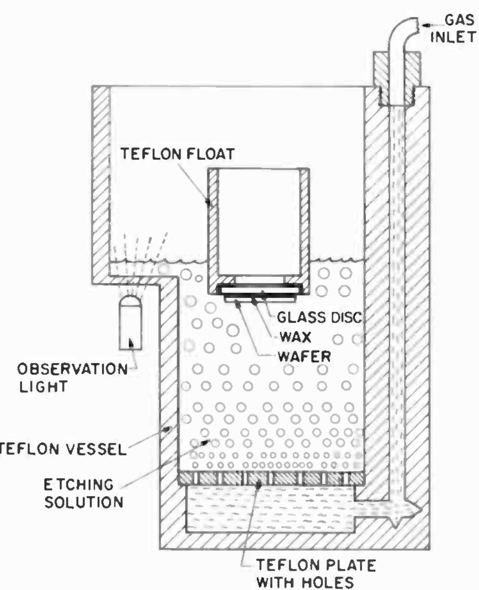

Fig. 1—Cross-sectional drawing of etching chamber.

Etchant

Initially, the etching solution used with this apparatus was a mixture of 7% by volume of 48% HF and 93% by volume of 70% HNO_3, with N_2 as the agitating gas. This combination produced wafers that were uniform in thickness, but whose surfaces were often quite rough. Fig. 3a shows a photomicrograph of a typical wafer after etching with the HF-HNO_3-N_2 systems.

At first, the agitating gas was thought to be chemically passive. However, further experimentation with several gases and gas mixtures indicated that certain gases did lead to better surface characteristics for the etched wafer. Specifically, CO_2, CO, and NO yielded the most

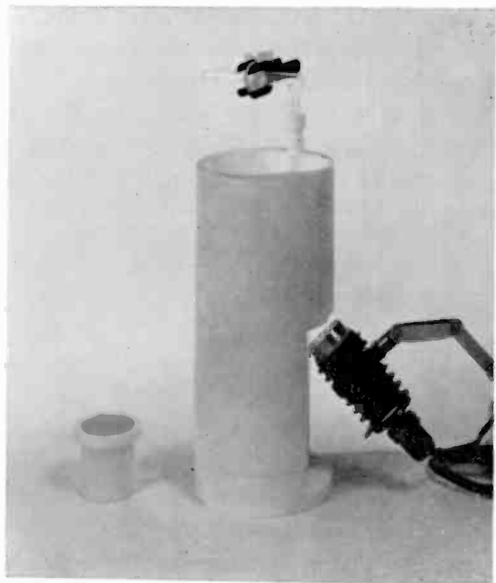

Fig. 2—Photograph of etching chamber.

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Fig. 3—Etched Silicon surfaces (oblique lighting): left, etched with HF-HNO_3 using N_2 bubbles; right, etched with preferred etch using CO_2 bubbles.

blemish-free surfaces, while N_2, O_2, NO_2 and Ar gave varying degrees of surface inhomogeneity, implying that the gas agitant can play a chemical, as well as physical role in the etching process.

An etch solution has been devised, for use with the apparatus described above, that produces smooth, chemically polished surfaces (see Fig. 3b). The composition of the preferred etch solution is:

70% Nitric Acid	90 ml
48% Hydrofluoric Acid	9.5 ml
Glacial Acetic Acid	0.5 ml
Sodium Chlorite, $NaClO_2$	1.4 grams
Carbon Dioxide	bubbled through the solution at 0.5 liter/minute

Although it was found that $NaNO_2$ could be substituted for the $NaClO_2$, the latter is preferred. The $NaNO_2$ imparts a reddish-brown color to the solution and liberates reddish-brown N_2O_4 gas, making it difficult to observe the light transmission of the wafers. With $NaClO_2$, the solution is a pale greenish yellow that does not obscure the light transmitted by the thinned silicon wafer.

The acetate acid was also found to be necessary in order to obtain blemish-free surfaces. However, if amounts larger than 1.0 ml were used in the preferred etch composition, a passivation layer formed that interfered with the etching. Such passivation layers have been previously reported[6] and identified as a fluorosilicate composition.

Procedure

The three acids are mixed together in the Teflon chamber, and the CO_2 gas is turned on. The solid sodium chlorite is added *slowly and carefully*, since considerable frothing takes place when it is added. When the frothing has subsided, the wafer, mounted on the float, is placed in the etch. The etch rate, about 0.6 mil/minute, has been found to be essentially independent of the wafer orientation and resistivity. The end point of the etching may be determined by timing if the wafer and mounting are not translucent. If, however, the silicon wafer is being thinned to less than 1 mil and the mounting is translucent, the end point may be determined by periodically moving the float into the illuminated overhang of the etching chamber and observing the color of the transmitted light. Due to the relatively gradual increase of the adsorption coefficient with an increase of the photon energy for silicon[7], the transmitted light changes in hue as the silicon wafer is thinned. With a 28-watt microscope light for illumination, the transmitted color

ranges from crimson red for 0.9-mil-thick wafers, to orange-red for 0.65-mil wafers, to yellow for 0.4-mil and under wafers. With some practice, it has been found possible to stop the etching reproducibly to a tolerance of about ±0.1 mil.

In this way, a thin wafer can be obtained without removing it from the etchant before completion. Such premature removal often leads to "stain films" and poor surface quality. When the etching is completed, the wafer is immediately flushed in distilled water and removed from the float.

It is important that the mounting wax be resistant to attack by the etching solution, otherwise the decomposed wax deposits on the wafer during etching, thereby degrading the surface. A pure paraffin wax (Bareco* Be Square 190/195 #1 white wax) has been found satisfactory.

Evaluation

An evaluation of the uniformity of etching was obtained by measuring silicon wafers with a Proficorder** along the same path, before and after etching. The wafers were (100) orientation, 20 mils thick, 1.4 inches in diameter, 3 ohm-cm n-type, Czochralski-grown material, one side lapped, the other polished. One wafer was etched on the polished surface, and another on the lapped surface. Etching times of 10 minutes were used to remove approximately 6 mils of silicon. Representative results of the Proficorder recordings before and after etching are shown in Figs. 4a and 4b.

The etched surfaces of the wafers were observed to be flat and specular with a short-range nonuniformity of 10 to 20 microinches independent of the surface finish on the starting wafer. The long-range deviation in wafer thickness is typically ±0.1 mil from the original thickness. For the fabrication of a variety of semiconductor arrays, such as dielectrically isolated structures, this is satisfactory.

Conclusions

An apparatus and an etchant have been developed for the uniform chemical thinning of silicon wafers. The approach involves the use of gas bubbles impinging on the surface during etching to ensure a continuous supply of fresh etchant and the continuous removal of reaction products. For silicon, a special etch has been devised to obtain defect-

* Bareco Division, Petrolite Corp., Ardmore, Pa.
** A product of the Bendix Corp.

free surfaces. Silicon wafers of 1¼-inch diameter can readily be thinned by 6 mils, while introducing less than 0.1 mil nonuniformity. When thinning silicon wafers to less than 1 mil, visual determination of the end point to tolerances of about 0.1 mil is obtained.

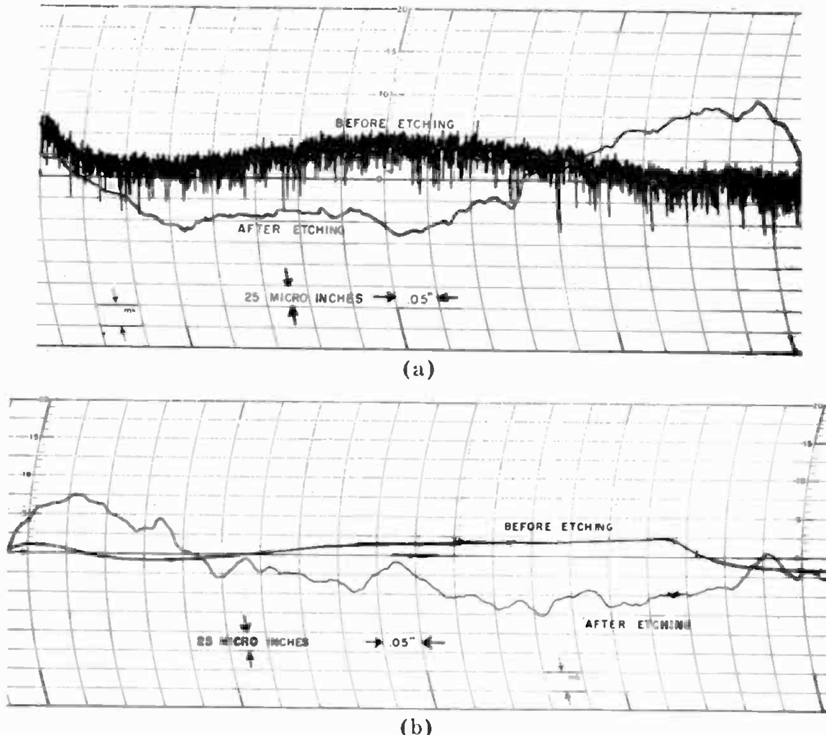

Fig. 4—Proficorder Graphs of surface roughness of a silicon wafer before and after etching: (a) initially lapped surface and (b) initially polished surface.

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The Etching of Deep Vertical-Walled Patterns In Silicon

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Abstract—A method of etching silicon has been developed that enables vertical walls to be etched. This development increases by at least an order of magnitude the ratio of etch depth to slot width, and also essentially eliminates undercutting of the mask. It is anticipated that this process will lead to the fabrication of isolated structures having component densities not previously attainable. Especially attractive is the possibility of fabricating image sensors using isolated single-crystal silicon bars (each containing a number of devices) at densities of 1000 lines per inch or greater.

Introduction

In the fabrication of dielectrically isolated structures in silicon (such as Beam Lead,[1] Double Poly,[2] Decal,[3] and Handle Wafer[4] structures), it is necessary to etch patterns into a silicon wafer. In general, relief patterns chemically etched into silicon surfaces have sloped sides or rounded channels, limiting the geometries that can be attained. The difficulty in providing deep, narrow grooves limits the component density that can be achieved in an array. A technique for chemically etching vertical-walled relief patterns in a silicon wafer has therefore been devised.

Limitation of Present Techniques

For dielectrically isolated array structures, two types of etch schemes are generally used:

(A) *Non-Selective Acid Etch, Usually* HF-HNO_3

This type of etch undercuts the etch mask in all directions to a distance approximately equal to the depth of the etching. If we assume a pattern of parallel bars and spaces, each of width (w), the limiting depth of etching is $w/2$. The etch mask at this point is completely undercut as shown in Fig. 1.

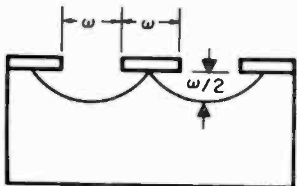

Fig. 1—Cross section of acid-etched silicon.

(B) *Crystallographically Selective Etch on (100) Wafers*

This type of etching has been described, for instance, in the etching of Beam Lead structures.[1] The mask is aligned so that the grid pattern in the mask is parallel to the intersections of {111} planes with the (100) surface. Since {111} planes are highly resistant to attack by caustic etches, they form the walls of the etched grooves. These {111} planes slope down and outward from the mask at an angle of about 54.7° as shown in Fig. 2. The limitation on the etch depth is reached when the walls of adjacent regions meet to form a V-shaped groove, and the etching stops. This occurs when the depth is about 0.7 times the mask opening. If a high component density (i.e., small center-to-center spacing) is required, as in the various types of dielectric or air isolation processes, the silicon must be made very thin to permit complete isolation to be achieved.

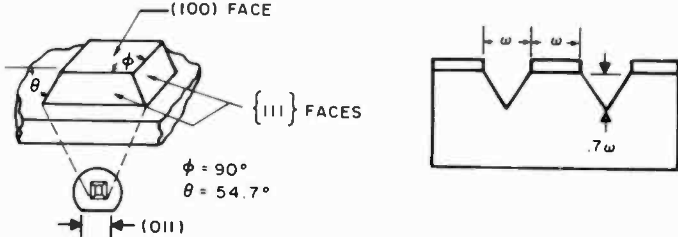

Fig. 2—Perspective and cross-sectional views of (110) surface silicon, crystallographically etched.

Vertical Wall Etching

It is both possible and practical, however, to etch deep patterns having walls almost exactly perpendicular to the surface. This is done by using a conventional caustic etch (i.e., KOH) with a silicon wafer having a (110) surface orientation. The straight lines of the mask must be

aligned parallel to the two sets of {111} planes that intersect the (110) surface vertically. Crystallography then requires that the geometry of the surface pattern be restricted to parallel bars or parallelograms as illustrated in Fig. 3.

A similar result was shown by Bean and Gleim[5] for the etching of shallow (0.12 mil) grooves in silicon by vapor-phase techniques.

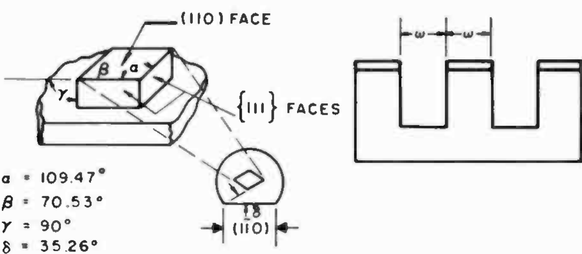

Fig. 3—Perspective and cross-sectional views of (100) surface silicon, crystallographically etched.

Experimental

A silicon wafer having a (110) surface orientation served as a starting point; as an etch, a boiling mixture of 100 g of KOH in 100 cc of H_2O was employed. A pattern of parallel bars, 0.5 mil wide on 1.0 mil centers was defined in a 1-micron thermally grown SiO_2 layer serving as the etch mask. Grooves about 2 mils deep were formed by etching for 6 minutes. A disk of Corning #7070 glass was hot pressed into the resulting grooves at 750°C at a few hundred psi. A photomicrograph of the array sectioned along a line perpendicular to the direction of the bars is shown in Fig. 4.* The silicon wafer was then lapped away from the back leaving the isolated bars of silicon embedded in the glass. Fig. 5 shows this array illuminated by light transmitted through the glass regions. The side etching in each direction is about 2 microns, while the depth of the etching is about 50 microns. Thus the ratio of depth to side etching is about 25:1.

Proposed Applications

All processes for providing dielectric isolation for integrated circuits or other silicon devices require that the silicon be separated into

* The V-shaped bottoms represent residual (111) and $(11\bar{1})$ planes; however, when wider grooves (i.e., 0.003 inch) are defined, these planes are not revealed, and a flat-bottomed groove, as sketched in Fig. 3, results.

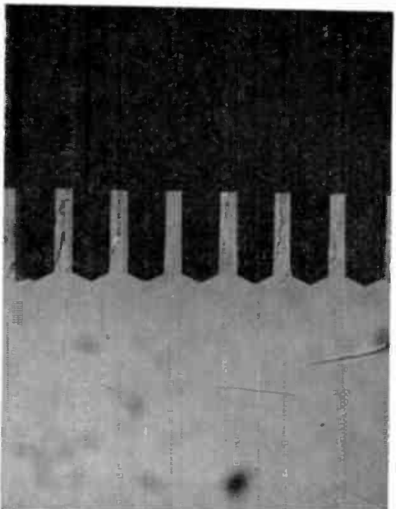

Fig. 4—Cross section of etched sample with glass refill (1000 bars per inch; light-colored portion is silicon).

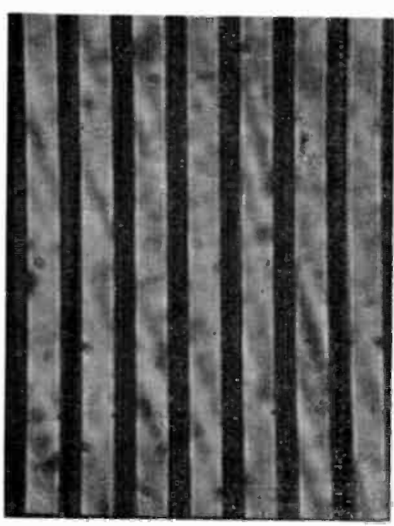

Fig. 5—Array of silicon bars isolated in glass (1000 bars per inch; dark-colored portion is silicon).

discrete regions, normally by etching. To achieve a high component density with (100) or (111) surface wafers, the silicon must be made very thin because of the aspect ratio limitations detailed previously. This is an expensive process, and when the component density exceeds a certain level, the required thickness uniformity cannot be maintained over the area of the wafer. When (110) surface wafers are employed, this constraint is minimized. Specifically, this process should be applicable to the fabrication of Decal and Handle Wafer types of circuits. Also, it should enable improved Beam Lead structures to be fabricated, especially of the types that provide for dielectric isolation between the individual components. Because of the structural integrity required, the thickness of the silicon in the Beam Lead type of circuit cannot be less than about 2 mils. This restriction limits the component density attainable with conventional processing on (100) wafers. Vertical etching would relax this restriction and permit the fabrication of more densely packed and/or more mechanically sound Beam Lead circuits.

High-density components are also required for other solid-state silicon arrays, such as those used in fabricating image sensors. With the technique described here, a density of 1000 bars/inch or more is attainable.

Conclusions

A technique for etching (110) surface silicon wafers has been developed that enables vertical walls to be formed. This increases by at least an order of magnitude the ratio of etch depth to groove width that can be attained, and also essentially eliminates undercutting of the mask. It is anticipated that this process will lead to the fabrication of isolated structures having component densities not previously attainable.

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Evaporation of Aluminum with rf-Induced Substrate Bias

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Abstract—DC sputtering with rf-induced substrate bias has been shown useful for the deposition of metals that do not recrystallize easily. It is shown that, by changing the deposition source from dc sputtering to thermal evaporation, easily recrystallized metals such as Al may be deposited with the beneficial effects of the substrate bias. Al films produced by this technique are fine-grained smooth polycrystals. The film resistivity is a few percent higher than bulk values. The interface between the film and its substrate is kept very clean by the action of sputter etching before and during deposition. Direct ohmic contacts to silicon can be made without the need for sintering. In addition, several competing phenomena in the discharge may be combined to effect a compromise, allowing one to coat over very steep edges uniformily, even when an edge is not in the line of sight of the vapor stream.

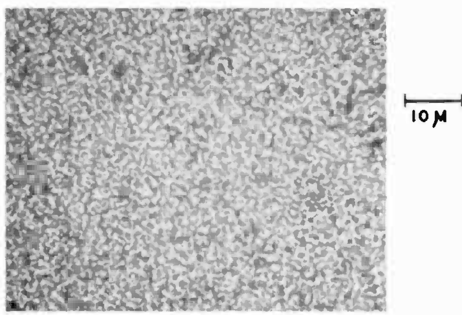
Introduction

Recently, dc sputtering with rf-induced substrate bias[1] has been shown useful for the deposition of a variety of metals. The process is generally applicable to refractory metals. However, metals having low temperatures of bulk recrystallization exhibit grain growth and, in some cases, grain boundary oxidation when deposited in this fashion. Aluminum, being very active chemically and having a very low temperature of bulk recrystallization (150°C)[2], yielded very grainy films when deposited by sputtering with rf-induced substrate bias. It was shown that Al films deposited at very low rates (10 Å/min) were relatively fine-grained, while films deposited at 50 Å/min were extremely coarse grained with extensive grain boundary oxidation (Fig. 1).

The fact that the films deposited at 10 Å/min and those deposited at 50 Å/min had the same applied substrate bias suggests that the cause of graininess is the energy of the source (dc sputtering) rather than the rf-induced substrate bias. To test this hypothesis, the deposition source was changed from dc sputtering to thermal evaporation—

atoms evaporated by this technique have much lower average kinetic energy.

A. FINE GRAINED AT 10 Å/MIN., 50 V. BIAS.



B. COARSE GRAINED WITH GRAIN BOUNDARY OXIDATION AT 50 Å/MIN., 50 V. BIAS.

Fig. 1—Microstructure of Al films dc sputtered with rf-induced substrate bias (after Ref. [1]).

In concept, thermal evaporation with an rf-induced substrate bias is very similar to the "ion plating" technique described by Mattox,[3,4] except that an rf-induced substrate bias is used instead of a dc bias. When insulating substrates are employed, the use of rf allows a pulsating negative bias to exist on the substrate from the onset of deposition, while with dc bias, no effect is evident until the film is nucleated to the point of being electrically continuous. The beneficial effects of the rf-induced bias have been discussed previously.[1]

Recent investigations of the structure and properties of thermally evaporated Al films have illustrated many of the subtle problems that are inherent in the process.[5-13] Grain growth,[5,12,13] hillock formation,[5,6] whisker growth,[5] electromigration,[7,8,14-17] poor adhesion,[7] rapid recrystal-

lization,[2,9] high resistivity,[18] and surface oxidation[10,11,19] are but a few of the problems encountered with Al films.

The use of an rf-induced substrate bias during thermal evaporation of Al alleviates some of the process difficulties. It cannot, of course, change any of the chemical properties of the metal itself. The emphasis in this work is on structure, resistivity, surface morphology, and the interface between the metal film and the substrate.

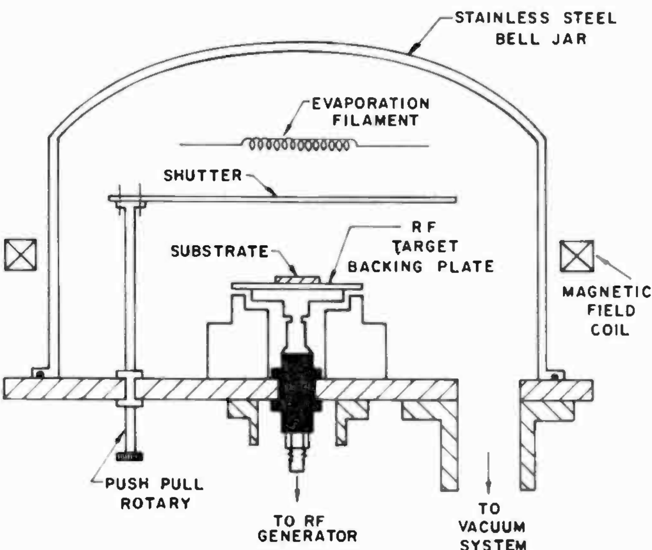


Fig. 2—Cross section of the apparatus for evaporation with rf-induced substrate bias.

Equipment and Experimental Techniques

Fig. 2 shows a cross-section of the appartus used in these investigations. The rf target assembly, which is used as a substrate platform, has been described previously.[20] An evaporation filament is suspended above the rf target and a movable shutter is interposed between the filament and rf target. An external magnetic field coil is sometimes employed to confine and intensify the rf discharge by constraining the discharge electrons to follow a helical path.

The disposition of the filament above the substrate in this apparatus requires that the evaporant wet the filament. Crucible-type sources cannot be used without substantial modification of the appartus. Since it is not desirable to use clamps to support the substrate in any other position, the rf target must be located as shown in Fig. 2. Any clamps

on the substrate surface act as high field points in the discharge, resulting in nonuniform substrate bombardment.

The problems involved in evaporating Al from a filament that has been wet by Al are well-known.[21] The main difficulty is the rapid diffusion of impurities from the bulk of the filament when the evaporant alloys with the filament material. These impurities are subsequently evaporated and become incorporated into the deposited film. This effect can be reduced by pre-evaporation onto the shutter before deposition onto the substrates. The filaments used in this study are stranded tungsten spirals. The Al was more than 99.9% pure as determined by emission spectrographic analysis. The major impurities were Si (0.05%), Cu (0.01%), Fe (0.02%), Mn (0.0005%), and Ti (0.01%).

In this investigation, all depositions were conducted with the following sequence of operations:

1. The bare filaments are resistance heated in vacuum to remove surface contamination, and then they are wound with a fixed length of Al wire.
2. The filament is then clamped into the support arms (not shown in Fig. 2). The substrates are ultrasonically cleaned in methyl alcohol, spun dry, and placed on the rf target backing plate. (The backing-plate material is aluminum).
3. The vacuum system is pumped out to a pressure less than 5×10^{-6} Torr, and the aluminum is melted onto the tungsten filament at a temperature higher than that to be used during the subsequent deposition. The filament is then turned off.
4. Argon is introduced into the vacuum system to a pressure of 2.5 ± 0.5 millitorr, and the substrates are sputter-etched at an average sheath potential of -700 V for 10 minutes.
5. The rf-induced substrate bias conditions to be employed in the deposition are established without turning off the rf power, (i.e., the average sheath potential, magnetic field, and argon pressure are adjusted).
6. The filament is then heated to remelt the Al, and the desired filament power is established.
7. The shutter is then opened and deposition proceeds.

The filament power was fixed at a level that yielded an Al deposition rate of $3000 \pm 10\%$ Å/min, and the deposition time was 2 minutes. Most of the depositions were conducted at an Ar pressure of 2.5 ± 0.5 millitorr, and this pressure is to be assumed unless otherwise indicated. Similarly, most depositions were run without a magnetic field. For the most part, the only processing variable was the average level of the rf-induced substrate bias.

Results and Discussion

Resistivity

The film resistivity, as measured by standard four-point probe techniques, averaged 3.1 microhm-cm for average rf bias levels from −100 to −750 V. With no bias applied, the resistivity averaged 3.6 microhm-cm. The 3.1 microhm-cm figure is approximately 3.2 to 3.5% higher than the values cited for bulk Al in various handbooks. No dependence upon bias voltage was observed in the interval studied (−100 to −750 V). This behavior is in sharp contrast to that of metals that are *sputtered* with an rf-induced substrate bias.[1] Similarly, this behavior differs from that found when Al films are rf-sputtered with a negative substrate bias[22] and when Al films are rf sputter etched.[23]

The Aluminum–Substrate Interface (Ohmic Contacts to Silicon Diodes)

Because the substrates are sputter etched immediately prior to deposition, a very clean interface between the Al and its substrate would be expected. However, under the sputter-etching conditions described above, the surface cannot be kept atomically clean because the rate of Ar^0 diffusion to the surface exceeds the rate of Ar^+ bombardment of the surface.[24] A surface heavily sorbed with a noble gas is to be preferred to a surface contaminated by oxides, cleaning-solvent residues, etc.

In addition, when the rf-induced bias is applied during deposition, the film is constantly "scrubbed" as it is grown. This should result in the de-sputtering of loosely bonded material arriving at the substrate, yielding films that have high adhesion and low pin-hole densities.

The most immediate illustration of the cleanliness of the interface is the direct formation of ohmic contacts to silicon diodes. It is well-known that thermally evaporated Al films do not make ohmic contact to Si unless they are sintered, usually at temperatures between 250°-550°C.

Several wafers of planar diodes were fabricated. All had the same geometry, but half had 2-ohm-cm p-type top contacts and half had 2-ohm-cm n-type top contacts. The wafers were quartered. Platinum silicide was formed in the contacts of one quarter of each wafer by conventional methods.[25] These quarters were used as control samples. Al was evaporated onto the other quarters. Fig. 3 shows the forward voltage drop at 10 mA forward current as a function of rf-induced substrate bias for the samples as deposited. In the bias range: −400

to −600 V the contact is indistinguishable from the platinum silicide controls. If no sputter-etching of the substrate and no rf-induced substrate bias is used, the forward voltage drop averages about 1.3-1.4 V at 10 mA forward current. Clearly, the sputter-etching before deposition plays the major role in ensuring intimate Al–Si contact. When the substrate is sputter-etched but not biased, the forward voltage drop is 0.75 V. The decrease in voltage drop with increasing bias is small by comparison (Fig. 3), but the effect of the bias is still evident.

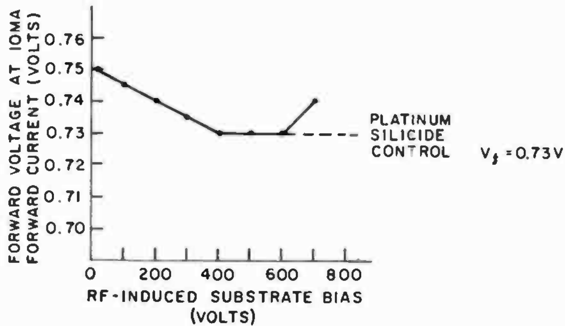


Fig. 3—Forward voltage-drop at 10 mA forward current (n/p and p/n) diodes).

Adhesion and Pinhole Density

Films deposited on fused silica and $(1\bar{1}02)$ sapphire were examined for pinhole density by scanning the substrates raster-fashion with an optical microscope, using transmitted light, at a magnification of ×100. No pinholes were detected in any film regardless of whether or not an rf-induced bias was applied during deposition. This is taken as further proof of the efficacy of rf sputter etching prior to film deposition.

Upon mild temperature cycling (25°C to 300°C to 25°C in one hour), pinholes were observed in the samples deposited at bias levels from the floating potential (typically −4 V) to −200 V and from −600 to −750 V. None appeared in the films deposited between −300 and −500 V.

The formation of pinholes is interpreted as resulting from poor adhesion. Rosenberg and Berenbaum[7] have shown that locally poor adhesion is largely responsible for pinhole formation and is, in part, responsible for electromigration in Al films. The effect of the substrate bias seems to be related to the immediate de-sputtering of loosely bonded material arriving at the substrate surface.

Crystallography

X-ray diffractometer traces indicate that the films are randomly oriented polycrystals with some slight {111} preferred orientation. However, at bias levels greater than −700 V, the {111} preferred orientation becomes quite pronounced. Above this level recrystallization and grain growth become evident in the films.

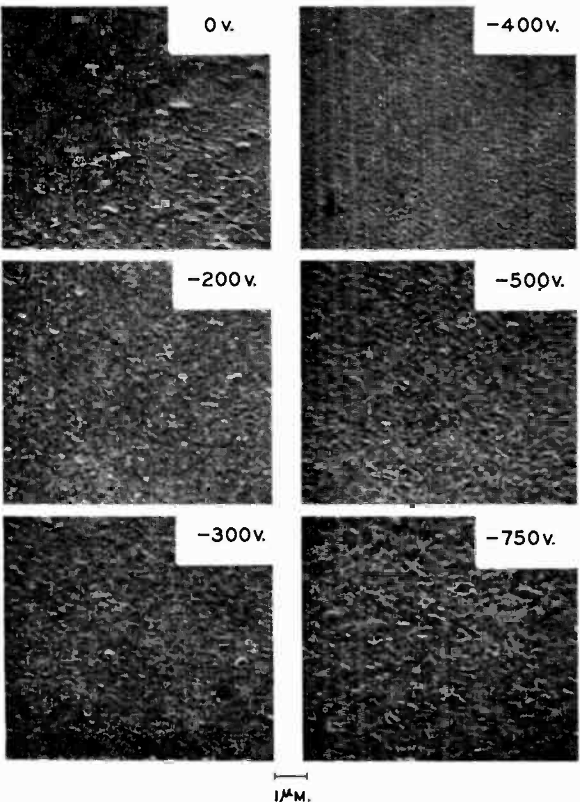


Fig. 4—Surface morphology of Al films vs. substrate bias.

Surface Morphology

Fig. 4 is a series of scanning electron micrographs of Al films deposited on oxidized silicon wafers at various substrate bias levels. At low bias levels, there is evidence of incipient hillock formation and some microscopic pitting. As the bias level is increased, these defects become less evident. The smoothest film is that deposited at a −400 V bias. A higher magnification view of this same film is shown in Fig. 5. Above

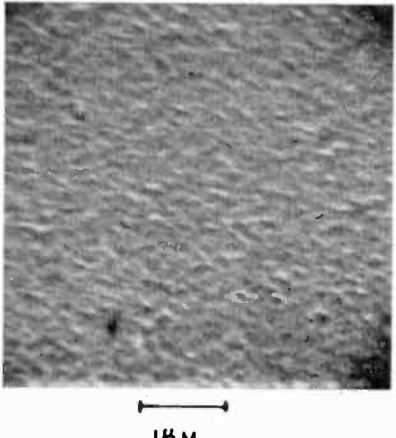


Fig. 5—Enlarged scanning electron micrograph illustrating the surface smoothness of films deposited at −400 V bias.

−400 V bias levels, the surface begins to roughen again as grain growth sets in.

Coating Over Steep Edges

Seeman[26] has shown that it is possible to coat the inside walls of deep narrow cavities very uniformly by dc bias sputtering. We have observed similar behavior when sputtering with rf-induced substrate bias. To determine whether the same uniform coatings can be applied during evaporation with an rf-induced substrate bias, silicon wafers were oxidized to a thickness of 10,000 Å, photoresisted, and sputter etched to form the grid pattern shown in Fig. 6. Sputter etching pro-

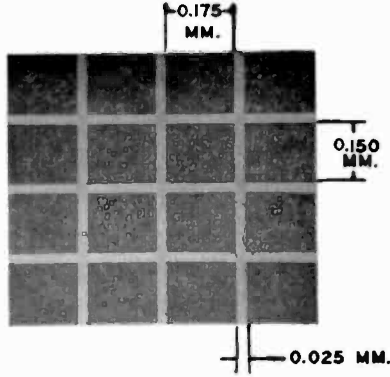


Fig. 6—Sputter-etched grid pattern (Light lines are Si, rectangles are SiO_2).

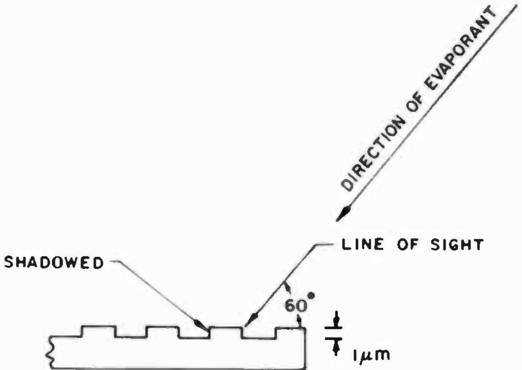


Fig. 7—Disposition of the substrate with respect to the filament to produce a line of sight and a shadowed edge.

duces nearly vertical side walls,[20,27,28] a worst case for coating processes such as evaporation. The direction of evaporation was purposely arranged so that one side wall of the grid pattern was in the line of sight, while the opposing wall was shadowed (Fig. 7).

The photoresist used during the sputter-etching of this grid pattern was not sufficiently thick to etch through the 10,000 Å oxide. As a result, the oxide surface remaining after sputter-etching had a rough appearance (Fig. 8). To coat these surfaces uniformly is more difficult than to coat a smooth surface.

Seven different sets of conditions were used to separate the effects of argon pressure, substrate bias, and magnetic field. Increasing argon pressure and magnetic field increase the current density of the rf-

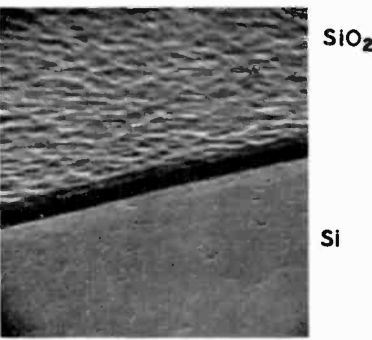


Fig. 8—Roughened SiO_2 after sputter etching due to thin resist (step height = 10,000 Å).

Table 1—Pressure-Bias Conditions and Results (LOS = Line of Sight)

Condition	Pressure (millitorr)	Average Substrate Bias (volts)	Magnetic Field (gauss)	Results
1	0.005	0	0	Shadowed edge not coated; LOS edges coated.
2	2.5	0	0	All edges coated.
3	2.5	−400	0	All edges coated.
4	2.5	−400	25	All edges coated.
5	10.	0	0	Shadowed edge not coated; LOS edges coated.
6	10.	−400	0	No edge coated.
7	10.	−400	25	All edges coated, but non-uniformly. Film very rough.

induced substrate bias and the probability that the metal species being evaporated will be ionized.[29]

The film edges were examined in a scanning electron microscope after deposition. If the edge is fractured, or has no Al on it, the edge charges up in the electron beam, yielding a very high light level in the micrographs (Fig. 9). In these micrographs, a corner of the grid pattern is examined. One edge shown is the shadowed edge and the other is an edge parallel to the direction of the vapor stream. The pressure and bias conditions used for these runs and the results are shown in Table 1.

A. HIGH VACUUM, NO BIAS.

Fig. 9a—Scanning electron micrograph of Al evaporated over sputter-etched edges at 0.005 millitorr with no bias (magnification = 10,000×).

Since conditions 2, 3 and 4, in Table 1 gave the best results in this preliminary examination, they were investigated further by etching a stripe in the Al film normal to the steep edge. Then, the side walls of the Al films were examined in the scanning microscope to determine the relative thickness of Al on the side walls of the step as compared to the thickness on the plane surfaces. Figs. 10 to 12 show the side walls of these films as they go over the steep edge on the line of sight and shadowed sides of the rectangle. The cracking that is evident near some edges is thought to be due to seepage under the photoresist of the chemical etchant used to define the Al stripes.

Clearly, the best conditions for coating over the edge comprise a

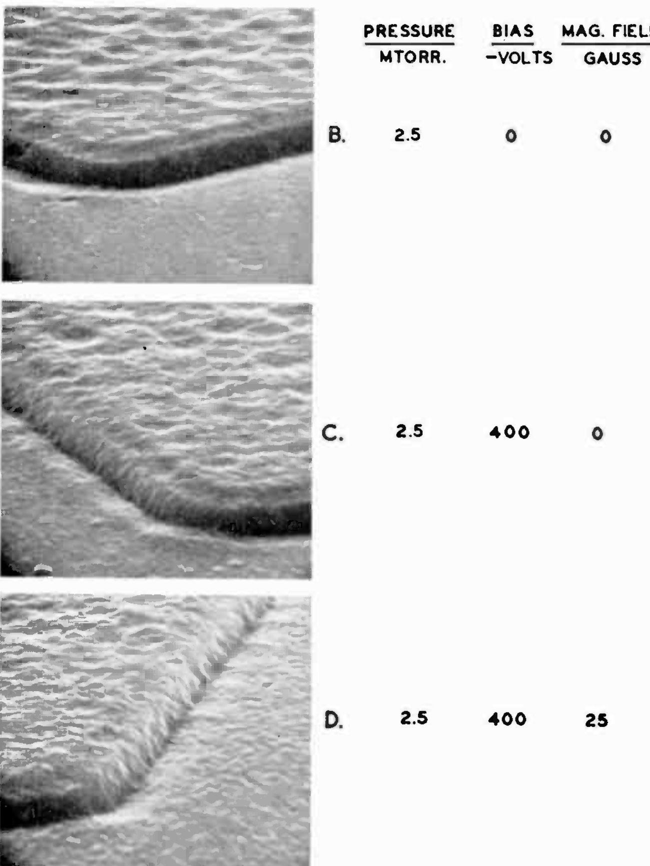


Fig. 9b-d—Scanning electron micrograph of Al evaporated over sputter-etched edges at 2.5 millitorr (magnification = 10,000×).

moderately high pressure (2.5 millitorr), a −400 V bias, and a moderate magnetic flux density (25 gauss). When no magnetic field is used with the bias, or when no bias is used at all, the side wall thickness of the shadowed edges is thinner than the film on the plane surfaces.

Considering the effect of pressure alone, when no bias is applied, it is evident that a moderately high pressure (2.5 millitorr) produces films that coat over edges better than films deposited under high-vacuum conditions. However, films deposited at even higher pressures (10 millitorr) do not exhibit the same uniformity over the edges. Because of scattering of the evaporant by a high gas pressure, one would expect to find progressively more coating uniformity with increasing pressure.

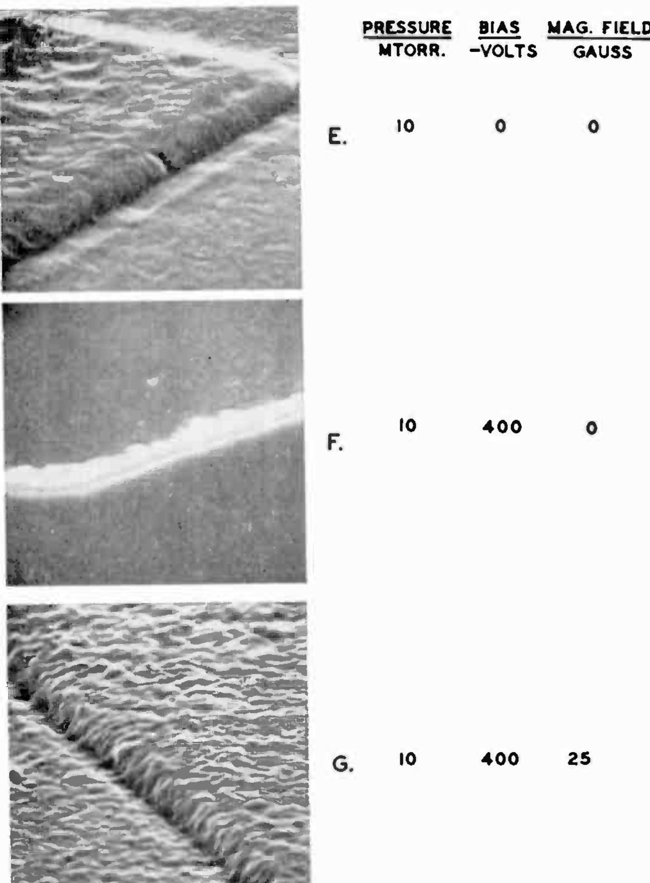


Fig. 9e-g—Scanning electron micrograph of Al evaporated over sputter-etched edges at 10 millitorr (magnification of E and G = 10,000×; F = 5,000×).

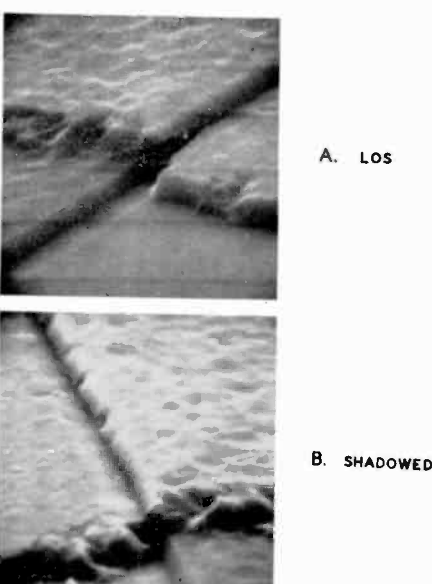


Fig. 10—Scanning electron micrograph of Al film cross section over a sputter-etched edge (argon pressure = 2.5 mtorr., bias = 0, $B = 0$).

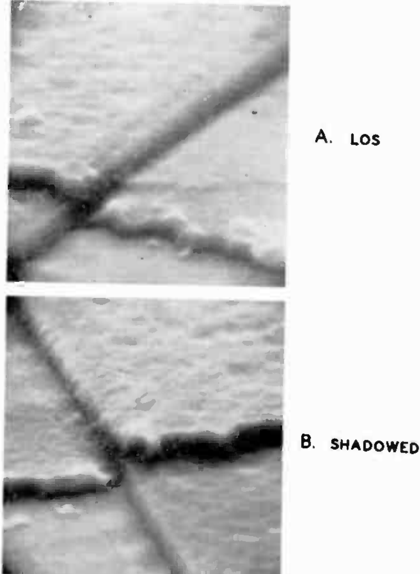
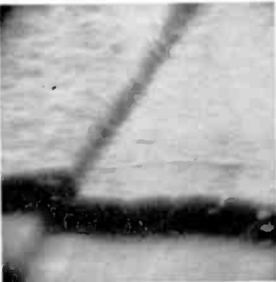


Fig. 11—Scanning electron micrograph of Al film cross section over a sputter-etched edge (argon pressure = 2.5 mtorr., bias = −400 V, $B = 0$).

Such is the case only up to a point. The decreasing ability to coat over the steep edge when very high pressures are used must be related to gas occlusions in the film, which would tend to weaken the structure and allow cracks to form in it near the sharp edges. When the film is sputter etched during deposition at high pressures, these structural weaknesses become quite apparent (condition 6, Table I and Fig. 9f). The effect of more vigorous sputter etching during deposition at 10 millitorr (by superimposing a magnetic field on the substrate bias) must tend to outgas the film, providing some coating over the edge. However, the massive outgassing leaves a very rough surface as a result of collapsing gas pockets (Fig. 9g).

A. LOS



B. SHADOWED

Fig. 12—Scanning electron micrograph of Al film cross section over a sputter etched edge (argon pressure = 2.5 mtorr., bias = −400 V, B = 25 gauss).

At more moderate pressures (2.5 millitorr), where less gas is to be expected in the films, all edges are coated; but the coating becomes progressively more uniform as the discharge current is increased by the magnetic field. Since the edge represents a high-field point in the discharge, the bending of the equipotential lines at this edge results in a higher current density discharge in this region than exists on the plane surfaces (Fig. 13). But a higher current density, of and by itself, implies more sputter etching and, hence, a *thinner film* in the vicinity of the edge. Our observation of a thick film on the edge is

inconsistent with the higher current density in this region unless a substantial fraction of the species bombarding the surface are Al ions. If a substantial fraction of the evaporant is ionized in transit to the substrates, the Al ion current density would be increased in the vicinity of the steep edge, thus depositing a thicker film there to counteract the effect of increased sputter-etching. Furthermore, Al ions would be accelerated toward the substrate at an average energy of 400 eV (peak energy = 1700 eV), leading to shallow implantation of the Al. This implantation theory is consistent with the observations that ohmic contacts are formed *in situ,* and that the films are very adherent and pinhole free.

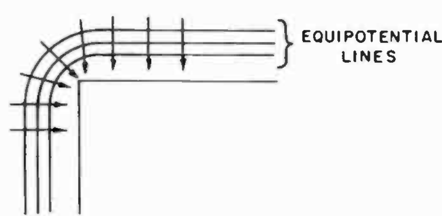


Fig. 13—Bending of equipotentials at a high field point.

The conditions existing in the apparatus are favorable to the formation of Al ions, especially in view of the low ionization potential of Al (5.984 eV) as compared to that of Ar (15.755 eV). The metal is in the gaseous state, an rf discharge of sufficient intensity to ionize Ar is present in the vapor stream, and the magnetic field constrains discharge electrons to a helical path to increase the ionic density of all species present. We have observed metal ions spectroscopically when metal targets of Ag, Au, Cr, Cu, Mg, Mo, Ni, Pt, Rh, Ta, and Ti were rf sputtered with similar discharge parameters. Stuart and Wehner[19] utilized the ionization of sputtered materials to determine sputtering yields. The conditions under which these yield studies were conducted were similar to those in the present investigation. During a run, whenever the shutter was opened between the filament and the rf target, the sheath potential at the target was observed to decrease slightly (5 to 20 V). Since this potential is generated by discharge electrons on the target surface,[30,31] the only way in which it can be reduced to a lower negative value is to increase the number of positive ions arriving at the surface. If the Al is partly ionized in the discharge, the Al+ arriving at the rf target would recombine with the electrons there and, hence, decrease the potential to a smaller negative value.

Seeman[26] speculated that uniform edge coatings are obtained in dc

bias sputtering by the re-deposition of material sputter etched from the plane surfaces at a small angle. It is very likely that this mechanism is operable as well.

These results indicate that there are a number of competing effects that must be taken into account for optimum coating over steep edges. Many compromises must be made. The gas pressure must be high to increase scattering and to have an rf discharge; but if it is too high, excessive gas occlusions (resulting in structural weaknesses) develop. The region of the edge is subjected to more bombardment than other regions; but some of the bombarding species are Al ions arriving with very high energy (400 eV average energy), and so would be expected to stick very well. A magnetic field is used to maximize the ionization of Al while keeping the pressure low to minimize gas absorption. When all of these competing effects and compromises are taken into account, it is possible to coat uniformly over these steep edges, even when the edges are not in the line of sight of the evaporation source.

Conclusion

The massive recrystallization of Al films deposited by dc sputtering with rf-induced substrate bias is a result of the energy of the deposition source, rather than the substrate bias. When a less energetic deposition source (thermal evaporation) is employed with an rf-induced substrate bias, the resultant films are fine-grained, smooth polycrystals. The film resistivity is a few percent higher than bulk values and is nearly independent of bias level. The interface between the film and substrate is very clean as evidenced by the ability to make direct ohmic contacts to silicon diodes and by the pinhole-free nature of the deposits. Several competing phenomena may be combined to effect a compromise that allows one to coat over very steep edges uniformly, even when the edge is not in the line of sight of the vapor stream.

Acknowledgments

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Back-Scattering of Material Emitted from RF-Sputtering Targets

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Abstract—When a solid surface is bombarded by energetic ions, one observes emission of various species. Some of the emitted material is reflected back to the surface. We have studied the quantity and spatial distribution of reflected material in a two-terminal rf-sputtering apparatus using electron-probe microanalysis as the principal analytic technique. Both the quantity and distribution of material can be controlled by appropriate adjustment of the sputtering conditions. Increasing the gas pressure, discharge current, magnetic flux density, and/or the sputtering yield of the material increases the amount reflected. Increasing the primary bombarding energy decreases the amount reflected. The distribution of material is mainly influenced by the magnetic flux density. These results apply to all processes in which a substrate is attached to a sputtering target, as is the case in rf-sputter-etching, bias sputtering, and related processes.

Introduction

When a solid surface is bombarded by energetic ions, one observes emission from the surface of neutral particles, secondary positive and negative ions, secondary electrons, and electromagnetic radition.[1] If the bombardment occurs in a glow discharge, some of the neutrals (sputtered particles) and positive ions are reflected back to the target. Neutrals are reflected by collisions with sputtering gas atoms and positive ions are pulled back by electrostatic attraction. It has been established for over 40 years that some of the material removed from a solid surface by ion bombardment is reflected back to the surface.[2] This effect has been shown qualitatively to be related to the sputtering gas pressure. To obtain a higher collection efficiency of sputtered material for sputtering yield studies, several techniques were devised to sputter at low pressures (glow discharge with a magnetic field, low

pressure supported plasmas, and ion beams). These have been reviewed by Wehner.[8]

To date, no extensive quantitative data on the phenomenon are available. Ecker and Emeleus[4] gave a theoretical treatment of the problem for dc sputtering in tubes. For routine sputter deposition of films, the amount of material reflected back to the target surface need be known only qualitatively. However, when a device of concern *is* the target or a part of it (as is the case in sputter-etching,[5-9] dc bias sputtering,[10] rf-induced bias sputtering,[11] and "ion plating",[12] the quantity and distribution of the back-scattered material should be known, since it can have a profound influence on the electrical properties of the device.

We have studied the quantity and spatial distribution of back-scattered materials in a 2-terminal rf-sputtering apparatus[9] using electron probe (x-ray) microanalysis[13] as the principal analytic technique. The sputtering parameters investigated were the sputtering gas pressure, the sputtering time, the bombarding potential, the magnetic flux density normal to the target, and the sputtering yield of the material being reflected back to the surface.

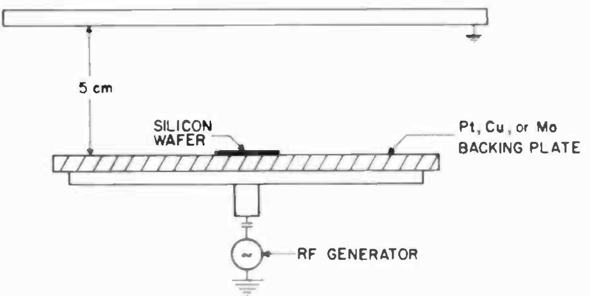

Fig. 1—Pertinent details of the apparatus.

Preparation of Test Specimens

Round, boron-doped, silicon wafers (24 mm diameter × 0.1 mm thick) were placed in the center of a 15-cm-diameter rf target as shown in Fig. 1. The details of the rf target assembly have been described previously.[9] A grounded metal plate was suspended above the target as shown. The shields around the rf target are not shown in Fig. 1.

The silicon wafers were simply rf-sputter-etched while resting on backing plates of Pt, Cu, or Mo. Then the silicon wafers were examined in the electron microprobe for the edge-to-edge metal distribution. Prior to each run, the rf target was sputter-cleaned for a minimum of

60 minutes to avoid introducing contamination from prior runs. Most of the work was done with Pt. The Cu and Mo targets were used only to study the effect of the sputtering yield on the quantity and distribution of back-scattered material.

Electron Probe X-Ray Microanalysis Techniques

The microprobe used in this study was a JEOLCO type JXA-3A with a nominal 15° take-off angle and a gas flow proportional counter. A P10 gas counter (90 argon-10 methane by volume) was used. Table 1 shows the curved crystal analyzers, the emission lines, and angles used for monitoring Pt, Cu, Mo, and Si.

Table 1

Metal	Emission Line	Angle	Crystal
Pt	Pt $L\alpha$	38° 3′	LiF
Cu	Cu $K\alpha$	26° 40′	quartz
Mo	Mo $L\alpha$	23° 31′	KAP (potassium acid phthalate)
Si	Si $K\alpha$	31° 4′	KAP

All the emission lines used are first-order lines. All three of the analyzing crystals are mounted on a rotating drum, thus allowing utilization of a single spectrometer table and counting system. To obtain the maximum resolution for wafer profiles, a focused primary beam was used. The beam diameter was 1.1 to 1.2 micrometers in diameter. A 25 kV accelerating voltage was found empirically to yield optimum sensitivity for these samples. The beam current was held within the limits 25-30 μA.

To ensure day-to-day repeatability of the microprobe measurement, a small region (approximately 100 micrometers in diameter) of a silicon standard was checked daily. Measurements on this standard were taken at a clean spot each time to avoid contamination build-up from prior measurements. Sample measurements were then corrected for any variation of the measurements of the standard.

When measuring the samples for this investigation, characteristic x-ray intensity measurements were taken at each beam-landing location for a period of time such that successive total counts differed by less than 1σ.

Under normal circumstances the microprobe yields only arbitrary values without calibration. However, in the case of thin films, Birks[13] has shown that the characteristic x-ray intensity generated in the film is a linear function of film thickness between 0 and about 3000 Å. For this investigation, films deposited for calibration of the microprobe were measured independently by multiple beam interferometry between 450 and 2000 Å. The calibration samples were then measured in the

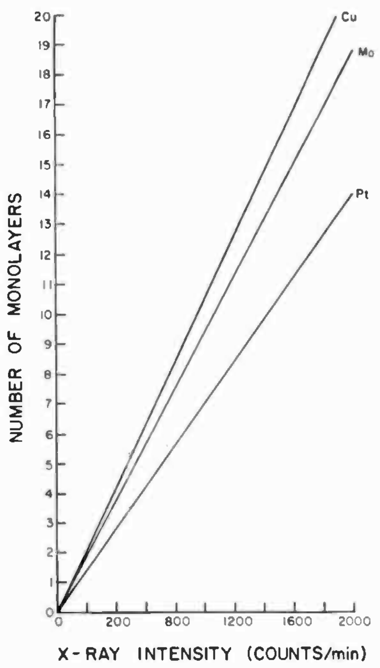

Fig. 2—Electron microprobe calibration.

electron microprobe and the thickness and number of x-ray counts per minute were related by the simple straight-line formula to determine the slope of the line. In all cases, the sensitivity of the microprobe was such that the minimum detectable number of counts per minute corresponded to a thickness somewhat less than one atomic diameter; that is, equivalent to fractional monolayer coverage. Since the material backscattered during rf sputter-etching is generally in the range 1-10 monolayers of metal, the data and the calibrations were plotted in terms of monolayers rather than absolute thickness. Fig. 2 shows the calibration curves for the microprobe.

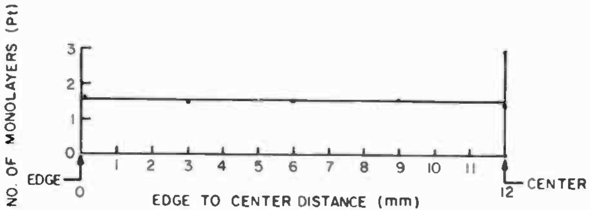

Fig. 3—Average profile (six wafers); series 1, time to equilibration.

Results and Discussion

The parameters studied were the sputtering time, the sputtering gas pressure, the sputtering voltage, the magnetic field normal to the target surface, and the sputtering yield of the back-scattered metal. In each case, the quantity and distribution of reflected material on the silicon wafer was determined. A Pt backing plate was used for all except the sputtering-yield series.

Sputtering Time

It was first necessary to determine whether or not back-scattered material comes to some kind of an equilibrium as a function of time. An arbitrary set of sputtering conditions was chosen and wafers were sputter-etched for times varying from 5 to 102 minutes. The conditions used were representative of routine sputter-etching conditions.

argon pressure = 5 millitorr
peak-to-peak rf voltage = 2800 V.
average dc level at target = −700 V.
magnetic flux density = 25 gauss.

The distribution of back-scattered Pt was quite uniform under these conditions (Fig. 3). Fig. 4 shows the average thickness of back-scattered material on these wafers as a function of time. For very

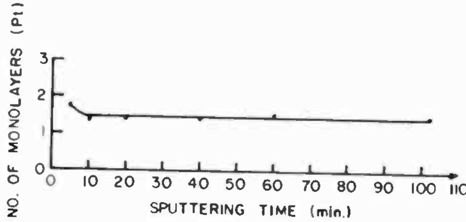

Fig. 4—Quantity of reflected platinum versus sputtering time.

short times, the average thickness is slightly higher than for longer times. The surface is essentially equilibrated after about 10 minutes of etching. The true equilibrium time is probably less than 5 minutes. The slightly higher values observed for the 5-minute runs are probably due to initial outgassing of the target when the discharge is first started. As will be shown, a small increase in gas pressure increases the amount of back-scattered material.

Based on these results, all subsequent runs were conducted for 20 minutes.

Sputtering Gas Pressure

Using the same discharge conditions as those cited above, and a sputtering time of 20 minutes, the gas pressure was varied from 1.0 to 40 millitorr of argon. At the higher pressures it was found that the distribution of Pt across the wafer varied. More was deposited on the

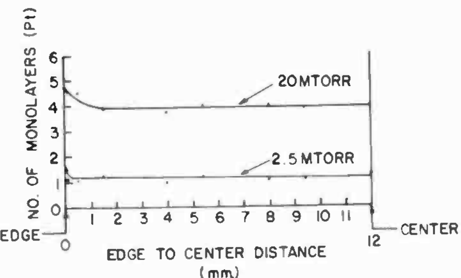

Fig. 5—Typical wafer profiles; series 2, effect of argon pressure.

edges than in the center. Fig. 5 shows the distribution of Pt across the wafers for the 2.5- and 20-millitorr runs. On all wafers, the region 1.5 mm from the wafer edge to the center was uniform in thickness.

Fig. 6 illustrates the dependence of the amount of reflected material on the gas pressure. The edge regions are plotted separately. The average for the center regions is plotted together.

With increasing pressure, the amount of material reflected back in the wafer centers saturates at about 20 millitorr, whereas near the edge, saturation appears to occur near 40 millitorr.

As the pressure is increased, the sputter-etch rate (rate of material removal) is increased. Hence, more Pt is available in the discharge to be reflected back. At the same time, more material is removed from the silicon wafer, leading to saturation of the amount of reflected material. The mean-free path of emitted material decreases with in-

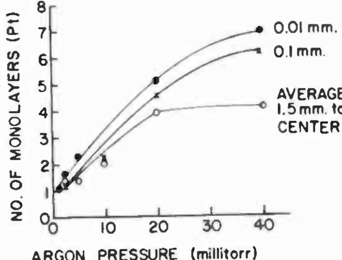

Fig. 6—Quantity of reflected platinum versus argon pressure with edge-to-center distance as a parameter.

creasing pressure. This implies that more Pt should be reflected near the wafer edge than in the center as is observed (Fig. 6).

Target Potential

Using a sputtering gas pressure of 20 millitorr, a magnetic flux density of 25 gauss, and a sputtering time of 20 minutes, the average dc level at the target surface (sheath potential) was varied from −500 to −900 V. Again the center region of the wafers (1.4 mm from the edge to the center) was quite uniform in thickness for all wafers, but the edges showed increased amounts of reflected Pt. Fig. 7 shows the amount of material reflected in the uniform center region as a function

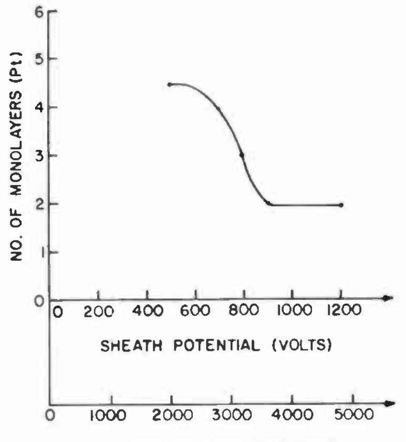

Fig. 7—Quantity of reflected platinum in the uniform center region of the wafers versus primary bombarding potential.

of voltage. Fig. 8 shows typical distributions of reflected material near the wafer edge.

As the bombarding voltage is increased, the center of the energy distribution of sputtered material increases. Therefore, collisions of sputtered atoms with argon atoms would be less likely to slow down the emitted material enough to back-scatter it before it reaches the collector plate (Fig. 1). As a result, the amount of back-scattered material is substantially reduced. Saturation occurs at about −900 V.

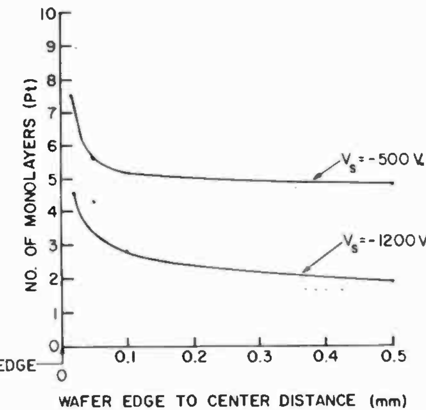

Fig. 8—Typical wafer profiles near the wafer edge for high and low bombarding potentials.

Since this behavior seems to be related to mean-free-path considerations, the saturation voltage should be a function of the pressure-separation product.

Magnetic Flux Density

The following conditions were held constant in this part of the investigation:

argon pressure = 20 millitorr,
sheath potential = −700 V (2800 V p-p),
sputtering time = 20 minutes.

The magnetic flux density was varied from 0 to 100 gauss. The magnetic field has the most profound influence on the quantity and distribution of back-scattered material of all the sputtering parameters studied (Fig. 9). A flux density of 25 gauss was used to study all the other parameters because it was found empirically that this field re-

sulted in the best uniformity while sputter etching with the system. It is clear that this field also produces the most uniform distribution of back-scattered material.

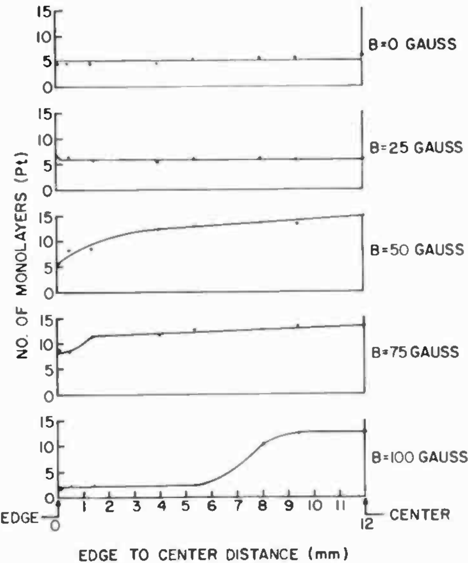

Fig. 9—Wafer profiles of reflected platinum for various magnetic flux densities.

As the field is increased, the relative amount of reflected Pt in the center of the wafers increases as compared to the amount remaining on the edges. At the voltage and pressure used here, much of the emitted material does not have a sufficiently high initial velocity for it to reach the collector plate (Fig. 7). As the magnetic field is increased the probability of ionizing a substantial fraction of the emitted Pt becomes greater because of the increased probability of impact ionization in the negative glow region of the discharge[14] and the emission of secondary Pt+ from the target itself.[15-21] We have observed Pt+ spectroscopically, but we cannot determine whether these ions originate at the target or in the glow. While back-scattering of neutrals is a long-range, collision-limited diffusion phenomenon, the back-scattering of Pt+ is a short-range electrostatic effect. Any Pt+ generated under these conditions is accelerated back to the target at an energy level nearly determined by the target potential.[22] These Pt ions then become part of the bombarding species at the target. Pt+ ($M = 195.09$) is a much more efficient sputtering ion than is Ar+

($M = 39.948$). As the magnetic field is increased, increasing the probability of ionizing the emitted Pt, progressively more Pt^+ bombardment of the silicon wafer occurs. Most of the Pt^+ bombardment should occur near the edge of the silicon wafer. More material is back-scattered as neutral Pt into the center of the wafer because more Pt is available to be back-scattered, as a result of increasing the discharge current produced by the increased magnetic field.

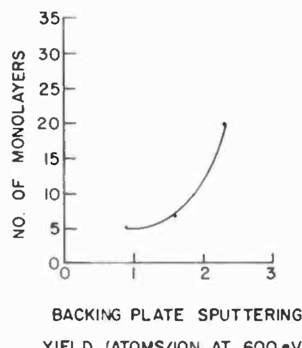

Fig. 10—Amount of reflected material in the uniform wafer centers versus the sputtering yield of the reflected material. (Yields after Laegreid and Wehner, Ref. [23]).

Sputtering Yield of the Back-Scattered Metal

Fig. 10 shows the effect of the sputtering yield of the backing plate material on the amount of back-scattering observed in the uniform, center regions of the wafers under the following conditions:

argon pressure = 40 millitorr,
peak-to-peak rf voltage = 2800 volts,
sheath potential = −700 volts,
magnetic flux density = 25 gauss,
sputtering time = 20 minutes.

Clearly there is an abrupt rise in the amount of material back-scattered as the yield (i.e., amount of material in the gas phase) increases. The relative profiles do not change from those observed with Pt (Fig. 5).

Crystal Structure of the Back-Scattered Material

The substrates onto which these materials were reflected were single-crystal [111] silicon. Numerous samples were analyzed by re-

flection electron diffraction to determine whether the material reflected formed compounds with the substrate. In every case, the electron diffraction patterns revealed an amorphous surface layer. The spot pattern of the [111] single-crystal substrate was visible, but any polycrystalline rings that might have been present were obscured by the amorphous surface layer.

Conclusions

The implications of this study extend to sputter-etching processes, bias sputtering (dc and rf), ion plating, and related processes. The fact that the amount and distribution of the material reflected back to the surface can be controlled is important to all of these processes.

We have noted in the past[9] that during sputter-etching to delineate a pattern with photoresist, the material removed from the surface is all removed at the same rate. The composite etch rate is determined by the photoresist material, the material being etched, the pattern, and the backing-plate material. It was inferred that somehow the entire surface exposed to the rf discharge must come to an equilibrium such that the material exposed to the discharge is everywhere the same. From this work it is clear that reflection of emitted material is the mechanism by which this occurs. The entire target surface becomes a mixture of all the materials present on it. The set of conditions found empirically to result in uniform etching of substrate surfaces were those used in the present investigation to determine the time to target surface equilibration (Fig. 3). This work shows that those conditions result in the most uniform amount of back-scattered material across the surface. Of more interest than the profile, however, is the amount of material required to produce this effect (approximately 1.5 monolayers). This implies that nearly all the material removal that occurs when a target is sputtered under these conditions occurs from the first few monolayers of the target surface. Variations in the sputtering parameters affect the depth from which material is removed. As may be seen from Fig. 10, the sputtering yield of the surfaces also influences the depth from which material is removed.

For sputter-etching to delineate a pattern or to clean a surface uniformly, the amount of back-scattered material should be minimized in quantity and made uniform in distribution. Furthermore, the backing plate should be a material that will have no detrimental effect on the part being etched when the backing-plate material is reflected onto the surface of the part. Ideally, it should be the same material as that of the substrate being bombarded.

In some cases it may be beneficial to maximize the quantity of back-scattered material to produce a controllably thin mixture of substrate and backing plate materials. For example, when deposition from a dc or rf source with an rf-induced substrate bias is used, it is possible to promote adhesion to a substrate by using reflected material to form a graded interface prior to opening the shutter to start the main deposition. That is, by using a backing plate of the material to be deposited, the initial stages of film growth can be accomplished during the sputter cleaning of the substrate by way of back-scattered material mixing with substrate material.

Clearly, some of the substrate material is reflected onto the backing plate as well. This effect changes the nature of the backing plate surface in the same way that it changes the substrate surface. Hence, to produce uniform results from one run to another, it is necessary to remove the surface layer of reflected material from the backing plate between runs. This should be standard practice for rf-sputter-etching, bias sputtering, and related processes.

The microprobe sensitivity indicated by Birks[13] for measuring film thicknesses down to a few angstroms has been demonstrated.

Summary

We have shown that the quantity and spatial distribution of material back-scattered to small disks located on an rf sputtering target can be controlled within certain limits by appropriate adjustment of the sputtering conditions. Both the quantity and distribution of material come to saturation in a very short period of time. The amount of material reflected is influenced by those parameters that increase the removal rate of material from the surface (pressure, magnetic field or current, and the sputtering yield of the material). When the energy of the emitted material is increased by increasing the primary bombarding energy, the quantity of reflected material is decreased. The distribution of reflected material is mainly influenced by magnetic fields normal to the target surface. Increased magnetic fields result in a higher concentration of metal ions in the discharge. These metals contribute to higher sputter-etch rates near the edge of the substrate.

These results apply to all sputtering processes in which a substrate is connected to a sputtering target, as is the case in rf sputter-etching, bias sputtering and related processes. Depending on the process, the effect can be maximized, minimized and otherwise controlled.

These results tend to support the view that sputtering occurs in the first few monolayers of target surfaces.

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Vapor-Deposited Tungsten as a Metallization and Interconnection Material for Silicon Devices

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Abstract—A procedure for metallizing and intraconnecting silicon devices and integrated circuits with tungsten is described. For this purpose, a chemical-vapor-deposition technique involving reduction of tungsten hexafluoride is employed. Advantages of tungsten metallization and high-temperture properties of tungsten-to-silicon contacts are discussed.

Introduction

For the metallization of silicon devices, the most widely used material is aluminum. It has the advantages of high conductivity and excellent adhesion both to silicon and to silicon dioxide. It also forms low-resistance ohmic contacts to p-type and heavily doped n-type silicon. It is easily deposited by evaporation techniques and can readily be defined into high-resolution patterns. However, aluminum has a number of disadvantages. Because of the low melting point of the aluminum–silicon eutectic (577°C) and because of rapid diffusion of aluminum along grain boundaries, metallized devices cannot be heated safely above about 525°C. Furthermore, aluminum metallization exhibits certain types of failure under electrical stress, in part because of its low activation energy for self diffusion.[1] For certain power devices, these limitations are unacceptable. Aluminum metallization is also unsatisfactory when it will be exposed to moisture or air during operation of a device, since it corrodes readily. Finally, successful multilevel metallization of integrated circuits with aluminum requires exceptionally precise control of the processing sequence to avoid high-resistance aluminum-to-aluminum contacts and undercutting of aluminum feed throughs.

Most of the information in this paper was presented as a recent "news" paper, 231 RNP, at the Electrochemical Society Meeting in Detroit, Michigan, October 1969.

To overcome these disadvantages, a number of metallization systems have been suggested. Perhaps the most successful of these is the platinum silicide/titanium/platinum/gold metallization used with beam-lead devices.[2] This metallization system has particular advantages for preparing hermetically sealed chips that must withstand corrosive attack by atmospheric constituents. However, the number of materials involved and the added processing steps required make this metallization system rather expensive. Molybdenum/gold metallization has been suggested,[3] but the processing equipment is again expensive and inconvenient to use.*

Tungsten offers a number of advantages as a contact metallization and intraconnection material for silicon devices and integrated circuits (see Table 1). With respect to thermal coefficient of expansion, silicon is more closely matched by tungsten than by any other elemental metal. Tungsten contacts to heavily doped n- and p-type silicon are ohmic, and its resistivity is only about 2½ times that of aluminum. It adheres well to silicon and to silicon dioxide and can readily be defined into high-resolution patterns. It is hard, not easily scratched, and is not attacked readily by aqueous HF nor by atmospheric constituents. The lowest melting point in the binary system tungsten–silicon is 1410°C. Tungsten does not diffuse readily into silicon, and its activation energy for self diffusion is one of the highest known for metals. For these reasons, it is especially suitable for power devices and for multilevel metallization applications. We have therefore investigated tungsten as a metallization material for silicon devices and integrated circuits.

Deposition of Tungsten Films

Tungsten is readily deposited on silicon device wafers by chemical vapor deposition from tungsten hexafluoride. The adhesion of the films is excellent if a suitable processing sequence is employed. The deposition procedure and devices prepared by this method are described in this paper. An electro-etching process used to define patterns in the tungsten films will be discussed in a forthcoming paper.

Tungsten hexafluoride was chosen as the source for tungsten because it is gaseous at room temperature (bp. 17.3°C) making its handling easy. It is readily available in high purity, at low cost, and in large quantities. Furthermore, no lower valence fluorides are known.[4] On reduction, the hexafluoride is reduced smoothly to the metal.

* Nickel is employed for a number of large-area power devices where adhesion to oxide layers is not required, but it is not generally satisfactory for integrated circuits or for small-geometry devices.

Table 1—Comparison of Contact Metallization and Intraconnection Materials for Silicon Devices

	Linear Coefficient of thermal expansion† $\frac{\Delta l}{l}$ °C^{-1}	Temp. Range (°C)	Melting Point†† of Metal (°C)	Melting Point†† of Eutectic with Silicon (°C)	Bulk Resistivity at 20° C. (Ohm-cm)
Si	4.15×10^{-6} 3.6×10^{-6}*	0 – 50 25 – 600	1430		
W	4.46×10^{-6}	25 – 500	3370	1410	5.5×10^{-6}
Mo	5.5×10^{-6}	25 – 500	2620	~1400	4.8×10^{-6}
Pt	8.8×10^{-6}	−150 – 600	1755	830	10.5×10^{-6}
Ni	15.7×10^{-6}	0 – 550	1452	964	6.9×10^{-6}
Al	22.5×10^{-6}	0 – 600	600	577.2	2.26×10^{-6}

† Source: "Integrated Silicon Device Technology" Volume V, *Physical-Electrical Properties of Si*, July 1964 Research Triangle Inst., Durham, N.C.

†† Source: M. Hansen, *Constitution of Binary Alloys*, Second Ed. McGraw Hill, New York (1958).

* Source: C. C. Wang, Private Communication.

Tungsten hexafluoride reacts with *silicon* on contact at temperatures above about 400°C according to the following equation:

$$2WF_6 + 3Si \rightarrow 3SiF_4 \uparrow + 2W.$$

This reaction has been employed by Crowell, Sarace, and Sze[5] to form Schottky barrier diodes to silicon. If the silicon is sufficiently heavily doped, we have found that ohmic contacts can be made to either p- or n-type material. For this purpose, resistivities below about 0.1 ohm-cm p-type, and below about 0.01 ohm-cm n-type have been found satisfactory; the more heavily doped, the better.

If tungsten hexafluoride is allowed to contact *silicon dioxide* at this temperature, the surface of the oxide is attacked chemically. If the hexafluoride is sufficiently dilute, the surface becomes almost imperceptibly textured, and tungsten films subsequently deposited on such a surface adhere very strongly. The texture of the surface cannot be seen by the naked eye but is visible if a finely focussed light beam is allowed to impinge on the surface and the surface is viewed at an angle so that the scattered light can be seen. Under these conditions a very slight haziness can be observed that is not present in the unetched oxide surface.

When a silicon device wafer, opened and ready for metallization, is exposed to dilute tungsten hexafluoride at about 700°C, the silicon regions quickly and selectively become coated with tungsten. In addition, the oxide regions will be slightly etched. This mild vapor etching helps to remove any thin oxide layers over the silicon regions, cleans the oxide surface, and ensures that tungsten films, subsequently deposited on the oxide, will be adherent.*

In the presence of hydrogen, tungsten hexafluoride is reduced to metallic tungsten at temperatures in the neighborhood of 700°C according to the following reaction:

$$WF_6 + 3H_2 \rightarrow W + 6HF \uparrow.$$

By means of this reaction, tungsten films can be deposited uniformly both on oxide and on (tungsten metallized) silicon regions. In our work, these two types of reaction, contact reduction and hydrogen reduction, are used in sequence.

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* To minimize undercutting at the edges of openings, a chemical-vapor-deposited silicon dioxide layer[7] covering the entire wafer can be employed. The surface of this oxide layer is lightly etched with tungsten hexafluoride as the first step in the metallization. The oxide is then patterned with photoresist and contact areas are opened through the oxide. The silicon regions are subsequently metallized with tungsten by contact reduction.

The apparatus employed for this work, shown in Fig. 1, consists of a simple fused-quartz deposition chamber similar to that employed for the epitaxial growth of silicon. The substrate is placed on a silicon-carbide-coated carbon susceptor, through one end of which a thermocouple is inserted. By means of this thermocouple, the output of an rf generator is controlled to give a constant temperature in the block.

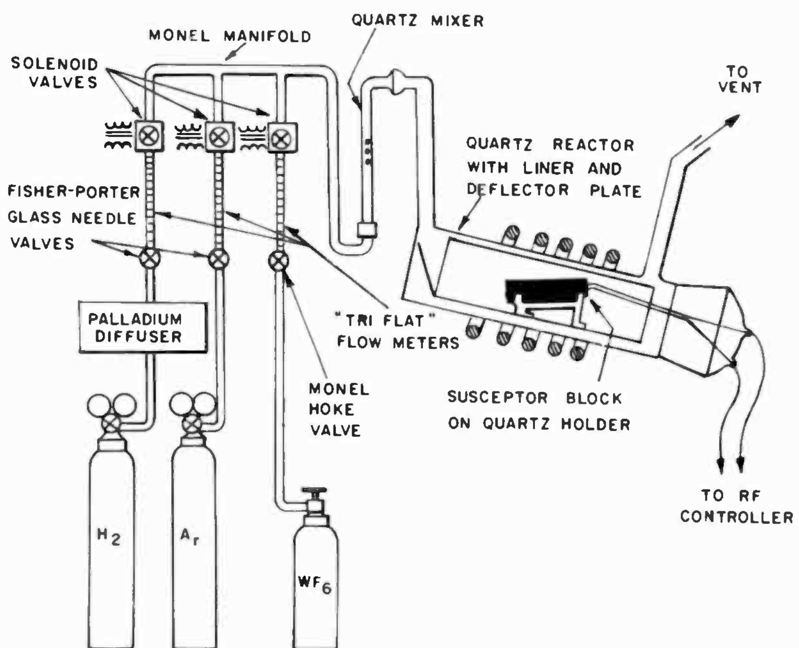


Fig. 1—Apparatus for deposition of tungsten layers from tungsten hexafluoride.

A wafer is cleaned, placed on the susceptor, and inserted into the deposition chamber. The thermocouple is inserted and the reaction chamber is closed. After purging the chamber for a few minutes with argon flowing at about 7 liters/minute the substrates are brought to 700°C. At this point a few cc/minute of tungsten hexafluoride are introduced for a period of a few seconds. The change in the appearance of the substrate wafer resulting from this step is clearly visible. The silicon regions become more metallic, and the oxide thickness decreases slightly as indicated by a change in the interference color. The tungsten hexafluoride is purged from the system, and the argon is replaced by hydrogen flowing at about 10 liters/minute. Gaseous tungsten hexafluoride is next introduced into the reactor, a few cc at a time, and

deposition takes place on the heated susceptor and the substrate. When the desired thickness of tungsten has been deposited, the tungsten hexafluoride flow is terminated and the substrate and susceptor are allowed to cool to room temperature in hydrogen. At this point, the hydrogen is replaced by argon, and a few minutes later, the substrate is removed from the reaction chamber.

Characterization of Tungsten Layers

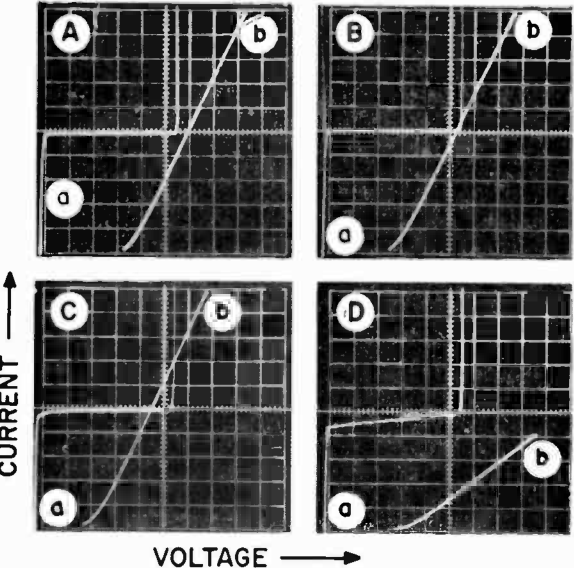
For tungsten layers up to about 0.5 μm in thickness, the surface is specular, corresponding to that of the substrate. At thicknesses of about 1 μm or more, the surface becomes slightly matte but is still very smooth. Thicknesses up to 5 μm have been deposited on silicon device wafers with no indication of cracking or separation of the tungsten from the substrate wafer.

The deposited tungsten films have a resistivity of 6×10^{-7} ohm-cm $\pm 10\%$ the same as that of bulk tungsten within the error of measurement. Since this resistivity is about 2.5 times that of bulk aluminum, the thickness of tungsten required for a given device will be somewhat higher than that required with aluminum metallization. In practice, however, the sheet resistivity of evaporated aluminum films rarely equals the bulk value. Tungsten films having a thickness of about 1 μm have been found satisfactory for a variety of experimental devices.

Vapor-deposited tungsten films are hard, brittle, and very adherent. Probe tips can be run across the pattern layers with no gouging out of metal. The only evidence of probing is a slight burnishing of the surface. Patterns can readily be formed in the layers by electroetching combined with chemical etching in alkaline ferricyanide.

Tungsten contacts to heavily doped silicon are ohmic and unaffected by heat treatment in neutral or reducing atmosphere at temperatures up to 900°C for a few minutes. Typical forward and reverse characteristics for the emitter–base junction of an experimental tungsten-metalized transistor are shown in Fig. 2, both prior to and subsequent to heat treatment. These devices, having emitter–base junction depths of about 1.5 μm, were heated in argon at temperatures ranging up to 900°C for periods up to 20 minutes, with no perceptible increase in the forward resistance nor any degradation of the reverse characteristics of the junction.

If the hot, metallized wafer is exposed to air, the tungsten will oxidize and the forward resistance of a transistor will increase greatly (Fig. 2-D). Care must be taken to ensure that the tungsten is cooled



(A) Initial Characteristics
(B) After treatment at 800°C in Ar for 12 minutes in a closed system
(C) After treatment at 900 to 950°C for 20 minutes in Ar in closed system
(D) After treatment at 850°C in Ar for 20 minutes in open tube furnace uncapped at open end

Fig. 2—Reverse-bias ((a) curves) and forward-bias ((b) curves) characteristics of emitter-base junction in an experimental tungsten-metallized transistor (emitter junction about 1.5 μm deep) before and after heat treatment. For reverse bias, current = 9.5 mA per division and voltage = 1.0 V per division; for forward bias, current = 100 mA per division and voltage = 0.2 V per division.

to below 300°C before it is exposed to an oxidizing ambient. However, if the tungsten metallization is sealed beneath a layer of silicon nitride of silicon dioxide, oxidation of the metal can be prevented and the metallized units can then be heated in air with no deleterious effects. Because of the high-temperature properties of the tungsten-to-silicon contact, temperatures of 850°C or higher can be employed for the deposition of silicon nitride. Alternatively, vapor-deposited silicon dioxide layers can be densified in neutral atmosphere at high temperature if desired.

Tungsten itself is not readily bonded and is not wet by solder. A suitable layer of an interface metal is therefore needed to permit interconnections to external circuitry. Metals such as nickel, platinum, copper, gold, and aluminum can be deposited by a variety of methods

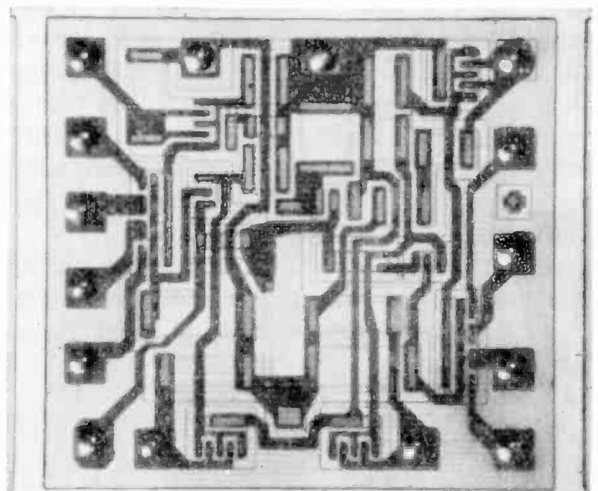


Fig. 3—Tungsten-metallized, silicon-nitride-sealed integrated-circuit chip with solder bumps.

at appropriate stages in the processing, depending on the termination desired. An example of a device formed with a platinum interface layer and solder bumps is shown in Fig. 3, while a device having wire bonds is shown in Fig. 4.

The adhesion of the deposited tungsten to the silicon dioxide present on device wafers was evaluated using a tensile tester.* For this pur-

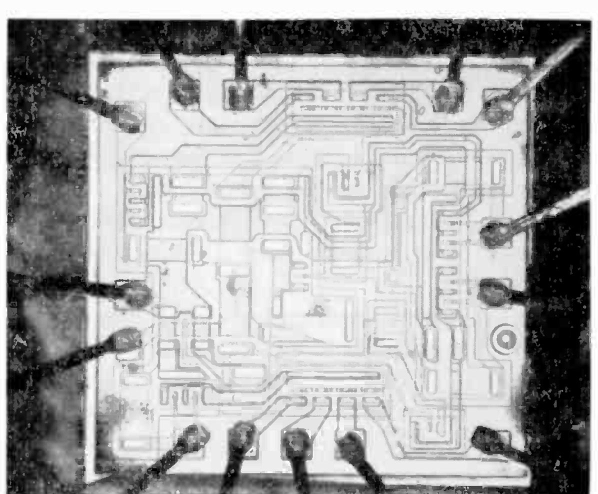


Fig. 4—Tungsten-metallized, silicon-nitride-sealed integrated-circuit chip, wire bonded in ceramic flatpack.

* Instron Engineering Corporation, Quincy, Mass.

pose, a sputtered platinum layer was first deposited on the tungsten and then selectively de-sputtered to leave 0.005-inch Pt dots on approximately 0.005-inch-square tungsten pads. Thermocompression (nail head) bonds were formed with 0.002-inch and 0.005-inch Au wires. Vertical-pull measurements showed bond strengths typically between 8000 and 25,000 psi (or approx. 60-180 g on a 0.005-inch pad). Failure occurred in the gold wire, at the SiO_2-Si interface, or in the Si itself, rather than at the W/SiO_2 or W/metal interfaces.

Extensive temperature cycling tests have not been carried out, but no failures have been observed for glassed, tungsten-metallized, integrated-circuit chips cycled five times rapidly from dry ice–acetone slurry (−65°C) to molten lead at 350°C.

Tungsten-Metallized Devices

Both discrete transistors and integrated circuits of the dual 4-input emitter-coupled logic type have been tungsten metallized and dc probed. Following pattern etching of the tungsten, yields comparable to those for aluminum-metallized factory product were obtained. The circuits were subsequently coated with a 1500-Å silicon nitride layer at 850°C. Next, openings through the nitride, in the contact-pad regions only, were formed by conventional silicon dioxide masking[7] and photolithographic processing.[7] Tungsten is attacked only very slowly by hot phosphoric acid, and the etching time is not critical. Repeat dc wafer probing at this point showed that no degradation of the electrical characteristics resulted from this processing sequence. A number of these devices, platinum metallized in the contact-pad region only, were mounted in flat packs and bonded ultrasonically with aluminum wires. The devices then underwent final testing and yields were found to be comparable to those for aluminum-metallized factory products. Finally, pull measurements were made on the bonded chips. It was observed that the failure mechanism was the pulling apart of the aluminum wire at an applied force of 6 grams, the same as observed for aluminum-metallized products.

It has also been observed that, under conditions leading to rapid aluminum "swelling" for conventionally metallized devices, the tungsten metallized units have not failed, even after several hundred hours of testing.

Multilayer Metallization with Tungsten

Tungsten has a number of advantages for multilevel metallization. Crossover test arrays have been constructed using tungsten for the

upper and lower metallization with vapor-deposited silicon dioxide, densified at 800° for 10 minutes in Ar, serving as the insulator. Appropriate contact holes are etched through the oxide layer down to the tungsten surface. Since tungsten is inert to HF-containing etchants, this step is noncritical. A second tungsten layer is then vapor deposited and suitably patterned. Examination of these crossovers showed that no high-resistance contacts were encountered (Fig. 5). This is probably

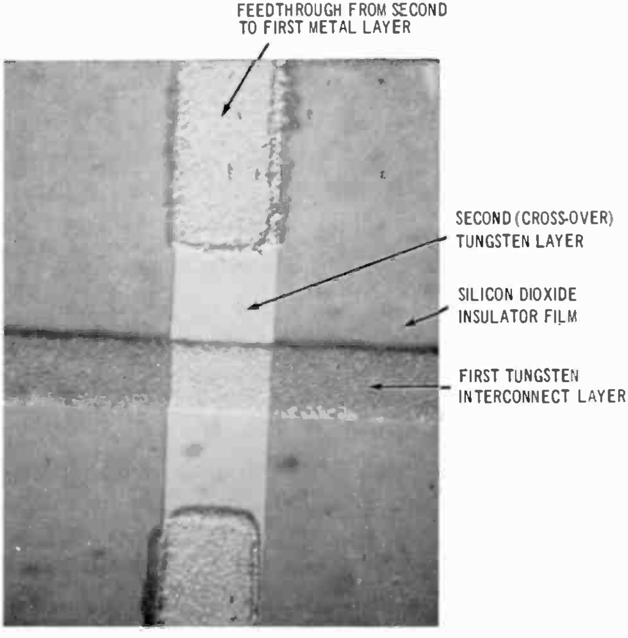


Fig. 5—Element in cross-over pattern prepared using tungsten and vapor-deposited SiO_2.

attributable to the etching action of tungsten hexafluoride on any thin silicon-oxide-layer residues, and to the fact that tungsten oxides are reduced to the metal at the deposition temperature employed. Shorting or low-voltage breakdown through the densified insulator has not been observed. This is perhaps partly because recrystallization of the first tungsten metal layer does not occur at the processing temperatures employed. Consequently, there are no "hillocks" present on the surface to puncture the dielectric layer.

Conclusions

For the metallization of silicon devices, tungsten has a number of

advantages. It permits the fabrication of transistors and integrated circuits that can be passivated at high temperature. In such circuits, the passivating layer covers the metallization pattern as well as the active areas of the device or circuit. Openings need then be made only in the contact-pad regions, away from sensitive junctions. Contacts between tungsten and heavily doped silicon are ohmic and are not degraded by heat treatment at temperatures up to 900°C and for times of the order of 20 minutes in neutral or reducing atmosphere. Multilayer structures can be prepared using only tungsten and a vapor-deposited silicon dioxide layer.

Acknowledgment

The authors would like to thank W. Kern for critically reading the manuscript and for his help in the thermal cycling measurements made on tungsten metallized devices. They would also like to thank N. E. Wolff for many valuable suggestions and stimulating discussions.

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Two Room-Temperature Electroless Nickel Plating Baths—Properties and Characteristics

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Abstract—Two alkaline electroless nickel plating baths giving an approximate plating rate of 0.1 mil/hr at room temperature are described. One bath employs hypophosphite and the other dimethylamine borane (DMAB) as the reducing agent. Both baths yield a dense deposit, one containing less than 3% of phosphorus, while the second has a boron content of less than 0.5%. By appropriate modification of the composition, the plating rate may be made independent of the concentrations of either nickel or reducing agent. Both baths exhibit a plating rate independent of pH over a wide pH range.

Although the baths employ the same complexing media, distinct variations in the chemical characteristics, as well as in the physical properties of the deposits from them, were noted. Reasons for this behavior are suggested, and a hypothesis concerning the nickel complex(es) existing in bulk solution has been formulated to account for the kinetic behavior of the bath.

Introduction

Since the discovery of the electroless plating process by Brenner and Riddell,[1] considerable attention has been devoted to the development of proprietary baths and to the investigation of the basic phenomena taking place. For the electroless plating of nickel, both acidic and alkaline type baths are available; however, all commercially available baths are intended for use at elevated temperatures.[2] In most baths, organic complexing agents are employed, and little emphasis has been given to baths containing inorganic complexing agents. In 1960, Schwartz[3] described an alkaline type electroless nickel bath employing ammonia and pyrophosphate as the complexing agents. Operated at 68 to 74°C, the bath had a fast plating rate and gave a deposit containing 5% phosphorus. Loss of ammonia at these temperatures alters the performance of the bath and has discouraged the widespread use of this and other alkaline baths.

In the present investigation, the complexing agents described by

Schwartz are employed; however, operation of the bath is at room temperature. Both hypophosphite and dimethylamine borane (DMAB) have been successfully employed as reducing agents. The roles of ammonia and pyrophosphate in the plating process have been investigated. The baths have a number of advantages in the plating of semiconductors and insulators, such as organic polymers.

Materials

All chemicals used in this investigation were of reagent grade; except for the dimethylamine borane (DMAB) reducing agent,* which was better than 99% pure. The water used was deionized and then double distilled.

Measurement and Control

All deposition rate measurements were made on alumina. The substrates** were pretreated by conventional tin/palladium activation. In all cases the weight gain was monitored for a 10.0-minute deposition time. The volume of the electroless bath was maintained at 200 cc and no external agitation[4] was provided.

To monitor *p*H, a Beckman Model 76 *p*H meter was used. All reported *p*H values are estimated to be within ±0.05 *p*H unit. Temperature control of better than ±0.1°C was achieved using a constant-temperature bath controlled by a commercial thermoregulator. Absorbance studies in the visible range were made in a Beckman spectrophotometer, Model DB-G.

Bath Compositions

Typical formulations for the electroless nickel baths are given in Table I. Plating rates are approximately 350 Å per minute at room temperature for these formulations. By suitable adjustment of the components, plating rates up to about 400 Å/min can be obtained at room temperature.

In these plating baths, ammonia and pyrophosphate are employed as complexing agents for the nickel ions, and either hypophosphite or dimethylamineborane (DMAB) as reducing agents. For convenience, two solutions are prepared that are mixed in equal volume ratio just

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* Callery Chemical Company, Callery, Pennsylvania.
** American Lava Corporation, 2-inch by 2-inch #614 plain.

Table I—Chemical Make-Up of Baths

Solution A	
$NiSO_4.6H_2O$	50 g/l
$Na_4P_2O_7.10H_2O$	100 g/l
NH_4OH (58%)	45 cc/l
Solution B	
$NaH_2PO_2.H_2O$	50 g/l
or	
$(CH_3)_2NHBH_3$	3 g/l

prior to use. One (A solution) contains the nickel ion, ammonia, and pyrophosphate. The other (B solution) contains the reducing agent. Normally, these solutions would be mixed in the ratio 1:1.

The properties of the nickel films deposited from each of the baths are summarized in Table II. To minimize slow precipitation from the A solution on long-term storage (periods of several months or longer), the ammonia content must be properly adjusted. In specific, solutions having 50 g/l of $NiSO_4.6H_2O$ and 100 g/l of $Na_4P_2O_7.10H_2O$ are most stable when the ammonia content corresponds to an initial pH of about 9.8 to 10.0.

Table II—Room Temperature Electroless Nickel Chemical and Physical Properties of Deposits

	Ni-B	Ni-P
	%B<0.5	%P<3
Approximate resistivity (ohm-cm)	15×10^{-6}	30×10^{-6}
Activation energy (KCAL/Mole)	8.5	14
Self-Initiation	most metals	limited
Approx. melting point (°C)[5] (M.P.$_{Ni}$ – 1452°C)	1420	1240
Eutectic Temperature (°C)	1140	880
Eutectic Composition	4% B	10% P
	Both deposits are: Bright, Dense, Hard, Magnetic, Solderable	
Approx. Plating Rate at 25°C	← 0.1 mil/hr →	

Plating Rate Dependency on Ammonia Concentrations and *p*H

Since both ammonia and pyrophosphate are capable of forming complexes with nickel ions,[6] the plating rate would be expected to vary between two extremes, the first corresponding to no ammonia in the system and the second to a bath having excess ammonia in comparison to pyrophosphate. Fig. 1 shows the manner in which the plating rate

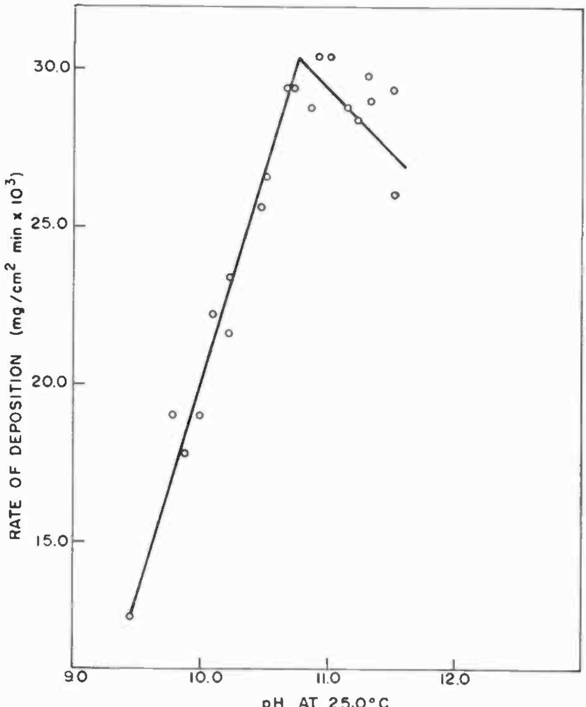


Fig. 1—Rate of deposition versus *p*H varied with NH_4OH with the following composition held constant: $NiSO_4.6H_2O$ 25.0 g/l, $Na_4P_2O_7.10H_2O$ 50 g/l, and DMAB 1.5 g/l.

varies as the ammonia content increases as reflected in the initial *p*H of the bath. Upon adding ammonia initially, the plating rate increases rapidly. With further addition, the rate passes through a maximum value and then decreases again. This behavior is common to all baths formulated with these complexing agents, although the maximum in plating rate occurs at an ammonia concentration corresponding to a *p*H of about 10.7 for the Ni-B bath and of 10.1 for the Ni-P system. Attempts to account for this difference were unsuccessful; there is no

apparent chemical reaction between ammonia and either DMAB or hypophosphite, nor does the addition of DMAB or hypophosphite to a nickel-pyrophosphate-ammonia bath appear to alter the nature of complex existing in bulk solution.

In an attempt to examine the sensitivity of the current baths to operating *p*H, solutions containing fixed ammonia were prepared and the *p*H was extended by the addition of sodium hydroxide. Fig. 2

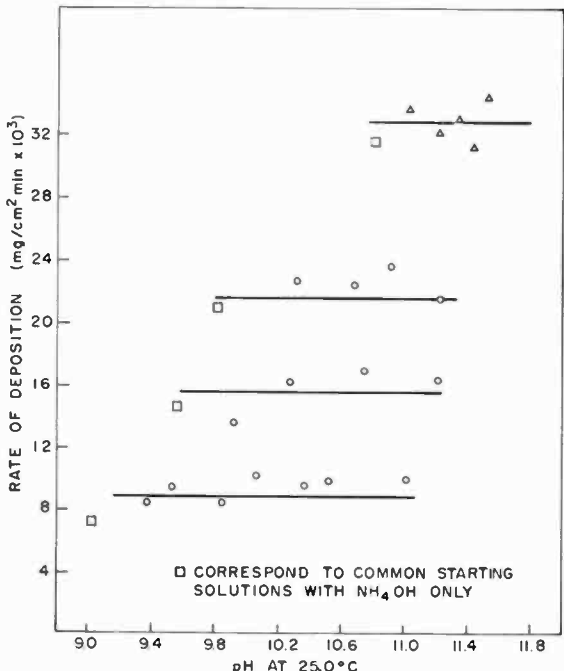


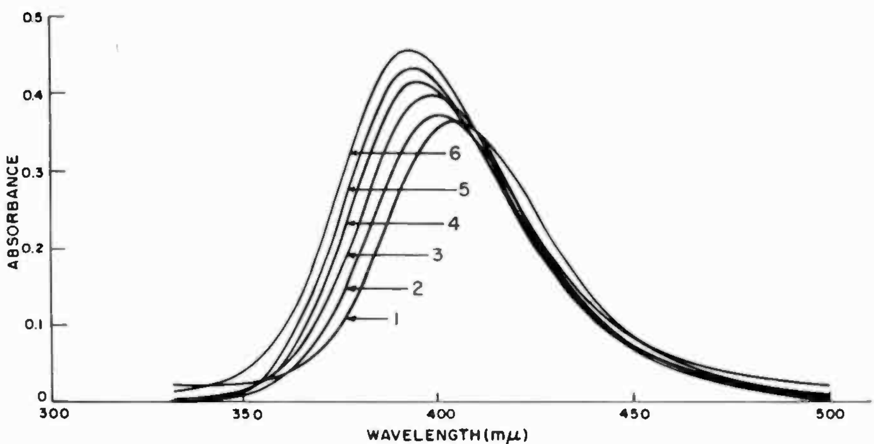
Fig. 2—Rate of deposition versus *p*H varied with NaOH.

shows that the plating rate is independent of operating *p*H provided the ammonia content is fixed. Furthermore, there is no apparent change in the absorption spectrum from one to another of these solutions. This effect was also found to be applicable at temperatures above 25°C.

It was found that the operating *p*H may fall below the initial make-up value (with ammonia only) without altering the plating rate.

Nature of the Complexes Present

The spectral absorbance of these solutions was monitored in the visible range as a function of ammonia content, as shown in Fig. 3. Since



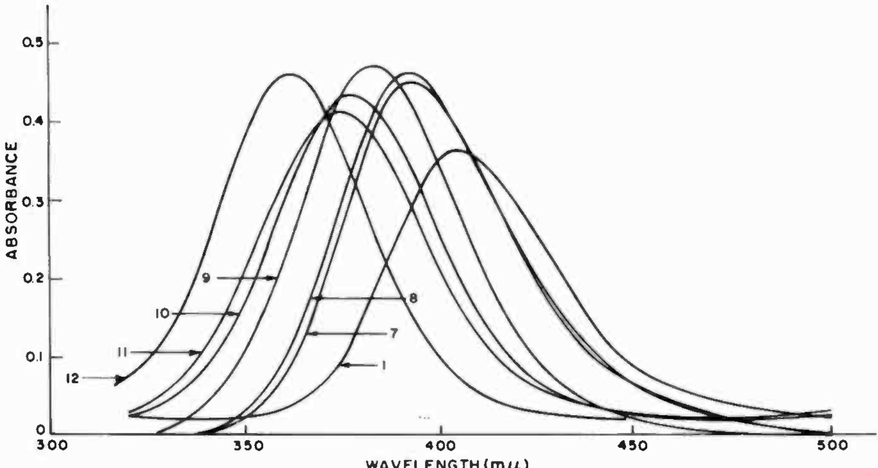


Fig. 3—The effect of increasing the ammonia content on the absorbance curves for solutions containing 25.0 g/l $NiSO_4.6H_2O$ and 50.0 g/l $Na_4P_2O_7.10H_2O$. The following are the NH_4OH molar concentration, and the values in parenthesis correspond to the initial *p*H at 25°C:

1. 0; 2. 2.64×10^{-2} (8.65); 3. 5.28×10^{-2} (9.75);

4. 7.92×10^{-2} (9.78); 5. 1.06×10^{-1} (10.05);

6. 1.32×10^{-1} (10.24); 7. 1.59×10^{-1} (10.40);

8. 1.85×10^{-1} (10.52); 9. 6.7×10^{-1} (11.70);

10. 9.25×10^{-1} (12.0); 11. 1.32 (12.15); 12. ammonia only without pyrophosphate (11.65).

Cell length = 5 mm.

there is no discernible effect associated with the addition of reducing agent, the material was omitted for convenience. In solutions 1 through 12, the ratio of the concentration of ammonia to pyrophosphate increases, with solutions 1 and 12 containing only pyrophosphate or ammonia, respectively. From Fig. 3, it is noted that there is a spectral shift towards shorter wavelength as the ammonia content is increased. Furthermore, there are two isosbestic points; at 408 mμ and 370 mμ. In view of the presence of the isosbestic points,[7] it is postulated that there are at least three distinct nickel complexes in these baths. The ammonia-to-pyrophosphate ratio changes the relative concentrations of these complexes and causes the observed changes in plating rate. The complexes involved are probably:

$$Ni(P_2O_7)_2^{-6} \overset{NH_3}{\rightleftarrows} [Ni(P_2O_7)_x(NH_3)_y]^{-4x+2} \overset{NH_3}{\rightleftarrows} Ni(NH_3)_6^{+2}$$

The formation of the mixed complex apparently accounts for the rapid increase in plating rate as ammonia is added. Although there is no information about such a mixed complex with nickel, earlier investigations with copper have demonstrated the existence of a mixed complex for that cation when ammonia and pyrophosphate are present.[8] For our nickel baths, it is observed that solutions having a low ammonia content are unstable due to the formation of a precipitate. Furthermore, solutions having only nickel and pyrophosphate in a molar ratio of 0.82 to 1.2 form a solution when first mixed. When allowed to age, however, a gel-like structure[9] forms. The gel may be readily dissolved by addition of ammonia or any other complexing agent for the nickel ion. If the molar ratio of nickel to pyrophosphate is lowered sufficiently, i.e., to 0.59 or less, no gelling takes place.

Effect of Temperature

Like most chemical reactions, electroless plating processes are known to be temperature dependent. Fig. 4 shows the manner in which the main reaction products of the hypophosphite-containing bath (Ni, P, and H_2) are affected by variation in the deposition temperature. Assuming the Arrhenius equation to apply, the activation energy for the formation of each of these products is 14.0 ± 0.5 kcal/mole. The constancy of the activation energy value for these three products suggests that the value is associated with the decomposition of hypophosphite. All three products are formed by reduction involving a single intermediate (hydride). Apparently, the formation of this intermediate is the rate-controlling step, as suggested by Lukes.[10] It should be noted

that changing the operating temperature alters the composition of the deposit. In specific, deposits obtained at 25°C and 70°C contained about 2.5% and 5% phosphorus, respectively. This trend is consistent with a recently reported observation[11] that the percent phosphorus in deposits increases with increased temperature of deposition.

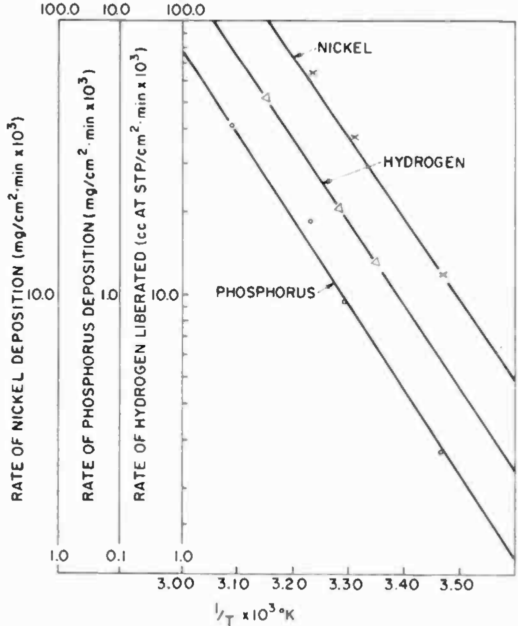


Fig. 4—Plating rate versus temperature of the nickel-phosphorus bath.

For the bath prepared with DMAB as the reducing agent, Fig. 5 shows the manner in which the plating rate varies with temperature. The corresponding activation energy for this chemical process is found to be 8.5 ± 0.5 kcal/mole. Due to the low boron content in the deposit, it is difficult to state what compositional trend, if any, results with temperature variations.

Activation on "Non-Catalytic" Metals

The direct electroless plating of nickel (Ni-P) onto metallic substrates is limited essentially to the following "catalytic" metals: nickel, cobalt, iron, palladium, and rhodium. In order to electrolessly plate onto other metals, either of the following approaches is conventionally used as a preliminary step:

1. Application of a dc "strike" of nickel that provides a thin catalytic film.
2. Incorporation of suitable catalysts such as palladium onto the surface.
3. Formation of a galvanic cell through contacting the substrate to be plated with a more active metal.

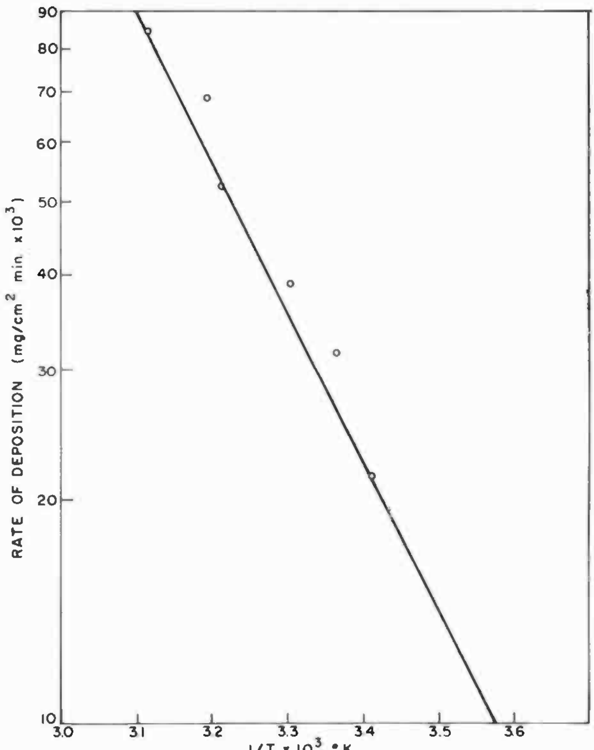


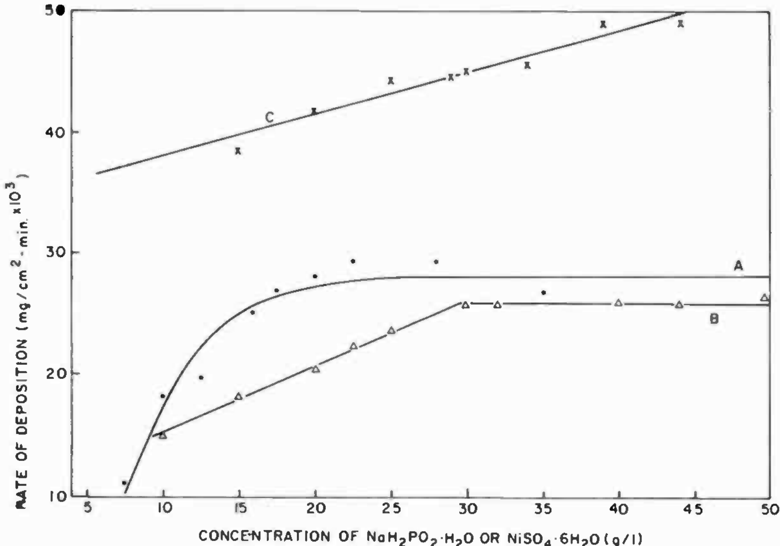
Fig. 5—Plating rate versus temperature for the nickel-boron bath.

In the course of this investigation, it was found that Ni-B will deposit directly on these same catalytic metals. It also deposits directly on copper, silver, gold, vanadium, chromium, and titanium at room temperature without any activation step. Other normally non-catalytic metals such as tungsten, molydbenum, and aluminum can be plated directly without an activation step if the bath is heated to about 40°C. In the case of selenium, direct initiation will take place at temperatures

of about 90°C. This unique characteristic is consistent with the low activation energy for the Ni-B bath.

Plating Rate Dependency on Reactant Concentration

For the NiP bath, the plating rate as a function of nickel and hypophosphite content was studied. As seen in Fig. 6, the bath can be pre-



A. Composition is $Na_4P_2O_7.10H_2O$-50 g/l, $NaH_2PO_2.H_2O$-25 g/l and NH_4OH to an initial *p*H of 10.5. $NiSO_4.6H_2O$ variable at 25.0 ± 0.2°C.

B. Composition is $Na_4P_2O_7.10H_2O$-50 g/l, $NiSO_4.6H_2O$-25 g/l and NH_4OH to an initial *p*H of 10.5. $NaH_2PO_2.H_2O$ variable at 25.0 ± 0.2°C.

C. Same composition as (B); however, at 35.0°C ± 0.2°C.

Fig. 6—Plating rate versus reactant concentrations.

pared so as to yield a plating rate independent of the nickel-ion concentration or, alternatively, independent of the hypophosphite concentration. Because these results appear to contradict earlier reports[1,2] concerning plating rate dependence on hypophosphite concentration for alkaline baths, this effect was examined in detail. It was found that the nature of the plating rate independency correlates with the molar ratio of nickel to hypophosphite.

The following extreme cases have been noted:

1) For $\frac{Ni^{++}}{H_2PO_2^-} > 0.2$, the plating rate is independent of the nickel ion concentration, but dependent on the hypophosphite concentration.

2) For $\frac{Ni^{++}}{H_2PO_2^-} < 0.2$, the plating rate is independent of the hypophosphite concentration but dependent on the nickel ion concentration.

In each of the above cases, the dependency on either nickel or hypophosphite was first order. Furthermore, although a plating rate inde-

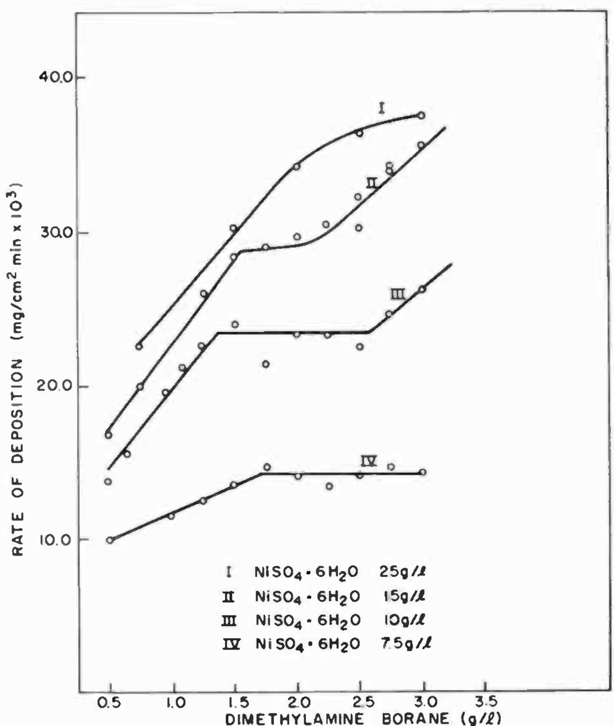


Fig. 7—Rate of deposition versus dimethylamine borane concentration at 25.0° ± 0.2°C.

pendent of hypophosphite concentration is obtained at room temperature, this independency is not retained if the temperature is raised. In specific, when the bath corresponding to Fig. 6b was operated at 35°C, a first-order dependency on the hypophosphite concentration was observed, rather than the independence characteristic of 25°C operation (Fig. 6c). For citrate- ammoniacal baths, the same behavior —a plating rate independent of the hypophosphite concentration—can be obtained for suitable composition.

The plating rate is independent of *p*H over a broad *p*H range whether the bath is nickel-ion-concentration dependent or reducing-agent-concentration dependent. Similarly, examination of the Ni-B bath demonstrated that the plating rate can be made independent of *p*H and either the nickel-ion concentration or the DMAB concentration as shown in Fig. 7.

Advantages

Operation of these baths at room temperature provides improved control over the bath composition, since little ammonia is lost under these conditions. The resulting deposits are generally fine-grained, dense and corrosion resistant. The appartus and the processing steps are very simple.

In metallizing semiconductor devices, the freedom to choose either phosphorus or boron as an impurity in the nickel provides a significant advantage. Ohmic contacts can be formed to either p-type or n-type silicon, as desired.

For the plating of plastics, baths operating at room temperature have a major advantage, especially for plastics that are heat sensitive. Adherent nickel layers up to several thousand angstroms thick were plated on a variety of plastics. The deposits initiate rapidly and the coatings are uniform and reproducible, especially with the room-temperature Ni-B bath.

Conclusions

Although the two electroless plating baths described in this paper employ different reducing agents, their kinetic behavior is quite similar. This similarity is ascribed to the active nickel complex(es) existing in solution. For both types of bath, it has been demonstrated that bath composition can be modified to yield

1. Plating rate independent of reducing agent, but dependent on the nickel-ion concentration;
2. or plating rate independent of nickel concentration, but dependent on the reducing agent concentration;
3. the plating rate is independent of *p*H for either of the above cases.

The ability of the DMAB-Ni bath to self-initiate on a wide variety of metallic surfaces is especially useful. It eliminates pretreatment, which is often required when plating is carried out with hypophosphite-

Ni. The baths have a number of advantages for the plating of electronic components and plastics and especially organic materials that are temperature sensitive.

Acknowledgments

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Fabrication of Al_2O_3 COS/MOS Integrated Circuits*

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Abstract—Complementary MOS integrated circuits with plasma-grown aluminum oxide as gate insulator have been fabricated for the first time. The basic requirements of the complementary technology have been achieved, i.e., low flatband voltage and stable oxide properties. In addition, radiation tests on these units confirm previous findings with MOS capacitors that the use of plasma-grown Al_2O_3 offers an increase in hardness by a factor of 50 or more over that of conventional units with SiO_2.

Introduction

In Metal-Oxide-Semiconductor (MOS) devices the dielectric film used as gate insulator is an active, integral part of the device, and device operation and characteristics are very sensitive to its properties. Hence, in MOS technology, emphasis is placed on the fabrication of this oxide rather than on diffusion, as in bipolar technology.

For a large number of noncritical applications, the currently commercially available MOS devices and integrated circuits with SiO_2 gate oxide are adequate. The processing is now well under control and has been reduced to a relatively straightforward procedure. Excellent results have been obtained with increasingly larger and more sophisticated integrated circuits, so that low-cost large-scale integration (LSI) of MOS circuits offers considerable promise for the future. However, for certain more critical requirements, two major reliability problems have been encountered: (1) the migration of minute traces of impurities through the films, especially at elevated temperatures and under high field conditions, results in serious drifting and changes in the device characteristics; (2) radiation also causes drift and/or degradation in device characteristics due to charge generation and trapping in the oxide.

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Recently, technological advances were made that allow improved performance of MOS devices in these areas by utilizing aluminum oxide as the gate insulator. Aluminum oxide made by two different techniques has led to significant improvements in resistance to both bias-temperature stress and radiation exposure.[1-3] These techniques are: (1) plasma anodization of Al,[4,5] and (2) low temperature pyrolytic decomposition[6] of Al-alkoxides. Plasma-grown Al_2O_3 shows, at present, greater promise for COS/MOS applications and will be the subject of this paper.

From the fabrication of MOS devices it was found that plasma-grown Al_2O_3, when used as the gate insulator, can lead to the following advantages:

1. *Low Ion Drift Properties:* Al_2O_3 resists ion drift up to two orders of magnitude more than SiO_2, indicating that MOS devices made from it exhibit stability to bias-temperature stress. This property manifests itself in two very practical results: (a) ultraclean technology as required for SiO_2 (state-of-the-art)[7] devices would *not* be necessary (this should reflect itself in the cost, yield, and uniformity of LSI arrays), and (b) Al_2O_3 could act as a junction seal and encapsulant for both MOS and bipolar LSI. A thin film of Al_2O_3 on a junction or over an MOS device would act as a passivation layer giving the equivalent of a hermetic seal.

2. *Radiation Resistance:* Measurements made to date on MOS devices on single crystal silicon show good radiation resistance,[1,2,8] better than SiO_2[9] and Si_3N_4 devices.[10] This is important to arrays that will be exposed to the radiation fields of space or nuclear environments. The reason for this improvement is most probably connected with the particular defect structure of Al_2O_3.

Other important properties of the plasma grown oxide are summarized in Table 1.

Table 1—Properties of Plasma-grown Al_2O_3

Property	Value
Relative Dielectric Constant	8.0 − 8.7
Loss Tangent ($f = 100$ kHz)	0.02
Surface State Density	2×10^{10} states/cm^2-eV
Index of Refraction	1.67 − 1.70

The Plasma-Anodization Process

The technique of plasma anodization of a metal to form the metal oxide is a relatively new one and, to date, has been primarily used to form oxides of metals for thin-film capacitors. The most prominent ma-

terials[4,5] formed have been Al_2O_3 and Ta_2O_5. In general, it has been found that these insulating films are amorphous, with a low dissipation factor and a high breakdown voltage.

Plasma anodization is carried out in a vacuum system that has been modified as shown in Fig. 1. The aluminized silicon wafer is placed in

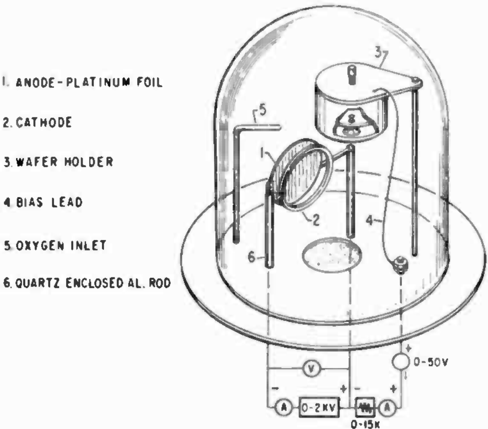

Fig. 1—Schematic representation of the plasma anodization chamber.

a closed, insulating, sample holder that has openings for exposure of the front surface of the wafer and for admission of a contact lead. Electrical contact is made to the back of the wafer with a pressure-contact jig. Once the sample is in place, the system is evacuated to 1×10^{-6} torr and back-filled with dry oxygen. The pressure is set at 0.3 torr and a glow discharge is ignited between anode and cathode. The sample, which is in the glow or "positive column" portion of the discharge, is biased positively with respect to the wall potential (defined as the potential that, when applied to a conducting probe in a plasma, reduces the current flow to zero). Because the wall potential may vary considerably during one anodization, depending on the condition of the anode, it must be monitored throughout the anodization. This is accomplished by adding an additional electrode to serve as a plasma probe.

The growth rate of the oxide is greatly dependent on the geometry of the anodization system and is not always linear with voltage. If the film is thick enough so that it is not completely anodized, the growth is self-limiting in a fashion analogous to that of wet anodization. Typically, the oxide is observed to grow at 22 Å/V, although this can vary considerably with the geometry of the anodization system

and the mode of operation.[11] For MOS applications, the aluminum film must be completely anodized, since any free Al at the interface would act as surface states. Hence, a potential sufficient to anodize all the aluminum must be applied. If this potential is too high, however, a thin film of SiO_2 can be formed at the silicon interface, causing electrical instability (hysteresis in *C-V* testing) as well as deterioration in the resistance to ionizing radiation. The presence of the SiO_2

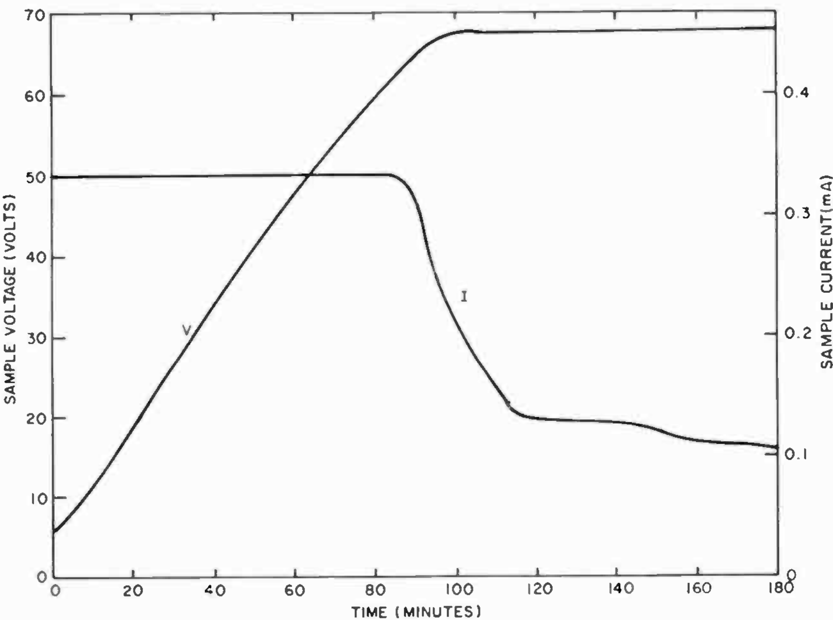

Fig. 2—Variation of sample voltage and current with time during plasma anodization of a typical MOS unit.

layer can be detected by ellipsometry measurements, which reveal considerable deviation in the index of refraction and measured film thickness from that expected for Al_2O_3 alone. For the circuits fabricated in this investigation, good-quality Al_2O_3 films on Si were obtained under conditions listed in Table 2. As shown in Fig. 2, a constant current is maintained until the desired voltage, indicative of a certain film thickness, is obtained. This voltage is then held constant and the current is allowed to decay. The net voltage on the sample is the applied voltage minus the wall potential.

The utilization of the plasma-grown oxide is much more difficult for active device configurations than for simple MOS capacitors be-

cause of the peculiar etching characteristics of this oxide. The most straightforward fabrication scheme would be to chemically etch the required geometrical patterns in the oxide after its formation. However, upon exposure to hot phosphoric acid (80 to 180°C), the plasma-grown oxide softens and eventually peels from the substrate. Similar effects are observed upon exposure to buffered HF. Hence, direct chemical etching cannot be utilized at the present. Thus, an alternate technique, namely etching of the aluminum film prior to anodization, was developed and refined sufficiently to allow device fabrication.

Table 2—Typical Plasma Anodization Parameters

Parameter	Value
Pressure	0.3 torr (oxygen)
V_P (anode to cathode voltage)	800 to 1100 V
I_P (plasma current)	40 to 60 mA
Aluminum thickness	420 Å
Initial sample current	0.3 mA/cm^2
Final applied voltage	60 to 70 V
Total time of anodization	2 to 3 hours
Al_2O_3 thickness	640 Å

COS/MOS Processing With Plasma-Grown Al_2O_3

A. General Procedure

The processing of the wafer proceeds in the same manner as for the conventional SiO_2 unit up through step 6 of Fig. 3. At this point, there are two schemes that can be utilized, depending on whether the stepped SOi_2 is to be under or over the Al_2O_3 layer.

In the A version, illustrated in Fig. 4, SiO_2 is removed from the active region only, leaving the stepped oxide on the remainder of the wafer. The wafer is then metallized (420 Å of aluminum), contact holes are formed in the aluminum film, and anodization of this film is carried out under the conditions listed in Table 2.

In the B version, all oxide is removed from the entire wafer. The wafer is then metallized, contact holes are formed in the aluminum film, and the anodization is carried out in the normal manner. Finally, SiO_2 is deposited and then densified at 800 to 1000°C before the desired stepped-oxide pattern is formed.

In either version, the unit is completed by first removing the oxide formed in the contact holes during the anodization by a 30 sec etch in buffered HF, followed by an anneal at 350°C for one hour in hydrogen,

and finally by forming the contact metallization. The units are then electrically probed, and acceptable units are selected from the diced wafer and bonded into 14-lead flatpacks for testing. The topological view of a completed unit is shown in Fig. 5. A schematic cross section showing external connections is shown in Fig. 6.

B. Critical Process Steps

1. Wafer Preparation—The wafer must be free of both particulate contamination and adsorbed moisture prior to aluminum metallization, since either can result in oxide defects (bubbles, pinholes, etc.), thereby causing failure by electrical conduction. The effects of moisture can be largely eliminated by heating the wafer in an inert ambient prior to metallization. Particulate contamination is minimized by careful clean-

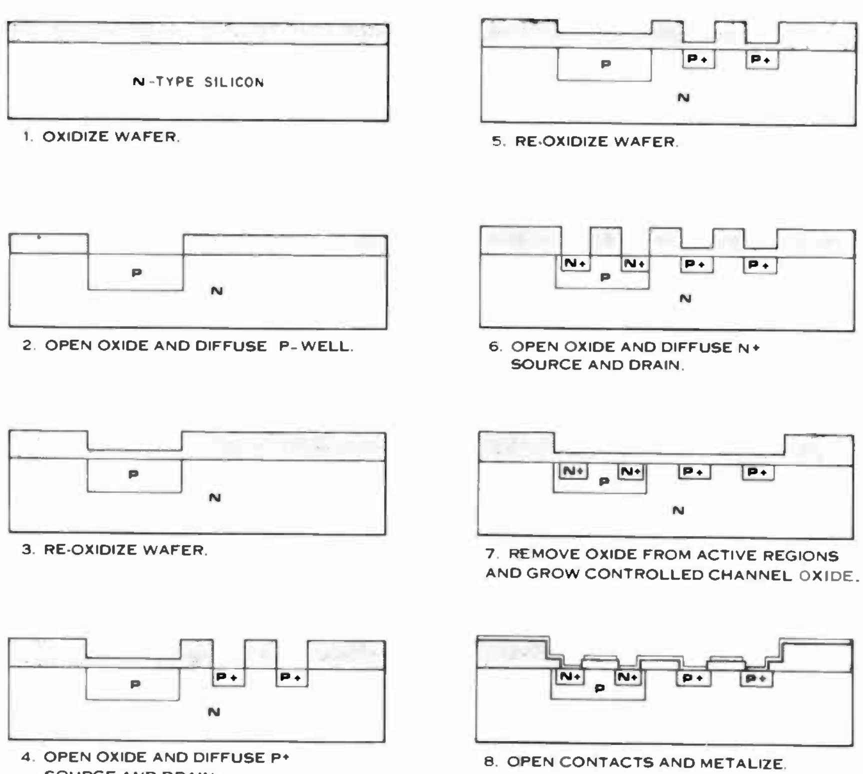

Fig. 3—Major processing steps for complementary MOS integrated circuits with thermally grown SiO_2 channel oxide.

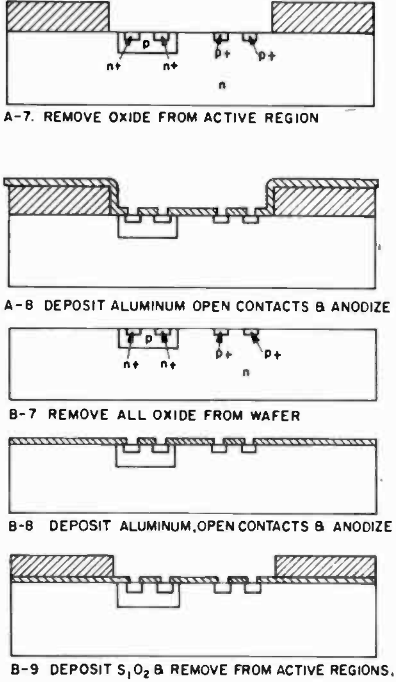

Fig. 4—Major processing steps for utilization of plasma-grown Al_2O_3 in complementary MOS integrated circuits.

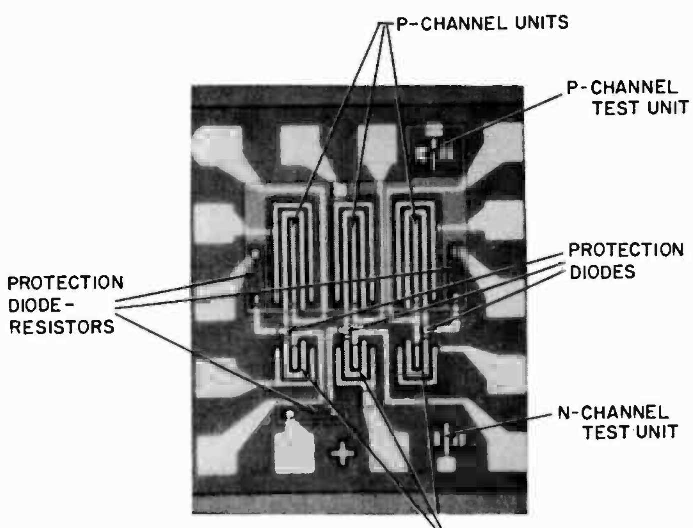

Fig. 5—Topological view of RCA CD-4007 Dual Complementary Pair Plus Inverter.

ing immediately before placing the wafer in the vacuum system for metallization.

2. Aluminum Deposition—Since the oxide thickness is determined by the thickness of the aluminum film, the metallization must be accurately controlled. This can be done quite easily with a quartz crystal monitor. The thickness is normally verified optically by the Tolansky interference technique. Verification is important, since over-anodization results in the formation of a thin SiO_2 layer at the silicon interface and, in some cases, is responsible for the appearance of oxide defects such as bubbles or other fine structures.

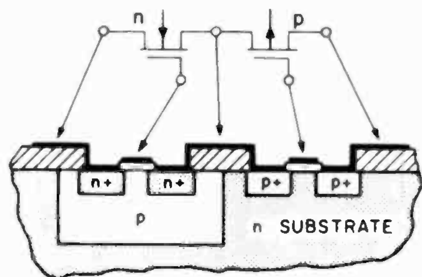

Fig. 6—Cross-section view of COS/MOS inverter showing external connections.

3. Measurement of Sample Voltage—As indicated above, the effective voltage applied to the sample is the supply voltage minus the wall potential. The wall potential is determined not only by the plasma parameters, but also by the condition of the anode. During a given anodization, the wall potential increases in magnitude. In some cases, for an anode that has been reused a number of times, the wall potential may vary by as much as 10 V during an anodization. Hence, the wall potential must be monitored continuously. Monitoring is achieved by a plasma probe in conjunction with a high impedance meter, such as an electrometer or nulling volt-meter. Errors result if the input impedance of the meter is below 10^9 ohms.

4. Control of Current Density—Control of the current density is necessary to obtain high-quality oxide in a reasonable time. If the current density is too high, especially as the growth approaches the silicon interface, oxide defects such as bubbles or fine grainy structure result. On the other hand, if the current density is too low, the anodization proceeds too slowly.

5. Effects of Stepped Oxide—When the Al_2O_3 is formed over the stepped oxide, as in version A of Fig. 4, additional care must be taken

to ensure that the aluminum is completely anodized over the SiO_2 regions. In version B, the etching of the desired pattern in the SiO_2 overlying the Al_2O_3 must be controlled very accurately, since buffered HF attacks the Al_2O_3–silicon interface, causing the oxide to peel.

6. Removal of Oxide from Contact Holes—During the anodization, 50 to 100 Å of SiO_2 form in the contact holes. This oxide must be removed by buffered HF so that contact can be made to the source and drain regions of the devices. Because the buffered etch attacks the Al_2O_3, photoresist is used to protect the Al_2O_3 during this step.

Electrical Properties

Both discrete n-channel units and complementary symmetry MOS inverters (CD-4007) with plasma grown Al_2O_3 as the gate insulator have been evaluated. In general, a lower yield and a reduction in device quality has been found in comparing the discrete ring-dot units with the individual MOS units on the CD-4007 circuit, as summarized in Table 3. This is attributed to the greater complexity of the circuit over the discrete ring-dot structure and, in particular, to difficulties involving the formation of the stepped oxide, which was not utilized for the discrete structure.

Table 3—Comparison of Discrete MOS Characteristics on CD-4007 and Ring-Dot Test Units

Unit		Threshold (Volts)	Field-Effect Mobility (cm^2/V-sec)
CD-4007	n-channel unit	$+4.0 \pm .5$	23
Plasma Al_2O_3 (640 Å)	p-channel unit	$-2.0 \pm .5$	46
CD-4007	n-channel unit	$2.0 \pm .5$	102
SiO_2 (1000 Å)	p-channel unit	$-1.5 \pm .5$	144
Ring-Dot Plasma Al_2O_3	n-channel unit	$1.5 \pm .5$	150

Typical transfer characteristics for inverter pairs on the CD-4007 chip are shown in Fig. 7, together with the current flow from the power supply. The schematic for these inverters is also shown in the figure. The characteristics of the plasma-grown Al_2O_3 units are offset to the right of those of the conventional SiO_2 units due to the large threshold of the n-channel units, and they are somewhat distorted due to contact resistance. On the other hand, there is no appreciable current flow in either steady state condition ($V_{in} = 0$ or $+10$ V) as required for most COS/MOS applications. With refinements in the processing technology, these characteristics should be improved considerably.

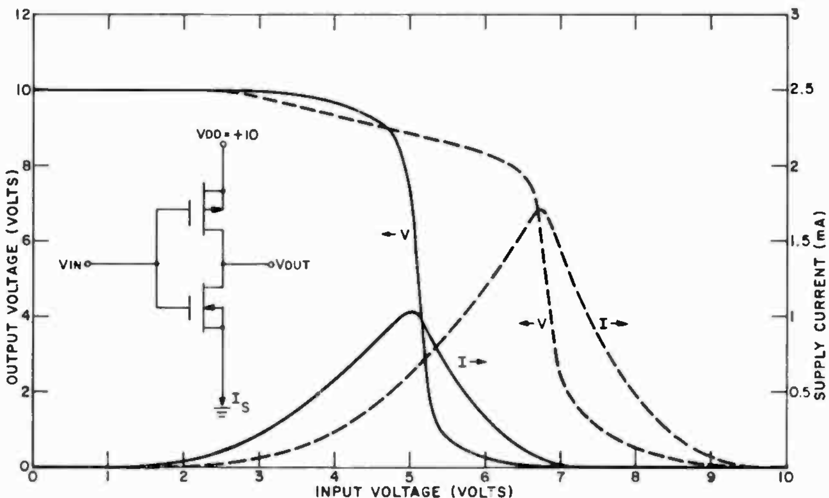

Fig. 7—Typical transfer characteristic of CD-4007 inverter for connection shown in insert: solid curve for conventional SiO_2 unit, dashed curve for unit with plasma-grown Al_2O_3.

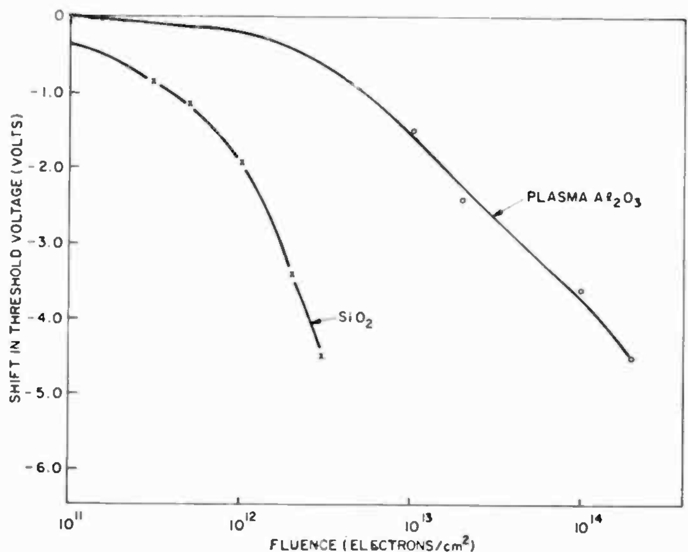

Fig. 8—Shift in threshold voltage as a function of fluence for CD-4007 inverters with $V_{in} = +10$ volts during bombardment.

Small shifts (~0.5 V) in these transfer characteristics due to bias temperature stress (150°C, 10 V, 5 min) have been observed. However, these are opposite in direction to shifts caused by positive ion drift and are attributed to interface-state effects.

The units with plasma-grown oxide show promise of considerable radiation hardness, as illustrated by the comparison shown in Fig. 8.[12] All units were bombarded with 1-MeV electrons in the Van de Graaff facility at RCA Laboratories. Fig. 8 shows the net shifts in threshold voltage for the CD-4007 for an input voltage of +10 V, which is the most severe condition for the conventional SiO_2 units. These results, together with additional tests under other biasing conditions, indicate that the use of plasma-grown Al_2O_3 offers an increase in radiation hardness by a factor of 50 or more over that of the conventional units with SiO_2.

Conclusions and Recommendations

The results reported in this paper clearly show two major achievements:

1. The first successful fabrication of operating integrated circuits using Al_2O_3 as gate insulator, thus proving the feasibility of an Al_2O_3-MOS technology.
2. The first demonstration that the degree of radiation hardening, expected from MOS-capacitor data, has been achieved in active device structures and integrated circuits.

Considerable work remains to be done, especially in the areas of geometrical pattern definition, optimization of oxide properties and formation techniques, and active-device fabrication. Once these difficulties have been eliminated, and statistically significant results have been obtained, there will be enough confidence in the Al_2O_3 technology that it can be transferred into an experimental line for fabrication of integrated circuits. This can then lead to a radiation-resistant technology for integrated-circuit capability.

Acknowledgements

C. Benyon, J. Groppe, G. Mark, and J. Shaw assisted during fabrication and testing of the devices; D. Flatley, W. French and J. Scott provided the CD-4007 substrates, and F. Kolondra participated in radiation testing of the completed devices. The authors are indebted to all.

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Optimization of Charge Storage in the MNOS Memory Device

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Abstract—The charge-storage performance of MNOS (Metal Nitride Oxide Silicon) memory devices operating in the direct-tunneling mode has been studied as a function of two fabrication parameters: (1) deposition temperature of the Si_3N_4 layer and (2) thickness of the SiO_2 tunneling layer. The deposition temperature of the Si_3N_4 was varied from 650 to 1100°C; the optimum value was found to be about 700°C. The SiO_2 thickness was varied from 16 to 35 Å and the optimum value was found to be about 20 Å. Memory transistors were fabricated using these optimum values. Gate threshold voltage shifts of 2 volts were obtained using switching pulses of 100 nanoseconds duration and ±34 volts amplitude.

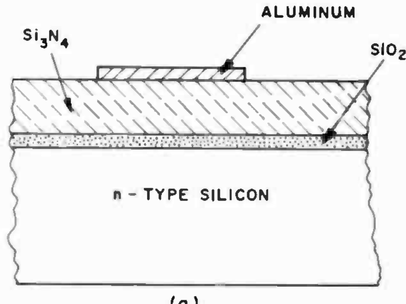
Introduction

A new memory element has recently been developed that utilizes the hysteresis effects observed in connection with certain insulators in MIS field-effect transistors.[1-3] In more conventional approaches to the application of transistors to provide information storage, the transistors, which exhibit no hysteresis, are combined into a circuit that does exhibit hysteresis.[4] The memory function then is a property of the circuit. In the memory behavior described in this paper, the transistors themselves have memory; each transistor is capable of storing one bit of information.

The usual form of these transistors is a standard IGFET (Insulated-Gate Field-Effect Transistor) structure in which the SiO_2 (silicon dioxide) gate insulator is replaced by a double insulator, typically a layer of of SiO_2 nearest the silicon substrate and a layer of Si_3N_4 (silicon nitride) over the SiO_2. This structure is commonly called a Metal-Nitride-Oxide-Silicon (MNOS) memory transistor. The hysteresis is associated with the existence of traps (electronic states) at or near the SiO_2–Si_3N_4 interface, and the threshold voltage of the IGFET is influenced by the charge state of the traps.

There are several possible modes of operation by which the traps can be charged and discharged. These include direct tunneling between the traps and the silicon;[5] Fowler–Nordeim tunneling through the SiO_2 barrier;[6] bulk conduction in the Si_3N_4, which can be in the form of several different mechanisms;[6-7] and direct carrier injection over the Schottky barrier between the silicon and the SiO_2.[8] The devices treated in this paper are intended to operate in the direct tunneling mode.

In this paper we report the effect of varying the SiO_2 thickness and the Si_3N_4 deposition temperature on the operation of MNOS devices, and determine practical values of these parameters for fabricating useful devices.



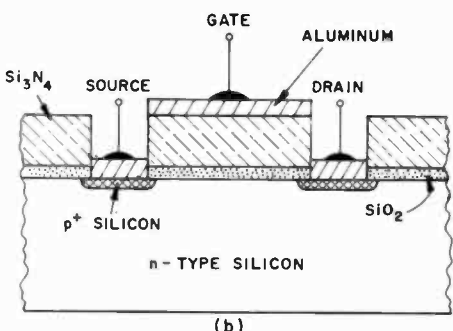


Fig. 1—Schematic illustration of MNOS devices: (a) capacitor, (b) transistor.

The MNOS Memory Transistor

Schematic illustrations of an MNOS capacitor and an MNOS transistor are shown in Figs. 1(a) and 1(b), respectively. Traps exist at or near the interface between the SiO_2 and the Si_3N_4. These traps can be charged and discharged by the application of a sufficiently large voltage

of suitable polarity to the gate electrode. The charge states of the traps influence the silicon surface potential and, therefore, can affect the threshold voltage of the MNOS transistor. The charge states are stable and electronically alterable, which makes them ideally suited to perform a memory function.

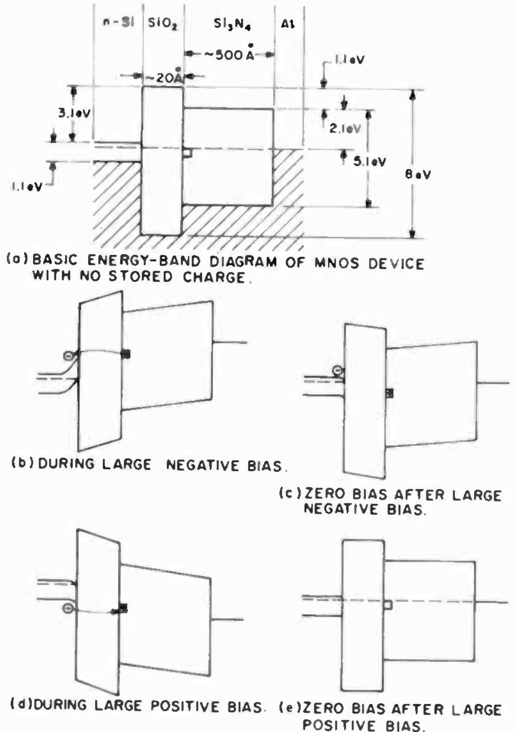


Fig. 2—Energy-band diagrams of an MNOS device for various bias conditions.

If the SiO_2 layer is made sufficiently thin (<35-40 Å), the traps can communicate with the silicon by direct tunneling through the SiO_2 energy barrier. The basic electron energy-band diagram of the physical model, which can be used to explain the switching characteristics of such a direct-tunneling mode transistor, is shown in Fig. 2(a).[3] For simplicity, the traps, which are indicated by squares in Fig. 2, are assumed to be donor-type.

Each trap is assumed to be electrically neutral when filled with an electron, and positively charged when empty. Application of a large negative voltage to the gate, as indicated in Fig. 2(b), raises the

traps in energy relative to the silicon, permitting those traps that are energetically above the conduction band edge of the silicon, and are within a probable tunneling distance, to give up an electron to the silicon. When the gate voltage is returned to ground, as shown in Fig. 2(c), the empty traps, which are now positively charged, are energetically opposite the forbidden gap of the silicon, and are therefore metastable.

In a similar fashion, application of a large positive voltage permits electrons to tunnel from the silicon valence band back to the traps, thereby neutralizing their positive charge and returning them to their original charge state. This process is indicated in Figs. 2(d) and 2(e).

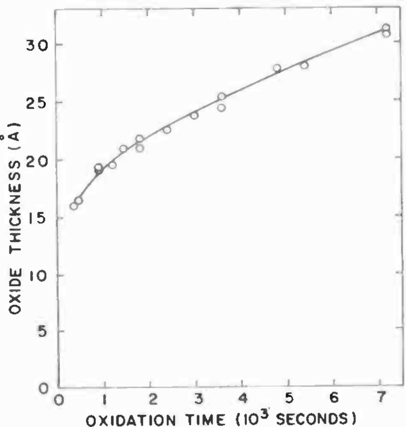


Fig. 3—Growth of silicon dioxide on silicon in water at 600°C.

Insulator Preparation

A *sine qua non* for the fabrication of direct-tunneling-mode MNOS memory transistors is the capability for growing SiO_2 (on Si) that is thin enough to permit direct tunneling to occur. Suitable films of SiO_2 can be prepared at 600° C in a water-vapor ambient, and the techniques required to produce these films have been previously presented.[9] Experimental data showing the thickness of SiO_2 grown versus the oxidation time in water vapor at 600° C are shown in Fig. 3. These data can be predictably reproduced with a maximum deviation from the desired thickness of about 1 Å. The thickness of the SiO_2 is measured by ellipsometry.

The Si_3N_4 is deposited in a resistance-heated furnace by the reac-

tion of silane (SiH_4) and ammonia (NH_3). The ammonia-to-silane ratio is maintained at about 10^4:1. This is to ensure a low bulk conductivity for the Si_3N_4, which results in good device performance. The Si_3N_4 thickness is also measured by ellipsometry.

Experimental Results

A series of experimental samples was prepared to determine the effect of the deposition temperature of the Si_3N_4 on the physical and electrical properties of the MNOS structure. The Si_3N_4 was deposited in the temperature range 650–1100° C. In these samples, the thickness of the SiO_2 layer was maintained at 20 Å, and the Si_3N_4 thickness varied from 500–750 Å from sample to sample, with very good uniformity over each sample. The substrate material was 10 ohm-cm, n-type, (100) oriented silicon.

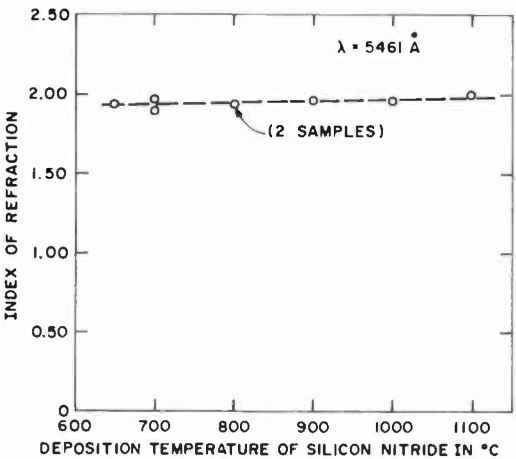


Fig. 4—Index of refraction of silicon nitride as a function of deposition temperature.

The index of refraction of the Si_3N_4 was independently determined by ellipsometry, and is shown as a function of the Si_3N_4 deposition temperature in Fig. 4. The uniformity of the index of refraction over the investigated temperature range indicates that no change of phase in the Si_3N_4 is encountered as the deposition temperature is varied within this range.

Aluminum dots with diameters of the order of 25 mils were evaporated through a metal mask to form MNOS capacitors. The capacitor areas were determined by taking photomicrographs of known

magnification and subsequently measuring the micrograph areas with a planimeter. An evaporated aluminum back contact to the silicon was provided.

Measurements of the capacitance of the MNOS structure were taken at 100 kHz with the silicon surface biased heavily into the

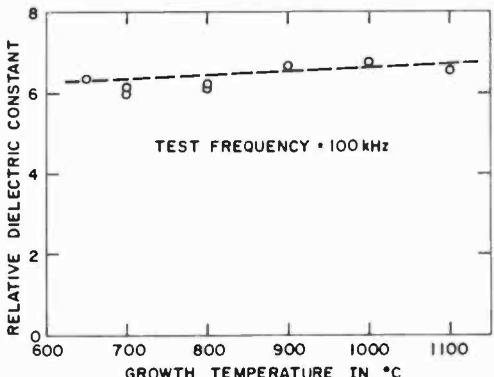


Fig. 5—Relative dielectric constant of silicon nitride as a function of deposition temperature.

accumulation region. The relative dielectric constant, K_n, of the Si_3N_4 was then calculated from the relation

$$K_n = \frac{l_n}{\left[\frac{A}{C} - \frac{l_{ox}}{K_{ox}\epsilon_o}\right]\epsilon_o}, \qquad [1]$$

where C is the measured capacitance, l_n is the thickness of the Si_3N_4, l_{ox} is the thickness of the SiO_2, K_{ox} is the relative dielectric constant of the SiO_2, ϵ_o is the permittivity of free space. The variation of K_n as a function of deposition temperature is shown in Fig. 5.

Measurements of the bulk conductivity of the Si_3N_4 layers were taken, again with the silicon surface accumulated. The results are presented in Fig. 6 in the form of current density versus the square root of the applied field. All of the individual sample data exhibit a linear slope over many orders of magnitude, indicating that conduction occurs through the Frenkel–Poole mechanism.[7]

Typical data for the measurement of capacitance versus voltage (C-V) of MNOS capacitors is indicated in Fig. 7. The curve labeled

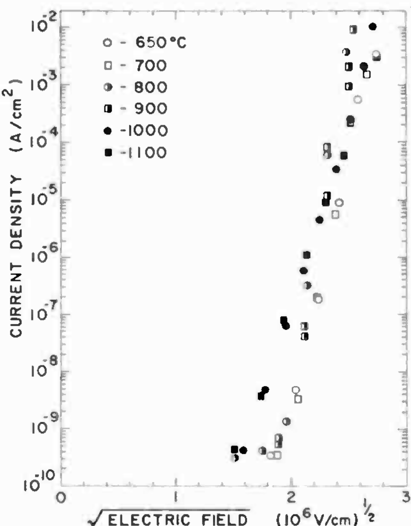


Fig. 6—Current density versus square root of electric field for Si_3N_4 layers deposited in the temperature range 650–1100°C.

original is the *C-V* characteristic of the capacitor prior to the application of large gate fields. The other curves are the *C-V* characteristics that result from holding the gate at the designated potential for 10 seconds prior to the measurement. At some point, the application of an increased voltage causes no further shift in the *C-V* characteristic. When this occurs the maximum possible charge is stored. This is indicated by the curve labeled —25 and —30 in Fig. 7. The voltage offset from the origin for the individual curves is measured at the flat-band capacitance value, which is indicated by the dotted line in Fig. 7.

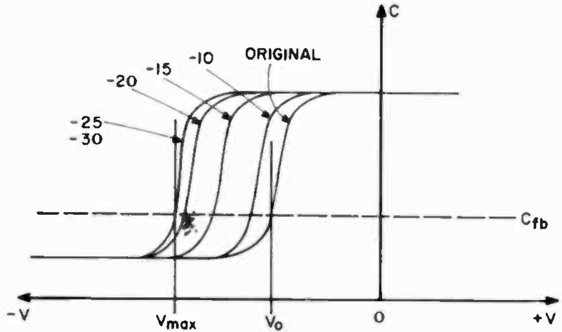


Fig. 7—Typical *C-V* data for MNOS capacitor.

The charge stored in the MNOS structure is determined, to a good approximation, from the relation

$$Q = -\frac{V_{fb} K_n}{l_n} \times 5.5 \times 10^{13}, \qquad [2]$$

where Q is measured in units of the magnitude of the electronic charge per square cm of surface area, V_{fb} is the flat-band voltage in volts, and l_n is the silicon nitride thickness in Å.

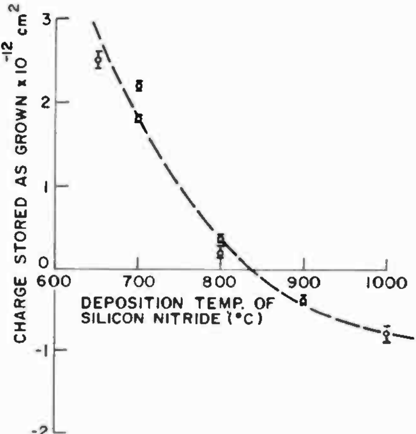


Fig. 8—Initial charge stored in MNOS structure versus deposition temperature of silicon nitride.

The charge stored in the capacitor as grown, Q_o, is determined by substituting the initial offset voltage, V_o, into Eq. [2]. The values of K_n and l_n are known from previous measurements for the individual samples. The results of the experimental determination of Q_o as a function of the Si_3N_4 deposition temperature are shown in Fig. 8. No data are presented for 1100° C, because large currents flowed when positive voltages were applied to this sample.

An important result of the experiment described above is that the charge initially stored in the double-insulator structure can be monotonically varied from positive charge for growth temperatures below about 850° C to negative charge for deposition temperatures above 850° C. This ability to selectively vary the magnitude and sign of the initially stored charge is potentially significant even for applications other than memory transistor arrays.

The maximum positive charge that can be stored in the structure,

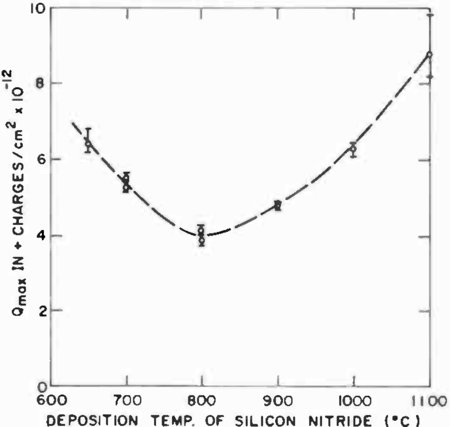


Fig. 9—Maximum positive stored charge for negative potential versus deposition temperature of silicon nitride.

Q_{max}, is shown as a function of the Si_3N_4 deposition temperature in Fig. 9. The maximum possible threshold shift for the MNOS structure is proportional to Q_{max}.

Of great importance to the practical application of MNOS memory transistors is the long-term retention of the stored charge. The charge storage as a function of time was measured in the following manner. A sufficiently large negative voltage was applied in order to store the maximum possible positive charge. The voltage across the capacitor was then reduced to zero, and periodic measurements of the flat-band voltage were made, with the voltage reduced to zero after each measurement. The charge stored as a function of time was normalized to the maximum stored charge and is presented in Fig. 10.

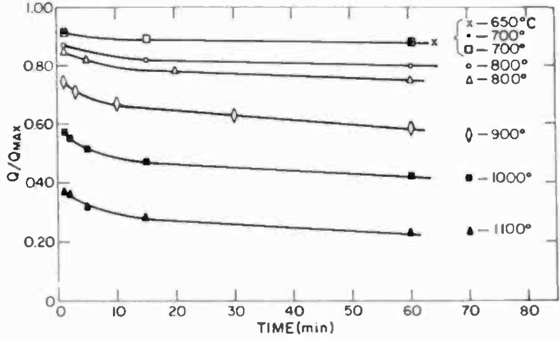


Fig. 10—Charge stored versus time with deposition temperature as a parameter.

The mechanism responsible for the relaxation of the stored charge is thought to be the following. The charge stored in the traps causes an electric field to exist in the Si_3N_4. This causes charge to be conducted from the traps, which in turn reduces the field in the Si_3N_4. This mechanism is consistent with the current density, as determined from an extrapolation of the data in Fig. 6, that would flow due to an electric field of the magnitude produced by the amount of charge stored. The fact that the ability to retain charge decreases with increasing deposition temperature also supports this theory, since the bulk conductivity of the Si_3N_4 in the low-field regions increases with increasing deposition temperature. Also, since the current density is a strongly nonlinear function of the electric field, the decrease of the stored charge at a decreasing rate is expected, in good agreement with the results shown in Fig. 10. There is also the possibility that alternative mechanisms for relaxation of the stored charge exist and may even dominate the device performance when the Si_3N_4 conductivity is sufficiently low. This possibility is currently being investigated.

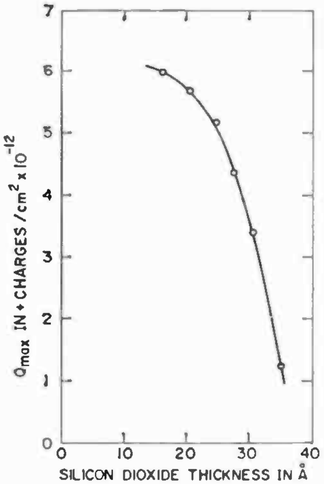


Fig. 11—Maximum charge stored versus SiO_2 thickness.

A second series of experimental capacitors was prepared. The Si_3N_4 was deposited at 700° C for each of the samples, and the thickness of the thin SiO_2 layer was varied between 16 and 35 Å. The maximum positive charge that could be stored, Q_{max}, is shown as a function of SiO_2 thickness in Fig. 11. The data indicate that for oxide thicknesses greater than $\approx$ 35–40 Å, the ability to alter the charge in the traps is lost. This is in good agreement with the theoretical tunneling distance

in SiO_2 for a measurement time of a few seconds.[10] The experimental data also support the previous assumption of a spatial distribution of traps, which was invoked to explain the switching behavior of MNOS transistors.[5]

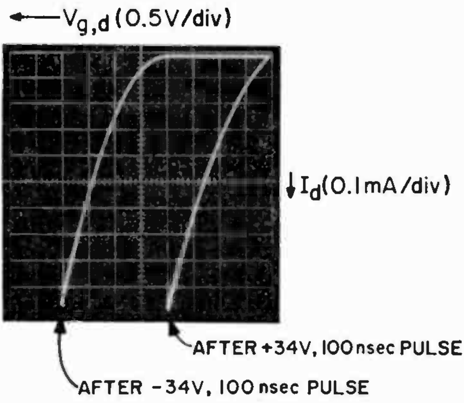


Fig. 12—Drain current versus voltage applied to both gate and drain.

Finally, the previous experimental results were used as a guide in preparing experimental MNOS transistors. The transistors have a channel width of 0.3 mil and a channel length of 5 mils. The gate insulator is made up of a 20-Å film of SiO_2 and a 425-Å film of Si_3N_4. The Si_3N_4 was deposited at 700° C. The transfer characteristics of one of these transistors is presented as the drain current versus the voltage of the gate and the drain (connected together) to the source and substrate (connected together) in Fig. 12. The two characteristics shown correspond to the two stable states associated with switching pulses of 100 nanoseconds duration and ±34 V.

The state of the transistor can be interrogated with a gate pulse of —1.5 volts amplitude. If it is in the "off" state (after —34 V pulse), there will be no drain current. If it is in the "on" state (after +34 V pulse), there will be about 0.6 mA of drain current. This is shown very clearly in the three terminal characteristics of the devices presented in Fig. 13.

Conclusions

The results of this work indicate that Si_3N_4 to be employed in direct-tunneling mode MNOS memory transistors should be deposited at about 700° C. This temperature represents a practical compromise

among the requirements of large trap density, long-term charge retention, and the deposition rate of the Si_3N_4.

A thickness of 20 Å for the SiO_2 is a practical value in terms of both maximum charge storage and reproducibility.

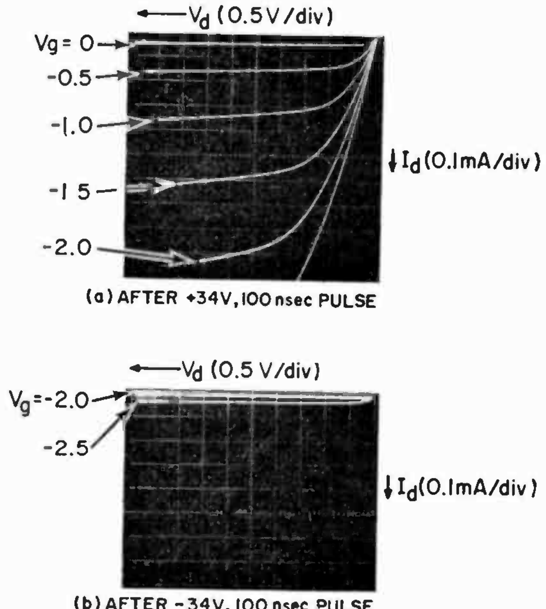


Fig. 13—Drain current versus drain voltage with gate voltage as a parameter.

Acknowledgments

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The Epitaxial Growth of Silicon on Sapphire and Spinel Substrates: Suppression of Changes in the Film Properties During Device Processing

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Abstract—The electrical properties of silicon thin films on insulating substrates change during the thermal treatments used in device processing. These changes can be associated with contamination of the films by substrate constituents. Suppression of the contamination by adjustment of the epitaxial growth conditions, and use of a new substrate material, has led to considerable improvements in the stability of the properties. An after-oxidation hole mobility of 165 cm^2/V-sec, with a hole concentration of 5.2×10^{15}/cc, has been achieved in a 1.7-micron thick film on $(1\bar{1}02)$ sapphire. At a similar hole concentration, an after-oxidation mobility of 300 cm^2/V-sec has been observed in a 1.5-micron thick silicon film deposited on (111) spinel.

Introduction

It is important to make available for solid-state microcircuit applications single-crystal thin films of silicon on insulating substrates with semiconducting properties similar to the properties of bulk silicon. The realization of good quality silicon on dielectric, rather than semiconducting, substrates is important for a number of reasons:

- Complete electrical isolation is obtained between individual devices; this is of particular importance in closely spaced integrated arrays.
- Both active and passive components may be fabricated on the insulating substrates; thus, entire circuits may be included on one substrate.
- Parasitic capacitances are eliminated; in silicon-on-silicon structures the active components are electrically isolated from the semiconducting substrate by back-biased p-n junctions that contribute troublesome capacitance, particularly in high-frequency circuits.

–Radiation resistance of devices should be enhanced; in silicon-on-silicon devices, radiation-induced currents are generated at the device–substrate junctions.

The problem has been not only one of achieving near bulk electrical properties in the thin films, but also of maintaining the as-deposited properties during the thermal treatments used in device processing. The two considerations are of equal importance. The most critical device-processing step is the growth of the gate oxide in an oxidizing ambient at $\sim 1100°C$.

The semiconducting properties of silicon epitaxially grown on the insulating substrate materials appear to be limited by three basic factors[1]:

–the crystallographic mismatch between silicon and the substrate crystal.[2-4]

–contamination of the silicon film as the result of chemical reactions between the deposition constituents and the substrate material.[3,5-7]

–stress in the silicon due to the difference between the thermal coefficients of expansion of the silicon and the substrate; the stress is introduced as the composite cools from the deposition temperature.[1,8,9]

The as-deposited semiconducting properties are strongly influenced by all three factors cited. The change in the film properties during thermal oxidation appears to be dominated by the impurity content of the silicon.[7] The lattice mismatch and thermal coefficient of expansion may be adjusted by choice of substrate crystals. The impurity content, however, is not only a strong function of the reactivity of the substrate surface, but also of the deposition conditions. Since the crystalline perfection of the silicon thin film is influenced by both the lattice mismatch and the impurity content, this property is also a strong function of the deposition conditions. Therefore, the approach to suppressing changes in the electrical properties during device processing involves both the choice of a substrate material and adjustment of the deposition conditions. In this study, a variety of growth parameters were investigated on single-crystal alumina (sapphire) and magnesium aluminate (spinel) substrates.

Sapphire and Spinel as Substrate Materials

A number of materials have been considered as substrates for the growth of epitaxial silicon films. A review of the results obtained was

recently published.[1] Of all the materials considered or investigated, only single-crystal sapphire, spinel, and beryllia are now under investigation to any extent at various laboratories in the U. S. and Europe. Sapphire is commercially available and has been the most extensively studied substrate material.[1,10-12] Electrical properties usable for a variety of device applications[13] have been obtained in silicon on sapphire, and effort continues to further improve the silicon–sapphire composite, as shown in this paper.

Although recent research has yielded more control over the silicon-on-sapphire system, the semiconducting properties of silicon on this substrate appear to be inherently limited by a crystallographic mismatch between the rhombohedral sapphire and the cubic silicon, and by the chemical reactivity of the sapphire surface. The cubic spinel lattice is a better match to silicon[15,18-20] than that of sapphire, and the surface is more chemically inert[14] than that of sapphire. Therefore, this material is now under investigation at a number of laboratories.

Spinel within the compositional range desirable for substrate usage[15] ($MgO \cdot 1.5Al_2O_3$ to $MgO \cdot 2.5Al_2O_3$) is not available commercially. Research is in progress at RCA Laboratories on the growth and characterization of single-crystal spinel.[15] Alumina-rich spinel crystals are being grown by the flame fusion process,[15] and the stoichiometric crystals are being grown by flux[16] and Czochralski methods. The flame fusion and Czochralski methods are also being used at Siemens,[17] and the Czochralski material is now being offered commercially by the Royal Radar Establishment,[21,22] and Union Carbide Corporation.[23]

Single-crystal beryllia is of interest as a substrate material[24,25] because of its relatively high thermal conductivity. This property is desirable for dissipation of power in microwave devices. The crystals are difficult to grow, and material of the quality required for substrate usage is not commercially available. Research on the hydrothermal synthesis of single-crystal beryllia is in progress at North American Aviation, Inc.[26] Beryllia is not included in this study because of a lack of availability of the material.

The physical properties of the two materials under study here—sapphire and spinel—are compared to the properties of silicon in Table 1.

Evaluation of the Semiconducting Properties of Silicon on Sapphire and Silicon on Spinel

Mobility as a function of the carrier concentration is the semiconducting property used to initially characterize the quality of the epitaxial

Table 1—Physical Properties of Silicon, Sapphire, and Spinel

	Silicon Si	Sapphire α-Al_2O_3	Spinel* $MgAl_2O_4$
Crystal Structure			
system	face-centered cubic	rhombohedral	face-centered cubic
unit cell dimension, Å	a = 5.4301	a = 4.758 c = 12.991	a = 8.0808
Density			
g/cc	2.33	3.98	3.58
Hardness			
mohs	7	9	8
Melting Process			
mp, °C	1412	2030	2105
congruency	congruent	congruent	congruent
Vaporization Process			
bp, °C	3145	2980	unknown
species	Si-Si_7	Al_2O and O_2	unknown (Mg-rich)
congruency	congruent	congruent	incongruent
Dielectric Constant	11.7 (500c-30Mc)	9.4 ($\perp$ to c) (100c-100Kc)	8.4 (100c-100Kc)
Dissipation Factor			
tan	—	$10^{-3} - 10^{-4}$	$10^{-3} - 10^{-4}$
Refractive Index	3.4975 (at 1.357 μ	1.7707 (at 5461 Å	1.7202 (at 5461 Å)
Optical Transmission	—	80% min. (0.24-6.0 μ, 0.0175 in.)	80% min. (0.31-5.1 μ, 0.0175 in.)
Thermal Conductivity			
cal/cm-sec-°C, at 25°C	0.30	0.065 (60° to c axis)	0.035
Thermal Expansion Coefficient			
1/°C (25-800°C)	3.59	8.40 (60° to c axis)	7.45

* Properties determined using truly stoichiometric spinel single crystals grown by a flux technique developed at RCA Laboratories.

silicon films deposited on sapphire and spinel. With this electrical data, comparisons can be made between silicon on sapphire, silicon on spinel, and bulk silicon.

The mobility is an appropriate property to use as a measurement of film quality because it is particularly sensitive to both crystallographic structure and impurity content of the films. It should be emphasized that the mobility is also a strong function of the dopant type and concentration, the thickness of the film, and the thermal treatment of the film subsequent to deposition. For any meaningful comparison of the effect of various deposition parameters or types of

substrate material on the mobility of the silicon film, the carrier type and concentration, film thickness, and post-deposition treatment must be explicitly stated. During device fabrication, oxide layers are grown on the film surface to serve as diffusion barriers and dielectric components of the device structure. The total of the oxidations employed in fabricating an MOS device is approximately equivalent to a single oxidation of 1 hour in dry oxygen at 1100°C. For this reason, in evaluating the silicon films on sapphire and on spinel, the mobilities are measured as-deposited and also subsequent to 1 hour of oxidation at temperatures between 1100 and 1200°C. During the course of this investigation the oxidation temperature was lowered from 1200 to 1100°C; changes in electrical properties observed during the 1100°C oxidation were similar to those observed at the higher temperature.

Mobility as a function of carrier concentration in bulk silicon has been measured at a number of laboratories in recent years. The values are rather scattered, and no one curve can be taken as a complete representation of the bulk properties. The range of the scatter given

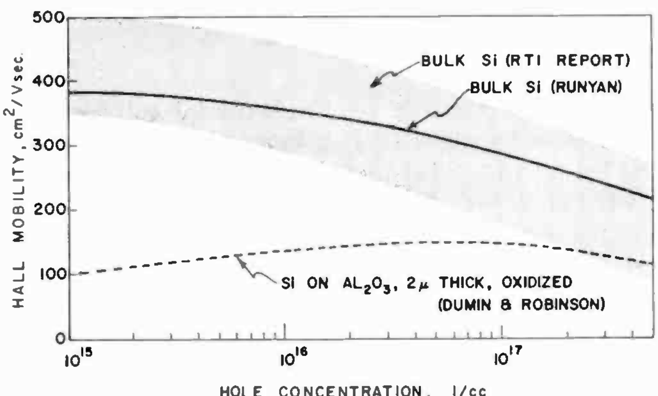

Fig. 1—Mobility as a function of carrier concentration: (a) For 2-micron-thick Si films on sapphire, after oxidation (Ref. [5]), (b) a range reported for bulk Si (Ref. [27]), (c) a curve representing an average of values (Ref. [28]).

in one summary report[27] is presented in Fig. 1. In making quantitative comparisons between the properties of the thin films and the properties of the bulk silicon, it is inconvenient to use a wide range of values. In past reports we have used a bulk silicon curve that has been published as representing a reasonable average of the bulk silicon mobility.[28] This particular curve had been used by some of the early investigators[5] in comparing silicon-on-sapphire properties with bulk properties, and since

it is also our purpose to compare the silicon-on-spinel with silicon-on-sapphire, we have adopted the reference of the earlier authors. Both of these curves are also presented in Fig. 1.

The "percent of bulk mobility" used within this report serves as a meaningful quantitative indication of the progress made in developing the methods to deposit thin silicon films on spinel substrates. The bulk mobility versus carrier concentration curve also provides a correction factor when comparing the properties of films of different carrier concentrations. These values are internally consistent within this paper, but "greater than 100% of bulk" is not meant to imply that the mobilities are greater than any bulk value reported, but they are indeed greater than average and fall within the upper limits of the range shown in Fig. 1.

The device application of most interest for the silicon on insulating substrates has been the complementary-pair MOS device structure employed for computer circuitry. The starting composite for the fabrication of this circuit is a lightly boron doped film between 1.0 and 1.5 microns thick. Therefore, p-type material is used for comparative purposes in this paper.

Epitaxial Growth Apparatus

Silicon is epitaxially grown on single-crystal substrate surfaces by pyrolysis of gaseous silane (SiH_4) in a hydrogen atmosphere at temperatures between 1000 and 1100°C. The substrate is heated by direct contact with an inductively heated susceptor positioned in a water-cooled quartz ampoule. The rf susceptor is a pyrolytic-carbon-coated pure carbon block. The dense pyrolytic coating prevents outgassing of the pressed carbon block. This type of susceptor has been found to be more free of impurities than the silicon-carbide-coated carbon blocks commonly used as rf susceptors.

The gas-metering and -mixing apparatus is schematically presented in Fig. 2. This system is completely He leak-tight. The gases are mixed in glass bulbs before they are passed into the growth chamber so that the doping agents (diborane or arsine) are uniformly distributed throughout the deposit. The doping gas is diluted twice in the system so that flowmeters can be used with sufficiently high gas flows to provide good accuracy. Accurate metering is necessary because, depending on the doping level desired, the dopant source gas of 10 ppm dopant in H_2 is diluted by as much as 500 to 1 before it passes into the growth chamber. An important feature of the gas-control system is the provision to stabilize the gas flows and metering valve settings before the reactants are exposed to the substrate.

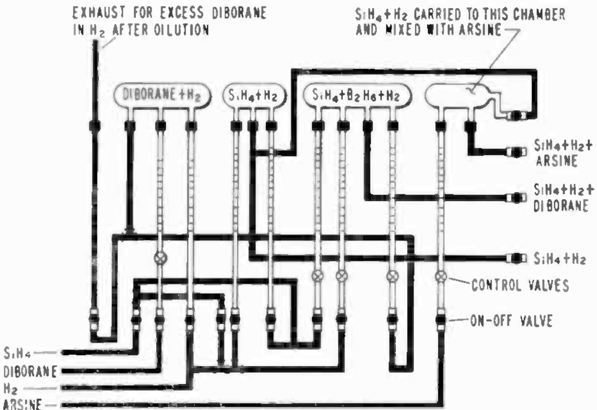

Fig. 2—Schematic of the gas-metering system for the deposition of silicon on insulating substrates.

The rate of growth is observed as the deposit is formed with an infrared detector (Beckman Instruments Model 924-1230) focused on the substrate.[29] Since the substrate is maintained above 1000°C, it acts as an infrared source. A narrow wavelength range is received at the detector by imposing a filter between the source and the detector. As the silicon film grows, interference peaks are observed in the detector output that are a function of the wavelength of the radiation received and the thickness of the film. Thus, at any one instant, the film thickness is known. The experimental setup is schematically presented in Fig. 3.

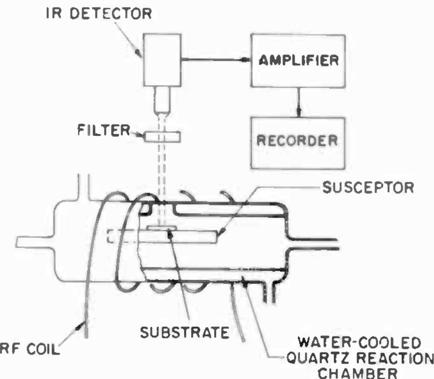

Fig. 3—Schematic of the growth chamber and the deposition rate monitoring system.

Epitaxial Growth of Silicon on Sapphire

Silicon films epitaxially grown on sapphire by the decomposition of silane in a hydrogen atmosphere are typically heavily doped by aluminum from the substrate. This autodoping[5] may be the result of one or both of the following reactions;[30, 31]

$$Al_2O_3 + 2H_2 \rightleftharpoons Al_2O + 2H_2O$$
$$Al_2O_3 + 2Si \rightleftharpoons Al_2O + 2SiO$$

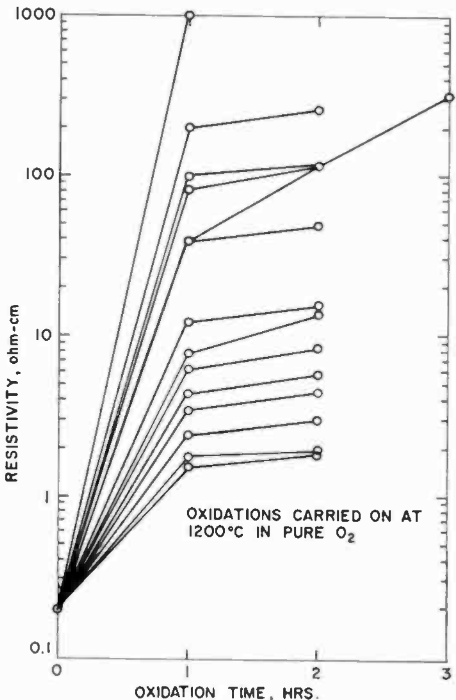

Fig. 4—Change of resistivity as a function of thermal oxidation for 1.7-micron-thick silicon on sapphire deposited at a rate of 0.3 micron/min.

The gaseous Al_2O may be incorporated into the growing silicon film prior to complete coverage of the substrate surface. Due to the presence of the aluminum in the films, the hole concentration of the as-deposited silicon is more a function of the deposition conditions than of the intentionally added boron over a wide range of boron concentrations. The effect is clearly shown in Fig. 4. After exposure to dry oxygen for 1

hour at 1200°C, the film resistivity is a function of the amount of boron added, but the as-deposited resistivity of all the films is ~0.2 ohm-cm. The as-deposited hole concentration is $\sim 3 \times 10^{17}$/cc. The change in the electrical properties on oxidation is attributed to either the removal[7] or electrical de-activation of the aluminum in the silicon films.

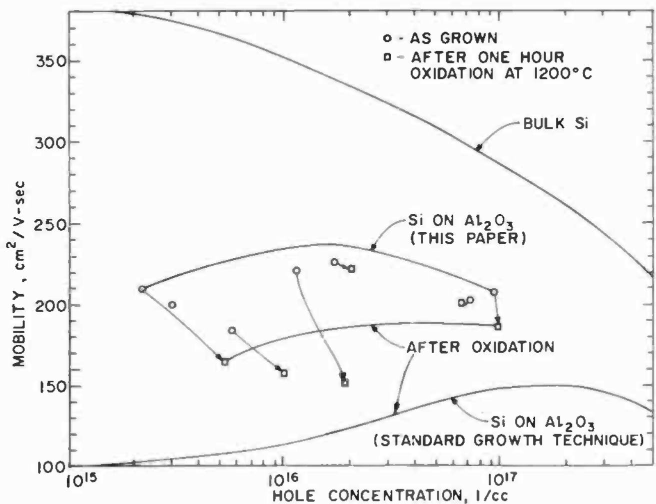

Fig. 5—Mobility versus hole concentration for 1.7-micron-thick silicon on (1$\bar{1}$02) sapphire. The arrows indicate the change in characteristics after thermal oxidation at 1200°C for 1 hour.

In an effort to stabilize the properties of the films during thermal oxidation, deposition procedures were developed to minimize the aluminum contamination by suppression of the reactions shown above. The gaseous lower oxidation state oxide of aluminum (Al_2O) may be formed only if the reaction product can escape. Therefore, the surface of the substrate is covered as rapidly as is possible, consistent with good crystallinity in the deposited film. The deposition temperature is also decreased in order to minimize the contamination reaction. The details of seeking the optimum conditions are discussed in a separate paper.[33] As compared to conditions typically employed in the past, the deposition rate has been increased from ~0.3 to 2.0 microns/min, and the deposition temperature has been decreased from 1125° to 1000°C.

The electrical properties of 1.7 micron-thick silicon deposited using the modified conditions are shown as a function of the carrier concentration and thermal oxidation in Fig. 5. The electrical properties of oxidized silicon films prepared by the "standard" procedure are also

shown. It is in the low-hole-concentration range that the suppression of changes in the film properties on thermal oxidation is most important for device applications. The low-hole-concentration films are also the most influenced by aluminum contamination. It is seen in Fig. 5 that a mobility of 210 cm^2/V-sec in a film with a hole concentration of 2.2×10^{15}/cc is decreased on oxidation to 165 cm^2/V-sec with a corresponding hole concentration of 5.2×10^{15}/cc. By contrast, the hole concentration of a film prepared by the standard method typically would have decreased from $\sim 1 \times 10^{17}$ to 5×10^{15}/cc, with an after-oxidation mobility of $\sim$110 cm^2/V-sec. It is interesting to note that the hole concentrations of the films grown by the modified method increase on oxidation, while the hole concentrations on films grown by the standard method decrease on oxidation. This effect is not completely understood at this time and is the subject of current investigations.

Although resistivity measurements do not provide as much information as Hall measurements, the determination of the resistivity is rapid and nondestructive, and therefore is used to monitor changes in the electrical properties of the silicon thin films. The resistivities of the films prepared in a series similar to that presented in Fig. 5 were measured as a function of thermal oxidation. The results are presented in Fig. 6. It can be seen that the as-deposited resistivities are a function of the amount of boron added, in contrast to the fixed as-deposited film resistivities shown in Fig. 4. On thermal oxidation, relatively large decreases in resistivity are observed for the high-resistivity films as the result of increases in the carrier concentration of the films. For highly doped films, the resistivity increases slightly during oxidation because there is no change in the carrier concentration while there is a small decrease in the mobility. In the 1 to 10 ohm-cm resistivity range, reproducibly small decreases in the resistivity are observed during thermal oxidation. This carrier concentration mobility range is of most interest for the fabrication of MOS devices.

Epitaxial Growth of Silicon on Spinel Substrates

In the effort to stabilize the electrical properties of silicon on spinel during thermal oxidation, the growth rate has proven to be the most critical deposition parameter.[34] An optimum growth temperature of 1100°C was established, holding the other deposition parameters constant. The substrates are annealed at 1150°C for 20 minutes prior to the silicon deposition. This substrate anneal–thermal-etch procedure yields an undamaged single-crystal surface, as shown by low-angle electron diffraction.

Early in the evaluation of spinel as a substrate material, a deposition rate of 0.4 micron/min was employed. This rate is similar to the "standard" rate used for the deposition of silicon on sapphire. The hole mobility as a function of carrier concentration and thermal oxidation of silicon deposited on (111) spinel at 0.4 micron/min is given in Fig. 7. The films are 1.5 micron thick. The substrates are within the composition range between $MgO \cdot 1.5Al_2O_3$ and $MgO \cdot 2.0Al_2O_3$. It is seen that the as-deposited mobilities of the 1.5-micron thick films are similar to bulk mobilities for hole concentrations as low as 5×10^{15}/cc.

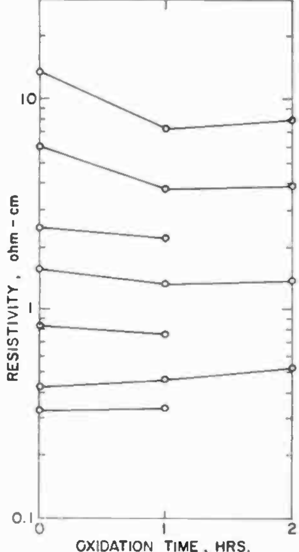

Fig. 6—Change of resistivity as a function of thermal oxidation for 1.7-micron-thick silicon on sapphire deposited at a rate of 2 microns/min.

For hole concentrations greater than $\sim 2 \times 10^{16}$/cc, the mobility is not significantly degraded by thermal oxidation at 1200°C for 1 hour. For hole concentrations less than $\sim 2 \times 10^{16}$/cc, the degradation of the mobility increases sharply with decreasing carrier concentration. Also included in Fig. 7 are the electrical characteristics of films deposited at a rate of 0.8 micron/min. For hole concentrations below $\sim 2 \times 10^{16}$/cc, the change in properties on thermal oxidation is less for the films deposited at the higher rate. At hole concentrations of $\sim 5 \times 10^{15}$/cc, the after-oxidation mobilities of films deposited at 0.4 micron/min are too low for use in device structures, but the after-oxidation mobility of a

film deposited at 0.8 micron/min is ~60% of the bulk value (see Table 2).

The stability of electrical properties during thermal oxidation is considerably improved by increasing the deposition rate to 2.0 microns/min. The mobility as a function of hole concentration and thermal oxidation for 1.5 micron thick films grown at 2.0 microns/min is shown in Fig. 8. Although large changes in the mobilities are observed during thermal oxidation for the low-hole-concentration films, an after-oxidation mobility of 155 cm^2/V-sec was realized in a film with a hole concentration of 1.3×10^{15}/cc. The as-deposited mobility of this film was 235 cm^2/V-sec with a hole concentration of 1.8×10^{15}/cc. It is interesting to note in Fig. 8 that while the as-deposited mobilities do not fall on a smooth curve, the after-oxidation values do. This effect is not understood at this time.

Table 2—Effect of Growth Rate on Stability to Thermal Oxidation for Samples with Similar as-Deposited Properties[34]

Sample Number	Growth Rate microns/min	Thermal Treatment	n_a 1/cc	mobility cm^2/V-sec	% Decrease on Oxidation	% of Bulk
49	0.4	as-deposited	4.5×10^{15}	350		95
		oxidized	1.5×10^{15}	55	86	13
73	0.8	as-deposited	5.6×10^{15}	335		92
		oxidized	4.2×10^{15}	225	33	60
170	2.0	as-deposited	4.9×10^{15}	330		91
		oxidized	4.0×10^{15}	300	9	82

The effect of the growth rate on the stability of properties during thermal oxidation is summarized in Table 2 for films with similar as-deposited properties.

The mobility, and change of mobility on oxidation, of films with hole concentrations less than 5×10^{15}/cc are shown as a function of the higher growth rates in Table 3. The films are very sensitive to deposition parameters in this doping range. For the most part, excellent stabilities were achieved, but the results are somewhat scattered due to the difficultly of controlling both the intentionally and unintentionally added impurities at these carrier-concentration levels. The highest after-oxidation mobility for hole concentrations $\sim 2 \times 10^{15}$/cc was observed in a film deposited at a rate of 5.4 microns/min. There is less scatter in the after-oxidation than in the as-deposited mobilities. With

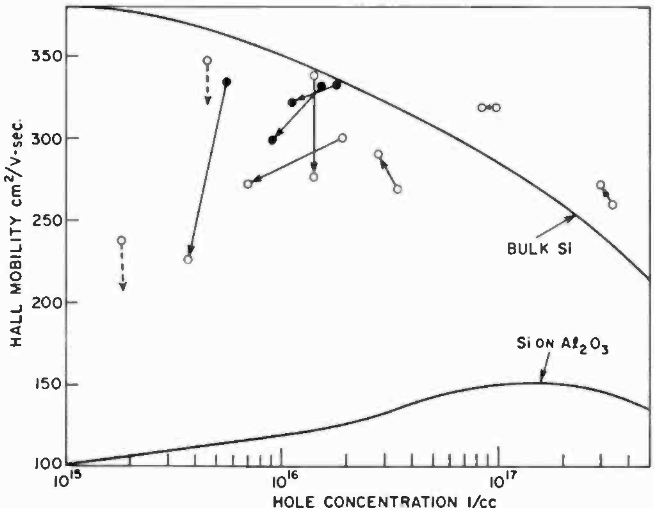

Fig. 7—Mobility versus hole concentration for 1.5-micron-thick silicon films on (111) spinel. The arrows indicate the change in the characteristics after thermal oxidation at 1200°C for 1 hour. The open circles are for material deposited ~0.4 micron/min; the solid circles are for material deposited at ~0.8 micron/min.

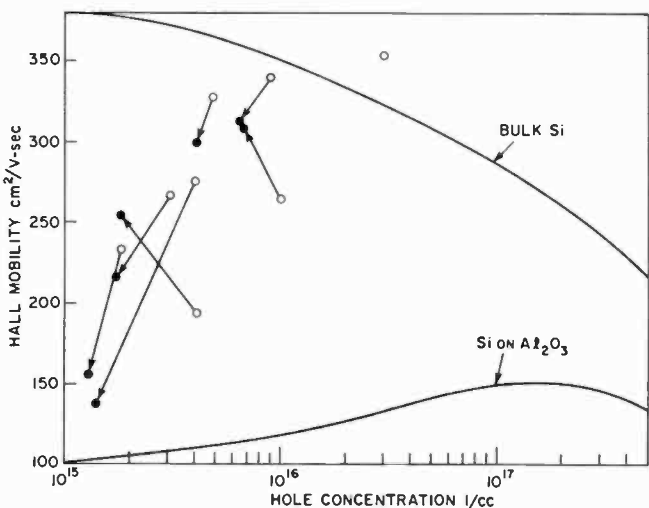

Fig. 8—Mobility versus hole concentration for 1.5-micron-thick silicon films on (111) spinel. The arrows indicate the change in characteristics after thermal oxidation at 1100°C for 1 hour. The films were deposited at a rate of 2.0 micron/min.

the particular gas stream conditions employed at present, the rate cannot be further increased by increasing the silane content of the source gas.

Table 3—Mobility and Stability of Mobility on Oxidation as a Function of Growth Rate at Low Carrier Concentrations

Sample	Deposition Rate microns/min	Thermal Treatment	n_a 1/cc	mobility cm²/V-sec	% Decrease in Mobility on Oxidation	% of Bulk Mobility
286A	4.4	as-deposited	3.4×10^{15}	265		71
oxidized		oxidized	1.8×10^{15}	250	6	66
292A	4.7	as-deposited	1.8×10^{15}	230		61
oxidized		oxidized	1.2×10^{15}	250	8 (incr.)	66
288A	5.1	as-deposited	4.3×10^{15}	330		90
oxidized		oxidized	2.6×10^{15}	260	21	69
289A	5.4	as-deposited	2.4×10^{15}	305		81
oxidized		oxidized	2.0×10^{15}	290	5	77

Thickness: 1.6 to 1.8 μ
Growth temperature: 1100°C
Films oxidized for 1 hr at 1100°C on $MgO \cdot 2.5Al_2O_3$

It is clear from the data presented that although the as-deposited electrical properties are not a strong function of the silicon deposition rate, the after-oxidation properties are highly dependent on the deposition rate, and considerable improvement has been achieved by using growth rates as high as 5.4 micron/min.

The electrical data presented above was taken on silicon films deposited on single-crystal spinel prepared by the flame-fusion process. Films have also been epitaxially deposited on Czochralski crystals grown both at the RCA Laboratories[35] and at the Union Carbide Corporation.[23] The composition of the Czochralski-grown spinel is nominally $MgO \cdot Al_2O_3$. It has been observed that the surface of the Czochralski spinel is more reactive than the surface of the flame-fusion spinel under the conditions employed for the pyrolysis of silane in hydrogen. This surface reactivity is not completely understood at this time, particularly since good growth has been achieved on stoichiometric flux-grown spinel.[36] Different methods must be employed to prepare the surface of the stoichiometric Czochralski crystals than are employed for the preparation of the alumina-rich flame-fusion material. The magnitude of the as-deposited hole mobilities, and the changes in the mobilities on thermal oxidation, in (111) silicon on Czochralski spinel fall between values commonly obtained in (111) silicon on flame-fusion spinel and in (100) silicon on sapphire. For example, at a hole concentration of

4.2×10^{16}/cc, an as-deposited mobility of 250 cm^2/V-sec was realized in a 1.5-micron thick silicon film on Czochralski spinel. This represents ~80% of bulk silicon mobility. On thermal oxidation the hole concentration did not change, and the mobility decreased 10% to a value of 225 cm^2/V-sec. After-oxidation hole mobilities in excess of 300 cm^2/V-sec are typically obtained in equivalent silicon films on flame-fusion spinel.

Summary

Both the magnitude of mobilities and the stability of the electrical properties during thermal oxidation of silicon thin films on sapphire have been considerably improved by adjustment of the deposition conditions. The improvements may be interpreted as resulting from the suppression of the contamination of the silicon by aluminum from the sapphire substrate. In adjusting the deposition conditions, it has been assumed that the aluminum contamination is the result of the formation of gaseous Al_2O and the incorporation of the oxide into the silicon film prior to complete coverage of the substrate surface while gases may still escape. The use of a relatively low deposition temperature inhibits the formation of the oxide, and the use of a relatively high deposition rate leads to the rapid coverage of the surface and blockage of evolution of the gaseous oxide. Employing the modified deposition conditions, an after-oxidation mobility of 165 cm^2/V-sec has been realized at a hole concentration of 5.2×10^{15}/cc. At this hole concentration, a mobility of ~110 cm^2/V-sec is typically obtained using the standard growth conditions. It appears that the properties of silicon on sapphire substrates have been very nearly optimized,[1] and that further improvement will be achieved only by the use of another substrate material.

Magnesium aluminate spinel has been evaluated as a substrate material for silicon epitaxy, primarily because of the relative chemical inertness of the material under the silicon deposition conditions and because of the better match in the crystal structure of the cubic spinel with the cubic silicon. The best electrical properties have been achieved in (111) silicon grown on (111) spinel. Good quality (111) silicon has not been realized on the rhombohedral sapphire substrates. Using rates similar to those employed for the growth of silicon on sapphire, near bulk hole mobilities have been achieved in 1.5-micron thick films for hole concentrations as low as 5×10^{15}/cc. For hole concentrations above $\sim 2 \times 10^{16}$/cc, the electrical properties are very stable during thermal oxidation, and the mobilities are not sensitive to the deposition rate. For hole concentrations less than $\sim 2 \times 10^{16}$/cc, the hole mobilities de-

crease with decreasing hole concentration, and the amount of degradation on thermal oxidation increases with decreasing hole concentration. The magnitude of the degradation on thermal oxidation is critically dependent on the deposition rate. The decrease in the degradation of mobility with an increase in the deposition rate may be attributed to the processes similar to those discussed for the silicon-on-sapphire system. Using a deposition rate of 5.4 micron/min, an after-oxidation hole mobility of 290 cm^2/V-sec was obtained at a hole concentration of 2.0×10^{15}/cc. While the deposition apparatus could be modified to further increase the deposition rate, use of higher rates is impractical because of the short duration of the run when preparing films between 1.0 and 1.5 microns thick.

Acknowledgment

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The Performance of Complementary MOS Transistors on Insulating Substrates

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Abstract—High quality enhancement-type complementary MOS transistors on insulating substrates can be fabricated either by a deep-depletion technology that utilizes a thin high-resistivity p-type silicon film or by a two-stage epitaxial technology that utilizes two lower resistivity p- and n-type films. The deep-depletion technology is characterized by a simple process sequence, low threshold voltages, and stringent control of the doping density in the silicon. The two-stage epitaxial technology is characterized by a more complex process sequence, higher threshold voltages, and greater tolerance to doping variations in the films.

Measurement of the effective inversion layer mobilities of both silicon-on-sapphire and bulk silicon complementary MOS transistors have demonstrated that the effective mobilities of silicon-on-sapphire devices compare very favorably (to better than 70%) with the corresponding mobilities on the commercially available silicon complementary transistors, even though the measured Hall mobilities on the thin films are reduced to $\approx$ 30 percent of bulk values. Theoretical junction breakdown voltages are also achieved with the 1-micron silicon films, indicating reasonably good crystal structure. Based on the above data, it is concluded that either the quality of the bulk silicon at the top surface of the 1-micron silicon-on-sapphire films is very comparable to that of bulk silicon or the effective mobility obtained in enhancement-type MOS transistors is relatively independent of the crystalline quality of the silicon.

Introduction

Substantial increases in the operating speed of silicon Metal-Oxide-Semiconductor (MOS) transistor circuits can be achieved by reducing all the unnecessary internal and stray capacitances in the active devices and interconnections. The most direct way of doing this is to grow a very thin film of single-crystal silicon on a dielectric substrate, fabricate

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the active devices and interconnections, then remove all the unnecessary silicon from the substrate.[1] The active devices are then electrically isolated by the substrate, the capacitance between interconnections and substrate is eliminated, and large-area horizontal diffused junctions are replaced by small-area vertical diffused junctions.[2] These techniques have been used to fabricate integrated circuits using both p- and n-channel MOS transistors (PMOST and NMOST). Research at RCA Laboratories has resulted in the fabrication of complementary MOS (CMOS) integrated circuits on thin films of single-crystal silicon grown epitaxially on single-crystal sapphire. These integrated circuits are composed entirely of NMOS and PMOS transistors and exhibit internal delays of less than one nanosecond per gate and power dissipation of less than ten microwatts per bit.[3-5]

The use of 1-micron thick silicon films grown on insulating substrates allows fabrication of enhancement-mode CMOS transistor pairs by either of two technologies. Deep-Depletion[6] technology can be used to fabricate both types of complementary devices simultaneously on a thin high-resistivity p-type film. These devices have very low threshold voltages; however, precise control of the doping in the thin film is required. The second technology provides both p- and n-type thin silicon films by means of two epitaxial growth steps.[7,8] The complementary devices operate as do conventional enhancement-mode CMOS transistors fabricated on bulk-silicon substrates. Lower resistivity material may be used in the two-stage process; therefore, the doping of the material is easier to control.

The material requirements for each of these two technologies are examined here and the performance of the resulting devices is analyzed. The effect of the poorer crystalline structure of the heteroepitaxial silicon films on the effective inversion-layer mobility is demonstrated by comparison with similar devices fabricated on bulk silicon.

Deep-Depletion Complementary MOS Transistors

The fabrication and operation of deep-depletion MOS transistors have been analyzed in detail[9] and only a brief description is given here. Both the NMOS and PMOS transistors are fabricated in a thin p-type silicon film, typically 1-micron thick, having a resistivity greater than 10 ohm-cm. The fabrication sequence and completed devices are shown in Figs. 1 and 2. The NMOS enhancement-mode transistors operates in the usual manner,[10] i.e., application of a positive gate-source voltage $V_{GS} \geqq V_{TN}$ inverts the surface of the p-type silicon and establishes a conducting channel between n+ source-and-drain regions. The gate

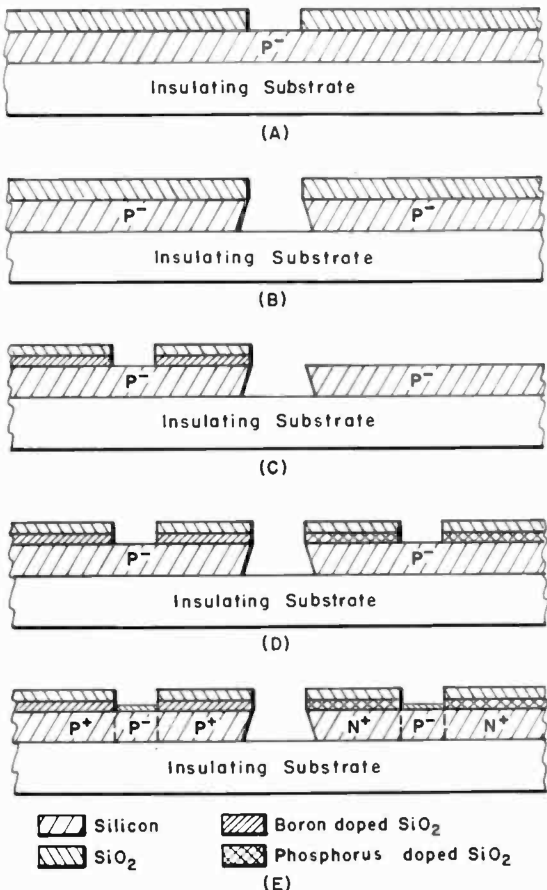


Fig. 1—Deep-depletion CMOS process.

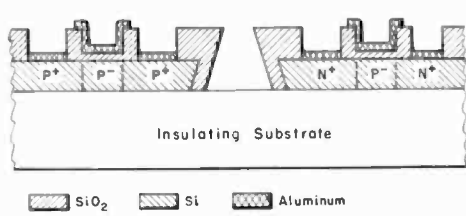


Fig. 2—Completed deep-depletion CMOS structure.

electrode (aluminum) to p-type silicon work-function potential difference, V_{GSC}, is of such a polarity (negative) to deplete the surface of the p-type film, creating a surface space-charge region composed entirely of immobile ionized acceptor atoms. Since the PMOST is a junctionless structure, it is necessary that the width of this space-charge region be at least equal to the film thickness, T_S, so that negligible source–drain current will flow when $V_{GS} = 0$. Application of small negative V_{GS} removes the gate-electrode-induced depletion region and accumulates holes at the surface. The PMOST, therefore, operates similarly to a conventional enhancement-mode PMOST with a very low threshold voltage. The requirement that the zero gate-bias width of the surface space-charge region extend through the film determines the upper limits on the thickness and doping of the thin p-type silicon film.

In order to fully realize the low power dissipation inherent in CMOS circuits, it is necessary that

V_{TP} = threshold voltage of PMOST < 0

V_{TN} = threshold voltage of NMOST > 0

For simultaneous fabrication of enhancement NMOST and PMOST, the following relations between device parameters must be satisfied:

$$V_{TN} = V_{OX}(\text{inv}) + V_{SC}(\text{inv}) + V_{GSC} - V_{SS}(\text{inv}) > 0 \qquad [1]$$

and

$$T_S < X_D\,(V_{GSC}) \leq X_{DM}, \qquad [2]$$

where[11]

$$X_D\,(V_{GSC}) = \frac{T_{OX}\,\epsilon_S}{\epsilon_{OX}} \left\{ \sqrt{1 - \left[\frac{2\,\epsilon_{OX}^2}{eN_A\,\epsilon_S\,T_{OX}^2}\right] V_{GSC} + \left[\frac{2\,\epsilon_{OX}}{eN_A\,\epsilon_S T_{OX}}\right] Q_{SS}} - 1 \right\} \qquad [3]$$

= thickness of p-silicon depleted by gate-electrode–silicon work-function difference, V_{GSC}.

$X_{DM}\,(N_A) = \sqrt{2\,\epsilon_S |\,(2\phi_{FP})\,|/eN_A}$ = maximum possible value of X_D,[12] [4]

$V_{OX}(\text{inv}) = (T_{OX}/\epsilon_{OX})\,\sqrt{2e\epsilon_S N\,|\phi_S(\text{inv})|}$ = voltage drop across the gate oxide at the onset of inversion or $\phi_S = \phi_S(\text{inv})$ (V_{OX} is positive for p-type material and negative for n-type material),

$V_{SC}(\text{inv}) = \phi_S(\text{inv})$ = voltage drop across the Si surface space-charge region at the onset of inversion (ϕ_S is positive for p-type material and negative for n-type material),

$V_{GSO}(N_A) = \Phi_G - \Phi_{SC}/e =$ electrostatic potential difference between gate electrode and channel silicon due to the work-function difference between the two materials,

$V_{SS}(\text{inv}) = eT_{OX} N_{SS}(\text{inv})/\epsilon_{OX} =$ equivalent applied gate voltage due to effective oxide and $Si\text{-}SiO_2$ interface charge density, N_{SS} (this includes both mobile and immobile oxide charge; if "fast" surface states are present, N_{SS} is a function of ϕ_S and must be evaluated at $\phi_S = \phi_S(\text{inv})$; it is assumed that V_{SS} is positive),

$\phi_S =$ electrostatic surface potential of channel silicon referred to the intrinsic Fermi level of the channel silicon,

$N_A =$ magnitude of acceptor concentration in the channel silicon,

$\epsilon_{OX} =$ permittivity of the gate oxide,

$\epsilon_S =$ permittivity of the channel silicon,

$T_{OX} =$ thickness of the gate oxide,

$e =$ magnitude of the electronic charge.

Two assumptions are made in calculating Eq. [1]:

1. $\phi_S(\text{inv}) = 2\phi_F$ where ϕ_F is the Fermi potential of the channel silicon. This is equivalent to the assumption that the surface is inverted when the minority-carrier density at the surface equals the impurity-atom density in the channel silicon. Several authors[13] define $\phi_S(\text{inv}) = \phi_F$, which is the point at which the surface becomes intrinsic. Theoretically, the source and drain are no longer separated by back-to-back p-n junctions when the surface becomes intrinsic, and surface leakage current can flow between source and drain. The definition $\phi_S(\text{inv}) = 2\phi_F$ is adequate to define the point at which significant (1 μA) surface current flows, especially when drain-current saturation is taken into account; however, in order to minimize the standby power of the CMOS circuit, both Eqs. [1] and [2] must be satisfied by large margins to allow for normal process tolerances.
2. $N_{SS} =$ constant independent of ϕ_S is the "fast" interface state density can be neglected. The resulting C-V curve of the transsistor is displaced parallel to the ideal ($N_{SS} = 0$, $V_{GSO} = 0$) C-V curve. In practice, careful preparation of the silicon surface before thermal oxidation reduces the "fast" interface state density to $< 5 \times 10^{10} \text{cm}^{-2}$.[14] If N_{SS} is a function of ϕ, then it is assumed for the purpose of these calculations that $N_{SS} = N_{SS}(2\phi_F)$.

The gate-electrode–silicon electrostatic potential difference, V_{GSC}, was calculated using the relationship:

$$V_{GSC} = \frac{\Phi_G - \Phi_{SC}}{e} = \left(\pm \frac{kT}{e} \ln \frac{N_G}{n_i} \left(- \right) \pm \frac{kT}{e} \ln \frac{N}{n_i} \right). \qquad [5]$$

The work function of the gate electrode material, Φ_G, is expressed in terms of an equivalent doping density of bulk silicon, N_G. To determine N_G for gate electrode materials other than silicon, it is necessary to have accurate values for Φ_G and χ_{SC}. Several values of the electron affinity, χ of silicon have been reported[15] ranging between 4.05 eV $\leq \chi \leq$ 4.30 eV. For these calculations, an average value of $\chi = 4.20$ eV $\pm$ 0.1 eV was chosen. Other constants used were

$$\Phi_G = 4.20 \text{ eV (aluminum)}$$

$$N_G = 2.0 \times 10^{19} \text{cm}^{-3} \text{ (aluminum)}$$

$$n_i = 1.45 \times 10^{10} \text{cm}^{-3}$$

$$\epsilon_{OX} = 3.85\, \epsilon_O$$

$$\epsilon_{SI} = 11.7\, \epsilon_O$$

$$T_{OX} = 1400 \text{ Å}$$

$$\epsilon_O = 8.85 \times 10^{-14} \text{ F} - \text{cm}^{-1}$$

It should be noted that the accuracy of the threshold-voltage calculations is limited to $\pm$0.1 V due to variations in the reported values of χ. Eq. [2] states that in order to obtain an enhancement deep-depletion PMOST, the depletion-region width due to the gate-electrode–silicon work-function difference (V_{GSC}) must be > the thickness of the silicon film T_S. This width must also be $\leq$ the maximum obtainable depletion region width (X_{DM}), which is a function of the carrier concentration N_A.

Figs. 3 and 4 show graphs of V_{TN}, X_D, and X_{DM} as a function of N_A as calculated from Eqs. [1], [3], and [4], respectively. Both $N_{SS} = 0$ and $N_{SS} = 5 \times 10^{10}$cm^{-2}, which is a representative value for a clean thermal oxide on (100) silicon, are considered. Inspection of Figs. 3 and 4, in view of Eqs. [1] and [2], leads to the following conclusions.

1. For the ideal case of $N_{SS} = 0$, if $T_S = 1$ micron, the usable region of N_A is limited to $N_A = 3\text{-}6 \times 10^{14}$cm^{-3} to simultaneously satisfy Eqs. [1] and [2]. This imposes a rather severe materials

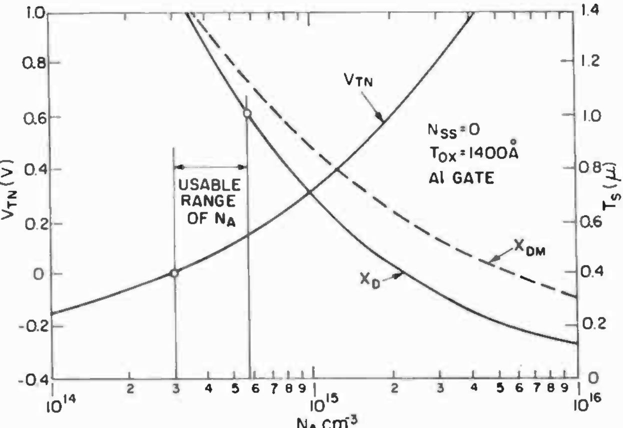


Fig. 3—Selection of film thickness and doping for deep-depletion process ($Nss = 0$).

requirement in that the reproducible epitaxial growth of a uniformly doped 20 to 50 ohm-cm 1-micron p-type silicon film is difficult even on a generic silicon substrate. The heteroepitaxial growth of the film on an insulating substrate produces additional problems, such as autodoping of the film by constituents of the substrate[16] and precipitation of impurities during thermal oxidation,[17] both of which can result in nonuniform doping of the thin silicon film. Impurity redistribution at the surface must also be taken into account.[18]

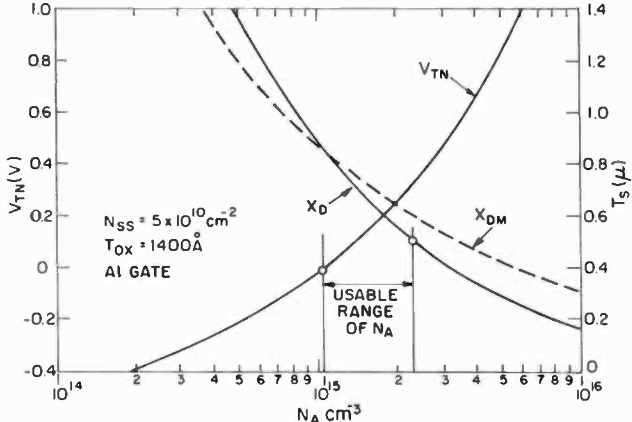
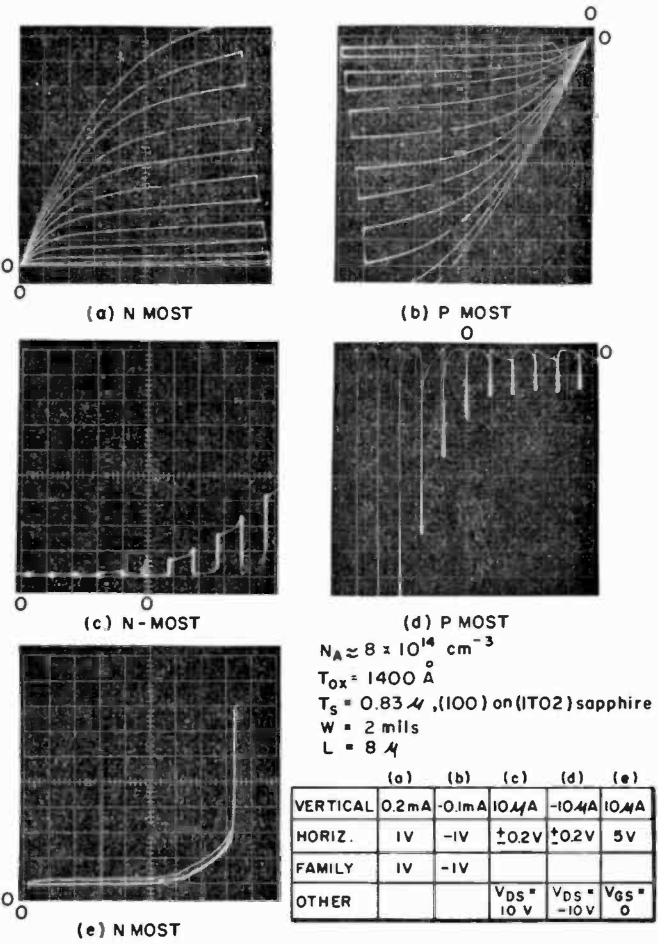


Fig. 4—Selection of film thickness and doping for deep-depletion process ($Nss = 5 \times 10^{10} cm^{-2}$).

The difficulties in obtaining uniformly-doped high-resistivity *p*-type films on sapphire are well illustrated by the deep-depletion-technology complementary MOS transistor pair shown in Fig. 5. The doping density of the film increases as the silicon–sapphire interface is approached, as illustrated by Fig. 5c and 5e. The value of $V_{TN} \approx 0.0$ V is consistent with $N_A \approx 1 \times 10^{15}\text{cm}^{-3}$. However, the source-drain breakdown voltage in Fig. 5e indicates $N_A \approx 1\text{-}2 \times 10^{16}\text{cm}^{-3}$ near the silicon–sapphire interface. Refer-



	(a)	(b)	(c)	(d)	(e)
VERTICAL	0.2 mA	-0.1 mA	10 μA	-10 μA	10 μA
HORIZ.	1V	-1V	±0.2V	±0.2V	5V
FAMILY	1V	-1V			
OTHER			V_{DS} = 10 V	V_{DS} = -10 V	V_{GS} = 0

Fig. 5—Illustration of the effects of non-uniform doping in the deep-depletion structure.

ring to Fig. 4, it is seen that if $T_S = 0.83$ micron and $N_A \approx 1 \times 10^{15} cm^{-3}$ throughout the film, the PMOST should have zero drain–source current at $V_{GS} = 0$. Fig. 5d shows that I_{DS} cannot be reduced below -15 A, which further confirms the increase in N_A at the interface.

2. In the more realistic case of $N_{SS} = 5 \times 10^{10} cm^{-2}$, for a reasonably wide usable range of $N_A \approx$ 1-2 $\times 10^{15} cm^{-3}$, T_S must be reduced to 0.5 micron. At present, the 0.5 micron p-type films that are grown on sapphire have surface (field-effect) mobilities that are severely reduced due to the poor crystal structure of the thin film, resulting in poor device performance. If, however, good-quality 0.5 micron silicon films can be obtained, the deep-depletion technology is very attractive, since the use of the thinner films allows heavier doping of the p-type film, shorter diffusion times, and smaller crossover steps to the sapphire substrate.

3. The threshold voltages in the deep-depletion technology are very low,

$$0 < V_{TN} < 0.5 \ V$$

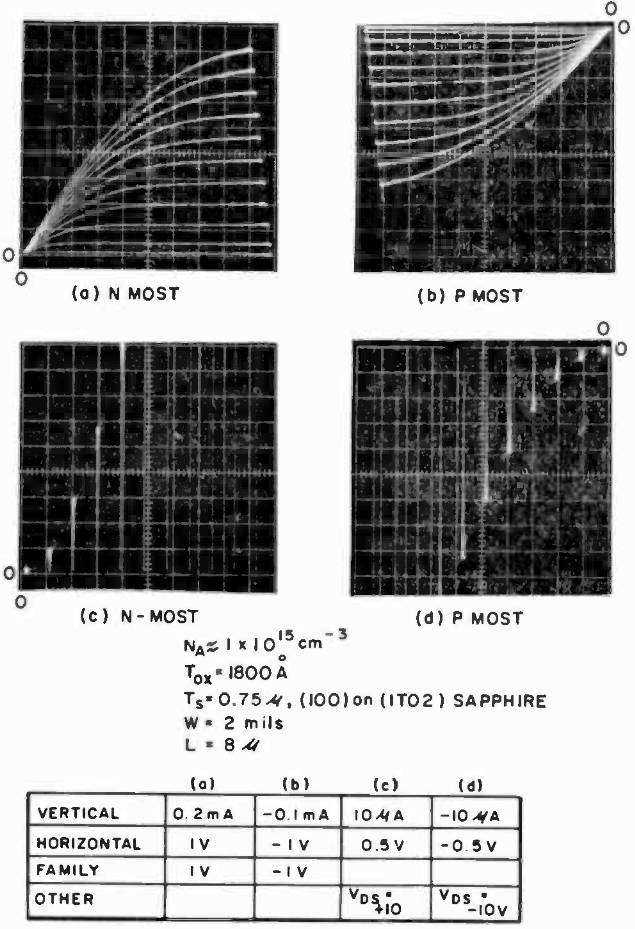
$$0 > V_{TP} > -0.5 \ V$$

if the values of N_A are confined to the usable range for that particular value of N_{SS}, T_{OX}, and T_S. The actual value of V_{TP} depends on the value of source-drain current used to define the threshold voltage, since finite source-drain current begins to flow when $X_D < T_S$.

The discussion above illustrates the precise control of film thickness and doping necessary to realize the advantages of very high speed and simple process technology inherent in the deep-depletion technology. Typical characteristics of complementary MOS transistors fabricated by the deep-depletion technology in a 0.75 micron film of 30 ohm-cm p-type <100> silicon grown on $(1\bar{1}02)$ sapphire are shown in Fig. 6.

Two-Stage Epitaxial Complementary MOS Transistor

To avoid the severe materials requirements encountered in using 1-micron films of high-resistivity ($N_A = 3\text{-}6 \times 10^{14} cm^{-3}$) p-type silicon, a process has been developed that utilizes two heteroepitaxial growth steps on sapphire to provide opposite conductivity-type channel silicon-on-sapphire for conventional enhancement-type CMOS transistors. This



	(a)	(b)	(c)	(d)
VERTICAL	0.2 mA	-0.1 mA	10 μA	-10 μA
HORIZONTAL	1 V	-1 V	0.5 V	-0.5 V
FAMILY	1 V	-1 V		
OTHER			V_{DS} = +10	V_{DS} = -10 V

Fig. 6—Deep-depletion CMOS transistors on sapphire.

more complicated method allows the use of lower-resistivity p-type silicon, since the PMOST no longer operates in the deep-depletion mode. The PMOST is now a p^+-n-p^+ structure and the NMOST remains an n^+-p-n^+ structure as in the deep-depletion technology. The process sequence and finished device structures are shown in Figs. 7 and 8. In the two-stage CMOS process, the p-type silicon is doped at a level of $N_A \approx$ 2-4 $\times 10^{16}$cm^{-3} and the n-type silicon is doped at a level of $N_D \approx$ 2-6 $\times 10^{15}$cm^{-3}. Both films are approximately 1-micron thick.

A disadvantage in using the lower-resistivity silicon is seen from the threshold voltage curves shown in Figs. 9 and 10. These curves are

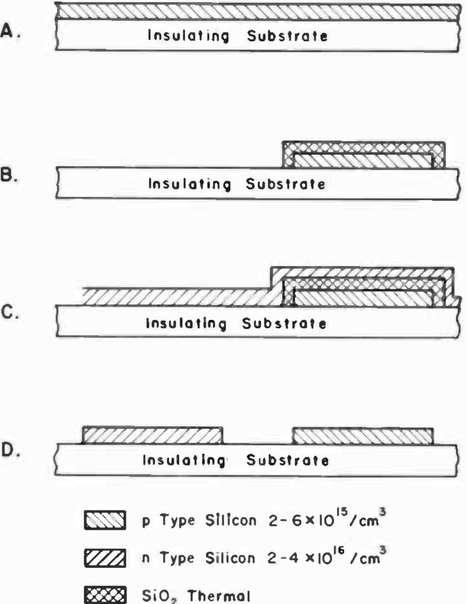


Fig. 7—Two-stage epitaxial process substrate preparation.

computer calculations in Eq. [1] for various material and geometry parameters. The assumptions used in the calculations were discussed above. Inspection of Figs. 9 and 10 shows that the doping densities stated above will produce the following threshold voltages:

$$-1.75 \text{ V} \geq V_{TP} \geq -2.75 \text{ V}$$

$$1.75 \text{ V} \leq V_{TN} \leq 2.25 \text{ V}$$

These values assume that $T_{OX} = 1000$ Å of thermal SiO_2, $N_{SS} = 5 \times 10^{10}$

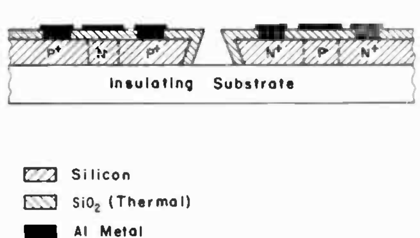


Fig. 8—Completed two stage epitaxial CMOS structure.

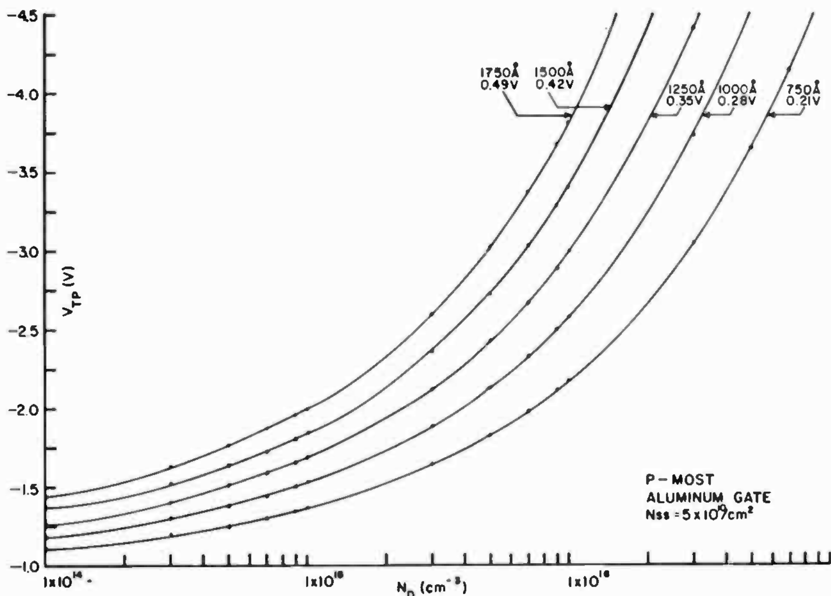


Fig. 9—Theoretical threshold voltages for two-stage epitaxial-process PMOST ($V_{SS} = eN_{SS}/C_{ox}$).

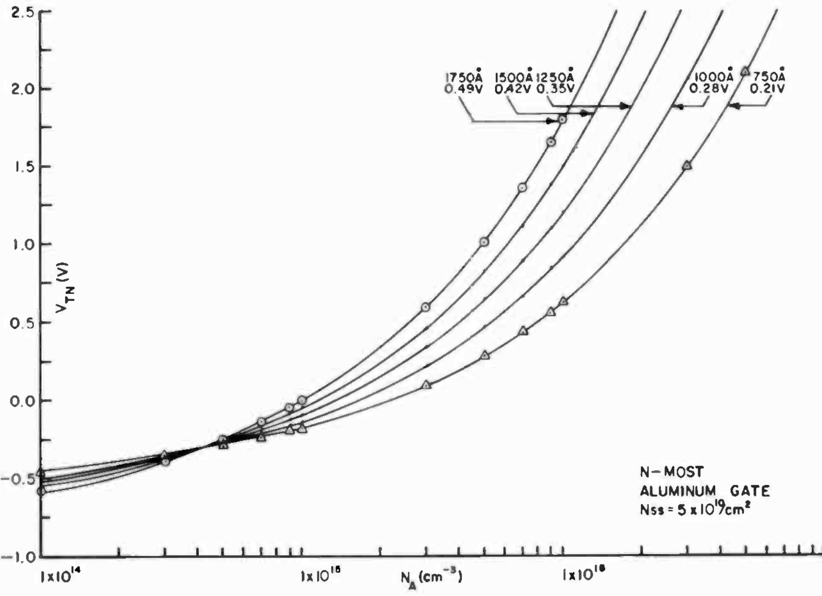


Fig. 10—Theoretical threshold voltages for two-stage epitaxial-process NMOST ($V_{SS} = eN_{SS}/C_{ox}$).

cm^{-2}, and the gate electrodes are aluminium. These threshold voltages should be compared with those for the deep-depletion technology ($0 \leq |V_T| \leq 0.5$ V). The effect of the magnitudes of V_{TP} and V_{TN} on the operating speed of CMOS circuits is illustrated by the expression for the pair delay T_D of a CMOS inverter,[19]

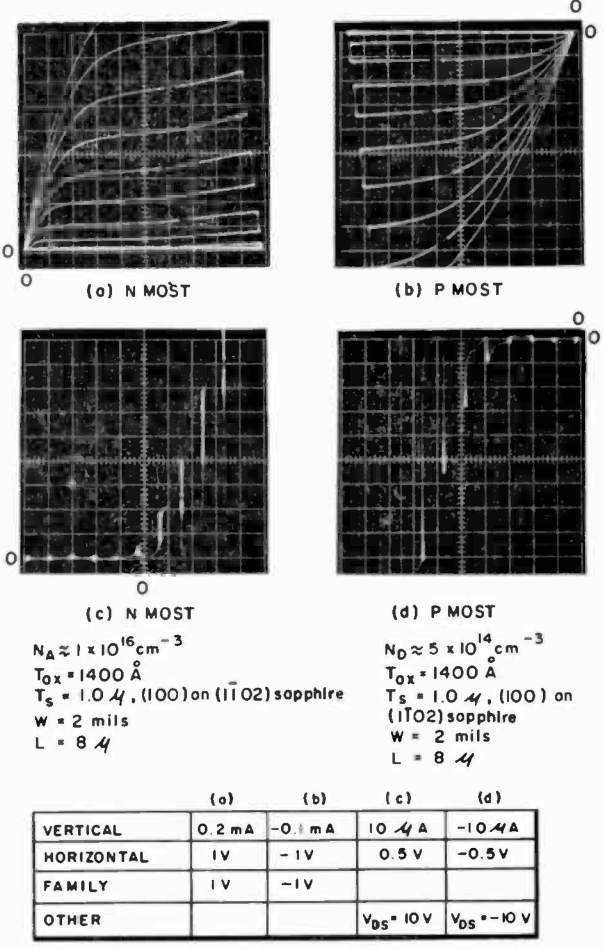
$$T_D \approx K \left\{ \frac{1}{(V_O - V_{TN})^2} + \frac{1}{\beta\,(V_O - |V_{TP}|)^2} \right\} V_O, \qquad [6]$$

where V_O is the supply voltage and K and β are other device parameters. It can be shown from Eq. [6] that if $V_O = 10$ V, increasing $V_{TN} = -V_{TP}$ from 0.5 to 2.0 V increases the pair delay T_D by 40%, a significant increase. Circuits fabricated using the two-stage process have operated at speeds of 50MHz ($V_O = 10$ V) and 95 MHz ($V_O = 20$ V) even with the high values of V_T, illustrating the inherent speed of silicon-on-sapphire integrated circuits.[5]

The above discussion illustrates that the use of lower resistivity silicon films relaxes the doping control required in the film, but at the expense of a more complicated technology and higher threshold voltages. The performance of typical complementary MOS transistor pairs fabricated in (100) p- and n-type silicon grown on $(1\bar{1}02)$ sapphire using the two-stage epitaxial technology is shown in Fig. 11. The doping densities of the silicon films are $1 \times 10^{16} cm^{-3}$ (p-type) and $5 \times 10^{14} cm^{-3}$ (n-type). The threshold voltages are $V_{TN} \approx 2.0$ V and $V_{TP} \approx -1.5$ V, as shown in Figs. 11c and 11d. Figs. 12a and 12b demonstrate the sharp source–drain breakdown voltages obtained from the extermely small area ($5 \times 10^{-7} cm^2$) vertical-diffused junctions, indicating that the silicon is of reasonably good quality throughout the thickness of the film. The experimental source–drain breakdown voltages agree extremely well with the calculated breakdown voltages of abrupt one-sided junctions with a 1-micron radius of curvature.[20]

Effects of Crystal Perfection on Device Performance

The most potentially serious problems in fabricating integrated circuits on thin heteroepitaxial films are due to the degradation of the physical and electrical properties of the silicon films. There exists a crystallographic mismatch and a mismatch of thermal coefficient of expansion between silicon and both single-crystal sapphire and single-crystal spinel, the two materials most often used for the insulating substrate.[21] A review of these problems is given in a related paper.[22]



	(a)	(b)	(c)	(d)
VERTICAL	0.2 mA	-0.1 mA	10 μA	-10 μA
HORIZONTAL	1 V	- 1 V	0.5 V	-0.5 V
FAMILY	1 V	-1 V		
OTHER			V_{DS} = 10 V	V_{DS} = -10 V

Fig. 11—Two-stage epitaxial process CMOS transistors on sapphire.

It suffices here to say that the thin silicon films have a very large defect density, especially near the silicon–substrate interface. This defect density results in reduced bulk mobility and increased susceptibility of the silicon to contaminants that may be electrically active as donors or acceptors.[23] The problems caused by electrically-active defects and external contaminants can be reduced by limiting the exposure of the silicon film to high temperatures (> 500°C) during device processing.[8] Since the resistivity of bulk silicon is too low for use as an insulating substrate, the reduced crystal perfection of thin silicon films grown on

materials having a different lattice structure than silicon is virtually unavoidable.

Fortunately, the enhancement-type MOS transistor is ideally suited for use in circuits fabricated on less-than-ideal silicon, because the performance of the transistor depends primarily on the electrical properties of a very thin ($<<1000$ Å) inversion layer of minority carriers located at the surface of the film. Since the bulk mobilities of

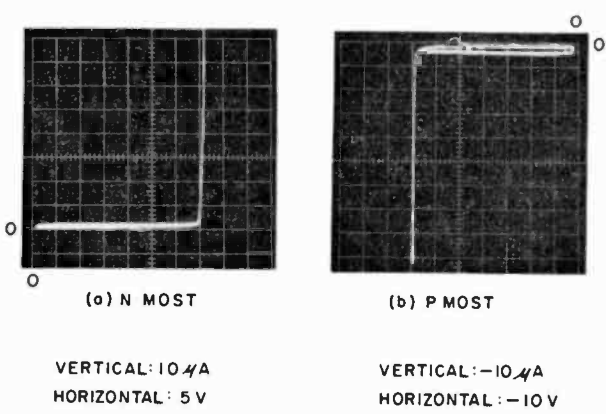


Fig. 12—Source-drain breakdown characteristics of two-stage epitaxial CMOS transistors.

single-crystal silicon films on sapphire improve with increasing film thickness, higher bulk mobilities are observed at the surface.[23] In addition, the mobility of the minority carriers in the surface inversion layer is strongly dependent on the quality of the SiO_2-Si interface at the surface of the silicon. Previous work has demonstrated that, by the use of the same techniques used on bulk silicon devices,[14] low interface state densities ($<5\times10^{10}$cm^{-2} on (100) silicon) can be produced with thermal silicon dioxide grown on (100) silicon.[6] Finally, it is shown below that the effective mobility of the mobile charge in the inversion layer is not significantly reduced by a drastic decrease in the bulk mobility characteristic of the thin silicon film. A brief review of the effective mobility concept is followed by the results of mobility measurements on both silicon-on-sapphire complementary MOS transistors and commercially available bulk silicon complementary MOS transistors.

Measurement of Effective Mobility

The effective mobility μ_{eff} of the mobile minority carriers in the

inversion layer at the surface of a silicon film is defined as the weighted average of the minority-carrier mobility over the finite thickness of the inversion layer, i.e., [24]

$$\mu_{eff} = \frac{\int_0^{X_i} n(x)\,\mu(n)\,dx}{\int_0^{X_i} n(x)\,dx}, \qquad [7]$$

where

$n(x)$ = spatially-dependent minority carrier concentration in the inversion layer (cm^{-3}).

$\mu(n)$ = density-dependent minority carrier mobility (cm^2/V-sec).

X_i = thickness of the inversion layer (cm).

Assuming the inversion layer exists, X_i is determined by the distance from the oxidized surface to the interior point in the silicon where the material becomes electrically intrinsic, i.e., $\phi(X_i) = \phi_F$. Therefore, the surface potential, ϕ_S, must be greater than ϕ_F for any inversion to exist. As discussed above, the onset of strong inversion is usually defined as $\phi_S = 2\phi_F$.

The effective mobility can be determined by the field-effect conductance method[24] in which the drain conductance at very small drain voltages g_{DSO} is measured as a function of the gate-to-source voltage V_{GS} of the MOS transistor. The value of μ_{eff} is determined from

$$g_{DSO} = \frac{\mu_{eff}\,Q_{inv}\,W}{L} \qquad [8]$$

where

Q_{inv} = minority carrier charge per unit area in the inversion layer (coul/cm^2)

W = width of channel region (*cm*)

L = length of channel region (*cm*)

It is assumed that μ_{eff} is a constant independent of the lateral electric field along the channel. The effective mobility does vary as a function of the normal gate electrode field. Since very small drain voltages V_{DS} are used (several kT/e), the channel is uniformly inverted from source-to-drain for any $|V_{GS}| > |V_T|$ and the transistor essentially becomes a gate-controlled resistor.

There are two methods of determining Q_{inv}. For large gate voltages, the following approximation can be made:

$$Q_{inv} \approx \frac{\epsilon_{OX}}{T_{OX}} (V_{GS} - V_T) \,;\; V_{GS} >> V_T \qquad [9]$$

The approximation above[24] is accurate when the channel is so strongly inverted that the capacitance of the inversion layer dominates the geometrical capacitance of the channel oxide,

$$\frac{C_{GS}}{C_{OX}} \approx 1 \qquad [10]$$

where:

C_{GS} = series capacitance between gate electrode and source electrode (pF).

$C_{OX} = \epsilon_{OX} WL/T_{OX}$ = geometrical channel oxide capacitance (pF).

The value of V_T used in calculating Q_{inv} from Eq. [9] is obtained by extrapolating the g_{DSO} versus V_{GS} curve to $g_{SDO} = 0$. The intercept is the operational value of V_T for use in Eq. [9]. The extrapolation must be made from the linear part of the g_{DSO} versus V_{GS} curve since Eq. [9] implies a linear relationship between Q_{inv} and V_{GS}. It has been shown [24] that the use of Eq. [9] with V_T determined as above underestimates Q_{inv} for surface potentials in the range $2\phi_F \leq \phi_S < 2\phi_F + (5kT/e)$ so that μ_{eff} is overestimated for values of $V_{GS} - V_T < 1.5$ V for the usual values of T_{OX}, N_A, and N_D. Therefore, Eq. [9] should only be used for calculating μ_{eff} when $V_{GS} >> V_T$. Fig. 13 illustrates the C_{GS} and g_{DSO} versus V_{GS} curves for an NMOS transistor similar to that of Figs. 11a and 11c. Note the following features:

1. V_{TN} (= 1.5 V) for calculations using Eq. [9] is determined by extrapolating from the linear part of the g_{DSO} curve to $g_{DSO} = 0$.

2. The value of C_{GS} corresponding to the extrapolated $V_{TN} = 1.5$ V is $0.95C_{OX}$, indicating Eq. [10] is satisfied.
3. The value of C_{GS}/C_{OX} corresponding to $\phi_S = 2\phi_F$ is 0.70. The value of V_{GS} for $\phi_S = 2\phi_F$ is 1.2 V which is the true value of V_{TN} $(2\phi_F)$, corresponding to the onset of heavy inversion.
4. Only the inversion part of the C_{GS} versus V_{GS} curve can be measured for these transistors because of the extremely small (less than 0.1 C_{OX}) source-junction capacitance in series with

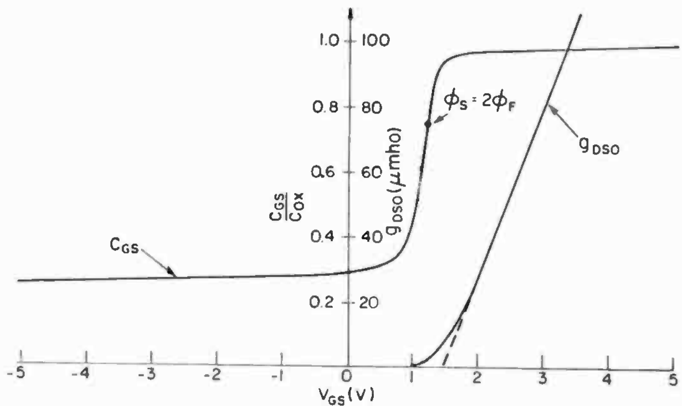


Fig. 13—Experimental gate capacitance and low-field drain conductance of two-stage epitaxial NMOST.

the series combination of the oxide and space-charge capacitances. Only during inversion is the source junction capacitance shorted out. In the depletion and accumulation regions, C_{GS} essentially measures the overlap capacitance between the gate electrode and source. This feature of the thin film MOS transistors is important in digital circuits because the capacitive loading of "OFF" transistors becomes negligible, thus increasing the available fanout. The extremely small capacitance of the drain junction greatly improves the high-frequency response of the MOS transistor in linear small-signal applications.

The inversion layer charge Q_{inv} may be determined accurately for all values of V_{GS} by rigorously solving Posson's equation to determine the minority-carrier surface charge as a function of the surface potential ϕ_S and the total charge in the semiconductor. This relation has been tabulated.[12,24] The remaining step is to relate ϕ_S to the applied V_{GS}. The most convenient method is to use the tabulated ideal curves of

C_{GS} versus V_{GS}, available in the literature.[25] Extreme care must be taken to accurately determine the flatband voltage shift ΔV_{FB} that must be added to the voltage axis of the ideal C_{GS} curve,

$$\Delta V_{FB} = V_{GSO} - V_{SS}. \qquad [11]$$

The flatband voltage shift is more conveniently determined by comparing the experimental C_{GS} versus V_{GS} curve for the transistor with the ideal curve. Normally, ΔV_{FB} is negative, so the ideal C_{GS} curve should be shifted to the left. The difficulty in any method for determining Q_{inv} is that Q_{inv} is of the order of 10^{10} to 10^{12} charges/cm^2. Unless great care is taken during the oxidation steps, the fast surface-state density can be of the same order of magnitude as Q_{inv}. These fast states can trap the mobile charges in the inversion layer and lead to overestimation of Q_{inv} in the mobility calculations.

Measured values of g_{DSO} have been used to determine μ_{eff} and the results of the measurements are presented below.

Experimental Results

Fig. 14 presents the μ_{eff} of electrons in the inversion layers of the following devices calculated using eq. [9]:

a. An NMOS transistor similar to that of Figs. 11a and 11c fabricated with the two-stage epitaxial process on (100) silicon.

b. The NMOST transistor shown in Figs. 5a, 5c, and 5e fabricated with the deep-depletion process on (100) silicon.

c. A commercial NMOS transistor comprising part of an RCA CD4007D complementary symmetry inverter. The substrate is (100) silicon with $N_A \approx 2.8 \times 10^{16}$cm^{-3} and $T_{OX} = 1200$ Å.[26]

Fig. 15 presents the results of calculating μ_{eff} for holes using Eq. [9] for the following PMOS transistors:

a. A PMOS transistor similar to that of Figs. 11b and 11d fabricated with the two-stage epitaxial process on (100) silicon.

b. The PMOS transistor shown in Figs. 6b and 6d fabricated with the deep-depletion process on (100) silicon.

c. A commercial PMOS transistor comprising part of a RCA CD4007D complementary symmetry inverter. The substrate is (100) bulk silicon with $N_D \approx 2.8 \times 10^{15}$cm^{-3} and $T_{OX} = 1200$ Å.[28]

The data of Figs. 14 and 15 suggests the following conclusions.

1. The effective mobility of electrons in the inversion layer of the

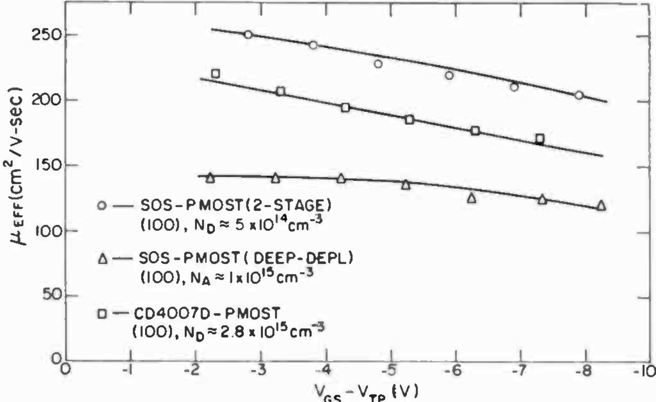


Fig. 14—Effective electron mobility for CMOS transistors on sapphire.

silicon-on-sapphire NMOS transistors is at least 70% of the corresponding mobility of a similar bulk-silicon NMOS transistor and increases to at least 80% when the high-resistivity silicon of the deep-depletion technology is used.

2. The effective mobility of the inversion-layer electrons and holes tends to decrease slightly with increasing gate electric field in agreement with previous work.[24] The effective inversion-layer hole mobility appears to be more dependent on the normal electric field than the effective electron mobility.

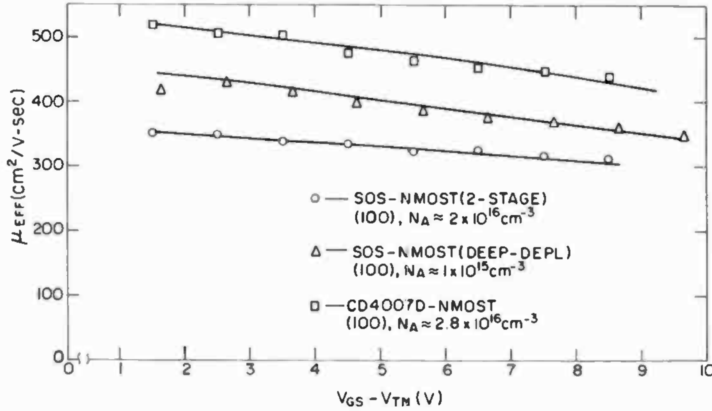


Fig. 15—Effective hole mobility for CMOS transistors on sapphire.

3. The effective inversion-layer hole mobility of the two-stage epitaxial silicon-on-sapphire PMOST is actually greater than the corresponding mobility of the corresponding bulk silicon PMOST.
4. The effective hole mobility of the deep-depletion PMOST is considerably reduced over that of the two-stage epitaxial-process PMOST. It is felt that this is due to the very low bulk hole mobility, and the fact that the current is carried by an accumulation layer of majority holes, not by an inversion layer of minority holes as in the two-stage epitaxial PMOST.
5. The effective mobility of both holes and electrons in the inversion layers on (100) silicon appears to increase with increasing resistivity of the silicon.

The small, if any, degradation of μ_{eff} on the silicon-on-sapphire devices compared to similar devices fabricated in bulk silicon is even more significant for several reasons:

1. The average Hall mobility of the p-type silicon ($N_A \approx 1 \times 10^{15}$ cm^{-3}) used in the deep-depletion technology (see Figs. 5 and 14) is $\approx$100 cm^2/volt-sec or $\approx$25% of the corresponding Hall mobility for bulk silicon. The silicon-on-sapphire Hall samples are thermally oxidized (one hour in dry O_2 at 1100°C) to simulate the amount of thermal oxidation in the device processing preparatory to measuring the mobility.
2. The average Hall mobilities of the p-type ($N_A \approx 2 \times 10^{16}$cm^{-3}) and n-type ($N_D \approx 5 \times 10^{14}$cm^{-3}) silicon films used in the two-stage epitaxial transistors of Fig. 11 are typically (after oxidation)

   p-type: 120 cm^2/V-sec or 36% bulk mobility

   n-type: 550 cm^2/V-sec or 30% bulk mobility

It should be mentioned that the measured Hall mobilities of the silicon-on-sapphire films are weighted averages over the thickness of the film, so that a low Hall mobility does not necessarily indicate that the silicon film has a uniformly poor structure. However, the very low values obtained suggest that as a whole, the 1-micron silicon-on-sapphire films have a very large defect density even at the top surface of the film.

The accuracy of the calculated effective mobilities presented in Figs. 13, 14, and 15 is entirely dependent on the degree of confidence in the values of T_{OX}, W, and L. The channel length, L, is the most

difficult parameter to accurately determine, particularly on silicon-on-sapphire devices. Considering the degree of confidence in L, the values of μ_{eff} presented above are thought to be accurate to $\pm 15\%$ for all the devices measured. Series source-and-drain resistance was not a factor due to the low channel conductances of the measured devices. The values of g_{DSO} were determined on a Tektronix curve-tracer with values of V_{DS} between 25 and 50 mV.

Conclusions

High quality enhancement-type complementary MOS transistors on insulating substrates can be fabricated either by a deep-depletion technology that utilizes a thin high-resistivity p-type silicon film or a two-stage epitaxial technology that utilizes two lower resistivity p- and n-type films. The deep-depletion technology is characterized by a simple process sequence, low threshold voltages, and stringent control of the doping density in the silicon. The two-stage epitaxial technology is characterized by a more complex process sequence, higher threshold voltages, and greater tolerance to doping variations in the films. High-speed integrated circuits have been successfully fabricated using both technologies and have demonstrated the superior performance inherent in the concept of complementary MOS transistor circuits on an insulating substrate.

Measurement of the effective inversion-layer mobilities of both silicon-on-sapphire and bulk silicon complementary MOS transistors have demonstrated that the drastically reduced bulk Hall mobilities of present 1-micron silicon-on-sapphire films is not a good indication of either the crystalline quality of the top surface of the films or of the expected effective inversion layer mobility in enhancement-type devices. The effective mobilities of silicon-on-sapphire devices compare very favorably (to better than 70%) with the corresponding mobilities on the commercial bulk-silicon complementary transistors, even though the measured Hall mobilities on the thin films are reduced to $\approx$30% of bulk values. Theoretical junction-breakdown voltages are also achieved with the 1-micron silicon films, indicating reasonably good crystal structure. Based on the above data, either the quality of the bulk silicon at the top surface of the 1-micron silicon-on-sapphire films is very comparable to that of bulk silicon or the effective mobility obtained in enhancement-type MOS transistors is relatively independent of the crystalline quality of the silicon. A more detailed examination of these relationships is in progress.

Acknowledgment

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Monitoring Silicon Tetrachloride Concentration in Hydrogen Carrier Gas*

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Abstract—A thermal conductivity detector has been constructed to monitor the concentration of silicon tetrachloride vapor in hydrogen carrier gas as used in epitaxial reactors. Significant variations in vapor concentrations with time have been detected for a constant carrier gas flow through a typical evaporator. The causes of these variations have been determined and methods of controlling them devised. The apparatus may be used to determine concentrations of other gas and vapor mixtures.

Introduction

This paper, describes an inexpensive, simple, reliable apparatus that permits monitoring and control of the concentration of silicon tetrachloride in hydrogen carrier gas as used in epitaxial reactors. The concentrations of interest are on the order of 0.1 mole percent $SiCl_4$; it is desired to measure fluctuations of one-tenth this amount or $\pm 0.01\%$.

The benefits to be gained from such a system for epitaxial reactors include

(1) higher yield of satisfactory devices because of better uniformity of epitaxial layers,

(2) better reproducibility of device characteristics because deposits are more uniform,

(3) ability to grow well-controlled multiple layers without interrupting processing,

(4) ability to make unusual doping profiles for developing new devices.

These benefits assume that both pure and doped $SiCl_4$ vapor concentrations can be monitored, so that control of doping is possible.

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The approach followed in developing a suitable system was to adapt an existing detector used in gas chromatography, specifically the thermal conductivity detector. Thermal conductivity detectors are inexpensive, simple, and nondestructive. They are adequately sensitive, and their performance is well-known.[1] Furthermore, detectors of this type have been successfully used in chromatography to detect $SiCl_4$ concentrations.[2]

Problems in using detectors of this type for $SiCl_4$ monitoring arise from the corrosive nature of the $SiCl_4$ and the high gas-flow rates used in epitaxy. Chromatography systems for gases of this type must be constructed entirely of corrosion-resistant materials.[3] High gas-flow rates tend to introduce noise into thermal conductivity detectors.[4,5]

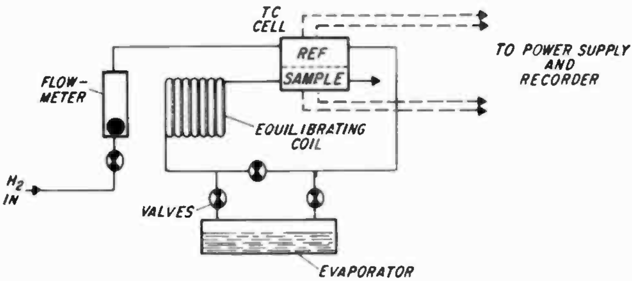

Fig. 1—System diagram.

Apparatus

Fig. 1 is a diagram of the monitoring system. It shows the flowmeter, the thermal conductivity cell, the control valves, the evaporator, and the equilibrating coil. Hydrogen gas enters through a needle valve and the flowmeter is set to the desired flow rate, typically 3 liters/minute. The hydrogen passes through the reference side of the thermal conductivity cell to the control valves. These valves permit the hydrogen to flow through the evaporator or to bypass it. The evaporator contains liquid silicon tetrachloride at room temperature. A reservoir (not shown) maintains a constant liquid level in the evaporator.

The gas, either pure hydrogen or hydrogen plus silicon tetrachloride, next passes through the equilibrating coil. The coil is a length of about 10 feet of the same ¼-inch Teflon tubing used throughout the system. The coil allows the cool vapor from the evaporator to reach room temperature before entering the detector. This was found to be necessary in preliminary tests of the apparatus, because temperature changes

resulting from the cool vapor were masking the thermal conductivity changes in the gas.

From the equilibrating coil, the gas passes through the sample side of the detector and out of the system. Both sample and reference chambers contain identical thermistors. The thermistors are bead-in-glass probes (VECO 52A6) selected to withstand the corrosive gas. They are connected to the power supply and recorder by electrical leads as indicated.

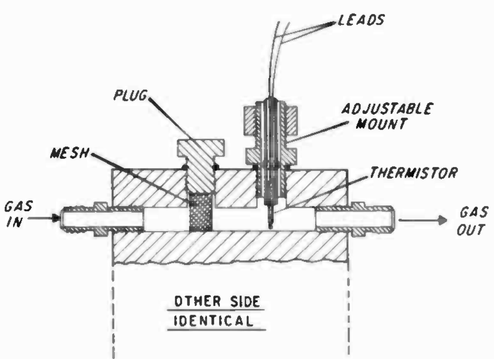

Fig. 2—Thermal conductivity cell.

Fig. 2 is a sectional view of half of the thermal conductivity cell. It is made from a block of Monel so as to resist corrosion. The block is bored through to form a gas passage, with standard fittings at either end. Two holes are bored perpendicular to the main passage to form tee's with it. One tee contains the thermistor in an adjustable mount. The lead end of the thermistor probe is epoxied inside a short length of ¼-inch glass tubing. The tubing fits inside an adjustable mount, made from a standard Teflon fitting by boring out the internal lip. This allows the thermistor bead to be positioned directly in the gas stream, or withdrawn into the tee. Withdrawing the thermistor from the direct gas stream corresponds to the diffusion mode of operation for chromatography detectors. It increases signal and reduces flow sensitivity, at the expense of increasing the response time.[6]

The second tee, upstream of the thermistor, contains a cylindrical screen of 40-mesh stainless steel, held in place by a Teflon plug. This screen is shaped to completely fill the passage, so that the entire gas flow passes through the mesh. It was added to smooth out gas flow within the detector after initial tests showed that disturbed flow was causing electrical noise on the signal output at high gas-flow rates.

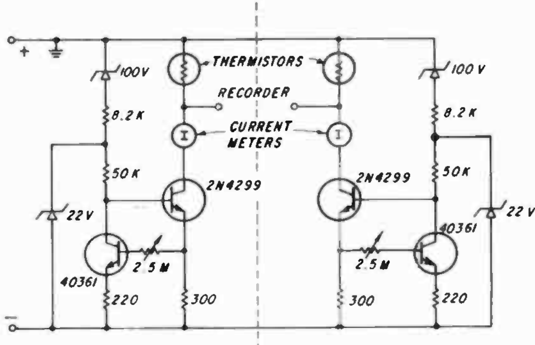

Fig. 3—Thermistor power supply.

The mesh smooths this flow and reduces the noise. In later tests, positioning the thermistor probe out of the gas stream, as previously described, also reduced the effects of flow fluctuations.

Fig. 3 is a schematic of the transitorized constant current supply. It consists of two matched circuits, each of which provides a current source for one thermistor. Normally, currents are adjusted to give 5 mA through each thermistor. The recorder then measures the difference in voltage drop across the two thermistors as a function of time. This changes with the thermal conductivity of the gas mixture as described below.

Fig. 4 is a photograph of the thermal conductivity cell and power-supply chassis. The sample and reference chambers are side by side, with gas inlet and outlet connections on opposite sides of the block. The thermistor tubes are seen protruding from the adjustable mounts, just downstream from the plain Teflon plugs. Several turns of the equilibrating coil appear under the lower thermal shielding. The power supply is in front of the chassis, with the current meters and controls

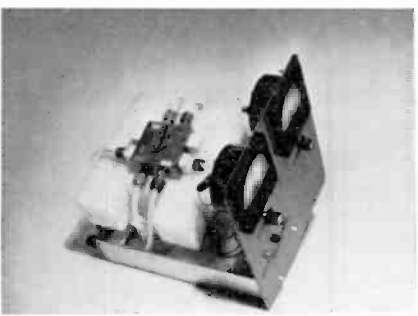

Fig. 4—Thermal conductivity cell and power supply.

visable on the front panel. The recorder connections are on the lower right portion of the front panel; the gas lines and power cord are connected at the rear of the chassis.

Fig. 5 is a simplified diagram of a silicon tetrachloride evaporator typical of those used for epitaxy. It is a glass cylinder approximately 10 inches long by 3½ inches in diameter. Carrier gas enters through a ball check valve and blows directly downwards on the liquid. The gas exits through another check valve at the far end. An upper reservoir (not drawn to scale) keeps the evaporator half full of liquid silicon tetrachloride.

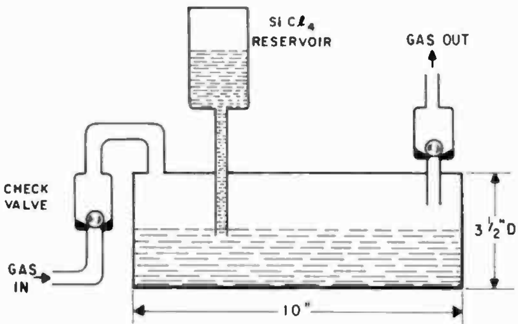

Fig. 5—Evaporator.

Operating Procedure

Initially the carrier gas flows with the evaporator valves closed and the by-pass valve open. This passes pure hydrogen through both sample and reference chambers, giving a recorder base line corresponding to a zero concentration of $SiCl_4$. Next, the bypass valve is closed and the evaporator valves opened, so that the entire hydrogen flow from the reference chamber passes through the evaporator before entering the sample chamber. The reference thermistor remains in a hydrogen flow, while the sample thermistor is exposed to hydrogen plus some amount of silicon tetrachloride. Since the thermal conductivity of the $H_2 + SiCl_4$ is lower than that of pure H_2, the thermistor temperature increases until it reaches a new equilibrium point. The change in temperature causes a change in electrical resistance that is sensed and recorded in a conventional bridge circuit.[7]

Calibration

The detector was calibrated by relating the electrical signal at the recorder to the concentration of silicon tetrachloride in the sample cell.

To establish this concentration, an infrared spectrophotometer (Perkin-Elmer Type 137) was used. The gas cell of the spectrophotometer was connected in series with the output of the reference side of thermal conductivity detector, so that the gas mixture passed through the spectrophotometer cell. The infrared absorption of the silicon tetrachloride vapor was measured and used to compute the vapor concentration in the cell by standard methods. Since the thermal conductivity system is much more sensitive than the spectrophotometer, the calibration covers only the upper ranges of gas concentration. However, sufficient data points were taken to establish a good linear response.

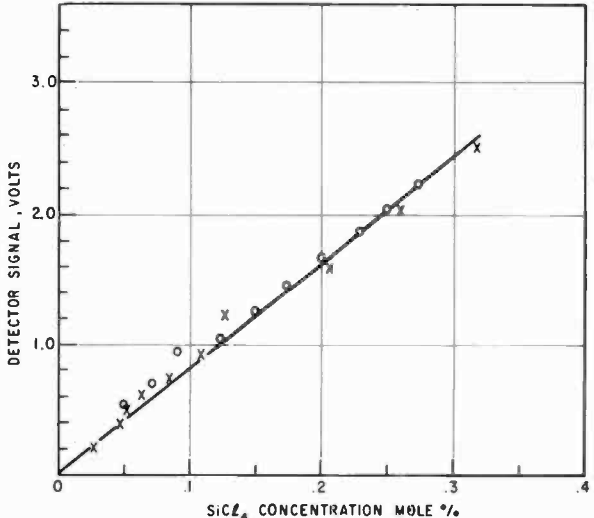

Fig. 6—Detector calibration.

Different gas concentrations were obtained by immersing the evaporator in a cooling bath and varying its temperature. A mixture of isopropanol and dry ice was used to slowly lower the temperature of the evaporator. When temperature equilibrium was reached, the infrared absorption and the detector signal were noted. The temperature was then lowered to obtain another concentration.

This technique provided a wide range of vapor concentrations at a constant hydrogen flow rate. Hence, signals due to flow changes are avoided.

Fig. 6 is a typical detector calibration curve. It shows the detector signal in volts as a function of silicon tetrachloride concentration in mole percent. The detector signal is the voltage at the recorder

terminals; the vapor concentration was computed as described from the IR absorption measurement.

This particular curve is for a specific pair of thermistors, located at a specific position using the adjustable mounts, and at one specific operating current and gas flow rate. The X's are data points taken while cooling the evaporator; the open circles are points taken while returning to room temperature.

This calibration is for the concentration range up to 0.3 mole percent; other tests covered concentrations up to 1% and down to 0.004%. The minimum concentration, 0.004%, was achieved by diluting a concentration level (from the cooled evaporator) that was measurable with the IR with an additional flow of pure hydrogen, thus lowering the concentration by a known factor. The signal-to-noise ratio at 0.004 mole percent was approximately 5, which puts the lower detection limit of the present system near 0.001%. This is well below the target sensitivity of 0.01%.

The stability and reproducibility of detector measurements were tested, since there have been reports of thermistor instability in hydrogen ambients. Two calibration curves were made as described above, separated by an interval of two months during which the detector was in normal use. No change in detector characteristics was found; the curves were identical within the range of experimental error.

Thermistor pairs have been used for hundreds of hours in hydrogen ambient over the past year without any detectable instability or change in characteristics. The bead-in-glass probes used are protected by relatively thick glass coatings; thermistors previously reported as being unstable in hydrogen have been of the microbead type with extremely thin glass coatings. No such instability was found in our system.

Results

The calibrated detector was used to monitor the output of the evaporator under conditions approximating those of a typical epitaxial deposition. Fig. 7 shows the silicon tetrachloride concentration as a function of time. It was made as previously described, by first bypassing the evaporator to obtain a zero-concentration base line, then opening the evaporator valves and closing the bypass valve. The curve, starting from zero-time, represents the concentration in the evaporator output as it is supplied to the epitaxial system.

Two significant changes in concentration are observed. The first is an initial concentration peak that occurs during the first 50 to 100

seconds of flow. The second change is a slow, continuing decrease in concentration that continues until flow is terminated. In the test indicated, the initial peak reached 0.65 mole percent, while the decrease was from 0.35 to 0.29 percent.

The initial peak results from a sweep-out of the saturated vapor that fills the free volume of the evaporator before carrier gas enters. The size and sharpness of this peak depend on many variables, such as carrier-gas flow rate, reservoir temperature, and the time interval during which quiescent conditions have prevailed (i.e., the time interval since carrier gas last flowed through the evaporator). In worst cases, the initial peak may be more than 20 times the ultimate steady-state value.

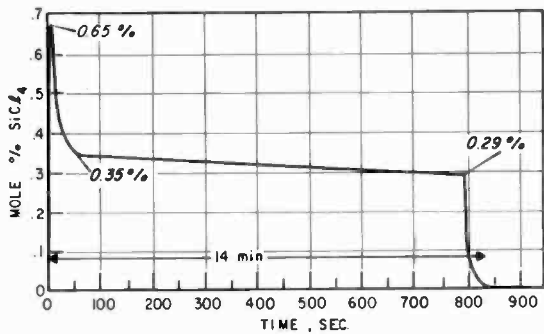

Fig. 7—Concentration change with time.

Since nucleation of the epitaxial deposit occurs when the first $SiCl_4$ enters the epitaxial reactor, and since nucleation is critical, uncontrolled peak concentrations of this nature should be avoided. An adequate method is to discard the initial vapor flow rather than passing it through the reactor.

The gradual decrease in concentration with time results from evaporative cooling of the liquid in the evaporator. It continues as long as evaporation continues. A monotonic decrease has been observed during tests lasting more than two hours, during which the concentration dropped to nearly half of its initial steady-state value.

Temperature measurements were made in the evaporator to relate evaporator-liquid temperature changes to gas concentration changes. Thermocouple probes were inserted through fittings in a special demountable end-plate that replaced one end of the reservoir. The probes were submerged to a known depth in the fluid, and moved to different positions, both along the axis and off the axis of the reservoir.

The liquid temperature was found to decrease continually during an evaporation. The temperature is nonuniform, being coldest at the surface, and decreasing along the surface as the hydrogen inlet is approached. In one case, a temperature difference of 4°C was measured over a distance of 1 cm along the surface near the inlet.

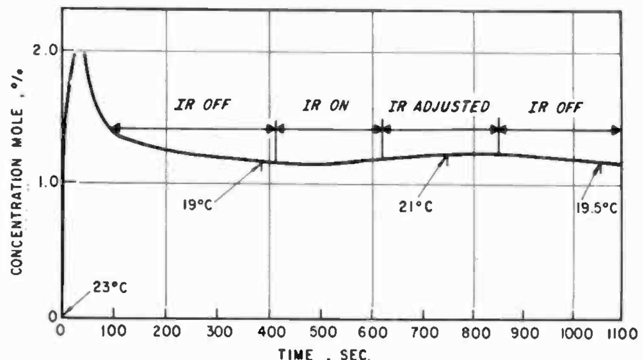

Fig. 8—Concentration change with temperature.

Fig. 8 relates temperature data to concentration changes. It shows a recording of concentration versus time, as in the previous figure. The liquid temperature at the surface under the gas inlet is noted at several points during the recording. Also, a 250 W infrared lamp was used to heat the evaporator during the periods indicated.

The temperature of the liquid $SiCl_4$ is 23° C when evaporation begins. After 380 seconds, the temperature has dropped to 19° C. The heat lamp is then turned on, and after a lag, the concentration begins to increase. The lamp current is adjusted to give a constant concentration, which occurs at 21° C. Finally, the lamp is turned off, allowing the temperature and the concentration to decrease. The temperature is 19.5° C near the end of the test.

While this figure shows the concentration and temperature changes over a relatively short time, similar changes continue as long as evaporation continues. The change in concentration is not linear with temperature, since the vapor pressure is not a linear function of temperature. Conversion of the temperature data to vapor pressure (using standard curves) shows a linear relation between the observed concentration and the vapor pressure.

The heat lamp provides a simple means of concentration control. By adjusting the lamp current, it was possible to maintain a uniform

concentration at any desired level, without further adjustment. A proportional controller of the type normally used for temperature control is now being tested as a feedback system. If this is successful, it will be possible to maintain a given concentration by setting the feedback control, and then change rapidly to a new, constant concentration by suitably adjusting the controls.

The monitoring system was further tested using an operating epitaxial reactor. Monitoring the $SiCl_4$ concentration during normal operation revealed the same uncontrolled changes as previously described: an initial concentration peak, and a continuing decrease during evaporation. The IR lamp and control were successfully used to maintain a uniform concentration and to change this concentration to another uniform level when desired.

Other Applications

The system was used with several organic vapors during testing (e.g., acetone, isopropanol). It was also used to monitor the concentration of stannic chloride ($SnCl_4$) from a bubbler used for depositing tin oxide coatings. The bubbler showed an initial concentration peak similar to that of an evaporator. The steady concentration decrease was not as steep as in an evaporator and would be trivial for the relatively short time spans used in this deposition.

The monitoring system is potentially useful in any application where gas concentration must be precisely known and controlled. Performance in any specific situation depends on the concentration level, the flow rates, and the thermal conductivities of the particular gases involved, as well as their corrosive properties and stability.

Conclusions

The gas-concentration monitoring system, using a thermal conductivity cell, provides an inexpensive, simple, nondestructive means for monitoring the concentration of $SiCl_4$ used in epitaxial reactors. The sensitivity, stability, and reproducibility of the system has been tested on a working epitaxial reactor, and found to be satisfactory.

The silicon tetrachloride vapor concentration from a typical evaporator shows large, uncontrolled variations for a constant carrier gas flow. These variations are an initial peak, resulting from a sweep-out of saturated vapor in the evaporator, and a steady decrease resulting from evaporative cooling of the liquid. For precise work, the initial peak should be diverted from the epitaxial reactor and discarded. The

steady decrease can be prevented by supplying heat to the evaporator in an amount that balances the heat losses. A constant vapor concentration has been maintained in this manner, using a heat lamp under manual control. An automatic system with proportional feedback to a heater would be a simple extension of this principle.

The concentration monitoring system has potential application to the precise control of any gas mixture in which the thermal conductivity of the gas components is sufficiently different.

Acknowledgments

The construction of the constant current supplies for the thermistor bridge was carried out by J. Groppe, who also made many of the measurements in this work.

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An Inexpensive Integrating Photoresist Exposure Control System

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Abstract—An inexpensive apparatus has been constructed that provides precise control of photoresist exposure, a step widely employed in electronic device manufacturing. A sensor monitors the total incident light flux and, through appropriate circuitry, terminates the exposure when a predetermined value is reached. Digital logic circuits and integrated circuit counters are employed. The apparatus offers significant advantages in cost, simplicity, and ruggedness over commercially available apparatus.

Introduction

This paper describes a novel apparatus for controlling the exposure of photoresist layers. A photodiode in a relaxation oscillator circuit responds to incident light to provide a series of pulses whose repetition rate is proportional to light intensity. These pulses are counted by a counter circuit that shuts off the light source when a predetermined exposure has been reached.

Several commercial systems are available for exposure control. However, all of those tested were found to have certain drawbacks: cost, complexity, low sensitivity, limited range, instability, and lack of ruggedness. The system described in this report provides adequate control at a reasonable cost.

Description

1. General

Incident light may be integrated by using a photosensitive resistor to control the charging current into a capacitor. This technique is used, for example, in one type of electronic shutter now available on cameras.[1]

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It is useful for exposures up to about one minute, but becomes impractical for much longer periods.

The light-sensitive oscillator described in this report uses a photosensitive resistor-capacitor network as the timing circuit in a relaxation oscillator. A small, near-linear portion of the capacitor charging curve is used so that the oscillator frequency will be linearly dependent on the light intensity incident on the photosensitive element. This oscillator output is differentiated to give a pulsed output. In effect, this portion of the circuit is an inexpensive analog to a digital converter. The circuit responds continually to any fluctuations in light output by changing interpulse spacing. The pulses are counted via commercially available integrated-circuit digital counters until a preset number is reached. Digital logic circuitry then terminates the exposure.

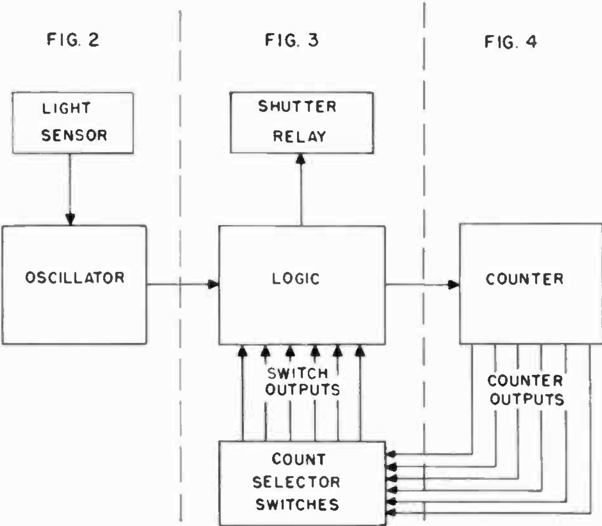

Fig. 1—System diagram.

Fig. 1 is an overall diagram of the apparatus, showing the light-sensitive oscillator controlled by the photosensitive element, the logic circuitry that gates the oscillator pulses into the counter, the "presetable" pulse counter that receives the oscillator output pulses through the logic gates and activates the logic through count-select switches, and the associated power supplies and indicators.

2. Oscillator and Logic Driver

Fig. 2 shows the light-sensitive oscillator and logic driver. The oscillator employs a unijunction transistor. Biasing resistors are selected

by standard techniques to optimize thermal stability.[2] The light sensor is connected through external jacks as indicated. It may be a solid-state photoconductor, a vacuum photodiode, or any similar photosensitive element. The timing capacitor C_T is selected to provide a desirable count rate at the light levels (sensor resistance) employed. The oscillator output pulse is amplified in the logic driver 2N1306 and supplied to the counter gate.

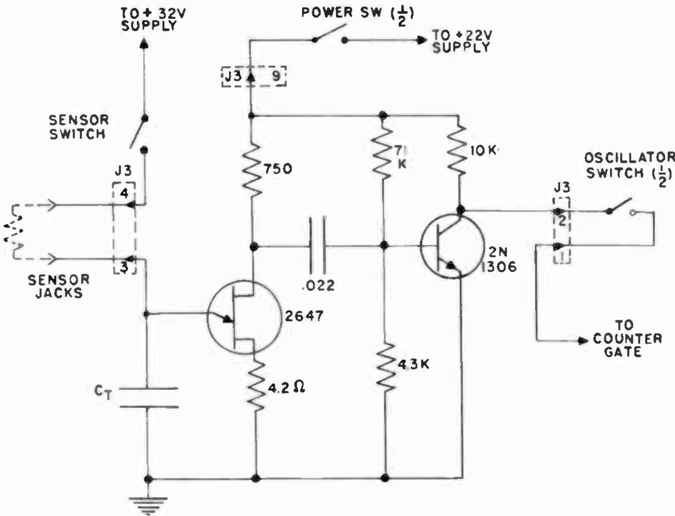

Fig. 2—Oscillator and logic driver.

3. Logic and Count Selector

Fig. 3 is a diagram of the logic and the count-selector switches. The logic circuits gate oscillator pulses to the counter and control the shutter relay. The count-selector switches determine the counter output at which the logic will act to close the shutter.

The counter gate, CD2200 #4, passes pulses from the oscillator to the counter during shutter-open time.

The selector gate, comprising a 2N1306 transistor and three 1N482 diodes, controls the shutter relay and the counter gate. It acts as an AND gate for the outputs of the three decade gates.

The decade gates are connected to the count-selector switches. When the desired count is reached in each decade, they operate to terminate the exposure.

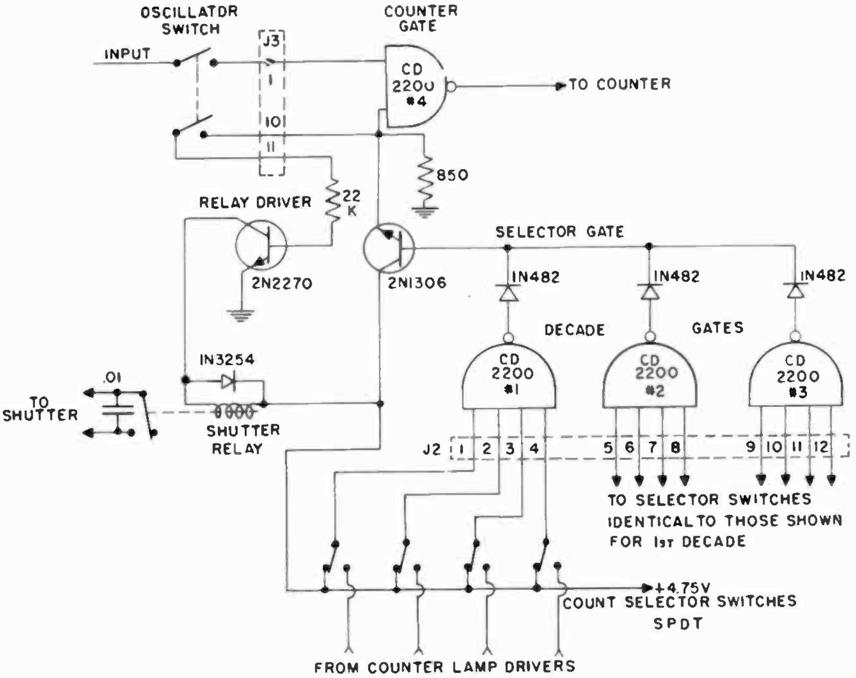

Fig. 3—Logic and count-selector switches.

The count-selector switches are single-pole double-throw switches that connect each input of the decade gates to either a fixed voltage level (+4.75V) or to the counter output. In selecting a desired pulse count (exposure), the switches corresponding to logical 0 in the desired count connect the fixed level (logical "1") to the gates. The switches corresponding to "1" in the desired count connect counter output to the gates. When the desired count is reached, these counter outputs become simultaneously "1" for the first time; the gate inputs are all "1", and the gates operate.

Logic circuit operation will be described assuming a desired count has been set into the selector switches, and the reset button is pushed to start the counters from zero.

A "0" level exists at those decade gate inputs that are connected to the counters through the selector switches. Since the decade gates are NAND gates, a "1" (positive voltage) level exists at the output of one or more decade gates; this activates the selector gate by biasing the associated node on, turning on the 2N1306 transistor. The 2N1306 turns on the relay driver, which operates the shutter relay and opens

the shutter. The 2N1306 also provides a logical "1" level to one input of the counter gate. The other counter gate input is at a logical "1" level from the logic driver. Therefore, the counter gate output is a logical "0" level. When a count occurs, it appears at the counter gate input as a negative pulse. This disables the gate for the duration of the pulse causing a similar positive pulse to appear at the gate output and to enter the counter.

When the preselected count is reached, those counter outputs connected to the decade gates all become 1 simultaneously for the first time since the onset of counting. Since all other decade gate inputs were previously fixed at "1" by the selector switches, every one of the decade gates has a "1" at its input. All outputs become "0", turning off the 2N1306, which turns off the relay driver (closing the shutter) and removes the logical level from the counter gate input, so that no more counts are passed.

Pressing the reset button clears the counters, allowing recycling of the above sequence.

4. Counter

Fig. 4 is a diagram of the counter. It consists of SN7490N counters connected as a five-decade counter circuit. The outputs are in binary-coded decimal format. The three highest decades are connected to indicator lamps through 2N1306 lamp drivers, which also provide outputs to the count selector switches. The reset switch sets all counters to zero to initiate counting. In normal operation, this acts as the shutter control button.

5. Light Sensors

A variety of light sensors were used in the exposure control apparatus. Cadmium sulfide and cadmium sulfo-selenide photoconductors, both ¼-inch diameter and 1-inch diameter units, were evaluated. The best combination of spectral response and stability for mecury vapor illumination was obtained with the RCA 4403 broad area (1-inch diameter) photoconductor.

A vacuum photodiode (Raytheon 934) was also successfully tested with the system. It offers excellent stability and reproducibility, but has relatively low sensitivity and is somewhat less rugged than the CdS detectors. Also, since the charging current from the photodiode is limited to 5 microamps, the timing capacitor must be small.

Testing

The stability objective was to provide exposure times repeatable to within ±1% when sensing a constant light level. Data was gathered by controlling a clock timer with the shutter relay. The timer recorded the number of seconds required to reach a given count. This corresponds to the number of seconds for which the shutter would be open.

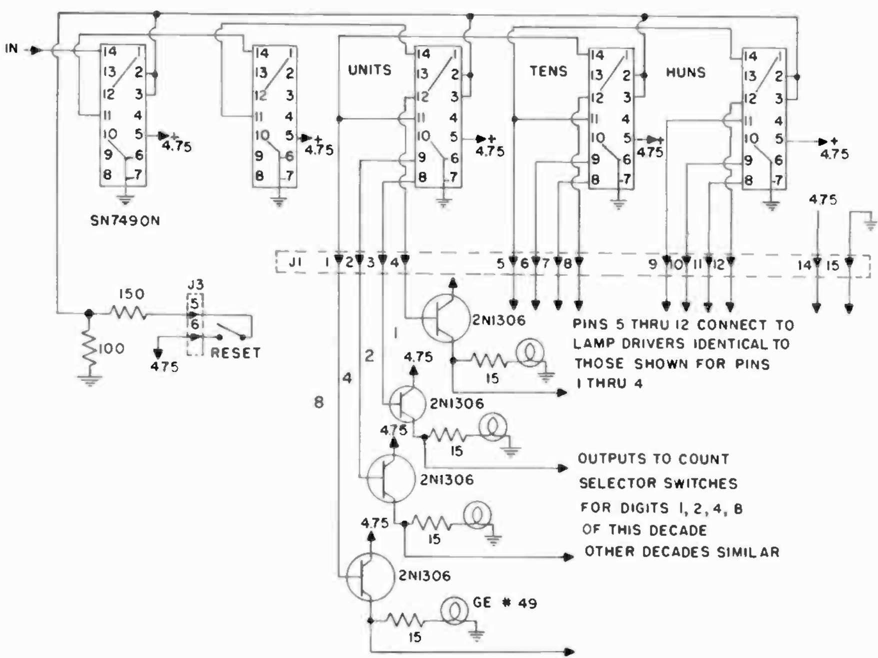

Fig. 4—Five-decade counter.

In a typical series of tests with the 4403 photocell, a standard deviation of 0.18 seconds was obtained for a mean exposure time of 93.7 seconds. The maximum time to reach the corresponding count was 94.0 seconds, and the minimum 93.3 seconds. This gives a variation of less than ±0.5%, well within the desired range.

Sensitivity testing was not based on any fixed standard; the practical design objective was that the system be sensitive enough to function effectively at the light levels normally employed in photoresist exposure.

Conclusions

A system has been constructed and tested for controlling the exposure of photoresists. It has advantages in simplicity, sensitivity, stability, and ruggedness over other available systems.

Acknowledgments

The assistance of J. V. Groppe in circuit design, construction and testing is gratefully acknowledged. W. H. Moles supplied design data for the counter and logic circuitry. J. A. Amick and N. R. Goldstein provided technical advice and stimulating discussion.

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Detection of Damage on Silicon Surfaces: Origin and Propagation of Defects

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Abstract—Boundary conditions were established for the detection of surface damage by oxidation and Sirtl etching, referred to subsequently as OS. The oxidation was performed at 1100°C to obtain in excess of 0.5 micrometer of SiO_2, and was followed by a Sirtl etching. Essentially damage-free surfaces can be prepared by chemical polishing, and these surfaces show no signs of being damaged by the growth of oxide up to 1-micrometer thick. Oxidation only enhances defects already present; it does not cause defects.

Oxides grown on damaged silicon have a relatively low dielectric integrity, as determined by comparison of the OS method with an electrolytic decoration method. Defect propagation between 900° and 1100° C in steam and dry oxygen, after heating in argon and hydrogen was studied. The results suggest that microcracks and their propagation by the wedging action exerted by oxidation fit the described phenomena.

Introduction

Imperfections in the silicon surface of solid-state devices are likely to cause degradation by providing recombination centers as a result of a local change of mobility and resistivity, and by attracting heavy metal impurities (Cu, Au, Fe) and possibly carbon and oxygen so that precipitates are formed.

The literature contains many references that relate electrical faults to defects.[1-10] These references pertain to diffusion-induced faults, scratches, and bulk dislocations, and in most cases deal with (111)-oriented wafers. Queisser and van Loon[10] and Thomas[11] have shown that a characteristic line defect forms when mechanically polished wafers are oxidized, that the defect length is surprisingly uniform, and that the length increases with oxidation time. Fisher and Amick[12] recognized that the line structure, as verified in this study, is characteristic of mechanical damage, that it is observed on (100) and (110) planes as well as on (111) planes, and that the steam oxidation itself does not cause these structures.

J. E. Lawrence[13] studied stacking-fault annihilation by transmission electron microscopy and found a similar line-structure behavior (i.e., growth of defects on strain sites) and annealing effect. Although Lawrence's work dealt with (111) silicon and damage induced by diamond polishing, the defect density and the density change during some types of annealing are similar to the ones found in this study.

The work reported in this paper was undertaken to establish an unambiguous routine method of inspecting the surface perfection of integrated-circuit substrates. This work is part of a comprehensive study on the growth of defect-free oxides.

Oxide-film perfection was also evaluated by an improved pinhole decoration technique.[14] From the pinhole decoration technique, it became clear that the dielectric integrity of oxide films grown on substrates polished with zirconia in sodium hypochlorite medium was considerably poorer than that of oxides prepared on chemically polished wafers.

In view of some conflicting reports about the effect of annealing and oxidation at low temperature, several conditions for development of defect sites were examined. The study of these conditions led to the formation of a phenomenological theory and further tests to establish the facts.

Experimental

Silicon Wafers

Czochralsky n- and p-type wafers with 3×10^{14} to 10^{16} carriers/cm^3 were examined. Except for ascertaining that the techniques provided essentially the same results on (111) planes and that the geometry of faults was similar to those reported by Fisher and Amick,[12] the experimental work was confined to (100)-plane material. Bulk dislocation did not become visible upon Sirtl etching on the (100) orientation; therefore, defect structures can be unambiguously ascribed to external causes.

Methods of Surface Preparation

Chemically polished wafers obtained from commercial sources were prepared by a technique involving acid etching and lapping of sawed wafers and polishing with alkaline silica gel to remove either 30 to 40 micrometers directly or 5 to 10 micrometers after an intermediate zirconia* polish. Alternatively, wafers prepared by copper polishing[15,16] were obtained commercially.

* Nominal particle size was 0.5 micrometer.

Most mechanically polished wafers were prepared by the zirconia method. Some comparison tests, however, were also made on wafers that were first chemically polished by Al_2O_3** in neutral suspension to remove defects. All wafers were cleaned in ammonical and acidic hydrogen peroxide solution as described by Kern and Puotinen.[17]

Oxidation and Etching

Except as otherwise indicated in tables or figures, the wafers were oxidized immediately after cleaning, either in steam or in dry oxygen at 1100°C. Furnaces were checked for cleanliness by periodic capacitance–voltage measurements on metal–oxide–semiconductor (MOS) capacitors and found to produce a device flat-band shift of less than 0.2 volt after 1 minute of 10^6 V/cm bias at 300°C.

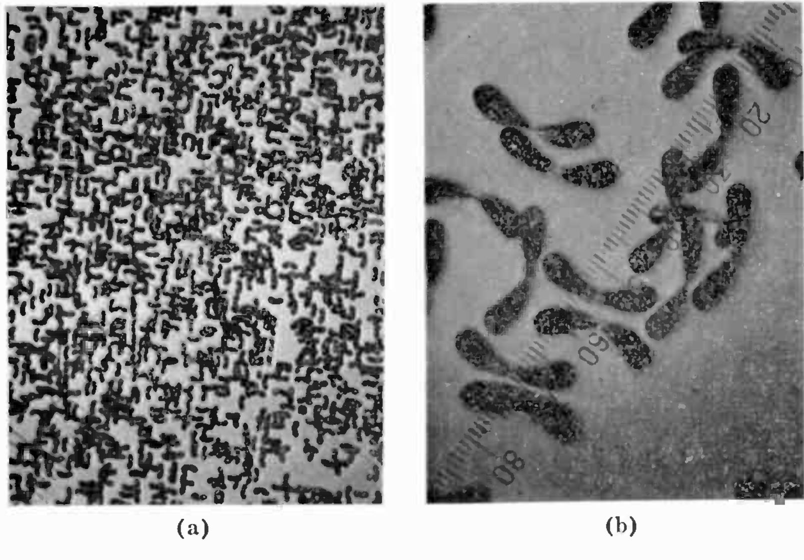
After oxidation, the oxide was checked for thickness by ultraviolet interferometry and then removed by use of hydrofluoric acid. At this stage neither microscopy nor roughness checks made with a Talysurf 4 profilometer revealed any change in surface roughness (<200 Å) compared to the original surface finish.

Next, the samples were etched for 3 minutes in Sirtl etch*[18] and examined by differential interference contrast by use of a Reichert or Nikon microscope. Defect density counts of typical areas were taken from photographs. Talysurf profiles were taken in many instances, and invariably showed that the observed defects, which were typically like those in Fig. 1(a) and 1(b), were raised above the background surface by up to 2 micrometers as shown in Fig. 1(c).

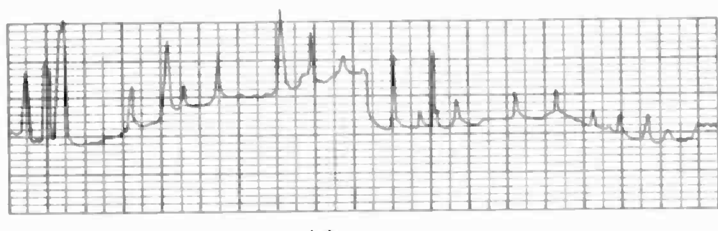
The effect of the etch time on the appearance and height of defects is illustrated in Fig. 2. The defects not only change in appearance, but actually seem to increase in size as etching proceeds from 42 to 51 micrometers in length and from 1 to 12 micrometers in width at the midpoint. The various shapes result from differences in etchability of the defect ends and edges, which consist of spiral dislocations, stacking faults, associated strain fields, and possibly precipitates associated with a defect after OS.

An attempt was made to determine the difference in etch rate between defect and matrix silicon by successive Sirtl etchings and referencing the amount of material removed to a portion of the wafer protected by means of silicon nitride. The defects appear to etch at about half the rate of the matrix; however, the test was not sufficiently

** Linde "B", nominal particle size 0.05 micrometer.
* 50g CrO_3 + 100 ml H_2O + 100 ml 48% HF.



(a) (b)



(c)

Fig. 1—(a) 1.01 μm thick, steam oxide on Lustrox, polished wafer, Sirtl etched surface, magnified 64 times; (b) same as (a) except magnified 640 times, showing defect density of 4×10^6 defects/cm^2; and (c) Talysurf profile of (a); vertical scale, 1 small division equals 0.1 μm; horizontal scale, 1 small division equals 50 μm.

discriminating or precise to provide more than an approximate indication.

The etch rate of undamaged silicon in Sirtl etch at room temperature was about 3 micrometers per minute.

Results

Surface Preparation

Zirconia-polished wafers typically showed 2 to 8×10^6 defects per cm^2 uniformly distributed. Gel-polished wafers from three sources generally

had just a few defects ($\approx$100), but sometimes also had a small number of patches with defect densities up to 1000 per cm^2. Although copper-polished wafers were similar to gel-polished wafers, on occasion the center area contained a patch of defects that were quite uniformly spread and in some wafers were very short (3 micrometers). All defects appeared similar in shape, and ranged in length from 21 to 42 micrometers. In the occasional wafer that had not been completely polished, the defective area had a hazy appearance easily visible to the

	ETCH TIME min	DEPTH μm	DEFECT LENGTH μm	WIDTH μm
(a)	1	3.3	42	1
(b)	3	7	44	3
(c)	6	15	46	6
(d)	12	31.5	51	12

Fig. 2—Effect of Sirtl etch time on defect or morphology of zirconia polished surface for four etch times.

naked eye. Zirconia-polished materials showed closely similar lengths of defects on each wafer, such as 32 to 34 micrometers or 40 to 41 micrometers. Gel-polished wafers showed wider ranges, such as 27 to 34 micrometers or 22 to 36 micrometers. A series of tests was made in which 25-micrometer thicknesses were successively etched from mechanically polished surfaces by use of nitric-hydrofluoric acid (95:5) prior to oxidation. The surface was uneven after etching, but the defect density decreased dramatically after removal of 5 micrometers of surface from a value of 2×10^5/cm^2 to a mostly clear surface having a few patches with 1 to 4×10^3 defects/cm^2. Removal of an additional 5 micrometers of surface did not greatly change this pattern.

Wafers that had received a final polish with alumina had as many defects as zirconia-polished wafers. When gel-, copper-, or alumina-polished wafers were repolished with zirconia, the usual defects appeared after OS. Wafers with no defects that had been deliberately

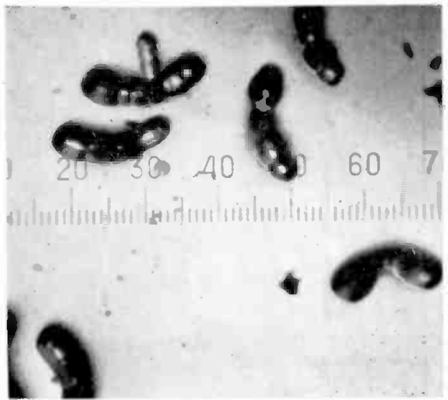


Fig. 3—Scratch made on gel polished silicon by 5.1 μm diameter steel ball after OS (×640).

scratched with stainless steel, titanium, tungsten carbide, or silicon showed similar defects in the scratched areas, as shown in Fig. 3.

Temperature

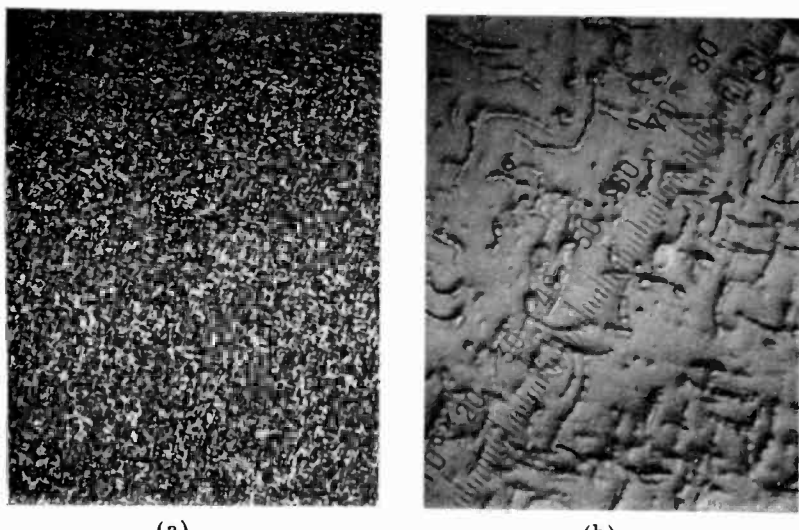
After oxidation at 900°C, no defects could be found, nor did the surface roughness change as measured by the Talysurf profilometer. However, when similar wafers were stripped of their oxides in HF and reoxidized at 1100°C, approximately twice as many defects appeared, but their shape and size were similar to those observed after the 1100°C oxidation alone. Oxidation at 950, 1000, and 1050°C produced conical defects as shown in Table 1.

Table 1—Effect of Temperature on Development After OS of Mechanically Polished Surfaces. (Note that three conditions exist: (1) no defects after 900°C OS, (2) conical defects at >900° and <1100°C, and (3) oxbow shapes at 1100°C. Most of the work described was done at 1100°C.)

Oxide Thickness (micrometers) and Growth Method	Length (micrometers)	Defects Density (cm^{-2})	Type
0.4 at 900°C in steam	none	none	—
0.43 at 900°C in dry O_2	none	none	—
0.43 at 900°C in steam then HF and 0.4 at 1100°C steam	24-27	$8\text{-}10 \times 10^6$	oxbow
0.46 at 1100°C in dry O_2	20-50	$\sim 10^5$	line
0.4 at 950°C in steam	2-3	$\sim 2 \times 10^7$	conical
0.4 at 1000°C in steam	3.5-5	$\sim 2 \times 10^7$	conical
0.4 at 1050°C in steam	4	$\sim 7 \times 10^6$	conical
0.4 at 1100°C in steam	21-23	$3\text{-}4 \times 10^6$	oxbow

Annealing

On the tentative assumption that the propagation of surface defects, scratches, or microcracks was caused by the wedging effect within a crack arising from the volume change during oxidation of SiO_2, annealing in either a neutral or reducing atmosphere was tried prior to oxidation to lessen the propagation. Wafers were heated in an argon atmosphere with less than 5 ppm $(O_2 + H_2O)$ and in some cases containing 5% of palladium-diffused hydrogen. When the wafers were oxidized at



(a) (b)

Fig. 4—Effect of annealing on Lustrox polished surface: (a) 0.74 μm thick steam-grown SiO_2 at 1100°C after 45-minute anneal in Ar at 1100°C, followed by Sirtl etch (×64); (b) at a defect density 5×10^7 defects /cm^2 (×640).

1100°C in steam, the number of defects increased and the length decreased. In addition, the shape of the defects changed. The end loops of the defects disappeared, the main arch showed discrete structure, and the defects separated into fragments, as shown in Figs. 4 and 5. The results of the annealing are summarized in Table 2. The Talysurf traces shown in Fig. 6 indicate that annealing also reduces the apparent height of defects by about one half.

Steam versus Dry Oxidation

Fisher and Amick obtained most of their results from (111) material after oxidation at 1200°C in steam. They briefly mentioned that water

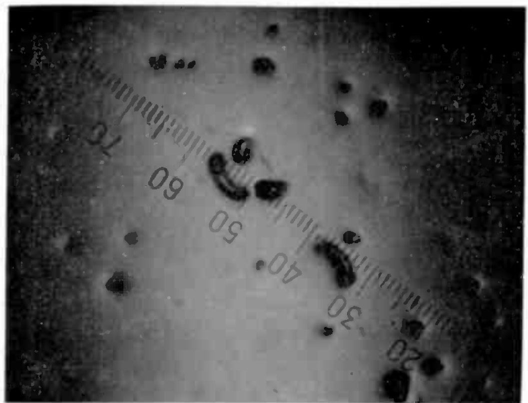
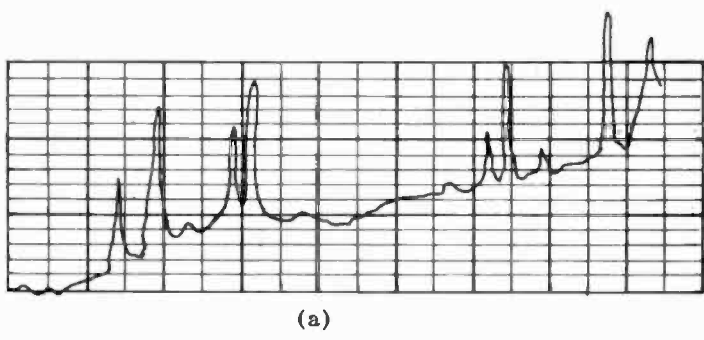
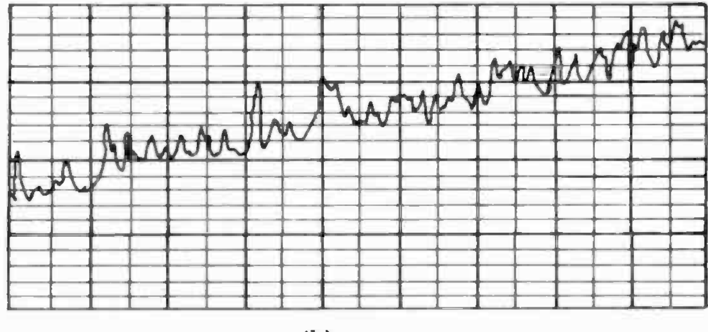


Fig. 5—Effect of H_2 annealing on Lustrox polished surface when annealed 30 minutes in $Ar + 5\% H_2$, oxidized at 1100°C in steam to 1.0 μm thick SiO_2 and Sirtl etched (×640).



(a)



(b)

Fig. 6—Talysurf trace of Sirtl etched surface: (a) 1.0 μm thick steam grown oxide and (b) 45 minute anneal in Ar at 1100°C prior to oxidation (vertical scale, 1 small division = 0.1 μm; horizontal scale, 1 small division = 50 μm).

Table 2—Effect of Annealing Prior to Oxidation (values show ranges of two or more experiments).

1100°C Anneal	Time (min)	Steam Oxidation Time (min)	Steam Oxidation Thickness (μm)	Total Time at 1100°C (min)	length (μm)	Defects Density per cm^2	height (μm)
—	—	130	1.01	130	37-39	$4\text{-}6 \times 10^5$	0.3-1.5
Argon	30	130	1.01	160	14, 20, 28-35	$0.3\text{-}8 \times 10^7$	0.5-1.5
Argon	45	85	0.81	130	10-22	$4\text{-}9 \times 10^7$	0.2-0.6
Argon	85	45	0.56	130	8-14	$2\text{-}30 \times 10^7$	0.2-0.4
Argon	115	15	0.28	130	2-8	$1\text{-}5 \times 10^7$	0.2-0.9
$Ar + 5\% H_2$	30	130	1.01	160	5-14	$1\text{-}4 \times 10^6$	0.2-1.1
$Ar + 5\% H_2$	900	130	1.01	1030	see fig. 5	$\sim 10^6$	0.2-2.2

vapor was necessary to bring out the defect structure and that the length of defect was related to time and oxide thickness. Table 3 indicates that the defects form readily but more slowly in dry oxygen than in steam; for oxide thicknesses in excess of 0.5 micrometer, the results are unambiguous. When lengths of defects are compared, it is clear that defects grown in dry oxygen are much longer (for equivalent oxide thickness) than those formed in steam, as shown in Fig. 7. Also,

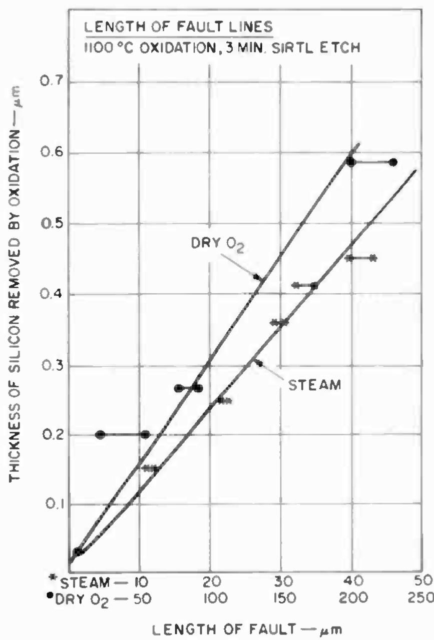
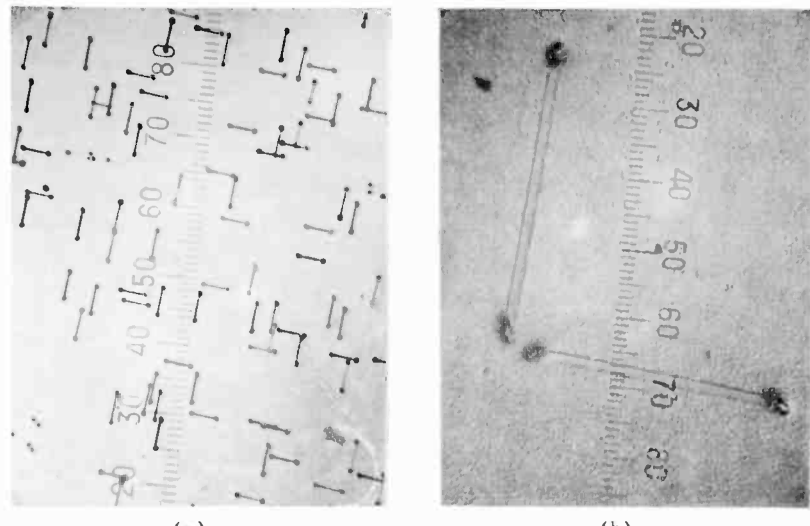


Fig. 7—Thickness of silicon removed by 1100°C oxidation and three-minute Sirtl etch as a function of length of fault.

the defects appear straighter and thinner than those produced by steam oxidation, as shown in Fig. 8. Overetching produces different appearances from defects obtained from steam oxidation, as shown in Fig. 9.

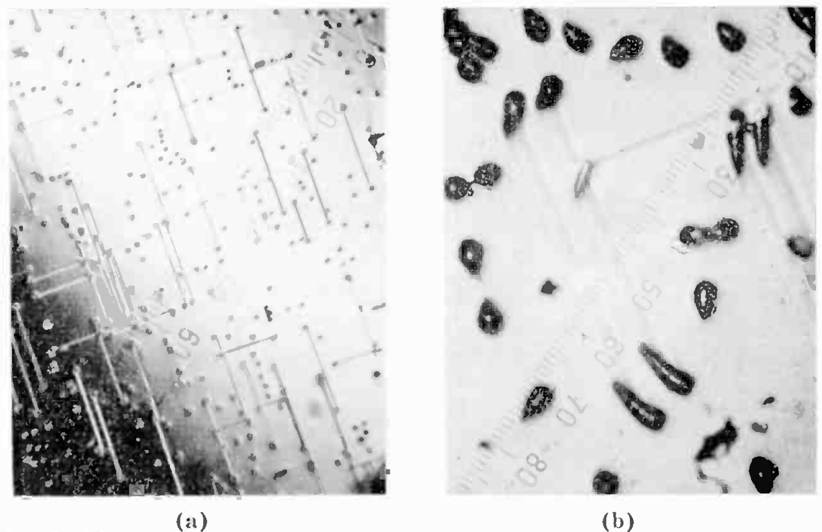
Dielectric Properties of Oxides in Relation to Defects

A comparison of a typical OS haze pattern for poorly polished silicon wafers is compared with the copper decoration method in Fig. 10. An important consideration is the electrical behavior of the Si–SiO_2 interface. As a check of this behavior, "good" and "bad" wafers were oxidized and decorated with copper by the technique referred to by



(a) (b)

Fig. 8—Dry oxidation Lustrox polished surface: (a) 0.60 μm thick SiO_2 grown in dry O_2 at 1100°C for 960 minutes, Sirtl etched (×64); (b) at a defect density of 5 × 10^5 defects/cm^2, length 80-90 μm (×640).



(a) (b)

Fig. 9—Defect patterns after prolonged oxidation: (a) Sirtl etched after 68 hours oxidation at 1100°C in dry O_2 (1.33 μm SiO_2) (note formation of dot defects) (×64); (b) effect of extended etching (12 minutes in Sirtl etch) on the appearance of the defects (×320).

Shannon.[14] There was a close correspondence between wafers that showed a high defect density by the OS method and the oxide integrity.

In addition, the percentage of short circuits in MOS transistor gates was 10 to 20% higher in mechanically polished wafers, as compared to chemically polished silicon.

Table 3—Defects Produced by Steam and Dry O_2 Conditions

Oxidation		Defects	
Time (min)	Thickness (μm)	Length (μm)	Density per cm^2
Steam at 1100°C			
15	0.3	9-11	$2\text{-}4 \times 10^5$
45	0.54	21-23	$3\text{-}6 \times 10^5$
85	0.80	30-32	$4\text{-}8 \times 10^5$
130	1.01	37-39	$4\text{-}8 \times 10^5$
Dry O_2 at 1100°C			
42	0.1	2-3	$\sim 10^5$
480	0.46	20-50	$\sim 10^5$
460	0.60	80-90	5×10^5
4100	1.33	200-230 4-6	$2\text{-}4 \times 10^5$* $1\text{-}2 \times 10^6$**

* Lines (see Fig. 8).
** Dots (see Fig. 8).

Recommended Procedure

Wafers to be tested should be cleaned by any of the well-established methods used in "clean" technology, and oxidized at 1100°C in steam to grow between 0.5 and 0.8 micrometer of SiO_2. The oxide is then removed by means of dilute hydrofluoric acid, and the wafer is Sirtl etched for three minutes, rinsed, and dried. Wafers are photographed under oblique illumination to show any haze pattern over the entire wafer. They are then examined by use of a low- (40 to 80×) and high-power (400 to 800×) differential interference contrast microscope.

Discussion

The results of this study suggest that abrasive polishing can cause damage to a silicon surface that invariably leads to the formation of severe crystal defects upon oxidation. There is also evidence to suggest that an oxide grown on a mechanically damaged surface contains

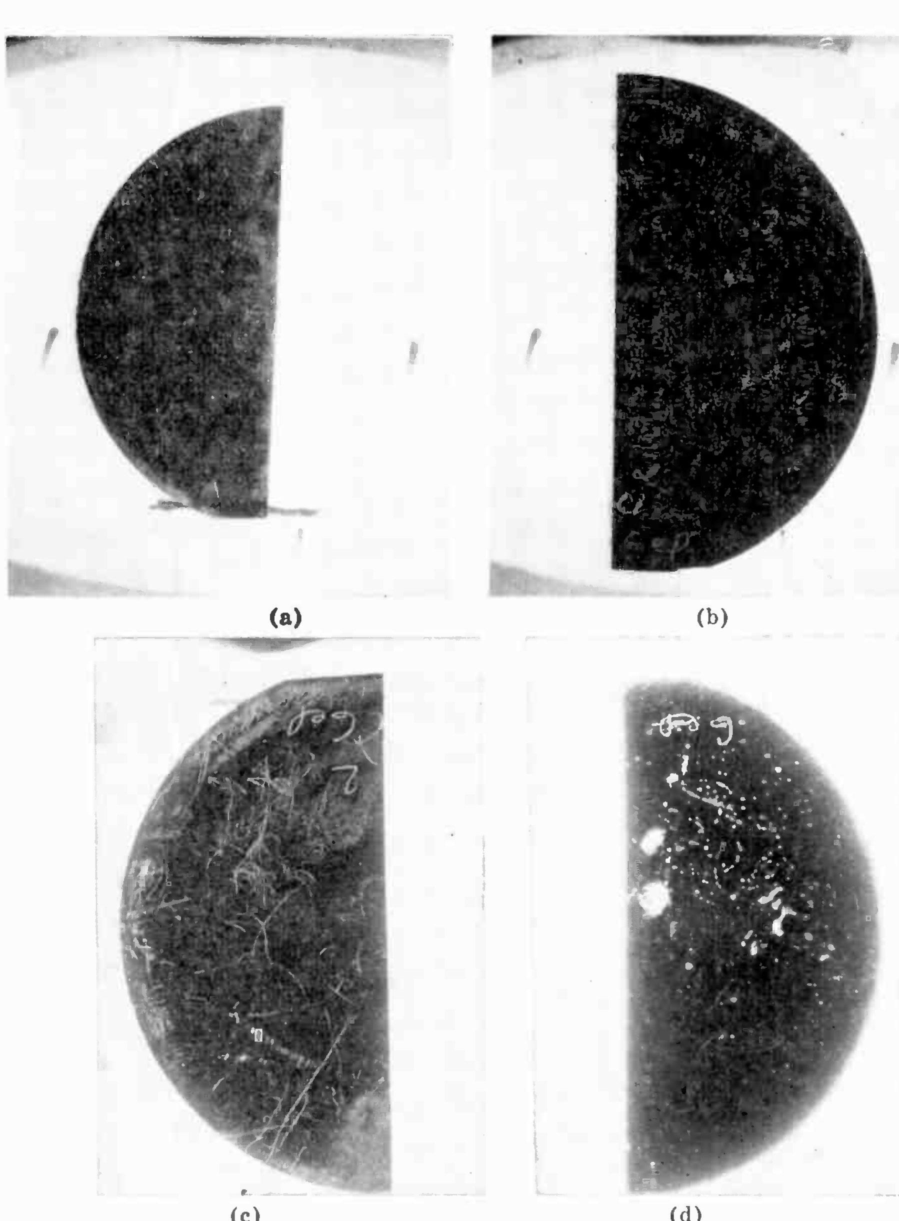


Fig. 10—Comparison of OS with Copper decoration as a method of defect detection: (a) OS on mechanically polished surface (hazy areas have 5×10^5 defects/cm^2; (b) same as (a), but chemically polished surface (note scratches on the right edge due to poor handling); (c) OS on gel polished wafer (insufficient surface removed to remove damage; (d) copper decorated defects on poorly polished wafer (1000Å SiO_2 5×10^6 V/cm field during decoration[14]).

more dielectric defects than that grown on undamaged chemically polished silicon. There was no investigation to determine whether this mechanical damage was caused by poor polishing technique or inevitably caused by ZrO_2 in alkaline media. However, wafers sampled over a three-year period, including polished defect-free wafers and deliberately scratched wafers showed similar defects on OS etching. It is reasonable to assume that damage was present in all the ZrO_2-polished wafers, and that the oxidation and annealing effects are, in fact, caused by some interaction of damage and oxygen.

The following observations and comments can be made as a result of this investigation:

(a) Oxidation in steam or dry oxygen leads to the generation of similar defects except that the defects become about four times longer in dry oxygen than in steam for comparable amounts of silicon oxidized, as shown in Fig. 7. The fact that the length of the defect line varies with the square root of time suggests a diffusion or precipitation phenomenon.

(b) Virtually no defects can be detected as a result of the OS method on chemically polished material. Zirconia- and alumina-polished silicon oxidized at 1100°C exhibits 10^5 to 10^6 faults irrespective of oxidation time or method (dry O_2 or steam). No damage is detectable by microscopy or Talysurf profilometry before or after oxidation but prior to Sirtl etching. The implication is that potential sites for defects are created by mechanical damage but are revealed only by oxidation. It appears that a dynamic relationship is involved in the generation of the defects.

(c) Zirconia-polished wafers oxidized at temperatures of 1100°C or more produce oxbow-shaped defects that often have pronounced terminal thickening. At 950, 1000, and 1050°C, the defects are conical. (Electron microscopy and diffraction may give more precise information in three dimensions.) No defects are observable after OS at 900°C or less. However, when oxidation at 900°C is followed by removal of this oxide and reoxidation at 1100°C and etching, the usual defects reappear. At least two mechanisms are therefore involved in the generation and propagation of defects.

(d) Annealing in argon prior to oxidation decreases the length and height of the defects after Sirtl etching, but vastly increases the number of defects. Heat treatment at 1100°C in hydrogen reduces the size and number of defects drastically. The hydrogen treatment implicates oxygen as a major factor by reducing SiO_2 to a volatile species (H_2O and SiO) more rapidly than neutral annealing, in which only silicon monoxide resulting from the reaction of $Si + SiO_2 = 2SiO$

can form. It is speculated that discrete sites exist in defect areas that have a different reactivity because of a strain field arising from localized clustering of oxygen atoms around the lattice strain or mismatch point. It is suggested that these sites reduce more easily, so that each defect can break up into several discrete portions; this assumption explains the apparent increase in numbers, but decrease in size, during the initial heating in argon and the more rapid reduction in hydrogen.

(e) The effect of prolonged oxidation shows that defect propagation is primarily a surface phenomenon. Observations indicate that, compared to defect length, the defects do not extend very deeply into the surface as determined by cleaving and by the appearance of the defects on Sirtl etching. However, during very long, dry oxidation (68 hours at 1100°C), a second type of defect develops that is conical in shape; this behavior may indicate bulk phenomena.

This phenomenological approach suggests that zirconia polishing causes stress corrosion and leaves strained sites in the silicon surface. The high degree of uniformity of length and shape of defects suggests that not just crude scratches are involved (although some are clearly visible). Rather, it is believed that the abrasive action of the ZrO_2 is coupled with oxidation promoted by the alkaline medium, and that these oxidized sites cause strain sites that, in turn, act as nucleation centers for further precipitation reactions. The volume expansion when Si oxidizes to SiO_2 is about a factor of 2.3 and can, therefore, put considerable strain into the surface layer, as demonstrated by Prussin.[19] In addition, deeper scratches or micro-cracks oxidize and may also contain debris that appear as extra stress razurs. No zirconium was detected in the surface of ZrO_2-polished wafers by electron microprobe analysis.

It is believed that the damage sites become natural centers for attracting fast diffusion impurities, and also change the local oxidation rates sufficiently to be the cause of dielectric defect centers in the resulting oxide films.

The different observations at low and high temperatures can be correlated with a competing annealing reaction that involves the self-diffusion rate in silicon and its yield strength. For example, at 900°C oxygen diffusion presumably proceeds along the damage sites ahead of the advancing Si–SiO_2 boundary. However, very little healing can take place at the tip of the defect, because the self-diffusion rate of silicon is too small and the temperature is too low to achieve substantial stress relief.

At 1100°C, especially at the low oxidation rate in dry O_2 (as com-

pared to the rapid oxidation rate in steam), stress relief by self-diffusion is pronounced and penetration in depth is limited. The appearance of a different defect at intermediate temperatures suggest that a mechanism of horizontal propagation having a different activation energy is preponderant. The crystallographic propagation of the strain centers into the surface under the influence of the wedging action of oxidation is highly complex and requires considerably more sophisticated analysis by such methods as electron-beam microprobe, electron microscopy and diffraction, Auger spectroscopy, transmission electron microscopy, infrared transmission, or copper decoration before strain propagation can be elucidated.

The oxidation-differential etch technique is capable of delineating the area and density of defects. The correlation of this work with other diagnostic techniques and device parameter studies promises to lead to substantial improvements in process technology because of quantitative measurements that the new methods provide. It is also essential to the manufacture of a technically and economically sound product that a better understanding be gained of the damage and its propagation in successive processing steps, and that this defect propagation be related to device parameters.

Acknowledgments

The author thanks B. Upton for sample measurements, D. A. Puotinen and W. J. Shannon for helpful discussions, R. Vibronek for help with cross-checking, and E. Bertin for the electron-microprobe analyses.

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A Study of Dielectric Defect Detection by Decoration With Copper

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Abstract—A reproducible technique for locating defects in dielectric films was established by decoration with copper. The reproducibility of the decoration method was found to be dependent on the electrolytic conductivity, the electric field distribution, and the dielectric surface potential. Examination showed that many of the defect sites were nucleated with a central pit that took on the orientation of the substrate. The decoration method was used to examine the relationship between the type of silicon surface preparation and the integrity of the oxide. The decoration study revealed that chemically polished wafers had approximately one-half as many defects as abrasively polished wafers.

Introduction

Defects in dielectric isolation are a major cause of low yields in the fabrication of monolithic silicon integrated circuits and metal-oxide-semiconductor (MOS) devices.

Defects in dielectric films are caused by differences in oxidation rates (resulting from surface damage that leads to thin spots), residual abrasive and dust particles disrupting the continuity of the oxide (as a result of the formation of glass with a large coefficient of thermal expansion that causes cracking upon cooling), and mechanical flexing of wafers (which leads to strain and cracking).

The minute size of the dielectric film defects and the highly reflective nature of the dielectric film preclude microscopy as a practical method of detection. Other methods to detect the dielectric film defects that have been explored include replica electron miscroscopy, high-temperature chlorine etching, and the electrochemical autograph[1]; however, none of these methods were found to be both simple and reproducible. Although the voltage breakdown of MOS capacitors has been used as a guide, this method requires extensive preparation and interpretive effort. Measurement of the true dielectric leakage is

difficult, because many defects are partial or potential pinholes, and the amount of leakage is dependent on the strength of the electric field.

Because the electric field plays such a critical role in an MOS device, the most promising method for the rapid location of dielectric defects seemed to be decoration with copper. Although the decoration methods described by Besser and Meinhard[1] and Navan[2] showed the technique to be feasible, these methods did not consider either the electric-field distribution or the surface-voltage dependence of the integrity of the dielectric. This paper presents data that describe some of the interactions associated with the decoration technique and applies the technique to a study of the relationship between silicon surface preparation and the oxide integrity.

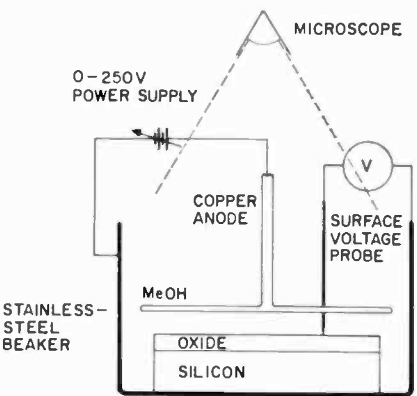

Fig. 1—Experimental apparatus.

Apparatus and Technique

The experimental apparatus consisted of a 0-to-250-volt dc constant-voltage power supply, a stainless-steel beaker used both to hold the wafer and to make cathodic contact to the silicon substrate, a low-power microscope and light to view the decoration, and a micromanipulator to hold the copper anode and the surface voltage probe. To assure uniform decoration, the electric field was made uniform across the wafer by use of a copper mesh as the anode. In all cases, the copper mesh was larger than the diameter of the silicon wafer, as shown in Fig. 1.

Because the voltage drop across the absolute methanol electrolyte is a large percentage of the potential applied to the anode, only the voltage measured at the surface of the oxide controls the field within

the oxide, and thus the defect density. The potential gradient between the anode and the oxide layer serves only to propel the copper ions to the vicinity of the oxide surface, where the ions interact with the high-field centers caused by the defects.

The surface potential was varied by manipulation of both the power-supply controls and the distance between the wafer and the copper anode. (Once the surface voltage was set, it varied by plus or minus 5% over a 1-hour period as a result of slight changes in the resistivity of the methanol caused by hydration and evaporation.) The anode was etched regularly in dilute nitric acid to remove the copper oxide build-up, and dust contamination was avoided by installing the entire apparatus in a laminar-flow station. Appendix A describes the details of actual operation.

Reproducibility

The reproducibility of the decoration technique at a constant surface potential was demonstrated by first oxidizing a (100)-plane copper-polished silicon wafer to 1000 Å in steam, etching the oxide off the back with HF, and decorating for one minute with a surface potential of 60 volts (6×10^6 V/cm). The wafer was then photographed under oblique illumination. The copper deposits were etched off in dilute nitric acid, and the decoration was repeated. Macrophotographs of the two samples are shown in Fig. 2. The average defect density was 13.5/cm^2 and 14.8/cm^2, respectively.

Examination of the defect sites by use of differential interference microscopy showed that copper was deposited in a ring around the site. The area directly around the site was clear, and in many cases the site itself bore the orientation pattern of the (100) crystal plane properly aligned to the (011) reference flat plane of the wafer, as shown in Fig. 3.

When a (111)-plane wafer was decorated as described previously, many of the central defect sites bore the triangular orientation of that crystal plane properly aligned to the (011) reference flat plane, as shown in Fig. 4. If the decoration were allowed to continue, however, the deposit would eventually cover the defect site completely.

Application

For investigation of dielectric integrity as a function of surface preparation, (100)-plane Lustrox, silica-gel, and copper-polished wafers were oxidized to 1000 Å in steam at 1100°C. All wafers received identical pre-oxidation cleaning, as described by Kern and Puotinen[3].

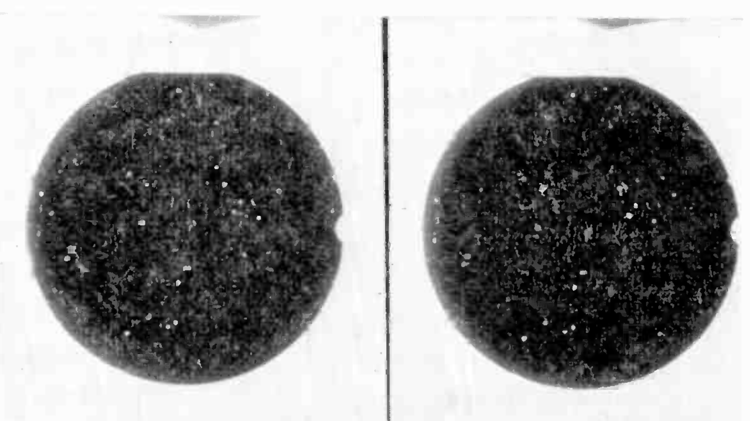

Fig. 2—Reproducible decoration patterns.

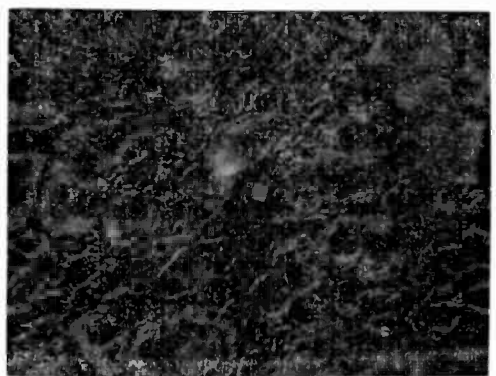

Fig. 3—(100) Copper decorated site.

Fig. 4—(111) Copper decorated site.

The oxide was then removed from the backs of the wafers with HF, and each oxide was decorated and photographed according to the following sequence:

Oxide Field (V/cm)	Time (minutes)
1×10^6	30
2×10^6	2
4×10^6	1
6×10^6	1
8×10^6	1

The decorations were observed to grow in size but not increase in number as a function of time.

Fig. 5 shows some typical photographs after oxidation. In addition to local defect sites, scratches caused by abrasive polishing or handling by forceps are clearly visible. Fig. 6 shows a curve of average defect density as a function of applied field for each of the polishing techniques.

Discussion

Figs. 5 and 6 indicate that dielectric integrity is relative and exponentially dependent upon surface voltage. (The curves in Fig. 6 represent a least-squares exponential fit of the average defect density as a function of oxide-field data, the correlation coefficients were 0.973, 0.982, and 0.986, respectively.) A valid operational voltage for checking oxide integrity for a specific application might be a surface voltage equivalent to the electric field that the oxide is subjected to under final circuit probing. Dielectric films that show no defects after this surface-voltage exposure would be considered to possess adequate dielectric strength.

The topography of the decorated site is shown in Figs. 3 and 4. Copper does not appear to deposit at the central nucleation site nor on the area directly around the site. It is hypothesized that the gas evolution (which Navan[2] identified as hydrogen by gas chromatography and believed to be caused by electrolysis of absorbed water) originating from the center of the defect site limits the diffusion of the copper ions towards the high-field spot and forces the copper to discharge around, rather than on, the defect site. Eventually, enough copper is deposited around the site to cover the nucleation center.

The crystallographic orientation of the central pit is explained by assuming that a defect, such as a crack or a discontinuity, in the oxide causes a sufficient build-up in hydrogen pressure to blow out a section of the oxide and an attached piece of the silicon substrate. This sequence of events has been qualitatively verified by the observation

that more crystallographically oriented defect sites appeared on wafers decorated at high surface voltages than at lower voltages, and that more hydrogen was evolved. These events indicate that decoration is a destructive test.

Figs. 5 and 6 also show substantially fewer oxide decorations on the chemically polished wafers than on the mechanically polished

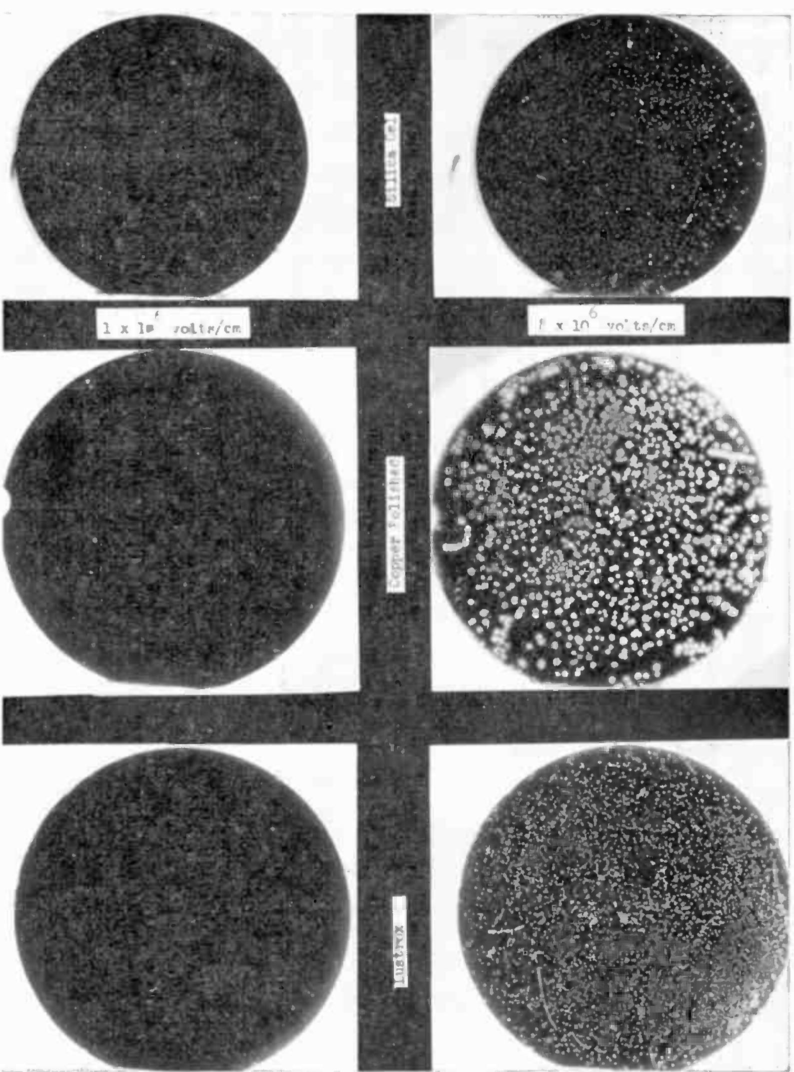

Fig. 5—Typical photographs.

silicon wafers. Fewer decorations are expected, because some of the oxide defects on the mechanically polished wafers are caused by abrasive particles or debris left in micro-cracks that cause discontinuities or weak spots during oxidation.

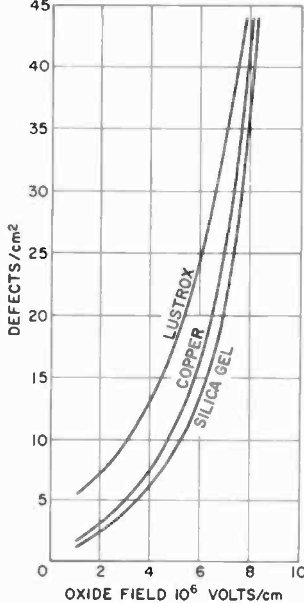

Fig. 6—Defects as a function of oxide field for different polishing techniques.

Conclusion

Decoration by copper on dielectric layers has been found to be a valuable tool in locating electrically active sites on both oxide and nitride layers. When properly implemented and applied, the decoration method becomes a quick and reliable method of determining dielectric integrity.

Acknowledgments

The author thanks R. Vibronek for help in the early stages of experimentation, S. Sestrich for help in building the current apparatus and preparing and decorating the samples, and D. Puotinen and A. Mayer for many valuable suggestions and technical discussions.

Appendix A—Detailed Operating Instructions for the Copper Decoration.

1. Etch the beaker and the copper anode in $H_2O:HNO_3$ (20:1) to remove any oxide layers.
2. Rinse the beaker and the copper anode in deionized water; follow with a rinse in absolute methanol to remove any remaining water.
3. Place the wafer in the beaker, position the copper anode approximately ⅜-inch above the oxide area, and fill the beaker with absolute methanol.
4. Set the surface-voltage probe on the oxide surface.
5. Adjust the power-supply controls or the anode height to obtain the desired surface voltage.
6. Continue decorating until a copper ring becomes visible around the defect site.
7. Remove wafer and at 2-3× using oblique illumination.

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Selective Electroless Plating by Selective Deactivation

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Abstract—A technique for the selective plating of metals and their alloys on dielectric substrates is described. The deposited metal film is confined to the surface of a patterned organic film rather than the underlying substrates. This newly developed technique is based upon the selective etching of catalytic nuclei from certain regions and thus confining the plating to those regions where the catalyst is present.

Introduction

Selective electroless plating of metals may be defined as the deposition of metals on preselected areas of a given substrate. There is a growing need for such processes, especially in the electronic industry, since they lead to inexpensive techniques for the fabrication of semiconductor devices, metal arrays, and printed circuits. Selective electroless plating also lends itself to the forming of precision metal parts, and thus eliminates typical problems of undercutting commonly observed in etch-down processes.

To electrolessly plate on dielectric substrates, it is necessary to provide a catalytic surface capable of initiating deposition. Although there are several possible methods[1] for providing the requisite catalyst, the following two-step sequence is by far the most commonly employed. The substrate to be plated is immersed in an acidic stannous chloride solution, rinsed in water, dipped into an acidic palladium chloride solution, and then rinsed again.

The following are believed to be the main physical and chemical reactions taking place during this sequence:

1. *Sensitization through stannous adsorption*

$$Sn^{+2} + S^* \rightarrow S^*.Sn^{+2} \text{ (adsorbed)}$$

2. *Activation through a chemical replacement*

$$S^*.Sn^{+2} \text{ (adsorbed)} + Pd^{2+} \rightarrow S^*.Pd \text{ (adsorbed)} + Sn^{+4}$$

where S^* is the surface site on dielectric surfaces. Although the detailed structure of the adsorbed stannous layer is not well understood,

evidence exists that freshly deposited layers consist of a hydrated stannous oxide[2] phase (which forms in alkaline media) as well as a stannic oxide phase.[3]

The net result of this sequence[4] is the formation of finely divided (approximately 50 Å in diameter) catalytic palladium nuclei giving a surface with an island-type structure. The average "thickness" of the palladium layer is less than that for a monatomic surface layer. It is the physical presence and chemical activity of the palladium that is a prerequisite for the initiation of the electroless plating processes.

In order to achieve selectivity in the subsequent deposition of a metal layer by electroless plating, various methods for providing patterns of catalytic nuclei are used. Although several techniques[5] for selective electroless plating are described in the literature, the one described in this paper provides for selective plating on a special organic film on a substrate, rather than on the underlying substrate itself.

Experimental Procedures

Fig. 1 shows the main steps used in the current process. Typical 2 × 2 inch glass slides (E. Leitz, Inc., No. 19821) having low porosity were used as substrates. At the conclusion of step 1 (Fig. 1) an organic film pattern is present on the surface. The pattern chosen corresponds to the final metallic pattern desired. Typical patterning materials are dichromate-sensitized fish glue and dichromate-sensitized PVA photoresists. These materials are often employed for their low cost and because they are developed in aqueous media. The composition and mode of application of the resists was standard. Commercial positive photoresists have also been used successfully for this purpose. Following the patterning step, the substrate is immersed in stannous chloride sensitizer, followed by an immersion in palladium chloride activator. At this stage (Fig. 1, step 2) the palladium catalyst is present on both the substrate and the organic film. By a brief immersion in a suitable etchant (e.g., aqueous $FeCl_3$, HNO_3, HCl, or H_2SO_4), a selective deactivation of the catalyst on the substrate surface takes place. Subsequent immersion into an electroless plating bath results in the selective deposition as shown at the conclusion of step 4. Although palladium is used most commonly as the catalytic initiator, silver and gold activators were also employed successfully in the current technique.

To obtain a qualitative estimate of the palladium and tin present following each of the basic steps in Fig. 1, an electron microprobe was

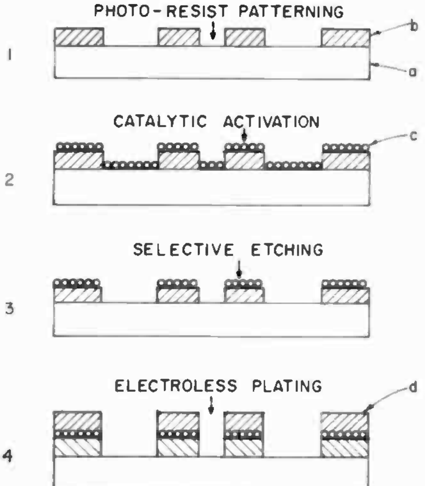

Fig. 1—Selective plating through selective etching (a. dielectric substrate, b. photoresist, c. catalyst, d. electroless metal deposit).

utilized. Measurements were carried out on a glass substrate with a patterned PVA resist. Table I shows the relative number of counts for Pd $\overline{L\alpha_1}$, Sn $\overline{L\alpha_1}$ lines. The etchant used in this instance was 30% HNO_3 at room temperature.

From Table I, it is apparent that the Sn (and consequently the Pd) concentration on the photoresist surface is greater than the concentration on the substrate surface. This effect is probably caused by the photoresist surface having a greater area than its geometrical area, probably due to surface roughness. This increased surface roughness allows for increased catalyst surface density. It is interesting to note that there is a significant count for the adsorbed tin, suggesting that the replacement of the stannous ion by the palladium ion is incomplete. Excess etching will result in the deactivation of both photoresist and glass surfaces.

Table I—Measured Net Intensity of X-Ray Spectral Line Counts/20 sec.

Sample	Etching Time (Sec)	Palladium		Tin	
		Glass	Photoresist	Glass	Photoresist
1	None	14	63	238	341
2	10	ND*	25	102	185
3	20	ND*	ND*	85	69

* Not detected.

Due to the differing characteristics of various organic films, it was found that a mild baking prior to the etching is especially helpful in those cases in which the organic film does not provide sufficient "protection" for the catalyst. During baking, the selectivity of the process is greatly enhanced.

One application of this process is the formation of precision parts by selective plating. Typically, 500 lines/inch mesh patterns could be prepared with good resolution. With proper precautions in handling the resist and the plating solutions, mesh patterns having 1000 lines/inch could also be formed. The technique should be useful in preparing embedded circuits,[6] using either chemical plating, or a combination of chemical and electrolytic plating. The process lends itself readily to reprocessing of the substrates, provided the initial patterned layer is unaltered.

Conclusions

With the increased technological emphasis on electroless plating processes, selective deposition techniques are being developed to yield simplified patterned deposition processes. In contrast to most selective electroless plating techniques, the technique described in this paper permits deposition of metals onto a patterned organic film rather than onto the underlying substrate. Although the technique is best operated with nonporous substrates, modifications can be made to permit use of the technique in conjunction with porous substrates. The substrate employed in this process may serve either as a temporary "handle" on which a metallic pattern is formed, or it may be present in the final product with the resist film and metallic pattern adherent to it.

Acknowledgment

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A Novel Technique for Forming Glass-to-Metal Seals Using a Silicon Nitride Interface Layer

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Abstract—A novel technique for fabricating glass-to-metal seals has been developed. It is based on the use of a silicon nitride layer either as a substitute for, or in addition to, the metal/metal-oxide layer in the seal. This method offers a number of advantages over standard techniques for forming glass-to-metal seals.

Introduction

A glass-to-metal seal normally comprises a glass, a metal, and an intermediate transition layer of an oxide of the metal being sealed. The quality of the seal is principally dependent on the nature of this transition layer. The exact mechanism by which the oxide bonds the glass to the metal is still subject to debate, but the general principles leading to a good seal are well established. It is necessary that the metal oxide layer be adherent to the metal, and that the glass "wet" the oxide. In order for the metal oxide to be adherent, it must remain very thin, normally below 1 micron in thickness, to prevent scaling and a weakening of the seal.

Although thin, adherent oxide layers can be formed on the surface of most metals, it is often difficult to maintain this quality during glassing in air. Consequently, the procedures for making seals are often restrictive and/or expensive. For example, in the case of molybdenum, a heavy powdery oxide is rapidly formed in the presence of air, making it necessary for the sealing to be done in a nonoxidizing atmosphere. This requirement makes it impractical to fabricate molybdenum–glass seals with a torch or in a lathe; rather it is necessary to use a controlled-atmosphere oven.

Another problem encountered is the reaction of the glass with the metal or oxide to form undesirable products in the seal. Tungsten oxide (WO_3) for example often reacts[1] with sodium in the glass to form a

series of sodium tungstate structures. Since these are somewhat water soluble, seals containing appreciable amounts of them are prone to leak when exposed to humid or wet conditions.

Gold presents another unique problem, since it does not form an oxide. Consequently, no method of making a glass-to-gold seal has heretofore been found to the knowledge of the authors.

The method of making glass-to-metal seals described in this paper circumvents these and other problems normally encountered in a glass–metal sealing. It makes possible the fabrication of structures and material combinations that have been impractical or impossible to prepare by earlier methods.

Concept

The glass-to-metal sealing method described here is based on the use of a silicon nitride layer, either as a substitute for, or in addition to, the metal-oxide layer in the seal.

Silicon nitride can be deposited from the vapor phase onto any metal that will withstand the deposition temperature, about 700°C, in a reducing atmosphere. The adhesion of submicron-thick silicon nitride films to all metals tested appears to be excellent, and the silicon nitride was found to be readily "wet" by a wide variety of common glasses and frits.

An important property of silicon nitride, one that renders it useful for this purpose, is its impermeability to oxygen and metal ions. This impermeability has been exploited in the semiconductor art, where Si_3N_4 films only about 1000 Å thick are used as diffusion barriers against oxygen, alkali metals, and semiconductor dopants.

Hence, a metal member that is coated with a thin Si_3N_4 layer can be glassed by any desired technique in ordinary room atmosphere without danger of over-oxidizing the metal, corroding it, or having it react with the glass.

Silicon Nitride Deposition

Chemical reactions used to form silicon nitride layers involve a source of silicon, such as SiH_4, and a source of nitrogen, usually NH_3. A typical reaction, the one used in this work, is

$$3SiH_4 + 4NH_3 \xrightarrow{>600^\circ C} Si_3N_4 + 12H_2.$$

Heating may be carried out either in a resistance-heated furnace, or in

an rf-heated appartus. If the size and geometry of the sample permit, rf heating is preferred, since it avoids undesirable deposition of silicon nitride on the furnace walls.

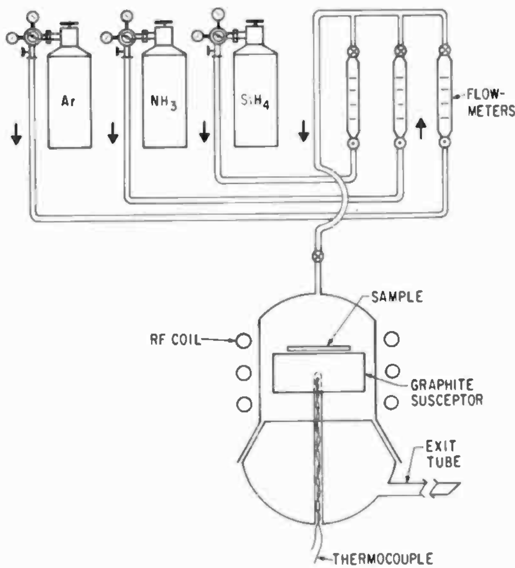

Fig. 1—Si_3N_4 deposition system.

A diagram of the rf deposition system used to prepare the samples for the work reported here is shown in Fig. 1. The fused-quartz reaction chamber is about 2 inches in diameter by 6 inches long. A gas exit attached to 5 feet of ¼ inch tubing, with a 1/16-inch-diameter constricted opening at the end is provided. The long, constricted, exit tube prevents the back-diffusion of air, which would degrade the deposit by forming a silicon oxynitride. The steps in a typical Si_3N_4 deposition proceed as follows:

1. The metal part is placed on the susceptor block, or, if the geometry is suitable, the metal part can act as the susceptor.
2. The system is purged with Ar flowing at 1 liter/min for 10 min.
3. The Ar is turned off and the NH_3 is turned on at a flow rate of 85 cc/min.
4. The metal is allowed to equilibrate in the NH_3 atmosphere at a

suitable temperature. If the metal being coated has an oxide that can be chemically reduced at a temperature below the melting point of the metal, the reduction may proceed during this interval. In the case of tungsten, for example, the native surface oxides are reduced in the 800-900°C temperature range in hydrogen or NH_3. Metals can also be degassed by heating them to a suitable temperature in either NH_3 or H_2.

5. The silane (SiH_4) is turned on. A flow rate of 1 cc/min of 3% silane in hydrogen was generally used. Empirically it was found necessary to maintain a high ratio of NH_3 to SiH_4 in order to obtain good-quality films. Ratios of 45:1 to 200:1 were found to give satisfactory Si_3N_4 layers. Under these conditions the deposition rate of the Si_3N_4 is about 1000 Å/min.
6. After the required film thickness is obtained, the SiH_4 flow and the rf generator are turned off. When the system has cooled, the NH_3 is turned off and the sample is removed.

Experimental

Flat sheets of various metals, about $1 \times 1 \times 1/32$ inch were coated on both sides with silicon nitride by the process described above. A control sample of each type of metal without the Si_3N_4 coating was also prepared. One side of each piece, sample and control, was coated with a glass frit suspended in an amyl acetate binder as described below. Both pieces were then heated in air in an oven. These experiments, with a subjective appraisal of the results based on visual observation, are summarized below.

A. Molybdenum

Corning Pyroceram #45 frit

Si_3N_4 coated—sealed well; good glass-to-surface adhesion; metal oxide free

Uncoated—poor seal due to over-oxidation; metal chalky white and powdery

B. Copper

Owens Illinois #CV-102 frit

Si_3N_4 coated—good glass seal; metal free of oxidation

Uncoated—seal poor; metal highly oxidized, powdery

C. Tantalum

Owens Illinois #SG67 frit

Si_3N_4 coated—good seal; metal free of oxidation

Uncoated—metal severely oxidized to a chalky white powder

D. Kovar

Corning #7570 frit

Si_3N_4 coated—good seal; metal free of oxidation

Uncoated—seal fair; metal oxidized

E. Gold

Owens Illinois CV-102, frit

Si_3N_4 coated—good glass seal

Uncoated—glass would not seal to the gold

Fig. 2 shows a photomicrograph of an angle-lapped section of the molybdenum sample (A) coated with the divitrified Pyroceram #45 glass–ceramic. The silicon nitride layer, which can be discerned by the interference bands, faithfully follows the surface roughness contour of the metal and apparently does not chip loose during the lapping and polishing procedure.

Fig. 3 shows the reverse side of two molybdenum plates after the sealing operation. The uncoated control sample is covered with a thick scaling layer of molybdenum oxide, while the Si_3N_4-coated sample remains mechanically sound.

In order to evaluate this process in a useful structure, a tube-stem seal was made. This seal used 7 molybdenum pins 0.040 inch in diameter that were coated with Si_3N_4 using the process described. When the finished seal was leak tested, it showed no detectable helium leak at 10^{-8} Torr. Also, there was no evidence of oxidation of the molybdenum pins. A physically strong, leak-free butt seal was also made by sealing Corning #7052 glass tubing to a silicon-nitride-coated, ½-inch × O.D. × 1/32-inch-wall molybdenum tube using a standard glass-working lathe.

Conclusions

For many metals, the use of a silicon nitride intermediate layer in glass-to-metal seals appears to have several advantages over the use of

Fig. 2—Angle-lapped section of a molybdenum plate glassed with Pyroceram #45 frit (approx. 600×).

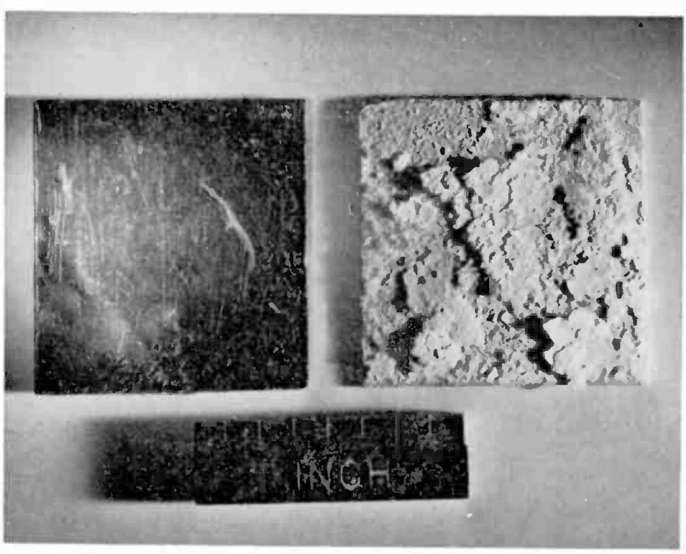

Fig. 3—Si_3N_4 coated side (left) and uncoated side (right) of molybdenum plate after sealing.

metal oxide layers.

1) Inert atmospheres are not required in the glassing step. Hence, even readily oxidizable metals can be sealed in a lathe or at the bench.
2) Less skill is required to make seals, since the operator would not have to be concerned with obtaining and retaining the proper type and thickness of oxide on the metal, as is now required in tungsten–glass seals for instance.
3) There is no adverse reaction of the glass with the metal or its oxide.
4) The composition of an alloy to be sealed to glass can be selected without regard to the nature or adherence of the oxide that it forms.
5) Gold, and presumably other nonoxidizable metals, can be sealed to glass.
6) In making vacuum-tube structures, the problem of oxidized parts in the tube arising from operations such as stem sealing, could be eliminated.
7) Metal parts could be degassed and silicon nitride coated in one furnace operation. Thereafter, they should be capable of being stored for long periods of time without readsorbing gas from the atmosphere.

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Frank Jerome Marlowe. Reduction of Turn-On Delay in Liquid Crystal Cell (3,503,-672)

Stuart Stanley Perlman and Bernard Goldstein, Method and Apparatus for Detecting Light by Capacitance Change Using Semiconductor Material With Depletion Layer (3,502,884)

Charles William Reno and Richard James Tarzaiski, Scanning Laser Obstruction Detection System Utilizing A Retroreflective Strip (3,500,063)

Roland Norman Rhodes and John Brewer Beck, Transistor Deflection Circuits (3,-502,935)

Martin Robert Royce, Soren Milton Thomsen, and Perry Neil Yocom, Process for Preparing Phosphor (3,502,590)

Peter Schiff, Switching Type Voltage and Current Regulator and Load Therefor (3,500,127)

George William Taylor, Display Apparatus (3,503,551)

Richard Earl Werner, Variable Frequency Oscillator with Constant Amplitude Output (3,500,246)

Herbert Claire Werner, Method for Glass to Glass Sealing Utilizing Softened and Rigid Circumferential Segments (3,503,727)

AUTHORS

James A. Amick received an A.B. in Chemistry from Princeton University in 1949. He spent a year as a predoctoral fellow at Brookhaven National Laboratory, Upton, Long Island, and returned to Princeton for an M.A. and Ph.D. in Physical Chemistry in 1951 and 1952, respectively. In 1953, after a postdoctoral year at Princeton, Dr. Amick joined RCA Laboratories in 1953, where his starting assignment was with the physical analysis group. In 1955 he began working on Electrofax, and in 1956-57 he spent a year at Laboratories, RCA, Ltd., in Zurich, Switzerland. On returning to Princeton, he was assigned to the Materials Research Laboratory where he engaged in research on the stabilization of semiconductor surfaces, and the epitaxial growth of semiconductor elements and III-V compounds. Late in 1963 he joined the Process Research and Development Laboratory, which subsequently was incorporated into the Process and Applied Materials Research Laboratory. Currently he is head of the Materials Processing Research Group, which devises new processing techniques for improved semiconductor devices, integrated circuits, and arrays.

Dr. Amick is a Fellow of the American Institute of Chemists and a member of the American Chemical Society, the Electrochemical Society, AAAS, and Sigma Xi. He is listed in Leaders in American Science.

Jules E. Benbenek attended Rider College, Rutgers University, and the Armed Forces Technical Schools. As an Officer in the U. S. Army Mr. Benbenek served as a specialist and consultant to the Glass Technology Department, Technical Services Unit, War Department Technical Staff. He joined RCA Laboratories in 1944 and is the Supervisor of the Glass Technology Department. Mr. Benbenek is a member of the American Scientific Glass Society, has served as Vice Chairman at several symposia, and presently is the National Chairman. He is the Technical Editor of **Fusion**, a trade journal, a Senior Member of the IEEE, and a member of the American Optical Society.

Edward J. Boleky received his BSEE (magna cum laude) from the University of Pennsylvania in 1966, and the MSE from Princeton University in 1968, specializing in semiconductor device physics. Mr. Boleky joined the staff of RCA Laboratories in June, 1966, and has engaged in research on CMOS decoders, MOS tetrodes, and UHF frequency synthesis. He is presently involved with the analysis, design and fabrication of high-speed digital integrated circuits.

Glenn W. Cullen received the B.S. degree in chemistry from the University of Cincinnati in 1953, and the Ph.D. degree in inorganic chemistry from the University of Illinois in 1956. During the following two years he served on the teaching staff and as a Group Supervisor in the Electronics Department of the U. S. Army Air Defense School (Surface to Air Missiles) at Ft. Bliss, Texas. On release from the Army in 1958 he joined the staff of RCA Laboratories, Princeton, N. J., and initially worked on the chemical stabilization of semiconductor surfaces. Subsequent to this work he was involved in the chemical vapor deposition of Nb_3Sn, Nb, Ta and Nb-Ta superconducting thin films. This activity included the characterization of the electrical properties of the deposits at low temperatures in high magnetic fields. For the past three years Dr. Cullen has been involved in the preparation and characterization of silicon thin films epitaxially deposited on insulating substrate materials. Dr. Cullen is the Head of the Materials Applied Synthesis Group within the Process and Materials Applied Research Laboratory.

Dr. Cullen is a member of the American Chemical Society, the Electrochemical Society, the Society of Sigma Xi, and Alpha Chi Sigma.

Michael T. Duffy received the B.Sc. degree from University College, Dublin, in 1958 and completed his Ph.D. studies in Solid State Chemistry in 1963. He was a teaching assistant at this University from 1961 to 1963. In 1964, he joined the University of Toronto as a Research Associate, engaged in molecular beam studies. In July 1966, he joined the staff of RCA Laboratories, Princeton, N. J. Since then, he has been engaged in materials research in the field of integrated electronics and particularly in the area of thin film dielectrics and MIS structures.

Nathan Feldstein attended The City College of New York where he received a Bachelor of Chemical Engineering degree. Following graduation, he was employed by Corning Glass Works in Corning, New York, as a development engineer in the Ceramic Division. While in the Army, he served as an instructor in the School of Chemical, Biological, and Radiological Warfare in the Panama Canal Zone. While pursuing graduate work in Physical Chemistry at New York University, Dr. Feldstein was a teaching fellow at the same school, and later a lecturer in the Department of Chemistry of Brooklyn College. He joined the staff of RCA Laboratories in January 1966. His research activity has been primarily concerned with research and development of electrolytic and electroless plating solutions for applications in the electronics industry.

Dr. Feldstein is a current member of A.C.S., E.C.S., A.E.S., Phi Lambda Upsilon, and Sigma Xi.

Kier M. Finlayson did his undergraduate training in physics at the Massachusetts Institute of Technology, receiving his degree in 1950, and did graduate work in physics at the University of Missouri. From 1958 to 1965, he was on the technical staff of the Research Laboratories, Corning Glass Works, where he was concerned with the precipitation of crystalline phases from glass systems. From 1965 to 1968, he was a staff member of the Columbus Laboratories Battelle Memorial Institute, where he contributed to sponsored research on the bonding and interaction between solids. In 1968, Mr. Finlayson joined the color product engineering laboratory of RCA Electronic Components, Lancaster, Pa., as an analytical physicist. He has responsibility for the application of x-ray and electron-beam analysis instrumentation to the characterization of materials for the development and manufacture of electron-tube devices. Mr. Finlayson is a member of the American Crystallographic Association and the Electron Probe Society of America.

Alvin Malcolm Goodman was born in 1930 in Philadelphia, Pa. He attended the Drexel Institute of Technology, Philadelphia, Pa., and received a B.S.E. in 1952. He did graduate work at Princeton University, receiving an M.A. in 1955 and a Ph.D. in 1958. From June 1956 to January 1957 he served as Research Assistant at Princeton University, and then as Assistant Professor of Electrical Engineering at the Case Institute of Technology up to June 1959. He performed research at RCA Laboratories as a summer employee in 1954, 1955, and 1958. He has been a Member of the Technical Staff since June 1959. Dr. Goodman has specialized in solid-state physics. His thesis subject was "Dember Effect and Trap Levels in Silver Chloride". He is a member of the American Physical Society, Sigmi Xi and the Institute of Electrical and Electronics Engineers, and is listed in American Men of Science.

G. Eugene Gottlieb received the B.S. degree in chemistry from Rutgers University in 1956, the M.S. degree in physical chemistry from Temple University in 1958, the M.B.A. degree from Rutgers University in 1964, and is currently completing his thesis for a Ph.D. in ceramics from Rutgers University. From 1958 to 1960, he was associated with the Philco Corporation, working on the selection, preparation, and evaluation of thermoelectric materials. In 1960 he joined RCA Laboratories, where he has been engaged in vapor phase transport of III-V semiconductors, single crystal growth of electro-optic materials from the vapor phase, and the synthesis and crystal growth of organic semiconductors. For the past four years Mr. Gottlieb has concentrated on the epitaxial growth of silicon films on insulating substrates.

Mr. Gottlieb is a member of the American Chemical Society, American Ceramic Society, Keramos, The Electrochemical Society, and is listed in American Men of Science.

Werner Kern received a certificate in chemistry in 1944 from the University of Basle, Switzerland, and a diploma in chemical technology in 1946. He published a thesis on the chromatographic isolation and characterization of fluorescing polynuclear hydrocarbons which he discovered in soil. He was analytical research chemist with Hoffmann-LaRoche in Switzerland, and in 1948 transferred to their research division in New Jersey specializing in developing radiochemical and microanalytical methods. In 1955 he received an AB degree in chemistry from Rutgers University. In 1958 he joined Nuclear Corporation of America where he became chief chemist directing research in nuclear and radiation chemistry. He joined RCA Electronic Components and Devices Division in 1959 to conduct radiochemical investigations devoted mainly to the study of semiconductor surface contamination. Since 1964 he has been at RCA Laboratories as Member of the Technical Staff, where his activity has centered in semiconductor process research in the areas of solid-state device passivation, new methods of chemical vapor deposition of oxide and glass films, and the development of analytical methods for controlling these processes.

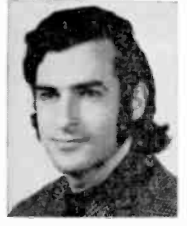
Mr. Kern is a member of the American Chemical Society, the Electrochemical Society, the Society of Sigma Xi, the Geological Society of New Jersey, and is listed in American Men in Science.

Thomas S. Lancsek attended Moravian College in Bethlehem, Pennsylvania, where he received a B.S. in Chemistry in 1969. He joined RCA Laboratories in June 1969 and has been primarily involved with research and development of electrolytic and electroless plating solutions for applications in the electronics industry.

Alfred Mayer received his B.Sc. from London University and was elected a Fellow of the Royal Institute of Chemistry in 1951. After working as a research chemist at the British Cast Iron Research Association and Magnesium Electron Ltd. in England on analytical methods of extraction metallurgy, he joined Quebec Metallurgical Industries in Ottawa. Here he led a group that succeeded in developing new processes for the extraction of niobium and tantalum from ores, their separation and reduction to metals. Mr. Mayer joined RCA Solid-State Div., Somerville in 1959, and became an Engineering Leader in 1961. He worked on the purification of gallium, synthesis of gallium arsenide, epitaxy, and the construction of high-temperature rectifiers. For the last few years, his group has worked on basic silicon device technology and process control techniques. This has led to advances in silicon surface preparation, clean oxidation, handling, and testing of dielectric films, deposition of doped oxides, and measurements of material and device properties and contacting methods. Mr. Mayer is a member of the Electrochemical Society and the Royal Institute of Chemistry.

Frank B. Micheletti received his B.S. in Electrical Engineering, with Highest Distinction, from Purdue University in 1963. From 1963 to 1965, he attended Princeton University, receiving his M.S. in 1965. During the same period, he was a member of the staff of RCA Laboratories on the Research Training Program working in the area of magnetic memories, epitaxial deposition of germanium thin films, and chemically-deposited CdS thin films. Following a year of full time study at Princeton on an NSF Fellowship, he returned to RCA to complete his doctoral dissertation. He received the degree of Ph.D. in Electrical Engineering in 1968 from Princeton University. His thesis research was concerned with the effects of chemisorbed oxygen on the photoelectronic properties of polycrystalline CdS films.

At present, Dr. Micheletti is engaged in research on silicon-aluminum oxide MIS devices and technology. A joint effort with Dr. Karl Zaininger and Peter Norris, also of RCA Laboratories, has recently established that this technology can result in a significant hardening of MOS devices in a radiation environment.



Peter E. Norris received his B.S. in electrical engineering from MIT in 1965. From 1965 to 1967 he attended graduate school at MIT receiving both the M.S. and Engineer's degrees in 1967. During this period he was a member of the Laboratory for Insulation Research, working in the area of high resistivity semiconductors. In 1967 he attended the University of Colorado before joining RCA Laboratories in 1968. As a member of the Research Training Program at the Laboratories, he worked on large screen television displays, photochromics, and radiation damage in MOS devices. At present he is with the Solid State Device Technology Group engaged in research on improved insulation for IC technology.

John J. O'Neill, Jr. joined RCA Laboratories, Princeton, New Jersey in 1956. From 1956 to 1962 he worked on the synthesis of III-V compounds. In 1962 he transferred to the Energy Conversion Group at Princeton and was engaged principally in the development of polycrystalline GaAs solar cells. Mr. O'Neill is presently with the Process Research and Development Laboratory where he is working on r-f sputtering. Mr. O'Neill is currently attending Rutgers University, New Brunswick, N. J.

Stephen T. Opresko received a B.S. degree in chemistry from the Allentown College of St. Francis de Salles, Center Valley, Pennsylvania in 1969. During the summer of 1968, Mr. Opresko was employed at the Atlas Chemical Company, where he worked on detonators and explosive initiators, developed a rust removal solution, and assisted in the design of a novel explosive operated valve. Upon graduation from college, Mr. Opresko joined the RCA Laboratories as a Research Associate. His initial assignment was in the Process and Materials Applied Research Laboratory, where he worked on processes used in fabricating dielectrically isolated silicon arrays. In this work, he developed a new etching system for chemically thinning and polishing silicon. At present, Mr. Opresko is associated with the Materials Research Laboratory, where he is engaged in research on crystal growth from a melt and on chemical vapor transport methods related to the vapor-phase growth of single crystals.

David Puotinen received an S. B. degree from MIT in 1959. Until September 1962, he was a research staff member of the Energy Conversion and Semiconductor Laboratory at MIT working on crystal growth and the galvanomagnetic properties of chalcognides. Since that time he has been with the Electronic Components Division of RCA Corporation working initially on the fabrication and parametric analysis of thermoelectric devices and high temperature metallurgy. More recently, he has been active in all phases of semiconductor materials and process technology, including doped oxide diffusions, COS/MOS technology, and the development of instrumentation and measurement techniques.

Mr. Puotinen is a registered Professional Engineer and a member of the American Chemical Society, the Electrochemical Society and the Institute of Electrical Engineers.

George A. Riley received a B.S. in Physics from Providence College and an M.S. in Physics from Cornell University. He joined the RCA Service Company on the BMEWS project in 1960. He transferred to RCA Laboratories in 1964, working in the Electronics Research Laboratory and The Process Research Laboratory. He is presently Administrator, Advanced Systems Planning, at the RCA Graphic Systems Division, Dayton, N. J.

Edward C. Ross received the BSEE degree from Drexel Institute of Technology in 1964 and the MSE, MA, and Ph.D. degrees from Princeton University in 1966, 1967 and 1969, respectively. He joined RCA Laboratories in 1964, where he has been working in the fields of integrated arrays of MOS field-effect transistors, the electrical and physical characteristics of silicon-on-sapphire films, and the physics and application of field-effect storage transistors.

Dr. Ross is a member of Tau Beta Pi, Eta Kappa Nu, and the Institute of Electrical and Electronics Engineers.

Laurence Royer attended Albright and Franklin and Marshall Colleges and is now enrolled in an RCA Institutes Electronics program. He has been with RCA for over four years. More than two years were spent in the Conversion Tube operation associated with the manufacture of image orthicons. The remainder of his time has been occupied specifically by electron microprobe analysis in the laboratory at Lancaster. Prior to his association with RCA, he was employed by Armstrong Cork Company, and worked at their Research and Development Center Analytical Laboratory for six years.

William H. Schilp, Jr. received his B.S. in Physics from St. Peter's College, in 1962. Concurrently he was employed at Electro-Tec Corporation, East Caldwell, N. J., where he was responsible for analysis of plating solutions and plating quality control. Upon receiving his degree, he joined the Isomet Corporation, Palisades Park, N. J., as a junior scientist concerned with oxygen regeneration systems for manned satellites. From 1962 to 1964, he served in the U.S. Army as an ordnance supply officer. In 1964, he joined the Process Research and Development Laboratory of RCA Laboratories, where he is engaged in semiconductor process research, in particular on techniques for providing dielectric isolation in integrated circuits. In March 1969, he joined the RCA Solid-State Division at Somerville, N. J. He is presently pursuing an M.S. degree in physics at Fairleigh Dickinson University.

William Shannon received the B. S. degree in Physics from Florida State University in 1968. As an undergraduate, he worked with both the Radio Astronomy and Solid State Research groups. His responsibilities included research into the electromagnetic phenomena of the planet Jupiter, the Faraday rotation of the earth, and the measurement and analysis of magnetic susceptibilities. In 1968, Mr. Shannon joined RCA Solid-State Division, Somerville, N. J., where he has been actively involved in the development of measurement techniques for silicon and gallium arsenide devices. These included measurement of epitaxial layer resistivity and diffusion profiles from differentials capacitance and diode harmonic analysis. Mr. Shannon is presently involved in the development of silicon ingot evaluation techniques, and dielectric defect detection methods for in-process control of device parameters. He is actively involved with the ASTM, and is presently doing graduate work at Newark College of Engineering.

Joseph M. Shaw attended Seton Hall University where he received his B.S. in Physics in 1963. He is currently doing graduate work in Metallurgy at the University of Pennsylvania. After his discharge from the U.S. Navy in 1955, he was employed by the E. I. Dupont Company, in Newark, New Jersey, as a member of the Physical Chemistry Laboratory of the Pigments Department, where he was engaged in the physical characterization of organic pigments and later in the development of flake pigments produced by chemical vapor deposition of metals and oxide films. In 1964 he joined the Process Research and Development Laboratory of RCA Laboratories, Princeton, N. J., working on the application of vapor deposition techniques in the metallization of semiconductor materials. He is presently associated with the Process and Materials Applied Research Laboratory, where he is engaged in research and techniques relating to the vapor growth of insulators and oxides on MOS devices.

Robert R. Speers received a B. Sci. degree in Physics from the University of Michigan in 1961. He received the M. Sci. degree in 1963 and the Ph. D. degree in 1966, both in Elec. Eng. from the Ohio State University. His masters work concerned an experimental investigation of the initiation of electrical breakdown across vacuum gaps. He specialized in solid state electronics for his doctoral work, with particular emphasis on the effects of nuclear radiation on solid state devices. From 1964 to 1966, Dr. Speers was employed half-time by Phylatron Corp., Columbus, Ohio. During this time he helped develop a GaAs diode cryogenic thermometer and experimentally and theoretically investigated the neutron energy dependence (0.5-22Mev) of the damage constant of a p-i-n silicon fast neutron dosimeter (1-1500 rads). The latter study was the basis of his Ph. D. dissertation. Dr. Speers joined the Conversion Devices Laboratory, an Affiliated Laboratory of the David Sarnoff Research Center, in the Autumn of 1966. From 1966 to 1967, he investigated the properties of photoconductors and photoconductor–electron–beam interactions in vidicon imaging tubes. Since 1967, he has been investigating and developing infrared sensitive integrated-circuit imaging arrays. In 1969 he joined RCA Laboratories where he has continued this research.

Dr. Speers is a Member of Sigma Xi, IEEE, and the American Physical Society.

Arthur I. Stoller received a B.S. degree in Ceramics in 1953 from Rutgers University, where he was elected to Keramos, the Honorary Ceramic Engineering Society. He received an M.S. in Electrical Engineering at Rutgers in 1969. He served as a Signal Corps officer from 1953 to 1955. He joined RCA Laboratories in 1955, working on magnetic materials and devices for several years. In 1963 Mr. Stoller joined the Process Research and Development Laboratory, where he has been working in the research and development of semiconductor processes and he has done extensive research on the development of new integrated-circuit isolation techniques. Mr. Stoller is a member of Sigma Psi.

J. L. Vossen joined RCA in 1958 after receiving a B.S. in physics from St. Joseph's College. He was first associated with the Microelectronics Department of the RCA Solid-State Division in Somerville, N. J. There, his work centered on thick- and thin-film passive component processes. In 1962, Mr. Vossen transferred to the Advanced Communications Laboratory of the Defense Communications Systems Division in New York City, where he led a group conducting research on precision thin film resistors and capacitors. In 1965 he joined the Process Research and Development Laboratory of the RCA Laboratories in Princeton, N. J., where he has been engaged in research on sputtering processes and other physical methods of film deposition.

Mr. Vossen is a member of the American Physical Society, the American Vacuum Society, the Electrochemical Society and Sigma Xi.

Chih-Chun Wang received his B.S. degree in Chemical Engineering in 1955 from the National Taiwan University, Taiwan, China, his M.S. degree at Kansas State University in 1959, and his Ph.D. degree in Physical Chemistry in 1962 from Colorado State University. From 1962 to 1963 he received the postdoctoral training in high temperature physical chemistry research group of the University of Kansas. In 1963 Dr. Wang joined the research staff of RCA Laboratories where he has been engaged in research on synthesis and characterization of electronic materials, including wide-bandgap III-V semiconductors, ferromagnetic transition metal oxides, refractory dielectrics, and thin films. Dr. Wang has specialized in crystal growth and vapor-phase deposition of electronic materials, thermodynamics and kinetics of high temperature systems, x-ray crystallography, and mass spectrometry.

Dr. Wang is a member of the American Chemical Society, Electrochemical Society, Sigmi Xi, Sigma Pi Sigma, and Phi Lambda Upsilon. He is listed in American Men of Science, Leading Men in the United States of America, and International Biography of Contemporary Achievement.

Karl H. Zaininger received the BEE degree (magna cum laude) from City College of New York in 1959; the MSE in 1961, the MA in 1962, and the Ph.D. in Engineering Physics in 1964 from Princeton University. In 1959, Dr. Zaininger joined the staff of RCA Laboratories. At RCA, he worked in research on various semiconductor devices, and has been involved in research on silicon-based MOS devices since their original inception. His research activities with the MOS devices have included basic studies in the area of semiconductor surface physics. He is presently concerned with MIS device physics and technology, with measurement techniques, and with the physics of radiation damage in MIS systems. In August 1968, Dr. Zaininger was appointed Head of the Solid-State Device Technology group at RCA Laboratories.

Dr. Zaininger is a Senior Member of the Institute of Electrical and Electronics Engineers, and a member of Tau Beta Pi, Eta Kappa Nu, Sigma Xi, and the Shevchenko Scientific Society.