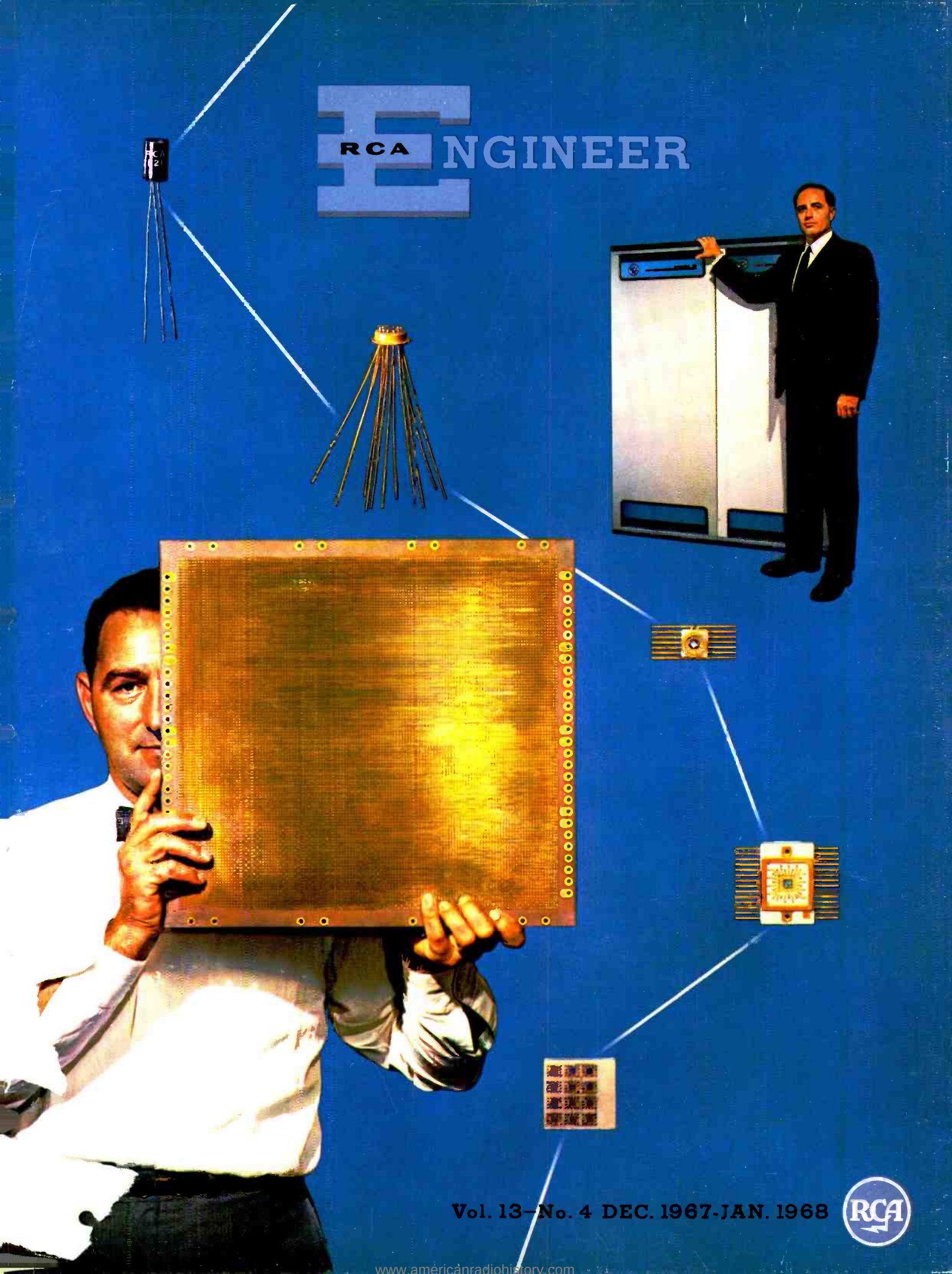
RCA ENGINEER



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RCA

OUR COVER

The interconnection platter being held by John Surina of DEP Advanced Technology demonstrates the dramatic improvements achievable with today's packaging technology; a platter of this size could contain the circuits and interconnections necessary to perform the same function as the latest Spectra 70/45 processor occupying the two cabinets shown next to Bert Walker, also of Advanced Technology. An important companion to the improvement in packaging is the continuing advance in device technology: less than a decade ago, the transistor (upper left) started a new era of packaging; soon, multiple-circuit arrays (lower right) will contain hundreds of transistors as well as several hundred passive components.

Computer Technology

RCA is immersed in the third generation of computer technology and is planning for the fourth generation. The transition to arrays from integrated circuits is similar in nature to the transition to integrated circuits from transistors. Technical decisions at every design level must continue to be made with full awareness of system architecture, software capability, interconnection philosophy, maintenance and test philosophy, and device performance. The degree of transition, however, is extreme. Firm discipline must be maintained throughout the design cycle, since the design will be transformed into relatively immutable semiconductor and multilayer boards. ECN's will be very expensive in dollars and time.

Computer design aids will be an absolute necessity for the fourth generation. The large number of functions on an array and the great number of possible states of the array demand large scale computer simulation for complete exploration of the design —computer breadboarding. The method for testing the array must be considered not only in the array design, but in the logic partitioning. Design decisions must be committed to the computer to permit error detection and automatic generation of array and interconnection artwork.

RCA has been doing its homework for the fourth generation—in semiconductor technology, advanced interconnection techniques, computer aided design and logic simulation, automated routing and artwork generation, and machine organization. Much more remains to be done, however, and the existing capabilities of several divisions of RCA must be successfully integrated to achieve winning strength. You can help this integration process by increasing your awareness of the role and contribution of companion organizations and disciplines. You can make a good start by reading the articles in this issue of the ENGINEER.

D J Parker

D. J. Parker, Manager, Advanced Technology, Defense Engineering, Defense Electronic Products

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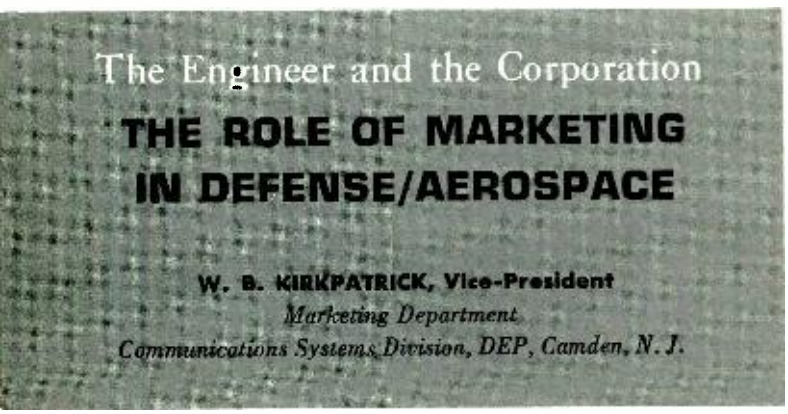
CONTENTS

A TECHNICAL JOURNAL PUBLISHED BY **RADIO CORPORATION OF AMERICA,** PRODUCT ENGINEERING 2-8, CAMDEN, N. J.

● To disseminate to RCA engineers technical information of professional value. ● To publish in an appropriate manner important technical developments at RCA, and the role of the engineer. ● To serve as a medium of interchange of technical information between various groups at RCA. ● To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions. ● To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field. ● To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management. ● To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

RCA ENGINEER articles are indexed annually in the April-May Issue and in the "Index to RCA Technical Papers."

Because the defense/aerospace market is a technical one, engineering is central; it is a business in which planning is paramount—and that is marketing's function—linking the business with the customer. Defense/aerospace and commercial marketing organizations contrast sharply both in major objectives and in commitments. This paper describes the planning necessary for a successful marketing function and covers the interfaces between the customer's buying agencies and the contractor's engineering function with special attention to marketing's role in this interface.



W. B. KIRKPATRICK, Vice-President
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In industries other than defense/aerospace, the marketing function is a fundamental management responsibility about which the business is focused. In civilian and commercial industries, marketing personnel analyze markets, develop statements of customer requirements, specify products to fill those requirements, participate in (or direct) the styling of that product, and promote its sale. In broad terms, the marketing organization represents both a translation function and a distribution function. To perform the translation function, marketing synthesizes a market requirement—sometimes even before the customer is aware of his need—and translates it into a product specification for the benefit of the engineering and manufacturing. As a distribution function, marketing identifies and cultivates customers that buy the output of the factory at a profit to the company.

In this non-government marketplace and in these days of highly developed manufacturing technology, a keen marketing sense is crucial to management. Each market has its own peculiar requirements which must be understood fully by executive management.

On the other hand, executive management's understanding of the engineering and production functions is less crucial. Within the range of their product area, engineering can develop and manufacturing can build almost any product; engineering and production uncertainties usually can be reduced to a financial risk within comparatively narrow limits. However, the marketing risk—*Has the proper product been specified?*—is not definable within such narrow limits. For example, different automobiles, even though very similar, sell at wildly different rates. Production will be increased heavily on some models and other manufacturers will attempt to duplicate those models; another model that does not sell may be dropped from production. In both cases—the model with high volume sales and the model that was discontinued—engineering and manufacturing presumably did their job, since both models functioned relatively equally. The critical difference in the two cases is attributable to the depth and accuracy of the market research and the product specifications.

Final manuscript received October 11, 1966.

SOME DEFENSE/AEROSPACE MARKETING LIMITATIONS

In the defense/aerospace industry, a large part of the traditional marketing role is played by the buying agencies. Agencies such as the Army Electronics Command, the Air Force Systems Command, the Bureau of Naval Weapons, and the Manned Spacecraft Center, analyze the "market" and develop statements of customer's requirements, specify products to fill those requirements, and promote their sale by getting procurement approval from headquarters. Industry may supplement some of these functions in certain respects, such as aiding in the developing of customer requirements or specifying products, but it is always done as a supporting function to the buying agency. The decision is never the contractor's; it is always retained by the government.

Marketing often assists the customer in identifying products, and even may canvass customers (buying agencies) to determine market potential for new developments, but this should not obscure the fact that Marketing does not have the power of decision in developing statements of customer requirements, of specifying products to fill those requirements, nor of promoting their sale. Defense/aerospace industry marketing organizations can translate to engineering and manufacturing the projected needs of the customer. They can use their resources and insight to determine which of a wealth of competing programs to pursue. But they cannot formally specify what engineering will develop nor what manufacturing will build, nor what the customer will use — these are all buying agency functions.

RESPONSE OF DEFENSE/AEROSPACE MARKETING

To counterbalance the large technical risks that industry must take to compete in the defense/aerospace market, firm contracts are required by government contractors before large commitments are made. This effect is exactly opposite to that in non-government businesses where the technical risk is more under control, but the business risk is great. These companies risk large commitments of their resources in the firm expectation that buyers will be waiting when the products come off the assembly lines. In doing business with the government, however, contractors demand that their buyer make the major financial commitment before the work is started. The pre-proposal funds spent by a defense contractor in competing for an award, although significant, are never of the magnitude of those required in purely civilian industry to launch an entirely new product line, such as a color TV or a compact automobile. The major risk in the defense/aerospace industry is a technical one: *Can a contractor build what he claims within the price and budget he defines?* In contracting with the government, each contract must stand or fall on its own merits; one cannot assume that further orders will be available over which to amortize tooling or engineering, or to adjust price and value. In the civilian market, however, all these alternatives are open so that mistakes or miscalculations can be corrected. In both cases, the risk is carefully considered, but in the defense/aerospace industry, technology and technical management are, in general, the limiting factors — not the depth and accuracy of the market analysis.

Just because the contractor cannot directly specify the product he hopes to develop and build does not mean he is without power to affect its specifications. When the requirement is first defined by the using agency, the contractor is encouraged to contribute technical ideas on equipment that can fill the requirement. A specification is then prepared by the buying agency that reflects the best ideas of industry and the laboratories of the buying agency. To the degree that the contractor's ideas represent the most valid means of solv-

ing the problem, he is the "favored" bidder (i.e., he understands the problem and has a solution that fits the specification). The most successful way of affecting the specification is to get the technical experts from the contractor's engineering organization to meet with the customer's technical experts. In this way, the contractor's people may get a clear technical understanding of the customer's problems. The contractor's engineers can apply their broadly based technical knowledge to the specific requirement and postulate feasible alternatives. The technical story that results should include not only an accurate statement of the technical objectives and the functional requirements for the product, but should also contain an accurate estimate of the customer's technical preference and motivations. Ideally, the story should be complete to the level of 1) what is the customer's technical staff working towards, 2) how can the contractor's proposed product help advance the customer's people to their goal, and 3) how can the proposed product completely reflect the customer's needs? In other words, how can the contractor's people make themselves essential to the customer's success? This role of technical interfacing, although set-up by marketing, is definitely an engineering function. If this role is performed only by marketing people, there is a natural biasing of the facts to both the customer and to engineering that can be disastrous at worst and time-wasting at best. When a man has no easily definable product to sell, he is likely to over-represent the engineering forces he sells, on the one hand, and under-represent the difficulty of the design task to engineering on the other. Marketing's role in selling an engineering effort is interfacing and selecting — to bring together the customer (with his requirements) and the engineer (with his technology) on programs that have a high probability of reaching operational status.

Simultaneously, the contractor's marketing personnel can meet with the customer's organization. Marketing should be getting an accurate idea of the funds available for the product, where the product stands in the government programming cycle, and, to the extent possible, determine if the product is potentially an APOLLO or a DYNA-SOAR, a MINUTEMAN or a SKYBOLT.

These are the marketing roles: 1) the selection of high-potential programs, and 2) the collection, integration, and definition of the interface, business, financial, and management climates of these programs. Marketing then can develop the profile of the product to present to engineering and manufacturing; the decision is then theirs whether they can or cannot economically meet the requirements. But it is a marketing function to develop the product profile — the definition of the winning bid. The "homework" cycle continues and inputs are refined, but the critical effort is in fully comprehending the customer's total needs and in molding the response to fit. This period is one of interaction, for the customer can, in some ways, mold his specification of the requirements to include special features or techniques that he feels offer potential advantages to the user. The astute contractor should try to convince his customer to include feasible requirements of this kind so as to enhance his chances of winning.

The product specification is not constrained by the capabilities of a particular engineering organization — the buying agency can select or specify the engineering organization best qualified for each development job. Hence, the product specifications need not be conservative, nor even realistic; the penalty of failure lies primarily upon the industry engineering organization, not upon those within the buying agency who may too rigidly or inadequately specify the product. In the event of an unsuccessful development, the buying agency suffers a penalty also, but it is a second-order effect only — one that takes place only after the industry engineering organization has exhausted a considerable amount of its own resources. In a non-government industry, the marketing group who specifies a product has a real stake in the success of its development within cost and schedule because they are organizationally and financially bound to their own engineering organization: failure of a product development leads directly to failure of those who specified the product. This immediate check and balance effect simply does not operate in the government market. At best, in the defense/aerospace market, the contractor, through his marketing organization, must make an astute choice of which programs to pursue. To an equal extent, engineering and production organizations must be accurate in projecting the schedules and budgets they can meet.

Additionally, the cost of engineering is traditionally a loading applied to products in production. A fortuitously selected product specification results in high production, thus multiplying the opportunities for profit while reducing the cost of engineering per unit produced. In the defense/aerospace industry, however, engineering and production are often separated, each is funded individually, and successive production orders are not only funded individually, they may also be placed in different manufacturing facilities.

PRODUCT PLANNING

The setting of the business perspective and the definition of its goals are the objectives of planning. The formal plans are regularly of two types: operating plans (short-range plans and long-range plans); and product-line plans.

Operating Plans

Operating plans are the overall business plan and budget that detail the expected operating expenses and income and show the measure of success (return on assets, profit after taxes, etc.) that the operating unit expects to achieve for the time period involved. These are prepared by integrating the budgets prepared by each operating unit and are the final product of the financial units of the organization.

WILLIAM B. KIRKPATRICK received the BS degree in Electrical Engineering from the University of Pennsylvania in 1942. From 1942 to 1946, Mr. Kirkpatrick served with the U.S. Army Signal Corps and Air Force. With the Air Force, he was a Project Officer responsible for the design, development, and testing of airborne radar equipment at Wright Field, Ohio. Following his discharge from military service with the rank of Major, he joined Curtiss-Wright Corporation. Mr. Kirkpatrick was appointed Division Vice President, Marketing Department, Communications Systems Division, on August 1, 1966, with responsibility for all marketing activities, including planning, new market development, sales, contract negotiations, and administration for the division. Previously, Mr. Kirkpatrick had been Marketing Manager of RCA's Communications Systems Division, and prior to that he was Manager of Business Planning for the division. Earlier, he had been Manager of RCA's Defense Marketing for Air Force and National Aeronautics and Space Administration programs, and had held various other managerial and marketing positions since joining RCA in 1947.

W. B. Kirkpatrick conducts staff meeting. Clockwise are: J. C. Donofrio, F. H. Stetler, Jr., J. L. Owings, W. B. Kirkpatrick, J. C. Belanger, R. McGough, C. L. Dodd and T. D. Finley.

The short-range plan, or operating plan for the year, is based on the total sales forecasts from the product-line plans and is an amalgamation and reconciliation of the program plans for each product or contract, the new technology or independent research and development plan, the marketing or project analysis plan, and the planned allocation of overhead and administrative resources. The utility of the operating plan for the year is directly related to how well it is followed. Since the corporation depends on the ability of each independent operating unit to meet its commitment, the problem facing operational management is to attain the objectives of the plan.

The long-range plan is similar in structure and content to the short-range plan, except that it projects over a longer time span; consequently, it becomes less quantitative with time. Although it is less exact than the one-year plan it is by no means less important; this plan sets the basic structure of the business for the future by defining goals in terms of business objectives: e.g., profit and return on assets. Its value and accuracy are directly related to the quality of the product-line plans upon which it is based.

It is important to understand the utility of these plans. Long-range planning is sometimes misunderstood; it does not deal directly with future decisions (a future decision can only be a postponed decision which in itself is a current decision). It deals with the impact on the future of present decisions. It is concerned with what has to be done now so that the future can be met with success. Important decisions permanently and irrevocably set the course of events for the future. The pertinent questions that long-range planning tries to answer are:

1) What considerations (facilities, technology, access to talent, economic conditions, etc.) of the future must be worked with today?
2) What time-cycles are important?
3) What effect do these have on a decision today?

Product-Line Plan

The product-line plan is a multi-year plan for the market area that purchases that product-line. Based upon the customer and his needs, it defines the product he will buy. The product-line plan is market-oriented and views the product as a function of the market; in this way it differs totally from the operating plan which is company-oriented and views the business as a function of the products being sold. Because of this essential difference in outlook, the product-line plan is a primary marketing responsibility. The product-line plan combines elements of both long-range and short-range planning. It is directly related to the operating plan for the year and is based upon market projections for each product-line. These market projections represent an attempt to forecast the probable dimensions of a particular market: Who will buy how much of what kind of product and for how long? The purpose of the forecasting is to set up a range of probabilities that reasonably describe what is likely to occur; however, forecasting is used to isolate constraints that limit one's opportunities in the future. Once these are identified, work (planning) can be directed at reducing those constraints through development of new techniques, application of advanced technology, introduction of new concepts, etc. The product-line plan is largely based on a series of discrete opportunities: the contracts awarded by the government. Each milestone is marked by the success or failure of a technical proposal, and each success or failure redirects or constrains the product-line plan.

THE PROPOSAL

The operating plans and product-line plans are common to both defense/aerospace and commercial marketing; there is, however, one other type of plan that is imposed mainly by the defense market, and it is peculiarly a marketing document — the proposal. Proposals, particularly those for major procurements, are complete plans — technical, management, production, facility, personnel, fiscal, etc. — for the conduct of a program which has been carefully and distinctively defined by the buying agencies. It encompasses every activity that will be applied to a program and details exactly how each job will be done and how contingencies will be handled. The product that is finally bought in production quantities is the physical embodiment that results from the series of detailed plans, that began with the advanced technology proposals, that led to the development proposal, that in turn led to the first production-quantity proposal, that ultimately led to the volume manufacturing quote. It is through these plans that executive management guides the company to new business opportunities.

When marketing begins to develop a customer who is working towards the specification of a product, it is done within the confines of the long-range, short range, and product-line plans. If the potential product does not fit within the range of planned activities, it is determined whether 1) the plan should be changed or 2) the interest in the potential product should cease. The formalized review of these factors usually occurs during a pre-bid review or bid-review meeting. The questions that must be applied to render a bid/no-bid decision are: 1) *Is it a job the company needs to win?* 2) *Is it a job the company can win?* Both questions with all their implications must be answered affirmatively in order to bid.

After the bid decision, the collection of information continues in accord with the goals of the planning and the proposal. As these formal plans — long-range, short-range, and product line — are refined and detailed to reflect the various customers' needs and their specific requirements, the natural results are the detailed business plan — a series of proposals in each product area. As specific jobs are won or lost, the areas of feasible action for the future are further constrained. This information is used to modify the plans and represent the feedback loop that makes planning self-correcting. When marketing is engaged in this product and business planning, it is acting in its highest capacity as an arm of executive management.

Marketing's efforts culminate with the proposal — it is the central marketing document. Although engineering, in fact, usually writes the bulk of the proposal, the guidance and direction of the overall effort is a marketing function. (As discussed previously, the *marketing function* is not restricted to the *Marketing Department.*)

CONCLUSIONS

Marketing's role in defense/aerospace industry is to develop a product profile and business and management plan that responds to the customer's total requirement. (The customer's total requirement encompasses more than is contained in the formal bid package.) The plan must be developed in consonance with the contractor's one-year plan, five-year plan, and product-line plan. At key milestones during its development, it should be reviewed with executive-level management for their concurrence or redirection.

A SURVEY OF THE LAST DECADE OF COMPUTER DEVELOPMENT

In the last ten years, the computer industry has seen two generations of computers. Initiated by the transistor and improvements in memory devices, computers have become dramatically faster and more powerful. Developments in machine organization, the use of time sharing, and the introduction of microprogramming have served to reinforce these hardware developments. With large-scale integration now becoming a reality, large (capacity) computers using monolithic integrated circuit arrays of hundreds of logic gates will provide our next generation.

SAUL LEVY
Data Processing Research
RCA Laboratories, Princeton, N. J.

THIS SURVEY covers the period from about 1957 to the present; an excellent survey of the period up to that time is contained in Bauer.[1] The paper by Bauer is a reasonably thorough discussion of the development and the state of the computer art up to the time of the introduction of the first transistorized computers and represents an accurate view of the computer world as it appeared to a knowledgeable observer in 1957. However, since Bauer addresses himself to large-scale systems, he neglects to mention such important (historically) machines as the IBM-650[2] which was the first really production-type model of a full-sized computer. It was first introduced in 1954, and at its peak, there were well over 2,000 installations.

HARDWARE DEVELOPMENTS

Transistors

The first major change in hardware in the period since Bauer's report was the introduction of the transistor. It was a great boon to the computing field for three main reasons:

1) It required much less power than the vacuum tube;
2) It was physically much smaller in size, and
3) It was a considerably longer-lived device.

These three factors, combined in various proportion, made possible the existence of far more powerful computers (many more logic elements) than could ever have been possible with the vacuum-tube technology. There was, of course, progress in transistors as circuits were made faster, but during the period in which the discrete transistor circuit was the mainstay of the computer logic (a period of only about six years 1960 to 1966) most of the improvements in computer performance were due to improvements in memory — magnetic core memory in particular.

Memory Devices

Core memories became larger (10^6-bit memories were standard for any moderately large computer installation and some of the larger installations included 10^7 bits). Speeds increased to where cycle times approaching 1 μs were common, and through the use of interleaving of independent banks of memory, effective cycle times measured in hundreds of nanoseconds were realized. The core memory has proved a remarkably durable device. It was first introduced into the computer in the early to mid 1950's and has remained the major memory device from that time to the present. Only in the current generation of machines (and only in a small number of machines) is there any suggestion of a replacement for the core.

Univac, in its 9000 series machines[3] is including a plated wire memory which can operate in the non-destructive read mode at 600-ns cycle time, Burroughs has a 500-ns flat-film memory for its super-large 8500 system, and IBM has taken orders for the 360/95[5]—a super high speed computer with magnetic-film main memory which operates at 125-ns cycle time. However, at the date of this writing (June 1967) no one has yet delivered such a device to a customer. At present, core memories which operate at 750 to 850 ns are common and CDC has demonstrated full scale core memories operating at 250 ns. It would appear, however, that the discrete core memory has seen its peak as a main memory.

Logic Elements

In third generation computers, integrated circuits have become the standard logic device (monolithic circuits for most manufacturers—hybrid circuits for IBM) and logical speeds have started to increase markedly: circuits with pair delays of under 5 ns are commonly available from semiconductor manufacturers and are beginning to appear in machines. Within the next few years, large-scale integrated arrays of gates (100 to 300 on a single wafer) will become commonplace, and at that time and for the same reasons, the integrated array will be as much an improvement over the discrete transistor as the transistor was over the vacuum tube. The RCA LIMAC[6] computer will be one of the first computers constructed from the new LSI technology and should contribute a great deal to RCA's standing as an innovator in the computer world.

Scratchpad Memories

In the 1960's the scratchpad memory, which is a small auxiliary memory operating about an order of magnitude faster than main memory speed, became quite common. At first, these were small core memories which could be made very fast because of their size — they have been replaced by small flat-film memories in some machines and by arrays of transistor registers in others. The scratchpad seems an ideal place to introduce LSI; in the SDS Σ-7 machine the memory is built from integrated arrays containing eight bits of transistor flip-flop storage.[7] Since this is such an obvious area to apply the large arrays, fully integrated solid-state scratchpad memories will probably appear before 1970 and will surely be a standard feature of the next generation of computer.

Another argument for using solid-state devices rather than magnetics for scratchpad memories stems from the requirements for a disproportionately large quantity of electronics just to make the magnetic memory electrically com-

Final manuscript received June 27, 1967.

SAUL LEVY received the BSEE in 1956 from Rensselaer Polytechnic Institute. In 1959, he received the MS in Mathematics from New York University. He is currently working towards the PhD in mathematics at Yeshiva University, where he is studying mathematical logic and foundations of mathematics. In 1956, he joined ITT Laboratories where he worked on all phases of the design, construction, and installation of a large special-purpose computing system. In 1959, he became a member of the computer theory group at RCA Laboratories. At RCA, he has worked extensively in switching theory and has studied problems associated with logical synthesis using flexible logic elements, redundancy techniques to improve the reliability of switching networks, and machine organizations that would be better suited to construction in a batch process technology.

patible with the logic (e.g. line drivers, sense amplifiers, level shifters, etc.). The semiconductor memory can be made compatible with the logic devices without the aid of additional interface electronics.

MACHINE ORGANIZATION

Instruction Words

In the earliest machines (such as SEAC), the size of storage, and consequently the address size, were small. This made it convenient for a single instruction word to contain several addresses. In the early drum machines, the modified single address or (1 + 1 address) structure was quite common. In this form, an instruction word contains an op-code and an op-address as in a single address instruction, but it also contains the address of the next instruction to be executed (Fig. 1). Thus, instructions could be distributed around the drum to minimize expected waiting times between instructions. With the advent of randomly accessible main memory this is no longer necessary and successive instructions are normally considered to lie in successive memory locations. As the size of memories increased, longer addresses were required to access a piece of data and this tended to make it difficult to fit several addresses into a single instruction word. Most current machines have either a double address (two operands specified) or a single address (one operand and the accumulator) with one noteable exception, the CDC 6600. Addressing for large data bases is generally broken into two components: a base value stored in a full-length register which generally is set and holds a single value over a portion of computation, and a displacement value (typically 12 to 16 bits) which is shorter in length than the base and is the portion of the address carried along in the instruction (Fig. 2). An instruction which needs to access main memory specifies the base address register (one of 8 or maybe 16) and a displacement, and the address in memory is computed by adding the displacement to the contents of the base address register (plus whatever address modifiers are specified).

GENERAL COMMENTS

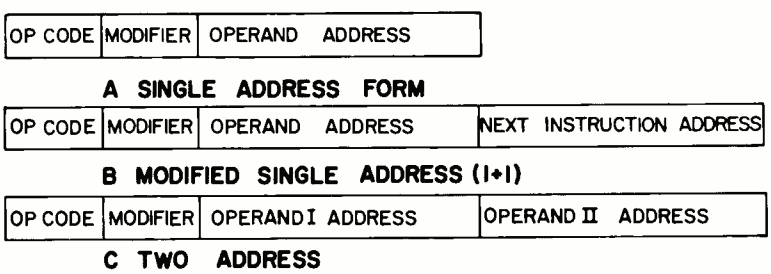
The progress in the early 60's was very much evolutionary. Main memories became faster and larger, electromagnetic devices made billions of bits of storage available in millisecond access times, and the basic logic gates became faster. The small machine became very popular spearheaded by the unbelievable success of the IBM 1400 series: nearly 15,000 of these were sold either as small stand-alone units or as peripheral processors for the larger 7,000 series. (RCA's small computers—the 301 and 501—together accounted for about 750 machines.)

The upper-middle-size machine was dominated substantially by the IBM 709—7094-7094II. However the most interesting progress occurred in the development of large-size machines. Both the LARC and the STRETCH[1] were failures both technically and financially: neither met its design goals and neither was produced for anywhere near its selling price (although IBM claims that much of its loss was in effect recovered by incorporating much of the STRETCH design—hardware mostly—into the 7090 series). However, only the CDC 6600 shows serious potential for becoming a financially successful large computer. The basic organization of this machine represents a departure from conventional machines. There is a single central processor which has ten functioning instruction units (i.e. multiplier, divider, shifter, etc.) capable of parallel operation. The central processor which operates on 60-bit words is a very high speed unit with typical arithmetic operation times running from a 300 ns floating add to a 3μs floating divide. "Surrounding" the central processor are ten small complete computers each with its own 4096-word memory (12-bit words). These peripheral processors control I/O and handle the general functions of data preparation for the central machine (which stores 131,000 60-bit words).

The machine, first delivered in 1964, has the major bugs worked out of it and now seems on its way to general acceptance as *the* big machine. The memory which has a cycle time of 1 μs (fast for 1964) is overlapped 32 ways, although the machine cycle is such that only 10 memory accesses may be made in 1 μs. The basic memory module is 4096 words by 12 bits. These are stacked 5 high and arranged into 32 banks to make the main memory, and are used individually as peripheral processor memories.

The central processor has a set of eight 60-bit high-speed registers, $X_0, X_1, \cdots, X_7$ which are used for holding operands and results. Associated with these registers are eight 18-bit address registers $A_0, A_1, \cdots, A_7$. A change in the contents of any one of registers A_1 through A_5 results in new data being fetched from the main memory location (as specified by the contents of that register) and placed in the corresponding X register. In a similar manner, changes in A_6 or A_7 result in the contents of the corresponding X register being stored. (There are also eight 18-bit registers ($B_0, \cdots, B_7$) used to hold modifiers and tallies. These are used in the conventional way.) Most central processor instructions are three address instructions specifying two operand registers and a result. There is an elaborate look-ahead mechanism including an instruction stack holding up to

Fig. 1—Instruction words.



32 instructions which is used to keep the appropriate operands in the high speed registers when they are needed. The ten peripheral processors are used mainly for general overhead and I/O processing.

Much attention to machine organization has been focussed on array or cellular computers. These computers are composed of a matrix of small individual computers, each communicating with some restricted set of "neighbors" and each doing its own processing. Examples of such machines are 1) the Holland[9] machine where each processor worked independently of the others with no central control and 2) the Solomon[10] where the processors worked in parallel but under the control of a single central processor. Of the two types, the difficulties of programming the Holland machine were never overcome and the machine was never built. An early scaled-down version of Solomon was built for RADC, but severe restrictions in connectivity, difficulty of programming, etc. resulted in its being set aside. A strong argument against the approaches taken in the array machines described above is stated in "Grosch's Law". Grosch's Law[11] is an element of the folklore of computers which has been verified empirically and which states roughly that *computing power increases as the square of cost.* This holds within the bounds of the current technology. But this says, in effect, that putting together multiple simple computers to do a larger job is not as economical as building a more complex single processor. The current effort to build a Solomon[12] is more reasonable in that each of the basic processors, instead of being a simple device, is a computer which is at the edge of the technology. It is being built by Burroughs for the University of Illinois and funded by ARPA. The memory is to be 250-ns thin films and the logic, which will be built by Texas Instruments, Inc., will approach large scale integration. In general, the array machine appears to be effective for the type of problem which can keep many processors busy. This is a restricted, but apparently large, class of problems; it now remains to be seen how effectively the machine can be used.

Another approach to the supercomputer is a multi-computer system where the computers, instead of being identical, are specialized to the task. An example of such a machine is the CDC 6600 mentioned above and the more recent IBM 360/90[5] machines. The 360/90 contains special I/O processors, a special fixed-point processor, a special floating-point arithmetic unit, and a special processor whose main job is to look ahead in the program and schedule the execution of instructions so as to keep the floating-point-arithmetic unit busy. There is a great deal invested in the floating point unit; in fact, it alone is bigger (more gates) than the largest computer IBM has built previously[13]. Similar to the 6600, it has autonomous computation units, but they are of a type known as pipeline units. In the multiplier for example (which is an almost combinational 64-bit floating point—about 20,000 gates) the time for a multiplication is 180 ns, but it is operated in three cycles of about 60 ns each. A new multiply can be entered each 60 ns, so that at any given instant three multiplications at different stages of activity can be in process in the single multiplier. The floating-point unit contains its own set of hardware registers, and the main task of the special processor is to see that all the operands required in the floating-point instructions are available in the registers at the time they are needed so as to ensure that the floating-point unit is not kept waiting for a piece of data to arrive from main memory. The machine is programmed in the conventional way (in fact it is compatible with the rest of the 360 line) and any alterations in sequencing, etc. are handled in the special processor.

TIME SHARING

The biggest stir in the computer field has been caused by time sharing. The first major endeavor in that field was in MIT's project MAC[14] using an IBM 7094 specially adapted to work with an extra-large core memory. The system was virtually all in software with the exception of additional I/O buffers and, of course, the terminals. Since the initial project MAC experience, all the major manufacturers are constructing computers with special hardware to facilitate time sharing: the GE 645 came first and is replacing computers at project MAC and Bell Labs New Jersey locations, among others. The SDS Σ-7 is a smaller machine that has won acceptance at several smaller users. IBM announced a machine, the 360/67 which is intended for time sharing and which immediately swept the large time-sharing market selling to MIT Lincoln Labs (not project MAC), Bell Labs midwest, and almost everyone else interested in large machines. There are also other machines like the Honeywell 8200, the CDC 6500, and the Univac 1108 multiprocessor system.

RCA is making a moderate-scale time-sharing system, the 70/46, which will compete with the SDS machine and others of that size. Though there are

R1 names fast access register which contains first operand

B2 is the name of the base register used in forming the address of operand two

X2 names the index register used in computing the address of operand two

D2 is the displacement used in computing the address of operand two

OPERAND 1 is in the register R1

OPERAND 2 is in the address computed by adding the contents of base register B2, and the contents of index register X2, and D2

Fig. 2—Third generation computer instruction (Rx format).

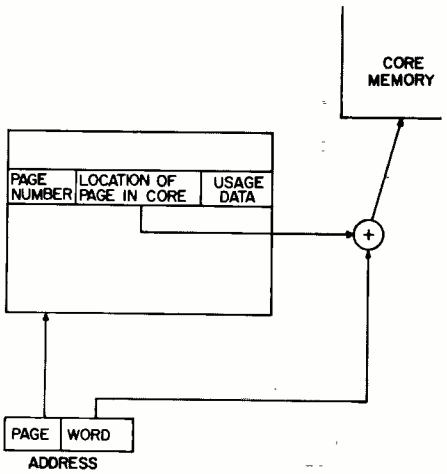


Fig. 3—Page addressing scheme.

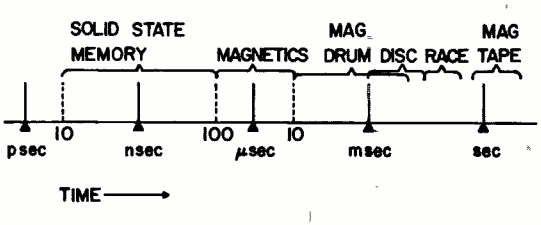


Fig. 4—Spectrum of memory devices.

many time-sharing systems now in operation from the very modest GE265 (GE 235 and model-30 buffer) up to the DEC PDP 6 at Applied Logic or the SDS 940 (with 11 languages) at Berkeley, and of course, project MAC; all of these are essentially software systems—no special hardware to assist in such difficult tasks as management of a storage hierarchy; consequently there is inefficiency introduced when they are operated in a time shared environment. The 'typical' on-line user expects rapid (at most a few seconds) response from the computer. Then, the only way for the machine to satisfy many users is to alternate in some reasonable order among them with a cycle time which is very short. If the main memory of the machine were infinite, each user could fit his whole program in memory; in each time slot, the machine would execute a piece of the stored program for the appropriate user. But memories are not infinite, and in general, the sum of the memory requirements exceeds the capacity of the main memory. This must be hidden from the user—he should not have to worry about limiting his program size in accordance with the needs of other users. So something must be done to make the main memory appear "as big as it must".

PAGING

This is a general description of paging (Fig. 3): most manufacturers have adopted some variation. About 1960, the computer group at the University of Manchester[15] was faced with the problem of building a high-speed computer with only a small core memory and a reasonably-sized drum memory for back up. They attempted to build a system where the entire memory (core and drum) was addressed as if it were in core. The technique worked essentially as follows (the numbers are approximate): memory was divided into 512 word units called pages, the core memory held 32 pages. The drum storage was 96K words. There was a special set of 32 page registers which held the addresses of the 32 pages contained in the core memory in addition to some simple housekeeping information (e.g. when a particular page was last addressed). A memory address could be thought of as consisting of two components:

1) A 9-bit page name specifying in which page the address was located; and
2) A 9-bit address specifying which of the 512 words in that page was specified.

When a reference to memory was requested, the page portion of the address was checked against the table; if the page was shown to be in memory, the reference continued; if not, it had to be brought in from the drum. If there was no vacant page on the drum, this would have to wait until a page was dumped from core onto the drum. One of the jobs of the system was to see that there was always an empty page in core when it was needed. To assist in this process, the page table stored special usage information (for example, has this page been written into?) as well as the location of pages in core.

In time-shared computers, paging is used to make large core memories appear enormous. Certain variations on the paging scheme are quite common; the most significant of these is segmentation which is, roughly, an extra level of paging. The pages are arranged in segments in much the same way as words are arranged in pages and the address is thought of as containing three components: the segment number, the page number, and the word number. But essentially the technique is the same as paging.

MICROPROGRAMMING

In 1951, Wilks first suggested that the control sequence for a computer might be put into a read-only memory—associating with each of the lines in the processor to be controlled, a bit or set of bits stored in words in the read-only memory.[16] A sequence of words would be associated with each command. Thus, a certain flexibility is introduced into the control of the computer that is not present when the control sequence is generated by wired-in gates. To build a microprogram control, the memory used must be 1) low cost and 2) very fast. The current generation of machines—at least the IBM system 360 and the RCA Spectra 70 have microprogram controls for the lower-speed members of the family. Both manufacturers (RCA in the 70/55 and IBM in the 360/75 and 360/90) find that to get the speed required for fast machines at an economical price, wired logic is necessary. RCA's read-only memory is in two overlapped memory banks each with a 960-ns cycle time giving an effective read time of 480 ns/step. IBM has read-only memory in the 360/65 operating as fast as 125 ns. The microprogram control also enables both manufacturers to provide emulators with their computers. An emulator is essentially an additional read-only memory which enables the computer to interpret and execute an additional set of instructions, typically for a second generation computer. In this way, a user can run without any rewriting or preparation a program written for his old machine and much faster than he could have run it with a software simulator. Emulators are available to run IBM 1401, RCA 301, and RCA 501 programs on the Spectra 70/45 and 70/35; IBM has emulators enabling to run 1401 and 7000 series programs on the appropriate 360 machines. Read-only memories are generally only mechanically alterable although the Honeywell 8200[17] will have a read-only memory which will be electrically alterable by the manufacturer.

INPUT-OUTPUT EQUIPMENT

Surprisingly enough, the progress in I/O equipment has been very slow as compared to the electronics. High-speed line-at-a-time printers operating at 1000 to 1200 lines/min. were common in 1960 and are still at the upper limit for mechanical printers. Console typewriters which punch and type at a maximum speed of about characters/sec. are also the rule now as they were in 1960 (or even earlier). Punched-paper-tape readers similarly have remained at virtually the same performance level since 1960 (about 1000 characters/sec.—read, about 100 characters/sec.—punch). Card readers have almost doubled in speed; but if one considers that computer speeds have increased by 1 to 2 orders of magnitude, then it is not very significant. However, there have been major improvements in magnetic recording techniques resulting in very high bit densities on magnetic media. This results in high speed magnetic tapes (120 to 240 kilobytes/second for high-speed units) and high-speed high-density magnetic drums (1 μs read or write times with capacities of 10^7 bits and access times of 10 to 20 ms).

New random-access storage devices with capacities far exceeding drums and access times measured in milliseconds have appeared. The primary device of this type is the magnetic disc memory which stores data on a stack of magnetic discs. A typical disc memory stores about 7,000,000 bytes which may be accessed in about 100 ms and then read at a 150-kilobyte rate. It is not uncommon for a computer to contain as many as eight of these devices. Another class of random-access device involves data stored on magnetic cards which must be selected from a file and brought under the read/write heads. These include the RCA RACE, the NCR CRAM, and the IBM Data Cell. Access times average about 200 to 250 ms and data is then read at 70 kilobyte rates. The attractive feature of this device is that its capacity is large —almost 600 million bytes/unit with each RCA or IBM machine having a capacity to handle up to eight units with a single controller. Because of the rela-

tively long times taken to access the first piece of information (Fig. 4) these devices find their primary application as block storage devices; one does not normally go to them to acquire a single piece of information, but rather to acquire a relatively large sequence of adjacent pieces of data. There are several new special devices for handling communications between computers and the outside, including such special-purpose devices as those which assemble voice messages. Communications buffers and data gathering devices are standard in every product line.

A device which has become more common in present generation machines, to a large extent as a result of time sharing, is the graphic console. This enables the user to communicate with the computer in a picture language much as he himself would use in order to solve problems with pencil and paper.

SOFTWARE

At about the time that Bauer's report was written (1957) IBM introduced the first FORTRAN compiler. There had been other user-oriented languages (even compilers) before but FORTRAN was the first designed to produce "good" code that is comparable in quality to that produced by hand by a "good" programmer. FORTRAN became the first widely accepted programming language to be adopted for use on the machines of several manufacturers. At present, better than 100 processors have been prepared for the FORTRAN language and it is available for nearly every computer intended for scientific use which is available in this country. After FORTRAN, COBOL (a Business-oriented counterpart) was introduced; then another scientific language ALGOL in its several versions became very popular in Europe and at certain universities. Most recently, IBM has announced PL/I which is a kind of superset of all the others. These languages all fit into the category of problem-oriented languages (their instruction repetoire is closer to the needs of the problems to be handled than the languages of the machines on which they are to be implemented). These languages have been joined lately by a host of special purpose languages such as COCO[18] which is suited to the problems of civil engineers, SKETCHPAD[19] which is a pictorial language for use with graphical I/O devices, etc. But FORTRAN remains the most widely used of all computer languages.

At present, the machine-oriented language is used primarily by two classes of user: 1) systems programmers and 2) others for whom there is no problem-oriented language suitable for their particular class of problem.

As the number and variety of problem-oriented languages increases, the fraction of computer users for the machine language will continue to decline. The use of problem-oriented languages carries with it a compatibility not carried by the machine language.

Compatibility at the machine language level is an important feature of third generation computers. IBM, RCA, Univac, and Burroughs have introduced compatible families of machines where machine-language programs written on one member of a machine family can be run on other members of the same family (with some restrictions on system configuration). RCA has designed its Spectra 70 to be language compatible, generally, with the IBM 360-series; Univac has apparently done the same with its 9000-series. But the most significant compatibility lies in the common user-oriented languages.

PREDICTIONS FOR THE NEAR FUTURE

The next generation of computer will surely be constructed of monolithic integrated circuits, although the number of gates on a single circuit will probably range from 4 to 300. The largest arrays to appear will most probably be in scratchpad memory. Monolithic memories, probably magnetic, will overtake the core memory as the main memory for computers. However, as the batch fabrication technology improves, solid-state scratchpad memories on the order of a few thousands of words at very high speeds should become common, and what is now the main memory will become less significant in the scheme of operation of the computer.

The current generation of computers is better oriented to multi-processor operation than the preceding generations and this trend will undoubtedly continue. There are provisions for sharing memory banks as well as I/O channels; in fact, several systems such as the time sharing machines are designed and sold as multiprocessors. (These include GE 645, IBM 360/67, CDC 6500, Honeywell 8200, and Burroughs B8500.)

The pipeline-type processor described briefly above in connection with the IBM 360/90 will achieve more general acceptance. Time sharing will surely have a great impact on the fourth generation of machines. The market for small consoles (like the teletype and the graphic consoles) will increase by orders of magnitude. Machines for time sharing of two main types will be marketed. The first (like the PDP 10, the RCA 70/46, and the SDS Σ-7) will serve those users who envision the running many small-to-medium size problems in a generally restricted environment—requiring fewer than, say, a dozen languages (e.g. FORTRAN, SNOBOL, COBOL, and a debugging language).

The large machines (the GE 645 or the project MAC system) would be used in what is commonly called the "computer utility" mode. This would involve the maintenance of large special files for many of the users as well as a capacity for each of the users to contribute to the system the work he has invested in the machine. Then a new language or set of routines developed by one user for the system can be immediately made available to the other users. (Naturally, if desired, privacy could be maintained.) There is a current market for both types of systems, and this market should continue.

REFERENCES

1. W. F. Bauer, "Modern Large Scale Computer Design", *Computers and Automation*, 1957.
2. F. E. Hamilton and E. C. Kubie, "The IBM Magnetic Drum Calculator Type 650," *JACM*, Vol. 1, PB (Jan. 1954).
3. "The Univac 9200 and 9300," *Datamation* (Jul. 1966).
4. "The Burroughs B8500," *Datamation* (Aug. 1965).
5. Talk delivered at Princeton University EE Department by a repesentative of IBM. Details of the 360/91 a version of the same machine equipped with a conventional core memory may be found in the *IBM Journal of Research and Development*, Vol. 11, No. 1 (Jan. 1967).
6. Sidnam, S. Levy, H. Miller, R. Lindhardt, "LIMAC: a Large Integrated Monolithic Array Computer," this issue of the RCA ENGINEER.
7. "The Sigma 7 from SDS" *Datamation* (Mar. 1966).
8. J. Thornton, "Parallel Operation in the Control Data 6600," *Proceedings FJCC*, Volume II (1964).
9. J. Holland, "A Universal Computer Capable of Executing an Arbitrary Number of Subprograms Simultaneously," *Proceedings of the EJCC*, Winter 1959.
10. D. L. Slotnick, W. C. Bosch, and R. C. McReynolds, "The Solomon Computer," *Proc. FJCC* (1962) pp. 97-107.
11. D. Slotnick, "Unconventional Systems" *Proceedings SJCC* (1967).
12. K. E. Knight, "Changes in Computer Performance," *Datamation* (Sep. 1966).
13. John Earle, Panel Discusion on Logic Partioning in LSI, ISSCC (Feb. 1967).
14. F. J. Corbato, M. Merwin-Daggett and R. C. Daley—"An Experimental Time-Sharing System" *Proceedings SJCC* (1962) p. 335, "The compatible Time-Sharing System Programmer's Guide" *MIT Press* (1963).
15. T. D. Kilburn, B. G. Edwards, M. J. Lanigan, and F. H. Summer, "One Level Storage System", *IRE transactions on Electronic Computers*, Vol. EC-11, No. 2, (Apr. 1962).
16. M. V. Wilkes, "The Best Way to Design an Automatic Calculating Machine," Manchester University Inaugural Conference, Manchester (Jul. 1951) pp. 16-18.
17. "The Honeywell 8200" *Datamation* (Jul. 1965).
18. D. Holstein, "Are You Ready for Computer-Aided Design", Product Engineering (Nov. 23, 1964).
19. I. E. Sutherland, "SKETCHPAD: A Man-Machine Graphical Communications System," *Proc. SJCC*, Vol. 23 (May 1963). T. E. Johnson, "SKETCHPAD III Three Dimensional Graphical Communication with a Digital Computer," *Ibid.*
20. N. Nisenoff, "Hardware for Information Processing Systems: Today and in the Future," *Proceedings of the IEEE*, Vol. 54, No. 12, (Dec. 1966).
21. T. H. Bonn, "Mass Storage: A Broad Review," *Proceedings of the IEEE*, Vol. 54, No. 12, (Dec. 1966).

THE ALGEBRA OF CLASSES

The algebra of classes is a descriptive name of a Boolean algebra and is similar in most respects to set theory which is taught to some extent in elementary and high schools as "the new math." This article introduces several tangentially important aspects of this subject as it applies to computer design for those readers who may not have had contact with it before. A bibliography is furnished for those whose interest leads them to pursue the subject in more detail. Because the algebra of classes and the algebra of sets are isomorphic forms of Boolean algebra, their terms will often be used interchangeably.

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C. M. WRIGHT received the BS in 1951 from the US Merchant Marine Academy, and sailed as Third and Second Mate aboard US Merchant Marine vessels. He served on active duty in the US Navy for four years as a Lieutenant in the Submarine Service. In March, 1959, he joined RCA Service Company as a computer engineer in the newly-formed EDPS division, where his first assignment was with the RCA 501 Project Development group. Later he assisted in the installation and maintenance of the first RCA 501 Data Processing System. He was manager of the CIA installation; later was promoted to EDPS Area Manager; and, in January, 1962, was promoted to EDPS District Manager. During this time he earned a diploma in automation electronics and studied physics, statistics, and operations analysis at George Washington University. In 1963, he worked at RCA, Van Nuys, on special assignment designing the engineering logic of the RCA 3488 Random Access Unit. He returned to the Cherry Hill offices in December, 1965, as manager, EDPS Special Projects. Mr. Wright has had a patent granted for a logic circuit design and currently has two patents pending. In August, 1967, he transferred to the patent operations staff of RCA Patents and Licensing. He is studying for a JD degree at Temple University and belongs to the Operations Research Society of America and the American Bar Association (student member).

DIGITAL CIRCUITS and networks can be classified in many ways, e.g., combinatorial versus sequential, synchronous versus asynchronous, inverting versus noninverting. Digital circuit inputs are usually two-valued but an infinite number of multi-valued logics can be systemized. This article will be devoted to two-valued, combinatorial logic using both inverting and noninverting gates. [*Editor's note:* The paper by A. Turecki in this issue describes a three-valued logic.]

The first encounter with Boolean algebra is usually in the form of equations such as

$$AB' + (BC)' + AC = 0$$

where the prime (′) denotes *not*. The juxtaposition of variables is understood to be the AND operation, called also the *intersection, logical product, conjunction* and *cap*. The plus sign represents the OR function and has other names such as the *union, logical sum, disjunction,* and *cup*.

When an expression is true, it is equated to 1 and when false, to 0; however, voltages in digital circuits are seldom assigned unique polarities for true or false. For example, in the RCA 301, an input to an AND gate is true when low, but to an OR gate, high is true. (This can depend on the point of view as will be seen later in the article.) Since the notation is used with known circuits, there will never be any ambiguities.

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VENN DIAGRAMS

To visualize the logical shorthand of George Boole (1815-1864), *Venn* diagrams were found useful. Fig. 1 shows a Venn diagram for one variable. The shaded area inside the circle is the class denoted by A; what is meant specifically by the class of A is not important. The box in which the circle is enclosed is considered the *universe*, represented by I. The area outside the box is in the *null* class symbolized by $\emptyset$.

Fig. 1—One-variable Venn diagram.

The area inside the box but not enclosed by the circle is the class of *not-A* or A'. If the universe shown is considered to be all humans, then let A be the class of all male. Obviously then, A' is the class of all females.

The following relations can be seen immediately from the diagram:

$$A + A' = I = 1$$
$$AA' = \emptyset = 0$$
$$A + A = \mathrm{A}$$
$$A'' = \mathrm{A}$$

Fig. 2—Two-variable Venn diagram.

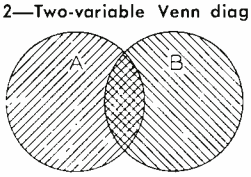


Fig. 2 is a Venn diagram of two variables. If the universe is considered a set, two variables generate four subsets:

AB' (left shading)
$A'B$ (right shading)
AB (cross-hatching)
$A'B'$ (unshaded area)

Note that the OR function is the EITHER . . . OR . . ., OR BOTH (called the INCLUSIVE OR as opposed to the EXCLUSIVE OR) so that A includes AB' and AB. Therefore,

$$AB + AB' + A'B + A'B' = I = 1$$

and

$$(A+B)\ (A+B')\ (A'+B)\ (A'+B') = 0$$

The first equation is in a form called the *sum of products* and the second, the *product of sums* for the complete set. They contain only *canonical* terms: all terms contain all the variables. If the following equation were expressed in canonical form

$$AB + AC' + B'C = D,$$

it would be

$$ABC + ABC' + AB'C' + A'B'C + AB'C = D$$

The sum of products for the complete set of subsets formed by two variables can be used to simplify the following equation shown schematically in Fig. 3:

$$ABC + AB'C + A'BC = C(AB + AB' + A'B).$$

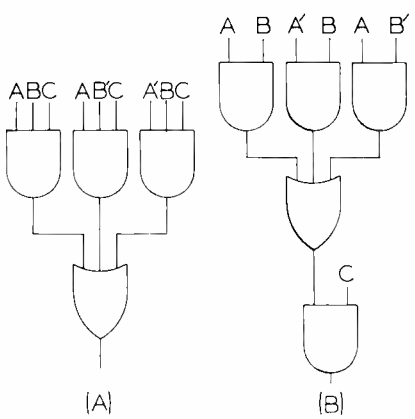


Fig. 3—Schematic representation of the sum of products for the set of subsets formed by two variables.

Referring to Fig. 2 $(AB + AB' + A'B)$ is the entire shaded part and, when removed, leaves only $A'B'$. It follows then that

$$AB + AB' + A'B = (A'B')'$$

and the equation reduces to

$$(A'B')'C.$$

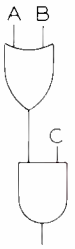
DeMORGAN'S THEOREM

De Morgan's Theorem can be introduced at this point to simplify the expression further: *A primed function is equal to the same function with the* AND *and* OR *operations replaced by* OR *and* AND *operations respectively, and the elements primed.* In other words,

$$(A'B')' = (A')' + (B')' = A + B$$

So that the circuit simplifies to $(A + B)C$ as shown in Fig. 4.

Fig. 4—Simplification as a result of DeMorgan's theorem.



A more complex application of De Morgan's Theorem is

$$(AB' + A'B)' = (AB')'\ (A'B)' = (A' + B)\ (A + B')$$

and if the last expression is multiplied out according to the laws of algebra (cross-multiplied):

$$A'A + A'B' + AB + BB' = A'B' + AB$$

so that

$$(AB' + A'B)' = A'B' + AB$$

which can be verified from the Venn diagram in Fig. 2.

De Morgan's Theorem also explains how a positive (or negative) input AND gate and a negative (or positive) input OR gate can be the same circuit.

Figs. 5 and 6 show Venn's original diagrams for three and four variables

Fig. 5—Three-variable Venn diagram.

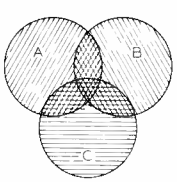
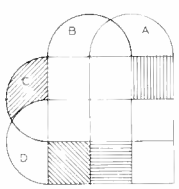


Fig. 6 — Four-variable Venn diagram.



respectively. Fig. 6 has the following expressions shaded:

$A'B'CD'$ (left shading)
$A'BC'D$ (right shading)
$ABC'D$ (horizontal shading)
$AB'CD'$ (vertical shading).

The diagram illustrates that

$$A'B'CD' + AB'CD' = B'CD'$$

and

$$A'BC'D + ABC'D = BC'D$$

These simplifications can be seen directly from the equations since

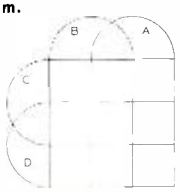
$$A'B'CD' + AB'CD' = (A' + A)B'CD' = B'CD'.$$

However, the following equation is not easily simplified without the diagram:

$$A'BD + A'B'C'D + ABC'D + ACD + B'D.$$

Fig. 7 is a blank four-variable Venn diagram provided for the simplification of the above equation.

Fig. 7 — Blank four-variable Venn diagram.



KARNAUGH MAPS

As the number of variables increases beyond four, Venn diagrams become quite burdensome and hard to use. *Veitch* diagrams were an improvement over Venn's but Karnaugh[1] developed a mapping system which is simpler to use. *Karnaugh maps* can be used to analyze expressions containing up to eight variables.

In the notation that follows, expressions will be understood to be in canonical form with A first, B second, and so on. However, if A' is meant, 0 will be used and if A is meant, 1 will be used so that $AB'C'D$ will be written 1001.

Gray Code

For use in explaining the Karnaugh Map, the *Gray code* will be introduced. Various error-correcting and sequential codes have been developed for specific uses. One in which only a single variable changes between steps is called a Gray code. The following tabulation shows how one such code can be constructed.

Decimal	*Binary (weighted)*	*Gray*
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

While a Gray code cannot be used for arithmetic purposes because each position does not have a specific weight (or radix exponent), it is useful for count-

ing circuits and analog-to-digital (A/D) conversion. For instance, a shaft encoder using weighted binary numbers must change all four bits going from position 7 to position 8, and if the motion is slight there is a chance that some contacts will not be made while others will. Therefore, going from 7 to 8 could be incorrectly decoded as going to position 9 if the least significant digit were slightly lagging. With the Gray code, any change indicates a new position without ambiguities. Note also that the Gray code "folds over", that is, changing one bit of the last figure will result in the first figure again.

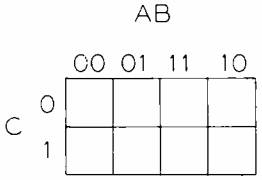
When A/D conversions are made, it is usually desirable to perform arithmetic on the results. Therefore, the conversion is made utilizing a Gray code which is then decoded into weighted binary. The simple rules used for decoding are:

1) The most significant digits are the same; and
2) The subsequent Gray code bits are exclusively OR'd to the previous binary bits to give the corresponding binary digits.

Three Variables

Fig. 8 shows a three-variable Karnaugh Map. The values of AB are in Gray code across the top and the two values of C are along the side. The eight cells formed by the two rows and four columns correspond to the eight possible canonical expressions using three variables. Each cell is arranged so that each adjacent cell horizontally or vertically is reached by changing only one variable. Note that the left edge should be visualized as folding around to meet the right edge so that the first and fourth columns are considered adjoining.

Fig. 8—Three-variable Karnaugh map.



To use the map, the expression to be simplified is expanded into canonical terms and each corresponding cell in the map is labelled with a 1 and the rest with a 0, except as discussed later. If two 1's are in adjacent cells, the variable that changes from 1 to 0 between the cells can be eliminated from the term. If four 1's are in adjacent cells, the two variables whose values change from 1 to 0 can be eliminated in the term covering them.

The following example will show how this works. It was already shown that

$$AB + AC' + B'C = ABC + ABC' + AB'C' + AB'C + A'B'C.$$

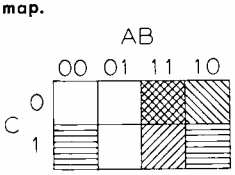
This can be simplified by

$$A(BC + BC' + B'C' + B'C) + A'B'C = A + B'C$$

because the expression in parenthesis is equal to 1 and A implies $AB'C$ so that $A + A'B'C = A + B'C$. This should be equally capable of simplification using a Karnaugh Map. Fig. 9 shows the original equation in the following way:

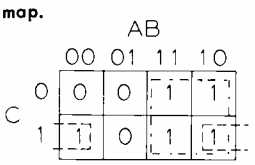
1) AB (left shading)
2) AC' (right shading)
3) $B'C$ (horizontal shading)

Fig. 9—Simplification using a three-variable Karnaugh map.



The overlapping subset caused by the intersection of AB and AC' is crosshatched. In Fig. 10, the shaded squares, corresponding to the canonical terms of the expression, are labelled with 1 and the rest with 0.

Fig. 10 — Elimination of terms using the Karnaugh map.



In Fig. 10, the 1's in 001 and 101 are adjacent to each other; thus, A, the variable that changes from 1 to 0 between the cells, can be eliminated and the term $B'C$ includes both of the cells. Four 1's are seen to be adjacent in such a manner that each is adjacent to two of the others. This can occur in squares or in a line so that two variables can be eliminated. In Fig. 10, both B and C go from 1 to 0 in the adjacencies so that the constant variable, A, encompasses all four canonical terms.

Note that the 1 of the term $AB'C$ is covered twice which is valid and also desirable since it permits a reduction in hardware. In fact, if a gating scheme is chosen so that each term is covered twice, a gate can fail without affecting the function. If the expression $BC + AC' + A'B'$ is gated as shown in Fig. 11, any one of the gates can fail without the circuit becoming inoperative. From this simple example, it is apparent that selective redundancy can be provided. The question may arise at this point, "Why not use two gates for each of the original functions?" If the probability of failure depends only on the gates, it would make no difference. The scheme in Fig. 11, however, provides some immunity from source failures because the gates' inputs are better distributed.

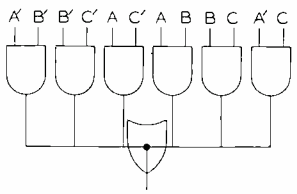


Fig. 11 — Redundant gating scheme.

Four Variables

A four-variable Karnaugh Map is shown in Fig. 12. In this map the left and right edges are adjacent and so are the top and bottom edges. The map should be visualized as being toroidal in shape, i.e., as if it were drawn on a doughnut or inner tube.

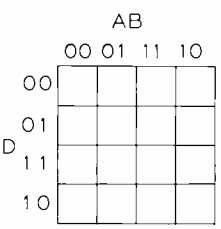


Fig. 12—Blank four-variable Karnaugh map.

Before working an example on a four variable map, *don't care* conditions should be discussed. Many times there will be input combinations which will never occur during normal operation. A term based on such a combination would never have the value of 1, otherwise there would arise the dilemma of designing a circuit capable of doing what need never be done. The values of 0 need only be assigned to terms which can arise but for which no output is desired. The terms which cannot occur could be designed to give an output without invalidating the circuit's task. On the other hand, such terms need not be decoded either. The rule is to use *don't care* conditions, denoted by X, to reduce the required gating. For example, suppose a circuit is to be designed to give an output when the

number in a scale-of-ten counter is divisible by three. A scale-of-ten counter usually employs feedback in a four bit binary counter to reset the count to 0 after a count of 9 has been reached. Therefore, the following tabulation gives the characteristics of the required circuit (the X values will never occur).

Input *ABCD*	*Output*
0000	0
0001	0
0010	0
0011	1
0100	0
0101	0
0110	1
0111	0
1000	0
1001	1
1010	X
1011	X
1100	X
1101	X
1110	X
1111	X

Fig. 13 is the required Karnaugh Map showing the desired outputs in the cells.

CD \ AB	00	01	11	10
00	0	0	X	0
01	0	0	X	1
11	1	0	X	X
10	0	1	X	X

Fig. 13—Application of a four-variable Karnaugh map.

The term 0011 has a value of 1 which can be combined with the X (taken now as 1) in the cell 1011 so that it simplifies to $B'CD$. The 1 in the cell 0110 combines with the X at 1110 so that it reduces to BCD'. The 1 at 1001 is adjacent to the X in 1101, and these two are adjacent to 1111 and 1011, so it reduces to AD. Since it is only necessary to include all the 1's, the complete solution is $B'CD + BCD' + AD$. Without the *don't care* conditions, three four-input gates would be required.

Six Variables

Fig. 14 shows a six-variable Karnaugh Map. Besides the adjacencies of the edges, cells equidistant from the vertical and horizontal center lines are to be considered adjacent, i.e., if the map is folded along the vertical or horizontal center line, adjacent cells will overlap. For example, 111011 is adjacent to 011011 and to 111111.

As a sample problem, design a circuit which gives an output only when a decimal number is providing the inputs using RCA 501 code. The RCA 501 uses an excess-three code and the decimal numbers are 23_8 to 34_8. There will be no *dont' care* conditions.

Fig. 15 shows a completed map and the simplest circuit equation can be seen to be $A'B(CD' + C'D + D'EF + DE'F')$. If the alphabetics are 40_8 to 71_8 inclusive and they are the zero terms (everything except numerals and letters are *don't care* terms), it is easily verified that the circuit output is simply A'.

Multi-Output Functions

The Karnaugh Map permits minimization of multi-output functions, too. This can be most easily accomplished, for a few outputs, by writing the ones and zeroes in their respective cells using one map. For example, the following functions

$$F_1 = ABC' + CD' + BCD + B'C'D'$$
$$F_2 = AB + A'B'C + BCD + A'BCD'$$
$$F_3 = A'CD + A'B'D' + A'BCD' + AB'D'$$

are mapped in Fig. 16. Fig. 17 shows the simplest gating to generate these three functions. The method of arriving at a minimal solution is to group output 1's together to form as few products as necessary. Referring to Fig. 16, the term $A'BC$ is common to all outputs as is $A'CD'$. It is better, however, to look for groupings of four 1's.

The term AB is used in outputs 1 and 2. The four corners—which are adjacent, remember—give $B'D'$ and are used in outputs 1 and 3. The term $A'C$ is used in outputs 2 and 3 and BC is used in outputs 1 and 2. These four terms include all the output 1's and furnish a complete solution.

Inverting Logic

Another advantage of Karnaugh maps is their use to bring out the advantages inherent in inverting logic: Inverting logic consists of either NAND gates, whose outputs are low when all inputs are high (*not*-AND), or NOR gates, whose outputs are low when any input is high (*not*-OR). In non-inverting logic, the complement of a variable (A' is the complement of A) is usually required as often as the uncomplemented variable so an inverter using active circuit elements is needed. Using inverting logic, all combinations can be generated using only uncomplemented variables. This is advantageous when complements are not so readily available as they are with flip-flops, such as when bussing signals or where pin limitations exist on plug-ins.

With several levels of gating, each gate's output forms an inhibit on the inputs to following gates. A simple example of how this is useful is the simplicity with which $AC'D' + BC'D'$ can be generated with NOR logic as shown in Fig. 18. This general type of circuit can be taken from a map by encoding loops of 1's and 0's and inhibiting the 0's with higher level gates. A map for the function generated by the logic diagram in Fig. 18 will show how this rule is applied.

The versatility and power of inverting logic gates can be seen in the implementation of a seven-variable parity checker where the complements are not available (as on a bus or transmission line). Fig. 19 shows a parity checker using NAND gates.

MULTILEVEL LOGIC

Multilevel gating can decrease the number of gates required to generate a given function. Such circuits are designed for non-inverting logic using *decomposition* methods, whereas with inverting logic the method is referred to as *transformation*. Fig. 20 shows a multilevel logic schematic for $(A'C + B'C + A'C'D + B'C'D)$. A sum-of-products generation would require four gates and two in-

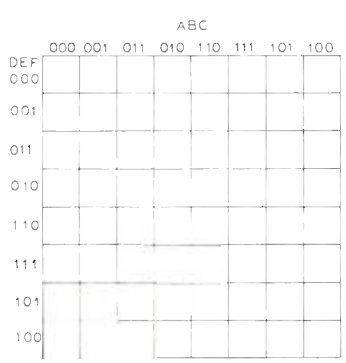


Fig. 14 — Blank six-variable Karnaugh map.

DEF \ ABC	000	001	011	010	110	111	101	100
000	0	0	1	0	0	0	0	0
001	0	0	1	0	0	0	0	0
011	0	0	1	1	0	0	0	0
010	0	0	1	0	0	0	0	0
110	0	0	0	1	0	0	0	0
111	0	0	0	1	0	0	0	0
101	0	0	0	1	0	0	0	0
100	0	0	1	1	0	0	0	0

Fig. 15 — Completed six-variable Karnaugh map.

verters. A product-of-sums circuit requires three gates and two inverters.

The technique described here is only one of many that a logic designer should be familiar with so as to be able to design the best circuit for a given function. For instance, multilevel logic, while more economical to use, may result in enough accumulated delay through each stage to render it too slow for some applications. However, designing every circuit to work as fast as possible is equally bad judgment. Also, graphic techniques are neither suited to automated design methods nor useful for large numbers of input variables and output functions. Methods developed by Quine, McCluskey, Hoffman, Ashenhurst, Ledley, and others can be used as necessary depending upon system requirements. Boolean matrices provide a mathematical approach to the design and analysis of large network arrays and sequential networks.

CONCLUDING REMARKS

It should be stressed that Boolean algebra will not give any answers that clear and concise mental reasoning can not provide. Its values are that it forces an organized approach to the problem at hand and furnishes a memory aid.

The engineer's basic job is to solve problems. He must bring the knowledge of several years training and experience to bear on each task. He must also have an organized approach which is not unlike the function of a data processing machine.

The steps involved in problem solving are

1) Getting *correct* input in usable form;
2) Rearranging the data with facts already known in accordance with the laws of thought (formal logic); and,
3) Arranging the deductions in usable output form.

The knowledge of the engineer constitutes the major premise in step 2) above and the parameters of the problem furnish the minor premise.

In assimilating the input information, it is necessary to take steps to insure that it is correct. Logic consists of *tautologies*, that is, relations that are *valid* independently of the *truth* of the propositions involved.

Alternatively, if the reasoning process is faulty, the correctness of the input will not insure a true result. There are two major fallacies that are committed frequently, even among expert researchers. Scientists and engineers should be wary of them because they can cause much wasted effort.

In the proposition *if A, then B* (or *A implies B*), *A* is called the antecedent and *B* is the consequent. The first fallacy is called *affirming the consequent*; it is stated, *if A implies B, then B implies A*. That this is wrong can be seen from the following proposition: *if the automobile has no gasoline, then it will not run.* It is not valid to reason: *it is not running, therefore, there is no gasoline.* The automobile may not be running because the ignition switch is off.

The second fallacy is called *denying the antecedent* and is stated: *if A implies B, then A′ implies B′*. Using the example proposition above, it is not valid to conclude: *the automobile has gasoline, therefore it is running.*

Another example of the first fallacy is based on the following proposition: *It is generally true that the larger a river, the larger the city at its mouth.* Building a bigger city will not increase the size of the river.

No engineer should make the mistakes in the above examples but these fallacies creep into reasoning in more subtle ways. Personal bias and desires, or convenience, or lack of complete knowledge about a subject will often lead the unwary thinker awry.

If two numbers are not equal, one must be greater than the other appears to be a self-evident truth. It is, however, not true.[2]

REFERENCES

1. Karnaugh, M., "The Map Method of Synthesis of Combinational Logic Circuits", *AIEE Transactions on Communication and Electronics*, LXXII, Nov., (1953) pp. 593-595.
2. Gamow, George, *One Two Three . . . Infinity* (New York, Viking Press, 1947), pp. 31 et seq.
3. Curtis, H. Allen, *The Design of Switching Circuits* (Princeton, D. Von Nostrand, 1962).
4. Korn, G. A. and J. M., *Mathematical Handbook for Scientists and Engineers* (New York, McGraw-Hill, 1961) sec. 12.
5. Ledley, R. S., *Digital Computer and Control Engineering*, (New York: McGraw-Hill, 1960).
6. Machol, R. E., et al. *System Engineering Handbook*. (New York: McGraw-Hill, 1965) chap. 41.
7. Maley, G. A. and Earle, J. *The Logic Design of Transistor Digital Computers*. (Englewood Cliffs, Prentice-Hall, 1963).

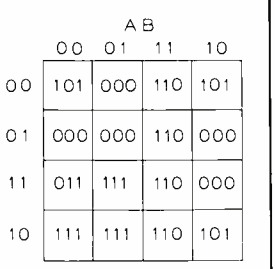


Fig. 16—Karnaugh map for minimization of multi-output functions.

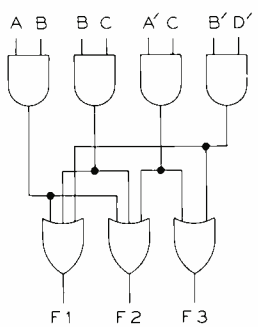
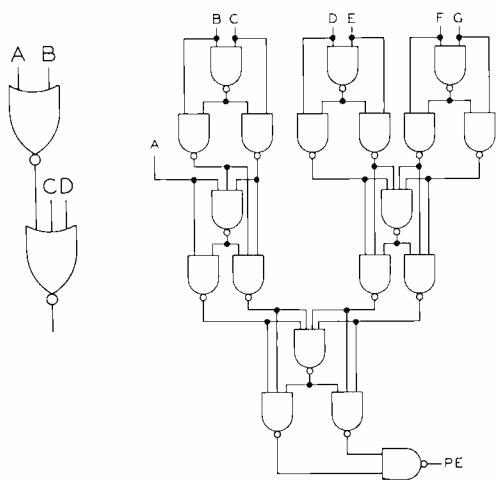


Fig. 17—Implementation of the functions mapped in Fig. 16.

Fig. 19—Parity checker using NAND gates.



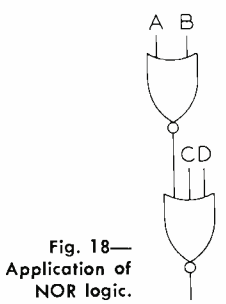


Fig. 18—Application of NOR logic.

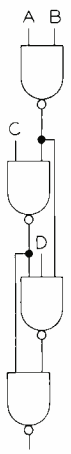


Fig. 20—Multilevel logic schematic.

THE TERNARY NUMBER SYSTEM FOR DIGITAL COMPUTERS

The most efficient radix for a number system is **e**, the base of the natural logarithm. Since 3 is the nearest integer to **e**, it is reasonable to investigate the possibility that a ternary computer should be more efficient than a binary computer. For example, a 10-digit decimal number needs 40 bits in binary coded form, 33 digits in straight binary translation, and 21 digits in ternary representation. Provided a ternary-register element costs the same as a binary element, a ternary computer appears to be very attractive. In present computers, the numerical systems are either binary or binary coded because most of the available switching elements are of binary nature. In this paper, a ternary number system is shown to be more efficient than a binary system provided that the ternary-element costs are not more than 1.5 times greater than the cost of a binary element. A ternary algebra is developed, and a ternary switching system is described.

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Editor's note: In our discussions with the author, an interesting algorithm for converting from the base-three number system to the base-ten system came to light; this is published as an Engineering Note in this issue.

Readers with a limited background in the formal structure of arithmetic (set theory, algebra of classes, Boolean algebra, etc.) may find the paper in this issue by C. Wright, "The Algebra of Classes," a useful introduction to this paper by A. Turecki.

IN DIGITAL COMPUTERS, all the arithmetic operations, fixed or floating point, are carried out on integers. The sign of a quantity and its magnitude in the floating-point system are operated by a sign logic and an exponent logic respectively. Hence, in the number representation for computers there must be methods for indicating sign and exponents of the operand quantities. Most digital computers use positional notation with fixed radices of 2, 8, 10 or 16. At least one mass-produced computer uses a notation with radixes of 2 and 5 (the bi-quinary notation which was used the first time in one of the earliest digital computing devices, the Chinese *suan pan*).

THE COST CONSIDERATIONS OF VARIOUS RADIX SYSTEMS

Let us assume that to represent each symbol in a given numerical system we need one logic element, and that the maximum numerical quantity to be handled is N. If r is the radix of the system the number of the required elements is $r \log_r N$ for $\log_r N >> 1$.

For the evaluation of different numerical systems we introduce a function, f_r, the ratio of the required hardware for the r-radix system and for the binary (2-radix) system:

$$f_r = r \log_r N / 2 \log_2 N = r/2 \log_2 r$$

Setting the derivative of f_r equal to zero,

$$df/dr = (\log_2 r - \log_2 e)/2(\log_2 r)^2 = 0$$

the minimum occurs at $r = e$. Thus, if the logic and memory elements with r-stable states were only $r/2$ times more complex than the presently used elements with two stable states, the r-radix numerical system would be the most economical.

Let us now consider the case where the numerical systems of the base $r>2$ are binary coded. For the comparison of the required hardware we should use the function

$$g_r = I_r / \log_2 r$$

where I_r is an integer and is the minimum required number of binary bits for the representation of one digit of the r-base. The magnitude of g_r for some values of r is as follows:

r	2	3	4	5	6
f_r	1.000	0.946	1.000	1.078	1.148
g_r	1.000	1.262	1.000	1.294	1.148
r	7	8	9	10	100
f_r	1.247	1.333	1.420	1.505	7.526
g_r	1.069	1.000	1.262	1.204	1.053

Note that:

1) For $r \geq 2$, $g_r \geq 1$;
2) for r equal to the positive powers of 2, $g_r = 1$;
3) For $r = 5$, g_r reaches the maximum value;
4) For $r = 6$, $g_r = f_r$; and
5) For $r >> 1$, $g_r = 1$.

Thus, using two-stable-state logic elements, the most economical numerical systems are of the base of 2, 4, 8, . . . , 2^n; the decimal system is only 20% more expensive than the binary. If one could develop sufficiently reliable three-stable-state logic elements which would be only 3/2 times more expensive than the corresponding binary element, the saving of 5.4% $[(f_3 - f_2)/f_2 = 0.054]$ in the arithmetic unit hardware would be accompanied by an increase in the memory cost by 26% $[(g_3 - g_2)/g_2 = 0.26]$ if the memory used were still 2-state. Hence, the ternary system would be justified only if both 3-state logic elements and 3-state memory elements were available.

These comparisons for different numerical systems have not considered the variations in the complexity of required logical schemes since this can be seen only after a scheme is developed. Therefore, the commonly used argument, that present availability of two-state logic elements warrants the use of the binary numerical system in computers, can be accepted only conditionally.

One argument for the binary system is its claimed simplicity in performing

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arithmetical operations. However, the occurrence of carries in the ternary addition is 41% lower than in binary addition, while the multiplication table is of the same order of simplicity.

SOME TERNARY CODES AND ALGORITHMS

We shall investigate in detail two ternary codes. For a lack of a better name, the ternary code with digits 0, 1, and 2, will be referred to as a *straight* ternary code, and with digits −1, 0, +1 (or simpler −, 0 and +) as a *symmetric* code:

Decimal Equiv.	Straight Code 3^2	3^1	3^0	Symmetric Code 3^2	3^1	3^0
0	0	0	0	0	0	0
1	0	0	1	0	0	+
2	0	0	2	0	+	−
3	0	1	0	0	+	0
4	0	1	1	0	+	+
5	0	1	2	+	−	−
6	0	2	0	+	−	0
7	0	2	1	+	−	+
8	0	2	2	+	0	−
9	1	0	0	+	0	0
10	1	0	1	+	0	+
11	1	0	2	+	+	−
12	1	1	0	+	+	0
13	1	1	1	+	+	+
•	•	•	•			
•	•	•	•			
•	•	•	•			
26	2	2	2			

Decimal Equiv.	Symmetric Code 3^2	3^1	3^0
0	0	0	0
−1	0	0	−
−2	0	−	+
−3	0	−	0
−4	0	−	−
−5	−	+	+
−6	−	+	0
−7	−	+	−
−8	−	0	+
−9	−	0	0
−10	−	0	−
−11	−	−	+
−12	−	−	0
−13	−	−	−

Note that the decimal range of the straight ternary code for n digits is

$$2\sum_{p=0}^{n-1} 3^p,$$

while the range of the symmetrical code is

$$\pm\sum_{p=0}^{n-1} 3^p.$$

Since the former code requires an additional digit for the sign designation, the range of the latter code is greater (for the same number of memory elements) by

$$3^n - \sum_{p=0}^{n-1} 3^p.$$

Ternary addition in straight code follows the sum and carry tables given below:

Sum

B \ A	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

Carry

B \ A	0	1	2
0	0	0	0
1	0	0	1
2	0	1	1

The percentage of the carry occurrence for a ternary full adder is 50% and the same is for a binary full adder. The 2's complementing of this code follows the truth table of the ternary logical connective of cycling:

Number	0	1	2
2's Compl	2	1	0

Subtraction, following the commonly used technique in digital computers, is performed by adding the subtractive complement of the subtrahend to the subtractor. The subtractive complement of an integer N to the base r and of n significant digits is defined as $N = r^n - N$. Let $(\pm A) \pm (\pm B) = (\pm C)$; the complete algorithm for add/subtract is as follows:

1) Assume the sign of the result C to be the same as the sign of the operand A.
2) If there are unlike signs of operands in add, or like signs in subtract, generate 2's complement of the B operand and inject a carry to the least significant stage of the adder. The carry will be referred to as the initial carry, and this carry together with the 2's complementing of the subtrahend generates the subtractive complement.
3) If the condition described in 2) above, exists and the most significant stage of the adder generates a carry, which will be referred to as the final carry, the result at the output of the ternary adder is correct.
4) If the condition described in 2) above, exists and there is no final carry, the result is wrong. This case requires the subtractive complementing and sign-change correction of the result.
5) If there are like signs of operands in add or unlike signs in subtract, the result (as generated by the adder) is correct. In this case, the final carry indicates an overflow, i.e., the result exceeds the precision of the adder.

Note that the algorithm is the same as one used for binary add/subtract. The addition in the symmetric code follows the rules given in the sum and carry tables:

Sum

B \ A	0	+	−
0	0	+	−
+	+	−	0
−	−	0	+

Carry

B \ A	0	+	−
0	0	0	0
+	0	+	0
−	0	0	−

As can be seen from the carry table, the percentage of the carry occurrence is $100 \cdot 8/27 = 29\%$. This is 41% lower than in the binary code.

The subtraction in this code is extremely simple. It is performed by adding the subtrahend with the reversed sign to the subtractor:

Example:

For $A > B$, let $A = 5$ and $B = 2$,

$$\begin{array}{r} 5 \\ -2 \\ \hline 3 \end{array} \rightarrow \begin{array}{r} +\,-\,- \\ -\,0\,+\,- \\ \hline \end{array} \rightarrow \begin{array}{r} +\,-\,- \\ +\,0\,-\,+ \\ \hline 0\,+\,0 \end{array}$$

For $A < B$, let $A = 3$ and $B = 5$,

$$\begin{array}{r} 3 \\ -5 \\ \hline -2 \end{array} \rightarrow \begin{array}{r} 0\,+\,0 \\ -\,+\,-\,- \\ \hline \end{array} \rightarrow \begin{array}{r} 0\,+\,0 \\ +\,-\,+\,+ \\ \hline 0\,-\,+ \end{array}$$

For $A < B$, the subtractive complementing path (which usually takes double the time of the add/subtract execution) is not required. This property of the code will also produce some saving in the hardware of the arithmetic unit.

The multiplication in symmetric code follows the algebraic rule for signs:

Product

B \ A	0	+	−
0	0	0	0
+	0	+	−
−	0	−	+

Note that the multiplication in this code does not generate a carry, while the straight ternary code does for $2 \times 2 = 11$.

Example: $2 \times 8 = 16$

$$(0\ +\ -) \times (+\ 0\ -)$$

$0\ -\ +$ 0^{th} *partial product*

$0\ 0\ 0\ 0$ 1^{st} *partial product*

$0\ +\ -\ 0\ 0$ 2^{nd} *partial product*

$+\ -\ -\ +$ *final product*

DEVELOPMENT OF A TERNARY SWITCHING ALGEBRA

The extension of the Boolean algebra to the ternary switching circuits will be modeled mainly after the many-valued propositional logic introduced by Post.

The three basic Boolean operations are *union, intersection,* and *complementation* which are mechanized by *or, and,* and *invert* logic elements. These concepts, with certain modifications, will be used in the development of the ternary logic.

A Post algebra P is a class C of elements $p, q, r, \cdots$ with two basic operations; $p \cdot q$ (*product*) and p' (*cycling*). Assuming three truth values (0, 1, and 2) for the elements of C, the above mentioned operators are defined by the following truth tables.

Product

q \ p	0	1	2
0	0	0	0
1	0	1	1
2	0	1	2

Cycling

p	p′
0	1
1	2
2	0

As defined here, $p \cdot q = min\ (p, q)$; that is, the product of p and q equals the smallest truth value, and represents a ternary *and* function.

Many mysteries of multi-valued logics will be cleared up when one realizes that the words *and, or,* and *not* have at best only tenuous analogy with their meanings in natural languages. A three-valued logic function means nothing more than the particular matrix pattern of the truth table that is permitted by that relation. If instead of saying *A implies B* in a ternary system, we said *A galumphs B,* considerable clarity might result.

In this paper, though it is recognized that there are significant differences in the structure of two-valued and many-valued logics, the analogies between the systems will be stressed and the binary logic will be considered to be a special case of multi-valued logic. For instance, if in the truth table defining the ternary *and* the truth value of 2 is excluded, it becomes the truth table for the familiar binary *and.* The same applies for the *cycling* concept, after eliminating 2, it becomes a binary *not.* In the binary logic, the *double not* of a variable is equal to the variable. It follows then that if a *double not* of a variable yields the variable, then a *triple cycling* in ternary logic should yield the same result. Hence Post's cycling was defined accordingly.

Fundamental to any logic algebra is the existence of an algebraic form of any function which explicitly gives the value of the function for every combination of variable values; this is the *canonical form* of the function. Closely associated with the canonical form is the *expansion theorem* which expands any function in a series about any of its variables. The canonical form is a result of expanding about all variables of a function. This form is the essence of synthesis; applying the expansion theorem in reverse is the first major step in *minimization.*

A logic switching algebra, to become a useful tool for the analysis and synthesis of switching networks, should operate with connectives which are complete functionally. The *completeness* of a connective or a group of connectives can be described for 3-valued logic as follows: there are 3^{3^n} different functions of n variables, and a given connective is complete if it is possible to express all the 3^{3^n} functions with only that connective or a group of connectives.

There are several ways of proving the completeness of a given connective or a group of connectives; one way is to prove an expansion theorem, while another is to establish an *isomorphism* (one-to-one relationship that preserves the operations of addition, multiplication, and the order relationship) between the algebra to be tested and another algebra which is known to be complete.

By definition a Post function is any element of a finite set P built up from elements of an arbitrary set C by a finite number of combinations of *product* and *cycling* operations. Since the ternary switching functions as defined by tables of logic values are themselves Post functions, there is a canonical expansion of the functions in terms of the product and cycling operation. Hence, the ternary switching logic, as presented here, is complete.

To simplify the analysis and synthesis of the ternary functions, some auxiliary operations will be introduced. These are *sum* $(p + q)$ and negation (p and J) operations.

$(p + q)$

q \ p	0	1	2
0	0	1	2
1	1	1	2
2	2	2	2

p	$\bar{p}$	$J_0(p)$	$J_1(p)$	$J_2(p)$
0	2	2	0	0
1	1	0	2	0
2	0	0	0	2

As defined here, $p + q = \max\ (p, q)$ and $J_k(p) = 2$, if $k = p$; $J_k(p) = 0$ if $k \neq p$.

Note that the J operation, reduced to the binary logic, becomes the binary negation. According to the definition, $J_0(1) = J_1(0) = 0$ and $J_1(1) = J_0(0) = 1$. Therefore, if $J_1(p) = p$, then $J_0(p) = \bar{p}$; the bar signifies binary negation.

In the ternary switching logic, there are $3^3 = 27$ different functions for one variable. The table of all 27 ternary functions can be reduced to the four binary functions for one variable, once again showing that the binary as well as the ternary logics are special cases of the general m-valued logic system developed by Post.

p	0	1	2	*Ternary Functions*
f_0	0	0	0	$J_0(p) \cdot J_1(p)$
f_5	0	1	2	$J_2(p) + J_1(p) \cdot 1 = p$
f_{21}	2	1	0	$J_0(p) + J_1(p) \cdot 1$
f_{26}	2	2	2	$J_0(p) + J_1(p) + J_2(p)$

p	0	1	*Binary Functions*
f_0	0	0	$J_0(p) \cdot J_1(p) = p \cdot \bar{p}$
f_5	0	1	p
f_{21}	1	0	$J_0(p) = \bar{p}$
f_{26}	1	1	$J_0(p) + J_1(p) = p + \bar{p}$

In determining logical functions from given truth tables it is necessary to be familiar with some systematic techniques. However, one should not overlook the importance of the truth table inspection before general methods are applied. If a special pattern is noticed, the required function can be written directly from the truth table.

A general method for determining logic equations in terms of J operators, defined by truth tables, is as follows:

1) Write down separate J *minterms* (a minterm of n variables is the Boolean product of these n variables with each variable present in either its true or complemented form) for each non-zero term of the function, making the order of J operators equal to the truth value of the corresponding variables. If this term is 1, multiply the generated minterm by 1.
2) To produce the complete equation, realizing the given function, add all the J minterms.
3) Simplify the equation.

Example:

Determine the logic equation for the function f defined by the truth table as shown below.

p	q	f	*J minterms*
1	1	1	$J_1(p) \cdot J_1(q) \cdot 1$
1	2	1	$J_1(p) \cdot J_2(q) \cdot 1$
2	1	1	$J_2(p) \cdot J_1(q) \cdot 1$
2	2	2	$J_2(p) \cdot J_2(q)$

The portion of the truth table not shown contains all zeros under f.

$$f = J_1(p) \cdot J_1(q) \cdot 1 + J_1(p) \cdot J_2(q) \cdot 1 + J_2(p) \cdot J_1(q) \cdot 1 + J_2(p) \cdot J_2(q)$$
$$= J_1(p) \cdot 1 \cdot [J_1(q) + J_2(q)] + J_2(p) \cdot [J_1(q) \cdot 1 + J_2(q)] \ldots$$
$$= J_1(p) \cdot 1 \cdot q + J_2(p) \cdot q$$
$$= [J_1(p) \cdot 1 + J_2(p)] \cdot q$$
$$= p \cdot q$$

To simplify the binary logic functions, the Veitch diagram technique is often more convenient and faster than algebraic manipulation. It was found that the Veitch diagrams can be extended, to ternary logic:

Veitch Diagrams

Binary

	a	a'
b	3	1
b'	2	0

Ternary

	p	p'	p''
q	8	5	2
q'	7	4	1
q''	6	3	0

The Veitch diagram rules for ternary logic, compared to those for binary logic, are as follows:

1) In binary Veitch diagrams, the truth values assumed are $a = 1$ and $\bar{a} = 0$; similarly in the ternary diagrams $p = 2$, $p' = 1$, and $p'' = 0$. The most significant variable in this example is at the top of the diagram for both ternary and binary diagrams.
2) Any binary function transferred from the truth table to the Veitch diagram is marked by 1's in the corresponding cells. Since the ternary function is defined in its truth table by either 2's and/or 1's, the corresponding cells are also marked by either 2's or 1's.
3) If a cell in the binary Veitch diagram can be either 1 or 0 (i.e., a corresponding minterm is redundant) the cell is marked by X. The cell is redundant in the ternary Veitch diagram only if it can be either 2 or 1 or 0; in this case, similarly, it will be marked by X (i.e., the cell can take any convenient truth value for the function simplification purposes). Any cell of the ternary Veitch diagram can assume only one truth value or be redundant.
4) For any mechanized binary function, the existence and the non-existence of the output corresponds to the truth values 1 and 0 respectively. In the case of the ternary function, the existence of the output corresponds to either 2 or 1, and the non-existence of the output to 0. A function producing 2 or 1 output will be denoted by f_2 and f_1 respectively. If the truth table defining a function contains 2's and 1's, the total expression for the function will be $f = f_2 + f_1$.

Example:

Use the Veitch diagram for the minimization of the function defined by the truth table in the previous example.

p	q	f
1	1	1
1	2	1
2	1	1
2	2	2

	p	p'	p''
q	2	1	0
q'	1	1	0
q''	0	0	0

Inspecting the Veitch diagram one can see that the pattern is the same as of the matrix defining the ternary intersection. That is, $f = f_1 + f_2 = p \cdot q$.

To become proficient in ternary Veitch diagram techniques, one should first be able to recognize as many different ternary Veitch patterns as possible.

To translate a ternary Veitch diagram into a disjunctive form consisting of J minterms, proceed in the following manner:

1) If a pattern can be expressed in terms of *intersection*, *union*, and/or *cycling* connectives such that

$$f = f(p, q \cdots, s)$$

then
$$f = J_2 [f(p, q, \cdots, s)] + J_1 [f(p, q, \cdots, s)] \cdot 1$$

Example:

	p	p'	p''
q	2	2	2
q'	2	1	1
q''	2	1	0

Since the Veitch diagram is of the function $f = p + q$, $f = J_2(p + q) + J_2 (p + q) \cdot 1$

2) If the pattern of a function is not readily recognizable, combine 2's and 1's separately into the simplest expressions using the same technique as in the use of the binary Veitch diagrams. If $f_2 = f_2(p, q, \cdots, s)$ and $f_1 = f_1(p, q, \cdots, s)$ then $f = J_2[f_2(p, q, \cdots, s)] + J_2[f_1(p, q, \cdots, s)] \cdot 1$

Example:

	p	p'	p''
q	2	1	1
q'	2	0	0
q''	2	0	0

From this pattern, we get $f_2 = p$ *and* $f_1 = q(p' + p'')$, $f = J_2(p) + J_2[q(p' + p'')]$

3) For expressing f_1, consider any cell with 2 to be a redundant term since $2 + 1 = 2$.

$$\begin{matrix} 2\ 1\ 1 \\ 2\ 0\ 0 \\ 2\ 0\ 0 \end{matrix} = \begin{matrix} 2\ 0\ 0 \\ 2\ 0\ 0 \\ 2\ 0\ 0 \end{matrix} + \begin{matrix} 1\ 1\ 1 \\ 0\ 0\ 0 \\ 0\ 0\ 0 \end{matrix}$$

Using this property for the above example,

$$f = J_2(p) + J_2[q(p' + p'')] \cdot 1$$
$$= J_2(p) + J_2(q) \cdot 1$$

All the described methods of generating logic equations for the functions defined by truth tables can be used for any number of variables. The complexity of handling a higher number of variables does not appear to be greater than the equivalent problem in the binary logic. The fact that the number of different ternary logic functions is much greater than for the same number of binary logic functions does not make the ternary techniques proportionally more complicated.

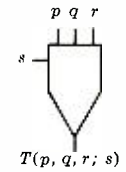
THE TERNARY CONDITIONED-DISJUNCTION

In computer manufacturing, it is more economical and convenient to use only one type of circuit as a basic logic element. For instance, in the present digital computers, to mechanize three basic logic connectives—*and*, *or*, and *not*—we use either *nor* or *nand* logic elements. All the ternary functions can be mechanized by a single logic element.[1] This basic element is a conditioned-disjunction. The notation symbol for the ternary conditioned-disjunction is

$$T(p, q, r; s)$$

and its functional definition can be stated as p, q, or r if $s = 0$, $s = 1$, or $s = 2$, respectively:

s	$T(p, q, r; s)$
0	p
1	q
2	r



The general expression for the ternary function of n variables in terms of T operators is:

$f(p, q, r, \cdots, s) = T[f(0, q, r, \cdots, s), f(1, q, r, \cdots, s), f(2, q, r, \cdots, s); p]$

where $f(0, q, r, \cdots, s)$, $f(1, q, r, \cdots, s)$ and $f(2, q, r, \cdots, s)$ are the ternary functions of $(n - 1)$ variables. This result follows directly from the Post algebra and the definition of the T operator.

A simple method has been developed for mechanizing ternary functions using T operators. To the author's knowledge, the method appears to be novel since no reference describing it had been found. The procedure is as follows:

1) Translate a truth table, defining a ternary function, into its equivalent Veitch diagram;
2) Write all the $n!$ possible equations in terms of T operators, where n is the number of variables; and
3) Select the equation of the minimal form.

For example, a general Veitch diagram for a ternary function with two variables is shown below:

	p	p'	p''
q	a_{11}	a_{12}	a_{13}
q'	a_{21}	a_{22}	a_{23}
q''	a_{31}	a_{32}	a_{33}

$f(q, p)$

	p	p'	p''
q			
q'			
q''			

$f(p, q)$

	p	p'	p''
q			
q'			
q''			

The two forms of the function can be written: $f(q, p) = T[T(a_{33}, a_{23}, a_{13}; q), T(a_{32}, a_{22}, a_{12}; q), T(a_{31}, a_{21}, a_{11}; q); p]$

$f(p, q) = T[T(a_{33}, a_{32}, a_{31}; p), T(a_{23}, a_{22}, a_{21}; p), T(a_{13}, a_{12}, a_{11}; p); q]$

The above functions, in logic diagram form, are shown in Fig. 1.

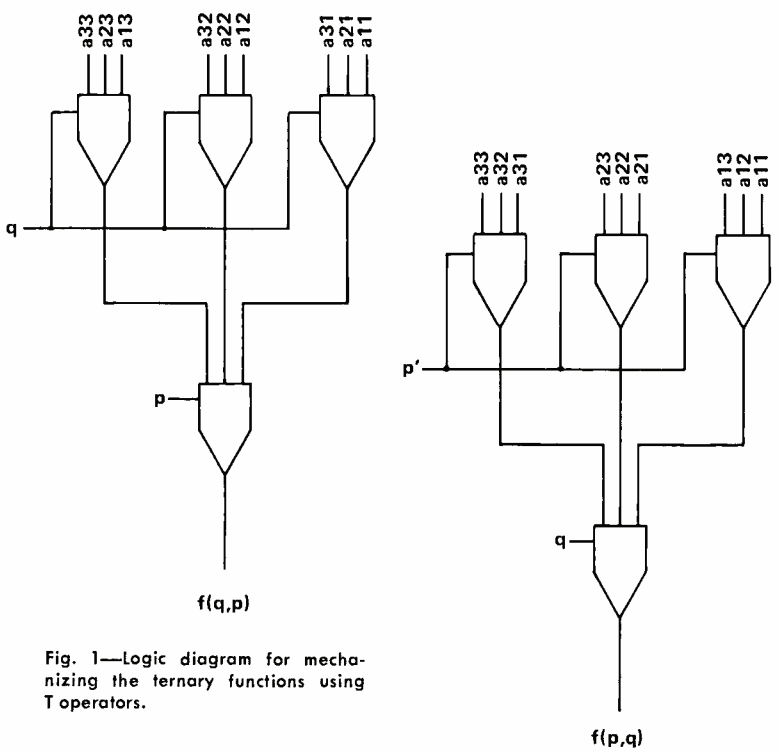


Fig. 1—Logic diagram for mechanizing the ternary functions using T operators.

As can be seen in the Veitch diagram and the determined equations, writing down the required equations is very simple. Starting from the right bottom corner of the Veitch diagram (i.e., from the minterm designated by the ternary zero) one may proceed either up or to the left producing $f(q, p)$ or $f(p, q)$, respectively. Since $f(q, p) = f(p, q)$ the one of the simpler form is selected. With some experience in this technique, it will not be necessary to try all the possible solutions, since some Veitch diagram patterns suggest the factoring ways producing a minimal form.

CONCLUSIONS

Essentially, the system of the ternary logic is characterized by a rather close analogy to the systems of Boolean algebra, normally used for the case of the binary logic. One of the more outstanding differences is that in the ternary system the number of the different equations is considerably higher than the number of the binary equations for the same number of variables.

Also, the number of possible ternary operators is higher than the number of binary operators, but in both cases there are single operators which provide complete logic systems. As a whole, the difference between the two logics are predominantly of quantitative nature. After one becomes familiar with some fundamental principles of a multi-valued logic, the ternary logic does not create any conceptual difficulties. However the manipulation of the ternary logic is more complex than that of the binary logic, and probably will remain so regardless of what new switching algebra techniques are developed in the future.

The commonly accepted opinion that the number of components in a ternary computer will be smaller than that used in a binary computer is based on considerations related to the storage of data by ternary elements. Therefore, the use of the ternary numerical system in digital computers would be justified only if both 3-state switching and memory elements were available. With the recent technological advances in various semiconductor devices, magnetic cores, and cryogenics, there are indications that the circuit design of simple and reliable ternary devices is feasible.

The author has completed the logic design of the following ternary functions: a tri-stable memory element ("tri-flop") for store, trigger, and shift-register applications, timing-pulse generators, comparators, adders, and data transfers between registers. A T operator was used as a basic switching element throughout the exercise for the application of the described ternary logic, and no unusual problems were encountered.

The same T operator can be used as either a 3-state or 2-state switching device, this property being controlled by truth-functional constants associated with T operators. It is an extremely useful property of T operators since some control signals should exhibit two states only.

Although an optimum mechanization of the ternary full-adder has not been achieved, the ternary adder compares very well with the binary adder (ten T-elements versus nine *nor*-elements). This is significant because the increase in range in changing from binary to ternary notation with the same number of digits, n, is $(3/2)^n$.

In selecting a numerical system, one should also consider the cost and speed of conversion to and from the decimal system. Any binary conversion algorithm can be modified for the ternary conversion, and, in most of the cases, the execution of ternary conversion is faster.

There exists a ternary code, referred to as a symmetric code in this paper, which does not require the designations of algebraic signs. The full adder for this code is more expensive than the adder for the straight ternary (14 versus 9 elements). However, the arithmetic can be performed without sign logic or subtractive complementing and sign change correction.

In recent years, many papers have been appearing on ternary logic. The subject is becoming of greater interest to the logicians recognizing many advantages of the system. It is still too early to speculate whether the computer industry will ever switch from binary to ternary logic. An extensive evaluation program is necessary to determine whether the use of the ternary system for digital computers would be justified economically.

Although an engineering team designing their first ternary computer today could have some problems, these would be considerably simpler than the problems encountered by the team designing the first electronic digital computer a mere 20 years ago.

BIBLIOGRAPHY

1. E. L. Post, "Introduction to a General Theory of Elementary Propositions," *American Journal of Mathematics*, Vol. 43 (1921) pp. 163-185.
2. J. Lukasiewicz, "On Three-Valued Logic," *Ruch Filozoficzny*, Vol. 5 (1920 pp. 169-171.
3. D. A. Bocvar, "On a Three-Valued Calculus and Its Application To The Analysis of Contradictions," *Matematicheskij Sbornik*, Vol. 4 (1939) pp. 287-308.
4. A. Rose, "Conditioned Disjunction as a Primitive Connective For the M-Valued Propositional Calculus," *Mathematische Annalen* (1951) pp. 76-78.
5. A. Turecki, "The Use of the Ternary Numerical System in Digital Computers," a thesis submitted to the Moore School of Electrical Engineering, University of Pennsylvania (June, 1963).

COMPUTER SOFTWARE CONTROL SYSTEMS

The development, present uses, and future applications of computer control systems are described. Starting with a definition of the control system itself, several other terms related to computer software are defined. Both batch-processing and time-sharing systems are covered with particular attention to extending their usefulness for future, more complex systems.

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IN COMPUTER TERMINOLOGY, a *control system* is a program that produces an environment for user programs to operate in a computer. Generally, the purpose of a control system is to make the use of the computer easier and more efficient. Such a system constitutes a dynamic interface between hardware and user program. These systems are also sometimes called operating systems, monitors, supervisors, or executive programs. Control systems are as old as computers, and vary in size from a few simple routines to very elaborate software systems containing several hundred thousand instructions that may represent an investment of hundreds of man years of effort.

The term *operating system* today usually implies all general software supplied by the manufacturer with a line of computers. Rudimentary beginnings of operating systems were sub-programs for floating point arithmetic, sets of library routines, special print routines, and complete interpretive systems that provided the user with a new set of simple and easy-to-use commands.

Compilers transform defined source languages (such as FORTRAN) into a set of machine instructions, and are not considered as part of the control system. *Language systems* form an entire class by themselves in the computer sciences.

FIRST GENERATION COMPUTERS

First generation computers could operate only on one program at a time. As computers became more expensive, machine operators could not efficiently schedule the machines, and control systems began to assume some of the tasks of the operator: accepting jobs for processing, initiating the loading procedures for each program in sequence, and providing for diagnostic memory print-out in case of unexpected user program failure.

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SECOND GENERATION COMPUTERS

Second generation computers made it possible to operate input and output concurrently with execution of instructions that use high-speed memory only. Control systems assigned and scheduled buffers for the input and output, initiated the input output operation, and signaled its completion back to the using program.

Frequently, it is not possible to do worthwhile work, such as arithmetic involving high-speed storage only, during the input and output cycle in a given program. Better use of a computer with respect to concurrent input/output can be made if several programs are at hand for operation. The basic philosophy is to have two or more programs loaded in memory. The first program operates until it has to perform input or output; after initiation of input or output, the control is transferred to the second program while the first program waits for its input or output to complete. It is obvious that with a good mix of programs, the total time of completion for these programs, multiprogrammed, is less than that of executing them in sequence.

THIRD GENERATION COMPUTERS

Third generation control systems provide the management of concurrent input and output, the switch between multiple programs and the allocation of resources with respect to time, memory, and input or output devices. A further major feature of third generation software is the availability of a *data management* function, that facilitates the use and access of files to the user. Files are sets of information stored on auxiliary devices such as tapes and discs. Files may be divided into a number of records which are individually accessible. The more comprehensive systems allow the user to work with his files on a logical level; that is, he can refer to his files by name regardless on which storage medium they reside and how they are physically recorded.

Third generation hardware and software have become so complex that "stand alone" user programs are practically impossible and very uneconomical. A certain basic amount of software for the control system is a prerequisite for operating a computer facility.

Control systems divide into two major categories: *Batch-Processing Systems* and *Time-Sharing Systems*. The conceptual distinction comes from their difference in access methods, scheduling, and resource allocation. The practical distinction lies in the higher complexity of time-sharing systems caused by new types of equipment and software techniques.

BATCH-PROCESSING SYSTEMS

In a batch-processing system, jobs are accepted and scheduled to run to completion in the sequence in which they arrive. If the system provides for multiprogramming, several programs may be loaded into the computer and then executed in the order of their assigned priority and within the constraints of the available resources (such as memory and storage devices).

Task Management

The control system lets the first program execute until it starts an input/output operation, then it transfers control to the program with the next highest priority until either it initiates input or output or the first program has completed its input or output. At that time, control goes either to a program with lower priority or to the first program with the highest priority. A program that is either running, or scheduled to run, is called a *task*. Tasks may perform several jobs such as compile, load, or execute. Description of the jobs are expressed in a job control language; the information about the jobs is accumulated in the so-called job stream.

The *task management* of the control system allocates the necessary amount of high-speed memory, calls in overlays of programs, and provides for memory protection to prevent destruction of information of a task by another task.

Data Management

Data management gives the user two important facilities: file handling and record processing. When a user wants to work with a file, he "opens" the file by means of a command to the data management system. The data management checks the allocated peripheral devices on which the file is located, and if they are detachable storage media, such as tapes, it issues mounting instructions to the operator. Detachable storage media have tables of contents and labels that are checked by the system to insure that the proper file is mounted at the input or output device. The data management further checks the type of file and in which manner it can be accessed.

In most systems, files can be organized and accessed according to either the *direct-access method* or the *sequential-access method.* The basic direct-access method allows the user to address records and tracks on storage devices directly. The user specifies how the records are arranged on the device and he, in essence, provides the searching, read, and write instructions. Data management provides the dynamic allocation of buffer space. The sequential-access method facilitates the reading and writing of records which are strictly in sequential order on a physical device such as magnetic tape. The *indexed sequential method* associates a key with each record of the file and recognizes the logical order of the keys or records. It is therefore possible to read, write, insert, or delete records by referring to their keys. The system will perform the operation regardless of where the records are physically placed. It is not necessary for the user to utilize the space that becomes free after deletions or concern himself with procedures to handle overflow incidents that occur by insertions into a full track. Notice that logical order and physical order of records on the storage device generally do not coincide.

It is mainly the development of data management functions and multi-tasking that third-generation batch-processing systems have achieved for the user. Newer systems also provide *emulation* as concurrent tasks in the system operations. Emulation is the simulation of another computer and is usually accomplished by using special hardware and software.

The functions that batch-processing control systems provide to ease the user's work are not without cost and must be paid for with a certain amount of overhead. The overhead shows in two ways:

1) The more functions the control system provides, the more space is needed. Present systems occupy anywhere from 5% to 25% of high-speed memory during operation.
2) The control system needs time to check on legitimacy of accesses, search for records, and switch between tasks.

If the tasks are well balanced with respect to input/output, the switch between them produces additional machine capacity through parallel operation far in excess of the time used by the control system. There are certainly cases where systems use an undue amount of time for unproductive work, but generally speaking, present batch-processing control systems provide effective computer use that would not be possible if jobs were processed in the old-fashioned manner of running only one job at a time and under the exclusive control of a human operator.

TIME-SHARING SYSTEMS

Time-sharing control systems have been developed during the last two or three years. They represent the most complex control systems to date because they perform most functions of the batch-processing systems in addition to the interactive time-sharing functions. Time-sharing systems provide:

1) Remote access to the computer simultaneously for a large number of remote users;
2) A scheduling technique that favors short jobs for fast turn-around;
3) On-line files privately or generally accessible to users at the terminals at all times.

Very often during the program-building and checkout phase, only small corrections or additions are made to a program. Changes punched into cards, submitted

70/15 PROGRAMMING SYSTEMS

Loader Routines
Input/Output Control
Utility Routines
Test Routines
Report Program Generator
Autoflow
Assembly System
Sort/Merge Generator(s)
Library Maintenance Routines

70/25 PRIMARY OPERATING SYSTEM

Executive
File Control Processor
Peripheral Control System
Job Control
Report Program Generator
Macro Assembly System
Sort/Merge
1401 Simulator
Diagnostic Routines
Library Maintenance Routines

70/35-45-55 PRIMARY OPERATING SYSTEM

Executive
File Control Processor
Peripheral Control System
Job Control
Report Program Generator
COBOL (32K)
Macro Assembly System
Sort/Merge
Library Maintenance Routines
Diagnostic Routines

70/35-45-55 PRIMARY COMMUNICATIONS ORIENTED SYSTEM

Supervisor, including macros for multi-channel communications program linkage
Peripheral Control
Snapshot macros
Program loaders

70/35-45-55 TAPE OPERATING SYSTEM

Executive
File Control Processor
Media-to-Media Conversion Programs
FORTRAN IV
Macro Assembly System
Monitor Control
Report Program Generator
COBOL
AIDS—Automatic Integrated Debugging System
Sort/Merge Generator
Library Maintenance Routines
Diagnostic Routines

70/35-45-55 TAPE/DISC OPERATING SYSTEM

Executive
File Control Processor
Media-to-Media Conversion Programs
FORTRAN IV
Macro Assembly System
Monitor Control
Report Program Generator
Communications Control (multi-channel)
COBOL
Sort/Merge Generator
Library Maintenance Routines
Diagnostic Routines
AIDS—Automatic Integrated Debugging System

70/45 BASIC TIME SHARING SYSTEM

Control Program
Command Language
Edit Language
Interactive FORTRAN
Desk Calculator Mode
FORTRAN Syntax Checker
Switching Module

70/46 TIME SHARING OPERATING SYSTEM

Executive
Data Management System
Diagnostic Routines
Job Control
Command Language Processor
FORTRAN IV
COBOL
IDOL Interactive Debugging-Oriented Language
Report Program Generator
Assembler
Conversational FORTRAN
Conversational FORTRAN Syntax Checker
Conversational COBOL Syntax Checker
Conversational Assembler Syntax Checker
Conversational Desk Calculator
Conversational Text Editor
Linkage Editor
User File Maintenance Routines
System File Maintenance Routines
Sort/Merge
Test Data Generator

MANAGEMENT SCIENCE SYSTEMS APPLICATION PROGRAM PACKAGES

Systems Flow Simulator
Multiple Project Planning and Resource Allocation
PERT
APT Numerical Control Language
EXCEL Civil Engineering System
Statistical System
Matrix Operations
Square Root and Transcendentals
Linear Programming System
Market Forecasting System
SSS-70 Scientific Subroutines System
Decision Table Program

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to a batch-processing system usually causes delays for hours in a busy installation despite the fact that actual machine time needed for the job may only be a few seconds. In time-sharing, the user enters commands from his terminal which may be either a teletype or a video display.[1] The system accepts the command and gives the user a few hundred milliseconds of processor time. If the user's job is short and finishes in that time, he will receive the answer within seconds at his terminal. After receipt of the computer response, the user will prepare for the next request. Considering that users normally take from 10 to 30 seconds "think" time between entering commands and assuming that the average command takes only a fraction of a second to execute, it is possible to service a good number of users simultaneously. Internally, of course, the requests are taken serially, but due to the actual short execution time, responses occurring within seconds give users the impression that they have simultaneous access to the processor.

From a control system point of view, time-sharing systems differ from batch-processing systems by their typical number of active tasks. In a batch-processing system, one usually thinks of three to six concurrently active tasks, whereas in a time-sharing system, 30 to 100 users are considered typical.

Relocation of Memory

It is obvious that all user programs cannot share memory at the same time without making the allowable program size prohibitively small. To permit use of any sensible program size requires swapping of programs between auxiliary storage and high-speed memory. This demands fast input and output to and from a high capacity storage device and also an efficient means for relocating programs. Efficient relocation is significant because the control system cannot easily assign the same place in memory for each of so many programs every time a swap takes place.

The difficulties of relocation can be partly overcome through software and by restricting maximum program size and limiting the language-processor capability. In currently available restricted systems, programs may not exceed from about 4,000 to 8,000 bytes. Restricting the capability to one or two language processors saves space because all users can share the same copy of the language processor in memory. Language processors in these systems are considered part of the system and not of the user program.[1]

The Translation Table

In general, users of time-sharing systems must have the flexibility to use any language processor, any program prepared at the terminal, or any executable object module, regardless of origin. A better and advanced solution to the relocation problem is a combined hardware software system which works as follows. Memory is divided into blocks of equal size; each program will always consist of an integral number of such blocks. Every effective address generated in an instruction goes through a table look-up process by the hardware before the data is fetched from physical memory. The machine uses the first digits or bits of the address for look-up in this *translation table*. For example, if blocks are one thousand characters long, the address is taken with the exception of the three rightmost digits which signifies the block number. The table contains, for each logical block number, the actual physical block number where the control system has placed the block of the program. The control-system software sets the table according to the correspondence between logical block number as the user program sees it and the physical block number as the system has assigned it at the time of execution.

To relocate a program necessitates only resetting the block numbers in the table. The hardware automatically performs the translation by look up in the table for every address encountered. By this method, blocks of a program may be placed in memory discontiguously because every address is analyzed and translated, and it does not matter where a particular block is located in physical memory.

By means of the translation table, the user can address in his own world, and the system can place the program anywhere in memory it sees fit. A table serves only one user. When another user obtains execution, the machine works with *his* table. This protects users mutually since their translation table settings do not contain any block number assigned to another user, and therefore it is impossible to accidentally (or maliciously) destroy information of another user.

Paging

This method yields one other advantage. The size of memory that a user may address depends only on how many block entries are allowed in the translation table. Because a program can never address all blocks at once during execution—strictly speaking it needs only one block at a time—only a small portion of the total program needs to be physically present in memory for the duration of a processing period of a few hundred milliseconds. Therefore, the control system may load only a few blocks of the program, but set a warning control bit in the translation table for blocks not presently loaded in memory. Any time the program in execution tries to access a block not in memory, an interrupt will result. The control system may then obtain the missing block from auxiliary storage and processing of the program can continue.

This method of handling memory allocation of programs is called *paging*, and the above mentioned blocks are referred to as *pages*. The fictitious large address space that the user may have is called *virtual memory*. If a user operates in a virtual memory that is larger than the physical memory available in the equipment, no more than a fraction of his program will be loaded in physical memory at any time. The virtual memory concept practically replaces the need for overlays. The user just extends the address space and leaves it to the system to perform overlays automatically by paging.

Task Management

Task management in a time sharing system must accommodate a large number

of users, provide protection, and allocate resources dynamically. The resource allocation is further complicated by the paging mechanism since input and output to other peripheral equipment must be coordinated with the swapping of programs. Blocks of user programs that are receiving input cannot be swapped even if the rest of the program is made inactive during execution of another user program. Some implementations of paging mechanism have run into significant difficulties from an efficiency point of view.[3] The answer to efficient paging lies in proper choice of algorithms and auxiliary storage devices. Devices such as discs are not feasible for paging.

The scheduling of tasks is an important factor in time sharing. As mentioned earlier, one of the purposes of time sharing is to give short jobs preferential treatment. A common method is the so-called round-robin. In the round-robin scheduling system, the servicing processor grants a certain quantum of time—in the order of half a second—to each requesting task or user. If the request is less than the time quantum, the request is completed and the user receives a response. If the request cannot be finished within the time quantum, it is interrupted and the next user gets a time quantum, and so forth. A long job is obviously delayed since it is done in installments of time quanta and time elapses between installments for time quanta given to other users waiting.

In practice, the round-robin scheduling is always modified since programs may not be able to use their full time quantum, either because they need input/output or because part of their program is not immediately available in memory due to paging. Relatively complicated scheduling algorithms result by considering optimization of time, space, and transmission to auxiliary storage. Further, certain parameters (such as the number of active users leading to adaptable scheduling algorithms) may change with time.[2]

Data Management

The *data management* of a time-sharing system maintains a catalog for all user files, protects them when they are private and guards the procedures of file sharing for files that users have declared as sharable. All file creating, accessing, and updating can be done either directly from a terminal by specific commands or by executing programs in the form of specific instruction sequences (macro calls). All access methods implemented for batch-processing systems, predominantly the sequential and indexed sequential, are available in time sharing.

Larger Systems

Valuable program debugging features are implemented in larger time-sharing systems. *Interactive compilers* facilitate source-language debugging by allowing 1) to compile a statement at a time, 2) to execute a statement at a time, and 3) to display or print specific variables on demand.[1]

Special Commands

Special commands help to debug running object programs. By entering commands from his terminal, a user may stop the execution of a program at any particular time and at any particular location; he can then make changes to the program, display or print contents of registers or values of variables, and resume the execution of the program. Conditional stops can be placed into the program such that the stop occurs after a certain point has been passed a specified number of times or a certain variable has obtained a given value. All these commands can be given in absolute or symbolic if symbol tables are available to the system.[2]

The Text Editor

One major language processor, the *text editor*, is implemented for almost all time sharing systems. The text editor allows to enter and modify text, or more precise, character strings. Commands facilitate the insertion, deletion, movement and replacement of character strings. Locations in the text can be specified by line number, character number in lines and by content. Text editors are the major tool for changing source language during the process of debugging.

FUTURE TRENDS

From past experience, it is evident that software control systems will be even more critical for the performance of future computer systems than for present ones. As hardware becomes more complex, a single user can neither use a system efficiently by himself nor can he acquire the necessary skill to run a system without a control system supplied with the hardware.

Future systems will emphasize more parallel operation using multiple processors for more efficiency and higher through-put. Processors and blocks of high-speed memory will be considered resources like any other device. The concept of the all-knowing central supervisor will change to a concept of multiple resources that are scheduled according to availability and ability to perform a certain task. Practically every system will have some kind of remote access devices attached, challenging the dominance of card-handling devices in today's computer installations. Systems will be required to operate 24 hours a day, seven days a week. There will be multiples of each component to allow the system to fail soft by maintaining the basic function in case some components are temporarily disabled. Better methods and equipment will be required to guarantee safety of on-line files that are vital to individual users and businesses. Automatic file backup and redundant recording, the two possible solutions to this problem, demand significant development and consideration in future system design. New concepts such as the inclusion of files into virtual memory are considered in some advanced systems.[4,5]

Briefly, the user references a location in a segment or file. He has a large number of segments available to him, maybe a million, and each segment may have up to a million words. The user can address in a two-dimensional way by specifying the segment and the location in the segment. Any time he refers to another segment (file) the system will automatically link and load that segment to allow execution of his program. This is different from the conventional concept where the user thinks of files as inactive information in storage and where programs in execution must "read" files to use them. In the above concept, one simply addresses anything in the segments (files) and the system accesses it. This puts a heavy burden on the system, but it is logically, and from the user's viewpoint, much superior to the conventional file concept.

For improved speed, parts of control systems will be programmed in microinstruction using read-only memory techniques. Micro instructions in read-only memory are usually three to five times faster than normal instructions due to simplification in statiscizing and reduction of main memory accesses.

Generally, the emphasis in future development of software control systems will be to serve the main objectives of attaining higher speed, reliability, and maintainability, which present quite a challenge to today's designers.

REFERENCES

1) Reference Manual, 70-45-601, *The RCA Spectra 70/45 Basic Time Sharing System*, (Jul. 1967)

2) *The RCA Spectra 70/46 Time Sharing Operating System*, System Objectives and Facilities, (Apr. 1967) Processor Reference Manual, 70-46-601, *Spectra 70, 70/46*, (Apr. 1967)

3) N. R. Nielson, "The Simulation of Time Sharing Systems," *Communications ACM*, (Jul. 1967)

4) J. B. Dennis, "Segmentation and the Design of Multiprogrammed Computer Systems," *IEEE International Convention Record*, New York (1965) Part 3

5) V. A. Vyssotzky, F. J. Corbato and R. M. Graham, "Structure of the Multics Supervisor," *AFIPS Conference Proceedings*, Volume 27, Part 1 (1965)

INTEGRATED CIRCUIT PACKAGING FOR ADVANCED COMPUTERS

The new chip technology has focused equipment designers' attention on packaging techniques for modern computers. Protection, interconnection, and configuration concepts for integrated circuits are evolving to meet changing performance demands. This article presents several solutions already in development to solve the varied problems of this discipline.

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THE GOAL of the packaging engineer is to protect, connect, cool and house the circuits that make up a computer. His effectiveness can be measured directly in the cost, performance, maintainability, and reliability of the completed machine. The relative importance of proper packaging can be seen from an examination of the central working portion of a modern high-speed computer. All of the integrated circuits required to build a Spectra 70/45 processor will fit in a thimble; the 50,000-to-1 increase in volume is required by today's packaging limitations.

ELECTRO-MECHANICAL PROBLEMS

The mechanical design of the equipment package has a direct bearing on electrical performance. The newer high-speed circuits are now fast enough to have the propagation delay of a foot of cable represent a large percentage of the circuit switching speed. This delay can no longer be tolerated; cable lengths must be reduced. The fast risetime pulses and the minimum signal levels make the circuits more susceptible to noise and crosstalk. Transmission line interconnections are used to reduce the noise and crosstalk. The integrated circuits are sensitive to maximum temperatures and to temperature differences; thus, an adequate and constant-cooling system is an integral element of a high speed computer.

Maintainability and reliability are essential considerations in the proper design of a high speed machine. In general, maintainability is promoted by having easily removed modules. The logic contained on a module should be readily isolated and identified as working or not. The module should be small enough to be repetitive and available as a spare part. If the module is expensive it should be capable of being readily repaired and returned to stock. Maximum reliability requires nonpluggable connections, all joints soldered or welded, and circuits spread out to minimize thermal problems.

The design techniques that would result in maximum performance usually conflict with those that would reduce cost. For example, a large module improves reliability and maintainability, but the larger the module the more likely it is to be unique. This approach leads to 100% stocking of replacement parts. With high reliability systems, a surprising problem arises: maintenance calls become so rare that adequate training of troubleshooters is impractical. Thus, there must be a trade-off between 1) the use of large plug-in modules where fault isolation time can be reduced, and 2) increased down time while inexperienced troubleshooters search for the problem in a nonmodular system.

CIRCUIT PROTECTION

Throughout the packaging of a computer system, the packaging engineer must evaluate the effects of one design choice on the other machine parameters. The design of a very high-speed machine will require the highest speed circuits. These circuits will generate more heat, be more sensitive to temperature differences, and will require the use of transmission lines for interconnections. Similarly, attempts to reduce the number of types of spare parts will result in inefficient use of the building blocks and a physically larger system.

Design compromises are reached by handling five interrelated levels: components, circuits, functions, subsystems, and systems. Integrated circuits have removed the component compromises from the jurisdiction of the equipment packaging engineer. All the components required for computer circuits are diffused into flakes of silicon and interconnected to become circuits by vapor depositing aluminum conductors on the silicon surface.

The aluminum metalization is vapor deposited approximately 6,000 angstroms thick and 2 mils wide. The conductors are about 2 mils apart. The aluminum which is deposited on top of the silicon chip is unprotected from corrosive atmosphere in this state. The accepted method of providing protection from chemical attack has been to seal the silicon chip in an atmosphere of pure nitrogen. To verify that the package is properly sealed, the unit is exposed to a high pressure atmosphere of helium or a radioactive tracer gas. The gas is then detected when it leaks from a faulty unit under low pressure. These leak detectors are capable of detecting leaks as small as 10^{-10} cc/sec. The established acceptable leak rate for the integrated circuit packages is 10^{-7} cc/sec.

The early attempts to provide a plastic package in place of the ceramic package met with failure because of the testing methods used. The absorption of the helium by the epoxy makes it difficult to determine whether there really is a leak.

There have been attempts made by various means to provide a glass coating over the surface of the chip. Sputtering, vapor deposition, and chemical reactions have been tried with various degrees of success. The method developed by the RCA Laboratories and announced as the "Decal Chip" seems to solve the deposition problems, provide adequate hermetic seal, and completely avoid problems created by differences in thermal expansion characteristics.[1]

CHIP PACKAGING

TO-5 Package

The integrated circuit chips are placed in a ceramic package 500 times their volume to bring connections (which were 6 or 7 thousandths of an inch apart) to a widely spaced grid more compatible with normal printed-circuit dimensions. The package also provides an

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environmental seal and a means of handling the circuit. The TO-5 package (Fig. 1) was an early contender for integrated-circuit packaging because of past experience sealing transistor cans. However, with the leads all existing on one hidden surface, aligning the pins with holes for mounting and for the simultaneous unsoldering of all joints for removal was extremely difficult. Also, the tight circle of leads prevented printed connections through the pattern and forced layouts with packages widely spaced.

Planar Flat-Pack

Fig. 2 illustrates the planar flat-pack with leads along two opposing sides spaced on 0.050-inch centers. These circuits can be surface mounted, or by reforming the leads, they can be mounted through plated holes in the printed boards. The integrated circuits can be removed from this form either by unsoldering each lead or by clipping all the leads. The flat-pack also permits connecting leads to run through the pattern in one direction. To print wires between the flat-pack leads, these leads are usually placed in an off-set pattern.

Dual-In-Line Package

A more universally acceptable package has begun to replace the 14-lead flat package. It normally has seven leads along each long side spaced 0.100 inch (Fig. 3). Despite its slightly larger size, this dual-in-line package can be arranged on a printed card more efficiently than can the planar lead flatpack.

LID Package

Fig. 4 shows the leadless inverted device (LID) which has had limited acceptance. This package provides a U-channel in which the silicon chip is mounted at the inside center, and the legs of the channel are divided into pillars. Metal deposited on the channel is etched into individual conductors leading from the chip to the surface of the pillars. This unit can now be inverted and either soldered or ultrasonically bonded to a printed board. The pillars are normally on 0.025-inch centers and require more sophisticated printed-board techniques for adequate interconnections. This technique provides no hermetic seal and little physical protection.

Device Connections

So far no comment has been made about the methods of connecting the conductive pads on the silicon chip to the leads of the package in which it is mounted. The earliest packages had the silicon chip bonded to the base of the package with the circuit facing up. One-mil diameter gold wires were then thermocompression bonded to the pads on the silicon and to the external connecting lead (Fig. 5). Because the intermetallic diffusion products of gold, aluminum, and silicon are brittle and lead to device failures, the gold wires were replaced with aluminum wires. The thermo-compression bonded joints are made one at a time by an operator working with the aid of a microscope. The process is very costly and has a low yield.

Face-Down Bonding

Attempts to overcome the lead bonding cost have resulted in various forms of face-down bonding. Bumps or pillars are built up on either the silicon chip or the mating substrate. The silicon chip is then flipped onto the substrate (Fig. 6) so that the bumps and the conductive pads are adequately aligned. The application of vertical pressure and horizontal ultrasonic relative vibration causes heat buildup and the welding of all joints simultaneously. Some variations provide a solder coating and apply heat to join the parts by reflow solderings.

Face-down mounting of chips has been successful in pilot runs and will soon be the standard mounting for silicon chips within any of the standard packages. Mounting silicon circuits directly on circuit boards seems to be a natural extension of this technique. A number of independent efforts are being made in other companies to develop this ability. Two basic problem areas exist which prevent immediate use of uncased chips:

1) Present testing methods require the addition of the standard packages to make suitable electrical contact. Therefore some revision in probing methods will be required to test the chip without a package.
2) The hermetic sealing of the chip is difficult to achieve; however, the technique which uses application of glass to the silicon surface promises to provide the necessary seal. Alternatively, seals can be provided over each chip as mounted on the substrate or the entire substrate can be encased in an hermetic container.

FUNCTIONAL MODULES

The circuits in their protective envelope of glass, ceramic, plastic, or metal must be mounted on a suitable substrate and interconnected in some functional form. This grouping of circuits has been constructed in the form of a plug-in module board. At first, all leads from all circuits were brought out through the connector in an attempt to design universal modules. As packaging densities increased, the number of connections leaving the

Fig. 1—The TO-5 package mainly used for sealing transistors.

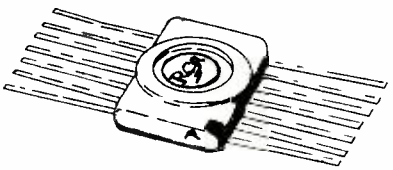

Fig. 2—Planar lead flatpack used for mounting integrated circuits.

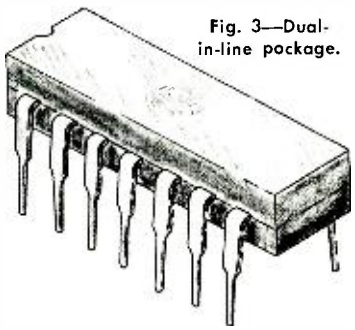

Fig. 3—Dual-in-line package.

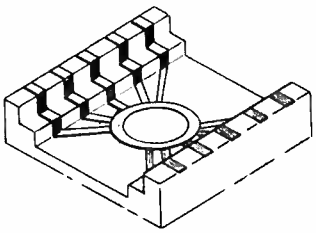

Fig. 4—U-channel carrier.

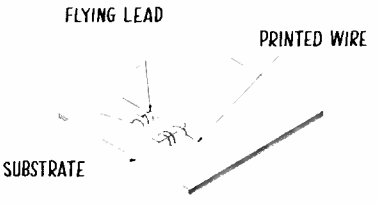

Fig. 5—Thermocompression bonding technique for connecting the conductive pads on a chip to the leads of its package.

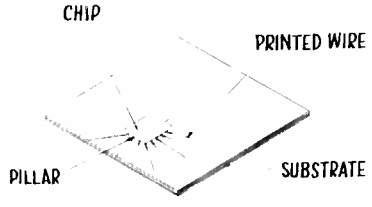

Fig. 6—Face-down bonding method which will soon be a standard technique.

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module limited the complexity obtainable. By arranging functional interconnections within the module, the circuit-to-pin ratio was increased. The resulting pin savings came at the expense of spare parts, for now within a machine there were many more different types of plug-in modules than there would have been with a universal construction. The number of pin connections still represent the limiting item to the module. With little effort on plug-in 3x4-inch cards all the required interconnection can be performed on two layers. Lead lengths are relatively short, and at the speeds involved, transmission-line interconnections are not needed. At future circuit operating speeds of 5 ns pair delay and less, 3x4-inch cards will require controlled impedance interconnections.

ARRAYS

In the near future the plug-in module containing circuit packages will be replaced by LSI (large scale integration) or by a form of large array referred to as hybrid. In the hybrid array, a number of integrated circuit chips are mounted on a substrate containing interconnections. This substrate is then mounted in a large multipin package similar to the flat-packs of the simple circuit chip. In this form it will look identical to the LSI package. The extension of the planar flat-pack or the dual-in-line package is not practical for a great many pins. As the package size increases to accommodate the required pin quantity, it must be increased in all directions to maintain adequate mechanical strength. This increases the package cost and the internal lead lengths, decreasing part of the speed gain and cost saving by the large array. The surface mounting area required increases so that there would be little difference between the area required for a 28-lead package and two 14-lead packages.

LSI is the ultimate in packaging functional groups of circuits. For this concept, a number of circuits are arranged on one silicon chip. The metallization pattern is then applied to both connect the components into circuit form and to interconnect the circuits into an array. This is done by one layer of metal if possible. If necessary, a layer of silicon dioxide is deposited over the first level of metal and a second layer of interconnection is used to finish the connection pattern. When this process becomes common practice an additional level of design will be removed from the domain of the equipment packaging engineer.

SUBSYSTEMS

The design of the subsystem packaging and interconnections provides more potential variety than any other part of the computer structure. Since functional modules are normally designed as plug-in units, the subsystem structure is required to hold a series of connectors and provide for their interconnection. The structure must provide adequate cooling for the circuits without interfering with the necessary accessibility for maintenance.

The earliest computers provided a nest as the supporting structure. Interconnections were provided by point-to-point wiring between pins of the connectors. Currently, this kind of wiring is done by automatic wire-wrap machines, controlled by magnetic tape and making connections to posts at the intersections of a 0.100-inch grid. The wire-wrap machines cannot provide the controlled impedance interconnections required by modern high speed computers.

The present Spectra 70 computer design has replaced the wire-wrap interconnections with multilayer printed-circuit boards. Ground planes with adequate control of line width and dielectric thickness provide a controlled impedance connection. New platters will be capable of providing controlled impedance interconnections to signal pins on a 0.100-inch grid.[2]

For future packaging of subsystems, a much more sophisticated technique will be required for mounting and interconnecting substrates. As a result of current work, a number of assembly methods are evolving. The designs conceived are based on a functional plug-in module approximately 5/8-inch square containing interconnections and up to a dozen face-down bonded silicon chips. The use of an additional assembly will greatly increase the circuit density while reducing the wiring complexity of the platter.

The concept under development will provide 32 functional modules mounted on a multilayer board 4 inches wide by 4 inches tall. This board can plug into a connector mounted on a platter. If we now consider this 4-inch square board as having three vertical flexible areas built into it the assembly can fold into a module 4 inches tall by 1 inch square. The modules will interleave, forming an extremely dense three-dimensional package. To take maximum advantage of the construction, the closing edges of the folded assembly will include a connection, thus shortening some of the connections from 3½ inch to ½ inch long and reducing the maximum length by 2 inches.

The construction envisioned will result in circuit densities averaging 50 per cubic inch and reaching 75 to 80 with power densities, based on today's circuit, of 10 watts per cubic inch.

CONCLUSION

The various techniques needed to successfully package uncased chips are being developed at the present time. The hermetic sealing of the chip with glass is being developed by the RCA Laboratories. The face-down mounting of integrated circuits has been accomplished by a variety of methods, any of which appear to be adaptable to automated factory operation. The substrate needed to mount the chips will require .004 inch wide lines and plated through-holes less than .010 inch in diameter. Printing techniques have proved suitable for use at the substrate sizes involved. Ceramics are being produced on a regular basis with .008 inch holes. Laser drilling of even smaller holes is practical. The flexible section of the proposed folded assembly is similar to the printed circuit cables that have become commonplace. The power density is only 1/10 that experienced with power tubes which have been successfully cooled with inert fluorocarbon liquids.

Uncased chip packaging is feasible, requiring the combination of a number of techniques already successfully used. The results should be several orders of magnitude shrinkage in volume with a comparable decrease in connection length, cost, and increase in reliability.

REFERENCES

1. A. I. Stoller, J. A. Amick, N. E. Wolff, "Getting the Most out of Circuits with Dielectric Isolation," *Electronics*, Vol. 40, No. 6 (Mar. 20, 1967).
2. J. Surina, "Nanosecond Packaging with Multilayer Printed-Circuit Boards," this issue of the RCA ENGINEER.

THE MINIMATRIX: FLEXIBLE APPROACH TO PRODUCTION OF EMITTER COUPLED LOGIC ARRAYS

The Minimatrix is a "master slice" approach designed to resolve some of the problems inherent in the demand for higher packaging density and reduced transmission delays. This paper discusses the philosophy, and the approach of the Minimatrix concept. Design-automation using computer-aided techniques to generate the artwork for a 14-gate adder design is also described and illustrated.

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LARGE CAPACITY, high speed data processing systems will rely increasingly on array technology. The high data flow rates required by these computers will demand a much higher circuit packaging density to reduce delays along transmission lines between logic stages.

However, the general use of arrays is somewhat hampered by the diverse requirements of the user and the manufacturer. The device manufacturer would like large arrays to follow the same route taken by integrated circuit users up to the present: use one or two types in very large quantity. However, the equipment manufacturers say that not enough repetition of even small blocks of logic occurs to permit efficient utilization of a few standard types. Further, a short design and fabrication cycle is required so that the equipment designer can quickly get samples to determine that the integrated circuit array does indeed meet his performance requirements and to facilitate changes as quickly as they may be required.

Many array philosophies can be adapted by an integrated circuit manufacturer; the three most commonly described are:

1) *Functional Arrays* which are designed specifically for a particular use thereby minimizing wasted area on a chip by efficient use of every component;
2) *Master Slice Arrays* which are composed of "cells" (a simple circuit, or group of undesignated components) which are interconnected with different metalization patterns to create different logic functions; and
3) *Discretionary Arrays* which are essentially master slice arrays; however, the cells on the wafer are pre-tested. For any one function, different metalization patterns are created tying together only those cells which are known to be operational.

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NINE-CELL MINIMATRIX ARRAYS

The low pin-to-gate ratio functional logic that large arrays can adequately service represents anywhere from 30 to 60% of a processor, depending on its size and purpose. The control logic, with its high pin-to-gate ratio, accounts for much of the remaining logic circuitry. A fixed number of gates on a fixed chip size results in inefficient use of the integrated circuit array in control logic application. Thus, the ability to produce different size chips for larger and smaller functional blocks, as well as for control logic from the same wafer is desirable. The smallest chip, with its higher yield and lower relative pin-to-gate ratio, would satisfy the control logic requirement. The minimatrix approach provides this total capability.

After a study of circuit type requirements for various arrays, a "cell" configuration (Fig. 1) was decided upon. The cell consists of 7 transistors and 10 resistors and, using standard integrated circuit layout rules, occupies a 0.018x0.018-inch area. Nine of these cells are arranged in a 3x3 minimatrix to form the basic building block for all the CML special purpose arrays. The 9-cell building block itself occupies a 0.056x0.056 inch area which is well within the processing limitations currently adhered to at Somerville. No metalization pattern is placed within the basic building block; i.e., the minimatrix is, in its undefined state, a group of uncommitted resistors and transistors. With this approach, for any array configuration, all masks up to and including the contact mask are identical—only the metalization masks are changed to create a given logic function.

One of the chief disadvantages of the universal approach is the wasted area, since all components are not used for all applications. However, the approach being pursued more efficiently utilizes area. To better understand this concept, consider the following:

1) CML arrays need fairly heavy metalization paths in the ground and —5.0-volt lines on the chip.
2) Usually, this heavy metalization would be facilitated on the second level of metalization. However, in two-layer metalization techniques, the more area covered on the second level by metal, the more probability there is of discovering pin-holes in the insulating layer between the first and second layers of aluminum. Also, since the power supply and ground distribution busses carry the heaviest current, any contact resistance in the first-to-second layer via holes would be amplified to the detriment of the circuit logic levels.
3) A study made by the Array Group at SECD Somerville in a progam sponsored by Wright-Patterson AFB (Contract AF33(615)-3491) shows that on the first layer alone, the area occupied by the metal paths equals that occupied by the components on that layer. This study was made with all the power supply metalization paths on the second layer.

In the master-slice array approach, all cells are placed adjacent to one another leaving no area for wiring. Also, the cells are grouped in such a manner so that the area occupied by unused components can be used to supply area for power supply distribution on the *first* level of metalization. Therefore, ground and —5.0 volts can be *adequately* distributed on the first layer of metalization. Also, the cells are configured to allow for cell-interconnect metalization on the first layer. This leaves the second layer of metalization with the comparatively sparse interconnections for creating the required array logic function. Thus pinhole effects are reduced and yield is greatly increased by allowing for loose tolerance second-layer metalization masks and first-to-second layer contact masks. The first layer of circuitry then contains no wasted components since the area occupied by unused components would be required in any event. This is because the power supply distribution pattern is used on the first layer. Placing the power supply metalization on the first layer has another excellent advantage in that every circuit on the chip is operational at the first (conventional) level of metalization. Therefore every gate and flip-flop in the array can be pretested before it is interconnected with the second level of metalization.

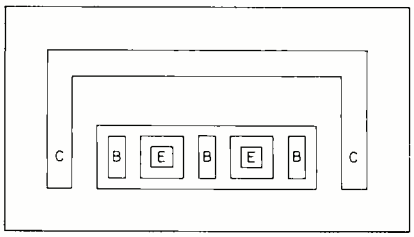


Fig. 2a—Triple base-stripe transistar-three base contacts.

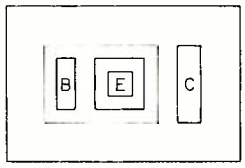


Fig. 2b—Single base-stripe transistor.

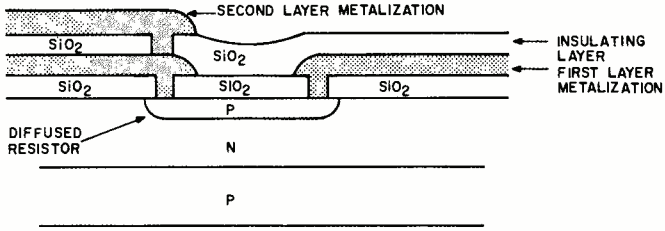


Fig. 3—Cross-section of two-layer metalization structure.

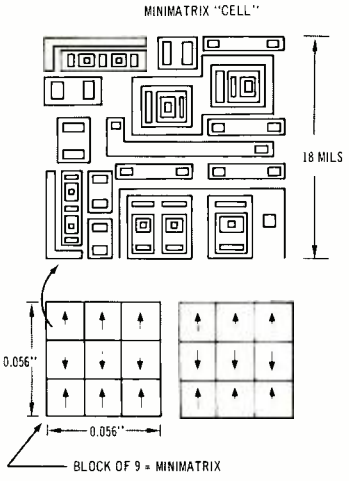
An integrated circuit wafer containing these 9-cell minimatrixes can be used to build 9-, 18-, or 36-gate arrays by simply scribing the wafer at different scribe intervals. For example, the 9-cell chip is 56x56 mils; the 18-cell chip is 118x56 mils; and the 36-cell chip is 118x118 mils.

Presently, bonding pads are placed over unused components, to reduce the actual number of cells available for circuit designation. However, tests will be made to determine whether or not the active circuit area can be bonded over along the edge of the chip.

Although a great deal of fabrication flexibility has been achieved, it is not enough. Equally important is the system flexibility of the minimatrix approach. To demonstrate this, four functions were chosen: a memory switch chip, a gated register chip, a full adder chip, and a shifter chip. The first and second layer metalization patterns for each of these functions were taped to scale so potential wiring limitations could be examined—no severe limitations were encountered. An independent evaluation of flexibility was made in DEP where several different circuit configurations were generated without encountering wiring difficulties. In summary, the minimatrix approach has the following features:

1) Any size array from 1 to 36 gates can be accommodated.
2) Chip sizes from 56x56 mils through 118x118 mils can be made.
3) Both "universal" and functional arrays can be accommodated.

Fig. 1—Cell layout and orientation in basic building blocks.



4) Power dissipation can be reduced where system requirements allow, since a choice of component values exists.
5) All of the above four features are accommodated with the same integrated circuit wafer.
6) Besides the design automation techniques described in this paper, another metalization mask-making system has been devised so that taped layouts of the desired metalization masks at 200X magnification can be used to produce metalization masks directly (no rubylith required)—thus providing quick turn-around time.
7) No special processing or photographic capabilities are required to make arrays up to the first level of metalization.

FABRICATION TECHNOLOGY

Two types of transistors are used in the basic cell structure: The transistor shown in Fig. 2a has two emitters and three base contacts and is capable of driving 50-ohm terminated transmission lines when used as a gate emitter-follower output transistor. The transistor shown in Fig. 2b is used in the differential amplifier portion of the logic circuit. However, both transistors have standard geometries and are fabricated using a standard diffusion profile.

The only non-standard fabrication process associated with the fabrication of these arrays is the multilayer metalization process. Fig. 3 shows a cross-sectional view of two-layer metalization. Both layers of conductors are aluminum, while the insulating layer is a deposited SiO_2 glass. In addition to the standard set of diffusion masks, another contact mask is required to define those areas where the first and second layers of aluminum make contact through the SiO_2 insulating layer. Also, of course, a mask is needed to define the second layer metalization pattern. A *black-out* mask is then used to close all those contacts in unused components so that metalization patterns can be run over these components and not make contact with them.

Array yield per wafer is directly related to the area per array. One obvious way to decrease area is to shrink individual component sizes and component spacing. However, this procedure can only be used until component failures and poor component tolerances begin to destroy yield.

To study this problem, a 4-cell test-pattern chip was designed in conjunction with the arrays. Fig. 4 is a photomicrograph of a test chip containing four identical circuits. However each of the four circuits is successively smaller: from 18x18 mils to 15x15 mils. This decreased size is accomplished simply by shrinking the size of components and component spacing. Wafers of these test circuits are being automatically probed and tested by computer for power dissipation, logic levels, noise immunity, and component integrity. From these tests will come the relative yield figures for the four different size cells.

Now that feasibility has been established, improved performance characteristics will be sought through the use of shallow diffusion techniques and smaller transistor geometries. Also, yield improvements can be realized by using redundant processing techniques.

COMPUTER AIDED MASK ARTWORK GENERATION

There are essentially two sets of masks involved in the fabrication of integrated circuit arrays using the minimatrix approach. The first set of masks is used to generate the *basic array* which contains no metalization interconnections. Wafers containing large numbers of these *basic arrays* will be stored on the shelves of the semiconductor manufacturers, thus these *basic arrays* remain fixed in topology. By adding metalization interconnects to the *basic array*, a wide variety of functional and nonfunctional logic configurations can be generated. Minimatrix accomplishes this by using four masks. This set of four masks will be referred to as the custom array. In general, the device manufacturer will be primarily concerned with the generation of the artwork for the *basic array*, while both the device manufacturer and the equipment designer will be jointly, responsible for the *custom array* artwork generation.

The flow chart for the computer aided mask artwork generation is shown in Fig. 5. The two dotted blocks refer to

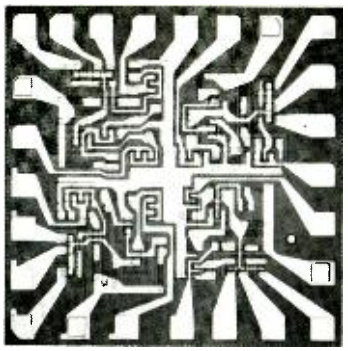


Fig. 4—Four-cell test pattern chip.

the generation of the *basic array* and the *custom array*. As seen in Fig. 5, all artwork generation begins with a hand-drawn layout on dimensionally stable grid-lined material such as mylar film. Depending on the size of the device or component, and the resolution required, scale factors may be anywhere from 100 to 2000 or higher.

In these layouts, the intersections of all lines forming a closed polygon must fall on the intersection of a vertical and horizontal grid line. The information drawn on the mylar film is then digitized (an electromechanical technique for storing the relative loactions of all polygon vertices). Punched cards containing this information serve as input data for a computer program which generates plotting instructions for the automatic artwork generator. These instructions are placed on tape which in turn drives the automatic artwork plotter. The artwork is plotted on glass at a 60X scale with all closed polygons darkened. Contact prints are made on mylar film and sent to the semiconductor manufacturer who reduces the artwork by 60. Glass plates at a 1-to-1 scale (the working plates) containing the various mask patterns are then generated. These are the masks which will be used in the fabrication process.

BASIC ARRAY ARTWORK GENERATION

A flow chart for the *basic array* artwork generation is shown in Fig. 6. As a result of the design philosophy discussed earlier, the type of components, their geometry, and their relative positions are known. These components are laid out at 2000X as shown by the transistor breakdown in Fig. 7. Each of these elements of the transistor relates to a particular diffusion or oxide step (more specifically, to a particular mask). The relationship between the transistor elements in Fig. 7 and the mask level is shown in Table I. In a manner similar to the transistor breakdown resistors and special components such as mask alignment keys, photo-alignment keys, and dicing area components are digitized, identified by a code, and stored on tape.

TABLE I—Relationship Between Transistor Levels and Process Step

Transistor Elements (Fig. 3) Mask Number	*Description of Process Step*
1	N + pocket
2	N + collector ring
3	N Isolation
4	P + Diffusion
5	P Diffusion-base and resistor
6	N + diffusion
7	First oxide on contact
8	First Metal Comp

Upon call, these components can be automatically retrieved and used to form selective patterns of the components stored on tape. The mechanism for doing this is the orientation and location (O & L) pattern (Fig. 8). All components are located at a given *X-Y* coordinate with respect to the reference point 0.0. The orientation of the letter *R* indicates the desired orientation of each component centered at its *X-Y* reference point. The 18-component basic cell is given a code name, placed on tape, and treated as a single entity. By calling for it by name, the computer program effectively creates the patterns for the various masking levels, as indicated in Figs. 9a through Fig. 9g. The composite of the basic cell is shown in Fig. 9h. The wafer containing the basic arrays is made of many of the composites, except that all the closed polygons are filled: all oxide openings or contacts have been metalized.

Intragate Metalizations

At this point in the process, individual gate metalization patterns can be developed, identified, and stored for future use. The particular intragate patterns developed thus far for the minimatrix program were laid out at 2000X. Fig. 10a illustrates the intragate connections for a 3-input gate with the NOR output available and an internal bias supply source; Fig. 10b is the intragate metalization for a 2-input gate with complementary output. When needed, these intragate patterns are retrieved by calling out their code name and location on an O & L pattern. The proper set of components will be automatically connected together by the interconnecting patterns generated by the automatic artwork generator under control of the computer generated tape.

Basic 9-Cell Pattern

The basic 9-cell pattern is generated simply by using an O&L pattern to call for and locate nine of the basic cells. Again the automatic process will generate the artwork for all the mask levels required for the 9-cell pattern.

The 36-Cell Basic Array

Once the mask artworks for the basic 9-cell array have been checked and veri-

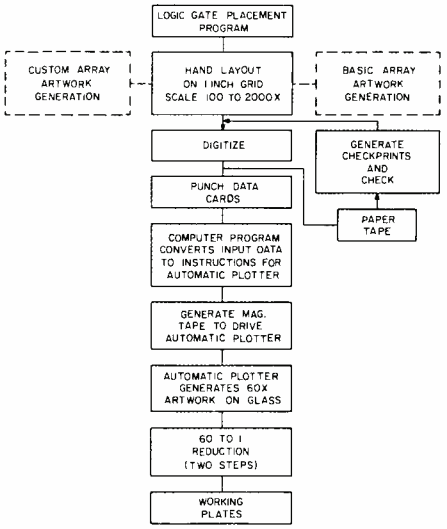


Fig. 5—Flow chart for computer-aided mask artwork generation.

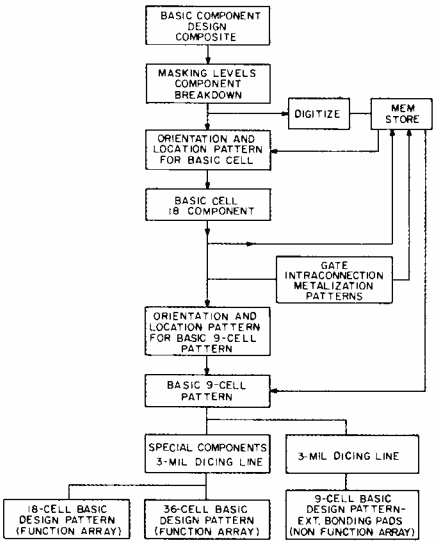


Fig. 6—Flow chart for generation of basic array artwork.

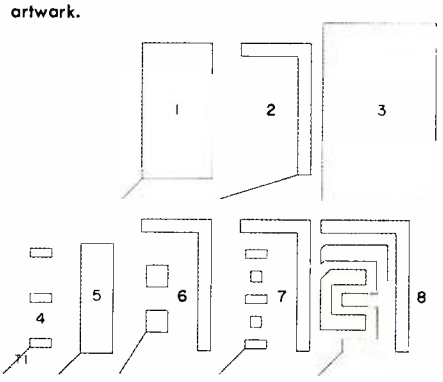


Fig. 7—Transistor diffusion and contact levels for basic array.

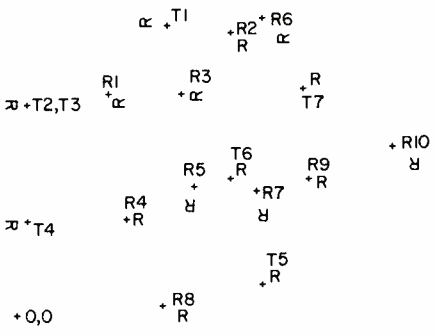
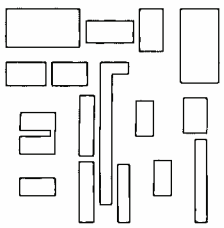
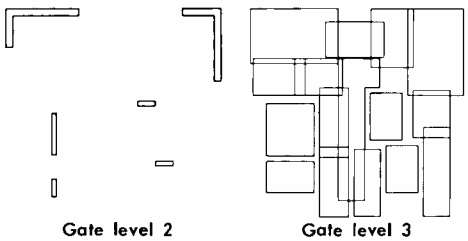


Fig. 8—Orientation and location for 18-component basic cell.

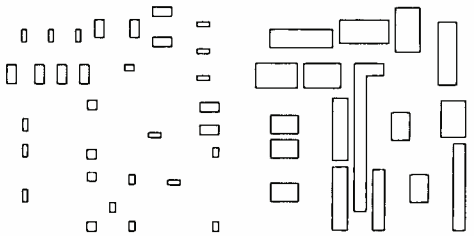


Gate level 1

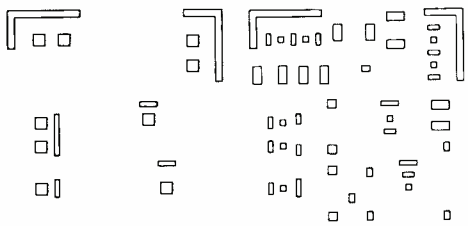
Fig. 9—Patterns for various masking levels of 18-campanent basic cell.



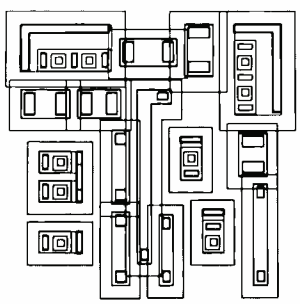
Gate level 2 Gate level 3



Gate level 4 Gate level 5



Gate level 6 Gate level 7



Composite of the basic cell.

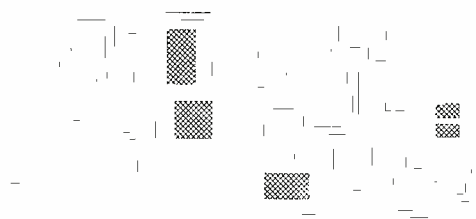


Fig. 10a—Intragate metalization far 3-input, NOR output internal bias supply.

Fig. 10b—Intragate metalizatian far 2-input, camplementary output.

fied, they are used to generate final working plates containing many of these 9-cell patterns by a photographic step and repeat process. Thus, at this point the array contains many cells of unconnected or uncommitted components. Depending on the particular application, the wafer can be cut into 9-cell, 18-cell, and 36-cell chips. Therefore, while maintaining the advantage of being universal, various chip sizes (with their attendant yield advantages) are available depending on the particular logic requirement. In this way, the basic array services the requirements of low pin-to-gate ratios associated with data paths as well as high pin-to-gate ratios of the logic associated with the control paths. A 36-cell portion of the wafer containing the basic cells is shown in Fig. 11. An enlarged reproduction of the 36-cell array on dimensionally stable mylar film with 0.1-inch grids is used to aid in the generation of the interconnecting metalization artwork.

CUSTOM ARRAY ARTWORK GENERATION

Initial Steps

To use the basic array to obtain integrated circuit arrays that perform some particular logic function, the previously mentioned set of four custom metalization and contact masks are required. The artworks for these four masks are the only ones that must be generated to produce new logic configurations. They are the first and second metalization layers, the second contact, and the blackout mask artwork. The blackout mask contains extremely simple patterns. The first metalization mask is the most complex but requires little hand layout.

The steps for generating the artwork for the custom masks are shown in Fig. 12. Although not an intrinsic part of the artwork generation process, the logic should be verified as being functionally correct and providing the required timing or delay. LOGSIM, a logical gate simulator program, has been developed and is available for the purpose. Assuming that each basic cell (17 components)

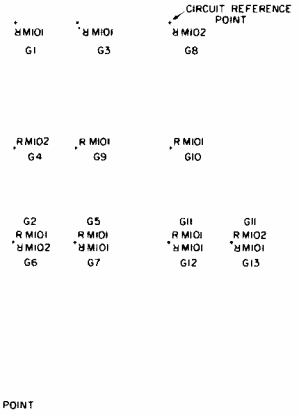


Fig. 13—Orientation and location (O&L) pattern for adder first layer metalization.

corresponds to a gate in the logic, some particular cell location is then assigned to the various gates in the array. The manner in which these gate assignments or placements are made has a strong influence on the length, complexity, and crossover pattern of the intergate wiring. To aid in efficiently placing the gates, an automatic gate program is used.

Sample Design Using The Faur Mask Types

The design of the artwork for an adder will be used to illustrate the procedure for generating the custom artwork. Following the assignment of gate position by the placement program, the O&L pattern (Fig. 13) is drawn. At each circuit reference point there is an *R* (or an inverted *R*) followed by an *M* number. The *M* number, for example *M101*, instructs the computer to retrieve the metalization pattern of Fig. 5a. The automatic plotter will draw this metalization pattern in one of eight orientations which is defined by the orientation of the letter *R*. The process will be repeated for each of the 14 metalization patterns called for by this O&L drawing, resulting in 14 intraconnected gates. To provide for test transistors and to connect ground and the supply voltage to pins, a custom interconnect pattern is drawn. This is identified by the name *M151* and called by the O&L pattern of Fig. 13 by that name. In future designs, a large portion of the interconnect pattern will also be computer supplied. At this point all the required input information is

Fig. 11—A portion of the 36-cell basic array.

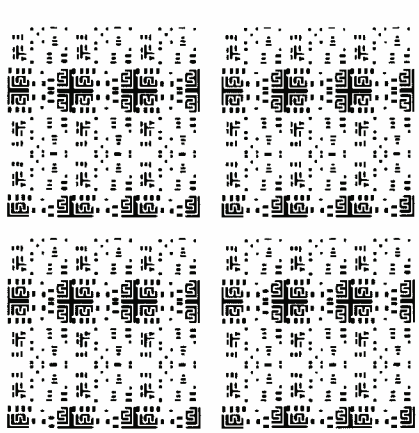
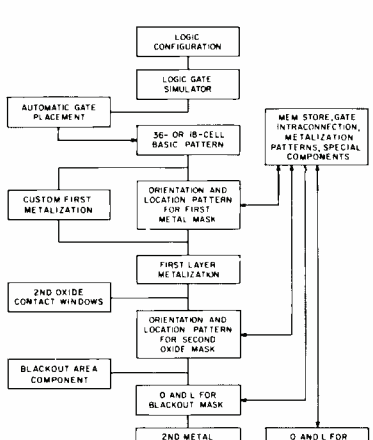


Fig. 12—Flow chart for custom array artwork generation.



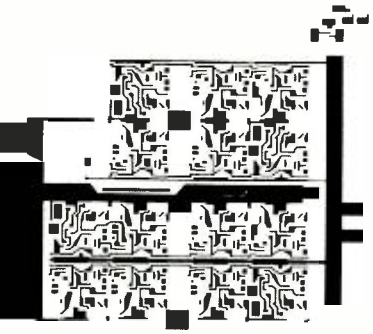


Fig. 14—First metalization mask for the adder.

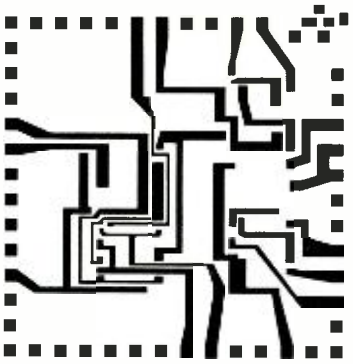


Fig. 15—Second metalization mask for the adder.

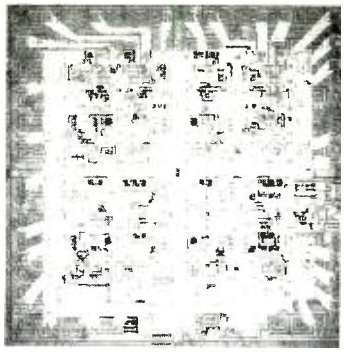


Fig. 16—Photomicrograph of memory switch chip.

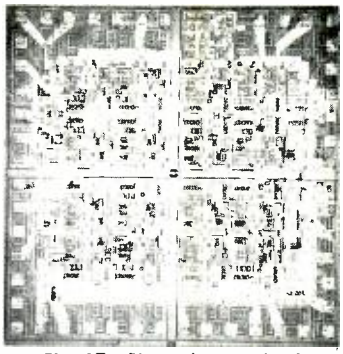


Fig. 17—Photomicrograph of register chip.

stored on tape and the automatic plotter can now plot to 60X scale the complete first-layer metalization pattern. Fig. 14 shows the first metalization mask for the adder.

The second oxide or contact mask artwork is produced by overlaying the basic 36-cell array artwork with a grid mylar film. Keeping in mind the gate metalization patterns used, the oxide openings are drawn over the input and output terminals of the used gates. This step is a little awkward at first, but with a few days practice it becomes quite easy. To this artwork must be added oxide openings for crossovers should they be required when the second layer metalization is drawn.

The blackout mask artwork is a relatively simple mask that prevents the oxide removal from contacts on the outside perimeter where unused elements exist. This gives an extra level of protection against oxide break-through under the bond pads when wires are bonded to the pads either by thermal compression or ultrasonic techniques.

The second metalization mask interconnects the various gates to produce the desired logic function. Depending on the gate function, various areas on each basic cell are available for crossovers. That is, a second layer metal connects to the first layer through an oxide opening, moves along certain specified areas on the first layer, and returns to the second layer through another oxide opening. These oxide openings must be added to the oxide mask artwork at the appropriate locations. The second metalization artwork is shown in Fig. 15.

TESTING AND OPERATIONAL RESULTS

At the time of this writing, two array types, the memory switch chip and register chip, were successfully fabricated with the minimatrix approach. Figs. 16 and 17 show the wafer and chip photomicrographs. Each of these arrays are packaged in a 28-lead flat pack. Testing of these types is done at three levels:

1) DC wafer probe tests at first layer metalization;
2) DC wafer probe tests of completed array; and
3) Dynamic testing of the packaged array function.

At first layer DC wafer probe, a sampling of the gates in the array is tested for current drain, logic levels, and reference voltage. The second wafer DC probe tests the array function to some extent. Exhaustive functional testing has not been performed on these arrays in the wafer form. In fact fewer than 32 tests are performed at this level. Exhaustive testing, after the array was packaged, has not resulted in rejection of any circuit which passed the limited DC testing done on the wafer. Under no-load conditions, array circuitry propagation delay is approximately 2 ns.

ACKNOWLEDGEMENTS

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The design automation techniques described were originally conceived and implemented by C. Pendred of Advanced Technology and R. Geshner and J. Proesson of Central Engineering to produce artwork for printed circuit boards. They later adapted these techniques to produce mask artwork for bipolar and MOS arrays. The computer programs were written by C. Pendred and S. Petty of Advanced Technology.

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NANOSECOND PACKAGING WITH MULTILAYER PRINTED CIRCUIT BOARDS

A significant change in packaging design concepts using multi-layer printed circuit boards is underway. Future computer systems with logic-speed requirements in the nanosecond propagation range will not tolerate the propagation delay times of present digital equipment. A new design attitude and approach is necessary: efficiency of interconnections to improve high speed performance and to maintain large data-handling capabilities demands primary concern.

JOHN J. SURINA

Computer Circuits and Packaging

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Specifications for new generations of computers historically include requirements for handling greater amounts of data and faster processing of this expanded data volume. Processing speed and data volume requirements for data processing equipments of the near future were recently more closely defined in conjunction with several study programs, such as the planning of the RCA proposal for the Illiac iv System. In terms of hardware, the more stringent performance requirements for the proposed designs have resulted in use of higher speed gates, and an increase in the number of gates per machine.

In the past, physical size of equipments was essentially unrestricted except for the housing-space requirement. Relatively minor speed and electrical performance advantages accrued from denser packaging.

The next plateau of machine speed and data handling size specifications, has brought about a revision in some of the hardware design concepts previously applied. These revisions are forced upon equipment designers by the more important role that propagation delays within interconnections play in determining system performance. Gate speed requirements in the low nanosecond region are incompatible with the large propagation delays inherent in the interconnections between gates of past equipment designs. The larger data volume handling requirements only emphasize the importance of minimizing interconnection propagation delays, since increased numbers of gates within a machine inevitably result in greater physical separation between gates.

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To accomplish the performance goals established for the future families of machines, equipment packaging philosophy is undergoing marked changes. The packaging format for a machine will be chosen more from the viewpoint of optimizing overall machine performance, rather than for space or fabrication economy. High density packaging will be a prime requisite to reduce distances between active gates and thus reduce propagation delay. Packaging configurations and materials will be chosen to enhance efficiency of interconnections, so as to directly improve high speed performance while preserving the large data handling capabilities.

RELATIONSHIPS OF SYSTEM PARAMETERS TO PACKAGING

Gate Speed

The next plateau of gate speed requirements for digital machines is foreseen as 4 nanoseconds wired worst case pair delay. This translates to 2 ns at the basic per gate, or per stage, level. As a reference for comparison, equipments presently being produced call for wired worst-case pair-delays of 25 ns (12.5 ns per gate, or stage).

Stage (or gate) delay can be looked upon as the sum of three relatively independent elements:

1) Basic unloaded circuit delay,
2) Additional circuit delay resulting from loading on the circuit, and
3) Propagation delay between circuits.

The first element is essentially independent of equipment packaging design, being a function of the circuit configuration chosen, speed characteristics of active semiconductors, and physical geometries at the active switching-device level. The second element can be influenced not only by the choice of the circuit configuration and the active switching device, but also by the packaging format. The capacitances associated with the pads, separable connectors, and interconnections between circuits must be considered as much a part of the loading on a driving gate as the input impedance of the gate being driven. The third element, propagation delay between circuits, is a function of both the length of interconnections between gates and the velocity of propagation through the interconnections. Both of these factors are directly influenced by the equipment packaging design. Interconnection length is a function of packaging density. When propagation delays through interconnections approach an appreciable percentage of the total allowable stage delay, the only recourse is to reduce the length of the interconnection between stages; i.e., the stages must be closer together and packaging density must increase.

On the other hand, the velocity of propagation is determined primarily by the dielectric medium. Signal circuit propagation delays as low as 1.016 ns/ft[1] might be achieved through use of air dielectric; however delays encountered with the practical dielectrics used in equipment designs range from 1.5 to 2.5 ns/ft.

To grasp more firmly the implications and magnitudes of the packaging density requirements, let us perform a sample calculation based on the 2 ns/stage requirement which has been established as our goal. At this level, a logical apportionment would be to assign equal weight to each of the three delay component elements: ⅔ ns each to the unloaded circuit delay, to the loading effect, and to the propagation delay.

When using interconnections with propagation delays of 2.4 ns/ft, two-thirds of a nanosecond is represented by approximately 3 in. of line length — an exceedingly small worst-case distance.

Packaging densities achieved and demonstrated suitable for the 25 ns wired worst-case pair-delays of present equipment (12½ ns stage delays) are approximately 850 gates/ft.[3] This design provides for several feet of interconnection length. Packaging densities in the range of 5.000 to 10.000 gates/ft.[3] are projected as required to meet the 4-ns wired worst-case pair-delay specifications for the new generation of computers. Even these densities assume taking advantage of developments in other areas, such as system logic design techniques to reduce hardware delays, improvements in logic partitioning, and computer-controlled logic-block placement.

Signal Risetimes

As machine speed requirements rise, the signal risetimes (the time required for signal levels to switch from one binary state to the other) must decrease. Signal risetimes must remain a small fraction of the minimum overlap time (determined from circuit and system design considerations) necessary to ensure binary signal level coincidence in performance of *and*, *or* and other Boolean operations. Signal risetimes must also be appreciably shorter than the delay required per stage in order not to affect the overall stage delays.

Risetimes of 1 nanosecond or less are probably compatible with the 2-ns stage-delay specification and logic speeds for the new generation machines under consideration. In present machine designs, average risetimes of 7.5 ns (5.5 to 9.5 ns limits) are used with the 12.5-ns stage delays to accomplish the speed performance levels required. Previous slower machine designs used slower risetime and stage delays.

For those less familiar with time-domain than frequency-domain analysis, the speed implications might be made clearer by a reminder that the bandwidth requirements for interconnections between stages are inversely proportional to the risetimes of the signals being propagated. Bandwidth (BW) and risetime (T_r) are related by the expression[2]: $BW_{3dB} = 0.35 / T_r$, where T_r is the risetime in ns, and BW_{3dB} is in GHz.

Signals with slow risetimes as used in past slow speed machines could be transmitted satisfactorily between stages with "open wire" interconnections. Open wire conductors with random spacing to ground return paths have narrow but adequate bandwidth characteristics, and the physical interconnection lengths are short compared to electrical wavelengths involved.

For the 7.5 ns average signal risetimes in the present designs, microstrip transmission lines are needed to effect interconnections between stages separated by more than 6 inches. The transmission lines must be properly terminated to prevent signal reflections, and appropriately spaced to keep crosstalk within acceptable limits.[3]

For signal risetimes of 1 ns and less (risetimes down to ½ ns should probably be expected in a 1-ns worst-case design) the interconnections between stages must be designed to handle even greater bandwidths. Signal transmission line geometries, materials, and production tolerances must be chosen and more stringently controlled. This will allow faithful transmittance without degradation of signals being propagated down the lines, and also keep spurious noise generated through signal reflections or crosstalk at an acceptably low level.

Virtually all interconnections must be designed as transmission lines. Since line propagation delays of 2.4 ns/ft and risetimes down to ½ ns can be expected, full amplitude signal reflections are possible in as little as 2½-inch sections of line. Coupling regions between parallel lines of the same length can generate maximum amplitude backward and formidably high forward crosstalk signals, indicating that properly controlled and terminated transmission lines might be necessary for interconnection distances in the order of one inch.

Separable connectors between assembly levels which handle signals with these risetime characteristics will also require special design precautions. Appropriately short connector lengths (in the order of less than 1 inch for the sum of both signal and ground leads) and closer control of characteristic impedance within the connector (so as to present less of a mismatch with the transmission line impedance level used for fixed interconnections) will probably be required.

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Special attention will be necessary to ensure that power distribution systems present adequately low source and bypassing impedances. High capacitance (obtained with dielectrics exhibiting low loss characteristics over the wide bandwidths), low resistance, and low inductances must be maintained throughout the power distribution system.

Pin Density

At first, the packaging density of digital equipment might seem to be increased simply through use of a larger number of active gates at the plug-in-card first-assembly level. This tempting design avenue is soon found to be a dead-end, since addition of gates to the card level generates a need for connector pins mating with the next higher level, which are not available.

The relationship between the number of gates per assembly level and the num-

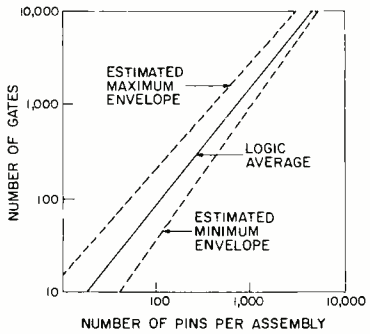


Fig. 1—Relation between number of gates per assembly and interconnections required.

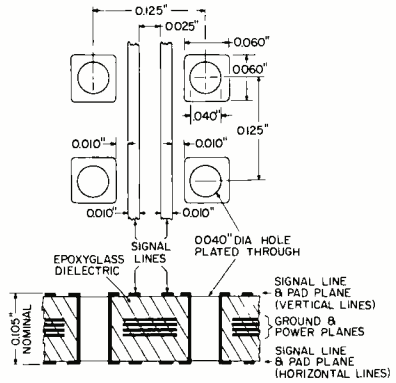


Fig. 2—Present platter grid and cross-sectional format.

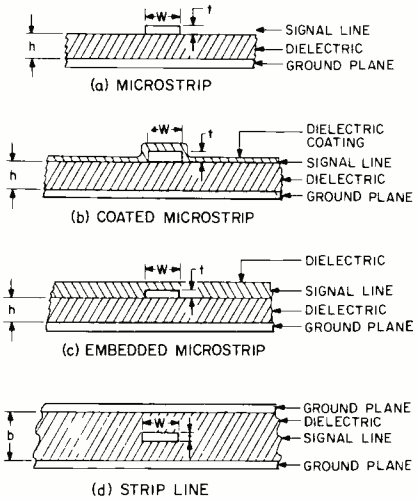


Fig. 3—Printed circuit transmission line cross-sectional configurations.

ber of pins required has been determined through studies of gate-to-pin ratios, at various assembly levels, used in present and past generations of digital equipment designs. This relationship is shown plotted in Fig. 1.[4] Note that the relationship between pins and gates is not a directly proportional one. Some benefits accrue through use of more gates per assembly, although the advantages are minimal for small increases in assembly size.

The practical way, then, to reap the benefits of increased gate population at the plug-in or first level of assembly is to provide for additional connector pins to mate with the next higher (platter) assembly. This must be accomplished without requiring additional area on the platter.

Presently used platter assemblies have provision for connection pads and plated through holes on a 0.125-inch grid. Separable connector pins cannot occupy all grid locations, since provision must be included for such necessities as via holes (which join interconnection lines on separate signal layers), terminating resistors, and power and ground connections.

Providing more connector pins per unit area on a platter without sacrificing grid locations committed for other necessary functions can be accomplished only through reduction of the 0.125-inch grid, thus making available additional potential connector-pin grid locations. Reducing the grid to 0.100 inch provides 25 percent additional grid hole locations, and has been found to be compatible with other design considerations.

A study was made to determine what packaging densities could be achieved through reducing the platter grid spacing to 0.100 inch, in addition to other evolutionary changes which are considered feasible for a production design within one year. Results are presented in Table I. Assumptions for four high density optional packaging configurations include use of a 60- to 100-pin separable connector for signal pins, and placement of transmission-line terminating resistors on the plug-in card so as to be compatible with the faster risetime and stage-delay specifications of active circuits.

Packaging densities achievable were also a function of the type of packaging used to house the active integrated circuit gates which are assembled on the plug-in card. Maximum packaging densities are accomplished through use of functional "large array" integrated circuit packages at the device level. Similar conclusions about the necessity for large arrays, to achieve the high speed goals required, have been reached by others.

Interconnection Density

When the number of connector pins per unit area which require interconnection is increased to achieve higher packaging densities, provisions must be made to increase the conductors available per unit area with which to effect the interconnections. Interconnections in the present designs are made through lines on two signal planes. A sketch outlining the platter grid, line and cross-sectional formats is shown in Fig. 2. Lines on one signal plane are orthogonal to those on the other, allowing interconnections to be made in either horizontal or vertical directions.

One method of evaluating the adequacy of interconnection conductors provided in a new design is to compare the amount of conductors available per active connector pin with those required in a design known to be adequate. Through analysis of the interconnection lines used in the existing successful RCA equipments, one can obtain realistic insight into the requirements of the proposed high density design if use is made of a similar multilayer board interconnection arrangement.

Analysis based on platter assemblies which used the maximum percentage of the available copper conductors (therefore were primarily copper conductor limited) shows that just under 12 unit grid lengths of conductor were required for each active connector pin. Applying the same analysis to the proposed high packaging density designs using a 0.100-inch grid indicates that one orthogonal pair of signal planes would make available six unit grid lengths of conductor per active signal pin, or approximately one-half of the interconnection capability required.

Investigations have been made to determine the best way to at least double the interconnection capability provided by the presently used two printed circuit signal planes, but including a 0.100 inch grid necessary to achieve the high packaging densities. Efforts centered mainly around the following three potentially practical modifications of the existing format:

1) Use of more than two lines between pad locations;
2) Use of additional signal line planes (but no additional ground planes); and
3) Use of additional signal line and ground planes.

Incorporation of additional signal-line planes together with associated ground planes (modification 3) was found to be the most practical approach. The latent fabrication problems associated with the more complex cross-sectional geometry are outweighed by the promise of meeting both electrical and interconnection density requirements. A more thorough analysis of this configuration is presented in the next section.

The Spectra 70 is the first RCA computer to incorporate many of these electrical interconnection principles which could provide a basis for development of higher-speed equipment.

MULTI-SIGNAL LAYER PLATTER DESIGN FACTORS

Fabrication Limitotions

Modifications and changes in any design are always limited by the production fabrication techniques which are available. To stay within a realistic design time frame for the next generation equipments, let us consider the modifications which can be implemented with methods and facilities already available, or techniques which could be developed to full fruition and demonstrated to be practical within 1 year.

The desired packaging densities will involve use of more complex laminated multi-layer printed-circuit-board assemblies. The problems associated with these board assemblies are proportional to board area, and thus would manifest themselves more forcefully in the large 18 x 18-inch platter assembly. In large multilayer board assemblies incorporating transmission-line signal-interconnection layers, four fabrication factors are the key items limiting usable grid and interconnection densities.[5] These four factors, and levels of fabrication capability which were expected to be practical within a reasonable time frame, are delineated as follows:

1) *Line width:* Minimum printed circuit line widths down to 0.005 inch, for line width controlled within ±10 percent (on internal layer only).
2) *Dielectric material:* Dielectric material to remain G-10 epoxyglass (relative dielectric constant of approximately 5.0), pending development of laminating techniques which would allow incorporation of more than one dielectric material into multilayer assemblies.
3) *Plated hole:* The ratio of laminated-board thickness to plated-through-hole diameter of below 5 to 1.
4) *Pad dimensions:* Diameter of copper pads at plated-through hole locations must be at least 20 thousandths greater than hole diameter (hole diameters of 0.030 inch minimum recommended).

Each signal-circuit transmission line interconnection layer incorporated into the multilayer board assembly would physically consist of one of the four cross-sectional configurations shown in Fig. 3. Any one of the three microstrip configurations could be used for signal layers nearest the two outside surfaces of a laminated board assembly. Additional signal-line layers (more than the two maximum available in microstrip) must use the strip-line configuration shown, which requires use of ground planes on each side of the signal line.

Optimum Multilayer Boord Dimensions

Combining fabrication limitations on line width and dielectric constant of 5—factors 1 and 2 listed above—with available design data on printed circuit transmission lines,[3,6] the dimensions of practical microstrip and strip transmission lines for the normally encountered signal-circuit characteristic impedances were calculated. The results of these calculations are shown in Table II.

Translating the information in Table II and key fabrication factors 3 and 4 (plated-through hole diameter ratio and pad diameter) into a design for a singly laminated multi-layer board assembly incorporating four signal transmission line layers and two power distribution layers results in Table III. Approximate maximum board thickness was calculated for the total of 12 copper layers required in the cross-section configuration shown in Fig. 4. The four signal layers shown provide the minimum interconnection density estimated to be required, and the two power planes are considered the minimum necessary for power distribution.

Relation Between Grid Spacing and Characteristic Impedonce

Table III shows that to provide at least four signal layers of interconnections with a 0.100-inch grid, the system impedance must be considered. The impedances chosen for the table are close to those standards values normally used, and for which commercial coaxial cable is available. The highest "standard" impedance for which a 0.100 inch grid can be maintained is 50 ohms. At 75 ohms, the board thickness for a four-signal-layer assembly causes (at the 5 to 1 maximum board-thickness-to-hole-diameter ratio) the plated hole diameter and pad diameter to increase to the point where the desired two signal lines plus pad cannot be placed within the 0.100 inch grid, and still maintain minimum conductor spacing. A "compromise" impedance between 50 and 75 ohms (65 ohms) might be considered attractive were it not for the difficulty in obtaining standard cable at this impedance to use for interconnections between multilayer board assemblies.

An additional advantage for the choice of 50 ohms as the system characteristic

TABLE II—Approximate Dimensions for Printed Circuit Tronsmission Line with Epoxyglass Dielectric

Z_0 (ohms)	Con-figuration	Line Width (mils)	Copper Thick-ness (mils)	Dielec-tric Thick-ness h (mils)	Dielec-tric Thick-ness b (mils)
50	Microstrip	10	-	6	-
	Embedded Microstrip	7.5	14	6	-
	Strip Line	5	14	-	16
75	Microstrip	10	-	15	-
	Embedded Microstrip	7.5	14	15	-
	Strip Line	5	14	-	40
100	Microstrip	10	-	29	-
	Embedded Microstrip	7.5	14	25	-
	Strip Line	5	7	-	80

TABLE I—Packaging Densities for Platter Grid Spacing of 0.100 inch

Packaging Configuration	Platter Cross-Sectional Interconnection Signal Layer Format	Plug-In Card Integrated Circuit Complement (Maximum)	Packaging Density (gates/ft³)
Present RCA equipment design	2 signal layers singly laminated	16 14-lead flatpacks	850
Option 1	4 signal layers singly laminated	35 14-lead flatpacks	4160
Option 2	4 to 6 signal layers singly laminated	4 28-lead flatpacks 4 14-lead flatpacks	6360
Option 3	4 to 6 signal layers sequentially laminated	4 28-lead flatpacks 4 14-lead flatpacks (device leads inserted into holes)	8050
Option 4	4 to 6 signal layers sequentially laminated	4 28-lead flatpacks 24 14-lead flatpacks (surface mounted active devices)	over 10,000

TABLE III—Key Dimensions for Multilayer Board Assemblies with Four Signal Layers

System Characteristic Impedance (ohms)	Approximate Maximum Board Thickness* (inches)	Minimum Plated Hole Diameter** (inches)	Minimum Pad Diameter (inches)	Minimum Grid Spacing† (inches)
50	0.110	0.030	0.050	0.100
75	0.179	0.036	0.056	0.125
100	0.291	0.059	0.079	0.150

* Copper thicknesses of 2 ounce assumed for pads, ground, and power planes. Dielectric thicknesses conform to Table II, with minimum of 0.005 inch for non-critical power and pad plane insulation. Dielectric thickness tolerance ±10% or ±0.001 inch, whichever is greater.

** Minimum hole diameter 1/5 of board thickness, or 0.030 inch, whichever is smaller.

† Only standard grid multiples of 0.025 inch are considered. Two lines between pad locations are assumed, with 0.0075 inch nominal spacing between lines and pads, and 0.020 inch separation between lines.

impedance is the fact that more than four signal layers are possible within a singly-laminated multilayer board assembly while still maintaining the 0.100 inch grid. This possibility not only provides a safety factor allowing for even higher interconnection densities but also could alleviate problems in associated design areas (such as the logic partitioning and placement programs) which aim to avoid copper-line limitations through decentralization of interconnections.

Attenuation Characteristics of Printed Circuit Transmission Lines

The dimensions listed in Table II show that printed-circuit lines with smaller cross-sectional area are to be applied to the new packaging design (past controlled impedance designs used 10-mil-wide lines and 2-ounce copper). Faster signal rise-times must also be handled. These two factors suggest possible problems could be encountered due to attenuation of low and high frequency signal components propagated within these lines.[1]

Low frequency attenuation is primarily a function of the DC resistance of the line. The DC resistance of 1-ounce copper is 0.485 milliohm/square, which can be expressed in a more easily appreciated form as 1.16 ohms/ft for the 5 mil (minimum) line width expected. Since signal transmission line lengths will be kept short to minimize propagation delays, the low frequency attenuation characteristics should be compatible with this application.

Based on data obtained on the microstrip line geometry, high-frequency attenuation characteristics of the printed-circuit transmission lines are seen to be consistent with the 1-ns risetime signals to be interconnected. Epoxyglass dielectric is probably adequate for the line lengths expected in this high density design.

Crosstalk

An electrical characteristic that must be critically examined and appraised before the multilayer board assembly using the 0.100-inch grid can be considered a usable packaging component deals with crosstalk between signal lines. Crosstalk results from the transfer of energy between lines due to capacitive and inductive coupling between the lines.

Pulse crosstalk between printed lines in the microstrip physical configuration has been reported quite thoroughly.[2] Crosstalk for the embedded microstrip and strip-line configuration at the impedance levels and line spacings under consideration were computed and preliminarily verified by experiment.

The 10-percent maximum back crosstalk and 1.3-percent/ft forward crosstalk values found in the present Spectra 70 equipments are probably suitable maximum values to use as a guide for evaluation of any new proposed configuration. If the present Spectra 70 design with microstrip lines were used for interconnection of 1-ns risetime signals, forward crosstalk would increase by a factor of 5 to approximately 6.5 percent/ft. Back crosstalk would not increase in amplitude, but the maximum value of 10 percent would occur in lines 1/5th the 5-ns length, or in approximately 3.3 inches. Minor overall crosstalk improvements might be made by using the embedded microstrip configuration, but two major objections—being limited to two signal layers and a 0.125 inch grid—would not be overcome.

Four 100-ohm signal layers could be made available on a 0.150-inch grid, using the embedded microstrip and strip transmission line configuration, and still stay within reasonable crosstalk limits. At 50-ohm characteristic impedance, however, four signal layers with the required 0.100 inch grid become practical and the benefits of considerably reduced crosstalk values are available.

Single and Sequentially Laminated Board Assemblies

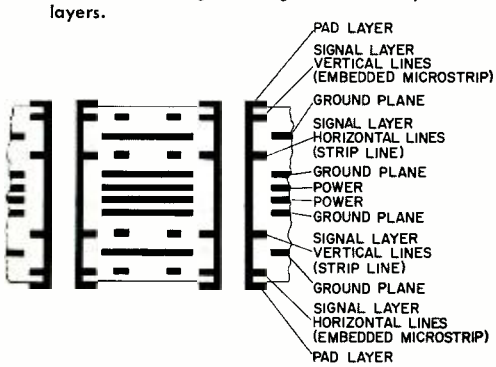
The present Spectra 70-45/55 multilayer platter (Fig. 2) includes six copper layers (two with etched signal lines) interleaved with appropriate dielectric layers, all of which are laminated together at one time to form a homogeneous assembly. Plated-through holes at pads located on a 0.125-inch minimum grid are used for all interconnections between any of the six copper layers. Connector pins mating platter wiring with plug-in card wiring can be used in alternate 0.125-inch grid locations, while in other grid locations, plated-through holes are used for terminating resistor pins or without pins to serve as *via* holes. Via holes are those plated-through holes used to interconnect wiring within the platter assembly, but do not connect directly to outside assemblies through a pin. In the Spectra 70-45/55 platter, via holes interconnect wiring only on the two signal planes. Via holes are a necessity to provide cross-over connections. In the Spectra designs, a ratio of three via holes to two signal-connector pins is necessary.

When more than two signal layers are incorporated in a singly laminated platter assembly (Fig. 4) all connector pin locations and via hole interconnections between any two signal layers will still require a plated-through hole through the entire board assembly. It would be advantageous to increase via hole usage and efficiency in multilayer board assemblies using more than two signal planes if some method could be devised to allow more than one via hole connection to be made at a plated-through via hole location.

One way of effecting more than one via hole connection at a via hole location is by using the sequentially laminated type of multilayer board assembly (Fig. 5c). Plated-through holes going through the entire board are used for connector pins mating with interconnections on other assemblies. Via holes can extend only partially through the board as shown, allowing more than one via hole interconnection at a grid location point.

The 12-copper-layer sequentially-laminated assembly (Fig. 5c) would be constructed by using two laminating steps, increasing fabrication complexity and cost. The particular assembly shown

Fig. 4—Singly laminated multilayer board cross section, including four signal and two power layers.



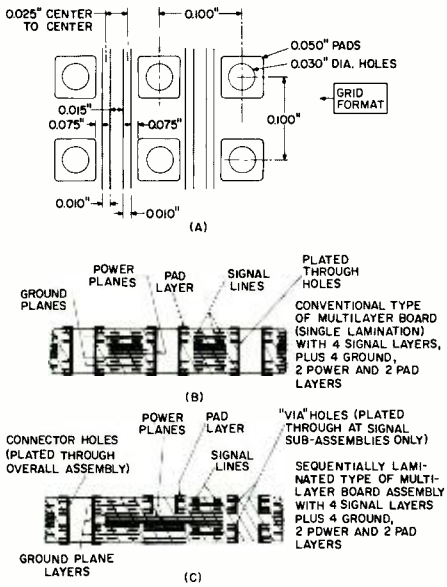


Fig. 5—Proposed platter configuration, 0.100-inch grid, and alternate cross-sectional formats.

would be first treated as three separate singly laminated boards: one for laminating the top five copper layers, the second for the two internal power layers, and the third for the bottom five layers. Via-hole locations for each of these separate sections would be drilled and plated-through independently. The three separate sections would be laminated together in the second laminating step, with connector pin holes drilled and plated-through after this second lamination.

For a platter which incorporates more than two signal layers on the outside surfaces (such as the four-signal-layer, singly or sequentially laminated boafd assemblies proposed) the simple method of physically cutting printed lines is not applicable for removing connections on internal layers. A modification technique which severs internal connections and provides for addition of discrete external wires is under development for ease of platter modification and maintenance.

Signal Connector Design

For the ½-ns signal risetimes which could be expected for a 1 ns worst case design, full amplitude reflections are possible in impedance discontinuities of as short as 2½ inches. This distance includes both the length of the hot signal conductor plus the effective length of the ground circuit path.

For example, in a 50-ohm system, a connector of 100-ohm effective impedance 2½ inches long would mean a voltage reflection coefficient (VRC) of:[7]

$$\text{VRC} = \frac{\text{Reflected voltage}}{\text{Forward voltage}} = \frac{Z - Z_o}{Z + Z_o} = \frac{100 - 50}{100 + 50} = \tfrac{1}{3}.$$

Shorter effective connector lengths would result in proportionally lower reflections; that is, a 1-inch length would produce ($\frac{1}{2.5}$) x ($\frac{1}{3}$) = $\frac{1}{7.5}$, or a 13.3 percent reflection. To attenuate amplitude of reflections, a separable connector must be designed either with its controlled impedance being the same as the system characteristic impedance, or with its overall length (signal plus ground circuits) reduced.

Crosstalk between signal pins of a multipin separable connector must also be critically appraised, and can be expected to be a limiting item at the close 0.100-inch grid spacings planned.[7]

Present commercially available separable connectors are inadequate from both signal reflections and crosstalk performance requirements for the fast risetimes expected. Suitable designs are possible, however, through use of shorter hot signal conductors, shortened ground paths, and additions of ground planes which will both isolate the various signal circuits within the connector and effectively control characteristic impedance of the transmission lines built into the connector.

Power Connector Design

Supplying input DC power to plug-in board assemblies of past designs has usually been accomplished by using the same contacts within the separable connector as used for signal-circuit connections. Current and voltage requirements for plug-in boards have been comfortably within the electrical rating of these contacts, satisfying the only important electrical consideration.

The higher operating speed goals of the proposed design involves increased power requirements due both to active device inefficiencies at high frequencies and to the well-known relationship between the electrical energy W supplied to a circuit and risetime:

$$W = EQ = EIt = Pt,$$

where E is the source EMF, Q is charge, I is current, t is time, and P is power. As risetime, t, decreases, P must increase. The higher packaging densities involved with the high speed design also increases power requirements per plug-in assembly, since more circuits will be mounted on each card. These factors lead to increased current handling capability being required of the connector interfacing the plug-in and platter assemblies.

The increased current and faster signal risetimes bring about the need to reduce the inductance of the power connector (to eliminate voltage spike, $E = L\,dI/dt$, across the connector). Use of current-mode-logic gates, where the average current is relatively constant because of the reciprocal current steering action of the two output transistors, minimizes, but does not eliminate, power distribution problems stemming from series inductance within the DC power lines.

To reduce the series inductance of the power line, the power connector should be designed as a low-impedance transmission line, where the hot and ground leads are placed in close proximity. Connector length must be kept short, including the ground circuit.

The power connector requirements can probably most easily be met for the plug-in assembly/platter structure by designing the DC power separable connector as part of the plug-in-card edge-guide assembly normally used only to ensure precise card alignment. Large cross-sectional area conductors and contacts can be molded within the edge guide to achieve the minimum inductance, resistance, and impedance characteristics.

EXPERIMENTAL RESULTS

The packaging concepts outlined in this article have been verified through measurements on working feasibility models. Design and electrical performance data on the microstrip, embedded microstrip, and strip-line transmission line geometries are available as a result of an experimental program. The electrical information encompasses the 40- to 150-ohm range of characteristic impedance, and corresponding data on propagation delay, low and high frequency attenuation, and crosstalk. The physical range covers line widths down to 3 mils, line spaces down to 20 mils, and dielectric thicknesses down to 8 mils, on full-sized 18 x 18-inch platters.

A test vehicle incorporating active high-speed devices mounted on plug-in boards and interconnected on a 12-copper layer (4-signal layer) singly laminated platter has been constructed. Satisfactory operation at logic speeds in the 4-ns pair-delay, 1-ns risetime range has been demonstrated.

Presently under development in Advanced Technology is a full-scale test vehicle incorporating approximately 2000 logic gates packaged in large array and standard 14-lead flatpack packages. Plug-in board assemblies include four controlled impedance layers (12 copper layers) interconnected upon a full size 19 x 20-inch six-signal layer (19-copper layer) sequentially laminated platter.

ACKNOWLEDGEMENT

Multilayer printed circuit boards used in this program were constructed by RCA Central Engineering, Camden, who developed the fabrication techniques required to implement the new assemblies.

REFERENCES

1. *Reference Data for Radio Engineers*, 4th edition, International Telephone and Telegraph, Inc., New York, p. 554.
2. F. E. Terman and J. M. Pettit, *Electronic Measurements*, second edition, McGraw-Hill, p. 259.
3. *Design and Fabrication of Nanosecond Digital Equipment*, Engineering Guide, RCA Applied Research.
4. A. T. Ling, *private communication*, 1965.
5. J. J. Surina, *RCA Internal Report*.
6. J. J. Surina, *RCA Internal Report*.
7. Reference 1, page 562.
8. Harris, Radzelovage and Springfield, "A Multiple Signal Pluggable Connector for a High Speed Computer System," Sixth International Electronic Circuit Packaging Symposium, San Francisco, (Aug. 23, 1965).

COMPUTER CIRCUIT NOISE IMMUNITY AND SYSTEM NOISE

This article provides a broad coverage of the Spectra 70 and an advanced computing system in terms of their circuit noise immunity and system noise sources. The fundamental parameters of each system are detailed and a general evaluation of noise sources in high speed computer systems is discussed. Further, a graphical technique for calculating circuit noise immunity is detailed. With this knowledge, the logic circuit and systems designers can make favorable and economical tradeoffs without impairing system reliability or increasing circuit costs.

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THE University of Illinois under an award from the Department of Defense will design, develop, and operate a large-scale highly parallel computing system—ILLIAC IV. RCA was involved in Phase I of this project which was a study directed toward developing a system design, optimized on the basis of hardware and software considerations. The results of these studies are the basis for this comparison of a "next generation" computer with the existing Spectra computer.

In terms of circuit requirements, the Spectra and ILLIAC IV computers are quite similar. Each uses current-mode-logic circuits in a monolithic silicon integrated form. The logic pair delays are 24 ns for the Spectra 70-45/55 computers and 5 ns for the advanced computer. Of interest here is the faster risetime circuits associated with the decreased logic delay (3.5 ns and 0.4 ns respectively). The packaging requirements of these systems are substantially different and can be characterized adequately by their transmission line impedance. For the Spectra, 100-ohm lines are used while the advanced computer will use 50-ohm lines.

Final manuscript received September 21, 1967.

The design of computing systems has always involved a number of compromises between many conflicting requirements; depending on the technology employed, and problems to be solved, a priority level was established for each requirement. Today, with the advent of high speed circuits and high density packaging, the most stringent requirement, aside from the basic gate delay, is noise immunity. In general, as faster system risetimes are experienced, the greater is the requirement for high circuit noise immunity.

To manufacture high speed circuits of the next generation will require more complex fabricating processes and higher resolution artwork. The result is that the circuit specification yield compared to its slower speed predecessor (Spectra) drops considerably if the same system noise immunity is required. Thus two alternatives—accepting reasonably priced, reduced noise immunity circuits or higher priced maximum noise immunity circuits—are available to the system designer. When considering that fast risetime circuits may not only increase the magnitude of machine noises but also introduce new sources of noise, the above tradeoff is not easily made.

NOISE IMMUNITY

The circuit schematic for a Spectra-70 gate is shown in Fig. 1. Transistor $Q2$ is at a fixed bias of -1.2 volts provided by the bias driver. As the input (V_{IN}), which for this example, is assumed to be -0.8 volt initially, approaches -1.2 volts $Q1$ will start turning off. When $Q1$ turns off, the NOR output will change from -1.6 volts to -0.8 volt and the OR output from -0.8 volt to -1.6 volts. Therefore the circuit provides both inverted and noninverted outputs for a given input.

The -0.8 volt level, which is the most positive level, will be defined as the logical ONE level, and the -1.6 volts level will be defined as the logical ZERO level. The operating boundaries of the gate are shown in Fig. 2. In the following discussion, note that "greater than" and "maximum" means more positive and "less than" and "minimum" means more negative.

For any input voltage excitation greater than or equal to the MIN-ONE level, the NOR output voltage will indicate a level less than or equal to the MAX-ZERO level and the OR output will indi-

Fig. 1—The basic Spectra 70 gate circuit.

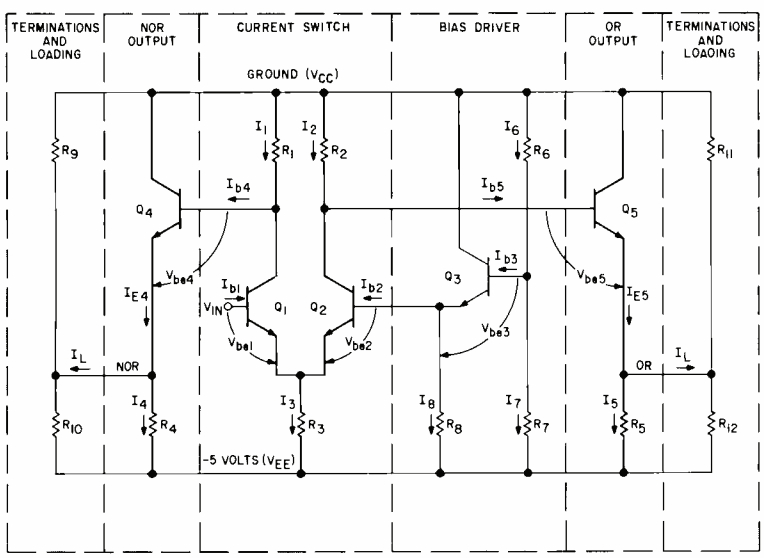


Fig. 2—Logic levels for Spectra gate.

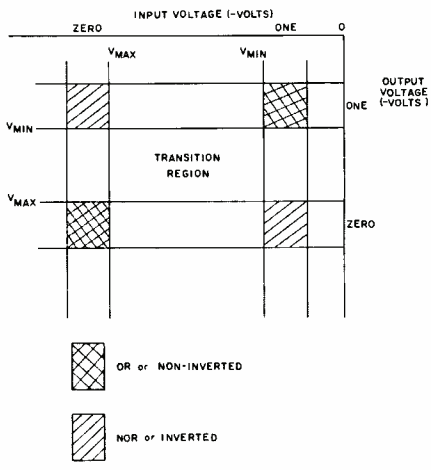


TABLE I—Logic Level and Bias Driver Equations

Voltage Input High

OR

$$E_{OR} = \frac{(R_2/R_5)\,V_{EE} - \beta_5 V_{be5} - I_L R_2}{\beta_5 + (R_2/R_5)}$$

NOR

$$E_{NOR} = \frac{(R_1/R_4)\,V_{EE} - (R_1/R_3)\,\alpha_1\beta_4\,(V_{1N} - V_{be1} - V_{EE}) - \beta_4 V_{be4} - R_1 I_L}{\beta_4 + (R_1/R_4)}$$

Voltage Input Low

OR

$$E_{OR} = \frac{(R_2/R_5)\,V_{EE} - (R_2/R_3)\,\alpha_2\beta_5\,(V_{REF} - V_{be2} - V_{EE}) - \beta_5 V_{be5} - R_2 I_L}{\beta_5 + (R_2/R_5)}$$

NOR

$$E_{NOR} = \frac{(R_1/R_4)\,V_{EE} - \beta_4 V_{be4} - R_1 I_L}{\beta_4 + (R_1/R_4)}$$

BIAS DRIVER

$$V_{REF} = \frac{V_{EE} - \dfrac{R_7}{\beta_3}2I_{b2} + \dfrac{R_7}{R_8}\dfrac{V_{EE}}{\beta_3} - V_{be3}\left(\dfrac{R_6 + R_7}{R_6}\right)}{\dfrac{R_6 + R_7}{R_6} + \dfrac{R_7}{R_8}\dfrac{1}{\beta_3}}$$

cate a level greater than or equal to the MIN-ONE level.

For any input voltage excitation less than or equal to the MAX-ZERO level, the NOR output voltage will indicate a level greater than or equal to the MIN-ONE level and the OR output will indicate a level less than or equal to the MAX-ZERO level. V_{MIN} ONE is the minimum allowed input ONE level in a logic system; V_{MAX} ZERO is the maximum allowed input ZERO level in a logic system. Therefore, restricted areas of operation have been defined for the gate as shown by the cross-hatched areas. The operation of the gate should exist within these boundaries under any steady-state condition of operation of the gate.

Various interpretations of circuit noise immunity and the effects of machine noises in system operation have been made. In this work, circuit noise immunity is defined as the magnitude of change of input signal from a steady-state input level that will produce a detectable output level change. Also, strictly speaking, both a DC and AC circuit noise immunity exists. The AC noise immunity for the Spectra circuit was experimentally determined to be greater than DC noise immunity. The relationship of AC-to-DC noise immunity is shown in Fig. 3.

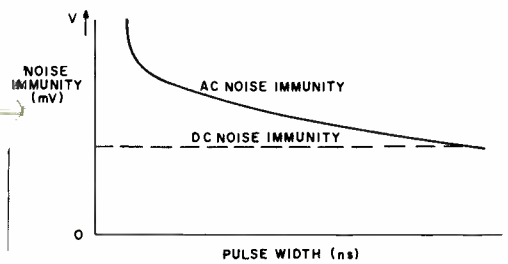
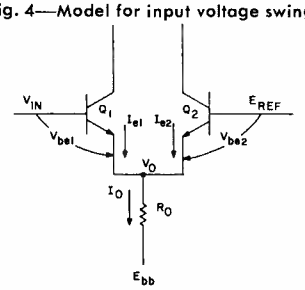


Fig. 3—AC and DC noise immunity relationship.

Fig. 4—Model for input voltage swing.

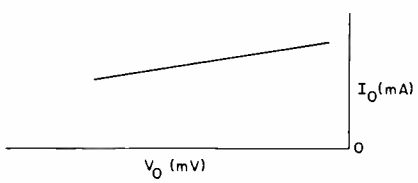


The noise immunity of this circuit is analyzed by developing worst-case equations (Table I) of the following:[1]

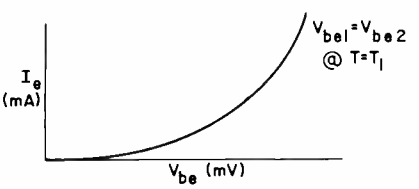
1) Bias driver output voltage;
2) Minimum value of the high level voltage (0.8 volt);
3) Maximum value of the low level voltage (1.6 volt); and
4) Minimum value of the input swing voltage required to switch the transistors.

By the use of a DC computer-map program, the equations listed in Table I with their appropriate device characteristics, tolerance, and thermal coefficients, can be used to describe the logic levels and bias driver voltage over the temperature range of interest.[2]

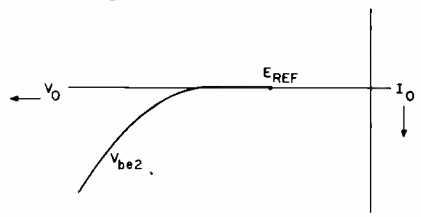
The next analytical step is computation of the minimum value of voltage input swing required to switch the current-switch transistors. For this analysis, consider Fig. 4 which shows the basic current switch under analysis.[11] By using the relationship $I_o = (E_{bb} - V_o)/R_o$, I_o can be plotted as a function of V_o. This yields the following curve:



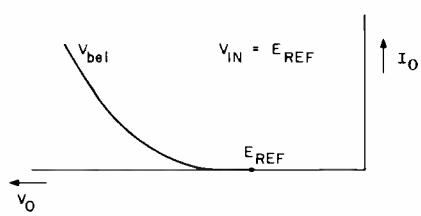
Next we make the valid assumption that $Q1$ and $Q2$ transistors are identical so that V_{be1} is equal to V_{be2} for given values of current. This follows from the fact that transistors $Q1$ and $Q2$ are on the same integrated circuit chip.



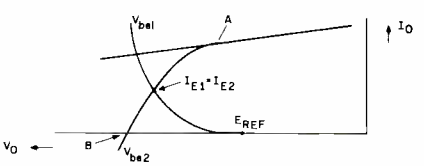
The V_{be} data used in the analysis are specifically for a two-stripe geometry integrated circuit transistor at the outer limits of the V_{be} spread. A two-stripe transistor is characterized by the number of contacts in the base and emitter diffusion areas (1b, 1e). The curve can then be modified for the particular temperature of interest by using a V_{be} temperature coefficient of 2mV/°C. From the nodal point, designated V_o, the current I_{E2} and the quantity $(V_{be2} + E_{REF})$ are seen to be negative. This yields the following plot.



Since the currents I_{E1} and I_{E2} are equal when $V_{IN} = E_{REF}$, the following relationship can be derived:



The composite characteristic would then be



Transistor $Q1$ is turned on fully by shifting V_{be1} to the right until it intersects point A so that $I_{E1} = I_o$. Shifting V_{be1} to the left until it intersects point B will make $I_{E1} = 0$ so that $Q2$ is fully on and $I_{E2} = I_o$.

The results of the complete analysis are shown in Fig. 5. These data are from

an unterminated line condition, and this example represents but one of many test cases run. For convenience the noise immunity of a typical case at the high and low levels at 70°C is given.

BASIC DIFFERENCES BETWEEN SPECTRA AND ILLIAC TYPES

Parameters

To make some statements in regard to noise immunity, it is first necessary to discuss the parameter changes in the two systems.

System Noises

There are many sources of noise in digital computer systems. Only those noises related to the circuit, interconnections, and power distribution are considered; noises related to radiation, static charges, or mechanical switching are not. One of the first considerations is circuit risetime, which forms the base for many of the calculations. Fig. 7 shows the marked decrease in computer risetimes for various systems. As an indication of expected risetimes, consider the idealized circuit of Fig. 6.[5]

The switch represents a transistor, the load capacitance (C), and the TERMINATING resistance (R_o). Such a circuit is closely approximated by any high speed device driven by a constant current. Then $I = C\,\Delta V/\Delta t$, where Δt is risetime, ΔV is voltage swing, and C is $n(C_i + C_s)$; and where n is circuit fanout. C_i is circuit input capacitance; and C_s is capacitance of connection to transmission line. I is the available current which is equal to the supply voltage divided by the total power of the supply. Therefore

$$t_r = [n\,(C_i + C_s)\,\Delta V]\,V_s/P_s$$

For the case, $n\,(C_i + C_s) = 20$ pF, $\Delta V = 0.8$ V, $V_s = 5$ V, and $P_s = 200$ mW:

$$t_r = (20 \times 10^{-12})\,(0.8)\,(5)/200 \times 10^{-3} = 0.4 \text{ ns}$$

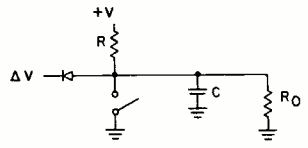


Fig. 6—Idealized circuit for risetime evaluation.

For the next generation of machines, risetimes of 0.4 ns may be expected.

Generally, crosstalk and reflection phenomena and the power distribution scheme are the sources of machine noise. Specifically, in the circuit this noise is attributable to phantom-OR connections, feedthrough noise, OR-NOR level difference, actual capacitive loading and OR/NOR unbalanced loading. Fanout noise sources are serial net loading along with radial net undershoot and overshoot. Platter-generated noise includes crosstalk, impedance mismatch, capacitance of via holes, and the DC platter drop. Plug-in crosstalk and power distribution noise, and wiring crosstalk and mismatch are additional sources. Of course connection discontinuity is always a potential noise source.

The details of these calculations for the Spectra and ILLIAC type machines are contained in Reference 4. For our purposes, cases will be selected to show fundamental differences and how they are handled.

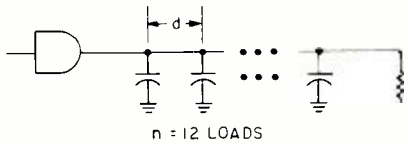
First, consider a major source of noise: the serial net loading noise. The percent reflection will reduce for the advanced computer case even though its risetime is 4 to 5 times as fast; however, this is not necessarily true of all cases. The gate input capacity for both circuits is assumed to be 5 pF. If the product of the line impedance and capacitance per load is kept constant, the value of reflection is kept constant.

$$Z_1 C_1 = \Gamma_1$$
$$Z_2 C_2 = \Gamma_1$$

Solving for C_2,

$$C_2 = \frac{Z_1 C_1}{Z_2}$$

$$C_2 = \frac{50\ \Omega}{100\ \Omega} \times 5 \text{ pF} = 2.5 \text{ pF}$$



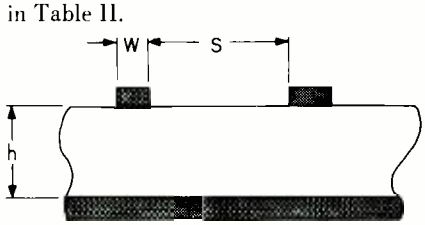
Therefore, in going from a 100-ohm to 50-ohm impedance system, the effective capacity is reduced by one-half. Design curves from Reference 7 give

Spectra	*Advanced Computer*
$rt = 4$ ns	$rt = 1$ ns
$Z_o = 100$ ohms	$Z_o = 50$ ohms
$C = 5$ pF	$C = 2.5$ pF
$n = 12$ LOADS	$n = 12$ LOADS
3-inch electrical spacing	3-inch electrical spacing
Reflection = 25.5%	Reflection = 13%

Thus we have the interesting result that the percent reflection decreases for the faster risetime system. Again caution is needed in the analysis of particular cases.

Second, consider the platter crosstalk noises. Crosstalk effects can be conveniently compared by the two crosstalk constants, K_B (back crosstalk) and K_F (forward crosstalk). The equations are: $V_B = K_B V_o$, where V_B is the magnitude of backcrosstalk and V_o is the input swing; $V_F = K_F\, l\, dV/dt$, where l is the line length and dv/dt is the slope of the input signal.

The platter cross-section appears as in the sketch below; W and S are defined in Table II.

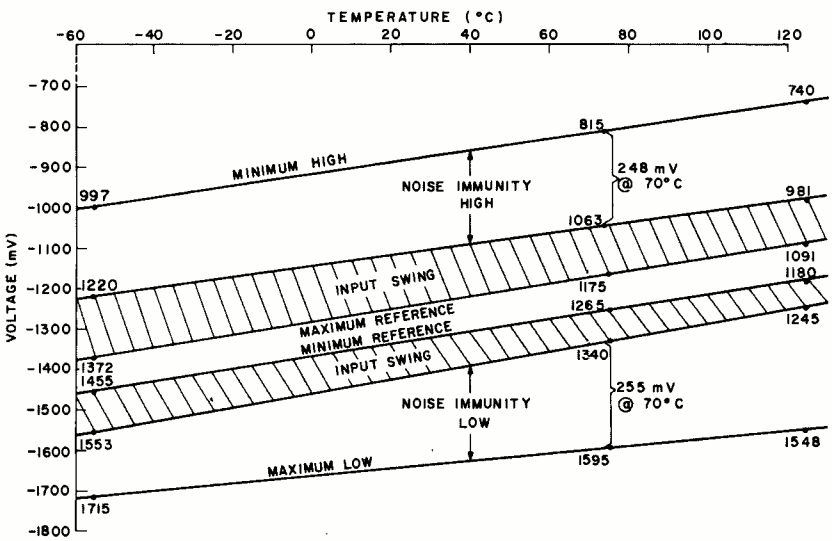


In Table I, the Spectra line spacing was 25 mils while the advanced computer was 15 mils. The K_B would increase as the line spacing gets closer.[7] Note however that in going from a 100-ohm to 50-ohm system, the H decreases significantly. The result is that K_B decreases.

Both the platter and plug-ins in the ILLIAC computer will use coated transmission lines. It has been shown that the forward crosstalk constant K_B of a coated line can be reduced to zero.[8] Therefore the forward crosstalk is less in the advanced machine than in the Spectra. Again this is an interesting result since V_F is proportional to the risetime.

Thus, two opposite results, in terms of crosstalk and reflection, have been

Fig. 5—Noise immunity as a function of operating temperature.



produced. Both are attributable to the packaging format chosen. Normally, these phenomena would be expected to increase when going from a 4 ns to a 1 ns system. One may begin to conclude that a faster risetime system is easier to build so that a reduced noise immunity circuit may be used. However, this is not the case. Actually, while some of the noise sources are decreasing in value others are increasing.

Consider the signal connector for both the Spectra and the advanced computer. The Spectra connector is not a controlled impedance connector. The signal connector in the advanced computer must be a controlled impedance connector since it may have to handle 0.4 ns risetimes. Therein lies the problem: For risetimes of 0.4 ns, impedance discontinuities could occur for line lengths of 1 inch. Therefore, the separable connector should have its overall length (signal plus ground) reduced. In addition, the effective connector impedance should be as close to 50 ohms as possible. For example, if the effective impedance were 80 ohm instead of 50 ohms, the percent reflection would be

$$\Gamma = \frac{Z - Zo}{Z + Zo} = \frac{80 - 50}{80 + 50} = 23\%$$

Crosstalk between signal pins of a connector is now a major problem for operation at the risetimes of interest.[10] In addition, the grid spacing of the platter has been reduced from 125 mils to 100 mils for the advanced computer, thus placing the pins closer together. Again, shorter signal conductors must be used, ground paths must be shortened, and ground planes must be added to isolate the various signals on pins in the same proximity.

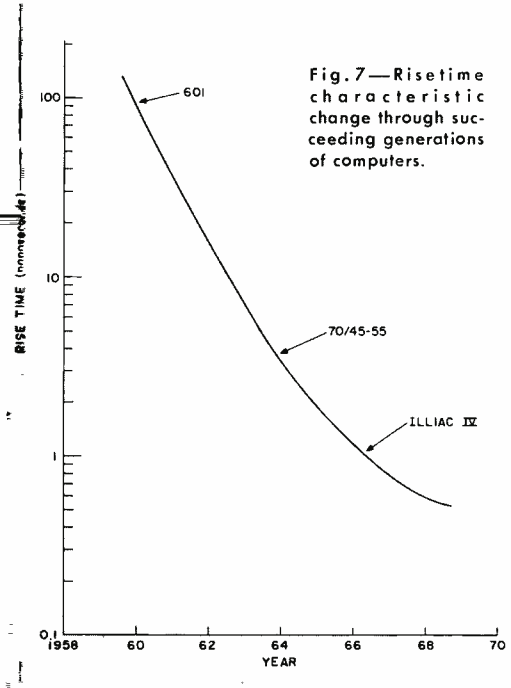


Fig. 7—Risetime characteristic change through succeeding generations of computers.

TABLE II—Parameter Changes

Parameter	*Spectra 70-45/55*	*Advanced Computer*
Circuit		
Pair Delay Worst Case	24 ns	5 ns
Noise Immunity	250 mV	?
Rise Time Minimum	3.5 ns	0.4-1 ns
Circuit Dissipation	125 mW	100 mW
Input Capacitance	5.5 pF (av.)	4 pF (av.)
Line Termination	100 ohms on platter	50 ohms on Plug in
Line Termination Dissipation	58 mW (av.)	115 mW (av.)
Platter		
Signal layers	2	4 to 6
Characteristic impedance	100	50 ohms
Line spacing	25 mils (S)	15 mils
Line widths	10 mils (W)	10 mils
Distributed capacitance	1.7 pF/in	3.7 pF/in
Via hole capacitance	1 pF	1.5 pF
Plug-ins per platter	116	50
Grid spacing	125 mils	100 mils
Plug-in		
Size	3 x 4 inches	7 x 8 inches
Impedance	Not Controlled	50 ohms
Gates per plug-in	12 (av.)	120 (av.)
Connector	48 pins—not designed to handle 3.5-ns risetimes	120 pins—to be designed to handle 0.4 ns risetimes

Another major problem area is the actual power distribution system. The next generation of computer will be a high gate-density system. Therefore, a very low impedance system will be needed to handle the increased currents and faster risetime circuits.

CONCLUSIONS

Spectra is a computer that has been built and for which the circuit noise immunity and appropriate wiring rules have proven to be adequate. ILLIAC IV represents a class of computing machine that may be the very next generation computer in terms of the circuit densities and circuit risetimes. This type of system requires close scrutiny in terms of evaluating system noises and specifying circuit noise immunity.

In the Spectra, a one-third allocation of noise immunity was made for reflections (80 mV), crosstalk (80 mV), and power distribution (80 mV).[6] It is very unlikely that a faster risetime computer could utilize a circuit with less than 240 or 250 mV of noise immunity. Yet this prospect exists because the artwork and process problems associated with smaller geometry devices are expected to significantly increase the cost of the new high speed circuits.

One step toward the realization and use of a reduced noise immunity circuit is first in understanding the strong interplay between circuits and packaging. With a knowledge of both circuits and packaging parameters, a re-allocation of noise immunity may be made to handle the noise problems of new design areas such as a separable controlled impedance connector.

ACKNOWLEDGEMENT

In addition to the references cited, further acknowledgement is given to the EDP circuit design group under S. E. Basara for past conversations.

BIBLIOGRAPHY

1. M. D'Agostino, "Study of High Speed Digital Integrated Logic Gate Circuits" RCA Internal Report (Aug. 1965).
2. C. Pendred, "DC Map Program," RCA Internal Report.
3. M. J. Flynn, "Complex Integrated Circuit Arrays" *Electronics* (July 11, 1966) p. 111.
4. J. J. DiGiacomo, "Noise Immunity in Illiac IV Circuits", RCA Internal Report (Sept. 1966).
5. A. Chen, A. Sheng, "286/2861 AC Power Distribution System" RCA Internal Report, (June 1965).
6. S. E. Basara, "The Impact of Monolithic Integrated Circuits on Computer Design" RCA Reprint PE-257 (Oct. 1965).
7. J. J. DiGiacomo, A. Feller, H. R. Kaupp, J. J. Surina et al., "Design and Fabrication of Nanosecond Digital Equipment", RCA Report, (Mar. 1965).
8. H. R. Kaupp, "Effects of Coating Microstrip Transmission Lines" RCA Report (Jan 1966).
9. J. Surina, "Packaging of Nanosecond Digital Arrays using Multilayer Circuit Boards" (June 1967).
10. J. Harris, W. Radzelovage, W. Springfield, "A Multiple Signal Pluggable Connector for a High Speed Computer System", IBM Corporation.
11. D. H. Chung, J. A. Palmieri, Design of ACP Resistor-Coupled Switching Circuits," *IBM Journal* (Jul 1963)

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THE STANDARD INPUT/OUTPUT INTERFACE FOR THE RCA SPECTRA 70

This paper describes the major aspects of the RCA Spectra 70 standard input/output interface. It is not the purpose of this paper to provide the detailed definition of interface signals and timing but rather to indicate what the interface is and how it is used.

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THE STANDARD INTERFACE defines the logical, electrical, and mechanical requirements for interconnecting the Spectra 70 processors and the control electronics in peripheral devices. As such, the interface definition is influenced by, but not limited to, the design of a single processor or control electronics. In fact, the interface satisfies the requirements of two basically dissimilar classes of processors and all Spectra control electronics units.

BEFORE SPECTRA

In state-of-the-art designs of input/output immediately before the Spectra 70 series, the interfacing logic (excluding some nominal device electronics) between a processor and a device was integrated within the design of a processor —i.e., interfacing logic (control modules) was packaged within the processor or in a rack immediately adjacent. This integration permitted control module designers to use processor timing pulse and common packaging. However, some problems in cabling and packaging were experienced (e.g., in the RCA 3301 system where up to 100 lines might be required in a control module/processor interface and where certain devices were restricted to the modes to which they might be attached). Additionally, input/output instructions were designed to the characteristics of specific devices. Within the RCA 3301 System, greater configuration flexibility was achieved with increased commonality of I/O instructions so that as new devices became available they could be easily added to the system. However, control modules were still incorporated within the processor. The point here is not to critically view those systems by hindsight; they satisfied the requirements for which they were designed (to perform as stand-alone systems with no need to interchange or extend the life of peripheral devices). However, the requirements of the Spectra 70 series, by contrast, are quite divergent.

Final manuscript received July 28, 1967.

GEORGE J. SMITH received the BEE from New York University in 1957. He is currently doing graduate work at the University of Pennsylvania. Before joining RCA, Mr. Smith was employed at Bell Telephone Laboratories in systems design of message store and forward systems. He joined EDP Engineering in 1959 and was involved in the application of computer-based message-switching systems, including the systems design, test, and installation of an on-line management information system. Additional activities include the planning and implementation of the standard I/O interface in Spectra 70 series processors and control electronics.

CONCEPTUAL ASPECTS

The initial planning of the Spectra 70 Systems included four processors and approximately twenty-four peripheral devices. This has subsequently been expanded so that currently six processors —the 70/15, 75/25, 70/35, 70/45, 70/46, and 70/55—and over thirty-eight peripheral devices are included within the series. Within this series, two classes of processors are represented: the 70/15 and 70/25 in one class and the 70/35 processor and higher models in the other. The principal distinctions between the two classes are based on packaging and functional requirements. The early members of the series—the 70/15 and 70/25 processors—are packaged using discrete components and are instruction-code compatible with one another. The later additions to the series use integrated circuit techniques and are instruction-code compatible with the IBM 360 systems (except for the privileged operations including input/output). However, functional compatibility had to be achieved in input/output operations. This compatibility was extended to include the organization of the two types of processor input/output channels: multiplexer and selector. At this same time, it was desirable to establish compatible input/output operations with foreign licensees with whom we were then working.

In summary, then, the underlying requirements for developing a standard input/output interface were:

1) To design one set of peripheral devices which could be attached, without modification, to any Spectra 70 processor;
2) To provide for input/output operations which were functionally compatible with the IBM 360 system;
3) To provide a compatible subset of input/output operations for the 70/15 and 70/25 processors;

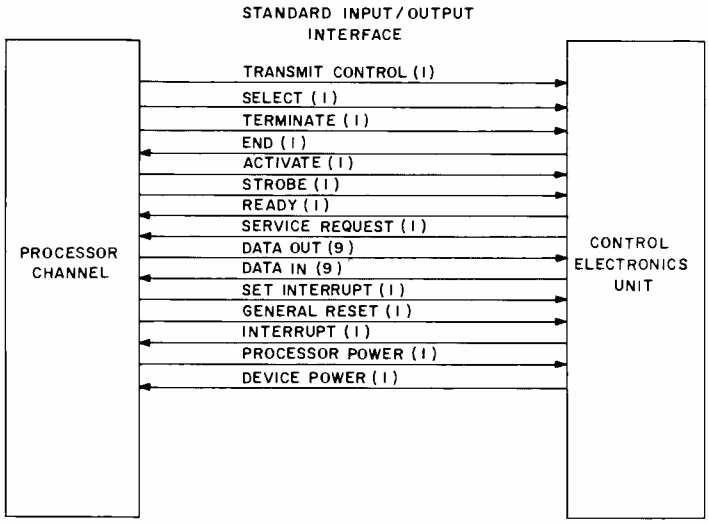


Fig. 1—Connections between the processor chonnel ond the control electronics.

4) To provide a flexible means of processor/peripheral connection which is independent of device speed and operating characteristics; and
5) To accommodate the needs of foreign licensees.

PHYSICAL ASPECTS

Interface Terminals

Peripheral devices are connected to processors by channels and control electronics units; channels direct the flow of information between processor storage and control electronics units. Byte count and data addresses are maintained in the processor. A control electronics unit provides the logic to adapt the standard signal sequences of a channel to the characteristics of a peripheral device.

Configurations

The connection between a processor channel and a control electronics unit is provided by the RCA Standard Interface (Fig. 1). A channel is connected to control electronics by means of trunks, which consist of the complete set of 31 interface lines required to terminate each control electronics on a channel. The number of control electronics units which can be attached to a channel is a function of the processor and the type of channel, i.e., multiplexer or selector. A multiplexer channel can time share its facilities with as many as 256 simultaneously operating devices. This number is a function of a particular processor design. The facilities of a selector channel cannot be used by more than one device at a time (i.e., for an on-line operation such as a data transfer).

Interface Signals and Lines

Referring to Fig. 1, the signals and lines of the standard interface are functionally associated into six groups: qualifiers, operation limiters, service control, data lines, miscellaneous control and power interlocks.

Qualifiers (Transmit, Control, Select): The logical states of the transmit control and select lines are used to indicate that:

1) A processor is transmitting an address,
2) Data or control information is on the data-out lines,
3) A control electronics can transmit address or status, or
4) Data information is on the data-in lines.

Operation limiters (Terminate, End): The function of these signals is to indicate the end of an input/output operation. The termination of an operation can be initiated by a channel or by a control electronics unit.

Service control (Activate, Strobe, Ready, Service Request): The function of these lines is to establish a link between a processor and a control electronics unit for the initiation of an input/output operation. or for the transfer of a data or statue byte.

Data lines (Data Out, Data In): Data-out lines are used to transmit address, control, or data. Upto 256 devices can be addressed over these lines. The number of devices which can be physically attached to a control electronics unit is a function of the specific unit. Data-in lines are used to transmit data or status information. Information on data out or data in is transmitted bit parallel. byte serial.

Miscellaneous control (Set Interrupt, General Reset, Interrupt): These signals are used for those functions not directly required for a byte transfer but for related operations. Set interrupt is used in conjunction with the interrupt subsystem if the 70/35, 70/45, and 70/55 processors to indicate to software when a prescribed number of bytes have been read or written. The interrupt signal is also used to indicate completion of an input/output operation or that a device is requesting a service. The General Reset signal is used to reset a control electronics unit to a quiescent state.

Power Interlocks (Processor Power, Device Power): The functions of these lines are to indicate that power is on in the processor and a control electronics unit respectively.

Systems Topography

Control electronics units are attached to processor channels by a single cable up to 100 feet long. The cable consists of thirty-seven twisted-pair conductors for the standard interface signals. Control electronics/device power is provided in a separate cable.

OPERATIONAL ASPECTS

Device Addressing

Device addresses are transmitted over the Data-Out lines. A device address consists of 8 bits, thus up to 256 addresses can be specified on a channel. A device address cannot be duplicated on a channel but can be duplicated within a system.

Device Operations

Device operations are specified in command codes which are transmitted over Data-Out lines. Two sets of command codes have been specified. The first of these is a minimum compatible set common to all Spectra 70 processors. This set with one exception is used by software. The second set, generated by hardware. is used for control functions which are transparent to software. The bit assignments for the first set are described as follows:

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
X	X	X	X	0	0	0	1	*Command*
X	X	X	X	0	0	1	0	*Sense*
X	X	X	X	0	0	1	1	*Read backward*
X	X	X	X	0	1	0	0	*Write*
X	X	X	X	0	1	0	1	*Erase*
X	X	X	X	0	1	1	0	*Read*
X	X	X	X	0	1	1	1	*Send status*
X	X	X	X	1	0	0	0	*Write control*
X	X	X	X	1	0	0	0	*No operation**

X: Don't care (0 or 1)
* Hardware generated

These commands are used to transfer information between processor memory and a peripheral device. In general, the

names of the commands are descriptive of the operation which is performed and will not be further elaborated here except to note again that data, control, address, and sense bytes are transmitted over data-out or data-in lines. Distinction among the kinds of data is made in a control electronics or a processor depending on the command being executed.

Set-1 commands can be issued singly by software or from a list of chained commands the subsequent issuance of which does not require program interruption.

Device Status

Two levels of device status are reported: 1) a standard device byte (SDB) which is common to all devices; 2) sense bytes (transferred to a processor as a result of a sense command) which can be uniquely specified for each device. Sense-byte bits are provided for detailed software tests of device status. The SDBs give a general description of device status and include status information for both hardware and software. The following list describes the bits and functions of the SDB:

Bit Position	*Name*	*Function*
2^0	Status modify	Used by the 70/35, 45, and 55 processors in command chaining operations. Not used in the 70/15 and 25 processors.
2^1	Inoperable	Indicates the operating status of a previously addressed device.
2^2	Secondary indicator	Indicates the occurrence of a status condition.
2^3	Device end	Indicates that a device has completed an operation and no longer requires the use of a control electronics/channel.
2^4	Control busy	Indicates that the control electronics is busy and is not available for another operation.
2^5	Device busy	Indicates that the addressed device is busy and is not available for another operation.
2^6	Termination interrupt pending	This bit is set as a result of a command generated by hardware at the end of an I/O operation. The effect is to pass the I/O completion for subsequent processing by software.
2^7	Manual request	This bit is used to indicate that an off-line request for program service has been made.

The Standard Device Byte is tested by hardware during command initiation and termination. Following termination, it is available to software for testing the results of an operation.

Channel Connectivity

All control electronics units designed to the requirements of the standard interface can be interchanged without modification between multiplexer or selector channels. Distinction between the two signal sequences is made in the channel. This provides greater flexibility in system configuration where the selection of channel attachment is limited by device rate alone and by no other device characteristic.

Transfer Rate

As a function of interface signal timing, a maximum information transfer rate of 1.3 megabytes is possible. Practically, however, this rate is reduced in the different Spectra processors depending on their channel design requirements.

Interface Operations

A detailed description of interface operations is beyond the scope of this paper. Further, no description of interface operations would be complete without reference to a specific control electronics or processor, particularly in the area of status conditions as they affect hardware and software. The specification of the standard interface provides the rules for interconnecting Spectra 70 processors and control electronics. It has been stated that the standard interface provides the necessary conditions for the interconnection while the terminal units provide the sufficient conditions. With these qualifications in mind, a simplified description of interface operations on a hypothetical control electronics unit will be undertaken to demonstrate the use of the interface. For this purpose, a control electronics will be treated as a sequential network as shown in Fig. 2.

A control electronics is viewed as an entity which includes the device interface as internal signals. A similar view is taken of the operation of a processor channel. In Fig. 2, only those lines pertinent to the description command initiation, data transfer, end reporting, and interrupt processing are shown.

The state of a control electronics is defined to be a function of four output signals: Service Request, End, Ready, and Interrupt. The functions of these lines are:

Service Request: The true state of this signal indicates that a control electronics is requesting a channel service for a byte transfer.

End: The true state of this signal indicates that a control electronics is requesting a channel service to report status at the end of an input/output operation. This signal is sent in conjunction with the Service Request signal.

Ready: The true state of this signal indicates that a control electronics is ready to report status for a command initiation or interrupt processing.

Interrupt: The true state of this signal indicates that a control electronics is requesting a program service for a termination interrupt, program controlled interrupt, or manual request interrupt.

The interface operations of command-initiation or interrupt-processing and data-transfer or end-reporting can occur simultaneously. In the following simplified descriptions, these operations will be treated individually.

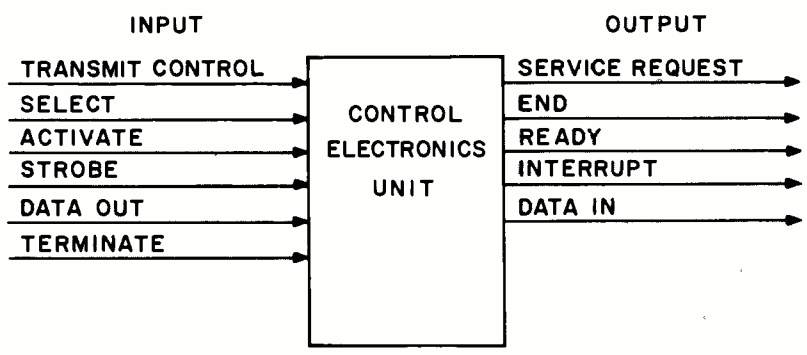
The status of a control electronics is designated according to the following table:

Service Request	*End*	*Ready*	*Interrupt*	*State Designation*
0	0	0	0	S_0 *
0	0	0	1	S_1
0	0	1	0	S_2
1	0	0	0	S_8
1	1	0	0	S_{12}

* This state implies that a control electronics or device is operable and available (not busy).

The inputs to a control electronics, generated by a processor channel as a result of an instruction or in response to the preceding signals, are designated according to the following table:

Fig. 2—Control electronics as a sequential network.



Transmit Control	*Select*	*Activate*	*Strobe*	*Designation*
0	0	0	0	I_0
*0	0	1	1	I_3
0	1	0	0	I_4
1	0	0	0	I_8
*1	0	0	1	I_9
*1	1	0	1	I_{13}

* Only steady-state valid signal combinations are designated. Transitionary or invalid sequences are not considered to simplify the description of operations. For example, there is no specification of the maximum time displacement of the activate and strobe signals, but in practice those signals must be transmitted during input/output servicing. For this discussion, this combination is considered to occur simultaneously.

Fig. 3 is a state-graph description of interface operations. Operations are shown for a hypothetical control electronics on which only one device is executing a read operation. Operations are shown for both selector and multiplexer channels.

Command Initiation

Command initiation is a three-step process consisting of device selection, status testing (SDB), and command issuance. A device address is broadcast to all control electronics attached to a channel. The control electronics, which recognizes the address, responds with a Ready signal as shown in the transition from state S_0 to S_2. (If no control electronics responds within a prescribed time interval, the addressed device is considered to be inoperative by the processor.) Following Ready response, the status (SDB) of the control electronics or device is tested after which the command is issued (strobed) by the channel, and the control electronics state changes from S_2 to S_8. The notation DOUT $\neq$ WRU refers to a Set-2 command which will be discussed under interrupt processing.

Note that no state transition occurs until a strobe signal is issued by the processor. The gating of the SDB (or device address in data transfer or end reporting) is a passive operation controlled by the Transmit Control and Select processor signals.

Data Transfer

In S_8, a control electronics is requesting a byte transfer by means of the service request signal. On a multiplexer channel, as shown by the dotted lines in Fig. 3, the device address is transmitted to the processor before the data byte. Again, no state change occurs until the processor issues a strobe signal which indicates that the byte has been accepted by the processor. A control electronics can thereafter remain in S_8 or go to S_{12} for termination. The case shown is an illustration of control electronics initiated termination. A processor can also initiate termination by transmitting a terminate signal when strobing the last byte to be transferred. In both cases, the control electronics makes a transition from state S_8 to S_{12}.

End Reporting

In state S_{12} the control electronics is reporting the end of the read operation by Service Request and End Signals. As in the case of data transfer, the processor controls the information on the Data-In lines. On a multiplexer channel, the device address is transmitted before the Standard Device Byte. In response to the Service Request and End signals, a processor can issue commands that

1) Reset the control electronics to return to state S_0,
2) Return to S_8 and execute a chained command, or
3) Make the interrupt line and 2^6 bit of the SDB true for later processing. The last case is considered in the transition from state S_{12} to state S_1.

Interrupt Processing

When processing interrupts a set 2 command, designated *Who Are You* (WRU), is broadcast to all control electronics on a channel. Control electronics, with an interrupt pending, gate the address of the interrupting device to Data-In lines after which an interface is strobed by the processor and the control electronics changes from state S_1 to a state designated in Fig. 3 as S_0*. This state is effectively identical to state S_1 except that the interrupt line is reset. The function of that line is assumed by the 2^6 bit of the SDB. This has been implemented for hardware compatibility.

Following WRU and Strobe, a control electronics responds with Ready after which the standard device byte is stored for program interpretation. The 'Send Status command and Strobe cause the control electronics to reset the 2^6 bit of the SDB and to return to state S_0.

ACKNOWLEDGEMENT

The success of the standard interface program is due to the efforts of many who cannot all be cited here. But acknowledgement is due particularly to Messrs. J. Schell and T. Floyd of EDP Palm Beach Engineering for their major contributions to the concept and its detailed implementation.

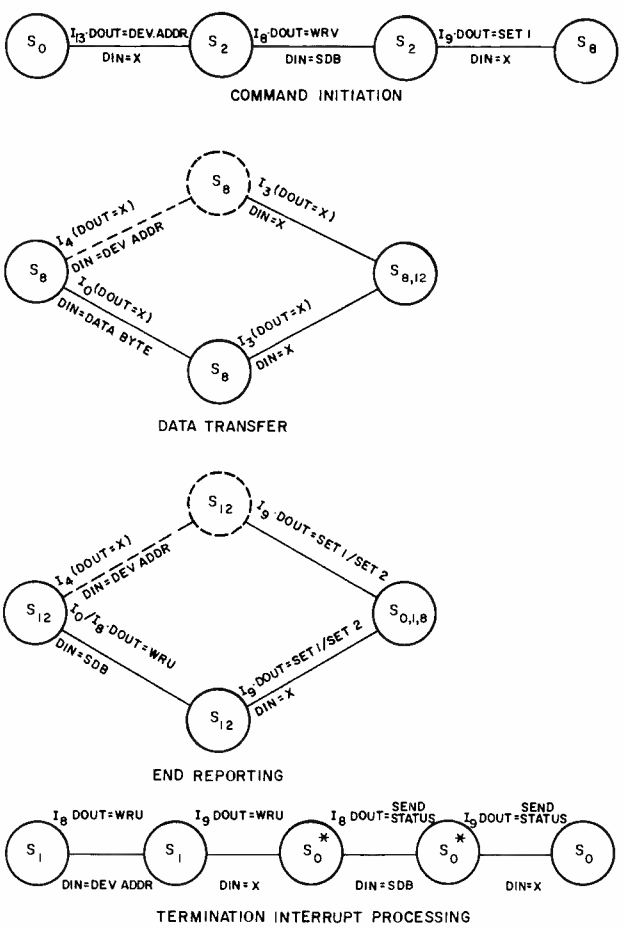


Fig. 3—Standard interface operations.

EMULATION TECHNIQUES ON THE RCA SPECTRA SYSTEMS

The very rapid advances in computer technology have made it desirable for users to update their existing data processing equipment with third-generation hardware. To accomplish this transition, a user must consider the cost of converting his programs—a major project for which the typical user seldom has a sufficient programming staff. In the past, simulation software has been supplied by the manufacturers to facilitate the program conversion effort; however, this technique is very inefficient. Simulation in general is economically practical only for infrequently run programs, and the more frequently run programs must immediately be recoded before the old system can be replaced. Emulation is a technique involving both hardware and software which permits existing programs written for the old system to be efficiently run directly on the new system. The hardware cost is small and the performance is at least an order of magnitude better than simulation.

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T. A. FRANKS received the BEE from Rensselaer Polytechnic Institute in 1956 and the MS from Stanford University on a fellowship program in 1957. Since joining RCA in 1956, he has taken part in the development of solid-state memory circuits; worked on various drum buffer memories; participated in the systems architecture, logic design, and application of several advanced real-time processing system; and was a project engineer on a BMEWS computer installation. Upon joining EDP in 1962, he was the engineering project leader of the RCA 3301 and Spectra 70/45-55 systems; then was manager of emulator microprogramming activities; and is currently manager, computer projects. Mr. Franks is a licensed professional in the state of New Jersey and a member of the IEEE, Tau Beta Pi, Sigma Xi and Eta Kappa Nu.

C. S. WARREN received the BSEE in 1952 from Virginia Polytechnic Institute. He joined RCA in 1952 as an engineer on the specialized training program, following which he spent seven years in advanced development working on magnetic memory devices and transistor circuit design and development. Also during this period, he was responsible for the design of several memory systems used in BMEWS. In 1959, Mr. Warren was transferred to the Van Nuys Division of RCA where he was made leader of a logic design group and was responsible for the design of a small real-time computer, initially used in instrumentation radars. In 1963, Mr. Warren transferred to his current position as Leader, Advanced Systems, in EDP Systems Engineering. In his current capacity, he has played a major role in the architecture and design of the Spectra 70 Emulators. Mr. Warren is a member of the IEEE, Eta Kappa Nu, and author of several papers and patents.

COMPUTER TECHNOLOGY has continued to experience rapid advances in machine performance, range of application, and varieties of peripheral devices. Accordingly, data processing users have, at various times, had to consider the economics of trading in outmoded equipment and replacing with the latest units. As users have become more sophisticated in the application of computers, a substantial investment exists in their library of programs and data files. The considerations of how to make a smooth transition from one system to another with minimum loss of investment has typically been traumatic.

There are currently several techniques that aid in this conversion, but none is a panacea:

Higher Level Languages: Any portion of the work that has been programmed in a machine-independent language can be run on a new computer, if a compiler is provided for that language. However, compilers have not been truly machine independent and often the language compilers are not available with delivery of the equipment. Further difficulties arise when machine language coded subroutines are mixed with the higher level language statements to patch in a special feature or fix a bug.

Translation: Each instruction or group of instructions can be automatically changed from the machine language of the old computer to that of the new. This translation is performed from either source

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language or object program decks. Translators process the instructions before execution time; hence, it is difficult to translate an instruction that will be modified or replaced by the program itself before its actual execution. Translation is generally less successful between two computers that differ widely in architecture.

Simulation: Simulation differs from translation in that each instruction is interpreted in sequence at execution time. An image of the entire state of the computer being simulated (memory contents, registers, indicators, etc.) is maintained on a bit-for-bit or character-for-character basis in the simulating computer. Strict adherence to this rule of interpretation at execution time removes the conceptual problems present with translation. Because of their simplicity, interpretive routine simulators have been quite successful. Unlike a translator, a simulator must interpret an instruction each time it is executed rather than just once. Thus, there is a large performance degradation due to the interpretive overhead. Further limitations are often required on the fidelity of the interpretive routines to keep the simulation program size within reason. Most simulator programs have not been fast enough to be of significant value in the conversion efforts.

Reprogram: As a last resort, a problem may be reprogrammed in the new computer language. This reprogramming is costly, time consuming, and is just a brute force solution to the conversion problem. Eventually, all programs of value will be reprogrammed. However, reprogramming and debugging to this extent during a tolerably short transition interval is usually not feasible.

Emulation: An emulator is a package supplied by the computer manufacturer that includes special hardware and a complementary set of software. The package runs in the manner of an interpretive routine simulator program but is approximately an order of magnitude faster. The combination of emulator and the new computer in effect create an extended computer which, to the user, is the computer for which the original object code was written. The advantages of emulation are simplicity of operation and system thruput performance. Thruput can typically range from equal to four times better than the original system depending on the application.

EMULATION

In the Spectra computer series, emulation is used to perform the interpretive processing on all non input/output instructions by hardware microprogram. Interpretive processing of input/output instructions is handled by the complementary set of software. Microprogram computers generally have two sequence counters, one for the macro-instruction sequence, with which the machine language programmer is familiar, and one for a micro-instruction sequence, which interprets and executes the macro-instruction. These micro-instruction sequence steps are called elementary operations (EO's) and are pre-wired in a read-only memory.

The economic feasibility of read-only memories has allowed the Spectra 70/35 and 70/45 computers to employ these techniques for system control. Additional read-only memories may be optional add-ons to the system; each one containing the micro-instruction steps corresponding to a particular order code. Several earlier machines of the microprogram type have been described in the literature and include the TRW-133[1], Packard Bell 440[2] and Collins 8401[3]. The Spectra 70/45 and 70/35 have also been described.[4,5]

A microprogram simulation is invariably more efficient than a macroprogram simulation, since the interpretation is being executed at a point of least difference between the computers. On a macroprogram level, computers have widely different structures: instruction formats, fixed or variable data fields, binary or decimal character codes, etc. On a microprogram level, the ability to process bit-by-bit or character-for-character allows the more complex macro-level operations to be implemented by relatively straightforward sequences of elementary-bit or character manipulations.

To take a different view of the efficiency of micro versus macroprogramming, a given data processing problem coded in machine language for several computers causes a wide variation in the total number of memory cycles. The most efficient routine is a result of the computer with the best instruction repertoire for the original problem. This has been evident in the performance of software simulators. Emulators or microprogrammed simulators allow routines which, in terms of memory cycles, show little difference from the original computer's operation. Interpretive routine simulation by hardware microprogram allows the process to be done at the point of minimum difference.

The complementary set of software in emulation has a large part to play. In several cases, it becomes uneconomical to do a function by microprogram. Software control of input/output sequences allows a flexible approach to performance enhancements such as buffering, look-ahead, multiprogramming, and additions of facilities for handling peripheral devices not included in the initial microprogram release. Execution of appropriate error-recovery procedures is a problem best handled by software. Also, to the operator, the systems are totally dissimilar; the software provides an interpretive console to allow execution of operating procedures in the most convenient manner.

IMPLEMENTATION

Emulation is provided on the 70/35 and 70/45 by the inclusion of additional read-only memory banks, special software package, and some minor hardware modifications to the respective processors. The added read-only memory is used in two ways: interpret the instruction repertoire of the machine being emulated and to provide some special Spectra 70 instructions to assist the software portion of the emulator. The wired program within the read-only memory is referred to as the Emulator Microprogram (EMP).

The software portion of the emulator is called the emulator control program (ECP) and consists of two components: the emulator monitor system (EMS) and the emulator interface program (EIP). The EMS is a special operating system designed to run any of the Spectra 70 emulator features. The EIP is a special software package designed for each emulator to interface the EMP with the EMS. Both the EIP and EMS are programs written in Spectra 70 code. The primary responsibilities of the EIP are:

1) Translate the I/O instruction of the machine being emulated to equivalent Spectra 70 operations;
2) Perform any peculiar code translations;
3) Interpret I/O termination conditions and set any necessary emulated indicators; and
4) Interpret and execute all emulated console functions relating to errors, normal operation intervention, initialization, etc.

The hardware modifications consist of the control logic necessary for selecting and addressing the added read-only memory banks, and some added functions, to the microprogrammed structure of the machine to facilitate or enhance the emulation capability. In the implementation discussion which follows, it is assumed that the reader is generally familiar with normal Spectra operations and technology.[5,6]

The operation of the emulator is controlled by two control bits in the Interrupt-Status Register. The first bit is the *Emulator ON (EON)* and the second bit is the *Bank 3 (BK3)* control; the *BK3* control selects one of two possible emulators. The 70/45 allows up to two different emulators to be added to the system; the 70/35 allows only one. With the *Emulator ON (EON-1)* the four normal program states of the Spectra 70 processor take on the following functions:

Program State 1 fetches and executes all instructions out of the added read-only memory (bank 2 or 3 depending on the state of the *BK3* emulator control).
Program States 2, 3 and 4 fetch and execute all Spectra instructions out of the original Spectra read-only memory bank and allow a special set of EIP instructions unique to the emulator.

By designing the program states to operate in this manner, the emulator can

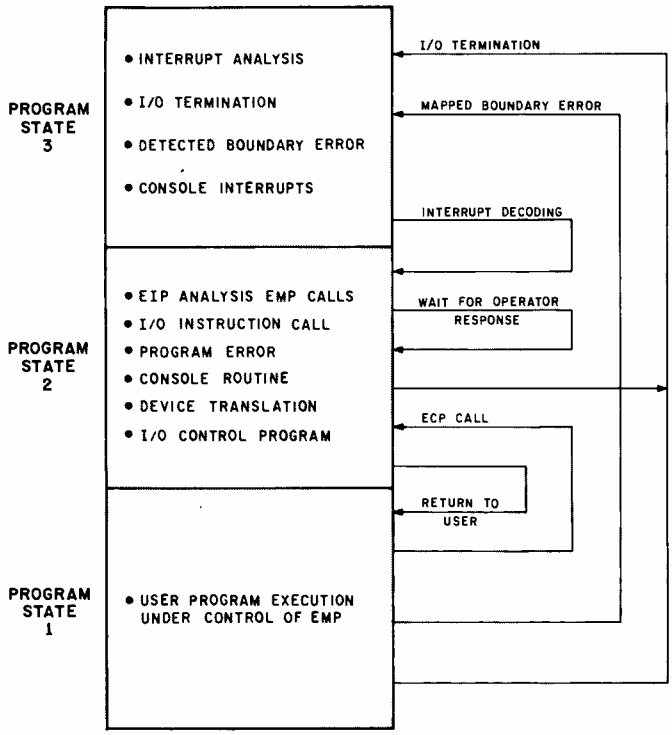

Fig. 1—Utilization of Spectra 70 program states by the emulator.

incorporate normal Spectra 70 coding for the ECP which must be executed in program states 2 and 3 and execution of the user's program being emulated in program state 1.

Fig. 1 illustrates how the program states of the Spectra 70 are used by the emulator. Program state 1 is the state in which the user program is executed under control of the emulator microprogram (EMP). State 3 is used by the EMS to analyze all program interrupts. All interrupts. once analyzed, are turned over to either the emulator monitor system (EMS) or emulator interface program (EIP) in program state 2 for proper handling of the interrupt. In program state 2, the bulk of the EIP and EMS are executed. An EIP routine analyzes all I/O instructions encountered by the EMP and prepares them for execution. Program errors encountered in the user's program are handled in program state 2; the console routine for operator communications is contained in program state 2 and the I/O control program which is responsible for issuing all I/O commands are also contained in program state 2.

During execution of a user program, the EMP will turn control over to the ECP for any of the following reasons:

1) An I/O instruction is staticized and decoded;
2) A condition is detected that would result in a machine halt or malfunction in the emulated machine; or
3) The instruction fetch or data fetch/store was outside permitted memory bounds.

For the first two conditions. the EMP will turn control over to the EIP in program state 2 directly. Communication with the EIP portion of the emulator is through a communication constant which is used by the software to determine the reason for the EIP call. In the case of an I/O instruction, the EIP will return control back to the EMP in program state 1 as soon as the I/O instruction has been executed and/or the device started. In the case of error conditions, the ECP will generally be required to give a printout on the console and wait for a response by the operator. Under any condition, the ECP will return control to the EMP in program state 1 only when the emulated program is able to continue its operation. The third condition is an automatic interrupt to program state 3 where it is handled like all other interrupts by the ECP. Special hardware has been added to the processor to facilitate the detection of the memory boundary used by the emulated program. This is a special addressing error condition detected only when the emulator operation is in effect.

MAPPING

The operation of the emulator depends on an instruction-for-instruction interpretation of the program being emulated. To do this, the characteristics of the native machine must be mapped one-for-one into the Spectra processor. To date. all of the machines being emulated on the Spectra equipment have been character oriented and, with the exception of the RCA 501, are decimally addressed machines. Spectra is a combination word and character machine with binary addressing and 8-bit characters. These characters of the Spectra and the machines to be emulated permitted a rather straightforward mapping of memory on a character-for-character basis. A contiguous portion of the Spectra main memory represents the main memory of the system being emulated. This portion of the Spectra memory is bounded on both sides by a special character which is used by the EMP to detect an operation which crosses the boundary. The ECP or software portion of the emulator resides outside these boundaries. To permit multiprogramming and facilitate two emulators in the system. the mapped memory is floated.

In addition to main memory, all registers and indicators used or referenced by the instruction repertoire of the native machine must be mapped or allocated equivalent storage in the Spectra 70 system. In all the emulators designed to date, the Spectra floating-point registers were assigned the function of representing the native machine registers and indicators. These were chosen for two primary reasons:

1) The floating point registers were not needed by the software portion of the emulator, and therefore, would not require storing and restoration every time the program state is changed;
2) The software system operating in program states 2 and 3 can access the floating-point registers as readily as the EMP. This later was a key consideration since both the software and, particularly, microprograms require frequent access to the mapped registers.

The ready availability of these registers is a major factor in the performance of the emulator.

In addition to the mapping of registers and memory. the emulator requires storage for conversion and translation tables. Address conversion and code translation tables are required to enhance the performance of the emulator. In all the Spectra emulators to date, the general registers for program state 1 were allocated to address conversion tables, since these registers are most readily accessible by the EMP, and address constants are the most frequently accessed arguments. Other tables needed by the microprogram utilize a special portion of main memory which is not accessible to the programmer. Normally. this portion is allocated to the multiplexer subchannel register. This restricted the number of subchannel registers that the emulator system could use to 64. However, this has not affected any system configurations to date since 64 still provides adequate room for expansion. This approach has the advantage that more of the main memory space is conserved for the programmer.

EMULATOR MICROPROGRAM

The emulator microprogram (EMP) consists of the following parts:

1) Instruction fetch and decode;

2) Individual execution algorithms for emulated instructions; and
3) Decode and execution of all special Spectra instructions.

The instruction fetch and decode portion of the emulator microprogram is entered automatically whenever an instruction in program state 1 is completed or whenever control is returned to program state 1. This portion of the EMP is common to the interpretation or execution of all emulated instructions. It fetches from mapped memory the next instruction, performs any necessary address conversions, updates all simulated machine registers, decodes the operations, and enters the execute portion of the instruction.

The instructions consist of individual microprogram routines. In the case of non-I/O instructions, these routines perform the operation and leave all simulated registers, indicators, and memory locations exactly as in the native machine. In the case of an I/O instruction, the EMP decodes the particular operation into an ECP communication constant which is utilized to select an appropriate EIP subroutine. Control is then switched by the EMP to program state 2 so that this selected EIP subroutine may proceed with the translation into an equivalent Spectra operation. The EIP will return control to the EMP only after the I/O operation is completed or the device is initiated and I/O simultaneity is specified and permitted.

The third portion of the EMP consists of the microprogramming routines for special operations to assist the EIP. For example the 301 emulator uses a move and translate instruction to move data of specified length from one memory location to another, translating the codes from one representation to another via a specified conversion table. In the case of this special operation, the EIP can translate I/O data from 301 codes to Spectra codes, thus permitting standard Spectra devices to be substituted for 301 devices. The special operations are in the format of Spectra 70 instructions and can only be executed when in States 2, 3 or 4 and the *EON* control is set to one. If the emulator is not *ON* or the emulator bank specified is not installed, these special operation codes (op-codes) will cause a normal illegal op-code error to occur. The special op-codes are fetched and staticized as a normal Spectra 70 instruction using the Spectra read-only memory bank. In the Spectra 70 staticizing microgram, a group of unused op-codes are assigned to these special operations and are designed to automatically branch to a fixed read-only memory location in the emulator bank. If the emulator is not installed or the emulator control is not *ON*, this branch will result in an op-code error. At this fixed read-only memory location, the EMP must decode all the special operations for this particular emulator. Once decoded, the EMP completes the execution of the special operation. This technique of expanding the Spectra repertoire permits each emulator to have its unique set of special instructions.

EMULATOR SYSTEM PERFORMANCE

In an emulator system design, performance is predominantly determined by 1) similarity of the processor being emulated and the emulating processor and 2) degree of fidelity desired in the processing functions. These factors can be separated into two categories: those related to the internal instructions and those related to the input-output functions. A partial list of items found to be of principal significance is tabulated below:

Internal Instructions

1) Conversion of decimal memory addresses to a binary equivalent;
2) Differences in character codes between the system being emulated and Spectra representations.

Input-Output Functions

3) Per-character processes required on data exchanges with peripheral devices;
4) Emulator software overhead required for interpretative translation of input/output requirements; and
5) Peripheral equipment speed differences.

Memory Address Conversion

All Spectra data processors employ straight binary-coded address references. The 70/45, for example, allows binary addresses ranging to 18 bits. However, the 1410 system employs a five-digit decimal field. The 1401 and 301 systems employ six-bit characters with a combination of decimal digits and zone bit combinations within each character of the address field to designate a memory reference. A conversion must thus be performed for each operand address fetched from the native address format to an equivalent Spectra binary reference. Since the base of mapped memory or equivalent location of the emulated system's zero address is relocated to some other non-zero value, this offset must be incorporated in the address conversion algorithm. These conversions have generally been implemented through series of decimal-to-binary table lookups so as to reduce the execution time. To further reduce the extra addition cycle required for the mapped memory base offset, one of the decimal-to-binary tables is offset an equivalent amount by the emulation software at initial load time. Thus, the decimal-to-binary weight and base offset are available in one table lookup operation.

Character codes

Character-code representations in the system to be emulated and Spectra equivalents are generally not the same. Operations such as comparisons and addition/subtractions therefore follow different rules. For example, the six-bit binary-coded decimal (BCD) representations used in the 1410 and 1401 systems differ from Spectra formats in two ways:

1) The collating sequence used in compare operations does not correspond to the actual binary weights; and
2) The binary representation of the decimal digit zero is 1010, not 0000 as in Spectra.

To eliminate special translations for every compare or arithmetic operation, the 1400 BCD characters are represented internally in extended BCD interchange code (EBCDIC) whose binary codes correct the above peculiarities. Since EBCDIC is a standard for Spectra equipment, compatible translation facilities are included in all input/output devices to convert card, tape, etc. codes into EBCDIC as the data is entering or leaving the processor. Thus, the codes are automatically translated as data is read or written and internal emulator processing of the characters is compatible with the Spectra hardware arithmetic unit.

Some internal operations still require conversion of the EBCDIC codes into BCD, and vice versa. Examples are the move-digit/zone or branch-on-bit-equal instructions. However, the additional penalty to these instructions is small compared to the gains in other algorithms.

Similar problems, although not as severe, occur with 301 and 501 codes. Here the difficulty is concatenation of a six-bit character into an eight-bit byte. Special provisions must be made to insure proper propagation of carries in arithmetic operations.

Per-Character I/O Processes

Input/output operations in the Spectra system are count controlled. For instance, a tape write command employs a starting memory address and a specific number of bytes to be written out. Input/output instructions available in the 1410, 1401, and 501 systems, however, are symbol controlled. That is, the length of a field to be written out (or read in) is determined by the location of a special terminating symbol in memory. Thus, before an emulated I/O instruction can be converted into an equivalent Spectra command, the field must be scanned to determine a byte count. This scanning operation adds to the time required to execute an I/O instruction and constitutes additional overhead. The time involved is determined on a per-character basis and if performed with conventional

instructions, would range from approximately 10 to 25 μs, depending on application. However, by utilizing special microprogrammed routines designed for these processes, the per-character times range from 1.2 to 5.5 μs. Through microprogramming techniques, almost an order of magnitude improvement was possible. When compared with the data rate from a 60KB tape station, this processing typically represents an increase of only 15% in data transfer time, which is exclusive of start/stop delays. Thus, the apparent increase in total type time is not excessive.

Emulation Software Overhead

The complimentary software package employed in an emulator (called ECP) provides the translation linkage to execute I/O instructions. To perform this function, a variety of actions are required 1) to initiate the equivalent Spectra device operation and 2) to translate termination conditions into corresponding mapped emulation indicators. Where appropriate, routines have been included to enhance system performance. These include such facilities as:

1) Advanced card reading into a buffer area;
2) Advanced print release by moving data to be printed into a buffer area;
3) Error recovery through retries; and
4) Provision for multiprogramming two emulation operations.

Typically, execution of the ECP routines adds 0.5 to 1.5 ms to the execution time of an I/O operation (exclusive of any per-character processing). This overhead can be minimized by overlapping the processing with input/output operations and using the above enhancements.

Peripheral Speed Differences

Device speeds in I/O-bound programs have as direct a bearing on overall thruput as execution time of internal instructions in compute-bound programs. By selecting peripheral devices which are faster than the corresponding units in the system being emulated, substantial improvements in thruput can be achieved. The start/stop characteristics of I/O devices can be as significant in system performance as the data rates; particularly where short records are involved. It is difficult to predict I/O performance or system thruput due to the complex inter-relationship between the device time, ECP overhead, and internal instruction mix being executed through microprograms.

Performance Measurements

The level of emulator performance is usually measured by total program thruput. This performance is determined by inter-relationships between the following:

1) Execution time of the microprogrammed internal (non-I/O) instructions;
2) I/O device character rates and start/stop times;
3) ECP overhead time required to translate I/O requirements into Spectra equivalents; and
4) The timing distribution of the above three items in actual operations.

The "average" performance ratios of native instruction times to emulated instruction times are listed below:

Parameter	*1410*	*1401*	*301*	*501*
Memory Speed Native System (μs)	4.5	11.5	7.0	15.0
Performance Ratios:				
Native time of 70/45	2.3	4.1	2.6	2.4
Native time of 70/35	*	3.8	1.6	*

* 1410 and 501 emulators are not available for the 70/35 system.

These figures were derived from a weighted mix of typical internal instructions, and hence are considered "average." The ratios vary from 1.6 to 4.1 and in no case is emulation slower than the original system; these figures illustrate the efficiency of emulation at the microprogrammed level versus simulation at the instruction level. Typical performance of simulation programs would be approximately an order of magnitude slower.

If programs only consisted of internal instructions and essentially no I/O activity, then the above ratios would properly represent thruput. However, most commercial data processing activities are quite dependent on extensive I/O activity. Thus, performance of the peripheral devices is a very significant factor in determining thruput. Peripheral device performance between the native system and emulating system may generally be compared on two accounts: per-character data rates and start/stop times. Since I/O activity can be (and usually is) overlapped with internal processing functions, an emulating system with devices twice as fast as the native configuration and a minimum of non-overlapped processing will not have an equivalent increase in thruput.

Any ECP overhead time required to translate I/O requirements into Spectra equivalents adds to the execution times of the I/O instructions. ECP device initiation/termination sequences are by their very nature non-overlapped with any emulation processing time. Device initiation or termination times may only be overlapped with I/O activity on another I/O channel if such activity is required by the program being emulated. To this extent, ECP overhead does not quite add directly to total program execution time. However, the effects of ECP overhead are most noticeable in I/O bound programs handling short records. Per-character I/O processing is an ECP function and since it occurs at initiation or termination time, can be considered as an extension of the ECP overhead factors.

The most complex factor affecting performance is the timing distribution of internal processing, I/O activity, and ECP overhead functions. These interrelationships can cause idle processor or I/O time at points in the emulated program where none existed in the native system. Evaluation of this factor in the design of emulators was only attempted through timing simulation runs. The effects and interrelationships were too complex to predict by a simple set of ground rules. Actual program running times have been measured on the 301 and 1410 emulators for the 70/45. The thruput ratios range from 1.30 to 2.95 on the 301 and from 1.89 to 2.66 on the 1410. The variability of thruput reflects the interplay between the four performance factors described above.

CONCLUSIONS

The emulators, as described in the article, are currently operational. Field experience has proven them to be a valuable program conversion technique. It has been demonstrated that a user program can be run directly on the emulator without reprogramming and with an actual increase in performance. Emulation has been made economically feasible, primarily because of the use of read-only memory in the design of the computer control and the improved cost-performance ratio of third generation hardware.

Emulation, on the other hand, has not solved the reprogramming problem faced by a user who wants to take full advantage of third generation hardware. It does, however, permit him to spread his reprogramming investment over a longer period of time. Although the primary purpose of emulation is to ease the user's burden of reprogramming, it has, in certain instances, actually reduced the total rental cost.

ACKNOWLEDGMENTS

The emulator design has been the joint effort of many groups and individuals within the EDP organization. Special mention is made of Engineers and Programmers within the Emulation Design group and the designers of the Spectra 70/35 and 70/45 systems, without whose cooperation this program would not have been possible.

REFERENCES

1. McGee, "The TRW-133 Computer," *Datamation*, Vol. 10, No. 2, p. 27,
2. Boutwell, "The PB-440 Computer," *Datamation*, Vol. 10, No. 2, p. 30,
3. Beck and Keeler, "The C-8401 Data Processor," *Datamation*, Vol. 10, No. 2, p. 35,
4. Cambell and Neilson, "Microprogramming the Spectra 70/35: *Datamation*, Vol. 12, No. 9, p. 64,
5. Yen, "Internal Logic Structure of the 70/45," RCA reprints PE-257, PE-258.
6. Form 70-35-601, *70/35—70/45—70/55 Processors Reference Manual*, RCA, Electronic Data Processing Div., Cherry Hill, N.J.

A SIMPLE DISPLAY FOR CHARACTERS AND GRAPHICS

The MODEL T display system accepts coded digital data from a voice-grade telephone line and displays graphical and alphanumeric information on a direct-view storage tube. No local refresh is required to maintain the display. The MODEL T operates in an incremental vector mode, each vector being described by 7 bits. A vector calls for the display to move the beam from its present location along one of eight directions, a distance of one of eight permissible lengths, with the beam either on or off. A vector is drawn as a series of dots which are written at a uniform rate. A minimum command structure is provided. The MODEL T draws 240 vectors/second (over a 2400-baud telephone link) and can thus display rather complicated patterns in a matter of seconds. Alphanumeric symbols can be formed from a sequence of vectors under software control. Even so, the MODEL T can write text substantially faster than a teletypewriter. The essential virtue of the MODEL T is the combined graphic and alphanumeric capability in an economic design.

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RECENTLY interest has been expressed in the problem of making it easier for the computer user to interact with the machine while his job is being run. Time-shared computers offer this capability by giving each of a number of users the illusion that he is the sole user of the machine and by permitting him (via a remote console) to direct or modify the process of computation while on-line. Man-machine interaction is easier if the machine can make pictures.

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An experimental prototype for this purpose was designed with emphasis on simplicity. The prototype, called MODEL T, is a low cost soft-copy display with alphanumeric and graphic capability. It is primarily intended for remote applications where a limited bandwidth connection (such as a voice-grade telephone line) links the display to the computer.

CIRCUIT DESCRIPTION

The MODEL T contains the necessary electronics to accept code groups (7 bits + parity) from a remote source, to interpret them as vectors or commands, and to generate deflection signals for the display device. This particular code was chosen primarily because it is identical with that used to communicate with other terminal devices such as teletype printers. Thus the MODEL T can communicate with most newer computers with little or no hardware modifications.

Fig. 1 shows the code assignment chosen for the MODEL T. The 7 information bits are divided into three categories: bits B1, B2, B3 specify one of 8 directions; bit B4 determines whether the beam is to be unblanked; and bits B5, B6, B7 indicate one of 8 lengths. Thus a vector is specified as a prescribed length in a given direction with the beam unblanked (or blanked). The permissible directions are the 8 major compass points, and the 8 lengths are 0, 1, 2, 4, 8, 16, 32, and 64 units. Vector motion is incremental, each code group being interpreted as a beam motion from its last point. Constant writing speed is employed to insure uniform brightness on the display. The special situation of a vector of zero length with the beam off is used for machine commands as will be explained later.

The operation of the MODEL T system is outlined in the system flow chart (Fig. 2). In the configuration most often used, the input is a serial signal on one wire, such as a telephone modem might provide. The system may be adapted to other inputs: for example, seven parallel contact closures to ground

Bits	B_1	B_2	B_3 Direction or Instruction	B_4 Unblank	B_5	B_6	B_7 Length	Function
INSTRUCTIONS	0	0	0	0	0	0	0	Null-Idle
	1	0	1	0	0	0	0	Null-Idle
	1	1	0	0	0	0	0	End of Message/ Lock System
	1	1	1	0	0	0	0	Unlock System
	1	0	0	0	0	0	0	Reset Position
	0	1	0	0	0	0	0	Erase Upper Half Screen
	0	0	1	0	0	0	0	Erase Lower Half Screen
	0	1	1	0	0	0	0	Erase Both Halves
					0	0	0	0
					0	0	1	1
					0	1	0	2
					0	1	1	4
					1	0	0	8
					1	0	1	16
					1	1	0	32
					1	1	1	64
VECTORS				1				Unblank beam before moving and after each Δ position
	0	0	0					Right
	1	0	0					Right and Up
	0	1	0					Up
	1	1	0					Up and Left
	0	0	1					Left
	1	0	1					Left and Down
	0	1	1					Down
	1	1	1					Down and Right

Fig. 1—MODEL T code structure

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CHARLES M. WINE received the BEE from the City College of New York in 1959 and then joined the technical staff of RCA Laboratories. There he has been involved in psycho-acoustic research, investigation of the uses of tunnel diodes in home instruments, ultra-high speed computer circuit research, and cryogenic computer devices and memories. More recently he has been working in the areas of read-only memories and advanced computer input-output equipment. Mr. Wine is a member of Eta Kappa Nu, Tau Beta Pi, ACM, and AAAS.

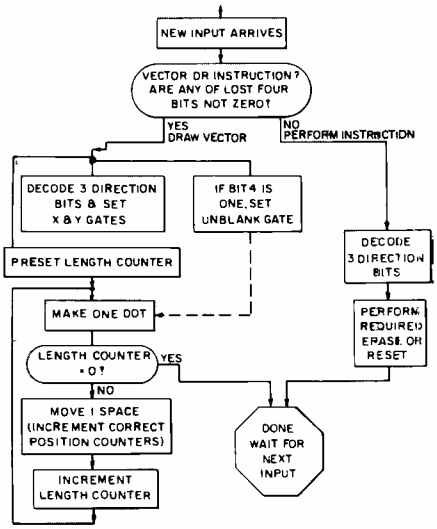


Fig. 2—MODEL T system flow chart

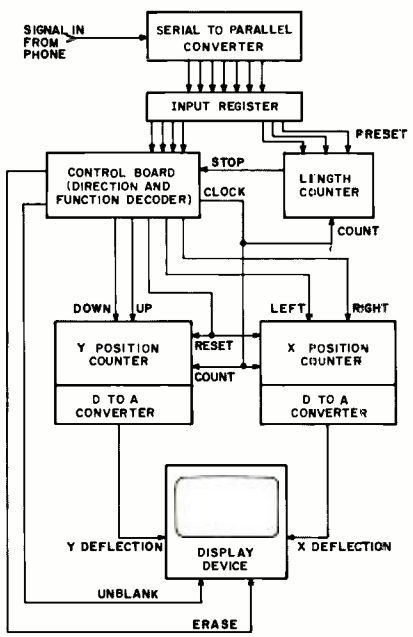
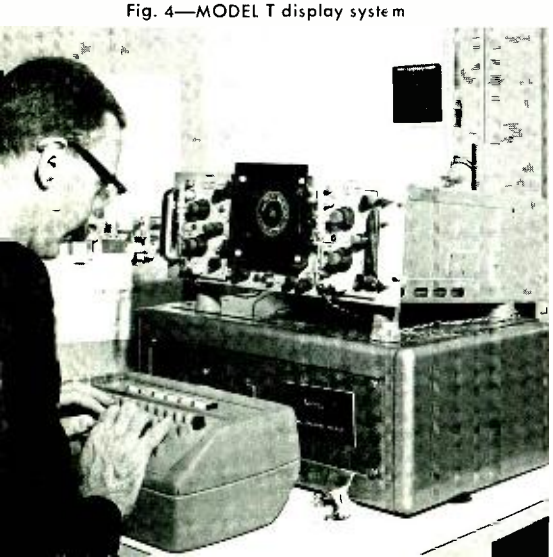


Fig. 3—MODEL T display system block diagram

Fig. 4—MODEL T display system



from a tape reader can be provided by simply replacing one input interface board. The input is checked for parity. Under operator control, a parity error may be ignored or may lock the display and send an interrupt back to the computer. When an input is accepted, it is transferred into a seven-bit parallel register which holds it until the next input comes. If bit 4 (the unblank bit) or any of the length bits (bits 5, 6, and 7) are *one*, a status flip-flop is set to begin the drawing of a vector. The first three bits (the direction bits) are decoded to provide a "move right" or a "move left" signal and a "move up" or "move down" signal. The length bits are used to preset a 7-bit binary counter (the length counter) to 128 minus the number of dots in the vector to be drawn. Under control of a free-running clock, the system proceeds to produce an unblank pulse (if bit 4 is a *one*), increment the X and/or Y (position) counters, and increment the length counter. After each unblank pulse, but before each move pulse, the state of the length counter is checked. When it is "all zeros", the status flip-flop is reset, returning the system to the quiescent state. If the input code calls for zero length, one unblank pulse is produced, plotting one point on the screen. If, for example, the input calls for a vector 16 units long, 17 dots are put on the screen, the first at the original location and the last 16 units away in the specified direction. The beam position is stored in a pair of 9-bit counters, one for X and one for Y. These counters count the clock pulses, incrementing when the beam is to move up and/or right, and decrementing when the beam is to move down and/or left. The outputs from the position counters are combined in a binary-ladder digital-to-analog conversion network which produces deflection voltages for X and Y.

An input code that called for the system to draw vectors of zero length with the beam off in any of the eight directions would be wasted if treated as a normal code: it would do nothing. These codes, distinguished by the last four bits being zero, are used as instructions. When an instruction is received, the three direction bits are decoded to provide output pulses to erase the screen or to reset the position counters to all zeros (the lower left corner).

The basic circuit building blocks used were the Signetics SP 600A series, dual in-line integrated circuits. These were selected on a basis of availability and cost; other circuits could be substituted. The system was partitioned into 6 printed circuit boards, each containing between 10 and 23 integrated circuits. Fig. 3 is the system block diagram. A photograph of the MODEL T is shown in Fig. 4.

OPERATIONAL CHARACTERISTICS

Display

The MODEL T writes on a field of 512x 512 addressable points. Inherently, the display has no flicker. Fig. 5 shows photographs of typical display images. Approximately 5000 vectors can be comfortably displayed at once. An estimate in these terms is somewhat vague because of the different possible vector lengths (i.e., one could have a 512x512 checkerboard pattern of dots, but the eye could not necessarily resolve it). The display device used in experiments to date has been the Tektronix 564 storage oscilloscope with a 5″ viewing tube. This is an appreciably more sophisticated unit than required. The MODEL T deflection output is $\approx$ ½ volt/cm and requires a 100-kHz bandwidth deflection amplifier to drive the storage tube. A more spartan design would be adequate for the present application, and should cost appreciably less.

The repeatability of the display is quite good; the same message can be rewritten on top of itself without noticeable degradation. No problem exists with respect to drift, etc., after the normal warm-up time of the display scope. Three digital-to-analog techniques were breadboarded (operational amplifier integrator, binary-weighted resistance summer, binary ladder) and the binary ladder approach was selected. The binary ladder uses only two resistor values and has smaller current supply variations. The latter point made it possible to eliminate two separate, regulated power supplies for the output boards.

Data Source

The "natural" data source for the MODEL T is the telephone line. This is probably the most economic—and surely the most accessible—means of linking the display console with the remote computer. With reasonable care, a telephone line with a 3-kHz bandwidth can transmit up to $\approx$ 2400 bits/second. Higher data rates may be obtained under special conditions. The practical limit is set by the permissible error rate and hence is sensitive to the particular telephone line used on a given connection. Nominal adjustments in the timing circuits of the MODEL T make it compatible with any feasible telephone rate. For a given situation, the user must know the data rate and insert the proper timing plug into the input board.

Vector drawing rates of 10 to 240 vectors/second may be obtained over the telephone line. At 120 vectors/second, relatively complex figures may be written in a matter of seconds. This drawing rate has been found to be psychologically acceptable for many applications. Of course, substantially higher rates

may be obtained if an alternate data source (coax link) is available. The ultimate rate is limited by the writing speed of the storage tube (approximately 10,000 vectors/second).

A variety of options may be employed to interface with the telephone line. A Bell 202C data set is quite adequate for high speed applications. Where the data rate is lower or where the expense of the data set is to be avoided, acoustic coupling to the telephone set offers advantages. The signal into the teletype may be paralleled with a MODEL T to reduce the amount of equipment and permit drawing on the display (without typing) or typing (without drawing on the display).

Random errors will be introduced into code groups by noise in the telephone system. The MODEL T includes an automatic interrupt on a parity error (even or odd parity at users option). Upon detection of a parity error, the MODEL T will reject the vector, lock itself out, and signal the viewer that an error has been received. The normal means for interrupting the computer uses a narrowband signal and hence requires time. During this period between error detection and alerting the sender, the source may have sent several additional code groups. The recommended procedure is that the computer should back up to a previous reset signal, or a known absolute coordinate, on the display and generate signals from that point anew. It would be convenient for the computer to handle the transmission in blocks, storing the absolute beam position at the head of each block. An error would require retransmission of the block.

Character Generation

The basic MODEL T does not include a character generator, hence alphanumeric symbols must be generated from software commands and transmitted as a string of vectors. For the person with limited need for alphanumeric features, or for one who needs an extensive font, this is a reasonable arrangement. The primary drawback is drawing speed, since approximately 10 vectors may be required for each symbol. Provision has been made for the modular addition of a character generator for those who desire it. The MODEL T is modified to contain a mode switch. When a string of alphanumeric symbols are to be written, the message is preceded by the command "shift to character generator" which sets the mode switch and routes all subsequent signals to the character generator. The output of the character generator drives the X and Y output boards. To exit from the character generator mode, the message is terminated by a suitable non-print code which reverses the mode switch.

Even without a character generator the MODEL T draws alphanumeric symbols faster than a teletypewriter. The combination of the internal regeneration features in the storage tube and the lack of selective erase make it awkward to edit alphanumeric messages, unless one is willing to retransmit the entire string after each change. Thus, the MODEL T is not especially suited for extensive alphanumeric editing.

Cost

The cost of building duplicates of the MODEL T, on a laboratory scale, were approximately $500 exclusive of the display device ($1100 for the commercial storage scope). It appears that for a cost of under $2000 a personal display terminal with considerable flexibility could be produced, and it is not unreasonable to look forward to display systems which are comparable in cost to color TV sets.

APPLICATIONS

Considerable experience has been obtained with the MODEL T in an on-line mode with a remote time-shared computer. The key to effective computer graphics lies in the combination of user-oriented software with a low cost display. Substantial software assistance has been provided by colleagues of the authors at RCA Laboratories. A system has been demonstrated for the important mask-design artwork problem.

Using a convenient problem-oriented language, the user types the information describing the mask geometry. As the design proceeds, the operator may request a current picture of the mask on the MODEL T. The immediate visual feedback permits prompt error correction via a software patch. When the design is completed and checked, the program produces a paper-tape output containing control information for an automatic drafting machine. The resolution of the display does not affect the ultimate accuracy of the mask. Using this procedure, a one-day turn-around between design and the actual mask may be obtained.

For many situations the operator may desire a hard-copy text of the image on the display. Two means are currently employed: a Polaroid photograph provides a quick copy adequate for many purposes. For complex drawings where more resolution is required, or where it is desirable to be able to write on the copy, the MODEL T can provide signals for a digital or analog mechanical plotter.

SUMMARY

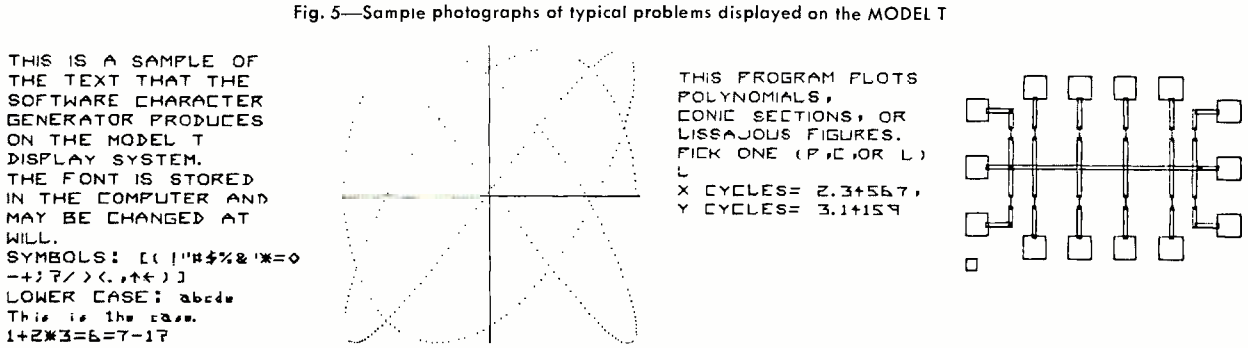
The MODEL T is intended to be useful in a dual sense. On one level it is a practical, flexible display device which can be quite useful to a user in problem solving or displaying information. By constructing units and placing them in a working environment, valuable feedback is obtained concerning the real needs in man-machine interaction. About 18 units are now in on-line operation at the RCA Laboratories and the various product divisions. In another sense, the MODEL T focuses on the information flow in a limited bandwidth link to a computer. Telephone lines will probably link the majority of future remote terminal systems. The question of how best to represent the data and what hardware is needed at each end of the link is important. Storage tube displays such as the MODEL T seem particularly suited for telephone modem systems.

It is not unreasonable to imagine display units based on the type illustrated by the MODEL T to be widely used in industry and at home. The logic is sufficiently simple that one might look forward to completely integrating it as a single wafer of MOS or bipolar transistors. The resulting personal display would be as compact and as portable as the popular miniature television sets.

ACKNOWLEDGEMENT

The authors express their appreciation to N. Jachetti who constructed many of the circuits in the MODEL T. They are indebted to Drs. R. Rosenfeld, R. Winder, and K. Kaplan for their progamming support and enthusiasm.

Fig. 5—Sample photographs of typical problems displayed on the MODEL T



Alphanumeric message

On-Line calculation of a lissajous figure, and

Mask for semiconductor application

LIMAC: A LARGE INTEGRATED MONOLITHIC ARRAY COMPUTER

A new approach to a computer organization promises very effective utilization of the large-scale integration (LSI) technology. A two-dimensional functional partitioning of logical structures is employed. First, data structures are grouped into functional modules which include a processing matrix and associated operand registers. Data processing control which is unique to the function is retained as an integral part of the functional module. Operands, control words, and status words flow between functional modules on a common set of bus wires. A simple centralized control responding to information transfer micro-instructions directs operation of this bus. Machine commands are comprised of a string of these information transfer micro-instructions.

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From left to right are S. Y. Levy, H. S. Miller, R. J. Linhardt and R. D. Sidnam.

THE SYSTEM ARCHITECTURE described in this paper overcomes the problems of current computer architectures which fail to effectively utilize LSI array technology. The total system is exceedingly flexible in both performance and instruction set. The fabrication of a hundred or more logic gates on a silicon chip presents new system and circuit design problems. Whether these large-scale integrated (LSI) arrays of logic gates are fabricated by careful control to obtain 100% acceptability of all the gates on the chip or whether discretionary wiring is used to avoid defective gates, circuit and system problems are basically the same. Problems of power dissipation, noise immunity, and signal levels are all interlocked with the environment of the circuit within an array. The system architectural problem is to derive maximum reliability and speed from the LSI technology by reducing external connections and encompassing all functionally related logic in one tightly packed array.

As this paper demonstrates, present system organizations can not effectively utilize the LSI technology; a new system architecture is required. Effective utilization of LSI while this new technology is still in its infancy is desirable. Employment of even a few modest-sized arrays in operational systems will give impetus to LSI and will provide LSI manufacturers with the feedback necessary to guide continuing technological development.

As an example of a new system approach, a general purpose computer capable of solving sophisticated navigational problems is being designed and built by RCA for the Air Force. This experimental computer, which will illustrate the effective use of large arrays, employs functional partitioning of both the data path and control structures. Functional partitioning of the control structure is unique with this computer's architecture and is the key to a very favorable utilization of arrays from 30 gates upward in size.

The circuits for array use are emitter-coupled logic gates. Fabrication techniques are being improved to the point where reasonable yields of 100% perfect arrays of 100 or more gates will be realized.

CURRENT SYSTEMS

Some current computers use a memory-oriented design (Fig. 1).[1] In this type of design, the multiplicity of registers used to store program instruction addresses, machine status words, intermediate numerical results, constants, etc., are all contained in one high-speed memory. A combinatorial processing matrix is inserted within the data-register regeneration-logic loop (heavy lines in Fig. 1). Actual data processing (such functions as incrementing, extraction, movement, table look-up, and status recognition) is accomplished in the memory-read/regenerate cycle: a memory read-process/regenerate cycle. Utility and intermediate storage registers buffer this processing loop to the main memory bank and input/output channels.

Not shown in Fig. 1 is the other half of the machine's logic which controls this data loop. Control logic encompasses all logic not directly associated with the data path. Control signals prime logic gates throughout the data path, and a sequence of priming signals carry out an instruction. The large set of dissimilar services that individual units in the data path are called upon to perform gives rise to a formless scattering of logic elements and in no sense can be considered regular or divisible.[2] If a gate appears to be connected in the same manner as its neighbors or roughly appears similar, then it is called regular. Thus, the data transfer paths between registers in a parallel machine are very much alike and are clearly regular, whereas a single gate hanging from the register and detecting an unique condition clearly could *not* be classified as regular. Compare the regularity of a data path register to control logic as illustrated in Fig. 2. In many machines, this control logic comprises 60% of the main frame logic. It is just this irregularity of control that hinders effective utilization of large arrays and calls for a new system architecture.

This need for a new system organizational approach is clearly demonstrated by attempting to partition current computer systems into arrays of a hundred or so logic gates. The practicality of any partitioning for large arrays is measured by the number of logic interconnections that must be made across the boundary (the bonded wire jumpers between bonding pads on the silicon chip and the pins or leads of the package). Currently, bonding pads are placed on 10-mil centers which would allow approximately 100 pads around the perimeter of a one-quarter-inch-square silicon chip. The objective, then, is to partition a computer into arrays that contain a maximum number of gates with a limitation on the number of pins. A measure of effective utilization of the LSI technology is the number of connections per array (the gate-to-pin ratio).

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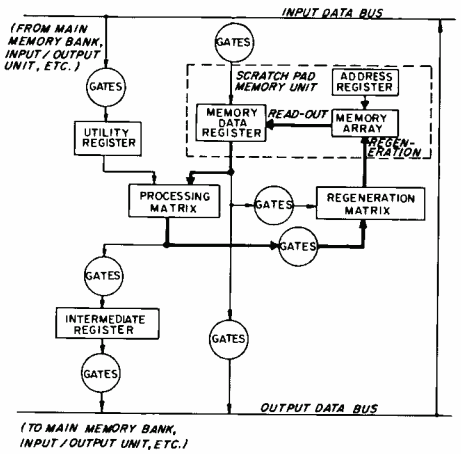
Fig. 1 — Black diagram of a memory-oriented computer architecture.



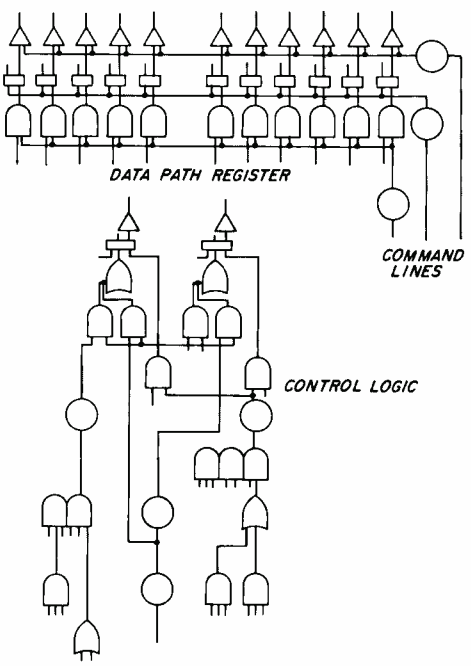


Fig. 2—Comparative example of regular data structures and irregular control structures.

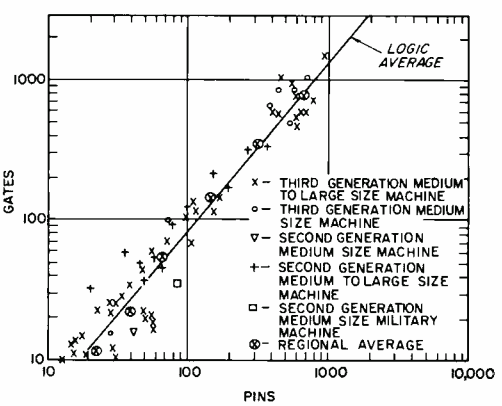


Fig. 3—Partitioning data for second and third generation computers. Medium size machines are 20,000 gates; medium-to-large machines are 30,000 gates.

The data in Fig. 3 illustrates the standard partitioning of a broad cross-section of existing computers.[3] This data includes computers constructed from both discrete components and integrated circuits during the past two generations. Each point in Fig. 3 represents the number of gates contained on a plug-in card, platter, etc., and the number of logical connections to the pins of the plug-in card or platter.

For example, a typical 3x4-inch plug-in card in a third generation medium-size machine contains 13 gates and has 30 logical connections to its pins. Thus, this card is represented by a *circle* at coordinate position (*13 gates, 30 pins*) in Fig. 3. A typical 17x18-inch interconnection platter in the same machine interconnects 865 gates contained on 69 plug-cards and has 480 logic connections to its terminals; this platter is repsenented by a *circle* at coordinate position (*865 gates, 480 pins*).

The main obstacle to constructing a conventionally organized computer with large arrays lies in the irregularity of the control structures. This irregularity is reflected in the excessive number of leads required to support a gate in the conventional system. Using 100 connections as a guide, Fig. 3 indicates that at most 130 logic gates will be encompassed by a large array. The average number is 85 gates for 100 connections. An average of 85 gates/array is not too satisfying when LSI technologists are suggesting a potential in the neighborhood of 1,000 gates/array. Current computer organizational techniques will fall an order of magnitude short in effective utilization of the large array technology.

REGISTER MACHINE CONCEPT—STEP 1

The evolution of a new system organization that has a more favorable use of large arrays should move towards a machine structured of modules (or arrays) wherein each module consists of a completely self-contained processor having local storage (or registers), some simple processing logic, and all control necessary for the array to execute its function. In this way, each array contains a buffer or register interface with the outside world, some processing logic, a control matrix, and a set of flip-flops used in the sequential portion of control. Each array control sees only the state of its own array and does not see the states of other arrays. Thus the array control structure is reduced from its conventional counterpart and the requirements for communication outside the array are reduced correspondingly. These considerations lead to the *register machine* concept so named for the registers that serve as the interface for the individual array.[4]

In contrast to earlier examples of partitioning for batch fabrication (or LSI)[2] a register machine is partitioned into separate, more sophisticated *instruction execution units* (IEU), each of which performs either one machine instruction or a very similar set of machine instructions. A generalized block diagram of a register machine is shown in Fig. 4. The boxes labeled IEU denote instruction execution units and a five-part machine bus serves as the communication channel between an IEU and main memory.

In the operation of a register machine, the contents of the program counter are used to fetch a program instruction from memory and load the instruction register. An operation group decoder attached to the instruction register activates the proper IEU for execution of the program instruction. An individual IEU is shown in Fig. 5. The decoder and data processing clock together generate the proper internal sequence of enabling and inhibiting signals for the adder. A buffer or register interface provides logical interface with the IEU and memory, and each IEU contains control logic for this register interface.

For example, an add command fetched from memory and loaded in the instruction register would cause the *add* IEU to be enabled. Subsequently, the add instruction would be transferred into the register interface of the *add* IEU and the control logic for the register interface would go about fetching the two operands from memory for the addition computation. After receipt of both operands, the adder logic is enabled and the operands are processed. The register interface control returns the computational result to main memory before the next machine instruction is fetched from memory.

Register machine designs for a character-oriented machine (RCA-301) and for a parallel-word machine (RCA-4102) have been completed down to the level of small logical blocks (e.g., 6-bit counter, 24-bit comparater, etc.) so that the NOR gate count is not precise. [*Editor's note:* Descriptions of the register-machine designs for the character-oriented machine (RCA-301) and the parallel-word machine (RCA-4102) were available as appendixes with the original manuscript of this paper. Due to space limitations, this material could not be included with the final version; however, the information is available from the authors.]

Estimating the count as closely as possible but always trying to keep an error on the conservative side, the gate count in the 301 register machine is of the same order as the count in the conventional 301. But the distribution of the gates is changed considerably: in the conventional design, some 63% of the gates are used for control—in the register machine this is reduced to less than 30%; also, in the conventional design, the register subsystems account for only 25% of the equipment—in the register machine, the register subsystems require about 65% of the machine. The control portion of the machine consists of those gates which are used to generate controlling signals. In the register machine, control consists of the operation decoder, the control matrices, the control counters, special comparators and address generators, special decoding gates, and the special control bits in the registers. The register subsystem includes the parallel gating into and out of the registers.

In contrast, the register machine version of the parallel-word 4102 requires somewhere between three halves and twice the quantity of equipment required in the original machine. The register-machine version is more regular in form, again especially in control, but the overall effect is not nearly so pronounced as it was in the case of character-oriented 301. This is a result of two factors:

1) The 4102 data path is larger than that of the 301, and is about as regular in structure;
2) The 4102 control is considerably smaller than that of the 301, and it is precisely in the control area that the register technique presents its greatest advantage over the conventional design methods.

Regularity, as defined above, is a property of the *gate* level of the machine. The major goal of the register machine concept is to obtain an increase in the regularity of the system. The register machine version of the 301 and 4102 were surely an improvement over the conventional designs on this basis. The only significant candidates for non-regularity are control matrices within an IEU. Control gating and counter portions of an IEU seldom run more than 50 gates. In register machines, data paths are different in form (they are larger than in the conventional design as evidenced by the five-part machine bus) but they remain regular. The quantity of equipment devoted to control is considerably reduced and what remains may far more reasonably be called *regular* than may the control in the two conventional machines. As an added bonus, the decentralized control eliminates much of the maze of long lines which emanate from a centralized control unit.

LIMAC CONCEPT—STEP 2

Functional partitioning at a machine command level was the first step in developing a system organization better suited to a large array. The next evolutionary step introduces a second dimension in the partitioning of control. Control is now divided into two functionally independent classes: *information transfer* and *data processing execution*. In oversimplified terms, memory addressing control is retained as a centralized feature while data processing execution control is decentralized throughout the processing modules now called *function execution units*. This is in contrast to the register machine concept that provides each IEU with capability for data retrieval and storage.

Data processing execution control is unique to the computation logic and its connections to the associated data registers contained within one processing module; information transfer control is common to all processing modules. Information transfer control directs instruction retrieval, data retrieval and storage, instruction and data transfers between machine registers and status word transfers, all over a common set of bus wires. No distinction is made between data and control words—only the *names* of transfer source and destination denote differences. Control and status words are logically complementary, i.e., a register name serving as the destination of a control word also serves as the source of a status word.

This second dimension in functional partitioning of the control structure treats operands, instructions and data addresses, and control and status words all in the same manner. This leads naturally to the elementary operation (EO) format of control (also known as microprogramming).[5-7] A program instruction is executed by set of control words wherein each one corresponds to a single step or elementary operation in the execution of the instruction. The high degree of flexibility inherent in EO control format is necessary to eliminate special-case-hardware configurations required in register machines to execute uniquely structured machine commands. The accumulator in the register machine 4102 is one example of a special-case-hardware configuration. With partitioning of the control structure, the full capability of all machine hardware can be utilized to implement uniquely structured machine commands.

Both information transfer and data processing control systems employ the EO format. Within a function execution unit, states of internal data path transmission gates and conditioning signals for the processing matrix are indicated by the binary pattern contained with the EO register (Fig. 7). The source and destination of an information transfer over the machine bus are specified by bit patterns contained in the instruction register. With EO control formats, irregular control structures are replaced by regular memory structures; the irregularity of control is transformed into the bit patterns stored in regular memory structures.

Even though the EO control format is a step towards regularizing control structures, selection of the proper EO sequence in current machines is governed by a collection of logic gates often referred to as sequencing logic. This centralized sequencing logic is complex due to the multiplicity of demands placed upon it. Numerous feedback conditions from data path logic must be handled. For example, an EO sequence for machine MULTIPLY must contain a branch operation to handle the two possibilities for the multiplier bit. In addition, other signals denote demands of input/output equipment, etc. It is the total collection of many such *conditional* feedback signals that still give rise to the irregular complexity of the control structures in the conventional machine.

Structural differences between LIMAC and the register machine are illustrated by comparing Figs. 4, 5, 6, and 7. Note that the machine bus structure has been reduced from five-parts to two-parts. In LIMAC, an *information transfer bus* carries the word transfers, and a *register identification bus* signifies register names of source and destination in the information transfers. Recognition logic, labeled *R* and associated with each LIMAC function execution unit in Fig. 6, decodes the identification signals contained on the identification bus and connects the register as either a sender or receiver to the information bus.

Unlike the register machine that operates in machine commands, LIMAC executes a string of *information transfer micro-instructions* for each machine command operation code. Thus, a machine instruction is executed by first transferring operands into a functional module. This is accomplished with one or more information transfer micro-instructions fetched from memory by the wired staticizing sequencer and executed in the instruction register. Then an EO control word is transferred into the EO register of the functional module thereby specifying the connectivity of the internal data structure for execution of the machine instruction; another information transfer micro-instruction accomplishes this EO word transfer.

The operation code of the machine instruction serves as the base address in memory of the sequence of micro-instructions defining the machine in-

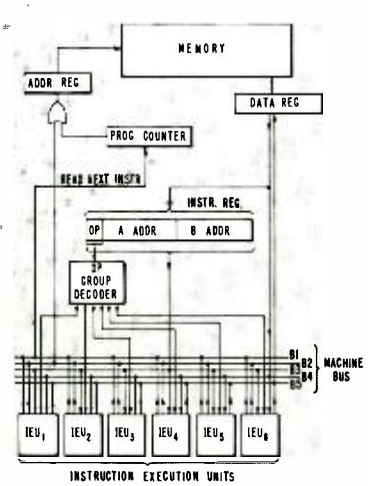
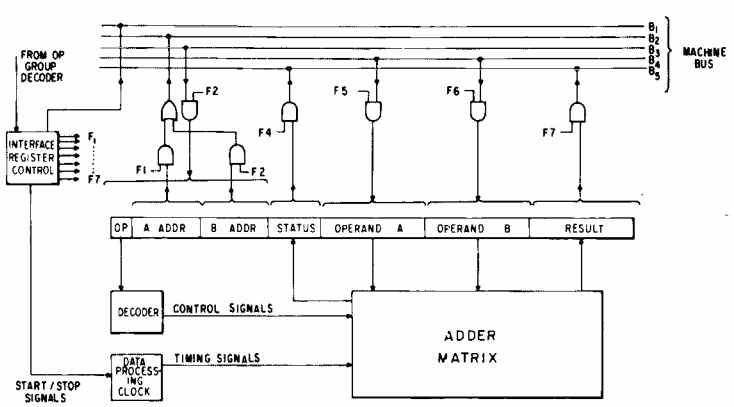


Fig. 4—General block diagram of a register machine. Five parts of the machine bus are: B1, read next instruction flag; B2, memory address; B3, instruction word B4, data word from memory; and B5, data word to memory.

Fig. 5—General block diagram of an instruction execution unit of a register machine.



struction. A termination bit on the last micro-instruction of the sequence causes the wired staticizing sequencer to fetch the next machine command from memory. Similar macro-to-micro language translation techniques are employed in other conventionally organized, contemporary machine, and as LIMAC does, a variable instruction machine language format is employed.[9,10]

In the execution of complex instructions such as multiply and divide, the LIMAC concept again takes advantage of the capabilities of the large array technology. The technology offers small, fast, fixed memories. Sequences of EO control words for multiplication, etc., can be stored in a fast fixed memory contained within a functional module. The output of the fixed memory serves as an alternate source for the gating and conditioning signals normally provided by the EO register (Fig. 7). Rather than transferring an EO control word describing the connectivity pattern into the EO register, a start address in the fixed memory is transferred to the function execution unit. The asynchronous feature of the machine bus permits independent operation of a module once a data process operation has been initiated. In slightly oversimplified terms, each function execution unit is a very specialized computer; all are capable of independent operation.

The information transfer control system interprets only two instructions: one instruction designates by name both the source and destination registers for an information word transfer. The second instruction designates the mask pattern used for comparison with a status register to implement conditional jumps. Conditional jumps are implemented by using an information transfer micro-instruction to move a status word from a function execution unit into the status register. The operation code of a conditional jump micro-instruction causes the AND/OR comparator network (Fig. 6) to match *ones* in the status register against *ones* in the instruction register. If at least one match occurs, the conditional jump is implemented by the wired staticizing sequencer. LIMAC has two fundamental types of conditional jump micro-instructions:

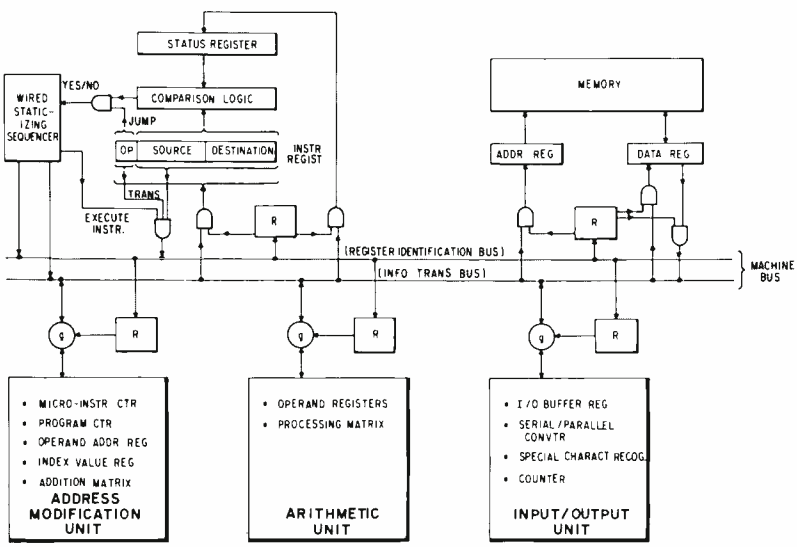


Fig. 6—General block diagram of a LIMAC machine.

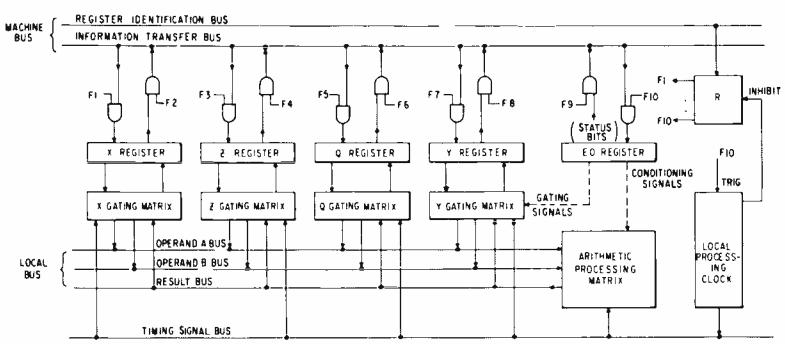


Fig. 7—General block diagram of a function execution unit in the LIMAC machine.

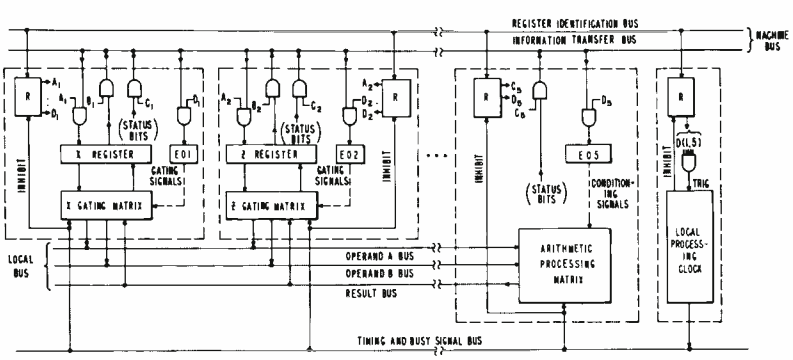


Fig. 8—Subpartitioning of a LIMAC functional unit. The doshed boxes indicate the subpartitions.

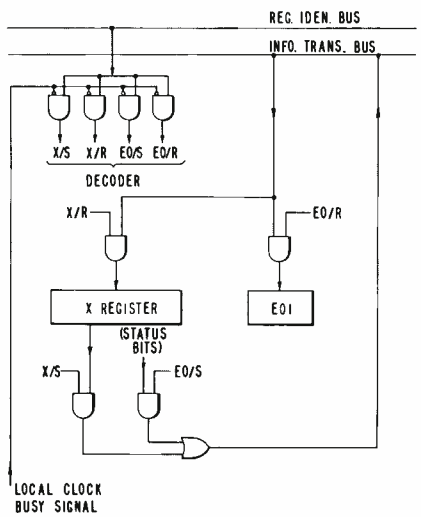


Fig. 9—Recognition logic. Decoded signals X/S, X/R, EO/S, EO/R indicate which register is to function as a sender or receiver in relation to the LIMAC information transfer bus.

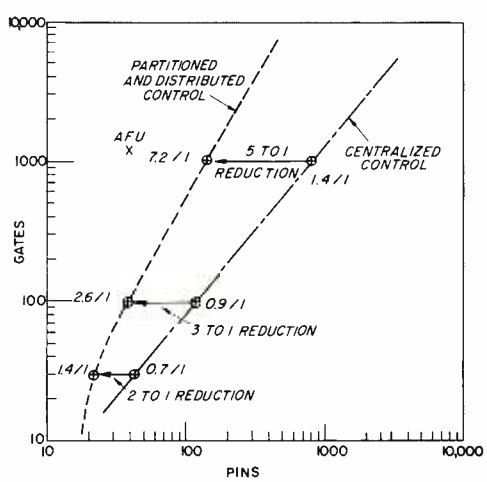


Fig. 10—Comparison of the average partitioning data of conventional architectures with the average LIMAC partitioning data.

1) *Conditional return:* if the status condition is present, software control moves to the next micro-instruction in sequence; otherwise software control is returned to the next machine instruction in sequence.
2) *Conditional skip:* if the test condition is present, software control moves to the next micro-instructions and executes the third in sequence.

This skip-over-two allows unlimited jumping of micro-programs throughout LIMAC's memory; the first micro-instruction contains the information transfer instruction for loading the micro-instruction counter with the contents of the second micro-statement. The micro-instruction counter is always pointing to the next micro-instruction.

Two additional features for conditional jumps are incorporated in LIMAC. One permits reversal in responses of the wired staticizing sequencer to the yes/no output of the comparator; i.e., the sequencer response for the presence of at least one status bit is interchanged with the response to the absence of all, and vice-versa. The second feature permits loading of the status register with the complement of the status word. Thus, the micro-programmer has four possible logical interpretations of status bits for each of the two conditional jump instructions at his disposal:

1) Jump on presence of at least one bit,
2) Jump on presence of all,
3) Jump on absence of at least one bit,
4) Jump on absence of all.

The hardware cost of this added flexibility is insignificant; the savings in micro-instructions is quite significant.

FUNCTION EXECUTION UNIT SUBPARTITIONING

Even though the LSI technology is undergoing rapid development, full integration of a complete LIMAC type of function execution unit on a single chip may not always be possible nor advisable. Testing of exceptionally large and complex arrays and a commonality often exhibited by subpartions of different categories of functional modules are two economic considerations which will moderate array size. A large array system organization must exhibit capability for effective subpartitioning. Fig. 8 illustrates how a LIMAC function execution unit is subpartitioned.

In formal terms, the composition of a functional module is a processing matrix for execution of the function and the operand registers associated with the execution of the function. Subpartitioning, then, is along the natural boundaries of the operand registers and processing matrix which comprise a functional unit. Data processing execution control is distributed among these subpartitions, and being EO formatted, distribution of data-processing control is simply segmentation of the EO register and replication of the machine-bus recognition logic.

Fig. 8 shows how an arithmetic unit is subdivided along the lines of operand registers with gating matrices, the arithmetic processing matrix, and the local processing clock. Each subpartition contains a small EO register that holds a subset of the control word normally stored in the EO register of Fig. 7. Recognition logic for gating status bits, EO commands, and operands to and from the information transfer bus is also an integral part of each subpartition. Fig. 9 illustrates the simplicity of this recognition logic. In Fig. 9, the decoded signals *X/S, S/R, EO/S, EO/R* indicate which register (*X* or *EO1*) is to operate as a sender (*S*) or receiver (*R*) in relationship to the information transfer bus.

A *local* bus structure interconnects the subpartitions of a functional module in the same sense that the machine bus interconnects all functional modules. Local-bus recognition logic is not a part of the sub-structures as is the case with the machine bus since the data processing execution control word is a logical union of control words *EO1* through *EO5*.

Each function execution unit operates on its own local processing clock as indicated in Fig. 8. This local clock is started by loading an EO command word into the composite of registers *EO1* through *EO5*. Timing signals are distributed to the subpartitions on the timing bus, and each individual recognition logic decoder is inhibited from operating as shown in Fig. 9.

LIMAC machine instructions are executed in an asynchronous mode. Progression from one micro-instruction execution to another is controlled by reply signals; the receipt of information by the receiver register generates a reply signal that causes the wired staticizing sequencer to advance. Inhibition of either the register sender recognition logic or register receiver recognition logic by a local processing clock prevents information transfer and execution of the micro-instruction until both local data processing clocks have completed their cycles.

The utility of the LIMAC concept in terms of gate-to-pin ratios is illustrated in Fig. 10. The average partitioning curve for conventional architectures (from Fig. 3) is reproduced in Fig. 10 for comparison with LIMAC partitioning data. Reductions in pin requirements (for reliability) by a factor of two or more are indicated. For larger arrays which would have a one-inch perimeter and support on the order of 100-pins, the average number of gates that can be utilized on the array is increased by almost an order of magnitude. LIMAC machines should benefit significantly from the performance potentials offered by the large array technology.

CONCLUSION

We have described two steps in the evolutionary development of a system architecture suited to large-scale integration. This evolutionary development has gone from conventional machine design first to a one-dimensional functional control partitioning (the register machine) and then to a two-dimensional EO formatted control partitioning (the LIMAC machine). The objective is not just to generate high gate-to-pin ratios for large arrays but more importantly to maximize the performance benefit offered by the LSI technology through employment of a functional module organization. The second step in evolutionary development retains this functional module organization without loss in computing flexibilities inherent in micro-programming.

The total system using the LIMAC concept is flexible in character. Functional modules communicate via a common data bus and have a standard interface; these modules are easily exchanged or added to customize or enhance total performance in terms of special needs. Through micro-programming, user language instructions are readily definable in terms of unique applications.

REFERENCES

1. A. T. Ling, "Scratchpad-Oriented Designs in the RCA Spectra 70", *Proceedings of the 1965 Fall Joint Computer Conference* (Nov. 1965) p. 667.
2. J. J. Pariser, "Connection Considerations with a View Toward Batch Fabrication", *Proceedings of the National Symposium of the Impact of Batch Fabrication on Future Computer* (Apr. 1965) p. 213.
3. A. T. Ling, formerly with the Electronic Data Processing Division of RCA, private communication (Nov. 1965). Mr. Ling is currently with Scientific Data Systems, Santa Monica, California.
4. S. Y. Levy, "The Register Machine: A Computer Organization Suitable for Batch Fabrication", presented at evening Session 3.1 at the National Symposium of the Impact of Batch Fabrication on Future Computers (Apr. 1965). Also presented at 1966 IEEE Workshop on Large-Scale Integration, Lake Arrowhead, California (Sep. 1, 1966).
5. M. V. Wilkes, "Micro-Programming", *Proc. EJCC* (1958) p. 18.
6. J. A. Weisbecker, "Data Processing System", U.S. Patent No. 3,309,679 (issued March 14, 1967).
7. C. R. Campbell, D. A. Neilson, "Micro-Programming The Spectra 70/35", *Datamation*, p. 64, September 1966.
8. H. R. Beelitz, H. S. Miller, R. J. Linhardt, R. D. Sidnam, "Partitioning for Large-Scale Integration", *Digest of Technical Papers*, International Solid-State Circuits Conf., Philadelphia (Feb. 1967).
9. A. L. Spence, "Hardware and Software Interactions—A Machine Organization Solution—The Variable Instruction Computer", presented at First Spaceborne Computer Workshop, Aerospace Corporation (Sep. 1966).
10. E. H. Miller, "Reliability Aspects of the RCA/USAF Variable Instruction Computer", RCA reprint PE-361.

A RANDOM-VIBRATION FATIGUE ANALYSIS

This paper offers a simplified approach to the complex problem of random vibration, a new environmental requirement of the missile and rocket era. The essentials of random vibration theory are used to establish a fatigue analysis. A general discussion is offered on the elementary principles of sinusoidal input and response before application to the random case. Then random vibration is briefly described and the basic means of measurement are presented. The vibration so obtained describes the environment. The random response is determined from this with fatigue-producing parameters equivalent to the sinusoidal case. Fatigue criteria for sinusoidal stresses are defined and adjusted for random stresses. Then the results of NASA random-fatigue tests are presented to indicate that fatigue life is unaffected by spectral shape. The narrowband response is described and its clearly defined character is suggested as an analytical model for the general random vibration. The probability aspects are given for the ultimate objective of achieving the stress-cycle count. Finally a problem of random-fatigue is presented for a simple beam with single degree of freedom.

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MATERIAL FATIGUE of a structural member is primarily the result of repeated stress reversals. These reversals occur when a member is exposed to a source of vibration—sinusoidal or random. For sinusoidal vibration the member responds to a single exciting frequency as determined by its own resonance and damping. For the general random vibration, which encompasses a wide range of frequencies, the member responds to each frequency component according to its resonance and damping. In each case, the member experiences fatigue due to its vibrational response.

A beam or structure which supports mass is elastic and can be damped internally and externally. This elastic system is typically shown by the model of Fig. 1a, being vibrated sinusoidally.

The resonant frequency, f_n, of the system in Hertz (cycles/second) is:

$$f_n = (1/2\pi)\sqrt{k/m} \qquad (1)$$

where k is the spring constant (lbs./inch deflection) and m is mass in slugs.

The sinusoidal exciting vibration is shown in Fig. 1b as a plot of acceleration in g units versus time. The peak amplitude is A and exciting frequency is f. The mass is vibrated sinusoidally at the same exciting frequency f, but its acceleration is multiplied by a transmissibility factor T. Thus, the acceleration response of the mass is:

$$g_r = Tg_o \qquad (2)$$

and its time history is shown in Fig. 1c where the peak amplitude becomes $T{\cdot}A$. The transmissibility factor is defined by:

$$T = \left[\frac{(Qf_n/f)^2 + 1}{(Qf_n/f)^2 - Q^2 + 1}\right]^{1/2} \qquad (3)$$

where f is the exciting frequency; f_n is the resonant frequency; and Q is the amplification factor. Q is a function of the system damping; a system is considered lightly damped when $Q \geq 10$. A linear plot of transmissibility versus frequency ratio for $Q = 10$ is shown in Fig. 2.

The structural member now experiences fatigue because of exposure to its own response. Thus, the spring of Fig. 1a is being fatigued by the response vibration of Fig. 1c. The time histories of sinusoidal vibration shown in Fig. 1b and 1c do not present a problem for determining instantaneous values of acceleration. They are completely defined by frequency and constant amplitude. However, the general case of random vibration is not deterministic for instantaneous values and its time history appears typically erratic as shown in Fig. 3.

The source of such vibration is usually the combustion and exhaust areas of a rocket or turbojet engine. The immediate structure responds and provides a random input for the attaching elements and equipment. No periodicity exists for peak amplitude and crossings of the time axis; the vibration is considered as an aggregate of component vibrations over a wide frequency range. The amplitude of each frequency component varies randomly with time. The time record of Fig. 3 does not provide an analytical definition for random vibration. However, the statistical nature of such vibration can be defined by a spectral plot which is generated using the following basic arrangement. An accelerometer-transducer attached to the source converts accelerations to proportional voltages over the entire frequency range of the vibration. A narrowband filter restricts the accelerometer output signal. This remaining narrowband signal is then squared and recorded on an oscillograph. When the squared voltage is calibrated to squared acceleration, the result is an oscillograph record as

This analysis was successfully employed at RCA for the VHF transceiver on the Lunar Excursion Module (contract NAS-9-1100 for NASA through Grumman Aircraft Engineering Corp.) Final manuscript received 1, August, 1967.

Fig. 1—Input and response for sinusoidal vibration: (a) vibration model, (b) input, (c) response.

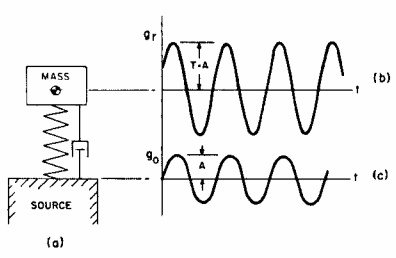
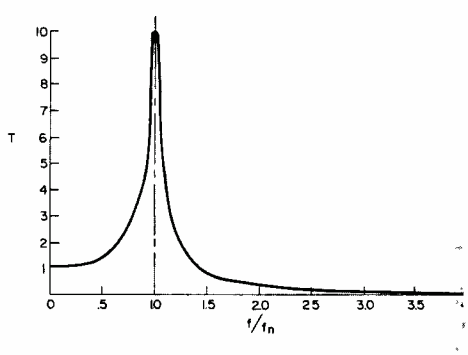


Fig. 2—Transmissibility curve for Q = 10.



shown in Fig. 4. If the record is of sufficient time duration $(t_2 - t_1)$, the mean square acceleration becomes

$$\overline{g_o^2} = \frac{1}{(t_2 - t_1)} \int_{t_1}^{t_2} g_o^2 dt \qquad (4)$$

The mean squared acceleration measured through the filter bandwidth Δf can be expressed in density form as:

$$G_o = \overline{g_o^2}/\Delta f = g^2/\text{Hz} \qquad (5)$$

As bandwidth is continually reduced, the square of an RMS random acceleration becomes proportional to the bandwidth, or $\overline{g_o^2} \propto \Delta f$. Therefore, as Δf decreases, the quantity g^2/Hz approaches a constant value. This becomes the spectral density for a center frequency f of bandwidth Δf. Filters may be deployed over the entire frequency range for determining spectral density at many center frequencies. The spectral densities can then be plotted as functions of frequency (Fig. 5) for defining the random vibration at the source.

Each frequency component for the plot in Fig. 5 is expressed in terms of the square of acceleration. The response to each is then obtained by squaring Eq. 2.

$$g_r^2 = T^2 g_o^2 \qquad (6)$$

The transmissibility in Fig. 2 is now squared to obtain T^2 versus f/f_n as in the logarithmic plot of Fig. 6.

The spectral density curve of Fig. 5 is now considered as an input to the elastic system. Applying Eq. 6 results in the spectral response curve of Fig. 7.

The area under the spectral response curve represents the total mean-square acceleration of the elastic system's mass. Thus:

$$g_{RMS}^2 = \int_{f_1}^{f_2} G_r(f) df \qquad (7)$$

Fig. 3—Typical random-vibration plot.

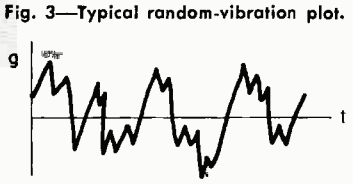
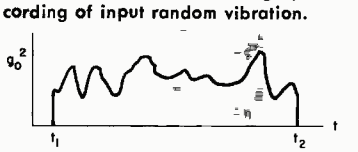


Fig. 4—Narrowband oscillograph recording of input random vibration.



The root mean square value, g_{RMS}, defines the measure of amplitude for long time periods of the random case typified in Fig. 3. A statistical frequency also exists for random vibration and is expressed by:[2]

$$f_k^2 = \int_{f_1}^{f_2} G_r(f) f^2 df \Big/ \int_{f_1}^{f_2} G_r(f) df \qquad (8)$$

The expression defines, for Fig. 3, an average frequency of crossing the time axis with positive slope. It should be observed that the numerator of Eq. 8 is the moment of inertia of the spectral density plot about the ordinate axis. The denominator is the area of the spectral plot and therefore f_k is the radius of gyration of the spectral density area about the ordinate axis.

As a sinusoidal vibration is defined by its constant amplitude and constant frequency, we now have the statistical counterparts for random vibration expressed as amplitude and frequency by Eqs. 7 and 8, respectively. Fatigue, in both cases, depends on a stress-cycle count. These parameters are easily obtained for sinusoidal vibration, but are dealt with by statistical means for random vibration. A random stress can only be expressed in terms of probability of occurrence. The probability aspects will be described later in the paper.

FATIGUE CRITERIA

Fatigue data is obtained from sinusoidal vibration and is given as stress amplitude versus number of cycles to failure. The plotted data is known as an *S-N* curve (Fig. 8). This data is available for structural materials of smooth and notched specimens.[3]

Fatigue damage can be determined for a structural member responding to a sine vibration. Its vibration response, typical of Fig. 1c, is known for amplitude, frequency, and exposure time. The stress amplitude is S_1; the actual number of cycles, n_1, is the frequency-time product; and the number of cycles to failure, N_1, is obtained from the curve of Fig. 8. The damage at this stress level, is then expressed as the consumed fraction of life by the ratio n_1/N_1.

The same structural member may be exposed to other levels of vibration independently. Knowing the parameters for each vibration level, we can determine their respective damage ratios n/N. The total damage is then defined by Miner's Hypothesis, which is given in the following series:

$$\sum \frac{n}{N} = \frac{n_1}{N_1} + \frac{n_2}{N_2} + \cdots + \frac{n_k}{N_k} = 1 \qquad (9)$$

Fig. 5—Input spectral density.

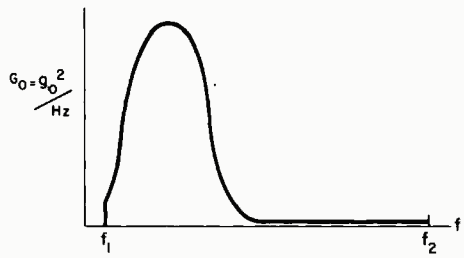


Fig. 6—Transmissibility-squared curve for Q = 10.

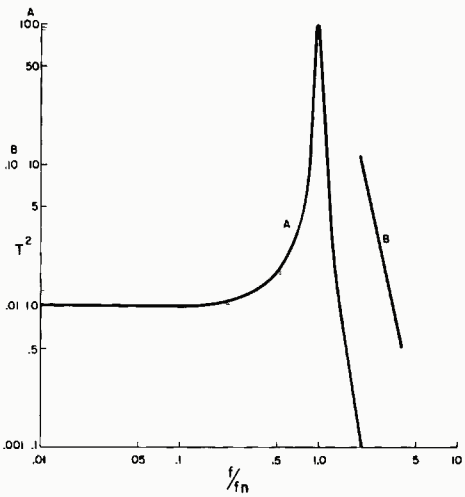


Fig. 7—Spectral density response.

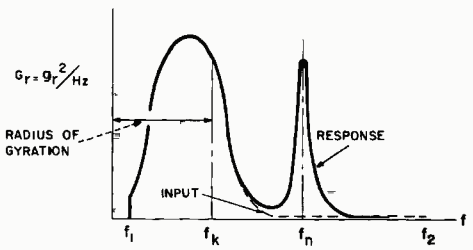
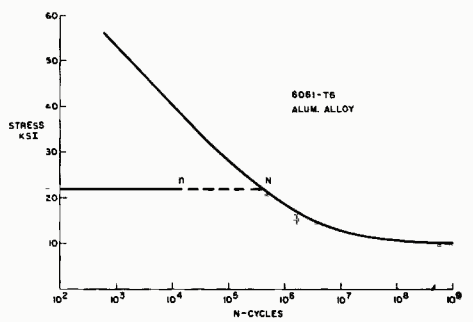


Fig. 8—Stress versus number of cycles to failure.



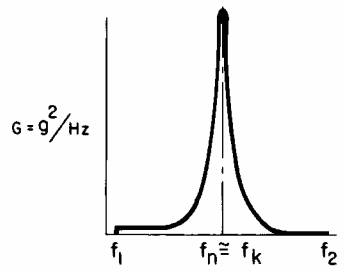


Fig. 9—Spectrol density response—narrowband.

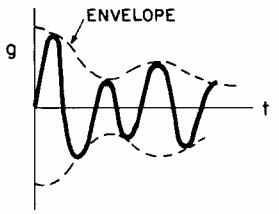


Fig. 10—Time record for narrowbond response.

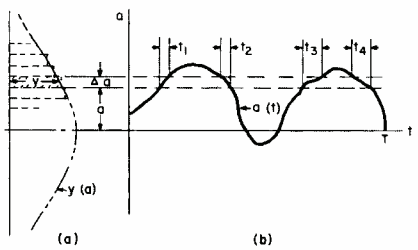


Fig. 11—Relationship of distribution to random signal: (a) distribution and (b) random time record.

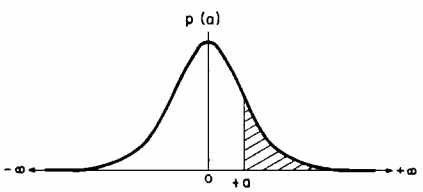
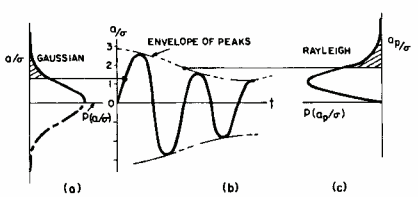


Fig. 12—Gaussian probability density.

Fig. 13—Relationship between Gaussian and Rayleigh density and a random sinusoid: (a) Gaussian density, (b) time record of random sinusoid, (c) Rayleigh density.



The cumulative law is reliable for the general case of sinusoidal vibration, but must be modified for others. Therefore, it is convenient to define the law as;

$$\sum n/N = C \text{ (constant)} \qquad (10)$$

Values of C are reflected in the many types of vibration and order of stress application. It may also be influenced by the range of stress levels. A value of $C = 0.5$ is recommended for random vibration.[4]

Equivalent S-N curves for random vibration do not exist for the many various structural alloys. Therefore, the sinusoidal fatigue criteria will be adapted to our random-fatigue analysis.

RANDOM-FATIGUE TEST RESULTS

In accordance with the best available random-fatigue test data, the following is pertinent to our analysis:[1] the shape of the spectral-density response curve does not affect random-fatigue life. Random-fatigue life for any given stress level is defined as the product of statistical frequency (Eq. 8) and time of exposure to failure. This criteria will be used for establishing the base of a random-fatigue analysis for all spectral shapes.

This test data was made available in late 1965, and served to substantiate the assumptions used for a random-fatigue analysis, similar to that in this paper.

NARROWBAND VIBRATION

A narrowband random vibration is exemplified by a grouping of significant spectral density within a range of frequencies whose width is small compared with the magnitude of the center frequency (Fig. 9). The narrowband process is typical for highly resonant systems which are characterized by low damping. The sample function as dominated by this narrowband spectrum is shown in Fig. 10.

The function appears as a sinusoid with frequency f_n but with slowly varying random amplitude and random phase. The statistical frequency f_k approaches the resonant frequency f_n as the random vibration narrows in bandwidth.

The function is recognized as possessing individual cycles and the envelope as being a smooth continuous function in itself. The instantaneous value of random amplitude follows a very definite statistical law and the envelope function follows another related statistical law.

Because random fatigue life is independent of spectra shape, the clearly defined characteristics of the narrow-band process can serve as the model for a random-fatigue analysis.

PROBABILITY

Statistical processes obey probability laws which express, by fraction of time or frequency of occurrence, that a certain event is expected within certain limits. Therefore, probability theory is applied to random vibration where the amplitude cannot be defined for any instant but may be expressed in percent of time it lies within given limits. Fig. 11b is a sample of a random signal taken over the time T.

The probability that the function $a(t)$ lies within (a) and $(a + \Delta a)$ is related to the fraction of time $\Delta t/T$, where $\Delta t = t_1 + t_2 + t_3 + t_4$. This can be represented in Fig. 11a by a corresponding rectangular element whose area is $y \cdot \Delta a$. The length, y, of the element is the average probability density for the interval Δa. Increments of Δa can be taken in both directions of amplitude until a series of rectangular elements are obtained. A smooth curve drawn through the elements as shown in Fig. 11a will give us an approximate probability density function $y(a)$. Each element here, expressed in fraction of time, becomes:

$$y(a) \cdot \Delta a = \Delta t/T$$

and

$$y(a) = \Delta t/\Delta a \cdot T \qquad (11)$$

The probability density function becomes precise when Δa and Δt approach zero, and the time, T, becomes infinite. The function now denoted by $p(a)$ is defined by the following (where the limit is assumed to exist):

$$p(a) = \lim_{\Delta a \to o} \lim_{T \to \infty} (\Delta t/\Delta a \cdot T) \qquad (12)$$

When $p(a)$ is known over the entire range of the random function $a(t)$ we can express the probability of the function lying within the interval α to β by the following:

$$\text{Prob}[\alpha < a(t) < \beta] = \int_{\alpha}^{\beta} p(a)da \qquad (13)$$

The probability that the function lies between $-\infty$ and $+\infty$ is 1; therefore:

$$\int_{-\infty}^{+\infty} p(a)da = 1 \qquad (14)$$

The amplitude of random vibration varies statistically with time according

to the Gaussian probability law. This law is characteristic of many statistical phenomena in nature and its probability density is expressed as:

$$p(a) = \exp(-a^2/2\sigma) \Big/ \sigma\sqrt{2\pi} \quad (15)$$

where a is the variable amplitude, and σ is the standard deviation (RMS value of the variable amplitude).

As previously mentioned, the square of the amplitude a is integrated over a long time period to obtain the mean-squared average $\overline{a^2}$. The square root of $\overline{a^2}$ becomes a_{RMS} and is designated by σ. The RMS value is used as a reference level to which all other levels of amplitude are related. The probability density curve is shown in Fig. 12. The probability of exceeding any instantaneous amplitude $+a$ in fraction of time is the shaded area and becomes:

$$\int_{+a}^{+\infty} p(a)da = \frac{1}{\sigma\sqrt{2\pi}} \int_{+a}^{+\infty} \exp(-a^2/2\sigma^2)da \quad (16)$$

It is convenient to express a in dimensionless form in σ units. Therefore the ratio a/σ now becomes a non-dimensional amplitude and its plot against time for the narrowband random vibration may be represented as in Fig. 13b. The significance of the Gaussian density curve in relation to the random sinusoid is shown in Figs. 13a and 13b. The shaded area of the probability curve indicates the fraction of time any amplitude $+a/\sigma$ of the sinusoid is being exceeded.

The sinusoid of Fig. 13b, when related to amplitude of stress, contributes to fatigue damage by its peaks and stress reversals. Therefore, a probability function describing the envelope of peaks related to the Gaussian σ will determine the distribution of peak values over time. The Rayleigh probability law, which is derived on the supposition of a Gaussian random amplitude, satisfies this definition. The Rayleigh Probability density function is expressed by:

$$p(a_p) = (a_p/\sigma)\exp(-a_p^2/2\sigma^2) \quad (17)$$

where a_p is the variable peak amplitude or any point on the envelope of peaks, and σ is the RMS value of amplitude of Eq. 15. The Rayleigh Probability curve for the density function of Eq. 17 may be represented in Fig. 14. The probability of exceeding any peak amplitude $+a_p$ in fraction of time is the shaded area and becomes:

$$\int_{+a_p}^{\infty} p(a_p)da_p = \int_{+a_p}^{\infty} (a_p/\sigma^2)\exp(-a_p^2/2\sigma^2)da_p = \exp(-a_p^2/2\sigma^2) \quad (18)$$

Again we may resort to the dimensionless form of expressing amplitude in units of σ by letting $r = a_p/\sigma$. (19)

If we consider the envelope function of Fig. 13b to be $r(t)$, the result of Eq. 18 in this dimensionless form is:

$$\text{Prob}[r < r(t) < \infty] = \exp(-r^2/2) \quad (20)$$

The Rayleigh density curve is shown in its proper relation to the random sinusoid in Figs. 13b and 13c. The shaded area represents the fraction of time any value $r = a_p/\sigma$ of the envelope is being exceeded.

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The integral of Eq. 20 may be plotted against r as in Fig. 15. This universal curve for the Rayleigh probability offers the analyst a graphical method for selecting time increments. The analyst can also tabulate the integral of Eq. 20 as in Table I.

The tabular form is constructed by listing r and percent of time exceeding r. The difference between adjacent time percentage yields Δt percent and an average $\bar{r}$. The same result can be obtained from Fig. 15. The last two columns of Table I will be used in our fatigue analysis.

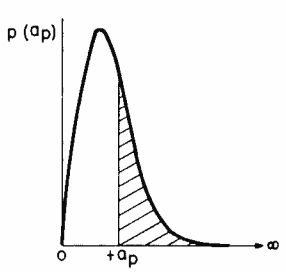


Fig. 14—Rayleigh probability density.

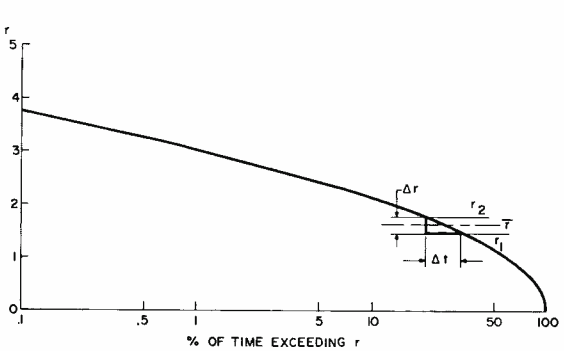


Fig. 15—Rayleigh probability distribution.

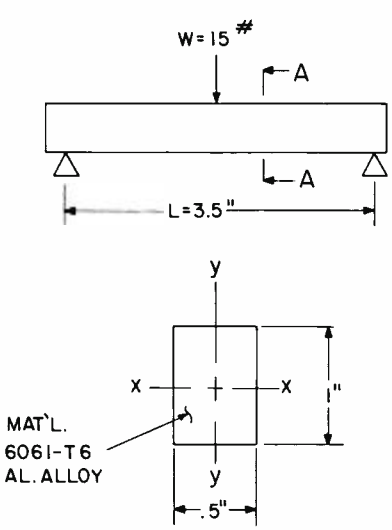


Fig. 16—Vibration model.

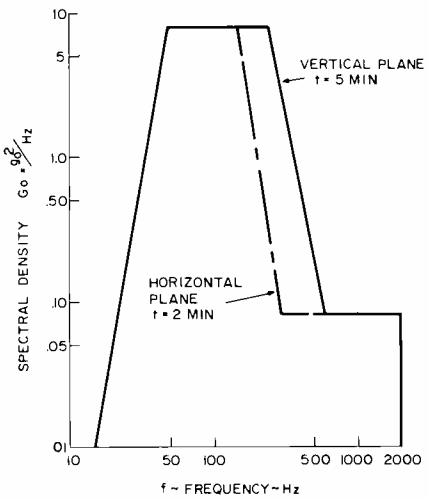


Fig. 17—Logarithmic plot of input requirements.

TABLE I—TABULATION OF VALUES FROM EQ. 20.

r	% time exceeding r	$\bar{r}$	$\Delta t\%$
		3.625	0.140
3.625	0.140	3.50	0.196
3.375	0.336	3.25	0.421
3.125	0.757	3.00	0.846
2.875	1.602 $\Delta t\%$	2.75	1.585
2.625	3.187	2.50	2.768
2.375	5.955	2.25	4.497
2.125	10.452	2.00	6.783
1.875	17.235	1.75	9.462
1.625	26.697	1.50	12.150
1.375	38.847	1.25	14.255
1.125	53.102	1.00	15.086
0.875	68.188	0.75	14.066
0.625	82.254	0.50	10.956
0.375	93.210	0.25	6.013
0.125	99.220	0.063	0.778
0.000	—		

SAMPLE PROBLEM

Assume that an equipment of given weight is supported as a simple beam in all directions. The beam represents the integral support structure of the equipment. This elastic system is exposed to separate test environments described as random vibrations for given test times and its fatigue effects are then analyzed. Our vibration model is shown with sectional properties in Fig. 16.

The resonant frequency of a concentrated load at the center of an assumed weightless simple beam is:

$$f_n = \frac{1}{2\pi}\sqrt{\frac{48EIg}{WL^3}} \qquad (21)$$

where E is the modulus of elasticity of the beam material (lb/in^2); I is the moment of inertia of the beam section (in^4); g is the acceleration of gravity (386 in/sec^2); W is the weight of the load on the beam (lbs); and L is the length of the span (in).

Therefore, the vertical resonance is:

$$f_{ny} = \frac{1}{2\pi}\sqrt{\frac{48 \times 10.5 \times 10^6 \times 0.0417 \times 839}{15 \times (3.5)^3}} = 565 \text{ Hz}$$

and the horizontal resonance is:

$$f_{nx} = f_{ny}\sqrt{I_y/I_x} = 565\sqrt{\frac{0.0104}{0.0417}} = 285 \text{ Hz}$$

For simplification, the effect of shear deflection on resonant frequency is not considered.

The customer or contracting agency specifies the environment for which the engineer designs his product. For random vibration, it is defined by a spectral density plot and exposure time and is submitted to the vendor as a design test condition. The logarithmic plot in Fig. 17 typifies this input requirement and is used for our sample fatigue analysis. Vertical and horizontal conditions are applied separately.

The response to the inputs of Fig. 17 is:

$$G_r = T^2 G_o \qquad (22)$$

where G_r is spectral density response; T is transmissibility; and G_o is spectral density input.

By assuming the elastic system in Fig. 16 to be damped so that $Q = 10$, the values of T^2 are obtained from Fig. 6 which plots T^2 versus f/f_n. The response to the vertical plane input for a resonance of $f_n = 565$ Hz is tabulated in Table II; the response to the horizontal plane input for a resonance of $f_n = 285$ Hz is tabulated in Table III.

TABLE II—VERTICAL PLANE RESPONSE TO $f_n = 565$ Hz

Input				Response
f	G_o	f/f_n	T^2	$G_r = G_o \times T^2$
15	0.01	0.027	1	0.01
20	0.05	0.035	1	0.05
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
450	0.36	0.796	6.70	2.41
500	0.22	0.885	19.	4.18
565	0.105	1.000	100	10.50
600	0.08	1.062	40	3.20
650	0.08	1.150	10	0.80
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1800	0.08	3.190	0.013	0.0010
2000	0.08	3.540	0.009	0.0007

TABLE III—HORIZONTAL PLANE RESPONSE TO $f_n = 285$ Hz

Input				Response
f	G_o	f/f_n	T^2	$G = Go \times T^2$
15	0.01	0.053	1	0.01
20	0.05	0.070	1	0.05
30	0.48	0.105	1.02	0.49
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
250	0.27	0.875	14.00	3.78
285	0.09	1.000	100	9.00
300	0.08	1.053	45	3.60
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1600	0.08	5.610	0.0014	0.00011
1800	0.08	6.320	0.0010	0.00008
2000	0.08	7.020	0.0008	0.000064

The input and response spectral densities of Tables II and III are plotted in Figs. 18 and 19, respectively. At this point, only the response curve is important. The input curve is plotted here for demonstrating the effect of the elastic system on the input to produce a response. If the system were so rigid that its resonant frequency is, say $f_n = 3000$ Hz, then the response curve would practically coincide with the input curve.

As previously stated, only the response curve properties are required for a fatigue analysis. The input spectral density can easily be expressed mathematically as a function of frequency, but the response function becomes too cumbersome. Therefore, the essential param-

Fig. 18—Spectral density response for $f_n = 565$ Hz in the vertical plane.

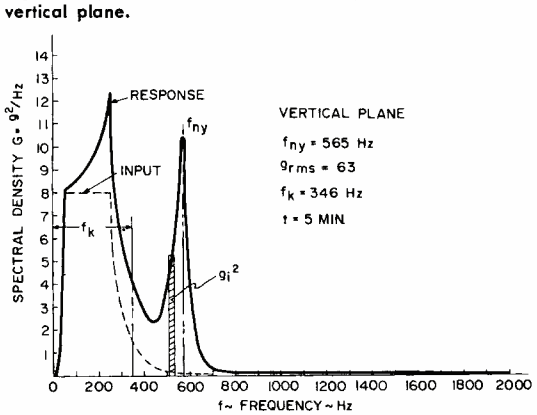
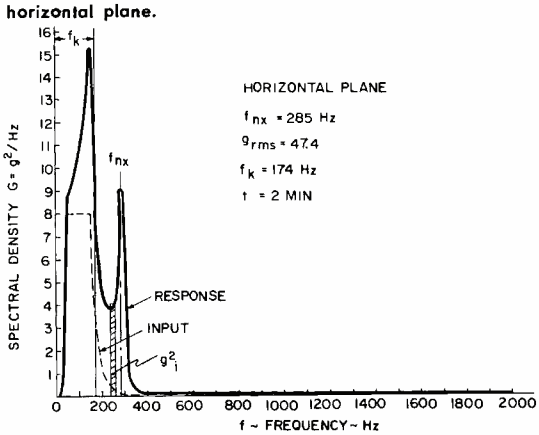


Fig. 19—Spectral density response for $f_n = 285$ Hz in the horizontal plane.



eters required for fatigue are best extracted from the spectral density response by applying Eqs. 7 and 8 by graphical methods. The area beneath the spectral response curve can be divided into rectangular elements and the graphical integration of Eq. 7 performed to obtain the g_{RMS} or 1-σ value. Also, for determining the statistical frequency of Eq. 8, the moment of inertia of all rectangular elements about the ordinate axis is the integral of the numerator. As previously mentioned, the denominator is the area beneath the spectral response curve. Thus, the integrations of Eq. 8 can be performed graphically to obtain the statistical frequency in terms of radius of gyration of the response area about the ordinate axis. If the response areas of Figs. 18 or 19 are divided into rectangular elements as typified by g_i^2, then the 1σ value is:

$$g_{RMS}^2 = \sum_{i=1}^{n} g_i^2 \qquad (23)$$

The statistical frequency, f_k, is the radius of gyration about the ordinate axis and is expressed as:

f_k^2 = Moment of Inertia/Area

$$= \sum_{i=1}^{n} g_i^2 f_i^2 / \sum_{i=1}^{n} g_i^2 \qquad (24)$$

The integrations of Eqs. 23 and 24 have been performed in the prescribed manner for the response areas of Figs. 18 and 19. The resulting 1-σ values and statistical frequencies are respectively shown on Figs. 18 and 19. A tabulation for the operations of Eqs. 23 and 24 would appear as follows:

Item i	G	Δf	$g_i^2 = Gx\Delta f$	f_i	$g_i^2 f_i^2$
1	G_1	Δf_1	g_1^2	f_1	$g_1^2 f_1^2$
.	.	.	.	.	.
.	.	.	.	.	.
n	G_n	Δf_n	g_n^2	f_n	$g_n^2 f_n^2$
			$\sum_{i=1}^{n} g_i^2$		$\sum_{i=1}^{n} g_i^2 f_i^2$

TABLE V—STRESS-CYCLE COUNT FOR THE HORIZONTAL PLANE

r	Δt%	Stress S	Time (sec) $t = (t/100) \times 2 \times 60$	$n = f_k \times t$	N (Fig. 8)	n/N
3.625	.140	54,300	0.168	29	800	0.0362
3.50	.196	52,325	0.235	41	1,100	0.0372
3.25	.421	48,600	0.505	88	2,100	0.0420
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1.25	14.255	18,688	17.104	2,976	1,000,000	0.0030
1.00	15.086	14,950	18.104	3,150	4,000,000	0.0008
0.75	14.066	11,213	16.879	2,937	60.000,000	—
0.50	10.956	7,475	13.147	2,288	—	—
0.25	6.013	3,738	7.212	1,255	—	—
0.063	0.778	942	0.936	163		—

$\Sigma n/N = 0.3034$

Stress-Cycle Count (Vertical)

From Fig. 18, $g_{RMS} = 63$; $f_k = 346$ Hz; $t = 5$ min. From Fig. 16, maximum bending stress at 1σ:

$S = g_{RMS} \times MC/I_x = 63 \times (15/2) \times 1.75 \times 0.5/0.0417 = 9900$ lb/in^2

From Table I, $\overline{r}$ and Δt% are used in the first two columns of Table IV with $\overline{r}$ now shown as r.

NOTES:

1) The stress amplitude, $S = r \times 9900$;
2) The cycles used at any stress level, $n = f_k x t$;
3) The available cycles to failure at any stress level, N, is found from Fig. 8.

Stress-Cycle Count (Horizontal)

From Fig. 19, $g_{RMS} = 47.4$; $f_k =$ Hz; $t = 2$ min. From Fig. 16, max. bending stress at 1σ (Table V):

$S = g_{RMS} \times MC/I_y = 47.4 + (15/2) \times 1.75 \times 0.25/0.0104 = 14{,}950$ lb/in^2

NOTES:

1) The stress amplitude, $S = r \times 14950$; and
2) Notes 2) and 3) of Table IV apply.

Random-Fatigue Damage

The results of Tables IV and V are independent because the random vibrations of the vertical and horizontal planes do not occur simultaneously. Since any corner of the beam section of Fig. 16 experiences the stresses of Table IV and V, the total damage becomes:

$$\Sigma\, n/N = 0.110 + 0.303 = 0.413$$

The contracting agency desires to know how far the actual damage is from fatigue failure. This is best described by a margin of safety, M, in percent:

$$M = 100\left(\frac{c - \Sigma n/N}{\Sigma n/N}\right) = 100\left(\frac{0.5 - 0.413}{0.413}\right) = 21\%$$

TABLE IV—STRESS-CYCLE COUNT FOR THE VERTICAL PLANE

r	Δt%	Stress S	Time (sec) $t = (t/100) \times 5 \times 60$	$n = f_k \times t$	N (Fig. 9)	n/N
3.625	0.140	35,900	0.420	145	11,100	0.0131
3.50	0.196	34,650	0.588	203	25,000	0.0081
3.25	0.421	32,175	1.263	438	40,000	0.0110
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1.25	14.255	12,375	42.759	14,795	15,000,000	0.0010
1.00	15.086	9,900	45.261	15,661	—	—
0.75	14.066	7,425	42.198	14,601	—	—
0.50	10.956	4,950	32.868	11,373	—	—
0.25	6.013	2,475	18.030	6,239	—	—
0.063	0.778	624	2.340	810	—	—

$\Sigma n/N = 0.1103$

CONCLUDING REMARKS

The values of C for the damage law of Eq. 10 need not be interpreted as strict recommendations. The engineer may extrapolate other values from available data and judge its realism for his particular problem.

As previously mentioned, the wideband fatigue analysis is performed exactly as for the narrowband since fatigue life is identical for all spectral shapes of the same RMS level. This is a most interesting point if we consider that a wideband spectrum is composed of many narrowband elements. This may offer an unexplored area for the analytical study of random vibration and the mechanism of material fatigue.

ACKNOWLEDGEMENT

The author acknowledges the help and encouragement provided by H. Herman and D. B. Wolfe.

BIBLIOGRAPHY

1. S. Clevenson and R. Steiner, *Fatigue Life Under Various Random Loading Spectra*, NASA Langley Research Center, Hampton, Va.
2. Crandall and Mark, *Random Vibration*, (Academic Press, New York and London, 1963) p. 44.
3. Mil-Hdbk-5, *Metallic Materials and Elements for Flight Vehicle Structures*, Dept. of Defense, Washington, D.C.
4. Harris and Crede, *Shock and Vibration Handbook*, (McGraw-Hill, 1963) Vol. 2, pp. 24, 12.

A NEW LITHIUM DIFFUSION SYSTEM FOR SEMICONDUCTORS

A new lithium diffusion system, frequently used at the RCA Laboratories for fabrication of solid-state devices is described. Since lithium is highly reactive, diffusion must be made under extremely dry and clean conditions to minimize introduction of foreign particles into the semiconductor element. The system described is clean, dry, temperature-flexible and can be closely controlled.

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THE USE of interchanging lithium atoms in semiconductor devices (such as in solar cells, in flexodes or in thin-film[1] devices in general) has proved to be highly significant. For example, the earlier types of junction solar cells diffused with boron to form a P-junction on floating-zone silicon suffered serious radiation damage when used in outer space. Such cells with lithium atoms present in the structure,[2] however, are capable of self healing because of rapid movement of mobile Li ions into the imperfections caused by radiation. A uniform distribution of the Li atoms in the structure is therefore important in these types of devices. Silicon solar cells with lithium as the only junction material have been made. Such cells yield, at present, one half the power output of the boron-lithium solar cells first mentioned. They produced a steady output during a test period of 15 months.

A fairly sophisticated system has been developed that enables one to diffuse the Li atoms into the substrates with uniform distribution or to obtain P-N junctions by a gradient diffusion technique. The system is based on the use of 99.9% lithium metal, which is evaporated and diffused. A pre-cleaning and handling procedure of the metal is also included.

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Generally, lithium metal reacts rapidly in air at room temperature and increases its reactivity at higher temperatures. Therefore, thorough investigation and tests have been made to find the best possible enclosure material, atmosphere, evaporator, and jig material for the process. Very little reaction takes place if one uses argon gas as a blanket for molten lithium in combination with molybdenum jigs and fixtures. The lithium is melted in a steady argon gas flow and the vapor transmitted and diffused into the heated substrates. The argon gas is ideally suited for transporting the lithium vapor with very little reaction. There are two important variables available in the system:

(1) The evaporator temperature that determines the rate of evaporation, and
(2) The substrate temperature that determines the solubility of the lithium.

No apparent surface reaction takes place on the diffused substrates during and after the diffusion process. The substrates can be measured with a four-point probe immediately after the process without grinding or polishing the surface. Up to four 2 cm square by 1 mm thick wafers can be assembled in levels and processed in one operation. The diffused substrate assembly can be pulled out of the heated diffusion zone into the cool portion of the diffusion enclosure for annealing in lithium-argon atmosphere, or stored in a pure argon gas flow without exposure to air. Diffusions can be made at temperatures from 300°C up to 660°C for both silicon and germanium materials.

DESCRIPTION

The argon lithium diffusion system is shown in Fig. 1. The enclosure for the process is a 2-ft. long 1-in. diameter quartz tube vertically mounted inside a cylindrical 10-in. high 9½-in. diameter oven. The oven is fastened to a steel stand secured to the bench top. Also, the tube is fastened to the stand at the upper end. The oven, made of stainless-steel sheet metal is packed with fire brick insulation forming a cylindrical heat chamber 4-in. high with a 4-in. diameter. Six axially situated globar rods generate the heat for the 4-in. long substrate zone with negligible heat gradient in the zone. The long internal fore tube surface prevents unwanted contaminants from reaching the substrate during the diffusion.

The evaporator-gas-inlet assembly con-

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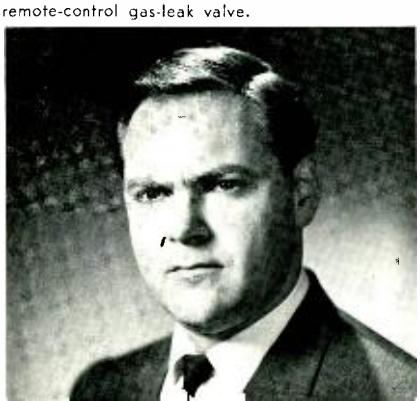


sists of 1) a "skirt" tube stem, and 2) a coated molybdenum evaporator used as the heater element for indirectly heating the molybdenum evaporator cup. The assembly is shown inserted into the lower quartz tube opening using a high-temperature rubber ring seal. The ¼-in. stem tubulation is connected to the argon gas source via a cold trap.

The upper tube opening air-tight seal has a 0.040-in. molybdenum wire able to slide axially in a high-temperature rubber support and a gas outlet connection leading to an air-trap. The substrate jig is attached to the molybdenum wire which can be lowered into the heated zone for diffusion or stored in the cool, protruding portion of the tube. The present system is operated manually using two rheostats for controlling the evaporator and the substrate heaters. It is important to dry the system's inclosure, jigs, and substrates before the actual diffusion takes place. It is also important to lower the dew-point of the argon gas by passing the gas through a cold-trap containing acetone and dry ice. The system is usually dried by turning on both heat sources to about 100°C for 10 minutes under a dry gas flow. Thereafter the heat sources are turned off and the jig is pulled from the heat zone and stored, as described earlier, with the gas flow remaining on.

CLEANING OF THE Li METAL AND SYSTEM OPERATION

The 99.9% lithium raw material used is shaped as a rod, ½-in. OD and 3-in. long and stored in an air-tight toluene container. A suitable piece of the metal, usually 40 mg. is cut directly from the rod in the container and transported into a metal beaker containing water-free (200 proof) alcohol. A relatively "slow" reaction takes place in the alcohol which removes the dark oxide layer on the metal and otherwise cleans the metal. When a silvery surface appears, the metal should be placed into the molybdenum evaporator cup in the diffusion system. Immediately after the lithium is placed in the cup, the heater is turned on to bring the temperature above the melting point of the lithium which is 186°C. Once it is melted and then cooled, no deterioration takes place and the system can be opened to air in the upper end for the removal or the changing of substrates a number of times without any reaction. This is done under constant gas flow with evaporator heater turned *off* each time.

UNIFORM HEAT DIFFUSION OF GERMANIUM AND SILICON

After drying, the gas flow is adjusted to 7 cm^3/min. and the diffusion is started. The dried substrates are lowered into the substrate zone and the heater element turned on. It takes about 5 minutes to stabilize the temperature which is monitored by thermocouples. A diffusion temperature of 500°C is usually selected, but temperatures from 300°C up to 600°C can be used. After the temperature is stabilized, the evaporator is turned on to 750°C and the diffusion takes place. The lithium diffuses relatively rapidly into the substrates. For example, a 2-cm square by 1-mm thick germanium wafer gives uniform Li distributions after 20 minutes, even when three such wafers are mounted in the jig. After such a diffusion period, a germanium wafer can change from 50 ohm-cm to 0.004 ohm-cm without an apparent surface reaction.

GRADIENT HEAT DIFFUSION OF GERMANIUM AND SILICON

A gradient diffusion differs from the diffusion described in the previous paragraph in that the highly soluble lithium atoms must be trapped in the substrate surface in a thin and uniform layer. A slightly different technique is used to obtain as narrow a junction as possible. When a ¼-in. square 0.020-in. thick silicon wafer is attached to a liquid cooled block (Fig. 2) good heat conductivity is established to one surface of the wafer while the other surface becomes heated by radiation. The assembly is lowered into the heated zone and diffused as described earlier. The lithium atoms will diffuse and remain in the radiation heated surface structure of the wafer depending upon three variables: the surface temperature, the circulation of the liquid, and the annealing. The sharpness of the established junction is therefore strongly related to the gradient heat in the substrate during the diffusion process. In the same manner, the yield of power from the finished fabricated cells is also dependent upon this process.

ACKNOWLEDGMENT

The author thanks Nissim Almeleh for his interest in the system developed, for his encouragement, and for adapting the system in his extensive research on germanium and thin film devices.

REFERENCES

1. Nissim Almeleh: Solubility and Precipitation of Lithium in Germanium, Bull. APS *12*, 390 (1967).
2. J. J. Wysocki: Lithium-Doped Radiation-Resistant Silicon Solar Cells, IEEE Trans on Nuclear Science *Ns-13* (6), 168 (1966).
3. J. J. Wysocki, P. Rappaport, E. Davison, R. Hand, and J. J. Loferski: Lithium-Doped Radiation-Resistant Silicon Solar Cells, Appl. Phys. Letters 9, No. 1 (1966).

Fig. 1—Lithium diffusion system.

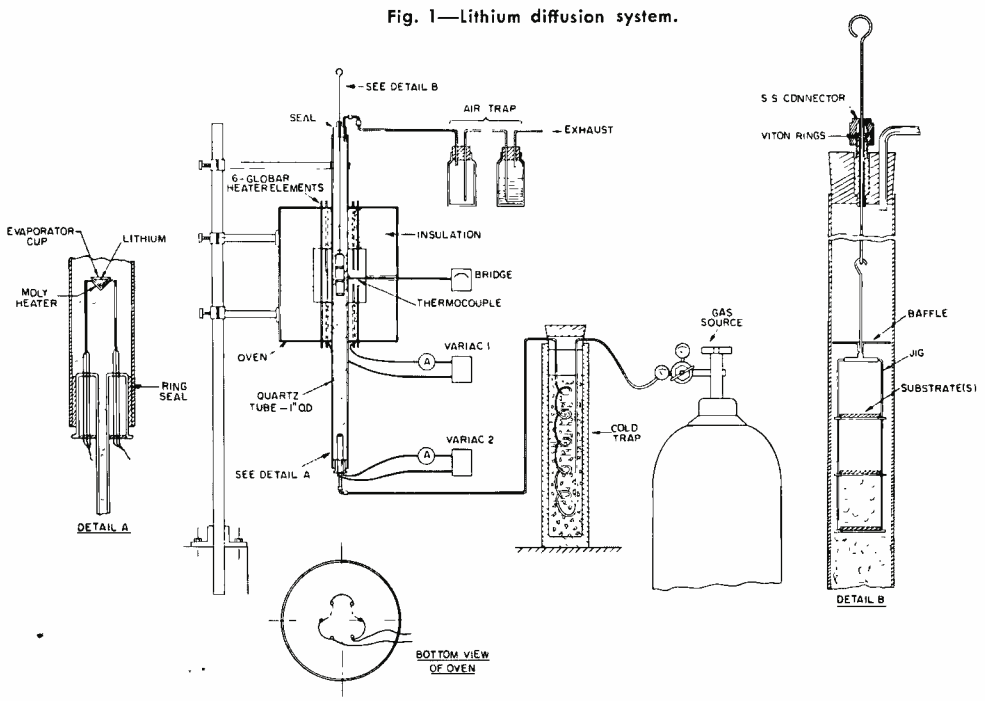
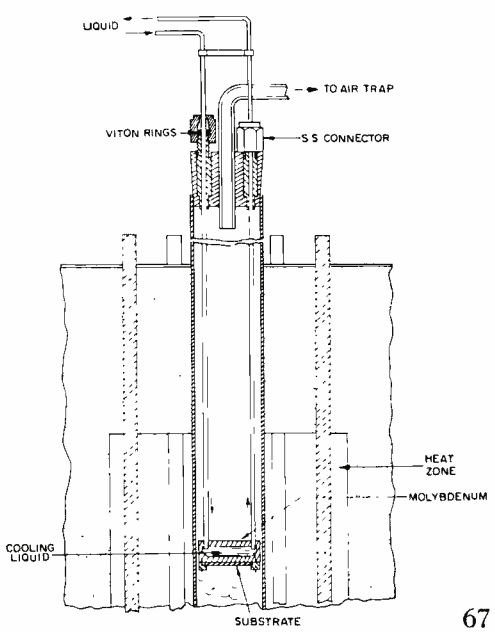


Fig. 2—Junction diffusion.



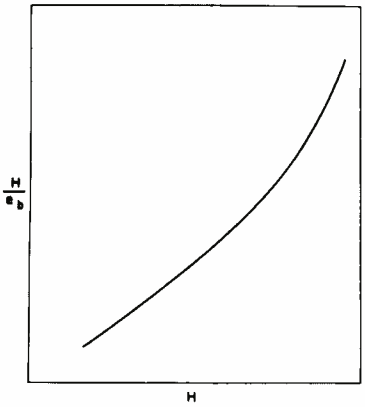


Fig. 4—Battery charge-rate-to-efficiency relationship.

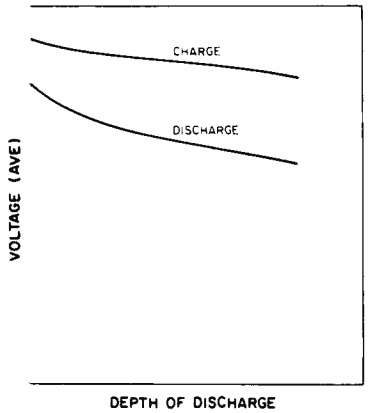


Fig. 5—Average battery voltage versus discharge depth.

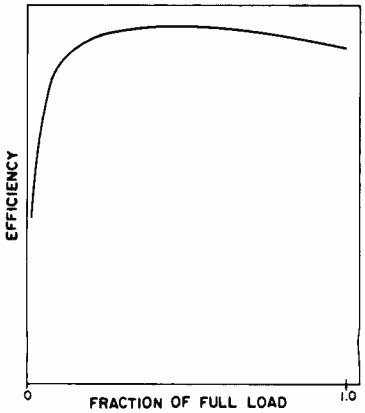


Fig. 6—Charge electronics efficiency versus load.

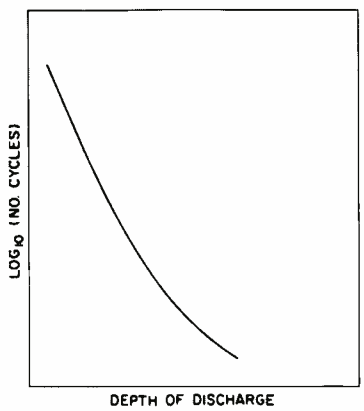


Fig. 3—Cycle life of a battery.

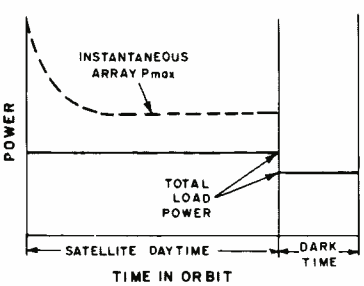


Fig. 2—Major power-time relationships.

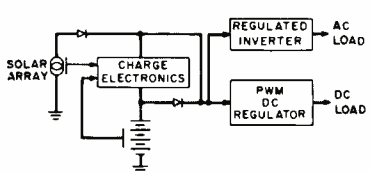


Fig. 1—Simplified block diagram of a space power system.

DESIGN OF A SPACE POWER SYSTEM BY COMPUTER

This article contains a description of a computer program used to perform space power systems designs, including sizing of storage batteries, solar cell arrays, and power conditioning. The purpose of the article is twofold: first, to serve as an illustration of an engineering task successfully accomplished through the combined efforts of design engineers and computer programmers; second, to stimulate interest in the particular problems tackled by a space power system design engineer. Contents of the article include a description of a typical photovoltaic space power system, parametric characteristics of its major components, design functions performed by the computer program with an emphasis on the engineering approach, and a numerical example of a typical computer solution.

PAUL NEKRASOV

Space Power Subsystem Design

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THE DESIGN of a space power system by computer is another outstanding example of application of the computer to the solution of complex engineering problems. The portion of a spacecraft that generates and distributes electrical power consists of a number of components of unrelated properties. Intermarriage of these components into an optimum spacecraft subsystem of the design quality demanded by present-day standards is a logical challenge to the current art of computer programming.

The discussion to follow offers an insight into the complexity of the design problems tackled by a particular computer program, written to perform parametric designs of multikilowatt power supplies for manned earth-orbiting applications under NASA Contract NAS-9-5266 (a conceptual study of a photovoltaic power system for an orbiting manned laboratory module). The program relies on vast amounts of stored component information and performs numerous operations, ranging from arithmetic to advanced decision-making.

Currently in FORTRAN II format, the program is run on the RCA 601 computer; approximate running time is less than ten seconds/solution. Fourteen standard IBM cards are required to completely define a set of mission requirements and machine instructions to initiate a solution cycle. All stored component data may be changed or up-dated as desired by the user. A complete solution is delivered as a printout of the input mission requirements, the system constraints selected by the program based on these inputs, the intermediate results of interest, and the final results of the computation performed.

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PAUL S. NEKRASOV received the BSEE in 1953, and the MS in Physics in 1955 from the Virginia Polytechnic Institute. Upon graduation, he joined the General Electric Company where he became a member of the advanced training program. He was with the IT&T Laboratories between 1956 and 1959, where he was engaged in several radar, missile guidance, and test range instrumentation programs. Upon joining the Astro-Electronics Division of RCA in 1959, he participated in computer systems studies and then joined the space power department in 1960. Mr. Nekrasov was responsible for the power systems analysis of several space programs such as Nimbus, Tiros, Relay, Ranger, and Lunar Orbiter. He is the author of a number of technical papers and studies of space power systems involving both conventional and advanced techniques.

DESCRIPTION

In general terms, the program logic applies to space power systems consisting of a source of energy, such as a solar-cell array, storage batteries, and power-conditioning electronics utilizing pulse-width-modulation techniques. As such,

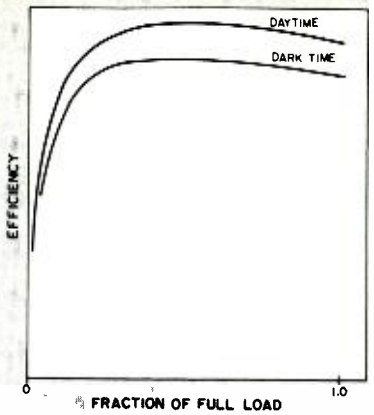


Fig. 7—PWM regulator efficiency versus load.

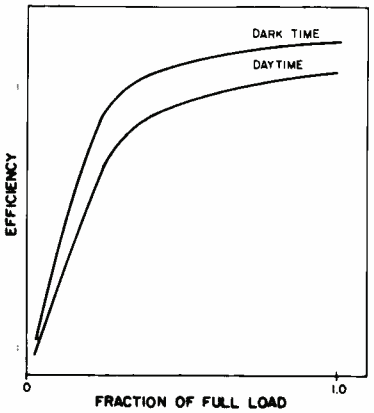


Fig. 8—Inverter efficiency versus load.

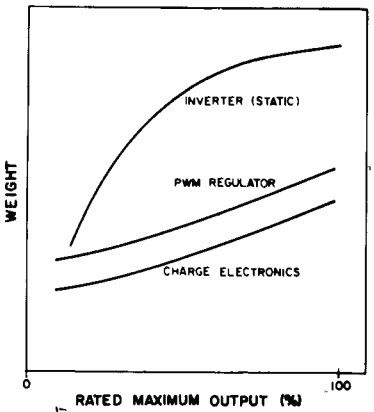


Fig. 9—Electronics weight.

it is applicable to a broad range of requirements, both current and future. A typical block diagram of a solar-array type of power system is given in Fig. 1. When the array is active, load power is supplied by the array through the regulators. Battery charge is accumulated through the charge electronics, which, in addition to its other functions, protects the battery by proper control of the charge current. During eclipse, load power is supplied to the regulators by the battery. The system can supply both AC and DC regulated loads. Special provisions included in the charge electronics enable the system to maintain a continuous match between the solar-array output and the combined load by operating the array at its maximum power point. Fig. 2 illustrates a typical load profile, as well as the instantaneous variation of the array maximum power magnitude as a function of time in orbit.

The computer program under discussion has been modeled after the block diagram configuration and the load profile variation shown. The primary objective is to establish valid quantitative relationships between the major components of the power system, for a set of programmed mission input requirements that are as follows:

Orbit altitude,
Daytime and dark-time load and AC/DC load magnitudes,
Mission lifetime, and
Charged-particle flux.

In addition, several options can be exercised in the area of the specific component type to be used. Any mission inputs can be varied, individually or as a group, over a wide range in any desired steps, initiating a new solution each time. Each solution provides detailed numerical information regarding the major parameters of the entire system, as well as the operating parameters of its individual components (such as their number and rating) and the degree that the components would be stressed in actual flight. The accuracy of the computed solutions depends on the accuracy and validity of the component characteristics and of other stored data. Many of the individual functions performed by the program rely on calculated average values of component voltages, efficiencies, and other quantities. Stored information,

TABLE I—Stored Data

Classification	Data
Battery*	Cycle life versus depth of discharge d, Fig. 3. Maximum safe d. Maximum charge rate H (hours). Minimum H. Peak instantaneous H. H versus ampere-hour efficiency e_h, Fig. 4. Number of cells/battery. Charge and discharge voltage/cell, Fig. 5. Watt-hours/pound. Watt-hours/ft.^{3}
Electronics**	Maximum full load. Efficiency versus fraction of full load, Figs. 6, 7, and 8. Weight, Fig. 9. Weight/unit volume.
Solar Array	Maximum power/cell versus temperature and flux, Fig. 10†. Effective area/cell. Weight density (lb/ft^2).
Temperature	Solar cell temperature versus time in orbit and altitude, Fig. 11.
Obital	Fractional time in the sun, orbital period, and number of eclipses/year versus altitude, Fig. 12.

* Nickel-cadmium and silver-cadmium battery data stored.
** Charge electronics, inverter, and pulse-width-modulated regulator.
† High and low base resistivity solar-cell data stored.

TABLE II—Program Outputs (Typical Solution)

Component; Parameter	Computed Value
Battery	
Total capacity	611 Ah
Maximum number of cycles	5740
Discharge depth	16%
Average charge rate	5 h
Charge/discharge ratio	1.164
Packaged weight	2761 lb
Packaged volume	60.2 ft^3
No. of battery packs	5
Solar Array	
Power	15.29 kW, average 23.58 kW, maximum 14.49 kW, minimum
Area	1720 ft^2 (oriented normal to sun vector)
Weight	1279 lb
No. of 2-by-3 cm solar cells	249,228
Electronics	
PWM regulators (4); peak output (each),	1371 watts, DC
Inverters (2); peak output (each),	1370 watts, AC
Charge electronics (5); peak output (each),	40.7 A
Total weight	488.6 lb
Total volume	11 ft^3
Total Weight of Power System	4529 lb

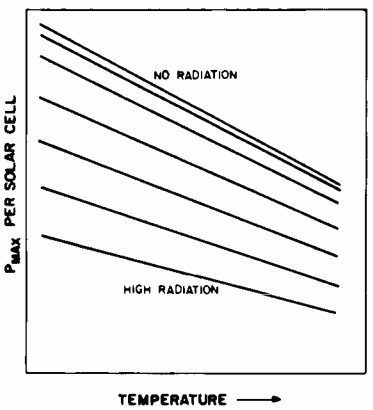


Fig. 10—Maximum power per cell versus temperature and irradiation level.

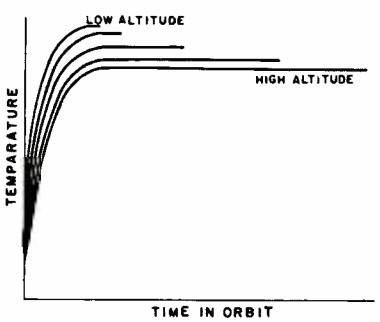


Fig. 11—Temperature-time profiles.

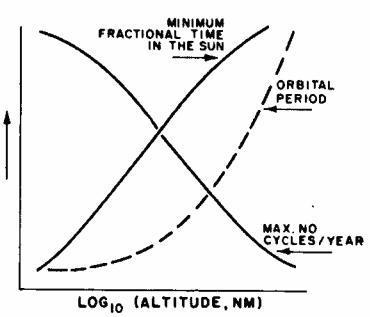


Fig. 12—Orbital characteristics.

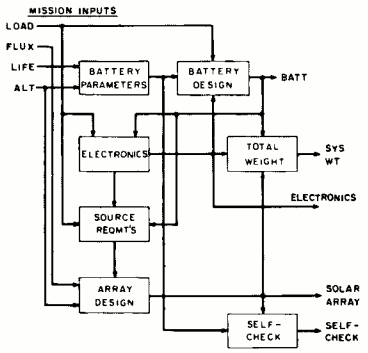


Fig. 13—Simplified flow chart of the program logic.

however. is basically raw component data not requiring a great deal of reduction to fit the program format; as such, it can be quickly and easily up-dated as the need arises. Required data is given in Table I, with references to Figs. illustrating the data format where stored data is other than a fixed number.

Table II is a list of selected parameters delivered as program outputs after each solution. Numerical quantities are given to illustrate the results of a specific solution corresponding to a 200-nautical-mile, 30°-inclination orbit, a nickel-cadmium battery system, low base resistivity solar cells, and a 5-kW load (plus 3.22 kW additional during daytime) with two-thirds of all loads delivered at DC voltage. Mission requirements included a one-year life.

MAJOR DESIGN FUNCTIONS

The following discussion covers briefly the details of the design logic performed by the computer program (Fig. 13). The program is described in terms of seven interdependent functions, with an emphasis on the engineering approach developed as a first step towards implementation of the design procedure in computer language.

Battery Parameters Function

The object is to determine the two significant operating parameters of the battery system. The first of these, the discharge depth factor, d, is a parameter related to the use of the battery in the discharge mode. It is determined by calculating d using two different criteria commonly employed: one is a function of the stored cycle-life data and the other is based on the maximum charge-rate limitation. The two calculated d values are compared with the stored value of the maximum safe d and the lowest of the three values is selected as the governing design parameter.

The second parameter is the average relative charge rate, H (hours), a descriptive parameter when the battery is under charge. Its numerical value is determined on the basis of the particular design limitation instrumental in the selection of d and the solution of certain algebraic expressions relating the charge rate to the orbital parameters and battery efficiency. The selected value is within the limits of minimum and maximum H.

Battery Design Function

Battery discharge (ampere-hours/orbit) is calculated based on dark-time load magnitude, discharge voltage, specific orbital parameters for the orbit altitude programmed, and appropriate electronics efficiency factors determined by the electronics function. This quantity is divided by the selected d to yield total battery capacity. Based on capacity, selected H, and weight/volume factors stored, the function determines the amount of the required average charge current, battery weight, and volume.

Electronics Function

This function is concerned with the definition of the pulse-width-modulated (PWM) regulator, inverter, and charge electronics. In general terms, the function analyzes the programmed load information and determines the maximum load requirements for each block. Given the stored maximum allowable load/unit, the number of units of a given type is then calculated. The program may, for example, determine that the number of individual PWM regulator units is four, paralleled together to satisfy peak load, with each regulator to be designed to a stated full-load requirement within the maximum per-unit load limitation dictated by component availability.

The establishment of the number and rating of the units of each type is followed by the calculation of their efficiencies. The efficiency factors are stored as a function of the percent of full load and, in certain cases, input voltage. In all, five efficiency factors are calculated: two each for the PWM regulator and inverter (one factor for daytime operation, and one for dark-time), and one for charge electronics. Weight and volume of all electronics is also calculated, including allowances for peripheral items such as telemetry, cabling, and harnessing.

Source Requirements Function

The orbit-average power to be delivered by the solar array is determined by this function. The required power equals the sum of the daytime load requirements and battery charge, referred to the array terminals. The load power component is found, using the programmed daytime load requirement and the calculated electronics efficiency factors; battery charge power is similarly found from the average charge current magnitude determined by the battery design function.

Array Design Function

Using the programmed mission inputs for the charged particle flux and altitude, the program selects the solar cell temperature/time variation and the per-cell power-output-versus-temperature characteristic appropriate to the conditions of the projected mission. From these, the orbit-average power/cell is found by time-integration of the instantaneous cell output. The average power/cell thus determined, and the output information of the source requirements function permits a calculation of the required number of solar cells, the total array area, and the weight of the array.

The array design function recognizes the peak-charge-rate limitation imposed by the batteries and automatically rejects excessive array energy not capable of being absorbed as safe charge. Following that, the number of cells (weight, area of the array) is adjusted to compensate for the energy rejected by initiating a series of iterative design cycles.

Minimum, maximum, and average array output, as well as the amount of array energy rejected (usually of the order of one percent) are also calculated and delivered as program outputs.

Self-Check and Monitoring Function

This function uses alternate methods of calculating certain quantities to lend confidence to the validity of the obtained systems solution. For example, the average charge rate H is calculated based on the array design performed by the program and compared to its required value determined by the Battery Parameters Function.

Total Systems Weight Function

Individual weights of the batteries, electronics, and solar array are added and the sum is delivered as program output.

CONCLUSION

Several hundred parametric designs of space power systems have been prepared by the use of the computer program described. Fast, accurate information has been made available to make engineering decisions on a short notice, and to perform detailed trade-off studies with a view toward minimum weight, the ultimate in reliability, the lowest possible volume, or another objective depending on the particular constraints imposed on the power system. It has also been possible to use the program in such a way as to define the range of missions that the power system can support, given a set of assumed hardware characteristics.

ACKNOWLEDGEMENTS

Participation of the entire technical staff of the AED Space Power Department is gratefully acknowledged, particularly the spirit of cooperation between the component and systems skill areas, which led to the successful design of this computer program.

THREE RCA MEN ELECTED IEEE FELLOWS

The three RCA men cited herein have been honored for their professional achievements by being elected Fellows of the Institute of Electrical and Electronics Engineers. This recognition is extended each year by the IEEE to those who have made outstanding contributions to the field of electronics.

ERVIN M. BRADBURD

Manager, Advanced Communications Technology
Communications Systems Division, New York, N.Y.

. . . for contributions to communication transmission systems and techniques.

ERVIN M. BRADBURD received the BSEE and MSEE from Columbia University in 1941 and 1943, respectively. From 1943 to 1954, Mr. Bradburd was with Federal Telecommunications Laboratory. For eight of these years, he was employed in a supervisory capacity, directing development and design of navigational aids, television transmitters, and PTM, radio-relay communication systems. He was responsible for the development of a standard line of VHF and UHF TV transmitters and for the design of the engineering model of the TACAN ground equipment. In 1954, he joined Olympic Radio and Television, where he was in charge of research and development of military electronic equipment. Mr. Bradburd joined RCA Communications Systems Laboratory in 1956. He was promoted to Manager, Advanced Communications Techniques, New York Systems Laboratory, in 1957. His group worked on the intrabase communications for BMEWS, the AN/GRC-50 radio relay set, and the Minuteman Hardened Communications System. From the Fall of 1959 through the Spring of 1961, he was responsible for the transmission design for the Unicom project under a joint RCA/PTL/ITT Program. Following this, he supervised communications R&D programs until mid-1964, when he was given the responsibility of the engineering effort on the VOCOM program. At the conclusion of the latter program, Mr. Bradburd was promoted to Manager, Advanced Communications Laboratory. He has since been promoted to Manager, Advanced Communications Technology. Mr. Bradburd is a member of Tau Beta Pi and was awarded the ILLIG Medal for scholarship upon his graduation from Columbia University. He holds nine patents and is the author of several papers on delay lines, TV transmitters, and satellite communications.

MAX H. MESNER

Manager, TV Cameras
Astro-Electronics Division, Princeton, N.J.

. . . for major contributions to the design of television cameras for spacecraft.

MAX H. MESNER received his BSEE degree from the University of Missouri in 1940, after which he joined the RCA Research Laboratories. He became associated with the Astro-Electronics Division of RCA upon its formation in March 1958. Mr. Mesner was responsible for the TV camera systems used in TIROS, and has directed the development of a number of miniaturized TV cameras including those for NIMBUS, RANGER, and APOLLO. Mr. Mesner's association with TIROS also included the responsibility for systems checking and environmental testing for the TIROS payload during the prototype phase of TIROS I. More recently he has been directing development effort in the field of very high resolution television for space missions. At the present time he is Manager, TV Cameras. As a research engineer on the technical staff of RCA Laboratories Mr. Mesner's research and development activity included radar indicators and pulse modulators, storage tubes and circuitry for both airborne and ground radar recording, and tube development for memories for digital computers. He was active in the development of color television from 1949 until 1958 where he contributed to the development of color television receiver encoders, special color cameras, and line-screen kinescopes and receivers using line-screen techniques. Mr. Mesner is a senior member of the IEEE, member of Society of Photo-Optical Instrumentation Engineers, a member of Sigma Xi, Tau Beta Pi, and Eta Kappa Nu. He holds 13 U.S. patents.

JOHN H. MULLER

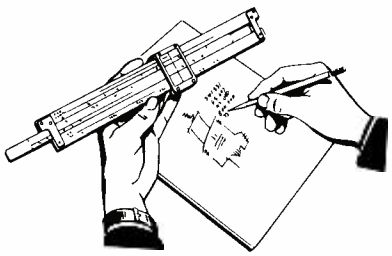
Vice President, Engineering Administration
RCA Communications, Inc., New York, N.Y.

. . . for contributions in extending radiocommunications to global telegraph and telephone systems.

JOHN H. MULLER attended the New York State Nautical School in 1920 and received the BS from Brown University in 1926. Mr. Muller joined RCA in 1926 as a student engineer. He served in engineering, construction, and operating capacities in various U.S. and overseas stations. He became Manager, Plant Valuation Division, in 1936. He became Assistant to the Vice President and Chief Engineer in 1942, and was appointed Assistant to the Executive Vice President in 1948. He was elected Assistant Vice President in 1952, and Vice President in 1953. He is a member of the Board of Directors of Marconi Telegraph-Cable Company. Since 1944, he has served on 12 U.S. Department of State delegations to International Telecommunications Conferences. From 1958 to 1960, he was on loan to RCA's Defense Electronics Products Division as Manager, BMEWS. In his present position as Vice President, Engineering Administration, he is responsible for the engineering administration related to all capital projects implementation. Mr. Muller is a Colonel, United States Air Force (Ret.), and a Trustee of Brown University. He was a Senior Member of the IEEE prior to becoming a Fellow. He is a member of the Veteran's Wireless Operators Association, Armed Forces Communications and Electronics Society, the Armed Forces Association, Reserve Officers Association, Brown University Club, the Merchants Club (New York City), and the Newcomen Society in North America.

Engineering and Research NOTES

BRIEF TECHNICAL PAPERS OF CURRENT INTEREST



Ternary to Decimal Conversion

A. Turecki
Palm Beach Operations
Electronic Data Processing,
Palm Beach Gardens, Florida

There exists a very simple algorithm for ternary (base 3) to decimal (base 10) conversion. The process used to accomplish this conversion is as follows:

1) Organize the ternary digits in groups of two, inserting zero at the most significant end if required.
2) Convert each two-bit group to its nonary (base 9) equivalent.
3) Select the most significant nonary digit, shift right one position, and subtract from the nonary number using decimal arithmetic.
4) Select the most and the next-to-the-most significant digit of the newly formed operand, shift right one position and subtract from the operand.
5) Repeat the above step increasing the subtractor by one digit each time.
6) The final subtraction occurs when the least significant digit of the subtractor is aligned vertically with the least significant digit of the operand. The result of the final subtraction is the decimal equivalent of the original ternary number.

Example:

	10 02 11 02	*Ternary*
	3 2 4 2	↓ *Nonary*
−	3	
	2 9 4 2	
−	2 9	
	2 6 5 2	
−	2 6 5	
	2 3 8 7	*Decimal*

The same principle can be used for converting a decimal number to its nonary and then ternary equivalent, but instead of subtracting, the consecutive selected portions should be added using radix nine arithmetic.

Example:

	2 3 8 7	*Decimal*
+	2	
	2 5 8 7	
+	2 5	
	2 8 4 7	
+	2 8 4	
	3 2 4 2	*Nonary*
	10 02 11 02	↓ *Ternary*

In the above conversion examples, the radices of the numbers differed by 1. In general, the procedure of conversion is the same but the shifted subtractor is to be multiplied by the differences of the radices.

Example (Binary to Decimal conversion, using 8 as a multiplier):

	1 0 0 1 1 1 0 1	*Binary*
−	8	
	2 0 1 1 1 0 1	
−	1 6	
	4 1 1 1 0 1	
−	3 2	
	9 1 1 0 1	
−	7 2	
	1 9 1 0 1	
−	1 5 2	
	3 9 0 1	
−	3 1 2	
	7 8 1	
−	6 2 4	
	1 5 7	*Decimal*

This algorithm was developed by the author in 1962 for his master's thesis, but his thesis advisor, Dr. M. Rubinoff, referred him to J. E. Croy's earlier report, "Rapid Technique of Manual of Machine Binary to Decimal Conversion" (IRE Transactions, Vol. EC-10, No. 4, 1961, p. 777) describing the same general principle. It is interesting to note that the algorithm has been reinvented recently by S. Hartmann (see "A New Method for Number System Conversion" in Computer Design, April 1967, p. 68).

Computer-Aided Selection of Test Points and Fault Isolation Procedures

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Advanced Systems and Technology
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Final manuscript received February 21, 1967.

Reducing the cost of maintenance with automation is increasingly emphasized by the Department of Defense. Consequently, much money and effort are being expended to develop automatic test equipment and fault isolation procedures.[1,2]

A next step is the computer-aided selection of test points and the automatic generation of the fault isolation procedure during the circuit design, so that test points are not limited to the normal circuit interface terminals.[3] Other techniques utilize only test points available for circuit operation and functional testing.[4,5,6] For simplicity and directness, the program considers only electronic components causing a detectable change in a test reading and assumes realistic failure modes. For use on present automatic test equipment, the program considers only voltage and impedance measurements between test points. The semiconductor models used are derived from those of Ebers and Moll[7,8] (Fig. 1) and are linearized whenever practical.

The program is in two parts: the algorithm for selecting test points and that for generating test procedure. The algorithm designates which circuit nodes are to be test points by these rules:

1) One test point on each bridge-type configuration;
2) A test point at the output of each stage;
3) A test point at the junction of three or more transistors;
4) No test point is selected that could adversely affect the operation of the circuit (for example, the base node of a transistor in the common emitter or common collector configuration).

The test procedure is then generated by an algorithm utilizing the concept of major and minor signal paths. The major signal path includes all components whose faults are easily detectable by a measurement between two test points. All other components are in a minor signal path of the test signal. The algorithm specifies three types of measurements:

1) Impedance between two points (usually DC resistance) where the major signal path is the minimum impedance path;
2) Gain between two points on the functional signal path, and the major signal path through the elements whose failure affects the gain;
3) Emitter bias voltages, where fault modes in certain transistors and other elements on the major bias path are detectable.

Analysis of a circuit requires a representation that can be manipulated. The admittance matrix is convenient to establish for com-

putation and easy to manipulate. Although the general admittance matrix is complex, it becomes real for DC.

For DC testing the program takes these component values for the matrix:

Resistors	$1/R$
Capacitors	A very small DC conductance
Inductors	A large DC conductance
Diodes and Transistors	Equivalent DC conductances for the passive parts.

As the diode and transistor nonlinearities are included in the current column matrix (Eq. 1) the conductance matrix is independent of operating points.

For AC tests the admittance matrix is complex. The real parts are the same resistor, diode, and transistor contributions while the imaginary parts consist of the usual capacitive and inductive susceptances (ωC and $-1/\omega L$). The general mixed set of circuit equations is Eq. 1, where $I_1, I_2, \cdots, I_L$ are known constants (independent current sources at these nodes), $I_m, \cdots, I_q$ are unknown currents, $V_1, V_2, \cdots, V_L$ are unknown voltages, and $V_m, \cdots, V_q$ are known.

$$\begin{bmatrix} I_1 \\ \cdot \\ \cdot \\ \cdot \\ I_L \\ I_m \\ \cdot \\ \cdot \\ \cdot \\ I_q \end{bmatrix} = \left[\begin{array}{ccc:ccc} Y_{11} & \cdots & Y_{1L} & Y_{1m} & \cdots & Y_{1q} \\ \cdot & & \cdot & \cdot & & \cdot \\ \cdot & & \cdot & \cdot & & \cdot \\ \cdot & & \cdot & \cdot & & \cdot \\ Y_{L1} & \cdots & Y_{LL} & Y_{Lm} & \cdots & Y_{Lq} \\ \hdashline Y_{m1} & \cdots & Y_{mL} & Y_{mm} & \cdots & Y_{mq} \\ \cdot & & \cdot & \cdot & & \cdot \\ \cdot & & \cdot & \cdot & & \cdot \\ \cdot & & \cdot & \cdot & & \cdot \\ Y_{q1} & \cdots & Y_{qL} & Y_{qm} & \cdots & Y_{qq} \end{array}\right] \begin{bmatrix} V_1 \\ \cdot \\ \cdot \\ \cdot \\ V_L \\ V_m \\ \cdot \\ \cdot \\ \cdot \\ V_q \end{bmatrix} \tag{1}$$

The upper portion of Eq. 1 may be written in partitioned matrix form, with each section named by the element in its lower right-hand corner.

$$[I_L] = [Y_{LL}]\,[V_L] + [Y_{Lq}]\,[V_q] \tag{2}$$

Solving for the matrix V_L from Eq. 2

$$[Y_{LL}]\,[V_L] = [I_L] - [Y_{Lq}]\,[V_q] \tag{3}$$

$$[V_L] = [Y_{LL}]^{-1}\{[I_L] - [Y_{Lq}]\,[V_q]\} \tag{4}$$

The vector $[I_L]$ includes the contributions of external current sources and the sources of the transistor. Since $[Y_{Lq}]\,[V_q]$ has the dimensions of current, the term within braces is more easily written as $[I']$ and considered as a current vector containing the contributions of current and voltage sources.

The equation for the voltages at nodes not connected to voltage sources may then be stated symbolically as in Eq. 5.

$$[V_L] = [Y_{LL}]^{-1}\,[I'] \tag{5}$$

The impedances and nodal voltages are computed for a fault simulation. The voltages $[V_L]$ are the values which would be measured in the circuit if the computer-simulated fault were an actual fault in the circuit.

The available computer memory space limits the maximum size of the admittance matrix, so the technique must be modified for larger circuits. The two basic approaches considered for treating large circuits are mathematical partitioning and "staging". Because mathematical partitioning requires secondary storage and extensive computation time, it has been abandoned in favor of staging.

In staging, the original circuit is divided into segments (stages), primarily on the basis of DC independence (i.e., stages are usually bounded by coupling capacitors). During the processing of a stage, the others are collapsed into a pair of two-port representations with proper input and output loading characteristics.

The transistor model chosen for this program is the Ebers-Moll representation. With the obvious simplification, it also represents diodes. Because of the low frequency of test signals, the diffusion capacitances were omitted. The model is otherwise that used in the NET-1 circuit analysis program. The large-signal models are linearized for small signals in the program while the Newton-Raphson iterative technique is used for non-linear equations. The required derivatives are obtained in closed form rather than numerically.

This is a promising beginning in the development of a general program to assign test points and generate the test procedures for fault isolation of electronic circuits. The present program has been applied to two circuits of 35 and 100 components. Although both were analog circuits, nothing in the technique precludes digital circuits.

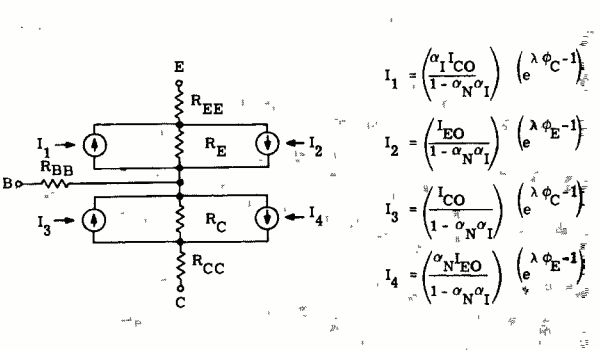
References

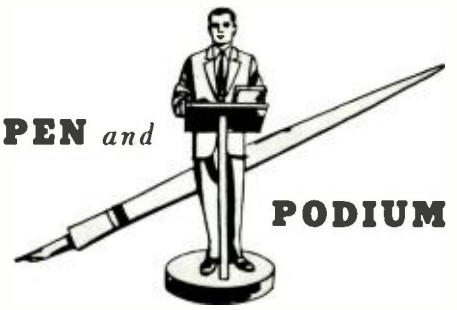
1. Mayper, *Problems and Pitfalls in Automatic Test Computer Programming*, Contract SETE, Contract NObsr 82988, New York University, School of Engineering and Science, Research Division, New York (May 1965).
2. Evanzia, "Automatic Test Equipment, A Million Dollar Screwdriver", *Electronics* (Aug. 23, 1965).
3. Maenpa, McBride, Stahl, *Investigation of Fault Diagnosis by Transfer Function Techniques*, ITT Kellogg Communications System, a division of International Telephone and Telegraph Corporation, Tech. Report AFAPL-TR-65-113 (Nov. 1965).
4. Barry et al., *Programmed Algorithm for Test Point Selection*, Contract No. AF 33 (615)-3033, Aerospace Systems Division, Radio Corporation of America, Burlington, Mass. (June 30, 1966).
5. Atwood, et al., *Mathematical Approach Leading to Optimum Automatic Test Techniques*, Aerospace Systems Division, Radio Corporation of America, Contract No. DA-36-039-SC-88546 (Nov. 30, 1965).
6. Buchsbaum, Mah, Hannon, *Investigation of Fault Diagnosis by Computational Methods for Microcircuits*, Univac Division, Sperry Rand Corporation, Technical Report AFAPL-TR-65-111 (Nov. 1965).
7. Ebers and Moll, "Large-Signal Behavior of Junction Transistors", *Proc. of the IRE* (Dec. 1954), pp. 1761-1772.

Parameters of the Ebers-Moll transistor model

I_1	$\dfrac{I_{EO}}{1-\alpha_N\alpha_I}(e^{\lambda\phi E}-1)$
I_2	$\alpha_N I_1$
I_3	$\dfrac{I_{CO}}{1-\alpha_N\alpha_I}(e^{\lambda\phi C}-1)$
I_4	$\alpha_I I_3$
I_{EO}	Emitter reverse saturation current
I_{CO}	Collector reverse saturation current
α_N	Forward current gain
α_I	Inverse current gain
λ	q/kT—Exponent multiplier which assumes a positive value for PNP and a negative value for an NPN transistor
q	Charge of an electron
k	Boltzman's constant
T	Temperature in degrees Kelvin
$\varnothing_E$	Emitter to base intrinsic junction voltage
$\varnothing_C$	Collector to base intrinsic junction voltage
R_C	Collector-base junction leakage resistance
R_{CC}	Collector bulk resistance + lead resistance + contact resistance
R_{BB}	Intrinsic base resistance
R_E	Emitter—base junction leakage resistance
R_{EE}	Emitter bulk resistance + lead resistance + contact resistance
C_{TC}	$\dfrac{R_1}{[V_{ZC}+\lvert\varnothing_C\rvert]^{N_E}}$ collector-base junction transition capacitance
C_{TE}	$\dfrac{R_2}{[V_{ZE}+\lvert\varnothing_E\rvert]^{N_E}}$ emittance-base junction transition capacitance
R_1	A constant
V_{ZC}, V_{ZE}	Contact potential associated with collector and emitter junctions
N_C, N_E	Grading constant associated with the collector and emitter junctions is $\approx$ 0.33 for a graded junction and 0.50 for a step junction

Fig. 1—Modified Ebers-Moll model





COMPREHENSIVE SUBJECT-AUTHOR INDEX

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ACOUSTOELECTRIC CURRENT SATURATION in CdS as a Fluctuation Process—A. R. Moore (Labs, Pr) ; *J. of Applied Physics*, Vol. 38, No. 5, 4/67

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GaAs AT MICROWAVE FREQUENCIES, Resonance Behavior of the Dielectric Constant of—R. D. Larrabee, W. A. Hicinbothem (Labs, Pr) ; *Applied Physics Letters*, Vol. 10, No. 12, 6/15/67

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TRANSIENT SPACE-CHARGE-LIMITED CURRENTS Including Diffusion—R. B. Schilling (Labs, Pr) ; *Solid State Electronics*, Vol. 10, 1967

VAPOR DEPOSITED SILICON DIOXIDE, Dielectric Defects in—J. T. Wallmark, D. W. Flatley (Labs, Pr) ; Electrochemical Soc. Mtg., Chicago, Ill., 10/15-20/67

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FAR INFRARED ABSORPTION MEASUREMENTS in the Region of the Non-Devonshire Lines in Alkali Halides Containing OH and OD Impurities—D. R. Bosomworth (Labs, Pr); *Solid State Communications*, Vol. 5, 1967

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OPTICALLY INDUCED Tm^{2+} IONS in Trigonal Sites in BaF—E. S. Sabisky, C. H. Anderson (Labs, Pr); *Physical Review*, Vol. 159, No. 2, 7/10/67

PHOTOSENSITIVITY and Minority-Carrier Tunneling in Silicon/Silicon-Nitride Structures—E. D. Savoye, R. Simon (ECD, Pr); Conf. on Photoelectric and Secondary-Electron Emission, U. of Minnesota, 8/29-30/67

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HANDHELD TACTICAL RADAR PROGRAM—R. A. Van Olst (MSR, Mrstn); IEEE Mtg., Columbus, Ohio; 10/18/67

REAL-TIME PULSE DOPPLER RADAR AMBIGUITY RESOLUTION, An Application of Invariant Imbedding Smoothing to—R. F. Pavley (MSR, Mrstn); 1967 National Electronics Conf., Chicago; 10/23-25/67; *Proceedings*

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SHORT-PULSE TARGET IDENTIFICATION, Some Notes on—S. M. Sherman, T. Murakami (MSR, Mrstn); Ground Identification of Satellites (GISAT) Symp. sponsored by ARPA, held at MITRE, 10/2-4/67; *Proceedings*

TIME AVERAGED RADAR CROSS SECTION OF THE MOON—R. S. Ruffine (Labs, Pr); *J. of Geophysical Research*, Vol. 72, No. 16, 8/15/67

WIDEBAND RADAR, Some System Problems in—S. M. Sherman (MSR, Mrstn); Ground Identification of Satellites (GiSat) Symp., sponsored by ARPA, held at MITRE, 10/2-4/67; *Proceedings*

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INSULATED-GATE FIELD-EFFECT TRANSISTORS in Oscillator Circuits—G. D. Hanchett (ECD, Som); WESCON, San Francisco, Calif., 8/22-25/67; WESCON Preprint, 8/67

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MOS-FET as a Product and AGC Gate—W. M. Stobbe (ECD, Hr); *RCA Ham Tips*, Oct.

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TV TRANSMITTER PERFORMANCE MEASUREMENTS AND PICTURE QUALITY, Correlation Between—T. M. Gluyas, W. L. Behrend (B&CP, Mdw. Lds.); IEEE Fall Broadcast Symposium, Sept. 23, 1967, Wash., D.C.

TELEVISION PROGRAMMING, The Use of Special Effects in—S. A. Barboun (B&CP, Cam) SMPTE Tech. Conf. Sept. 19, 1967, Chicago. Ill., and IEEE Broadcast Symp., Sept. 21, 1967, Wash., D.C.

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Vilkomerson, D. H. R. optics
von Philipsborn, H. properties, molecular
Wallmark, J. T. properties, chemical
Wallmark, J. T. properties, electrical
Waxman, A. electromagnetic waves
Waxman, A. solid-state devices
Weakliem, H. A. properties, molecular
Wehner, R. mathematics
Wehner, R. properties, atomic
Weinstein, H. computer storage
Williams, R. properties, chemical
Wojtowicz, P. J. mathematics
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Zaininger, K. H. circuits, integrated
Zaininger, K. H. radiation effects
Zaininger, K. H. solid-state devices
Zernik, W. properties, molecular

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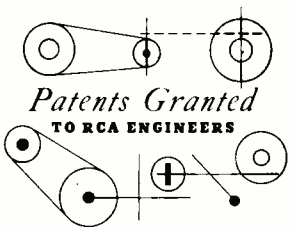
Bachynski, M. P. electromagnetic waves
Bachynski, M. P. plasma physics
Chisholm, K. G. television broadcasting
Gibbs, B. W. electromagnetic waves
Gibbs, B. W. plasma physics
Graf, K. A. antennas
Graf, K. A. plasma physics
Graf, K. A. electromagnetic waves
Jassby, D. L. antennas
Jassby, D. L. plasma physics
Komlos, S. G. spacecraft
Komlos, S. G. transmission lines

SYSTEMS ENG. EVALUATION & RES.

Barnla, J. D. space navigation
Breckman, J. space navigation

WEST COAST DIVISION

Levy, D. circuits, integrated
Paolantonio, A. control systems



As Reported By RCA Domestic Patents, Princeton

ELECTRONIC COMPONENTS AND DEVICES

High Power, High Frequency Transistor—H. Becke, E. F. Cave, D. Stolnitz (ECD, Som) U.S. Pat. 3,355,636, November 28, 1967

Cathode Ray Tube Screen with Color Areas of Differing Contours—D. J. Donahue, A. E. Harady (ECD, Lanc) U.S. Pat. 3,354,341, November 21, 1967

Wire Combing—J. Swyt (ECD, Hr) U.S. Pat. 3,352,331, November 14, 1967

Semiconductor Device—D. H. Rauscher (ECD, Som) U.S. Pat. 3,349,474, October 31, 1967

Low Dark Current Photoconductive Device—W. M. Kramer (ECD, Lanc) U.S. Pat. 3,350,595, October 31, 1967

Latched Ferrite Circulators—W. W. Siekanowicz, W. A. Schilling, I. Bardash (ECD, Pr) U.S. Pat. 3,350,663, October 31, 1967

Indium Doped Pickup Tube Target—R. L. Van Asselt (ECD, Lanc) U.S. Pat. 3,350,591. October 31, 1967

Electron Multiplier Dynode Having an Aperture of Reduced Secondary Emission—D. F. Battson (ECD, Lanc) U.S. Pat. 3,346,752, October 10, 1967

Transistor Protection Circuit for Radio Transmitter—S. J. Matyckas (ECD, Som) U.S. Pat. 3,345,570, October 3, 1967

BROADCAST COMMUNICATIONS PRODUCTS DIVISION

Electron Gun for Use in a Cathode Ray Tube Exhibiting Enhanced Electron Emission—J. W. Coleman (BCD, Cam) U.S. Pat. 3,355,618, November 28, 1967

System for Regulating Focus Current and Voltage in a Television Camera—W. J. Cosgrove (BCD, Cam) U.S. Pat. 3,355,621, November 28, 1967

Motion Picture Apparatus with Magnetic and Optical Sound Reproducing Means—B. F. Floden (BCD, Cam) U.S. Pat. 3,352,975, November 14, 1967

Counter Circuit—F. I. Johnson (BCD, Cam) U.S. Pat. 3,351,781, November 7, 1967

Phase Comparator Using Bistable and Logic Elements—R. R. Brooks (BCD, Cam) U.S. Pat. 3,328,688, June 27, 1967 (assigned to U.S. Gov't)

A.C. Meter Having Temperature Compensated Rectifiers Biased or Linear Operation—H. Groot (BCD, Cam) U.S. Pat. 3,329,896, July 4, 1967 (assigned to U.S. Gov't)

RCA LABORATORIES

Integrated Logic Arrays Employing Insulated-Gate Field-Effect Devices Having a Common Source Region and Shared Gates—J. W. Tuska (Labs, Pr) U.S. Pat. 3,355,598, November 28, 1967

Insulated-Gate Field Effect Triode with an Insulator Having the Same Atomic Spacing as the Channel—H. Johnson (Labs, Pr) U.S. Pat. 3,355,637, November 28, 1967

Memory Using Charge Storage Diodes—M. M. Kaufman (Labs, Pr) U.S. Pat. 3,355,720, November 28, 1967

Information Storage—J. R. Burns (Labs, Pr) U.S. Pat. 3,355,721, November 28, 1967

Light Frequency Shifter—D. J. Blattner (Labs, Pr) U.S. Pat. 3,353,896, November 21, 1967

Oxide Bonded Semiconductor Wafer Utilizing Intrinsic and Degenerate Material—J. A. Amick (Labs, Pr) U.S. Pat. 3,354,354, November 21, 1967

Element and Apparatus for Generating Coherent Radiation—Z. J. Kiss (Labs, Pr) U.S. Pat. 3,354,406, November 21, 1967

Associative Memory with Sequential Multiple Match Resolution—R. O. Winder (Labs, Pr) U.S. Pat. 3,354,436, November 21, 1967

Cryoelectric Circuits—R. A. Gange (Labs, Pr) U.S. Pat. 3,354,441, November 21, 1967

Signaling Loop Including Railroad Tracks—G. W. Gray (Labs, Pr) U.S. Pat. 3,353,018. November 14, 1967

Parametric Subharmonic Oscillator—J. C. Miller, A. W. Lo (Labs, Pr) U.S. Pat. 3,351,771, November 7, 1967

Computer System Employing Specialized Instruction Execution Units—S. Y. Levy (Labs, Pr) U.S. Pat. 3,351,918, November 7, 1967

Spin Wave Traveling Wave Amplifiers—B. Vural (Labs, Pr) U.S. Pat. 3,350,656, October 31, 1967

Flexible Logic Circuit Utilizing Field Effect Transistors and Light Responsive Devices—R. A. Powlus (Labs, Pr) U.S. Pat. 3,348,064. October 17, 1967

Electrostatic Recording Element—H. G. Greig (Labs, Pr) U.S. Pat. 3,346,381, October 10, 1967

Dark Current Reduction in Photoconductive Target by Barrier Junction Between Opposite Conductivity Type Materials—J. Dresner (Labs, Pr) U.S. Pat. 3,346,755, October 10, 1967

Raster Distortion Correction—W. H. Barkow (Labs, Pr) U.S. Pat. 3,346,765, October 10. 1967

Laser System Employing Means with No Moving Parts for Producing an Angularly Rotatable Beam of Coherent Light—H. R. Lewis (Labs, Pr) U.S. Pat. 3,344.365, September 26, 1967

Magnetic Shift Register—G. R. Briggs (Labs. Pr) U.S. Pat. 3,344,414, September 26, 1967

Magnetic Shift Register—G. R. Briggs (Labs, Pr) U.S. Pat. 3,344,415. September 26, 1967

Simple Method of Making Photovoltaic Junctions—S. G. Ellis (Labs, Pr) U.S. Pat. 3,340,599, September 12, 1967

HOME INSTRUMENTS DIVISION

Synchronous Demodulators—G. E. Kelly (HI, CH) U.S. Pat. 3,351,708, November 7. 1967

Color Demodulators—L. A. Cochran, J. A. Konkel (HI, Indpls) U.S. Pat. 3.351,709. November 7, 1967

Color Television Kinescope Ultor Voltage Regulator Utilizing a Voltage Dependent Resistor in the Control Grid Circuit of the Regulator Triode—A. H. Rickling (HI, Indpls) U.S. Pat. 3,350.599, October 31, 1967

Electrical Circuit Employing an Insulated Gate Field Effect Transistor Having Output Circuit Means Coupled to the Substrate Thereof—D. J. Carlson, G. E. Theriault (HI, Pr) U.S. Pat. 3,348,062. October 17, 1967

Regulated Voltage Supplies for Cathode Ray Tube Systems—J. Stark, Jr. (HI, Indpls) U.S. Pat. 3,346,763, October 10, 1967

FM Detector System Suitable for Integration in a Monolithic Semiconductor Body—J. Avins (HI, Som) U.S. Pat. 3,355,669, November 28, 1967

MISSILE & SURFACE RADAR DIVISION

Digital Storage and Generation of Video Signals—D. A. Cole, C. R. Corson, A. C. Stocker (MSR, Mrstn) U.S. Pat. 3,345,458, October 3, 1967

Cryogenic Analog-to-Digital Converter—C. J. Hughes, M. J. Campanella (MSR, Mrstn) U.S. Pat. 3,327,303, June 20, 1967

Antenna—E. O. Johnson (MSR, Mrstn) U.S. Pat. D209,147, November 7, 1967

ADVANCED TECHNOLOGY

Electronic Switching System Utilizing Delay Means for Switching Transient Elimination—J. T. Heizer, F. E. Shashoua (AT, Cam) U.S. Pat. 3,346.702, October 10, 1967

Electrostatic Printing Process Wherein Development is Achieved by Sequential Application of Carrier Liquid and Developer Particles—P. E. Wright (AT, Cam) U.S. Pat. 3,343,956. September 26, 1967

Helical Scan Transducer Apparatus Utilizing Time Sharing Head to Minimize Distortion during Edge Changeover—F. E. Shashoua (AT, Cam) U.S. Pat. 3,352,977, November 14. 1967

ELECTRONIC DATA PROCESSING

Flexible Type Mounts in High Speed Printing Machines—A. A. Sariti (EDP, Cam) U.S. Pat. 3,353,482. November 21, 1967

First Stroke Locator for a Character Reader—H. B. Currie (EDP, Cam) U.S. Pat. 3,349,372, October 24. 1967

Character Reader that Quandrantizes Characters—E. C. Ross (EDP, Cam) U.S. Pat. 3,348.200, October 17, 1967

Buffer—F. E. Brooks (EDP, Cam) U.S. Pat. 3,348,209, October 17, 1967

Lamp Driver Circuits—N. R. Stewart (EDP, Pennsauken) U.S. Pat. 3,346,770. October 10, 1967

Tape Reel Servo—G. V. Jacoby (EDP, Cam) U.S. Pat. 3,345,008, October 3, 1967

Magnetic Tape Cartridge Changing Mechonism—W. Deighton, A. G. Caprio (EDP, Cam) U.S. Pat. 3,343,687, September 26, 1967

AEROSPACE SYSTEMS DIVISION

Two Card Detector—L. W. Bleiman (ASD, VanNuys) U.S. Pat. 3,354,273, November 21, 1967

Slide Bearing Employing a Fluorocarbon Lubricant—A. Lichowsky (ASD. VanNuys) U.S. Pat. 3,350,143, October 31, 1967

Logic Gate Oscillator—W. Henn (ASD, Burl) U.S. Pat. 3,350,659, October 31. 1967

ASTRO-ELECTRONICS DIVISION

Vehicle Identification Apparatus—G. W. Gray (AED, Pr) U.S. Pat. 3.351,938, November 7. 1967

SEMICONDUCTOR DIVISION

Semiconductor Device Assemblage having Two Convex Tabs—P. C. Baumann (SD, Findlay, O) U.S. Pat. 3,355,635, November 28, 1967

Method of Stabilizing Semi-Conductor Devices having Exposed Suraces of a Hydrophilic Oxide—M. A. Polinsky, G. F. Damon (SD, Som) U.S. Pat. 3,352,712, November 14, 1967

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Diode-Capacitor Bit Storage Circuit—R. J. Clark (RCA Vic Ltd, Montreal, Can) U.S. Pat. 3,355.723, November 28, 1967

Ferroelectric Switching Circuits—E. Fatuzzo (RCA Labs Ltd, Zurich, Switz) U.S. Pat. 3,354.442, November 21, 1967

Ferroelectric Circuit Element Material and Transducer Utilizing Same—R. Nitsche (RCA Labs, Ltd, Zurich, Switz) October 17, 1967

NEW BUSINESS PROGRAMS

Substantially Linear Output Gage Device—W. R. Murphy (Industrial & Auto Prod, Plymouth, Mich) U.S. Pat. 3,344,527, October 3, 1967

Meetings

JAN. 16-18: **Reliability Symposium**, G-R, ASQC, et al, Sheraton Boston Hotel, Boston, Mass. **Prog. Info.:** V. R. Monshaw, Astro Elec. Div., RCA, P.O. Box 800, Princeton, N.J.

JAN. 25-27: **The Mathematical Association of America**, Fifty-first Annual Meeting, San Francisco Hilton, San Francisco, Calif. **Prog. Info.:** Harry M. Gehman, Executive Director, SUNY at Buffalo, Univ. of Buffalo, Buffalo, New York.

JAN. 28-FEB. 2, 1968: **Winter Power Meeting**, G-P, Statler Hilton Hotel, New York, N.Y. **Prog. Info.:** IEEE Headquarters, Technical Conf. Services, 345 E. 47th St., New York, N.Y. 10017.

FEB. 13-15, 1968: **Aerospace & Electronic Systems Winter Convention (WINCON)**, G-AES, L.A. Council, International Hotel, Los Angeles, Calif. **Prog. Info.:** IEEE Headquarters, 345 E. 47th St., New York, N.Y.

FEB. 14-16, 1968: **Int'l Solid State Circuits Conference**, SSC Council, Phila. Section, Univ. of Penna., Univ. of Penna. & Sheraton Hotel, Phila., Penna. **Prog. Info.:** R. L. Petritz, Texas Inst. Inc., P.O. Box 012, Dallas, Texas.

FEB. 28-MAR. 1, 1968: **Scintillation & Semiconductor Counter Symp.**, G-NC, U.S. Atomic Energy Comm., NBS, Shoreham Hotel, Washington, D.C. **Prog. Info.:** W. A. Higinbotham, Brookhaven Nat'l Lab., Upton, New York.

MAR. 18-21, 1968: **IEEE International Convention & Exhibition**, IEEE, Coliseum & N.Y. Hilton Hotel, New York, N.Y. **Prog. Info.:** J. M. Kinn, IEEE, 345 E. 47th St., New York, N.Y.

MAR. 27-28, 1968: **IEEE/ASME Joint Railroad Conference**, G-IGA, ASME, Conrad Hilton Hotel, Chicago, Illinois. **Prog. Info.:** IEEE Headquarters, 345 E. 47th St., N.Y., N.Y.

PROFESSIONAL MEETINGS

DATES AND DEADLINES

Be sure deadlines are met—consult your Technical Publications Administrator or your Editorial Representative for the lead time necessary to obtain RCA approvals (and government approvals, if applicable). Remember, abstracts and manuscripts must be so approved BEFORE sending them to the meeting committee.

APR. 3-5, 1968: **Int'l Magnetics Conference (INTERMAG)**, G-MAG, Sheraton Park Hotel, Washington, D.C. **Prog. Info.:** J. M. Lommel, Gen'l Elec. Res. & Dev. Ctr., P.O. Box 8, Schenectady, N.Y.

APR. 9-11, 1968: **International Symposium on Pulse-Rate and Pulse Number Signals in Automatic Control**, American Society of Mechanical Engineers. **Prog. Info.:** United Engineering Center, 345 E. 47th St. New York, N.Y.

APR. 9-11, 1968: **National Telemetering Conference**, G-AES, G-Com-Tech., Shamrock Hilton Hotel, Houston, Texas. **Prog. Info.:** IEEE Headquarters, 345 E. 47th St., New York, N.Y.

APR. 17-19, 1968: **Southwestern IEEE Conf. & Exhibition (SWIEEECO)**, Region , Houston Conv. & Exh. Ctr., Sheraton Lincoln Hotel, Houston, Texas. **Prog. Info.:** J. V. Leeds, Jr., Rice Univ., P.O. Box 1892, Houston, Texas.

APR. 23-26, 1968: **Cybernetics Conference, German Sec. of IEEE, DGK, NTG**, Munich, F. R. Germany. **Prog. Info.:** H. H. Burghoff, 6 Frankfurt Main 70, F. R. Germany, Stresemann Allee 2, VDE-Haus.

MAY 1, 1968: **The American Society of Mechanical Engineers, Automatic Control Division**, Winter Annual Meeting. **Prog. Info.:** Prof. R. E. Goodson, School of Mechanical Engineering, Purdue University, Lafayette, Ind.

MAY 5-9, 1968: **The Electrochemical Society**, Statler-Hilton Hotel, Boston, Mass. **Prog. Info.:** Electrochemical Society, 30 East 42nd St., New York, N.Y.

MAY 6-7, 1968: **Human Factors in Electronics Symposium**, G-HFE, Marriott Twin Bridges Motor Hotel, Washington, D.C. **Prog. Info.:** H. P. Birmingham, U.S. Naval Res. Lab., Code 5120, Washington, D.C.

JUNE 17-19, 1968: **The American Society of Mechanical Engineers**, Automatic Control Division, Third IFAC/IFIP Symposium on the State of the Art in the Use of Digital Computers in the Control of Processes, Systems, Machines, Toronto, Canada. **Prog. Info.:** United Engineering Center, 345 E. 47th St., New York, N.Y.

JUNE 20-21, 1968: **The American Society of Mechanical Engineers**, Automatic Control Division, Second Systems Engineering Symposium on Optimal Systems Planning, Cleveland, Ohio. **Prog. Info.:** United Engineering Center, 345 E. 47th St., New York, N.Y.

JUNE 26-28, 1968: **The American Society of Mechanical Engineers**, Automatic Control Division, JACC, University of Michigan, Ann Arbor, Michigan. **Prog. Info.:** United Engineering Center, 345 E. 47th St., New York, N.Y.

Calls For Papers

APR. 3-5, 1968: **9th Symposium, Engineering Aspects of Magnetohydrodynamics**, University of Tennessee Space Institute, ASME, IEEE, AIAA. **Deadline Info. (now) to:** L. E. Ring, Program Chairman, MHD Symposium, ARO, Inc., Arnold Air Force Station, Tennessee.

MAY 5-10, 1968: **SMPTE 103rd Technical Conference**, Century Plaza Hotel, Los Angeles, Calif. **Deadline Info.:** SMPTE Headquarters, Att.: 103rd Conference, 9 East 41st Street, New York, N.Y.

MAY 8-10, 1968: **Electronic Components Technical Conference**, G-PMP, EIA, Marriott Twin Bridges Motor Hotel, Washington, D.C. **Deadline Info.: 1/30/68 (papers) to:** F. M. Collins, Speer Res. Lab., Packard Rd., & 47th St., Niagara Falls, N.Y.

MAY 14-17, 1968: **Int'l Quantum Electronic Conference**, G-ED, G-MTT, JCQE, AIP, Everglades Hotel, Miami, Florida. **Deadline Info.: 1/8/68 (sum.) to:** R. W. Terhune, Ford Motor Co., Detroit, Michigan.

MAY 20-22, 1968: **Int'l Microwave Symposium**, Howard Johnson Motor Lodge, Detroit, Michigan, G-MTT. **Deadline Info.: 1/8/68 (abst. & sum.) to:** G. I. Haddad, Univ. of Mich., Dept. of E.E., Ann Arbor, Michigan.

JUNE 23-28, 1968: **Summer Power Meeting**, Sherman House, Chicago, Illinois, G-P, **Deadline Info.: 2/9/68 (papers) to:** IEEE Headquarters, 345 E. 47th St., New York, N.Y.

JUNE 25-28, 1968: **Conf. of Precision Electromagnetic Measurements**, Boulder, Colorado. **Deadline Info.: 2/12/68 (abst. & sum.) to:** Donald D. King, Aerospace Corporation, P.O. Box 95085, Los Angeles, Calif.

AUG. 27-29, 1968: **ACM National Conference and Exposition**, Las Vegas, Nevada. **Prog. Info.:** Marvin W. Ehlers Program Committee Chairman, Ehlers, Maremont & Co., 57 W. Grand Ave., Chicago, Illinois. **Deadline Info.: 3/1/68 (paper) to:** Marvin W. Ehlers.

Engineering NEWS *and* HIGHLIGHTS

NEW ENGINEERING APPOINTMENTS AT AED

C. S. Constantino, General Manager, Astro-Electronics Division recently announced the following appointments: **Dr. Richard B. Marsten,** Chief Engineer and **Dr. Warren P. Manger,** Manager, Advanced Systems and Technology.

Dr. R. B. Marsten

Dr. Marsten received the SB and SM in Electrical Communications in 1946 from the Massachusetts Institute of Technology, and the PhD in Electrical Engineering from the University of Pennsylvania in 1951. Since 1946, Dr. Marsten has worked as a research assistant, consultant engineer, and university professor. While associated with L.F.E., the Allen B. DuMont Laboratories, Polarad Electronics Corp., and Air Associates, his work was concentrated in the areas of microwave, communications, and display design and development. Upon joining RCA in 1956, he participated in a wide variety of successful programs in sophisticated radar design, and integration and application of advanced electronic techniques. Dr. Marsten has been with the Astro-Electronics Division since 1961. During this time, he was assigned the management responsibility for the Spacecraft Electronics Department. In 1964, this responsibility was expanded to include spacecraft camera systems and equipments. Dr. Marsten is an associate fellow of the AIAA, Chairman-Elect of its National Technical Committee on Communication Systems, and member of its Publications Committee. In 1966, Dr. Marsten as Program Chairman of the AIAA Communications Satellite Systems Conference, edited the book *Communications Satellite Systems Technology*. He was invited in 1967 by the National Academy of Sciences to participate in its space application study at Woods Hole where he served as deputy to the chairman of the panel on broadcasting. He is also a senior member of the IEEE.

Dr. Manger received an SB degree in Mechanical Engineering in 1943 and a PhD in Mathematics in 1949, both from MIT. Dr. Manger joined RCA as an engineering manager in 1958 at essentially the same time that the Astro-Electronics Division was formed. For the first few years he was responsible for thermal design, attitude control, and various system engineering aspects of the TIROS program. In 1960 he was given additional responsibilities for overall spacecraft systems engineering and design, including space power engineering, structural design, and materials engineering. His groups spearheaded the development of magnetic methods of attitude control, and later the Stabilite stabilization method-techniques which have played a key role in many AED spacecraft and in current projects. In 1965 Dr. Manger became Manager of Systems Engineering and Advanced Projects within the Engineering Department with responsibility for direction of systems engineering activities on proposals, studies, and hardware programs. Dr. Manger is a co-author of "Theory of Servomechanisms," (Chapter IV of Volume 25) of the *Radiation Laboratory Series.*

ABOUT THIS ISSUE

Our thanks go to **M. G. Pietz, J. Friedman, C. W. Sall,** and **G. D. Smoliar** for their efforts in the early planning, expediting, and coordinating of this issue of the RCA ENGINEER.

DR'S CHANG AND NICOLL NAMED FELLOWS AT LABS

Dr. Kern K. N. Chang and **Dr. Frederick H. Nicoll** have been named Fellows of the Technical Staff of RCA Laboratories, Princeton, N.J. In making the announcement, **Dr. James Hillier,** Vice President, RCA Laboratories, said the Fellow designation is comparable to the same title used by universities and technical societies. It is given by RCA in recognition of sustained technical contribution in the past and in anticipation of continued technical contribution.

LICENSED ENGINEERS

H. Russell, DEP-ASD, PE-21504, Mass.
D. J. Ettelman, DEP-AED, PE-10834, N.J.
C. F. Rose, HI, PE-12619, Indiana
W. R. Murphy, I&AP, PE-16336, Michigan
J. Cordora, DEP-AED, PE-002250E, Penna.

CONTENTS: DEC. 1967 RCA REVIEW

The RCA REVIEW is published quarterly. Copies are available in all RCA libraries. Subscription rates are as follows (rates are discounted 20% for RCA employees):

	DOMESTIC	FOREIGN
1-year	$4.00	$4.40
2-year	7.00	7.80
3-year	9.00	10.20

STAFF ANNOUNCEMENTS

By action of the Board of Directors of Radio Corporation of America at its meeting on November 2, 1967, **Robert W. Sarnoff** will become Chief Executive Officer of RCA, effective January 1, 1968. Mr. Sarnoff will continue as President and Chief Administrative Officer of RCA.

Robert W. Sarnoff, President, announced the following changes in executive responsibilities: **C. M. Odorizzi** is Senior Executive Vice President, Services, and is responsible for the RCA Service Company, RCA Communications, Inc., RCA Parts and Accessories, and the Hertz Corporation. **W. W. Watts** is Senior Executive Vice President, Defense and Commercial Systems, and is responsible for Defense Electronic Products and the Broadcast and Communications Products Division. **D. L. Mills** is Senior Executive Vice President, Consumer Products and Components, and is responsible for the RCA Victor Home Instruments Division, the RCA Sales Corporation, Electronic Components and Devices, the RCA Victor Distributing Corp., the RCA Victor Record Division, and the RCA Magnetic Products Division. **J. B. Farese** is Executive Vice President, Electronic Components and Devices, reporting to Mr. Mills. **J. R. Bradburn** is Executive Vice President, Information Systems, and is responsible for Electronic Data Processing, EDP Service, and the Graphic Systems Division.

W. W. Watts, Group Executive Vice President, announced that **A. K. Weber,** Vice President, will be on the staff of the Group Executive Vice President. In his new post, Mr. Weber will perform special assignments at the direction of the Group Executive Vice President, and in addition, will have responsibility for community relations activities in the greater Camden area.

W. W. Watts, Group Executive Vice President, appointed **I. K. Kessler** Division Vice President, Defense Electronic Products. Mr. Kessler will be responsible for the direction of the operating divisions and the staff of Defense Electronic Products.

W. W. Watts, Group Executive Vice President, appointed **J. M. Hertzberg** Division Vice President, International Communications Projects. Mr. Hertzberg will be responsible for planning and coordinating interdivisional product and systems programs in the communications field on a global basis.

I. K. Kessler, Division Vice President, Defense Electronic Products, announced the following appointments in Defense Electronic Products: **J. R. McAllister** is appointed General Manager, Aerospace Systems Division; **S. N. Lev** is appointed Division Vice President and General Manager, Communications Systems Division; **S. Sternberg** is appointed General Manager, West Coast Division.

H. J. Woll, Chief Engineer, Aerospace Systems Division, Defense Electronic Products, announced the following new appointments in the Engineering Department: **D. J. Cushing,** Manager, Systems Support Engineering; and **E. M. Stockton,** Manager, Automatic Test Equipment Engineering.

STAFF ANNOUNCEMENTS (con't)

P. E. Seeley, Manager, Advanced Systems and Technology, Aerospace Systems Division, Defense Electronic Products, announced the organization of the Advanced Systems and Technology Activity as follows:

E. Karnstein, Manager, Optical Physics Techniques; **R. B. Merrill,** Manager, Systems Development; **W. P. Peyser,** Manager, Microelectric Techniques; and **H. Logemann,** Manager, Sensor Techniques.

R. S. Holmes, Division Vice President, Medical Electronics, appointed **P. Greenberg** Manager, Product Assurance.

J. Hillier, Vice President, RCA Laboratories, Research and Engineering, announced the organization of the RCA Laboratories as follows: **A. N. Curtiss,** Staff Vice President, Administration; **H. W. Leverenz,** Staff Vice President, Research and Business Evaluation; **J. A. Rajchman,** Staff Vice President, Data Processing Research; **W. M. Webster,** Staff Vice President, Materials and Device Research; **A. A. Barco,** Staff Advisor; **L. R. Day,** Director, Special Development Projects; **K. H. Fischbeck,** Manager, Graphic Systems Applied Research Laboratory; **L. S. Nergaard,** Director, Microwave Research Laboratory; **K. H. Pawers,** Director, Communications Research Laboratory; **H. Rosenthal,** Manager, Technical Administration; and **C. P. Smith,** Director, Consumer Electronics Research Laboratory.

W. M. Webster, Staff Vice President, Materials and Device Research, RCA Laboratories, Research and Engineering, announced the organization of Materials and Device Research as follows: **G. B. Herzog,** Director, Process Research and Development Laboratory; **H. R. Lewis,** Director, Electronic Research Laboratory; **F. D. Rosi,** Director, Materials Research Laboratory; and **W. M. Webster,** Acting Director, Data Processing Applied Research Laboratory.

W. M. Webster, Acting Director, Data Processing Applied Research Laboratory, RCA Laboratories, Research and Engineering, announced the organization of the Data Processing Applied Research Laboratory as follows: **N. L. Gordan,** Head, Programming Research; **B. J. Lechner,** Head, Peripheral Equipment Research; **M. H. Lewin,** Head, Digital Systems Research; **D. A. Ross,** Head, Electronic Printing Research; and **R. A. Shahbender,** Head, Magnetic Memories Research (temporary assignment).

J. A. Rajchman, Staff Vice President, Data Processing Research, RCA Laboratories, Research and Engineering, announced the organization of Data Processing Research as follows: **S. Amarel,** Head, Computer Theory Research; **L. L. Burns, Jr.,** Head, Computer Optical Devices Research; and **R. A. Shahbender,** Head, Computer Digital Devices Research.

D. J. Donahue, Manager, Solid State and Receiving Tube Division, Electronic Components and Devices, announced the organization of the Solid State Operations Department as follows: **R. M. Cohen,** Manager, Special Engineering Programs; **R. J. Hall,** Manager, Solid State Signal Device Manufacturing; **R. L. Klem,** Manager, Operations Planning and Services; and **R. H. Pollack,** Manager, Solid State Engineering.

LES FLORY IS ED REP FOR MEDICAL ELECTRONICS

Leslie E. Flory has been appointed RCA ENGINEER Editorial Representative for Medical Electronics. Mr. Flory has been Chief Scientist with Medical Electronics since its formation earlier this year. Mr. Flory received the BS in Electrical Engineering at the University of Kansas in 1930. From 1930 to 1942, he was a member of the Research Division of RCA Manufacturing Company, Camden, N. J. In 1942, he transferred to RCA Laboratories Division, Princeton, N. J., continuing his work in TV pickup tubes, including image tubes and sensory devices. From 1964 to 1967, Mr. Flory was leader of the special systems research group of the AED Physical Research Laboratory. He has published numerous articles and has forty U.S. Patents. Mr. Flory is a Fellow of the IEEE; a Member of SMPTE; and is the Secretary General of the International Federation for Medical and Biological Engineering.

IEEE COMMUNICATIONS CONFERENCE

Preliminary plans for the 1968 IEEE International Conference on Communication were discussed recently by **David Shore,** Chief Engineer, DEP, and Chairman of the operating committee. Mr. Shore's committee includes **Jahn H. Gager,** General Electric, Treasurer; **T. T. N. Bucher,** RCA, Secretary; **Lewis Winner,** Consultant, Conference Manager; **Robert S. Carruthers,** IT&T Corp., Technical Program; **C. Raymond Kraus,** Consultant, Vice Chairman; and **Henry G. Sparks,** University of Pennsylvania, local arrangements.

Also on the committee are **Sol Zebrawitz,** Philco-Ford, IEEE Philadelphia Section; **Jaseph G. Mullen,** RCA, exhibits; **Richard Guenther,** RCA, Vice Chairman; **Edward A. Fasko,** G.E., international arrangements; **Jahn H. Gayer,** GE, Treasurer; **Haward A. Bond,** Philco-Ford, local arrangements; **C. Williamsan,** AT&T, banquet; **Amose E. Joel,** Bell Telephone Co., IEEE Comtcct Group and **M. Keith Wilder,** RCA, IEEE Philadelphia Section, are sponsor representatives.

The conference will take place on June 12-14, 1968, at the Sheraton Hotel in Philadelphia.

25th ANNIVERSARY OF THE TWT

On November 16, 1967, **Dr. Rudalph Kampfner,** one of the originators of the traveling-wave tube, was given a plaque commemorating the 25th anniversary of this occasion. This plaque was presented by the Microwave Tube Operations Department, Industrial Tube Division, EC&D, Harrison, N.J.—*H. J. Wolkstein*

ACHIEVEMENTS CITED

R. J. McEvoy, D. Staiman, R. D. Wattis, and **R. J. Wimberger** of the Missile and Surface Radar Division were cited for their performance during the second quarter of 1967. The four engineers and their wives were honored at a luncheon and received reference texts of their choice and desk plaques.

At the Astro-Electronics Division, **L. Freedman** was named Engineer of the Month for September, 1967, and **J. Fagan** was the Engineer of the Month for October. In addition to receiving a certificate and a check to be used to purchase technical books, these engineers and their wives were honored at a luncheon.

PROFESSIONAL ACTIVITIES

Aerospace Systems Division, Burlington, Mass. **Jahn S. Furnstahal** has been elected to the flight testing committee of the Aerospace Industries Association.

Arthur W. Sinkenson has been elected to the electronic materials and processes committee of the Aerospace Materials Division of the Society of Automotive Engineers.

Melvin M. Miller has been listed in the 1968-1969 edition of *Who's Who in the East.* This eleventh edition contains a list of biographies of those "Who contributed to the development of the Eastern United States or Canada."

Don Buch was on the service publications committee and program manager for the October 25-26 meeting of the AIA.—*D. B. Dobson*

Astro-Electronics Division, Princeton, N. J.

F. J. Yannotti has been appointed national chairman for the technical program on space environment for the Institute of Environmental Sciences. Mr. Yannotti is also the session chairman of the facilities design committee for the IES. **J. McClanahan** is the alternate session chairman of the facilities design committee. **D. Hartenbaum** was named the historian of the Mid-Atlantic chapter of the Institute of Environmental Sciences.

S. H. Durvani was appointed to the Educational Committee of the Princeton, N. J., section of the IEEE.—*S. Weisberger*

Broadcast and Communications Products Division, Camden, N. J. **H. S. Wilson,** Engineering Manager, Microwave Engineering, served as chairman for a panel discussion on "New Developments in Microwave Communications Systems."—*K. C. Shaver*

Henry M. Kozanowski was appointed to the Board of Governors representing the Eastern Region of the Society of Motion Picture and Television Engineers.

Communications Systems Div., Camden, N.J.

The EWS Session at the national meeting of the IEEE Industry and General Applications Group in Pittsburgh on October 3 took the form of a skit illustrating by bad example and humor how to make a good technical presentation. **Jim Lufkin,** of Honeywell, Inc., Minneapolis, wrote the playlet and also played the part of a Project Engineer. **Bab McGahey** of Westinghouse in Pittsburgh played a Chief Engineer; **Stan Higgins** of Westinghouse, Pittsburgh was an Editor, and **Wes Fields** of RCA, Camden, N. J., played a "nervous speaker."—*C. W. Fields*

Electronic Data Processing, Camden, N. J.

Paul Duke, Methods Analyst/Programmer, Engineering, gave an address on behalf of the Philadelphia Regional Blind Veteran's Association at a testimonial given to the President's Advisory Commission on Veteran's Affairs at the Sheraton Hotel in Philadelphia on September 23, 1967.—*G. D. Smoliar*

Graphic Systems Division, Dayton, N. J.

GSD has begun a series of courses in FORTRAN programming. The instructor is **Hugh W. Stewart,** Sr. Mbr., Tech. Staff. The first course provides engineers with a working knowledge of FORTRAN; the second, in January, is for administrative personnel, and the third, in March, is for persons with no prior familiarity with computers.—*J. Gold*

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FUTURE ISSUES

The next issue of the RCA Engineer emphasizes Broadcast and Communications Products. Some of the topics to be covered are:

New motion picture equipment
TV transmitters
Signal processing equipment
Mobile Communications equipment
Single-sideband techniques and equipment
Microwave relay systems
Improving automatic sensitivity in color TV film cameras

Discussions of the following themes are planned for future issues:

Graphic Systems and Devices
Automatic Testing
Man-Machine Alliances in Engineering
Electron Tubes: Conversion, Power, Color TV
Interdisciplinary Aspects of Modern Engineering
New RCA Computers
Laser Devices and Systems

° Technical Publication Administrators.

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