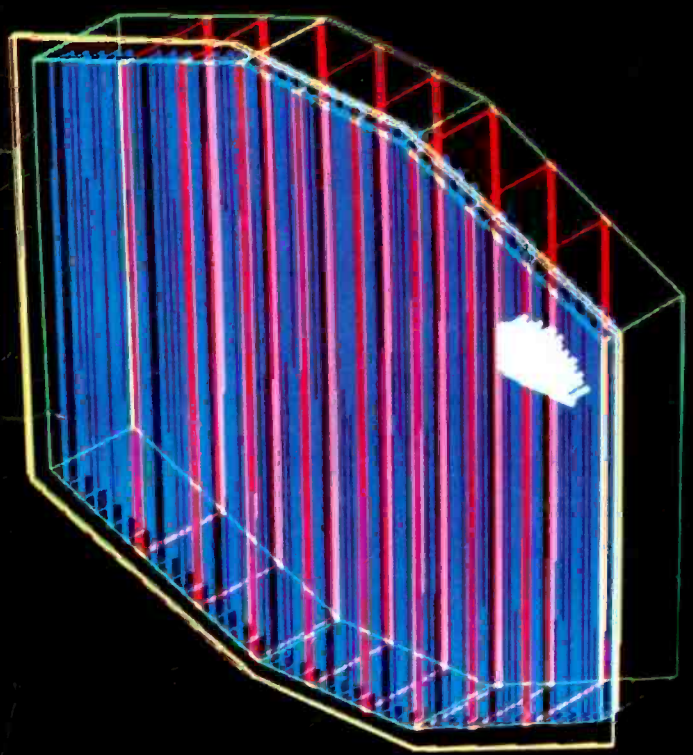
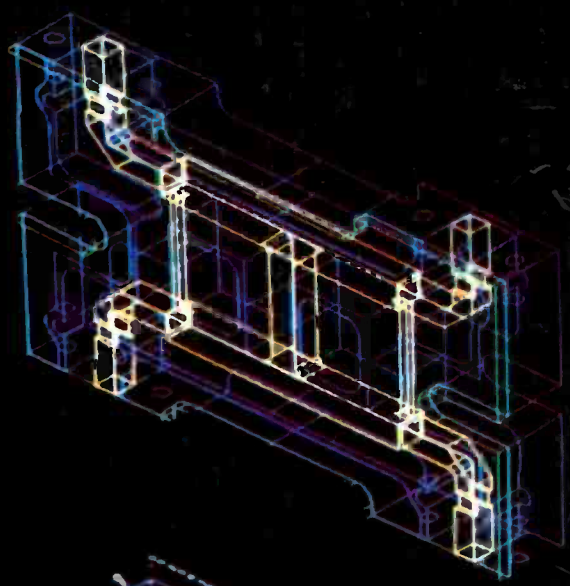
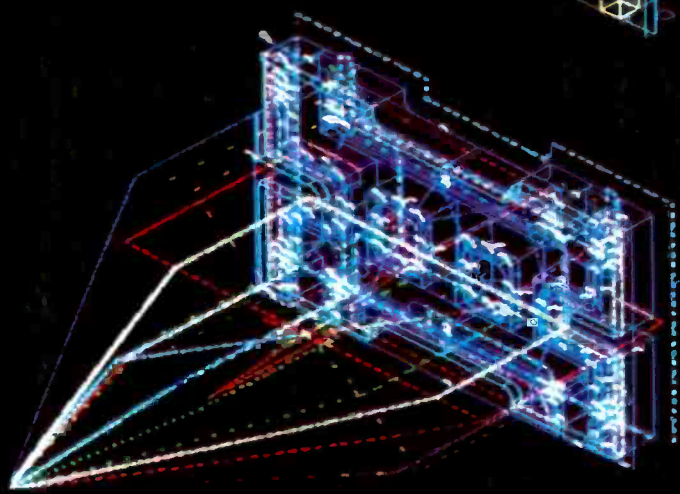
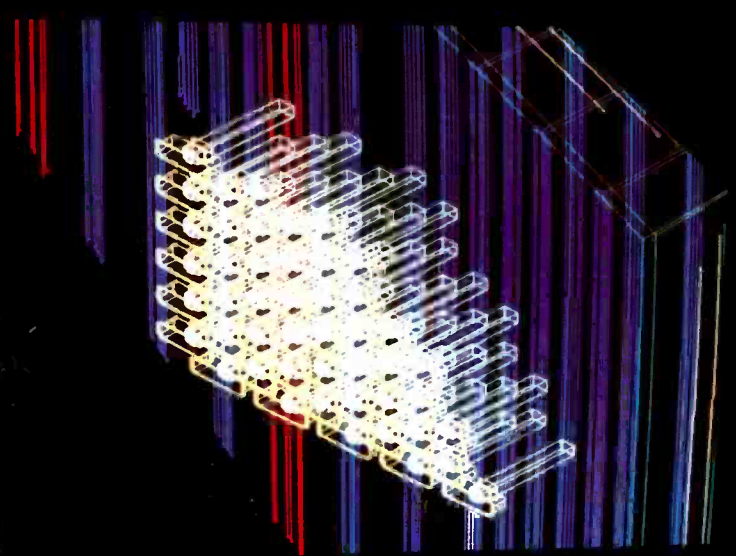
RCA Engineer

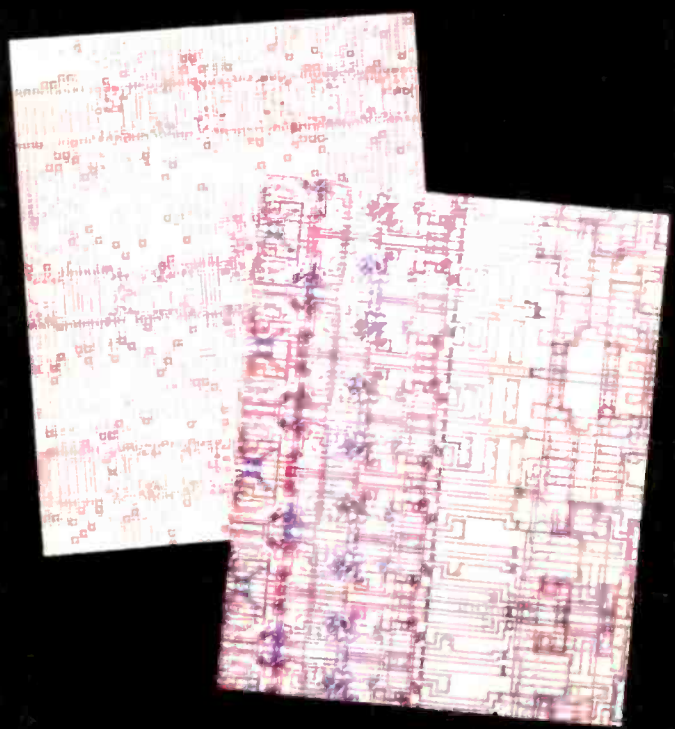
Vol. 26 No. 6 May/June 1981











CAD/CAM

Cover design by Louise M. Carr

Our front cover shows two types of CAD/CAM displays, one used in microwave design and production at Missile and Surface Radar, Moorestown, N.J.; the other, in LSI design.

At the upper left is an isometric view of the AEGIS EDM-4 antenna array face, phase shifters, main and secondary supports, outer shell, and mounting flange. A magnified isometric representation of the array face (lower left) reveals horns, phase shifters, and secondary stiffeners. At upper right is an isometric view of an assembled branchline coupler showing the cover as well as inner and outer conductors. Toolpath information is added to the branchline coupler outer conductor design in the center right display. The toolpath information is processed onto numeric control paper tape, which in turn, directs the Bridgeport CNC mill in the process of cutting the part. (For more information, see the article on pages 51-57.)

At the lower right, are two detailed drawings of LSI circuit layouts used by engineers to check the accuracy of computer-generated LSI layouts.

On the back cover, we show the subjective display results of the "light-to-light" computer simulation program for TV system design and evaluation, developed at RCA Laboratories, Princeton, N.J. (see pages 15-23).

RCA Engineer

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•To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

J.B. Feller

The computer-aided path to productivity

It is particularly appropriate that we address CAD/CAM in today's environment of ever-growing attention to productivity. I am sure each of us sees the computer in the hands of enlightened design and manufacturing engineers as one of the more obvious opportunities to improve productivity over the whole spectrum of our electronic business.

The computer is a powerful and versatile engineering tool. Tirelessly, with great speed and accuracy, it can calculate, simulate, or manipulate large volumes of data. The computer is one of the few commodities whose capabilities have been increasing and whose price has been decreasing. Thus, the productivity of the computer itself has vastly increased in the last 20 years. These facts have permitted engineers to increase the efficiency of doing traditional tasks and, more important, have opened the door to new horizons. One note: enthusiasm for using the computer must be tempered by the fact that the computer does not yet exercise judgment. We must continually apply judgment to ensure that our use of the computer is enhancing productivity.

One of the more exciting engineering applications of the computer simplifies the manufacturing-engineering interface. This innovation will permit more direct, error-free, and rapid contact between the engineer and his creation. It will give to the hardware engineer at least a portion of that direct creative experience available to the software engineer. The discipline of such techniques will also permit feedback to the engineer of cost-effective design rules and manufacturing methods.

I trust that you, as an ever-learning professional, will benefit by the ideas and reports in this issue of the *RCA Engineer*, and that you will continue to lead us to higher productivity and the benefits which that will bring.

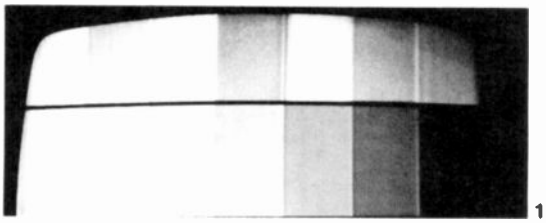
James B Feller

James B. Feller
Division Vice-President, Engineering
Government Systems Division

RCA Engineer
Vol. 26|No. 6 May|June 1981

in this issue...

Computer-aided design and manufacturing



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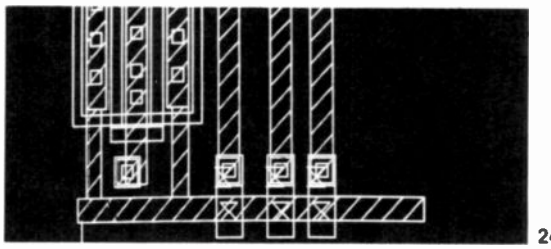
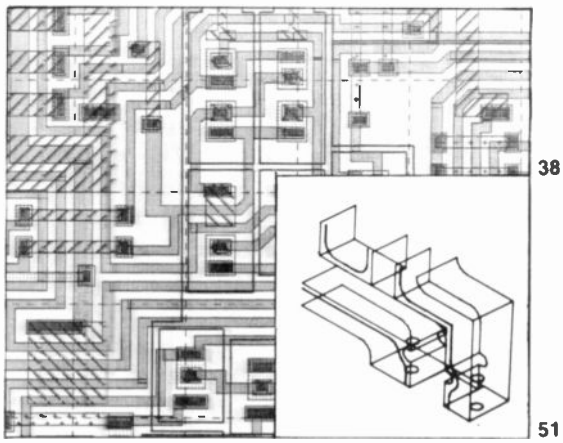


24

■ **Feller|Noto** CADDAS is considered a practical and cost-effective design approach for any activity about to incorporate custom LSI into its product line.

■ **Perlman** Selection of the best modification or circuit design change can be easily made without breadboarding all of the possibilities.

■ **Judice** At this moment, computer-aided design (CAD) is helping RCA deliver state-of-the-art products by reducing the time required to move ideas from the drawing board to the production line.



38

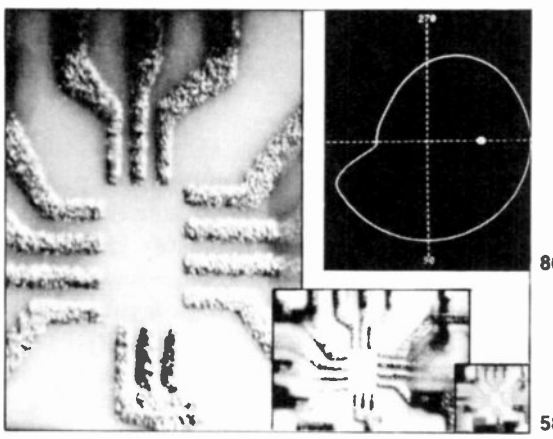
51

■ **Auerbach** The addition of a user-input language that allowed design rules to be specified in a simple and self-evident manner reduced the effort in mastering the program.

■ **Rifkin** Once the computer-aided design is finished, the MASK programs help a pattern generator or MEBES convert them into a set of masks for actual IC production processes.

■ **Borgini|Noto|Suskind** The heart of the AUA is the repetitive internal cells that are combined to form logic functions and then interconnected via a metallization pattern to produce a chip design.

■ **Wiegand** A design need only be entered once into a three-dimensional interactive computer graphics system. The need to recreate drawings and regenerate information is eliminated.



80

58

■ **Laskey|Wildenberger** Present manual inspection techniques require a microscope evaluation that economically limits the degree of inspection performed and results in operator fatigue.

■ **Peters** Over the past 12 years, the ATL Computer Center has developed a system of computer programs to produce wire-wrap and test equipment control tapes or cards from engineering inputs.

■ **Monat|Roberts** Most information was based on DL data but Engineering did not input the DLs to the database. It became apparent that if that were done, there were potentially many benefits.

■ **Reid-Green|Marder** By traditional methods, there was about a four-day cycle from inception through engineering drawing to completion.

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■ **Rosenberg** We at RCA have added to this vocabulary, our own CAD terms and equipment names, some of which are, of course, unique to specific RCA locations.

in future issues...

anniversary issue
microprocessor applications
SelectaVision® VideoDisc
manufacturing engineering
productivity

A.Feller|R. Noto

Fully automatic custom LSI design: Present and future

After fifteen years of success with the standard cell approach to making custom LSIs, RCA's family of automatic layout programs is still growing.

Abstract: *Following a brief review in this paper of the standard cell approach for generating random-logic custom large-scale-integration (LSI) devices, the status of various cell families is described. This includes operational, developmental, and experimental families. A description of the CADDA system follows. This is a minicomputer-controlled system which aids the user in executing all of the required programs by minimizing the quantity and types of input data that must be entered into the system. Completing the paper is a brief introduction to the fourth-generation (SMP2D) and fifth-generation (MACPAR) LSI and very-large-scale-integration (VLSI) automatic layout programs.*

About 15 years ago, the Advanced Technology Laboratories (ATL) of the Government Systems Division, with contract support, started the development of the standard cell approach for generating low-cost, quick-turnaround, custom large-scale integration (LSI). The first-generation automatic layout program — called Placement, Routing, and Folding (PRF)[1] — was developed to automatically lay out two-phase dynamic p-well metal-oxide-semiconductor (PMOS) logic. The second-generation automatic layout program, know as the Placement and Routing 2-Dimensional (PR2D) program, was developed by ATL with NASA support in 1969 for complementary metal-oxide-semiconductor (CMOS) static logic.[2] Several hundred custom LSI types were developed at RCA using this program, including about 55 for the GSD TENLEY and SEELEY programs.

In 1973, under an ERADCOM contract,[3] the multiport standard cell family was developed. This involved the development of a family of multiport standard cells and the development of a third-generation automatic layout program called the Multi-Port 2-Dimensional (MP2D) program. Except in rare instances, all new standard cell designs, whether CMOS/silicon-on-sapphire (SOS) or CMOS-bulk, now use the multiport approach. Within RCA the standard cell approach (the PR2D and MP2D automatic layout programs and their corresponding cell families) is often referred to as Automatic Placement and Routing, or APAR.

The standard cell approach

The RCA standard cell approach (also known as APAR) for generating random-logic custom LSI devices has been described several times in various publications.[4, 5] Therefore, only a brief summary of the standard cell approach will be presented here, emphasizing certain features followed by a discussion of recent developments and new capabilities.

This concept for the generation of LSI devices begins with the design, layout, and validation of a group of custom circuits, which are called standard cells because of their general building-block nature. Within the framework of the standard cell topology, all the inherent efficiency of handcrafted custom designs may be incorporated into these individual circuit cells. Once validated, the cells are given an identification number and permanently stored. To use these stored cells in a logic design, the user calls for them by their identification numbers. The computer retrieves the cell data from the stored library such that the individual cells are represented by a collection of polygons on the several mask levels. Other portions of the computer program automatically interconnect the standard cell circuits into the required functions.

It is characteristic of this approach that the interconnections will always be completed successfully by the automatic layout program. The low design cost and quick turnaround time result directly from this fact. Although the automatic layout capability will always provide a com-

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Final manuscript received Feb. 9, 1981.

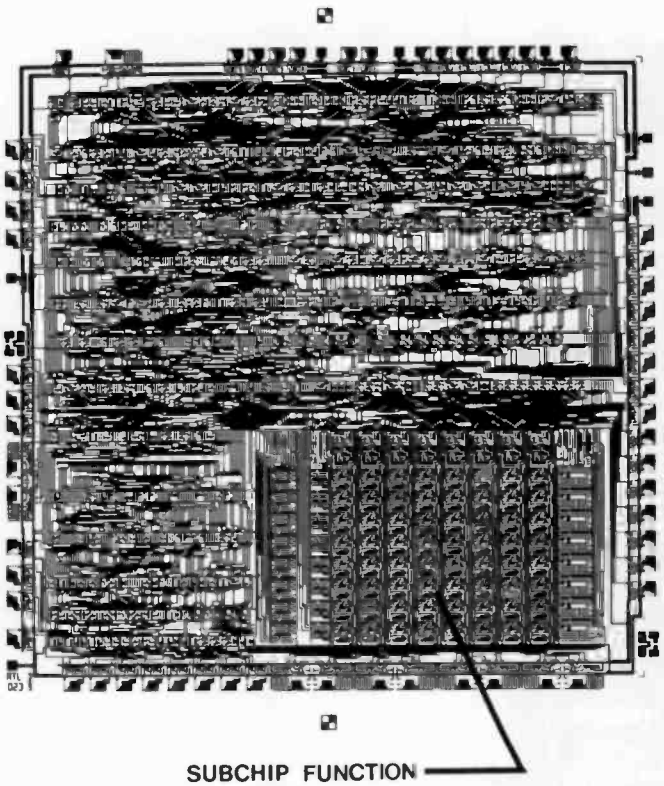

Fig. 1. Data path of ATMAC microprocessor.

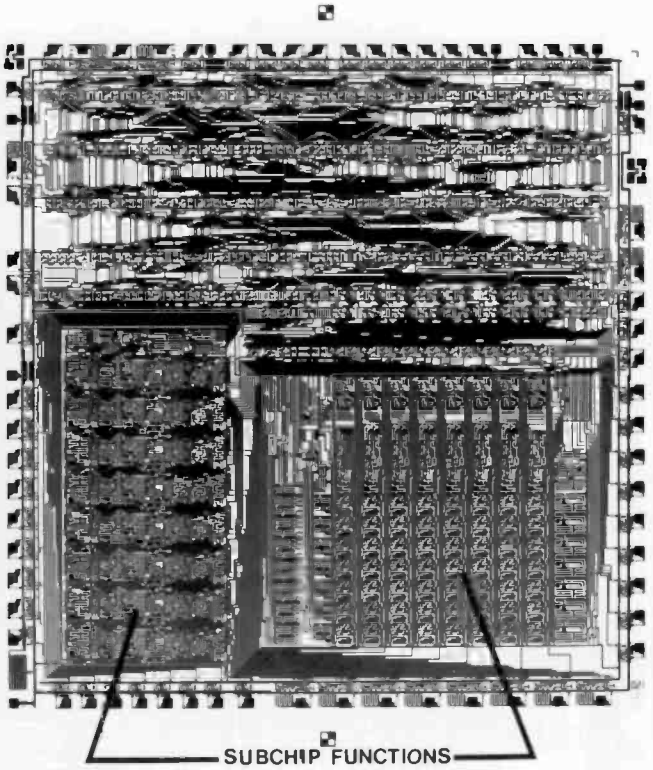

Fig. 2. Control chip of ATMAC microprocessor.

pleted layout, editing (as on an interactive graphics system) generally is done to optimize performance or to incorporate special or unique characteristics into the circuit. However, this is voluntary. The standard cell design capability will generate a layout ready for automatic fabrication, entirely free of human intervention.

Special performance capabilities

The original objective of the standard LSI design approach was to provide designers a low-cost, quick-turnaround LSI design capability. This remains one of the main objectives of the program. But — particularly in recent years — speed, performance, and device density have become equally important to system designers. As a result, various new performance and density capabilities have been incorporated into the automatic layout program and will be discussed in the following sections.

The subchip option

As previously stated, the automatic layout of random logic was the principal objective of the automatic layout programs. There are, however, many regular structures such as RAMs, ROMs, PLAs, PROMs, EPROMs, and register stacks that find many applications in digital systems. Because of their regular or repetitive structure, these functions are readily laid out by conventional handcrafted techniques, including layouts on interactive graphic terminals.

The subchip option[6] allows the standard cell automatic layout program to accept a functional design such as a RAM or a register stack, which may have been remotely designed by conventional handcrafted techniques, and to make all connections to it, automatically, while simultaneously generating an automatic layout for the remainder of the host chip. The net effect of incorporating the subchip option into the standard cell layout is to combine the high density and performance optimization associated with handcrafted designs with the low-cost quick-turnaround capability that the standard cell automatic layout program provides.

Illustrations of the subchip option are shown in Figs. 1 and 2 (a two-chip, 14-MHz, expandable, CMOS/SOS array microprocessor — the ATMAC). The subchip function,[7] shown in Fig. 1, which is the data portion of the microprocessor, is a multiread, multiwrite, 8 x 8 register stack. The remainder of the chip contains random logic that was automatically placed and routed by the automatic layout capability. The control portion of the microprocessor, shown in Fig. 2, contains two subchip functions. One is an 8 x 8 register stack, whose design differs from that in the data chip. The other is a 4 x 8 LIFO stack, which also contains the program counter.

Supercell

Another technique for achieving the high density and high performance of handcrafted functional blocks, but still using the automatic routing capability of the standard cell approach, is the concept of the supercell.[6] The supercell is a

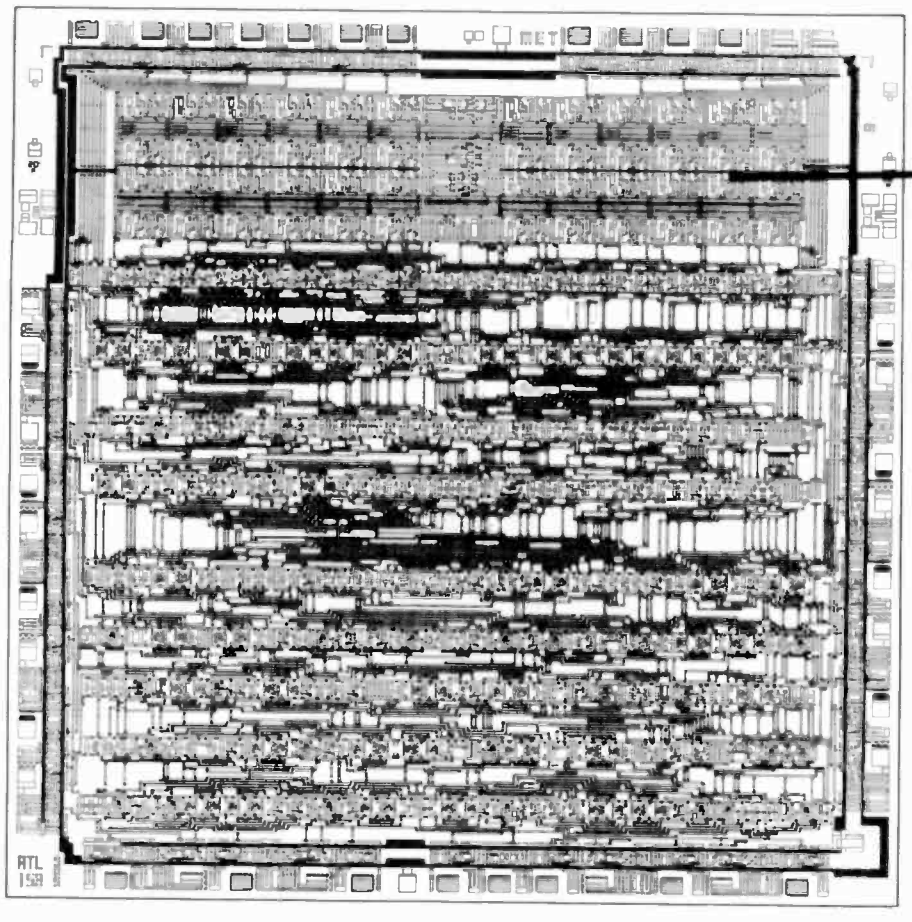

Fig. 3. CMOS/SOS version of 2910 microprogram sequencer.

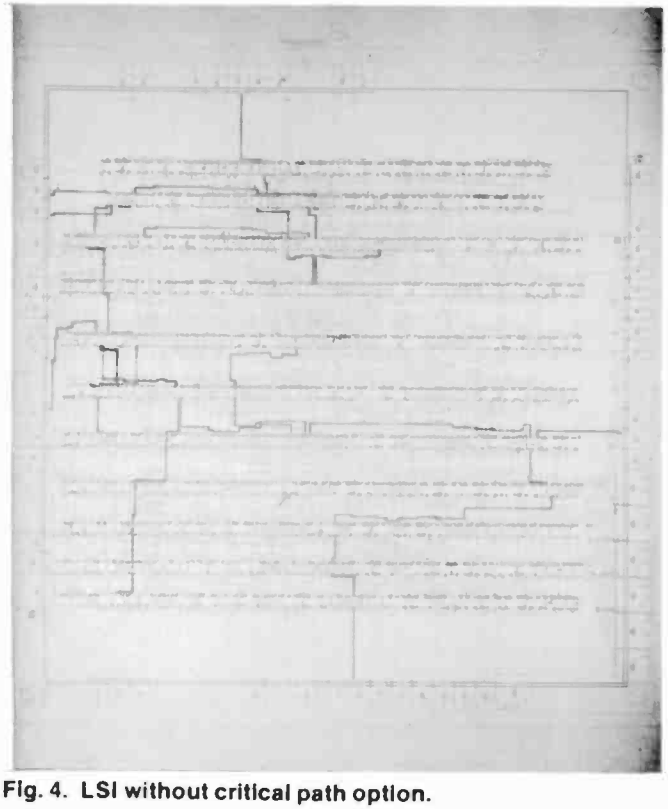

Fig. 4. LSI without critical path option.

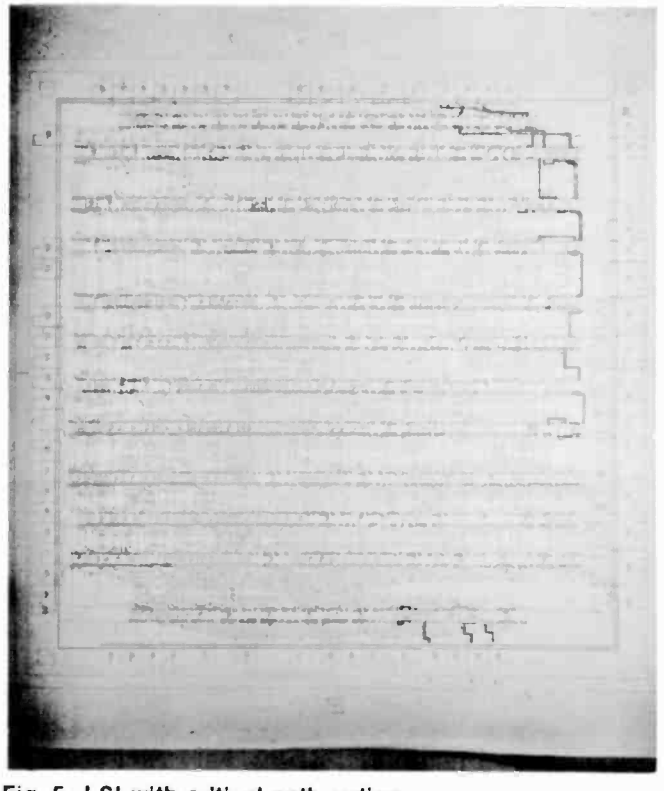

Fig. 5. LSI with critical path option.

circuit that is designed by handcrafted techniques which, while maintaining the same input/output relationship as any standard cell, provides a variety of special functions designed to enhance the performance of the LSI device. Although a supercell is treated as any other cell during the automatic routing phase, it can be designed with many unique properties.

An example of a supercell is shown in Fig. 3. This chip is a microprogrammable controller designed to support bit-slice microprocessors. The supercell, which occupies a full row across the top of the chip, is a 4 x 12 register stack. It is made of sections that are repeated across the face of the chip.

Critical path option

The critical path option[8] is a technique designed into the algorithms of the automatic layout program. The CPO minimizes the delay through paths identified by the user as critical. Under ordinary circumstances, the placement and routing algorithms will place all cells in the chip in a manner that minimizes total wire length and total cross-over (that is, it will seek to minimize the chip area). The routing algorithm will then generate the interconnections for the chip, emphasizing metal interconnects as opposed to the somewhat higher resistivity polysilicon interconnects. When the critical path is selected, the program will place those cells identified as part of each critical path not only as close to each as possible, but also in a manner to maximize the use of metal for the interconnections. Both of these actions will minimize the delay associated with the interconnection parasitics.

A typical illustration of the critical path option is shown in Figs. 4 and 5. These layouts are generated by the standard cell automatic layout program through identical input data, but with one exception. In Fig. 4, the critical path option was not exercised, while in Fig. 5, the critical path option was exercised. To indicate the actual impact of the CPO, several critical paths are identified in each layout. A visual comparison of these paths in each of the two layouts clearly demonstrates how the delays in those paths, identified as critical, are reduced as a result of the CPO option. In addition to the critical path option, several other techniques have been incorporated into the standard cell layout capability to maximize the operating speed of standard-cell-generated LSI devices.

Standard cell LSI and VLSI devices

Over the last several years, hundreds of LSI arrays have been generated using the standard cell approach. Over 500 CMOS/SOS and bulk-silicon chips have been designed by the standard cell approach. Many of these chip types were designed by the PR2D program, the predecessor to the current MP2D program. Although the PR2D automatic layout program is still available, it is recommended that the MP2D program be used for all new designs.

RCA's standard cell families

The current status of the standard cell families in RCA is contained in Table I. There are three categories — operational, developmental, and experimental. The operational cell families are those that are in current use. The developmental cell families are those that are in the design phase with a planned release in the near future

Table I. RCA standard cell families.

Status	*Name and Technology*	*Cell Height (Mils)*	*No. of Cell Types*	*No. of Chip Types*	*Comments (Discontinued or Non-Recommended Families Not Included)*
Operational	C^2L	12.6	>50	>15	≈6-micron SSTC + SSD Source — Compatible with then-current MP2D Program (APAR)
	SiGATE CMOS/SOS	4.2	>60	>40	6.25- and 5-micron channels — Two versions available MP2D (10-volt standard process)
	SiGATE CMOS/SOS	4.2	>45	8-10	4-micron channels, standard 700-Å process MP2D (10-volt, 5-volt)
	SiGATE CMOS/SOS Rad Hard	6.3	50	≈10	Rad. Hard. Process — specially designed circuitry, 5-micron channels, MP2D-compatible (10-volt)
In Development	CMOS Bulk Silicon Oxide Isolation	6.7	25	—	5-micron channels — now under development, multi-sourceable design rules available in mid-1981 MP2D (5-volt)
	SiGATE CMOS/SOS	2.8	30+	—	Advanced 3-micron cell family — eleven more circuits to be devleoped in 1981 being evaluated on test chip. Proposed next CMOS/SOS standard cell family (5-volt)
Experimental	CMOS Bulk Silicon Oxide Isolation	—	—	—	Advanced 3-micron channels, due in early 1982 (5-volt)

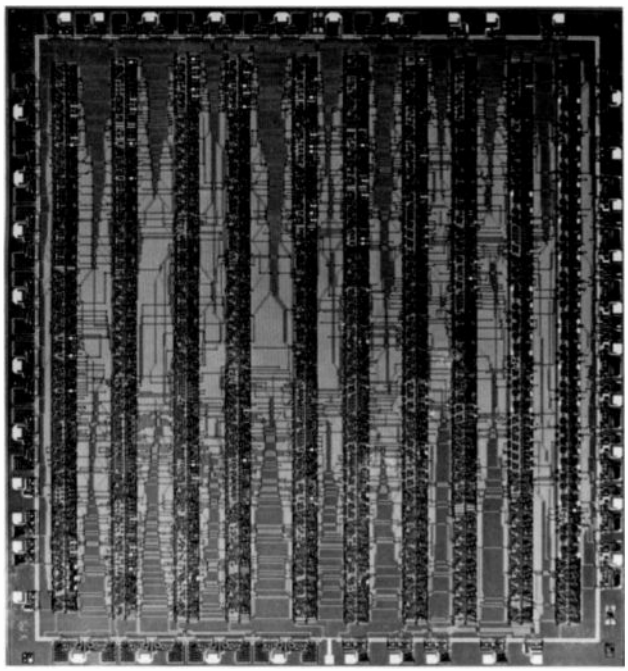

Fig. 6. C²L APAR LSI device.

(approximately one year). The experimental families are those whose release date is indefinite.

Operational cell families

12.6-mil C^2L (closed-geometry silicon-gate CMOS bulk silicon)

At present, this is the only operational bulk-silicon standard cell family that is compatible with the MP2D program. Its principal users have been SSD and SSTC, who developed the cell family primarily for industrial applications. An illustration of an LSI chip produced for an automotive application is shown in Fig. 6. It contains 6,250 transistors in an area of 290 x 270 mils for a device density of 12.5 mils^2/device.

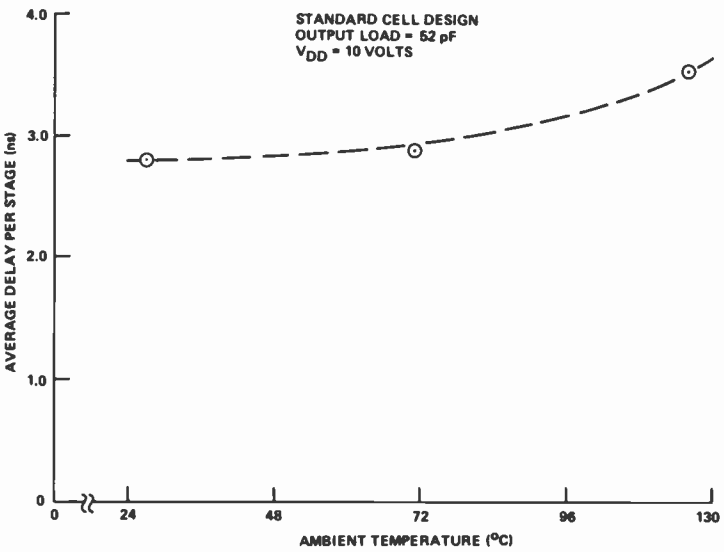

Fig. 7. Typical stage delay for four-micron CMOS/SOS cells.

4.2-mil silicon-gate CMOS/SOS 5- and 6.25-micron channel

These two cell families, which differ primarily in the channel dimension, were used in the design of more than 50 CMOS/SOS LSI devices. Most of the recent chip types used these families. However, once the Solid State Technology Center (SSTC) established the 4-micron, 700-Å process as a standard process, these families were replaced by still another version of the 4.2-mil CMOS/SOS families, the 4-micron version.

4.2-mil silicon-gate CMOS/SOS 4-micron channel

This version of the 4.2-mil families was especially developed to provide high-speed LSI arrays for the AEGIS program. Because of the narrow 4-micron channel and the requirement to operate at 10 V, SSTC reduced the gate oxide to 700 Å accompanied by the appropriate scaling techniques. Although, as in the case of the AEGIS program, this family can operate with a 10-V operating level, it is recommended for 5-V operation. This cell family is recommended for new LSI designs where the high speed of CMOS/SOS is required.

Figure 7 illustrates the performance that this cell family can provide. The figure shows the average stage delay versus temperature for one of the critical logic paths in the TCS208 Scalar chip, one of the standard cell LSI devices designed for the AEGIS program.[9] The delay at room ambient is less than 3 ns per stage. It should be noted that the scalar contains about 500 gates, small by today's standards. For the larger chips, there will be some performance degradation, but they will be in this range.

A 5-V application of this cell family is given in Fig. 8 and shows the "Formatter" chip, a device designed for the Modular Adaptive Signal Sorter (MASS) system being developed by GCS.

At present, the 4.2-mil 4-micron cell family contains 44 cells. With continued usage over the next few years, this family can be expected to increase to about 62 cells.

6.3-mil radiation-hardened silicon-gate CMOS/SOS cell family

This cell family[10] was specifically designed to produce radiation-resistant LSI devices that can perform normally in the presence of a 10^6 total dose accumulation and a dose rate in excess of 5 x 10^{12} rads/s. Achievement of these results required advanced circuit and processing techniques. SSTC developed a special radiation-hardened CMOS/SOS process while ATL developed special circuit and layout techniques. There are more than 65 cells in this well-documented cell family. At present, it is being used to design at least 19 LSI chips for the Fault-Tolerant Spaceborne Computer program. More than eight have already been designed. One of these chips is shown in Fig. 9. It is a 232 x 221 mil^2 chip containing 3517 transistors.

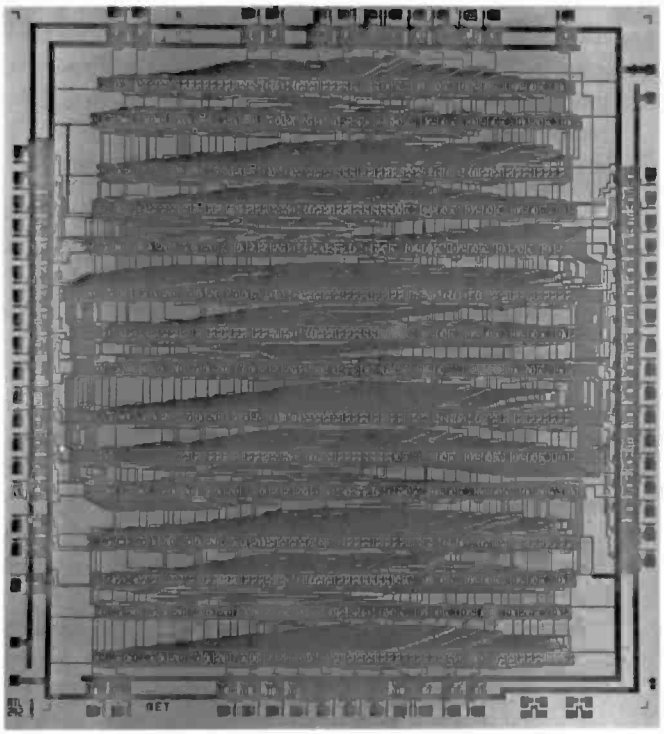

Fig. 8. CMOS/SOS formatter chip for MASS program.

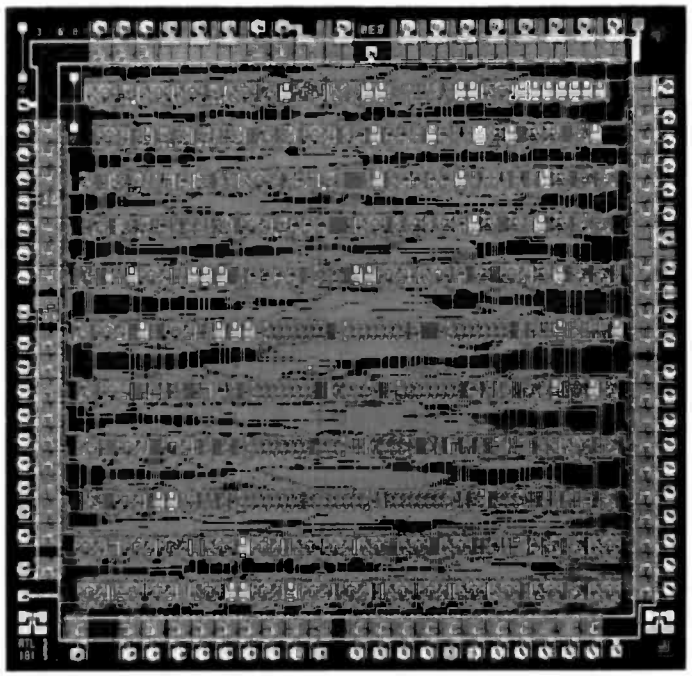

Fig. 9. ROM sequencer (232 x 221 mils, 3517 transistors).

Development cell families

2.8-*mil* (3-*micron channel*) *silicon-gate CMOS/SOS*

This cell family[11] was developed in a 1980 ATL IR&D program. Nineteen cells have been designed to date. Eleven more are scheduled to be developed during a 1981 IR&D program. The cells, which use a 3-micron gate length, are designed to provide high-density, high-performance LSI devices with a 5-V operating level.

Most of the 19 cell types have been incorporated into a special-purpose test chip, the TCS244, which is now in the fabrication cycle. Evaluation and characterization of the 2.8-mil standard cells are two of the many functions that the TCS244 CMOS/SOS test chip will provide. Figure 10 shows a 1129-transistor ALU that was generated by the MP2D automatic layout program using the 2.8-mil cell family. It is one of the many tests that were designed into the TCS244 test chip. Not including bonding pad area, this layout has a density of 3.64 mils^2/device. This is about a three-to-one improvement in density as compared to the most dense existing random logic CMOS/SOS standard cell LSI devices. Although there will be a decrease in density for the larger chips, the relative density advantage should remain.

In accordance with present schedules, this cell family should be conditionally released in the second half of 1981 based on SSTC evaluation and position on the design rules including the 3-micron gate length.

Lateral oxide-isolated silicon-gate bulk-silicon standard cell family

Recently the Solid State Division (SSD) introduced into their process line a new LSI, CMOS, silicon-gate, bulk-silicon technology[11] that will ultimately replace the closed-cell logic (C^2L) process as the principal LSI bulk-silicon technology. It achieves its high density because of new design rules and the use of oxide isolation that eliminates the area-consuming guard bands and field shields.

As part of its 1980 IR&D program, ATL initiated the design of a 6.7-mil-high MP2D-compatible (APAR) standard cell family using this process. Approximately 25 cells have been designed and partially checked. Changes had to be made in the MP2D algorithms to ensure program compatibility.

An approximate indication of the high density potential of this family can be seen in Table II. This table contains the

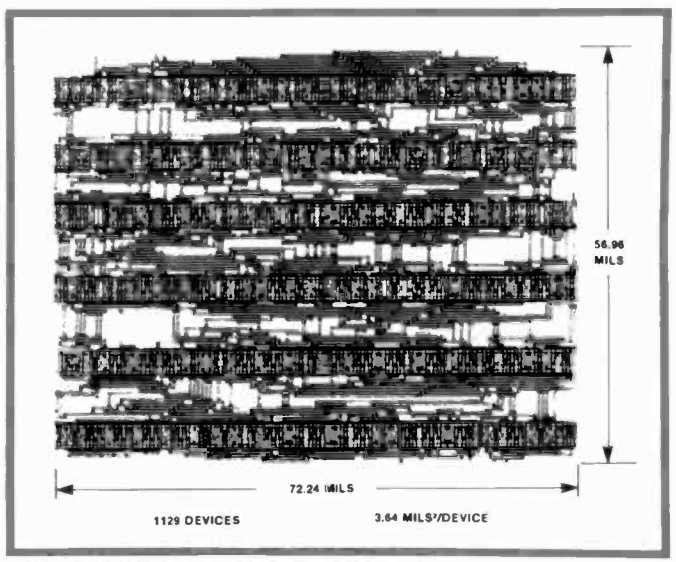

Fig. 10. Internal area of eight-bit ALU.

statistics on the MP2D layouts of several chip types using the C^2L and the oxide-isolated bulk cell families. In generating the layouts using the oxide-isolated bulk cells, the width of several cells not yet designed were approximated. In addition, certain patterns and cells, which ultimately must be included in the layouts, were not included. Also, the design rules for the two processes were different. Nevertheless, the data in Table II can still serve as an indication of the potential area reduction that the new process and design rules will yield relative to the C^2L process.

The chip area is reduced to half the area of those chips using the C^2L process. Furthermore, the saving applies to both the 3000-transistor chip as well as to the 6000-transistor chip.

Because it is compatible with the 5-V CMOS/SOS technology, this new cell family, when available, will offer RCA the benefits of a complete, system-compatible dual technology. Where high density and high speed are required, the 4.2-mil, 4-micron CMOS/SOS family is recommended. For high-density application where high speed is not critical, the oxide-isolated, bulk-silicon family will be recommended.

Because no data base exists for the bulk technology, its actual performance cannot be rigorously specified. However, through computer simulation analyses it is anticipated that the 5-V CMOS/SOS technology will be used for LSI applications requiring average stage delays of less than 13 ns. If the delays in excess of 13 ns are acceptable, the bulk technology will be satisfactory.

Experimental cell families

3-micron oxide-isolated CMOS bulk-silicon cell family

The development of an advanced bulk-silicon standard cell family using 3-micron channels is part of the 1981 ATL IR&D programs. The definition and formulation of the process, the processing techniques, processing equipment, and the design rules are currently under development by SSTC and SSD. Based on preliminary inputs on processing steps and design rules, some experimental circuit concepts have been developed. During 1981, the process is expected to reach a state where official, but preliminary, design rules can be released. At this time, the cell design for the family can be expected to proceed at a rapid rate.

2-micron channel CMOS/SOS cell family

B. Leung of SSTC, with processing assistance from N. Goldsmith of the David Sarnoff Research Center, has already developed CMOS/SOS transistors with channels that are 2 microns and less. These and other advanced device and processing techniques, such as low resistivity silicide gate material, were developed on an IR&D program. These developments utilized processing techniques such as plasma etching, positive photoresist, arsenic implanting, and noncontact projection printing techniques. It is expected that these and other processing techniques and equipments, together with the benefit of a new clean-room facility in SSTC, will permit the design of experimental devices using 2-micron channels.

In anticipation of the availability of a 2-micron process, ATL designed a 2-micron version of the 1129-transistor ALU shown in Fig. 10. It is also included on the TCS244 test chip. Thus, the TCS244 test chip contains two, 8-bit ALU LSI test circuits which are identical except for their channel length. One uses 3-micron channels, the other uses 2-micron channels.

Note that much of the new equipment, the processing techniques, and the processing materials will be used in establishing the 3-micron, bulk silicon as well as the 3-micron CMOS/SOS processes. The move from 3 to 2 microns will continue with appropriate scaling and improved techniques to use the various processing and fabrication techniques.

Designing LSI devices with the standard cell approach

To aid the designer in selecting the appropriate cells, a standard cell notebook is available. All of the logic cells are

Table II. C^2L CMOS 1 area comparison.

LSI Type	*Total Area mil²*	*Area/Dev (mil²/D)*	*%Area Reduction*	*No. of Transistors*	*Active Area (mil²)*	*Area/Dev (mil²/D)*	*%Area Reduction*	*Comments*
TVC256 (GCS)	40,530	13.4	45	3,024	25,600	8.5	43	C^2L
CMOS I - 56	22,080	7.4			14,520	4.95		Cell Ht. = 6.7M
ATL BOSCH I/O	118,340	18.9			93,800	16.1		C^2L
CMOS I I/O	60,690	9.7			44,230	7.5		Cell Ht. = 6.7M
TA11038	105,800	16.9	47	6,260	83,700	14.1	52	C^2L
CMOS I 11038	55,450	8.8			39,800	6.7		Cell Ht. = 6.7M
CMOS I 11038	56,600	9.1			40,760	6.9		Cell Ht. = 10.0M

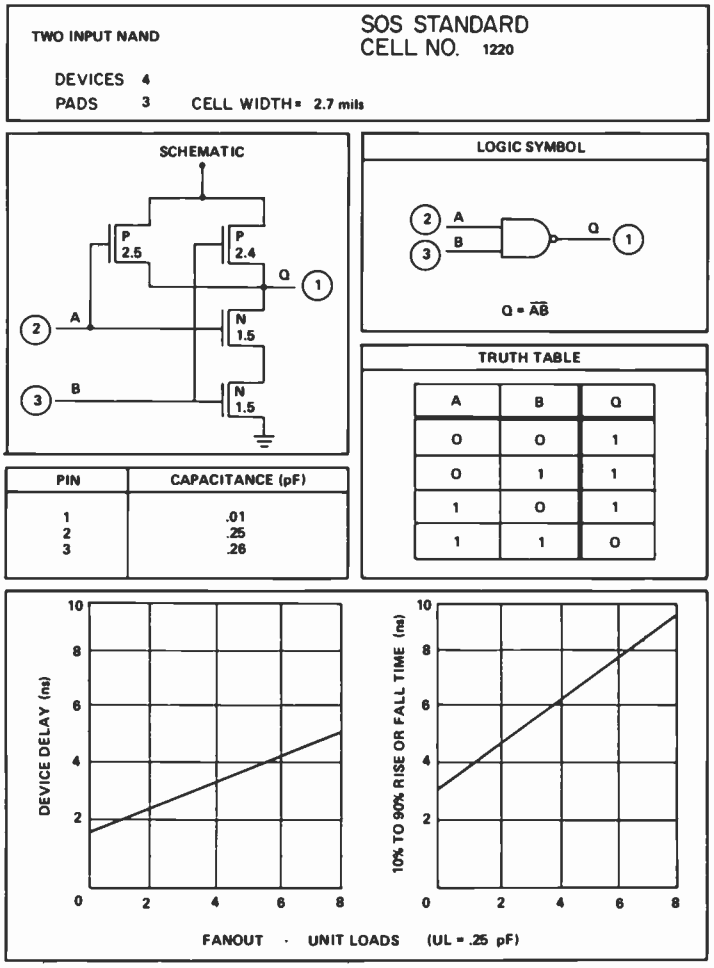

Fig. 11. Typical data sheet.

fully characterized and documented in the form of data sheets. Figure 11 illustrates a typical data sheet. It provides the name and function of the cell, the circuit and the logic configuration, the Boolean equation, the truth table, and the dynamic performance data.

To generate an LSI layout using this design approach, it is necessary to supply only a net list containing the cell identification numbers and their connectivity. Although a considerable amount of additional information is required, such as the cell artwork data and the cell input/output locations, the user is not required to supply it. This and other needed and relevant information are automatically supplied by the midicomputer-controlled[14] computer-aided design and design automation system (CADDAS)[12] shown in Fig. 12. Three such systems are now operational in Camden, New Jersey, using the Prime computer.

Of particular interest in Fig. 12 is the portion of CADDAS identified as DAMACS, an acronym for data management and control system. It is DAMACS that automatically supplies the additional data that is required for the particular program being executed. For example, if the MP2D (APAR) automatic layout program is being executed, it will automatically supply the correct pin data corresponding to the selected standard cell family.

Before a chip is laid out, it is general practice to verify the

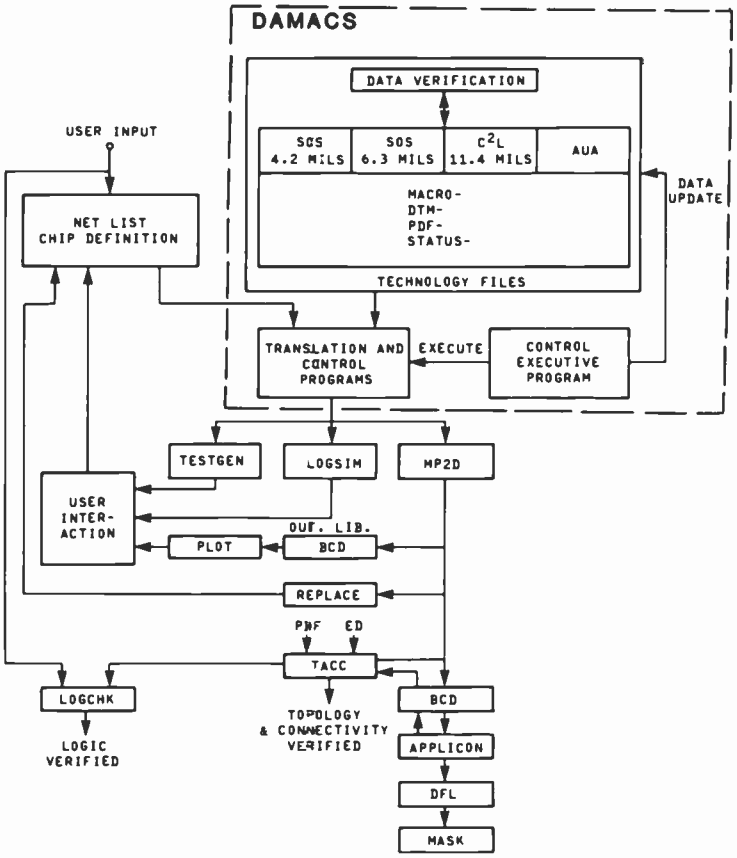

Fig. 12. CADDAS system including Data Management and Control System.

logic using a logic simulator such as LOGSIM. Special macros are required as part of the input data for LOGSIM. DAMACS will automatically supply the appropriate macro for cell families that are currently stored in the technology files. DAMACS will also automatically supply the net list in the format required by LOGSIM. The only input that the user must supply are the test vectors describing the desired output for a given input. The LOGSIM logic simulator will generate an output for any given input and automatically compare it to the expected output.

Similarly, for other design-aid programs which are part of CADDAS, DAMACS facilitates the use of the computer-aided design (CAD) system by minimizing the quantity and complexity of the data that the user is required to supply.

CADDAS, and its various application programs such as MP2D — the automatic layout program; LOGSIM — the logic gate simulator; TESTGEN — a test sequence generation program with fault detection and identification capability; and TACC[13] — a program that automatically and simultaneously checks interconnections on the chip for connectivity and design rule violations, combine to form a mature, thoroughly debugged system for designing LSI devices and subsystems. It is a low-cost system that requires very little additional maintenance beyond that of a service contract.

Because of this, CADDAS is considered a practical and

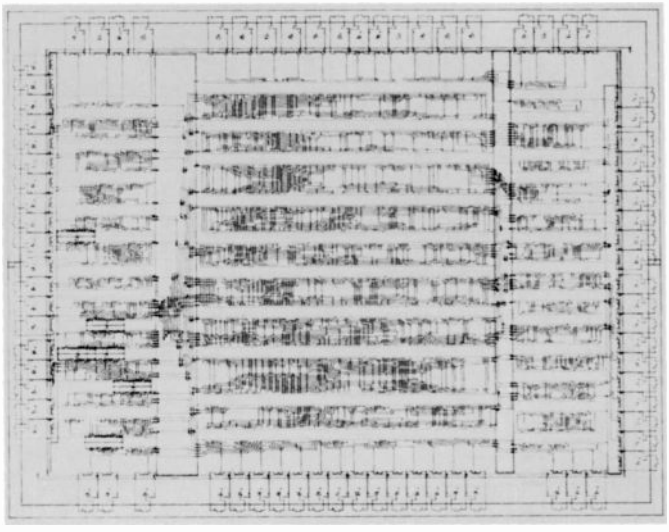

Fig. 13. Fourth-generation LSI automatic layout program.

cost-effective design approach for any activity about to incorporate custom LSI into its product line.

Fourth- and fifth-generation automatic layout programs

It is anticipated that the MP2D (APAR) program will not only continue to be used in the mid- and late-1980s, but it will be used at an increasing rate. However, because of the continually evolving technology that will support larger and more complex chips, there will be a corresponding need for new-generation automatic layout programs. To address this problem, concepts and approaches for fourth- and fifth-generation programs were developed.

The layout shown in Fig. 13 is an illustration of the Segmented MP2D (SMP2D) program — the fourth-generation, standard cell automatic layout program. Its objective is not only to accommodate random logic designs in the 12,000-transistor to 20,000-transistor range, but to provide a 2- to 4-ns propagation delay.

The SMP2D program offers a high degree of flexibility as compared to previous automatic layout techniques. Except for perhaps power distribution, the three segments in Fig. 13 are virtually independent of each other. For example, the vertical coordinate of the cell rows in each of the three segments or groups may be at completely arbitrary levels. A natural consequence of this is that the number of cell rows in each segment can be, and generally will be, different. Other examples of flexibility that will lead to increased density and higher performance include the use of logic cells in the perimeter area normally reserved for input/output pads, the absence of a fixed topology associated with the perimeter or pad area, the use of cell rows as input/output pads, and a more effective power distribution system.

Providing these topological flexibilities requires new software algorithms of increasing complexity and sophistication. These required software changes, together with the topological development, are currently being developed by ATL under a U.S. Army contract.

The requirement to provide VLSI devices in the 40,000- to 60,000-transistor range in the late 1980s has already been identified in one program, the DoD VHSIC program. The VHSIC program will not only directly affect the businesses of the RCA Government divisions, but also virtually any product line that will be using LSI and VLSI devices in the late 1980s. To address these objectives ATL has defined and is currently developing, under a U.S. Army contract, the fifth-generation automatic layout program — Macrocell Automatic Placement and Routing, MACPAR.

Unlike the first four generation programs devoted to standard cell interconnections, MACPAR is designed to interconnect macrocells (or modules). The macrocells can be generated by any one of the various basic design approaches. This could include handcrafted approaches, MP2D or SMP2D designs, gate universal arrays (GUAs), automated universal arrays (AUAs), Programmable Logic Arrays (PLAs), etc. This concept is illustrated in Fig. 4.

Aside from maintaining orthogonality with respect to the basic grid structure, the MACPAR placement algorithm will place the modules with virtually no constraint on their location and orientation. The routing algorithms will rely almost completely on sophisticated variations of the global pathfinder routing routine, which is a maze-searching algorithm. A conceptual illustration of a MACPAR layout showing the complete randomness of the module location and wiring patterns is presented in Fig. 15.

Summary and conclusions

The fifteen-year history of the standard cell approach for generating low-cost, quick-turnaround random logic custom LSI devices is highlighted by the density and performance capabilities of the MP2D automatic layout program, which is used by all current and proposed standard cell families.

The status of the standard cell families in RCA include four current operational, two developmental, and two experimental cell families. The operational families consist of C^2L bulk and five CMOS/SOS families, including a special radiation-hardened family. One of the development families is a CMOS/SOS version that will provide speeds in the 2- to 4-ns range and densities that will provide 2,000 gates (8,000 transistors) in a 200- x 200-mil^2 chip that should be available in early 1982. Another development family, which should be available in late 1981, is a new oxide-isolated bulk-silicon family. This offers a gate potential of 1,000 gates in a 200- x 200-mil^2 chip. A 2-micron CMOS/SOS family and a 3-micron oxide-isolated, bulk-silicon experimental family offer further significant improvements in density and performance within the framework of low-cost and quick-turnaround capabilities.

A mature, low-cost, midicomputer-controlled[14] CAD

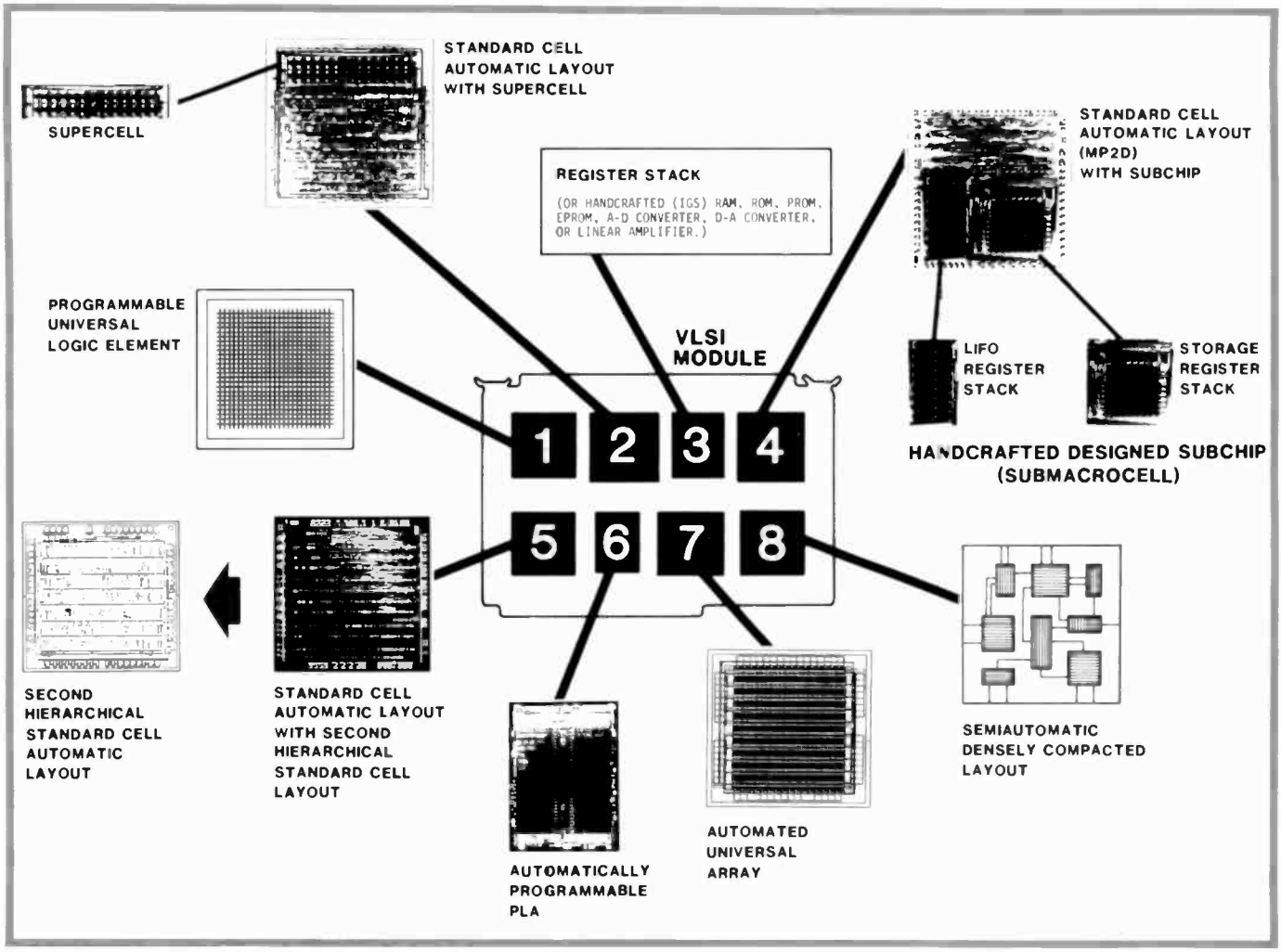

Fig. 14. Fifth-generation automatic layout program.

Authors Al Feller (left) and Richard Noto (right).

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Richard Noto is a Principal Member of the Technical Staff in the Digital Systems Laboratory of the Advanced Technology Laboratories. He has been with RCA since 1961 when his initial responsibilities concerned logic design and analysis. Since 1966 his efforts have centered on design automation for LSI MOS arrays. Mr. Noto developed and wrote the Placement and Routing 2-Dimensional (PR2D) and the Multi-Port 2-Dimensional (MP2D) programs. Recently he developed a general-purpose routing algorithm and a program for the fully automated placement and single-level routing of fixed-geometry gate universal arrays.

Contact him at:
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TACNET: 222-3815

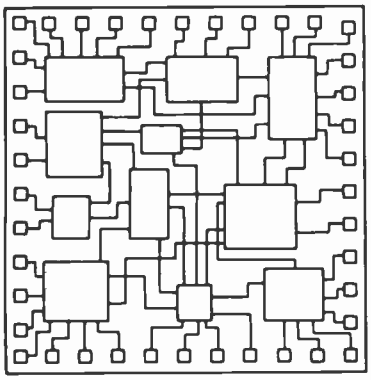

Fig. 15. Macrocells for MACPAR program.

system, CADDAS, not only executes all of the various programs associated with the design and layout of VLSI devices and subsystems, but also dramatically reduces the quantity and complexity of the data that the user must supply. For any activity whose product line will employ custom LSI devices, the ownership and operation of such systems will make it cost-effective for these activities to design their own custom LSI devices.

The fourth- and fifth-generation programs, SMP2D and MACPAR, are now under development. These programs are being designed to extend the standard cell capability for random logic design to 6,000- and 15,000-gate levels, respectively.

Acknowledgments

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- A.M. Smith — principal design of the 5-micron bulk technology family;
- M.W. Stebnisky — principal design of the 2.8-mil CMOS/SOS circuits;
- B.S. Wagner and D.C. Smith — development of CADDAS and DAMACS;
- F. Borgini — design and consultant efforts;
- S. Sharma — analysis and characterization of various cells using the R-CAP program;
- All others whose efforts have been valuable in varying degrees to the development of these programs.

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9. Abeyta, I., Knezich, A.G., and Shedd, R.D., "High-Speed CMOS/SOS Custom and Standard Cell Design for Advanced Signal Processing Applications," *Proc. IEEE/ICCC* (Oct. 1980).
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11. Feller, A. and Stebnisky, M.W., "State-of-the-Art CMOS/SOS Technology for Next-Generation Computers," *Proc. IEEE/ICCC* (Oct. 1980).
12. Borgini, F., *et al.*, "Automated Design Procedures for VLSI," Technical Report for ERADCOM, DELET-TR-782960-3 (June 1980).
13. Wagner, B.S., "A Multi-Technology Checking Program for Large-Scale Integrated Circuits Based on Standard Cells," *RCA Engineer*, Vol. 26, No. 2, pp. 46-52 (Sept./Oct. 1980).
14. What is required to run the automatic layout programs is a computer larger than the typical minicomputer (hence, "midicomputer"). Execution capability and storage capacity are the principal factors in selecting the type. In ATL, we use the Prime 750. Smaller systems have been used successfully.

S.S. Perlman

Computer tool evaluates horizontal transient response of the NTSC color TV system

A computer simulation program with subjective display capability provides a new tool for TV system design and evaluation.

Abstract: *A computer simulation program to faithfully calculate the overall horizontal transient response of an NTSC color TV system from light-image input to light-image output is described. The program processes two horizontal lines of picture data in either the time domain or the corresponding, Fourier-transformed, frequency domain. Electronic processing, linear and nonlinear, is directly simulated in a serial fashion as the signal passes through the entire system. Program results are presented as software-generated plots and tables or are displayed subjectively on a TV monitor. Microprocessor-controlled video hardware converts the digital software-program results into corresponding sets of analog red-green-blue (RGB) signals that drive the kine inputs of the display monitor. A split-screen capability permits easy simultaneous subjective comparisons of up to four different program results corresponding to changes made anywhere within the system.*

The quality of a color television system is frequently measured on the basis of its response to a variety of test patterns. Measurements of horizontal transient response for standard patterns like the composite, multiburst or color-bar test signals, have long been recognized as suitable vehicles for evaluation.[1] Computer-aided evaluations for certain luminance (black-and-white) transitions have been employed successfully. The effects of various combinations of vestigial sideband (VSB) filters, FCC predistortion filters and receiver RF/IF processing were demonstrated many years ago to greatly influence the errors and distortions in the received luminance waveshapes.[2]

The Light-to-Light (L-to-L) programs extend the computer-model concept to color, in addition to the luminance signals; they also simulate directly and trace these signals as they pass through a complete NTSC television system. Vertically equivalent TV signals are treated in the simulation; software-generated plots can be directly compared to experimental oscilloscope traces at corresponding locations anywhere within the system. Signals are traced from the camera's light-image input to the receiver's light-image output. A special display capability permits subjective viewing of the simulated responses in order to enhance evaluation.

The L-to-L programs were developed as an aid for system and circuit designers in their quest to analyze the overall performance effects of signal processing changes made anywhere within the TV systems. Complicated design problems, like those related to chroma-quadrature or color-edge distortion, for example, can now be directly evaluated via computer-simulation techniques without the need to construct complicated test fixtures.

Programming techniques

A television system can conveniently be divided into three basic portions: the camera, the transmitter, and the receiver. The L-to-L computer simulation treats each of these independently and combines them with other portions, as shown in Fig. 1. The programs simulate real TV-like signals and process them in a serial fashion as they pass through the system from a light-image input to a light-image output. Each portion of the system is divided into a series of programmed boxes, each containing appropriate mathematical models to represent the actual signal processing involved. Both linear and nonlinear processing

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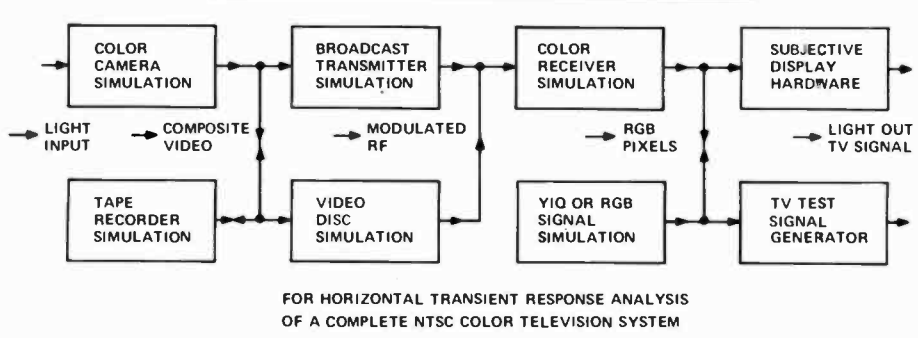


Fig. 1. Block diagram for the Light-to-Light computer simulation.

are treated. Software-generated plots and data tables are designed to compare with experimentally obtainable oscilloscope traces or data anywhere within the system.

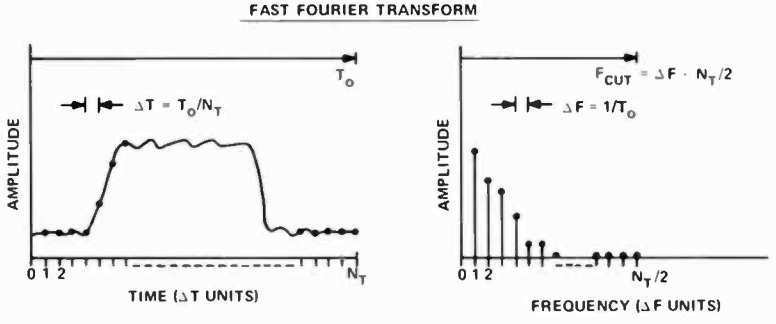
Essentially, all of the processings in the camera, transmitter, and receiver portions of the system have been successfully programmed. Simulations for the tape recorder and VideoDisc portions are currently under consideration and not yet fully programmed. The subjective display hardware and the test-signal generator are fully operational. These portions of the simulation convert the red-green-blue (RGB) or composite video signals into sampled digital picture-element (pixel) data and then to equivalent analog TV signals in an NTSC format.

Also included as part of the L-to-L simulation is a special portion designed to aid in research related to the evaluation of psychological effects or human visual perception of color transitions. Test patterns with arbitrarily defined hue saturation and luminance transitions can be displayed and used subjectively to evaluate viewer preferences.

Output signals from each portion of the simulation are designed to be totally compatible and acceptable as input signals to the next or other portions. A special provision is provided via a jump-and-alter subroutine which allows the user to change signals and then to jump to any other box location within the program or to go to the start of another program for a different portion of the system. Possible alter options include saving a signal on disc file, inputting a new signal from a disc file, changing domain (time or frequency) of a signal, applying an MTF (filter) to the signal, adding two signals, multiplying two signals, copying another signal, combing-out odd or even harmonics from a signal, amplitude modulating with a carrier, adding impulse noise, applying nonlinear clipping, and plotting resulting signals on a graphic terminal[3] or flat-bed plotter.[4] The jump routine provides an easy method for cycling through one of the boxes in the program in order to evaluate effects of various design changes.

Programming limitations

The L-to-L simulation programs have been written in Fortran IV language using the CMS interactive mode on an IBM/370 computer. The simulated TV signals are each stored as a pair of arrays (real and imaginary vector parts). A trade-off between array size and sample rate or cutoff (Nyquist) frequency had to be established. Figure 2 reviews



N_T	T_o 63.555 μs = 1 H LINE			T_o = 127.11 μs = 2 H LINES			T_o = 254.22 μs = 4 H LINES		
	ΔT (ns)	ΔF (kHz)	F_{CUT} (MHz)	ΔT (ns)	ΔF (kHz)	F_{CUT} (MHz)	ΔT (ns)	Δ F(kHz)	F_{CUT} (MHz)
1024	62.07	15.73	8.06	124.1	7.87	4.03	248.3	3.93	2.01
2048	31.03	↓	16.11	62.07	↓	8.06	124.1	↓	4.03
4096	15.52	↓	32.22	31.03	↓	16.11	62.07	↓	8.06
8192	7.76	↓	64.45	15.52	↓	32.22	31.03	↓	16.11
16384	3.88	↓	128.9	7.76	↓	64.45	15.52	↓	32.22

Fig. 2. Fundamental parameters for the Fast Fourier Transform. Only the signal periodicity, T_0, and the number of data samples, N_T, need be chosen to get the required bandwidth, F_{CUT}, and the proper harmonic content, ΔF.

some fundamentals of the Fast Fourier Transform (FFT) used to convert between the time and frequency domain representations of the signal. Variables of interest are:

T_0 = Time Window (or periodicity),
N_T = Number of Samples (or array size),
F_{CUT} = Highest Harmonic Frequency (or Nyquist frequency),
ΔF = Lowest Harmonic Frequency,
and ΔT = Sample Time.

These are interrelated by the equations in the figures such that only two, T_0 and N_T, need be chosen. In addition, the FFT algorithm requires N_T to be an integer power of two.

The best choice for the L-to-L programs is to make T_0 equal two horizontal TV lines (2*63.55 μsec ≡ 2H) and $N_T = 2^{12} = 4096$. For these values, F_{CUT} = 16.11 MHz and ΔF = 15.734/2 kHz (half the horizontal line rate) and ΔT = 0.03101 μsec. Lower N_T values lead to inadequate F_{CUT} or bandwidth while lower T_0 leads to improper harmonic content to express a composite NTSC video signal. Proper harmonic content is maintained, provided T_0 is expanded in multiples of 2H lines; however, larger T_0 values were considered impractical due to the corresponding larger array sizes needed. For example, to represent a four-field stationary TV image, T_0 = 1050H is required with a corresponding array size, $N_T = 2^{21}$ = 2,097,152 to keep similar bandwidth. This little exercise serves to demonstrate the enormous quantity of information contained in a TV scene. Clearly, a compromise had to be established, and T_0 = 2H was selected as the periodicity of the simulated TV signals. This compromise restricts the simulation to vertically equivalent scenes, like color-bar patterns, and to the analysis of horizontal transient response only.

Any time-domain TV signal can be simulated by sampling at the selected rate of 0.031 μsec or 2048 per H line. The data can then be entered into the computer and stored as the desired signal. When transformed to the frequency domain, a series of $N_T/2$ harmonics of one-half the horizontal line rate (15.734/2 kHz) will result. The sum of these waves with the corresponding amplitudes and phase angles will yield the original time-domain signal, provided the high-frequency content of the wave remains below the 16.11-MHz Nyquist frequency selected.[5]

Simulation of the various electronic processes encountered in the TV system can usually be accomplished by simple mathematical or computer manipulation of the individual time- or frequency-domain samples corresponding to the TV signal. For example, modulation-transfer functions (MTFs) or electronic filters can be applied by a frequency-domain-vector multiplication of the MTFs' amplitude and phase characteristics with the corresponding amplitude and phase properties of the signal. This process is generally easier than the equivalent time-domain convolution with the impulse response of the MTF. In the L-to-L programs, MTFs can be described as data sets of frequency amplitude and phase angle in the range of interest. Interpolation techniques are employed to evaluate the MTF at the 15.734/2 kHz harmonic frequency's need. The programs also accept MTFs expressed as poles and zeros, and calculate the amplitude and phase responses at the harmonic frequencies. Other electronic processes can be handled in a similar fashion. Generally speaking, nonlinear functions, like clipping, are performed by manipulation of time-domain signals.

Program example

Camera portion

Use of the L-to-L simulation begins with the choice of an input light pattern corresponding to an arbitrary color image. Horizontal 2H time-domain traces of the R, G, and B signals are selected or taken from a disc file.[b] Processing then proceeds as outlined in Table I.

As an example, consider a program run using a standard EIA color-bar test signal (100-percent saturated colors at 75-percent amplitude). A standard camera design, meeting NTSC specifications, is also assumed. After processing with appropriate MTFs and matrix elements, a composite video signal is obtained and saved at the end of the camera portion of the program. The frequency-domain representation of the signal is shown in Fig. 3. Both luma and chroma information are presented but can be separated easily by viewing only the even harmonics (luma) or the odd

Table I. Summary of camera simulation.

A.	Select light input time signals for R, G, and B.[a]
B.	FFT to frequency domain.[b]
C.	Apply optical MTF to R, G, and B.[b]
D.	Apply pick-up device MTF to R, G, and B.[b]
E.	FFT to time domain.[b]
F.	Apply nonlinear gamma correction to R, G, and B.[b]
G.	Apply encoder matrix to form Y, I, and Q.
H.	FFT to frequency domain.
I.	Apply different MTF to Y, I, and Q.
J.	Modulate color subcarrier with I and Q.
K.	Form composite signal.
L.	FFT to time domain.
M.	Add SYNC to signal.
N.	Convert to IRE units.
O.	FFT to frequency domain.
P.	Save composite camera output signal.

[a] Choices include EIA color bars, composite and multiburst signals, or arbitrary R, G, and B signals stored in disc file.

[b] This step omitted for standard test pattern signals, like EIA color bars.

harmonics (chroma), as shown in Fig. 4. The time-domain equivalent of the camera output signal is given in Fig. 5. Only the first 25 μsec of the 2H trace is shown. Of course, the camera I and Q modulators set the amplitudes and phases of the chroma signals for the different colors of the signal to their proper values relative to the burst.

The camera output signal represents a baseband input signal that can be used in essentially any of the other portions of the L-to-L programs.

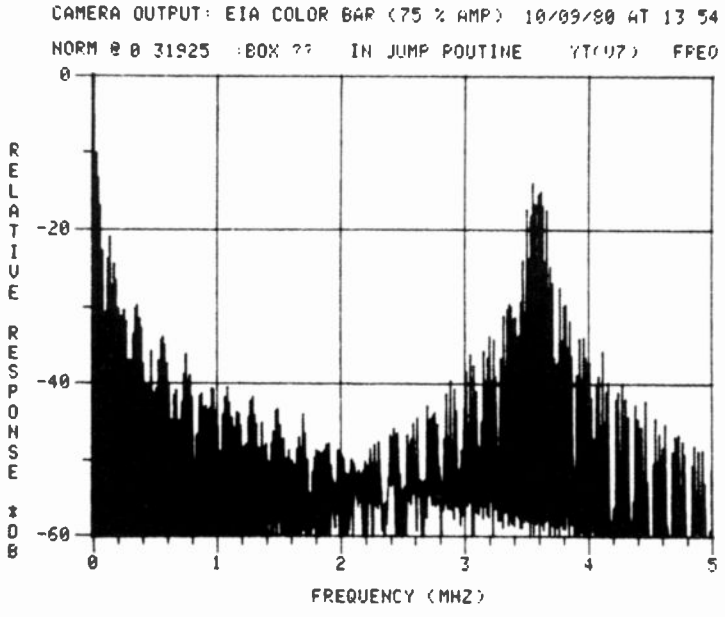


Fig. 3. Simulated camera output signal in the frequency domain for the example program run showing both odd and even harmonics of half the horizontal line rate.

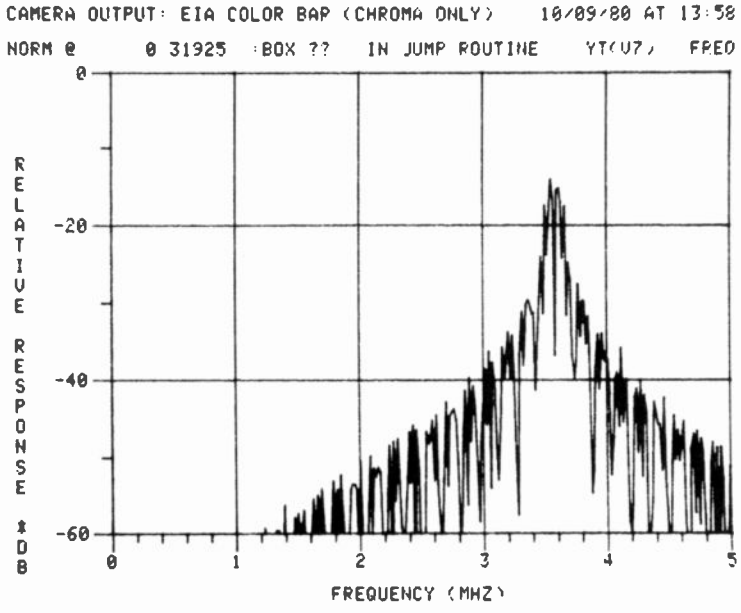


Fig. 4. Simulated camera output signal in frequency domain for the example program run showing only odd harmonics of half the horizontal line rate.

Transmitter portion

The program run continues with the assumption of a standard NTSC transmitter (Channel 4 with picture carrier at 67.25 MHz). The processing is outlined in Table II. Again, appropriate MTF characteristics and process variables are selected and the signal leaving the transmitter is as shown in Fig. 6. The spectrum actually shown, however, has the transmitter output signal (66 to 72 MHz) plus two adjacent channel signals (at −10dB) that were

Table II. Summary of transmitter simulation.

A.	Input composite baseband signal.
B.	Apply predistortion MTF.
C.	Apply phase equalization.[a]
D.	Apply low-pass MTF.
E.	FFT to time domain.
F.	Adjust video gain for % modulation.
G.	Modulate RF carrier.
H.	FFT to frequency domain.
I.	Apply power amplifier gain and MTF.
J.	Apply vestigial sideband MTF.
K.	Add frequency-modulated sound signal (single tone).
L.	Save RF transmitter output signal.[b]

[a] Simulation of RCA TTS-1B Delay Equalizer System can be used. User selects desired switch positions.

[b] Signal corresponds to the positive half of the modulation envelope.

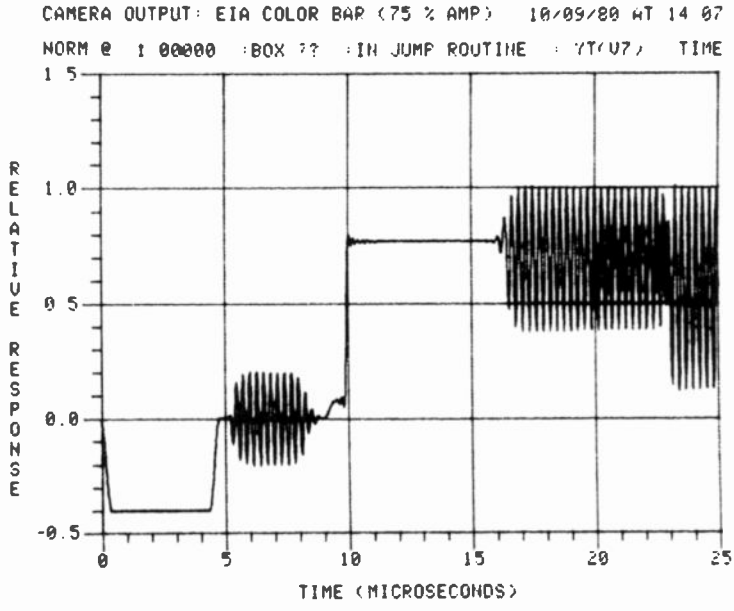


Fig. 5. Simulated camera output signal in the time domain for the example program run showing only the first 25 microseconds of the first horizontal line.

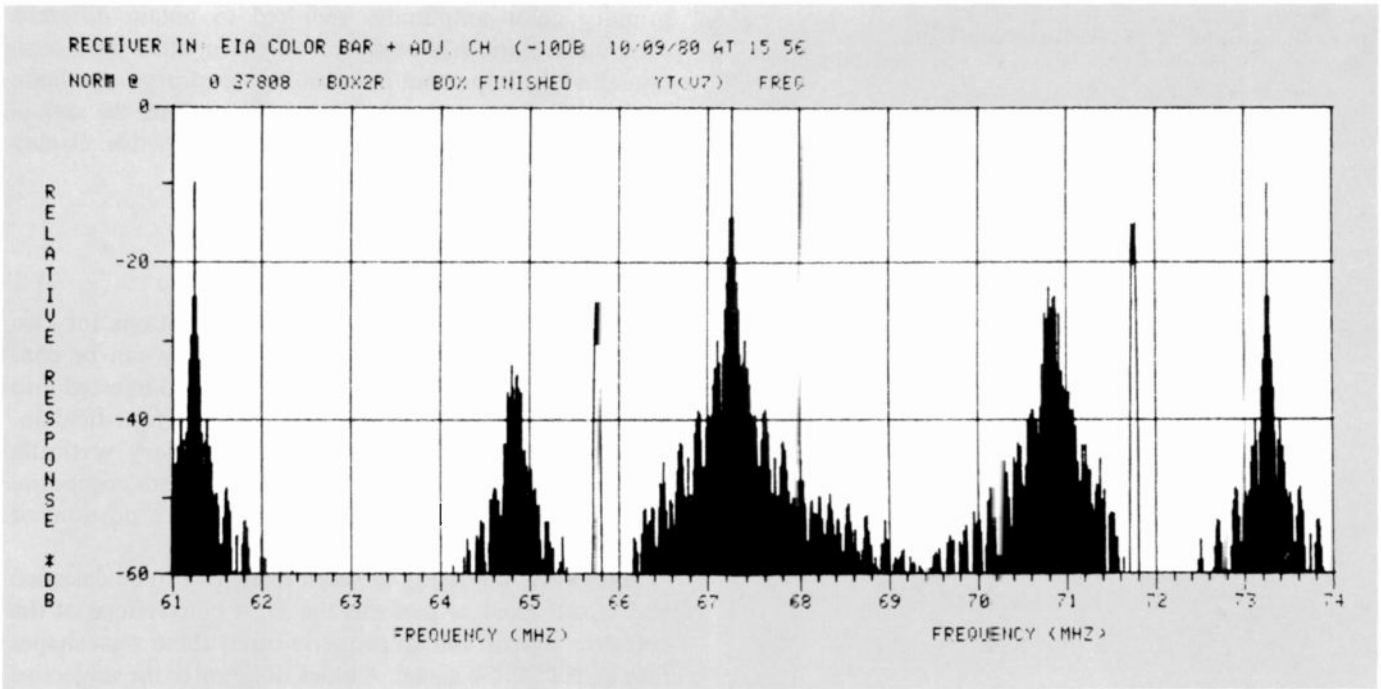


Fig. 6. Simulated transmitter output signal in frequency domain for the example program run showing main-channel information (67.25 MHz) plus adjacent-channel signals at -10 dB amplitude.

added in the beginning of the receiver portion of the program. The time-domain equivalent for the modulation envelope of the transmitter output signal is complicated by the presence of the FM-modulated sound carrier at 67.25 + 4.5 MHz. On location, the signal is demodulated with special equipment and viewed directly on an oscilloscope.[7] A comparable capability is provided in the L-to-L programs by a simulation of the response of an ideal demodulator. The RF/IF section provides flat-band response plus the proper Nyquist slope region. It also provides equalization for the predistortion and rejection characteristics for co-channel sound and adjacent-channel signals. Figure 7 shows the resultant demodulated and synchronously detected transmitter output signal. Consumer TV receivers need not match such ideal front-end characteristics. The cost of implementation makes these designs impractical. Generally, less than ideal characteristics are tolerated with an attempt made during baseband processing to correct for any deficiency.

Receiver portion

Our example program run now proceeds to the receiver portion. An outline of the processing included is given in Table III. We shall assume a typical consumer-TV receiver design. The front-end RF and IF sections are lumped-element designs. Envelope detection is employed, followed by a power splitter, and luma/chroma separation filters. Chroma-demodulation angles and gain values are designed to match the specific primary phosphor colors of the kinescope.[8]

When the simulation is performed with the receiver controls (like tint, chroma, peaking, etc.) set at their nominal values, the resultant RGB kine-input signals are as shown in Fig. 8. A careful examination of these waveforms demonstrates the presence of various effects typically observed in experimental measurements made on such receiver designs. For example, we see (1) dot crawl, or the presence of odd harmonics in the RGB signals, (2) luma peaking, or presence of preshoot and overshoot on luma transitions, (3) color-matrix adjustments, or the change in

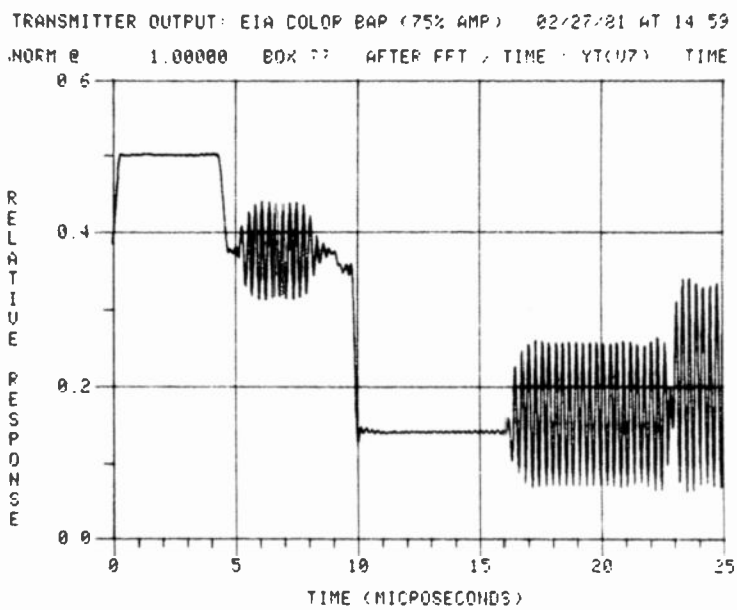


Fig. 7. Simulated transmitter output signal, in time domain, after demodulation and detection using high-quality studio equipment.

Table III. Summary of receiver simulation.

A.	Input RF signal.[a]
B.	Add reflections (echos).
C.	Add adjacent channel signals.
D.	Apply RF gain and MTFs.
E.	Modulate to IF frequencies.
F.	Apply MTFs and IF gain.
G.	Detect to baseband signal.[b]
H.	Apply detector MTF and nonlinearity.
I.	Apply sound, alias, and/or equalization MTFs.[c]
J.	FFT to time domain.
K.	Apply AGC and convert to IRE units.
L.	FFT to frequency domain.
M.	Apply CCD or power splitter.
N.	Apply 3.58 chroma trap to luma signal.[c]
O.	Apply luma-phase adjust.[c]
P.	Apply CCD-clock MTF.[c]
Q.	Add vertical restoration signals to luma.[c, d]
R.	Apply luma peaker and delay adjust.
S.	Apply chroma peaker and delay adjust.
T.	FFT to time domain.
U.	Apply automatic chroma gain adjust.
V.	Recover chroma-burst phase for demodulator.
W.	Demodulate chroma with desired gain and angles.
X.	Apply color-difference MTFs.
Y.	Apply decoder matrix for R, G, and B.
Z.	Apply kine-driver MTF to R, G, and B.
Za.	Save R, G, and B kine signals for display.
Zb.	FFT to time domain.
Zc.	Evaluate color-error information.[e]
Zd.	Adjust brightness and contrast.
Ze.	Apply kine gamma correction.
Zf.	Calculate light output versus distance.

[a] RF and IF processing can be bypassed if input is composite baseband signal.

[b] Envelope or synchronous detection available.

[c] Omit if inappropriate for design.

[d] Vertical restoration in the L-to-L Program introduces only chroma noise (dot crawl components) into the luma signal.

[e] Quantitative numbers can be calculated to express color errors experienced during a color transition.[16]

primary color amplitudes required to obtain different saturated colors. Although software-generated plots contain all of the important information necessary to evaluate horizontal transient response of a TV system, the task is greatly simplified by the use of the subjective display capability of the simulation.

Subjective display portion

Since the L-to-L signals are direct simulations for two horizontal lines of video information, they can be converted to equivalent analog waveshapes and injected into the appropriate line positions to form a four-field interlaced raster corresponding to a stationary vertically equivalent TV scene. This is possible for both composite video signals, like those leaving the camera portion, or RGB video signals leaving the receiver.

Hardware, operating at video rates, had to be designed and constructed to perform the D/A conversions of the software signals and to properly insert these waveshapes into an NTSC TV signal. A block diagram of the subjective display hardware is presented in Fig. 9. Pixel values are obtained by software-interpolation techniques using the chosen video-display rate of 14.32 MHz (four times the color subcarrier).[9] The pixels are stored as 8-bit integers with a total of 1820 needed for each 2H-long signal. Once the pixel values have been computed, they are transferred via a modem to the display microprocessor and stored on a floppy disc for later use.[10]

In order to display RGB signals, 3 times 1820 pixels — or roughly 6K of RAM — is needed. The microprocessor memory map was designed to contain 24K of high-speed (video rate) RAM. Thus, four complete sets of RGB pixels can be stored and accessed by the microprocessor and the video-control circuits. Each set of RGB pixels can correspond to a different program run and, therefore, to different design changes in the TV system.

Control circuits were designed to simultaneously address corresponding RGB pixel values at the video rate and to route this data to the three digital-to-analog (D/A) converters.[11] A sync generator chip provides the basic timing for a standard NTSC TV signal.[12] Microprocessor software was developed to provide trigger information for the control circuits so that pixel data could be properly inserted and interlaced into the NTSC format. The processor is operated in an interrupt mode or on a time-shared basis so that normal processor functions can be performed even when the display is turned on. Since sufficient RAM is provided to store four sets of pixels, it is possible to divide the TV raster into bands and simultaneously display different program results.

The RGB signals from our test run (Fig. 8) were processed as outlined above and the resulting TV signals were displayed on an RGB monitor.[13, 14] Figure 10 shows the monitor screen.[15] (It is a black-and-white version of the color photograph shown on the back cover.) Band 1, at the top of the screen, represents the scene for our test run of the

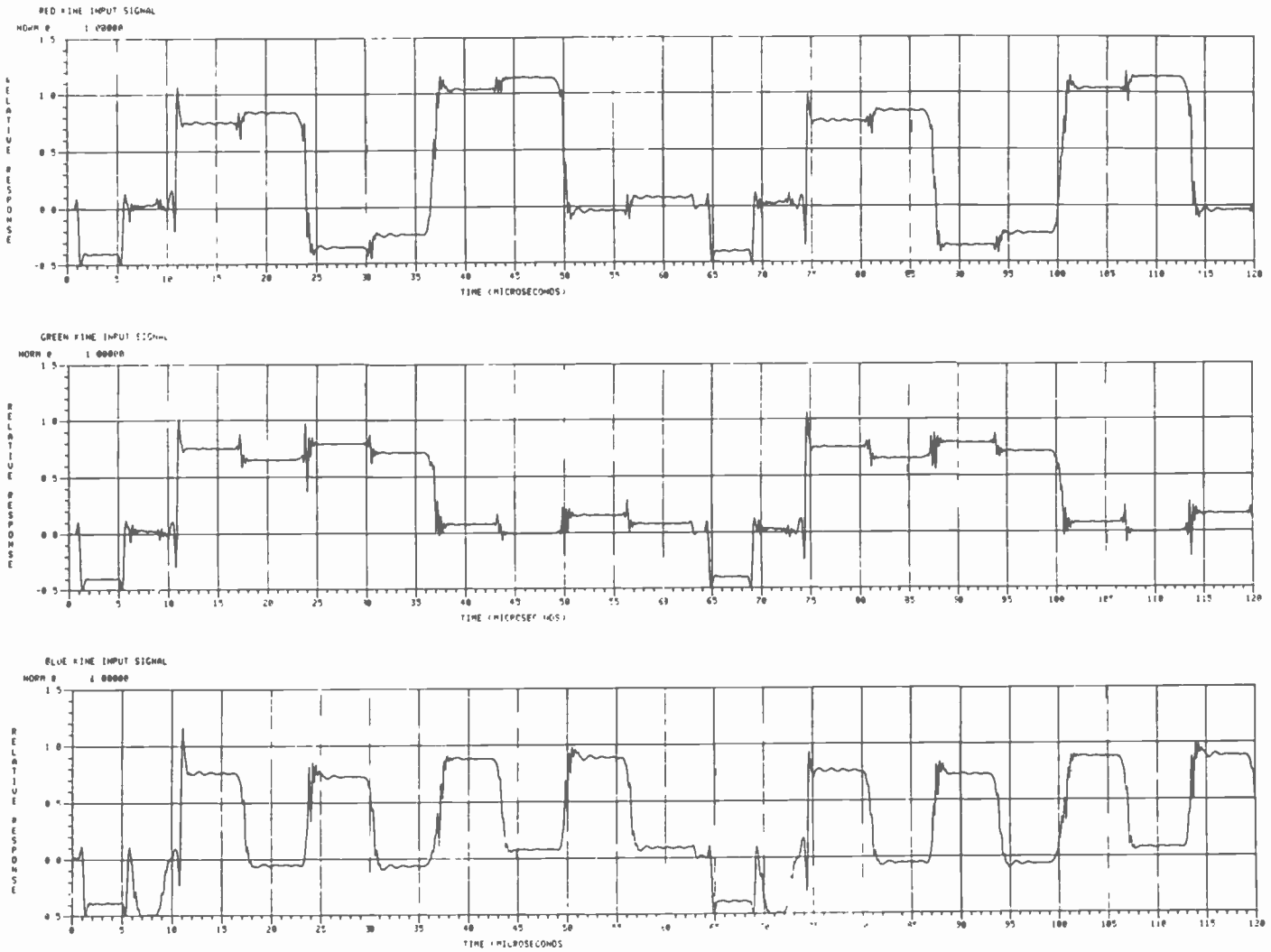


Fig. 8. Simulated RGB kine signals in the time domain for the example program run showing the entire two horizontal lines considered.

program; this corresponds to the TV system with the camera, transmitter, and receiver controls set to nominal design values. The other bands correspond to other program runs where everything was kept constant except: Band 2, chroma gain in the receiver reduced a factor of ten below nominal; Band 3, tint control in the receiver adjusted so that chroma demodulation was +30 degrees from nominal; and Band 4, tint control in the receiver adjusted so that chroma demodulation was at −30 degrees from nominal. These other program examples correspond to rather obvious changes in the TV system, and are presented merely to demonstrate the effectiveness of the subjective display capability. Analyses of these simulated RGB waveshapes without the use of the subjective display would be much more difficult and less satisfactory. Of course, the L-to-L simulation programs are intended to treat the more interesting cases where results of system design changes are not immediately obvious or even predictable without the aid of a simulation program.

Summary

A new computer tool for evaluations of horizontal transient response of the NTSC color television system is described and demonstrated. Vertically equivalent television signals are simulated and mathematically processed in a serial fashion to exactly copy actual linear and nonlinear electronic processing in current camera, transmitter, and receiver designs. Color-bar signals with arbitrarily defined color transitions can be processed and results can be presented on a subjective TV monitor display.

Simultaneous display and evaluation of up to four signals is possible. Each can correspond to a slight modification of any of the processing steps within the entire TV system. Consequently, selection of the best modification or circuit design change can be easily made without breadboarding all of the possibilities.

Comparable simulations for VideoDisc and videotape recorders and players are not fully operational, but, when

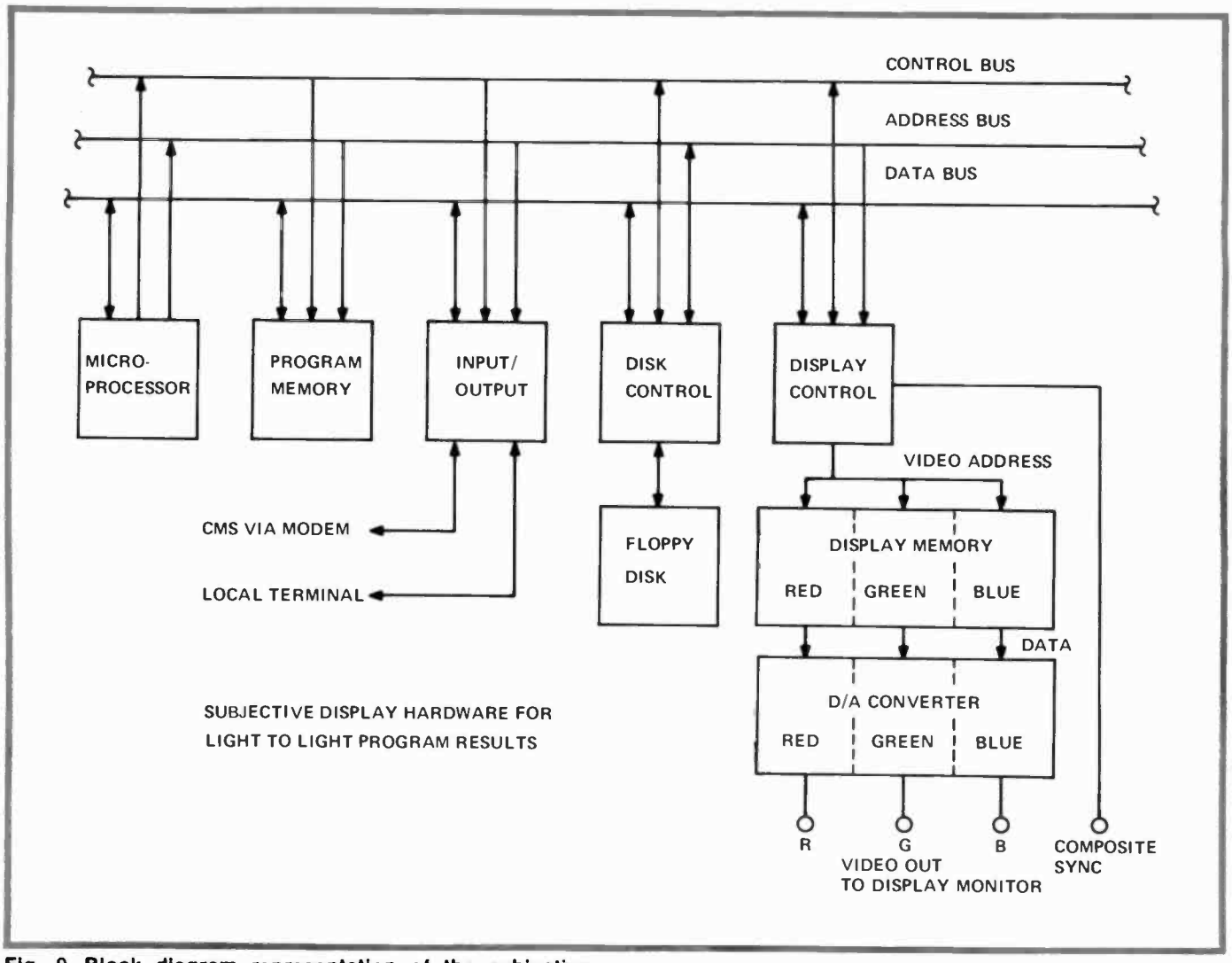


Fig. 9. Block diagram representation of the subjective display hardware.

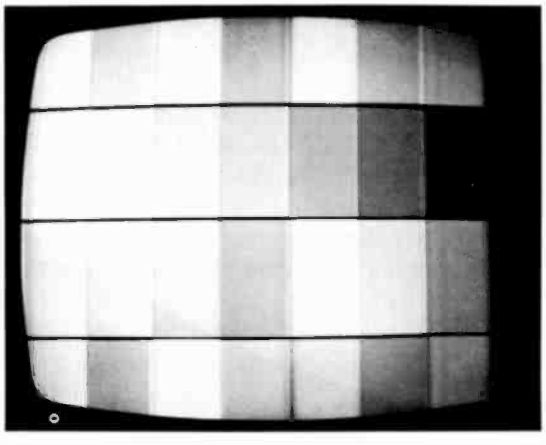
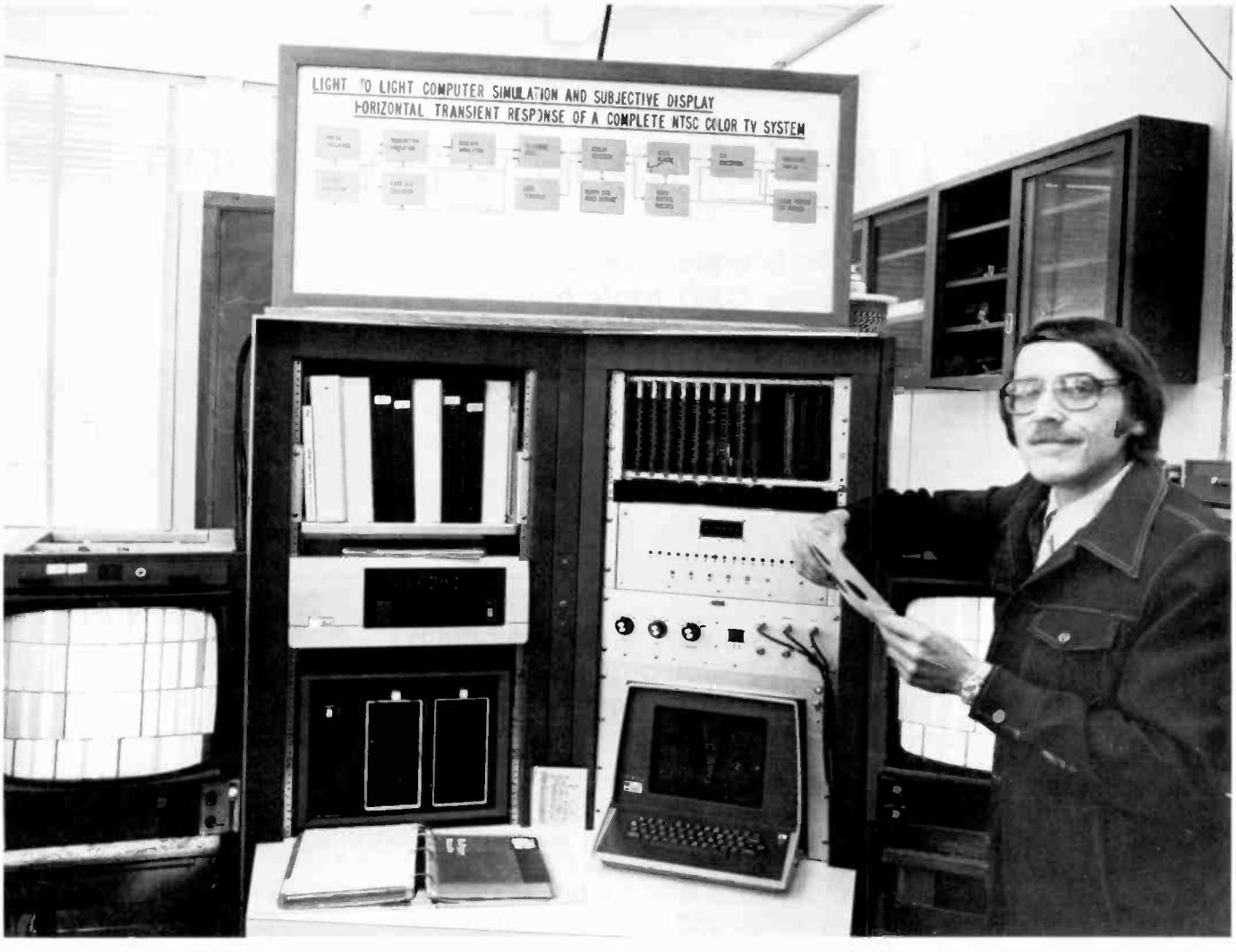


Fig. 10. Photograph of the subjective display monitor, showing results of program run (Band 1 at top) plus results for similar runs (other bands) corresponding to different changes in receiver's design parameters. See color photo on back cover.

available, should ultimately prove an excellent design aid. Subjective and simultaneous comparisons of TV systems using these components with others employing the normal camera, transmitter, and receiver designs should be possible. This unique display capability gives the L-to-L simulation program a special advantage over the more traditional evaluation techniques.

Acknowledgments

The author gratefully acknowledges many discussions with numerous researchers within RCA working on specific portions of the TV system. D.H. Pritchard and A.C. Schroeder deserve particular mention for being instrumental in suggesting the project and providing overall information on the NTSC TV system. Special thanks is also given to J.P. Bingham for suggesting the addition of a subjective display capability, and to H.G. Lewis, A.L. Greenberg, and H.M. Kern for their assistance in the design and construction of the necessary hardware.



Author Stu Perlman shown with hardware for subjective display portion of the Light-to-Light program. Included are an RGB monitor with RCA phosphors (at the left), the microprocessor and floppy disk (center left), RAM cards, control circuits and a graphic terminal (center right), and a second RGB monitor with Conrac phosphors (right side).

Stu Perlman joined RCA Laboratories in 1962 as an Engineering Consultant and a year later as a full-time Member of Technical Staff. Dr. Perlman's research efforts have included work on semiconductor heterojunctions, plezoferroelectric analog memory devices, and microsonic (SAW) TV-IF filters; for the past few years, he has worked on television system analysis employing computer simulation techniques.

Contact him at:
RCA Laboratories
Princeton, N.J.
TACNET: 226-2919

References and notes

1. These test signals are often included during the vertical interval, lines 18 and 19, of a standard NTSC transmission
2. Bingham, J.P. and Patel, C.B., "Effects of Vestigial Sideband Passband Characteristics Upon Television Transient Response," *IEEE Trans. Broadcasting*, Vol. BC-22, No. 3, pp. 68-72 (Sept. 1976).
3. Tektronix computer graphics terminals, such as Model 4006-1, display terminal.
4. Tektronix computer graphics terminals, such as Model 4662, interactive digital plotter.
5. Ramirez, R.W., "The Fast Fourier Transform's Errors Are Predictable, Therefore Manageable," *Electron.*, Vol. 47, No. 12, pp. 96-102 (June 13, 1974).
6. A choice of three built-in test signals is provided: EIA color bars, composite and multiburst. Other signals have to inputted from the terminal or a disc file.
7. Tektronix 1450 demodulator, for example.
8. For example, "field" phosphors are used in RCA kinescopes. These differ from the NTSC standard phosphors, mainly in the color of the green phosphor.
9. This rate is generally accepted as a standard video rate in NTSC broadcast studio equipment.
10. Intel 8085 microprocessor plus SBC80 diskette system.
11. Only one D/A converter is needed when composite video test signals are being generated.
12. Fairchild 3262B TV SYNC generator.
13. An RGB monitor is needed which has broadband kine inputs (greater than the receiver design being simulated).
14. The monitor should have the exact kinescope or at least the same phosphor colors as the receiver being simulated.
15. Conrac color television monitor, Model RHM. The phosphors of this monitor do not agree with RCA field phosphors. They are closer to the NTSC standard phosphors.
16. Pritchard, D.H. and Wagner, T.M., "Color Signal Inphase and Quadrature Distortion Measurement and Evaluation," *RCA Rev.*, Vol. 38, pp. 31-32 (March 1977).

L.J. Judice

LSI: The Computer Connection

A behind-the-scenes view of the LSI design cycle shows how CAD tools help at every step.

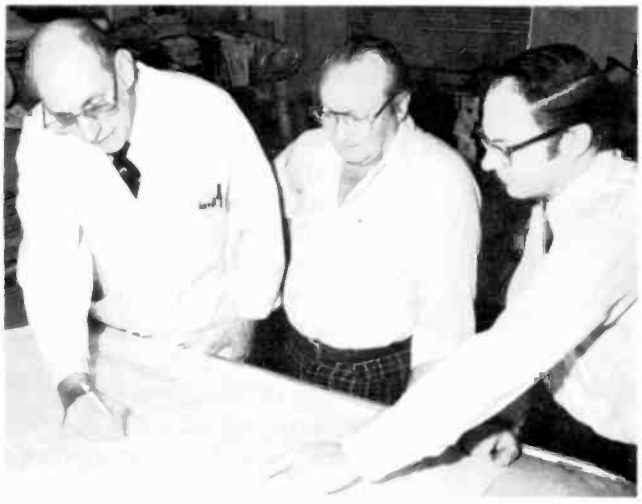
Few trends in modern technology hold more promise for RCA than the explosive growth of microelectronics. Advances in disciplines, such as solid-state device physics and photolithography, have transformed the circuit designer into a system designer who can incorporate tens of thousands of functions on a single slice of silicon.

Advances in application areas such as consumer electronics, automotive electronics and telecommunications are predicated on the development of more powerful microprocessors and more sophisticated linear circuits.

Paradoxically, however, the design of tomorrow's microcomputers may be impossible without the aid of today's computers. At this moment, computer-aided design (CAD) is helping RCA deliver state-of-the-art products by reducing the time required to move ideas from the drawing board to the production line. Tomorrow it will play a key role in developing the potential that exists for us in what some call the Second Industrial Revolution.

This photoessay records and explains the CAD capabilities developed by the Design Automation department of the Solid State Technology Center (SSTC) in Somerville, New Jersey, and used throughout SSTC and the Solid State Division. This article demonstrates how pervasive computer technology helps at nearly every stage of the LSI design cycle. The photographs depict the work flow in the course of a typical design, and a list of references enables the reader to obtain more detailed information.

Reprint RE-26-6-3 Final manuscript received March 4, 1981.



1 We begin with a schematic diagram, the standard description of the engineer's solution to a customer's problem. Although it marks the end of the conceptual phase of design, it is also the beginning of the road towards realization.

A. MIMIC Output.

```
>>: .restore  tnum=0
>>: .apply  pattern=pjctr
>>: .print  prange:1-12
>>: .trace  prange:12 - 16  list:
>>: .nowarn  hazard:
>>: .simulate

                                CR  9 9 9
                                LE  1 2 3
                                OS
                                CE
                                KT
                    7 T    1:  10  0 0 0
                    0 T    2:  11  0 0 0
                    0 T    3:  01  0 0 0
                    4 T    4:  11  1 0 0
                    0 T    5:  01  1 0 0
                    4 T    6:  11  1 1 0
                    0 T    7:  01  1 1 0
                    6 T    8:  11  1 1 1
                    0 T    9:  01  1 1 1
                    6 T   10:  11  0 1 1
                    0 T   11:  01  0 1 1
TRACE-ON-CHANGE...SIGNAL: CLOCK
     TIME:     0, TEST:    12, LEVELS: 0  -> 1
TRACE-ON-CHANGE...SIGNAL: Q2
     TIME:     6, TEST:    12, LEVELS: 1  -> 0
     6 T   12:  11  0 0 1
TRACE-ON-CHANGE...SIGNAL: CLOCK
     TIME:     0, TEST:    13, LEVELS: 1  -> 0
TRACE-ON-CHANGE...SIGNAL: F3.1
     TIME:     0, TEST:    13, LEVELS: 1  -> 0
TRACE-ON-CHANGE...SIGNAL: CLOCK
     TIME:     0, TEST:    14, LEVELS: 0  -> 1
TRACE-ON-CHANGE...SIGNAL: Q1
     TIME:     6, TEST:    14, LEVELS: 1  -> 0
TRACE-ON-CHANGE...SIGNAL: BACK
     TIME:     7, TEST:    14, LEVELS: 0  -> 1
TRACE-ON-CHANGE...SIGNAL: CLOCK
     TIME:     0, TEST:    15, LEVELS: 1  -> 0
TRACE-ON-CHANGE...SIGNAL: F1.1
     TIME:     0, TEST:    15, LEVELS: 0  -> 1
TRACE-ON-CHANGE...SIGNAL: CLOCK
     TIME:     0, TEST:    16, LEVELS: 0  -> 1
TRACE-ON-CHANGE...SIGNAL: RESET
     TIME:     0, TEST:    16, LEVELS: 1  -> 0
TRACE-ON-CHANGE...SIGNAL: RBUF
     TIME:     0, TEST:    16, LEVELS: 1  -> 0
TRACE-ON-CHANGE...SIGNAL: F1.1
     TIME:     0, TEST:    16, LEVELS: 1  -> 0
>>: .quit

QUIT COMMAND ISSUED...EXITING FROM MIMIC!!
```

Run Commands

Signal Names

Pattern Numbers

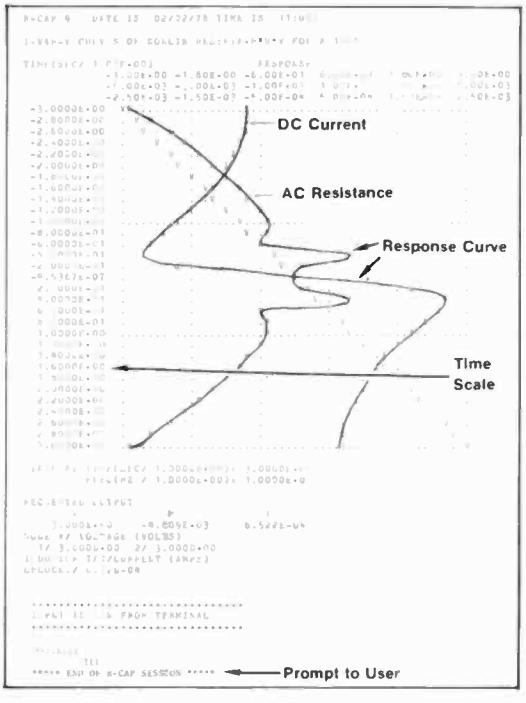
Signal Values

Transition from 0 to 1

Trace of Signals as each Changes

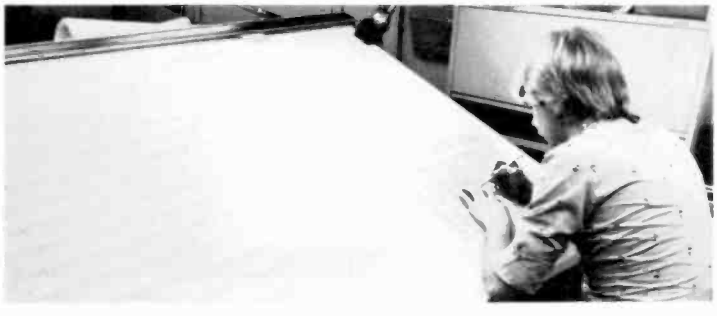
End of Simulation

2 Before committing a circuit to production, simulation tools can test and refine the engineer's suppositions. After translating the schematic into a simulation language, interactive simulators are used to predict circuit behavior. RCAP, the circuit simulator, can display the value of various parameters, such as voltage, over a period of time at a given node. MIMIC, a logic simulator, can trace signals in a digital circuit and warn of possible problems such as hazards (the undesirable effect of the variation in response time of different devices in a circuit).



B. RCAP Output.

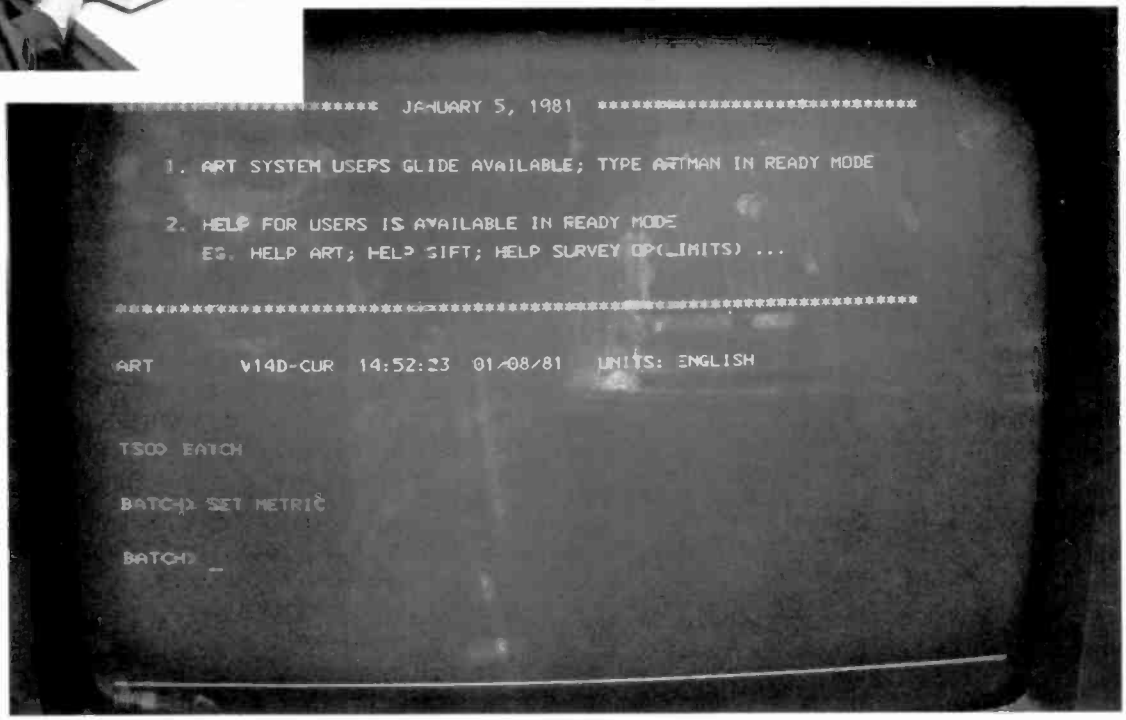
3 When the circuit is finalized, layout designers begin the task of translating symbols on the schematic diagram into mask artwork. Especially on high-volume circuits, silicon area or "real estate" is a precious commodity that designers are trained to conserve. Here a designer adds labels to the artwork to improve recognition of important features.



4 Artwork is captured or "digitized" on an interactive graphics system, in this case an Applicon Super VLSI Design System. The location of an electronic "puck" on the large tablet (foreground) is detected and recorded by a computer and instantly displayed on the raster-scan cathode-ray-tube display (background). Once digitized, artwork is immediately accessible for corrections or modifications using the Applicon's raster-scan display and a pen-like stylus.

7 Once loaded on the 370, the artwork digitized on the Applicon can be accessed by the ART System either interactively to perform simple checks on in batch mode to initiate complex tasks such as CRITIC. CRITIC checks an entire IC artwork file against an English-like description of its design rules. It produces a complete report which explains all detected errors.

A. ART System timesharing.



(a)

5

Artwork files from the Applicon are transferred by magnetic tape to the Corporate Information (CISS) computer facility in Somerville, New Jersey.

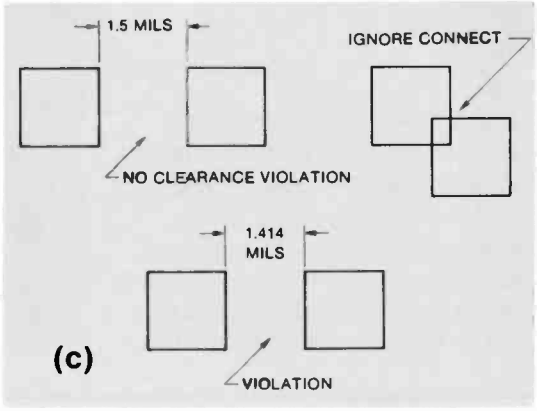
Artwork can also be transmitted electronically over local telephone lines. The corporate computers can be accessed through a vast network of remote terminals.

6

The Somerville computer center consists of two IBM 370/168 processors with large memory and on-line storage capabilities. The system in the foreground is host to the Design Automation ART System, a powerful set of tools for the analysis and modification of IC artwork.

B. CRITIC report.

C. CRITIC rule violation.




```
CRITIC    V13B-CUR  10:57:15  01/12/81   UNITS: ENGLISH

                                        Statement of Design Rule in CRITIC Language
<DESIGN RULE>  MASK2 CLEARS MASK1 BY 1.5 IGNORE CONNECT

               VIOLATIONS ARE IN DEFINITION  18 IN DATASET TSO582.ERRORS.DFL/0

Mask Levels
. MASK2    FIGURE 'A' LOCATED AT (    11.000,     1.000)
.
      WAS ORIGINALLY -
    P X11Y1 R1 B1 L1 T1

  * MASK1    FIGURE 'B' LOCATED AT (    10.000,     2.000)
      WAS ORIGINALLY -                                          Description of each Figure
    P X10Y2 T2 R2 B2 L2
                                                                Location of Actual Rule Violation
    *
    * VERTEX(    11.000,     1.000) IS     1.414   FROM SIDE(    10.000,     2.000)-(    10.000,     4.000)
    * VERTEX(    11.000,     1.000) IS     1.414   FROM SIDE(    12.000,     4.000)-(    12.000,     2.000)
    * VERTEX(    11.000,     1.000) IS     1.000   FROM SIDE(    12.000,     2.000)-(    10.000,     2.000)
    * VERTEX(    12.000,     1.000) IS     1.000   FROM SIDE(    12.000,     4.000)-(    12.000,     2.000)
    * VERTEX(    12.000,     1.000) IS     1.000   FROM SIDE(    12.000,     2.000)-(    10.000,     2.000)
    * VERTEX(    10.000,     2.000) IS     1.414   FROM SIDE(    11.000,     1.000)-(    12.000,     1.000)
    * VERTEX(    10.000,     2.000) IS     1.414   FROM SIDE(    11.000,     0.0   )-(    11.000,     1.000)
    * VERTEX(    12.000,     2.000) IS     1.000   FROM SIDE(    11.000,     1.000)-(    12.000,     1.000)
    * VERTEX(    12.000,     2.000) IS     1.000   FROM SIDE(    12.000,     1.000)-(    12.000,     0.0   )
    * VERTEX(    12.000,     2.000) IS     1.414   FROM SIDE(    11.000,     0.0   )-(    11.000,     1.000)

                NUMBER OF VIOLATIONS REPORTED:      1     Summary for this Design Rule
                TIME SPENT ON CHECK:      0 MIN     2 SEC
```

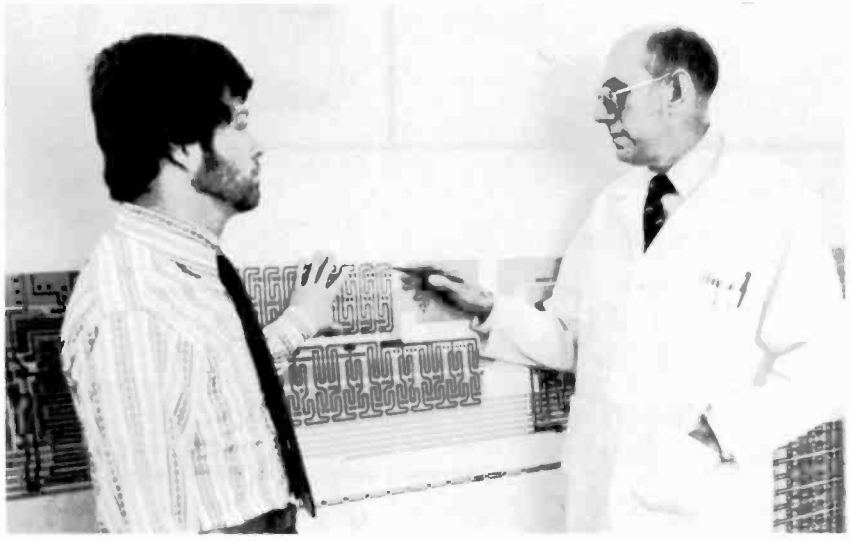
(b)

8

The ART program generates hardcopy output of a DFL file on a variety of graphics hardware including a Versatec 72-inch electrostatic plotter.

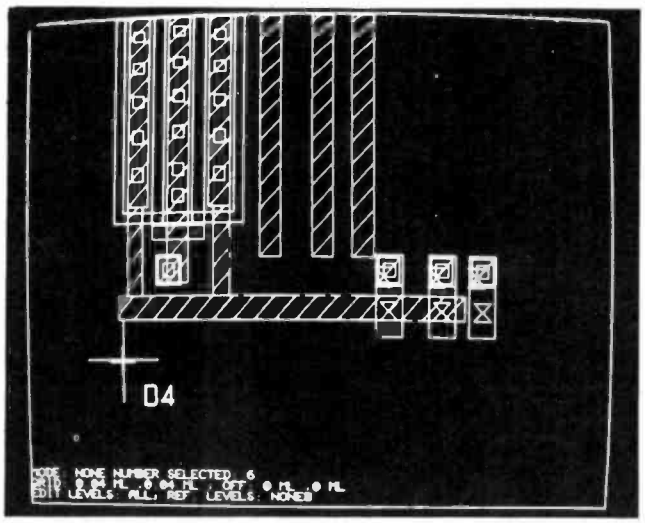
9

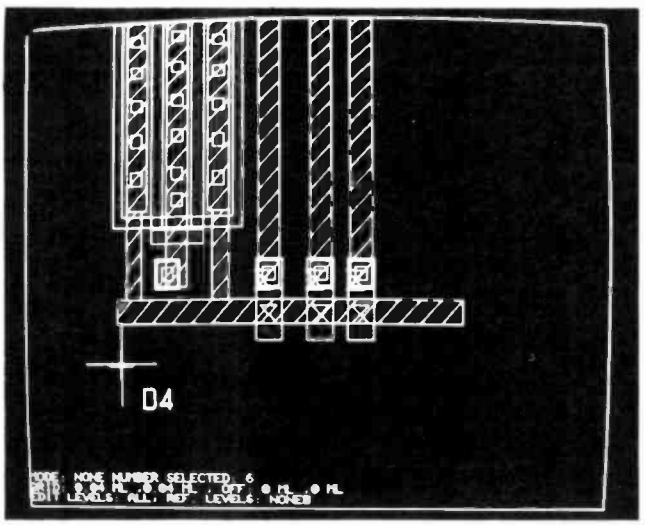
The Versatec can draw plots over 40 feet long and incorporate coded shading patterns to distinguish various mask levels. Shading and the capability for huge blowups permit quicker and easier detection of digitizing or layout errors missed by CRITIC.



10

When errors are discovered, the artwork file can be restored on the Applicon through magnetic tape. In this case, we wish to correct the location of three "tunnels" — silicon structures used to allow metal lines to cross underneath other metal lines. By selecting the figures displayed on the CRT using a tablet and stylus, and by specifying a new location, our correction is quickly effected.

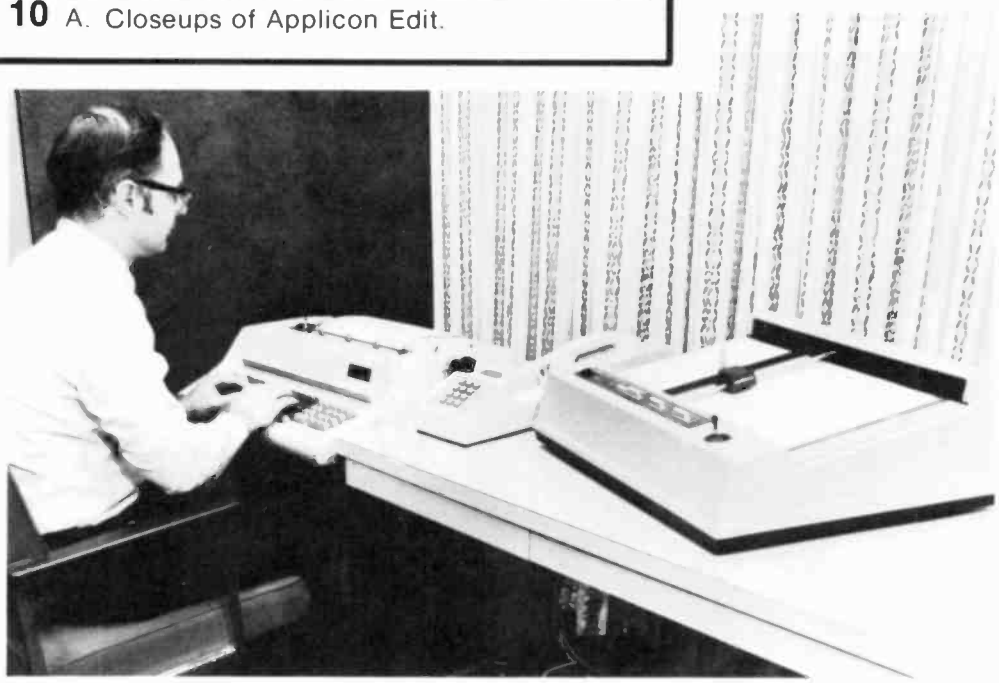


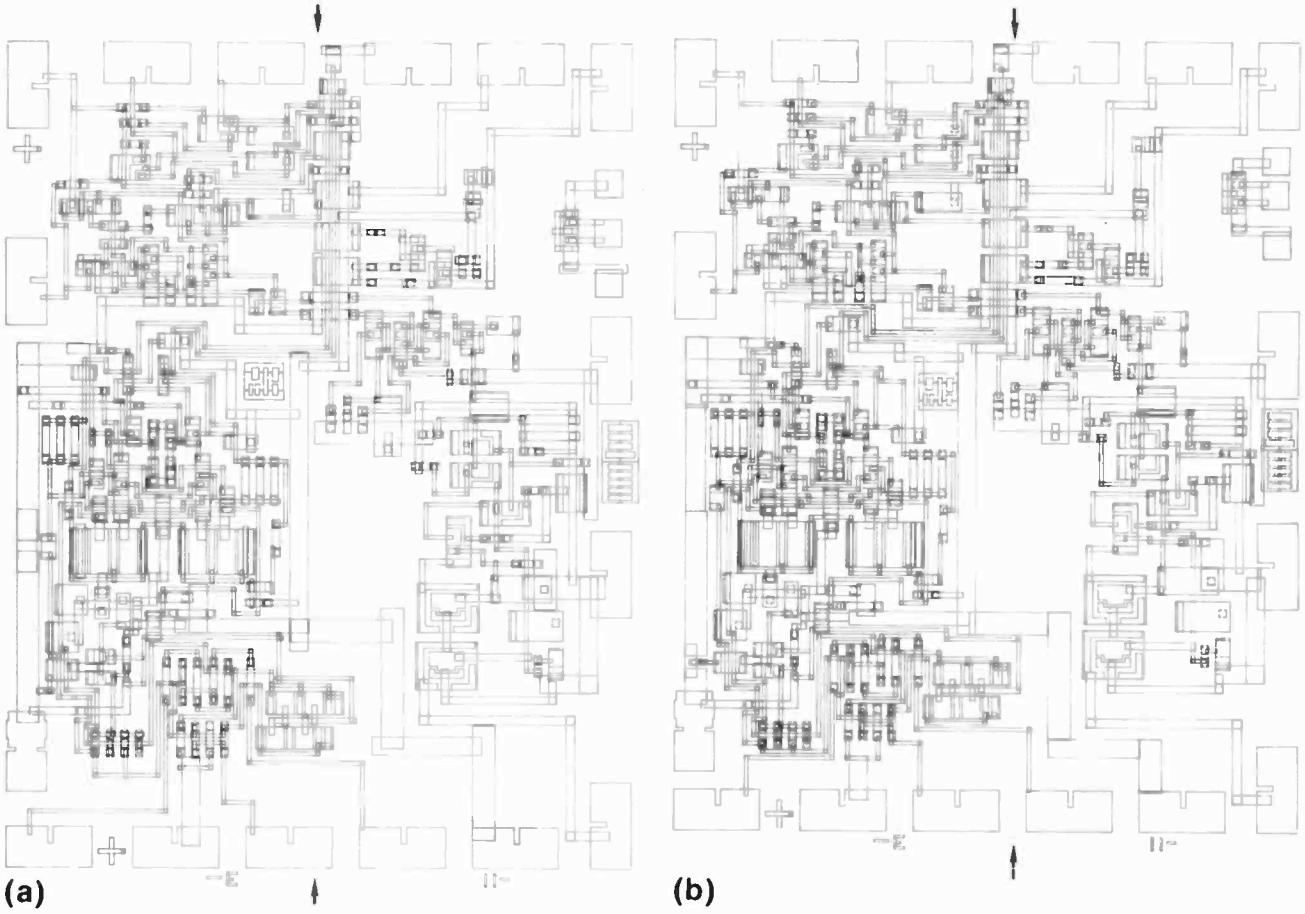


10 A. Closeups of Applicon Edit.

11 Close interactions between designers and CAD developers are common in Somerville. In addition to giving the design community a source for consultation on advanced capabilities, they provide Design Automation with numerous contacts to discuss future plans and test research projects.

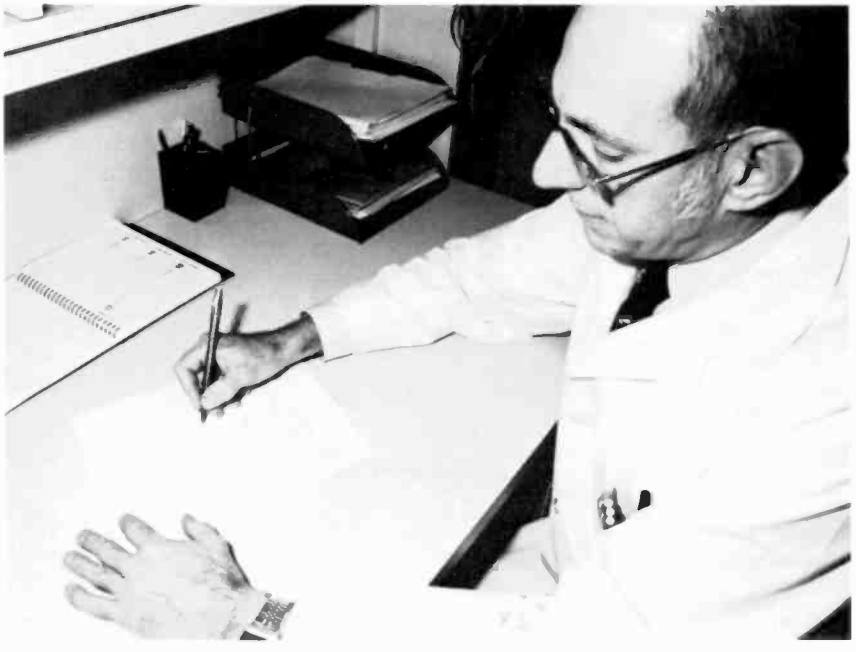
12 One advanced capability is computer-aided layout compaction. Artwork is squeezed in a given direction automatically, while obeying a set of given design rules. Results of layout compaction experiments can be displayed on interactive plotters such as the Tektronix 4662 connected directly to the 370.





(a) (b)

12 *(cont.)* Layout compaction experiment. A two minute computer run on an IBM 370/168 compressed Figure A in the *y* direction (arrows) resulting in Fig. B. This small space savings eliminated almost two man-months of manual editing.



13

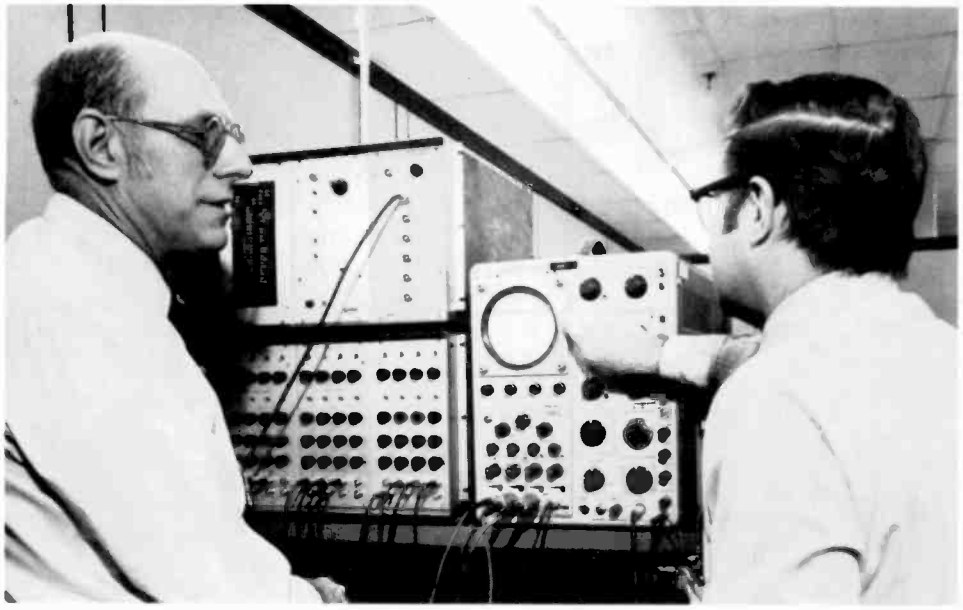
When all corrections and modifications have been made to the artwork, a mask set is requested. The engineer fills out a simple form to direct the submission of a batch job that generates the information needed to produce a mask.

14 The ART System writes a tape which will drive the ETEC Manufacturing Electron Beam Exposure System (MEBES) located in Somerville, New Jersey. ART also automatically generates all the documentation required by the photomask lab.

15 The MEBES itself is controlled by a minicomputer and uses the tape generated by the ART System to direct the exposure of a chrome plate with a 0.25-micron-wide electron beam.

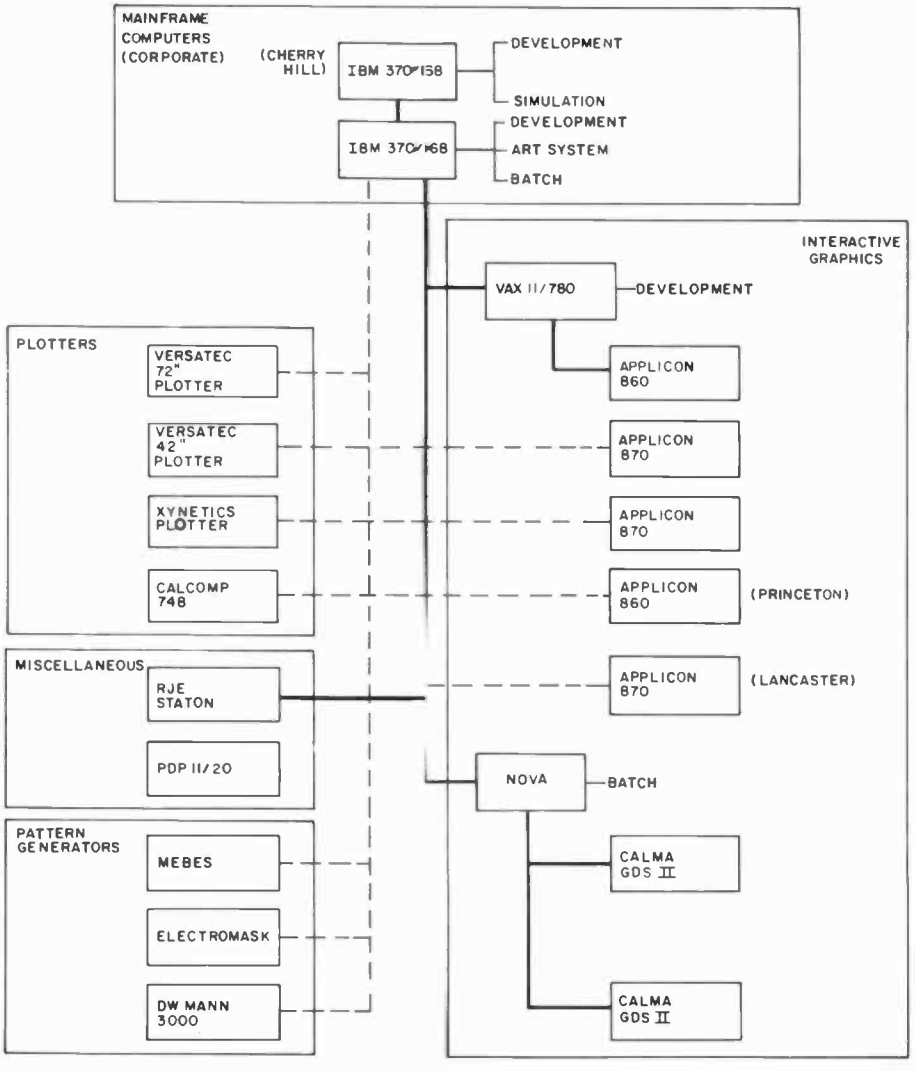
16 A MEBES-produced mask set is then used to fabricate integrated circuits on silicon wafers. This complex procedure relies on microcomputers at many steps to monitor processes and to aid in inspection for maximum quality control.

17 Wafers are subjected to electrical tests by automated test systems such as the Keithley System 2. Results of these tests can be analyzed to influence future design revisions and to refine processing steps.

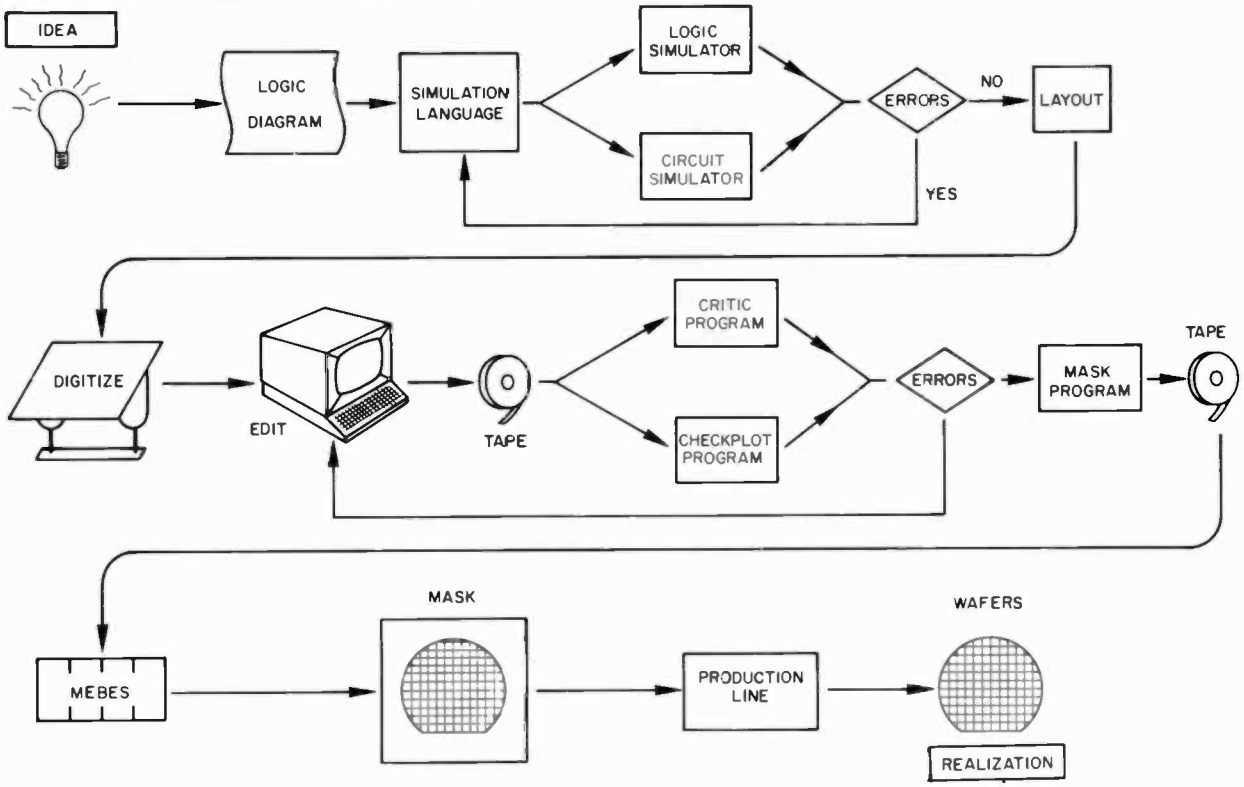


18

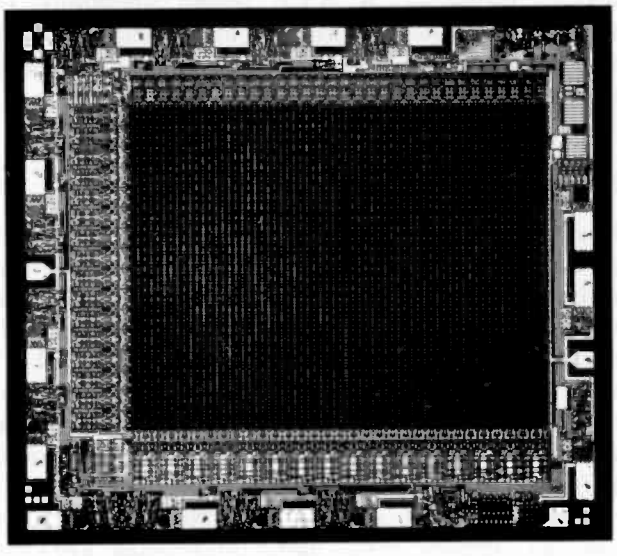
Completion! Working samples are tested by the design team and output waveforms are compared to those predicted by simulation programs. The next step is delivery of working parts to customers.



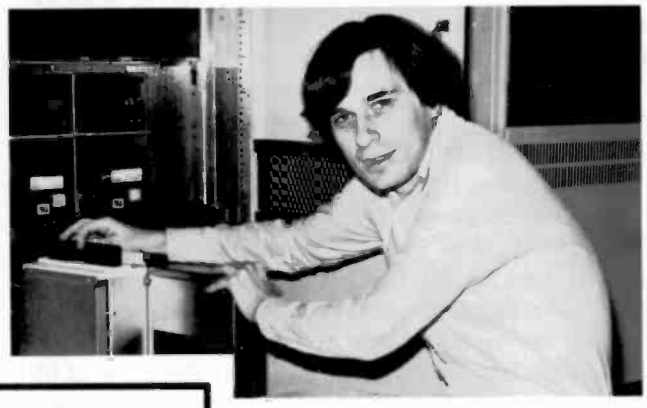
Dimensions of CAD in SSD and SSTC. RCA has invested well over $2,000,000 in CAD tools (not including mainframe computers). Recent additions include two Calma GDS II interactive graphics systems and a Digital Equipment Corporation VAX 11/780 superminicomputer.



From idea to realization: CAD's ability to allow the detection and correction of errors — before production — increases the chances of building ICs "right the first time."



The finished product: Photomicrograph of a completed IC.



Louis Judice, an Associate Member of the Technical Staff in the Design Automation department of the Solid State Technology Center, joined RCA in 1978. His current responsibilities include investigation of interactive techniques for VLSI chip planning and routing, and the development of a CAD minicomputer facility based on a Digital Equipment Corporation VAX 11/780. He has also taught RCA CEE course *C51 Introduction to Microprocessors* and he participated as an instructor in RCA's Minorities In Engineering Program.

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R.A. Auerbach

CRITIC highlights errors in IC-mask artwork

After creating computerized artwork, the designer can obtain a checkplot for visual inspection. But the computerized CRITIC design-rule checking program, using the designer's geometrical rules, can check more quickly and thoroughly for errors.

Abstract: *Checking IC-mask artwork for errors is a tedious job made simpler by using computer aids. RCA IC designers use the CRITIC program to methodically analyze mask artwork and identify potential trouble spots, which they then check manually.*

The complexity of integrated circuits (ICs) has long ago overwhelmed the designers' ability to manually check the mask artwork. Thus, for over nine years, they have relied on the CRITIC design-rule-checking program to search through the artwork and produce a mask subset containing only those polygons involved in violations.

At RCA, where IC technology abounds, it is important for the CRITIC program to be general in its problem-solving ability. This generality has always been a fundamental part of CRITIC (Computer Recognition of Illegal Technology in Integrated Circuits) and has led to its successful use by the diverse design community.

How does one make a program satisfy the needs of SSI (small-scale integration) through LSI (large-scale integration) complexity, linear or digital circuitry, bipolar or CMOS (complementary metal-oxide semiconductor) technology , SOS (silicon-on-sapphire) CMOS or bulk CMOS implementation, and so on? The solution chosen by the Design Automation department in Solid State Division was to look for the "lowest common denominator" that satisfies the apparently conflicting requirements. The department developed a program that performs simple geometric operations on polygons.

Soon after this program was developed, another aspect of the design-rule-checking problem surfaced. Program developers were concerned with the user interface to the program, i.e., the ability of a designer to translate his or her rules into a format understood by the program. Human engineering is an important consideration in developing any tool, whether it's a computer program or a hammer. In CRITIC's case, the addition of a user-input language that allowed rules to be specified in a simple and self-evident manner reduced the effort in mastering the program.

Today, CRITIC is a high-performance tool used routinely throughout RCA's IC design community. This paper discusses the two aspects, mentioned above, that made CRITIC successful: its general geometric checking capability and its powerful user interface.

Definition of terms

Before delving into exactly what geometric capability exists in CRITIC, the reader should understand some terminology. For the purposes of the computer, a *mask level* is simply a collection of polygons. The actual count of polygons per level can be as small as a few hundred or as large as many thousand. A *polygon,* of course, is a collection of connected line segments that enclose an area. A polygon comprises *vertices* that are the endpoints of the line segments.

The CRITIC program works with the vertices and from them can calculate certain useful information. For example, it can distinguish between the inside and the outside of a polygon, discern whether two line segments cross, or calculate the distance between a vertex and a line segment. Sophisticated checking capability is then built up from these very basic operations.

Complexity and computer costs

To simplify the rule checking, geometric tests are divided into two categories: checks performed on a single polygon and those performed between two polygons. When per-

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forming single-polygon checks, CRITIC need only analyze the vertices for one polygon at a time. The computer time required to perform such checks is a function of the number of vertices in the polygon, which usually is a relatively small number (between 4 and 125). The computer costs are proportional to the computer time and tend to be fairly low for the single polygon checks.

Checking complexity increases when CRITIC examines polygons in pairs. The formula that calculates the possible number of pairs (C) in a mask level containing N polygons is:

$$C = \frac{N(N-1)}{2}$$

Substituting some typical values for N, we find $C = 1225$ for $N = 50$, $C = 124{,}750$ for $N = 500$, and $C = 12{,}497{,}500$ for $N = 5000$. Even the powerful I.B.M. computers in RCA's Corporate Information Systems and Services (CISS) computer center would have a problem cost-effectively checking errors for all pairs in a complex mask level. Fortunately, algorithms exist which can reduce the value of C significantly and thus make the checking of pairs cost-effective. The details of the algorithms are beyond the scope of this paper.

Single-polygon design-rule checks

The simplest of checks, the single-polygon design-rule checks, involve calculating, for each polygon, either its width or its area. For each polygon, the narrowest cross section is considered its width, as indicated by the dotted lines in Fig. 1. Design rules often require that this width be greater than or equal to a minimum amount, so CRITIC's job is to report any instances where that is not true.

In some cases, a designer may wish to guarantee that a polygon have a minimum area and will, therefore, request that CRITIC calculate the area of each and compare it to a desired minimum. In Fig. 2, there will be three different results depending on whether only the minimum width is checked, or only the minimum area, or both. The check for only the minimum width flags polygon C as an error; the check for the minimum area flags polygon B; and the check for both minimum width and area flags B and C. In all cases, polygon A is correct.

Design-rule checks on pairs

Designers commonly refer to design-rule checks on pairs as "level-to-level" checks since often one level is being checked against another. CRITIC examines each pair and determines first the geometric relationship between the two polygons and then the minimum spacing between them.

The various geometric relationships are illustrated in Fig. 3, which shows all of the possible ways that polygon A can interact with polygon B. Briefly, the definitions for each relationship are:

clearance—polygons are totally disjoint

butt—polygons touch along an edge or a vertex

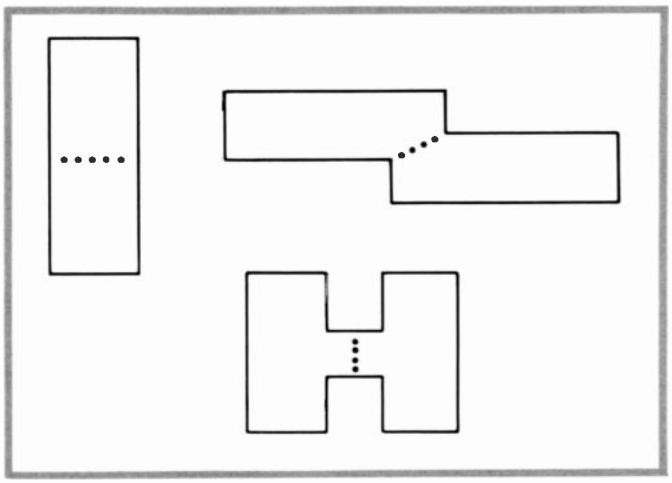

Fig. 1. Dotted lines show the minimum width of each polygon. This cross section must be greater than or equal to the minimum width design rule; otherwise, a violation exists.

overlap—polygons share some common area

inside—one polygon's area is totally covered by the other's

contain—one polygon's area totally covers the other's

identical—polygons are totally equivalent.

These definitions are intuitive and, thus, make the task of writing design rules very easy.

Our understanding of the concept of minimum spacing is also very intuitive. Different classes of spacing are recognized depending on the geometric relationship between the polygons. Figure 4 depicts the four most common types, and the dotted lines indicate where the separation distance is measured.

Determining the geometric relationship, comparing it to the user-specified relationship, reporting any discrepancy as an error, measuring the separation distance, and comparing it with a user-specified value all comprise a level-to-level design-rule check. Figure 5 shows a flowchart of this logic.

The reader should now have some notion of CRITIC's basic capability and should also have noticed an interesting fact: we mentioned nothing about integrated circuits. This

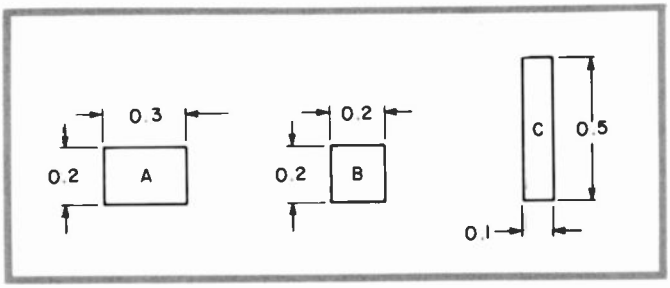

Fig. 2. Polygons undergoing minimum-width check. Polygon A passes the minimum width and area checks; polygon B fails the area check; polygon C fails the width check. For the above, minimum width is 0.2 mils and minimum area is 0.05 mils^2.

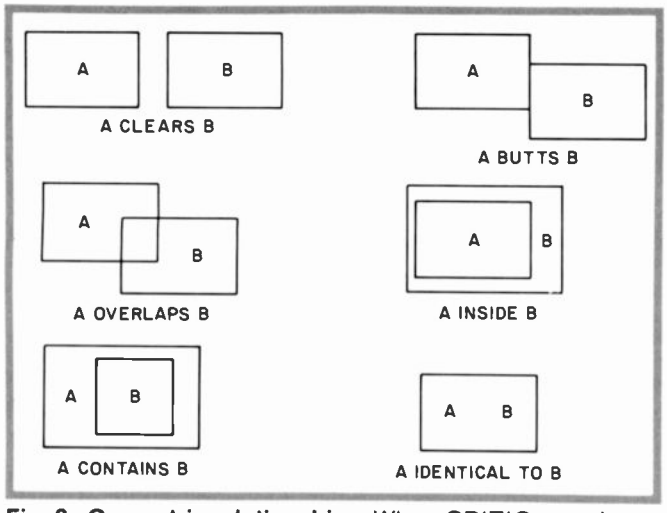

Fig. 3. Geometric relationships. When CRITIC examines a pair of polygons, it determines which of these geometrical relationships applies.

"oversight" highlights, in an indirect manner, the claim that CRITIC is a general-purpose geometric checker. Nothing in the above description indicates that the program is restricted to specific rules for a specific technology. We can now shift our attention to a discussion of the user interface.

User interface: the input language

An important goal in developing the interface was to make the input language easy to use and easy to understand, for the novice as well as the expert. Once accomplished, this "easy" input language would encourage designers to share experience and techniques. In fact, this did occur.

Three basic statements in the CRITIC language cover the capabilities described in the previous sections. A user encodes the rules for a technology using these statements and enters them into a data file on the computer. Once a high level of confidence is reached for a set of rules, then others designing in the same technology need only reference the data file.

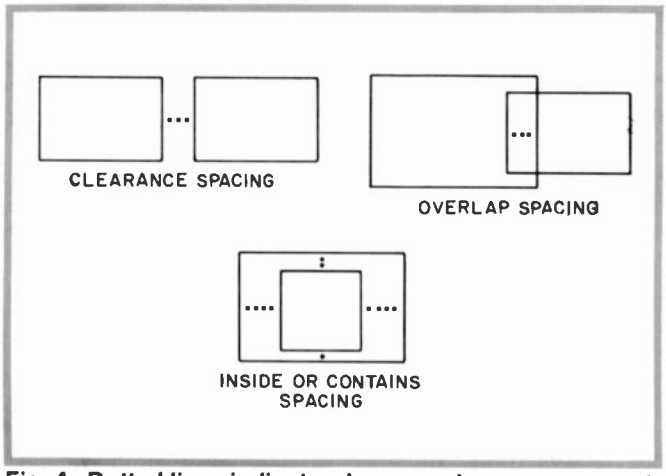

Fig. 4. Dotted lines indicate where spacing measurements are made. Depending on the geometrical relationship desired, CRITIC measures the spacing between the pair of polygons.

Level statement

The CRITIC level statement serves a dual role: it identifies which mask levels are to be checked and it allows the specification of the minimum width and area check for the levels. In addition, a useful feature provided by this statement is the ability to attach a name to a mask level that normally is referenced by an impersonal number. The name, as opposed to the number, makes the rule self-documenting and understandable by those not familiar with a technology's mask-numbering scheme.

An example of this statement for the mask level, shown in Fig. 2, is the following:

BOXES are level 35 width .2 area .05

Of course, this is a fictional rule, but it illustrates how one would check a fictional level 35 where polygons are required to have a minimum width of 0.2 mils and minimum area of 0.05 square mils.

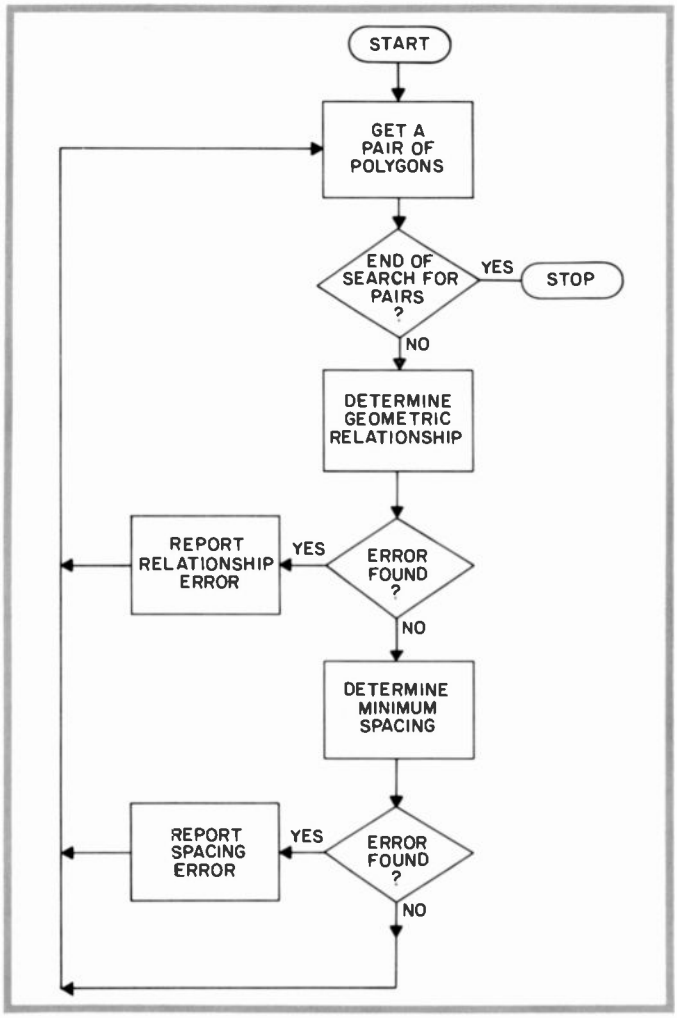

Fig. 5. Flowchart of level-to-level check. CRITIC first determines which geometrical relationship applies before it does the spacing check.

Polygon-extraction statement

Very often two or more rules may be applicable to only one mask level. In these cases, the program must separate the set of polygons on that mask level into many subsets that then can be checked with different rules. For example, imagine another fictional level called FLAVOR comprising MINT polygons and CHERRY polygons. Since a different rule applies to a MINT than to a CHERRY, the FLAVOR level must be divided into two subsets. If we can find a geometric relationship that one subset obeys and the other does not, then the extraction statement provides the tool to create the subsets. How is this done? The answer is best given with an illustration using these fictional levels:

Suppose that in this technology, MINT polygons always fall inside one of the polygons on the BOXES level while the CHERRY ones do not. If this is the case, then the necessary geometric distinction between the two subsets exist, and the extraction statement can create the subsets with the following statements:

MINT is defined FLAVOR inside BOXES

CHERRY is defined FLAVOR not inside BOXES

In addition to creating sublevels, the extraction statement can perform minimum width and area checks in a manner similar to the level statement.

The above example used the inside relationship; however, all six of the geometric relationships are valid in this statement, making this a very powerful and flexible capability.

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Level-comparison statement

This third statement allows the user to specify the level-to-level checks discussed earlier and illustrated in Fig. 5. Its usage is best revealed through examples. So far, the examples have introduced two mask levels, BOXES and FLAVOR. Furthermore, FLAVOR was divided into two subsets referred to as MINT and CHERRY. The only checking performed on those levels has been a minimum width and area check.

Now, it is desirable to perform some level comparisons. For example, this fictional technology requires that all MINT polygons be inside one of the BOXES polygons by a minimum spacing of 0.1 mils. That rule is written as:

MINT inside BOXES by .1

A second rule requires that CHERRY polygons clear MINT polygons by 0.2 mils and clear themselves by 0.1 mils. Those rules, in CRITIC language are:

CHERRY clears MINT by .2
CHERRY clears CHERRY by .1

All of the geometric relationships are valid in this statement although the minimum spacing requirement may not have any meaning for some.

By now the reader should have a good sense of the "flavor" of CRITIC's language and how one encodes design rules. Many more checking features exist, but are not presented in this paper.

Conclusion

Since its introduction nine years ago, CRITIC has evolved into a powerful and productive tool. In 1974, when an article on CRITIC first appeared[1], computerized design-rule checking was in its early stages. Today, it is considered a mature and stable field. Research is now turning to a new problem first posed by early CRITIC users: computerized correction of design-rule errors. Until that problem is solved, CRITIC will remain well entrenched in the IC-design cycle.

Reference

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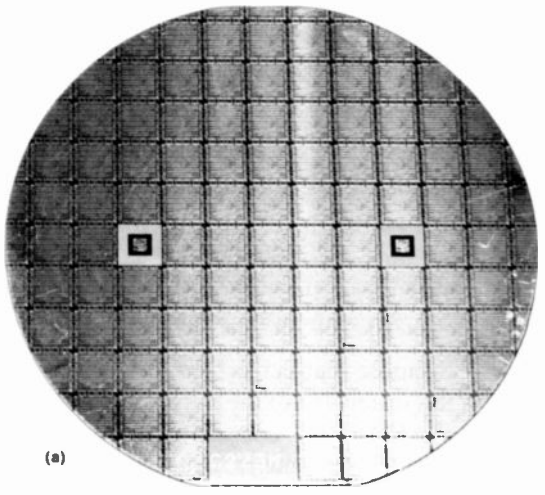
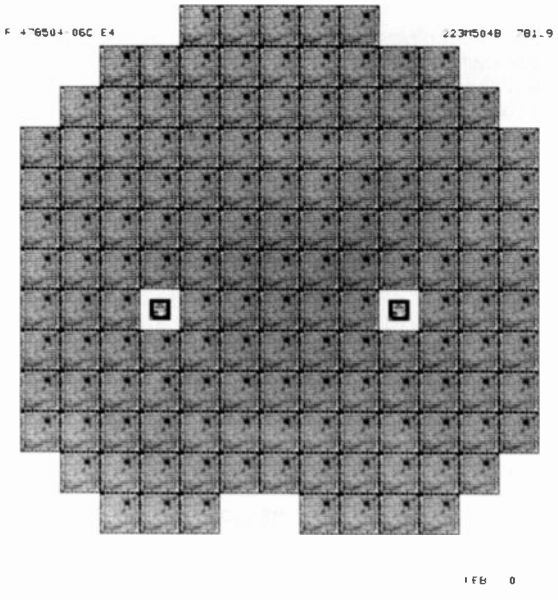
H. Rifkin

MASK automates mask making for wafer exposure

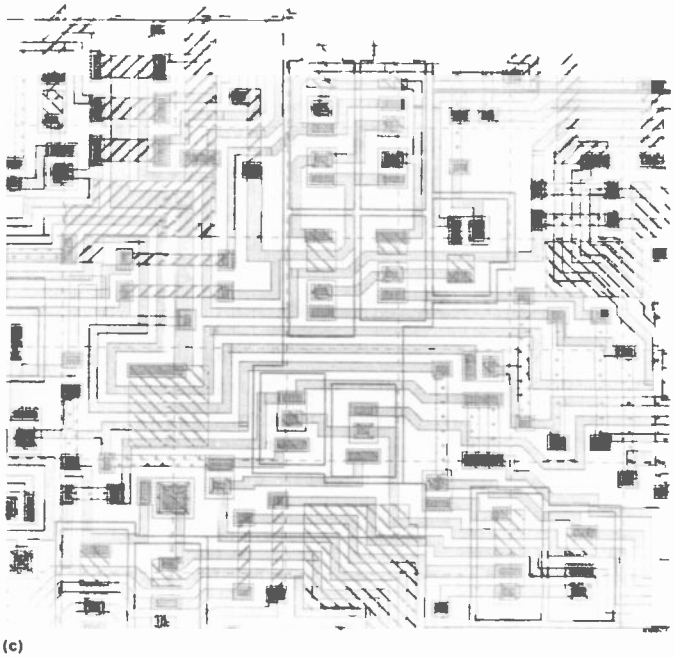
Once the computer-aided design is finished, the MASK programs help a pattern generator or MEBES convert them into a set of masks for actual IC production processes.



(a)



(b)



(c)

Fig. 1. (a) Wafer, (b) Mask, (c) Checkplot.

Before an integrated circuit (IC) can be produced in the factory, the designer must convert it from a computer-aided-design (CAD) representation into a set of masks that can be used to expose the wafers. A mask contains the photographic image of one level, or step, of an IC (Fig. 1). Depending upon later processing steps, a mask can be a positive image (opaque devices with the unused area clear) or it can be a negative image called "reverse tone." The mask is used to photolithographically expose the wafer in the factory. A wafer not only contains the "micro" images of the chip but also contains test devices and humanly readable information.

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Abstract: *The author describes, step-by-step, the MASK system used to automate the production of IC masks from computer-aided design layouts.*

Presently, a mask can be made in one of two ways. The first of these is to use a machine known as a pattern generator (PG). The PG will expose a single, 10X image of the chip on a glass plate known as a reticle. This reticle is then combined with the reticles of the test chips on a step-and-repeat machine that optically reduces the image and produces the multiple exposures. The other method is to use the Manufacturing-Electron-Beam-Exposure System (MEBES) to directly expose the 1X multiple images on the mask, using an electron beam instead of light.

Both of these methods require the following steps. The artwork must be converted from the CAD language into a format understandable by the pattern generator or MEBES. To verify that there were no conversion errors and that no data was somehow lost, this machine-readable format should be converted back into the CAD language and then checkplotted. A separate machine-readable file must be produced to get the step-and-repeat machine or MEBES to produce the correct mask layout. Finally, a descriptive work order, or request form, should be filled out and given to the Photo Technology Operation (PTO).

The SSTC Design Automation department has created programs to perform each of the above functions. A user could execute each step individually, supplying each with the information needed. But each step requires information that ranges from a little to a lot, much of which is common to all of them. Therefore, supplying this information a number of times tends to be error prone and time consuming. Additionally much of the information, such as test devices used, is common to all chips of a particular technology. So the MASK program was created to automate this process, to supply a way of storing technology-dependent information, and thereby to diminish the probability of error.

The MASK system

MASK combines the above tasks into three basic functions. These are: formatting and deformatting the pattern-generator tape, generating a control tape for the step-and-repeat machine, and creating a request form (Fig. 2). Since the main pattern-generator program is called MAP (Master Artwork Program) and has been around for several years, the process of creating a pattern-generator tape is known as MAPping. Similarly, since the step-and-repeat program is known as SANDRA (Step-AND-Repeat Array), the step-and-repeat generation step is known as the SANDRA step.

One of the features of MASK is that it frees the user from the need to answer a great number of questions. Most of the information needed to make a mask, such as levels, test devices, types of glass and other processing options, are fairly standard for a given technology. So MASK was designed to read this information from what is called a Technology File. Then, it just needs to ask for information which will change from chip to chip (Fig. 3).

When an IC is produced, one of the parameters needed is the step-and-repeat size. This is the distance from one chip to the next on the wafer. Because of limitations with the machines that cut the wafers into chips (known as scribers), this distance must be an even number of mils. The terms

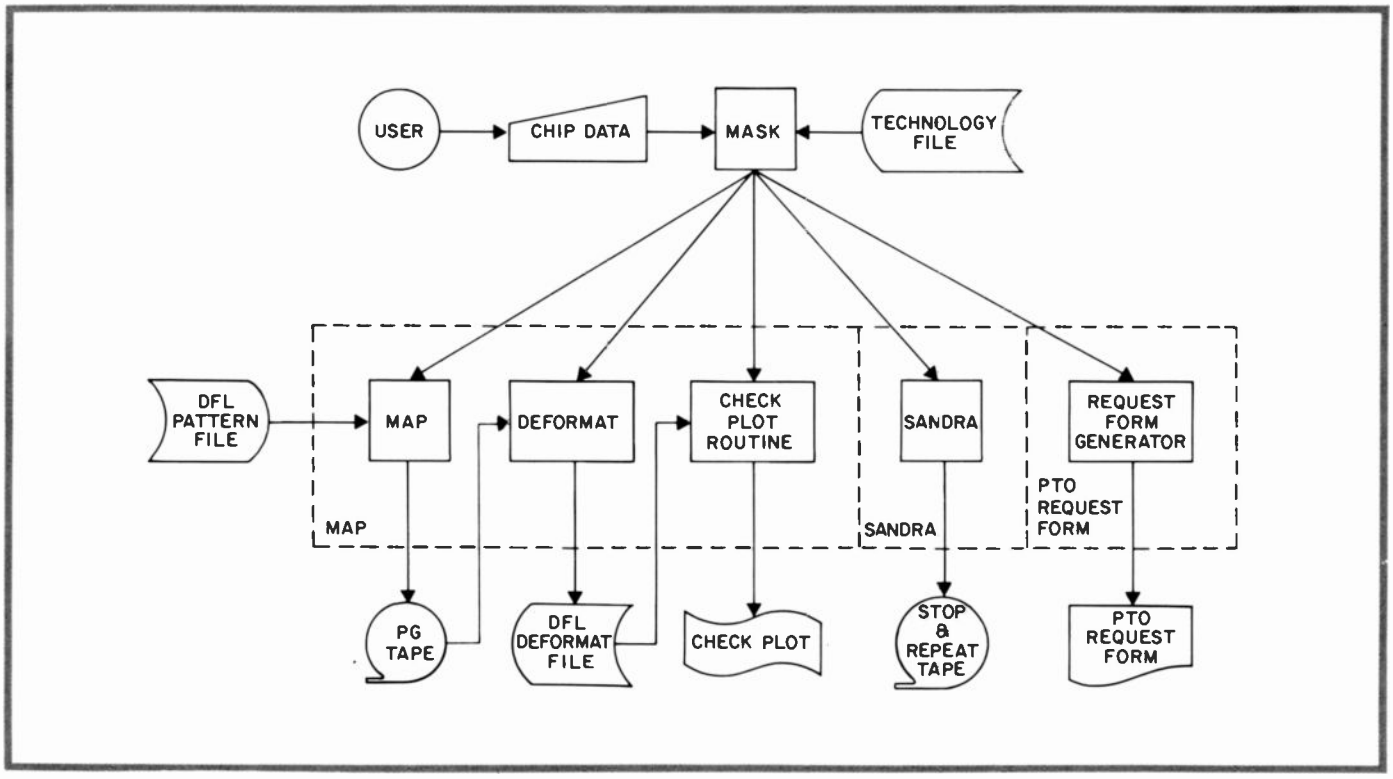

Fig. 2. Diagram of various steps in MASK showing the three functions.

```
   MASK              V036          05/19/81   10:36:38
DO YOU WISH TO RUN SANDRA? YES
DO YOU WISH TO CREATE A PMO REQUEST FORM? YES
DO YOU WISH TO RUN MAP? YES
ENTER THE LEVELS TO MAP FOR THIS RUN: 1-6
NAME YOUR TECHNOLOGY FILE. TS0631.CMOS1.FR11082.DATA
CHIP LEVELS: 1-6
DOES YOUR FILE CONTAIN A BORDER? NO
DO YOU WISH TO HAVE A BORDER GENERATED? YES
DO YOU HAVE A STANDARD BORDER? YES
BORDER: CSSD
NOM LOWER CORNER: 0,0
NOM STEP AND REPEAT SIZE: 138,137
PATTERN GENERATOR SCALE: 1
DEVICE NO: TA10128B
DRAWING NUMBER: 24788739
REQUESTED BY: RIFKIN
JOB TYPE: NEW
DEPARTMENT: 632
ALIS NUMBER: 10128B
PHONE EXT.: 6926
SHIP TO: RIFKIN
ARE ANY OF THE LEVELS REVISIONS? NO
DO YOU WISH TO ADD TO OR OVERRIDE ANY OF THE
INFORMATION IN THE TECHNOLOGY FILE, OR
CHANGE ANY OF THE INFORMATION ENTERED?  NO
NAME OF FILE TO BE SUBMITTED TO MAP? TA10128B.DFL
P.G. TAPE: A00384
VERSATEC SCALE: 250
CLASS: DAY
CPU TIME: 3
VERSATEC TAPE: A00384
```

Fig. 3. A typical MASK run.

"street," "scribe line," and "border" are synonymous and signify a special area, set aside for the scriber to cut-in. Two other numbers are important to the scriber: border width, which is the dependent on the scriber being used, and the distance between the inside of the scribe line and the active area. This distance must be some minimum distance so that any fracturing caused by breaking the wafer along the scribe line will not reach the active components. One of the programs associated with MAP, which will be described later, will automatically generate a border for a chip, given these three numbers.

After a chip has been in production for a while, however, it is sometimes desirable to shrink it so that more chips can be placed on a wafer. This shrinkage is described as a percentage and is usually 10 percent. If the step-and-repeat size is just simple-mindedly shrunk by 10 percent, there is a high probability that it will no longer be an even mil. The best solution to this is for MASK to automatically correct the unshrunken (nominal) number either up or down so that, after the shrink, it will come out to an even mil. Given the nominal number, the shrink, and the final step-and-repeat size, MASK will find the new nominal values. To ensure that the distance between the border and active area remain correct, MASK will also re-center the border surrounding the new size.

The first step in the MASK routine is to ask the user which of the three functions are desired. Although we prefer that SANDRA, MAP and the PTO request-form generator be run at the same time, this is not always possible, or desirable. Next, MASK asks the name of the technology file. It asks for the levels to be processed and then for all of the chip-dependent information. After this information has been read-in, MASK performs its special processing, dealing with the English-to-metric conversions and borders. Then, it collects the information into a large data file that SANDRA and the request-form generator can read. MASK also sets up all the parameters needed to run MAP and execute the other programs. Finally, it creates a control file to run the various programs, and submits a background job to do the actual work.

The MAP program

The first program to be executed is MAP. There are really five subtasks lumped under the heading of MAP, but only three are performed by the MAP program. These three are: border creation and insertion, "smashing" (or cutting) into trapezoids for MEBES or rectangles for the PGs, and formatting in the MEBES or PG language. The remaining two functions are deformatting and checkplotting.

The first subtask is to create and insert borders (or outlines) into the chip artwork. These borders are used to separate one chip from another on a mask and to provide space for the scriber or cutter to use in separating the chips. To calculate the proper size and placement of the border artwork, the program uses the lower corner, the border width, and the step-and-repeat size. The artwork for the border is then merged with the chip artwork into a new file.

The CAD language (DFL) is basically a hierarchical language where a group of associated figures can be grouped together into a definition and then, whenever these figures are needed, only the definition name need be placed in the file. This arrangement is used to save space in the file, but the smashing program needs to see the actual figures in their locations rather than the definition name. Therefore, the border information is merged into the file, *and* all definition calls are replaced with the proper artwork.

The next step is to take the general polygonal shapes of the artwork and smash, or cut, them into primitive four-sided figures, which can be either trapezoids for MEBES or

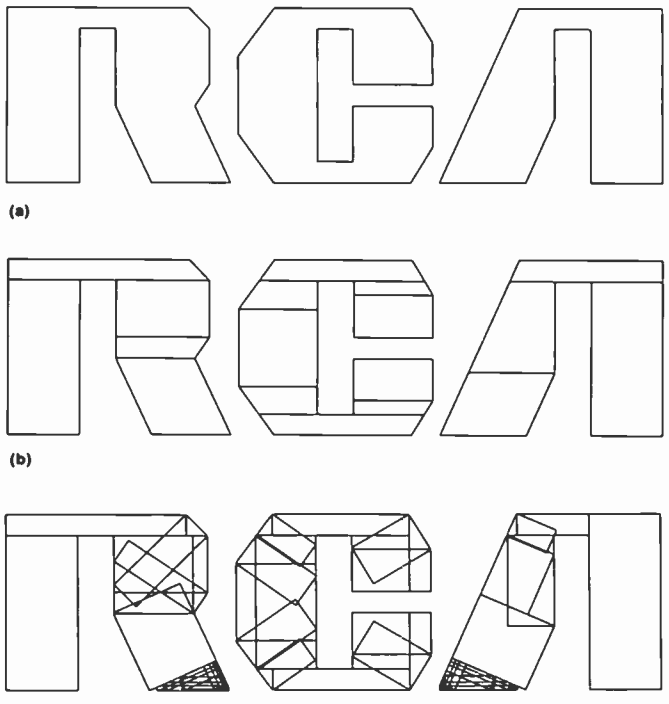

Fig. 4. (a) Some general polygons; (b) those same polygons cut into MEBES trapezoids; (c) and polygons cut into PG rectangles.

rectangles for the PGs (Fig. 4). For the MEBES, a trapezoid is defined as a four-sided figure with a horizontal top and bottom (a triangle is just a trapezoid with a null- or zero-length top or bottom). A rectangle for the PG machines is a four-sided figure which may be rotated to any angle. Any polygon can be cut into one of these. It can be cut into trapezoids by taking each corner — one-by-one — and drawing a horizontal line through it. It is somewhat more difficult to cut a general polygon into rectangles but a minimum covering set can be found.

Finally, these primitives are formatted into the MEBES, or PG language and written onto a magnetic tape. In the MEBES language, a trapezoid is described by its lower left corner, a height, a width, and the slopes of the sides. Rectangles are considered a special case and only need a corner, height, and width.

In the various steps of MAP, a number of problems can occur that would not be detected until a mask is made. These problems can be caused by incorrect specifications or by a program bug. In order to spare the user the expense of making a mask containing an error, designers use a program that translates, or deformats, a file from the MEBES or PG back into DFL. Once this DFL file has been recreated, it can be checkplotted and then compared with the original file, and the user's expectations.

The SANDRA program

Once a chip has been converted into MEBES language and has been placed on tape, or once a reticle has been made, the next step is to make a mask. In general, a mask is an array of chips roughly in the shape of a wafer, but close inspection will show that it also contains test devices and several label fields. Even without these complications, creating a roughly circular array (a wafer is a circle with a small area called the "flat" clipped off the bottom) of a given size from a given step-and-repeat size and at the same time maximizing the number of patterns within the wafer and minimizing those outside, is a non-trivial task. In addition to placement of information on a mask, such parameters as the tone geometry, scale, resist, and mask material must also be specified. All of this is what the SANDRA program was developed to do.

The label information falls into two categories: information that appears only on the mask, and information that will also appear on the wafer. The label information that appears only on the mask — the pattern name, drawing number, level and mask material — is used to identify the mask in the factory, and to order new masks. In order to identify the wafer as it is being processed, the pattern name is also placed on the wafer so that it can be plainly seen at arm's length. This identification is known as the ALIS (Arm's-Length-Identification-System) number. Finally, each mask has its level number placed in a designated location in the wafer area. Thus, as the wafer is being processed, it can be seen which levels have been done.

Once a wafer has been processed, only about half the cost of making the chip has been spent. The rest of the cost is used to test and package the chip. It is expensive and time consuming to test each of the chips on a wafer circuit probe, and to package and then test them, so at certain locations on the wafer, the chip pattern has been replaced with a pattern that contains a few simple devices that will be tested first. The rationale is that if these simple devices do not work, there is a good chance that there was a problem in processing and that none of the more complex chips will work. These test keys are also used for process characterization and control.

All of this information is described to the MEBES in a special file, or to the step-and-repeat machine in a file, or a tape. This file deals with the placement of chip information on the mask. SANDRA has a number of standard mask layouts from which the user can choose. These layouts contain the locations and the number of the test chip, the shape of the array, and the location of the ALIS number and level IDs. One of these can be chosen and specified or, if the user wishes, he can specify a custom array by giving SANDRA a graphical representation of how the wafer should look. In either case, SANDRA will calculate the position of each chip on the mask and place this in the file. The ALIS number and level IDs are characters, and are generated by taking a small square and stepping it on the mask in the shape of the characters. All of this information is added to the end of the MAP tape and is also printed for the user to check.

The PTO request form

Finally, once the user has his tape with a SANDRA file on

PHOTOMASK TOOLING ORDER

DEVICE NO: TA10128B
DWG NO: 2345661
ALIS NO: 10128B
DIAG KEY 1: 247346
ARRAY DWG NO 183199619A
DIAG KEY 2:
DIAG KEY 3:

PRODUCT LINE: COS/MOS
JOB TYPE: TEST
PRODUCTION TYPE: CONTACT
P.G. TYPE: ETEC
P.G. TAPE: A00631
RETICLE REDUCTION:
RETICLE AMOUNT:

REQUESTED BY: RIFKIN
DEPARTMENT: 632
PHONE EXT: 6926
SHIP TO: RIFKIN
PHONE EXT: 6926
S&R MASK INSP: QA
PROD MASK INSP: TS

PMO SHOP ORDER NO:
DATE SUBMITTED: 03/02/81
S&R MACHINE NO:
DIE S&R: 120.00,120.00
MASK SIZE: 4.00
FLASHED AREA BIASED BY:
GEOMETRY: POSITIVE

LEV NO	REV	RET ID	LEVEL NAME	DIGI AREA	GRID	RUN TIME HRS	FLASH COUNT	T.GM CODE	S&R AMT	PROD MASK AMT	PROD MASK MAT	FOILS	H R OVER LAYS	DIAG KEY LEV	DIAG KEY REV	DIAG KEY CODE	SHIPPING AMT	SHIPPING DATE	SHIPPING COMP
1			WELL	OPQ	Y		289			3	L		1	1	B				
2	A		P+	OPQ	Y		2397			3	L		1	2					
3	B		N+	OPQ	Y		2272			3	L		1	3					
4	C		S.O.	OPQ	Y		2394			5	L		1	4					
5	D		CONT.	OPQ	Y		1574			3	L		1	5					
6	E		METAL	CLR	N		4213			3	L		1	6					
7			PROT.	OPQ	Y		91			3	L		1	7					

SCHEDULE: DATE SUBMITTED: SCHEDULE WEEK OUT: DATE: PMO APPROVED BY:

Fig. 5. A PTO request form.

it, he must only fill in the request forms and submit them to the mask lab to get his masks. But because most of the information on the form has been used by one of the previous programs, and as a means to fully automate the mask-making process, MASK executes a program which will generate a request form automatically for the user. This program reads the information from the data file and prints it out in the form of the official PTO request form (Fig. 5).

Conclusion

The goal of the MASK system was to simplify and speed up the process of mask making. For the majority of the users at the Solid State Division, this goal has been achieved. There are still improvements to be made. Work is now progressing in two areas. First, we must speed up the MAP program so that it can remain cost-effective for VLSI devices. Second, we must improve the flexibility of the SANDRA program to meet the needs of the new mask-aligning equipment.

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F. Borgini|R. Noto|B.A. Suskind

Automated Universal Array

With the trend towards ever-increasing functional complexities, and thus device counts, an automatic layout capability is mandatory for a viable universal array approach to achieve custom LSI designs.

Abstract: *The automated universal array (AUA) system is a new, minimum-cost approach for generating custom LSI devices. It incorporates a specially developed fixed-geometry design with an automatic layout program. Using this system, custom LSI devices can be produced by generation of a single unique metal level, with the interconnections determined and optimized automatically. This article describes the topological design of the AUA chip, the effectiveness of the fully automatic layout program, the description of a test chip metal pattern, and AUA characterization results obtained from the test chip. The preliminary efforts to develop a demonstration vehicle of an existing Army application will also be briefly discussed.*

The universal array, the gate array, the master slice, and the uncommitted logic arrays are all descriptors of a custom approach for LSI and VLSI devices in both the MOS and bipolar technology that is being used heavily in the computer, communication, automotive, and other commercial areas. Designs using these custom approaches require the user to define, in many instances, two or three levels of artwork information (generally bipolar) and one unique level (typically in the MOS technology). This approach presently relies almost exclusively on manual layout techniques, which frequently make extensive use of interactive graphic techniques. The manual layout of a semi-custom array becomes costly and time-consuming as gate counts and design complexities increase, thereby negating the attractiveness of this design approach. To alleviate this burden, the Automated Universal Array (AUA) system was developed.

The AUA system requires only one unique metal artwork level for any logic application, and the artwork for this level is generated automatically. The automatic layout software has proven very effective, achieving 100-percent connectivity, with gate utilization as high as 98 percent for complex random-logic applications.

The AUA was specially designed for single-level routing and compatibility with automatic layout techniques. It consists of a pattern of predefined, uncommitted, active components that provide for logic function implementation and chip interfacing, and a region of passive components and wiring areas used for logic routing. The design is equivalent to 800 two-input gates, but this basic approach could be expanded by a factor of 2.0 or 2.5 and still achieve the desired results. The AUA is designed with typically 4-μm channel lengths and 4-μm minimum poly-to-poly spacing.

The inherent advantages of the universal array approach include: wafer stockpiling; ease of design; ease of design change; low cost; rapid turnaround; standard process compatibility; and compatibility with other computer-aided design programs such as logic simulation, design rule checking, test generation, and artwork connectivity checking.

Array design

The design and layout of the basic array consists of four distinct areas. These areas include the basic internal cell, the basic peripheral cell, the internal interconnect region, and special circuits. The final design features of these areas are influenced by the requirements of the layout program and the results obtained from executed test cases. A summary of the final AUA design features is given in Table I.

Basic internal cell

The heart of the AUA is the repetitive internal cells that are combined to form logic functions and then interconnected via a metallization pattern to produce a chip design of some

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Table I. Automated Universal Array

One Custom Mask	Metal
Technology	Silicon gate CMOS/SOS
Size	208 x 208 mils
Feature Size	3.5 to 4 microns
Number of Basic Internal Cells	640
Number of Peripheral Cells	62
Routing Grid	10 microns (horizontal) x 12 microns (vertical)
Miscellaneous Peripheral Circuits	
Prescalar	2 stages
"D" FF W/reset	8 stages
Large Inverter	2
Level Shifter	1
Total Equivalent Gate Count	800 (3200 transistors)

logic application. The basic internal cell, shown in Fig. 1, has the following features:

- The basic cell is symmetrical. This means that logic patterns can be placed in a cell row with a normal orientation or it can be flipped 180 degrees around the y-axis.
- Each basic cell has a feedthrough capability. This allows signals to pass through a cell row.
- The basic cell has three internal wiring channels available. This will increase the probability that the layout of most individual logic functions can be generated via the internal channels. Therefore, the runway will be used almost exclusively for the routing of wire connecting the logic functions.
- A multiport capability is provided for all inputs and outputs.
- A provision has been made for multiple access at each input and output pin.
- The basic cell is an equivalent two-input gate function. The symmetrical nature requires a common source diffusion for the *n*-type and *p*-type transistors for area efficiency.

The most essential of the internal cell features is the provision for multiple access at each input and output pin. As presented in Fig. 1, each input and output has four direct-access points — two at the bottom and two at the top of the cell. Secondary access points are provided by the runway interconnect pattern. To assure 100-percent connectivity, with a cell utilization rate of greater than 90 percent, it is imperative that the cell input/output pins are not easily blocked.

The design dimensions of the basic internal cell are:

- Cell width 60 μm (2.4 mils)
- Cell height 120 μm (4.8 mils)
- Pin-to-pin spacing 12 μm (0.48 mil)
- Metal width 6 μm (0.24 mil)
- Power bus width 16 μm (0.64 mil)

The grid used for the basic internal cell design is 10 by 12 μm in the x and y directions, respectively. This grid provides a compatible grid structure with the AUA interconnect region. The basic cell height of 120 μm excludes the three horizontal wiring channels available on the top and bottom of the cell. The *n* and *p* devices are 46 μm (1.84 mils) and 48 μm (1.92 mils), respectively. The AUA contains 640 internal cells placed in 10 rows of 64 basic cells each.

The AUA system utilizes a library of logic functions containing one or more basic cells with the I/O pins

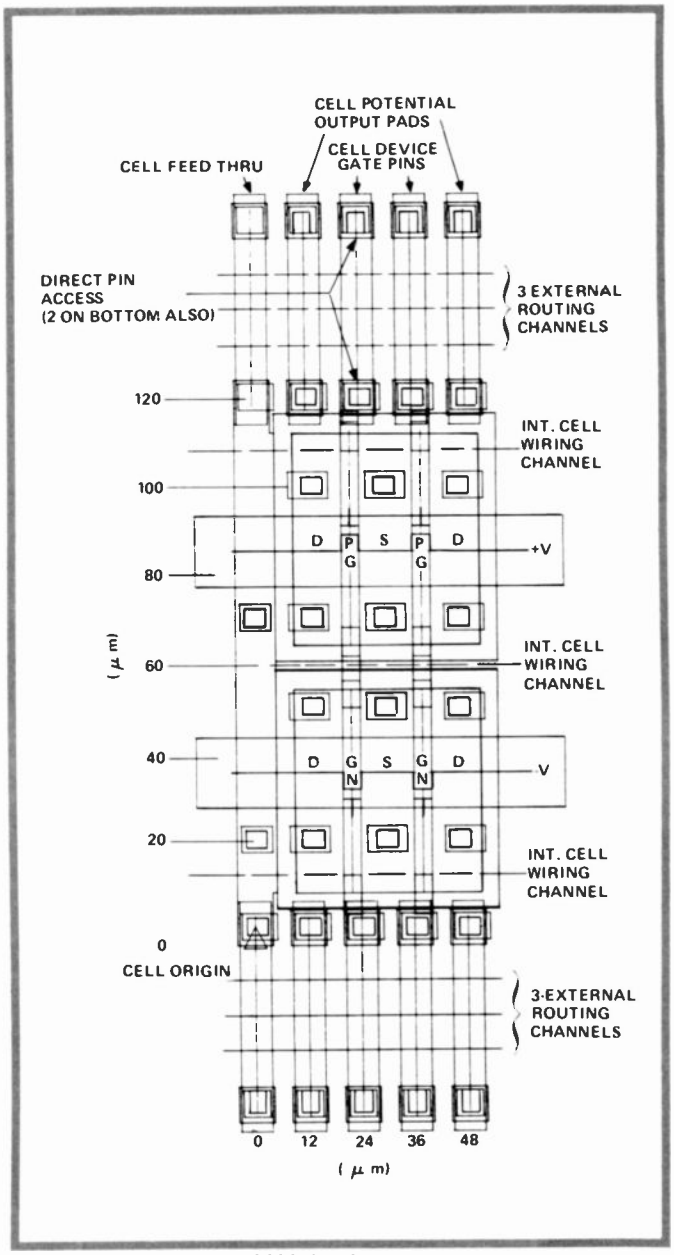

Fig. 1. Layout of an AUA basic internal cell.

identified to specify the target points for interconnecting the logic. In general, the logic cell, customized metal patterns are self-contained within the basic cell areas, but in some of the more complex functions it may be necessary for the layout program to finalize the design by automatically routing the customized metal in the runway area.

Basic peripheral cell design

The basic peripheral cell (shown in Fig. 2) will normally be used as an input/output cell that will interface off-chip. It is also possible to use the peripheral cells for on-chip usage if available. The peripheral cell design includes:

- Input protection circuitry (resistor, gated diode, and spark gap)
- Two *n* and two *p* transistors
- One *n* and one *p* high-impedance transistors
- Bonding pad
- Power distribution area
- Seven access pins for the routing program.

The above features are contained in an area of 200 x 450 μm (8 x 18 mils). The 8-mil dimension has been maintained to keep symmetry with the cell row and roadbed height and to maximize the number of bonding pads available. All of the component parts of the peripheral cell are uncommitted except for the high-impedance *n* and *p* transistors. These devices have one terminal committed to −V and +V, respectively. This provides for a high degree of flexibility in the design of interface functions.

The usage of the I/O cells is the same as the internal cells. This means that the AUA cell library contains I/O functions with their own pin data files. Therefore, the layout program will automatically place and connect the I/O functions.

The AUA contains two basic peripheral cell designs because of the interleaved power distribution buses. One basic design is located on the left side and top row of the chip, while the other design is located on the right side and bottom row. There are 62 peripheral cells placed around the four sides of the AUA.

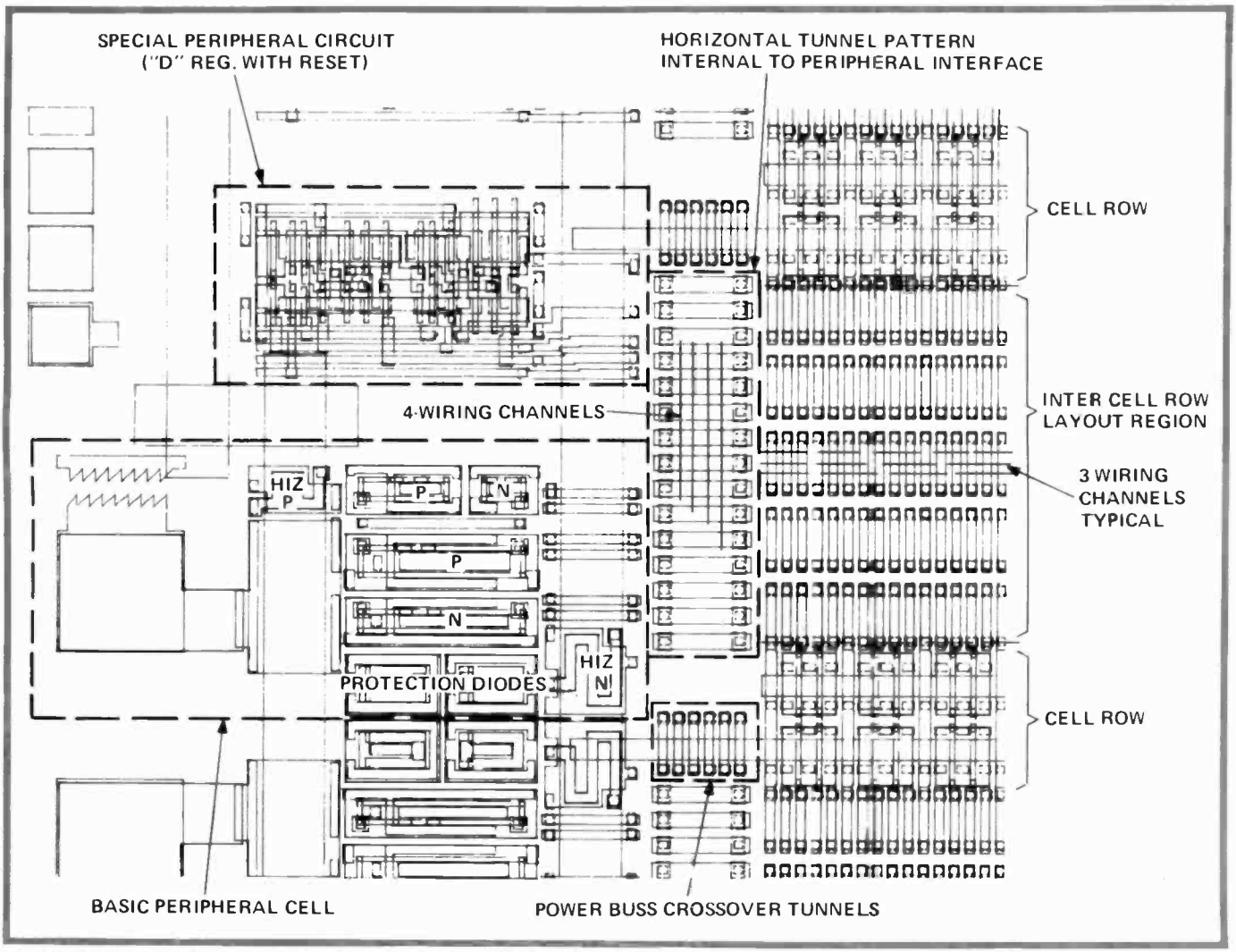

Fig. 2. Layout of the basic peripheral cell, special circuits, and the interconnect tunnel pattern.

Input protection circuit

The input protection circuitry consists of spark gap, five squares of $p+$ epitaxy, and two gated diodes. The five squares of $p+$ epitaxy are typically 300 ohms and are used as a series resistor as part of the input protection network. If the cell is used as an output circuit, the 300-ohm series resistor will be short-circuited by the metallization pattern. The gated diodes have a junction periphery of approximately 8 mils (200 μm).

Available transistors

There are six devices available that can be metallized to provide the desired interface function. The two high-Z devices are used primarily as pull-up or pull-down resistors on gate inputs. The impedance of these devices is typically 300 kilohms at 5 V. It is possible to use the high-Z devices in an inverter configuration if the peripheral cell is not being used as an I/O cell.

The remaining four devices can be used to implement a variety of I/O functions. These devices have edgeless gates (polysilicon does not run off the epitaxy), which improve the input protection capability. The devices can be paired to provide a large and small inverter that can be used in any desired combination. Some useful I/O functions that can be designed are:

- Inverting input or output cell
- Noninverting input or output cell
- Tristate function
- Passive input or output function.

If necessary, the four devices can be used as a two-input gate for internal chip usage when not being used as an interface circuit. The peripheral devices can be used to provide a transistor-transistor-logic interface at 5 V (sink 1.6 mA at 0.4 V). Because of the power distribution through the peripheral cells, a small resistor consisting of approximately one-half square of polysilicon (approximately 10 ohms) will always be in series with the function implemented.

There are seven I/O pins spaced on 12-μm (or multiples of 12-μm) centers to access the cell. One of these pins is dedicated to the gate input of the high impedance p or n transistor. Although only a maximum of two or three pins may ever be used in a circuit function, the individual circuit layouts can be more easily and efficiently generated.

Internal interconnect region

The internal interconnect area is a very crucial design area because it presents a fixed routing surface and must be optimized to ensure 100-percent connectivity. The final design features are:

- Fifteen horizontal metal channels are between cell rows. These channels are incorporated into groups of three, with five tunnel patterns between cell rows.
- Vertical tunneling between cell rows encompasses all available vertical channels.
- Vertical spacing between the tunnels allows the diagonal interconnects between the adjacent tunnels to provide lateral signal movement.
- The side routing area to pads is part of the overall interconnect area.

Figure 2 shows the implementation of the interconnect tunnel pattern for a small portion of the chip between cell rows. Included in the figure are the vertical tunnel pattern between cell rows with three horizontal metal channels per tunnel, the horizontal tunnel pattern that interfaces the center cell area to the side row peripheral cells, and the power bus crossover tunnels.

The basic internal cell contributes one tunnel pattern each and a total of two tunnel patterns (six metal channels) between cell rows. The vertical dimension for the 15-channel tunnel pattern, with diagonal line connectability, is 280 μm (11.2 mils). The horizontal tunnel pattern is placed on 20-μm centers, which makes it compatible with the 10-μm spacing in the internal cell region. Therefore, a metal channel is available between the horizontal tunnels. The side routing roadbed will provide for four signal wires to be vertically routed. The series of six vertical tunnels in the side routing area is to provide a path for the cell row power bus to connect to the appropriate bus ring in the peripheral area.

The entire routing area is on a 10-μm horizontal by 12-μm vertical grid. The grid dimensions were a direct result of the process rules used in the design. The 0.0 reference point for routing coordinates is located at the origin of the lower left horizontal side routing tunnel pattern. The internal routing area extends from the reference point to the end of the right side horizontal tunnel pattern in the x-direction and vertically to the origin of the top-row peripheral circuits.

The reference point is also the origin of the bottom row bonding pads. Between the bottom row of peripheral circuits and the first cell row, only nine wiring channels are available. This is also true for the top cell row and the top row of peripheral circuits. Because the wiring is lighter in this region, it was not necessary to include 15 horizontal wiring channels. The routing to the right and left side peripheral terminates at a predetermined horizontal side routing tunnel pattern. Each of the pins on the side peripherals is assigned to its own specific horizontal tunnel connection and, depending on the circuit function specified for each location, the information located in the pin data file (PDF) will determine the connectivity the program will make. Because the peripheral circuit pins are on a 12-μm grid, no special connection needs to be made to the top and bottom rows of circuits. The internal tunnel pattern was included at every possible location because of the fixed routing area, the practical limitation on the number of horizontal wiring channels, and the provision for future growth (that is, expand the number of internal cells).

Special peripheral circuits

A variety of special circuits have been designed and located in the periphery of the AUA chip. The special circuits designed into the AUA are functions that are frequently required in applications. The active circuits in the AUA designs are:

- Voltage reference circuit
- Zener diode stack
- D-type M/S registers with reset — eight independent stages (four on each side of the chip)
- Prescaler — two independent stages
- Large inverters — two independent stages.

The use of these functions is automatically incorporated by the placement and layout programs. The linear amplifier and Zener diode functions have a single unique layout pattern, while the others could have several layout patterns associated with them. All the special circuit functions are customized layouts to provide optimum performance. Figure 2 presents the layout of the "D" M/S register with reset.

These special circuits can be used for level translations (voltage reference), on-chip oscillator designs (Zener diode), countdown of high input frequency signals (prescaler), high-speed shifting operations (M/S registers), and for driving heavy loads on-chip such as a clock line (large inverter). In addition, the registers and prescalers can be used to alleviate high gate utilization of the internal cells if necessary.

AUA software development

Automatic layout capability

The AUA program provides fully automatic layouts — specifically, automatic cell placement followed by cell interconnection. The placement function uses a pair interchange technique in the placement algorithms. These algorithms have several objectives to accomplish. They are to develop a placement of AUA cells on the chip such that: the total length of all nodes is near minimum; the length of all cells on each cell row is within the maximum allowed and all cell rows are nearly equal length; and, in conjunction with the first two objectives as well as gate-pin reassignment and cell reorientation, the minimum crossover in the routing is provided. There are two basic routing techniques used in the program — a direct-routing algorithm and a general-purpose pathfinder (or maze-runner) routing algorithm.

The direct algorithm is a very fast operation and nominally completes 80 to 85 percent of the required routing. For relatively simple logic, over 90 percent is completed by the direct technique. This procedure uses the fact that for simple connectivity requirements, known minimum routing channels are often available and are, therefore, used.

The remaining 15 to 20 percent of the connectivity is completed by the general-purpose pathfinder routing algorithm. This routing technique will find all possible remaining paths and, then, will find the minimum path.

Among the automatic options of the program is the very important critical path (or minimum delay) feature for a specified subset of the logic. As part of the input data, a reasonable number of logic paths may be identified as critical. The standard cells associated with all branches of all critical paths will receive special consideration during the placement phase. This special consideration will yield minimal routing in low utilization areas of the array such that minimum time delay will be achieved for members of all critical paths.

Roadbed geometry

A key factor in the solution of single-level, fixed-geometry automated routing is gate-pin accessibility. That is, for very high routing completion probability with one level, it is critical that access to any unrouted gate pin not be blocked by previous routing. The greater the gate-pin accessibility potential, the greater the probability of accomplishing 100-percent routing automatically by the program. The roadbed geometry has been designed such that each gate pin has a large number of potential access points. Figure 3 illustrates a few of these (identified by Xs) for the gate pin identified as "A."

A second key factor is the signal crossover potential. It is critical that a large number of signal crossovers be provided for high routing completion probability. The greater the signal crossover potential, the greater the probability of automatically accomplishing 100-percent routing. The roadbed geometry has been designed such that there is a large number of potential crossover points for each gate pin. Figure 3 illustrates a few of the potential crossover points (identified by bars) for the gate-pin identified as "B."

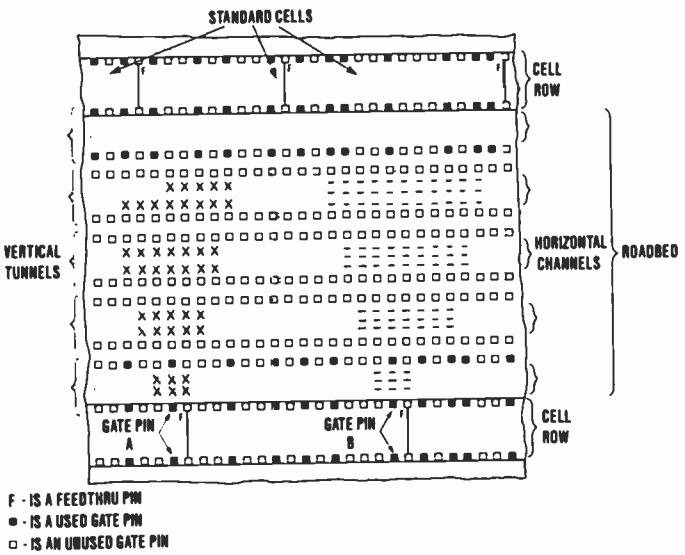

Fig. 3. AUA gate-pin accessibility and crossover potential.

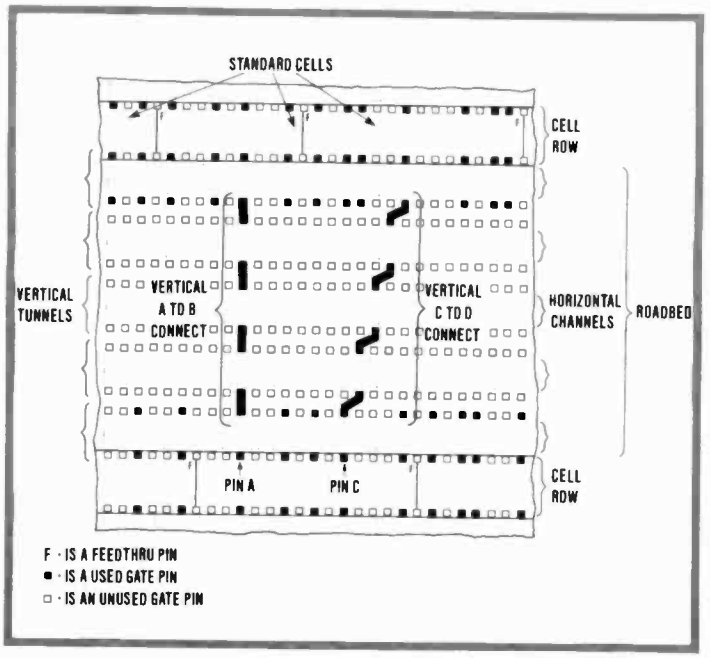

Fig. 4. Examples of vertical and diagonal tunnel-end connectivity.

The tunnel pattern in the AUA layout consists of four channels between vertically adjacent tunnel ends. The channel between the vertically adjacent tunnel ends is used to provide vertical or diagonal connectivity, both of which are illustrated in Fig. 4. The reason for this specific layout is to provide high probability of achieving 100-percent automatic connectivity with very high interior gate utilization (over 95 percent) for ultracomplex random logic. For relatively simple logic (such as shift registers) this AUA design would be underused.

Test results

The automatic layout program was evaluated with several demonstration vehicles. Two of these evaluation test problems are described here. In both cases, the arrays were 100-percent automatically placed and routed by the program. Test Problem 1 is a universal adder in which 81.6 percent of the 640 interior gates are used. Test Problem 2 is a 32 x 8 MUX (formatter) using 98.8 percent of the interior gates.

Test Problem 1 results are shown in Figs. 5 and 6. These figures not only illustrate the checkplot layout of the array, but simultaneously show the application of the critical path option of the program. Six critical paths were selected to test this feature. They are indicated by the heavy lines in Fig. 5 to represent the "before" state of the routing. These paths were purposely chosen from among the longest routed paths of the logic. After specification to the critical path option, the program was re-executed. The results (or "after" state) are shown in Fig. 6, where the connectivity of the paths is again indicated by the heavy lines. Note that all of the standard cells connected by these paths are now closely clustered, and located at the end of the rows, which are, typically, sparsely routed areas. The resultant routing is significantly reduced compared to that shown in Fig. 5.

In addition to nominal logic requirements, Test Problem 1 also included extra logic to test the use of the special peripheral circuits (the voltage reference circuit, a low-impedance inverter, the eight M/S flip-flops, and the two-stage prescaler). Once again, full and optimum routing was achieved. The entire problem contained 791 pin-pair connections.

Test Problem 2 was particularly chosen to test the upper limit of the program. The routing requirements were

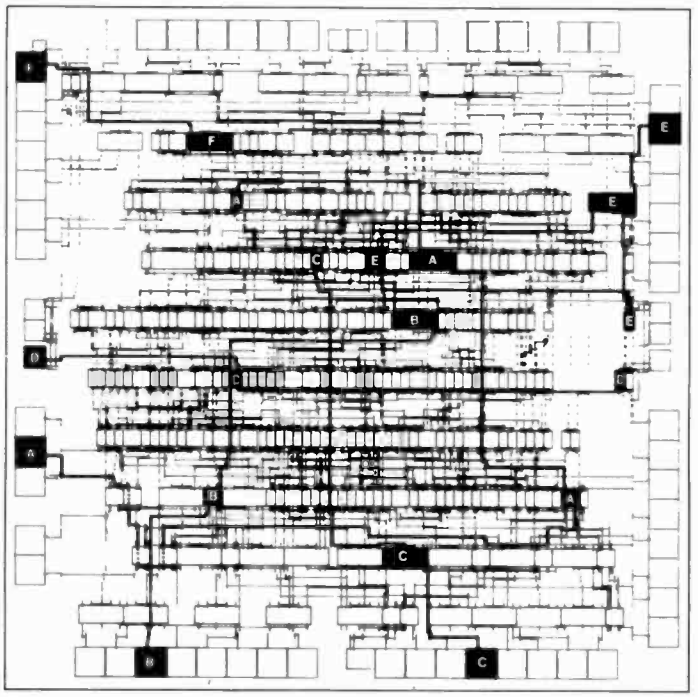

Fig. 5. Critical path routing before optimization.

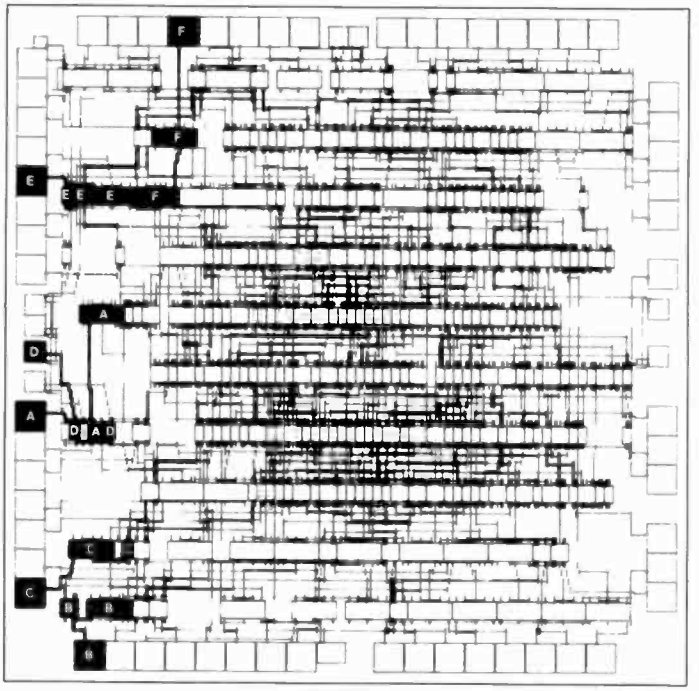

Fig. 6. Optimized critical path routing.

extremely complex, as indicated by the heavy use of the roadbed shown in Fig. 7. In spite of this complexity, 100-percent connectivity was achieved with 98.8-percent gate utilization. It is expected, therefore, that 100-percent routing will be achieved automatically for virtually every chip design, even for random logic functions with their more complex and dense interconnection matrix.

Figure 7 highlights routing chosen at random for several two-pin nodes and several five-pin nodes. The problem contained 1176 pin-pair connections.

AUA test chip

To validate the basic AUA design and also characterize its performance, a customized metal pattern was generated that provides this capability. Figure 8 is a photomicrograph of the finished AUA test chip. This test chip uses almost every available active device and a large portion of the many interconnect tunnel patterns. The test chip has verified that all of the various basic cells and special circuits that comprise the total AUA design are correct. The basic internal cells were configured into ring counters, NAND and NOR delay chains, and various shift register and counter circuits, mainly for characterization purposes. The basic internal cells were also used to develop a logic network that was intended to validate the basic design.

The basic peripheral circuits were also used in a variety of ways to ensure all devices were independently tested and, therefore, verified for all 62 peripheral circuits.

AUA characterization data

The data being presented are results obtained at 5 V, but the test circuits were observed to operate at 3 to 10 V. The test results represent typical data taken on approximately 20 parts from one wafer process run and are summarized in Table II.

Table II. Summary of AUA performance characteristics.

AUA test circuit	*Test circuit performance at 5 V*
Ring oscillator	700-ps stage delay
NAND, NOR delay chain	1.2-ns stage delay
Output drive capability	30-pF load: t_r = 21 ns, t_f = 17 ns
	I_{SINK} = 3.0 mA (V_{OUT} = 0.4 V)
Toggle rate of internal cell counter logic	~100 MHz

Ring oscillators

There were two ring oscillators on the AUA test chip with both consisting of inverters. Each inverter stage had the input to the next inverter as its load, with no additional parasitic RC networks, and, thus, provided the optimum condition for internal cell performance. The typical stage delay measured on the ring oscillator at 5V is 700 ps per stage.

NAND and NOR delay chains

NAND and NOR delay chains were included on the test chip, with each stage loaded only with the input of the next stage, and, thus, provided optimum performance for these circuits. The typical stage delay at 5 V was approximately 1.2 ns per stage. In applications the chip environment will degrade this performance, the amount dependent on the fanout and the AUA layout.

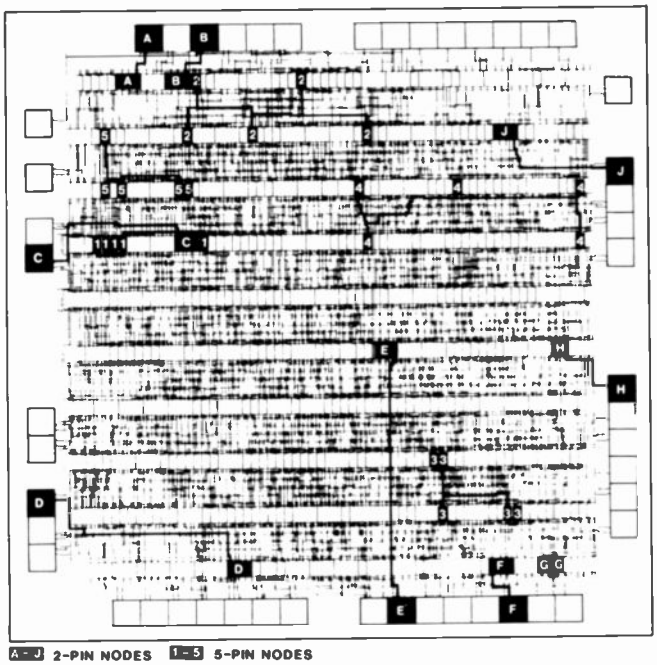

Fig. 7. Routing in a highly complex layout.

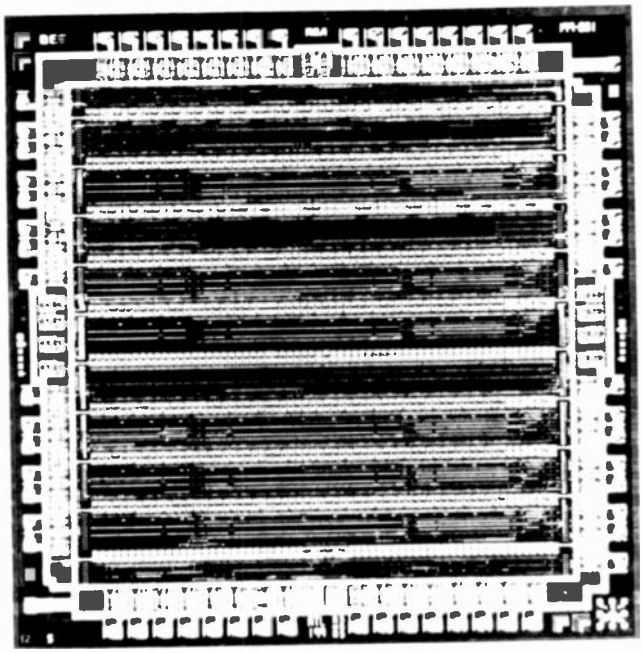

Fig. 8. Photomicrograph of the finished AUA test chip.

Peripheral circuit drive

The basic peripheral circuit was configured into a tristate driver and its output loaded with 30 pF. The rise-times under these load conditions were typically 21 ns and the fall times were 17 ns. The maximum current sinking capability is typically 3.0 mA or approximately 2 T^2L loads (V_{OUT} = 0.4 V at 1.6 mA).

Internal counter operating rate

Several versions of a counter circuit were implemented with the internal cells. Toggle rates approaching 100 MHz at 5 V were observed. Maximum toggle capability determination had not been made, but is expected to exceed 100 MHz at 5 V.

AUA demonstration vehicle

A logic diagram of an Army application has been successfully run using the AUA system. A checkplot of the layout for this application is shown in Fig. 9. For this particular application, the layout was generated in approximately four to six hours.

Conclusions

The AUA system automatic layout capability has been successfully demonstrated by results from test cases and a demonstration chip from an Army application. At the same time, the AUA topological design has been verified and characterized by the generation of a customized test metal pattern.

The present AUA design approach can possibly be extended from 800 gates to approximately 2000 gates without sacrificing 100-percent connectivity for 90-percent gate utilization rates and without increasing chip size to an unacceptable level. For chip sizes beyond this range, new concepts will be required in both the layout program and topological design.

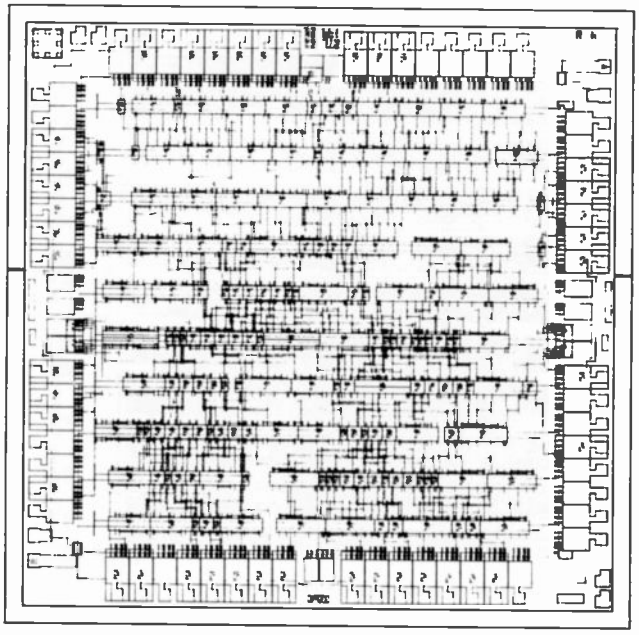

Fig. 9. Checkplot of a demonstration chip.

Acknowledgment

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B.A. Wiegand

Three-dimensional interactive computer-aided design and manufacture of mechanical structures

CAD/CAM systems promise to revolutionize high technology industries. At RCA Missile and Surface Radar, a CAD/CAM system is now being developed to handle the entire design-development-production process of microwave and mechanical structures.

Abstract: *The complexity and accuracy requirements of microwave structures for low-sidelobe antenna systems exceed current capabilities to design, document, build and test them within reasonable time and cost goals. A three-dimensional (3 D) computer-aided design/computer-aided manufacturing (CAD/CAM) system is being developed that will improve turnaround time, increase accuracy, and reduce the number of steps from design to finished part. It will provide common data bases to solve engineering problems in static and dynamic modeling, spatial interference control, part and assembly documentation, and generation of numerical control machine instructions.*

The ability to create a data base early in the design process minimizes the amount of effort required to bring a project from conception to completion. Unlike traditional design methods which require drawings to be manually produced, filed, retrieved, and logged for each step in the product cycle, a design need only be entered once into a three-dimensional interactive computer graphics system. The need to recreate drawings and regenerate information is eliminated because the data base created in the design stage is immediately accessible for successive steps in product development.

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A 3D CAD/CAM system can be used to great advantage in the development process. The product cycle typically consists of the following stages: design, prototype analysis, documentation, fabrication, and test. Beginning with the design stage, the system is used to model parts and assemblies for initial sketches or layout drawings. Pictorial representations of rotated parts may also be generated in correct proportion to one another for technical illustration. The data base is then used to perform interference checks, and during the analysis stage, to determine determine mass properties and analyze the effects of stress. Using the same data base, documentation such as detail and assembly drawings can be generated. Because the design is developed on and stored in the system, manufacturing applications, such as numerical control, are enhanced. Finally, the single graphics data base facilitates engineering changes throughout the entire product cycle.

Hardware description

The three-dimensional CAD/CAM system being developed is centered around an Applicon Graphics System (AGS). The AGS/885 Central Processing Facility (CPF) is the nucleus of the Applicon Graphics System. While primarily dedicated to computational tasks, the CPF is also the control point to which all interactive and input/output devices are attached.

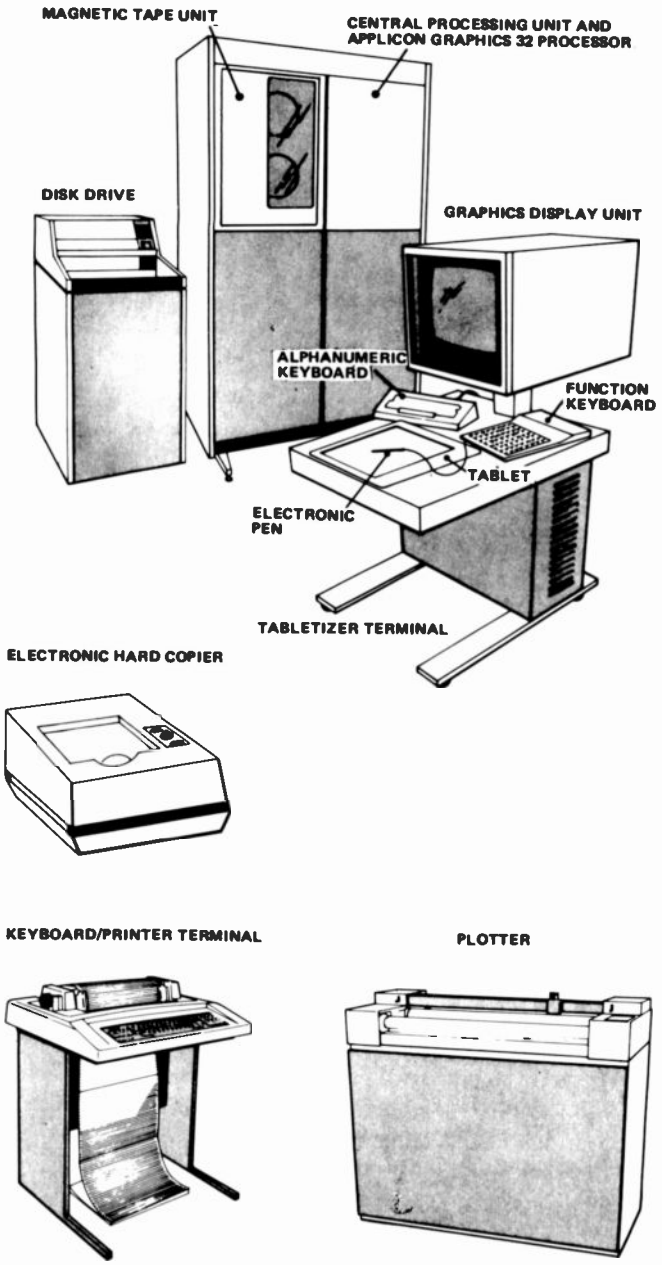


Fig. 1. Applicon Graphics System. This is an advanced system for high-precision engineering design, drafting and manufacturing applications. It offers the designer a solution to the problem of true three-dimensional representation, while providing the draftsperson with a significant advance in computer-aided drafting and the manufacturer with the capability of producing parts programs directly from part geometries.

The entire AGS is shown diagramatically in Fig. 1, and its components are described as follows:

1. *Central processing unit (CPU)* — performs as the system computer and is composed of a DEC PDP-11/34 with 208 kb of semiconductor memory. Its primary functions are to execute user commands and control the flow of data between user work stations and the CPF.
2. *Applicon Graphics-32 Proceessor* — used to provide an interface between the AGS/885 and tabletizer terminals. The processor also responds to numerous complex computational functions enabling the PDP-11/34 to attend to other system operations.
3. *Disk unit with removable 200-mb pack* — provides immediate on-line access to files.
4. *Magnetic tape unit* — used to load applicon software, interface with other systems, and provide low-cost archival storage of software, drawings, and other data.
5. *Tabletizer terminal* — a work station where users can perform drawing activities and control system functions. Work station components include:
   - A graphics display unit used to view drawing or system operations. Each terminal features a selective erase capability that allows selected components to be edited without having to redisplay the entire image on the CRT. This feature considerably reduces the number of time-consuming redisplays needed while editing.
   - An electronic tablet and pen used to enter hand drawn symbols or to utilize menus located on the tablet. A unique feature is the ability of the system to recognize predefined hand drawn symbols as commands. This feature allows the invocation of complex command structures with a pen stroke rather than by time-consuming manual entry.
   - An alphanumeric keyboard used to manually enter text, special characters and commands not previously defined as menu functions or tablet strokes.
   - A function keyboard, which accepts predefined menus as overlays and complements the electronic tablet menus and symbol library, thus extending the capacity for rapid data entry.
6. *Electronic Hard Copier* — an electrostatic type copier which copies everything on the display within 20 seconds.
7. *Plotter* — plots drawings at various scales, on vellum or mylar, with or without preprinted drawing formats, of consistent high quality that meets all government requirements.
8. *Keyboard/printer terminal* — provides an alternative to using the graphic display for tasks unrelated to drawing activity.

Software description

The Applicon Operating System is controlled by the following four cooperatively functioning software systems:

- Digital Equipment Corporation RSX-11M which is a compact real-time operating system designed for a wide variety of applications where many processes must be concurrently monitored and controlled.
- Applicon Graphics System 900 IMAGE multiprocessing system which utilizes a dual-processor architecture to maximize throughput.
- Applicon Graphics-32 microprocessor which provides a

software interface between the terminals and the PDP-11/34. This arrangement frees the host PDP-11/34 from handling the frequent interruptions required for an effective man-machine interface and enables the host processor to accommodate system related tasks more efficiently.

- Applicon Graphic System 880 IMAGE which is an advanced 3D Graphics application system for high-precision engineering design and drafting. It speeds and simplifies preparation of 3D graphic data into models and drawings.

In addition to these major software systems, options commonly used by the CAD/CAM system include a Fortran interface which permits Fortran access and modification of the AGS data base, a macro interface which allows manipulation of drawing files and modification of the 880 command set, and a numerical control programming package which interactively generates automatically programmed tool (APT) part programs utilizing tool descriptions, bounded geometries and tool path controls.

System files

In addition to handling conventional source and object files, the system provides a graphically oriented file type known as a drawing file. Drawing files differ from source and object files in that they are Applicon-specific in form and contain user-generated graphic and alphanumeric data used to create and maintain models, part and assembly drawings.

Drawing files consist of three user-created parts — a dictionary, a library, and drawing. The dictionary contains alphanumeric names, hand-drawn symbols, and menus that define specific commands (or strings of commands called macros). Many of these commands relate to the development and movement of drawing components. The library contains graphics components that the user assembles into entire drawings using commands previously defined in the dictionary. Library descriptions of components may be changed or renamed at anytime, resulting in the changes being made automatically throughout the drawing, wherever those components appear. This feature is invaluable when it comes to rework, engineering change, and customizing. Drawings are created by the use of commands from the dictionary and components from the library. The drawing is actually a record of component instances and placement within bounded three-dimensional space. Dictionaries and libraries are usually combined to form start files from which new drawing files are developed, saving the expense of regenerating definitions. For example, a start file could be copied and custom-tailored to meet the needs of a specific project.

System operating modes

The four major AGS operating modes are control (CTRL), edit (EDIT), edit component (ECMP), and teach (TEAC) (Fig. 2). While working at a terminal, a user may easily switch from one operating mode to another by giving the appropriate command via the keyboard, function keyboard, menu, or tablet stroke.

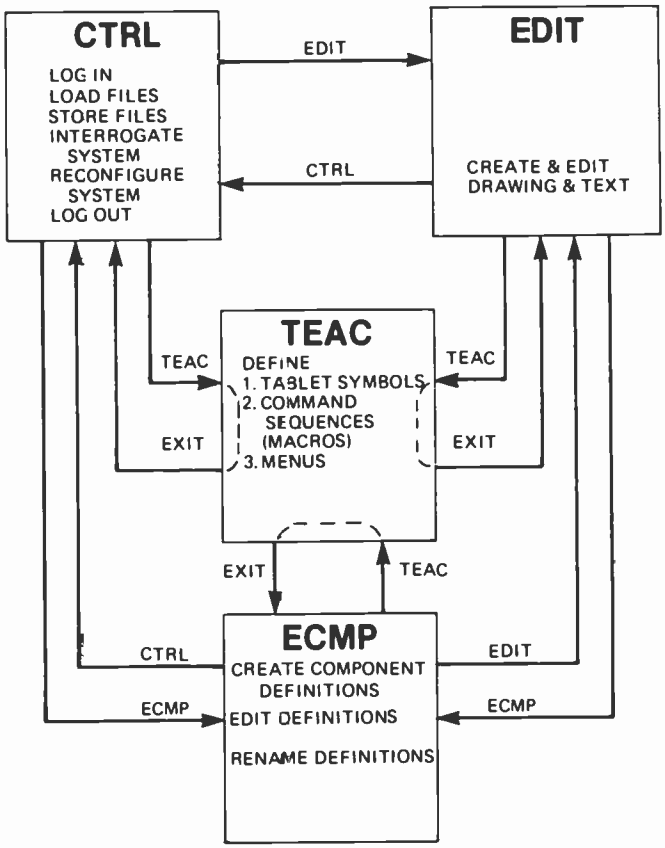


Fig. 2. AGS operating modes. All sessions at the graphics station start and end in the CTRL mode. Most of the time, however, is spent in the EDIT mode where actual construction and modification of the graphics data take place. The remaining modes, TEAC and ECMP, are used as needed to define commands and construct library components.

In the control mode, users log on and off the system, load, store and copy files, manipulate devices and activities to optimize production, and obtain information on system devices, activities, and files.

In teach mode, the user develops the dictionary of command definitions consisting of tablet symbols and names that represent commands, or command sequences. Names, commands, and macros are also assigned to menu elements for use by the tablet menu, or the function keyboard menu, or both.

In edit mode, the operator uses commands to arrange components into drawings. Typical edit functions performed on drawings include adding, deleting, copying, rotating, moving, and scaling components, manipulating views, changing text and dimensions, and sending drawings to plotters.

In edit component mode, users can create and modify library components. This mode has all the editing and viewing features of edit mode.

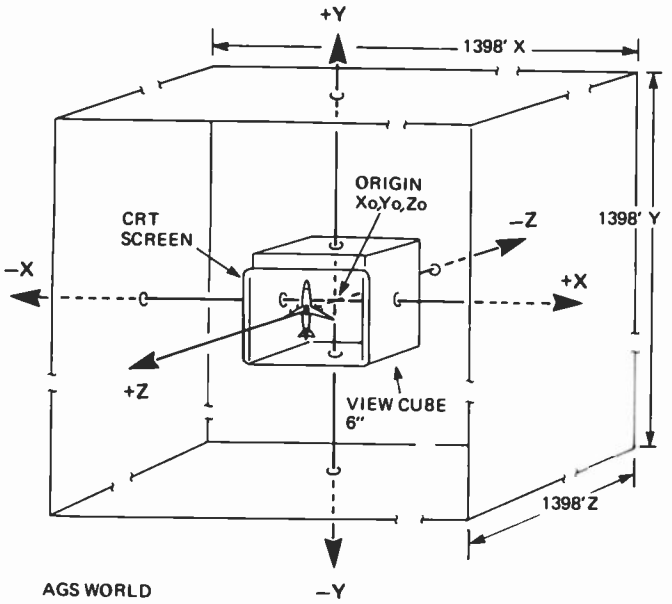


Fig. 3. The AGS world is a cube containing a centrally located three-dimensional coordinate system within which graphic construction takes place. Viewing of the space within the AGS world is accomplished by varying the size and location of the view cube.

Graphic construction and viewing concepts

The AGS drawing world (Fig. 3) contains a three-dimensional coordinate system with central origin. There are almost 17 million units that are addressable along each axis in a 3D coordinate system. Natural (real-world) units can be assigned an appropriate number of AGS units to obtain the accuracy that the application requires. There are two common measurements used within the system:

10,000 units = 1 inch (natural) for English System definition, and

1,000 units = 1 millimeter (natural) for metric system definition

The 10,000 units/inch provides a definition cube of approximately 140 feet on a side to an accuracy of the closest one ten-thousandth of an inch. Figure 3 illustrates the AGS drawing world with an assignment of 1,000 units to an inch.

The graphic display terminals for AGS systems have 19-inch diagonal measurements. For a user to display the entire AGS drawing world at all times would be unrealistic as well as unworkable. The view cube (Fig. 3) is a means for looking at smaller portions of the drawing world. The view cube size and location can be quickly changed, within drawing-world limits, at any time by using a simple tablet stroke. The view cube contains six faces or surfaces that have a direct correspondence to views prepared on orthogonal drawings — front, right, top, left, bottom, and aft. In addition, there is the capability for displaying rotated views which are categorized as flying-eye views. Included are isometric, dimetric, arbitrary trimetric, stereo, and perspective views. The system permits the display of up to four views simultaneously by dividing the graphic display into four equal parts to display the views requested.

The drawing world has built-in displayable grid features that enable the rapid manual placement and development of components. Grid positions are indicated by small dots on the screen and may have the same or different dimensions along each of the *x*, *y*, or *z* axes. Grids are defined and varied by the user and provide the capability of positioning components to the nearest grid intersection when they are added to the drawing. For extremely fine off-grid placements, absolute coordinate data may be entered from the keyboard.

System applications

In order to design, document, test and fabricate a part utilizing an AGS 3D system, a series of events will occur that require the cooperative effort and skills of a number of disciplines. Figure 4 shows the essential elements of this system. The part must first be conceptualized by engineering and then reviewed by the drafting department and an AGS software specialist to determine how the AGS should be configured in terms of start-files, menus, macros, and other supporting software.

If the part is to be fabricated utilizing the AGS numerical control capability, machining information will be required from factory personnel. When the engineering, drafting, and factory requirements are complete, the AGS specialist will assemble the software required to support the task.

The engineer may conceptualize the part directly on the AGS, using some of the standard engineering aids included in the system such as mass property calculations. These aids enable the engineer to compute areas and perimeters, centroids and principal axes, moments of area and inertia, radius of gyration, and weight and volume of solids with constant thickness. He may also request that the AGS specialist implement some data base interface software to further assist in the concept construction and analysis.

The part is then modeled, viewed and checked for design conformance. If approved, it is combined with other parts comprising an assembly. At this point it is analyzed for spatial interference with other parts in the assembly. When a part is judged to be correct, it is scheduled for documentation utilizing applicable drafting standards.

If the part is to be produced by numerical control (NC) equipment, a copy of the production drawing is sent to the

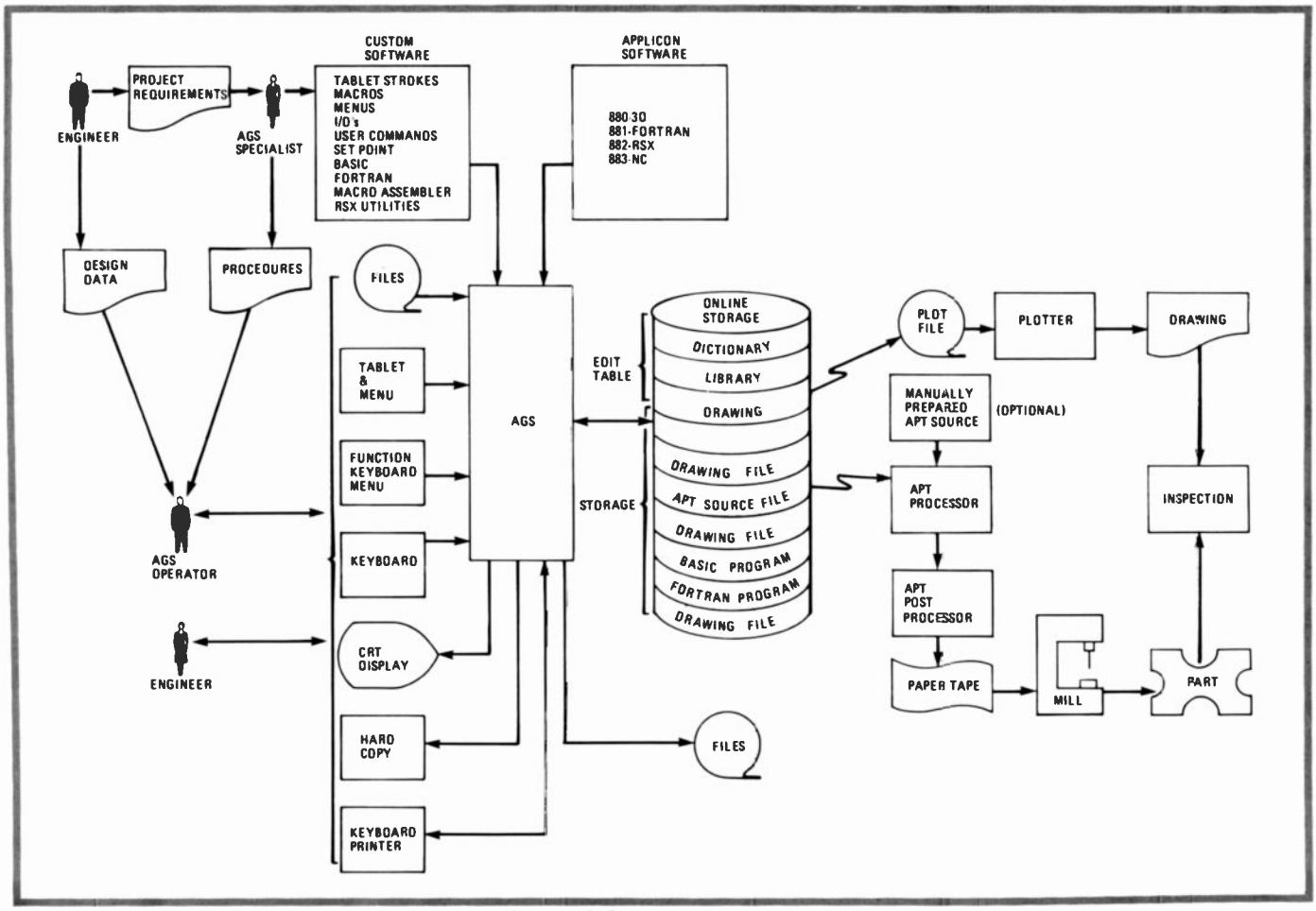


Fig. 4. The mechanical CAD/CAM system is used for design, documentation analysis, and production of parts and assemblies.

factory where it is studied for machining operations. When a machining plan has been developed, it is documented and sent back to the AGS. The machining document contains specifications for the number and type of tools to be used and other applicable information such as tool direction, feed rates, spindle speeds, coolant options, and clearance planes. This information will be used to compose and label tool driving geometry, generate tool parameters and paths, and produce an APT (automatically programmed tool) source file. The APT source file, plus drawings and listings of the labeled geometry and toolpaths, are returned to the factory for final approval. If satisfactory, the APT source file is then processed into an NC tape to drive the automated tool, otherwise it is modified or reworked. Changes can be made automatically on the AGS or by off-line terminal editing of the source file.

APT processing is currently done in a timesharing mode and consists of two operations. First, the APT source file is converted into a tool center line or cutter-location (CL) file. The APT processor produces diagnostic messages in the form of warnings or errors, when warranted. It also produces a listing of all geometry normally used for toolpath validation. In the second operation, the CL file is converted by a machine-specific software post processor designed to output NC commands for the user's automated machinery.

The NC tape thus generated is placed on the NC machine. Following the procedures set forth in the machining document, the operator produces the part. The part is then inspected for dimensional accuracy using the production drawing as a reference.

Conclusions

While the mechanical CAD/CAM system described here has not yet realized its full capability, it has already proved its usefulness in initial applications and holds great promise for future productivity gains. As with any new system, training is required. Time spent initializing a system by creating macros, menus, and component definitions also is not immediately rewarded. The real productivity results from using this stored data on subsequent applications. Also, once a data base of parts and assemblies is created, it has many other uses. It can quickly provide views of objects from any angle for technical illustrating; serve as a common reference for project members, resulting in greater project control; be used to avoid spatial interference problems caused by independent or decen-

Development of a microwave subassembly

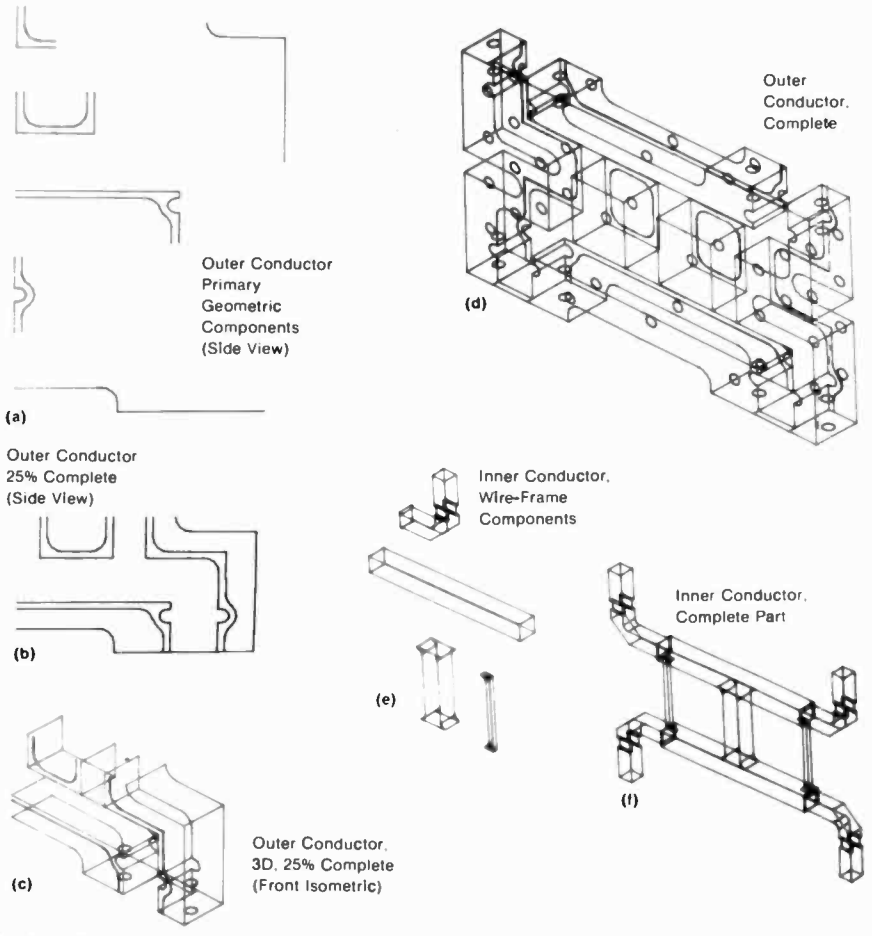


Fig. 5. Three parts form the subassembly: an outer conductor, inner conductor, and cover. The outer conductor is symmetrical so only a portion of its elements need to be generated, reducing development time and improving accuracy. **(a)** Primal geometric components are used to form **(b)** one-quarter of the outer conductor. **(c)** A wire-frame model is created by projecting geometric elements along the third axis (Z in this case). The resulting quadrant is copied and mirrored about the X and Y axes, and holes are added to form **(d)** the complete outer conductor model. The inner conductor was modeled differently. Although symmetrical, the design required that the conductor ends have the ability to be easily modified. To accomplish this, wire-frame components were generated and combined to form **(e)** four basic components that were positioned to form **(f)** the complete inner conductor. End configurations are changed simply by replacing the basic end component. **(g)** The cover was generated the same way as the outer conductor using two of the primal geometric elements from **(a)**.

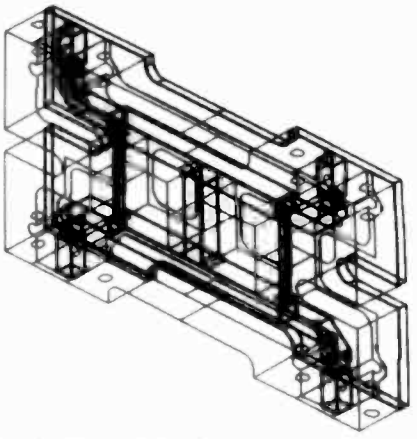
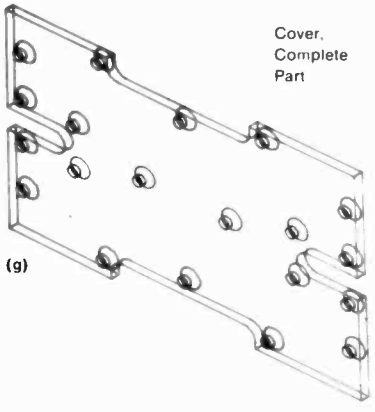


Fig. 6. Complete microwave subassembly. All three parts are combined and appear as they will when fabricated and assembled. The system allowed us to rotate and view the assembly, and check it for form and fit prior to production.



tralized development; permit the computation of static and dynamic properties of parts; produce tool paths and APT parts programs for numerical control application; serve as the basis for a family of parts network; and provide a means to quickly modify and re-document a design.

Interactive graphic technology is advancing rapidly, resulting in faster response times, more automated design techniques, and broader applications resulting in greater speed, accuracy and cost-effectiveness. As qualified personnel become more scarce, labor rates and material costs continue to increase, and manufacturing processes become more sophisticated, powerful computer-based systems that address these problem areas may become a requirement rather than an option.

Acknowledgment

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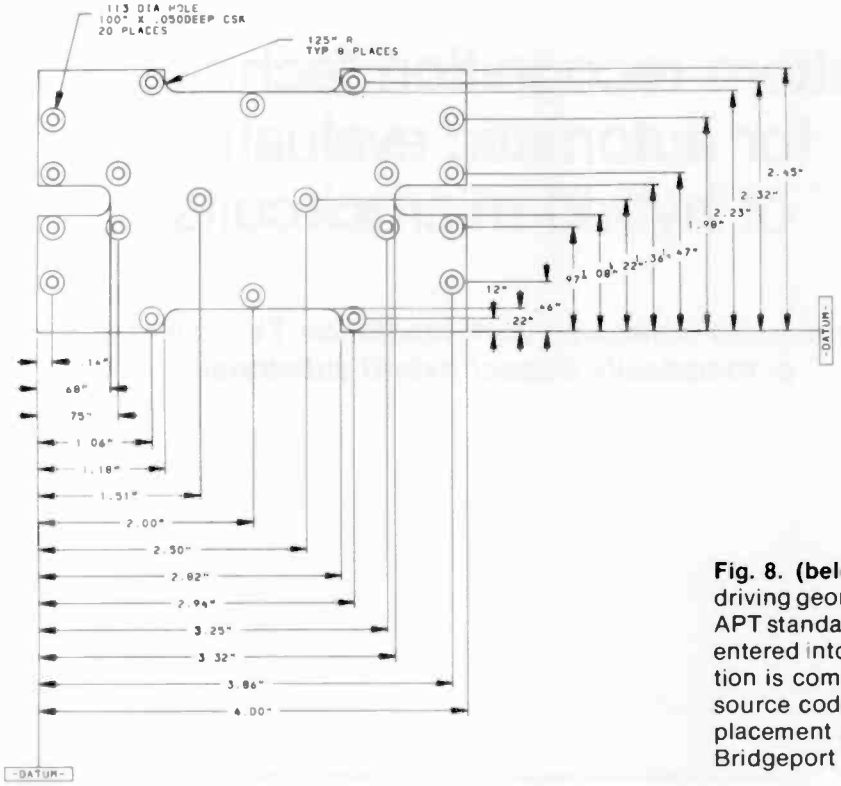
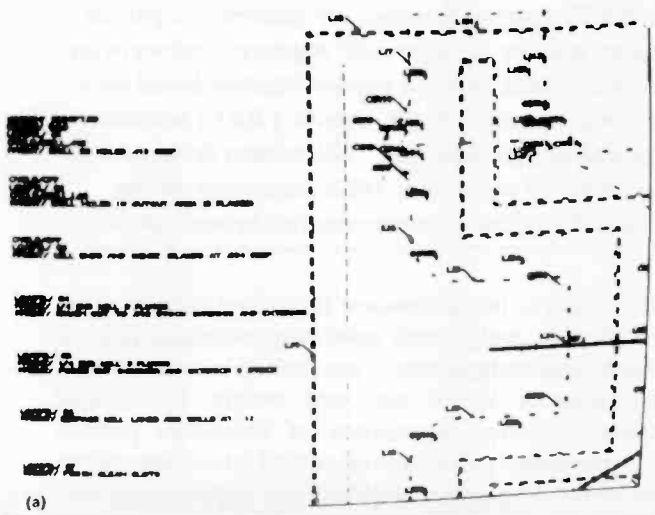


Fig. 7. Dimensioned cover. The cover is fully dimensioned by the AGS baseline dimensioning feature. Up to 28 dimension and extension lines can be added to the part, in one operation, using this option. The standard dimensioning feature allows single dimensions to be inserted. Dimensioning features are selected simply by using a menu.

Fig. 8. (below) Tool Paths and APT source code. Tool driving geometry is extracted from the model and labeled to APT standards. Tooling information from the factory is then entered into the AGS to form tool definitions. This information is combined to produce **(a)** tool paths and **(b)** APT source code. Tool path drawings are used to verify tool placement and motion. APT source file is processed into Bridgeport Numerical Control Tape for part fabrication.



(a)

```
      =LINE 1 294.-0 829.-0 1.1 2615.-0 829.-0 1
      =CIRCLE 1 2615.-0 8915.-0 1.0 0625
      =CIRCLE 1 2615.-0 8915.-0 1.0 0625
      =LINE 1 2615.-0 954.-0 1.1 294.-0 954.-0 1
      =LINE 1 294.-0 954.-0 1.1 294.-1 375.-0 1
      =LINE/-0 19.0 3665.-0 1.-0 19.-0 3665.-0 1
      =LINE/-0 19.-0 3665.-0 1.-0 8.-0 3665.-0 1
      =LINE/-0 8.-0 3665.-0 1.-0 8.0 3665.-0 1
      =LINE/-0 8.0 3665.-0 1.-0 19.0 3665.-0 1
MACHIN  BRDGPT 20
ORIGIN  0.0 5
LOADTL  01
CYCLE DRILL  412
PPRINT  DRILL 20 HOLES  412 DEEP
RETRACT START OF CUT SEQUENCE 0
        CUTTER/0 089 0 0.0 0025
        COOLNT/MIST
        SPINDL/3200
        FEDRAT/4 0
        TLAXIS/0 0.0 0.1 0
          FROM/0 0.0 0.5 0
          ZSURF/(PLANE/0 0.0 0.1 0.1 5)
          GOTO/0 94.-1 1.1 5
          ZSURF/(PLANE/0 0.0 0.1 0.0 0)
          GOTO/0 94.-1 1.0 0
          GOTO/1 25.-0 25.0 0
          GOTO/1 86.-0 25.0 0
          GOTO/1 86.-0 76.0 0
          GOTO/0 0.-0 803.0 0
          GOTO/0 495.0 0.0 0
          GOTO/0 0.0 803.0 0
          GOTO/-0 495.0 0.0 0
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          GOTO/-1 25.-0 25.0 0
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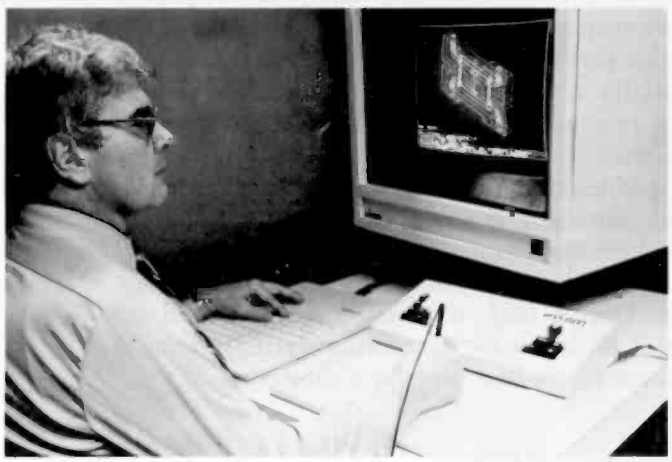
(b)



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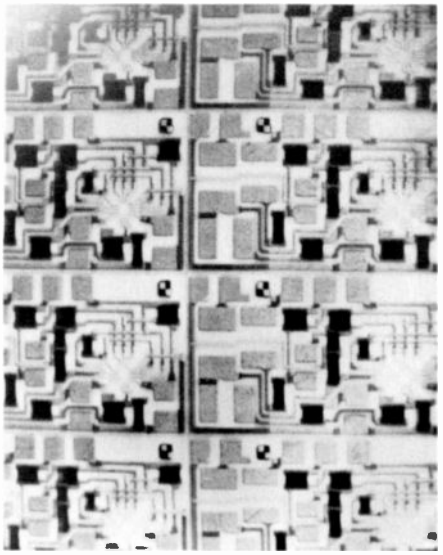

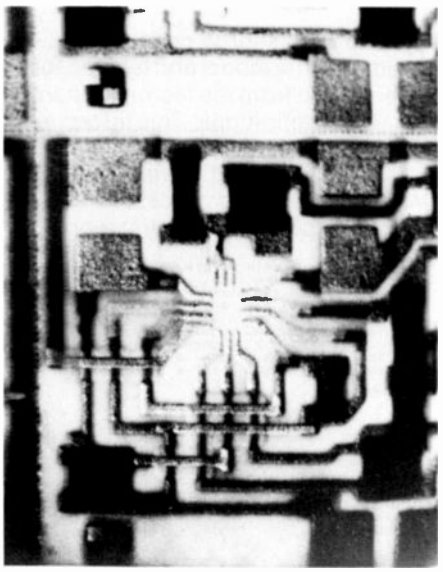

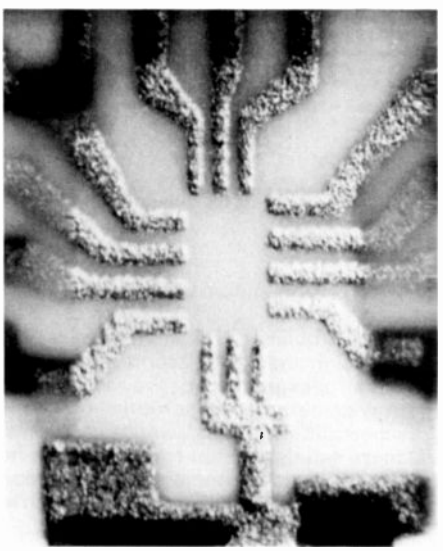

Complete print patterns can be ascertained with 1:1 zoom. A 3:1 zoom can be used to assess major faults. Detailed inspection requires 10:1 zoom.

J.M. Laskey|R.J. Wildenberger

Pattern recognition techniques for automatic evaluation of hybrid microcircuits

A computer-controlled high-resolution TV system can automatically inspect hybrid substrates.

Abstract: *This paper describes the pattern recognition techniques used in an automatic in-process microcircuit evaluation (AIME) system implementation based on a high-resolution return beam vidicon (RBV) television camera and storage technique. This system demonstrated the feasibility of automatic, 100% inspection during printing of thick-film conductor lines on hybrid substrates.*

Hybrid devices — using standard integrated chips, custom interconnection, and ceramic substrates containing printed conductors and components — are finding increased use in military systems where size and weight are critical parameters. Current geometries of thick-film printed circuit components (resistors and critical interconnections) require visual inspection of tolerances approaching one mil. Present manual inspection techniques require a microscope evaluation that economically limits the degree of inspection performed and results in operator fatigue. A need exists for a more automated method of in-process inspection, to improve yield and assure a higher degree of quality control.

This paper describes the pattern recognition techniques used in an automatic in-process microcircuit evaluation (AIME) system implementation based on a high-resolution return beam vidicon (RBV) television camera and storage technique. During tests, this system demonstrated the feasibility of automatic 100% inspection during printing of thick-film conductor lines on hybrid substrates.

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System approach

At the onset of this program, system-design concepts were characterized by several baseline program requirements, namely:

1. Apply thick-film hybrid visual inspection criteria (Method 2017.1, MIL-STD-883A).
2. Develop system techniques to support inspection rates approaching 750 substrates/hour.
3. Implement system on a minicomputer with reasonable memory storage (≤10 megabytes).
4. Use, if applicable, an available return beam vidicon (RBV) camera system in the demonstration model.

Several studies/analyses were conducted to convert the requirements into definitive system concepts and baseline designs for the demonstration model. They included:

1. Characterizing thick-film printing defects to establish system resolution.
2. Establishing illumination design (source, intensity, spectral properties, geometry).
3. Investigating possible techniques using other than a RBV scanning system.
4. Developing system operation timing requirements and a system error budget.

Design approaches involved tradeoffs between three interactive system parameters: resolution, speed, and dynamic range. Resolution, the fineness of detail the system can detect, was derived from the printing defect characterization. System speed, image scan and store time were derived from the overall goal of 750 substrates/hour. Dynamic range, the image-gray-scale range detectable by the system, was an area of design compromise that did not impact overall system requirements.

Alternative system approaches were considered — namely, techniques based on a laser differential line scanner, and a capacitive-coupled photo-diode (CCPD) array. The laser scanner was developed to inspect the repetitive matrix of patterns on IC masks (transparent objects). The incident laser beam was split and aligned to scan identical areas of adjacent patterns on the mask, detectors were placed on the opposite side of the mask, and the mask was translated in X and Y directions for scanning. The CCPD technique was based on scanning of a "master" and "test" substrate pattern simultaneously with separate, aligned CCPD arrays, and detecting difference video from each array cell-pair. In the final evaluation, neither alternative technique overcame the performance capabilities and inherent minimum-risk approach of using the available RBV camera.

Thick-film substrate characteristics

The substrate geometry and different kinds of thick-film processing flaws drive the requirements of the inspection system. Figure 1 shows the results of evaluation of typical defects such as: opens, shorts, whiskers between lines, line scratches and smears.

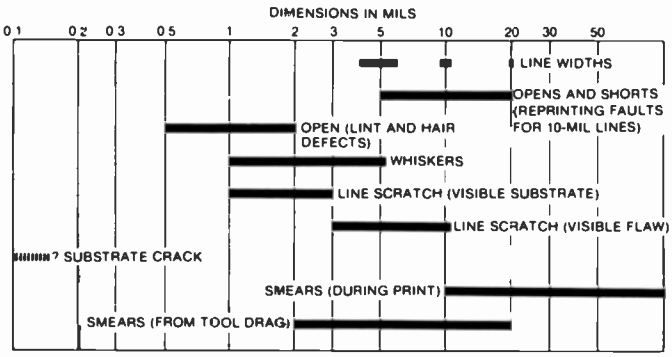

Fig. 1. Typical sizes of substrate features/faults (mils). The faults depicted are common to the printing of thick film hybrids.

Practical experience indicates that opens in 10-mil lines caused by defective printing will not generally be less than 5 mils. Similarly, short circuits between 10-mil lines separated by 10 mils will be such that the width of the shorting link will range between 5 and 20 mils. Opens due to trapped lint or hair that later vaporizes at high temperatures are in the range of 0.5 to 2 mils.

Television camera requirements

The heart of the AIME system is the return beam vidicon (RBV) camera. The RBV was chosen as the electro-optical sensor because of its very high resolution over the entire image area. The RBV can provide readout at a continuous rate with a steady-state optical exposure or in nearly-real time with a discrete input consisting of a shuttered exposure. With discrete input, the information can be read out in a variety of modes, including the slow, single-frame scan or the fast, multiframe scan. While the shuttered or discrete input mode of operation has not been used to demonstrate basic feasibility, it can be used as a method for achieving a production throughput of 750 substrates/hour. The prime features used in the current AIME system are:

- High enough resolution to permit viewing and storing the entire (2-inch x 2-inch) substrate image.
- Large storage capacity with low lateral leakage.
- Use of high-speed computer-controlled electron-beam scanning of selected portions of the stored image at zoom ratios suitable for adequate substrate evaluation.
- Operation at standard 525 TVL rates for compatibility with video recorders, displays, and so on.

The electron optics of the RBV tube and external magnetic assembly provide outstanding aperture response over the entire sensing layer. Figure 2 includes the sine wave response characteristic or Modulation Transfer Function (MTF) of the 4.5-inch RBV and also includes, for

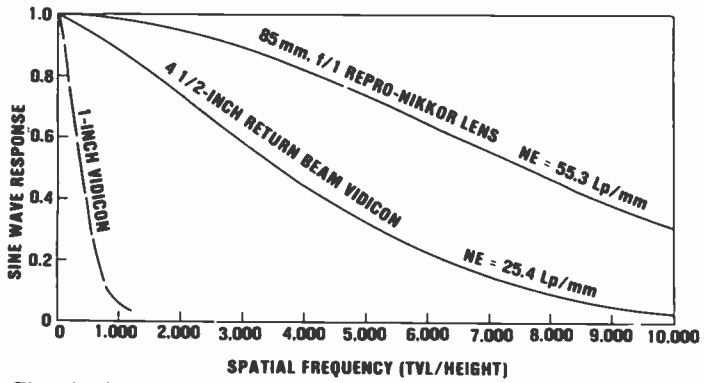

Fig. 2. Sine wave response. The lens/RBV combination permits resolution of fine detail.

comparative purposes, the MTF of a standard one-inch vidicon. The RBV provides approximately ten times the linear (equivalent to 100 times the area) resolution of standard TV sensors. The high resolving power of 100 line pairs/mm (10,000 TVL/RH) has been demonstrated over the entire sensing layer.

Figure 2 also contains a representative MTF for the lens that is used in the system. Its performance is excellent, and the lens/RBV combination permits resolution of fine detail while viewing an entire 2- x 2-inch substrate and also provides a sequence of sub-images by means of electron-beam zoom and steering at a standard 525 TVL readout rate.

Selection of electronic magnification

Selection of the electronic zoom ratio must be given careful consideration. A high zoom-ratio yields greatest image detail but, if excessive, can generate large amounts of superfluous data which slows down the substrate inspection rate.

Analysis of the RBV camera MTF with electronic zoom and video bandwidth filter is depicted in Fig. 3. The increase in width of a given line image is shown as a function of zoom ratio.

Examination of image detail dimensions of Fig. 1 and the image fidelity of Fig. 3 results in the conclusion that:

- The presence of complete print patterns can be ascertained with full substrate imaging (1:1 zoom).
- Assessment of major faults will require approximately 3:1 zoom.
- Detail examination and classification of minute defects in critical areas will require approximately 10:1 zoom.

System operation

The following description explains how the system is set up and used to perform inspections. First, a sequence of frames representing a fault-free substrate is recorded on the video disc. During this recording process the selected zoom

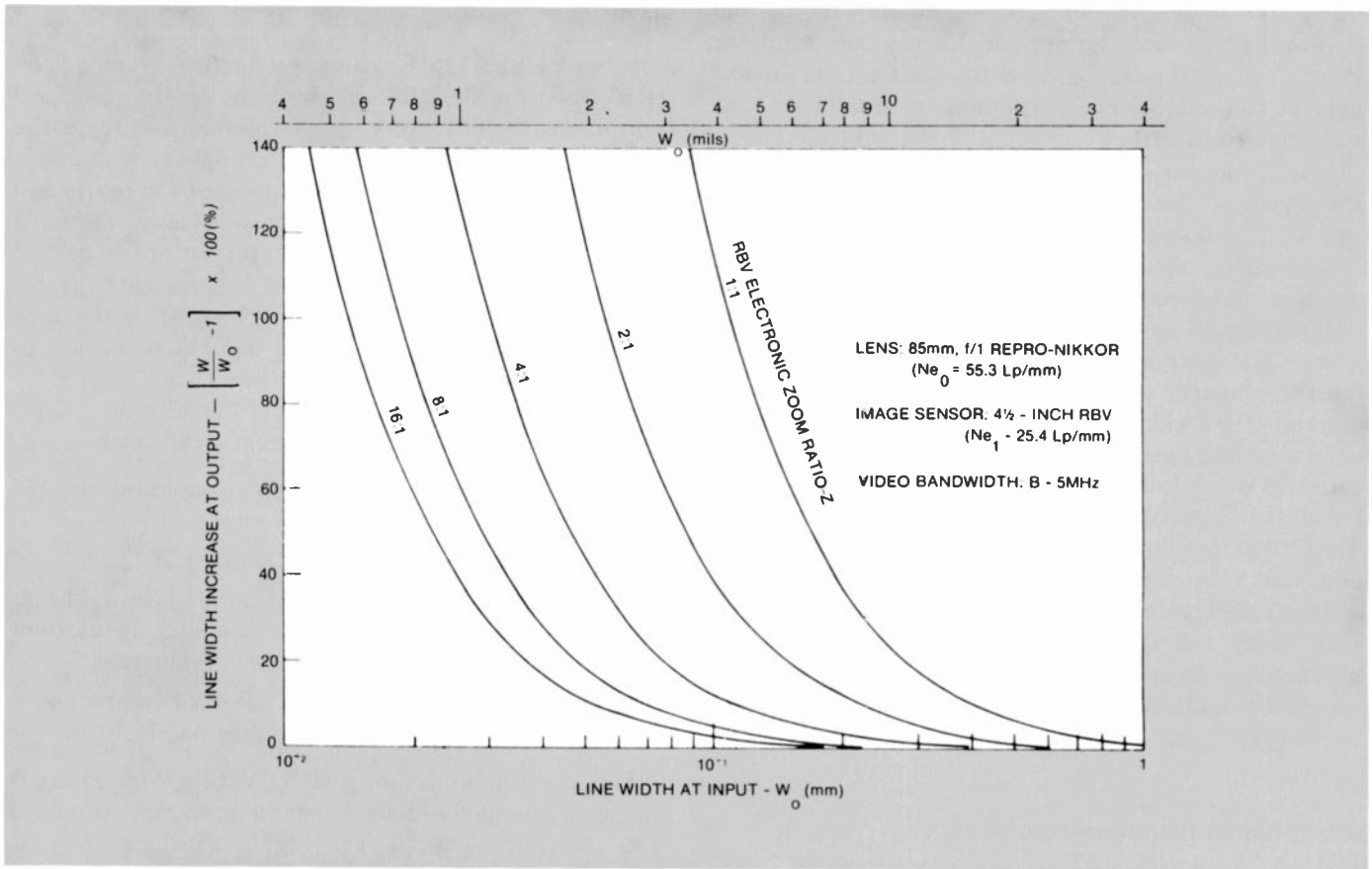

Fig. 3. Line image fidelity of video chain. A zoom ratio of 10 : 1 is optimum for the resolution of fine detail without excessive line-width variation.

ratios, illumination, and sector for each frame are automatically stored in the computer. Upon completion of the recording process, a program is stored in the computer, which will automatically perform this same sequence of operations during the inspection process. The system is now prepared to inspect substrates automatically. Figure 4 is a block diagram of the AIME system.

The substrate to be inspected is placed in the holding fixture, and the inspection program is initiated. The program selects the desired track on the video recorder, and via the time-base corrector, supplies this video to the video processor. Simultaneously and synchronously, live video from the RBV camera is fed to the video processor.

The video output of the RBV, representing the test substrate image, is compared line-by-line to the stored reference image in real-time (1/30 sec). The difference data resulting from the comparison of video level signals represents possible abnormalities. This data is sent to the computer system for final software processing and a pass/fail decision. This comparative approach significantly reduces the data processed by the computer (difference data only), minimizing computer memory requirements without impacting the inspection rate.

The video processor performs two functions. First, the difference between the RBV video signal and the video disc-recorder signal output is taken, digitized, and fed into the core memory of the AIME system computer. Second, the processor takes the same difference video signal and combines it with the RBV video signal, which is then displayed on the color video monitor.

The RBV video signal appears as a black-and-white image on the monitor. The difference video is directed to the red and green gun-driver circuits. Thus, if the RBV image is wider than the recorded image, the green color-gun output is increased, resulting in a highlighting of the greater than normal area. A similar result is obtained if the image is narrower than the recorded image, except now the red color-gun output is increased. If a defect is detected, the operator can observe the color-highlighted defect on the monitor. When the inspection is complete, the AIME control repositions the RBV beam scan to the next area to be inspected, and repeats the above process until the inspection is completed. The detection and location of defects are automatically recorded on a hard-copy line printer.

AIME software

Real-time-disc operating system (RDOS) and CLI

RDOS is a comprehensive and flexible operating system normally used with the disc-based S-130 computer system.

The Command Line Interpreter (CLI) is a dynamic interface to RDOS via the console and translates the input as commands to the operating system.

Run-time system

General The AIME Run-Time System (ARTS) performs the functions of program generation, test generation, and test execution. It is written in a high-level language (ALGOL) using structured programming techniques to obtain modularization for ease of maintenance and understanding. Assembly language modules are minimized

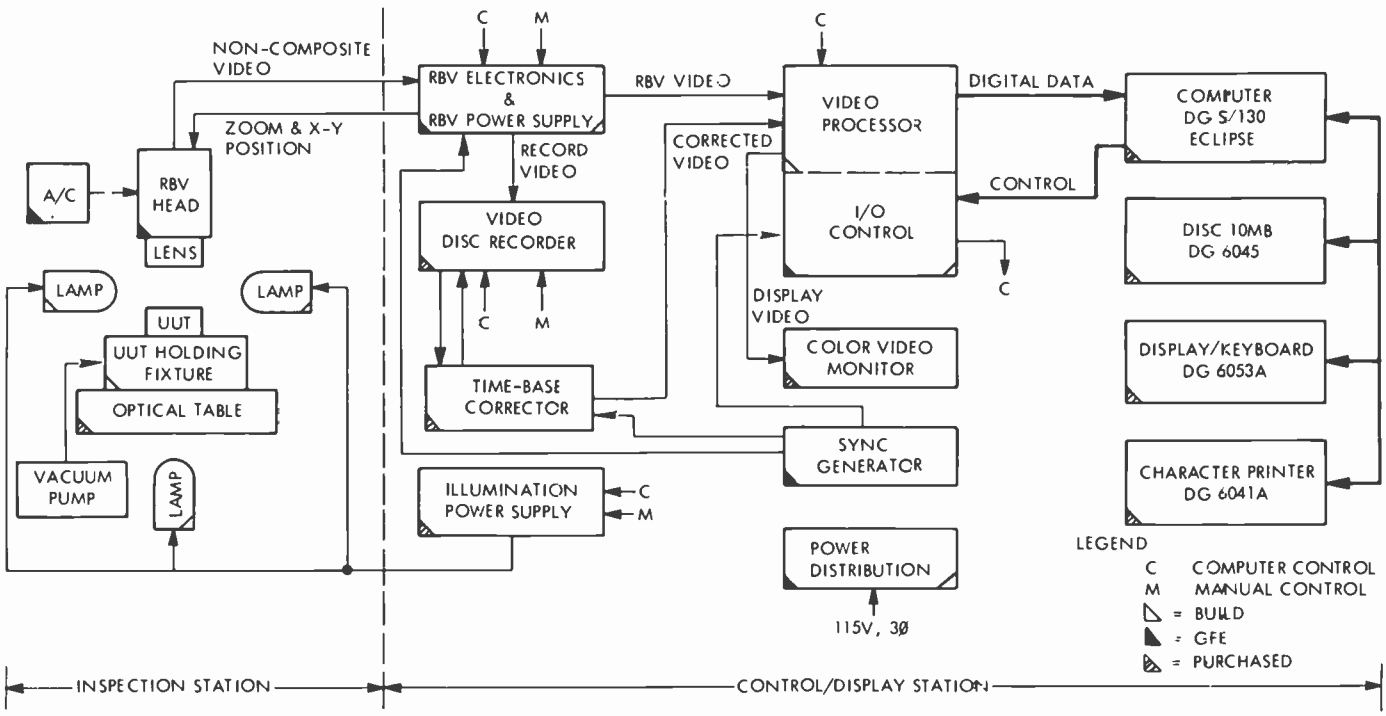

Fig. 4. AIME system block diagram. Recorded video is compared with live video in real-time to detect differences.

and used only where necessary for speed or special-purpose programming such as required in image processing.

Program generation can be accomplished either on-line or off-line. On-line program generation allows the user to try various setups for X-Y positions, zoom, illumination, and so on. When a specific test setup is decided upon, the system software will remember, on operator command, the exact setup and will place the test setup in sequence with respect to other tests contained in a source file listing.

Test Program Generation The test program generator is used to create automatic and semi-automatic test programs. The operator can activate and control the system from the keyboard. Sectors have been designated for the user in positioning the sub-images on the monitor. The higher the zoom ratio, the greater the number of sectors. Sectors are square and are numbered from left to right and from the top down. When a suitable image is seen on the monitor, the operator initiates the following system actions: (1) interrogation of all system status registers, and storage of the current setup data for the image; (2) the generation of a set of commands and related setup data, which when executed at a later date, will result in the exact same setup conditions; (3) indexing and storage of the image on the video disc-recorder; and (4) the generation of a MASK of the current image for the automatic test program.

Image processing

One of the outputs of the real-time video processor is a digital signal, which represents the video difference between the recorded video and the live video from the sample being inspected. When a difference exists, the digital level is a high or "1." When no difference exists, the level is a low or "0". The high level indicates that a defect is present in the sample, since the two video signals do not cancel. This digital representation of the difference video is strobed into computer memory using a 9.53-MHz strobe. The strobe is generated by counting down the 14.3-MHz clock from the time-base corrector unit. The 14.3-MHz clock is also used to generate the horizontal sweep frequency. Thus, the strobe is in synchronization with the entire video timing chain. The strobe is gated by the horizontal synchronization pulse of each video line, and the difference video is strobed into memory on a line-by-line basis. The frequency of the strobe and the synchronization method used causes each line of difference video to be stored in memory as 416 bits of information or twenty-six 16-bit words. This line-by-line storage is continued vertically down the entire image. The number of lines stored is 480, or thirty groups of sixteen lines each. The stored difference video is represented by 416 times 480 bits, or a total of 199,680 bits of information.

Defect detection is performed by counting the "ones" stored in memory. This counting is performed by examining the number of "ones" stored in a sixteen-bit by sixteen-bit sector of memory. Starting in the upper left corner, the

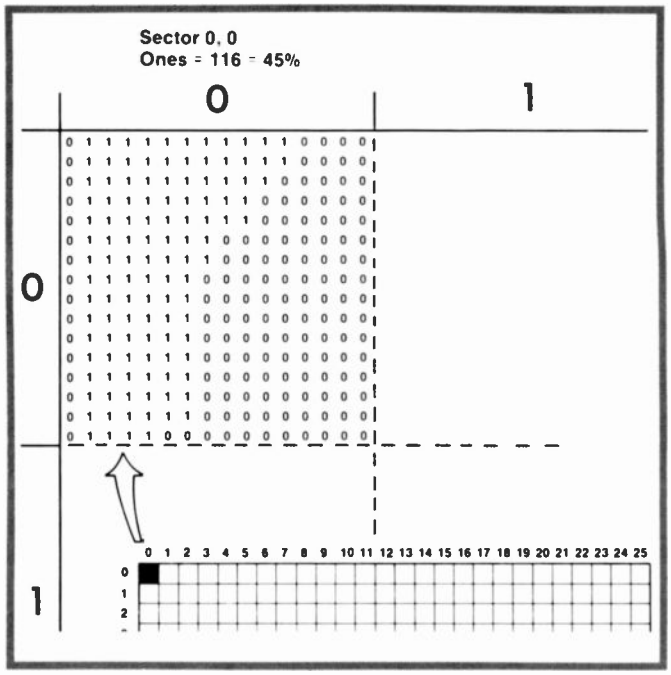

Fig. 5. Video processing technique. Storage and processing of difference video reduces memory requirements and speeds processing.

image is divided into 26-by-30 sectors. The sector 0,0 is detailed in Fig. 5. Each sector is examined to determine the number of "ones" contained in that sector. This examination is continued across the image until all sectors in that row are examined. The processing then looks at the next row of sixteen bits (starting with sector 1,0) and continues this pattern until the entire image (780 sectors) has been examined. The maximum number of "ones" that can be contained in any sector is sixteen times sixteen or 256 "ones." A count of 256 indicates a defect that covers the entire sector. In the sample sector shown in Fig. 5, there are 116 "ones" or 45 percent. The software program is designed such that a threshold can be designated to define what level of "ones" constitutes a defect within a sector. This limit is set as the percentage of "ones" within a sector which constitute an acceptable level. If the percentage is set at 10 percent, the number of "ones" within a sector would have to exceed 26 in order to be classified as a defect. This threshold technique permits the system to ignore random "ones" generated by noise, misregistration and system instabilities. After the program has examined all sectors, the printout specifies which sector, by row and column, had the greatest number of "ones." If none of the sectors exceed the limit, the substrate is considered acceptable.

Mask Generation The strobe frequency selected to store the video difference provides a granularity of approximately 0.4 mils. Therefore, each bit in memory represents a linear dimension equivalent to 0.4 mils of substrate printing. Development testing showed that the variations or roughness of the edge of a printed line could be as great as 0.5 mils. In addition to these variations, printed misregistrations of up to 1.0 mil were also observed. The combination of these variations resulted in high incidence

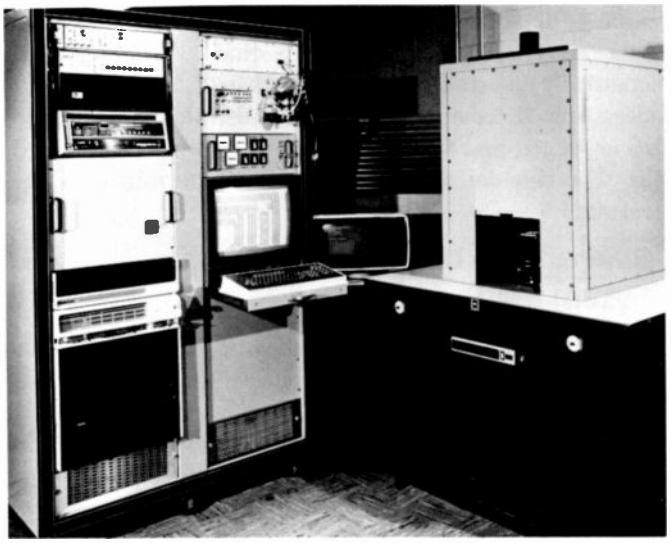

Fig. 6. AIME system. The system uses standard commercial video equipment to reduce costs and simplify maintenance.

of erroneous defect callouts at the line edges. As a means of minimizing these false alarms, a software program was developed to generate a mask pattern for each image. Each reference pattern is strobed into memory without differencing. The software program then looks at each line of the digitized pattern, first horizontally and then vertically. When the program detects a data transition at an etch boundary, it inserts a block of "0"s before and after this transition. The number of "0"s to be inserted is entered into the program prior to the start of the mask generation. Since each "0" is equal to 0.4 mils, the mask width at the etch boundary can be selected in increments of 0.4 mils. The mask automatically inserts "ones" at all other memory locations. The resultant mask data is stored in the computer disk storage. When processing an unknown sample, the mask data is read into computer memory and "AND"ed with the difference video data. The resultant data is then ready for processing and the effects of printing roughness and misregistration have been minimized.

AIME hardware

A photograph of the AIME system, shown in Fig. 6, consists of two major elements: the Control/Display Station and the Inspection Station. A magnified image of an actual hybrid substrate can be seen on the video display.

Inspection station

The inspection station consists of a shrouded structure on an air-suspension optical table as shown in Fig. 7. A precision, three-axis, adjustable holding-fixture orthogonally registers the hybrid substrate to the RBV optical axis. The RBV is rigidly held to the table and external cooling air is ducted to the assembly to preclude vibrations, and a positive internal shroud pressure maintains a dust-free atmosphere.

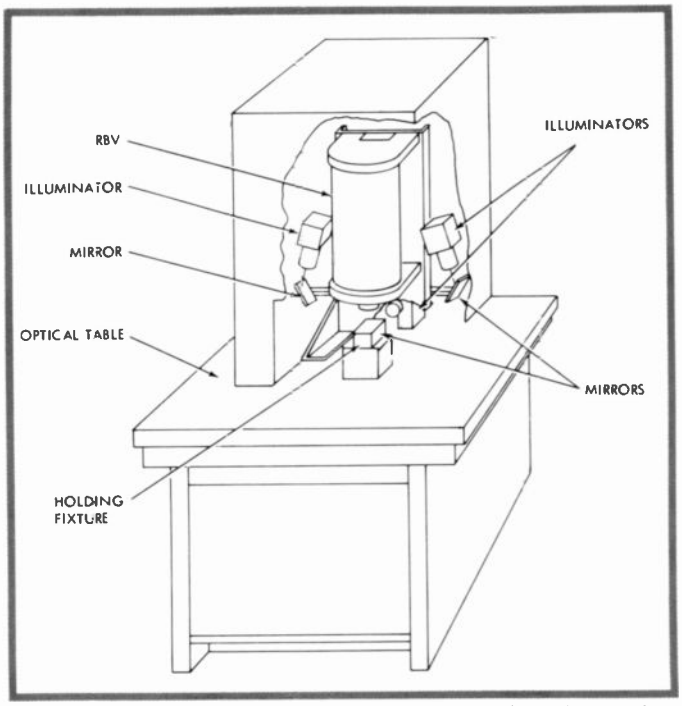

Fig. 7. Inspection station. The ability to illuminate the substrate from the front or rear permits optimization of contrast levels.

Two illuminators are located 180 degrees apart and the defocused filament is imaged via folding mirrors to provide frontal illumination for pre-cap inspection. A third illuminator (located on the optical table) is provided to produce back lighting for print inspection. Light from this illumination is folded 90 degrees by locating a mirror beneath the holding fixture. The hybrid is held in precision alignment against three reference points with a back-plane vacuum around the edges, providing a central open area for the back illumination.

Control/display station

The control/display station consists of a double-rack assembly. One of the two major functions performed by this station is control of the AIME operating modes. This control is maintained by the computer and associated peripherals. The remaining elements of the control/display station are associated with the RBV and video processor. These include: the video disc recorder, sync generator, time base corrector, color-video monitor, and illumination power supplies. The AIME system can be controlled either with the computer and associated interface (CPU control), or with controls located on the front panels of the RBV electronics chassis, the video-processor chassis, and the video disc recorder.

Fault detection

The evaluation of the AIME system capability to detect faults on printed substrates consisted of testing 12 sub-

strates containing faults typical of those found in the manufacturing process. Line widths represented are 4, 6, 8, and 10 mils. Faults contained on the 12 defective substrates include breaks in the printed path, excessive ink along a printed path, "necking-down" or narrowing of the printed path, and shorts between two printed paths.

AIME is programmed to automatically test substrates in the zoom-10 mode of image magnification. In this mode of magnification, the substrate is recorded or examined in 49 separate sectors. In addition, each sector is electronically subdivided and evaluated as a 26 x 30 matrix of subsectors. Should a defect be detected, the row and column of the substrate containing the defect is printed on the AIME printer. In the event of multiple defects within a sector, the largest defect is reported.

At the start of testing, each of the substrates was individually inspected by the test operator, using AIME in the manual mode of operation. The defects, visually detected by the test operator, were then recorded on a printed enlargement of the substrate layout. A defect-free "Master" substrate was then recorded by AIME in the automatic mode and a "go-chain" test was made in which the recorded substrate image was compared with the actual "Master" substrate. This test verified the proper operation of AIME.

Each defective substrate was then evaluated by AIME. AIME was programmed to operate in the automatic mode with the verification flag set so that the test operator could confirm the defect detected by AIME. Mechanical realignment of the substrate was performed during the test as required by the test operator to minimize misalignment between the substrate and the "Master" recorded image. The defects detected by AIME were automatically printed on the AIME printer, and were also manually recorded by the test operator on data sheets.

Each defect on a substrate was classified as to size. Three size classifications were used — 0 to 3 mils (small), 3 to 6 mils (medium), and greater than 6 mils. The defect size was noted on the data sheets. In this manner, it was possible to subjectively judge the ability of AIME to detect different-sized defects. The results of the AIME demonstration system to detect defects of varying size are summarized in Table I. These results indicate that overall, AIME successfully detected 96.4% of the substrate defects. AIME successfully detected 100% of the substrate defects size 3 mils or larger, and 82% of the substrate defects less than 3 mils. The calculated percentages were determined by the formula:

$$\frac{\text{(Type or Total) Defects Detected}}{\text{Total Number of Defects}} \times 100 = \%\ \text{Detected}$$

The total number of defects is the number of defects per substrate less defects in excess of one per sector. AIME will detect the largest defect in a sector; therefore, it is inappropriate to include more than one defect per sector in the above calculations.

Conclusions

Feasibility of a computer-controlled high-resolution television system for automatic inspection of hybrid substrates has been demonstrated. The following achievements were validated by this program:

- Automatic detection of line widths varying from 3 mils to 10 mils.
- Automatic detection of opens and shorts varying from 1 mil to 10 mils.
- Computer-controlled beam steering and raster zoom for high-speed processing.
- Video display with color augmentation for visual analysis of substrate faults.
- Hardware functional compatibility demonstrating real-time video-comparison technique.
- Validation of software algorithms for automatic program-sequence control and fault processing.

Acknowledgment

The work on this project was funded as part of the

Table I. Summary of AIME data. Defect detection was demonstrated for a large variety of substrate faults.

Substrate Number	2A1	3A1	3A2	4A1	4A2	5A1	5A2	6A1	6A2	7A1	8A1	8A2	*Total*
Total defects	24	33	26	34	30	19	16	22	20	36	35	36	331
0-3-mil defects	5	6	1	2	0	12	10	2	4	11	4	6	63
3-6-mil defects	7	14	8	15	13	6	6	10	9	15	13	20	136
>6-mil defects	12	13	17	17	17	1	0	10	7	10	18	10	132
Total defects detected	24	30	26	34	30	16	15	22	20	35	34	33	319
0-3-mil detected	5	3	1	2	0	9	9	2	5 4	10	3	3	51
3-6-mil detected	7	14	6	15	13	6	6	10	9	15	13	20	136
>6-mil detected	12	13	17	17	17	1	0	10	7	10	18	10	132
Defects missed	0	3	0	0	0	3	1	0	0	1	1	3	12

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Left to right: Richard Wildenberger, Manager, Design Engineering; and John Laskey, Manager, Program Management.

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Mr. Laskey joined RCA in 1955. Automatic test equipment technology matured during this period, and he was part of the team that developed RCA's present ATE Product Line. During the 1960s, he served as Project Engineer and Senior Project Engineer on the LCSS Program. In the early 1970s, he was a key member of the team that developed EQUATE, the first third-generation ATE. Since then Mr. Laskey was the Program Manager responsible for development of the U.S. Army's ATE language OPAL, and the Program Manager for the AIME system for hybrid microcircuit visual inspection.

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J.K. Peters

Automatic wire-wrap control system

Literally billions of wire-terminal connections used by electronics firms like RCA demand automatic wire-wrap machines with numerical control.

Abstract: *Over the past 12 years, the Advanced Technology Laboratories Computer Center has developed a system of computer programs to produce wire-wrap and test equipment control tapes or cards from engineering inputs. The system accepts wire-list or pin-signal list inputs in universally general formats, making the engineering/manufacturing interface relatively simple. The system also generates valuable documentation outputs, such as cross references and diagnostic listings. The control media (punched paper tape and cards) are currently used to operate Gardner-Denver horizontal and vertical automatic wire-wrap machines, various semiautomatic machines, and a DITMCO automatic panel tester.*

Wire-wrap is a solderless termination technique that costs little and is highly reliable. The connection is easily and rapidly formed, and resists — without failure — extremes of environmental stresses.

The electronics industry makes literally billions of wire-terminal connections each year. Maximum savings in time and labor are realized through the use of automatic machines. The latest models of Gardner-Denver automatic wire-wrap machines can terminate approximately 800 wires per hour, that is, about 6,000 wires per eight-hour shift. Numerical control is provided by punched cards or punched paper tape.

The wire-wrap connection is formed by tightly wrapping solid wire around a sharp-edged rectangular terminal so as to cause an indentation in both the terminal and the wire. Wire-wrap combines excellent mechanical integrity with a high degree of electrical stability.

The Gardner-Denver automatic wire-wrap machine (Fig. 1) is air-operated, electronically controlled, and capable of wrapping a network of interconnecting wires according to a programmed input signal. Two to four seconds are required to complete a single wrapping cycle. During this period, a length of wire is cut, stripped, dressed to a particular wire pattern, and wrapped at both ends to two separate terminals.

The automatic wire-wrap tool consists of a stationary sleeve, a wrapping bit, and a means of rotating the bit. The wrapping bit has an axial opening provided to house a terminal during wrapping. An additional groove, or feed slot, is cut longitudinally along the outside circumference, parallel to the first. This accommodates the stripped wire, which is inserted into the end of the tool, then bent over a notch in the stationary sleeve and thereby anchored. During wrapping, the bit is rotated around the stationary terminal, pulling the bare end of the wire out of the feed slot and around the terminal.

Initial pressures of about 100,000 lb/in^2 exist in the center of the contact area. Cold flow causes a drop in pressure to about 29,000 lb/in^2 immediately following wrapping. This pressure remains nearly constant for the life of the connection.

Experiments involving thermal shock, temperature cycling, vibration testing, and exposure to moisture indicate that severe environmental conditions have relatively little effect on wire-wrapped connections.

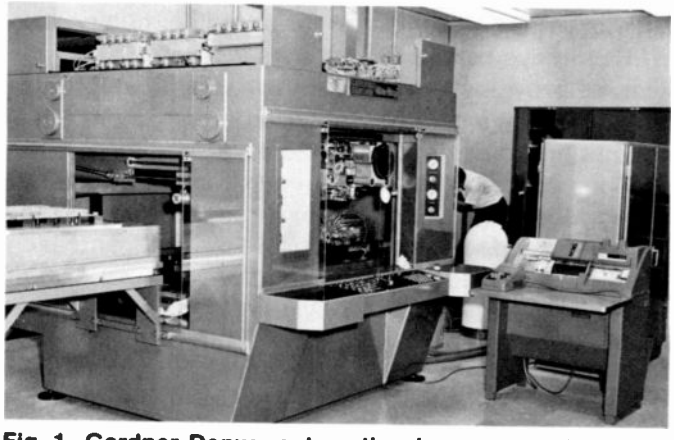

Fig. 1. Gardner-Denver automatic wire-wrap machine

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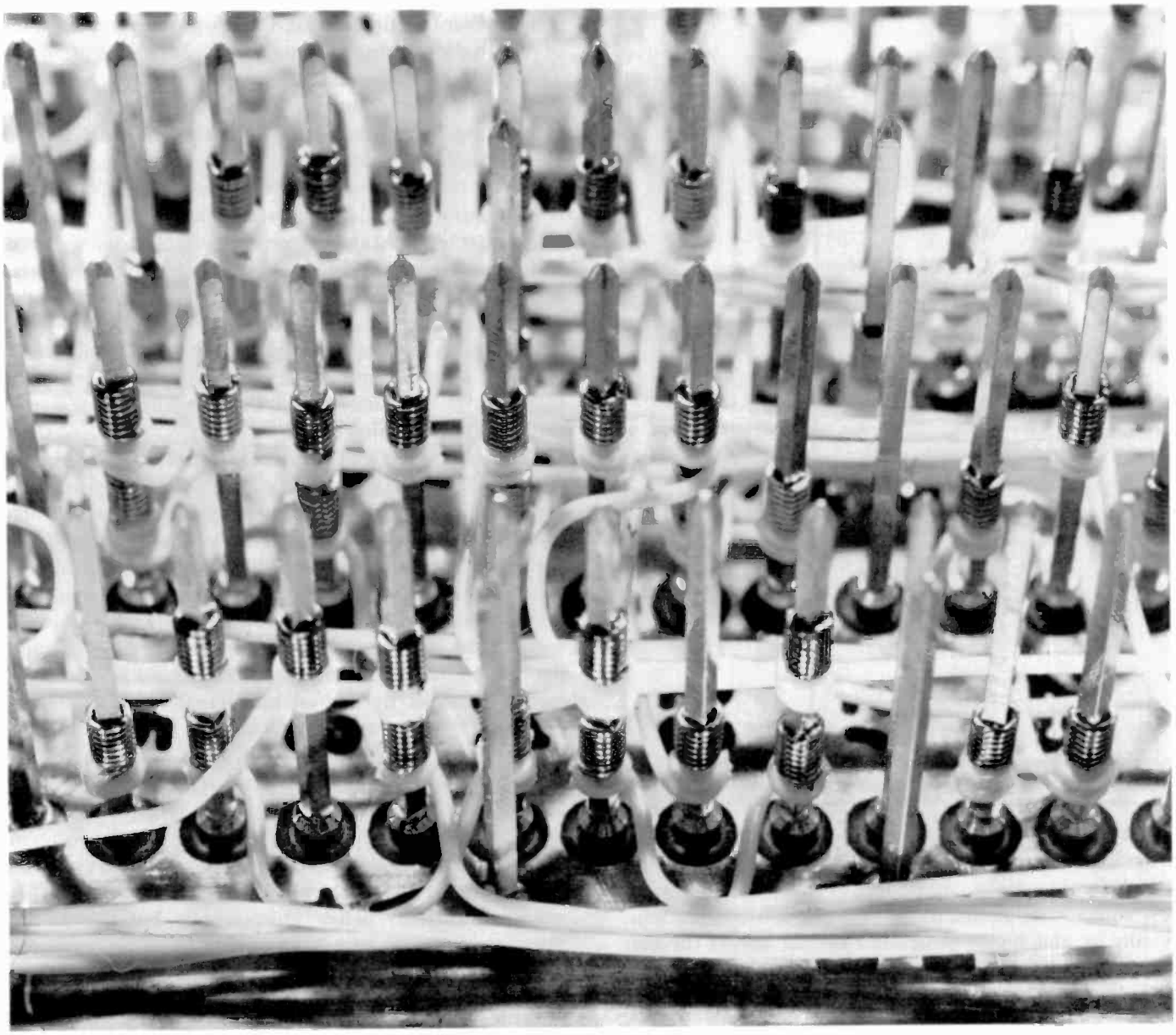


Fig. 2. Typical wire-wrap multilevel connections.

Three wires may be terminated on one wire-wrap terminal; the vertical level specified is referred to as the Z level (Fig. 2). The Z levels are arbitrarily designated as first, second, and third level. The first Z level is that wiring connected nearest the base of the terminal. Preferred wiring technique dictates that wiring between terminals be accomplished at the same level, to avoid aggravation of wire-removal problems. The newer Gardner-Denver machines perform terminations in this manner, with both ends of a given wire always at the same level.

Input requirements

The data inputs to the ATL Computer Center system of wire-wrap programs may be "from-to" lists or "pin-signal" lists. The primary function of a from-to list is to stipulate the end-terminals of each wire. A pin-signal list identifies the signal that will be served by each terminal on the panel.

Computer programs translate this input data into X-Y coordinates on the panel to be wired. These coordinates are combined with auxiliary information and then encoded on punched paper tape or punched cards. These media control the operation of the wire-wrap machines. One card or one paper tape record will have all the information required by the automatic wire-wrap machine to route one wire in a prescribed manner, to place the wire in a predetermined position on the panel, and to wrap the ends of the wire on specified terminals.

LOOP program

Although the ATL wire-wrap control system consists of over two dozen computer programs, the discussion here is limited to the more important ones.

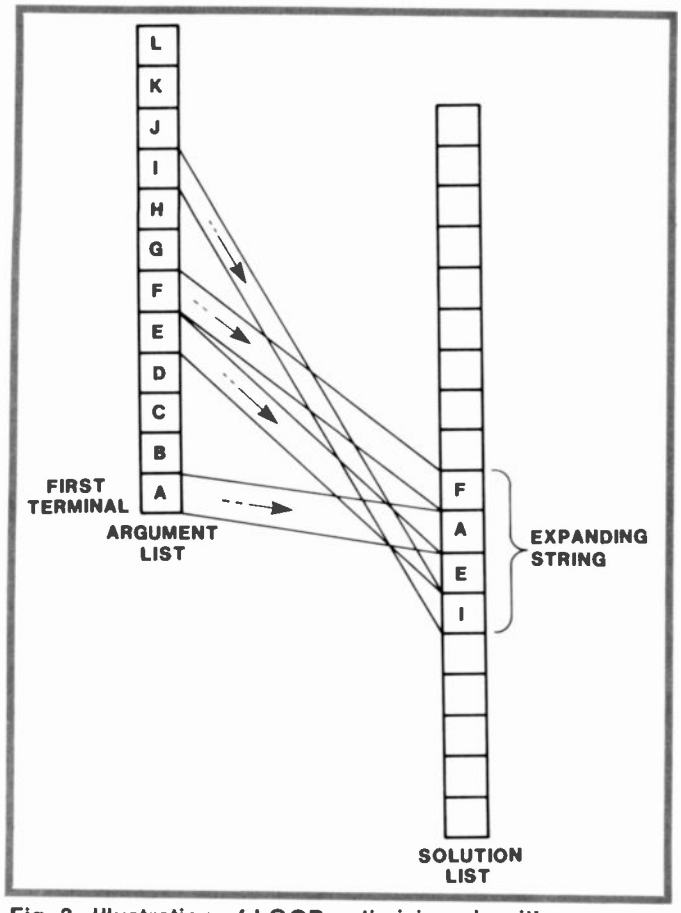


Fig. 3. Illustration of LOOP optimizing algorithm.

The LOOP program, the most central and the most used program in the ATL system, has two basic functions. LOOP first translates component or panel terminology to X-Y coordinates needed by the machine-driving programs. A concise and highly structured format allows the user (commonly a programmer) to describe to the program a way to calculate the coordinates from the terminal descriptions. The number of cards used in this parameterization process is kept to a minimum without sacrificing flexibility.

The other function of LOOP finds ways to connect a set of terminal locations with a single path of minimum length. This problem is classically referred to as the "traveling-salesman problem," or as a "closed Hamiltonian circuit." Several algorithms have been published that will always give an optimal solution but at excessive cost in both computer time and memory. The algorithm used by LOOP is a compromise that is relatively quick.

The first terminal and the terminal closest to it are placed in the middle of the solution list and removed from the argument list. Next, terminals nearest to either end of the expanding string are added progressively until all of them have been accounted for (Fig. 3). The total length and tentative solution are stored. The original order of the terminals is randomized and that random order is run through the algorithm again.

If the total length of the new solution is less than that stored, the new one replaces the old. This process is repeated a number of times, approximately equal to the square root of the number of terminals in the string. Then the string is written out in wire form, and the next string is considered. This output includes the terminal description, the level of the wire (first, second or third), the other terminal description, the level again, the signal name, and the X-Y coordinates of the terminals, all in a 60-character record readable by any of the actual machine-driving programs.

The use of randomizing strings is known as a Monte-Carlo technique. To appreciate the need for randomizing, consider the set of points representing terminal locations shown in Fig. 4. Running through the above algorithm in order and without randomizing, we come to solution J,A,B,C,D,E,F,G,H,I,K, which is non-optimal. Another example, perhaps better conceptually but not as appropriate to usual wire-wrap situations, is the sawtooth example in Fig. 5. Unless this string is considered in precisely the right order (that is, A-J) the optimal solution is difficult to reach without trying all possible permutations or randomizing as above.

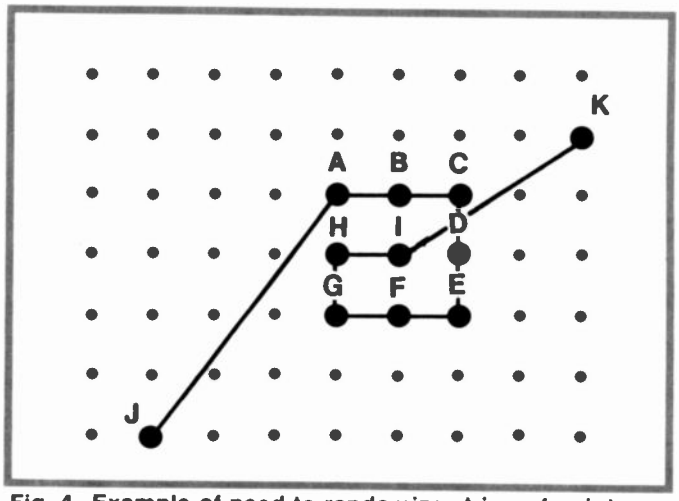


Fig. 4. Example of need to randomize string of points.

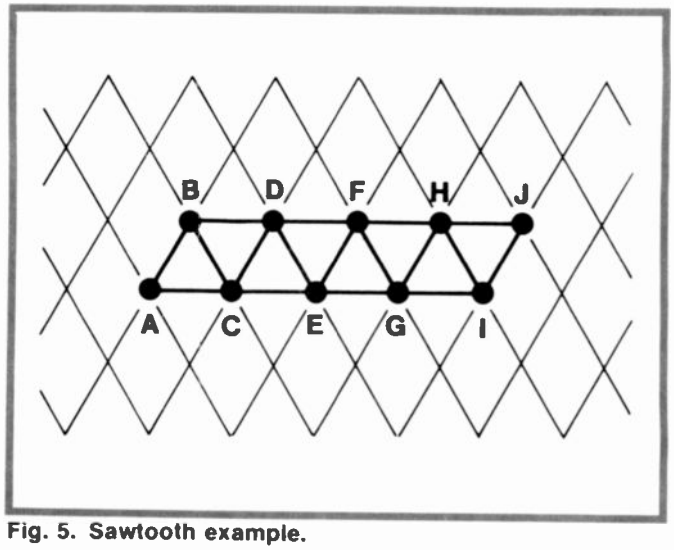


Fig. 5. Sawtooth example.

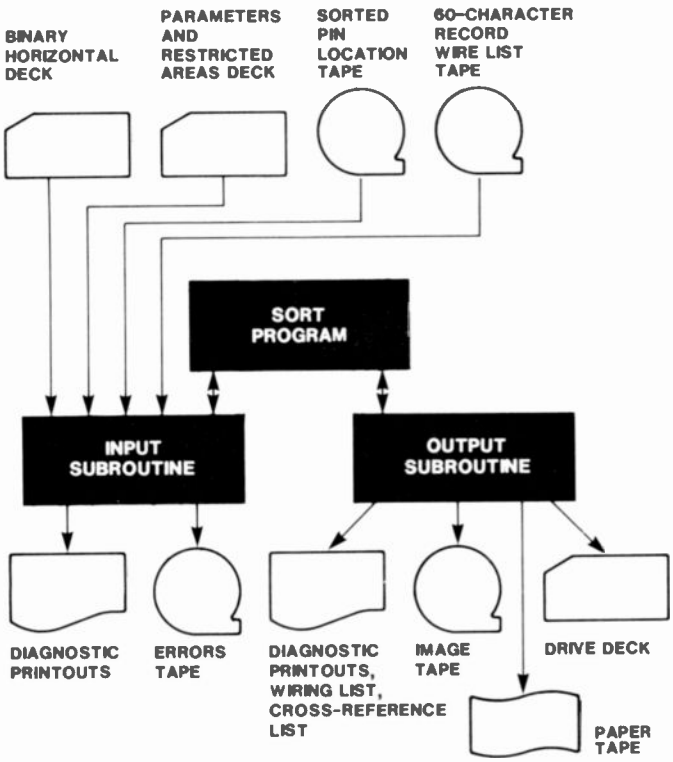


Fig. 6. Simplified flowchart of automatic wire-wrap program.

Wire-wrap programs

Programming for the automatic wire-wrap machine consists of converting wire-connection lists or wire-connection data to machine language. Machine information is then recorded on a punched card that in turn provides input to the machine. One card or one paper tape record will have all the information required by the automatic wire-wrap machine to route one wire in a prescribed manner, to place the wire in a predetermined position on the panel, and to wrap the ends of the wire on specified terminals. Any or all of these routing, patterning, or wrapping considerations can be controlled by the programmer.

Programs GDSQNG, GDSTNG, GSQNG2 and RESQGD are the same basic program, with only the "via-point" subroutine changed. The program is structured into an input section and an output section, each being called by an RCA TDOS SORT main program. These sections function as if they are separate entities.

Figure 6 shows a simplified flowchart. The input section does general setup and parameter readings, then reads records from the 60-character wire-list file created previously, usually by program LOOP, creating as many as five sort records. The first two records are for the eventual cross-reference listing if required. Two separate records are created for checking for level conflicts by the locations of terminals rather than by their descriptions. Next, the "via-point" subroutine is called to get the desired wire-wrap pattern.

The via-point subroutines used in GDSQNG, GDSTNG, and GSQNG2 have code that prevents violations of described restricted areas. This is done by expanding the legs of a U-shaped pattern to specified limits in the four different rotational positions, progressively, until either all wires and dressing fingers will drop in legal places, or a prescribed limit is reached (Fig. 7). Then, rear dressing fingers (or Z patterns) are tried (Fig. 8). If no legal pattern is found, the pattern that would have been generated if no restriction were applied, is generated and a message is then printed.

The via-point subroutines call functions to determine if a tentative via-point is in a restricted area, or if a wire crosses through a restricted area, or if the via-point is either directly over a terminal or at a legal distance from a terminal. The restricted areas are of two types — a wire restricted area or a via-point restricted area — and are simply rectangles described by their corner points.

The terminal test for via-points is optional (Fig. 9). Terminal locations are read from a tape which is sorted first by the Y-coordinates, then by the X-coordinates. The unique Y-coordinates are stored in one array and the X-coordinates corresponding to each Y-coordinate in a separate array. Thus, duplicate Y values are not stored, greatly conserving memory. Up to approximately 20,000 terminal locations are permitted.

Because this Y-location array is kept in sorted order, the binary search method is used to access it, making the search

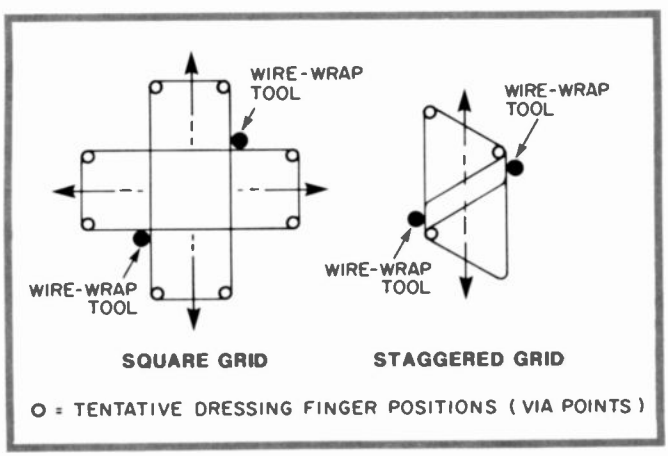


Fig. 7. Examples of expanding U-shaped patterns.

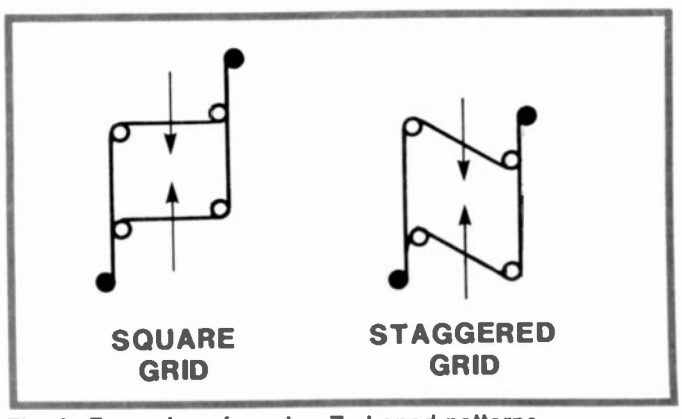


Fig. 8. Examples of moving Z-shaped patterns.

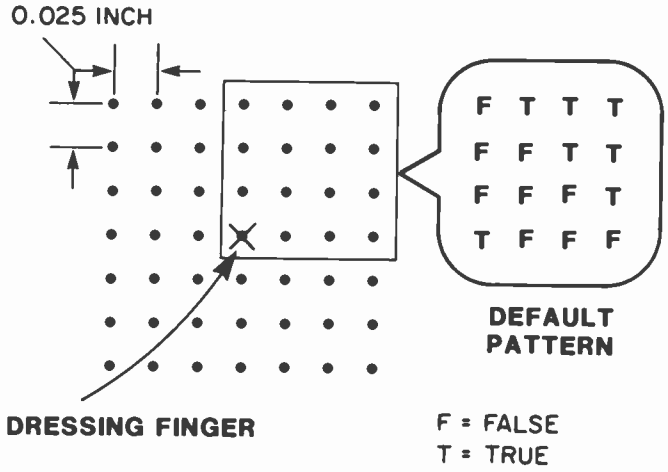


Fig. 9. Illustration of reject pattern for terminal test.

very quick. The definition of legal places to drop a dressing finger is made by a four-element by four-element logical array representing the upper right corner of a six-by-six module (0.025-inch) domain around each terminal. This pattern, called the reject pattern, can be altered at run time. "Altering" would be used to prohibit using a terminal as a via-point to prevent tight wires in a densely wired panel. Altering could also loosen up the restrictions to allow more wires to pass on a complex panel.

Another feature of the standard via-point subroutines is that the panel is rotated 90 degrees each time a new wire is considered. The patterns generated are designed so that this rotation distributes density throughout the terminal area.

After the via-points are assigned, the main input routine attempts to assign dressing finger locations, tool locations, table rotational position, and, in the case of the horizontal wire-wrap machine, pallet lateral position to form the wire. Sorting information is then generated, and the completed wire record is released to the main program (SORT).

Each record released, including the cross-reference and level conflict record, has a group key in the highest location which will cause the records to sort into logical groups, with records within each group sorted in different ways. This technique is hard on the disks but allows a single-sort file to be handled.

The output section first gets a setup record, then records to check for level conflicts. The records have been sorted by the location of one of the pins and contain the Z-level and the full original input record. If a pin is found to be used more than once on a level, a diagnostic message is printed, and an internal sequence number for the wire involved is put in a table for later rejection or warning messages. In addition, a check is optionally made for terminals which appear with different signal names and appropriate messages generated.

The next set of records coming to the output section are those which have all the information necessary to generate the media to actually run the wire-wrap machine. These records have been sorted in an order which is believed to operate the machine in the fastest and best way. The level

Fig. 10. DITMCO test system.

conflict table is searched and, if a conflict is known to exist, appropriate actions are taken. A table of an internal sequence number for each record generated on the output media is kept for later use in the cross-reference listing.

The last set of records is for the so-called cross-reference listing. This is basically a double-entry wire listing in terminal order, with the sequence number of the generated wiring record. It is printed two-across but is sorted down the page.

Utility programs

Some of the ATL wire-wrap programs are designated as utility programs, because they are used in both the wire-wrap software system described above and in the DITMCO software system. INPLST and INPT50 list card image files from the card reader or tape while possibly also writing a control tape. KLOOP1 and KLOOP2 analyze complete wire lists, generating Z-levels and signal numbers. The STRING program processes signals, generating string listings similar to that produced by LOOP, and then flags errors such as open circuits, level conflicts, and star patterns.

DITMCO programs

After the wiring of a panel has been completed, it may be desirable to check the accuracy of the wiring by manual or automatic means. Studies have shown that computer-programmed automatic wire-wrapping achieves an error rate of less than 0.01 percent. However, if the required error rate must approach zero, automatic testing is preferred.

At ATL, Camden, New Jersey, a DITMCO test system (Fig. 10) is capable of automatically checking for connectivity and short circuits in panels containing up to 50,000 terminals. This equipment is driven by paper tapes created by a combination of the utility programs and four special DITMCO programs.

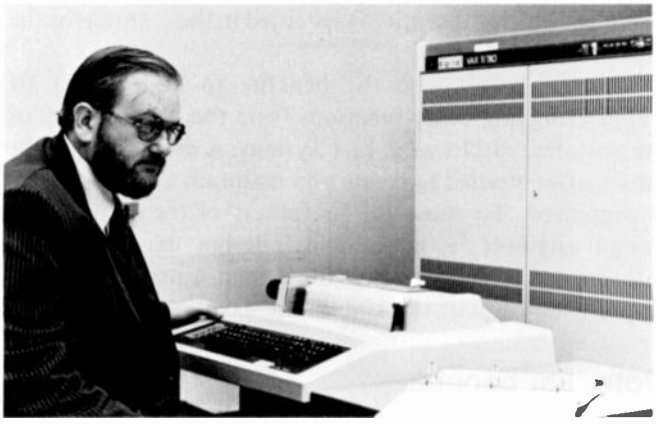
The first DITMCO program, called ADDADD (from "ADD ADDress"), translates input terminal data (identical to the from-to data used by the wire-wrap programs) to five-digit addresses for the DITMCO test system. Three DITMCO programs (DTMCO1, DTMCO2, and DTMCO3) use the data from ADDADD to generate sorted listings in DITMCO machine address

order, signal name order, and terminal description order. These programs also generate diagnostic listings of possible problems (such as shorted signals and other inconsistencies) and produce punched paper tapes to drive the DITMCO test system. The bulk of these listings was minimized by printing several items across the page in order to facilitate their use by test personnel.

Summary

Although the Advanced Technology Laboratories' wire-wrap computer programs have proven very effective, they do require considerable turnaround time because the SPECTRA 70 computer in ATL is run as a batch processing system. As an example, the average wire-wrap job takes two to three weeks to process. However, the Digital Equipment Corporation VAX computer (Fig. 11), that ATL is installing in the spring of 1981, should reduce processing time to only two or three hours. This reduction in turnaround time will be achieved by using the interactive capability of the VAX computer. In addition, the interactive capability will facilitate checking for errors in the encoded geometry descriptions in the wire lists, etc. Consequently, it will be possible to complete a wire-wrap job in one sitting.

Fig. 11. VAX computer.



Jack Peters has worked in systems and applications programming since joining RCA in 1966. He started with the former Electronic Processing Division, then transferred to the Advanced Technology Laboratories in 1968. In ATL he generated the automatic wire-wrap control system, and has maintained a close relationship with Camden Manufacturing, both in the Government and Commercial areas. He often plays a major role in the Engineering/Manufacturing interface. Jack also provides computer user consultation to engineers, as well as maintaining the operating software for the Advanced Technology Computer Center. He is now involved with converting the Computer Center to the new VAX 11/780 system. Jack is a Senior Member of the Engineering Staff of ATL.

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Camden, N.J.
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R.A. Monat|W.C. Roberts

Consumer Electronics' automated drawing list system

By entering a list of parts data into a computerized database, a design engineer may extract information to assist him in product design.

Abstract: *This paper describes the concept of Consumer Electronics' Drawing List (list of parts) and shows how design engineers may extract information from the computerized version to assist in the design process. After an introduction, potential benefits of the Automated Drawing List System are presented. Information elements in the drawing list are explained. To show the usefulness of the system to a design engineer, we develop a hypothetical example. Finally, ideas for the future are explored.*

A drawing list (DL) is the primary vehicle to communicate a product design from Design Engineering to other operations within the Division such as Manufacturing, Purchasing, Production Planning, and Cost Standards. Other documents — for example, mechanical drawings — are necessary to completely communicate a design. The DL can be thought of as an index to the documents.

During the designing process and after the design is completed, other operations within the Division, using the DL, work with Design Engineering to convert the design into a finished product. Cost Standards determines the standard cost of a design by considering the materials and labor necessary to manufacture the product. The cost is one of the factors used to evaluate a design. Purchasing lines up suppliers in advance to assure an adequate supply of parts, and, when required, contracts for tooling at an early date. Manufacturing uses the computer to convert the DL to a "Bill of Materials" so that Purchasing can order parts from the suppliers, and so that the manufacturing process can be developed.

Each DL in the automated version can list the parts necessary for up to twelve related assemblies. An assembly, also called a group, is identified by the drawing number of the DL and its group number (3 digits) on the DL. In the body of the DL, each item line includes, as basic information, a drawing-part number, a description, and the quantity per group. Each group is defined by those items for which a quantity is specified in the column for the group.

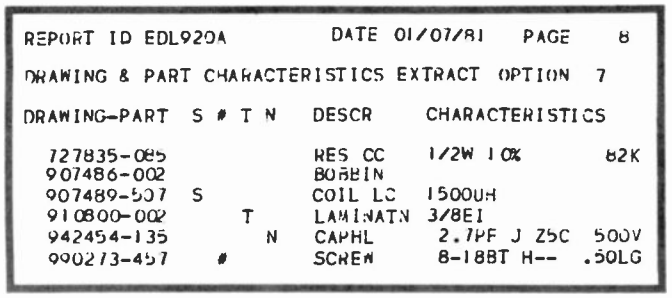
This paper presents the benefits to be realized by Engineering and other functions from the development of the Automated Drawing List System. A discussion of the information needed to create and maintain a Drawing List is presented. To show the usefulness of the system to a design engineer, a hypothetical design example using information in the system is developed. Finally, ideas for future expansion of the system are explored.

Potential benefits

Over the years, each operational function has entered information consistent with its own information retrieval needs into the central database. Most information was based on DL data but Engineering did not input the DLs to the database. It became apparent that there were potentially many benefits for the Division if Engineering would enter the complete DL information. These include:

- More-accurate, up-to-date input to the database coupled with a reduction of total input workload.
- Rapid transmission of data to distant manufacturing plants.
- More-versatile and faster cost guidance during design.
- Rapid access to current "where-used" and material-status information.
- Automatic generation of part description from part number input.
- Facilitation of the input of a new DL by additions and deletions to a similar one already in the file.
- Reduction of hard-copy distribution.
- Earlier, more-accurate availability of information to help

Reprint 26-6-12
Final manuscript received March 25, 1981.



REPORT ID EDL920A DATE 01/07/81 PAGE 8

DRAWING & PART CHARACTERISTICS EXTRACT OPTION 7

DRAWING-PART	S	#	T	N	DESCR	CHARACTERISTICS
727835-085					RES CC	1/2W 10% 62K
907486-002					BOBBIN	
907489-507	S				COIL LC	1500UH
910800-002			T		LAMINATN	3/8EI
942454-135				N	CAPHL	2.7PF J Z5C 500V
990273-457		#			SCREW	8-18BT H-- .50LG

Fig. 1. Typical master parts file entries. Each part of the DL system has an entry in the master parts file. The data is a drawing-part number, an abbreviated description, and characteristics used to modify the description.

Manufacturing, Purchasing, and Cost Standards in their planning.

- More-rapid availability of engineering change information.
- Means to expedite engineering parts approval (E-Approval) for any model.
- Allow the occasional user to access information without having to maintain his own current files.
- Information retrieved is current.

Improvements in techniques for data management, coupled with the added complexity of widely dispersed manufacturing facilities, further added to the motivation to implement a complete Automated Drawing List System.

DL data entry

Master parts file

At the heart of the Automated Drawing List System is the master parts file. A single master parts file supports all DLs. For each part, there is a record in this file. The elements of interest to the engineer in each record are the drawing-part number, the part name, characteristics describing the part, and a special characters field. The part name and characteristics comprise the description field. A drawing-part number is a unique identifier for each part and is used to specify individual parts or assemblies. The part name, an eight-character string, is used to grossly classify the part. For example, the part name RES CFFP specifies a carbon-film flameproof resistor, and RES WW specifies a wire-wound resistor.

The characteristics, an eighteen-character string, are used to further specify the part. Within this field are attributes peculiar to the part name. Continuing with the above example, for the part name RES CFFP the characteristics are power dissipation, tolerance, and resistance. A possible characteristics string for a 500K ohm 1/4 watt resistor with a 10 percent tolerance is: 1/4W 10% 500K. A manual lists the acceptable part names and the format of the associated characteristics field. Lastly, the special characters field is used to denote four attributes (S, #, T, N) which may apply regardless of part name. The first of these characters (S) is used to indicate a part which is "safety critical," that is, the part, independent of application, affects the safety of the assembly in which it is included and substitutions for the part are not permitted. The next character (#) is used to indicate that sample parts do not require an engineering parts approval (E-Approval). The third character (T) is used to indicate that tooling may be required to fabricate the part. The final special character (N) is used to indicate that a part is non-preferred. Some entries from the master parts file are shown in Fig. 1.

Creating a DL

A skeletal DL must be created before any groups can be created. Creation of a DL requires that a title, generic equipment designator, and drawing number be entered into the system. The title is intended to be used for a basic description of the assemblies on the DL. A generic equipment designator classifies the equipment and may be used as the root of a model number. The drawing number and the group, together, form a unique identifier for the assemblies to be defined.

Creating a group

On the skeletal DL, a column for quantity data must be reserved for each group to be created. To do this, a header for each group is entered. This header consists of a group status code, a group letter and number, the specific equipment designator and identification of the next higher assembly. Allowable group status codes are "signed off" (SO), "blackline" (BL), and "under development"(UD). Group letters, when suffixed to the generic equipment designator, identify a specific equipment. Again, the group number in conjunction with the drawing, uniquely identify the assembly. Figure 2 shows the coding of a data sheet required to create a skeletal DL with two groups.

Now that a skeletal DL exists with a reserved group, particular items are to be added to define the group. Items are added in a logical order, leaving some space for expansion at a later date. The definition of an item consists of an item number, a drawing-part number, and the quantity. The item number specifies a line within the body of the DL. Given a drawing-part number, the part description and characteristics are automatically extracted from the master parts file and printed on the DL. The quantity can be either a number (for example, 2), "as required" (AR) for oil-house items such as lubricants or inks, or "X" to specify a reference drawing.

Other fields exist within the item format where additional information may be entered. A special character field contains the identifiers (S, #, T, N) described above and extracted from the master parts file, plus an additional column (*) to define the insertion method if an item is to be automatically inserted. An asterisk (*) in this field can denote automatic insertion in general, while axial, radial, or hardware automatic insertion are indicated by "A," "D,"

TC	CHARACTERISTICS	DRWG NO	NAME	PROPERTY OF RCA
	BACHASSIS ASY	1459014	CTC111	

S - SAFETY CRITICAL
\# - NO E-FORM REQUIRED
* - MAY BE AUTO INSERTED
I - TOOLING MAY BE REQUIRED
N - NON-PREFERRED PART
R - SAFETY RELATED
I - SCHEMATIC SYMBOL INDICATOR
C - CIRCUIT GROUP INDICATOR

TC	SO	CI	GROUP	FIRST MADE FOR
	SO	A	501	CTC111A :CTR423
	UD	B	502	CTC111B :CTR439

TC	ITEM	DRAWING NO.	PART OF GROUP	S	#	*	I	N	DESCRIPTION NAME	DESCRIPTION CHARACTERISTICS	I	REFERENCE

Fig. 2. Portion of DL system input form showing data for skeletal DL. Assemblies 1459014-501 and 1459014-502 are to be defined. The remainder of the form is used for entry of a master parts file record or line items for the DL.

and "H" respectively. A notes field can be used for text to provide additional information. Part of this field may be used for the electrical component schematic reference designator (for example, R302). For assigning items to particular circuits, a circuit group indicator (a single letter) is used. This provides a method for grouping components, both mechanical and electrical, for functional circuit cost indications and other analyses. If the component may present a safety consideration because of the way it is used in the particular equipment, an "R" is entered to indicate that the part is considered to be safety-related. Safety-critical requirements supersede safety-related requirements.

Maintaining a DL

The above discussion concentrated on establishing an initial DL. Once the DL has been established, it may be

CTC-111 ASY CHASSIS : 1459014 : DL : PROPERTY OF RCA CORPORATION DO NOT REPRODUCE WITHOUT PERMISSION : DIST CODE : 102 : PAGE 1 OF 7 PAGES

S=SAFETY CRITICAL R=SAFETY RELATED
#=NO E-FORM REQUIRED C=CIRCUIT GROUP INDICATOR
*=MAY BE AUTO INSERTED
A=AXIAL,D=RADIAL,H=HDWE
I=TOOLING MAY BE REQD
N=NON-PREFERRED PART

SO A 501 CTR 423
SO B 502 CTR 439
SO C 503 CTR 424
SO D 504 CTR 424
SO E 505 CTR 444
SO F 506 CTR 426
SO H 507 CTR 423
SO J 508 CTR 423
UD K 509 CTR

ITEM	DRAWING	PT	S	#	*	I	N	DESCRIPTION	NOTES	C	R	UM	501	502	503	504	505	506	507	508	509
1	2830598-001							CHASSIS ASY	CTC-111A KEY/KEY SCAN				X								
2	2830598-002							CHASSIS ASY	CTC-111B REMOTE					X							
3	2830598-003							CHASSIS ASY	CTC-111C DUAL-DIM KEY						X						
4	2830598-004							CHASSIS ASY	CTC-111D DUAL-DIM REMOT							X					
5	2830598-005							CHASSIS ASY	CTC-111E HI-PERF AUD RE								X				
6	2830598-006							CHASSIS ASY	CTC-111F KEY/KEYSCN SGL									X			
7	2830598-007							CHASSIS ASY	CTC-111H REMOTE SGLTONE										X		
8	2830598-008							CHASSIS ASY	CTC-111J VIDEO IN/OUT S											X	
9	2830598-009							CHASSIS ASY	CTC-111K VIDEO IN/OUT A												X
10																					
11																					
12																					
13																					
14	1459011-501							BD ASY DL													
15																					
16	1459011-502							BD ASY DL													
17	1459011-507							CBM ASY DL													
18	1459011-508							CBM ASY DL													
19	1459011-509							CBM ASY DL													
20																					
21																					
22																					
23																					
24	1458774-502		#					MODULE ASY DL 455002 RA	PW2300													
25																					
26	1458775-502							AUDIO OUTPUT ASY D/L	PW2200												
27																					
28	2843128-501							DL VIDEO IN/OUT ASY													
29																					
30	2843128-502							DL VIDEO IN/OUT ASY													
31																					
32																					
33																					
34																					
35																					
36																					

DATE 04/22/81 : LATEST REVISION THIS PAGE IS 010 : DL : 1459014

Fig. 3. An example of one page of a DL document, with one revision sheet, produced using the Automated DL system. Note how different assemblies can call for different line items through the use of entries in the quantity fields.

modified to reflect changes in the design or to correct clerical errors. All fields except the DL drawing number and group numbers can be changed. Groups and items may be added to or deleted from the DL. By convention, all modifications to the body of the DL must be reflected in the revision history.

Data necessary to create an entry in the revision history are: revision number, Engineering Change Notice (ECN) number, text describing the change, and the names of the responsible individuals. If a change is being made as a result of an ECN, the ECN number is entered. The text is descriptive of the change and should facilitate the recreation of the earlier version of the DL. Figure 3 shows an example of a DL document, with a revision sheet, produced using the Automated DL System.

Retrieving DL data

The system capabilities for retrieval of information from the database are limited only by the extent of the data entered by the collective operational functions and whether or not the need is great enough to justify the programming effort. To demonstrate typical information available to the design engineer as a dynamic tool, we will take you through a hypothetical case that will select a component for use in a horizontal output transistor circuit. Not all of the available retrieval features are used in this example, but this sampling will show the power of the system. In general, the reports are available on CRT terminals or in a hard-copy form at an adjacent printer. A full-time data center operator is also available to retrieve a hard copy of the information.

Characteristics search

The schematic calls for the use of a 1/4W resistor of approximately 50 ohms. The engineer determines that a carbon-film flameproof type is needed to meet performance requirements. First, a complete listing of candidates is obtained by asking for a master parts file search by part name and characteristics. The parameters of the search are typed into the terminal in answer to the questions asked by the program. In this case the parameters are: description — RESISTOR CFFP and characteristics — 1/4 WATT, 5%,

```
-----------------------------------------------------------------------------------------------------------
                         :            :             :   RCA CONSUMER ELECTRONICS DRAWING LIST    :              PAGE  5 OF  7 PAGES
MASTER REVISION PAGE :  1459014   : DL             :                                            : DIST CODE : 102
-----------------------------------------------------------------------------------------------------------
PAGE NO.  01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

LST REV.  10 10 10 12 12 12 12
-----------------------------------------------------------------------------------------------------------
PAGE NO.  41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80

LST REV.
-----------------------------------------------------------------------------------------------------------
REMARKS: THOSE ITEMS CLASSIFIED *S* ARE SAFETY CRITICAL AND HAVE SPECIAL CHARACTERISTICS WHILE THOSE CLASSIFIED *R* ARE SAFETY
 RELATED AND ARE RESTRICTED BECAUSE OF APPLICATION. SUBSTITUTIONS FOR *S* AND/OR *R* SPECIFIED PARTS ARE PERMITTED ONLY BY SPECIAL
 WRITTEN DIRECTIVE ORIGINATED BY RCA DESIGN ENGINEERING AND/OR SAFETY ENGINEERING. THESE PARTS ARE IDENTIFIED BY SHADING ON THE
 SCHEMATIC.
-----------------------------------------------------------------------------------------------------------


-----------------------------------------------------------------------------------------------------------
SUB   1  ECN# 000000                                                  :
         G-503 THRU 505 ENTERED UNDER DEVELOPMENT.                    G-501 & 502 CHECKED AND ISSUED.
         "SIGNED OFF - 7/15/80"
         07/10/80    R ALTMNSHOFR    M ROBERTS       R SIZEMORE
         07/10/80
         JJK   CWR   WAL   PRK   RJD   SVS   PDG   MLS   DEC   JFB
                     XXX   XXX               XXX   XXX   XXX   XXX
-----------------------------------------------------------------------------------------------------------
SUB   2  ECN# 057516                                                  :
         ALL GROUPS: ITEM 73 DWG REF WAS 990157-13. ITEM 80 DWG REF   WAS 1464550-17. ADDED ITEM 108.
         "SIGNED OFF - 8/28/80"
         08/15/80    R ALTMNSHOFR    M ROBERTS       R SIZEMORE
         08/15/80
         JJK   CWR   WAL   PRK   RGD   SVS   PDG   MLS   DEC   JFB
         XXX   XXX   XXX   XXX   XXX         XXX   XXX   XXX   XXX
-----------------------------------------------------------------------------------------------------------
SUB   3  ECN# 000000                                                  :
         G-503 & 504 CHECKED AND ISSUED.                              "SIGNED OFF - 9/12/80"
         09/12/80    J KOPCZYNSKI    R DURE          R SIZEMORE
         09/12/80
         JTT   CWR   WAL   PRK   SVS   PDG   MLS   DEC   JFB   KLK
         XXX   XXX   XXX   XXX         XXX   XXX   XXX   XXX   XXX
-----------------------------------------------------------------------------------------------------------
SUB   4  ECN# 057715                                                  :
         ALL GROUPS: ADDED ITEM 120. DELETED REFERENCE TO ITEM 21 IN NOTES COLUMN OF ITEM 139. REVISED FIRST MADE FOR COLUMN.
         ADDED NOTES TO ITEMS 1 THRU 5. G-503 & 504: ITEM 140 QTY WAS2.
         G-505 CHECKED AND ISSUED.                                    "SIGNED OFF - 9/19/80"
         09/17/80    J KOPCZYNSKI    R DURE          R SIZEMORE
         09/17/80
         JTT   CWR   WAL   PRK   SVS   PDG   MLS   DEC   JFB   KLK
         XXX   XXX   XXX   XXX               XXX   XXX   XXX   XXX
-----------------------------------------------------------------------------------------------------------
SUB   5  ECN# 058176                                                  :
         ALL GROUPS, ITEM 115 REF WAS 99084-23.                       "SIGNED OFF - 12/19/80"
         12/15/80    J KOPCZYNSKI    L LEONHARDT     L REED
         12/15/80
         JTT   CWR   WAL   PRK   PDJ   MLS   DEC   JFB   KLK

-----------------------------------------------------------------------------------------------------------
                                          :                                           :                :
                              DATE 04/22/81:        LATEST REVISION THIS PAGE IS 012  : DL             :  1459014
-----------------------------------------------------------------------------------------------------------
```

Fig. 3. (continued). Revision sheet.

REPORT ID EDL920A DATE 01/06/81 PAGE 1

DRAWING & PART CHARACTERISTICS EXTRACT OPTION 6

DRAWING-PART	S	#	T	N	DESCR	CHARACTERISTICS		
993272-349					RES CFFP	1/4W	5%	10R
993272-353					RES CFFP	1/4W	5%	15R
993272-356					RES CFFP	1/4W	5%	20R
993272-357					RES CFFP	1/4W	5%	22R
993272-361					RES CFFP	1/4W	5%	33R
993272-365					RES CFFP	1/4W	5%	47R
993272-373					RES CFFP	1/4W	5%	100R
993272-380					RES CFFP	1/4W	5%	200R
993272-381					RES CFFP	1/4W	5%	220R
993272-391					RES CFFP	1/4W	5%	560R

E N D - O F - R E P O R T

Fig. 4. Drawing and Part Characteristics Extract Report. This example shows the results of a search for a ¼-watt carbon-film flame proof resistor in the range of 1 to 999 ohms. If the engineer knows a part description and/or characteristics, he can use this report to find drawing-part numbers.

CU	0	993272-365	EA	0705	2		RES CFFP1/4W	5%	5.28	51380
CU	T	993272-365	32 EA	0505	2		RES CFFP1/4W	5%	4.90	51380
CU	C	993272-365	EA	0705	2		RES CFFP1/4W	5%	6.62	61380
CU	J	993272-365	EA	0705	2		RES CFFP1/4W	5%	4.98	51380
8F	0	993272-365	EA	0705	2	I	RES CFFP1/4W	5%	5.28	51380
8F	T	993272-365	32 EA	0505	2	S	RES CFFP1/4W	5%	4.90	51380
8F	C	993272-365	EA	0705	2	I	RES CFFP1/4W	5%	6.62	61380
8F	J	993272-365	EA	0705	2	S	RES CFFP1/4W	5%	4.98	51380
81	0	993272-365	EA	0705	2	S	RES CFFP1/4W	5%	5.16	112180
81	T	993272-365	32 EA	0705	2	S	RES CFFP1/4W	5%	4.80	112180
81	C	993272-365	EA	0705	2	S	RES CFFP1/4W	5%	6.00	112180
81	J	993272-365	EA	0705	2	S	RES CFFP1/4W	5%	4.87	112180
80	0	993272-365	EA	0705	2	I	RES CFFP1/4W	5%	5.28	51380
80	T	993272-365	32 EA	0505	2	S	RES CFFP1/4W	5%	4.90	51380
80	C	993272-365	EA	0705	2	I	RES CFFP1/4W	5%	6.62	61380
80	J	993272-365	EA	0705	2	S	RES CFFP1/4W	5%	4.98	51380

Fig. 5. Standard Cost Report. The standard cost for the selected resistor (993272-365) for different cost periods and different plants is displayed in this report. For the current cost period 'CU' the standard cost of the resistor in domestic plants is $5.28 per 1000. The engineer may now compare the costs of various components.

AND RESISTANCE IN THE RANGE OF 1 TO 999 OHMS. Figure 4 shows the report from this search. This report represents option 6 of this program — search by description and characteristic range. Six other options allow the master parts file to be searched by other parameters such as special characters (S, #, T, N), description only, characteristics only, and combinations of these. The search criteria can be quite broad or very narrow.

After reviewing the list of candidate parts, the engineer decides that the 47-ohm resistor (part number 993272-365) most closely matches the desired criteria.

Part cost

The next information desired might be the part cost. By using the part-cost program and typing in the drawing and part number, the report shown in Fig. 5 is generated. The first column is the cost period. The second column indicates the plant location. The part number and its description are in the next two columns. The last two columns are the cost per 1000 parts and the date of the last update. From this information, the engineer can determine the cost applied at the plant of manufacture.

Vendor name

The engineer can then call up a program to determine the part status. Figure 6 shows this report wherein the vendor (or vendors, if multiple-sourced) name is given along with

REPORT ID EDL910A ENGINEERING WHERE-USED DATE 01/06/81 PAGE 1

DRAWING-PT. PART-DESCRIPTION

ASSY #-GRP.	DESC	E/S	QUANTITY	ITEM	SCHEM REF	MODEL
993272-365 RES CFFP1/4W 5% 47R						
CTC112-00M	HORIZONTAL OUTPUT CI	2	1.	4019	R444	
CTC131-00M	HORIZONTAL OUTPUT	2	1.	4019	R444	
CTC131-601	HOIZ XSTR ASSY	2	1.	19	R444	
1458748-501	CTC107A	1	1.	741	R532	CTC107A
1458748-502	CTC 107ADL	1	1.	741	R532	
1458748-505	CHASSIS	1	1.	741	R532	CTC108A
1458748-506	CHASSIS ASY DL	1	1.	741	R532	
1458748-507	CHASSIS ASY DL	1	1.	741	R532	
1458748-508	CHASSIS ASY DL	1	1.	741	R532	
1458748-509	CHASSIS	1	1.	741	R532	CTC109A
1458748-510	CHASSIS ASY	1	1.	741	R532	
1458748-602	CTC107A	2	1.	741	R532	
1458748-606	CTC108	2	1.	741	R532	
1458748-610	CTC109	2	1.	741	R532	
1458938-501	CHASSIS ASY	2	1.	502	R816	KCS207A
1458938-502	CHASSIS ASY	2	1.	502	R816	KCS207B
1458938-503	CHASSIS ASY	2	1.	502	R816	
1459015-501	CTC-107 D/L	1	1.	741	R532	
1459015-502	CTC107B	1	1.	741	R532	
1459015-505	CHASSIS ASY DL	1	1.	741	R532	
1459015-506	CHASSIS ASY DL	1	1.	741	R532	
1459015-507	CTC108F	1	1.	741	R532	
1459015-510	CHASSIS ASY DL	1	1.	741	R532	
1459015-511	CHASSIS ASY DL	1	1.	741	R532	CTC110B
1459015-V07	VERTICAL CIRCUIT	2	1.	741	R532	
1459015-V08	VERTICAL CIRCUIT	2	1.	741	R532	
1459015-V10	VERTICAL CIRCUIT	2	1.	741	R532	
2841295-501	HORIZ XSTR ASY DL	1	1.	19	R444	
2842251-501	CKE-108B KIT	1	1.	741	R532	
VERT108-107	13"17"19" COLOR	2	1.	741	R532	
VERT108-108	13"17"19" COLOR	2	1.	741	R532	

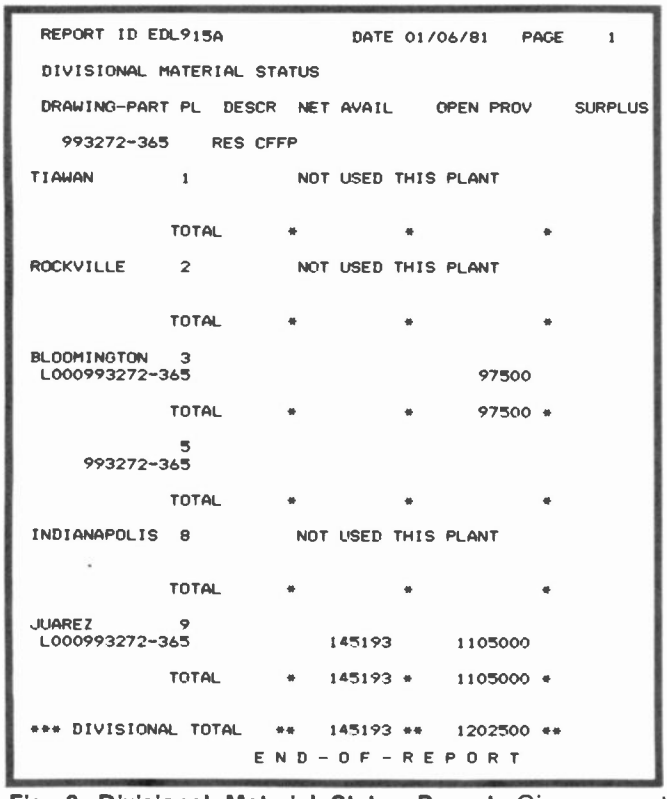
E N D - O F - R E P O R T

Fig. 7. Where Used Report. This report instance lists all other assemblies that use the resistor 993272-365. Knowing that model CTC107A (1458747-501) is currently in production, the engineer then knows the part of interest is in current use. For this model, the resistor's schematic reference designator is R532 and it is called for in item 741 on the 1458748 DL.

RPT ID EHE39 PART STATUS DATE: 010981 PAGE 1

DRAWING	PART SC	SUB	COMM	DESCRIPTION	E-FORM	PRI	DATE IN	DD	LAST ACTION	BL	BY	V/CODE	V/LOC	VENDOR NAME	WHERE-USED	P	M	S	L	XXXX
993272-365		0005		RES CFFP1/4W	5	109315	5/23/77	A	6/04/79	05	63	24965	GE	DRALORIC ELECTR						

Fig. 6. Engineering Approval Status Report. This report indicates that the part received an engineering approval on E-Form #109315. Also, the engineer can use this report to find the vendor's name, in this case, Draloric.



```
 REPORT ID EDL915A              DATE 01/06/81   PAGE     1

 DIVISIONAL MATERIAL STATUS

 DRAWING-PART PL  DESCR  NET AVAIL     OPEN PROV     SURPLUS

   993272-365     RES CFFP

TIAWAN          1          NOT USED THIS PLANT


                TOTAL      *          *             *

ROCKVILLE       2          NOT USED THIS PLANT


                TOTAL      *          *             *

BLOOMINGTON     3
 L000993272-365                              97500

                TOTAL      *          *       97500 *

                5
      993272-365

                TOTAL      *          *             *

INDIANAPOLIS    8          NOT USED THIS PLANT


                TOTAL      *          *             *

JUAREZ          9
 L000993272-365                 145193       1105000

                TOTAL      *   145193 *     1105000 *


*** DIVISIONAL TOTAL    **    145193 **    1202500 **
                    E N D - O F - R E P O R T
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Fig. 8. Divisional Material Status Report. Given a part number, this report is used to determine the quantity at each plant.

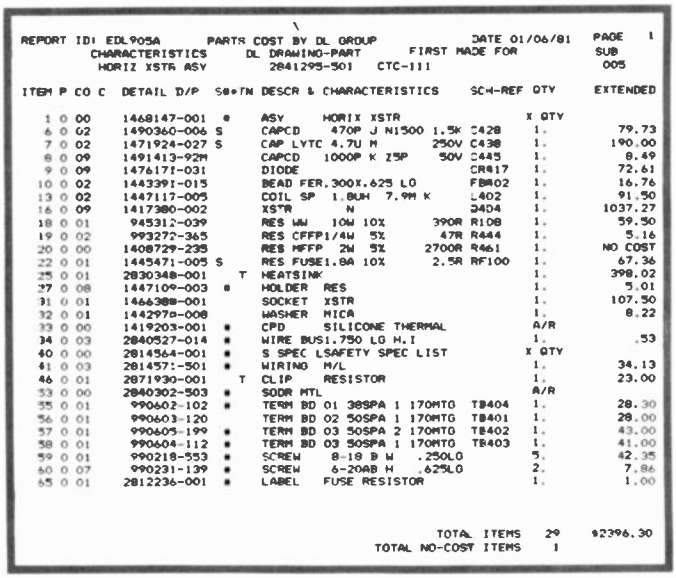
other information, including the status of engineering approvals (in this case, approved on E-Form 109315).

Where used

The next question might be: "Where was the part used before?" Figure 7 is the report resulting from a query to the always current "where-used" program. The report is self-explanatory, with the exception of the E/S column. The E/S column represents "engineering status" and is an indication of who entered the information into the database. A "1" indicates the data was entered by Design Engineering, based on an actual DL. A "2" indicates the data was entered by cost standards based on an inquiry for cost information. From the report, the design engineer can see that not only has this part been used extensively, but its future use is also contemplated as indicated by the first three and the last two entries for which no DL numbers have been assigned.

Division material status

To determine the Division-wide material status of this part, the Divisional material status program is called on oddly enough! The report shown in Fig. 8 results. This report shows the status at all plant locations and indicates where parts might be found for testing or sample builds. There are no parts in surplus, but 145193 are available in the Juarez plant and there are quite a few on open order.



```
REPORT ID: EDL905A      PARTS COST BY DL GROUP              DATE 01/06/81   PAGE   1
        CHARACTERISTICS       DL DRAWING-PART      FIRST MADE FOR            SUB
          HORIZ XSTR ASY        2841295-501   CTC-111                         005

ITEM P CO C  DETAIL D/P  S#FN DESCR & CHARACTERISTICS     SCH-REF  QTY     EXTENDED

   1 0 00    1468147-001  #    ASY     HORIX XSTR                    X QTY
   6 0 02    1490360-006  S    CAPCD    470P J N1500 1.5K C428      1.          79.73
   7 0 02    1471924-027  S    CAP LYTC 4.7U M       250V C438      1.         190.00
   8 0 09    1491413-92M       CAPCD   1000P K Z5P    50V C445      1.           8.49
   9 0 09    1476171-031       DIODE                         CR817  1.          72.61
  10 0 02    1443391-015       BEAD FER.300X.625 LG          FB802  1.          16.76
  13 0 02    1447117-005       COIL SP  1.8UH  7.9M K       L402   1.          91.50
  16 0 09    1417380-002       XSTR      N                   Q404   1.        1037.27
  18 0 01     945312-039       RES WW    10W 10%      390R R108   1.          59.50
  19 0 02     993272-365       RES CFFP1/4W  5%       47R R444   1.           5.16
  20 0 00    1408729-235       RES MFFP  2W  5%     2700R R461   1.         NO COST
  22 0 01    1445471-005  S    RES FUSE1.8A 10%       2.5R RF100  1.          67.36
  25 0 01    2830348-001    T  HEATSINK                           1.         398.02
  27 0 08    1447109-003  #    HOLDER  RES                        1.           5.01
  31 0 01    1466388-001       SOCKET  XSTR                      1.         107.50
  32 0 01    1442970-008       WASHER  MICA                      1.           8.22
  33 0 00    1419203-001  #    CPD     SILICONE THERMAL          A/R
  34 0 03    2840527-014  #    WIRE BUS1.750 LG H.I              1.           .53
  40 0 00    2814564-001  #    S SPEC LSAFETY SPEC LIST          X QTY
  41 0 03    2814571-501  #    WIRING  M/L                       1.          34.13
  46 0 01    2871930-001    T  CLIP    RESISTOR                 1.          23.00
  53 0 00    2840302-503  #    SODR MTL                          A/R
  55 0 01     990602-102  #    TERM BD 01 38SPA 1 170MTG  TB404  1.          28.30
  56 0 01     990603-120       TERM BD 02 50SPA 1 170MTG  TB401  1.          28.00
  57 0 01     990605-199  #    TERM BD 03 50SPA 2 170MTG  TB402  1.          43.00
  58 0 01     990604-112  #    TERM BD 03 50SPA 1 170MTG  TB403  1.          41.00
  59 0 01     990218-553  #    SCREW    8-18 P W   .250LG        5.          42.35
  60 0 07     990231-139  #    SCREW    6-20AB H   .625LG        2.           7.86
  65 0 01    2812236-001  #    LABEL   FUSE RESISTOR             1.           1.00

                                                  TOTAL ITEMS   29     $2396.30
                                              TOTAL NO-COST ITEMS    1
```

Fig. 9. Parts Cost By DL Group Report. The cost of individual parts and the cost of the assembly can be determined by using this report. The part selected (item 19) has a cost of $5.16 per 1000, and the total assembly costs $2,396.30 per 1000.

Assembly cost

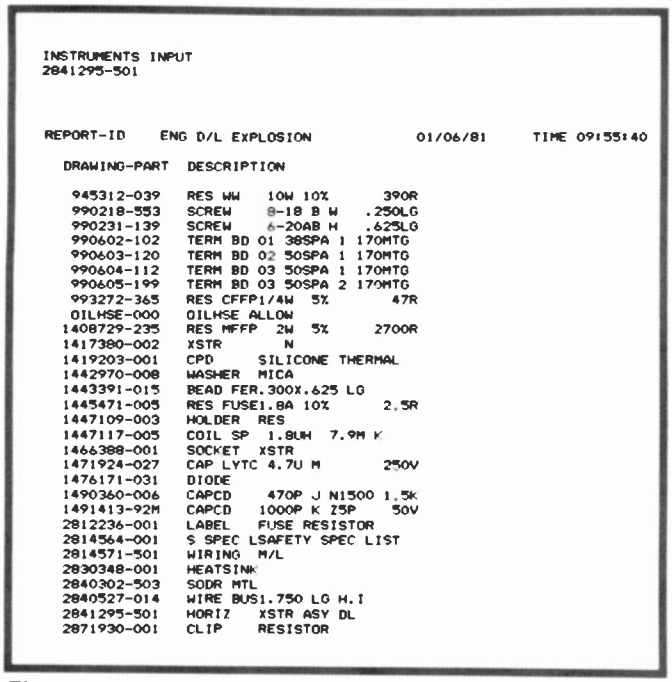
Having chosen a part, verified a reasonable part cost, determined that there is an engineering-approved source, found that there is sufficient usage of this part to qualify it as a "standard" part, and located parts from which to draw a small quantity for development use, the engineer is ready to include the part in the assembly. The next question might be: "What is the total parts cost of this assembly?" Figure 9 is a listing of the entire DL group with the associated material costs and a total. There is one item for which a cost has not been developed, but the total plus an educated guess on that part yields a very close approximation of the assembly parts costs. In addition to the "Parts Cost By DL Group" shown, this program has options to list parts costs in drawing-part number sequence or by DL circuit group indicator, thereby providing costs by circuit function. The option also exists to report costs reflected by the plant of manufacture. Another feature of this program is a summary of assembly part costs broken down by the part's country-of-origin.

DL explosion

The next step might be ordering parts for the complete assembly for a sample build to prove out the design. The DL explosion, shown in Fig. 10, provides a complete listing in drawing-part number sequence as a handy shopping list that also assures that all parts are ordered.

Chassis component analysis

Finally, the assembly can be reviewed in an analysis of component count and method of insertion into the circuit



INSTRUMENTS INPUT
2841295-501

REPORT-ID ENG D/L EXPLOSION 01/06/81 TIME 09:55:40

DRAWING-PART	DESCRIPTION
945312-039	RES WW 10W 10% 390R
990218-553	SCREW 8-18 B W .250LG
990231-139	SCREW 6-20AB H .625LG
990602-102	TERM BD 01 38SPA 1 170MTG
990603-120	TERM BD 02 50SPA 1 170MTG
990604-112	TERM BD 03 50SPA 1 170MTG
990605-199	TERM BD 03 50SPA 2 170MTG
993272-365	RES CFFP1/4W 5% 47R
OILHSE-000	OILHSE ALLOW
1408729-235	RES MFFP 2W 5% 2700R
1417380-002	XSTR N
1419203-001	CPD SILICONE THERMAL
1442970-008	WASHER MICA
1443391-015	BEAD FER.300X.625 LG
1445471-005	RES FUSE1.8A 10% 2.5R
1447109-003	HOLDER RES
1447117-005	COIL SP 1.8UH 7.9M K
1466388-001	SOCKET XSTR
1471924-027	CAP LYTC 4.7U M 250V
1476171-031	DIODE
1490360-006	CAPCD 470P J N1500 1.5K
1491413-92M	CAPCD 1000P K Z5P 50V
2812236-001	LABEL FUSE RESISTOR
2814564-001	S SPEC LSAFETY SPEC LIST
2814571-501	WIRING M/L
2830348-001	HEATSINK
2840302-503	SODR MTL
2840527-014	WIRE BUS1.750 LG H.I
2841295-501	HORIZ XSTR ASY DL
2871930-001	CLIP RESISTOR

Fig. 10. DL Explosion Report. A complete list of parts, in numerical order, for the assembly 2841295-501 is shown here. This report will also include the parts from the sub-assemblies called for in the assembly DL.

board (ACI = Automatic Component Insertion). Figure 11 represents the report output by this program. The example shown is not that of our horizontal output transistor assembly but a more representative analysis of a complete circuit board assembly for a color-television instrument. This illustrative case shows some of the wealth of information available to the design engineer when the engineering

REPORT ID: EDL945 REPORT NAME:CHASSIS COMPONENT ANALYSIS DATE 1/06/81

D/L DWG & PT 1459011-501 CHASSIS DESIGNATION 001459011501

ELECTRICAL	QTY	MECHANICAL	QTY
TOTAL COMPONENTS	582	ACI D JUMPERS	85
ACI D COMPONENTS EXCL JUMPERS	329	MANUAL INSERTED JUMPERS	1
MANUAL INSERTED COMPONENTS	253	STAKES	
TRANSISTORS	31	BEAD CHAIN TERMINALS	
IC S	7	EYELET	13
DIODES	4	GRIPLETS	
COILS/TUNABLE	12	TERMINAL STRIPS	
COILS/TRANS (SMALL/FIXED)	28	FERRITE BEADS ACI D	3
TRANSFORMERS	2	FERRITE BEADS MANUAL INSERTED	9
VARIABLE RESISTOR	17		
MINILYTICS	51		
CAPS POLYESTER	26		
OTHER CAPS	54		
RESISTORS	14		
OTHERS	7		

Fig. 11. Chassis Component Analysis Report. This report analyzes the components (electrical and mechanical) used in a television chassis. In this example, the chassis is one used in the ColorTrak instruments.

input of the assembly DL is combined with the input of all of the other groups into one comprehensive database.

Future

The Automated Drawing List System, as described, is being used daily to maintain DLs. As the design engineers learn more about how the system may help them to do a better job, they are using it more frequently. As a result of using the information from the system, the engineers are thinking of additional reports they would like to see. Also, plans for modernization of the Engineering and Drafting functions affect future plans for the Automated DL System.

Several enhancements to the current system are planned for the coming year. A majority of the data for the revision history can be extracted from the transactions necessary to maintain the DL. This data can then be automatically formatted and entered into the revision history, providing several benefits. Changes to the body of the DL would be accurately reflected. The Drafting checker could more easily determine that the intended changes had been made.

Currently, the part names and the characteristic formats are documented in a manual. Because it is left to individuals, entries in these fields are not always consistent. As can be seen from this discussion of information retrieval, conventions must be followed in order that all relevant information can be extracted. Instead of relying on the individual, Consumer Electronics plans for the computer to perform a check on the validity of the information entered.

Due to the limited size of the characteristics field (18 characters), very little information concerning the part, outside of gross characteristics, can be entered into the system. Consumer Electronics plans to expand this field to better support engineering decisions. By having characteristics, such as reliability, de-rating factors, and operating temperature ranges available, the engineer could more easily select the best part for the application, and be able to consider the effect of the part on the remainder of the assembly. This data could be valuable for constructing simulation models.

Because the information from the DLs is available in a central location in a consistent format, additional analysis of the data can be performed to support the design engineer. For example, the Chassis Component Analysis Report (Fig. 11) is to be expanded to include a table showing — for each type of electrical component — the quantity to be inserted by each insertion method. Currently, material cost is the primary factor considered when making a decision as to which part should be used, although the labor cost is intuitively considered. By making both material and labor costs available during the design process, a more cost-effective design can be made.

As other automated systems are introduced into Engineering and Drafting, it will become necessary for the Automated DL System to be integrated. A system which

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Bill Roberts is a member of the engineering staff in the New Products Laboratory at Consumer Electronics. He is currently assigned to Advanced Computer-Aided Mechanical Design. Joining RCA in 1950 in the CE Audio Products Group, he was involved with radios and phonographs as draftsman, engineer, group leader and manager. In 1971, he was assigned to the CE Consumer VTR Design Group and became the Mechanical Design Group Leader. He has also been involved with color TV chassis design.

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New Products Laboratory
Consumer Electronics Division
Indianapolis, Ind.
TACNET: 422-6823

Authors Bob Monat (standing) and Bill Roberts (seated).

would assign drawing numbers could also be used to gather enough information to create the master parts file record for the new drawing. Tieing the DL System into material ordering and project tracking systems could expedite the design process by allowing more time for engineering.

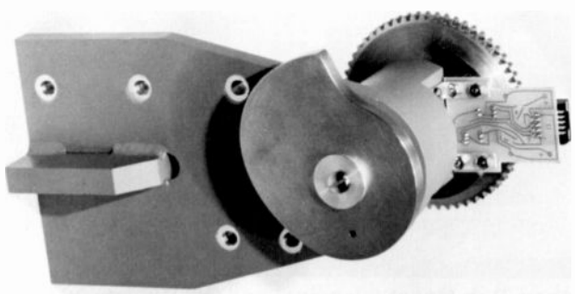
Conclusions

The Consumer Electronics Division's Automated Drawing List System, as implemented, has started to provide benefits to the Division. Design Engineering is at the point where the cost of entering the data into the computerized system is being overtaken by the benefits realized by the design engineers and the engineering managers. The departments which consume DL data agree that they receive accurate and timely data. As usage increases, ideas for better use of the information are generated. Development of the system has caused all users to take a fresh look at what they have been doing with DLs. Other design and manufacturing divisions could realize some of the same benefits if similar systems were implemented.

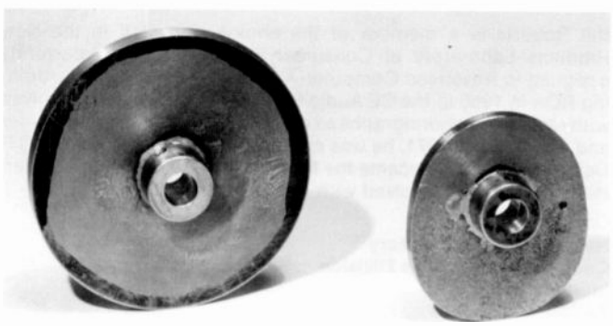
K.S. Reid-Green|W.Z. Marder

Numerically controlled machining of cams

Researchers are using computer-aided manufacturing (CAM) to make old-fashioned cams the "new-fashioned" way.



Lifting cam mounted in subassembly. This cam provides a coarse lifting motion via a cycloidal section and a fine adjustment via a constant velocity section.



Cams are made from "cam blanks." A guide hole is drilled one inch from the center of a circular cam blank. The cam blank is then fastened to the bed of the milling machine by bolting it through the hub. A pin through the guide hole assures that the cam is stationary and held in the required orientation while it is being profiled.

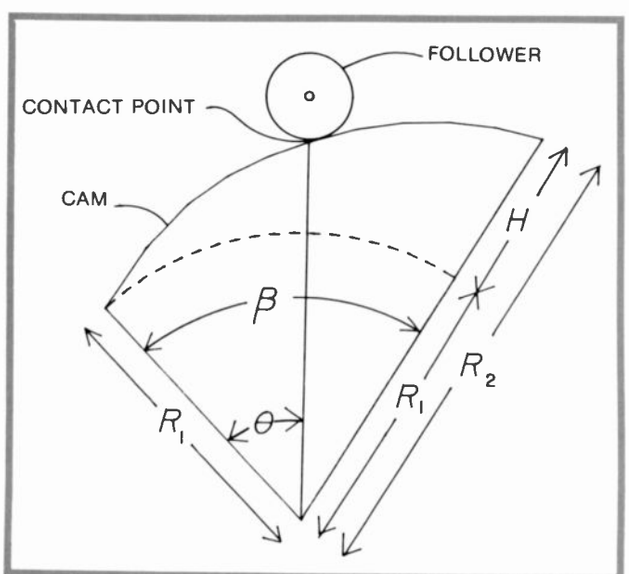


Fig. 1. A cam is composed of two or more profile sections. Each section can be described as a function of the angle of the section β; the change in radius H between the initial radius R_1 and final radius R_2; and the angle Θ, the current position of the cam follower.

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Abstract: *Using inexpensive Tektronix computing equipment, the authors attacked two principal problems in cam production. They reduced the possibilities for human error and controlled the tolerance between the true cam and its polygonal approximation.*

Probably the best-known application of cams is found in the internal combustion engine. Intake and exhaust valves are opened by cams that rotate around a shaft driven by gears connecting it to the crankshaft. The opening and closing of the valves is thus controlled precisely in synchrony with the combustion cycle.

Valve-lifting cams have a profile similar to a cross-section through an egg and are relatively simple, being symmetrical about one axis. More complex cams may have regions that impose various linear motions — including a constant velocity, a constant acceleration, or no motion — on the cam follower. It is obvious that a rotating circular "cam" would impart no motion to a cam follower: During the time a circular section passes under it, the follower "dwells", that is, the follower lift Y equals zero. The equation for a constant velocity cam section is $Y = H\theta/\beta$, where H is the total lift over the angle β, β is the angle of the cam section, and θ is the current cam angle (Fig. 1).

It is assumed that the cam is rotating at a constant

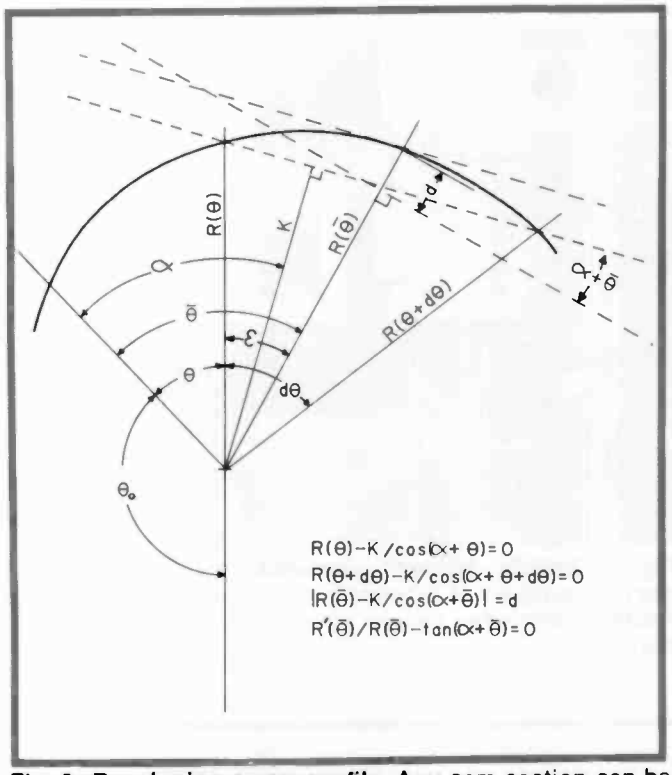


Fig. 2. Developing a cam profile. Any cam section can be described in terms of four equations with four unknowns. Since a numerical milling machine cuts straight lines, the purpose of the method is to control the error *d* between the true profile and its linear approximation.

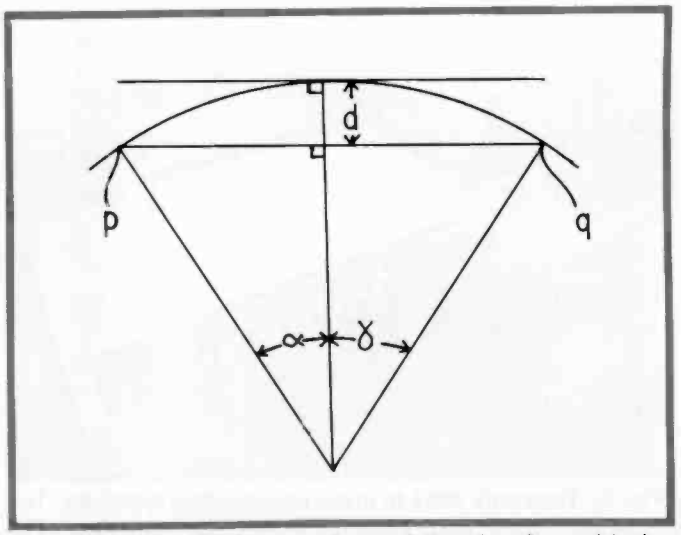


Fig. 3. Finding the intersections of the chord *pq* with the cam profile. Two iterative processes are used. First, beginning at *p*, the angle α must be found at which *d* is the required value. Second, the point *q* at which the chord crosses the profile is found, by guessing that γ equals α and iterating as necessary.

velocity and that the line passing through the center of rotation of the cam and through the center of the follower also passes through the contact point. (It doesn't, except in the case of dwell sections, but the error introduced is trivial enough to be ignored.)

Other useful profile equations are:

CYCLOIDAL: $$Y = H\left(\frac{\theta}{\beta} - \frac{1}{2\pi}\sin 2\pi\frac{\theta}{\beta}\right)$$

smooth transition from dwell to motion

PARABOLIC: $$Y = 2H\left(\frac{\theta}{\beta}\right)^2 \text{ while } \frac{\theta}{\beta} < 0.5$$

constant acceleration

$$Y = H - 2H\left(1 - \frac{\theta}{\beta}\right)^2 \text{ while } \frac{\theta}{\beta} \geq 0.5$$

constant acceleration in the opposite direction

HARMONIC: $$Y = \frac{H}{2}\left(1 - \cos\frac{\pi\theta}{\beta}\right)$$

sinusoidal follower motion

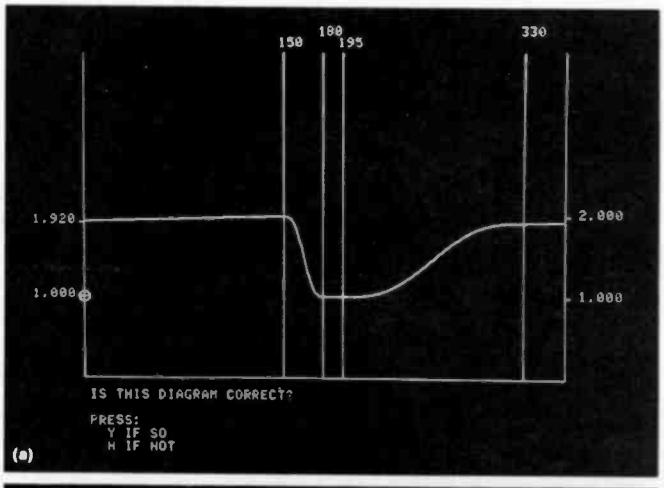
Cams are useful mechanical components, but in practice it is difficult for the engineer to communicate the need for a particular cam in terms useful to the machinist — the usual engineering drawing is not very valuable in this case. In the past, a widely used method required an accurate, full-scale drawing which the machinist would inscribe on a piece of stock. The machinist would then cut off as much material as possible and file the cam until it was reduced to the inscribed profile. Another method, using numerically controlled milling machinery, required the engineer to compute points on the profile at regular, close intervals, thus providing a polygonal approximation to the true cam. The opportunity for error in this technique is enormous unless the responsibility for computation and subsequent conversion to milling machine language can be taken away from the engineer and mill operator. Furthermore, regular angular increments around the cam do not provide for a constant error between the true profile and the polygonal approximation except on the circular or dwell sections of the cam.

Considering the availability of inexpensive computing equipment, we attacked the two principal problems existing in the usual cam production method — to reduce the possibilities for human error and to control the tolerance between the true cam and its polygonal approximation. We found that any well-defined trigonometric profile can be described in terms of four equations in four unknowns (Fig. 2).

It was necessary to use these equations to find the set of points describing the cam so that the maximum distance *d* between the true cam and the series of straight lines to be cut by the numerical mill was a constant. A good value for *d* is the tolerance of the milling machine.

To establish each straight-line cut, the mean-value theorem was applied. This theorem states that the difference between a chord and an arc is at its maximum where the chord is parallel to a line tangent to the arc.

Fig. 4. Tektronix 4052 to make engineering drawings. The engineer uses this equipment to design cams. The engineering drawing produced on the 4663 plotter is sent to the milling machine.



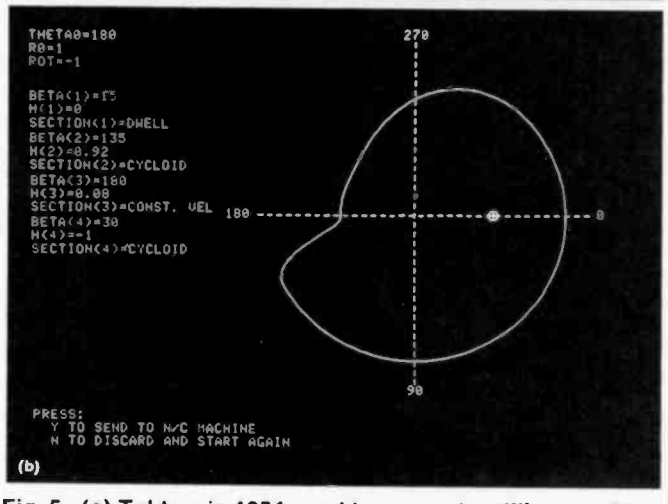


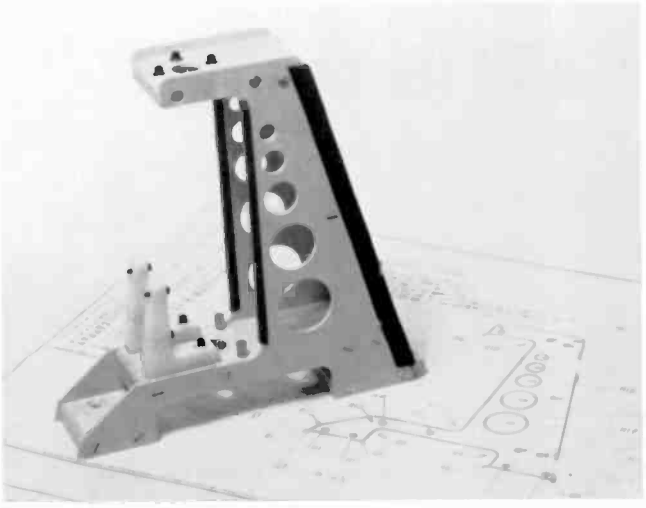
Fig. 5. (a) Tektronix 4051 used to generate milling machine program. The milling machine operator enters a short list of numbers from the engineering drawing to describe the cam. Displayed on the screen is a cam profile which will be identical to the engineering drawing unless an input error has occurred. **(b)** After the milling machine operator accepts the cam follower diagram, the 4051 displays the outline of the cam to be cut, thus affording the operator another opportunity to correct mistakes.

Fig. 6. Spindle Wizard™ numerical mill. The milling machine program is automatically loaded into the milling machine controller (shown at right) from the Tektronix 4051.

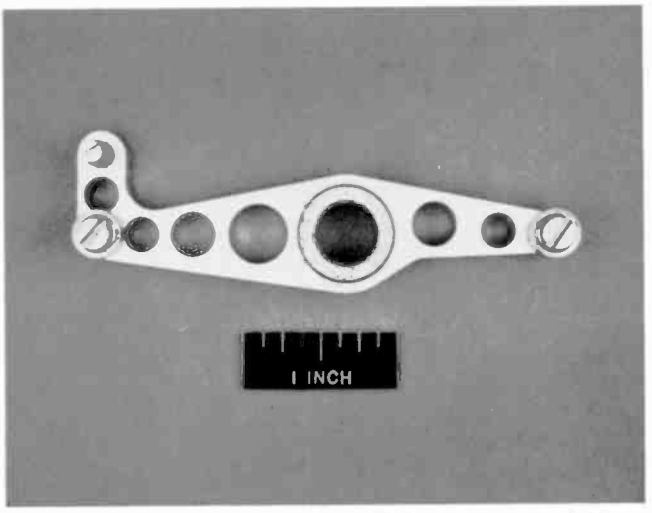
Beginning from a point p on the profile (Fig. 3), a bisection algorithm to find d was applied until d was determined to be between 95 percent and 100 percent of the established tolerance of the mill, in this case 0.0005 inches. Thus, the angle α was established. Next, it was necessary to find q, the point at which the other end of the chord passed through the arc. In circular sections this is a trivial task, because $\delta = \alpha$. We found that $\delta = \alpha$ is a very good first approximation for the non-circular sections, frequently requiring no iterative improvement. We also found that the old-fashioned one-degree increment was considerably closer than necessary — a typical cam can be approximated by an irregular polygon of about 75 sides and retain 0.0005-inch accuracy.

The equipment used in the cam profiler system consists of a Tektronix 4052 intelligent terminal (Fig. 4) with a 4663 plotter to produce the engineering drawing and to verify that the input describes the required cam, a Tektronix 4051 (Fig. 5) to convert the cam description to milling machine language, and a Spindle Wizard™ numerical mill (Fig. 6). The 4051 and 4052 are somewhat redundant, allowing for concurrent development of new parts by the engineer (the system is also used to generate flat parts), with production by the mill operator. If one of the terminals should fail, the system can still be used, because the development and production functions can be done by the same machine, albeit at reduced efficiency.

Use of this system has reduced the time needed to develop a new cam about eightfold. By traditional methods, there was about a four-day cycle from inception through engineering drawing to completion. The current cycle is about four hours, making even one-of-a-kind cams economical to produce.



Flat part shown in subassembly with computer-generated mechanical drawing. Note parameter list at left of drawing.



Milling-machine accuracy is sufficient to generate very small parts.

A similar program produces flat parts

Cams make up a small percentage of the parts made by the intelligent terminal/milling machine. Another program generates milling-machine language to cut flat parts that can be defined in terms of a profile made up of alternating circular arcs and lines tangent to arcs at both ends of the line. The case in which two lines intersect can usually be described acceptably as being joined by an arc of 0.001" radius. A wide variety of parts can be defined in the above terms, including Geneva mechanisms, linkages, brackets, and so on.

All that is necessary to describe such a part is the radius and center of each arc, and whether the mill cuts around the outside or inside of the arc. If the radius is entered as a negative number, the mill is instructed to cut inside the arc. Arcs are described beginning anywhere on the part and proceeding in a counterclockwise direction. The computer constructs the required tangent lines after verifying that none of the described circles overlap.

As in the cam program, the engineering drawing is drawn automatically and sent to the milling machine, together with a list of values for the operator to enter. The drawing is replicated at the milling machine so that the operator may verify the accuracy of his input before cutting the part.

Authors Keith Reid-Green (left) and Bill Marder (right).

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L.M. Rosenberg

Glossary of CAD programs and terms

The growing complexity of integrated circuits has increased the importance of CAD (Computer-Aided Design) software tools to assist RCA engineers in the design, manufacture and test of these electronic devices. Therefore, not only has the use of existing CAD tools grown significantly in the last few years, but many new ones have been developed to support special requirements. This has produced a proliferation of new program acronyms, CAD terms, and equipment names. We at RCA have added to this vocabulary, our own CAD terms and equipment names, some of which are, of course, unique to specific RCA locations.

In order to aid those unfamiliar with these terms, this glossary of CAD terms has been compiled. Although originally developed for the Solid State Division, it has been generalized to make it useful to all divisions of RCA using Design Automation software.

As new programs and systems are being added continually, and new designers will be using those and existing ones, the author intends to update this glossary periodically. Therefore, suggestions and comments are invited.

AFTER (Automatic Functional Test Encoding Routine) Program which automatically translates the output of a logic simulation program (e.g., TESTGEN or MIMIC) or a manually generated high-level description of functional tests to the specific format required to control an automatic IC test set such as Datatron, Teradyne or Sentry.

AGS (Applicon Graphic Systems) See Applicon.

APAR (Automatic Placement and Routing Program) A layout program which automatically "places" (positions) standard cells into regular rows then "routes" (wires) these cells between the rows. ATL/GSD developed three generations of APAR: PRF, PR2D and MP2D (please see these terms).

APPLICON Vendor supplied interactive graphics system for generation and editing of IC mask artwork. RCA has both 870 (second generation) systems and an 860 (third generation) system.

ART (ARTwork System) Unified system of IC artwork processing programs including CRITIC, MAP, SURVEY, SIFT, ROMGEN, CHECKPLOT, UNION, WEAVE, MODIFY, etc.

AUA (Automatic Universal Array) A program, similar to APAR, which automatically places and routes a universal array. (Available in late 1981.)

AUTOFILL A procedure which automatically generates the guardbands and P-well artwork for a CMOS design.

AUTOROM Program which automatically generates a mask-making tape and a test tape for a mask programmable ROM, given only the name of the binary data file, the variant number and the ROM type. It automatically generates the variant number artwork to be inserted on the mask; runs ROMGEN, SIFT and ROMTEST.

BANNING Name of NSA contract to GSD/ATL to develop the original APAR program. Sometimes used to describe the program and sometimes used to describe the APAR artwork format.

BATCH RCA colloquial term usually used to describe the submitting of a DFL file to MAP and/or MASK for the generation of a pattern generator tape. Sometimes used to describe the submittal of any program to the "background" computer mode.

CALCOMP Flatbed multi-pen checkplotter.

CALMA Vendor supplied interactive graphics system for generation and editing of IC mask artwork. At this writing, two GDS-II systems (each with four, color graphics terminals) are in SSD/Design Automation.

Checkplot A drawing generated by a computer-controlled "checkplotter" displaying IC mask artwork in outline or shaded format. It is used to visually verify correctness. Also refers to the CAD Program which translates DFL (please see) into checkplotter format.

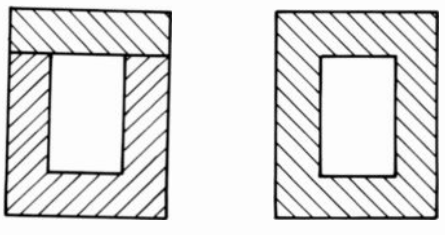
CMS (Conversational Monitoring System) IBM's time-sharing system that runs in Cherry Hill under the VM operating system.

ComputerVision Vendor supplied interactive graphics system for generation and editing of IC and PCB art work.

Control File Data in a computer file which can control a CAD Program or an automatic machine such as a mask making machine. For example, a CRITIC Control File contains the design rules to be verified by CRITIC in an English like language.

CRITIC (Computer Recognition of Illegal Technology in Integrated Circuits) Design Rule Checking (DRC) Program that reports minimum tolerance violations (width, spacing, enclosure), and illegal topology relations (overlap, abutt, cross, contain, disjoint) in integrated circuit mask artwork.

CUT Program which slices artwork with multiple connected regions ("holes and exteriors") such as bagel-shaped figure into abutting simply connected regions.



DAFTER (DATATRON AFTER) Similar to AFTER but only supports the Datatron tester and only runs on Design Automation's PDP-11 minicomputer.

DEFORMAT Converts pattern generator tapes such as D.W. Mann, Electromask and MEBES (see MAP), to DFL for verification purposes (e.g., checkplotting).

DEGEN ("Degenerate") Predecessor of DEFORMAT. Some groups incorrectly refer to DEFORMAT as DEGEN.

DFL (Design File Language) RCA's official universal mask artwork representation (format). Designed to be efficient for computer programs (see PLOTS).

DPS (Digitizer Plotter Systems) Interactive Graphics System developed by DA ten years ago. Obsoleted by Applicon and Calma.

FLOSS (Finished Layout Starting from Sketch) An experimental program that compacts a loose design layout (sketch) or chip plan while obeying specified design rules.

FRAGMENT Slices a polygon with numerous sides into a number of abutting polygons, each containing less than a user-specified number of sides. Used to satisfy maximum limits of some systems (such as Applicon or Calma) or to increase the efficiency of processing them.

GUA (Gate Universal Array) See Universal Array.

GDS-II (Graphics Display System—Version II) Latest Calma Model (see Calma).

LOGSIM) Similar to the MIMIC logic simulator but much older, with fewer capabilities. Essentially obsoleted by MIMIC.

MAP (Master Artwork/program) Pattern generator (PG) program which translates from DFL format to one capable of driving reticle- and mask-making equipment such as D.W. Mann 3000, Electromask 2500 Pattern Generators, and ETEC MEBES (Manufacturing Electron Beam Exposure System).

MASK Unified CAD System to generate a magnetic tape containing that data required to create a mask (step-and-repeat array of chip artwork on glass). This program obtains all possible standard data from a Technology File (please see), prompts the designer for the remaining required information (such as chip size), and then runs the MAP, SANDRA, DEFORMAT and VERSATEC Programs (please see these) to generate the mask making tape and a deformatted checkplot tape.

MIMIC (Module Imitating Modern Integrated Circuits) An interactive logic simulation program which accepts hierarchical network descriptions on a gate level (AND, OR, NOR, bilateral transmission gate, F/F, DFF, SRFF), delay information (versus fanout or capacitance) and digital signal inputs and predicts digital circuit response (logical one's and zero's).

MOSFIT (MOS FITting Program) A program which calculates the best R-CAP MOS model parameters to "fit" a set of MOS current vs. voltage measurements.

MP2D (Multiport, Two Dimensional) Third generation APAR program similar to PR2D (please see) except that it uses "multiport" cells (pins on top and bottom of each cell) for higher density (improved routing).

PLOTS RCA's mask artwork representation designed to be easy to read and write by a human. It has a one-to-one conformity to DFL.

PRF (Placement Routing and Folding) First generation APAR program which automatically "places" standard cells in a single row, "routes" these cells and then "folds" the row serpentine-like into a square region. This 15-year old program is now obsolete.

PR2D (Placement and Routing in Two-Dimensions) Second generation APAR program automatically "places" standard cells into a two-dimensional array and then automatically wires them. Cells have pins on one side only and, therefore, may be placed back-to-back. Essentially obsolete now.

R-CAP (RCA Circuit Analysis Program) An interactive circuit simulation program that accepts circuit descriptions on a component level (resistors, capacitors, inductors, diodes, bipolar transistors, MOS transistors), and predicts electrical circuit response (voltage and/or current vs. time waveforms; and amplitude and/or phase vs. frequency).

ROMGEN (ROM Generation) Program which translates a file containing ROM binary data (series of one's and zero's) into the DFL artwork required to manufacture a mask programmable ROM. See also ROMTEST and AUTOROM.

ROMTEST Program which translates a file containing ROM binary data (series of one's and zero's) into a functional test program for that ROM. Supports Macrodata 104, PW Mustang, Teradyne J283 and Sentry.

SANDRA (Step-AND-Repeat Array) This program generates the proper chip location information for a mask array. It handles dropouts for test inserts, the test inserts, the ALIS (Arm's Length Identification System) number generation and mask-labeling information.

SIFT Performs utility operations on mask artwork such as "explicitizing" (macro expansion), level changes, level extraction, windowing, conversion from Plots to DFL and back, conversion from disk to magnetic tape, and so on.

SMART (Selective Modification of Artwork Regions and Topologies) Performs Boolean operations on mask artwork such as logical AND (intersection) and OR (union). These may be useful prior to using CRITIC. Able to oversize and undersize artwork ("BIASING") to compensate for dimensional changes in mask making and processing. Automatically modifies artwork or, in some cases, generates new mask levels from existing ones.

SURVEY Summarizes the contents and size of an artwork file and reports errors or potential problems of a general nature that may cause problems in subsequent processing (such as self-crossing polygons and empty definitions).

TDAS (Test Data Analysis System) Collects, compresses, stores, analyzes and displays production electrical test data. Reports include histograms, long term trends, wafer maps and tabular displays. Installed on seven different processing lines in three manufacturing locations.

Technology File Computer file read by the MASK Program which contains all standard information for a specified technology (mask levels, tones, geometries, wafer, and MASK size, etc.). This minimizes work and chance of specifications errors.

TESTGEN Performs logic simulation (see MIMIC) displaying stable-state results (not detailed timing information) and performs worst-case hazard analysis. It also performs fault simulation that analyzes fault coverage by reporting undetected stuck-at-ONE and stuck-at-zero nets. It can perform limited automatic test generation.

TSO (Time Sharing Option) IBM's time sharing system that runs in Somerville under VS (see VS).

Universal Array Quick-turnaround custom IC design technique. All but one mask level is predefined. The metal level customizes the design. Predefined metal artwork "cells" can create desired logic building blocks (NANDS, Counter stager, etc.). Sometimes called master-slice outside of RCA.

VERSATEC High speed electrostatic checkplotter. Available in various widths from 12 inches to 72 inches. SSD has 36- and a 72-inch version. Capable of generating a six-foot square shaded checkplot in less than 10 minutes. Also refers to software which generates the magnetic control tape from a DFL file.

VM (Virtual Machine Operating System) IBM's operating system allows "virtual computers" to simultaneously and transparently run on one real machine. Each virtual computer appears to own all the hardware, from the user's point of view. Each virtual computer may run under VS or any other IBM operating sytem. Required in order to run CMS.

VS (Virtual System Operating System) Name of IBM's standard operating system (OS) that runs on a virtual memory machine such as the 370/168 in Somerville.

WEAVE A program which combines two DFL mask artwork files which contain some identical definition numbers. The artwork in each definition number from each file is merged together into a single file.

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Patents

Americom

Levin, H.L.
Antenna deicing apparatus—4259671

Commercial Communications Systems

Boyd, W.M.
Exciter having incidental phase correction compensation in consonance with output power level—4249214

Ferrie, R.G.
Systems for comparing and ranking a plurality of signal inputs—4255740

Lucchi, G.A.|Aires, R.H.
Aircraft weather radar system—4249174

Wright, D.I.
Video signal dropout compensator—4250521

Consumer Electronics

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Television horizontal AFPC with phase detector driven at twice the horizontal frequency—4251833

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Knight, P.R.
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Regulated deflection circuit—4251756

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Knop, K.|Kane, J.
Tunable diffractive subtractive filter—4251137

Knop, K.
Diffractive color filter—4255019

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Molinari, T.E.
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Robbi, A.D.
Digital drive circuit for electric motor or the like—4249119

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Laser rounding a Shapp semiconductor projection—4249960

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Regulated deflection circuit—4254366

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Williams, R.
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Adjustable passband filter—4250475

Patent Operations

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Continuous tuning arrangement for a multiband television receiver—4249256

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Rodgers, R.L., 3rd
Television synchronizing system operable from nonstandard signals—4253116

Schade, O.H., Jr.
Multi-mode relaxation oscillator—4250464

Schade, O.H., Jr.
Smoke detector—4250500

Steckler, S.A.|Balaban, A.R.
Television horizontal AFPC with phase detector driven at twice the horizontal frequency—4250525

Wheatley, C.F., Jr.
Balanced-to-single-ended signal converters—4254381

Wilson, W.|Egenski, F.J.
Free hold down of wafers for material removal—4258508

Witte, W.R.
Method of making transformer—4258467

Wittlinger, H.A.
Battery test system, as for smoke detector alarm—4251811

Yorkanis, B.J.
Inhibit circuit for a differential amplifier—4257009

Pen and Podium

Recent RCA technical papers and presentations

To obtain copies of papers, check your library or contact the author or his divisional Technical Publications Administrator (listed on back cover) for a reprint.

Astro-Electronics

J. Frohbieter
RCA Satcom Test Planning—6th Aerospace Testing Seminar, Los Angeles, Calif. (3/11-13/81)

C. Hubert
Spacecraft Attitude Acquisition from an Arbitrary Spinning or Tumbling State—*Guidance and Control Journal* (3-4/81)

A. Rosenberg|D. Hogan
Simultaneous Lidar Measurements of Temperature and Humidity Profiles: Error Analysis—Univ. of Jerusalem and Nuclear Research Center, Beer-Sheva, Israel (3/7/81)

Automated Systems

J.W. Betz
Undersea Surveillance—Eta Kappa Nu Honorary Society, Rensselaers Polytechnic Institute, Troy, N.Y. (3/81)

R.C. Guyer
The GVS-5: A Versatile Handheld Laser Rangefinder for Tactical Use—ASME Student Chapter, Northeastern Univ., Boston, Mass. (5/81)

R.E. Hartwell
The Development of Automated Test Procedures for Complex Electro-Mechanical Systems—Mechanical Failures Prevention Group, Gaitherburg, Md. (4/81)

J. M. Laskey|R.J. Wildenberger
Pattern Recognition Techniques for Automatic Evaluation of Hybrid Microcircuits—NEPCON West '81, Anaheim, Calif. 2/25/81

S.B. Mesnick
The Evolution of DoD Warranty Requirements—National Contract Management Association Workshop, Waltham, Mass. (3/81)

S.S. Perra
Reduction of Test Equipment Proliferation with Third Generation ATE—Mechanical Failures Prevention Group, Gaitherburg, Md. (4/81)

J.C. Phillips
Professional Communications—Society of Women Engineers, Boston Univ., Boston, Mass. (4/81)

J.C. Phillips
Professional Communications—ASME Student Chapter, Univ. of Lowell, Lowell, Mass. (4/81)

K.I. Pressman
Session Chairman and Organizer of Workshop on Contracting Concepts—National Contract Management Assoc. Workshop, Waltham, Mass. (3/81)

R.E. Range
Public Law 95-507 — An Overview of Subcontracting Plans for Small Businesses—National Contract Management Assoc. Workshop, Waltham, Mass. (3/81)

Commercial Communications Systems

R.M. Unetich
UHF Variable Coupler Presentation—Presented to PBS Engineering Committee at KLVK-TV, Las Vegas, Nev. (4/11/81)

R.S. Zborowski
Recent Improvements in UHF TV Transmitter Efficiency—Presented to Association of Federal Communication Consulting Engineers at Washington, D.C. (2/19/81)

Laboratories

R.C. Alig
Kinescope Electron Gun Design—*RCA Review*, Vol. 41 (12/80)

R.A. Bartolini
Diode Laser Optical Recording Using Trilayer Structures—*IEEE Jour. of Quantum Electronics*, Vol. QE-17, No. 1 (1/81)

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Optical Discs for Information Storage—*Nature*, Vol. 287, No. 5783, pp. 583-585, MacMillan Journals Ltd., 1980 (10/16/80)

D. Botez
InGaAsP/InP Double-Heterostructure Lasers: Simple Expressions for Wave Confinement, Beamwidth and Threshold Current over Wide Ranges in Wavelength (1.1-1.65 μm)—*IEEE Jour. of Quantum Electronics*, Vol. QE-17, No. 2 (2/81)

C.R. Carlson|R.W. Cohen
A Simple Psychophysical Model for Predicting the Visibility of Displayed Information—*Proceedings* of the SID, Vol. 21, No. 3 (1980)

K.K.N. Chang
An Analytic Solution of a Magnetic Electron-Beam Bender—*RCA Review*, Vol. 42, No. 1 (3/81)

D.J. Channin|G.H. Olsen|M. Ettenberg
Self-Oscillations and Dynamic Behavior of Aged InGaAsP Laser Diodes—*IEEE Jour. of Quantum Electronics*, Vol. QE-17, No. 2 (2/81)

J.I. Gittleman|E.K. Sichel
Are Pyrolyzed Polyimides Conducting Polymers?—*Jour. of Electronic Materials*, Vol. 10, No. 2 (1981)

F.Z. Hawrylo
Efficient Visible Emission from Highly-Doped Liquid-Phase Epitaxially Grown InP—*Applied Physics Letters*, Vol. 37, No. 11 (12/1/80)

M.L. Hitchman|V. Eichenberger
A Simple Method of End-Point Determination for Plasma Etching—*Jour. Vac. Sci. Technol.*, American Vacuum Society, Vol. 17, No. 6 (11-12/80)

S.T. Hsu
Low Frequency Excess Noise in SOS MOS FETs—*RCA Review*, Vol. 41 (12/80)

A.C. Ipri
Evaluation of CMOS Transistor Related Design Rules—*RCA Review*, Vol. 41 (12/80)

E.O. Johnson|S. Tosima
Visual-Perception-Related Effects in Chinese-Japanese Written Characters—*RCA Review*, Vol. 42, No. 1 (3/81)

H. Kressel
Semiconductor Lasers—*Handbook on Semiconductors*, Vol. 4, North-Holland Publishing Co. (1981)

M. Kumar
Dual-Gate MESFET Variable-Gain Constant-Output Power Amplifier—*IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-29, No. 3 (3/81)

I. Ladany|S.H. McFarlane III
J.T. McGinn
The Role of Buffer Layers in Reducing Degradation in Lasers and LEDs—Inst. Phys. Conf. Ser. No. 56: Chapter 6

V. Mangulis
Frequency Diversity in Low Angle Radar Tracking—*IEEE Transactions on Aerospace and Electronic Systems*, Vol. AES-17, No. 1 (1/81)

A.R. Moore
Carrier Lifetime in Photovoltaic Solar Concentrator Cells by the Small-Signal Open-Circuit Decay Method—*RCA Review*, Vol. 40 (12/80)

G.H. Olsen|T.J. Zamerowski
Vapor-Phase Growth of (In,Ga)(As,P) Quaternary Alloys—*IEEE Jour. of Quantum Electronics*, Vol. QE-17, No. 2 (2/81)

D. Refield
Method for Revaluation of Antireflection Coatings—*Solar Cells*, Vol. 3, pp. 27-33, ©Elsevier Sequoia/Printed in The Netherlands (1981)

D. Redfield
Selective Observation of Electrically-Active Grain Boundaries in Silicon—*Appl. Phys. Lett.*, Vol. 38, No. 3, ©1981 American Institute of Physics (2/1/81)

G.A. Reitmeier
Spatial Compression and Expansion of Digital Television Images—*RCA Review*, Vol. 42, No. 1 (3/81)

D. Thebault|L. Jastrzebski
Review of Factors Affecting Warpage of Silicon Wafers—*RCA Review*, Vol. 41, No. 4 (12/80)

J.H. Thomas, III|D.E. Carlson
An AES/XPS Study of the Chemistry of Palladium on Hydrogenated Amorphous Silicon Schottky Barrier Solar Cells—*Jour. Electrochem. Soc.: Solid State Science and Technology* (2/81)

J.H. Thomas, III
Phosphorus Concentration in Hydrogenated Amorphous Silicon Using Ion-Implanted References—*Jour. Vac. Sci. Technol.*, Vol. 17, No. 6, 1980 American Vacuum Society (11-12/80)

C.P. Wu|E.W. Maby (MIT Cambridge, Mass.)
Carrier Mobility in Laser-Annealed Silicon-on-Sapphire Films—*RCA Review*, Vol. 42, No. 1 (3/81)

P.J. Zanzucchi|W.R. Frenchu
Optical Reflectance: A Sensitive Nondestructive Method for Detecting Surface Damage in Crystalline GaAs and Other Semiconductors—*APPLIED OPTICS*, Vol. 20, No. 4 (2/15/81)

Missile and Surface Radar

K. Abend
Spectral Estimation for Doppler Resolution in Radar Imaging of Aircraft—Valley Forge Research Center, Noontime Seminar, Moore School of Electrical Engineering, Univ. of Pa. (3/81)

O.G. Allen
Considerations for Productivity Improvement (During the Product Design and Manufacturing Phase)—Workshop on Quality Assurance Defense Logistics Agency, Headquarters, Cameron Station, Alexandria, Va. (3/81)

W.H. Beckett
Development Experience in Distributed Simulators—Proceedings, Twelfth Annual Pittsburgh Conference on Modeling and Simulation, Pittsburgh, Pa. (4/30/81 & 5/1/81)

F.J. Buckley
Software Quality Assurance—Instructor, IEEE Three-day Continuing Education Seminar, San Francisco, Calif. (3/81); London, England (3/81)

D.B. Campbell, *et al.*
Design Budgeting—A Bold New Ship Acquisition...Now a Proven Concept—*Naval Engineers Jour.*, ASNE, Washington, D.C. (4/81)

S.R. Chowdhury
Effect of Memory Contention on Processing Time—*Proceedings*, Twelfth Annual Pittsburgh Conference on Modeling and Simulation, Pittsburgh, Pa. (4/30/81 & 5/1/81)

A. Chressanthis|B. Gaffney
M. Rauchwerk, presenter
An Analysis of the Detection Performance of a Digital Hard Limited CFAR—*Proceedings*, IEEE Southeastcon '81, Huntsville, Ala. (4/81)

B. Gaffney|J.J. O'Brien
(presenter, M. Rauchwerk)
A High Speed Digital Noise Generator—

Proceedings, IEEE Southeastcon '81 Conference, Huntsville, Ala. (4/81)

G.J. Gaudreau
Environment Simulation Technique for Subprogram Testing—*Proceedings*, Twelfth Annual Pittsburgh Conference on Modeling and Simulation, Pittsburgh, Pa. (4/30/81 & 5/1/81)

W.C. Grubb, Jr.
Electro-Optics for Non-Electrical Engineers—George Washington Univ., Washington, D.C. (3/81)

W.C. Grubb, Jr.
Minicomputers and Microprocessors for Non-Electrical Engineers—Drexel Univ., Philadelphia, Pa. (4/81)

J.H. Johnson
Applying Simulation Concepts to Verification Testing—*Proceedings*, Twelfth Annual Pittsburgh Conference on Modeling and Simulation, Pittsburgh, Pa. (4/30/81 & 5/1/81)

R.W. Martin
Automated Phased Array Antenna Testing—The Near Field Approach—L.I. Chapter IEEE, Polytechnic Institute of New York (3/81)

R.J. Renfrow
AEGIS System Performance in ECM—Association of Old Crows, Huntsville, Ala. (4/81)

R.L. Schelhorn
Thick-Film Copper Circuit Applications—Joint Keystone—New York ISHM, Edison, N.J. (4/81)

R.L. Schelhorn
Thick-Film Copper for Multi-Layer and Co-Fired Circuit Applications—Canadian/American ISHM Symposium, Ottawa, Canada (4/81)

A.J. Stanchina
Comments on Design Budgeting—A Bold New Ship Acquisition Strategy - Now a Proven Concept—ASNE Day 1981, Washington, D.C. (4/30/81 & 5/1/81)

Solid State Division

J.J. Chinery|R. Buckley
Voltage-Breakdown Testing of Power Transistors—*New Electronics*, Vol. 13, No. 22 (11/11/80)

N.A. Macina
Maximum Entropy Modeling for Identification and Detection of Certain Classes of Dynamic Events—*RCA Review*, Vol. 42, No. 1 (3/81)

I.E. Martin
A New High-Frequency SCR for Use in Inverters and Motor Controllers—Eighth International Solid-State Power Electronics Conference, Dallas, Tex. (4/29/81)

Engineering News and Highlights

Woll appointed Staff Vice-President and Chief Engineer

In March 1981, **Dr. Harry J. Woll** was appointed Staff Vice-President and Chief Engineer, RCA Electronic Products, Systems and Services. Previously, Dr. Woll was Division Vice-President and General Manager, Automated Systems, in Burlington, Mass.

Since joining RCA as an engineer in 1941, Dr. Woll has progressed through engineering and operations management positions of increasing responsibility. His professional career has included activity and responsibility in the development of circuitry, micro-electronics, lasers, computers, electro-optics, automatic test equipment and air traffic control systems. He holds 20 patents in electronics.

Hospodor appointed Division Vice-President and General Manager of Automated Systems

Andrew T. Hospodor has been appointed Division Vice-President and General Manager of RCA Automated Systems. Mr. Hospodor joined RCA in 1966 and advanced through a series of positions to Marketing Director of the RCA Advanced Technology Laboratories in Camden, New Jersey. He transferred to RCA Automated Systems in 1977 as Director of Marketing and Advanced Planning. In 1979, he was named manager of Command and Control Programs, directing RCA's efforts in command and control and undersea warfare programs.

Mr. Hospodor holds a bachelor's degree in Mechanical Engineering from Cornell University as well as a master's degree in Business Administration and Mechanical Engineering from Lehigh University. In 1976, he completed the Harvard University program for Management Development.

Dukes is new Ed Rep at Laboratories

Eva Dukes has been appointed Editorial Representative for RCA Laboratories, Princeton. She joined RCA in 1976 as Administrator, Technical Publications. Her department is involved in editing government contract reports, proposals, and, intermittently, other types of technical copy. In 1980, she was IR&D Coordinator for the Laboratories.

Ms. Dukes began her publications career as a technical writer at GAF Corporation. Most of her time at Interscience Publishers

E. Dukes

(later merged with John Wiley & Sons, Inc.) was spent as Associate Editor of the Kirk-Othmer *Encyclopedia of Chemical Technology*, 2nd ed. At Globe Book Co., she was Executive Editor for Science and at Marcel Dekker, Inc., she was acquisitions editor for several series of medical books. In 1977-78, Ms. Dukes was President of the New York Chapter of the Society for Technical Communications.

Contact her at:
RCA Laboratories
Princeton, N.J.
TACNET: 226-2882

Staff Announcements

Consumer Electronics

J. Peter Bingham, Division Vice-President, Engineering, announces the organization of Engineering as follows: **Larry A. Cochran,** Manager, Signal Systems and Components; **Eugene Lemke,** Chief Engineer, Advanced Projects; **James A. McDonald,** Manager, Display Systems Engineering; **Perry C. Olsen,** Manager, Product Design Engineering; and, in the New Products Laboratory, **James E. Carnes,** Manager, Television Advanced Development; and **J. Peter Bingham,** Acting Manager, Digital Systems.

Larry A. Cochran, Manager, Signal Systems and Components, announces the appointments of **Roger W. Fitch** as Manager, Components Engineering, and **Ronald R. Norley** as Manager, Competitive Analysis and Taiwan Coordination.

Perry C. Olsen, Manager, Product Design Engineering, announces the organization of Product Design Engineering as follows: **Robert D. Altmanshofer,** Manager, Engineering—Juarez; **Eldon L. Batz,** Manager, Resident Engineering; **Elmer L. Cosgrove,** Manager, Engineering Services; **Melvin W. Garlotte,** Manager, Mechanical Engineering Television Instrument Design; **James J. Kopczynski,** Manager, Project Engineering; **James C. Marsh, Jr.,** Manager, Project Engineering; **Roger D. Sandefer,** Manager, Engineering Design Support; **James B. Waldron,** Manager, Mechanical Engineering Television Chassis and Sub-Assembly Design; and **Paul C. Wilmarth,** Manager, Project Engineering.

James E. Carnes, Manager, Television Advanced Development, announces the organization of Television Advanced Development as follows: **John C. Peer,** Manager, Television Systems Development; **Richard A. Sunshine,** Manager, Advanced Mechanical Engineering and Computer-Aided Design; **Craig S. Young,** Manager, Mechanical Computer-Aided Design; and **James E. Carnes,** Acting Manager, Technology Applications.

Distributor and Special Products

Jack K. Sauter, Group Vice-President, announces the appointment of **Edward A. Boschetti** as Division Vice-President and General Manager, Distributor and Special Products Division.

Government Systems Division

Francis H. Stelter, Jr., Division Vice-President, Marketing, announces the appointment of **David Shore** as Division Vice-President, Business Development.

Laboratories

Brown F. Williams, Staff Vice-President, Display and Energy Systems Research, announces the organization of Display and Energy Systems as follows: **Carmen A. Catanese,** Director, Picture Tube Systems Research Laboratory; **Robert D. Lohman,** Director, Display Processing and Manufacturing Research Laboratory; and **Brown F. Williams,** Acting, Energy Systems Research Laboratory.

James J. Tietjen, Staff Vice-President, Materials and Components Research, announces the appointment of **Jon K. Clemens** as Director, VideoDisc Systems Research Laboratory.

Jon K. Clemens, Director, VideoDisc Systems Research Laboratory, announces the organization of VideoDisc Systems Research Laboratory as follows: **Marvin Blecker** continues as Head, Systems Evaluation Research; **Paul W. Lyons** continues as Manager, VideoDisc Testing Center; **John G.N. Henderson,** Head, Signal Systems Research; **James J. Gibson** continues as Fellow, Technical Staff; **Eugene O. Keizer** continues as Staff Scientist; **James J. Power,** Head, Player Control Research; **John A. vanRaalte** continues as Head, Video Recording Research; and **John H. Reisner** continues as Fellow, Technical Staff.

Arthur Kaiman, Director, Advanced Systems Research Laboratory, announces the organization of the Advanced Systems Research Laboratory as follows: **Ted N. Altman,** Head, Microsystems Research; **Charles M. Wine** continues as Fellow, Technical Staff; **Allen J. Korenjak** continues as Head, Software Technology Research; **Thomas M. Stiller** continues as Fellow, Technical Staff; **Emilie M. Lengel** continues as Head, Systems Technology Research; **Allen H. Simon** continues as Fellow, Technical Staff; **Eduard Luedicke** continues as Fellow, Technical Staff; **Martin Rayl** continues as Head, Manufacturing and Product Assurance Research; **D. Alex Ross** continues as Staff Engineer; and **Lawrence D. Ryan** continues as Head, Microtechnology Research.

David E. O'Connor, Director, Integrated Circuit Technology, Research Laboratory, announces the organization of the Integrated Circuit Technology Research Laboratory as follows: **Norman Goldsmith** continues as Head, Lithography and IC Processing; **Gary W. Hughes** continues as Head, LSI Imagers and Special Devices; **Walter F. Kosonocky** continues as Fellow, Technical Staff; **Paul K. Weimer** continues as Fellow, Technical Staff; **Louis S. Napoli,** Head, LSI Devices and Memories; and **George L. Schnable** continues as Head, Device Physics and Reliability.

David D. Holmes, Director, Consumer Electronics Research Laboratory, announces the organization of the Consumer Electronics Research Laboratory as follows: **Thomas V. Bolger,** Head, Signal Processing Research; **Dalton H. Pritchard** continues as Fellow, Technical Staff; **Robert H. Dawson** continues as Head, New Technology Applications Research (Somerville); **Leopold A. Harwood** continues as Fellow, Technical Staff; **Stanley P. Knight** continues as Head, Signal Conversion Systems Research; **Lubomyr S. Onyshkevych** continues as Head, Electronic Packaging Research; **Werner F. Wedam** continues as Head, Television Receiver Systems Research; and **Kern K.N. Chang** continues as Fellow, Technical Staff.

Solid State Division

Leonard W. Grove, Manager, Electro-Optics & Devices, Manufacturing, announces the appointment of **Richard W. Longsderff** as Manager, Manufacturing Methods and Industrial Engineering.

Fifty-one Scientists honored at RCA Labs

Fifty-one scientists have been given RCA Laboratories Outstanding Achievement Awards for contributions to electronics research and engineering during 1980, it was announced by **Dr. William M. Webster,** Vice-President, RCA Laboratories.

Recipients of individual awards are:

Andrew G.F. Dingwall, for the development application, and commercial demonstration of a dramatic new MOS approach to the high-speed A/D circuits needed for commercial and TV applications.

John R. Fields, for the development of theoretical and computer models leading to improved understanding and design of electron-optical systems for new displays.

Robert E. Flory, for the development of signal-processing circuitry used in a lightweight broadcast television recorder.

Smith Freeman, for contributions to the theory and practice of analog fault-isolation techniques.

Donald R. Preslar, for the development of high-performance bipolar circuits.

Chih Chun Wang, for contributions to the science and technology of VideoDisc lubrication.

George J. Whitley, for product-assurance innovations in the factory environment.

Peter J. Zanzucchi, for developing and implementing innovative methods in optical spectroscopy and applying them in the solution of many urgent problems.

Recipients of team awards are:

William E. Babcock, Irwin Gordon and **Frank S. Wendt,** for contributions to the development of a novel power-supply system.

C. Rodney Burg, Ernest E. Doerschuk, Pabitra Datta, Abraham Goldman, and **Aaron W. Levine,** for contributions to the development and implementation of casein-based etch resists for aperture-mask production.

Danny Chin, John G.N. Henderson, and **Robert J. Maturo,** for contributions to the development of novel TV tuning systems.

Shiu-Shin Chio, David A. Furst, Rudolph H. Hedel, Michael J. Mindel, and **Harry L. Pinch,** for contributions to the development of a mass-produced, durable VideoDisc stylus electrode.

John F. Corboy, Jr., and **Michael T. Duffy,** for contributions to the development and application of an innovative technique for the optical characterization of the near-surface crystal structure of silicon.

Brian R. Dornan, Ho-Chung Huang, Paul F. Pelka, Walter J. Slusark, Jr., and **You-Sun-Wu,** for contributions to the development of solid-state, GaAs FET power amplifiers for use in RCA SATCOM satellites.

Frank Z. Hawrylo, Ivan Ladany, and **Gregory H. Olsen,** for contributions to the development of 1.3 μm InGaAsP lasers and LEDs.

Macy E. Heller, William C. Henderson, III, Grzegorz Kaganowicz, W. Ronald Roach, and **John W. Robinson,** for contributions to micromachining technology.

Eric F. Hockings, Harry E. McCandless, and **Carl H. Meitzer,** for contributions to the development of a modularization procedure in the beam-forming region of an electron gun.

Krishnamurthy Jonnalagadda, Richard J. Klensch, and **Dipankar Raychaudhuri,** for contributions to the modeling, analysis, and measurement of the nonlinear crosstalk effects of two carriers sharing a satellite transponder.

John H. Reisner, Robert E. Simms, John Valachovic, and **Corris A. Whybark,** for contributions to the development of improved VideoDisc cutter heads.

Barkow honored

William H. Barkow, Picture Tube Systems Research Laboratory, has been appointed a Fellow of the Technical Staff of RCA Laboratories. The designation of Fellow is comparable to the same title used by universities and virtually all technical societies, and is given in recognition of a record of sustained technical contributions in the past and of anticipated continued technical contributions in the future.

Automated Systems Technical Excellence Awards for Third and Fourth Quarters of 1980

The Burlington Technical Excellence Committee has reviewed nominations submitted during the third and fourth quarters of 1980. The results are one team award selection and one individual award selection.

Team Award

The Advanced Autonomous Array (A^3) design, development and test groups achieved technical excellence while displaying enthusiasm and dedication. The Team's professional approach to problem solving, close coordination, innovative approach to integration, and steadfast application of diligence and energy resulted in the successful achievement of program objectives. Cited for their achievements are:

P. Berrett
J.B. Bourque
D.J. Cassidy
P.S. Eggimann
R.C. Guyer
W.X. Johnson
D. Lambropoulos
D.A. Panaccione
M.A. Polanik
L.E. Rhodes
H.L. Slade
R.E. Tetrev

The A^3 program objective is to develop and apply new LSI array computer technology to data processing of undersea acoustic signals, in order to implement a remote, unattended submarine tracking system. The feasibility phase of the program was completed. It demonstrated to the Navy and DOD a significant milestone in showing the capability of this new system.

RCA Automated Systems, using the ATMAC from ATL, developed the A^3 hardware and software. The system was successfully integrated and tested by AS personnel in the fall of 1980 on a Pacific ocean sea test. The team effort consisted of:

- Development of a two-way communication system.
- Development of software for the Shore Based Processor and Control Station (SBPCS).
- Integration of an advanced LSI microcomputer (the ATMAC) into a buoy data processing subsystem.
- Integration of the RCA buoy equipment with the Sanders undersea acoustic array.
- Total systems integration (sea, satellite

Advanced Autonomous Array Team Award winners with H.J. Woll, Division Vice-President and General Manager; E.M. Stockton, Chief Engineer; and R.K. Gorman, Manager, Design Engineering. (Left to right, front row) Dr. Woll, R. Gorman, L.E. Rhodes, D.J. Cassidy, J.B. Bourque, P. Berrett, W.X. Johnson. (Back row) E.M. Stockton, R.C. Guyer, M.A. Polanik, R.E. Tetrev, P.S. Eggimann, D.A. Panaccione, D. Lambropoulos, H.S. Slade. (Currently, Dr. Woll is Staff Vice-President and Chief Engineer, Electronic Products, Systems and Services. E.M. Stockton is now Manager, Command and Control Programs, Automated Systems,Burlington).

Left to right: D.M. Priestley, Chief Engineer; A.C. Muller and Mrs. Muller; B.A. Bendel, Manager, Design Engineering. (D.M. Priestley was named Chief Engineer in March 1981.)

relay and land hardware and software) and successful data taking operations.

In addition to the development tasks, it was necessary for part of the team to work on a Navy ship at sea during the evaluation phase. This group was responsible for final setup adjustments and kept the buoy equipments operating properly, despite difficult working conditions.

Individual Award

Albert C. Muller has been recognized for technical excellence in the design of a programmable pulse generator used on the E3A Depot ATE.

The EQUATE ATE System contains two independent, fully programmable 100 MHz pulse generators, implemented via a combination of RF cans and two layer PCBs. Customer requirements dictated the need for eight such generators in the same physical space (17 x 10 x 3 inches), as the previous two.

Al Muller, lead design engineer on the project, recognized that, though a new logic design would be required for this application, the key to a successful implementation was being able to package over 30 high-speed ECL integrated circuits on a 9½- x 3-inch PCB. The space constraint required a multi-layer PCB design where impedances were very carefully controlled among the variables of PCB material, PCB layer spacing, and etch width and length.

The RCA Standards did not provide a "Cookbook" solution to this problem. Al Muller developed the necessary design rules, identified the appropriate PCB materials, and evaluated alternative form factors. He produced a design consisting of a seven-layer PCB, including two 50-ohm and two 100-ohm layers and created a new logic design for the overall pulse assembly using only the new controlled impedance PCBs, thereby eliminating the need for costly and space consuming RF cans. The final product met both the physical and electrical requirements. Equally as important, a new set of design rules have been developed which can be used for a variety of high-density digital IC packaging problems.

Symposium on Mechanical Engineering held at Moorestown

The second RCA corporate technical symposium for mechanical engineers was held on April 23, 1981, at Missile and Surface Radar, Moorestown, N.J. The theme of the symposium was "Mechanical Design for Producibility." About two-thirds of the close to 100 symposium attendees from many locations and business units exchanged experiences at a reception on the evening prior to the symposium. **George R. Field,** the chairman/organizer of the symposium, introduced the speakers and his planning committee at this occasion.

Joseph C. Volpe, Director, Product Operations, MSR, opened the symposium with a welcome and emphasized the value of a work session of this kind. **Bernard J. Matulis,** Chief Engineer, MSR, followed with a keynote on the meeting's theme. Following a dozen presentations with question and answer interplay, a tour of the AEGIS production test center was conducted.

The speakers and their topics are listed below. If you have a need for specifics on a particular talk, contact the respective author(s).

Managing Design for Producibility
James C. Miller, *Picture Tube Division*

Packaging Density and Environment Factors
Mike Risch, *Missile and Surface Radar*

Role of Manufacturing Engineering in Design Process
Earl Horne/Jack Drake/, *"SelectaVision"*

Innovation in Product Design
M. Holbreich, *Government Communications Systems*

Computer-Aided Design of Shell and Tube Heat Exchanger
William Bernard, *Missile and Surface Radar*

Bench Marking Computer-Aided Design Systems for Printed-Circuit
V. Iandoli, *Government Communications Systems*

Mechanical Design and Integration of Phased Arrays
John Drenik, *Missile and Surface Radar*

Analytical Evaluation of the Composite Communications Satellite Antenna Reflector Design
J.R. Badura/R.N. Gounder/K.W. Tung, *Astro-Electronics*

Analog and Digital Module Nests, the Productivity of their Manufacture Balanced against the Productivity of their Use
William C. Young, *Missile and Surface Radar*

Space Shuttle Closed-Circuit Television System
Derek S. Binge, *Astro-Electronics*

The Evaluated Tubular Collector
Marvin S. Crouthamel, *Advanced Technology Laboratories*

Overview of AEGIS System
William E. Scull, *Missile and Surface Radar*

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Cablevision Systems		
*John Ovnick	Van Nuys, California	534-3011

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Francis Holt	Indianapolis, Indiana	422-5217
Chuck Limberg	Indianapolis, Indiana	422-5117
Don Willis	Indianapolis, Indiana	422-5883

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*Ed Goldberg	Princeton, New Jersey	229-2544
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Dale Sherman	Burlington, Massachusetts	326-2985
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GSD Staff		
*Ed Moore	Cherry Hill, New Jersey	222-5833
Missile and Surface Radar		
*Don Higgs	Moorestown, New Jersey	224-2836
Jack Friedman	Moorestown, New Jersey	224-2112

National Broadcasting Company (NBC)

*Bob Mausler	New York, New York	324-4385

Patent Operations

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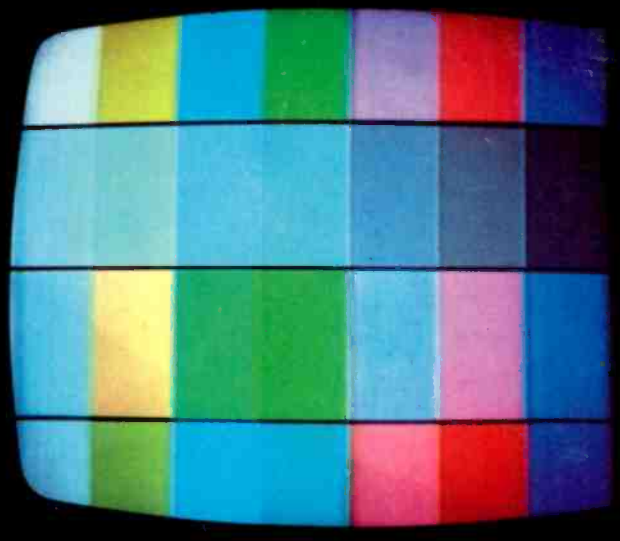

The subjective display portion of the light-to-light computer simulation for the horizontal transient response of an NTSC color television system is shown here. Four different program results can be simultaneously displayed. For further information see pages 15-23.

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