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Do it right the first time!

Do it right the first time! applies to all phases of a product's development and life. The importance of everyone focusing on quality is stated by **Dave Troxel** in his article on page 57, and **Roy Pollack** gives his perspective on the subject of quality in the cover message on the facing page.

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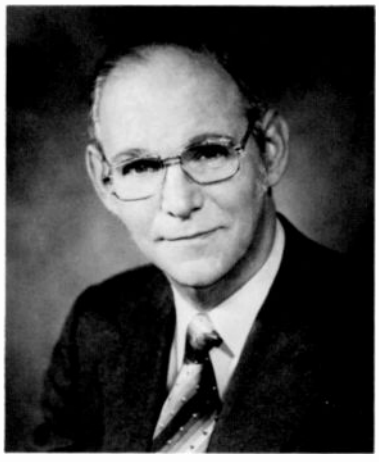
•To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

Good quality is good business



Roy H. Pollack

My feelings on the subject of quality can be expressed in one short sentence: Good quality is good business. Let me offer a few reasons to support this:

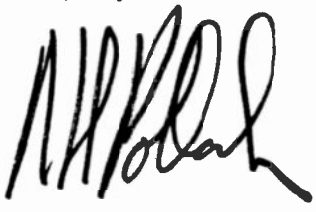
1. Quality dictates the size and nature of our financial exposure. Think about the tremendous financial losses incurred in many industries in recent years as a direct result of product recalls. A manufacturer who is quality negligent will not long survive in the marketplace.

2. Quality determines our capability to compete successfully. Japan has made quality a critical competitive element. We can no longer confuse, rationalize, ignore or deny the fact of outstanding Japanese quality. Let us make quality so important in our operations that it becomes a positive constant in the sales equation. We will then beat our competition.

3. Quality is the best integrating report card available to grade the total business structure. It is the best measure of management effectiveness. Quality — good or poor — begins with the inception of a project; it starts with product and market planning. A quality rating begins by asking these types of questions:

- Have we planned such a short product life that we cannot really benefit from the life cycle learning curve?
- Did we really complete the research and development tasks?
- Did the engineering sign-off of the design have complete validity?
- Do we recognize that quality, like signal to noise, degrades as we move through processing operations?
- Do we detect, and positively react to, small signals of *un*quality fast enough? Or do we simply hope those signals will disappear?
- Do we realistically and appropriately allow cost to assure quality?
- Do we recognize that software requires the same elements of design, planning, and control as does hardware?
- Do we expect to achieve quality at the final test station? Or do we recognize that the end of the line is far too late to build in quality?
- Have we provided enough time and resources to carry a product through all the essential and necessary steps so that we can honestly dignify the item by calling it a product?

Our challenge is to make quality a pervasive reality at RCA. If we agree that "Good quality is good business," and if we take the appropriate actions to develop a true quality milieu, then we will indeed be making a great contribution to the success of our company.



Roy H. Pollack
Executive Vice President

Highlights

data collection and analysis

automating the collection and analysis of test data reduces labor and rework costs, increases yields and reduces field failure.

page 9

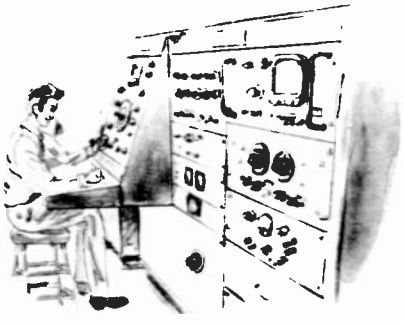
software systems

software reliability is the probability of "satisfactory" operation for a specified time in a specified environment.

page 18

components

how are failure rates estimated when little or no data are available?
how is high reliability attained through chip complexity?



page 36

the service area

a customer-oriented quality service program and a new approach to service training and rating provide new levels of optimum service.

page 42

in future issues

RCA worldwide, color TV receivers, anniversary issue, custom LSI, communication trends, computer-aided design

Illustrations by L.M. Carr

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E. Shecter

Product assurance and RCA

The following paper points out the objectives of this issue and briefly describes the contents of each group of articles.

The Product Assurance role in our corporate entities covers a broad range of disciplines that help RCA to deliver a product that will meet or exceed our customers' expectations. To do this task in a way that has a favorable impact on the profitability of the corporation and supports increased market penetration is the challenge that we must face.

The decade of the eighties may well be characterized by competition in the marketplace of product quality and long-term trouble free service. We have already observed during the seventies the inroads in the market achieved by Japanese products whose superior performance helped capture substantial market share. We have seen the development of a more sophisticated consumer who demands more of the products he purchases. We have seen legislation that penalizes companies whose products are unreliable or unsafe through legal action and this will continue. We have seen the cost of services rise very substantially so that consumers have become sensitive to maintenance costs. And in the military and government area, we have seen the increasing demand for reliable equipment to support fleet readiness or mission assurance or low life cycle costs as the means of competitive evaluation. How effectively Product Assurance responds to these challenges may well be a determining factor in our corporate growth and profitability.

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This issue's objective

The papers in this issue of the *RCA Engineer* are but a sampling of the kinds of technology and management support the Product Assurance function can provide to improve the likelihood that we will achieve these goals. But the Product Assurance disciplines must apply in conjunction with other technological and management growth. The explosion in electronic technology must lead to improved functional performance as well as improved life performance of our products. At the same time, management must provide the leadership and focus so that the total resources of the company reduce waste in all forms such as excess trouble shooting, rework, scrap and warranty costs — all of which reduce performance and have adverse bottom line impact.

There are many roles and activities under way in the various business areas of RCA and this issue is devoted to providing information on some of the techniques used in these business areas. The objective is to stimulate your imagination — as you read these articles, think about how the methodology might be adopted or adapted to your particular area of interest to improve your business.

Product Assurance spans the scope of business activities from the concept stages in design throughout the design process, into the procurement phases through manufacturing and test, final acceptance and ultimately in the field performance. It applies equally well to services and program software as well as hardware.

Parts product assurance

This group of papers addresses an application of quality technology to parts design and manufacture. In picture tubes, the use of statistically designed experiments enabled the comparison of multiple factors affecting performance and the interaction of these factors to identify those characteristics that are significant. Using this technique, an important breakthrough resulted in the development of low arc picture tubes. This and other statistical methods can be extremely useful in developing optimum design and process specifications and should be considered in all of our business operations. Statistical support is available to all business areas upon request.

Also in the parts area, the programs are discussed that are in use at the Solid State Division to stress test new and existing SSD devices to identify failure mechanisms and provide information on design and process problems. This important contribution to SSD device performance not only provides an insight into efforts to improve devices but also is useful in analyzing stress testing that can be performed in other business units. The concept of real-time indicators (RTI), which are accelerated tests used for process control purposes, is also reviewed.

Concurrently with device reliability stress testing, device technology is rapidly expanding. Also pointed out, by example, is the benefit in performance and reliability using large scale integration (LSI) rather than small scale or medium scale integra-

tion in design. The tradeoff in time and cost along with reliability is explored. RCA, as a leader in engineering technology, is heavily involved using LSI, microprocessors and other state-of-the-art technology in all of its electronic product lines.

Product assurance in the service area

How RCA Service Company collects quality data to use in measuring service quality and how data are put to use to continually upgrade the quality of service is illustrated. This is but one aspect of a comprehensive and diverse set of quality programs in use at the Service Company.

In an attempt to similarly measure service quality at RCA Americom, the approach taken to measure communication service quality for a diverse range of services is presented. The system provides visibility into service quality and triggers corrective action that has led and continues to lead in the direction of improved service to our customers.

Product assurance in commercial products

Many of the techniques used in the military are usable in commercial areas. This is taken into cognizance in comparing requirements for the coaxitron amplifier produced by our Electro-Optics and Devices activity in Lancaster. How the application of military specification quality requirements, while initially appearing to be more stringent and more costly, ended up by reducing scrap, rework and warranty costs to a point which more than offset the increased cost of a more rigorous control system is demonstrated.

In still another application of a military technique to a commercial environment, the application of Reliability Growth Testing to a commercial airborne radar is reviewed. This technique is used on all new products prior to production release. Combined stresses including thermal cycling and vibration along with on-off equipment operation have the effect of shortening evaluation time and identifying potential equipment weaknesses. Design or manufacturing modifications can be implemented prior to costly changes during production. Illustrative data are presented from the actual results obtained on one

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For more references, see page 60.

specific weather radar. This method coupled with some other reliability approaches such as part level burn-in on selected parts have led to significant reductions in warranty costs and greatly improved customer satisfaction.

Not to be outdone, methods such as this are being implemented in our Broadcast operation in manufacturing commercial studio television cameras, tape recorders and other broadcast equipment. How the Standards Program is used as a focal point for implementing design and manufacturing practices to produce high reliability equipment at competitive prices is demonstrated. Broadcast reports that the high quality and reliability achieved are a strong point enabling increased sales coupled with reduced warranty costs. It should be emphasized that Broadcast also uses the concept of 100 percent thermal cycling of boards to stress parts and cause marginal part or workmanship problems to surface in test.

Product assurance in military systems

Normally, the reliability aspect of Product Assurance initiates the process. The relationship of the systems designers to the reliability activity is addressed. An illustration is given of how the systems design is influenced by reliability considerations in military hardware and how the reliability engineer must continue his efforts in conjunction with design engineering to develop a system that achieves not only performance objectives but reliability requirements simultaneously. Done properly, total design and subsequent system costs can be minimized — when done without proper and timely coordination, costs rise and either performance or reliability suffers. With continued demands for longer, trouble-free performance, it is imperative that lessons learned from this presentation be applied universally throughout the company.

Along these same lines, our military customers are seeking ways to provide some systems with the capability of meeting requirements without human attendance. The equipment operating and support costs are rising so rapidly that funds that would normally be used for acquisition of new weapons systems are being drained off to provide for operation and support of existing equipment. One possible solution is to develop equipment requiring a minimum of operating and support personnel. Techniques used to develop an approach to solving this problem are discussed. Similar techniques could be adapted to non-military equipment and those readers involved in commercial systems might well consider the approaches used for this purpose.

A practical example of low-cost design while still meeting a reliability requirement uses the Design to Unit Production Cost (DTUPC) concept. This was put to use on the Simplified Test Equipment for Internal Combustion Engines (STE/ICE) in our Automated Systems Business Unit. A major contributor to enabling fifty percent cost reduction in the design phase (and ultimately in production) was the contribution of the reliability activity through the use of the proper quality level semiconductors.

Software product assurance

As weapon systems become more complex, computers and computer programs assume an increasing share of the system and, therefore, affect the system's reliability. There are distinct conceptual differences between hardware and software reliability. Some of these differences are identified and an overview of the current models for prediction of software reliability is presented. In addition, some techniques are mentioned which can be used to improve software reliability. This subject is one that could well occupy volumes in its own right, but the purpose in including it is to sensitize the reader to the subject.

Data collection and analysis

Recognizing that a business must be run in a manner that not only generates a product or a service but must also simultaneously generate information that can be used to improve that product or service, several papers are included that demonstrate how various business areas generate and use this information. The Defect Analysis Repair and Trouble Shooting (DARTS) system is used in Consumer Electronics to provide real-time feedback of test information to enable rapid corrective action. Also presented is the Process Monitoring and Control (PMC) system, a computerized system that combines quality data with production status. It also provides for simple yet comprehensive statistical quality control capability. The computerized Manufacturing Attributes Planning Summary (MAPS) is discussed that is used in Electro-Optics Division to identify defects by processing area along with associated costs to allow management to properly prioritize corrective action.

Conclusion

These papers and others were presented at the first RCA Symposium on Reliability and Quality held at RCA Laboratories on October 18 and 19, 1979. The attempt was to demonstrate the wide range of reliability and quality techniques used in the various RCA business areas. Time did not permit the full scope of activities to be presented. These disciplines are considered key to RCA's continued success in the business world. Product and service quality in the broad sense are symbols of a mature, responsible corporation. As R.H. Pollack states in the introduction to this issue — *Good Quality is Good Business.*

Ed Shecter is a Fellow of the American Society for Quality Control and has served in various section and national offices. He has delivered over fifty papers on various subjects in Quality and Reliability throughout the country. He has published chapters in the *Handbook of Modern Manufacturing* by Maynard Research Associates and in the third edition of the *Quality Control Handbook* by J.M. Juran.

He is presently Manager, Special Programs, RCA Astro-Electronics. Prior to this assignment he was Director, Product Assurance, RCA "SelectaVision" VideoDisc operations, responsible for establishing product assurance policy for RCA VideoDisc operations. He also served as Manager, GSD Government Product Assurance, RCA Government Systems Division.

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H.S. Baird|T.M. Stiller

Quick analysis of TV factory tests and repairs— the DARTS system

Defect analysis for real-time supervision (DARTS) has successfully automated the collection and analysis of test and repair data on the chassis assembly line.

Abstract: *Up-to-the-minute information about the operation of an assembly line permits factory managers to identify and solve problems quickly. With increased automation of test equipment, available data have grown in volume and improved in quality. Manual collection and analysis are slow and sketchy at best.*

The test, troubleshoot, and repair loop on an RCA TV chassis assembly line is monitored by a minicomputer system, called DARTS (defect analysis for real-time supervision.) The flood of test data from automatic testers, and a trickle of repair entries from troubleshooters, are distilled to the essentials: throughput and yield of the test stations; most-frequent patterns of test rejects; and most-frequent repairs.

Background

Up-to-the-minute information about the operation of an assembly line permits managers to identify and solve problems quickly. With the increasing use of automatic test equipment, the data potentially useful to managers have grown in volume and precision. Manual line monitoring methods have been relied upon in the past although they are slow and sketchy at best.

Computers can be successfully applied to this problem, particularly if a few simple manufacturing disciplines are observed. Consistent product flow makes it possible to ensure 100 percent automatic monitoring of throughput and yield. Product serialization permits the tracking of individual items and, thus, the association of repairs with reject symptoms. Computers are fast enough to monitor the large volume of automatic test data, and their memory can contain several days' production data. The result can be a much improved understanding of the behavior of the manufacturing system and, thus, improved control.

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Color TV chassis assembly line

The environment of the system we will describe is a modern color TV factory located in Bloomington, Indiana. The particular assembly lines are lines 11 and 12; *the exclusive concern* is the chassis assembly section of the line, as opposed to instrument assembly. These relatively new assembly lines are manufacturing a new chassis, and it was felt that close monitoring of the lines was essential, especially in the early months of operation. The line features a single test-troubleshoot-repair loop following all automatic and manual assembly.

Product flow

Each assembled chassis passes through four automatic test stations: two "alignment" stations (A1, A2); and two "test" stations (T1, T2) (Fig. 1). Each test station performs several dozen electronic tests under the control of a minicomputer. If the chassis passes all tests at all four stations, it then continues on to instrument assembly.

If the chassis fails any test at any station, it is automatically diverted to the troubleshooting area where the defect is identified and repaired and a description of the repair is recorded.

A repaired chassis is returned to the assembly line just prior to the first test station (A1), where it begins retesting. For a small fraction of chassis, this cycle of test and repair is not the last — several cycles may be required before it finally passes.

Managing the line

The factory managers want to maximize the *throughput* of the line (good chassis built in a day) for a given labor cost. Each extra cycle of test and repair consumes labor and increases in-process inventory. So it is important to maintain high *yield* (percent product passing test the first time).

Yield may be reduced in two ways:

1. defects in the chassis, or
2. false rejects by the testers.

Obviously, the test and repair data themselves supply the answers to management's questions:

- What is the throughput and yield of the line by test station?
- What are the recurring problems: defects or false rejects?
- Which defects occur repeatedly?
- Which reject patterns occur repeatedly?

Quick response to problems is critical. It

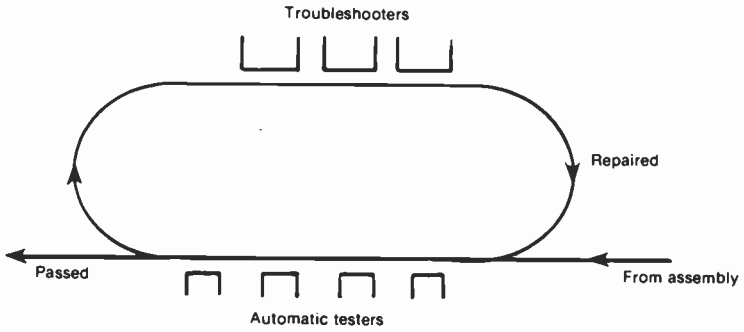

Fig. 1. Each assembled chassis passes through four automatic test stations.

is generally felt by line managers that an anlaysis of factory problems more than a few hours old often is too late to be useful.

Defect analysis for real-time supervision (DARTS)

The DARTS system is intended to automate virtually all the data collection and analysis required by line managers for the test-and-repair loop. DARTS can monitor two assembly lines simultaneously, keeping all information strictly separated by line. It is strictly "passive," as it does not directly control any manufacturing or test equipment.

DARTS monitors all test stations, receiving "pass" and detailed "reject" messages over communications lines (Fig. 2). Any repairs recorded by troubleshooters are typed into DARTS video terminals when convenient. As this information is received, it is filed both in chronological logs and by unique chassis serial number.

At any time, a manager or engineer can request reports which reflect up-to-the-minute happenings on the line. These reports are carefully organized for clarity and ease of use. Summary reports give a quick overview of the throughput and yield, broken down by production hour and individual test station as well as totalled by day and station. Detail reports are sorted so that "hotspots," such as frequently occurring test reject patterns, are found at the top. These DARTS functions are described in detail in the next section.

Functions

Potential users

The users of DARTS include the line manager, manufacturing engineers, test engineers, troubleshooters, and quality control personnel.

The line manager can receive a summary report of throughput and yield at any time of the day.

Manufacturing engineers use the detail repair report to spot frequently occurring defective components or workmanship problems. These repairs are associated with individual chassis so that a tendency for chassis to cycle repeatedly, indicating a lack of consistency between test standards and troubleshooter methods, can be easily noticed.

Test engineers use the summary yield report to spot downward trends by individual test station, while detail reports show, by test station, the most-frequently occurring reject "patterns" (a pattern is a particular series of tests failed). Questions about the detailed parametric value of certain rejects can be answered by consulting a chassis cycle report showing every test or repair associated with an individual chassis.

Troubleshooters can use the reject pattern report, which associates reject patterns with all the repairs made for them, to compile a reject "dictionary." This dictionary is useful because it combines the experience of all troubleshooters over all shifts who otherwise would not have an opportunity to share their expertise.

Quality control personnel, interested in the long-term as well as short-term analysis of repairs, can receive from DARTS a daily magnetic tape list of all repairs, coded to be compatible with the separate factory-wide defect reporting system (DRS).

Human engineering

The great variety of potential users of DARTS underscores the importance of good human engineering, that is, ease and convenience of use after a minimum of training. The system should be simple and consistent in its expectations of the user; it should clearly prompt or remind the user, accept short free-form replies, and be tolerant of errors. These aspects have been stressed within DARTS.

Most user-requested programs first prompt the user to select, for example, the assembly line of interest or specify a report time period. The user may reply in free format, with natural abbreviations for commonly occurring options. If a mistake is made, the program explains what replies are expected and gives the user another try. For the expert user who knows what the prompts will be it is possible to "anticipate" the replies, typing them in along with the command name, thus saving time.

Monitoring the testers

DARTS constantly monitors the test stations (four per assembly line). Reject messages include a list of failed tests, each accompanied by a parametric measured value. The measured value is outside minimum and maximum limits established in the test program. For convenience of users, DARTS also keeps a copy of this table of test limits and reproduces them on certain reports next to the measured value.

Monitoring the repairs

There is a video terminal on the factory floor near the test-and-repair loop which is used to enter repair descriptions written by the troubleshooters. A repair entry consists of:

1. Chassis serial number, to identify the product;

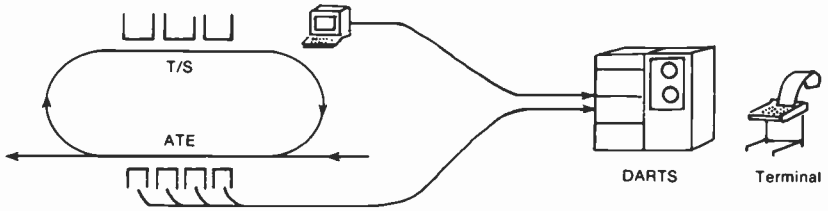

Fig. 2. DARTS monitors all test stations, receiving "pass" and detailed "reject" messages over communication lines.

2. Component name (e.g., R304, CR50, Q410); and
3. Defect code (e.g., NSOD, LO, OK) — "OK" identifies a false reject.

Tracking cycles

As data are received for a chassis, it may become clear that the chassis has started a new cycle of test and repair. This may be signalled by showing up again at test station A1 (the first) or, more generally, by appearing to reverse the normal test sequence. Cycles are stored separately, each labeled with the starting date and time of day.

Reports

DARTS reports may be requested for either of the assembly lines, and for a specified interval of time (the "report period"), usually from the start of production until the present.

The *Test* report consists of a two-page summary, one for current and one for all products. Each page gives, for each test station and production hour, the total chassis tested (including multiple counts for retests), total chassis rejected, and the computed percentage yield. Also computed are the totals and yields by test station and for the whole line. Optionally, the user can request, in addition to the summaries, a list of all test rejects in chronological order. An even more voluminous option prints all "pass" messages as well as rejects.

The *Pattern* report shows, for each test station, which "patterns" (distinct lists of failed tests) occurred and how often, with the more frequently occurring printed first. Along with each pattern are shown all associated repairs, that is, those entered during the same cycle for the chassis that failed with that pattern.

The *Repair* report consists of two parts, one for component repairs and one for workmanship repairs. In each part, the repair codes are shown across the page as headers to columns and down the page are listed the components associated with the repair. The components are sorted with most frequently repaired at the top.

The chassis *Cycles* report shows the complete history on file for any of a list of chassis (or for all at once).

The *DRSTAP* program writes a list of all repairs to a magnetic tape. This is for use in the separate factory-wide defect reporting system (DRS).

Susie McClary, top, operates the General Automation 16/45 minicomputer console. Sue Dausch, bottom, operates the defect entry terminal.

Hardware and software

Minicomputer system

DARTS is based on the General Automation 16/45 minicomputer with 32-k words random access memory (RAM). The central processing unit (CPU) was chosen for spare parts and maintenance compatibility with the automatic testers. Mass memory is a 10-M byte disk with two platters, one fixed and one in a removable cartridge. One platter is dedicated to storage of programs, both in source and binary; the other is partitioned into files for data storage. Storage is adequate for about two and a half days' normal production for two lines.

The user and operator console is a DECwriter III, operating at 1200 Baud. A 9-track 800-bpi magnetic tape drive is used for program release and writing DRS tapes. Communication with the testers and videos is via an 8-channel asynchronous communications multiplexor with line adaptor for 20-mA current-loop operation, at 9600 Baud.

The total hardware cost for DARTS (including spares) is about $70,000. A team of four specified, designed, and implemented the system in one year.

RCA extensions for event-driven control

The DARTS software runs within the GA RTOS operating system, which was used virtually unmodified. Programs were written almost entirely in FLECS, a structured-control preprocessor for FORTRAN.

In one area, RTOS was inadequate. It is strictly a schedule-driven operating system, and intertask communication was needed. Therefore, three general facilities were built, providing intertask synchronization, message queues, and task-independent "core blocks." These event-driven facilities are imbedded within RTOS, managed by a high-priority core-resident program.

Communications

DARTS monitors four test minicomputers (two on each line) over serial communications lines. Since DARTS is located, for the convenience of managers, in an office area, the cables are several hundred feet long. Operating with 20-mA current loop successfully eliminated noise problems even in a factory with high environmental electrical noise.

The DARTS video terminals are Hazeltine Modular Ones, operated in FORMAT 2 mode. Communication is at 9600 Baud to provide quick response for the users.

Operations

DARTS requires a part-time trained operator to perform such functions as startup and shutdown, initializing data files, maintaining parametric tables (such as legal defect codes), installing new software releases, regular hardware maintenance, and responding to unexpected problems. A detailed "DARTS Operations Guide" spells out these duties.

Summary

DARTS has successfully automated the collection and analysis of test and repair data on the chassis assembly line. The response of the line managers and engineers has been positive. In many cases the summary reports have led to an early recognition of assembly and testing problems. The detail reports are particularly useful in tracking down these problems. The DARTS-generated throughput and yield summaries have been accepted as the official daily production report. Without a system such as DARTS, non-productive labor must be used, but cannot do the job as quickly or thoroughly. The replication cost of DARTS is less than $50,000 (spare equipment adds $20,000). Benefits are not only improved understanding and control of the line, but also labor reduction. Notice has been taken of DARTS' impact, and other manufacturing groups within RCA are planning to install similar systems.

Acknowledgments

The RCA Laboratories' DARTS team has included many people in addition to the authors. Allen Korenjak supervised; programming was done by Arthur Anton, G. David Ripley, Stuart Golin, Eleanore Wells, and H. Garrett Long. Eleanore Wells, in addition, shouldered much of the operations and debugging burden at the Laboratories' site, and contributed to training of CE personnel.

We wish to acknowledge particularly the cooperation and help of many people at Consumer Electronics. At Bloomington, especially, Bob Fein, John Keith, Bruce Schaffer, Ed Curtis, Ken Brooks, and Tim Nisley. At Indianapolis, especially, Steve Race, Ben Borman, Art Kaiman, Dick Sunshine, and Larry Turpin.

Tom Stiller, standing, and Henry Baird helped to design and implement the DARTS system.

Henry Baird is a member of the Technical Staff, Automation Systems Research Group. He has worked on computer-aided design of ICs, LSI circuit mask artwork verification, factory modelling, and real-time assembly-time monitoring. Future work will concentrate on programmable automation, such as automatic visual inspection and robot vision.

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Tom Stiller, a Fellow of RCA Laboratories, has worked with the non-numeric aspects of computing for the last 14 years — work ranging from the development of function-evaluation subroutines and general-service programs up to multiprogramming operating systems and simulation of new computers prior to their manufacture.

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ERIC: a process monitoring and control system

Reduction in labor costs and increased yields show that ERIC is pioneering the building of quality into the epitaxial wafers used for power products.

Abstract: *A computer-based process control system called ERIC is used at the Mountaintop, Pa., RCA Power Semiconductor Plant. The system monitors products coming from a complex epitaxial growth process, calculates changes in the process control parameters, and feeds these changes back to personnel controlling the epitaxial reactors. Today the system provides*: 1. *disciplined data collection, sampling, and validation*; 2. *consistency of process control*; 3. *an accurate accessible historical data base*; *and* 4. *numerous management and engineering reports. Areas requiring further work are*: 1. *improved input data accuracy*; 2. *improved control algorithm as process understanding grows*; *and* 3. *quantification of resulting yield improvement. The promise is lower cost for RCA's power products through better yield, quality, and understanding.*

Why focus on quality?

Profit is the return on an investment in quality. The story of Japanese industry is known to all. None can dispute the success Japanese industry enjoys managing with quality as a prime objective.

- Quality can be tested into product but at the cost of reduced yield.
- Quality can be designed into product but there is a propensity for subsequently changing design rules to optimize yield at the expense of quality.
- Quality can be built into product by process control. There is no ambiguity about the merits of this approach.

Process control improves both yield and reliability.

Figure 1 illustrates that yield improvement leads to an increase in throughput and reduction in manufacturing cost. In a demand market, the increase in throughput immediately translates to margin and greater market penetration. Reliability improvement enhances RCA's reputation again leading to greater market penetration.

What are ERIC and PMC?

ERIC is a process control system used in the manufacture of power transistors. It uses the PMC computer system[1] as a basic component. The system provides a means of improving and deskilling the production of silicon wafers by integrating, in a process control algorithm, the experience of many process engineers. Silicon layers a few

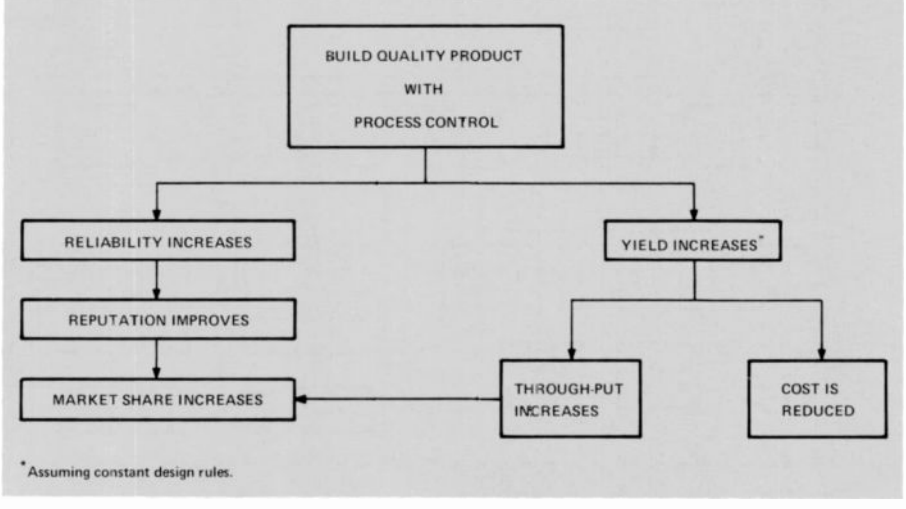

Fig. 1. Yield improvement leads to an increase in throughput and reduction in manufacturing cost.

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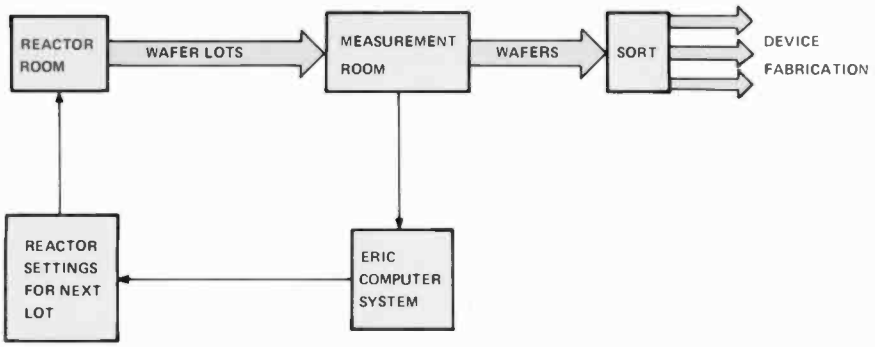

Fig. 2. Product and information flow.

thousandths of an inch thick are grown from gasses as they pass over wafer substrates. Power transistors are then formed from these layers by subsequent diffusion processes. The dopant concentration and thickness of these layers are critical parameters controlling the gain, breakdown voltage, and energy dissipating capability of the finished transistor. These "quality" characteristics result from the proper timing, temperature, and flow of the gasses during epitaxial layer growth. ERIC determines for each epitaxial reactor and wafer type what the timing and flow should be for a given temperature based on the history of previous processing results. To do this ERIC:

- Collects measured data characterizing epitaxial wafers by lot.
- Validates these data in real time providing a means of error correction.
- Stores the data.
- Uses the data to control subsequent processing.
- Provides reports covering quality, production performance, process "recipes," and process control capability.

How does ERIC improve quality?

The flow of product and information is shown in Fig. 2. Epitaxial wafers are batch produced in the reactor room. These batches or lots of wafers are measured for layer thickness, and resistivity (dopant concentration) and then sorted into categories for subsequent device fabrication. The measurements are taken in a controlled way by the ERIC computer system and used to produce a "recipe" for the next batch.

The system used to collect and analyze these data is shown in Figs. 3 through 6. The sampling of data is controlled by the computer. It specifies to the operators which wafers to measure and controls how many measurements to make, and at what location on each wafer the measurement is to be conducted.

When the next batch of wafers is ready for processing, the operator requests from ERIC a run formation document shown in Fig. 7. Any changes in reactor control settings from the last run are indicated by "*". This run form is produced by an algorithm which currently uses

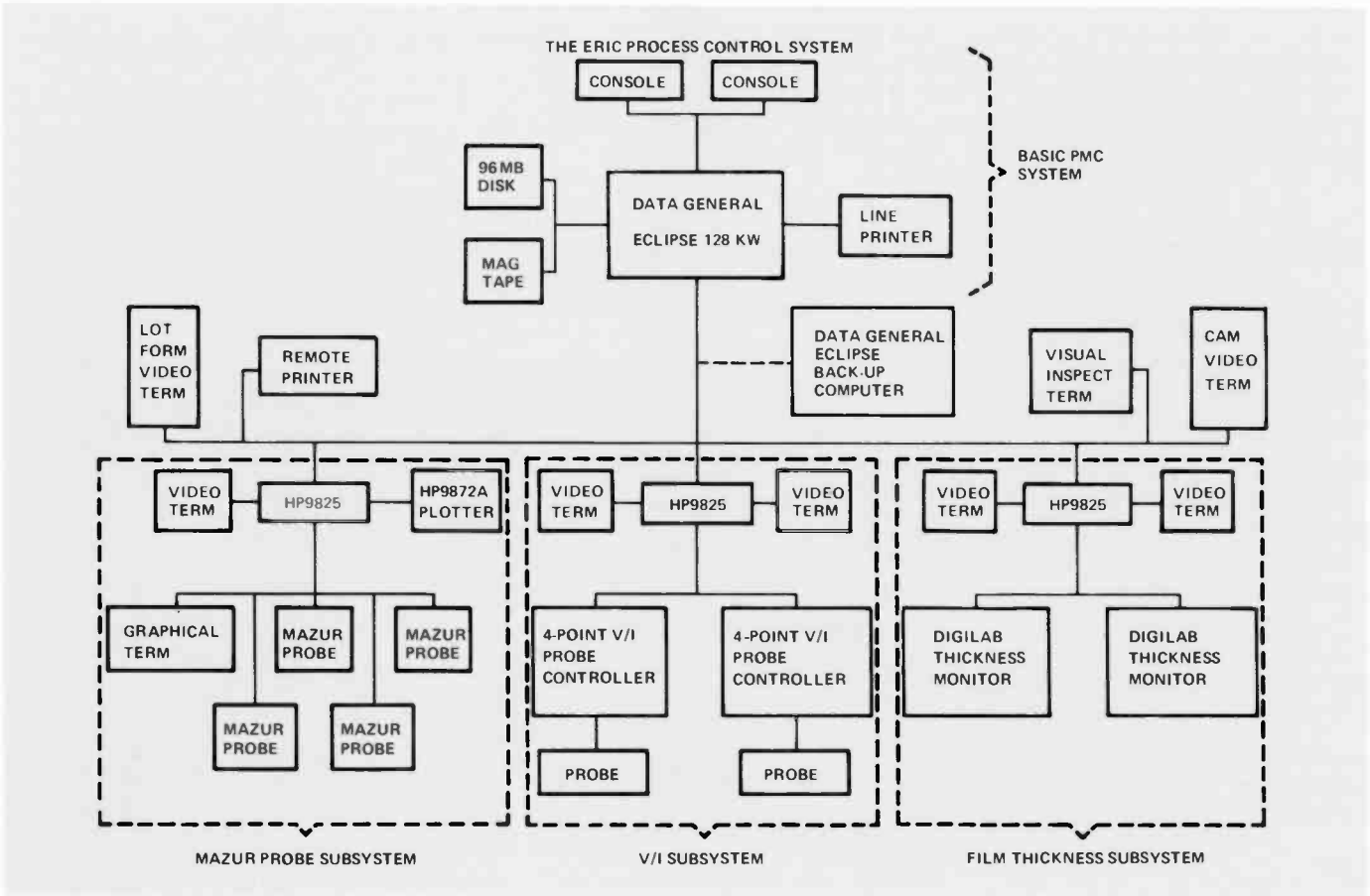

Fig. 3. The ERIC basic PMC system.

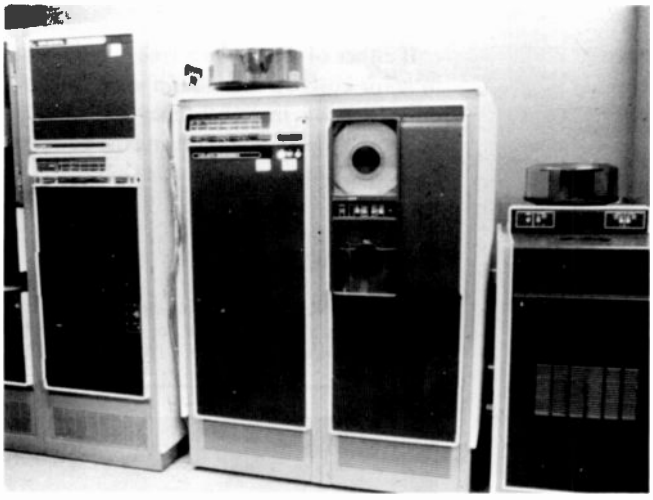

Fig. 4. Management computer for ERIC. The Data General Eclipse Computer and its backup are shown here with the 96MB disk. These computers use the PMC software system to service the subsystems shown in Figs. 5 and 6.

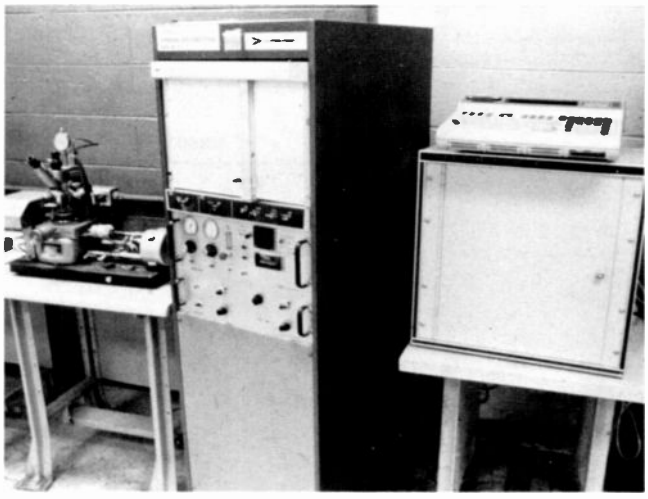

Fig. 5. Mazur probe subsystem. The probe is at left with the controller at center and HP9825 microprocessor at right. This subsystem gathers data automatically to determine the resistivity (dopant concentration) as a function of depth in the epitaxial wafer.

Fig. 6. Four point V/I probe subsystem. The probe is at left with its controller at center followed by the HP 9825 microprocessor and video terminal. This subsystem gathers resistivity data from prescribed positions on each wafer following a prescribed sampling plan.

measurements taken from the last five runs with the most recent more heavily weighted.

Results from ERIC's use

The ERIC system has been in production use since August 1, 1979. Initial engineering tests prior to production indicated that the control algorithm was sufficiently accurate to use in production, if computer generated warning indicators were invoked when control setting changes exceeded certain limits. With these in effect, the system now gathers data and predicts control for about 60 percent of the Solid State Division's wafer production.

```
                              .RUN FORMATION

TYPE WO1044  REACTOR V11R RUN 63  CONTROL # 133.    SHIFT  3   8/15/79

TARGET THICKNESS            4.50
EPI REACTOR GROWTH RATE     .064                      SUGGESTED   ACTUAL
RECOMMENDED GROWTH TIME     69.2   WAFER LOADING  5,5,5,5,0  5,5,5,5,0  P RUN
COMMENTS: C
-----------------------------REACTOR PROGRAM-----------------------------
SEQ    CYCLE          TIME  HCL  DOPANT  INJECT SICL4   H2     BK-PR DIL-PR
1   H2 PURGE          5.0                              12/3
2   RF PREHEAT        15.0                              "
3   HCL ETCH          10.0  10.0                        "
4   DELAY  1          2.0          995.0          10.0  "      8.0   12.0
5   DOPE  1   (N)     5.0 *                             "
6   DELAY  2          2.0          925.0*               "
7   DOPE  2   (N)     19.2*                             "
8   DELAY  3          2.0          310.0                "
9   DOPE  3   (N)     19.2*                             "
10  DELAY  4          2.0          775.0                "      8.0   12.0
11  DOPE  4   (P)     25.8*                             "
12  DELAY             .5
13  DELAY             15.0
```

Fig. 7. Run formation instructions are furnished by the ERIC system to the operators setting up the reactors.

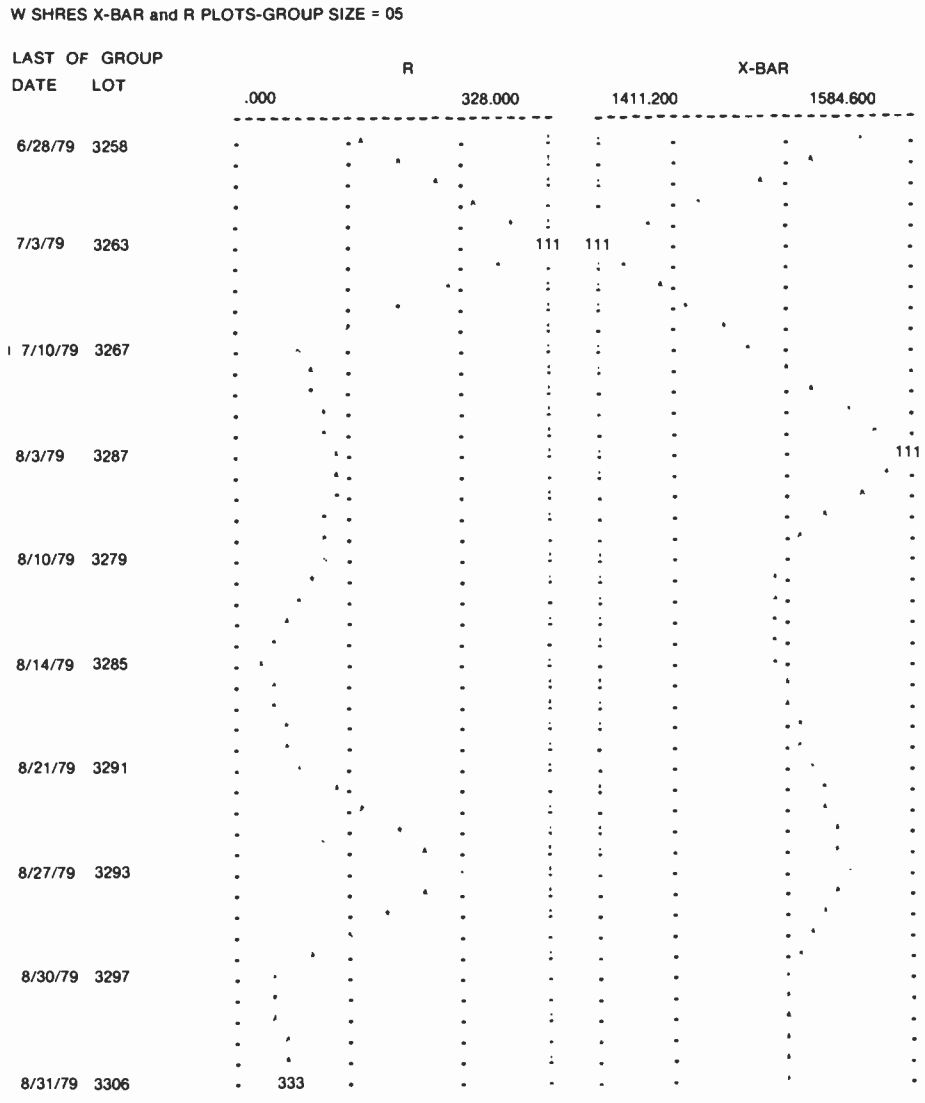

Fig. 8. Control charts are produced by ERIC.

The results relative to control, yield, etc., are being evaluated to form a basis for further refinement of the control algorithm. Computer generated control charts, as illustrated in Fig. 8, are used to monitor reactor performance.

Conclusion

An epitaxial process control system with human intervention (non-closed loop) is operating in a manufacturing environment. Production data are being analyzed to determine if:

1. The currently used algorithm controls critical device characteristics better than engineers. (Initial results say "Yes.")

2. Changes in the algorithm can further improve control. (After only two iterations this has got to be "yes.")

If either of the above is true, a reduction in labor cost, an increase in yield, and an improvement in consistency (reliability) will result. ERIC is pioneering the building of quality into semiconductor products.

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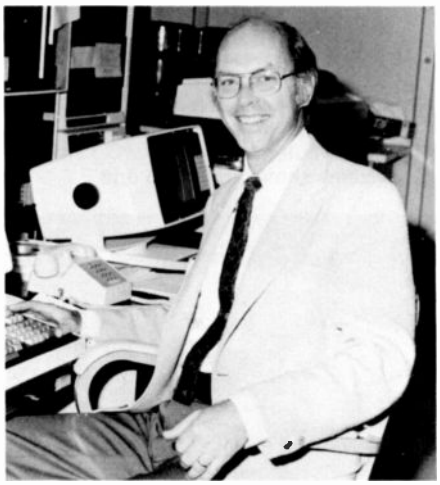

John Gaylord joined RCA in 1952 and worked for the ensuing eleven years as engineer, engineering leader, and manager of small power tube design at Lancaster, Pa. Mr. Gaylord moved to the David Sarnoff Research Center in 1963 developing scanning electron microscopy techniques for semiconductor failure analysis. Three years later he moved to the Solid State Division. As group leader and manager of Power Transistor Design he was responsible for the development of much of RCA's current product line of epitaxial base and high voltage switching transistors. In 1971 he moved to Solid State Technology Center as manager of Advanced Power Semiconductor Development.

Five years ago Mr. Gaylord initiated in the Solid State Technology Center a program to assist RCA manufacturing by developing computer-based systems for Process Monitoring and Control. He is currently managing this activity and is also manager of Computer Aided Manufacturing for the Solid State Division.

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D.C. Bowen|J.M. Shukal

Software reliability

Software reliability is the probability of "satisfactory" operation for a specified time in a specified environment.

Abstract: *This paper provides an overview of software reliability today. The conceptual differences between hardware and software reliability disciplines are discussed. The current models for prediction of software reliability are summarized. Techniques commonly used to improve software reliability are identified.*

A review of software reliability issues, addressed to an engineering community that is still preponderantly non-software in orientation and experience, naturally lends itself to a two-part treatment.

First, a comparison is made of concepts such as failure modes and failure consequences as they relate to both hardware and software; for without a good understanding of how and why things fail no credible reliability assessment is possible. Beyond the definitions of the most basic terms, however, the conventional wisdom of hardware reliability is of little or no use to the software engineer.

Second, an attempt has been made to summarize the various theories that have been proposed for reliability modeling of software. While some of these approaches have been supported by isolated efforts to gather data, others have not, and all have fallen short of widespread acceptance or use. It is worth noting that the large quantities of high quality data of the type needed to truly substantiate any reliability model are inherently much more difficult to acquire for software than for hardware. Some enhancement of software reliability may be achieved by the imposition of good engineering practices throughout the software development and verification cycle.

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Definitions of terms

The authors have elected to use the following definitions that have already been published and are believed to have found general acceptance in the technical community. Beyond these basic definitions, however, there is little common ground to be shared by the disciplines of software and hardware reliability.

Software reliability is the probability of "satisfactory" operation for a specified time in a specified environment.

Software failure rate is equal to the number of applicable software failures in a time interval divided by the time interval.

A *software failure* is any occurrence attributable to software in which the system did not meet its performance requirements.

While software reliability and software failure rate, as defined above, are specifically applicable to real-time software, simple equivalents for batch processing would replace the parameter of time with one for number of transactions.

Software/hardware comparisons

Failure modes

Table I lists six failure causes, two of which are shared by software and hardware, two of which are unique to software, and two of which are unique to hardware. For simplicity, analog-type hardware is assumed. Large-scale digital circuitry and firmware share some of the software-unique failures as well as those that are traditionally associated with hardware.

A brief description of each failure mode follows:

- *Part Failure* — Self-explanatory. May be random or pattern in nature.
- *Workmanship Failure* — Self-explanatory. May also be random or pattern.
- *Coding Errors* — These include errors made by the programmer in the final stage of software implementation. Typical examples are incorrect statements, misspelled names, and missing symbols. Coding errors are frequently limited to a single line of code.
- *Logic Errors* — These include incorrect coding of algorithms, misinterpretation of design statements, and unsuccessful attempts to modify algorithms to simplify coding or increase execution speed as typical examples. Logic errors are usually confined to a relatively small subset of the total lines of code.
- *Design and Specification Failures* — "Design" and "specification" are commonly used in software to describe progressively higher levels of design in the system hierarchy. Hardware equivalents would be the component and critical item specifications, respectively; or the critical item and prime item specifications, respectively. In very complex systems, hardware or software, there may be more than the two layers of documentation used for this simplified comparison.

In software, "design" documentation concerns itself with detailed implementation of allocated software functions within a computer program and within

Table I. Software/hardware failure causes.

Failure Mode	*Consequences of Failure*	
	Software	*Hardware*
Part failure	N/A	Small
Workmanship	N/A	Small
Coding error	Trivial	N/A
Logic error	Small-Med.	N/A
Design problem	Med.-Large	Medium
Specification problem	Large-Critical	Large

the system-wide constraints imposed upon it. "Specification" includes such top-level design considerations as architecture, system-wide timing constraints, allocation of functional requirements, and available memory to major subsystems (or computer programs), a definition of the hardware environment, and communications protocols to be used by all subsystems.

Hardware analogies are the "black box" design and the block diagram that defines all internal interfaces and allocates functional requirements to the "black box" level.

Failure consequences

In addition to listing the more common failure modes, Table I represents an attempt to qualitatively identify the consequences of failure modes for both software and hardware as they relate to the cost and time required to fix.* As should be expected, the first four failure modes are generally of much lesser consequence than are those which reveal deficiencies in the design or specification, although pattern failures in hardware are occasionally costly to identify and fix.

Of particular interest is the relatively greater severity to software of failures that are attributable to design and/or specification deficiencies. These types of deficiencies, when discovered late in the software development cycle, can lead to significant program re-direction and costly overruns. High among the cost and schedule drivers are the massive code changes that may be required, the ripple effect of any major change into other areas of the system software that had previously been working well, and fundamental software/hardware incompatibilities, such as lack of sufficient memory and inadequate speed of execution.

*Not to be confused with the failure mode "effects" or "criticality" which are intended to convey the impact of failures on system operational use. Failure of a 10-cent part, or an undetected coding error in a single line of code can, conceivably, cause catastrophic loss of operational capability while their consequences in terms of repair time and cost are usually trivial.

Software failure rate trends

The expression "failure rate" came from the hardware world and literally describes a typical event where a part works well initially, and at some arbitrary later time ceases to work as it should.

In software, a more appropriate expression would be "error detection rate." Software itself cannot fail, but an error that has always resided in the software may take weeks, months, or even years to detect. Intuitively, it would seem to follow that, given a fixed number of errors in software at the start of actual use, as errors are initially detected and removed, the total number of errors remaining would be reduced, leading to a lower rate of detection. This is a description of exponential decay and logically leads to an assumption that it should be possible to fit a curve to observed data and project what failure rate should be experienced by the system at a later point in time. In fact, however, this is not the case since there is yet another important difference between software and hardware failures.

In hardware, the failed part is usually relatively easy to isolate and replace. In software, correction of other than the most trivial coding errors always carries with it the risk of inadvertently injecting a whole new set of errors into the software, some of which may not be immediately detected. Therefore, during the error removal process, the total of latent errors (detected and undetected) in the software does not remain constant but increases monotonically. The general effect, as a function of time, is shown in Fig. 1. The failure rate curve periodically rises as new errors, introduced during the debugging process, are detected and removed. When the software contains no serious design or specification flaws, it can be expected to eventually achieve an acceptably low failure rate. Hypothetically, there is no absolute lower bound to software failure rate.

Techniques and models for the prediction of software reliability

For more than fifteen years, attempts have been made to develop analytical models which could be used to quantify software reliability. Mathematical models are used to predict reliability on the basis of parameters previously known or evaluated during the integration and test phase. Most models are based on error rate and elapsed testing time. These models can be broken down into general categories or types.

The exponential models of Shooman and Musa bear the closest resemblance to those currently used in the hardware environment (see previous discussion). They assume that the number of errors in the system remains constant, i.e., total errors minus those found equal the number of errors left in the system.

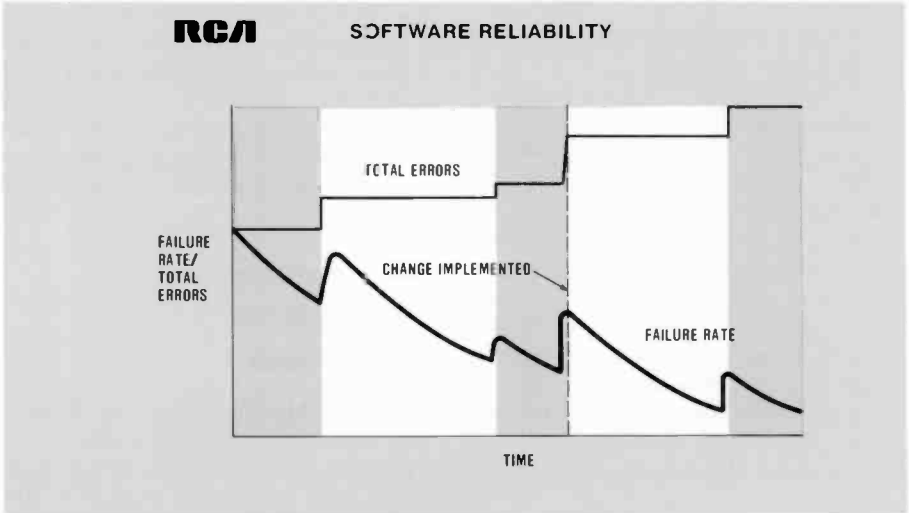

Fig. 1. The failure rate, shown as a function of time, rises periodically as new errors are introduced during debugging.

Table II. Techniques for prediction.

Type	*Developer*	*Predicts*	*Comment*
• Complexity/size factor	Motley/Brooks (IBM) Halstead	Initial error content	May be used prior to code Useful on large data samples
• Exponential	Shooman Musa	MTTF Relation between calendar and execution time Initial error content Probable time to next failure	Typical hardware model
• Execution time theory	Nelson Shooman micromodel	Reliability Failure rate	Computer center environment Stress on software related to processor time utilized
• Poisson	Jelinski/Moranda geometric Goel/Okumoto Schneidewind	Failure rate	"Find" and "fix" data included
• Bayesian	Littlewood/Verrall	Reliability	Errors not removed with certainty
	Goel/Okumoto	Expected number of errors Probable time to next failure	Reliability related to past performance
• Markov	Littlewood Trivedi/Shooman	Reliability MTTF Availability	Error correction time a factor

Models based on execution time theory like the Shooman micromodel and Nelson's model prove to be useful primarily in the computer center environment They are based on the assumption that the processor time utilized in executing the program is the best practical measure for characterizing stress placed on the software. The number of errors in the system is then related to the error removal rate disregarding variations in inputs.

Models exist which relate factors of complexity or size to software reliability as Motley and Brooks' (IBM) model and Halstead's model which shows the relationship of reliability to the number of operators and operands in a program. Variations occur based on programming language used. These models may be implemented prior to development of code, but are appropriate for use only on large samples of data.

The Bayesian techniques as developed by Littlewood-Verrall and Goel-Okumoto relate to software reliability in the operational environment. In these stochastic models, periods of error-free execution cause reliability to improve, and conversely, if failures are sufficiently frequent, the reliability is predicted to get progressively worse. Unlike most of the models considered here, errors are not assumed to be removed with certainty. These models attempt to quantify the probabilistic nature of a programmer's actions during the debug phase.

Nonhomogeneous Poisson models include both "find" and "fix" error data as in the Jelinski-Moranda Geometric Poisson model developed by Goel and Okumoto and Schneidewind. The models assume a constant error detection rate.

Littlewood and Trivedi-Shooman developed Markov models in which error correction time is introduced as a factor. An assumption here is that a program can be decomposed into "R"number of subprograms and execution proceeds by switching among them according to a Markov process. A summary of these models is presented in Table II. A myriad of other models can be found in the literature; however, no consensus has been achieved in the software community.

Shortcomings of present techniques

The models that exist today exhibit drawbacks which limit their applicability. "There is no single metric or reliability model which can give a useful reliability evaluation or estimation from a theoretical viewpoint."[1]

Techniques and models frequently are limited to a particular environment or phase of development and are not applicable through the total life cycle.

The assumptions upon which the models discussed previously are based have not been rigorously verified. The techniques lack a base of statistics proving their effectiveness. Sufficient data substantiating their effectiveness on multiple projects are lacking, and no confidence limits have been established to aid in the interpretation of results obtained.

The number of techniques available gives rise to the need for comparative studies to determine relative worth of the various techniques. However, the single greatest obstacle to overcome for encouraging more widespread use of reliability calculations is the inconsistent and incomplete data available. Data are difficult to collect due to variations in software operational profiles, classification or privacy of data, and lack of motivation by individuals responsible for reporting errors. Various definitions of reliability require different inputs.

Why predict?

Software is taking a larger proportion of system development dollars each year. The cost of maintaining this software over its life is several times the cost of development. It is obvious why the prediction of software reliability is desirable. Possible fringe benefits from good reliability estimation are its use as an evaluation tool for monitoring software engineering, monitoring project status, scheduling, and for forecasting of personnel requirements. Reliability predictions can serve as a basis

for determining the appropriate time to terminate system testing and can serve as a handy rule of thumb for initiation of formal configuration management of code. Systems Engineering receives vital feedback of their efforts from the data, and cost tradeoffs can be made for future enhancements, some of which might reduce the system life cycle cost.

Means of improving reliability

There are many accepted techniques for improving software reliability. These are based on certain assumptions. Specifically, reduction in the complexity of the design will reduce the number of errors. By freezing the design early and providing clear, complete high-level specifications giving performance requirements for the system, guidance is given to the programmmer when it is most needed — early in the development cycle.

The later in the development cycle a change or problem is encountered, the more costly it is to correct. Early and complete design reviews by technically competent individuals and subsequent control of changes, especially in the critical area of interfaces, help reduce mistakes that frequently prove to be the costliest and most difficult to fix. At this time, establishment of reserves in areas like memory and I/O channels help reduce impact of changes required late in the development cycle or for system enhancements.

The early start of verification and validation is recommended to detect changes as early in the development cycle as possible to help reduce their impact. Throughout the entire development cycle, the use of software tools helps reduce the number of errors through the use of special preprocessors, compilers, link editors, etc.

The prudent selection of one or more programming languages providing the "best-fit" for the application reduces the number of errors in a program. The use of such well-known techniques of development as structured programming and the enforcement of standards and conventions not only reduces errors early in the development cycle but makes maintenance of software easier.

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Conclusion

During the past, many reliability models have been developed. The task at hand is to accumulate reliable data to use in the evaluation of the various techniques. Until a conscientious effort is made by industry, only limited advancement toward the goal of formalizing software reliability estimation will be achieved.

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L.J. Gallace

Predicting solid-state device reliability

How do you estimate failure rates when little or no data are available?

Abstract: *Accelerated life tests are commonly used to predict device reliability. This method often assumes an activation energy of 1.1 eV, which may not always be valid. This paper tells how to go about making such tests, what assumptions can be made about them, and gives results of tests showing activation energies for a number of product lines and failure modes.*

The prediction of reliability is important to the equipment manufacturer because it permits him to determine warranty limits when extensive reliability data are not available. Today, when many systems are changing from mechanical to electronic operation, these predictions are especially useful and necessary because they allow the manufacturer to determine the expected performance and life of newly designed systems that do not yet have actual reliability data available. Expected performance predictions covering a period of five years and based on known failure mechanisms are usually required. Designers also use the predicted data in developmental work to eliminate guesswork and to provide expected confidence levels for new system design.

Predicting reliability

The assignment of a numerical reliability figure to a product implies achievement of that figure. Classically, such achievement has been demonstrated through the use of a statistically designed accelerated test that provides an objective conclusion regarding achievement along with a degree of error. Accelerated tests are used for two purposes:

1. As a measure of lot-to-lot variation of either quality or reliability of solid-state devices; and
2. As a means of predicting application failure rates by the use of life tests.

Tests whose primary purpose is to demonstrate equipment reliability can be sometimes reduced to proper division of the time-temperature domain with an Arrhenius (log failure rate vs. the reciprocal of temperature) plot. Data taken at high temperatures are then extrapolated on this straight-line plot to provide failure data at lower temperatures. Often an assumed activation energy of 1 to 1.1 eV, which is standard for silicon planar technology, is used for prediction in this domain.

This analysis of the reliability-prediction procedure addresses the two issues of lot quality and reliability control. Failure-rate prediction from accelerated tests is based on the assumption that one can predict life or extrapolate data over time when data do not exist or are economically impossible to generate. The validity of this approach rests on the assumption that there is only one mechanism of failure and that no infant mortality is present in the failure distribution. Infant-mortality failures, which may be packaging- and/or chip-related, generally occur in the processes at different periods of time and, to a large extent, independently; that is, this class of failure has some statistical independence. In the application environment, where the physical and electrical environments may be changing (time variable environment), failure rates can be predicted by:

1. Testing the devices in the actual or simulated environment and experimentally determining the failure rate. This method is very expensive and time consuming.
2. Using accelerated tests based on the performance of a device after a few cycles in a simulated environment. Development of the tests is not easy, but once they are developed, they can be performed in a very short time.
3. Determining the steady-state thermal environment that produced the same failure rate as the actual variable environment.

Therefore, the interpretation of the essence of overstress in an accelerated test requires a knowledge of:

1. The predominant failure mode under rated stress conditions;
2. The environment that excites that failure mode; and
3. The qualitative relationship between the level of stress in the environment and the rate of occurrence of the failure.

When this information is known, the problem of measuring reliability can be attacked from three points of view:

1. Measurement of reliability in applications;

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Typical accelerated aging tests

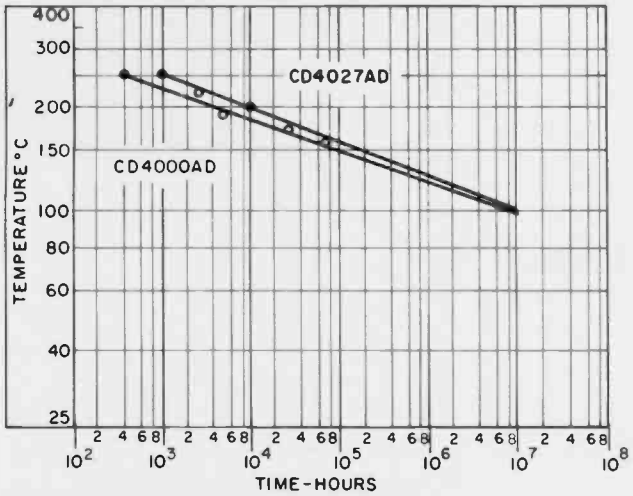

Fig. 1. Two digital ICs, tested via constant-stress method, gave activation energies of 1.123 and 1.227 eV.

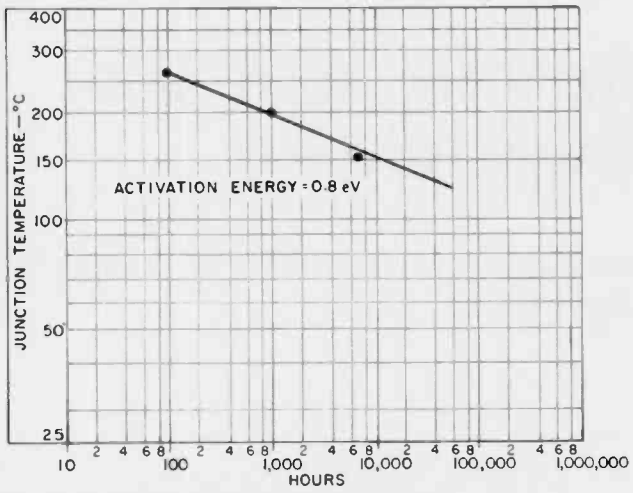

Fig. 2. High-voltage silicon power transistor shows beta degradation with life. Activation energy here is 0.8 eV.

2. Measurement by means of acceptance tests used to determine reliability; and

3. Measurement by means of tests used to control manufacturing processes so that factors causing failure mechanisms can be eliminated in that step.

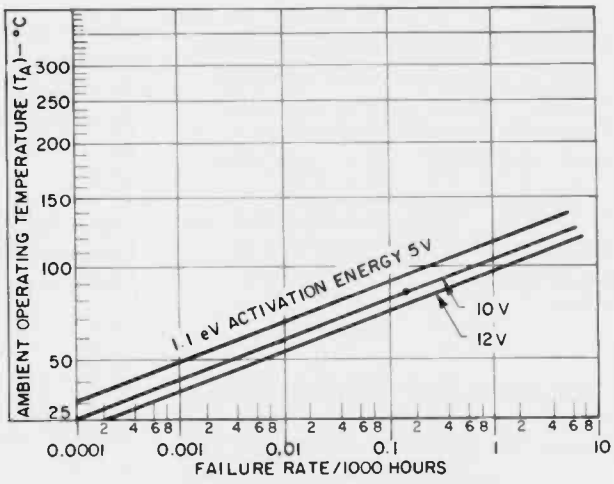

Fig. 3. COS/MOS devices show failure-rate voltage-acceleration based on 1.1-eV activation energy.

Measuring reliability

Measurement for applications

Using tests, instead of the actual application, may produce errors. For example, test-equipment failures may degrade units; testing failure definitions may be tighter than those causing failure in equipment; and power, voltage, and thermal stresses may be more severe than those met in the actual application. The test must not measure the performance of the circuit in which the device is used, but rather measure device parameter stability.

Measurement for acceptance

In measuring reliability by means of acceptance tests and incoming quality tests, the problems of sample sizes, failure definition, stress levels, test time, and previous product history must be considered. After the incoming quality-control system has been running and failures do occur, all of these factors tend to be compromised in some way. If 100 units are tested and product acceptance is based on one failure and the product rejection on two failures, two different decisions are being made about product generated by identical processes. The commercial issues would override that kind of a decision, and one of the other factors, such as increased sample size or previous product history, would be weighted more than the actual failure criteria when determining whether to accept or reject the lot in which the failure occurred. Of course, this method involves a great number of engineering and quality personnel in what should be routine incoming quality-control inspection.

Measurement for control

Measuring reliability for the purpose of interceding in the manufacturing process is considered to be the most effective way of attaining uniform lot-to-lot reliability. The Solid State Division's real-time controls are an attempt to do this for known failure mechanisms. Real-time control information is used immediately after it is generated to make corrections in the process. In contrast, information generated by the incoming quality-control tests for the customer is after-the-fact data and can only be used in a general way to make improvements in the process. Solid State Division measurements for control are centered around developing the real-time tests.

Reducing field failure rates

At this time it is questionable whether incoming quality-control life tests performed by customers can actually reduce failure rates to the levels they desire. Experience has shown that neither the tightening of acceptance quality levels (AQLs) nor lot stress sampling tests can

have much impact on reducing failure rates, except where the reliability of product is questionable. It has become very difficult to use sampling tests to reduce the failure rate of a device that has a failure rate less than one percent/1000 hours at a maximum-rated junction temperature of 150°C. The screening or burn-in of commercial product is not being advocated; however, it must be understood that there is a limit to acceptance sampling, and that eventually only 100 percent testing becomes feasible.

Determining the activation energy

The use of a 1- to 1.1-eV activation energy to predict reliability when no data exist is a good assumption based on data generated in the industry. However, this activation energy cannot be used for all products and all types because it is structure- and technology-dependent as well as process-dependent. Before an activation energy is assumed, tests must be performed at various temperatures and the proper statistical regression applied, as in Figs. 1-3.

Care must be taken not to assume the Arrhenius relationship by the use of accelerated tests that produce the same failure mechanism at both accelerated and rated temperatures. The same failure mechanism can occur at different temperatures, but for different failure causes, and still show identical activation energies. This phenomenon will still appear as a straight-line plot on Arrhenius paper. However, the failures that occur at the higher temperature, although they look like the same mechanism as those at the rated temperature, will never be induced until a certain critical temperature is reached. As long as the devices in the lot operate below this temperature, less failures will occur. Therefore, any prediction work done with results gathered above the critical temperature will grossly overestimate the failure rate in comparison to predictions made at temperatures below the critical temperature.

Table I shows a number of RCA product lines, the life test applied to each line, and the activation energies determined.

An accelerated aging test based on temperature as the sole accelerating means can be developed with the aid of an Arrhenius plot. Kinetic studies that describe how reaction rates vary with temperature are used to supply several points at the higher temperature where material degrades more rapidly. The straight-line plot is then interpolated to normal temperatures to predict service life.

Arrhenius postulated that a certain minimum amount of activation energy is required for reactions to take place; in terms of components, this means that a fixed amount of energy is required to cause a component to fail. He also pointed out that reaction rates are based on temperature parameters alone. However, studies conducted at high temperatures may miss component failure mechanisms that occur only at low temperatures. (Although these types of failures are not common, they have been identified.)

Table I. Product lines and activation energies.

Type	*Life test*	*Activation energy (eV)*
COS/MOS	Bias	1.123 to 1.227
Linear IC, gold chip	Operating	1.51
Power transistor	Storage	0.50
	Power thermal cycle	0.25
High-voltage power transistor	Operating	0.80
RF power transistor	Operating	1.01

Conclusion

With the help of the Arrhenius relationship, failure rates can be estimated under conditions where little or no data are available, provided the proper experiments and analysis of data have been performed. Predicting system reliability from predictions of component failure rates is not simple; however, the component failure rates can be a great aid in designing reliable systems.

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Larry Gallace joined the RCA Solid State Division in 1958, and has worked predominantly in the area of reliability engineering. In 1971, he became project leader with responsibility for the reliability evaluation of a broad range of power devices; in 1972, he was appointed Manager of the Reliability Engineering Laboratory for all solid-state devices. In 1979, he was made Manager, Quality and Reliability, Integrated Circuits, and later that same year, Director, Quality and Reliability Assurance for all Solid State Division products.

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High reliability through chip complexity

Computer-aided design tools, extensive chip testing and reliable chip technology enable LSI chips to make significant contributions to system reliability.

Abstract: *Larger, more complex chips are being developed with more gates of logic per area. Data indicate that these larger chips give fewer failures per gate. The use of computer-aided design tools such as programs for chip layout and test is described. Examples of CMOS chips made at RCA are discussed as well as the techniques used for reliable design.*

The semiconductor industry is moving toward larger chips, just as it has been doing for twenty years now (Fig. 1). Memory is the pacing element. The architectural and design problems associated with building a larger memory are relatively straight-forward. Microprocessors lag slightly because the architectural and design options for a general purpose programmable system are not nearly as tractable. However, microprocessors and their peripheral controllers are now available with over 20,000 gates on a single chip. These devices are the result of design teams working for more than a year to pack the required logic on the smallest possible chip and are subject to significant rework, missed schedules and unanticipated logic changes. Ultimately these high volume large chips are perfected as a result of extended interaction with the user community, but the crises and delays encountered along the way often leave a residue of distrust for large chip microelectronics.

Rome Air Development Center (RADC) issues MIL-HDBK-217, which provides failure rate models for electronic equipment. They reflected this general concern for the reliability of large logic chips in their 1976 issue and tempered it in 1979. Using their model (Fig. 2), the failure rate for a model system consisting of 20,000 gates (a typical minicomputer, for example) is calculated as a function of the number of gates on each chip. At twenty gates per chip, 1000 chips are used and at 1000 gates per chip only 20 chips are used. This is the failure rate associated with the chips and ignores the added printed circuit boards and wiring required to interconnect 1000 packaged devices instead of 20 devices. Note that in 1976, the optimum reliability was achieved at 200 gates/chip,

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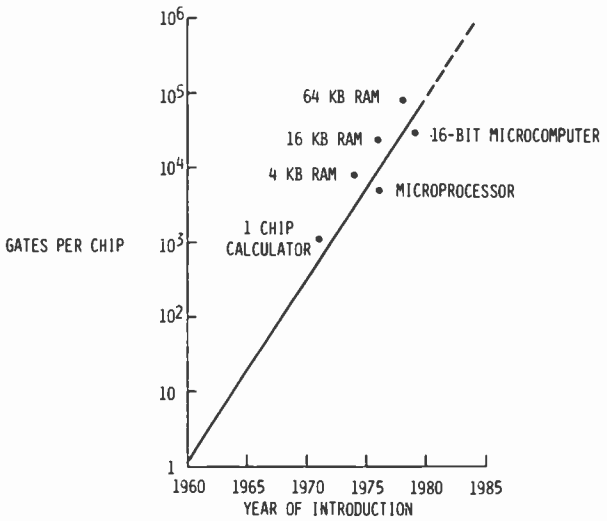

Fig. 1. The semiconductor industry is moving toward larger chips.

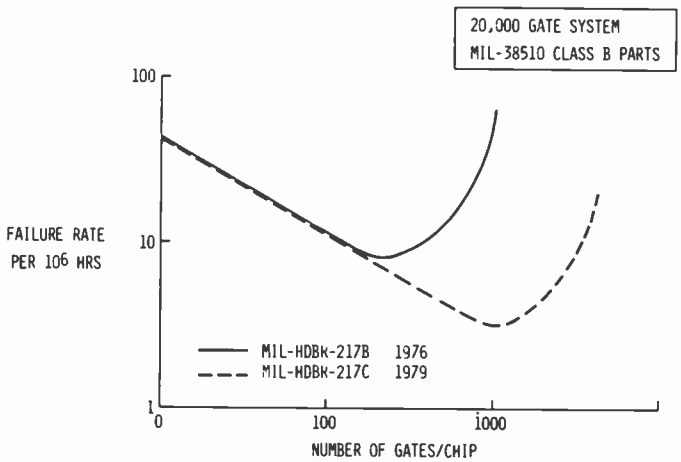

Fig. 2. The failure rate for a model system is calculated as a function of the number of gates on each chip.

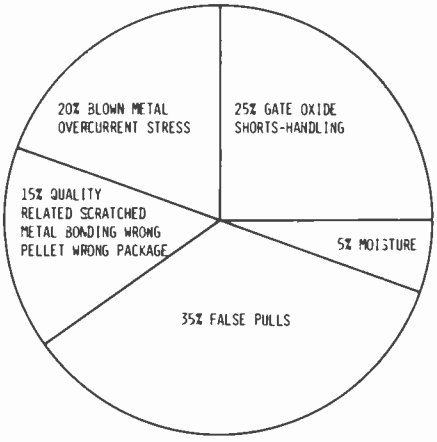

Fig. 3. Mechanisms that normally occur in field failures.

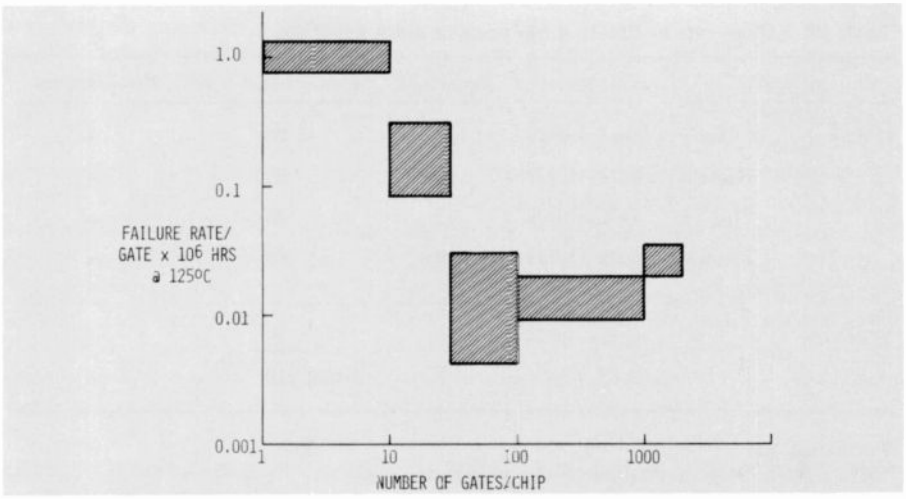

Fig. 4. This data, plotted on a failure rate per gate basis, shows that complex chips offer a reliability advantage.

while in 1979, the projection was for an optimum at 1000 gates/chip.

Causes of CMOS failure

The pie chart in Fig. 3 shows the mechanisms that were found in a large number of CMOS field failures. This article is focused on CMOS parts, since they are made and used so extensively in RCA. Most of these mechanisms relate to per package problems — bonding difficulties, input protection circuit failures, etc. Similarly, examining the failure mechanisms encountered in 125°C life tests (see Table I), most items are package or bond-pad associated. Therefore, large chips and small chips with equal pin counts and similar packages should be equally reliable. However, there are some layout dependent mechanisms. CMOS parts require guard-banding to protect against leaky inversion layers from ionic charge motion. In addition, there are design criteria related to drive and speed constraints that must be met and other design rules whose violation may be a reliability hazard. Nonetheless, the data in Table II indicate that the failure rate is not, in fact, significantly dependent on chip size. The data below 100 gates are taken from an RADC Reliability Analysis Center compilation, but are confined to high temperature tests (125°C or higher) of post 1973 vintage. The data include CMOS parts from Motorola, Signetics, National Semiconductor and other vendors, as well as RCA. The data for more complex chips are RCA-generated. The silicon-on-sapphire (SOS), random access memory (RAM) data, which are very good, are shown separate from the CDP 1802 data.

Examining this data, plotted on a failure-rate-per-gate basis (Fig. 4) shows that complex chips offer a reliability advantage. These failure-rate figures are at 125°C. To examine some reliability results for room temperature operating conditions, the RCA satelites, designed and built at Astro-Electronics, offer 210 million device hours without a single hard failure (Table III). These results include a mix of parts mostly of small scale integration (SSI) and medium scale integration (MSI) complexity. The memory parts have been excluded because twelve memory chips are used in a hybrid package and other reliability factors enter for these memory chips.

Table I. Failure mechanism in 125°C life testing.

— 125° C *Life Tests*
• Dielectric breakdown
• Bonding
• Foreign material
• Metalization
• Ionic charge motion

CMOS/SOS military requirements

There are some unique problems associated with military applications. For space application, parts that are radiation tolerant are required. Bulk CMOS parts incorporate parasitic *p-n* junctions which can interact to show SCR action and cause latchup when a pulse of radiation is incident (or when power supplies are applied in the incorrect sequence). Alpha particles and cosmic rays have been identified as a potential source of soft failures in RAMs. These energetic particles leave behind a trail of hole-electron pairs as they pass through the semiconductor and the resulting current can upset the data storage. Such effects are not encountered in CMOS/SOS parts where only the portion of the particle path in the thin silicon film contributes to the upset current. On the other hand, a wide variety of CMOS bulk parts are available today with megarad total dose capability.

The design cycle for a custom large scale integration (LSI) part, including fabrica-

Table II. CMOS failure rate in high temperature life tests.

Number of gates	*Number of parts-tested*	*Number of failures*	*Thousands of device hours*	λ *failures/* 10^6 *Hrs at* 125° *C*	λ *lower* 20%	λ *upper* 80%
1 - 10	2185	12	4212	2.8	2.3	3.8
11 - 30	614	1	495	2.0	1.7	6.3
31 - 100	364	0	1092	0.9	0.2	1.5
101 - 1000	679	4	1094	3.7	2.8	6.1
≥1001 (1802)	230	8	226	35.0	30.0	53.0
>1001 (SOS RAM)	893	3	438	6.8	5.3	12.0

Table III. Failure rate in CMOS logic parts on RCA satellites.

		Operation	*Hours* x 10^3	**Device hours* x 10^6	*Hard failures*
DMSP	Flight 1	3/77— 9/79	22	70	—
	Flight 2	6/77—10/79	20	63	—
	Flight 3	5/78—10/79	12	38	—
	Flight 4	6/79—10/79	3	10	—
TIROS N		10/78—10/79	9	29	—
				Total 210	

Failure rate per 10^6 hours = 0.005
*3167 *CMOS* devices (other than memory) per spacecraft

Table IV. Custom LSI advantages and disadvantages.

Advantages	*Disadvantages*
More cost effective	Front end design costs
Better performance	Turnaround time
Smaller size, weight	Qualification
Easier to shield	Potential for errors
Improved reliability	Time slippage Reliability hazards
Easier diagnostics and repair	Adequate testing

tion of demonstration vehicle devices, can occupy a significant fraction of a military contract effort. With this time limitation, if there are errors or system design changes to be incorporated, it is vital that the correction procedure does not introduce further errors. Without constrained design tools and extensive checking, any changes can (and often do) introduce numerous errors.

Finally, military quality requirements call for preseal visual inspection of the chip itself. Such inspection can be lengthy and can erode the yield substantially since the inspection procedures and criteria now in use evolved from the inspection of relatively simple chips. There is extensive effort in the industry to substitute added electrical testing (at high voltage and high temperature) in place of the visual inspection.

Custom LSI considerations

Custom LSI parts are used because they are often more cost-effective than assemblages of catalogue parts which would need to be assembled on large boards. Table IV shows the advantages vs. the disadvantages of LSI parts. For MOS parts, speed degradation results every time the signal must go off the chip and large area-consuming drivers are required at every output pin. The more of the processing that can be done on the chip, the faster the signal can be handled. The diagnosis of faults is easier when large functional blocks can be tested and replaced if defective.

The most serious deterents to the use of large-chip custom LSI are the front end design cost and the time required for the design to be implemented. These problems have been addressed in Government Systems Division (GSD) by the development of computer-aided design tools which trade-off chip area minimization for reduced design costs and by the development of the Solid State Technology Center (SSTC) as a quick turnaround producer of custom LSI parts. Qualification of high-volume part designs by the semiconductor merchant supplier is accomplished during the long development and the extended production cycle. Family qualification and constrained design techniques which build a heritage of reliability in the building blocks for a technology substitute in custom LSI. The potential for errors is minimized by maximum use of computer aids and of design verification techniques. Finally, the most serious inherent problem of large chip custom LSI is that the limited access to the complex logic on the chip, through the pins, makes it difficult to test completely to validate the chip design and to assure reliable performance.

Computer-aided design tools

Programs exist for simulation of devices, of building blocks and cells, for simulation of the logic and of the circuit timing. A computer program, CRITIC, is used to check for design rule violations in the new parts of each design and the interconnection net list is checked automatically against the actual layout topology. Test generation is not a "solved" problem, but using the TESTGEN program, a test sequence can be checked to identify the nodes it exercises. Additional tests can be inserted to provide coverage at any omitted nodes. Finally, the design is transferred between various display and execution equipments — the Versatec check plotter, the Applicon Interactive Graphic Design System, and the MEBES mask generator system. (It is vital that the reformatting required be done by a computer-controlled system to prevent errors.)

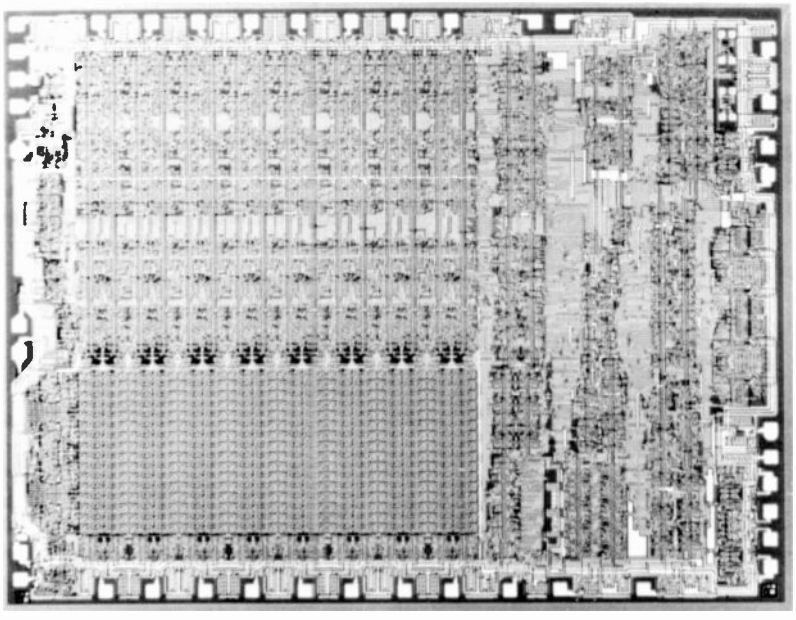

Fig. 5. This CDP 1802 COSMAC microprocessor is a hand-crafted layout.

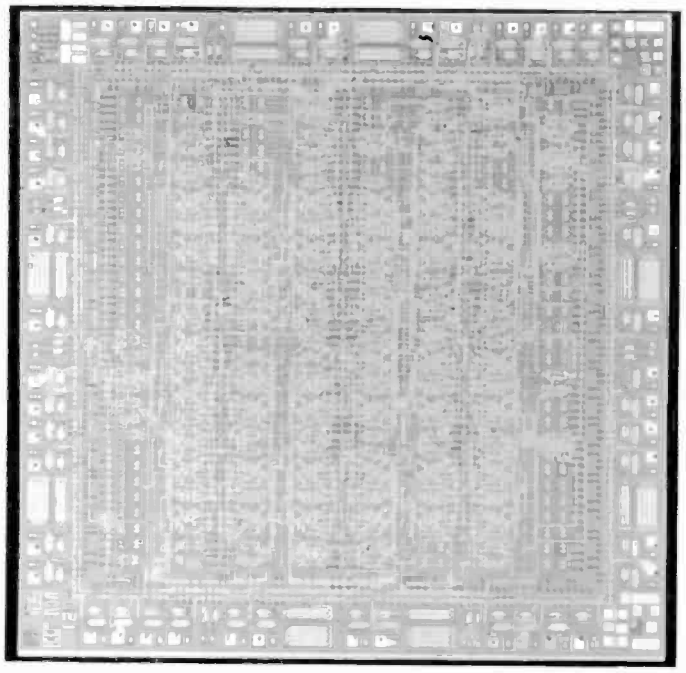

Fig. 6. The TV system synch generator chip uses 300 gates of logic on a 230 x 230 mil area.

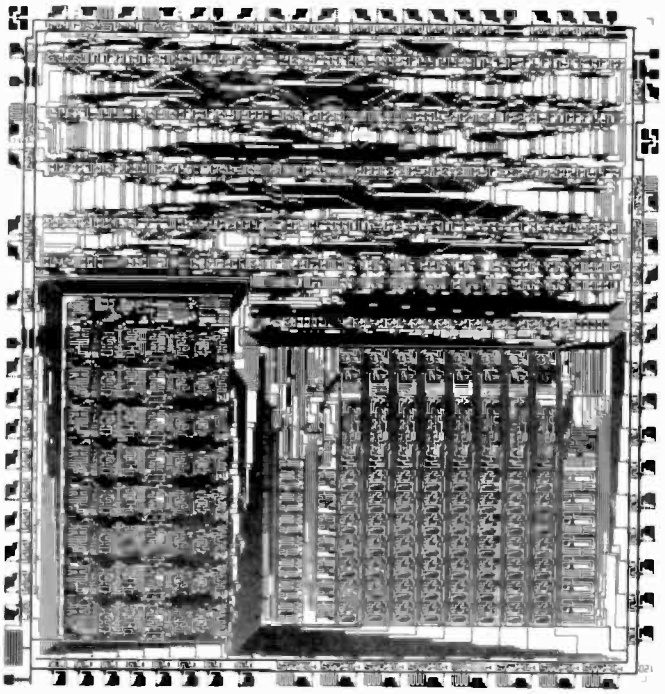

Fig. 7. The ATMAC IOFU chip incorporates close to 2000 gates on a 270 x 170 mil area.

CMOS chips that illustrate design approaches

The CDP1802 COSMOS Microprocessor (Fig. 5) is a hand-crafted layout. It includes over 1200 gates on a 230 x 180 mil chip. The layout was carefully prepared by a dedicated team and it is the example that proves the rule — it worked correctly the first time. The regular area on the lower left is the memory register stack on the chip and the regular structure above it is the 8-bit parallel data path. This device makes very effective use of chip area.

At the other extreme, is a TV system synch generator chip (Fig. 6) for Broadcast Systems. It makes use of the gate universal array approach. Close to 300 gates of logic are available on this 230 x 230 mil chip. Not all of the gates are used. The design is accomplished using predesigned cellular layouts for the logic elements and then interconnecting the logic elements. A variety of CMOS Universal Gate Arrays are available in both bulk and SOS technologies (Table V). Current effort at GSD is focused on an automated technique for layout and interconnection since the Universal Array interconnection net layout is increasingly demanding as more gates are put on a chip and a higher percentage of the available gates is used (80-90 percent is the normal range).

Automatic placement and routing

The chip in Fig. 7 is one of two that make up the ATMAC microprocessor, a signal processing oriented 8-bit CMOS/SOS system that runs at better than 10 MHz. It incorporates close to 2000 gates on a 270 x 270 mil chip and is a combination of careful hand-crafted layout of the register areas as well as a standard cell layout for the random logic. The ability to mix design techniques is important in microprocessor

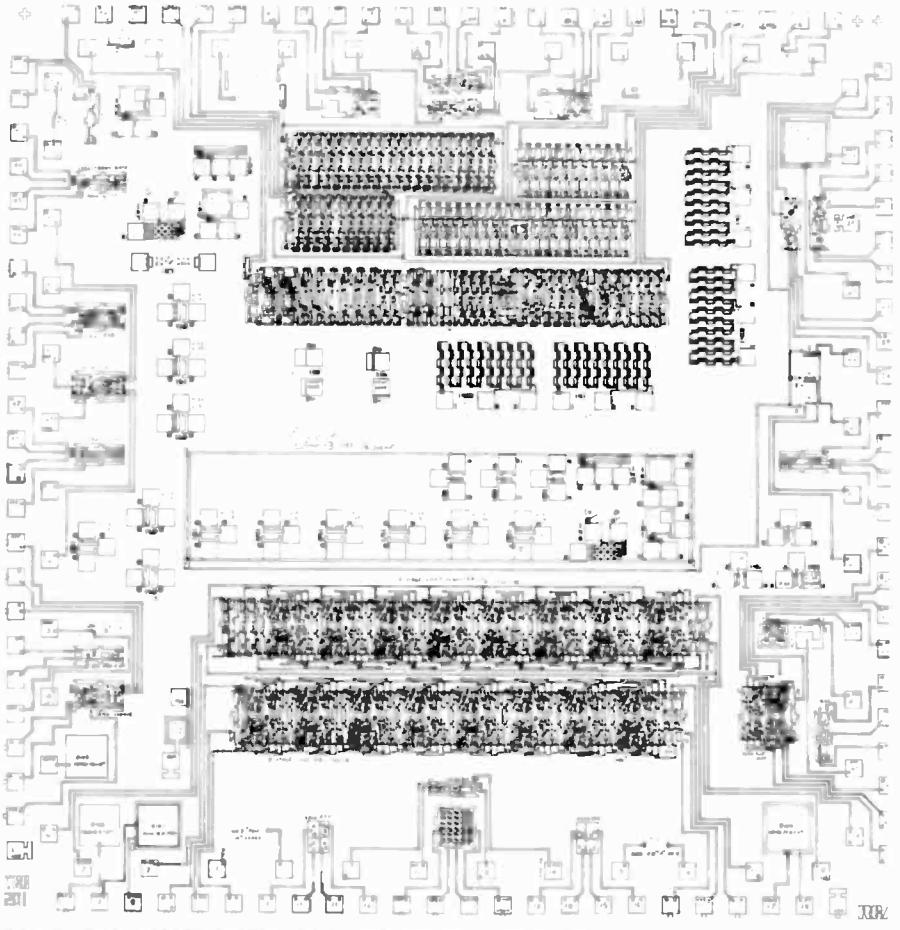

Fig. 8. A standard cell test chip is used to characterize the cells.

chip design. The random logic layout is done using the automatic placement and routing (APAR) scheme, which is the basis for most of GSD's custom LSI designs. Using this technique in 1974, a group of three engineers in Camden designed 38 custom LSI arrays over an 18-month period. This technique is the most highly automated available.

The logic design, annotated in terms of the standard cell library elements, is input to the MP2D program which automatically places the cells and interconnects them. The layout can then be examined in check plot form. Changes can be made to optimize the layout using an Applicon Interactive Graphics System. Such changes cost time but, more seriously, they frequently introduce errors. One path commonly elected is to revise the placement, but to then let the MP2D program reroute the wiring in an error-free fashion. When the layout is satisfactory, a check plot is prepared, the critical path speed is checked, and the layout topology is subjected to a check against the original net list. The design file language information is converted to the proper format so that it can be input to the MEBES mask fab machine. All of these programs intercommunicate through a common data base.

The cellular elements used in this design are available in a variety of technologies, in the form of open-ended libraries of cells designed, characterized and proven for reliability. Figure 8 shows a test chip on which the basic cells in the library are provided with separate bondout pads for each. Combinations of cells are used to measure propagation delays and to characterize drive capabilities and requirements. Individual cells are life tested. After such extensive testing of the cells, there is a high degree of confidence that a chip built by assembly of such cells will function properly and provide reliable chip operation.

Testing

Testing of large chips is a significant problem. The internal nodes, tucked safely away from outside static discharges and parasitic capacitances, are also inaccessible for testing. Typically, a test program will simply "put the part through its paces" and check that, when the inputs go through the expected signal sequence, the outputs will follow in the desired fashion. This is inadequate to characterize possible defects inside the chip. In a telecommunications program several years ago, the normal noise environment provided spurious input signals which changed the state of the LSI part so that its subsequent behavior was incorrect and depended on the status of nodes that had not been exercised in functional testing. This is a serious problem because testing every node for "stuck at 1" or "stuck at 0" is difficult.

Just for calibration, Sandia engineers generated a "complete" set of test vectors for the CDP 1802 which included 160,000 test vectors. There was some redundancy in this set, but the MIL 38510/470 slash sheet uses 12,000 test vectors, and previously, commercial grade testing used less than 6,000 test vectors.

A test sequence can be generated to test combination logic networks completely. But for sequential networks, including storage elements (e.g., latches, flip-flops, etc.), it is not generally possible to define a complete sequence of test vectors. At present, a CAD program, TESTGEN, is used which accepts the proposed sequence of test vectors and identifies those nodes which are exercised. A skilled test designer can then add test vectors to test the remaining nodes and can often complete the job. Several computer system houses have developed and imposed design constraints which assure testability of the chip. The IBM System, Level Sensitive Scan Design, requires that all storage elements be directly accessible from off the chip in a chain fashion. A known signal can be passed down the chain to initialize the chip condition and testing can proceed as for a combinational chip. This constraint has been estimated by IBM to require 20 percent additional chip area, but it reduces the testing problem to one that can be solved by an automatic test generation computer program.

Conclusion

With tested building blocks, computer checks of the interconnection networks, automatic data handling systems, extensive chip testing and basically reliable chip technology, large custom LSI chips can contribute significantly to system reliability.

Jack Hillbrand, Staff Technical Advisor on Government Systems Division's Engineering Staff, has been involved for the past eight years in supporting the use of semiconductor parts and specifically, custom LSIs by GSD. Previous to that he was at Somerville for a decade with SSD and SSTC where he was involved in the early development of power transistors and CMOS ICs. Jack joined RCA Laboratories directly from school in 1956 after receiving an ScD from the Massachusetts Institute of Technology. He is a Fellow of the IEEE.

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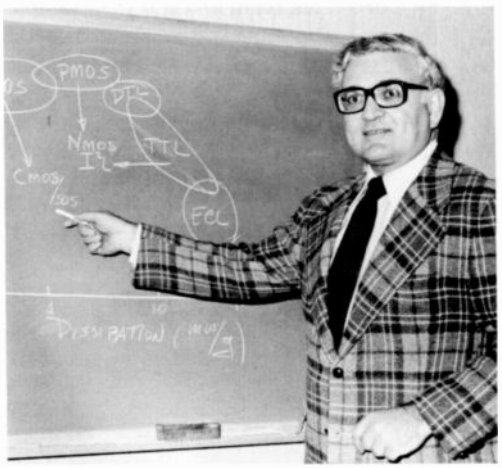

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C.W. Thierfelder|F.J. Hinnenkamp

Low arc picture tube development using statistically designed experiments

Factorial experiments provide testing efficiency and cost effectiveness, interaction of test results, and thorough data analysis, resulting in quality picture tube performance.

Abstract: *Low arc picture tubes have been developed that are expected to result in better television reliability and lower warranty cost. This important breakthrough resulted from the extensive effort of the Princeton (DSRC) Laboratories, PTD, CE Interdivisional Task Force and the use of statistically designed experiments. How these experiments implemented the decrease of picture tube arcing, thus, giving a better quality tube, is described.*

Picture tube arcing has been a problem since the beginning of commercial television. Although much effort has been directed over the years to develop low-arc picture tubes and to employ arc-circuit protection, arcing has continued to cause damage to the receiver circuitry or to the picture tube resulting in the cost of occasional service calls.

During 1978, RCA commercialized a limited quantity of high performance TV receivers featuring a new, high resolution high potential precision inline (HiPi) electron gun and compact chassis. Reliability testing increased management's concerns related to picture tube arc damage to integrated circuits (ICs), solid state devices and components, and to the frequency of set shutdowns. Consequently, protection was increased throughout the receiver to prevent service call failures for customers. The application of the higher focus voltage to the "low voltage region" of the HiPi electron gun resulted in a secondary emission charge build-up on the insulators and a "trigger arcing" phenomenon. Some of the chassis were subjected to several hundred arc discharges during life before the picture tube arced to stability. The higher arcing frequency necessitated arc suppression to negate the risk of arc induced overvoltage stresses to chassis components and occasional receiver shutdown.

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An Interdivisional Task Force, comprised of representatives from Princeton (DSRC) Laboratories, Picture Tube Division (PTD), and Consumer Electronics (CE), was organized to address and correct this reliability problem before RCA converted a major portion of the production to the new high performance HiPi picture tube and planar chassis designs. The chassis arc protection was reviewed and improved. A higher resistance internal conductive coating was developed for the picture tube and commercialized to reduce the peak arc current by a factor of approximately three to one and thereby reduce the incidence of circuit damage. An improved high voltage conditioning process was developed and conveyorized in the PTD plants to assure management control of the process parameters. This RF spotknock (RFSK) process seeks out the emission sites and blunts them to reduce the arcing incidence significantly. A model describing the picture tube arcing phenomenon was developed.[1] It has been shown that metalized bead suppressors (MBS) in conjunction with RFSK high voltage processing are effective in producing very low arc picture tubes. Production build-up of the MBS has been started to support CE's production requirements. A further optimization of the picture tube internal conductive coating resistance is being developed which is expected to further reduce the peak arc current to about 100 amperes. It is planned to introduce this new soft arc development during the first half of 1980. The anticipated learning curve improvements of these developments are expected to result in a near zero arc tube in the future.

Arc phenomena and prevention

Picture tube arcing is very difficult to measure and to analyze statistically because it normally occurs on a small portion of the product and varies erratically with time. Picture tubes usually arc to stability when operated under normal conditions. The arcing frequency tends to decrease exponentially with time; however, some tubes will be stable initially and then develop an arc later on in life before they finally arc to stability. The high performance, higher voltage, HiPi and tripotential electron gun designs have increased the arcing incidence and complexity. Figure 1 is a photograph of the HiPi electron gun. The sample on the left shows the multiform glass bead plane view and the right-hand sample shows the electrode plane view.

There are two basic types of high voltage instability breakdowns experienced in picture tubes: First, the "interelectrode arc"

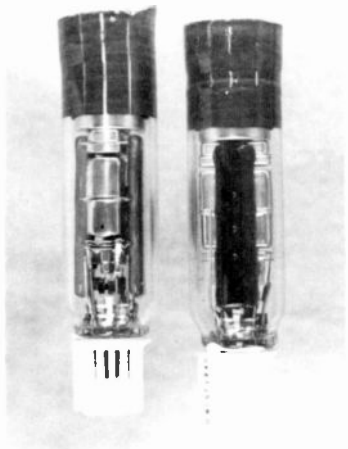

Fig. 1. The sample on the left shows the multiform glass bead plane view of the HiPi electron gun, and the right-hand sample shows the electrode plane view.

and second, the "trigger arc," or flashover, that results from a complex insulator charging phenomenon. The interelectrode arc occurs between two adjacent electrodes in an electron gun to which high voltage is applied such as the focus lens (G3 and G4) and the prefocus lens (G2 and G3). The interelectrode arc occurs in a vacuum due either to field emission from microprotrusions[2] or to the passage of particulate matter from the low to the higher voltage electrode,[3] which breaks down the vacuum in the space between the electrodes. Sharp points, microprotrusions, foreign particles, dust, or sharp electrode edges can create the high voltage gradients required to produce the field emission, which in turn leads to the voltage breakdown, interelectrode type of arc. The formation of such an arc is shown in the time-lapse photographs in Fig. 2. The left-hand photograph shows the field emission from the G3 electrode impinging upon the neck glass. The second and third photographs show the build-up of the field emission and the resulting interelectrode arc.

The "trigger arc," or flashover, is caused by a complex and relatively uncontrolled build-up of potentials on the insulative surfaces of the neck glass and the multiform glass bead in the "low voltage region" of the electron gun. The trigger arc is usually preceded by a visual blue glow of the neck glass in the vicinity of the cathode near the G2 connection.

Drs. K.G. Hernqvist and C.W. Struck of the Princeton Laboratories developed a computer model[4] describing the neck and electron gun charging characteristics. Dr. Hernqvist has further developed his model with the collaboration of experimental laboratory observations and the results of numerous Task Force-designed experiments executed in the PTD factories. A high potential is established along the neck glass due to the bulk or the surface conductivity of the glass. Field emission occurs from sharp points near the neck glass. Electrons impact the glass and multiform beads and charge it to a potential of approximately 3,000 volts where the secondary electron emission yield is unity. Electron avalanches are formed along the neck glass primarily in the vicinity of the multiform bead. Electron stimulated desorption occurs as the avalanche produces a zone of desorbed gas near the glass surface. Electrons ionize the desorbed gas molecules. The resulting positive ions travel to the field emitter sites and thereby enhance the emission level. This leads to a runaway condition, plasma formation and results in a "trigger arc." It is not uncommon for several interelectrode arcs to follow a trigger arc. The formation of a trigger arc is shown in Fig. 3. The left-hand photograph shows the field emission blue glow excitation of the neck glass in the cathode and G3 region. The middle photograph shows the avalanche build-up. The right-hand view shows the plasma formation and the resulting high-energy trigger arc discharge.

Two primary Pareto arcing prevention techniques have been developed to reduce the incidence of interelectrode and trigger arcing. The first is the application of RF spotknocking to the finished tube. This is a most effective way to clear the electron gun of residual dust, foreign particles, microprotrusions, and sharp point field emitter sites and thereby minimize interelectrode arcing. The second is to employ an electrically floating, conductive suppressor patch or band on the insulators in the low voltage region of the electron gun. Such a suppressor prevents the regenerative secondary emission avalanche build-up plasma formation described above and thereby effectively eliminates trigger arcing. Figure 4 is a photograph of the MBS applied near the center of the multiform bead shown on the right-hand sample gun. This conductive patch charges up to a potential that varies with time according to the particular high voltage stability conditions. It eliminates the avalanche build-up and the resulting trigger arc.

Picture tube manufacturing conditions

Modern picture tube mass production plants are clean environments to prevent foreign materials and field emission arc sources from being assembled inside the tube. Every component part and material used in the manufacture of a picture tube

Fig. 2. The formation of the interelectrode arc is shown in these time-lapse photographs.

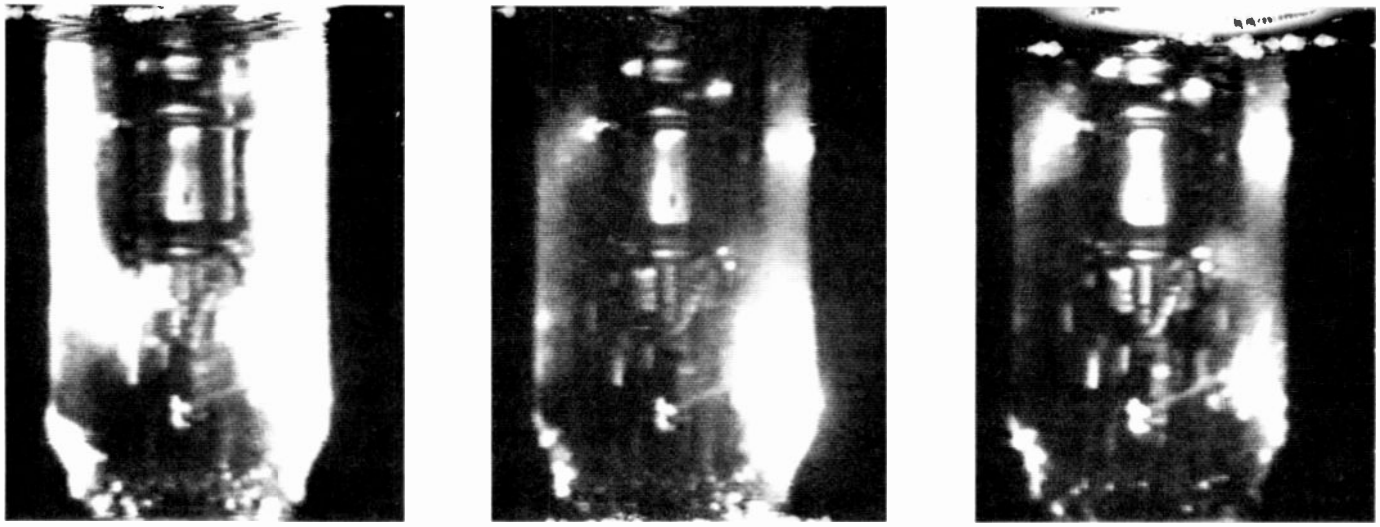

Fig. 3. The left photograph shows the field emission excitation of the neck glass in the cathode and G3 region during the formation of a trigger arc. The middle photograph shows the avalanche build-up. On the right, the plasma formation and resulting high-energy trigger arc discharge are shown.

receives extensive washing and cleaning operations. The mount parts are tumbled, deburred, and carefully washed and fired. The beaded electron gun assemblies and shadow masks are usually ultrasonically washed. The panels and funnels are carefully washed and the finished sub-assemblies are "air scrubbed" to remove any foreign materials. However, to mass produce picture tubes without high voltage processing and spotknocking would require ultra "clean-room" conditions, which would be extremely costly with questionable success since there are a large number of known and unknown arcing variables that occur in the mass production of picture tubes and that vary from time to time.

Evaluation testing procedure

Several key decisions were made early in this Interdivisional HVS Task Force development that contributed to an understanding of the mechanism and resulting control of the arcing phenomena which had evaded picture tube manufacturers for many decades. These were:

1. Sample tubes to be evaluated for arcing had to be manufactured under production conditions at one of the RCA picture tube plants to assure that all actual production known and unknown arcing causal variations were included in the evaluation tests.
2. Good experimental test designs and statistical techniques had to be used along with adequate pretest planning to assure that necessary arrangements were made to obtain well executed, representative test results.
3. All tests were to be made with an adequate sample size to permit statistically meaningful analysis and results to be obtained. The control tubes had to made at the same time, duplicating the test samples except for the parameters being tested. Multivariable tests were to be employed to compare with the control tests in order to identify which of the variables had the strongest significant effect on arc reduction and which variables were relatively unimportant.
4. The arc count testing had to be done essentially at one location to simulate the handling and transportation exposure normally encountered by the product as it is delivered to the customer's plant. Stressed arc count testing was to be made at the maximum operating voltages and had to be extended in time to permit the product to arc to stability during the test period. An accelerated ON-OFF operating cycle was to be used to shorten the test period.
5. Randomization techniques were to be employed throughout selection, production, and testing of the picture tubes and their component parts.
6. High-low failure mode analysis techniques were to be used on selected samples to identify the real causal variations responsible for the arc count performance.
7. Confirmation tests were to be run to determine the time-to-time product variations and to turn on and off the effects of the established significant variables.
8. Supervision and guidance to explain the evaluation tests were to be given to the different activities and plant personnel who were responsible for running the tests.

Experimental design strategies

A number of different statistical-engineering strategies are available to help generate clues as to the nature of often-unsuspected but important variables that actually control the dispersion of a product characteristic such as arcing.

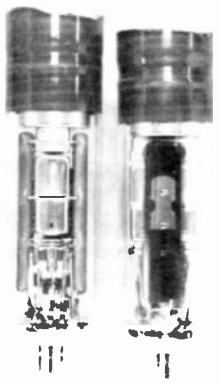

Fig. 4. The conductive path of the multiform bead, shown on the right-hand sample gun, charges up to a potential that varies with time.

Multi-vary analysis may be used to evaluate a stratified (non-random) sample of consecutive items. This particular form of measuring the product permits plotting a chart that reveals the relative size of three or more independent components of the total variation, which has been excessive. The major components are time, cyclical, and positional variations; the largest of which indicates that the yet, undiscovered controlling variable is a member of that "family."

Factorial designed experiments permit the simultaneous evaluation of variation influences of two or even more of the variables suggested by the family identification clues; their separate as well as their combined, interactive effects are numerically identified.

When one of the strongest of these causal variables seems to emerge, a rank order comparison of the expected better (B) condition may be made against the current (C) unchanged condition. It is a way of testing one's ability to turn the trouble on and off, like a light switch; but with sample size and random sequence control to reach pre-selected statistical levels of risk and confidence.

Statistical analysis techniques

Picture tube arcing is very difficult to measure and to analyze statistically because it normally occurs on a small portion of the product, varies erratically with time, and follows a non-normal distribution with more than one mode. The statistical test cell sample size employed for arc counting varies from eight to fifteen to thirty depending upon the arcing frequency and dispersion characteristics. It is not too unusual to find one or two high arc counts well beyond the normal distribution in a test cell.

Four statistical analysis techniques were employed for this study: Weibull Analysis, Rank Order Analysis, Computer Program Analysis of Variance, and Benchmark Comparisons.

The Weibull Analysis offers several advantages and was widely used because:

1. Most of the data plots are a straight line on Weibull paper, regardless of the shape of the frequency distribution;
2. Very high arc counts do not exert undue influence such as they do when averages are used; and
3. The plot presents a visual data display which facilitates one's ability to grasp and understand differences of many data points.

The Rank Order Analysis is an easy method to apply, and is especially useful when two or more relatively small groups of data are being analyzed, such as in the case of B versus C comparisons and multi-vary tests.

The Computer Program Analysis of Variance is a technique used to evaluate large factorial tests. It can readily show the effect of higher order interactions.

The Benchmark Comparison method has been widely used to compare the arc count performance of many tests for different reference operating test periods. The benchmarks found to be most meaningful were the % 0, %>3, %>10, and the median arc counts. A plot of these benchmarks is very useful in monitoring the progress made in reducing the arc count and eliminating the high arc tubes.

A combination of two or more of the above analysis methods was widely used in order to improve the confidence of the conclusions reached. Individual tests were replicated when borderline significances were obtained and to enhance the confidence of strong effects.

Failure mode analysis

One of the most important statistical analysis techniques employed by the Task Force was the use of high-low arc pair defect analysis methods to get clues from the product to define the actual failure reasons. One can usually make corrections in designs, materials, or processes to eliminate or reduce the particular failure mode cause once it has been identified. However, one often makes expensive engineering changes by analyzing and taking corrective action based on the analysis of the failures, or high arcers, only to find that the product arcing characteristics were not improved because the assumed defect had very little or no real effect.

D.J. Shahan and P.R. Liller of PTD made many high-low arc pair analyses so paired comparisons could be made of the observations versus the actual arc performance. Their work produced very important product clues that were evaluated by follow-up designed experiments and contributed greatly to the success of this project. Many of the historical factors thought to have major effects on high voltage stability proved to have little or no effect on the actual arc performance. They developed the light amplification recording system (LARS),[5] shown in Fig. 5, to study the arcing mechanisms in real time, slow motion, and stop action on a video tape. This system was widely used for pair-analysis and to develop the model to understand the arcing mechanism. A tube to be evaluated is mounted in the LARS cabinet and connected to the internal power supplies. An image intensifier camera is focused on the electron gun and connected to a monitor and video tape recorder. The room is darkened so the high voltage instability effects can be observed at very low light levels below the visual threshold as the operating voltages are raised to the normal operating and to the stressed 50-kV anode voltage level. The stray emission and arcing can be observed and studied for possible causes. The LARS photographs shown in Figs. 2 and 3 illustrate the stray emission and arc discharge of an interelectrode and trigger arc.

Experimental test results

The effectiveness of the Interdivisional Task Force program to improve the high voltage stability of RCA's HiPi picture tubes is conclusively shown on the benchmark histogram in Fig. 6. One wants a very high percentage of no-arc tubes, a very low percentage of greater than 3 or 10 percent arc tubes, and median arc counts. The poor arcing characteristic of the HiPi regular product made during 1978 is illustrated by the eight test results shown in Fig. 6, in comparison to the low arc performance of the nine tests of the improved product featuring the MBS and RFSK developments. Each test data point represents at least thirty sample tubes made

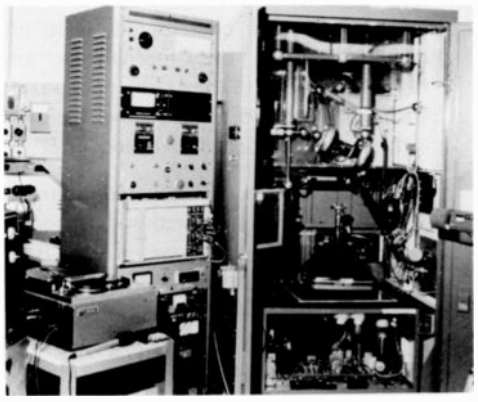

Fig. 5. This light amplification recording system aids in the study of arcing mechanisms in real time.

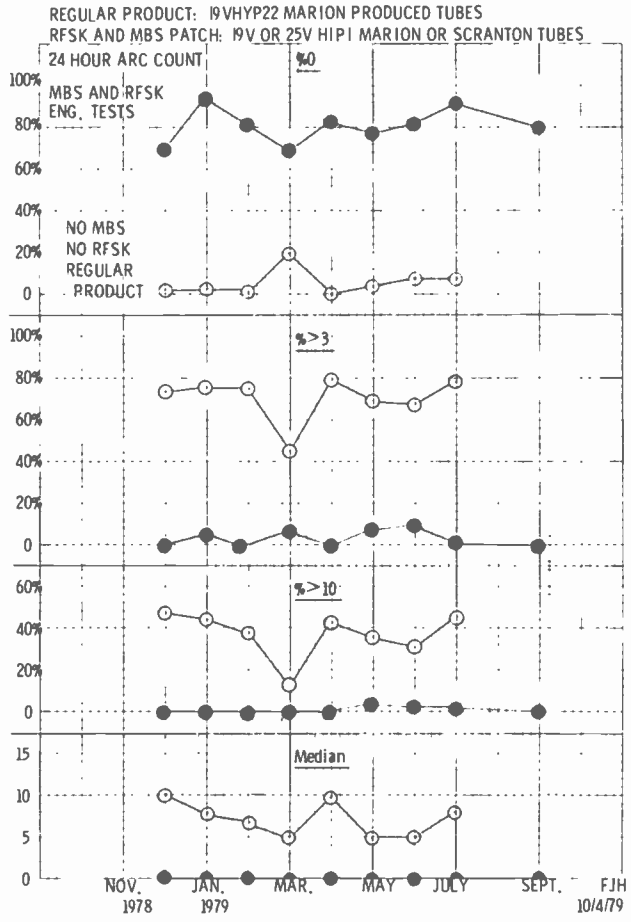

Fig. 6. The effectiveness of the interdivisional Task Force program to improve high-voltage stability of HiPi picture tubes is shown on this benchmark histogram.

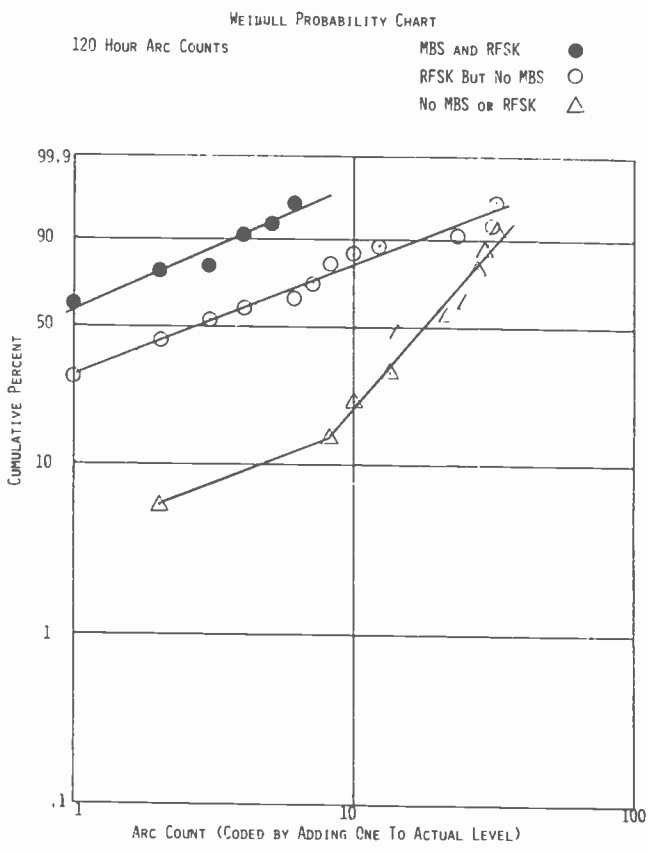

Fig. 7. This Weibull data display shows three sets of data from arc-time-test number 66 plotted on Weibull probability paper.

under production conditions in the factories.

An example of the Weibull data display is illustrated in Fig. 7. Three sets of data from arc-time-test number 66 were plotted on Weibull probability paper by adding one to the zero and other actual arc count values. The lowest arc count plot is for a sample of thirty tubes made with the MBS and RFSK features. The intermediate arc count curve is for a control test made without the MBS but with RFSK processing. The poorest arc performance was obtained with the control samples made without the MBS and RFSK developments under the same production conditions. The confidence level associated with these differences is readily determined by the use of charts or tables. The confidence level is 99 percent or greater for all three of the paired comparisons shown in this Weibull plot. The same data are displayed in the frequency distribution charts shown in Fig. 8. The product made without the RFSK and MBS developments has a wide dispersion and poor arc performance shown in the top distribution. The RFSK improvement is illustrated by the middle distribution. The combined RFSK and MBS improvement is shown with the low arc tight distribution in the bottom chart.

The rank sum test is a nonparametric statistical test which may be used to compare small sample results from two pop-

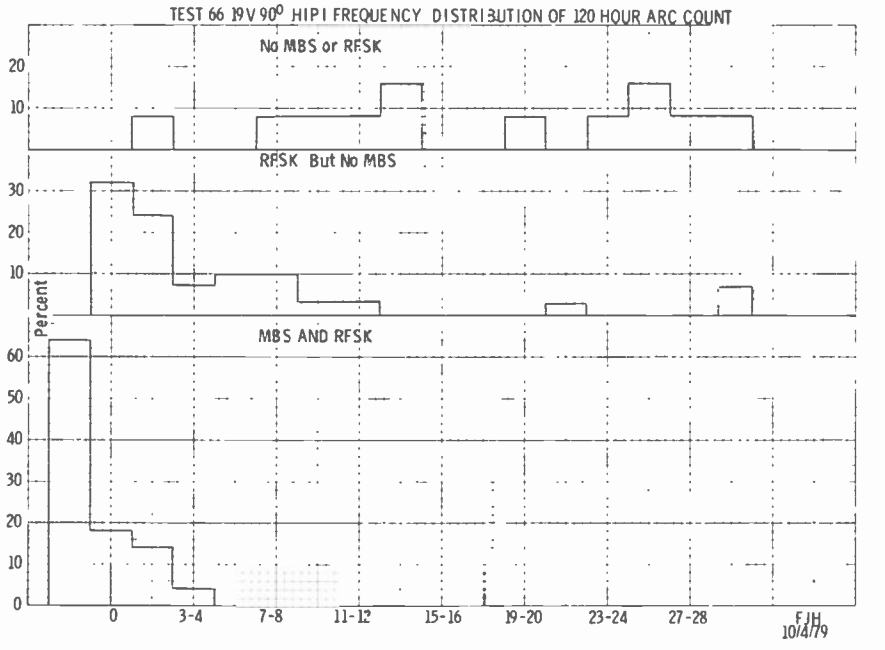

Fig. 8. The three sets of data from arc-time-test number 66 are displayed in these frequency distribution charts.

Table I. Rank sums data analysis.

Arc Time Test #31	*Evaporated Chrome on Beads*				
120 *Hour Arc Count*		*Ranking of Data*			*Calculation of Rank Sums*
Test (B)	*Control (C)*	*Rank*			
0	0	1	B		B = (7x5) + 11.5 + 14 + 16 = 76.5
0	0	2	B		C = (2x5) + (3x11.5) + 15 + 17 + 18 + 19 + 20 = 133.5
0	1	3	B		Rank sums test
0	1	4	B	Tied	B = 76.5
0	1	5	B		C = 133.5
0	6	6	B		Reference to a table of rank sums shows this difference is significant at the 98% level.
0	8	7	B		
1	12	8	C		
3	16	9	C		
7	18	10	B		
		11	C	Tied	
		12	C		
		13	C		
		14	B		
		15	C		
		16	B		
		17	C		
		18	C		
		19	C		
		20	C		

ulations regardless of the type of distribution characteristic of each. Nonparametric statistics make comparisons between the individual values and not between parameters such as the mean and standard deviation.

In the rank sum test, the values from both samples are put together and ranked from lowest to highest (or vice versa). The lowest value is given the first rank, or 1, and the highest value is given a rank equal to the total number of items.

If the two samples are not really different, the ranking of the items will tend to intermingle the groups and the rank sums of each will be about equal. If the two samples are different, the values from one group will tend toward the lower ranking while the other group will tend toward the higher ranking. Probabilities may be assigned to the occurrence of all ranking combinations by chance alone and the actual results compared with them to determine significance.

Arc time test #31, the very first test result of a MBS product, is shown in Table I along with the rank sum test to determine significance.

The factorial experiment (Table II) is a test design in which all levels of each factor (variable) in the experiment are combined with all levels of every other factor. The advantages of such a design are:

1. Efficiency and cost effectiveness — more information can be extracted from a fewer number of samples than the classical, one-at-a-time test design.

2. Interactions — the test results for a combination of two or more factors that are different than the numerical sum of their individual contributions. Since all combinations of factors and levels are included in this design, any interaction effects of the factors can readily be determined by analyzing the data.

3. Data analysis — such parameters as the mean, standard deviation, confidence limits, significance of differences, etc. can readily be determined by using Analysis of Variance computer programs.

Table III tabulates the results of an MBS patch and high-voltage processing factorial test. An analysis of these data indicates there are only two main effects: the MBS patch and RFSK process significantly lower the arc count.

Table II. Factorial combination of five test variables.

Factorial Design		
Factors	*+ Level*	*− Level*
1. MBS patch	Yes	No
2. Initial spotknock	On	Off
3. High voltage age	On	Off
4. Post IIP CDBG	On	Off
5. Post IIP RFSK	On	Off

Cell No.	1	2	3	4	5
1	+	+	+	+	+
2	+	+	+	+	−
3	+	+	+	−	+
4	+	+	+	−	−
5	+	+	−	+	+
6	+	+	−	+	−
7	+	+	−	−	+
8	+	+	−	−	−
9	+	−	+	+	+
10	+	−	+	+	−
11	+	−	+	−	+
12	+	−	+	−	−
13	+	−	−	+	+
14	+	−	−	+	−
15	+	−	−	−	+
16	+	−	−	−	−
17	−	+	+	+	+
18	−	+	+	+	−
19	−	+	+	−	+
20	−	+	+	−	−
21	−	+	−	+	+
22	−	+	−	+	−
23	−	+	−	−	+
24	−	+	−	−	−
25	−	−	+	+	+
26	−	−	+	+	−
27	−	−	+	−	+
28	−	−	+	−	−
29	−	−	−	+	+
30	−	−	−	+	−
31	−	−	−	−	+
32	−	−	−	−	−

Acknowledgments

The credit for the developments described in this article is due to the individual and collective efforts of the Princeton (DSRC) Laboratories, PTD, and CE Interdivisional HVS Task Force and their support organizations. The seated members of the HVS Task Force representing Princeton were E.V. Fitzke, K.G. Hernqvist, and R.D. Lohman. Representing PTD were J.K. Breneman, F.J. Hinnenkamp, L.F. Hopen, R.L. Leigh, and C.W. Thierfelder. Representing CE was C.W. Hoyt.

Table III. Marion MBS patch and high-voltage processing factorial (arc count after 120 hrs).

	MBS Patch		*Initial Spotknock*		*High Voltage Age*		*Post IIP CDBG*		*Post IIP RFSK*	
	Yes	*No*	*On*	*Off*	*On*	*Off*	*On*	*Off*	*On*	*Off*
% 0	31	1	20	12	15	18	12	20	19	14
% > 3	44	79	58	64	60	62	61	60	45	76
% > 10	19	51	25	44	30	40	36	34	20	50
Median	2	11	5	7	6	6	6	6	3	10
MBS Patch										
% 0			38	25	28	35	25	38	40	22
% > 3			38	50	42	45	45	42	22	65
% > 10			10	28	10	28	20	18	10	28
Median			2	3	2	2	2	2	1	6
No MBS Patch										
% 0			2	0	2	0	0	2	0	2
% > 3			78	80	78	80	78	80	68	90
% > 10			40	62	50	52	52	50	30	72
Median			8	22	11	11	14	11	6	23

Conclusions:

1. Both the MBS patch and Post IIP RFSK significantly lower the arc count. There are no other significant main effects.
2. There are two significant interactions:

   A. The effect of the RFSK is enhanced when high voltage age is on and there is no MBS patch.

   B. Without RFSK or the MBS patch, high voltage age increases the arc count.

The authors wish to thank D.J. Shahan for his helpful advice on test design, data analysis and statistical techniques.

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Chuck Thierfelder, left, and Frank Hinnenkamp were among those representing PTD for the HVS Task Force.

Chuck Thierfelder, Division Vice President, Product Safety, Quality and Reliability, of the Picture Tube Division, has held his present assignment since January of 1978. Prior to this, he held the position of Division Vice President of Technical Programs during 1976 and 1977. He had previously been Division Vice President, Manufacturing, from June of 1973 through December of 1975; Division Vice President, Engineering, and Chief Engineer from 1965 to May of 1973; and had held various picture tube engineering positions since 1943.

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Frank Hinnenkamp, Manager of Reliability, Warranty and Life Test for the Picture Tube Division, has held his present assignment since June of 1978. His previous experience at RCA includes cathodes, heaters, life test and statistical work in areas of design of experiments and data analysis.

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L. Gibbons

The Solid State Division's Reliability Engineering Laboratory

Highly accelerated tests, which are real-time quality indicators, are used to control the reliability of the end product by in-process control.

Abstract: *The Solid State Division's Reliability Engineering Laboratory (REL) is a unique engineering department that tests devices to failure to determine characteristics which could cause equipment failure. Having this information at hand, members of REL work with design and applications engineers to ensure that a product is improved to the point of being customer-worthy before it is introduced to the market. Accelerated stress tests, performed by REL, serve to establish the data base for reliability prediction on all Solid State products.*

Solid State Division's (SSD) Reliability Engineering Laboratory (REL) was organized more than ten years ago. Although the management has changed, the basic charter of REL has remained unchanged: to determine the actual performance capability of a product to assure that it can fulfill its reliability and specification requirements.

Semiconductor reliability

The design and consistent production of reliable semiconductor devices is a demanding and continuing task. Reduction of field failure rates to a few tenths of one percent was once considered a highly optimistic goal. Semiconductor devices recently developed for the consumer and automotive industries, however, have demonstrated that this goal can be achieved. The demand for even further improvement in reliability performance will surely continue, i.e., in the area of 0.01 to 0.02 percent in the system warranty period (system warranty of 3 to 12 months).

There are several key elements essential to the achievement of high levels of reliability:

- Reliability evaluation of prototype devices;
- Inherent design integrity;
- Reliability — verification testing;
- Effective physics of failure analysis and information feedback;
- Proper rating and characterization;
- Design and application compatibility;
- Proper operating and handling procedures; and
- Real-time indicators (RTI).

A reliability program must accomplish at least four objectives:

1. Provide information to the design team early in the program.
2. Establish the design margin of the final product design.
3. Establish real-time controls and other reliability test procedures at the manufacturing plant to ensure that the reliability level is maintained throughout the production cycle.
4. Enable prediction of reliability in the end use application.

Product development

Within RCA, the responsibility for product development rests with three distinct engineering disciplines:

Applications Engineering — Responsible for defining the circuit requirements for the device in the form of an objective specification.

Design and Process Engineering — Responsible for the design of the semiconductor devices to meet the objective specification.

Reliability Engineering — Responsible for the device based upon customer requirements and defining its capability with respect to all potential failure mechanisms.

Although distinctively different disciplines, the three engineering departments interact continuously among themselves and with manufacturing and quality control to meet a common goal — reliable, cost-effective semiconductor devices.

Figure 1 is a flow chart showing the interaction of all of the engineering disciplines with other departments during product development, from initial planning to volume production. The purpose of this chart is to demonstrate to the reader that SSD has a well-defined procedure for reliability evaluation during the comprehensive product development cycle.

REL serves as a key integrating factor for reliability within SSD. Its responsibilities during product development may be stated as follows:

1. Definition of stress test program;
2. Evaluation of product to test program;
3. Definition of reliability assurance test conditions; and
4. Definition of real-time indicators.

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Final manuscript received Oct. 31, 1977.

The definition above is a multifaceted evaluation of the life, mechanical, and environmental capability of the product. Figure 2 shows a typical reliability test program.

Certainly one of the primary objectives of this evaluation program is to detect any potential inherent failure mechanism quickly and economically. This is done by developing and employing accelerated test methods at levels sufficient to generate a failure distribution. Reliability physics analysis is then employed to determine the basic cause of device failure and to develop models for future use in proposing process or device changes. As a result of these tests, REL is able to develop and institute real-time indicators (RTIs). These are highly accelerated tests used to control the reliability of the end product by in-process control. In this manner REL develops the reliability data base on all new devices prior to their introduction into manufacturing.

In addition to the above-mentioned responsibilities, REL has several other related objectives. The department conducts reliability evaluations of competitive products, evaluates unique customer reliability requirements, provides major customer support for all reliability programs and coordinates all external publications on reliability. In short, the department acts as the central investigative unit for SSD for all reliability-related issues.

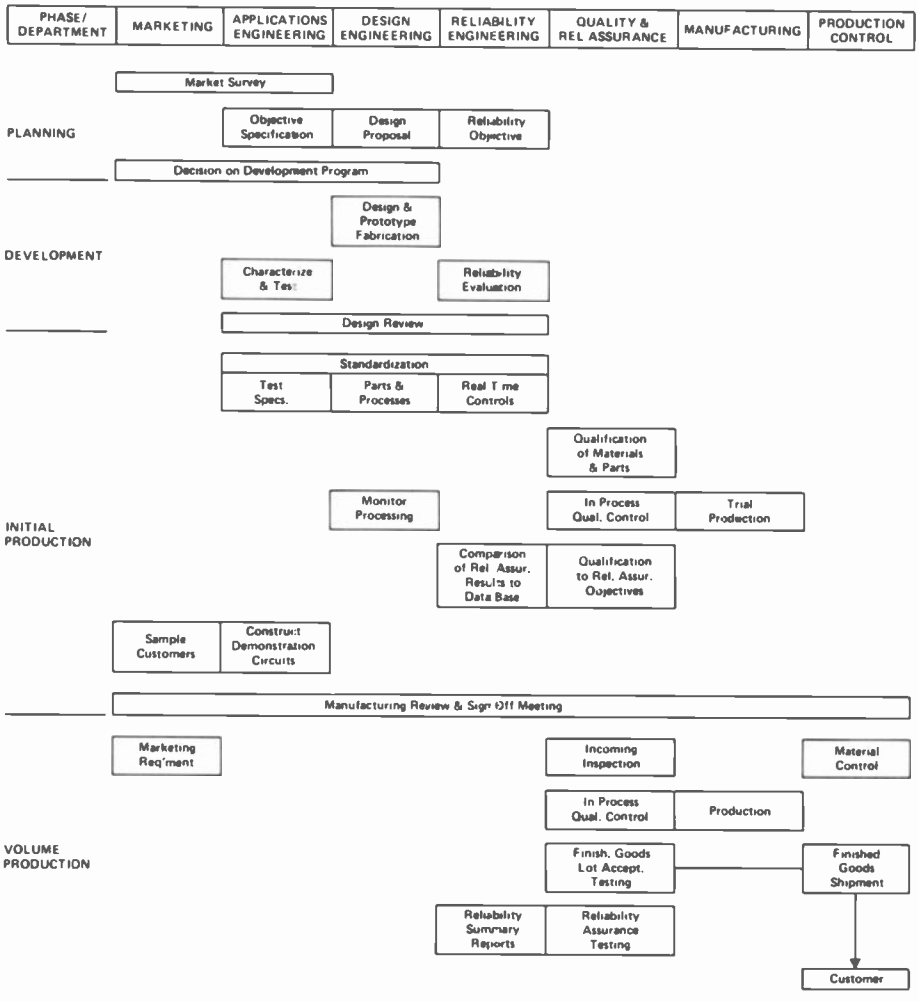


Fig. 1. All engineering disciplines interact with other departments during product development, from initial planning to volume production.

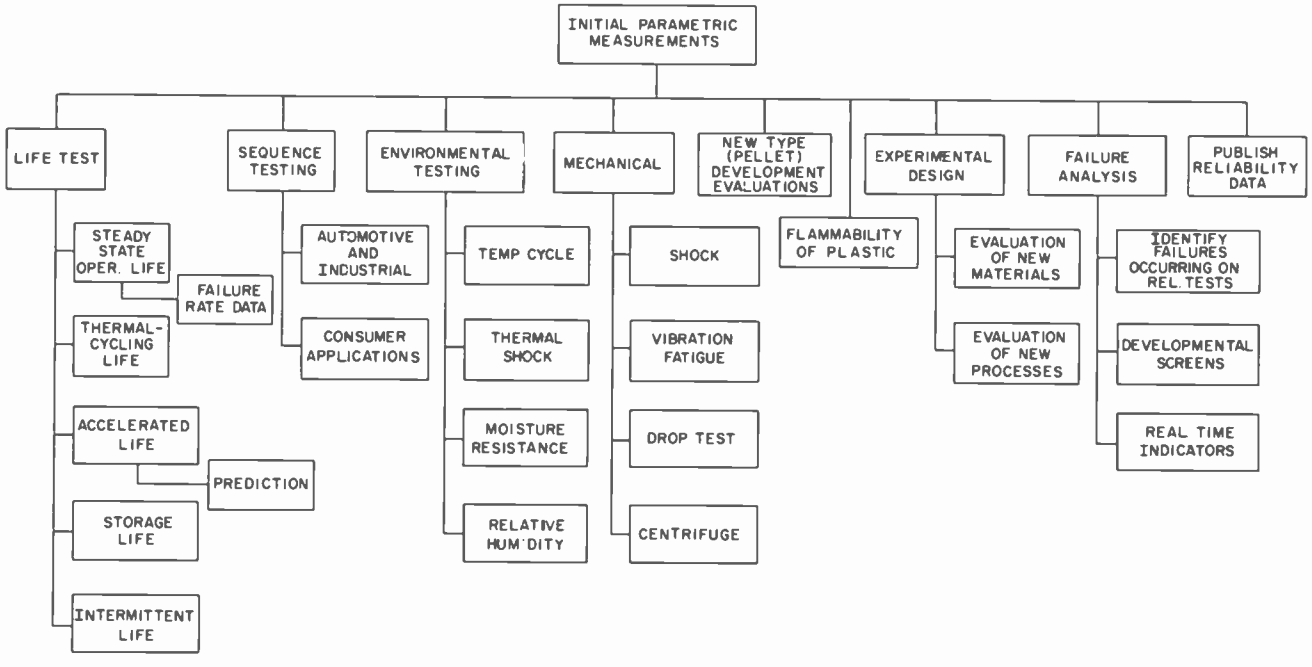


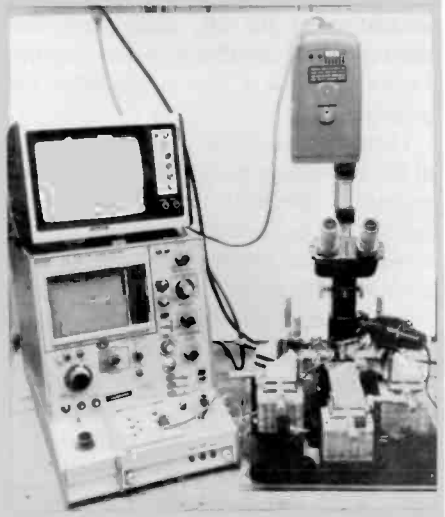
Fig. 2. Typical reliability test program.

A look at REL's test equipment.

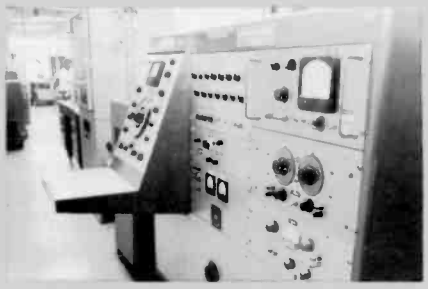
One of the pacing factors in the ability of the Reliability Engineering Laboratory (REL) to successfully evaluate SSD products is the availability of the necessary capital equipment. The photographs show examples of such equipment. Since its creation some ten years ago, REL has obtained a significant amount of equipment for use in mechanical, environmental and stress testing of solid state components. These funds have been justified by considering that one major customer field problem is more costly to the corporation than is the equipment. In fact, it has been estimated that the payback on capital and engineering expense for REL may be as high as 50 to 1.

A complete inventory of the REL equipment currently requires some 36 pages. Much of this covers life test boards which are unique to individual device types. The balance covers major equipment which falls into several generic classes. Some of this equipment is listed in the following table.

It should be stressed that equipment are only tools, which in themselves do not predict the reliability of a component. These tools, however, in the hands of a skilled reliability engineer may be used to predict useful life, to identify potential failure and wearout mechanisms, and to propose screens for potentially objectionable mechanisms.



Analytical and microsurgery probes used for device analysis.



Control panel for vibration variable frequency equipment.

Equipment for REL laboratory.

Generic Equipment	*Range of Operation*	*Use*	*Mil-Std 883B, Method*
Ovens	Room temperature to 343°C	High temperature bias and operating life tests.	1016, 1008.1 1005.2
Temperature chamber	-65°C to +175°C	High power dissipation operating life tests.	1005.2
Temperature cycling chamber	-65°C to +200°C	Air to air temperature cycling tests.	1010.2
Thermal shock	-70°C to 200°C	Liquid to liquid thermal shock tests.	1011.2
Humidity chamber	31°C to 93°C	Bias humidity tests.	1046.2 (Mil-Std 750)
Salt atm. chamber	35°C, salt solution as specified	Std and customized salt atmosphere tests.	1009.2
Salt spray	38°C, salt solution	Std and customized salt spray testing.	1046.2 (Mil-Std 750)
Autoclave (pressure cooker)	0 to 50 psig	Accelerated moisture testing.	
Moisture resistance chamber	-10°C to 90°C, cycled humidity controlled between 25°C and 65°C	Std and customized moisture resistance testing.	1004.2
Altitude chamber	Sea level to 30,000 ft., room temperature to +150°C		1001
Centrifuge	To 20,000 RPM, 30,000 G		2001.2
Mechanical shock machine	0.3 to 0.8 ms, up to 3,000 G		2002.2
Vibration, variable frequency	To 2,000 cycles, 25 G		2007.1
Vibration fatigue, 60 cycles	To 40 G		2005.1
Solderability equipment	To 300°C		2004.2

Len Gibbons has been Manager of the SSD Reliability Engineering Laboratory since August, 1978. He is a twenty-year veteran with RCA. Prior to his present position he held management positions in Discrete Power Applications and Thyristor Marketing. He is a member of the IEEE Reliability Society, Tau Beta Pi, and Eta Kappa Nu.

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J.E. Steoger

Quality measurement and control in a service environment

A new approach to service training and rating provides good quality service.

Abstract: *Measurement and control of service quality differ from those of production quality. The Service Company must approach quality control from a training and rating of technicians standpoint. This article describes some of the techniques used by the Service Company in television repair service for quality measurement and control.*

Organization of the Service Company

The RCA Service Company is a large organization providing a multitude of services to many kinds of customers. The Company is organized according to the kind of customer being served.

The Government Services Department is involved with federal, state and municipal agencies. Many kinds of services are offered to these customers including Technical Writing and Documentation, Systems and Field Engineering, Operations Research, Oceanographic, Curriculum Development and Education and Training.

Consumer Services is the department which is most familiar. It provides demand and contract service on products sold by the RCA Consumer Electronics Divisions; installs and services Whirlpool appliances; installs and services master antenna systems; and sells or leases television receivers, sound and communication systems, telephone equipment and other electronic systems developed for the hotel/motel, health care and educational markets.

The Technical Services Department serves many different kinds of customers not covered by the other two departments. The products range from airline reservations systems, broadcast transmitting and studio equipment, electron microscopes, satellite earth stations, theater equipment, and include leasing and servicing of teleprinters and video tape duplication.

Each of the major departments within the RCA Service Company operates independently and provides most of its own support services. Because of the very wide range of services provided, and the many kinds of products which are involved, the Service Company must have people on its payroll with a variety of abilities. The services require janitors, welders, machinists, clerical people, technical writers, educators, and engineers and scientists through the Ph.D. level in most of the technical disciplines.

There are many quality control methods used in these three departments; however, this paper will be limited to the control of television service quality. This is only one of many quality programs in use by the Consumer Services Department.

The techniques used for the measurement and control of quality of service differ in many respects from those used in a production environment. It is economically impossible to obtain accurate field data comparable to that with which quality control engineers are most familiar, so a major effort must be exerted to prevent a low-quality service from being produced at the outset and to collect such data that will permit determination of trends from the norm. The selection and training of employees are crucial to providing good service.

Training quality technicians

Our field technicians are represented by the International Brotherhood of Electrical Workers (IBEW). The union contract recognizes the fact that educational and experience levels will be distributed over a wide range, and categories and wage rates have been established to encourage the technicians to improve their technical knowledge and performance. A home study course has been developed, consisting of 40 lessons, to enable a technician to improve his knowledge. Incentive is provided by tying progression through the various steps and related rate increases to satisfactory completion of a specified number of home study lessons. An applicant's formal training and work experience determine the step at which he begins.

On-the-job training

An applicant who has no formal electronic schooling and no practical TV experience, but appears to have a potential for this type of work, would be hired into Step 1 (see Fig. 1)—the lowest category for technicians. One with appropriate school-

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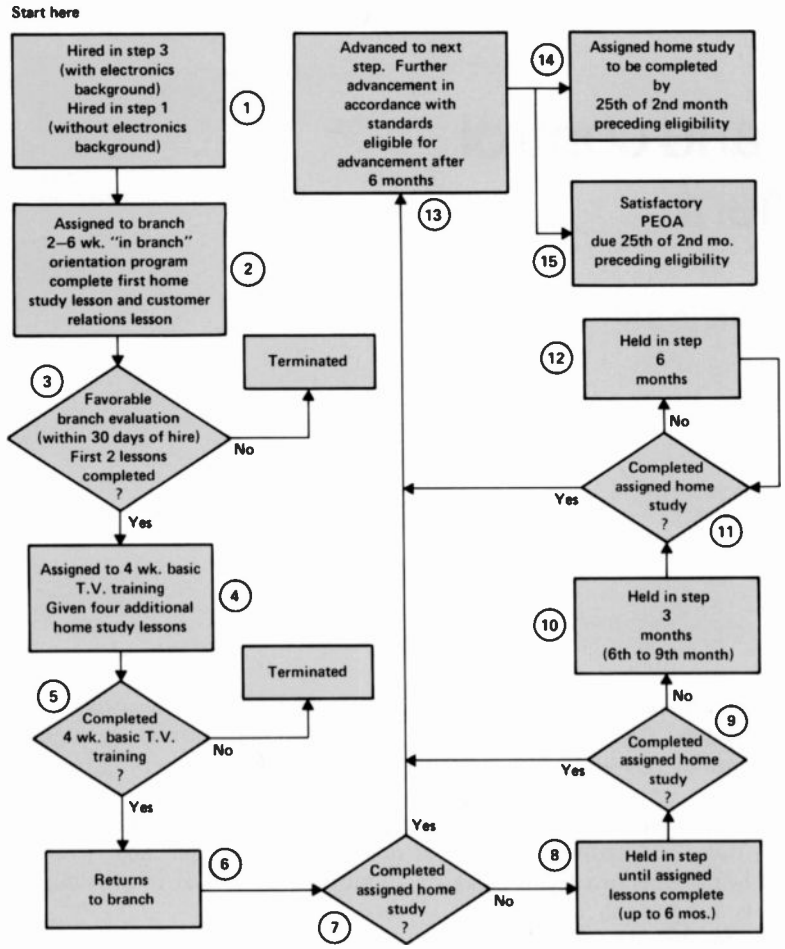

Fig. 1. Technicians hired into Step 3 must receive at least 40 hours of on-the-job training and complete home study lessons.

ing but no practical TV service experience would be placed in Step 3.

Technicians hired into these categories must receive at least 40 hours of on-the-job training (OJT) in a branch and complete certain prescribed home study lessons before being sent to an RCA Service Company Training Center for formal training. One of the lessons that must be completed is Customer Relations. On-the-job training includes accompanying a competent field service technician on field in-home TV service calls for one week. If time permits, supervised OJT may also include antenna installation, bench work and work with commercial products or telephone systems.

Apprentices who complete the pre-school OJT requirements and successfully complete the Customer Relations and initial technical home study lessons with a grade of 70 or better are given a pre-school interview. In this interview, the supervisor assesses the trainee's attitude toward pursuing the TV technical profession and, from a review of job exposure and home study performance, evaluates the trainee's potential to continue development as a TV technician. If the review is positive, a trainee registration for Basic TV Course is prepared and the trainee is sent to one of four training centers for four weeks of formal classroom and lab training (Fig. 2).

Upon return to the branch, the trainees must receive at least an additional 20 days of TV field service OJT during the next six month in a way which provides maximum support at the beginning of the period and gradually withdraws support through the period. An apprentice hired into Step 1, the lowest category, will normally require four years to complete all of the home study lessons and progress to Journeyman status.

Training centers

There are approximately 165 RCA Service Company Consumer Service branches located in major cities throughout the country (see Fig. 3). These branches are grouped into 14 districts and each district has a Field Service Administrator. One of the duties of a Field Service Administrator is to assist branch management with determination of training requirements. Each technician's performance is periodically reviewed and the need for further training is considered. In addition to the basic four week course, our training centers provide advanced courses such as Fundamental and Advanced Service Techniques, Bench Repair, VCR and Commercial Products.

Prior to release of new products, Field Service Administrators (FSA), Training Center Managers and other key personnel are trained by the Consumer Electronics staff in Indianapolis. The FSAs then set up short training programs in each branch to acquaint the technicians with the features of the new models and service techniques to be used in their repair.

A great deal of money is spent to insure the technical competence of technicians on the Service Company's payroll. Labor costs are rising rapidly and the Service Company branches must be provided with tools, test equipment and vehicles that will allow the technicians to perform most efficiently. All of these items are selected by the home office and must be approved before they may be purchased or used by the branches. Personnel safety becomes an important consideration in selection of power tools and ladders. Time is saved and product quality maintained through the use of only exact replacement parts supplied by the RCA Distributor and Special Products Division.

Rating technicians

Information obtained from branch weekly performance reports allows the Service Company to analyze the performance and quality of service rendered by every technician. The home office provides a computerized summary of performance to each branch on a monthly basis. All of the items affecting productivity and quality of service are shown. There is also a separate monthly performance record for each technician in the branch, and a "peel off" label containing these statistics is affixed to the record each month. This performance record is used for counselling purposes since performance trends are easily identified.

Several of the items included in the Performance Report are used to calculate the quality of service rendered by each technician. From the customer's standpoint, it is important that the service technician arrive at the approximate time promised and that the receiver be conclusively repaired on the first call without

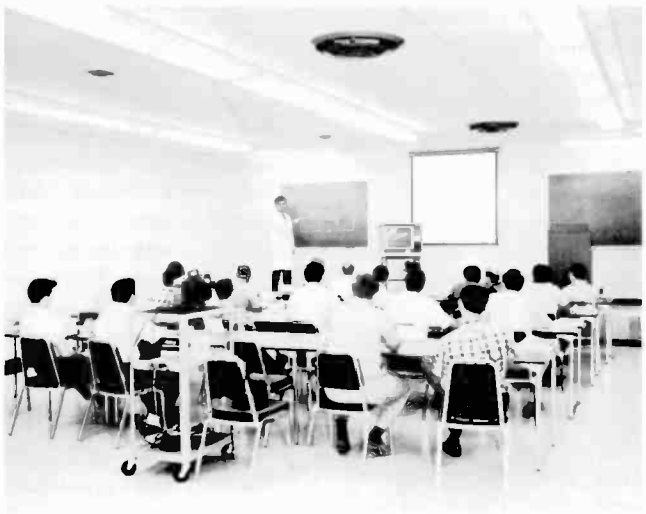

Fig. 2. If the trainee receives a positive pre-school interview, he is sent to one of four training centers for four weeks of formal classroom and laboratory training.

removing the chassis from the home for service. These needs are addressed in calculating the quality of service. Referring to Fig. 4, if the technician does not arrive at the approximate time promised, he receives a "not at home" rating. If he has not kept his parts kit complete, or has not analyzed the job card to draw needed special parts from the stock, he receives a "reschedule for parts" or a "chassis pull" rating. If the repairs are not properly made, his rating will be a "callback." If all goes well, he receives a "complete" rating. His quality % rating is then computed by:

$$\text{Quality } \% = \frac{\text{Net Completes}}{\text{Contacts}}$$

Summaries are listed by technician for branch use, by branch and district for regional analysis, and by district and region for comparison with national averages.

The Service Company is very sensitive to the way branches handle incoming service requests. The customer may not be in the best frame of mind when the service call is placed, and if the telephone clerk is not pleasant and diplomatic, it is going to be that much more difficult for the service technician to complete the job and leave a happy customer.

There is an employee in the home office who calls each branch at least twice a year, posing as a local customer needing service on a TV receiver. At least one Sears, one GE, and a large independent in the area are called at the same time. Each area is surveyed as fast as possible on the same day. The length of time required to answer the call is logged; how the call is answered; whether the telephone clerk was pleasant in her response; how soon a service call could be scheduled; if service could not be delivered promptly, what sort of excuse was used; how charges were explained; whether credit cards would be accepted; and whether evening or Saturday service could be scheduled.

Fig. 3. There are approximately 165 RCA Service Company Consumer Service branches located in major cities throughout the country.

Service quality vs. production quality

The measurement of quality of service includes many factors not present in the manufacture of a product, which are subjective, not needed for controlling the manufacture of a "thing," or getting it through final test and onto a truck. The Service Company is dealing directly with customers and they may feel that the service rendered is of poor quality, even though the serviceman has satisfactorily repaired the product. Some of the techniques and controls may appear crude but they work. Statistics must be adequate to get to the root of a problem so corrective action may be taken. The reports generated make it very easy to identify trends.

The Service Company has television

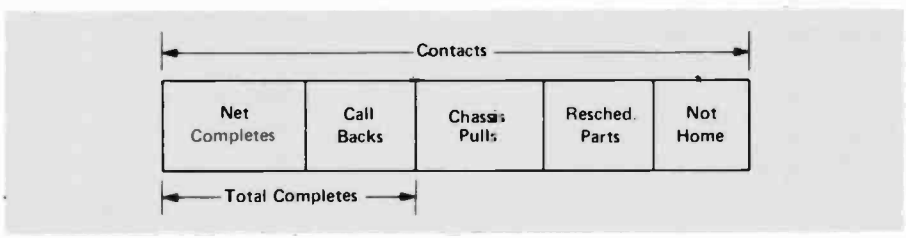

Fig. 4. The customer's needs are addressed in calculating the quality of service.

receivers under lease to hotels, motels and hospitals. This gives another opportunity to measure customer satisfaction with products and with service. Once a year a Satisfaction Survey Card is mailed to each lease customer. Every card returned is acknowledged by the Commercial Sales Department and, if problems exist, they are forwarded to the cognizant District Manager for corrective action.

Handling complaints

With over a million service contracts in force, 2,600,000 service calls are being made a year. That is one service call every eleven seconds. The Consumer Affairs Department receives complaints and inquiries from branch customers by letter or telephone calls. Complaints are coded, logged and sent to the branch with a report form. All letters are acknowledged in writing — usually within 24 hours. Consumer Affairs pursues the case until the report is received from the branch indicating that the complaint was resolved to the customer's satisfaction. When reports are not received by the end of the following month, the case is entered on the Overdue Report. The information recorded in the log book is used to prepare a weekly and monthly report so that management can monitor the complaint situation.

The Weekly Complaint Report segregates the complaints several different ways for analysis. Complaints are listed by product line — television, appliances, VCRs, telephone systems and all other. Television complaint ratios are charted for a 12-week period and historical data are included to compare current performance with that of similar periods in the prior two years. The present goal is 0.14 complaints per 100 exposures. The 10 worst performing branches in the current week are listed and their 12-month averages are shown for comparison. Another section lists the poorest performing branches based on 12-month averages. Replacement parts problems are shown in another section of the Weekly Report.

Visibility is a very important element of a quality control program. The distribution list for the Complaint Report includes E.H. Griffiths, and this gives about the ultimate in visibility.

Conclusion

The following definition of quality assurance describes the Service Company's goals: A management discipline consisting of a planned and systematic program covering all functions and actions necessary to provide adequate confidence that the end item or service will perform satisfactorily in actual operation, thereby assuring customer satisfaction, customer confidence, new business and a profitable company.

Joe Steoger joined RCA in 1942 as a Field Engineer for the RCA Manufacturing Company. After serving in various other capacities, he was made Operations Manager, Technical Products Department, for the Service Company in 1963. He now holds the position of Manager, Consumer Services Engineering Support, and acts as a liaison between the Service Company and the Engineering Departments of other RCA Divisions and outside vendors.

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Reprint book on Picture Tube Technology to be published in March 1980

A reprint featuring picture-tube articles from the *RCA Engineer* will be printed in early March. This issue will contain about 20 articles written by RCA scientists and engineers on the following topics:

1. **Business profiles**—a discussion of the color television picture-tube market from a worldwide perspective.
2. **History**—a chronology of picture-tube development at RCA.
3. **Technology surveys**—recent trends in color picture-tube design and major developments in phosphors and screen-application techniques.
4. **Elements**—filter phosphors, high-resolution bipotential-focus guns, precision in-line shadow masks and contoured-line screens.
5. **Techniques**—for measurement of cathode temperatures, rapid-scan determination of optical spectra, evaluation of test results from small data groups, and x-radiation measurement and control.
6. **Manufacturing**—equipment development, use of microcomputers, and prototype manufacturing in research and development.
7. **Glass making**—Circleville glass making and computer usage in a glass-forming operation.

To place advance orders for this reprint, send your request to *RCA Engineer*, Bldg. 204-2, Cherry Hill, N.J., attention of Dorothy Snyder. The approximate cost of the picture-tube reprint is $2.75 per copy.

S. Schreier|P.W. DeBaylo

Quality assurance: measurement and action

A customer-oriented quality service program at Americom provides new levels of optimum service.

Abstract: *RCA's domesic communications satellite system provides a wide variety of services to many different users. This diversity and customer orientation created a challenge for reliability and quality assurance: to design and develop a program that would assimilate all performance data into a system for measuring the quality of the services provided. These efforts resulted in a system, unique in the industry, which provides a vehicle for corrective actions and continuous improvements.*

Introduction

Satellite technology, opening up a new era in domestic communications, allows for highly reliable video, program audio, voice and data transmissions at lower costs than previously available. RCA Americom is a service-oriented company, providing common carrier communications to the contiguous 48 states, Alaska and Hawaii, through the operation of its own spacecraft and ground communications network.

Rigorous quality assurance procedures are enforced during the spacecraft production and test phases to maximize the reliability of the orbital segment.[1] Once launched, the integrity of the communications service is largely dependent upon: 1. the reliability, configuration and maintenance of the ground equipment; 2. the expertise of field technicians and management in performing speedy trouble detection and fault correction; and 3. the support provided by the other companies involved in a segment of the end-to-end service.

The quality assurance aspects of a service industry are significantly different from those found in manufacturing. In a service industry, quality is often merely a subjective evaluation by a customer, intangible and difficult to measure, while performance standards are not always available. Trouble sources are not localized and can be at the near or distant end, or with other carrier equipment which is largely beyond Americom's control. There is also a large degree of customer/technician interaction during both trouble detection and correction.

In a service industry, conventional reliability and quality assurance concepts must be addressed from the customer's vantage point in order to maximize service availability. A service-oriented approach for trouble collection, analysis, measuring, reporting and service improvement was designed by Americom's reliability and quality assurance (R&QA) group to fit the characteristics and needs of its provided services. While some of the measurements and techniques are unique to the communications industry, the approach and methods to be described may be useful to other service companies within the RCA Corporation.

Satcom system — an overview

Americom inaugurated communications services in December 1973, using leased transponder space, and now owns and operates two, 24 transponder, C-band spacecraft.[2]

The ground segment of the SATCOM network consists of six Americom owned and operated commercial earth stations; terrestrial microwave hops between the earth stations and the central telecommunications offices (CTO) in the nearby urban areas; and some 20 dedicated earth stations, primarily providing leased communications services directly to the various government agencies (e.g., NASA, NOAA/NESS, DOD). At the CTOs, Americom interfaces with the local telephone company land lines which provide communications directly to the customer's office. Two fully redundant spacecraft control centers, co-located at the Vernon Valley and South Mountain earth stations, are also part of the system capable of sending commands to each spacecraft, receiving telemetry, performing ranging, and tracking data, and providing overall spacecraft control.

A variety of services is available to customers with the present SATCOM system. These include: 1. network quality commercial television distribution from TV studio-to-studio; 2. cable television distribution from a studio or an earh station to multi-point, receive-only earth stations; 3. program audio distribution from a studio directly to the audio broad-

This paper was condensed from an unpublished manuscript of the same title. For details contact the authors.

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Final manuscript received Oct..

Americom's customer service center

All troubles that occur on a private lease channel, voice grade service, are reported by the customer, via a toll free number, directly to Americom's Customer Service Center (CSC). The CSC coordinates and tracks the troubleshooting, summarizes outage information, and keeps the customer informed as to what actions are being taken.

It is Americom's policy that all customers are to be called back with the status of their trouble, and that 95 percent of these calls are to be made within two hours. Initially, only 82 percent of the callbacks were made and only 69 percent were within the two hour time frame. A quality measurement system was established, and through visibility and dedication of the CSC personnel, callback performance has increased to be consistently better than 99 percent in both areas.

casters; 4. leased channel, medium and high speed digital data transmission from one dedicated earth station to another; and 5. voice grade, FDM-fm, private leased channel services, from one customer office to another. Each spacecraft transponder can simultaneously accommodate a large mixture of these services, depending upon their bandwidth, frequency and power requirements. This capability has been previously described in an *RCA Engineer* article.[3]

A typical voice grade service flow is depicted in Fig. 1. Telephone/data message signals are forwarded from a customer's office (e.g., New York City), via a New York Telephone company land line to Americom's New York CTO on Broad Street. The signal is processed, multiplexed into supergroups, and transmitted via terrestrial microwave to the local New York earth station at Vernon Valley, New Jersey. There, the signal is upconverted/modulated with a specific 6-GHz carrier and transmitted to a transponder in a SATCOM spacecraft.

On the downlink, the signal is frequency translated to 4 GHz, amplified and retransmitted with similar downlink distribution, reversing the process.

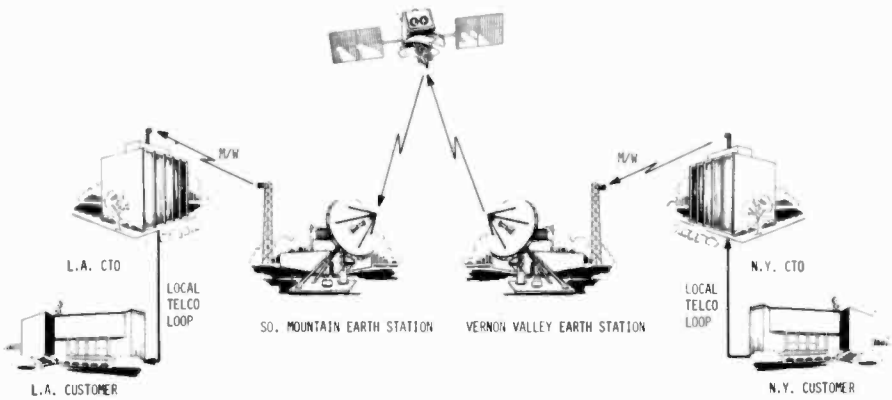


Fig. 1. Americom's typical private leased channel operation and signal distribution provides voice-grade service flow.

Service quality program

Translation of traditional quality assurance techniques to a diverse communications service industry presented a significant challenge. Groundwork for the establishment of service performance requirements, the measurement of availability, and the seeking of service improvement began as early as 1975. In mid-1977, a formalized R&QA organization was established at Americom, working across the board in support of engineering, operations and marketing.

As a service company, Americom does not manufacture the equipment utilized at its multiple operational centers. In addition, Americom performs only a limited amount of its own equipment installations. Its prime engineering functions are systems design, specification, frequency coordination, procurement, and monitoring of implementation by "turn-key" vendors. The majority of its technical people are thus engaged in the daily operations and maintenance of its wholly-owned earth stations, microwave, CTO and spacecraft facilities.

The quality system developed had two objectives. First, procedures and practices have been established to influence design, specification, procurement, and implementation activities. These efforts are along the more traditional lines of vendor quality programs, availability modeling, design reviews and acceptance testing, directed at minimizing infant mortalities and the improvement of long-term reliability. The second objective was the establishment of a trouble reporting/corrective action (TR/CA) system for measuring operational performance, analyzing the data, and recommending corrective/preventive actions. Outputs from the system: 1. provide for the detection of recurring problems with hardware, procedures and/or personnel; 2. provide

data for detailed failure analyses/investigations; 3. provide information to support trouble discussion with vendors or other common carriers; and perhaps most important, 4. inform top management of how well this system is or is not performing. This management visibility of all quality reports and efforts is a potent quality improvement tool.

This second activity, the establishment of a TR/CA system, will be the focus for the remainder of this paper.

Trouble reporting/corrective action system

A portion of the total quality system is built around the reporting of a trouble and the corrective actions taken. Reporting of troubles has been formalized, as a tool for operations and R&QA, by the recording of pertinent trouble information on a trouble report, hereafter called a TR/CA. The TR/CA is initiated as soon as a trouble has been reported, and is completed when the trouble has been cleared and all actions have been taken. Key features that this system provides are:

- A standardized means for documenting all trouble within the SATCOM system.
- A closed-loop corrective action system, emphasizing timely resolution and preventive actions.
- A data base for trend analyses, reliability/maintainability determination, pursuance of corrective actions with vendors, determination of customer credits.
- A computerization of all field TR/CAs for management reports and data access.

Trouble complaint sources

Troubles in the space segment are detected via continuous monitor of a telemetry stream providing health and status information to video displays and computers for automatic fault detection and alarming. All troubles or apparent anomalies are noted immediately, and a TR/CA generated to document the problem and provide a vehicle for its resolution (Fig. 2).

Most troubles that occur with equipment at the commercial or government dedicated earth stations or microwave sites are also detectable visually and via alarms. Some sites are fully redundant and service is restored by automatic switch-over once a fault is detected. At other sites, manual intervention is required, which can result in slightly longer outages. TR/CAs are generated by the site technician responsible for the maintenance of the equipment at fault or the services provided.

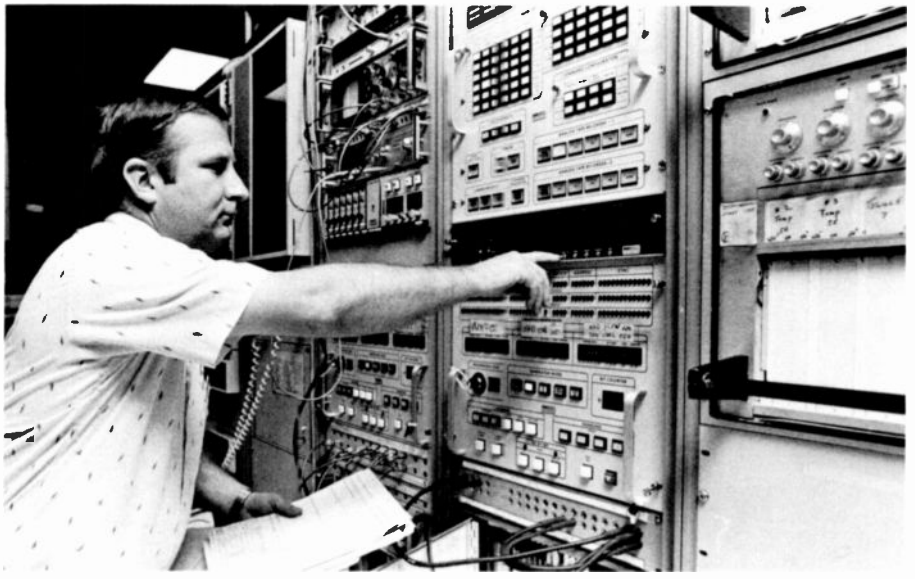


Fig. 2. T.P. Tubbs monitors a data modem at Vernon Valley earth station while filling out a trouble report/corrective action report form.

For private leased channel services, the TR/CA is usually generated as a result of a customer's advising Americom about service quality. Troubles are reported to Americom's Customer Service Center (CSC) at headquarters. In addition, there are several other sources for detecting trouble. These include various Americom entities: CTO, earth station, marketing personnel, customer representative engineer (CRE), a traffic recorder located in the CTO, as well as another connecting carrier, commonly called a telephone company (Telco), and the customer's equipment vendor.

Measurement of quality

Definitions

The basic measurements of quality of service or performance at Americom are Availability and Untroubled Service. *Availability* is defined as uninterrupted operating time divided by scheduled operating time, expressed as a percentage. It is concerned solely with troubles that cause interruptions of service. *Untroubled Service* is defined as trouble-free time divided by scheduled operating time. It encompasses impairments of service as well as interruptions. All troubles that are within Americom's responsibility are classified into either of these two categories. Customer-caused troubles are not within Americom's responsibility and are not included in the measurement of service quality.

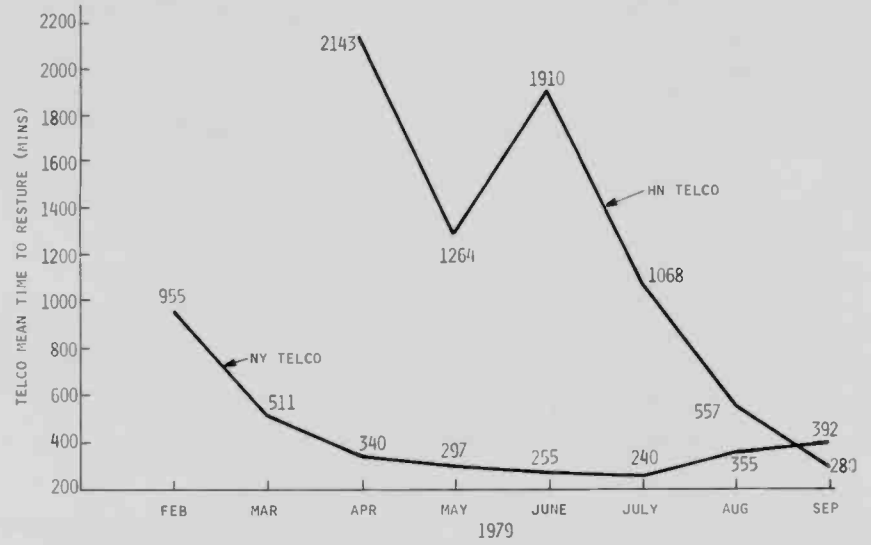
Trouble data review

Each TR/CA is reviewed by R&QA, edited, summary information added, and the pertinent trouble information abstracted and posted on various statistical sheets and/or readied for data processing. The summarization of the data, monthly, weekly, or on demand, the analysis of the results, the comparison to past results, all combine to form the process of the measurement of the quality of service. Measurement is followed by publishing of the quality data in reports distributed to various levels of company management, and initiation of preventive action efforts involving the appropriate groups within and outside the company, when applicable.

Quality standards

A measurement system needs limits or goals against which the measured performance can be compared in order to flag the problem areas and alert operations that some action is necessary. The quality standards used at Americom (Table I) represent average minimum acceptable performance levels. They have been developed from empirical data and adjusted upward over the years as performance has improved. Service standards are also provided to marketing for their use in developing prospective customers.

Influence of TELCO on leased channel quality



New York and Houston TELCO mean time to restore service improvement.

Typically, between 70 and 90 percent of the private leased channel (PLC) outage minutes were attributable to the telephone company and, thus, were thought to be beyond Americom's control. A concerted effort was launched in 1977 to monitor and define the impact of TELCO on PLC availability. Data were collected and presented to New York TELCO, and later, to other regional telephone companies, with insistence that their performance improve. Monthly meetings, with the business relations groups within TELCO and Americom's Operations and R&QA personnel, resulted in commitments to improve services. Through added staff at TELCO and some hardware modifications, a significant improvement in mean time to restore was achieved.

Monthly comparison of other carrier performance during 1979. Mean time to restore (min)/number of interruptions of service.

Carrier	*May*	*Apr.*	*Feb.*
NY TEL	297/51	340/61	955/50
PTT-SF	172/15	286/9	298/7
PTT-LA	274/20	214/10	403/8
ILL BELL	362/20	567/16	383/11
HN BELL	1264/27	2143/22	313/14
CA BELL	658/3	123/2	208/4

Table I. Service/facility performance standards.

	Availability (%)	*Untroubled service* (%)
System	99.75	99.67
PLC	99.68	99.62
GLC	99.80	99.70
CTO	99.84	99.81
Spacecraft	99.99	—
Earth station (commercial)	99.96	—
Earth station (government)	99.90	—
Microwave	99.99	—
TV	99.99	—
Transponder	99.99	—
Program audio	99.90	—

Service quality — visibility, action, improvement

A system of reporting and analysis has been designed to measure and evaluate the various components that combine to provide Americom's quality of service. Measured performance is published monthly in two basic reports: a quality of service report, presented in chart form graphically depicting individual service and system performance, and an earth station/microwave/spacecraft TR/CA summary, directed primarily at equipment and operations problems in the field. Both documents are issued to all levels of management within the company and selected portions are used as part of a monthly business review presentation to corporate management.

Providing quality information is not sufficient in itself to bring about improvement. Action, corrective and preventive, based on the quality information, must be sought after on a routine and regular basis from the various groups responsible for the performance. R&QA works with the engineering and operations groups, providing early warnings, reminders, and measurement of the effectiveness of the actions taken by these groups. Persuasion by R&QA must be persistent and consistent so that significant actions are designed and taken to reduce the number of recurring quality problems that cause service quality to deteriorate.

Leased channel (L/C) performance

System performance, combining private and government-leased channel services, is graphically tracked and shown in Fig. 3. The dramatic improvement in performance over the last several years is attributable to the combined efforts of Operations, Telco and R&QA. Equally as significant, is the convergence of the availability and untroubled service plots, the latter being the customer's true perception of his performance since it is the combination of all problems. This improvement is felt to be the result of better education on the customer's part in determining the quality of their service, and improved technology introduced by Americom in the industry (e.g., echo cancellers).

A variety of summaries are published each month depicting individual L/C performance. These show the availability for each channel operating below our standard for the month, for the current month and one of the two previous months, and show availability for PLC customers with groups of channels. Interruptions and outage minutes are categorized and tracked graphically by trouble location as shown in Fig. 4. Government LC quality performance is also compared with the competition, as extracted from NASA's monthly quality publication *NASCOM Network Ground Communications Availability Report*. For similar routes, Americom's services are, in general, equal to or better than the other carriers listed.

Performance of operating groups

Measurement of job performance is necessary in an operational environment since it is the combined efforts of man and machine that provide our communication services. Performance is measured on a

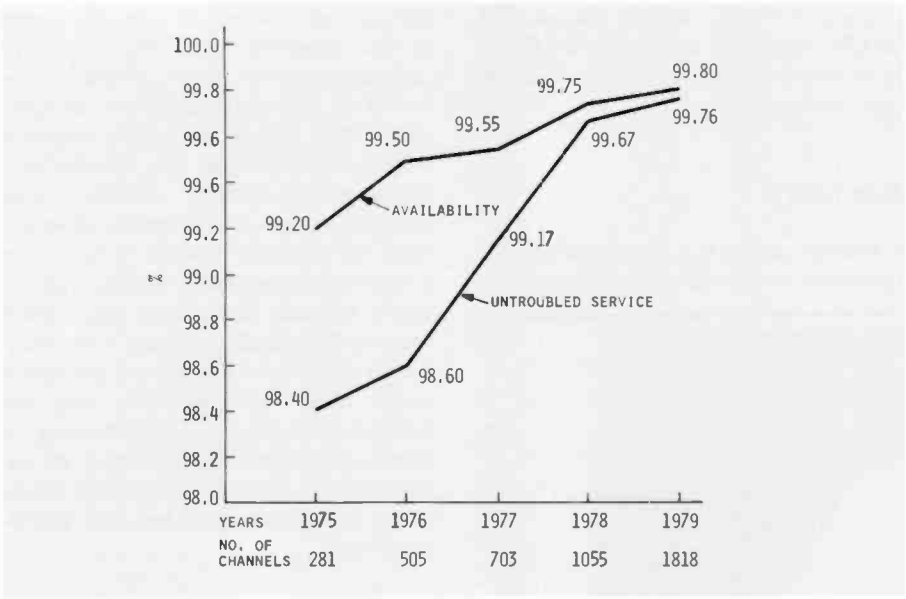


Fig. 3. This system leased channel performance graph combines government and private services.

group basis to avoid finger pointing at any individual. The groups that are monitored monthly are the CTOs, CSC, Telcos, earth stations and spacecraft.

Each of the operating groups is measured to determine the mean time to restore service for troubles it was involved with, giving insight to management as to the quality of the staff, responsiveness to customers, and the adequacy of the tools and procedures used during troubleshooting and repair. Data summaries are also provided, indicating the cause of interruptions that resulted in below standard performance. Combined, this performance visibility allows operations to take preventive actions, reducing the likelihood of troubles in the future and, when they occur, to be prepared to minimize the effect upon service.

Trouble analysis

Data collected via the TR/CA system have proven to be invaluable to R&QA and operations in analyzing equipment failures for trends and generic failure modes. Results of these evaluations have been used for discussing corrective actions with vendors; influencing hardware selection and specification in future procurements; making field improvements in operating environment, equipment location, and maintenance procedures; and reducing operating costs. For example, a recurring trouble with a low power driver amplifier used in an uplink was isolated by failure analysis to an IMPATT diode wear-out failure mechanism. Since four diodes are used in each unit, it was determined to be more economical to replace the failed units with an improved design instead of performing the repairs. Similar improvements have been realized with low-noise receivers, test equipments, and data modems.

Trend studies also have influenced procedural problems and facility requirements. Several problems with backup power systems were related to the lack of preventive maintenance schedules and practices. As a result, detailed procedures were generated by our facilities activity as a result and are now in use. In the same area, commercial power failures have been monitored at each location and cost-effective recommendations have been made for additions of backup power systems.

Problems with operational equipment or facility design are formalized by translation into a discrepancy report. This report provides a vehicle for obtaining funding and for implementing required corrections. Emphasis has been placed upon resolution of discrepancies that have a direct impact on operational performance.

R&QA in the near future

The ability of R&QA to continue in its efforts to develop new techniques and to improve services is challenged by Americom's rapid growth. Not only does the large increase in the number of leased channels (and the corresponding numbers of troubles) have to be accommodated, but R&QA must also expand its efforts to better support the growing TV and program audio product lines. Operational excellence must not be compromised during these periods of service expansion.

Accordingly, R&QA has taken the necessary first steps to improve efficiency

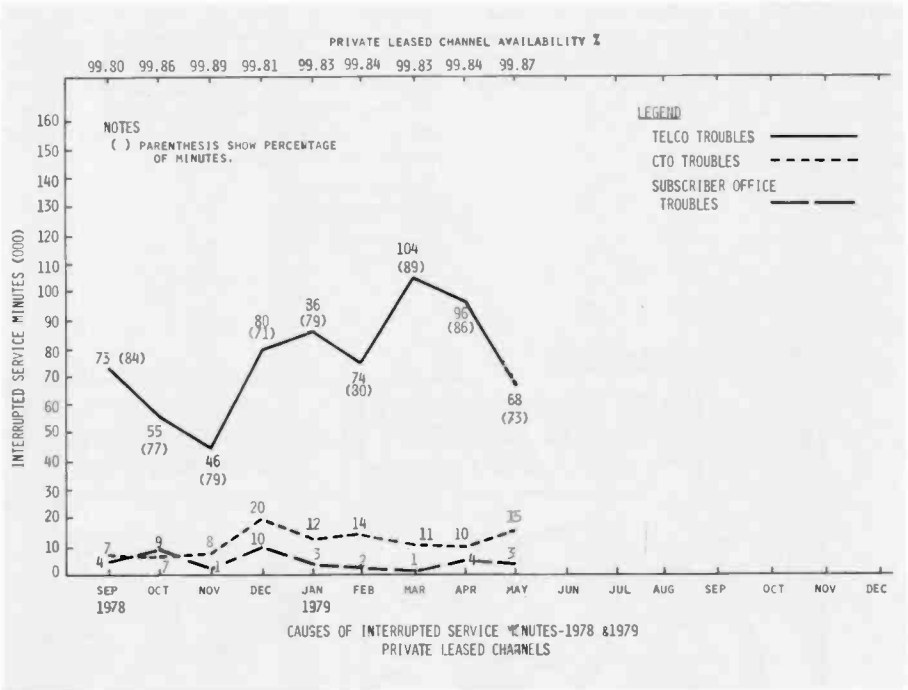


Fig. 4. Interruptions and outage minutes are categorized and tracked graphically by trouble location (1978 and 1979).

and prevent service quality from deteriorating. A formal vendor quality function was established to handle the large volume of new equipment procurements. Efforts have also begun to automate the TR/CA reporting system in the CTO and CSC. This latter program, when computerized, will reduce much of the manual effort currently expended by R&QA, provide the quality information on a more timely basis, result in efficiencies at the CTO and CSC, and enable R&QA to fill in some of the quality gaps that still exist in Americom.

Summary

A quality system has been developed at Americom to provide a means for measuring the performance of communication services provided to a wide range of customers, and for making problem areas visible to technical operations management. What makes this system unique is that it departs from the conventional manufacturing-oriented quality techniques and monitors the quality of service from the customer's point of view. The formal trouble reporting/corrective action system contains all pertinent information required to analyze the cause of the trouble, its effect upon service, and provides a useful tool for operations and the marketing functions. Improvements in service have been dramatic and are attributable to the mutual cooperation and dedication of the operations and R&QA functions.

Paul DeBaylo, standing, and Saul Schreier analyze performance information.

Saul Schreier is Senior Member, Engineering staff, Reliability and Quality Assurance group, at RCA Americom. He was instrumental in developing the trouble reporting and quality measuring system described and continues to utilize and maintain them for all the product lines. Previously, he was with RCA Globcom where he also developed and maintained their product line trouble reporting and quality measuring system.

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Paul DeBaylo is presently Manager of Reliability and Quality Assurance for the Technical Operations Department within RCA Americom. He is responsible for the assurance of spacecraft reliability and for the establishment/implementation of programs to measure and improve the availability of communication services. Paul joined RCA in 1975 as Resident Systems Engineer at RCA-Astro Electronics during the development, testing, launch, and in-orbit evaluation phases of the F1/F2 spacecraft program.

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Acknowledgments

The improvements, in service quality described, are not the result of any one individual or group, but rather attributable to the concerted efforts of each member of the Technical Operations Department, both at headquarters and in the field. Each member's dedication and support during the first difficult years of Americom's existence is commendable.

The authors also wish to thank J. Connelly for his graphics assistance, and E. Blount for typing the many drafts of this paper.

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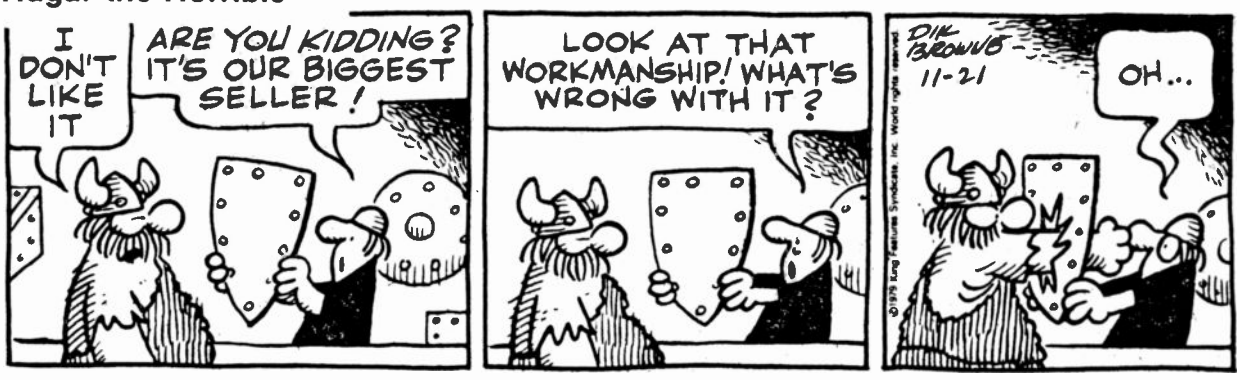
Hagar the Horrible



W.E. Bradley|G.J. Buchko

Do MIL spec quality systems pay off in the commercial world?

Incorporating MIL quality control standards in commercial systems pays in dollars and in customer satisfaction.

Abstract: *RCA Lancaster designed and is producing a high-power, integral cavity triode amplifier according to MIL specification quality control standards. During this process, it was found that incorporating the MIL standards into production of commercial manufacturing systems provided a good system for setting and maintaining quality control standards. This article describes how the MIL standards are being used in commercial systems and the end results of using these standards.*

In June 1958, Rome Air Development Center awarded a contract to RCA Lancaster to design and develop a high-power, integral cavity triode amplifier operating in the 400-MHz range at a peak power level of over 1 megawatt at a 10 percent bandwidth. Over the next thirteen years, various development contracts were awarded to Lancaster to complete the design and the development of this amplifier. These contracts culminated with the first production contract from General Electric, Utica, New York, in June 1971.

Background

The system developed was the Coaxitron Amplifier which consists of an RCA 4668 Coaxitron Tube, an RCA Y1143 Driver Input Circuit Assembly, and an RCA 4655 Cermolox Driver Tube (Figs. 1 and 2). The cost of a Coaxitron Amplifier is roughly $100,000 per unit. This complete unit becomes the final amplifier in the GE APS-125 radar set. GE supplies the radar to Grumman Aircraft who in turn supplies the U.S. Navy as the prime contractor for the E2C Fleet Air Defense Weapons System.

This amplifier unit was unique in its design features, and it required a unique quality system. That is, most products produced at the Lancaster location are commercial products and are produced using standard commercial quality practices. The quality system specified in the contract for the Coaxitron program is a customer standard patterned after MIL-Q-9858. In addition, MIL standards dealing with special processes were specified. This system required closer tracking of materials, parts, and procedures than the commercial systems in use, resulting in the development and implementation of new quality systems. These systems included a traceability system for materials, parts, and subassemblies.

When the first production units were placed in service, major quality and reliability problems were encountered. Many of these problems were systems interface oriented, but failure analysis of units indicated many possible failure modes caused by either imperfect design, manufacturing difficulties, or part problems. The normal corrective action cycle for this project was proven to be too slow in keeping up with the field problems. During the period from December 1971 to May 1973, it became evident that major changes were needed in every phase of the program from field personnel training to parts tolerances changes.

Developing the quality system

In a joint GE-RCA audit of all phases of manufacturing, conducted in May 1973, specific areas of concern were noted, management support obtained, a plan was developed to solve problems in these areas

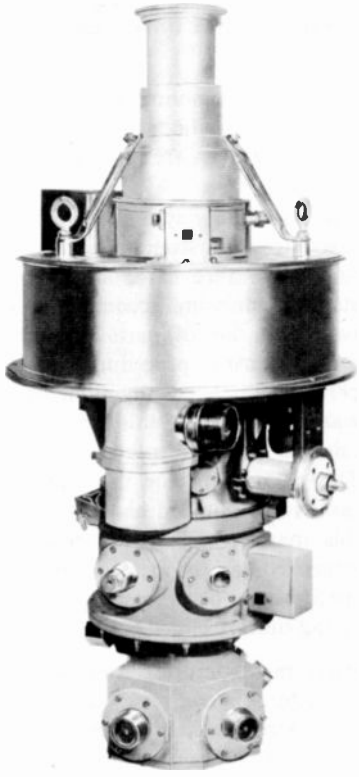


Fig. 1. The Coaxitron Amplifier is a high-power, integral cavity triode amplifier.

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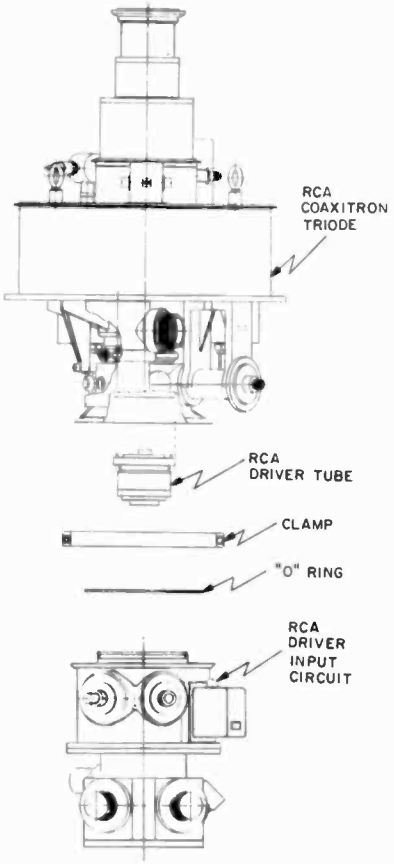

Fig. 2. The Coaxitron Amplifier consists of an RCA 4668 Coaxitron Tube, an RCA Y1143 Driver Input Circuit Assembly, and an RCA 4655 Cermolox Driver Tube.

of concern, and personnel were reassigned to accomplish specific tasks.

Tasks undertaken are listed below:

1. The traceability system for parts and assemblies was strengthened. In addition to a trace card, an up-to-date standard drawing accompanied each part or a lot of parts through the manufacturing procedure. As each person completed any dimension, it was recorded on this drawing and initialed by the respective individual. The parts inspector then added his results and initialed his recordings. In this manner, quality awareness was improved and the incidence of out-of-specification parts reaching manufacturing units declined.
2. Parts manufacturing and inspection procedures were reviewed, updated, and strengthened. New facilities and/or tooling were requested and obtained as required.
3. Flow diagrams for all major subassemblies were drawn.
4. Each subassembly manufacturing procedure and each part specification in the subassembly was reviewed by a joint quality and reliability assurance (Q&RA), Engineering, and Manufacturing team. The individuals involved in manufacturing each assembly participated in this review. Procedures were written, as far as possible, in a language easily understood by all. In some complicated subassemblies, two or three updates were necessary before final completion. Each procedure contains inspection points and quality audit points. No material may be processed past these points without quality acceptance.

   The engineering standards system used to document parts and procedures and its associated change control system was reviewed and found to be too slow for the rapidly moving program. To speed the system and improve its control features, several changes were adopted. All engineering changes were given priority in the system and were hand carried for approval or approved in group meetings. Handwritten approved copies of standards were filed in work areas and utilized until "clean copy" could be produced by the system. A list of applicable standards and their latest revision status, called the "Effectivity List," was developed and issued each time engineering standards were updated. In this way, all persons using standards knew the current revision level on a timely basis.
5. The three subassembly areas were supplied with travel tickets for every subassembly fabricated and their usage explained to those involved. All personnel were cautioned that only documented procedures would be used to fabricate and test subassemblies. In-process auditing by Quality persons reinforced this position.
6. Yield charts maintained by hourly personnel were instituted in all manufacturing areas.
7. A complete, formal system of audit stations was written based on the new manufacturing procedure. These audit stations detail quality requirements and are administered by Quality technicians. Manufacturing in-process audit stations are in reality Quality inspection gates. Material does not continue in the manufacturing flow until formally approved by the Quality activity.

   Specific audits were also written for any special process employed in this program such as heat treating, brazing, welding, painting, plating, and aluminum sand castings. These audits are done to assure conformance to required MIL standards.
8. The nonconforming material system used by each involved department was reviewed and strengthened.
9. First level management reporting was begun, including results of each month's audits and each month's yield. An additional bi-monthly report of electrical test, data trends, yields, and nonconforming material content of each unit was issued to higher levels of management.
10. A specific "Coaxitron Quality Manual," which supplemented the Lancaster Quality Manual, was issued containing all systems unique to this project and detailed each of them with flow diagrams.
11. A formal system of failure analysis/corrective action was instituted. The system provided immediate feedback from failure analysis to all interested activities, including Engineering, Manufacturing, and Quality, in addition to the customers, GE, Grumman, and the Navy.
12. Customer surveillance by GE was increased to audit overall quality and manufacturing systems' performance and hardware performance during testing.

Establishing measurements

A necessary part of establishing or expanding any system is the ability to measure the results of the changes using whatever criteria are necessary and/or available. When the decision was made to implement more far-reaching systems than previously used in this program, a number of criteria outlined below were selected for measurement.

Reliability growth curve

Data for the field usage is collected by the user, the U.S. Navy, and returned through GE to RCA.

Figure 3 is a plot of mean time between failures (MTBF) versus accumulated hours of field operation. The three solid lines are of constant slope representing the rate at which the reliability of an electronic system

can be expected to improve with accumulated life, assuming that normal, good manufacturing and quality practices are followed. The slope plotted was chosen based on past experience with similar devices during field usage.

Any point on the top line represents what the expected MTBF of a unit will be, exclusive of any handling failures or past failures for which corrective action has been effectively implemented. For example, a unit made at a point in time where 50,000 hours of life have been accumulated by all units which have been in use would be expected to have an average life of approximately 1,000 hours. A unit made at the time when 100,000 hours of life have been accumulated will have a MTBF of slightly less than 1,500 hours, a 50 percent improvement with two times the accumulated life. This line then represents what the expected performance of a newly fabricated unit will be barring handling type failures. In a similar manner, the second line represents the expected reliability growth of a unit exclusive only of handling failures. The third solid line represents the expected reliability growth of units with no failures excluded.

A separate line was plotted excluding handling failures because early field experience pointed out that they were a significant part of the failure pattern of these devices and, because of the specific field usage conditions, handling would continue to be a factor in the MTBF.

These curves have been found to be useful in predicting warranty usage which forms a separate part of the customer price of each unit and have served as a basis for internal cost and inventory control.

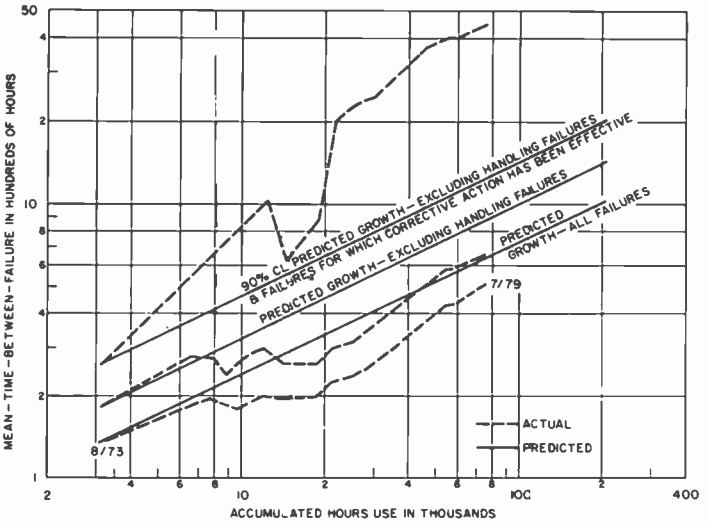

Fig. 3. This plot of MTBF versus accumulated hours of field operation shows the rate at which the reliability of an electronic system can be expected to improve.

Warranty costs

Warranty costs are normally tracked at Lancaster by product line with emphasis given to major dollar value contributors to these costs. Due to the cost importance and visibility of the Coaxitron Amplifier program, a separate reporting system was used in addition to inclusion of the figures in the standard report.

In-process yield summary

Amplifier subassemblies were fabricated in three separate departmental areas. Because of this fact and the high cost of any subassemblies contained in the Coaxitron Amplifier, unified reporting on scrap and rework cost was begun late in 1974. Table I is an example of the systems used in this reporting for the Coaxitron Tube area. Using these figures, management was made aware of the trends. The report was first issued on a monthly basis, then as improvement was noted, on a bi-monthly and then quarterly basis. These reports provided an overview of in-process efficiency for upper management without a large amount of detail. In addition, all three manufacturing areas involved were provided with yield information they normally would not receive. This information and trend analysis on electrical characteristics was issued in one report titled, "Coaxitron Visibility Report."

Table I. Typical 4668 yield summary.

Period Covered	*Assly. Produced*	*Initial OK*	*Rework*	*Rework OK*	*Scrapped*	*Net Yield*
Avg. 1975	42	39 @ 93%	.67%	.67 @ 100%	2.75 @ 7%	39.67 @ 94%
Avg. 1976	49.5	48 @ 97%	1.16%	.92 @ 79%	.067 @ .08%	48.8 @ 99%
Avg. 1977	45.6	43.6 @ 96%	2.08%	1.75 @ 84%	.33 @ .7%	45.25 @ 99.3%
Jan. 1977	58	56 @ 97%	3	3 @ 100%	0	58 @ 100%
Feb. 1977	84	83 @ 99%	1	1 @ 100%	0	84 @ 100%
Mar. 1977	84	76 @ 91%	8	5 @ 63%	3 @ 4%	81 @ 96%
Apr. 1977	35	32 @ 91%	3	3 @ 100%	0	35 @ 100%
May 1977	53	52 @ 98%	1	1 @ 100%	0	53 @ 100%
June 1977	65	64 @ 98%	1	1 @ 100%	0	65 @ 100%
July 1977	26	25 @ 96%	1	1 @ 100%	0	26 @ 100%
Aug. 1977	34	31 @ 91%	3	3 @ 100%	0	34 @ 100%
Sept. 1977	50	49 @ 98%	1	1 @ 100%	0	50 @ 100%
Oct. 1977	29	28 @ 97%	1	0 @ 0%	1 @ 3%	28 @ 97%
Nov. 1977	12	12 @ 100%	0	0 @ 0%	0	12 @ 100%
Dec. 1977	17	15 @ 88%	2	2 @ 100%	0	17 @ 100%
	547	523 @ 96%	25	21 @ 84%	4 @ .7%	543 @ 99.3%

Program results

Reliability growth

The dotted lines in Fig. 3 show the actual reliability of the Coaxitron Amplifier system. At the beginning of the program, the most optimistic value of MTBF, that line representing life with handling failures and corrective actions excluded, shows 260 hours. The predicted value at the current point in time with accumulated hours of usage at 80,000 hours shows a MTBF of 4,500 hours, a 17 times improvement. The actual value of MTBF demonstrated, including all failures, is 510 hours, exceeding the beginning value by 4 times. It should also be noted that the slope of the trend line is higher than predicted. The slope will decrease as "wear out" of units begins and is expected to approach a constant MTBF. The other two lines, which include many variables out of the control of the manufacturer, are approaching both the predicted slope and the predicted values of MTBF.

Warranty and field repair costs

It must be remembered that every dollar spent for warranty directly affects profit. A

Table II. Coaxitron Amplifier warranty usage.

Year	*% Sales*	*Year*	*% Sales*
1971	2.5	1975	16.4
1972	1.4	1976	2.3
1973	15.4	1977	1.4
1974	20.0	1978	.5

warranty figure of 1 percent of sales is good for this tube line and is as good as or better than many other commercial or military tube lines fabricated at the Lancaster location.

Table II shows the build-up of the field problem in terms of sales and the constant and dramatic improvement of these costs. Figure 4 uses driver circuit subassembly failure patterns to indicate field improvement in failure rate.

In-process yields

When reporting was begun early in 1975, subassembly yields for the Coaxitron Tube, the most expensive, complex assembly in the amplifier, were averaging 94 percent. If permanent records had been started earlier in the project, yields would have been worse. Information available indicates yields in the area of 85 to 90 percent for the 1973-1974 time frame. The average yield for the years 1978, 1977, 1976, was 98.9 percent, with a high of 99.3 percent and a low of 98.3 percent. Figure 5 illustrates this was the trend when the system was being implemented.

Figure 6 shows the change in the content of dispositioned nonconforming material per the Coaxitron Tube unit. These parts are mainly machined parts containing as high as 30-40 dimensions. A rapid fall-off can be noted here, indicating the system was exerting desirable pressure for quality improvement. In the other two major components of the system, the driver tube and the driver input circuit, similar trends were observed.

Characteristic improvement

One of the characteristics of a good, formal quality system is the ability to trace improvements in yields, warranty, and reliability. In addition, this system improves the traceability of individual units to the point where, in many cases, electrical testing parameter trends can be compared to fabrication process changes or material changes.

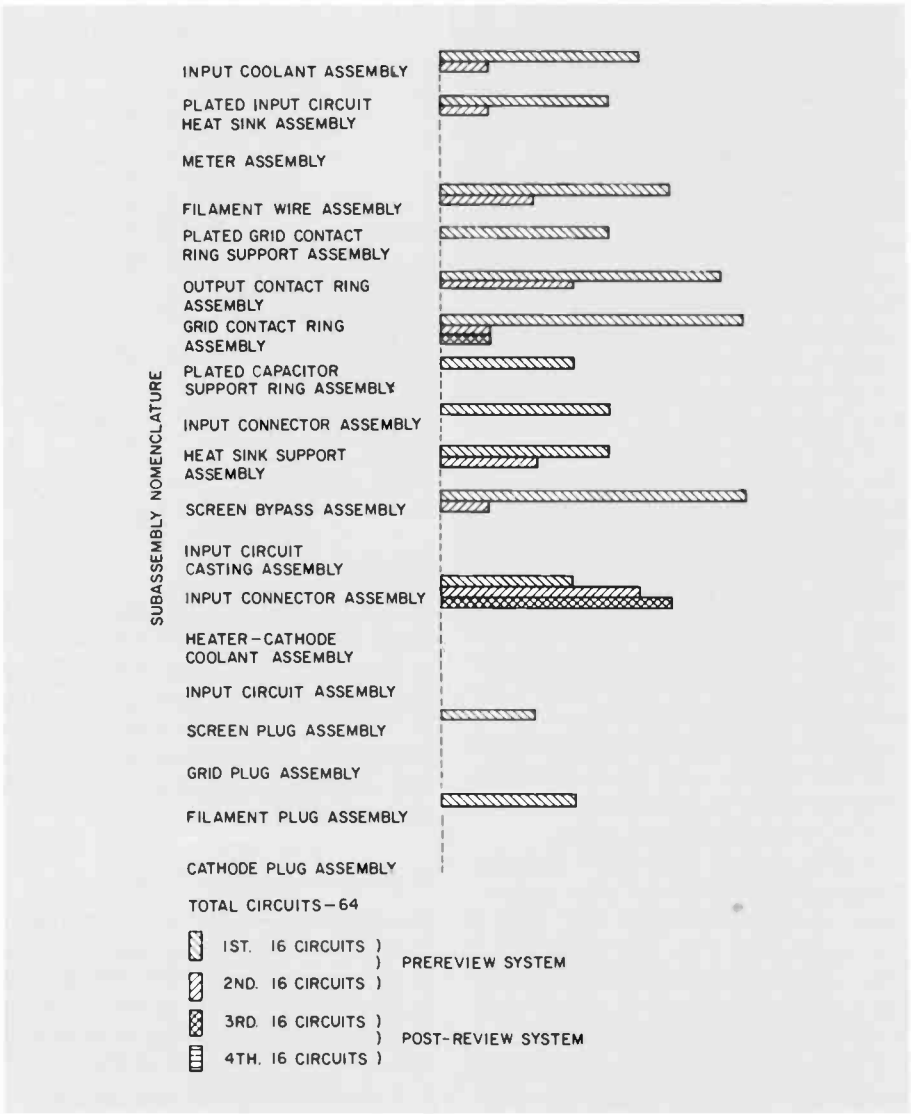

Fig. 4. Driver circuit subassembly failure patterns indicate field improvement in failure rate.

In the case of the 4655 Coaxitron Driver Tube, a good example of this ability is illustrated with Fig. 7. This figure shows the results of a purposeful change made to improve the plate current characteristic of the tube. It can be seen that in addition to a shift in the level (average) of this characteristic, a tightening of dispersion of the data is also evident. The tightening, less range, was caused by better control being exerted on all processes by the manufacturing activity and the Quality activity.

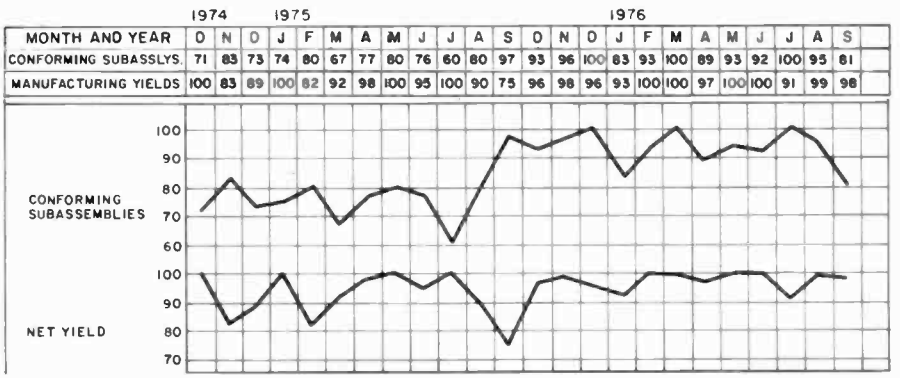

Fig. 5. When reporting was begun in 1975, subassembly yields for the Coaxitron Tube were averaging 94%.

Management conclusions

Obviously, a program of this magnitude is not undertaken without examining the need for such a program. It does require management and Quality staffing emphasis, and most importantly, a belief on the part of the people involved that the effort is worthwhile and useful. As mentioned earlier, the need for a better controlled program was pointed out by field failures and manufacturing difficulties. This combination automatically generated management emphasis at RCA and at the customer. When a decision was made to improve the current system, the staffing followed. After plans and systems had been developed and were ready for implementation, these items were put into action. In the case of this program, a number of group meetings were held with all concerned, from manager to stockmen. An overview of the program, and its applications and problems were provided to everyone. Specific items and systems were then discussed with those persons directly involved. This approach proved worthwhile.

It can be seen from the warranty viewpoint alone that the system pays in dollars. It also pays in intangibles such as customer satisfaction and a far-reaching attitude change in persons using the system. RCA Power Tube management has become so convinced of the usefulness of this system and its benefits, that the system, slightly modified to eliminate minor elements of the system, is being used in other projects such as the Department of Energy, Fusion Energy 200 kV Switch Tube, the Aegis Radar Switch Tube, and the Phalanx Radar Switch Tube. In addition, benefits from these systems acrue on standard commercial product since the auditing points out problems common to the project and commercial areas.

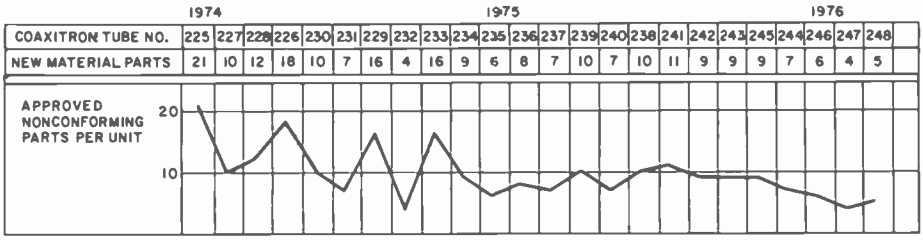

Fig. 6. These changes occurred in the content of dispositioned nonconforming material per Coaxitron Tube unit.

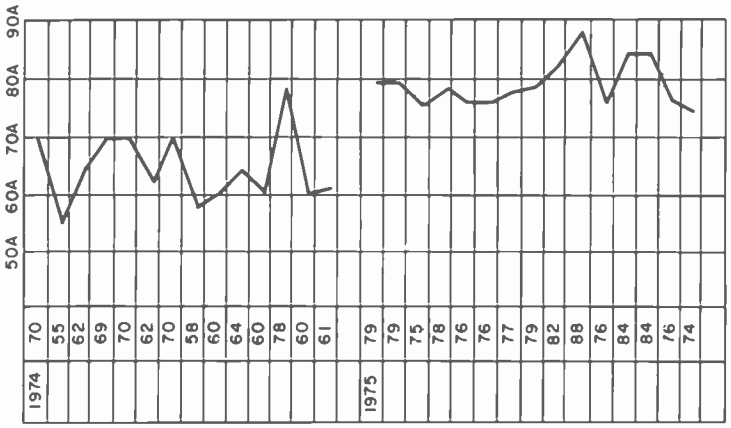

Fig. 7. An example that the characteristics of a good, formal quality system are the ability to trace improvements in yields, warranty and reliability is illustrated by the 4655 Coaxitron Driver Tube.

Bill Bradley, left, and Jerry Buchko are shown with the Coaxitron Amplifier.

Bill Bradley joined RCA in 1952. He has held various positions in Manufacturing and Quality and Reliability Assurance. He is presently Manager of Quality and Reliability Assurance for the Electro Optics and Devices Operation of the Solid State Division.

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Jerry Buchko joined RCA in 1959, with his first assignment being in Power Tube Applications. During the 14 years he was in the Power Tube Design and Applications groups, he was responsible for the design of many of the current line of Cermolox TV Broadcast tubes. In 1973, he transferred to the Quality and Reliability Systems Engineering group to work directly on the Coaxitron Quality System. His current assignment is to develop and maintain the Quality Systems for FM Broadcast tubes, Switch Tube for fusion energy research and other military and commercial power tubes.

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E.B. Gamble

Reliability growth testing of avionic equipment

The Reliability Growth Program has significantly contributed to Avionics Systems' ability to reduce warranty costs while increasing customer satisfaction.

Abstract: *This presentation covers the salient features of the Reliability Growth Program used by RCA Avionics Systems to achieve cost effective reliability for each new system produced for the aviation market. The origin of reliability growth is reviewed and illustrative data are presented from the actual results obtained with RCA's PriMUS-20/30 X-Band Digital Weather Radar.*

RCA Avionics Systems engages in a dedicated program to achieve the highest practical and cost effective reliability for systems produced for commercial and general aviation markets.

There are four basic elements of this reliability program, but it is the purpose of this paper to dwell specifically on only one of the elements: the Reliability Growth Program, or RGP. Therefore, only a brief overview of the basic reliability program is given so as to place the RGP in proper perspective relative to the overall program.

In covering the RGP, first the mathematical model will be introduced and briefly reviewed, then, the details of RGP implementation at RCA Avionics Systems will be provided. In other words, for those considering the use of RGP, details are provided showing what needs to be done with emphasis on illustrations using a typical avionics RGP as an example.

The reliability program

Brief descriptions of the four basic elements of the reliability program are provided in the following paragraphs. If the reader desires additional information regarding these elements, reference 1 is recommended.

- *Design standardization*—All designers are required to follow specified design practice and derating policies and to use components with established levels of performance, quality and reliability. An active design review program assures adherence to the specified policies.
- *Mean time between failures (MTBF) prediction*—The MTBF for each major assembly and the overall system is predicted using failure rates derived from MIL-HDBK-217 for the expected operating and environmental stress conditions.
- *Reliability Growth Program*—Pilot production systems are subjected to a stringent environmental test program defined as a Reliability Growth Program (RGP). During this RGP regimen, every failure trend is identified and corrective action is determined and implemented for the systems under test. This causes the system reliability to improve with time, and RGP testing is continued until the demonstrated MTBF reaches the expected level.

Production AGREE testing—Every production system is subjected to between three and five days of AGREE cycling comprising 54 to 90 hours of operation at high ambient temperature, with a ten-minute vibration cycle each hour, nine to fifteen power and thermal cycles, and an aggregate vibration time of nine to fifteen hours. In this manner, system reliability is maintained at a high level because infant mortality failures are detected and corrected, and new failure trends are identified and eliminated.

During the past several years, this reliability program has been successfully utilized on several avionics programs. These include PriMUS-10 DME, and the following weather radars:

Display storage tube—AVQ-56/PriMUS-35

Digital monochromatic—PriMUS-40, PriMUS-20/30, AVQ-30* Indicator, Weatherscout

Digital ColoRadar—PriMus-400 PriMus-90*

RGP testing will soon be initiated for the AVQ-30* Color Indicator and PriMUS 200/300 Slim Line Radar Systems. The reliability program has been successful on all programs including the first three listed, for which the design standardization phase was not fully implemented.

*AVQ-30 and PriMus-90 are utilized by commercial airlines.

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The origin of reliability growth

Patterned reliability growth was first recognized and published by J.T. Duane[2] of General Electric's Motor and Generator Department in 1962. His conclusions were based on analysis of test and operational data on five divergent groups of products: two hydro-mechanical devices, two complex aircraft generators, and one jet engine. Simply stated, his concept of reliability growth is:

> For a constant level of corrective action effort and timely implementation, reliability growth closely approximates a straight line on a log-log scale.

Mathematically, this is a simple straightforward model

$$\lambda_{\Sigma} = \frac{F}{H} = KH^{-\alpha} \qquad (1)$$

where: λ_{Σ} = Cumulative failure rate

H = Total test time

F = Failures during H

α = Reliability growth rate

K = Constant determined by circumstances

A log-log plot of equation 1 for a hypothetical case appears in Fig. 1 as the upper straight line with slope $-\alpha$. The model appears so simple that it prompts the comment, "Could real life possibly behave this way?". However, extensive critical evaluation by GE's Aerospace Electronics Department, as well as RCA Avionics' test results, have confirmed its validity. Two GE papers[3,4] are highly recommended for those interested in additional material on reliability growth planning and effectiveness. E.O. Codier states, "This model fits real life like a glove. It fits so well that if a set of data fails to fit it, we are justified in questioning the data or the program that produced it to find out why."

Let's examine some general characteristics of the growth model. The constant K and the growth rate α are determined automatically as the data are accumulated. Thus, while growth rate is predictable within general ranges, the actual value can only be determined as the results are analyzed. Experience of many test programs has shown that:

a. growth rate is a direct function of the level of effort and can range between 0.1 and 0.6;

b. growth rate will range between 0.3 and 0.5 where a systematic and deliberate reliability improvement effort is being made;

c. for a given level of effort, the growth rate is:

- higher for analog hardware than for digital hardware,
- higher for newly designed equipment than for equipment that has matured in production, and
- higher in proportion to severity of test conditions.

In the example of Fig. 1, the value of K is 0.1414 and α is assumed to be 0.5. Assume the initial failure rate of 10/1000 hours has resulted from two failures within 200 hours of test time. The slope of $-\frac{1}{2}$ shows that to decrease failure rate by one octave (to 5/1000 hours) will require two octaves more test time (800 hours); or to decrease by one decade (to 1/1000 hours) will require two decades more test time (20,000 hours).

The reciprocal of cumulative failure rate is cumulative MTBF (test time divided by total failures). The equivalent to the λ_{Σ} plot in Fig. 1 becomes the lower curve (MTBF) using the right-hand ordinate. Many observers dislike the curve going down as things get better; therefore, the MTBF plot provides results in an "up is good" format.

Formulation of RGP plan

There are five basic areas to be considered when formulating the RGP plan. As we progress through these areas, the parameters used for the RCA Avionics PriMus-20/30 RGP plan will serve as illustration.

- *Establish MTBF goal* — The basis for the MTBF goal should be a prediction in accordance with MIL-HDBK-217. For the PriMUS-20/30 system, the predicted MTBF at 70° C component ambient was 1240 hours. For a test regimen which is significantly more severe than the expected use environment, demonstrating 50 percent of the predicted MTBF is considered adequate. Thus, the MTBF goal for the PriMUS-20/30 RGP was 620 hours.
- *Determine required test hours* — Experience shows that the required test hours will be ten to fifteen times the MTBF to be demonstrated. Based on this, the PriMUS-20/30 RGP test plan provided for a test period ranging between 6,500 and 9,000 hours.
- *Determine quantity of systems* — The number of systems tested is strictly a trade-off between how soon the results are needed versus how many systems can be committed to RGP considering cost, availability, and subsequent disposition. A minimum of three systems is desirable to assure some statistical sampling of production. Five each PriMUS-20 and PriMUS-30 systems, which differ only slightly in operational function, were scheduled for a minimum test period of 650 hours.
- *Select environmental regimen* — Numerous environmental profiles are available for consideration, including many in MIL-STD-781; however, the basic regimen used by RCA Avionics

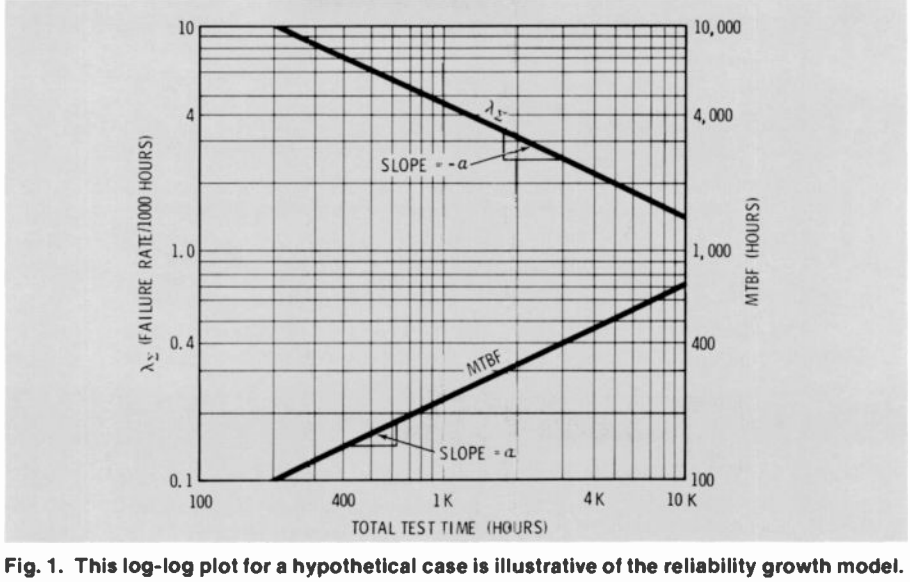

Fig. 1. This log-log plot for a hypothetical case is illustrative of the reliability growth model.

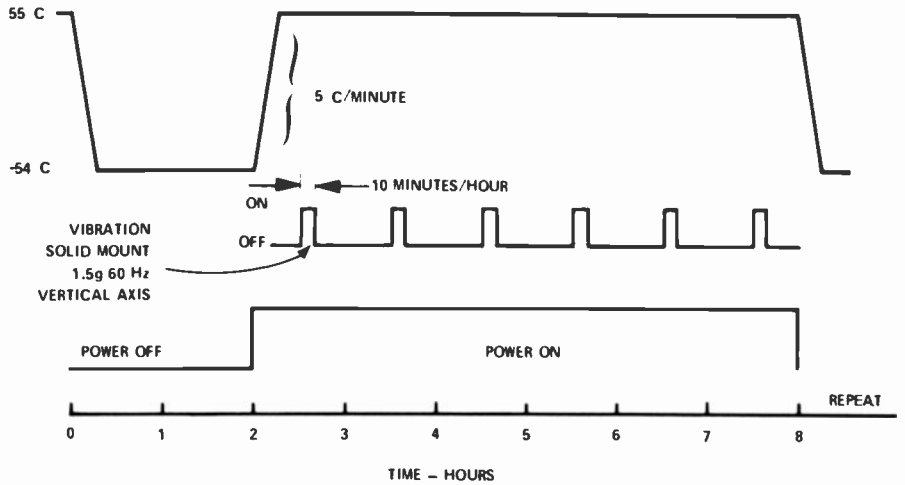

Fig. 2. During the environmental program cycle for the AGREE test plan, the power is OFF during cold soak, and power plus intermittent vibration are applied during high temperature exposure.

Systems is the AGREE test plan illustrated by Fig. 2. As illustrated, the power is OFF during cold soak, and power plus intermittent vibration are applied during high temperature exposure. With this regimen, the ratio of accumulated life to test time is 0.75; therefore, four hours of test time are required for each three hours of accumulated life. Thus, in terms of severity for the PriMUS-20/30 RGP, the characteristics of the planned test are:

Equipment life (hours)	650
Test time (hours)	867
Thermal and power cycles	110
Vibration cycles	660
Hours of vibration	110

- *Assign responsibilities* — The performance of RGP will generally be a team effort and, for a successful plan, it is important for each activity to understand its participation and responsibilities. At RCA Avionics Systems, the team includes Design Engineering, Parts Management, Test Engineering, and Quality Assurance. Responsibilities are assigned in four definitive areas as follows:

1. Performance evaluation: In accordance with a detailed equipment test plan, Test Engineering is assigned responsibility for daily evaluation of system performance and recording results in the system log book. Observation of a system malfunction is noted in the system log and the occurrence is witnessed by the assigned Design Engineering representative. Failures are reported on RCA Failure Report Form DEL 1314.
2. Malfunction analysis: Because of intimate knowledge of system and circuit operational modes, Design Engineering is assigned responsibility for system malfunction analysis. This procedure exposes the designer firsthand to the various types of failure modes attributable to his design and assures rapid diagnosis and expedient return of the system to the test program. It is important to recognize that RGP is not the time to have factory technicians learn how to repair the system. Each unidentified erroneous removal could add several hours of analysis effort.
3. Part failure analysis: Responsibility for analysis of defective parts is assigned to Parts Management. Where required, Design Engineering provides assistance in isolating system operational modes that may be contributory to observed part failures. Assistance of the part manufacturer is obtained as applicable in the determination of failure modes and/or corrective action.
4. Corrective action: Upon identification of either an actual or potential failure trend, applicable corrective action will be determined. The proposed corrective action will be reviewed and approved by Design Engineering, Parts Management, Test Engineering, Manufacturing, and Quality Assurance, after which systems under test will be modified on a minimum down-time schedule. New system modules cannot be substituted as an expedient to minimize down-time; i.e., testing must be continued with the original system modules.

Table I. Tabulation of results for PriMUS - 20/30 RGP.

A. Failure incidents (from 43 system failure events)

Primary failures	52
Secondary failures	19
Visual removals	7
Erroneous removals	2
Total incidents	80

B. Defect categories and corrective action for primary failures

Defect Category	*Failure Quantity*	*Corrective Action*	*Relevant to MTBF*
Design	14	13	1
Design/procedures	4	3	1
Workmanship/procedures	6	6	0
Vendor process/quality	20	18	2
Random part defects	8	0	8
Totals	52	40	12

C. Demonstrated MTBF = 670 hours (8,024 ÷ 12)

Analyzing the results

As the RGP testing progresses, it is necessary to concurrently analyze and categorize failures, determine and verify validity of corrective action, and maintain a running plot of reliability growth. These procedures are best illustrated by reviewing the actual results of the PriMUS-20/30 RGP test.

The ten systems under test completed 8,024 hours of operation. Table I summarizes and tabulates the results and il-

lustrates the segregation of failures and failure category assignment. Definitions applicable to Table I are as follows:

- *Failure event* — An observation at a test interval that a system fails one or more specified performance parameters.
- *Failure incident* — Each defect, part removal, or repair action comprises a failure incident. One or more failure incidents will result from each failure event.
- *Primary failure* — The initial failure of an event involving one or more incidents.
- *Secondary failure* — One or more items which failed sequentially subsequent to, and as a direct result of, a primary failure.
- *Visual removal* — Item removed because of corrective action decision but not observed as a failure.
- *Erroneous removal* — Item removed which does not correct the observed failure.

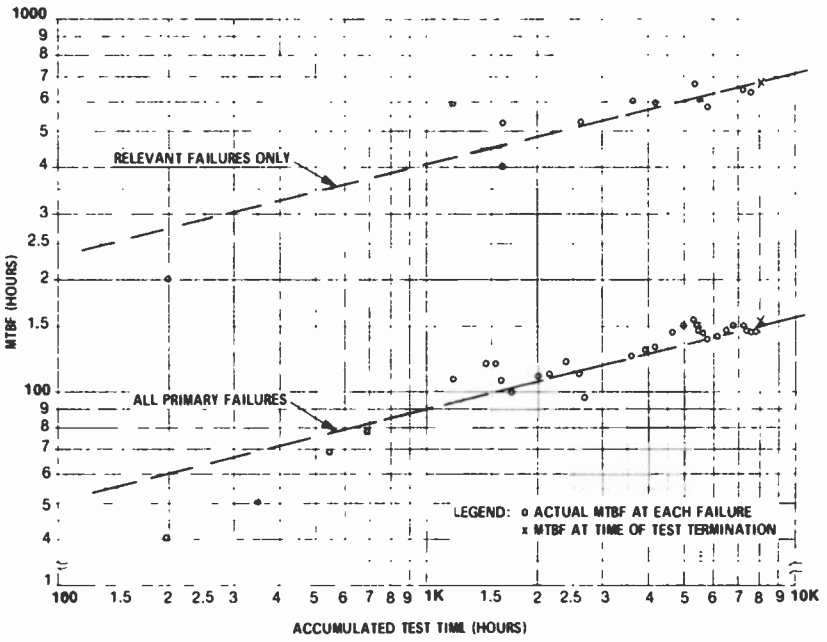

Fig. 3. The system Reliability Growth is plotted in accordance with the Duane hypothesis.

Table I shows that 52 primary failures occurred during the test program. Corrective action was implemented for 40 of these, leaving a balance of 12 failures considered relevant to determination of MTBF. Based on 8,024 accumulated operating hours with 12 failures, the demonstrated MTBF is 670 hours, which exceeds the established goal of 620 hours.

To evaluate reliability growth, the system MTBF, based on both sets of results (primary and relevant failures), is plotted in accordance with the Duane hypothesis on Fig. 3. The lower data set includes the 52 primary failures and exhibits an MTBF growth from first failure (25 hours — not shown) to 154 hours at time of test termination. The upper data set considers only the 12 relevant failures, and exhibits an MTBF growth from first failure (200 hours) to 670 hours at time of test termination.

The slope of the "growth" lines in Fig. 3 is approximately 0.25, which is reasonable considering that the PriMUS-20/30 systems consist primarily of new digital designs coupled with mature production. For total test time less than 1500 hours, a significant number of points are aligned along a growth line with α approximately equal to 0.5. This could either be a "signal-to-noise ratio" problem with the early data or a subset growth model. In general, the Duane model is tolerant of this type of situation in the long run.

The two plots on Fig. 3 illustrate a very significant point. Throughout the industry there are wide discrepancies and opinions on the definition of "failures" and "relevant failures." Note, however, that the "growth" lines for "all primary failures" and "relevant failures" are both drawn with the same slope ($\alpha = 0.25$); and each fits its data set reasonably well. In general, short term slopes other than the main slope also track within a reasonable tolerance. Thus, it is evident that, although differences in failure definition affect the apparent MTBF, the key factor (reliability growth rate) is virtually unaffected.

Organizing the data

Proper data organization for ease of analysis is a must for an RGP evaluation of this magnitude. Failure trends need to be identified and accurate corrective actions must be determined from the analysis. Also, some failures may be related to one or more previous failures. If the program is being run for a specific customer, it probably will be necessary to justify decisions to his satisfaction. Without good data organization, accomplishing these tasks will be very difficult.

Several tabular formats were found useful for data organization for RGP testing. The first is a pseudo-graph format used to summarize the history of each system. An event flag identifies the approximate time of failure, and all incidents associated with the event are listed in the applicable column; receiver-transmitter, indicator, or antenna. Independent incidents are stacked vertically and secondary incidents are shown adjacent to the primary failures. Thus, each such chart provides a snapshot of the performance of one system during the test program. In this way, significant differences in failure history for different systems are readily identified; for example, for the PriMUS-20/30 RGP, System No. 6 exhibited six events with twelve incidents whereas System No. 8 exhibited only one event with one incident. A second tabulation provides a brief descriptive summary of failure events for each system and accompanies each system chart.

The third format is a method of tabulating the failed items by part number and circuit location. This facilitates identification of trends to either a specific part number or system application. A system event column on this tabulation cross-references the items to the system charts. Tabulation of failure mode and failure cause provides the basis for corrective action implementation.

Conclusions

RCA Avionics Systems is committed to providing its customers with the design reliability of the equipment at the early phases of production. The Reliability Growth Program is used primarily to find out "where Avionics Systems is" on a given product, and continue testing and corrective action until MTBF improves to where it has to be. However, for those involved with a contractual reliability program, it is also a valuable tool for planning and managing a contractual program, as indicated by reference 4.

Summaries of corrective actions help in determining relevance of failures.

Another item of data organization is a tabulation of corrective action taken. Below is a representative sample of items extracted from the Corrective Action Summary of the PriMus-20/30 RGP analysis. This tabulation provides the basis for determining relevance of failures to MTBF.

Design Defects

Resistor: 990413-505 (150 Ohm, 1/4 watt)

The incorrect power rating specified for this resistor placed it under continuous overstress. A 3-watt resistor was specified as a replacement. Based on this action, all observed failures were considered non-relevant to MTBF determination.

Workmanship and procedural defects

Workmanship

Intermittent operation resulted from a hand-soldered terminal which contained no solder. Corrective action consisted of better identification of all hand solder locations and tightening of inspection of such areas. Based on this action, the observed failure was considered non-relevant to MTBF determination.

Test Procedure

The turn-on procedure initially programmed for RGP testing applied power to the R/T first and then to the Indicator, several minutes later. In Normal system use, both units are turned on simultaneously via an Indicator pushbutton. Internal power supply design was based on the normal procedure and contains features, such as ramping circuits which prevent instantaneous application of power to system circuits. The programmed turn-on sequence circumvented these features resulting in the following overstresses:

- Surge current ratings of indicator tantalum capacitors (two failures observed) were exceeded.
- The low voltage power supply in the R/T lost regulation from the instantaneous overload and subsequent transients resulted in a 30 percent voltage overshoot, thereby overstressing parts associated with the Indicator High Voltage Power Supply (HV Transformer breakdown observed and two associated drive transistors).

—The test program was modified to turn on all system components simultaneously. As a result of this action, the 5 observed failures were considered non-relevant to MTBF determination.

Random Vendor Defects

Diode; Switching: 3718366-20 (1N4148)

After 120 thermal cycles, an intermittent connection was found at the cathode of this diode. No other solder deficiencies were apparent in the surrounding printed circuit area. Repeated attempts to solder the lead were not successful because the plating on the kovar lead was missing. Inspection of other applications of this diode, as well as a sample quantity from stock revealed no similar deficiencies. No corrective action was believed feasible, therefore the failure was considered relevant to MTBF determination.

For those persons interested in, or considering the use of RGP, the illustrations and insight provided by this exposure to RCA Avionics Systems' experience will be helpful. RGP has significantly contributed to Avionics Systems' ability to reduce warranty costs while at the same time increasing customer satisfaction, which in turn has increased market demand for its products.

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Design for high reliability and low cost

High reliability and cost reduction begin at the design phase of manufacturing.

Abstract: *Basic and fundamental design principals and techniques are essential to achieving high reliability and low cost. Fundamental principals pertain to parts selection, parts application, partitioning and testing. Supporting techniques include worst cast analysis, failure mode and effects analysis, qualification and step-stress testing, screening of both parts and assemblies, failure reporting and analysis and several analytical models for cost assessment and control. Essential support for design activities should be derived from manufacturing, purchasing, and environmental test activities and specialty groups such as reliability, parts materials and processes, human factors, configuration management and documentation.*

The reliability objectives of an equipment development program are accomplished not by the reliability activity alone or any one specialist alone, but by the collective effort of all program functions.

The principal requirements and goals are usually set by customers, government laws and regulations or industry standards. Subordinate goals are often established within each program. Personnel usually come from several different sections or divisions and other companies as well. These people and their functional groups must all be integrated effectively by program management. A thorough indoctrination is needed regarding program requirements and goals and the techniques and procedures that will provide reliability. A similar integrated effort is needed to achieve low cost.[1,2,3]

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Basic perspectives

Designing for high reliability and low cost requires that several things be brought into perspective. Reliability can be stated in explicit quantitative terms such as failure rates, mean time between failures or probability of survival, but a meter cannot be used to make an instantaneous measurement to determine what the reliability is. High reliability is even less tangible because this is relative. The influencing considerations are the complexity of the item; the function and mission that is to be performed, including duration; and the operating conditions and environment. In the early days of satellites, a life of three to six months was considered high reliability. Now the satellite life is five to eight years with much greater satellite complexity. The Minuteman program was the first major program to demonstrate that high reliability can be achieved if the causes of failure are identified and eliminated.

Cost can be just as difficult to assess as reliability. Industry often interprets cost as the amount of money necessary to develop and produce an item. Frequently, this also has been the viewpoint of the consumer, particularly at contract award. But the consumer's main concern is life cycle cost or total cost of ownership — the cost of operating and supporting the equipment throughout its total period of use must be added to the purchase price.

The key to successful reliability and cost reduction is: *Do it right the first time*! Obviously, anytime something is only done once, rather than two or three times, substantial cost penalty is avoided. And doing it right means minimizing the potential for failures and pushing the reliability higher. This admonition, to do it right the first time, applies to every aspect of getting higher reliability and reducing the cost.

Parts selection

One of the first considerations in achieving reliability and cost reduction is parts selection which occurs early in the life cycle of manufacturing. The guiding criteria are the following:

1. Maximize the use of proven parts. Qualification tests should have established the capability to provide the necessary performance under the range of environments and use conditions anticipated. Prior use should show problem-free performance.
2. Maximize the use of proven vendors. Qualification alone is insufficient; some vendors exhibit a poor or inconsistent quality history. If the low cost vendor is a marginal quality producer, the cost of correcting problems in the product will far exceed the purchase savings. In making vendor selections, quality performance is a more important criterion than cost.
3. Minimize the number of parts types. This mainly contributes to cost savings

through larger quantities for better purchase price, fewer items and vendors to track, and simplified logistics.

4. Monitor vendor changes in design, materials or processes. Inconsequential changes, to reduce cost or improve delivery schedules, can produce a subtle change in characteristics resulting in equipment performance being marginal or erratic.

Thus, the key reliability and cost considerations in parts selection are to maximize the use of proven parts and vendors, minimize the part types and monitor vendor changes.

Parts application

A second and closely related aspect of design for reliability and cost reduction is parts application. Each part must be capable of providing the necessary performance characteristics over the range of environmental and use conditions it will experience. Parts should be used conservatively, that is, operated at derated levels of electrical, thermal or mechanical stress. An associated aspect of derating is to practice worst case design. Consideration must be given to parameter tolerances and particularly the wider limits that can occur under some stress conditions. Also to be considered are the end-of-life values or the parameter drifts that occur with time. Another important element of parts application that is an essential ingredient of proper derating is good thermal design. When equipment first became solid state design, largely based on transistors and diodes, power densities were quite low and thermal design was quite simple. Now with high-density large scale integration (LSI) devices being employed in large numbers in small compact printed circuit board configurations, the higher power densities have made thermal design a critical task. Here again, worst case conditions must be the primary evaluation.

Partitioning

A third important element of design for reliability and cost reduction is partitioning, or how the whole design is subdivided electrically and mechanically into modular building blocks. The relationship of this design element to reliability is primarily through its impact on thermal design. The basics that apply here are: 1. strive for uniform power densities; 2. avoid concentrations of power; 3. avoid stagnation areas in cooling air flow; 4. where relatively high power modules are unavoidable, apply special cooling techniques to minimize local temperature rise; 5. place the highest dissipation modules as close to the end of the cooling path as possible to achieve the lowest average temperature for all modules; and 6. employ isolation techniques on particularly high dissipation parts or modules to minimize the impact on adjacent items.

In many instances, the impact of partitioning is more significant to cost than reliability and sometimes it is important to both. An example of the latter is equipment that required three channels to handle mission requirements. Each channel included three sequential functions (A, B and C). One partitioning arrangement has one module with function A replicated three times. Two additional modules similarly handle functions B and C, respectively. The dotted lines in Fig. 1 depict this modular arrangement. An alternate partitioning incorporates functions A, B and C for one channel in one module. This same module is used two additional times to complete the total configuration as shown in Fig. 2. The latter arrangement has definite reliability and cost advantages.

When a failure occurs, the effect will likely be the loss of one channel for either partitioning arrangement. However, when corrective maintenance is performed by module replacement, configuration A (Fig. 1) loses all three channels whereas configuration B (Fig. 2) retains two channels in operation, which provides greater reliability. Configuration A requires the detail physical design and manufacture of three different modules whereas only one is needed for B. Thus, design costs are less, manufacturing costs are lower (a larger, more economical run is made on only one module), and logistics are similarly simplified for the user. The net result is lower initial cost as well as life cycle cost and greater reliability.

A potential need for maintenance points to yet another feature that must be carefully analyzed during the partitioning design effort and that is testability. Whenever a failure occurs, functional capability must be restored as quickly as possible. This is commonly accomplished by replacement of the failed module, assembly or equipment. Thus, prompt failure detection and rapid isolation of the specific failed replaceable items are vital to achieving high system availability. This is done by arranging the partitioning to provide for the simplest, most unambiguous test point complement or built-in test function supported by failure mode and effects analysis. Effective design for testability minimizes both maintenance personnel skill level and maintenance time, which are major elements of life cycle cost.

Testing

Qualification testing at any level, from part to system, proves the success of the design and is an important element in achieving high reliability. Similarly, the reliability demonstration test yields data that fulfill the mean time between failure (MTBF) requirement. A supplementary version of the customary qualification testing, that is

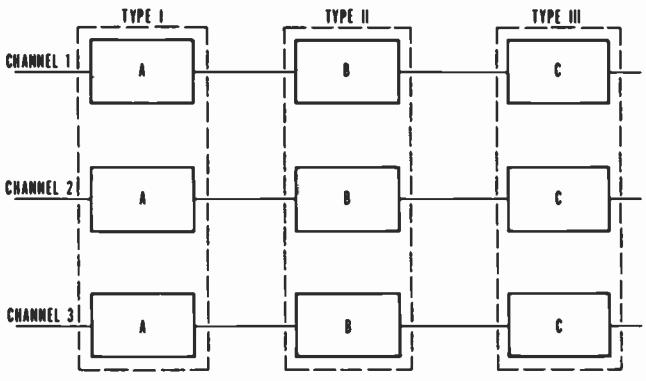

Fig. 1. Partitioning using three module types.

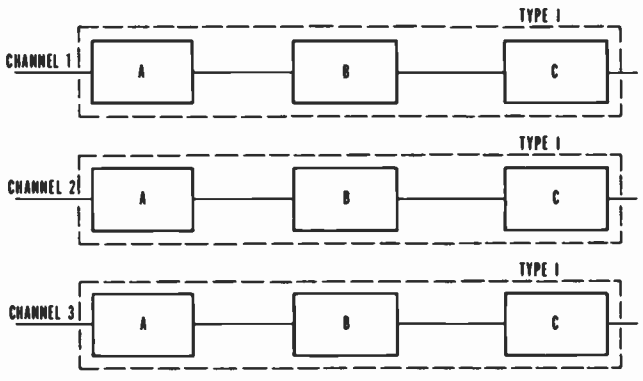

Fig. 2. Partitioning using only one module type.

not always used but has substantial merit for getting high reliability, is step-stress testing. Stress levels are applied that incrementally progress beyond the specified maximum and minimum values at which the equipment must perform. The objective is to determine that there is at least some minimum safety margin in the design.[4,5]

Screening

Screening or burn-in testing is another test concept that has reliability significance. It is used at all levels, from parts to complete equipment, to identify parts and equipment discrepencies and to eliminate these from the remaining normal population. When screening can effectively accomplish this objective, the reliability of the product will be improved. To be effective, a screening test must be sensitive to the likely failure modes and mechanisms of the items being screened. Thus, some degree of customizing the test is in order.

Willoughby, in his keynote address to the Environmental Stress Screening Conference,[6] supported the need for screening with the following points:

1. Reliability in mature designs is less than expected.
2. Manufacturing results do not measure up to expectations.
3. Seventy percent of repairs are in random category — half parts and half workmanship.
4. Semiconductor devices are the predominant problem.
5. Hi-rel devices are not as good as expected.
6. Incoming inspection failures are higher than anticipated.
7. Cost of finding a defective at various manufacturing stages is: five dollars at incoming inspection, thirty at first assembly and three hundred in the completed system.

Screening must begin at the parts level, before modules or assemblies are made. The most cost-effective screening techniques at the parts level are thermal cycling and particle impact noise detection (PIND). The latter technique is specifically applicable to devices with internal cavities and electrical short possibilities. At the higher assembly levels, the preferred techniques are random vibration (6-G level) and thermal cycling, both effective on most types of workmanship defects. Thus, until the time when part vendor and equipment manufacturer quality levels are significantly increased, screening, at least on a selective basis, is in order and will yield reliability and cost dividends.[6,7]

Failure reporting, analysis and corrective action

Another prime contributor to reliability improvement and cost reduction that must not be overlooked is failure reporting, analysis and corrective action. As with screening, the earlier this discipline is invoked the greater the cost payoff becomes. Anytime a failure occurs, from breadboard testing on, it should be completely documented and carefully analyzed as to cause and contributing factors. An important element of these investigations is destructive physical analysis (DPA) on the failed device. This should usually be done unless the cause of failure is otherwise evident.[8]

Cost assessment and control

The foregoing discussions have highlighted several fundamental design principals and techniques, along with some support concepts, as they bear on achieving high reliability and low cost. Although some specific areas of cost impact have been addressed, it is appropriate to identify several tools that can support the design effort by providing a means for overall cost assessment and control.[9,10]

Design-to-cost

The most important factor in limiting equipment cost is setting and maintaining a cost target. The discipline of addressing a cost target limits design solutions which fit within the scope of the target. Design-to-cost can have great impact on an equipment design program, but only if a target is established and allocated firmly, and if performance against the target is monitored throughout the design cycle. The assignment of firm targets and allocations forces designers to look for solutions to fit these costs. Periodic evaluations of design elements guard against lapses of the discipline or surprise cost drivers. A manufacturing estimate of purchasing, fabrication and assembly costs can help in selecting the lowest-cost alternative.

The complexity of design discipline for low cost can vary according to the complexity of the design and the degree of difference between the cost target and previous efforts of the design group. Most equipment would probably benefit from computerized analysis tools.

Price model

In the earliest stages of concept development, the *price* model can be used. The design-to-cost mode of price requires a cost target and the estimated complexity of the proposed design. Iteration can give guidance as to what changes in component types and size are necessary for a successful design. The assessment of new component development requirements will allow tradeoff of non-recurring and recurring costs.[11,12,13]

When specific design elements are conceived to the point of a proposed bill of materials, more detailed analytical models can make more accurate evaluations. The tasks of cost estimation and control are made easier and more accurate by estimating and monitoring elemental costs. Costs should be controlled at least down to the lowest assembly level, so that design attention can be addressed precisely where it is needed. Estimation of cost elements within assemblies can speed the comparison of design alternatives, and highlight cost impacts of repeatedly used components. Such attention needs to be directed to multiple-use integrated circuits or other high-cost items, and helps to control the influence of vendors and manufacturing facilities.

Unit production cost tracking model

RCA's "Unit Production Cost Tracking Model" is designed to track cost allocations to the lowest assembly level, and across as many as 99 commonly-applied cost categories. It compares cost performance with targets at each assembly level. It has the capability to account for the effects of inflation on the target, and it tracks overall performance against the target as the design progresses.[14]

Life cycle cost models

The control of design for life cycle cost of ownership requires a means of estimating future support costs. Since these costs depend upon several uncertain parameters,

Dave Troxel, seated, and Harvey Barton read a data printout analysis.

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such as hours of operation, numbers of failures and times for repair, their estimation cannot be precise beforehand. For this reason, operating and support cost estimates are used primarily to compare one alternative against another. In this regard, the evaluations are dependable, for the factors that cause differences between alternatives tend to have statistical convergence in errors that are compared. Several computer models have been developed for estimating life cycle cost of ownership.[15, 16, 17, 18] Some of these are designed primarily to evaluate support costs, and are used by the military services who developed them. The Army uses Generalized Electronic Maintenance Model (GEMM),[19] which is one of the most capable, having provisions to estimate transportation costs due to deployment, as well as the more commonly measured spares and repair costs. Other similar models are used by the Navy and Air Force.[20, 21, 22]

Summary

Designing for high reliability and low cost requires a disciplined and well integrated effort not only among the several design disciplines but also among the supporting functions of manufacturing, purchasing, environmental testing and the specialty areas of reliability, parts, material, processes, human factors, configuration management and documentation. Emphasis must be on the design fundamentals of parts selection, parts application, partitioning and testing. Important design support techniques include worst case analysis, failure mode and effects analysis, qualification and step-stress testing, screening of parts and higher-level assemblies, failure reporting and analysis, and a family of analytical models for cost assessment and control. The designers' efforts as well as the efforts of the support groups must all be focused on the motto, "*Do it right the first time*!"

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The interface between systems design and reliability

The combined efforts of the design and reliability engineers, program manager, and systems engineers design reliability into a system from the very beginning using interactive computerized analysis aids.

Abstract: *The basic problems in electronics hardware design are described in terms of the reliability engineering process. How, when, and with whom these problems are solved by cooperative effort determine the level of success in achieving a reliable system design. The basic goals of voltage commonality, design simplification, and minimization of undesirable characteristics are outlined. Also treated are some typical reliability design architectures — single thread,* m *out of* n, *and parallel redundancy with switching.*

Where does reliability start?

During the concept and design phase of a system, the reliability engineer is confronted with three initial problems: to analyze the program's reliability requirements, to assist in developing a design concept that meets these requirements, and to interpret the specified reliability requirements for the designers.

The second and third problems are particularly challenging, since the design concepts and actual subsystem designs directly impact the frequency and severity of the failures that will occur in the system.

However, system designers sometimes need clarification of the implication and the exact meaning of a particular reliability parameter and how it will affect the system design. The reliability engineer cannot assume that the members of the design group will understand all the intricacies of the reliability parameters associated with the system requirements.

A relationship of cooperation is essential to the success of any reliability-oriented system design. Therefore, early in the program, one of the most important tasks involves active cooperation between the system designers (the true architects of system reliability) and the reliability engineers who bear a specific responsibility in this area.

It should be noted that although this paper addresses only electronic hardware reliability. a close relationship exists between *reliability, maintainability,* and *availability* in terms of realistic requirements for most military systems.

Defining the design interface problem

The first step toward solution to this design interface problem is to recognize that it is a problem and then develop a methodical way to solve it. Indoctrination of program personnel to familiarize them with basic reliability requirements is the initial part of the solution. The program systems engineer is the key person; he controls the overall design. The reliability engineer takes the first step toward controlling design reliability in discussions with the systems engineer on how the reliability parameters affect the system concept and the selection of hardware.

The systems engineer must, of course, be motivated not only by the reliability engineer, but also by management concern and support. Therefore, program and marketing managers must also be fully aware of the reliability requirements. Separate management meetings are useful in the exchange of ideas, questions, and suggestions. Reliability guidance at the *beginning* of the program is a key to a system designed with reliability in mind.

With the preliminary groundwork established, the systems, design, and reliability engineers must work together to verify the concepts for the system architecture and the requirements for each electrical and mechanical subsystem. Program memos are a part of this process, documenting the system philosophy for a reliable design. But memos are not enough. Person-to-person contact between the reliability engineer and designers is essential to ensure that the reliability design message is clear. Through this cooperative effort, the design will conform to the reliability groundwork established at the start of the program.

Analyzing the design for reliability

The second part of the design interface is the actual design and reliability analysis. The approach used is shown in the flow chart in Fig. 1. It begins with the establishment of the system reliability requirements, continues with the allocation of these

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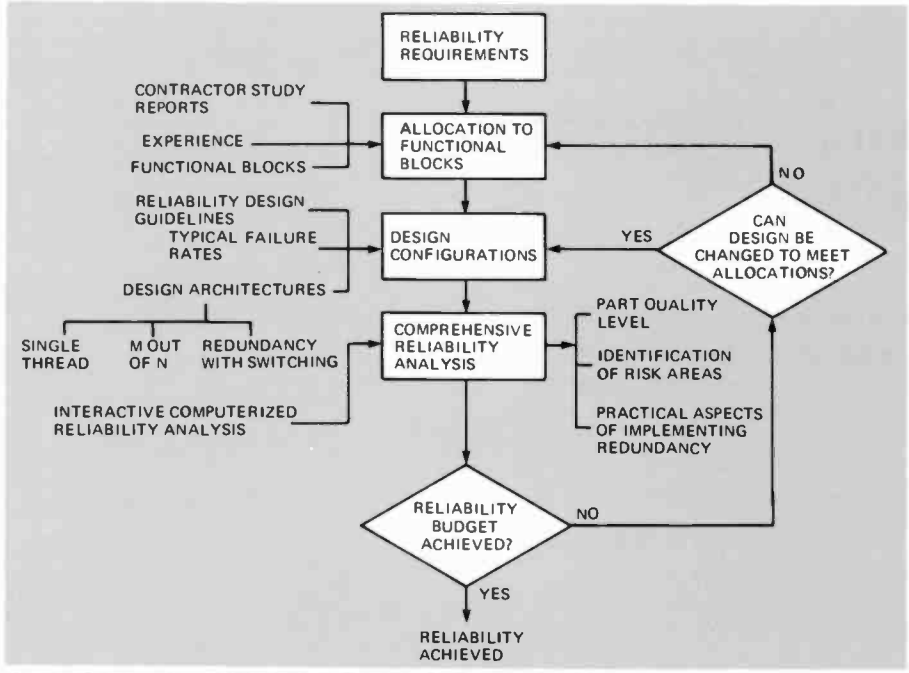


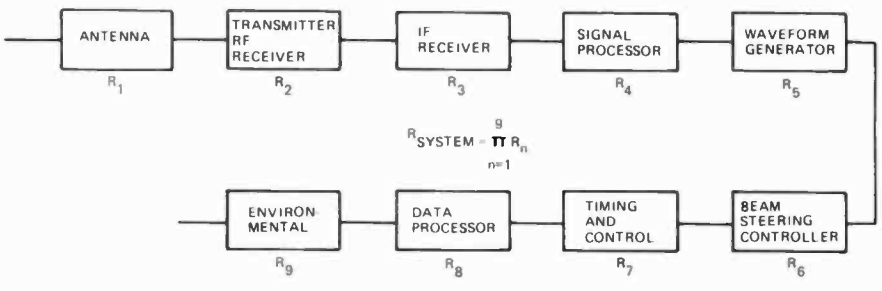
Fig. 1. This process builds reliability into the system design.

requirements to the subsystem elements, then moves into the design of the subsystems with reliability guidance, and finally results in a comprehensive reliability analysis of the candidate design. The design/analysis of the system is an iterative approach. Analysis results are fed back to the design process and, if these analyses indicate that the required performance is not being achieved, then either the design must be changed or the subsystem reliability requirements must be revised.

System reliability allocations

The customer's system reliability requirements (usually in the form of numerics) are allocated down to the subsystem level to form the basis of the design. These numerics may be in terms of reliability (probability of success), mean time between failures (MTBF), or failure rates, as appropriate, to provide a baseline against which a candidate design configuration is measured (Fig. 2).

After the system is defined in terms of a functional block diagram, with the systems engineer, the reliability engineer allocates the reliability requirements to each of the subsystems. This allocation process is not automatic. It is based primarily on the reliability engineer's judgment, experience with previous designs, and the anticipated complexity of the subsystems themselves. The initial allocations represent best early estimates, and are expected to change through adjustments as each subsystem design matures. Reliability of some subsystems may be found to be better than allocated, and some worse. The allocations are then changed for those subsystems having problems by decreasing the allocations for the more reliable ones.



R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{SYS}
.9999	0.9592	0.9779	0.9972	0.9851	0.9944	0.9900	0.9922	.9999	0.9

Fig. 2. This example of the allocation of system-inherent reliability numerics uses a typical radar design.

The systems engineer provides subsystem functional requirements to the designers, along with guidance on concepts for possible design approaches. At that point, the reliability engineer supplies the designers with the tools to enable them to develop a successful design: reliability design guidelines, reliability data on contemplated components, and design architecture considerations (Fig. 3).

The reliability design guidelines center around three keys: (1) voltage commonality, (2) design simplification, and (3) the reliability checklist. A positive design approach stresses these three key features.

Voltage commonality

Up to half of the unreliability associated with a given design may be due to the power supplies. The designer normally synthesizes his design with a goal of meeting a specific *functional* performance requirement, sometimes underestimating the impact of the support electronics necessary for the design to work.

As an example, assume that a design requires 200 discrete microcircuits, but could also be implemented with a single microprocessor. At first glance, the latter appears to be a more attractive alternative. But perhaps the microprocessor requires four different power supplies to make it work, while the concept using the discrete parts requires only a single power supply. The discrete design will then be more reliable unless a different microprocessor can be selected that requires only one, or at most two power supplies. As can be seen from this example, it is important to establish the power supply philosophy at the start of the design and to enforce it throughout the design process. Minimizing the numbers and types of power supplies not only improves system reliability, but also pays dividends in terms of logistics supportability and total program costs.

Design simplification

This key concerns itself with the goal of minimizing the number of parts used in a subsystem, and minimizing application of parts that require adjustment. After all, the parts cause a system to fail, so that if their number can be reduced, the system reliability will be improved. Designs that have broad tolerances or are self-adjusting are preferred over those that require use of adjustable parts (e.g., trimmer resistors and capacitors). Adjustable, variable-value

parts generally have higher failure rates than do fixed-value components.

The reliability checklist

This list serves as a reminder of undesirable component characteristics the reliability engineer and designer must look for in reviewing a proposed design. A representative partial list includes:

- unproven parts;
- parts subject to wearout, drifting, or heating;
- parts requiring adjustments or periodic realignment;
- parts requiring adjustment of other components upon replacement; and
- parts requiring supporting hardware (e.g., power supplies, amplifiers, potentiometers).

The literature includes examples of more extensive checklists that are useful in the formal design review process.

Component and subsystem designers need not be reliability experts, but they must have some knowledge of the reliability of the components they will be using in their designs. Part of the reliability engineer's job is to supply the designers with a listing of typical failure rates for items likely to be used in the design. These items, which may be either custom designed or purchased, include amplifiers, A/D converters, D/A converters, power supplies, tubes, semiconductors, and integrated circuits. Armed with this failure-rate information, the designers are in a position to make preliminary reliability assessments of their design concepts. They have an idea of potential reliability problem areas and risk areas, established very early in the design stage.

Computer-aided design architecture selection

The designers must consider a variety of design architectures in addition to the design keys and typical failure rates. These alternative design architectures are, of course, important, but they become critical in systems for which stringent system reliability requirements are dictated. Many types of architecture are available, including several of considerable complexity. For the purposes of illustration, three typical design architectures are considered here (and illustrated in Fig. 4): single thread, "*m* out of *n*," and redundant.

Single thread design

The first example is a single thread design (series reliability), in which any failure in the design causes the system to fail its operability criteria. The single thread design is basically appealing because of simplicity and low cost deriving from the use of a minimum number of parts. Fault isolation in a single thread design is also relatively easy, since any fault will make the subsystem totally inoperative. This is the selected approach for most general system designs.

m *out of* n *design*

The second type, "*m* out of *n*," is also categorized as parallel redundancy. This architecture is sometimes described as offering "graceful degradation" or being "fail safe." An example is a transmitter configuration that uses a group of paralleled transmit modules that can operate independently. When a failure occurs, there is a loss of subsystem performance, but enough residual performance remains to enable the subsystem to meet its performance criteria. The reliability of this architecture is far superior to that of a single thread design, but a price must be paid. The more complex design requires many more parts and complicates fault detection and isolation. Since the design is fault-tolerant, failures of individual blocks may not be recognized until the accumulated number of failures results in unacceptable performance. Thus, a method must be provided to assess the operability and perform fault isolation of the *m* out of *n* architecture. In spite of those complications, the *m* out of *n* architecture must be considered whenever the allocated reliability cannot be achieved with the single thread design and the allocations cannot be modified to accommodate it.

Redundant system design

The third type of design architecture, the redundant system, is usually applied only

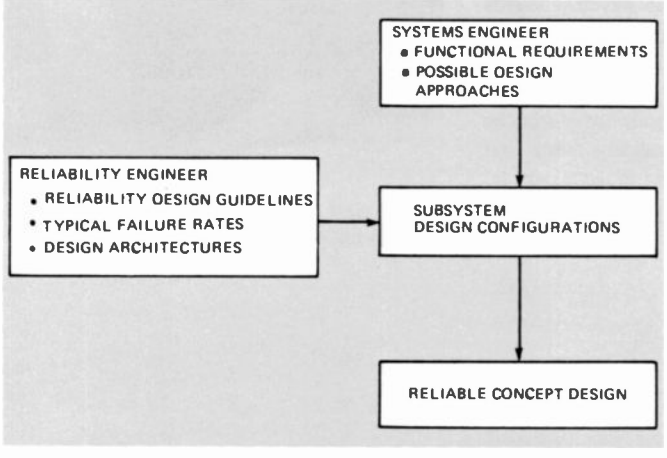


Fig. 3. Reliability engineers' contributions in conjunction with the systems engineer to subsystem design configurations result in a high reliability concept design.

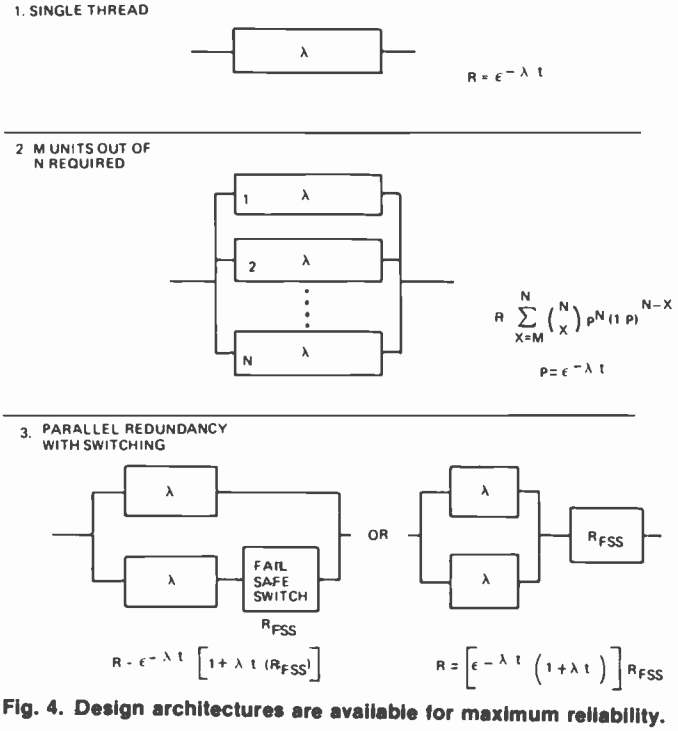


Fig. 4. Design architectures are available for maximum reliability.

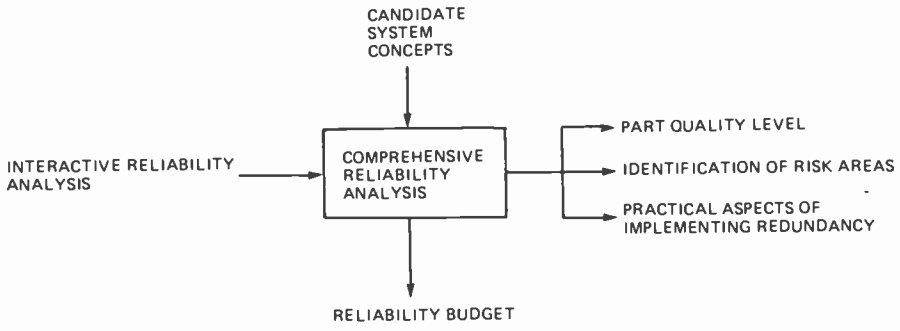


Fig. 5. An analysis of candidate system concepts provides reliability.

after the first two approaches have been considered and found inadequate (some designs cannot be synthesized into an *m* out of *n* architecture). A waveform generator, for example, may be required to supply a variety of local oscillator signals throughout the system. Normally, each of these signals is essential. To apply an *m* out of *n* approach to this problem, the designer must devise a system that will continue to work after the loss of any single local oscillator. Failing this, the last remaining architecture must be considered. It is a brute force approach to achieving reliability — the outright duplication of the function. This redundancy is the least efficient of the design architectures since it more than doubles the hardware required by the single thread design.

When this architecture must be used, the reliability spotlight focuses on the practical aspects of implementing the redundancy. Automatic fault detection and switchover capability become necessary, but may be too complex to implement with a practical amount of hardware. Reliability of the fault detection and switching functions may be worse than that of the function being made redundant. Accordingly, a failure modes and effects analysis is required for the switching scheme, since it is the critical item in the redundant system.

Designs that use a fail-safe switch are preferred. In these designs, the switching scheme has no failure modes that would prevent one of the redundant units from being connected to the rest of the system. Fail-safe switches are not easy to design, so the switching scheme is sometimes included in series with the redundant items. Regardless of the design chosen, the switching scheme is still the critical function.

After several concepts have been developed that are considered viable, the reliability engineer conducts a comprehensive analysis of the proposed candidates (Fig. 5). In this analysis, the reliability engineer determines the part quality levels that can be used to implement the design, identifies reliability risk areas, and studies any redundancy switching schemes. The computer provides the interactive capability for immediate feedback to reliability questions.

Since the design/analysis loop is an iterative one, the reliability analyses must be conducted rapidly during this phase in order to support the designers. A variety of interactive computerized analysis aids have been developed to help provide quick responses. The results of the analyses are fed back to the designers and, through repeated design/analysis iterations, a viable design is finally synthesized.

Conclusions

This computer-aided iterative approach to design for reliability was used recently on an Air Force program to develop highly reliable, unattended radars. The design synthesized using this design methodology received many favorable comments from the customer. Other methodologies may be just as workable, but judging from that experience, this one does indeed work. Its success requires full participation of the program manager, systems engineers, and design and reliability engineers in the process of designing reliability into the system. Reliability *cannot* be added after the design is completed.

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Sid Abbott, left, and Ted Schilsky review system concepts.

R.E. Killion

Achieving reliability in unattended systems

An unattended radar station poses the tough tradeoff of very low operating and maintenance costs vs. high design and initial purchase costs.

Abstract: *Radars and other surveillance stations in remote regions, (e.g., the Arctic), are now being designed to operate unattended for months on end. This imposes new standards of reliability, and the designers of these stations face two challenges: 1. to achieve the required reliability without eating up the cost savings afforded by unattended operation; and 2. to demonstrate, without prohibitively lengthy or expensive operating tests, that the high reliability has actually been achieved. This paper addresses the two challenges.*

Traditionally, surveillance and tracking radar systems in remote areas such as the Arctic are manned with sufficient numbers of operating and maintenance personnel to support around-the-clock operation. As a result, provisions must be made for billeting and messing, environmental comfort, on-site recreation, medical support, and furloughing for rest and recreation.

The cost of maintaining personnel at these remote sites has become an increasing burden on military budgets. Consequently, more and more consideration is being given to the feasibility of unmanned sites. This paper discusses the impact of unmanned sites on the reliability, maintainability, design, and test considerations of a remotely operated surveillance radar system. Only selected aspects of the total reliability effort will be addressed—specifically, those activities that are uniquely affected by this design concept.

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System concept

A generalized system concept will be described to serve as a basis for the reliability/maintainability (R/M) discussions. The R/M considerations discussed, however, are generally applicable to any system of unattended sites that can be visited periodically on a planned basis.

Figure 1 depicts a surveillance radar system in a remote Arctic region. This system consists of a series of radars; the series is made up of a repeating cycle consisting of one long-range minimally attended radar (MAR) and five short-range (gap-filler) unattended radars (UARs). A logistics node (LN) station, which supports the operation and maintenance of radar line, is located at the site of the MAR. In general, an LN can support one MAR and three UARs over a distance of 120 miles either side of the MAR. The LNs are in communication contact with a common remote operational control center (ROCC). Appropriate radar performance and operational status data is communicated to the ROCC via microwave links or satellites. Radar data collected at any UAR is automatically communicated via microwave link between UARs to the adjacent MARs, where the data is processed and communicated to the ROCC. Operationally, the loss of one MAR or two adjacent UARs will incur system downtime. An isolated UAR can fail without causing system downtime.

This paper focuses attention on the UAR and its relationship to the LN and ROCC, rather than the MAR. Because the UARs are unattended, both raw radar data and equipment operational status are transmitted digitally to the LN. When a failure occurs, a maintenance crew from the LN travels to the UAR site by helicopter to restore it to operation. Considering the distances involved, the weather, and the number of sites, one can see that high reliability and effective status monitoring are essential.

Customer requirements

A ground-based manual surveillance radar system usually has its reliability expressed in terms of availability. The user is concerned with maintaining an acceptable ratio of "uptime" to total calendar time over a specified interval.

Mean-time-between-failure (MTBF) is usually subject to a tradeoff with mean-time-to-repair (MTTR) when designing the system to meet a specified inherent availability. In the case of an unattended radar, MTBF takes on added significance. This reliability parameter is used to provide assurance that a probability of 0.9 or better exists that the radar can operate without a failure for a specified period of time. It is this period of time, designated as t_i in Fig. 2, that determines the provisions and personnel required at the logistics nodes to support the UARs. In various system-design concepts, t_i has taken on values ranging from 12 months to 1 month.

Station mean recovery time is a parameter unique to the unattended site. It specifies the mean duration of a site outage, and includes the time to automatically detect a fault, automatically notify the LN, travel to the site, repair, and check out. Actual values under consideration have ranged from one to four days. The longer periods take into account weather con-

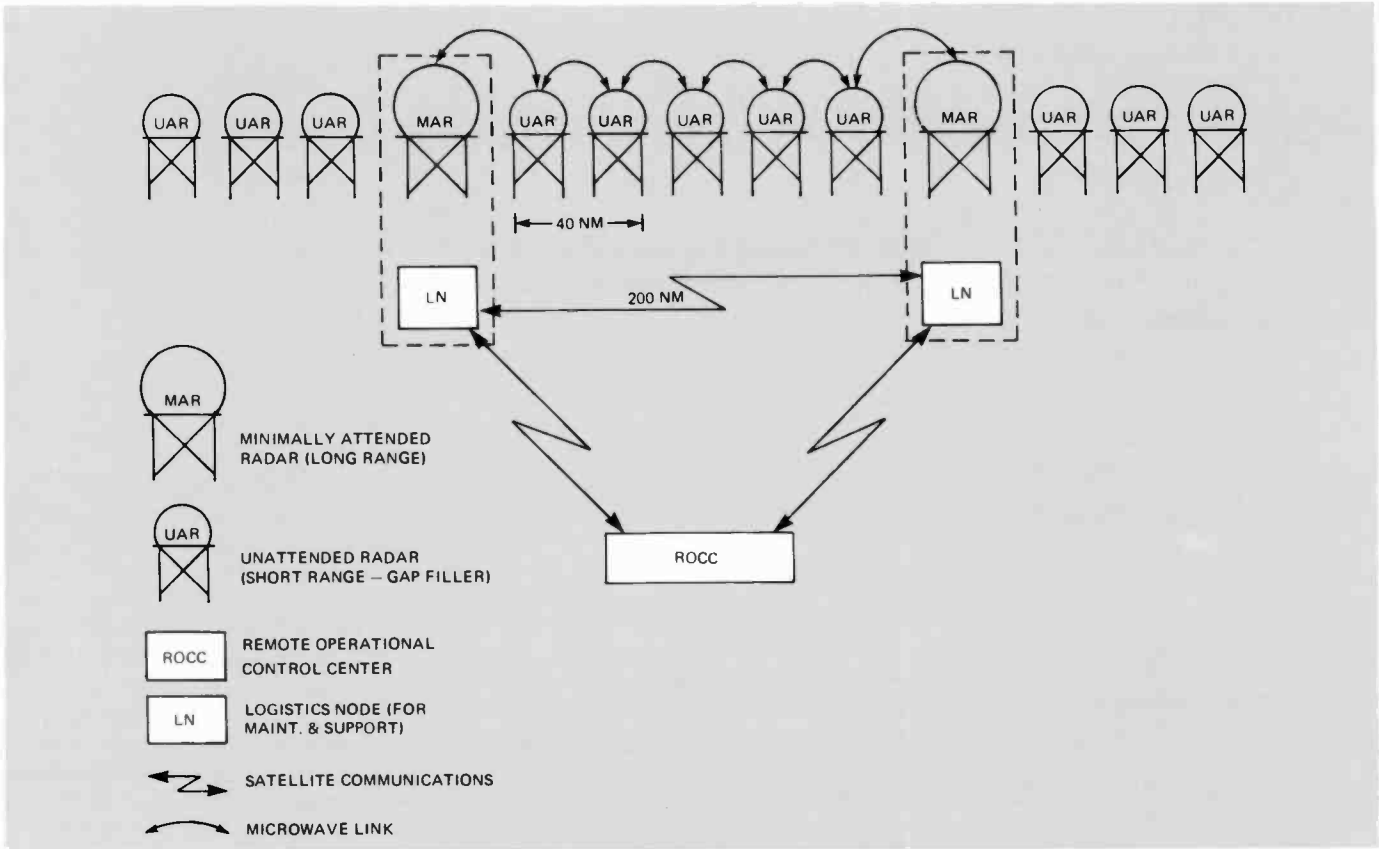

Fig. 1. Surveillance radar system consists of a repeating sequence of long-range and short-range radars. The long-range radars have minimal operating personnel and the short-range radars are unattended. A logistics node, or supply and maintenance center, based at each long-range radar, serves the unattended radars by helicopter. System design allows one unattended radar to fail without causing downtime.

ditions delaying access to the failed site. The combination of the station MTBF and recovery time must be compatible with the station availability requirement.

System availability is applicable to a group consisting of MARs, UARs, LNs, communications, prime power, and an ROCC. A UAR will affect system availability only if two adjacent UARs are in a failed state at the same time. The specified station reliability and mean recovery time assure a low probability of adjacent UAR failures.

Design considerations for reliability and maintainability

To achieve the specified reliability requirements, one should interpret those requirements in terms of design characteristics. In this particular case, unavailability (U), which is the complement of availability, is the parameter used.

$$\text{Unavailability} = 1 - \text{Availability}$$

$$U = 1 - A$$

Unavailability is appropriate because it is a function of all of the reliability parameters previously discussed: availability, reliability, and site recovery time. Inherent availability (A_I) is a design parameter, and

$$A_I = \frac{\text{MTBF}}{\text{MTBF} + \text{MTTR}}$$

Operational availability (A_O) recognizes, additionally, downtime sources other than equipment repair time (MTTR). These sources include site recovery time, travel time, and on-line preventive maintenance.

$$A_O = \frac{\text{Uptime}}{\text{Uptime} + \text{Downtime}}$$

If uptime plus downtime is considered to equal total time (T), then:

$$\text{Downtime} = \text{Unavailability} \times T$$

Downtime can be classified as scheduled or unscheduled. This classification is useful because either type of downtime can be controlled by specific design actions. Table I lists some of the design factors contributing to scheduled and to unscheduled downtime. Some of the design characteristics that we recommend avoiding would be perfectly acceptable if the radar site were manned; but in an unmanned site they are either completely objectionable or

Table I. Unavailability can be caused by scheduled (for regular maintenance) or unscheduled downtime (caused by failure). Both can be avoided by specific design measures.

Unavailability	
Scheduled downtime	
Avoid	• Limited-life items
Avoid	• Need for lubrication and cleaning
Avoid	• Need for alignment and calibration
Minimize	• Failure rate of redundant equipment
Unscheduled downtime	
Avoid	• Weak links (series elements)
	• High component failure rates
	• Operating for extended periods with no available back up equipment
	Causes —Ineffective fault detection —Long repair times —Unknown spares or test equipment requirements

they must be controlled to a greater than normal degree. Each item in Table I is discussed briefly to highlight its significance at an unmanned site.

Avoiding scheduled downtime

The following tend to contribute to scheduled downtime:

- *Limited life items.* These include the bearings, motors, and lubricants associated with rotating electromechanical antennas, and powered fans and mechanisms. The use of these items is undesirable because their needs for periodic maintenance and replacement run counter to the concept of an unmanned site. An electronically steerable array could eliminate most of these downtime contributors.
- *Lubrication and cleaning.* These requirements are closely related to the use of bearings and the filters associated with forced-air cooling systems. Because the site is unmanned, the ambient temperature can be maintained low enough to avoid the need for air cooling. Good derating policies also aid in reducing the Δt associated with the operating equipment temperature rise.
- *Circuit stability.* This is essential to prevent drift and avoid the need for scheduled realignment and calibration. Circuit stability also helps reduce or eliminate the need for alignment and calibration when assemblies are replaced at the organizational level during repairs.
- *Redundancy.* When the need for redundancy is established, a decision must be made about the level of unit reliability to be specified. This is one of the many cost-tradeoff decisions that must be made. The unit reliability, expressed in terms of failure rate, must be such that there is a very low probability of a second failure during the period of time that one of the redundant units is down awaiting repair. The reliability of a unit can be varied by varying the quality/reliability level of its parts or by derating the parts. For example, the failure of unit 1 in Fig. 3 would not cause site downtime because an operational unit 2 would satisfy the site performance needs. Unit 1 could possibly fail months before any scheduled or unscheduled visit to the site. Consequently, the unit reliability level should reasonably assure that unit 2 could survive until at least the next scheduled visit and thus not cause site downtime. A low unit reliability means shorter time between scheduled visits to the site to restore the site to its full reliability level.

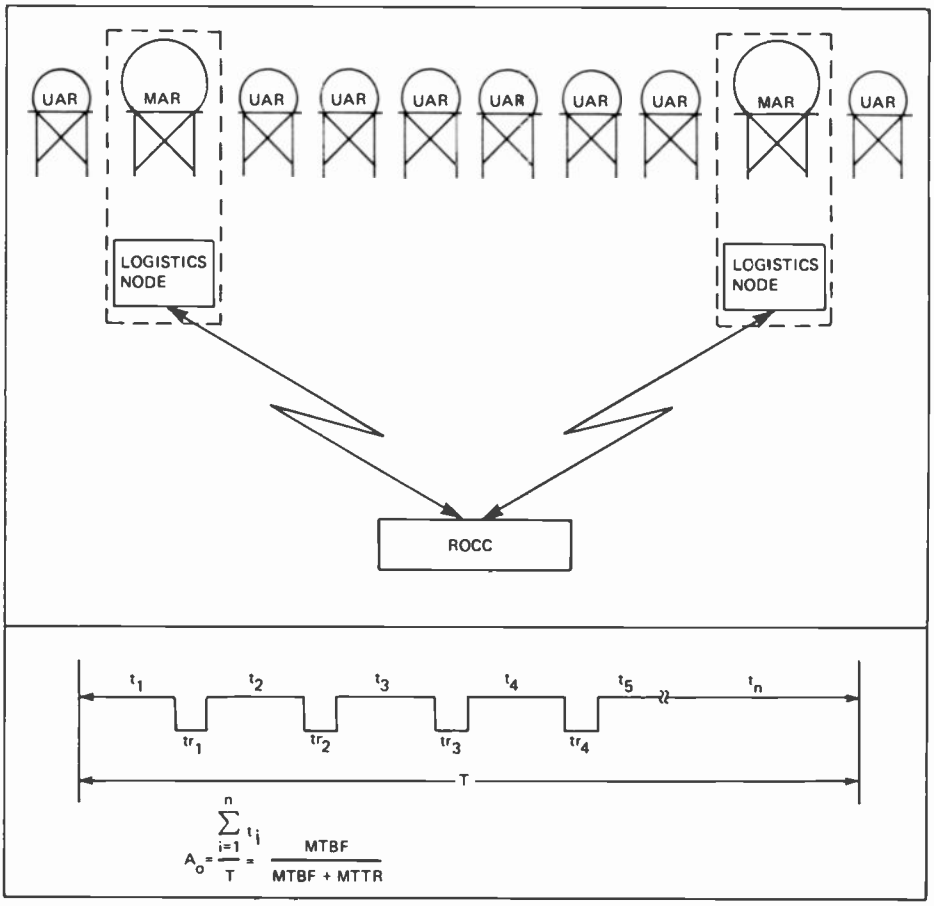

Fig. 2. System operational availability depends upon the availability of the individual radars.

Avoiding unscheduled downtime

The preceding design considerations would affect the amount of scheduled downtime a particular site might incur. System design must also take into account the vulnerability of the site to unscheduled downtime. "Unscheduled downtime" in Table I identifies the following design characteristics that would tend to increase the probability of unscheduled outages.

- *Weak links.* This refers to the series elements in the reliability model of the site equipment. Ideally, all series elements would be eliminated; but sometimes this is not practical, as with the UAR site timing and control circuitry, which has multiple interfaces with other hardware. In such cases, three approaches can improve the reliability of any series function; all three should be applied. They are: circuit simplification, part derating, and use of high-reliability parts.
- *High-failure-rate parts.* Another factor contributing to unscheduled downtime is the use of parts with high failure rates. Obviously, this is totally unacceptable for series functions, and is frequently almost as unacceptable for units in redundant configurations. As stated earlier, the use of high-failure-rate parts increases the probability of losing the backup equipment and, even more important, of incurring a site failure if all units in a redundant configuration fail. The reader might question why anyone would even consider using a part with a high failure rate, and suggest that this is not a realistic problem. Unfortunately, it *is* a realistic problem, and for either of two reasons. Some parts are inherently unreliable as a result of their construction, while others are unreliable because of their applica-

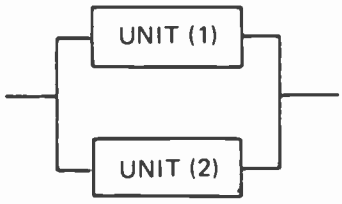

Fig. 3. Redundant units avoid unscheduled downtime. Failure of unit 1 would not cause system downtime. However, at least one unit must not fail between scheduled maintenance visits.

Failure detection and isolation

The impact of failure detection and isolation on system availability takes on special importance in unattended systems. This subject is treated here in terms of the factors that have the greatest influence on failure detection and isolation.

Assume that it is possible to quantize the probability that a failure will be detected and isolated to permit repair within a specified period of time. If we designate this probability as P_{DI} then it is apparent that system availability will be degraded as P_{DI} deviates from unity.

$$A_S \times P_{DI} = A_{S(eff)}$$

where:

A_S = system availability

P_{DI} = probability of effective failure detection and isolation

$A_{S(eff)}$ = effective system availability

Two factors can cause P_{DI} to be less than 1.0:

1. The probability of failure of the fault detection and isolation hardware or software.
2. The level of coverage capability built into the fault detection and isolation fuction; that is, what percentage of failures was it designed to detect?

The first factor can be handled in a straightforward manner by making a reliability prediction of the built-in test equipment (BITE) and calculating the probability of failure-free performance between scheduled checkouts of the BITE. The second factor, controlling coverage capability, is more of a challenge. It can be greatly influenced by the complexity of the BITE design, the size of the lowest replaceable unit (LRU), and the skill of the maintenance personnel. Each of these influences is discussed below.

BITE design

Two alternative approaches can be applied to BITE design for large systems such as the conceptual unattended radar discussed in this paper. In the first, BITE is a centralized function, with stimuli and sensors directed to and embedded in the various radar elements (including support functions such as prime power and environmental control facilities). In the second approach, BITE is built into each of the radar functions and each functional BITE operates independently. Either approach can be applied effectively but the concept of a unique BITE for each major function offers some advantages that can enhance the overall BITE performance.

Prominent among these advantages is the design approach itself. A complex, centralized BITE requires a major design effort that tends to become competitive rather than integral with the design of the system functions. In contrast, the multiple-BITE approach places responsibility for BITE design with the designers of the various system functions, thereby assuring equal priority of effort by the designers most familiar with a specific function.

LRU size

The size of the lowest replaceable unit greatly impacts BITE complexity. Military customers tend to drive LRUs to smaller and smaller sizes, principally because smaller LRUs are less expensive and have low failure rates. On the surface this seems desirable. However, the military supply systems are still using criteria that penalize equipment using these inexpensive, low-failure-rate LRUs. For example, the supply systems frequently exclude these items from their spares lists. And this exclusion means reduced operational availability when failures occur and spares must be obtained from a remote location.

tion. Typical examples are non-wirewound trim pots and microwave power transistors. Trim pots should not be used in unmanned systems, even if the purpose of the trim pot is limited to factory adjustment. When using microwave power transistors in a transmit module, there is a tendency to drive the devices too hard, rather than add another device in the circuit to achieve the desired output. This application causes high junction temperatures and pushes the failure rate up significantly.

- *Operating without backup.* This class of design characteristics results in prolonged operating periods without redundant backup after a unit failure has occurred. Because we are dealing with an unmanned site, effective fault detection and remote status reporting are essential. Both timeliness and accuracy of fault detection are critical. If a given fault were to go undetected, the consequence could be extended operation of the equipment without benefit of backup for some critical function. If the fault-detection system is not adequately specific, larger complements of spares and test equipment may have to be transported to the site to cover a wider range of failure possibilities. An even more serious consequence would be that of maintenance personnel taking the wrong test equipment or spares to the site.

The need to restore equipment rapidly to full operational status also places greater emphasis on packaging design to facilitate access and reassembly. Packaging designers must consider the working conditions resulting from the Arctic climate and the fact that equipment shelters are not heated for personnel comfort. The equipment shelters will be mounted on elevated platforms to assure unobstructed radar operation. Therefore, maintenance personnel must know what spares and test equipment are needed before they leave the LN and before they climb the towers to the equipment locations. A concept proposed to further enhance the monitoring and status reporting from the UAR to the LN is the use of a portable tester that could be plugged into a connector panel at the foot of the tower to aid in fault localization. This would further reduce the chances of carrying the wrong spares, tools, or test equipment up the towers.

The unattended radar concept affords a good example of the treatment of reliability and maintainability as design parameters.

R/M cost tradeoffs

Nothing highlights the importance of considering R/M during the early design concept effort better than the results of related cost-tradeoff studies. It is not the intent here to discuss cost-tradeoff methodology, but rather to identify some

Another undesirable outgrowth of small LRUs is increased complexity in the BITE subsystem, with a greater probability of failure and a greater probability of ambiguous fault causes, all resulting in fault isolation uncertainty. The point here is that the smallest LRU is not necessarily the most desirable. BITE complexity must be considered as well as the spare parts criteria used by the supply organization.

Maintenance skills

Complexity of all military equipment, including BITE systems, is driven by the lowest maintenance skill levels available at the initial maintenance level. These skill levels have been decreasing in recent years, making it necessary to design diagnostic equipment that has a high probability (>95%) of detecting and isolating faults without the aid of maintenance personnel. This kind of system design, of course, is expensive — sometimes prohibitively so. One result on some procurements is that compromises are made that adversely affect long-term performance. Clearly the military services must seriously consider the impact of decreasing maintenance skill levels on system operation.

of the more significant cost tradeoffs associated with the design of unattended systems.

The most important tradeoff is between acquisition cost and operation and maintenance (O&M) cost. The motivation behind the unattended design concept is the reduction of O&M cost. In this design concept, O&M cost reductions are easily identified and measurable. The most significant factors contributing to this cost reduction are the following:

- No full-time personnel at the UARs.
- A centralized support crew (at the LN) that services up to seven sites.
- Centralized spares, resulting in an overall spares-inventory reduction.
- Reduction in fuel usage, because of no need to provide personnel comfort.

On the other hand, the acquisition cost of this type of system is significantly higher than the conventional system at a manned station. The reasons for this additional cost are also obvious:

- Duplicate equipment and circuitry for redundancy.
- Sophisticated remote monitoring and status reporting.
- A more intensive design effort to achieve the required reliability.

The challenge to the system designer is to accomplish these objectives within present-day acquisition dollar constraints. No matter how impressive the O&M cost savings, they will not create the unlimited instant financial resources needed to acquire the initially expensive system capable of achieving the O&M cost savings.

All other costs tradeoffs pale into insignificance by comparison with the preceding one. There are, however, some others worth mentioning. One in particular is related to the piece-part reliability of those parts used in redundant equipment. Ideally, we would like to use the most reliable parts obtainable, but their use may impose penalties such as cost and procurement difficulties. In general, we should use the best parts we can procure within our dollar and schedule constraints, as long as the reliability of these parts supports the equipment reliability requirements.

It would be helpful for future design efforts if we could generalize and state that it is always better to use high reliability parts in a series configuration than it is to use military-quality parts in a redundant configuration. Unfortunately the solution is not that straightforward, and as a result the approach must be tailored to each problem. There are too many factors, some of which vary with time, that impact the approach used. Parts costs and availability in the marketplace are not stable enough to standardize on a preferred approach. The complexity of some system functions rules out techniques that would be perfectly valid for another function. But there is a bright side to this situation: it precludes "cook book" approaches that trap reliability engineers into providing answers without detailed knowledge of the design.

Some equipment designs do not lend themselves as easily to total redundancy as others. Rather than duplicate, for example, an entire signal processor or data processor, it may be more realistic to use a combination of serial and redundant paths within these major radar-system functions. Cost and reliability should be two of the factors used to make this decision.

A final design consideration that lends itself to a tradeoff of cost, reliability, and maintainability is the level of sophistication designed into the monitoring and status-reporting system. The question that must be answered is, "What is the consequence of an erroneous report?" In this design concept, the consequences would be increased site downtime, a higher probability of system downtime, and a loss of confidence in the remote monitoring system, which may undermine the overall concept of an unmanned system.

Reliability measurement

Demonstrating very high reliabilities

Formal demonstration of the reliability of the unattended system can be a challenging task. It is difficult to run a meaningful reliability demonstration test when the inherent reliability of the system is so high that it results in few failures and thus forces a lengthening of test time, an increase in the number of items on test, and a reduction in the statistical confidence in the test results. Although this system is relatively complex, based on a parts count, the use of redundancy, an M-out-of-N antenna configuration, and a built-in capability to degrade gracefully to an unacceptable level could result in an overall UAR MTBF of approximately 80,000 hours. (This would be the time between those failures that cause site downtime.) A conventional MIL-STD-781C test would require a test duration of at least three times the MTBF, or 240,000 hours (almost 27.5 years)! This is obviously impractical, and the nature of the system does not permit the use of multiple test samples as a means of reducing test time.

MTBE vs. MTBF

The paradox to be resolved is how to design a very reliable system, yet one that fails frequently enough to permit the use of conventional reliability demonstration test techniques. A solution to this enigma exists if we redefine failure. It was previously stated that the system under consideration has an MTBF of approximately 80,000 hours, and this estimate considers only failures resulting in UAR site downtime. However, if we consider all hardware failures, including those that merely degrade performance to a lower but acceptable level, we can estimate a new value of MTBF. To avoid confusion, this new estimate should be renamed mean-time-between-events (MTBE). This same site

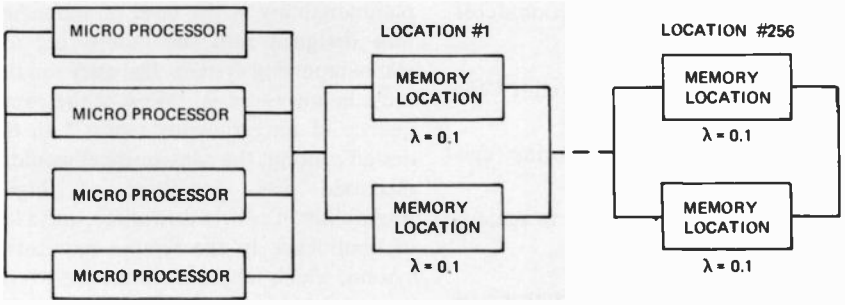

Fig. 4. Data-processing subsystem uses redundant memory locations. For subsystem to fail, both memories at each location must fail. This typical simplified system is used to explain MTBF vs. MTBE in text.

with an MTBF of 80,000 hours would have an MTBE of approximately 600 hours, or 14 failures per year. We can now deal with the problem more realistically. There are, however, new problems to be resolved. It is conceivable that we could pass the MTBE test and still fail an MTBF test if all or most of the events were associated with the same portion of a given subsystem.

Consider a data-processor subsystem such as that in Fig. 4. For the data-processor subsystem to function properly, at least one of the two memories at each of the 256 locations must be operable. Let us assume the test requirements and results shown in Table II.

Comparing the test conditions with the test results, one sees that the resulting failure events were less than the maximum allowable, and based strictly on MTBE criteria it could be concluded that the system passed the test. But since both memories in the same data-processor memory location failed, the data processor failed; and so based on MTBF criteria, the entire system failed. Even if the coincident failures had not occurred, the occurrence of six memory events in six months would be equivalent to a total data-processor memory (256 x 2 = 512 memories) failure event rate of 1370 failures/10^6 hours compared with a predicted rate of 51.6 failures/10^6 hours. This excessive rate means that even if coincident failures had not occurred during the test, a significant probability exists that they could occur during normal operation.

Table II. Pass or fail? It depends upon the definition. These data show a system that fails via MTBF criteria, yet passes via MTBE criteria. MTBE criteria must therefore be modified slightly to give meaningful results.

Test conditions	
Total test time	6 months
Number of systems on test	1 system
Allowable failure events	10 events
Test results	
Test duration	6 months
Total failure events	8 events
• Data-processor memory failures	6 events*
• Transmitter module failure	1 event
• Low voltage power supply failure	1 event

*Two memories in the same memory location failed.

The conclusion we must draw from this example is that passing a straight MTBE test does not provide adequate assurance that we can pass an MTBF test. Some additional accept/reject criteria are needed. The following three criteria must be met:

1. Total allowable MTBE events must not be exceeded.
2. If coincident failures occur that would result in a system failure (MTBF), the specified probability of occurrence of system failures must not be exceeded (i.e., a 90 percent probability of failure-free operation for a specified period of time must be achieved).
3. Whenever multiple failures of a system function that is redundant (backed up in some manner to minimize system failures) occur, there must be less than a 10 percent chance that the number of failures could have occurred by chance if the predicted failure rate were valid.

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These additional controls should provide greater confidence that the MTBE test results are an accurate indicator that the MTBF specified (or required to support the specified probability of failure-free operation) is, in fact, achievable. A statistical reliability demonstration test should not of itself justify a feeling of confidence that the system will perform reliably under normal field usage. It is essential to overlay on this approach an effective "test and fix" concept to assure that failure causes disclosed during the test are actually eliminated through corrective action that is verified by test under realistic operating conditions.

Conclusion

Unattended systems of the type described are technically feasible. Their design imposes a significant level of design discipline beyond that required of conventional systems. Probably the biggest challenge is limiting the acquisition cost of the system, because the design concept is inherently expensive.

V. Ragavan|M.R. Paglee

A microprocessor-controlled data display system

Easily written software replaces complicated hardware for the performance of complex interpretive functions. The result is increased system reliability.

Abstract: *This paper deals with the application of a microprocessor in a display system which indicates the status of two unmanned radar receiver sites at the Kwajalein Missile Range. The Z-80 microprocessor is used to drive four display panels, containing lamps and digits, based on a set of 32-bit words received from the two sites.*

The microprocessor in the system allows flexibility in interpreting the bit pattern of the input word set. Changes in the input bit assignments which may arise from modifications of the overall radar system could be implemented merely by rewriting the software and "reburning" programmable read-only memories (PROMs), thus avoiding substantial modifications in the hardware. A simulation/checkout program has been incorporated into the system to aid in debugging of new software as it is written. The detailed operation of the microprocessor hardware and software is described.

How the system works

A microprocessor affords a number of advantages in analyzing and responding to complex bit patterns. Particularly important is the flexibility inherent in its use within a system which is subject to modification in these bit patterns. Because bit recognition is accomplished by software, changing the system merely involves a change in software and "reburning" a few programmable read-only memories (PROMs).

The Z-80 microprocessor was, therefore, selected to drive a set of data display panels based on a group of input bits. The system to be monitored is presently being installed in the Kwajalein Missile Range and consists of radar receivers located at two remote island sites. Because these receiver sites are essentially unmanned, a status display system located at the main radar control center becomes necessary. This system displays the status of various receiver functions and the receiver site environment. It provides continuous monitoring of the sites so that corrective action can be taken if abnormal conditions arise. In addition, the display panels can check proper functioning of the digital data link and the receiver equipment.

The status display system receives a group of 32-bit words from each remote site. These words contain all the information necessary to drive the digit displays and lamps on the display panels.

The Z-80 microprocessor analyzes this input data, turns on specified lamps, and loads specific numbers into the appropriate digit displays on the panels. The input data are updated every 100 ms. The Z-80 in the system takes approximately 30 ms to analyze and respond to the data from both sites. Hence, it can respond to every change in the input and update the panel displays accordingly.

The Z-80 software consists of two programs. One program performs the analysis of the input data and drives the panels; the other program simulates the Z-80 central processing unit (CPU) and allows execution of instructions in the single step mode, thus facilitating the checkout of new software or modifications of the existing software.

System hardware

As presented in the system diagram of Fig. 1, the hardware in the system consists of:

1. The Z-80 CPU and its clock and control circuits.
2. 8-K of PROM memory containing the firmware and PROM tables, and 256 bytes of random access memory (RAM) containing the program stack and several dedicated, as well as scratchpad, memory locations.
3. Two input buffer memories, each dedicated to a remote site. These memories contain four 64 x 8 bipolar RAMs and can store up to sixty-four 32-bit status words from each of the two sites.
4. Two output registers which are loaded periodically by the microprocessor. The data in these registers are transmitted

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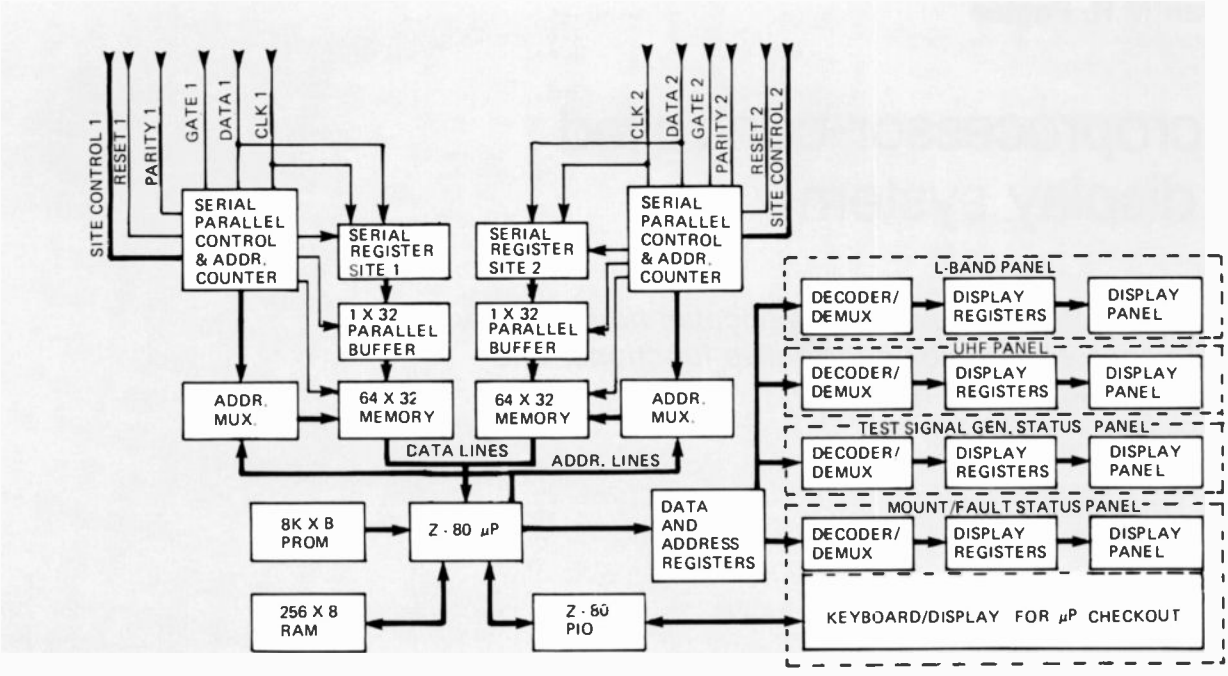

Fig. 1. The microprocessor-controlled data display system monitors antenna mount, wind conditions, fault conditions at the remote sites, plus the operation of the microprocessor.

through differential line drivers/line receivers and twisted-pair cables to the four panels.

5. A Z-80 parallel input/output (PIO) chip which implements the interface between the Z-80 CPU and the keyboard and microprocessor control switches located on the mount fault panel.
6. Four distinct status panels, the L-band receiver status panel, the UHF receiver status panel, the test/signal generator status panel, and the mount/fault status panel. Each panel contains its own decoding logic and is driven by data in the output registers.

The mount/fault panel at the upper left of Fig. 2 contains digital azimuth/elevation (AZ/EL) readouts of the antenna mount as well as wind conditions, light emitting diodes (LEDs) displaying the existence of fault conditions at the remote sites, and three rows of 32 LEDs showing contents of corresponding thumbwheel switch. In addition, the mount/fault panel contains the keyboard, address/data displays and control switches, all of which allow the operator to check out microprocessor operation.

The other three panels are mounted vertically at the right in the photograph. The test-signal generator panel at the top gives information regarding test signals inserted at various points in the receiver electronics; the L-band receiver panel and the UHF receiver panel at bottom right contain LEDs inserted at different points in the receiver block diagram. These LEDs, when lit, indicate the signal path through the L-band and UHF receivers, respectively. Some digital displays on these panels indicate, among other things, the magnitude of attenuation at specified points in the receiver. The hardware is housed in one unit (bottom left in the photograph) and is connected by cables to the four status panels.

Input buffer memory

The microprocessor is reset every 100 ms by a reset pulse on one of the input lines. It can also be reset by a reset switch on the microprocessor control keyboard located on the mount/fault panel. The system can be operated either in remote or local mode and this is controlled by two switches located on the microprocessor control panel. In remote mode, the input buffer memory can be loaded with data from the remote sites and the input reset pulse is applied to the microprocessor. In local mode, the buffer memory cannot be loaded from the input data lines and only the reset switch on the control panel can reset the microprocessor. The operator can load data into memory in local mode and, by observing the display, run through a complete test of the software. New software can also be debugged in the local mode using the single step facility.

In remote mode, the 32-bit words from the remote sites are strobed in serially into 32-bit registers. Control logic at the input arranges each input word into four bytes and writes it into buffer memory. New data is received every 100 ms and all of it is received within a 5-ms slot in the 100-ms interval. During the data read-in interval, the microprocessor is placed in a wait state and its operation is suspended. During the remaining 95 ms, the microprocessor is in the normal operating mode. The input buffer memory can be accessed by the microprocessor only during the time the data is not changing.

Display registers

The microprocessor analyzes the input data based on the firmware stored in PROM. It derives several pairs of output words which it loads sequentially into the two output registers using strobes generated by decoding the I/O control lines of the microprocessor. The I/O control signals are initiated by the implementation of I/O instructions by the CPU. Each pair of output words consists of an 8-bit data and an 8-bit address word. The 8-bit data word in the pair is eventually loaded into a particular display register in one of the four panels and the corresponding 8-bit

address word determines the register into which the data word is loaded. The data word in each pair is loaded into the output data register before the address word so that the data are stable when the latter word is decoded and a particular display register is selected.

The data from the output registers are transmitted to the four panels through differential line drivers and twisted pair cables. All four panels receive identical data. The address and data words are strobed into two buffer registers at each panel. The data word is applied to all the display registers in the panel, and the address word is applied to the decoding logic. The data are loaded into one particular display register depending on the address word.

The eight bits of the data word can either drive eight LED lamps on or off, depending on the state of the bits, or can contain two 4-bit binary coded decimal (BCD) digits to drive two specific digit displays. In the latter case, BCD to 7-segment decoders are used to drive the displays. In the former case, open collector transistor-transistor-logic (TTL) buffers are used to drive the individual lamps.

In some cases, the data word may contain fault bits which signal the existence of an abnormal or undesirable condition in one of the two remote receiver sites. The lamp corresponding to this bit needs to be latched on and remain in that state even if the fault condition ceases to exist. In order to accomplish this, the fault bit is applied to the inputs of a flipflop which serves as the display register, and the strobe derived from the address word is used to latch the flipflop on, thus, keeping the lamp on until the flipflop is cleared by a RESET LATCH switch.

To summarize, the display registers in the panels either drive lamps, digital displays or fault lamps which, if turned on, are latched in that condition until the operator clears them.

PIO control lines

The Z-80 CPU interfaces with the keyboard, data and address displays and the control switches on the microprocessor control panel through the Z-80 PIO chip. The PIO is connected to the CPU data bus and is controlled by the CPU control lines and a few of the address lines. It contains two 8-bit I/O ports which can be configured in the input or output mode under control of the CPU. In the input mode, the PIO reads in 16-bit address words (using both ports) or 8-bit data words (using port B) from the microprocessor control panel. In the output mode, the PIO transfers 8-bit data words through port B to the data display on the control panel.

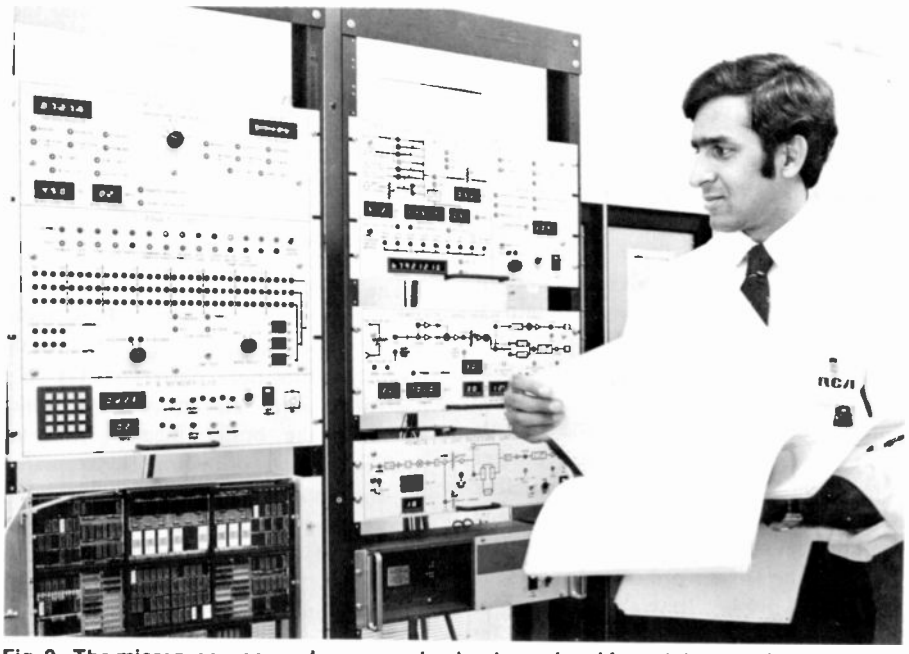

Fig. 2. The microprocessor and memory checkout panel and four status panels give data for antenna mount, wind conditions, microprocessor operation and test signal information.

Memory access is not achieved through direct memory access (DMA). It is under microprocessor control in the course of an interrupt service routine. During the interrupt, a 16-bit address is fetched from the PIO ports, and the data stored in that location are transmitted through the PIO to the keyboard data display. Similarly, an 8-bit data word from the keyboard data register can be written into a location that has just been examined.

The hardware described makes up the shell of a flexible display system. Merely by executing a few output instructions, the microprocessor can load data into any of the display registers. The firmware stored in PROM thus provides the intelligence, and converts the hardware into an operating, reliable display system which can be easily modified, if system changes make that necessary.

System software

The software, which is the heart of the system, consists of two main programs. The first program, stored in 2 K of PROM and utilizing tables stored in an additional 512 bytes of PROM, directs the microprocessor to read the input words from buffer memory, and based on this input data, load the display registers in the panels with appropriate output data.

The second program stored in PROM contains the keyboard service routine and occupies 1.5-k bytes of memory. This program allows the operator to write into memory and to debug new software.

I/O program

Input words. The first five input words contain a binary representation of the AZ and EL pointing angles of the receiving antenna. Each of the five 32-bit input words consists of one 16-bit AZ reading and one 16-bit EL reading. The five readings correspond to samples taken at the 0 ms, 20 ms, 40 ms, 60 ms, and 80 ms points within the 100-ms interval. The 16-bit readings are converted by the software to milliradian readings using a table look-up. Each of the five readings is preceded by an AZ/EL select word which is loaded into an AZ/EL select register in the mount/fault panel. This word is compared to a word generated by the AZ/EL select switch on the panel and if the two words are the same, the corresponding AZ and EL milliradian readings are read into the AZ, EL encoder displays.

In most cases, the word that is sent to a particular data display is derived in a relatively simple manner from a group of bits in one of the input words. In other cases, some computation, table look-up, and binary to BCD conversion is required to derive an output data word from a group

of bits or an input word. Similarly, in most cases, output words that are used to drive lamps are derived directly from an input bit sequence, while in a few cases some bit manipulation is performed on the input bits to come up with the output bits.

Besides loading the display registers of all the panels, the software transmits each 32-bit word to the three 32-bit word displays on the mount/fault panel. Each of the three 32-bit word displays contains a thumbwheel switch which determines which word is to be read into that particular word display. Prior to outputting any 32-bit word, the microprocessor sends out an 8-bit word number consisting of two BCD digits. This number is compared to the two digits of each thumbwheel switch, and if the numbers are identical, the 32-bit word is loaded into the 32-bit word display. In this manner, any of the 32-bit words in the input buffer memory can be read directly into one or more of three 32-bit word displays.

The word display operates in either the manual or automatic mode. In manual mode, the word displayed corresponds to the thumbwheel switch setting. In automatic mode, the thumbwheel switch setting is overridden when one of several specified fault conditions exists. Under these conditions, the word containing the fault bit or group of bits is automatically latched into the word display. This is accomplished by loading a certain address into the address register. The address decoder in the mount/fault panel containing the word display generates the strobe used to latch the fault word into the word display.

Site switch. One of the features of the first program is that it incorporates a software site switch. Each panel contains a site switch which allows the operator to select the site data that is to be displayed on that particular panel. The UHF panel does not have a site switch because only one of the two remote sites (ILLEGINI) has the capability of receiving UHF data. The site switch is implemented by the use of both hardware and software.

The most significant bit of each address word determines the site with which the data is associated. It is compared with the site switch output and if the data is not associated with the site selected by the site switch, the decoding logic is disabled and the data are not read into the selected register. The interpretation of the input bits is independent of the site at which the data originated. Hence, the same software can be used for data from either site. Only a few parameters need to be changed and they are:

1. The starting address of buffer memory corresponding to the site to be analyzed.
2. Bit 7 (the MSB) of all locations in RAM containing display register addresses, which are eventually loaded into the output address register.

The Z-80 16-bit index registers I*X* and I*Y* are particularly useful. If the index register contains the starting address of the portion of memory corresponding to a particular site, all instructions which reference the buffer memory can use relative indexed addressing. Hence, merely by changing the contents of the index register at the beginning of the program, the data from the selected site can be analyzed.

At the end of the program, bit 7 of all RAM locations containing display register addresses is changed to the opposite state, so that during the subsequent traversal of the program the addresses loaded into the address register will allow the other site data to be selected.

The total amount of time taken by the main program to analyze data from both sites is approximately 30 ms. Hence, it utilizes 30 percent of the time available between reset pulses. This leaves enough time for expansion of the software in the event of future modifications.

Read/write program

This program consists of approximately 600 lines of assembly code and performs two main functions:

1. It allows the operator to examine and write into any memory location, including the input buffer memory, from the keyboard located on the mount/fault panel.
2. It allows the operator to debug any new software by executing the instructions one step at a time and examining all microprocessor registers after each step.

Keyboard service program. The main program which drives the panels is independent of the keyboard service program which is entirely contained in two interrupt routines that are executed only under program interrupt conditions.

The Z-80 PIO chip contains two I/O ports each of which can generate an interrupt with a unique interrupt vector. The Z-80 is placed in Interrupt Mode 2, which allows the interrupting device, in this case, the PIO, to load the Z-80 data bus with the lower order 8 bytes of the location that contains the starting address of the interrupt routine. The higher order 8 bytes are obtained from the interrupt register in the CPU. Hence, an interrupt generated by either port of the Z-80 PIO instructs the CPU to jump to the starting address of the interrupt routine associated with that port.

The Port A interrupt routine examines memory locations specified by the operator and loads the contents of that location into the data display at the keyboard. This interrupt routine also interrogates the operator to obtain the single step starting address, end address, and number of instructions to be executed per step.

The Port B interrupt service routine writes data specified by the operator into a previously examined memory location. The Port B service routine also contains the single-step program.

Single-step program. The single-step program is entered by keying in address 'FFFF'. Once it is entered, the top of the program stack is loaded with the beginning location of an infinite loop, hence, when return from interrupt is executed, the program enters the infinite loop and waits for operator action. After the preliminary single-step information has been keyed in, the single-step program in the B service routine is entered when the operator depresses the single-step switch.

This program fetches and executes the next instructions or group of instructions, saves the contents of the registers, and waits. The registers can then be examined to observe the effects of the instructions.

The program first ensures that the next instruction address is not greater than the last address specified. It then determines the number of bytes making up the instruction and jumps to one of four routines depending on whether it is a four-byte, three-byte, two-byte, or one-byte instruction. In each case, the entire instruction is transferred to a specified location in RAM. The contents of the registers are then retrieved; the program jumps to the location at which the instruction is stored, executes the instruction, and jumps back to the single-step program. The register contents which may have been changed by the execution of the instruction are then immediately saved.

The single-step program, therefore, simulates the major registers in the Z-80 CPU and simulates, in software, the instruction decode hardware. The PC and all registers are accessible during the entire course of a single-step operation and can be

examined and changed after or before execution of any step. Hence, this routine presents the operator with a flexible method of debugging any software modification. In fact, the entire panel program can be rewritten under the direction of the single-step routine.

Conclusion

The system described above represents a flexible method of implementing a data display and is superior to pure hardware implementation. The I/O and interrupt features of the Z-80 allow substantial operator control and interaction and, by adding a few more PIO chips, the operator control features can be vastly expanded. Changes can be implemented with minimal effort and easily written software can take the place of complicated hardware to perform complex interpretive functions. In addition, system reliability is greatly improved if the ratio of software, on which reliable system operation is contingent, is increased with respect to the hardware.

Acknowledgments

The authors wish to thank several people who contributed to the design, development and successful completion of this project. D.K. Guhn wrote the initial specification and developed the overall system design. D. Costello, and R. St. John made several helpful suggestions during the course of the project.

Robert Paglee and members of his group perform radar signal processing and command and control design functions. He was initially employed by RCA as an engineer in 1944, and has remained continuously with the company since that time. His background covers a wide variety of electronic equipment, including radar, sonar, radio and TV broadcasting equipment, computers and communications systems.

He has participated in the design of many types of instrumentation radars, including AN/FPS-16, AN/FPQ-6, AN/TPQ-18, AN/MPS-36, and DIR. He has also contributed to AN/FPS-95, AN/SPY-1, AN/TPQ-27 PTR and other radar designs.

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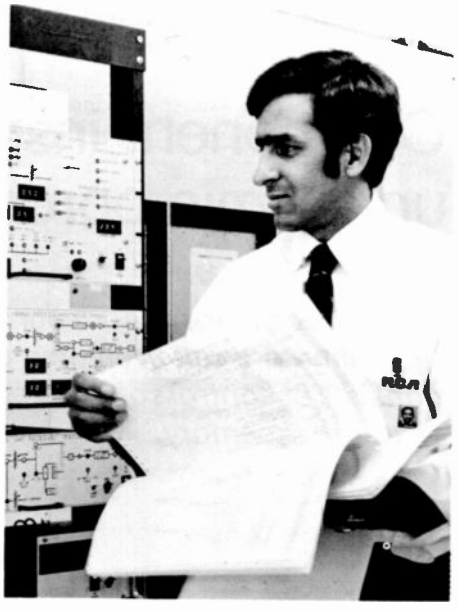

Vivek Ragavan joined RCA in June, 1978, and was involved in digital logic design projects, including redesign of portions of the L-Band Data Recording System for Tradex, development of a digitally-controlled audiovisual "diorama" to display the capabilities of the AN/SPY-1 radar, and the assignment described in this article. He has recently left the company.

A.R. Marcantonio|M.J. Cherbak

Component inspection system under microprocessor control

Microprocessor-based testing of incoming parts offers the flexibility of a relatively low cost firmware design that consists of control software and component specifications in read-only memory.

Abstract: *An inspection system is presented that automatically verifies all essential potentiometer characteristics. Control software and characteristic data are partitioned into separate EPROMS facilitating limit changes. System hardware includes a two-board microcomputer, a versatile control panel, and a custom test fixture driven by a stepping motor. Operating modes are: 'go/no go' for production testing and a 'characteristic trace' mode, which provides an oscilloscope display of the potentiometer response, for engineering analysis. Initial results indicate that the system is quite effective in identifying potentiometer defects including non-monotonic or discontinuous taper.*

Microprocessors (μPs) permit the implementation of test and control systems that would not be cost-effective, if more powerful central processing units (CPUs) were used. Offering the flexibility of a firmware-based design at relatively low cost, μP-controlled testers are finding their way into an ever-increasing applications base.[1,2] The system described here is an example of μP-based testing applied to the high volume manufacturing of electronic products. Microprocessors are excellent control candidates for systems such as the one presented here where speed and computation requirements are not critical, and low overall cost enables dedication to a specific function.

Background

Competition for market-share in electronic consumer products has grown more intense in recent years. Ideally, consumer product manufacturers would each like to make a component that costs less and contains fewer defective parts than their competitors' product. Unfortunately, low cost together with a total absence of defective parts is not always easily obtained in the same package and some tradeoffs are involved. One such tradeoff applies to the balance between the degree of testing a product receives, and the product's cost. A thoroughly tested product, other factors being equal, will generally perform better and cost more. So the question is, how much testing is cost effective?

In the device testing area, passive components typically have a failure rate much lower than active ones. This in itself is not justification for assembling them into systems without adequate testing, since the cost of identification and replacement of defective components increases ten-fold between each level of the product cycle,[3] as shown in the graph of Fig. 1.

This relationship alone, between cost and repair point, would seem to justify the economics of incoming inspection of all components, including those with low failure rates. In addition, many automatic test equipment manufacturers recommend 100 percent component testing for assemblies run through their equipment.

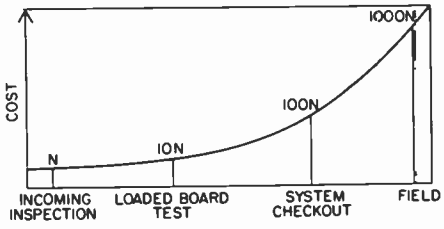

Fig. 1. Relative costs to find and replace a defective component at various levels in the product cycle.

Some of the more obvious reasons for 100 percent testing of all incoming parts are as follows:

1. The least costly place to catch defects is on incoming inspection, before assembly (note Fig. 1 curve).
2. The total number of rejects in the finished product is at least as great as the sum of the individual rejects. For example, let's assume we have 700 components on the TV chassis board, and the average reject rate is 0.2 percent. Then the finished receiver will contain, at least for this oversimplified example, 1.4 rejects average/set.
3. Automated lines are not equipped to buffer a high number of rejects; they become very inefficient.
4. If a defective component fails in the finished product, under power, there is a reasonable possibility that it will cause other components to fail as well.
5. Field failures are not only extremely costly, they serve to reduce the perceived quality of our product, in the eyes of the customer.

The inspection system described moves RCA closer to a posture of completely effective testing by providing the capability to 100 percent test potentiometers, prior to their assembly into the television receiver.

System overview

The tester, shown in Fig. 2, was developed to perform incoming-parts inspection on

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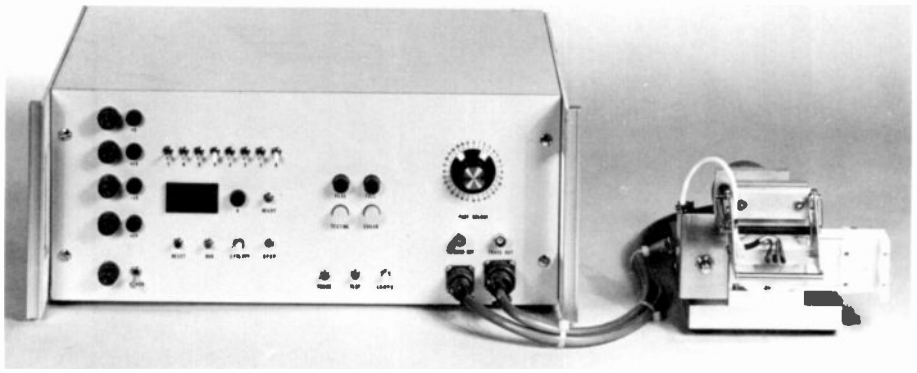

Fig. 2. The incoming-parts testing for potentiometers is accomplished with this tester which consists of a 7" x 19¼" chassis, that contains all the system electronics and a control panel, and that interconnects to a small assembly supporting the stepping motor, clutch and potentiometer chuck.

potentiometers. As mentioned above, passive components typically have low reject rates, but incoming inspection is still warranted when overall volume is high.[3]

The system is based on the RCA COSMAC Evaluation board[4] with control program and potentiometer characteristics stored in erasable programmable read-only memory (EPROM). The potentiometer's setting is manipulated by a stepping motor under CPU control. A mechanical clutch in series with the stepper's drive train is adjusted to slip, and thereby fail defective potentiometers requiring excessive turning torque. The control program operates on a sixteen-byte parameter field, known as the characteristic, which uniquely defines the part being tested. Verified parameters include: residual and maximum resistance, monotonicity, taper, torque, and angle of rotation.

Operation

In order to inspect a component, the operator places the component in the test fixture, swings the contact block into place, and pushes the test button. The control program directs the stepper to peg the potentiometer shaft to the counter-clockwise stop. Residual resistance is measured and verified. The potentiometer is then stepped through its rotation by the program, while its taper is checked. The resistance plot must be monotonic and of the correct slope. When the clockwise stop is reached, maximum resistance is measured and verified, and rotational limits checked. If any of the tests fail, the testing sequence is terminated and a fail lamp is turned on. If no tests fail, at the end of the testing sequence, a pass lamp is turned on. If the potentiometer fails, a trace mode may be executed which displays the parts' responses on an oscilloscope for further analysis.

Hardware system

A block diagram of the hardware system is presented in Fig. 3. Attributes of the hardware are summarized as follows:

Physical Appearance:

- A 7- x 19¼-inch chassis, containing all the system electronics and a control panel, is electrically interconnected to a small assembly supporting the stepping motor, clutch, and potentiometer chuck (Fig. 2).

Electrical Components:

- The enhanced RCA COSMAC evaluation board is capable of addressing 4-k bytes of memory (switchable in 1-k byte increments to EPROM or RAM), and contains a 1.5-MHz system clock, a buffered address bus, a power on reset-run, and regulators for −5 Vdc and +12 Vdc.
- The input/output board contains a relay matrix for closing sense resistor paths and selecting potentiometer terminals, a buffered 8-bit, 0−10-Vdc A/D converter, a buffered 8-bit, 0 −10-Vdc D/A converter, a precision 10-Vdc, 1-amp power supply with foldback current limiting, and necessary front panel control logic and I/O ports.
- The unipolar stepper drive interface consists of transistor motor drivers, and sequencing and direction logic.
- The control panel contains switches for system power, reset, run program, start test and potentiometer selection, and indicator lamps for logic supplies and test status.
- The stepping motor, operated at 24 Vdc, is capable of 400 steps/second, 30-ounce inches of torque, and a step-angle resolution of 1.8 degrees.

Software system

The system control program is implemented in COSMAC level I assembly language. It includes subroutines for time delay and stepping-motor positioning, and occupies about 75 percent of a 1-k byte EPROM chip.

A memory map is presented in Fig. 4. Two micropages, starting at 0800 hex, are reserved for characteristic field storage.

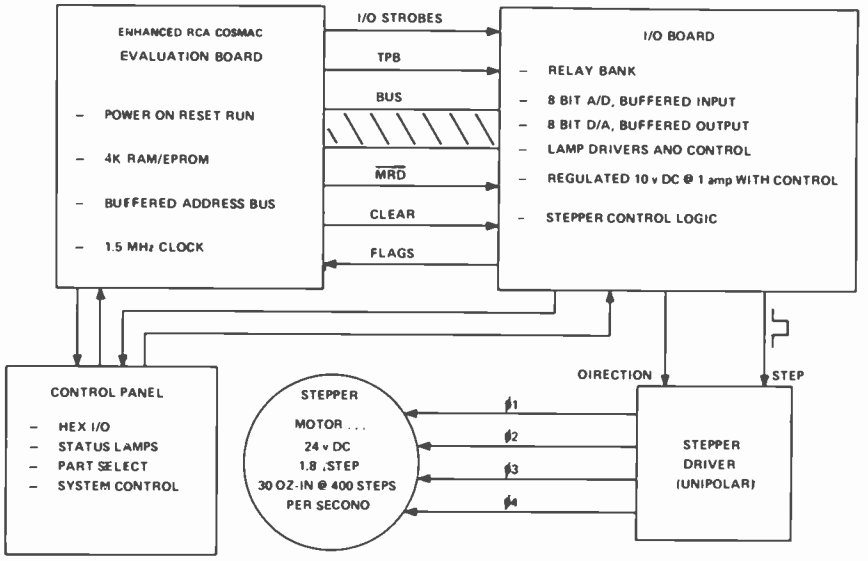

Fig. 3. The block diagram of the hardware system shows an RCA COSMAC evaluation board capable of addressing 4-k bytes of memory.

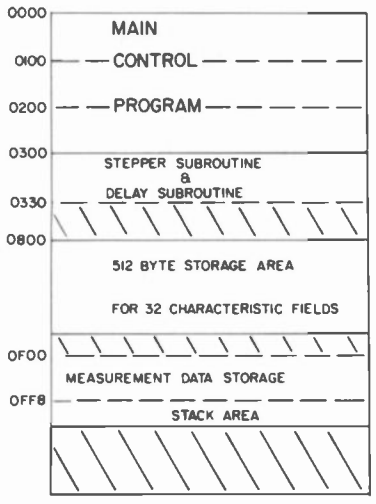

Fig. 4. Two micropages, starting at 0800 hex, will accommodate specifications for thirty-two different potentiometers. A single page of memory, starting at 0F00 hex, is used for potentiometer measurements and stack storage.

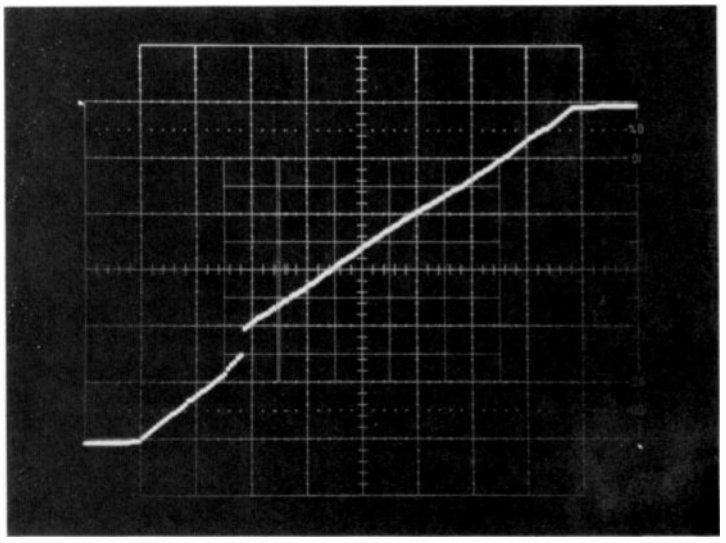

Fig. 5. Using the 'characteristic trace' mode, this response trace of a defective linear-taper potentiometer, with discontinuity in slope, was obtained.

This area will accommodate specifications for thirty-two different potentiometers. The control program is directed to a specific field by using the part select value, read from the front panel, as a vector into this 512-byte table. A single page of memory, starting at 0F00 hex, is used for potentiometer measurements and stack storage.

Measurements

In 'production test' mode, measurements are made by sensing the voltage drop across a known resistor in series with the potentiometer under test. The circuit is effected by using one relay of the I/O board matrix and a sense resistor, with one or more of the four control relays to form a measurement loop. The precision 10-Vdc supply (software controlled) provides the stimulus, and the response is measured with an eight-bit A/D converter.

In the 'characteristic trace' mode, an eight-bit D/A converter refreshes a scope display using previously stored analog data and a short output routine. All measurement data is written to RAM where it can be recalled for further analysis at the completion of the test. Figure 5 contains a reproduction of a scope photo obtained using the 'characteristic trace' mode. The response trace is of a linear-taper potentiometer that has a discontinuous slope.

Characteristic

Before a potentiometer can be inspected, the control program must have access to its specifications. This is effected through the use of a sixteen-byte parameter field known as the characteristic. Its format is detailed in Fig. 6. This field uniquely defines the part being tested, in terms of residual and maximum resistance, taper and rotational limits; and covers both linear and nonlinear tapers. It places all the specifications for a part in one location thereby facilitating implementation of the characteristic and enabling all characteristic fields to be partitioned into a separate memory area from the system control program.

This feature is essential since it allows potentiometer specifications to be added or changed easily. The characteristic enables the potentiometers' resistance plots to be profiled by four separate regions, each with a different resolution and slope (Fig. 7). An examination of the two bytes, comprising each profile region field, is as follows.

The first character of each of the profile-region fields dictates the number of 1.8° steps to be taken before a slope measurement is made. The second character is the maximum slope allowed for the given step increment. The last two characters define the end count in 1.8° steps, for that profile region.

As seen in the example, shown in Fig. 7, the steps/move are two dictating (2 x 1.8°) per increment or 3.6°. The maximum slope allowed is 5. That means the change in resistance for a 3.6° increment should not exceed 5/256 or approximately two percent of the total resistance. The end count (4E hex) defines the end of region #N to be 140° into the potentiometer's rotation. The byte assignments for the individual characteristic fields are presented in Table I.

Conclusion

Inspection of incoming parts is justifiable on the basis of being the most cost-effective way of screening out reject parts, and it is essential for high-volume manufacturing.

Microprocessor-based testing of incoming parts offers the flexibility of firmware design at a relatively low cost. The tester described here enables simple

Table I. Characteristic-field byte assignments.

Byte #	*Assignment*
0:	Part type, 00 = single, 10 = double.
1:	Matrix address of residual sense resistor.
2:	Upper residual limit.
3:	Steps/move and maximum slope allowed, region #1.
4:	End-count region #1 (1.8-degree steps).
5:	Steps/move and maximum slope allowed, region #2.
6:	End-count region #2 (1.8-degree steps).
7:	Steps/move and maximum slope allowed, region #3.
8:	End-count region #3 (1.8-degree steps).
9:	Steps/move and maximum slope allowed, region #4.
A:	End-count region #4 (1.8-degree steps).
B:	Matrix address of maximum sense resistor.
C:	Upper limit on maximum resistance.
D:	Lower limit on maximum resistance.
E:	Upper limit of rotational angle (1.8-degree steps).
F:	Lower limit of rotational angle (1.8-degree steps).

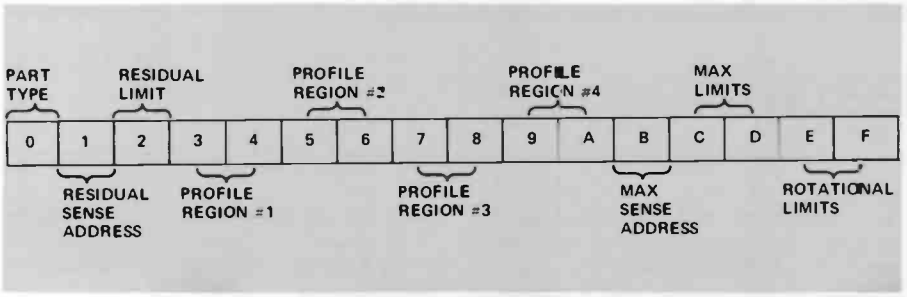

Fig. 6. The control program has access to the potentiometer specifications through a sixteen-byte parameter field known as the characteristic.

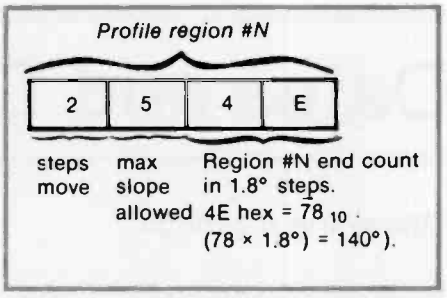

Fig. 7. Example of a profile region segment of a characteristic field.

part specification changes by utilizing separate EPROMS for program and limits. A key system concept is the interpretive approach to user programming. This method, successfully employed in an earlier μP-based tester,[1] enables a complex test system to be programmed by a relatively unsophisticated user. In the present system, user programming of part specifications is effected through the use of the characteristic field.

Acknowledgment

The authors are grateful to A. Abramovich, J.G. Aceti, H.D. Hanson, and T.F. Lenihan of RCA, whose efforts helped make this system possible. Thanks are also due to K. Bernardo, R. DeStephanis, J. Egan, S. Noto, R.S. Schmidt, and W. Feick for excellent system implementation and documentation, and outstanding fixture design and development.

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1. Marcantonio, A.R., "Microprocessor-Based Printed Circuit Board Tester," *Proceedings of IECI '78*, Philadelphia, Pa. (March, 1978).
2. Marcantonio, A.R., "Microcomputer-Controlled Potentiometer Test System," *Proceedings of IECI '79*, Philadelphia, Pa. (March, 1979).
3. Yates, W., "Passive Component Testing," *Electronic Products* (Sept., 1978).
4. Evaluation Kit Manual for the RCA COSMAC Microprocessor, MPM-203, RCA Solid State Division, Somerville, N.J.

Mike Cherbak is shown, on left, discussing a computer printout with Angelo Marcantonio.

Angelo Marcantonio has been involved in research on computer hardware and software systems since he joined RCA Laboratories in 1970. As a member of the original microprocessor team, he designed and programmed interpretive languages and applications software. He is presently a member of the Microsystems Research Group where he is engaged in the design of automated test and control systems for manufacturing, the development of test strategies and methodology applicable to complex consumer products, and research in manufacturing automation and industrial robotics.

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Mike Cherbak is a Component Test Design Engineer, currently responsible for electrical testing of purchased components and light sub-assemblies at the RCA Bloomington Consumer Electronics plant. His duties include both hardware and software design and back-up support for sophisticated component test systems.

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Dates and Deadlines

Upcoming meetings

Ed. Note: Meetings are listed chronologically. Listed after the meeting title (in bold type) are the sponsor(s), the location, and the person to contact for more information.

FEB 13-15, 1980—**Intl. Solid State Circuits Conference** (SSC, San Francisco Sec.) Hilton Hotel, San Francisco, CA **Prog Info:** Lewis Winner, 301 Almeria Ave., Coral Gables, FL 33134 (305-446-8193)

FEB 25-28, 1980—**COMPCON Spring '80** (C) Jack Tar Hotel, San Francisco, CA **Prog Info:** Harry Hayman, P.O. Box 639, Silver Spring, MD 20901 (301-439-7007)

FEB 26-28, 1980—**Laser and Electro-Optical Systems/Inertial Confinement Fusion** (QEA, OSA) Town & Country Hotel, San Diego, CA **Prog Info:** Joan Connor, Optical Society of America, 2000 L Street N.W. (Suite 620), Washington, DC 20036 (202-293-1420)

MAR 3-5, 1980—**NCC Office Automation Congress** (C) **Prog Info:** Harry Hayman, P.O. Box 639, Silver Spring, MD 20901 (301-439-7007)

MAR 4-6, 1980—**International Zurich Seminar on Digital Communications** (Switzerland Sec. COM (Cooperating)) Swiss Federal Institute of Tech. on Digital Communications, Zurich, Switzerland **Prog Info:** Prof. P.E. Leuthold, Eidgenossische Technische Hochschule Zurich Institut Fur Hochfrequenztechnik, Sternwartstrasse 7, Zurich, Switzerland (Tele.: T41-1-326211)

MAR 11-14, 1980—**Computer Architecture for Non-numeric Processing 5th Workshop** (C) Pacific Grove, CA **Prog Info:** Harry Hayman, P.O. Box 639, Silver Spring, MD 20901 (301-439-7007)

MAR 16-18, 1980—**Particle Accelerator Conference** (NPS) **Prog Info:** Dr. Louis Castrell, NPS Meetings Coordinator, National Bureau of Standards, C333 Radiation Physics, Washington, DC 20234

MAR 17-20, 1980—**Industrial Control & Instrumentation Applications of Mini & Microcomputers** (IECI) Sponsors: IECI, Sheraton Hotel, JFK Blvd., Phila., PA **Prog Info:** Patrick P. Fasang, RCA Corp., Route 38, Cherry Hill, NJ 08358 (609-338-5020)

MAR 24-25, 1980—**Radio Transmitters and Modulation Techniques** (IEE, IERE) IEE, Savoy Place, London, WC2 **Prog Info:** Conference Dept., IEE, Savoy Place, London WC2R OBL, England

MAR 24-27, 1980—**Magnetic Fluids 2nd Intl. Conf.** (MAG) Marriott Inn, Orlando, FL **Prog Info:** Markus Zahn, Dept of EE, Univ. of Florida, Gainesville, FL 32611 (904-392-4964 Ofc., 904-392-4960 Sect.)

APR 7-11, 1980—**Optical Computing Int'l. Conference** (C) Hyatt Regency, Washington, DC **Prog Info:** Sam Horvitz, P.O. Box 274, Waterford, CT 06385 (Office: 203-447-4270, Home: 203-442-0829)

APR 8-10, 1980—**Reliability Physics Symposium** (R, ED) Caesar's Palace, Las Vegas, NV **Prog Info:** Glen T. Cheney, Bell Laboratories, 555 Union Blvd., Allentown, PA 18103 (215-439-7628)

APR 9-11, 1980—**Intl. Conf. on Acoustics, Speech and Signal Processing** (ASSP, IEEE), Fairmount Hotel, Denver, CO **Prog Info:** J. Robert Ashley, Univ. of Colorado, Coll. of Engr. & Appl. Sci., Dept. of Elec. & Comp. Engr., 1100 14th Street, Denver, CO 80202 (303-629-2554 or 2872)

APR 13-16, 1980—**Southeastcon '80,** Opryland Hotel, Nashville, TN **Prog Info:** Larry K. Wilson, Box 1687, Station B, Nashville, TN 37235 (615) 322-2771)

APR 21-23, 1980—**American Power Conference** Ill. Inst. Tech., PES & 8 other engr. societies, Palmer House, Chicago, IL **Prog Info:** R.A. Budenholzer, 246 E-1, IIT, Chicago, IL 60616 (312-567-3196)

APR 21-24, 1980—**Intl Magnetics Conf.** (INTERMAG) (MAG), Boston Sheraton Hotel, Boston, MA **Prog Info:** D.I. Gordon, Naval Surface Weapons Center, White Oak Lab., Silver Spring, MD 20910 (202-394-2167)

APR 28-30, 1980—**Internation Radar Conference** (IEEE, AES, IEEE Wash. section), Stouffer's National Center Hotel, Arlington, VA **Prog Info:** R.T. Hill/J. Kalitta, c/o Conference Office, 777 14th St., NW Suite 917, Washington, DC 20005 (202-637-4217)

APR 28-30, 1980—**30th Electronic Components Conference** (CHMT, EIA) Hyatt Regency San Francisco, San Francisco, CA **Prog Info:** Dr. H.J. Gisler, Electro Scientific Industries, 13900 N.W. Science Park Dr., Portland, OR 97229 (503-641-4141)

APR 28-30, 1980—**Circuits and Systems Int'l. Symposium** (CAS) Shamrock Hilton Hotel, Houston, TX **Prog Info:** Prof. R.J.P. DeFigueiredo, General Chairman, Dept. of Electrical Engineering, Rice University, P.O. Box 1892, Houston, TX 77001 (713-527-8101, ext. 3568)

May 5-11, 1980—**Global Technology 2000** (AIAA) Baltimore Convention Center Baltimore, MD **Prog Info:** American Institute of Aeronautics and Astronautics, 1290 Ave. of the Americas, New York, NY 10019 (212) 581-4300

MAY 12-15, 1980—**Industrial and Commercial Power Systems Conference** (IA, IEEE, Houston Section), Stouffer's Greenway Plaza, Houston, TX **Prog Info:** Baldwin Bridger, Powell Elect. Mfg. Co., P.O. Box 12818, Houston, TX 77017 (713-944-6900)

MAY 13-15, 1980—**Electro** (IEEE sponsors) Reg 1, New Eng. Council, METSAC, (ERA, New Eng. & N.Y. chapters), Boston-Sheraton Hynes Auditorium, Boston, MA **Prog Info:** Dale Litherland, Electronic Conventions, Inc., 999 N. Sepulveda Blvd., El Segundo, CA 90245 (213-772-2965)

MAY 19-20, 1980—**Southeast Symp. on System Theory** (C), Old Dominion University, Cavalier Hotel, Virginia Beach, VA **Prog Info:** Harry Hayman, P.O. Box 639, Silver Spring, MD 20901 (301-439-7007)

MAY 28-30, 1980—**Intl. Microwave Symp.** (MTT) Shoreham Americana Hotel, Washington, D.C. **Prog. Info:** Lawrence R. Whicker, Naval Research Lab Code 5250, Washington, DC 20375 (202-767-3312)

JUNE 8-11, 1980—**Intl. Conference on Communications,** Red Lion Inn, Seattle, WA **Prog Info:** W.W. Keltner, Room 1402, 1600 Bell Plaza, Seattle, WA 98191 (206-345-3999) & (206-655-3601)

June 9-11, 1980—**Int'l. Symposium on Electrical Insulation** (IEEE) (EI) 57 Park Plaza Hotel, Boston, MA **Prog Info:** Dr. H. St. Onge, IREQ-Hydro Quebec Institute of Research, P.O. Box 1000, Varennes, PQ, Canada, JOL 2 PO (514-652-8420)

JUNE 10-12, 1980—**Development in Power-System Protection, 2nd International Conference** (IEEE UKRI SEC., IEE, IMA) IEEE, Savoy Place, London WC2 **Prog Info:** Conference Dept., IEE Savoy Place, London WC2R OBL, England

JUNE 23-27, 1980—**Conference on Precision Electro-Magnetic Measurements (CPEM)** (IEEE Sponsors: IM; other sponsors: NBS, URSI/USNC) Stadthalle, City of Braunschweig, Fed. Rep. Germany **Prog Info:** Prof. Horst Captuller, Physikalisch Technische, Bundesanstalt, Bundsealle-100, D-3300 Braunschweig, Fed. Rep. Germany

JULY 15-18, 1980—**Nuclear and Space Radiation Effects Conference** (IEEE sponsors: NPS, other sponsors: DNA, JPL)Cornell University, Ithaca, NY **Prog Info:** Harold L. Flescher, Raytheon Com-

pany, 528 Boston Post Rd., Mailstop 1K5, Sudbury, MA 01776 (617) 443-9521, (ext. 3057)

AUG 13-15, 1980—**Joint Automatic Control Conference** (IEEE sponsors: CS, other sponsors: ASME, AIAA, ISA) Sheraton Palace, San Francisco, CA **Prog Info:** Prof. David Hullender, Dept. of Mechanical Engineering, University of Texas, Arlington, TX 76010 (817) 273-2561

Pen and Podium

Recent RCA technical papers and presentations

To obtain copies of papers, check your library or contact the author or his divisional Technical Publications Administrator (listed on back cover) for a reprint.

Astro-Electronics

A. Aukstikalnis|G. Beck
R. Buntschuh
Adaptable spacecraft computer experience—AIAA/IEEE/ACM/NASA Computers in Aerospace Conf. II, Hyatt House Hotel, Los Angeles, CA (10/22/79)

S. Gaston
RCA Satcom Ni-Cd batteries operational results—NASA/GSFC Battery Workshop, Greenbelt, MD (11/14/79)

L. Gomberg|R. Te Beest|Lt. Col. McElroy
DMSP Block 5D-1 computer controlled spacecraft—Int'l. Telemetering Conf., San Diego, CA (11/19/79)

R. Hoedemaker|C. Staloff
A compatible STS/PA - D/RCA Satcom Telemetry & Command System—Int'l. Telemetering Conf., San Diego, CA (11/19/79)

Automated Systems

M.J. Cantella
Image pattern signal to noise analysis for focal plane sensors—IRIS Specialty Group on Infrared Imaging, Dallas, TX (11/79)

B.R. Clay
Application areas — two dimensional displays—Chapter X *Handbook of Optical Holography*, Academic Press (11/79)

W.X. Johnson
Advanced Autonomous Array (U)—Second Combat Systems Symposium, Annapolis, MD (10/17/79)

N.L. Laschever
The case for alternate fuels—Ediorial for the *IEEE Reflector* (11/79)

J.P. Mergler
C³I Command Language—Military Electronics Defence Expo '79, Anaheim, CA (10/24/79)

E.H. Miller
ASAS, All Source Analysis System/TCAC, Technical Control & Analysis Centers (U)—EASCON '79, Arlington, VA (10/10/79)

Advanced Technology Laboratories

A. Feller|M. Stebnisky
Scaled and unscaled 3 - 4 micron versions of a 5 - 6.35 micron CMOS/SOS test chip—SOS Workshop, Carefree, AZ (10/4-6/79)

D.A. Gandolfo|J.R. Tower|L.D. Elliott
D.M. McCarthy|F.V. Shallcross, RCAL
S.C. Munroe, MIT
A 512-stage analog-binary programmable transversal filter—5th Int'l. Conf. on Charge-Coupled Devices, Edinburgh, UK, *Proceedings* (9/12-14/79)

D.A. Gandolfo|J.R. Tower|L.D. Elliott
E.J. Nossen, GCS|L.W. Martinson, MSR
CCDs for Spread Spectrum Applications—3rd Int'l. Specialist Seminar on "Signal Processing", Hydro, England, *Proceedings* (9/18-21/79)

Government Communications Systems

R.W. Allen
MD-945/TSC digital data modem for SHF Satellite Communications Systems—NTC, Washington, DC, *Proceedings* (11/27/79)

H. Barton, Jr.
Cost tracking model with learning curve extension—EIA G-47 Comm. Mtg., Washington, DC (11/27/79)

W. Blackman
In search of a solution—Elec. Conn. Conf., *Packaging RCA* (10/79)

E.J. Nossen|V.F. Volertas
Unidirectional phase shift keying—NTC, Washington, DC, *Proceedings* (11/29/79)

J. Rothweiler|J. Bradshaw|N. Macina
Investigation of CCD application to multi channel receiver design—NTC, Washington, DC, *Proceedings* (11/27/79)

D.M. Ward
Minority electrical engineers in the electronics industry—*Conf. Record*, Eng. Mgmt. Society of IEEE, Arlington, VA (11/5-6/79)

Laboratories

C.R. Carlson|R.W. Cohen
Power spectral densities for pictorial scenes: edges and $1/f^2$ spectra —Annual Meeting of the Optical Society of America, Rochester, NY; Abstract in *TOSA*, Vol. 69, No. 10, p. 1450 (10/79)

M. Caulton|W.L. Sked|F.S. Wozniak
The adherence of chromium and titanium films deposited on alumina, quartz, and glass—testing and improvement of electron-beam-deposition techniques, *RCA Review*, Vol. 40 (6/79)

L.S. Cosentino|V. Christiano|J.G. Endriz
G.F. Stockdale|J.L. Cooper J.N. Hewitt
J.B. Harrison, Jr.
Feedback multiplier flat-panel television: II-technologies—*IEEE Transactions on Electron Devices*, Vol. ED-26, No. 9 (9/79)

D.A. DeWolf
Focusing and deflection of electron beams produced by feedback multipliers in a flat TV display—*IEEE Transactions on Electron Devices*, Vol. ED-26, No. 9 (9/79)

J. Dresner
Feedback multiplier flat-panel television: III—ion bombardment, dynode life, and ambient pressure—*IEEE Transactions on Electron Devices*, Vol. ED-26, No. 9 (9/79)

R.S. Engelbrecht
The effect of rain on satellite communications—*RCA Review*, Vol. 40 (6/79)

M. Ettenberg|D.R. Patterson
E.J. Denlinger
A temperature-compensated laser module

for optical communications—*RCA Review*, Vol. 40 (6/79)

K.G. Hernqvist
Approaches to a practical hollow cathode laser—International Conf. on Lasers '79, Orlando, FL (12/17-21/79)

M.L. Hitchman
Proton diffusion in hydrogen tungsten bronzes—*Thin Solid Films*, 61 pp. 341-348 (1979)

M. Inoue
A model for the acceptor state in II-VI compounds—*J. Phys. Chem. Solids*, Vol. 40, pp. 857-862 (1979)

L.B. Johnston
Feedback multiplier flat-panel television: IV—anode sensing—*IEEE Trans. on Electron Devices*, Vol. ED-26, No. 9 (9/79)

M. Kaplan|D. Meyerhofer
Response of diazoquinone resists to optical and electron-beam exposure—*RCA Review*, Vol. 40, No. 2 (6/79)

A.R. Moore
An optimized grid design for a sun-concentrator solar cell—*RCA Review*, Vol. 40, No. 2 (6/79)

A.R. Moore
Optimum grid design for a nonuniformly illuminated sun-concentrator solar cell—*RCA Review*, Vol. 40 (6/79)

J.H. Thomas III|A.M. Goodman
AES and XPS studies of semi-insulating polycrystalline silicon (SIPOS) layers—*J. of the Electrochemical Society*, Vol. 126, No. 10 (10/79)

M. Toda
High field dielectric loss of PVF_2 and the electromechanical conversion efficiency of a PVF_2 fan—*Ferroelectrics*, Vol. 22, pp. 919-923 (1979)

M. Toda
Theory of air flow generation by a resonant type PVF_2 bimorph cantilever vibrator—*Ferroelectrics*, Vol. 22, pp 911-918 (1979)

M. Toda|S. Osaka
Vibrational fan using the piezoelectric polymer PVF_2—*Proc. of the IEEE*, Vol. 67, No. 8 (8/79)

Missile and Surface Radar

F.J. Buckley
Software quality assurance—Two-day Continuing Professional Education Seminar (sponsored by Drexel Univ.), Washington, DC (11/14-15/79)

J.E. Friedman|J. Haness
Documentation—the hidden cost of management—IEEE Engineering Management Conf., Arlington, VA (11/5-7/79)

L.W. Martinson, et al.
CCDs for spread spectrum applications—3rd Int'l. Specialist Seminar on "Signal Processing," Peebles Hotel, Hydor, England (9/18-21/79)

M.I. Rozansky
Doppler servo tracker with frequency synthesizer feedback—*RCA Review*, Vol. 40 (6/79)

R.L. Schelhorn
A universal probing technique for continuity and isolation—1979 Int'l. Microelectronics Symposium, Los Angeles, CA (11/13-15/79)

A. Schwarzmann
Printed transmission lines—Phila. Chapter IEEE Mtg. (11/27/79)

H. Urkowitz
Models for radar design and evaluation—USAF Warning Information Correlation (WIC) Program, meeting of WIC Threat Working Group, Arlington, VA (10/30 - 11/1/79)

RCA Records

J. Freeman|G. Teague
Computerized multiattribute labor control system for warehousing—AIIE Region VIII Conf., Indianapolis, IN (10/28/79)

R. Wartzok
A programmable controller application in injection molding machines—RCA MEPS Conf., Indianapolis, IN (11/13/79)

Patents

Automated Systems

Arntsen, A.P.
Coupling a frequency modulated signal to a tuned load—4173743

Commercial Communications Systems

Dischert, R.A.
Television control system—4170024

Consumer Electronics

Lagoni, W.A.|Webb, J.B.
Burst gate circuit—4173023

Lehmann, W.L.
Antenna isolation device—4173742

Laboratories

Babcock, W.E.|Hess, R.L.
Television S-correction linearity device—4176303

Comizzoli, R.B.
Chemically treating the overcoat of a semiconductor device—4173683

Credelle, T.L.|Spong, F.W.
Recording a synthetic focused-image hologram on a thermally deformable plastic—4174881

Denlinger, E.J.|Veloric, H.S.
Contact for semiconductor devices—4173768

Dholakia, A.R.
Grooved record playback system—4173348

Fecht, H.R.
Raster distortion correction circuit—4169988

Flatley, D.W.
Method for making semiconductor structure—4174217

Ipri, A.C.|Scott, J.H., Jr.
Method for making silicon on sapphire transistor utilizing predeposition of leads—4169746

Jebens, R.W.
Method of fabrication of a fresnel lens—4170616

Kressel, H.|Spak, M.A.
Method of defining contact openings in insulating layers on semiconductor devices without the formation of undesirable pinholes—4174252

Marlowe, F.J.
Multiple standard television sync generator—4169659

Marlowe, F.J.|Anderson, C.H.
Flat display device—4174523

McCarthy, D.C.|Rayl, M.
Printed circuit board with increased arc track resistance—4174531

Scott, H.M.
Regulating television horizontal deflection arrangement—4176304

Toda, M.|Matsumoto, Y.|Osaka, S.
Signal pickup arm lifting/lowering and groove skipper apparatus—4176376

Missile and Surface Radar

Bowman, D.F.
Frequency-scanned antenna—4170778 (assigned to U.S. government)

Picture Tube Division

Stone, R.P.|Morrell, A.M.
Cathode-ray tube having a stepped shadow mask—4173729

Turnbull, J.C.
Method for coating cathode material on cathode substrate—4170811

SelectaVision

Huff, L.D.
Toggle mechanism for video disc player—4175751

Solid State Division

Dingwall, A.G.
Integrated gate field effect transistors having closed gate structure with controlled avalanche characteristics—4173022

Harford, J.R.
Signal attenuator—4172239

Khajezadeh, H.
Method of making a semiconductor integrated circuit device utilizing simultaneous outdiffusion and autodoping during epitaxial deposition—4170501

Leidich, A.J.
Self-biasing amplifier stage—4172999

Zuber, J.R.
Novel solvent drying agent—4169807

Engineering News and Highlights

Valente elected President of RCA

Maurice R. Valente, has been elected President, Chief Operating Officer, and a Director of RCA Corporation, effective January 1, 1980. He was formerly Executive Vice President, International Telephone and Telegraph Corporation.

Mr. Valente, 50, has held a number of high-level executive assignments at ITT, both here and abroad, since joining the company in 1965, rising to his current position of Executive Vice President, and a member of the Office of the Chief Executive, with responsibility for the Consumer Products and Services Group. Previously he had spent six years in an executive capacity with the Crane Company and, prior to that, four years with Motorola, Inc.

In his new post, Mr. Valente will have day-to-day responsibility for all of RCA's major operating units with the exception of The Hertz Corporation and the National Broadcasting Company, which at this time will continue to report directly to Mr. Griffiths.

Mr. Valente joined ITT in 1965 as Staff Assistant, Executive Vice President, Industrial Products Group, rising through the executive ranks where he became Director of Staff Operations, North America in 1969. In 1970, he was named Vice President, Group Executive, Defense Group; in 1972, Senior Vice President, Director Operations, Staff Worldwide; and from 1974 to 1979 was Executive Vice President and President, ITT Europe, Africa, and the Middle East.

Griffiths named Chairman of the Board

Edgar H. Griffiths, who has been President since September, 1976, has been named Chairman of the Board, effective January 1, and continues as Chief Executive Officer. Mr. Griffiths, who has been with RCA since 1948, will be only the sixth Chairman in RCA's history. He has been a member of the Board of Directors since 1972.

Mr. Griffiths joined RCA at the RCA Camden facility in 1948. A year later he transferred to the RCA Service Company. He was named Treasurer and Controller of the Service Company in 1957, a position he held until 1963. In April 1963, Mr. Griffiths was appointed Division Vice President, International Finance for the RCA International Division. Three years later, he was named Division Vice President, Commercial Services, for the RCA Service Company.

Mr. Griffiths was appointed President of the RCA Service Company in 1968 and held that position until June 1971, when he was elected an Executive Vice President, Services. Subsequently, Mr. Griffiths was made responsible for all of RCA's Electronics and Diversified Businesses which constituted two of the three major business groups of the Company.

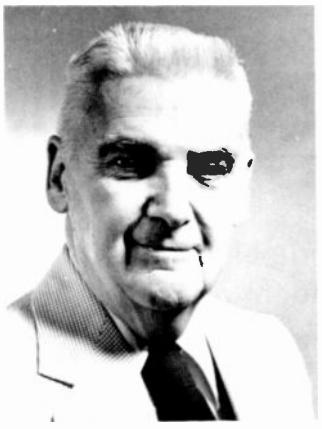
Mr. Griffiths is a member of The Business Roundtable, The Conference Board and the Emergency Committee for American Trade.

Matulis named Chief Engineer of MSR

The appointment of **Bernard J. Matulis** as Chief Engineer at Missile and Surface Radar was announced by **William V. Goodwin,** Division Vice President and General Manager. In his new post, Mr. Matulis is responsible for all engineering activities, including the development of advanced techniques needed for future government electronic defense systems. He succeeds **Joseph C Volpe,** who was recently promoted to Director, Product Operations.

Mr. Matulis has held various managerial and design engineering positions at RCA since joining the company in 1956. Most recently, he managed the integration of hardware subsystems and computer programs into final, tested radar systems.

Moore is new TPA for GSD Staff



Edwin E. Moore joined RCA in an industrial engineering capacity in 1942. He transferred in 1947 to the engineering department of the Component Parts organization. He continued in Component Engineering Administration and Services until 1959. Transferring to Cherry Hill, he was Manager of engineering services for the Home Instruments Division until they relocated to Indianapolis. In 1962, he joined the Surface Communications Division of what is now Government Systems and held various posts there until 1970 when he became a part of the GSD staff engineering group. Contact him at Government Systems Division, Cherry Hill, N.J., ext. 5833.

Grosh is new Ed Rep for Solid State Division

John Grosh was recently appointed Editorial Representative for Solid State Division, Electro-Optics and Devices, at Lancaster. He succeeds Ralph Engstrom, who is retiring. Mr. Grosh has been with RCA since 1953. He is Technical Staff Leader of the Environmental Engineering Group where he has been involved in thermal and structural testing and design of products ranging from Vidicons for TIROS to the Coaxitron Super Power Tube. He was instrumental in establishing a Finite Element Modeling capability at Lancaster and is an APL fanatic. Contact him at: Environmental Engineering, Electro-Optics and Devices, Lancaster, Pa., ext. 2077.

Staff announcements

Broadcast Systems

Appointment of **Gordon H. Allison, Jr.** as Administrator, Broadcast Audio Products, for RCA Broadcast Systems was announced today by **Verne S. Mattison,** Manager, Transmitter Equipment Engineering and Product Management. Mr. Allison is responsible for the product management of RCA's line of audio equipment for radio and television broadcasters, including audio consoles, tape recorders, microphones and other audio systems.

Consumer Electronics

Alfred Crager is appointed Manager, Test Technology. He reports to **Bennie L. Borman,** Director, Manufacturing Engineering and Technology.

Global Communications

Martin L. Finkelstein is appointed to the newly created position of Vice President, Service Assurance. In his capacity, he will be responsible for Quality Control Programs for Company services to assure customer satisfaction and compliance with Globcom standards of reliability and quality. Mr. Finkelstein will report to **Robert J. Angliss,** Executive Vice President, Switched Services. The organization of Service Assurance is announced as follows: **William F. Gerrity,** Administrator, Customer Service Assurance; **Richard L. Wickman,** Administrator, Quality Analysis and Control.

Laboratories

Carmen A. Cantanese has been named Head, Kinescope Systems, reporting to **Brown F. Williams,** Director, Display and Energy Systems Research Laboratory.

Missile and Surface Radar

Appointment of **Joseph C. Volpe** as Director, Product Operations, at Missile and Surface Radar (MSR), Moorestown, N.J., was announced today by **William V. Goodwin,** Division Vice President and General Manager. Mr. Volpe is responsible for engineering, manufacturing, and purchasing activities at Moorestown as well as for plant operations of the facility. He had served as Chief Engineer there since 1974.

Solid State Division

Thomas L. Cambria, Director, announces the organization of Management Information Systems as follows: **John W. Gaylord,** Manager, Computer Aided Manufacturing; **Thomas G. Kilroy,** Manager, Systems Integration and Control; **George J. Pulsinelli,** Administrator, MIS Administration; **Rajesh K. Tandon,** Manager, Application Development; **Edward J. Tirpak,** Manager, Computer Center; **William F. Cronin,** Manager, MIS Lancaster; **Didier Nicolai,** Manager, MIS Europe.

Rajesh K. Tandon, Manager, announces the organization of Application Development as follows: **Louis J. Ciabattoni,** Manager, Operations Support Systems Design; **David H. Lovell,** Manager, Decision Support Systems Design; **Louis Sand,** Manager, Financial Systems Design; **Rajesh K. Tandon,** Acting Manager, Plant Systems Design.

VideoDisc Operations

Bruce M. Allan is appointed Director, Video Systems Product Planning. In this capacity Mr. Allan will be responsible for Product Planning of the "SelectaVision" Video Disc Player. He will continue to report to **David E. Daly,** Division Vice President, Product Planning and Industrial Design.

Foy E. Wilkey is appointed Administrator, Video Systems Product Planning. He reports to **Bruce M. Allan,** Director, Video Systems Product Planning.

Promotions

Consumer Electronics

James C. Marsh, Jr. from Senior Member, Engineering Staff, to Manager, Project Engineering.

John C. Peer from Senior Member, Engineering Staff, to Manager TV Systems Development.

Robert M. Rast from Manager, New Product Development, to Manager, Digital Systems.

Solid State Division

Francis M. Dezura from Member, Technical Staff, to Leader, Technical Staff.

Stephen R. Reiutz from Member, Technical Staff, to Leader, Technical Staff.

Professional activities

Consumer Electronics

J. Wells and **G. Bogantz** were consulted and acted as directors for digitally recording the Commemorative 50th Anniversary Record Album for the Indianapolis Symphony Orchestra.

Laboratories

Paul M. Russo addressed the DSRC Colloquium in a personal presentation on the rapidly expanding capability of large scale integration (LSI) and its interaction with computer hardware and software technology. This interaction gave birth to the now ubiquitous microprocessor marking the beginning of the second computer revolution. Recent trends in digital LSI and their impact on microprocessor technology were reviewed. The microprocessor industry was discussed with special emphasis on unit sales projections and on the increasing challenges facing vendors. Industrial, commercial and consumer applications were overviewed. Finally, a few examples of microprocessor uses in RCA businesses and products were described. This presentation is highlighted in an article by Dr. Russo that appeared in the *RCA Engineer*, Vol. 25, No. 2, Oct./Nov.

A videotape of the talk is available on loan to RCA employees through Engineering Education in Cherry Hill. For information on getting the tape, call Margaret Gilfillan on TACNET 222, ext. 5255. Ask for Tape No. 168.

Recently, the Society of Women Engineers, whose New Jersey Section President is **Daryl Ann Doane,** a Member of the Technical Staff at the Labs, sponsored a day-long educational seminar/workshop: Insight—A Career Seminar—held at the Labs.

The purpose of the seminar/workshop was to help women understand how they operate in a business environment, and why they do so. The seminar/workshop sought to teach participants how to bring into a workable balance the demands of one's "corporate self" (operating within the corporate structure of a business environment) and the needs of ones "inner self." According to **Maida Berenblatt,** the Human Relations Consultant who designed and offers these seminar/workshops, "The corporate self and the inner self produce a working dialogue." Toward this end, workshop participants analyzed their work methods and responses, and related their inner reactions to the corporate interactions.

According to Dr. Doane, "the participants found the information presented on the dynamics of human behavior in the morning seminar informative and of value. The dialogue established between the leader, Ms. Berenblatt, and the participants during the afternoon workshop was especially helpful in examining patterns and alternatives for more effective interactions on the job."

The Society of Women Engineers was especially appreciative of the cooperation/sponsorship of RCA Laboratories **(Al Pinsky)** in hosting the seminar/workshop at the Laboratories, and in providing facilities, personnel and luncheon.

Books by RCA authors

Robert M. Mendelson of RCA's Solid State Division is the author of *Interrelated Integrated Electronics Circuits for the Radio Amateur, Technician, Hobbyist, and CB'er,* a book recently published by the Hayden Book Co., Inc., Rochelle Park, N.J.

The book provides a variety of projects that have appeal to the home builder. More than 25 useful circuits are described that can be built by any Ham, technician, or hobbyist who is able to use a screwdriver, pliers, and soldering iron. These circuits include power supplies and accessories, linear CMOS amplifiers, passive circuits (passive attenuator, Wheatstone bridge, resistance box), electronic measuring instruments, and games. Each circuit has been built, tested, and in many cases, used to aid in the construction of later projects. Although the projects use solid-state integrated circuits, a few useful passive devices are included. Most projects can be combined to provide higher performance.

Circuit operation is discussed in everyday language. Construction details, layouts, and photographs are provided for each project to simplify its duplication. While most circuits are shown on printed circuit boards, they all can be hand wired using perforated boards and terminals. Sockets are used for all ICs to allow for easy replacement and servicing. However, direct soldering may also be used.

Room is left for the builder's originality as, for example, in the mechanical construction of the DVM and digital probes or in packaging some of the circuit boards to fit individual needs. This should broaden the home builder's construction abilities in the very interesting field of solid-state construction.

Obituary

Evelyn Jetter

Evelyn Jetter, an RCA engineer who invented the ignition transistor used by the automotive industry, died on December 19 at Beth Israel Hospital in New York City. She was 52 years old.

Mrs. Jetter received her B.S. degree in Electrical Engineering from Cooper Union and her M.S. in Physics from Rutgers University. She was a founding member of the Society of Women Engineers.

Joining RCA in 1967, Mrs. Jetter was most recently employed as a member of the technical staff of the Solid State Technology Center at Somerville, N.J.

During the mid-1970s, Mrs. Jetter was granted a patent for her design of the original ignition transistor which is widely used by the automotive industry. RCA currently produces hundreds of thousands of these devices each month for two major auto manufacturers. Mrs. Jetter also was the primary developer of a group of epitaxial-base power transistors which are employed in many types of industrial and consumer electronic equipment.

In 1977, Mrs. Jetter received an achievement award from the David Sarnoff Research Center for her outstanding contributions to the development of a computer system for controlling semiconductor manufacturing.

Prior to joining RCA, Mrs. Jetter was employed by the Atomic Energy Commission and Lionel Industries.

Moorestown announces five third-quarter 1979 Technical Excellence Award winners


Mandour


Neilson


Pruitt


Smiley


Suhy

Five Technical Excellence Awards were presented to Missile and Surface Radar personnel during the third quarter 1979. The award winners and brief summaries of the citations are given below.

J.A. Mandour — for his computer algorithm that enables the AN/SPY-1A radar to acquire and track SM-2 vertically launched missiles at extremely short ranges. The SM-2 Vertical Launch System will replace the rail launchers now used, but ship and missile dynamics complicate AN/SPY-1A capture of each newly launched missile. Mr. Mandour's algorithm provides accurate designation of the AN/SPY-1A radar beam to the missile position.

J.O. Neilson — for developing the system design and computer software architecture for the Digital Control Processor subsystem of the Defense Unit Segment of the Low Altitude Defense System (LoAD). His innovative system design uses an eight-microprocessor architecture, thus achieving a low-cost modular structure that is both flexible and expandable.

D.L. Pruitt — for his technical leadership in the design and development of the Wide-band Amplifier, an advanced state-of-the-art transmitter. It includes several RCA design "firsts": the largest high frequency inverter power supply ever built, an SCR-controlled focus-coil power supply, all solid-state control logic, and transversal equalizer for better bandpass characteristics.

J.W. Smiley — for his design concepts and development of ADS-B1, a new system for logic capture, reproduction, and net listing used in the automated design of modules. Mr. Smiley's design is two generations improved over the current Autodraft system originally developed for AEGIS backplane design. ADS-B1 is currently operating successfully in support of PRIMUS logic design effort.

G.W. Suhy — for his technical achievements and leadership in the design and development of Build 3 of the AEGIS C&D Interface Simulator System computer programs. His simulator programs contributed directly to the testing and integration of the C&D tactical computer programs that will be used as part of the next AEGIS milestone tests (AIM-2).

Burlington gives second- and third-quarter Technical Excellence Awards

The Burlington Technical Excellence Committee has reviewed candidate nominations for the second and third quarters of 1979, and the results are: one team of three engineers and one technician; and two individual engineers have been cited for their achievements.

The individual awards go to:

Harvey Goldstand — for creative engineering work on the Vehicle Monitoring System. He specified, designed and conducted the development of a 17,000-word real-time, multi-mode, multi-task software system using the RCA 1802 microprocessor. This software was completed on schedule, in budget, and operated for over ten months and 12,000 vehicle test miles (equal to 300,000 road miles) without a single program error.

Peter Arntsen — for designing, building and debugging a complicated broadband communication jamming equipment. He invented an approach that circumvented the fundamental limitations imposed by a very wide frequency bandwidth and antenna problems. The scheme he devised is that a varactor is used to tune the narrow antenna bandwidth in synchronism with the jammer's VCO, as it is swept over the band of interest. Using this technique, he built a jammer which tunes over a two octave frequency band.

The team developed a laboratory model of an IR Schottky Barrier Camera which has achieved outstanding thermal sensitivity and imaging performance. Demonstrations with this camera during the past two months have yielded great enthusiasm by RCA personnel, outside technical consultants and prospective customers. Future system applications are being projected.

The specific contributions of each of the team members are as follows:

Mike Cantella — was overall team leader for the Schottky barrier IR sensor application development. This included theoretical modeling and assessment of CCD array, equipment and system performance com-


Goldstand


Arntsen

putations and coordination of associated device development at RCA Laboratories. He made significant contributions to the optical, electrical and thermal design of the laboratory model camera. A patent disclosure for a special video sampling technique was submitted jointly with J. Klein.

Jack Klein — had prime responsibility for electronic circuit development. This effort has included design of all timing, video and power supply circuits and optimization of readout modes. He displayed considerable ingenuity in instrumenting and debugging

the camera to provide an outstanding performance. Various test and data recording instruments were successfully integrated by him with the camera. This enabled acquisition and assessment of laboratory and field performance data.

Don Morand — was responsible for mechanical design. This activity included integration of optics, cold shield, dewar and CCD array components. He showed particular ingenuity in the means used to achieve excellent cryogenic cooling performance. This was accomplished despite difficult electrical and optical performance requirements. Also, a comprehensive thermal analysis model was developed by him. The package has been operated reliably in the field with no moisture condensation problems and with minimal consumption of liquid N_2, which are very important factors in making the demonstration a success.

Team leader Mike Cantella (4th from left) and members Jack Klein (2nd from left), Bob Sharland and Don Morand (2nd and 3rd from right, respectively) were congratulated by Dr. Harry Woll (left, Division Vice President and General Manager, Automated Systems), Fred Martin (3rd from left, Manager, Radiation Systems Engineering), and Gene Stockton (right, Chief Engineer).

Bob Sharland — was responsible for electrical fabrication and the assembly and test of all electro-optical components associated with the camera. The hardware elements that he worked with included electrical circuitry, optics, cryogenic instrumentation, high vacuum equipment, thermal sources and video and instrumentation tape recorders. He also accomplished significant results in interpreting diverse types of test data. He contributed materially to design changes which culminated in successful operation of the camera. In addition, he played an important role in the design, execution and interpretation of laboratory and field performance tests as well as carrying out the demonstrations.

Second manufacturing engineering productivity symposium held at Indianapolis

The Second Manufacturing Engineering Productivity Symposium was held at Consumer Electronics Home Office in Indianapolis, Indiana on November 13/14. Based on feedback from the inaugural symposium held in December, 1978, the format was expanded to two days and papers on very specific topics having broad interest were presented. It is felt that this time away from the production environment for a discussion of problems, ideas, and technologies with other members of the manufacturing and industrial engineering community was highly valuable and helped to upgrade the overall manufacturing engineering effort within the corporation. The meeting was organized and directed by **Steve Race,** Manager of Manufacturing Services.

This symposium was divided into two general areas with papers on the first day focusing on Computers in Manufacturing and, on the second day, on New Processing Techniques. In addition, arrangements were made for **Dean Poeth** of the highly respected Battelle Laboratories to present a summary of their research document prepared for the Society of Manufacturing Engineers entitled *Future Trends in Manufacturing Technology*. Two tours were conducted for the symposium: a tour of the IEMS facility in the Bloomington plant on November 13 and an optional tour of the Safety/Reliability laboratory on November 14.

A videotape of the talks is available on loan to RCA employees through Engineering Education in Cherry Hill. For information on getting the tape, call Margaret Gilfillan on TACNET 222, ext. 5255. Ask for Tape No. 411.

Symposium agenda

November 13 — Computers in Manufacturing

"Computer Applications in Process Control"	**R.A. McFarlane,** SSD
"The Development of Computer Aided Automatic Insertion"	**M.J. Gallagher,** GSD/CCSD
"A Programmable Controller Application in Injection Molding Machines"	**R.E. Wartzok,** Records
IEMS Update	**J.S. Race,** CE

November 14 — New Processing Techniques

"Manufacturing Engineering Education — Future Directions?"	**F.E. Burris,** Staff
"Ultrasonic Cleaning of Color Picture Tube Subassemblies"	**W.R. Rysz,** PTD
"An Automated System for Printed Circuit Board Production"	**J.R. Arvin,** CE
"Non-contact Inspection and Measurement"	**D.P. Bortfeld,** Labs
"Future Trends In Manufacturing Technology"	**D. Poeth,** Battelle Labs

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Custom LSI symposium held at DSRC

A Corporate Symposium on the subject of custom LSI circuits was held on December 11 at the David Sarnoff Research Center in Princeton. Jack Hilibrand of GSD Engineering served as chairman of the symposium. The objective of the symposium was to encourage the use of custom LSI arrays within RCA by:

- Describing successful programs;
- Reviewing problems encountered;
- Discussing the potential of custom LSI for enhanced RCA competitiveness at the system level; and
- Presenting the resources available within RCA for custom LSI implementation.

If you were unable to attend and are interested in the content of the talks, consult the following sources:

- Copies of the speakers' viewgraphs...these can be found in RCA technical libraries. A few copies are available for those not having access to a library: contact Jack Hilibrand on TACNET 222, ext. 5035.
- Videotapes of the talks...these are available on loan to RCA employees through Engineering Education in Cherry Hill. For information on getting the tapes, call Margaret Gilfillan on TACNET 222, ext. 5255. Ask for Tape No. 412.

Also, some of the papers presented will appear in the *RCA Engineer*, Vol. 26, No. 2, Aug./Sept. 1980.

Speakers and topics that were covered are listed below:

"GVS-5"	**J. Woodward** Automated Systems	"Tools for CAD"	**L. Rosenberg** Solid State Technology Center
"Tenley/Seeley"	**E. Mozzi** Government Communications Systems	"Standard Cells & Beyond"	**A. Feller** Advanced Technology Laboratories
"I^2L at Lancaster"	**R. Rodgers** Electro-Optics and Devices	"Testing Custom LSI Arrays"	**T. Mayhew/ R. Bergman** Solid State Technology Center
"Custom LSI in Automated Cameras from Broadcast"	**A. Lind** Broadcast Systems		
"Custom Parts at Consumer Electronics"	**J. Carnes** Consumer Electronics	"Custom Microelectronics in Automotive"	**T. Crossley** Solid State Division
Keynote Speaker	**H. Kressel** RCA Laboratories	"Universal Arrays in Avionics Systems"	**R. Aires** Avionics Systems

Microprocessor applications symposium held at DSRC

A Corporate symposium on Microprocessor Applications was held at the David Sarnoff Research Center in Princeton on November 7. Fifteen papers described how microprocessors are being put to use to enhance technical designs or solve problems. The attendance of 145 evidenced the high interest in the topic.

Wendell Anderson, Staff Technical Advisor, Government Systems Division, served as the program coordinator. **Don Latham,** Division Vice President, Engineering, GSD, in an introductory talk, discussed the issues and concerns associated with microprocessors and their applications.

Copies of the viewgraphs used in the talks will be available in RCA technical libraries. Wendell Anderson has a limited number of copies available for those RCA employees not having access to a library. Contact him in Cherry Hill on TACNET 222, ext. 5835 for a copy. For more information on a specific talk, contact the author.

The speakers and topics that were discussed are listed below:

"Microprocessor in the TK-47 Color Camera"	**B. Hurley** Broadcast Systems	"The P50M: A Microprocessor-Based Signal Processor Using the PRIMUS Weather Radar"	**B. Buch** Missile and Surface Radar
"Microprocessor Applied to Broadcast Video Tape Recorder"	**K.J. Hamalainen** Broadcast Systems	"MASS: A Modular ESM Signal Processor"	**A. Kaplan** Government Communications Systems
"Microprocessor FM Transmitter Controller"	**E. Kohn** RCA Laboratories	"Automated Potentiometer Testing"	**M. Cherbak** Consumer Electronics
"Distributed Microprocessor Systems"	**T.A. Martin** GSD Engineering	"Automated Keyboard Tester"	**N. Fedele** RCA Laboratories
"Sonar Signal Processing with ATMAC"	**W. Helbig** Advanced Technology Laboratories	"Auto Programmer for Programming TV Viewing"	**B.W. Beyers** Consumer Electronics
"Microprocessor Requirements for Next Generation Engine Test Equipment"	**M.J. Gilbert** Automated Systems	"Microprocessor for Energy Management"	**K.S. Vanguri** RCA Laboratories
"Architectural Tradeoffs for Advanced Spaceborne Computers Using Bit-Slice Approaches"	**K.K. Oey** Astro-Electronics	"Interpretive Programming of Controller Applications"	**P.K. Baltzer** RCA Laboratories
"Microprocessor Applications in Radar Control"	**W. Verheggen** Missile and Surface Radar		

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