RCA Engineer

20th Anniversary Issue

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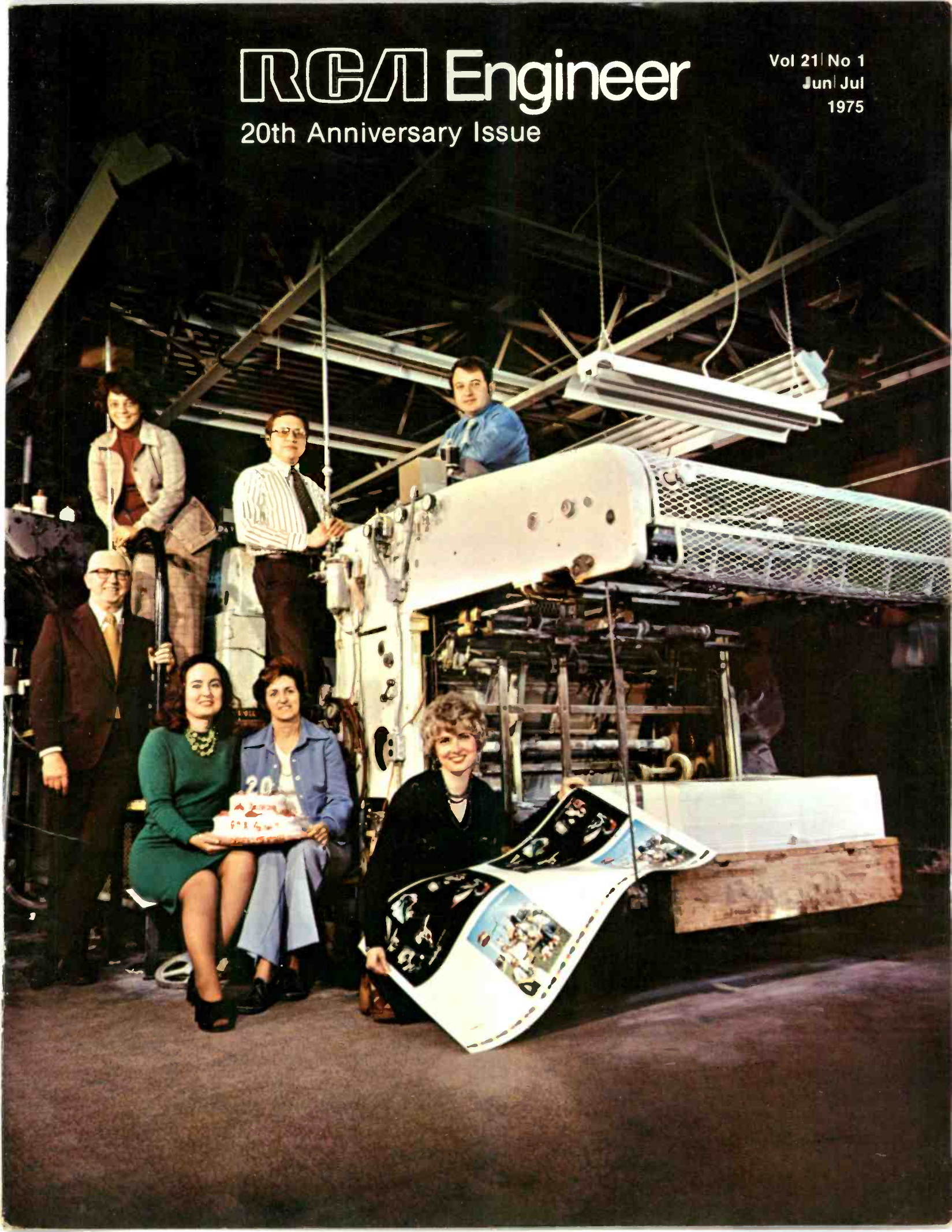

The "easy road"...

In marking the *RCA Engineer's* 20th anniversary, I offer two thoughts as the journal's first editor. *First*, thanks to the editorial staffs and the readers (who are the contributors) for supporting the journal since its inception in 1955. *Second*, before my retirement early next year, I'd like to share with you an overriding thought which has haunted me during my editorial work with RCA's engineers. My concern relates to the role of the engineer in carrying out technical communications processes — a challenging and seemingly difficult path; but, in the long run, it is the easy road.

The easy road to business success calls for a sound and sought-after product— aggressively marketed at a reasonable price that returns a fair profit. Utopia? Not at all. The first two ingredients — a sound product, and a viable market — are achievable through capable engineering in companion with solid marketing research and careful sales planning. Then, why do some excellent products fail to attract favorable attention? What are the missing links?

"Guilty" are gaps in two essential communication areas: early proprietary documentation and subsequent non-proprietary technical communication. Both are easily overlooked! But how can such omissions occur at RCA where everyone knows the value of research, design, and patent data — where technical reports supply proprietary know-how, where technical papers create strong product interest — and where the basic information is adapted later for instruction books, service notes, technical advertisements, etc.?

The answer is *such omissions occur very easily* — whenever communication needs are set aside during design deadline pressures and short manufacturing-engineering schedules. Granted, speed helps beat competitors to the marketplace; but, not having the supporting product information on time can lead to serious problems. Engineers and managers who postpone writing about current designs inevitably find themselves already in the next design phase. Then, producing vital technical data and sales literature often means launching a costly "crash" program, frequently "too little and too late."

Everyone needing technical information relies on RCA's engineers and scientists who must have strong management support during demanding product cycles. The whole complex of formal and informal channels of communication is critically important. Acceptance of this concept at all working levels is a potent force in advancing our business posture.

So, take the easy road; keep everyone informed by providing enough time to complete your technical communications. In doing so, you'll help assure the prosperity of your product designs and your company's business.

W. O. Hadlock

W.O. Hadlock, Manager
Technical Communications
Corporate Engineering
Cherry Hill, N.J.

Our Cover

...from the people who bring you the *RCA Engineer*. The entire *Engineer* staff is gathered around the two-color press (used to print *RCA Engineer* covers) to celebrate the journal's twentieth anniversary. Seated, holding the cake, are Juli Clifton (left) and Dottie Snyder. Joan Dunn (front) is holding a press sheet of the last two covers. From left to right are Bill Hadlock, Pat Gibson, Frank Strobl, and John Phillips.

The back cover shows the staff in various phases of editorial work; interspersed are several *RCA Engineer* covers from the past twenty years. The group photo on the back cover shows editors Hadlock (seated), Strobl (left), and Phillips, in a planning session with TPA's (left to right) Joe Steoger (Service Company, Cherry Hill), Tony Liguori (GCASD, Camden), and Don Higgs (MSRD, Moorestown).

Credits:
Photography: John Semonish, Commercial Engineering, Picture Tube Division, Clark, N.J.
The printing press on the front cover belongs to LPI/NDI, Pennsauken, N.J.

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RCA Engineer

• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

Contents

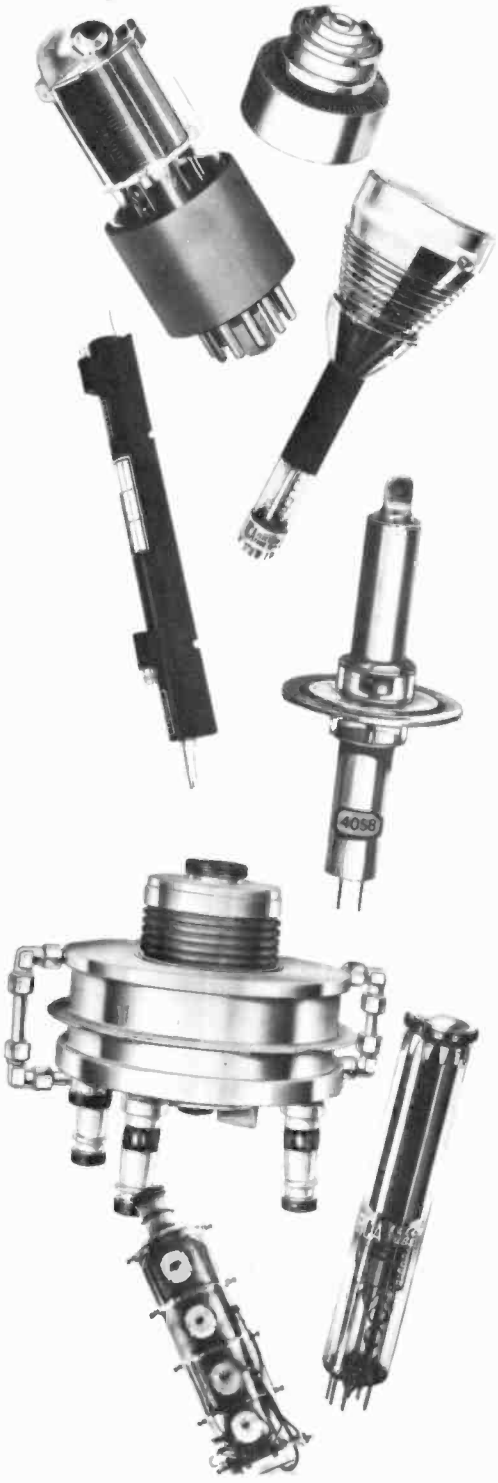
Emphasis —20th Anniversary Issue

The Engineer and the Corporation

Electron tubes — a technology forecast

H. K. Jenny

Electron-tube technology is frequently predicted to be a vanishing force in electronics or, at least one in limbo. However, domestic electron-tube sales volume accounts for three-billion dollars today. The major factors affecting the future of the electron tube such as its coexistence with several companion technologies involving electro-optic detection and imaging applications requiring a number of specialized devices are discussed. The future role of camera tubes and lasers plus the use of a number of electron tubes in high-power and microwave applications are reviewed. Microwave cooking devices and electron-tube displays are other applications mentioned. In addition, the unique characteristics of certain electron tubes that make them solidly entrenched from both performance and cost considerations are presented.



IT IS USEFUL, from time to time, to look at a product area to consider what has happened to it, where it is, and where it might be going.

The title *technology forecast* is rather pretentious for such a review; in reality, it is more of a probing effort aimed at highlighting some of the implications to those interested in the fields covered.

Hans K. Jenny, Senior Technical Advisor, EO and Devices, SSD, Lancaster, Pa. received an MS in EE from the Swiss Federal Institute of Technology in 1943 where he was active as Assistant Professor until 1946 doing research on low noise behavior of klystrons. He joined the RCA Tube Division in 1946 as microwave tube design engineer. Later, he became Engineering Manager of groups concerned with microwave tubes and solid state devices and Operations Manager, Microwave Solid State Operations in Harrison. Since 1972, he has been Senior Technical Advisor of the Industrial Tube Division which has recently been renamed and incorporated in the SSD organization. Since writing this article, Mr. Jenny has joined the Staff of Engineering Professional Programs.

Although one may feel eminently well qualified to visualize the future in one's specialities, experience has proven that many events have not occurred in the predicted manner (example: the heralded arrival of interactive tv in the home) and more or less unforecasted events have materialized with surprising speed and magnitude (calculators). Unpredictable breakthroughs on one hand and interaction of politics, economics and social problems on the other play a key role in keeping the future an exciting challenge and the forecaster aware of his humble capabilities.

What about the predictions[1], now almost twenty-five years old, that solid state is taking over and tubes represent a dying, antiquated species?

The magnitude of today's electron tube sales volume does not bear this out. Have we reached the top plateau in tube technology? Although the phase of maximum inventions may have passed, a review shows a surprising amount of progress in performance, and a continuing and successful engineering effort. It is hoped that the following review may stimulate today's engineer to consider a

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Final manuscript received March 26, 1975. A more detailed version of this paper was presented at the IEEE Intercon 75, New York City.

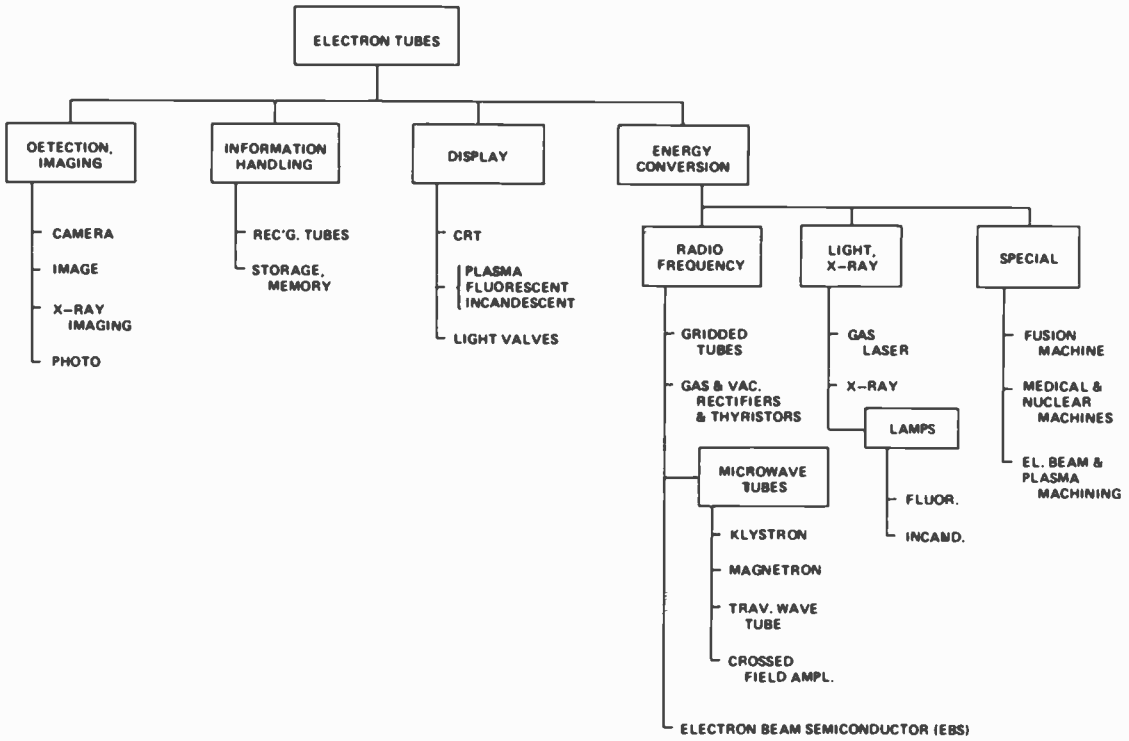

Fig. 1 — The electron-tube family tree.

career in this fascinating and challenging product area and to remind management, marketing and government agencies that much gold remains to be mined in this business.

The electron tube business

The product variety that comprises the electron tube family is outlined in the *family tree* of Fig. 1. This tremendously broad spectrum of products is responsible for an annual U.S. sales volume of around three billion dollars today.

Lamp business represents the oldest, most mature and quite profitable sector of the tube business and continues to grow at about 7% per year. Ninety percent of sales is in replacement business. The technology is not yet saturated and improvements in phosphors have been yielding substantial (30%) brightness advances in the past twenty years. Today, with energy conservation at a premium, continued progress can be expected.

Fusion power should play a major role in the energy supply during the next century. With mounting emphasis on the necessary research to evolve practical systems, quite a number of large fusion machines of the Tokamak[2] type will be built during the coming quarter century. Each machine requires the expenditure of many tens of millions of dollars and involves a substantial expertise in electron tube technology.

It is significant to review the electron tube families concerned with electronic systems.

Consumer markets have accounted for about 70% of electron tube sales during the past 40 years; three new consumer market potentials which could have a substantial effect on future sales will be discussed.

In 1965, worldwide electron-tube business was about twice that of U.S. sales. This ratio grew to 3 times in 1975 and is expected to be 5 times by 1985, thereby providing more potential. There is a growing trend for European and Japanese R&D efforts to be strongly directed at challenging the U.S. technical lead.

What keeps the tube business healthy?

The Major factors influencing the health and future of the tube business are listed in Table I. In tracing these factors through the major tube families, it should be noted that an upward integration, in particular, leads to products falling outside the definition of "electron tube". However, these devices and products are now becoming an important part of the world of the electron tube businesses and their engineers; thus, the effects of such products are considered also.

Special characteristics

Consider a rocket moving through the atmosphere, heavily hindered by heat-creating friction, then breaking out into the free flow of outer space — the perfect vacuum. Similarly, the electron encounters substantial obstacles when mov-

Table I — Factors influencing the electron tube business.

a) *Firm entrenchments* in an established market

b) *Special characteristics* better suited to use than competing technologies

c) *Continuous upgrading* of cost effectiveness through:

Cost/Life/Reliability Advances
Performance Improvements
Performance Extension Through *Hybridization*

d) Business base extension through *Upward Integration*

Table II — Types of upward integration.

Category	*Description*	*Examples*
Component integration	Include circuitry to achieve higher levels of performance	Microwave tubes Radiosonde Tube/cavity combination
Functions	To provide customer with a product that is easier to use, has higher reliability	Tubes with modulation, control and power supplies CRT's with yokes PMT's with power supply & amplifiers Scanners (laser & detector combination)
New generation products	Utilize established expertise in a market to replace own products with a more advanced technology.	Microwave solid-state products *Si* Target Tubes CCD's and Flat panel tv
Systems	Provide end-use item utilizing component base (especially high-volume/low-cost products), cut multiple mark-ups, increase cost effectiveness.	Cameras

ing through semiconductors as compared to more ideal conditions in vacuum. By greatly shortening the path that the electron encounters in its strenuous journey — the fabulous family of semiconductor devices has been born, a family ideally suited for low-power, moderately fast information handling. Astounding progress has been made by squeezing thousands of functions into a microspace.

But, those electrons in vacuum are ready to move rapidly, require little energy to be guided and modulated, move in dense high-energy packs or finely defined electron beams, and can be accelerated to much higher velocities than can be done in semiconductors. This feature gives electron tubes their special characteristics and advances their competitive position.

Inertia in solids is a basic phenomena limiting semiconductor performance. Attempts have been made to find a solid state analog to electron tubes by, for instance, stacking photoconductors between interaction media. Best performance, you guessed it, is achieved when the media is a vacuum!

Hybrids

Products combining electron-tube and solid-state technologies are called hybrids. Application of solid-state technology to certain tube families usually extends performance and prolongs the life span of these products. Some hybrids have reached the market (silicon target camera tubes, photomultipliers with III-V compounds, etc.), but many are still in the development stages.

Through an entrenchment in a market with electron tubes and newly gained solid-state expertise, the electron-tube manufacturer is now in an excellent position to move into competitive technologies, obsolete outdated products, and remain in the market.

Upward integration

At one time the world of the electron tube engineer (and business) extended little beyond the vacuum envelope. Things have been changing a lot since then. The expansion of the products made by the tube business through several levels of upward integration is outlined in Table II. By growing from component to function, moving into solid-state technologies and even on to some end-user products, the scope of the electron tube business and the engineer is greatly enlarged. The degree to which the tube organization is willing and able to pursue upward integration has a profound effect on its growth potential.

The parameters of longevity

The receiving tube story portrays well the parameters of longevity; once a cost-effective product is introduced, it develops a strong lifeline and tremendous resistance towards obsolescence by more modern technology. Today, the life of the receiving tube is approaching its end, but what a fascinating story!

The receiving tube

Conceived in the early 1900's (Fleming diode 1904, De Forest triode 1905), the receiving tube really got today's electronics industry going. During World War I, production started for military equipment and later on the home radio provided the first electronic consumer market. Black & white tv was demonstrated at the 1939 World's Fair to the public and got off the ground after World War II, but not before the bombshell of the transistor discovery in 1948 initiated the dire prediction of impeding obsolescence of these tubes.

So what happened? The information on Fig. 2 reconstructs and illustrates the history of one of the most successful and profitable product lines of electronic business. Consumer product use means very large volume. The pricing curve showing price increases as volume built up reflects new types required by television and indicates a cost effective product operating at good margins.

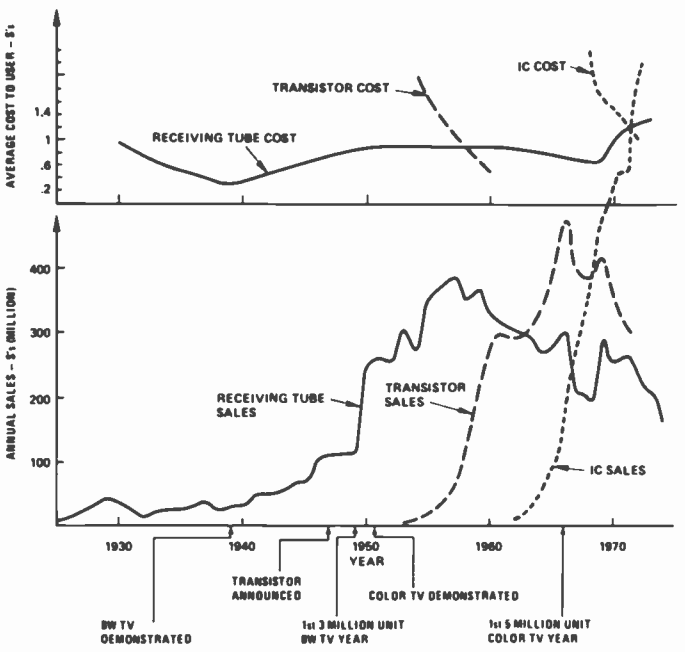

Fig. 2 — History of receiving tube sales and user costs.

It was not until 10 years after the announcement of the transistor that the new device became cost effective and really started competing. The effect on receiving tube prices then was not profound, the build-up of color tv provided new opportunities and it was not until 1966 (the first 8-million color set year) that volume dropped substantially — but not only for receiving tubes (a dip occurred in the economy). The transistor had also found an opponent in the evolving IC that was eventually to march off with the spoils. During 1974, the change of the tv industry to all solid state, except for the picture tube, shifted the role of the receiving tube to that of a replacement product only.

What this example shows is that receiving tubes, entrenched as the first comers, have held on for over three quarters of a century. And, after their obsolescence was indicated by the birth of the transistor in 1948, over 90% of total receiving tube sales volume was still to materialize!

The changing technology

Electro-optic imaging and detection tubes are entering an era of changing technology in which early challenges by new approches are being felt. This era may cover many, many years with fierce competitive action and coexistence of several technologies.

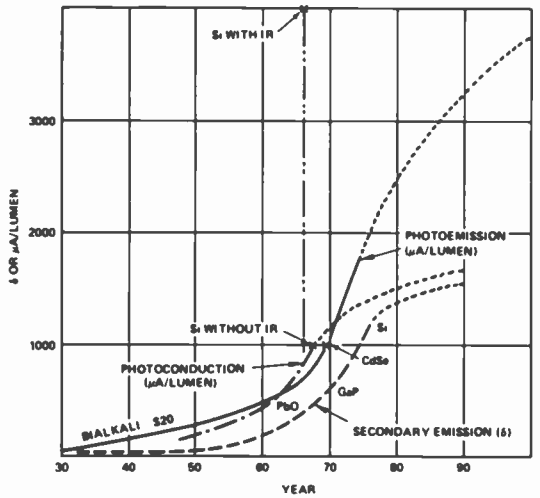

Fig. 3 — Historical progress of photoemission, photoconduction, and secondary emission.

Electro-optic detection and imaging tubes

Performance Upgrading — Applications of light signals involving conversion of photons to electrical signals continue their vigorous growth as television pick-up technology expands from broadcasting into industrial and commercial uses and later moves on into consumer products.

Sensitivity, resolution, lag, and cost represent the primary considerations for these products, with secondary ones being blooming, gain-bandwidth, portability, etc. Fig. 3 shows that conversion yields and secondary emission factors, major contributors to sensitivity, have shown very substantial improvements during the past years. The major gains in photoemission and secondary emission have been obtained by use of negative electron affinity surfaces (NEA) (III-V compounds and *Si* surfaces covered with monolayers of C_s and O)[4,5]. In predicting technology progress, cognizance must be taken of the fact that transmission-mode photocathodes are not yet equivalent in surface smoothness to reflection-mode cathodes, which have found their way into commercial products. The problems of improving smoothness and uniformity are, therefore, as important as further increases in sensitivity. As for the photoconductors, here also, performance requirements other than sensitivity (dark current, lag, process cost, etc.) contribute to the decisions governing their usage in tubes.

Hybrids — an approach to improved products

The combination of tube and solid state technologies have led to a number of viable new products and there are more to come. Among the new products are:

- *Photomultiplier* tubes with III-V compound elements are now commercially available.
- *Silicon target* (an array of silicon PN junctions) camera (ST, SIT, ISIT) tubes and storage tubes have already established themselves as an important and growing segment of the camera tube business. Some of its properties are indicated in Fig. 3. In addition, key characteristics include high reliability and a very long life.

- *Image-CCD*, a potential newcomer, is a combination image-intensifier tube with a CCD imager replacing the coventional phosphor target. Such a device combined with signal processing and a CRT-type display may leapfrog today's three generations of image tubes.

- *Hybrid photomultiplier tubes* combine sensitive photomultiplier front ends with electron bombarded target arrays as used in the EBS (Electron Beam Semiconductors), and could lead to more sensitive, higher resolution equipments.

None of the above-mentioned new products require technological breakthroughs but rather application of evolving technology in a cost effective manner. The demonstration of operating hardware is likely to occur in the next five-year period.

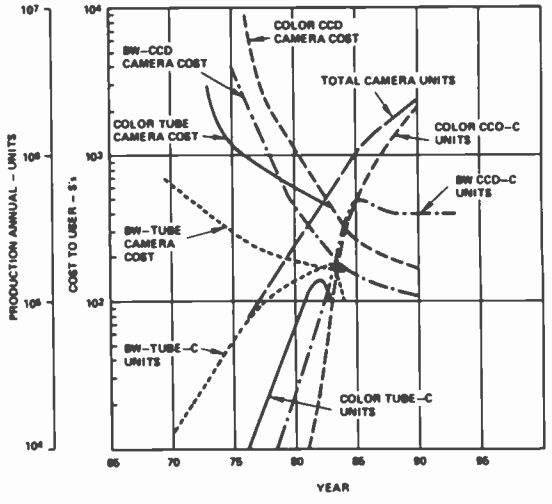

Fig. 4 — A possible outlook scenario for low-cost tv cameras.

Photomultiplier tubes

The versatile, sensitive photomultiplier tube has been finding many new uses during the past ten years resulting in an enviable steady growth pattern. Its applications cover the gamut from scientific instrumentation through medical equipment, laser ranging and communications equipment, character recognitions systems (such as point of sales equipment) to video playback equipment for consumer use. Its important parameters cover spectral response, frequency response, noise and performance uniformity.

The technical progress can be expected to continue as the quest proceeds for quantum efficiencies closer to 100%. Today's standard product ranges only about 10 - 15% (with the best bialkali tubes around 40%). Other performance upgrading is expected by pushing frequency response further into the IR range, attaining higher speed dynodes, and by improving electro-optics.

What about competition from the semiconductor photodiode? While each specific application may deserve a tradeoff study for tube versus semiconductor diode use, the following applies: The photomulitplier is best suited for applications where:

1) Large detector area is required,
2) Signal consists of a few photons only, and
3) Very high gain/bandwidth product is required

The semiconductor diode is best suited for applications where noise is not a major applications consideration. Also, applications in the infrared spectrum requiring cooling can take advantage of the, physically, much smaller diode.

Camera tubes

Rapidly expanding applications of camera tubes include: television broadcasting, military low-light-level uses, and closed circuit television, (covering security, surveillance, education, training and other applications). Home video-tape recording and electronic movies, sustain another creative and competitive activity. Historically, image orthicons utilize low quantum efficiency photoemitters. Nevertheless, such tubes have been largely displaced by devices using high quantum efficiency photoconductors, and a never ending procession of new types with different materials that yield improvements in several important performance characteristics.

It is in this field, that a most exciting semiconductor competitor in the form of the charge coupled (CCD) imager is making its early appearance and threatens to eventually take a big bite out of what has been exclusively a tube market.

We reach the challenging stage of looking at the future of camera tubes and competing CCD imagers. Easiest, probably, is a prediction of continuing camera tube use for applications requiring very high quality reproduction of images, such as tv studio use and high-fidelity tv utilizing

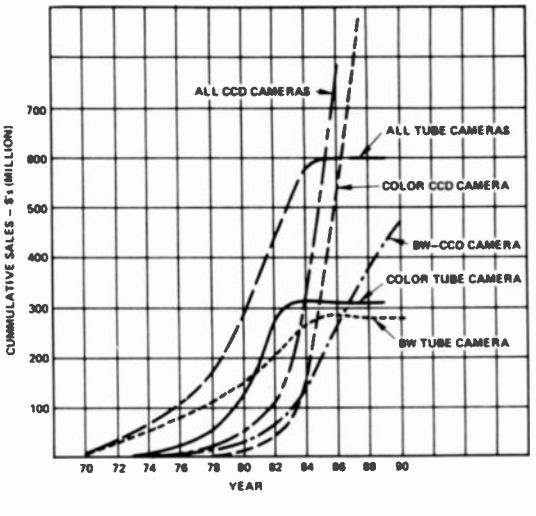

Fig. 5 — Sales of low-cost cameras, past and projected.

1000 or more lines. Movie makers will use videotape instead of film to compose and edit — and save through instant replay, many costly scene-shooting duplications. Space surveillance requires high resolution. And someday probably, CATV or satellite-to-home services, not encumbered by today's bandwidth limitations, will offer high-fidelity tv.

Another strong point of tubes is their very low-light-level capability which has no solid state equivalent. This capability could result in a hybrid with an image-tube front section coupled to a CCD imager. This low-light-level market will remain in the tube domain for many, many years.

Today's fastest growing camera market (in units) is in closed-circuit tv and the day of cameras reaching the consumer market is within the prediction span of this report. How fast will this camera market grow, and what will be the mix between B&W and color cameras, between tube and CCD cameras?

The following example is an attempt to estimate the life span of the vidicons used in this low-cost, high-quantity camera market. Fig. 4 sets the scenario showing total camera units and cost progression for B&W and color, tube and CCD cameras. To avoid an overly optimistic result for the tube cameras, the learning curve for the CCD cameras was assumed to be twice the rate of the tube cameras to the point where the costs converge. It was also assumed that once the CCD camera cost approaches the tube camera cost, the life of the latter has ended. This assumption is not the case for the vidicons, because replacement tubes will still be needed for a number of years.

Fig. 5 shows the cumulative sales resulting with various types of cameras. This pictures the total annual CCD-camera units produced to equal total tube-camera units in the year 1983, and cumulative sales for the two to be equal in 1986. The point to be made: exciting as the new technology is, the takeover is only accomplished after years of fighting down the learning curve to cost effectiveness.

Summary of electro-optic detector & imaging tubes

Because of their special characteristics in applications requiring large size, detection of a few photons or a very high gain/bandwidth product, tubes will persevere for many years.

Upgrading is taking place most actively though hybridizing of tube and solid state technologies and will continue.

Upward Integration is a fairly new endeavor in this product area, but is catching on.

Even though solid state competition is active, this product area shows good growth potential and a long life span.

The holdouts

Among the tube families most solidly entrenched because tube characteristics fitting the application needs have not encountered a strongly competitive technology are high-power gridded tubes, microwave tubes, and large display tubes.

High-power gridded and microwave tubes

Power and microwave tubes have matured substantially during the past years. One can state that for almost any conceivable need today, a specific tube can be developed rapidly, with high confidence and without requiring technological breakthroughs.

Special characteristics — power capability — Because of electron velocity saturation in semiconductors, electron tubes can theoretically provide power levels in excess of those of semiconductors by a factor of about:

$$\frac{\text{Output power of vacuum tubes}}{\text{Output power of solid state devices}} \cong \frac{\text{Speed of light}}{\text{Saturation velocity}} = 3\times10^{1}$$

Today, the gap is still substantially wider and, as applications require higher power and frequency levels, the electron-tube position gets increasingly more secure.

Fig. 6 shows power capability versus frequency for gridded tubes and microwave tubes as compared to solid state devices (today and in 1980). This comparison is valid for single devices and does not include the combination of devices through circuiting. It is easy to see that tubes have no match as far as high-power capability is concerned. It is not expected that single semiconductor devices will come within four orders of magnitude of high-power devices in the next twenty years. But, of course, power is not the only criteria since relatively few applications require power levels approaching the peak tube capabilities.

Performance upgrading: Matrix cathodes — Despite the fact that nickel and tungsten matrix cathodes have been around for many years, there are still tube types that can profit in life, reliability, and power capability in a cost effective manner from incorporation of a matrix cathode. Such efforts are under way.

Grids — Grids represent the limiting link

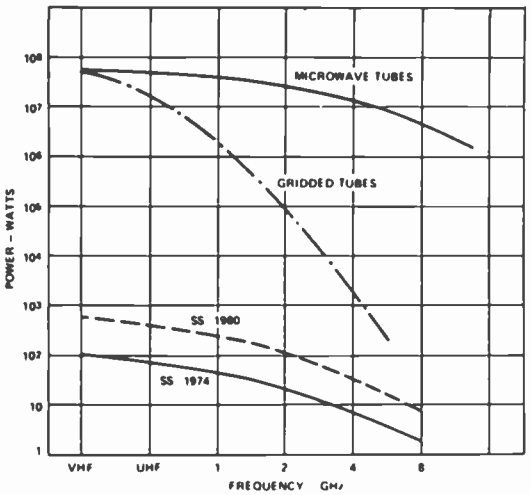

Fig. 6 — Power capabilities of electron tubes and solid-state devices.

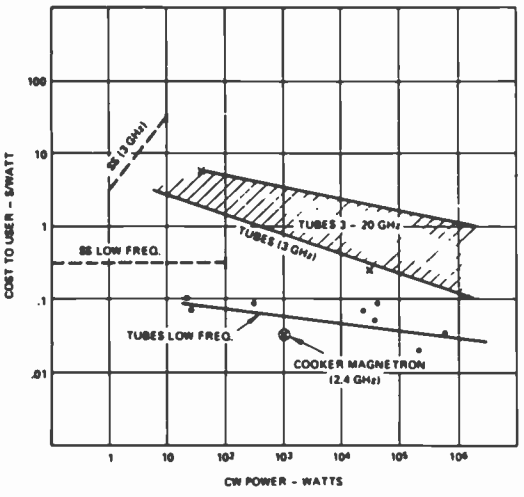

Fig. 7 — User cost (1974) of electron tubes and solid-state devices as a function of power and frequency.

in many power tubes, and excellent progress is being made with either coating of grids with material such as zirconium carbide and platinum to increase heat radiation and suppress grid emission, or use of pyrolytic graphite (crystallized carbon) which has most interesting and suitable anisotropic properties.

Shadow grid guns — Non-intercepting gridded guns are finding increased use in both gridded tubes and high-power linear-beam microwave tubes. A shadow grid placed near the cathode shields the control gird and cuts grid interception to a few hundredths of a percent of the beam current. Spacing between shadow grid and cathode is critical. Effort is underway to place a shadow grid, covered with non-emissive coating, on top of the cathode, thus operating at cathode temperature. The most laminar beam is obtained with this configuration[3].

Cost effectiveness — If we look at a comparison of costs (dollars per watt), again for single devices, we find in Fig. 7 that tubes still hold an edge at power levels above a few watts. Low-frequency applications up to a few watts have gone solid state, and even at microwave frequencies, narrow-band requirements up to a few watts are being lost, to the solid-state technology. And yet, the small power tube business is hanging on much longer than expected because of its favorable cost/performance ratio. Parallel and series operation of solid-state devices can be utilized to increase their power capability; however, cost and complexity of circuitry as well as difficulties dealing with the resulting extremely low-impedance levels limit the competitive potential of such an approach.

Magnitude of usage has a profound effect on cost. Note the extraordinary performance of the single power tube consumer product — the S-Band cooker magnetron. The cost per watt for this tube, even including the microwave oscillator circuitry, is almost two orders of magnitude below the S-Band tube cost curve.

Efficiency — Tube efficiency is playing an increasing role in today's world of energy shortage and satellite communications. Older principles of raising voltage, tapering circuits, tilting-fields, and depressing collectors, are now being applied in practice in modern tubes with travelling-wave tube efficiencies reaching 50% and klystron efficiencies approaching 70%, making them quite competitive with crossed field devices.

Bandwidth — Multi-octave helix-type travelling-wave tubes are appearing at increasing power output levels, utilizing dispersion-shaping support structures. Kilowatt peak output from 2 - 7 GHz has been demonstrated.

High-power coupled-cavity travelling wave tubes covering 45% bandwidth are being demonstrated utilizing two adjacent modes[3].

Focusing — The use of samarium cobalt magnets has allowed very substantial reductions in the weight of the magnet structures. Mini-travelling-wave tubes with watts of power output and wide bandwidth weigh a half pound compared to three to six pounds for earlier tubes. At present, the cost of these magnets still exceeds that of conventional focusing structures by a factor of four, and effort is directed at reducing this cost as well as expanding the application of these new materials.

Cost and reliability — There is much activity in the area of improving cost and reliability. Novel ways of cost reduction include application of solid-state technology such as is used in the printed-circuit travelling-wave tube. This approach allows substantial cost reduction for sizable production volume, but at the expense of several performance parameters.

Upward integration continues in an effort

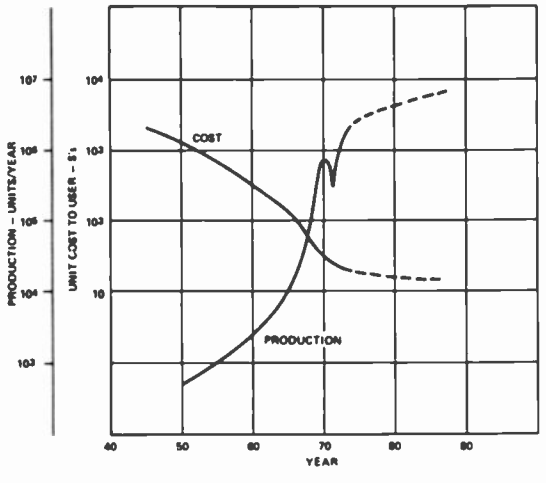

Fig. 8 — Production figures and user unit costs of cooker magnetrons, past and projected.

to enhance reliability and cost effectiveness. Microwave tubes, through necessity, have always included rf circuitry. Now, the packaging of power supply and modulation circuitry with the tube further eases the interfacing task of the user and increases life because the tube manufacturer can set operation parameters compatible with reliable operation.

Hybridization — The electron-beam semiconductor — Utilizing an electron beam to produce carrier multiplication in a pn junction represents a tube/solid-state hybrid with considerable promise.[3,6] Early work on the effect of electron bombardment of semiconductors started in the 1940's, but it was not until the 1960's that substantial, government-supported effort got underway to develop practical devices. One of the first major obstacles encountered was the stability of the semiconductor junction under the influence of electron bombardment. Substantial progress has been made in the past few years with encouraging life test results reported by several laboratories.

In the meantime, the controversy whether an electron-beam semiconductor (EBS) contains all the advantages or all the disadvantages of tube and solid-state technologies continues because the expected high level of microwave performance combined with small size and low cost potential has been elusive much longer than expected. The glimmer of hope continues, however, fanned by results such as the recent demonstration of 500 watts peak power at 1 1/2 GHz with 23 dB gain and 7% bandwidth. Future success will depend on continuing substantial R&D funding in an attempt to fully exploit the potential of these devices.[3,6]

The Cooker Magnetron — Potential of microwave cooking for the home was visualized right after the birth of powerful, efficient mangetrons in World War II. A chicken and egg situation existed. Potentially, low cost and high production rates were indicated, but lack of consumer appetite to pay for the startup costs and some question as to the market buildup rate held development back. Thus, the consumer cooking range played the stepchild role for many years as early business materialized in the low quantity, moderate cost commercial market (restaurants, airplanes, etc.). During the fifties and early sixties consumer-oven pioneers languished.

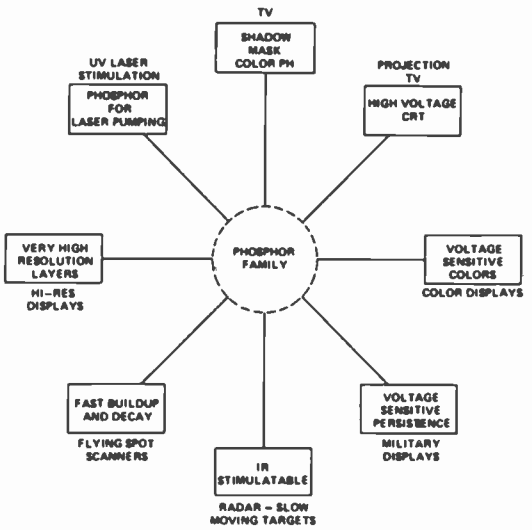

Fig. 9 — Phosphor capabilities.

It was the Japanese government that stimulated the major growth through a well developed program to educate their consumers through trained home economics teachers in the advantages and usage of microwave cooking. During 1969 microwave ranges took off in Japan, only to be squashed in 1971 by a radiation scare. However, prompt attention restored consumer confidence and a tremendous growth pattern was re-established. Fig. 8 shows annual Japanese unit production and costs.

At this point, magnetron production is around 2 million units/year and rising; the magnetron price appears to have stabilized around $20, and this new tube consumer business appears well established. Presently, the major portion of magnetrons are foreign built, with Japan the largest manufacturer. However, it is expected that the sharply rising U.S. domestic market will attract increasing domestic manufacture. At 3 cents per watt and tube reliability high, this socket will be difficult to displace.

Summary — high power gridded and microwave tubes

There is no competitive very-high-power technology yet evident.

Upgrading — Power tubes are very cost effective and holding off full domination by solid state at lower power levels longer than expected.

Upward integration — Effort is progressing rather slowly. This field is getting mature, growth is limited, and future life span expected to exceed 20 years.

Displays

Displays larger than a few inches are still dominated by the cathode-ray tube (CRT). For many years after its invention at the turn of the century, the CRT with its faintly glowing green willemite screen was used in many instrumentation applications. Explosive growth followed when the high-voltage, high-vacuum bright CRT was developed for black-and-white television in the late thirties. The sales level rapidly climbed to one quarter of the whole tube business, and then, with the introduction of color tv and the shadow-mask tube, it continued to climb until it exceeded sales of all other tubes put together (excluding lamps).

Today we find the versatile CRT still dominant in color tv, black & white tv, projection tv, instrumentation, and information handling systems.

Phosphors for many applications — The phosphor screen represents a key element of the CRT. Today such a wide variety of phosphors are available that they fit the needs of almost any conceivable application (Fig. 9 and Ref. 7).

Colored television displays

The shadow-mask color picture tube which emerged as the winner among several competitive designs is used in all worldwide color television consumer systems and is by far the largest single contributor to tube sales. Focus grill and

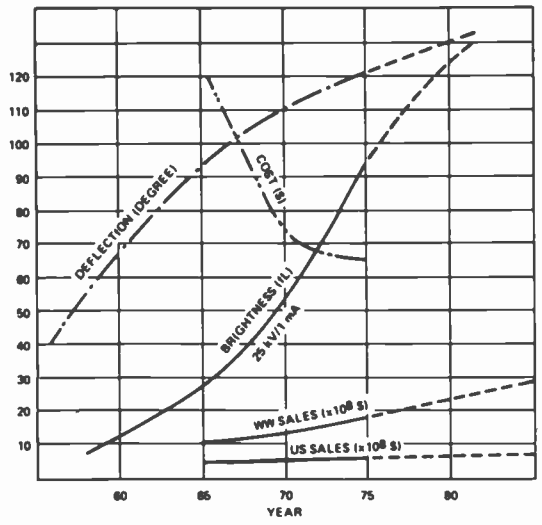

Fig. 10 — Progress of key parameters of shadow-mask color picture tubes.

Table III — Progress of elements for the shadow-mask color picture tube.

Element	1955-65 *Status*	1965-75 *Status*	*Possible Future*
Cathode	Oxide ($1^A/cm^2$)	Oxide ($1^A/cm^2$)	Dispenser or cold cathode
Gun	Crossover type	Crossover type	Laminar flow
Focus	12 convergence adjustments	Precision-in-line No adjustments	Precision-in-line No adjustments
Envelope	Metal	Glass/Glass Frit	Flat panel
Mask	Hole	Slots	Focus mask, and no mask (beam index)
Screen	All phosphor grey glass	Pos and Neg black matrix	Negative Black matrix
Phosphor	Light phosphor	Rare-earth phosphor	Dark phosphor

mesh tubes, indexing tubes, and penetration tubes have been evaluated and continue being pursued in laboratories around the world, with different degrees of activity, because of their competitive potential.

The key targets for improvement effort are: brightness, sharpness, color fidelity, cost, fast turn-on, and size of the display package. Although the shadow-mask tube was invented twenty-five years ago, improvement of its performance has steadily continued and every time a potential competitive solution shows promise it finds a "leaner, tougher" shadow-mask competitor which has so far weathered all attacks.

Fig. 10 and Table III show the progress of key elements and parameters with time. All indications point to continuing improvements in the shadow-mask technology. Once a brightness level is achieved which requires no further increases, trade-offs with other characteristics will continue to strengthen the tubes competitive stature. Any other system, to replace this tube in a well facilitated industry, would have to provide many outstanding advantages.

The ideal flat-panel display has been a dream since the inception of television. Today, various research laboratories are pursuing a multitude of appraoches to achieve such an end result. How does one approximate the ideal CRT, the tube with a cold cathode, 180° deflection, and substantially larger size at reasonable weight and still providing the same cost-effective performance? Flat-panel displays represent one of the most exciting areas of activity and will keep many tube engineers around the world busy for many years. General estimates indicate that introduction of a flat panel for consumer use will not occur before about 1990.

No review of consumer television is complete without mention of the potential viewing sensation of life-size television. Moderately priced projection-type display systems with about 4 by 6 foot screen size are now reaching the commercial market, and the next few years will determine the degree of consumer penetration by such systems which utilize one or several CRT type tubes.

Summary of Displays

Beam addressed color phosphors continue as the dominant large display technology. Small displays are solid-state dominated.

Upgrading — Because of the large market size and very competitive situation, product improvement continues very actively.

Upward integration — Mostly CRT-yoke packages - others limited to date.

The electron-tube display technology is expected to continue dominant for at least the next 15 years.

Outlook and conclusions

Conclusions

Today, the tube business continues as a very strong sector of electronics. Product entrenchment, special (unique) characteristics, product upgrading, and upward integration provide the impetus for long product life.

Fig. 11 goes back to the family tree to indicate what inroads solid state is likely to make on tubes in the next 10 years. It is not a frightening picture to the tube engineer. While we have dwelled considerably on the competitive standing between tubes and solid state it should also be pointed out that solid state is now

making new products cost effective for consumer applicaitons which in turn also provide increased usage of tubes for special purposes.

The word "electron tube" may soon represent an inadequate description of the products of the tube industry now getting hybridized and upward integrated beyond recognition of the "tube bottle". However, this action portends continuing business viability past the turn of the century.

Implications to the working engineer

Opportunities — The conventional electron tube scope will be substantially enlarged through:

- Continued exploitation of the tube's special characteristics.
- Hybridization - a partial move into solid state.
- Upward Integration - in some cases right up to end-user-proudct.
- New Product Areas - such as energy generation.
- Utilization of entrenchment and hybridization to move into new more competitive technologies.

Needs — The major needs of the working engineer include:

- A working knowledge of solid-state technology for creative product development.
- An understanding of both business and technical objectives with proper perspective on the significance of cost.
- A fundamental understanding of what makes the technology function and ability to apply this to cost-effective solutions.

It is important for the working engineer developing new products to understand the special characteristics of electron tubes and use them where they are more cost effective rather than follow a solid-state only approach.

The electron-tube business with its challenges requires a continuing infusion of motivated engineering talent to provide the progress which market needs demand.

Outlook

We have observed earlier that for the last forty years, 70% of the electron tube business has been consumer oriented. Large as the future of industrial and commercial markets appear, consumer products with worldwide use constitute an enormous potential.

We are but in the early and fairly primitive stages of a home television oriented technology which will lead to systems far beyond the limited and modest entertainment services provided by today's television set. With some breakthroughs in product simplicity and cost, today's technology is capable of providing to the consumer in his home an almost unlimited scope of services (including but not limited to entertainment) which are becoming increasingly more inconvenient to obtain in the traditional manner. Such developments will provide, by the turn of the century, a consumer market for electronic hardware of awesome proportions in which the electron tube business and engineers will play a key role alongside their other electronics partners.

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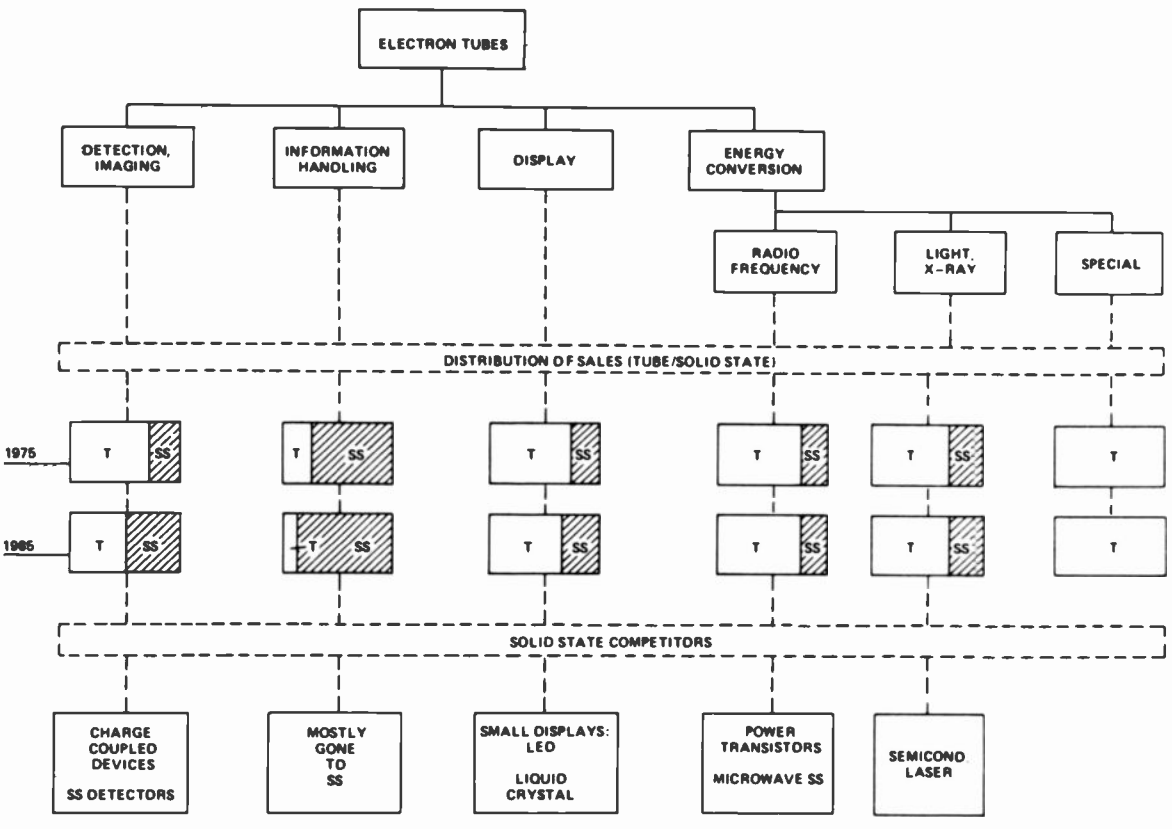

Fig. 11 — Inroads of solid-state devices on the sales of electron tubes.

Chroma processing using sample-and-hold techniques

L.A. Cochran| L.A. Harwood

The design of a second-generation, chroma-processing intergrated circuit is described together with its implementation into existing RCA solid-state modular color television receivers. Reasons for initiating this new design are discussed and a detailed explanation of the circuitry involved is presented. Performance characteristics of the first-and second-generation circuits are included.

IN 1970 RCA introduced the CTC-49 solid-state color television receiver which became the prototype of the XL-100 series. At the time the design of this receiver represented a departure from traditional circuitry and techniques used in consumer electronics. Due to new technical advances, the consumer was offered a receiver with improved performance, higher reliability, and easier maintainence. The receiver was partitioned into functional blocks constructed on easily replaceable modules. A major part of the signal processing was performed by custom-designed integrated circuits; their use resulted in a substantial reduction of discrete components thereby improving reliability and reducing cost. The design of this receiver, including modules and integrated circuits, is described in detail in a special issue of the *RCA Engineer*, Vol. 16, No. 5, Feb.-March 1971.

Larry A. Cochran joined RCA as a summer employee in June 1962. He received his BSEE in January of 1963 and his MSEE in June of 1968 from Purdue University. Since joining RCA, Mr. Cochran has worked in many areas of signal processing as a member of the color television product design group. He has been responsible for the design and development of new color synchronizing circuits, demodulation systems, and many other aspects of color signal processing. From 1968 to 1971, Mr. Cochran was associated with the utilization of silicon integrated circuit technology in the design of chroma processing circuitry. From 1971 to 1973, he was a leader in the advanced product development section of color television engineering. Since 1973, he has been a senior member of the engineering staff, responsible for the design and coordination of new signal processing circuits. He is a registered professional engineer, and a member of Eta Kappa Nu and Tau Beta Pi. He has five issued patents plus patents pending.

Chroma processing advances

The purpose of this paper is to describe further improvements in the area of chroma processing. A new module and integrated circuit were designed to perform the same basic functions as the original circuit with emphasis on utilizing all the information available in the signal so as to approach ultimate system performance capability, while at the same time substantially reducing the number of external components and adjustments.

As contrasted with commonly used IC designs, sample-and-hold techniques are used in the phase detectors for the automatic frequency and phase control (AFPC) and the automatic chroma control (ACC) killer loops. The improved signal-to-dc unbalance attained makes it possible to eliminate the adjustments conventionally used in those circuits. The only setup adjustment is a trimmer capacitor to tune the crystal filter.

The integrated circuit which performs the major functions is 73-mils square and is housed in a 16-terminal package. The external components required to make the circuit functional are shown with the integrated circuit in Fig. 1.

Major IC functions

The signal flow and organization of the integrated circuit are shown in block form in Fig. 2. The composite chroma signal is applied to the first chroma amplifier. The output from this stage proceeds along three paths. The first path leads to the doubly-balanced wideband AFPC detector. Here the burst signal is compared with the reference carrier to produce the required error signal for synchronization. Two sample-and-hold circuits achieve high-detection efficiency and bias stability. One sample-and-hold circuit samples the detected signal during the horizontal keying interval and stores the peak error signal in a filter capacitor. A second similar circuit provides an accurate reference potential as described later. The bias stability of this system is sufficient to eliminate the need for adjustments required in conventional circuit design.

The detected and filtered burst signal controls the frequency and phase of a voltage-controlled oscillator (VCO) by operating on an electronic phase-shifter. The VCO consists of an amplifier-limiter followed by the electronic phase-shifter. A crystal filter located betweeen the output of the phase-shifter and the input of the amplifier-limiter closes the loop of the VCO. The filtered oscillator signal is amplified to produce the required reference carriers for the AFPC and ACC synchronous detectors. The required quadrature relationship is obtained by $+\pi/4$ and $-/4$ radian integrated phase shift networks.

The ACC-killer detector is similar in structure to the AFPC detector, and is also driven from the first chroma-

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amplifier stage. It detects synchronously the in-phase component of the burst signal and produces a pulse signal proportional in amplitude to the level of the burst signal. The resulting control signal passes through a sampling circuit, as described above, and is applied to the killer and ACC amplifiers. The action of both amplifiers is delayed so that the unkill action takes place prior to ACC and the latter is fully activated upon reaching the predetermined burst level. The ACC amplifier controls the gain of the first chroma amplifier so as to maintain the burst-signal constant, while the killer amplifier enables the output stage in the presence of the burst signal.

The signal level to the second chroma amplifier is reduced to one-fourth of the available signal level to allow for the extremes of the chroma-signal excursions. A horizontal rate keyer operating on this stage removes the burst signal so that the output stage is *on* only during the horizontal scanning interval. A saturation control, available for front panel control, allows a continuous gain adjustment of this amplifier. A desirable feature of the saturation control is the linear correspondence between the control bias and the chroma output signal. The chroma minimum and maximum levels correspond to the minimum and maximum bias potentials respectively, without dead spots at the extreme of the control range. A threshold-type overload detector monitors the output signal and maintains the output from the second chroma amplifier below an arbitrarily set level. This prevents the overload of the picture tube usually experienced on noisy or excessively large chroma signals. The required keying signals for the vairous functions are generated by two cascaded keyer stages where either polarity pulses are generated.

Glossary

AFPC — A circuit which controls the frequency and phase of a source of oscillations by comparing them with oscillations of a reference signal and supplying correction voltage to the controlled source.

Burst Signal — That portion of the composite color signal, comprising a few cycles of sinewave of chrominance subcarrier frequency, which is used to establish a reference for demodulating the chrominance signal.

Reference Carrier — A continuous signal having the same frequency as the chrominance subcarrier and having fixed phase with respect to the color burst. This is the reference signal with which the phase of the carrier chrominance signal is compared for the purpose of modulation of demodulation.

ACC — A circuit which controls the amplitude of the chrominance signal by sensing the burst amplitude and applying a correction voltage to a gain-controlled chrominance amplifier.

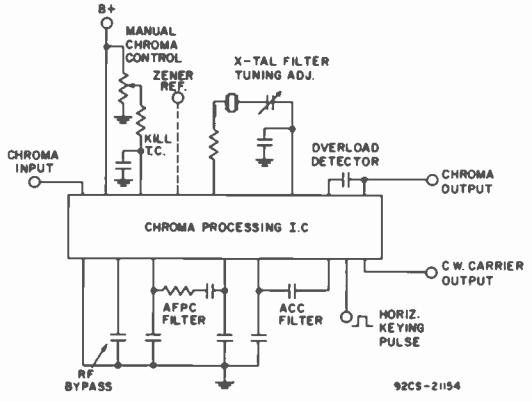

Fig. 1 — Components external to the IC.

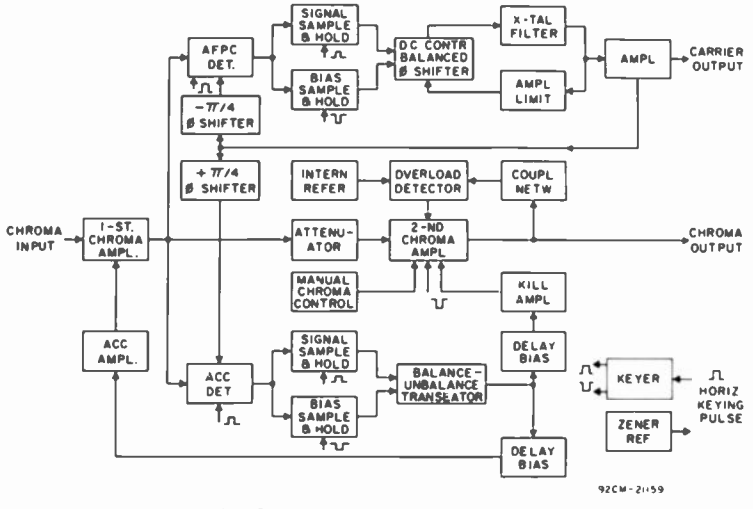

Fig. 2 — Signal flow and organization of the IC.

Regeneration of the subcarrier

The regeneration of the subcarraier is performed by the circuit shown in Fig. 3. The regeneration section consists of a synchronous phase detector, the sample-and-hold circuits, and a voltage-controlled oscillator. Several keying circuits serve to maintain the operation in proper time sequence.

The phase detector — The phase detector is formed by transistors Q1 to Q8. The composite chroma signal amplified by the first chroma amplifier is applied to

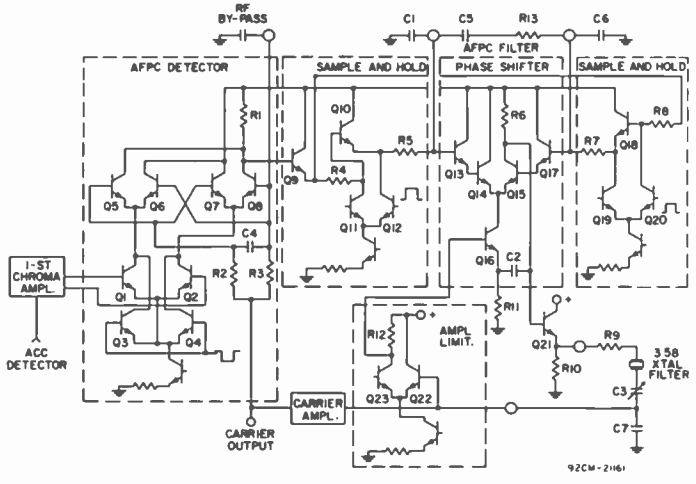

Fig. 3 — Subcarrier regeneration circuit.

transistors Q1 and Q2 and the reference carrier is applied to transistors Q5 and Q7. The product of the two signals is developed across the load resistor R1. Transistors Q3 and Q4, triggered by a horizontal rate keyer circuit, operate on the phase detector so as to allow detection of the burst signal only. The current compensation of transistors Q1 and Q2 by the gating transistors Q3 and Q4, and the absence of filtering at the output of the detector results in transient-free switching of the phase detector.

In the absence of chrominance, the potential across the load resistor R1 remains constant regardless of the keying. In the presence of the chrominance signal, the phase detector produces two time-spaced outputs: one during the horizontal scanning interval corresponding to the quiescent potential, the second during the horizontal keying interval representing the detected burst. Thus, the detected burst can be measured relative to the quiescent potential rather than to an arbitrary reference. This results in excellent stability for temperature and supply variations.

Sample-and-hold circuits — As previously stated, the sample-and-hold circuits shown in Fig. 3 allow efficient utilization of the detected error signal and provide a reliable reference potential. During the sampling interval, the detected pulse signal available at the detector load resistor R1 is translated to the filter capacitor C1 via transistors Q9 and Q10. Q9 serves to isolate the detector from the switching pulses generated in the sampling circuits. The sample-and-hold action is accomplished by controlling the conduction current in transistor Q10, thus alternating the charge path during those intervals. During the sampling interval, transistor Q10 conducts and its emitter exhibits a relatively low impedance in comparison with the value of the charging resistor R5. The detected signal is stored in the filter capacitor C1 — and the R5 × C1 product is the filter time constant during this time interval. During the hold period, transistor Q10 is *off* and the filter time constant is several orders of magnitude larger than previously. The discharge of the filter capacitor is reduced to very small base bias currents and little of the stored information is lost.

The *on* and *off* condition of the transistor Q10 is determined by the state of the transistor-pair Q11 and Q12. During the *on* (sampling) interval, a signal from the horizontal rate keyer disables transistor Q11 and the collector current of the transistor Q12 maintains the transistor Q10 in the *on* condition. During the *off* (hold) period, transistors Q11 and Q12 change their states and the transistor Q10 is *off*.

The bias sample-and-hold circuit, similar in structure to the above-described circuit, consists of the sampling switch Q18 and the transistor pair Q19 and Q20. The sample-and-hold circuit, also activated by a signal from a horizontal rate keyer, samples the quiescent potential of the phase detector. The two signals, the error and the bias, processed by the sampling circuits, are stored in filter capacitors, and are applied to opposite terminals of a differential phase control. The phase-control circuit synchronizes the reference carrier produced by the VCO.

Depending on the free-running frequency of the VCO, the detected signal is in the form of positive-or negative-going pulse trains which are then stored in a filter capacitor. The sampling switch has equal drive capabilities for both polarities of the signal: a requirement of particular importance in the presence of noise signals. Non-linear operation of the detector and sampling circuit would produce a rectified dc component causing an erroneous detuning of the VCO.

The VCO loop — The amplification and amplitude limiting of the oscillator signal takes place in the amplifier-limiter formed by the transistor pair Q22 and Q23. The output from Q23 is fed to the dc controlled phase-shifter and returns to the amplifier through a crystal filter. The amplifier operates in a non-inverting mode, hence, the total phase shift through the phase-shifter plus crystal filter must be a mulitple of 2 π radians. The crystal filter is tuned to the subcarrier frequency and the filter bandwidth is determined by a resistor in series with the crystal. The dc-controlled phase-shifter has a phase range of approximately $\pm \pi/4$ radians; and, a phase change activated by a control signal results in a corresponding oscillator frequency change.

In the phase-shifter, the oscillator signal available at the collector of Q23 is applied to the base of Q16 from which it proceeds along two paths. An integrated capacitor C2 couples this signal from the emitter of Q16 to the collector load of Q15; at this point, the signal is phase-shifted by approximately $\pi/4$ radians. In the second path, the signal arriving at the collector of Q15 passes through a current splitter formed by the transistor pair Q14, Q15; at this point, the signal is reduced to a level determined by the control voltage at the bases of transistors Q14 and Q15. At one extreme, transistor Q15 is *off* and the signal at the collector of Q15 arrives through the capacitor C2 only. Conversely, with transistor Q15 *on*, and Q14 *off*, the signal arriving through the transistor Q15 is phase-oriented so that the resultant signal has a phase of $3\pi/4$ radians. Phase-control is linear throughout most of the control range.

A buffer amplifier supplies the CW carrier required for the demodulators, and the carrier is available at a pin terminal. Internally, the buffer amplifier supplies the two synchronous detectors. Two R-C phase shifters fed from the buffer amplifier provide the required

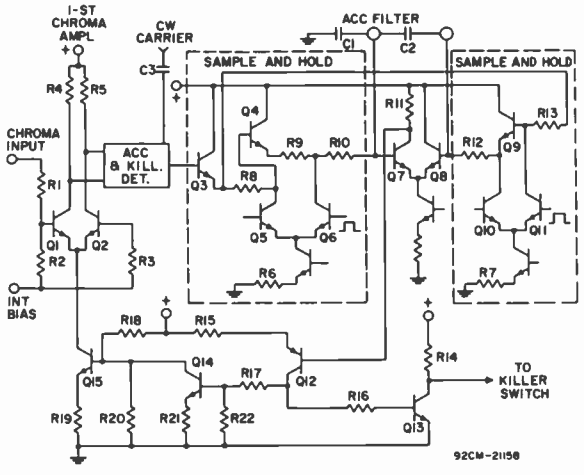

Fig. 4 — The first chroma amplifier and the ACC servo loop.

phase orientation. A low pass R2-C4 filter shifts the carrier to the AFPC detector by $-\pi/4$ while a high-pass filter provides a $+\pi/4$-oriented carrier for the ACC-killer detector.

Amplitude control of the chrominance signal

Two cascaded amplifier stages process the chroma signal and several signals are developed to control the gain of each stage.

First chroma amplifier and ACC servo loop — The first chroma amplifier, shown in Fig. 4 is controlled by the burst responsive ACC-killer detector only. The amplifier formed by the transistor pair Q1, Q2 is driven single-ended by the applied composite chroma signal. The amplified output from this stage drives the synchronous ACC-killer detector differentially. The gain of the first amplifier is a function of the dc emitter current supplied by the constant current source Q15; this current source is biased to provide a nominal gain in the first amplifier stage. The bias of the current source is reduced in response to a detected burst signal and the gain of the first stage diminishes correspondingly.

The ACC-killer detector is identical in structure to the AFPC detector. However, the CW carrier applied to the detector is in phase with the burst signal. The detected burst signal is processed by a sampling circuit in the same manner as previously described in the AFPC circuit. The signal sampling consists of the transistor-follower Q4 and the keyed-transistor pair Q5, Q6. Resistor R9 produces an intentional dc offset across the inputs of the differential pair Q7, Q8.

The bias-sampling circuit (consisting of transistors Q9,Q10,Q11) applies the quiescent bias to the base of transistor Q8. In the absence of a burst signal, the dc offset maintains transistor Q7 in the *off* condition and the following PNP transistor, Q12, is also disabled. Thus, the ACC amplifier Q14 is non-conducting and the current source Q15 provides the maximum current to the input stage.

The *off* state of transistor Q12 renders the killer amplifier (transistor Q13) inoperative, a condition required to disable the second chroma stage.

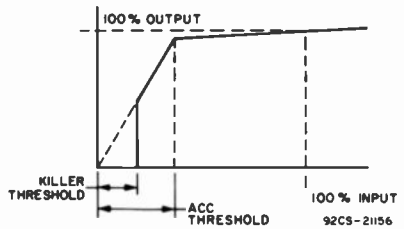

Fig. 5 — Normalized ACC characteristic.

Upon amplification of the burst signal in the first chroma amplifier, the detected burst signal increases proportionately to the amplitude of the input signal and combines differentially with the previously described bias signal in the collector load of transistor Q7. Prior to it, the detected and bias signals are smoothed by filter capacitors C1 and C2. Linear operation of the chroma amplifier, the detector, and the amplifier following the sampling circuit is maintained at a signal level sufficient to enable the transistor Q14. A potential of approximately 0.7V establishes the delay of the ACC characteristic, as shown in Fig. 5. The chroma (burst) signal at the output of the first stage remains essentially constant with further increase of input signal. The increasing dc potential at collector of Q12 also activates the killer-amplifier Q13. To maintain a predictable killer threshold, the amplifier action is referenced to the delay point of the ACC. As previously stated, the ACC begins to function at a signal where the dc potential across resistor R22 reaches 0.7V. The killer threshold starts prior to the ACC action and is determined by the drop across resistors R17 and R22. Thus, the two threshold signals are predictably established by the ratio of R22/CR17+R22.

The second chroma amplifier — The operation of the second chroma amplifier is controlled simultaneously by several signals. As described previously, they are: a customer-operated gain (saturation) control, the killer detector signal, the overload detector, and the keyer.

The amplifier circuit of Fig. 6 is formed by the transistor pair Q1, Q2 and is driven differentially by the first chroma amplifier. The signal level to this stage is reduced by means of a resistive voltage divider. The amplifier Q1, Q2 is interrupted during the horizontal keying interval by the transistor pair Q3, Q4 to remove the burst information from the composite signal. The gating transistors Q3 and Q4 are connected so that their emitters and collectors are in parallel with the respective emitters and collectors of transistors Q1 and Q2. The resulting collector current compensation maintains the quiescent output potential regardless of the keying operation.

The gain of the second chroma amplifier is adjusted by varying the current in the transistor Q8. A resistive divider (R5, R6) fed from a follower-stage Q9 provides the bias potential to the base of the transistor Q8; thus, the voltage drop across resistor R4 determines the current flowing from the collector of Q8 to the emitters of Q1 and Q2. The diode D1 compensates the base-to-emitter potential of the transistor Q8.

Since bias resistors R5, R6, R4, and amplifier load resistor R1, are all located on the same IC chip, the resistance ratio of these components is accurately controlled. Thus, the gain of the second chroma amplifier determined by these components is very predictable, and becomes a function of the bias potential applied to the base of transistor Q9 only.

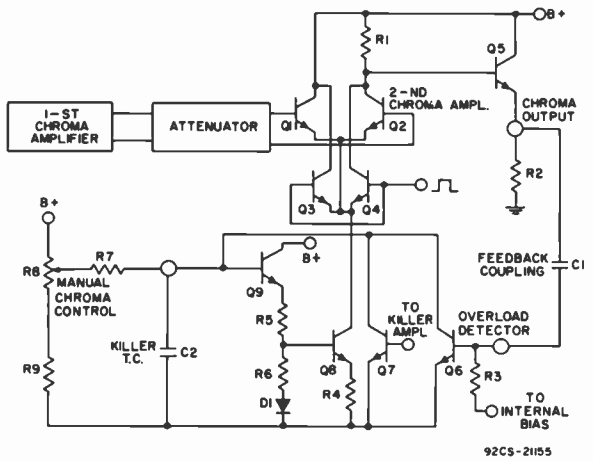

Fig. 6 — Chroma output stage.

Interfacing IC's with external control circuits usually presents problems due to the large tolerances associated with both components. The circuit used here overcomes these difficulties. Transistor follower Q9 exhibits negligible loading on the bias setting potentiometer R8. Thus, the gain of the second chroma amplifier is uniqely determined by the rotation of the control potentiometer and is relatively independent of its resistance value.

The killer operation is also performed on the second chroma amplifier. The amplifier output from the ACC-killer detector is applied to the killer switch Q7. In the presence of a burst signal, transistor Q7 is *off* and the chroma amplifier remains undisturbed. In the absence of a burst signal, the collector current in Q7 reduces the potential on the base of the transistor Q9 so as to cut off the second chroma amplifier.

The overload detector — The ACC and the manually operated saturation controls provide the essential means to maintain the proper chrominance level to the picture tube. Under certain conditions, however, the presence of the ACC is detrimental. As previously stated, the ACC servo loop maintains a constant output level of the burst signal regardless of the chroma information. Transmitter variations in burst-to-chroma ratios are improperly corrected by the ACC action and, on signals with low burst-to-chroma ratios, the excessively amplified chroma can exceed the dynamic range of the picture tube.

Similar overload problems are experienced when receiving weak signals. The synchronous ACC detector produces a control signal proportional to the average value of the burst-interval signal, and noise does not contribute to the output. Although this type of noise-immune detection is necessary for reliable operation of the killer circuits, it is less desirable for the ACC action because the noise-peaks plus signal tend to produce undesirable over-saturation effects.

Therefore, the overload detector operating on the second chroma stage is designed to eliminate both these overload problems. The chroma signal from the output terminal of the second chroma amplifier is coupled, by means of the coupling capacitor C1 to overload detector Q6. Transistor Q6 is biased by means of an internal bias supply to 0.5V, and remains *off* until its base potential is raised to approximatley 0.7. Thus, detection takes place whenever chroma signal plus dc bias equals or exceeds 0.7V. The detected and filtered signal lowers the bias potential on the base of transistor Q9 and reduces the gain of the output stage.

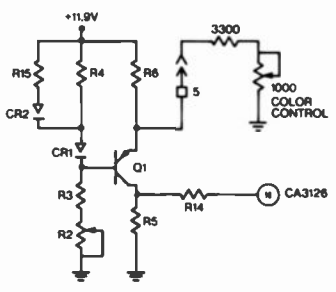

Fig. 8 — Signal servo loop and manual color control.

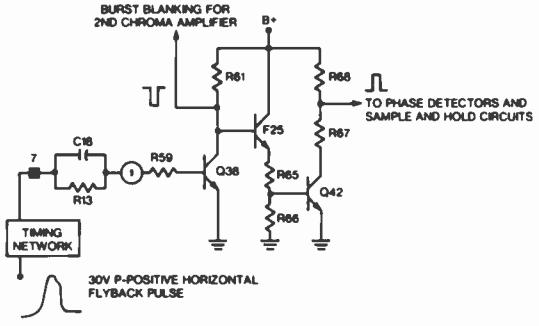

Fig. 9 — Circuit for generating gating pulses for burst blanking of second chroma amplifier.

Module design

Basic design philosophy followed by RCA since the introduction of the XL-100 solid state modular chassis has been to avoid introduction of new modules which do not retrofit previous designs — until such time as new-generation chassis are introduced. This philosophy was adhered to in the design of the MAC002B chroma-I module; the latter has, as its basic building block, the CA3126 monolithic integrated circuit. Operation of the CA3126 in the simplest manner was shown in Fig. 1. Utilizing the CA3126 in a modular design to retrofit previous XL-100 chassis required certain compromises in ultimate cost and simplicity; however, even in its retrofit form a significant improvement in performance and simplicity was realized.

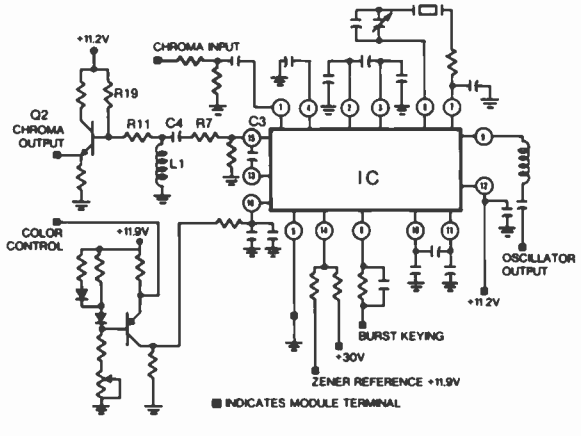

Fig. 7 — The CA3126 shown in relation to other circuitry.

First chroma amplifier and ACC circuit

A chroma input signal (applied to modules terminal 3) has been frequency contoured to compensate for the slope of the i.f. in the chroma region. Fig. 7 shows the CA3126 as used in the retrofit modular design. As described previously, the input amplifier is gain controlled via the ACC sample-and-hold detector circuits. The chroma signal is fed differentially to the output amplifier (Q25, F16, Q24); the output is gain controlled by a second servo loop that senses signal information.

Second chroma amplifier and color control

The second chroma amplifier is gain controlled (via terminal 16 of the IC) by both the signal servo-loop and the manual color control (see Fig. 8). Q1 and associated components comprise a non-inverting dc translator interfacing the CA3126 color control requirements with those provided by existing XL-100 solid state chassis. The circuit consisting of R4, CR1, R15, and CR2 provides V_{BE} temperature compensation for Q1.

Variable resistor R2, one of the two setup adjustments required for this module, compensates for tolerances in the DC translator.

The signal servo loop is closed via C3. Both the loop gain and the threshold of this circuit can be controlled external to the integrated circuit; thus, the option of utilizing the circuit for noise protection only is provided.

The chroma output signal is coupled from pin 15 of the integrated circuit through the high-pass filter consisting of L1, C4, R7, R11, and R19. The purposes of this filter are to provide rejection to frequencies below the chroma passband and to provide additional frequency contouring within the chroma passband for achieving a symmetrical amplitude and phase response. Voltage divider R11 and R19 provides the correct signal for driving the color demodulators. Due to the presence of an external horizontal blanking circuit on module pin 6, it was necessary to add transistor Q2 for providing a low-driving-source impedance.

Gating pulse circuits

Generation of gating pulses required for burst blanking of the second chroma amplifier and setup of the sample-and-hold circuits is shown in Fig. 9. A positive horizontal flyback pulse is applied to timing network external to the module. The design of this timing circuit was such as to match the flyback pulse characteristic shape to the input impedance of the original XL-100 chroma module in a manner providing the correct burst gating. A retrofit problem existed in that several different timing circuits were in use. The problem was solved by using R13 and C18 to allow Q38 to clamp on the peak of the horizontal gating pulse. This clamp action reduced gating-pulse width variations which can occur with high voltage Q38 beta variations.

Oscillator, AFPC, and ACC detectors

The use of an AFPC controlled 3.58-MHz oscillator in conjunction with sample-and-hold detectors provides a high-performance, noise-immune subcarrier regeneration system. Internal monolithic phasing elements provide both the required 90° offset between the AFPC and killer-ACC detectors and the voltage-controlled phase shift needed for the VCO. A block diagram of the subcarrier regeneration system along with the required external components is shown in Fig. 10. Capacitors C8 and C9 are the hold capacitors associated respectively with the *signal* sample-and-hold circuit and the *bias* sample-and-hold circuit. Capacitor C16 in conjunction with resistor R1 provides the low-frequency phase compensation needed to prevent hunting. The oscillator loop is closed through the circuit consisting of R18, C12, C11, and the crystal. Capacitor C12 in conjunction with R18 provides the additional phaseshift needed in the oscillator loop to obtain a symmetrical pull-in range. A one-volt peak-to-peak oscillator signal is coupled to the module output terminal through coil L2 needed to restore correct subcarrier phase.

The sample-and-hold detectors associated with the ACC-killer function are very similar to those used in the AFPC loop. The hold capacitors associated with these detectors are C6 and C7. Capacitor C5 prevents vertical rate distortion from occurring due to loss of burst during a portion of the vertical retrace interval.

Summary

The development of the CA3126 chroma-processing integrated circuit and its subsequent implementation into the XL-100 chassis has been the result of a joint effort by the Consumer Electronics and Solid State Divisions of RCA. A significant improvement in performance and manufacturability has been achieved while realizing a cost reduction. The use of synchronous detection and sampling techniques resulted in excellent signal stability, fewer external components, and fewer factory adjustments. Table I shows a comparison of some of the important characteristics of the first generation MAC002A chroma processing circuit and the MAC002B chroma processor using the CA3126 integrated circuit.

Acknowledgments

The authors acknowledge the contributions of E.J. Wittmann (Consumer Electronics Division — Somerville) who participated in the design of the I.C., W.A. Lagoni (Consumer Electronics Division — Indianapolis) who participated in the development and testing of the module, and W. Austin and L. Teslenko (Solid State Division) who participated in the device development.

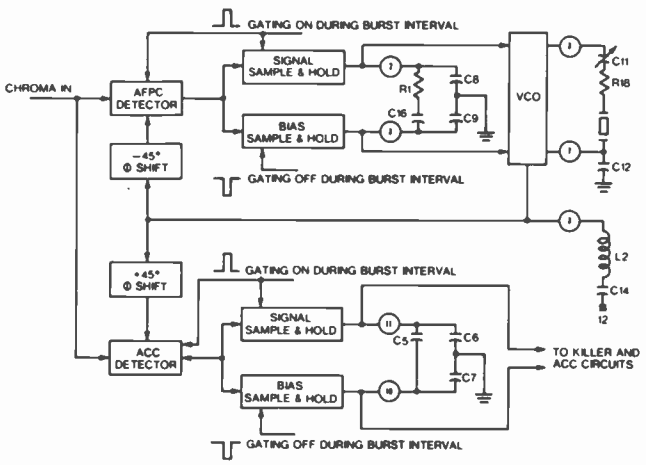

Fig. 10 — Block diagram of subcarrier regeneration system.

Table I — First-generation chroma processing compared with the CA3126 integrated circuit version.

Item	*First Generation chroma* (MAC002A)	*Second Generation chroma* (MAC002B)
Total factory adjustments	7	2
Adjustable coils	2	0
Adjustable resistors	3	1
ACC performamce		
Output @20% chroma input	88%	98%
Output @ 20% burst input	330%	110%
Kill level	8%	4%
Oscillator performance		
Static phase error	20°/100Hz	4°/100Hz
Pull-in range	± 300Hz	± 500Hz
Chroma output variation from 8 to 11 cycles of burst	20%	1%
Chroma output tolerance	±40%	±15%

Microwave data bus technology

E. W. Richter

Information and control requirements are rapidly increasing for sophisticated self-contained systems, such as aircraft, spacecraft, ships, or building complexes. Microwave technology offers the advantages of broad bandwidth and ease of systems configuration that are conducive to the attainment of the more effective data buses. The 19- to 23-GHz microwave frequency band is particularly suited to self-contained systems because of the sparsity of radiating systems in this microwave region — and because it affords adequate bandwidths. In addition, the small size components assure a compact system that utilizes a mature technology. Various system configurations and competing transmission lines and devices are evaluated and described herein.

Ed W. Richter, Engineering Scientist, Government Communications and Automated Systems Division, Burlington, received a BS in Physics from Queens College in 1943 and pursued graduate studies at New York University and Boston University. Since joining RCA in 1962, he has been designing microwave portions of the MTE and LM test equipment systems. His component contributions were in the design of octave bandwidth devices such as couplers, mixers, single sideband generators, precision attenuators and most recently harmonic generators providing five or ten times frequency multiplication. Some of these devices have been combined to provide the extension of synthesized frequencies necessary for microwave ATE stimulus. Other combinations provide integral microwave measurement capabilities that are directed to the requirements of radar and communications systems. Mr. Richter's current activity is directed toward analysis of the test requirements of modern microwave radar and communications systems, and toward development of automatic test equipment to satisfy these requirements. Recently developed miniaturized, precision, solid state or integrated devices are all investigated to provide economically and technically feasible designs of appropriately versatile, accurate and reliable automatic microwave test systems. Mr. Richter is a member of Sigma XI and the IEEE and is a past chairman of the Microwave Theory and Techniques Group of the Boston Section of the IEEE. He is a registered professional engineer in the Commonwealth of Massachusetts and is the author of several papers on microwave topics.

THE DEMANDS for data-handling arrangements to support major, self-contained aircraft systems, space vehicles, ships or building complexes are continuously increasing. Such major, complex systems are becoming more commonplace, since a high degree of complexity is now technically feasible. It is often necessary to change the complement of equipment in existing systems, as management and mission requirements change, to meet new and developing system utilization goals.

Advantage of microwave technology

All the above needs are occurring in a time of financial constraint that makes both economy and the ability to change configurations mandatory. To accommodate such change, the unique value of microwave implementation satisfies the following combination of urgent requirements:

- A mature technology,
- Wide bandwidths are available,
- Economy associated with a single data bus,
- Low weight associated with a single data bus,
- Economy for modification, and the
- Ability to operate under the most severe environments.

System data-handling requirements

Data transfer requirements of a modern military aircraft have been analyzed,[1] as typical of self-contained systems. Equipment is located in several discrete

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locations and data must be communicated to several others. Typical data rates for several different system functions are:

Function	*Data rate*
Radars	80 Mbps
Displays	20-80 Mbps
Electro-optics	200 Mbps
Countermeasures	200-500 Mbps

Fig. 1 typifies the physical dimensions and data rates required for a military aircraft installation. The maximum bandwidth requirements are approximately 4 GHz; thus, bands above 4 GHz must be used. The 4 to 18 GHz region is well suited to transmission through the atmosphere and has led to the current plethora of systems in this region. The existence of the water vapor absorption centered at 22.3 CHz has led to an avoidance of this spectral region. Thus, use of the 19- to -23 GHz region establishes and environment of reduced possibility of mutual interference between the data bus and the system it serves.

Transmission lines

Various known transmission lines are compared here for low leakage, low loss, freedom from resonant absorptions, low dispersion, small size, light weight, stability, ease of coupling, convenience of adaptation to existing system structures, and moderate cost.

The most competitive transmission lines are:

1) Coaxial line (TEM mode),
2) Flexible waveguide (TE_{01} mode),
3) Rectangular waveguide (TE_{01} mode),
4) Elliptical waveguide (TE_{01} mode),
5) Oversized rectangular waveguide (TE_{01} mode),
6) Oversized elliptical waveguide (TE_{01} mode), and
7) Oversized rectangular waveguide (TE_{10} mode).

The transmission lines above are listed approximately in order of decreasing attenuation coefficient. The flexible waveguide and the elliptical guide (not oversized) may be considered as minor variations of the rectangular guide.

The best of the coaxial transmission lines tested is a semi-rigid line having a 0.141 inch outer diameter; the next best is similar to RG-142B/U. The modification

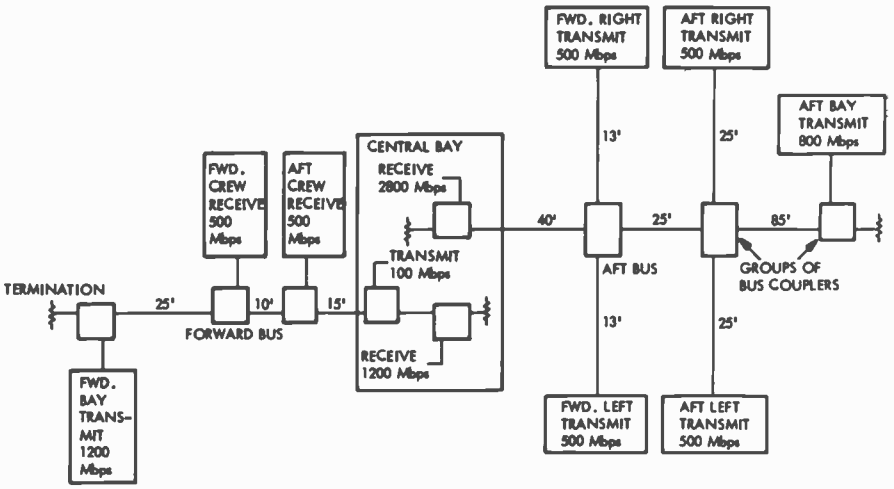

Fig. 1 — Bandwidth requirements for aircraft microwave data-bus, wideband signals.

(SF-142B) consists of the inner shield of the outer conductor being composed of a braid of flat strips of silver plated metal. The measured 22 GHz performances and weights of several transmission lines are tabulated below:

Coaxial Line	dB/100 ft	lbs/100 ft
SF-142B	72.0	3.8
UT-141A	55.0	3.2
Rectangular Guide TE_{01} mode		
RG-121 U	13.9	6.5
RG-351/U	8.0	8.4
Oversized Rectangular Guide TE_{01} mode		
RG-349/U	5.7	9.7
RG-347/U	4.9	15.0
RG-67/U	3.4	16.5
Oversized Elliptical Guide TE_{01} mode		
115-137	3.1	36.0
Oversized Rectangular Guide TE_{10} mode		
GR-106/U	2.1	68.0

All waveguides listed above are aluminum; the oversized guides are capable of propagating in several modes. Bends, twists and tapers to single-mode guides all result in absorption resonances. RG-351/U is the largest single-mode (TE_{01}) guide for the frequency band considered and is completely free of all absorption resonances below 23.1 GHz. Radius requriements for bends and length requirements for twists are kept to a minimum, and the RG-351/U can be used for the bus couplers as well as the bus line. It may be most economical to use RG-121/U for the *transmitting source* and *receive sink* modules because of the availability of existing component designs. Quarter wavelength transformers will suffice as transitions between these sizes.

Signal sources

A microwave signal source for data-bus use should be small, uncomplicated, and have modest power supply requirements. Output power is based upon system parameters — and the range of +10 to +20 dBm is useful. Two types of solid-state sources are viable candidates. They are Impatt/Avalanche or transferred electron oscillators (TEO); the TEO sources have the advantage of low power supply voltage.

A survey of available TEO sources indicates an output power variation of 2.8 to 18 mW per hundred dollars; the best ratio was achieved by a +20 dBm nominal output device. At 22 GHz, the pulling figure within the 1.5:1 VSWR load region was 12 MHz — and output power was 15 dBm ± 0.8 dB. VSWR loads up to 4:1 at all phases were tolerated with only minor degradation of performance. Mechanical tuning extends from 18.3 to 22.4 GHz and is approximately linear. Output power is greater than +13 dBm from 19.8 to 22.4 GHz. Bias voltage may be varied between 4.0 and 6.5 volts with only slight effects on output power and frequency.

Bus couplers

The bus-coupler task is to route a relatively broadband signal to or from a data-bus transmission line with a coupling that is both directional and reciprocal. The directionality conserves signal power by routing it only toward devices with which it must communicate. The reciprocity allows the development

of transponder modules that combine source (transmitter) and sink (receiver) functions.

Insertion loss should be small over the entire band of frequencies for the data bus; but, coupling should be optimized over a narrower band. The latter should be a band that is broad enough to handle the data requirements of each system — and be more narrow than the bandwidth of the data bus transmission line. These conditions make some frequency diversity possible.

Multiple bus lines, which are desirable to increase redundancy reliability, impose another requirement that the coupler with only small adaptation should be capable of coupling to more than one data-bus line simultaneously.

Ring-resonator directional filters have been modified in concept and developed to meet the data-bus requirements. Cohn and Coale[2] discuss the use of ring-shaped strip lines that are an integral number of wavelengths in circumference and coupled to each of two transmission lines. Such strip lines couple all of the signal at the resonant frequency of the ring from the input line. Tischer[1] describes the properties of waveguide ring resonators coupled to a single line and also describes a tuning technique using a waveguide width variation readily achieved by adjusting one half of the circular ring relative to the other. Resonances occur at wavelengths:

$$\lambda_R = [(N^2/L^2) + (1/4\ A^2)]^{-1/2}$$

where: N is the integral number of wavelengths in the ring, L is the mean circumference of the ring, and A is the width of the guide in the ring.

Jaumann[4] extended the concept by adding an output guide so that the device achieves directional filter status. His input and output guides were U-shaped; each guide was coupled to a ring structure by an array of apertures through the sidewall and extending over one half the circumference of the ring. Two rings were coupled with a similar array of apertures extending over the remaining half circumference. The width of the ring waveguides was adjustable to allow alignment of the resonant frequency of each ring. This adjustment results in a movement in the relative positions of the waveguide connection flanges.

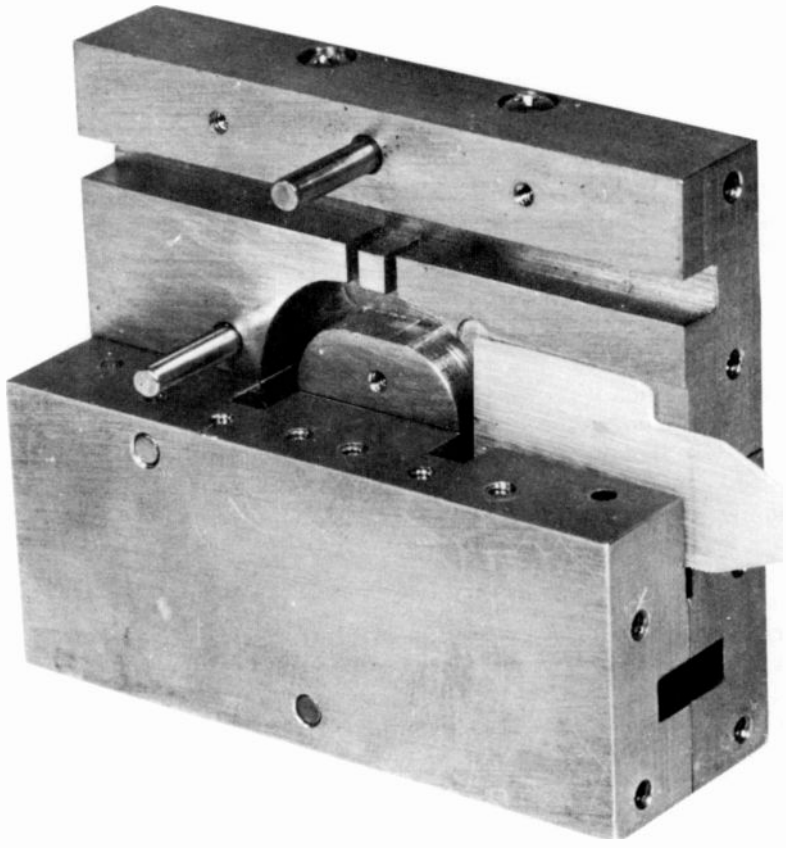

Fig. 2 — Tunable ring-coupled bus coupler.

Ohtomo and Shimada[5] developed the design further and produced conveniently tunable directional filters. One single ring filter had a bandwidth of 240 MHz at 46.5 GHz — and a double-ring filter had a 440 MHz bandwidth. Topwall coupling as well as sidewall coupling has been used. In the case of topwall coupling, the variation of the width of the guide in the rings could not be used for tuning; instead a dielectric rod was gruadually introduced.

The current approach abandons the U shaped input and output guide structures in favor of straight guides more suitable for insertion in a bus line. The exact circular shape of the ring circuit is also discarded in favor of a race-track shaped ring (the straight portions accommodate the coupling structure).

Recognizing that the highest Q portion of the filter is the ring resonator, coupling sections have been simplified to the use of branched guide couplers. Branched coupling is sufficiently constant even when tunable ring couplers are used.

Fig. 2 shows a partially assembled coupler in which tuning is accomplished by a dielectric vane introduced in the center plane of the guide where fields are maximum and wall currents are approximately zero. The test model used a four-wavelength ring with competing resonances outside the band at 18.9 and 25.4 GHz.

The tuning range of the model is 360 MHz centered about 22 GHz; the coupling of each of the directional-coupler slot pairs is 9.6 ± 0.4 dB. The 3dB bandwidth is virtually constant, varying from 120 MHz at one end of the tuning range to 125 MHz at the other. When a small vane of resistively metallized dielectric is introduced, the loss in the ring is varied. Ring attenuations (varying from 0 to 3.3 dB) result in a broadening of the bandwidth and a reduction of the main-line insertion loss, as shown in Fig. 3 and 4. The reduction in main-line insertion loss is important for data-bus couplers because it retains adequate signal in the main line in any coupled band to allow for subsequent additional coupling within the same band.

The bandpass bandwidths for both 1 and 3 dB levels maximize in the vicinity of 2-dB ring attenuation; their values are respectively 150 and 330 MHz. Coupling is 10.5 dB, directivity is 13.5 dB, and insertion loss is down to only 3.3 dB. In this condition, the test model fulfills all of the bus coupler requirements.

Phase modulation

Modulation is necessary to code the carrier with the data to be communicated. Many modulation varieties are useful; perhaps the most simple is amplitude modulation. The latter, however, is neither the most efficient nor the most immune to noise degradation of the intelligence to be communicated. Digital phase modulation of a coherent signal is increasing in popularilty among communications systems designers for just these reasons; the most simple form of digital phase modulation provides shifts in phase between 0 and π radians.

A circulator/diode switch (Fig. 5a) is used as the modulator; however, a coax-to-waveguide transition with oppositely biased diodes (Fig. 5b) is a promising alternative.[6] Both methods require diodes. The modulation period requirement (approximately 10 ns) makes it necessary to have switching time of 10 ns or shorter. PIN diodes with 2.5 ns switching time are used.

The PIN diode mount is similar to that used by Clemetson, et al.[7] The diode is positioned at one end of a coaxial resonator offset from the center of the guide; this positioning approxiamtes an impedance match for almost any resonator Z_o. The geometry of the diode mount is shown in Fig. 6. In a test model, the coaxial line is a half-wavelength long and the distance along the waveguide from the plane of the loaded coax to the plane of the short is varied to attain a midband reflected wave phase shift of 0.25 λg. This corresponds to a 180° phase shift when the diode mount is used with a circulator. The bandwidth over which the measured phase shift exceeds 0.2 λg is used to compare relative bandwidths. Two diode mounts appear to be necessray to cover the 4-GHz band.

Demodulators

The role of the demodulator is to receive and store the phase-modulation condition so that it can be combined with a subsequent signal of the second phase-modulation condition in a constructively interfering manner. The function is quite similar to the interferometers used in the field of physical optics. The only difference is the relation between the modulation rate and the incremental phase delay in one of the two paths. Clemetson, et al[7] used a bridge demodulator (Fig. 7a) consisting of two hybrid junctions and connecting lines, one exceeding the other by a length that is traversed by the signal in one modulation time slot. If the *on* and *off* times were equal, one time slot would be equal to half the period of the modulaiton. The variable attenuator compensates for the loss of the delay line and the termination — and the isolators are used to improve the performance of the bridge.

A reflex demodulator (Fig. 7b) provides considerable simplification. It utilizes the isolation inherent in the hybrid junction; attenuation balance is accomplished as before but the phase balance is much more easily achieved with an adjustable *short*. The delay link is reflectively terminated and since it is traversed twice by the signal, only half as much line is required. A dielectrically loaded coaxial line provides additional foreshortening — by a factor equal to the square root of the dielectric constant, as well as by the $\lambda g/\lambda o$ ratio of the waveguide alternative.

The properties of the reflex demodulator and its driver require a delay of 10.6 ns. If a non-reflex demodulator were used it would require 163 inches of waveguide delay line; the length is shortened to only 44 inches of dielectrically loaded coaxial line in the reflex configuration.

System performance

A system consisting of a source module

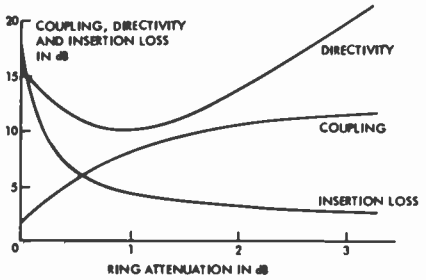

Fig. 3 — Coupling, directivity, and insertion loss in dB versus ring attenuation in dB.

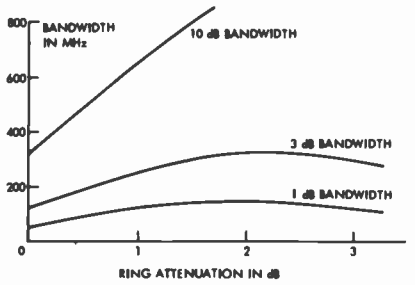

Fig. 4 — Bandwidth in MHz versus ring attenuation in dB.

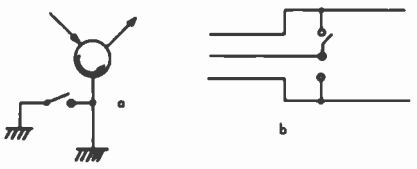

Fig. 5 — Diode phase modulator.

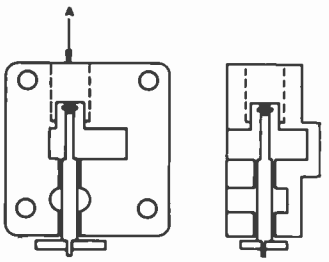

Fig. 6 — Phase modulator.

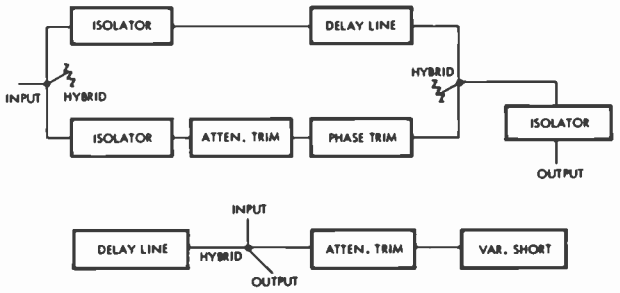

Fig. 7 — Demodulator types.

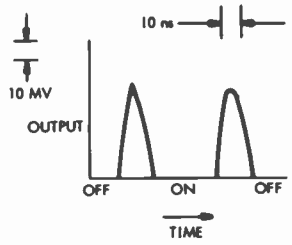

Fig. 8 — Demodulator waveform.

coupled to a length of line, and a coupled sink module has been configured for test evaluation; both couplers are 10 dB nominal. The source is initially operated in a CW manner. The variable attenuator and adjustable short of the demodulator are adjusted for a null at the detector. This adjustment balances the reflex demodulator and provides a signal to the detector only during the transition periods of the phase modulator. Fig. 8 shows the transition relative to the *on/off* conditions of the bias pulse on the modulator. The measured receiver sensitivity for the model is 24 mV/mW.

$$P_r = FKTB = 4 \times 10^{-13}\ W$$

Where F is 2 for a noise figure of 3 dB, B is 50 MHz, K is Boltzmann's constant and T is the temperature in Kelvin degrees.

In the 50-ohm system used in the model, P_r corresponds to a video noise voltage of 4.5×10^{-6} volts. The microwave power required to produce an equal signal is related to the system sensivitity as follows:

$$P_s = 4.5 \times 10^{-6}\ V / 24 \times 10^{-3}\ V/mW$$
$$= -37.3\ dBm$$

Due to the square-law action of the detector, a 10-dB increase in rf power will increase the signal-to-noise ratio by 20 dB; this ratio results in a bit-error rate of 10^{-8} and is attained at an rf level of −27.3 dB into the demodulator assembly. Using the measured transmitter output of +15 dBm, the allowable attenuation by couplers and lines is (15 + 27 = 42 dB). This level satisfies the sensitivity requirements for the model where each coupling in and coupling out of the bus line introduces a 10 dB change; line attenuation is 8 dB per hundred feet.

Increased sensitivity, attainable by the use of a superheterodyne sink module, increases the allowable path loss to approximately 90 dB. This is at the expense of greater complexity and cost, but it is indicative of the range of data-transfer system requirements that may be satisfied by the microwave technique.

Conclusion

Techniques applicable to a microwave data-bus and a system model have been described. A more complete visualization of the variety of possible system configurations may be gained from Fig. 9.

Similar couplers are used for both sources (transmitters) and sinks (receivers). Such couplers may be either single (as shown in five of those depicted) or they may be multiple (as shown for the center receiver module). The center receiver module couples signals from either or both of two bus lines to a single receiver and data output.

The source or sink modules may be coupled either directly or remotely to the bus couplers. The indirectly branched-line coupling from the modules to the bus couplers is expected to be very convenient for outboard systems frequently required in the wing-or tail-mounted pods of aircraft installations.

Increased technological development and utilization of the 18 to 23 GHz band can be expected for digital communications systems for special common carriers. The digital modulation/demodulation techniques of the same types developed and described in this study program are expected to be used. The transmission paths, whether guided or radiated, are expected to be considerably longer than those required in self-contained systems. Losses will be counteracted by the use of repeaters, and the digital techniques will eliminate the exponential buildup of noise that is otherwise characteristic of multiple-repeater systems. The existence of these communication systems in the same frequency range contemplated for data bus use is not expected to increase interference. The atmospheric water-vapor attenuation and the excellent shielding provided by the metallic waveguides, as well as the high directivity easily attained for the communications systems antennas should prevent interference.

The use of digitally modulated waves at frequencies approximating 20 GHz is technically mature and is a timely expression of what can be done at this time.

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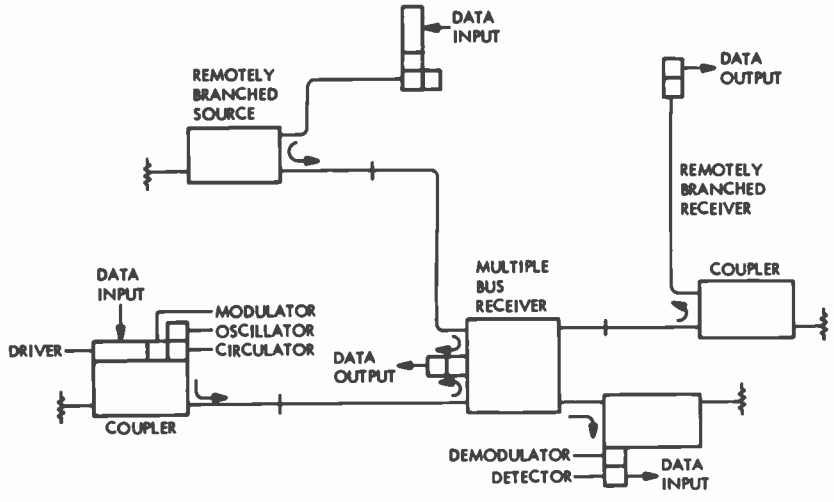

Fig. 9 — Possible system configurations.

RCA Satcom System

J. Napoli| J. Christopher

Communication satellite systems of the future must handle a high capacity of diversified services; however, present communications satellites are not able to provide these services without significant launch costs. This paper describes how advanced technologies and new developments of both launch vehicle and spacecraft, as presently undertaken by RCA Globcom/RCA Alascom, lead to economical provision of communications services.

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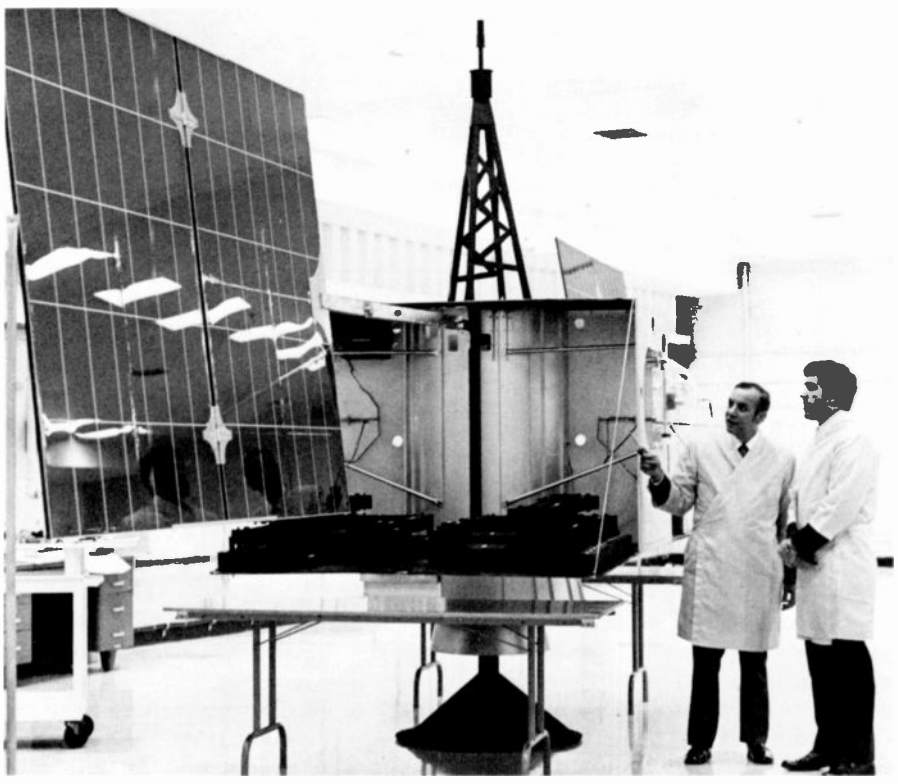
John Chrisopher, Director, Spacecraft Engineering and Production, RCA Global Communications, Inc., New York, N.Y., received the BSME in 1950 from New York University and the MSME in 1965 from the University of Pennsylvania. Mr. Christopher accumulated 24 years of Aerospace design experience with the General Electric Space Division and Goodyear Aerospace Corporation. At Goodyear he was a structural analysis engineer and was the company's designated structural representative to the Navy for airship construction. Mr. Christopher joined General Electric in 1960 and was involved in the development and test of the Mark III and Mark VI re-entry vehicles. He started working communication satellite programs with the Air Force Advent Satellite Program and pursued this product line as Manager, Vehicle Engineering of Advanced Programs. In this position, he was responsible for the spacecraft design, including all of mechanical and housekeeping subsystems on General Electric's ATS-F and G program, the Fleetsatcom, Aerosat, military programs, and Japanese Broadcast Satellite activities up to the time of contract award. Mr. Christopher joined RCA Global Communications, Inc., as Manager of Spacecraft Engineering in November 1973. In April 1974 he was appointed Director of the Spacecraft Engineering and Production for the RCA SATCOM spacecraft, launch vehicle, mission operations, and support services.

Authors Christopher (left) and Napoli: at the integration site for the RCA Satcom satellite.



IN the fourth quarter of 1975, RCA Global Communications, Inc. and RCA Alaska Communications, Inc. will launch a new generation of communication satellites, marking the beginning of RCA's Phase II toward establishing a multi-purpose domestic satellite communications system — the RCA Satcom System.

Phase I consists of leasing transponders on the Canadian ANIK II satellite and has been operational since December 1973. This interim system will be phased out by the improved spacecraft and ground station system being developed.

As a start to planning Phase II, technical and economic system objectives and design choices were established, based on an intensive market analysis of private-line and other sources in the contiguous 48 states, Alaska, and Hawaii. The system chosen is based on a complement of 24-transponder, eight-year-life spacecraft, in the 2000-lb weight range. Included in the tradeoff analysis was the cost of launching with an advanced uprated Thor Delta (3914), whose development was not then approved by NASA. This launch vehicle could provide the additional performance required for a relatively small cost increase over the 2914 Thor Delta. RCA's decision to privately fund its share of the launch-vehicle uprating, via a separate contract with McDonnell Douglas Astronautics Company, marks the first time industry has set design requirements and provided funds for development of a launch vehicle. The spacecraft/launch-vehicle combination selected is the most economical means of positioning high-capacity communication satellites in geosynchronous orbit.

Because of the decisions made to invest in the advanced technology of the RCA Satcom System, rather than to use existing hardware with lesser performance, improved communication services will be made available at substantially reduced rates.

Satcom systems objectives

Based on telecommunication traffic patterns projected for the fifty states for the next ten years, a set of system objectives evolved. Of prime concern is

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Table I — Candidate configurations.

Freq. Plan (GHz)	*No. of Xponders*	*Satellite Design*	*Launch-vehicle Payload req.*	*Advantages*	*Disadvantages*
6/4	12	Spin stabilized	1550 lbs	• Proven design	• Does not permit a competitive edge against other proposed systems
6/4 6/4	12 12	Two spin-stabilized spacecraft	Two-1550-lb launch vehicles	• Proven design • Permits high-capacity communications • Provides ample spare capacity	• Not cost effective • Requires additional orbital space-decreasing world resource • Increase in TT&C Station Costs
6/4 & 14/12	12 6	Spin stabilized	1550 lb	• Proven satellite design • Increased communications capacity	• 14/12 GHz frequencies not demonstrated in commercial applications • Power limited • Increase in cost and complexity of control stations
6/4 & 14/12 or 12/7	12 12	Spin stabilized	2000 lb	• Proven satellite design • Increase communications capacity	• 14/12 and 14/7 frequencies not demonstrated in commercial applications • Power limited during eclipse • Increase in cost and complexity of control station. • New development for launch vehicle
6/4	24	Body stabilized	2000 lb	• Proven TWTA's • Hardware derived from other programs • High-capacity communications • Power and fuel for 8-year mission	• New development for launch vehicle, spacecraft structure, and AKM.

coverage of the rapidly expanding Alaskan market, with emphasis on tv broadcast and demand-assigned telephone traffic. Specific service objectives for the entire system are as follows:

- Provide reliable telecommunication services to interconnect the contiguous 48 states, Alaska and Hawaii.
- Provide a full range of private-line analog and digital voice, data, and video services to subscibers within these locations.
- Provide message toll telephone service for Alaska, including the upgrading of service in the remote areas of the state.
- Provide network-quality tv signal transmission services to the major commercial and educational tv networks, plus catv operators.
- Provide a low-cost alternative to the established terrestrial facilities which presently provide the above services.

Design trade studies

The RCA Satcom spacecraft/launch-vehicle configuration was chosen from several candidates because it best satisfied the performance, minimum life, and economic objectives of the mission. The ability of operating all 24 of the 6/4-GHz transponder channels at the specified radiated power throughout the minimum eight-year life, including eclipse periods, was the most challenging of all requirements to satisfy utilizing state-of-the-art technology. This requirement, compatible with a relatively economic up-rated thrust-augmented Thor Delta launch vehicle would give the RCA Satcom System a competitive lead over presently proposed systems filed with the FCC by other applicants. The tradeoffs of candidate configurations are summarized in Table I.

Each of three bidders responding to the RCA Globcom/RCA Alascom requirements for a suitable spacecraft

proposed a three-axis body-stabilized platform to support the power and attitude requirements of the 24-transponder payload. The selected design, as depicted in Fig. 1, was awarded to the RCA Astro-Electronics Division.

Delta 3914 launch vehicle

Agreements for the development of the uprated Thor Delta launch vehicle, the Delta 3914, have been consummated between, McDonnell Aeronautics and Space Administration, and RCA Globcom and RCA Alascom. The development of the 3914 has increased the geosynchronous transfer orbit useful load from 1,550 (for the 2914) to 2000 lb. Thus, the development of the Delta 3914 was as instrumental in meeting the system requirements for a 24-transponder channel spacecraft as was the three-axis controlled spacecraft.

The Delta 3914 is a direct evolution of the Delta 2914 standard NASA configuration. It has been NASA's opinion that the uprating of the Delta vehicle from the 2914 configuration to the 3914, though substantial, represents minimal technical risk. The major difference between the model 3914 and the model 2914 is the substitution of the larger Thiokol Castor IV solid augumentation motors and the attendant attach hardware in lieu of the standard Castor II motors. Most important, the spacecraft/launch-vehicle interface is the same, and the vehicle flight requirements for the 3914 are within the envelope of those for the 2914. In fact, with the use of an acoustic shroud, all 3914 environmental design factors are lower than for the 2914.

The key to the modification was an extensive wind-tunnel test program, undertaken to confirm the 3914 vehicle's stability control analysis, and to provide additional understanding of the solid motor release and drop sequence. As a result of this testing, a positive-acting spring separation system for the solid motor separation was developed and a five, four solid-motor jettison sequence was selected to maximize performance. This, with the associated structural redesign and static test of the boat tail section, which supports the larger thrust motors, comprised the major elements of the uprating. The second and third stages of the 3914 are identical to the 2914. Each of these activities and all design and development efforts associated with the

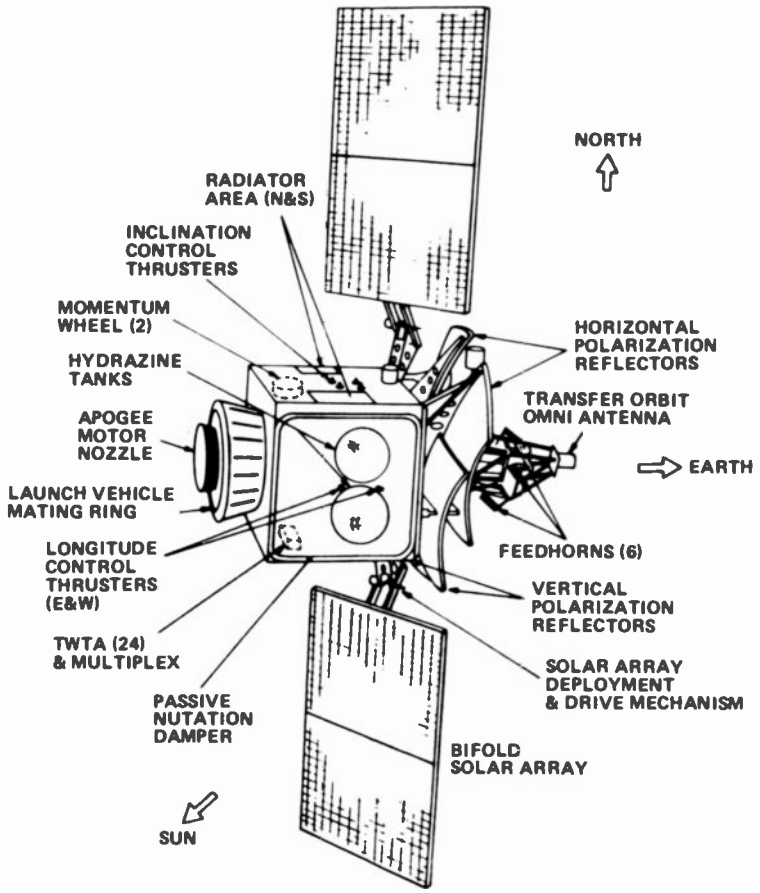

Fig. 1 — RCA Satcom satellite.

Table II — Characteristics of communications subsystem.

Element	*Key performance features*	*Technical approach*
Overall subsystem	• 24 34-MHz channels to CONUS, Alaska, at 32 dB_W • 12 34-MHz channels to Hawaii at 26 dB_W • Redundancy	• Reuse of spectrum through polarization diversity; precise position and pointing control and beam shaping to minimize rf power. • Separate offset feed-spot beam coverage. • Dual solid-state wideband receiver-driver; 24 independent channels.
Transponder	• 24 independent channels • Lightweight multicoupler diplexers	• Use of 24 flight-proven high-efficiency TWTA's with independent power supplies. • Space-qualified graphite fiber epoxy composite filters.
Antennas	• Cross-polarization isolation Receive — 33-dB Transmit — 33-dB • Low-risk mechanical design	• Separate receive antenna for each polarization; isolation based on full-scale test data • No reflector feed deployment required.

Fig. 2 — RCA Satcom system coverage.

3914 configuration have been reviewed and approved by NASA.

Basic flight reliability and performance of the Castor IV motor have been demonstrated by the U.S. Air Force during qualification firings and flights of the Athena H vehicle. The required 11° nozzle cant modification on the Castor IV motor, for 3914 application, was reviewed and approved by the U.S. Air Force/Aerospace Corporation. Qualification test firings of the modified Castor IV were completely successful and verified the analytical studies.

To accommodate the larger 3914, modifications of launch complex 17A at the Kennedy Space Center were necessary.

Thus, the Delta 3914 development is substantial, and also constrained by a very tight schedule. Yet, the program has met all major milestones, design decisions have been implemented smoothly, and the overall development is proceeding as planned. This is attributed to the coordination and cooperation of RCA Astro-Electronics Division, McDonnell Douglas, and NASA in this unique launch-vehicle development program.

Space segment

The satellite system has been designed to fulfill three primary mission requirements:

- Communications coverage for Alaska, Hawaii, and the contiguous 48 states.
- Capability of operating all 24 transponder channels at specified power throughout the minimum 8-year life, including eclipse periods.
- Compatibility with the Delta 3914 launch vehicle (2000 lb. useful transfer-orbit payload).

The spacecraft design provides radiated power over the areas shown in Fig. 2. With the satellite positioned at a given longitude, a corresponding E-W pointing offset maintains the beam coverage over these areas independent of the actual longitude station. The antenna assembly directs all 24 channels to Alaska, as well as to the lower 48 states, and couples outputs from 12 channels to the Hawaii spot beam.

Frequency reuse establishes 24 independent 34-MHz channels within the 500-MHz allocated band. The channels are spaced on 20-MHz centers, but are transmitted via alternately horizontal and vertical polarizations in order to isolate adjacent channels. The high degree of polarization isolation required to support this system is achieved in the antenna reflectors via orthogonal reflecting grids embedded in supporting dielectric surfaces. Preliminary tests indicate that greater than 33-dB polarization discrimination, for both receive and transmit beams, has been achieved throughout the specified coverage area.

The transponder design (Fig. 3) includes a separate receiver for each polarization, so that twelve out of twenty-four channels are supported by each receiver. These receivers contain fully redundant signal paths, each of which consists of a low-noise tunnel diode amplifier front-end, a Schottky-barrier diode mixer, and a high-gain transistorized amplifier driver.

The twelve channels in each receiver output are separated, amplified, and recombined via the input multiplexers, twenty-four non-redundant traveling-wave tube amplifiers, and the output multiplexers. Both the input and output multiplexers are constructed out of plated graphite-fiber epoxy composite (GFEC) waveguide, which is being pioneered for this application by RCA Limited

The signal design for these channels include:

- Single-carrier fdm-fm or tdma (frequency division multiplex—frequency modulation or time-division multiple access, respectively). The projected capacity of an fdm-fm carrier is approximately 900 voice channels.
- Single channel per carrier with demand assigned-routing capability and approximately 500-channel capacity.
- Single carrier fm-tv of network quality, and
- Approximately 50 megabit data stream.

A summary of the communications subsystem is shown in Table II.

Spacecraft bus subsystems and system performance

Each spacecraft housekeeping subsystem has been designed for optimum performance and maximum probability of successful operation. The spacecraft operating survival probabilities with 20 transponders operational at the end of 7 and 8 years respectively are 0.6 and 0.5. Assurance of program success is provided by the use of space-proven components for all the subsystems. Further, redundancy and parts selection have been applied in such a manner as to ensure specified reliabilities over the system lifetime. The salient performance features and technical approaches are summarized in Table III.

Ground operation centers

Two redundant telemetry, tracking, and command (TT&C) ground stations, one

at the East Coast and one at the West Coast, contribute to operational reliability of the RCA Satcom multi-spacecraft communication system.

Collocated at each site is the Satellite Technical Operations Control Center (STOCC) capable of monitoring and controllng three spacecraft during commercial operations. The East Coast TT&C/STOCC will be designated as system controller, with the West Coast facility operating in a standby mode, fully capable of assuming systems control at a moment's notice.

A central control console at the STOCC enables a single operator to monitor spacecraft performance, ascertain orbit position, and to issue commands to each of the three RCA Satcom spacecraft. Collocated at each site are communications antennas, one for each spacecraft. To facilitate transfer-orbit operations, each TT&C site is equipped with a 10-meter auto-track antenna capable of 360° rotation in azimuth and 90° in elevation.

Two 3-kW transmitters can be combined to provide ample power margin for ranging and commanding during transfer-orbit operations as well as on-station commercial operation. TT&C capability for transfer orbit operations is augmented via Intelsat's Fucino (Italy) and Carnarvon (Australia) stations, providing backup coverage during initial orbits. These stations have been instrumented by RCA Globcom/RCA Alascom for compatibility with the RCA Satcom spacecraft.

Earth segment

The major functional elements of the RCA Satcom System are the Earth Stations with an associated Central Terminal Office, the Demand Assign-

Table III — Spacecraft support subsystems characteristics.

Subsystem	*Key performance features*	*Technical approach*
Command, ranging and telemetry	• 248-command capability with false command rate $< 10^{-22}$ • 121-channel telemetry capacity with accuracy of ±2.5%	• Ternary fsk command system based on existing RCA design. • pam/fm/pm telemetry subsystem utilizing qualified circuits.
Apogee motor	• Mass fraction (propellant wt/total wt) = 0.939 • impulse propellant. spacecraft-weight ratio = 0.951	• High efficiency provided by use of proven design approach and high specific • Carbon-carbon contoured nozzle saves weight and improves performance
Reaction control	• Blowdown monopropellant hydrazine systems incorporating surface-tension propellant management provides 1500 ft/s • Operational redundancy	• Flight-proven thrusters and propellant management system result in least technical, cost, and schedule risk for 8-year mission requirements. • Thrusters and tankage arranged in functionally redundant half-systems.
Attitude control	• Autonomous three-axis body stabilized control system providing pointing accuracies of ±0.12° E-W, ±0.14° N-S; E-W offset pointing from 0° to ±5° also provided. • Spacecraft is nutationally stable during all modes	• Momentum-bias and magnetic-attitude control demonstrated on operational satellites; control using mass expulsion provided during ΔV maneuvers; attitude sensing techniques are flight proven. • Stable inertia ratio in transfer orbit and momentum wheel stability in operational mode.
Power	• Efficient power system providing over 550 W throughout 8-year design life • Provides power for 24 transponder during eclipse.	• Direct energy transfer system developed and flown. Single-axis sun-oriented solar array; three-battery configuration for full eclipse power; all components based on existing designs.
Thermal	• Maintains all components in suitable thermal operating environment (e.g., batteries 0° to 10°C; reaction control + 5° to 50°C; and communications 0° to 50°C)	• Passive control insulators and surface finishes are flight proven; ground-commanded heaters minimize internal power dissipation range. • OSR's for radiator surfaces.
Structures	• Lightweight design of 5.6% of transfer orbit weight. • Satisfies all frequency and dynamic envelope constraints of booster.	• Use of honeycomb and machined magnesium materials. • Based on extensive design and test experience on spacecraft for Delta booster.

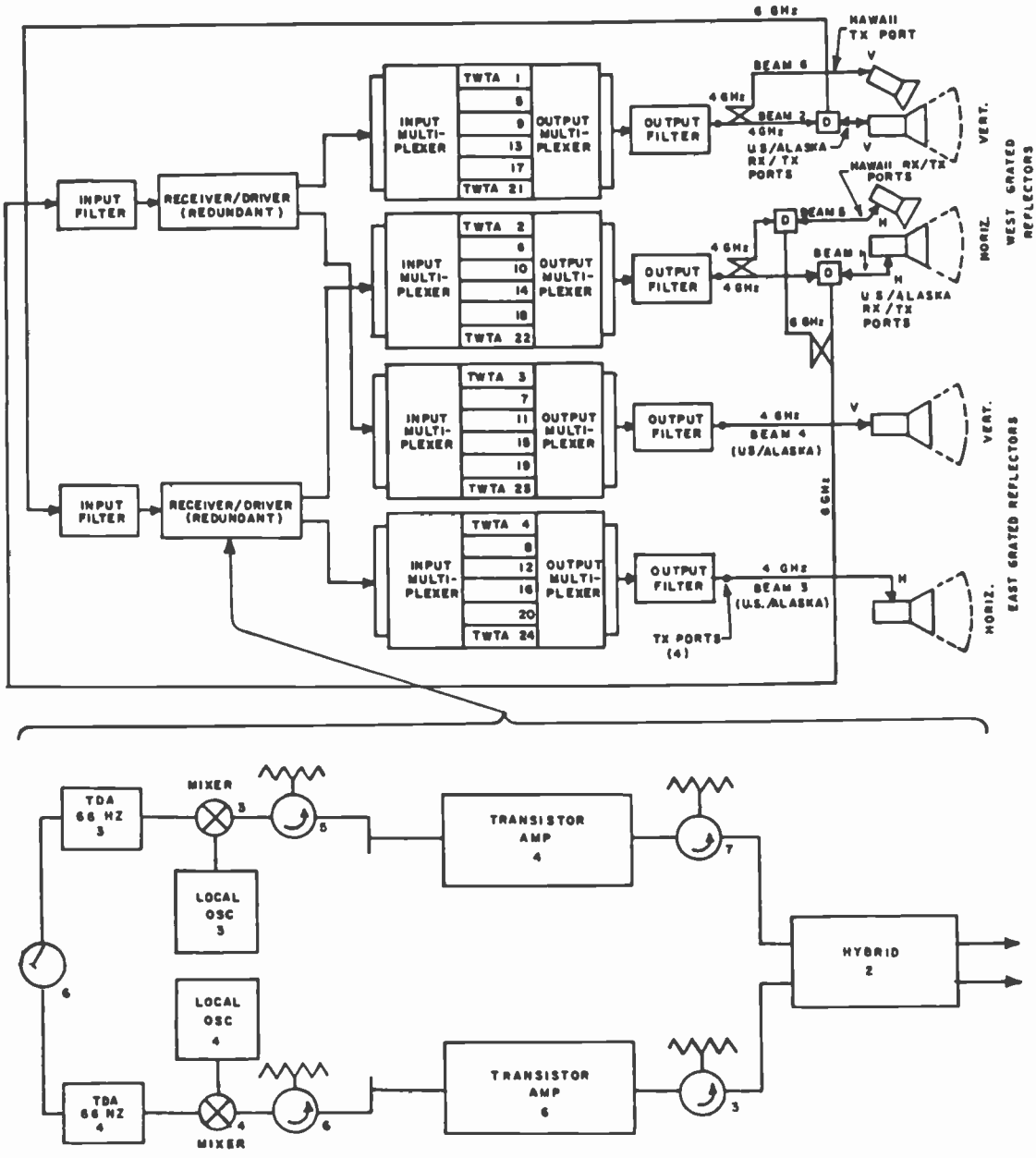

Fig. 3 — Communication subsystem.

ment Control Center, the Communications Satellites, and the supporting terrestrial line links. Fig. 4 shows the interrelationships of these major system components.

Telephone access lines and other communications circuits from the user's locations are connected by terrestrial links, to the Earth station. These Earth stations in turn, are interconnected through domestic satellite channels to provide long-haul telecommunications transmission.

A special feature of the RCA Satcom System is that satellite channels may be assigned for use between any two specific geographical locations upon demand. This feature, known as Demand Assignment, considerably reduces the number of satellite channels required to meet the peak traffic loads of switched networks. Demand Assignment works to assign satellite channel frequency-pairs to establish interconnections as calls are made by the users. These assignments are made by selecting satellite channels from the available pool, then assigning a pair of frequencies to each of the points wishing to communicate. The Earth Stations at those points automatically communicate on the assigned frequencies for the duration of the call. At the end of the call, the frequencies are reassigned to the pool to await allocation to a new call. In some networks, fixed assigned point-to-point channels are required. They can be readily obtained through a permanent assignments of frequency pairs.

Considerable flexibility has been designed and built into the various hardware components of the Satcom system. Thus, RCA Satcom can accommodate any combination of video, switched or point-to-point voice, teleprinter, data, facsimile, or other wideband transmission, both efficiently and at the lowest possible total cost. This flexibility insures that cutover from the user's old system will proceed with little or no disruption to his daily operations.

An important new concept in the RCA Satcom system is automatic maintenance monitoring. This feature will permit the location and isolation of circuit faults before the user is aware of any difficulty. Automatic switchover to standby facilities is provided in many cases to insure full and continuous end-to-end service. Service monitoring positions manned 24 hours a day are accessible to the user, to handle any difficulties that may arise and fail to be corrected before coming to his notice.

Stations presently communicating through the interim RCA Satcom System are located at Valley Forge, Pa.; Pt. Reyes, Calif.; Juneau, Alaska; Bartlett, Alaska; Put River, Alaska; and Valdez, Alaska. Additional stations are being procured and will be sited near a number of major U.S. population centers to coincide, roughly, with the launching of the RCA Satcom spacecraft.

Summary

The RCA Satcom System is designed to meet critical needs for additional long-distance telephone circuits in Alaska more economically than through the use of existing satellite facilities. In addition, the cost of leased voice-grade circuits between the East and West Coasts of the contiguous U.S. will decrease approximately 35% compared to a terrestrial line.

Besides message telephone service in the case of Alaska and private-line services, the RCA Satcom System may also be used for network television transmission services. The lower cost of live television transmission via RCA Satcom to and from Alaska makes live programming more practical for the state.

Once the full system has been established and made operational, continual technological improvements will be introduced to make the RCA Satcom services even more cost effective to subscribers.

Acknowledgment

The authors gratefully acknowledge H. Landerer of Services for planning and coordinating support; also acknowledged are the engineers in the Leased Facilities and Engineering Department of RCA Global Communications, who were instrumental in implementing the RCA Satcom program.

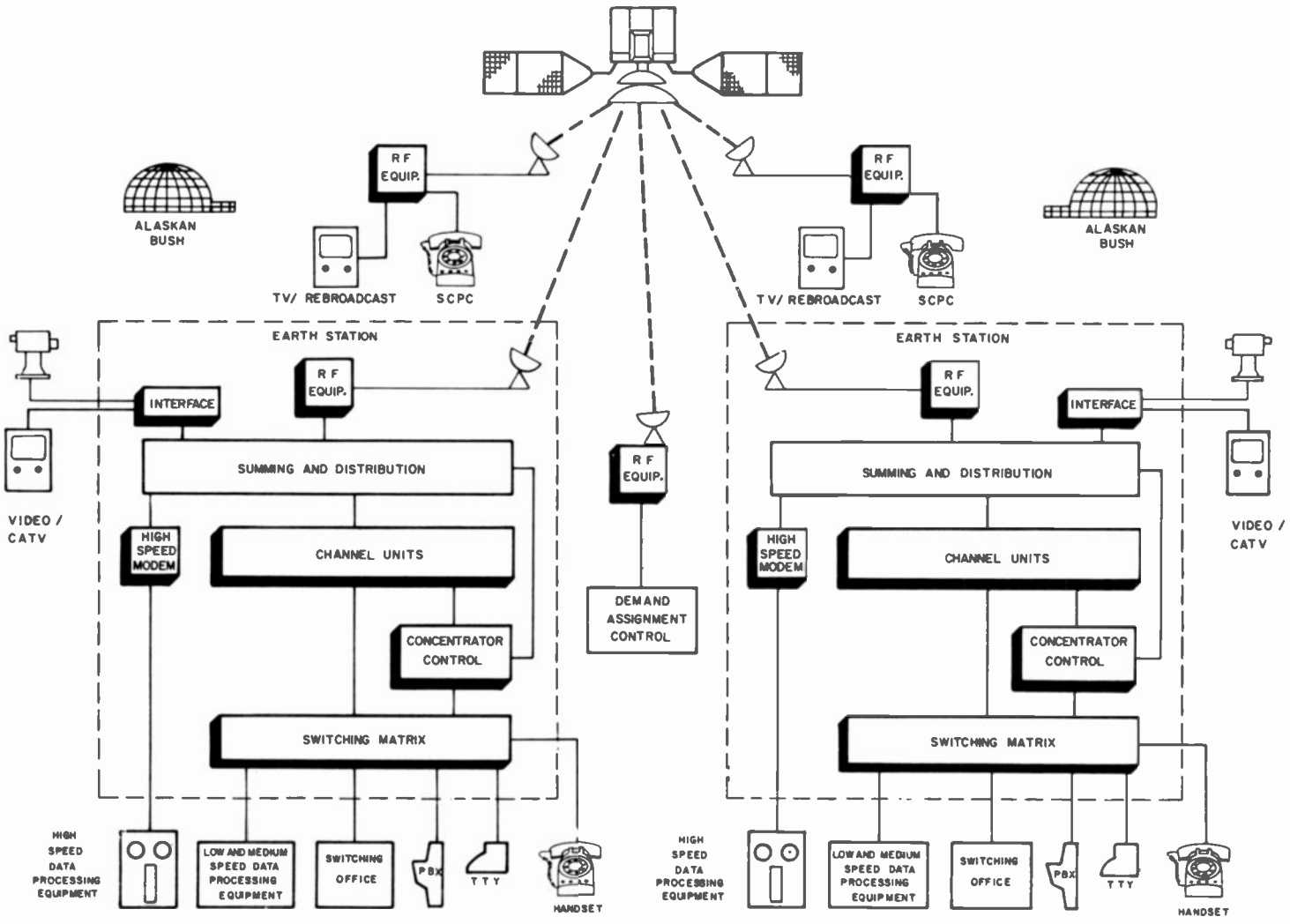

Fig. 4 — Major RCA Satcom system components.

Charge-coupled devices and radar signal processing

L. O. Upton| G. J. Mayer

Recent advances in charge-coupled device (CCD) technology show significant potential for improving performance of radar signal processors and for reducing the hardware complement. The application of CCDs to moving-target indicator (MTI) transversal filters is discussed and supported by experimental data. Tutorial information on CCDs and the description of a continuing CCD matched-filter program are also included.

CHARGE-COUPLED DEVICES (CCD) are members of the rapidly expanding semiconductor charge-transport-device family. The distinguishing feature of this family of devices is the ability to store and transfer information by the controlled movement of electric charge. In essence, CCDs exhibit both digital and analog device characteristics. They are digital in the sense of clocking information from storage cell to storage cell, as in a shift register. They are analog in that each cell content representing information has a continuum of levels (voltages) rather than the binary "0" or "1" states of digital systems.

The digital techniques for handling and processing radar data, in general, have yielded excellent results, but at a high cost in terms of the quantity of hardware required, power dissipation, and circuit interconnection complexity. CCD technology has significant potential for reducing the hardware complement and improving system performance by eliminating the need for analog-to-digital converters and complex digital multipliers, and by increasing internal data rates beyond one gigahertz.

A particularly apparent and attractive application of CCD delay-lines is in the area of transversal filters. Transversal or non-recursive sampled-data filters are widely used in radar signal processing, interpolation, and moving target indicator (MTI) clutter rejection.

Transversal filters provide frequency selective characteristics for target clutter discrimination on a doppler-frequency basis. In general, the MTI transversal filter, or MTI canceller, is designed to place a frequency attenuation notch at the centroid of the clutter frequency spectrum and to pass all other doppler frequencies. If the target doppler is different than the clutter doppler, then target detection is improved.

A second general class of CCD filters involves application to matched filtering or correlation processing. This area of application may well be the most advantageous for CCD implementation, since it is usually the high cost item of a radar signal processor.

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CCD technology

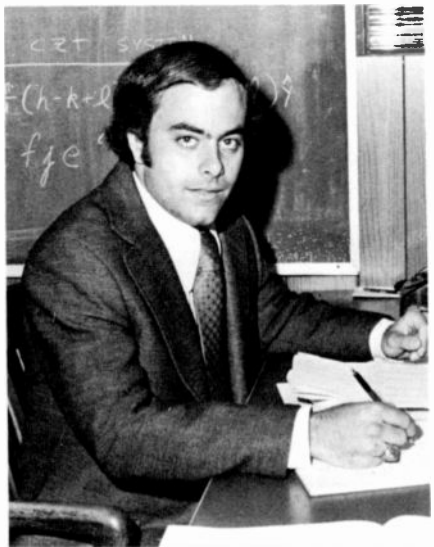
The development of the charge-coupled device (CCD) has been rapid since its inception five years ago.[1,2] The technology has advanced from the laboratory demonstration of eight-stage shift registers (which lost 1% of the stored information on every stage transfer) to high-speed 500-stage registers[3] with transfer efficiencies up to 99.99%.[4,5]

Basic charge—transfer action

A three-phase CCD is physically a linear array of MOS (metal-oxide-semiconductor) capacitors spaced very closely together with every third one connected to the same clock voltage, as shown in Fig. 1.

To transfer charge to the right, from ϕ_1 to ϕ_2, a positive voltage is applied to the ϕ_2 gates. This positive voltage forms a deep charge well under the ϕ_2 gates, into which the ϕ_1 charge spills. The capacitors must be closely spaced so that the depletion layers overlap strongly and the surface potential in the gap region is a smooth

Gerard J. Mayer, Advanced Technology, Missile and Surface Radar Division, Moorestown, New Jersey, received the BE in electrical engineering from Villanova University in 1973. He is currently pursuing the MS at the University of Pennsylvania. Mr. Mayer is presently investigating the application of Charge Coupled Devices (CCD) to signal processing. Since joining MSRD's Advanced Systems and Technology group in 1973, he has been involved in the design, implementation and evaluation of a developmental CCD clutter rejection system which was used to evaluate the signal processing potential of CCD. He has prime responsibility for the development of CCD signal processing at MSRD, including a CCD radar pulse compression system. Previous assignments included the design of subsystems for an advanced CMOS/SOS digital pulse compression signal processor. He developed a custom CMOS/SOS array which is a basic building block of the processor and implements a variety of signal processing functions. He has also performed system studies on image rejection, image jamming and cover pulse jamming for the Navy's Aegis system. Mr. Mayer is a member of Eta Kappa Nu.



transition from one region to another.

To complete the charge transfer, the positive voltage on the ϕ_1 gate is changed to a small positive dc level sufficient to maintain a shallow well under the ϕ_1 gates. Now the ϕ_2 wells are deeper, a condition which causes any charge that has remained in the ϕ_1 wells to spill into the ϕ_2 wells. Most of the charge that originally was under the ϕ_1 gate has been transferred to the well under the ϕ_2 gate. The small amount of charge that is not transferred from the ϕ_1 well determines the transfer efficiency.

The charge is prevented from moving under the ϕ_3 gate by the barrier formed from the shallow well under the ϕ_3 gate. The same process moves the charge from the ϕ_2 well to the ϕ_3 well. After one complete cycle of a particular clock, the packet of charge has been moved one stage (three gates) to the right. No significant amount of thermal charge accumulates in a particular well because it is continually being swept out by the charge-transfer action.

At the output, the charge is transferred into a reversed-biased drain diffusion and, from there, to the substrate. The charging current required to maintain the drain diffusion (fixed-potential) can be measured to determine the signal magnitude (current-sensing); alternatively, a re-settable floating diffusion can be employed which controls the potential of a gate (voltage sensing).[6]

In three-phase CCDs, the potential wells are symmetrical, and the charge-transfer direction is controlled by the asymmetrical gate voltages (phase clocks). A two-phase CCD can be constructed in which the potential well has a built in asymmetry that determines the direction of the charge transfer; the potential well must be deeper in the direction of charge transfer. This can be achieved by having two thicknesses of oxide under one gate or by incorporating a variation in the doping level. A two-phase CCD can be operated with only one phase clock and a dc bias on the other phase clock gates. These clocking characteristics give the CCD flexibility to adapt to a wide variety of applications.

The transfer efficiency of a CCD determines how many stages a signal can be passed through before the output signal becomes seriously degraded. The fraction of the total charge that is transferred per gate is called the transfer efficiency, η. The fraction left behind is the loss per transfer, ϵ. If the transfer efficiency is $\eta = 99\%$, the input signal will be nearly lost after 100 stages. The transfer efficiency is therefore a very important figure of merit for the CCD.

The CCD device that has been described is a surface-channel device. Another type is the buried-channel device in which the charge transport occurs inside the body of the silicon substrate. The significant differences between surface and buried-channel devices are shown in Table I.

Device technology

Five different types of charge-coupling structures have been used for surface-channel CCDs, as shown in Fig. 2. The single metal-gate CCD (Fig. 2a) is the structure introduced by Bell Laboratories in 1970.[2] RCA Laboratories constructed

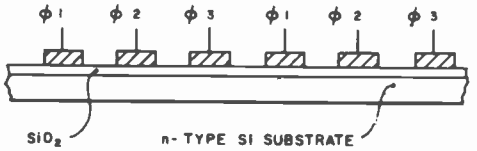


Fig. 1 — CCD structure.

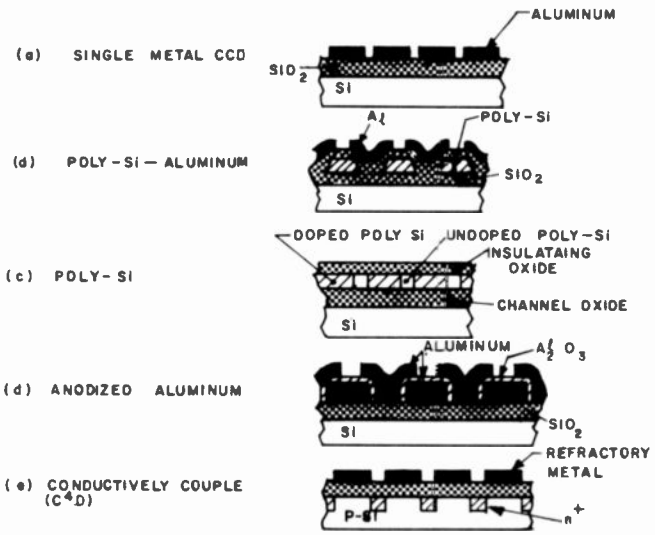


Fig. 2 — Differing technologies for charge-coupling gate structures.

Table I — CCD characteristics — surface-vs. buried-channel.

	Surface channel	*Buried channel*
Fabrication	Simplest	Requires additional processes, resulting in lower yield
Transfer efficiency	99.99%	99.999%
Frequency	10 to 20 MHz	> 100 MHz
Signal handling capability	Large signal capability (> 1 V)	Small signal—charge less than surface channel
Dynamic range	40 to 50 dB	40 to 50 dB

single metal-gate p-channel and n-channel CCDs, but found their transfer loss high ($\epsilon \geq 10^{-3}$). The operations of the single metal-gate CCDs can be achieved with the sealed-channel charge-coupling structures shown in Figs. 2b, 2c, 2d, and 2e.

A sealed-channel CCD in the form of polysilicon gates overlapped by aluminum gates (Fig. 2b) has been developed at RCA Laboratories. This device operates with transfer loss $\epsilon \leq 10^{-4}$ for a clock frequency $f_c \leq 2$ MHz and $\epsilon = 10^{-3}$ at $f_c = 20$ MHz. The sealed-channel CCD of Fig. 2c was also developed by RCA Laboratories and has been used for imaging. In this design, the CCD gates are heavily doped polysilicon regions separated by undoped, high-resistance intervening polysilicon spaces that provide a conductive seal over the channel oxide in the inter-gate spaces.

Another sealed-channel CCD is the anodized aluminum charge-coupling structure shown in Fig. 2d. The main advantage of this structure is that both gate layers are made up of low resistivity conductors which eliminate the time delay associated with clock voltage buildups of long polysilicon gates. For most signal processing applications, this time delay is not expected to present a problem. This structure was also built at RCA Laboratories.

The conductively coupled CCD (C^4D) shown in Fig. 2e is a single metal-gate CCD with diffusions lined up between the gates, to conductively couple the charge between the potential wells under the gates. The C^4D is not practical for signal processing applications because the performance of the device resembles the bucket-brigade mode of operation, with transfer inefficiency in the range of 10^{-3}.

Buried-channel CCDs have also been constructed at RCA Laboratories. These devices can operate at higher frequencies than surface-channel CCDs, but they are more difficult to fabricate and can accept only low-voltage signals.

The number and variety of CCD structures under design and evaluation are imposing, and still expanding. The result of this development and evaluation process is a rapid increase in understanding of charge-coupled devices and optimism for their widespread implementation in signal processing applications in the near future. Specific examples, resulting from a series of studies and analyses, are described briefly in the following paragraphs.

MTI clutter rejection

The clutter signal received by a radar is energy reflected from pseudo-stationary and moving objects such as terrain, weather formations, and man-made objects such as chaff. The clutter echo normally encountered in radar applications is many orders of magnitude larger than the desired target return and has the characteristics of many scatterers individually fluctuating in random patterns but with an overall average directional drift or velocity. The return from a clutter patch or volume thus has associated with it a spectral width that depends on the particular type of reflecting clutter, and an average doppler that depends on the transmitted frequency and the average radial velocity of the clutter mass relative to the radar platform.

The object of MTI (moving-target indicator) clutter-rejection signal processing is to operate on the composite radar return to reduce the clutter power and improve the resultant target detectability. The technique for selectively rejecting the clutter, but not the moving target, is to discriminate on a doppler-frequency basis. This may be accomplished by designing a filter that rejects the doppler-frequency band occupied by the clutter power spectrum while passing all other frequency components.

One configuration particularly well-suited to a CCD implementation is the tapped delay-line class and is a member of the non-recursive sampled data filter configuration. An elementary form of an MTI filter is shown in Fig. 3. It is a delay line with a single delay element and is known as a two-pulse or a subtraction canceller. The delay interval, τ, is precisely equal to the radar pulse repetition interval (PRI).

An experimental two-pulse ($N = 2$) transversal MTI filter was constructed to evaluate the applicability of CCD delay lines to clutter-rejection cancellers. The devices used were 128-stage p-channel with a 45-dB dynamic range. The sample rate used for all the experiments was 1 MHz; performance goals included a 40-dB cancellation ratio and a 1-μs resolution cell.

The block diagram of the experimental CCD - MTI is shown in Fig. 4. Normal phase-detected video is presented simultaneously to the delayed and undelayed channels (signal paths). The input amplifier, K_1, was used to compensate for gain variations between the CCD delayed channel and the undelayed. The signal output of a CCD, as described previously, consists of the phase-one clock with the desired output additively combined. The purpose of the sample-and-hold circuit (S/H) was to eliminate the transient effects of the phase-one clock and to provide a relatively "clean" reconstruction of the delayed input signal to the differential subtractor. The transfer function of this configuration is

$$H(\omega) = a_0 - a_1 \exp(-j\omega t)$$

With a_0 and a_1 equal to unity, i.e., equal channel weighting, $H(\omega)$ has the characteristic sine-rectified waveform characteristic with attenuation nulls at integer multiples of $(1/\tau)$.

A number of experiments were conducted on the CCD MTI, with device performance optimization as an initial objective. Clocking waveforms of the type shown in Fig. 5 were applied to the CCD phase clocks. In addition, the time position of the sample-and-hold control pulse (Fig. 6) was selected to maximize the recoverable signal to noise. Results of these experiments indicated the following p-channel, 128-stage, surface-channel device parameters:

Dynamic range	>45 dB
Sample rate	>10 MHz
Transfer efficiency	≅99.98%
Minimum signal level	≅10 mV

Dynamic testing consisted of applying sinusoidal and pulsed waveforms to the CCD MTI input. An experiment of particular interest was conducted by sweeping the input sinusoidal signal over many octaves and multiple comb-filter notch positions. The waveform indicated in Fig. 7 is the canceller response to the swept frequency input. The nulls of the

cancelled output are positioned at multiples of 7.8 kHz. The theoretical nulls calculated from Eq. 1 are:

$$f_{nulls} = \frac{(1,2,\cdots,\infty)}{(1/f_c)\,(M)} \qquad (2)$$

Where f_c is the phase clock rate and M is the number of delay-line stages. It is clear that the null positions can be changed by altering either the clock sample rate or the number of delay stages.

Measured performance on the CCD-MTI indicated a minimum null residue consistent with a cancellation ratio of 36 dB. This result is in close agreement with the transfer efficiency of 99.98% and the 128-stage length; in general, the results to date are encouraging. The CCDs operated reliably and at a level of performance suitable for many radar systems. Continuing CCD development to improve speed, dynamic range and efficiency will appreciably expand their applicability in a number of areas related to signal processing problems.

CCDs for matched filtering

The work described in this paper represents part of a continuing program to apply charge-coupled devices to appropriate elements of radar signal processing. It is anticipated that CCDs will have their greatest impact in the pulse-compression area, since matched filters are generally the highest cost subsystem in a radar signal processor. As an example, current studies and analyses indicate a very real potential for CCD application in conjunction with recent advances in pulse-compression techniques.

The RCA-developed linear fm pulse-compression technique, termed the step-transform process, was developed into a highly efficient design which resulted in a 50% reduction in hardware over previously known FFT convolution approaches. An analysis of the step-transform process, in turn, indicated that additional significant reductions in hardware could be achieved by performing the discrete Fourier transform (DFT) functions required in the step-transform process with the chirp-Z transform (CZT) algorithm. The CZT is a method for performing the DFT using

Fig. 3 — Two-pulse MTI canceller.

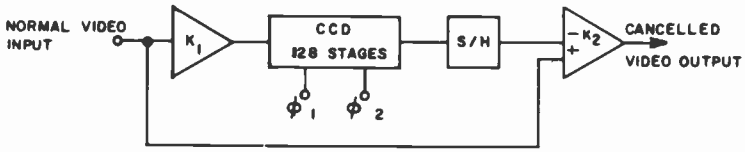
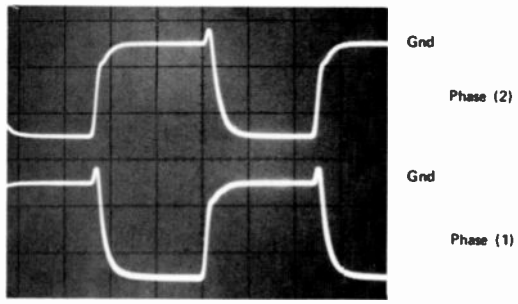
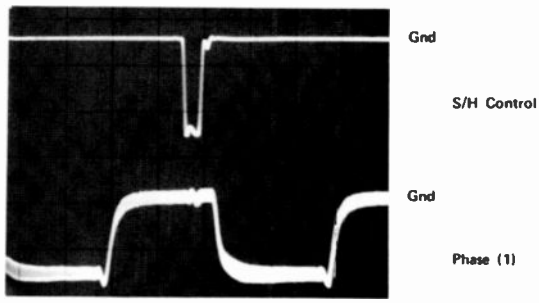


Fig. 4 — CCD two-pulse canceller.



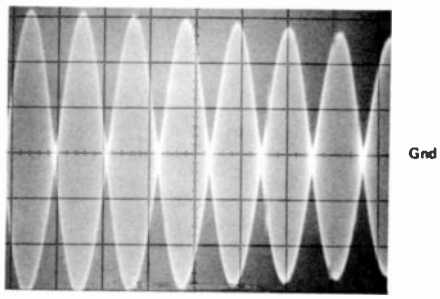
Verfical = 5.0 V/Div.
Horizontal = .2us/Div.

Fig. 5 — CCD bi-phase clocks.



Vertical = 5.0 V/Div.
Horizontal = .2us/Div.

Fig. 6 — S/H control pulse (and) phase (1) clock (inverted).



Vertical = 0.2 V/Div.
Horizontal = 2.5 ms/Div.

Fig. 7 — CCD — MTI output for a swept frequency input.

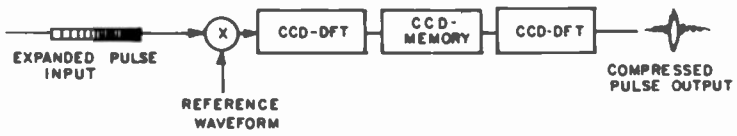


Fig. 8 — CCD step-transform processor.

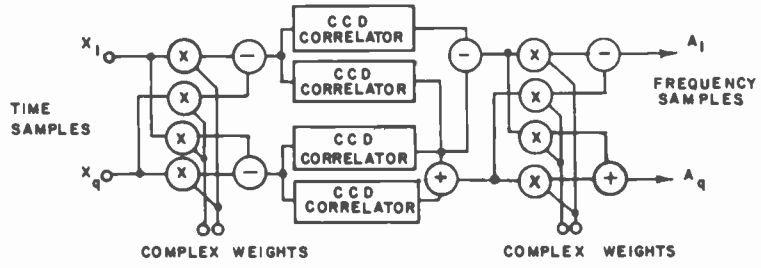


Fig. 9 — Chirp-Z transform approach for performing the discrete Fourier transform.

weighted tapped delay-lines[8]. The results of this analysis and a recognition of the unique CCD hardware saving properties applicable to the CZT and the step-transform process, form the basis for the continuing matched-filter development program.

Fig. 8 is a block diagram of the CCD step-transform processor. The step-transform algorithm functionally operates by mixing the expanded pulse video input with a frequency-ramped reference waveform. The effect of this mixing is to convert the long-duration input linear fm waveform into a staircase waveform with individual "steps," each of duration much less than the expanded pulse length. The first CCD-CZT operates on the contiguous steps and enters the spectral coefficients associated with each step into the recorder CCD memory. The second CCD-CZT operates on appropriately selected spectral samples from each of the steps across the entire waveform and provides a coherent weighted sum at the output. A square-sum combination of the real and imaginary output channels provides the compressed pulse output.

The most important subsystem in the CCD step-transform processor is the CCD-CZT (Fig. 9). The chirp-Z transform process involves premultiplication of the input time samples by weight vectors of unit magnitude and phase angles which exhibit a quadratic phase progression across the N-sample aperture. The CCD correlators convolve the phase-weighted input samples with a complex chirped impulse-response function of the form

$$h(t) = \cos(n^2 / N) + j \sin(n^2/N) \qquad (3)$$

$$(n = 0,1, \cdots, N-1)$$

Outputs of the complex convolution are phase corrected in the output complex multiplier to give the CZT spectral coefficients.

Fig. 10 presents the block diagram of the CCD step-transform processor currently under consideration. The half-aperture delay is provided to facilitate a continuous matched-filtering process. A particularly noteworthy feature of the proposed system is the combining of weighting functions and multipliers as compared to a straightforward use of two subsystems of the type shown in Fig. 9 in the system of Fig. 8.

The two reference storage memory locations combine the DFT weighting coefficients, reference waveform, and sidelobe suppression weighting. This functional combination results in a very efficient hardware implementation approach.

Conclusion

The application of charge-coupled devices to radar signal processing is still in its infancy. The applications of the device, to date, have tended to be as replacement components for more costly alternative implementations. The experience gained in the design of the MTI transversal filter described herein, and the noteworthy advantages evident in the chirp-Z step-transform processor analysis, are important indicators of expected future success in applying charge-coupled devices over a wide range of signal processing problems.

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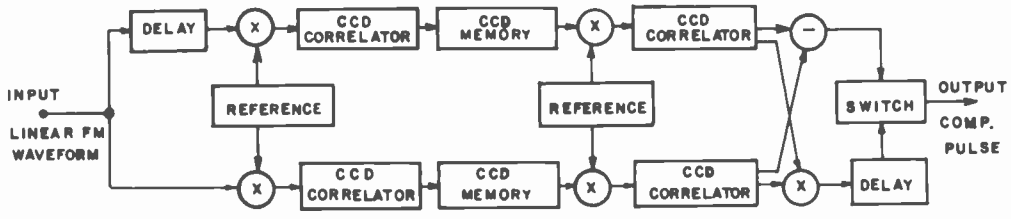

Fig. 10 — Implementation block diagram—CCD step-transform processor.

TESTGEN: An interactive test generation and logic simulation program

H. I. Hellman

Digital logic devices such as plug-ins, LSI chips or complete assemblies require testing procedures to insure proper operation. Past practice involved construction of a final assembly or a breadboard for testing and checkout. On this basis, the engineer specified a factory testing procedure; the process was usually costly, and in addition, a breadboard of an LSI chip may be impractical. The stumbling blocks are overcome by TESTGEN, a program to assist engineers in determining the accuracy of logic designs using simulation techniques. A complete set of test patterns may be derived which insure that the majority of all possible faults are detected. With the advent of LSI and MSI, the need for logic simulation and test pattern generation increased significantly. Programs such as TESTGEN, can virtually eliminate costly design errors prior to chip fabrication and logic assembly.

AUTOMATIC GENERATION of tests for combinational logic is presently available to RCA engineers. The original program called AGAT[1] has been greatly expanded; the latest version (XAGAT) is currently used to automatically generate tests for combinational logic nets, together with a fault dictionary. An improved method of path sensitizing, generally refererred to as the D algorithm,[2] is included; a manual describing the program operation is available.[3].

A parallel fault simulator (FLTSIM) for sequential logic circuits was subsequently developed.[4] FLTSIM performs both logic validation (good logic simulation), and fault simulations based on test sequences determined by the user; a manual describing program operation is cited in Ref. 3. To permit more accurate race-and hazard-analysis, a three-value simulator (SIM3V) was developed.[5,6,7] The techniques developed in SIM3V and FLTSIM permitted derivation of an expanded three-value fault simulator (EFLTSIM).

TESTGEN

The cumulative experience and background gained from the earlier programs led to the most recent program, TESTGEN, which is the subject of this paper. A user's manual and some notes describing TESTGEN are cited in Refs. 8 and 9; in Refs. 10 and 11, several TESTGEN users describe their experiences in the use of the program. For more background information on test generation, there are two good reference books available.[12,13]

General operation

TESTGEN, an interactive test generation and logic simulation program, operates on the New Time Sharing System (NTSS) at David Sarnoff Research Center, Princeton. Most RCA divisions are presently using the program via a telephone line in conjunction with a time-sharing terminal. The program operates by asking the user to enter answers to a number of questions at the terminal; these include:

1) Location of logic data file,
2) Assigned problem number,
3) Location of test pattern file,
4) Nodes to be observed,
5) Flip-flops and/or latches to be initialized,
6) The sequence of patterns to be simulated,
7) Data printout option, and
8) Fault option.

Such questions are posed as the need arises so that the program can check the validity of the successive responses. When an error occurs, an error message is printed; major errors must be corrected before proceeding. However, in many instances, this requires only a few minutes of analysis and is superior to a computer batch run where a lag of several hours or more interrupts the engineer's continuity of thought.

Another advantage of the time sharing system is the use of intermediate data storage files. The user may stop at some convenient point, store the data, and resume at some later time at his convenience.

The NTSS system includes an excellent *Editor* which rapidly enables the user to make extensive modifications to his field and search for unique data strings (e.g. element #307). There is also a DO mode which permits the user to store a series of responses to questions by TESTGEN on one or several files. Thus, when responses

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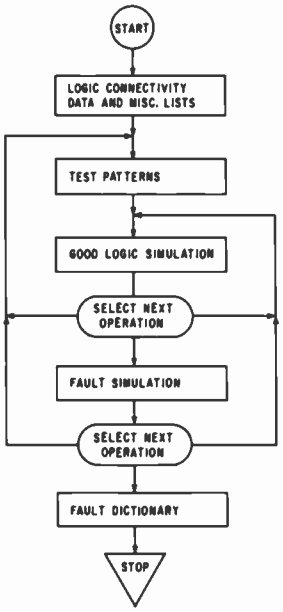

Fig. 1 — TESTGEN flow chart

are always the same, the user is spared the trouble of repeating these responses during successive call-ups of TESTGEN.

The user can choose various options and direct the program operation sequence at various points throughout the program. Several options and features provided by TESTGEN are described later.

The various sections of TESTGEN

TESTGEN consists of the following sections:

1) Logic connectivity,
2) Test patterns,
3) Good logic simulation,
4) Fault simulation, and
5) Fault dictionary.

The flow chart showing the various TESTGEN sections is shown on Fig. 1. The program reads the logic connectivity from the data file specified by the user, and performs a number of error-checking operations. If these are performed satisfactorily, several lists are generated for both internal program use and, optionally, external-user use. After the user selects one of several available fault options, the corresponding fault lists are generated for subsequent use in fault simulation.

Test patterns are required prior to simulation. The user has several options available. Test patterns may be entered either manually or from an external file; they may be appended to the data file; or, they may be generated using a semi-automatic mode. The sequence in which patterns are entered does not necessarily need to correspond with the sequence in which patterns are to be executed.

Good logic simulation is performed using a three-value simulator (0-1-X). All elements are initially placed in an X (i.e. unknown) state — and the user may select any of several available techniques for initialization. The user may initialize flip-flops and latches, or apply a sequence of test patterns to initialize the logic. Subsequently, test pattern sequences are selected to verify that logic responses are in accordance with the designer's criteria. If any races appear during the simulation, the user is immediately notified and may request a detailed RACE ANALYSIS.

When simulation is lengthy, or when a user wishes to analyze the simulation data before proceding, the last state of the logic may be stored in a file. At a subsequent interactive session, the file may be recalled, and simulation can be continued from the last state.

After the user is satisfied with a good logic simulation, fault simulation may be performed. The number of faults simulated depends on the size of the logic net and the fault option selected. The fault simulator will handle a group of 128 faults simultaneously for all test patterns. After all fault groups are simulated, a summary score is printed, including a list of faults which have not been tested by the selected test patterns. The user may store the fault simulation data, and analyze the untested faults to determine the additional test patterns needed. When additional patterns have been determined, the sequence of good logic simulation and fault simulation may be performed. Optionally, only the untested faults may be selected for further fault simulation at this point.

After each fault simulation, the user has the option of printing the fault dictionary prior to the termination of the current run. The fault dictionary contains a number of pass/fail patterns, where each pattern corresponds to one or more faults. When the test patterns are used to check a logic network using a testing device, and a fault is found, the pass/fail pattern which most closely corresponds to the operation of the unit under test will identify the faulty node.

Logic connectivity

TESTGEN requires logic connectivity to be entered as a series of records on the NTSS data file, where each record describes a single logic element. The following logic types are included:

Gates: AND,NAND,OR,NOR
Latches: RS,DL
Clocked flip-flops: JK,D,T,RS
Miscellaneous: EXCLUSIVE OR, DELAY

The delay element is available for use in logic nets where delays have been designed into the logic to avoid races and hazards. All of the flip-flops and latches have direct set/reset inputs which can be selected at the user's option; inputs are simulated as macro elements using Boolean equations. The clocked flip-flops are assumed to have two state variables similar to a master-slave operation mode.

When special flip-flops or other logic configurations are used repetitively, a MACRO consisting of standard logic element types may be used to represent the special logic configuration. A program called MACRO will automatically generate the logic connectivity data for use with TESTGEN.

The three-value simulators

Both good logic simulations and fault simulations are performed using a three-value simulator. The allowable levels are 0, 1, and X, where the X state represents either an unknown level, or a level in transition (0 to 1, or 1 to 0). Boolean operations conform to the rules shown in Fig. 2.

Simulation is performed using an activity vector (selective trace) technique. With this method all changed primary inputs are set = X and a list of their successors (loads) is generated. These elements are simulated, and all elements whose outputs change from the previous state form the basis of the next activity vector. This

AND	OR	NOT
X.X = X	X + X = X	X' = X
X.0 = 0	X + 0 = X	0' = 1
X.1 = X	X + 1 = 1	1' = 0
0.0 = 0	0 + 0 = 0	
0.1 = 0	0 + 1 = 1	
1.1 = 1	1 + 1 = 1	

Fig. 2 — Three-value simulation Boolean logic rules.

is equivalent to propagation of X's through the network and is defined as an X simulation. This operation continues until there are no further changes. At this time, the primary inputs are set to their new values, and a value simulation is now performed.

This technique has the capability of determining potential races within the logic. It will uncover *spikes* which may cause a latch or flip-flop to go to an indeterminate (X) state.

The clocked flip-flops are special Boolean equations which assume that there is an internal delay between the master and slave section of the flip-flop. This avoids the problem usually found with three-value simulators which use gate level representation of clocked flip-flops and the need for addition of delay elements. It should be noted that spikes occurring at the synchronous inputs will be detected. In addition, races occurring at asynchronous inputs (direct set/reset) will propagate to the flip-flop outputs.

Race/hazard analysis

Races in sequential logic nets may be caused in several ways. In some cases, two primary inputs changing simultaneously may cause the races. In other cases, the logic may have been designed so that changing a single primary input (such as a clock line) causes a spike at the input to a latch or a flip-flop. (It should be noted that a spike or race in only combinational logic is not considered a race by TESTGEN). When a race is detected, the user may request a RACE analysis at that point in the simulation. The terminal will print each group of 50 nodes on three consecutive lines, as follows:

1) Test # — Levels at nodes for preceding test.
2) X simulation — X simulation of pattern causing the race.
3) RACE/HAZARD — Value simulation of pattern causing the race.

If a spike on the input to a flip-flop or latch is the cause of the race, one or more of the following vertical bit patterns are found:

	Spike	Spike
1) Test	0	1
2) X simulation	X	X
3) RACE/HAZARD	0	1

The particular latch or flip-flop affected

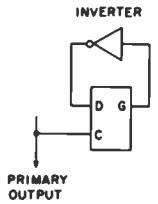

Fig. 3 — Spike detector — Initialize clocked D, FF to 0 (or 1). If spike occurs on primary output line, FF goes to X state.

by the race will be seen as an X on the RACE/HAZARD line. When a race is detected, corrective action is required by the user. If two primary inputs are changing simultaneously, insertion of an additional pattern will usually correct this problem. If only a single input is changing, the user should analyze his circuit for possible improper design. When analysis indicates that a delay is required, this element can be added to the logic connectivity at the appropriate location.

The delay element operates in the same manner as the built-in delay for the clocked flip-flop. During the X simulation, the propagation of the X level is stopped at the input of the delay element. This has the effect of masking all races beyond the delay element, and the user is cautioned to carefully analyze its effect.

There are instances where a spike on a primary output may affect sequential logic driven by the primary output. A dummy spike detector can be added at the primary output to detect this condition (see Fig. 3). An available option permits spikes to be checked at all internal and output nodes. This option eliminates the need for the dummy spike detector.

Fault simulation

A faulty network is assumed to be a good network containing a single fault. A fault is defined as either an element output (or an input) stuck-at-one (SA1) or stuck-at-zero (SA0). Fault simulation is speeded up by simulating up to 128 faulty networks simultaneously. Since races may occur in faulty networks, the three-value fault simulator is very useful in detecting races.

When input faults are optionally selected, fault collapsing is automatically applied. Here, all input faults, indistinguishable from element output faults, are deleted. (For example, in the case of a NAND gate, an input node SA0 is indistinguishable from the output SA1).

In fault simulation, the test-pattern sequence applied for good logic simulation is applied to the faulty networks. When one or more primary output levels on the good logic network and a faulty network differ for any test pattern, the single fault of the faulty network is assumed to have been tested.

For large networks having more than 1000 faults, simulation costs may become very significant. This network will require at least 8 consecutive fault simulation passes (1000/128) and several features have been included to reduce costs.

After fault simulation has been executed, the user may opt to simulate only untested faults. Another available option is to select a smaller subset of all possible faults most likely to fail. The user may decide to use a BATCH version of TESTGEN where a computer run cost is approximately 30% to 40% of the equivalent interactive computer cost.

Initially, fault lists are established for all assumed faults. As each fault is tested, the fault lists are updated. The user has the option of printing and/or saving detailed fault data in a file. In this case, during each fault simulation pass, the faults tested at each primary output for each test are listed. A corresponding option pertaining to races caused by faults is also available. Here, the faults which cause races and propagate an X level to primary outputs are listed for each primary output and each test. The race information may explain to the user why certain faults were not tested.

The fault simulator initializes all faulty networks to an X state. At the end of a fault simulation run, when the user desires to continue testing only untested faults, the state of the untested faulty networks must be extracted from each group of 128 initial faults. Since this is a complex operation and would require a large amount of computer time, the present version of TESTGEN requires the user to reinitialize the new sets of faulty networks (i.e. an initialization test sequence is required).

An option is available to the user to retain initialization in subsequent fault simulations. Here, the state of all faulty networks is saved in an external file.

When delay elements are used, the X values are inhibited from propagating

during the X simulation. This causes the three-value simulator to behave as a two-value simulator and the circuit may not reach a steady state during the value simulation. Such an oscillation case (determined by an iteration counter) and the nodes in the oscillation loop are printed. Oscillation problems may occur frequently during fault simulation in one or several faulty networks. When the oscillation state is detected during fault simulation, the nodes of the faulty networks (in the oscillation loop) are changed to an X state and the fault simulation continues to the next test pattern.

Initialization

Initialization of a sequential logic network can be a major problem. If a master reset (clear) is made available in the logic, test generation problems are eased considerably. In the case of LSI chips, a designer, attempting to pack a maximum amount of logic on a single chip, may find that a master reset is a luxury. In these cases, it may be necessary to use up to several hundred test patterns before all logic goes to a known state.

TESTGEN permits an unlimited number of initialization test patterns. To avoid a "runaway" condition, the program asks the user every 16 patterns for permission to continue.

Lengthy initialization sequences also cause a significant increase in fault simulation costs since the state of each faulty network must be simulated. In the case where a faulty network cannot be initialized, the fault simulator cannot be certain whether the fault has been detected since the primary output of the faulty network remains in an X state.

If an X state type of fault is present, when a logic unit is tested, a primary output may be in the correct state at test No. 1. The fault simulator has an option permitting faulty networks in the "X" state at test No. 1 to be initialized to the *good logic state*. With this assumption, the fault will be detected when the primary output is supposed to change state on the next logic transition. If the primary output is in the incorrect state at test No. 1, it is detected at that point.

Race and oscillation analysis circuit

A latch spike analysis circuit is shown in Fig. 4; the latch is reset in its initial state and a 1 to 0 transition is applied at terminal 1. It can be seen that the output of element #7 will depend on the delay element, as follows:

Run #	*Delay element unit gate delays*	*Output element #7*
1	1	Negative spike
2	2	Negative pulse: width=1 gate delay
3	3	Negative pulse: width=2 gate delays

These three cases have been run on TESTGEN and the results are shown in Figs. 5, 6, and 7 respectively. The *Simulation Test Data...Levels* indicates the state of 9 nodes on each horizontal simualtion line. (nodes 3 and 4 are always

```
ENTER...(1) DSET# ?11-20? (2) PROBLEM CODE PRxx **>>11,PR02
PR02   ***LATCH SPIKE ANALYSIS***
PRINT LOGIC DATA?.ENTER 2=LOGIC NET ONLY;1=ALL;0=NONE**>>0
PREVIOUS SIMULATION DATA SAVED?...ENTER DSET# ?90-99?=YES;0=NO**>>0
ENTER FAULT OPTION#...1=PRIMARY INPUTS & OUTPUTS +FLIP FLOPS
 2=SELECTED LISTS OUTPUTS; 3= ALL OUTPUTS; 4=ALL OUTPUTS & INPUTS
 5=SELECTED LISTS OUTPUTS & INPUTS**>>1
TEST#  0 ;CPU TIME=    4.57 SECONDS;   09:01:35

# NET INPUTS=  2; # GATES=  5; # LATCHES=  0; # CLOCKED FLIP FLOPS=  0

FAST/NO X PRIMARY INPUTS USED?...ENTER 1=YES; 0=NO**>>0

 LIST OF NET OUTPUTS
   8   9
ENTER # UNITS DELAY (1-16) FOR DELAY ELEMENTS**>>1
PRINT LIST OF UNTESTED FAULTS?...ENTER 1=YES;0=NO**>>0
SELECT TEST MODE...0=DSET#;1=MANUAL;2=SEMI-AUTOMATIC**>>0
   4 TESTS ENTERED FROM DSET#
TEST PATTERN SELECTION.....LAST PATTERN#=   4
EXAMPLES...17,26?17A26?; 12,-32?12 THRU 32?; 7,0??;END?; 0,9?END?
  ***TO REPEAT PREVIOUS RANGE N TIMES, ENTER  0,N ***
ENTER 2 TEST NUMBERS**>>1 2
ENTER 2 TEST NUMBERS**>>3 0

PRINT TEST PATTERNS?..ENTER 1=YES;0=NO**>>0
SELECT NEXT OPERATION...1= MODIFY PATTERN SELECTION
2= SELECT TEST MODE; 3= SIMULATION**>>3
TEST#  0 ;CPU TIME=    6.73 SECONDS;   09:04:00
PRINT X SIMULATION DATA?...ENTER 1=YES OR 0=NO**>>0
PRINT SIMULATION TEST DATA?. ENTER 0=NONE;1=ALL;2=PRIM. INPUTS & OUTPUTS
 3=PRIMARY INPUTS & SELECTED NODES;4=SELECTED NODES**>>1

SIMULATION TEST DATA...LEVELS
PATT#                5    10    15    20    25    30
  1 TEST    1 10101 0101
  2 TEST    2 11101 0101
  3 RACE/HZD 01100 1122
RACE/HAZARD ANALYSIS REQD?...ENTER 1=YES;0=NO**>>1
                       NEGATIVE SPIKE - NODE #7
          RACE/HAZARD ANALYSIS *****   NODES    1   -9
  2 TEST    2 11101 0101
X SIMULATION 21101 2222
  3 RACE/HZD 01100 1122
CONTINUE SIMULATION FROM LAST VALID TEST?...ENTER 1=YES;0=NO**>>
```

Fig. 5 — Run number one.

```
ENTER...(1) DSET# ?11-20? (2) PROBLEM CODE PRxx **>>11,PR02
PR02   ***LATCH SPIKE ANALYSIS***
PRINT LOGIC DATA?.ENTER 2=LOGIC NET ONLY;1=ALL;0=NONE**>>0
PREVIOUS SIMULATION DATA SAVED?...ENTER DSET# ?90-99?=YES;0=NO**>>0
ENTER FAULT OPTION#...1=PRIMARY INPUTS & OUTPUTS +FLIP FLOPS
 2=SELECTED LISTS OUTPUTS; 3= ALL OUTPUTS; 4=ALL OUTPUTS & INPUTS
 5=SELECTED LISTS OUTPUTS & INPUTS**>>1
TEST#  0 ;CPU TIME=    9.03 SECONDS;   09:07:16

# NET INPUTS=  2; # GATES=  5; # LATCHES=  0; # CLOCKED FLIP FLOPS=  0

FAST/NO X PRIMARY INPUTS USED?...ENTER 1=YES; 0=NO**>>0

 LIST OF NET OUTPUTS
   8   9
ENTER # UNITS DELAY (1-16) FOR DELAY ELEMENTS**>>2
PRINT LIST OF UNTESTED FAULTS?...ENTER 1=YES;0=NO**>>0
SELECT TEST MODE...0=DSET#;1=MANUAL;2=SEMI-AUTOMATIC**>>0
   4 TESTS ENTERED FROM DSET#
TEST PATTERN SELECTION.....LAST PATTERN#=   4
EXAMPLES...17,26?17A26?; 12,-32?12 THRU 32?; 7,0??;END?; 0,0?END?
  ***TO REPEAT PREVIOUS RANGE N TIMES, ENTER  0,N ***
ENTER 2 TEST NUMBERS**>>1,2
ENTER 2 TEST NUMBERS**>>3,0
PRINT TEST PATTERNS?..ENTER 1=YES;0=NO**>>0
SELECT NEXT OPERATION...1= MODIFY PATTERN SELECTION
2= SELECT TEST MODE; 3= SIMULATION**>>3
TEST#  0 ;CPU TIME=   10.91 SECONDS;   09:09:25
PRINT X SIMULATION DATA?...ENTER 1=YES OR 0=NO**>>0
PRINT SIMULATION TEST DATA?. ENTER 0=NONE;1=ALL;2=PRIM. INPUTS & OUTPUTS
 3=PRIMARY INPUTS & SELECTED NODES;4=SELECTED NODES**>>1

SIMULATION TEST DATA...LEVELS
PATT#                5    10    15    20
  1 TEST    1 10101 0101
  2 TEST    2 11101 0101
OSCIL. LIST; TEST#    3      9   8
OSCIL. LIST; TEST#    3      8   9
OSCIL. LIST; TEST#    3      9   8
OSCIL. LIST; TEST#    3      8   9
OSCIL. LIST; TEST#    3      9   8
OSCIL. LIST; TEST#    3      8   9
OSCIL. LIST; TEST#    3      9   8
OSCIL. LIST; TEST#    3      8   9
OSCIL. LIST; TEST#    3      9   8
OSCIL. LIST; TEST#    3      8   9
OSCIL. LIST; TEST#    3      9   8
OSCIL. LIST; TEST#    3      8   9
OSCIL. LIST; TEST#    3      9   8
OSCIL. LIST; TEST#    3      8   9
OSCIL. LIST; TEST#    3      9   8
OSCIL. LIST; TEST#    3      8   9
TEST#  3 ;CPU TIME=   12.44 SECONDS;   09:10:04
CONTINUE SIMULATION?...ENTER 1=YES;0=NO**>>
```

Fig. 6 — Run number two.

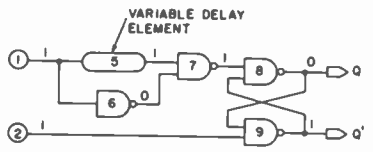

Fig. 4 — Latch spike analysis circuit (PRO2). Elements 6, 7, 8, 9 are *NAND* gates with unit delay; element 5 is a variable delay element.

logical 1 and 0). In each run, test #1 (input pattern 10) and test #2 (input pattern 11) are used to initialize the latch. Test #3 (input pattern 01) changes input #1 from 1 to 0.

In Fig. 5, a race is shown; the RACE/HAZARD analysis indicates a negative spike on node #7 (logic level 2 = X state). In Fig. 6, the circuit is oscillating at test #3; this is due to generation of a negative pulse 1 gate-delay-wide. Note that elements 8 and 9 appear on each successive activity vector due to the narrow pulse circulating within the 8-9 latch loop.

In Fig. 7 for run #3, selection of X simulation option 9 provides a detailed printout of each activity vector. (Each horizontal line indicates the activity vector for each successive unit of time = 1 gate delay). Of particular interest are the activity vectors labeled t_1 thru t_6 for test #3. The following should be noted:

a) Element #7 changes to 0 at t_2 and goes back to 1 at t_4. This is the negative pulse 2 unit gate delays wide.

b) Delay element #5 stays at 1 during the X simulation and changes to 0 at t_6.

c) Element #9 changes to 0 at t_4 and locks latch 8, 9 into the set state.

Summary

Some of the salient features of the TESTGEN program have been discussed. RCA engineers have access to the TESTGEN *User's Manual* which demonstrates some of the detailed operations and explains some of the detailed steps and possible techniques.

To enable the user to run very large logic nets and/or very long test sequences, there is a *Batch* version of TESTGEN available to the user. New techniques have been devleoped in an endeavor to create more cost effective fault simulators.[12,13] Techniques originally derived for use with combinatorial logic and latches may be used as the basis for a cost effective fault simulator for complex sequential logic.

Automatic test generation is a complex problem requiring solution, especially for large highly sequential logic nets requiring long initialization sequences[14]. A significant amount of effort and research is required to achieve this goal. Some previous research[15,16] indicates that a pure algorithmic approach should be combined with heuristic techniques in developing a cost effective automatic test generation program. At RCA there are many problems still to be solved; to keep pace with the very rapid increase in digital-logic technology; these include:

1) A more cost-effective fault simulator,
2) Automatic test generation for large logic nets (over 1000 elements), especially those requiring long initialization sequences,
3) More effective methods of storing fault dictionary data, and
4) Use of more cost-effective computer systems.

```
ENTER...(1) OSET# ?11-20? (2) PROBLEM CODE PRxx **>>11,PRO2
PRO2   ***LATCH SPIKE ANALYSIS***
PRINT LOGIC DATA?.ENTER 2=LOGIC NET ONLY;1=ALL;0=NONE**>>0
PREVIOUS SIMULATION DATA SAVED?...ENTER OSET# ?10-19?=YES;0=NO**>>0
ENTER FAULT OPTION#...1=PRIMARY INPUTS & OUTPUTS +FLIP FLOPS
 2=SELECTED LISTS OUTPUTS; 3= ALL OUTPUTS; 4=ALL OUTPUTS & INPUTS
 5=SELECTED LISTS OUTPUTS & INPUTS**>>1
TEST#  0 ;CPU TIME=   13.37 SECONDS;    00:13:39

# NET INPUTS=  2; # GATES=  5; # LATCHES=  0; # CLOCKED FLIP FLOPS=  0

FAST/NO X PRIMARY INPUTS USED?...ENTER 1=YES; 0=NO**>>0

 LIST OF NET OUTPUTS
   8   9
ENTER # UNITS DELAY (1-16) FOR DELAY ELEMENTS**>>3
PRINT LIST OF UNTESTED FAULTS?...ENTER 1=YES;0=NO**>>0
SELECT TEST MODE...0=OSET#;1=MANUAL;2=SEMI-AUTOMATIC**>>0
   4 TESTS ENTERED FROM OSET#
TEST PATTERN SELECTION.....LAST PATTERN#=   4
EXAMPLES...17,26?17A26?; 12,-32?12 THRU 32?; 7,0??;END?; 0,0?END?
  ***TO REPEAT PREVIOUS RANGE N TIMES, ENTER  0,N ***
ENTER 2 TEST NUMBERS**>>1,2
ENTER 2 TEST NUMBERS**>>3,0
PRINT TEST PATTERNS?..ENTER 1=YES;0=NO**>>0
SELECT NEXT OPERATION...1= MODIFY PATTERN SELECTION
2= SELECT TEST MODE; 3= SIMULATION**>>3
TEST#  0 ;CPU TIME=   16.10 SECONDS;    00:15:41
PRINT X SIMULATION DATA?...ENTER 1=YES OR 0=NO**>>0
PRINT SIMULATION TEST DATA?. ENTER 0=NONE;1=ALL;2=PRIM. INPUTS & OUTPUTS
 3=PRIMARY INPUTS & SELECTED NODES;4=SELECTED NODES**>>1

SIMULATION TEST DATA...LEVELS
PATT#              5    10
X SIMULATION 22102 2222
X SIMULATION 22102 2222
X SIMULATION 22102 2222
  1 ISEQ#  1 10102 0221
  1 ISEQ#  1 10102 0121
  1 ISEQ#  1 10101 0101
  1 ISEQ#  1 10101 0101
  1 ISEQ#  1 10101 0101
  1 TEST   1 10101 0101
X SIMULATION 12101 0101
  2 TEST   2 11101 0101
  2 TEST   2 11101 0101
  2 TEST   2 11101 0101
X SIMULATION 21101 2101
X SIMULATION 21101 2201
X SIMULATION 21101 2221
X SIMULATION 21101 2222
X SIMULATION 21101 2222
t1  3 TEST   3 01101 1222
t2  3 TEST   3 01101 1022
t3  3 TEST   3 01100 1012
t4  3 TEST   3 01100 1110
t5  3 TEST   3 01100 1110
t6  3 TEST   3 01100 1110
    3 TEST   3 01100 1110
SELECT NEXT OPERATION...1= SIMULATE ALL FAULTS;2= SIMULATE ONLY UNTESTED
FAULTS;3= SELECT TEST MODE;4= PATTERN SELECTION;5= SAVE DATA;
```

Fig. 7 — Run number three

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MOS array design: universal array, APAR, or custom

R.H. Bergman| M. Aguilera| G. E. Skorup

Design procedures for MOS arrays have undergone significant changes in the past several years. In addition to the increases in array size due to greater processing yields, and improvements in performance as a result of a variety of emerging and maturing processes, computer aids have been developed which simplify the sizable task of array design and layout. This article describes the three array design techniques currently in use in RCA and indicates the manner in which they use computer aids.

UNIVERSAL ARRAY (UA) is a digital LSI design and implementation technique that possesses the following attributes:

- Low initial design cost.
- Very short design and fabrication cycle.
- Even shorter error-correction cycle.
- Quickly and easily implemented by a logic designer without need for solid-state process familiarity.
- Applicable to small quantity production
- Custom definition of only a single mask level. All other masks remain the same from design to design.

The design or layout procedure is simply implemented with the following operations.

- Construction of a logic diagram annotated in logic elements as defined in the Universal Array standard-cell library.
- Manual placement of decals of UA standard-cell logic functions on a gridded mylar form.
- Drawing of interconnect lines between UA standard-cell logic functions.

Gordon Skorup, Solid State Technology Center, Somerville, N.J., received the BSEE from Milwaukee School of Engineering in 1945 and an Associate degree in Business Administration from the Evening Division of the Wharton School of Finance and Commerce in 1963. He has done work toward an MSEE at Drexel Institute of Technology. Mr. Skorup joined the receiver design section of the RCA TV Division in 1947, and worked on the design and development of both vacuum tube and transistorized television receivers. In 1961 the tv division was relocated and he was assigned first to the Projects Section of M&SR Division and then to the Advanced Technique Development section, where he investigated solid state and semiconductor laser simulation, transmission, detection and signal processing. From 1964 through 1965 he was the project engineer responsible for the development and design of prototype optical correlation equipment for undersea warfare. From 1966 to 1969 he has been responsible for all P-MOS applications and proposals in the M&SR Division. In 1969, he became a market planner for COS/MOS in SSD. In 1970 he joined the MOS Monolithic Application group in G&CS where he has been responsible for the design and application of P-MOS and COS/MOS Universal Arrays. This group became part of SSTC in 1972 where it is continuing and expanding its Universal Array design application efforts.

Richard Bergman, Mgr., Applications and Photolab, Solid State Technology Center, Somerville, N.J., received the BSEE from Rutgers University in 1953. After graduation he joined RCA and worked in Advanced Development and Advanced Technology activities until 1966. During this period he had responsibility for development programs in logic, ultrasonics, and high speed digital circuits. From 1966 to the present he has been involved in Large Scale Array Technology. His responsibilities have included: the development of tools to provide low-cost, quick turnaround LSI vehicles, circuit and logic simulation, and computer aids for array design. His activity has been responsible for the design, layout, artwork and mask fabrication of several hundred complex array designs employing PMOS, CMOS, SOS and bipolar technologies. In 1968, he assumed responsibility for a high quality photomask facility that produces large area high quality photomasks for LSI arrays. He is a member of Tau Beta Pi and Eta Kappa Nu.

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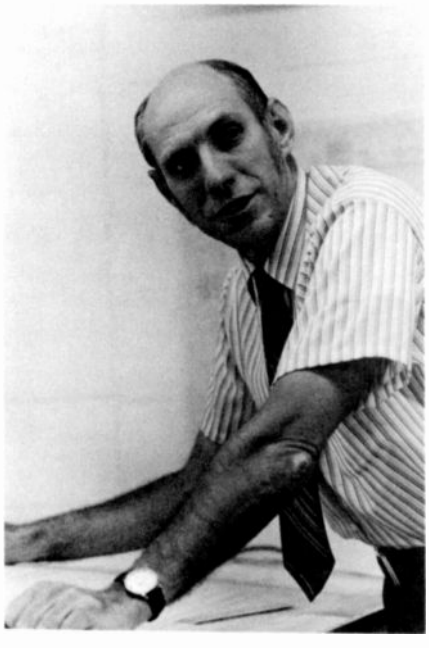
Manuel Aguilera, Solid State Technology Center, Somerville, N.J., received the BSEE from the Ohio State University in 1959. He joined RCA in June 1959 in the Airborne Systems Division to work on servo design for the BOMARC program. He was responsible for testing and evaluation of all semiconductor circuits for the RCA R100 computer. He designed P-MOS C-MOS LSI arrays while on loan to the Defense Microelectronics division. He joined the Roche Medical Electronics Division of Hoffman-LaRoche in June 1969 as an Engineering Leader. The design team under his direction designed blood pressure, neonatal, fetal and patient monitoring equipment. He returned to the SSTC division in December 1972 as a design engineer responsible for computer-aided design of LSI. He is a member of the IEEE and AAMI.



This completes the IC design or layout. From this information, artwork and masks are generated and devices fabricated. Additionally, a test program is defined that will specify the array logic inputs and expected outputs. A *Universal Array User's Manual* details all the steps required in designing, laying out, and testing a Universal Array. It contains a complete library of UA standard cell logic functions and static and dynamic device characteristics.

Universal array

The Universay Array (UA) consists of pMOS devices, nMOS devices, p+ and n+ tunnels, zener diodes, and pads placed in a fixed pattern on a silicon substrate. All drains, sources, gates, tunnel ends, and pads are accessible for interconnection with metal. In the COS/MOS process, normally seven mask levels must be made for each design. In the Universal Array technique, six of these mask layers are fixed for each array size. Only one mask level, the metal mask, is unique for each custom design. With this technique, a logic design engineer without semiconductor processing experience or knowledge of IC layout design rules can easily and readily originate his own unique large-scale integrated circuit (LSI). A family of several sizes of COS(MOS Universal Arrays has been designed containing from 82 to 276 gates.

Figure 1 shows the TCC 040 Universal Array (UA) and contains 138 UA cells (a UA cell contains two p and two n devices) in its interior and 30 other cells around its periphery. Actual size of the array layout form is 125 times actual chip size. At this scale, the grid line pattern (246 by 245 for the TCC 040) has a grid spacing of 0.1 inch or 10 lines to the inch. The TCC 040 has forty pads located around the periphery of the chip. Adjacent to each pad is a pMOS/nMOS pair; these pairs are normally connected to form an inverter for input wave shaping or for output buffering. Adjacent to these I/O devices and circling the internal cell area are two concentric metal rings which are used for +V and −V supply voltage. In the center area of the array is a repeated pattern of internal cells which are used for the bulk of the logic. Additionally, four very large devices can be seen in the periphery of the chip —one on each side. These are extra large devices to be used for driving TTL and other off-chip devices requiring large sink/source currents. Also, two pairs of high impedance devices are located on each of the four sides. These are useful for referencing floating input gates to either +V or −V. They may also be used as very slow inverters where long delay times are desired. In the lower left corner are located three large and eight small zener diodes for regulation uses. In addition, of course, there are the usual various alignment marks and test devices for processing and control purposes. Larger arrays contain more internal, I/O, and low-Z cells and more pads. Smaller arrays, likewise, contain less of each.

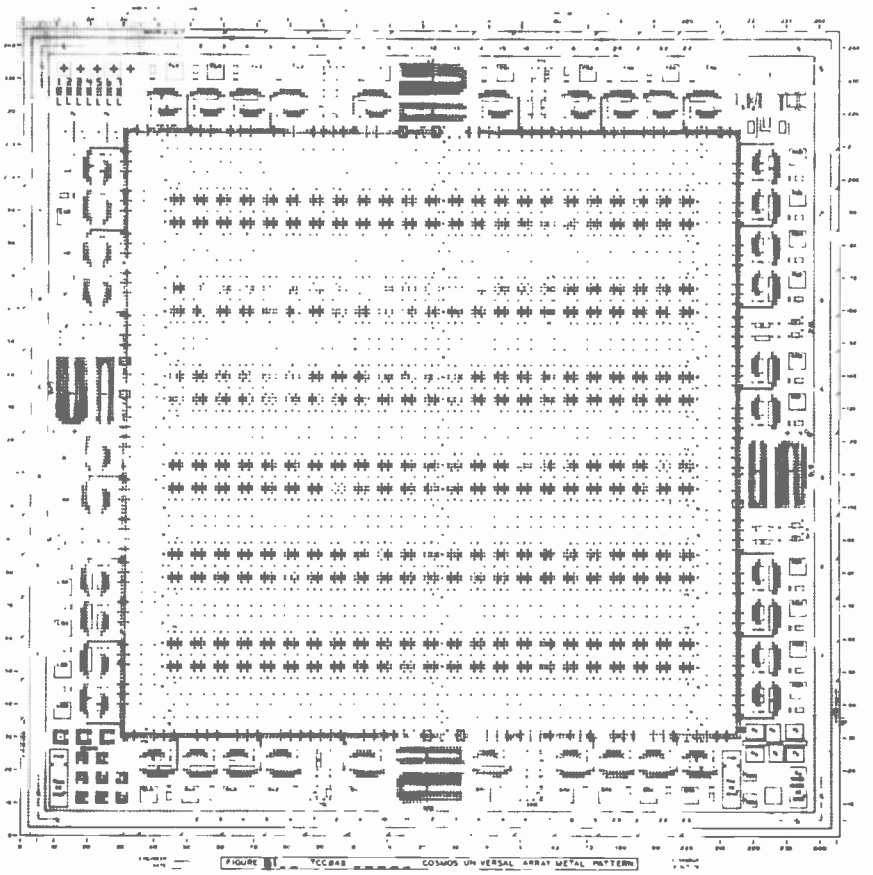


Fig. 1 — Typical 168-gate Universal Array metal layout form that shows chip content. the form is used for defining the customized metal layer.

UA standard logic cells

Key elements in the UA design technique are 1) the uniform grid structure for placement of metal lines and 2) the use of pre-defined interconnection patterns referred to as UA standard logic cells which define useful logic functions.

Since all device drain, gate, and source contacts are directly accessible, various circuit configurations can be implemented by proper metal interconnection. (See Fig. 2).

Each UA standard-logic-cell metal pattern is available on adhesive-backed decals for placement on a 125 × mylar layout form of the type shown in Fig. 2. Manual placement of decals is made in a manner which facilitates convenient interconnect between logic blocks. Manual drawing of lines on the grid structure completely defines connections between logic functions.

Design and artwork procedures

The procedure required to implement a UA is shown in Fig. 3. The first step (block 1), is to create a logic diagram that is annotated in logic cells from the UA Logic Cell Library. Such an oversimplified schematic is shown in Fig. 4. Each logic symbol contains three pieces of information. T' e top line is a unique Sequential Logic Block Number (*e.g.*, 104) assigned to that logic symbol. The middle line gives the UA Logic Cell Type Number (*e.g.*, 04g) and uniquely specifies a particular logic function. The bottom line indicates the location (*e.g.*, A21 and

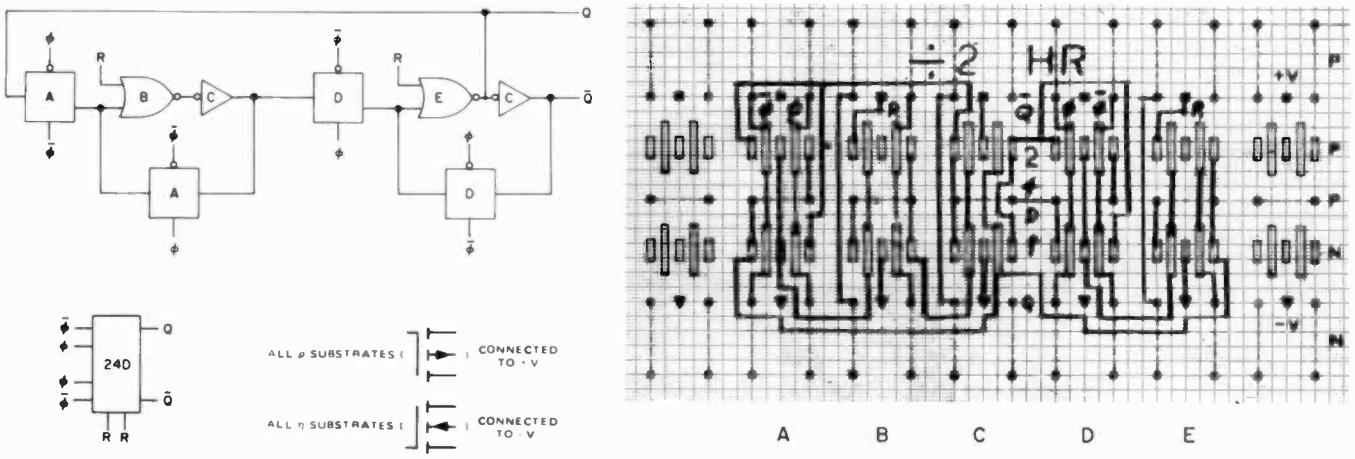


Fig. 2 — Circuit configuration for a binary divider with high reset, its metal interconnect pattern, and its logic symbol.

means row A, column 21) of that logic function on the UA layout form. Before a layout is actually made, the location of the cell, obviously, is not known. However, after layout completion, cell location is added to the annotated logic diagram. Cell location is most helpful during checking and testing. Other pertinent data such as Pad Designation, Package Pin Number, and Signal Name are also added.

From the annotated logic (block 1, Fig. 3), a layout (2) is made which is eventually converted to Gerber artwork with the help of several design automation aids. The metal pattern is defined on 125× mylar layout forms (2) by placement of adhesive-backed logic-cell decals and hand-drawn pencil lines.

A layout of the logic diagram is shown in Fig. 5. Logic cells 101, 102, 103, 104, 106, and 107 were defined by decals, while pencil lines were hand drawn to interconnect logic functions as desired. The layout is now complete. It is now necessary to capture the cell and interconnect information into a computer file for checkplotting, checking and artwork generation. Artwork information is presently captured or digitized, as in (3) of Fig. 3, via a design automation aid called a Graph Pen Digitizer. This apparatus consists of a "pen" and a table on which is laid the completed 125 × mylar layout form. By touching the tip of the Graf Pen at the start, corners, and end of each line, it generates an acoustic spark that travels horizontally and vertically to acoustic microphones which sense when the acoustic wave is received.

Time difference is measured and translated to physical distance across the layout. The resultant raw coordinate data is converted to PLOTS language, by running the ALACARTE program (5) resulting in a PLOTS file (7) located on NTSS. Conversion from PLOTS to DFL

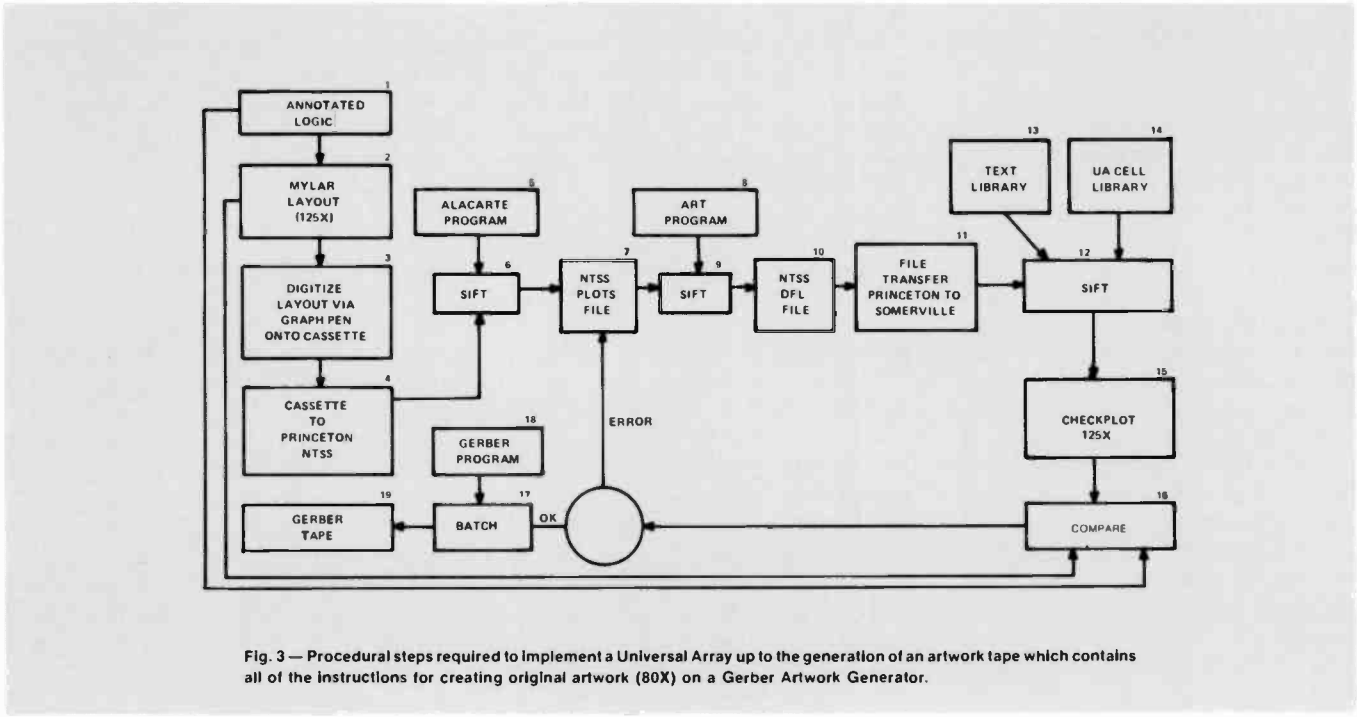


Fig. 3 — Procedural steps required to implement a Universal Array up to the generation of an artwork tape which contains all of the instructions for creating original artwork (80X) on a Gerber Artwork Generator.

(Design File Language), a machine language, is performed by running the PLOTS file through the ART program (8). The resultant DFL file (8) is then used to draw a checkplot of the layout to verify the accuracy of metal capture. The checkplotter is driven by a computer that SIFTS (12) a text library (13) and the UA cell library (14) with the metal connect information so that a complete checkplot of both UA logic cell and interconnect metal are present on the 125 × checkplot (15). Initial checkplotting is compared (16) with the original layout by direct overlay to obviate any errors of omission. Errors are corrected via editing of the PLOTS file and the loop is rerun for a second checkplot. When all obvious overlay errors have been corrected, a final check is made against the annotated logic diagram. When the checkplot is correct, the DFL file is run through the Gerber MAP program (18). The resultant Gerber tape (19) is used to operate a Gerber Artwork Generator which creates 80× artwork on glass.

Concurrent with the digitizing and checkplotting cycle, the logic system is duplicated on a hardware logic simulator which is also at 125 scale. It contains p and n devices in pattern locations identical to the mylar layout form. For each logic decal, there is an identical printed-circuit (PC) board which, when plugged into the hardware logic simulator, actually implements electrically the logic function of the decal. Jumper wires connect PC plug-in boards together on the same layout form. Inputs to the simulator are obtained from a logic tester. Predicted outputs are also generated by the tester. Comparison is then made between the predicted outputs from the tester and the actual outputs from the hardware logic simulator. This procedure verifies the circuit layout and the test pattern. Knowing that the test pattern is correct is particularly helpful when performing wafer testing of the fabricated chips. Software simulation and test generation programs are also used instead of hardware simulation and are described in another part of this article.

Future DA aids

Although the previously described procedure for capturing design information and for fulfilling testing requirements is effective, there are improvements that would further enhance

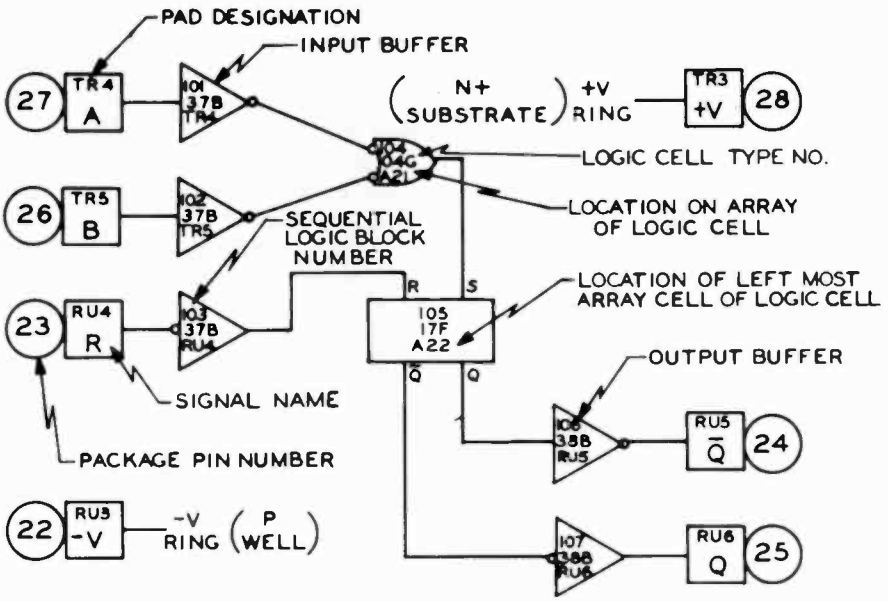


Fig. 4 — Sample logic format.

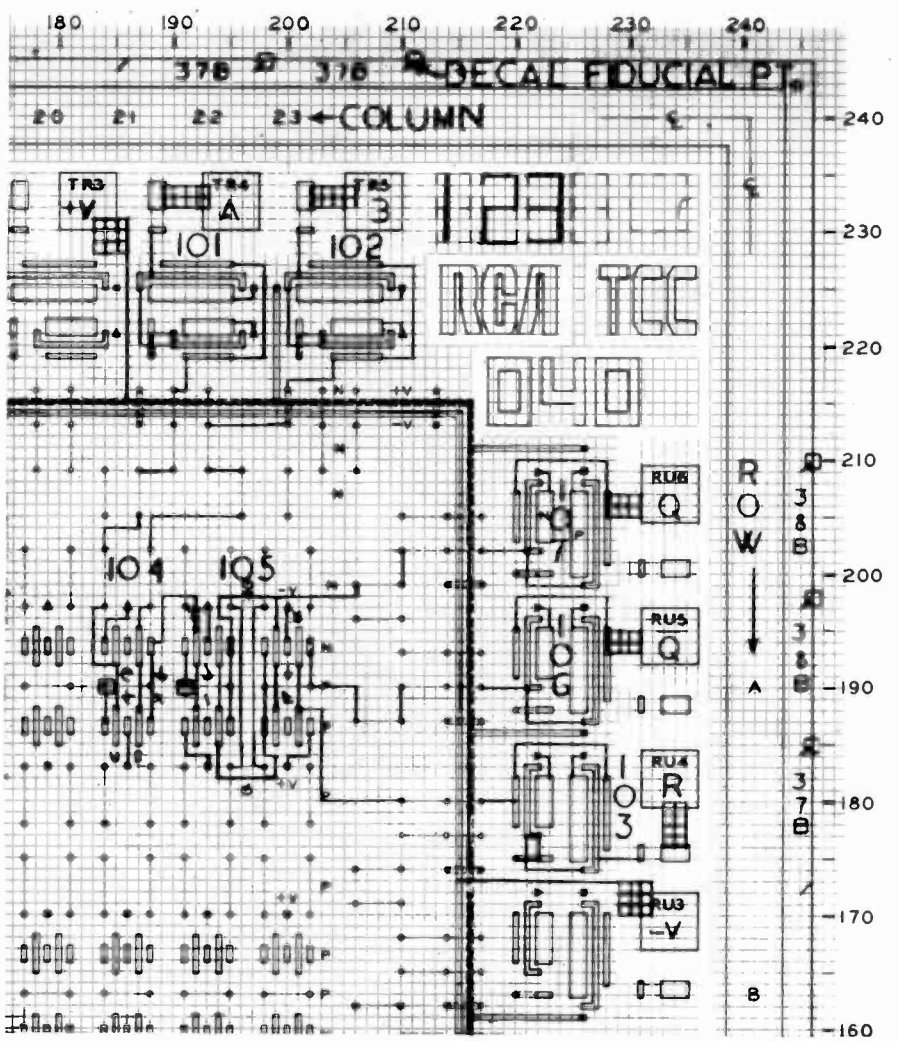


Fig. 5 — Metal pattern developed from sample logic format shown in Fig. 4.

the procedure. The present procedure requires an undesirable amount of time in queuing between differnt DA aids. In a "quick" turnaround design and fabrication cycle, this must be reduced to a minimum. Also, more efficient means of checking and testing are desired. An advanced UA digitizing, plotting, and testing system that is presently under development is shown in Fig. 6. In the figure, drawing the annotated logic diagram (1) and preparing the mylar layout (2) is the same as before. Digitizing (3) is done on a stand-alone interactive graphics system, called Applicon. The Applicon consists of a digitizing table, a computer, graphic display scopes, memory storage, and a drum plotter.

After digitizing into a data file, the file is run through the LOCCHK program (4) which verifies that all logic cells are properly placed and oriented. Any errors will be flagged. A checkplot (5) is then drawn from digitized data (3), and Text and UA cell libraries (6). It is originally compared against the mylar layout as before, but editing can be done interactively on the system by using a scope display. A second checkplot can then be made immediately and compared against the annotated logic diagram as a final check. Again, any changes can be made and checkplotted immediately. When the file is correct, it can then be run through the Gerber MAP program (7) to generate a Gerber tape (8) for 80× artwork generation. All blocks marked by an asterisk are performed on the Applicon system. The data file obtained in (3) can be run through the ARTCON program (9) to automatically generate a net list (10). When compared directly with the annotated logic diagram (1), it provides an alternative and even more desirable method of layout checking. The net list, together with the test pattern input (not shown), can be run through the TESTGEN program (11) to provide a test pattern that will be used for wafer and package testing. The ARTCON and TESTGEN programs would replace the hardware logic simulator now in use. The system shown in Fig. 6 will greatly reduce the time span between layout and Gerber tape and provide reliable patterns for device test.

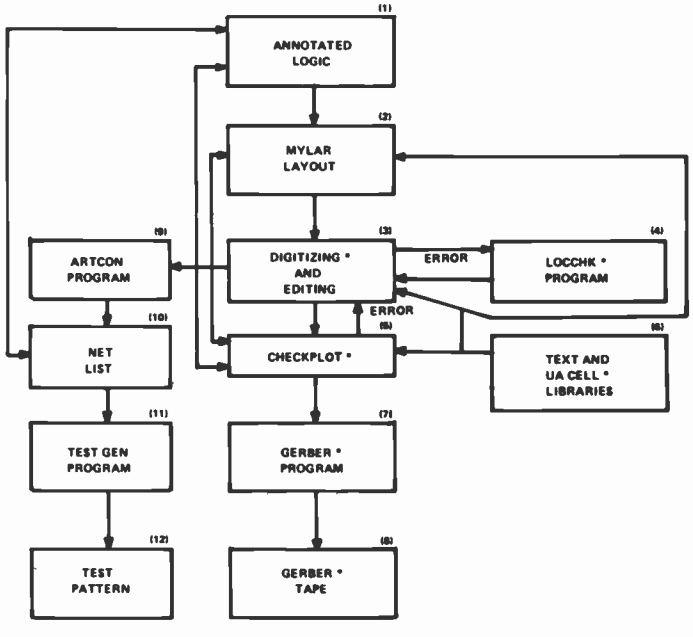


Fig. 6 — Advanced system for digitizing, plotting, and testing the universal array.

APAR

The APAR standard-cell LSI array system is a series of computer programs and design automation techniques that automatically translate a partitioned logic diagram into a set of instructions for driving an automatic plotter which generates precision mask artwork for complex LSI arrays of basic cells.

Two elements are basic to the APAR standard cell custom array approach:

1) Basic cell circuit libraries
2) Design automation (D/A) computer programs

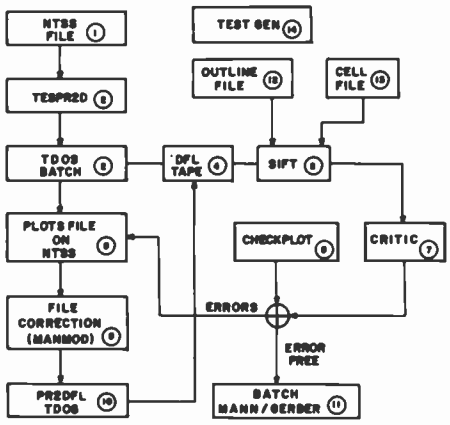


Fig. 7 — Operations required to produce LSI arrays. Flowchart also includes the computer programs and design aids that allow the basic APAR LSI system to adapt to a wide range of logic configurations, as well as to check and verify proper chip layout.

PR2DA
PR2DAE
PR2DFL
ART
MAP
CRITIC

The cell concept for producing LSI arrays begins with the design, layout, and validation of a group of custom circuits called standard cells. Once validated, the cells are given identification or pattern numbers and are permanently stored. To use one of these cells in a logic design, the user calls for the desired cell by pattern number. Nonstandard cells are also designed for particular jobs. The PR2D is then used to automatically generate the metalization and/or tunnels to interconnect the standard cells into the required logical functions. The computer programs accept the user's input in the form of a properly identified logic net list and produce, as an output, a magnetic tape and a file on NTSS that will result in the production of a set of instructions for driving an automatic plotter. The plotter, in turn, generates the artwork necessary to fabricate the array. The NTSS file in PLOTS language is used primarily for manual modification (MANMOD). The system flowchart is shown in Fig. 7.

Input data requirements

To use this system to produce LSI arrays, a user is required only to provide at the minimum a logic design which can be partitioned into APAR standard cells. The input data requirements for the artwork computer program are derived from the partitioned logic. This input data requirement includes the following

steps:

1) Copying of standard pin data file.
2) The sequential numbering of all the logic elements (pattern to gate file).
3) The generation of the net list showing the connectivity.

With the acceptance of this input data, the standard cell LSI array system then provides a low cost, quick turnaround capability for generating the mask artwork for the desired complex LSI array.

Standard cell library

The standard cell library is an open-ended collection of logic circuits implemented with the P-MOS, silicon gate or C-MOS technology. All standard cells have been defined, designed, topologically configured (in accordance with standard design and process rules), analyzed, and then permanently stored for future use on the NTSS system. The present C-MOS library is quite extensive and is designed to meet present and anticipated C-MOS implementation needs. However, it is also open-ended to allow the user to define and design new cells to meet unique future system requirements in the most efficient manner possible. P-MOS, SOS, and silicon gate libraries are still in the development phase.

The C-MOS standard cell data sheet (Fig. 8) describes the function and performance of each of the standard cells in the present family.

The standard cell databook also supplements the data sheet information with a brief description of such pertinent items as unique driving capabilities, undefined output states, and influences of output loading on clock rate. A means of estimating intercell wiring capacitance is also given. The data contained in these data sheets are based on a continuing program of circuit analysis, test array design and evaluation. RCAP (RCA Circuit Analysis Program) is used for the theoretical analysis of the complex circuits and yields an excellent basis for the evaluation of experimental data. To date, two test arrays have been fabricated and are being evaluated. A third array is in the design cycle. The goal of this program is to verify all information which is contained on the data sheets relative to our latest processing techniques.

Design procedure

The basic steps associated with processing an array through APAR are shown in Fig. 7 and include:

1) Preparation of NTSS file
2) Subjecting this file to TESPR2D
3) TDOS batch of this file
4) Preparation of DFL tape for sifting
5) Sifting the DFL tape with the appropriate file
6) Obtaining a checkplot
7) Running CRITIC
8) Storing the plots file on NTSS
9) Correcting the plots file (Manmod)
10) Running PR2DFL and
11) Batching the file for Gerber or Mann artwork.

The NTSS file(1) is the file which contains the necessary data for entry of a unique design into the PR2D program. This file will consists of the MODE card, Common Data Change cards, Array Header Card, Standard Pin Data File, Element-Pattern definition and connectivity list.

This file is subjected to the TESPR2D program (2) which screens it for correctness and indicates errors. Among the errors detected by this program are invalid element pattern assignment, invalid pattern number for an element, multiple use of an element, invalid node data, multiple use of element pins, too many bonding pads etc. In addition to the list of errors a summary of chip statistics is listed at the terminal which includes total linear mils, linear mils per row, projected maximum size and unused pins. Corrections or modifications to the file can be made which will insure that the file will be accepted by the PR2D program. The ability to make corrections based on the output of this program, which takes minutes to run, instead of waiting for an overnight batch, greatly reduces the lag time to correct errors.

After the successful running of TESPR2D the file is ready for batching on TDOS (Tape Disk Operating System) (3). The individual must add to the file the required job control list for running PR2D. The output of the PR2D program is in a language not compatible with the Plots or DFL languages. Therefore, a

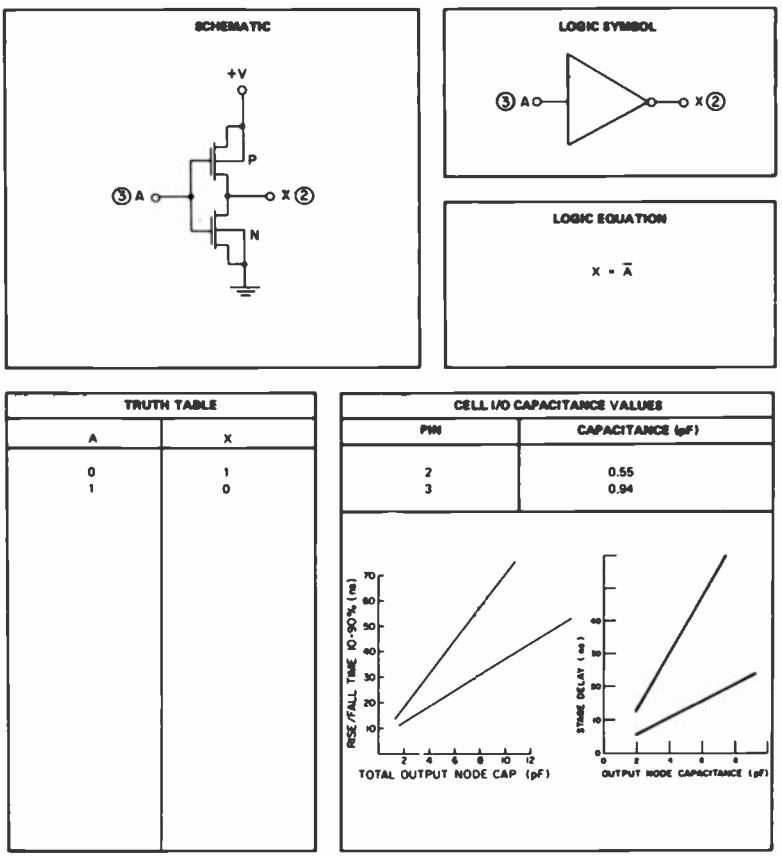


Fig. 8 — Typical C-MOS standard cell data sheet. Each sheet contains cell name, cell number, cell width, schematic diagram, logic symbol, logic equation, truth table, input and output capacitance at each cell, and delay characteristics *vs.* load capacitance.

conversion program is run during the batch which results in Plots and DFL files being written to tape. The Plots tape is read onto the users NTSS usercode and the DFL tape is sent to the users location.

This DFL tape is sifted (5) by the user with either the standard Outline file (12) or the Standard Cell file (13) dependent upon his requirements. The Outline file allows quicker plotting of the checkplot (6) and is used primarily for checkplots to be used for checking connectivity. The cell file is sifted when it is necessary to run CRITIC (7) or it is necessary to obtain a visual presentation of cell components in relationship to connectivity patterns.

The CRITIC program is run on a file which has been sifted with the cells of interest. The relation and width checks requested by the user are performed with an error listing and an error file made available. The user may use either or both to determine whether his file is error free. The user must use caution when requesting error checks as design rule checking is a time-consuming process.

The user must correct the plots file (8 & 9) which is resident on his usercode. The plots file is corrected because it is user oriented for ease of reading, understanding and editing. The file is corrected using standard NTSS editing procedures.

The corrected file must be converted from plots to DFL through use of the ART program (10). This may be done on NTSS or in Somerville on the checkplotter which contains a PDP-8 that is equipped with a version of ART. The loop from DFL tape through checkplot, file correction and ART must be repeated until an error free file is obtained.

When the user determines that his file is error free he batches the file on TDOS for either Mann or Gerber tape (11). The Mann tape or the Gerber tape can be processed to obtain useable artwork.

An optional feature of our present system is the capability for subjecting our design to test generation (TESTGEN, 14) and logic simulation (LOGSIM) programs. Testgen is an interactive test generation program for sequential logic which allows the immediate checking of test pattern validity or generation of a test pattern. The program has three modes of operation, DSET, Manual and Semiautomatic.

The program is available on NTSS, TDOS, and is being implemented on TSO.

Future design aids

A series of programs have been written for the processing of a common input file with either APAR, TESTGEN, or LOGSIM. These programs are grouped under the common name "COMPUTER AIDED DESIGN DATA BASE." These programs allow the user to encode an array once and through the use of a series of extraction programs construct input files for each of the three programs. This will greatly reduce the user input file preparation time and increase the use of the various programs.

Custom design

The custom design technique is the classic approach to implementing an MOS array. By the use of extensive manual procedures, a high-density, compact array can be achieved. This approach provides the lowest recurring cost for quantities of devices, but has the highest developmental (non-recurring cost).

Prior to the development of computer aids for array design, completely manual procedures were used in custom designs. Costs were high and turn-around times long. Changes in the design were difficult to implement, frequently requiring a redesign effort that was unacceptable to the customer.

Cell Approach

As computer aids became available, the majority of the custom designs for digital MOS logic were implemented using a cell library technique. A library of commonly used logic building blocks for a particular processing technology was developed. These "standard cells" were carefully laid out by hand to minimize area. The cells were then digitized and entered into the standard graphics (DFL) system. Each layout was carefully checked to establish the accuracy of its layout and performance. This cell library was then made available for array designs. These multi-ended cells are a prime reason for the smaller custom designs.

Custom design with cells

The array designer selects the appropriate cells to implement his logic. His layout consists of the placement of the selected cells in an efficient manner, and the interconnection of these cells to implement his logic. This approach results in considerable cost and time savings. Checkplots of cells are avaialble from automatic plotting equipment. The Digitizer Plotter System (DPS) or Applicon System can be used to digitize and checkplot new cells and enter them into the cell library. The designer can use the DPS system to call out the cells and plot them in their desired locations. Interconnections can be readily implemented on the DPS system. The editing features of the system allow the designer to move, add, or change components of the design as required. Interim and final checkplots are available as required to assist in planning and checking the layout.

At the completion of the layout task, the CRITIC program is availalbe to automatically check the design for layout violations. This automatic program is of considerable value as it methodically checks design rules, a task that is lengthy and prone to error when done by humans.

The checked design is automatically convered by computer program (ARTDWM) into an artwork tape (DW-Mann or Gerber) which is used to drive the automatic artwork generation equipment directly.

Summary

Computer aids have had a significant impact on custom array design. The impact has not been in the area of reduced chip size or increased performance, but rather in the areas of quicker design time, increased accuracy, and a reduction of high skill manpower requirements. These factors are essential to maintaining a competitive array capability.

Comparison of approaches

Density/cost

As has been described in the foregoing sections, the custom array design ap-

proach is the most expensive and time consuming approach of the three. It does provide, however, a more compact implementation that allows a considerable cost advantage when quantity pricing is considered.

The Universal Array approach and APAR approach are valuable techniques which reduce design time and design cost, but result in an array layout that is less efficient in area usage than the custom approach. As a general rule of thumb, the density of the APAR and Universal Array approaches are about 1/2 to 1/3 of the density of the custom design. The exact ratio depends upon the type of logic being implemented. The Universal Array is most efficiently used when the cell and interconnect areas available on the fixed format configuration are close to full use. The Universal Array also provides better relative density when used to implement gates and flip-flops in more random logic structures. The APAR approach, generally provides a slightly higher density capability than Universal Arrays. The APAR standard cell implementation of counter and shift register logic functions is more efficient than the Universal Array version.

Facilities burden

This evaluation factor is important to indicate the degree to which the particular approach utilizes the facilities available for array design and fabrication. In a period of order backlog, queuing for equipment usage, etc. consideration has be be given to the approach which minimizes its use of limited facilities. In this area the Universal Array has a clear advantage. Basic to the approach is a fixed array format with customizing occurring only on a portion of the metal mask. The impact of this approach means only one level of checkplot, artwork, and mask is required to define the application. This compares with 7 unique levels required to define an APAR or custom design. The Universal Array also has decided advantage in the wafer fabrication, probing, and testing areas. Wafers can be processed in bulk to the metal definition level and stored for later use. The investment in these stored wafers is of a low risk nature due to the continuing use of the Universal array vehicle for other applications. Probing and testing are simplified by the use of a common probe card for all applications. As application experience builds up for a basic Universal Array structure, confidence is increased that the basic design and non-varying mask set is good, as proven by past experience.

Design time

The APAR and Universal Array approaches have a decided advantage in design turn-around time. The APAR approach gains its reduction in design time via the placement and routing program that replaces the manual layout. By this technique it is possible to replace several months' effort with a few weeks effort. By use of this approach, a small engineering staff can design many array types. Once the design is firm, the time required to process artwork and masks and wafers does not vary significantly from a custom design. The Universal Array approach uses manual placement and interconnect techniques. Experience however has shown that the simplified procedure of placing cell decals on a standard layout form and interconnecting them on a fixed grid format does not require much time. An experienced person can accomplish this task within a few days to a week. The single artwork/mask requirement coupled with the availability of stockpiled wafers, reduces the fabrication cycle time to a minimum.

Error recovery

Changes are a way of life in array design, especially in a new program. The consequence of a change in requirement (logic change) or error in implementation varies considerably depending upon the time at which the change has to be made, and the magnitude of the change. Two cases are described here. The first is a simple error discovered at wafer probe. Errors of this type include wrong logic connections, wrong logic cell used, inverter left out, etc.

In the case of a custom design, correction usually involves modification to the layout of a degree that depends upon the location of the problem on the array. In the worst case, rework involves moving many devices to open an area in the middle of the array to insert an extra function. The fabrication cycle is the same as in the initial design except that probe-debug time is reduced by the experience gained on the first go around.

For an APAR design, the consequences are not usually as severe. The lower density of the APAR design means that there is usually room to add and change the array without as much manual modification time. In the worst case, the APAR program would have to be run again.

The Universal Array approach has the best approach to recover from a simple error. In the worst case, only one mask level needs changing. Frequently there is an unused cell nearby that can be used for the modification. Changes to the one level of artwork can usually be made in a day or two and the availability of stockpiled wafers cuts the fabrication cycle time to a few days instead of 2-3 weeks.

The second type of error to be discussed is a more complex type discovered after sample units have been packaged. An error of this type requires a major redesign effort for all three approaches. Due, however, to the low-cost-quick-response capabilities of the Universal Array and APAR approaches, a significant quantity of time can be saved if either of these approaches is used. Assuming one major and one minor redesign cycle, a universal array design can be implemented in approximately one third the time and cost of a custom design. The break-even quantity is 20,000 to 50,000 units. The APAR approach has higher design cost and time with a correspondingly lower breakeven quantity.

Summary

Three design approaches for complex MOS array design have been reviewed and compared. The Universal Array approach is best for quick turn-around applications where the logic design, technology or application is most likely to change. The APAR approach should be used when the UA standard cell library is not sufficient to implement the design and when specialized cells such as D/A converters, and low-impedance drivers, must be designed for the given application. The APAR approach is also good for quick turn-around applications, gives higher density than the universal array approach, but is not as responsive to changes. Both the APAR and UA approaches are excellent tools to be used until the logic has been proven. The custom approach should be reserved for applications where high volume justifies the high design cost and time. All three approaches rely heavily on computer aids.

The 1975 David Sarnoff Awards for Outstanding Technical Achievement

RCA's highest technical honors, the annual David Sarnoff Awards for Outstanding Technical Achievement, have been announced for 1975. Each award consists of a gold medal and a bronze replica, a framed citation, and a cash prize. Awards for individual accomplishment were established in 1956 to commemorate the fiftieth anniversary in radio, television and electronics of David Sarnoff; awards for team performance were initiated in 1961. All engineering and research activities of RCA divisions and subsidiary companies are eligible for the awards. Chief Engineers and/or Laboratory Directors in each location present nominations annually. Final selections are made by a committee of RCA executives, of which the Executive Vice President, Research and Engineering, serves as chairman.


S. Lipp


T. Saulnier


S. Trond

For outstanding achievement in the development and practical implementation of a high-contrast phosphor television screen

Steven Lipp
Theodore Saulnier, Jr.
Stephen Trond

Dr. Lipp of RCA Laboratories, Princeton, N.J. and Messrs. Trond and Saulnier of the Picture Tube Division, Lancaster, Pa., developed a practical phosphor for color television screens that reduces the amount of reflected light without seriously degrading the efficiency of light output. The teamwork involved in this unique development is an excellent example of how products can be transferred from research to a product division in a reasonable time and at an acceptable cost.


R. Baugh


T. Mehling


W. Patton


G. Stevens

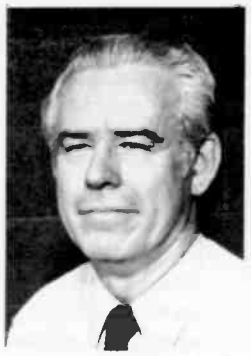
For outstanding contributions in the development of a multifunction tactical phased array radar system

Richard A. Baugh
Thomas H. Mehling
Willard T. Patton
George H. Stevens

Messrs. Baugh, Mehling, and Stevens, and Dr. Patton of the Missile and Surface Radar Division, Moorestown, N.J., played key roles in the development of the AN/SPY-1 phased array radar, which is recognized as one of the major technical advances in radar system design over the past decade. The AN/SPY-1 — the heart of the AEGIS Weapon System — provides simultaneous search, detection, and tracking of a large number of targets in an environment of noise, clutter, jamming, and a multiplicity of friendly and enemy aircraft, missiles, and ships. This capability for simultaneous multifunction performance (which no other radar has yet been able to demonstrate) is the result of the design concepts and implementation efforts of Baugh, Mehling, Patton, and Stevens.

For excellence in the design and development of a hand-held, two-way portable radio

Bill Autry
Lee F. Crowley
Heshmat Khajezadeh
Andrew M. Missenda



B. Autry

L. Crowley

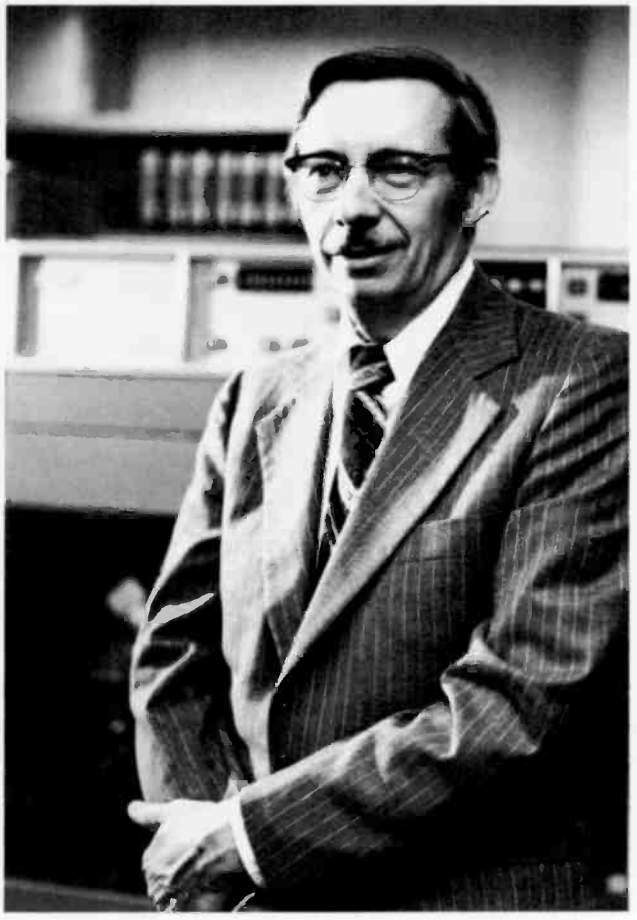
H. Khajezadeh

A. Missenda

Messrs. Autry, Crowley, and Missenda of Mobile Communications Systems, Meadow Lands, Pa., and Mr. Khajezadeh of Solid State Division, Somerville, N.J., were responsible for the engineering design, development, and team leadership on RCA's new TACTEC hand-held radio product line aimed at the commercial land mobile radio services market. The program was very successful in meeting the goals of producing a reliable, maintainable, compact, and economical two-way hand-held radio which is the performance leader in its field. The TACTEC radio is a blend of custom-integrated-circuit and thick-film hybrid technologies coupled with the design and production experience of the mobile radio activity. It has met with great success in the marketplace.

In recognition of his many outstanding technical contributions enhancing RCA's reputation as a leading supplier of television systems

Arch C. Luther



Mr. Luther has made a series of highly significant and important technical contributions to Broadcast Systems' success. Over 20 years ago, he developed a totally new and highly innovative approach for synchronizing generators. During the early years of color development, Mr. Luther reduced a full rack of signal processing electronics in the TK-41 Color Camera System to less than 12 inches. This accomplishment was, incidentally, prior to the introduction of the transistor and was achieved through innovative circuit design. When transistors did emerge, Mr. Luther was the first individual within Broadcast Systems to use this technology to contribute to such new products as a processing amplifier for video tape recorders, a solid-state servo that made possible the synchronization of video tape signals with television signals from other sources, and the first all-solid-state professional video tape recorder. Mr. Luther's creative abilities were also instrumental in conceptualizing the design and development of the TCR-100 Video Tape Cartridge Recorder. More recently, major advances in design to cost and module standardization have been achieved as a result of Mr. Luther's involvement in all of Broadcast Systems' engineering activities.

Operational implementation of a broadcast television frame synchronizer

R. J. Butler

The first permanent installation of a television frame synchronizer in the U.S. and the successful processing of various type of signals for broadcast are discussed. The frame synchronizer is well suited to overcoming problems in video switching due to: videotape servo instabilities, Doppler effects in satellite video distribution, and instantaneous event integration without genlock in electronic journalism. It has become a powerful and valuable tool for the broadcaster.

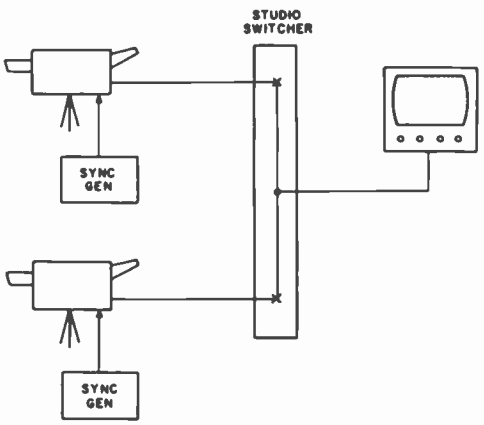
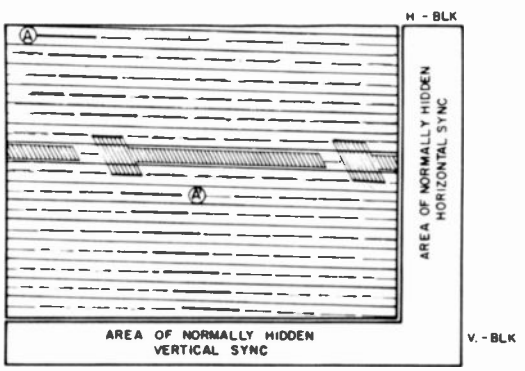


Fig. 1a — Two pictures generated from different time bases.



Fib. 1b — Two different pictures mixed on the same monitor which do not accomplish scanning in the same time interval. A — upper left corner of picture no. 1; A' — upper left corner of picture no. 2.

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STORAGE and resynchronization of nonsynchronous video signals is now possible by the use of a digital frame synchronizer. The first network use of the frame synchronizer occurred at NBC's facilities in New York on 7 April 1974. On this occasion, tennis matches originating in Germany via satellite were integrated into an NBC network program. This same frame synchronizer was later permanently installed in the NBC Burbank plant. Its installation marked the end of a long search for a device that could correct nonsynchronous video switching problems. Although videotape difficulties resulting from nonsynchronous video switches were the prime reason for needing such a device, other recent developments in the broadcast world presented problems which the synchronizer was well suited to solve. Video satellite distribution, with its Doppler problems, and electronic journalism, requiring instant event integration without genlock, have made the frame synchronizer a very useful tool in the broadcast business.

Nonsynchronous-signal problems

The television picture is a serial transmission of picture elements which makes up lines: 262½ lines make up a field; and two successive interlaced fields complete one picture frame. Two successive picture frames make up one color frame. The generation, transmission, or storage of color pictures can modify the serial nature of color signals. The modifications make one picture incompatible with another picture at a mixing junction. When this happens, the picture signals are said to be nonsynchronous. Nonsynchronous conditions arise from two basic causes:

1) The time base or scanning rate of the two signals being compared is not the same,
2) The arrival time at the mixing juntion is not the same for each signal.

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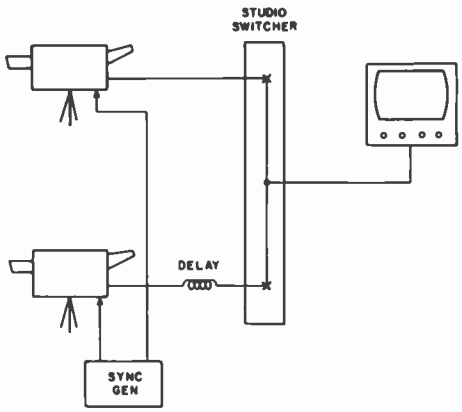

Fig. 2a — Two pictures generated from the same time base.

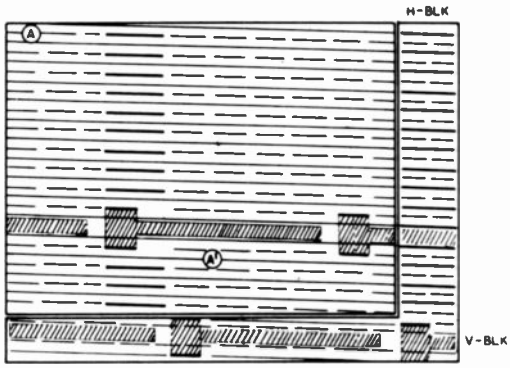

Fig. 2b — Two different pictures mixed on the same monitor which accomplish scanning in the same time interval but do not arrive at the monitor in time coincidence. A — upper left corner picture no. 1; A' — upper left corner picture no. 2.

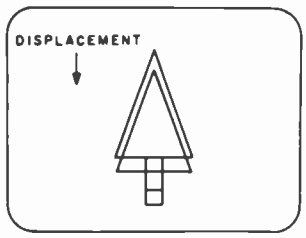

Fig. 5 — Vertical displacement of picture.

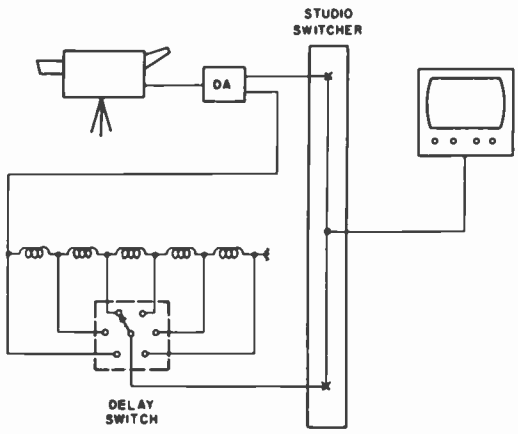

Fig. 6 — Delay line of variable length interposed between a program source and studio switcher.

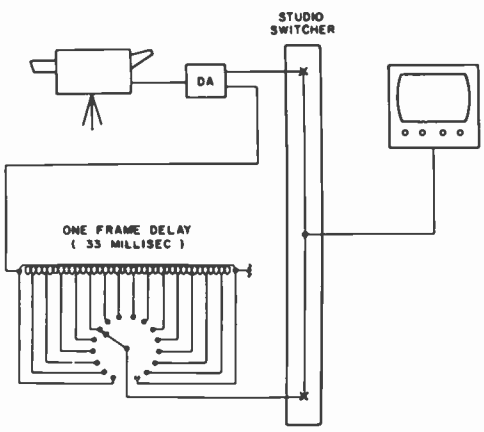

Fig. 7 — Another delay line having finer increments than in Fig. 6.

Fig. 1a shows how two pictures might be generated from different time bases. Fig. 1b illustrates the subjective effect of mixing two signals on one monitor where each has a different time-base frequency. Fig. 2a shows how two pictures generated from the same time base might become nonsynchronous. Fig. 2b illustrates a mixture of two signals on the same monitor where the time-base frequency is identical but the arrival time at the mixing junction is not the same.

Each of the preceding nonsynchronous conditions will prevent the use of special effects between such signals at a studio mixing junction. It is interesting to note that the sole cause for one of the nonsychronous conditions is a difference in the path length to the mixing junction.

Fig. 3 shows that the exact same picture would be considered nonsynchronous if the two paths it took to the comparison point were sufficiently different in electrical length. The magnitude of the delay difference would have different effects during the time the two signals were in combination. Several nanoseconds differential in delay would cause only color error during the mixture. Several microseconds delay would cause horizontal displacement as illustrated in Fig. 4. Many lines of delay cause a vertical displacement (Fig. 5), and several frames of delay would cause motion or a time displacement.

In Fig. 6, the various amounts of delay discussed above are switched into one path leading to a mixing junction. As the switch is rotated clockwise, the delay is increased in large increments, and an abrupt displacement of the delayed picture is noted. Finer increments of delay, switched in a similar manner, are shown in Fig. 7; they continuously move the delayed picture to the right as compared to the undelayed scene. Had the delay switch in Fig. 7 been rotated in a counterclockwise direction, the delayed picture would have moved progressively to the left or earlier in time.

Fig. 8 shows the effect of switching as viewed on the mixing monitor. This illustration bears a striking resemblance to the conditions illustrated in Fig. 1b., where two signals with different time-base frequencies had been mixed. The causes of the problems were different in each case, but the characteristics of the nonsynchronous condition are identical.

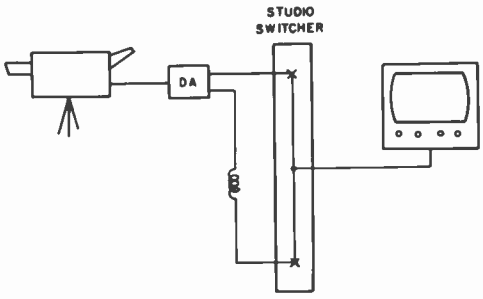

Fig. 3 — Identical picture nonsynchronous at mixing junction.

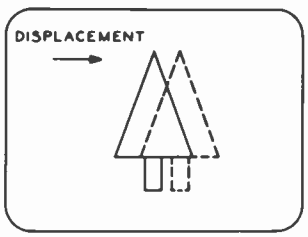

Fig. 4 — Horizontal displacement of picture.

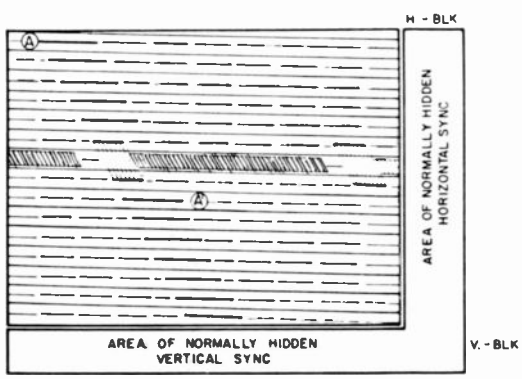

Fig. 8 — Two different pictures mixed on the same monitor which do not accomplish scanning in the same time interval. A — upper left hand corner picture no. 1; A' — upper left hand corner picture no. 2.

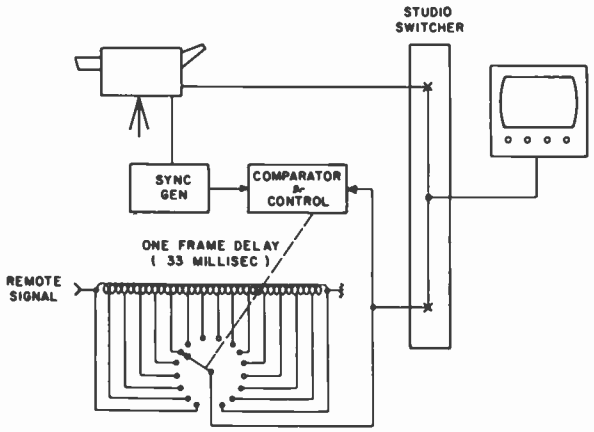

Fig. 9 — Possible delay-line construction of a frame synchronizer.

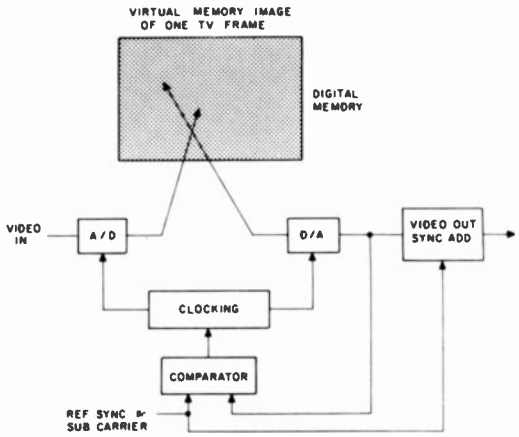

Fig. 10 — Frame synchronizer employing virtual memory image of one tv frame to accomplish the required delay.

If the delay mechanism had an infinite range of delay, a simple switching in or out of delay elements could synthesize a video signal of any desired time base.

The solution

Industry now has a practical solution to the nonsynchronous signal problem, which in effect, is equivalent to the construction of a delay line of sufficient length with fine enough increments of delays so that they may be switched in or out without subjective or visible effect (Fig. 9). If the signal to be synchronized is generated from a time base of equal frequency but arrives at the mixing junction displaced in time, the delay line is set either longer or shorter until synchronous conditions are achieved. If the signal to be synchronized is generated from a time base different than that of the receiving point, the delay line is instantaneously set to complement the remote signal so that it is synchronous. Then the delay is increased or decreased so that the synchronous condition is maintained.

If the delay line is exactly one frame long, then the picture entering the line and the picture leaving the line are, for all practical purposes, synchronous. If the signal at the input of the line and the signal leaving the line were mixed, the only unwanted subjective effect might be a lag when motion occurred. Since the subcarrier is an odd multiple of one-half frame frequency, a mixture of two color pictures exactly one frame apart would result in the cancellation of all chroma. This can be overcome by making the delay difference one frame, plus or minus one-half cycle of subcarrier.

Operating within broadcast standards, the remote and local signals could have a maximum subcarrier frequency offset of 20 Hz. This offset would represent a delay shift of 5.6 μs/s. Since one frame of delay is approximately equal to 33 ms, it would take 1½ hrs for the delay line to sample all of its delay positions. Somewhere during the 1½ hr period, the delay would shift from the beginning of the line to the end of the line, thus reusing the frame stored within the delay line. Or the switch might, for the opposite case of the time-base difference, switch from the end of the delay line to the input of the line, thus, completely skipping over the frame presently stored within the line. This process converts the time-base characteristics of the remote incoming signals to those of the reference signal supplied to the frame synchronizer.

If the reference signal supplied to the synchronizer was derived from a rubidium standard, then the video processed through the synchronizer would be rubidium-accurate. Since rubidium standards are designed to be at the center of the broadcast standards, the maximum subcarrier differential to any other signal within the standards would be 10 Hz, thus the minimum delay recycling time would be 3 hrs. If the incoming remote signal has a subcarrier frequency offset of, for example, 100 Hz the delay line would cycle ten times faster or at a rate of once every 18 min. This characteristic of the frame synchronizer is what makes it so valuable in dealing with remote signals generated by electronic journalism cameras and portable tape recorders. Genlock was never able to cope with the problem. Even rubidium standards alone could not help the situation.

For simplicity of explanation in the above, the frame synchronizer was described as a segmented delay line of one-frame electrical length. In practice, this is not the case; the unit is a sophisticated digital memory complimented by analog and digital circuitry which behaves much like the switchable delay used in the explanations. However, since it is a memory device and not a delay line, it can store and continually reproduce the single frame held in its memory (Fig. 10) This attribute of the frame synchronizer leads to another of its most valuable applications.

Although the broadcaster can control those switching functions which occur in his own plant, he is vey often required to prerecord remote or network activities for later playback. Nonsynchronous switching of video signals has a devastating effect on videotape servo systems. The instantaneous change in sync timing of the incoming signal fed to the videotape recorder during record may result in a 3- to 4-s picture outage during playback while the playback servos stabilize. Introducing a frame synchronizer in the video path prior to the recording VTR will automatically convert all incoming nonsynchronous switches to synchronous switches. This is accomplished since, upon recognition of nonsynchronous input signal conditions, the frame synchronizer repeats the last synchronous field in storage and then switches to the newly stored and synchronized incoming signal. In addition to storing and repeating the last synchronous field during the recovery from a nonsynchronous switch, the frame synchronizer continuously provides an output of reference sync and burst whether or not it is fed an input signal. This

prevents the audio wow and picture outage during playback servo stabilization which might have occurred during a gap in switching among input signals.

Processing quality

The frame synchronizer is essentially a transparent window to the television signal. The distortions and noise added to the signal as it is processed result in a picture quality which can be best described as comparable to one negative generation of quadruplex videotape. In other words, four passes through the frame synchronizer would be equal to a second generation videotape with respect to noise. Two passes through the unit would be equal to a first generation videotape with respect to linear and nonlinear distortions.

Applications

The integration of remote signals received over telephone lines without the need for genlock is one straightforward application of the frame synchronizer. The point of origin of the remote signal is of no consequence since the frame synchronizer can synchronize a standard signal originating at any point. If two remote signals were to be integrated simultaneously, two frame synchronizers would be required. Although this is a possible operating situation and even though NBC plans to have at least two frame synchronizers at its New York and Burbank plants, effective input switching and output distribution of a single frame synchronizer seems the appropriate solution.

The synchronizer could also perform the remote synchronizing function of signals received via satellite. Geo-stationary satellites are not absolutely stationary with relation to a given point on the earth's surface. The satellite usually oscillates over a 24 hr period in a "lazy-8" pattern. For this reason, the transmission path length is alternately lengthening and shortening. These variations in path length present no problem to the synchronizer, since it can dynamically vary the inserted delay in a complementary manner.

Electronic journalism

The age of electronic journalism has arrived. It presents many problems which the frame synchronizer can solve with ease. Fig. 11 shows two possible operating situations where a news event is required to be integrated directly into a program in progress. If the event is happening while the program is on the air, no previous timing or genlock checks need be made. The signal delivered to the studio is usable as soon as the microwave path has been established. Frequency offsets at the remote camera, microwave fades, and path-length variations are all complemented by the synchronizer.

If the event had been recorded on a portable heterodyne-type equipment shortly before the program was to be broadcast, this same portable equipment may be used to play back the event during the program. One additional processing step must, however, be provided at home base. Heterodyne processing of the chroma signal in playback alters the chroma and burst relationship to the scanning frequencies. The frame synchronizer expects these relationships to be correct. A preprocessing step called correlation will make this type of remote signal acceptable to the frame synchronizer. The correlation process reheterodynes the incoming chroma signal with a varying subcarrier derived from the incoming sync signal.

Plant installation

Fig. 12 shows how the synchronizer is to be installed in the NBC New York plant. One output of the plant routing switcher is supplied as an input to the synchronizer. The output of the synchronizer is returned to the routing switcher as an input. Although not shown in this drawing, all plant videotape recorders receive their input signals from the same routing switcher. This arrangement means that any VTR may use the output of the synchronizer when recording remote signals where nonsynchronous switching is expected. Any studio may also use the output of the synchronizer since they too are supplied signals from the same routing switcher.

On those occasions where multiple remote signals are to be used within the context of one show (e.g., during election coverage), the coordinating studio has one of its less-used production switching busses return to the routing switcher as an input. Master control, which is normally in control of the input to the synchronizer, calls up the studio buss as the synchronizers' assigned input. Any number of remotes may then be assigned

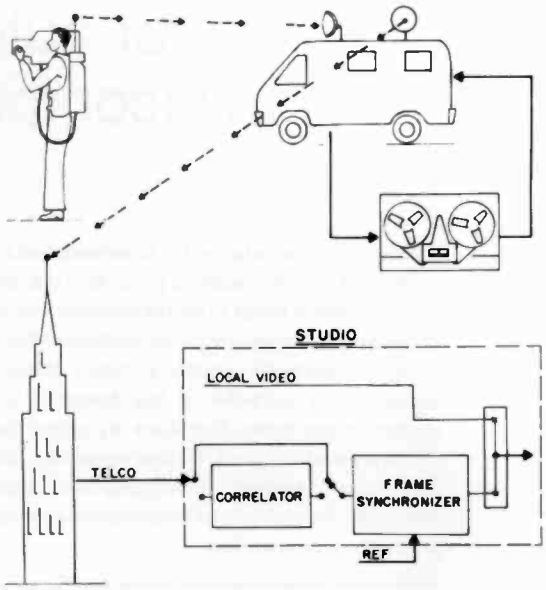

Fig. 11 — Frame synchronizer used with electronic journalism.

to the production switcher via the routing switcher, as shown. In addition, the output of the synchronizer can appear as an input to the production switcher. This configuration allows the production personnel in charge of the program to determine which remote should be processed by the synchronizer. The technical director simply makes the appropriate subswitch on his preview buss.

Conclusion

Our goal as technical broadcasters has always been to provide those facilities which will improve our technical product and result in better television coverage for the general public. The television frame synchronizer meets this objective.

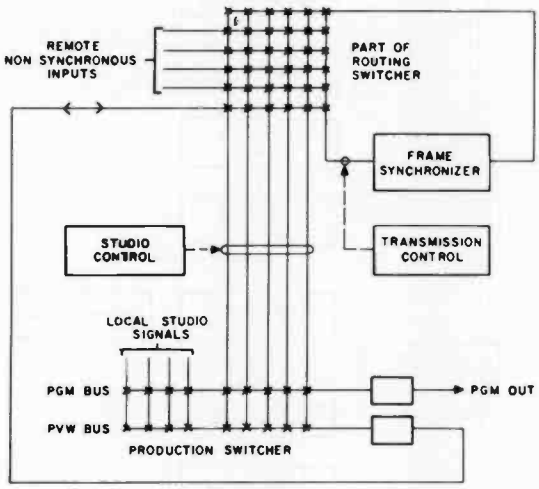

Fig. 12 — Frame synchronizer installation at NBC New York.

Software for automatic testing using minicomputers

J. H. O'Connell

Software implementation for automatic test systems controlled by minicomputers can be a costly and time consuming process. This paper describes a procedure for implementing software which tends to minimize costs and avoid delays caused by unexpected problems. The procedure consists of completely defining the test system functions and performing a series of hardware versus software tradeoffs during the design and implementation process. The purpose of the tradeoffs is to determine the least costly method of implementing tester functions by either hardware, software or some combination of hardware and software. Delays caused by unexpected problems are reduced by including hardware and software debugging aids which shorten the time to validate the tester system functions. An example of implementing an automatic test system in accordance with these procedures is provided.

AUTOMATIC TESTING provides many benefits, such as shorter testing time, more thorough tests, and consistent test results. These benefits usually result in a delivered product that has fewer defects. Obtaining these benefits is costly and, therefore, a well-planned development process should be used to minimize the cost and time required to implement an automatic test system.

Since minicomputers are low in cost, they are a logical choice for a processor or central controller in an automatic test system. This paper will not describe the pros and cons of the minicomputer selection process; but, rather it assumes that an automatic test system will be implemented with a given minicomputer processor, special purpose interfacing hardware, and a software test program. Because many readers are familiar with the hardware design techniques needed to implement the interfacing hardware, and because software implementation costs sometimes exceed hardware costs, this paper will highlight the software design approach, which tends to minimize costs and helps to meet schedules.

The software design techniques that result in lower costs are initially to define the tests to be performed and then to perform a series of tradeoffs which result in an optimum test system. Some of these tradeoffs are: manual versus automatic test functions, hardware versus software test functions, and special purpose versus general purpose software operating systems.

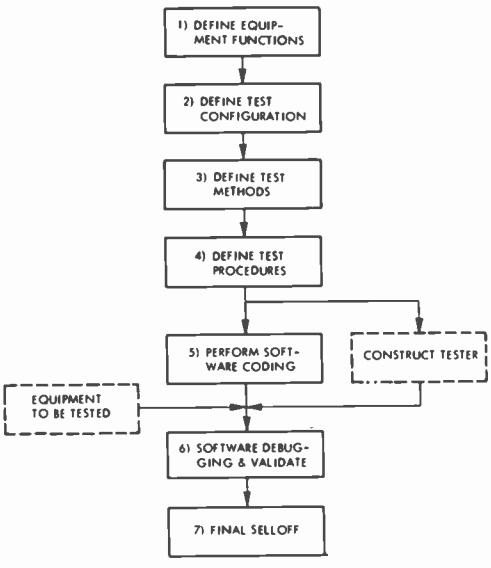

Fig. 1 — Tester development.

Development process

This paper describes seven major development steps that lead to a successful automatic test system. These steps are executed in the sequence shown in Fig. 1. A detailed explanation of each step follows after a brief explanation of an automatic test system that was developed in accordance with this process.

The example automatic test system was designed to test all of the functions of a computer controlled console. The console's primary functions are to display faults automatically detected in a large phased-array radar and to provide an operator control interface for testing the radar. The console interfaces with an AN/UYK-7 military computer. The major devices within the console are: a status panel which indicates the location of faults, a data acquisition controller to acquire measured data from remote test points, a display buffer for displaying text on a video display monitor and accepting text from a keyboard, and a remote controller which interfaces with a remote console that provides an additional operator control point.

The automatic tester major functions are shown outside of the dashed lines in Fig. 2; the console is within the dashed lines. The tester simulates three console interfaces — to the control computer, the data acquisition hardware, and the remote console. These simulated interfaces may be controlled automatically by a computer program in the minicomputer, or manually by a manual control panel. The test operator interface consists of a teletypewriter connected to the minicom-

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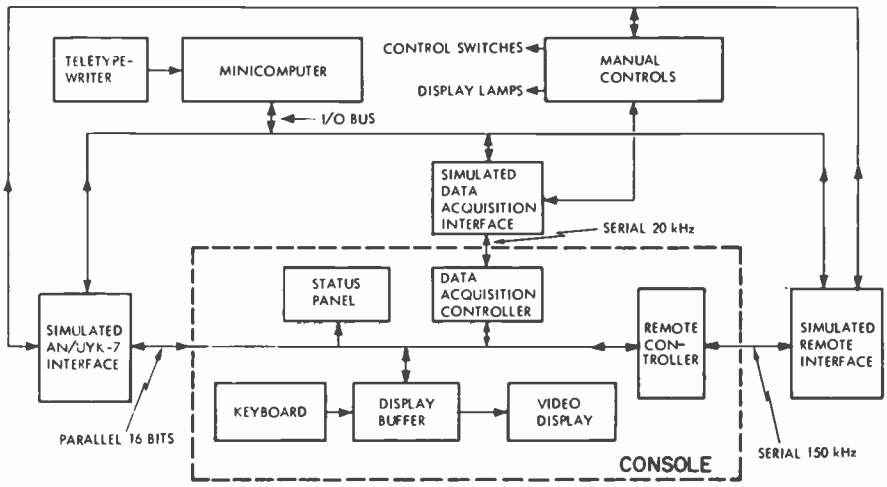

Fig. 2 — Block diagram of automatic tester and console under test.

puter and switches and display lamps on the manual control panel.

Define equipment functions

The first development step (see Fig. 1) is to define the equipment functions which must be tested. One of these functions is a test of the external electrical interfaces. This may appear to be a trivial process, but it is important to insure that no functions are omitted. Also, a complete list of the testable functions aids the design process required to define the tester hardware and software functions. If this step is performed correctly, there is very little chance that the tester will need a retrofit after it is completed.

For the example console under test, the major testable functions are given below:

- Lighting all status indicators on the status panel to all possible states (there are five states per indicator).
- Acquiring measured values from remote test points through the data acquisition controller. Data acquisition is accomplished by outputting a 10-bit test-point address which is decoded by a remote assembly and then by returning a 10-bit measured value.
- Perform input and output data transfers to a remote console through the remote console controller.
- Input ASCII characters from the keyboard and display ASCII characters on the video display through the display buffer.

There are three external electrical interfaces which require testing: a 16-bit parallel interface to the AN/UYK-7 computer, a 20-kHz serial interface to remote data acquisition assemblies, and a 150-kHz serial interface to a remote console.

Define test configuration

The next development step is to define the automatic tester configuration. The configuration consists of the interfaces to the equipment under test, the control of tester functions, and the interface to the test operator. The purpose of this development step is to define the tester in block-diagram form so that detailed design requirements can be generated.

In determining the tester configuration, a tradeoff between automatic and manual control functions can be made to optimize the tester hardware. It is possible to perform all tester control functions automatically from the minicomputer and thereby eliminate all of the hardware for manual controls. However, such a tester would be difficult to debug during its construction phase. The critical debugging area is the simulated interfaces which need to be easily controlled while checking them out. An engineer performing this process may work more efficiently if he can control a data transfer by setting switches on the control panel rather than by manually inserting computer instructions into the minicomputer memory. Therefore, some manual control functions, which will shorten the debugging time period, should be added to the tester. These functions also allow debugging to continue if there is a computer failure.

The next tradeoff area is hardware versus software testing of input data and test conditions. For many test requirements, it is possible to do all testing by software. This approach is desirable because it eliminates some hardware. Before making this decision, the tester configuration should be carefully reviewed to find areas where software testing is not feasible. The most likely candidates are tests that must be performed faster than can be done by software. Such a timing constraint occurred in the tester remote console interface. When data are sent to the remote console from the console, they must be checked for odd parity and they must be retransmitted within 6 μs if parity is incorrect. This time interval is much too short for the software to perform the parity check.

Another technique that may be used to perform test functions quickly is to use a programmable read-only memory (ROM) in the minicomputer. Such a ROM may be able to perform the test function within the time constraints, and it would be cost effective if it is used for several test functions.

Define test methods

The next development step is to define a test method for each equipment function. The test method consists applying a test stimulus, executing the test, acquiring test measurements or results, and checking the rest results. Test results are usually checked by comparing measurements to an expected value or limit.

For the console tester, many of the test stimuli are data words stored in memory. The tests are executed by outputting the data words through the simulated interfaces to the console. Test results are acquired by checking that the data transfer terminated properly and then checking any data words inputted by the console or viewing any console operator displays.

A good example of a test method is data acquisition. The computer sends a 10-bit test point address through the simulated AN/UYK-7 interface, and it is outputted from the console to the simulated data acquisition interface. The minicomputer then returns a 10-bit measured value through the interfaces in the reverse direction. The test passes if both the test point address and the measured value are returned to memory exactly as they were sent out.

While defining test methods, a tradeoff between automatic and manual test-result verification can be performed. The advantage of manual test verification is

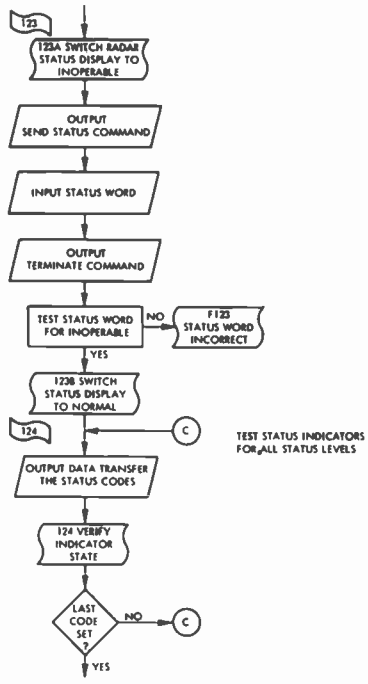

Fig. 3 — Sample test.

that less software is required. However, it will take longer to perform the test and the possibility of a human test error is increased. The best way to resolve this tradeoff is to estimate the increase in testing costs due to longer test times and then compare this increase to the cost of implementing the additional software.

There are some situations where automatic test result verification is not feasible because there are additional hardware costs to consider. This occurs in the console when checking the operator displays. It would take the equivalent of a color television camera and signal processing hardware to prove that the displays are lit correctly. Since this is not feasible, manual verification of output displays was selected.

Define test procedures

This is the last development step needed to complete the tester design. This step consists of translating each test method from the previous step, into tester hardware, software, and operator actions. This step produces a set of hardware logic diagrams and schematics, a set of flow charts for the test software, and a step-by-step procedure for the test operator. These documents are the primary design specifications from which the tester is implemented.

A sample flow chart for the console tester is shown in Fig. 3. Test 123 checks the status panel for an inoperable condition, and test 124 checks the status indicators for all states. The test operator messages which are typed on the teletypewriter are shown within the scroll symbols. Test 123 requires that the operator set and reset the inoperable switch, but the test is performed automatically. If a test failure occurs, message "F123 Status Word Incorrect" will be typed. In test 124, the operator must visually check that the display indicators are set to the correct state, and the computer program will go around a loop five times.

There are several tradeoffs which can be performed while defining the test procedures. The first is a general purpose versus a special purpose software operating system. Many minicomputer manufacturers offer general purpose operating systems which can be considered for automatic test systems. They offer potential cost savings by reducing the amount of software to be produced. Before making this tradeoff, it should be determined which software functions are required to be performed by the operating system. For an automatic tester, some of these functions are handling interrupts, typing operator messages, and decoding operator commands. If only one equipment is to be tested at a time, all tests will be performed sequentially and there is no need to provide multi-programming scheduling. After determining the functions needed by the tester, the next step is to study the general purpose operating system to determine if they are included. If they are not, then the choice is to modify the standard system or create a special purpose system. Since the operating system requirements are not difficult to provide, it would probably be cheaper to implement a special purpose system rather than try to learn how to modify a general purpose system. Also, the general purpose system is likely to include functions not required by the tester. Therefore, it would require more memory core than the special purpose system. For the console tester, it was decided to implement a simple special purpose software operating system.

The next tradeoff is manual versus automatic test result recording. The advantage of recording test results automatically is that it shortens the testing time and eliminates the possibility of human error. However, it does require more software and it may require additional hardware, such as a magnetic tape recorder if there is not enough core memory. Again, this tradeoff can be best resolved by calculating the cost savings from reduced test time and comparing it to the additional hardware and software costs. For the console tester, it is planned to test less than ten consoles and therefore manual test result recording was selected.

The last tradeoff is an operator control interface consisting of a teletypewriter versus special purpose switches and displays. As indicated previously, there are several points in the test procedure where the operator must intervene. He may control the test either through the teletypewriter keyboard or through special purpose controls on the control panel. The teletypewriter has an advantage in that it is a very flexible interface and it also produces a hard copy of all operator test actions. To eliminate the cost of the teletypewriter, it is required to design a special purpose operator control interface to the computer and purchase some additional hardware. This tradeoff for the console tester resulted in nearly equal costs; however, the hard copy output from the teletypewriter was the deciding factor in favor of the teletypewriter. Another factor which was considered was that the teletypewriter can be used to type computer program listings which eliminated computer time charges for assembling test programs on a larger computer.

The test operator control commands provided for the console tester are as follows:

G to continue the test

H to halt a text

*R*XXX to repeat a test XXX.

Perform software coding

Software coding can be done in parallel with construction of the tester hardware, and it consists of writing the minicomputer instructions and test data on coding sheets for later transfer to the minicomputer assembler. The purpose of coding is to translate the test requirements defined on the flow charts into a set of instructions executed by the computer. This step is a major cost item in implementing the software, and every reasonable technique should be used to minimize the time required to perform this step.

If the person who does the coding is not the hardware designer, it is possible to reduce his coding effort by defining the software requirements in a manner that he can readily understand. Since the test program will execute in the minicomputer, the programmer should not be expected to know how the interface hardware works. Rather, he needs to know how to perform a data transfer over the minicomputer I/O bus and how to correctly set the bits in each data word. This explanation can best be provided by a hardware designer who has had some minicomputer programming experience.

The first tradeoff to perform is a higher level programming language versus assembly language. Many minicomputer manufacturers offer programming languages such as Fortran, Basic and Algol. These languages are easier to learn and they usually require less effort to code. However, they require an operating system to execute, and the operating system does not include the I/O interface to the simulated interface hardware and the handling of tester interrupts. These operating system functions can be added; however, they must be done by using assembly language programming and they require learning the details of the high-level program operating system. Since minicomputers have a small number of instructions, it is probably easier to learn the assembly language instructions rather than to learn how to add functions to a higher level programming language. For the console tester, it was decided to write the programs in assembly language.

The next tradeoff is straightforward coding versus common subroutines. It is possible to code the test programs directly from the flow charts in a straightforward manner. However, if common subroutines are implemented, it is possible to reduce the coding effort by not having to repeat the code for functions which are performed many times. To achieve this potential savings, the flow charts should be carefully reviewed to find those functions which are repeated many times. Examples of repetitive functions are I/O data transfers and time delays. As an example, an I/O data transfer common sub-routine is designed to perform all data transfer functions. When it is called, it receives as arguments the data memory address and the number of data words to be transferred. Therefore, whenever the programmer is required to perform an I/O data transfer, he need only specify the subroutine call code and the arguments for data address and number of words to be transferred.

Another software coding consideration which can save some time in debugging is to organize the code sequence so that it may easily be found on the program listing. For the console tester, each test started on a new listing page with a title containing the test number. The first code set consisted of all the instructions needed to execute the test. This was followed by the instructions to handle test failures, such as typing a test failure message. The next code set consisted of the data words needed to perform the test. The final code set is the text of the operator control and test failure messages. On the right hand of the listing appeared remarks which explained the test functions. Since this organization of the code was standardized for all tests, it proved to be very useful in finding software problems during test debugging.

Software debugging and validation

This step is performed when the tester hardware and equipment is available. Again, this step can be a major cost item if some unexpected problems are found. There are several techniques available which can be used to minimize the time to perform this step.

For the console tester, the following debugging aids were helpful in reducing the debugging time: a) the lamp displays on the panel connected to control lines quite often indicated that the problem was somewhere in the hardware and not in the software; b) the minicomputer control panel provided for display of any instruction or data word in memory and it also allowed for changing data words and test limits. c) When timing problems were found, a computer program instruction was changed to cause an endless loop of data transfers; the signal waveforms were then checked with an oscilloscope. d) If the test program required additional instructions, a "patch" of instructions was easily added in an unused section of memory.

After the obvious software problems were corrected, the program was validated by intentionally introducing failures into the equipment hardware. This check proved that the software would print the correct error message when a failure was found.

Final selloff

This step proves that the automatic tester is correctly implemented and that it can be used to test equipment. The procedure for final selloff is usually determined by customer requirements. This procedure affects the software implementation process in two areas: providing documented test results and recovering from test failures if an error or fault should occur.

In the example tester, test results were recorded manually on a separate test data sheet. However, the software was designed to provide a positive indication of a test passing or failing. Since the customer witnessed the selloff test, he was given a copy of the step-by-step procedure which describes the test performed by the computer and how test results are indicated on the teletypewriter.

If a test failure should occur, the step-by-step procedure describes how corrective action may be performed. The software includes an operator command for repeating the test to prove that the test may now pass. In addition, every test program includes a test that automatically initializes the test hardware and the console under test. Performing the initialization test is sometimes necessary in order to recover from a test failure.

If the automatic test system is required to test large quantities of test equipment, the software may be designed to record test results automatically on magnetic tape. This allows for additional processing of test results to summarize test parameters and analyze failure trends.

Conclusions

The software implementation process described for an automatic test system using a minicomputer tends to reduce implementation costs and shorten the time required to code the software. Several tradeoffs can be performed during the system design phase which lead to an optimum system. These tradeoffs can be applied to a wide range of military or commercial equipment to produce automatic test systems at reasonable costs.

Automated system support for the EPABX model 600

H.J. Kelsey| M.E. Meer| P.R. Slojewski

A solid state PABX with a wide variety of standard and optional features has been developed by RCA for entry in the commercial telephone market. A number of system size classes were developed to make RCA EPABX cost competitive with other existing systems — electronic and electromechanical — foreign and domestic. Each system class is populated with lines and trunks to suit the end-customer requirements. The number of lines, trunks and features vary from system-to-system, making each system essentially unique. In view of the large number of systems projected for delivery in the next few years, the large quantity of support documentation required and a resultant massive demand on manpower tends to increase cost. The key factor in providing low-cost support for a stepped-up production rate is to use automation in the translation of system requirements into equipment drawing lists, parts and assembly accumulation lists and wiring schedules — so that a short turnaround time from receipt of order to equipment delivery can be achieved. A computer program has been developed by RCA to automatically generate the system parts and accumulation lists, wiring decks, DITMCO wiring tests, pricing data, and finally as an extra output, parts usage data for automatic recording of support and stock material. This paper demonstrates how the program works, and by inference, shows how it can be applied to any other product with a significant production rate.

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Mark E. Meer, a senior member of the technical staff in the Government and Automated Systems Division, Camden, N.J. received his BSME degree from Robert College in Istanbul, Turkey in 1950 — and his MME from New York University in 1951. He did extensive graduate work at NYU in electronic engineering. Mr. Meer joined RCA in 1956 and has since been assigned to several project engineering tasks. On Minuteman he was the DEI coordinator and project engineer on the development of several automatic test equipments at the drawer and system levels. In telephone systems he was project engineer on several subsystems on Unicon and Vocom and worked on the development of a family of solid state tactical switching equipment from which the EPABX was ultimately spawned. Currently, Mr. Meer is assigned to the EPABX SYSTEM group as project engineer on a special application PABX. He is the responsible design engineer on the Automated Ordering Program.

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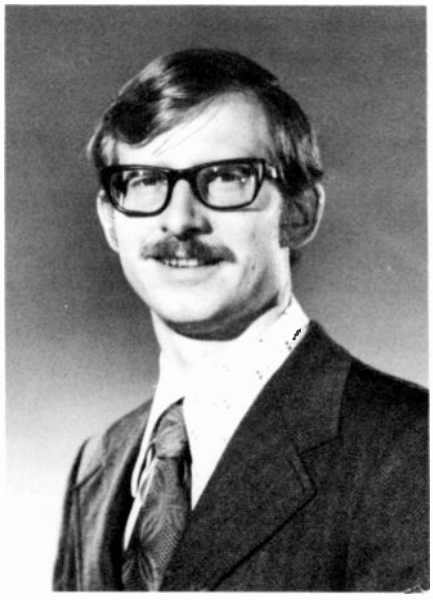


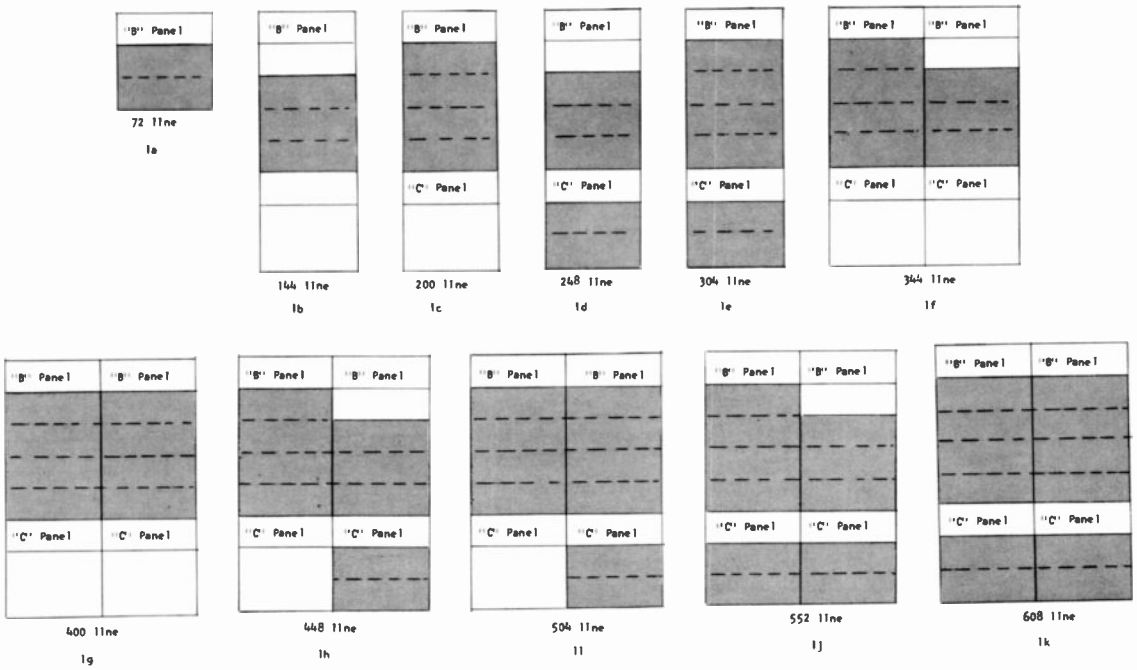


Fig. 1 — System size configurations showing eleven arrangements.

THE RCA EPABX is a highly sophisticated product using large-scale integrated circuit (LSI) devices — and the system provides a wide variety of standard and optional features. To provide a system that competes effectively with a variety of optimally designed system sizes, EPABX is configured in 11 sizes ranging from 72 lines to 600 lines (see Figs. 1a through k).

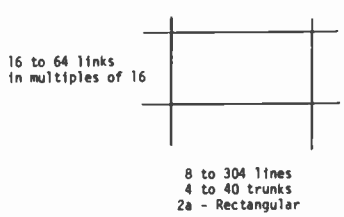
Each system size can be depopulated for both lines and trunks, as required for a particular customer's application. Physically, the system sizes up to 304 lines are packaged in a single rack; system sizes larger than 304 lines are packaged in two racks. The basic matrix is rectangular for all systems up to 304 lines; in multirack operation, the matrix is a graded rectangular variation (Figs. 2a and 2b) and is dependent on the telephone-traffic-carrying requirements; links (horizontals) can be provided as necessary in multiples of 16 (16, 32, 48 and 64 links).

Several standard and optional service features, when implemented, require both custom wiring and additional hardware. Space is provided in the basic backplane for some optional features, while other features require additional backplanes. Of the standard features that require custom wiring, the numbering plan is by far the most complex where one-, two-, three-, and four-digit telephone numbers may be intermixed to satisfy special customer requirements. Other standard features requiring custom wiring are shown in Table I.

Custom wiring and variable hardware requirements are not limited to the standard features mentioned above. The system common control is also affected by the size class, the number of attendant consoles used, the number of links (horizontals) in the matrix, and the number of registers, trunks, lines, etc.

The number of variables affecting system hardware and wiring (Table II) is so extensive that the number of possible systems is almost infinite, requiring a vast amount of documentation. To manually generate such documentation would require an inordinate amount of time.

In addition to the items listed in Table II that affect hardware, the EPABX is offered in two versions: one for the hotel-motel market and the other for business and telephone company applications.



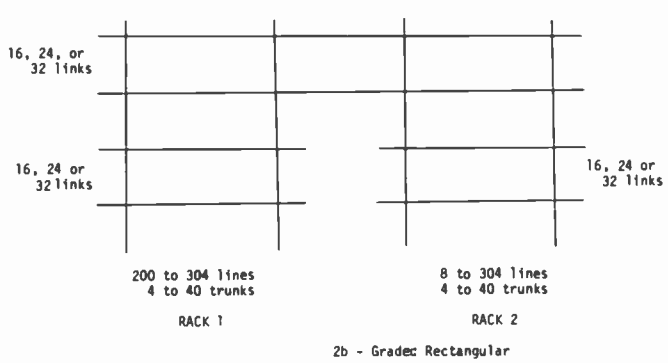


Fig. 2a — A rectangular matrix.

Table I — System variables affecting wiring.

- *Numbering Plan* — intermixed 1, 2, 3 and 4 digits to each line.
- *Hunt-not-busy* — to any group (s) of lines in any group size - also on trunks.
- *Class of serive* — any one of 10 classes of service to any line.
- *Night-answer assignment* — up to 5 assignments to any 5 lines.
- *Paging, dictation, and rapid wakeup trunks assignment* — to any trunk.
- *Dial or hook-switch flash transfer* — in multiples of 8 lines to any number of lines.

Table II — System variables affecting hardware.

- Number of lines
- Number of trunks
- Number of registers
- Number of attendant consoles
- Number of electronic message register consoles
- Selection of 1 or more of 15 "A" options
- Selection of 1 or more of 6 "B" options (requiring the use of additional 1 row backplane)
- Matrix expansion (requiring the use of an additional 1 row backplane)

Table III — Inputs to automated ordering.

- Switch size class and model (hotel/motel or business)
- Number of lines (equipped & wired for)
- Number of trunks (equipped, wired for, and mix two way, incoming and outgoing, paging, dictation or rapid wakeup)
- Traffic capability
- Number of attendant consoles (max of 3)
- Number of electronic message register consoles (max of 3)
- Number plan (including night answer assignments, hunt groups and classes of service assignments)
- Toll restriction for each trunk group
- List of features required

Approach

The preparation of hardware pullout lists, wiring decks, and test tapes for each system in the conventional manner (using technical personnel to meet the short turnaround required) necessitates an extreme degree of care and accuracy. Errors in wiring and hardware callouts result in delays in the factory and potentially greater field problems with associated increased costs in field trouble shooting.

A computer program is designed so that the following outputs are generated for a given set of input variables:

1) Parts accumulation list by equipment schedule (ES), master item (MI) and assembly drawing numbers.
2) Module location chart.
3) Busy-lamp field-configuration chart.
4) Drive deck for the Gardner Denver (GD) machine.
5) Tapes for PIC and DITMCO machines.
6) System definition tables.
7) System loop and positional index lists.
8) System price.

Section I — Customer Information

RCA Government Communications & Automated Systems Division

Sheet ___ of ___
Date Prepared ___
Prepared by ___
Phone No ___
Approved by ___
Rev ___ Rev. Date ___
Control Number (CC1-15LJ)

Line No. (CC 16-19LJ)			
H1	Purchase Order No. (CC 21-35LJ)	System Size & Type (CC 50-54LJ)	
H2	Name (CC 21-60LJ)		
H3	Location (CC 21-60LJ)		
H4	City (CC 21-40LJ)	State (CC 42-43)	Zip Code (CC 45-49)
	Shipping Date (CC 51-56)	On Site Date (CC 56-63)	

QCC 2074 8/74

Fig. 3a — Automated ordering form — customer information.

Section III System Features

RCA Government Communications & Automated Systems Division

Control Number (CC1-15LJ) Rev. ___ Date ___ Sheet ___ of ___

Line No. (CC 16-19LJ)	No (C21)	Yes (C23)	Qty (CC 26)	Description	Remarks
2000				Station Hunting	
2001				U/A Night Answering	
2002				Assigned Night Answer Annunciator Kit (Must have U/A)(Max 5)	
2003				Unassigned Night Answer Annunciator Kit (Must have U/A)(Max 5)	
2004	X			Unassigned	
2005				Paging Trunk Without Dry Contact (Line Circuit)	
2006				Paging Trunk With Dry Contact (Trunk Circuit)	
2007				Rapid Wake Up	
2008				Dictation Trunk	
2009				Tie Line Service	
2010				Area Code Split	
2011				Hardwire Interface	
2012				-48V AC Talk Supply	
2013		X		+12V Junction Box	
2014				Trunk Speed Up	
2015				3 Digit Speed Up	
2016				Camp On Busy With Recall	
2017				Progressive Conference	
2018				Electronic Message Register Console (Max 3)	(Hotel/Motel only)
2019				CEK Interface (Must have EMR)	(Hotel/Motel only)
2020				3 Digit Toll Restriction - If Yes Complete Sect VI	
2021				Busy Lamp Field (Max 2)	
2022				Handset (Attendant Console)	
2023				Set of Rack Casters	
2024				On Site Spares Kit	
2025	X			Unassigned	
				Unassigned	
				Unassigned	
				Unassigned	
				Unassigned	
				Unassigned	

QCC 2076 8/24

Fig. 3c — Automated ordering form—system features.

Table III summarizes the inputs required for the program. Fg. 3a through c show the automated ordering form.

To minimize computer memory size, simplify system construction, and to automatically generate the decks and tapes required for wiring and tests, the numbers of system configurations are made discrete. By assigning unique locations to each backplane within a rack, unique allocation of modules within a backplane, and by unique allocation of interface connectors to individual functions, discreteness is achieved. Within the system, ground rules are set on ways to populate a system for lines, trunks, and registers.

The matrix appearances (verticals) are preassigned so that if locations of line and trunk circuit modules and registers, etc., are known, the number of matrix cards is automatically determined. This same scheme is used throughout the system to determine the number of the different modules required. In the "B" option-feature backplane, the DTMF receivers are assigned on a one-forone basis to the registers. Similarly, the DTMF generator #1 is assigned to attendant console #2 to console #2. In the "C"backplane (matrix expansion), matrix module 20 (MX-20) is the link expansion for MX-1, and MX-21 for MX-02 and so forth. In two-rack systems, rack 1 is always the master—and rack 2, the slave. The layout of each rack is identical to the layout of a single rack system of the same size.

Wiring rule Tables are developed for each condition requiring customized wiring. Tables and wiring lists are generated for all standard wiring for each backplane, and are referenced by the program rather than regenerated for each system. Among these wires are all the common control busses, the tip and ring for each line circuit, the transmit receive and control leads for each trunk circuit, etc. All these rules, assignments and tables are stored in the computer memory banks and are accessed by the punched cards, tapes, etc; prepared from the order form input.

The *automated ordering program* is divided into two phases: phase one is used in the price quotation to the customer and phase two is for building the system. Phase one provides the following:

Verification of inputs— the cards are doubly punched and compared to the order form for verification. At this time, any inconsistency is detected and flagged for correction.

Automatic assignment of line circuits to the telephone numbering plan. This step determines the number of line-circuit cards required and verifies that the system size can accommodate the number of cards.

Automatic assignment of trunk circuits to the trunk groups and trunk access numbers.

Verify system size compatibility with order requirements (verify that the system is feasible).

Compile feature hardware requirements and compare to availability of features in the system.

Compile and printout the hardware accumulation list.

Compile and printout a system price.

The printouts obtained from Phase I of the program including the price quotation are submitted to the customer. Following acceptance of a customer purchase order, a control number is assigned and provides the trigger to start Phase II of the program. Phase II provides the outputs listed in summary form in Table IV.

Section II — System Configuration

RCA Government Communications & Automated Systems Division

Sheet ___ of ___
Rev ___ Date ___
Control Number (CC1-15LJ)

Line No (CC 16-18LJ) 1000

A System Size (CC 21-23)
( ) 072 ( ) 248 ( ) 400 ( ) 562
( ) 144 ( ) 304 ( ) 448 ( ) 608
( ) 200 ( ) 344 ( ) 504

B System Mode (CC 24)
( ) B = Business
( ) H = Hotel-Motel

C Mode of Operation (CC 26)
( ) A = Dial Pulse
( ) B = Dial Pulse/DTMF

D Traffic Capability
1. System Selection Table No ___ (CC 28-30RJ Zero Fill)
2. Link Configuration ___ (CC 32-33RJ)

E Stations
Qty Active Lines ___ (CC 37-39RJ Zero Fill)
Qty Reserved Lines ___ (CC 41-43RJ Zero Fill)

F Attendant Console(s) Type Code ___ (CC 45) Qty ___ (CC 47)
A = 20 Trunk CSL
B = 20 Trunk CSL with Calling Number Display
C = 40 Trunk CSL
D = 40 Trunk CSL with Calling Number Display

G Power Subsystem (CC 49)
( ) A = AC Supply
( ) B = Battery Back-up

H Administrative Restriction (Telephone Numbers)
(CC 51-54)

Remarks

GCC 2075 8/74

Section II — (Cont J) Trunk Configuration

RCA Government Communications & Automated Systems Division

Sheet ___ of ___
Rev ___ Date ___
Control Number (CC1-15LJ)

Line No. CC 16-18LJ	Trunk Group Number	Trunk Access Code CC 21-22LJ	Trunk Restr Code CC 25	CBK CC 26	Total TW Trunks CC 27-28RJ	Total OG Trunks CC 29-30RJ	Total IC Trunks CC 32-33RJ	Total Qty Trunks CC 36-38RJ	Trunk Function Code CC 38-39
1001	Direct Outward Dialing Trunk Gr 1								
1002	Direct Outward Dialing Trunk Gr 2								
1003	Direct Outward Dialing Trunk Gr 3								
1004	Trunk GP 4 Unassigned								
1005	Rapid Wakeup Trunk Gr 5								
1006	Dial Access Paging Trunk Gr 6	Note 1							
1007	Oper. Access Paging Trunk Gr 7								
1008	Dictation Trunk Gr 8	Note 1							
1009	Trunk Totals								

Trunk Restriction Codes
Blank = Toll Terminal/TSPS
A = 0/1 Restriction on Local Area Codes
B = 3 Digit Toll Restriction
C = 0/1 Permit per Trunk Group

CBK Code
Blank = No CBK
K = CBK

Trunk Function Codes
DD = Local DOD on Local & Wide Area
LD = Long Distance
TL = Tie Line Service
MG = Multiple Trunk Group Access

Note 1. For Dial Access Code Refer to Section IV

GCC 2075-1 8/74

Fig. 3b — Automated ordering form — system configuration.

Table IV — Automated ordering program for phase II.

1) System parts accumulation list by ES and MI.

2) G.D. standard wiring decks (reference thereto)

3) G.D. custom wiring decks.

4) PIC standard wiring tape.

5) DITMCO tape for backplane printed wiring (reference thereto).

6) DITMCO tape for standard wiring plus printed wiring (reference thereto).

7) DITMCO tape for standard plus printed circuit plus custom wiring tape.

8) Module location chart.

9) Busy lamp field chart.

10) System loop list.

11) System position index list.

11) Line circuit assignments list by telephone number, class of service, paging, hunt group, and night answer assignments.

13) Trunk circuit assignments list by trunk access number, trunk type, group, and restrictions.

14) List of features and instruction book modifiers.

15) System price.

16) ES and MI usage list for an input to the automatic reorder program.

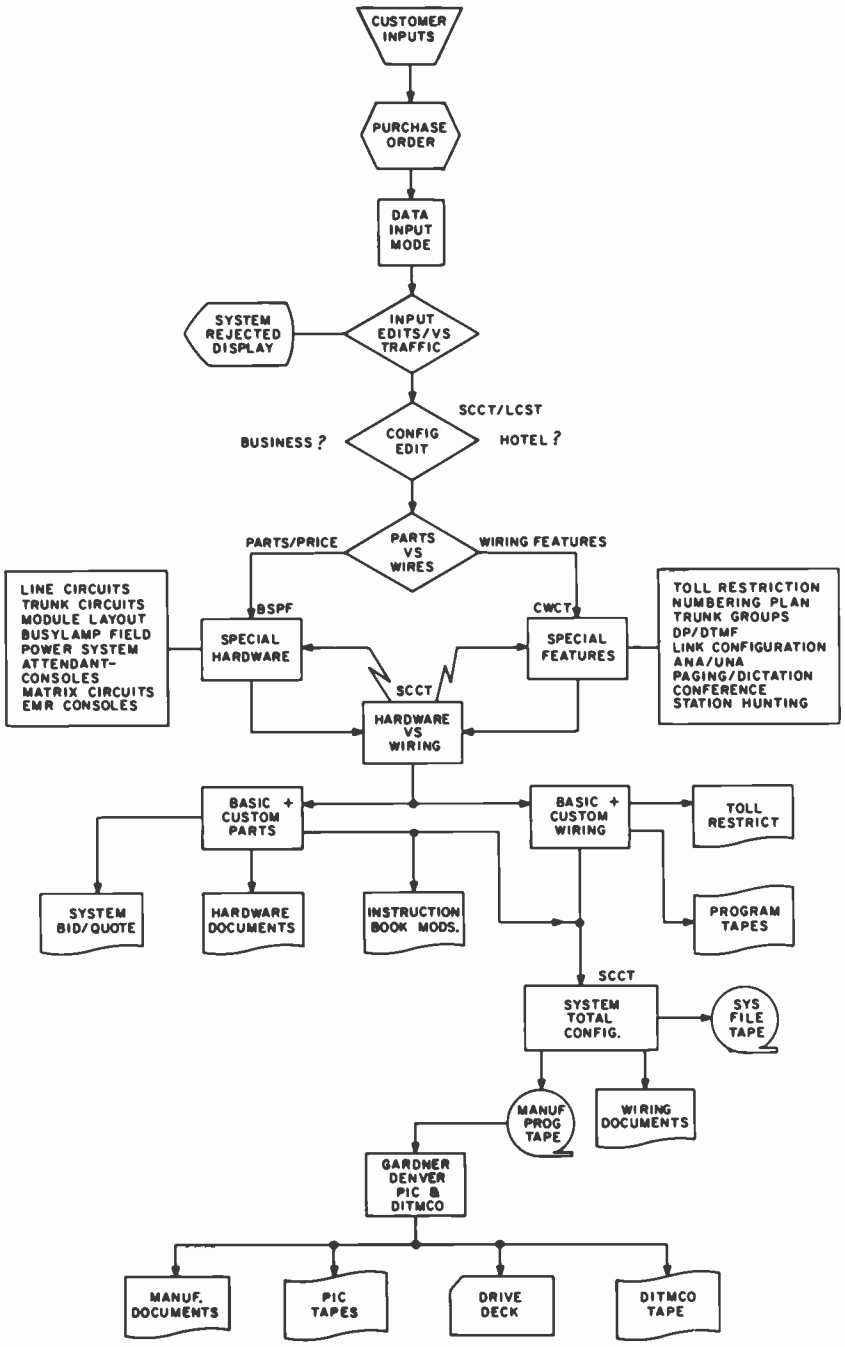


Fig. 4 — EPABX automated ordering and configuration control diagram.

The turnaround time for phase one is approximately four hours. From input to keypunch, to final program outputs—the complete program spans 8 hours running time, or a three-day turnaround maximum. The turnaround time with the associated advantages of accuracy and cost makes the use of this program for commercial business an economic necessity.

Operation

The *automated ordering program* is developed for use as a completely interactive operating system creating a variety of outputs to fully develop complete EPABX systems on a quick-reaction turnaround basis. The program provides support to engineering, drafting, and manufacturing in such areas as system tests, parts and inventory control, and field service.

A typical program operation is initiated when the customer requirements are translated by the equipment specialists into an input to the *automated ordering program*. This input may be inserted into the operating system by such means as punch-cards, seven- or eight-channel paper tape, key tape disc or direct image scanner.

The program files and tables control the automation program for the EPABX. These tables include: system configuration control, link (horizontals) configuration selection, basic switch parts file, and custom wiring control. Incoming data to the program is input edited for complete customer information by comparing the input against a master configuration file stored in the program data base. The validation process includes a validation of system size and class, model, traffic capability and mode of operation.

If the input data is incomplete or erroneous, the Phase I of the program will continue until it ends, and then display the problem areas in the incoming order. When the input edit is accomplished with no conflicts, the Phase II edit step may then be initiated.

The system configuration control tables (SCCT) are the master control file of the automation program. The SCCT houses the file numbers for all basic and optional or variable features and the file numbers for the complementary wiring to implement these features. In general, the SCCT contains an inventory or file of the basic and optional features and capabilities; SCCT contains the automation control indices for each of the available system configurations. The sequential chain of events of the SCCT program is to follow the format of the purchase order.

By comparing the requirements of a system to the capabilities of the systems stored in the automation program, the SCCT verifies that the system is valid and producible. The appropriate file control numbers of the SCCT then index the basic switch-parts file (BSPF) which, in turn, produces a tape of the parts complement for the system. The custom wiring control tables (CWCT) are then indexed, and a tape is produced which contains the complementary wiring for the implementation of all the features specified for the system.

The validity of the system size and class, traffic capability, and module complement is determined, in part, by the program assignment of the line circuits and trunk circuits. Line circuits are assigned in sequential order as determined by the telephone extension numbering plan. Trunk circuits are assigned according to their type, group and dial access codes. After the line circuits and trunk circuits have been assigned to a specific location, the SCCT indexes the link configuration selection tables (LCST). The LCST, in conjunction with the SCCT, tests the workload of the system to determine that the system requirements are within the capability of the system indexed by the SCCT. These tests include the following:

1) Check the feasibility of the features.

2) Check the parameters of each feature (essentially a quantitative check).

3) Index the parts complement for each feature and produce a magnetic tape file for all parts.

4) Index the complentary wiring for each variable feature and produce magnetic tape file of the custom wiring.

At this point, the basic system size and module complement is established. It should be noted that the ultimate system size and module complement is contingent on the many optional feature variables. Complete panels may have to be added when a feature is needed. As an example, if the traffic requirements of a system necessitates a link configuration beyond the capability of the basic switch, then the matrix expansion backplane is added. When all hardware requirements are satisfied, the program proceeds to combine all basic and custom data into a unique system control file for each PABX processed. This control file then proceeds throgh the program and, by interaction with the stored data base (basic + custom rule tables), begins to generate the many outputs required by those support areas previously mentioned. A library of drawings and price information is available at the end of the second SCCT process (hardware vs.wiring).

By executing the proper request, the program has the option of producing only quotation information or quotation information plus the parts lists, tabulations, and drawings from the *basic* plus custom-parts-file library tape. The following reports are generated from this file:

1) A line circuit tabulation which provides such information as line circuit card number vs. telephone number vs. card location vs. class of service vs. dial/manual call transfer vs. station hunt group and advises if equipped for night answering, paging, off-premise extension.

2) A trunk circuit tabulation which provides the following information: trunk card vs. trunk suffix vs. trunk access digit vs. trunk type vs. trunk group vs. trunk part number and trunk VCA vs. trunks appearing at console.

3) A parts accumulation tabulation by part number, quantity, location, type, and a total parts price summary sheet. This tabulation is to be used for parts accumulation and as an input to inventory control for each switch being built.

4) A busy-lamp field-layout drawing, showing lamp location vs. lamp number vs. room number.

5) A module plug-in location chart, showing rack and panel location, plug-in location, plug-in part number and type per location.

6) Summary usage list-trigger to the inventory control program.

After completion of the preceeding output tabulations, the automation program advances to the BPCW (basic plus custom wiring) file where optional features are recovered. Stored in this file (among others) are the tables for the restrictor function module where trunk permit/deny area and office codes for the particular switch are stored. Before proceeding to SCCT, a toll restriction tabulation is produced, showing trunk group number, and restricted telephone numbers.

The program finally goes into the phase of the SCCT where the library of documents is contained. For each system, a listing of drawings and other pertinent documents are provided. This listing consists of:

1) Connection lists and a listing of specifications. These listings include basic specifications and connection lists which are common to all systems, and variable specifications and connection lists which are dependent on and controlled by the selected variable system features.

2) An end-product switch definition tabulation, showing number of lines, trunks, features, and assemblies (as built to customer requirements). Assembly and part numbers to be used are included for manufacturing support.

3) A complete switch copper path and supporting pin index of used and spare pins.

4) A complete switch configuration magnetic tape for input to the Gardner Denver automatic wire-wrap machine program, semiautomatic wire-wrap program, and the DITMCO test automation program.

The program has several access points for changes. Such changes as the numbering plan, classes of service, number of trunks, etc., that affect hardware, wiring or both, may be fed into the program at discrete points prior to the generation of the system outputs (wiring decks and tapes, DITMCO tapes etc.). Changes at these points may salvage up to 90% of the computer time. It must be noted that once the loading charts are fed into the program (start of Phase II), changes cannot be implemented. The program must either be stopped and the switch reprocessed, or the changes be implemented manually.

The extended scope of the program and its flexibility may thus be adapted to any system or product where system variables are the norm, and the demand on documentation and manpower is excessive, and where accuracy, cost savings, and speed are paramount.

Electron tube radioactivity calculations

K.M. Finlayson| J. M. Forman

This paper outlines a procedure for calculating electron-tube radioactivity from known physical quantities. The procedure has been reviewed and approved by the JEDEC JT-16 Committee on Government Specifications and Standards and has been published by the Electronic Industries Association (EIA) as JEDEC Publication No. 89. The appropriate equation is derived and dimensional analysis is included to cover the wide range of radioactive decay rates.

RADIOACTIVE isotopes are, on occasion, intentionally added by manufacturers of electron tubes to improve tube performance or to increase tube life. For this reason, manufacturers may be required to determine the total radioactivity in microcuries per tube (μc/tube) to comply with existing Federal regulations. It is usually impractical to measure the radioactivity with any degree of precision. The radionuclide is often surrounded by electrodes, spacers, and an envelope such that the geometry considerations preclude a realistic calibration of a measuring device. Moreover, the amount of radionuclide added is often so small that the radiation is difficult to discern from the normal background radiation.

Because it is impractical to measure the radioactivity directly, the radioactivity for electron tubes shall be determined by a calculation technique in terms of the known radionuclides which have been intentionally added to the electron tube. One can calculate the radioactivity in μc/tube for an electron tube in terms of the mass of the radioactive nuclide and the specific activity of the nuclide. Specific activity is the rate of decay of one gram of the radioactive element or nuclide relative to the decay rate of radium.

Basic theory

The number of atoms (dN) in any one radioactive element that will disintegrate in a small interval dt is proportional to the number of atoms (N) present at the beginning of the time period dt.

$$-dN = \lambda N dt \qquad (1)$$

The fundamental law that describes the rate of disintegration or decay of a radioactive element is therefore as follows:

$$-dN/dt = \lambda N \qquad (2)$$

Rearranging Eq. 1 and integrating:

$$\int dN/N = -\int \lambda dt$$

or

$$\ln N = -\lambda t + C \qquad (3)$$

at $t = 0$, $N = No$; therefore, Eq. 3 can be rewritten:

$$\ln No = -\lambda(0) + C$$

or

$$C = \ln N_o$$

Referring to Eq. 3 again and replacing C,

$$\ln N = -\lambda t + \ln N_o$$

and

$$\ln N - \ln N_o = -\lambda t$$

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Jules M. Forman, Engineering Standards, Electro-Optics and Devices, Solid State Division, Lancaster, Pa., received the ME from Stevens Institute of Technology in 1940, was a teaching fellow at Stevens from 1940 to 1941 and did graduate work there from 1940 to 1942. He joined RCA Harrison in 1941, and transferred to RCA Lancaster in 1942. Since 1942, he has designed numerous electromechanical electronic test sets, life test equipments, and has worked on the special application of electronic circuitry. He was promoted to Leader of Special Equipment Engineering in 1951. From 1956 to 1962, his activity expanded to include Special Equipment and Environmental Engineering, having the additional responsibility for environmental engineering evaluation and testing of all new and improved tube ruggedization. From 1962 to 1970, Mr. Forman was Manager, Environmental, Special Equipment & Specifications Engineering in the Electrical Measurements and Environmental Engineering Laboratory. Since 1970, Mr. Forman has been responsible for Government Coordination Engineering with the military services for the Industrial Tube Division of Lancaster. Mr. Forman, since 1970, is the RCA Industrial Tube Division consultant member to the Joint Electron Device Engineering Council (JEDEC), JT-16 Committee on Government Specifications and Standards. The committee is responsible for the national coordination and recommendations of technical and other government related matters for the entire electron tube industry in conjunction with military technical advisors. Mr. Forman, is a senior member of the IEEE, Vice President of the Society for the Advancement of Management, a member of NSPE, and holds a Professional Electrical Engineering license in the state of Pennsylvania. Mr. Forman is also a Past President of Lincoln Chapter, PSPE, encompassing Lancaster, York, and Adam Counties.

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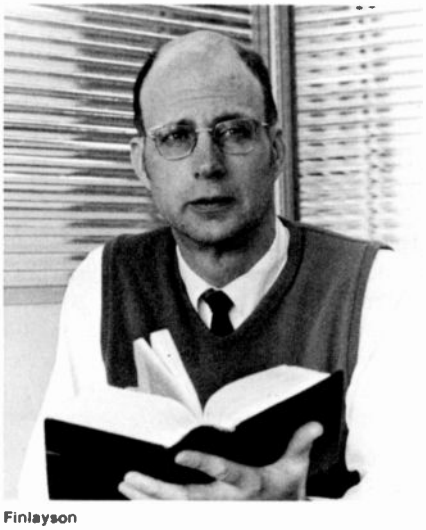

Finlayson

Forman

The natural logarithmic form to base e is:

$$\ln (N/N_o) = -\lambda t \qquad (4)$$

Rewriting Eq. 4 in exponential form:

$$\exp(-\lambda t) = N/N_o$$

$$N_t = N_o \exp(-\lambda t) \qquad (5)$$

Eqs. 4 and 5 are written in terms of the natural logarithm to the base e, a fundamental constant which applies to other natural phenomena as well as radioactive decay.

A simplified expression for the half-life time T can thus be derived from Eq. 5 as follows:

$$N_t = N_o \exp(-\lambda t)$$

since $N_t = \frac{1}{2} N_o$ in half-life time where $t = T$

$$\frac{1}{2} N_o = N_o \exp(-\lambda T)$$
$$0.5 = \exp(-\lambda T)$$
$$\ln 0.5 = -\lambda T \ln e$$

and the half-life time of the particular radioactive element is:

$$T = 0.0693/\lambda \qquad (6)$$

For radioactive decay calculations, the "half-life" is a more convenient parameter to use than the decay constant λ. *The rate of disintegration* (Eq. 2) can now be expressed in terms of the half-life T.

$$-dN/dt = 0.693N/T \qquad (7)$$

The decay rate for any radioactive substance is referenced to the decay rate of radium. One curie of a radioactive substance is that amount having an activity of 3.7×10^{10} disintegrations/second, the disintegration rate of radium. 1.0 μc is defined to be 3.7×10^4 disintegrations/second. Also, according to Avogadros principle, there are 6.02×10^{23} atoms in a gram-atom or in a mass equivalent to the atomic weight expressed in grams. Therefore, the number of atoms in one gram is:

$$N = 6.02 \times 10^{23}/A \qquad (8)$$

Therefore, the Specific Activity is:

$$S.A. = \frac{0.693}{T} \frac{6.02 \times 10^{23}}{A} \frac{1}{3.7 \times 10^4}$$
$$= \frac{1.13 \times 10^{19}}{TA} \qquad (9a)$$

Dimensionally,

$$S.A. = \frac{1}{\text{s}} \frac{\text{atoms}}{\text{g}} \frac{\mu\text{c}}{\text{atom/s}}$$
$$= \frac{\text{microcuries}}{\text{grams of radioactive element}} \qquad (9b)$$

It should be noted that Eq. 9 is based on a half-life, T, in seconds. $S.A.$ may be calculated for half-life in minutes, hours, days, or years by applying appropriate conversion factors.

To obtain the radioactivity in μc/tube:

$$\textit{Radioactivity} = S.A. \times \textit{actual mass} \qquad (10)$$

where the *actual mass* is the number of grams of radioactive element used in the tube.

If the radioactive element or nuclide is part of a mixture or a chemical compound, the specific-activity expression must be reduced by an amount corresponding to the fraction of the material which is radioactive because specific activity ($S.A.$) is expressed per gram of radioactive element rather than the compound.

Radioactivity calculation

The calculation of radioactivity is accomplished by substituting in Eq. 10 where the specific activity, calculated from Eq. 9, is multiplied by the mass of the radioactive nuclide that is used in the tube. Half-life values of radioactive elements may be found in Ref. 4.

An example of such a calculation is shown below:

Pure radioactive element

For Re^{187}, $T = 4.3 \times 10^{10}$ years and $A = 187$. If there is 0.1 gm of Re^{187} in a tube, Eq. 9 can be applied to compute $S.A.$

To express $S.A.$ in terms of T (years):

$$S.A. = \frac{1.13 \times 10^{19}}{TA} \frac{1 \text{ yr}}{0.3156 \times 10^8 \text{ s}}$$
$$= \frac{3.58 \times 10^{11}}{TA}$$

and

$$S.A. = \frac{3.58 \times 10^{11}}{(4.3 \times 10^{10})(187)}$$
$$= 0.445 \ \mu\text{c/gm}$$

Then, from Eq. 10,

$$\textit{Radioactivity} = 0.0445 \times 0.1 \text{ gm of } Re^{187}$$
$$= 0.0045 \ \mu\text{c/tube}$$

For several pure radioactive elements or nuclides

When more than one radioactive element or nuclide is present in an electron tube, then the radioactivity of each specie is determined (as above) and the radioactivity results can then be added to give the total radioactivity for the electron tube.

For several radioactive compounds in an electron tube

When more than one radioactive compound is present in an electron tube, then the radioactivity of each compound is determined and the radioactivity results can then be added to give the total radioactivity for the electron tube.

References

1. *Reference Data for Radio Engineers*, Fourth Edition (International Telephone & Telegraph Corporation, 1956).
2. *Sourcebook on Atomic Energy* (D. Van Nostrand Co. Inc., Princeton, New Jersey, 1970).
3. Electron Tube Radioactivity Calculations in Microcuries/Tube, JEDEC Publication No. 89 (February 1974).
4. *Radiological Health Handbook*, U.S. Dept. of HEW, Public Service Publication #2016, January 1970.

Definition of terms and symbols

A	Atomic weight of a radioactive element, expressed in grams/gram-atom.
N_t (or N)	Number of radioactive atoms of an element at time t.
N_o	Original number of radioactive atoms of an element at time $t = 0$.
$-dN/dt$	Rate of disintegration (the rate of change of N is negative because N is descreasing with time.
t	Decay time.
T	Half-life of a radioactive element or "nuclide." This is the time required for one half the number of atoms in a given element to disintegrate.
$S.A.$	Specific Activity, or rate of decay of one gram of the radioactive element or nuclide expressed curies or microcuries per gram.
λ	Proportionality constant for decay or disintegration of a given radioactive element (often called decay or disintegration constant).

The R-CAP program— an integrated circuit simulator

C.B. Davis | M. I. Payne

R-CAP is a computer program for simulating the detailed responses of electronic networks. While the program is particularly suitable for IC design problems, it has many features applicable to other technologies. For IC design, R-CAP provides a cost-effective tool which, unlike breadboard (analog) models, allows complete control of both parasitic effects and device parameters. Complete control for the designer is the main advantage of computer (digital) simulation of networks, since more accurate modeling of layout and device parasitics — and the examination of circuit design tradeoffs can be achieved. Also, the effects of processing spreads on circuit performance may be evaluated. Greater design flexibility has resulted in the increased use of computer simulation throughout the solid state industry, Ref.1. The salient features of R-CAP are described herein both from a user's and a program implementation standpoint, and the application of the R-CAP program to both analog and digital circuits design is discussed.

TO PERFORM a circuit analysis where a schematic diagram exists, the designer must first create a computer-readable file. Such a file must contain all the connectivity and component-value data represented by the circuit schematic.

Building and using the network file

The file (prepared in R-CAP language)[2] can be thought of as a deck of punched cards containing *all the pertinent data* (sourcing conditions, temperatures, etc.) required for a complete network description; as such, it becomes a computer model of the network to be analyzed. In reality, the typical R-CAP user enters information into the file on a time-sharing system (either NTSS or IBM/T-SO) in card image. Then, R-CAP is called upon to examine the network file for typographical and connectivity errors. R-CAP informs the designer of any errors and where they occur. Upon request, R-CAP gives the network's connectivity as output in another form, a node map, since R-CAP cannot diagnose all connectivity errors.

The designer then uses the file editor provided on the system to correct his file and resubmits it for analysis by R-CAP. After all errors of a syntactic nature have been corrected, request is made for a particular analysis and a display of the desired network responses in graphical or tabular form. At this point the user may choose to perform the actual simulation in a time-sharing (foreground) or batch (background) computing mode. Usually, the selection depends on the economics and system facilities of the computer installation: batch is cheaper but gives longer turnaround especially on smaller (<15 node) networks. A typical, though small for illustrative reasons, R-CAP file is shown in Fig. 2. Fig. 1 is a schematic for this network and Fig. 3 is the response calculated by R-CAP. After reviewing the response obtained, the designer alters the design (sourcing conditions, temperature, component values, topology, etc.) and resimulates until the specifications are met, and his problems are analyzed. Also he may elect to examine how tolerant the circuit is to processing variations so that manufacturing yield will be acceptable. R-CAP can determine validity or redundancy of test conditions and limits relative to specification — and assist in improving test times and yields, thus reducing costs.

R-CAP is flexible

The above description, while terse (a thorough treatment is given in Ref. 2), gives an idea of the features that R-CAP possesses. The program, written almost entirely in a "universal" high level language (FORTRAN-IV), requires less

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C.B. Davis, Design Automation, Solid State Technology Center, Somerville, New Jersey, received the BS in electrical engineering in 1962 from Pratt Institute and the MS in electrophysics from Polytechnic Institute of Brooklyn in 1964. In 1962 he joined RCA Laboratories as a research trainee. In 1965 he joined the Applied Mathematics Group at the Laboratories and worked on the application of digital computers to the solution of scientific problems. In 1967 he received an RCA Laboratories Achievement Award for work which culminated in the automated design of tools for the fabrication of magnetic deflection systems. In 1968 he received an RCA Laboratories Doctoral Study Award for a year's study toward the PhD in mathematics at N.Y.U. Upon returning to the Laboratories he initiated research on adaptive finite difference methods for approximating solutions to ordinary and partial differential equations. This work led to investigation into and analysis of implicit numerical integration formulas and sparse matrix algorithms. In 1971 he transferred to the Design Automation group of the Solid State Technology Center, Somerville and worked on developing software for analysis of nonliner solid state networks and model parameterization. Mr. Davis is a member of Tau Beta Pi, Sigma Xi, Eta Kappa Nu and ACM and is the author of several technical papers.

Authors Davis (left) and Payne

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than 200 kilobytes of memory and therefore is available on most of the major computer operating systems in use within RCA. These include IBM/TSO and OS, SPECTRA TDOS, and NTSS.

R-CAP looks the same to the user since his network file does not need modification dependent upon the computer system under which it is actually running. Since it runs in a time-sharing mode, R-CAP is interactive; therefore, long waits are not required to remove typographical errors from files. Indeed, the R-CAP language is designed to be format free, easily readable, well documented and logically consistent so that learning it is not a formidable task. In addition, R-CAP provides a comprehensive and explicit set of error messages which aid immensely in the program's use.

Another R-CAP feature is its flexibility in hosting all forms of analyses typically required in design problems. These analyses include dc, small-signal ac (frequency domain), and transient (time domain) analysis options. Thus, with a single description of his network in R-CAP language, a designer can obtain a complete set of responses, and then vary the designable parameters to meet specifications. The repertoire of responses computed is likewise extensive in that node voltages, branch voltages, device and supply pin currents, device power dissipation and supplied power can be calculated and displayed. The flexibility of being able to access a varied set of options through a single input language means that designers need not go through the laborious time-consuming and error-prone tasks of redescribing their networks to optimize design with respect to varied specifications.

Restrictions on network size currently imposed on R-CAP users are that there be: 1) less than 255 for the sum of nodes, sources and inductors; and 2) less than 850 components in the network. There are no restrictions on the number of individual component types (resistors, diodes, bipolar transistors, etc).

R-CAP contains built-in nonlinear device models for both bipolar and MOS transistors including parasitics, in addition to those for linear components and diodes. Methods of obtaining model parameters for bipolar devices are given in Ref. 2. The information required is

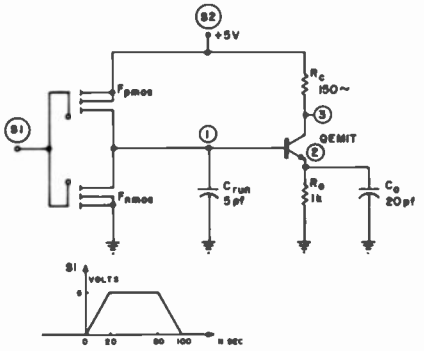

Fig. 1 — Schematic diagram of demonstration circuit.

```
  1 %MSG=NO
  2 BEGIN; R-CAP DEMO CONTAINING MOS AND BIPOLAR TRANSISTORS
  3 ;
  4 ; "CHIP" PARAMETERS (EXCEPT EOX) ARE GIVEN DEFAULT VALUES-
  5 #CHIP;EOX=3.82
  6 ;
  7 ;  MOS DEVICES ARE DEFINED BY-
  8 #FET1(PMOS):L=0.3,W=7
  9 #FET2(NMOS):L=0.3,W=4
 10 ;
 11 ;  DRAIN & SOURCE JUNCTION DIODES ARE DEFINED BY-
 12 #D1;CO=1.1E-12,FT=1E6,IS=1E-15,MO=1,PO=1E6,VO=1.5
 13 ;
 14 ;  BIPOLAR DEVICE IS DEFINED BY-
 15 #Q1(NPN);BI=0.5,CC=0.82E-12,FTI=2.65E6,IC=1.58E-13,MC=1.035,PC=5E5,
 16 +VC=0.75,BN=50,CE=1.08E-12,FTN=3.6EP,IE=4.85E-14,ME=1.001,PE=5E5,
 17 +VE=0.75
 18 SCALE TIME BY 1E-9; FROM HERE DOWN TIME IS IN NANOSECONDS
 19 SCALE CAPS BY 1E-12; FROM HERE DOWN CAPS ARE IN PICOFARADS
 20 ;
 21 ;  SOURCES ARE DEFINED BY-
 22 S1:000,5@20,5@80,0@100
 23 S2:5
 24 ;
 25 ; MOS DEVICE CONNECTIONS
 26 ;      R-CAP AUTOMATICALLY INSERTS ALL PARASITICS
 27 FPMOS:1,S1,S2,S2=FET1
 28 FNMOS:1,S1,0,0=FET2
 29 CRUN:1,0=5
 30 ; BIPOLAR TRANSISTOR CONNECTION
 31 QEMIT:1,3,2=01
 32 BF:2,0=1000
 33 RC:S2,3=150
 34 CO:2,0=20
 35 END
```

```
NODES=  3  VARIABLES=  3  SOURCES=  2  TEMP= 20R.0
 36 ."R-CAP DEMO CONTAINING MOS AND BIPOLAR TRANSISTORS"
 37 .RANGE:0,5
 38 .PLOT:1,1 2,F 3,C
 39 .TR:5,4.5,4.5
 40 .RUN:-25,200,10
 41 .SIM
```

Fig. 2 — R-CAP input data for the demonstration circuit.

```
OUTPUT ON DSET0


R-CAP V.B
   10/01/74 16:53:28


R-CAP DEMO CONTAINING MOS AND BIPOLAR TRANSISTORS
STATE AT T=-2.50E+01
NODE VOLTS
  5.000E+00   4.500E+00   4.500E+00
TIME(SEC/ 1.00E-09)          RESPONSE(* 1.00E+00)
          0.00E+00  1.00E+00  2.00E+00  3.00E+00  4.00E+00  5.00E+00
 -2.5000E+01 .....................................................C.....B
  1.5000E+01 .          .         .         .         . F C     I.
  5.0000E+00 .          .         .         .         . F C     I.
  5.0000E+00 .          .         .         .         . F C     I.
  1.5000E+01 .          .         .         .         . F C     I .
  2.5000E+01 .          .         .         .  F      I.        C.
  3.5000E+01 .          .        F    I     .         .         C
  4.5000E+01 .          . E       .         .         .         C
  5.5000E+01 .    I  F  .         .         .         .         C
  6.5000E+01 .I  E      .         .         .         .         C
  7.5000E+01 I..F.....................................................C
  8.5000E+01 I F        .         .         .         .         C
  9.5000E+01 IF         .         .         .         .         C
  1.0500E+02 .E  I      .         .         .         .         C
  1.1500E+02 .   E      I         .         .         .      C  .
  1.2500E+02 .          .F     I  .         .         .     C   .
  1.3500E+02 .          .        E .   I    .         .     C   .
  1.4500E+02 .          .          .  F     I         .    C    .
  1.5500E+02 .          .          .         E     I   .   C     .
  1.6500E+02 .          .          .       F     I     .  C      .
  1.7500E+02 .....................................F.....IC.......
  1.8500E+02 .          .          .         .        F.   CI     .
  1.9500E+02 .          .          .         .        F   C  I    .
STATE AT T= 2.00E+02
NODE VOLTS
  4.715E+00   4.068E+00   4.386E+00
>>
```

Fig. 3 — R-CAP's computer response of the demonstration circuit.

generally available from device data sheets or with relatively simple measurements. The MOS model is supported by a set of automated procedures[3] primed by data taken on test devices or off-the-shelf product; representative model parameter data are available from the authors. The program assigns default values for all device parameters reflecting the results of device characterization procedures. Defaults are, of course, overridden by any user-specified parameter inputs.

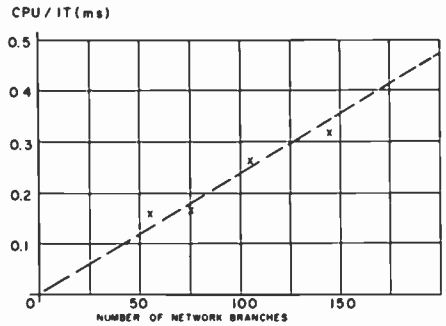

Fig. 4 — CPU time/iteration versus number of network branches.

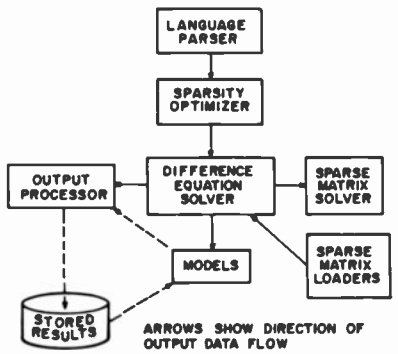

Fig. 5 — R-CAP program structure.

Analysis method and program structure

The tradeoffs discussed next involve formulation of a network equation which leads to economic simulation. There are numerous formulations of equations describing network behavior. Among these are the node, mesh, loop, cutset, hybrid[4] and state-variable for current and voltage laws and the branch constitutive relations for the network. It is clear, since formulations describe the same physical system, that they must result in the same network responses. Branin[5] mathematically proved the equivalence of formulations by showing them all equivalent to a more general tableau formulation.[6] It also is true that the mathematical probelm involved in obtaining network response is independent of the exact network formulation selected. Mathematically (at least in the case of transient response), the problem is to find the solution to a system of n-implicit nonlinear first-order differential equations in n-unknowns, given initial conditions on the unknowns. (In the case of frequency domain analysis, all time derivatives are replaced by $j\omega$ times the Fourier transformed variable and a linearization of the system is solved for the transformed variable). Thus, the system to be solved for the n-component network state vector, x is

$$F(x', x, p, t) = 0$$
$$\text{(given } x(t_o) = x_o\text{)} \qquad (1)$$

where F is an n-vector-valued, continuously differentiable, function in the $n+1$ arguments x and t; p is an m-vector consisting of the network parameters (*e.g.*, component and model parameter values, temperatures, etc.); x' is the derivative of x with respect to time.

Thus the variables at one's disposal in selecting a network formulation are the number of unknowns, n, and the extent to which one can exploit the fact that in real networks any node (or loop) is directly coupled to only a few immediate neighbors. The objective in this selection is to minimize computation time (simulation cost) including both network setup and actual response computation costs. In designing R-CAP the nodal-analysis formulation method was chosen to assure the smallest n and node-to-node coupling attainable for any given network. The small coupling achieved enables the systems to be structurally identical to the network incidence matrix.

Jessel[7] has used a statistical approach for determining the network equation formulation that is computationally optimum. One of his conclusions is that the nodal approach is somewhat superior, since it requires a lower level of software complexity than alternate approaches.

It has also been shown by Ho et al[8], that some of the previously-thought-of limitations in network modeling flexibility can be easily overcome when one adheres to the basic form given by Eq. 1. Our experience in using R-CAP (Fig. 4), indicates that the nodal formulation results in a CPU utilization roughly proportional to the number of network branches. We believe this type of performance to be optimal in that any formulation must result in evaluation of branch currents. Programming techniques and algorithms do, however, determine the size of the proportionality constant.

Program design

In designing a program to solve large systems in the form of Eq. 1, it is valuable, for reasons of extensibility of algorithmic and modeling features and software maintainability, to partition the problem into basic groups of software modules which interface relatively independently. The program structure (Fig. 5) does this effectively; functions of the various blocks are explained below:

The difference equation solver

The function of the equation solver is to obtain an accurate approximation to the solution, $x(t)$, of Eq. 1 with minimal computation cost and user intervention. In R-CAP, the algorithm to accomplish this consists of substituting a second-order numerical difference formula[9,10] for x in Eq. 1. The approximate solution, say $x_a(t)$, is then solved for the next simulated time-step given its values at the present time, and the two immediately preceding times. The procedure for computing x_a consists of solving the difference analog of Eq. 1 iteratively by Newton's method since the nonlinear models in the system must be converged. Automatic control is maintained on the time grid such that the largest time intervals are selected consistent with keeping the error, as measured by the difference between $x_a(t)$ and $x(t)$, and the size of F in Eq. 1 small.

Sparse matrix solver

A potentially-costly portion of the simulation process is the Newton iterative loop, since it is the most frequently executed step in the computation. Therefore, it should be as efficient as possible to assure good overall performance. Since Newton's method consists of solving a sequence of linearized versions of the actual nonlinear system, the problem of solving linear equations on a computer is really what is at the core of the algorithm. Furthermore, it turns out that the linear systems arising are sparse, having mostly entries with zero

values; this occurs since nodes are coupled only to a few (2.5 on the average[7]) neighboring nodes. In addition, the matrices occurring in the nodal formulation are symmetrically structured. If any $aji \neq 0$, then $aij \neq 0$ —and tend to be well conditioned. Round-off errors tend not to be amplified during the solution process. We capitalize on these features of the problem by storing all non zero entries in a linked-list data structure where symmetric pairs (*aij*, *aji*) are stored adjacently and fetched together. In this way, no zero-operand arithmetic is performed in the linear equation solution. If such properties were not exploited, computer time would be proportional to the cube of the number of network nodes instead of proportional to the far-smaller number of branches, as has been exhibited in Fig. 4.

Model modules

Each of these subprograms has the function of computing the contributions to the function F (*e.g.*, currents, charges, etc.) of Eq. 1. The contributions arise from a mathematical model for a physical device given the terminal conditions, (*e.g.*, voltages, model parameters, β, threshold, etc.) and the time or frequency for which response is desired. Since these modules are self standing (independent of R-CAP's internal data structure), their number can be easily increased by designers whose modeling requirements are not satisfied by R-CAP's repertoire of built-in models. Also, the model subprograms are usable for other tasks, such as device characterization studies.[1]

Sparse matrix loaders

This group of subprograms provides isolation of the model subprograms from the R-CAP's data structure. Thus, changes in data structure do not necessitate revision of any programs in the model library, either built-in or user supported.

Output processor

This section of code displays those output variables chosen by the designer from R-CAP's repertoire of network outputs. Among the tasks performed are:

a) the interpolation of the designer-selected results onto the user-specified grid since, as has been previously explained, the calculated grid is adaptively selected for optimal accuracy and convergence; and therefore is not the same as that selected by the user, and

b) the computation of auxilary output functions, such as device pin currents, power dissipations, etc., not calculated as part of the solution to Eq. 1.

Confining this function to a distinct package facilitates extension of R-CAP's repertoire of output functions without affecting other program blocks.

Stored results

R-CAP performs any of the user-selected output functions when given previously-stored simulation results (approximate solutions to Eq. 1). This flexibility is particularly useful when the designer wishes to re-run a simulation using different grids or output responses. The computational (cost) advantage of retrieving these results from a file, rather than incurring the cost of recomputing them, is substantial (typically in excess of a factor of 5). As indicated, the output processor operates equally well from stored or calculated results.

Sparsity optimizer

The most frequently executed tasks in analysis are sparse matrix inversion and evaluation of the function F (branch currents, etc.) in Eq. 1. Pre-optimization of the network matrix[12] is accomplished by reordering the network node labels which the designer has arbitrarily assigned. Optimization, which is carried out so as to minimize the *non-zero* arithmetic required to perform a sparse-matrix inversion, is only performed once — since optimization depends only on network topology (connectivity) and not component values. A second benefit of preoptimizing the network is that round-off errors are minimized since these grow in proportion to the square root of the number of non-zero arithmetic operations performed.

Language parser

This final group of subprograms is the one the designer sees. The language parser performs the function of translating the input file into a form usable by the previously discussed program elements. R-CAP's data structure is loaded with a set of tables (network parameter values, connectivity lists, run-time parameter values, etc.) to control the other parts of the program. The language parser also reports syntactical and some connectivity errors to the user. A detailed description of the R-CAP data structure follows.

R-CAP data base

One of the attributes of R-CAP contributing to its relatively low operating cost is the structure of its data base. There are a variety of methods employed to get the user's data checked and ready for the analysis section of a circuit analysis program. The method used by SCEPTRE, for example, is to generate FORTRAN code compiled and link-edited between the language parser's execution and the analysis section's execution. This method has a high overhead cost associated with using it.

R-CAP uses a table-driven scheme consisting of one large array to store all connection, parameter (model) and plot request data in a linked list structure. Table I below shows the structure blocks for: 1) component connections, 2) model parameters and 3) plots.

Table I — Data structure blocks for component connections, model parameter, and plot block.

Component Connection Block	Model Type No.	No. of Terminals	Tables of network nodes to which device is connected	Pointer to model parameter block	Pointer to plot block
Model Parameter Block	Model Type No.	No. of pieces (data)	Data		
Plot Block	Pointer to next plot block	Encoded variable and function selection entries	Encoded page no. and symbol to be plotted	Value(s) of variables to be plotted	

A typical model parameter block contains data fed in by the user. A copy of the block is modified for the temperature specified and stored for use by the analysis section. This obviates the need for recomputing model temperature dependence during analysis. It also enables parameter modifications for reruns, since the user's original input data has been saved.

In cases where data in connection blocks does not exceed the integer value of 255, up to four pieces of data are packed byte-by-byte into one four-byte word. Simple routines perform the packing and unpacking and little code is generated to put data into the data base or take data from it. The only limitation for the number of components and parameters etc., in R-CAP, is essentially the size of the large data array. There is no limit, specifically, on the number of transistors, only the total storage. This allows easy transfer from machine-to-machine without extensive program changes so that the user has access to larger machines for running larger circuits.

User models

The data-base structure of R-CAP allows a very powerful option, for the sophisticated user, which can be exercised at a small cost in computer time — unlike many other programs. The user can write his own model routines to replace or supplement R-CAP's built-in models.

Such model routines are invoked by the user-model connections allowed in the syntax, together with user-supplied model parameters. The user writes FORTRAN subroutines which a) check the parameter data, and b) compute branch currents and conductances, given the terminal conditions (*e.g.*, voltages) for each user model connected. The code needed for this task is relatively small, about 50 lines for voltage dependent resistors, for example. The user-model feature is a direct consequence of the previously mentioned modular structure of R-CAP. The user-model technique may be used for any component for which a numerically stable model can be devised.

Applications of R-CAP

Since R-CAP obtains cost-effective and accurate network response given the network model, the designer must assure that the network model is accurate. Even when the network is not *dead accurate*, it is often more accurate than a breadboard simulation and can be varied to tune network response by noting relative, and not absolute, changes in performance. Also *on chip* responses can be observed without changing that response due to the measurements.

R-CAP can be used in many circuit applications; however, there are some more suitable candidates for analysis than others. R-CAP is most suitable for analyzing ac and transient situations, rather than dc, because the dc models for the transistor and diodes in R-CAP do not have as many parameters as needed to specify a better dc model. Indeed, even when a better model is available, many parameters are difficult to measure.

In ac and transient analysis, the more suitable circuits are those where frequency and transient responses are determined by nodal capacitors, currents and resistors, rather than by internal transistor parameters. R-CAP's Ebers-Moll bipolar transistor model appears to be satisfactory for use at frequencies less than about $1/2\,F_t$ but above that becomes somewhat inaccurate, *i.e.*, it is satisfactory for most IC designs. The choice of the model is a compromise between operating costs, in terms of computer time and storage — versus the accuracy required. Many of the comments about bipolar transistors also apply to MOS devices, although insufficient experience within the Solid State Division does not allow as complete an evaluation.

An Arithmetic Logic Unit (ALU) functionally equivalent to the TI74LS181, was fabricated based on computer-aided design by R-CAP. The circuit consists of approximately 200 bipolar transistors and 100 dependent nodes. Measured propagation delays were near those predicted by the program. However, an investigation was made to determine if the speed could be improved without seriously increasing the power dissipation. R-CAP was successfully used to determine the areas where improvement could be made, and the *before and after* plots are shown in Figs. 6a and 6b. The ALU circuit was most suitable for R-CAP simulation for two reasons. First, the circuit could have been constructed as a breadboard, but the stray capacitances would have masked the areas giving rise to propagation delays on the chips, making such analysis rather futile. Second, hand calculations were considered difficult and inaccurate since the high impedances and low capacitances gave rise to many time constants whose effects could not be determined singly. This circuit cost $25/analysis on SSD's IBM 370/158.

The next example, the operational amplifier circuit shown in Fig. 7, demonstrates, the versatility of R-CAP. R-CAP was set up to give a unity-gain closed-loop transient run, followed by a

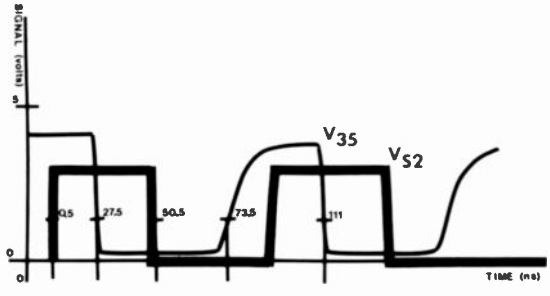

Fig. 6a — ALU response before tuning by R-CAP simulation.

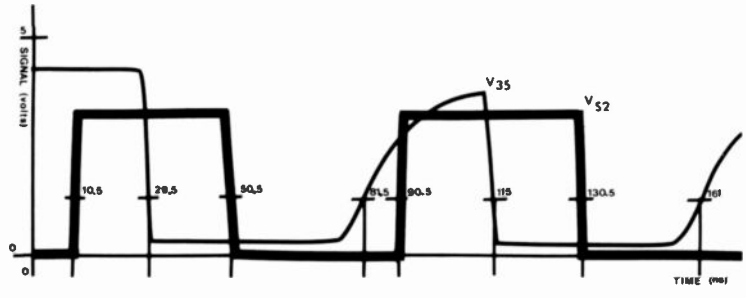

Fig. 6b — ALU response after tuning by R-CAP analysis.

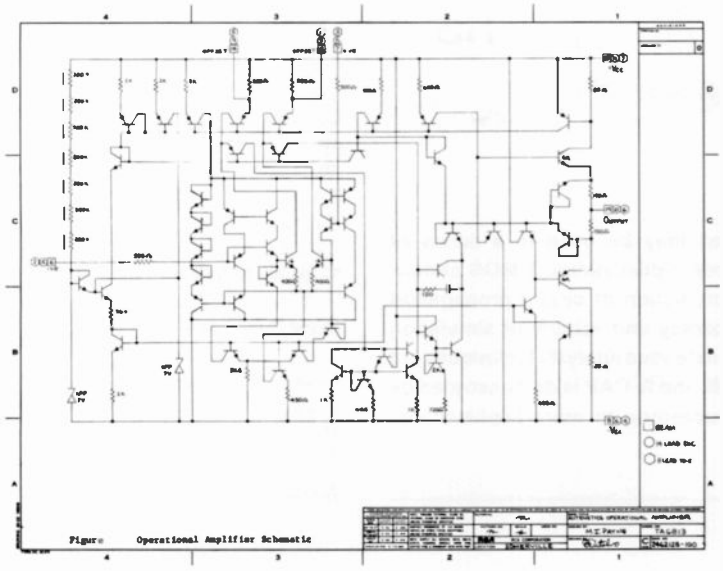

Fig. 7 — Operational amplifier schematic.

frequency and phase plot for unity gain.

Only a few simple commands were needed to obtain representative readings, and computer analysis comes nearer reality. The circuit cost about $50 to run on SSD's computer.

Breadboard *vs* computer

The philosophy used in high-speed bipolar integrated circuits for the design of linear and digital circuits has required the use of both breadboard and computer. The computer was used for these responses that are difficult to obtain from a breadboard; however, the breadboard has been used to determine overall performance, of say, an operational amplifier. The effects of *beta* falloff with input bias current, latch-up conditions, of interfacing with other circuits, can all be measured more readily using a breadboard and at a cost much reduced from that of the computer.

On the other hand, digital circuits, which could be evaluated by hand calculation for items the computer could not check, were never breadboarded and functioned as predicted.

Thus, the breadboard and the computer were used to supplement each other, and not to substitute for each other.

Management of R-CAP

The costs of operating a computer have never been negligible, neither have the costs of employing engineers. Therefore, before deciding whether or not to use R-CAP, an evaluation of the costs to be incurred by using R-CAP or not using it must be made. On the negative side, the cost of training personnel must be considered; along with this, the costs in computer time of learning errors and even the cost of a circuit failure by incorrect use of the program, as well as the actual computer cost must be considered. On the positive side, the lower cost of technicians due to less breadboarding is a factor, as well as a possible lower cost for necessary engineering time.

Once proficient in the use of computer analysis of circuits, it is the authors' contention that not only can total costs be lower, but the elapsed time of a circuit design and redesign cycle can be reduced. The time for the initial design is reduced as well as the probability of a second or n'th cut of the same circuit.

R-CAP as a problem-solving tool

Even though extensive design work and computer simulation may be done, Murphy's well-known law has determined that sometimes an integrated circuit may not work as expected, and indeed may not work at all. Such a circuit was an edge-triggered J-K Flip Flop. Extensive computer and hand analysis had been used in the design of this part. After construction, it was found that when the clock was left in the high state for extended periods of time, the circuit failed to operate at all. This input condition, previously not considered, was now simulated on an existing computer model; the rather obscure charging that caused the problem was immediately spotted. This permitted mask changes to be made rapidly, and the circuit subsequently functioned properly.

The point worthy of mention concerning this circuit, is that simulation by hand or by computer can only cover a reasonable number of possible conditions and not all, at least not economically or within the allowed span of time. Computers can look at internal voltages and currents not normally accessible, and help fix problem circuits more quickly.

Conclusions

R-CAP has been used over the past two years as a cost-effective design aid within RCA. The basic program design concepts embodied in it have been proved adaptive to a varied number of applications. Also its modular design philosophy allows for convenient future growth in both user options and cost-effectiveness. Our primary current interest is in economical device (process feedback) and network modeling since these are the areas that limit our predictive design capability.

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FETSIM and R-CAP programs in computer-aided design

W.A. Rauch

FETSIM and R-CAP computer-aided design programs may be used in a series of applications described herein. MOS circuit analysis, cost optimization, CMOS circuit-layout and design, master-slave flip-flop simulation, prediction of circuit propagation delays and drive capabilities, establishment of the accuracy and validity of simulation models, design of LSI arrays, and the use of advanced or extended analysis techniques are some areas considered by the author. The use of FETSIM and R-CAP is demonstrated by describing the least complex application first and proceeding to more sophisticated design needs.

Terms and symbols

V_{TP} ..... Threshold voltage *P* transistor
V_{TN} ..... Threshold voltage *N transistor*
L_{eff} ..... Effective channel length
μp ..... Mobility *P* transistor
μn ..... Mobility *N* transistor
N_D ..... Donor density
N_A ..... Accepter density
T_{ox} ..... Oxide thickness
Slope N (In Sat.) slope of drain characteristics N transistor
Slope P (In Sat.) slope of drain characteristics P transistor
C_{g-s} ..... Capacitance, gate-to-source
C_{g-d} ..... Capacitance, gate-to-drain
R_n ..... Resistance of polysilicon strip
I_{DP} ..... *P* transistor drain current
I_{DN} ..... *N* transistor drain current

THE DESIGN of CMOS-SOS standard cell LSI arrays can be optimized and design cost minimized by utilizing computer-aided design techniques. The use of such techniques eliminates the necessity for MSI and discrete-component breadboarding. Currently two programs (FETSIM and R-CAP) provide design assistance for CMOS-SOS standard cells and LSI arrays.

Two valuable programs

The FETSIM program is capable of performing dc and transient analyses of MOS circuits that employ almost any combination of resistive-capacitive elements, N-MOS transistors, and/or P-MOS transistors. The version of FETSIM which provides a graphic output capability on the Spectra 70 and the Calcomp-7000 series plotter is called FETGM4.

The R-CAP program has the added capability of being available on both a time-sharing and batch basis for transistor circuit analysis. R-CAP enables computation of the dc operating point and transient response of both bipolar and MOS transistor circuits. Both FETSIM and R-CAP provide graphic output as well as tabular output.

There are many areas requiring circuit design analysis where the two programs find application. FETSIM and R-CAP are particularly valuable in CMOS standard-cell circuit layout and design to ensure optimum drive capability and propagation delays. Program uses may be extended from the internal analysis of an individual CMOS cell (logic element) to the prediction of drive capabilities, edge times, and of propagation delays on LSI arrays, in the following examples: 1) between cells, 2) between arrays (chips) on a hybrid (substrate), 3) between hybrids on a *platter* (circuit board), and 4) between hybrids off the *platter* driving a transmission line.

Cell circuit optimization and characterization

The use of the FETSIM and R-CAP programs as computer design aids is more easily understood by examining the least complex of the previously mentioned applications and then going on to the more complicated.

Initially, consider the design and performance of the two-input *nor* CMOS-SOS standard cell shown in Fig. 1. The term "CMOS cell" may be easily understood by an examination of layout, schematic, and logic symbol of that device displayed in Fig. 1. The cell has been laid out (Fig. 1b) according to the required design rules from the circuit diagram (Fig. 1c) and logically performs the two-input *nor* function (Fig. 1a).

To determine performance, the program requires (as input data) the complete circuit topology, device parameters, process parameters, and control parameters. The user specifies initial node conditions, input-pulse rise and fall

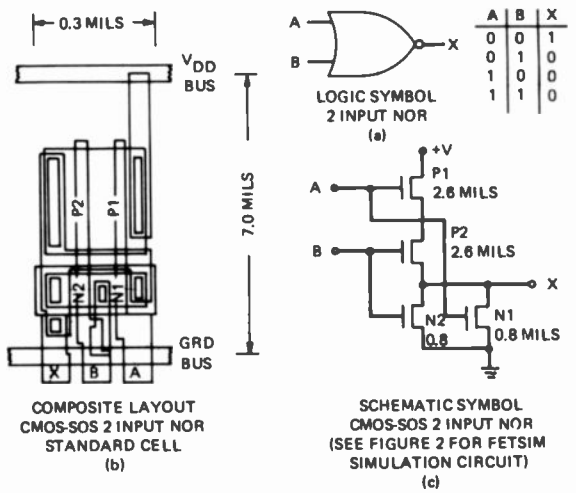

Fig. 1 — Two-input *nor* CMOS-SOS standard cell configuration.

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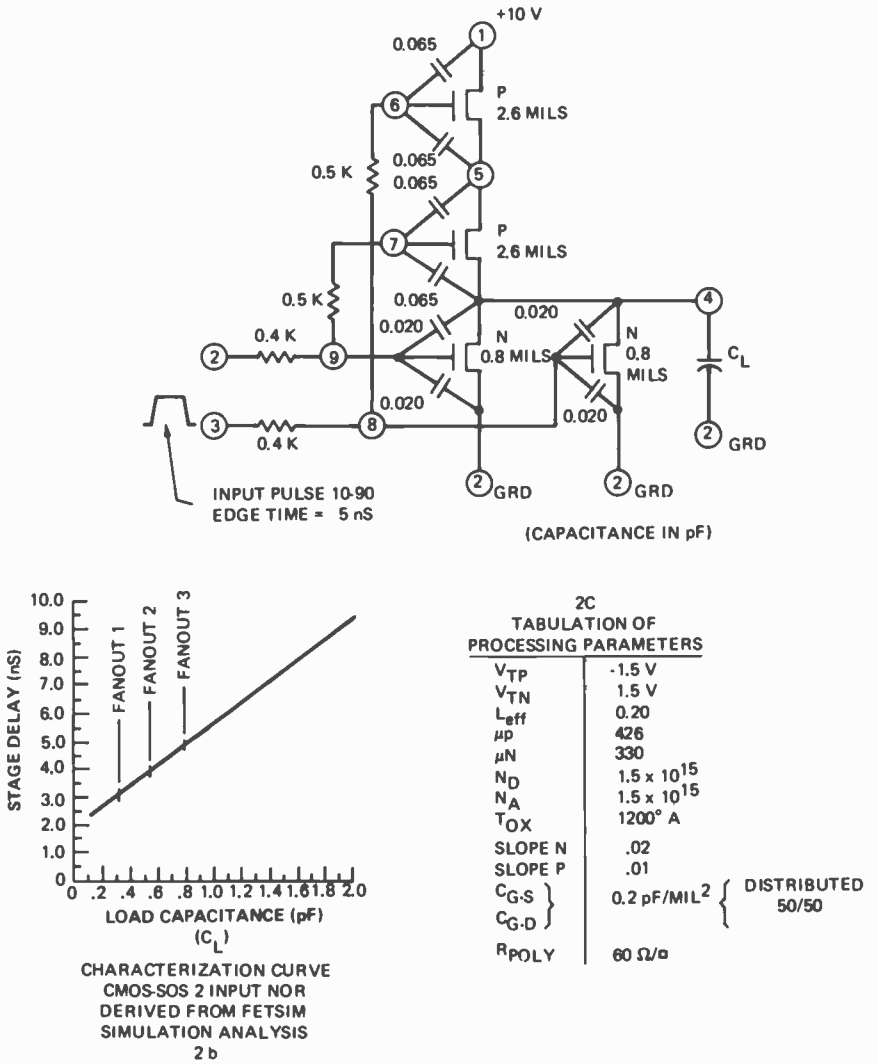

Fig. 2 — Two-input *nor* CMOS-SOS standard cell FETSIM model and characterization.

times, and the width and time between succeeding pulses. The FETSIM simulation circuit has been modeled from the cell topology and is shown in Fig. 2a. The circuit now includes resistive and capacitive elements not previously shown in the schematic of Fig. 1c. The values of R and C were calculated from a combination of the topology and the parameters displayed in the tabulation of Fig. 2c.

The gate-to-source and gate-to-drain capacitances were determined by multiplying the device's channel length (0.25 mils) by the channel width (0.8 mils for the N device and 2.6 mils for the P device); then, mulitplying the product by the process parameters of 0.2 pF/mil^2; and, finally distributing 50% for gate-to-drain and 50% for gate-to-source. Parasitic capacitances due to polysilicon and metal crossovers are negligible for this particular layout.

The resistance (R_p) of the polysilicon gate may be determined by counting the number of squares of polysilicon as related by the cell topology. The number of squares of polysilicon is then multiplied by 60 (ohms-per-square) to determine the gate resistance. If the term "square" is not familiar, consider a polysilicon strip 100 mils long by 0.4 mils wide. Dividing length by width gives 250 squares; then multiplying 250 squares by 60 ohms/square gives 12.5 kilohms.

Incorporation of the input data into the program permits FETSIM to simulate the circuit under transient conditions. The program prints out, in tabular form, the device currents and circuit nodal voltages as a functon of time and graphically outputs the same data if so requested. By varying the load capacitance (C_L, Fig. 2a), a complete characterization of the stage time delay as a function of C_L may be determined (see Fig. 2b).

From these same simulations, a 10 to 90% edge-time characterization curve may be obtained. Evaluation of these curves gives an indication of whether the device sizes have been designed to provide optimum drive and delay performance. Additionally, for an even more complex circuit whose performance did not meet anticipated requirements, the designer could determine (from the simulation data) exactly where the performance was deficient within the circuit model. Appropriate design changes in the cell layout to reduce unwanted parasitic capacitances and impedance paths, and revised device sizes to improve drive capabilities, could be made to improve performance, which would be verified through an additional simulation. The ability to quickly determine the performance effects of design changes without

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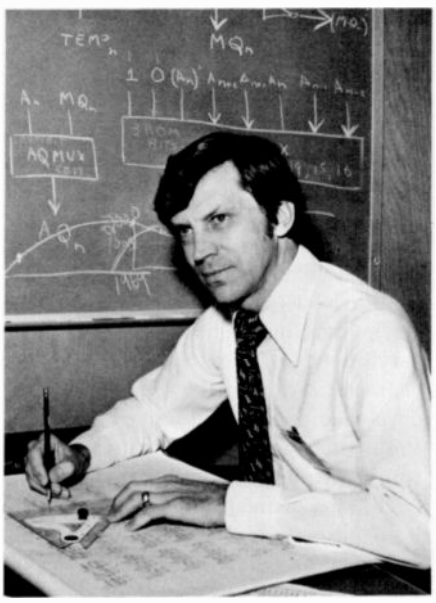


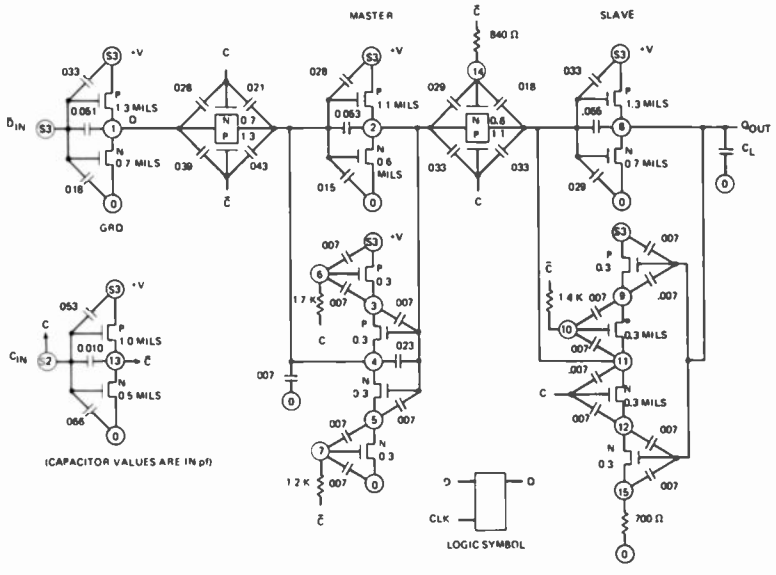


Fig. 3a — R-CAP simulation circuit and computer printout for a master-slave flip-flop.

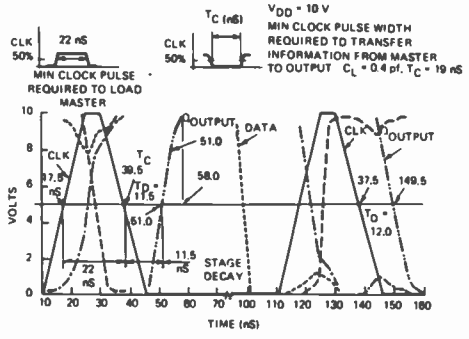


Fig. 3b — Clock pulse relationships for master-slave flip-flop.

having to process and test the chip is a key advantage of the circuit simulation.

The same type of simulation applied to a more sophisticated circuit, such as a master-slave flip-flop, serves as another example to demonstrate computer-aided design. In this example, the user determines: 1) the minimum clock-pulse width required to load the master, 2) the minimum clock-pulse required to transfer information from the master to the output as a function of load capacitance, and 3) the overall time required to clock through data (also as a function of capacitive loading).

The R-CAP simulation circuit of this master-slave flip-flop is shown in Fig. 3a, along with the computer printout indicating the points of interest mentioned above. Fig. 3b displays: 1) an 11.5-ns stage delay measured from negative-going clock to positive-going output, 2) a 22-ns minimum clock pulse required to load the master, and 3) a minimum width clock-pulse of 19 ns required to transfer information from the master to the output. This simualtion was based on a 15-ns, 10-to-90% rise or fall time for the clock signal and 0.4 pF load capacitor. By varying the load capacitance, a complete characterization of the flip-flop may be developed with additional computer simulations. These same simulations would also be evaluated to optimize the circuit design and performance previously described, and would exhibit any suspected race conditions existing within the circuit at the single-level logic stages.

Characterization data and curves such as those exhibited in the "Standard-Cell C-MOS LSI-Array User's Manual", published by the Advanced Technology Laboratories (ATL), Camden, for CMOS bulk silicon, metal-gate technology—are presently being generated also for the CMOS-SOS, silicon-gate technology. The characterization data, which will be included in that publication is directly obtained by the application of computer-aided design techniques to optimize cell performance, as described above.

Simulation and analysis validation

Before additional applications of these programs as design aids are described, the accuracy and validity of the simulation will be demonstrated to establish complete confidence in the simulation model. This has been accomplished by measuring, in the laboratory, the overall chain delay of the eight-stage, two-input *nor* chain (including output buffers), shown in Fig. 4. The 17.5-ns time delay shown in Fig. 4a was measured on a CMOS-SOS standard cell LSI test array designed by ATL to demonstrate the potential and effectiveness of the standard-cell SOS technology. The measurement was photographically documented and included in a report evaluating the first single sampling of the test chip. Obtained also from this same test chip were the *N* and *P* test-transistor drain characteristics, similarly documented, photographically, from a curve tracer.

After an actual delay measurement and a set of transistor parameters from the test chip are obtained, the processing parameters used in the simulation model may be revised to closely approximate, by simulation, the measured drain characteristics. Once a match is obtained between the simulation and measured transistor characteristics, a FETSIM or R-CAP simulation of the two-input *nor* chain (Fig. 4a) may be made and compared to the 17.5-ns measured delay. The drain characteristic match obtained is displayed by the curves of Fig. 4b. The figure shows a plot of the measured and simulated drain currents for both *N* and *P* devices. Varying the mobility (μp and μn) and the curve slope (slope *N* and slope *P*) tabulated in the list of processing parameters (Fig. 4c) enabled the generation of this simulated curve. Further revision, particularly to the doping levels (N_D and N_A) and threshold (V_{TN} and V_{TP}) would have even more closely approximated the measured curve. The simulation of the two-input *nor* chain revealed an overall chain delay of 18.9 ns, as compared to the 17.5 ns measured delay — an 8% difference.

Without further improving our simulation model, additional simulations must be considered to be slightly conservative and accurate to within approximately 10%. This difference of 8% may be attributed particularly to the inaccuracy of measuring the load capacity of 5.5 pF at the output pin of the test chip. Further refinement of the simulation model should ultimately give exact simulated comparison with the measured data.

Having established a degree of confidence in the simulation model, the user can predict within reasonable accuracy the actual single-stage delay of the CMOS-SOS standard-cell two-input *nor*. Investigation of this simulation

revealed an 8.4-ns delay for the two buffer-inverters at the end of the chain of Fig. 4a. The end of the chain delay of the measured 17.5-ns delay may then be obtained by calculation to be 7.7 ns. Subtracting this end-chain delay from the overall delay gives a 9.8-ns delay for the six-stage, two-input *nor* chain on the test chip. This remainder, divided by six stages of two-input *nor*'s, gives a stage delay of 1.63-ns single-stage delay for the test chip cell. This may be compared to the 1.70-ns delay obtained from the simulation of Fig. 4a.

LSI array computer-aided design

Of particular interest to the LSI designer are drive capabilities and propagation delays both on and off the chip. An approach to analyzing these problem areas is delineated by the diagram represented in Fig. 5.

In the center of the diagram, a square represents an R-CAP or FETSIM model of the cell or circuit under analysis. At the input side of the circuit under analysis, an *RC* coupling network represents the resistance of the chip's polysilicon interconnects and the capacitive coupling between polysilicon and metal crossovers. The importance of this coupling network is in its effect upon the input signals edge time. At the input to the coupling network, an R-CAP or FETSIM-modeled inverter drive circuit more realistically simulates the input signal to the circuit under analysis — and eliminates the possibility of infinite drive capability. At the output of the circuit under analysis are additional coupling networks, representing a fan-out of one or more. Attached to the output of the coupling network, a load capacitor represents the capacitance driving the chip — or perhaps the input capacitance to another cell on the same chip, or any combination of capacitive loading that might enter into the analysis.

The values of *R* and *C* to be used in the analysis shown in Fig. 5 would be calculated from the topology of the APAR-generated routing and placement

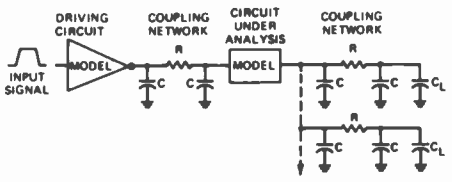


Fig. 5 — Simulation technique, schematic diagram.

composite diagram of the LSI array. In fact the LSI designer may intuitively assign values in order to perform initial analysis prior to fixed placement of the CMOS-SOS standard cells on the array.

Determination of polysilicon resistance values for R may be determined from the topology by counting the number of polysilicon squares and multiplying by 60 ohms/square, as previously described for characterizing and optimizing the two-input *nor* cell. Typical values for polysilicon interconnects generally range from 1 to 2 kilohms.

The value *C* may be determined from the area overlapping at the crossover points of polysilicon and metal interconnects. To clarify this consider the metal as a wire bus that electrically connects two points on the LSI chip. Passing orthogonally beneath this metal, but separated by an oxide insulation, is the polysilicon interconnect strip. The area of overlap multiplied by 0.033 pF/mil^2 (for a 6000-Å-thick oxide) gives the capacitance contributed by the crossover of polysilicon and metal. Typical values of *C* range from 0.02 pF for a single crossover to 3.0 pF for several crossovers. The resistance and capacitance should be appropriately distributed, so that the simulation model better reflects the real conditions under analysis.

Variations of this analysis technique may be applied to the many different drive and time-delay situations previously mentioned. Consider for instance the square representing the R-CAP- or FETSIM-modeled circuit to be analyzed in the example of Fig. 5 just discussed. This method provides a technique, through simulation of existing conditions, to evaluate the output driving stage of the circuit under test. If the output buffer was required to drive a 30-pF load in 20 ns over a 10-volt operation, the analysis (including all load and parasitic capacitances, and interconnecting path resistances) would demonstrate the effectiveness of the cir-

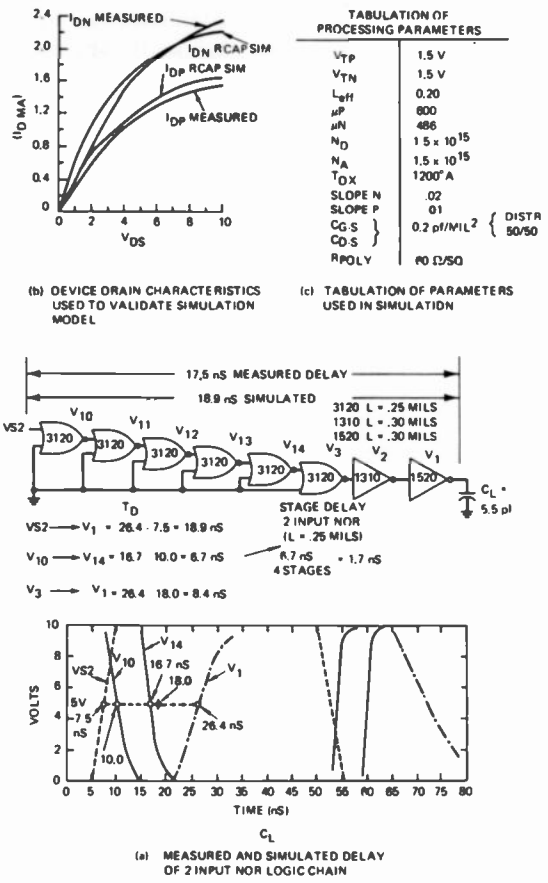


Fig. 4 — Simulation of a test chip logic chain.

cuit design. Obviously, depending on whether the simulation favorably verified the anticipated operation or demonstrated its inadequacy, design changes impacting either the cell design or revised interfacing with the circuits output would have to be considered.

Extended CAD analysis techniques

An extension of the previously described analysis technique serves as an initial attempt at analyzing a tristate driver scheme with bipolar off-substrate drivers and transmission line termination (see Fig. 6).

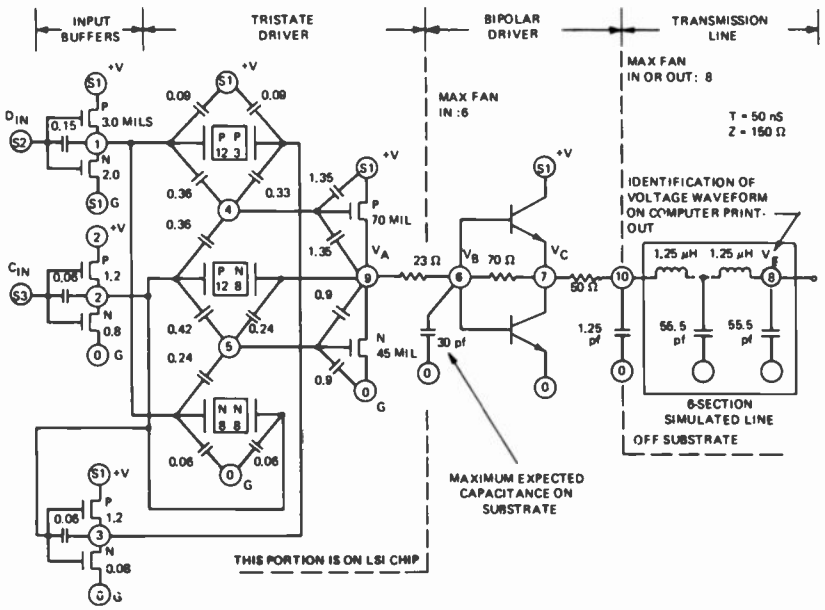
Since reflections developed by an improperly terminated transmission line might be of sufficient magnitude to produce false logic levels or exceed circuit voltage specifications, this extended technique was included in the R-CAP simulation of the tristate driver depicted by Fig. 6. The transmission line is characterized in the simulation by its 50-ns delay (T_D) measured between nodes V_D and V_E and its characteristic impedance of 150 ohms (Z_o). This particular simulation was made with the transmission line unterminated, and displays an undershoot of 2.2 volts and an overshoot of 3 volts. The output drive capability is demonstrated by the plot of node voltage, V_A, at node 9 shown in Fig. 6. The 10 to 90% edge time is approximately 30 ns, driving into the resistor, and 30 pF maximum expected capacitance off chip; these values meet anticipated design specifications for drive capability. An additional simulation, revised to include additional fanouts of transmission line, should reduce $L\,di/dt$ effects. However, this consideration, as a method to reduce reflections by increasing the fanout, also introduces crosstalk due to mutual capacitance and mutual inductance which cannot be neglected.

The simulation also reveals that the effect of the 50-ohm protective resistor at the bipolar output is to make the transmission line delay 4.5 ns longer, as shown by the 54.5-ns delay between V_C and V_E in Fig. 6. This particular analysis is incomplete and is presented here merely to demonstrate the practicality of applying R-CAP to this type of problem.

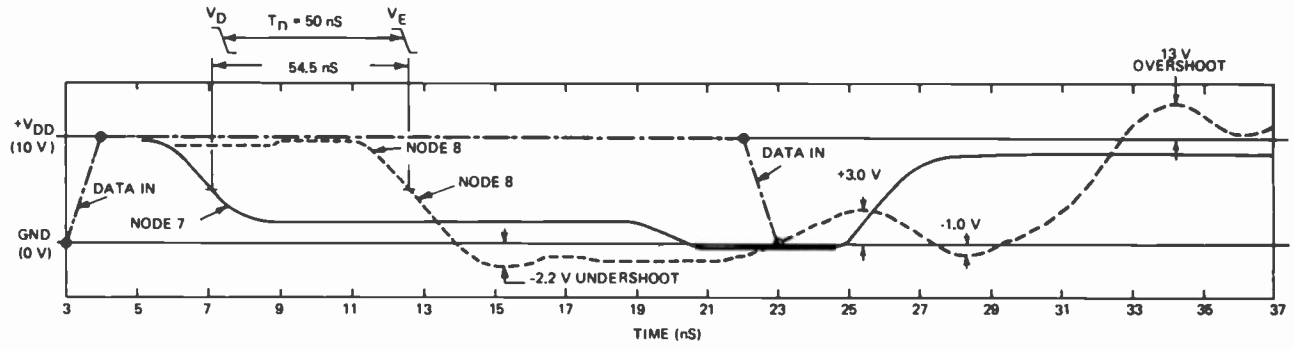
Conclusion

The use of the foregoing simulations and analysis techniques in computer-aided designs is not limited to the applications described. For instance, the design engineer may want to introduce into his program of design and analysis, investigations into such areas as input capacitance, or input and output transfer characteristics as typical examples. In addition, the advantage of simulation over breadboarding is the ability to investigate the effect of varying processing parameters without waiting for new devices to be made, with the accompanying costs of varying process variation and manufacture. The actual abundance of data to be derived from the R-CAP and FETSIM simulation is limited only by the amount of innovative application.

Access to the R-CAP circuit analysis program may be achieved through the RCA Solid State Technology Center (SSTC), Design Automation, Somerville, New Jersey. The FETSIM program may be accessed through the Advanced Technology Laboratories, Camden, N.J.



(a) SIMULATION CIRCUIT



(b) COMPUTER-DEVELOPED CHARACTERISTIC CURVES

Fig. 6 — R-CAP simulation circuit and computer printout for a tri-state driver.

Power-transistor reliability

D.M. Baugher| L. J. Gallace

Improved field failure rates for power semiconductor products are a primary user consideration in the mid 1970's. Although this consideration is not new, there is a new commitment by automotive, television, and other manufacturers to spend additional dollars to buy products that have undergone special screening and testing. The trend indicates that another level of awareness and sophistication has been reached in dealing with the problem of field failure. This paper describes, for power transistors, some reasons for the trend, methods and test procedures for achieving more reliable field performance, cost impact of screens, and hermetic versus plastic-package considerations.

THE military and certain equipment manufacturers have long recognized the need for high-reliability parts, and have paid a premium for JAN, JAN TX, and parts manufactured to demanding high-reliability specifications. These parts command a premium price of three to six times that asked for comparable commercial parts; Table I offers a comparison of prices and explains how various JAN TX types differ from commercial types. The obvious explanation for paying such a premium for high-reliability is that field failure either must be minimized or eliminated. The loss of a military weapon or weapons system or the loss of life justifies the added cost.

In the consumer industry, however, the cost of a failure cannot always be well defined. Poor performance of a particular product will surely cause a loss of image and sales, and hence represents a cost; but this cost is not easily determined. Fig. 1 emphasizes in a general way the consumer-product manufacturers' dilemma by plotting warranty costs and component-reliability costs against reliability. Since component cost skyrockets as reliability approaches 100%, it is obvious that less than 100% reliability must be tolerated.

Undoubtedly, the biggest single factor affecting field-failure emphasis is warranty costs. Recent consumer awareness of the manufacturer's liability to keep a new product operating over the warranty period has created the concomitant consumer awareness that significant warranty protection is worth dollars. However, in most cases the consumer does not wish to pay more for this protection. The net result is that different manufacturers have similar warranties for similar products and provide competitive pricing. The problem now becomes one of trading off parts cost for reduced warranty costs to establish a favorable image of reliability for the product being sold. An example will clarify this point.

Fig. 2 shows the relationship between warranty cost for repair, improvement in device failure rate, and additional dollars that can be spent on an improved device. If a radio warranty cost is $10 and the field failure rate can be reduced by 1%, then for every 100 radios, a service call costing the manufacturer $10 can be avoided; this expense, when applied to 100 radios means $10/100-radios or $.10 per radio extra can be spent in manufacturing costs. In other words, the profit picture for the manufacturer remains the same, his field-failure rate is reduced, and his customer satisfaction improves. The desirability of such a trade-off is obvious.

Other factors have also created pressure to improve device capability. In the case of automotive electronics, safety and performance criteria have been legislated.

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Table I — Economic factors in military high-reliability discrete devices (JAN, JAN TX, JAN TWX Specifications to MIL-S-19500).

Type	*Description*	*Price Comparison* Com'l	*JAN*[1]	*JAN TX*[2]	*JAN TXV*[3]
2N2857	SMALL SIGNAL H.F. RF AMP	$1.98	$2.30	$6.30	$ 9.30
2N3055	L.F. POWER TRANS.	1.05	1.44	6.00	9.00
2N3585	H.V. POWER TRANS.	1.68	3.40	7.20	12.20

[1] JAN types are exactly the same as commercial types except for documentation and certification procedures. They are government inspected.

[2] JAN TX types are subjected to 100% burn-in and are tested after burn-in. The fabrication of burn-in racks presents a major problem in economics and logistics. 100% burn-in can be effective in removing infant-mortality failures.

[3] JAN TXV types receive 100% pre-seal visual inspection

To meet these requirements, power semiconductors must be used. These devices must now compete with very reliable, simpler mechanical devices that have been perfected over the past 50 years. The new electronic systems represent additional failure modes that didn't exist before, and most importantly, warranty costs must be controlled.

To summarize, the recent emphasis on reliability relates primarily to consumer awareness and the need to control warranty costs. These factors, along with the consumer-product manufacturer's realization that a trade-off in parts cost and warranty cost is to his advantage, have meant that he is willing to pay more for improved devices. The possibility of getting more money for an improved device has caught the attention of semiconductor manufacturers. It remains, therefore, to investigate how this possibility can be realized.

Trends in reliability

The experience of electronic-component manufacturers has shown that consumer-product manufacturers whose production exceeds several hundred thousand pieces of equipment per month are requesting AQLs (acceptable quality levels) of 0.25% and, in some cases, 0.1%. If this request is meant to reduce incoming inspection losses or provide lower line-failure rates, then it has merit. If, however, this request is made on the assumption that lower field-failure rates will occur, then it is a questionable procedure, since compliance to electrical specifications does not guarantee long life. The cost penalty for these very low AQL's can be considerable due to extra precautions and test procedures that must be observed by the component manufacturer. The typical range of this cost premium varies from 1 to 5 cents per device for relatively simple electrical parameters.

Field-failure rates for components produced in large volume are typically less than a few percent. Typical rates vary from that for a troublesome part, which may be over 1%, to that for simple diodes with little stress, which may approach 0.01%.

Few consumer-product manufacturers are satisfied with a field-failure rate of 1%; most would like to see 0.1%. Fig. 2 shows that, for this performance, an additional incurred cost of five to ten cents could probably be supported by the manufacturer. Based on this economic limitation, the problem cannot be solved with elaborate 100% screens, such as burn-in or pre-seal visuals. Heavy documentation and serialization of product should also be avoided. The task of picking out the one unit in 1,000 that will fail during an equipment-warranty period is obviously a formidable challenge.

A beginning

There is no simple method by which a semiconductor that will provide field-failure rates that approach a few tenths of one percent can be chosen. The concept of defining several levels of reliability is a useful starting point. Six levels of reliability have been suggested:

Level 1 — Commercial product — off the shelf.

Level 2 — JAN types — same as commercial parts except for documentation and certification procedures. They are government inspected.

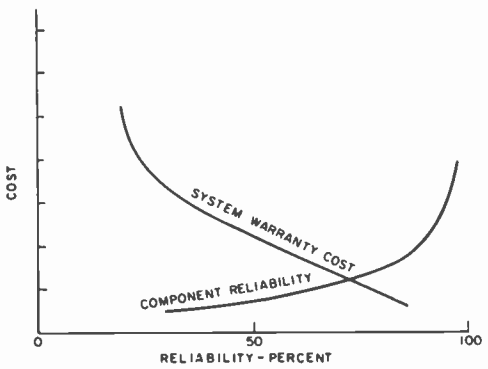

Fig. 1 — Warranty costs and component-reliability costs as a function of reliability.

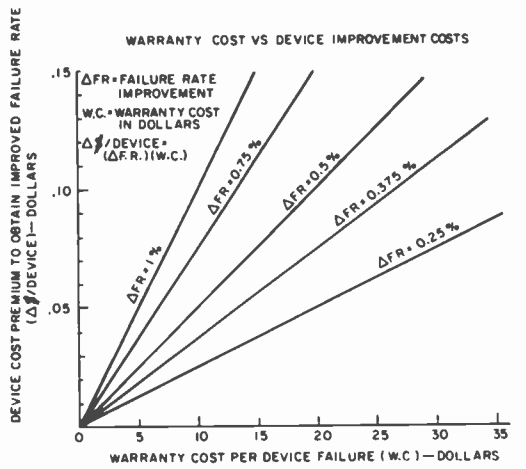

Fig. 2 — The relationship between warranty cost for repair, improvement in device failure rate, and additional dollars that can be spent on an improved device.

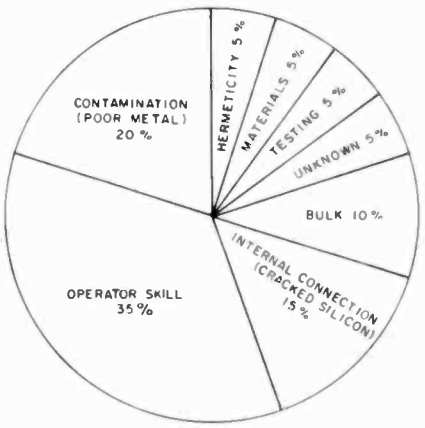

Fig. 3 — Typical failure modes for the TO-3 hermetic package.

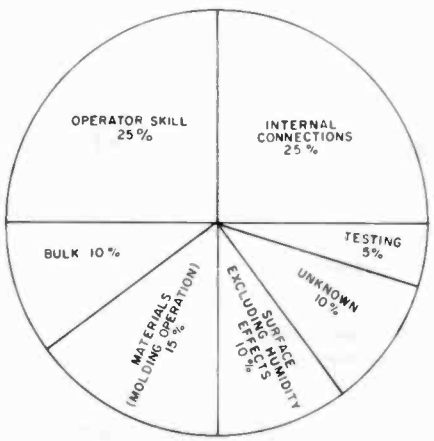

Fig. 4 — Typical failure modes for the TO-220 VERSAWATT package.

Level 3 — Commercial product — real-time controls plus 100% electrical screens for reliability.

Level 4 — JAN TX — 100% burn-in, serialization of product required.

Level 5 — JAN TXW — JAN TX with 100% pre-seal visual.

Level 6 — Captive Line — quality and reliability assurance provisions rigorously specified by user.

Level 3 is discussed in detail below.

Good field performance depends on at least two factors:

1) Is the device specified and used properly?

2) Is the device inherently reliable when used properly?

The following guidelines have been used successfully in the past.

Electrical considerations

Voltage breakdowns — Use low-energy devices at 70% maximum rating and high-energy devices at 90% of maximum rating.

Current gain — Provide pad of 15 to 20% to allow for degradation.

Leakage — Be careful to separate circuit needs from reliability considerations, such as surface stability.

Energy test — Provide I_s/b protection for forward bias conditions; E_s/b protection for inductive circuits.

Reliability considerations

High-temperature tests — Guarantee high-temperature performance.

Low-level leakage — Test for stability.

Delta temperature — Provide adequate heat-sinking to minimize T_c.

Operating temperature — Operate at 50 to 75% of maximum rating.

Transistor protection — Protect power transistors from electrical transients.

Equipment manufacturers should write specifications to show clearly which parameters dictate circuit operation and which parameters indicate reliability requirements. The advantage of this method is that, as product improvements are made, some reliability tests can be modified or eliminated with the result that costs can be reduced without influencing circuit operation. This method is also highly desirable when it is considered that often the people who originate specifications then move on to other assignments.

Factor 1 (above) considerations, those concerning proper specification and use of a device, can be largely performed by the user with some help from the supplier. Factor 2 considerations, those involving inherent reliability, can only be resolved by a combined effort of the user and supplier. Factor 2 considerations are the more subtle, and have received considerable emphasis recently. The concern is with failures which apparently occur within specification ratings and that relate to long-term performance. The key to any meaningful approach in improving long-range performance is failure analysis. Field failures must be analyzed to determine basic modes and mechanisms of failure. Once the modes and mechanisms are established, accelerated tests must be designed to correlate with the actual application so that the cause of failure may be determined in the laboratory. The supplier must then institute a design program to improve and control the product. Finally, the new product must

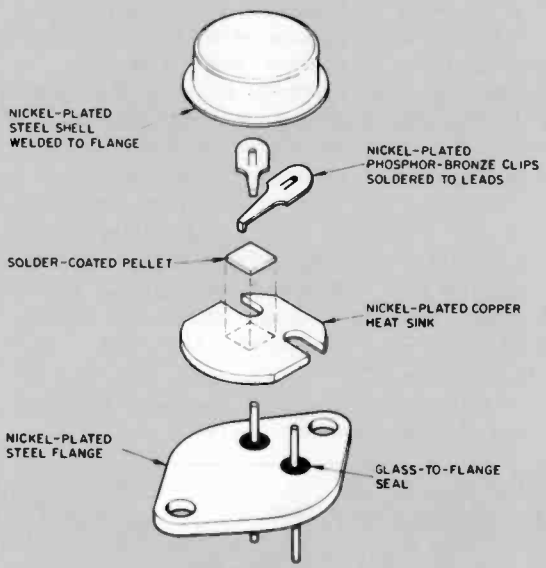

Fig. 5 — Construction of the RCA steel TO-3 package.

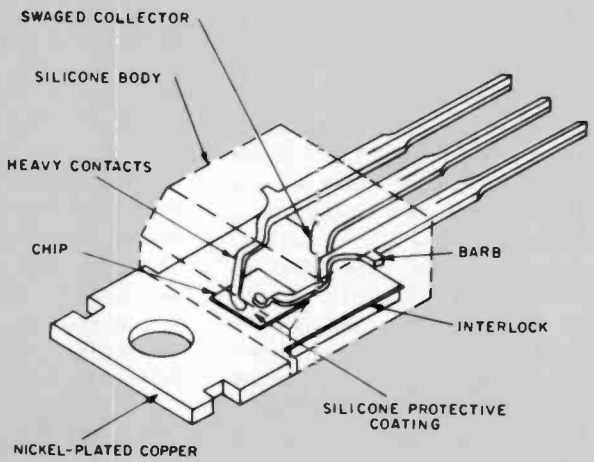

Fig. 6 — Construction of the TO-220 VERSAWATT package.

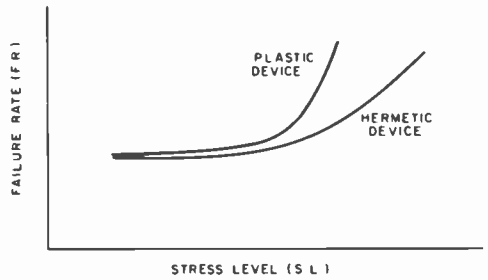

Fig. 7 — Industry experience with comparable power transistors showing that plastic-package performance approaches that for hermetic when stress levels are low.

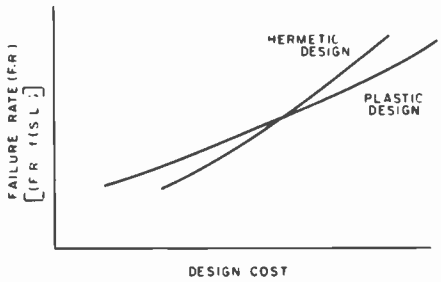

Fig. 8 — Economic situation when plastic-and hermetic-package-design stress levels are adjusted to give comparable failure rates.

be evaluated under actual field conditions.

Where the effort can be justified, the best approach to the solution of factor-2 problems is to have the supplier and the user set up periodic meetings where test results and future plans can be discussed. The user must be willing to provide field failure-rate data and failed devices with proper documentation for analysis, and he must also be willing to segregate and run potentially improved devices. The supplier must be willing to perform failure analysis, develop accelerated tests to produce comparable failure modes, make process changes, set up controls, and provide the improved product for evaluation.

To the extent that not all users can justify this type of effort, they can take advantage of the effort made and results achieved by others. These efforts and results are discussed in detail below.

Package considerations

It was suggested earlier that failure analysis plays a key part in reliability improvement. An examination of typical failure modes for the RCA hermetic package (TO-3) and VERSAWATT plastic package (TO-220) is shown in Figs. 3 and 4 respectively. Fig. 5 shows the construction of a TO-3 package, and Fig. 6 shows the construction of a typical VERSAWATT TO-220 package. Bondwire versions of these types of packages are also available in the industry. It has been empirically determined that thermal-cycling tests are good accelerated tests to use to evaluate product improvements in both plastic and hermetic packages. Defects in workmanship and contact integrity of bonds and chip mounting are investigated by means of this technique.

In the case of plastic packages, sequence testing, which allows moisture to penetrate the package, has been highly successful. An example of a typical sequence test is shown below:

1) Autoclave: T_A = 121°C, 30 psia, 16 hours
2) Temperature cycle: −40°C to 85°C, 10 cycles
3) Autoclave: T_A = 121°C, 30 psia, 16 hours
4) Storage life: 85°C, 168 hours
5) Operating life: P_c = 1.0W, T_c = 85°C
6) Thermal fatigue: P_t = 2.5W, ΔT_c = 50°C $\leqslant T_t$ max. 90°C, 1000 cycles
7) Operating life: P_t = 1.0W, T_c = 85°C

When performing failure analysis, consideration must be given to whether the device is soft soldered or hard soldered. In soft-soldered devices, the metal interfaces between the emitter, base, and collector contacts consist of nickel-lead-tin metals which expand and contract at different rates during thermal cycling. Because of the difference in coefficients of expansion of these materials, an appreciable amount of shearing takes place that causes fatigue failure at the contact point. The longer the stress continues, the more the solder moves to relieve the stress. If the movement continues long enough, the joints rupture, and actual physical displacement of the silicon pellet occurs; this displacement is called pellet "walk". Linear movements of as much as 20 mils have occurred.

In hard-soldered devices, the predominant failure mechanism occurs in the silicon crystal. Since no plastic flow occurs in hard solder, the silicon must take up some of the strain in the system. Cracks in the silicon, generally under the bonding-wire area, are the most common failure mechanism.

Figs. 7 and 8 illustrate, in a qualitative way, a portion of the problem that an equipment manufacturer must face when deciding whether to use a hermetic or a plastic package. Fig. 7 illustrates industry experience and shows that, for comparable power transistors, plastic-package performance approaches that for hermetic when the stress level is low. At higher stress levels, the hermetic package has the advantage. Fig. 8 shows that when plastic and hermetic designs are adjusted in stress level to give comparable failure rates, the plastic-package is more economical at high stress levels. Manufacturers of linear regulated power supplies who use power transistors at high junction-temperature stress levels have recognized this fact for some time. A cost differential for hermetic and plastic packages can be estimated on the basis of the information in Figs. 7 and 8; Table II shows this differential.

On a percentage basis, use of the hermetic-package may boost the device cost by as much as 40 or 50%. If, however, the stress-associated failure rate is relatively high, the additional investment may be justified.

Because the hermetic package appears to provide adequate field-failure rates in the majority of cases, and since the plastic package is a close runner-up with an obvious cost advantage, the major reliability improvement work is being performed on the plastic package. The techniques and screens which have been applied to plastic packages are described below in the section entitled *Screens*.

One notable exception of the generalized statement that hermetic devices exhibit better performance than plastic should be mentioned. The better performance

Table II — Cost trade-off: plastic versus hermetic packages.

Packages	*Cost premium*
TO-5 vs. TO-5 Plastic	+ $.10
TO-66 vs. VERSAWATT	+ $.12
TO-3 vs. VERSAWATT	+ $.14

depends on the controlled environment guaranteed by the hermetic enclosure. Fig. 9 shows an aluminum package with soldered eyelets. When this package is thermal-cycled, the soldered eyelets become non-hermetic and early failure occurs.[1]

One final caution concerning plastic packages should be made to the user. These packages are considerably more vulnerable to mechanical damage than hermetic packages. As a result, special handling procedures must be observed while lead-forming, mounting, soldering, and cleaning. These procedures have been documented by most device suppliers and should be followed closely.[2]

Screens

As mentioned previously, thermal-fatigue testing has been a good test for evaluating power transistors. Fig. 10 shows plots of cycles-to-first-failure as a function of ΔT for a hermetic-and a plastic-packaged transistor; Fig. 11 shows typical thermal-cycling rating curves for the same pellet in both hermetic and plastic packages; and Table III lists recommended test conditions for various types. Table IV shows typical thermal-cycling requirements for various applications, and Figs. 12 and 13 show a typical test circuit and test rack.

It remains to be described how the thermal-fatigue test can be used to assure the user of good product. If this test is run the way reliability tests are usually run, the product is shipped long before a failure shows up. However, real-time controls (RTC), a concept that has been applied to thermal-fatigue testing, but that certainly is not limited to this type of test, can be used to help isolate the failures before a product is shipped. Very simply, RTC is an accelerated reliability test that is performed before product is tested and shipped. It can be used, therefore, to control product, but, most importantly, to provide immediate feedback in the manufacturing line to eliminate the source of failures. The types of test used in RTC are designed to produce information in three days and provide process-control data. Typical examples of thermal-fatigue, real-time-control conditions are shown in Table V.

When a process is under the best possible control, such as that provided by RTC, it is still necessary to perform some simple but effective 100% electrical-parameter

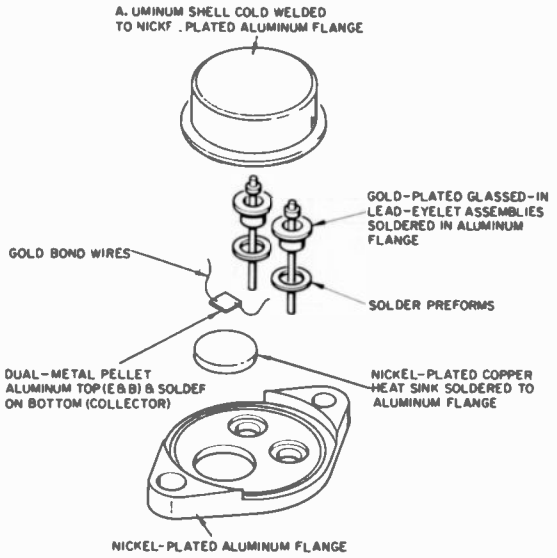

Fig. 9 — Construction of an aluminum package with soldered eyelets.

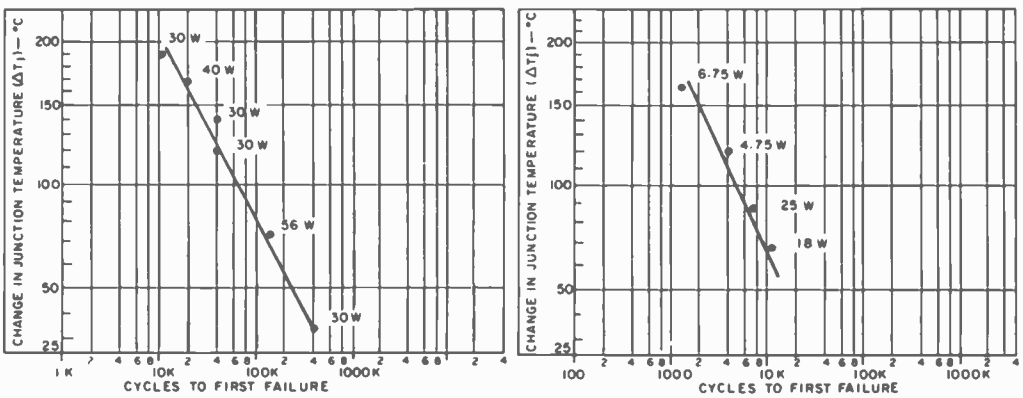

Fig. 10 — Cycles-to-first-failure as a function of a change in junction temperture for a hermetic-and a plastic-packaged transistor: (a) represents the hermetic, TO-3 package and (b) the plastic, TO-220, VERSAWATT package.

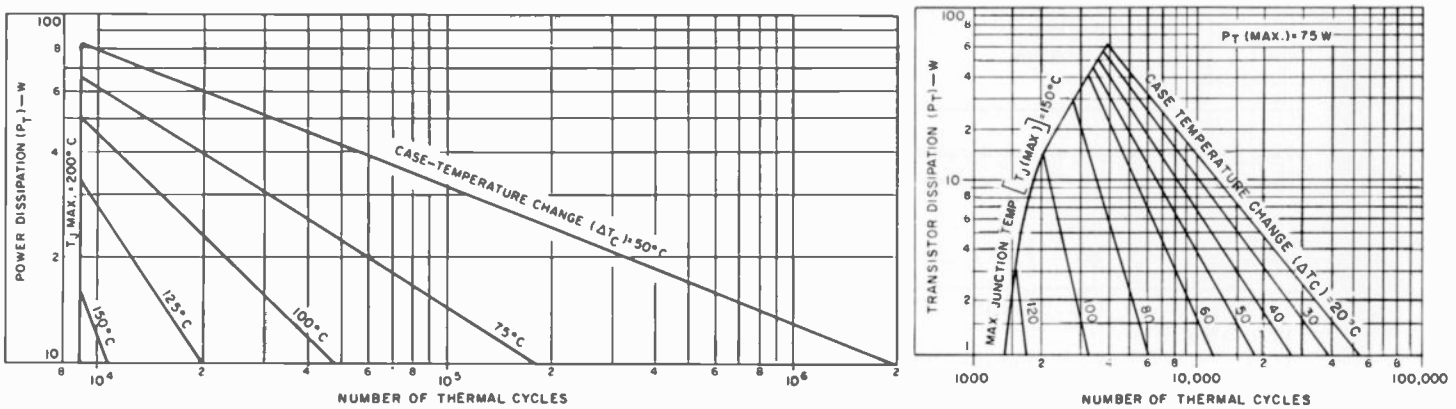

Fig. 11 — Typical thermal-cycling rating curves for the same pellet in both hermetic and plastic packages: (a) relates to the TO-3 hermetic package and (b) to the plastic, TO-220 VERSAWATT package.

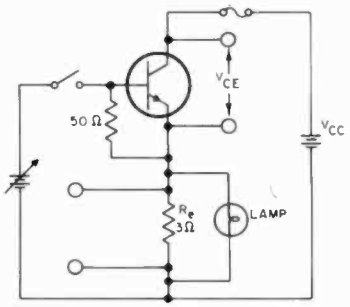

Fig. 12 — Test circuit used in thermal-fatigue testing.

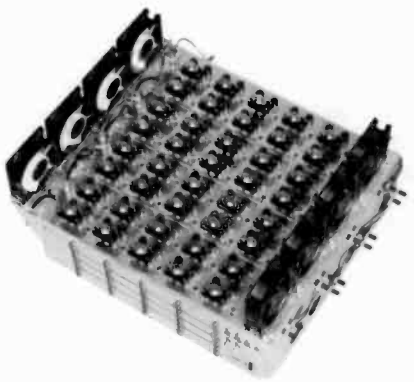

Fig. 13 — Test rack used in thermal-fatigue testing.

Table III — Recommended test conditions for various packages.

Package	*Power* (*W*)	T_A(°C)	ΔT_A(°C)	t_{on}	t_{off}	*Heat sink*
TO-220 VERSAWATT	18	55 to 110	55	3 min.	3 min.	3°C/W
	4.75	35 to 155	120	50s	100s	Free air
TO-3 Hermetic	16	40 to 130	90	50s	100s	Free air
	56	70 to 120	50	15s	25s	6.3°C/W
TO-66 Hermetic	8.5	35 to 155	120	50s	100s	Free air
RCA "TO-5" Plastic	1.5	35 to 135	100	60s	90s	Free air
TO-5 Hermetic	1.5	30 to 115	85	60s	90s	Free air

Table IV — Thermal-cycling requirements for typical applications of power transistors.

Application	*Circuit*	P_T (*W*)	ΔT_c (°C)	*Minimum equipment life required (years)*	*Typical thermal-cycling-rating required (cycles)*
Auto radio	Class A	8	75	5	5,000
Audio output	Class AB	2	45	5	5,000
Power supply	Series reg.	50	65	5	10,000
	Switching reg.	15	65	5	10,000
Hi-fi audio amplifier	Class AB	35	50	5	5,000
Computer power supply	Series reg.	50	65	10	10,000
Computer peripheral equip.	Solenoid driver	5	5	10	1.3×10^5
Television	Vertical out	10	75	5	7,5000
	Audio out.	8	75	5	7,5000
Sonar modulator	Linear ampl.	100	55	10	144×10^3

Table V — Typical examples of real-time-control conditions.

Type	*Power* (*W*)	T_A(°C)	ΔT_c(°C)	*Cycles/Day*	*N*	*Test Duration*	*Ac No.*
TO-220 VERSAWATT	4.75	35 to 155	120	576	40	1700	0
						3000	0
TO-3 Hermetic	56	70 to 120	50	2200	40	4400	0
						6600	1

screens to weed out the few-tenths-of-one-percent failures that could still occur. These parameters are carefully selected on the basis of the reliability analyses of the basic failure mechanisms that can exist in very small percentages: poor contacts, solder voids, and unrelieved stresses in the pellets. Specific screens for these defects are shown below in two categories.

Category 1 — Volume screens

These screens can be performed on automated test equipment at relatively low cost. A 2- to 5-cent premium per device is typical.

V_{EBR} — High-current, emitter-base test to weed out poor contacts or metallization problems. Particularly useful with solder clips. Test can be performed on computer consoles.

Pulse T.R. — Poor chip mounting can be detected with a 50-ms pulse, thermal-resistance (T.R.) test. Because of thermal time constants, the readings cannot be directly correlated to dc thermal resistance.

PRT — Tests units ability to handle power 50-ms test.

Hot-socket test — Detects poor bond-wire connections. Where equipment and temperature are not standard, an additional premium must be paid for this test.

Category 2 — custom screens

These screens require special test facilities and handling procedures. A cost premium twice that of volume screens is typical.

Stability — An effective visual test that to date must be performed on a curve tracer. The operator must make a judgment based on curve-tracer results.

Temperature cycling — This test introduces stresses and strains in the interconnect system and in the silicon die. Criticism to end points similar to those determined in the stability test are often needed. Cost premium is highly dependent on end-point criteria.

Failure-rate predictions

It is very difficult to predict failure rates. If it is known that thermal cycling will produce the dominant failure mode, then thermal-cycling rating charts, such as those shown in Fig. 11, are relevant. If the stress is primarily temperature related, then the curves shown in MIL HDBR 217A and Fig. 14 are relevant. The use of 100% screen tests, such as JAN TX and JAN TXV, may reduce the failure rate by

one order of magnitude.

Experience with several consumer-product manufacturers indicates that unscreened plastic product can incur field-failure rates over a one year period of something in excess of one percent. Once the major failure mechanism is identified, RTC instituted, and screens applied, the failure rate can be reduced to a few tenths of one percent. Hermetic devices are less sensitive to screens and typically exhibit a factor of three to ten times improvement over unscreened plastic. Fig. 15 shows failure rate as a function of junction temperature for various reliability levels of power transistors.

New product trends

The status of semiconductor screens and the data they provide on failure rates will certainly change from that presented in this paper over the next few years. In general, however, change is usually slower than expected.

Glass passivation, both hard and deposited, has been used with success, but has not made large improvements in field-failure rates. Improvement is lacking because contact problems still remain, and the method of application and the quality of the glass have not been perfected. Glass passivation is, however, an active area, and when the process has been sufficiently mastered, failure rates related to surface instability will improve.

Since thermal-cycling causes failure due to expansion and contraction of materials, new advances in plastic will certainly improve this situation. New clip materials and solders may also help.

From a device point of view, lower failure rates will result from:

1) Process controls which permit a greater tailoring of device parameters to a given application. Epitaxial growth appears to afford the greatest chance for optimization, particularly at high voltage.
2) Process controls which deskill the operation. Mechanical handling and assembly are examples.
3) A better understanding of the strengths and limitations of each of the major power-device technologies (i.e., single diffused, epitaxial, multiple diffused). The inherent ruggedness of single-diffused devices, for example, make them ideal for high-energy applications.

New circuit techniques can contribute to overall improvements in reliability. Circuits that utilize redundancy or that essentially derate device requirements will contribute to an improvement in the field performance of a device.

New and better rating systems will contribute to field performance. Thermal cycling is the first data-sheet rating that provides information on long-term performance; other ratings will be developed.

No matter what technical advances may occur, the task of keeping field-failure rates low at a reasonable price to the user will remain. New concepts in rating, screening and real-time controls will play an important part. These new concepts, along with a combined effort on the parts of the component manufacturer and the user to define and eliminate failure modes by means of the latest technology, will bring success to both.

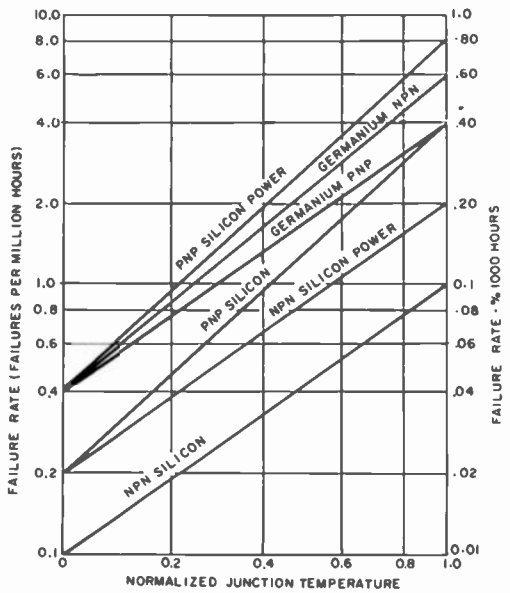

Fig. 14 — Failure rates (in failures per 10^6 hours) for MIL-S-19500 transistors; for power transistors 1 W or greater at ambient temperature of 25°C, multiply values shown by two.

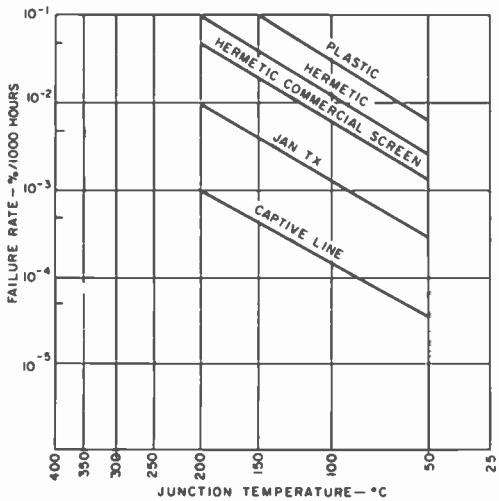

Fig. 15 — Failure rate as a function of junction temperature for various reliability levels of power transistors.

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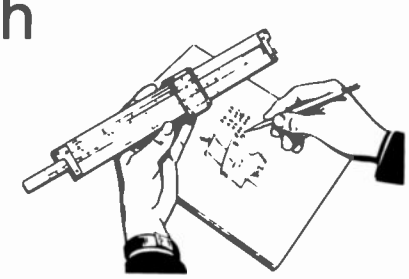

Miniature air flow switch

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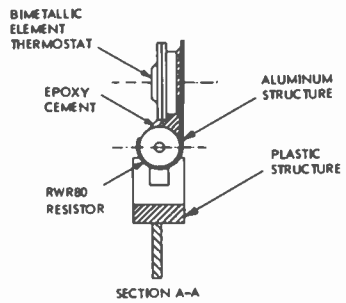
When air is used as a primary coolant for removing heat from electronic components, there is always the possibility of components overheating if there is a stoppage or reduction in the air flow rate. Should this occur — whether it is due to blower failure, dirty air filter, or other forms of air blockage — it is necessary to use a device to provide indication of a malfunction. Currently, there are two common types of devices (among others) to provide this function. One is a vane in the air stream that is attached to a microswitch and the other is a temperature-sensitive variable-resistance-type device within a bridge circuit. Both types require a reasonable packaging volume and their resistance to extreme elements of the military environment is questionable.



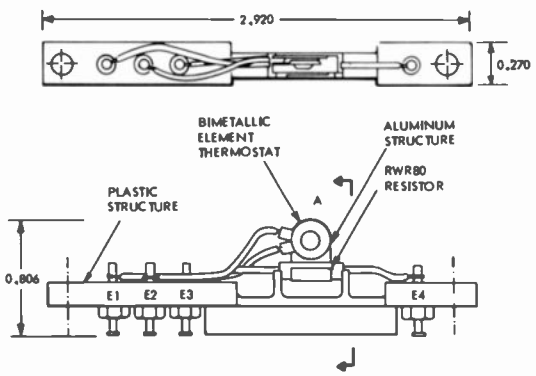


Fig. 1 — Air-flow switch assembly details.

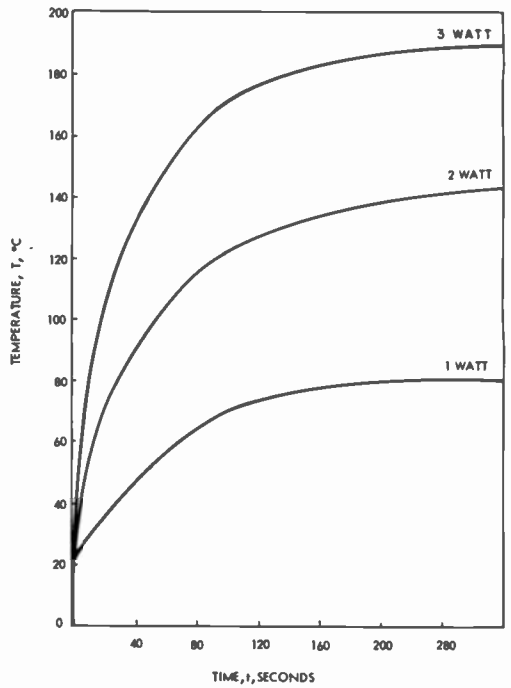


Fig. 2 — Air-flow switch assembly heat-up characteristics in an ambient of 22°C.

A requirement for an air-flow switch that could be mounted between printed-circuit boards, 0.30 in. on center-to-center spacing, and that could withstand the required military environments, motivated the design of a miniature air-flow switch. The switch assembly consisted of a compact thermostatic switch, a small heater element (wirewound resistor), and a lightweight metallic structure as shown on Fig. 1. These three elements are put together as an assembly with an epoxy adhesive and then mounted to a thermally insulated mounting bracket in such a manner that there is a minimum heat loss.

The mode of operation consists of activating the heater element to a given energy level while simultaneously circulating air over the assembly. For every air-flow rate and ambient temperature, there is a given assembly steady-state temperature which is lower than the thermostatic switch-activating temperature. When air flow stops, the air-flow switch assembly begins to increase in temperature quickly

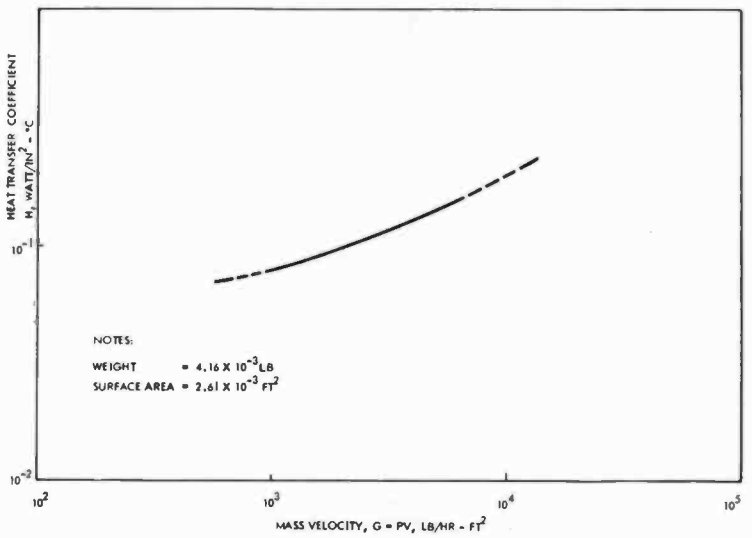


Fig. 3 — Air-flow switch assembly heat transfer film coefficient characteristics in air at 22°C.

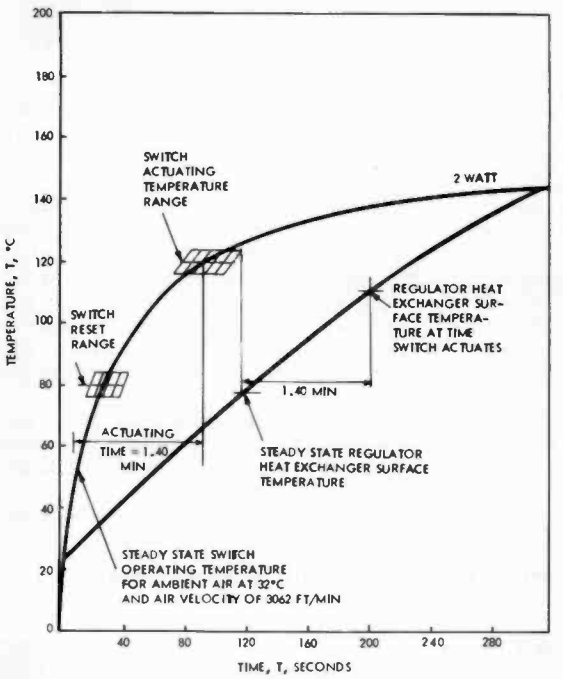


Fig. 4 — Air flow switch assembly time-temperature characteristics for a particular application.

because of its small mass and lack of air flow to remove heat from it. When the air-flow switch assembly temperature reaches the thermostatic switch actuating temperature the switch closes (or opens) to de-energize the heater element and any other electronic circuitry that is being protected. As the air-flow-switch-assembly temperature decreases by transferring heat to its surrounding environment, the thermostatic switch will reset itself at some predetermined lower temperature, and the heater element will be re-energized along with the electronic circuitry and air flow that it controls. The air-flow switch assembly will then return to its original steady-state operating temperature and remain there until there is another air-flow failure and the cycle will repeat itself.

Fig. 2 shows the heat-up characteristics of switch assembly when it is in a free-air ambient of 22°C (71.6°F). Each curve represents the switch assembly temperature change for three levels of power dissipation in the heater element. Fig. 3 provides design data on the heat transfer characteristics of the switch when air is flowing over it. The solid line part of the curve was determined from actual test data while the dashed portions of the curve are extrapolations.

Consider now, by way of example, a typical application of this switch. Assume that a cabinet full of electronic equipment contains a chassis with components that are temperature sensitive. The basic cooling technique is by forced-air convection and the chassis has an inlet air duct readily accessible for mounting an air-flow switch. From a preliminary analysis, it is established that a two-watt resistor in the air-flow switch will be satisfactory for the application. Next, the actuation point of the thermostatic switch is selected to be 120 ± 4°C with a reset temperature of 80 ± 4°C. Air-flow data shows the inlet air temperature to be 32°C and velocity across switch approximately 3060 ft/min. With these data, a heat transfer film coefficient is estimated $h \approx 2.4 \times$ W/in^2°C and a boundary layer temperature differential of 22.2°C. With a bulk air temperature of 32°C the actual surface temperature of the switch assembly should approximate 54.2°C. These data are shown in Fig. 4. As can be seen, the estimated time for switch actuation at 120°C is approximately 1.4 minutes. The next step in the analysis is to assure that there is no part overheating at the moment that the switch is overheating. A review of all components of this chassis shows that there are several power transistors in the regulator section of the power supply, each dissipating approximately 60 W, and mounted to a finned type heat sink which is also forced-air cooled. The time-temperature characteristics of this assembly are estimated and also plotted on Fig. 4. Estimated steady-state operating heat exchanger surface temperature was 76°C and maximum attainable heat exchanger surface temperature was determined to be 156.4°C before transistor junctions become affected. As can be seen, actual heat exchanger surface temperature after 1.4 min. of heating up approximates 111°C and is substantially lower than required. Therefore, the air-flow switch satisfactorily protects the transistor junction from overheating when there is an air-flow failure.

In summary, a small compact and rugged air-flow switch has been designed. It has many applications where minimum circuitry, mechanical simplicity and long term reliability are required. And, it can be constructed from readily available components at reasonable cost.

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Reciprocal switchable multiport transducer using a diode array across each port

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A plan view of a switchable transducer is shown in Fig. 1. The transducer is an enclosed waveguide cavity having broad top and bottom walls spaced by narrow walls. The waveguide cavity has three large openings in the side walls labeled as port 1, port 2 and port 3 in Fig. 1. Fig. 2 is an elevation view of the transducer as viewed from Port. 1. A first array of diodes (11) is coupled between the broad walls of the cavity across port 1. These diodes are connected as shown in Fig. 2 and are coupled to a bias source capable of reverse or forward biasing the array of diodes. An rf bypass of the bias source is provided as represented by the capacitors shown in Fig. 1. This may be accomplished by the proper dimensions of the hole in the cavity to permit passage of the biasing wire. Similarly an array of diodes (15) is connected and properly biased across port 2, and an array of diodes (17) is connected and properly biased across port 3.

In the operation of the transducer, the diode arrays are selectively forward and reverse biased at high speed, and in time sequence, to correspondingly present a short circuit or open circuit across the

Fig. 1 — Switchable transducer, plan view.

FIG. 1

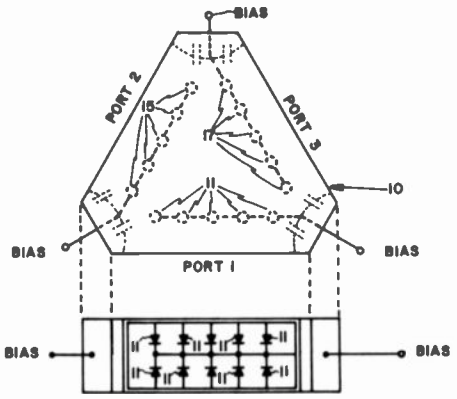

FIG. 2

Fig. 2 — Switchable transducer, elevation view.

respective openings in the side walls at the several ports. When, for example, diode arrays (11) and (15) are reverse biased and diode array (17) is forward biased, r.f. energy at port 1 exits at port 2. When diode arrays (15) and (17) are reverse biased and diode (11) is forward biased, r.f. energy at port 2 exits at port 3. When diode arrays (17) and (11) are reverse biased and diode array (15) is forward biased, r.f. energy at port 3 exits at port 1.

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High voltage dc protection circuit

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Missile and Surface Radar Division
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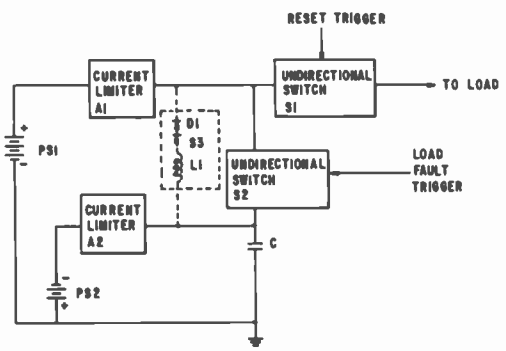

Fig. 1 — High voltage dc protection circuit.

The high voltage protection circuit shown in Fig. 1 provides a means for disconnecting a shorted or faulty load from a dc power source with microsecond speed.

A high voltage dc power supply (PS1) feeds high voltage dc power to a load via current limiting device (A1) and a unidirectional series switch (S1). The current limiting device may be, for example, a saturable reactor. Switch S1 may take the form of a thyratron, ignitron, thyristor stack, spark gap in series with a diode stack, mechanical switch in series with a diode stack, etc.

A second unidirectional switch (S2) is connected in series with capacitor (C) from a point between limiter (A1) and switch (S1) to a point at ground potential. Switch (S2) may take any of the forms mentioned with regard to switch (S1). A second current limiter (A2) and a second dc power supply (PS2) are connected in series between one side of capacitor C and the point at ground potential.

Upon receipt of a load-fault trigger signal, or other turn-off command, switch S2 closes. The closing of switch S2 places an inverse voltage across switch S1, thus allowing switch S1 to recover forward blocking ability. The size of capacitor C and the current limiting characteristic of device A1 are chosen such that the inverse voltage on switch S1 is held long enough to insure that switch S1 does in fact recover its forward blocking ability.

Capacitor C continues to charge through limiter A1 to a voltage higher than the voltage level of PS1, at which point the current through switch S2 will attempt to reverse. This causes switch S2 to enter the forward blocking mode. With switches S1 and S2 in the forward blocking state, capacitor C recharges to the voltage level of the second power supply PS2 via the second current limiter device A2. If desired, switch S2 may now be reset to the *on* condition by the application of a reset trigger signal thereto.

If a high efficiency circuit is desired, the energy stored on capacitor C may be returned to the source via an oscillatory discharge through switch S3, shown in phantom in Fig. 1.

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250 Recording Components and Equipment

disk, drum, tape, film, holographic and other assemblies for audio, image, and data systems.

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325 Checkout, Maintenance, and User Support

automatic test equipment, (ATE), maintenance and repair methods.

DIGITAL BOARD TESTER, A multimode — L. Gemellaro, R. Gariepy, E. Leach, A. Muller (GCASD, Burl) IEEE Seminar, Boston Chapter, Mfg. Techniques, Cambridge, Mass.; 3/20/75

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340 Communications

industrial, military, commercial systems, telephony, telegraphy and telemetry, (excludes: television, and broadcast radio).

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360 Computer Equipment

processors, memories, and peripherals.

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MICROPROCESSOR SYSTEM, A practical, low-cost home/school — J. Weisbecker (Labs,Pr) *Computer Magazine*, Vol. 7, No. 8, pp. 20-31, 8/74

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365 Computer Programming and Applications

languages, software systems, and general applications (excluding: specific programs for scientific use).

SOFTWARE TESTING tools for real-time sensor control systems, Experience with — S.A. Steele (MSRD,Mrstn) 1975 International Conference on Reliable Software, Los Angeles, Calif. 4/21-23/75

SYSTEM RELIABILITY using fault-tolerant software, Improvement in — S.A. Steele, S.R. McCammon (MSRD,Mrstn) Milwaukee Symposium on Automatic Computation and Control, 4/17/75

380 Graphic Arts and Documentation

printing, photography, and typesetting; writing, editing, and publishing; information storage, retrieval, and library science.

PHOTOGRAPHY in industry — C.W. Asbrand (GCASD,Burl) "Career Days," Westwood High School, Westwood, Mass.; 3/13-14/75

Author Index

Subject listed opposite each author's name indicates where complete citation to his paper may be found in the subject index. An author may have more than one paper for each subject category.

Advanced Technology Laboratories

Freiman, F.R., 180
Merkert, R., 130
Merriam, A., 130
Miller, D. III, 240
Pate, E., 130
Solomon, J., 130

Astro-Electronics Division

Binge, D., 310
Hume, C.R., 310
Keigler, J.E., 310
Treadwell, R., 310

Government Communications & Automated Systems Division

Asbrand, C.W., 380
Barton, H.R., 310
Black, O.T., 170
Boehm, P., 340
Cantella, M.J., 210
Dzierzeski, S.J., 215
Garnepy, R., 325
Gemellaro, L., 325
Guzy, J., 340
Leach, E., 325
Shirak, F.R., 325
Willett, J., 175

RCA Limited

Bell, A.B., 310
Brown, A.G., 215
Feher, K., 215
Foldes, P., 225
Hurlburt, D.H., 215
Lo, G., 310
Raab, A., 225
Roux, M., 215

Laboratories

Abeles, B., 205
Abrahams, M.S., 160, 205
Alphonse, G.A., 240
Ametani, K., 160, 205, 240
Appert, J.R., 205, 240
Ban, V.S., 205
Bell, A.E., 205
Berkeyheiser, J.E., 205
Blanc, J., 205
Bortfeld, D.P., 240
Branin, P.B., 105
Buiocchi, C.J., 160, 205
Burke, W.J. 205,240
Caplin, A.D., 205
Carlson, D.E., 205
Channin, D.J., 160, 240
Chiang, Y.S., 210
Chin, T.N., 210
Clorfeine, A.S., 210
Cohen, R.W., 210, 245
Conradi, J. F., 205
Cosentino, L.S., 245
Coutts, M.D., 210
Crandall, R.S., 205
Crossley, P.A., 210
Cullen, G.W., 205
Curtice, W.R., 215
D'Aiello, R.V., 210
Denlinger, E.J., 210, 215
deWolf, D.A., 225
Dingwall, A.G.F., 210
Dougherty, F.C., 205
Douglas, E.C., 210
Dresner, J., 205
Endriz, J.G., 125
Engelbrecht, R.S., 250
Enstrom, R.E., 205, 240
Escher, J.S., 220, 240
Ettenberg, M., 205
Etzold, K.F., 255
Faughnan, B.W., 205
Fehlmann, R., 160
Fisher, D.G., 210, 240
Fonger, W.H., 105
Fujita, H., 160, 205
Gannon, J.J., 205
Gosh, A.K., 205
Goldsmith, N., 205
Goldstein, B., 205
Goodman, A.M., 160, 205
Goodman, L.A., 245
Gorog, I., 245
Gossenberger, H.F., 240
Gurney, R., 215
Ham, W.E., 210
Hammer, J.M., 240
Hanak, J.J., 210
Hang, K.W., 205
Kerzog, G.B., 360
Ho, P.T., 215
Hoffman, D.M., 150, 210
Huang, H.C., 210, 215
Iguchi, Y., 160
Inoue, M., 125
Jolly, S.T., 210
Kaplan, G.S., 320
Kaplan, M., 205
Kiess, H., 205
Kleinknecht, H.P., 240
Knox, J.D., 215
Kokkas, A.G., 205, 210
Kovac, M.G., 215
Kressel, H., 205, 210, 240
Ladany, I., 205, 240
Lampert, M.A., 240
Levin, B.J., 210
Levine, A.W., 205
Levine, J.D., 210
Ligenza, J.R., 205
Lockwood, H.F., 240
McFarlane, S.H., 205, 210
McIntyre, R.J., 240
Martinelli, R.U., 205
Merz, W.J., 125
Meyerhofer, D., 205
Mezrich, R.S., 255
Neil, C.C., 240
Nelson, H., 105
Nuese, C.J., 205, 240
Okada, Y., 205
Olmstead, J.A., 160
Olsen, G.H., 240
Olson, H.F., 255
Onyshkevych, L.S., 215
Osaska, S., 210
Pankove, J.I., 205, 240
Phillips, W., 240
Pike, W.S., 215
Poliniak, E.S., 205
Powell, R.J., 205
Priestley, E.B., 240
Putzrath, F., 215
Redfield, D., 205, 220
Reynolds, J.F., 210
Roach, W.R., 240
Robinson, P.H., 205, 210
Ronen, R.S., 160
Rose, A., 240
Rosen, A., 210
Rosen, J., 215
Sandercock, J.R., 205
Schneider, M.S., 205
Shahbender, R., 215
Shallcross, F.V., 215
Sheng, P., 125, 205
Staebler, D.L., 240, 360
Steigmeier, E.F., 125
Sterzer, F., 320
Stevenson, D.M., 210
Stewart, W.C., 245
Stockdale, G.F., 205
Sunshine, R.A., 210
Sussman, A., 105, 205
Szostak, D., 205
Takahashi, T., 205
Toda, M., 210
Tomkiel, S., 215
Turski, Z., 215
Upadhyayula, L.C., 210
Vilkomerson, D.H.R., 255
Vossen, J.L., 170
Wang, C.C., 205
Webb, P.P., 240
Weimer, P.K., 215
Weisbecker, J., 360
Wen, C.P., 210
Widmer, A.E., 160, 240
Williams, R., 125, 205
Wittke, J., 240
Wojtowicz, P.J., 105, 125
Woods, M.H., 125, 205
Yamada, O., 205

Missile and Surface Radar Division

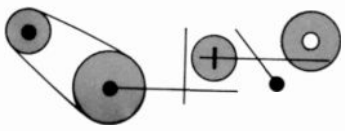
Adams, F.G., 180
Buckley, M.W., 180
Gross, S.D., 320
Hurley, J.W., 315
Liston, J., 320
McCammon, S.R., 365
Martinson, L.W., 320
Nessmith, J.T., 225
Palmer, F., 320
Patton, W.T., 225
Sherman, S.M., 225, 320
Sparks, G.M., 320
Staiman, D., 320
Steele, S.A., 365
Stevens, G.H., 320
Urkowitz, H., 320
Weinstock, W.W., 320

Solid State Division

Giovachino, D., 210
Jenny, H. K., 210
Rodgers, R., 210

Patents Granted

to RCA Engineers



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Method of bonding metals together — A.F. Arnold, A.Z. Miller (SSTC,Smvl) U.S. Pat. 3875652, April 8, 1975

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Method of electroless plating — A.F. Arnold (SSTC,Smvl) U.S. Pat. 3877981, April 15, 1975

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Electron discharge device including an electron emissive electrode having an undulating cross-sectional contour — R.D. Faulkner (EC,Lanc) U.S. Pat. 3875441 April 1, 1975

Cathode ray tube with radiation-emitting index strip-like areas — R.D. Thompson (EC,Lanc) U.S. Pat. 3875450, April 1, 1975

Apertured-mask cathode-ray tube having half-tone array of heat-absorbing areas on target surface — R.H. Godfrey (EC,Lanc) U.S. Pat. 3878427, April 15, 1975

Cathode ray tube having shadow mask and screen with tailored heat transfer properties — H.E. Kuzminiski, F.M. Sohn (EC, Lanc) U.S. Pat. 3878428, April 15, 1975

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Commercial Communications Systems Division

R-F switching circuit — M.E. Adams, R. Feryszka (CCSD,Cam) U.S. Pat. 3872325, March 18, 1975

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Advanced Technology Laboratories

Delta modulator utilizing a duty cycle circuit — E.P. McGrogan, Jr. (ATL,Cam) U.S. Pat. 3879663, April 22, 1975

Energy peak/time averaging seismic intrusion detector — G.J. Dusheck, Jr. (ATL,Cam) U.S. Pat. 3879720, April 22, 1975

Missile and Surface Radar Divison

Distributed transmission line filter — B. Golant, N.R. Landry (MSRD,Mrstn) U.S. Pat. 3870690, APril 22, 1975

Range tracking circuit — A.D. Arsem (MSRD,Mrstn) U.S. Pat. 3879740, April 22, 1975

Amplifier blanking circuit — A.D. Arsem (MSRD,Mrstn) U.S. Pat. 3882407, May 6, 1975

Doppler correlation radar exhibiting reduced time side lobes — T.V. Bolger (MSRD,Mrstn) U.S. Pat. 3882493, May 6, 1975

Doppler correlation radar providing combined target detection and ranging — T.V. Bolger (MSRD,Mrstn) U.S. Pat. 3882494, May 6, 1975

Doppler correlation radar providing coarse-range detection resolution — T.V. Bolger (MSRD,Mrstn) U.S. Pat. 3882495, May 6, 1975

Special Contract Inventor

Circuit for applying data signals across a micorphone input circuit — C. A. Rypinski, J.E. Pera (Special Contract Inv.) U.S. Pat. 3870958, March 11, 1975.

Engineering News and Highlights

Dr. Hillier Honored by I.R.I.

James Hillier, Executive Vice President, Research and Engineering, recently received the 1975 Industrial Research Institute Medal at the Institute's annual meeting in White Sulphur Springs, W.Va.

The I.R.I. Medal was established in 1945 and is given annually "to recognize and honor outstanding accomplishment in leadership or management of industrial research which contributes broadly to the development of industry and to the benefit of society."

The Medal was given at a banquet honoring Dr. Hillier. Toastmaster was **N. Bruce Hannay,** currently President of I.R.I., and Vice President, Research and Patents, of Bell Laboratories. **Anthony L. Conrad,** President and Chief Operating Officer of RCA Corporation, introduced Dr. Hillier; and **Herbert I. Fusfeld,** immediate past president of I.R.I., and Director of Research, Kennecott Copper Corporation, made the medal presentation. Prior to the banquet, Dr. Hillier had delivered a short address entitled "Industrial Research Management — The Changing Challenge."

Dr. Hillier studied at the University of Toronto, where he received the BA in Mathematics and Physics in 1937, MA in Physics in 1938, and PhD in Physics in 1941. Between 1937 and 1940, while Dr. Hillier was a research assistant at the University of Toronto, he and a colleague, Albert Prebus, designed and built the first successful high-resolution electron microscope in the Western Hemisphere. Following this achievement, Dr. Hillier joined RCA in 1940 as a research physicist at Camden, N.J. Working with a group under the direction of Dr. V.K. Zworykin, Dr. Hillier designed the first commercial electron microscope to be made available in the United States.

In 1955, he was appointed Chief Engineer, RCA Industrial Electronic Products. In 1957, he went to RCA Laboratories as General Manager and a year later was elected Vice President. He was named Vice President, RCA Research and Engineering, in 1968, and in January 1969 he was appointed to his present position.

Dr. Hillier was president of the Industrial Research Institute in 1963. He has written more than 100 technical papers and has been issued 40 U.S. patents. He is a Fellow of the American Physical Society, the AAAS, the IEEE, and is an Eminent Member of Eta Kappa Nu. He is a past president of the Electron Microscope Society of America, and a member of Sigma Xi.

Broadcast Systems Engineering Conference

The third annual Broadcast Systems Engineering Conference was held on May 12, 1975 at the Cherry Hill Inn. It was attended by more than 300 people consisting of the technical and product management staff of Broadcast Systems in Camden and Gibbsboro, and included Manufacturing management personnel and guests from Corporate Staff, G&CS Staff, RCA Laboratories, and Meadow Lands.

The theme of the conference, IDEAS, was introduced by **A.D. Luther,** Chief Engineer, Broadcast Systems. The theme is an acronym for Invention, Development, Engineering, Action, and Success — all of which were stressed as being necessary for each step of a new program.

The speakers at the conference were **N. VanderDussen,** Broadcast Systems, Division Vice President, who reviewed the Broadcast Systems business picture; **A.F. Inglis,** Division Vice President and General Manager, who emphasized the importance of Product Design; and **B.F. Melchionni,** Manager, CRAE Shop and Systems Engineering, who described a typical new Broadcast station, highlighted with photographs of the recently installed WREG station. Mr. Luther then presented a paper on how to develop goals for new product development, and this was followed by **W.S. Sepich,** Manager, Engineering Technical Support, making a presentation on Advances in Design and Drafting Practices.

After the group discussions, **H.H. Klerx,** Manager, Control Equipment Engineering and Product Management, presented a review of the NAB Convention which was recently held in Las Vegas. This was followed by reports from each of the discussion group chairmen.

After cocktails and dinner, two awards were presented: Seven individuals received a Team Achievement Award for outstanding contributions to the WREG program. Sixty-nine individuals received Team Achievement Awards for outstanding contributions to the TR-600 program. In addition, recognition was also given to individuals for the following accomplishments:

Attendance at University Courses
Attendance at RCA After-Hours Courses
Attendance at Training Seminars
Publishing and Presenting Papers
Issuing Patent Disclosures
Patents Awarded

Recipients of team achievement award for outstanding contributions to the TR-600 program.

N. VanderDussen, VP, Broadcast Systems, presenting team achievement awards for outstanding contributions to the WREG program.

F. William Storck, who worked for Eldridge Johnson and the Victor Talking Machine Co. in the 1920's, examines one of the 900 slides used by Ed Hutto (center) in his history of the Victor company. Mr. Storck, president of the N.J. Wire Stitching Machine Co., a firm founded by Mr. Johnson, was invited to the presentation by RCA's Community Relations activity. He was accompanied to the presentation by Elmer McDaniel, Administrator Urban Affairs.

ATL engineer presents history of Victory Talking Machine Co.

Ed Hutto of the Advanced Technology Laboratories in Camden has done some extensive research to put together a highly interesting story of Eldridge Johnson and the Victor Talking Machine Co., the company purchased by the Radio Corporation of America in 1929 in order to gain a manufacturing facility in Camden.

Mr. Hutto's research is now on 900 slides, pared down from 1,700 slides which he shows with the help of three projectors, three screens and a sound track.

The hour-long show was recently presented every lunch hour for two weeks in Camden.

Ed narrates the tale of Mr. Johnson's successes. From his first repair shop, to his wire stitching machine company, to his interest in the early gramophone devices, to the founding and growth of the Victor Talking Machine Co. Included on the sound track are recordings of the great Victor artists of the 1920's. Hutto's story details the superseding of the record business in Camden as radio improved, the sale of Victor to a New York group before it was purchased by Radio Corporation of America and concludes with accounts of Mr. Johnson's wealth and his philanthropic interests.

Williams elected to Brazillian Academy of Sciences

Dr. Richard Williams, RCA Laboratories, Princeton, N.J. was recently elected a Corresponding Member of the Brazillian Academy of Sciences.

Dr. Williams was graduated from Miami University (Oxford, Ohio) in 1950 and received the PhD in Physical Chemistry from Harvard University in 1954. He joined RCA Laboratories in 1958 and has since received two RCA Laboratories Achievement Awards, a David Sarnoff Award in Science, and has been named a Fellow of the Laboratories. In 1969, he was a Fulbright Lecturer in the Escola de Engenharia, Sao Carlos, Brazil. Dr. Williams is a member of Phi Beta Kappa and a Fellow of the American Physical Society.

Dr. Williams has performed outstanding research on the electrical properties of insulators, internal photoemission, solid surfaces, high electric fields in solids, liquid crystals and electrons on the surface of liquid helium.

Mueller receives Notre Dame Engineering Award

Dr. Charles W. Mueller, a Fellow of RCA Laboratories, Princeton, N.J., has been honored by the College of Engineering of the University of Notre Dame. Dr. Mueller received the 1975 Engineering Honor Award

— For his contributions to the electron device field from vacuum tubes to silicon-on-sapphire integrated circuits.

— For his pioneering work in the development of the alloy junction transistor which helped further the solid state revolution in electronics.

— For his development of silicon vidicons and silicon storage vidicons.

— For his overall technical excellence as recognized by his receipt of the J.J. Ebers Award.

— For his continuing outstanding contributions to RCA which has twice accorded him its highest technical honor, the David Sarnoff Award.

Dr. Mueller received the BSc (magna cum laude) from the University of Notre Dame in 1934 and the MS from MIT in 1936. He worked for the Raytheon Corporation for two years before returning to MIT for his doctorate.

All of Dr. Mueller's significant research was done at RCA Laboratories, Princeton, N.J., where he has worked since 1942.

Dr. Mueller is a Fellow of the IEEE, and a member of the American Physical Society and Sigma Xi. He has three times received RCA's highest technical honor, the David Sarnoff Award, as well as three RCA Laboratories Achievement Awards. In 1972, he received the J.J. Ebers Award from the IEEE Group on Electron Devices. He has published 17 technical papers and holds 18 U.S. Patents.

GCASD — Camden Authors' and Inventors' Reception

Government Communications and Automated Systems Division, Camden, honored 71 members of its technical staff at a special Authors' and Inventors' Reception on May 8, 1975. Each of the men honored had, in 1974, either authored a paper, prepared a patent disclosure, or had a patent issued in his name.

The reception was hosted by **Don Parker,** Chief Engineer. The guests included **J.M. Osborne,** Division Vice President and General Manager, GCASD; **Dr. H.J. Woll,** Division Vice President, G&CS Government Engineering; **Dr. W.J. Underwood,** Manager, Engineering Professional Programs; **W.O. Hadlock,** Editor, *RCA Engineer*; and **J.S. Tripoli,** the 1974 Camden Resident Patent Attorney.

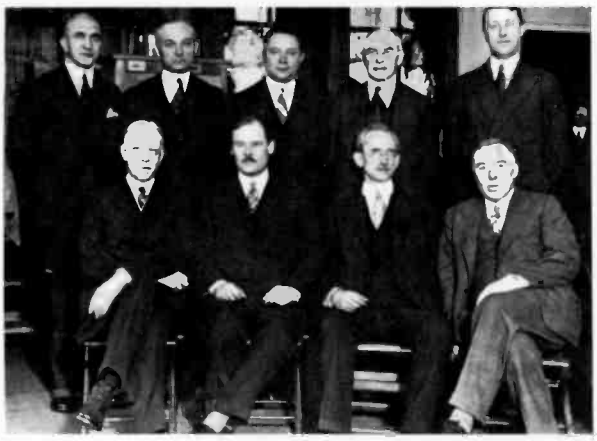
Special recognition was given to **E.J. Nossen** who authored eight papers and six patent disclosures, **D. Hampel** for his five papers and two patent disclosures, and **E. Starner** for his four papers and four patent disclosures. Also honored was **A. Liquori,** who was given a desk accessory in recognition of the issuance of his twentieth patent.

Dr. H.J. Woll, Division Vice President G&CS Government Engineering, congratulating Eugene Starner for his four papers and four patent disclosures.

Division Vice President and General Manager, James M. Osborne with E.J. Nossen who generated eight papers and six patent disclosures.

Donald J. Parker, Chief Engineer, GCASD, distributing round tuit buttons to J. Yanosov and E. Lachocki in line with GCASD-C philosophy, "When something needs doing, we get a round tuit immediately".

Division Vice President and General Manager, James M. Osborne, presenting a desk accessory to Anthony Liquori in recognition of the issuance of his twentieth patent. J. S. Tripoli, 1974 Camden Resident Patent Attorney assists with the presentation.



Dr. Alexanderson (front row, second from left) at the first demonstration of television broadcasting, by RCA and the General Electric Company, at Schenectady, N.Y., Left to right, standing: J.L. Ray, Gen. Sales Manager, RCA; E.P. Edwards, Mgr. Radio Division, General Electric Co.; David Sarnoff, VP and GM, RCA; E.W. Rice, Jr., Hon. Chairman of Board, G.E. Co.; E.Y. Allen, Vice-pres., G.E. Co. Seated: H.P. Davis, Vice Pres., Westinghouse Co.; E.F.W. Alexanderson, chief consulting engineer RCA, whose apparatus is being tested; D. McFarlan Moore, G.E. engineer and inventor of neon lamp used for television; S.M. Kintner, Manager, Research Div., Westinghouse Company. (Photo in *Wireless Age*, 1928).

Dr. Ernst Alexanderson dies at 97

Dr. Ernst F.W. Alexanderson, the engineer whose high-frequency alternator made possible the first voice radio broadcast in 1906, and who later contributed to the development of television technology, died on May 14, at the age of 97 at his home in Schenectady, N.Y.

Dr. Alexanderson, a native of Sweden, held 322 patents, most of them granted during a 46-year career with the General Electric Company that began in 1902.

In the early days of television development, Dr. Alexanderson was chief consulting engineer to RCA. After his retirement from G.E. in 1948, Dr. Alexanderson resumed this earlier association in 1952, as a consultant in developing the basic color television system used in this country.

ATL Authors' and Inventors' Reception

Advanced Technology Laboratories of G&CS recently held a reception at the Cherry Hill Inn honoring 32 members of its technical staff who have presented or published papers or who have received patents over the past year. After cocktails and dinner, **Paul Wright,** Director of ATL and host for the reception, congratulated the group for their professional performance and then introduced **Dr. Harry Woll**, Div. V.P., Government Engineering who added his congratulations. The evening culminated with a presentation on the Electro-Optics and Devices business by **Dr. Ralph Simon,** Div. V.P., Electro-Optics and Devices, Solid State Division, Somerville, N.J.

Licensed engineers

When you receive a professional license, send your name, PE number (and state in which registered), RCA division, location, and telephone number to: *RCA Engineer*, Bldg. 204-2, RCA, Cherry Hill, N.J. New listings (and corrections or changes to previous listings) will be published in each issue.

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J.P. Defandorf, Needham, Mass.; MA-17772, Massachusetts.

Distributor and Special Products Division

J.J. Kelly, Rocky River, Ohio; OH-029742E, Ohio.

Patent Operations

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Missile and Surface Radar Division

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Astro-Electronics Division

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H.L. Schwartzberg, Princeton, N.J.; PA-4532E, Pennsylvania; NJ-19978, New Jersey.

Advanced Technology Laboratories

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Government Communications and Automated Systems Division

D.J. Parker, Camden, N.J.; NJ-21110, New Jersey.

J.A. Dodd, Jr., Camden, N.J.; NJ-12988, New Jersey.

Staff

E.A. Roloff, Cherry Hill, N.J.; E-10262, Missouri; NJ-17760, New Jersey.

Consumer Electronics

H.E. Chaney, Bloomington, Ind.; IN-15932, Indiana.

MSRD engineers participate in International Radar Conference

Engineers from the Missile & Surface Radar Division, Moorestown, N.J., presented five papers covering significant areas of radar systems and technology at the recent International Radar Conference sponsored by the Institute of Electrical and Electronics Engineers, (IEEE), in Arlington, Va.

The papers were:
— "Directional Velocity Sorting MTI with Staggered Pulse Spacing", by **Dr. H. Urkowitz.**
— "Phase Variations in a Monopulse Antenna" by **Dr. J.T. Nessmith** and **S.M. Sherman.**
— "A Programmable Digital Processor for Airborne Radar" by **L.W. Martinson.**
— "Automatic Detection, Acquisition and Tracking in Clutter Using a Coherent Tracking Radar" by **Dr. G.M. Sparks** and **G.H. Stevens.**
— "Wideband and Solid-State Transceiver Module Evaluation for Radar Applications" by **S.D. Grodd, J. Liston, F.I. Palmer, Dr. D. Staiman.**

Bryce D. Inman, Manager, Combat Systems Development, in MSRD's AEGIS Department was Chairman of Session III, "Moving Target Indication (MTI)".

Three RCA engineers also served as guest lecturers at two intensive three-day state-of-the-art courses in radar technology held in conjunction with the IEEE Conference. They are **Dr. Willard T. Patton,** ("Array Feeds" and "Phase Shifters and the AEGIS Array"); **Dr. Walter Weinstock** ("Computer Control of Multifunction Radar"); and **Dr. Samuel Sherman** ("Complex Angle Monopulse" and "Practical Application of Complex Angle Monopulse").

Dr. S.M. Sherman — "Pulse Variations in a Monopulse Antenna."

Dr. H. Urkowitz — "Directional Velocity Sorting MTI with Staggered Pulse Spacing."

Dr. G.M. Sparks — "Automatic Detection, Acquisition, and Tracking in Clutter Using a Coherent Tracking Radar."

Staff Announcements

Picture Tube Division

Joseph H. Colgrove, Division Vice President and General Manager, Picture Tube Division has announced the organization as follows: **Wellesley J. Dodds,** Manager, Quality and Reliability Assurance; **D. Joseph Donahue,** Division Vice President, Engineering; **Robert F. Dunn,** Director, Domestic Market Planning; **Arnold M. Durham,** Manager, News and Information; **William G. Hartzell,** Division Vice President, International; **Lawrence A. Kameen,** Division Vice President, Industrial Relations; **Clifford H. Lane,** Division Vice President, Technical Planning; **Robert B. Means,** Division Vice President, Domestic Sales; **Stanley N. Roseberry,** Division Vice President, Finance; and **Charles W. Thierfelder,** Division Vice President, Manufacturing.

Solid State Division

Ralph E. Simon, Division Vice President, Electro-Optics & Devices has announced the following organizations as follows:

Electro-Optics & Equipment Operations: **Harold R. Krall,** Manager, Electro-Optics & Equipment Operations; **David E. Bowser,** Leader, Engineering — Subassemblies & Equipment; **Joseph T. Gote,** Leader, Engineering — Video Equipment; **Victor C. Hauk,** Manager, Market Planning — Systems & Equipment; **Harold R. Krall,** Acting Manager, Manufacturing — Systems & Equipment; and **Philip H. Vokrot,** Administrator, Operations Control — Systems & Equipment.

Charge-Couple Device Operations: **Robert L. Rodgers,** Manager, Charge Coupled Device Operations: **William N. Henry.** Manager, Manufacturing — Charge Coupled Devices; **Roy A. Minet,** Manager, Marketing Planning — Charge Coupled Devices; and **Robert L. Rodgers,** Acting Manager, Engineering — Charge Coupled Devices.

Quality & Reliability Assurance — EOD: **William E. Bradley,** Manager, Quality & Reliability Assurance — EOD and Acting Leader, Quality & Reliability Assurance Systems Engineering; **Joseph J. Carroll,** Manager, Quality & Reliability Assurance; and **Junior A. Molzahn,** Administrator, Quality & Reliability Assurance Planning & Cost Administration.

Lancaster Operations Support: **C. Price Smith,** Manager, Lancaster Operations Support; **William F. Cronin,** Manager, Management Information Systems; **Gust S. Diamantoni,** Manager, Industrial Engineering; **Alan D. Greer,** Manager, Manufacturing — Parts & Works; **Arthur W. Hoeck,** Manager, Finanacial Operations — Lancaster; **Robert C. Pontz,** Manager, Materials; and **Charles A. Smith,** Manager, Plant Engineering.

Power Tube Operations: **Charles W. Bizal,** Director, Power Tube Operations; **Ronald M. Bowes,** Manager, Market Planning — Power Tubes; **Leroy Caprarola,** Manager, Thermoelectric Operations; **John G. Kindbom,** Manager, Manufacturing — Triodes & Tetrodes; **William S. Lynch,** Manager, Manufacturing — External Anodes; **Herbert W. Sawyer,** Manager, Manufacturing — Internal Anodes & Pencil Tubes; **Joseph D. Schmitt,** Manager, Operations Control — Power Tubes; and **Thomas E. Yingst,** Manager, Engineering — Power Tubes.

Electro-Optics Operations: **Thomas T. Lewis,** Director, Electro-Optics Operations; **Thaddeus J. Brabowski,** Manager, Market Planning — Displays & Emitters; **Clarence H. Groach,** Manager, Operations Control — Electro-Optics; **Leonard W. Grove,** Manager, Manufacturing — Electro-Optics; **N. Richard Hangen,** Manager, Market Development — Research & Development; **Fred A. Helvy,** Manager, Applications Engineering — Electro-Optics; **Edward F. McDonough,** Manager, Market Planning — Photodetectors; **Ronald G. Powers,** Manager, Solid State Detectors — Canada; **Carl L. Rintz,** Manager, Market Planning — Imaging Devices; and **Eugene D. Savage,** Manager, Engineering — Electro-Optics.

Norman C. Turner, Director, COS/MOS Products has announced the organization as follows: **David S. Jacobson,** Manager, Process Engineering & Cost Reduction — COS/MOS IC; **Martin A. Blumenfeld,** Leader, Process Technology, **Walter F. Lawrence,** Project Leader, Packaging Technology; **Gordon S. Putnam,** Acting Administrator, Cost Reduction Planning; **Russell D. Knapp,** Administrator, Product Planning — COS/MOS IC; **George A. Riley,** Manager, Market Planning — COS/MOS IC; **Thomas C. Kelly,** Administrator, Product Administration; **Julius Litus, Jr.,** Administrator, Market Planning; **Henry L. Pujol,** Administrator, Market Planning; **Gary J. Summers,** Administrator, Market Planning; **Alexander W. Young,** Manager, Design Engineering — COS/MOS IC; **Edward C. Crossley,** Leader, Test Technology; **Richard P. Fillmore,** Leader, Custom Circuit Design; **Robert C. Heuner,** Leader, Standard Circuit Design; and **Alexander W. Young,** Acting Leader, Applications Engineering.

Richard L. Sanquini, Director, Bipolar IC Operations has announced the appointment of **Seymoure Reich** as Manager, Market Planning — Consumer Linear IC.

Ben A. Jacoby. Division Vice President, Solid State Marketing, has announced the appointment of **Robert T. Jeffery** as Manager, Marketing Services.

Anthony J. Froio, Manager, Advertising and Sales Promotion has announced the organization as follows: **Dale W. Ludlum,** Administrator, Advertising: **Eleanor M. McElwee,** Manager, Engineering Publications; **Gerald E. Ryan,** Administrator, Sales Promotion; and **Arthur P. Sweet, Jr.,** Leader, Engineering Publications — EOD.

Mobile Communications Systems

Samuel P. Vrankovich, Plant Manager, Meadow Lands, Pa., has announced the appointment of **Dale O. Erickson** as Manager, Manufacturing Engineering.

Donald W. Goodwin, Manager, Federal Government Area Sales has announced the appointment of **Charles W. Herrin** as Manager, Government Field Executive Account Sales.

Palm Beach Division

James F. Callahan, Manager, Planning and Product Development has announced the appointments of **George W. Reel, Jr.,** and **Robert S. Singleton** as Staff Product Planners for the Dataway line of electronic management systems for hotels, motels and hospitals. **George A. Earle,** Director, Marketing has announced the appointment of **Karen L. Tenne** as Product Planner for RCA's Dataway line.

Consumer Electronics

Jay J. Brandinger, Division Vice President, Television Engineering, has appointed **Robert J. Lewis** Chief International Engineer.

Shirak appointed to National Advisory post

F. Ralph Shirak, Manager Automated Test Systems Programs, Government Communications and Automated Systems Division, Burlington, Mass., has been appointed an Associate Member of the Defense Science Board. Mr. Shirak will serve on the Science Board's Task Force on Electronic Test Equipment.

The Board advises the Secretary of Defense and the Director of Defense Research and Engineering on research and engineering and provides long-range guidance in these areas to the Department of Defense.

Mr. Shirak has been involved in the automatic test equipment area for more than 10 years and currently is responsible for GCASD — Burlington's automatic test equipment line.

Mr. Shirak received the BS in 1949 from Drexel Institute of Technology. He joined RCA in 1955 as Administrator of Production Engineering Programming. Previously he had been Director of Engineering, Dubrow Electronic Industries, Burlington, N.J., and a research physicist with the Rohm & Haas Company, Philadelphia.

Mr. Shirak is a member of the IEEE. He holds several patents on instrumentation for industrial processes.

Bianculli

Engstrom

Skavicus

Haynes

Bianculli, Engstrom, Skavicus named Ed Reps

Robert M. Cohen, Director of Quality and Reliability Assurance at the Solid State Division, and a member of the *RCA Engineer* Advisory Board has appointed **Anthony J. Bianculli** Editorial Representative for Integrated Circuits and Special Devices at Solid State Division in Somerville, N.J.

Dr. Ralph E. Simon, Division V.P., Electro-Optics and Devices, Solid State Division, has appointed **Ralph E. Engstrom** Editorial Representative for Electro-Optics and Devices at Solid State Division in Lancaster, Pa.

E.M. Stockton, Chief Engineer, Government Communications and Automated Systems Division, Burlington Operations, has appointed **Albert J. Skavicus** Editorial Representative for GCASD in Burlington, Mass.

Editorial Representatives are responsible for planning and processing articles for the *RCA Engineer* and for working with the Technical Publications Administrators in their Divisions to support the corporate-wide technical papers and reports program. A complete listing of Technical Publications Administrators and Editorial Representatives is provided on the inside back cover of each *RCA Engineer* issue.

Anthony J. Bianculli received the BSME from the Polytechnic Institute of Brooklyn in 1949. He joined RCA in 1952 as a design engineer in Microwave Tube Operations at Harrison, N.J. Over the next ten years, he had a succession of responsibilities at that location including Manager, Development Shop and Equipment Design, and Manager, Nuvistor Pilot Production. In 1962, Mr. Bianculli transferred to RCA Laboratories, Princeton, N.J., where he was Head of Device Technology and a member of the Advanced Manufacturing Equipment Research and Development Group. In 1970, he joined the Solid State Division's Equipment Technology Group and, in 1972, assumed his present position as Manager, Engineering Standards. He is currently a member of the American Society of Mechanical Engineers and of the Standards Engineering Society.

Dr. Ralph W. Engstrom completed his undergraduate work at St. Olaf College in 1935 and received the PhD in Physics from Northwestern University in 1939. Since joining RCA in 1941, he has been associated as an engineer, group leader, and engineering manager with various photosensitive devices, including photomultipliers, image tubes, and camera tubes. He has published numerous articles relating to these devices and their applications. At present Dr. Engstrom is a senior engineer serving as a staff consultant. He is a Fellow in the American Physical Society, a member of the Optical Society of America and of Sigma Xi.

Albert J. Skavicus received the BSEE (summa cum laude) from the Catholic University of America in 1943. Following his graduation, he taught in the ASTP Program at the Catholic University. He joined RCA in 1946 after two years of military service. Initial responsibilities were for design and development of portions of the Shoran Navigation and Bombing System in Camden, N.J.

In 1952, he was promoted to Engineering Group Leader responsible for design of the Shoran Mod II Ground Station. From 1955 to 1966, he was an engineering design manager on the Astra and Aries airborne radar fire control system. In 1966, Mr. Skavicus transferred to GCASD in Burlington, Mass. and assumed design responsibilities in the System Support Engineering Group. He was promoted to Section Manager of Engineering Services in 1968 and is currently in that position.

Haynes appointed to TREND Editorial Board

Harold E. Haynes has been appointed to serve on the TREND Editorial Board. Editorial Board Members participate in the planning, review, and approval of suitable material for publication in TREND.

Harold Haynes received the BSEE from the University of Nebraska in 1939, and in 1940 joined the Photophone Advanced Development group of RCA in Camden — an activity which through a long history has evolved into the present Advanced Technology Laboratories of G&CS. The activity was moved to Indianapolis in 1941, and returned to Camden in 1946. From 1957 to 1959 Mr. Haynes was a development engineer in the Commercial Electronic Products Division, and at the conclusion of that period was appointed Staff Engineer in ATL, a position he occupied for the next eight years. From 1967 to 1972 he headed the Advanced Development group of the Graphic Systems Division. In 1972 he was appointed Staff Engineer, G&CS, reporting to Dr. H.J. Woll, Division Vice President G&CS Government Engineering.

Jenny on Corporate Engineering Staff

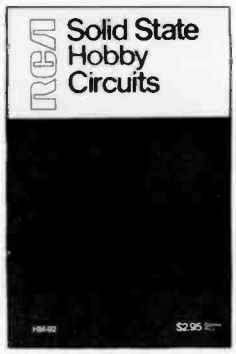
Dr. William J. Underwood, Director, Engineering Professional Programs, of Corporate Engineering has appointed **Hans K. Jenny** Staff Technical Specialist. In this capacity, Mr. Jenny is responsible for a variety of staff assignments for enhancing technical and professional stature among RCA's engineers and scientists. He will also serve as engineering management consultant to the functions of Engineering Professional Programs: Technical Communications, Technical Information Systems, and Engineering Education. Mr. Jenny was formerly Senior Technical Advisor in the Industrial Tube Division at Lancaster.

Mr. Jenny's biography appears with his review paper on electron tubes (p. 2, this issue).

Longo named to Delta Mu Delta

Anthony Longo, Engineering Leader, RCA Global Communications, Inc. was recently named to the national business honor society Delta Mu Delta, Alpha Xi Chapter at the New York Institute of Technology. The NYIT chapter was chartered as a means of recognizing superior scholastic achievement among students majoring in business administration. Mr. Longo is pursuing his master of business administration degree at the college's Old Westbury Campus.

In 1958 Mr. Longo joined RCA Laboratories, transferred to RCA Advanced Communications Laboratories, and then joined RCA Global Communications. At Globcom he is engaged in analysis of customer data communications requirements and is responsible for design and development of specialized systems hardware.



New Hobby Circuits Manual

An updated 400-page edition of the RCA *Hobby Circuits* manual is available from the Solid State Division. This edition presents 68 useful solid-state circuits plus substantial information on theory, operation, and construction of these circuits. The book has been organized specifically for experimenters, hobbyists, radio amateurs, educators, students, and others interested in solid-state devices and circuits.

The operation of each circuit is described in detail, and photographs, schematic diagrams, parts lists, and construction layouts are given. For most of the circuits, full-size drilling or printed-circuit templates are provided to simplify construction of the circuit boards.

Copies of the manual may be ordered at a special employee's price of $1.80 each (list price: $2.95) by sending checks or money orders to:

RCA Solid State Division
c/Julia Gawryluk,
Zone 126, Box 3200,
Somerville, N.J. 08876.

Since this offer is for RCA employees only, please include your clock and department numbers.

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*Technical Publications Administrators (asterisked * above) are responsible for review and approval of papers and presentations













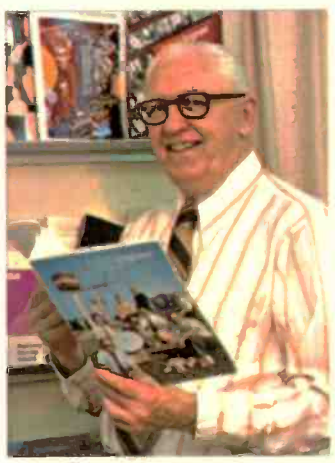
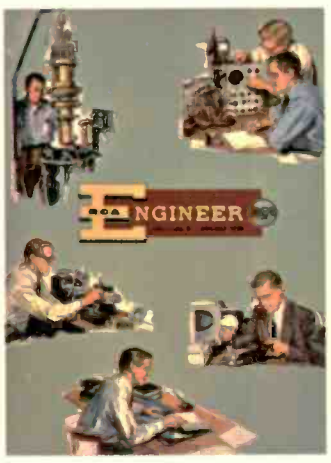







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