J. D. Callaghan 215-800

RCA ENGINEER

Vol. 8—No. 6 · APRIL—MAY 1963

RCA

OUR COVER

. . . an RCA 601 Computer System, delivered to the New Jersey Bell Telephone Company at Teaneck, N.J., in December 1962. This system was the first of five scheduled for customer delivery by the end of 1963. Shown are Miss Barbara Allen, New Jersey Bell Telephone Company Console Operator, J. J. Worthington, Manager of the RCA 601 Project, and Michael Arya, RCA 601 Logic Design Engineer.

The Tidal Wave of Electronic Data Processing

Electronic data processing—from a small ripple in the late 1940's—has surged into a powerful force for business, industry, and the military, and its momentum is increasing at a rapid rate. Technological and application developments have reinforced each other, providing additional impetus and directions for the field to propagate.

ENIAC, the first electronic computer, was delivered to the Aberdeen Proving Grounds in 1947. Mathematicians used its high-speed computation ability, provided by vacuum tubes, to solve artillery ballistic problems. In the early 1950's, magnetic memories gave the computer increased power and flexibility. In the same era, magnetic tape stations and drums began providing large and rapid bulk files for data and instruction storage. Augmented by high-speed input equipment and printers, the computer—which had been the almost-exclusive tool of the mathematician—became part of a data-processing system that could serve the business world in areas such as stock control, payroll application, and insurance billing.

The RCA 501 heralded the advent of the transistorized computers, which increased reliability, performance, and compactness and opened up new doors in the fields of military and industrial control.

Today, the practical applications of data-processing systems are being expanded by the development of micromagnetic and cryogenic memories, random-access files, optical character reading, data input and collection devices, fast and flexible display systems, and powerful means for integrating communication facilities with computers. The host of technological advances not only are opening up new functions but also are providing increased system performance at lower cost, bringing many new applications into economic practicality.

But in the final analysis, technological advances are only generating better and better tools. Far more people are required *to effectively utilize* these tools than to develop them. The challenges of successful application are in many ways more difficult. Historically, it has been difficult and slow to overcome the inertia and smugness of present practice. The rewards are great, however, and one only has to view the many application advances to "get the picture."

Engineering is presently utilizing computer systems for mathematical reductions, statistical analysis, circuit design, generation of wire lists, drawing control, schedule and cost control, and simulation studies, to name a few. *Increased productivity* is a primary challenge to all of us, and it is the goal that we *must* achieve to stay competitive—whether from an individual, or company, or national point of view. Electronic data processing provides a tremendous opportunity to achieve this goal. It will require that the individual become knowledgeable and conversant with this tool and that he apply it imaginatively to his area of responsibility.

The wave is here. *Are you prepared to swim?*

A. D. Beard
Chief Engineer
Electronic Data Processing
Radio Corporation of America

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VOL. 8, NO. 6

APRIL-MAY 1963

CONTENTS

A TECHNICAL JOURNAL PUBLISHED BY **RADIO CORPORATION OF AMERICA,** PRODUCT ENGINEERING 2-8 CAMDEN, N. J.

● *To disseminate to RCA engineers technical information of professional value.* ● *To publish in an appropriate manner important technical developments at RCA, and the role of the engineer.* ● *To serve as a medium of interchange of technical information between various groups at RCA.* ● *To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions.* ● *To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field.* ● *To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management.* ● *To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.*

An index to RCA ENGINEER articles appears annually in the April-May issue.

Managers, Leaders, and Laboratory Directors whose engineers and scientists prepare RCA internal technical reports accomplish these goals: 1) keep other RCA engineers informed, 2) enable RCA engineers to gain new insight, 3) solve related engineering problems, and 4) further the use of RCA's scientific knowledge. This paper generally describes RCA's technical reporting program and answers questions about the author's professional task of writing reports.

The Engineer and the Corporation

TECHNICAL REPORTS AND ENGINEERING MEMORANDA: Questions and Answers

W. O. HADLOCK, Administrator
RCA Technical Publications
Product Engineering, Research and Engineering
Camden, N.J.

ENGINEERS AND SCIENTISTS who provide *Technical Reports* (TR's) and *Engineering Memoranda* (EM's) benefit their associates in other divisions—and implement RCA policy effectively. More important, the engineers producing such reports help secure for RCA a *maximum return on its investment* in engineering and research.

Each division in RCA has a specific operating procedure (Refs. 1 and 2 are examples) covering the preparation and distribution of TR's and EM's. Because such instructions vary in minor detail, the information herein is generally applicable to engineers and scientists in all activities. For additional information, engineers are encouraged to seek the advice of engineering supervisors — and the *Technical Publication Administrators* or *Technical Report Coordinators* (see Fig. 1).

RCA'S POLICY FOR TR's AND EM's

Quoted here is a statement of RCA's policy regarding TR's and EM's[3]; the essence of this policy is incorporated in the formal procedures of the major divisions of RCA.

> "It is the policy of the Radio Corporation of America:
>
> 1) To record the results of engineering and research investigations and distribute them internally to all major operating units. In this way, technical progress becomes available to the interested engineering and management employees, and duplicate investigations can be avoided. All RCA units will actively support this policy by (1) requiring preparation of reports where results merit dissemination and (2) providing the authors with the necessary writing time."

GENERAL INFORMATION ON TECHNICAL REPORTS

TR's and EM's are *company private* documents; they provide information for use by appropriate technical personnel within RCA. Such documents are traditional communication media used by RCA for nearly three decades to transmit scientific knowledge within the Corporation, and are available for reference at RCA engineering libraries.

Why Write Reports?

RCA engineers must do more than discern and solve new problems. Their professional responsibility includes the preparation of reports to benefit other RCA engineers. Here are some of the reasons for writing reports:

1) Provide a permanent record (for patent, legal, engineering and management) of valuable work completed.
2) Avoid duplication of engineering and research.
3) Inform other engineers of results accomplished to help solve their related problems.
4) Suggest techniques for other scientific work.
5) Show that certain methods of solution are blind alleys.
6) Use as a basis for future technical papers.

TR's and EM's capture the interest of engineering management and others who may further apply new ideas—a novel idea usually has value far beyond that envisioned originally.

What is a TR?

A TR records the results of important engineering or research work. TR's can represent either significant small parts of the project or the total result. Often, the written report is the only record that work was undertaken, completed and evaluated. The contents of the reports vary widely; however, TR's usually represent the best information obtainable from an engineering group.

What is an EM?

The EM records results of engineering or research investigations limited in scope, but which may be of interest to other RCA units. Examples are: description of some unusual phenomenon discovered in the course of a project, trip reports, or reports on technical meetings attended. EM's are less formal than TR's, often represent the endeavors of an individual engineer, and may cover preliminary investigations, ultimately to be covered by a TR.

Shall it be a TR or an EM?

TR's provide a medium for interchanging major technical information and stimulating internal feedback. TR's and most EM's receive a corporate-wide distribution. When EM's are of interest to only a small number of persons, distribution may be limited to a few interested engineers. The final decision of whether the report shall be a TR or an EM is made by the engineer-author and his supervisor who can appraise the significance of the work done.

WILLIAM O. HADLOCK graduated from Clarkson College of Technology with a BSEE. Upon graduation, he joined General Electric's Radio Receiver Engineering where he worked in components engineering, design of farm radios, and later in television transmitter design. During World War II he became Assistant Mgr. of Commercial Service Activities, GE Electronic Tube Division, and introduced GE's series of Electronic Tube Manuals. Mr. Hadlock joined RCA in 1947 to work on the Advertising and Promotion of RCA technical equipment for sale to TV and Broadcast Stations. In 1949, he became Mgr., Broadcast and TV Advertising and Sales Promotion and Managing Editor of "Broadcast News". In 1955, Mr. Hadlock became Editor, "RCA ENGINEER", to inaugurate and publish the present company-wide journal. In 1959, he was also named RCA Staff Technical Publications Administrator. Mr. Hadlock is a Senior Member of IEEE, Member of PTGEWS, and a member of the American Association of Industrial Editors.


L. S. BEENY, RCA International Div., Clark, N. J.


K. A. CHITTICK, RCA Victor Home Instruments, Indianapolis, Ind.


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W. A. HOWARD, NBC and RCA Institutes, New York, N. Y.


W. C. JACKSON, RCA Communications, Inc., New York, N. Y.


. A. M. MAX, RCA Victor ecord Div., Indianapolis, id.


C. A. MEYER, Electron Tube and SC&M Divisions, Harrison, N. J.


T. T. PATTERSON, Electronic Data Processing, Camden, N. J.


D. R. PRATT, Broadcast and Communications, Camden, N. J.


H. J. RUSSELL, RCA Victor Co., Ltd., Montreal, Can.


C. W. SALL, RCA Laboratories, Princeton, N. J.


F. D. WHITMORE, Defense Electronic Products, Camden, N. J.

When to Write Reports?

The occasion to write a TR or an EM may arise during the course of an engineering investigation as well as upon its completion. Although contract reports are usually stipulated and scheduled by the contracting agencies, such work may later form the basis for valuable TR's. The engineer can, with the guidance of his leader, manager or lab director, determine the proper timing. Generally, publication of TR's and EM's should be considered as follows:

1) Upon completion of a major engineering project.
2) Upon completion of any discrete portion of a project.
3) Whenever the information is of value to RCA engineers.
4) Whenever new techniques are developed.
5) When unclassified contract reports are of interest to other divisions, and can be issued as TR's and EM's.
6) When classified contract reports are declassified, and can be converted to TR's and EM's.
7) Prior to public disclosure of new information.

Who is Eligible to Write a Report?

RCA engineers or scientists are encouraged to prepare TR's and EM's as a part of their work. However, all members of the RCA technical staff, including the managers, leaders, project administrators and technicians are eligible to write reports. Before the decision is made to write, the author should obtain approval from his supervisor.

Other RCA Reports, and Government Reports

Several other categories of reports are used within RCA, such as Government Contract Reports, Progress Reports, and Coded Engineering Letters. Distribution and release of such material is controlled by the Chief Engineer.

Government Contract Reports are prepared and distributed in accordance with the terms of the contracts in which RCA participates, and in conformance with Government security regulations included in the RCA Personnel Policy Manual and Procedures of each division.

Although TR's and EM's are not recommended for reporting classified work, certain phases of such work may be unclassified and valuable (as TR's and EM's) to engineers in other divisions. When Government Contract Reports are declassified, engineering supervisors should distribute the pertinent information (as TR's or EM's).

Required Approvals

Each division has definite approval requirements for TR's and EM's. These nearly always include the following, in advance of distribution: 1) Technical and administrative (policy) approval by the head of the engineering activity, the Chief Engineer or his designated representative, and 2) patent approval by the Director, Domestic Patents.

Report File Numbers

Every TR and EM must bear a report index (file) number[1,2,3] to facilitate future reference, library filing, and retrieval. Report numbers should appear in the upper right-hand corner of the title and distribution pages. Contact the Technical Publications Administrator (TPA) or the activity in your division responsible for the assignment of appropriate index numbers for TR's and EM's.

DISTRIBUTION OF TR'S AND EM'S

Each division of RCA initiates a corporate-wide *minimum standard distribution* to key engineering personnel in all activities of RCA. This minimum distribution is based on the recommendations of major operating unit staffs. Additional distribution can be made by the originating division to authorized RCA personnel having sufficient interest. In some divisions, the need to limit distribution may arise because of contractual requirements.

Initial distribution includes two groups: 1) those requiring complete reports, and 2) those requiring "title pages only" (these include summary and distribution pages). A wide distribution of title pages and a small mailing of complete reports keeps engineering activities informed and reduces paperwork. Recipients of title pages may borrow complete reports from local libraries. Success of the "title pages only" distribution relies on libraries having reference copies of complete reports available.

PLANNING AND ORGANIZING TR'S

A technical report must present facts together with logical conclusions and recommendations. Thus, the writer's goal is to organize and present essential facts and related material so that the report can be easily understood.

Early Analysis: Analyze the entire project before writing. Ask and answer these questions: What is the purpose of the report? Who will the readers be? How much background must be included? Can the reader make an intelligent evaluation? What is the message for the reader? What steps were followed in the project?

Value of an Outline: Before starting the rough draft, make an outline to answer the above questions. Change the outline, add to it, or subtract from it, as work progresses. Major headings in the outline finally become the table of

Fig. 2 — Combination "topic-sentence outline" for preparing TR's and EM's.

I. PLANNING AND ORGANIZING
  1. Preliminary
     a. Study available material; keep good records.
  2. Early Writing Stages
     a. Decide on audience and reader needs.
     b. Analyze material; decide what to say.
     c. Make rough outline as a guide.
  3. Consider Forms of Organization
     a. Chronological account (rare)
     b. Describe a product or technique
     c. Emphasize methodology
     d. Describe a project
     e. Describe an investigation

II. WRITING THE REPORT
  1. Get it on paper promptly; rewrite and polish.

III. A "TR" ON AN INVESTIGATION
  1. **Front matter:** Title—summary, distribution, and content pages.
  2. **Introduction:** Importance of work, objectives, preview of contents, and gist of conclusions.
  3. **Body:** Summarize findings; describe equipment, methods, and results.
  4. **Conclusions, recommendations** and bibliography.
  5. **Appendix:** History, derivations, and detailed data.

IV. ILLUSTRATING
  1. Complement and illuminate the text.
  2. Simplify diagrams; use in right places.

V. OBSERVE CONVENTIONS OF UNIFORMITY
  1. Spelling and punctuation.
  2. Tables, literature citations, etc.

contents of the report (Fig. 2). Before beginning a project, a preliminary outline frequently helps determine the developmental steps necessary.

WRITING EFFECTIVE REPORTS

Major features of effectively written reports are as follows: 1) they are technically sound, 2) they contain useful information and whenever possible, advances in the state-of-the-art, 3) they are positive in tone, factual, logical and impersonal, and 4) they assist other engineers.

Obtaining Good Readability

To communicate ideas, a report must satisfy the specialized readers to whom it is directed—and, at the same time, be understood by as wide an audience as possible. So, select the "nuggets" of the work for special attention instead of repeating all the stages of thought and action. However, occasionally unproductive results may be of great interest and of value to certain engineers. This is a matter of judgment for the author.

Satisfy reader requirements by writing the summary, report proper, and the appendix in varying degrees of detail. The *summary* provides the gist of the report. The *body* appeals to the reader who follows the work closely. The *appendix* supplies calculations and detailed analysis. Thus, an effective, easy-to-read report tells the story in barest facts, repeats it in greater detail, and supports the main thesis with related information. Here are ten important "do's" for better readability:

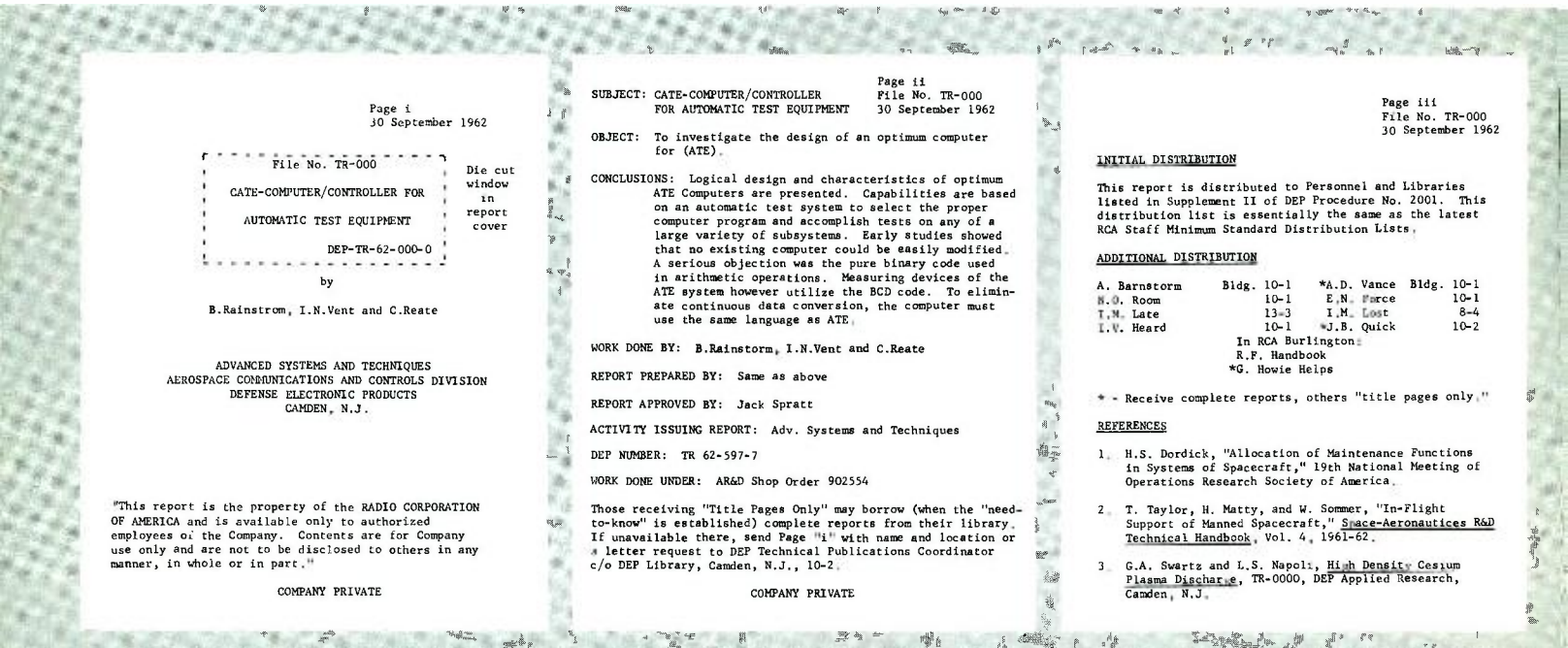
1) Satisfy your reader by communicating ideas.
2) Be direct—avoid backing into ideas.
3) Avoid "weasel" words; e.g., *it is reported, it might appear, it is not too clear.*
4) Weed out unnecessary words; e.g., *whereas, due to the fact that.*
5) Avoid over-elaboration and self-debates.
6) Use active verbs to express positive action.
7) Keep sentences and paragraphs short.
8) Speak out with ideas; do not imply.
9) Reinforce with appropriate illustrations.
10) Make conclusions and recommendations forceful.

ELEMENTS OF TR'S AND EM'S

Uniformity in appearance, contents and arrangement of RCA intradivisional TR's and EM's is desirable. Understandably, minor variations such as the types of covers and handling of title-page summaries do exist. However, *all reports usually require the following basic elements*; these are illustrated by the sample pages in Figs. 3 to 8.

Report Covers

TR's and EM's can be bound in any appropriate folder or cover such as RCA Form #339 for smaller reports, or RCA Form #239 for larger ones. Satisfactory covers are available in the various divisions. Technical Publications Administrators or Report Coordinators will recommend the most suitable types. Some, such as DEP's Form #DE-222, have window cutouts through which the title of the report appears (Fig. 3).



Page i
30 September 1962

File No. TR-000

CATE-COMPUTER/CONTROLLER FOR

AUTOMATIC TEST EQUIPMENT

DEP-TR-62-000-0

Die cut window in report cover

by

B.Rainstrom, I.N.Vent and C.Reate

ADVANCED SYSTEMS AND TECHNIQUES
AEROSPACE COMMUNICATIONS AND CONTROLS DIVISION
DEFENSE ELECTRONIC PRODUCTS
CAMDEN, N.J.

"This report is the property of the RADIO CORPORATION OF AMERICA and is available only to authorized employees of the Company. Contents are for Company use only and are not to be disclosed to others in any manner, in whole or in part."

COMPANY PRIVATE

Fig. 3—A title page for use with window-type cover like the DEP-222. Note information that shows through cover cutout.

Page ii
File No. TR-000
30 September 1962

SUBJECT: CATE-COMPUTER/CONTROLLER FOR AUTOMATIC TEST EQUIPMENT

OBJECT: To investigate the design of an optimum computer for (ATE).

CONCLUSIONS: Logical design and characteristics of optimum ATE Computers are presented. Capabilities are based on an automatic test system to select the proper computer program and accomplish tests on any of a large variety of subsystems. Early studies showed that no existing computer could be easily modified. A serious objection was the pure binary code used in arithmetic operations. Measuring devices of the ATE system however utilize the BCD code. To eliminate continuous data conversion, the computer must use the same language as ATE.

WORK DONE BY: B.Rainstorm, I.N.Vent and C.Reate

REPORT PREPARED BY: Same as above

REPORT APPROVED BY: Jack Spratt

ACTIVITY ISSUING REPORT: Adv. Systems and Techniques

DEP NUMBER: TR 62-597-7

WORK DONE UNDER: AR&D Shop Order 902554

Those receiving "Title Pages Only" may borrow (when the "need-to-know" is established) complete reports from their library. If unavailable there, send Page "i" with name and location or a letter request to DEP Technical Publications Coordinator c/o DEP Library, Camden, N.J., 10-2.

COMPANY PRIVATE

Fig. 4 — DEP's "title page" includes a summary; this plus a cover sheet and the page of Fig. 5 go to the "title-page-only" lists.

Page iii
File No. TR-000
30 September 1962

INITIAL DISTRIBUTION

This report is distributed to Personnel and Libraries listed in Supplement II of DEP Procedure No. 2001. This distribution list is essentially the same as the latest RCA Staff Minimum Standard Distribution Lists.

ADDITIONAL DISTRIBUTION

A. Barnstorm	Bldg. 10-1	*A.D. Vance	Bldg. 10-1
N.O. Room	10-1	E.N. Force	10-1
T.M. Late	13-3	I.M. Lost	8-4
I.V. Heard	10-1	*J.B. Quick	10-2
In RCA Burlington:			
R.F. Handbook			
*G. Howie Helps			

* - Receive complete reports, others "title pages only."

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1. H.S. Dordick, "Allocation of Maintenance Functions in Systems of Spacecraft," 19th National Meeting of Operations Research Society of America.
2. T. Taylor, H. Matty, and W. Sommer, "In-Flight Support of Manned Spacecraft," Space-Aeronautics R&D Technical Handbook, Vol. 4, 1961-62.
3. G.A. Swartz and L.S. Napoli, High Density Cesium Plasma Discharge, TR-0000, DEP Applied Research, Camden, N.J.

Fig. 5 — DEP's distribution page refers to the standard and additional mailings made.

Title Page and Summary

The title, names of the authors, report file number, and date are repeated on the title page. Carefully select titles to be brief but comprehensive enough to be distinguished from other reports. Government contract numbers (when required) are included on the title page (Fig. 4).

The subject, object, and conclusion (Fig. 4) serve as an effective summary or abstract. These elements give the reader a concise preview of what he will find in the report. Such a capsule assists the reader who scans—and encourages the serious reader to study the report more thoroughly.

Distribution Page and References

This page includes the following information: *Company Private* notation, file number, date, and a distribution statement covering the "minimum standard" distribution or a code number specified by divisional procedures. Special distribution is listed by name and location, indicating whether complete reports or title pages were sent (Fig. 5). Numbered references may also be included for the convenience of those receiving "title pages only."

Table of Contents

The table of contents should include the main divisions and subdivisions of the report, showing page numbers where material can be found. Appendixes, tables, and figures may also be listed on the contents page (Fig. 6).

Introduction

To help the reader, repeat the title at the top of the introduction page. A good introduction indicates what is to follow, defines the subject under discussion, and states objectives. Reference to companion projects will be helpful—assume the reader has little knowledge of the purpose or scope of the investigation. Prior research problems, associated concepts, and prevailing ideas may be briefly described.

Description of the Investigation

The section following the introduction describes what was done and how it was achieved. (Fig. 7 is a typical text page.) Include enough information so the readers can reach an opinion of the accuracy, reliability, and usefulness of the work. Typical items to discuss are as follows: 1) theoretical considerations, 2) experimental procedures, 3) design of apparatus, 4) comparison of predicted and observed data, and 5) summarized results.

Conclusion and Recommendations

This final section enumerates significant findings, and supplies supporting information needed to understand what was achieved. Recommend steps for applying the results of the work. Describe benefits expected from such application and mention unique features of the work. Suggest further work that seems desirable State opinions, but distinguish those not supported by proof.

Appendixes

Supplementary information too specialized to include in the body of the report (but important to some readers) should be presented in appendixes. Examples are as follows: lengthy historical background, details of experimental equipment, procedures, analytical methods, calculations, and derivations.

References and Bibliography

Referenced items are numbered sequentially to agree with the order in which superscript numbers appear in the text. Bibliographies may include any publication which the engineer-author considers helpful. Abstracts, letters, or private communication may be referenced in the absence of formal printed publications. Fig. 8 is a bibliography showing the style for eight types of literature citations.

ACKNOWLEDGMENT

The Technical Publications Administrators and Report Coordinators (Fig. 1) supplied valuable source material and made helpful suggestions for this article.

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1. *Preparation and Control of Technical Reports, Engineering Memoranda and Contract Reports*, DEP Procedure No. 2001.
2. *Technical Reporting Procedure*, RCA Laboratories No. 503.
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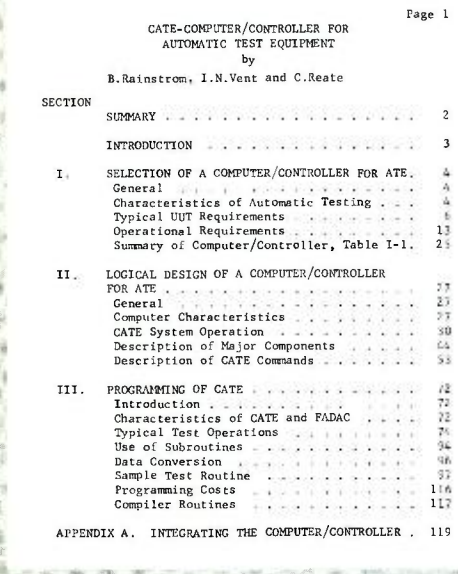


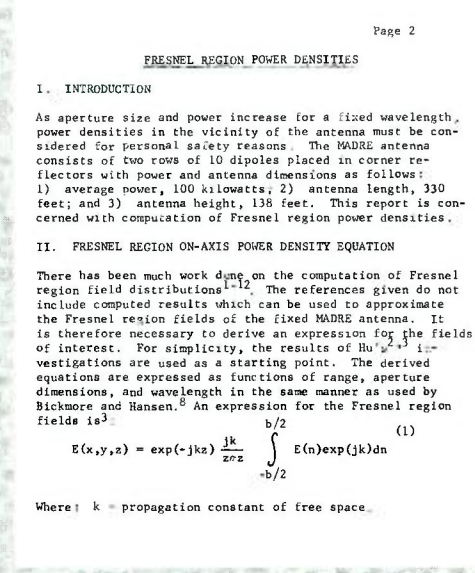
Page 1

CATE-COMPUTER/CONTROLLER FOR AUTOMATIC TEST EQUIPMENT

by

B.Rainstrom, I.N.Vent and C.Reate

Fig. 6—A table-of-contents page; introductory and text pages follow.



Page 2

FRESNEL REGION POWER DENSITIES

I. INTRODUCTION

As aperture size and power increase for a fixed wavelength, power densities in the vicinity of the antenna must be considered for personal safety reasons. The MADRE antenna consists of two rows of 10 dipoles placed in corner reflectors with power and antenna dimensions as follows: 1) average power, 100 kilowatts; 2) antenna length, 330 feet; and 3) antenna height, 138 feet. This report is concerned with computation of Fresnel region power densities.

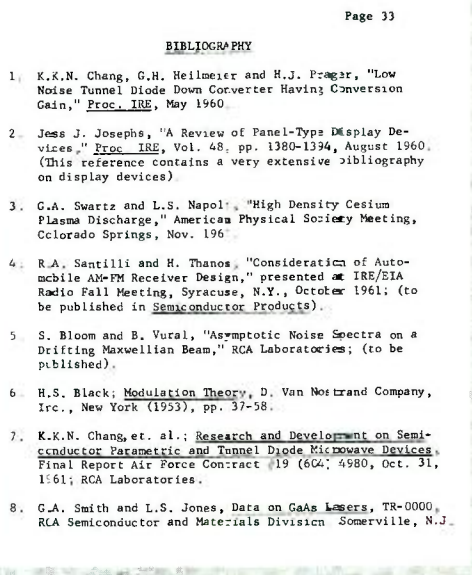
II. FRESNEL REGION ON-AXIS POWER DENSITY EQUATION

There has been much work done on the computation of Fresnel region field distributions[1-12]. The references given do not include computed results which can be used to approximate the Fresnel region fields of the fixed MADRE antenna. It is therefore necessary to derive an expression for the fields of interest. For simplicity, the results of Hu[2,3] investigations are used as a starting point. The derived equations are expressed as functions of range, aperture dimensions, and wavelength in the same manner as used by Bickmore and Hansen.[8] An expression for the Fresnel region fields is[3]

$$E(x,y,z) = \exp(-jkz)\,\frac{jk}{z\sigma z}\int_{-b/2}^{b/2} E(n)\exp(jk)dn \qquad (1)$$

Where: k = propagation constant of free space

Fig. 7—Typical text page for "TR's"; a report title and introduction are included.



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5. S. Bloom and B. Vural, "Asymptotic Noise Spectra on a Drifting Maxwellian Beam," RCA Laboratories; (to be published).

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Fig. 8—Typical reference list or bibliography. Eight types of citations are included.

RCA COMPUTER RESEARCH

... Some History, and a Review of Current Work

Dr. J. A. RAJCHMAN, Director
Computer Research Laboratory
RCA Laboratories
Princeton, N. J.

DR. JAN A. RAJCHMAN, Director, of the Computer Research Laboratory, RCA Laboratories, Princeton, N. J. developed the magnetic core memory system that is now the standard information-storage device in modern computers, and is responsible for pioneering contributions to the development of the electron multiplier tube. Dr. Rajchman received the Diploma E.E. (equivalent to an MSEE) in 1934 and a Doctor of Science degree in 1938 from the Swiss Federal Institute of Technology. His entire professional career has been with RCA. A student engineer at Camden during the summer of 1935, Dr. Rajchman a research engineer in 1936. In 1942, he was transferred to the RCA Laboratories in Princeton. He became Associate Director, Systems Research Laboratory, in 1959. He assumed his present position in September 1961. His first field of work was electron optics. During World War II, he was among the first to apply electronics to computers. Later, he worked on the betatron. After the war he resumed work on computers and developed the selectron, and shortly thereafter, the magnetic core memory. He contributed many magnetic switching circuits, the transfluxor, the magnetic plate memory, and magnetically controlled electro-luminescent display panels. Dr. Rajchman is co-recipient of the 1947 Levy Medal of the Franklin Institute for his work on the betatron. He received the Liebmann Memorial Prize for the year 1960 for his contributions to the development of magnetic devices for information processing. Dr. Rajchman is a holder of more than 90 U.S. Patents and the author of many technical papers. He is a Fellow of the IEEE.

RCA computer research effort is centered in the Computer Research Laboratory of the RCA Laboratories, Princeton, N. J. This paper first traces the beginnings and progress of that research as far back as 1939. Perhaps surprising will be the significance of RCA contributions to early computer development. While RCA was not the first to commercially exploit the computer, it was actually a major pioneer in computer research. The present work of the Computer Research Laboratory is then reviewed with attention to memory speeds and storage capacity, superconductive memories, content-addressable and read-only memories, logic switching circuits, input-output devices, and computer theory.

THE COMPUTER RESEARCH LABORATORY of RCA Laboratories, Princeton, is concerned with conception and realization of computer systems, subsystems, and components, as well as with computer applications. It comprises more than fifty scientists and engineers in a field of growing importance to RCA. Established as a separate entity in September 1961, it is now one of the six main laboratories of the David Sarnoff Research Center.[1]

SOME HISTORY

Computer research started at RCA as far back as 1939. The impetus was the dire need to replace the slow and inaccurate "directors" then used for controlling anti-aircraft guns by rapid and accurate controls made necessary by the fast planes of the day. There was real vision on the part of the military to perceive then that such complex calculations could be achieved by electronics. After all, in those days electronic pulse counters used in cosmic-ray research were the closest thing to electronic computers. In the early war years, a small group at RCA in Camden took this extremely interesting challenge and worked out many of the fundamental principles of electronic computers still in use today. The two main approaches, analog and digital, were considered. (At that time these were called *continuous* and *discrete*.) The analog approach yielded the first practical solution to the fire-control problem, and an actual computer was used in combat.

In the digital approach, of direct interest here, great progress was made in the concepts and prototype circuits, but the technology of those days did not permit the practical realization of such computers for field use. It was realized then that computations in the binary code are the simplest (although manipulation of decimal numbers by properly coded *on-off* signals was also considered). All the elements necessary for a complete binary computer were conceived and incorporated in experimental prototypes. These included registers of flip-flops, shift registers, counters, adders and subtracters, multipliers and dividers, and generalized code converters. Because the vacuum tube was then the only device that provided gain and a switching threshold, a great deal of mixing of signals by resistive networks was used for logic switching. Today, this would be called *threshold logic* or *majority logic*.

For instance, one example of such networks was in connection with carries occurring in binary arithmetic when the sum of the digits exceeds one —the equivalent of exceeding nine in the decimal system. The chain of carries that can run the full length of the number to be added was obtained by resistively coupled circuits. Multiplication was produced by successive additions made in a single adder, alternated with register shifts, as is generally done today. But interestingly enough, an "integrated" multiplier was also made in which all additions were made simultaneously in a single DC-coupled circuit including a number of adders. Fig. 1 shows such a multiplier for two 6-digit numbers (up to 64 by 64).

Another device based on resistive or other high impedance coupling was a code converter that we then called an *arbitrary function generator* and would in some instances today call a *read-only fixed memory*. The device consisted of numerous resistances located at selected locations of a regular array that were connected by columns and rows. When the column wires were energized according to the input code, a certain unique row was selected. The selected row turned on a tube whose output excited a corresponding row wire in another array in which the pattern of the locations of the resistances determined the desired fixed code conversion. The potentials on the column of this second array were indicative of the output. Fig. 2, shows part of a 1942 experimental array which comprised more than 10,000 resistances, and which converted a 7-bit code into a 13-bit code and operated in about 20 μsec.

We soon realized that complete computers could be built for solving intricate equations at high speed, including those of the original fire-control problem, by using a sufficient number of regular radio tubes. However, the tremendous number, running into many thousands, seemed to make the approach impractical. We then developed a special vacuum tube, the *Computron*, in which the many logic functions necessary in an adder and multiplier were obtained by direct connections between electrodes within the tube itself.

About that time, the need became acute for much more rapid computing of ballistic tables for guns because computations by existing methods lagged the constant improvements in weapons. In fact, the need was so pressing that the government decided to undertake the development of an electronic computer despite the requirement for an estimated 20,000 to 30,000 tubes. The project was considered by RCA, but actually was undertaken by the University of Pennsylvania and resulted in one of the first electronic computers, the ENIAC. However, since the work that had been done at RCA was by far the most advanced at the time, we were asked to consult on the project. Many of our ideas were actually the basis of the circuits used, particularly the resistive function generator.

Early Memories

The next chapter in RCA's computer research dates back to the period immediately following the end of the war. At that time, John Von Neumann of the Institute of Advanced Study in Princeton put forward a far-reaching proposal for building a universal machine which would be based on the use of a stored program. The idea was to have a central memory in which numbers could be stored and from which they could be extracted, and a means to solve the problem through a programmed series of coded instructions which themselves could be stored in the memory. A single arithmetic processor and means for input and output completed the computer. By writing various programs, the same machine could be made to solve a great variety of problems; in fact, any problem whose solution could be obtained by a logical sequence of computations. The idea of the stored program was born gradually while the ENIAC and some of its successors were being designed. Von Neumann crystallized all these ideas into an extremely elegant proposal that can well be considered as being the foundation of the present art.

What was needed above all, of course, was an electronic memory and this is what RCA Laboratories undertook to provide. The year was 1947. The memory had to have a so-called *random access*—that is, be able to accept information identified by a coded address and deliver it on the basis of that address. This allowed the information to be stored and retrieved in any order without any sequential scanning of the entire memory as was necessary in the case of some proposals at the time. We conceived a purely "integrated" storage tube which we called the *Selectron* (Fig. 3). The tube had two orthogonal sets of parallel wires by which a flow of electrons could be controlled so as to pass through any desired selected window formed by the wires. The electron current at that window bombarded a metallic element which stored information in terms of one of two stable potentials. *This tube was the first truly digital random-access memory*. It had a storage of 256 bits and an access time of about 15 μsec. At the time, this tube was the ultimate in intricate vacuum-tube technology, and although it had nearly ideal performance, it was relatively expensive. RCA made a few hundred Selectrons for a machine made at the Rand Corporation in California. This machine was patterned after the one at the Institute of Advanced Study at Princeton University. The tubes operated satisfactorily for about five years until the machine was made obsolete by commercial models with magnetic memories.

Magnetic Memories

In the late forties the memory still presented a problem. A variety of beam-deflected cathode-ray electrostatic storage tubes were developed, the simplest in structure and the most widely used being the so-called Williams tube. However, we were looking for a more reliable and less-delicate memory system.

Fig. 1—Digital multiplier (1940 vintage) for numbers up to 64 by 64 = 4096.

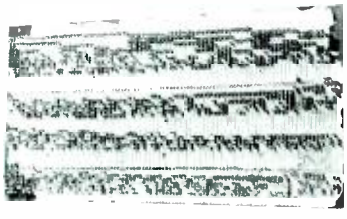


Fig. 2—Resistive matrix for code conversion, or early "read-only" memory (1942).

Fig. 3—Selectron memory tube, 256 bits.

Fig. 4—Myriabit core memory 10,000 cores 0.054 OD, 0.034 ID.

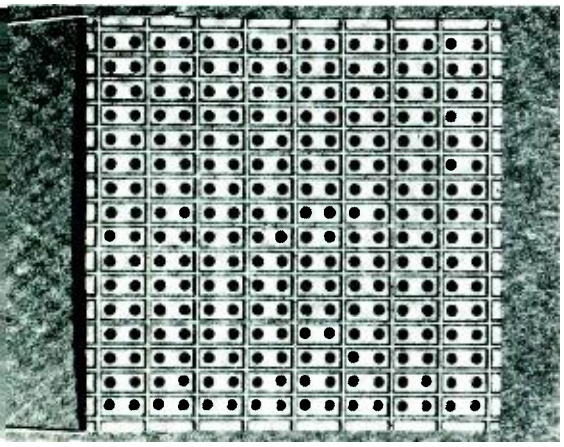


Fig. 5—Ferrite aperture memory plate; 256 bits, ¾" square.

This epoch marks a most important step in computer research at RCA Laboratories: the conception of the magnetic memory. It proved to be far more reliable than the storage tubes, generally extendable to larger capacities, capable of working faster, and also less expensive. At approximately the same period, a group at MIT also worked on magnetic memories.

The principle of magnetic memory operation depends on storing each bit in terms of the direction of remanent magnetization in magnetic cores, which may be shaped as rings. In a sense the core "remembers" in which direction it was excited last. The read-out is obtained by attempting to change the state of the core by sending a current through it in a given direction. If the state changes, the induced voltage due to the change of flux provides the read-out signal and the knowledge permits restoration of the core to its original state. This procedure is the so-called *destructive read-out* mode. The selection of a core among many in an array is obtained with a relative economy of driving circuits by making it necessary that two or more currents energize the core in coincidence for it to switch. This requirement presupposes that the cores have a sharp and well defined threshold of switching—that is, that they are made of a material with a substantially rectangular hysteresis loop. Special alloys of metals having such loops had been developed during the war for magnetic amplifiers and permitted us to make the first magnetic-memory prototypes. But these were delicate, expensive, and relatively slow in switching.

Fortunately, ferrites had been developed at RCA Laboratories for use in transformers and cathode-ray-tube deflection yokes, and proved to be fast switching, rugged, and inexpensive. The problem was to obtain ferrites with rectangular loops. These were obtained from the Materials Section of RCA Laboratories in a relatively short time through the synthesis of ferrites with the proper compositions—with magnesium and manganese activators. Methods were then developed to automatically mold and test small cores. The smaller the core, the less driving current it required and the faster it switched—but, of course, the more difficult it was to handle and wire. The compromise size, an outside diameter of 0.054 inch, that was chosen for the large experimental prototype turned out to be the reduced size reached in production only three years ago. The prototype, dubbed the *Myriabit* (Fig. 4) had 10,000 cores, required several racks of vacuum tubes, and operated in a cycle time of about 25 μsec. (A description of the Myriabit was published in 1953.) Since then, the ferrite-core memory has been highly perfected. The advent of the transistor made it possible to greatly reduce the size and power of the associated circuits. Memories with hundreds of thousands to millions of bits operating in a few microseconds are now standard products.

The fact that in the memory the core is used as switching element, in addition to its main storing function, induced us to consider it as a switch for pure logic functions. Array and combinatorial switches were developed, some of which are still used for addressing memories. The magnetic shift register, developed elsewhere in the mid-forties, was greatly improved. The general possibility of an all-magnetic computer with only a few tube drives was fully demonstrated, but the spectacular advent of transistors provided a much better technique for digital switching. Incidentally, this is an example of the abundance of technical means that are at our disposal today. If it were not for the transistor, all present computers would probably be magnetic. As it happens, there is a revival of interest in magnetic switching for space use where immunity to radiation damage and great reliability are of paramount importance.

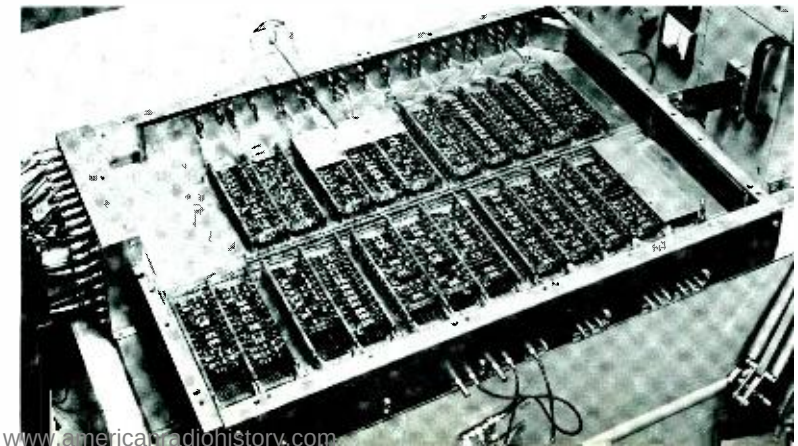
The next step in magnetic memories was toward integrated fabrication in an effort to avoid the necessity of making and wiring each core individually. A plate of ferrite was molded with an array of holes and covered with a metallic coating so patterned as to provide a winding linking all holes. The plate had 256 holes in an area ¾ inch x ¾ inch (Fig. 5). The apertured plate was a significant advance and was the precursor of recent successes in micromagnetics, and at the time, of the transfluxor.

The transfluxor[2] includes a square loop core with two or more apertures. It can store digital and analog information and can be read off nondestructively. The device has found a great variety of specialized applications. It has also been used in all-magnetic logic consisting of circuits with transfluxors and wire only. Memories with nondestructive readout as well as content-addressable memories were made of transfluxors. The transfluxor was the basis of the first electroluminescent display array, a description of which was published in 1957.

Ultra Fast Computers

To complete the historical background leading to our present position, mention must be made of a relatively large Navy-sponsored research program which RCA undertook in mid-1957. This program was aimed at increasing the speed of computers from 1 Mc to 1,000 Mc. The Laboratories played the major role in the project in its early stage, while RCA Electronic Data Processing (EDP) & Materials Division (SC&M) did most of it during the latter part of the program. Many phenomena were canvassed as possible candidates for extremely fast devices, including such diverse effects as vacuum electronics, ionization in semiconductors at very low temperatures, superconductivity, magnetic switching and effects in thin films. However, substantial effort was devoted to only two approaches: The first depended on the use of a variable-capacitance diode in phase-locked oscillator circuits operated at microwave frequencies. The second and more successful approach was that of the tunnel diode. Shortly after the publication by Esaki of the tunneling

Fig. 6—Logic subsystem of tunnel diodes with stage delay of 1 nsec.



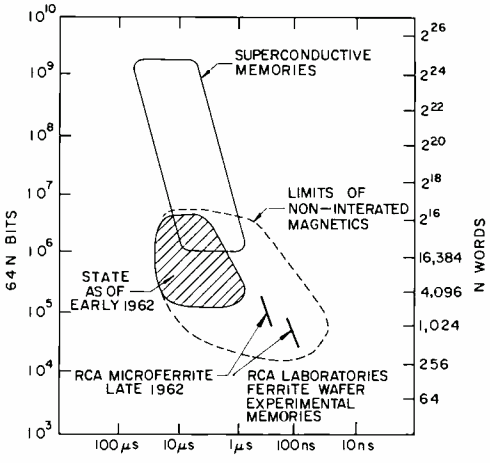


Fig. 7—Storage capacity and cycle time of various memories.

diode effect, work was undertaken at the Laboratories on tunnel diodes. Tunnel diodes operating at the speed of interest were developed in a very short time. Since the tunnel diode is a two-terminal device with negative resistance, entirely new circuit concepts were required to capitalize on the gain inherent in the negative resistance and to provide directionality to the information flow. An exhaustive study of possible circuits was made. A certain type of DC-coupled circuit was finally selected and with it EDP has succeeded in building a prototype subsystem demonstrating the technical feasibility of both tunnel diode logic and memory. The logic stage delay is about one nanosecond, and the essential logic elements can be operated at 300 megapulses/sec, (Fig. 6). This is essentially within the original goal. The project gave birth to the modern high-speed digital circuitry with times expressed in nanoseconds (10^{-9} second) rather than microseconds. It was also largely responsible for such innovations in instrumentation as the fractional-nanosecond sampling oscilloscope. The project was of great help to SC&M in developing commercial tunnel diodes.

This rather lengthy historical introduction is given here because many of the early efforts of RCA in computers are not generally known throughout RCA. While RCA was not the first in the commercial exploitation of electronic computers, it was actually a pioneer in the early research work.

THE LABORATORY TODAY

Today the romantic period in which the challenge was to discover "how to do it" is past and so are the last decade's miseries of computers failing every few minutes. Instead, there is a solid $3 billion industry in which RCA has a strong belief and heavy commitment. The competition is severe. Under these circumstances, *what should be the research program of the Computer Laboratory?* The following is a brief account of the goals chosen and of the progress toward their realization.

Memories

The amount and the accessibility of stored information in computers plays the same crucial role as does the signal-to-noise ratio in communications. The characteristic of the memory of a computer determines the capability of the whole system. This is not surprising, since in the universal stored-program computer of today, all information as to *what to do, how to do it,* and *what data to do it on,* is stored in the memory. Every step involves access to the memory. Obviously, large storage capacities and fast access are essential. The trend of the last few years only accentuates the importance of the memory. Invariably it turns out to be easier to simulate almost any logical task by programming within the memory, rather than building special hardware for the purpose. For his patterns the computer architect has no choice but to prefer the stored states of well-ordered cells of the memory rather than some chaotic wiring of physical parts.

As already mentioned, the magnetic core array, resulting from our research of about a decade ago, has provided computers with a really workable memory that is now the mainstay of the art. We believe that equally significant steps in the art are possible by further innovations in memory, which still represents the most important and fertile ground for research. For that reason, a substantial part of our effort is in that field and is likely to continue for a number of years. We are now engaged in work in magnetic, superconductive, and other types of memories.

The storage capacity and the time of access are the main characteristics of memory. These two parameters are plotted in Fig. 7, where the state of commercial ferrite core memories at the beginning of 1962 is illustrated by the crosshatched area. Maximum capacities are a few million bits and minimum access is about ¾ of a microsecond. We have been working to improve upon these limits, as follows:

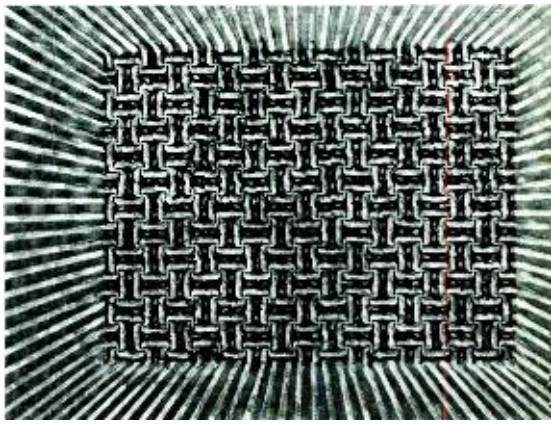
Speed

The speed of a core memory depends strongly on the size of its elements. The smaller the core diameter, the greater is the magnetomotive force due to the maximum drive current possible from a given transistor—and therefore the faster is the switching of the core. Also, the small bit spacings produce corresponding short delays along windings. While a number of other factors must be considered to obtain high speed, miniaturization of the elements is an absolute prerequisite. For that reason we have concentrated our research of the last few years on technologies for making memories with elements drastically smaller than is possible with the conventional molded ring-shaped cores strung on wires.

We have recently worked out a technique for making holes in ferrite by means of electron-beam drilling.[3] Very intense beams of high-energy electrons can produce in microseconds enough heat to sublimate ferrite, even though this ceramic material is very refractory. For example, 1-mil holes can be made quite easily in wafers 10 mils thick. To obtain windings, these small holes are plugged with a conducting paste, the wafer is coated with copper, and a winding is microphotoetched on the two faces of the wafer. A cluster of four holes, each with a single winding, is used and has the effect of four windings through a single hole. The wafers are assembled in a mosaic and the wafer-to-wafer connections for the entire array are completed in a single soldering operation (Fig. 8). Arrays of 16 words of 12 bits each have been operated with a cycle time of 100 nsec. Larger capacity memories would be slower; for example, one with 1024 words would have a cycle time of 150 nsec. This is illustrated on Fig. 7 for the case of a typical word of 64 bits, i.e., a capacity of 65,536 bits. Incidentally, the word length has practically no influence on access time in high-speed word-organized memories.

The Semiconductor and Materials Division, RCA Electronic Data Processing, and the Electron Tube Division worked with the RCA Laboratories on microferrite memories, and have given indispensable assistance in the above project. Concurrently with it, and as a result of it, the SC&M Memory Operation at Needham developed and in mid-

Fig. 8—Mosaic of microferrite wafers; 16 x 12.



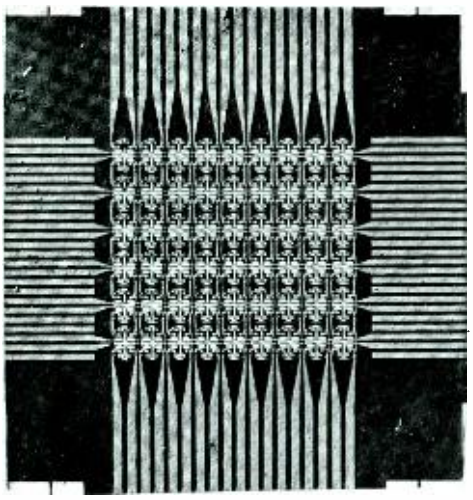


Fig. 9—FLEA memory, about ¾" square.

1962 announced a commercial microferrite memory. This memory has a cycle time of 375 nsec and is the fastest commercially available. A typical memory module may have 256 words of 36 bits each, as illustrated on Fig. 7. The memory is made of cores with 50-mil outside diameter and 10-mil inside diameter, which are metallized on their faces and on the wall of the hole. The cores are mounted on strips and the metallizations are connected so as to produce one winding. Straight wires strung through many parallel strips complete the assembly. This memory represents an important step toward integrated fabrication as only a single hand-threading operation remains.[4,5]

We are presently attempting to develop a microtechnology that provides elements even smaller than those practical with the electron-beam drilling and subsequent microphotoengraved windings, and which at the same time is completely integrated in that a single operation provides elements, windings, and interconnections. We hope thus to both improve performance and lower cost. Promising initial success has been attained.

Storage Capacity

In considering the largest storage capacity attainable in magnetic memories, one could think of the question simply in economic terms. For example, one could obtain a billion-bit memory by buying one thousand conventional memories of one million bits each. Such a memory would cost a good fraction of a billion dollars, but worse yet, the delivery time probably would be very long. This can be appreciated by considering that automatic machines making and wiring elements at the rate of one per second would require more than 30 years to complete a billion-bit memory. It is very unlikely that higher fabrication speeds with obvious parallelings could speed up the present bit-by-bit construction technique by the orders of magnitude required to make it practical. Clearly, batch fabrication or integrated techniques are the real hope.

This hope underlay our work on the apertured ferrite plate mentioned earlier. However, it turned out that the step toward integration, with 256 bits batch fabricated and requiring some hand wiring, has not yet had a great economic impact. More recently, we attempted to take a much larger step by using thin sheets of permalloy. An array of holes is photoengraved in the sheet by a technique similar to that used for the shadow mask of the tri-color cathode ray tube. The sheet is then coated with an insulating layer and a layer of copper. The copper is photoetched to produce winding and connections. The lack of a sufficiently rectangular hysteresis loop and uniformity on the sheet was overcome by the use of miniature transfluxors for each bit, instead of single cores. Sheets with 16 x 8 transfluxors were developed and a stack of 20 was built into the prototype memory (Fig. 9). This prototype, tested by the Surface Communications Division is of interest to the Signal Corps because it can operate in a wide temperature range, typically −70° C to 150° C, owing to the high Curie temperature of the permalloy. Larger sheets can be made, although this would be much easier if materials with better properties were available. At the moment, the ferrite integrated technology alluded to above seems to be more promising. In any case, a vigorous development along either of these two or some other approach is likely to provide the necessary integrated magnetic technology for the practical making of hundreds of millions of elements.

Unfortunately, integration of magnetics alone is not sufficient—the associated electronic circuitry must be integrated as well. It can be estimated that for large capacities, one semiconductor element is required for every 200 magnetic storage elements. This is a conservative estimate; many commercial systems have a greater percentage of circuitry. The several million semiconductor devices required for a billion-bit memory are two to three orders of magnitude more than the number of logic elements in today's largest computers. Thus, it is obvious that the real promise for really large magnetic memories lies in the combined integration of magnetic and semiconductor technologies. It turns out that this is also the best approach to high speed. For these reasons we have started intensive research in this area, and are considering the use of diodes as well as transistors. Some progress has been already achieved. However, it appears that superconductivity may offer an easier road to large capacity memories.

Superconductive Memories

Superconductive phenomena are essentially ideal for computer applications. Persistent supercurrents are a natural form of storage, and sharply defined thresholds between superconductive and normal states permit switching. Moreover, the technology of thin superconductive films offers the unique possibility of simultaneous miniature batch fabrication of storage elements, addressing switches, and all connections. For these reasons, about five years ago we decided to investigate this relatively esoteric phenomenon. We were soon convinced that the cost of cooling to liquid-helium temperatures makes superconductive computer systems of economic interest only if such cost can be spread over a very large number of elements—upwards of millions. On the other hand, as explained above, our magnetic-memory work showed that this was about the limit of nonintegrated magnetic-semiconductor techniques. The conclusions were obvious: work on very-large-capacity superconductive memories, and for computer logic circuits, consider only that work which is necessary in conjunc-

Fig. 10—White room and facilities for superconductive thin film fabrication.

tion with the memory. After a number of relatively complicated arrangements, a solution was found that appears to be the simplest possible: it consists of making only the minimal straight connections of the memory's schematic, and obtaining the necessary storing and switching devices incidentally, as it were, along the connections. The principle is briefly as follows.

Two perpendicular sets of parallel. suitably insulated lead strips are evaporated on top of a continuous film of tin. When an x and y strip carry a current I, the magnetic field pattern at their intersection is at 45° with respect to the strips. The intensity of the field is maximum at the intersection and diminishes gradually with distance. Consequently, there is a sharply defined region within which the field in the tin sheet exceeds a critical value and renders the sheet normal, and outside of which it does not. Within that region, it is possible to induce persistent supercurrents and change the polarity of previously induced persistent supercurrents. The final polarity obtained depends on the polarity of the primary driving currents and determines whether a one or a zero is stored. An element is switched only if the primary excitation is opposite to that which previously established its state, and only if it exceeds a certain definite threshold. The situation is thus quite analogous to that of a hysteretic magnetic element with a perfect square loop. A voltage is induced in a sense winding on the opposite side of the memory plane. No magnetic fields leak through the superconductive memory plane, other than at the selected location, because it is a perfect magnetic shield; thus, there are no disturb signals caused by half excitations.

To address the memory, the drive currents x and y are steered to the selected lines by a network of cryotrons. A *cryotron* is a superconductive gate, described by Dudley Buck in 1956, which depends on the fact that a normal resistive path can be established in a superconductive strip if a sufficiently high current is passed on a superimposed strip. In the selecting networks, the cryotrons are arranged in trees, and at every bifurcation one of the cryotrons is resistive and the other superconductive according to the value of the corresponding binary address bit. The currents are steered through the only completely superconductive path to the desired memory line.

We plan to use the superconductive memory in a semiconductor computer. The drivers for the cryotrons, the sense circuits, and the write and rewrite circuits are of the conventional transistor type. Here, however, in contrast to magnetic memories, the number of circuits and components increase only very moderately with capacity.

Thus far, the progress has consisted mostly of the necessary groundwork: theoretical understanding of all effects and mastery of the thin-film technology. Most samples were made on early experimental vacuum evaporating systems, but systems with a greater degree of control and automation were built in cooperation with SC&M. Also, a special "white room" was built (Fig. 10). The proper functioning of the continuous-sheet memory itself was proven in 10 x 10 and 4 x 4 arrays and signals with 30:1 discrimination were obtained. The cryotrons were tested. A plane with 128 x 128 = 16,384 bits and 508 cryotrons was also built (Fig. 11). The tester for this plane uses electronic circuitry built by EDP. It is hoped that the cycle time will be only one or two microseconds.

Content-Addressable and Read-Only Memories

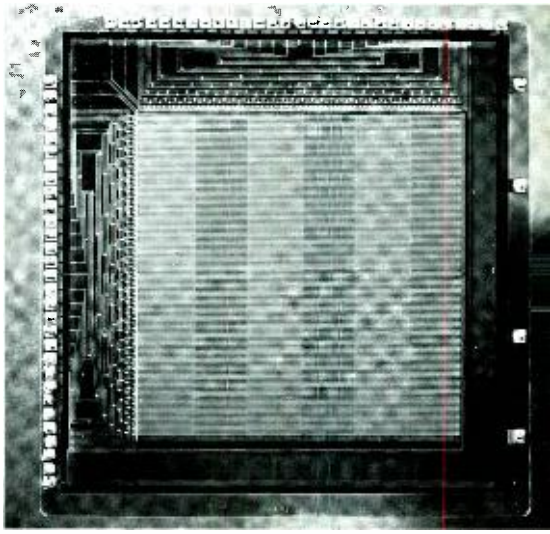
In addition to our efforts to increase the speed and the storage capacity of random access memories, we are also investigating memories with more generalized means of access. When a computer is put to the task of ordering, merging, sorting, and collating information, it does so today by serially examining every word stored in its memory. This is a slow process even with very fast memories. If it were possible to address the memory through the content of part of the information itself and retrieve the remaining part associated with it, these tasks and many others could be done much faster. Such memories are called *content addressable*, *associative*, or *search* memories. The essential of content addressability is to compare simultaneously a given word with all words of the memory and to detect perfect match wherever it occurs. The matching signal provides the location and identification of the associated information. This requires the mixing of logic with storage functions in the storing array itself. Because a content-addressable memory is likely to be the most useful when it has a large storage capacity, its realization presents technological problems akin to those of a large random-access memory, only somewhat more difficult. Therefore, we consider it to be a natural future development following the work toward large capacity *per se*. Nevertheless, we have some research in the field to establish the special logic of switching and methods for using such memories. For example, nondestructive read-out of the storing element is essential, as all bits of the memory must be sensed simultaneously and could not be all rewritten by any sensible amount of electronics. We have found ways to use arrays of transfluxors which are, of course, nondestructive read-out devices. Also, we have conceived very simple modifications of the continuous-sheet superconductive memory to obtain nondestructive and content-addressable memories.

To complete the account of our work on memories, mention must be made of fixed, or *read-only*, memories, of which the resistive matrix of the war years was a very early precursor. Today, we are considering two types: One consists of condensers arrayed in patterns and driven by tunnel diode circuitry. This can be considered as an integral part of the logic of a very fast computer. The other is an attempt to make highly modularized fixed memories which could be used in indexing for information retrieval and, in general, in dealing with tabular data.

Logic Switching Circuits

Increased speed in computers has yielded great returns throughout the short history of the art, as the effective computation speed went up by a factor much greater than the cost, and the computer could attack ever more ambitious tasks. The five-year Navy-sponsored project mentioned earlier has pushed speed almost to its goal of 1000 Mc, momentarily beyond economic profitability, but ultimately only a step toward the profitability of even higher speeds. These may be attained by optical techniques opened by such new developments as the electronically controlled gallium arsenide lasers, fiber optics, and new concepts for optical computers. We have started a modest exploration toward this far-reaching possibility. We are also studying limits to speed imposed by fundamental physical constraints through the analysis of the energy of

Fig. 11—Cryoelectric memory planes with 128 by 128 = 16,384 bits, and 508 cryotrons. Class Plate is 2" x 2".



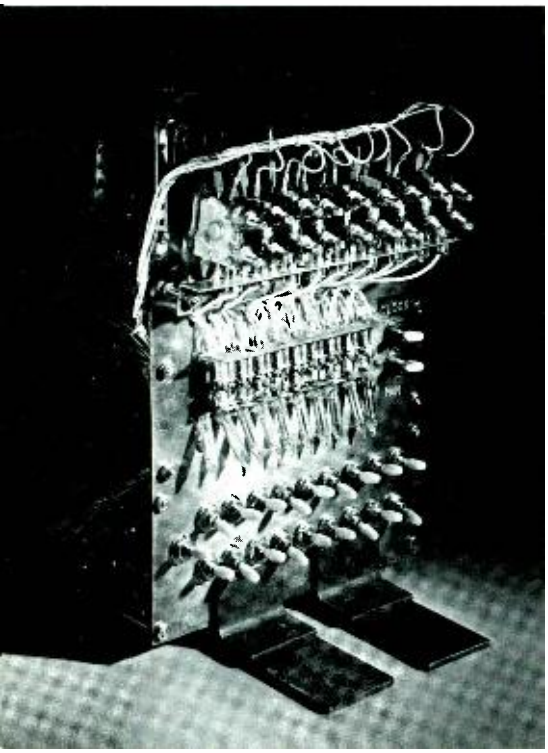


Fig. 12—Nine-stage adder carry circuits; tunnel diodes and transistors.

information-carrying energy in computer networks.

Of more immediate importance is our work with transistor and tunnel-diode circuits which, though somewhat slower, at about 200 Mc, have much wider margins of operation than the pure tunnel-diode circuits of the project just mentioned. Some of the principles of these circuits have been adopted for VANGUARD by the Advanced Development Laboratory of EDP and DEP Applied Research. Among them is a particularly simple and effective parallel adder, in which the carries are propagated from the least to the most significant position by a string of tunnel-diode gates. The propagation depends only on the properties of the tunnel diodes and is, therefore, very fast. Input and output to the tunnel-diode carry chain is by means of transistors which provide the necessary gain and whose somewhat slower response does not appreciably affect the speed of the adder, since it is not cumulative along the string. The nine-stage carry chain shown in Fig. 12 has operated with an average delay of only 0.3 nsec per stage. A 50-bit word length would entail a delay time of only 15 nsec.

The recent advances of integrated semiconductor technology may be a boon to still higher speeds. More likely, it may pave the way to the use of lavish numbers of somewhat slower components and avert the long trend toward the ever-more-efficient use of a few ultra-fast ones. The Computer Laboratory is considering some of the many problems posed by this intriguing possibility. It is not presently involved with the integration technology itself, for which it depends on the Electronic Research Laboratory and SC&M. Integrated technology is best at providing dense arrays of nearly identical elements such as thin-film or metallic-oxide unipolar transistors. To make specific logic networks out of such arrays, we are investigating the use of interspersed photoelements so that any desired microconnection pattern can be obtained optically. Also, we are considering means to tolerate defective elements in large arrays, a condition essential for obtaining reasonable production yields. This is achieved through the redundant use of several elements to do the switching possible with only one.

While we are deferring a substantial effort in superconductive logic elements in favor of large-capacity memories according to a research strategy mentioned before, we have a continuing fundamental effort relating to cryoelectric devices. In addition to computer logic circuits, we are considering the problem of amplifying very small signals. We are exploring various approaches to the problem including superconductive tunneling and magnetic control. The latter method has yielded very promising results and may provide low-noise amplification at microwave frequencies.

Input-Output Devices

The advent of the electronic computer was greatly facilitated by previous developments in typing, recording, and printing of digital data. This inheritance includes punched cards, punched tapes, the magnetic tape, electric typewriters, electric printers, films, and even electronic photography. All of these are electromechanical and originally did not attract as much research interest as the electronic computer itself, the *sine qua non* of the whole system. But today, the emphasis is changing *because the central computer is no longer the bottleneck*, and the input and output devices, which are the interface between man-and-machine, play a dominant role in the extent and convenience of usage.

At the RCA Laboratories, there are a number of projects in the area. In the Acoustic and Electromechanical Laboratory there is work with magnetic recording, high-speed printing, Electrofax, and the phonetic typewriter. In the Computer Research Laboratory there are three projects; large and fixed memories, character recognition, and displays.

The work in large and fixed memories described previously is cited here because these devices are intended to make unnecessary today's use of tapes for auxiliary memory. The tapes are excellent input-output devices and excellent records for dead storage. But their use as auxiliary memories, with fast stop-go mechanisms, is a costly artificiality and a source of much grief in computer maintenance.

The objective of our work in character recognition is to develop the logical principles of a reading machine which can tolerate changes in style — i.e. changes in the font (style or size of typography) and imperfections in printing. Such logic was developed by experimental simulating procedures on a general-purpose computer. Recognition is accomplished by detecting sequentially a set of geometric character features which tend to be independent of type style and printing imperfections. This logic was of help in the design of optical character-recognition machines being worked on by EDP. It is hoped that a relatively simple machine, consisting mostly of a fixed memory containing all the required recognition logic, can be built to recognize characters at rates of 100 characters per second or greater. The design of such a machine was simulated on a large general-purpose computer.

Electronic displays of numerals, letters, and graphs, is an important form of computer output. Furthermore, the problem of a flat display such as mural television is akin to that of a computer memory. There must be rapid access to many elements and each element must have storing properties. The difference is, of course, that the elements must emit or control light in the display but only provide an electric signal to a common circuit in the memory. Computer memory techniques were applied to this problem and published in 1957, as was mentioned, and resulted in a transfluxor controlled electroluminescent display. A similar application was started recently. It is based on a ferroelectric equivalent of the transfluxor, the *transcharger*, which may overcome the complexity in construction and excessive power requirements of the otherwise promising earlier approach. Some success has been obtained with various transchargers made of newly improved ferroelectric materials.

Computer Theory

The physical makeup of computers can still be improved enormously. The majority of our activities are aimed at order of magnitude increases in storage capacity and computer speed, drastic cost reductions, and better inputs and outputs. However, we realized several years ago that great strides are needed in design efficiency, organization and application of computers, and that in the not-too-distant future the really important

progress may be possible only in this field. We have started a theoretical group which has grown gradually and now has an important research program. The program includes studies in *switching theory*, in *system analysis*, and in *artificial intelligence*.

Switching theory is aimed at providing a systematic basis for efficient computer logic and circuit design. Two areas have been studied: threshold logic and reliability of networks. A theory was developed which deals with the threshold gate in much the same fashion that conventional switching theory deals with *and, or* or *nor* gates. General theorems were established and applied to specific problems. For example, taking the simplest significant three-input threshold gate (the majority gate), ways to realize all three-input switching functions have been systematized. This theory has also provided insight into a class of proposed adaptive machines based on methods of variable-parameter threshold devices. With respect to the reliability of switching networks, our approach has been the introduction of redundancy at the element level. By using three elements instead of one, and then triplets of triplets, etc., we showed that such a recursive network is in fact efficient in redundancy, although it requires many elements. It is the only way we know to build reliable equipment from really poor components. Other schemes of redundancy are being investigated.

In system analysis, we are concentrating on the problem of developing mathematical criteria for adaptive systems. In systems having a finite number of possible discrete states, the feedback arrangements customary in simple analog systems are not possible. The main problem consists of finding the decision criteria making it possible to jump from any given state of the system to another so that the system progresses toward some desired goal. The mathematical theory of Markov chains, which are ordered series of states each being derivable from its predecessor, is the basis of our study. A number of mathematical inventions have been made beyond the known classical theory, and several concepts have been developed which make it convenient to have an insight on this difficult problem.

Artificial intelligence (a connotation now gaining acceptance) describes a growing activity aimed at mechanizing certain intellectual processes commonly used by people in devising solutions to problems. Such processes involve heuristic methods where guesses, hunches, trial and error, etc. are used. Work in this area is expected to broaden the use of computers to problems for which either a systematic solution procedure does not exist, or if it does exist, is too cumbersome to be of any real value. We are studying the question of automatic problem-solving by attempting to develop procedures that construct simple proofs to theorems in the propositional calculus. This problem, with its simple known formalism, enabled us to work out a general framework for problem-solving procedures. We are also working on the possibility of automatically forming a theory on the basis of examples. Here, we are searching for the proper general program for a computer from which specific programs could be constructed so that an unknown problem would be solved on the basis of a number of given similar solved problems. In general, we found that the subjects of automatic theory formation and problem solving are closely related. Considerable progress in both was recently realized.

In computer theory, we are working in fields which may be considered to be at the opposite ends of a spectrum: on one hand, the theory of building the elementary parts of today's machines, and on the other the possibility of extensions to endeavors which require the conception of new computation schemes and also of new relevant mathematics. In the middle of this spectrum is the large field of the practitioner of computer design and utilization centered on the problems of machine organization and programing. Developments in machine organization and in programing languages and their processors are closely related. They are extremely important and constitute a large activity throughout the country. Machine designers and users that are close to the logic and economics of specific applications are best qualified to establish the requirements and to propose solutions in these areas. We have directed our research in theory of computers to general design principles and to new schemes for extended future applications, rather than the working out of specific machine or software designs. This is consistent with our work on the physical aspects of computers, where we tend to look at new principles rather than build improvements of well-known solutions. For these reasons, we have limited our efforts in machine architecture and software to cooperation with EDP. We plan to enlarge our activity in this field.

CONCLUSIONS

The traditional task of electronics is confined to the faithful transmission of information in space and time. The advent of computers changed this radically. The job is now to combine and cause the interaction of signals so as to create new signals which explicitly represent their useful content. Viewed in this sense, the art of electronics has acquired a new breadth and started on a path even more inspiring than that entered upon by its early pioneers.

Electronic computers have already made a tremendous impact wherever lengthy routine tasks were sufficiently systematized to be ready for rapid automation. These are the well known business applications to general accounting, to insurance, to transportation reservations, to payroll, to inventory control, etc. Of similar importance were, of course, scientific applications which gave birth to the art. Space travel is inconceivable without computers, and so are numerous military systems. The list of new fields could be continued to cover weather predictions, medical electronics, traffic control, management control, automation and many others. These applications are well known, and have already had a great impact on our lives.

Less known perhaps, but of even greater importance, is a revolution in our thinking. No longer is it necessary to confine ourselves to simple thought-patterns striving for economy of manipulative steps. We can now contemplate arbitrarily large numbers of manipulations and thereby handle usefully almost any problem we desire. There hardly seems any intellectual endeavor which is not being profoundly re-examined because of this possibility. Universities and even high schools are bringing computers into their regular curricula, and applied mathematics is permeating all science.

Speaking for myself, I have to admit, along with most early workers in the field, that our wildest dreams of the formative years did not envisage the great developments which have already occurred, and even less the promise of the foreseeable future.

The impact of computers can be expressed more pragmatically in terms of dollars. The electronic data processing industry in 1962 was a business of $2.8 billion, and it is believed that it will reach $3.5 billion in 1963. We believe that RCA must and will play a leading role in this business. The Computer Research Laboratory is striving to help RCA in this leadership.

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FIVE YEARS OF PROGRESS ... A Review of RCA Electronic Data Processing Product Engineering

The last five years have been very significant technically in the engineering of RCA product-line computer systems. This paper reviews those technical landmarks and provides an over-all view of the present product-line state of the art in RCA Electronic Data Processing Engineering.

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J. N. MARSHALL graduated from Cambridge University, U.K., with an Honors Degree in Mathematics and Physics in 1939. He then worked on rapid-scanning radar and identification at the R.A.F. Research Establishment. In 1943, he was assigned to the U.S. Naval Research Laboratory as project engineer on RF test equipment and check-out systems for a radar identification system. With RCA since 1946, he has been project engineer on part of the Teleran Air Navigation System and a Target Designation System for the Navy. As Mgr., Advanced Development, for Commercial Electronic Products, he supervised development of a computer, a complex telemetering system, and industrial instrumentation of various types. Since joining EDP four years ago, Mr. Marshall has headed up development engineering groups on industrial computer applications and ultra-high-speed computers. He is now Mgr. of Computer Advanced Development, reporting to C. A. Gunther, Vice President of Technical Programs for EDP and DEP. He is an IEEE Member and has several U.S. Patents.

TWO MILESTONES were passed by RCA Electronic Data Processing late in 1962: *the first* RCA 601 computer was delivered to New Jersey Bell Telephone Company; and *the first* Air Force DATA-COM (Phase I, COMLOGNET) installation containing two Communication Data Processors (CDP's) was accepted by the Air Force.

The RCA 601 and the CDP are large computers with 5×10^5 to 1.5×10^6 bits of memory capacity operating at a 1.5-μsec cycle, a long word length of 56 bits, and an unusual flexibility of instruction handling, both word and character. They are the most powerful machines designed for data processing and are exceeded in size and capability only by the very largest scientific machines, such as STRETCH and LARC. These achievements make RCA a *full-line supplier* of EDP equipment.

EARLY COMMERCIAL COMPUTERS

The delivery of the first RCA 501 system in 1958 was the start of RCA's large-scale entry into the data processing field. Prior to that, the delivery of five BIZMAC systems represented an enormous engineering achievement, and provided an education in marketing, planning, programming, and fabrication which made the RCA 501 possible. But it is these last five years that have seen EDP mature. A wide variety of products were introduced between the RCA 501 and 601, of which the RCA 301 was unquestionably the most important. Approximately 300 RCA computing systems are now in the field and 100 systems are on order; in addition to RCA's computers going to external customer applications, the various divisions of RCA are making good use of EDP's commercial computer designs (see Table I).

This five-year period can be considered as a first full cycle for RCA, and makes it suitable at this time to review what has happened technically during this period.

ON-LINE OPERATION

One of the features of the RCA 501 was its capability to operate printers *on line* without use of tape as an intermediary. A simultaneous mode was provided in which an input or output instruction could be held and operated as required at the relatively slow rate of the peripheral devices; at the same time, computing instructions were executed in the normal mode, and only interrupted when the memory was actually needed for transfers to and from peripheral equipment. Tape read or write could be performed simultaneously with computation, or the computer could be assigned to operate the printer essentially whole-time with a limited amount of editing. This welcomed innovation permitted an improvement in sorting and merging functions on tape and avoided the high cost of the electronics in existing off-line printer equipment.

More sophisticated solutions for operating multiple peripheral equipment have since been developed. The improvements in techniques to maximize the utilization of peripheral equipment, and to work on-line to multiple communication channels or data sensors, are important areas of present development.

The RCA 301 control units[1] permit (with some restrictions) the use of simultaneous modes by different peripheral equipment alternately, provided they do not use too large a percentage of the memory cycles all together. In this way, more than one simultaneous function is possible. Recently, a control unit for multiple communication channels has been added which can receive or transmit on 80 telegraph channels. The *Communications Mode Control* (CMC-80) samples single-channel buffers on each line and loads or empties them to the memory as required. The memory addresses are decided by the count in the sampling mechanism so that each transfer automatically occurs to (or from) the memory without need for any routine to find the appropriate address. Block transfers are then arranged between the general work areas of the memory and this staging area which directly transfers data to the CMC-80. A system using the CMC-80 and RCA 301 provides immediate connection to *Electronic Data Gathering Equipment* (EDGE) units installed at a Lockheed plant in California.

The RCA 110 control computer[2] includes another feature in that any input device such as a pressure or temperature sensor could automatically interrupt the computer and go to a specialized subroutine, without any input-output instruction having appeared internally. These interrupts have five levels of priority so that, for example, alarm warnings can take top priority. Those interrupts set flip-flops which are sensed automatically by the computer between instructions.

The RCA 601[3] has a sophisticated scheme of this kind which permits running multiple input-output functions up to a level set by the individual speed-weight ratios of the functions. Memory interlocks are provided so that input-output routines, or simultaneous computing routines cannot have access to the wrong areas and damage information belonging to other programs.

The RCA 4101 military computer[4] also has a priority-interrupt scheme and multiple simultaneous operations.

The problem is to minimize the hardware required for buffers and storing of alternate addresses, instructions, etc.,

TABLE I—RCA 301 and 501 Computer Installations at RCA Locations

RCA VICTOR HOME INSTRUMENTS DIV., INDPLS., IND.
RCA 501; RCA 301
Warehousing & Shipping
Analysis of Finished Goods
General Accounting
Quality Control
Value Analysis
Parts Scheduling
Sales Planning
Payroll
Operations Research
Production Control

NATIONAL BROADCASTING CO., NEW YORK CITY, N.Y.
RCA 301
Payroll
General Accounting
Station Time Billing
Station Switching
Cost Accounting

RCA SERVICE CO., CHICAGO, ILL.
RCA 301; RCA 501
Demand Deposit
Bank MICR Check Sorting
Payrolls
Subscription Fulfillment
Reader Inquiry Service
Mailing List Maintenance
Broker Accounting
Bookkeeping Service
Test Scoring and Analysis
Records and Statistics

RCA SERVICE CO. (FINANCIAL) CHERRY HILL, N.J.
RCA 501
General Accounting
Gross Margin Reporting
Demand Service
Contract Fulfillment
Payroll
Physical Inventory

RCA SERVICE CO., WASHINGTON, D.C.
RCA 501
Demand Deposit
Payrolls
Subscription Fulfillment
Reader Inquiry Service
Mailing List Maintenance
Broker Accounting
Bookkeeping Service
Government Statistics
Service Billing
Federal Credit Union Accounting
International Trade Statistics
Test Scoring & Analysis
Records & Statistics

ELECTRON TUBE DIV., HARRISON, N.J.
RCA 301; RCA 501
Sales Reporting
Profitability of Items
Gross Margin Records
Financial Planning
Factory Loading
Quality Control
Statistical Reporting
Sales Reporting
Financial Reporting
Inventory Control
Central Billing

RCA COMMUNICATIONS, INC., NEW YORK CITY, N.Y.
RCA 501
Billing
Communications Statistics
General Accounting
Payroll
Traffic Bureau Statistics
Accounts Receivable
FCC Statistics
Foreign Message Recording

RCA SERVICE CO., CHERRY HILL, N.J.
RCA 501
Demand Deposit
Payrolls
Reader Inquiry Service
Broker Accounting
Government Statistics
Subscription Fulfillment
Mailing List Maintenance
Bookkeeping Service
Stock Transfers

RCA SERVICE CO., SAN FRANCISCO, CALIF.
RCA 501
Demand Deposit
Savings Accounting
Payrolls
Billing and Accounts
Subscription Fulfillment
Reader Inquiry Service
Mailing List Maintenance
Property Title Records

ELECTRON TUBE DIV., LANCASTER, PA.
RCA 301
Payroll
Marketing Analysis
Factory Loading
Material Control
Cost Standard
Life Test

DEFENSE ELECTRONICS PRODUCTS, CAMDEN & MOORESTOWN
RCA 501 in Moorestown; Two RCA 501 in Camden
Payroll
Material Operations
MINUTEMAN Project
Quality Control

DATA SYSTEMS DIV., DEP, VAN NUYS, CALIF.
RCA 301
Engineering Simulation
General Accounting
Payroll
Purchasing

DATA SYSTEMS DIV., DEP, BETHESDA, MARYLAND
RCA 301
Information Retrieval
Equipment Design
Research New Techniques
Data Reduction
Engineering Evaluations

ASTRO ELECTRONICS, DEP, HIGHTSTOWN, N.J.
RCA 501
Scientific Simulation
Information Retrieval
BMEWS Point-to-Point Contact
Scientific Space Calculations
Data Reduction

RCA RECORD DIV., INDIANAPOLIS, IND.
RCA 301
Distribution & Warehousing
Production Control
Material Control
General Accounting

RCA SERVICE CO. (TRAINING) CHERRY HILL, N.J.
RCA 301
Maintenance Engr. Training

EDP, NEW YORK SERVICE CENTER, N.Y.C., N.Y.
Two RCA 501
Brokerage Service
Savings Accounting
Subscription Fulfillment
Mailing List Maintenance
Property Title Records
Demand Deposit
Payrolls
Reader Inquiry Service
Billing and Accounts

EDP, CHERRY HILL DATA CENTER, CHERRY HILL, N.J.
RCA 501; Two RCA 301
Customer Support
Payroll
Programming Support
Sales Demonstrations

Note: RCA 301, 501, and 601 computer installations are also located at RCA plants in West Palm Beach, Fla., Camden, N.J. and Pennsauken, N.J. These installations are primarily used for engineering design and development techniques, rather than the commercial-type computer uses shown above.

and still provide a break-in on interrupt, to indicate completion of a read-in cycle and provide lock-outs for memory. At the same time, maximum performance is required in terms of using a minimum number of memory cycles for servicing input or output. For a data-processing machine, elegant solutions in this area are more important than arithmetic capability.

PROGRAMMABILITY

The RCA 501 was the first machine to be designed after a real programming capability had been developed in RCA. Its specification was determined by a team of programmers and logic designers working together to explore trade-offs between hardware costs and program convenience, and to design a machine that fits neatly together.

The RCA 501, unlike the BIZMAC machines, had no drum. The drum had been used to provide program storage at reduced cost, and instructions were surged into the core memory in groups of 64 in order to be executed. Part of the reason was the reduced cost of core memories, but more important was the view that the automatic programming techniques then envisaged would be severely complicated by two levels of storage.

Automatic programming—the use of the computer to convert a program written in simplified form to detailed machine language—was already well developed for scientific applications. Assembly routines using simplified instruction formats (corresponding to one or two machine instructions) and assigning memory locations for data were in general use. Algebraic compilers, such as FORTRAN, took convenient mathematical statements (not simply related to machine instruction) and constructed programs to execute them. However, there were no sophisticated business compilers such as the *Common Business Oriented Language* (COBOL) which was first used by RCA and Univac in 1960.

An alternate form of automatic programming, first thoroughly developed at Bell Laboratories, is the *interpreter*. This type of program is initially developed in a convenient language (such as algebraic forms in scientific work) and then interpreted by routines stored in the computer's memory. This is inefficient in terms of time to do the job on a computer and wastes memory space. However, as it involves no previous compiling time, it is economical for single-shot jobs and is widely used for engineering purposes.

An ideal computer would interpret from instructions in natural language, with an efficiency in performance equal to compiled programs. Attempts are now being made in this direction. An example is the English Electric KDF9 which uses push-down memories to provide powerful arithmetic functions fitting well with an algebraic notation called *Reverse Polish* in which a sequence of data symbols and operators describe the arithmetic functions to be performed.

In business data processing, it has so far appeared that a good data processor is automatically good at compiling and convenient to compile for. There has not been a major effort to design machines performing more of the automatic programming in the hardware. This relation will, however, become more important in the future and machines using instructions in natural language directly are a possibility.

CHARACTERS AND WORDS

Important to RCA was the introduction of variable word length in BIZMAC, where data was handled character-by-character and symbols were used to designate item and message separation. This organization of data had proved

convenient for business users. It was important in conserving tape, since data was packed tightly without spaces or zeros to fill out standard word lengths. It also saved programming effort in that the symbols could automatically complete instructions and complicated multiple precision arrangements were avoided since there was no fixed word to overflow. It was adopted by other manufacturers (the best confirmation) and included in the RCA 501.

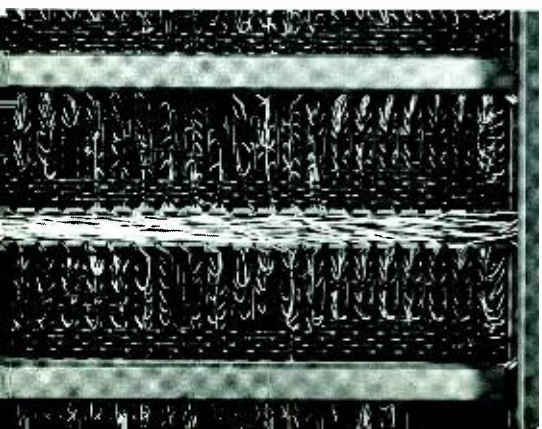
However, character-by-character operation is slow and in one place in particular, the reading of instructions from memory, was too great a restriction. The RCA 501, therefore, reads four characters (28 bits) at a time from a 28-bit-deep memory and staticizes instructions (8 characters or 56 bits) in two reads. This feature was also adopted for data transfers, which take place in *tetrads*, (four characters at a time). The RCA 501 therefore has fixed-word features—so does the RCA 301, but being a small machine, it staticizes and transfers two characters at a time.

Though the earliest electronic computers were serial decimal, machines which were designed for high-speed arithmetic functions have been parallel-binary fixed-word-length ever since the early 1950's. At the end of the 1950's, machines of this type appeared with the ability to address parts of words by additional bits on the address, and thus had some character-by-character capability and adaptability to variable word length. Some machines were also built using parallel-decimal operation, such as the *Livermore Atomic Reactor Computer* (LARC) and the IBM 7074. The 7074 has capability for handling 10 decimal digits in parallel, as well as character-by-character operations.

The RCA 601 is a sophisticated composite machine having both fixed-word and variable-word character-by-character operations. It can address either words or any fraction of a word, such as a character, and can operate character-by-character with either symbol control to indicate the end of a variable-length word, or a fixed number of characters not necessarily forming a number of complete words. It also has variable instruction length. It has built-in arithmetic capability which treats the 56-bit word as 8 decimal digits operated on in parallel; it can also operate character serially. The RCA 604 high-speed arithmetic unit, an attachment for the processor in the RCA 601 system, provides parallel binary and decimal floating-point operations.

What was a direct choice between fixed- and variable-word machines in the BIZMAC days has become a complex issue of internal organization, and a three-way problem between programming convenience, complexity and speed. The RCA 601 to a considerable extent achieves the best of both worlds, but it has not been determined how to accomplish this in smaller machines.

Fig. 1—This photo of the RCA-501 back-panel wiring is an example of neat, clean, business-like wiring by use of panduits.



COMPUTER HARDWARE

One of the problems in the early days of the RCA 501 development was to decide between transistors for logic circuits and a variety of pulse and AC-driven magnetic circuits. The appeal of the magnetic circuits was reliability. It took a full-scale study of a magnetic computer on a government contract to show that magnetic circuits driven by a 100-kc sine wave permitted the transit of only one logic stage in each half cycle (5 μsec); in contrast, transistor circuits using a 200-kc clock could transit through five to ten logic layers in the 5 μsec of a single time-slot, and were therefore five to ten times faster. Today, with stage or pair delay a standard parameter, this would be more quickly recognized. It also turned out that magnetic circuits needed about ten diodes per gate to operate at this speed—this undermined the reliability argument. At intervals during the RCA 501 development, rumors were received that a competitor had fast, simple, cheap and reliable magnetic circuits, and the issue came up for discussion. One of the arguments for transistors was their broad application in non-computer applications to ensure low device cost and good reliability as a result of the high volume and the resultant funds for development and design.

The RCA 501 was the first large transistorized computer to be delivered to a customer. We have no cause to regret the decision to transistorize. The reliability has indeed turned out to be excellent even though we can now design circuits with much better margins than were then possible. Within a year of the first delivery, it was apparent that transistor failure would not be an important source of system downtime; in fact, the lifetime maintenance cost of a transistor circuit was not more than 10% of its original cost.

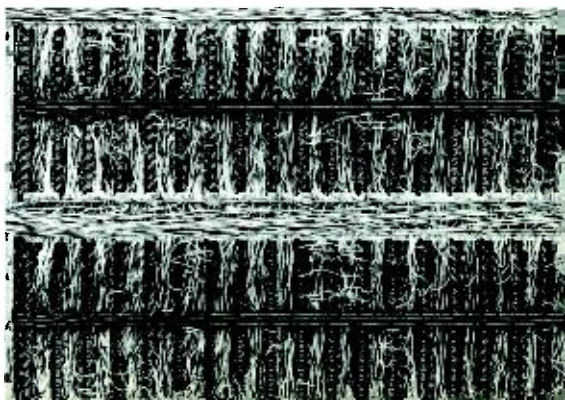
When transistors were first used, there was some interest in point-contact units because of their higher speed; there was no real belief that junction transistors would ever be as fast as tubes. The junction units were preferred because of reliability. Within a few years, the RCA 601 circuits appeared with 50-nsec stage delays instead of the 500 nsec of the RCA 501 circuits; these were as fast as any tube circuits ever built. As far as the author knows, this was the carry propagation circuit in the IBM 704 with the identical 50-nsec stage delay. Now, we can see another improvement factor of ten with transistors. These improvements will be a major factor in increasing computer performance. The cost of transistor circuits is now 25 to 30% that of the tube circuits of 1957.

The RCA 501 memory problem was to transistorize all associated circuits. The magnetic core stack is only slightly changed from the BIZMAC stack and operates at essentially the same speed. The combination of high current, speed, and back voltage required in memory drivers was a real problem for the devices. The prototype RCA 501 went into test with a tube-driven memory built as an insurance program, just because of these difficulties. Yet, in a few short years, the RCA 601 memory appeared at ten times the speed (1.5- instead of 15-μsec cycle time). Even in the RCA 301, where cost was the prime factor, the memory operates at 7 μsec.

INTERCONNECTIONS

One area which has rapidly grown in importance since the RCA 501 design, is interconnections. In BIZMAC days, signal wires were on stringers and were separated by about an inch to reduce capacity coupling which was a problem in the high impedance tube circuits. Transistor circuits are lower impedance and tests indicated that signal wires could be bundled together without undesirable levels of cross-talk. This turned out to be justified in all cases except the

Fig. 2—Higher speeds and advanced programming needs have created increased wiring densities as shown in this photo of the RCA-601 back-panel wiring.



long cables to the memory where coax had to be used. The placement of wires in *panduit* or covered slots (instead of using harnesses) made the signal wiring of the RCA 501 (Fig. 1) much simpler than BIZMAC. Unfortunately, increasing speed and decreasing size of modules are again making this problem increasingly difficult. The RCA 601 and future faster computers must use some kind of transmission line, twisted pair or coax, for all but the shortest connections (Fig. 2).

The first BIZMAC installation used 30,000 tubes, and since each tube had an eight-pin socket, and was also on a plug-in board, there were about 350,000 spring contacts. This received careful attention but it was never a major reliability problem. The lower voltages and higher currents of transistors made this a more difficult problem even though transistors were soldered into circuits. A much greater effort went into the plug and socket; but by careful design and the use of gold plating, successful results were achieved.

For new machines, the interconnections and fabrication scheme are a major problem. The increasing number of circuits on a board has led to serious problems in controlling the number of different types of boards. The logic designer is deeply involved in questions of board types, wiring rules and physical layout. A whole new area of expert knowledge has developed about the problems of wire, contacts and circuit assembly. It involves the physics, metallurgy, and chemistry of the devices themselves, the radiation and propagation properties of assemblies, and immensely complicated organizational problems in machine layout. It is an area where computer assistance to design can be of great importance. Under the title of *packaging*, which is not a suitably romantic title, a whole new skill is growing up.

The problem of interconnections has also become important in memories where the ringing of a stack structure following application of a drive pulse is a major source of noise, reducing operating margins and limiting speed of operation. It is controlled by the physical arrangement of wires and ground planes.

PERIPHERAL EQUIPMENT

The problems of peripheral equipment (reliability of tape recording, tape and head wear, card jams, print quality, and printer reliability) are old, and antedate the RCA 501. However, we are presently solving these problems at a different performance level. Tape-recording speeds went to 33 kc with the RCA 501, (BIZMAC II was 16.7 kc) and are now going to 120 kc, though the mechanisms have an obvious family resemblance. An enormous amount of work on recording techniques, tape guiding, error control, tape quality, head design, and many other areas has made possible this increase in performance.

Recording techniques have changed substantially. The RCA 501 tape station used pulse recording and the key problems of the day were eliminating crosstalk in heads and obtaining tape with few dropouts. The crosstalk problem is now relatively well controlled. Present stations use non-return-to-zero recording at much higher densities. The key head problem is *gap-scatter*—the variation in the position of effective magnetic gap. Tape quality and dropouts are still very much of a problem, and tape testing and qualifying is an important field.

The RCA 501 printer produced 600 lines/min; now 1000 lines/min is standard. The quality is much improved and the alignment and uniformity of characters of the 1958 printer would not be acceptable today. We also read and punch cards at 600/min and 200/min, instead of 400/min and 150/min.

THE NEXT FIVE YEARS

With all these changes in performance, the nature of the problems has changed to a lesser degree. The revolution in peripheral equipment is just coming after a phase of consolidation and squeezing the most out of the available techniques. Optical character recognition, mass memories with the capacity of tape and access times below a second, broader use of on-line communications to remote points, and multiple inputs using EDGE and similar equipment are becoming major factors. The next five years are likely to see a radical new and advanced group of peripheral equipments, just as the RCA 501, 301, and 601 were radically different and better than the BIZMAC generation which preceded them.

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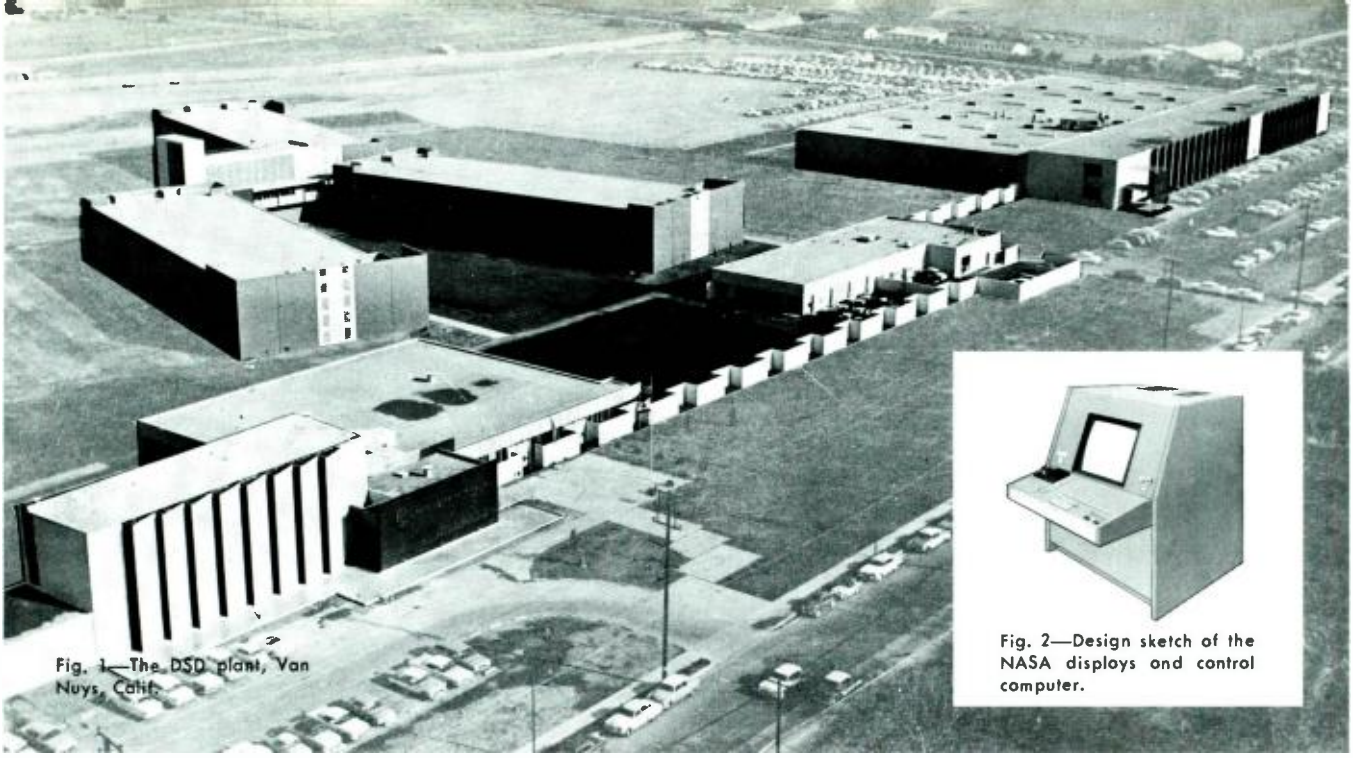

Fig. 1—The DSD plant, Van Nuys, Calif.

Fig. 2—Design sketch of the NASA displays and control computer.

PRODUCT TRENDS IN THE DEP DATA SYSTEMS DIVISION

Reviewed here are current product-engineering activities of the Data Systems Division of Defense Electronic Products, along with some market trends and plans. DSD, which grew from an original 500 personnel in 1959 to 2000 in 1962, now operates in two locations: the headquarters facility in Van Nuys, California, and at its Data Systems Center in Bethesda, Maryland.

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and
D. J. PIZZICARA, Staff Engineer
Data Systems Division
DEP, Van Nuys, California

THE DATA SYSTEMS Division of Defense Electronic Products is an integrated organization of 2000 people devoted to the data processing and display business. Its basic mission is to pioneer advances in the data arts and carry them to the product-line stage—both individual equipments and total systems.

Some idea of the economic challenge of data processing may be gauged from the national rate of expenditure. Total government and business expenditures for 1962 are in excess of a $2 billion rate, nearly 1/200 of the gross national product. Projections indicate an increase to a rate between $4 billion and $7 billion by 1970. This would place data processing in a position of prominence currently characterized by the apparel or paper industries.

An informative picture of data processing activities in the Data Systems Division may be gained by considering the following questions: *What are our products?*; *What are our prospects?*; and *What are our personnel skills?*

MARKET AND PRODUCT TRENDS

Near-future projections show that the following product areas will make up the base of data-processing business in the next two to three years:

1) *Digital data processors* — computers and associated devices.
2) *Visual data processors* — displays, film processors, electroluminescent panels, etc.
3) *Informative storage and retrieval processors* — video file, hybrid combinations of Electrofax, RACE (Random-Access Card Equipment), and digital and visual processors.

Market studies of the military, NASA and other areas show an overwhelming trend toward wider application of data-processing technologies. Applications such as weapon-control centers, tracking, data instrumentation, data reduction, check-out, launch control, command and management control, intelligence processing, countermeasures, weather prediction, patent and document processing, and air-traffic control, to name a few, are all dependent upon this advancing art for implementation. In DEP-DSD, numerous products and systems concerned with data processing are being developed and delivered to the military.

For example, the following products were delivered to defense customers during 1962:

Mobile Automatic Programmed Checkout Equipment—MAPCHE

MOBILE APCHE[1], or MAPCHE, is the prime checkout equipment employed to test and validate most subsystems of the various ATLAS missiles and associated air-ground equipment. It performs discrete response tests, analog response tests, timing tests, and servo-response tests. To evaluate a system under test, a deck of punched cards, programmed for an automatically sequenced test, is inserted in a card reader. A program control interprets this data and generates the proper stimuli and response.

RCA-4100 Computer

The RCA 4100 is a digital computer for military use of the internally stored program type.[3] It features 16 priority-interrupt levels, a magnetic core memory of 4096, 8192, or 16,384 words of 30 bits, and adaptability to van, shipboard, and fixed installation. The priority-interrupt feature conveys to the RCA-4100 a powerful real-time capability both from the standpoint of multichannel input-output and multiprogram control.

The RCA 4100 uses solid-state components and satisfies a combined military specification based upon MIL-E-16400C, MIL-E-4158B, and XEL303 requirements. A computer using identical

modules has experienced only 12 minutes downtime in 24-hour-per-day operation over a nine-month period.

High-Speed Arithmetic Unit for RCA 604

The RCA 604 High-Speed Arithmetic Unit and the RCA 603 Processor combine to provide a complex having advanced scientific computing and data processing capabilities. The RCA 604 multiplies, divides, adds, subtracts, and multiply accumulates in either fixed. floating-point, or psuedo-floating-point modes. The machine has a 36-bit mantissa and a 9-bit characteristic. It performs arithmetic in either single or double precision. Computation time for floating-point multiplication can be accomplished in about 6 μsec, exclusive of memory accesses. Exclusive of power supplies, the RCA 604 occupies two racks and employs about 15,000 transistors.

RADCON Digital Computer

The RADCON digital computer is especially adapted to military tactical utilization. It is a bus-organized, parallel, synchronous, single-address machine with a fixed program stored in a special wired-core memory. Loss of program instructions during a tactical situation is virtually impossible, since instructions are represented by wires threaded through pulse transformers contained in plug-in program trays. Programs are altered by changing program trays when rapid changes are desired. The RADCON has the following features: 1) a random-access, coincident-current core memory for data, 2) three index registers, 3) an interpreter for address modification and selection, 4) a sophisticated arithmetic unit, 5) error-detecting facilities, 6) error registers to hold errors for later analysis and action, and 7) real-time input-output facilities. Interface equipments include optical encoder strobing circuitry, digital-to-analog and analog-to-digital converters, a frequency-to-digital converter for encoding doppler, and a 54-kc digital data link required by the dispersion of the RADCON subsystem.

RCA 110 Computer System

The RCA 110 Computer System[6] is furnished to NASA for use as checkout control in the SATURN Program. It is comprised of eight cabinets (three main frame, five peripheral) and ancillary equipment consisting of an electric typewriter, a paper-tape reader and a paper-tape punch. The entire complex meets RFI military requirements. Peripheral equipment consists of analog and discrete switching units, power supplies, and tape stations. The RCA 110 has a serial arithmetic unit with parallel access to core storage. Programming flexibility is enhanced by the large storage capacity provided by both the high-speed working storage (4096 words) and the drum bulk storage (32.768 words).

As a central control unit, the RCA 110 communicates with other equipment through peripheral input-output units. Each class of signals (command, response, analog, discrete) is handled through its own channel under computer control and enters or leaves the computer through the appropriate input-output buffer.

RANGER Video Processor

This program. a subcontract from the DEP Astro-Electronics Division, Princeton, is for the Jet Propulsion Laboratory lunar program, RANGER. The first system has already been delivered for recording spacecraft video signals of the lunar surfaces. Recordings are made simultaneously on magnetic tape and film. The resolution and geometric accuracy achieved in this equipment far exceeds that of previous video recorders. In addition, the video processor checks out spacecraft cameras and associated ground support equipment prior to launch from Cape Canaveral.

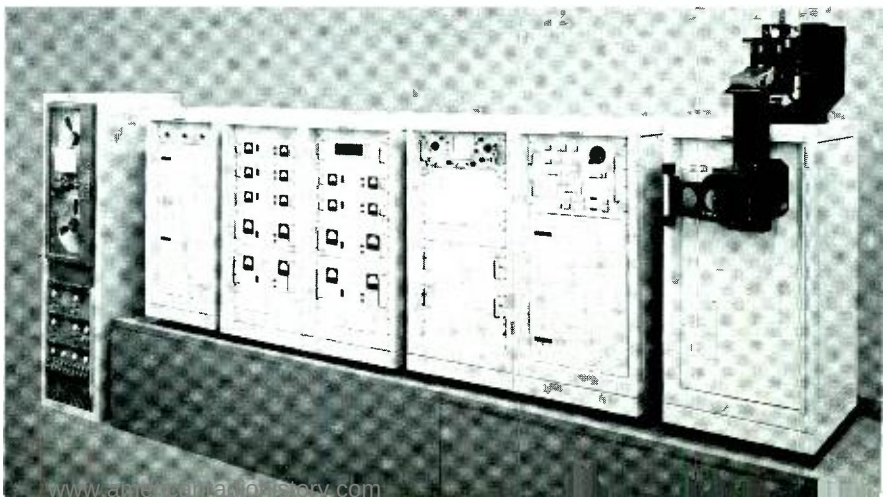
NASA Display and Control Console

The Display and Control Console consists of a desk-type console with a 21-inch display storage tube. It displays information in the form of charts, graphs, or printed pages under operator control. Printed pages can be presented at a rate of 8,000 alpha numeric charac-

D. J. PIZZICARA, Staff Engineer DSD, received the BSEE in Electronic Engineering from City College of New York and MSEE from Harvard University. He has completed advanced courses at Brooklyn Polytechnic Institute. His 15 years professional experience includes communication equipment, electronic computer development, and weapons systems direction equipment as well as engineering administration of several major computer systems. Additionally he served with the Air Force, instructing enlisted and officer personnel in electronics, physics, and mathematics. Mr. Pizzicara has been associated with the following engineering projects: the MKIII Computer for TALOS, weapon direction equipment for TALOS, TERRIER and TARTAR; and the data processing central for the MARS. Mr. Pizzicara is a member of Tau Beta Pi and Eta Kappa Nu societies. He received the regents scholarship and faculty award in mathematics. He has U.S. patents pending in the application of aided track techniques to scan conversion system, and has published several papers.

G. F. BREITWIESER Chief Engineer and Projects Manager of DSD when this paper was written, received the BS in Marine Engineering from the United States Coast Guard Academy and BSEE and MSEE from the Massachusetts Institute of Technology. His 18 years' experience incluae radar, sonar, and weapons control engineering as well as engineering administration of several major weapons systems. Serving with the Coast Guard, he gained experience as a radar, sonar, and/or gunnery officer, and later as officer-in-charge of engineering at the Electronic Engineering Test Station. Among the engineering projects Mr. Breitwieser has been associated with are: design and development of the AN/FPS-10D Height Finder Radar· project engineer on the Army Fire Control system for TERRIER; and manager of electronic development on such systems as the T44 Tank Fire Control system, the AN/SPS-12 Search Radar system, the AN/UPS-1 Assault Search Radar, the AN/FPS-16 Instrumentation and Radar system, the TALOS IM-70 Weapon system, and the MK 8 Shipboard Fire Direction system for TALOS. More recently, he has been concerned with the WS-107A-1 Atlas Launch Control and Checkout system, and the RCA portions of the Ballistic Missile Early Warning system (BMEWS). He is a member of IEEE and was awarded the coveted RCA Victor "Award of Merit."

Fig. 3—RANGER video processor.



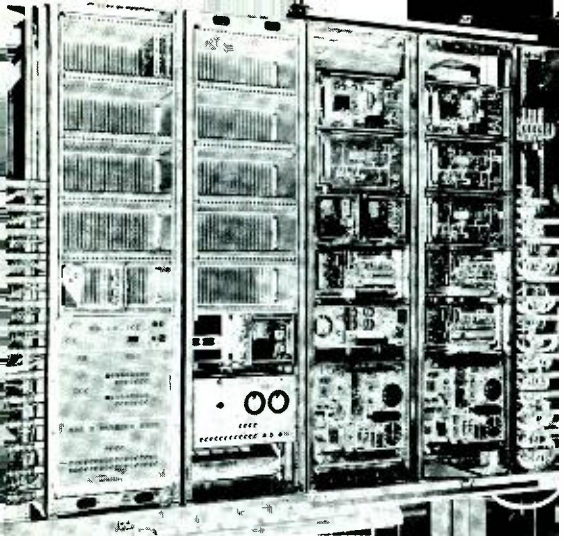


Fig. 4—RADCON computer.

Fig. 5—Mobile APCHE.

ters per second, permitting a full page of 1,600 characters to be presented in 0.2 of a second. Data can be retained on the tube face for up to two minutes and erased under operator control.

A typewriter type keyboard containing 43 alphanumeric characters and symbols controls the display console. In addition, a smaller keyboard containing 18 special symbols is used with the RCA 110 Computer.

FUTURE PROSPECTS

DEP-DSD is currently participating in the following missile or space programs: ATLAS, SATURN C, NOVA, BMEWS, and MINUTEMAN. Adidtionally, proposals are pending on such programs as: LUNAR EXCURSION MODULE, SATURN C5, NOVA, SATURN OPERATIONAL FLIGHT CONTROL SCHEME, APOLLO—GOSS, and ADVENT.

The RCA 110 and RCA 4102 computers launched in 1962 are being offered as on-line, real-time computers. Both machines promise a two- or three-year useful life in the market place and should yield a significant return on investment.

Another step forward is the *video file* concept for electronic image-processing or document storage and retrieval. The video-file development promises to be a cornerstone of DEP-DSD's entry into this important market. Information storage-and-retrieval systems', by 1967, may well represent a volume of business exceeding that of computer data-processing systems.

RACE (Random Access Card Equipment) is a new bulk store which will make large scale information storage and retrieval systems a practical reality. RACE has potential to store a billion bits (digital), or in excess of a million video images or film clips with average random access of 300 milliseconds.

The ready availability of such techniques as ELSI[2] (Electroluminescent Storage Indicator), high-speed jump scan, and digital-generated video will increase RCA's penetration in the command-control and program-management display fields. Typical of future applications are the Navy Strike Command, a flag officer strategic and tactical system; and the Management Program Command System to be located at the Directorate in Washington, D.C. A further development, now in its infancy, is reflective display. This has application to large-screen displays, providing the capability of high information rates. Reflective displays have the advantage that room illumination contributes to the brightness of the observed display, facilitating normal operator functions of writing or reading messages. These developments plus higher circuit speeds (clock rates up to 100 Mc) and memory-cycle speeds (0.2 microseconds or better) are today's technological building blocks.

ENGINEERING

DEP-DSD has grown from the 1959 force of approximately 500 (200 engineers) to 2000 in 1962, including an Engineering Department of approximately 1,100 at Van Nuys and 100 at the Data Systems Center at Bethesda, Maryland. This rapid growth was concurrent with the execution of several military programs grossing $200 million.

To carry out these programs, DSD requires the following broad mixture of skills:

System Application Analyst
Programmers
Operations Analyst
Machine Organization Specialists
Logic Designers
Product Planners
Numerical Analyst
Intelligence Specialists
Library Research Specialists
Language Analysts

The organized efforts of these specialists will conceive tomorrow's data-processing products. Along with advanced skills, the need arises for new concepts in product design and manufacturing techniques. Present-day components, operating well into the VHF region, have pushed conventional wiring and packaging techniques close to the limit of their capabilities. The data-processing art is facing a new challenge to package, interconnect, and manufacture micromodular and microelectronic circuitry for operation in VHF.

An idea of the impending radical changes imposed by molecular electronics can be gained from the fact that thousands of thin-film transistors can be deposited on one square inch of substrate. Clearly, the capabilities of manual dexterity are exceeded—and automation is demanded. Several research and development programs are being pursued to gain insight and solutions to these problems.

Successful prosecution of these endeavors is essential to expanding the base of data processing applications. A few untapped markets are as follows: libraries, the medical profession, and the legal profession. All require the services of the data processing field to contain and harness the aptly termed information explosion.[7]

CONCLUSION

RCA has entrusted DEP-DSD with considerable funding for proprietary data-processing equipment development. These developments will become our base of business operations for the next two or three years. In the data-processing market, an *off-the-shelf* product is mandatory to compete successfully with the rest of the industry. Consequently, we must continue to enter into new and challenging product areas involving advanced concepts.

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THE RCA 301 SCIENTIFIC COMPUTER

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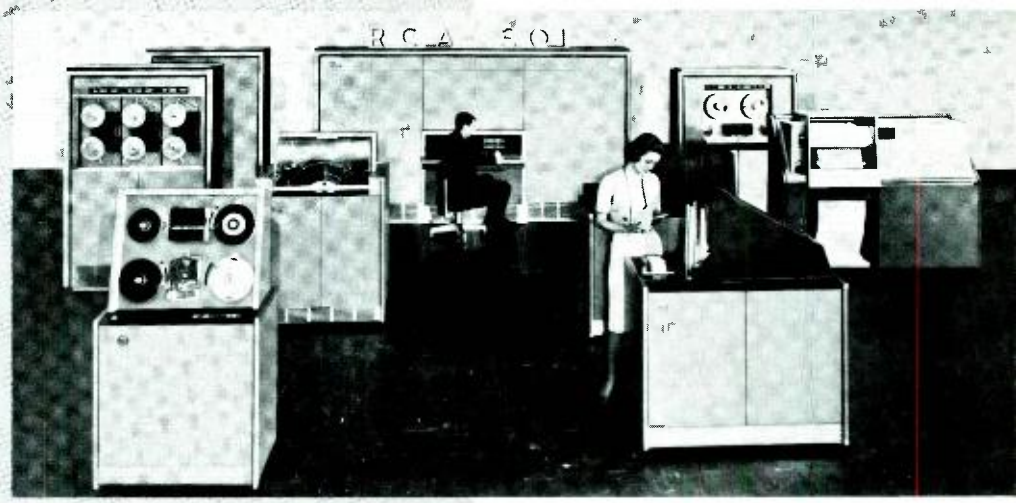
A new high-speed arithmetic unit is now available for the RCA 301 Computer to add scientific capability to the basic RCA 301 System. With a new total of 58 instructions, a user can apply the RCA 301 efficiently to both technical and business problems. The new arithmetic unit can be added to any existing RCA 301 system, and a variety of subroutines and programs are made available by RCA for scientific applications.



THE *high-speed arithmetic unit*, latest enhancement of the RCA 301 System, adds scientific capability to the low-cost, high-capacity RCA 301 Computer. With this capability, a customer can acquire greater efficiency for his rental dollars and schedule time for both technical and business assignments.

With the addition of the high-speed arithmetic unit, the present RCA 301 instruction repertoire is increased from 48 to 58 instructions, and the execution of arithmetic instructions is accomplished at least 100 times faster. The 10 new instructions are: *Fixed and floating add*, *subtract*, *multiply* and *divide*, *shift register*, and *store register*. The data format of a fixed-point operand consists of eight digits, and that of a floating-point operand consists of ten digits. The least-significant two digits are the exponent, and the remaining eight digits are the fraction of the operand. The sign and the overflow are indicated by the standard RCA 301 zone bits.

The instruction format is consistent with the present RCA 301 format, the only variation being the interpretation of the *N* digit. The two most significant bits of the *N* digit indicate that the operands *a* and *b* are taken either from the *A* and *B* address locations or from the accumulator. The next bit controls whether the result is stored in the accumulator only or is also transferred to the *A* address location. The last three bits of the *N* digit control the selection of the three index fields for the *A* and *B* address modification which is carried out during staticizing. Also, the modified tally instruction permits the incrementing or decrementing of the index fields on the consecutive runs through a program loop. This adds a very powerful tool to the RCA 301 Scientific Computer.

To be consistent with the original RCA 301 modular philosophy, the arithmetic unit can be added to *any* RCA 301 System in the field. The estimated time of the field installation, which includes some necessary modifications to the 301 basic processor unit, is 40 hours.

RCA makes available a variety of scientific subroutines for matrix operations, linear programming, statistical analysis, differential equations, and curve-fitting, plus scientific and Bell Interpreter Systems, UMAC (an algebraic compiler employing FORTRAN mathematical statements), and RCA 301 FORTRAN. Also available are some special industrial programs, such as lens design, bus scheduling, electrical load distribution, power requirements analysis, and others.

Current marketing reports indicate that the RCA 301 Scientific Computer *has no serious competitors in its price range.*

FUNCTIONAL SPECIFICATIONS

After the modifications required for the addition of the high-speed arithmetic unit, the basic processor unit models 304 and 305 become Models 354 and 355, respectively. The arithmetic unit provides the hardware for high-speed fixed- and floating-point arithmetic and associated address modifications. The unit occupies 12 rows (a half rack) of the control module rack.

The arithmetic unit consists of an addressable upper accumulator and lower accumulator, two nonaddressable arithmetic registers, and a high-speed parallel adder. Standard core memory locations are assigned for address modification. They are the three Index fields used during staticizing and the three increment fields used by the modified tally instruction.

Any quantity falling within the range of 10^{-99} to 10^{+99} can be represented in the floating-point format to the eight-digit precision. All the floating-point results are automatically normalized and rounded. To make double-precision programs possible, the results of fixed point arithmetic are not rounded.

Since the operands of both fixed and floating arithmetic are word-oriented, they must always begin at even locations in the core memory. The floating-point zero is represented by the zero fraction with the exponent of −99.

All the arithmetic-unit errors stopping the computer are indicated by the ARIE alarm on the processor console. There are six different conditions that will ac-

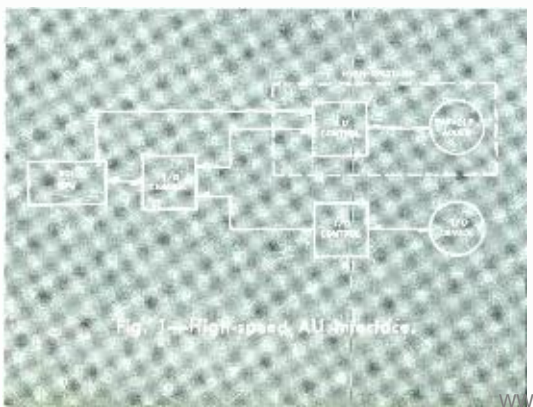


Fig. 1—High-speed AU interfaces.

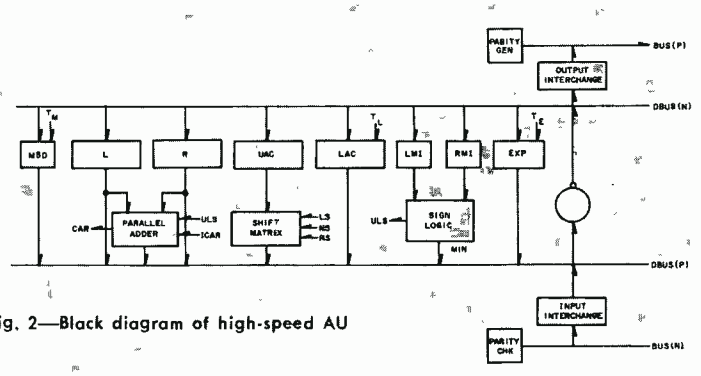


Fig. 2—Black diagram of high-speed AU

tuate the ARIE alarm: 1) *data parity error*, 2) *non-normalized operand*, 3) *dividend greater than divisor*, 4) *zero divisor*, 5) *zero operand with the exponent not equal to −99*, and 6) *modified address exceeding the core-memory capacity*.

The data characters in the arithmetic unit are numeric (straight binary-coded decimal) and therefore the 2^4 and 2^5 zone bits are ignored with the exception of the permissible 2^4 bit in the most-significant digit and the 2^5 bit in the least-significant digit of a quantity, signifying an overflow and negative sign, respectively. Both zone bits can be transferred from the arithmetic unit to the core memory, but only the zone bit signifying the negative sign can be transferred from the memory to the Arithmetic Unit.

Depending on the sign of the result, a corresponding PRI *(previous result indicator)* is set at the completion of any arithmetic instruction. SCAR, signifying an overflow, may be set only in *fixed add/subtract* and in any floating instruction indicating that the resultant exponent exceeds the range of ±99.

FUNCTIONAL DESCRIPTION

Intercommunication with 301 Basic Processor

The similarity between the high-speed arithmetic unit and any input-output control module (besides their common modular structure) can better be seen if the parallel adder is considered to be the arithmetic unit's peripheral device (Fig. 1). Some of the signals, not available from the input-output channel, are obtained through additional lines. These are codes of the new arithmetic unit instructions, new status levels, and special controls.

While the average input-output device speeds are far below the present processor speeds, a good balance was achieved between the 301 basic processor and the parallel adder in the high-speed arithmetic unit. Any further speeding up of the adder would not be justified by the performance-versus-cost relationship.

Although the high-speed arithmetic unit has its own eight-clock-pulse generator, it runs synchronously with the basic processor, BPU. The purpose of the arithmetic-unit clock is to subdivide status levels into more timing slots that are available from the 301 basic processor. This increases the number of performable functions per status level.

The High-Speed Arithmetic Unit

There are eight data buses (DBUS0 to DBUS7) connected, via read-in and read-out gates, to the corresponding digits of all the arithmetic-unit registers. The data from the core memory is transferred one dyad at a time via BUS2 and BUS3 of the input-output channel and the input interchange to the consecutive DBUS's starting from the least significant pair. The input interchange is switched by means of control signals IN1 to IN4 which are generated by a counter running during the loading of operands to the arithmetic unit. Similarly, the output interchange controlled by the signals OUT1 to OUT4 switches the consecutive pairs of DBUS's to the core memory via BUS2 and BUS3. There is a provision made to transfer all the four digits of *A* or *B* address at one time. Moreover, if the address has any zone bits in its most significant digit (signifying either 20,000 or 40,000 character memory) the input interchange generates an equivalent fifth digit. After performing an address modification, the resultant fifth digit is combined with the address most significant digit in the output interchange.

The parity of the incoming data is checked at the input interchange. All the DBUS's consist of four lines with the exception of DBUS0 and DBUS6 which also have 2^4 lines and DBUS7 which has a 2^5 line. After the execution of an arithmetic instruction, the four-bit numeric code is transferred back to the seven-bit code at the output interchange.

There are eight registers in the arithmetic unit (Fig. 2). Starting from the left, the registers are:

MSD—*most significant digit.* This is a single-digit register triggerable up or down. As its name implies, it is the most significant digit of sums, partial products, and partial remainders.

L and R—*left operand* and *right operand.* Both registers are eight-digit registers and their contents provide the input to the parallel adder.

UAC—*upper accumulator.* This register stores results and is associated with the shift matrix.

LAC—*lower accumulator.* This register, with its least-significant digit LAC7 (triggerable up or down), is used for generating the quotient in *divide* and exhausting the multiplier in *multiply* instructions. It is also used to store the second part of the product in *fixed multiply* and remainder in *fixed divide.*

LMI and RMI—These are single-bit registers used for storing the signs of operands. In association with the sign logic, they generate the ULS *(unlike signs)* signal and MIN (the sign of the results).

EXP—*Exponent Register.* This register is a two-digit algebraic up or down counter.

Parallel Adder and Sign Logic

The eight-digit parallel adder operates on straight binary-coded decimal digits.

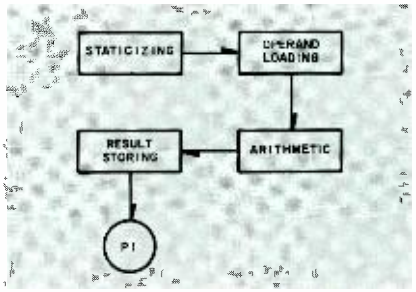


Fig. 3—General fixed point arithmetic flow chart.

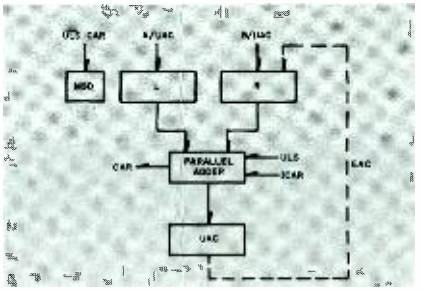


Fig. 4—*Add/sub* data flow chart.

Fig. 3—Fixed-point arithmetic instructions, general functional flow chart. The RCA 301 Computer, being a two-address system, requires *Ai* for the transfer of the result to the memory. This is accomplished by loading the *B* operand into the arithmetic unit and transferring *Ai* to the *B* register. This register is then used in the final step of the arithmetic instructions, which is loading of the result into memory.

Fig. 4—Add-subtract, fixed point. After loading the L and R registers, a minimum of 3 μsec is allowed for the adder to propagate carry. The output of the adder is then transferred to UAC. The result has an overflow if ULS·CAR. This condition is used for triggering up MSD. If MSD = 0, the 2^4 bit is set in the most significant digit of UAC. The condition ULS·CAR initiates the EAC procedure. In this case, L and R registers are reset, UAC→R, and $0 + \bar{R} \rightarrow$ UAC, thus correcting the result in the manner explained above.

Fig. 5—Multiply, fixed point. The loading of operands proceeds in a similar manner as in *fixed add-subtract*, but the destination of operands is different. The multiplicand *a* is transferred into R and the multiplier *b* into LAC. The multiplication algorithm consists of two cycles; a consecutive addition (generating partial product) and a right coupled shift. The consecutive addition proceeds as follows:

L + R is transferred to UAC.
If there is a carry, MSD is triggered up.
LAC7 (l.s.d. of LAC) is triggered down.
UAC is transferred to L and the cycle is repeated until LAC7 = 0.
When LAC7 = 0, the shift cycle performs a coupled right shift of MSD, L, and LAC, and triggers the digit counter down.
If the digit counter XC ≠ 8 and LAC7 ≠ 0, the first cycle is selected again.

After eight shifts, the multiplication is completed and the final product, consisting of 15 or 16 digits, is stored in UAC and LAC. For single precision, only the part in UAC is used. For double precision, the parts in UAC and LAC are used.

Fig. 6—Divide, fixed-point. The loading of operands is the same as in *fixed add-subtract*. The divident *a* is transferred into L and the divisor *b* into R. The division algorithm consists of two cycles; a consecutive subtraction (generating partial remainder) and a left coupled shift. The procedure is as follows:

A left shift of L is executed, transferring the m.s.d. of L into MSD. This step enables multiple precision.
The subtraction cycle is then started with L—R being transferred to UAC.
If there is no carry, MSD is triggered down.
If MSD ≠ 15, LAC7 is triggered up and UAC is transferred to L.
The cycle is then repeated.
When MSD = 15 (which means the difference L—R is negative), the left coupled shift of MSD, L, and LAC is performed, the digit counter is trig-

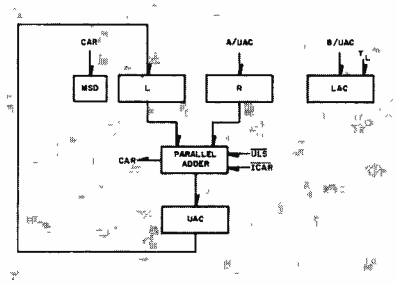


Fig. 5—*Multiply* data flow chart.

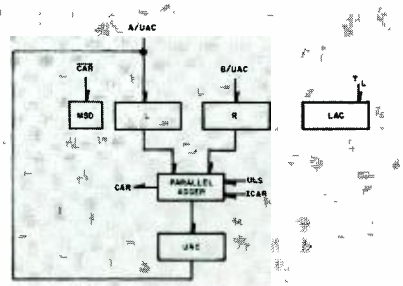


Fig. 6—*Divide* data flow chart.

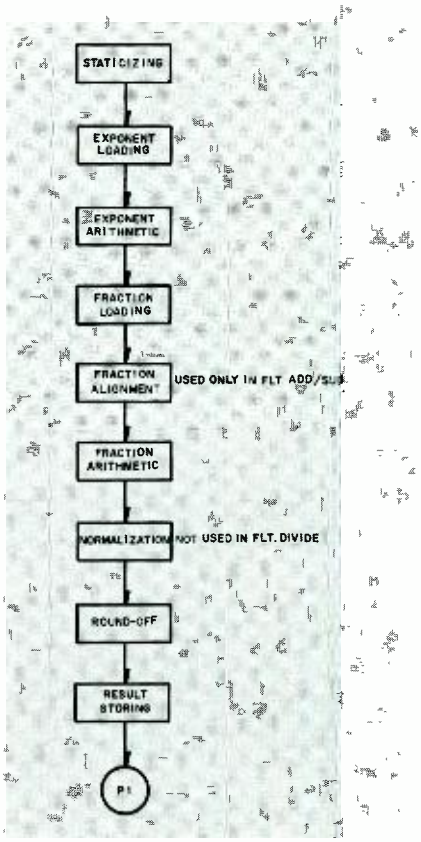


Fig. 7—General floating point arithmetic flow chart.

gered up, and the subtraction cycle is selected unconditionally.

The execution is terminated in the subtraction cycle when MSD = 15 and XC = 7.

Fig. 7—Floating-point arithmetic instructions. Floating-point arithmetic uses only the algorithms previously described and is similar to fixed-point arithmetic with some additional operations. The additional operations are exponent arithmetic, alignment of fractions (used in *floating add-subtract*, only), normalization of results, and round-off. The exponent arithmetic is a straight addition or subtraction depending on the instruction. The normalization is a left or right shift of the result with the corresponding correction of the exponent. The latter is done by triggering the exponent register algebraically up or down. The round-off is carried out on the basis of the least significant digit outside the eight digit precision. The general flow charts contained herein do not indicate any special paths. The charts are of a general nature because, depending on the instruction options and the result itself, some of the functions may be redundant. These procedures are bypassed, whenever applicable and justified by the involved cost, by means of special case status level selections.

Add or Subtract, floating point. The exponent arithmetic carried out three independent functions, and they are as follows: 1) it stores the algebraically larger exponent; 2) computes the exponent difference; and 3) determines which fraction is to be shifted to the right for the alignment purposes. During the alignment, the shifted-off digits from L and R are stored in LAC in a straight or complemented form, depending on the ULS signal state. This is done in order to provide the information for rounding-off. The fraction arithmetic is, in principle, identical to the *fixed add-subtract* arithmetic. During the normalization, the result is either shifted right (if MSD $\neq$ 0) or shifted left (if there are any zeros in the most significant portion of the result and MSD = 0). The rounding-off is performed by adding 1 to the result if LACO$\geq$5. The solution of the case of an overflow produced during the round-off is left for the readers.

Multiply, floating point. The exponent arithmetic generates an algebraic sum of the operand exponents. The fraction arithmetic is identical to the one of the fixed multiply. As the final product may consist of 15 or 16 digits, the normalization, if any, produces one coupled left shift of UAC and LAC. In the rounding-off, as before, the result is incremented by 1 if LACO$\geq$5.

Divide, floating point. The exponent arithmetic produces an algebraic difference of the operand exponents. In the fraction arithmetic, if $a<b$, the dividend is shifted one place to the right, thus cancelling the need for the normalization of the result. The following consecutive subtractions and shifts are the same as in the *fixed divide*. For the rounding-off purposes, the ninth cycle of the consecutive subtractions is carried out, but the ninth quotient digit is not allowed to exceed five. If the digit is five, the rounding-off takes place, otherwise, the execution of the division is terminated.

It can be shown that the excess-three code has hardly any advantage over the straight binary code in decimal adders. The excess-three self-complementing code requires some decoding at the adder output and, as a result, is more expensive than the complementing of the straight code. The complementing circuit is associated with the R input only.

The most fundamental operation in the arithmetic unit is addition. The adder performs subtractions using the following algorithm.

Case 1: $a>b$

$$a-b \equiv a+\bar{b} =$$
$$a+(10^n-b) = 10^n+(a+b)$$

Instead of subtracting b, add its ten's-complement $\bar{b}$. The presence of 10^n, being a carry of n-digit precision, indicates that the result is correct. In this case, the sign of the result is taken to be the same as one of the operand a.

Case 2: $a<b$

$$a-b \equiv a+\bar{b} = d$$

As there is no carry, the following procedure, known as EAC *(end around carry)* is initated:

$$0+\bar{d} = 0+[10^n-(a+\bar{b})] =$$
$$0+10^n-[a+(10^n-b)] = -a+b$$

In this case, the sign of the result is taken as the opposite of the operand a.

In the adder, the complementing of b operand is initiated by the ULS signal. It is carried out by the complementing of each digit to 9 and then with the generated ICAR *(initial carry)* the result is effectively increased by 1:

$$\bar{b} = 99999999 - b_0b_1b_2b_3b_4b_5b_6b_7 +$$
$$1 = 10^8 - b$$

The sign logic is mechanized to follow the fundamental rules of the arithmetic.

The parallel adder is also used for the arithmetic on exponents in the floating-point instruction. It was planned originally to provide a special two-digit adder for the exponent arithmetic, but the additional cost would not justify a negligible saving of time.

INSTRUCTIONS

Figs. 3 through 7 and their accompanying captions and text describe both the fixed-point and floating-point arithmetic instructions of the RCA 301 Scientific Computer.

SUMMARY

This article has given a general picture of the high-speed arithmetic unit to readers who are familiar with the RCA 301 System.[1] Some of the minor details, often far from being easy problems for an elegant solution, were omitted. Readers interested in more-complete details of the high-speed arithmetic unit are welcome to request, through the normal channels, the functional specifications for Processor Models 354 and 355, status level flow charts, and logic drawings.

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ANATOLE TURECKI received his BSc degree in Engineering from the University of London in 1949. From 1949 to 1956 he was employed by Harris Lebus, Ltd. (London) as a Research Engineer; was employed by Tasma Pty. (Sydney) as a Development Engineer; and was a Lecturer in the Radio School of the Royal Melbourne Technical College. He joined RCA in 1956 in the Broadcast Engineering Division where he designed and tested TV transmitting antennas. He transferred to RCA Electronic Data Processing in 1960 where he assisted in design and testing of the RCA 301 System. He completed all course requirements for his MSEE at the University of Pennsylvania in 1960, and his thesis, "Ternary Numerical System in Digital Computers", is presently being submitted. He is a Member of IEEE and holds a U. S. Patent.

Fig. 1a — RCA 601 control console.

THE RCA 601 COMPUTER SYSTEM

Design of the RCA 601, largest of RCA's product-line computers, involved solution of major problems in circuit packaging and wiring techniques occasioned by the complexity and speed of the machine. The first RCA 601 System was delivered to the New Jersey Bell Telephone Company and became operational in December 1962. The success of solutions to the design challenges is marked by the fact that machine "up time" has considerably surpassed original expectations. For another user, a second system was recently delivered, and three more are scheduled for 1963. The RCA 601 features many powerful programming and operating features, and has a basic high-speed memory capacity of 8,192 words of 56 bits each which can be expanded by addition of up to twelve memory stacks of 2,048 words each. Data readout from the memory is in less than 0.9 μsec, and the complete memory cycle is 1.5 μsec.

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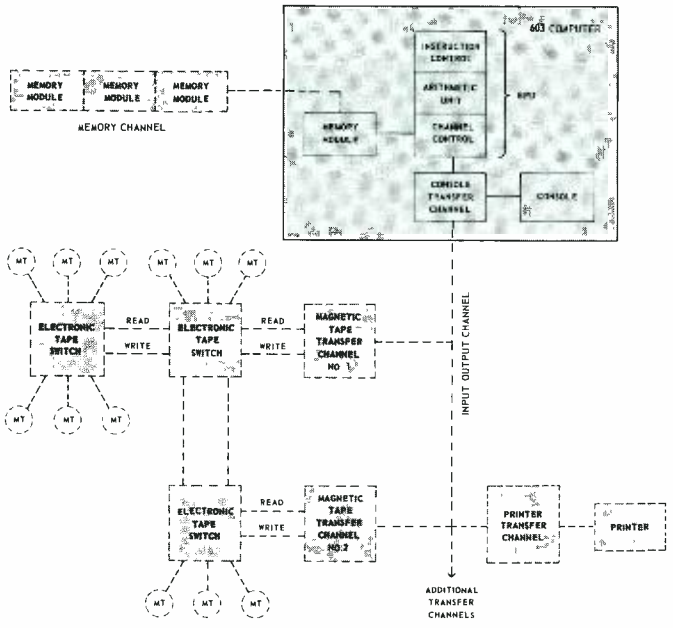

Fig. 1b — RCA 601 System, illustrating expandability.

THE RCA 601 is a variable-address computer with an instruction complement that can handle both word-oriented and variable-length-data problems. The computer incorporates an extremely powerful address-modification scheme which allows indirect addressing, many levels of modification, and the ability to increment the modifiers. Another important feature of the RCA 601 is its ability to have automatic interrupts for servicing of input-output equipment or console demand functions. Errors also cause interrupts, rather than machine stoppage, giving a programmer the ability to utilize programming rollback features or diagnostic routines.

BASIC SYSTEM

Fig. 1 illustrates system expandability. The basic computer system consists of a console, a basic processing unit, a high-speed memory (8,192 words of 56 bits each), a power supply, and a console

* In association with J. J. O'Donnel, E. Gloates, B. Freedman, and W. Gibbeson of Electronic Data Processing.

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transfer channel. The basic processor contains hardware necessary to mechanize instructions, an arithmetic unit capable of doing word additions, and controls necessary to link the associated units. The arithmetic unit also provides a data handling capability (shifting, masking, merging) of all the various character lengths. Up to 12 additional stacks (2048 words each) of high-speed memory modules can be added to the basic computer.

The logic within the computer is asynchronous. Therefore, the subclocks of the machine are self-timed, and the worst-case delays need not be considered for all paths. During a data transmission, for example, the contents of the register receiving data are compared with those of the transmitting register to determine when the transmission is complete. This comparison is also used to provide a high degree of accuracy control. Each subclock—for example data transfer, high-speed memory, or arithmetic unit, controls a portion of the computer's logic. Each is started individually and operates independently, except for necessary interlocks at points of timing intersection. Because of this type of logical construction, overlapped operation is possible—individual subclocks can operate concurrently, even though they may be under the control of different steps in the execution of an instruction. Since there is no need to wait for each step to conclude before starting the next, and because each step is self timed, considerable computer time is saved.

The console (Fig. 1a) is divided into two major areas:

1) The *operator area* which contains such features as numeric displays of registers or memory contents, a digital keyboard for entering information into the system, a paper tape reader and a flexowriter which may be used for input as well as output.
2) The *supplementary indicator area* which houses the indicators necessary to display many registers and flip-flops in order to facilitate trouble shooting and thereby minimize downtime.

Another major feature of the system is its input-output handling capability. As Fig. 1 shows, there is an expandable input-output channel. Transfer channels are attached via this link to the computer, so that additional input-output devices may communicate with the high-speed memory. Each transfer channel not only adds the ability to interchange information with more peripheral devices, but also adds degrees of simultaneity so that up to 16 devices may be operating concurrently with normal processing. Therefore, it is possible to have eight *read's*, eight *write's* and the computer operating together. The system can handle up to 48 tape stations at speeds of 33-, 66- and 120-kc through electronic switches which allow more than one transfer channel to communicate with each station. The console also communicates with the basic processor through the console transfer channel and the input-output channel. Many functions of the console can therefore be handled while the program is operating. For example, it is possible to read out of or write to the memory from the console while the machine is running a program.

HIGH-SPEED MEMORY

The high-speed memory is an asynchronous unit. When running at maximum speed, the time for a complete cycle (read out the information and write it back into the memory) is 1.5 μsec. Data is read out onto the bus in less than 0.9 μsec. Because it is asynchronous, the memory can perform part of a cycle, stop while the processor makes changes, then continue on with the next part of the cycle instead of having to perform a complete cycle for each part.

Close cooperation between RCA Laboratories, Princeton, the SC & M Needham Materials Operation and the RCA 601 project personnel, produced the fastest large-memory system built by RCA.

The stack is designed so that only two wires, at right angles to each other, pass through the core. One wire is an address-drive line which carries both read and write pulses. The other wire is a digit-sense line which carries the digit pulse during the write part of the cycle and the core output during the read part of the cycle. Coincidence of the write-current and digit-current pulses causes the core to switch to a *1* state. The core will return to a *0* state if the digit write pulse is absent when the write pulse is present.

Address (Drive-Line) System

Fig. 2 illustrates the method of selection of a particular drive line, and how only one wire is used for both read and write pulses.

The emitters of the current switches are connected to the output of a common driver which is used as a constant-current source of the read and write pulses. One write and one read current switch which have their collectors tied together through diodes to a current bus using 32 lines, can be selected. At the bottom (grounded) end of the drive line, one write and one read voltage switch can be selected. Their collectors are also tied together through diodes; however, there is a read and a write diode associated with each drive line to prevent sneak current paths (e.g., path *A, B, C, D, E*). The voltage switch boards, with all their diodes, plug directly into the stack.

Digit-Sensing System

A simplified diagram of the digit-sense system is shown in Fig. 3. It illustrates how only one wire is used to carry both the digit write pulse during writing and to sense the core output during read. The design of the stack is such that the digit-sense winding crosses the address (drive) lines at right angles.

PROGRAMMING

Inasmuch as the overall RCA 601 design philosophy called for a tape-to-tape system (i.e., all peripheral operations are performed via an RCA 301 computer) the RCA 601 software system was designed around a *magnetic-tape library* concept. Because of the complexity of the RCA 601 system, the programming package provided by RCA consists of four primary areas: the *executive system*, the *file-control processor*, the *sort-merge*, and the *RCA 601 assembly system*.

Fig. 2 — High-speed memory drive system.

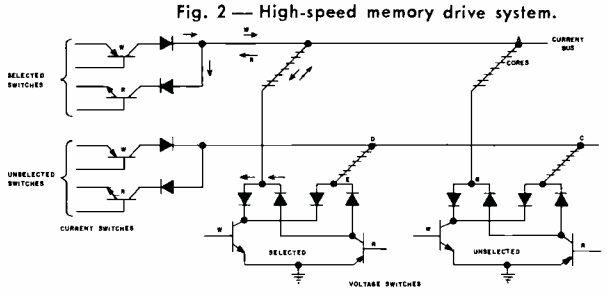
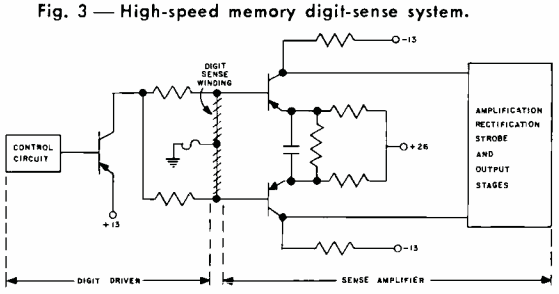


Fig. 3 — High-speed memory digit-sense system.



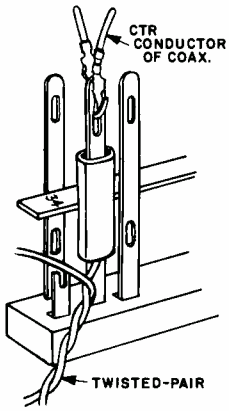


Fig. 4 — RCA 601 metallic clip connector.

In order to properly service the program library tape, the executive system was developed to control program loading and operation. One of the outstanding features of this system is the console demand facility which allows the computer operator to automatically interrupt the program in operation to: take memory or tape prints, discontinue the current program, continue with the next program in a prestored list, reassign input-output devices, and perform other functions common to the operation of a large scale computer system.

The file-control processor automatically directs the simultaneous input and output operations of the RCA 601. With it, the user can easily make use of the flexibility of the RCA 601 in the area of tape processing. The file control processor insures that all available input areas are filled and that data is made available to the user when required by the program. It also performs appropriate tape-label checks and controls input-output error recovery as well as many other functions required for the efficient utilization of the RCA 601 as a data-processing system.

The RCA 601 sort-merge package consists of two powerful generalized sort and merge routines which automatically tailor themselves to best fit the desired application as expressed through a series of parameters entered via the console paper tape reader or prestored on program library tape.

The RCA 601 assembly system links the entire package. In addition to providing the normal features of a good assembly system, such as symbolic representations for all machine instructions and features, subroutines and symbolic memory allocation, the RCA 601 assembly system provides a series of macroinstructions that automatically supply program linkage with the executive system and the file-control processor. Through these instructions, the program may instruct the executive system and file-control processor to perform such functions as calling in additional segments of the program, typing a message on the monitor printer, reading or writing magnetic tape, or even calling in another program to replace itself.

RACK DESIGN

Mechanical design challenges of the RCA 601 racks were created to a large degree by the need to minimize interconnections between racks—and reduce effects of noise and crosstalk. The use of somewhat larger racks and a high-density packaging of the electronic circuits resulted from these new standards of compactness. The 44-inch racks were designed to accommodate 650 plug-in circuits, and the 22-inch racks to house 325 plug-ins.

The basic processor, power supply, and high-speed memory are housed in the 44-inch racks and the remaining units (the transfer channels) occupy racks 22 inches wide. Cooling air is circulated in each rack by centrifugal fans capable of supplying air at 350 cfm against a back pressure of 0.5 inches of water. If the air flow is impaired, an alarm is activated by a protective device consisting of a set of air vanes and switches.

Cabling and Rack Wiring

Peripheral device and power cables enter the rack from the bottom section of the blower assembly. The signal cables (coax wired) connect between racks through side connectors. Power cables are of a new design which provides maximum decoupling. This cable is made up of layers of thin flat conductors employing the necessary circular-mil areas to carry the required current. The new power-cable design has very low inductance due to a favorable ratio of surface area to cross-sectional area.

Cables are sandwiched together—a voltage conductor, a ground conductor, a voltage conductor, etc. Conductors are insulated from each other by using a high-K material. This combination of a small-inductance cable and a very large distributed capacitance is ideally suited for supplying step loads, by assuring a minimum voltage drop and maximum HF filtering.

A number of special techniques were developed to permit the innerconnection of large numbers of logical elements, prevent excessive build-up of wire in certain areas, and reduce the noise due to common impedance. These techniques included a specially developed coax of very small diameter, solder clips which relieved the strain on the center conductor of this coax, multi-level terminals on the connector (Fig. 4), and a special grounding system isolated from the frame (Fig. 5).

The RCA 601 wiring schedule was prepared by an RCA 501 computer utilizing 1) plug-in location and pin number of the source signal from the logic diagram, 2) plug-in location and pin number of the destination from the logic diagram, and 3) the wiring parameters. In order to minimize crosstalk, the following wiring parameters were used: 1) trees less than 6 inches use single wire, 2) trees between 6 inches and 4 feet require twisted-pair wire, and 3) all trees over 4 feet require coaxial cable.

Module Boards

To package the large number of transistors in an RCA 601 rack, it was found that the packing density of the RCA 301 module board was insufficient. For example, the RCA 601 required an average of 14 to 16 (with a maximum of 24) transistors per module board while the RCA 301 averaged only 8.8 transistors per module board (with a maximum of 18). The number of pins best suited to these logic requirements was determined to be 35.

The final pin-connector boards retain the basic features of the RCA 301 and RCA 501 designs, but with additional pins. Fig. 4 illustrates a portion of the connector and the metallic clip presently used on the plug-in to provide suitable board connections.

PLUG-IN-CIRCUIT PACKAGING

The RCA 601 system required a special plug-in-circuit design. The goal was to provide a special-purpose board with greater packaging density. For example, approximately 9500 transistors on 650 plug-ins, were to be packaged in a single 44-inch rack. The final RCA 601 design consisted of plug-in units made up of mother boards and submodules. The submodules serve a dual purpose: 1) to free the main board area for signal and interconnections and 2) to provide maximum exposure of the board-mounted

Fig. 5 — RCA 601 backwiring.

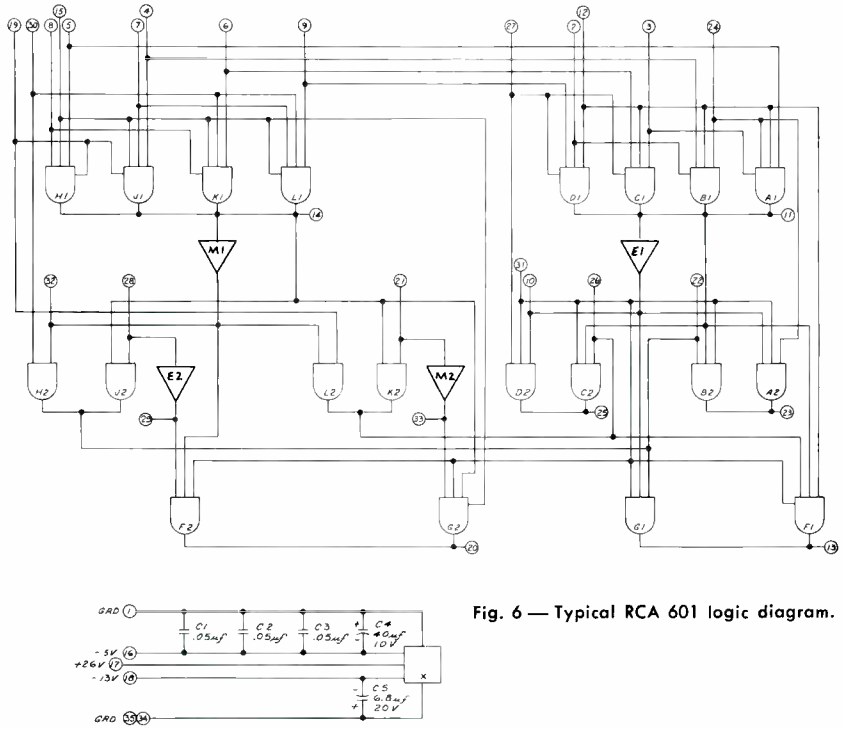


Fig. 6 — Typical RCA 601 logic diagram.

components to the cooling air. Each submodule in the logic and control sections contains two circuits and is easily accessible for repairs and rework. Whenever possible, specialized logic functions are combined on one board. Fig. 6 illustrates the large amount of logic circuitry mounted on the sample plug-in of Fig. 7.

In previous module packaging design, the handling of the input diodes and the mounting of the resistors and capacitors caused problems. Thus, for the RCA 601, the design and development of a new diode package and of an integrated-assembly *printed electronic component* were completed. The printed component contains the required resistor and capacitor elements. The diode packages contain either two or three RCA diodes in a TO-5 transistor case; this highly reliable unit was developed by the Semiconductor and Materials Division to meet RCA 601 specifications.

The final printed-electronic-component package design was to contain the four resistors and a capacitor required for the logic and power gates. Performance specifications called for elements meeting or exceeding the characteristics of standard components. Cost was limited to approximately that of assembling standard components.

The complete RCA 601 plug-in board consists of a filter, a termination board, submodule elements, and the etched circuit pattern. The termination board supplies a resistive termination for any signal pin on the mother board (Fig. 7). The end load on a tree is terminated and discharged so that the line voltage falls as the source decreases. On the average, eight trees terminate on every plug-in; terminating resistors have clips so that connections may be made from any signal pin to the −5-volt return. The ohmic value of these resistors is determined by knowledge of the tree source (high-speed power, high-speed transistor) and the number of loads being driven.

Because of the special-purpose configuration, there are many types of boards in the RCA 601 system; however, some degree of standardization was possible in the submodule area. One basic configuration was used for approximately 80 percent of the submodules in the system. By varying the components, different layouts were accomplished.

Submodules are subjected to strict tests. Each basic submodule must satisfy a detailed performance specification—signal levels, circuit delays, rise times, fall times, etc. After assembly of the submodules to the plug-in boards, a logic test is performed. (No actual performance measurements are made at the plug-in level.) The plug-in and submodule test procedures are incorporated into the drawing structure for future use.

SPARES

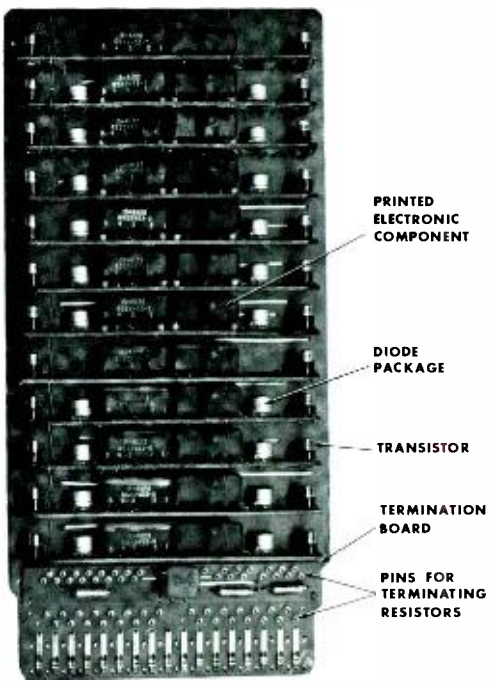
A new approach was developed for the RCA 601 to reduce the spares needed to maintain the system. Studies promised substantial savings if an effective method of plugging in the submodules could be developed. To accomplish this and at the same time stay within stringent height requirements was the main objective (0.8-inch spacing of plug-in units in the rack). Fig. 8 illustrates the pin-and-socket approach which finally proved satisfactory. Cost estimates indicate that this method and a proper sampling plan have reduced the cost of spare plug-ins by more than 50 percent.

CONCLUSION

Experience provided by the RCA 601 program indicates that the limits of using present packaging and wiring techniques on large-scale computers is rapidly being approached. As circuit speeds increase and computers become more complex, wire lengths and termination become more critical. Noise pick-up through capacitive and inductive coupling, and common impedance become problems of increasing concern.

These design problems, however, were successfully solved in the RCA 601. The first system (see front-cover picture) was delivered to the New Jersey Bell Telephone Company and became operational on Dec. 1, 1962. Since then, use of the equipment has rapidly grown from eight to over fourteen hours per day. The machine "up-time" has considerably surpassed original expectations. A second system was recently turned over to Public Service Electric and Gas Company of New Jersey. Completion of three more RCA 601 systems is scheduled for 1963.

Fig. 7—Typical RCA 601 plug-in circuit module.



AUTOMATIC DATA RECORDING SYSTEM

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* This work was completed while the author was with RCA Electronic Data Processing, Cherry Hill, N. J.

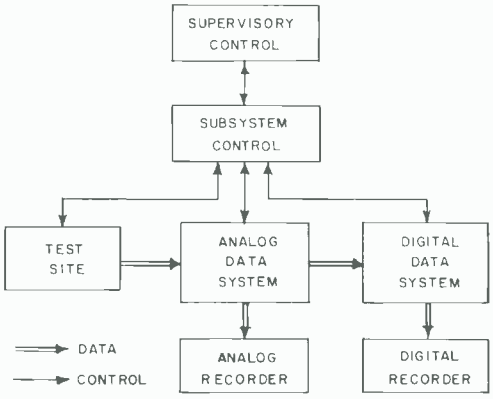


Fig. 1—The basic ADR system.

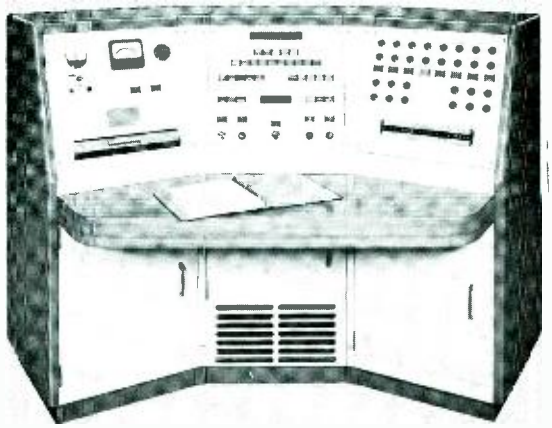


Fig. 5—The ADR supervisory control console.

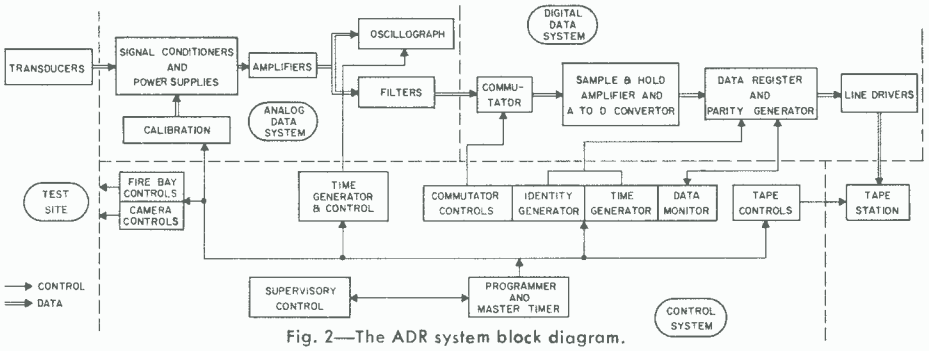
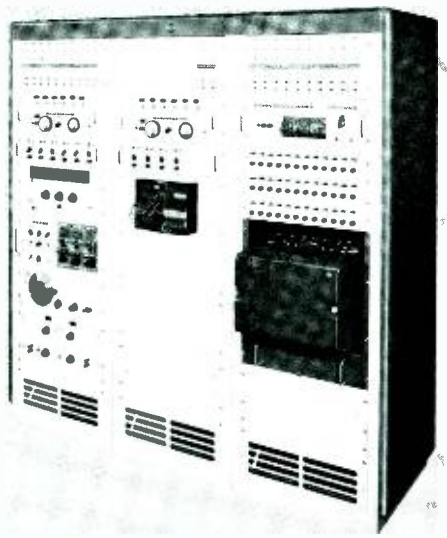


Fig. 2—The ADR system block diagram.



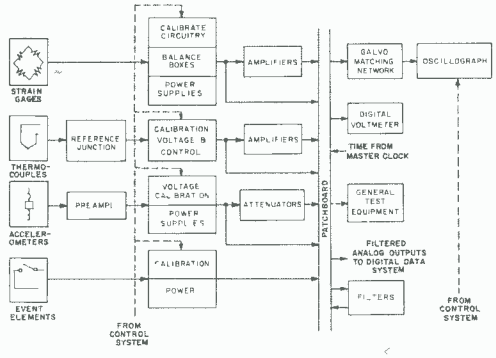
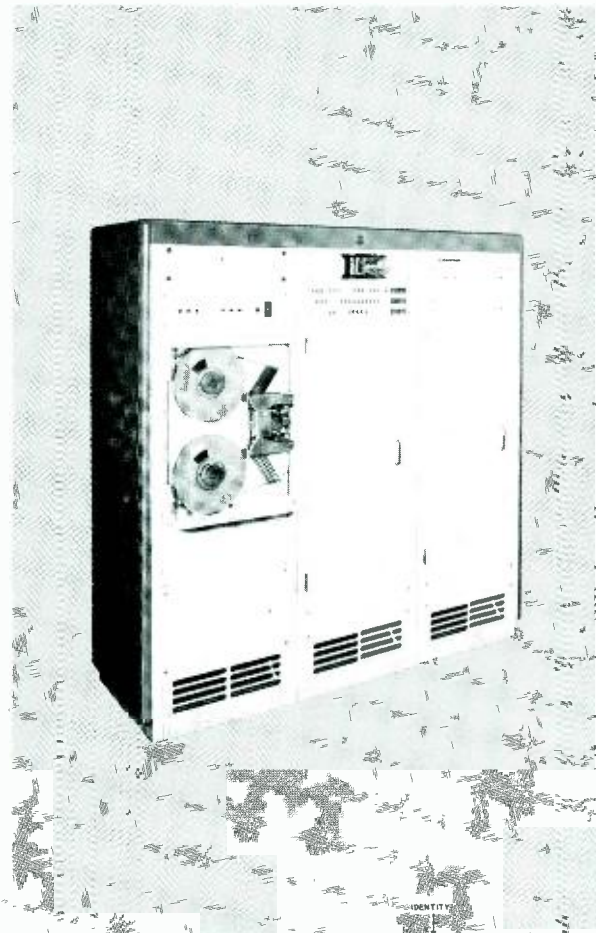


Fig. 3—The ADR analog racks; inset diagram shows equipment included.



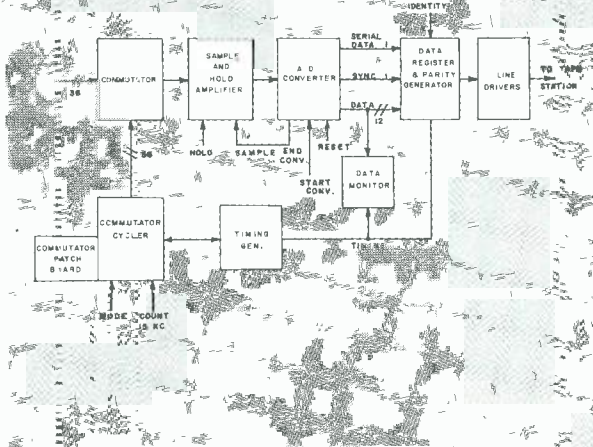


Fig. 4—The ADR digital racks; inset diagram shows equipment included.

The Automatic Data Recording System (ADR), designed and manufactured by RCA Electronic Data Processing for the Naval Propellant Plant, Indianhead, Md., is a custom installation of analog, digital, and control subsystems. The ADR system functions as an integral part of the Naval facility in research and development testing of solid-propellent engines. During such testing, the ADR system synchronizes and controls the operation of the entire facility, monitors the test, and provides both analog and digital recording of the test data. Data output of the ADR system is fed to the Propellent Plant's RCA 501 Computer for reduction and analysis.

THE AUTOMATIC DATA RECORDING SYSTEM (ADR), illustrated in Figs. 1 and 2, accepts analog inputs from 36 transducers such as thermocouples, strain gages and accelerometers which monitor the engine under test.

The *analog subsystem* provides the required signal conditioning to convert the transducer response to accurate high-level voltages. These voltages are then used as inputs to the digital subsystem and may be graphically recorded on an oscillograph.

The *digital subsystem* samples the many incoming analog signals in a preprogrammed pattern and accurately digitizes the samples. The operating rate is 15,000 samples/sec; digital outputs are arranged in a format suitable for acceptance by an RCA 501 computer and are recorded on an RCA 581 magnetic-tape station. After performance of the test, the magnetic tapes are read back into the RCA 501 computer installed at the Naval Propellant Plant and data is analyzed to evaluate engine performance. The overall data inaccuracy is designed to be less than ±0.05 percent and actual operating results are often as low as ±0.02 percent.

The *control subsystem* is a programmed sequencer and control center for directing and synchronizing the many operations in the test bay and in the analog and digital subsystems. The console provides 1) automatic operation of the entire test cycle, 2) immediate display of abnormal conditions and, 3) means for the operator to rapidly override all major equipments.

ANALOG SUBSYSTEM

The analog system (Fig. 3) has inputs consisting of strain gages, thermocouples, accelerometers, and breakwire sensors. The voltage signals from strain gages and thermocouples are low level (on the order of millivolts). Such signals are not suitable for driving all of the succeeding equipment and must be amplified by highly linear, stable, and reliable amplifiers.

The calibration equipment operates on demand and applies to each of the strain-gage inputs a series of known resistances and to each of the thermocouple inputs a series of known voltages. The signal is sent through the entire system and the final digital value is monitored. The ouput signal derived from this known input may be used as a scale factor to calibrate data taken from an actual test. Any of the analog inputs including the breakwire sensor voltages may be preserved on an analog recorder and all signals are sent to the digitalizing system. A patchboard is supplied to provide flexibility in making the desired interconnections.

The most crucial and complex technical problem in the entire system is that of spurious signals in the analog system. These spurious noise signals arise from a variety of sources, are difficult to control, and often have greater amplitudes than the desired signal. A distribution of system error allowances requires that the noise be attenuated to a level resulting in no more than ±0.015-percent error. The required total noise-attenuation factor is about 10,000:1 and, for specific cases (such as 60-cycle common mode voltages), the required attenuation is 1,000,000:1.

Unwanted noise signals must be treated by both preventive and curative controls. Prevention is accomplished by means of circuit isolation, proper grounding techniques, shielding and careful material selection. These measures attenuate the unwanted errors. Curative measures consist of common-mode rejection and filtering techniques used to separate the wanted from unwanted signals and to reject the latter.[1]

In the Naval Propellant Plant installation, most of the input lines may carry significant signals from DC to as high as 10,000 cycles. Under these circumstances, the impulse and AC power noise cannot be reduced by filtering and multiplexing of the low-level primary signal at the required rates is not feasible. For these reasons, each input line is amplified by a high-gain, low-noise amplifier. The selected commercial amplifier has a floating differential input, thereby preventing spurious currents through ground returns; a high degree of common-mode rejection is provided.

Input lines are twisted pair with efficient shielding. The shields are carefully insulated and are grounded at only one location. The input lines are not carried through conventional patch panels to the amplifiers, but are wired directly to the amplifier inputs. Monitor taps are carried to the patch panel for test and setup purposes. The amplifiers are interchangeable, and the low-impedance amplifier outputs are carried in miniature coax to patch panels, carefully designed to prevent undesirable common grounds in the output circuits.

Full consideration was given to all preventive and curative measures for the Naval Propellant Plant installation. The results in terms of system accuracy and stability (±0.02 percent for 6 hours) have fully justified the design criteria.

DIGITAL SUBSYSTEM

In the digital data system (Fig. 4), the amplified and filtered signals from incoming lines are sampled at a rate up to 15,000 data-points/sec. Lowpass filters, located in the analog racks, are used to strip out undesirable frequency components before sampling. This is done in order to prevent *aliasing errors* caused by sampling at a rate lower than the *Shannon limit* (two times the highest frequency component). The filters must offer very flat response in the passband and a high cutoff rate (30 db/octave). The design of such filters is complex and the testing is even more difficult.[2] The passive filters manufactured for RCA were based on designs initially prepared by Frank Brock of the microwave group of the RCA Broadcast and Communications Products Division, Camden. They were proved satisfactory in all respects. Each input line is sampled in a programmed sequence and each sample is converted into a binary number permitting highly accurate recording of original data.

A. S. BUCHMAN graduated from Cornell Univ. in 1948 with degrees in Mechanical and Administrative Engineering, and later completed studies toward an MS in Physics at Drexel Institute of Technology. Associated with Shallcross Manufacturing Company until 1954, he was Chief Development Engineer with responsibility for developing processes and automatic machinery. He was later employed by Ford Instrument Company as Principal Engineer where he designed special-purpose analog computers and airborne reconnaissance systems. With RCA since 1957, Mr. Buchman has designed airborne optical systems and studied the applications of magnetic, optical, infrared and ultrasonic techniques to industrial control problems. With RCA Electronic Data Processing, Mr. Buchman specialized in real-time digital systems. He was responsible for an intensive study of data collection for the Princeton University Stellarator. As one of the first members of the EDP Industrial Computer Systems Department, he was responsible for systems and application engineering and for the design of input-output systems for real-time process-control computers. Now, in the DEP Aerospace Communication and Controls Division, Mr. Buchman is responsible for advanced computer systems, which includes both investigation of advanced digital techniques and systems and application analysis.

The commutator performs the sampling cycle through the incoming lines in either of two desired modes: 1) any selected line is sampled continuously, and 2) lines are sampled in a programmed sequence set up by the operator. Each data sample is sustained in the *sample and hold unit* while it is quantized into a 12-bit binary character in an analog-to-digital converter.

To permit the 12-bit binary characters to be recorded in a desirable format, each 12-bit character must be broken into two 6-bit characters. An extra, or parity, bit is added such that each resulting 7-bit character will consist of an odd number of bits. Thus, each 12-bit character is converted into two 7-bit characters of odd parity. In each 1/50-second interval, elapsed-time and identity information characters are inserted in the data. Completely encoded information is sent to the digital tape station.

The digital system has three features of special interest. One is the coupling between the analog and digital sections. To prevent noise in the digital system from feeding into the analog system, special isolation is provided. All data lines are transformer-coupled between the analog-to-digital converter and the data registers. Further, the ground circuits in both the analog and digital sections are isolated from frame and chassis; such grounds are made common only at the attachment point to a grounding rod located near the installation.

A second feature of importance is the *commutator programmer*. The commutator consists of 36 electronic switches, each connected to one of the analog input lines. Switches are normally open and may be individually controlled to close upon receiving an electronic signal. The signals controlling the 36 switches are derived from a train of pulses occurring at a 15-kc rate.

These pulses must be distributed to the 36 channels such that individual channels can be sampled at rates of 5,000, 500, 250, or 50 samples/sec. Proper operation requires that only one switch be closed at a time and that sampling-rate assignments (programming) be established quickly and without error. In RCA's ADR design, these requirements are fully satisfied. Programming is performed merely by patching one cord for each input line into a hole for the desired sampling rate. All problems of proper interlacing of signals as well as remaining within the required 15,000-sample/sec rate are automatically accounted for.

The third major feature in the digital area is the *data monitor*. When a channel to be monitored is selected by the operator, the programming signal for that channel triggers the data monitor which stores the digitized channel value in a counting register. Slow-speed 100-kc pulses are applied to count this register to zero while the same pulses are counted upward from zero in a decimal-display counter. Thus, in 100 μsec, the decimal counter will display the proper value with a resolution of 1 part in 10,000. As long as a channel is selected, the data monitor will continue to update to display current data.

CONTROL SECTION

The ADR control group is the central command agency for the entire installation. The control group includes: 1) a master timer for generating all timing and synchronizing signals; 2) the subsystem control panels which direct the test site, analog and digital data systems; and 3) a central supervisory panel. All of these controls and panels are grouped on the control console where they may be readily monitored and adjusted by the operator.

Automatic control is provided to sound warning horns, check safety circuits, start high-speed cameras, and provide ignition pulses for the rocket motor. In addition, the data system is completely and automatically calibrated prior to performing a test; the oscillographic recorder is automatically operated at an appropriate speed for each stage of testing. The digital subsystem, including the tape station, is automatically set to an initial condition and is started at the beginning of calibration. It is then stopped and again started when ignition current begins to flow. This system is turned off automatically at the completion of test.

The supervisory control console is shown in Fig. 5. The panel on the left contains the master power switches, the voltage supply monitor, a special engine-igniter test unit and an intercom for communication from the block house to the test bay. The center panel (from top to bottom) provides the real-time data display and the switches to select the channel to be displayed. Complete controls and alarm indicators are provided for the tape station and oscillograph.

The next row includes pretest controls, count-down clock, and home controls which permit manual operation of specified equipments. The lower part of this panel provides the test *start* and *stop* controls. Many interlocks and safety features are provided to ensure against inadvertant firing and to accurately time this operation.

The panel on the right selects accurate *start* and *stop* times for cameras and other devices; these times are referenced to t_o (the time of application of ignition current) and are selectable from 50-seconds-before-t_o to 100-seconds-after-t_o. Octal switches at the bottom of this panel select an identification code interlaced with real-time information and recorded on the digital tape fifty times a second. All timing signals for facility synchronization and countdown are generated in and distributed by the control subsystem. The arrangement of controls and indicators is based on hierarchy of control. This places the lowest level of local control at the operating equipment and concentrates supervisory controls and summary reports at the control console. In turn, those controls requiring the least attention are located on the left and right panels and the master controls are concentrated on the center panel. The functions performed by the controls have been carefully selected to permit the operator to maintain complete control of the facility without burdening him with performing routine tasks.

OPERATIONAL EXPERIENCE

The ADR system was designed, manufactured and passed on-site acceptance tests within eight months after the date of order. During the initial warranty period, the equipments were operated by the customer in approximately 100 test firings. No problems were severe enough to warrant service calls. At the end of this period, minor logic changes were made by RCA and considerable effort was expended by the customer in correcting problems in primary power sources and other customer-supplied segments of the facility. The ADR system has greatly enhanced the usefulness of an important government facility and justifies the careful engineering planning and design.

ACKNOWLEDGMENT

Recognition for work on this project is due to three groups: 1) the RCA Engineering Group, consisting of Project Engineer L. W. Honens, J. Goveia, K. Ronan and many others; 2) the RCA Production group, which under Fred Smith built a professional piece of gear from rough sketches; and 3) the NPP staff, who cooperated and aided in every step of design and construction. Particularly, the help of K. Carr, B. Meers and W. Allison was appreciated by all who worked on the ADR System.

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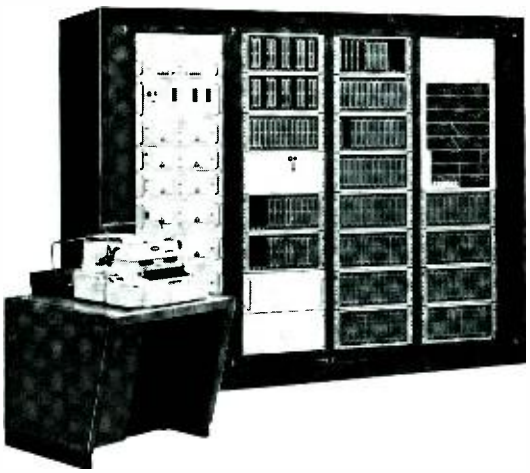

THE RCA 4100 SERIES MILITARY DIGITAL COMPUTERS

At top left, the RCA 4101 data processor, military designation CP-685/GPQ, is designed for real-time radar data-processing and control applications. It is constructed on swinging doors intended for van-wall or shipboard-bulkhead mounting and is designed and built to a combined military specification based on MIL-E-16400C, MIL-E-4158B, and XEL303. Several RCA 4101 Digital Computers are in service with RCA MIPIR radars (Missile Precision Instrumentation Radar) in van and shipboard installations on the Atlantic Missile Range and another is scheduled for service on the Pacific Missile Range.

At bottom left, the RCA 4102 data processor is designed for real-time data-processing and control service and general-purpose scientific applications. It is constructed on standard DEP racks and, like the RCA 4101, is designed and built to a combined military specification. The operator's desk, control console, and flexowriter are standard parts of the basic system, and buffer system, and buffer control units for conventional peripheral devices are available. The control panel provides the means for operator control of the central processing unit. It contains sets of indicators for displaying the CPU registers and a set of manual input switches for inserting information into the CPU. Controls are also provided to facilitate manual program tracing and computer maintenance.

The RCA 4100 Series Digital Computers comprise a family of systems designed for real-time control and scientific-data-processing applications requiring simultaneous execution of a number of different programs. The members of the RCA 4100 family, including the 4101, 4102, 4103, and 4150, are solid-state throughout, militarized, and similar in their mechanical, electrical, arithmetic, and programming characteristics.

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All of the RCA 4100 Series Computers feature multiple-function time-shared registers and use of the computer random-access core memory to store 96 *index registers* (the RCA 4150 has 112) and 16 *instruction-location counters* in addition to data and instructions. These features permit a significant reduction in hardware, resulting in machines having the computational power of large-scale data processors but the moderate cost and hardware complement normally associated with medium-scale data processors. The computers also feature a powerful instruction complement enabling programmers to execute simultaneous arithmetic, bookkeeping, test, and branching functions within single instructions. Another feature, common to all members of the family, is a 16-level priority-interrupt system which permits interruption of programs by higher priority programs initiated by external demands occurring at random intervals.

The computers automatically remember the status of any interrupted program and preserve its integrity; the computers return to the original programs even though "interruptions of interruptions" are iterated to a high degree of complexity. The priority-interrupt feature simplifies the scheduling of peripheral devices and permits acquisition of external data from randomly-active channels with short holding times. This is done without periodic scanning and status testing of input channels and the attendant reduction of computing time.

GENERAL DESCRIPTION

All members of the family are parallel, bus-organized machines, and all but the RCA 4150 utilize a binary fractional data word of 30-bit length. They incorporate random-access core memories ranging in size from 4,096 to 32,768 words. The memory read-write cycle time for a typical machine, the RCA 4102, is 5.5 μsec. Most short operations in the RCA 4102, such as addition, are performed in 16.5 μsec, which includes instruction and operand fetching. Indexing adds 5.5 μsec to this time. Multiplication is performed in 75.5 μsec. The RCA 4150 has all of the features of the others, but in addition, has a 36-bit word length, built-in floating-point instructions, and a more powerful instruction complement. Since it is quite different from the other members of the family in some respects, and has not yet reached the hardware development stage, it will not be discussed further in this article.

The machines are designed to handle conventional peripheral equipment, including a flexowriter, paper-tape readers and punches, card readers and punches, magnetic tape stations, and high-speed line printers. Typically, eight magnetic tape stations, four card readers, a card punch, and four line-printers can be handled by a Central Processing Unit (CPU) equipped with four control units. Moreover, different combinations of peripheral equipments or additional equipments may be obtained by adding control units. Peripheral devices such as flexowriters, which transfer data a word or less at a time instead of blocks of words do not require control units.

Standard software packages have been developed and are available for the RCA 4100 Series Computers. These packages currently include two symbolic language assemblers, a library of scientific com-

putation subroutines, input-output subroutines, floating-point subroutines, conversion subroutines, and debugging and maintenance programs. The following descriptions apply to the RCA 4102 Computer; variations relating to the RCA 4101 and the RCA 4103 are described as they are encountered.

MACHINE ORGANIZATION

The simplicity of the machine organization can be seen by reference to Fig. 1. The entire CPU centers around the 30-bit internal data-transfer bus; all register-to-register transfers within the machine are made via this bus. Most of the registers shown in Fig. 1 perform at least two functions; this partly accounts for the small amount of hardware required (less than 3,000 transistors for a 4,096-word machine, including core memory).

The *instruction register* staticizes the operation fields of the current instruction. The content of this register is decoded to implement the micro-operations necessary to perform the instruction. For input-output operations, part of the instruction-register content addresses peripheral equipment and controls suboperations in the peripheral equipment.

The *flag register* stores a bit for each priority level which must be serviced. Individual priority bits in this register are set by external devices demanding attention, or by internal programs signalling a desired transfer to another program. The most-significant set bit in this register determines the currently-active program.

The *demand register*, connected to bits 23 through 26 of the bus, contains the binary code for the priority currently active, and supplies part of the address of the instruction-location counter for the currently-active priority. This register is also used to address the external peripheral equipment channel of the corresponding priority number.

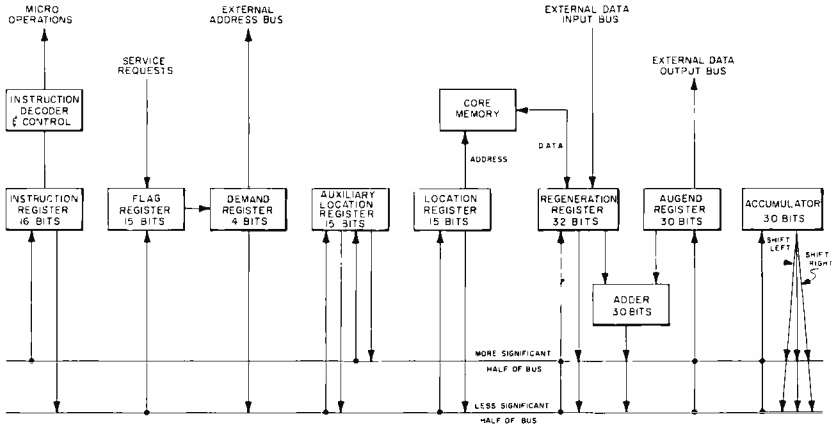

Fig. 1—RCA 4102 block diagram.

The memory used in the RCA 4100 Series Computers is a coincident-current magnetic-core memory with a 5.5-μsec read-write cycle. Standard memory sizes are 4,096 words expandable to 8,192, and 8,192 words expandable to 16,384. The RCA 4103 Computer, which is a special modification of the RCA 4102 to suit a particular application, has a 32,768-word memory. The additional addressing capability is obtained by modification of the operation field of the instruction word. The word length for the RCA 4100 Series Computers is 30 bits; however, two additional parity-check bits are included in the memory system to provide an odd parity check on each half-word for all core-storage transfers.

TABLE I—RCA 4102 Operations

Mnemonic	Instruction Name
ADD	*Add*
ADM	*Add Magnitude*
ADR	*Add and Replace*
ALA	*Shift AC Left, Algebraic*
ALC	*Shift AC Left, Circular*
ALL	*Shift AC Left, Logical*
ALX	*Add L to Index*
AMR	*Add Magnitude and Replace*
ANA	*AND to AC*
ANR	*AND and Replace*
ARA	*Shift AC Right, Algebraic*
ARC	*Shift AC Right, Circular*
ARL	*Shift AC Right, Logical*
DIV	*Divide*
DVH	*Divide Half-Word*
ERA	*Exclusive ϕR to AC*
ERR	*Exclusive ϕR and Replace*
FLS	*Flag Set*
HLT	*Halt*
IϕC	*Input Output Control*
JAC	*Jump on AC*
JIX	*Jump on Index*
JSX	*Jump and Set Index*
LDA	*Load AC*
LDϕ	*Load Output Word*
LDX	*Load Index*
LDZ	*Load Zero*
MPH	*Multiply Half-Word*
MPY	*Multiply*
NϕP	*No Operation*
ϕRA	*ϕR to AC*
ϕRR	*ϕR and Replace*
ϕRS	*ϕR to Storage*
PAX	*Place AC in Index*
PXA	*Place Index in AC*
SBM	*Subtract Magnitude*
SBR	*Subtract and Replace*
SKP	*Skip*
SMR	*Subtract Magnitude and Replace*
STA	*Store AC*
STI	*Store Input Word*
STX	*Store Index*
STZ	*Store Zero*
SUB	*Subtract*
TST	*Test Storage*
XAS	*Exchange AC and Storage*

The primary function of the *location register* is to hold the word address for all core-storage transfers.

The auxiliary location registers serves as an auxiliary address register during address modification; this occurs for indexing and branching operations.

The auxiliary location and location registers, together, perform as a multiplier-quotient register during *multiply* and *divide* operations. The auxiliary location register stores the more-significant half of the multiplier during multiply operations, and the location register stores the less-significant half. The auxiliary location register also stores the more-significant half of the quotient during divide operations, and the location register stores the less-significant half.

The *regeneration register* staticizes the core-storage word addressed by the location register. All transfers to or from the core storage take place through the regeneration register. The regeneration register also provides one input to the adder during logical and arithmetic operations, and acts as a slave to the accumulator during shift operations. Additionally, the regeneration register serves as an input register and all computer inputs enter this register.

The accumulator stores one of the initial operands and the final result of most arithmetic, logic, and shifting instructions. This register also provides complementing and shifting capabilities.

The *augend register* provides one of the inputs to the adder and also holds the multiplicand and the divisor during multiply and divide operations, respec-

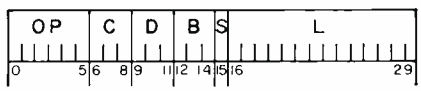

Fig. 2—RCA 4102 instruction word.

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tively. The augend register is connected to the computer output bus, and all output words leave the computer through this register.

The adder is not a register but a gating network which continually generates either the algebraic or the logical (modulo two) sum of the contents of the augend and the regeneration registers.

Not shown in Fig. 1 are the index registers and the instruction-location counters, since these registers are located in core storage. Each of the 16 priority levels has its own set of six index registers, an instruction-location counter, and a work space. Use of core-storage locations rather than the more conventional flip-flops as registers results in a significant reduction of the amount of hardware required. Moreover, priority interrupts are simplified because most information in use by an active program (all but the accumulator content) is already in core storage at the time of the interrupt; thus, complicated executive routines are not required to interrupt, hold, and re-initiate programs.

WORD FORMATS

All information in the RCA 4100 Series Computers is handled in parallel, binary words of 30 bits each. The data word is interpreted as a binary fraction using two's complement notation. The range of numbers that can be represented by the data word extends from -1 to $(1-2^{-29})$ (octal representation from *4000000000* to *3777777777*, respectively). The octal representation of the number 0 is always *0000000000* and never has a negative sign. The numbers outside this range are handled by appropriate scaling. The sign bit in a positive number is always *0*, and the sign bit in a negative number is always *1*.

Words used as instructions are interpreted according to the format shown in Fig. 2. The *OP*-code field, the *B* field, and the *L* field comprise a conventional instruction format found in single-address machines with indexing capability. The *OP*-code field (located in bits 0 through 5) controls the execution of 46 different primary instructions. Nine of these instructions are word transmission instructions, seven are logic instructions, six are shift instructions, twelve are arithmetic instructions, nine are control instructions, and three are input-output instructions. Table I shows the set of operations available with the RCA 4102. The *L* field, comprised of bits 16 through 29, represents the core-storage address of the operand to be fetched and operated upon. The *B* field specifies one of six index registers or the instruction-location counter. The sum of the number in the *L* field and the number contained in either the specified index register or the instruction-location counter forms the effective address of the operand. The effective address is the address of the word actually used in the execution of the instruction. If the *B* field specifies the instruction-location counter, as in relative addressing, the sum of the instruction-location counter content and the content of the *L* field becomes the effective address. Most RCA 4100 Series Computer instructions are indexable.

TABLE II—Normal C-Field Interpretation

C Value	Branch Condition	Subsidiary Function
0 (*D* even)	*No jump*	None
0 (*D* odd)	*No jump*	*Do not set Overflow Indicator*
1	*Initial Index Value = 0*	*Decrement Index*
2	*No jump*	*Decrement Index*
3	Final $C(AC) \geq 0$	None
4	Final $C(AC) > 0$	None
5	Final $C(AC) \neq 0$	None
6	Final $C(AC) = 0$	None
7	Final $C(AC) < 0$	None

A secondary instruction, specified by the *C*, *D*, and *S* fields, is included with all primary instructions. The *C* field, in most instructions, specifies conditions for branching and/or subsidiary functions that may be performed concurrently with the operation specified by the *OP*-code field. The normal branching conditions and subsidiary functions applying for most instructions are shown in Table II. The *C* field in input-output operations specifies the location of a peripheral device rather than a branch condition.

The *D* field determines the destination address if the branch condition specified by the *C* field is met. When this occurs, the content of the *D* field is added to the content of the instruction-location counter to yield a destination address. The value of *D* may range from zero through seven. When *D* is *0*, the current instruction is repeated if the condition specified by *C* is satisfied. Other *D* values, with a satisfied normal *C* condition, cause the computer to jump back *D* locations in memory to obtain the next instruction word. When used in conjunction with certain operation codes, the secondary instruction fields operate in other than the normal manner.

The *S* field is called the *suicide* bit. When *S* is *1*, the active priority flag is reset, thus ending the active program and starting the program with the next highest priority.

PRIORITY-INTERRUPT SYSTEM

The priority-interrupt feature of the RCA 4100 Series Computers serves a multiplicity of programs on a priority basis. The primary purpose of the priority interrupt system is to eliminate the need for program-controlled scheduling and status testing of input-output transfers.

The complete set of indicator flags is examined, simultaneously with the execution of each instruction, to determine which demanding program has the highest priority (Fig. 3). When the currently-active program has the highest priority of those demanding attention, the program proceeds without interruption. Otherwise, the system automatically transfers, at the completion of the current instruction, to the highest demanding priority.

During the priority-interrupt cycle, the machine logic ensures that the address of the next instruction of the interrupted priority is saved in its instruction-location counter. The only programming constraint is that each program affecting the accumulator content is responsible for restoring the original value. When all higher-priority demands are satisfied, control returns to the interrupted program, and the latter proceeds oblivious of the interruption. In this way, the priority-interrupt feature enables the computer to interleave a number of different programs.

Priority Assignment

Input-output routines for the RCA 4102 are generally short, and frequently consist of single instructions which do not affect accumulator content. After an input routine transfers data to memory, suitable programs are called on to process the new information. The various input-output and data-handling routines are assigned different priority levels. The priority-interrupt system automatically activates the proper program to process the new data transferred to the memory by other programs; therefore, the programmer need not perform periodic tests for the arrival of data.

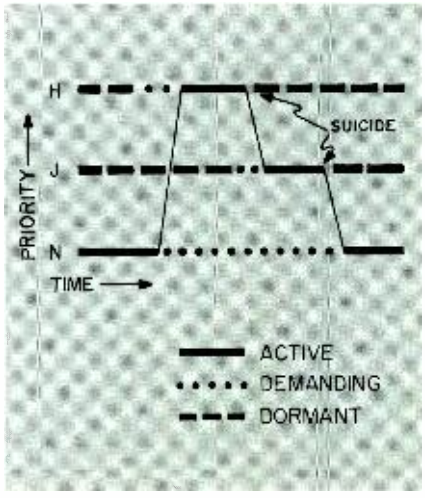

Fig. 3—Program interrupt example.

Because of these considerations, assignment of relative priority among the various input-output programs and devices is principally based on the allowable waiting time between data transfers. Computing programs are assigned lower priorities than those of input-output programs and computing priorities may be assigned arbitrarily, within this constraint, by the user. The lowest priority program, automatically executed when the flag register is cleared, is usually a self-check routine, which automatically exercises and tests the computer during idle time.

TIMING

Instructions in the RCA 4100 Series Computers are executed by sequences of micro-operations capable of clearing registers or transferring data to or from the bus, etc. The execution time of each instruction is divided into a number of status cycles. Each status cycle is subdivided into four, six, or eight ½-μsec time slots. A typical memory cycle (Fig. 4) consists of six time slots. During the first time slot, the address is placed in the location register and a read command is issued. Data are transferred from core storage to the regeneration register before the start of the third time slot. When the transfer is complete, a read echo signal is delivered by the memory to the computer control and timing circuits. During the time between the second time slot and the read echo signal from the memory, the computer clock hesitates, if necessary, to maintain synchronism. The read echo signal starts the third time slot. In the fourth time slot, a word to be placed into core storage is placed in the regeneration register (it could be the word already there as a result of the read operation) and a write command is issued to the memory.

When writing is complete, a write echo signal is delivered by the memory to the computer control and timing circuits. The computer clock again hesitates after the sixth slot, and is started by receipt of the write echo signal. All of the time slots shown in Fig. 4 are used in the execution of various micro-operations in addition to those which control memory access. A register can be set, cleared, or have its content transferred to another register in one time slot. Processing of a word read from memory to the regeneration register takes place during the third, fourth, fifth, and sixth time slots for all short instructions. Subsequent status cycles are required for processing of the word for long operations such as shifting, multiplying, and dividing.

As shown in Fig. 5, all RCA 4102 instructions start with a memory cycle to fetch the instruction. Prior to the start of the memory cycle, the address of the instruction is in the auxiliary location register. During the first time slot of this cycle, the address of the instruction is placed in the location register and a memory read cycle is started. This transfers the instruction from core storage to the regeneration register. Then the address bits of the instruction are transferred to the auxiliary location register and the operation bits are transferred to the instruction register to be decoded.

If indexing is required, as determined by the content of the *B* field in the instruction, another memory cycle occurs. During this memory cycle, the called-for index register is delivered to the regeneration register and the base address which is in the auxiliary location register is transferred to the augend register. The content of the index register is added to the base address in the adder and the sum is delivered to the location register to form the effective address. If indexing is not required, this cycle does not occur.

A third cycle (or second, if indexing is not required) takes place whenever an operation is to be performed on an operand located at the effective address. During this cycle, the operand is transferred from core storage to the regeneration register and the operation called for is completed (for short operations). For MPY, MPH, DIV, DVH, and XAS operations, this cycle is divided into eight time slots.

For long operations, such as multiplication, division, or shifts, additional status cycles are required. These status cycles do not require memory interrogation and are subdivided into four or eight time slots, depending upon the operation required. From zero to 16 of these additional status cycles may be required depending upon the instruction.

The execution of the operation called for by the operation field of the instruction is followed by a memory cycle in which the instruction-location counter is updated. This cycle is common to all instructions. The address of the memory location which contains the instruction-location counter is formed in the location register and a memory read cycle is started, delivering the instruction-location counter content to the regeneration register. Simultaneously, the branch control is set if the conditions specified by the *C* field and the result of the operation are met.

The augend register is set with the proper decrement as determined by the *C* and *D* fields of the instruction. The modified instruction location formed by the adder is transferred to the auxiliary location register, then returned via the regeneration register to core storage. Toward the end of this status cycle, the priority-interrupt flags are examined to determine the highest set priority. If the highest set priority is equal to the content of the demand register, then the program proceeds uninterrupted and the next status cycle, which is the first cycle

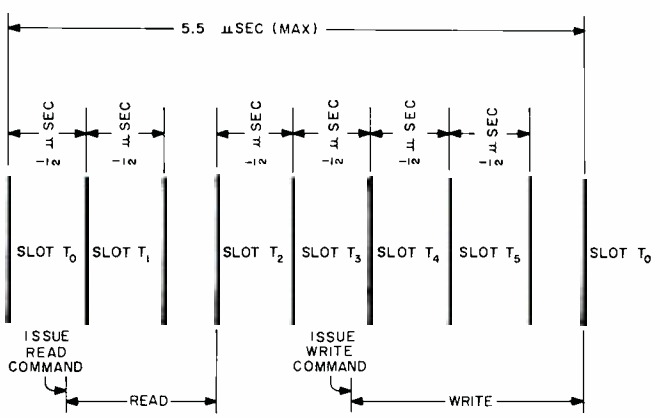

Fig. 4—Basic memory-access status cycle.

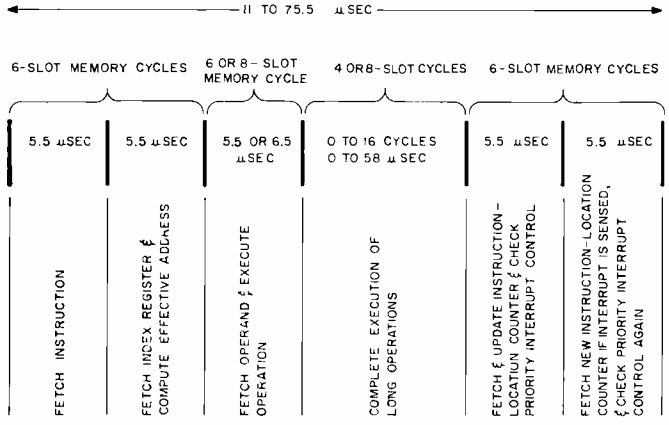

Fig. 5—Basic instruction status-cycle sequence.

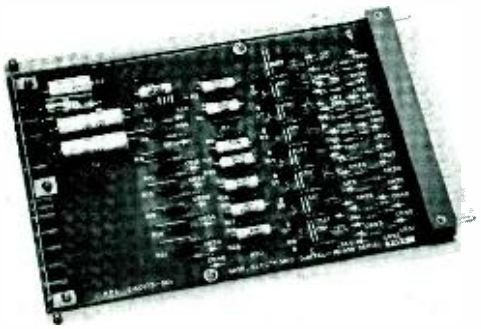

Fig. 6—RCA 4100 series logic module.

of the next instruction, proceeds as already described. Otherwise, another status cycle takes place which transfers to the auxiliary location register the content of the instruction-location counter associated with the interrupting program. Then the machine proceeds with the next instruction.

INPUT-OUTPUT

External devices, such as data links, radars, analog-digital converters, telemetry channels, and teletypes, requiring attention at random and unpredictable intervals, are connected to the RCA 4100 series CPU's by means of the regeneration register and the augend register with little or no intervening buffering or control logic. Each channel is assigned its own priority and the computer will handle up to 14 such channels. More than one device (up to eight) may be connected to a single priority level, provided only one at a time requires servicing. Each device generates a service-request signal whenever it is ready for the transfer of a word to or from the CPU. This service request sets a preassigned priority flag in the computer. The routine executed in this priority contains a single-instruction loop to perform the required data transfer. The single instruction (STI or LDϕ) is executed once in response to each service request, transferring one word to or from memory, and returning control, by means of the *S* field, to the computing routines. Using an index register to tally the service requests, the program can automatically notify another routine whenever a predetermined number of words has been transferred. This automatic notification relieves the program of any need for schedule control or periodic status-testing in the servicing of peripheral devices.

When several devices or channels are connected to the computer, each responds only to STI and/or LDϕ instructions executed in the priority level assigned to the device. The active-priority code, held in the demand register, thus serves as a peripheral channel address for input-output communication.

Other devices, such as flexowriters and perforated-tape equipments, communicate single computer words or less in response to each programmed control command. Communication between the RCA 4102 CPU and such a device is similar to that described above. The distinction lies in the need for a command from the CPU to control the operation of the device. This command is encoded into the *C* field of the STI or LDϕ instruction which performs the data transfer. For example, an LDϕ instruction, which orders the transfer of data to the flexowriter, simultaneously directs whether the data should be punched or typed, or both. After each service request has been processed, and when the device is ready for the next data transfer, the device sets its priority flag, automatically notifying the CPU. Several similar or dissimilar devices can be time-shared on a common priority level, provided no ambiguity or conflict arises in the interpretation of the *C* fields of the input-output instructions. As many as eight input or eight output devices can thus be serviced by each priority level. In this case, the *C* fields of the input-output instructions become a subsidiary peripheral address, supplementing the active-priority code for selecting and controlling peripheral devices.

Input-output devices which communicate blocks of data to and from the CPU, such as magnetic tape stations, line printers, and punched card equipments, use control units between the devices and the CPU for efficient communication. A number of similar block-transfer devices may communicate with the CPU through a single control unit. Each such control unit is connected to a specific CPU priority level, in which all data transfers (STI and LDϕ) for this control unit are executed.

Control commands, for directing the action of these block-transfer control units and their associated devices, are issued from the CPU by means of an IϕC instruction. The IϕC instruction, which may be executed in any priority level, transmits to the peripheral equipment a 15-bit control command which identifies:

1) Priority level of the control unit addressed
2) Specific device to be selected (if necessary)
3) Action to be performed
4) Type of data block

Once the action has been initiated, and for the duration of the specified data block, any required data transfers are performed as already described for word-transfer devices.

At present, control units have been designed and are available for the following: the RCA 381 high-data tape group, an IBM compatible tape station, a high-speed line printer, a card punch, and a card reader. These control units are module nests or groups of nests housed in one, two, or three-rack complexes called input-output equipment control cabinets. The cabinets provide a standard operating environment including common power supplies, blowers, cable assemblies, and common interface logic for several control units. A different control unit is required for each type of block-transfer device; however, one control unit will handle several devices. For instance, only one control unit is required for all six tape stations in the RCA 381 high-data tape group; the line-printer control unit will control up to four line printers; and the card-reader control unit will control up to four card readers.

LOGIC IMPLEMENTATION

The logic building block of the RCA 4100 Series Computers is a *nor* gate—a diode-coupled, diode-biased, grounded-emitter amplifier, combining the advantages of high fan-in, high fan-out, and restandardization of signal levels. Use of this type of gate results in noise-insensitive operation and simplicity of maintenance. High fan-out is achieved, with moderate power drain, through the use of silicon diodes as a nonlinear base resistor. The high storage of these "stabistor" diodes and the polarity of the logic diodes provide compensation for transistor charge storage effects. The gate output is clamped to speed output signal-level transitions and to provide a uniform signal level throughout the system. The worst-case signal delay through an *and/or* pair of these *nor* gates is less than 50 nsec. This standard gate is the only logic element used throughout the entire CPU. The gates are packaged eight to a module board and the entire CPU uses only 12 different types of module boards, including all of the memory boards. Over 70 percent of the module boards used in the CPU are of the type which holds the standard logic elements. A photograph of this board is shown in Fig. 6.

ACKNOWLEDGEMENT

The RCA 4100 Series Computers were the original work of a team of engineers headed by W. E. Woods, a Staff Engineering Scientist of the Data Systems Division, Van Nuys, California. While a great many engineers participated in the successful execution of this program, the primary contributions were made by H. Zieper, W. Helbig, and C. S. Warren.

AEROSPACE MICROMOD COMPUTER

Micromodules, interconnected with welded wiring, have made possible this general-purpose core-memory binary digital computer in an 0.6-cu ft unit weighing 30 lbs. It is a parallel machine operating in real time, with a 30-bit word length and a 1-Mc clock rate.

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SPACE TECHNOLOGY demands sophisticated guidance and control systems using computers with high-capacity memories and high computational speeds for solutions in real time. Concurrently, the requirements for extremely high reliability combined with low power, size, and weight are vital.

Simple analog computers of limited accuracy, digital differential analyzers (DDA), serial-drum general purpose machines—and random-access, high-speed, general purpose computers are currently available. Unfortunately, the random-access type, although more desirable from the standpoint of capability, is also usually highest in power consumed, size, and weight. The *Aerospace Micromod* (AM) computer overcomes the power, size and weight problems by using the micromodule packaging technique and careful logic design.

The ACCD series of computers started with the general-purpose STREAC computer, designed in 1957 for an advanced interceptor application. Using the same type of circuits, the computer engineers then conceived, built, and flight-tested a DDA type computer called the AM1100, for application to an Army navigational system. Next, a general-purpose computer was designed in 1961 to demonstrate the feasibility of a medium-range missile concept—and to demonstrate the feasibility of building computers using micromodules. One-half of the arithmetic section of this computer was successfully micromodularized; the AM computer described in this article grew out of that program.

GENERAL DESCRIPTION

The AM is a general-purpose, digital, core-memory, parallel, 30-bit, binary computer; it is packaged for aerospace environments in a 0.6-cu ft unit weighing 30 pounds. Micromodules are interconnected by welded wiring and surrounded by a rigid "egg crate" mechanical assembly which serves as an effective heat conduction path; power consumption is about 100 watts. The AM computer operates in real time, normally processes data to and from inertial devices and control mechanisms to provide a guidance function, handles telemetry requirements, operates specialized input devices, accepts and delivers analog and discrete information to missile subsystems, and participates in ground alignment and subsystem checkout. Table 1 summarizes the AM computer characteristics.

INSTRUCTION COMPLEMENT

One of the best ways to evaluate a computer's features, size and programmability is to inspect a list of available instructions. A rich instruction complement not only aids program writing, but enables the memory to be packed more efficiently, resulting in a smaller memory size. In aerospace applications, particularly, memory size must be minimized; of course, a balance must be struck between reductions in memory sizes and increases in arithmetic and control circuitry. Fig. 1 shows the complete instruction complement for the AM computer, including execution times; total times include access time to the program memory. Most of the instructions (see Fig. 1) are straightforward and common. A fairly unique feature, however, is the inclusion of *square root* as an instruction rather than a subroutine.

Square-Root Instruction

In the missile application for which the computer was configured, the use of square-root in tight, real-time loops virtually forced abandonment of a relatively short subroutine in favor of the programmable square-root instruction.

The square-root algorithm is designed to follow the "paper-and-pencil" method in its broad outlines, taking advantage of existing computer transfer paths. In the binary paper-and-pencil method of determining square root, the "answer so far" must be multiplied by four (two times the base of the number system) before trying the next digit; in the decimal method, the answer-so-far would be multiplied by twenty before trying the next digit.

In the binary system, the process is considerably simplified because it is easy to multiply by four (two left shifts) and because, with the base two the next trial digit is always a one. Furthermore, advantage was taken of the two's complement storage system for negative numbers. Since the squared trial digit is always *01* tacked on to the answer-so-far, the subtracting process and the formation and storage of answer digits can be combined in the memory register. Initially, that register is set to all *1's*, which is the two's complement of *0.00 . . . 0.1*.

A trial subtraction from the two most significant bits of the operand will show whether the root bit is a *0* or a *1*. The answer is then posted in the third least significant digit of the memory register as the complement of the true root bit. When two more digits are shifted into the accumulator, the memory register will hold the previously determined root bit multiplied by four and two's-complemented. The process is iterative until all root bits are determined. A final complementing step restores the root bits to their true form and the least significant bit is set to a *1* as an unbiased rounding step. A 30-bit operand thus produces a 30-bit square root, rounded.

Divide and Multiply Instructions

The AM computer departed from the division algorithm used in the earlier computers in one interesting respect, thereby reducing the execution time considerably.

Earlier design had implemented the *divide* instruction using a non-restoring algorithm wherein a subtraction or an addition of the divisor to the shifted dividend was always performed; the choice between addition and subtraction depends on the last quotient bit. The procedure would appear to be the most effi-

TABLE I—Summary of Computer Characteristics

Type

General-purpose, binary, parallel, 30-bit word length, 1-Mc clock rate

Arithmetic Data

3 index registers
24-μsec *add* time (incl. memory access)
102-μsec *multiply* time
108-μsec *divide* time
192-μsec *square root* time

Memory

4,096-word 18-bit program memory
1,536-word 30-bit data memory
(Both coincident-current core type)

Circuits

Resistance-coupled complementary transistor logic circuits
Silicon semiconductors

Packaging

Micromodular, with welded wiring

Fig. 1—RCA's AM computer instructions.

PERTINENT REGISTERS AND MEMORY LOCATIONS

A — 30-bit accumulator
B_X — 11-bit index registers (3)
Q — 30-bit Q register
d — 1 of 1536 data memory locations (word length 30 bits)
p — 1 of 4096 program memory locations (word length 18 bits)
(A), (d) signify contents of A, contents of memory location d, etc.

A three letter command designation (e.g., MAP) signifies a micro-instruction. Micro-instructions are coded by the 11 least significant bits of the program word.

Designation	Code	Explanation	Time (μsec)
BASIC INSTRUCTIONS			
AD d	20	Add (d) to (A)	24
SU d	21	Subtract (d) from (A)	24
MU d	10	Multiply (d) by (A)	102
DV d	11	Divide (A, Q) by (d)	108
SQ	12	Find square root (A)	192
EX d	24	Extract (A) per (d)	24
DATA TRANSFER INSTRUCTIONS			
CA d	22	Clear Add: Transfer (d) into A	24
ST d	26	Store (A) in d	24
TD d	15	Transfer n word Data block from p memory to d memory	12+24n
BLV	00X0036	Block Load or Verify (Inputs or verifies six-word block)	108
REGISTER MODIFY INSTRUCTIONS			
SB_XD	31,32,33	Set B to value of d	24
CLA	00 00210	Clear A	12
CLQ	00 00710	Clear Q	12
XAQ	00 00410	Exchange A and Q	12
AQA	01 00003	Add (A) + (Q) into A	24
AQQ	01 00006	Add (A) + (Q) into Q	24
LAQ	01 00001	Logical sum (A) + (Q) into A (No carries)	24
RND	02 00006	Round (A) per (Q)	12
MAP	02 00214	Make (A) Positive	12
MAN	02 00105	Make (A) Negative	12
AOA	02 00304	Add 1 to (A)	12
OCA	02 00400	One's Complement (A)	12
TCA	02 00704	Two's Complement (A)	12
JUMP INSTRUCTIONS			
(JU, JI and JN instructions have 11 bits to designate p; therefore, jumps are confined to the 2048 section of the p memory in which operating)			
JU p	06	Jump Unconditionally to p	12
CLP	00 00000	Clear Program address register; i.e., jump unconditionally to program address zero	12
JE d	14	Jump Exit: instruction in p and p+1. Jump to (p+1). Store p+2 address in d.	36
JR d	25	Jump return to address designated by (d), which may be result of previous JE instructions.	24
JI_Xd	35,36,37	Jump (Index) to d if (B_X) = 0. Otherwise continue. Decrement (B_X)	24
JN p	04	Jump to p if (A) is Negative. Otherwise continue.	12
SHIFT/ROTATE INSTRUCTIONS			
(A single shift instruction provides for shifting A and Q up to 15 bits. The number of shifts is specified by mn where m = 1 signifies 8 shifts and n = 0 to 7 shifts. Execution time varies from 12 μsec for 0-3 shifts to 36 μsec for 13-15 shifts.			
LLS	03031 mn	Logical Left Shift A and Q mn bits in closed ring, i.e., rotate (Sign shifted)	
ALS	03001 (2+m)n	Algebraic Left Shift A and Q mn bits. Zeros enter right side of Q (Sign unchanged)	
LRS	03015 (4+m)n	Logical Right Shift A and Q mn bits. Zeros enter left side of A	
ARS	03035 (6+m)n	Algebraic Right Shift A and Q mn bits.	

cient in time. Because of the double-rank technique used for the accumulator, and the necessity of shifting left after every addition or subtraction, a "restoring" algorithm was worked out to look ahead at the subtraction and sense whether or not an overflow would occur; then either the subtraction or an accumulator-restoring downshift was performed. When the influence of faster carry-gates was added to the new algorithm, the divide execution time was shortened from 300 μsec for the original 24-bit word length to 108 μsec for the 30-bit-word-length AM computer.

The *multiply* instruction, taking advantage also of the carry-gate speed, was reduced from 168 μsec for the original 24-bit word length to 102 μsec for the 30-bit AM computer.

Transfer Data Instruction

The use of two memories creates a need for transferring constants from the program to the data memory under program control. The *transfer data* instruction satisfies this need by providing variable-length block transfer; the sequence is halted by sensing for an all-zero constant.

MAJOR AM DIVISIONS

In Fig. 2, four main divisions are shown: 1) *memory*, 2) *arithmetic*, 3) *control*, and 4) *in-out*.

Memory Section

The memory section of the computer (see Fig. 2) has two separate coincident-current core memories that communicate with the rest of the computer through a single memory register. The program memory has a capacity of 4,096 words of 18 bits, and the data memory a capacity of 1,536 words of 30 bits.

Most aerospace applications require that the program and constants be stored in a memory in which a momentary power loss does not destroy the stored information and in which the memory reading process does not destroy the information read. A memory possessing these two properties is called *nonvolatile* and *nondestructive*. It is also advantageous when this memory can be electrically loaded rather than permanently wired, and be made all-electronic rather than electromechanical.

By providing two separate memories, the AM computer facilitates the substitution of the latest developments in the memory state-of-the-art as they become available. The program memory core can thus be removed and replaced whenever a nonvolatile, nondestructive device develops as a result of future research. Transfluxors are now available and practical, but their physical size is still too large to permit use in the AM computer. The first use of a transfluxor memory in computers was made in the RCA STREAC.

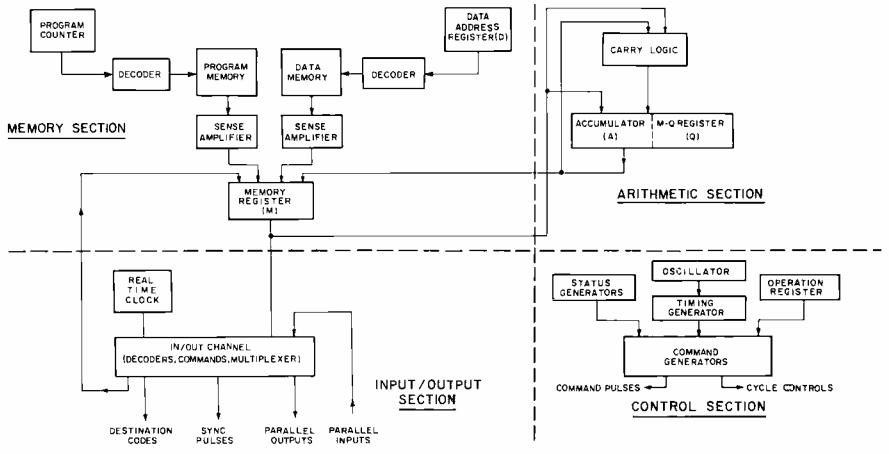
In addition to built-in flexibility for accommodating different program memory devices, the AM computer is designed to allow connection of both an external back-up memory and a manual plugboard memory. The external back-up memory is used for ground checkout of the missile subsystems, since functions useful only on the ground need not contribute to space-borne weight. The 64-word manual plugboard memory facilitates program debugging when used in conjunction with other controls in the checkout and control equipment.

The data memory is the working store for intermediate results. Content of the data memory must be changed in flight; therefore, a standard core memory must be used for this purpose. Advantage cannot be taken of transfluxor-like devices.

The Arithmetic Unit

The arithmetic unit is composed of three main parts: the *accumulator*, the *multiplier-quotient register*, and the *carry-gates*. In arithmetic operations, the memory register usually holds one of the operands, thus becoming a part-time mem-

Fig. 2—Simplified block diagram of the AM computer.



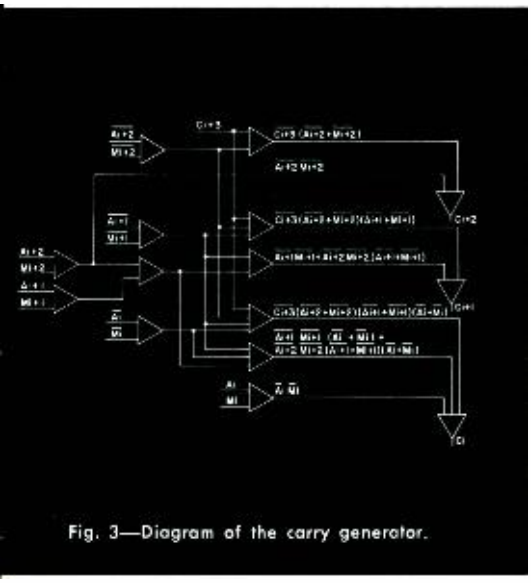


Fig. 3—Diagram of the carry generator.

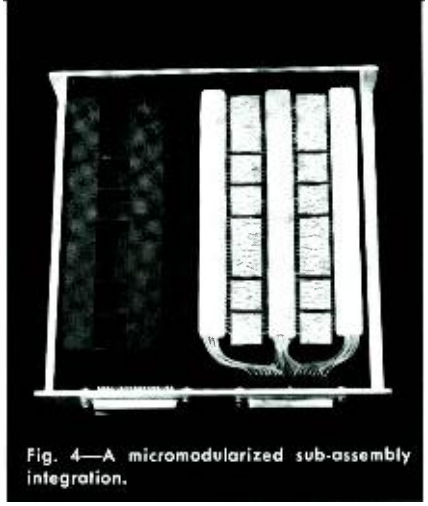


Fig. 4—A micromodularized sub-assembly integration.

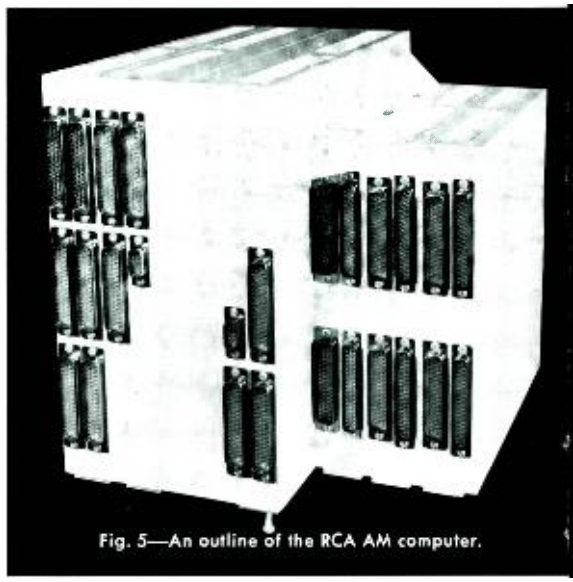


Fig. 5—An outline of the RCA AM computer.

ber of the arithmetic unit. The data address register is in the same category; its main functions are to address the data memory and serve as a temporary storage register during the square-root instruction.

The accumulator and the multiplier-quotient register are both double-rank, using the concept of "master-slave" control during transfer so that all race conditions are eliminated without resort to delay-line techniques. Both function as a single 60-bit unit during the shifting instructions, and in the multiply, divide, and square-root instructions.

The accumulator accomplishes all of its arithmetic functions by its ability to complement, add, to shift up and down, and to shift left and right.

The multiplier-quotient register holds the multiplier during the multiply instruction; at the end of the instruction it contains the 29 least significant bits of the double-length product. In the divide instruction it forms the quotient bits. Additionally, it is used for temporary storage.

A group size of three is used in the carry generator and "look-ahead" between bits in the group is employed; no look-ahead occurs between groups. The design results in seven pair-delays for a 30-bit carry generator; this delay is small enough so that all carries are propagated in less than one microsecond.

Fig. 3 shows one group in the carry generator; *nor* logic is employed, with circuits having a maximum fan-in of four and maximum fan-out of three. In conjunction with the logic shown, a technique of inverse carries in alternate groups results in a delay of one *nor* per group. This results in five pair delays; when added to a two-pair-delay end effect, the seven-pair-delay results.

The Control Unit

The control unit generates a number of command pulses, effecting transfers in a sequence defined by the algorithm requirements. In general, a command pulse energizes a set of gates associated with a complete register and therefore has relatively large drive capability. These command pulses are formed by gating structures which use the operation code combined with input information from the timing and status generators.

The *timing* and *status generators* optimally sequence and integrate the memory timing and many instructions of different duration. There were two basic inputs to this design: 1) the choice of a 12-μsec memory cycle as a reasonable speed-power compromise for aerospace applications, and 2) the use of digital circuits which accomplish basic transfers in 1 μsec.

With these basic inputs, the method of handling "looping" in the multiply, divide, and square-root instructions was investigated. The problem consists of determining the number of discrete steps or transfers required to process one bit of the answer, and of creating a timing loop where an integral number of bits can be processed. Furthermore, the number of loops required for processing all answer bits should be integral so that no time is "left over" in the last loop. Careful algorithm design resulted in a three-step-per-bit *multiply*, a three-step-per-bit *divide*, and a six-step-per-bit *square root*. A six-step timing loop appeared to be most advantageous; thus, a six-stage timing ring counter was designed to produce six $\frac{1}{2}$-μsec pulses with $\frac{1}{2}$-μsec spacing on six independent lines.

The status generator identifies cycles of the ring counter. The number of timing cycles contained in the various instructions varies widely. Specifically, twelve instructions contain 2 cycles, eleven contain 4, one contains 6, one contains 17, two contain 18, one contains 32, and two are variable in length under program control. The status generator consists of flip-flops interconnected as a ring counter containing loops of various lengths. Interstage transitions are controlled by the operation levels and time pulses. An overlap exists between levels so that no unusable time gaps exist. The loops are chosen so that status levels (F_0–F_8) not only keep track of timing generator cycles, but also indicate logic actions which are common among various instructions. For example, at a particular time during F_8, independent of the instruction being executed, a count is made on the program counter.

Two status levels, F_0 and F_{00}, are used only when index register modification is called for by the index-register selection bits. During these levels, the selected index register is read from the data memory, and added to the address section of the instruction; this procedure adds 12 μsec to the instruction time.

The In-Out Unit

The computer *in-out unit* is simple in concept but flexible in the range of its possible application.

A block of 32 data-memory addresses is set aside for input-output, each address identifying a unique channel. Using the memory register as an in-out buffer, inputs and outputs are handled as though the selected addresses were part of the data memory. Outputs, for example, are sent out by programming a store instruction with an output address. By means of synchronizing and addressing logic, the contents of the accumulator are sent via the memory register to the external destination.

Inputs are handled by the *clear* and *add*, *add* or *subtract* instructions with the appropriate input address. The selected input is channeled by means of the input multiplexer gates to the accumulator for processing.

One of the input addresses is a *real-time clock* included as part of the input-output equipment to keep track of real time during branching operations, and for a special purpose related to the missile mission. This clock is a 15-stage counter that counts clock pulses at a 500-kc rate, giving a resolution of 2 μsec. The clock is addressed for a reading under program control, using the *clear* and *add*, *add*, or *subtract* instructions. Basic timing is derived from a temperature controlled crystal oscillator.

COMPUTER CIRCUITS

The AM computer circuits were required to meet the following requirements: 1) high reliability, 2) low power dissipation, 3) small volume, and 4) micromodule packaging.

The final AM circuits keep reactive components to a minimum and are basically resistance-coupled circuits composed of resistors and transistors only. One exception is the carry propagation circuit where a diode-coupled transistor logic *nor* gate is used for very high-speed operation.

The silicon transistor and diode circuits operate within the temperature range of 0°C to +100°C; where fan-in–fan-out reduction can be tolerated, however, it is possible to extend the temperature range from −55°C to +125°C.

A good beta range and a controlled tolerance of the saturation voltage, $V_{CE(sat)}$, is required. The $V_{CE(sat)}$ was established at 0.2 volts, maximum, at high temperature. Such low saturation voltages can be attained with planar expitaxial silicon transistors. The computer utilizes a basic pair of complementary transistors: 2N995 (PNP) and 2N2206 (NPN). Both have good beta range (35 to 140) and acceptable $V_{CE(sat)}$. Both transistors are adequate for the computer clock frequency of 1 Mc.

Five basic circuits comprise 83% of the computer, the remaining 17% being memory circuits and pulse generators. The five circuits are the *gate*, *flip-flop*, *inverter*, *double-emitter-follower*, and *nor*.

Among the advantages of this type of resistance-coupled transistor logic is that these circuits are normally off; minute power is dissipated in this state. The pulse duration is normally 0.5 μsec and the duty cycle a maximum of 8%. The transistors are on (saturated) only during this pulse period. When saturated, the transistors dissipate a minimum of power because of the low $V_{CE(sat)}$. Low stress results in higher reliability and better compatibility with the micromodule from the standpoint of heat.

Another advantage of this circuitry and logic is noise immunity. With the absence of such reactive elements as speed-up capacitors, the transistors are not overstressed during switching transients. In addition, the noise coupling into a transistor base is kept at a minimum.

MICROMODULE PACKAGING

The AM computer meets the stringent requirements of MIL-E-8189B which governs the design of equipment for aerospace systems. The volume is approximately 0.6 cu ft and the weight is approximately 30 pounds. Passive cooling techniques are utilized in the construction to handle the 100 watts average power dissipation.

The computer is entirely micromodularized except for the basic oscillator unit; the computer is comprised of 1,607 micromodules of 24 different types. Every transistor is procured in a TO-46 case to comply with micromodule standards. Each micromodule contains an average of four transistors. For example: one module type contains four gates, another contains a flip-flop and two gates, another has two double emitter followers. The determination of what goes into a module was based on organization, functional location, and signal flow as well as ease of manufacture and avoidance of noise problems. A crystal-controlled temperature-stabilized (oven) oscillator was procured as a sealed unit. This oscillator has a stability better than one part in 10^6 for 30 hours.

Individual micromodules, selected as functionally dependent, are assembled in clusters of four, six, or eight units. This allows subassembly manufacturing and permits functional testing on a lower level. The clusters are mounted with thermal inserts into the structure shown in the mock-up wiring of Fig. 4. This type of construction provides sufficient heat sinking for the micromodules. All micromodules are interconnected using welded construction. The interconnections of a cluster are pre-welded before insertion into the structure, and finally the clusters are welded together after insertion into the structure. Fig. 5 shows the outline of the AM Computer.

RELIABILITY

Reliability for an aerospace system is of prime importance. Every effort in the design of the AM computer was applied toward developing a highly reliable system. The design goal was a mean-time-between-failure (MTBF) in excess of 2,000 hours. The decision to use welded construction was based on this reliability requirement. A calculated stress analysis of all the AM computer circuits disclosed an MTBF in excess of 9,000 hours.

R. K. GORMAN graduated from Carnegie Institute of Technology (BSEE) in 1953 and Northeastern University (MSEE) in 1961. Mr. Gorman joined RCA in 1953 in the Specialized Training Program. Upon completion of this program, he joined the Electron Tube Division in Lancaster, Pa. where he was responsible for design and development of color TV circuits and cathode ray tube test equipment. After active duty with the U. S. Army, he rejoined RCA in 1957 at the Airborne Systems Laboratory at Waltham, Massachusetts. He was responsible for design and development of circuits for the Data Link Program, including transistorized logic for storage, control, and input/output functions. In 1962, with the Computer Products section of ACCD, Mr. Gorman was responsible for the logic circuit design of the AM series computers. He is a Member of the IEEE and IEEE-PTGEC.

ARTHUR OLSSON graduated from the University of Chicago in 1947 and subsequently did graduate work in the Philosophy Department, specializing in epistemology and mathematical logic. Prior to joining RCA in 1957 as a logic designer, Mr. Olsson was a partner in the operation of a precision optical shop, making aerial camera filters, prisms and lenses, and also worked for the Underwood Corporation as a computer logical designer. At RCA, Mr. Olsson has been active in the design of four digital computers. He was the logic task engineer on the computer described in the accompanying article. He also has designed parts of the Automatic Programmed Checkout Equipment (APCHE) for the Atlas Missile.

F. HASSETT received his BSEE from Tufts University in 1953 and is continuing his education at Northeastern University. Since joining RCA in 1953, Mr. Hassett has been engaged in digital computer design and development. This work included the logic design for the NIFTE computer, the design of magnetic logic circuits, and the design responsibility for transistor logic circuits for an airborne computer and a digital computer system. He participated in the design of an automatic programmed checkout equipment (APCHE), and has had the logic responsibility for two general purpose missile guidance computers. Mr. Hassett is presently involved in the logic design of a digital computer employing the residue number system; he is also active in the design of a Multisystem Test Equipment (MTE) system which will automatically test a variety of subsystems. Mr. Hassett is a member of Tau Beta Pi.

The David Sarnoff

C

The 1963 Individual Awards for Science and Engineering

Dr. Paul K. Weimer

Dr. Morrel P. Bachynski

. . . About the Awards

RCA's highest technical honors are the four annual David Sarnoff Outstanding Achievement Awards. The awards, formally announced by Dr. Elmer W. Engstrom, President of RCA, consist of a gold medal, a bronze replica citation, and a cash prize for each man.

The Awards for individual accomplishment in science and in engineering were established in 1956 to commemorate the fiftieth anniversary in radio, television, and electronics of Brigadier General David Sarnoff, RCA Board Chairman. These have been made annually since to one scientist and one engineer. The two awards for team performance were initiated in 1961.

All engineering activities of RCA divisions and subsidiary companies are eligible for the Engineering Awards. The Chief Engineers in each location may present nominations annually. Similarly, members of the research staff of the RCA Laboratories are eligible for the Science Awards. Nominations are made by the Research Directors. Final selections are made by a committee of RCA executives, of which the Vice President, Research and Engineering, serves as Chairman.

DR. PAUL K. WEIMER, Member of the Technical Staff, Electronics Research Laboratory, RCA Laboratories, Princeton, N.J., recipient of the 1963 David Sarnoff Outstanding Achievement Award in Science . . . *"for basic and practical contributions leading to the successful and widely diversified application of evaporated thin films."*

DR. WEIMER is well known for his basic contributions to the development of the image orthicon and vidicon camera tubes used in television, and for his recent pioneering work in thin-film electronic devices and circuits. He has been on the staff of RCA Laboratories since 1942. Dr. Weimer contributed importantly to RCA's development of color television picture tubes during the early 1950's. During 1959-60, he undertook studies at the University of Paris under RCA sponsorship, concentrating upon new aspects of solid-state physics. Upon his return to RCA Laboratories, he turned to the development of new thin-film electronics devices and circuits. In 1961, he was responsible for the achievement of the thin-film transistor, the first practical amplifying device to be made entirely by evaporation techniques.

DR. MORREL P. BACHYNSKI, Director of the Microwave and Plasma Physics Research Laboratory, RCA Victor Company, Ltd., Montreal, Canada, recipient of the 1963 David Sarnoff Outstanding Achievement Award in Engineering . . . *"for outstanding and widely recognized achievements in the fields of microwaves and plasma physics."*

DR. BACHYNSKI has been widely recognized for his contributions to the understanding of electromagnetic wave propagation and his theoretical and experimental studies of aberrations in microwave lens systems. Since 1955, as a member of the staff of the RCA Victor Company, Ltd., Research Laboratories in Montreal, and later in charge of its Microwave and Plasma Physics Research Laboratories, he has been primarily concerned with short-wave propagation and plasma physics. In the latter area, Dr. Bachynski has made important contributions to the theory of electromagnetic wave interactions with plasmas confined in a magnetic field. He has also developed significant new microwave techniques for analyzing plasma. More recently, Dr. Bachynski has been responsible for the organization and supervision of an outstanding research group in microwave and plasma physics, which has received international recognition.

The 1963

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DR. BENJAMIN ABELES, DR. GEO
DR. JOHN P. DISMUKES, D
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Outstanding Achievement Awards

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L. J. CAPRAROLA, JOHN J. CARRONA, NORMAN S. FREEDMAN, LEWIS H. GNAU, CAREL W. HORSTING, and **WALTER F. LAWRENCE, JR.,** members of the engineering staff at the RCA Electron Tube Division, Harrison, N.J., recipients of the 1963 David Sarnoff Outstanding Team Award in Engineering . . . "*for team performance in developing practical structures and production methods for thermoelectric power generators.*"

wis H. Gnau

Carel W. Horsting

Walter F. Lawrence, Jr.

Both team awards in science and engineering have been awarded for achievements in thermoelectrics. The recipients of the team award in science were cited for their part in the development of new high-temperature thermoelectric materials, while the team recipients in engineering were recognized for their contributions in the application of high-temperature thermoelectric materials to efficient power-generation for such systems as nuclear-powered earth satellites.

Approximately eighteen months ago RCA Laboratories undertook an intensive program, largely Navy-sponsored, to develop thermoelectric materials capable of converting heat to electrical energy efficiently over a broad range of temperatures from room temperature up to 1000°C.

In the first two stages of the project, the RCA Laboratories group, using telluride compounds, developed several power-generating materials which operated in the range from 25°C to 550°C with higher efficiencies than any previously reported. In the most recent phase of the program, as a result of very precise measurements of the thermal conductivity (heat flow) in various semiconductors, the RCA scientists developed new germanium-silicon alloys that operated satisfactorily in the upper temperature range from 500°C to 1000°C. With these new alloys, it should be possible to develop sandwich-type thermocouples which produce electricity directly from heat over a broad temperature range with efficiencies up to 15%.

DR. ABELES, DR. CODY, DR. DISMUKES, DR. EKSTROM, AND DR. ROSI, winners of the Team Award in Science, were members of the group which developed the new germanium-silicon alloys for high-temperature power generation. As part of this project, they also developed a new diffusivity method for measuring the thermal conductivity of these materials, as well as a method of preparing their alloys with suitable properties for thermoelectric generating applications, and a zone-leveling technique to provide ingots of the alloys.

MESSRS. CAPRAROLA, CARRONA, FREEDMAN, GNAU, HORSTING, AND LAWRENCE, winners of the Team Award in Engineering, successfully developed a practical method of utilizing these superior new thermoelectric materials for satellite applications. This group had first to evolve a method for attaching electrical and thermal contacts to the thermocouples, and then to set up pilot production facilities to produce the thermocouples in usable quantities. In addition, they translated the Laboratories zone-leveling technique into a well-controlled, highly efficient material fabrication process.

As a result of this work, the RCA Electron Tube Division has been asked to supply germanium-silicon thermocouples—the key components—for the SNAP 10A project (*S*ystems for *N*uclear *A*uxiliary *P*ower) being undertaken by Atomics International for the Atomic Energy Commission.

In characterizing the achievements of the two award-winning teams, Dr. Engstrom stated: "*The unprecedented success of these two research and engineering teams in moving from materials research to device development in a few short months has been instrumental in putting RCA into the field of direct energy conversion as a new area of business. We feel they have laid the foundation for a major new RCA product line.*"

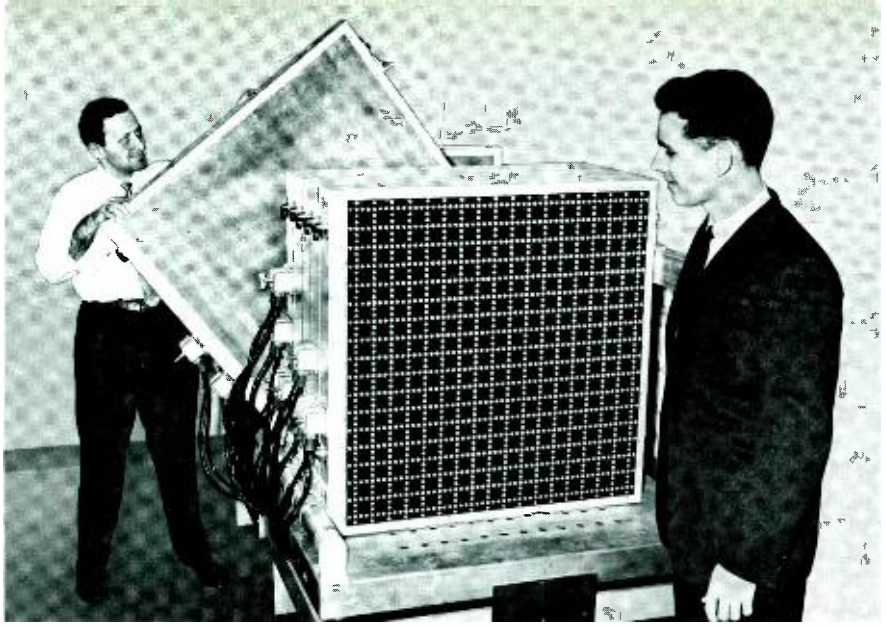

Fig. 2a — Retina model (view from direction A of Fig. 2b). M. Herscher, co-author, is pulling out one of the logic panels, while co-author T. P. Kelley observes.

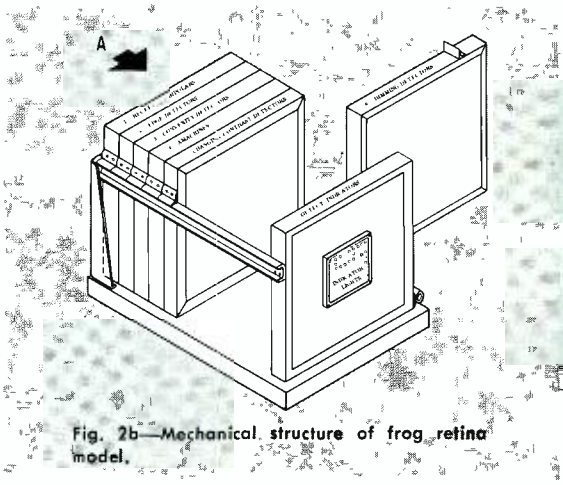

Fig. 2b—Mechanical structure of frog retina model.

FUNCTIONAL ELECTRONIC MODEL OF THE FROG RETINA

A functional electronic model of the frog retina has been constructed at DEP Applied Research which simulates many qualitative and quantitative properties of the visual system of the frog. Because of the unique construction techniques employed, intermediate logic outputs may be visually observed. The model abstracts visual features by using deterministic parallel processing and overlapping responsive-receptive fields — two features that are novel in the field of visual-pattern recognition. This equipment should provide a useful research tool for further studies in pattern recognition, feature abstraction, and parallel processing. The model, while itself capable of only limited performance, may well be a significant first step toward the design of complex equipment for surveillance, reconnaissance, and vehicular guidance.

M. B. HERSCHER and T. P. KELLEY
Applied Research
DEP, Camden, N.J.

THE FUNCTIONAL ELECTRONIC MODEL of the frog retina described herein is based on the physiological work of Lettvin and others[1,2,3], who measured the electrical signals that the frog retina was sending to the colliculus (the brain "mapping" center). These investigators distinguished four classes of optic-nerve fibers; each class carries different information regarding a specific feature of the image on the retina. Their studies revealed that the frog retina performs a sorting operation in which four classes of properties are abstracted: 1) edges, 2) moving convexities, 3) contrast changes and 4) dimming.

Fig. 1 shows schematically some of the qualitative properties of the feature-abstraction processes performed by the frog retina. The circle at the left (labeled *input*) contains four small figures representing images which might be presented to the retina; the arrow indicates the direction in which the images are assumed to be moving. Circles I through IV illustrate how these images are "mapped" into the colliculus. Circle I shows that the edge detectors abstract both stationary and moving edges. Circle II shows the features abstracted by the moving-convexity detectors; since only dark convexities moving toward the center of the field of view are detected, only the trailing edge of Image 1 and the entire outline of Image 2 are abstracted. In abstracting changes of contrast, the leading and trailing edges of all moving dark images are abstracted as shown in Circle III. Circle IV shows that the dimming detector abstracts only the leading edges of moving dark images.

In biological systems, the size of the *responsive-receptive field* (RRF) associated with the visual-image information-reduction process is an important consideration. The relative size of the RRF is proportional to the number of receptors projected onto one of the ganglion cells in any class. This projection is a result of a many-to-one transformation which occurs in the retina system. In the visual system of the frog, there is a specific size for the RRF which is associated with each of the four classes of feature-abstracting ganglion cells. The size of each receptive field increases as the ganglion class increases from 1 to 4.

The frog retina model which has been constructed possesses many of the specific feature-abstraction properties found in the frog. In addition, the model simulates other physiological properties such as the incorporation of overlapping receptive fields for each class of ganglion cell, and the preservation of the relative RRF size for each class of ganglion. The model also has a general physical correspondence to the anatomy of the frog retina; i.e., processing takes place in various neural layers. Since the ganglion cells of the frog are sensitive to both the speed and the size of the image presented to the retina, this sensitivity also is incorporated in the functional model.

GENERAL DESCRIPTION OF RETINA MODEL

This functional model employs seven processing layers which are mounted vertically as illustrated in Fig. 2. Fig. 2b shows where each logic function is located, while Fig 2a is a photograph of the actual retina model. The six layers perform parallel processing on the information presented to the retina. The seventh layer contains the output indicators and power distribution system for the model. Each of the six active processing planes may be removed from the main frame for testing or servicing. Fig. 2 shows layer 6 in this position. The interconnections for the first four processing layers are made by light transmission from neon lamps in the back of one layer to photoconductors in the front of

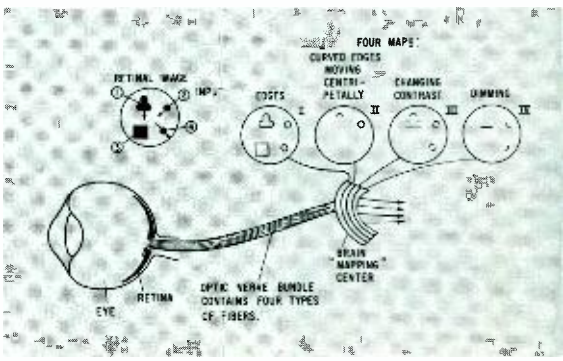

Fig. 1 — Schematic of frog visual system.

M. B. HERSCHER received his BSEE in 1953 and his MS in 1959 from Drexel Institute of Technology, and is presently enrolled in the PhD program at the University of Pennsylvania. His experience includes work at the Frankford Arsenal on electronic fuse circuitry. In 1953 he joined the Circuit Development Group in RCA. He spent 21 months as an officer in the U.S. Army Signal Corps, where he worked on transistor circuits as applied to frequency control, and returned to RCA in 1956. Since then, he has worked on development of high-power transistor audio amplifiers, transistor-magnetic pulse circuitry, nonlinear-amplitude coding devices, and semiconductor linear mixers. Recently, he was project engineer on a study of intelligence information processing and a transistor magnetic video recorder. Currently, he is a Project Engineer responsible for applied research on visual pattern recognition. He has taught several transistor circuit theory courses at RCA and the Fort Monmouth Signal Labs. He has published papers and is a coauthor of the 2nd edition of the "Handbook of Semiconductor Electronics."

T. P. KELLEY received his BS in Physics from St. Joseph's College, Philadelphia, Pa. in June 1961. He is currently studying for an MSEE at the University of Pennsylvania. Since joining RCA, Mr. Kelley has made contributions in many fields, including radar receivers, photovoltaic cells, and digital transmission. More recently, he has been conducting pattern-recognition studies. Specifically, he has studied the application of parallel logic schemes to pattern recognition problems, and the implementation of parallel logic through the use of light-emitting and light-sensing devices. This recent work has led directly to the design and construction of the functional electronic model of the frog retina. Mr. Kelley is a member of the Franklin Institute.

the following layer. In this manner, light provides the majority of the synaptic connections of the model. The neon lamps and photoconductors serve also as the principal circuit components for the threshold logic.

The output of the ganglion cells are available in two forms: 1) relay contact closures which provide binary electrical outputs, and 2) incandescent lamps which provide a two-dimensional display of the four features abstracted. The Class 1 and Class 2 indicator lamps provide binary visual outputs, while the Class 3 and Class 4 lamps provide analog outputs.

The following guidelines were used in the design and fabrication of the model.

1) A construction technique was selected which would permit individual logic functions to be fabricated on individual layers. This technique greatly simplifies the wiring and interconnection of components.
2) All components in each layer were made readily accessible, thereby permitting easy repair.
3) The logic for the various feature-abstraction functions was isolated to simplify the testing procedures.
4) Neon-lamp photoconductor interconnections were used between the first four processing layers to permit all circuits on each layer to be individually tested by observing the visual outputs.
5) The model was designed so that individual layers of logic may be modified, and/or replaced. In addition, logic changes can be made in some of the present layers by simple changes of wiring.
6) The model was designed to simulate the anatomy of the frog by using logic processing layers and by preserving the relative location of each ganglion class within these layers.

SYSTEM LOGIC

The system logic required to accomplish the feature-abstraction operations performed by the four classes of ganglia of the frog retina model is presented in this section. This logic is a modification of the logic originally described by E. E. Loebner[4].

Edge-Detection Neuron (Class 1)

The edge-detection neuron abstracts edges from the input image. In order to detect an edge, the existence and position of horizontal and vertical contrasts on the receptor matrix are detected by the bipolar neurons. Then, if a sufficient number of bipolar neurons of the same directionality are activated, an edge is presumed to exist in the receptive field of the Class 1 ganglion cell.

The basic contrast decisions are made by the bipolar neurons. These neurons are located in the first layer of the retina model and consist of two photoconductive receptors connected to two neon lamps in a balanced-bridge circuit. When contrast exists between the paired-input receptors, an appropriate neon lamp (bipolar output) is activated, thereby identifying the location and direction of contrast. Each bipolar neuron, then, provides two directional outputs per pair of input receptors. Since 1,296 input receptors are employed, there are 648 bipolar neurons which provide 1,296 outputs.

The activation of particular combinations of directional bipolar outputs results in the detection of an edge of minimum length. This detection is accomplished by summing four adjacent bipolar outputs which possess the same contrast directionality into a majority-of-four decision-maker as shown in Fig. 3. This majority logic is located in the edge-detection layer, where additional photoconductive cells receive the directional contrast information from the neon-lamp outputs of the receptor-bipolar layer. Thus, an edge will be de-

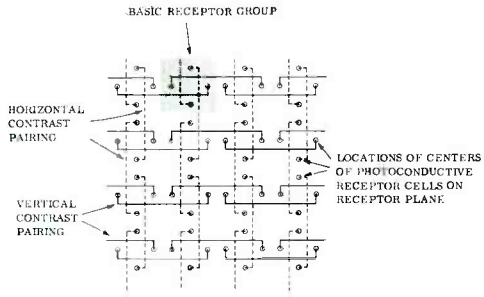

Fig. 3 — Portion of receptor matrix. This shows the bipolar pairing of receptors (Class 4 receptors are omitted in this figure).

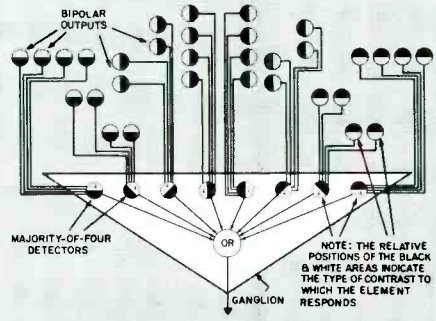

Fig. 4 — Edge-detecting ganglion cell (Class 1).

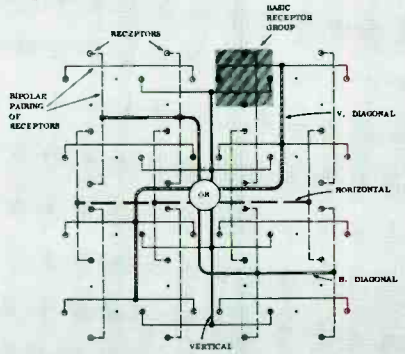

Fig. 5 — Complete layout of a typical Class 1 ganglian cell.

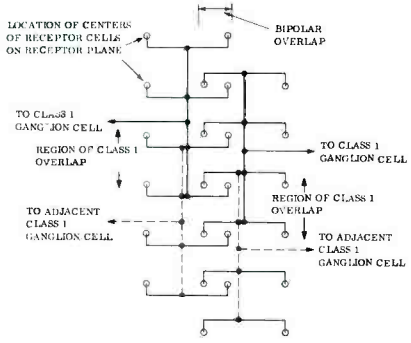

Fig. 6 — Portion of receptor matrix. This shows the bipolar pairing of receptors and summations of bipolars into majority-of-four detectors for *vertical* edge detection (other summations omitted for clarity).

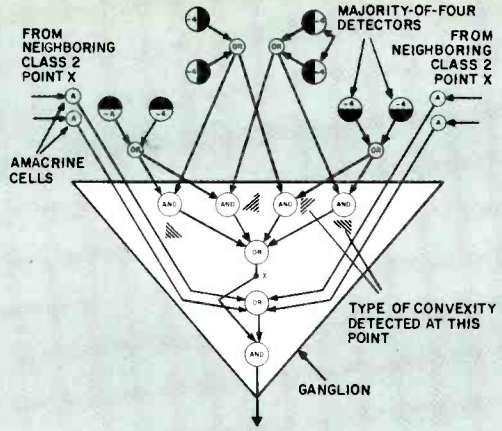

Fig. 7 — Tracked convexity ganglion cell (Class 2).

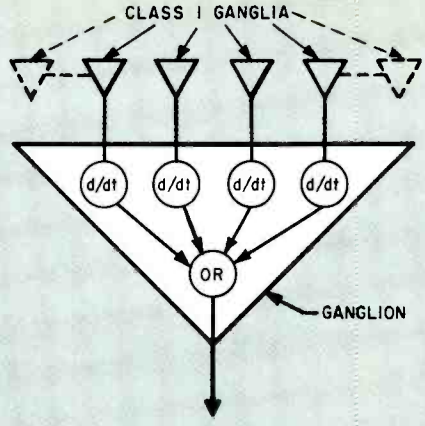

Fig. 9 — Changing contrast ganglion cell (Class 3).

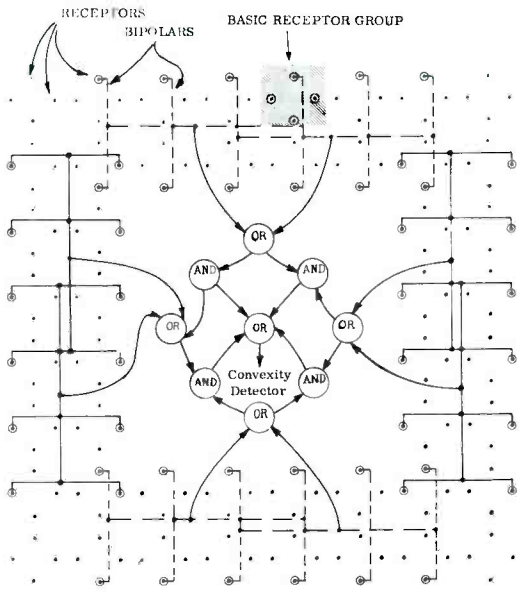

Fig. 8 — Portion of receptor plane showing logic connections for Class 2 ganglion cell.

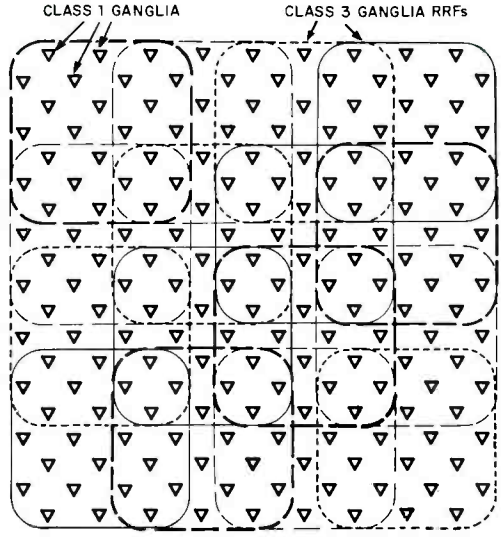

Fig. 10 — Class 3 ganglion cell overlap. This shows the overlap of Class 3 ganglia (squares), as well as the particular Class 1 ganglia (triangles) combined to form a Class 3 ganglion cell.

tected when an edge focused on the receptor plane is long enough to cause an output from at least three of four adjacent bipolars.

As stated above, the bipolar neurons determine the existence of horizontal and vertical contrasts only. It might seem that this restriction limits the detection of edges to only horizontal and vertical types. (Actually there is a range about the major axes of approximately $\pm 35°$ in which the presence of edges may be detected.) It is not necessary, however, to confine the bipolar neuron summation to adjacent horizontal or vertical bipolars. By summing several nonadjacent bipolar neurons of similar directionality, it is possible also to abstract diagonal edges. This additional summation permits the detection of all the possible orientations of edges appearing on the receptor matrix. Fig. 4 shows diagrammatically how eight connections of the four types of bipolar neuron outputs (two horizontal and two vertical types) are summed in an *or* gate to provide an output for the Class 1 ganglion cell. Thus a Class 1 ganglion output indicates the presence of an edge in a given location, irrespective of its orientation. The directional summations which make up the inputs for a Class 1 ganglion cell are shown in Fig. 5. This spatial arrangement leads to a Class 1 RRF consisting of 4 x 4 receptor-pairs.

An important feature of the model is the incorporation of overlap at various processing levels. For the Class 1 ganglia, overlap is present in the pairing of receptors and in the summation of bipolar neurons for the majority-of-four detectors. Each majority detector overlaps its neighbor by two bipolars. This feature, together with the requirement that only three of four inputs are necessary to activate the majority detector ensures that there are no insensitive spaces between neighboring majority detectors. In addition, this overlap also provides a form of spatial redundancy which reduces the possibility that a single malfunction will cause an error in the output. The ganglion cell overlap, as well as the receptor-pair overlap, is shown in Fig. 6. The overlap of ganglia results in a total of 180 Class 1 outputs for the retina model.

Moving-Convexity Neuron (Class 2)

The moving-convexity neuron abstracts dark convexities moving in a given direction. Inputs to the Class 2 ganglia are derived from the majority-of-four detectors of the Class 1 ganglion, as shown in Fig. 7. These inputs are obtained by sensing the neon-lamp outputs in the sec-

ond layer with photoconductive cells located in the third layer. Two overlapping majority-of-four detectors (which have the same directional contrast) feed an *or* gate.

A similar operation is performed on the output of six other bipolar neurons which are sensitive to contrast in a direction perpendicular to the first group of bipolar neurons. The second group of neurons also must have the proper spatial location with reference to the first group in order to be combined in an *and* gate, and thereby indicate the presence of a dark convexity. The output signals of the four possible combinations of convexities then are combined in an *or* gate to denote the detection of any convexity within the field of view of a particular Class 2 ganglion.

Fig. 8 shows the logic connections for a Class 2 ganglion cell, together with the relative spatial locations of the receptors. The RRF of a Class 2 ganglion cell for a frog is approximately 50 percent larger than that of the Class 1 ganglion cell. Therefore, on a relative basis, the RRF for the Class 2 ganglia of the model has six receptor-pairs on a side, as shown in Fig. 8.

In order to obtain an output from a Class 2 ganglion cell, it is necessary that a dark, convex object move across the input-receptor matrix in a given direction. The neural mechanism which provides tracking of lateral motion in the model is the *amacrine cell.*

Fig. 7 shows the location of the amacrine cells in the Class 2 ganglia logic. It is the function of the amacrine cells to provide a short-term memory of the presence of a convexity within the RRF of a convexity detector. The output (neon lamps) from the convexity detectors located in the third layer activate the inputs (photoconductive cells) to the amacrine circuits which are located in the fourth layer. The output of an activated amacrine is fed to specific adjacent Class 2 ganglion cells, enabling the *and* gate of these neurons to pass an output when a convexity is present in their receptive fields. Thus, a convexity will be tracked if it moves from one receptive field to another within a certain velocity range. For the Class 2 ganglia, a large amount of overlap is provided between the receptive fields of adjacent neurons. The model provides 90 output signals for the Class 2 ganglion cells.

Changing-Contrast Neuron (Class 3)

The changing-contrast neuron abstracts changes of contrast of relatively large dark objects appearing in its receptive field. As shown in Fig. 9, the Class 3 neuron of the model obtains its inputs from the Class 1 ganglia outputs derived previously. Many of these Class 1 outputs are summed in overlapping areas, then differentiated and fed through an *or* gate. Through the summation process, a large RRF for each Class 3 ganglion cell is obtained. Fig. 10 shows the arrangement of Class 1 outputs, represented by triangles. The 16 Class 3 ganglion cells are represented by large squares. This particular type of summation was chosen in order to obtain the proper receptive-field size for the Class 3 ganglia.

Since it is desirable to obtain analog information from the Class 3 ganglion cell, the *or* function is obtained by the linear addition of the transient voltages. The analog output therefore is a measure of the size and speed of the input image. Sixteen output signals from Class 3 ganglia are provided in the model.

Dimming Neuron (Class 4)

The dimming neuron abstracts changes in dimming appearing in its receptive field. The information for this neuron is most readily obtained by using separate receptors located on the input (receptor-bipolar) layer. These receptors take the central position in the basic block of receptors as shown in Fig. 11. Since the RRF of the dimming neuron is very large, many Class 4 receptors are summed before additional logic operations are performed. This summation is shown schematically in Fig. 12. Dimming is obtained by differentiating the summed receptor potentials (in order to detect motion of the input image) and then generating an *off* response to denote that dimming occurs. The *off* response is an analog output which simulates the envelope of the integrated physiological *off* response. The large overlapping receptive fields shown in Fig. 13 yield five independent output indications for the Class 4 ganglia.

SUMMARY

The functional model of the frog retina which has been constructed incorporates the four basic feature-abstraction functions found in the visual system of the frog.

The 4,580 logic operations contained in the model require the use of over 32,000 individual circuit components, including 3,793 photoconductive cells and 2,652 neon lamps. More than 2,000 neon-lamp-photoconductor pairs provide "light connections" between processing layers.

Because of the unique construction techniques employed, intermediate logic outputs may be visually observed. The model abstracts visual features by using deterministic parallel processing and overlapping responsive-receptive fields. The inclusion of these two features are novel in the field of visual-pattern recognition. This equipment therefore should provide a useful research tool for further studies in pattern recognition, feature abstraction, and parallel processing. The model, while itself capable of only limited performance, may well be a significant first step toward the design of complex equipment for surveillance, reconnaissance, and vehicular guidance.

ACKNOWLEDGEMENT

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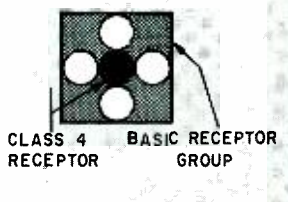

Fig. 11—Location of Class 4 receptors in basic receptor group.

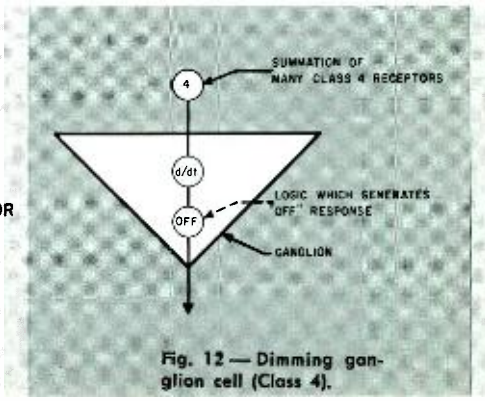

Fig. 12 — Dimming ganglion cell (Class 4).

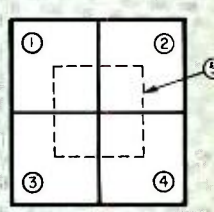

Fig. 13—Overlapping RRF's for the 5 Class 4 ganglia.

A SPECIAL PURPOSE DIGITAL COMPUTER FOR SEQUENTIAL DECODING

Theory of sequential decoding has been developed and explored at the Massachusetts Institute of Technology to the extent of experimental verification of principles on a general-purpose digital computer. This paper describes a recently designed, highly specialized computer which incorporates modifications of the original sequential-decoding concepts to minimize the machine complexity and the number of computations required to perform the decoding process. The resulting computer is sufficiently small that it becomes practical to consider it for either fixed or mobile military communications equipment where error rates in the order of one part in 10^8 or lower are necessary.

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THE COMMON METHOD for obtaining very low probability of error when communicating through noisy channels is to employ error-correction coding techniques.

ERROR-CORRECTION CODING

Let us first assume a mathematical model for a practical channel in order to illustrate clearly the general aspects of these techniques. A very convenient model is the *binary symmetric channel* (BSC) which has a binary alphabet and is characterized by the following transition probabilities:

$$\text{Prob}\{0 \text{ is received if } 0 \text{ was sent}\} = \text{Prob}\{1 \text{ is received if } 1 \text{ was sent}\} = q_0$$
$$\text{Prob}\{0 \text{ is received if } 1 \text{ was sent}\} = \text{Prob}\{1 \text{ is received if } 0 \text{ was sent}\} = p_0$$

Where: $p_0 = 1 - q_0$

Now, one might wonder why it should be necessary to go to the complexity of error-correction coding when simple redundancy can increase reliability. To answer, let us look at a simple redundancy technique. Suppose it is desired to transmit some binary sequence, x, of the symbols *0* and *1*, (call them information digits) and then reproduce this exact sequence in the output of the receiver after the sequence has passed through the channel. But instead of sending each information digit once, each is sent n times. If n is wisely chosen to be odd, then a majority decision can be used to select the most likely transmitted bit. It is clear that the reliability of communication is thereby improved over the transmission of unprotected digits. In fact, as n is increased to infinity, the probability of error approaches zero.

But unfortunately, at the same time, the rate of transmission R_t which equals 1/n in this case also approaches zero. This indicates a rather large price is being paid for reliability with this technique; namely, a linearly diminishing information rate. Shannon's theorem[1], however, indicates that it is not necessary to sacrifice information rate in order to get high reliability. Rather, as long as the rate is kept lower than some C, (which Shannon calls the channel capacity) and sufficiently complex coding is used, the probability of error can be made as small as desired.

Message Sequence	*Code Sequence or Code Word*
0.....00	0110.....0
0.....01	1001.....0
0.....10	1100.....1
.....	.....
.....	.....
11.....11	1101.....1

Fig. 1—An example of a code book for block-coding communication.

Shannon did not, however, present any coding algorithm that would provide the panacea for reliable communications, but techniques that satisfy his theorem have gradually been advanced since the time of his revolutionary paper. Most of these techniques fall into one or two principal classes, *block coding* or *sequential coding*. These will be discussed briefly in the following sections before proceeding to a description of the special purpose sequential decoding machine.

BLOCK CODING

In block coding for reliable communications, both transmitter and receiver possess identical code books (example, Fig. 1).

Suppose, for definiteness, that message sequences are taken in blocks of k digits, while code words consist of sequences of n digits ($n>k$) each. On the left-hand column of the code book appear the 2^k possible k-digit message sequences, while in the right-hand column of the code book the corresponding word appears.

000	000	000	000
			111
		111	010
			101
	111	010	011
			100
		101	001
			110
111	010	011	001
			110
		100	011
			100
	101	001	010
			101
		110	000
			111

Fig. 3—Code tree structure resulting from the encoding process of Fig. 2.

The code book is applied in communication as follows: The message is partitioned into successive, nonoverlapping k-tuples. Each k-tuple is located in the code book, and the corresponding code word in the right-hand column is transmitted one digit at a time. At the receiver the received sequence is partitioned into successive nonoverlapping n-tuples. Each n-tuple is then decoded as follows: It is compared to each of the 2^k code words to obtain the Hamming distance[2] between the received word and the code word. The receiver then decides in favor of that code word which is nearest to the received word according to the Hamming distance.

This decoding process is a maximal-likelihood decision scheme whenever code words are all equally likely to be sent. Note that the number (n) of digits per code word is often called the *code length*. A code of the type shown in Fig. 1 is called a *block code*. The number (2^k) of code words in the code book is called the *size* of the code. The *information rate* characteristic (bits/digit) of a block code is defined as

$$R_t = \frac{\log_2 (\textit{code size})}{\textit{code length}} = \frac{k}{n}$$

This last definition assumes that each of the code words is equally likely to be selected for transmission.

The Shannon–Elias theorem[1,3,8] states, essentially, that it is possible to obtain an arbitrarily low probability of error simply by using sufficiently long codes (large n). However, as n increases, the code size (2^{Rn}) increases exponentially with n for a fixed information rate. Hence, the maximal likelihood decoding scheme also increases exponentially in magnitude, since it implies a comparison

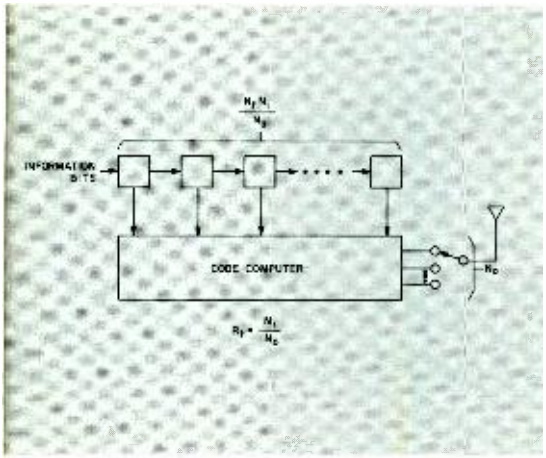


Fig. 2—A general form of a sequential encoder.

of the received word with *each* of the (2^{Rtn}) code words. A great deal of research has gone into the problem of finding special codes or special decoding schemes which may not be as effective as the maximal likelihood concept, but nevertheless yield low probability of error without excessive computation. Two such coding schemes, those of Reed–Muller[4,6] and Bosé–Ray-Chaulduri[5] appear to be most promising in this regard.

SEQUENTIAL CODING AND DECODING

The sequential technique offers a highly promising solution to the problem of decreasing probability of error exponentially with increasing n, without increasing equipment complexity exponentially.

The theoretical analysis of Wozencraft[7] indicated that the growth of complexity for a sequential decoder should vary approximately as $n_f \log n_f$. (In sequential decoding, n_f corresponds to n, or block length, in block decoding.) A fairly general form of a sequential encoding device is shown in Fig. 2. This encoder yields a code whose information rate R_t is given by

$$R_t = \frac{n_i}{n_0}$$

Where: n_i and n_0 are positive integers, and n_i is less than n_0. The encoding process is as follows: Suppose that x_1, x_2, etc., is the information sequence to be encoded. To begin with, the shift register in Fig. 2 contains $n_f n_i/n_0$ zeros. (It is assumed that n_0 divides n_f). Then the first n_i information symbols are shifted into the register. The code computer then computes n_0 distinct code digits which are fed to the transmitter, one digit at a time. Then the next n_i symbols are fed into the register, and another n_0 code digits are computed and fed into the transmitter.

This process continues. After n_f/n_0 such shifts, $x_1, \ldots, x_{ni}$ are dumped. Hence, each information digit affects precisely n_f code digits. It is for this reason that n_f is called the *code constraint length*. For simplicity of discussion, consider the case $n_i = 1$. Then $R_t = 1/n_0$, and n_0 divides n_f, the code constraint length. Then the above encoding process yields a code tree which might take the form shown in Fig. 3. When encoding sequentially, the binary decision to determine the branch progression from node to node is determined by whether the next information bit is a *1* or a *0*. The convention chosen is that if the next information bit is a *0*, the upper branch is chosen; the lower branch is chosen if it is a *1*.

At the receiver, there exists an identical encoding device which is in synchronism with the transmitter's code generator. This device generates a path of the code tree one branch (n_0 bits) at a time. At each node, one of the two possible branches (again assuming n_i=1), is chosen as being the closest (in the Hamming sense) to the received n_0-tuple. At each node, the decision to proceed through the tree is made only if one of the choices can be made without exceeding a distance threshold criterion. If one can proceed through the tree to the n_f/n_0 branch without exceeding the criterion, the information bit in the very first branch of the tree is decoded. Now, in stepping to the next branch the constraint no longer covers the branch which was decoded but affects the n_f/n_0 branches immediately following the first branch. As the decoding process continues, each acceptable branch results in a decoded information bit.

However, if at any node one may not proceed without exceeding the threshold criterion, a backtracking operation becomes necessary. Backtracking in the tree occurs one branch at a time until a path is found which permits proceeding again without exceeding the threshold criterion. If the search leads back to the first branch in the current tree after exhausting all possibilities, the threshold is loosened slightly, and a new attempt is made to proceed.

The threshold criterion mentioned refers to a series of probability criteria, from a most stringent one to the loosest possible, which are computed on the basis of an expected transition probability of error and the desired average probability of error per information digit. The approach is to attempt to decode using the most stringent criterion possible. For any one criterion, the maximum allowable number of disagreements depends on the point in the tree at which the comparison is made. The further the progression into the tree, the more disagreements are allowed for the same probability of error.

THE SEQUENTIAL DECODING COMPUTER

The functions of the *sequential decoding computer* are described by first discussing the encoding technique and then the resulting code structure which is processed by the computer.

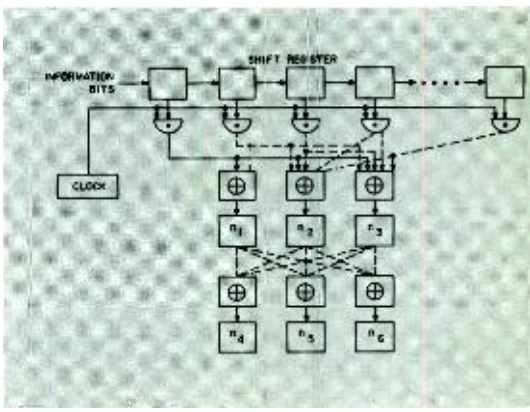
Encoding Technique

The code generator is illustrated in Fig. 4. It was thought desirable to provide considerable flexibility in the first experimental model; therefore, the code generator was designed to produce constraints and information rates which would be variable within limits. Fixing the ratio n_f/n_0 at 24, and varying the information rate R_t from ½ to ⅙ results in constraint lengths n_f ranging from 48 (for $R_t = ½$) to 144 (for $R_t = ⅙$).

Referring again to Fig. 4, information bits are fed serially into the 24-stage shift register. After each new information bit has been shifted in, taps from individual shift register stages are fed into three modulo-2 adders. The output from each adder is then a linear combination of the selected information bits which are present in the shift register. For reference, call the adder outputs n_1, n_2, and n_3. Selected taps from n_1, n_2, and n_3 are fed into a second set of three modulo-2 adders to form three additional outputs which are each a function of n_1, n_2, and n_3. For $R_t = ½$, only n_1 and n_2 are transmitted for each new information bit; for $R_t = ⅓$, adder outputs n_1, n_2, and n_3 are transmitted; and so on, until for $R_t = ⅙$, outputs n_1, n_2, n_3, n_4, n_5, and n_6 are transmitted. Since n_4, n_5, and n_6 are functions of n_1, n_2, and n_3, a maximum of only eight combinations are possible even though n_0 may equal 6.

The output from the first stage of the shift register, which holds the last received information bit, is connected to the first three modulo-2 adders to insure that the two possible configurations of three code digits represented by n_1, n_2, and n_3 are complementary. It appears that the additional tap connections to n_2 and n_3 can be made in a random fashion

Fig. 4—Sketch of the code generator.



to produce an acceptable set according to the coding theorem. An odd number of inputs (1 or 3) to each of the n_4, n_5, and n_6 modulo-2 adders insures that these additional code digits will be complementary in the same fashion.

The special class of codes obtained from this type of code generator satisfy Shannon's coding theorem and are well suited for sequential decoding. The complementary branches simplify the logic, speed up the computation time, and optimize the decision process by offering as choices at the nodes two sequences which are a maximum distance apart (in the Hamming sense).

Decoding Technique

Fig. 5 illustrates the fundamental decoder system. The received code is first quantized and then partitioned into non-overlapping n_0-tuples (branch lengths) in the input correlator. The distance between each received branch and the eight possible received branches is measured and stored in a random-access magnetic-core memory.

Upon reception of a message, the code generator starts generating a path sequence, one branch at a time. The branch comparator then decides at each node, which of the two complementary branches generated is the closest to the received n_0-tuple. The total distance between the tentatively accepted path sequence and the received branches is stored in the *total distance accumulator*. The associated threshold circuits decide at each node whether or not this total distance exceeds the allowable distance for the current path length. The threshold table, which is stored in the memory, provides the allowable distances for all possible path lengths. If the distance exceeds the threshold, backtracking is necessary, and the search is restarted at the previous node through the complementary branch which represents the second choice at that node. If the threshold was not exceeded, the branch counter decides whether or not the searching procedure has reached the end of the current constraint. If the end has been reached, an information bit is stored and is available for printing. The search procedure then continues with the constraint shifted one branch length. If the end of the constraint has not been reached, the search continues in the forward direction.

TABLE 1 — Rules of this Computer

1) The computer contains a code generator similar to the one at the transmission source. The only difference is that at the receiver only three code digits need be generated, regardless of the transmitted n_0, since only eight combinations are being received. The additional redundancy above three bits is helpful only in getting a particular waveform through the channel with more reliability. The sequential decoding reliability is still essentially the same as for $n_0 = 3$.

The code generator in the receiver generates a path sequence, three bits at a time, in the code tree. At each node of the tree, the memory is called upon for the distance between the next receiver-generated branch (3 bits) and the received n_0-tuple corresponding to the same node. Since the normalized distance per branch may range from 0 to 7, the complementary branch is selected as the correct one if the distance is greater than 3. The distance between the received branch and the chosen receiver branch is then added to a counter, recording the total distance to the latest node. As long as this total distance does not exceed the current criterion's allowable number of differences, the sequence proceeds in like manner from node to node.

When the operation has proceeded through 24 comparisons, a message bit is decoded, (*0* or *1*), depending on whether the first branch in the current tree is an upper (*0*) or a lower (*1*) branch.

2) If the distance threshold is exceeded at any node, the computer begins backtracking, one node at a time. The process of backtracking in the most efficient manner is as follows: From any node, the machine sequences back through the last selected branch to the previous node. An attempt is then made to proceed forward through the branch which had been previously discarded by comparing the total path distance through this branch to the threshold criterion. The searching procedure continues until some path is followed in the forward direction through 24 branches to the last branch of the current tree; or, the backtracking process reaches the first branch of the current tree, at which time the threshold is loosened, and the search is restarted at the node of deepest penetration within the current tree which had been recorded at the former criterion.

3) When the last branch of the current tree is passed, (at $k = 25$, where k is the branch number recorded in the branch counter) the information bit associated with the first branch in the current tree is removed from consideration and its contribution to the accumulated distance subtracted from the distance counter. The constraint now encompasses a new last branch. If the current criterion is the first, or most stringent criterion, the move is made to immediately compare the new branch to the corresponding received branch and depending on whether the threshold is exceeded or not, backtrack as before or decode another information bit.

If the current criterion is other than the first, the criterion is lowered by one and the attempt is made to proceed. If the threshold is exceeded, the criterion is raised back to its former value and from there the computer proceeds in the normal fashion to backtrack or go forward. This procedure forces the computer to decode at the lowest possible criterion, thereby decreasing probability of error. Also, since an n_0-tuple is discarded at this time, there is the likelihood that it contained some or all of the errors which forced the criterion up.

The flow diagram describing the decoding algorithm is illustrated in Fig. 6. The rules followed by the computer are specifically defined in Table I.

Results of Theoretical Studies— Independent Errors

In an effort to determine, with a fair degree of accuracy, the average decoding speed of the specialized digital computer for sequential decoding, several experiments were performed by hand computation.

Each experiment consisted of feeding the computer 3072 *code* bits, which represented 1024 *information* bits, and decoding the first 1000 of these information bits by following the rules and procedures of the computer. The code bits were assumed to be the all *0* sequence, which contained errors at a selected rate, distributed at random. A table of random digits[9] was used to select the occurrence of errors.

Each experiment consisted of assigning a specified average error rate to the code bits fed to the computer, and then counting the number of computations required to decode the 1000 information bits. One computation is defined to represent the comparison of the received n_0-tuple to the current branch in the tree, and all of the necessary recording and threshold examining required before proceeding to the next branch in the tree. Since the average time for a backtrack computation is almost identical to the time for a forward computation, the two will be considered as "computations."

Fig. 7 graphically shows the number of bits decoded at each criterion. Fig. 8 illustrates the frequency of the number of computations per backtrack.

In the first experiment, an average error rate of 0.01 was selected for the incoming code bits. It took only 1023 computations to decode the 1000 information bits, since there never occurred a necessity for backtracking. The additional 23 computations were required to get through the first tree (24 branches) before an information bit could be decoded, as will always be the case. The most errors that occurred during any one constraint was three. There were a total of 23 errors in this sample, while the mean number of errors was 30.7 for this size sample and error rate.

Since one computation requires 87.75 μsec, the average decoding rate was:

$$\frac{1 \text{ comput.}}{87.75\ \mu\text{sec}} \times \frac{1000 \text{ inf. bits}}{1023 \text{ comput.}} = 11{,}000 \text{ inf. bits/sec}$$

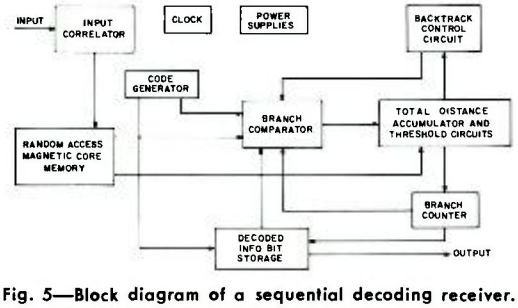


Fig. 5—Block diagram of a sequential decoding receiver.

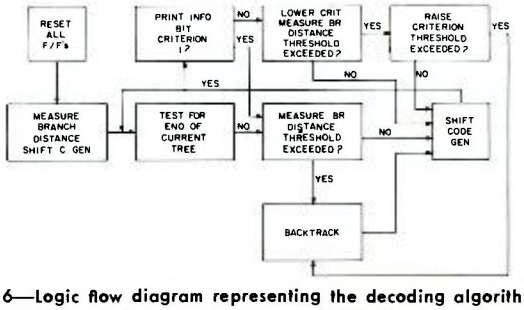


Fig. 6—Logic flow diagram representing the decoding algorithm.

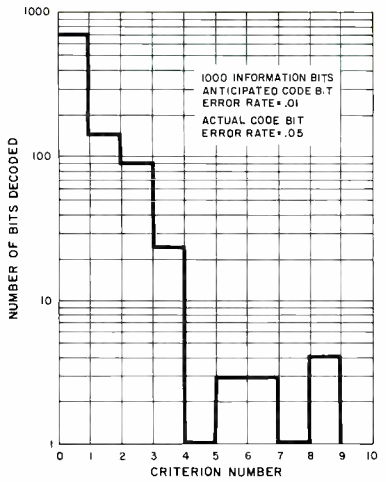


Fig. 7—Graph showing the number of bits decoded at each criterion.

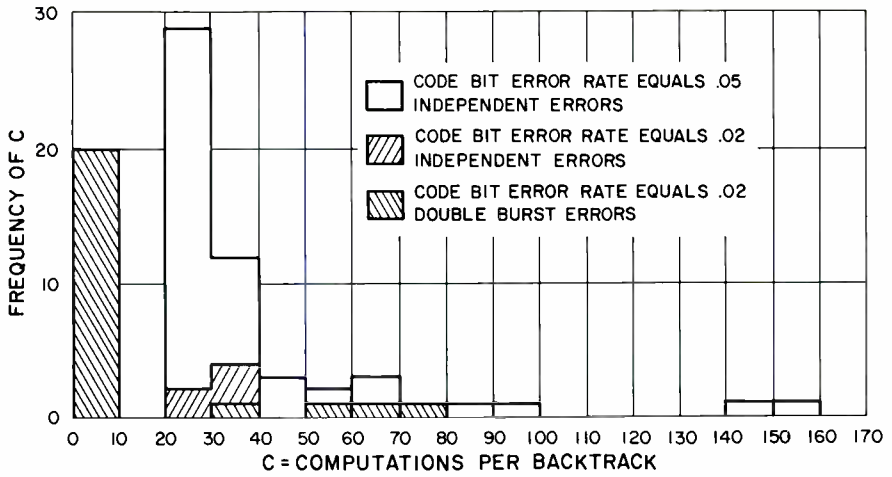


Fig. 8—A graph representing the number of backtracks which involved K.10 to (K.10 + 9) computations.

The number of computations per information bit was 1.023.

In the second experiment, an average error rate of 0.02 was assigned to the incoming code bits. The sample used contained 63 errors as compared to the mean of 61.4 errors for this size sample and error rate. The maximum number of errors within a constraint at any time was seven, necessitating the use of criterion 4. Backtracking was required 6 times, causing an additional 177 computations. The number of computations per information bit was 1.2. The average decoding rate was then:

$$\frac{1 \text{ Comput.}}{87.75\ \mu\text{sec.}} \times \frac{1000 \text{ inf. bits}}{1200 \text{ comput.}} = 9500 \text{ inf. bits/sec}$$

In the third experiment, an average error rate of 0.05 was assigned to the incoming code bits. There was a total of 147 errors in the sample as compared to a mean of 153.6 errors for this size sample and error rate. At one time there were ten errors within a constraint, necessitating the use of criterion 9. Backtracking was necessary 54 times, requiring an additional 2115 computations. The number of computations per information bit was 3.138. The average rate of the decoder was then:

$$\frac{1 \text{ comput.}}{87.75\ \mu\text{sec}} \times \frac{1000 \text{ inf. bits}}{3138 \text{ comput.}} = 3630 \text{ inf. bits/sec}$$

Results of Theoretical Studies—Burst Errors

In the following two experiments it was assumed that errors occurred in double bursts. The average error rate was selected as previously, but whenever an error was introduced there was also an error assumed on the very next bit.

In the fourth experiment, an average error rate of 0.01 was assigned to the incoming code bits. In this sample there were 44 errors as compared to the mean of 30.7. There were 12 double errors (2 errors on one branch) and 20 single errors. The maximum number of errors at any time within the constraint was four, therefore criterion 1 was used throughout the experiment. However, it was necessary to backtrack 12 times (each double error selects a wrong path initially), adding 84 computations to the decoding operation. The number of computations per information bit was 1.11. The average decoding rate was then:

$$\frac{1 \text{ comput.}}{87.75\ \mu\text{sec.}} \times \frac{1000 \text{ inf. bits}}{1107 \text{ comput.}} = 10{,}290 \text{ inf. bits/sec}$$

In the fifth experiment, an average rate of 0.02 was assigned to the incoming code bits. There were 58 errors; 20 double errors and 18 single errors, as compared to the mean for this size sample and error rate of 61.5 errors. It was necessary to backtrack 24 times, causing 302 additional computations. The maximum number of errors within one constraint was six, requiring criterion 3. The number of computations per information bit was 1.325. The average decoding rate was then:

$$\frac{1 \text{ comput.}}{87.75\ \mu\text{sec}} \times \frac{1000 \text{ inf. bits}}{1325 \text{ comput.}} = 8590 \text{ inf. bits/sec}$$

CONCLUSIONS

The entire experimental computer, including all logic, a random access core memory, and power supplies will fit into a standard 4-foot rack. The computer will use semiconductor circuitry (500 transistors), will operate at a basic clock rate of 285 kc, and will have the flexibility to receive at any keying rate up to 23 kilopulses/sec. The machine will decode information at rates up to 11.5 kilobits/sec. and should handle code bit-error rates up to one error in ten transmitted bits (10 percent).

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GEORGE C. HENNESSY graduated from Georgia Tech. in 1958 where he received his BSEE Cum Laude; he joined the Advanced Systems and Techniques Section of RCA's Aerospace Communications and Controls Division the same year. As a member of RCA's Graduate Study Program, Mr. Hennessy received his MSEE degree from the University of Pennsylvania in 1961. Mr. Hennessy has devoted most of his time to the field of digital communications involving various coding studies. He worked on a feasibility model of a secure anti-jam communications system, was a participating member of an inter-industry space weapon system study team, assisted in the study of an Aerospace Surveillance and Warning System, contributed to the system design of an integrated tracking and communications system, and has been directly involved in the development of ranging techniques for various programs. He is currently project engineer on a program developing an anti-jam real-time video link. He is a member of Tau Beta Pi, Phi Kappa Phi, Eta Kappa Nu, Phi Eta Sigma and the IRE. Mr Hennessy is also an instructor in the Physics Department of the LaSalle College Evening Division.

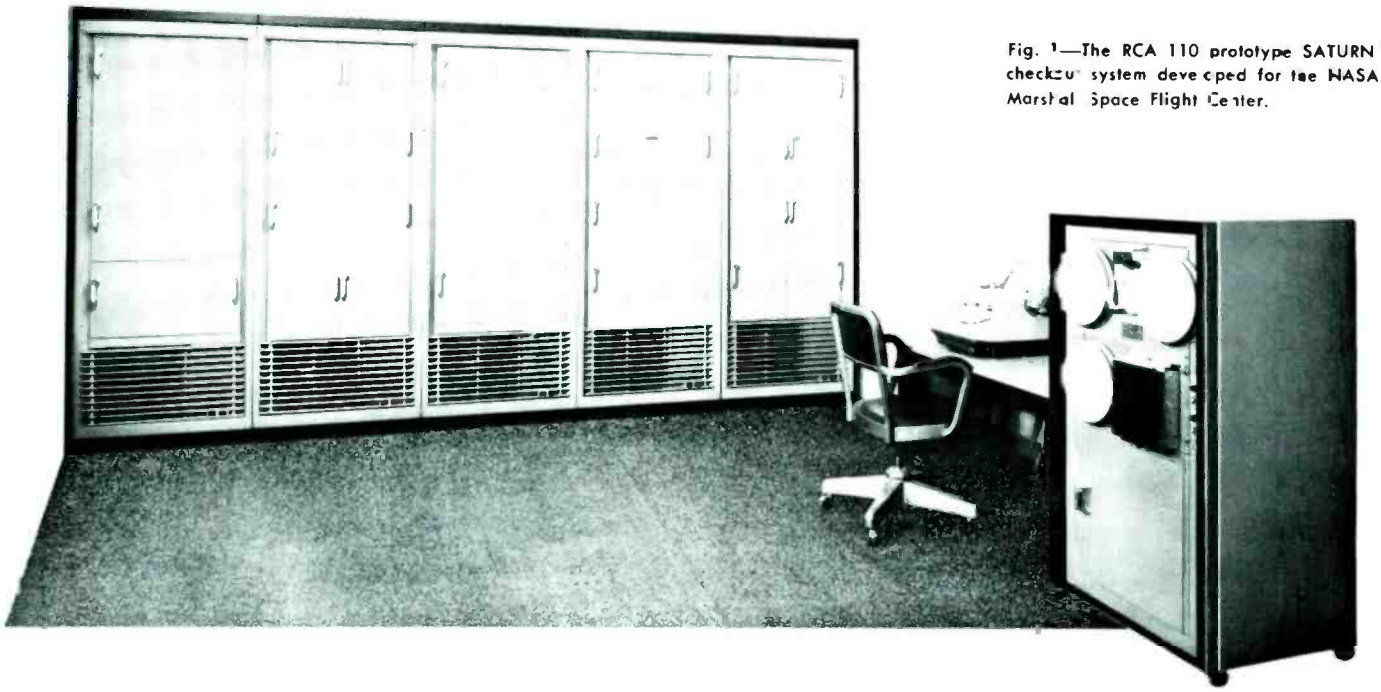

Fig. 1—The RCA 110 prototype SATURN checkout system developed for the NASA Marshal Space Flight Center.

HIGH-SPEED COMPUTER-CONTROLLED CHECKOUT SYSTEM FOR SATURN

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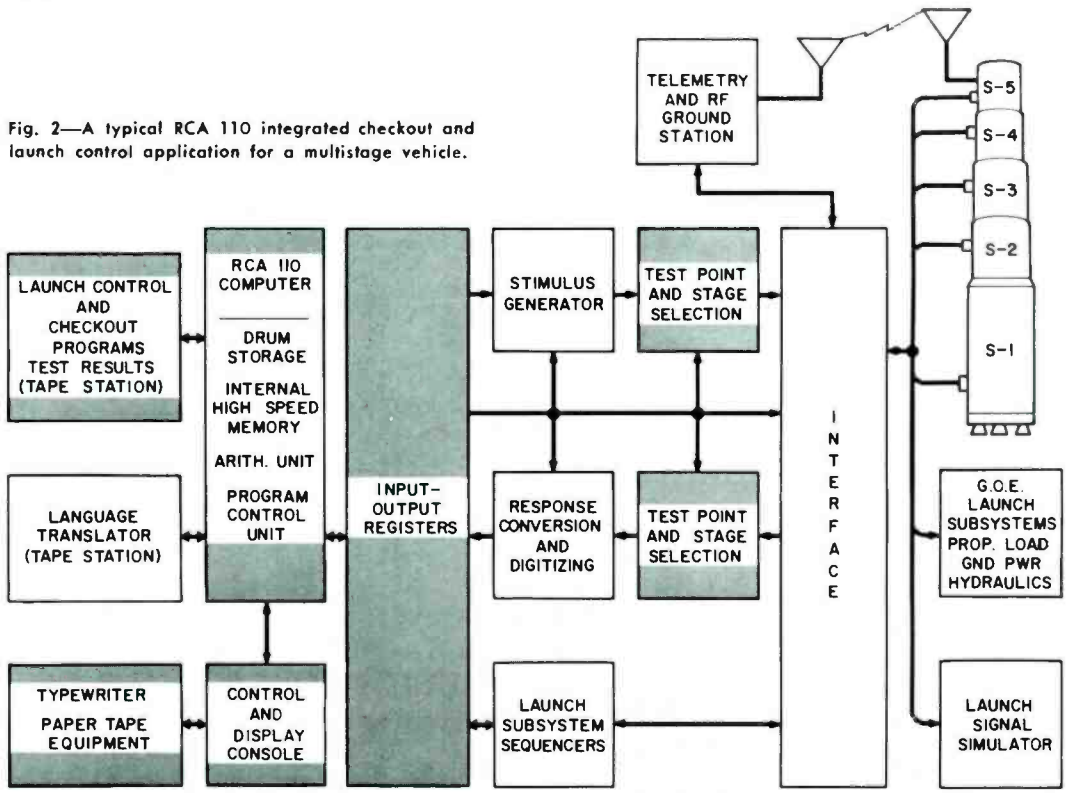
The RCA 110, originally a computer designed for industrial control, is now being utilized by the DEP Data Systems Division in its design of a high-speed checkout system for the NASA SATURN program. This new system will allow high-speed handling of the large amounts of data generated during checkout of the huge SATURN launch vehicles. The RCA 110 checkout system achieves operational speeds of 15,000 discrete and 2,000 analog signals per second. It has a 936-kc clock, 9.7-μsec memory cycle, and 28.85-μsec word time including access. A 24-bit word length yields data accuracies better than one part in eight million.

Fig. 2—A typical RCA 110 integrated checkout and launch control application for a multistage vehicle.



THE RCA 110 checkout system described herein evolved from the general-purpose, high-speed, real-time RCA 110 digital computer originally designed for industrial process control.[1] The DEP Data Systems Division developed this new RCA 110 system application to provide the speed, real-time control, reliability, flexibility, and precision required for automatic checkout of the large boosters of modern space vehicles. The SATURN checkout systems consist of RCA 110 computers and peripheral switching units designed by DEP-DSD for the NASA Marshall Space Flight Center, Huntsville, Ala., and the Launch Operations Center, Cape Canaveral, Fla.

DESIGN GOALS

Highly successful utilization of over eighty RCA APCHE (*A*utomatic *P*rogrammed *C*heckout *E*quipment) units,[2] an externally programmed system for the ATLAS tactical missile program, led to application studies of the internally programmed RCA 110 to meet design needs for greater checkout capacity, speed and reliability as dictated by the development of increasingly complex vehicles.

Application of the RCA 110 computer resulted in an operational speed increase from 2 cards, 300 discrete and 6 analog signals/sec with APCHE to 15,000 discrete and 2,000 analog signals/sec with the RCA 110. A prototype system (Fig. 1) was developed in 1961 and shipped to Marshall Space Flight Center, Huntsville, Ala., where it has been used for training and simulation work. A second system was installed there in December 1962.

Application of the RCA 110 Computer to the checkout of large aerospace vehicles has resulted in the following advantages:

1) Effective handling of greater number of parameters.
2) Increased operations.
3) Increased frequency of checks in a limited time period.
4) Rapid and accurate location of trouble points.
5) Greater reduction of errors due to the human element.
6) Flexibility permitting the checkout system to keep up with continuous improvement in vehicle performance.

CHECKOUT SYSTEM FEATURES

The SATURN ground computer systems under production for NASA operations consist of eight cabinets (three main frame, five peripheral). Each system includes a typewriter, a paper tape reader, and a paper-tape punch. Peripheral equipment consists of the analog and discrete switching units, power supplies and tape stations.

Speed of operation is an outstanding feature of the system. With a 936-kc clock, a 9.7-μsec memory cycle and a 28.85-μsec word time (including access) sufficient speed is available to perform all calculations and make control decisions as rapidly as test condition require in real time. Precision of data in checkout operations is provided by the 24-bit word length of this system yielding an accuracy of better than one part in eight million.

A feature of considerable importance to checkout operations for a launch complex is the power-failure arrangement of the SATURN ground computer system. Interruption of power to the SATURN ground computer system activates a power-interrupt sensing device, initiating an automatic program; a nonvolatile core memory stores all registers whose contents must be known in order to return to the proper point on a program, and then shuts the machine down in proper sequence. Upon reapplication of normal power, the computer starts in its usual sequence, ready to resume operations from the point of interruption.

An automatic priority-interrupt scheme allows the computer to interrupt a program to accept one of higher priority, automatically store the contents of all registers whose contents must be known in order to return to the proper program point, and then return to the same point in the interrupted program and resume interrupted operations automatically. Multiple priority interrupts can occur, causing the computer to step up through several levels of priority and back down again to the program originally interrupted. This permits each incomplete program to be finished when time is available. With this method, a checkout system constantly monitors the status of all subsystems and recognizes changes in status, including those subsystems already checked out. Automatic self-checking is normally programmed whenever computer time is available by assigning such operations the lowest priority level.

The validity of all data transferred between drum memory, core memory, and arithmetic unit is verified by parity checks. The address of an instruction causing a parity error is automatically stored to aid the operator in finding the trouble quickly.

Buffering allows the computer to perform calculations and input and output instructions simultaneously without reducing computing speed. Thus, the computer can be programmed to switch to alternate programs or take other emergency steps upon the occurrence of parity, overflow, or instruction code alarms while the condition is being corrected.

Programming flexibility is enhanced by the large storage capacity provided by both the high-speed working storage (4,096-word core memory) and the drum bulk storage (32,768-word capacity).

CHECKOUT OF MULTISTAGE SPACE VEHICLES

The SATURN ground computer complex is being phased into the SATURN system as a launch-control device for the entire launch vehicle. Fig. 2 shows the RCA 110 computer in a typical integrated checkout and launch control system for a multi-stage vehicle. The sections shaded are being provided by RCA under present NASA contracts.

Launch control and checkout programs stored on magnetic tape or in the drum memory are first transferred to the core memory; they are then available under program control. During tests, stimuli are transmitted to the appropriate stage or vehicle test point by input-output registers and the test-point and stage selector. The response is returned from the test point via a similar route and after processing can be displayed, stored on magnetic tape, punched out on paper tape, or printed out on hard copy.

The interface unit applies tests to any stage of the multi-stage vehicle, the Aerospace Ground Equipment (AGE), or to the launch signal simulators to permit overall system tests without lift off. Similarly, calibration and tests of the telemetry subsystem can be made by comparison with hard wire values.

COMPUTER SYSTEM OPERATION

The SATURN ground computer system utilizes the RCA 110 computer as a central control unit communicating with other equipment through peripheral, input-output units. Each class of signals (command, response, analog, discrete) is handled through its own channel, under computer control, and enters or leaves the computer through the appropriate input-output buffer.

Fig. 3 illustrates how the RCA 110 handles various classes of stimuli or signals. In the analog signal loop, a digital word is read out of the computer into the digital-to-analog (*D-A*) converter registers. These registers in turn drive the *D-A* converters to provide stimuli for the vehicle AGE. The analog response of the vehicle or of the AGE is received by

W. M. McCORD attended Rensselaer Polytechnic Institute, Carnegie Institute of Technology, the University of Michigan, and obtained his MSEE from Harvard University. He has completed graduate courses at the University of California, Los Angeles. His 20 years of engineering experience are in the fields of radar, computers, missiles, and engineering administration. Mr. McCord's responsibilities have included that of project manager, electronic section chief, and chief engineer. Among the engineering programs he has been associated with are: terminal guidance equipment for the TALOS Missile, BOFTE automatic checkout equipment for the TERRIER system checkout, the CORPORAL missile system, and the DYNASOAR hypersonic glider program. In his present capacity, Mr. McCord's principal duties are concerned with the ATLAS automatic Launch Control and Checkout Equipment, the SATURN computer system for automatic checkout of the SATURN launch vehicle, and various display and control projects. Mr. McCord is a senior member of the IEEE and a member of the Army Ordnance Association.

the analog input area (this consists of the analog multiplexer, the analog-to-digital *A-D* converter, and the analog input register) and converted back to digital form for handling by the central control computer.

The discrete signal loop generates 28-volt command signals. These command signals are supplied by the command register and associated discrete output registers and drivers as stimuli to the vehicle or to AGE. Here, 1,008 independently controlled signals can be set up in the discrete output registers. The discrete response of the vehicle or AGE is received in the discrete input section via the discrete signal selector.

A total of 1,008 discrete inputs can be connected to the discrete signal selector, which in turn routes 24 discretes at a time (24-bit word) into the computer.

The input and output registers are general-purpose, standard-word-length, 24-bit buffer registers with synchronization logic added for *data ready, data received, strobe*, and *reset* signals. These registers provide the communication link for a remote computer, the payload, and the digital-data acquisition system. Two 27-bit registers with synchronization logic provide the communications link for the airborne computer. The clock selector enables the programmer to read any one of the three time sources: countdown clock, eastern standard clock, or internal timer. The input-output registers enable the programmer to select discrete output registers, analog input signals, clock input and discrete input signals. All inputs (input registers and sense lines) and outputs (output registers and address lines) are under computer program control. The input-output complements of the SATURN ground computer complex consist of 8 input-output registers, 192 address lines, and 192 sense lines.

INPUT-OUTPUT DEVICES

Input-output register *O* is implemented with the control logic required to control and operate the input-output equipment being furnished with the computer system. The input-output equipment consists of a magnetic tape station with a 15,000-character/sec rate, a 60-character/sec paper-tape reader, a 60-character/sec paper-tape punch, a 10-character/sec electric typewriter, and a display and control console. The display and control console presents data on a 21-inch direct-view storage tube, either in message form or as a labeled plot of the element under test, as requested by the operator. Control of the computer and console is via typewriter-type keyboard and control switches. The display presentation is made up of 0.2-inch-high characters for good legibility and brightness in high ambient light viewing. Up to 1,600 characters can be presented in 0.2 seconds, with a holding time in excess of two minutes.

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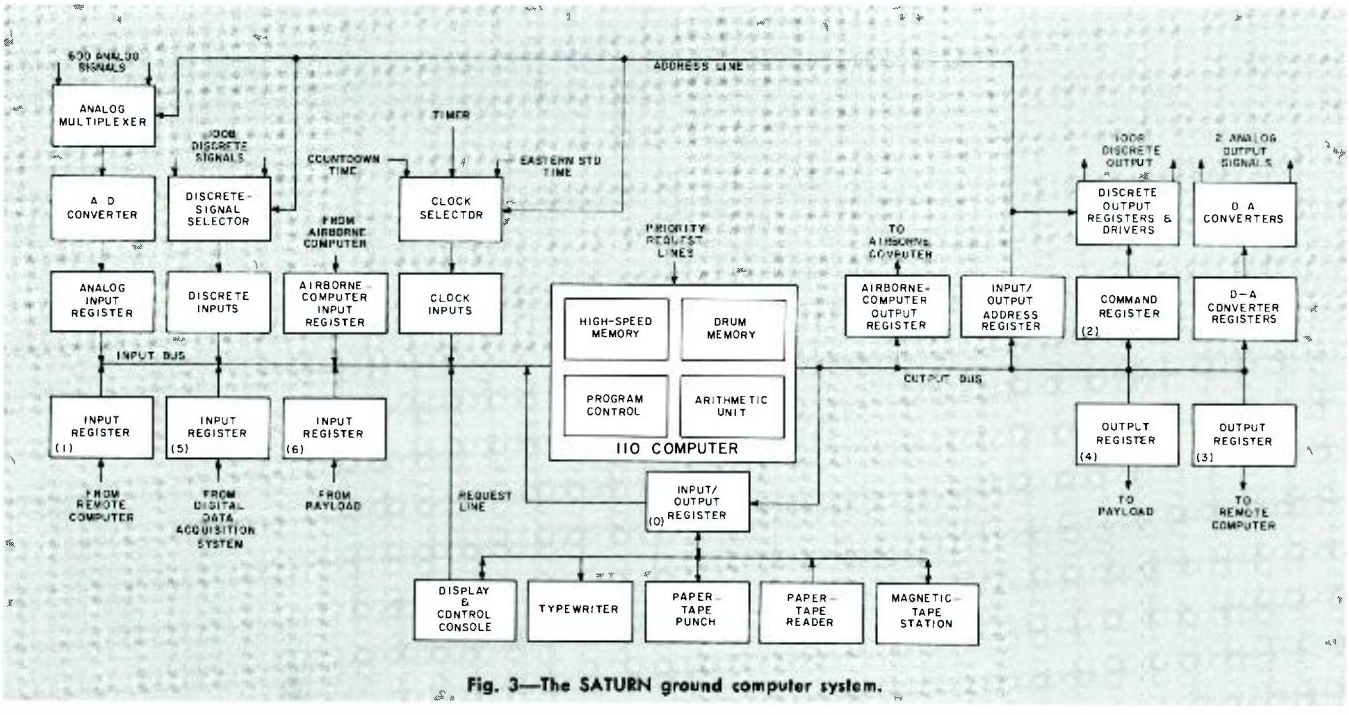

Fig. 3—The SATURN ground computer system.

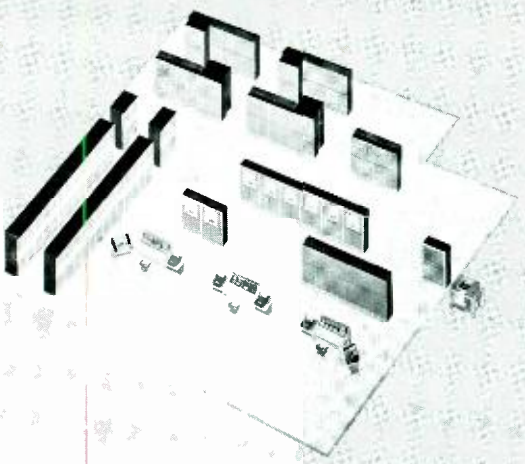

Fig. 1—ETS equipment arrangement at RCA Communications central telegraph office, New York.

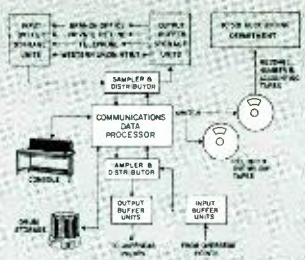

Fig. 2—The Electronic Telegraph System.

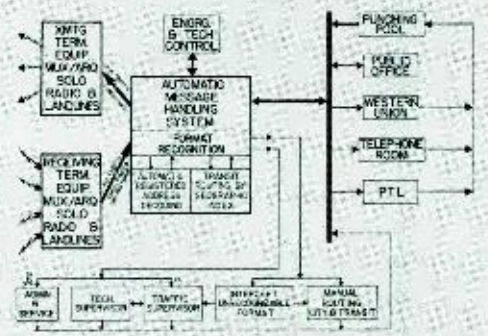

Fig. 3—Interconnection of traffic sources and loads to the Electronic Telegraph System.

A COMPUTER SWITCHING CENTER FOR INTERNATIONAL TELEGRAPH COMMUNICATIONS

At RCA Communications, Inc., central-office problems associated with handling large volumes of telegraph traffic in a global communications network will be effectively controlled by utilizing a pair of high-speed stored-program digital computers.

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New York City, N. Y.

TELEGRAPH COMMUNICATIONS commenced when Samuel Morse invented the telegraph and developed the code bearing his name. From these early days in 1837 until the 1930's, each circuit required a highly skilled Morse operator to hand-key the circuit and decode aural or ink-recorded signals into typewritten messages. The vagaries of the early radio circuits in the form of noise and fading were substantially overcome by the skill of the operator and the redundancy of the language.

MECHANIZATION BEFORE WORLD WAR II

Prior to World War II, printing telegraph machines using the 5-unit Baudot code were introduced as a first step in the mechanization of communications networks. In 1944, when RCA's international traffic reached 150 million paid words per year, mechanization was extended again with the introduction of the torn-tape relay system in its central telegraph offices. Incoming and outgoing messages were converted to perforated tapes and relayed to a tape transmitter associated with each transmitting channel. Further refinements were introduced into the torn-tape relay system such as multiple-teleprinter receiving and transmitting positions; however, the basic message handling functions of reception, sorting, routing, distribution, message sequence protection, and transmission still required extensive manual attention.

POST-WAR AUTOMATION

As the international public message traffic continued to grow (over 250 million words by RCA in 1960), the problems associated with manually handling such large volumes of perforated tapes made it increasingly difficult to maintain the necessary speed of service economically.

In 1956, an investigation was made of the possibilities of fully automating the international public message service. After examining several electromechanical systems, it became evident that existing approaches to the problem of automatic message switching were not sufficiently flexible to handle the wide range of international operating problems.

THE COMMUNICATIONS DATA PROCESSOR

By 1957, RCA Communications, Inc., with the cooperation of RCA Electronic Data Processing, began planning an *Electronic Telegraph System* utilizing high-speed stored-program digital computers. When it became evident that the existing RCA commercial computers were not suited to on-line communication requirements, a new-generation processor, the *Communications Data Processor* (CDP) was born.[1,2] This machine, designed as a real-time computer, examines and switches international messages to their proper destinations in milliseconds instead of the cross-office, perforated-tape relay time measured in minutes. Messages from 69 countries via 500 million route miles of radio and cable links will move continuously through the CDP as rapidly as the international communications links can carry the load.

SYSTEM OBJECTIVES AND DESIGN CONSIDERATIONS

The CDP will handle, through its 100 full-duplex channels (simultaneous reception and transmission), all classes of message traffic and all types of service communications flowing through the central telegraph office. Each message entering the CDP is automatically examined to determine the proper routing, and then switched to the proper outgoing channel by precedence in chronological order. When all desired destination channels are occupied, the message will be queued up in the intermediate drum storage to await its proper turn. As rapidly as each outgoing circuit becomes idle, the CDP will automatically select, in chronological order, the highest priority message within the system for transmission.

In addition to the prime task of routing messages, the CDP has been programmed to perform the following control, service, and accounting functions:

1) Verify sequence of inward channel message number.
2) Automatically insert an outward channel message number.

ROY K. ANDRES received the BSEE from New York University and attended MIT for graduate studies in switching and computer theory. Mr. Andres joined the Engineering Department of RCA Communications in 1946 where he participated in the conversion of international radio-telegraph circuits from Morse operation to the 5-unit printing telegraph torn-tape system. Since 1946, he has engaged in development of 5-unit telegraph switching systems, multiplex systems, automatic switching systems for microwave links, and data transmission systems; he holds patents in these and other fields. Presently, Mr. Andres is responsible for Automation and terminal Systems Engineering. In 1963, he will complete all operational aspects of the new Electronic Telegraph System using high-speed, stored program, digital computers. Final automation of the worldwide Telex network will also be completed permitting direct keyboard-to-keyboard conversation. Mr. Andres is a member of the IEEE and the professional-technical groups on Circuit Theory, Communications Systems, Electronic Computers, and Medical Electronics.

3) Record and print out a list of the inward message numbers with their corresponding outward message numbers for each channel.
4) Recognize the international four-letter destination code; when absent, examine the address line for city and country of destination, and look up the proper destination code in the internal geographic index.
5) Recognize registered addresses, compare them with the internally recorded directory, and insert the necessary code for local delivery.
6) Recognize and establish precedence in forwarding all messages.
7) Provide facilities for retransmitting messages when necessary.
8) Provide a long-term record storage (6 months) of all messages flowing through the central office.
9) Provide automatic detection of lost messages and character distortion within the system.
10) Edit and extract necessary information from each paid message for automatic customer billing and settling the international traffic accounts.

MESSAGE FORMAT

In any automatic message handling system, it is desirable to add certain basic elements to every message transmission in order to 1) distinguish the starting point and ending point of each message, and 2) direct the equipment to route each message to the proper circuit and ultimate destination.

During a 1960 International Communications Conference in New York sponsored by RCA Communications, Inc., an internationally acceptable message format was formulated and introduced as a recommendation to the CCITT (Consultative Committee on International Telephone and Telegraph). In February of 1962, this recommendation was adopted in Geneva and forwarded to the International Telecommunications Union for final ratification by all member countries.

This new format will include a "pilot-line" in the preamble of each message which contains a four-letter destination code, two-letter priority and class-of-service code, origin code, and the number of paid words in the message.

In addition to these indicators, it is desirable to obtain the worldwide use of a signal to appear at the start of the address line in order to permit the equipment to locate a Registered Address for automatic routing. The dash (—), which is signal No. 1 of the international five-unit alphabet in the upper case, was recommended for this indicator.

TRAFFIC FLOW

The traffic from local or domestic sources, prepared in the required format, will enter the system through the input buffer storage units. These buffers will perform the necessary speed change from the comparatively low-speed teleprinter equipment (50 to 150 baud) to the high internal speed of the CDP. The traffic is stored in the computer, examined for destination and priority, and switched to the overseas channel by priority in chronological order.

The ouput buffer units similarly convert the high internal computer speed to the relatively low speed of the overseas transmitting channels and the local teleprinter equipment.

Traffic received from overseas points enters the system through input buffer units, to be stored and examined within the CDP, and routed out through an output buffer unit to the proper delivery point. A monitor copy of all traffic passing through the system will be recorded on magnetic tape for future reference.

All locally originating traffic destined for overseas points will be examined for the required accounting and billing information and recorded on magnetic tapes for later processing as an off-line function into customers' bills.

The individual input message channel numbers of all processed messages will be checked for proper sequence and recorded on magnetic tape along with corresponding automatically-assigned output channel number. This continuous automatic check of message channel numbers will assure the continuity of all traffic through the system and the immediate reporting of any irregularity.

COMMUNICATIONS DATA PROCESSOR

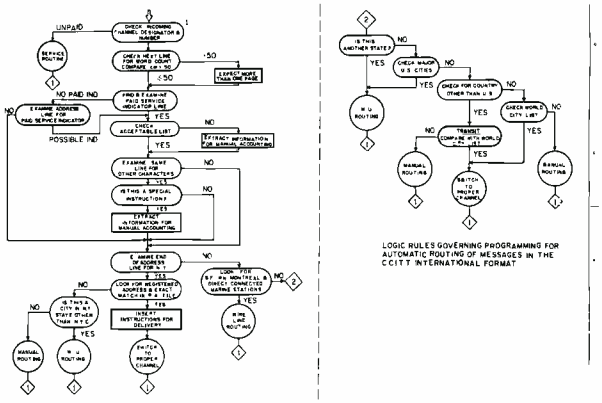
The CDP, a high-speed stored-program digital computer, is designed to accept and deliver (through line buffer transfer channels) data to and from a large number of channels simultaneously. Since the internal operating speed of the CDP permits character handling rates up to 2.5 million characters/sec, the total incoming and outgoing communications load of all channels (3,000 characters/sec) only consumes a small fraction of the available CDP time. The remaining CDP time is available to perform the necessary logic functions associated with examining the message format, comparing this information with recorded tables of routing instructions, transferring the message from one storage point to another and controlling the flow of traffic to all output channels.

STORAGE FACILITIES

Since many system functions will require message storage facilities of different capabilities, three principal methods of storage are used in the system: magnetic cores, drums, and tapes.

Magnetic cores are used for the high-speed memory of the CDP. The core memory of each CDP has a capacity of 131,072 characters and a read-write cycle time of 1.5 μsec. (The read-write cycle is the minimum time to record and recover information in the computer memory).

Fig. 4—Electronic Telegraph System block diagram of dual communications data processors and associated storage, input, output, and control devices.



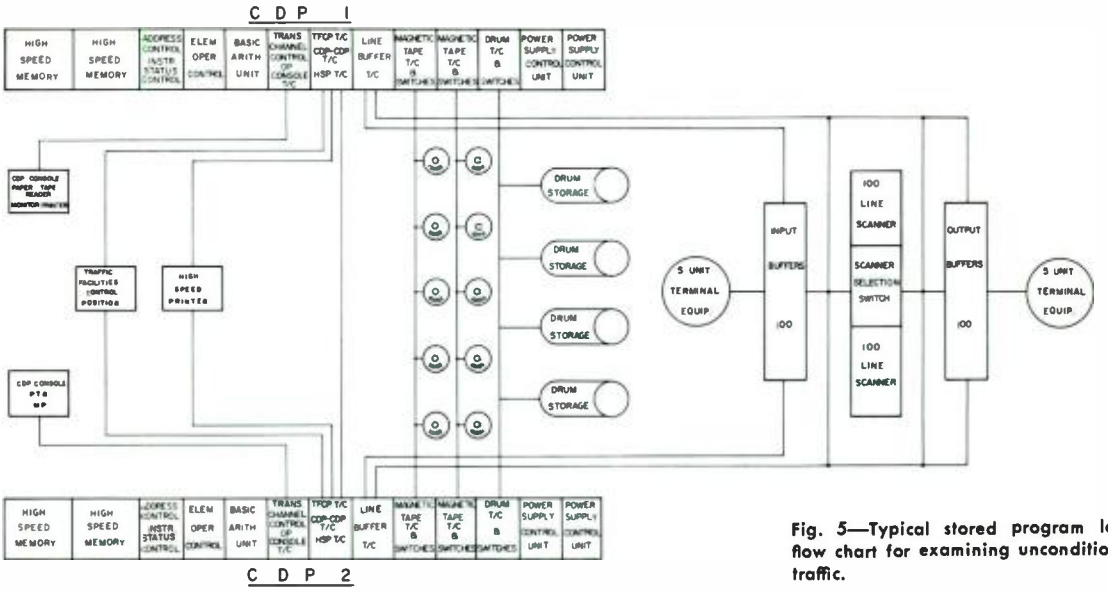


Fig. 5—Typical stored program logic flow chart for examining unconditioned traffic.

The high-speed memory along with the CDP logic operates with a duty cycle of 2.0 μsec and is used for storing the CDP program instructions, message accumulation and distribution, destination tables, queue lists, code conversion and working storage for message processing.

Four magnetic drums, each with a capacity of 384,000 characters are used for storing information which does not require the extremely short access time provided by the core memories. The average and maximum access time for any information stored on the magnetic drums is 33 milliseconds and 66 milliseconds, respectively. Two drums are used for *intermediate message storage* and *short-term reference storage* (rerun) providing a capacity for 1600 to 2000 average messages. One drum is used for *short-term reference storage* facility provides the ability to retransmit any of the last 800 to 1000 messages to leave the system without having to refer to the record copy in the magnetic tape. The third drum contains 12,000 *registered addresses* and their routing instruction codes and a *geographical index* of 150,000 characters for the world's cities and countries in three languages. The fourth drum operates as a floating spare.

Standard RCA 581 magnetic tape stations operating at 33,000 character/sec are used for providing overflow storage, permanent monitor copies of all traffic and for recording the message numbers and accounting information.

BACK-UP BY DUAL CDP'S

The requirement for continuous 24-hour service precludes the use of scheduled service periods for routine preventive maintenance. In order to insure continuous operation, the system employs two CDP's, each programmed to handle the full traffic load. Since crucial areas of possible common equipment failure involve the input accumulation cycle in the high-speed memories, the second CDP will perform these functions simultaneously.

Similarly, the queue lists will be assembled simultaneously in both high-speed memories so that the second CDP will be continuously aware of the location of every message in the system. It is, thus, possible to switch from one CDP to the other without interrupting traffic flow.

EXPANSION

The Electronic Telegraph System was designed to initially accommodate 100 input and 100 output telegraph channels each operating at speeds of 60 to 150 words/min or 6 to 15 characters/sec. The input-output capacity of the system, however, is not limited to this number of channels but is limited only by the available CDP operational time. Expansion of the number of input and output channels may be accomplished by adding more line sampler and distributor units and more input-output buffers. Additional high-speed memory may also be required to provide accumulation, distribution, and queue table areas for the new channels if contractions in the existing stored programs do not release sufficient memory area.

The high quality of transatlantic and transpacific coaxial cable channels permits the use of these channels for very-high-speed serial bit streams. In this application, the CDP can be programmed to transmit high-speed serial bit streams directly to wideband channels by changing the output buffering.

Digital data transmission shows much promise for the future and may develop in the direction of datagrams or filed data messages which could be handled by the system in much the same manner as regular message traffic. This form of service would offer data transmission facilities to subscribers not having sufficient volume to justify a private leased channel.

CONCLUSIONS

When considering the wide range of problems presented by a global communications network, electronic message switching implemented by stored program computers offers a communications facility with maximum flexibility and large growth potential. The inherent advantages of operating and channel loading efficiency, speed of service, and economy of international trunking facilities represent a major advance in the international communications field.

The expansion of multiple-channel coaxial-cable facilities and forthcoming satellite systems with their extremely wide bandwidths further emphasizes the necessity for greatly improved terminal message handling equipment. By utilizing the flexibility of Communication Data Processors, the full potential of advanced communications channels in all mediums can be realized. With a fully developed network of automatic electronic message handling systems, global communications with uniform procedures could provide the speed and variety of service required by an ever expanding communications need.

ACKNOWLEDGEMENT

The author gratefully acknowledges the assistance of L. P. Correard in preparing the figures included in this article.

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ENSURING SUCCESSFUL COMPUTER INSTALLATIONS

. . . the training of Computer Service Representatives

The rapid growth of RCA in the electronic-data-processing field has necessitated, on the part of the RCA Service Company, the development of a new breed — the RCA "computer service representative" (CSR). To install, maintain, and trouble-shoot complex electronic and electromechanical equipment, the CSR must be familiar with all related areas, such as computer programming and operation. Hundreds of such trained technical personnel are needed to install and maintain an ever-increasing number of RCA 301, 501, and 601 data-processing systems — which has led to the comprehensive program of personnel selection and training described herein.

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MOST OF THE training of the RCA computer service representatives (CSR's) takes place at the Electronic Data Processing Services (EDPS) Training Center of the RCA Service Co., located at Cherry Hill, New Jersey. The modern training facilities at the Center include classrooms and laboratories capable of handling an enrollment of several-hundred CSR trainees. The Center has its own RCA 301 and RCA 501 Systems. The equipment complement for each system is carefully selected to be representative of a typical customer's installation. Oscilloscopes and other test equipment, gauges and jigs, hand tools, and operating supplies such as magnetic tape and EAM cards are all duplicates of the equipment and supplies to be used by the CSR when assigned to a customer's installation.

WHO IS TRAINED

There are many classes held simultaneously at the Training Center on a variety of RCA data-processing equipments. Most of the technical personnel attending these classes are new employees who, after completing their training, will be assigned to a forthcoming computer installation. Also, there are a number of experienced field personnel who have returned to the Training Center to receive additional training, either in the form of advanced courses on certain pieces of equipment, or on an entirely new system. The majority of RCA's trained CSR's are capable of maintaining several types of RCA data-processing systems.

HOW TRAINING PROGRAMS ARE PLANNED AND REVIEWED

The development of a maintenance training program for a data-processing system begins many months *before* the delivery of the first system. As soon as preliminary engineering drawings are available, a team of instructors begins working with the design engineering group. By combining the knowledge obtained in working alongside the design group with their experience in developing data-processing training programs, these instructors prepare a preliminary specification for a maintenance training program. These specifications, together with the sales forecast for the system and anticipated delivery dates, provide the basis for estimating manpower requirements and hiring dates.

The training team continues working with the design engineers to develop the preliminary course outlines, lesson plans, and training notes. As the design work proceeds, and engineering drawings become final, the team completes the initial preparation of various sections of the program. These sections then enter the review phase.

Copies of the documentation for these sections such as the preliminary training manuals and notes, outlines, timing charts, and signal source lists, are submitted to the appropriate design activity for technical review. Concurrently, decisions are made to determine the mode of presentation, the types and numbers of training aids required, the method of reproduction and quantities of training manuals required, and the number of lecture and laboratory training hours required for effective presentation.

Close cooperation must be maintained with the engineering activity of RCA Electronic Data Processing throughout the design, development, and prototype testing of a new design. The training team benefits from the experience gained from engineering and manufacturing personnel engaged in the testing of prototype. By examining engineering data compiled during testing, noting areas requiring more precise and more frequent maintenance than others, the training team can modify previously prepared course material by giving proper emphasis to sensitive maintenance areas.

The maintenance training and engineering support capability must be achieved by the EDPS activity prior to the delivery of the first system to a customer (peripheral equipment released at later dates may require a different approach). Therefore, at periodic intervals during the design and development of the computer system, the initial delivery schedule, is reviewed, and estimates of manning requirements and hiring dates prepared. These estimates are reviewed

Fig. 1—A classroom training session on the RCA 301 computer; the Instructor is Don Schulman.

Fig. 2—Trainees shown working on high-speed memory alignment of the RCA 301 during a Training Laboratory session: l. to r. are Instructor, W. Harrison, Kurt Koster and Jim O'Brien.

by the EDPS Personnel activity. An appropriate lead time of one to three months for recruiting is allowed.

SELECTION OF TRAINEES

The selection of CSR candidates is a painstaking process. For every class of ten to fifteen trainees hired, hundreds of applicants may be interviewed and tested. Most candidates are selected from the top graduates of a technical school, such as the RCA Institute. A battery of selection tests is administered to preselected applicants. Tests include aptitude, general intelligence, abstract reasoning, logical reasoning, and mechanical comprehension, as well as technical knowledge. As a result of the close screening in the interviewing and selection process, the number of later dropouts is minimized. Although the present selection of techniques are comparatively successful, the EDPS Personnel and Training activities are continuing in an effort to further define the aptitudes and traits of successful students.

A TYPICAL TRAINING CYCLE

Most of the CSR trainees are presently being trained in the maintenance of the RCA 301 system. This typical training program is 17 weeks in length, and is divided between lecture classes providing a detailed knowledge of system functioning, trouble-shooting, and laboratory training on the equipment at the Training Center. Here, the trainee's skill of utilizing his knowledge to isolate and repair equipment malfunctions is developed.

Courses Studied

The training program begins with a basic course to provide background for the detailed study of the logical design of the system. Some of the topics included in this course are *numbering systems, binary arithmetic operation, transistor and diode switching circuits, logical elements,* and *magnetic core memories.*

The next course covers the *design philosophy, programming, operation,* and *maintenance* of the computer. Other courses cover the various *input-output buffers* and the *peripheral input-output devices* used in the 301 system.

Included in the weeks the trainee spends working with the equipment at the Training Center are courses on the *installation* of a 301 system, *preventive maintenance procedures,* the *assembly and disassembly* of the electromechanical peripheral equipment. Also covered are *test and maintenance programs* in performing preventive maintenance and isolating equipment malfunctions. Equipment malfunctions are induced by inserting defective components into the system. The types of failures simulated are based on a study of equipment failures in the field. However, primary emphasis is not made on specific problems and their solutions, but on the development of the trainee's approach to the solution of the problem.

Upon completion of the training at the Center, most CSR trainees undergo a period of on-the-job training. During this period, they work closely with experienced personnel in maintaining and trouble-shooting data processing equipment. As their experience increases, the degree of assistance required diminishes. This final phase concludes training on the computer. Then, the CSR is considered ready for an assignment.

OTHER TRAINING AIDS

The lecture and laboratory courses which compose the 301 training program are supplemented by a variety of training aids and manuals. Training manuals, encompassing thousands of pages, are utilized not only as texts in the various courses, but also as reference manuals by field personnel. Such manuals are developed by instructors for use in their training courses and are sufficiently comprehensive for experienced field personnel to use in "on-site" refresher courses. Engineering, programming, and methods personnel also find the manuals to be of considerable value. Contents of manuals are translated into French and Japanese.

OTHER TRAINING-CENTER COURSES

The courses used in the RCA 301 training program are only a few of those conducted at the Training Center. At the present time, courses are conducted on more than fifty individual items of data-processing equipment, ranging in length from a few hours study for a specific course on paper-tape handling equipment to several months on the more complex equipment. Specific courses on data-processing equipment, classes in operating and programming, and introductory seminars in data processing and computer logic are conducted for other activities within RCA. Courses of this type are tailored to fit the needs of the personnel enrolled. As a result of the sale of RCA data processing systems to other countries, the Training Center has conducted training programs for engineers and technicians from Sweden, England, France, Japan, South Africa, and Australia. Upon completion of their training, these people have returned to their native countries to establish their own maintenance, training, and engineering activities.

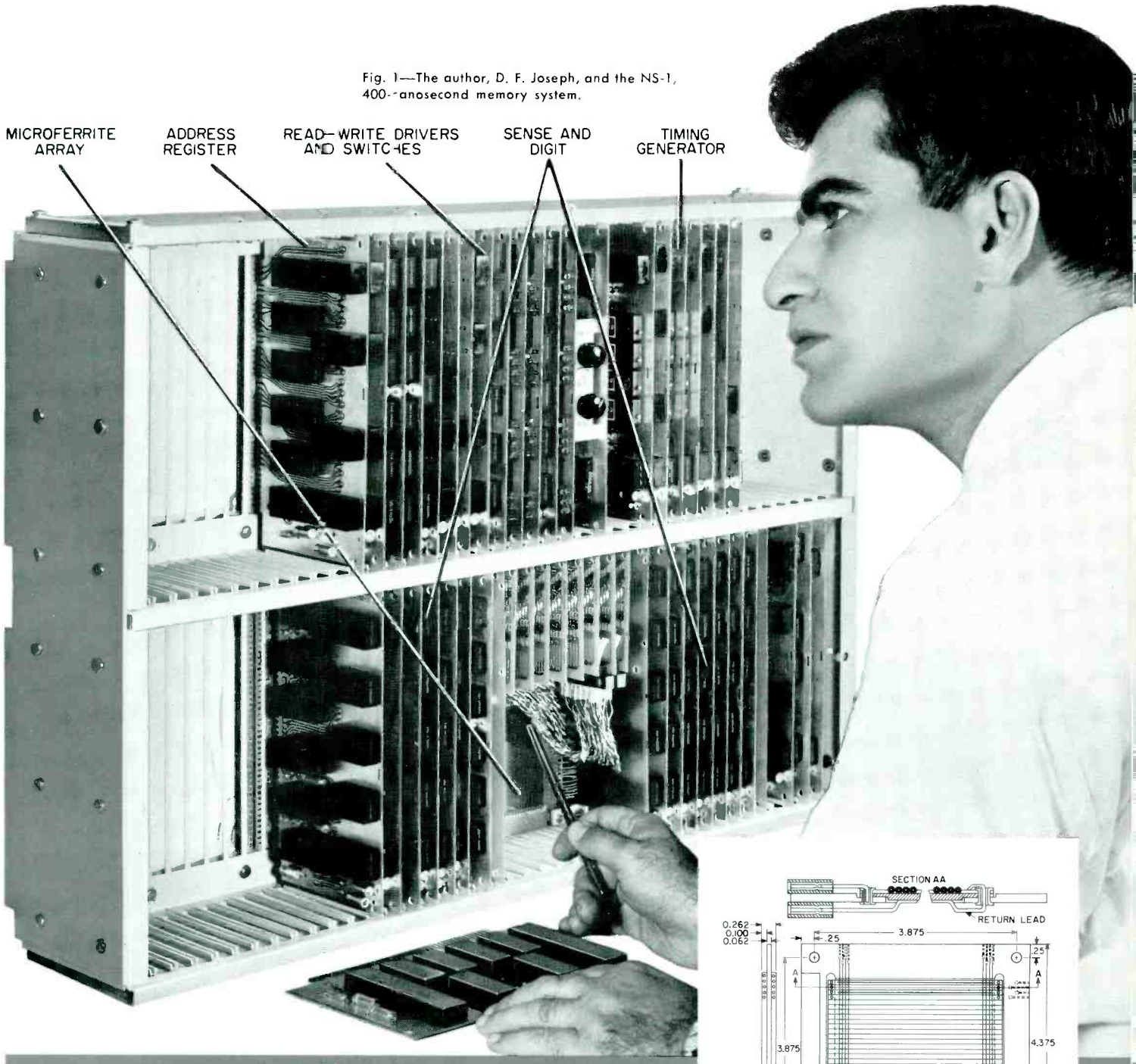
CONCLUSION

As the types and quantities of RCA data processing equipment continue to multiply, the increasingly diversified training requirements will necessitate further development and utilization of new and more-effective training techniques. The feasibility of using programmed learning techniques in various segments of the training program is being studied. In teaching computer operation, an experimental program using the computer itself as a teaching machine has been developed. Research is also underway in the use of simulators and simulation techniques which would minimize the training time required on certain data-processing equipment.

Fig. 3—Some of the RCA 301 computer system training manuals developed by the Instructors. Manuals are used for classroom instruction and for future reference in the field.

MYRON H. MAC DOUGALL graduated from the RCA Institutes Advanced Technology course in 1959, joining RCA as a Computing Equipment Engineer. In 1960, he was promoted to Manager, Laboratory Facilities, EDPS Training, and in 1961 was promoted to his present position of Manager, EDPS Training. He is a member of the IEEE and the ACM.

Fig. 1—The author, D. F. Joseph, and the NS-1, 400-nanosecond memory system.



THE NS1 – A NEW 400-NANOSECOND MICROFERRITE MEMORY SYSTEM

This sub-microsecond microferrite memory has a 400-nsec read-write time and is a random-access, word-organized system of 128 thirty-bit words. Since there are no programming restrictions on the memory, random access may be selected repetitively at the full clock rate of 2.5 Mc. Future basic memory module sizes of 500 to 1,000 sixty-bit words are feasible.

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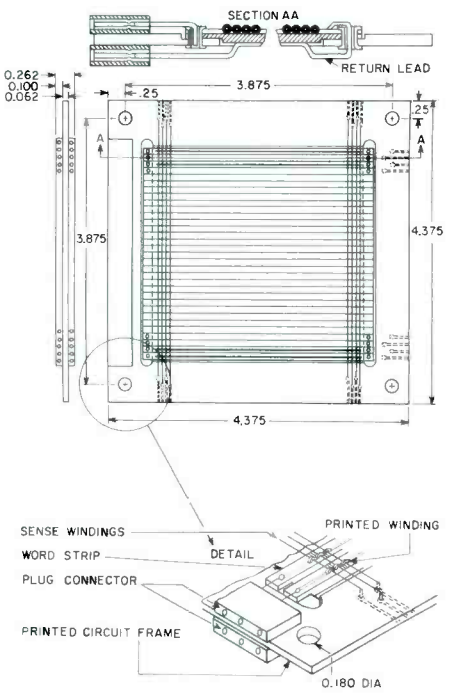


Fig. 2—N7100 microferrite array.

DAVID JOSEPH received his BSEE from the University of London in 1952 and his MSEE from the University of Pennsylvania in 1958. From 1952 to 1953 he was a Graduate Apprentice at the Edison Swan Electric Company in England, associated with the development of vacuum tubes. From 1953 to 1956 he was an engineer at the Bell Telephone Company of Canada, working on transmission problems, and from 1956 to 1958 he was an instructor at the University of Pennsylvania, working full time on a research project pertaining to high-frequency equivalent circuits and measurements of transistors. From 1958 to 1960 he was a Member of the Technical Staff at Bell Telephone Laboratories, working on the development of new magnetic devices and circuitry associated with memory systems. In January 1960, Mr. Joseph joined the RCA Memory Products Operation as Senior Member, Technical Staff in the Memory Systems Engineering Group. He has since been engaged in the design and development of memory systems as an engineer, then as group leader, and now as manager.

IN PRESENT-DAY advanced computer technology, the requirements of memory systems have been directed toward reading and writing in the sub-microsecond region. Of all the techniques proposed for sub-microsecond memories, he word-organized system using partially switched ferrite cores[1] has emerged as the most practical and successful. The ferrite device exists today as an economical production item[2], working models in the laboratory have been reported[3,4] and large sub-microsecond memories have been successfully built and tested.[5]

The Semiconductor and Materials Division's first sub-microsecond memory system, NS1, shown in Fig. 1, operates with a read-write cycle time of 400 nsec. It utilizes microferrite cores as memory elements and is constructed as a word-organized, two-core-per-bit memory system of 128 words of 30 bits each, addressable by random-access means. The memory system is completely solid-state. It uses RCA epitaxial mesa transistors in the logic and sensing circuits, and planar epitaxial transistors in the driving circuits. There are no programming restrictions imposed on the memory; hence, any random address may be selected repetitively at the full clock rate of 2.5 Mc.

Fig. 4—Core states, write 1, bipolar sensing.

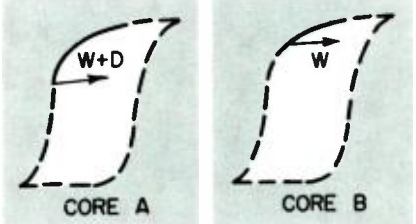
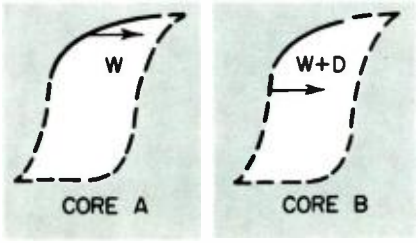


Fig. 5—Core states, write 0, bipolar sensing.



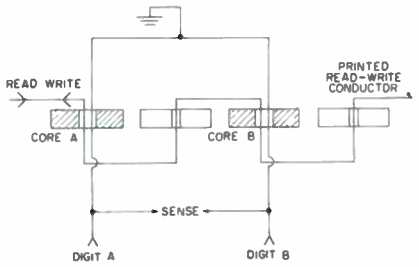


Fig. 3—Bit wiring, two cores per bit.

MICROFERRITE STACK DESIGN

The stack for the NS1 high-speed memory system is constructed of four RCA microferrite N7100 arrays modified for stacking. Each N7100 array consists of 32 word strips (Fig. 2); each word strip is 30 bits (60 cores) long. Microferrite cores have an outside diameter of 50 mils and an inside diameter of 10 mils. The cores are set end to end in each word strip and are connected by electroplated conductors. The word strips are set on 0.1-inch centers. The sense-digit line is strung through the cores in a conventional manner and is tied to terminals at the sides of the frame.

In this application, the printed conductor is utilized as the read-write drive line, and the sense-digit lines are interconnected in series through all four planes.

PRINCIPLES OF OPERATION

The microferrite memory uses two familiar principles of operation, partial switching and two-core-per-bit operation. Partial switching contributes greatly to the speed of operation; the two-core-per-bit arrangement simplifies the driving and sensing circuits. In two-core-per-bit operation, the drive-line load is constant, reversible flux voltages induced by fast-rising pulses are cancelled, and *0* and *1* output signals are relatively easy to discriminate because they are of opposite polarity. Bipolar sensing is used for further improvement of the signal-to-noise ratio.

The above statements are best illustrated by a description of single-bit operation. As shown in Fig. 3, the common read-write conductor is the printed winding along the word length, and the common sense-digit winding is a wire passing through the cores perpendicular to the word direction. For the writing of a *1*, a pulse of proper polarity and amplitude is applied to the read-write winding, while at the same time a pulse of proper amplitude and the same polarity is applied to digit winding *A* of Fig. 3. The resulting core states of the bit are shown in Fig. 4.

For reading, a pulse of proper amplitude but of polarity opposite to that of the write pulse is applied to the read-write winding. The voltages induced by cores *A* and *B* in the sense winding are of the same polarity, but the voltage from core *A* is larger than that from core *B*. The sense amplifier establishes the difference between the two voltages, and the net resulting voltage is read out as a *1*. For the writing of a *0*, the same pulses are applied as in the writing of a *1*, except that the digit pulse is applied to digit line *B* rather than to digit line *A*. The resulting core states of the bits are shown in Fig. 5. When the read pulse is applied to the read-write winding, the

Fig. 6—Digit, read, and write pulses. Horizontal sweep, 100 nsec/cm; vertical sensitivity, 200 mv/cm.

Pulse	Current (I), ma	Rise Time (T_r), nsec	Width (T) (between 50% points), nsec
Read	350	30	100
Write	220	24	48
Digit	70	20	80

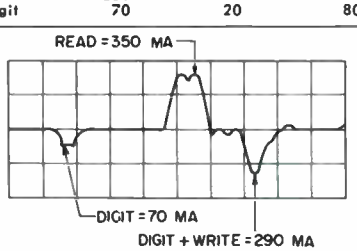


Fig. 7—Bit output from bipolar sensing. Horizontal sweep, 10 nsec/cm; vertical, 50 mv/cm; T_a, 70 nsec.

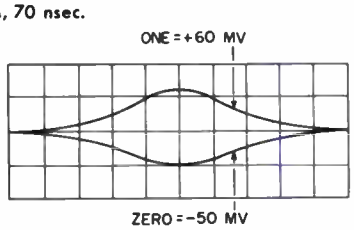
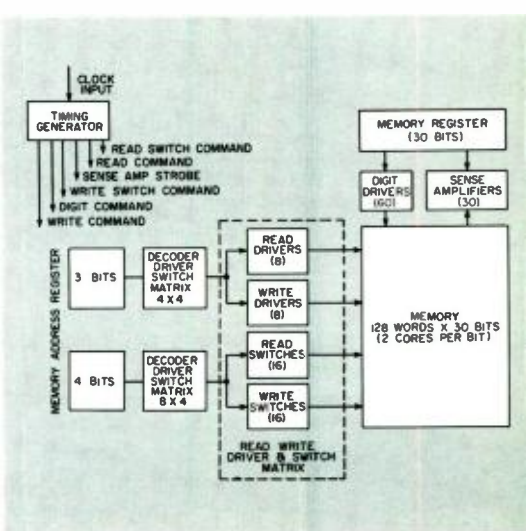


Fig. 8—NS-1 memory system.



voltage induced in the sense winding from core *B* is then larger than that from core *A*. The net resulting voltage in the sense amplifier is then similar to a *1*, but of opposite polarity, and is read out as a *0*.

The read-write and digit pulse characteristics are shown in Fig. 6. Fig. 7 shows typical *1* and *0* outputs of the bit for the pulse characteristics of Fig. 6.

MICROFERRITE ARRAY READ-WRITE DRIVE SYSTEM

Decoding from a seven-bit address register to the 128 word lines is accomplished in two levels by cascaded matrices. These matrices are called the *read-write driver* and *switch matrix*, and the *decoder driver* and *switch matrix*. Fig. 8 is a block diagram of the system.

The *read-write driver matrix* is an 8 by 16 bipolar matrix which drives the word lines through steering diodes. As shown in Fig. 9, there are 8 transformer-coupled read-write driver pairs and 16 transformer-coupled read-write switch pairs. Each word line has 4 matrix diodes located on both the driver and switch sides of the line. Driver current (read and write) is obtained from two current sources, as indicated in Fig. 9.

There are two decoder driver-switch matrices: one 4 by 4 matrix associated with the 8 read-write driver pairs, and one 8 by 4 matrix associated with the 16 read-write switch pairs. The decoder driver-switch is a unipolar-diode selection matrix which drives pulse-transformer primaries (of the read-write drivers and switches) as the matrix element. Fig. 10 shows a typical arrangement.

At the inputs of the decoder driver and switch, *and* gates are required to gate the appropriate read and write timing pulses together with the address levels. Pulse inputs are required only at the decoder driver inputs of the matrix. The decoder switch inputs use address levels to open or close the path to ground for the command pulses. The decoder driver is an emitter follower, and the decoder switch is a power gate.

The driving circuit operates as follows: The memory cycle is initiated by a clock pulse which is fed into a timing generator. (The operation of the timing generator is not discussed in this paper.) Simultaneously, the correct address is selected for the word to be interrogated, and the stabilized address levels appear at the *and*-gate inputs of the two decoder driver-switch matrices, as indicated in Fig. 10. In each of these matrices, one decoder switch is selected and a path is closed to ground for the current to flow in the primaries of the pulse transformers. The read-switch command is then applied, and the correctly addressed decoder driver in the 8 by 4 matrix is selected. A current pulse flows through the primary winding of the selected pulse transformer. The transformer functions as a level shifter to drive the read switch, and sufficient current is produced in the secondary winding to saturate the read-switch transistor.

Normally, the word lines are biased to a potential of 12 volts when no drivers or switches are selected, the outputs of the read drivers are at ground, and the outputs of the switches are at a potential of 24 volts, as shown in Fig. 9. When the appropriate read switch is selected, as discussed above, a ground path is established for drive current to flow. The read-drive command is then applied to the 4-by-4-decoder drive-switch matrix, and a read driver is selected by a similar process. The read-driver transistor is driven into saturation, and the current source is gated through. This current tends to flow to all word lines associated with the read driver; however, the full current flows only through the selected word line and through the selected switch to ground. The matrix diodes associated with the word lines block the flow of current into all unselected word lines. Read current flows for a specified period and is terminated when the read command is disabled and the read-switch command is disabled.

Write current, through the selected word line, is generated in a similar man-

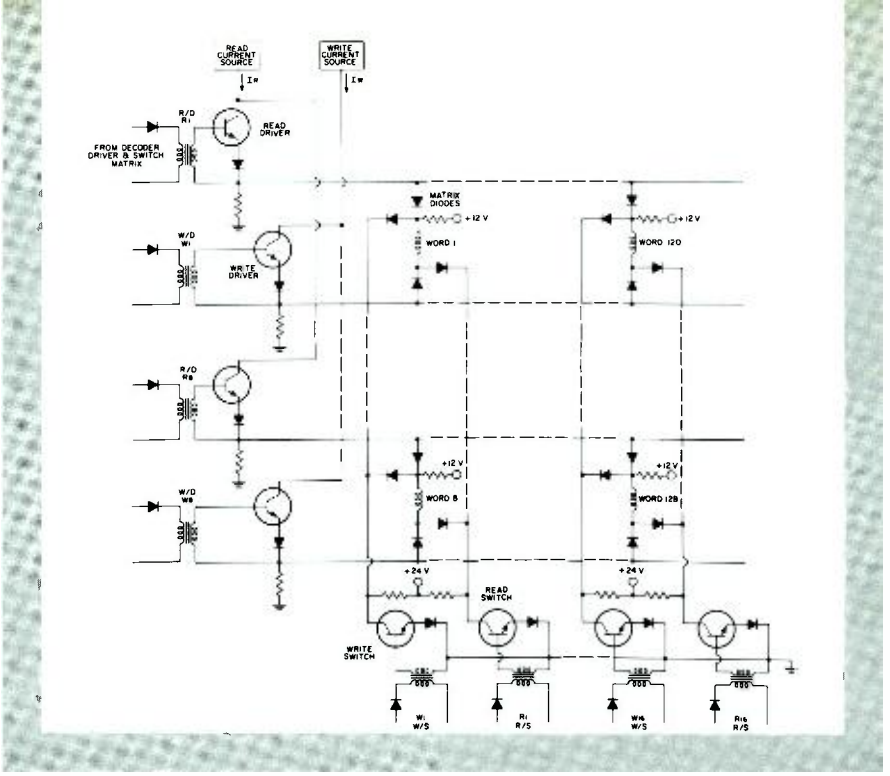
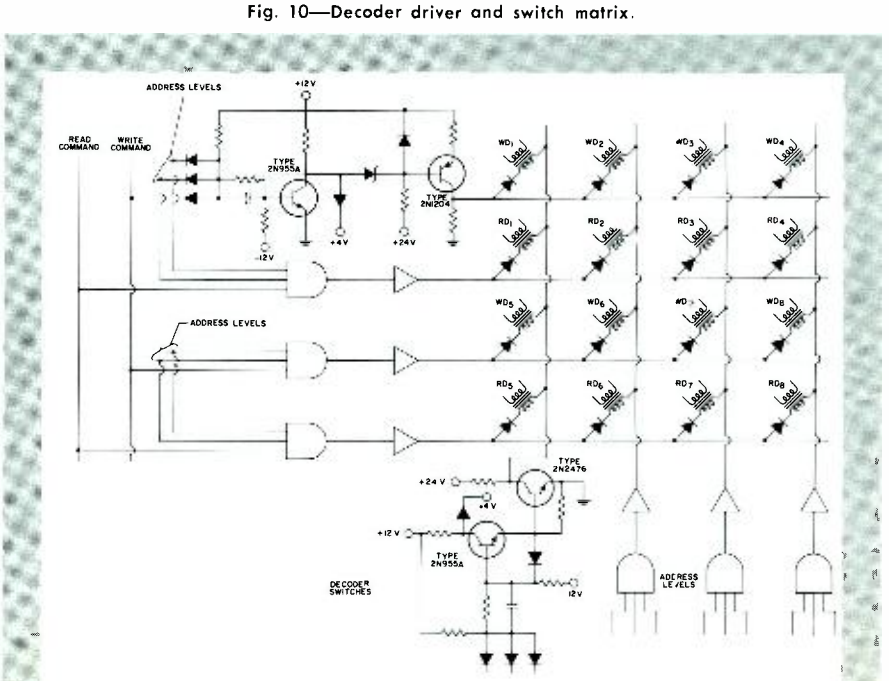


Fig. 9—Read-write driver and switch matrix.

Fig. 10—Decoder driver and switch matrix.



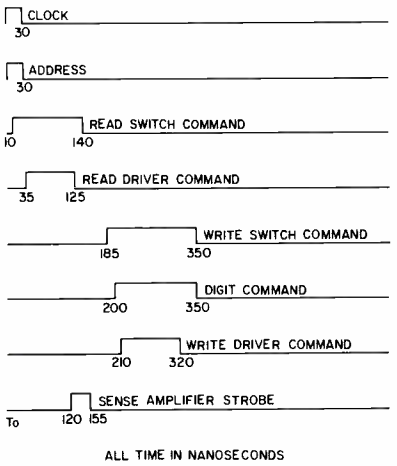


Fig. 11—Timing-generator command pulses.

ner by application of the write-switch command and write command to the decoder driver matrices. Fig. 11 shown the pulse widths and time sequences of these various commands.

SENSE-AMPLIFIER AND DIGIT-DRIVER OPERATION

The sense-amplifier and digit-driver interconnections to a sense-digit line are shown in Fig. 12. (Because the digit driver is only a voltage switch, its operation is simple and is not discussed here.) The sense amplifier is designed to detect usable signals of 30 millivolts and to recover from digit transients (which occur during the turn-on and turn-off of the digit driver) of several volts in about 30 nanoseconds. (This sense amplifier was developed by EDP Advanced Development, Pennsauken, N.J.)

The sense amplifier shown in Fig. 12 is of a differential type for common-mode rejection of noise in a two-core-per-bit sense output. The sense-winding inputs are connected so that when a *1* is read out of the memory, terminal 2 becomes more positive than terminal 1. Transistors Q_1 and Q_2 are used in the differential preamplifier circuit, Q_4 in a strobe gate, and Q_5 and D_1 (a tunnel diode) is the output "comparator" or pulse stretching circuit.

When a *1* is read out, Q_1 tends to conduct more and Q_2 to conduct less, (Q_1 and Q_2 are normally not saturated). More base drive is then supplied to Q_3. The collector current of Q_3 (also not saturated) flows through Q_4. Because diode D_1 is back-biased, there is no output. When the strobe command is applied, however, Q_4 is turned off and the current from Q_2 flows into the low impedance of forward-biased D_1 and switches it. The output transistor is thus driven to saturation for the duration of the strobe command.

When a *0* is read out, Q_2 tends to conduct more and Q_1 conducts less and the base drive of Q_3 is reduced. Because the collector current of Q_3 remains below the peak current of tunnel diode D_1, no output is possible.

The resistor-capacitor-diode network in the emitter circuit of Q_3 is designed to prevent false triggering of the output as a result of the reception of large digit noise.

SYSTEM TEST WAVEFORMS

The waveforms shown in Fig. 13 to 15 were obtained with a read-write cycle time of 400 nsec. The raw sense output of Fig. 13 shows a composite of *1*'s and *0*'s on a typical sense line; the digit and write transient recovery is accomplished within 350 nsec. Fig. 14 shows the strobed output of the sense amplifier for a pattern of all *1*'s and *0*'s. The read-write and digit currents are shown in Fig. 15.

CONCLUSIONS

The fabrication and operation of this ultra-high-speed memory system have been extremely successful. The system has been operated without errors at a cycle time of 375 nsec with read-drive currents of approximately 300 ma.

Investigations have shown that future basic memory module sizes of 500 to 1,000 words with 60 bits per word are feasible. The higher ratio of the sense-digit line delay to the cycle time for these larger modules will require a more complex timing program, and the sense-digit line terminations will require careful consideration.

As mentioned previously, the ferrite devices offer several advantages over other competing materials and devices. An important consideration in this program has been the core and bit uniformity. The ferrite cores that have been developed have shown excellent uniformity characteristics on two-core-per-bit operation. The high outputs (50 mv) and low current levels required for systems operation are another important factor.

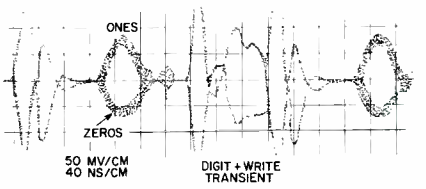


Fig. 13—Differential raw sense output of a bit. Composite *1* and *0* of 128 words are shown.

ACKNOWLEDGMENT

The author acknowledges the assistance in this project of J. Fung, R. Hogan, B. LeBlanc, J. Rodriguez, and U. Strasilla.

The helpful suggestions of Dr. H. P. Lemaire, P. D. Lawrence, and B. Frackiewicz in the applications of the microferrite device; and the help of E. Small for the mechanical packaging.

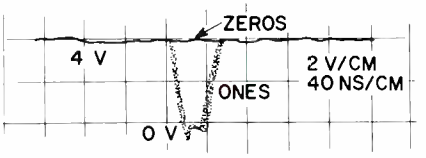


Fig. 14—Strobed output of sense amplifier.

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Fig. 12—Sense-amplifier and digit-driver layout.

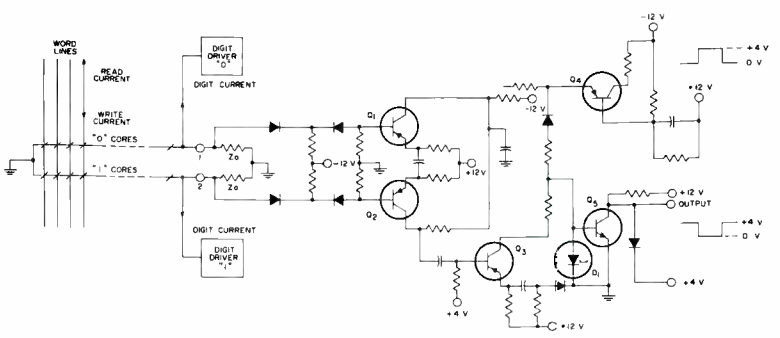
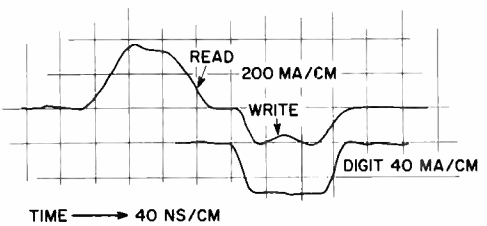


Fig. 15—Read, write, and digit currents.



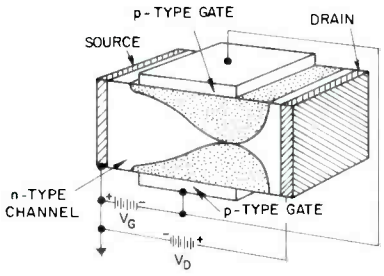


Fig. 1—Junction unipolar transistor structure.

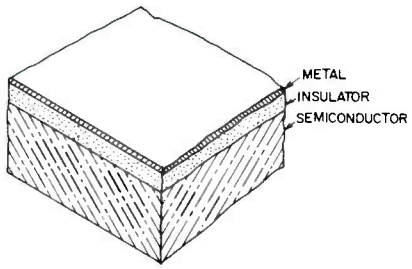


Fig. 2—Metal-insulator-semiconductor structure.

R. Vanozzi, RCA Laboratories, observes the electrical characteristics of a completely fabricated MOS transistor.

Fig. 3—Energy band diagram for metal-insulator-semiconductor contact.

THE MOS (INSULATED-GATE) FIELD-EFFECT TRANSISTOR

As originally proposed by Shockley[1], the unipolar field-effect transistor utilized the depletion region of a reverse biased p-n junction to control the cross-section, and hence the conductance, of a bar of semiconductor material (Fig. 1). The theoretical characteristics of this device were derived by Shockley[1] and others[2] and have since been experimentally confirmed. The device discussed in this paper represents a significant departure from the Shockley unit in that the reverse biased p-n junction has been superseded by the metal-insulator-semiconductor structure shown in Fig. 2. This structure can be used to enhance as well as deplete the charge near the surface of the semiconductor. The result is a new device[8] possessing a significantly increased versatility, a considerably simplified fabrication process, and a great promise for integrated-circuit applications—the metal-oxide-semiconductor (MOS) transistor.

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DURING THE EARLY YEARS in the development of semiconductor physics, consideration was given to the concept of using an external electric field normal to the surface of a semiconductor to control the carrier density near the surface. In 1948, Shockley and Pearson reported their results of field-effect measurements on n-type germanium in a letter to the *Physical Review*.[3] They placed a thin insulating strip between the semiconductor and an evaporated metal film, forming a parallel plate capacitor. The change in conductance of the semiconductor was measured as a function of the applied voltage across the capacitor. Since the excess or depletion of charge in the germanium can be calculated from the voltage and capacitance values, a corresponding change in the conductance should be observed. The results of this experiment showed that only 10 percent of the excess charge placed in the germanium contributed to the current. The rest was postulated to reside in bound states on the surface of the semiconductor.

Fig. 3 shows the energy band diagram for the metal-insulator-semiconductor structure, ignoring the effects of surface states and the difference in contact potential between the metal and semiconductor. A negative bias applied to the metal would tend to raise the energy bands in the semiconductor and deplete it of conduction electrons; a positive bias would tend to lower the bands and enhance the number of electrons in the semiconductor. If surface states are present, however, excess charge drawn into the semiconductor may reside in these bound states and not contribute to the current in the semiconductor.

From a qualitative viewpoint, the presence of these surface states may be understood by considering the atomic structure of a vacuum to diamond-type semiconductor (e.g. silicon, germanium) interface. The covalent type bond structure is illustrated in Fig. 4. The surface layer contains one bond per atom which is not shared by another atom; this bond is capable of accepting and holding an electron to satisfy its atomic structure.[4] From this "dangling bond" description, one would expect a surface state density

of electron acceptors equal to the number of atoms in an atomic monolayer ($1.37 \times 10^{15}/cm^2$ for silicon).

This picture, however, is considerably oversimplified. It has been experimentally observed that surface states (both acceptor and donor types) are distributed in energy throughout the forbidden gap and are characterized by a delay in response, or time constant.[5] Furthermore, these states are highly dependent upon surface conditions including the effects of adsorbed gases, surface strains, mechanical damage, etc.

It has been reported in the literature recently[1,5] that silicon dioxide thermally grown on the surface of a silicon wafer has the property of passivating the surface, or greatly reducing the density of surface states. It is this fact that motivated the work described in this paper.

THEORY OF OPERATION

A transistor possessing a metal-oxide-semiconductor control structure is illustrated in Fig. 5. In this unit, the intrinsic bulk material acts as a passive substrate; the active channel is a thin layer in the surface of the silicon under the thermally grown silicon dioxide. Consider first a transistor fabricated with the channel of the same conductivity type as the source and drain contacts; this may be operated in either the depletion or enhancement modes.

Depletion Mode: To operate in this mode, the gate is reverse biased so that carriers are depleted from the channel. Therefore, maximum drain current flows in this mode of operation for zero gate bias. This is analogous to the operation of the Shockley unit.

Enhancement Mode: Here, the gate is forward biased so that carriers are drawn into the channel; minimum drain current flows in this mode of operation for zero gate bias. In contrast to the Shockley p-n junction type unit, no gate current flows due to the insulating silicon dioxide layer.

Due to the continuity of the transfer characteristic from reverse bias to forward bias, operation at zero bias is possible. This yields considerable simplification in circuitry for many applications. A typical set of drain characteristics is shown in Fig. 6 indicating the different modes of operation.

Induced Channel Mode: This unit is fabricated with the channel and source-drain contacts of opposite conductivity type.[6] Back-to-back diodes are formed between source and drain contacts and the drain current is essentially zero for zero gate bias. To simplify the following discussion, a p-type channel with n-type source-drain contacts will be assumed. If a positive voltage is applied to the gate the energy bands will be bent in such a manner that holes are repelled from the channel and electrons drawn in. Hence, as the voltage is increased, the channel goes from p-type, through intrinsic, to n-type, at which point ohmic conduction from source to drain commences. Enhancement mode operation is obtained for a further increase in gate bias.

The utility of the induced channel unit lies particularly in the area of logical switching circuits, since the output voltage of the transistor is of the correct polarity to make direct coupled transistor logic feasible, without shifting voltage levels between stages.

EXPERIMENTAL RESULTS

It has been observed experimentally that

STEVEN R. HOFSTEIN graduated from the Cooper Union for the Advancement of Science and Art with a B.S.E.E. in 1959, and joined RCA Laboratories in the same year. While at the Laboratories he continued his studies at Princeton University under the RCA Graduate Study Program, receiving the MSEE degree in 1961. Awarded a David Sarnoff Fellowship for the academic year 1961-62, he continued his studies toward the Doctorate at Princeton full time, completing his course requirements in May 1962. He expects to receive the Ph.D. in 1963. In 1959-60, he proposed and analyzed several new field-effect transistor structures and related semiconductor devices. In 1960, he initiated work on the insulated-gate field-effect transistor, and in collaboration with F. P. Heiman, completed fabrication of these units in 1961. Mr. Hofstein is a member of Tau Beta Pi and the IEEE.

FREDERIC P. HEIMAN graduated from the City College of New York in 1960 with a BSEE. He joined RCA Laboratories that year under the Graduate Study Program, receiving the M.S.E. degree in June 1962. He is presently on leave of absence from the Laboratories completing the course requirements for the Ph.D. degree at Princeton under a David Sarnoff Fellowship. While on the Research Training Program, Mr. Heiman worked on high-speed tunnel-diode counting circuits and on an experimental null-zone detection system. With S. R. Hofstein, he helped develop the insulated gate field-effect transistor. Mr. Heiman is a member of Eta Kappa Nu and the IEEE.

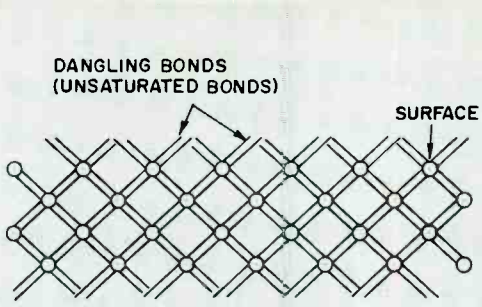

Fig. 4—Atomic diagram of diamond-type structure surface.

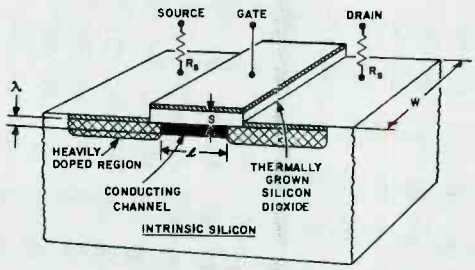

Fig. 5—MOS transistor structure: N = channel density; λ = channel depth; S = oxide thickness; μ = carrier mobility; l = channel length; R_s = parasitic series resistance; ε_{ox} = relative dielectric constant of oxide; W = channel width.

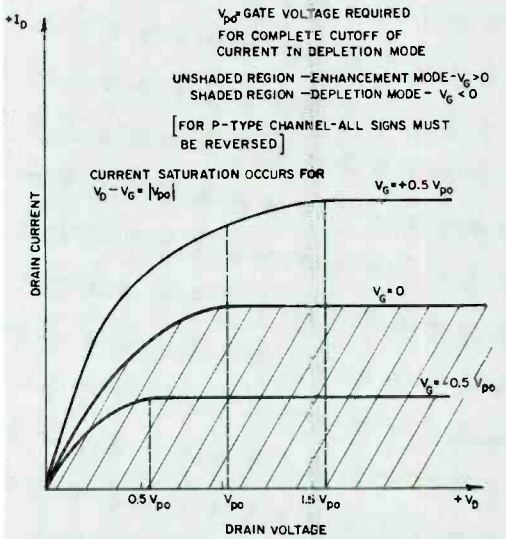

Fig. 6—Characteristic curves for N-type channel MOS transistor.

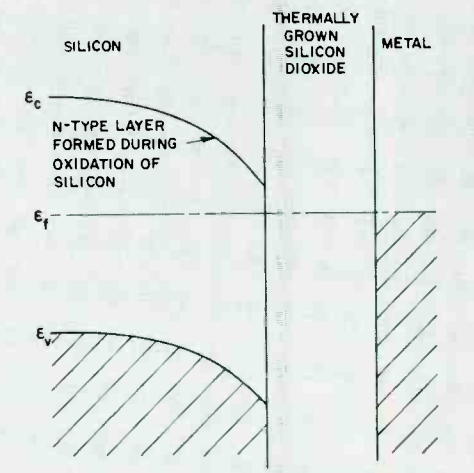

Fig. 7—Energy band diagram of MOS contact with thermally grown silicon dioxide insulator.

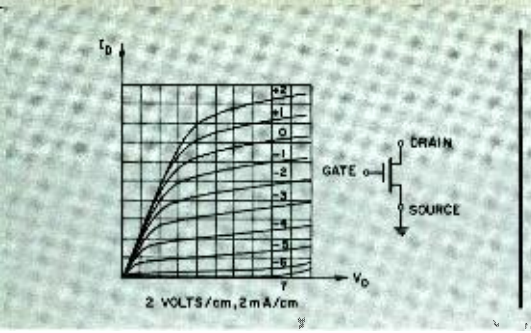

Fig. 8—Drain characteristics, experimental transistor.

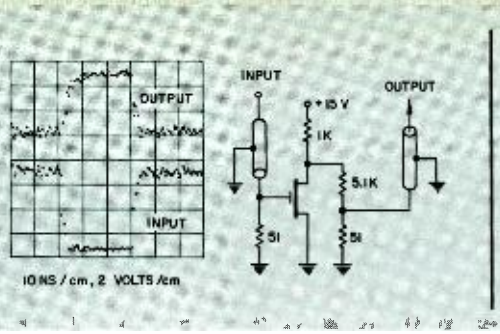

Fig. 9—Pulse response of transistor.

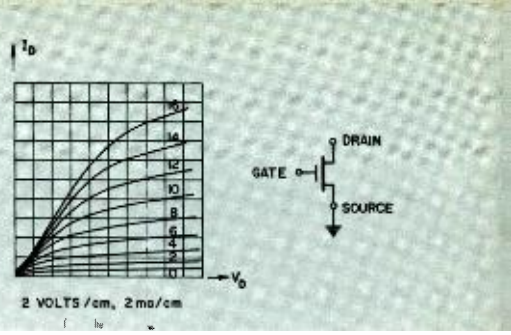

Fig. 10—Drain characteristics, enhancement transistor.

thermally grown silicon dioxide not only passivates the silicon surface but also produces a thin n-type skin on the surface of intrinsic silicon. The energy band diagram for a metal-oxide-semiconductor structure employing this surface inversion layer is shown in Fig. 7. The characteristic curves of a field-effect transistor which was fabricated with a channel derived from the oxide growth is illustrated in Fig. 8; both depletion and enhancement modes are displayed. Similar transistors have been fabricated with transconductances in the range of 2000 to 5000 micromhos; all have an input capacitance of 7 pf. Time constant measurements indicate an input leakage resistance of 10^{14} to 10^{16} ohms, confirming the excellent dielectric properties of thermally grown silicon dioxide.

Using a mercury relay pulser and sampling oscilloscope, the pulse response of this unit was measured. The circuit used, and waveforms obtained, are shown in Fig. 9; a rise time (10 to 90 percent) of 10 nsec is indicated. No storage or transit delays appear to be present and an improvement in geometry and dimensions should yield a corresponding improvement in response time. The zero-bias drain current is a function of the doping in the region under the oxide. For a unit which is to be operated entirely in the enhancement mode, the thermally created n-type inversion layer is undesirable and should be removed. Fig. 10 is a photograph of the drain characteristics of a transistor with the inversion layer removed; it operates entirely in the enhancement mode, i.e. minimum drain current for zero gate bias.

Since the original motivation for this work was the feasibility of integrating large arrays of these devices. the most recent structure fabricated was a "ladder-like" one of devices having a smaller channel width, in which the source of one unit is the drain of the adjacent unit; the interconnection of many devices is greatly facilitated with this geometry. Fig. 11 is a photomicrograph showing the layout of an array of completely fabricated transistors. The packing density is 2200 units per square inch.

Fig. 11—Geometry of a ladder-like structure.

TRANSISTOR DESIGN PARAMETERS

Excellent agreement has been obtained between theoretically predicted characteristics and those measured on experimental units.[7] The purpose of this section is to summarize the results of these calculations in such a manner as to permit the design of a transistor conforming to predetermined specifications. The transconductance for zero gate bias gm_o, total input capacitance C_o, pinch-off voltage V_{po}, and channel resistance for zero gate bias R_o are the parameters chosen to evaluate the transistor. Dimensions and symbols refer to Fig. 12.

$$R_o = \frac{1}{\mu q \omega (N\lambda)}$$

$$gm_o = \left(\frac{2}{R_o}\right)\frac{1}{1+K+\sqrt{1+K}}; \quad K \equiv \frac{2R_s}{R_o}$$

$$V_{po} = -q\frac{(N\lambda)S}{\varepsilon_{ox}} \qquad C_o = \frac{\varepsilon_{ox} l \omega}{S}$$

An increase in oxide thickness S increases the pinch-off voltage and decreases the input capacitance, but leaves the zero-bias transconductance unmodified. The thicker oxide unit operates at a higher power level, but has a faster response because of the smaller input capacitance. The quantity $N\lambda$ represents the total number of free carriers per unit surface area present in the channel with the gate at zero bias. Thus, the above equations do not apply to the induced channel unit.

CONCLUSIONS

Use of the insulated control electrode on the field-effect transistor structure yields several important advantages over its p-n junction predecessor. They are:

1) Transistors may be fabricated in which the mechanism of control is either depletion of channel charge, enhancement of channel charge, or a combination of both, thus providing greater freedom in circuit design.
2) The continuous characteristic from the negative gate bias region to the positive bias region allows operation at zero bias.
3) The oxide thickness provides a new design parameter; the thicker oxide units operate at higher speed and power level.
4) Gate leakage current is extremely low; time constant measurements yield an input resistance of 10^{14} to 10^{16} ohms.
5) The planar construction of these zero junction devices coupled with their highly uniform characteristics have yielded great promise for integrated circuit applications.

ACKNOWLEDGMENTS

The authors would like to acknowledge the able assistance of R. R. Vannozzi in fabricating these devices and alleviating many of the practical difficulties encountered. The information obtained from J. Olmstead and J. Scott of the RCA Semiconductor and Materials Division, Somerville, on the diffusion and cleaning procedures was essential to the realization of this transistor. Many important points were brought to light in the stimulating discussions with T. O. Stanley, and we would also like to thank J. T. Wallmark, K. H. Zaininger, M. E. Sekely, A. Rose, H. S. Sommers, Jr., L. Pensak and J. McCusker for their helpful comments. J. Briggs is responsible for the delicate job of dicing the wafers and G. Lang did the chemical polishing.

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7. F. R. Heiman and S. R. Hofstein, *paper to be published.*
8. The device described herein was announced in an *Engineering and Research Note*, RCA Engineer, Oct.-Nov. 1962.

FERROELECTRIC DECODING AND ADDRESSING FOR SOLID-STATE DISPLAYS

Decoding and addressing circuits associated with solid-state status-display systems are complex and costly, requiring numerous operational gates, decoders and addressing circuits for proper code translation. This paper describes ferroelectric circuits for economically performing such decoding and addressing operations for electroluminescent display modules.

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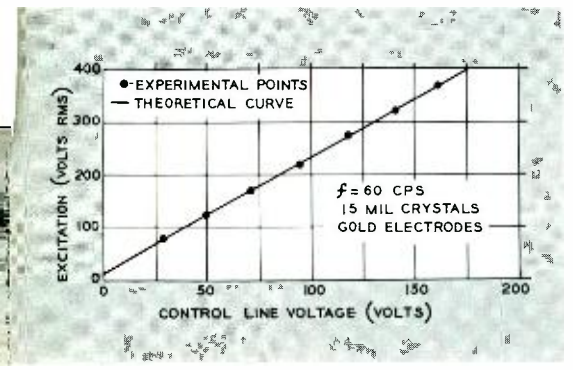
A PRIMARY PROBLEM encountered in the use of electroluminescent modules for status displays is the complexity and cost of associated data processing or display decoder equipment. In readout devices, such as those previously described by L. E. Haining,[1] the primary decoding function to be performed involves the selection of proper EL segments to form the desired pattern or character designated by an input code from a computer or buffer. Decoder input is in the form of binary voltage levels and the output must control the application of relatively high-voltage AC (say 250 volts-rms, 420 cps) to the EL display segments.

SMALL, INEXPENSIVE DECODING AND ADDRESSING CIRCUITS NEEDED

For a 35-segment alphanumeric readout module, about 1200 operational gates are required in the decoder to translate from a six-bit input code to the designation of the required segment arrangements to form the characters. Since it is desirable to have a decoder associated with each display module (actually, the decoder should be an integral portion of the module), these decoders must be small and inexpensive.

The most popular approach to date has been the use of photoconductive-electroluminescent control elements.[1,2] Although this approach provides an attractive solution to the decoding problem, its limitations include the need for an auxiliary interface between the decoding circuitry and the addressing input (since high-voltage AC must excite the input EL strips) and the slow speed of operation of available photoconductor elements.

Fig. 2—Control voltage required for cutoff.



Recently developed ferroelectric decoding circuits offer advantages in these two areas. Direct DC voltage addressing is used eliminating the requirement for an auxiliary input interface and the speed is faster by a factor of 5 or 10 than typical photoconductive circuits. Also, the decoder output is an AC voltage, allowing a direct coupling with the EL display segments. The logic circuits are relatively simple, have a high packing-density, use ultimately inexpensive materials, and allow completely solid-state construction.

FERROELECTRIC OPERATION

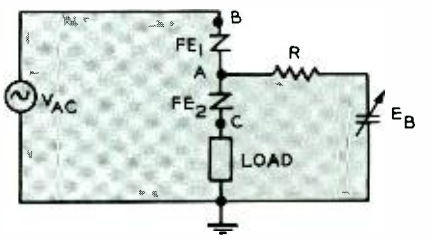
Ferroelectrics are materials which exhibit a reversible spontaneous electrical polarization. The ferroelectric circuit element takes the form of a capacitor with the ferroelectric material as the dielectric between the capacitor plates. When monocrystalline ferroelectrics are used, the capacitor is formed by painting and depositing conductive electrodes on opposite sides of a slab of the material. If a curve of charge through such a capacitor is plotted versus voltage applied, it resembles the familiar *B-H* hysteresis loop of a ferromagnetic material; hence the term "ferro"electric.

A number of theories have been offered to explain the intricate physical relations which account for this polarization characteristic. It is not the purpose of this paper to become concerned with the physics involved; rather, the ferroelectric capacitor will be viewed as a circuit element to be used in decoding applications.

FERROELECTRIC GATING CIRCUITS

Probably the most useful ferroelectric arrangement for display decoding is an extension of a basic two-crystal gate configuration.[3,4] This configuration makes use of the property that two ferroelectric capacitors in series appear to an AC excitation as a low impedance when the capacitors are polarized in like directions and appear as a high impedance when the ferroelectric elements (FE) are charged in opposite directions.

Fig. 1—Voltage-control operation of a two-crystal gate.



When the two series ferroelectrics (Fig. 1) are polarized in the same direction, the polarization of each will be reversed on each half-cycle of the AC excitation and this polarization reversal charge passes through the load element. The FE pair thus acts as a low impedance which allows the conduction of charge through the load. If, however, the FE capacitors are polarized oppositely, one is always saturated in the direction of the instantaneous applied voltage. This FE appears as a high impedance and prevents charge flow through the other FE and the load. Thus, practically the entire excitation voltage appears across FE_1 on one half-cycle of the excitation and across FE_2 on the opposite half-cycle.

This basic circuit is shown in Fig. 1 with the load (an EL segment) located between FE_2 and ground. The load could be placed between FE_1 and the AC excitation source, but in this case current drawn through the isolation resistor R when the gate is cut off will pass through the EL. In more complex decoding circuits, this leakage current may prevent as complete a cutoff of the EL as might be desired.

Control of the relative polarization of the two capacitors is accomplished by the application of a DC bias through an isolation resistance to the point of connection of the two ferroelectric capacitors. If the control voltage, E_B, is at ground potential, the ferroelectric elements will assume like polarizations and the gate will be in the conducting state. If, however, E_B is made sufficiently positive, the required AC steady-state conditions in the circuit make it impossible for the voltage at Point A in Fig. 1 to become negative enough to reverse the polarization of FE_2. This keeps the ferro-

electrics oppositely polarized and the circuit is in the high impedance or blocked state. Any control voltage between zero and the minimum required for cutoff will hold the gate in a partially conducting or intermediate impedance state.

The required control voltage is independent of the excitation frequency and has only a small dependence on the size, quality, and specific characteristics of the ferroelectric elements. Fig. 2 shows the correlation of theoretical and experimental results for a gate circuit using[5] ferroelectric capacitors of monocrystalline triglycine sulfate (TGS).

When the ferroelectric gate is switched from the conducting to nonconducting state or vice versa, enough external charge must be provided to the connection point of the FE crystal pair to completely reverse the polarization states. The time for complete switching is the time required to inject or remove this polarization reversal charge and is dependent on the control voltage, the control line resistance, the polarization reversal charge of the FE elements, and the amplitude of the AC excitation. (Mathematical relations for the control voltage required for cutoff and for the turn-on and turn-off times are developed in Reference 6.)

DECODING CHAINS

The basic principles of operation of the two-crystal ferroelectric gate may be utilized in developing ferroelectric configurations to perform logical operations. For notational convenience, the following symbology will be used:

1) A, B, etc., represent zero voltage level for logical *1* and some cutoff voltage level for logical *0*.
2) $\overline{A}$, $\overline{B}$, etc., represent some cutoff voltage level for logical *1* and zero voltage level for logical *0*.
3) *0* represents conduction of charge through the load.
4) + represents *or*.
5) • represents *and*.

If an additional series FE crystal and a second control line are added to the two-crystal gate, as shown in Fig. 3, the circuit will perform an *and* operation on the A and B inputs. If either input is at a DC level greater than the minimum required for cutoff, the two FE crystals adjacent to that control line will appear as a high impedance on alternate half-cycles and the gate will block. Conduction to the load occurs only if V_A and V_B are both below the cutoff potential. (For full conduction both should be at ground potential.) This corresponds to the logical operation $O = A \cdot B$. This type

H. T. GNUSE received the BSEE, summa cum laude, at Duke University in 1960. Upon graduation he received a commission in the United States Air Force. He joined RCA on the Graduate Study Program in 1960 and received the MSE degree at UCLA in June 1962. His graduate work was in the area of information systems and electronics, and his master's research and thesis were on "Ferroelectric Switching Circuitry." While at RCA he worked in the data handling and display area, his most recent work being in solid state displays. In July 1962, Mr. Gnuse began a three-year leave of absence from RCA for an active duty tour with the Aeronautical Systems Division of the Air Force Systems Command. He is a member of the IRE, Phi Beta Kappa, Eta Kappa Nu, and Tau Beta Pi and an associate member of the AIEE.

of series chain of *and* gates can be extended to allow a great number of inputs, the limit occurring when the equivalent impedance representing the FE crystals and the isolation resistors is such as to prevent sufficient voltage transfer to the load elements.

Parallel groupings of two-crystal gates perform *or* operations on the inputs. Referring to Fig. 4, if either input is at zero potential, conduction to the load will occur, but if both V_A and V_B are above cutoff, neither path can conduct charge to the load. The logical operation represented is $O = A + B$. The limit on the number of permissible parallel gates is determined by the natural capacitance of the ferroelectrics.

Extension of this technique to combinations of *and* and *or* operations is obvious. The circuit configuration of Fig. 5 has the following logical properties:

$$O = A \cdot B \cdot C + \overline{A} \cdot \overline{B} \cdot C$$

This of course represents the fact that conduction to the load will occur if any one complete chain connecting the AC excitation and the load is not blocked.

ELECTROLUMINESCENT LOADS FOR FE DECODERS

When the output load for an FE gate is an electroluminescent segment, the EL brightness will be a maximum when the control voltage is zero, corresponding to complete conduction in the gate. As the gate bias is increased, the brightness decreases since a larger percentage of the input excitation appears across the FE elements. For a gate circuit using a standard commercial RCA yellow EL plate and monocrystalline TGS ferroelectrics, the brightness vs. control voltage relation is as shown in Fig. 6. Below an EL-to-FE area ratio A_R of about 40 the brightness characteristics have little dependence on the area ratio.

For larger area ratios, the ferroelectrics saturate before the peak excitation voltage can be delivered to the EL, thus causing a lower output brightness for the completely conducting state. Fig. 6 shows that the EL brightness is below 0.005 foot-lamberts at cutoff (110 volts for the 250 volt-rms excitation) and is about 10 foot-lamberts at zero control voltage if proper area match is achieved. This represents an *on-off* contrast ratio for the single gate in the order of 2000:1.

Fig. 3—Basic AND gate circuit.

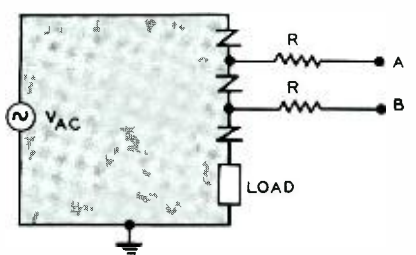
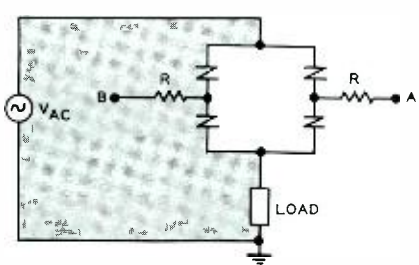


Fig. 4—Basic OR gate circuit.



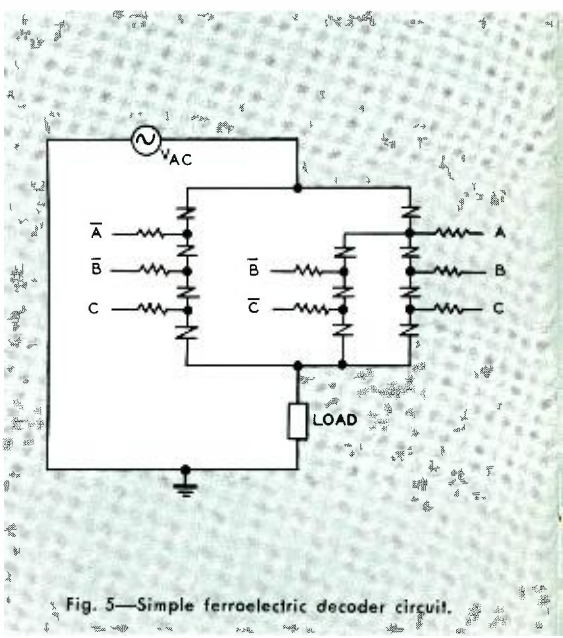


Fig. 5—Simple ferroelectric decoder circuit.

DISPLAY DECODER CIRCUIT

Various circuits were constructed utilizing ferroelectrics as simple switches and in decoding chains to demonstrate the feasibility of moderately complex configurations. The most conclusive demonstration of the feasibility of ferroelectric circuits for display decoding and direct addressing of EL segments was the successful operation of the six-bit decoder shown in Fig. 7. The decoding operation which this unit performs is that required for one of the segments in a 38-segment alphanumeric readout panel.

In operation, a computer-type parallel output of six bits indicates the character to be displayed by the readout. Each segment of the display panel has a decoding section such as that in Fig. 7 associated with it to cause the segment to light on the proper code designations. With 250-volt-rms excitation, the brightness of illuminated output segments was 3.2 foot-lamberts. With a control voltage of 125 volts, on typical codes for which the output was not to be excited, brightness of the EL was about 0.007 foot-lamberts. This represents a contrast ratio of nearly 500, which is encouraging in view of the large number of parallel paths and the length of the series paths in the decoder.

The 125-volt value of control voltage is, of course higher than would be desired if the source were to be from transistor circuitry. Work in progress at the RCA Laboratories in Princeton, and at the Electron Tube Division in Lancaster, Pa., indicates a good probability of development of efficient phosphors to operate at a much lower voltage than the 250 used here. If EL which operates efficiently at 50 volts-rms, for example, becomes available, control by small transistors will be very convenient.

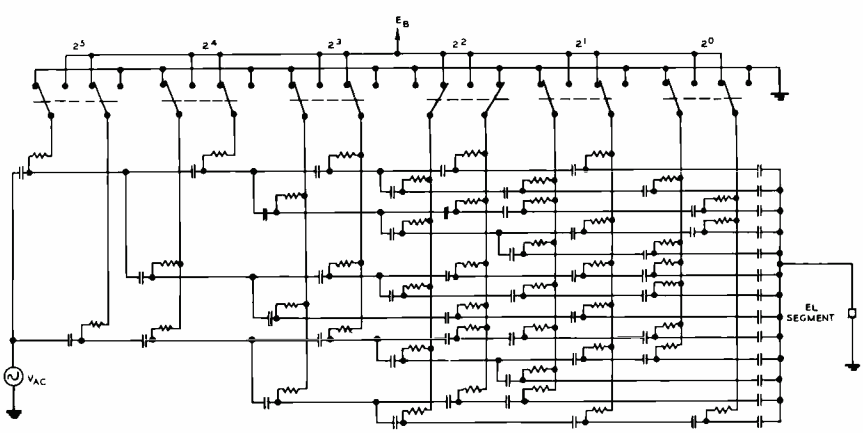
In order to obtain good voltage transfer to the load in the preceeding circuit, some restriction must be placed on the minimum allowable isolation resistance. Since the switching time is linearly dependent on the resistance of the control line, this also restricts the minimum switching speed which may be obtained in a practical design. For circuits of the complexity of the six-bit decoder, the minimum switching time is in the order of 10 msec. The voltage delivered to the load element in the conducting state was about 65 percent of the excitation voltage for this design.

In the circuitry tested here, the FE elements used were one or a few gates on a single crystal, and enclosed in a tube envelope for protection against atmospheric moisture. For use in practical circuits it is anticipated that the ferroelectric material could be grown in thin slabs so that a great number of FE capacitors could be formed on a single sheet by vacuum depositing proper electrode arrangements. This would allow a very high packing density of gates since each FE element might have a thickness of as little as 0.02 cm and an electrode area of only 0.02 sq cm. If printed resistors are used, complete integrated circuits should be possible with vacuum deposition and printed wiring of the circuitry involved indicates that the development of production techniques would result in decoding modules of relatively low cost.

CONCLUSIONS

The work described has demonstrated the feasibility of using ferroelectric circuits to perform decoding operations. The good impedance match of FE and EL elements and the AC voltage output of FE circuits make this approach useful as a combined decoding and addressing technique for solid-state display modules. The simplicity of the circuitry involved indicates that the development of production techniques would result in decoding modules of relatively low cost.

Fig. 7—A six-bit ferroelectric decoder to address one segment of a 35-element EL alphanumeric readout.



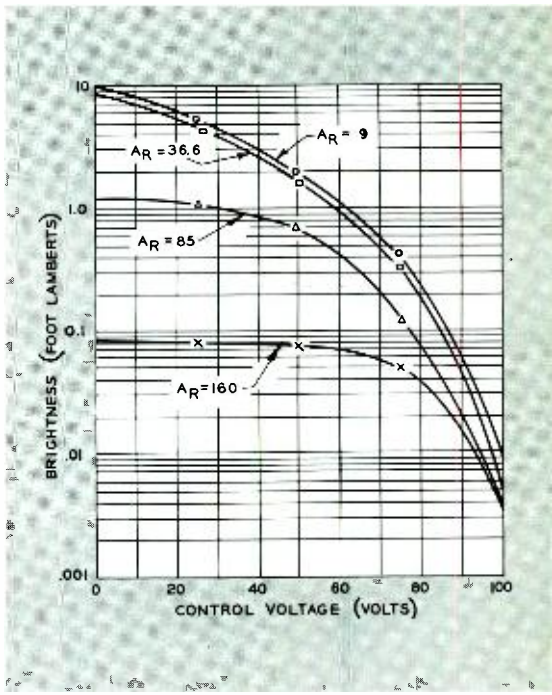


Fig. 6—Output brightness versus control-voltage charcteristics for a two-crystal FE gate with an EL load.

ACKNOWLEDGEMENT

The author is indebted to Dr. W. J. Merz of Zurich, and Dr. G. J. Goldsmith of the RCA Laboratories for high quality ferroelectrics used to begin the work, to G. S. Gadbois of the Tube Division at Lancaster, Pa., for the crystals sealed in tube envelopes which were used for the actual circuitry which was built and tested, and L. M. Seeberger for guidance of the program. Special thanks are due to L. E. Haining for his many suggestions and contributions throughout the investigation.

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Engineering and Research NOTES

BRIEF TECHNICAL PAPERS OF CURRENT INTEREST

A Geometrical Method to Investigate Dispersion Relations

by RYOGO HIROTA AND SOITIRO TOSIMA, *Laboratories RCA, Inc., Tokyo, Japan*

This geometrical method for solving dispersion relations is based on the analog between the dispersion relation and potential theory in a complex ω (frequency) plane. Physical quantities, such as plasma frequencies, drift and thermal velocities, relaxation times, etc., which are contained in the dispersion relation can be interpreted as electrical quantities—such as charges, dipole moments, and their positions in the complex plane. The well-known problem of an electron beam passing through a plasma is used to illustrate an application of the method.

An analog between complex potentials in the electrostatic theory (or in the hydrodynamics) and dispersion relations was established.

Consider a dispersion relation of the form:

$$D(\omega,\vec{k}) = C(\vec{k}) \tag{1}$$

where ω is a frequency, $\vec{k}$ a wave vector, $D(\omega, \vec{k})$ is assumed to be an analytical function of ω, and $C(\vec{k})$ a function of $\vec{k}$, independent of ω. The solution of Eq. 1 for a given $\vec{k}$ determines the character of the waves under investigation.

We have found that a potential analog of the dispersion equation was very helpful to find the solutions of Eq. 1. This analog has the following advantages: 1) Both of the real part and the imaginary part of ω can be found graphically using simple physical concepts such as an electric field, a charge distribution, a conductive wall, etc. in two-dimensional space; and 2) when the dispersion relation does not have a simple form, the method of the conformal mapping can be applied to solve the dispersion relation.

A complex potential $W(\omega)$ in two dimensional space (x, y) is given by:

$$W(\omega) = V(\omega) + iU(\omega) \qquad \omega = x + iy \tag{2}$$

Where: $V(\omega)$ is an electric potential (or a velocity potential) and $U(\omega)$ is a stream function. Since $W(\omega)$ is an analytical function of ω, we have the Cauchy-Riemann relation:

$$\frac{\partial U}{\partial x} = \frac{\partial V}{\partial y} = E_y \qquad \frac{\partial U}{\partial y} = \frac{\partial V}{\partial x} = -E_x \tag{3}$$

where E_x and E_y are the electric field (or the velocity) along the x and y axis, respectively. Then, a derivative of $-W$ with respect to ω becomes:

$$-\frac{dW}{d\omega} = -\frac{\partial W}{\partial x} = E_x - iE_y \tag{4}$$

Returning to the dispersion relation, we compare Eq. 1 and Eq. 4 to get:

$$D(\omega,\vec{k}) = -\frac{dW(\omega,\vec{k})}{d\omega}$$

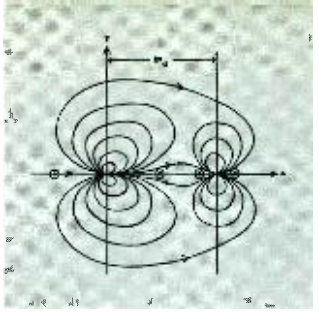

Fig. 1—Field distribution, ω plane, (arbitrary scale) for $\omega_{p1} > \omega_{p2} > 0$, and $\omega_{p1} < kv_d$.

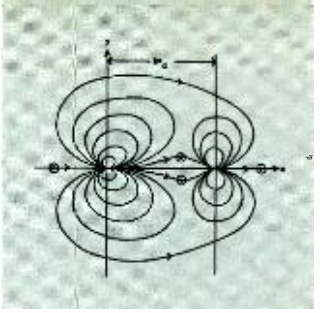

Fig. 2—Same as Fig. 1, but $\omega_{p1} > kv_d$.

Or:

$$W(\omega,\vec{k}) = -\int^{\omega} D(\omega,\vec{k})d\omega \tag{5}$$

And:

$$C(\vec{k}) = E_x(\vec{k}) - iE_y(\vec{k}) \tag{6}$$

Eq. 5 shows that the function $D(\omega, \vec{k})$ can be considered as the electric field (or the velocity) in the $\omega(x, y)$ plane. Hence, Eq. 1 can be interpreted as the problem of finding the positions with the given electric field (or the velocity) $E = C(\vec{k})$ where the field distribution $E(\omega)$ is given by $D(\omega, \vec{k})$.

As an illustration, the dispersion relation in the well-known case of the interaction between an electron beam and a plasma is:

$$\frac{\omega_{p1}^2}{\omega^2} + \frac{\omega_{p2}^2}{(\omega - kv_d)^2} = 1 \tag{7}$$

Where: ω_{p1} and ω_{p2} are the plasma frequencies of the thermal plasma and the electron beam, respectively, and v_d is the drift velocity of injected electrons. We have:

$$W(\omega) = -\int^{\omega}\left(\frac{\omega_{p1}^2}{\omega^2} + \frac{\omega_{p2}^2}{(\omega - kv_d)^2}\right) d\omega$$

Or:

$$W(\omega) = \frac{\omega_{p1}^2}{\omega} + \frac{\omega_{p2}^2}{\omega - kv_d} \tag{8}$$

Therefore, the field distribution in ω plane is given by two dipole moments of ω'_{p1} and ω'_{p2} located at $\omega = 0$ and at $\omega = kv_d$, respectively. This is shown in Figs. 1 and 2, where the positions where $E_x = 1$ and $E_y = 0$ are marked by $\odot$. From Figs. 1 and 2, we can immediately conclude that the frequency $Re\omega$ of the unstable wave, if it exists, is smaller than kv_d and that the instability can occur if the electric field E_x, on the real axis within $0 \leq Re\omega \leq kv_d$, is everywhere greater than unity. This is the well-known case[1] when

$$0 < kv_d < \left(\omega_{p1}^{\frac{2}{3}} + \omega_{p2}^{\frac{2}{3}}\right)^{3/2}$$

Applications of this method to other related problems are in progress.

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A New GaAs Laser That Can Be Pumped Electrically

by DR. J. I. PANKOVE, *RCA Laboratories, Princeton, N.J.*

In the conventional solid-state laser, light is used as the source of input power, i.e., the pump. In October 1962, workers at RCA Laboratories succeeded in achieving a semiconductor laser that is pumped by an electrical current and can probably be modulated at gigacycle rates by modulating this input current.

The new laser emits light at a wavelength of 8400 angstroms. The device is very simple, comprising only a p-n junction diode in a wafer of gallium arsenide. A similar diode was used here several years ago to generate a beam of ordinary incoherent light that was modulated with an audio signal. More recently, the incoherent light from the diode was modulated at 200 Mc.

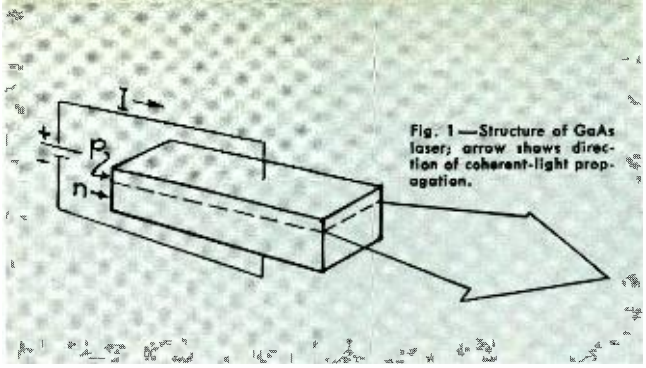


Fig. 1—Structure of GaAs laser; arrow shows direction of coherent-light propagation.

The gallium arsenide diode was converted into a laser by 1) altering its shape, 2) by decreasing the contact resistance to reduce the losses, and 3) by increasing the current density through the junction. A typical diode laser consists of a rectangular bar of gallium arsenide 5 mils high, 5 mils wide, and 20 mils long, with a 5-by-20-mil junction about a mil below the top surface (Fig. 1).

When the diode is cooled to 1.9°K by evaporating liquid helium, a low pulsed current causes the emission of incoherent light in all directions. However, when the pulse current is increased to about 2 amperes, the light waves in the direction of the long dimension of the junction become so intense that the emission from the recombination of electrons and holes is stimulated to occur in phase with the light waves. The light is then emitted from the end of the junction and, as in other lasers, the light is coherent because all of the emitted light waves are in phase.

At present, the diodes are pulsed with thirteen $\frac{1}{100}$-second pulses per second. They have been pulse-operated with lower duty cycles at temperatures as high as 77°K. During the pulses, even the small diodes described generate 3 watts of light, more than half of which goes into the coherent beam. Further improvement and instructive reduction in contact resistance is expected to permit CW operation.

The next step will be to increase the diode area. A 1000-fold increase in the present area, giving 1000 times the light output, should offer no fundamental fabrication problems and no serious cooling problems other than the high rate of consumption of liquid helium. If the cooling path can be improved sufficiently, liquid nitrogen will suffice. Modulation at very high frequencies is virtually assured, since the laser is identical in this respect with the diodes modulated earlier.

Dynagroove—Electronic Compensation of Distortion in Stereo Disk Recordings

by DR. J. G. WOODWARD AND E. C. FOX,
RCA Laboratories, Princeton, N. J.

The most fundamental and most troublesome cause of distortion in disk recording systems has now been largely eliminated by use of a dynamic distortion-compensation system developed at the RCA Laboratories. The distortion compensation is carried out by a self-contained unit that is connected into a standard recording system. In late February 1963, the RCA Victor Record Division announced the new *Dynagroove* stereophonic recordings which, in addition to other improvements, have very low distortion brought about by use of the new compensation system.

All disk recordings are made by use of a chisel-shaped cutter, but they are reproduced by a ball-shaped stylus. This difference in geometry gave rise to "tracing distortion" for the following reasons. For each stereo channel, the motion of the reproducing stylus must be identical with the motion of the cutter during recording if the distortion is to be low. The identical motions can occur only when the same point on the ball-shaped reproducing stylus always touches the groove, for a shift of the contact to another point on the curved surface of the ball changes the stylus deflection. In practice, such a shift occurs when the radius of the ball is no longer negligible compared with the radius of curvature of the groove modulation. The resulting deviation in stylus deflection causes tracing distortion, which is most apparent to the listener for high frequencies and when the pickup is near the center of the record.

It has been known for several years, and has been demonstrated in RCA Laboratories, that tracing distortion can be reduced by inverting the reproduced signal and rerecording it on a second master to give a complementary predistortion during this final recording. However, this method was found to be impractical because of its complexity and the inevitable loss in fidelity due to the double recording. The new method uses all-electronic precompensation of the signal fed to the cutter, a precompensation that takes into account amplitude, frequency, and the nearness of the cutter to the center of the record, and maintains the necessary control of the phase. While the circuitry is necessarily sophisticated, it is used only in the recording operation.

The first model of the two-channel system was tested by the Record Division in production equipment for stereo disk recording. The electronic system gives a reduction in distortion that is definitely appreciated by the listener, particularly in the inner portion of the recording where tracing distortion has been the most troublesome.

Simple Tunnel-Diode Synchonizer Gives HF Scopes New UHF Capability

by F. M. CARLSON,
Semiconductor and Materials Division, Somerville, N. J.

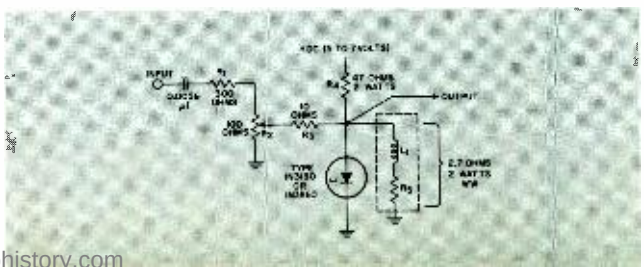
Many sampling oscilloscopes and some older-model scopes have signal bandwidths greater than their trigger (sync) circuits are capable of handling. Such scopes could easily display a 480-Mc sine wave if a reliable and stable method of triggering them were available. The tunnel-diode circuit shown in (Fig. 1) provides a convenient method of synchronizing any HF scope to any constant UHF up to the signal-bandwidth limits of the scope. Although the circuit shown does not provide an optimum method of synchronizing UHF scopes, it is one of the simplest and least expensive synchronization techniques. The upper frequency limit of the tunnel-diode circuit has not been determined, but is at least 1.2 Gc.

In operation, a DC bias of 5 to 7 volts applied to the synchronizer biases the tunnel diode in its negative-resistance region. Because this region is unstable, the diode begins to oscillate at a frequency controlled primarily by inductor L_1. For the value of inductance shown, the frequency is unimportant for this application. When as a UHF signal is applied to the input, the tunnel diode "locks" onto it, the output signal generated is an exact subharmonic of the input. This output, approximately 500 mv peak-to-peak, is used to trigger the sampling scope. The output frequency, about 10 Mc, is low enough to be within the frequency capabilities of the sync circuits of any HF scope.

In Fig. 1, C_1 blocks DC from the input circuit, and R_1 maintains input impedance at a fairly constant level in spite of variations in R_2 and also attenuates feedback from the output to input; R_2 attenuates large input signals, and R_3 prevents excessive currents if the wiper arm of R_2 is turned to ground; R_4 limits current, and R_5 forms a monostable lead line for the tunnel diode; L_1 sets the approximate frequency of oscillation.

Because the output and input are not totally isolated, some output signal appears at the input. This feedback is not objectionable

Fig. 1—Tunnel-diode sync circuit.



unless the input signal is small. If the feedback does disturb the signal source, a tunnel rectifier can be inserted between R_2 and R_3 to provide a fairly effective remedy. The tunnel rectifier passes the input signal with much less attenuation than an ordinary diode, but effectively blocks most of the output signal from the input circuit.

In use, a DC bias of 6 volts is applied first, and then the UHF signal is applied to the input. The trigger controls of the scope, potentiometer R_2, and the DC bias are adjusted until a stable display appears on the screen. (A well-regulated DC power supply is preferable.) If the scope display goes out of synchronization as the result of a change in input frequency or slight changes in circuit components due to heating, the DC bias can be varied by a few tenths of a volt to make the display stable again. The DC bias affects the self-oscillating frequency of the diode; by varying the bias the diode frequency can be brought close enough to some submultiple of the input frequency to lock the diode onto the input.

The author has successfully displayed a 1.2 —Gc sine wave on a sampling scope having trigger circuits ordinarily capable of handling a maximum of only 100 Mc. The circuit shown is also capable of providing countdowns from UHF frequencies in ratios from 2:1 to more than 100:1.

A Precise Technique for Measuring Satellite Moments of Inertia

by R. A. SCHIFFER AND J. REBMAN, *Astro-Electronics Division, DEP, Princeton, N. J.*

The principal moments of inertia of a satellite must be accurately measured to assure stable orbital motion and to maintain the desired attitude control. The Astro-Electronics Division, during its development of TIROS, RELAY, and SERT,[3] has developed a generalized laboratory technique for obtaining such precise moment-of-inertia data.

Basic to all techniques that might be used to measure polar moment of inertia, I, is determination of the relation between torque T and angular acceleration α about the desired axis ($I = T/\alpha$). There are two general methods of applying the torque: 1) a unidirectional drive such as a motor, and 2) an oscillatory drive such as a torsion pendulum or other torsional spring device. Both T and α may be measured directly or indirectly, and I may be measured directly or calculated.

Torsional Pendulum Design: The torsion-pendulum method was selected and the maximum anticipated error (in which the vehicle support structure was considered) was calculated using the first-order equation of motion for the torsion pendulum (first-order is sufficient if angular displacements are limited to less than 5°).

The moment of inertia I is given by:

$$I = \frac{WR^2\tau^2}{4\pi^2 L} \tag{1}$$

The fractional error in I is given by:

$$\frac{\Delta I}{I} = \frac{\Delta W}{W} + \frac{2\Delta R}{R} + \frac{2\Delta\tau RW^{1/2}}{(4\pi^2 LI)^{1/2}} + \frac{\Delta L}{L} + \frac{f}{I} \tag{2}$$

Where: R = radius of pendulum, W = weight, τ = period of oscillation, L = length of pendulum, f = friction term, ρ = radius of gyration, and δ = displacement.

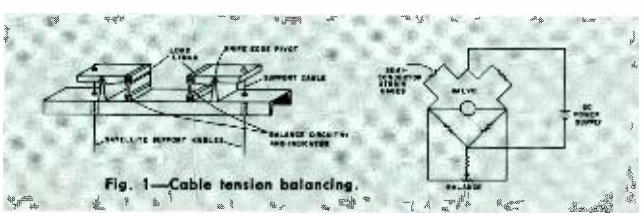


Fig. 1—Cable tension balancing.

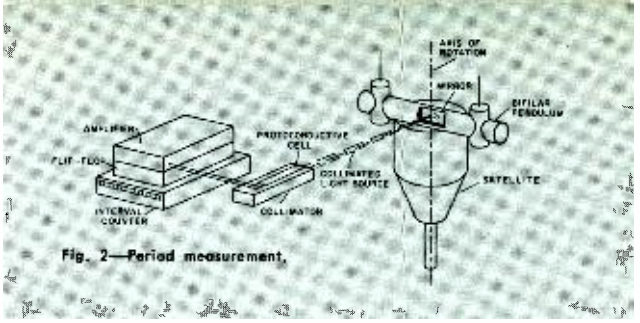


Fig. 2—Period measurement.

By differentiating Equation 2 with respect to R and setting the derivative equal to zero, the value of R for which $\Delta I/I$ is minimized is:

$$R = \left| \frac{\Delta R}{\Delta T} \left(\frac{4\pi^2 LI}{W} \right)^{1/2} \right|^{1/2} \tag{3}$$

With R from Equation 3, the largest practical value of L, the approximate values of W and I, and conservative "$\triangle$" values, Equation 2 can be used to estimate the maximum error. The value of f is the lumped friction factor; conservative estimates placed the value of f/I at less than 0.1% (a value substantiated by the extremely low damping observed.) In practice, a smaller total error is probable because it is unlikely that all errors will act in the same direction; however, for assurance, the maximum value should be used. (The maximum estimated error of the RELAY measurement was 0.5%.)

A two-wire, or *bifilar*, suspension was used for simplicity. The pendulum length L was about 330 inches, and the radius R was about 20 inches. Care was necessary to assure that the angular displacement and period are large enough that the body being measured can be considered a rigid body. The period of 3 to 4 seconds and the displacement about the axis of approximately 2° used for RELAY measurements are sufficient to ensure that the elemental masses are all moving in phase through the same angular displacement. The error introduced by measuring I about an axis displaced a distance δ from the principal axis is $(\delta/\rho)^2$. For RELAY, ρ was about 10 inches. Therefore, for δ equal to 0.1 inch, the error is approximately 0.01%, which is negligible.

For the pendulum configuration shown (Figs. 1, 2) the conditions described above correspond to a difference in the cable tension of $\Delta T \approx W\delta/R = 0.5$ lb. The calibration of the tension-measuring load cells indicates that the value obtained for $\triangle T$ is well below the tolerable minimum.

Instrumentation: To achieve proper cable-tension balancing, a cable-support system was designed which accurately senses the relative cable tensions. Specifically (Fig. 1) each cable is attached to a member which is free to rotate about a knife edge. The resulting moment is balanced by a load cell secured at the opposite side of the pivot. A Wheatstone-bridge circuit is employed, with the two load cells incorporated in opposite bridge arms such that equal cable tensions correspond to a null bridge condition. Thus, the cable tensions are kept within the differential amount prescribed by the error analysis.

To measure only the pure torsional period of oscillation, an optical system was designed to sense pure rotation and be insensitive to any *non*rotational (i.e. translational) motion. A thin band of high-intensity, collimated light was projected on a small mirror affixed at the rotational axis of the oscillating satellite (Fig. 2). As the satellite oscillates, the band of light periodically becomes normal to the mirror and is reflected directly back to the source, where it triggers a photocell. That signal (amplified) is fed through a flip-flop which passes only alternate pulses, and finally to an electronic interval-counter. Since the photocell responds only when the light source is normal to the mirror; *only rotation is sensed*, and all translational effects are eliminated.

Following calibration, measurements on RELAY required both pitch and yaw inertias. This can be accomplished by making three readings 45° apart and constructing a Mohr's Circle[2] to obtain the maximum-minimum transverse inertias. In this test, four sets of such measurements were made, each set shifted 45°. With two sets used as a check, the method proved to be very accurate, since both sets of calculations gave identical results.

1. R. Becker, *Introduction to Theoretical Mechanics*, McGraw-Hill, 1954.
2. Marks, *Mechanical Engineers Handbook*, 6th edition, McGraw-Hill, 1958.
3. TIROS is a meteorological satellite developed, fabricated, and tested for NASA. RELAY is a communications satellite being developed for NASA. SERT (Space Electric Rocket Test) is a satellite being developed to obtain data on ion propulsion engines in a space environment.

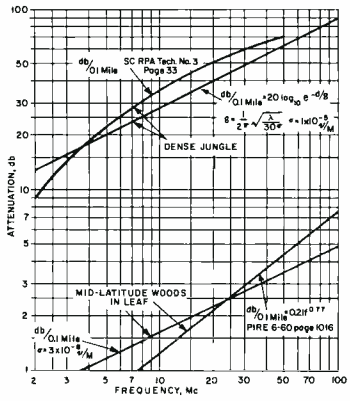


Fig. 1—Attenuation data.

HF and VHF Radio-Wave Attenuation Through Jungle and Woods

by S. KREVSKY,
Surface Communications Systems Laboratory, Surface Communications Division, DEP, New York, N.Y.

Experimental information on less through woods and jungles has been made available by a number of investigators.[1-4] However, analytic substantiation has been lacking. In this *Note*, a simple extension of the theory developed by Stratton[5] and Wheeler[6] has been applied to HF and VHF radio-wave attenuation in dense jungles.

The theory for the loss in the foliage is essentially the same as that for loss in any medium such as sea water where the field is attenuated exponentially with distance: Received field $= E = E_o \exp(-d/\delta)$; skin depth, meters $= \delta = (1/2\pi)\sqrt{\lambda/30\sigma}$; medium conductivity, mhos per meter $= \sigma$; and the loss in db $= \alpha = 20 \log_{10} |\exp(-d/\delta)|$. (*Note:* when $d = \delta$, then $\alpha = 8.68$ db.) Table 1 lists typical skin depths for various lossy media for 3 and 30 Mc.

The experimental information on the attenuation of ground-wave field strength versus distance at various frequencies, for vertically polarized waves through dense jungles of New Guinea, is derived from Reference 4 and page 33 of Reference 3. Fig. 1 shows this information replotted with *db per 0.1 mile* as a function of frequency together with the new curve of the analytical results. The loss due to midlatitude woods in leaf (also on Fig. 1) shows that a three-fold order-of-magnitude difference exists in relative conductivity between dense jungle and ordinary midlatitude woods in leaf. Obviously, specific identification and classification of the physical characteristics of foliage is necessary before reasonably close estimates of attenuation are feasible. On the other hand, Fig. 1 is indicative of the upper and lower loss limits, and Table 1 of the spread of typical physical constants.

TABLE 1—Typical Skin Depths for Various Lossy Media

Medium	*Conductivity* *Mhos/Meter*	*Skin Depth at 3Mc* *Meters*	*Skin Depth at 30Mc* *Meters*
Sea Water	4	0.15	0.05
Wet Soil (CCIR)[7]	3×10^{-2}	1.6	0.5
Fertile Soil (CCIR)	1×10^{-2}	2.9	0.9
Dry Soil (CCIR)	3×10^{-3}	5.1	1.6
Very Dry Soil (CCIR)	1×10^{-3}	9.1	2.9
Dry Soil Minimum (Wheeler)	1×10^{-4}	29	9.2
Dry Soil Minimum (Stratton)	1×10^{-5}	91	29
Dense Jungle Foliage	1×10^{-5}	91	29
Midlatitude Woods	3×10^{-8}	1600	500

1. H. T. Head, "The Influence of Trees on TV Field Strengths at UHF," *Proc. IRE*, Vol. 48, pp 1016-1020, June 1960.
2. B. Trevor, "UHF Propagation Through Woods and Underbrush," *RCA Review*, 1940-41, 5, p. 97.
3. *Ground Wave Field Intensities*, Signal Corps Radio Propagation Agency, Fort Monmouth, New Jersey Technical Report No. 3, Revised June 1949. Pages 9 and 33.
4. *Radio Propagation Through the New Guinea Rain Forest*, New Zealand Dept. of Scientific and Industrial Research (DSIR), Operational Research Section (ORS), Australia, Report No. 8-1944.
5. J. A. Stratton, *Electromagnetic Theory*, McGraw-Hill, N. Y., 1941, Pages 297-304, 344, and 345.
6. H. A. Wheeler, "Universal Skin Effect Chart for Conducting Materials," *Electronics*, Nov. 52, Pages 152-154; and H. A. Wheeler, "Fundamental Limitations of a small VLF Antenna for Submarines," *Trans. IRE-PGAP*, Vol. AP-6, No. 1; Jan. 58, pp. 123-125.
7. *Ground-Wave Propagation Curves Below 10 Mc*, CCIR Recommendation No. 307, Los Angeles, 1959.

Acknowledgment: The work reported in this paper was supported by the Communication Department of the U.S. Army Electronic Research and Development Laboratory under contract DA 36-039-AMC-00011 (E).

Thin-Film Resistors for Digital Microcircuits

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RCA's first Digital Microcircuits[1] used Cermet rod resistors. Although satisfactory from the standpoint of electrical and mechanical performance, these components had two drawbacks for long-term production planning:

1) The Cermet resistors were a purchased item, and cost projections for large quantities did not approach what was considered to be a reasonable price (the rule of thumb used was that the cost of each resistor should be less than that of a semiconductor pellet).
2) The cylindrical rod resistors did not lend themselves to future integration—either in fabrication or assembly. That is, each piece required separate handling for metallization, test, mounting, and bonding.

The solution adopted by the Computer Products Department of S&MD was the development of thin-film resistors. As shown in Fig. 1, about 700 resistors, each 0.036 by 0.036 inch, are evaporated on a glass substrate. This production technique is relatively inexpensive because all the labor costs of masking, metallization, and evaporation are divided by the relatively large number of units obtained. Only when the wafer is finally probed, diced, and sorted are individual costs incurred. Because these operations are the same as those used in the manufacture of transistors, both the necessary equipment and manufacturing skills are available in Somerville.

Each resistor has gold contacts and a gold-plated back, so that it can be mounted and bonded in the same manner as semiconductors. The resistive material, nichrome, has a silicon monoxide overcoating. Fig. 2 shows a Digital Microcircuit flip-flop circuit, fabricated from nine semiconductors and six thin-film resistors. These resistors are now made in values ranging from 20 ohms to 50,000 ohms, in tolerances of ±2, 5, and 10 percent. The temperature coefficient is 100 ppm/°C, and the power dissipation is 100 mw at 125°C.

The excellent electrical characteristics of these units at an effective dissipation rate of 200 watts/sq in. is attributable to two factors:

1) The use of flame-polished glass as the substrate material provides an extremely smooth surface that eliminates "hot spots" in the resistor, the major cause of instability under high power dissipation.
2) The units are hermetically sealed in a dry nitrogen atmosphere, which reduces oxidation and insures operating-life stability.

[Graphs showing the variation of resistor tolerance over a wafer, temperature coefficient from −55 to 125°C, and load life characteristics are available from the author.]

1. Medwin, A. H., "Digital Microcircuit Packages available from SC&M" RCA ENGINEER, *(Engineering & Research Notes)*, Vol. 8, No. 4, Dec. 1962-Jan. 1963, pp 40-41

Fig. 1—Top: Portion of wafer (each sector 0.36" sq.) showing gold contacts. Bottom: Resistive film evaporated on contacts.

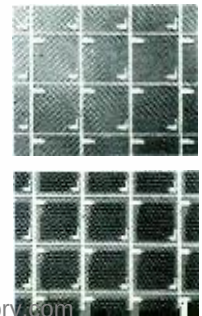
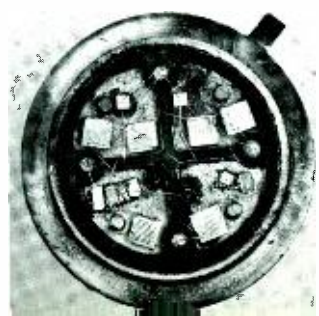
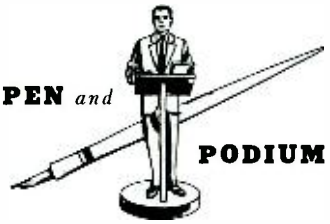


Fig. 2—DMC flip-flop; 9 semiconductors and 6 thin-film resistors.





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In January 1963, the IRE and the AIEE merged to form the Institute of Electrical and Electronics Engineers, Inc.—the IEEE. This has been reflected below in noting the sponsorship of conferences. Also, note that former IRE Professional Groups (PG's) and AIEE Technical Groups (TG's) are now called "Professional Technical Groups," or PTG's.

DATES *and* DEADLINES

Professional Meetings and Calls for Papers

Meetings

June 4-5, 1963: 5th Natl. Radio Frequency Interference Symp., PTGRFI; Bellevue-Stratford, Philadelphia, Pa. *Prog. Info.:* A. R. Kall, Ark Electronics Corp., 624 Davisville Rd., Willow Grove, Pa.

June 11-13, 1963: Natl. Symp. on Space Electronics and Telemetry, IEEE-PTGSET; Los Angeles, Calif. *Prog. Info.:* J. R. Kauke, Kauke and Co., 1632 Euclid St., Santa Monica, Calif.

June 14-17, 1963: 1st Natl. ISA Biomedical Sciences Instrumentation Symp.; Union Oil Co. Bldg., Los Angeles, Calif. *Prog. Info.:* R. E. Becker, Pacific Finance Corp., 621 S. Hope St., Los Angeles 17, Calif.

June 17-18, 1963: 1963 Chicago Spring Conf. on Broadcast and TV Receivers, PTGBTR Chicago Sect.; O'Hare Inn, Chicago, Ill. *Prog. Info.:* A. Cotsworth, Zenith Radio Corp., 6001 W. Dickens, Chicago, Ill.

June 19-21, 1963: Joint Automatic Control Conf., IEEE-ISA-ASME-AIChE; Univ. of Minnesota, Minneapolis, Minn. *Prog. Info.:* O. L. Updike, Univ. of Va., Charlotte, Va.

July 9-11, 1963: PTGAP Intl. Symp., PTGAP; Central Radio Prop. Lab., NBS, Boulder, Colo. *Prog. Info.:* Herman V. Cottony, NBS Labs., Boulder, Colo.

July 22-26, 1963: 5th Intl. Conf. on Medical Electronics, IFME; Univ. of Liege, Palais des Congres, Liege, Belgium. *Prog. Info.:* Dr. F. Bostem, 23 Blvd. Frere Orban, Liege, Belgium.

August 4-9, 1963: Intl. Conf. and Exhibit on Aerospace Support, IEEE-ASME; Sheraton-Park Hotel, Washington, D. C. *Prog. Info.:* D. B. Dobson, Systems Support Sec. 518, RCA, P. O. Box 588, Burlington, Mass.

August 20-23, 1963: WESCON (Western Electronic Show and Conf.), WEMA-All PTG's; Cow Palace, San Francisco, Calif. *Prog. Info.:* WESCON, 1435 La Cienega Blvd., Los Angeles, Calif.

Calls for Papers

August 12-14, 1963: Guidance and Control Conf.; Kresge Auditorium, Mass. Institute of Tech., Cambridge, Mass. *DEADLINE:* Abstracts; **3/15/63;** Manuscripts **6/17/63.** *For Info.:* Dr. Charles J. Mundo, Institute of Naval Studies, 185 Alewife Brook Parkway, Cambridge, Mass.

Oct. 7-9, 1963: 9th Natl. Communications Symp., PTGCS; Hotel Utica, Utica, N. Y. *DEADLINE:* Abstracts, approx. **6/1/63.** *For Info.:* IEEE Hdqs., 1 E. 79th St., New York 21, N. Y.

Oct. 21-23, 1963: East Coast Conf. on Aerospace and Navigational Electronics (ECCANE), PTGANE; Baltimore, Md. *DEADLINE:* Abstracts, approx. **7/2/63.** *For Info.:* IEEE Hdqs., 1 E. 79th St., New York 21, N. Y.

Oct. 28-30, 1963: Natl. Electronics Conf., IEEE and others; McCormick Place, Chicago, Ill. *DEADLINE:* Abstracts, **5/15/63**; Manuscripts, **8/1/63.** *For Info.:* Dr. Hansford W. Farris, E. E. Dept., Univ. of Mich., Ann Arbor, Mich.

Oct. 29-31, 1963: 10th Ann. Mtg. PGNS; 2nd Intl. Symp. on Plasmas Phenomena and Meas., PTGNS; El Cortez Hotel, San Diego, Calif. *DEADLINE:* Abstracts, approx. **7/1/63.** *For Info.:* O. Lyle Tiffany, Bendix Sys. Div., Ann Arbor, Mich.

Oct. 31-Nov. 1, 1963: 1963 Electron Devices Mtg., PTGED; Sheraton-Park Hotel, Washington, D. C. *DEADLINE:* Abstracts, approx. **8/1/63.** *For Info.:* IEEE Hdqs., 1 E. 79th St., New York 21, N. Y.

Nov. 4-6, 1963: NEREM (Northeast Res. and Eng. Mtg.), IEEE; Boston, Mass. *DEADLINE: Abstracts,* **6/7/63.** *For Info.:* NEREM-IEEE; Boston Office, 313 Washington St., Newton, Mass.

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Nov. 11-13, 1963: Radio Fall Meeting, IEEE-EIA; Hotel Syracuse, Syracuse, N. Y. *DEADLINE:* Abstracts, approx. **7/15/63.** *For Info.:* V. M. Graham, EIA Engrg. Dept., 11 W. 42nd St., New York 36, N. Y.

Nov. 12-14, 1963: Fall Joint Computer Conf., AFIPS (IEEE-ACM); Las Vegas Convention Center, Las Vegas, Nev. *DEADLINE:* Abstracts, approx. **6/1/63.** *For Info.:* J. D. Madden, Systems Dev. Corp., Santa Monica, Calif.

Nov. 18-20, 1963: 16th Ann. Conf. on Engineering in Medicine and Biology, IEEE-ISA; Lord Baltimore Hotel, Baltimore 3, Md. *DEADLINE:* Abstracts, **8/1/63.** *For Info.:* 16th Ann. Conf., Jenkins Hall—Johns Hopkins Univ., Baltimore 18, Md.

Dec. 5-6, 1963: 14th Natl. Conf. on Vehicular Communications, PTGVC; Dallas, Texas. *DEADLINE:* Abstracts, approx. **8/15/63.** *For Info.:* A. C. Simmons, Comm. Industries Inc., 511 N. Akard, Dallas, Tex.

Jan. 7-9, 1963: 10th Natl. Symp. on Reliability and Quality Control; Statler Hilton Hotel, Washington, D. C. *DEADLINE:* Abstracts, **5/15/63;** Manuscripts, **10/7/63.** *For Info.:* Dr. L. S. Gephart, Lockheed Missiles and Space Co., Depart. 64-01, Building 104, Sunnyvale, Calif.

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Surface Decoration and Domains in Very Thin Magnetic Films—M. D. Coutts: New York Society of Electron Microscopy, N. Y., March 21, 1963

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A Study of Tracking-Angle Errors in Stereodisk Recording—J. G. Woodward and E. C. Fox: EIA Recording Committee, Feb. 4, 1963; and IEEE International Convention, New York, March 28, 1963

The Behavior of Electrons in Strong Crossed Electric and Magnetic Fields—M. Glicksman and W. Hicinbothem: American Physical Society meeting, St. Louis, Mo., March 25-28, 1963

Evaporated Metal Contacts to Conducting Cadmium Sulfide Single Crystals—A. M. Goodman: Physical Society meeting, St. Louis, Mo., March 24-27, 1963

The Energy Distribution of Ions Formed in RF Spark Source—J. R. Woolston and R. E. Honig: ASTM E14 Conference on Mass Spectrometry, San Francisco, Calif., Feb. 19-24, 1963

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3,075,031—Lead Telluride-Tin Telluride Thermoelectric Compositions and Devices, Jan. 22, 1963; E. F. Hockings and W. L. Mularz

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3,075,083—Image Amplifying Device, Jan. 22, 1963; D. Kleitan and J. E. Ruedy

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3,076,051—Thermoelectric Devices and Methods of Making Same, Jan. 29, 1963; V. Haba

3,076,115—Traveling Wave Magnetron Amplifier Tubes, Jan. 29, 1963; P. T. Smith

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RCA VICTOR HOME INSTRUMENTS DIVISION

3,075,085—Synchronous Transistor Amplifier Employing Regeneration, Jan. 22, 1963; W. A. Helbig and G. W. Booth

3,075,171—Remote Control Receiver, Jan. 22, 1963; R. B. Hansen

3,080,528—Transistor Amplifier Circuits Utilizing a Zener Diode for Stabilization, Mar. 5, 1963; J. J. Davidson

3,080,529—Plural Input Signal Translating System, Mar. 5, 1963; J. B. Schultz and G. E. Theriault

DEFENSE ELECTRONIC PRODUCTS

3,075,189—Radar, Jan. 22, 1963; A. J. Lisicky

3,076,106—Inductive Circuits, Jan. 29, 1963; T. Douma

3,076,145—Pulse Discriminating Circuit, Jan. 29, 1963; W. O. Copeland and N. D. Latham

3,076,181—Shifting Apparatus, Jan. 29, 1963; V. L. Newhouse and A. S. Rettig

3,076,923—Overhead Protective Circuit, Feb. 5, 1963; D. J. Poitras

3,079,598—Analog-to-Digital Converter, Feb. 26, 1963; S. Wald

BROADCAST AND COMMUNICATIONS PRODUCTS DIV.

3,076,069—Combined Sensing and Switching Device, Jan. 29, 1963; M. DeCamillis, J. J. Hoelin and W. E. Johnson

3,079,467—Magnetic Head Construction, Feb. 26, 1963; M. Rettinger

ELECTRONIC DATA PROCESSING

3,076,943—Automatic Frequency and Phase Control, Feb. 5, 1963; M. Cooperman

3,079,472—Magnetic Field Structure for Transducers and Method of Constructing Same, Feb. 26, 1963; A. A. Sariti

ELECTRON TUBE DIVISION

3,081,526—Method of Making Electrode Spacing Means, Mar. 19, 1963; H. K. Donnell

3,082,115—Method of and Apparatus for Spraying Cathodes with Emissive Materials, Mar. 19, 1963; W. F. Griffin and J. F. Miller

RCA INTERNATIONAL DIVISION

3,077,550—High Voltage Power Supply Regulation, Feb. 12, 1963; A. Macovski

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Photoconductivity in Cubic Cadmium Sulfide—R. H. Bube and E. L. Lind: *Journal of Chemical Physics*, November 15, 1962

Optical Properties of the Silver and Cuprous Halides—M. Cardona: *The Physical Review*, January 1, 1963

Determination of Zirconium and Hafnium with Xylenol Orange and Methylthymol Blue—K. L. Cheng: *Analytical Chimica Acta*, October 23, 1962

Analytical Applications of Xylenol Orange-VI—Dr. K. L. Cheng: *Talanta*, December 1962

4,4′-Bis (dimethylamino) thiobenzoohenane (Thio-Michler's Ketone) and Its Related Compounds as Sensitive Reagents for Gold—K. L. Cheng and P. F. Lott: International Symposium on Microchemical Technology

Radiation-Induced Changes in Silicon Photovoltaic Cells—J. A. Baicker and B. W. Faughnan: *Journal of Applied Physics*, November 1962

Radiation Defect Introduction Rates in n- and p-Type Silicon in the Vicinity of the Radiation Damage Threshold—H. Flicker, J. J. Loferchi and J. Scott-Monck: *Physical Review*, December 15, 1962

ELECTRON TUBE DIVISION

Management's Role in Better Technical Papers—C. A. Meyer: IRE Joint PGEWS-PGEM Meeting, Syracuse, N. Y., January 24, 1963

Nuvistors for VHF Applications—R. M. Mendelson: Union County Amateur Radio Assoc., Roselle, N. J., January 25, 1963

The Electronic Organ Tuner (Part I)—A. M. Seybold: *Audio*, February 1963

Some Special Accessories for XRD-3, -5, and -6 X-Ray Secondary-Emission (Fluorescence) Spectrometers—E. P. Bertin and R. J. Longobucco: 4th Annual Seminar on X-Rays, Stevens Institute, Hoboken, N. J., January 28-30, 1963

X-Ray Fluorescence Spectrometric Analysis—E. P. Bertin: GE Seminar on X-Ray Spectrometry, Stevens Institute, Hoboken, N. J., January 28-30, 1963

Arc Protection Circuit—D. D. Mawhinney, *Electronics*, February 22, 1963

Microwave Devices—H. K. Jenny: Seminar for European RCA Distributors, Geneva, Switzerland, February 25-March 1, 1963

Theory and Performance of Depressed Trochoidal Collectors for Improving Traveling-Wave-Tube Efficiency—T. S. Chen, H. J. Wolkstein and R. W. McMurrough: IEEE International Convention, New York City, March 25-28, 1963

Factors Limiting the Resolution of Magnetically Focused Image-Intensifier Tubes — T. P. Csorba: AIEE Winter General Meeting, New York, N. Y., January 30, 1963

Opportunities in Electronics and Electrical Engineering—R. A. Lee: Pennington School for Boys, N. J., February 25, 1963

Characteristics and Applications of RCA Photosensitive Devices—A. G. Nekut: Seminar for European RCA Distributors, Geneva, Switzerland, February 25-March 1, 1963

High-Energy Rate Forming—G. L. Fassett: Lions Club, Landisville, Pa., March 4, 1963

Electronic Image Converter and Intensifier Tubes—G. A. Morton: Bronx High School of Science Astronomy Society, New York, N. Y., February 1, 1963

Cuprous Chloride Light Modulators—F. Sterzer, D. J. Blattner and S. F. Minter: Solid-State Circuits Conference, Philadelphia, Pa., February 20, 1963

Microwave Phototubes with Transmission Photocathodes—H. C. Johnson, D. J. Blattner, F. Sterzer and J. E. Ruedy: IEEE International Convention, New York City, March 25-28, 1963

SEMICONDUCTOR AND MATERIALS DIVISION

New Developments in Primary and Secondary Batteries—G. S. Lozier: Electrochemical Society Section Meetings, Boston, Mass., January 22, 1963

Techniques Associated with the Production of Micromodules—P. Nyul: New York Metropolitan Chapter of IRE-PGEP, January 23, 1963

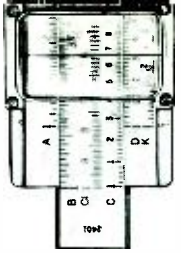
State of the Art in High-Frequency High-Power Transistors—J. Hilibrand: AIEE Winter General Meeting, New York, N. Y., January 28, 1963

L-Band GaAs Tunnel-Diode Oscillators with Power Outputs in the Range from 10 to 100 mw—A. Presser and A. E. Roswell: *Proceedings of the IRE* (Correspondence) January 1963

Radiochemical Determination of Zone-Refining Impurity Segregation in Gallium Trichloride—W. Kern: *Journal of Electrochemical Society*, January 1963

Some Factors Affecting the Degradation of GaAs Tunnel Diodes—A. Pikor, G. Elie, and R. Glicksman: *Journal of Electrochemical Society*, February 1963

Leak Detection of Semiconductor Device Hermetic Seals—D. B. Pearson: *Semiconductor Products*, February 1963

Engineering  **NEWS** *and* **HIGHLIGHTS**

TEN RCA EMPLOYEES RECEIVE SARNOFF FELLOWSHIPS

David Sarnoff Fellowships for graduate study in the 1963-64 academic year for ten RCA employees were announced recently by **Dr. Douglas H. Ewing,** RCA Vice President and Technical Director and Chairman of the RCA Education Committee. The Fellowship grants include full tuition and fees, plus an allowance for books, a stipend of $2,500 to $4,000 depending on the *Fellow's* marital status, and $1,000 as an unrestricted gift to the university. Although appointments are for one academic year, each *Fellow* is eligible for reappointment. Three of the ten recipients named this year are receiving awards for the second consecutive year.

David Sarnoff Fellows are selected on the basis of academic aptitude, promise of professional achievement, and character. Those receiving the awards have been granted leaves of absence from various RCA divisions and subsidiary companies.

The Fellows reappointed for a second year are:

Harold E. Davis, 27, NBC, Burbank, California, to continue studies toward an MBA in Financial Management at Columbia University.

Jacob Klapper, 32, DEP Surface Communications Laboratories, New York, to continue studies toward a Doctorate in Electrical Engineering at Brooklyn Polytechnic Institute.

John J. Moscony, 33, Electron Tube Division, Lancaster, Pa., to continue studies toward a Doctorate in Chemistry at the University of Pennsylvania.

The Fellows appointed for the first time are:

Alexander Avanessians, 40, RCA Communications, Inc., New York, to begin study toward a Doctorate in Communications at Columbia University.

Roger W. Cohen, 23, RCA Laboratories, Princeton, to continue studies toward a Doctorate in Physics at Rutgers.

Henry Kressel, 29, Semiconductor and Materials Division, Somerville, New Jersey, to study for a Doctorate in Physics at the University of Pennsylvania.

Martin L. Levene, 30, DEP Applied Research, Camden, to begin work toward a Doctorate in Mechanical Engineering at the University of Pennsylvania.

Robert A. Howell, 24, DEP Surface Communications Division, Camden, to study for a Doctorate in Industrial Management at the Massachusetts Institute of Technology.

John J. Serratore, 27, Electronic Data Processing, Cherry Hill, New Jersey, to begin study toward a Master of Business Administration degree at the University of Pennsylvania.

David E. Burrington, 31, National Broadcasting Company, Inc., Philadelphia, Pa., to study for a Master of Fine Arts degree.

FLORY, GREIG, MUELLER NAMED LABS FELLOWS

L. E. Flory, H. G. Greig, and **Dr. C. W. Mueller** have been named *Fellows of the Technical Staff* of the RCA Laboratories, Princeton, for their continued outstanding technical achievements. The significance of the title of *Fellow* is comparable to that used by technical societies and universities. It indicates leadership through individual contributions (rather than through managerial service).

Mr. Flory has been with RCA since 1930 and is known for television developments. He has received three *RCA Laboratories Achievement Awards* and holds 40 patents, primarily in industrial television.

Mr. Greig joined RCA Laboratories in 1943, and has primarily worked on chemical problems relating to electrophotography and ELECTROFAX. He holds three *RCA Laboratories Achievement Awards*, and 16 patents.

Dr. Mueller joined RCA in 1942 and is known for his work in high-frequency transistors. He has received three *RCA Laboratories Achievement Awards*, and was one of the recipients of the *1962 David Sarnoff Outstanding Team Award in Science.*

DR. DOUSMANIS HONORED BY GREEK KING

Dr. George Dousmanis, an RCA Laboratories research physicist, has been awarded the *Golden Cross of the Company of King George I,* by King Paul of Greece. A native of Greece, Dr. Dousmanis has been on leave from RCA Laboratories since August 1962 to work at "Democritus," the new nuclear research center in Athens designed to enable Greece to compete with other nations in the field of atomic energy.—*C. W. Sall*

RCA RESEARCH SYMPOSIUM

Approximately 300 of the government's top military and civilian scientific personnel observed a presentation on RCA Research Programs at the RCA Laboratories in Princeton, during March. The symposium, the largest of its type ever held, was attended by representatives of the Army, Navy, Air Force, Department of Defense, NASA, and government affiliated nonprofit organizations such as the Mitre and Rand Corporations.

DR. WEIMER RECEIVES SOLID-STATE CONFERENCE AWARD

Dr. Paul K. Weimer, RCA Laboratories, Princeton, recently received an *Outstanding Paper* award plaque at the 1963 International Solid-State Circuits Conference held in Philadelphia. Dr. Weimer's paper, "Evaporated Circuits Incorporating a Thin-Film Transistor," presented at the 1962 conference, was cited as "*a vital contribution to a major field of solid-state technology,*" [A later version of this paper appeared in the RCA ENGINEER, April-May 1962, Vol. 7, No. 6, under the title, "The TFT—A New Thin-Film Transistor."]

Dr. Weimer, who received his Ph.D. in Physics from Ohio State University and joined RCA Laboratories in 1942, is well known for his basic contributions to the original development of the image orthicon and vidicon camera tubes used in television, and for his recent pioneering work in thin-film devices. The latter led in 1961 to his achievement of the first known thin-film transistor.

[Dr. Weimer has also just received RCA's highest technical award for research *The David Sarnoff Outstanding Achievement Award for Science*, for 1963. See p. 40, *this issue.*]

HATHAWAY HONORED FOR AUTHORSHIP

J. Lewis Hathaway, Staff Engineer, National Broadcasting Company, has been named to receive the *Scott Helt Award* of the IEEE Professional Technical Group on Broadcasting for his paper, "An Improved Loudness Indicator." The award is given each year for the best paper to appear in the *Transactions on Broadcasting.*

Since 1956, two of Hathaway's NBC projects have been nominated for *Emmy* Awards. In 1956 he engineered the first live television broadcast—via airplane—from Cuba to the United States, and last year he developed "interleaved sound," a method of transmitting sound with a television picture, which was described in his paper in the Feb.-Mar. 1962, RCA ENGINEER.

—*W. A. Howard*

SC&M PRESENTS ANNUAL ENGINEERING ACHIEVEMENT AWARDS

The Semiconductor and Materials Division recently honored its engineers at the Division's fourth annual *Engineering Achievement Award* presentations. **Dr. Alan M. Glover,** Vice President and General Manager of the Division, presented the awards.

In recognition of outstanding performance, individual awards were presented to:

Milton J. Grimes, "*. . . for outstanding contribution to a number of successful device package development programs.*"

Theodore W. Kisor, "*. . . for accomplishments and contributions in the field of packaging design and in specific recognition for his creative ability.*"

Andrew C. Knowles, III, "*. . . for the high degree of customer acceptance and confidence which Mr. Knowles has achieved.*"

Robert E. Lepore, "*. . . for his outstanding contribution in the development of the 601 Memory Stack.*"

Robert J. Ryan, "*. . . for technical achievement and dedicated effort in developing a battery system for use in missile applications.*"

The following engineering teams received special recognition:

Fred Cohen, Leonard H. Gibbons, Jr., Henry Kressel, Hon Chui Lee, and Arthur H. Solomon, "*. . . for combined accomplishments in the development of a new product line of varactor devices.*"

Donald Pahls and Jerome E. Wright, "*. . . for combined accomplishments in the design and process improvements in an important family of RCA transistors.*"

Eric F. Cave and Bohdan R. Czorny, "*. . . for outstanding performance in the field of epitaxial technology.*"

LABS PRESENT 1962 ACHIEVEMENT AWARDS

The RCA Laboratories have named the following as recipients of 16th annual *RCA Laboratories Achievement Awards*. These 1962 awards are in recognition of outstanding contributions by members of the RCA Laboratories.

Donat D'Agostini, *for research leading to the development of an interpretive pulsed-plasma diagnostic technique.*

Philip K. Baltzer, *for research leading to improved ferrites with superior temperature tolerance for computer memories.*

Robert A. Gange, *for the conception and theoretical analysis of cryoelectric logic and memory devices.*

Jacob M. Hammer, *for research demonstrating the correlation between shot-noise current and thermal velocity noise in traveling-wave tubes.*

Frederick H. Nicoll, *for the conception of a new technique for growth of epitaxial semiconductor layers.*

John O. Schroeder, *for the development of novel circuitry for frequency-modulation stereophonic reception.*

John E. Volkmann, *for advances in the development of architectural acoustics.*

J. Torkel Wallmark, *for leadership, selective judgment, and technical resourcefulness in providing new semiconductor devices for evaluation in experimental circuits.*

Peter J. Wojtowicz, *for fundamental research leading to advances in the interpretation of magnetic materials phenomena.*

Juan J. Amodei, Joseph R. Burns, and Walter F. Kosonocky, *for team performance in the conception, analysis, and realization of very-high-speed digital circuits.*

Jacques M. Assour, Sol. E. Harrison, George H. Heilmeier, and Alan Sussman, *for team performance in the field of crystalline organic semiconductors and in the development of an organic semiconductor diode.*

Manuel Cardona, David L. Greenaway, and Gunther Harbeke, *for team performance leading to experimental determination and interpretation of band structures of Group IV, III-V, II-VI, and I-VII solids.*

Robert C. Duncan, Zoltan J. Kiss, and P. Neil Yocom, *for team performance in research on new optical maser materials and devices.*

Edward C. Fox, Ralph W. George, and J. Guy Woodward, *for team performance leading to the development of new concepts, elements, and systems for improving the sound quality of disk records.*

Frederic P. Heiman and Steven R. Hofstein, *for team performance in the development and analysis of silicon insulated-gate field-effect devices, and their application to integrated logic nets.*

John A. Inslee, Irwin M. Krittman, and Thomas H. Moore, *for team performance in the conception and development of a high resolution electrostatic image recording and storage system.*

Jeremiah H. Morgan and Winthrop S. Pike, *for team performance leading to the development of specialized television systems for high altitude astronomy.*

Louis S. Napoli and George A. Swartz, *for team performance leading to the conception and development of a new plasma source and to its successful operation in a 23-kilo-megacycle beam-plasma amplifier.*

Santiago R. Polo and Herbert A. Weakliem, *for team performance leading to advances in crystal field theory and applications to optical spectra of solids.*

Ivan H. Sublette and Juri Tults, *for team performance leading to the evolution of new character-recognition techniques.*

GLENN L. DIMMICK, PIONEER RCA INVENTOR & ENGINEER, HONORED ON RETIRING AFTER 33 YEARS SERVICE

Glenn L. Dimmick, a pioneer in the field of optics and sound, particularly in motion pictures and television, was honored by 250 associates recently at a dinner on the occasion of his retirement after a distinguished 33-year professional career with RCA.

Two unusual gifts were presented: One was a bound volume from the RCA Patent Department containing all of the 93 patents he has been granted during his work for RCA. The other was a trophy from DEP Applied Research in the form of a galvanometer, a device for recording sound on film —one of a number of Mr. Dimmick's inventions which won RCA an *Oscar* plaque from the Academy of Motion Picture Arts and Sciences in 1952. The "talking picture" technique employing this device, which Mr. Dimmick patented in 1933, is still widely used in the motion-picture industry.

Another of his inventions was a sound-powered telephone, hand-held and helmet-mounted, used by the tens of thousands during World War II. He also invented production methods for coating optical lenses by which RCA coated millions of lenses during World War II. Since 1948 Mr. Dimmick has been in RCA engineering management. Most recently, he has been coordinator of Applied Research and Development for the DEP Surface Communications Division.

He joined RCA Victor at Camden in 1930, two years after graduation as an electrical engineer at the University of Missouri. He is a member of Tau Beta Pi and Sigma Xi and is a *Fellow* of the Society of Motion Picture and Television Engineers. Among his awards, have been the *SMPTE Progress Medal* (1941); *the RCA Victor Award of Merit* (1949); *and the Missouri Honor Award for Distinguished Service in Engineering* (1955).—*C. W. Fields*

O. H. SCHADE HONORED IN WEST GERMANY

O. H. Schade, Sr., of ETD, Harrison, was recently honored by the Camera Industries of West Germany for his contribution in producing an objective and reproducible method of measuring the interrelationship between contrast rendition and resolution.

In the February 1963 edition of Camera News of West Germany, an article entitled "FRF—The Electronic Approach to Better Lens Quality" by H. J. Schneider presented basic facts about the frequency-response function, how it is presently used by the German optical industry, and how the work was pioneered by O. H. Schade.

—*J. H. Hirlinger*

SUPERPOWER KLYSTRONS FOR STANFORD ACCELERATOR

A $730,800 contract for 72 superpower tubes that will deliver a peak power output of 24 million watts has been awarded to the Electron Tube Division by Stanford University. The klystron amplifier tubes will supply RF energy for the 2-mile linear electron accelerator being built aat Stanford. The contract calls for delivery of three tubes per month starting September 1963. It gives Stanford the option to purchase up to 180 additional tubes. The klystrons will be produced at the ETD plant in Lancaster, Pa. Engineers of ETD Lancaster plant who are responsible for the development of the new klystron are: **A. C. Grimm, F. G. Hammersand, A. T. Plihcik, D. R. Trout,** and **T. E. Yingst.**

[For other RCA work in this field, see: Musson, "High-Power RF Equipment for the Cambridge Electron Accelerator," RCA ENGINEER, Vol. 8, No. 1, June-July 1961.]

REGISTERED PROFESSIONAL ENGINEERS

J. F. Dienst, RCA Labs., PE-12599, N. J.
W. S. Erbe, DEP-MM&SR, PE-12578, N. J.
N. U. Huffmaster, AED-DEP, EIT-10648-E, Mo.
H. K. MacKechnie, DEP, PE-495, Mass. & Ohio
W. H. Miller, ME-8955, Calif.
D. P. Pushner, DEP, PE-12593, N. J.
C. C. Reiff, B&C, PE-19198, Ohio and PE-3014E, Pa.
H. T. Schneider, DEP, PE-38632, N. Y.
H. L. Schwartzberg, AED-DEP, 4532-E, Pa.
B. P. Silverman, EDP, EE-5168, Calif.
G. D. Smoliar, EDP, PE-8722, Pa.
E. J. Williamson, RCAC-N. Y., PE-12575, N. J.
K. O. Frawley, BCPP, PE-9084E, Pa.
M. M. Gerber, SurfCom, PE-12750, N. J.

. . . PROMOTIONS . . .

to Engineering Leader & Manager

As reported by your Personnel Activity during the past two months. Location and new supervisor appear in parenthesis.

RCA Service Company

R. M. Corbin: from Engr., BMEWS, to *Ldr., Engineers,* BMEWS (W. M. Stobbe, Mgr., Site I—Technical)

L. L. Throop: from Engr., BMEWS, to *Ldr., Engineers,* BMEWS (W. M. Stobbe, Mgr., Site I—Technical)

R. J. Wakefield: from Engr., Elec. BMEWS to *Ldr., Engineers,* BMEWS (K. R. Lewis, Mgr., Site I—Support)

Electronic Data Processing

J. P. Brennan, Jr.: from Engr., to *Ldr., D&D* (R. A. Alexander, EDP Eng. Ldr., D&D)

Semiconductor and Materials Div.

G. S. Lozier: from Eng. Ldr., Prod. Dev., to *Mgr. Electrochem. Systems* (B. V. Dale, Mgr., Somerville)

G. Levy: from Engr. Prod. Devel. to *Eng. Ldr., Mfg.* (M. Geller, Mgr., Somerville)

R. Pinto: from Eng. Ldr., Prod. Dev., to *Mgr., Minuteman Project 404M* (P. Valentine, Mgr., Somerville)

J. W. Ritcey: from Adm., Prod. Evaluation to *Mgr., Mfg. & Prod. Eng.* (N. H. Green, Mgr., Comm. Semiconductor Prods. Dept., Findlay)

F. L. Wildes: from Mgr., Prod. Eng. to *Mgr., Type Eng.* (R. J. Hall, Mgr., Findlay Plant)

Electron Tube Division

R. A. Alleman: from Engr., Equip. Dev. to *Eng. Ldr., Equip. Dev.* (Mgr., Process Advanced Dev., Lancaster)

F. G. Block: from Eng. Ldr., Prod. Dev. to *Mgr., Thermionic Converter Eng.* (Mgr., Super Power Tube & Space Components Eng.—Lancaster)

R. W. Engstrom: from Mgr., Photo & Image Tube Eng. to *Mgr., Advanced Dev. Engrg.-Conversion Tube* (Mgr., Conversion Tube Operations—Lancaster)

J. E. Fagan: from Engr., Mfg. to *Mgr., Quality Testing & Purchased Tube Control* (A. N. Brooks, Mgr., Plant Quality Control, Marion)

J. M. Forman: from Eng. Ldr., Prod. Dev. to *Mgr., Environmental & Special Equip. Design Eng.* (Mgr., Life Test & Data, Lancaster)

A. C. Grimm: from Eng. Ldr., Prod. Dev. to *Mgr., Super Power Tube Design & Dev.* (Mgr., Super Power Tube & Space Components Eng.—Lancaster)

M. D. Harsh: from Eng. Ldr., Prod. Dev. to *Mgr., Prod. Eng.* (Mgr., Display Tube Operations, Lancaster)

A. L. Morehead: from Assoc. Engr., Prod. Dev. to *Mgr., Prod. Eng.* (Mgr., Photo & Image Tube Operations, Lancaster)

A. G. Nekut: from Eng. Ldr., Prod. Dev., to *Mgr., Prod. Eng.* (Mgr., Photo & Image Tube Operations, Lancaster)

B. Sheren: from Eng., Mfg. to *Mgr., Prod. Eng.* (Mgr., Power Tube Mfg., Lancaster)

P. D. Strubhar: from Eng. Ldr., Prod. Dev. to *Mgr., Chemical & Phys. Services* (Mgr., Chemical & Physical Lab., Lancaster)

T. E. Yingst, Jr.: from Eng. Ldr., Prod. Dev. to *Mgr., Super Power Tube Application & Equip. Eng.* (Mgr., Super Power Tube & Space Components Eng., Lancaster)

Missile and Surface Radar Division, DEP

D. W. Beal: from Mgr., System Proj. to *Mgr., Field Operations & Product Support* (J. J. Guidi, Moorestown)

F. Gardiner: from Mgr., Space Sys. Development to *Mgr., Engineering* (A. Mason, Moorestown)

D. D. Keys: from Engr. to *Ldr., E.S.P.* (L. T. Carapellotti, Moorestown)

D. C. McCarthy: from Ldr., Sys. Engrg. to *Mgr., Intelligence & Data Analysis* (H. W. Collar, Moorestown)

J. L. Nolan: from Engr. to *Ldr., Sys. Engrg., Experimental Programs* (R. Ekis, Moorestown)

W. T. Patton: from Engr. to *Ldr., D&D Antenna Research* (R. C. Spencer, Moorestown)

O. M. Woodward: from Engr. to *Ldr., D&D Antenna Research* (R. C. Spencer, Moorestown)

D. V. Wylde: from Engr. to *Ldr., Sys. Engrg. Weapons Sys. Analysis* (R. Cheetham, Moorestown)

Astro-Electronics Division, DEP

J. E. Dilley: from Ldr., Engrs. to *Mgr., Special Camera Systems* (J. Lehmann, Mgr., Space Observation Systems, Princeton)

A. Garfinkel: from Sr. Engr. to *Ldr., Engrs.* (J. Lehmann, Mgr., Space Observation Systems)

J. J. Newman: from Sr. Engr. to *Mgr., OGO Equipment Operations* (C. S. Constantino, Mgr., Equip. Projects)

Surface Communications Division, DEP

R. Larson: from Sr. Member Technical Staff to *Ldr., Design & Dev. Engr.* (P. J. Riley, Cambridge)

N. B. Zartman: from Sr. Member Technical Staff to *Ldr., Design & Dev. Engrs.* (Dr. N. H. Crooks, Cambridge)

Aerospace Communications and Controls Division, DEP

J. D. Aronson: from Chief Engr. (706P) to *Mgr., 706 Program* (D. C. Arnold, Burlington)

S. J. Brzeski: from Sr. Project Mbr., T.S. to *Ldr., T.S.* (T. Andreopoulos, Burlington)

W. X. Johnson: from Sr. Project Mbr., T.S. to *Ldr., T.S.* (A. M. Schneider, Burlington)

F. F. Martin: from Mgr., Project Operations (POSS) to *Mgr., POSS Program* (D. C. Arnold, Burlington)

P. E. Seeley: from Mgr., Electro-Optical Sys. to *Mgr., Advanced Sys. & Techniques* (H. J. Woll, Burlington)

Data Systems Division, DEP

C. Batsel: from Sr. Member D&D Engr. Staff to *Ldr., D&D Engr. Staff* (J. Cornell, Mgr., Van Nuys)

E. Bingo: from Principal Mbr., Eng. Staff to *Staff Eng. Scientist, Digital Circuits* (E. L. Byrne, Mgr., Van Nuys)

G. Canova: from Prin. Mbr., Proj. Engr. Staff to *Ldr., D&D Engr. Staff* (J. J. Murphy, Van Nuys)

G. Cassidy: from Ldr., Proj. Engrg. Staff to *Mgr., Systems Projects, Saturn Projects* (W. M. McCord, Van Nuys)

W. J. Davis: from Prin. Mbr., D&D Engr. Staff to *Staff Engr. Scientist* (L. Seeberger, Van Nuys)

A. Ess: from Prin. Mbr. D&D Engr. Staff to *Staff Engr. Scientist* (J. Murphy, Van Nuys)

E. Griffith: from Mbr., Engr. Staff to *Ldr., Systems Engr. Staff* (G. Murphy, Van Nuys)

B. E. Kempf: from Sr. Mbr. D&D Engr. Staff to *Ldr., Systems Engr. Staff* (E. Byrne, Van Nuys)

L. Perkins: from Sr. Mbr., D&D Engr. Staff to *Ldr., D&D Engr. Staff* (J. Wight, Acting Mgr., Van Nuys)

ANDERSON NAMED MGR., OPERATIONS; KIRKWOOD NAMED CHIEF ENGINEER FOR HOME INSTRUMENTS

Earl I. Anderson has been appointed Manager, Operations, of the RCA Victor Home Instruments Division, Indianapolis. **Loren R. Kirkwood** succeeds Mr. Anderson as Chief Engineer. In his new post, Mr. Anderson will be responsible for the Manufacturing, Materials, and Engineering Departments, and will report to **Delbert L. Mills,** Vice President and General Manager of the Division. The Finance and Personnel activities will continue to report directly to Mr. Mills.

Mr. Anderson, who joined RCA in 1937 as an engineer, has been Chief Engineer since 1959. He also served previously as Chief Engineer of the Communications Department of the former RCA Industrial Electronics Division and as Engineer in Charge of the Industry Service Laboratory in New York City. An IRE Fellow, he holds 30 patents in the radio-television field.

Mr. Kirkwood, who started with RCA in 1930 as a student engineer, was Manager, TV Product Engineering, before being named Chief Engineer. For many years he had been responsible for the color TV receiver development and design engineering for RCA Victor Home Instruments.

DR. WOLL NAMED CHIEF ENGINEER, DEP-ACCD; D. J. PARKER NAMED MGR., DEP APPLIED RESEARCH; ACCD HEADQUARTERS MOVE TO BURLINGTON

Dr. H. J. Woll has been named Chief Engineer of ACCD, as announced recently by **I. K. Kessler,** Division Vice President and General Manager. Dr. Woll had been Manager, DEP Applied Research, in Camden. In connection with this charge, **D. J. Parker** has been named Manager, Applied Research, succeeding Dr. Woll. Mr. Parker will report to **Dr. H. J. Watters,** Chief Defense Engineer for DEP.

The DEP-ACCD Burlington, Mass., plant has been named as ACCD headquarters, which was formerly in Camden. (ACCD work is carried on in both Burlington and Camden.)

D. Y. SMITH HEADS ETD AND SCM

On February 15, 1963, **D. Y. Smith** was appointed to the newly created position of Vice President and General Manager, Electronic Components and Devices. In this capacity, Mr. Smith will be responsible for the management and direction of the RCA Electron Tube Division and the RCA Semiconductor and Materials Division. Mr. Smith will continue as Vice President and General Manager of the RCA Electron Tube Division. **Dr. A. M. Glover,** Vice President and General Manager of the RCA Semiconductor and Materials Division, will report to Mr. Smith. Mr. Smith will report to **W. W. Watts,** Group Executive Vice President, RCA.

RCA APPLIES FOR STOCK IN SATELLITE CORPORATION

RCA Communications, Inc. has applied to the FCC for authorization to purchase stock in the Communications Satellite Corporation. The application was made in accordance with FCC rules and the Communications Satellite Act of 1962. RCA Communications expects to provide international services via satellite systems when they become available.

STAFF ANNOUNCEMENTS

Product Engineering (Staff), Camden: **S. H. Watson,** Mgr., Standardizing, has named **M. A. Savrin** as Administrator, Industrial Finishes Standards.

Broadcast and Communications Products Division, Camden: **C. M. Odorizzi,** Group Executive Vice President, has announced that the Broadcast and Communications Products Divsion has assumed responsibility for the engineering and marketing of Mobile Communications, Radiomarine, and Audio-Visual products.

C. H. Colledge, Division Vice President and General Manager, Broadcast and Communications Division, has announced that **A. F. Inglis** has been named Division Vice President, Communications Products Operations, reporting to Mr. Colledge. Mr. Inglis has assumed responsibility for Mobile Communications, Radiomarine, and Audio-Visual products. In addition, Mr. Inglis will retain responsibility for the engineering and merchandising of Broadcast transmitter and antenna products.

Mr. Inglis announces the organization of Communications Products Operations as: **R. N. Baggs,** Mgr., Radiomarine Marketing; **W. F. Covert,** Mgr., Meadow Lands Purchasing; **A. Fischer,** Mgr., Mobile Communications Marketing; **W. R. Griswold,** Mgr., Meadow Lands Personnel; **N. C. Colby,** Mgr., Communications Products Engineering; **E. N. Luddy,** Mgr., Broadcast Transmitting Equipment Merchandising; **C. W. Michaels,** Mgr., Planning and Market Research; **A. J. Platt,** Mgr., Audio-Visual Marketing; **R. E. Small,** Mgr., Financial Operations, Meadow Lands; **R. E. Wilson,** Plant Manager, Meadow Lands Plant; and **J. E. Young,** Mgr., Broadcast Transmitting Equipment Engineering.

M. A. Trainer has been named Mgr., Broadcast Studio Merchandising and Engineering Department, reporting to Mr. Colledge. In addition, Mr. Trainer will be responsible for liaison between RCA International Division and the Broadcast and Communications Products Division. Mr. Trainer names his staff as: **F. J. Herrman,** Mgr., Scientific Instruments and ITV Merchandising; **A. H. Lind,** Mgr., Studio Recording and Scientific Equipment Engineering; **A. M. Miller,** Mgr., Film Recording and West Coast Operations; and **W. B. Varnum,** Mgr., Studio Equipment Merchandising.

Defense Electronic Products: **W. G. Bain,** Vice President, DEP announces that Aviation Equipment Department will be established as an autonomous operation reporting to **S. N. Lev,** Division Vice President, Defense Manufacturing and Program Management. This operation will be located in the West Los Angeles plant, and **J. R. Shirley** will be Mgr., Aviation Equipment, reporting to Mr. Lev.

SZUKALSKI CHAIRS COMMITTEE ON PRINTED BOARDS

The Institute of Printed Circuits, Inc. (IPC) is concerned with studies and projects to further the development of the printed-circuit industry. RCA joined this organization in 1962. **E. A. Szukalski,** DEP Central Engineering, was recently named Chairman of a "Multi-Layer Wiring Board Committee," with the objective of establishing criteria for reliable multi-layer wiring board designs that reflect the capability of the printed-circuit industry and are compatible with the needs of the electronics industry. —*J. J. Lamb*

PROFESSIONAL ACTIVITIES

DEP-SurfCom, Cambridge, O.: The Cambridge Subsections of the IEEE joined five other societies in promotion of *National Engineer's Week* recently. **R. Luethy** was Toastmaster of the banquet celebrating these activities, and **P. J. Riley** was one of the speakers. **W. L. Pattison** was recently given three awards by the Cambridge Jaycee's for his outstanding contributions during 1962.—*P. J. Riley*

DEP-SurfCom, Camden: **S. W. Cochran,** Vice President and General Manager, SurfCom, was Chairman of Session 54 on "Advanced Techniques for Product Engineering" at the 1963 IEEE International Convention in New York. On Feb. 19, 1963, **C. W. Fields** served as Co-Chairman of a joint PTGEWS-PTGEM meeting in Philadelphia attended by 41 (17 from RCA), at which **A. H. Coleman,** SurfCom, and **W. J. Underwood,** M & S R, conducted an open-panel discussion on the problems of communications in an engineering organization. Interest in the subject runs high, as evidenced by the especially active audience participation in the discussion. — *C. W. Fields*

DEP-ACCD, Burlington: **A. R. Pelletier** was Chairman of the session on Acoustics at the Technical Meeting and Exposition of the Institute of Environmental Science in Los Angeles, Calif. on April 17-19, 1963. He also lectured on "An Introduction to Basic Acoustic Fundamentals as Applied to Acoustic Testing in the Laboratory."

Home Instruments, Indianapolis: The RCA Indianapolis plant is sponsoring an Explorer Scout Post whose specialty is electronics; four RCA engineering leaders are the advisors for the Post. In April, the Home Instruments Division was host to the Central Indiana IEEE Section for a tour of Plant Facilities.—*R. C. Graham*

DEP-SurfCom, New York: **Berthold Sheffield** was Chairman of the *Eta Kappa Nu* Eminent Member Induction Luncheon for MIT's Dean Gordon S. Brown on March 25, 1963. Mr. Sheffield was also Acting Chairman at an IEEE Meeting (NNJ) on April 16 which featured **E. D. Becken,** Vice President and Chief Engineer of RCA Communications, Inc., as speaker. **C. Paramithas** recently spoke on "The Design and Evaluation of an Inductive-Type Parametron Device" at the DEP Astro Electronics Division.—*M. Rosenthal*

Missile Test Project, RCA Service Co., Patrick AFB, Fla.: Some 850 persons from industry and government attended a Flight Testing Conference of the AIAA at Cocoa Beach. Four RCA papers were involved in the program (to be listed in *Pen and Podium*) and **D. Hill** was Vice Chairman of the March 19 Session.—*M. W. Tilden*

DEP Staff, Camden: **F. D. Whitmore** spoke to 200 members of the Delaware Valley Chapter of Broadcast Pioneers on "Philadelphia's Early Radio Days" on April 16. Highlight was an interesting brochure that he prepared and distributed, made up of news clippings dating back to 1922 that traced the development of local area radio.

DEP Data System Division, Van Nuys: On March 27, **F. A. Fagan** attended a PERT Orientation Course for Industry at the PERT Training Center at Bolling AFB, Washington, D.C., a newly established intergovernment facility to indoctrinate management of government and industry in advanced techniques for program management. **R. Lending** has been named to the executive committee of the IEEE Professional Technical Group on Communications Systems for 1963.—*D. J. Oda*

DEP Data Systems Division, Bethesda, Md.: **V. Meara** is active on both the ASW Navigation Committee of the NSIA and the Radio Receiver's Committee of the IEEE. **J. Logan** recently became an Associate Member of the Operations Research Society of America and the Washington Operations Research Council.—*H. J. Carter*

ETD, Lancaster: **C. W. Weineke** has been named Chairman of the recently formed Task Force for industry specifications on sealing glasses. The Task Force is part of Subcommittee V-B, ASTM Committee F-1 on Materials for Electron Tubes and Semiconductor Devices.—*G. G. Thomas*

MAGEE HEADS AIA GROUP ON MILITARY EQUIPMENT SPECS

At its January meeting, the Electronic Equipment Specification Committee (EESC) of AIA elected **S. K. Magee,** DEP Central Engineering, Chairman for the year 1963. EESC has, as its principal charter, the development of the AIA position on all general and related specifications for electronic equipment and the coordination of the AIA Industry position with the Military Service. EESC receives its policy guidance from the AIA Electronic Equipment Technical Committee (EETC) which has broad cognizance over research, design, development, and operating safety of electronic equipments in systems for piloted aircraft, missiles, and space vehicles. Additional information on General Specification Uniformity is carried in Issue 55 of the "DEP Components and Materials Bulletin."—*J. J. Lamb*

GUENTHER NAMED CHIEF SCIENTIST, SURFCOM; METZGER HEADS SYSTEMS LAB

Dr. Richard Guenther has been named Chief Scientist, DEP Surface Communications Division, with division-wide responsibilities for research and development planning. **Sidney Metzger** has been named Manager of the SurfCom Systems Laboratory, New York. Both report to **O. B. Cunningham,** Chief Engineer, SurfCom.

Dr. Guenther joined RCA in 1956. Prior he was with Bell Telephone Laboratories, the Signal Corps and companies in Germany. He received MEE and PhD degrees from the Institute of Technology, Danzig, in 1934 and 1937 respectively. He is a member of the IEEE and American Association for the Advancement of Science, and serves on Study Group No. 2, CCIR National Committee.

Sidney Metzger joined SurfCom from the Astro-Electronics Division, where he was responsible for the communication engineering of a number of satellite projects, including SCORE, TIROS and RELAY. He joined RCA in 1954. Before that he was with ITT Laboratories and the Signal Corps Laboratory. He received the BSEE at New York University in 1937 and the MEE from Polytechnic Institute of Brooklyn, 1950, and is a *Fellow* of the IEEE, an *Associate Fellow* of the American Institute of Aeronautics and Astronautics, and Chairman of its Technical Committee on Communications.

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