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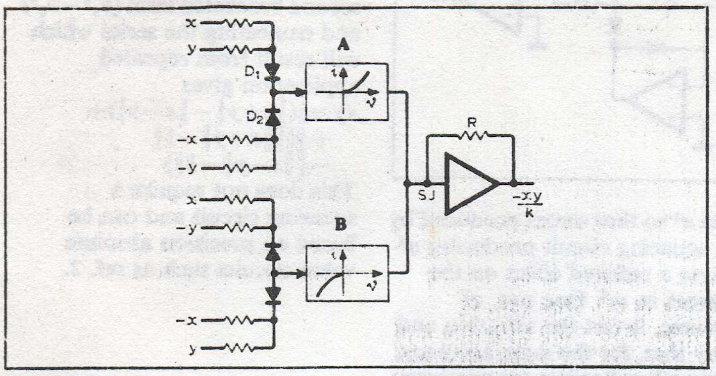
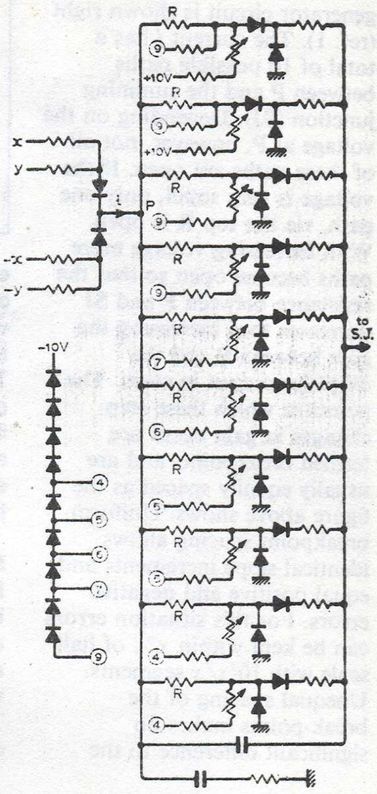
Set 29: Analogue multipliers—1

Quarter-squares multiplier



Description
Quarter square multipliers are found frequently in analogue/hybrid computers in which their high accuracy (0.05% of half scale) is required and their limited bandwidth (less than 10kHz) is no disadvantage. They implement the relationship $xy=\frac{1}{4}[(x+y)^2-(x-y)^2]$ i.e. multiplication based on a square law device—this is usually a diode function generator permanently set to provide a square law action. Such generators are usually single quadrant devices, e.g. A (above) requires a positive input and this necessitates the use of an absolute value circuit prior to it. If, for instance, $(x+y)$ is positive then D_1 conducts (and D_2 does not) and a positive voltage is applied to A. Likewise if $(x+y)$ is negative D_2 conducts (and D_1 does not) but again it is a positive voltage that is applied to A. Hence the output of A is proportional to $|(x+y)|^2$, which is the same as $(x+y)^2$. A similar argument applies to the other absolute value circuit, B; being a 3rd quadrant device, it produces a current proportional to $-(x-y)^2$.
The constant k appearing in the output expression depends on R and on the output characteristics of A and B. Generally, if the maximum value of X and Y is say P volts, then k is set to P.
If an absolute value circuit does not precede the squaring section then a total of four squaring sections are necessary. Despite the apparent increased complexity this is still sometimes done to avoid errors due to the diodes D_1 and D_2



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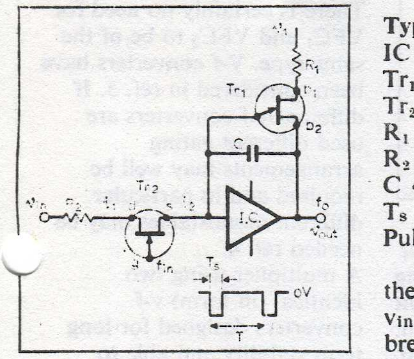
Set 29: Analogue multipliers—2

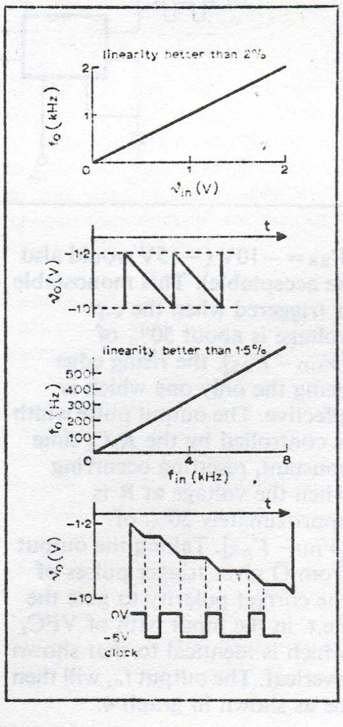
V-f converter multiplier



Circuit description
The circuit is a modification of the v-f converter described in ref. 1. The f.e.t. Tr_2 is the only addition. Graph 1 was obtained with f.e.t. permanently conducting, i.e. $V_{gs}=0 (f_{in}=0)$, and shows f_o to be proportional to v_{in}. This graph was obtained with v_1 set to 3.3V which setting gave an f_o of 2kHz with $v_{in}=2V$. Control of

Typical performance
IC 741, ±15V supplies
Tr_1 2N2646 u.j.t.
Tr_2 2N5486 f.e.t. (n-channel)
R_1 100Ω
R_2 1kΩ
C 47nF
T_s 100μs
Pulse height −5V

the relationship between f_o and v_{in} depends on the u.j.t. breakdown voltage and this is variable from device to device. The v-f conversion can be described as a conversion first from v_{in} to i_1 and secondly from i_1 to f_o. The greater i_1 the more rapidly does the capacitor charge and the more rapidly is the breakdown condition of the u.j.t. met. The downwards ramp of graph 2 shows this charging. On breakdown the u.j.t. shorts the capacitor so the output voltage



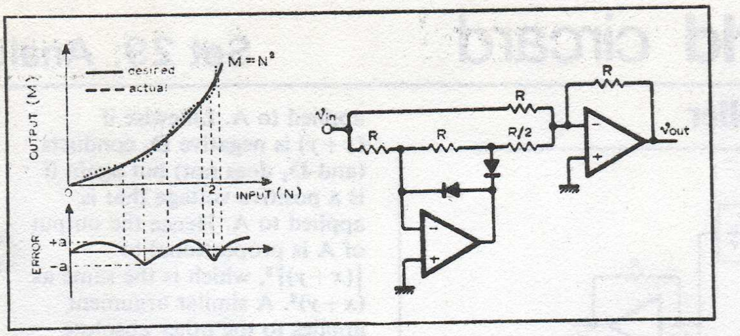
rises towards zero until the u.j.t. assumes its normal non-conducting role.
If now pulses are fed to the f.e.t. gate as shown, i_1 will become a train of current pulses i_2. f_o then depends on i_2.

$$f_o=k\,i_2=k\,i_1\cdot\frac{T_s}{T}=k\frac{v_{in}}{R_2}T_s\cdot f_{in}$$
$$=K_1\,v_{in}\,f_{in}$$

Graph 3 shows that f_o is indeed proportional to f_{in}, the proportionality between f_o and v_{in} being shown in graph 1. The multiplying action is thus experimentally verified.
If f_{in} is derived from another v-f converter we have $f_{in}=k_2v'_{in}$ and then $f_o=k''\,v_{in}\cdot v'_{in}$ so that f_o is proportional to the product of two voltages.

Component changes. The value of R_2 quoted i.e. 1kΩ is the absolute minimum usable. R_2 should be much larger than the f.e.t. "on" resistance (≈200Ω). Max. $R_2\approx100$kΩ;

and to provide further functions.
An example of a square law generator circuit is shown right (ref. 1). The current i has a total of 10 possible paths between P and the summing junction (SJ). Depending on the voltage at P, however, not all of these paths are open. If the voltage is very small, only one path, via the top R is open. With increasing voltage more paths become open so that the resistance between P and SJ decreases thus increasing the gain between P and the amplifier output in steps. The points at which these step changes in gain occur are termed breakpoints and are usually equally spaced as the figure above shows. Uniform breakpoint spacing allows identical slope increments and equal positive and negative errors. For this situation errors can be kept within x% of half scale with $10/\sqrt{x}$ segments. Unequal spacing of the break-points makes no significant difference to the



overall accuracy although it is common to have one or two extra breakpoints near zero for improved accuracy.
The use of the diode string to provide some of the biasing functions provides temperature compensation as well. The capacitors shown increase the frequency response.

Related circuits
If bandwidth is not essential but increased accuracy is, then use can be made of the relationship $m^2=\frac{1}{4}(1+2u+u^2)$ where $u=2|m|-1$.
The right hand side of this equation is not totally dependent on u^2 so that errors produced by a squaring circuit producing u^2 have a reduced effect on the errors in m^2. One can, of course, invert the situation and say that, for the same accuracy, fewer breakpoints are necessary and a less expensive squarer is produced. A "card" mechanising the right hand side of the equation is simply inserted as the A card in the circuit overleaf and with minor modifications a B card is produced.
If we now examine

$$xy=\frac{x+y^2}{2}-\frac{x-y^2}{2}=m_1{}^2-m_2{}^2$$

and apply the above equation for m we obtain

$$xy=\tfrac{1}{4}[2(u_1-u_2)+(u_1{}^2-u_2{}^2)]$$
$$=\tfrac{1}{2}(|x+y|-|x-y|)+\tfrac{1}{4}(u_1{}^2-u_2{}^2)$$

Reapplying the formula on the second bracketed term $(u_1{}^2-u_2{}^2)$ and truncating the series which will result from repeated application gives

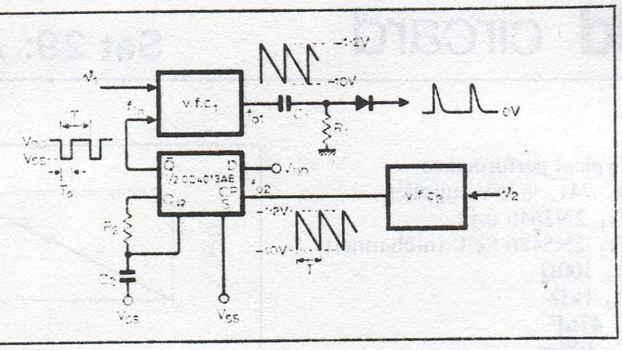
$$xy\approx\tfrac{1}{2}(|x+y|-|x-y|)+ +\tfrac{1}{4}\{||x+y|-1| -||x-y|-1|\}$$

This does not require a squaring circuit and can be based on precision absolute value circuits such as ref. 2.

References
1. Whigham, R. H. Fast 10-V quarter-square multiplier. Simulation 1965.
2. Set 4, card 3.
Korn and Korn. Electronic Analog and Hybrid Computers, 2nd edition, McGraw-Hill.

beyond this op-amp input currents become considerable. The value of C is related to that for R_2 as the ramp slope is $1/R_2C$. With C=4.7nF (and T_S=10μs) we achieved a maximum f_o of 10kHz. Higher values of f_o are difficult to achieve because of charge-storage effects in the u.j.t. affecting the discharge time. Pulse height must be sufficient to cause pinch-off of f.e.t. but not so high as to cause breakdown. −1 to −10V with this device was satisfactory.

Circuit modifications
The circuit above shows a complete circuit whose output frequency, f_{o1}, is proportional to the product of the voltages v_1 and v_2. The second voltage to frequency converter, VFC_2, is assumed to be identical to that shown in the main diagram overleaf with the omission of the f.e.t. gate; it will therefore produce an output as shown in graph 2. This output is fed to the c.m.o.s. monostable shown (ref. 2) in which V_{DD}=0V and



V_{SS}=−10V (−15V would also be acceptable). This monostable is triggered when the c.p. voltage is about 50% of $[V_{DD}-V_{SS}]$, the rising edge being the only one which is effective. The output pulse width is controlled by the R_2C_2 time constant, resetting occurring when the voltage at R is approximately 50% of $[V_{DD}-V_{SS}]$. Taking the output from $\bar{Q}$ gives trigger pulses of the correct polarity to gate the f.e.t. in the input path of VFC_1 which is identical to that shown overleaf. The output f_{o1} will then be as shown in graph 4.
The network comprising C_1, R_1 and D_1 is simply a differentiating network to produce a somewhat more normal type of pulse train. Note that f_{in} is equal to f_{o2} and that f_{o1} must be less than f_{in}.
In fact consideration of the operation of the system overleaf shows that f_{in} should be of the order of ten times the desired f_{o1}. Hence VFC_2 must operate at a much higher frequency than VFC_1 and consequently the input resistors and feedback capacitors will be different. Voltages v_1 and v_2 also affect the frequencies of operation. As the maximum frequency attainable from a unijunction type of v-f converter is of the order of 10kHz it may be necessary to use different types for a particular application. There is certainly no need for VFC_1 and VFC_2 to be of the same type. V-f converters have been considered in ref. 3. If different v-f converters are used different gating arrangements may well be required and in particular different monostables may be needed ref. 4.
A multiplier using two identical (in form) v-f converters designed for long term stability and able to accommodate floating inputs is described in detail in ref. 5.

Related circuits
Set 21, V-f converters, card 1
Set 19, Monostables, card 8
Set 21, V-f converters
Set 19, Monostables
Versatile integrator-multiplier, E. Ljung and S. Berglund, *Electronic Engineering*, Aug. 1974, pp. 38-40.

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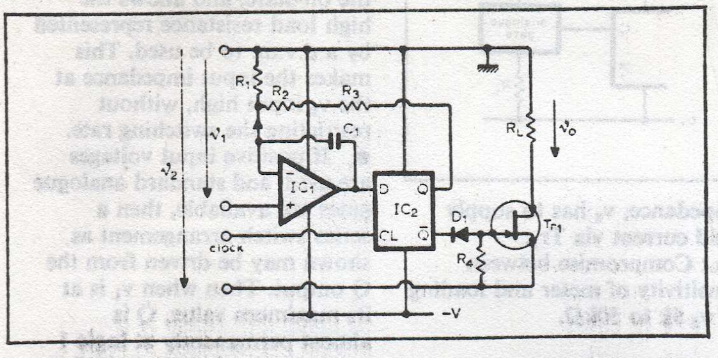
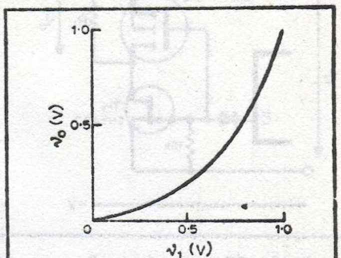
Set 29: Analogue multipliers—3

Delta-sigma modulator/multiplier



Typical performance
IC_1 N574N (Signetics)
IC_2 ½CD4013
D_1 1N4148
Tr_1 2N5457
R_1 4.7kΩ
R_2 100kΩ pot.
R_3 100kΩ
R_4 15kΩ
R_L 15kΩ
Supply −10V
v_1, v_2 0→ −1V
v_o 0→ −1V
$|v_o|=v_1v_2$



Circuit description
If an output waveform has a constant pulse height and width but the pulse-rate is proportional to an input voltage, then the mean value of the output is also proportional to that voltage. If the pulse height is made proportional to a second voltage the mean output becomes proportional to the product of the two voltages. A delta-sigma modulator converts a pulse-train into one with a smaller number of pulses, using an integrator to control the voltage on the D input of a flip-flop. As the mean voltage at the inverting and non-inverting inputs are the same and the mean current in the capacitor is zero, the fraction of the time for which Q is high is controlled by the input voltage v_1. The circuit configuration has a negative input voltage and supply because it was desired to use the simplest arrangement, and certain op-amps (e.g. Signetics 741) have an input common-mode range that includes the positive supply rail. The circuit can be adapted for any other op-amp by providing a separate positive bias. With dual supplies the system may equally be used with positive inputs and outputs if the flip-flop is powered from the positive rail.

The $\bar{Q}$ output is used to gate a junction f.e.t. on and off. With $\bar{Q}$ high (zero volts), the diode is non-conducting and R_4 establishes zero gate-source bias. With $\bar{Q}$ low ($-V$) the f.e.t. is off. This is true provided the second input voltage v_2 is small so that the reverse gate-source voltage is in excess of the pinch-off voltage. The load receives voltage pulses of duration equal to the inter pulse period and just less than v_2 in

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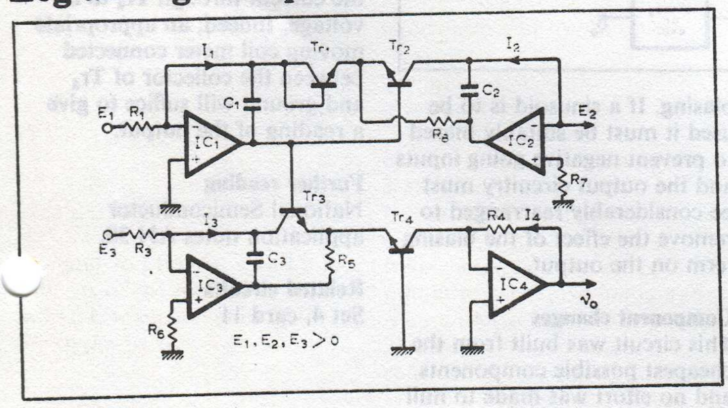
Set 29: Analogue multipliers—4

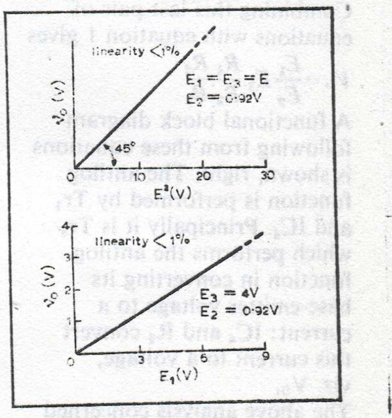
Log-antilog multiplier



Components
IC_{1-4} 741 (e.g. RC4136 quad package)
Tr_1 to Tr_4 1/5 CA3086
R_1, R_2, R_3, R_6, R_7 100kΩ
R_4 10kΩ, R_5 2.2kΩ
C_1 300pF, C_2 200pF
C_3 22pF
All passive components ±5%
Supply voltage ±7.5V

Performance
It can be shown (see text) that $v_o=E_1E_3R_2R_4/E_2R_1R_3$. With the resistor values chosen, assuming perfect components, $v_o=E_1E_3/10E_2$ and so the circuit can be used as a squarer ($E_1=E_3$ and E_2 constant), as a multiplier (E_2 constant E_1 and E_3 variable), as a divider (E_2 as divisor E_1 or E_3 as dividend, the other fixed) or as a device for obtaining the reciprocal of E_2 (E_1 and E_3 fixed). Results as a squarer are shown in graph 1 from which it will be noted that E_2 was set at 0.92 rather than 1V to achieve the slope of 45° (making up for component inaccuracy) and that the maximum v_o obtainable is less than 4V. Saturation of the transistors occurs at higher voltages. Graph 2 shows similar linearity for operation as a multiplier, multiplying the variable E_1 by the constant E_3. Identical results were obtained when the roles of E_1 and E_3 were reversed. Similar linearity was obtained with the device operated as an arithmetic inverter (reciprocal).

Circuit description
Analysis of the circuit is as follows:



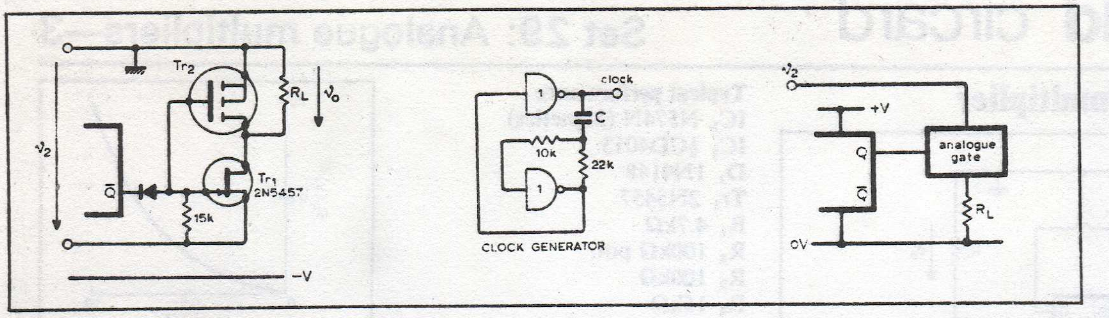
$I_1=E_1/R_1$ and $V_{be1}=\frac{kT}{q}\log_e i_1$

$i_2=E_2/R_2$ and $V_{be2}=\frac{kT}{q}\log_e i_2$

$V'=V_{be2}-V_{be1}=\frac{kT}{q}\log_e\frac{E_2R_1}{E_1R_2}$

$V_{be4}=-V'+V_{be3}=\frac{kT}{q}\log_e\frac{E_1E_3R_2}{E_2R_1R_3}$ (1)

as $V_{be3}=\frac{kT}{q}\log_e i_3$ and $i_3=E_3/R_3$



magnitude. The number of pulses in a given time is proportional to v_1. Hence the mean load voltage is $\propto v_1 v_2$. This can be read directly on a moving-coil meter, or filtered and fed to a d.v.m.

Component changes

IC_1: Any op-amp if supply requirements observed. Output is always close to the flip-flop threshold voltage i.e. does not approach either supply line. Supplies can be single-ended negative or positive depending on op-amp. Must be large enough to gate f.e.t. 6 to 15V.

Tr_1: Any n-channel junction f.e.t. with pinch-off below, say, 5V. Low on-resistance preferred.

D_1: General purpose switching diode.

IC_2: Any c.m.o.s. D-type flip-flop (set and reset grounded).

R_1, R_2, R_3: Ratio sets 'gain' i.e. usual potential divider relationship defines ratio of mean output at Q to v_1. Total resistance 10k to 10MΩ. Suggested ratios 5:1 to 20:1.

R_4: If too high, results in slow switching of f.e.t. from off-on state with reduced overall accuracy. If too low, additional current places unwanted extra load on v_2 source.

v_1, v_2: Typically $0 \rightarrow -1$V. v_1 feeds into very high impedance, v_2 has to supply load current via Tr_1.

R_L: Compromise between sensitivity of meter and loading of v_2 5k to 50kΩ.

Circuit modifications

- To improve switching times without adding an extra i.c., it is possible to use a p.m.o.s. transistor from a CD4007 package. If the remainder of the package is connected as in the circuit shown, a clock generator results. Frequencies from 10kHz to >100kHz have been tested with this system. In general clock rates of several MHz are feasible but would make heavy demands on the analogue switches. The p.m.o.s. device prevents charge storage across the load resistance in the off-state, and allows the high load resistance represented by a d.v.m. to be used. This makes the input impedance at the v_2 input high, without restricting the switching rate.
- If positive input voltages are used, and standard analogue gates are available, then a series switch arrangement as shown may be driven from the Q output. Then when v_1 is at its maximum value, Q is almost permanently at logic 1 and v_2 is gated through to the load for almost 100% of the time. A shunt gate driven from $\bar{Q}$ completes the configuration for higher switching speeds or where R_L is to be raised.
- In principle this can be interpreted as a combined V_1-f and V_2-amplitude converter system.

Related circuits

Set 15, card 9

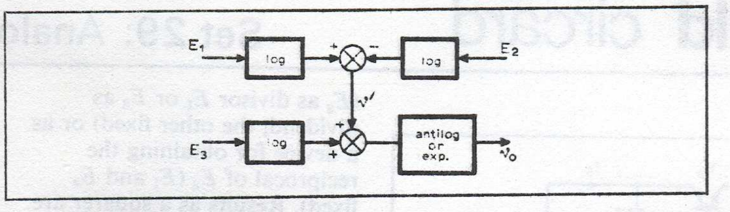
But $\log_e i_4 = qV_{be4}/kT$ and $I_4 = V_o/R_4$

Combining this last pair of equations with equation 1 gives

$$V_o = \frac{E_1}{E_2} E_3 . \frac{R_4}{R_3} \frac{R_2}{R_1}$$

A functional block diagram following from these equations is shown, right. The antilog function is performed by Tr_4 and IC_4. Principally it is Tr_4 which performs the antilog function in converting its base-emitter voltage to a current: IC_4 and R_4 convert this current to a voltage, viz. V_o.

The above analysis concerned d.c. conditions only, so all capacitors were ignored. Likewise R_5 and R_8 were ignored. The function of all of these components is to stabilize the loops in which they are contained. To see this, consider the simplest case viz. IC_3 and its associated circuitry. The loop gain of this circuit is the open-loop gain of IC_3 together with the gain of Tr_3 which is in common base mode and has a voltage gain given



approximately by $g_m \times$ the load on Tr_3. The load on Tr_3 is R_3 (by superposition the E_3 input end of R_3 is at ground). This voltage gain $g_m R_3$ is large and the overall loop gain is, therefore, considerably enhanced and instability is a considerable problem. The inclusion of R_5 reduces the feedback path gain as only a portion of the i.c. output voltage is applied to the base-emitter junction. For high frequency effects C_3 completely shorts out this feedback path amplifier, again improving stability. Note that g_m depends on the operating conditions i.e., in this case, on E_3 so that the problem is complex indeed. Note that all the input voltages must be positive to maintain correct transistor biasing. If a sinusoid is to be used it must be suitably biased to prevent negative going inputs and the output circuitry must be considerably rearranged to remove the effect of the biasing term on the output.

Component changes

This circuit was built from the cheapest possible components and no effort was made to null the i.cs. Considerable improvement in accuracy is obtainable if the resistors $R_1R_2R_3$ and R_4 are chosen to a much tighter tolerance. Nulling of i.cs will improve performance as will the use of i.cs with facility for feedforward compensation e.g. LM301 etc. The use of i.cs with very low input currents e.g. LM108 or f.e.t. input i.cs such as CA3130 will improve the lower end of the input range. These comments do not apply strictly to IC_4 which simply converts the current through Tr_4 to a voltage. Indeed, an appropriate moving coil meter connected between the collector of Tr_4 and ground will suffice to give a reading of the output.

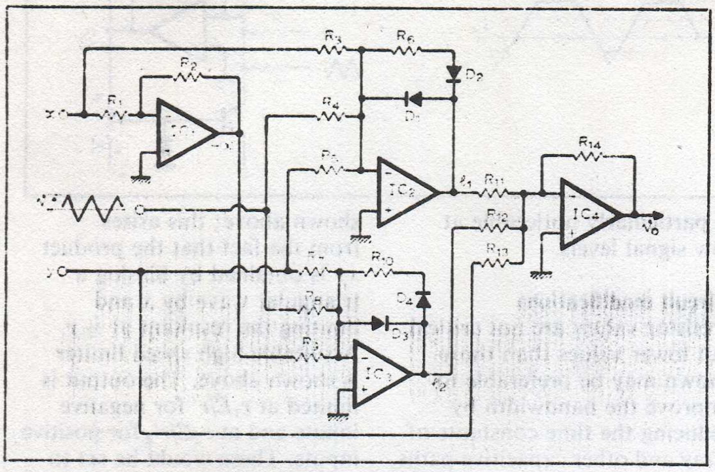
Further reading

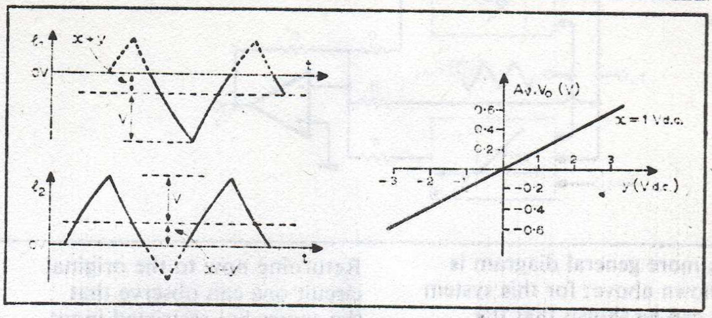
National Semiconductor application notes AN-30.

Related circuits

Set 4, card 11

Triangle-wave averaging multiplier



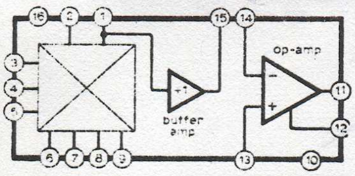


Components
R_1 to R_{14} 120kΩ
IC_1 741
D_1 PS101
pplies ±15V

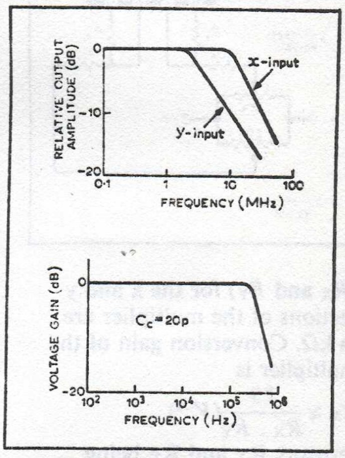
Performance
With v set at 4V and the frequency of the triangular waveform set at 1kHz graphs 1 and 2 were obtained. Linearity shown in graph 2 is better than 1%. Note that x and y are direct voltages and v_o is the average voltage at the output of IC_4. v_o is, of course, the inverted sum of e_1, e_2 and y. With x and y both at 1V and varying the frequency of the triangular wave the output accuracy was maintained within 1% up to 6kHz. The device is a 4-quadrant multiplier.

Description
The block comprising IC_2, R_3, R_4, R_5, R_6, D_1 and D_2 is a precision half-wave rectifier producing a negative output equal in magnitude to the sum of the input voltages when that sum is positive. The block producing e_2 can likewise be described. The sum of e_2, e_1 and y produces the output and at first sight the multiplier appears related to time-division (a.m./p.w.m.) multipliers. Analysis shows however that this multiplier is more closely related to the quarter-square multiplier, the reason being that the height of e_2 is closely related to the base of hatched triangle in graph 1 so that the area of the triangle becomes a square function.

Four-quadrant multiplier—characteristics



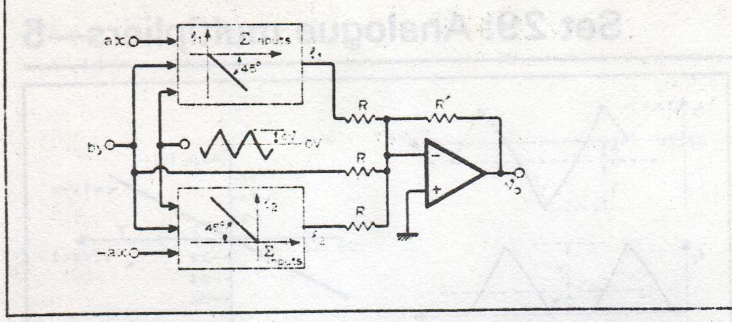
Pin designation
2 multiplier outputs
x input 4 common
5 y input 6 and 7 y gain
8 and 9 x gain
10 negative supply
11 op-amp output
12 compensation
13 non-inverting op-amp input
14 inverting op-amp input
15 high-frequency output
16 positive supply

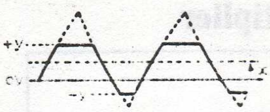


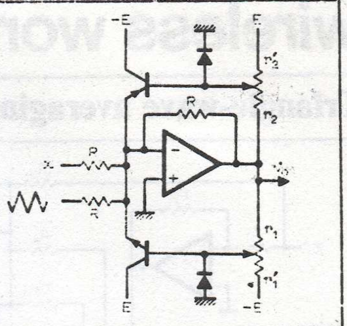
Description
The XR-2208/2308 is an op-amp combining a four-quadrant analogue multiplier, a high-frequency buffer amplifier and a differential-input op-amp on the same monolithic integrated circuit. The package is suitable for arithmetic operations and communication signal processing, maximum versatility being achieved by internally separating the amplifier and the multiplier-buffer section; suitable interconnections being made externally with passive components. The op-amp can be used as a post-detection amplifier in coherent detector applications or as a preamplifier for low-level input signals. The output from the buffer amplifier can be used for high-frequency signal processing, the multiplier-buffer section having a small-signal 3dB bandwidth of 8MHz and a transconductance bandwidth of 100MHz. The package can be operated from symmetrical supply rails in the range ±4.5 to ±16V. Very good power supply rejection and temperature stability are achieved by internally-regulating current and voltage levels.
The multiplier inputs x and y are applied to pins 3 and 5 respectively, with pin 4 common—normally the reference or ground terminal. However, in some applications x and y inputs are strapped together and pin 4 used as an input terminal. The d.c. bias currents at pins 3 and 5 are typically 3µA and at pin 4 typically 6µA. The differential output voltage (v_o) between pins 1 and 2 is often connected directly to the op-amp (pins 13 and 14), the final output (v_z) being obtained from pin 11.

$$v_o \approx \frac{25}{R_X \cdot R_Y} v_X \ v_Y$$

where all voltages are in volts and the gain control resistances







A more general diagram is shown above: for this system it can be shown that the average value of V_0 is:

$-\frac{R}{R}$ (average of e_1 + average of $e_2 + by$)

$$= -\frac{R'}{R}\left[\frac{-1}{4cV}(cV+ax+by)^2 + \frac{1}{4cV}(cV+ax+by)^2+by\right]$$

If $R' = \alpha R$, then this expression simplifies to

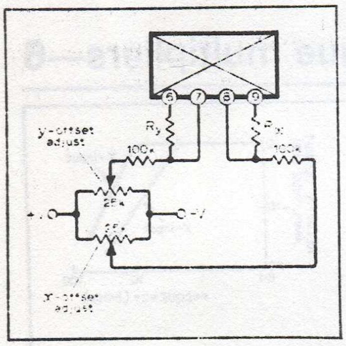
$$V_{0av} = \alpha\, xy\frac{ab}{cV}$$

Comparing this with the circuit overleaf we see that we have $\alpha = a = b = 1$ and $cV = 4$.

Returning now to the original circuit one can observe that the somewhat restricted input range is due to the fact that at no point should the bias voltage exceed the peak of the triangular wave. Clearly the input signal size can be increased by increasing the carrier magnitude and also by introducing factors a and b, reducing the effective input. The effect of these changes can be then cancelled by setting $R' = \alpha\, cV/ab$. The circuit is sensitive to d.c. components in the carrier and also to the carrier magnitude. The effect of a d.c. component is particularly noticeable at low signal levels.

Circuit modifications
Resistor values are not critical but lower values than those shown may be preferable to improve the bandwidth by reducing the time constants of stray and other capacitive paths. Resistor R′ may be replaced by a filter to remove the a.c. components of V_0. The d.c. impedance of such a filter should still equal R'. The system bandwidth can be increased by using a faster version of half-wave rectifiers[1].
● An alternative scheme is shown above; this arises from the fact that the product xy is obtained by biasing a triangular wave by x and limiting the resultant at $\pm y$. A suitable high speed limiter is shown above. The output is limited at r_1E/r' for negative inputs and at r_2E/r'_2 for positive inputs. These would be set to $\pm y$ respectively. Note that $r_1r_2 \ll R$ for good limiting.

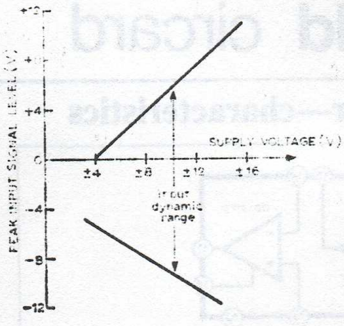
References
1. Set 22, card 3
2. Korn & Korn, Electronic Analog and Hybrid Computers, 2nd edition McGraw-Hill.



(R_X and R_Y) for the x and y sections of the multiplier are in kΩ. Conversion gain of the multiplier is

$$K_M \approx \frac{25}{R_X \cdot R_Y}(V^{-1})$$

resistors R_X and R_Y being connected as below; where the arrangement for adjusting the x and y offsets at pins 7 and 8 is also shown:
The operational amplifier is internally protected against short-circuit load conditions and can sink or source a current of 10mA into a resistive load. This amplifier can be compensated for unconditional stability by connecting a capacitor (C_C) of 20pF across pins 11 and 12. For higher voltage gains than unity, C_C is reduced to increase small-signal bandwidth and to improve slew-rate.
The unity-gain buffer amplifier if brought into use by connecting a resistor from pin 15 to ground and provides a low-impedance output for the multiplier section when the latter is used at high frequencies, in order to minimize capacitive loading of the multiplier output proper. The buffer output is not short-circuit protected and typically has a direct voltage of $V^+ - 4.5$ volts. The maximum direct current extracted from pin 15 should not exceed 10mA.
NOTE: When only the multiplier section or op-amp section is being used the input terminals of the unused section must be connected to ground.
The maximum peak x or y input signal that can be used for a given supply voltage without significant improvement

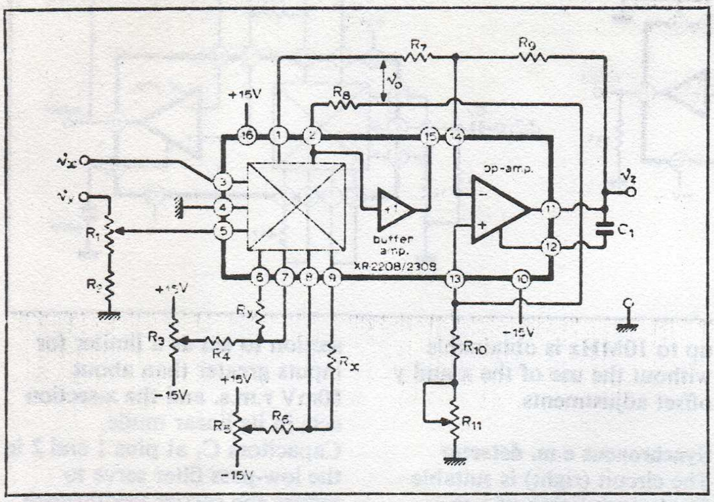


of the linearity of the multiplier is shown below.

Further reading
XR-2208/2308 Operational multiplier data sheet, EXAR, 1972.
XR-2208 Operational Multiplier, *New Electronics*, 1 April 1975, pp. 27-31.

Related circuits
Set 29, card 7

Four-quadrant multiplier—applications



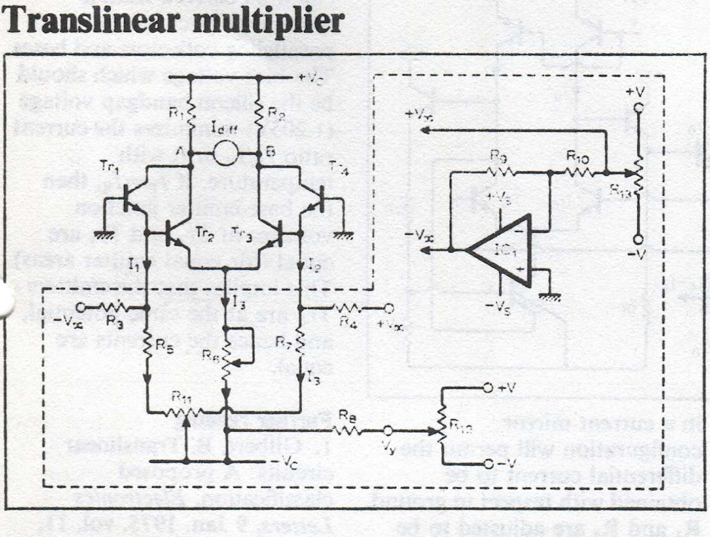
4-quadrant multiplier—applications
In most multiplication applications the operational amplifier and multiplier sections are interconnected as shown left providing a single-ended output signal and having a wide dynamic range. With the values shown below, the linear output swing is typically 10V for maximum input signals of 10V with a scale factor $K=0.1$.

Component values
Supplies ±15V
$V_{x(max)}$; $V_{y(max)}$ 10V
R_1, R_2 5kΩ
R_3, R_4, R_5, R_6, R_{11} 100kΩ
R_7, R_8 24kΩ, R_9 300kΩ
R_{10} 240kΩ, R_x 30kΩ
R_y 62kΩ, C_1 20pF
$V_z = V_x \cdot V_y/10$
R_1 scale factor
R_3 y-offset
R_5 x-offset
R_{11} output offset

Setting-up procedure
1. With 0V applied to both inputs and the output offset is adjusted to be 0V with R_{11}.
2. With a 20V pk-pk, 50Hz signal applied to the x-input and 0V to the y-input, R_3 is adjusted to provide minimum output voltage.
3. With a 20V pk-pk 50Hz signal applied to the y-input and 0V to the x-input, R_5 is adjusted to provide minimum output voltage.
4. Repeat step 1.
5. With +10V applied to both inputs, R_1 is adjusted to provide an output of +10V.
6. Step 5 may be repeated with different input voltages and different polarities to obtain best accuracy either over the whole input range or over some specific part of it.

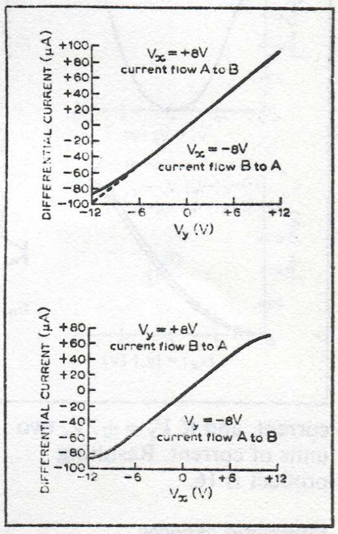
Squaring circuit
As shown over, the circuit used for squaring is essentially that used for multiplication except that the input signal is applied simultaneously to the x and y input terminals and only one input offset adjustment is required.
Adjustment procedure is:
1. With 0V applied to the input the output offset is adjusted to be 0V using R_{11}.
2. With +1V applied to the input R_3 is adjusted to make v_o 0.1V.
3. With +10V applied to the

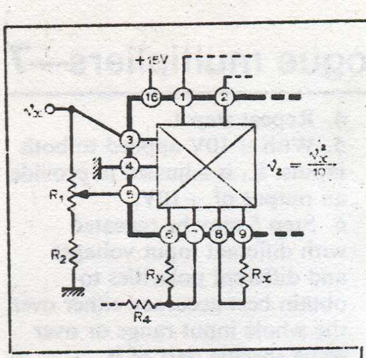
Translinear multiplier

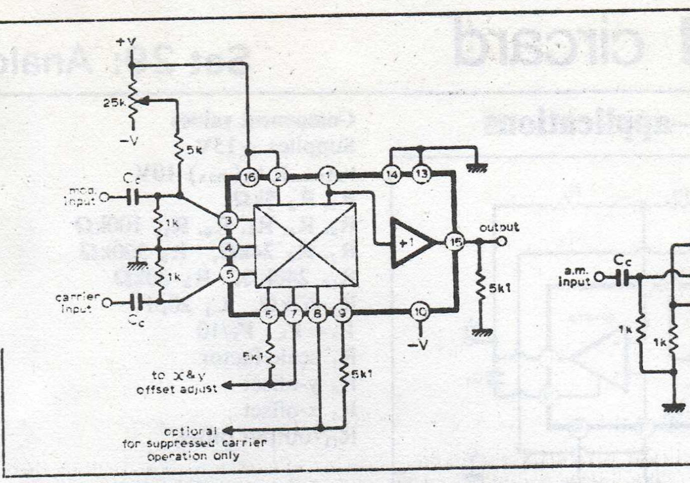


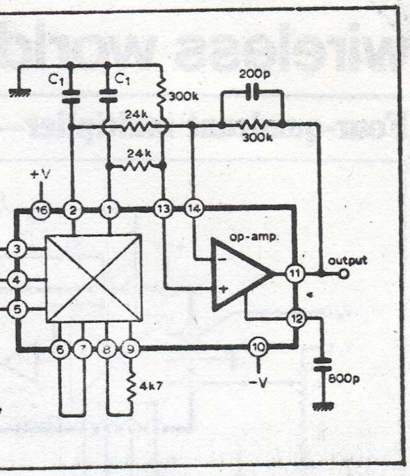
Circuit description
The circuit currents above are related to a defined current unit I, by the following:
$I_1=(1+X)I/2$ $I_2=(1-X)I/2$
$I_3=(1+Y)I$
where X and Y are controlled variables, and I_{diff} between Tr_2 and Tr_3 collectors is XYI. The circuit operates in the current domain and depends for its temperature independence on the proportionality of bipolar transistor g_m (transconductance) to the collector current. Currents I_1, I_2, I_3 are ideally current sources, and the above network comprising V_x, V_y, resistors R_3 to R_7 is an attempt to simulate such a condition e.g. I_3 is approximately equal to $-V_c/(R_7+R_{11}/2)\approx 100\mu A$ plus a multiple of 100μA defined by V_x/R_4 where V_x is increased in steps of 1V. These calculations assume that the base-emitter junction voltages are negligible. To obtain a balanced condition where $I_{diff}=0$ if either V_x or V_y is zero demands trimming of resistor R_6 and R_2 to allow for the 1.2V potential at the emitters of Tr_2, Tr_3. Linearity of I_{diff} is shown in accompanying graphs. Note, that if $V_x=+8V$, this is equivalent to eight units of

Typical data
Tr_{1-4} 1/5 CA3086
R_1 47kΩ ±5%
R_2 46.6kΩ (trimming required)
R_3, R_4, R_5, R_7, R_8 100kΩ ±5%
R_6 68.7kΩ (trimmed)
R_9, R_{10} 50kΩ IC1 741
R_{11} 100kΩ R_{12}, R_{13} 10kΩ
V_c ±15V
V: ±12V V_s: ±15V
N.B. Pin 13 of CA3086 must be connected to most negative potential.









input the output is adjusted to be +10V using R_1.

4. With −10V applied to the input check that the output is +10V, if this is not so repeat steps 1 to 3.

A.m. generator

The circuit (middle) is that recommended for generating double sideband signals or for suppressed-carrier a.m. generation. Modulation and carrier are applied to the x and y inputs respectively with a carrier level of 1V (r.m.s.). The level of the carrier appearing at the output is adjusted by means of the 25kΩ potentiometer which sets the d.c. level at pin 3. In suppressed-carrier applications, the carrier level at the output can be further reduced by means of the x and y offset adjustment controls. The buffer amplifier provides a unity gain low-impedance output, but if not required pin 15 should be open circuited to reduce power dissipation. Carrier suppression of 40dB up to 1MHz and 30dB up to 10MHz is obtainable without the use of the x and y offset adjustments.

Synchronous a.m. detector

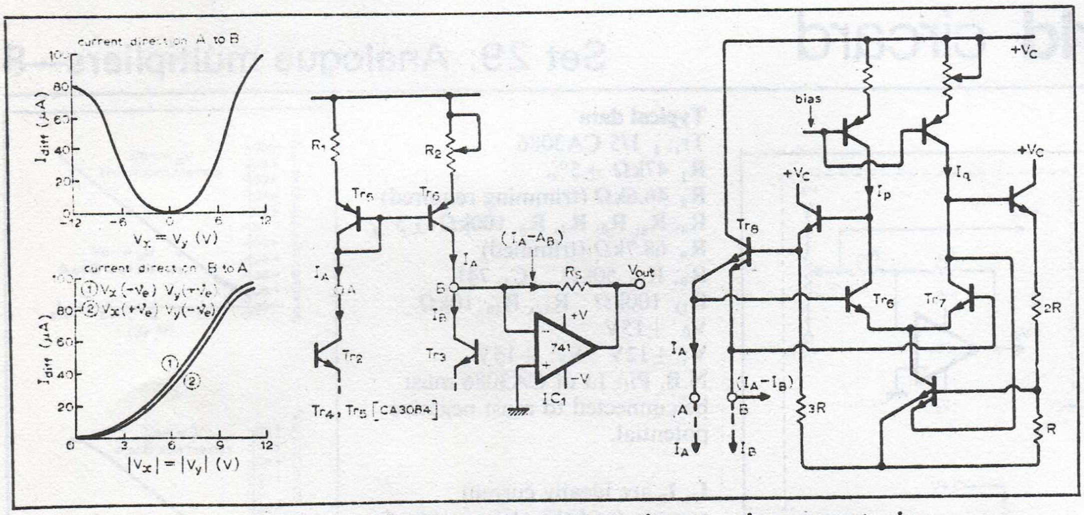
The circuit (right) is suitable for demodulation of a.m. signals with carrier frequencies up to 100MHz, with an input signal of at least 25mV r.m.s. The a.m. input is applied to the common terminal of the multiplier, the y-gain terminals are strapped allowing this section to act as a limiter for inputs greater than about 50mV r.m.s. and the x-section acts in its linear mode. Capacitors C_1 at pins 1 and 2 in the low-pass filter serve to reduce the carrier feedthrough to the output.

Further reading

XR-2208/2308 Operational multiplier data sheet, EXAR, 1972.

Related circuits

Set 29, card 6



current, and if $V_Y = +2V$, two units of current. Resulting product is 16.

Parameter changes

If $X = Y$, the output function is a squared function of those variables. Graphs of the resulting current variation are given above. For each graph, the effect of Y being negative causes a slight deviation from the true square law. Possibly due to inexact compensation for V_{BE} drops with network employed.

Component changes

Circuit is supply sensitive, especially at the low levels of current I. At $V_c = \pm 15V$, a 20% reduction of V_c provides a −3% error for $I_{diff} = 81\mu A$, but at 9μA, +30% error.

Circuit modifications

- Use of transistors Tr_4, Tr_5 in a current mirror configuration will permit the differential current to be obtained with respect to ground. R_1 and R_2 are adjusted to be similar to obtain equal collector currents in Tr_4, Tr_5. This current is converted to an equivalent voltage by driving into IC_1, such that $V_{out} = -(I_A I_B) R_S$.

A more sophisticated technique[2], with a wide frequency response, is shown extreme right. Transistor Tr_8, which has a double emitter, could be derived from a monolithic package by paralleling collectors and bases. The bias voltage which should be the silicon bandgap voltage (1.205V) minimizes the current ratio I_p/I_q drift with temperature. If $I_P = I_Q$, then the base-emitter junction voltages of Tr_6 and Tr_7 are equal (for equal emitter areas). This implies that the emitters of Tr_8 are at the same potential, and hence the currents are equal.

Further reading

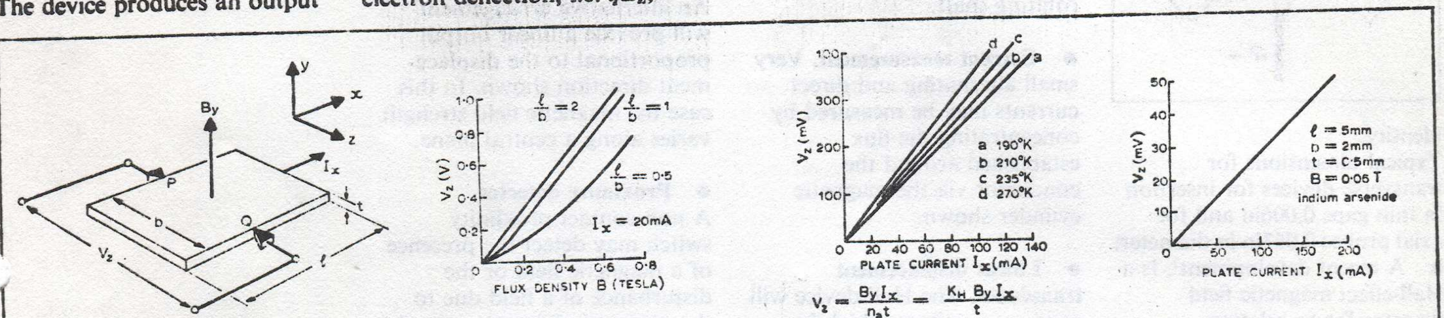
1. Gilbert, B. Translinear circuits: A proposed classification, *Electronics Letters*, 9 Jan. 1975. vol. 11, no. 1.
2. Gilbert, B. Wideband negative current mirror, *Electronics Letters*, 20 March, 1975. vol. 11, no. 6.
3. Korn & Korn. Electronic analogue and hybrid computers McGraw Hill 1972.

Hall-effect multiplier

Hall-effect multiplier
In a practical Hall plate, point electrodes between which the Hall voltage is developed are connected midway between the end-electrodes. Materials used for the plate are high mobility bulk semiconductors, with low conductivity: indium arsenide, germanium, indium antimonide.

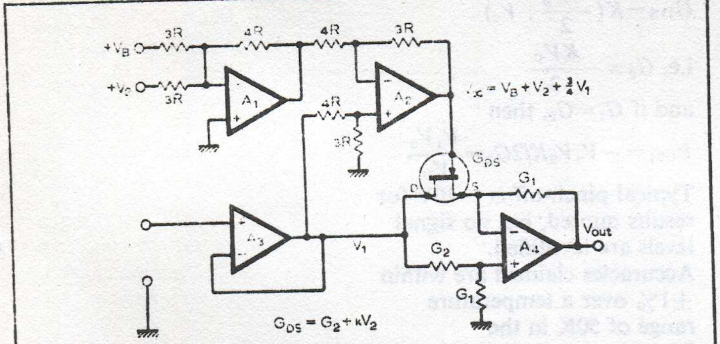
Background
The device produces an output voltage dependent on the product of two inputs—the plate current I_x, and an external magnetic field B_y (Tesla). Current flow is due to electrons n, charge q and drift velocity v_x. Hence current density
$J_x = I_x/bt = nqv_x$.
Deflecting force on electrons in direction Z due to B_y is
$F_z = B_y q v_x$.
At equilibrium, this just balances the field force due to electron deflection, i.e. qE_z,
$B_y q v_x = qE_z$ and $E_z = B_y v_x = B_y I_x/btnq$
The Hall voltage is $V_z = E_z b$
$V_z = B_y I_x/mqt = K_H B_y I_x/t$
K_H is known as the Hall coefficient and should be as large as possible for maximum output. Conductivity is $\sigma = qn\mu_n$ where μ_n is electron mobility
$K_H = 1/qn = \mu_n/\sigma$
High mobility, low-conductivity optimizes device Hall voltage for specific thickness t.

Applications
- An appropriately dimensioned device can be inserted within the air gap flux-path of a rotating electrical machine to determine flux density variations, when I_x is maintained constant.
- Both I_x and B_y can be generated by suitable voltages, and assuming fixed orientation between the Hall device and the field, then $V_z \propto V_x V_y$, where V_x and V_y may assume an alternating or direct voltage



$$V_z = \frac{B_y I_x}{n_q t} = \frac{K_H B_y I_x}{t}$$

F.e.t. analogue multiplier



Circuit description
The conductance G_{DS} of the junction field-effect transistor depends on the voltage V_x. To linearize the f.e.t. in its pre-pinch-off region V_x must comprise one half of the sum of the separate drain and source voltages with respect to ground. In this case, that is equivalent to $\frac{1}{2}(V_1 + V_1/2)$. The total gate-voltage is then a fixed bias voltage V_B, a signal voltage V_2 and the required $\frac{3}{4}V_1$ is obtained via A_3 and A_2. With then the equivalence of conductances G_1, the output voltage V_{out} is linearly proportional to the product of signals V_1 and V_2, when G_{DS} is equal to G_2 plus an incremental value proportional to V_2. Equating the potentials at the inverting and non-inverting inputs of amplifier A_4 and using the parallel generator concept then

$$\frac{V_1(G_2 + KV_2) + V_{out}G_1}{G_1 + G_2 + kV_x} = \frac{V_1 G_2}{G_1 + G_2}$$

This gives

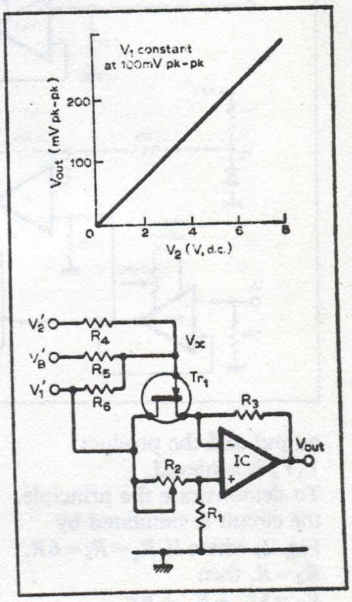
$$V_{out} = \frac{KV_1V_2}{G_1 + G_2}$$

The drain current drain-source voltage relationship is

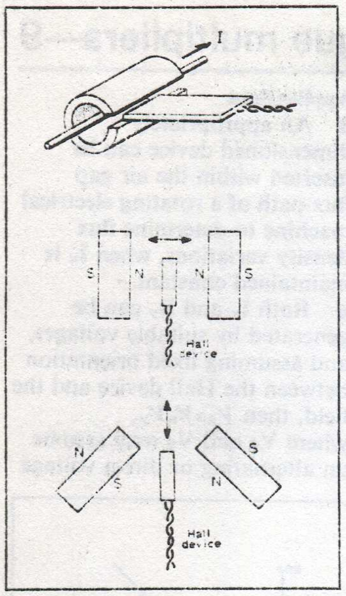
$$I_D \propto \left(V_G - V_P - \frac{V_D + V_S}{2}\right)V_{DS}$$

If V_G does comprise V_B, V_2 and $(V_D + V_S)/2$, then $G_{DS} = I_D/V_{DS} \propto (V_B - V_P + V_2)$ for pre-pinch-off.

Typical data (simulation)
IC SN741 Tr$_1$ 2N5457
R$_1$, R$_3$ 330Ω, R$_2$ 1kΩ
R$_4$, R$_5$ 22kΩ, R$_6$ 6.8kΩ
frequency 1KHz
V_1 maintained at 100mV pk-pk to achieve the best linearity. Linearity obtained is demonstrated on the graph.



If the constant of proportionality $K_1 = K$, and is such a value that $K_1(V_B - V_p) = G_2$, then a linearised relationship between the



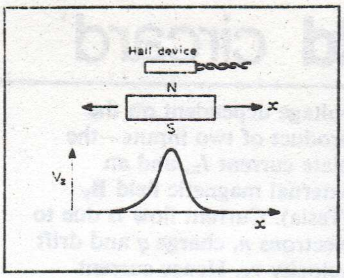
identity.
Typical dimensions for transverse devices for insertion in thin gaps 0.006in and for axial probes 0.063in in diameter.

- A recent development[1], is a Hall-effect magnetic field detector for translating information on the polarity and field strength of a magnetic into a differential output current using integrated circuit technology (Mullard TCA450A). This device offers a high level of sensitivity, low offset flux and is self-balancing. Typical supply voltage 4-16V. Magnetic sensitivity 0.4V/Tesla. Offset flux density $\pm 7.5 \times 10^{-3}$ Tesla.
Possible applications include isolated current sensing and control in high current situations, conversion of magnetic quantities into proportional currents, detection of positional movements of a rotating shaft.

- **Current measurement.** Very small alternating and direct currents may be measured by concentrating the flux established around the conductor via the magnetic cylinder shown.

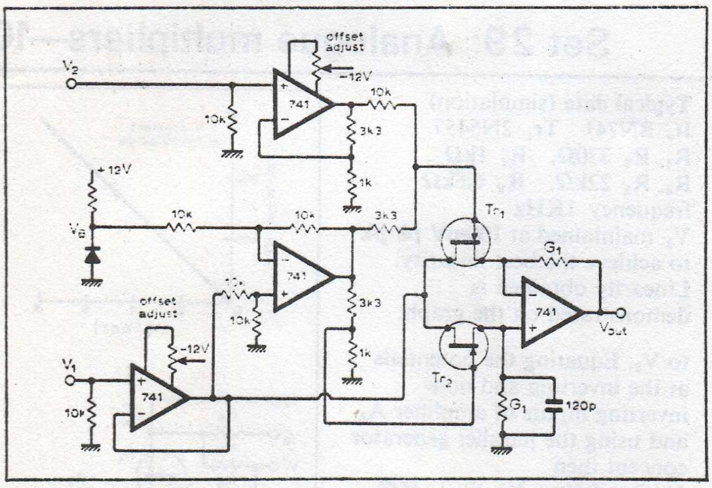
- **Linear displacement transducer.** The Hall device will produce a voltage which is a function of the motion between the device and a stationary magnetic field. Displacement laterally between the magnets will produce an output voltage when the device is moved from the mid-position. An alternative arrangement will provide a linear output proportional to the displacement direction shown. In this case the magnetic field strength varies along a central plane.

- **Proximity detector**
A non-contact proximity switch may detect the presence of a magnetic field or the disturbance of a field due to the presence of ferrous material. Hall voltage, V_z, variation in relation to relative position of magnetic and Hall device would be as shown.



References

Chasmer, R. P., Cohen, E., Holmes, D. P. Design and performance of a Hall-effect multiplier, *Proc. IEE* 106 Part B. Supplement 16, 1959.
Newsome, J. P. Application of the Hall effect. *Electronics & Power*, April 1966.
1. Mullard News Bulletin, 1975.



output and the product V_1V_2 is achieved.
To demonstrate the principle, the circuit is simulated by Fig. 2, where if $R_4 = R_5 = 6R$, $R_6 = R$, then
$V_x = \frac{3}{4}V_1 + V_2' + V_B'$.
To obtain the best linearity, these values of resistors need to be chosen empirically. This is most easily performed using an oscilloscope with an X−Y facility, where the input V_1 and output for V_2 zero volts are applied X−Y inputs respectively. Any non-linearity or offset can then be minimized by varying the resistors.
A more practical circuit (see reference) includes temperature compensation by making G_2 another voltage dependent conductance, using a matched field-effect transistor (above). For maximum signal amplitudes, f.e.ts with a high pinch-off should provide a wider working range.
Also if the gate bias V_B is arranged to be one half the pinch-off value, then

$$G_{DS} = K\left(-\frac{V_p}{2} + V_2\right)$$

i.e. $G_2 = -\dfrac{KV_p}{2}$

and if $G_1 = G_2$, then

$$V_{out} = -V_1V_2K/2G_2 = \frac{V_1V_2}{V_p}.$$

Typical pinch-off is −10V for results quoted, but no signal levels are identified.
Accuracies claimed are within ±1% over a temperature range of 50K in the frequency range 0 to 20kHz, using matched f.e.ts whose conductances are within ±5%.

Reference

Miller, A. Temperature compensated analogue multiplier, *Electronics Letters* 9 Sept. 1971, vol. 17, no. 18.

Related circuits
Set 22, card 7