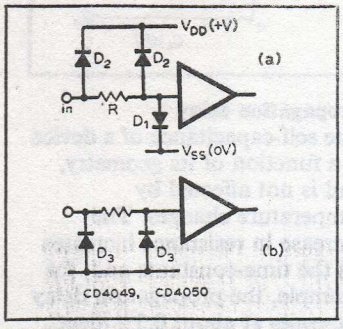
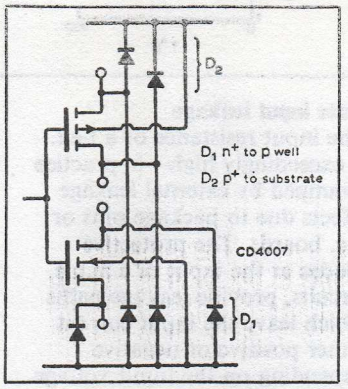
wireless world circard

Set 27: C.m.o.s.—1

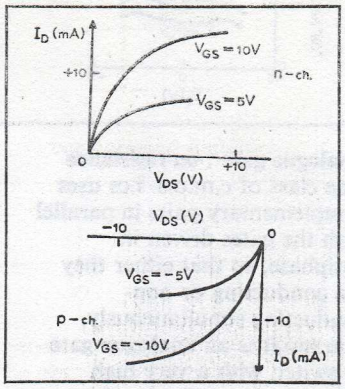
Devices and characteristics



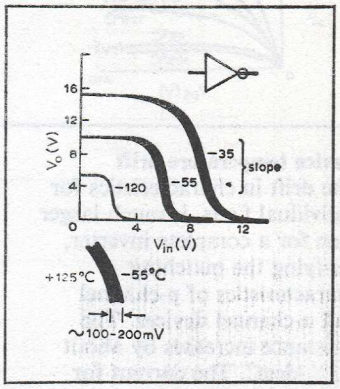
Input protection
A network of diodes at the input of each gate/inverter protects against transients. In linear applications they limit the range of input voltages that can be applied, in particular when the designer seeks access to individual devices, using a non-standard supply voltage to disable unwanted devices. Most packages conform to Fig. 1(a)—certain buffers to Fig. 1(b).



Output diodes
The processing steps needed to produce complementary devices leave a number of p-n junctions between source and drain and the supply terminals. In most devices the sources are already directly connected, but the junctions become apparent in certain i.cs with access to individual devices.



Device characteristics
Each device has a current that is a function of both gate and drain potentials. Above a critical voltage on the drain, which varies with V_{GS}, the drain current becomes largely constant i.e. the slope resistance is large and the device is in a constant-current mode, and said to be saturated. Below this voltage the output resistance is lower, non-linear and is varied by the gate-source voltage.



Transfer function
The output voltage changes sharply with input voltage at a particular input that is remarkably stable against temperature, has a broad tolerance from device to device but is at a roughly fixed percentage of supply for a given device.

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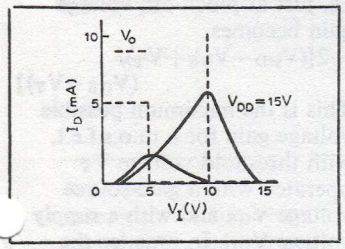
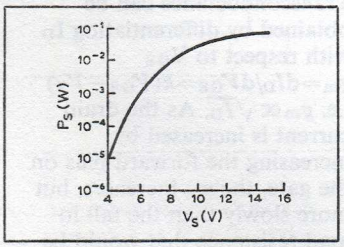
Set 27: C.m.o.s.—2

Linear circuit characteristics

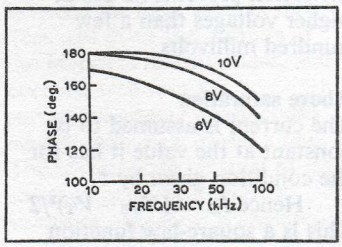


Current variations
When the input voltage to an inverter is varied, it is no longer true that the current remains at zero as in logic applications. For $V_I \approx V_{DD}/2$ the inverter output is in its linear region, both devices are forward-biased and the current rises to a maximum. At high supply voltages the current can be >20mA for high-current buffers. At low supply voltages the current is so low that the operation approximates to class B.

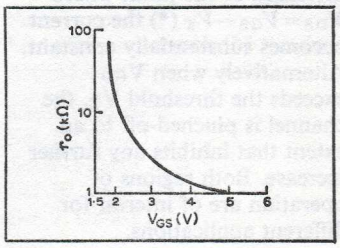


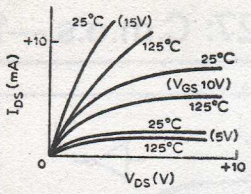
Power dissipation
As an example a NOR gate was biased for $V_O = V_I$ and the supply voltage varied from 4 to 15V. At the low end the current fell to 2μA with a dissipation below 10μW. At the supply maximum the dissipation approached 100mW—the limit suggested for any single gate or buffer with a package limit of 200mW. Thus it would not be safe to operate all four gates in the linear mode at the otherwise safe supply voltage of 15V.

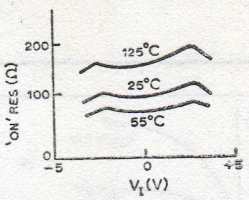
Phase/frequency variation
The change in characteristics with supply, extends to the phase shift at high frequencies. In a multi-stage amplifier this could bring the frequency at which instability might occur to below 600kHz (60° phase lag per stage at 6V supply would give a total phase shift of 180° in a three stage feedback amplifier). This together with the drastically increased output resistance makes it difficult to design linear amplifiers at supply voltages of 5V and below.

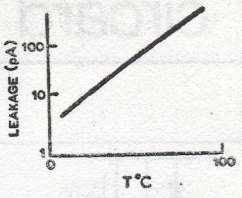


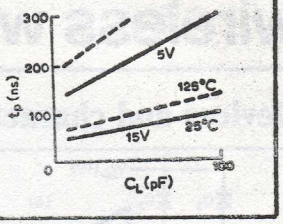
Output resistance
The slope-resistance of a m.o.s.f.e.t. is moderately linear close to the origin, and can be varied over a very wide range. At high values of V_{GS} the resistance can fall well below 1kΩ. As V_{GS} approaches the threshold voltage, the device is cut off and the slope resistance tends to infinity. In practice a controlled resistance of order 100kΩ is possible. In all cases the polarity of V_{DS} may be reversed, and the V/I characteristic is continuous though the voltage swing for reasonable linearity is restricted to a few hundred mV.









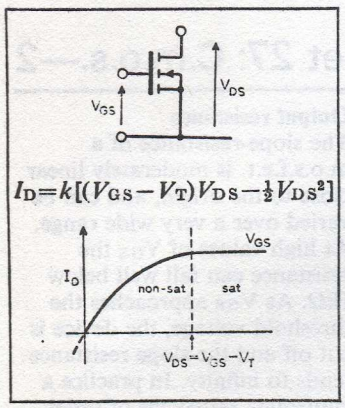


Device temperature drift
The drift in characteristics for individual f.e.ts, is much larger than for a complete inverter, verifying the matching characteristics of p-channel and n-channel devices. The resistance increases by about 0.3%/degC. The current for any combination of V_{DS} and V_{GS} falls by around 30% for the temperature range indicated. The current depends on a square-law relationship involving V_{GS} and V_{DS}, except in saturation when V_{DS} has little further effect.

Analogue gate : on-resistance
One class of c.m.o.s. i.cs uses complementary pairs in parallel with the gates driven in antiphase, so that either they are conducting or non-conducting simultaneously. The result is an analogue gate or switch with a very high off-resistance and a low but non-linear on-resistance. Again the resistance is temperature dependent, with a comparable temperature coefficient (caused by the same change in mobility of the current carriers). The pattern repeats itself at all voltages and currents.

Gate input leakage
The input resistance of a f.e.t. is exceedingly high—in practice swamped by external leakage effects due to package pins or p.c. boards. The protective diodes at the input of c.m.o.s. circuits, provide leakage paths which leave the input current either positive or negative depending on the input voltage. Though still very small the current varies exponentially with temperature. A leakage current of 10pA at room temperature could increase a hundredfold at the device maximum temperature. It is generally safe to assume an input resistance in excess of 10MΩ.

Propagation delay
The self-capacitance of a device is a function of its geometry, and is not affected by temperature changes. The increase in resistance increases all the time-constants and, for example, the propagation delay increases at about 0.3%/degC. Similar figures apply to most pulse characteristics, the speed at higher voltages being markedly improved. This is because the sharp fall in resistance allows the larger voltage swing to be achieved in a much shorter time. For linear operation, the bandwidth is much increased at higher voltages, and somewhat decreased at higher temperatures.



$$I_D = k[(V_{GS} - V_T)V_{DS} - \tfrac{1}{2}V_{DS}^2]$$

Basic device equations
The equation gives the drain current or a function of the p.ds between gate and source, and drain and source in the unsaturated region. As V_{DS} is increased to the point where $V_{DS} = V_{GS} - V_T$ (*) the current becomes substantially constant. Alternatively when V_{GD} exceeds the threshold V_T, the channel is pinched-off to an extent that inhibits any further increase. Both regions of operation are of interest for different applications.

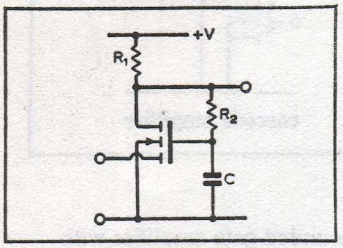
Below saturation
Both drain and gate potentials have an effect, but if V_{DS} is small then the equation approximates to a linear one—it extends below the origin but there is an additional constraint imposed by protective diodes.
$I_D \approx k(V_{GS} - V_T)V_{DS}$
Thus the slope resistance at low voltages becomes
$dV_{DS}/dI_D \approx 1/k(V_{GS} - V_T)$
This is a voltage-controlled resistance though it is neither a linear resistor nor a linear function of the controlling voltage. The departure from linearity is small enough for $V_{DS} < 100$mV to use the resistor in feedback networks etc to control gain, but distortion prevents its use at higher voltages than a few hundred millivolts.

Above saturation
The current is assumed to be constant at the value it has for the condition given by *.
Hence $I_D = k(V_{GS} - V_T)^2/2$
This is a square-law function requiring the elimination of V_T by some compensating circuit if a square law relationship is to be obtained between input and output voltages. Transconductance can be obtained by differentiating I_D with respect to V_{GS}
$g_m = dI_D/dV_{GS} = k(V_{GS} - V_T)$
i.e. $g_m \propto \sqrt{I_D}$. As the drain current is increased by increasing the forward bias on the gate, the g_m increases, but more slowly than the fall in load resistance that would be needed in a resistively loaded stage to allow that current to flow. Since the voltage gain depends on the product of g_m and R_L, higher voltage gains can be obtained by operating at the smallest possible current, increasing R_L accordingly. This information does not apply directly to c.m.o.s. inverters where the load of one m.o.s. device is the output of the other; it indicates a different pattern for f.e.ts from that familiar in bipolar designs where comparable voltage gains are available at all current levels.

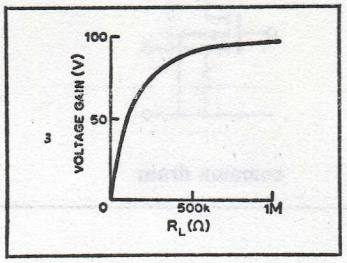
Assuming that the device is operated with the lowest possible V_{DS} to maximize R_L i.e. just at pinch-off, voltage gain becomes
$-2[(V_{DD} - V_{GS} + V_T)/(V_{GS} - V_T)]$
This is the maximum possible voltage gain for a m.o.s.f.e.t. with threshold voltage V_T operated with a gate-source voltage V_{GS} and with a supply voltage V_{DD}. In practice the voltage gain will be smaller in magnitude because of finite output resistance etc.
N.B. The basic form of these equations applies to all m.o.s.f.e.ts; the coefficients of practical devices differ from those given and account has to be taken of this—see card 7.

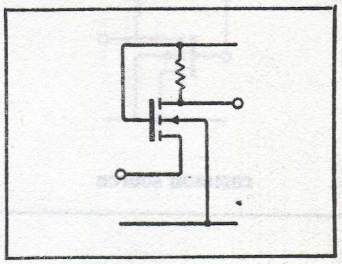
Further reading
Motorola, McMOS Handbook, 2nd edition 1974, pp. 1-7 to 1-18 and 3-1 to 3-7.
Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.

Device configurations



Typical performance
IC CD4007AE
in-channel device
Supply +10V
R_1 100kΩ
R_2 10MΩ
C 100nF
Voltage gain +50

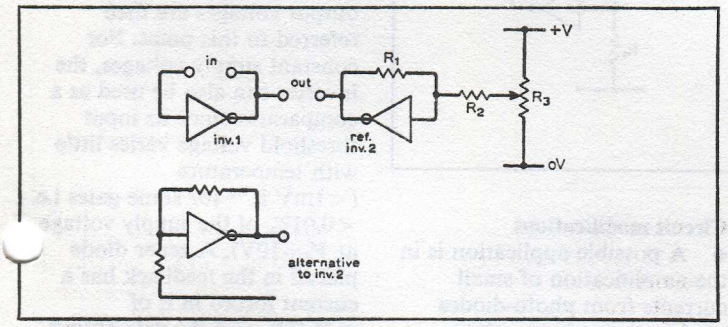




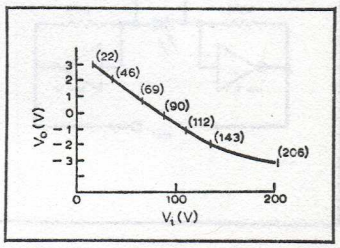
Circuit description
In certain c.m.o.s. i.cs, access may be gained to the sources/drains of individual f.e.ts (CD4907, CD3600 and similar). Where this is so, circuits may be constructed that are the counterparts of the more familiar common-base common-collector etc. Consider the common-gate amplifier shown above. The gate is grounded for a.c. purposes by the capacitor. The gate current is negligible and the p.d. across R_L may be assumed to be zero. The d.c. operating conditions for the amplifier are thus $V_{GD}=0$ and R_1 defines the direct current flow. The alternating voltage gain depends on the parallel value of R_1, R_2. The input impedance is low, and to a good approximation is $1/g_m$ where g_m is the transconductance of the device as usually defined. This varies with the operating current being proportional to $\sqrt{I_D}$. Since $I_D \propto 1/R_1$ if the p.d. across R_1 is constant (a reasonable approximation when the supply voltage is well above the device threshold voltage) then the voltage gain ($\approx g_m R_1$) is proportional to $\sqrt{R_1}$. The approximation is not valid at very low currents and the voltage gain is limited to about +100. The voltage gain for a given value of R_1 is roughly proportional to the square root of the supply voltage by the same reasoning, falling more rapidly as this approaches the threshold values. The amplifier has a high non-inverting voltage gain, a low input-impedance and a high output-impedance.

Component changes
IC: must be package with separate access to drain. Any discrete m.o.s. device (enhancement mode can be used in these circuits—the aim here being to indicate where c.m.o.s. packages can be adapted to provide functions that would otherwise require separate discrete components).
Supply: +5 to +15V.
Some gain available at lower supply voltages.
R_1: sets the quiescent levels and the output impedance. Can be replaced by current source for increased voltage gain.

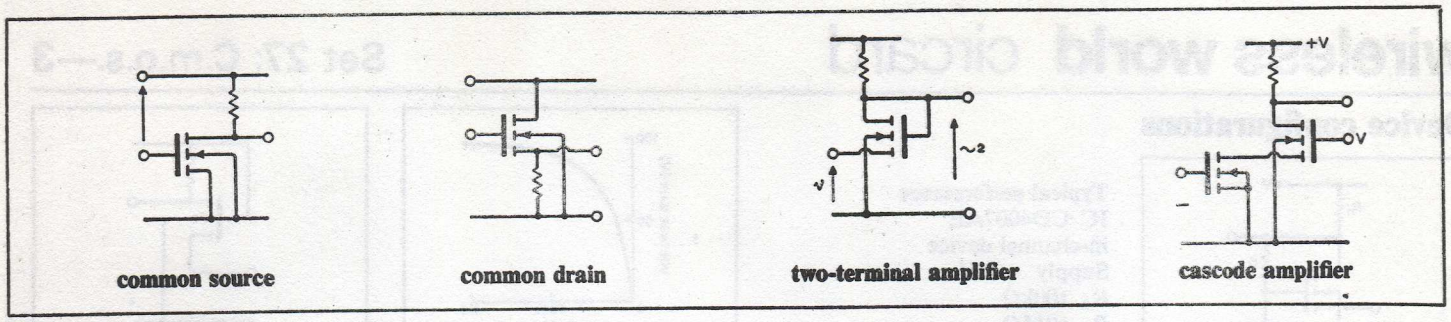
D.C. amplifiers



Typical performance
IC CD4001AE NOR
gates with 2 inputs active
Supply +10V
R_1 27kΩ
R_2 1MΩ
R_3 100kΩ



Circuit description
C.m.o.s. inverters are not suited to the amplification of small d.c. voltages. They have a threshold voltage range below and above which the output is saturated. The simplest way of biasing an inverter/gate into its linear region is via direct or resistive feedback from output to input. This ensures $V_{out}=V_{in}$ which is near the middle of its linear region, the voltage gain lying between −10 and −100. Although there is a measure of matching between devices on the same chip, the tolerances are much relaxed for digital circuits. The output voltage under these conditions may have a total spread of up to 40%, with the difference between gates from a given chip reduced to the order of 100mV. This allows the use of a pair of gates, one as the amplifier and the other to act as an artificial ground point. The offset voltage can be mulled out by injecting a portion of the supply via R_3 and R_2 as shown, while the offset itself has a relatively small temperature dependence. There remains one major advantage of these devices as d.c. amplifiers, viz their very high input impedance. If feedback is to be used to define the voltage gain while exploiting this high input impedance as fully as possible, the source can be connected between the input and output of the inverter. For a voltage gain of −100, 99% of the source voltage appears at the output terminal and 1% at the input i.e. the accuracy with which an input signal is transmitted to the load can be well within the tolerance of moving-coil meters. The current drawn from the source is not specified in the data sheets as these devices are intended for digital functions, but is basically due to the minute leakage currents of the reverse biased protective diodes. With



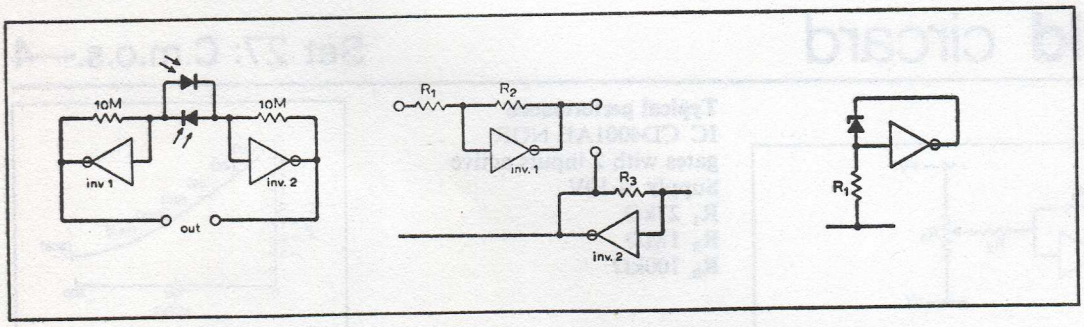
10k to 1MΩ.
R_2, C: provide decoupling and the time-constant must be long compared with period of lowest frequency. R_2 1M to 22MΩ.

Circuit modifications

- The gate can be connected directly to the positive supply, which reduces the component count, but removes the stabilizing action of the d.c. negative feedback. Otherwise, the a.c. properties are comparable.
- Each of the other device configurations is possible, the common-source version simply disregarding the presence of the p-channel device by ensuring that its source and/or drain is open circuit. The voltage gain is comparable to that for the common-gate stage but the input current is now zero, and the output is inverted.
- A common-drain or source-follower configuration can often be provided while using the other transistor of the complementary pair in some other circuit, e.g. astable oscillator. Whatever waveform appears at the common gate is transferred to the source with some attenuation but without loading the waveform. Since source and drain currents are equal an antiphase output can be obtained at the drain.

A novel arrangement joins the gate to the drain for 100% negative feedback. The device is now apparently a two-terminal device and might be expected to behave as a non-linear resistor. In fact it acts as a non-inverting voltage amplifier with a low voltage gain. This is because the substrate connection acts as a subsidiary gate and the operation is that of a grounded-gate amplifier with the gain much reduced by the feedback to the main gate. Any of the multi-transistor circuits can be implemented using several devices from a package and the example illustrated is the cascode circuit useful for high voltage gains where input-output isolation is important.

Cross references
Set 27, card 2.
Set 20, card 8.



some sample gates, the output changed by <1% for a change in source resistance of 4.7MΩ. The configuration is clearly restricted to a floating source (high impedance transducer such as piezo-electric devices) or would require a floating power supply. The second inverter compensates for most of the quiescent output by its matched characteristics, the remainder being cancelled by injecting a variable current via R_2, R_3.

Component changes

- The only changes in the resistors are to vary this offset compensation. The values are not critical, but $R_2 \gg R_3$ and R_1/R_2 = offset voltage/supply voltage, indicate the values. The inverters can be buffers, NOR and NAND gates or the inverters constructed from CD4007 or CD3600 packages. More of these compete in performance with op-amps constructed from the appropriate m.o.s. and bipolar transistors. They are intended only to extend the applications of inverters/gates to simple d.c. applications where the signal voltages are large enough that significant offset can be tolerated.

Circuit modifications

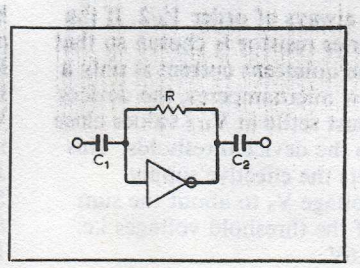
- A possible application is in the amplification of small currents from photo-diodes used in their photo-voltaic mode. For matched diodes exposed to different light intensities, there will be a current of given polarity representing the difference between the light intensities. This will drive the outputs of the inverters in anti-phase, and currents well into the sub-microampere range could be detected. $V_0 \approx 20M\Omega \times I_{diff}$. The inverter can be used in the see-saw mode with resistor values of megohms if required. The voltage gain can be set to between −1 and −10 with good accuracy, with a second inverter to provide an artificial ground point. Both input and output voltages are then referred to this point. For constant supply voltages, the inverter can also be used as a comparator since its input threshold voltage varies little with temperature (<1mV K^{-1} for some gates i.e. <0.01% of the supply voltage at V_s=10V). A zener diode placed in the feedback has a current forced in it of $\approx V_s/2R_1$ and the gate output voltage is raised by V_z over its normal threshold. This can be used to define the compensation current fed into other stages used as d.c. amplifiers etc.

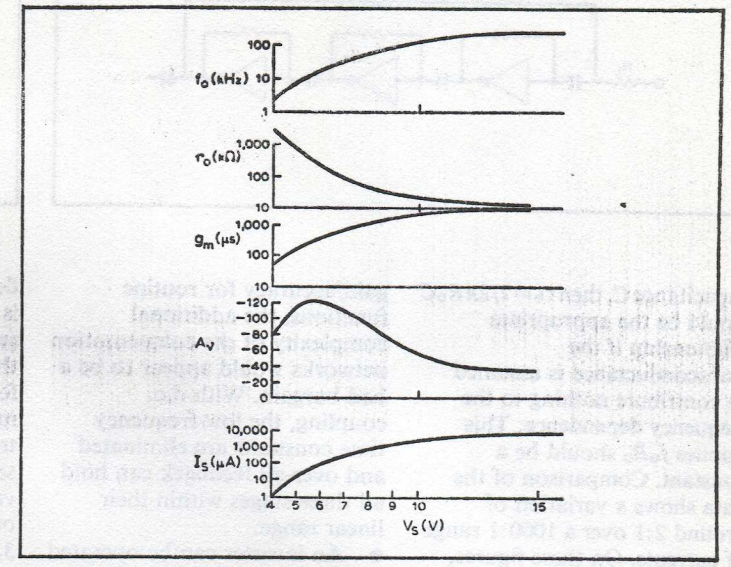
Further reading
McMOS Handbook, Motorola 2nd edition 1974, p. 8-15.

Cross references
Set 27, card 1.
Set 11, cards 5, 6.
Set 20, card 8.
Set 9, card 11.

A.C. amplifiers

Typical performance
IC ¼×CD7001AE
Supply +10V
Quiescent current 1.9mA
Output resistance 25kΩ
Voltage gain −53
Transconductance 2.1mS
Upper cut-off frequency 130kHz
R 6.8MΩ
C_1, C_2 100nF

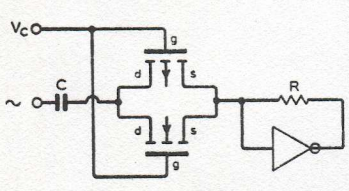




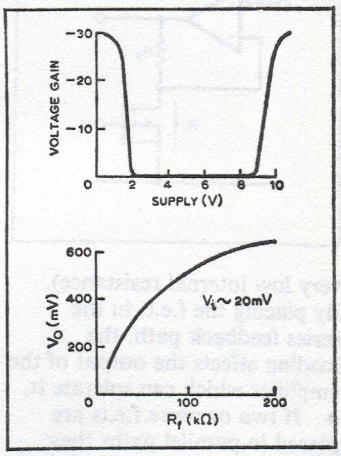
Circuit description
The basic open-loop behaviour of an amplifier can be predicted from its internal structure fairly readily in cases as simple as a c.m.o.s. inverter. For the resistive feedback bias as shown, the input and output potentials are equal. Hence each device operates with equal gate and drain potentials. This introduces opposing effects on the voltage gain as the supply voltage increases. First the increase in operating current which is very marked leads an increase in the transconductance (g_m). At the same time the output resistance is markedly reduced because each device is operated on or below the knee of its output characteristic. The net effect is that the overall voltage gain is relatively constant varying by only 10dB over a 1,000:1 range in currents. The measurements were all made with a probe having an input resistance of 10MΩ and with a total input capacitance and strays of about 18pF. The high voltage gain at the lower supply voltages is hard to make use of, since even the high feedback resistance contributes to the loading effect. The increase in cut-off frequency as the current rises, can be explained if we assume a total output capacitance which is constant. If the output resistance is r_o, the cut-off frequency f_o and the shunt

Gain-controlled amplifiers

Circuit description
A more familiar method of using a m.o.s.f.e.t. as part of a gain-controlled amplifier is to use it as the lower section of a potential-divider in either the forward or feedback paths of amplifier. This allows the m.o.s.f.e.t. to operate with source grounded and makes it easier to apply a control voltage to the gate. If the source is connected to any other point at a constant potential then a control signal may be applied, but it must be sufficient to take V_{GS} above its threshold value V_T. In the circuit shown, either or both of a complementary pair can be used with gates, sources and drains commoned, provided these are not already grounded internally. If the control voltage V_c is in the mid-range of the supply there is insufficient V_{GS} to bring either device into conduction and the voltage gain→0. When the control voltage is very low, the p-channel device is brought into its conducting state and the gain sharply increases. For $V_c \rightarrow V$, the n-channel device has a low slope resistance and the gain increases. The graph shows that either characteristic can give a voltage gain which can be controlled from zero up to −30. At the low values of gain the control action is rather sharp. The amplifier is another c.m.o.s. pair used as an inverter with R providing shunt feedback defining the input potential by the virtual earth action.

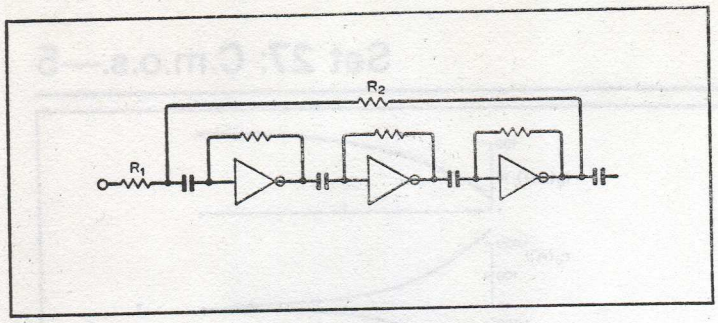


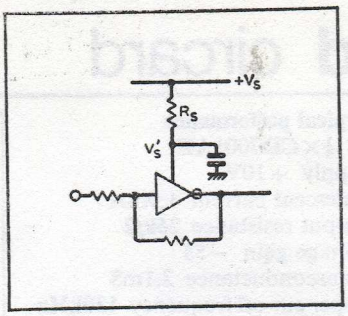
Typical performance
IC 2/3×CD4007
Supply 10V
R 220kΩ
C 1μF
Control V_c 0 to 10V voltage

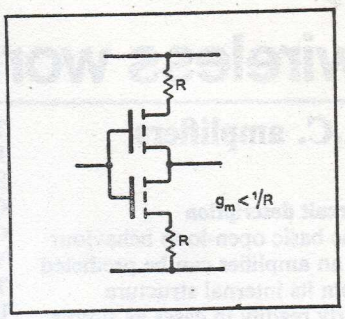


Component changes
IC: Any single m.o.s.f.e.t. either p- or n-channel may be used.
Supply voltage: since each f.e.t. receives a gate-source voltage which is $< V/2$ the supply voltage has to be >8V in this circuit.
R_f: 10k to 1MΩ
C: not critical. Determines l.f. response. 0.1 to 10μF.

Circuit modifications
● A conventional op-amp circuit can be used as a virtual earth amplifier with the f.e.t. in the forward or reverse paths. Because the f.e.t. has a variable resistance, this complicates the design of the system (unless the source has a







capacitance C, then $r_o = 1/2\pi R_o C$ would be the appropriate relationship if the transconductance is assumed to contribute nothing to the frequency dependence. This implies $f_o R_o$ should be a constant. Comparison of the data shows a variation of around 2:1 over a 1000:1 range of currents. On these figures, the output capacitance would be around 20pF.

Circuit modifications

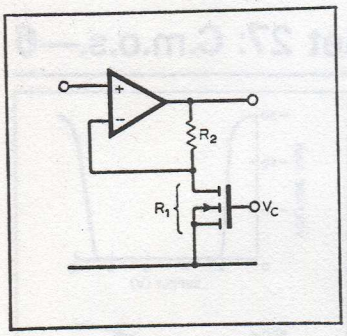
- Multi-stage amplifiers are possible, but since c.m.o.s. stages give sufficient gain/accuracy for routine functions, the additional complexity of the compensation networks would appear to be a bad bargain. With d.c. coupling, the low-frequency time constants are eliminated and over-all feedback can hold all three stages within their linear range.
- An inverter can be operated at low current from a high-voltage supply by adding a series resistor in the supply line and decoupling the inverter supply pin. N.B. The supply rejection ratio is only 6dB since the output of a device with feedback biasing is always of order $V_s/2$. If the series resistor is chosen so that the quiescent current is only a few microamperes, the devices must settle at V_{GS} values close to the device thresholds. This sets the effective supply voltage V_s to about the sum of the threshold voltages i.e. 3.6V.
- In devices with access to the sources (CD4007, CD3600 etc) resistors may be added as shown to define and reduce the g_m values while increasing the output impedance.

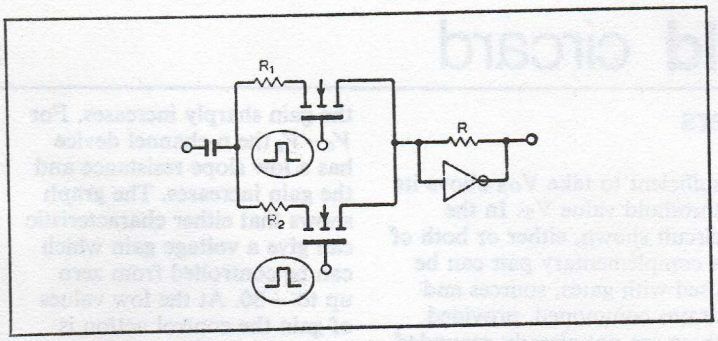
Further reading

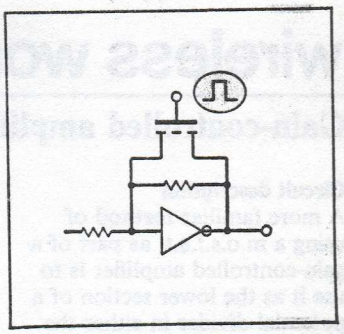
McMOS Handbook, Motorola pp. 8.3-8.15, 3.13-3.18, 2nd Edition, 1974.
Fitchen, F. C. and Ellerbruch, V. G., Linear operation of the m.o.s.f.e.t. complementary pair, *IEEE J. Solid State Circuits*, SC-6, 1971, Dec. pp. 422-423.
Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.

Cross references

Set 27, cards 1, 4, 6.
Set 27, cards 4, 6, 8.
Set 12, card 1.







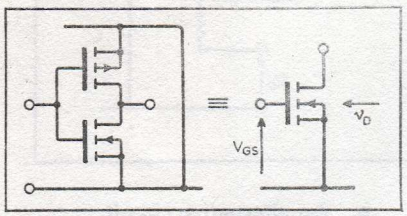
very low internal resistance). By placing the f.e.t. in the series feedback path, the loading affects the output of the amplifier which can tolerate it.

- If two or more f.e.ts are placed in parallel paths they may be gated on or off. This offers a simple alternative to a separate analogue gate i.c. if the performance requirements are not too critical. Both the gates and the inverting amplifier can be derived from a single low cost CD4007 or similar. If the gates of the m.o.s.f.e.ts are paralleled the gain is switched between $-R/R_1$ and $-R/R_2$ provided the on-resistances are low compared with R_1, R_2. It is suitable for gains in the region -1 to -25.
- The f.e.t. can also be placed across the feedback path provided the voltage swing is small enough to prevent non-linearity from producing excessive distortion. One or more devices can be used across both input and feedback paths. Non-linear elements or reactive components can also be placed in series with the f.e.ts. The on-resistance is high compared with devices designed specially as analogue gates.

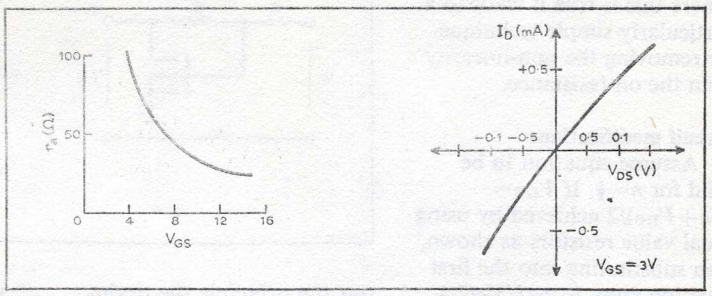
Cross references

Set 27, cards 1, 5, 7.
Set 20, card 8.
Set 21, card 4.
Set 22, card 7.
Set 16, card 10.

Controlled resistances



Typical performance
IC CD4049
V_D 50Ω at V_{GS} of 7V for n-channel device



Circuit description
Some i.cs contain multiple inverters e.g. CD4049 hex buffer. Consideration of their internal structure shows that if the V_{DD} line is shorted to the V_{SS} and then used as the common line, then a positive control voltage on any input varies the slope resistance of that output as if it were a single n-channel f.e.t. If the p.d. across the drain source path is less than 0.5V the internal diodes are not brought into conduction. Hence the package is equivalent to six independent well-matched n-channel enhancement mode f.e.ts. These can be used separately or in combinations in any circuits where voltage-controlled resistors are required. The slope resistance at the origin is controllable over a 10:1 range though the resistance becomes non-linear at a progressively lower drain-source voltage as the gate voltage approaches the threshold value. The non-linearity is indicated for V_{GS} of 3V. The devices match to within 5% with the samples tried but this is not covered by the package specifications since these were designed for digital applications. The resistance is non-linear. As the forward voltage drop across the drain-source path is increased, the value of V_{GD} is reduced, this reduces the forward bias and decreases the channel conductivity. Conversely, a negative current in the drain increases V_{GD} and increases the channel conductivity. When V_{GS} is large the contribution due to the small values of V_{DS} (0 to 200mV) is negligible and the on-resistance can be assumed linear for most applications. The example shown represents the lower limit of V_{GS} at which use as a controlled resistance might be acceptable. The non-linearity is predictable from the basic device equation (Set 27, card 2) $I_D = k[(V_{GS} - V_T)V_{DS} - nV_{DS}^2]$ This theoretical equation represents a wide variety of

Non-linear circuits I

Fig. 1

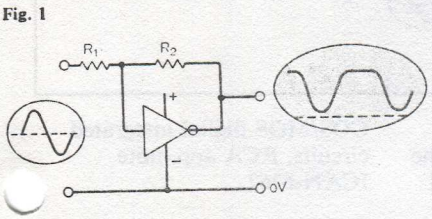
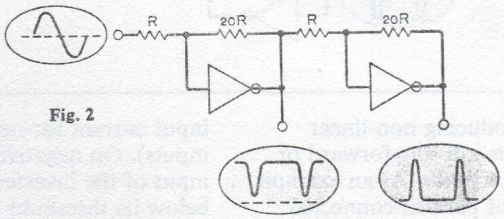


Fig. 2

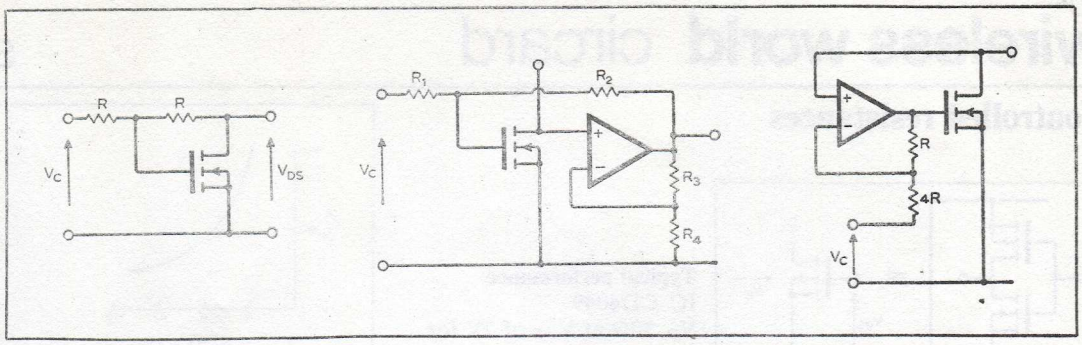


Circuit description 1
The inverter transfer function is such that the output changes rapidly only when the input is close to a threshold voltage of about 45% to 53% of the supply. If the circuit is fed from ground-referred sine-wave with no d.c. blocking capacitor then the output will be severely distorted in most cases. As an example consider a device with threshold 50% of supply and with $R_1 = R_2$. When the input is at zero, the output must be at +V since there will be equal p.ds across R_1, R_2. For all negative inputs the output holds constant at +V. For all positive inputs the change in the output is equal and opposite i.e. the positive half-cycle of input is reproduced as a negative half-cycle with respect to the positive line. The amplifier gain falls as the swing approaches the supply lines so that perfect half-wave rectification is not possible. If the circuit is followed by an identical second stage, the output is inverted and approximates to a non-inverted half-wave rectified version of the input. In each case the peak input has to approximately equal the supply for the output to swing through the whole supply range.

Circuit description 2
The resistors are made unequal to give an inverting gain to −10 to −20 depending on the open-loop gain. In this case the output remains at +V until the input approaches very closely to the inverter threshold voltage. It is only the positive peaks of the input signal that cause any change in the output. The output then consists of short-duration negative going swings coinciding with the positive peaks of the input. If a second identical stage follows it, the peaks are further sharpened up and inverting. The result is a highly amplified version of the extreme positive peaks of the input. The threshold voltage of a given device is a well defined fraction of the supply and varies little with temperature. Thus each device would respond to a particular peak input but once adjusted the response could be maintained.

Circuit description 3
If the original waveform is

devices over a range of currents and voltages, and it is common to assume $n=\frac{1}{2}$. Where this is true it leads to a particularly simple technique for removing the non-linearity from the on-resistance.



Circuit modifications

- Assume equation to be valid for $n=\frac{1}{2}$. If $V_{GS}=(V_C+V_{DS})/2$ achieved by using equal value resistors as shown, then substituting into the first equation gives $I_D=k[(V_C/2+V_{DS}/2-V_T)V_{DS}-\frac{1}{2}V_{DS}^2]=k(V_C/2-V_T)V_{DS}$ i.e. V_{DS} is a linear function of I_D for all values of I_D within the device limits, but the slope is controlled by the direct voltage V_C. The resistors attenuate the control action and V_C has to have twice the value it had in the simple circuit overleaf. Tests with devices from c.m.o.s. packages suggest that in this application considerably more feedback is needed to linearize the characteristic, though some improvement is offered. To test the principle the drain-source voltage has to be amplified before deriving the feedback.
- If the gain is made > minimum required to achieve compensation (e.g. $R_3=9R_4$ giving a gain of +10) then compensation is achieved with $R_1 \ll R_4$ i.e. the control voltage reaches the gate with little attenuation. With $R_2=7R_1$ and the above ratio for R_3/R_4 the on-resistance of a CD4049 n-channel device was controllable from 25 to 200Ω with characteristics matched in the positive and negative quadrants to better than 0.5% and a non-linearity of less than 1.5% (less than 0.5% up to 100Ω). The range of control voltages required was from 3.4V (200Ω) to 16.5V (25Ω). These resistor values feed back a portion of V_{DS} to the gate given by $[V_{DS}R_1/(R_1+R_2)][(R_3+R_4)/R_4]=1.25V_{DS}$. This suggests using $n=1.25$ for these devices to determine the necessary compensation. Unless $n<1$ it would seem to be necessary to use an amplifier with each device to obtain accurate linearization.
- An alternative circuit combines the resistive networks to apply a voltage to the gate of $V_C/4+1.25V_{DS}$. Though simpler, this version requires a larger range for V_C.

Further reading

Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.

Cross references

Set 27, cards 1, 6.
Set 22, card 7.

Fig. 3

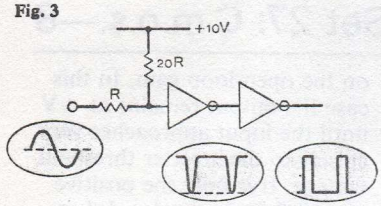


Fig. 4

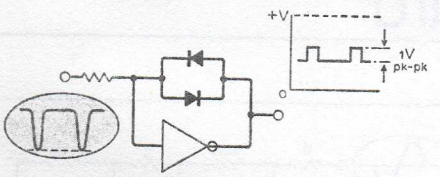
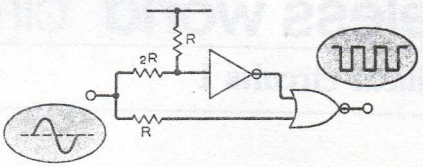


Fig. 5



unimportant, negative-feedback need not be used. The input is biased up to the supply rail and the output consists of negative-going pulses coinciding with the positive peaks of the input (the pulse width increases as the input-amplitude increases since the waveform lies above the threshold for a longer fraction of the cycle). If the output is applied directly to a second inverter the output is re-inverted and is sharpened into an almost rectangular pulse equal in height to the supply.

Circuit description 4

The output pulse from such a system can also be sharpened by introducing non-linear elements into the forward or feedback paths. As an example, a pair of parallel-connected back to back diodes limit the output swing to 1V peak to peak since the currents are small. Further, this swing is centred on the threshold voltage which can assist in direct coupling to other stages.

Circuit description 5

A simple frequency-doubler uses a NOR gate together with a peak-selector circuit. If either of the NOR gate inputs goes above its threshold, the output goes to logic 0. This happens on positive peaks of the input via R (which serves to limit any input current for negative inputs). On negative peaks, the input of the inverter is pulled below its threshold and its output goes high. This again drives the NOR gate output to logic 0. Thus there are two negative peaks to the output during one cycle of the input, representing frequency doubling. In principle the circuit could be followed by an active filter to retrieve a sine-wave which would be available for further frequency doubling.

Further reading

Dean, J. A. & Rupley, J. P., Astable and monostable oscillators using RCA COS/MOS digital integrated circuits, RCA app. note ICAN-6267.

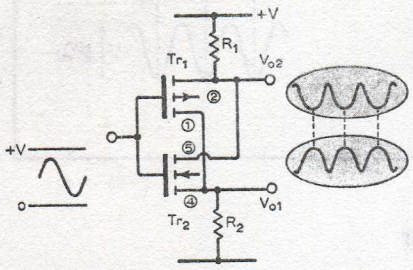
Cross references

Set 27, card 9.

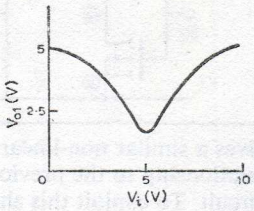
wireless world circard

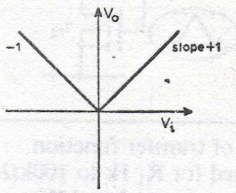
Set 27: C.m.o.s.—9

Non-linear circuits II



Typical data
IC 1/3×CD4007AE
Supply +10V
R_1 10kΩ
R_2 10kΩ
Output ≈ $V/2$ at $V_i = 0, V$ and $V/4$ at $V_i = V/2$.





Circuit description
The circuit exploits the non-linear characteristics of c.m.o.s. pairs by cross-coupling sources and drains of a single pair having a common gate. This produces the novel transfer function shown. When the input voltage is high, the p-channel device Tr_1 is non-conducting and the output voltages are determined only by the current in Tr_2. This has resistor R_2 in its source making the transfer function somewhat less than unity but with a linear slope. At all times the currents in R_1, R_2 are equal making the slopes inverse. As the input is low the reverse occurs with Tr_1 conducting, Tr_2 off. If the devices are truly complementary the output voltage would be the same at two values of input voltage, V_i and $V - V_i$. The minimum current and hence the minimum value of V_{o1} occurs for $V_i \sim V/2$. If the input is biased to this value and a sine-wave superimposed then the circuit behaves as a full-wave rectifier. This can be seen from the transfer function of an ideal full-wave rectifier in which $V_o = |V_i|$. Any other waveform can be applied, with bias offset if desired to further modify the output waveform. The output for a triangular wave input is a triangular wave of twice the fundamental frequency. In principle the process can be repeated by a.c. coupling into an identical second stage but waveform deterioration limits it to two or three stages at most.

Component changes
For anti-phase outputs $R_1 = R_2$. Values not critical and similar

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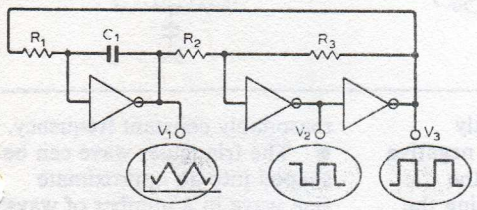
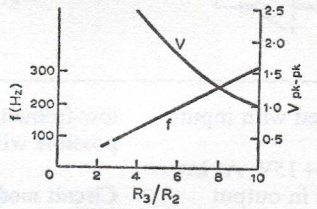
Set 27: C.m.o.s.—10

Square-triangle generator

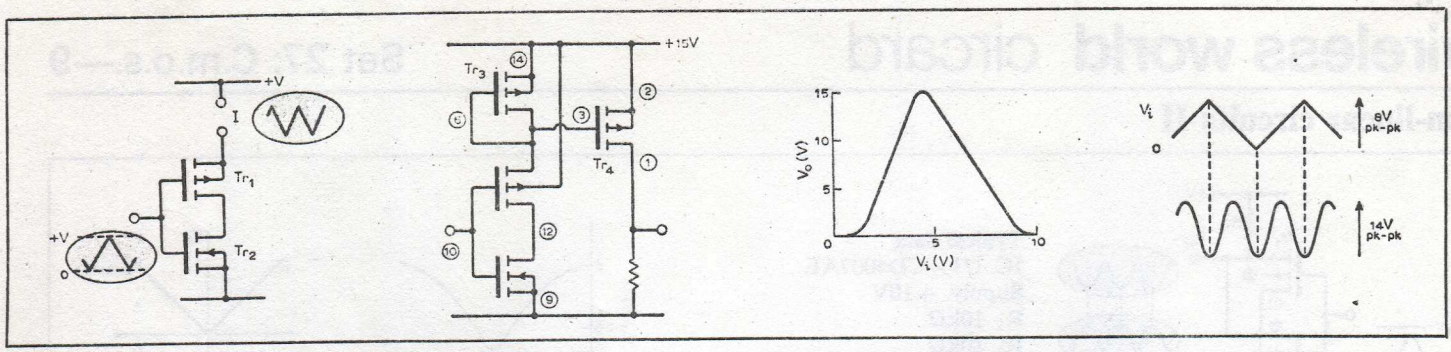


Typical performance
IC CD4007AE
Supply +10V
R_1 100kΩ
R_2, R_3 50kΩ
C_1 3.3nF



Circuit description
Since a c.m.o.s. inverter has a voltage gain of between −20 and −100 it can be employed for many of the functions usually associated with op-amps. An integrator fed with a constant direct voltage delivers a constant current to the capacitor. The output is then a linear ramp. When the gain of the amplifier is finite, the current changes with output amplitude leading to non-linearity. Even the limited gain of these inverters is sufficient to hold the non-linearity to within one or two per cent. A second limitation, that of finite input current, is not a problem with c.m.o.s. devices and the resistor values are limited only by the effects of stray capacitance on the waveforms. To make a free-running generator the ramp waveform is applied to an amplitude sensing switch—a pair of inverters with overall positive feedback suffices. The output of this switching circuit is a square-wave whose transitions coincide with the peaks of the triangular wave. Because the threshold voltage is not precisely 50% of the supply the positive and negative slopes are unequal as are the on-and-off periods of the square wave. This can be corrected as shown overleaf. There is a second square-wave in antiphase to the main output, while the frequency can be controlled without change in triangular wave amplitude by varying R_1 or C_1. Changing the ratio R_3/R_2 changes the amplitude of the triangular wave as well as the frequency. Since the slope remains the same under this change, the frequency is inverse to the amplitude.

Component changes
IC: any set of three inverters (or a single non-inverting buffer may replace the switch pair if available). NAND or NOR

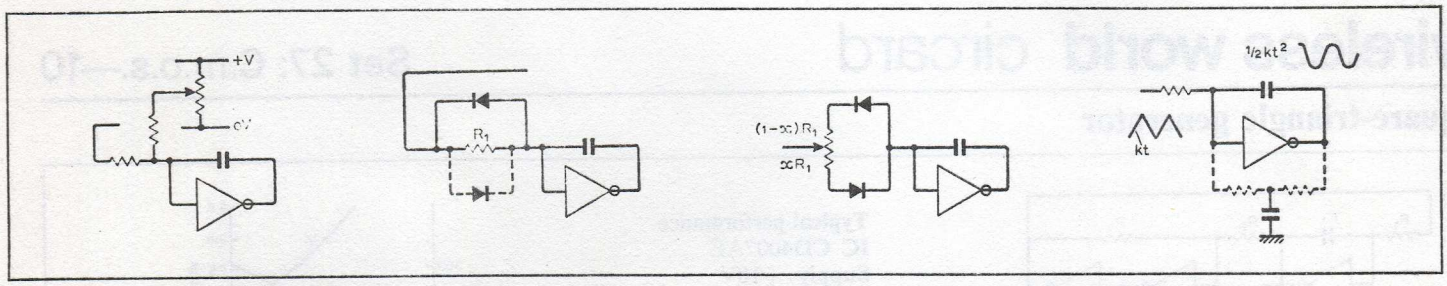


shape of transfer function obtained for R_1 1k to 100kΩ.
Supply voltage: 5 to 15V.
IC: the circuit depends on having access to both sources and drains of a complementary pair and can only be implemented with CD4007 and similar devices.

Circuit modifications

- If the current in a c.m.o.s. pair is monitored, it is found to pass through a maximum value at $V_i \approx V/2$ i.e. when both devices are about equally forward biased. At the two extremes $V_i \to 0$, $V_i \to V$ the current falls to zero. This gives a similar non-linear relationship to the previous circuit. To exploit this shape, the current can be fed to a current mirror composed of Tr_3, Tr_4. Output current flowing in R_1 passes through a peak on each excursion of V_i through the supply mid-point (with considerable variation from device to device in the actual values but all with a similar shape of transfer function). The value of R_1 depends on the supply as well as the devices but is typically 1k to 10kΩ.
- A triangular wave input gives a somewhat rounded wave output, there being no negative feedback in this circuit to linearize the transfer function.
- In addition to the above, there are a number of circuits that use the characteristics of the individual m.o.s. devices. By cancelling the threshold voltage, a close approximation to a square-law can be obtained. These will be covered in a later series of Circards.

Cross references
Set 27, cards 2, 8.



gates may be used with inputs paralleled.
Supply: +5 to +15V. At low voltages the rise in output impedance restricts the resistances to high values.
R_1: 10k to 10MΩ.
R_2, R_3: 10k to 10MΩ.
Triangular wave output should not exceed say 50% of the supply if waveform distortion is to be minimized. Hence $R_3/R_2 > 2$ is required. If the ratio is too large, the triangular wave amplitude may be too small for convenience, and switching transients more troublesome.
C_1: as low as 100pF with high values of resistance but generally 1n to 1μF. Very low-frequency triangular waves possible with this circuit.

Circuit modifications

- Many op-amp techniques can be adapted to improve or modify the output waveforms. N.B. The triangular wave has a large d.c. content being roughly centred on $V_S/2$. To change the slope a single fixed resistor may be taken from the integrator input to zero or $+V_S$. For controlled compensation, a potentiometer across the supply can be used.
- A good approximation to a sawtooth waveform follows, when R_1 is shunted by a diode. With the cathode driven by the trigger circuit, the output positive ramp is greatly speeded up while the negative ramp remains under the control of R_1. Reversing the diode gives a sharp negative edge followed by a controlled positive ramp.
- Replacing R_1 by a potentiometer and a pair of diodes, the charge and discharge cycles are varied. For equal voltage swings, one part of the cycle is proportional to xR_1 and the next by $(1-x)R_1$. The total period remains broadly constant though there are second-order effects that prevent this from being completely achieved. It gives a variable mark-space ratio to the square-wave with a reasonably constant frequency.
- The triangular wave can be shaped into an approximate sine wave in a number of ways. An amplifier can be added with non-linear elements in the forward or feedback paths. An alternative is to use a second integrator with decoupled d.c. feedback. This converts the ramps into parabolic sections which match a sine-wave reasonably well (as little as 4% t.h.d.).

Further reading
Santoni, A. & Trolese, G. Design ideas with COS/MOS, *New Electronics*, April 30, 1974, pp. 27-34.