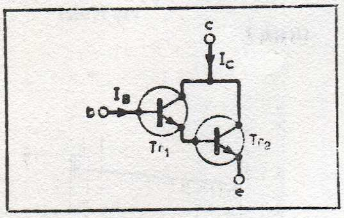
wireless world circard

Set 20: Transistor pairs—1

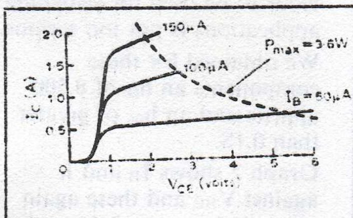
High current-gain pairs—1

Darlington pair

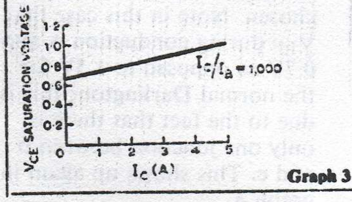


Components
Tr_1: BFR41 Tr_2: TIP3055

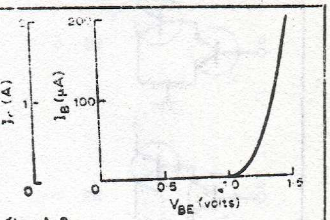
Description and characteristics
A Darlington pair as shown above is a frequently used two-transistor circuit, the purpose being to obtain high gain through cascading two transistors. Because large currents are obtained in the second transistor one frequently finds this to be a power transistor and that the arrangement is used in many switching applications.
As the circuit has only three terminals it can be regarded as a single high-gain transistor. The basic action is that I_b produces, through Tr_1, a large base drive for Tr_2. The total I_c is the sum of the two collector currents although the contribution of Tr_1 to I_c will be small if the gain of Tr_2 is large.
The characteristics obtained for the components quoted are as shown. From graph 1 we obtained an h_{oe} of about 25mS and an h_{fe} of about 11,000. Graph 2 shows an h_{ie} of around 70. These figures are in line with theory (see reference). Graph 2 also shows the dependence of I_c on I_b, the two graphs being indistinguishable because of the scales chosen.
For switching applications the value of V_{CE} is important. V_{CE}sat is defined as that V_{CE} corresponding to an arbitrarily



Graph 1

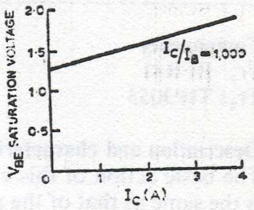


Graph 3

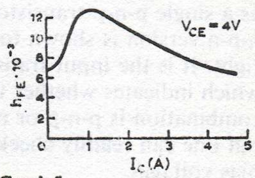


Graph 2

low I_c/I_b ratio, in this case 1,000 (graph 3). With higher I_c/I_b ratios, corresponding to lower I_B values the value of V_{CE} will be lower. The corresponding graph of V_{BE}sat. is shown in graph 4.
Graph 5 shows the dependence of h_{fe} on I_c, the drop in h_{fe} at high I_c being due to saturation and that at low I_c being due to lack of base drive to Tr_1.



Graph 4



Graph 5

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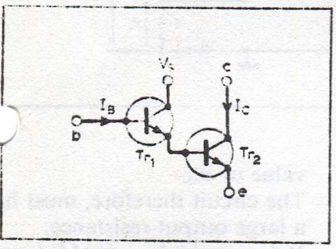
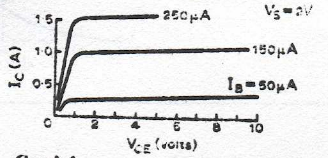
Set 20: Transistor pairs—2

High current-gain pairs—2

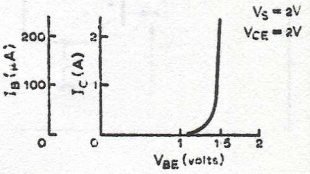


Components
Tr_1: BFR41
Tr_2: TIP3055

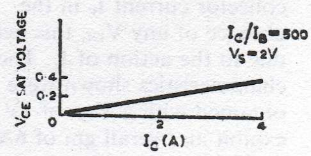
Performance and description
The Darlington circuits on card 1 are both super β circuits but have the additional charactistic that they only have three terminals and so can be regarded as a single transistor. The circuit shown above also has high gain but has four terminals, three of which can be regarded as base, emitter and collector, the fourth being connected to a voltage which gives some control over the characteristics. The principal difference in performance of this circuit is that a low saturation voltage is obtained.
From graph 1 we obtained an h_{fe} of 7,000 and an h_{oe} of 25mS for V_s=2.0V. Characteristics for V_s=4.0V are virtually identical.
Graph 3 shows the low V_{ce}sat values obtained, slightly lower values being obtained for V_s=4.0V.
Graph 4 shows the expected V_{BE}sat values around 1.5V since two base-emitter junctions are between b and e. Again slightly lower values are obtained for V_s=4.0V. The graph of h_{fe} is shown in graph 5, the figures being in line with the previously obtained h_{fe}.



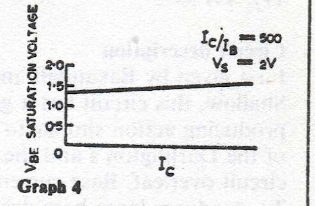
Graph 1



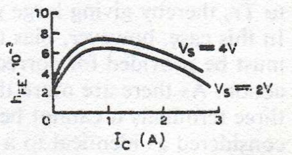
Graph 2



Graph 3



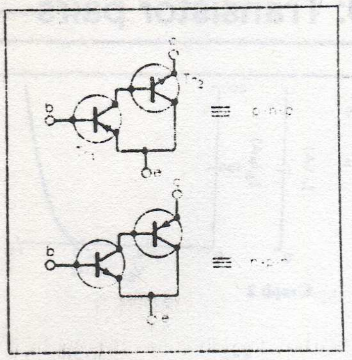
Graph 4



Graph 5

Note that in this configuration Tr_1 will have supply voltage V_s across it and will normally require a current-limiting resistor in its collector lead.

Complementary Darlington pair



Components
Tr_1: BFR81
Tr_2: TIP3055

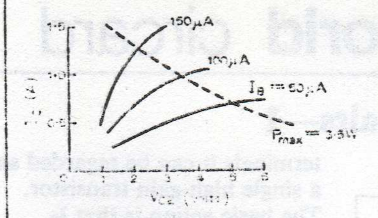
Description and characteristics
The basic action of this circuit is the same as that of the normal Darlington pair. Note that the circuit in this format is acting as a single p-n-p transistor. An n-p-n version is shown to the right. It is the input transistor which indicates whether the combination is p-n-p or n-p-n but one can readily check the bias voltages.

Graph 1 shows the output characteristics: not eminently suitable for a small-signal amplifier, but as the circuit tends to be used for switching applications is not too serious. We obtained for these components an h_{fe} of 8,500 approx and an h_{oe} of greater than 0.1S.

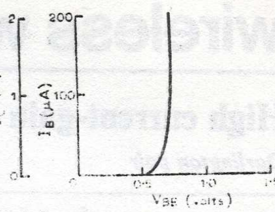
Graph 2 shows I_B and I_c against V_{BE} and these again coincide because of the scale chosen. Note in this case that V_{BE} during conduction is about 0.7V as opposed to 1.5V for the normal Darlington; this is due to the fact that there is only one junction between b and e. This shows up again in graph 4.

By the same token, the graph of V_{CEsat} (graph 3) is much the same as that for the normal Darlington.

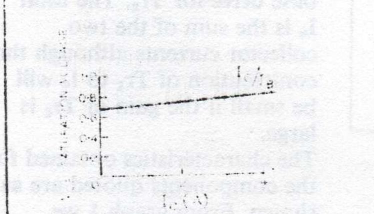
Graph 5 again has much the same shape as that for the normal Darlington though with a lower maximum value, which is in line with the reduced h_{fe}.



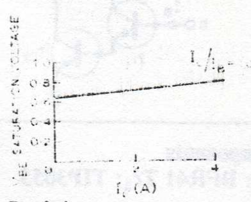
Graph 1



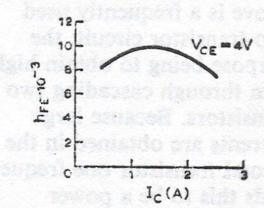
Graph 2



Graph 3



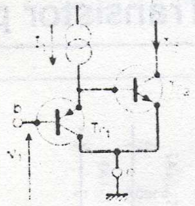
Graph 4

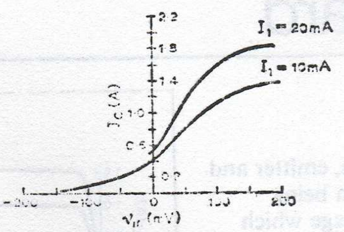


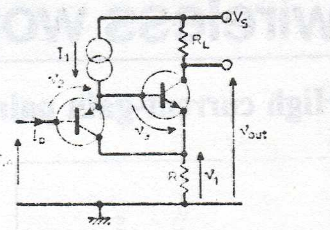
Graph 5

Further reading
Burwen, E. High-gain triple Darlington has low saturation voltage, *Electronics*, 3 Oct., 1974.

Reference
Ajdler, J. Transistor circuits, *Electronic Engineering* 1965, p.757. See also p.338 and p.112, same year.







Components
Tr_1: BFR81
Tr_2: TIP3055

Circuit description
First given by Baxandall and Shallow, this circuit has a gain producing action similar to that of the Darlington's and the circuit overleaf. Base current to Tr_1 produces large base drive to Tr_2 thereby giving large gain. In this case, however, bias (I_1) must be provided for correct action. As there are more than three terminals it cannot be considered as identical to a single transistor, and it displays some characteristics that one does not obtain with single transistors. In particular, one obtains collector current I_c in the absence of any V_{in}, this being due to the action of I_1. The characteristics shown were obtained with a V_{CE} of 1V and exhibit an overall gm of 6A/V, obtained at V_{in} of zero.

The components used were chosen for comparison with the other super β pairs but certain features would dictate other choices. For example, the circuit simulates a p-n-p transistor whilst having an n-p-n output stage. In monolithic i.cs with lateral transistors, n-p-n transistors have low gain so that Tr_1 would dictate the overall gain. As Tr_1 has a very low voltage across it, viz V_{be} of Tr_2, then Tr_1 can be made to have high gain—see MC1538R.

When used as shown above right, the circuit exhibits extremely high output resistance which, allied to the high current gain, gives large voltage gain. The reason for this is that $v_1 = v_3 + v_2 + v_{in}$ and as v_3 and v_2 cancel, both being base-emitter voltages, then $v_1 = v_{in}$ and the current in R_L is thus defined by I_1 and the current in R, no matter the value of R_2.

The circuit therefore, must have a large output resistance. Values as high as 50MΩ have been quoted.

Further reading
Baxandall, P. J. and Shallow, E. W. Constant-current source with unusually high internal resistance and good temperature stability; *Electronics Letters* vol. 2, p.351 1966.
Jarger, R. C. A high output resistance source, *IEEE Journal of Solid-State Circuits*, Aug. 1974, pp.192-4.

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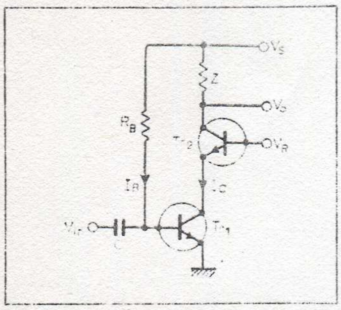
Set 20: Transistor pairs—3

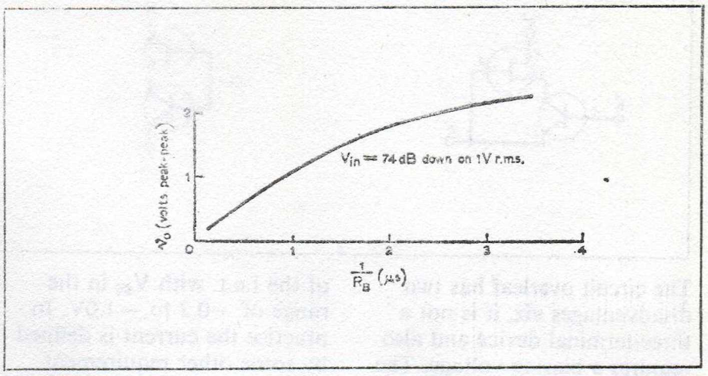
Cascode amplifier



Components
Tr_1, Tr_2: BFR41
V_s: 10V
Z: 660mH coil plus stray capacitance plus c.p.o. loading
C: coupling capacitor
R_B: see graph
V_o: see graph

Circuit description
Tr_1 is a common-emitter amplifier which is feeding Tr_2 in common-base mode. The load on Tr_1 is therefore a near short-circuit a.c.-wise. In addition, the current gain of Tr_2 is near unity but its output impedance is high, due to the common-base mode of operation. The combination therefore shows the gain characteristics of a short-circuited c.e. stage plus the output impedance characteristics of c.b. It is therefore ideally suited for the driving of tuned resonant loads or indeed of any high impedance load.

The basic equations are
$I_c = g_m V_{in}$
$I_c \approx I_L$
$g_m = I_c/26mV$
$V_o = Z_L I_L$
The second equation assumes unity current gain through Tr_2 and the last equation assumes that h_{ob} (for Tr_2) is very low.
The net result is
$V_o/V_{in} = g_m Z_L$



Since I_c is almost linearly related to I_B, particularly if V_{CE} of Tr_1 is constant which it is in this case, then g_m is controllable by R_B. The net result is the graph shown. For each result the circuit was retuned for resonance, the change in resonant frequency being of around 1.5% over the complete range.
With $R_B = 1M\Omega$, the resonant frequency was 924kHz and the bandwidth 18.5kHz giving a Q of 50. V_R is not critical—it is only required to produce correct transistor action. In these results it was 3V. A 1.5-nF supply decoupling capacitor was necessary.
Note that the graph represents a range of voltage gain from 50dB to 71dB and that the range of R_B is 20:1.

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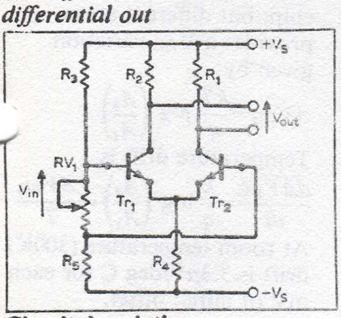
Set 20: Transistor pairs—4

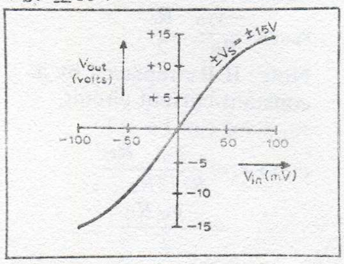
Long-tailed pair

(a) Differential in-differential out



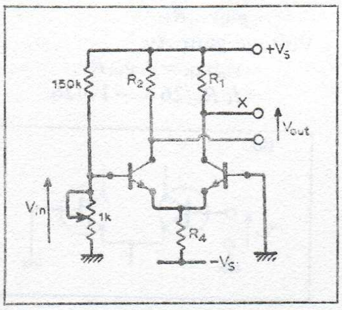
Circuit description
This emitter-coupled differential amplifier should have a large value for R_4 to provide a high common-mode rejection ratio (c.m.r.r.). This implies that the differential output voltage between collectors for a common signal at the bases, is very small and ideally zero.
In general, the output signal depends on the difference between the signals at the transistor bases. Each transistor receives half the signal i.e. the gain to each output is half of that provided by a single transistor under the same conditions.

Performance data
Tr_1, Tr_2: matched pair from CA3086. R_1, R_2, R_4: 100kΩ
R_3, R_5: 150kΩ, RV_1: 1kΩ
V_s: ±15V



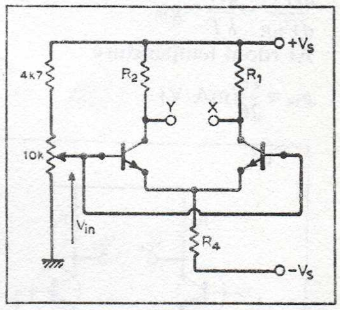
Gain slope: typically 230.
Variation in gain: ±1% for several choices of CA3086.
Reducing R_1, R_2 by similar ratios will maintain slope at same order of magnitude.

(b) Single-ended in, differential out

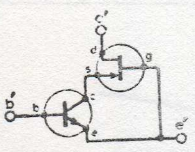


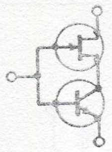
V_{in}: 10mV d.c. (20mV)
V_{out}: 2.39V d.c. (4.79V)
i.e. gain slope similar to (a)
$$\frac{\Delta V_{out}}{\Delta V_{in}} = 240$$
For single-ended output:
V_{out} = voltage between X and ground.
$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{10.28V - 9.06V}{20mV - 10mV} = 122.$$
i.e. gain is halved.

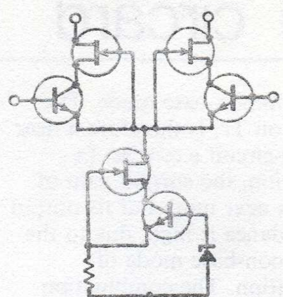
(c) Common mode input



$$\frac{\Delta V_{xy}}{\Delta V_{in}} = \frac{0.149 - 0.142}{2 - 1} = 0.007$$
For single-ended output (terminal X to ground):
$$\frac{\Delta V_{out}}{\Delta V_{in}} = 0.0045$$
c.m.r.r. improved by trimming R_1, R_2 for zero balance.
Figure of merit is c.m.r.r. or voltage gain for differential inputs divided by voltage gain for common-mode inputs that is 0.007/230.







The circuit overleaf has two disadvantages viz, it is not a three-terminal device and also requires a biasing voltage. The above circuit suffers from neither of these disadvantages. The circuit is self-biasing provided only that I_c is less than I_d by an amount sufficient that the resulting V_{gs} keeps the bipolar transistor well out of saturation. Typically V_{ce} would need to be in the range 0.2 to 1.0V (though a higher value would be preferable for higher gain). This means that the operating current is restricted to the I_d of the f.e.t. with V_{gs} in the range of −0.2 to −1.0V. In practice the current is defined by some other requirement (drift, matching etc) and is often much less than I_{dss}—the f.e.t. current with $V_{gs}=0$ (which would give no gain from the bipolar anyway). The f.e.t. will frequently be required to operate near pinch-off. The circuit, above centre, is a less common form which loses the merit of low capacitive feedback. It does, however, have the merit of increased current capability since the f.e.t. can operate with V_{gs}=0V.

The circuit right is of a form found as the input of some commercially available differential amplifiers. Each two-transistor block can be regarded as a single transistor and the circuit is then recognisable as a long-tailed pair. The tail uses the high output impedance of the pair to provide an excellent constant-current source the other two pairs being used for their high voltage gain.

Cross references
Set 20, cards 4, 10.

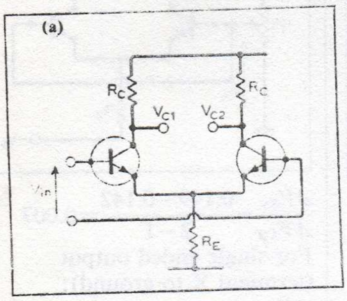
Useful relationships
Bipolar transistor collector current related to base-emitter voltage by

$$I_C \approx I_S \exp qV_{BE}/kT$$

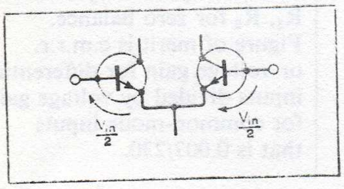
$$\frac{dI_C}{dV_{BE}} = \frac{qI_C}{kT} = g_m$$

At room temperature

$$g_m \approx \frac{I_C}{26}(\text{mA/V})$$



Differential input signal can be considered as



$$v_{C1} = -g_m \frac{v_{in}}{2} R_C$$

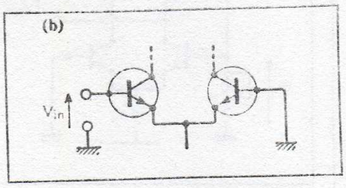
$$v_{C2} = -g_m \frac{-v_{in}}{2} R_C$$

Differential output given by

$$v_0 = v_{C1} - v_{C2}$$
$$= -g_m v_{in} R_C.$$

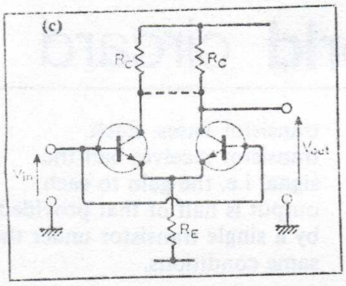
Voltage gain A_V

$$= v_0/v_{in} = -g_m R_C$$
$$= I_C R_C/26 = -V_C/26.$$



This single-ended input signal can be considered as the algebraic sum of differential and common-mode signals: i.e. $v_{in} = v_{in}/2 + v_{in}/2$ and $0 = \underbrace{v_{in}/2}_{\text{common mode}} - \underbrace{v_{in}/2}_{\text{differential mode}}$

For c.m.r.r. high, effect of common-mode signals negligible. Hence single-ended input equivalent to differential input.



For identical transistors the collectors are at equal potentials for common-mode signals. Hence they can be considered connected together

$$v_{out} \approx \frac{-v_{in}}{R_E} \cdot \frac{R_c}{2}$$

Note: If R_E replaced by a constant-current circuit, v_{out}(cm) can be $\ll 1$.

$$\text{c.m.r.r.} = \frac{-g_m \cdot R_C}{R_C/2R_E}$$
$$= \frac{-g_m R_E}{2}$$

Temperature drift
For a pair of identical transistors, balanced to provide zero difference between the base-emitter voltages of each, then the temperature drift is theoretically zero—a basic advantage of the differential mode.

$$V_{BE} \approx \frac{kT}{q} \log\left(\frac{I_c}{AT^r}\right)$$

A is dependent on transistor area. Two transistors on same chip, but different areas, provides a V_{BE} variation given by

$$\Delta V_{BE} = \frac{kT}{q} \log\left(\frac{A_2}{A_1}\right)$$

Temperature drift is

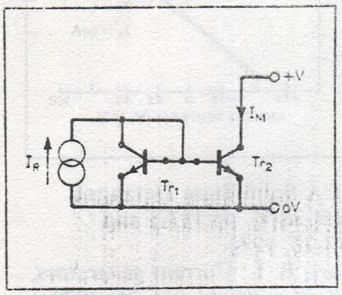
$$\frac{d\Delta V_{BE}}{dt} = \frac{k}{q} \log\left(\frac{A_2}{A_1}\right) = \frac{\Delta V_{BE}}{T}$$

At room temperature (300K) drift is 3.3μV/deg C for each mV of initial offset.

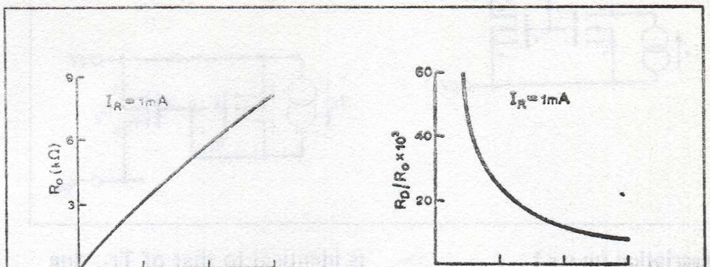
Further reading
Thermal variation of the emitter-base voltage of bipolar transistors. Widlar, R. J. *Proc. IEEE* Jan. 1967.
Limits of temperature drift in non-compensated d.c. amplifiers. *IEEE Journal of Solid-State Circuits*, Feb. 1970.

Cross reference
Set 12, card 10

Current mirrors



Typical data
Tr_1, Tr_2: part of CA3086
I_R: 1mA from commercial current generator, ±0.05%
I_M: measured using 4-digit multimeter.
Curves opposite show R_o and R_D as functions of +V.

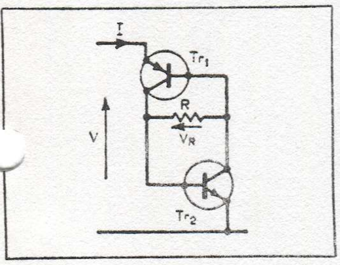


Description (bipolar)
The current mirror is an extremely useful two-transistor circuit extensively used as an integral part of monolithic operational amplifiers to define the current, the mirror current I_M, in terms of a reference current I_R. With identical transistors the base-emitter voltages are identical and if Tr_2 has a high current gain the collector currents I_R and I_M are matched, to a first order. Any matched pair of n-p-n transistors may be used but those on a single chip are preferred; the variable temperature sensitivity of discrete device reduces reliability of the circuit.
An important requirement in many applications of the current mirror is a high output resistance. The left-hand graph above shows that the static output resistance ($R_o = V/I_M$) increases with V for a given reference current value. However, the right-hand graph shows that whilst the dynamic output resistance ($R_D/\delta V/\delta I_M$) also increases with V, the far more rapid rise in R_o causes the ratio of dynamic to static output resistance to fall rapidly with increasing V. Hence, a compromise must be made between the values of R_o and R_D to be used with a given value of I_M.

For currents in the microamp range the output resistance of the current mirror can be increased by inserting a negative feedback resistor in the emitter lead of Tr_2.

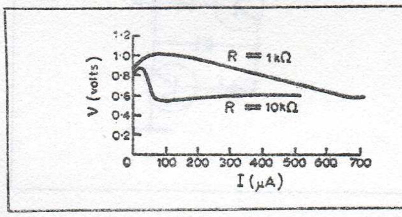
For higher current requirements, transistors on the same chip can be connected in parallel to increase the junction areas.

Complementary switching transistors



Components
Tr_1: BFR81, Tr_2: BFR41
R: 1k, 10kΩ

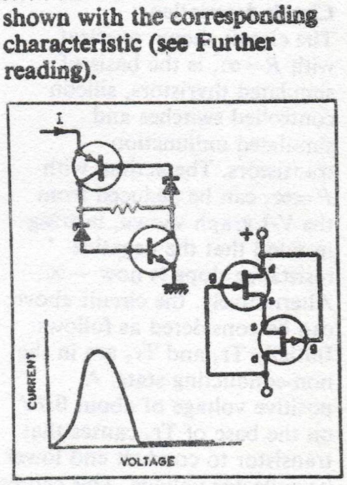
Performance
Slope in negative resistance region 0.75kΩ and 8kΩ for $R = 1k\Omega$ 10kΩ respectively (see graph).

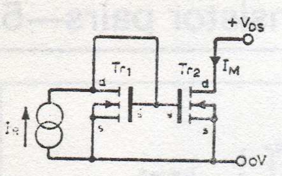


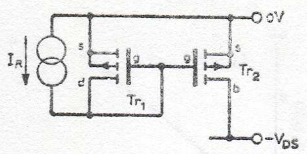
R	1kΩ	10kΩ
V_{peak}	1·05V	0·9V
I_{peak}	50μA	3μA
V_{trough}	0·65V	0·58V
I_{trough}	650μA	60μA

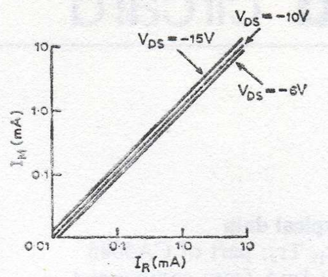
Circuit description
The arrangement of the complementary pair of transistors, with or without the resistor R, or connected between two other points, is a frequently used combination (see cross refs.). With the resistor R as shown, the circuit acts over a portion of its I-V characteristics as a negative resistance, of value $-R$ approximately. Graphs obtained are shown for values of 1k and 10kΩ.

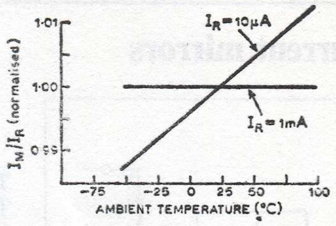
Initially with low I, V may be considered as $V_{EB_1} - V_R + V_{BE_2}$. As V_R is low initially V is the sum of the two exponential emitter-base voltages. As I increases these two voltages tend to 0.6V but V_R continues to rise and because of the minus sign V starts to fall, at a value slightly less than 1.2V. The fall continues (negative resistance region) until both transistors saturate. At this point we can no longer assume that all the current is passing through both collectors and R and we are best to view V as being $V_{EC_1} + V_R + V_{CE_2}$. Since the two transistor voltages are relatively fixed, V then starts rising again. The value of the trough is given by $V_{EC_1}\text{sat} + V_{BE_2}\text{sat} \approx V_{BE_2}\text{sat}$.
The voltage range of the circuit is readily increased by the modification shown opposite with Zener diodes appropriate to the application.
These circuits are described as being open-circuit stable, i.e. for any current drive there is a unique voltage. The dual of this is the voltage driven, short-circuit-stable device. An f.e.t. realization of this is shown with the corresponding characteristic (see Further reading).







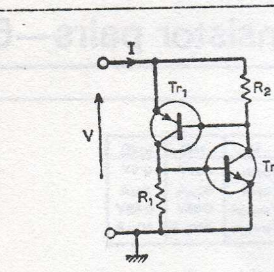


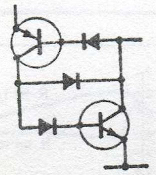


Description (m.o.s.)
Current mirror circuits can also be produced using m.o.s. transistors, the basic form using n-channel devices shown above left. Transistor Tr_1 is diode-connected performing as a transistor with 100% feedback. Thus its drain current is still controlled by its gate-source voltage V_{GS}, i.e. $I_D \approx g_{ss} V_{gs}$ where g_{ss} is the forward transconductance. Forcing a current I_R into this diode-connected transistor causes V_{GS} to rise until a state of equilibrium is attained when Tr_1 sinks the reference current. The gate-source voltage of Tr_2 is identical to that of Tr_1, due to the parallel connections. Hence if both have identical characteristics, Tr_2 is also capable of sinking an identical current, the mirror current I_M. A reasonably good degree of matching can be obtained between the n-channel devices on a monolithic chip, the mirror current being typically within 10% of the reference current.
A current mirror using monolithic p-channel i.g.f.e.ts, shown centre left, provides better performance than the n-channel type due to the ability to provide much closer matching of the characteristics of p-channel devices. Such a circuit provides an I_M/I_R ratio which is to a first order independent of V_{DS}, as shown centre right.
The graph above right shows that the normalized ratio of I_M/I_R is within 1% of its nominal value over a wide range of ambient temperatures and I_R values.

Further reading
Jaeger, R. C. High output resistance current source, *IEEE Journal of Solid-State Circuits*, pp.192-4, August, 1974.
RCA Solid State Databook SSD-201B, pp.183-8 and 213-25, 1974.
Hart, B. L. Current generators, *Wireless World*, vol. 76, 1970, pp.511-4.
Hart, B. L. Exdirectional current source, *Electronics Eng.* pp.39-41, July, 1974.

Cross references
Set 3, card 9.
Set 6, card 4.
Set 9, card 5.
Set 10, cards 1, 3, 7.
Set 12, cards 4, 7.
Set 15, card 6.
Set 16, card 1.
Set 20 card 0.





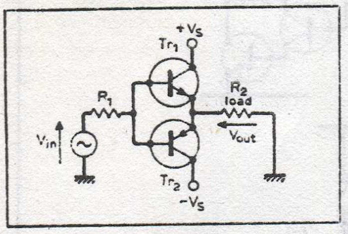
Circuit description
The circuit shown overleaf, with $R=\infty$, is the basis of simulated thyristors, silicon controlled switches and simulated unijunction transistors. The action, with $R=\infty$, can be deduced from the V-I graph shown, bearing in mind that the negative resistance slope is now $-\infty$. Alternatively, the circuit above can be considered as follows. Initially Tr_1 and Tr_2 are in the non-conducting state. A positive voltage of about 0.7V on the base of Tr_2 causes that transistor to conduct and lower its collector voltage. This causes Tr_1 to conduct and providing Tr_1 and Tr_2 produce sufficient current through R_2 and R_1 respectively to keep the transistors conducting, then the action is self-sustaining with a voltage of approximately one V_{BE} across the circuit. The circuit can thus be used as a switch, triggered by a suitable voltage at either base. With $R_1=R_2=1k\Omega$ a value of 1.3mA for I was found to be the minimum which would maintain conduction. This value is as expected as the current I will split fairly evenly between Tr_1 and R_1 and Tr_2 and R_2. Since approximately 0.65V is required at the base of each transistor to maintain conduction, it will be provided by 0.65mA in each path.
For high-speed switching it is important to prevent the transistors from saturating. Addition of the anti-saturation diodes shown prevents the collector voltages from dropping below V_{BE}. The base lead diodes are not essential.
Increasing R_1 increases the trigger voltage necessary and reduces the effect of trigger point transients.
Transients in the supply line give rise to false triggering due to rate effect. This can be reduced as R_2 is reduced although this increases the holding current necessary.

Further reading
G.E. Transistor Manual.
Sharma, S. M. Current-controlled negative resistance circuit. *Int. J. Electronics*, 1974, vol. 37, pp.209-18.
Negative resistance shown in dual f.e.t. device, *Electronics*, April 18, 1974, p.5E.

Cross references
Set 10, card 5.
Set 8, card 3.
Set 6, card 9.
Set 3, card 4.

wireless world circard

Complementary emitter-follower



Typical data
V_S: ±6V
T_1: BFR41, T_2: BFR81
R_1: 330Ω, R_2: 1kΩ
Signal frequency: 1kHz
Fundamental/3rd harmonic output/input shown on graphs

Circuit description
The basic circuit comprises a complementary n-p-n/p-n-p pair operating under class-C bias, and is the basis for many audio power/amplifiers. When a positive-going input signal exceeds about 0.7V, transistor Tr_1 will turn on, increasing its collector current which develops a voltage across the load R_2, but with a voltage gain of less than unity. At the same time Tr_2 is biased off. Similarly, a negative-going input signal turns Tr_2 on and Tr_1 off, and the circuit thus provides bidirectional currents through the emitter load. The base-emitter diode characteristic is non-linear at low voltages, resulting in cross-over distortion (approximately $2V_{BE}$) across the load. The resulting distortion on a sine wave input is shown in Fig. 1. Without an additional bias network, the effect of this distortion can be minimized by ensuring that $V_S \gg V_{BE}$. Using both positive and negative power supplies permits operation down to zero frequency. For a single supply a capacitor is required in series with the load, to provide the base and collector currents of Tr_2 during negative-going input signals.

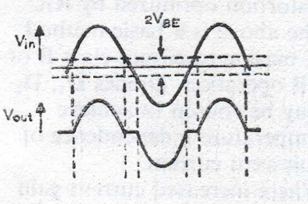


Fig. 1

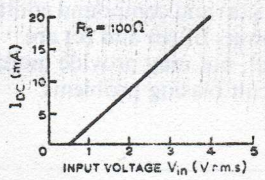


Fig. 2

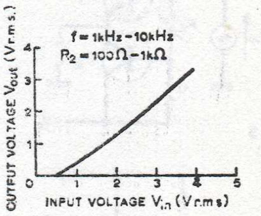


Fig. 3

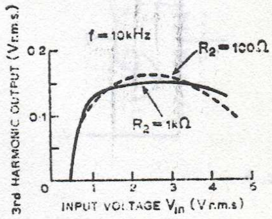
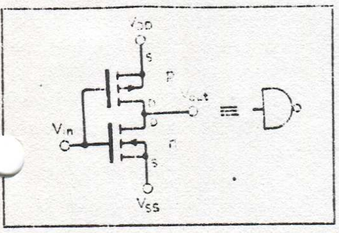


Fig. 4

Component changes
R_2: Range from 100 to 1kΩ. Variation in gain minimal.
Frequency: Up to 30kHz, little difference from lower frequency operation.
Variation of mean current with input level in Fig. 2.
R_1: Chosen to suppress parasitic oscillations. Alternative may be to keep interconnections very short to minimize series inductance.

wireless world circard

CMOS circuits



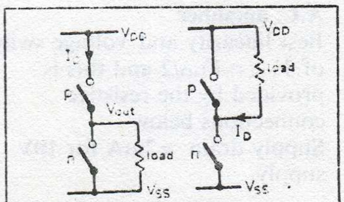


Fig. 1 Fig. 2

Description
The c.m.o.s. inverter shown above comprises a p-type and n-type enhancement mode m.o.s. transistor on the same chip. $V_{DD} - V_{SS}$ may be in the range 3 to 15V. The pair is useful in digital circuits because of well-defined threshold that V_{in} must exceed before the device turns on.
n-type: V_{GS} positive for ON
p-type: V_{GS} negative for ON
Where the output has to sink or source current, the pair can be envisaged as the series switches. Fig. 1 is a source condition, obtained for $V_{in} = V_{ss}$ and $V_{out} = V_{dd} - I_d R_o$ where R_o is the output resistance of p-transistor in the on state. For $V_{in} = V_{od}$, the n-type sinks current for Fig. 2; $V_{out} = I_d R_o$.
Basic i.c. package CD4007 contains one inverter and two complementary pairs with the drains unconnected. This permits a variety of interconnections: n-types are paralleled to increase sink current capability, Fig. 3. p-types are paralleled to increase source current capability, Fig. 4.

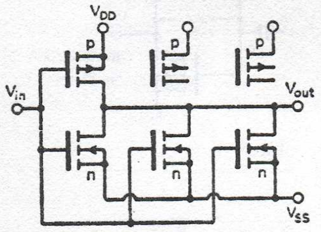


Fig. 3

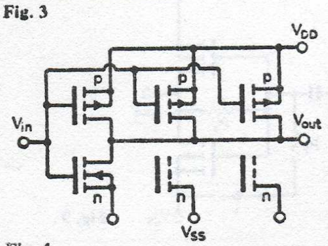


Fig. 4

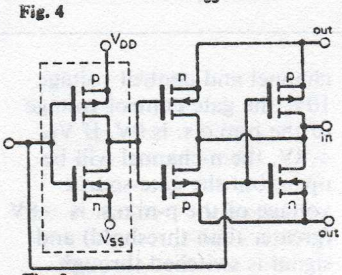
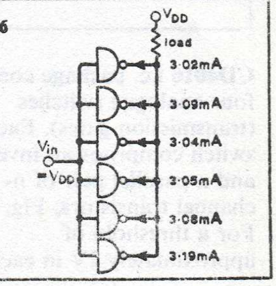


Fig. 5

Fig. 5 is a dual bi-directional transmission gate where the two outputs and input may be interchanged for two inputs and one output. Note that the position of the transistors in the middle pair have been reversed.
The CD4049 package contains six inverters with current drive capability almost an order of magnitude greater than basic package. Parallel connection for increasing current sinking indicates typical current sharing for d.c. condition, Fig. 6.

Fig. 6



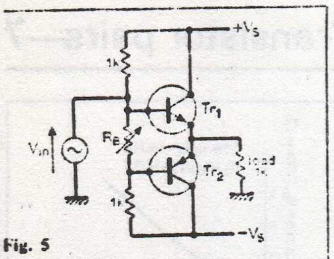


Fig. 5

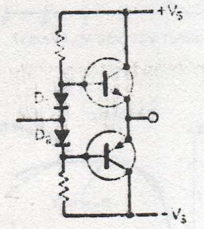


Fig. 6

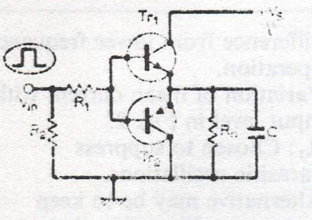


Fig. 7

Effect of bias (Figs. 5 & 6)
R_B varied until transistors just on the point of conduction. Graph shows 3rd harmonic distortion optimized by R_B.
The above is a basic method of biasing to ensure class B or AB operation. Diodes D_1, D_2 may be chosen to achieve temperature independence of quiescent current.
Where increased current gain is needed for high power outputs, the Darlington pair of Fig. 8 (a) and compound emitter followers of (b) and (c) are useful, but may provide more difficult biasing problems.

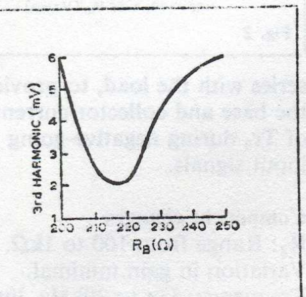
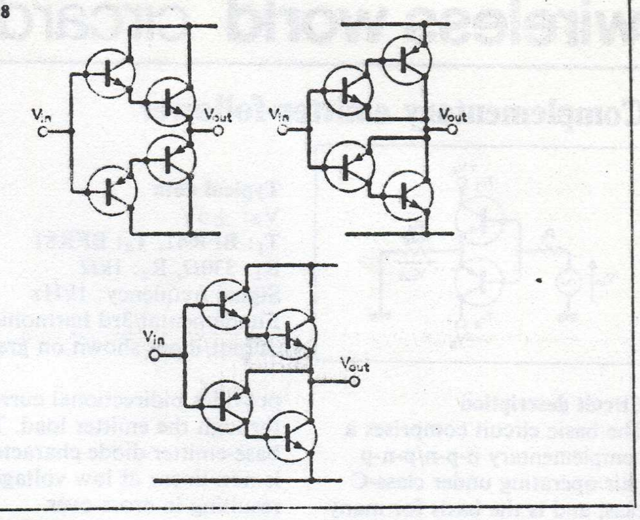


Fig. 8



Line driver (Fig. 7)
Driving 50-Ω cable with line capacitance slows pulse edges. Improved using complementary pair. Typical: fall time ⩾100ns but dependent on simulated cable capacitance (R_o: 50Ω, C: 3nF, t_F: 75ns).

Further reading
Williams, P. Voltage following. *Wireless World*, Sept., 1968.
Williams, G. E. Practical transistor circuit design and analysis, McGraw-Hill 1973.
Markus, T. Electronic circuits manual, McGraw-Hill.

Cross references
Set 7, cards 1, 3.
Set 20, card 1.

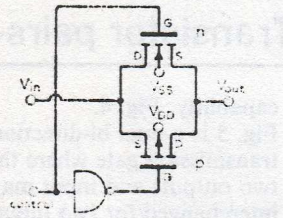


Fig. 7

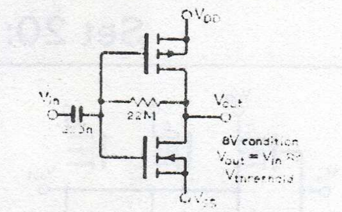


Fig. 8

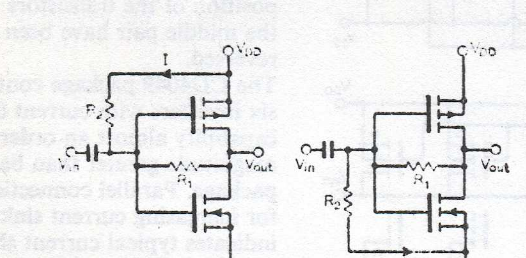


Fig. 9

CD4016 i.c. package contains four analogue switches (transmission gates). Each switch comprises an inverter and a parallel pair of n- and p-channel transistors, Fig. 7. For a threshold of approximately 2V in each channel and control voltage 10V, the gate control voltage of the p-m.o.s. is 0V. If V_{in} > 8V, the n-channel will be open, but the gate-source voltage of the p-m.o.s. is −8V (greater than threshold) and signal is switched through because the V_{GS} of each transistor never equals the threshold of the transistors, the full supply range can be switched through.

A.C. amplifier
Best linearity and voltage swing of $V_{out} = V_{DD}/2$ and this is provided by the resistive connections below
Supply drain ≈2mA for 10V supply.

Further reading
RCA Solid-State Databook Series SSD—203A 1973.
Design Ideas with COS/MOS *New Electronics*, April 30, 1974.
I.C. op-amp has CMOS output *Electronics*, Sept. 19, 1974.
Fitchen, F. C. and Ellerbruch, V. G. Linear operation of the MOSFFT complementing pair, *IEEE Journal of Solid-State Circuits*, Dec., 1971.

Cross references
Set 8, card 1.
Set 10, card 7.
Set 11, card 5.
Set 12, card 1.

Triples & mixed pairs

The principle of using transistors in pairs can often be usefully extended to the use of devices in triples, the resulting equivalent transistor having a current gain equal to the product of those of the individual transistors. In all such arrangements, two of which are shown above, the equivalent transistor has the same "polarity" as the input transistor.

The three n-p-n transistors in Fig. 1 act as a compound emitter-follower having a current gain of approximately h_{fe}^3, for large h_{fe}, and is useful for driving currents of several amps from a driver stage delivering less than a milliamp.

The complementary transistor triple in Fig. 2 is useful in voltage regulators as a low-dissipation series element, the V_{BE} and V_{CE} values of the equivalent transistor being the lowest possible for a triple. In this arrangement the temperature coefficient of only one transistor affects the output. The operating current in the input transistor will be very small, reducing its current gain. This effect can remove much of the benefit of using a triple instead of a pair. By using resistors as shown in Fig. 3 the operating currents in the earlier stages are increased and stabilized.

Thinking of the various pairs of devices discussed on other cards as elementary building blocks can prove a powerful method of developing more complicated circuit functions. For example, a long-tailed pair Tr_1, Tr_2 and Tr_3 may be used to drive a current mirror Tr_4 and Tr_5 as shown in Fig. 4 to produce a waveform generator which provides a symmetrical triangular output when driven by input pulses. This circuit uses the long-tailed pair to

Fig. 1

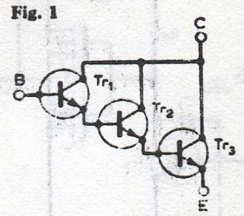


Fig. 2

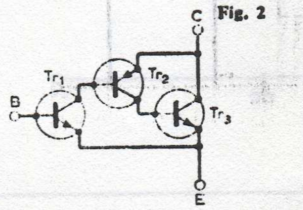
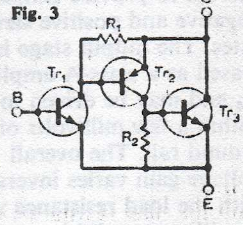


Fig. 3



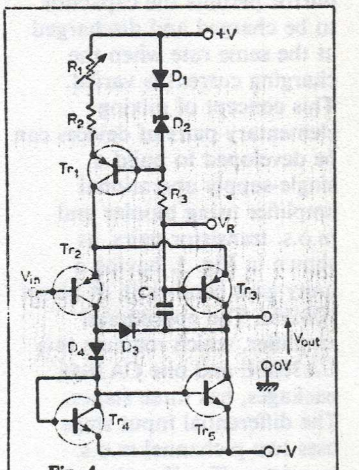


Fig. 4

Typical values. Supply ±10V, V_R 0V, R_1 5kΩ, R_2 2·2kΩ, R_3 4·7kΩ, C_1 33nF, D_1 1N914, D_2 1N5234, D_3, D_4 HP5082-2800, Tr_1, Tr_2, Tr_3 2N3546, Tr_4, Tr_5 $\frac{1}{2}\times$SL301-A.

Pot pourri

n-n-p/p-n-p simulation at high voltage

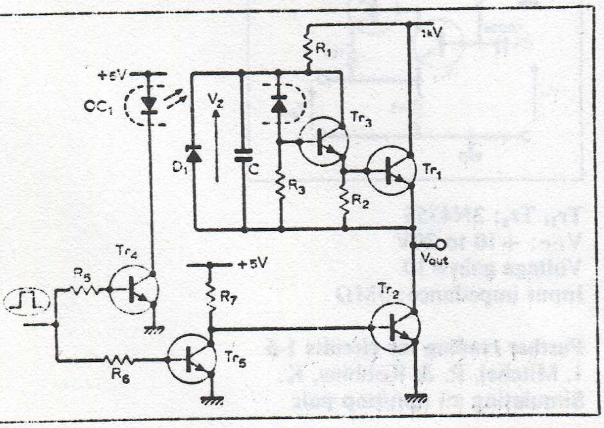
Optical couplers are used to provide fast high voltage switching with a simulated complementary pair. Transistors Tr_1 and Tr_2 are high-voltage n-p-n types: Tr_1 is on when Tr_2 is off and vice versa. With Tr_1 off, C charges to V_Z, storing charge. This is used to turn Tr_1 on fast when the optical coupler operates.

Optical coupler provides the polarity inversion when Tr_4 and Tr_5 are driven by 5V pulses.

Tr_3, Tr_4, Tr_5: 2N2222
R_1: 270kΩ (10W), R_2: 1kΩ
R_3: 100Ω, R_4: 47Ω R_5
R_6: 680Ω, C: 10nF
D_1: 6.8V zener, $OC1$: Monsanto MCO1

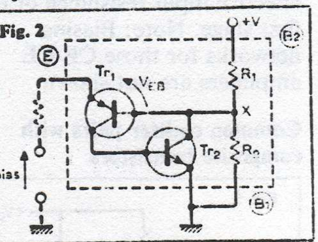
Rise and fall times of around 2μs are claimed for components used.

Fig. 1



Unijunction from bipolar pair

Fig. 2



Tr_1: 2N4126, Tr_2: 2N4124
R_1, R_2: 4.7kΩ, V: +3 to 25V

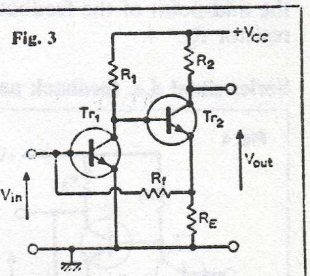
Because the collector current of Tr_1 is the base current of Tr_2 and vice versa, then any change of current provides a positive feedback action.

B_1, B_2 and E are the equivalent unijunction terminals. When E is open-circuit $V_X = R_1V/(R_1+R_2)$.

When the potential at E exceeds V_{EB} and V_X, both transistors saturate, and R_2 is short-circuited. This condition is maintained for a potential at E down to $V_{EB}+V_{CE}$sat of Tr_2. Switching speed depends on maximum frequency of of operation of the transistors. For Tr_1, Tr_2 silicon drift of $V_{EB}<3$mV/deg C.

Shunt-series d.c. feedback pair

Fig. 3



Current fed back via R_f is proportional to Tr_2 collector current, and thus the circuit provides current-shunt switch a defined current into two paths; which combined with a closely-matched current mirror permits the capacitor to be charged and discharged at the same rate when the charging current is varied. This concept of mixing elementary pairs of devices can be developed to build a single-supply operational amplifier using bipolar and m.o.s. transistor pairs, as shown in Fig. 5, having a unity-gain bandwidth of about 10MHz. The operational amplifier, which requires two CA3600E and one CA3046 packages, has three stages. The differential input stage uses two p-channel m.o.s. transistors Tr_3, Tr_4, the second stage uses an n-p-n bipolar transistor Tr_7 and the output stage is a complementary m.o.s. transistor pair Tr_8, Tr_9. The zener network, using two diode-connected transistors D_1, D_2 of the CA3046, feeds a p-channel current mirror Tr_1, Tr_2 that establishes a 400μA constant current in the input

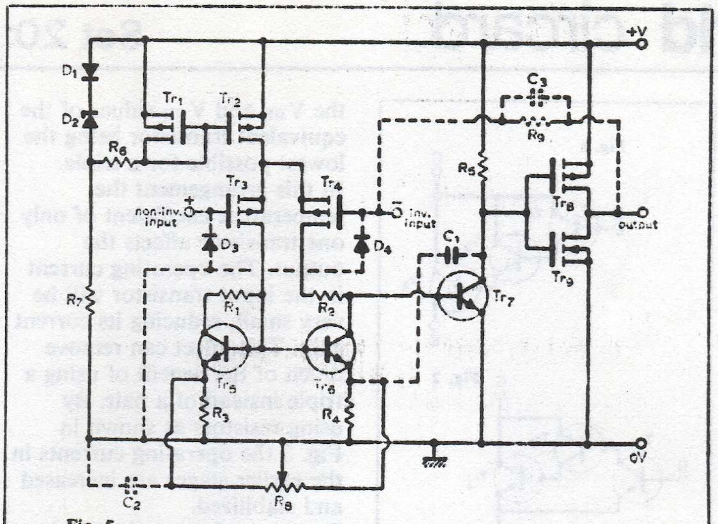


Fig. 5

stage. This differential-input amplifier is loaded by four resistors, R_1 to R_4, and a bipolar current mirror, Tr_5, Tr_6, to provide optimum balance, any voltage offset being nulled with the potentiometer R_8. The current in the second stage, determined by R_5, is adjusted to equal the 400-μA first-stage current to provide similar negative and positive slew rates. The output stage is biased as a class-A amplifier by R_5 and may be driven to within a few millivolts of the ground rail. The overall voltage gain varies inversely with the load resistance which, as with a monolithic operational amplifier, would have a value of about 2kΩ. Compensation requires inclusion of the feedback capacitor C_1, with C_2 added when using the operational amplifier as a unity-gain follower. In this configuration, R_9 and C_3 should be added to avoid the possibility of latch up and D_3 and D_4 added to the inputs to prevent negative-going input signals exceeding about 700mV which could also cause latch up. Typical values are: V+15V; R_1, R_2, R_3, R_4 200Ω±1%; R_5 20kΩ±1%; R_6 11kΩ±1%; R_7 7.5kΩ±1%; R_8 10kΩ; R_9 1kΩ; C_1 39pF; C_3 300pF; C_3 150pF; D_3, D_4 1N914.

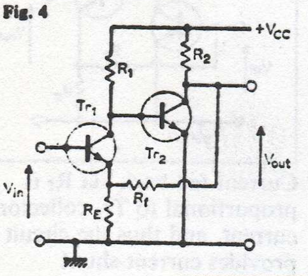
Further reading

Williams, P. Voltage Following, *Wireless World*, vol. 74, 1968, pp. 295-8.
Nowicki, J. R. Compound transistor connections, *Electronic Engineering*, September, 1971, p.63.
Burwen, E. High-gain triple Darlington has low saturation voltage, *Electronics*, Oct. 3, 1974.

negative feedback, which primarily controls the overall current-gain.
Effective current gain is $A_i/(1+\beta A_i)$ where A_i is the current gain of the two stages, with R_f connected between Tr_1 base and ground. $\beta \approx R_E/R_f$.
For $\beta < 0.1$, input resistance is $R_i/(1+\beta A_i)$ where R_i is input resistance without feedback.
Voltage gain $\approx \frac{R_f}{R_E} \cdot \frac{R_2}{R_S}$
where R_S is source resistance. Voltage gain can be increased by by-passing R_E, or by-passing the mid-point of the feedback resistor R_f.

Series-shunt d.c. feedback pair

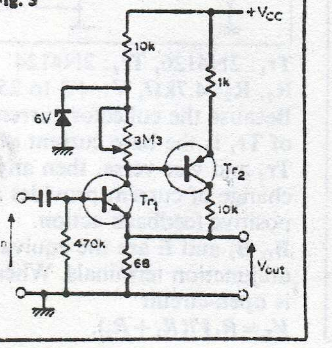
Fig. 4



In this connection, the voltage gain is now mainly affected by the feedback, and the input resistance is increased. Voltage gain is $A_v/(1+\beta A_v) \approx 1/\beta$ if A_v is large. A_v is the product of the gains of each stage, with R_F connected from Tr_2 collector to ground, and $\beta = R_E/R_F$. Input resistance is $R_i(1+\beta A_v)$, where R_i is effective input resistance of the first stage. Note: Biasing networks for those CE-CE amplifiers are not shown.

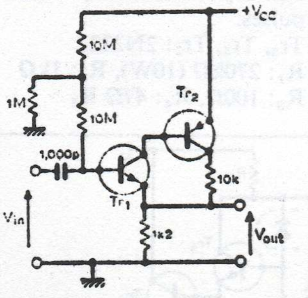
Common emitter pairs with composite transistors

Fig. 5



Tr_1, Tr_2: 2N4355
V_{CC}: 15 to 30V
Voltage gain ≈ 100
Cut-off frequency ≈ 10kHz
Input resistance > 200kΩ
By sacrificing voltage gain, a high input impedance can be obtained with the circuit shown below.

Fig. 6



Tr_1, Tr_2: 2N4355
V_{CC}: +10 to 30V
Voltage gain ≈ 10
Input impedance: 5MΩ

Further reading for circuits 1-6

1. Mitchel, P. & Robbins, K. Simulating an npn/pnp pair for high voltage switching. *Electronics*, Aug. 22, 1974.
2. Shyne, N. A. Bipolar pair simulates unijunction, *Electronics*, Jan. 24, 1974.
3, 5, 6. Cowles, L. G. Transistor circuit design, Prentice-Hall, 1972.
4. Millman & Halkies, Electronic Devices and Circuits, McGraw-Hill, 1967, p.502.

Cross references
Set 20, cards 6, 7.
Set 12, card 9.