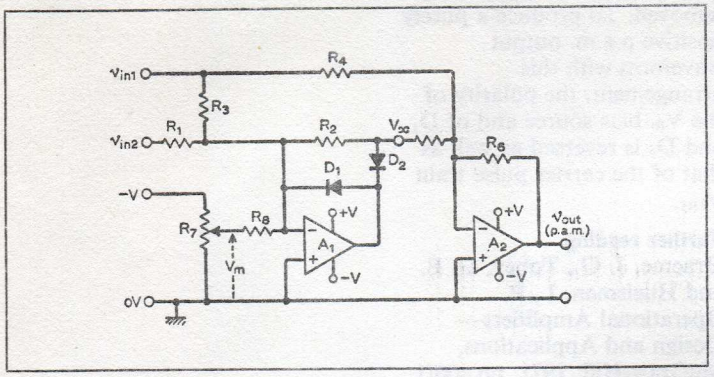
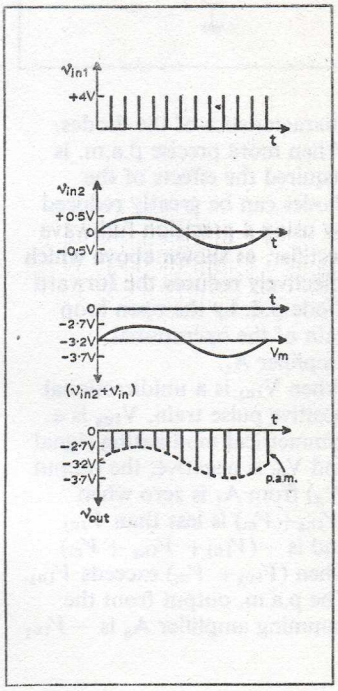
Pulse amplitude modulator with precision limiter



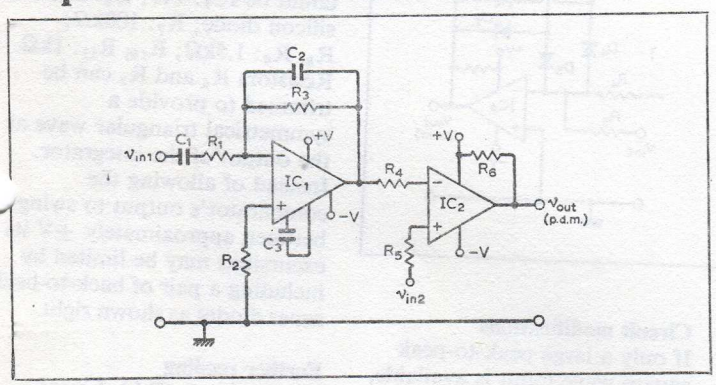
Typical performance
Supply: ±15V, +3.4mA, −17mA
A_1, A_2: 741
R_1 to R_6, R_8: 10kΩ; R_7: 1kΩ linear
D_1, D_2: PS101
V_{in1}: 4-V positive pulse train, p.r.f. 10kHz, m-s ratio 1:10
V_{in2}: 1-V pk-pk sinewave, f = 1kHz
V_m: −3.2V
V_{out}: p.a.m. output—see diagrams



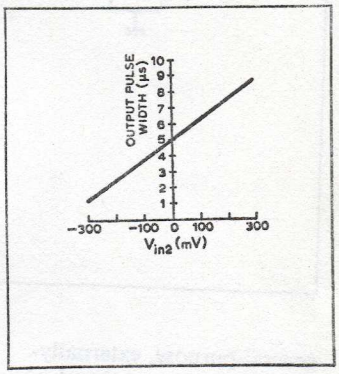
Circuit description
In most pulse amplitude modulator realizations the unmodulated carrier is in the form of a low duty-cycle, unidirectional pulse train. So with a symmetrical modulating signal the amplitude of the carrier pulses may be varied over the maximum range of zero to twice their unmodulated value with 100% modulation. The narrower the carrier pulses the greater the conservation of power but this is achieved at the expense of a wider transmission bandwidth for defined performance, as the shape of the pulse tops must be preserved.

A common method of producing p.a.m. is by the use of a diode bridge that allows and prevents transmission of the modulating signal under the control of a carrier switching pulse train. For many applications this technique is acceptable although its accuracy is determined by the

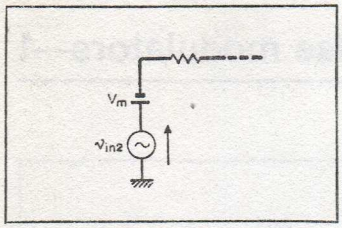
IC pulse duration modulator



Typical performance
Supply: ±15V, ±12mA
IC_1: 748, IC_2: 311
R_1, R_2, R_4, R_5: 1kΩ
R_3: 100kΩ, R_6: 2.2kΩ
C_1: 33nF, C_2: 1nF, C_3: 30pF
V_{in1}: 400mV pk-pk square wave at 100kHz
V_{out}: 28V pk-pk



Circuit description
In pulse width modulation, the unmodulated pulse train is often in the form of a square wave having a constant pulse repetition rate. The duty cycle of this square wave is then varied under the control of a d.c. or low-frequency modulating signal. The source waveform of the carrier signal may take various forms, e.g. a sinewave which is converted to a square wave for application to an integrator and comparator. The integrator converts the square wave to a triangular wave which is applied to one input of the comparator. In the absence of modulation, which is applied to the other input of the comparator, the output is a periodic pulse-train or square wave having a fixed duty cycle.
With a modulating signal applied to the second comparator input, the duty cycle of the output pulse train varies in sympathy with changes in the modulating waveform's instantaneous value, as the comparator's output state changes when the modulation input level exceeds or falls below that of the square wave applied to its other input.
The above diagram shows an integrated circuit version using a voltage comparator and a



characteristics of the diodes. When more precise p.a.m. is required the effects of the diodes can be greatly reduced by using a precision full-wave rectifier, as shown above which effectively reduces the forward diode p.d. by the open loop gain of the operational amplifier A_1.

When V_{in1} is a unidirectional positive pulse train, V_{in2} is a symmetrical modulating signal and V_m is negative, the output (V_x) from A_1 is zero when ($V_{in2}+V_m$) is less than V_{in1} and is $-(V_{in1}+V_{in2}+V_m)$ when ($V_{in2}+V_m$) exceeds V_{in1}. The p.a.m. output from the summing amplifier A_2 is $-V_{in1}$ when $V_x = 0$ and is ($V_{in2}+V_m$) when V_x is less than zero.

Component changes

Useful range of supply about ± 4 to ± 18V with suitable adjustment of V_{in1}, V_{in2} and V_M levels.
V_{in1} (max): 7.5-V pulses
V_{in1} (min): 3.5-Vpulses
V_M (max): 3.6V
V_M (min): 2.8V
Max. p.r.f. of V_{in1}: 70kHz (mark-space ratio of approximately unity required to retain output p.a.m. waveshape).

Circuit modifications

To produce a wholly positive pulse amplitude modulated output waveform instead of a purely negative output, the following changes should be made: V_{in1} is changed to a unidirectional negative pulse train, diodes D_1 and D_2 are connected with reverse polarity and R_7 is connected to the positive supply rail.

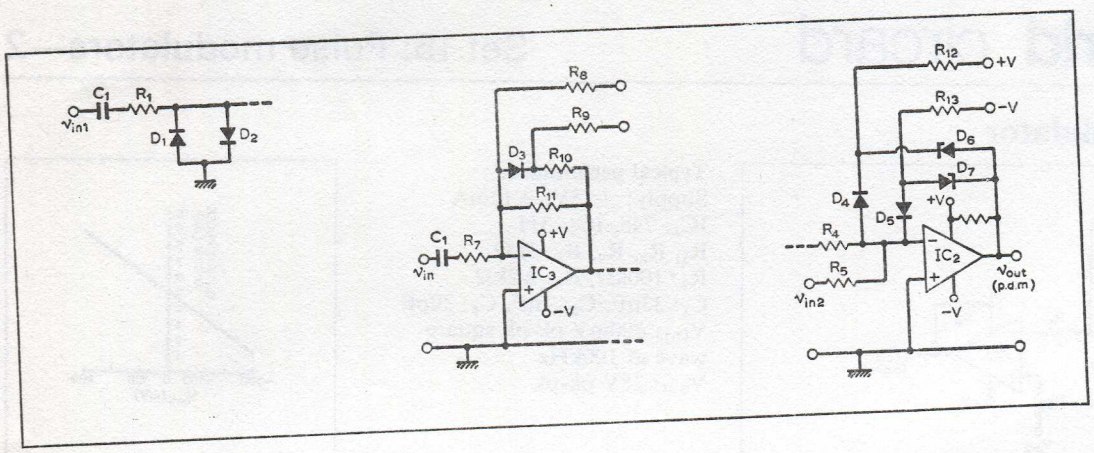
With a negative p.a.m. output signal the alternative biasing arrangement shown above may be used, i.e. a d.c. bias source can be connected in series with the modulation source, V_{in2}, and R_7 and R_8 removed. To produce a purely positive p.a.m. output waveform with this arrangement, the polarity of the V_m bias source and of D_1 and D_2 is reversed as well as that of the carrier pulse train V_{in1}.

Further reading

Graeme, J. G., Tobey, G. E. and Huelsman, L. P. Operational Amplifiers—Design and Applications, McGraw-Hill, 1971, pp.400/1.
Applications Manual for Operational Amplifiers, Philbrick/Nexus, 1965.
Cattermole, K. W., Transistor Circuits, 2nd edition, Heywood 1964.

Cross references

Series 15, cards 3 & 7.
Series 4, card 3.



general-purpose, externally-compensated operational amplifier for the integrator. Capacitor C_1 removes any d.c. component from the input square wave and R_8 provides d.c. negative feedback to define the mean output voltage of the triangular wave. The overall linearity obtainable is a function of the linearity of the triangular waveform applied to the comparator.

Component changes

Supply variation: ± 2.2 to ± 18V
$f_{max} \approx$ 200kHz with components shown. Change integrator time constant for different carrier p.r.fs. Unidirectional pulse width modulation can be produced by feeding the integrator with a train of narrow pulses and hence a sawtooth is applied to the comparator.

The comparator may be fed directly from a triangular or sawtooth wave source.

Circuit modifications

If only a large peak-to-peak square wave input is available, the input to the integrator may be clamped using a pair of back-to-back diodes (PS101, 1N914, etc.) as shown left.

When the available carrier source waveform is in the form of a sine wave it may be converted to a suitable form for application to the integrator by the circuit shown centre which amplifies and clips the output signal applied to the integrator. The input coupling capacitor of the original integrator can be dispensed with. Suitable components could be IC_3: 741; D_3: small silicon diode; R_7: 100kΩ; R_8, R_9: 1.5kΩ; R_{10}, R_{11}: 1kΩ. Resistors R_8 and R_9 can be trimmed to provide a symmetrical triangular wave at the output of the integrator. Instead of allowing the comparator's output to swing between approximately $\pm$V its excursions may be limited by including a pair of back-to-back zener diodes as shown right.

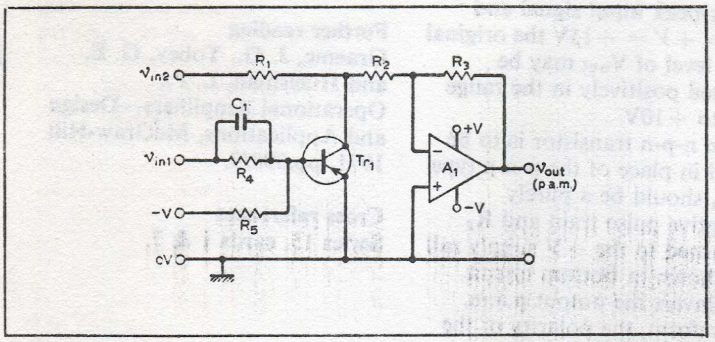
Further reading

Eimbinder, J. (Ed.), Linear IC's: Theory and Applications, Wiley, 1968, pp.15-7.
Graeme, J. D. and Tobey, G. E., Operational Amplifiers. McGraw-Hill, 1971, pp.412/3.

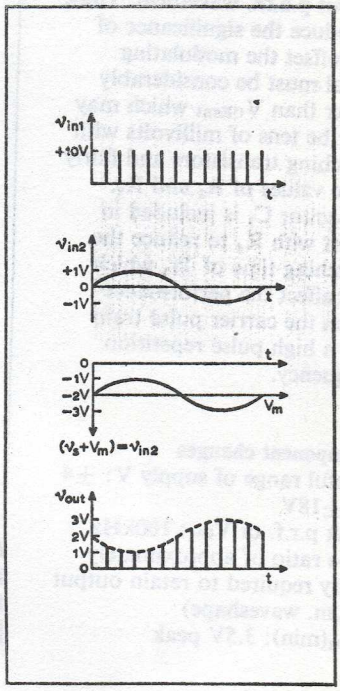
Cross references

Series 15, cards 4, 6, 7, 8, 10 & 11.
Series 2, card 1.
Series 3, card 1.

Pulse amplitude modulator with shunt gate

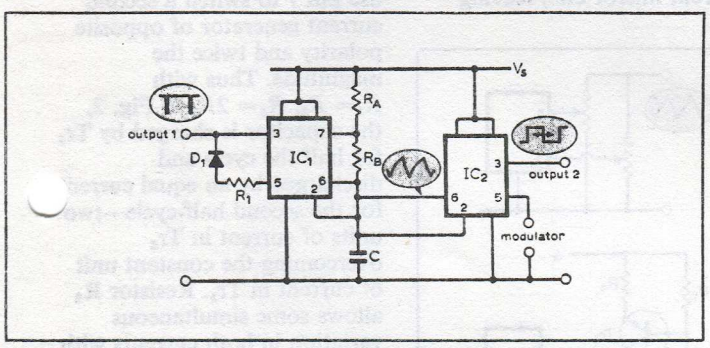


Typical performance
Supply: ±15V
A_1: 741; Tr_1: BC126
R_1, R_2: 5kΩ; R_3, R_4: 10kΩ
R_5: 33kΩ
C_1: 22pF
V_{in_1}: 10-V positive pulse train, p.r.f. 10kHz, m-s ratio 1:10
V_{in_2}: modulation input ($V_S + V_M$)
V_S: 2V pk-pk 1kHz sinewave superimposed on bias V_m
V_m: −2V

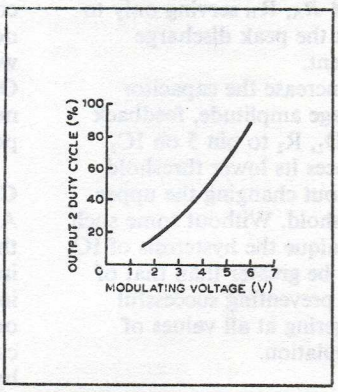


Circuit description
Diagram shows a pulse amplitude modulator using a shunt transistor to gate the modulating signal, superimposed on a suitable d.c. bias, applied to the input of the inverting operational amplifier.
The modulating signal is thus only presented to the amplifier when Tr_1 is switched off under the control of the low duty-cycle carrier pulse train applied to its base via R_4. This pulse train is wholly positive and must be of sufficient amplitude to overcome the continuous base drive provided from the negative supply rail via R_5.
When the modulating signal is allowed to pass to the operational amplifier it is inverted and appears at the output amplified by the factor $R_3/(R_1+R_2)$. When Tr_1 is switched on, the voltage appearing at the junction of R_1 and R_2 is the saturation voltage of Tr_1 which is amplified by the factor R_3/R_2. With $R_1 = R_2$ and $(R_1+R_2)=$

Pulse duration/position modulator

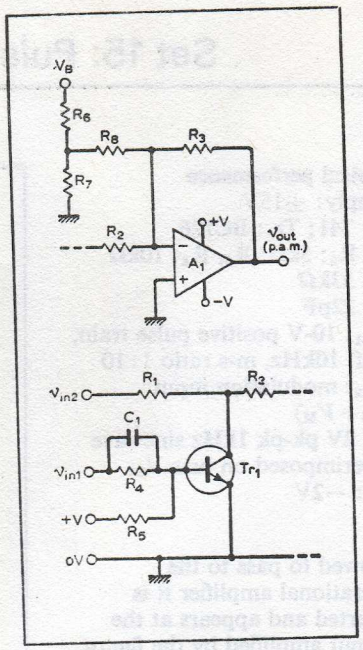


Typical performance
Supply: +10V
IC_1, IC_2: NE555V
R_A: 100kΩ, R_1: 680Ω
R_B: 330Ω, D: 1N914
C: 10nF
f: 980Hz
output 1: negative pulse, duration 7μs
output 2: positive-going edge synchronized to output 1
negative-going edge delayed by 0.31ms for $V_{mod} = +3V$



Circuit description
If a waveform of defined shape but variable frequency is applied to a circuit with defined upper and lower threshold voltages, then the output of that circuit will be a pulse waveform whose leading and trailing edges are defined in position. The relative positions of the waveforms then remain unaffected by the frequency of the generator provided its waveform is frequency independent. For a triangular or similar waveform both edges of the output can be modulated while for a sawtooth waveform one edge of the output is fixed and the other alone is modulated.
Independent modulation of frequency and duty cycle may be achieved as in the circuit shown. IC_1 is an astable based on the 555 timer with R_A+R_B setting the rise-time and R_B the fall-time (since the junction of the two resistors is grounded via pin 7 as the capacitor potential reaches the upper threshold). If the capacitive waveform is applied directly to the corresponding pins on IC_2, then variation of the threshold voltages of IC_2 modulates its output. By applying this voltage to pin 5 which sets the upper and lower threshold voltages in a 2:1 ratio by means of an internal potential divider both thresholds are varied. For one edge of output 2 to retain its position relative to output 1, the fall time of the capacitor voltage should be a small portion of the total time so

R_3, V_{in2} receives a gain of unity and V_{CEsat} a gain of 2. Ideally, V_{CEsat} is zero but is finite in practice so that an offset will be introduced to the output p.a.m. waveform. Thus, to reduce the significance of this offset the modulating signal must be considerably larger than V_{CEsat} which may only be tens of millivolts with switching transistors and fairly large values of R_1 and R_2. Capacitor C_1 is included in shunt with R_4 to reduce the switching time of Tr_1 which will affect the performance when the carrier pulse train has a high pulse repetition frequency.



Component changes
Useful range of supply V: ±4 to ±18V
Max p.r.f. of V_{in1}: 100kHz (m-s ratio of approximately unity required to retain output p.a.m. waveshape)
V_{in1}(min): 3.5V peak
V_m(max): 9V
V_m(min): 1V
V_s(max): 10V pk-pk, with $|V_m| \approx 5.3V$

Circuit modifications
The p.a.m. output waveform may be made to occupy a different voltage range by the addition of the resistor network shown at top. Using a 2V peak-peak input signal and $V_B = +V = +15V$ the original 0-V level of V_{out} may be shifted positively in the range 0V to +10V
If an n-p-n transistor is to be used in place of the p-n-p type V_{in1} should be a purely negative pulse train and R_5 returned to the +V supply rail as shown in bottom circuit.
To invert the output p.a.m. waveform, the polarity of the d.c. bias on which the modulating signal is superimposed should be reversed.
The gating function performed by the bipolar transistor can instead be performed by a field effect transistor. An advantage obtained from this change is a reduction of the offset in the p.a.m. waveforms introduced when the device is in the 0-V state. However, the direct capacitive feedthrough of the switching transients may be worse with an f.e.t. than with a bipolar transistor.

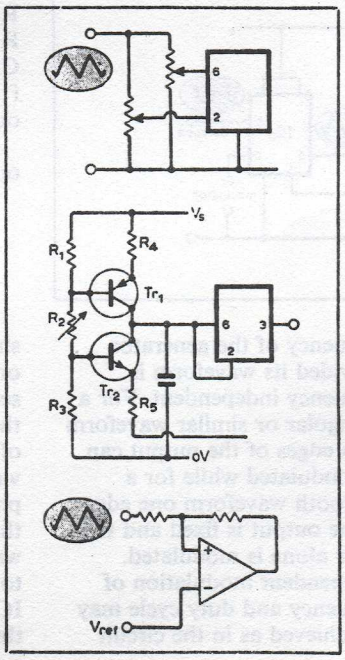
Further reading
Graeme, J. G., Tobey, G. E. and Huelsman, L. P., Operational Amplifiers—Design and Applications, McGraw-Hill 1971, pp.398/9.

Cross references
Series 15, cards 1 & 7.

variation of the lower threshold of IC_2 hardly affects the instant of the corresponding output 2 transition. This calls for $R_B \ll R_A$, R_B serving only to limit the peak discharge current.
To increase the capacitor voltage amplitude, feedback via D_1, R_1 to pin 5 on IC_1 reduces its lower threshold without changing the upper threshold. Without some such technique the hysteresis of IC_2 may be greater than that of IC_1, preventing successful triggering at all values of modulation.

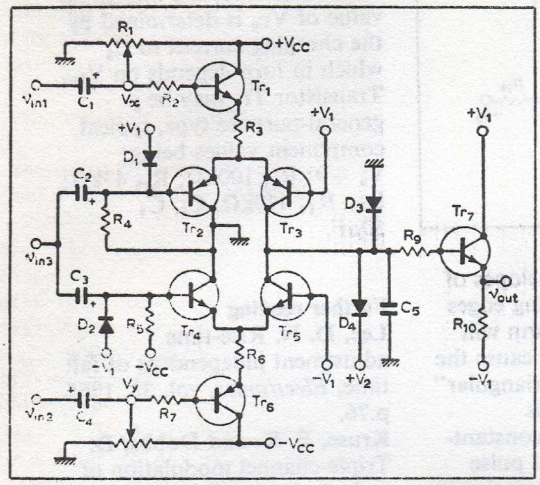
Component changes
IC_1, IC_2: 555 timer is available from Signetics, Motorola (MC1455) or in dual form from Exar (XR2556).
C: sets basic frequency range, $f = 1/0.6C(R_A+2R_B)$ for R_1 absent. Low values of R_1 increase both rise and fall-times. 100pF to 100μF
R_A: 1k to 10MΩ
R_B: 1k to 10MΩ
R_1: 220Ω upwards
D_1: General-purpose silicon diode
V_s: 4.5 to 18V
Modulation may be capacitively coupled to pin 5 on IC_2 if normal threshold levels suit the waveform applied to pins 6 & 2. Otherwise apply via resistive network to modify mean potential on pin 5 to suit.

Circuit modifications
As in Series 13, card 5, the thresholds may be varied independently by applying the input waveform through one or two potential dividers. This can be used to narrow the hysteresis from $V_s/3$ towards zero with the penalty that the potential dividers load the source, e.g. with 1k to 100kΩ values the waveform could not be taken directly across the capacitor of IC_1 on original circuit without severe limitations being placed on R_A, R_B.
The main modification that might be required would be the linearizing of the modulation, by replacing the resistors with constant-current sources (i.e. providing a linear variation of capacitor voltage against time). For a linear ramp, replace R_A by a constant-current stage (current mirror etc.) leaving R_B as a low value to minimize the fall-time. If a triangular-wave is required, for modulation of both pulse edges, then one method is to use pin 7 to switch a second current generator of opposite polarity and twice the magnitude. Thus with $R_1 = R_3$, $R_4 = 2R_5$ in Fig. 2, the capacitor is charged by Tr_1 for half the cycle and discharged by an equal current for the second half-cycle—two units of current in Tr_2 overcoming the constant unit of current in Tr_1. Resistor R_2 allows some simultaneous variation in both currents with little effect on their ratio, but the voltages across R_4, R_5 should be $< V_s/3$.
The method is of general applicability to any switching circuit having variable thresholds as in the op-amp circuits with positive feedback.

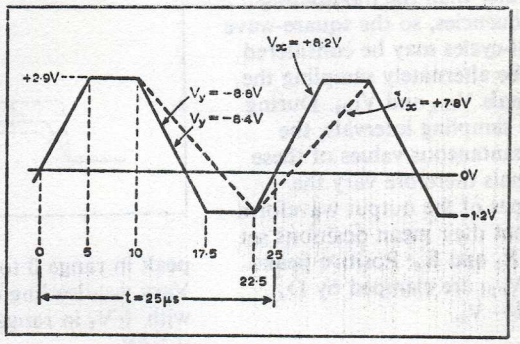


Cross references
Series 15, cards 2, 6, 7, 8, 10 & 11.
Series 3, card 9.

Variable slope modulator

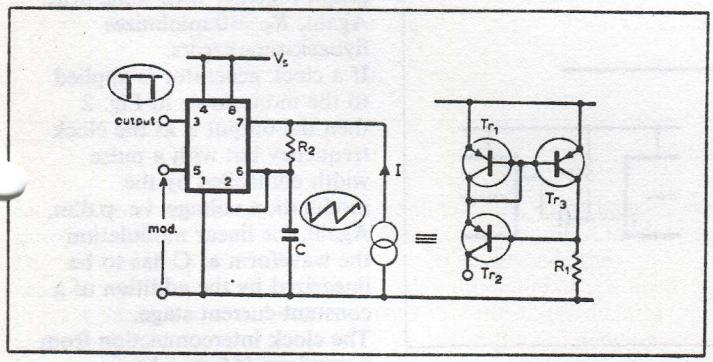


Typical performance
Supplies: ±25V, +2mA, −5mA
±V_1, ±6V, +14mA, −13mA
+V_2 = +3V, 14mA
Tr_1, Tr_4, Tr_5, Tr_7: BC125
Tr_2, Tr_3, Tr_6: BC126
Diodes: PS101; R_1, R_4, R_8, 10kΩ
R_2, R_7: 2.7kΩ; R_3, R_6: 1.5kΩ
R_5: 27kΩ
R_9: 100Ω; R_{10}: 820Ω
C_1 to C_4: 50μF
C_5: 1nF; V_x +8.2V
V_y −8.8V
v_{in3} 1V pk-pk square wave, p.r.f.: 40kHz
See v_{out} waveform opposite for v_{in1} and v_{in2} available range

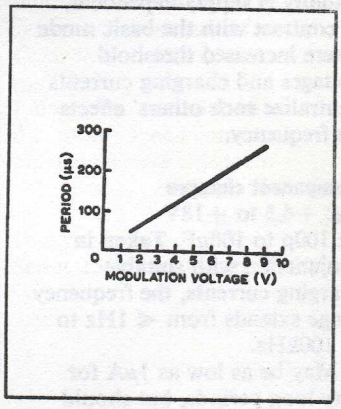


Circuit description
When a capacitor is charged or discharged with a constant current, the p.d. across it changes linearly with time. In the circuit shown the unmodulated output pulse train is in the form of a trapezoidal wave having the same p.r.f. as the input square wave (V_{in3}) and having leading and trailing edge slopes determined by V_x and V_y respectively.
When V_{in3} goes positive, Tr_3 is switched on and passes the constant current from Tr_1 to charge C_5. The magnitude of this current, and hence the rate of rise of V_{C5}, is set by R_1 and is linearly related to V_x.
When V_{in3} goes negative, Tr_5 discharges C_5 with a constant current through Tr_6. The magnitude of this current is set by R_8 and is linearly related to V_y.
Thus the slopes of the leading and trailing edges of the pulse-train output waveform from

Pulse modulation using 555 timer

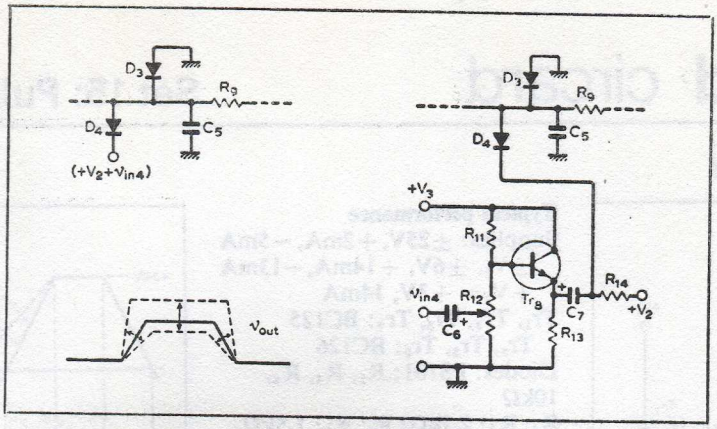


Typical performance
IC: NE555V
Supply: +12V
C: 4.7nF
R_2: 1kΩ, I = 100μA*
v_{mod}: 5V
Period: 150μs
Output: Duration of low-state 6μs, for load resistance 1kΩ
*Current may be provided by any constant-current circuit; that shown is one example for which Tr_1 to Tr_3 are elements of IC type CA3084; R_1=47kΩ.



Circuit description
Modulation of pulse period or repetition-rate may be carried out independently by control of the threshold voltages or the charging rate of the timing capacitor in astable circuits.
In the 555 timer a constant-current charging C gives a linear ramp. Upper threshold is equal to the potential at pin 5, v_{mod}, and the lower threshold to $v_{mod}/2$ by virtue of the internal potential divider. The capacitor is thus charged through $v_{mod}/2$ at a constant rate, giving a period that is a linear function of the modulation potential provided that the discharge time is very short. This indicates a low value for R_2, which may be reduced to zero (except where large values of C would result in the 200mA current limit of the discharge transistor being exceeded for long periods).
The constant current is critical to the linearity, since for the usual astable with a resistor from pin 7 to V_s, the charging rate varies throughout the cycle. For example, as v_{mod} approaches V_s the fractional increase in period is greater than that of the modulation voltage. One possible constant-current circuit is the enhanced current mirror. This requires a low terminal p.d. for the constant-current transistor Tr_2, i.e. the constant-current stage does not impose a limit on the upper

the emitter follower Tr_7 are controlled by V_x and V_y respectively, which can be made to vary independently by sources of modulation V_{in1} and V_{in2}. The p.r.f. of the carrier pulse train V_{in3} is much greater than the modulating frequencies, so the square-wave half-cycles may be considered to be alternately sampling the signals V_{in1} and V_{in2}. During the sampling intervals, the instantaneous values of these signals therefore vary the slopes of the output waveform about their mean positions set by R_1 and R_8. Positive peaks of V_{out} are clamped by D_4 and $+V_2$.



Component changes

v_{in1} (max) = v_{in2} (max) ≈ 760mV (1kHz)
Minimum frequency of v_{in1} and v_{in2} < 10Hz
v_{in3} (min) ≈ 700mV pk-pk
Max. p.r.f. of v_{in3} ≈ 200kHz with C_8 = 47pF
Min. duty cycle of v_{in3} 30%
Min. load resistance ≈ 220Ω
Vary $+V_2$ to set v_{out} positive peak in range 0 to +3.5V
Vary v_{out} leading edge slope with $+V_1$ in range +3 to +6.6V
Vary V_{out} trailing edge slope with $-V_1$ in range −6 to −7.5V
Reduce R_3 to reduce rise time of v_{out}
Reduce R_6 to reduce fall time of v_{out}

Circuit modifications

If the dynamic range of the modulating signals is restricted, the variations in the slopes of the leading and trailing edges of the output waveform will never be sufficient to cause the latter to assume a "triangular" pulse shape. With this restriction, V_{out} is a constant-amplitude trapezoidal pulse train with its positive peaks clamped by D_4 at $+V_2$. Hence, a third signal (V_{in4}) may be superposed on the $+V_2$ supply to provide trapezoidal-pulse amplitude modulation as shown left with V_{out} assuming the variations indicated below the circuit. One method of modulating the clamp voltage is shown right which uses an emitter-follower. All channels are no longer independent of each other since the maximum value of V_{C5} is determined by the charging current to C_5 which in turn depends on V_{in1}. Transistor Tr_8 may be a general-purpose type, typical component values being: V_3 +9; R_{11} 100kΩ; R_{12} 47kΩ; R_{13}, R_{14} 470kΩ; C_6, C_7 50μF.

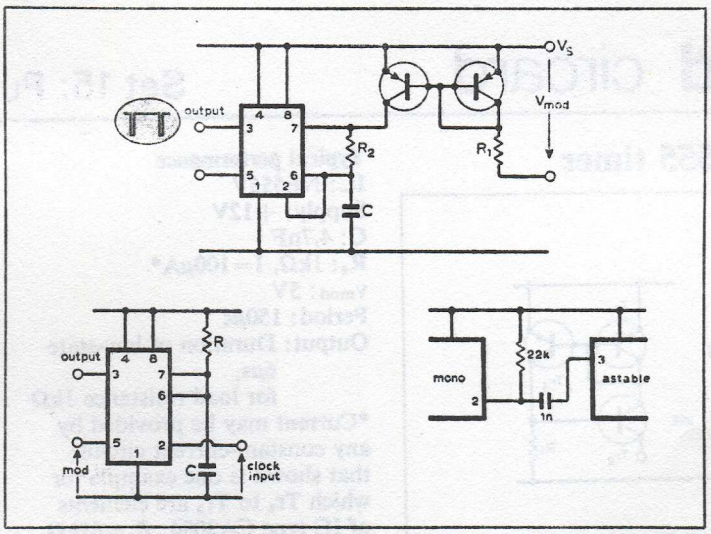
Further reading

Lee, D. N. Rise-time adjustment independent of fall time, *Electronics*, vol. 38, 1965, p.76.
Kruse, E. K. and Dobbs, D. Triple-channel modulation of a single pulse train. *Electronic Engineering*, April 1971, pp.36/7.

Cross reference

Series 15, card 7.

threshold/modulation voltage that can be used. Since the charging current is proportional to the supply voltage (ignoring V_{be} effects) the frequency stability is supply-dependent, in contrast with the basic mode where increased threshold voltages and charging currents neutralize each others' effects on frequency.



Component changes

V_S: +4.5 to +18V
C: 100p to 100μF. Taken in conjunction with suitable charging currents, the frequency range extends from ≪ 1Hz to > 100kHz.
I: May be as low as 1μA for very long periods, but should exceed 10μA for reasonable stability of period. Up to 10mA permissible for high frequency generation.
R_2: Should limit discharge current at pin 7 to 200mA. May be reduced to zero for low values of C in most cases, though peak currents exceed this rating for very short times. This reduces duration of low-state of output towards zero.
V_{mod}: For V_S of 12V, v_{mod} may range from 1.5 to 9V. The minimum value is of the same order at other supply voltages, while the upper is about 70% of V_S or greater for V_S > 10V. At low supply voltages internal V_{be} drops restrict the range further.

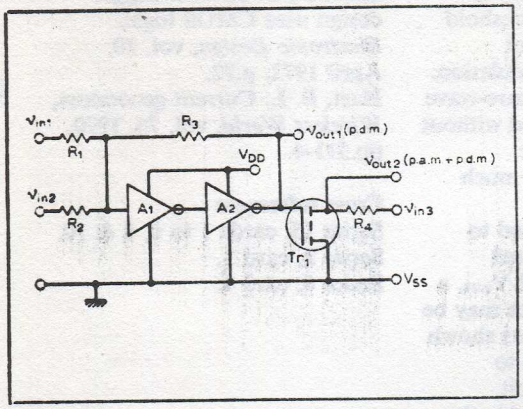
Circuit modifications

In circuits based on capacitor charging to define the period of the waveform, then constant current charging linearizes the waveform and, for defined switching points, the period will be inverse to the current, i.e. the frequency will be a linear function of the current. A simple adaptation is to apply the modulation to the current generator—a simpler current mirror is shown as an example with the diode p.d. introducing an offset to the v_{mod}/frequency graph together with some drift. Again, $R_2 \rightarrow 0$ minimizes flyback-time errors.
If a clock generator is applied to the monostable in Fig. 2 then the output is at the clock frequency but with a pulse width controlled by the modulation voltage, i.e. p.d.m. Again, for linear modulation the waveform at C has to be linearized by the addition of a constant-current stage.
The clock interconnection from a previous 555 may be as shown. The circuit may be conveniently implemented with a dual 555, but any other astable giving a negative-going edge approaching supply-voltage magnitude may be used.

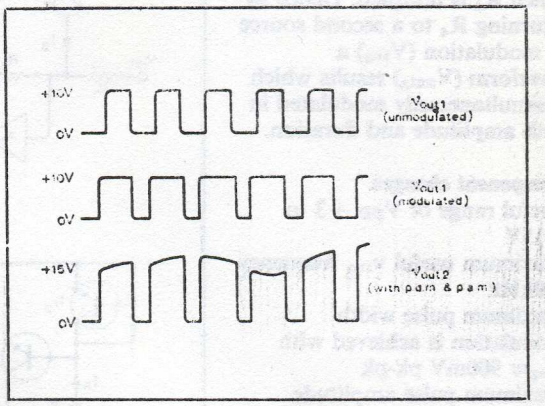
Cross references

Series 15, cards 2, 4, 7, 8, 10 & 11.
Series 3, card 9.

CMOS pulse amplitude/duration modulator

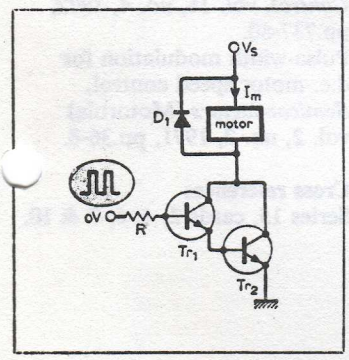


Typical performance
V_{DD}: +10V, 830μA; V_{SS}: 0V
A_1, A_2: ¼×CD4007
Tr_1: 1/6×CD4007; R_1, R_2: 1MΩ
R_3: 10MΩ; R_4: 10kΩ
v_{in1}: 11V pk-pk 50kHz triangular wave superposed on +2.1V d.c. bias to make v_{out1} a square wave
v_{in2}: Pulse-width modulation source is 500mV pk-pk at 1kHz
v_{in3}: Pulse-amplitude modulation source 2V pk-pk at 2kHz superposed on a d.c. bias of +5V



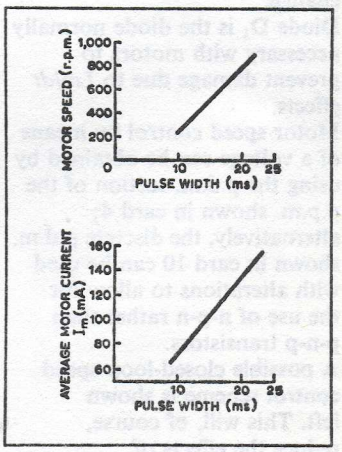
Circuit description
In the circuit shown a c.m.o.s. Schmitt-trigger circuit is formed by using A_1 and A_2 as a cascaded pair of inverters with positive feedback. In the absence of modulation, (V_{in2}= 0) the Schmitt switching action is determined by the ratio R_3/R_1 and V_{in1}. Provided R_3/R_1 is less than the forward gain in the linear region of the inverters, the switching action of the Schmitt follows the threshold crossings of the triangular wave input, V_{in1}. With a 10-V supply the Schmitt switches to $+V_{DD}$ when V_{in1} exceeds about +2.4V and switches back to V_{SS} (0V) when V_{in1} falls below about +1.85V.
For the purposes of pulse-width modulation it may be required to produce an modulated square-wave output (V_{out1}) and this may be obtained by superposing V_{in1} on a suitable d.c. bias (+2.1V) to produce unity mark-to-space ratio. This ratio may then be varied by causing the switching times of the Schmitt to be controlled by the p.d.m. signal (V_{in2}) which is conveniently fed to the A_1 input through R_2.

DC motor control using p.d.m.



Performance data
Supply: +40V
D_1: 1N4004
Tr_1: BFR41
Tr_2: TIP3055
R: 1kΩ
V_p: 6V
Pulse frequency: 40 per sec
Motor: 240V, 0.1-h.p.
6500 rev/min universal motor

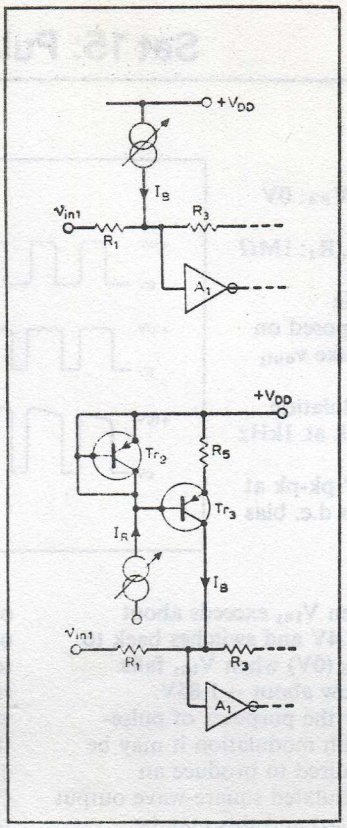
Circuit description
Circuit shows a pulse driven high-current switch Tr_1 and Tr_2 controlling the voltage applied to a motor. Basic principle involved is identical to that for thyristor driven motors viz that the average applied voltage controls the motor speed. During the pulse mark time Tr_2 conducts and the supply is able to supply current to the motor and during the pulse space time Tr_2 does not conduct and the supply is unable to deliver current. Clearly the greater the mark to space ratio of the pulse train the greater is the average applied voltage and with it the average motor current, I_m. Graphs show the results obtained. The linearity of these results, despite the fact that the motor was being used well outside its specifications, indicates the potential usefulness of the scheme.
Values of V_p and R are not critical so long as they provide sufficient base drive to Tr_1 to effect satisfactory switching and at the same time do not destroy Tr_1. In this case since we are switching currents less than 200mA and the current gain of Tr_1 and Tr_2 is greater than 1000 then the base drive to Tr_1 should be of the order of 0.2mA. Considerably less may suffice. The pulse frequency is not critical either. Maintaining a constant mark-space ratio, i.e. maintaining a constant average voltage, the motor ran at the same speed when the frequency was varied from 40Hz up to at least 4kHz. At higher frequencies lack of switching speed in the transistor



The p.d.m. signal is fed to Tr_1 which provides a similar output waveform but with its positive peak amplitude determined by the voltage to which R_4 is returned. Hence by returning R_4 to a second source of modulation (V_{in_2}) a waveform (V_{out_2}) results which is simultaneously modulated in both amplitude and duration.

Component changes
Useful range of V_{DD} +3 to +15V
Maximum useful v_{in_1} frequency 150kHz
Maximum pulse width modulation is achieved with $v_{in_2} \approx$ 900mV pk-pk
Maximum pulse amplitude modulation is obtained with $V_{in_2} \approx$ 12V pk-pk superposed on a d.c. bias of +9V

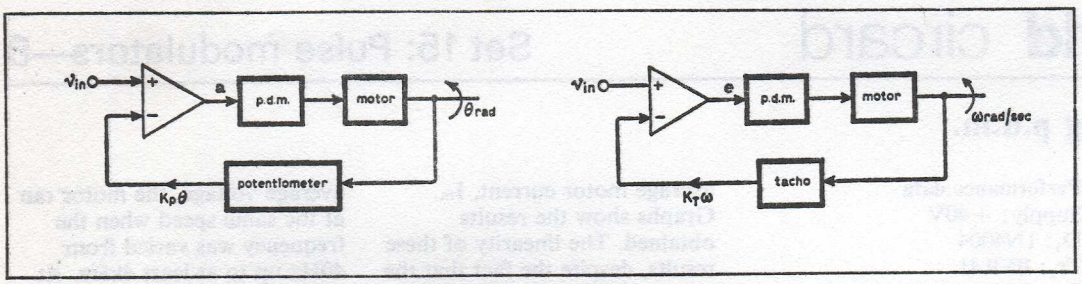
Circuit modifications
The d.c. bias on which V_{in_1} is superposed to provide a square-wave output may be dispensed with if a unity mark-to-space ratio is not required. If a low-duty-cycle pulse train output is required, the d.c. bias may be removed and the amplitude of the triangular wave (V_{in_1}) reduced so that it is only slightly in excess of the upper threshold level of the Schmitt but sufficient to allow modulation.
An approximately square-wave output can be obtained without a d.c. bias if the input triangular wave has a much larger amplitude.
When a d.c. bias is used to control the unmodulated mark-to-space ratio of V_{out}, a constant-current source may be used for this purpose as shown above. One method is to use an integrated circuit current mirror to provide the constant-current bias to set the unmodulated duty cycle as shown left. Negative feedback obtained by the inclusion of the emitter resistor R_5 raises the output impedance of the current mirror above that of a common-emitter stage.



Pulse duration modulation may be obtained by controlling I_R with the modulation signal.

Further reading
Schmidt, B. Schmitt trigger design uses CMOS logic, *Electronic Design*, vol. 20, April 1972, p.72.
Hart, B. L. Current generators, *Wireless World*, vol. 76, 1970, pp.511-4.

Cross references
Series 15, cards 1 to 6, 8 & 10.
Series 2, card 3.
Series 6, card 4.

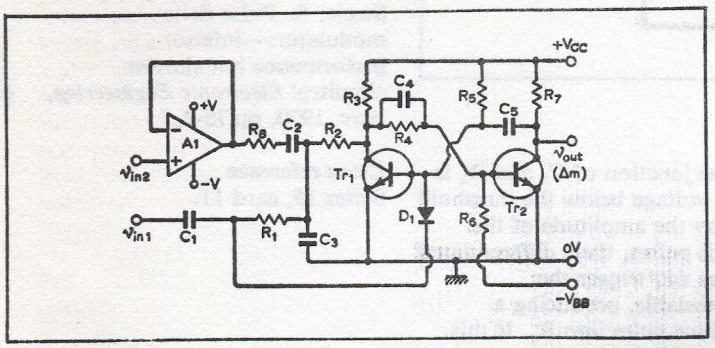


Further reading
Ghonaimy, M. A. R. and Aly, G. M. Phase-plane method for analysis of pulse-width modulated control systems. *International Journal of Control*, vol. 16, no. 4, 1972, pp.737-50.
Pulse-width modulation for d.c. motor speed control, *Semiconductors* (Motorola) vol. 2, no. 2, 1971, pp.36-8.

Cross references
Series 15, cards 2, 4, 6, 7 & 10.

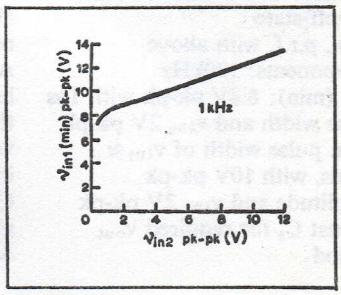
caused the motor speed to change.
Diode D_1 is the diode normally necessary with motors to prevent damage due to *Ldi/dt* effects.
Motor speed control by means of a voltage can be obtained by using the p.d.m. section of the p.p.m. shown in card 4; alternatively, the discrete p.d.m. shown in card 10 can be used with alterations to allow for the use of n-p-n rather than p-n-p transistors.
A possible closed-loop speed control scheme is shown left. This will, of course, reduce the effects of nonlinearities, disturbances, etc. If the motor and p.d.m. are known in advance the maximum value of e is fixed and this effectively dictates v_{in}, k and the differencing amplifier.
Diagram right shows a position control system; the output transducer need not, of course, be a potentiometer. This scheme has a considerable advantage in performance terms over conventional continuous control systems, because the steady state error in response to a step input in the presence of coulomb friction is eliminated. This is important in small motors in which brush friction is maximum torque developed by the motor. In the actuating signal 'a' and when this torque is less than the coulomb friction torque the motor shaft stops. Hence, 'a' can be non zero. However, if 'a' is feeding a p.d.m. as shown right, the motor develops maximum torque so long as 'a' is non zero, albeit for shorter and shorter intervals as 'a' reduces. Since the maximum torque is greater than the coulomb friction torque the motor can only come to rest when 'a' is zero.

Delta modulators

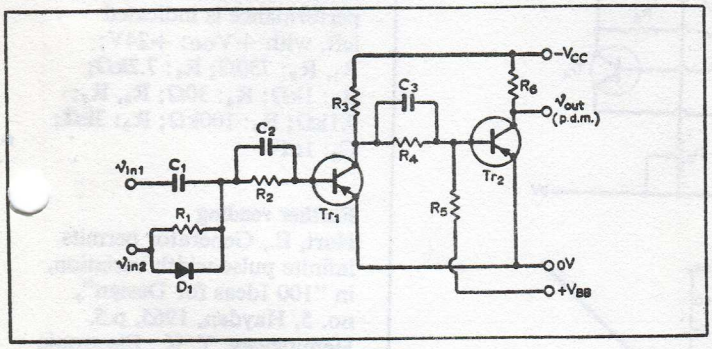


Typical performance
Supply (±V): ±12V, +22mA, −2.2mA; +Vcc: +12V
$-V_{BB}$: −5V at 200nA
A_1: 741; Tr_1, Tr_2: BC125
D_1: PS101
R_1: 10kΩ; R_2, R_3: 1kΩ
R_4: 4.7kΩ
R_5: 10kΩ; R_6: 22kΩ; R_7: 330Ω
R_8: 100Ω
C_1: 50pF; C_2: 1μF; C_3: 47nF
C_4: 220pF; C_5: 1nF
V_{in1}: 10V pk-pk pulses, p.r.f. 50kHz, duty cycle 10%
V_{in2}: 2V pk-pk sinewave at 1kHz
V_{out} (unmodulated) 0 to +12V pulses, p.r.f. 50kHz, m-s ratio 1:3
See overload characteristic opposite

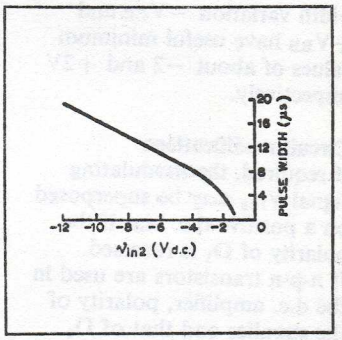
Circuit description
A delta modulator encodes an analogue signal into a train of binary pulses that represent the difference between the le[illegible] of the input signal at successive sampling times. The encoded pulse train has a repetition rate governed by the rate of change of the analogue signal; the greater this gradient the higher the density of the output pulses produced.
The delta modulator shown above employs a monostable multivibrator with C_5 controlling the monostable period and C_4 acting as a "speed-up" capacitor. The voltage follower A_1 is used as a low-output-impedance buffer between the modulation source and the junction of C_2 and R_2, R_8 being included to reduce ringing on the pulses at this junction.
In the stable state Tr_1 is on and Tr_2 is off so that a complementary V_{out} waveform is fed to C_2 via R_2. This signal is added to the modulating signal at the junction of R_2 and C_2. This composite voltage is



DC amplifier/pulse duration modulator



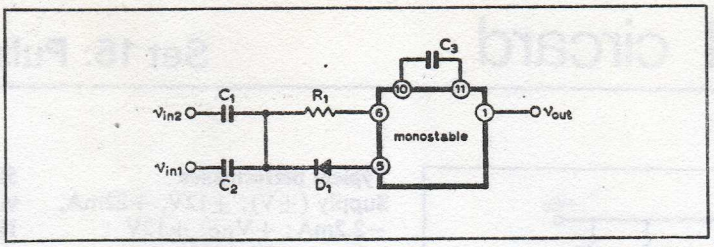
Typical performance
Supplies: $-V_{CC}$: −12V 9.7mA
$+V_{BB}$: +12V 1.8mA
Tr_1, Tr_2: BC126
D_1: PS101; R_1: 100kΩ
R_2: 22kΩ; R_3: 2.7kΩ
R_4: 470Ω; R_5: 6.8kΩ; R_6: 1kΩ
C_1: 100nF; C_2: 100pF
C_3: 470pF
V_{in1}: 3V pk-pk sawtooth at 50kHz



Circuit description
In the above circuit C_1, R_1 and D_1 act as a d.c. restorer where the peaks of the sawtooth wave (V_{in1}) are clamped to a level determined by V_{in2}. In the usual application of such a circuit, V_{in2} is a fixed d.c. level and provided that the time constant C_1R_1 is very much greater than the periodic time of V_{in1} the latter will be clamped to the desired level.
If a modulating signal, which varies much more slowly than V_{in1}, is used in place of a fixed value of V_{in2} the level to which the peaks of the sawtooth wave is clamped will be controlled by the variations in V_{in2}. Thus, the voltage appearing at the junction of C_1 and R_1 is effectively due to the addition of V_{in1} and V_{in2}.
This combined signal is applied to the input of a two-stage, high-gain, d.c. amplifier containing Tr_1 and Tr_2 which has the same form as a Schmitt trigger but with the hysteresis removed. When the input to this amplifier is large enough to change the state of Tr_1 an output pulse is obtained at Tr_2 collector having an amplitude almost equal to that of the $-V_{CC}$ supply. As the switching threshold is controlled by the level of the modulating signal the duration of the V_{out} pulses is linearly related to V_{in2} over a wide range of the latter—superposed on a suitable negative d.c. bias.

compared with a threshold voltage to determine whether the monostable will be triggered to its quasi-stable state. If the composite voltage across C_3 is less than the threshold, the differential clock pulses successfully trigger the monostable via D_1 until the voltage across C_3 is raised sufficiently to exceed the threshold. When this occurs the clock pulses fail to trigger the monostable circuit and C_3 discharges until the modulating signal input exceeds the voltage on C_3.

Component changes
$+V_{CC}$ (min): +7.4V
$-V_{BB}$ is non-critical: ensures Tr_2 off-state
Max. p.r.f. with above components: 130kHz
v_{in1} (min): 8.8V pk-pk with 1μs pulse width and v_{in2} 2V pk-pk
Min. pulse width of $v_{in1} \approx$ 900ns, with 10V pk-pk amplitude and v_{in2} 2V pk-pk
Adjust C_5 for required v_{out} period



Circuit modification
Another monostable form of delta modulator using an integrated circuit is shown above where the width of the output binary pulses is controlled by C_3. The analogue signal to be encoded (V_{in2}) and the clock pulses (V_{in1}) are fed to the junction of R_1 and D_1 via capacitors C_1 and C_2 respectively.
As V_{in2} would normally be a low-output-impedance source the complementary output voltage waveform (V_{out}) is integrated by R_1 and C_1.
Clock pulses are fed to the monostable via D_1 after being differentiated by C_2 and R_1.

If the junction of C_1 and R_1 is at a voltage below the threshold set by the amplitude of the clock pulses, their differentiated edges will trigger the monostable, producing a positive pulse into R_1. If this junction voltage is above the threshold the clock pulses are prevented from triggering the monostable. Junction threshold voltage is correctly adjusted by varying the amplitude of the clock pulses to cause the output pulse rate to be half the clock pulse rate.
Typical components are: monostable—DTμL9951; R_1 10kΩ; C_1 50nF; C_2 50pF.

Further reading

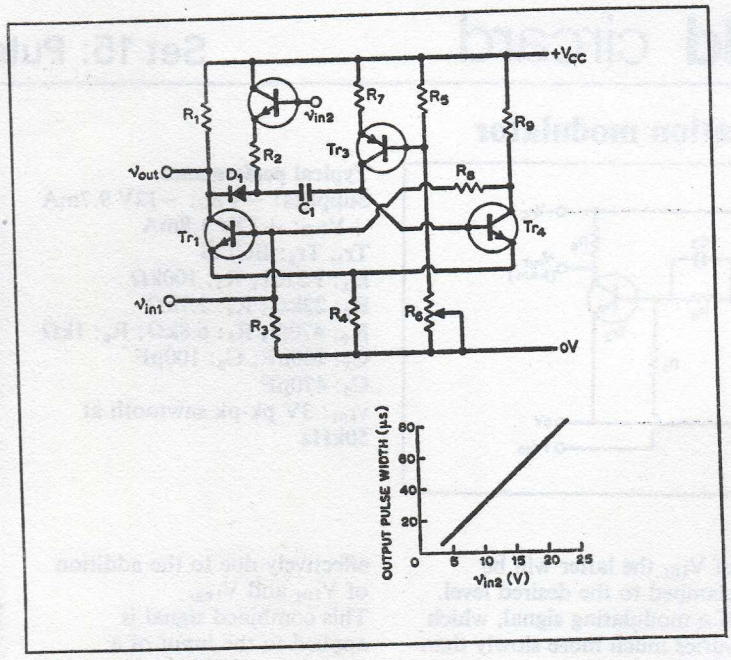
Steele, R. and Thomas, M. W. S. Two-transistor delta modulator, *Electronic Engineering*, Sept. 1968, pp.513-6.
Steele, R. Pulse delta modulators—inferior performance but simpler circuitry. *Electronic Engineering*, Nov. 1970, pp.75-9.

Cross reference
Series 15, card 11.

Hence, V_{out} is a pulse duration modulated pulse train.

Component changes
With a restricted range of pulse width variation $-V_{CC}$ and $+V_{BB}$ have useful minimum values of about -2 and $+2$V respectively.

Circuit modifications
If required, the modulating signal V_{in2} may be superposed on a positive d.c. bias if the polarity of D_1 is reversed.
If n-p-n transistors are used in the d.c. amplifier, polarity of the supplies and that of D_1 should be reversed.
A different approach to linear pulse-duration modulation is shown here. This circuit uses a monostable multivibrator to set the width of the unmodulated output pulses which have a repetition rate determined by that of the input positive pulse train, V_{in1}.
Output pulse width is a linear function of the modulating signal (V_{in2}) applied to the base of Tr_2 which serves as a constant-current generator.
With Tr_1 off and Tr_4 on and saturated D_1 is reverse-biased, if $V_{in2} < V_{CC}$, and C_1 charges.



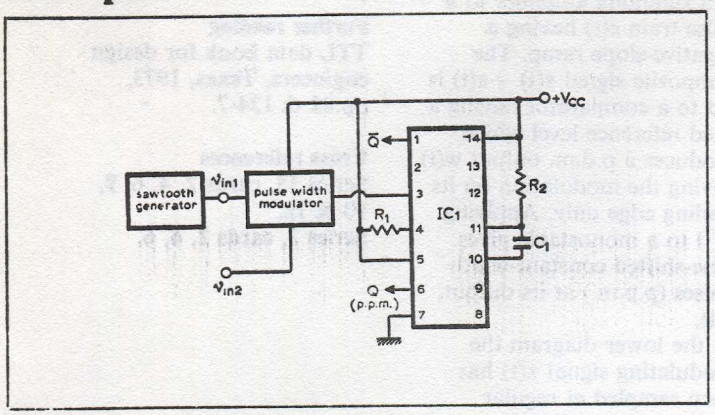
When Tr_1 is switched on by a V_{in1} pulse the charge on C_1 changes at a rate determined by the constant-current transistor Tr_2 until the base-emitter voltage of Tr_4 rises sufficiently to switch Tr_4 on and hence Tr_1 off. Capacitor C_1 is now isolated from Tr_1 collector which therefore switches off rapidly. Typical performance is indicated left, with $+V_{CC}$: +24V; R_1, R_9: 750Ω; R_2: 7.2kΩ; R_3: 1kΩ; R_4: 30Ω; R_5, R_7: 9.1kΩ; R_6: 100kΩ; R_8: 3kΩ; C_1: 1nF.

Further reading

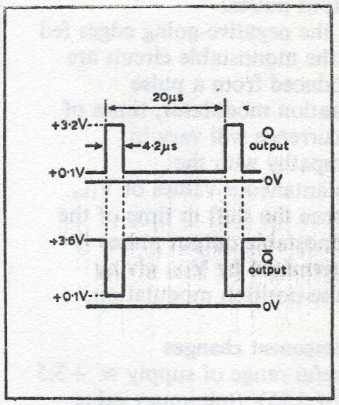
Hart, E., Generator permits infinite pulse-width variation, in "100 Ideas for Design", no. 5, Hayden, 1965, p.5.
Hemingway, T. K., Electronic Designer's Handbook, Business Publications, 1967, pp.17/9.
Hughes, R. S. Pulse width vs. control voltage made linear by generator in "100 Ideas for Design", no. 5, Hayden, 1965, p.76.

Cross references
Series 15, cards 2, 4, 6, 7, 8 & 11.

Pulse position modulator



Typical performance
Supply: +5V, +23.5mA
IC_1: SN74121N
R_1, R_2: 1kΩ; C_1: 6.8nF
Pulse duration modulator: see card 10 with Tr_1, Tr_2 BC125 (n-p-n) transistors, $+V_{CC}$: +5V; $-V_{BB}$: −5V and D_1 polarity reversed.
V_{in1}: 3V pk-pk sawtooth at 50kHz
V_{in2}: Sinewave modulation superposed on a direct bias of +3.75V to give square wave output from modulator



Circuit description
The pulse-position modulator employs a pulse-duration modulator feeding a t.t.l. integrated-circuit monostable package. Many different pulse-duration modulators could be used to drive the monostable provided that the output pulses are t.t.l.-compatible. The one used was the d.c. amplifier type described in card 10. To provide the required t.t.l. compatibility, the circuit shown in card 10 was modified to use BC125 (n-p-n) transistors with supplies of $+V_{CC}$ +5V and $-V_{BB}$ −5V the polarity of D_1 also being reversed. See card 10 for circuit description.
The t.t.l. monostable package provides complementary output pulses which can be initiated in several ways. With the connections shown, input B (pin 5) is held high and input A_2 (pin 4) which is unused is taken to $+V_{CC}$ through a 1-kΩ resistor. In this form the package acts as a monostable circuit providing an output pulse of defined width whenever input A_1 (pin 3) receives a logic-level negative-going trigger pulse. Width of the

Pulse code modulator

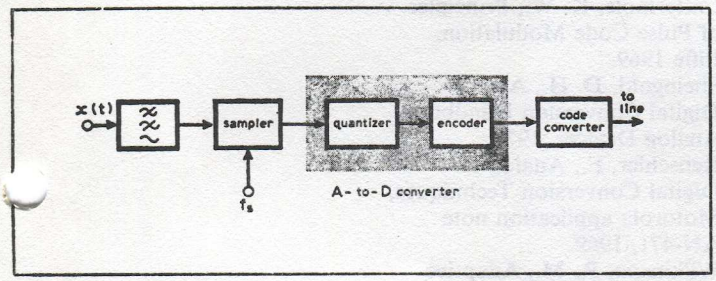
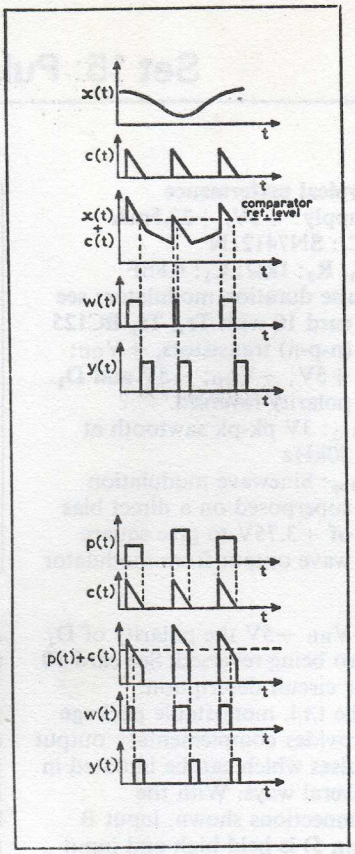


Diagram shows in block form the basic processes used in a single-channel pulse-code modulator. The analogue signal to be encoded, x(t), is passed to a sampling gate via a low-pass filter which defines the bandwidth of the modulation. The sample pulses are of low duty cycle and have a constant p.r.f. (f_s) that is at least twice that of the highest modulating signal component (f_m). In practice $f_s > 2f_m$, e.g. for speech that has been bandlimited to 0.3 to 3.4kHz, f_s= 8kHz. The output of the sampler is a p.a.m. signal which has an infinite possible number of amplitudes that are quantized, uniformly or non-uniformly, into a finite number of allowed levels. Although each sample is converted to the nearest allowed level, quantization inherently introduces errors or quantization noise. Non-uniform quantization of speech produces an improvement in the signal-to-quantization noise ratio.
Each quantized sample of the p.a.m. wave is then encoded into a group of pulses according to a binary code, the number of pulses in each code group being determined by the number of allowed levels in the quantization scheme. For speech transmission 128 levels are normally used, hence a 7-bit code is used (2^7= 128). For transmission, the coded signal is normally converted to a bipolar form to avoid wasting transmitter power by sending a d.c. component containing no information. One such code is alternate-mark-inversion (a.m.i.) which is a pseudo-ternary code with binary significance.
See the works, and their bibliographies, listed under in further reading for detailed system and circuitry techniques.
Diagram over shows an adaptive pulse code modulator for encoding speech. In this technique the coding signals change to track the changes in the "envelope" of the speech input x(t) after it has been bandlimited by the filter to 0.25 to 2.4kHz. The output is fed simultaneously to the voltage comparators A_1, A_2 and A_3; A_1 and A_3 together provide updated amplitude information by comparing x(t) with a feedback voltage $V_f(t)$ and its inverse respectively. Comparator A_1 produces an output logic 1 when $x(t) > +V_f(t)$ and A_3 produces a logic 1 output when x(t) is more negative than $-V_f(t)$. The A_1 and A_3 outputs are fed to bistable circuit FF2 via an

output pulses is determined by the value of C_1 with R_2 ensuring that this width is obtained accurately and repeatedly. Larger R_2 values for a given C_1 will widen the output pulses.
As the negative-going edges fed to the monostable circuit are produced from a pulse duration modulator, times of occurrence will vary in sympathy with the instantaneous values of V_{in_2}. Hence the shift in time of the monostable output pulses is determined by V_{in_2} giving pulse-position modulation.

Component changes
Useful range of supply ≈ +3.5 to +5.25V (minimum value not guaranteed)
Max. range of V_{in_2} ≈ 7V pk-pk superposed on a bias of +3.75V gives pulse shift of ≈ 14μs at p.p.m. output
Change R_2 and C_1 for different output pulse widths

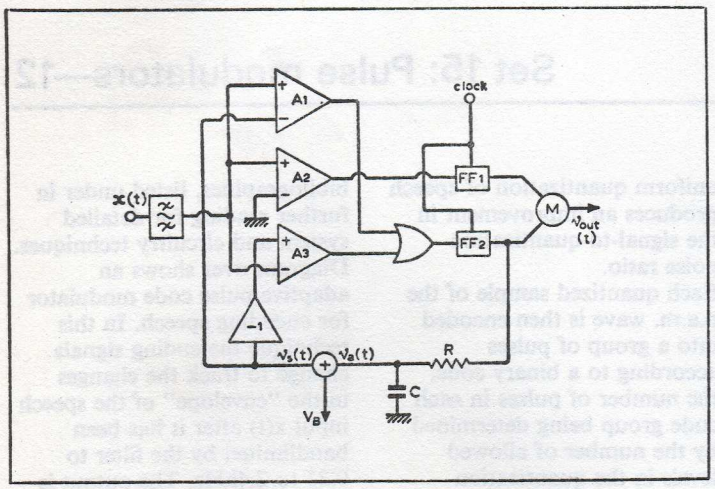
Circuit modifications
Pulse-position modulated



signals may be produced by a variety of electronic circuits which normally perform the signal processing indicated left. In the upper diagram the modulating signal x(t) is added in a summing amplifier to a pulse train c(t) having a negative-slope ramp. The composite signal x(t) +c(t) is fed to a comparator having a fixed reference level which produces a p.d.m. output w(t) having the modulation on its trailing edge only. Applying w(t) to a monostable gives time-shifted constant-width pulses (p.p.m.) at its output, y(t).
In the lower diagram the modulating signal x(t) has been sampled at regular intervals to produce the flat-topped p.a.m. wave p(t). The same sampling pulses are used to trigger a generator producing a synchronous train of pulses c(t) having a negative-slope ramp. The c(t) and p(t) signals are added as before and fed to a comparator producing a p.d.m. output w(t) which in turn feeds a monostable to produce the p.p.m. output y(t). Reversing the slope of the ramp in c(t) produces leading-edge p.d.m. to feed to the monostable.

Further reading
TTL data book for design engineers, Texas, 1973, pp.82 & 134-7.

Cross references
Series 15, cards 2, 4, 6, 9, 10 & 12.
Series 3, cards 2, 4, 6.



OR gate, the output of which is sampled at 4.8kHz. Thus, each amplitude information bit at the FF2 output is a logic 0 when the x(t) sample is in the range $-V_f(t) < x(t) < +V_f(t)$ and is a logic 1 when x(t) is outside this range.
The A_2 comparator provides x(t)-polarity information, producing a logic 1 at its output when x(t) is positive and a logic 0 when x(t) is negative. The A_2 output feeds bistable circuit FF1 which is sampled at 4.8kHz to produce polarity bits that are combined with the amplitude information bits in the multiplexer (M), which simply transmits its 2-channel inputs alternately at 9.6kbit/s. $V_f(t)$ is obtained by feeding the FF2 output to a 10ms RC integrator giving a positive output $V_a(t)$ to which is added a small d.c. bias (V_B) to ensure that $V_f(t)$ never falls to zero.

Further reading
Cattermole, K. W., Principles of Pulse Code Modulation, Iliffe 1969.
Sheingold, D. H., Analog-Digital Conversion Handbook, Analog Devices, 1972.
Renschler, E., Analog-to-Digital Conversion Techniques, Motorola application note AN-471, 1969.
Wilkinson, R. M., Adaptive Pulse Code Modulator for Speech Signals, SRDE report no. 72001, January 1972.

Cross reference
Series 15, card 11.