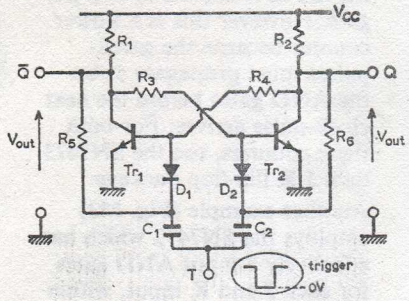
wireless world circard

Set 14: Digital counters—1

Basic binary counters



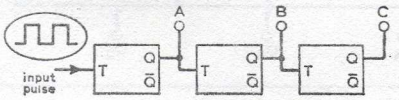
Typical data
Single bistable
Vcc: +12V
Tr_1, Tr_2: BC108
R_1, R_2: 3.3kΩ ±10%
R_3, R_4: 8.2kΩ ±10%
R_5, R_6: 6.8kΩ ±10%
C_1, C_2: 800pF
D_1, D_2: PS101
Frequency 100kHz typically
Trigger input ≈ 4V
Trigger input width < 1μs

Circuit operation

The bistable circuit is a T-type "flip-flop" in which the output changes state for a negative-going transition at the trigger-input. If the base-drive current is arranged so that Tr_2 is in saturation, its collector voltage will be about 0.2V. This is too low to forward-bias the base-emitter junction of Tr_1, about 0.7V, and hence Tr_1 will be off. This means its collector-emitter voltage is high, depending on R_1 and R_3, and the base-drive current for Tr_2 flows through R_1 and R_3. Hence the terminals identified (arbitrarily) as Q and $\bar{Q}$ are low and high respectively (0 and 1 for binary coding).

When the trigger input is high, the circuit is in a stable state. When the trigger input is driven near ground the negative-going pulse-edge is steered to Tr_2 base as D_2 is forward-biased. The anode of D_1 is approximately at $V_{CE(sat)}$ and because its cathode is connected to a high potential via R_5 it is reverse-biased. Therefore Tr_2 collector current is reduced, causing a rise in its collector voltage, increasing base-drive current to Tr_1. This causes Tr_1 collector voltage to drop and Tr_2 base current decreases causing a further increase in Tr_2 collector voltage. The process continues until the other stable state, Tr_1 conducting and Tr_2 off, is sustained. The next negative-going trigger pulse resets the circuit to its previous state. It produces one output pulse for every two trigger pulses.

The interconnection of these bistable circuits to give a binary ripple counter demands that the Q output of a previous flip-flop is connected to the trigger (or T−) input of the next flip-flop. This gives a natural count of 2^n where n is the number of stages, and 2^n is the number of states through which the counter progresses.



Circuit modification

Range of R_5, R_6: 4.7k to 47kΩ
Frequency variation: 150 to 30kHz
Range of C_1, C_2: 330 to 3300pF
Frequency variation: 140 to 90kHz
Increase turn-on speed with capacitors across resistors R_3 and R_4 typically 5 to 20% of C_1, C_2.
Increased frequency of operation possible with additional diodes connected

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Set 14: Digital counters—2

One out of n ring counter

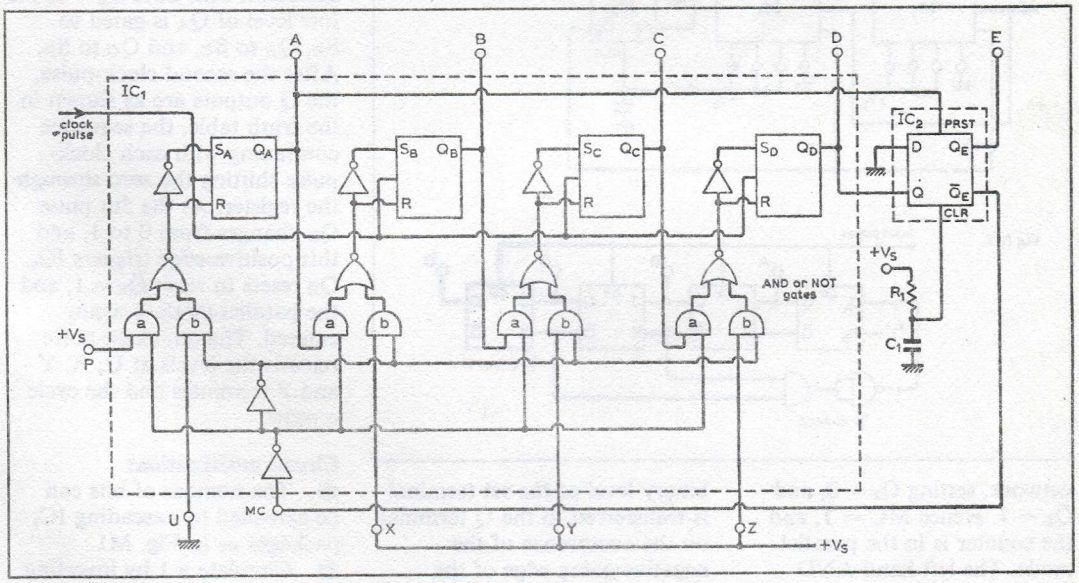
Typical data
IC_1: SN7495
IC_2: ½SN7474
V_s: +5V
P: 1kΩ
47pF

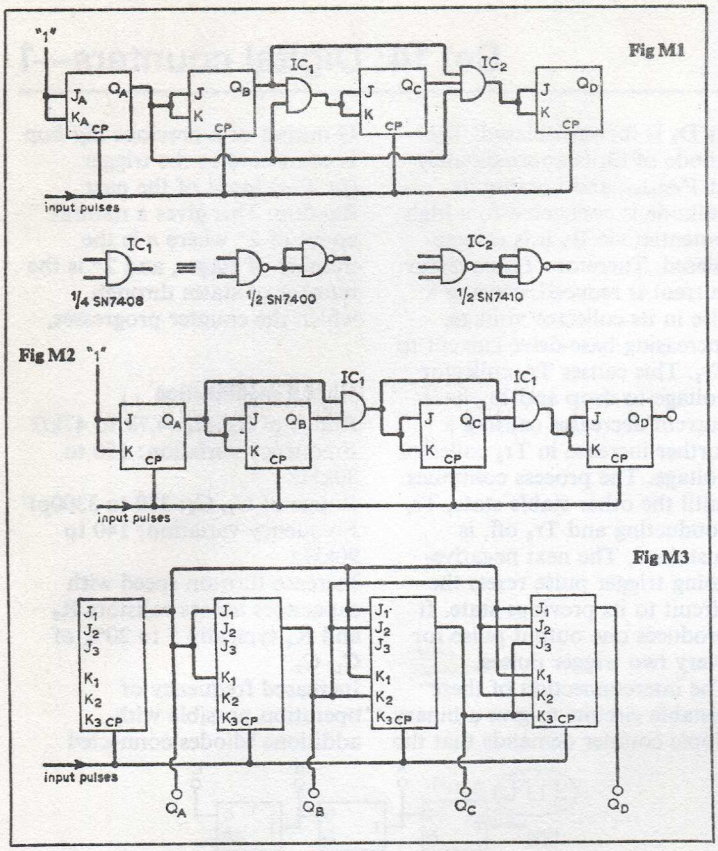
Circuit description

Component IC_1 is a 4-bit shift left or right register, comprising master-slave R-S flip-flops, with a parallel-loading capability via the AND-OR-NOT gates at terminals U, X, Y and Z. This is conditioned by mode-centre terminal MC equal to binary one. When MC=0, information transfers serially through the register, the clock-pulses being applied to the commoned right-shift and left-shift inputs (not shown). When used in conjunction with a positive-edge triggered flip-flop, IC_2, this arrangement provides a self-starting, self-priming ring-counter for circulating a zero.

When the supply V_s is switched on, the clear-input of IC_1 is pulled down to ground by CR

Clock pulse No.	Q_A	Q_B	Q_C	Q_D	Q_E
1	0	1	1	1	1
2	1	0	1	1	1
3	1	1	0	1	1
4	1	1	1	0	1
5	1	1	1	1	0
6	0	1	1	1	1





across R_5, R_6 (anode to collector).
High-speed transistors BSX19, BSX20 permit counting speeds up to 10MHz.

IC binary counter

The ripple binary counter is commonly implemented with integrated circuits using J-K flip-flops e.g. the SN7493 is a 4-bit binary counter within one package allowing a typical count rate up to 18MHz for d.c. supply +5V, and a typical load of 400Ω and 15pF. Synchronous binary counters using dual J-K master-slave flip-flops are shown above. In all cases decouple the power supply—typically 0.01μF per package.

In Fig M1, since $J_A=K_A=1$ (high), the first flip-flop acts as a toggle. The second flip-flop is triggered by alternate clock pulses the third—flop is gated by the Q_B and Q_C outputs and only changes when $Q_A=Q_B=1$. Similarly, the last flip-flop only changes state when $Q_A=Q_B=Q_C=1$. This counter has the disadvantage of long counter chains requiring AND gates with a large fan-in.

The situation is avoided with the counter of Fig. M2 where the fan-in is limited to two per gate. However this is a slower counter because the gated-pulses must propagate down the AND gates before the next clock-pulse arrives. For both these counters, use the SN7473 dual J-K flip-flop package.

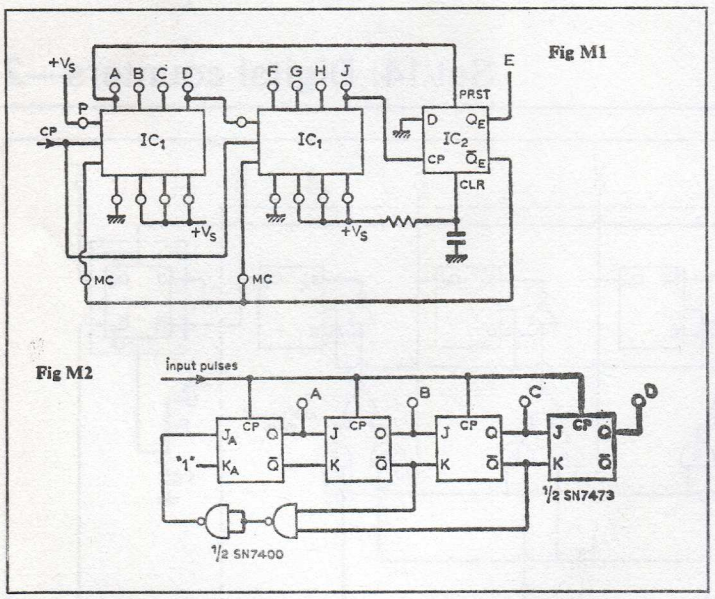
Another example (Fig. M3) employs the SN7472 which has effectively 3-input AND gates for each J and K input, within the package, which eliminate the need for external gates.

Further reading

Electronic Counting, Mullard, 1967.
Designing with TTL Integrated Circuits (Texas), McGraw-Hill 1971.
Counter delay slashed in half with interconnection scheme, *Electronic Design* 13, 1972.

Cross references

Series 14, cards 4, 6 & 12.



network, setting $Q_E=0$, and $\bar{Q}_E=1$. Hence MC = 1, and the counter is in the parallel mode. The left-hand AND gates are inhibited, and the voltage levels at inputs U, X, Y and Z are transferred to the set inputs, S_A to S_D, of IC_1.
In master-slave flip-flops, the binary level at the set terminal is transferred to the Q terminal on the occurrence of the negative-going edge of the clock-pulse.
After the first clock-pulse, $Q_A=0$, Q_B to $Q_D=1$. Also, Q_A is connected to the preset input of IC_1, and hence Q_E is set to binary one. Hence $\bar{Q}_E=0$, and the counter is switched to a serial-mode. The right-hand AND gates are now inhibited. Therefore $S_A=1$, the low level of Q_A is gated to S_B, Q_B to S_C, and Q_C to S_D. After the second clock-pulse, the Q outputs are as shown in the truth table, the sequence continuing with each clock-pulse shifting the zero through the register. At the 5th pulse, Q_D changes from 0 to 1, and this positive-edge triggers IC_2. Q_E resets to zero, $\bar{Q}_E=1$, and the parallel-mode is again entered. The 6th clock-pulse reloads the levels at U, X, Y and Z terminals and the cycle repeats.

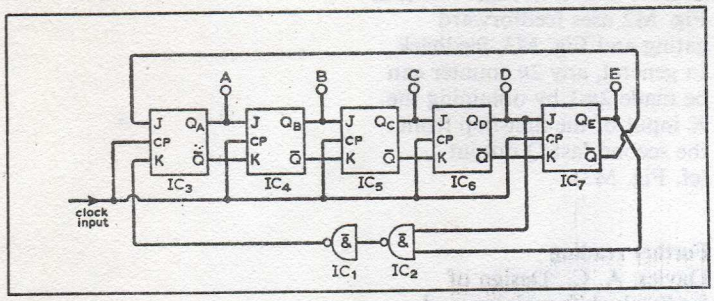
Circuit modifications

- The number of bits can be extended by cascading IC_1 packages as in Fig. M1.
- Circulate a 1 by inverting the counter outputs with t.t.l. NAND gates (SN7400) or c.m.o.s. hex buffers (CD4049).
- A 4-bit self-starting and correcting counter (Fig. M2) for circulating 1 uses J-K flip-flops and feedback via an AND gate. The flip-flops are connected as a shift register, where the state of Q_A is passed to Q_B, and Q_B to Q_C, etc. with each clock pulse. In general, for self-correcting, and when using J-K flip-flops, J_A should be the Boolean product of the complements of all but the first and last stages.

Further reading

Self-connecting ring counter requires no external gates, *Electronic Design* 9, 1973, p.138.
Malmstadt and Elke, Digital Electronics for Scientists, Benjamin, 1969.
Texas Instruments application report CA102,
Electronic Counting, Mullard, 1967.

Johnson counters



Circuit description

This counter, also called a switch-tail ring counter, allows $2n$ counts where n is the number of cascaded flip-flops. It is a synchronous counter in that changes at the Q outputs only take place on the occurrence of clock-pulse. If $J = \bar{K}$, the J input condition is transferred to the related Q output on the negative edge of the clock pulse, when the flip-flops are master-slave types. The above circuit has ten different states, the feedback via the AND gate causing self-correction after a few steps, should illegitimate states occur.

Consider all Q outputs to be in the 0 state. Hence $J_A = 1$ because $\bar{Q}_E = 1$. On the occurrence of the first clock pulse, the counter will load according to the truth-table. At each subsequent pulse, "1"s will be fed through the counter from the left until $Q_D = Q_E = 1$.

Typical data

Supply: 4.75 to 5.25V
IC_1, IC_2: $\frac{1}{2}$ SN7400
IC_3, IC_6: $\frac{1}{2}$ SN7473
Min. clock width: 20ns (between 50% levels)
Typical pulse height: 3.5 to 4.5V

It follows then that since $J_A = 0$, $K_A = 1$, that Q_A becomes 0 at the 6th clock-pulse. Zeros are subsequently transferred through the register according to the truth-table, until $Q_D = Q_E = 0$, then $J_A = 1$, $K_A = 0$, and the cycle repeats.

In general, when there are n stages in the counter, feedback via an AND gate from the last x stages, where x is the next larger integer to $n/3$ provides self-correction for n up to 25.

Decoding of each state is obtained using AND gates, as a unique pair exists for each state. These output pairs are indicated in the truth-table, and are applied to the gate inputs (these can be $\frac{1}{4} \times$ SN7400 in series).

Circuit modifications

The same output sequence is obtained from dual D-type flip-flops (SN7474) as Fig. M1. In general, assuming eight flip-flops are employed, A, B, C, D, E, F, G, H, then the

clock pulse	A	B	C	D	E	decoding outputs
	0	0	0	0	0	
1	1	0	0	0	0	$A\bar{B}$
2	1	1	0	0	0	$B\bar{C}$
3	1	1	1	0	0	$C\bar{D}$
4	1	1	1	1	0	$D\bar{E}$
5	1	1	1	1	1	$A\bar{E}$
6	0	1	1	1	1	$\bar{A}B$
7	0	0	1	1	1	$\bar{B}C$
8	0	0	0	1	1	$\bar{C}D$
9	0	0	0	0	1	$\bar{D}E$
10	0	0	0	0	0	$\bar{A}\bar{E}$

Reversible counters

Circuit description

Up-down or reversible counters alter their mode of counting under electrical control. The circuits shown are binary up-down counters in which the count direction is controlled by steering logic and either the flip-flop Q outputs are used for toggling subsequent flip-flops (UP) or the $\bar{Q}$ outputs are used when the Q outputs are inhibited. Fig. 1 is an asynchronous type and Fig. 2, a synchronous counter.

The equation for the output of the selector gate is, for example, $AX + \bar{A}\bar{X}$, the gating usually being implemented by the NAND gate interconnection of Fig. 3. When a logic 1 is applied to the up-down control line, the gates connected to $\bar{Q}$ are inhibited, and the flip-flops change state when their clock inputs undergo a 1 to 0

Fig 1

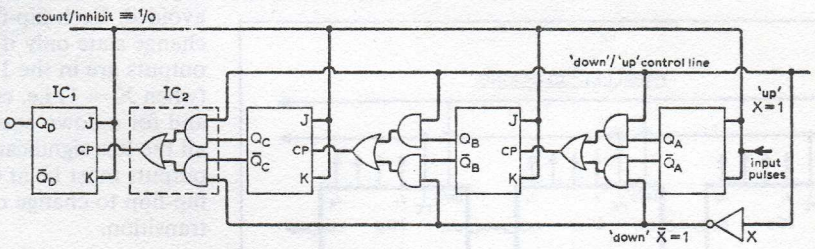


Fig 2

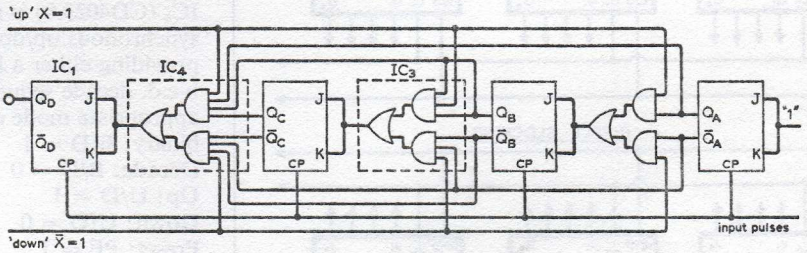
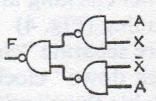


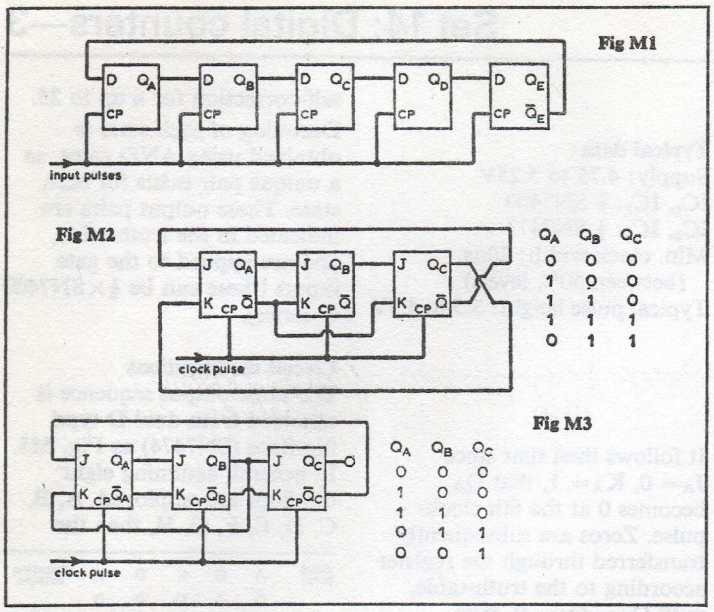
Fig 3



Integrated circuits

IC_1: SN7473
IC_2: $\frac{3}{4} \times$ SN7400
IC_3: SN7410
IC_4: SN7420 and $\frac{1}{4} \times$ SN7400
IC_5: CD4029A
Supply: 4.75 to 5.25V

Synchronous up-down b.c.d. and binary counters are available in packages SN74190 and SN74191 respectively.



Q_A	Q_B	Q_C
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1

Q_A	Q_B	Q_C
0	0	0
1	0	0
1	1	0
0	1	1
0	0	1

feedback functions for an even cyclic pattern are

$J = \bar{C}$, $K = B.C$	(6)
$J = \bar{D}$, $K = C.D$	(8)
$J = \bar{E}$, $K = D.E$	(10)
$J = \bar{F}$, $K = E.F$	(12)
$J = \bar{G}$, $K = E.F.G$	(14)
$J = \bar{H}$, $K = F.G.H$	(16)

An odd sequence ($2N$-1) counter can be implemented by bypassing the all "1"s state of the normal Johnson sequence i.e. the last two bits of the 111 . . . 10 state are detected, and the gating arranged to the first flip-flop so that the next state is 011 . . . 11. (Texas ref.).

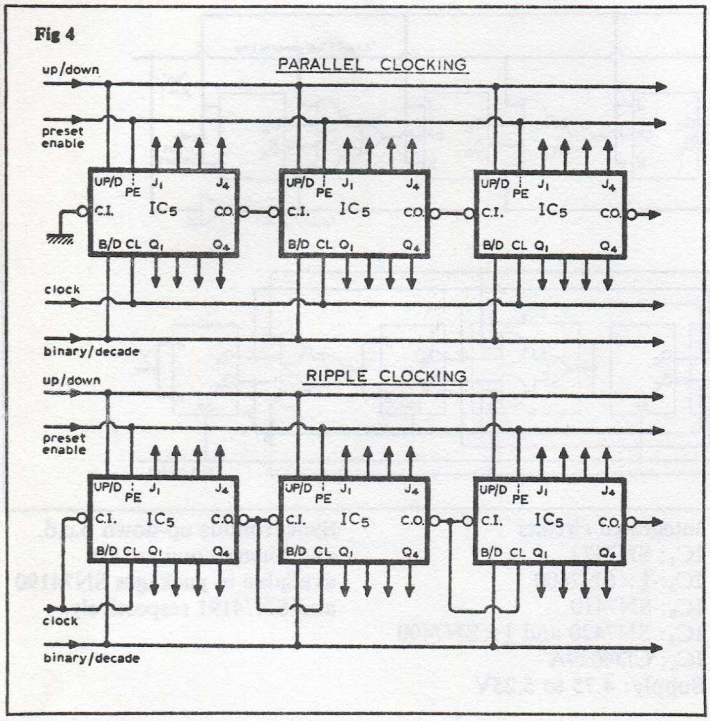
Other odd sequence counters can be implemented by J-K flip-flops without extra gating and are shown in Figs. M2 & 3. Fig. M2 uses feedforward gating and Fig. M3, feedback. In general, any $2n$ counter can be made $2n$-1 by obtaining the K input of the first-flop from the second last Q output (cf. Fig. M3).

Further reading

Davies, A. C., Design of feedback shift registers and other synchronous counters, *Radio and Electronic Engineer*, April 1969.
Texas Instruments application report CA102.
Kohonen, T. Digital circuits and devices, Prentice-Hall, 1972.
Malvino, A. P. & Leach, D. P., Digital principles and applications, McGraw-Hill, 1969.

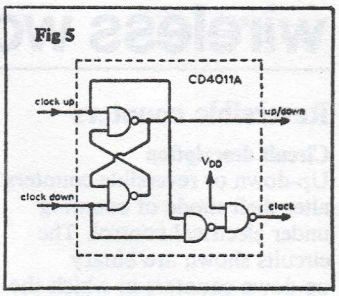
Cross references
Series 14, cards 9 & 12.

transition i.e. the Q outputs will change according to the normal binary sequence. If the control line becomes 0, the Q outputs will reverse sequence. To avoid a false triggering condition, the count/inhibit line must be 0 when the controlling function is altered from up to down or vice-versa.



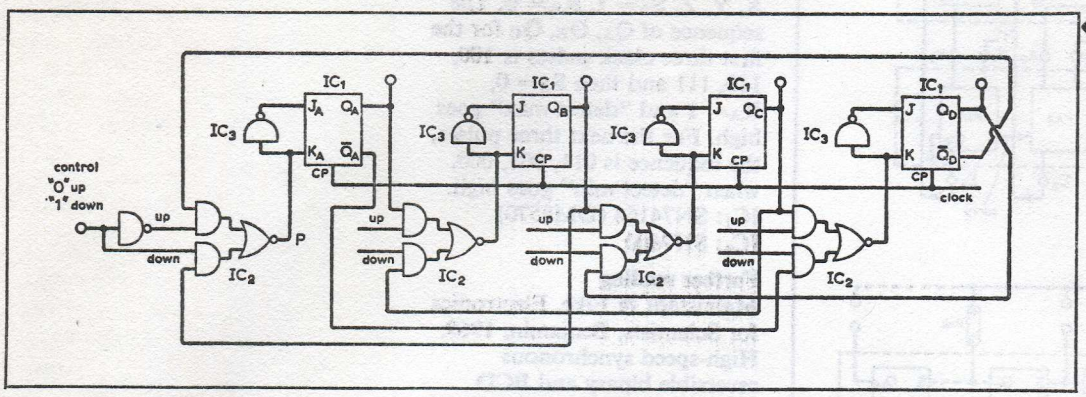
In the synchronous counter of Fig. 2 such a condition is avoided. Each flip-flop will change state only if previous Q outputs are in the 1 state (when X = 1) i.e. counting up, and for a down count ($\bar{X}$ = 1), all the less significant Q outputs must be at 0 for a flip-flop to change on a 1 to 0 transition.

IC_5 (CD4029A) is a presettable synchronous up/down counter providing either a binary or b-c.d. decade sequence with appropriate mode control, i.e.
binary: B/D = 1
Decade: B/D = 0
Up: U/D = 1
Down: U/D = 0
Preset: PE = 1
J1 to J4 = 1 or 0
Parallel clocking allows cascading (Fig. 4)
Where separate "clock up" and "clock down" clock pulses are available the circuit of Fig. 5 provides a simple interface to the up/down "clock" inputs.



Cross references
Series 14, cards 5 & 12.

Reversible counter with Johnson coding



Integrated circuits
IC_1: ½SN7473
IC_2: ½SN7451
IC_3: ¼SN7400

The AND-OR-NOT gates provide gating control for the up/down mode. The Boolean expression for the P output is $\overline{(\overline{Q_D} + (DWN)Q_B}$. If the control line = 0, then $P = Q_D = 0$. Hence $J_A = 1$, $K_A = 0$, and on the occurrence of the first clock pulse $Q_A = 1$. The counter would subsequently count up in Johnson code. However, if for example, the counter state is 1110 and control = 1, only the S output causes a change to make $Q_C = 0$ on the next pulse, and thus count down.

Circuit over (top), uses a 4-bit parallel adder and four D-type flip-flops. Consider the sum outputs $\Sigma_4 - \Sigma_1$ show 7_{10} i.e. 0111_2, where Σ_1 is the least significant bit, and that the next pulse should cause a decrement, hence control = 1. Each sum variable (Σ) is transferred to the Q output on the occurrence of the clock pulse via each D-type flip-flop. Inputs (B_1A_1), (B_2A_2) etc. are added and each produce 0 carry 1 except for (B_4A_4) which makes $\Sigma_4 = 1$. When the "carry's" ripple through, the result is 0110 with $C_{out} = 1$, which can be ignored. (This is 2's complement arithmetic, where negative-one, represented by 1111_2, is added to achieve subtraction).

IC_1: SN7483 (full adders)
IC_2: SN7495 (or 2×SN7474)
Typical operating frequency ≈ 10MHz

An eight-bit shift register is used to provide a variable modulus counter in which maximum and minimum counts may be detected is shown over (bottom). Shorting any one pair of

Divide by n counters

Counters with N states (modulus N) may comprise a sequence of counters with different moduli, integers n_1, n_2, n_3 etc. and $N = n_1 \times n_2 \times n_3 \ldots$ Even numbers are achieved by cascading as in Fig. 2 (modulus 2^m, where m is the number of flip-flops). Synchronous circuits for smaller odd numbers are shown below. Q_A is the least significant bit, the natural binary sequence is followed and positive logic assumed.

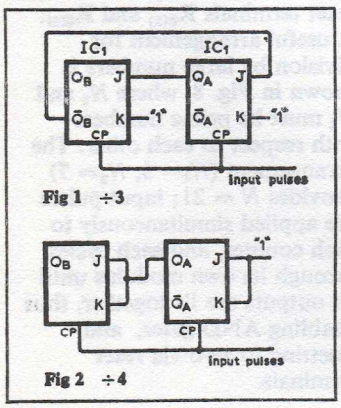


Fig 1 ÷3

Fig 2 ÷4

Components (typical)
IC_1: ½SN7473. IC_2: ⅓SN7410.
IC_3: ¼SN7400. IC_4: SN7472 (or ½SN7473 plus 3 input gates).
IC_5: SN7493. IC_6: ¼SN7408 (or ½SN7400). IC_7: ⅓SN7410.

Description

For the small prime numbers, it is sufficient to consider Fig. 3 as an example. Q_A flip-flop acts as a toggle and will change still on every input pulse while $\overline{Q}_C = 1$ ($Q_C = 0$). Q_B changes state whenever Q_A goes from 1 to 0. Q_C will only be set to 1 when both Q_A and Q_B are logic one i.e. on the 4th clock-pulse, because $J_1 = J_2 = J_3 = 1$ and the K inputs are 0. Hence on the 5th

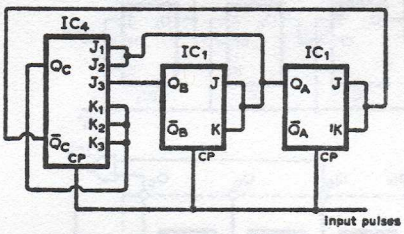


Fig 3 ÷5

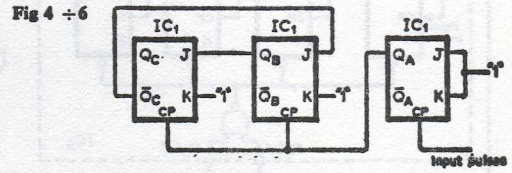


Fig 4 ÷6

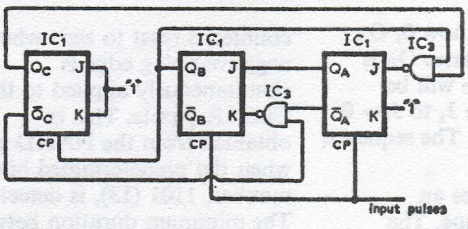
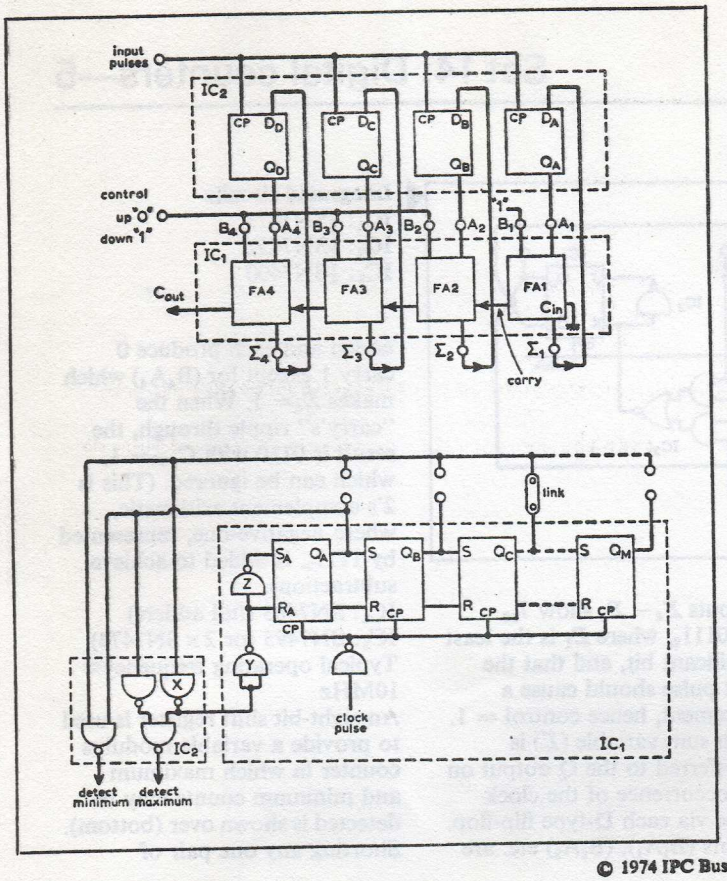


Fig 5 ÷7



external terminals decides the maximum counter loading at which the counter may then be considered to reverse.

Assume a counter cleared and a link at Q_C. Then, via gates X, Y, Z, $S_A = 1$, $R_A = 0$. The sequence of Q_A, Q_B, Q_C for the first three clock pulses is 100, 110, 111 and then $S_A = 0$, $R_A = 1$ and "detect max" goes high. For the next three pulses, the sequence is 011, 001, 000, when "detect min" goes high.

IC_1: SN74164 (DM8570)
IC_2: SN7400

Further reading

Malmstadt & Elke, Electronics for Scientists, Benjamin, 1969.

High-speed synchronous reversible binary and BCD counters. Texas Instruments application report B40.

Baccolini, G., Benetazzo, L., & Clements, G., Variable dead-zone counter as a maximum value follower, *IEEE Trans.* vol. ECI-20, Aug. 1973.

Cross references

Series 14, cards 4 & 12.

Fig 6

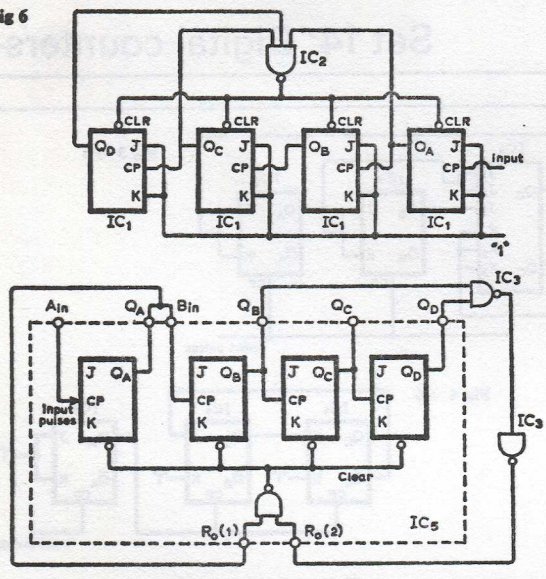


Fig 7

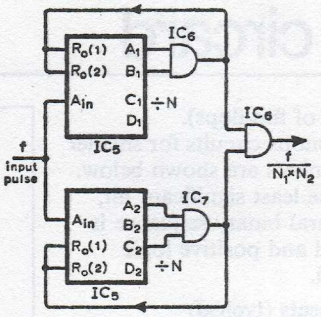


Fig 8

SN7493 connection

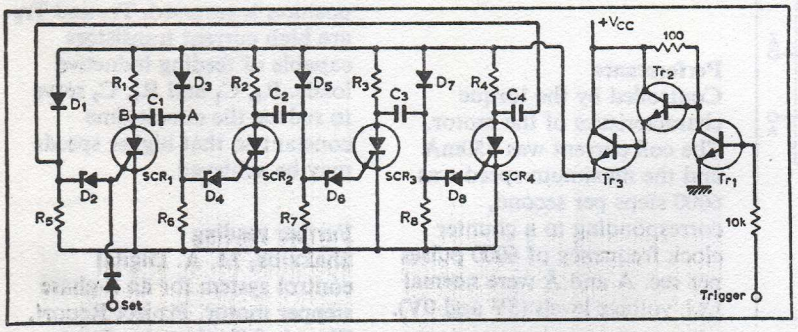
Divisor N	*Feedback*	*Extra gate*
9	A D	—
10	B D	—
11	A B D	2 I/P AND
12	C D	—
13	A C D	2 I/P AND
14	B C D	2 I/P AND
15	A B C D	3 I/P AND

pulse, since $\bar{Q}_C$ is now 0, Q_A will remain at 0 hence Q_B is logic zero, and Q_C will be reset to 0, because J_1 to $J_3 = 0$ and K_1 to $K_3 = 1$. The sequence then repeats.

Fig. 6 demonstrates an alternative technique. The counter is reset to zero when a negative-going edge is simultaneously applied to the CLEAR inputs. This is obtained from the NAND gate, when the predetermined binary number, 1101 (13), is detected. The minimum duration between input pulses depends on propagation delays of flip-flops, the gate delay, and the reset delay. If the output is to be read, the lines should be gated to avoid transmitting spikes that will appear on some lines depending on the divisor N.

MSI integrated circuit packages e.g. SN7493 4-bit ripple counter contains a NAND gate for clearing, but additional gating is necessary for certain counts (see Table 1). Fig. 7 is the connection for $N = 11_{01}$, the feedback being applied via reset terminals $R_{0(1)}$ and $R_{0(2)}$. A useful arrangement for division by large numbers is shown in Fig. 8, where N_1 and N_2 must be prime numbers with respect to each other. The arrangement ($N_1 = 3$, $N_2 = 7$) provides $N = 21$; input pulses are applied simultaneously to each counter, and each cycles through its own modulus until all outputs are l's together, thus enabling AND gates, and resetting to zero via reset terminals.

High-power counters



Component values
R_1, R_2, R_3, R_4: 5 to 10Ω
R_5, R_6, R_7, R_8: 100kΩ
C_1, C_2, C_3, C_4: 0.47μF
D_2, D_4, D_6, D_8: 1N757
D_1, D_3, D_5, D_7: 1N914
SCRs: 2N1595
Tr_1, Tr_2: 2N1420
Tr_3: 2N657A

Performance
V_{CC}: 9V
Trigger amplitude −6 to 9V
width >200μs
Set pulse: 3V max
Maximum frequency: 1kHz
Minimum frequency: depends on capacitor losses, s.c.r. leakage current, and diode leakage current

Circuit description-1
Circuit shows a four-stage dynamic ring counter with power capabilities per stage of 20W at between 2 and 5A. Consider first the situation where all the s.c.rs are non-conducting. A set pulse applied at the gate of SCR_1 causes it to conduct freely via the load resistor R_1 and this continues in the absence of a set voltage until the supply is removed, which occurs when a trigger pulse is applied as base drive to Tr_2 is then shunted to ground, removing base drive to Tr_3. While the supply is applied to the counter and SCR_1 is conducting, point B is at ground voltage and C_1 charges via D_3, so that $V_{AB} = V_{CC}$. When the supply is removed, C_1 retains this charge as there is no discharge path (apart from leakage).

When the supply is reapplied, SCR_1 remains non-conducting and point B rises to the supply. Consequently, point A will rise to $2V_{CC}$. If D_4 is chosen so that its breakdown voltage lies between V_{CC} and $2V_{CC}$, breakdown occurs and SCR_2 conducts so that current flows in the second load, R_2. Further trigger pulses will cause each succeeding stage to conduct. Resistor R_6 allows C_1 to continue discharging below the zener voltage of D_4. Diode D_3 arrests this discharge so that the final condition is zero charge on C_1—which is the initial condition of C_1 prior to SCR_1 conducting.
Continual rotation of a single logic 1 is what has been described so far. Two adjacent logic 1's cannot reliably be rotated by this scheme but there is no reason why any

High-speed counters

Circuit description
In most counting arrangements the decoding of the end of the sequence and the resulting resetting of the counter occur in the same clock period. This can be avoided by using the philosophy of the circuit of Fig. 1 and thereby obtain increased counting speeds, irrespective of the logic family used. Circuit shows a frequency divider in which the second last number to appear on the output of the counters is decoded. This is done by the AND gates A_1 and A_2 and occurs on the falling edge of the clock pulse when A_0 goes to logic 1, corresponding to the number 97. Inputs J′ and K′ are then in the logic 1 state and the next clock pulse triggers the flip-flop and also the strobe pulse. The counter remains in this state until the clock pulse at the end of the 99th state toggles the flip-flop back again. The counter is then ready to start up-counting again from the initial state, which is, of course, dictated by the b.c.d. data inputs.
This arrangement allows the reset pulse to be a full clock period wide and unaffected by the counter states. Further, the decoding time and the reset time occur in different clock periods, rather than in the same period as in other methods.

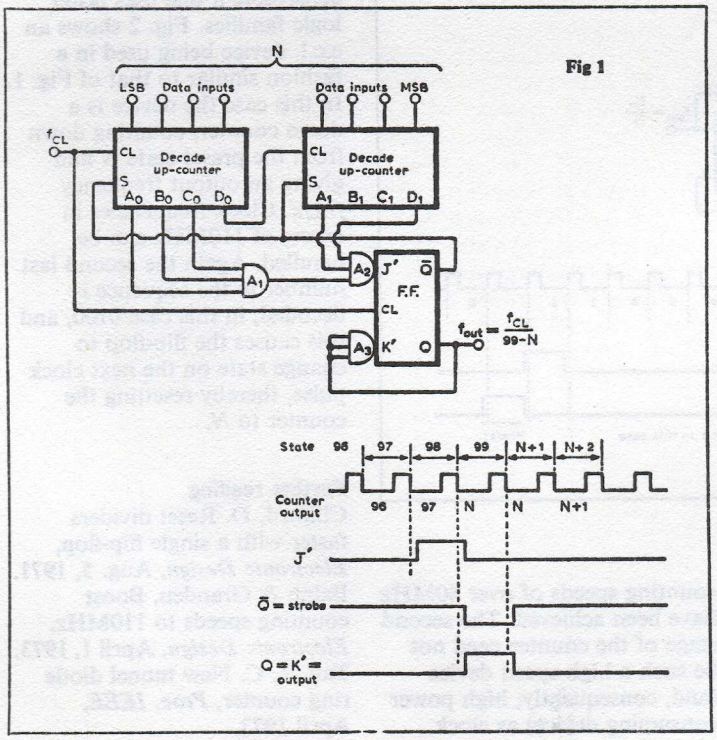


Fig 1

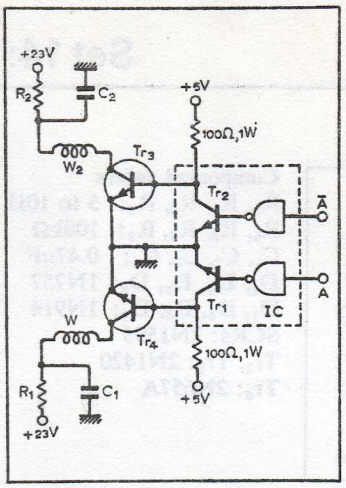
Components
Counters: 8290, decade up-counter for which the input data is on output when S is logic 0.
Flip-flop: 74H102 (high speed)
A_1, A_2, A_3: ½ MC3006

pattern cannot be rotated provided no two logic 1's are adjacent. Should more than one logic 1 be rotated then the supply section comprising Tr_1, Tr_3 and Tr_5 will require re-design as the current drawn if $n \times$ (current for one stage), n being the number of on stages.

To prevent noise falsely triggering any s.c.r., resistors between gate and ground should be provided.

Further reading

Strangio, High power counter drives 20W loads, *Electronics*, March 1, 1973.



Circuit description-2

A stepper motor drive is required to rotate a magnetic field pattern in either direction and at variable speed. This can be achieved by supplying the stator coils from an up-down counter with a variable pulse rate (see Card 4). Circuit shows ¼ of the drive circuitry for an 8-phase stepper motor with power consumption of 11W which is dissipated in only 4 of the phases at any one time. Two of these phases are shown in the diagram in the form of the 9 coils, W_1 and W_2. The motor operation requires that current flows in one of these coils at a time and this is achieved as shown. A and Ā are obtained from one stage of a 4-stage Johnson, up-down counter. If A is "high" then T_1 will not conduct and base drive is presented to T_4 and consequently current from the 23V supply will flow through W_1. Likewise no current flows through W_2 in this condition. However, if Ā is high the position is reversed. Tr_4 and Tr_8 are high current transistors capable of feeding inductive loads. R_1, C_1 and R_2, C_2 serve to reduce the circuit time constant so that higher speeds may be achieved.

Component values

R_1, R_2: 33Ω, 16W
C_1, C_2: 100μF, 40V
W_1, W_2: 9Ω stator coils
Tr_3, Tr_4: BSW 66
IC: SN75451P

Performance

Controlled by the torque characteristics of the motor. The coil current was 550mA and the maximum speed was 6000 steps per second, corresponding to a counter clock frequency of 6000 pulses per sec. A and Ā were normal t.t.l. voltage levels (5V and 0V).

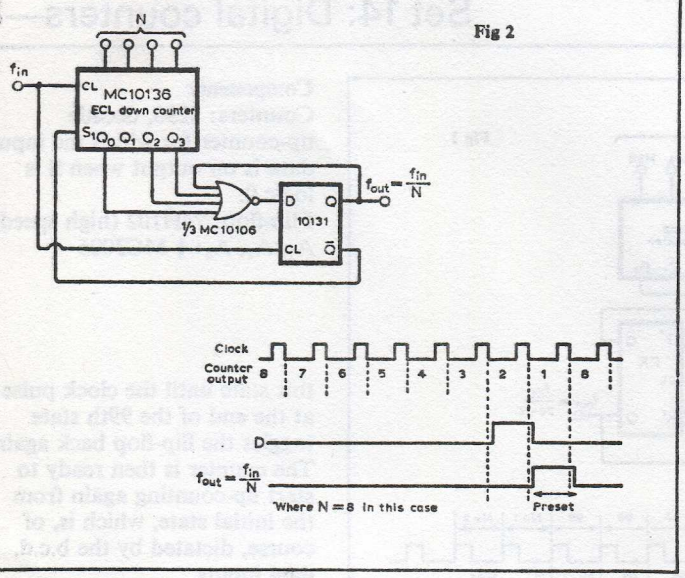
Further reading

Shakaiba, M. A. Digital eontrol system for an 8-phase stepper motor, Project Report, Electrical Engineering Dept, Paisley College of Technology.
King, D. S. Stepper motor for digital control systems, *Control and Instrumentation*, June 1971.
Fredrickson, T. R. Closed loop step motor, Proc. of Symposium on Pulse Rate and Pulse No. Systems, Budapest, 1968.

Cross reference

Series 14, card 5.

Fig 2



Hence the time taken for N to be fed in can be almost a full clock period and as a result higher clock frequencies can be handled.

With the devices quoted counting speeds of over 40MHz have been achieved. The second stage of the counter need not be such a high speed device (and, consequently, high power consuming device) as clock frequency to it is 1/10th of that to the first stage.

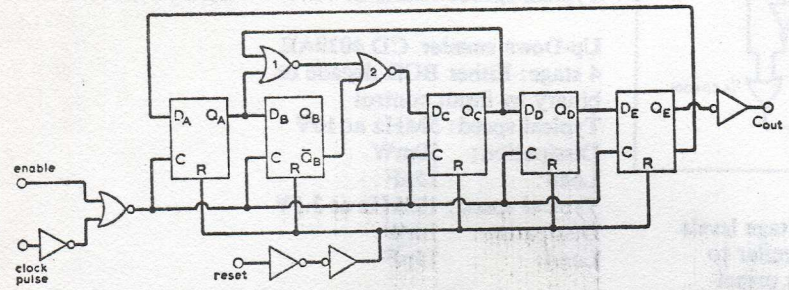
Higher frequencies are achievable if one uses faster logic families. Fig. 2 shows an e.c.l. device being used in a fashion similar to that of Fig. 1. In this case the device is a down counter, counting down from the preset state N and giving an output frequency $f_{CL/N}$. Clock frequencies in excess of 110MHz can be handled. Again the second last number in the sequence is decoded, in this case 0100, and this causes the flip-flop to change state on the next clock pulse, thereby resetting the counter to N.

Further reading

Clifford, D. Reset dividers faster with a single flip-flop, *Electronic Design*, Aug. 5, 1971.
Balph & Granden, Boost counting speeds to 110MHz, *Electronic Design*, April 1, 1973.
Tan, Z. C. New tunnel diode ring counter, *Proc. IEEE*, April 1973.

Low-power counters

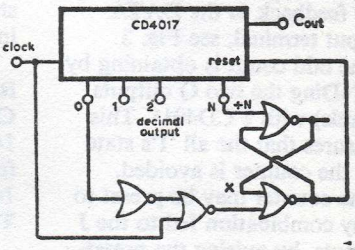
Fig 1



Package CD 4017AE
Temperature: −40 to +85°C
Typical speeds:
5MHz at 10V d.c.
1MHz at 3.5V
100kHz at 3.5V
Approximate power dissipation for the above values are 30mW, 1mW and 100μW respectively, for 15pF loading.
Minimum pulse width 100 nanoseconds at 10V.

Circuit description
The counter of Fig. 1 uses a Johnson configuration and obtains speeds in the region of 5 to 7MHz, each flip-flop operating at only one tenth of the input frequency. The counter is disabled if enable is high, reset to zero being achieved by applying a logic 1 level to reset. The counter sequences on the leading edge of each clock pulse, the Johnson code being maintained by ensuring that the D_C input is only high, when either Q_A and Q_B or Q_C and Q_B are high, via NOR gates 1 and 2. Additional gating (not shown) provides ten decoded outputs, which sequentially are high for one full clock period.
For count <ten, use quad-NOR i.c. CD4001. In Fig. 2 the cross-coupled pair is a reset latch, to ensure reset when flip-flops have different reset propagation delays. The decimal zero output is low except when counter is cleared, hence when the N output goes high, point X→0, and a reset pulse is generated while the clock is high. When counter resets, zero terminal goes high. This can drive another counter.

Fig 2



Decade counters

Circuit description
The four master-slave flip-flops of Figs. 1 and 3 are contained within one i.c. package, SN7490, and provides separate ÷5 and ÷2 facilities. A symmetrical decade counter where the period of the output pulse at Q_A is ten times the input pulse period with equal mark-to-space ratio is shown in Fig. 1, with the associated waveforms of Fig. 2. The J-K terminals with no inputs are internally connected to be logic 1. Flip-flop C toggles for all 1 to 0 transitions of Q_B, and D_D is set on the 4th pulse, but reset on the 5th pulse ($S = 0, R = 1$), thus setting Q_A. Q_B cannot change because $J_B = 0$, $K_B = 1$. For the next five pulses, the sequence of flip-flops B, C and D is similar, when Q_A is reset on the tenth pulse.

The connections of Fig. 3 allow the counter to sequence in an 8 4 2 1 b.c.d. code, where flip-flop D has the maximum weighting: gated direct reset lines (not shown) are provided to inhibit count inputs and return outputs to zero. Typical frequency and power dissipation is up to 18MHz, and around 160mW.

Another asynchronous 8 4 2 1 b.c.d. counter uses J-K flip-flops in a toggle mode (Fig. 4), has no logical hazards, and may be implemented with two SN7473 and one SN7400.

Fig. 5 is an 8421 b.c.d. synchronous counter, which requires 3-input AND gates of triple input J-K flip-flops. Q_A changes state for every clock-pulse (unused J-K inputs may be connected to logic '1'). Q_B changes on the 2nd, 4th, 6th, 8th clock pulses, but is inhibited from a 0 to 1 transition

Fig 1

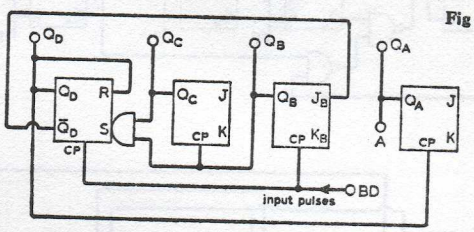


Fig 2

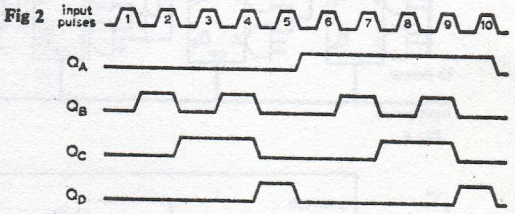
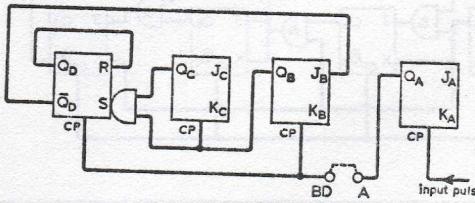


Fig 3



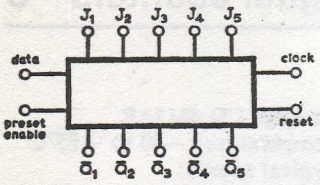


Fig 3

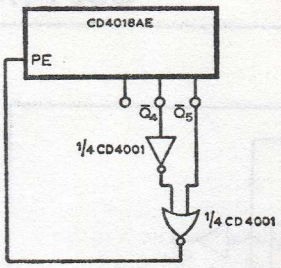


Fig 4

Programmable counter
$N = 1$ to 10 IC: CD4018
This is a 5-stage Johnson counter but with the Q outputs buffered with inverters to provide a Johnson BCD output. Counts less than ten achieved by feedback to the DATA input terminal, see Fig. 3. The odd count is obtaining by ANDing the two $\bar{Q}$ outputs (table) with ¼ CD4011. This ensures that the all '1's state of the counter is avoided. The counter may be preset to any combination fed to the J inputs, by pulsing the preset-enable input. Voltage levels and speeds are similar to CD4017AE. As a preset counter, counter will advance from preset state to 11110, where the right-most bit is $\bar{Q}_5$. The presence of $\bar{Q}_4$ and $\bar{Q}_5$ should be detected as shown in Fig. 4 to reset the counter.

Ripple counters
CD 4020AE
14 stages but outputs available from stage 1 and stages 4 to 14 inclusive.
Typical speed: 7MHz at 10V
2.5MHz at 5V
Power dissipation:
typical 1mW at 1MHz at 5V
10mW at 1MHz at 15V

CD 4040AE
12 stages
All 12 buffered outputs available
Typical speed: 8MHz at 10V.

Up-Down counter CD 4029AE
4 stage: Either BCD decade or binary by input control
Typical speed: 5MHz at 10V
Dissipation: 30mW
Load: 15pF
Typical speed: 100kHz at 3.5V
Dissipation: 1mW
Load: 15pF

Even count	*DATA*	*N*
	$\bar{Q}_1$	2
	$\bar{Q}_2$	4
	$\bar{Q}_3$	6
	$\bar{Q}_4$	8
	$\bar{Q}_5$	10

Odd count	*DATA*	*N*
	$\bar{Q}_1\ \bar{Q}_2$	3
	$\bar{Q}_2\ \bar{Q}_3$	5
	$\bar{Q}_3\ \bar{Q}_4$	7
	$\bar{Q}_4\ \bar{Q}_5$	9

Further reading
RCA Solid State Databook Series SSD-203A 1973

Cross references
Series 14, cards 4 and 10.
Series 11, card 6.

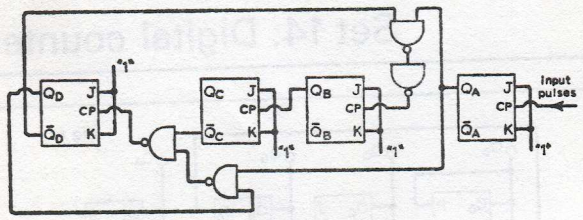


Fig 4

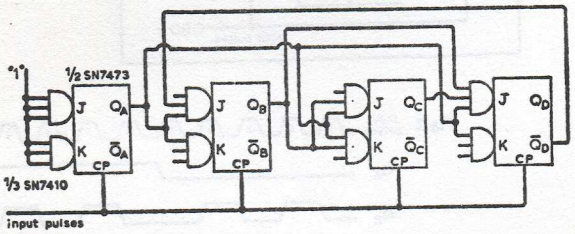


Fig 5

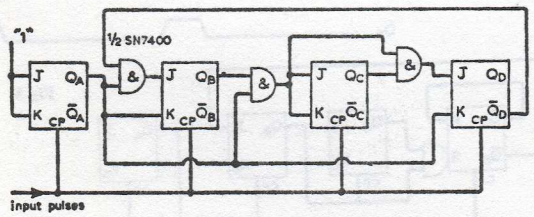


Fig 6

on the 10th pulse, since $\bar{Q}_D = 0$. Flip-flop C is toggled whenever $Q_A = Q_B = 1$, and Q_D undergoes a 0 to 1 transition when $Q_A = Q_B = Q_C = 1$, on the occurrence of the 8th pulse. Q_D resets to zero on the 10th pulse, because $J_1 = 0$ and the K inputs are high.

Implemented with either two SN7473 and three SN7410, or four off SN7472. Figs. 6 & 7 are two other forms of b.c.d. synchronous counters. Fig. 6 counts in 8421 code. Fig. 7 in excess-3 code. In each case the least significant bit is flip-flop A.

Further reading
T.T.L. Integrated Circuits, Counters and Shift Registers, application report CA102. Texas Instruments.
H. V. Malmstadt & C. G. Elke, Digital Electronics for Scientists, Benjamin, 1969.
Kohonen, T. Digital Circuits and Devices, Prentice-Hall, 1972.

Cross references
Series 14, cards 3 & 9.

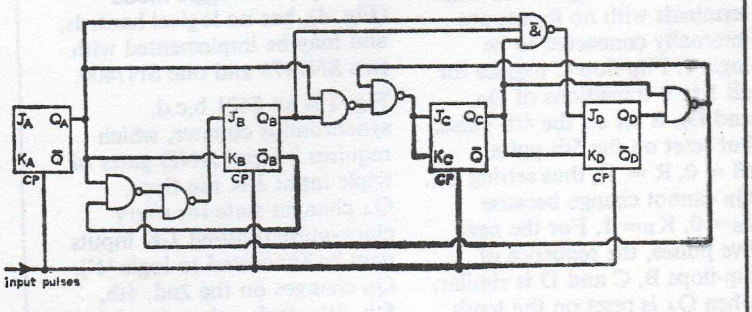
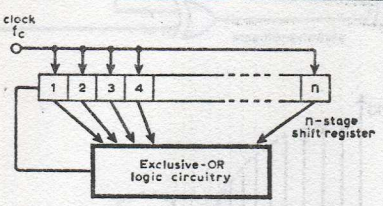


Fig 7

M-sequence generators

Fig 1



Description

Maximum length sequences (M-sequences) have many uses in data communications system identification and correlation methods. Some of them have properties very similar to that of band limited white noise, particularly if passed through simple first or second order R-C filters—hence the name pseudo-random-binary sequence (p.r.b.s.). They are produced by a simple synchronous shift register or counter with feedback from various stages determining the state of the first stage on receipt of each clock pulse. The feedback is basically by means of exclusive-OR gates (modulo-two gates). The basic diagram is as shown in Fig. 1, the output being taken from any stage. The sequence produced is cyclic and repeats itself after 2^n-1 pulses, the all-zero state being avoided. The maximum number of states for an n-stage register is 2^n but to prevent the all-zero state becoming a permanent state requires considerable extra logic and, hence, this state is avoided and the length 2^n-1 is described as maximal.

Long sequences can be generated by simple feedback arrangements. The Table indicates the simplest feedback arrangements for all those registers up to length 18, and all those beyond 18 and up to 33 which require only one exclusive-OR gate. Fig. 2 shows how the characteristic polynomials of the Table are interpreted in terms of hardware for the particular case of $n = 8$. If JK flip-flops are used as the register stages some simplification is possible

n	Characteristic Polynomial	J input	K input
2	$1 \oplus D \oplus D^2$	2	J
3	$1 \oplus D \oplus D^3$	3	J
4	$1 \oplus D \oplus D^4$	4	J
5	$1 \oplus D^3 \oplus D^5$	$2 \oplus 5$	J
6	$1 \oplus D \oplus D^6$	6	J
7	$1 \oplus D \oplus D^7$	7	J
8	$1 \oplus D \oplus D^3 \oplus D^5 \oplus D^8$	$3 \oplus 5 \oplus 8$	J
9	$1 \oplus D^4 \oplus D^9$	$4 \oplus 9$	J
10	$1 \oplus D^3 \oplus D^{10}$	$3 \oplus 10$	J
11	$1 \oplus D^2 \oplus D^{11}$	$2 \oplus 11$	J
12	$1 \oplus D \oplus D^4 \oplus D^6 \oplus D^{12}$	$4 \oplus 6 \oplus 12$	J
13	$1 \oplus D \oplus D^3 \oplus D^4 \oplus D^{13}$	$3 \oplus 4 \oplus 13$	J
14	$1 \oplus D \oplus D^6 \oplus D^{10} \oplus D^{14}$	$6 \oplus 10 \oplus 14$	J
15	$1 \oplus D \oplus D^{15}$	15	J
16	$1 \oplus D \oplus D^3 \oplus D^{12} \oplus D^{16}$	$3 \oplus 12 \oplus 16$	J
17	$1 \oplus D^3 \oplus D^{17}$	$3 \oplus 17$	J
18	$1 \oplus D^7 \oplus D^{18}$	$7 \oplus 18$	J
20	$1 \oplus D^3 \oplus D^{20}$	$3 \oplus 20$	J
21	$1 \oplus D^2 \oplus D^{21}$	$2 \oplus 21$	J
22	$1 \oplus D \oplus D^{22}$	22	J
23	$1 \oplus D^5 \oplus D^{23}$	$5 \oplus 23$	J
25	$1 \oplus D^3 \oplus D^{25}$	$3 \oplus 25$	J
28	$1 \oplus D^3 \oplus D^{28}$	$3 \oplus 28$	J
31	$1 \oplus D^3 \oplus D^{31}$	$3 \oplus 31$	J
33	$1 \oplus D^{13} \oplus D^{33}$	$13 \oplus 33$	J

Glossary: flip-flops and b.c.d. codes

Integrated circuit flip-flops are usually clocked i.e. the change of state is initiated by a timing pulse called the clock pulse. The outputs are commonly termed Q and $\bar{Q}$. If $Q = 1$, $\bar{Q} = 0$ (and vice versa). These states are dependent on the logical states of the flip-flop (or bistable) inputs and this dependence is shown in each associated TRUTH table, where Q_n is the state of the Q output after the nth pulse, and Q_{n+1} is the new state after the next pulse.

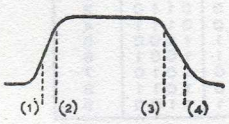
When Q is made to be logical '1', the flip-flop is said to have been SET, and when Q is made '0', the flip-flop has been RESET or CLEARED. Edge-triggered and master-slave types are available. The time for which data must be present before the clock pulse threshold (set-up time) and the time for which data must be maintained after the clock edge (hold time) are normally specified. The transfer of information in the master-slave flip-flop is according to the numbers marked on the pulse shown, and it may be considered that the master and slave flip-flops are distinct, but isolated or connected by gates.

(1) slave isolated from master

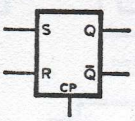
(2) data entered into master

(3) master is isolated from input terminals

(4) data is transferred from master-to-slave



R-S flip-flop



SYMBOL

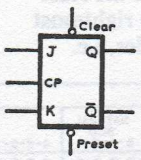
S	R	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	x

x = indeterminate

TRUTH TABLE

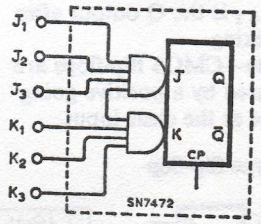
R = S = 1 must be avoided because the logical value of the Q output is uncertain.

J-K flip-flop



J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

This has two data inputs termed J and K (and may be considered to be similar to S and R of the R-S flip-flop), but no indeterminate state exists for any combination of the inputs. Multi-input J and K terminals are achieved on some i.cs with internal gating, where the J and K inputs are for example the ANDED inputs J_1 J_2 J_3 and K_1 K_2 K_3. CP is the clock-pulse terminal, Preset and Clear terminals may also be available. These inputs are maintained normally at logical '1'. A negative edge applied to PRESET, sets $Q = 1$, and if applied to CLEAR, makes $\bar{Q} = 1$. The negative edge triggering can be indicated by the small circle at the terminal as in diagram.



if the polynomial contains D to the power one. Column 3 or the table indicates the logic necessary for the J input and column 4 indicates the K input.

If the output of stage 1 is regarded as the output, versions of this sequence delayed by $L\Delta T$, where ΔT is the clock period and $L = 0$ to $n-1$, are clearly available from the remaining stages. Delays of up to $N\Delta T$, where $N = 2^n-1$ can also be generated by modulo-two addition of several of the output stages (ref. 1).

When the sequence is being used as a noise source the output is arranged so that logic $1 = +a$ volts and logic $0 = -a$ volts. The r.m.s. value of the waveform is than a^2 and the mean value is a/N (this would be zero if $N = 2^n$ rather than 2^n-1). The power spectrum, which is discrete, is where $a(k)$ is the power in (volt)^2 of the kth harmonic. $G(k)$ is shown in Fig. 3. The small d.c. term is often ignored.

Spacing between the lines of Fig. 3 is $1/N\Delta T$ and hence the power density spectrum (power per unit bandwidth) is $G(k)N\Delta T$. The 3-dB point for the power density spectrum occurs at approximately $1/3\Delta T$ so that for systems with bandwidth less than $1/3\Delta T$ the signal appears as white noise. Further, the autocorrelation function for the signal is very similar to that for white noise (ref. 1). The probability distribution of the signal is not at all Gaussian because it consists of two lines at $\pm a$ respectively. However, when passed through a suitable R-C filter with a break point less than $1/3\Delta T$ the distribution does become close to Gaussian i.e. that for band-limited white noise (ref. 2).

$$G(k) = \frac{a^2}{N^2} + \sum 2a^2 \frac{(N+1)}{N^2} \left(\frac{\sin \frac{\pi k}{N}}{\frac{\pi k}{N}} \right)^2$$

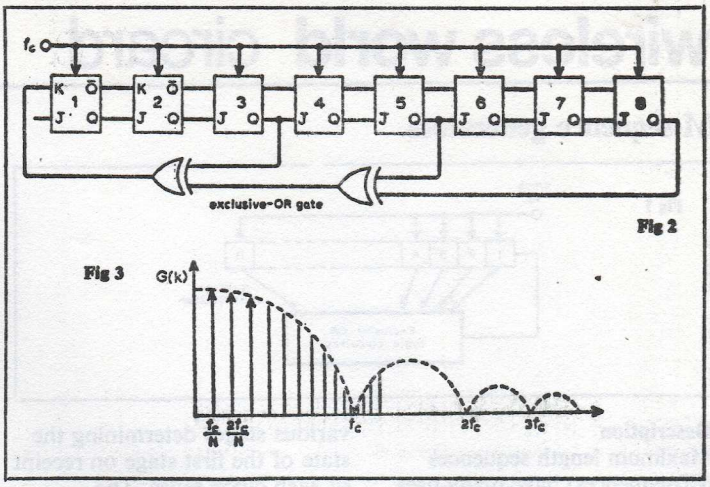


Fig 2

Fig 3

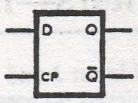
References

1. Davies, W. D. T., Generation and properties of M-sequences, *Control*, June, July and August 1966.
2. Roberts, P. D. & Davis, R. H., Some statistical properties of smoothed M-sequences, *Proc. I.E.E.* 1966 vol. 113, p.190.

Further reading

Davies, A. C., Design of feedback shift registers and other synchronous counters, *Radio and Electronic Engineer*, April 1969.
Peterson, W. W., Error Correcting Codes, MIT Technical Press 1961.
Golomb, S. W., Shift Register Sequences, Holden Day 1967.

D-type flip-flop



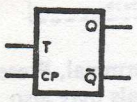
SYMBOL

D	Q_{n+1}
0	0
1	1

TRUTH TABLE

This has one data input, and may also have both outputs available. In the table, D is the input before clocking and Q_{n+1} is the Q output after clocking.
Note—CMOS flip-flops are cleared by a positive-going edge at the clear input.

T-type flip-flop



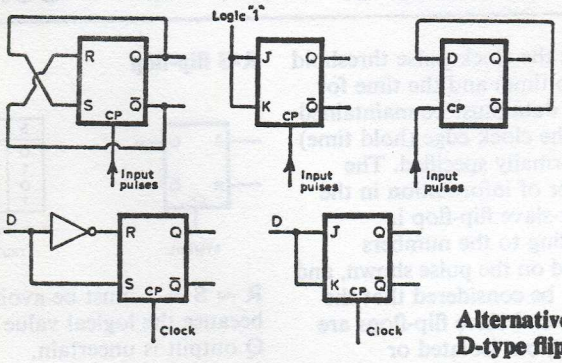
SYMBOL

T	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

TRUTH TABLE

This may be considered as the basic binary or toggle flip-flop. When T = 0, the Q output will not change state on the occurrence of a clock pulse. If T = 1, Q takes up the opposite state when the flip-flop is clocked.

Alternative toggle flip-flop



Alternative D-type flip-flop

Decimal codes

These are listed with the least significant bit (LSB) rightmost for the weighted codes, i.e. those in which a decimal numerical weighting is assigned to each bit position.

JOHNSON	NATURAL BCD 8-4-2-1	4-2-2-1	GRAY	EXCESS-3	DECIMAL NUMBER
00000	0000	0000	0000	0011	0
00001	0001	0001	0001	0100	1
00011	0010	0010	0011	0101	2
00111	0011	0011	0010	0110	3
01111	0100	1000	0110	0111	4
11111	0101	0111	0111	1000	5
11110	0110	1100	0101	1001	6
11100	0111	1101	0100	1010	7
11000	1000	1110	1100	1011	8
10000	1001	1111	1101	1100	9

Further reading

Walters, D. J. Integrated Circuit Systems, Iliffe Books, 1971.
Malmstadt & Elke, Digital Electronics for Scientists, W. A. Benjamin, 1969.
Texas Instruments Inc. Designing with TTL Integrated Circuits.

Cross references

Series 14, card 5.
Series 14, card 3.