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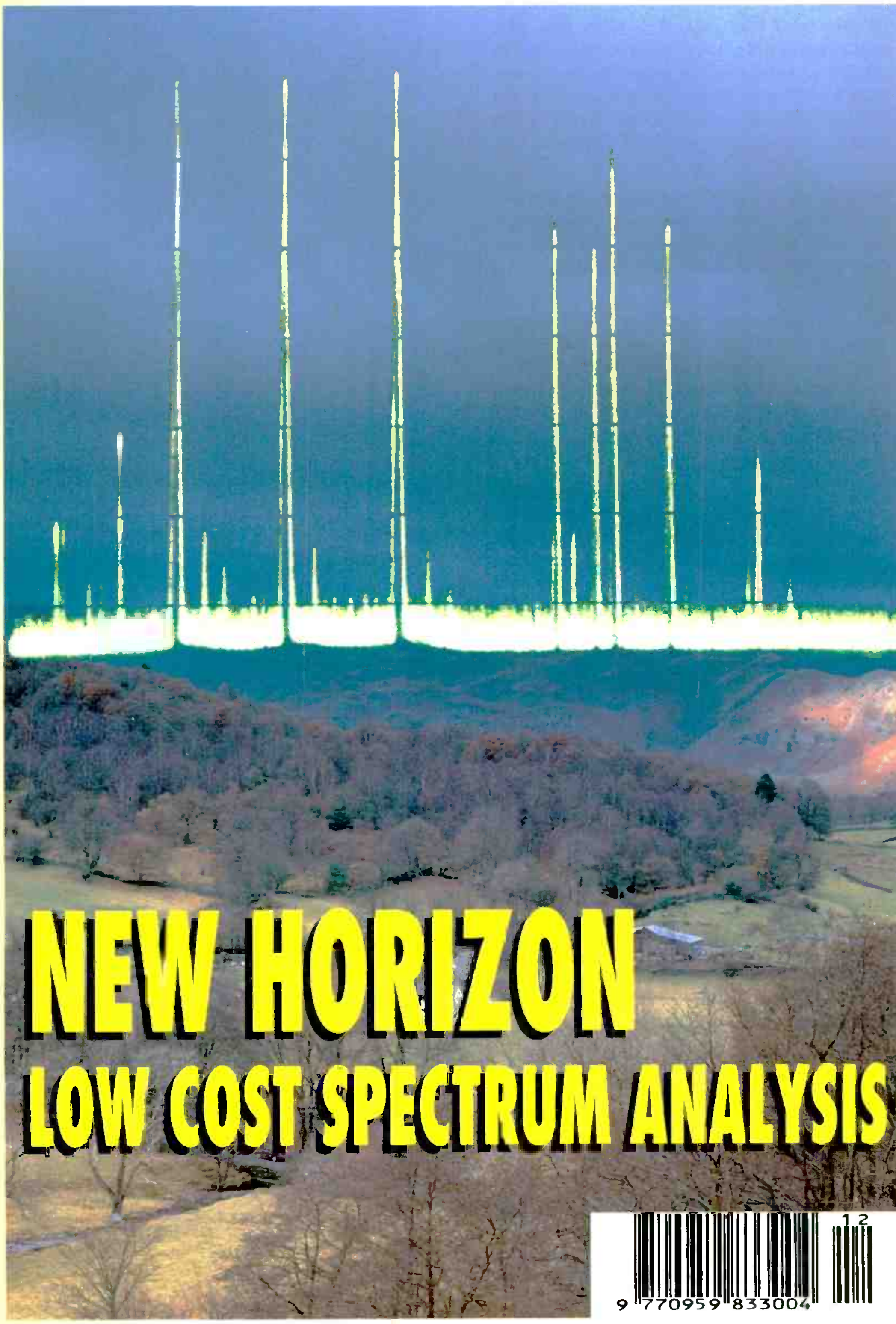

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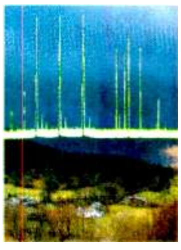

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REGULARS

In next month's issue: Designing a microprocessor controlled power supply. Matthew Rahman details a fully keypad-programmable, multi-rail laboratory instrument. His article provides detailed circuits and documented source code for the Z80 processor at the heart of the design. This code will be made available to readers on disk.

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REED BUSINESS PUBLISHING

New challenge for amateur radio

When was the last time that you read or heard something positive about amateur radio? I can't remember either. Everyone recalls and enjoys the Hancock sketch where the man himself played a pompous, petty and technically incompetent ham communicating with a world where everybody wanted to talk and nobody wanted to listen. We remember Tony Hancock's radio amateur because it encapsulates truth about the hobby more accurately than any words that we might write about it. Amateur radio desperately needs a new reason for its continued existence.

Radio communications was the principal driving force behind electronics development from its beginnings until the end of the second World War. It was used to tie empires to their mother countries, and then as an instrument of war itself when empires disintegrated. Radio hams found themselves involved in research and development, especially in the early days of radio, and then as a source of specialised skills in the war years.

There was a post–war surge of interest fuelled by the availability of surplus equipment, most of which required technical competence to adapt for amateur use. But when this was gone, radio amateurs became simple consumers and mostly bought their equipment off the shelf losing much of their technical independence and usefulness. Galton and Simpson were now able to document Hancock's radio ham.

Somewhat paradoxically, the intellectual decline in amateur radio reached a trough when the numbers engaged in the hobby peaked in the early Eighties. Two factors combined and contributed in this. Firstly, the multiple choice entrance examination was an order of magnitude easier to pass than its written predecessor; secondly, radiocomms as a hobby was massively popularised by the CB boom. Most of the new influx could contribute nothing except self-conscious and inane chatter using equipment which owed more to credit card companies than the owners' technical competence. We are now seeing a decline in the number of radio amateurs as the novelty wears off.

Naturally, this jaundiced view does not tell the whole story. One only has to look to the work of Amateur satellite groups and the activities of Surrey University to appreciate that some aspects of the hobby remain challenging, educational and useful. A few enlightened souls still manage to push the bounds of RF design engineering, usually by combining the demands of their jobs with the pursuit of their hobby. But if amateur radio is to command any respect – and retain its frequency allocations and privileges – it must take up new challenges.

The market requirement for cordless communications once again casts RF engineering as a driving technology. While it seems unlikely that amateur radio could contribute directly at chip level development, it has a role to play in enthusing and educating the next generation of RF engineers. As editor of this magazine, I hope to hear from radio amateurs prepared to experiment with direct digital synthesis, IF band DSP, spread spectrum communications, high performance small signal and large signal RF systems, broadband design techniques and packet transmission, etc.

If amateur radio finds itself incapable of, or indifferent to accepting a new challenge, then it does not deserve to survive.

Frank Ogden G4JST.

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ISDN does it now

Unkindly dubbed "it still does nothing", isdn (which actually stands for integrated services digital network) used to be regarded as an advanced telecommunications technology in search of an application.

All of a sudden, there are many applications as BT demonstrated in a recent series of briefings tied to the start of the Whitbread Round the World yacht race. BT will be using isdn as the final link in delivering compressed, digitised tv pictures transmitted via satellite from the yachts to be reconstituted by video codec at Reuters' west London studio.

Virtual application or virtual reality? ISDN promises telepresence by allowing the direct transmission of digitised, compressed video images over the public switched network. Real applications, such as remote data gathering, are only just starting to appear.

More mundanely, isdn is transmitting high-quality artwork between studios and clients, and letting users access and search photo libraries – and receive the images – by phone. House hunters can view properties without leaving estate agents' offices, and car buyers specify the options they would like, build the model on screen and view it from various angles, outside and in. Hairstylists can show customers how they would look with various styles, called up from a centralised databank and framed around their own faces.

In France the FNAC record store chain already has in-store multimedia music sampling terminals updated by isdn.

The technical and human possibilities of isdn, however, far exceed the replacement of motorcycle couriers or provision of a telephone jukebox. Peter Cochrane, research manager at BT's Martlesham Heath laboratories, described them as "virtual teleporting".

"Of necessity," he said, "we are going to have to replace physical travel with telecommunications and telepresence." He looks forward to "being able to communicate with other human beings on the basis of eye-contact, gaze awareness – right size, right colour, looking real." As an end-to-end digital link with bandwidth in excess of 50kbits/s, conveying sound, video, text and data in broadcast quality, virtually error free, isdn will soon provide that facility.

Already, via endoscopy, a surgeon can hold a case conference, in effect inside a patient who is many miles away, with colleagues also at distant locations.

At Southampton, BT introduced a surrogate head, using 3D wideband isdn technology. A user on-site wearing lightweight cameras on spectacle frames, transmits virtual reality images back to, for example, a technical expert or a surgeon, who can conduct the repair, examination or operation without leaving his or her base.

"Virtual reality may take out multimedia," predicted Cochrane. "It's much more natural and versatile."

The other advantage of isdn is its economy of telecommunications capacity. Cochrane predicts that the local call area will grow quickly at national and continental level to become global. Even now, NatWest Securities can send closing prices from the Paris Bourse to Edinburgh in 25s. A fashion retailer has reduced overnight polling (data-gathering) from 15min to 35s per store.

Although isdn is at its best on fibre optics, it can be carried on existing paired copper cables – usefully increasing their capacity – in a service called ISDN 2.

A package for retailers proposes to put all their voice links, epos data polling, credit card authorisation, and security video monitoring, each of which has its own dedicated line, onto one ISDN 2 line.

As the Whitbread sailors are being pounded around the world on the ocean wave they can reflect on the irony that the technology they are helping to test will one day mean that no-one need leave home again.

Peter Willis

Mirror, mirror on the chip

The possibility of aluminium mirrors projecting tv images from conventional cmos srams takes a step closer this month as scientists from Texas Instruments explain that they have improved the contrast ratio of their micromirror device to a level that can compete with standard crts.

The announcement will come between the 5th and 8th of December in Washington at the International Electronic Devices Meeting, one of the leading technical conferences for breakthroughs in semiconductors and other electron devices.

TI's device is a monolithic array of rotatable aluminium mirrors integrated on to the sram chip. Each sram cell controls the rotation of the overlying mirror via a piezo ceramic plug that changes shape depending on the charge on the cell.

Since the device was first announced, Texas Instruments has made structural improvements, increasing the contrast ratio to more than 100:1, a level necessary to compete with cathode ray tubes.

The firm will also describe the latest results from a research programme started in 1988. This programme is aimed at cutting the costs of chip production. A mini-factory in a 5000 cubic feet cleanroom has been built for 0.35µm chip fabrication that has achieved a world record wafer cycle time of three days.

Traditionally many wafers are subjected to the same manufacturing steps simultaneously, and large numbers of chips are made all at once. But the need to keep large open cleanroom spaces dirt free and the use of large, complex and expensive

Microscopic rotatable mirrors fabricated on conventional static ram cells could result in a technology to compete with CRTs. This picture was formed by reflection from the micromirrors.

capital equipment has driven production costs through the roof.

This logic has been turned on its head by TI with the idea of making only one finished wafer at a time from start to finish using a smaller and therefore less expensive cleanroom. Various advanced vacuum processors are used to speed up the thermal processing of the wafers.

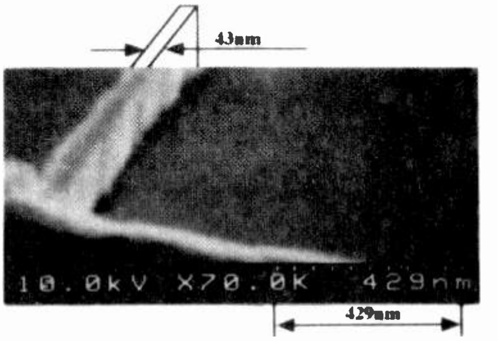
If the cleanrooms are shrinking so are the chips being made in them. For example, Toshiba will describe what it claims to be the smallest mos transistor ever built – a 40nm gate-length device. Sidewalls are from phospho-silicate glass and are 200nm thick.

Additionally, AT&T Bell Laboratories will describe the fastest cmos IC ever built with a gate delay of 11.8 picoseconds. It is built with 0.1µm cmos technology.

As expected at any conference of this type the industry driving force of more memory in less space is represented. With 16Mbyte chips starting to appear, eyes are turning to 256Mbyte drams, which are forecast to hit the market in about five years.

A paper from the IBM, Siemens, and Toshiba joint research team describes a 256Mbyte dram with a 0.6µm^2 trench cell structure. The cell is 25% smaller than conventional structures.

More than 200 invited and contributed research papers will be presented.



Smallest transistor in the world? Birdseye view of a gate electrode after poly-silicon reaction ion etching. Gate length obtained is 40nm.

Video disc recorder may rival tape

Engineers at Samsung's Advanced Institute of Technology are close to developing a digital video recorder using discs instead of tape.

Scheduled for launch in 1995, the machine will use magneto-optical erasable discs. But the Korean company can expect fierce competition from Japanese competitors such as Matsushita and Sony.

Both are working on digital video disc and tape recorders. Samsung hopes that the key laser component, developed with Russian engineers, will put it ahead of the Japanese by several years.

Korean electronics companies Samsung, Goldstar and Daewoo have the reputation of being efficient, low cost makers of technology developed elsewhere. Samsung though wants to start setting new standards.

When broadcast tv pictures are converted into digital code, the data stream runs at more than 200Mbit/s. Data compression according the MPEG-2 standard can reduce this by about 30:1 to 8Mbit/s, while still delivering quality that matches the Super-VHS tape system. But at this data rate a 12cm cd, with capacity of 600Mbyte, can store only about 10 min of video.

Samsung's storage target is a feature film up to 110min on a single disc. The first step is to make the disc double-sided, and 13cm in diameter, matching the size of magneto-optical discs already made for the computer industry and so benefitting from existing investment in manufacturing plant.

To store 55min on each side of a 13cm disc requires a data capacity more than 25Gbyte per side. To achieve this the pitch of the spiral track of data pits is reduced from 1.6µm for cd to 1µm, and the length of the data pits reduced from 3 to 0.3µm.

The beam from an infra-red laser as used in a cd player or existing disc recorder cannot be focused tightly enough to read such small pits; the wavelength is too long.

The Japanese are developing solid state blue lasers to do the job. Samsung's strategy has been to base the D-VDR on green laser light; predictions are that the high power blue lasers needed for recording onto disc will not be available at consumer prices until towards the end of the decade. Samsung believes green laser technology will be ready to sell by 1995 and this will put the D-VDR far enough ahead of the Japanese to create a de facto standard.

There is no high power solid state green laser yet but in 1991 SAIT engineer Insik Park went to Russia and saw how the IOFFE Technical Institute in St Petersburg was getting green light from infra-red lasers. Samsung signed a deal which brought Russian engineers to Korea for two years to work the D-VDR.

The technique is known as second harmonic generation. The source light is infrared from a 500mW GaAs laser, with wavelength of 0.8µm. This is beamed into a crystal of yttrium-aluminium-garnet doped with neodymium.

The infra red pumps the yag into lasing action that emits coherent light at a wavelength around 1µm. This light is then beamed into a second crystal of KTP (potassium titanyl phosphate) that has a non-linear optical characteristic and generates a second harmonic of the input frequency at 0.5µm. Thus the system emits coherent green light at a power of 20mW, strong enough to record onto the disc.

The US military has been working on the same technique to communicate with submarines, because sea water has an optical window at this wavelength. Very probably the work done in Russia was originally commissioned by the military. The practical difficulties, for instance keeping the infra-red laser cool enough to avoid self-destruction, have deterred electronics companies from trying to use the system for consumer products. US researchers used Peltier junctions. Samsung thinks the help it got from Russia makes the system affordable.

Said Insik Park: "Russian engineers are a lot cheaper than Japanese, and Japanese are reluctant to transfer technology. So it is much easier to hire Russian engineers."

SAIT recently showed a prototype video disc recorder spread out over a laboratory bench. This makes the 1995 target for a consumer launch seem optimistic but Samsung has a good track record of delivering promises on time.

Barry Fox

Dodgy chips beat gold and drugs

Stolen chips are worth more than gold or drugs, according to police fighting a growing microprocessor crimewave in Silicon Valley.

But some firms are fighting back. Intel is giving its microprocessors serial numbers following robberies that have led to a thriving grey market in 486 chips.

Intel will stamp serial numbers on its microprocessors and possibly extend the numbering system to other products. Other US semiconductor makers are also expected to announce that higher priced chips will have serial numbers.

In the most recent armed robbery, TEG Micro Technology in Fremont, California had more than $500,000 worth of chips stolen, mostly i486 microprocessors valued at more than $400 each. Two other armed robberies of Fremont businesses netted more than $300,000 worth of chips just weeks before the latest robbery.

Police say robbers can easily unload the chips in the grey market. Once they reach the grey market they are untraceable.

The serial number scheme is also intended to prevent the growing number of thefts by chip company staff who can easily smuggle out a handful of chips and earn hundreds of dollars.

Police say more chips are lost through staff theft than armed robberies.

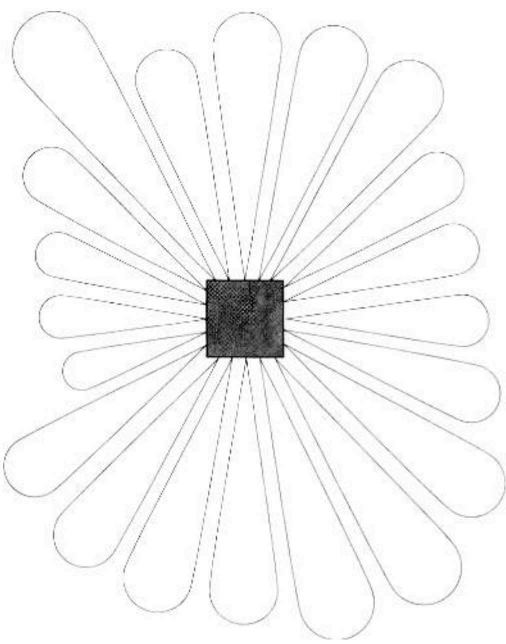
Antenna boost for cellular phones

A redesigned antenna looks set to save costs and give better coverage for cellular telephone services.

Called SmartAntenna and developed by Northern Telecom, the device uses four flat antenna panels mounted on a mast. Each panel can send out five overlapping beams that can be individually adjusted for strength.

This means the coverage area can be tailored to requirements with higher strength beams hitting built up areas, for example.

It also gives more flexibility in the positioning of the antenna; the base station no longer needs to be at the centre of the cell.



Multiple beam, flat-plate antenna allows propagation to be tailored to the terrain in any direction.

The mast is connected to a control module and radio base station in a cabin at the foot of the tower. Active electronics in the masthead and cabin comprises five functional blocks. The first is the antenna array itself along with beamformers and duplexers. Secondly, there is the switch matrix for transmit and receive that switches multiple transceivers into a single beam.

Dual redundant low noise amplifiers for each receive beam are fitted in the masthead equipment.

The control module in the cabin is responsible for switching the best transmit and receive beams to each of the transceivers on a timeslot by time-slot basis. Selection of the best beam is made according to received signal amplitude.

Finally, transmit power amplifiers, hybrid combiners and duplexers are fitted at the masthead. Test and alarm functions are distributed throughout the system.

Each plate antenna covers a 90° arc with its five beams. Each beam covers a fixed 18° arc and is controlled by changing the gain. Because of the higher gain, the antenna has about twice the range of a standard omni cell in rural areas, which can cut the number of base stations by up to 75% compared with omni cell sites and 50% compared with tri-sectored cell sites.

Improved carrier to interference ratio allows greater frequency re-use. Each time slot of each transceiver can be allocated to any mobile on any radial beam. Shadowing caused by buildings is also cut, reducing the number of dropped calls from mobile users.

Increases in receive sensitivity let mobiles transmit at lower power, increasing battery life and talk time.

Nortel Matra's cellular pcn system for providing DCS1800 networks in Europe will be the first to use the antennas.

Joint development sees 64Mbit dram samples

Siemens and IBM are sampling the 64Mbit dram they co-developed, but have yet to decide whether they will combine forces to make it.

Asked if sampling the chip to potential customers meant Siemens intended to supply it as a product, a representative replieda: "If we are sampling I understand that someone might be interested to manufacture it."

But he added: "Our development agreement with IBM does not include joint manufacturing."

Siemens' options on making the chip are "completely open" he said. "Both parties are negotiating the question what to do now."

IBM and Siemens reckon the decision is not urgent because first production of the 64Mbit will not be required until late 1995, ramping up to volume production in 1996.

"We are not in a hurry," said the Siemens representative. "We'll decide later next year."

Since it takes 18 months to build a wafer fab and bring it into production, the building works would have to be started in June 1994 for there to be any chance of making first silicon by late 1995.

As well as the 64Mbit deal, Siemens and IBM jointly make 16Mbit drams and share with Toshiba a joint research and development effort on the 256Mbit dram.

Esprit to go more commercial

The vice-chair of the European Commission, Martin Bangemann, has challenged critics of EC funded research saying future Esprit programmes will be tailored to produce more commercial results and products.

The fourth framework of projects to be awarded under the Esprit programme will, he said: "not only focus on technical challenges, but will ensure that the special activity will be noticed by the general public."

Bangemann, who is also commissioner in charge of information technology, said the previous policy of Esprit projects concentrating on "precompetitive development" led to accusations that the commission was spending money on nothing.

He rejected such charges saying: "It is not true that our programmes have no results, but the wider public is often unaware of them."

Bangemann was speaking at the launch of Goldrush, a computer from ICL that uses parallel processing technology. It was developed as part of an Esprit project called EDS.

Goldrush is a database server that can have up to 127 *Hypersparc* risc microprocessors.

Bangemann said: "Our future depends on quick acceptance of developments. We must see to it that European enterprises gain advantage through early access to products offered."

Philips to make monitor tubes in Austria

Philips is to start producing colour monitor tubes at its factory in Lebring, Austria.

About 29 million Dutch guilders are being invested to add 0.4 million monitor tubes to the 2 million cathode ray tubes already produced.

European demand for monitor tubes is expected to double from 2.5 million pieces a year to 5 million by 1997.

Monitor tube production will start late next year ending the monopoly of imports from the Far East. First off the line will be 15in tubes followed soon by 17in models.

Around 40 jobs will be created and some existing staff will be retrained to work on the new line. Philips already produces 2.5 million monitor tubes a year at its Taiwanese factory. ■

RESEARCH NOTES

Can noise improve your hearing?

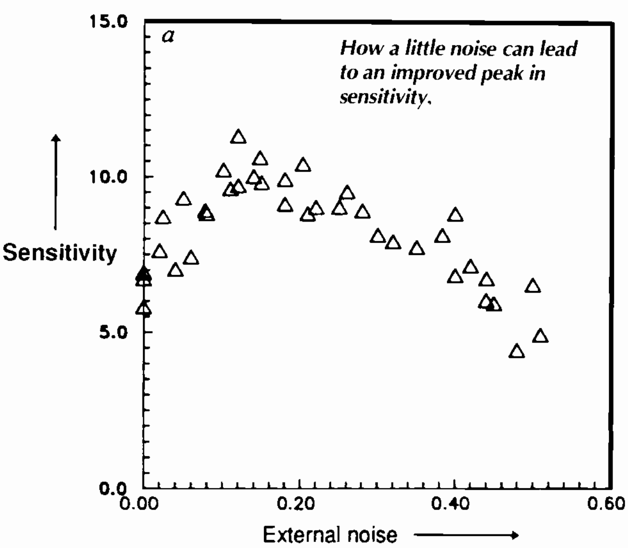
Traditional engineering wisdom takes for granted the assumption that you can hear better in a quiet environment. But workers in the US have been questioning that fact by using increased background noise to improve s/n ratios – with a little help from a crayfish.

In electronics design, great emphasis has always been placed on low-noise circuitry, whether for domestic audio or in rf front-ends listening for errant Martian spacecraft.

According to conventional linear information theory, random noise is detrimental to the transmission of data: end of argument... well, not quite.

Frank Moss and colleagues from the University of Missouri at St Louis have shown that a small amount of random noise may enhance, rather than obscure weak signals. Experiments to confirm this speculation (*Nature*, Vol 365, No 6444) were conducted, not with conventional electronic components, but with pick-up devices unlikely to be found in the average engineer's tool-bag. Moss and his team used specialised biological cells called mechanoreceptors, taken from crayfish tails.

As the name suggests, the normal function of these cells is to detect tiny water movements that might signal the presence of some larger and hungrier species. Because they are always working at (or beyond) the limits of conventional information theory in a permanently noisy environment, they were regarded as a good starting place to investigate the possibility of enhanced signal-to-noise performance.



How a little noise can lead to an improved peak in sensitivity.

The rather counter-intuitive notion that noise might actually improve performance derives from some research conducted over a decade ago into periodicities in climate. This work, together with later theoretical studies, showed that, in certain non-linear systems, the information content of a weak signal can be enhanced by noise through "stochastic resonance" in which the output coherence relative to the output noise passes through a maximum at an optimal value of the input noise. In other words a little noise does you good.

At the University of Missouri, Moss and his colleagues wired up the crayfish cells and stimulated them by moving water back and forth. The cells are so naturally sensitive that the equipment had to be isolated from everyday building vibrations at 10Hz and lower. What the team were trying to assess was the extent to which randomly-introduced water fluctuation affected the cells' ability to respond to regular periodic fluctuations.

When the effective signal-to-noise ratio of the system was computed from the measured electrical activity of the cells, Moss found very clear evidence of a certain noise intensity at which the s/n is a maximum. This improvement is about 4.5dB compared with the figure in the absence of noise.

Whether this enhancement is something that Nature has evolved to make the best of a noisy environment is a question as yet unanswered. But it does seem that the crayfish is by no means unique. Moss and his colleagues draw attention in their paper to various psycho-physical studies that have hinted at the existence of this effect in human visual perception. People, it seems, are much better at perceiving ambiguous shapes when they are presented in the context of visual "noise". Stochastic resonance is clearly not something which will improve the performance of conventional linear transducers. But in any artificial intelligence system or information processing context where non-linearity plays a part, we might well learn a lesson or two from the humble crayfish.

Fermat's ghost laid to rest?

For close on 400 years mathematicians have puzzled over one of the most intriguing numerical mysteries, the so-called last theorem of Pierre de Fermat. Fermat was a 17th century Frenchman who asserted that, for any whole number n greater than 2, the equation $x^n + y^n = z^n$ has no solution for which x,y and z are whole numbers greater than zero. What makes this assertion so intriguing is Fermat's tantalising hint that he knew a wonderful proof. But Fermat claimed he had no space in his notebook to write it down. The search for it has been a challenge to mathematicians ever since.

Over the years, the "theorem" has been verified in different ways for a variety of specific values of n. Number-crunching computer studies in the USA have recently validated Fermat's assertion for values of n up to 4 million. But a general proof has remained elusive... until a surprise announcement by Andrew Wiles, a British mathematician working at Princeton University.

Wiles' break-through follows some ground-laying by other workers who have progressively established links between Fermat's assertion and the properties of elliptic curves. Key to this is the so-called Taniyama conjecture, named after the Japanese mathematician Yutaka Taniyama. Proof of the Taniyama conjecture is generally agreed to amount to proof of Fermat's theorem.

Andrew Wiles has now presented a 200 page proof of the Taniyama conjecture, causing excitement for mathematicians all over the world – those who can understand it!

Some experts are saying that Wiles proof might take as long as a year to check over thoroughly, though it is said to look good. Establishing Fermat's assertion as a true theorem – something that can be proved as a general statement – will be far more than just a *tour de force* of number crunching. Mathematicians who have studied Wiles' work say that it will provide a valuable new tool to open up whole areas of number theory. One wonders if that's what Pierre de Fermat had in mind all those years ago.

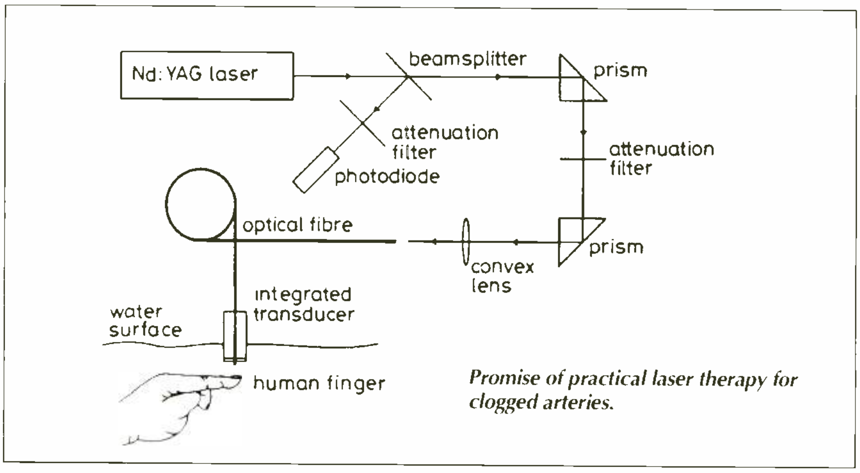
Laser/sound probe will declog your tubes...

Development by a UK team of a miniaturised probe that makes use of a laser's ability to cut as well as its ultrasonic characteristics could transform laser surgery of clogged arteries from the possible – into the practical.

Clogged arteries (atherosclerosis) are among the main causes of strokes and heart attacks. What happens is that a lining of cholesterol and similar fatty materials builds up in the form of plaques on the arterial walls until the blood supply is blocked or dangerously restricted. Doctors have long been trying to treat such blockages with drugs, by mechanically scraping away the cholesterol, by balloon angioplasty (stretching the artery walls) and by bypass surgery. More recently it has been shown that atherosclerotic plaques can be blasted away with pulses of powerful laser light.

But though enough laser energy can be fed along a fibre-optic catheter into some of the bigger blood vessels, laser ablation is not an-easy technique. It is made particularly difficult by the fact that, while x-rays can be used to guide a catheter, they will not show up the soft walls of the vessels.

Most therapeutic systems incorporate a second catheter, carrying an ultrasound probe to provide pictures on a screen for the surgeon to study. The only problem is that not many blood vessels are big enough to take two catheters at once, especially if they are already half blocked.



Promise of practical laser therapy for clogged arteries.

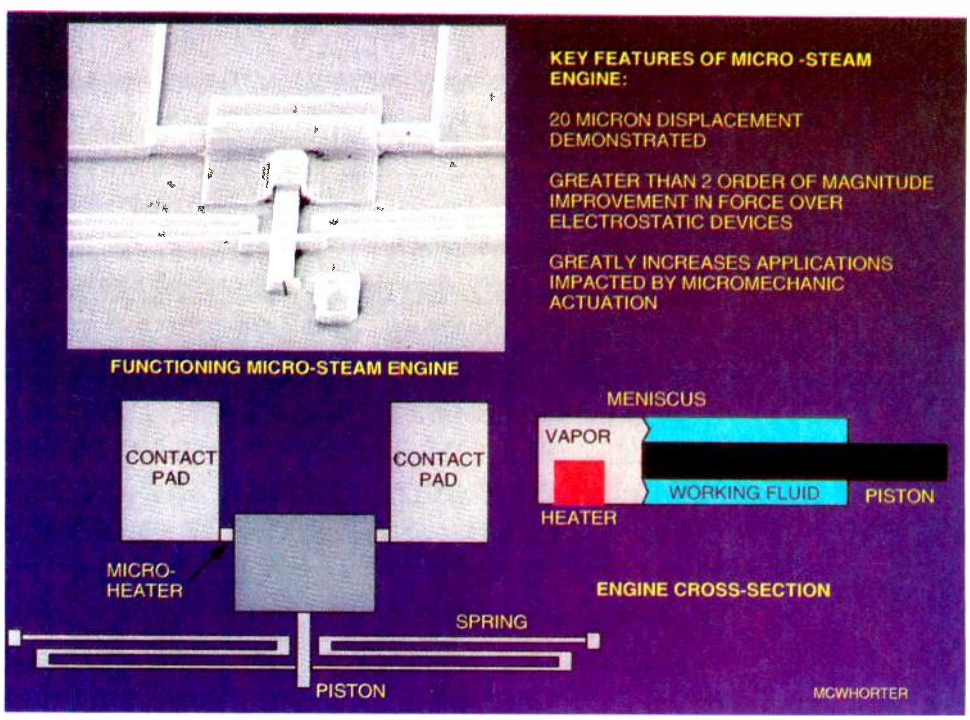
A new approach to this problem has been described (*Electronics Letters*, Vol 29, No 18) by a team of researchers at Umist and the Killingworth Hospital in Leeds. They have developed an experimental system that should eventually make it possible, using a single catheter, to image the body tissue at the same time as treating it with laser ablation.

The single-catheter probe makes use of the fact that laser light can induce its own ultrasonic vibrations when it hits a target. The team showed that usable ultrasonic signals could be generated in an experimental human finger using laser pulses with an energy of around 3mJ. This (thankfully for the volunteer) is enough to produce good images, but not enough to do any damage. In the experimental set-up, the energy was delivered along exactly the same 600/μm core fibre that is used at higher powers for ablation treatment. In their experiments, the team successfully picked up ultrasound echoes using a 3mm diameter polymer transducer fitted around the tip of the optical fibre. They say that further miniaturisation should lead to a whole range of medical applications apart, that is, from combining intra-arterial imaging with laser ablative therapy.

...or simply steam clean them

Researchers at Sandia National Laboratories in Albuquerque, New Mexico, have developed a steam engine smaller than a pinhead. The special motor is designed to power the growing number of micromechanical devices found in everything from weapons to medical equipment. Engineers have been able to machine tiny gear wheels, axles and ratchets no bigger than a few microns across, for some time. Manufacturing techniques are borrowed from the world of chip fabrication, where etching of components this size is routine. But the main problem with micromechanical devices has been to find a suitable micro-motor to power them. You can scale down a gear wheel to micron dimensions, but not a diesel engine or even a conventional electric motor or actuator: there are simply too many parts.

Micro-mechanical engineers machines have been forced to make do with



electrostatic micro-actuators, limited by small electrostatic forces and rarely having enough power to do much useful work.

Enter the micro steam engine, a motor that works on exactly the same principle as its larger cousins, except that it does it all inside a polysilicon cylinder a mere 2μm in diameter. Steam formed at one end of the cylinder when a micro-drop of water is heated by a hot filament, moves the tiny piston in proportion to the current supplied. A folding spring, attached to the piston, then returns it to its original position when the current is switched off.

Scaling the steam engine down to micron size has presented fewer problems than might be expected. Surface tension, which is often a bugbear in the use of fluids, has actually been exploited by the Sandia researchers in a way not possible on the macro scale. In the micro-cylinder it provides a perfect elastic membrane on the surface of the liquid drop.

Each stroke of the micro steam engine is a only 20μm in length. But unlike electrostatic micro-motors, it develops enough power to do a lot of useful work – such as performing surgery inside an artery.

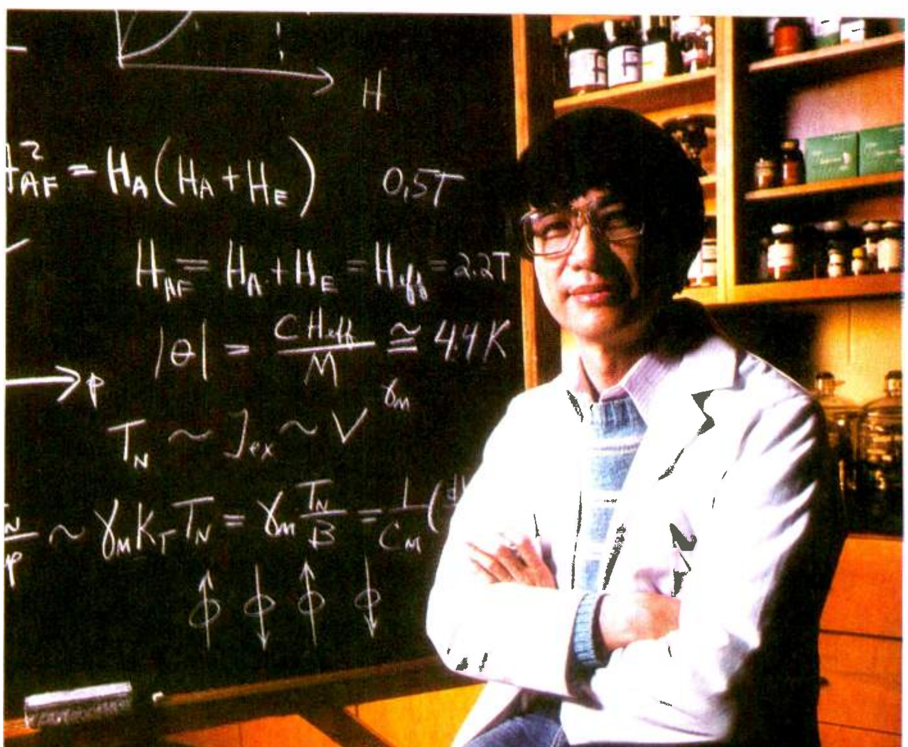
James Watt would have loved it.

Superconducting barrier starts to melt

High temperature superconductivity is back in the news with an announcement that scientists may be on the brink of ambient pressure superconducting at over 150K.

The excitement has be been created by Paul Chu and associates of the Texas Center for Superconductivity at the University of Houston (*Nature*, Vol 365, No 6444). If their results are anything to go by, it looks as if we are set for another sharp rise in T_c, the critical temperature at which ceramic copper oxide materials lose all their resistance. These high-temperature (in superconducting terms) superconductors are significant because the temperatures at which they work can be cheaply and easily achieved using liquid nitrogen. Admittedly, many technical problems still remain in utilising superconducting ceramics industrially, but they nevertheless hold out exciting prospects, especially if superconductivity can be achieved at room temperature.

At the beginning of this year, Chu's research group – and others in Russia, Japan and Switzerland – had painstakingly produced materials that would superconduct at 135 degrees above absolute zero. These layer compounds contained mercury in addition to barium, copper and oxygen and were a triumph of laboratory cookery.



Theory, for the most part, lagged behind patient empiricism.

Paul Chu's latest step forward (or upward) is the result both of meticulous experimental technique and also a critical analysis of progress so far.

"We found that the structure of the mercury-containing compound is rather different from others. That gave us the hint that the application of pressure would raise the temperature substantially", he says.

Using a ceramic based on mercury, barium, calcium, copper and oxygen, Chu found that a T_c of 153K could be achieved at a pressure of 150kbar. This is the highest temperature at which any material has yet exhibited superconducting properties — though the theoretical underpinning is still rather sketchy. "Two things happen, says Chu. "One is that we reduce the inter-atomic distances. As a result, some of the electrical charges move through the copper/oxygen layer, the active component of the material, more easily. Therefore the critical temperature goes higher.

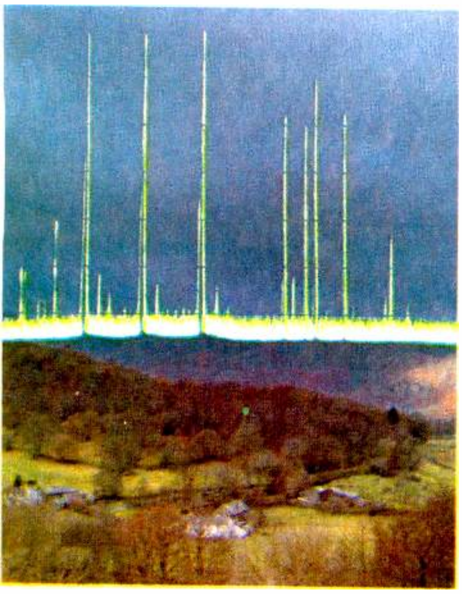
"In addition to that we've now found another factor. But the details of that are still unknown. We're still trying to find out."

That modest assessment of this pioneering work belies the real progress that has been made. Paul Chu and his colleagues have now assembled enough theoretical understanding to be able to predict the next step with confidence. Instead of using high pressures, they aim to make use of clever chemistry. As Chu observes: "High pressure brings atoms closer together, and there are chemical ways of doing the same thing. So by using chemical substitution, we hope to retain a high critical temperature at atmospheric pressure."

Early substitution attempts have so far not proved successful, mainly because attempts to tinker with the chemistry have disturbed the structure of the molecular lattice. But the team confidently expect to make a material that will become superconducting at 160K before very long.

Practical room-temperature superconductors are of course still a long way off, and even the existing high T_c ceramics are not without considerable manufacturing and operating problems. Physical brittleness and the loss of superconducting properties in the presence of strong magnetic fields are but two major obstacles. But if the history of this fascinating subject is anything to go by, there is bound to be more unexpected progress just when everyone is becoming complacent. Such is the nature of scientific discovery. ■

Research Notes is written by John Wilson of the BBC World Service.



ADD ON A SPECTRUM ANALYSER

Encounters with RF are much easier if a spectrum analyser is to hand. Although based on a commercial TV tuning head, Ian Hickman's design delivers linear, useful performance in its basic form and may be adapted to a much higher degree of sophistication including continuous coverage and wider frequency span.

An oscilloscope is undoubtedly the basic tool of the trade in general electronic design and development work. For investigating rf equipment, an instrument of sufficient bandwidth is a help and certainly much better than nothing.

A standard spectrum analyser is expensive; even a second hand model will cost the best part of £2000. An add-on box to the ubiquitous oscilloscope provides a much cheaper alternative. The design shown here is capable of further development in several directions, so this article should be regarded as a starting point.

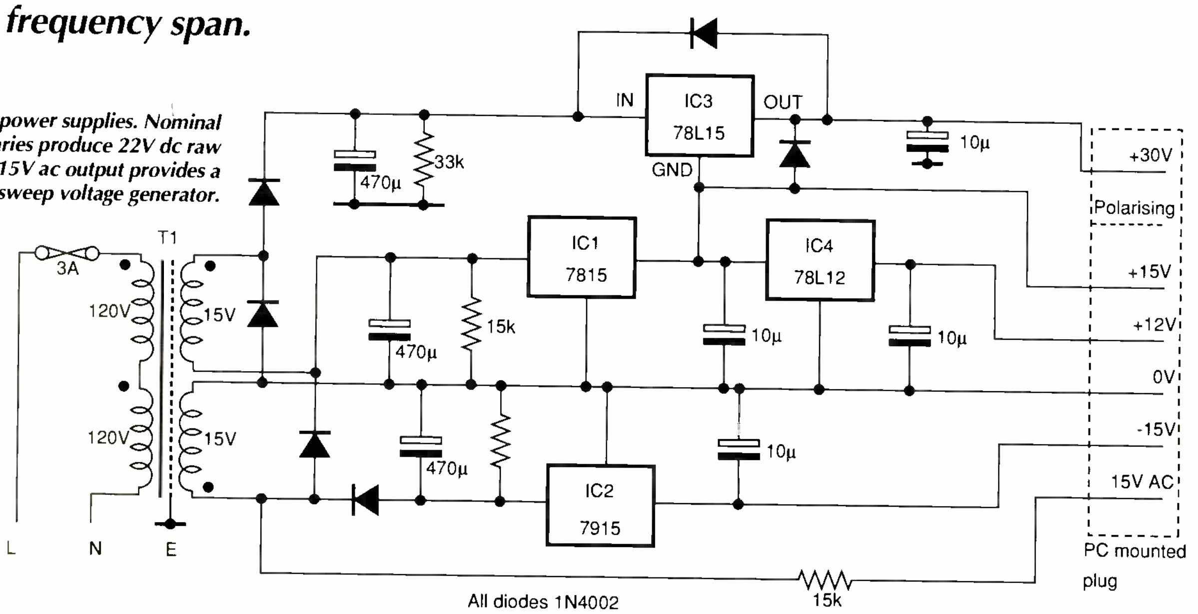
As it stands, it has its limitations so I think of it more as a spectrum monitor rather than a spectrum analyser. Nevertheless, it has already proved itself useful and would be even more so with suggested further development.

The spectrum monitor is built around a TV tuner, the particular one used here is a beautifully crafted all surface-mount example, the Toshiba *EG522F*. Possible suppliers of this unit are given in Ref. 1.

The *EG522F* provides continuous coverage from the bottom of Band I to the top of Band III in two ranges, a third range covering Bands IV/V. There is a gap between the top of Band III and the bottom of Band IV; the continuous coverage tuner mentioned in Ref. 2 is apparently no longer available. The design of this spectrum monitor is generally applicable to most types of TV tuner and any necessary circuit modifications should be straightforward.

It was desired to give the finished unit as much as possible of the feel of a classic spectrum analyser rather than the current generation of push-button controlled instruments. The design challenge was to leave the way open for further development if required. To

Fig. 1. Stabilized power supplies. Nominal 15V secondaries produce 22V dc raw supplies. The 15V ac output provides a timebase for the sweep voltage generator.



this end, within its case the monitor was constructed as three separate units – PSUs, sweep generator, RF/IF unit – interconnected by ribbon cables.

Power rails are ±15V for general analog circuitry, +12V for the tuner and +30V for its tuning varactor supply, **Fig. 1**, terminating in a 7-pin plug accepting a mating ribbon-cable-mounted socket (RS "inter PCB crimp" style).

Sweep circuitry

The sweep circuitry to drive the tuner's varactor tuning input is shown in basic form in **Fig. 2a**. This produces a sawtooth waveform of adjustable amplitude and fixed duration symmetrically disposed about ground. This means that as the span (the tuning range covered by the monitor) is increased or decreased (the dispersion is decreased or increased), a signal at or near the centre of the display becomes contracted or expanded width-wise but remains on-screen. This is a great convenience in use.

Operation is as follows. On negative excursions of the clock drive, Tr_2 is off and Tr_1 clamps the capacitor C_1 and the NI input of A_2 to the voltage at the output of A_1, Vclamp: the output therefore also sits at V_{clamp}, the voltage at the wiper of R_2. A_2 forms a Howland current pump, so that when Tr_2 is turned on, removing the clamp, a negative charging current V_{clamp}/R_5 is applied to the capacitor. As A_2 must act to maintain voltage equality between its inputs, a linear negative going ramp results. If C_1 is selected correctly relative to the clock frequency, the voltage across it will just reach $-V_{clamp}$ during each positive excursion of the clock, Fig. **2b**.

For convenience, the clock frequency is derived from the mains, giving a choice of sweep durations. The sweep amplitude can be set to any value from zero to maximum, the sweep remaining ground centred as illustrated in Fig. **2c**, where R_2 was used to advance V_{clamp} steadily from ground to its maximum value, over a number of sweeps.

Fig. 3 shows the full circuit of the sweep circuitry which operates as follows. The 15V ac from the psu is sliced by Tr_1 (Fig. **3a**) and fed to a hex inverter to sharpen up the edges. R_8 and R_9 around the first two inverters provide some hysteresis – without this, noise on the mains waveform will simply be squared up and fed to the counters as glitches causing miscounting. The output of the inverters is a clean 50Hz squarewave and appears at position 1 of switch S_{1B}. The half period is 10ms, this setting the shortest sweep duration. A string of four *74LS90* decade counters provide alternative sweep durations up to 100 seconds.

The selected squarewave from S_{1B} is level shifted by Tr_2 and Tr_3 to give a control waveform swinging (potentially) over ±15V, although the positive excursion only reaches V_{clamp}. This waveform is routed to control the fet in the sweep circuit, line 1. A_2 and A_1 provide currents via R_5 and R_6 which are fed to a summing amplifier to provide the main and fine tuning controls, line 2. R_4 is adjusted to make the full range of the centre frequency set control R_1 just cover the required 30V varactor tuning range of the TV tuner.

Lines 1 and 2 are connected as shown in Fig. **3b**, line 1 operating the clamp transistor Tr_4. Being a jfet, the gate turns on at 0.6V above V_{clamp}, so line 1 never in fact reaches +15V. The sweep generator operates as in Fig. 2a, with one or two additions. S_{1A} selects a size of capacitor appropriate to the sweep duration, two of the capacitors being re-used by altering the charging current by a factor of 100 via S_{1C}. (Note that for a linear sweep, it is sufficient to ensure that the ratio of R_{19} to R_{21} is the same as the ratio of the two resistors connected to the non-inverting input of A_3, the actual values can be whatever is convenient.)

R_{17} is adjusted so that the ramp output from A_3 swings equally positive and negative about earth. S_2 selects the span from full span for the selected band of operation of the TV tuner, via decade steps down to zero span, where the

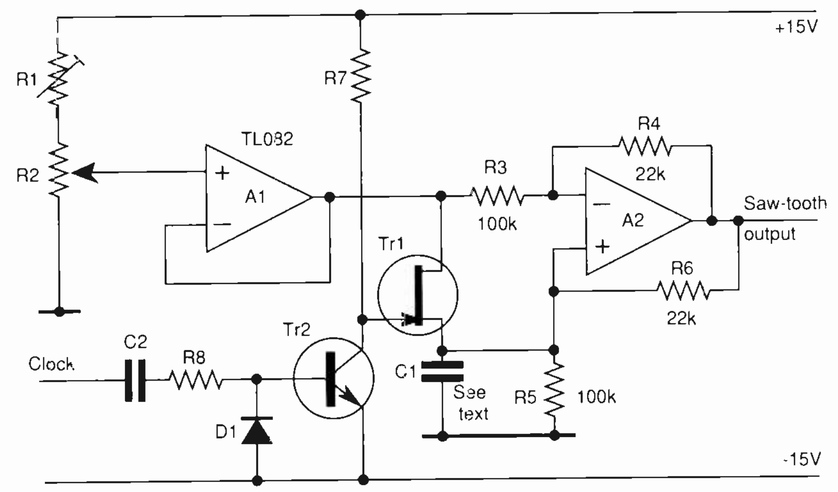
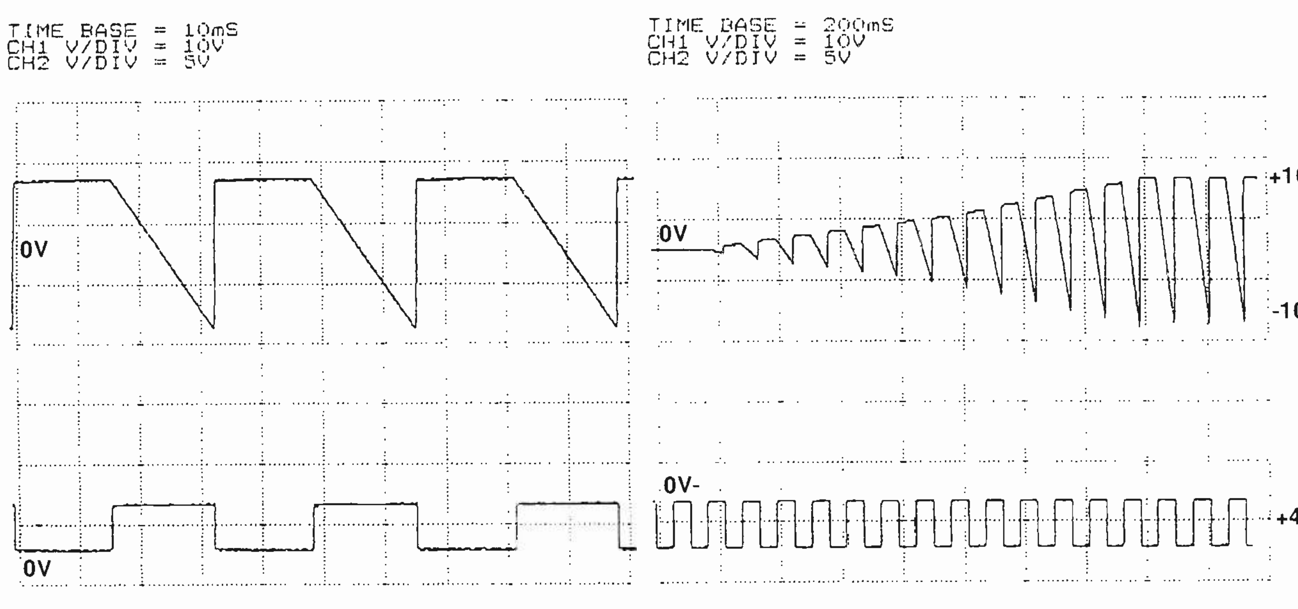


Fig. 2a. Basic circuit of the tuning sweep generator, employing a Howland current pump (A2 and associated resistors).

Fig. 2b. Output waveform shown in relation to the controlling clock waveform. c. Advancing R2 from ground to maximum increases the sweep width whilst remaining ground-centred.



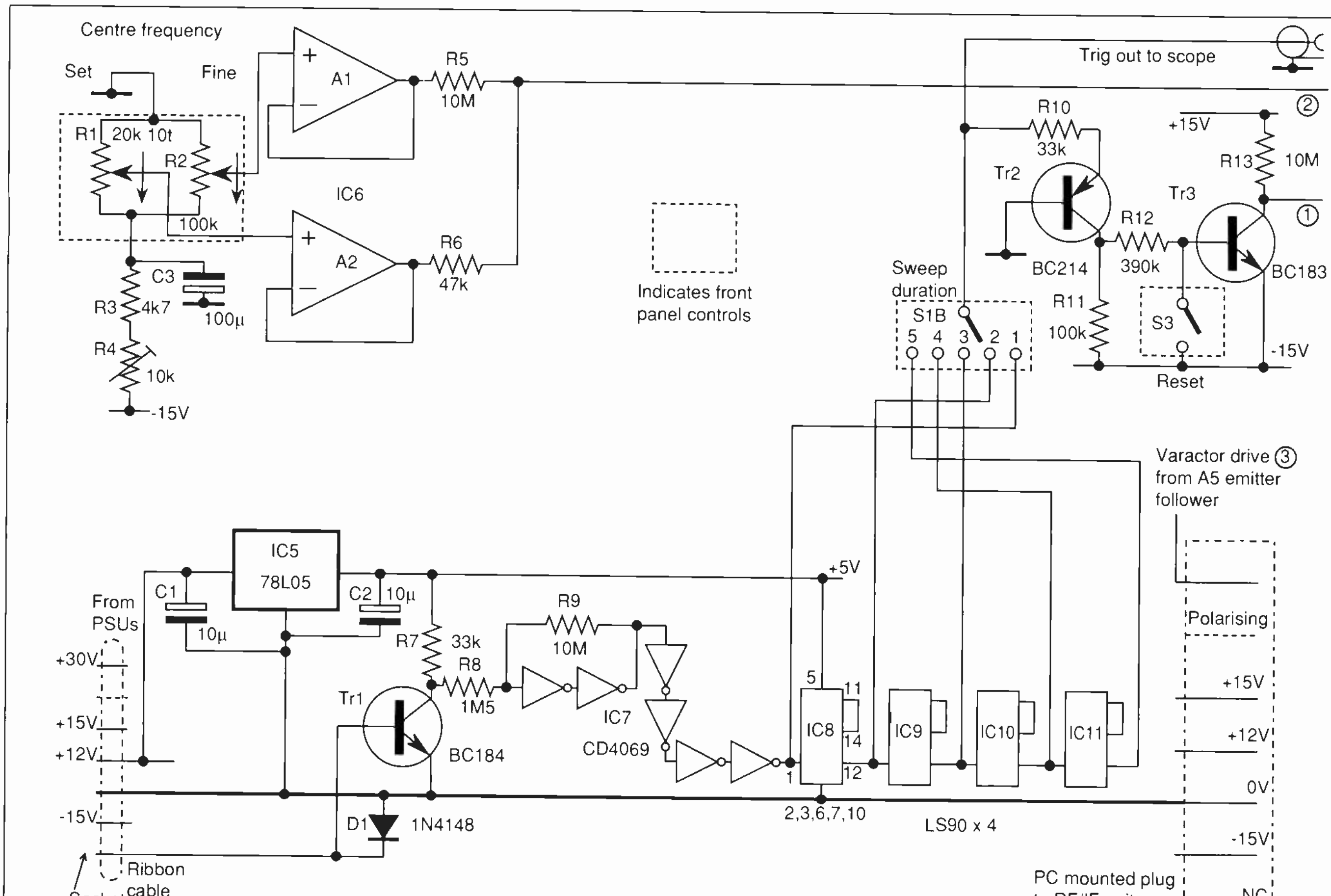


Fig. 3a. Sweep duration generator and centre frequency setting circuits.

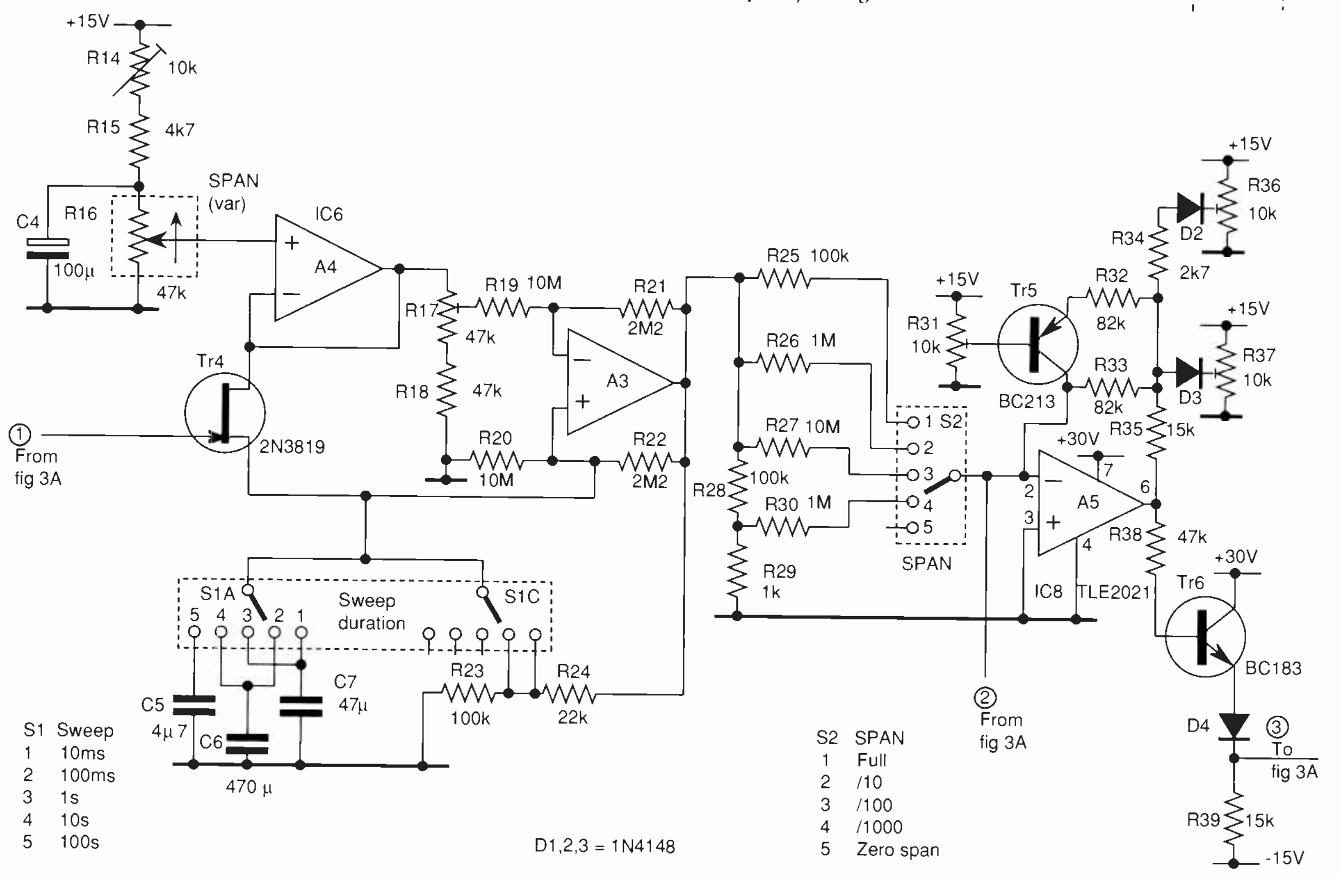


Fig. 3b. Sweep generator, sweep/centre-frequency summer and sweep shaping circuits.

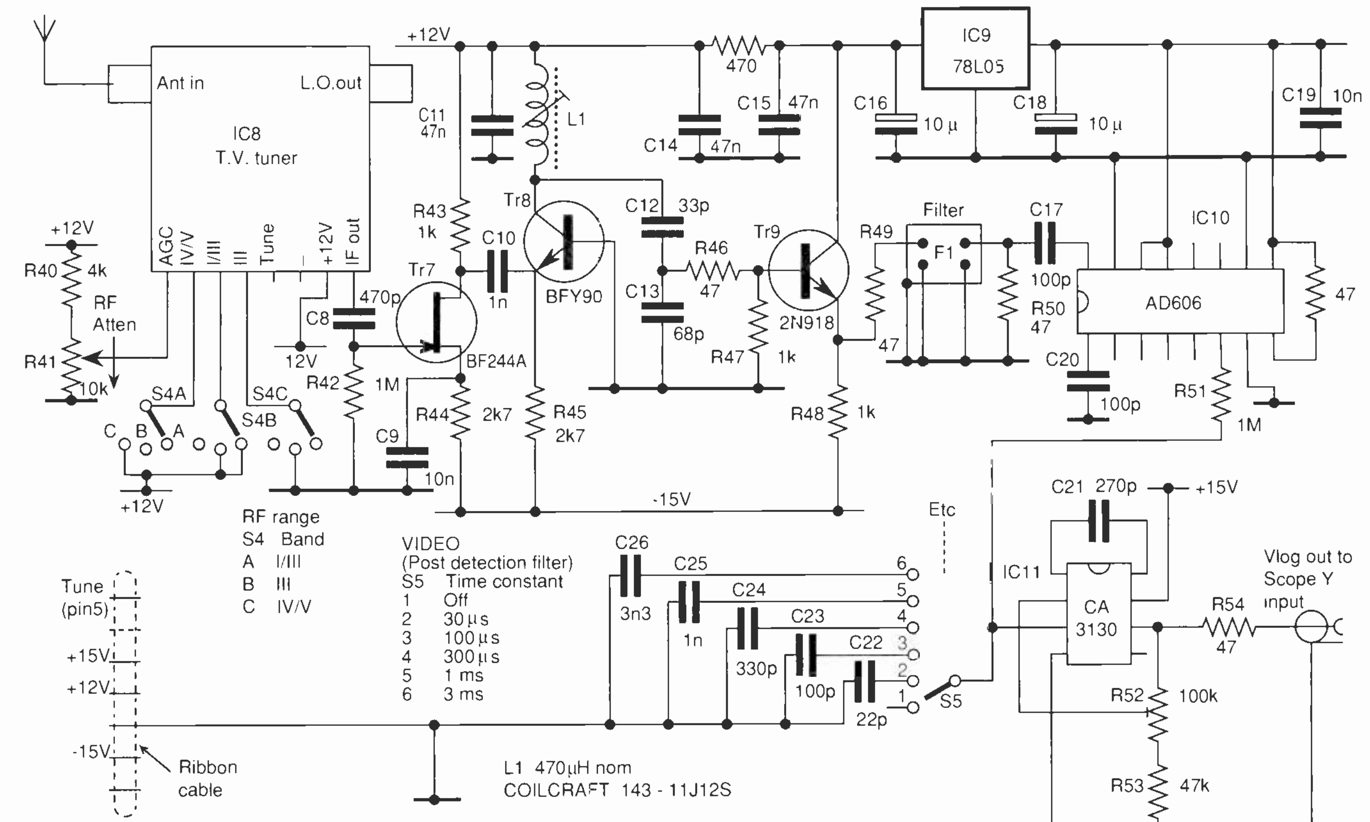


Fig. 4. Circuit diagram of the RF/IF unit. This is built around a Toshiba EG522F TV tuner, though almost any other model covering Bands I to V inclusive could be used.

tuner operates unswept at the spot frequency selected with centre frequency controls R_1 and R_2. R_{16} provides a continuously variable control between the settings given by S_2. R_{14} enables the full span, with var at max, to be set just to swing over the 0 to 30V tuning range of the tuner when centre frequency R_1 is set appropriately. If centre frequency is set to minimum or maximum, only the upper or lower half of the span will be displayed, at the left or right side of the oscilloscope trace respectively.

Inverting amplifier A_5 sums the negative-going sweep waveform and the negative tuning input from R_1 and R_2, to provide a positive-going voltage between 0 and +30V. It also provides waveform shaping, the reason for which is discussed later. The shaped sweep output from A_5 is level shifted by Tr_6 and D_4 before passing to the TV tuner varactor tuning input since it is important that the sweep should start right from zero volts if the bottom few MHz of Band I are to be covered.

All of the front panel controls shown in Fig. 3 (except the reset control, of which more later) were mounted on a sub-panel behind the main panel and connected to the sweep circuit board – mounted on the same sub-panel – via ribbon cable, making a self contained sub-unit.

RF section

Fig. 4 shows the RF/IF unit, which is powered via a ribbon cable from the sweep circuit board. The gain of the TV tuner IC_8 can be varied by means of R_{41}, which thus substitutes for the input attenuator of a conventional spectrum analyser. Compared to the latter, this spectrum monitor has the advantage of a tuned front end, as against a wideband direct-to-mixer architecture.

The front end tuning helps to minimize spurious responses – always a problem with any receiver, including spectrum analysers. The IF output of the tuner, covering approximately 34 – 40MHz, is applied via a fet buffer to grounded base amplifier Tr_8. This provides IF gain and some selectivity, its output being buffered by emitter follower Tr_9 and applied to the main IF filter F_1, of which more will be said later. The output of the filter is applied to a true successive detection logarithmic IF amplifier[3].

The required well decoupled +5V supply is produced locally by IC_9. The log amp output V_{log} is applied to an output buffer op-amp IC_{11} via a simple single-pole switchable video (post detection) filter, which is useful in reducing grass on the baseline when using a high dispersion (very narrow span) and a suitably slow sweep speed.

Filter time-constants up to one second were fitted in the instrument illustrated, but such large values will only be useful with wide dispersions at the slowest sweep speeds. The buffered V_{log} is applied to the Y input of the display used, typically an oscilloscope. R_{52} permits the scaling of the output to be adjusted to give a 10dB/division display.

Special considerations

The frequency vs tuning voltage law of the TV tuner is not linear, being simply whatever the L.O. varactor characteristic produces. Just how non-linear is clearly shown in **Fig. 5a** which shows both the linear tuning ramp and the output V_{log} from the IF strip, showing harmonics of a 10MHz pulse generator at 50, 60 through to 110MHz plus a 115MHz marker (span range switch S_2 being at full span and span variable control R_{16} fully clockwise). Also visible are the responses to the signals during the retrace, these being telescoped and delayed.

The frequency coverage is squashed up in the middle and unduly spread out towards the end with a yawning gap between 110 and 115MHz. The result of some simple linearisation is shown in Fig. 5b. As the ramp reaches about 10V, Tr5 turns on, adding a second feedback resistor R_{32} in parallel with R_{33}, halving the gain of A_5 and slowing the ramp down so as decompress the frequency coverage in the region of 70 to 100MHz, maintaining a 10MHz/division display.

Just before 100MHz, D_2 turns on, shunting some of the feedback current via R_{35} away from the input and thus speeding the ramp up again, whilst another more vicious breakpoint, due to D_3 at around 110MHz, speeds the ramp on its way to 30V, correctly locating the 115MHz marker just half a division away from the 110MHz harmonic.

The linearisation has been optimised for operation on Band A (bands I and II) and holds quite well on B (band III) with the particular tuner used. Ideally other shaping stages similar to A_5 would be employed for band III and band IV/V.

Note that whilst the linearisation shown in Figs 4 and 5 has produced an approximately constant 10MHz/division display on full span,

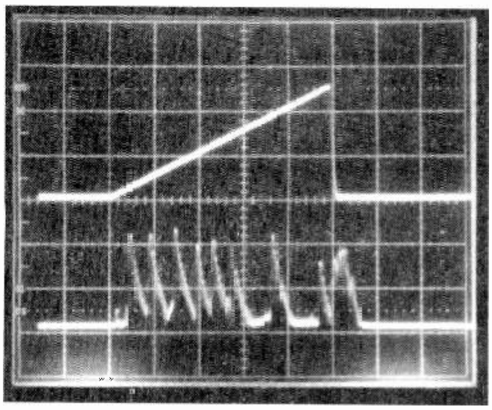


Fig. 5a. Upper trace, channel 1: the sweep output at cathode of D4 before the addition of linearising circuitry, 2ms/div. horizontal; 10V/div. vertical. Lower trace, channel 2: output Vlog from IF strip showing harmonics of a 10MHz pulse generator at 50, 60, etc to 110MHz plus a 115MHz marker. Sweep time 10ms.

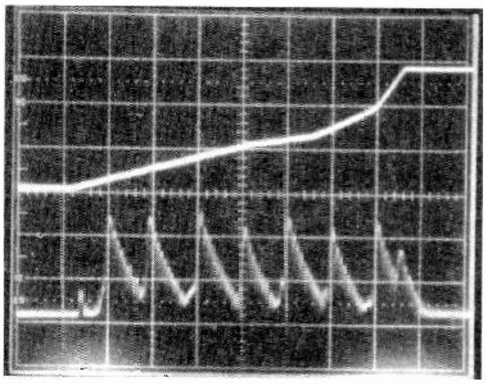


Fig. 5b. Upper trace: the ramp after shaping to linearise the frequency coverage, 1ms/div. horizontal; 10V/div. vertical.
Lower trace: as 5a. Note, as the ramp now reaches +30V in less than the 10ms nominal sweep time, the responses during the retrace are off-screen to the right.

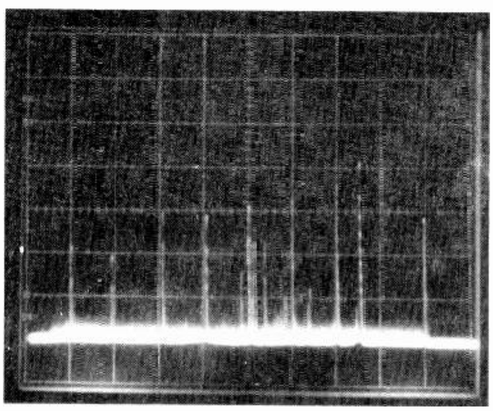


Fig. 5c. Channel 2 only: as 5b except sweep time 100ms. Many FM stations now visible in the range 88 – 104MHz.

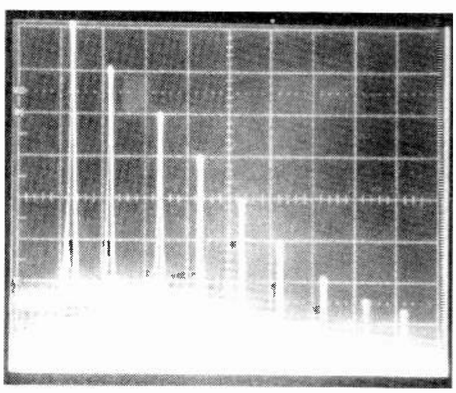


Fig. 5d. 80MHz CW signal reducing in six steps of 10dB plus two further steps of 5dB. Indicating excellent log-conformity over a 65dB range. SWEEP 100ms, SPAN 300kHz/div, VIDEO FILTER, 100us. (For clarity, the spectrum monitor fine tuning control was used to offset the display of the signal one division to the right at each step in this multiple exposure photo.)

for reduced spans S_2 attenuates the sawtooth *before* it is conveyed to the shaping stage. Consequently, for reduced spans the actual span/div depends upon the setting of the centre frequency control, although the portion of the full band displayed will be approximately linear, except where it happens to lie across one of the break points.

The filter used in the spectrum monitor illustrated is a 35.4MHz 6-pole crystal unit designed for 20kHz channel spacing applications. This was used as it was to hand just waiting for a suitable application. However, it is not ideal, having a basically square passband shape approximating the proverbial brick wall filter.

This is not a great inconvenience in practice: it simply means that a slower sweep speed than would suffice with an optimum Gaussian filter must be used. Even with a Gaussian filter, the combination of large span and fast sweep speed used in Fig. **5a** and **5b** would have been quite excessive – it was used as the stretching of the responses makes the effect of linearisation more easily visible.

Fig. **5c** shows the same Band A (43 to 118MHz) display using the nominal 100ms sweep. FM stations in the range 88 to 104MHz are clearly visible, no longer being lost in the tails of other responses.

Although the particular crystal filter used is no longer available, a number of alternatives present themselves. A not too dissimilar filter with a centre frequency of 34.368MHz is available from Ref. 4. Its 20kHz 3dB bandwidth (compared with 9.5kHz for the filter used in the prototype) would permit faster sweep speeds or wider spans to be used but, being only a 4-pole type, its ultimate attenuation is rather less and the one-off price may make it unattractive.

A choice of no less than five crystal filters in the range 35.0 to 35.9MHz is available from Ref. 5, with bandwidths ranging from 8kHz at –6dB (type *XF-354S02*) to 125kHz at –3dB (type *XF-350S02*, a linear phase type). A simple alternative would be to use synchronously tuned LC filters[2] though at least twice as many tuned stages should be employed in order to take advantage of the greatly increased on-screen dynamic range offered by the log-amp in the design featured here, compared to the linear scale used in Ref. 2.

The excellent dynamic range of the spectrum monitor is illustrated in the multiple exposure photo Fig. **5d**, which shows an 80MHz CW signal applied to the monitor via a 0 to 99.9dB step attenuator. The signal generator output frequency and level were left constant and a minimum of 20dB attenuation was employed, to buffer the monitor input from the signal generator output. The attenuation was increased by 60dB in 10dB steps and then by two further steps of 5dB, the display of the signal being offset to the right using the centre frequency controls at each step. Fig. 5d shows the excellent log-conformity of the display over a 65dB range, the error increasing to 3dB at -70dB relative to top-of-screen reference level. It also shows the inadequate 63dB ultimate attenuation of the crystal filter used, with the much wider LC stage taking over below that level.

An alternative to crystal or LC filters is to use saw filters, a suitable type being Murata *SAF39.2MB50P*. This is a low impedance 39.2MHz type designed for TV/VCR sound IF, some additional gain being necessary to allow for its 17dB typical insertion loss. Two of these filters[6] would provide an ultimate attenuation of around 80dB, enabling full use to be made of the subsequent log-amp's dynamic range. The 600kHz 6dB bandwidth of each filter would limit the discrimination of fine detail, but allow full span operation at the fastest sweep speed. They could then be backed up by switching in a narrower band filter as and when necessary.

Further development

A number of refinements which will occur to the reader could be incorporated in this spectrum monitor, to increase its capabilities and usefulness. One simple measure concerns the method of display. As my oscilloscope has sweep speed ranges in 1 - 2 - 5 sequence plus a variable control, the output from S_{1B} was simply used as a 'scope trigger. However, if R_{16} is set permanently at V_{clamp} and a further buffer op-amp added between A_3 and A_5 to implement the span(var) function, the fixed amplitude output from A_3 (suitably scaled and buffered) can be fed out to the display oscilloscope, set to dc coupled external X input, providing a sweep speed automatically coupled to the sweep speed control S_1.

At the slower sweep speeds, eg 1 or 10 seconds per sweep, a long persistence 'scope provides better viewing, whilst for the 100s sweep a digital storage 'scope or a simple storage adapter is very useful. However the slower sweep speeds are only necessary when using a narrow filter with a wide span.

If one of the slowest sweep speeds is in use, it can be very frustrating to realise just after the signal of interest appears on the screen, that one needed a different setting of this or that control, since there will be a long wait while the scan completes and then restarts. Pressing the reset button S_3 will reset the tuner sweep voltage to V_{clamp} to give another chance to see the signal, but without resetting either the sweep period selected by S_1 or the oscilloscope trace.

If one of the sections of the *4069* IC_7 is

Using the instrument

This spectrum monitor is rather like the earliest spectrum analysers; i.e. it is entirely up to the user to ensure that an appropriate IF bandwidth, video filter setting and sweep speed are used, suitable for the selected span. Failure to do so means that as the spectrum analyser sweeps past a signal, the latter will not remain within the filter bandwidth long enough for its full amplitude to be registered. This is important in a full-blown analyser, where the reference level (usually top of screen) is calibrated in absolute terms, e.g. 0dBm.

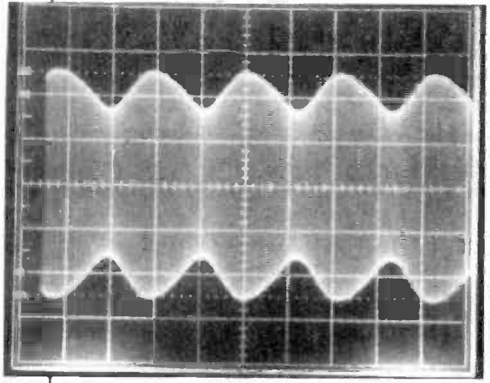


Fig. 6a. Oscilloscope display of the 100MHz output at maximum level from an inexpensive signal generator, with the fixed level internal 1kHz AM applied. Oscilloscope set to 100mV/div vertical, 500µs/div horizontal.

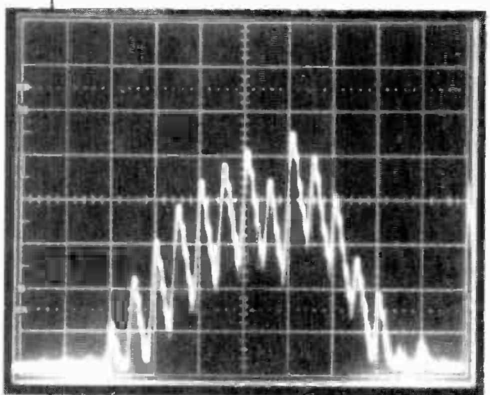


Fig. 6b. Display using the spectrum monitor of the same output but using 50kHz external modulation, set for the same modulation depth. SPAN 100kHz/div, vertical 10dB/div, 10ms SWEEP speed.

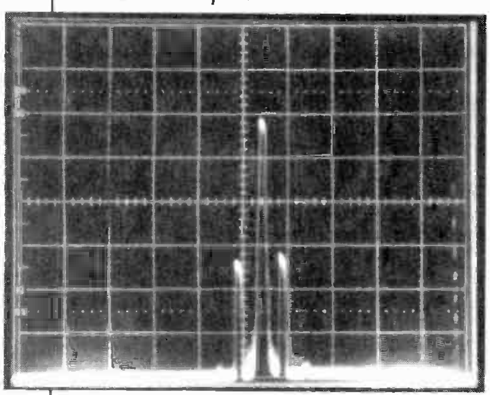


Fig. 6c. As 6b, but external modulation input reduced by 30dB, displayed 100ms SWEEP.

Fig. 6a shows the 100MHz output from an inexpensive signal generator with the internal 1kHz amplitude modulation switched on. The modulation is basically sinusoidal, though some low order distortion is clearly present. 50kHz external sinusoidal modulation was applied in place of the internal modulation, adjusted for the same modulation depth.

Fig. 6b shows the output, this time displayed via the spectrum monitor, at a dispersion of 100kHz/div. The large number of sidebands present, of slowly diminishing amplitude, are much more than could be explained by the small amount of AM envelope distortion, indicating a great deal of incidental FM on AM, a common occurrence in signal generators when, as here, the amplitude modulation is applied to the RF oscillator stage itself.

In Fig. **6c**, the amplitude of the applied 50kHz modulating waveform has been attenuated by 30dB, so the AM modulation depth is reduced from about 20% in Fig. 6a to 0.63%. This corresponds to AM sidebands of about 50dB down on carrier, whereas those in Fig. 6c are only around 30dB down. They are therefore almost entirely due to FM, the AM sidebands being responsible for the slight difference in level between the upper and lower FM sidebands. (While AM and first FM sidebands on one side of the carrier add, those on the other subtract.) Note that at the 10ms sweep used in Fig. 6b the sidebands are not completely resolved. For Fig. 6c, the 100ms sweep was selected, the 50kHz sidebands being resolved right down to the 60dB level.

Fig. 7a shows the spectrum monitor operating on Band C – covering bands IV and V. The span is just over 1MHz/div and shows a band IV tv signal showing (left to right) the vision carrier, the colour subcarrier, the sound carrier and immediately adjacent to it, the much broader band occupied by the nicam sound channel.

Fig. **7b** shows 4.8kb/s data applied to a VHF FM modulator, producing FSK with a ±40kHz shift. The signal is spread over a considerable band and clearly a receiver bandwidth in excess of 80kHz would be necessary to handle the signal. If a carrier is frequency modulated with a sinewave using a very large modulation index (peak deviation much larger than the modulating frequency), a rather similar picture results, except that the dip in the middle is much less pronounced and the sidebands fall away very rapidly at frequencies beyond the peak positive and negative deviation.

The spectrum shape approximates in fact the PSD (power spectral density) of the baseband sinewave. The PSD of a triangular wave is simply rectangular, and Fig. 7c shows triangular modulation applied to the inexpensive signal generator. At the carrier frequency of 100MHz, the AM modulation is in fact mainly FM and clearly closely approximates a rectangular distribution, the variation being no more than ±1dB over a bandwidth of 100kHz.

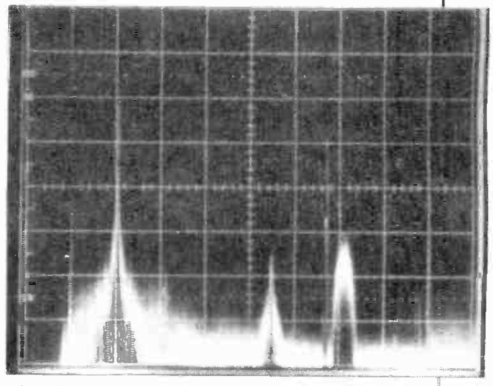


Fig. 7a. A band IV TV signal, showing (L to R) the vision carrier, colour sub-carrier, sound subcarrier and Nicam digital stereo signal.

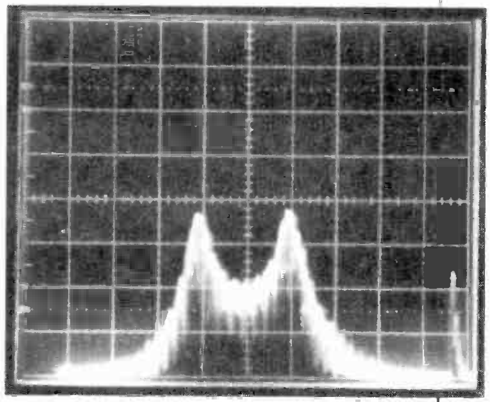


Fig. 7b. 4.8kb/s data FSK modulated onto a VHF carrier; 10dB/div vertical, 40kHz/div horizontal.

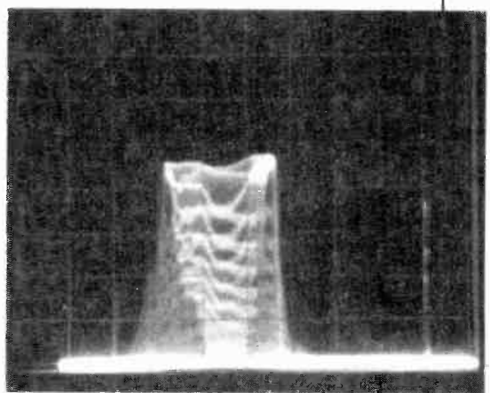


Fig. 7c. High modulation index FM produced by a triangular modulating waveform has a near rectangular envelope with a flat top and steep sides. Individual spectral lines are not visible in this 20s exposure as there was no relation between the modulating frequency and the sweep repetition period. The wavy lines are due to ringing on the tails of the filter response.

Such a signal is a useful excitation source for a testing a narrow band filter: the filter's characteristic can be displayed by applying its output to a spectrum analyser. This dodge is handy when, as with this spectrum monitor, there is no built-in tracking oscillator. A modulating frequency which bears no simple ratio to the repetition rate of the display sweep should be used, otherwise a series of spectral lines, stationary or slowly passing through the display, may result. This is due to a stroboscopic effect similar to the stationary or slowly rolling pattern of a Lissajous figure when the two frequencies are at or near a simple numerical relation.

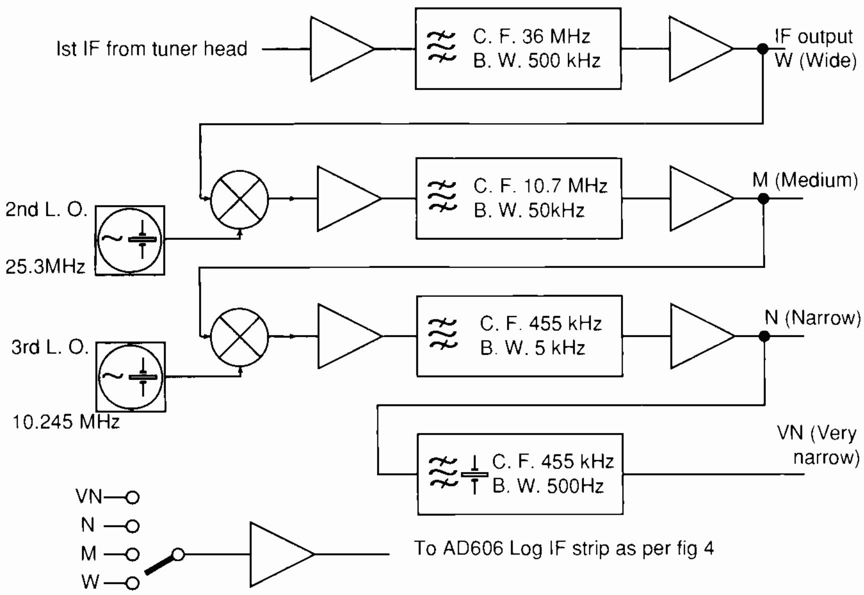


Fig. 8. Block diagram showing modified architecture, giving a choice of IF bandwidths. It is simpler to provide different signal paths for the different bandwidths rather than select the bandwidth by switching in one or other of several filters all operating at the same IF frequency.

priate tuning voltage from the DAC[7]. The use of multiplying DACs will provide linear interpolation between points, giving in effect a shaped varactor drive voltage waveform with *n* breakpoints per scan. With many breakpoints available, the change of slope at each will be very small, avoiding the harsh breaks visible in Fig. 5b. The two msbs of the prom could be used as select lines to call up a different law for each of the three bands.

Frequency readout

A true digital readout can be provided by counting the frequency of the LO output from the TV tuner, prescaled by a divide-by-100 circuit[8] to a more convenient frequency. Using the positive half cycle of the 5Hz squarewave at pin 12 of IC_8 provides a 100ms gate time which, in conjunction with the divide-by-100 prescaler, gives a 1kHz resolution. The positive-going edge can be used to jam a count equal to the IF frequency into a string of reversible counters, set to count down, the appearance of the borrow output switching a flip-flop to set the counters to UP count for the rest of the gate period.

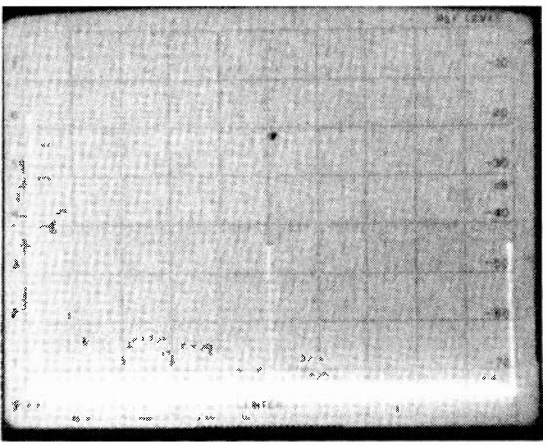


Fig. 9a. The L.O. output of the EG522F tuner at 490MHz, showing also the 2nd and 3rd harmonics. Span 100MHz/div, vertical 10dB/div, ref. level (top of screen) 0dBm.

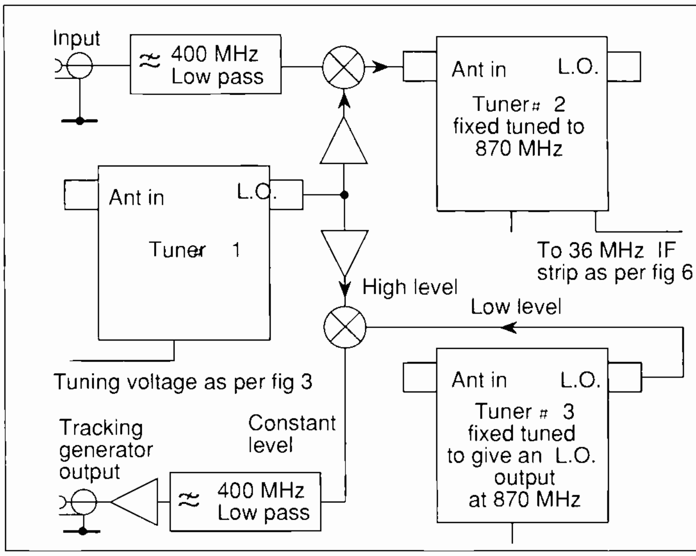


Fig. 9b. Block diagram of a spectrum monitor based on TV tuners, providing continuous coverage from below 1MHz up to approx. 400MHz.

redeployed to a position between S_{1B} and R_{10}, the sweep will occur during the *negative* half of the squarewave selected by S_{1B} (see Fig. 2b). A second pole of S_3 can then be used to reset IC_{8-11} to all logic zeros, avoiding a long wait during the unused 50% of the selected squarewave output from S_{1B} before the trace restarts – assuming the display 'scope is in the external X input mode, rather than using triggered internal timebase.

Working with a single IF bandwidth has its drawbacks. Switching filters is a messy business however it is achieved. **Fig. 8** shows an economical scheme using inexpensive stock filters.

Wide bandwidth LC or saw filters operating somewhere in the range 35 to 39MHz are used for the first IF permitting full span on each band to be examined without resort to very slow sweep speeds. A second conversion to 10.7MHz enables stock 50kHz filters to be used as an intermediate bandwidth, while a third conversion to 455kHz provides a choice of filters with bandwidths of 5kHz or less.

As **Fig. 8** indicates, no filter switching is involved: the desired output is simply selected and fed to the log IF strip, which can operate quite happily at each of these frequencies. The net gain of the second and third IFs is fixed at unity, so that switching bandwidths does not alter the height of the displayed response – provided of course that the span and sweep speed are not excessive.Another improvement would be better linearisation of the frequency axis avoiding sharp breakpoints, with the provision of shaping appropriate to each band. The easiest way to achieve this is probably to store *n* values in prom, *n* being a power of two, and read these out successively to DAC. The *n* values would correspond to equal increments along the frequency axis, each value being what was required to provide the appro-

The negative-going edge can reset the flip-flop and latch the count; for economy the negative half period could simply enable a seven segment decoder/display driven direct from the counters if you don't mind a flashing display.

If span is set to zero, the tuned frequency is indicated exactly. If span is set to one thousandth or even one hundredth of full span, the frequency will correspond to the centre of the screen, being of course the average frequency over the duration of the scan. In principle, the same applies up to full span, if the linearisation is good.

A simpler scheme for frequency readout uses a digital voltmeter. The output of A_2, besides feeding A_5, is also fed to a summing amplifier with pre-settable gain which combines it with a pre-settable offset. This is arranged (for example, on band A) so that with R_1 at zero, its output is 430mV and with

R_1 at maximum its output is 1.18V. This is fed to the DVM on the 2.000V range, providing a readout of 100kHz/mV. Similar scaling arrangements can be employed for the other bands, the accuracy of the resulting readout depending upon the accuracy of the linearisation employed.

This arrangement ignores the effect of centre frequency fine control R_2 which can, if desired, be taken into account as follows. The outputs of A_1 and A_2 are combined in a unity gain non-inverting summing amplifier, the output of which is fed via a 47K resistor to A_5 as now, and also to the scaling-cum-offset amplifier.

However, the simplest frequency calibration scheme of all, unlike the counters and displays, requires no additional kit whatever and unlike the DVM scheme, is totally independent of the exactness of linearisation. It is simply to calibrate, for each of the three bands, the centre screen frequency against the reading of the digital dial of the ten turn set centre frequency control R_1. Calibration charts are as effective as they are cheap, and in the present application they can also be very accurate, since all of the instrument's supplies are stabilised.

Continuous coverage

My final word concerns the missing coverage between the top of band III and the bottom of band IV, whilst also adding coverage from zero Hz up to the bottom of band I.

Many tuners now available will probably, like the Toshiba EG522F, have an LO output available. **Fig. 9a** shows the LO output from the tuner when tuned near the bottom of Band IV/V. The level of the 490MHz fundamental is −18dBm and the second and third harmonics are both well over 25dB down. The output over the rest of the band is well in excess of −18dBm. Using broadband amplifiers to boost the tuner's LO output to say +7dBm, it can then be applied as the mixer drive to a commercial double-balanced mixer, the signal input being applied to the mixer's signal port via a 400MHz low pass filter.

This tuner is used purely as a local oscillator, with the mixer's output being applied to the signal input of a *second* tv tuner fixed tuned to 870MHz, Fig. **9b**. The second tuner thus becomes the first IF of an up-converting 0-400MHz spectrum analyser, its output being fed to a 35MHz second IF strip as in Fig. 4.

This arrangement provides continuous coverage from 0Hz almost up to the top end of the 225 – 400MHz aviation band in one sweep, so only one set of sweep linearisation is necessary.

A most useful feature in a spectrum analyser, not always found even in professional models, is a tracking generator. This provides a constant amplitude CW test signal to which the analyser is always on tune. Fig. 9b also shows how for the paltry cost of yet another tuner and mixer, such a facility can be engineered. Used in conjunction with a reflection coefficient bridge, it turns a spectrum analyser into a rudimentary scalar network analyser. ■

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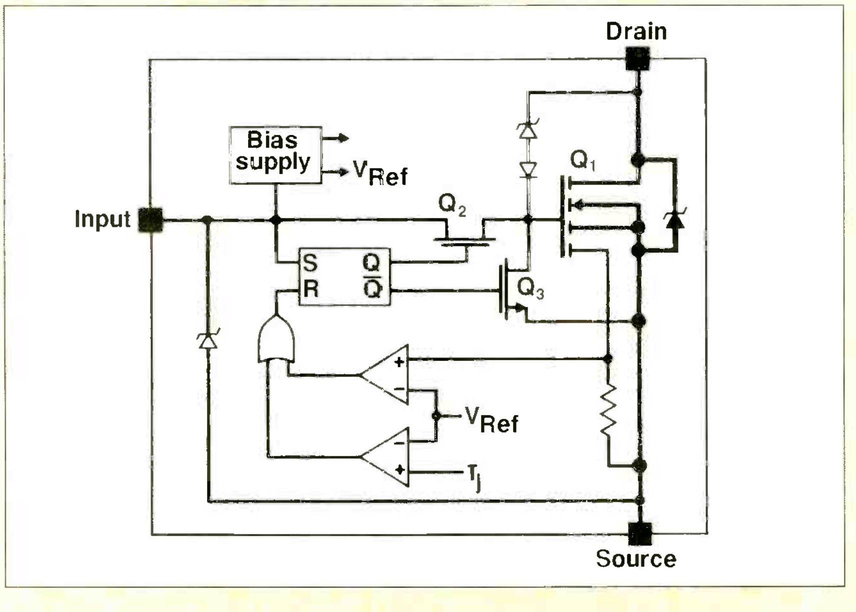
"Smart power" is generally taken to mean the inclusion of control and protection facilities into a discrete power transistor package. Most devices with this tag offer only limited protection through their integral thermal and overvoltage protection circuitry. International Rectifier has produced a mosfet which is so smart as to be virtually unburstable, yet cheap enough to replace standard mosfets in most applications. By Frank Ogden.

Smart enough to avoid destruction?

IRSF 3010

V_{ds}	50V
$R_{ds(on)}$	0.08Ω
I_{ds}	11A
$T_{junction}$	155°C
E_{AS}	44mJ



The ideal power mosfet would include decisive thermal shutdown with excess junction temperature, an overcurrent sensing mechanism which doesn't adversely affect on-resistance and a fast overvoltage clamp which dissipates spike energy in the main transistor channel. If device protection can be provided in a standard three-terminal package, so much the better. There are transistors on the market which have some these characteristics. The IRSF3010 has all of them – plus full ESD protection.

The device behaves like the n-channel 11A, 50V power mosfet which it is until a critical parameter is exceeded. From then on, internal protection circuitry takes over.

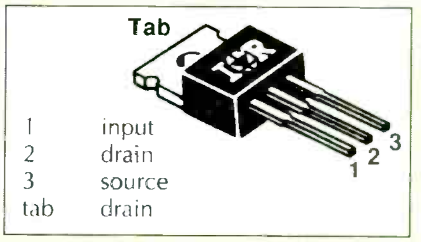
Referring to the functional diagram, the zener diode between the input and source provides ESD protection for the input and also limits the applicable voltage at the input to 10V. This mechanism will withstand the full 4000V body model discharge through the input pin of the device removing the need for any special handling precautions.

The internal RS bistable memorises the occurrence of an error condition and controls the state of the output transistor through Q_2 and Q_3. The flip-flop may be cleared by holding the input to the device low for a specified minimum period, typically around 7μs.

The comparator pair senses overcurrent and over-temperature signals against an internally generated reference. Either comparator can reset the fault flip-flop and turn the power transistor off. During fault condition, Q_2 disconnects the gate of Q_1 from the input while Q_3 shorts this to ground ensuring rapid power device turnoff.

The zener diode between the gate and

drain of the main power transistor causes channel conduction when the drain-source voltage of the device exceeds a predefined limit



Device operation

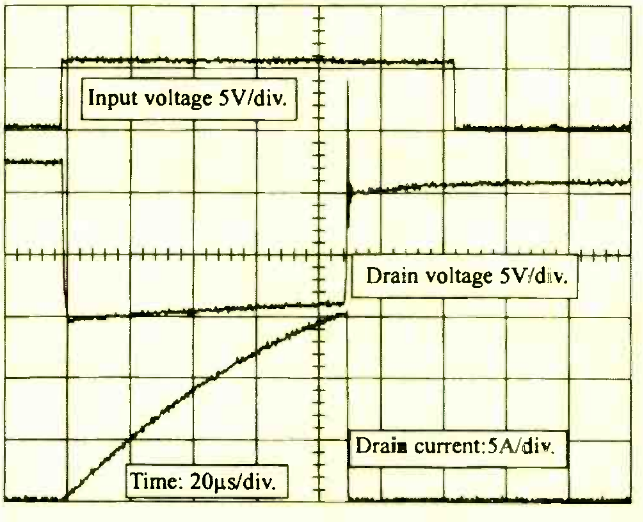
The control logic and protection circuits are powered from the signal on the input pin of the *IRSF3010*. When positive voltage appears at the input to the device, the flip-flop turns Q_2 on and connects the gate of the main device to the input. The turn-on speed is limited by the channel resistance of Q_2 and the gate charge requirements of Q_1. Using a higher input voltage will improve the turn-on time but it does not affect the turn-off switching speed. The control circuitry draws around 300µA from the device input terminal enabling compatibility with most drive circuitry.

When the drain current exceeds the preset limit, the protection circuit resets the internal flip-flop and turns Q_1 off. Holding the device input below 1.3V for a minimum of 7µs will restore normal operation. Unlike schemes which monitor the total current through the power transistor channel, current measurement in the IR device is made by examining the current flowing in just a few cells out of the several hundred thousand which make up the power transistor. This avoids an increase in device saturation voltage to accommodate the sensing circuitry.

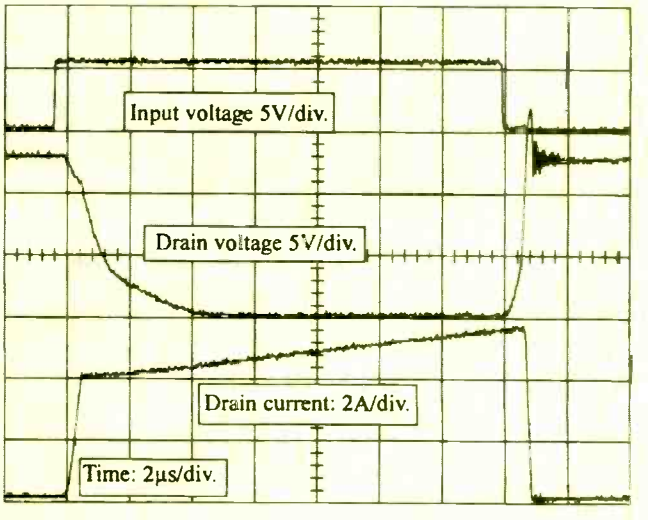
The device overvoltage circuitry also differs from the conventional. When the drain to source voltage exceeds 55V, the zener diode between gate and drain turns the device on before the breakdown voltage of the drain-source diode is reached. This greatly enhances the energy the device can dissipate during turn-off of inductive loads compared to the avalanche breakdown mode. Thus the transistor can be used for fast de-energisation of inductive loads. The absorbed energy is limited only by the maximum junction temperature. ■

READER SERVICES OFFER

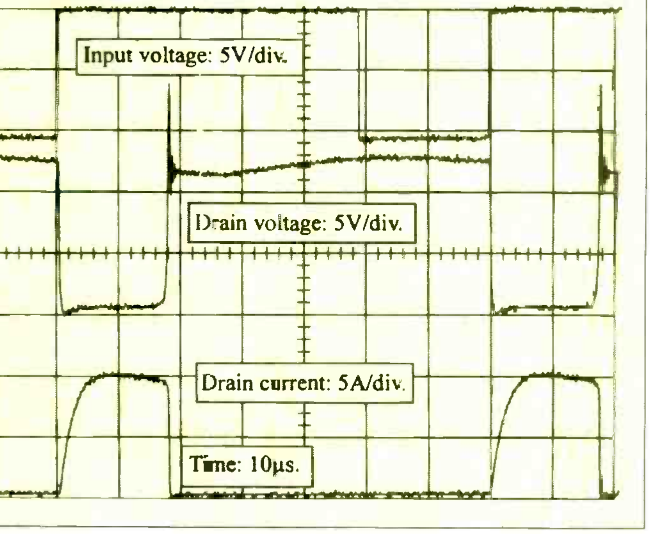
To obtain your free sample of the International Rectifier *IRSF3010* protected power transistor, fill in and send off the special reply card located between pages 1024 and 1025 of this issue. This reader services offer is being handled directly by International Rectifier. Our editorial office is unable to assist in any queries relating to it. This offer is restricted to the first 500 replies.



Above. Typical waveforms at overcurrent shutdown. After turn-on, the current in the inductor at the drain starts ramping up. At about 15A, the overcurrent protection shuts down the device.



Above right. Switching waveforms from clamped inductive load using 5V input voltage. In typical switching applications below 40kHz, the difference in switching losses between the IRSF3010 and a similar current rated standard mosfet is negligible.



Right. Over-temperature protection. The graphs show an IRSF3010 switching a 1Ω resistive load connected to a 12V power supply. When thermal balance is established, the junction temperature is limited on a pulse by pulse basis.

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Variable-inductance, low-frequency VCO

£100 WINNER

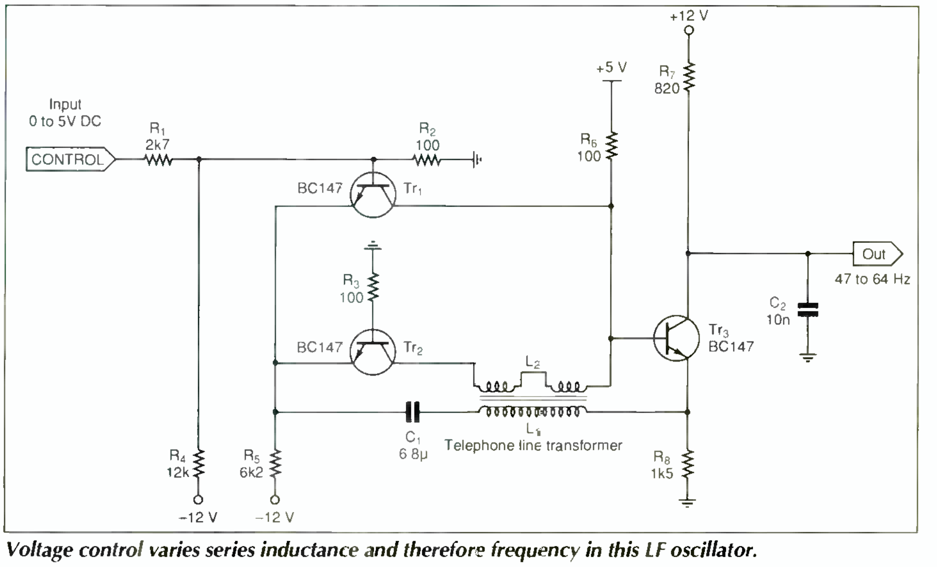
Variable-frequency oscillators using the then principle of varying inductance of a coil by varying mutual inductance in a transformer were first described by K C Johnson in *WW* April and May 1949. My adaptation is shown in the diagram.

If L is the inductance of a coil through which flows an alternating current and some part of the same current flows in a mutually coupled coil, the effective inductance of the first coil L_e is $L_2 \pm M$, since the second coil may or may not be wound in the same sense. M is the mutual inductance.

A differential voltage-controlled amplifier can be used to vary the proportion of the oscillatory current flowing through the second coil, the total oscillatory emitter current being shared in a varying proportion between the two halves of the amplifier. Since the effective inductance is in a series resonant circuit, the oscillator frequency also varies.

Transistor Tr_3 is an emitter follower feeding the common-base amplifier made up of Tr_1 and Tr_2, the differential pair, whose output goes to Tr_3 and completes the loop. Loop gain is set by $R_{6B\Delta2}$ to just over unity. Frequency is determined by C_1 and L_e, although since the coil in Tr_2 collector passes a direct current, ferrite cores affect the frequency.

In the oscillator shown, L_1 and L_2 were made from a telephone exchange line transformer, which gave a frequency range of 47-64Hz for a 0-5V input voltage.



Voltage control varies series inductance and therefore frequency in this LF oscillator.

Squegging at 600kHz occurred at zero crossing points, which was eliminated by the addition of C_2; a more suitable transformer may be designed to avoid the problem.

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DS1233 replaces monostable

Dallas's *DS1233 EconoReset*, described in the March 1992 issue (p910) normally resets a microprocessor after detecting upsets on its supply, but has other possibilities, being effectively a monostable in a TO-92 package which maintains a low on the output for 350ms after power is applied. Here, it delays and produces an inverted pulse with a fixed width. Its frugal power needs can be supplied by a cmos gate.

Figure 1 shows the former, in which it delays a rising edge by 350ms, replacing a monostable and an and-gate. When the cmos gate output rises, the *DS1233* output remains low for 350ms, going high after that period and returning low when power is removed.

In **Fig. 2**, a negative-going pulse wider than 350ms at the gate output produces a 350ms pulse from the *DS1233*. When the gate output goes low it applies power to the *DS1233*, the output going low for the time-out period and then returning high, unless the gate output is shorter than 350ms, in which case the output will correspond to the input.

Steve Winder
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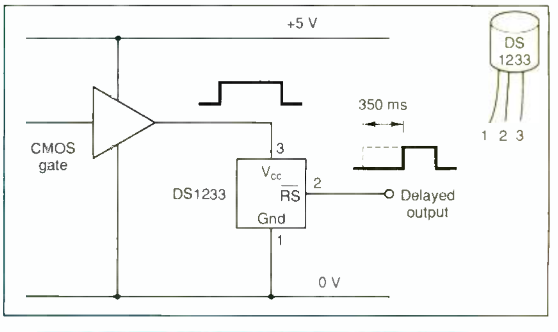

Fig. 1. Dallas's Econoreset microprocessor reset device used to delay a pulse rising edge by a fixed 350ms. Used in such a way, the DS1233 replaces a monostable and an And gate is contained in a small package. Power comes from the cmos gate.

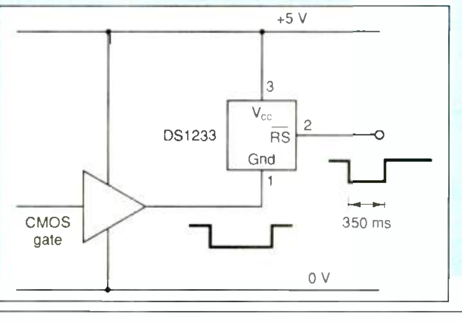

Fig. 2. The DS1233 produces a fixed 350ms negative-going pulse.

PC counter uses parallel printer port

Needing to use a PC as a counter/timer without tying up the i/o bus, it seemed that the printer port would serve the purpose, but that the counter would need a separate power supply. In the event, this was unnecessary, since power at 8mA is derived from the serial port. The circuit allows measurement of frequency and period of a TTL input under software control from the PC.

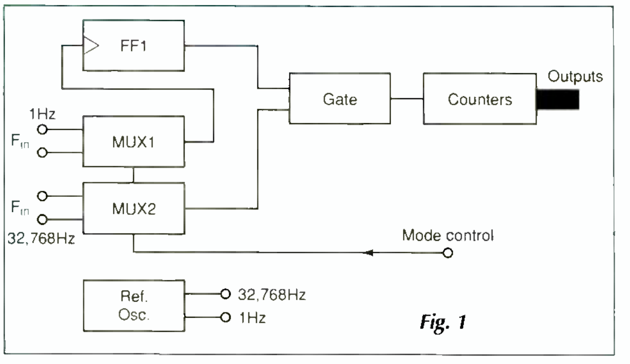

Fig. 1

Figure 1 shows clock signals coming from the *4060* 32.768kHz crystal oscillator, which delivers the basic crystal frequency for period counting. In this mode, one cycle of input signal gates the clock to the counter. In frequency measurement the gate is open for 1s, during which the input goes to the counter. Four quad tri-state switches pass the counter output, a nibble at a time, to the status port.

Operating procedure is first to select the frequency or period mode; to reset flip-flop 1 and the counter, FF1 being set by the rising edge of the input or the 1Hz reference in period mode; counting begins and when FF1 output goes to 1, counting stops. The PC then reads the 16 bits, four bits at a time.

Figure 2 is the complete circuit diagram of the counter adaptor and **Fig. 3** the power supply using the serial port.

The 5-bit input status port reads the count and monitors measurement cycle status, the data port to enable tri-state switches and for mode selection and the control port to reset FF1, the address of the printer adaptor in use (LPT 1, 2 or 3) being found in the dos data area.

In period mode, the count must be multiplied by 1/32768 to obtain a sensible reading.

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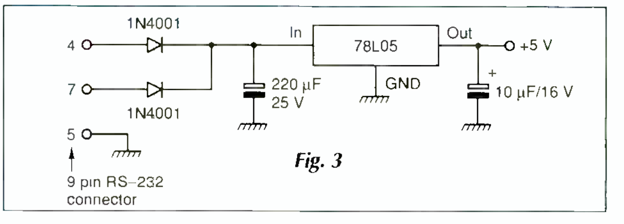
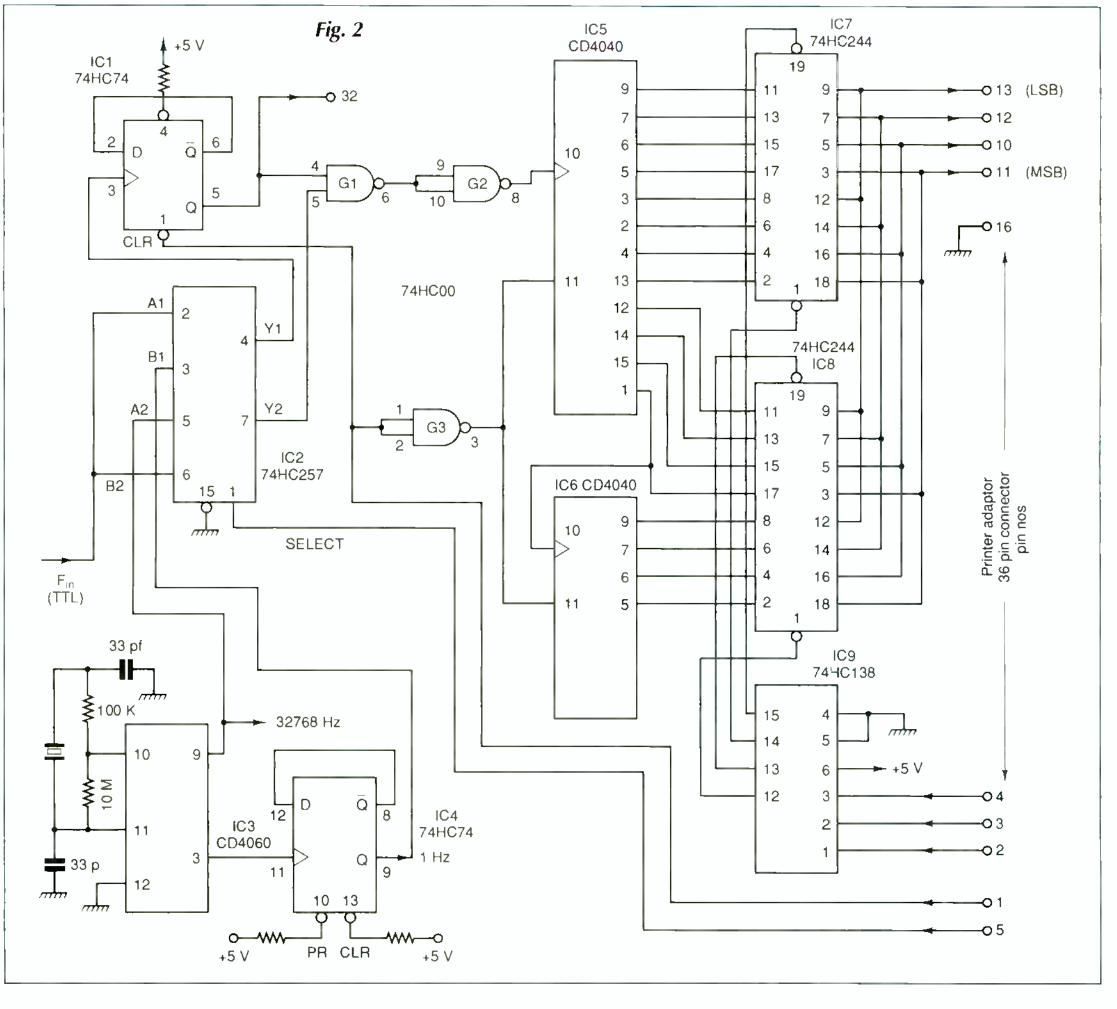


Fig. 3

Fig. 2



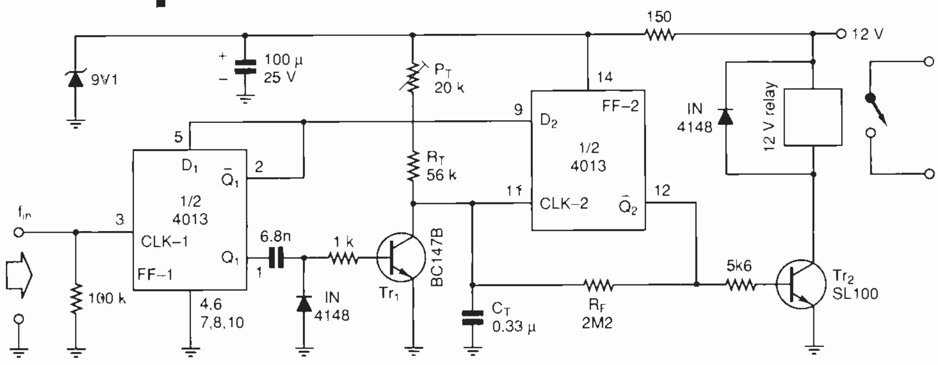
Using a PC's printer adaptor, this circuit converts the computer into a frequency/period counter needing no other power supply than the serial port.

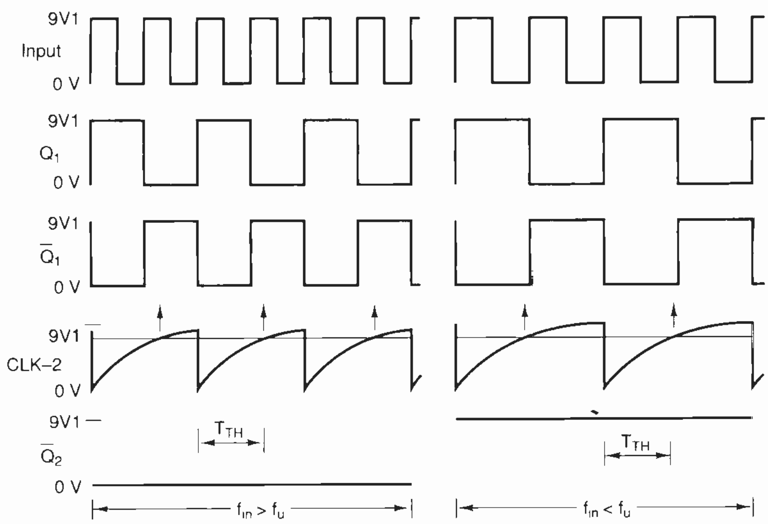
Under-frequency inverter protection

If a 50Hz inverter's output frequency falls below that required by the equipment it powers, this circuit disconnects the output.

Input comes from the inverter's driver stage, any asymmetry being eliminated by the first D-type flip-flop. At each low-to-high transition of Q_1, C_T discharges through the transistor Tr_1 and begins to charge again through R_T and P_T. As this voltage reaches the threshold voltage of Clock 2 input, the $\bar{Q}_1$ output latches into the second flip-flop. As shown in the timing diagram, the $\bar{Q}_2$ output, which drives the output transistor and therefore the relay, is either 0 or 1, depending on the input frequency. Resistor R_F inserts a little hysteresis to prevent relay chatter.

Adjust P_1 to make $T_{TH} = T_u$ (=$1/f_u$, the frequency at which the relay disconnects the load). This trip frequency can lie in the 48-62Hz range with the components shown.





Simple circuit disconnects inverter output if its frequency falls below a preset limit. It could easily be used with portable AC generators.

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Single-diode full-wave rectifier

This single-diode, single op-amp rectifier is used for LF rectification in an RTTY FSK demodulator.

During a positive input half wave, D_1 conducts and the circuit becomes a non-inverting amplifier, so that

$$v_{out} = v_{in}\frac{R_1}{R_1+R_2}$$

for positive inputs. On negative half cycles, D_1 is virtually an open circuit and on negative inputs.

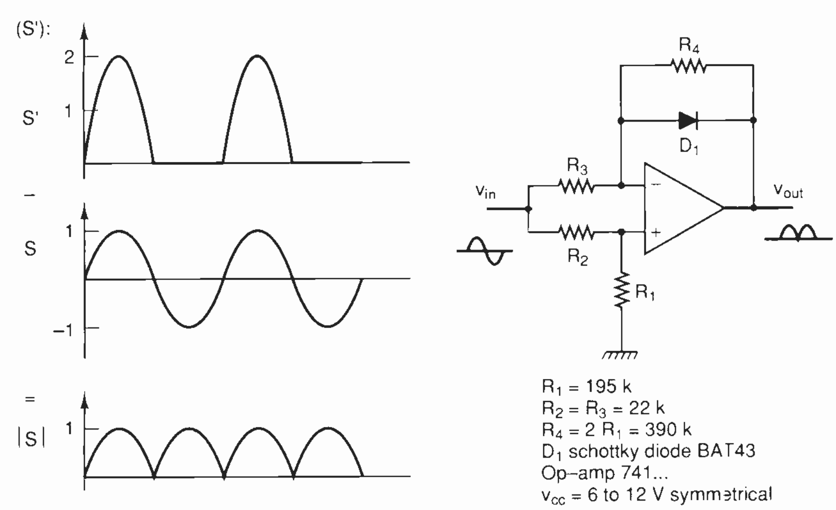
$$v_{out} = v_{in}\frac{R_1}{R_1+R_2}\left(1-\frac{R_2R_4}{R_1R_3}\right)$$

Making $R_3 = R_4$ and $R_1 = 2R_2$ reduces this to

$$v_{out} = v_{in}\frac{-R_1}{R_1+R_2}$$

which is the inverse of that for positive inputs and both half cycles are amplified.

Diode imperfections can cause an imbalance between the halves; in such cases, increase R_1 to 200-220kΩ.



Using only one diode and a single op-amp, this is a low-frequency, full-wave rectifier

Francois Guillet
France

LETTERS

Dirty Windows

What an interesting coincidence that Barry Fox's guest editorial (*EW + WW*, September) querying whether innovations and fancy features actually satisfy users needs, was in the same issue as some wag was telling us that Microsoft had spent the last ten years perfecting *Windows* (Update).

Is that why we hear about unrecoverable errors, lack of speed, the amount of hard disk space used, how many third party applications have to be loaded as well, how it gobbles up memory or what a pain it is to do a simple thing like copy a file? Of course, all these things will be sorted out in *Windows NT*, won't they? Or did I hear there was something called *Cairo* beyond that?

A less charitable view is that for the past 12 years Microsoft's operating systems have been crippled by some very poor decisions made in the eagerness to rush out something for the IBM PC, and the various versions of *Windows* followed a similar pattern because of eagerness to compete with the Macintosh gui.

Anyone who strays into their local school is likely to see quite young children opening windows, resizing them, launching applications by double clicking with a mouse, selecting files created by one application and dropping them into another. In other words using Acorn *Risc Os* they can do all the things a Windows user wants to do, and a good deal more easily.

Isn't it time that someone asked why it is that a small British company can produce a wimp based operating system which runs comfortably on a 1Mbyte machine with a single floppy disk, while multi-million dollar Microsoft is still

Out in the Cold

I was most interested to read Andy Wright's article on cold fusion (*EW + WW*, October). The emphasis is more on the radiation emitted and products formed, rather than on heat production. Even so, some important points were omitted, presumably for brevity. The original authors (Pons and Fleischmann) have withdrawn their claim for radiation emission and tritium formation. They concentrate only on heat production. They generate enough heat to bring the electrolyte to the boil, but the heat is much more easily explained in straight chemical terms on the assumption that there is no cold fusion.

I have seen a video of the F & P equipment in action and was surprised to see that no effort had been made to keep oxygen away from the palladium. The fact that hydrogen saturated palladium gets hot in the presence of oxygen has been known for a very long time. Palladium acts as a catalyst in the conversion of hydrogen (or heavy hydrogen) and oxygen to form water and heat.

During normal running the palladium is surrounded by oxygen in solution in the electrolyte, by oxygen bubbles coming off the platinum anode, and by oxygen in the gas above the liquid. Heavy hydrogen bubbles coming off the palladium effectively purge the oxygen from solution in the immediate vicinity of the cathode. If this equilibrium is disturbed, so that some oxygen reaches the palladium, then a hot spot is created, this sets up a convection current, bringing more oxygen down from the anode round the bottom of the tube and up past the central palladium electrode, producing even more heat. In the video, the electrolyte came to the boil, allowing oxygen from the gas phase to reach the palladium.

The total heat generated in the experiments of F & P was always less than the electrical energy put into the system. The electrical energy input was applied over several days or weeks. During this time it was accumulating a store of chemical energy in the form of hydrogen in the palladium. If for any reason, oxygen reached the palladium then this accumulated energy was released in a few minutes.

If I am right then you would also expect an experiment using ordinary light water to generate heat. Well, according to Pons himself, "It does". See *Nature* Vol 338 page 691.

David Dewey
Happs Edge, Herts

Andy Wright's timely reminder (*EW + WW*, October) that there is life in cold fusion after Fleischmann and Pons gives me a chance to state that there was one experimental angle that was ignored by the lemmings who rushed to exorcise the fusion cell 'heresy' threatening 'good' megabuck science.

All the experiments set up to investigate the F & P results took great care to screen the experiment from external radiation.

F & P did not – in fact the successful tests took place in an open laboratory well above sea level during the last solar maximum.

Could it be that the fusion cell has to be pumped with external radiation to start the reaction, and that this happened accidentally in the laboratory on several occasions coinciding with a solar flare? It would be easy to check from the solar emission records.

There's nothing unusual about starting a reaction by adding energy from a different source.

The chemical reaction in every internal combustion engine is started by external cranking power, and a fusion bomb has to be triggered by an atom (fission) bomb. So why not use external nuclear radiation to prime a cold fusion cell?

Until this approach has been tested, I consider reports of the death of cold fusion à la F & P to be premature and unjustified.

Anthony Hopwood
Upton-on-Severn, Worcester

The article "Clawing back respectability for cold fusion?" (*EW + WW*, October) tells us how AEA Harwell's researchers were unable to duplicate the Fleischmann and Pons results, but also reports that some researchers are "gaining tantalising glimpses of the effects first noted by Pons and Fleischmann".

Obviously, there is a reason why some fail and some occasionally succeed and eventually, with hindsight, the reason will become as clear as our understanding of why an oscillator can need an initial stimulus before it starts oscillating.

The F & P tests were seen to involve possible errors in estimating heat production due to small temperature differences between different cathode regions in the cell. Therefore, in setting out to replicate the experiment and measure any excess heat with greater precision the so-called experts used calorimeters in which cell temperature was assuredly uniform to within a small fraction of a degree.

The cold fusion reaction did not occur.

The physics of the 19th century tells us that a temperature gradient can develop an electric potential in a metal and so a non-uniform temperature can set up a residual charge in that metal. Such a source of negative charge could, within a cathode full of positive deuterons having the right geometry and current excitation, assist in bringing those deuterons close enough to fuse. But one needs a temperature gradient.

The cold fusion process no doubt depends upon the prior existence of a temperature gradient in the cathode before it develops heat that sustains in that cathode a temperature gradient so heat can be conducted away. This, as we well know from analogy with electric circuit theory, is a recipe for exponential escalation, instability, and even the runaway heat generation that F & P found in one experiment. The action needs that initial temperature gradient to be triggered!

So, since Harwell and others set out to do calorimeter tests rigorously and properly with well-monitored calorimeter apparatus, deliberately minimising temperature differentials to assure the temperature was monitored precisely, they merely choked off the action they sought to measure.

The recipe for sustained success involves injecting heat initially to get the cold fusion reactor started. The trigger depends upon a thermoelectric phenomenon, the Nernst effect.

Harold Aspden
Chilworth, Southampton

promising to sort things out with Windows NT? The last thing I read about Windows NT said that it would expect to find 8Mbyte of ram, but really needed 12Mbyte!

Apparently not! Month after month the computer press is full of reviews with headlines like "C compiler shoot out", "486 wars" or "Word-processor head to head". Magazines get fatter, worthwhile articles get fewer, but the advertising revenue rolls in.

Sadly I'm beginning to see the first signs of this trend in *EW + WW*. Almost every month there is an article described as "PC Engineering". It isn't, it's just a program review by a fancy name. I cannot remember when I last saw an article that mentioned any other computer than a PC.

The assumption seems to be that the PC is the industry standard and that any other computer must be a toy. Unfortunately joining two or three pieces of standard and supposedly compatible equipment, then persuading them to talk to each other, can still take a very long time.

I find it very hard to believe that people are not finding worthwhile and commercially viable uses for computers like the Amiga, Atari or the various Acorn Risc machines, which could find a mention in your pages. Looking back over 20 odd years of your magazine in its various guises, one thing that stands out is the number of oddballs finding a voice in your pages. So why the present obsession with helping Bill Gates' bid for world domination?

Les May
Rochdale

I agree with every word the corespondent says. Intel architecture is slow and stunted while Microsoft operating systems have always been cumbersome and inefficient. How IBM ever allowed Bill Gates to become the world's highest paid executive, and Intel the world's most profitable semiconductor is beyond me. The truth is that the two companies have more of their products in use than all their competitors combined — by a factor of several times. To ignore this in our reviews would be to do a disservice to our readers.
Personally I use a Macintosh.
Editor

Kids playing with Windows

John Carrey raises some very valid points about the dreadful *Windows* (*EW + WW*, October). To my understanding *Windows* was conceived as an aid for children to use PCs without the need to comprehend dos. That the adult world embraced the product is hardly in accordance with the old quotation: "When I became a man I put away childish things". Apart from this large useless package taking up a useful chunk of my hard disk. I can do anything quicker under dos.

I resent the loss of some 9Mbyte of disk space for a program that I am forced to use to run software because there is no dos alternative. But how much worse it is for schools with their low budgets and old machines, where a 40Mbyte hard disk is a luxury; more than 25% of disk space taken up with operating systems!

Professionally, I am involved in satellite remote sensing analysis, where the operational software is dos based. I am happy to report that I don't know of any *Windows* products in this field.

Recently I completed a low cost satellite image analysis package for schools, which includes 20Mbyte of high resolution satellite images, which for low capacity hard disk users can be loaded individually (250Kbyte each) from floppy. The analysis software requires 1Mbyte and no it does not run under *Windows* nor ever will!

DJ Standen

Slower using Windows

John Carrey's letter (*EW + WW*, October) criticises several aspects of Windows. The writer, as do other Windows critics, overlooks a basic fault inherent in Windows software.

Much commercial use of Windows type software involves continuous interaction with the keyboard user. The typical slow reaction time of the user partly conceals the extreme slowness of Windows basic execution.

Our work uses PC programs that need minimal user interaction and emphasise any slowness in execution. Two pairs of sample runs – each using identical input data and a 66MHz 486 system – demonstrate the inefficiency of graphics based text screens. These programs allow a run-time choice between text only and EGA graphics based screens.

For data requiring limited calculation the text only screen took 9s. An identical calculation using the EGA alternative took 283s – more than 30 times as long.

With data needing extended calculation the graphics screen had less effect but still took twice as long – 5 and 10 hours.

These were short test calculations. Practical use implies single runs lasting from a few minutes up to several months continuous calculation – with pro rata time increases for EGA. Apologists for Windows state that faster processors will solve this kind of problem – forgetting that many basic calculations are still far too slow.

Windows NT appears to offer even worse possibilities. A recent review emphasised its need for the fastest processors – presumably not to improve the speed of basic calculation.

When will someone produce a 32bit operating system that combines all essential basic facilities with maximum processor utilisation and excludes complex gimmicks?

RG Silson
Tring, Herts

Relay breakdown

After reading A. Millar's letter (*Clunky versus Cost*, *EW +WW*, October), I feel that several points raised in the letter are in need of clarification.

Mr Millar says that you cannot dismiss the mechanical switch or the relay too lightly. I wasn't aware, from what was written, that I had. The manuscript, as originally submitted, went into some depth about the pros and cons of said devices, but the editorial knife removed these references, probably because the article was primarily about solid state switching.

As far as lab tests on a new board are concerned, I, too, wholeheartedly concur that a quality relay does present itself as a perfect switch – no semiconductors to distort the signal or cause noise when new. However, Mr Millar seems to have missed the fact that all relays do age, the cheaper types faster than others. Once contacts become oxidised, the resultant high resistance, or resistance modulated by signal level, will cause all manner of intermittency, noise and distortion problems.

Cost was mentioned briefly by Mr Millar but not properly pursued. Yes, the *Focusrite* console dispenses unilaterally with any solid state switching, and its sonic performance, in all respects, is widely acclaimed by the pro-audio industry, and rightly so. However, it does cost hundreds of thousands of pounds; transparent audio performance is not achieved without some considerable cost. The real challenge is to engineer an audio switch which is fairly transparent and is economic enough to be fitted hundreds of times over in a budget/mid-priced console.

Furthermore, the cost of relay switching isn't related purely to the cost of the devices used, but more to the careful design of the environment surrounding the component. The inductive nature of the relay means that audio and switching ground return paths have to be isolated if splats are to be avoided. This philosophy can be extended as far as providing completely separate switching and audio supply rails, mechanical isolation of the relays (separate PCB's) and hefty

Spectrum space

The article "FM stations may close in spectrum shake-up" (*EW + WW*, September) about finding room in the spectrum for T-DAB makes me wonder whatever happened to bands I and III? These useful frequencies, once the home of 405-line tv in the UK, are still used for tv in the rest of the world.

I well remember the introduction of 625-line tv on uhf. We were told that, in about 20 years time, the vhf bands would carry two 625-line networks, in addition to the four planned on uhf.

Joseph B Fox
Redhill,
Surrey

trackwork/extensive ground planes. Furthermore, mutual-inductance coupling, poor regulation of supply rails, even microphonic pickup, all have to be considered if a design is to be a success. The extra time this requires at the design stage, the cost of larger or separate PCBs, drive and protection circuitry, isolation using opto-isolators etc. all add insidiously to the overall cost.

As far as the *SSM2142* solid state switch package is concerned it is sonically attractive but costly, around £8 per IC, with the switching function made "splat-free" using internal complementary ramp generators and comparators. Again, performance is achieved with cost.

Where commercial mixer switch designs are concerned, manufacturers are understandably reticent to publish circuit diagrams, so comparison with those shown in the article is somewhat difficult. What I had intended from the paper was an appraisal of the basic techniques employed in audio switching, rather than to provide the last word on commercial, cost-no object, topologies which have little relevance to most budget or mid-priced applications.

Mike Meechan
Reading
Berks

Absolute test not needed

I refer to the letter from Greg M Ball (*EW + WW*, August) about my articles a year earlier (*EW + WW*, July 1992). He notes that the simple THD test circuit (my **Fig. 1a** reproduced from the Burr Brown data sheet) results in a common mode input to the op amp as large as the signal output, which I did not specifically point out as it will have been appreciated by most readers.

Additional distortion in the non-inverting connection compared with the inverting circuit (often described as being due to common-mode failure) is a well known phenomenon and is the reason the inverting connection is usually preferred where lowest possible distortion is the design criterion. Equally the non-inverting circuit is usually preferred where lowest possible noise is the design criterion, leaving one with a problem where the largest possible dynamic range is the goal, since then noise and large-signal distortion are equally important.

The additional distortion in the NI connection due to common-mode failure is, as Ball notes, often even order, but my measurements show that the residual distortion of the OPA2640 is also even order in inverting operation. This leads to the intriguing possibility that in the NI connection there could be either addition or partial cancellation of the two sources of second harmonic distortion.

So while the ingenious Burr Brown test circuit is very convenient for an approximate evaluation of the device's distortion using a THD meter with only a modest performance, for precision measurements there is prima facie no substitute for a test set-up that takes absolute distortion measurements without relying on the distortion-multiplying arrangement discussed.

However, in practice less esoteric equipment can prove entirely adequate. Thus, where a designer has chosen to use the NI connection, the additional distortion due to common mode failure has to be accepted and the test method discussed (using the same gain as in the application envisaged) is appropriate.

On the other hand, for the inverting case, one can use a technique similar to one often used in evaluating an op amp's settling-time. A side chain consisting of an input and a feedback resistor equal in value to those defining the op amp's gain is used, the voltage at their junction being a mirror of that at the op amp's inverting input, that is the drive signal is largely cancelled out at this point.

Slight adjustment of one of the sidechain resistors, plus maybe a whisper of quadrature trim, let the input signal be entirely outphased at this point. It can then be connected to the virtual earth of another op amp, which will provide an amplified version of any signal at the output of the DUT for which there is no corresponding input signal, viz the DUT's distortion.

While cancellation of the input signal can never in practice be absolutely complete, up to 60dB of input signal rejection is certainly feasible, permitting the use of a modest THD meter to complete the measurement.

Ian Hickman
Waterlooville, Hampshire

Neural omissions

With reference to my article "Neural networks hit the jackpot?" (*EW + WW*, August), an important part of the original article appears to be missing.

The missing section should be added at the end of the box "Back propagation algorithm", where it states: "Contribution to the network error of the weights located between the input and hidden nodes can be found from calculating the derivative as follows:"

Unfortunately the calculations are not shown. Here is the missing part:

$$\frac{\delta E_n}{\delta W_{ij}} = y_i y_j \left(1 - y_j\right)\beta_j$$

where β_j is the error at the output of a hidden node, and is defined as:

$$\beta_j = \sum_k W_{jk} y_k \left(1 - y_k\right)\beta_k$$

We have derived β for each layer of the network, all that remains is to adjust the weights in the network to reduce the error. The change required in value for a weight between the input and hidden nodes is given by:

$$\Delta W_{ij} = -\delta y_i y_j \left(1 - y_j\right)\beta_j$$

and likewise for a weight between the hidden and output nodes:

$$\Delta W_{jk} = -\delta y_j y_k \left(1 - y_k\right)\beta_k$$

where δ represents the step size used in weight adjustment.

A typical value for δ used in other optimisation methods is 0.5. This is confirmed by Drew van Camp (a computer programmer and researcher at the University of Toronto).

Also, there is a small but important printing error on page 652 in the text below the first equation: e_i is not squared as stated. The second equation is correct since this involves taking the sum of the square of the errors.

George Overton
Kelmscott, Leicestershire

Give Workbench a chance

It is to be regretted that your reviewer of *Electronic Workbench* Pro (*EW + WW*, September) gave it a somewhat cool reception. It is obvious to me, that insufficient time was spent with what is after all a unique example of cad software. And it is unfortunate that the simple circuits that come with the software were the only ones that were tried.

The generally negative tenor of the review might well deter younger computer users and educational establishments from investigating it: where else can you find a program that has all the features it offers and at the price?

Sure enough, having used it for a number of months, it has idiosyncrasies and the odd bug or two (which were clearly not discovered, either). But then, what cad software hasn't? If I wanted more accurate quantitative measurements, I would go for *Spice* or *Analyser III*.

But for a designer, the sheer pleasure of knocking together a sample circuit in a few minutes and seeing how it behaves is extraordinarily valuable and time saving. Yes, it is memory greedy and not a little tardy, but with greater familiarity, ways round all these become apparent.

Also, version 3.0 is due any time and will address all the criticisms I have of it. But has your reviewer ever waited for a student to construct and then fathom out the workings of a simple circuit on a laboratory bench? This takes 2min 25s using a 386 plus coprocessor for a bandpass filter, which was the longest simulation I have recorded – about the same time for the soldering iron to heat.

Reg Williamson
Kidsgrove, Staffs

CFA: the last word?

FM Kabbary's letter (*EW +WW*, September) seeks to continue the debate on the crossed-field antenna but maybe it is time this dead horse was spared further flogging.

The claim to have found corrections to Maxwell's equations places Kabbary firmly in the ranks of the eccentrics. As for the assertion that many scientific and rigorous measurements have been made on the CFA, I feel this would be more convincing if any of these results had ever been published.

In the "CFA – RIP" article (*EW + WW*, May) a CFA was shown to produce a loss of 23dB, which corresponds to an efficiency of 0.5%. This is consistent with the results quoted by Martin Spencer (*EW + WW*, June 1991) who found an efficiency of 0.1%. These results are in my opinion quite believable and I do not think the CFA's protagonists can improve very much on them in properly controlled conditions. If I am wrong, where is the evidence?

Alan Boswell
Great Baddow, Chelmsford

Respect the giants

For many years space has been found in *EW + WW* for entertaining controversy about the validity of experiments on the effect of movement on the propagation of light. I want to suggest that it is unfair to readers without specialist knowledge of the issues to continue to imply that the observations are open to simple dispute. If you continue to publish letters perhaps they should come with some sort of health warning.

For those unfamiliar with the correspondence a brief explanation is appropriate. In the 19th century a number of experiments were carried out to discover the effects of moving the apparatus used to measure the speed of light. Those which Michelson and Morley performed in 1887 are the most famous.

It was strongly believed that light

was a wave motion and it was natural to expect that moving the apparatus would alter the speed of the light in the same way that wind alters the measured speed of sound. No effect at all could be discovered. This was a surprise to the earlier experimenters though it was probably what Michelson and Morley had come to expect.

However the source and receiver are moved, the measured speed of light in free space (commonly written as c) is, to the limit of experimental accuracy, that predicted by Maxwell for electromagnetic waves.

These experiments were difficult because the speeds with which natural effects move the apparatus are quite small compared with c. The speed of the earth in its orbit is about 30km/s compared with c at about 300,000km/s. To make the situation worse the effects studied depended on $(v/c)^2$.

Nevertheless, so long ago as 1892 Fitzgerald accepted the correctness of the observations and published the hypothesis that some then unknown physical effect shortened moving objects by just the amount needed to conceal the expected effects of change in speed. Later theorists showed that the effect would also have to reduce the duration of effects in moving apparatus to explain the observations fully.

Einstein's approach was entirely different. Accepting everyday experience, he assumed that motion had no effect on physical objects: changes that are only apparent arise in rulers and clocks when we try to relate measurements made at different speeds in a way that takes into account the constant velocity of light.

Later astronomical discoveries revealed movements, including the rotation of the galaxy, with speeds about ten times as great as the Earth's orbital motion. These factors too might have been expected to produce observable effects. Because of $(v/c)^2$ these would be a 100 times as large, making our confidence in the null actually recorded far greater than the experimenters themselves could feel.

All attempts to detect these effects of motion on the speed of light have relied on comparing the speed in two different directions. Until the development of atomic clocks in the last few decades indirect methods had to be used and these led to the $(v/c)^2$ that made the effects so small.

Nowadays it is possible to work in the obvious way with one clock at the source and another at the receiver. The global positioning system using artificial earth satellites inverts the procedure, assuming the speed of light to be constant and deducing positions by measuring the difference in arrival times of radio signals from several satellites. Any variation of the speed of light along one path would produce a proportional change in the apparent length of that path, leading to a corresponding error in position.

The accuracy of the system is a few tens of metres, while the path lengths are a few tens of thousands of kilometres. Thus changes of the speed of light of around one part in a million would be noticed as malfunctions of the system. I have noted above that the Earth's orbital motion has a speed one ten-thousandth part of that of light, much greater than this resolution.

As these satellites are in rapid motion relative to the Earth the suggestion that a stationary Earth is an adequate explanation for the null results of the 19th century experiments is ruled out. There are similar but more complex experiments which show the limit to be more than two orders of magnitude smaller. These measurements are so accurate that a second is now defined to be the time taken by 9,192,631,770 oscillations of a resonance frequency of the atom of cesium 133. The metre is defined implicitly by specifying the speed of light to be 299,792,458 metres per second.

It must be admitted that it is very surprising but light waves do not behave like sound waves or water waves in this respect. Twentieth century studies have shown that there are rather few respects in which they are similar but the others don't seem to worry your correspondents so much.

I have to say that most of the letter writers reveal an unattractive arrogance. Not only Einstein but several others who have contributed to the growth of modern physics are among the greatest intellects the world has known. How can anyone believe that with a few minutes casual thought (or rather lack of it) they can discover these giants' errors?

Michael Weatherill
Fife

MASTERING analogue filters

Designing a good analogue filter can be tedious and time consuming. Filter Master Active for the PC makes design quick and easy but at a price – as John Anderson explains.

Filter Master Active is a dos based filter design and optimisation tool intended to help specifying, dimensioning and analysing analogue filters. The package is from Omicrom, licensed by Intusoft of San Pedro, California. It handles a range of filter pass characteristics and allows selection of various approximations. There is also a choice of design options.

I remember well the struggle of synthesizing analogue filters to solve specific problems. The task was always tedious and a tricky compromise in component selection. This product provides a good route through the problem and is fast, allowing plenty of iterations in a reasonable amount of time.

Package overview

Comprising just a slim 150 page slim paperback manual, a disc and a parallel port dongle, the package costs over £600. Its manual is professionally produced and supplemented by a number of screen examples. A dozen sheet 'application note' is supplied though in reality this is really an addendum to the manual.

Installation was simple and uneventful, taking about 1.2Mbyte of hard disc space. The files comprise a number of Borland Graphical Interface (BGI) types. These allow the software to work with a wide range of different screen formats from CGA to VGA. Automatic screen sensing can be manually overridden to force mono graphics for lap top operation for example.

Tutorial section

On starting the program you are presented with an opening menu. This is the root menu for a quite complex tree of menus used to set the options for the program, synthesize filters and output results.

The manual leads in with an excellent tutorial of the design of a tenth order Cauer filter which took longer to specify than to synthesize! In only a few minutes, the tutorial introduction took this first design from paper specification to final design. This shows the user interface to be if not pretty then at least intuitive.

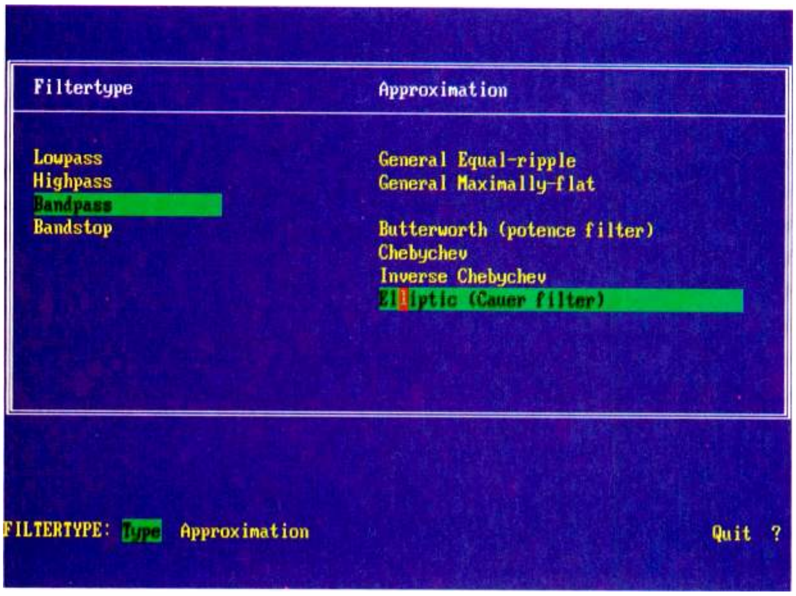
These glowing comments must be balanced against a fairly crude menu tree compared with modern graphical user interfaces. This problem shows up again in several other aspects of the program performance. In the end however, it is functionality and productivity that matter.

Throughout the program – even in graphics mode – a context sensitive help facility is available. It is at best adequate and at worst just a short description of each command. The help contents is a list of descriptors, usually one word, presented in a rather untidy list at the top of the screen.

Filter realisation

Filter Master Active uses a cascading technique to implement the final filter design. The technique involves a decoupled modes approach where first and second order filter structures are compounded to produce the final transfer function. In practice, problems can occur with this approach if capacitive loading on the output of the op-amps is large. This loading introduces additional poles in

Selection of the analogue filter type and its approximation is straightforward. The process is simplified further by using the mouse option.



the transfer function. In severe cases the current limit of the op-amp could be exceeded and a non-linear slew rate limit imposed. The filter synthesis technique is supposed to ensure that capacitive loading is kept low.

During the set-up sequence there is an option to select how the component values are to be realised. Options are specifically based on normal component values, the exact value or values based on series or parallel combinations of values.

To aid inspection of the synthesized filter, it can be 'drawn' as a circuit diagram using text characters. This is both crude and likely to cause confusion – if there was ever a reason for using a GUI, this is it. A nice feature is the ability to alter the individual component values. This allows assessment of the effects of choosing more practical component values. However this facility falls a long way short of a Monte Carlo tolerancing facility needed to determine the range of filter performances that might be expected with real components.

It is important to remember that *Filter Master Active* is limited to the design of active filters (those with operational amplifiers) using only resistors and capacitors.

Producing graphs

There is a variety of frequency and time simulations that can be run to assess the filter performance, ranging from Bode plots to time domain response. All simulations ran very quickly, producing an output graph in about a second.

The graphing facility has a very nice zoom feature. With the aid of the mouse, a rectangle around the area of interest is selected on the graph. This area is then presented as the new graph. The procedure can then be repeated several times. A useful facility is that you can have the design target filter specification superposed on the graph of the frequency response simulation. In this way, you can see how and where the target is not met.

Graphs include phase and group delay as well as linear amplitude frequency response. Although the automatic scaling was generally good it failed to scale the phase response properly. However the automatic scaling can be overridden manually.

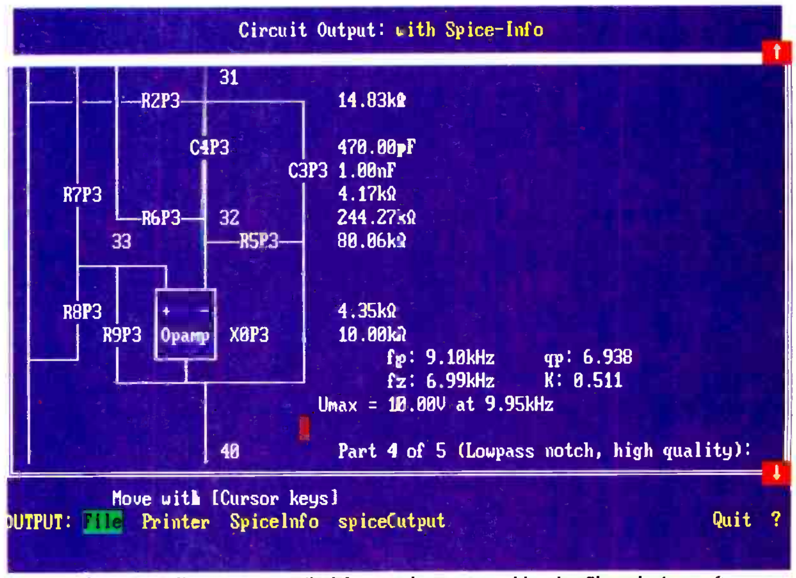
The hard copy section is really rather crude. One would expect a program of this price to at least present a comprehensive list of supported printers and plotters. Plotter output is HPGL, but with no pen selection. The printer output suits either an IBM dot matrix printer, non-IBM (presumably Epson) dot matrix printer, or PostScript. So if you use Laserjet or Ink jet printers you may have to invest in PostScript emulation.

A netlist for the filter design in ascii Spice form can be selected. The manual suggests that this will work with any Spice program but recommends the use of *IsSpice* – a version of Spice supplied by Intusoft.

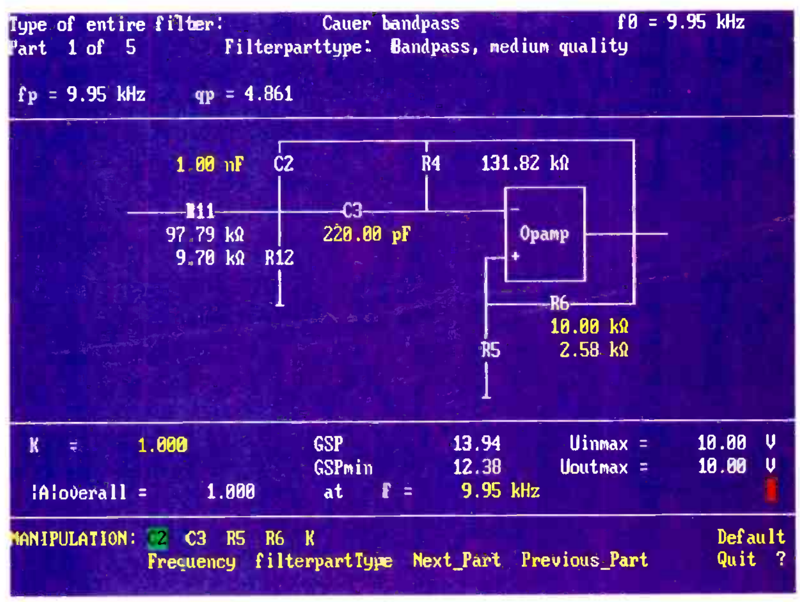
The difficult bits

For any filter design, tolerancing is one of the more difficult tasks. *Filter Master Active* does not provide any component tolerancing assistance. The only way in which this could be achieved is by using separate Spice modelling.

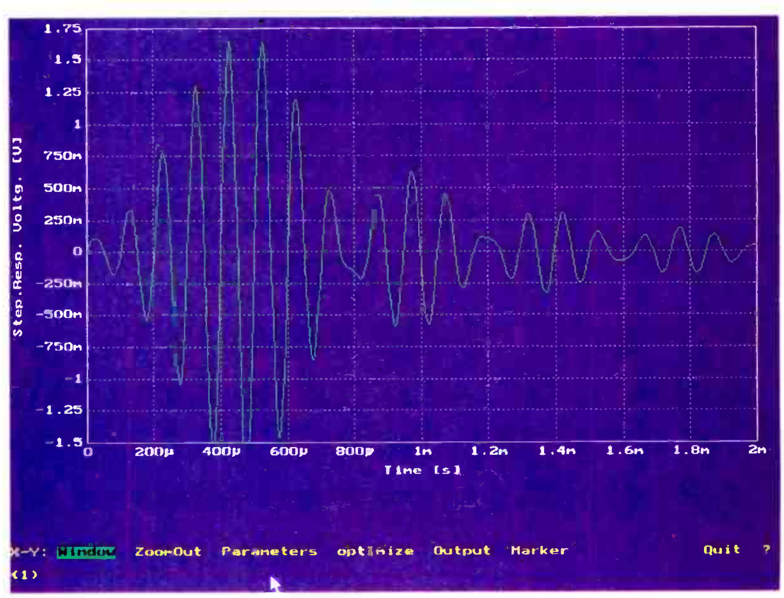
A similar problem exists for the effect of op-amp performance. Although the program allows specification of the op-amp, this is merely appended to the Spice file. No trimming of the filter components is provided to compensate. An example of this is presented in the



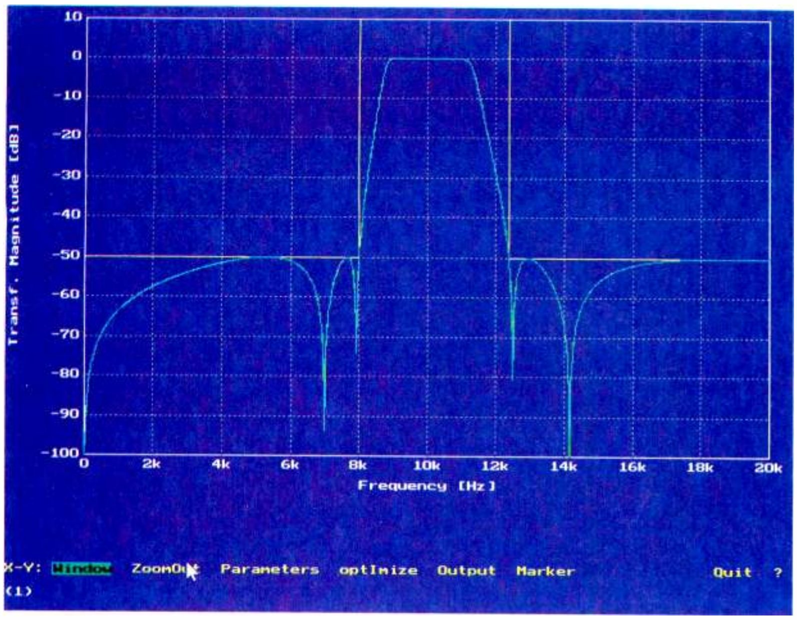
This crude circuit diagram, compiled from values created by the filter design software, is intended to provide an overview of the final circuit. Being based on text rather than graphical symbols however, it can be confusing.



Once the analogue filter is designed, you can tweak it by altering the values of individual components.



Graph display is usefully enhanced by the zoom function. With the aid of a mouse, the section of the curve to be zoomed is simply selected by pulling a rectangle around it.



Part of the package is a tutorial covering the design of a tenth-order Cauer filter which takes longer to specify than design.

applications sheet in the section dealing with interfacing with spice

Conclusions

This is a good product with good fundamental performance. The ability to synthesize and optimise filters quickly must improve productivity. If you need to design half a dozen non-canonic filters then the cost of the software will be easily repaid.

That said the whole program, although functional and robust, has a very crude feeling from the menu structure to the circuit drawing and printer support. Although the program does provide a spice interface, there is no netlist facility. This makes the transcription of the final design to schematic capture prone to error. But in the end these are user interface issues. In its encapsulation of filter design rules the program performs with distinction.

Further reading

The *Active Filter Design Book* by Moschytz and Horn, published by Wiley, provides a useful design guide for about £30. ■

SYSTEM REQUIREMENTS

PC with DOS 3.1 or later, 640K memory, 1.2Mbyte hard disc, optiona mouse, cga, ega, vga, ATT, MCGA or Hercules display, IBM dot matrix or PostScript printer, HPGL plotter, parallel port for dongle.

SUPPLIER DETAILS

At £610 plus £20 delivery, *Filter Master Active* is available from Technology Sources Ltd, Grove House Lodge, Falmouth Avenue, Newmarket, Suffolk. Tel. 0638 561460.

PC on a chip

Integration has now reached a level where it is possible to build a computer capable of out-performing the original PC-XT on a board with a credit-card footprint, as David Guest explains.

The embedded PC is not a new idea. Historically, the PC-XT was followed by the release of the *80188/80186*, which introduced the concept. Subsequently, NEC released the *V40* with an additional serial port and enhanced instruction set.

Register bank swapping and interrupt-driven macro services were introduced into the next generation – the *V25*, making the devices much more useful in real time systems. Finally, the later *V55* family comprised two processors, the PI and SC aimed at printer/fax applications and local area network (LAN) markets respectively.

Unlike the previously mentioned devices, the recently introduced PC-on-a-chip allows all the functions of a PC to be incorporated in embedded systems. This chip also takes advantage of PC user interfaces such as the keyboard and display, saving valuable development time.

Software tools for the embedded PC are inexpensive. Cross-compilers and emulators normally associated with micro-controller development are unnecessary. Software can easily be written easily on a high-level PC compiler,

Input/output system

The basic input/output system, or bios, has evolved with the PC. It has a well documented interface that isolates the operating system from the differences in the hardware of the system. It provides a power-on-self-test (post) initialising all of the peripherals in a well-defined sequence. First it configures the *8237* DMA and the *8253* timer chip to refresh dram. It then initialises a data field at 400_h to keep track of the hardware configuration. Next it sequences through the remaining peripherals.

Bios allows the dos operating system, and sometimes the compiler, to interface to the hardware via well-defined software interrupt calls. This is similar to the dos interface. Routines are called by the *8086* INT command with parameters being passed via the processor registers. For example, the following code would print the character "a" to the screen :

```
mov AH,02
mov DL, "a"
INT 21
```

The bios and dos calls are well documented in various text books.

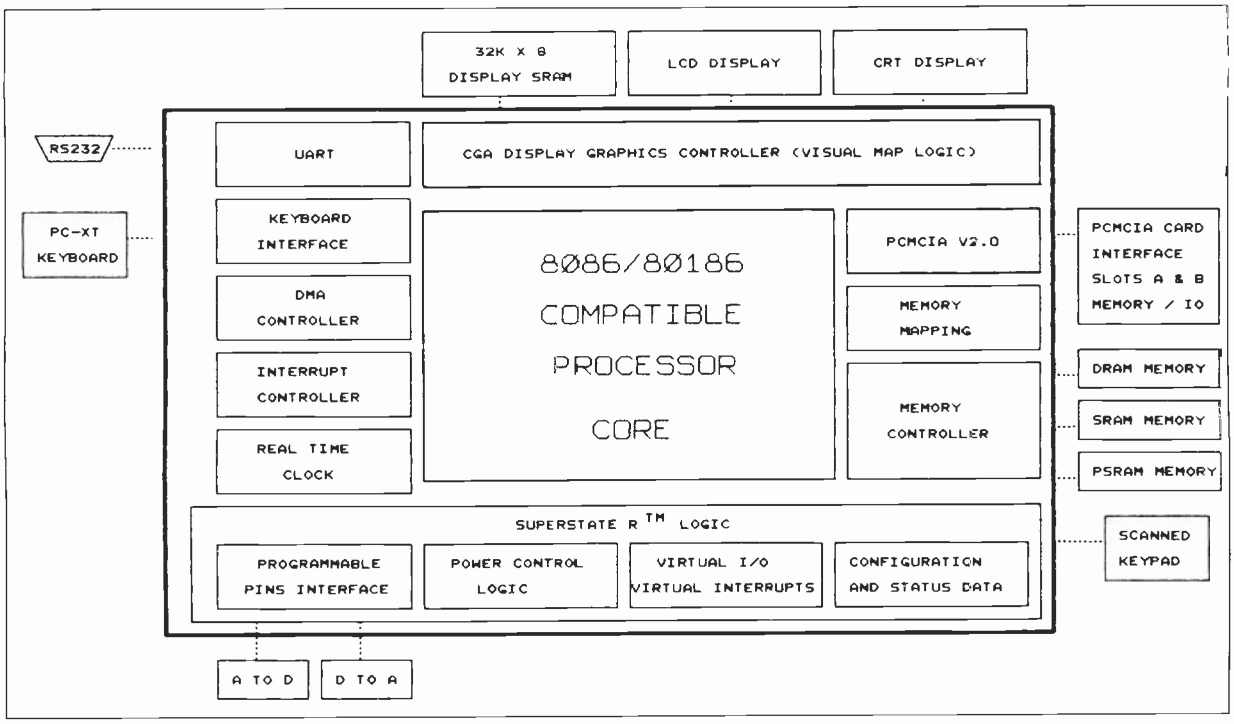


Fig. 1. PC features relevant to embedded peripherals are integrated into the F8680 PC-on-a-chip which is eight times faster than the original XT.

Original PC architecture progresses

In August 1981, IBM announced the first IBM Personal Computer based on the *8088*. Folowing a series of advances, the most significant of which was the launch of the *80286* in 1984, AT machines incorporating the new Intel *80386* processor, also called the *i386*, started shipping in 1987. Two versions existed, the SX with its cheaper external 16 bits bus and the DX with a full 32bit system. Now, the *80386* could support an enormous 4Gbyte of virtual memory. Its virtual *8086* mode supported multitasking software, notably Microsoft Windows, capable of running most dosbased software written for the *8086* and *80286* processors.

With its updated internal architecture, optimised instructions and higher clock speeds, the 16MHz *80386SX* was approximately fourteen times faster than the original XT. The higher system clock speeds associated with the 386 necessitated the use of special cache memory to realize its true performance.

The *80486* (or *i486)* chip is the logical successor to the more expensive top–end *80386* systems. The *80486* includes its own numerical co-processor with 8Kbyte of on-board cache. Its improved external bus supports burst mode, taking full advantage of the faster access modes of dram

Recently, the Pentium made its appearance. This is in fact the *80586*, but Intel decided in favour of a name rather than a number for copyright reasons. It boasts a 64bit data bus architecture with an internal architecture similar to two *i486s* in parallel.

Pentium has had mixed reviews in the press as its performance is hampered by the archaic PC architecture, and whether the performance justifies the extra expense is being debated. The recent introduction of "memory-hungry" *Windows NT* software is used as a stand alone operating system replacing dos, and brings Windows compatibility to computers based on other processors.

Two such computers claiming Workstation type performance are the *PowerPC* developed by Motorola and the *Alpha* chip developed by DEC. AMD is proposing *K5*, a hybrid RISC and CISC processor running PC software but technologically independent of Intel. Its performance would be equal to, if not if not better than, that of the *Pentium.*

such as Turbo C, Pascal or Basic. I prefer Turbo C. Its integrated environment and powerful debugging facilities substantially reduce software development time. Vast libraries for all the compilers are available. These provide windowed environments with a complex menu structure and with a multitude of input devices, such as keyboards, keypads and mice.

Two high-integration devices are currently on the market, providing all the architectural features of the AT computer. These are the *VG230* by Vadem or the *F8680* by Chips and Technologies. They have in common an interface for connecting directly to a PC keyboard, a CGA monitor with the option of driving an LCD graphics panel, and UART providing an RS232 serial port.

These ICs also support two PCMCIA 2.0 standard card-slot interfaces. Such cards make use of credit-card sized memory and I/O modules with a range of peripherals like modems, Ethernet, and hard-disk drives. Additionally, the Vadem has a built-in scanned keypad interface and a Centronics parallel port.

This article concentrates on the *F8680* PC-Chip for two reasons. Firstly it is readily available in small quantities without significant up-front costs. Secondly it is about half the price of its counterparts, at around £35 for small quantities.

Table 1. By far the strongest selling point of the F8680 PC-on a chip is its power management. In active mode a feature adding up to 127 cycles to the execution time of each instruction reduces memory accesses frequency and consequently current consumption.

Extra cycles	SRAM			DRAM		
	CHIP		RAM	CHIP		RAM
	5V	3V	5V	5V	3V	5V
0	46.7mA	34.8mA	26.2mA	50.2mA	38.4mA	65mA
127	16.6mA	14.9mA	1.3mA	23.9mA	15.7mA	16mA

Sram and dram current consumptions are based on six 128Kbyte chips and 256Kbyte SIMMs respectively, organised as three word wide banks of 256Kbyte.

Integrated PC-on-a-chip

The *F8680* PC-Chip, **Fig. 1**, is equivalent to an XT while containing all the peripherals associated with an AT. It runs software eight times faster than the original XT. This is twice as fast as the original AT, or approximately the same speed of a low end 16 MHz 386SX with slow dram and no cache. With over one hundred configuration registers, the *F8680* PC-chip provides more system features than a desktop PC. It is also optimised for use in battery powered systems.

Power management

By far the strongest selling point of the *F8680* PC-Chip is its power management facility. It places the device into a league of its own. Many of the chip's features are convenient but not essential. The power management however encompasses the complete system usefully reducing memory and external peripheral currents wherever possible.

The *F8680* PC-Chip is a static core device maintaining all its internal registers, even after stopping the processor clock. This allows it to operate from only 15μA, while still maintaining the real-time clock.

At pre-defined intervals the chip can be restored to full operation under control of the RTC or an external signal on the PWRUP pin. Operating the device at 3.3V reduces the current down even further to 5μA. Even when fully operational, the device only consumes around 40mA for an sram-based system to 75mA for one with dram.

When the system is active there is a fine-control feature adding up to 127 cycles to the execution time of each instruction. This reduces the frequency of memory accesses and, consequently, current consumption. Additionally, the chip itself uses less current, but the reduction is less significant, **Table 1**.

Access to power management is through a bios call ($1F_H$), making an easy-to-use software interface. Within the bios is a utility which assesses system activity and automatically controls the power management features to reduce the operating current of the system.

Memory management

On board, the PC-Chip has all the control and interface hardware for three banks of memory and system rom. It can drive dram memory directly, supplying both the multiplexed address lines and refresh cycle.

Each bank has an associated bank select register. Bank select registers, **Fig. 2**, define the memory cycle type, i.e. XT bus cycle, dram, sram or PCMCIA. They also define the memory size and its width, of either 8/16 bit. For CPU word transfers, the memory controller performs two accesses to byte wide memory.

There are two distinct mechanisms for controlling memory. Firstly, memory mapping maps the 16Mbyte of processor address space into physical memory, segmentable down to 32Kbyte. There can be 32 by 32Kbyte or 32 by 64Kbyte sections for the low end of memory with an additional two 512K or 1Mbyte sections for high end memory respectively.

Each of the 34 mapping registers contains two bits specifying the associated bank select register, which in turn defines the physical memory parameters. An additional three bits shift the location of the section on 128K boundaries, **Fig. 3**.

Bank switching is the second mechanism for controlling memory. It maps 16Kbyte, 32Kbyte, 64Kbyte blocks in segments D000, B000 and C000/E000/F000 respectively, **Fig. 4**. Therefore, available memory can be expanded below the 1MByte boundary imposed by dos (EMS).

When enabled, the bank switch supplies the upper address lines, giving access to the full 64Mbyte of address space. The PCMCIA interface uses the bank switching to access large amounts of memory, often used instead of disc drives.A full set of PCMCIA configuration registers supports two PCMCIA slots at revision 2.0. This revision is significant since it is the only one that has i/o features supporting a range of PCMCIA cards.

Additional registers allow even finer tuning of memory management, but the description of how is too lengthy for a magazine article.

i/o subsystem

All of the peripherals of the PC-XT in addition to the RTC normally associated with the PC-AT are contained in the i/o subsystem. Functions used within the XT architecture are implemented in hardware and SuperState R software. This association emulates the DMA subsystem and outperforms the standard DMA device.

Provision is also made for five multipurpose control pins which can be used for address decoding and for generating signals reflecting divisions of the 32kHz clock and processor status.

bios support

For a small royalty fee a fully configurable basic/input output system – bios – is available. Accompanied by a manual, the bios configuration utility adapts the bios to your own specific system requirements.

I will outline the more salient features. Firstly, the configuration software is interactive and gives a menu structure to all the modifiable system parameters. This can directly generate a binary image of the bios with the parameters and corresponding text file. The text file can be viewed and edited, and then read back into the configuration software.

To take advantage of the sophisticated power management facilities of the chip, the bios provides an automatic power saving mode. It also uses the battery backed ram associated with the real time clock to support a range of options. These can be modified via a built-in set-up screen when the system is active. This allows basic changes to the system parameters such as time and date and diskette type, which can be standard $5^1/_4$in, $3^1/_2$in or PCMCIA.

Additional external peripheral devices can be initialized by the bios, which is ideal for setting up intelligent

SuperState R

SuperState R logic is a hardware facility that intercepts all i/o transfers, interrupt and DMA requests. It supports a supervisory operating system which provides another level of hardware isolation below the bios This allows the interception of bios and dos calls. The chip uses such interception to simulate the real time clock with a simple 32 bit counter and other system functions.

Execute-in-place software

In small low powered systems, magnetic media are impractical. For this reason, roms are used for permanent data storage, so called rom-disks. As programs can be executed from rom, the rom disk introduces a new program format, XIP, which minimizes system ram requirements and reduces cost and power consumption.

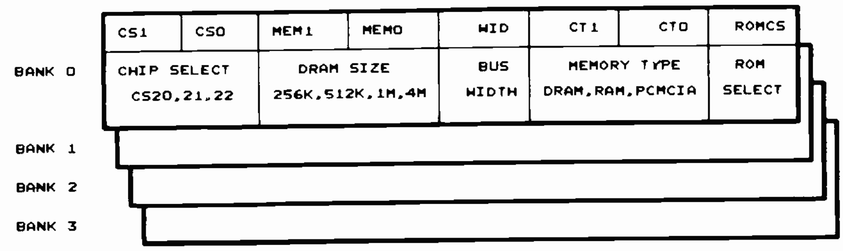


Fig. 2. Bank select registers add flexibility by allowing the memory cycle type to be defined. Choices are XT bus cycle, dram, sram or PCMCIA.

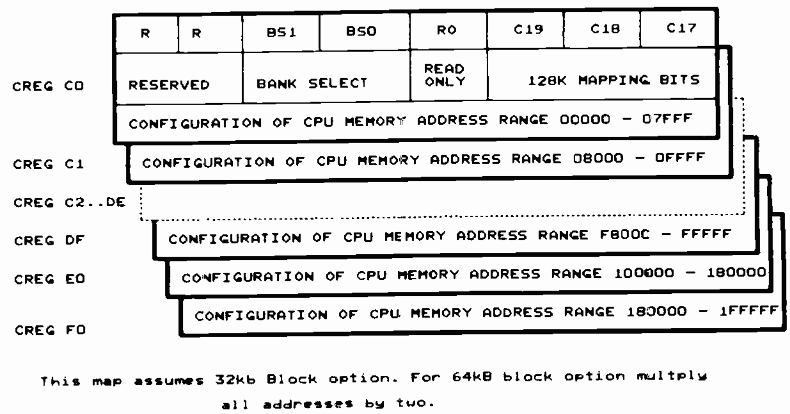
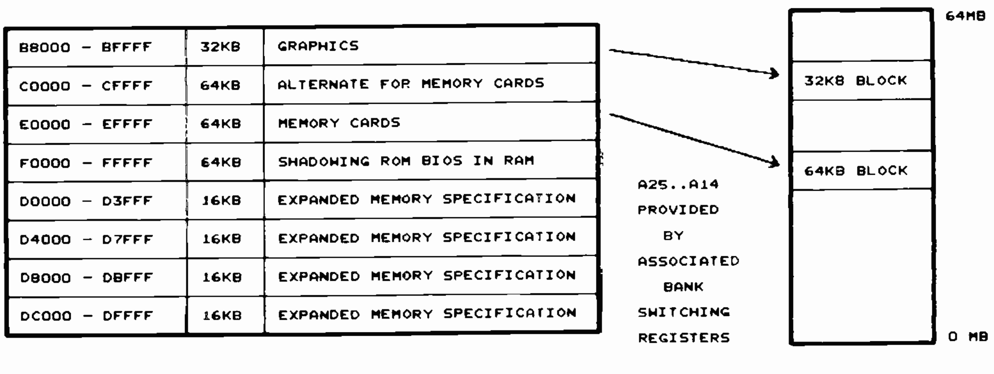


Fig. 3. Within the PC on a chip, memory mapping charts 16Mbyte of processor address space into physical memory, segmentable down to 32Kbyte.

Fig. 4. In addition to memory mapping, the PC on a chip has bank switch registers for mapping 16Kbyte, 32Kbyte, 64Kbyte blocks in different segments. In this way, available memory can be expanded below the 1MByte dos boundary.



external peripherals. Smaller LCD screens are supported and allow panning around the screen with specific keystrokes. This works well, except where the software generates menu bars across the top/bottom of the screen.

Eight or sixteen shades of grey can be displayed on an LCD module via the device's 'visual map' feature. Each shade is individually associated with any of the sixteen foreground and sixteen background colours available on a CGA monitor.

Further, a minibug utility is built into the bios which provides features similar to the standard debug utility. This allows interactive modification of memory and i/o, viewing of system registers and basic assembler/disassembler functions. It also supports single stepping through code and the addition of breakpoints.

Modification of SuperState R parameters is also possible via the debugger. To allow allows the use of keypads instead of an external PC type keyboard, the SuperState R feature provides a scanned keyboard facility. ■

DOS for embedded systems

The dos operating system provides the foundation necessary to run PC programs. PC programs come in two formats – executable files with the default extension .EXE, and command files with the extension .COM. Executable files have a header that informs dos of their memory requirements. dos will allocate the necessary memory and copy the program into memory.

Command files requires no memory allocation, and will load and run faster than the EXE files. However they can only be used for programs with less than 64K of memory. Both need dos for low level functions, such as reading a character from the keyboard or displaying characters to the VDU.

Standard dos includes numerous features that would not normally be appropriate for embedded systems. Some companies offer a cut-down version specifically adapted for such systems.

As far as I know, there are four systems providing a range of unique features, from the use of reduced memory to embedded debuggers. They are Promdos manufactured by Appcom, distributed by DSL, Rom-Dos manufactured by Datalite and distributed by Dex Dyne, MS dos 5 rom version manufactured by Microsoft, distributed by MMD and Embedded dos manufactured by General Software, distributed by Great Western Instruments.

Further reading

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Norton, P., *Inside the IBM PC*, 1986, Brady Books, New York.

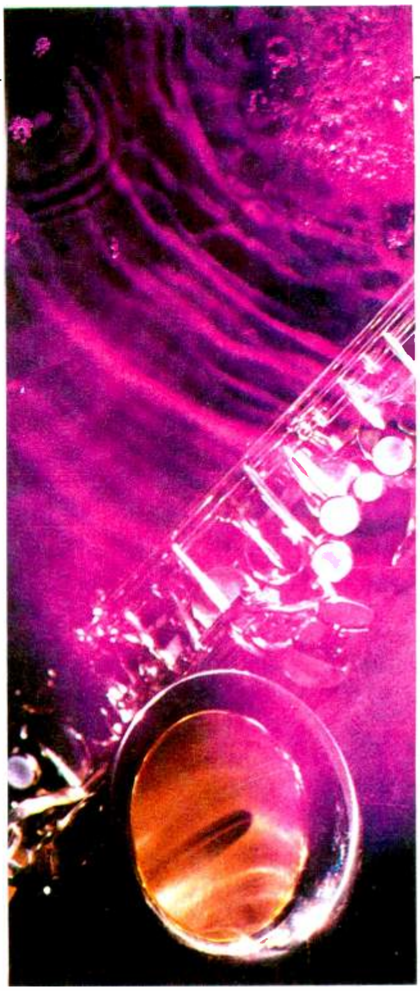
Reid, J., Newnes PC user's pocket book, 1991, Butterworth Heinemann, Oxford.

Sinclair, I., *Newnes 8086 family pocket book*, 1990, Butterworth Heinemann, Oxford.

Vadem VG-230 sub-notebook engine technical reference, Vadem, 1992, San Jose, California.

The previous article in this series dealt with several popular output stages, showing how their distortion could be attributed to three different mechanisms. This article examines ways of dealing with these shortcomings, and the effect of the distortion mechanisms on a closed loop output stage.

By Douglas Self.



Distortion in power amplifiers

5: output stages

From earlier work in this series, distortion from the small-signal stages may be kept to levels that will prove negligible compared with distortion from a closed-loop output stage. Similarly, future work in this series will show that distortion mechanisms 4 to 7 from my original list (*EW+WW, July 93*) can be effectively eliminated by lesser-known but straightforward methods. This leaves the third mechanism in its three components as the only distortion that is in any sense unavoidable: Class-B stages free from crossover artifacts are not exactly commonplace.

This is a good place to introduce the concept of a blameless amplifier, one designed so that all the easily-defeated distortion mechanisms have been rendered negligible. The word *blameless* has been carefully chosen to not imply perfection.

The first distortion, non-linearity in the input stage, cannot be totally eradicated but its onset can be pushed well above 20kHz. The second distortion, non-linearity in the voltage amplifier stage, can be effectively eliminated by cascoding. Distortion mechanisms four to seven, concerned with such things as earth return loops, power supply impedance and non-linear loading, can be made negligible by simple measures to be described later.

Large-signal distortion

The large-signal nonlinearity performance of all the bipolar junction transistor stages outlined in the previous part of this series have these features in common:

Large-signal nonlinearity increases as load impedance decreases. In a typical output stage loaded with 8Ω, closed-loop LSN is usually negligible, the THD residual being dominated by high-order crossover artefacts that are reduced less by negative feedback. At lower impedances, such as 4Ω, relatively pure third harmonic becomes obvious in the residual.

LSN worsens as the driver emitter or collector resistances are reduced, because the driver current swings are larger. On the other hand, this reduction improves output device turn-off, and will so decrease switchoff distortion: the usual compromise is around 47Ω to 100Ω.

The BJT output gain plots in the previous article reveal that the LSN is compressive, the voltage gain falling off with higher output currents. It is roughly symmetrical, generating third-harmonic, and is much greater at the very lowest load impedances: this is more of an issue now that 2Ω-capable (for a few minutes, anyway) amplifiers are considered macho, and some speaker designers are happy with 2Ω impedance troughs.

I suggest that the fundamental reason for this gain droop is the fall in output transistor beta as collector current increases, due to the onset of high level injection effects[1]. In the emitter follower topology, this fall in beta draws more output transistor base current from the driver emitter, pulling its gain down further from unity: this is the change in gain that affects the overall transfer ratio.

The output device gain is not directly affected, as beta does not appear in the classical expression for emitter follower gain, providing the source impedance is negligibly low. This assertion has been verified by altering an output stage simulated in Spice such that the output bases are driven directly from zero impedance voltage sources rather than drivers: this abolishes the gain droop effect, so it must be in the drivers rather than the output transistors.

Further evidence for this view is that in Spice simulation, the output device Ebers-Moll model can be altered so that beta does not drop with I_c (simply increase the value of the parameter IKF) and once more the gain droop does not occur, even with drivers. Here is one of the best uses of circuit simulation tweaking the untweakable. Gain droop does not affect fet outputs, which have no equivalent beta loss mechanism. See Fig. 12 of Part 4, where the wings of the fet gain plot do not turn downwards at large outputs.

It used to be commonplace for output transistors to be sold in pairs roughly matched for beta, allegedly to minimise distortion: this practice seems to have been abandoned. Simulation shows that beta mismatch produces an unbalanced gain droop that markedly increases low order harmonics without much effect on the higher ones. Modern amplifiers with adequate feedback factors will linearise this effectively. This appears to be why the practice has ceased.

Improving large signal linearity

It will be suggested that, in a closed loop blameless amplifier, the large signal nonlinearity contribution to total distortion (for 8Ω loading) is actually very small compared with that from crossover and switchoff. This is no longer true at 4Ω and still less so for lower load impedances. Thus ways of reducing this mechanism will still be useful.

The best precaution is to choose the most linear output topology; The previous article suggested that the open loop complementary

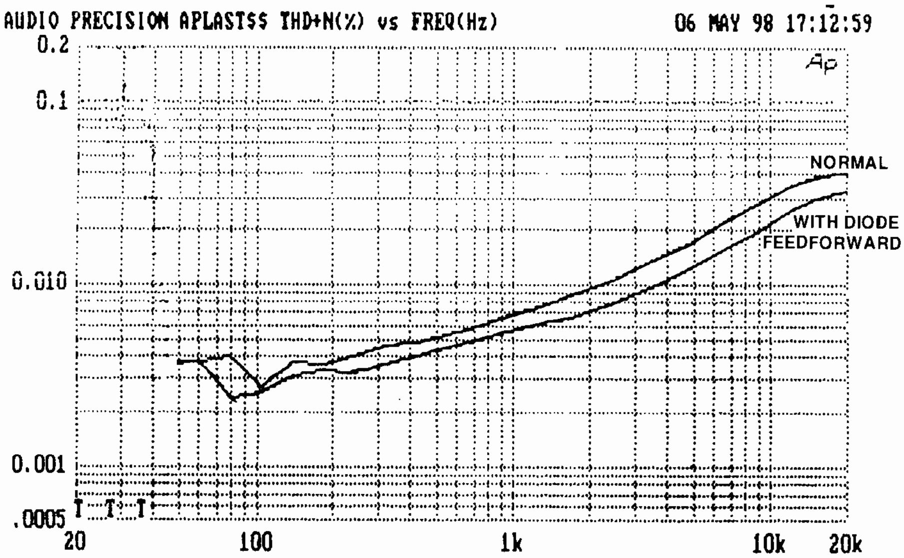


Fig. 1. Simple diode feedforward reduces distortion with sub-8Ω loads. Measured at 210W into 2.7Ω.

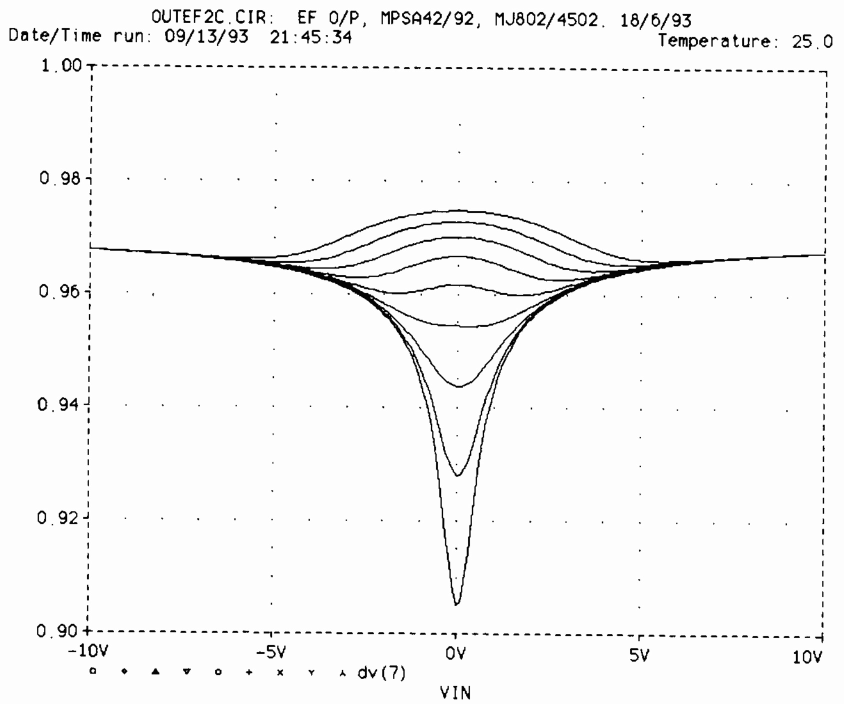


Fig. 2. Gain/output-voltage Spice plot for an emitter follower output shows how non-conjugate transistor characteristics at the crossover region cannot be blended into a flat line at any bias voltage setting. Bias varies 2.75 to 2.95V in 25mV steps, from too little to too much quiescent.

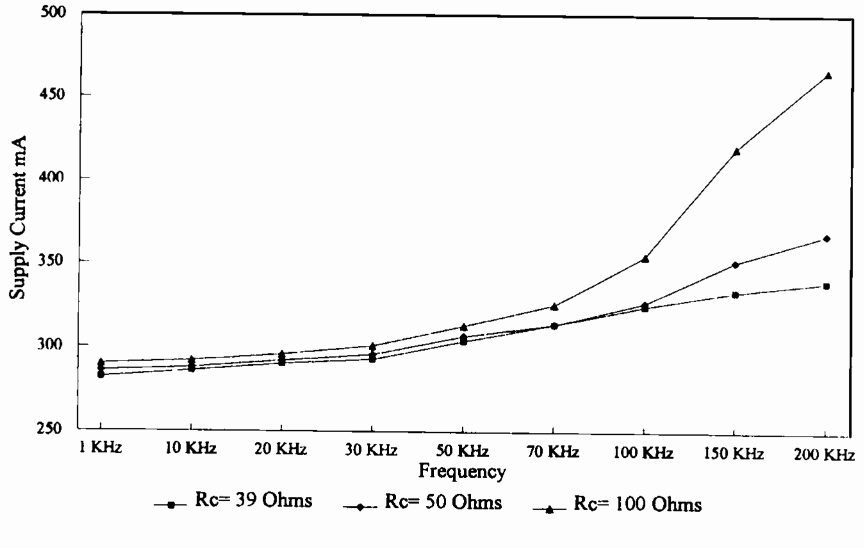


Fig. 3. Power supply current versus frequency, for a CFP output with the driver collector resistors varied. There is little to be gained from reducing Rc below 50Ω.

feedback pair output is at least twice as linear as its nearest competitor, (the emitter follower output) and so the CFP is usually the best choice unless the design emphasis is on minimising switchoff distortion.

In the small signal stages, we could virtually eliminate distortion. If the linearity of the input or voltage amplifier stage was inadequate, it was possible to come up with several ways in which it could be dramatically improved. A Class B output stage is a tougher proposition. In particular we must avoid complications to the forward path that lower the second amplifier pole P2, as this would reduce the amount of feedback that can be safely applied.

Several authors[2,3] have tried to show that the output emitter resistors of bipolar outputs can be fine tuned in value to minimise large signal distortion, the rationale being that the current dependent internal r_e of the output transistors will tend to cause the gain to rise at high currents, and that this gain variation can be minimised by appropriate choice of the external R_e. This is not true in practical output stages whose gain behaviour tends to be dominated by beta loss and its effect on the drivers. In any case the resistor values suggested are such tiny fractions of an ohm that quiescent stability would be perilous.

In real life the R_e of a CFP output stage can be varied between 0.5 and 0.2Ω without significantly affecting linearity; 0.22Ω is a good compromise between efficiency and stability.

The gain droop at high I_cs can be partly cancelled by a simple but effective feedforward mechanism. The emitter resistors R_e are shunted with silicon power diodes, which with typical circuit values will only conduct when 4 Ohm loads (or less) are driven. This causes a slight gain increase that works against the beta loss droop. The modest but dependable improvement can be seen in **Fig. 1**, measured with a 2.7Ω load.

If a 100W/8Ω amplifier is required to drive 4Ω loads then it will need paralleled output devices to cope with the power dissipation. Perhaps surprisingly, the paralleling of output BJTs (driven as usual from a single driver) has little effect on linearity, given elementary precautions to ensure current sharing. However, for the 2Ω case there is a definite linearity improvement on resorting to tripled output devices; this is consistent with the theory that LSN results from beta loss at high collector currents.

Crossover distortion

The worst problem in Class B is the crossover region, where control of the output voltage must be transferred from one device to another. Crossover distortion generates unpleasant high order harmonics with the potential to increase in percentage as signal level falls. There is a consensus that crossover caused the transistor sound of the 1960's, though to the best of my knowledge this has never actually been confirmed by the double blind testing of vintage equipment.

The V_{be}-I_c characteristic of a bipolar transistor is initially exponential, blending into linear as the emitter resistance R_e comes to dominate the transconductance. The usual Class B stage puts two of these curves back to back, and Peter Blomley has shown that these curves are non-conjugate[4], ie there is no way they can be rearranged to sum to a completely linear transfer characteristic, whatever the offset imposed by the bias voltage.

This can be demonstrated quickly and easily by Spice simulation; see **Fig. 2**. There is at first sight not much you can do except maintain the bias voltage, and hence quiescent current, at some optimal level for minimum gain deviation at crossover; quiescent current control is a topic that could fill a book in itself, and cannot be considered properly here.

It should be said that the crossover distortion levels generated in a blameless amplifier can be low up to around 1kHz, being barely visible in residual noise and only measurable with a spectrum analyser. For example, if a blameless closed-loop Class B amplifier is driven through a *TL072* unity gain buffer the added noise from this op-amp will usually submerge the 1kHz crossover artifacts into the noise floor. (It is most important to note that distortion mechanisms 4 to 7 create disturbances of the THD residual at the zero crossing point that can be easily mistaken for crossover distortion, but the actual mechanisms are quite different). However, the crossover distortion becomes obvious as the frequency increases, and the high order harmonics benefit less from NFB. See text panel *Improving crossover distortion*.

It will be seen later that in a blameless amplifier the linearity is dominated by crossover distortion, even with a well designed and optimally biased output stage. There is an obvious incentive to minimise it, but there seems no obvious way to reduce crossover gain deviations by tinkering with any of the relatively conventional stages considered so far. Significant improvement is only likely through application of one of the following techniques:

- The use of Class AB stages where the handover from one output device to the other is genuinely gradual, and not subject to the g_m doubling effects that an over biased Class B stage shows. One possibility is the so called Harmonic AB mode[5].
- Non-switching output stages where the output devices are clamped to prevent turn off, and thus hopefully avoiding the worst part of the V_{be}-I_c curve[6].
- Error correcting output stages implementing either error feedforward or error feedback. The latter is not the same thing as global NFB, being instead a form of cancellation[7].

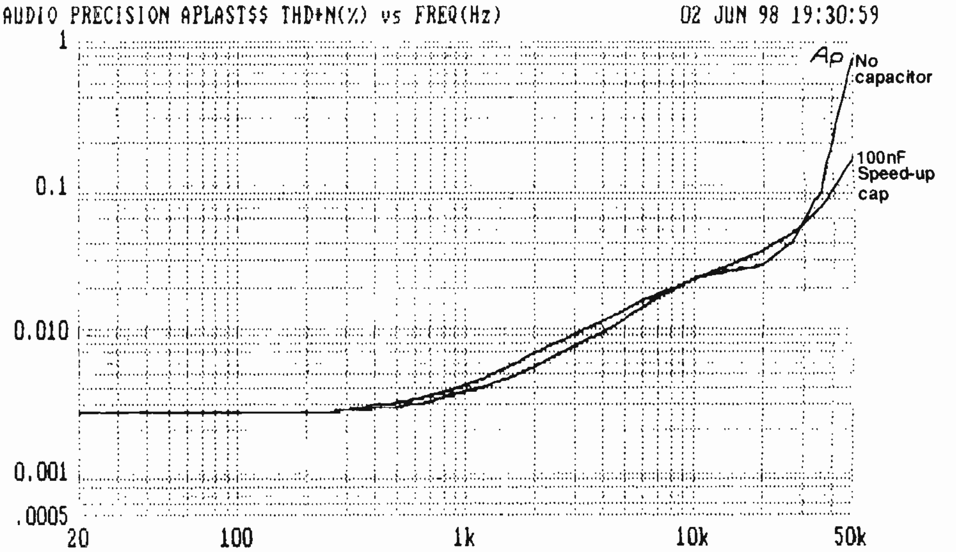


Fig. 4. HF THD reduction by adding speed-up capacitance across the common driver resistance of a Type II emitter follower output stage. Taken at 30W/8Ω

Once more, these will have to be examined in the future.

Switching distortion

This depends on several variables, notably the speed characteristics of the output devices and the output topology. Leaving aside the semiconductor physics and concentrating on the topology, the critical factor is whether or not the output stage can reverse bias the output device base emitter junctions to maximise the speed at which carriers are sucked out, so the device is turned off quickly.

The only conventional configuration that can reverse bias the output base emitter junctions is the emitter follower *type II*, described in the previous article. A second influence is the value of the driver emitter or collector resistors; the lower they are the faster the stored charge can be removed.

Applying these criteria can reduce HF distortion markedly, but it is equally important that it minimises output conduction overlap at high frequencies. If unchecked, overlap results in an inefficient – and potentially destructive – increase in supply current[8]. Illustrating this, **Fig. 3** shows current consumption vs frequency for varying driver collector resistance, for a CFP type output.

Figure 4 shows how HF THD is reduced by adding a speed-up capacitor over the common driver resistor of a *type II* emitter follower. At LF the difference is small, but at 40kHz THD is halved, indicating much cleaner switch-off. There is also a small benefit over the range 300Hz to 8kHz.

Selecting an output stage

Even if we stick to the most conventional of output stages, there are still an embarrassingly large number to choose from. The cost of a complementary pair of power fets is currently at least twice that of roughly equivalent BJTs, and taken with the poor linearity and low efficiency of these devices, the use of them may require a marketing rather than a technical motivation.

Turning to BJTs, and taking the material in this article with that in *Part 4*, I conclude that these are the following candidates for best output stage:

The emitter follower *type II* output stage is

The seven main sources of distortion

It is one of the central themes of this series that the primary sources of power amplifier distortion are sevenfold:

1. Nonlinearity in the input stage. For a well balanced differential pair distortion rises at 18dB/octave, and is 3rd harmonic. When unbalanced, HF distortion is higher and rises at 12dB/octave, being mostly 2nd harmonic.

2. Nonlinearity of the voltage amplifier stage (VAS), 2nd harmonic, rising at 6dB/octave.

3. Nonlinearity of the output stage. In Class B this may be a mix of large signal distortion and crossover effects, in general rising at 6dB/octave as the amount of NFB decreases; worsens with heavier loads.

4. Nonlinear loading of the VAS by the nonlinear input impedance of the output stage. Magnitude is essentially constant with frequency.

5. Nonlinearity caused by large rail decoupling capacitors feeding the distorted supply rail signals into the signal ground.

6. Nonlinearity caused by induction of Class B supply currents into the output, ground, or negative feedback lines.

7. Nonlinearity resulting from taking the NFB feed incorrectly.

the best at coping with switchoff distortion but the quiescent current stability is not of the best;

The CFP topology has good quiescent stability and low LSN; its worst drawback is that reverse biasing the output bases for fast switchoff is impossible without additional HT rails;

The quasi-complementary with Baxandall diode stage comes close to mimicking the emitter follower type stages in linearity, with a potential for cost saving on output devices. Quiescent stability is not as good as the CFP.

Closing the loop

In *Parts 2* and *3* of this series it was shown how relatively simple design rules could ensure that the THD of the small signal stages alone could be reduced to less than 0.001% across the audio band, in a repeatable fashion, and without using frightening amounts of negative feedback. Combining this subsystem with one of the more linear output stages such as the CFP version which gives 0.014% THD open loop, and having a feedback factor of at least 70 times across the band, it seems we have the ingredients for a virtually distortionless power amplifier, with THD below 0.001% from 10Hz to 20kHz. However, life is rarely so simple...

Fig. 5 shows the distortion performance of such a closed loop amplifier with an emitter follower output stage, **Fig. 6** showing the same with a CFP output stage. **Fig. 7** shows the THD of a quasi-complementary stage with Baxandall diode[9]. In each case distortion mechanisms 1, 2 and 4-7 have been eliminated by methods described in past and future sections of this series, to make the amplifier blameless.

It will be seen at once that these amplifiers are definitely not distortionless, though the performance is markedly superior to the usual run of hardware. THD in the LF region is very low, well below a noise floor of 0.0007%, and the usual rise below 100Hz is very small indeed. However, above 2kHz, THD rises with frequency at between 6 to 12 dB/octave, and the residual in this region is clearly time aligned with the crossover region, and consists of high order harmonics rather than second or third.

It is intriguing to note that the quasi-Bax output gives about the same HF THD as the emitter follower topology, confirming the statement that the addition of a Baxandall diode turns a conventional quasi-complementary stage with serious crossover asymmetry into a reasonable emulation of a complementary emitter follower stage.

Harmonic generation by crossover distortion

The usual nonlinear distortions generate most of their unwanted energy in low order harmonics that NFB can deal with effectively. However, crossover and switching distortions that warp only a small part of the output swing tend to push energy into high order harmonics, and this important process is demonstrated here, by Fourier analysis of a Spice waveform.

Take a sinewave fundamental, and treat the distortion as an added error signal *E*, letting the ratio *WR* describe the proportion of the cycle where $E>0$. If this error is a triangle wave extending over the whole cycle (*WR*=1) this would represent large signal nonlinearity, and **Fig. 9** shows that most of the harmonic energy goes into the 3rd and 5th harmonics; the even harmonics are all zero due to the symmetry of the waveform.

Fig. 10 shows how the situation is made more like crossover or switching distortion by squeezing the triangular error into the centre of the cycle so that its value is zero elsewhere; now $E>0$ for only half the cycle (denoted by *WR*= 0.5) and Fig. 9 shows that the even harmonics are no longer absent. As *WR* is further decreased, the energy is pushed into higher order harmonics, the amplitude of the lower harmonics falling.

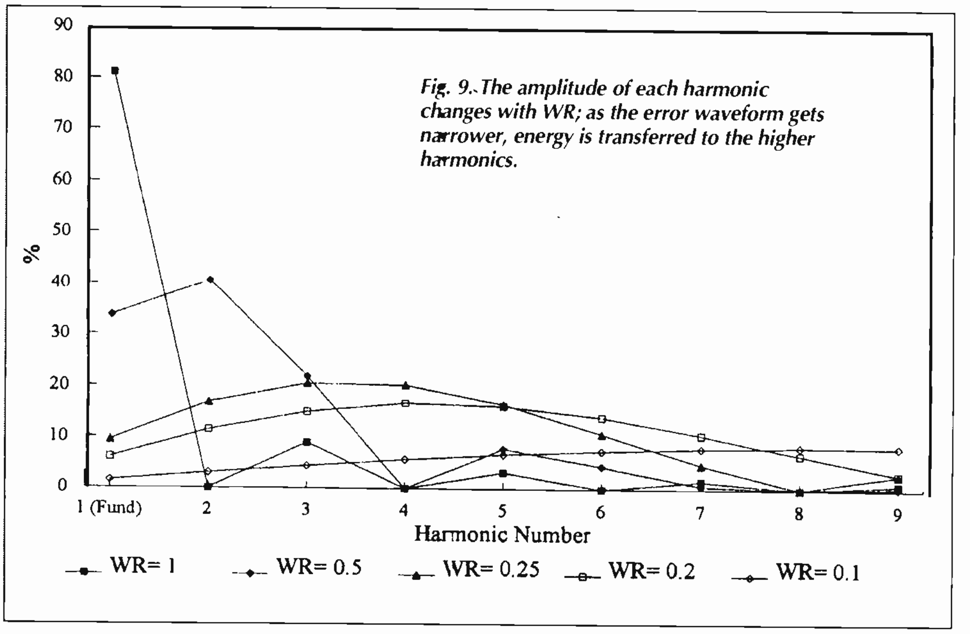


Fig. 9. The amplitude of each harmonic changes with WR; as the error waveform gets narrower, energy is transferred to the higher harmonics.

These high harmonics have roughly equal amplitude, spectrum analysis confirming that even in a blameless amplifier driven at 1kHz, harmonics are freely generated from the 7th to the 19th at a level within a dB or so. The 19th harmonic is only 10dB below the 3rd.

Thus, in an amplifier with crossover distortion, the order of the harmonics will decrease as signal amplitude reduces, and *WR* increases; their lower frequencies allow them to be better corrected by the frequency dependant negative feedback. This effect seems to work against the commonly assumed rise of percentage crossover distortion as level is reduced.

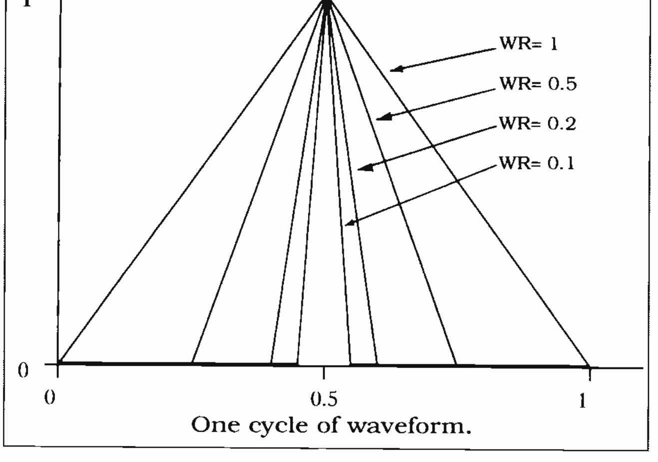


Fig. 10. Diagram of the error waveform E for some values of WR.

Table 1. summary of closed loop amp THD performance.

	1kHz	10kHz	
Emitter follower	0.0019%	0.013%	Fig. 5
CFP	0.0008%	0.005%	Fig. 6
Quasi Bax	0.0015%	0.015%	Fig. 7

AP plots in Figs 5 to 7 were taken at 100Wrms/8Ω, from an amplifier with an input error of –70dB at 10kHz and c/l gain of 27dB, giving a feedback factor of 43dB at this frequency. This is well above the dominant pole frequency, so the NFB factor is dropping at 6dB/octave and will be down to 37dB (or 70x) at 20kHz. My experience suggests that this is about as much NFB as is safe for general use, assuming an output inductor to improve stability with capacitive loads. Sadly, published data on this touchy topic seems non-existent.

There is significantly less HF THD with a CFP output; this cannot be due to large signal nonlinearity as this is negligible with an 8Ω load for all three stages, and must result from lower levels of high order crossover products.

Despite the promising ingredients, a distortionless amplifier has failed to materialise, so we had better find out why...

When an amplifier with a frequency dependent NFB factor produces distortion, the reduction is not due to the NFB factor at the fundamental frequency, but the amount available at the frequency of the harmonic in question.

A typical amplifier with open loop gain rolling off at 6dB/octave will be half as effective at reducing 4th-harmonic distortion as it is at reducing the second harmonic. LSN is largely third (and possibly second) harmonic, and so NFB will deal with this effectively. However, both crossover and switchoff distortions generate high-order harmonics significant up to at least the 19th and these receive much less linearisation. As the fundamental moves up in frequency the harmonics do too, and get even less feedback. This is the reason for the differentiated look to many distortion residuals; higher harmonics are emphasised at the rate of 6db/octave.

Here is a real example of the inability of NFB to cure all amplifier ills. To reduce this HF distortion we must reduce the crossover gain deviations of the output stage before closing the loop. There seems no obvious way to do this by minor modifications to any of the conventional output stages; we can only optimise the quiescent current.

Increasing the quiescent current will do no good for, as outlined in the previous article, Class AB is generally Not A Good Thing, producing more distortion than Class B, not less. **Fig. 8** makes this painfully clear for the closed-loop case; Class AB clearly gives the worst performance. (As before, the AB quiescent was set for 50:50 m/s ratio of the g_m doubling artefacts on the residual).

In this case the closed loop distortion is much greater than that from the small signal stages alone; however this is not automatic, and if the input pair is badly designed its HF distortion can easily exceed that caused by the output stage.

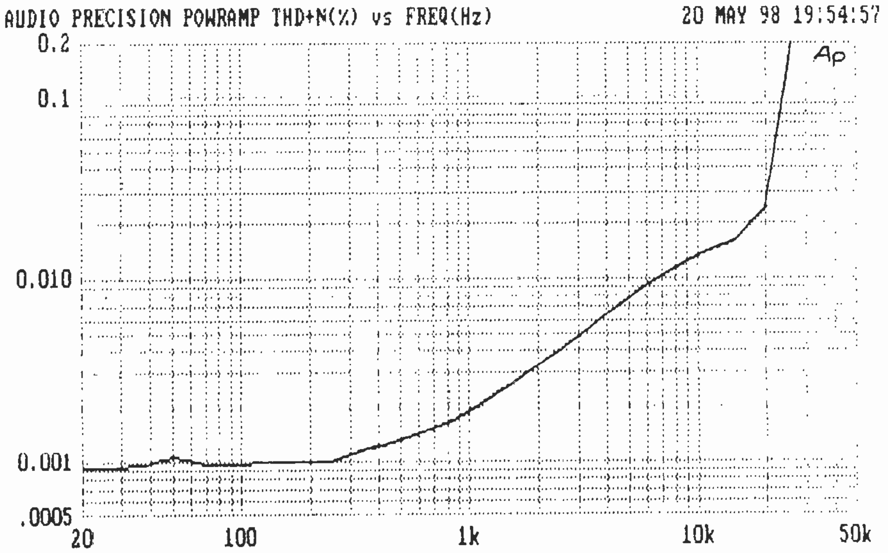


Fig. 5. Closed-loop amplifier performance with emitter follower output stage. 100W into 8Ω.

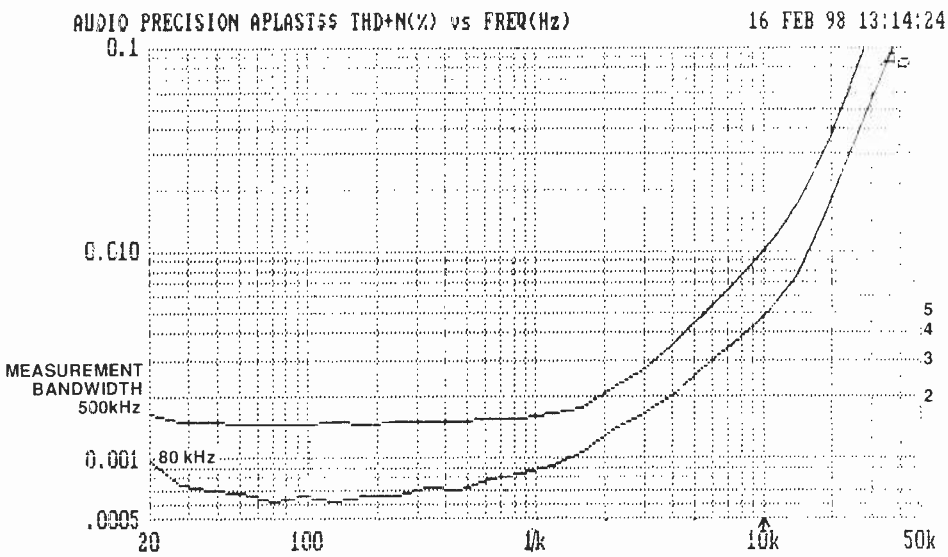


Fig. 6. Closed-loop amplifier performance with CFP output. 100W into 8Ω.

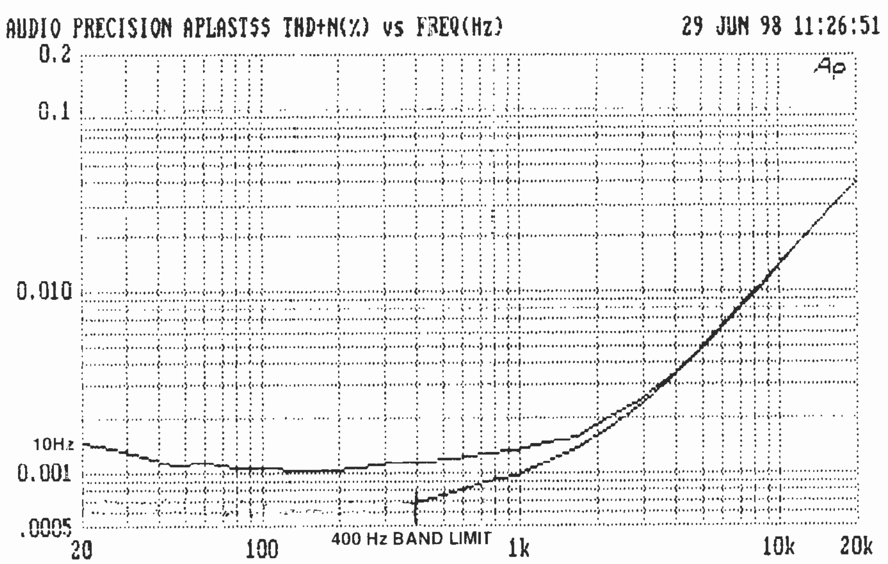


Fig. 7. Closed-loop amplifier performance; quasi-complementary output stage with Baxandall diode. 100W into 8Ω.

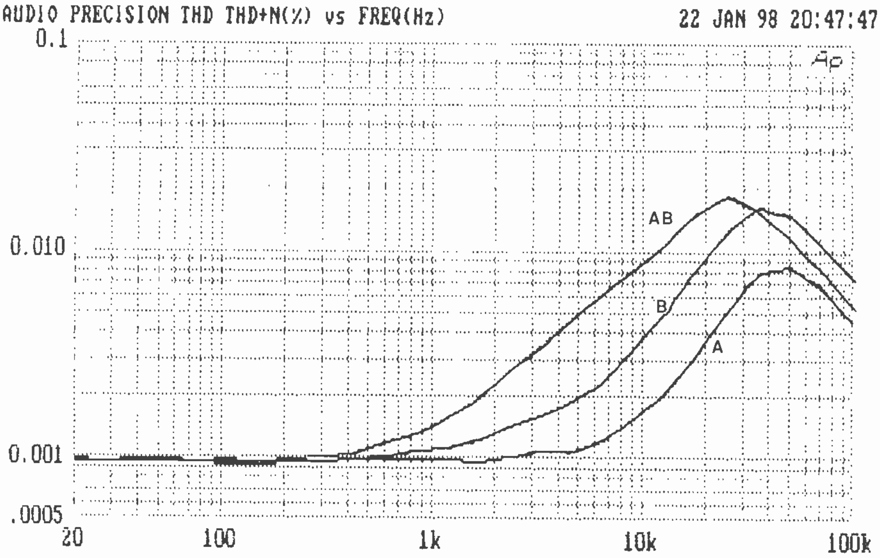


Fig. 8. Closed-loop CFP amp. Setting quiescent for Class AB gives more HF THD than either Class A or B.

The distortion figures given in this article are rather better than the usual run. I must emphasise that these are not freakish or unrepeatable figures. They are simply the result of attending to all seven of the major sources of distortion rather than just one or two. I have so far built 12 CFP amplifiers, and performance shows little variation.

Conclusions

Taking this and the previous article together, we can summarise. Class AB is best avoided. Use pure Class A or B, as AB will always have more distortion than either. Fet outputs offer freedom from some BJT problems, but in general have poorer linearity, lower efficiency, and cost more.

Distortion generated by a blameless amplifier driving an 8Ω load is almost entirely due to crossover effects and switching distortion. This does not hold for 4Ω or lower loads where third harmonic on the residual shows the presence of large signal nonlinearity caused by beta loss at high output currents. ■

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Working with programmable logic

2 : sequential logic

In combinatorial logic circuits, the order in which signals are applied makes no difference to the end result, once propagation delays have worked through. The converse is true with sequential logic.

There is usually a trigger signal, called the clock, which controls the passing of data from inputs to outputs. The triggering event is often the low to high transition of the clock input, and the state of the inputs at this moment (and a few nanoseconds before and after) determines what state the outputs will take immediately after the active clock edge. Any changes of input levels away from the active clock edge will not affect the output.

If the outputs are fed back, so that they form part of the input to the device, the result is a state machine. A typical state machine is shown in **Fig. 1**. The output state is held in a set of flip-flops called a register; the same clock is shared by all the flip-flops so that data is loaded into each one simultaneously. The core of the machine is still combinatorial logic but, even if the output of the core logic changes, the output register will not be altered until the active clock edge.

Many practical systems can be defined as state machines. Consider something as common as a lift (or elevator). In a three storey building, a lift can have seven possible states (see **Fig. 2**): it can be stationary at a floor, or in transit between any two of the floors, moving up or down. If it is stationary it will only move if it is called to another floor; if it is moving it will only stop if it has been called to the floor which it is approaching, unless that happens to be the top or bottom.

It may appear as if there is no clock in operation, but a system like this will use a clock to sample the state of the call buttons and lift position. These signals form the inputs to the system; the outputs will act as signals to the lift motor and brake, but will also be fed back as inputs so that the logic knows what the lift is doing.

For example, a call to floor three would be ignored if the lift was descending between floors two and one, but it would be acted on if the lift was stationary at floor two or one.

Note that a practical system would require several auxiliary circuits. For example, some prioritising of the call signals to prevent hogging and a time delay for the door opening and closing, but this does not alter the principles involved.

Registered proms

A standard prom can behave as a combinatorial logic circuit, so a circuit capable of supporting state machines can be made by adding an internal register. Because state information must be logically combined with input data, some of the prom outputs need to be connected back to the

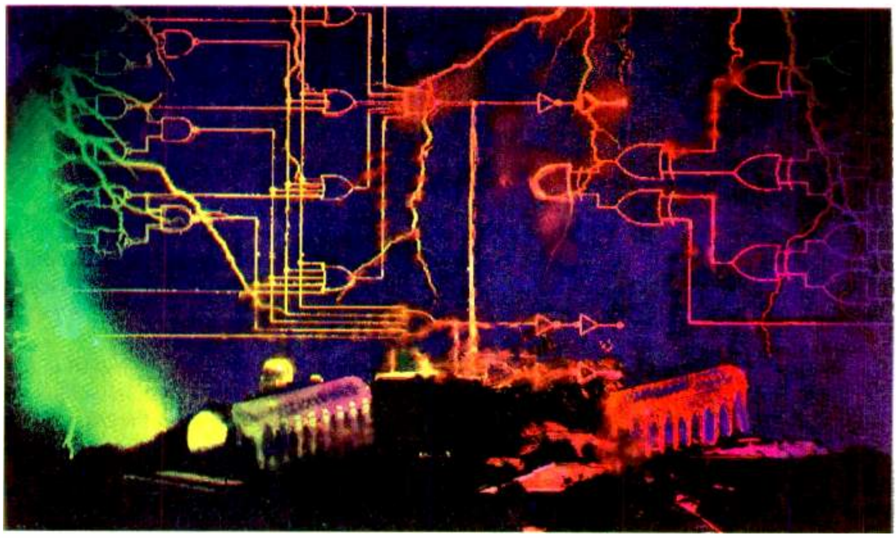


Illustration TRACY MARTIN

Registered functions, and state machines in particular, can fit into registered proms, registered PALs or FPLSs. Of these, FPLSs are versatile but also expensive and power hungry. As with combinatorial logic, each application needs to be decided on its merits. Geoff Bostock explains the ground rules.

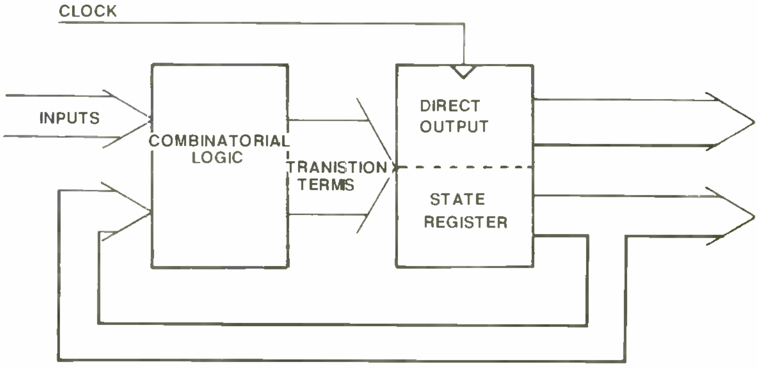


Fig. 1. Basic state machine block diagram.

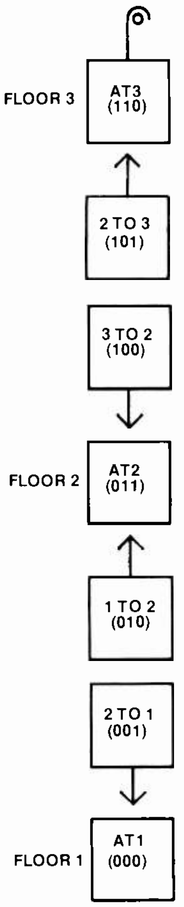


Fig. 2. Three-floor lift – basic states.

inputs. This has the effect of restricting the number of inputs available for logic connection.

Figure 3 shows how a 16K (2K x 8) registered prom could be connected to control the lift example described above. The seven states can be defined in three state bits; this leaves eight inputs free for inputs to control the lift. Some obvious inputs would be the call signals to the three floors and, perhaps, a door open indicator and emergency stop. It would also be sensible to include signals to indicate when each floor has been reached, in order to allow the lift to be stopped and the door opened.

There are also five outputs free. Possible uses for these could include signals to operate the lift motor, the door motor and one for the brake.

This configuration will just fit into a 16K prom but, as with combinatorial circuits, addition of another input would require a prom of twice the size to accommodate it. Moreover, two more states (ie nine altogether) would need another input and output because four state bits are required to define from nine to sixteen states.

Nevertheless, registered proms are available up to 64K in size and may be used for state machines. Indeed, Cypress has just brought out two proms specifically aimed at state machine applications. The *CY7C258* and *CY7C259* have internal feedback paths from some outputs to the input side of the prom array. Here they are multiplexed with address lines, giving the designer the option of choosing the width of the fed back state word. Each prom has a 16-bit wide output, although only eight are available in the *CY7C258*, and an 11-bit input with up to 11 output bits fed back.

The lift example, as described above, would just fit into one of these proms, so let us see how the system would be defined. **Fig. 4a** shows the state diagram for the lift controller. The seven states are defined as in Fig. 2, together with the values of `B2`, `B1` and `B0` for each state, while the arrows show the possible transitions between each state, together with the logic conditions which trigger the transition. Some way is needed to translate this diagram into a format that a PLD assembler will recognise.

This usually takes the form of state equations; the equations, which are equivalent to the state diagram, are shown in **Fig. 4b**. Conventionally, states are enclosed in square brackets; thus, `[AT3]` means state **AT3**. The `WHILE [S1] IF T1 THEN [S2] WITH O1` format is straightforward; `S1` is the present state of the system, `T1` is the logic condition which triggers a jump to state `S2`, while `O1` is the condition of the outputs in state `S2`.

The states and logic conditions must be defined separately, often by means of logic equations. For example, we could define `[AT3]` by:

`[AT3] = B2 & B1 & !B0,`

or as a number by `[AT3] = 6h` or `[AT3] = 110b`, in hexadecimal or binary respectively; the exact format

Fig. 4b. State equations for three-floor lift controller.

```
WHILE [AT3]
   IF !STOP & !DOOR OPEN & (CALL1 # CALL2) THEN [3TO2] WITH DOWN & CLOSE_DOOR

WHILE [3TO2]
   IF FLOOR2 & CALL2 THEN [AT2] WITH BRAKE & OPEN_DOOR
   IF !DOOR_OPEN & !STOP & CALL1 & !CALL2 & FLOOR2 THEN [2TO1]

WHILE [2TO3]
   IF FLOOR3 & CALL3 THEN [AT3] WITH BRAKE & OPEN_DOOR

WHILE [AT2]
   IF !DOOR_OPEN & !STOP & CALL3 THEN [2TO3] WITH UP & CLOSE_DOOR
   IF !DOOR_OPEN & !STOP & CALL1 THEN [2TO1] WITH DOWN & CLOSE_DOOR

WHILE [2TO1]
   IF FLOOR1 & CALL1 THEN [AT1] WITH BRAKE & OPEN_DOOR

WHILE [1TO2]
   IF FLOOR2 & CALL2 THEN [AT2] WITH BRAKE & OPEN_DOOR
   IF !DOOR_OPEN & !STOP & CALL3 & !CALL2 & FLOOR2 THEN [2TO3]

WHILE [AT1]
   IF !DOOR_OPEN & !STOP & (CALL2 # CALL3) THEN [1TO2] WITH UP & CLOSE_DOOR
```

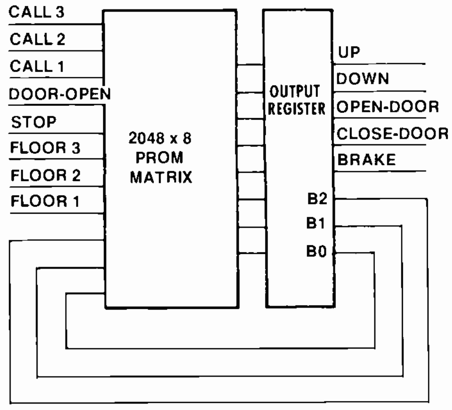


Fig. 3. 16K registered prom block diagram – wired as lift controller.

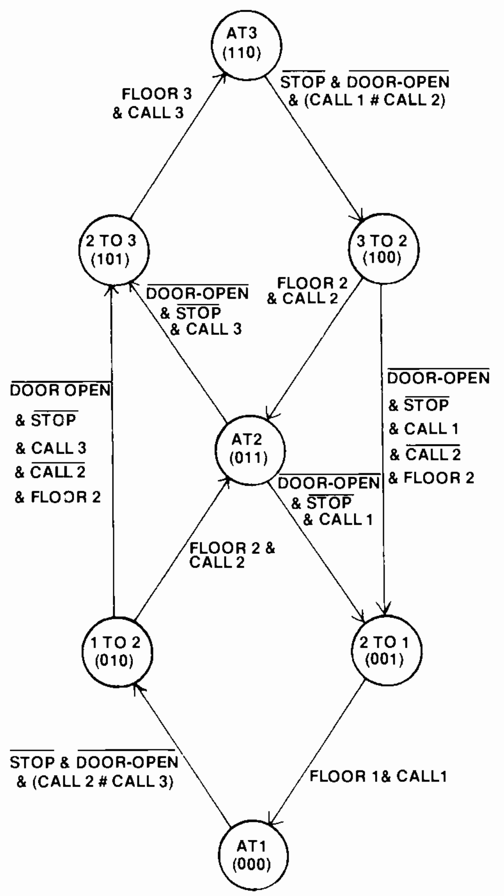


Fig. 4a. State diagram for three-floor lift controller.

The first step in building a state machine is to draw the state diagram of the system. Fig. 4a is the state diagram of a simplified controller for a lift operating between three floors. In a state machine, the state information is held in a set of flip-flops called the state register. Each state in the state diagram must be uniquely numbered so that correspondence can be established between the register and the diagram.

Transitions between states are shown on the diagram as arrows; each arrow is labelled with the logic function which must be true for the transition to occur. This is the transition condition for the jump, which will take place at the active edge of the common clock driving the state register.

To program a PLD with this data it must be converted to a format which will be recognised by a PLD logic assembler. A common format is the WHILE [..] IF ... THEN [..] WITH ... notation. The WHILE operator refers to the present state, the IF argument is the transition condition, THEN gives the next state and WITH defines any output which may be associated with the next state. The state equations derived from figure 4a are shown in Fig. 4b.

depends on which logic formatter is being used.

To complete this example the `door_close` and emergency stop signals must be defined. `Door_close` happens automatically when a call button is pressed and the door is open, although in a practical system there would be some delay after the lift reached a floor to allow passengers time to leave or enter the lift. It is defined by the equation:

```
CLOSE_DOOR := DOOR_OPEN & (CALL3 # CALL2 #
CALL1)
```

Here the symbol ':=' means equals at the active clock edge.

Similarly we can write an equation:

```
BRAKE := STOP # AT3 # AT2 # AT1
```

implying that the brakes are applied when the emergency stop button is hit or when the lift is stopped at one of the floors. Note that this notation means that the brakes will only be applied as long as the stop signal is active. This is because the register is made from D-type flip-flops, which do not hold their data once an input is removed, unlike J-K flip-flops.

Registered PALs

Registered proms suffer from the same drawbacks as combinatorial proms, the chief one being that an extra input requires a doubling of array size. This can be particularly irksome in state machines whose arrays have several inputs allocated to fed back outputs. As with combinatorial logic, the simplest solution is to make the and-array programmable; if the or-array is fixed the result is a PAL structure.

The circuit diagram of a basic registered PAL output is shown in **Fig. 5**. The registered output passes through an inverting three state buffer, but the feedback to the and-array is taken directly from the inverting output of the flip-flop. Even when the outputs are switched off the feedback is still operating. Both output and feedback are inverted, so registered PALs are effectively active-low, meaning that care must be taken over the way in which transition terms trigger state bit changes.

As with proms, D-type flip-flops are used to form the state register. Any state bit which should not change when the transition condition is removed must, therefore, be provided with a separate product term defining the 'hold' condition. We can illustrate this with a simple binary counter example.

The least significant bit always toggles when the counter is counting. It may be defined very simply by:

```
Q0 := !Q0 & COUNT
```

The next bit (`Q1`) toggles only when `Q0` is high; this might be defined by:

```
Q1 := !Q1 & Q0 & COUNT
```

This definition will cause `Q1` to go low whenever the transition condition (`!Q1 & Q0 & COUNT`) is not true, but we want `Q1` to remain high when `Q1` is high and `Q0` is low: that is counting from two to three. We also want `Q1` to stay high if `COUNT` goes low, and the count is halted temporarily. To do this we must add terms to that effect, so the complete equation for `Q1` becomes:

```
Q1 := !Q1 & Q0 & COUNT
   # Q1 & !Q0 & COUNT
   # Q1 & !COUNT
```

If we investigate adding a third counter bit we find that the situation becomes even worse. `Q2` will toggle low to high on the three to four transition, but must be held high on the next three counts, four, five and six. These three present states need two product terms to cover them: `Q2` is fully defined by:

```
Q2 := !Q2 & Q1 & Q0 & COUNT (toggle at 3 or 7)
   # Q2 & !Q1 & COUNT (hold high at 4 or 5)
   # Q2 & !Q0 & COUNT (hold high at 4 or 6)
   # Q2 & !COUNT (hold high interrupted count)
```

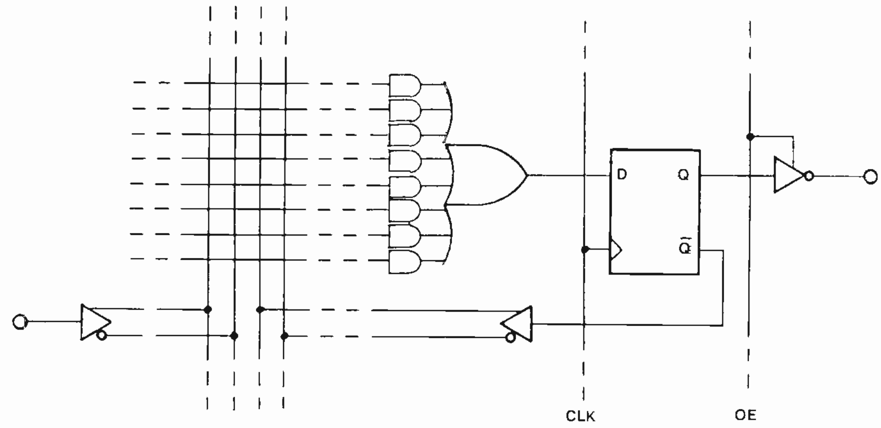


Fig. 5. One output of a standard registered PAL.

Every higher bit we count needs an additional product term to define the hold while counting condition. As we shall see, standard registered PALs contain just eight product terms per output, so the `Q6` output would use all the product terms available to it.

Fig. 6 shows the Karnaugh map for `Q2`. From this it may be deduced that `Q2` can be written:

```
Q2 := Q2 :#: Q1 & Q0 & COUNT
```

		0	0	1	1	COUNT
		0	1	1	0	Q2
0	0		H	H		
0	1		H	H		
1	1		H		H	
1	0		H	H		
Q1	Q0					

Fig. 6. Karnaugh map for third bit of a binary counter.

A registered output, such as that shown in **Fig. 7**, can cope with any order bit in a counter chain because the exclusive-or gate allows equations like this to be programmed directly into the PAL.

The standard families of registered PAL are based on the 20 pin combinatorial *PAL16L8* and 24 pin *PAL20L8*. In each case a series of PALs is available with registered outputs of the form of Fig. 5 replacing four, six or all eight of the combinatorial outputs. These make the *PAL16R4*, *PAL16R6* and *PAL16R8* from the *PAL16L8*, and *PAL20R4*, *PAL20R6* and *PAL20R8* from the *PAL20L8*.

A third family has been created by replacing four, eight or ten of the PAL20L10 combinatorial outputs by exclusive-OR registered outputs, as in Fig. 7. These are the *PAL20X4*, PAL20X8 and PAL20X10. Their principal use is in making counters; up to divide-by-1024 can be incorporated into the *PAL20X10*.

The *PAL16Rn* and *PAL20Rn* families may be used for making small state machines, but are limited by having only eight product terms per output, and by the need to include terms to hold the output high, as we saw with the basic counter. They are also useful in applications where synchronisation is required, when they can be considered merely as a combinatorial logic block driving a synchronising register.

Field programmable logic sequencers

Just as registered proms and PALs are derived from their combinatorial counterparts, so FPLSs are derived from

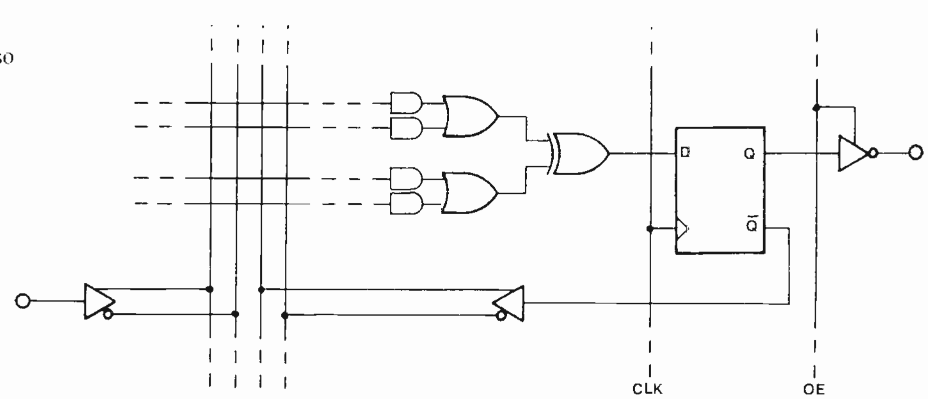


Fig. 7. One output of an exclusive-or registered PAL.

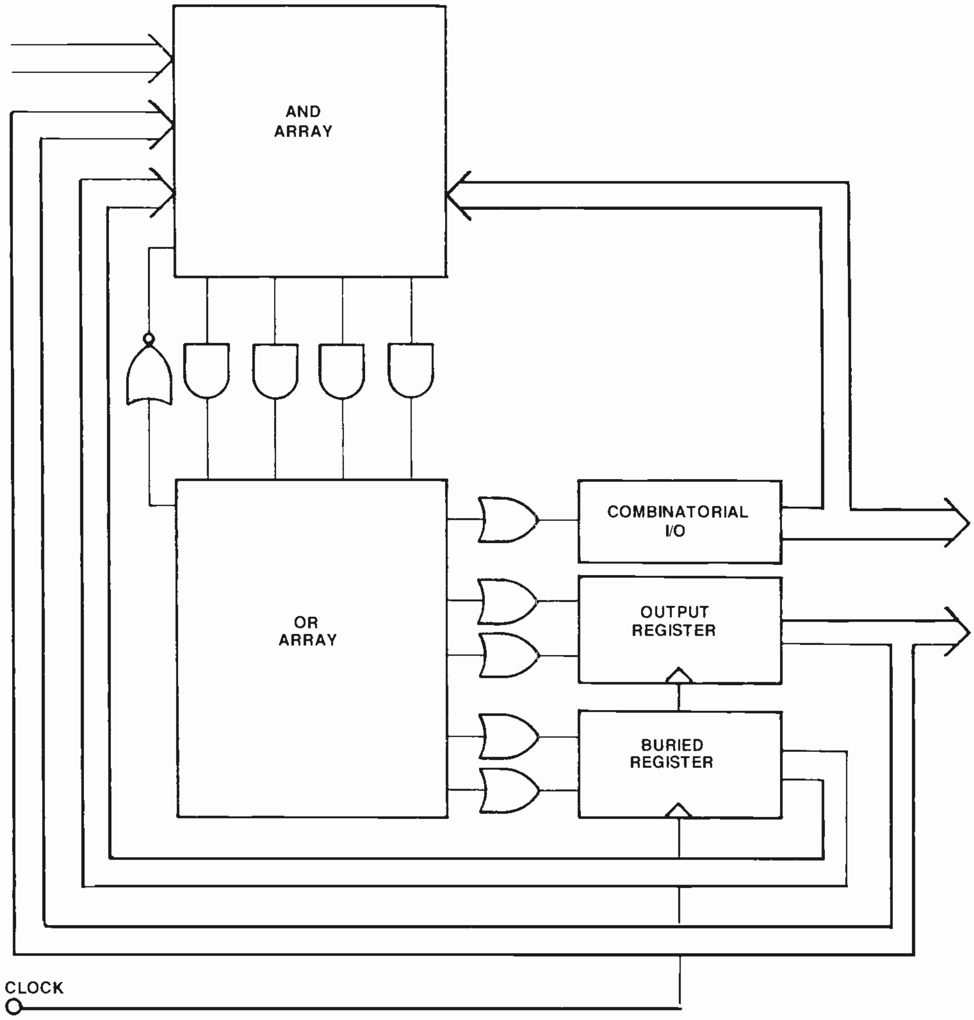


Fig. 8. Field programmable logic sequencer (FPLS) block diagram.

Fig. 9a, below left, state diagram of a priority controller for lift calls.

Fig. 9b, below right, state table of a priority controller for lift calls. FPLS programmers can accept state transition data in a state table format. This makes it unnecessary to use a logic assembler. Each present state is coded into the table, just as in an FPLA truth table, and the transition condition and next state entered on the same line. If there is more than one transition from any state then each transition must occupy a separate line, but the order in which lines are entered is unimportant except for readability. This table is the state table derived from the state diagram of Fig. 9a.

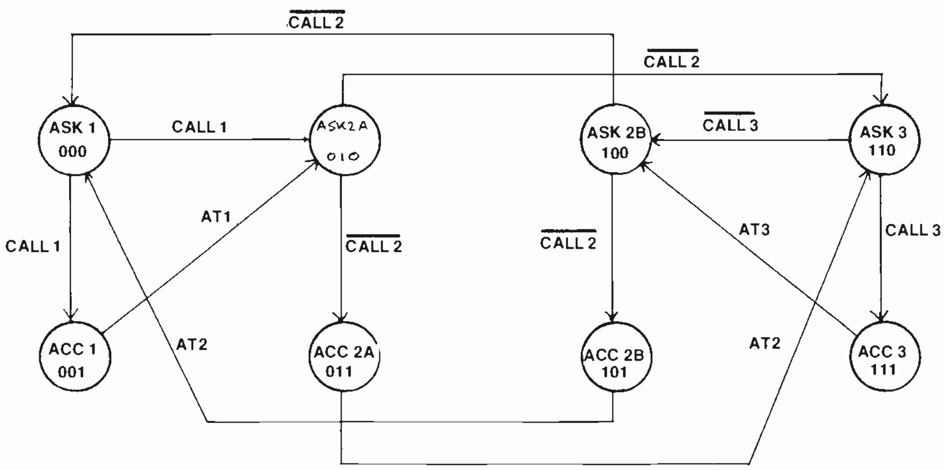
FPLAs. **Figure 8** shows a very general FPLS architecture; not all FPLSs have all the features shown in this diagram. Because the principal use of FPLSs is in building state machines, I will describe their architecture while bearing this in mind.

The state of the FPLS before the next active clock edge is called the present state, and this data is held in the buried register and/or the output register. The present state is fed back to the and-array where it is logically combined with input data. If the combination of feedback and input has been programmed into the FPLS as a valid transition condition, the appropriate product term will be high and will be fed into the or-array.

FPLSs use either R-S or J-K flip-flops as their register elements. Unlike D-types, once a high or low is established it will remain until the flip-flop is actively changed. A high from the and-array can be transmitted via programmable connections to or-terms feeding the flip-flop inputs. At the active clock edge these flip-flops will be set or reset, while any not receiving a high will remain unchanged. In this way a new present state is asserted.

If the feedback/input combination does not form a valid transition condition all the flip-flop inputs will be low when clocked, and the state of the register will remain unchanged.

As an example of how an FPLS can be used for a simple state machine, let us construct a priority control circuit for the three floor lift. The state diagram is shown in **Fig. 9a**. The state machine interrogates each call signal in turn and accepts the call if the signal is high. Floor 2 is given extra priority as it makes sense not to by-pass this floor if the lift is moving from one to three or *vice versa*. The diagram is



INPUTS						PRESENT STATE			NEXT STATE		
CALL 1	CALL 2	CALL 3	AT 1	AT 2	AT 3	S2	S1	S0	S2	S1	S0
H	-	-	-	-	-	L	L	L	L	L	H
L	-	-	-	-	-	L	L	L	L	H	L
-	-	-	H	-	-	L	L	H	L	H	L
-	H	-	-	-	-	L	H	L	L	H	H
-	L	-	-	-	-	L	H	L	H	H	L
-	-	-	-	H	-	L	H	H	H	H	L
-	-	H	-	-	-	H	H	L	H	H	H
-	-	L	-	-	-	H	H	L	H	L	L
-	-	-	-	-	H	H	H	H	H	L	L
-	H	-	-	-	-	H	L	L	H	L	H
-	L	-	-	-	-	H	L	L	L	L	L
-	-	-	-	H	-	H	L	H	L	L	L

arranged so that the third floor has priority over the first if the first floor was visited last, and the same in reverse.

The first stage in designing an FPLS for this state machine is to allocate binary numbers to each state. In this case we have given the `[ASK1]` state the number 000. The second floor enquiries have two states depending on the position of the lift; when it is at the first floor, or no response has been made to a first floor enquiry, we have the `[ASK2A]` state which we are calling 010, and so on for all eight states.

An FPLS state table has three sections in each row, or transition term: these are the input conditions, the present state and the next state. The usual way to proceed is to take each state in turn and define all the possible transitions out of them. Thus, the first line in the state table in Fig. 9b is the transition from `[ASK1]` to `[ACCEPT1]`, which needs `CALL1` high. The next line gives the result if `CALL1` is low, when the next state is `[ASK2A]` In all, twelve transition terms are required, each one corresponding to one arrow in the state diagram.

Physically, each transition term occupies one AND term in the and-array, with the inputs and present state, while the next state defines the or-array connections. An 'H' in an output column causes the AND term output to be connected to the 'J' of a J-K flip-flop or the 'S' of an R-S type, while an 'L' will join it to the 'K' or 'R'.

While we have described a manual entry method for generating the state table, it is equally valid to write state equations in the syntax described earlier. For example we could write:

```
WHILE [ASK1]
      IF CALL1 THEN [ACCEPT1]
      IF !CALL1 THEN [ASK2A]
```

and so on.

Either the Philips SNAP program or one of the proprietary assemblers, such as ABEL, CUPL or LOG/iC, can then be used to generate the state table from the state equations.

While this example is based on an imaginary lift which is confined to three floors, it might be easily modified to a situation where three processors are competing for resources in a multi-processor environment. Two methods are commonly used in this type of application, round robin, where each subject is interrogated in turn until one is found requiring service, and last granted lowest priority, where the controller creates a queue, the last processor going to the back of the queue when it has finished using the shared resources.

One feature unique to FPLSs is the complement term; it is an inverting feedback from the or-array to the and-array. Its purpose is to allow the `ELSE` construct in state equations. Logically, it does this by or-ing all the defined transitions from a given state and inverting the result. This is then itself used as an input condition for the case when none of the defined conditions is true.

The physical construction of the complement array is shown in **Fig. 10**, and we can illustrate its use with the state table in **Fig. 11a**. This is a state machine which allows access to a system via an entry code; it bears some resemblance to an automatic teller system ('hole-in-the-wall'), except that the PIN is hard-wired and only three digits have to be entered.

From the state `[START]` an '`8`' must be entered; this will be accompanied by a `KEY` signal to indicate a key depression and will cause a jump to state `[OK1]`. Any other number with `KEY` will cause a jump to `[FAIL]`. Releasing key '8' changes `KEY` to `!KEY` and state `[PAUSE1]` is entered. This proceeds with a '`1`' and a '`3`' until state `[PASS]` is reached when the system can be accessed. Once the transaction is complete the system will

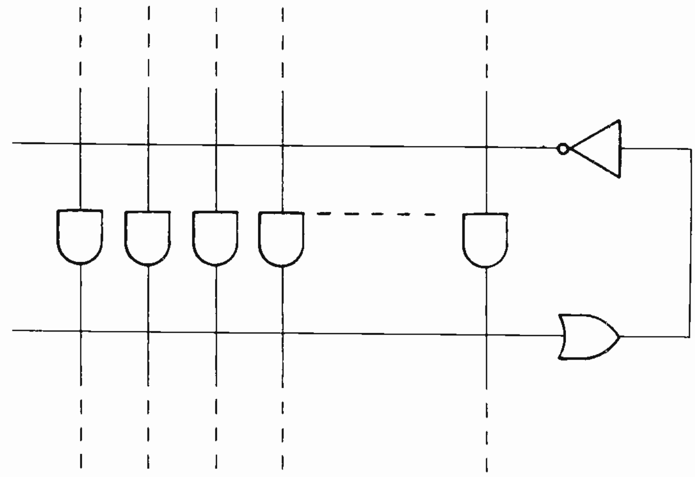
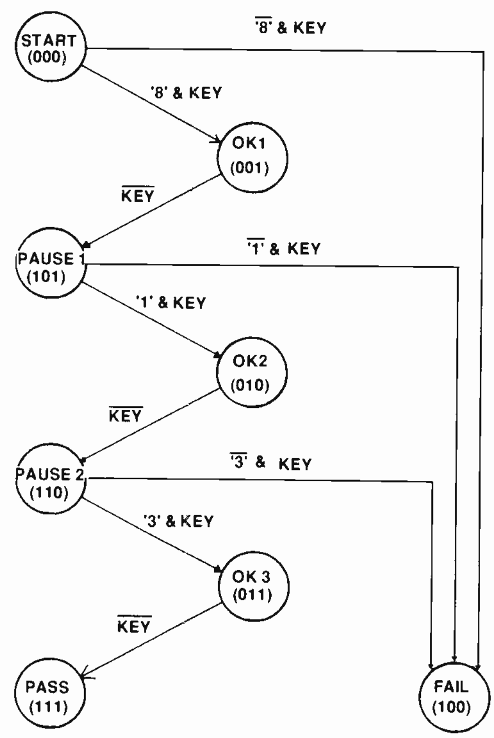


Fig. 10. FPLS complement term.



		INPUTS					PRESENT STATE			NEXT STATE		
C		B3	B2	B1	B0	KEY	S2	S1	S0	S2	S1	S0
A		H	L	L	L	H	L	L	L	L	L	H
•		-	-	-	-	H	L	L	L	H	L	L
-		-	-	-	-	L	L	L	H	H	L	H
A		L	L	L	H	H	H	L	H	L	H	L
•		-	-	-	-	H	H	L	H	H	L	L
-		-	-	-	-	L	L	H	L	H	H	L
A		L	L	H	H	H	H	H	L	L	H	H
•		-	-	-	-	H	H	H	L	H	L	L
-		-	-	-	-	L	L	H	H	H	H	H

Fig. 11a. State diagram of a simple coded access system.

Fig. 11b. State table of a simple coded access system. The complement term found in FPLSs is used to implement the ELSE condition. In the state diagram of Fig. 11a, a transition from [START] to [OK1] is triggered by an '8' being entered along with a valid key signal. Any other number will cause a jump to the [FAIL] state. This could be achieved by making transition terms with all other possible numbers, but the complement term allows this to be done in a single term.
Feeding back the inverse of '8' & KEY provides a logic signal which triggers the jump to [FAIL] when gated with the valid key input. The same complement term can be used by other states without interference because any TRUE transition overrides any FALSE inputs to the OR gate which drives the feedback. Also, if all the transitions from the current present state are FALSE, no other transitions can be TRUE because their present states are not the current present state.
Fig. 11b shows how the complement term is entered into a state table. An 'A' in the complement term column (C) generates a complement, that is it connects a transition to the complement OR gate. A '.' propagates the complement back to the input array.

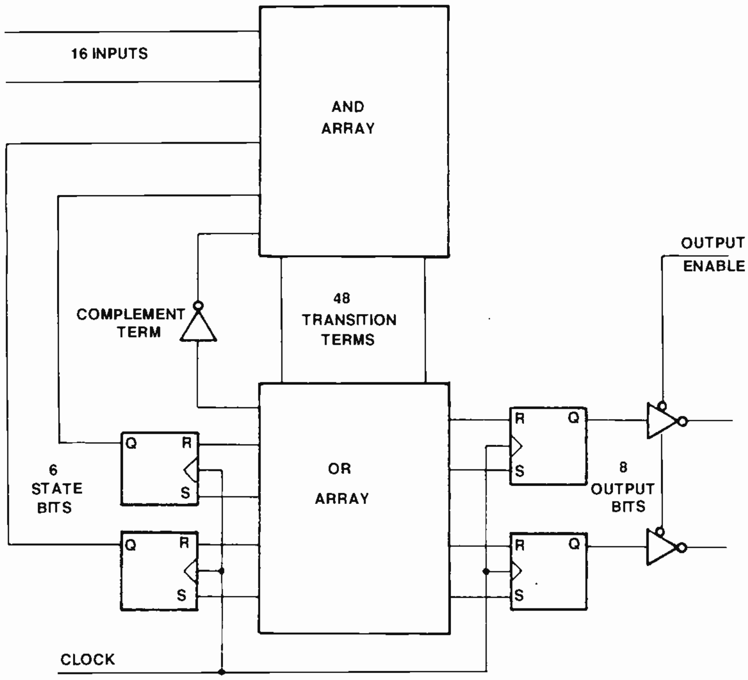


Fig. 12. PLS105 block diagram.

reset the state machine to **[START]**. **[FAIL]** will have the same effect except that the cash card will be retained.

The jump condition from **[START]** to **[OK1]** is easily defined as:

```
WHILE [START]
        IF B3 & !B2 & !B1 & !B0 & KEY THEN
```

[OK1] but the jump to **[FAIL]** needs four terms as **(!B3 & !B2 & !B1 & !B0)** must be expanded to **!B3 # B2 # B1 # B0**. However, with the complement term we can write the jump condition as:

```
ELSE IF KEY THEN [FAIL]
```

The complement term can still be used with transitions from states **[PAUSE1]** and **[PAUSE2]** because the logic signal which is fed back, inverted, is low if any of the transition terms or-ed into it is high. Even though, while in state **[START]**, the transitions out of **[PAUSE1]** and **[PAUSE2]** are invalid, the complement term will remain inactive unless the transition from **[START]** to **[OK1]** is itself invalid. A similar argument applies to **[PAUSE1]** and **[PAUSE2]** themselves.

Figure 11b shows the full state table for this system. The convention for entering the complement term is to use an 'A' for attaching it to an and-term, and a '.' for feeding it back to the and-array. The whole diagram can be defined in nine terms, and further reduction is possible with some simple logic minimisation. Without minimisation and the complement term, eighteen transition terms would have been required.

We can now look at FPLS device options. There are two families of FPLS based, respectively, on R-S and J-K flip-flops. The *PLS105* was introduced about fifteen years ago and has a straightforward architecture, as in **Fig. 12.** With sixteen inputs, an eight-bit output register, a six-bit internal register, 48 transition terms and a complement term, it can cope with some very complex state machines. The coded access system described above would fit into one corner of a *PLS105*.

There have been a number of derivatives of the chip. Where the *PLS105* needs a 28 pin package, the *PLS167* and *PLS168* fit into 24 pin packages by reducing the number of inputs and, in the case of the *PLS167*, the number of outputs. Some enhanced versions, such as the *PLUS405*, the *PLS506* and *PLS30S16* have also been made. They follow the same basic architecture but may have more transition terms or register bits.

Figure 13 shows the output register of the *PLS155* family. Based on a J-K flip-flop, it is surrounded by other programmable features which increase its versatility. Foremost of these is the J to K inverter. When this is active, it makes the J-K flip-flop emulate a D-type. The flip-flop type can be set for whichever is the most efficient for the application, and can even be changed in mid operation. This is described in a Philips application note, where a *PLS159* is used as an eight bit shift register/counter.

Another useful feature is the ability to load the register directly from the outputs. This could be used in testing the device, to set the register into a known state, or in operation: data from a microprocessor bus could be loaded into the register, and then read back at a later time after some modification according to the input conditions.

This family also contains combinatorial i/o pins. Each device has twelve potential outputs. These are either four (*PLS155*), six (*PLS157*) or eight (*PLS159/PLS179*) registered with the balance of twelve bidirectional i/o. The *PLS179* is a 24 pin device, with eight dedicated inputs, the others come in 20 pin packages with four inputs.

As a final example of using FPLSs, and the *PLS155* in particular, we can look at the design of a Gray Code counter. The count sequence for four bits is shown in **Fig. 14a**. Because there are sixteen states, sixteen transition terms would be needed if this were designed as a basic state machine. The Karnaugh Maps for the four counter bits are shown in **Fig. 14b,** for a design using D-type flip-flops. This cuts the design to thirteen transition terms.

Note, however, that **Q3** and **Q2** each require three terms, but inspection of the count sequence shows that they only change their level twice, as indicated by the rings round the changes in Fig. 14a. Toggling is a function of J-K flip-flops, so if **Q3** and **Q2** use these, two more terms can be saved. This is not crucial if no other functions are being incorporated into the FPLS, but a reduction from sixteen to eleven terms might be important if the Gray Code counter is only one part of the overall FPLS function.

The full state table for the FPLS is shown in **Fig. 14c.** The symbol '0' is used for the toggle function as both 'J' and 'K' inputs must be driven high for toggling; this is the unblown fuse condition of the FPLS. The fuse which enables the J to K inverter must also be blown for **Q3** and **Q2** , shown by a '.' in the flip-flop control field (**FC**). The **'A'** in this field for **Q1** and **Q0** leaves the inverter enable fuse intact.

To specify this function with equations is equally valid, and will give the same result if a PLD compiler is used to assemble them. The usual format for specifying the flip-flop type in any device where this is alterable is:

```
Q3.T := !Q3 & Q2 & !Q1 & !Q0
   # Q3 & !Q2 & !Q1 & !Q0
   .
   .
   Q0.D := !Q3 & !Q2 & !Q1
   # etc.
```

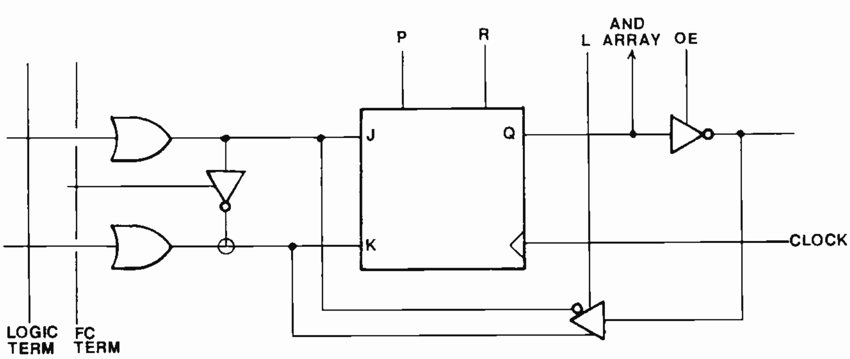


Fig. 13. PLS155 family output stage.

Q3	Q2	Q1	Q0
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
0	0	0	0

Fig. 14a. Gray code count sequence. Inspection of the count sequence shows that Q2 and Q3 only change state twice. As a result, two terms can be saved.

Q3

		0	0	1	1	Q3
		0	1	1	0	Q2
0	0		H	H		
0	1			H	H	
1	1			H	H	
1	0			H	H	
Q1	Q0					

Q2

		0	0	1	1	Q3
		0	1	1	0	Q2
0	0		H	H		
0	1		H	H		
1	1		H	H		
1	0	H	H			
Q1	Q0					

Q1

		0	0	1	1	Q3
		0	1	1	0	Q2
0	0					
0	1	H		H		
1	1	H		H		
1	0	H	H	H	H	
Q1	Q0					

Q0

		0	0	1	1	Q3
		0	1	1	0	Q2
0	0	H		H		
0	1	H		H		
1	1		H		H	
1	0		H		H	
Q1	Q0					

Fig. 14b. Karnaugh maps for gray code count bits.

Fig. 14c. State table for Gray Code counter. The composite flip-flop of the PLS155 can sometimes be useful in saving transition terms. and-term reduction is not such a useful function in registered PALs because each output has a fixed allocation of terms and, unless an output is likely to use more than its allocation, no advantage is obtained by reducing the number of terms in any one output because they cannot be used elsewhere.
In an FPLS, all the transition terms are useable by all outputs, so any saving makes more transition terms available for use if other functions are being included in the same PLD. The example of a Gray Code counter is relevant because this could well form just part of the overall function in one FPLS.
The composite flip-flop can be used as either a D-type or a J-K flip-flop. The count sequence of Fig. 14a is transformed into Karnaugh maps for D-types by entering the state prior to that in which the bit being mapped is set high. Thus, one cell for Q0 is 0000 because the next line in the sequence has Q0 set high.
Fig. 14b shows the resulting maps. Q3, Q2 and Q1 all need three terms while Q4 needs four, making a total of thirteen for the whole counter. This is three better than the sixteen which would be needed if each line of the counter was loaded directly by J-K flip-flops, but J-Ks can also be configured in toggle mode.
Inspection of the count sequence shows that Q3 and Q2 toggle twice per count but Q1 toggles four times and Q0 eight times. Sixteen terms would be used if all the flip-flops were set to toggle but, if only Q3 and Q2 are toggles, the term count is reduced to eleven.
The state table in Fig. 14c has just eleven lines. The first four use '.' in the flip-flop control column; this defines the flip-flop as J-K, and the '0's in the next state mean both J and K are connected to the active and-term, resulting in toggle operation.
The remaining seven lines, with 'A' in the flip-flop control column, leave the flip-flop as a D-type, with the J to K inverter enabled.

	PRESENT STATE				NEXT STATE			
FC	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
•	L	H	L	L	O	–	–	–
•	H	L	L	L	O	–	–	–
•	L	L	H	L	–	O	–	–
•	H	H	H	L	–	O	–	–
A	L	L	–	H	–	–	H	–
A	H	H	–	H	–	–	H	–
A	–	–	H	L	–	–	H	–
A	L	L	L	–	–	–	–	H
A	H	H	H	–	–	–	–	H
A	L	H	H	–	–	–	–	H
A	H	L	H	–	–	–	–	H

The facts and figures of HF receiver performance

Jon Dyer cuts through the haze of misunderstanding surrounding receiver performance. He looks in detail at each parameter, what it means and why it's important, and shows why "dynamic" performance parameters are vital.

Receiver performance specifications can be complex. But that is a necessity, as all parameters must be specified accurately and completely if confusion is to be avoided.

The first parameter to look at is sensitivity, the measure of a receiver's capability to amplify the smallest of signals without losing any of the "intelligence" carried by the signal. Once the signal level falls close to the receiver noise level, normally expressed as a signal to noise ratio (S/N), intelligibility will be lost. Even a hypothetically perfect (noiseless) receiver would still run into thermal noise.

Sensitivity is defined as the signal voltage required to give a specific S/N in a particular receiver bandwidth, for a particular receiver mode (eg AM or SSB). Modulation level is specified for AM (often 30%), and a modulation deviation (eg 5kHz) for FM. An alternative definition for FM is to use quieting sensitivity: the input level required to reduce output noise by, say, 20dB (squelch off). Bandwidth must also be taken into account because noise is proportional to square root of the bandwidth.

Bipolar transistors and fets can produce sensitivities of $0.5\mu V_{EMF}$ for a 10dB S/N ratio (3kHz bandwidth, HF, for an SSB or CW signal) and similar levels can be obtained on FM.

The figure for AM (30% modulation level, 6 or 8kHz bandwidth) is about 9-10dB (about three times) worse than the SSB/CW figure ($1.6\mu V_{EMF}$).

On VHF and above, receiver sensitivities are often even better.

Noise factor

The sensitivity figure is an intuitive way of describing the sensitivity of a receiver. But it is also rather complex, related to a particular bandwidth, temperature, receiver mode, S/N ratio, and input impedance.

A much more convenient measurement is the noise factor (NF), a single number telling everything that needs to be known about a receiver's sensitivity. It is the ratio of the S/N of a hypothetically perfect (noiseless) receiver, to that of a real receiver which adds its own noise to that of the thermal noise.

As the ratio of two ratios it is independent of bandwidth, temperature, mode, S/N, and impedance. 10dB is typical NF for an HF receiver, while at VHF/UHF noise factors of 5dB or less are common.

Noise on HF

But what happens in real life? In a wideband antenna system using a 3kHz receiver bandwidth at a quiet location, thermal noise calcu-

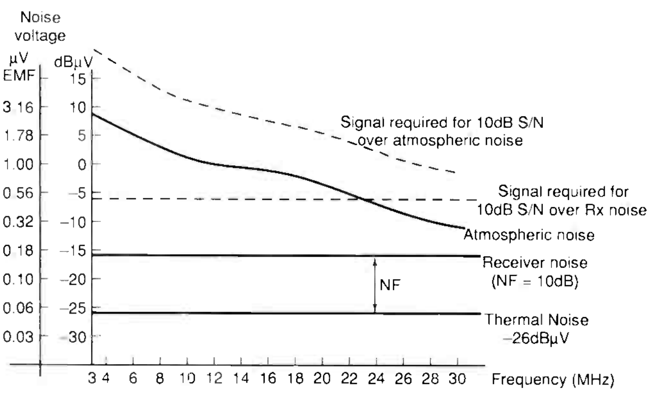


Fig. 1. Noise on HF in a 3kHz bandwidth. Even for a quiet atmosphere, a receiver with 0.5μVEMF for 10dB S/N will need a signal of between 1μVEMF and 10μVEMF.

lated for a typical system would be −26dBμV. If the receiver has a NF of 10dB, then its noise floor will be (**Fig. 1**) at −26 + 10 = −16dBμV. For most HF modes (SSB, AM, CW) an S/N of 10dB is adequate. To achieve 10dB, a signal will need to be 10dB above the receiver noise floor, which in this case is at −16 + 10 = −6dBμV, or 0.5 μV_{EMF}, shown in Fig. 1 as the horizontal dashed line.

This gives the well-known relationship that an NF of 10dB is equivalent to a sensitivity of approximately 0.5μV_{EMF} for a 10dB S/N in a 3kHz bandwidth. Sensitivity for any other bandwidth or S/N can be calculated using:

$$Sensitivity_{(dB)} = NF_{(dB)} + V_{N(dB)} + S/N_{(dB)}$$

Figure 1 also shows that the typical atmospheric noise for a quiet area at a quiet time is between 5 and 25dB above receiver noise. Under real operating conditions on HF, our receiver with its published sensitivity of 0.5μV_{EMF} for 10dB S/N, will need a signal of between 1μV_{EMF} (at 30MHz) and 10μV_{EMF} (3MHz) to give a 10dB S/N ratio – and this is for a quiet atmosphere (and no QRM)!

So, for this receiver, atmospheric noise, not receiver noise, limits performance on HF. Indeed, sensitivity could be reduced to 1μV_{EMF} (15dB NF) without loss of performance, except perhaps at 20 to 30MHz. There is little point in reducing NF below 10dB for an HF receiver using a wideband antenna – especially as sensitivity can only be obtained at the expense of dynamic effects such as intermodulation performance.

Advertised claims of 0.15μV_{EMF} for 10dB S/N are quite impossible. Even a perfect receiver with 0dB NF needs 0.16μV_{EMF} (−16dBμV) to achieve 10dB S/N, due to the thermal threshold of −26 dBμV.

VHF and above

Above 30MHz, as frequency increases background noise, now mainly cosmic, received by the antenna continues to fall: at greater than 120MHz it drops below thermal noise with the result that at quiet locations VHF and UHF receivers can benefit from less than 10dB NF. 2-5dB or less is quite achievable using careful circuit design.

Overall NF is usually determined by the NF of the first amplifying stage in the receiver – normally an RF amplifier (but sometimes a mixer). RF amplifiers invariably use low-noise fets, and careful attention must be paid to the circuit which couples the antenna to the first stage.

"Noise matching" is sometimes used on VHF/UHF equipment where, instead of matching receiver input impedance to the antenna impedance, the two impedances are deliberately mismatched to optimise NF.

Noise is proportional to the square root of bandwidth. If bandwidth is reduced from 3kHz to 300Hz, all noise voltages (thermal, receiver, man-made, and atmospheric) drop by a factor of $\sqrt{10}$ = 3.16, or 10dB. So, at this bandwidth, sensitivity for the 10dB NF receiver (0.5 μV_{EMF} in 3kHz), would be 0.5 / 3.16 = 0.16 μV_{EMF} for 10dB S/N.

This explains the continuing use of CW in the HF bands as a CW signal can still be copied when SSB would be lost in the noise.

Selectivity

Selectivity is the ability to tune one signal while rejecting other close–in signals, usually achieved by using crystal, mechanical, or ceramic block filters. The old constraint of a low second IF no longer applies, and in fact it is easier to design crystal filter frequencies higher than 1MHz. Standard IFs have been established at 1.4, 1.6, 9.0 and 10.7MHz, although the 455kHz IF is still very commonplace using ceramic filters.

Block filters are also used as "roofing filters" in the first IF of HF receivers[1] They are commonly in the VHF region, using 40 to 90MHz crystal filters. VHF and UHF receivers may have a first IF of many hundreds of MHz, using surface acoustic wave (SAW) filters.

Ideal filter response is a flat top with low ripple, and steep sides going down to a −80 dB (or greater) stop band which extends a long way out (**Fig. 2**). Selectivity is usually quoted at the nose bandwidth (6dB down), and the skirt bandwidth (at 60dB down), and for an eight pole SSB filter good values are 2.7kHz and 4.4kHz respectively.

One convenient measure of filter performances is shape factor (SF), the ratio of skirt bandwidth to nose bandwidth. Ideal SF is 1:1, with anything less than 2:1 for a 3kHz SSB filter being good.

Impedance matching into and out of a filter is significant and insertion loss (the loss caused by the filter in the middle of the passband – usually less than 10dB) must be made up by amplification.

A typical "suite" of filters in a high grade HF communications receiver might be 8kHz for AM, 2.7kHz for SSB (often with two asymmetrical filters, one for USB, one for LSB) and 1.0kHz, 300Hz, and 100Hz for CW, RTTY, and other narrowband data transmissions The trend in Amateur equipment is for the tightest possible SSB filter (2.4 kHz), and often 600Hz or 300Hz are used for CW. A VHF/UHF receiver may have any of these plus wider filters, perhaps 12kHz and 50kHz or even wider for FM (Hi-Fi FM tuners need a 200kHz filter).

Image (second channel) rejection

In the normal superheterodyning process, a wanted signal (f_S) beats in the mixer with the local oscillator (or synthesiser output) frequency (f_{LO}). One of the resultant products of the mixing process, usually $f_{LO} - f_S$, at the intermediate frequency (IF), is passed by the IF selectivity filter.

But another frequency, the image or second channel frequency ($f_{LO} + f_{IF}$), also beats with the local oscillator to produce a product at the IF. This frequency must be rejected by RF tuning, either ganged to the "tune" control or using a separate pre-selector control; or by switched bandpass filters, usually automatically switched on synthesised receivers. Image

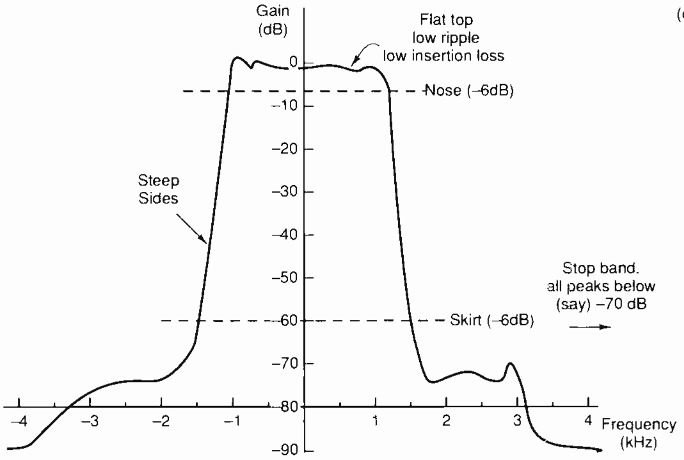


Fig. 2. Ideal filter response with a flat top and steep sides going down to −80dB stopband which extends a long way out.

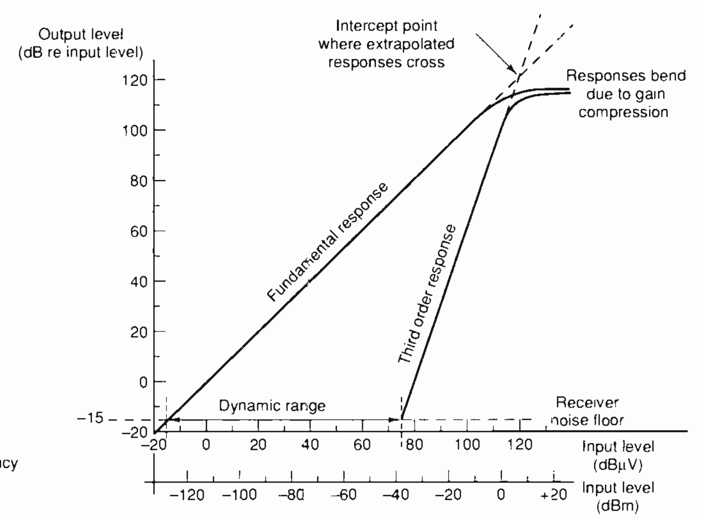


Fig. 3 Third order intercept gives a good indication of intermodulation, cross-modulation and blocking performance.

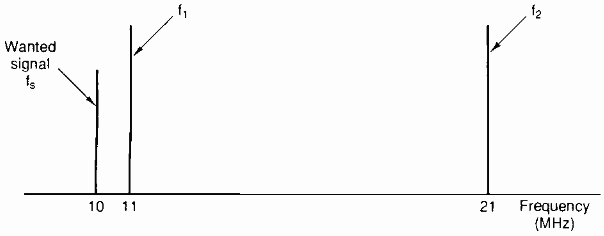


Fig. 4. Second order intermodulation products. A pair of signals causing beats at 10MHz. In a well designed receiver, second order IMP should be rejected by front-end tuning.

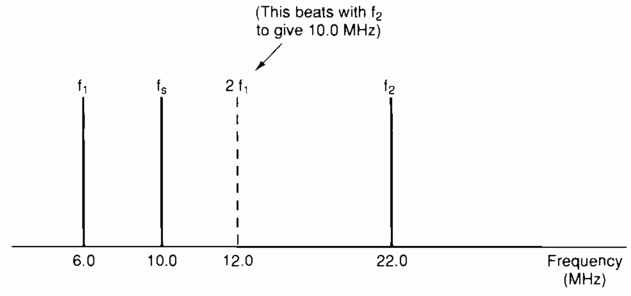


Fig. 5. Third order intermodulation products, where front-end tuning should easily reject both signals.

Fig. 6. Close-in third order IMPs that can not be rejected by front-end tuning.

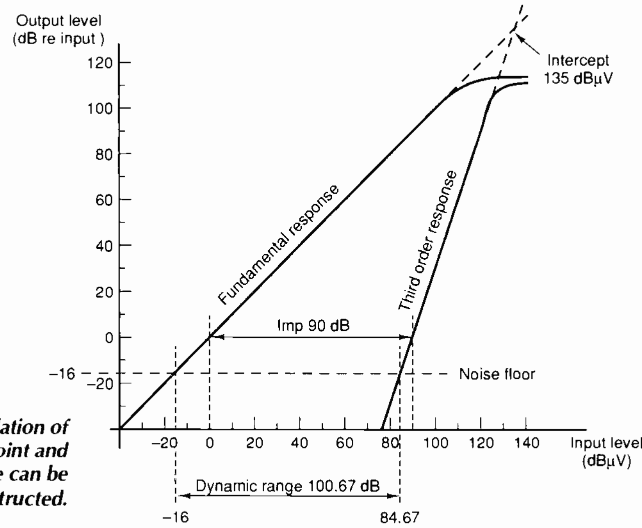


Fig. 7. Intermodulation of 90dB. Intercept point and dynamic range can be constructed.

frequency is equal to f_S plus twice the IF. So the higher the first IF, the further away from f_S will be the image frequency, and the easier it will be to reject. Up-conversion techniques on a HF receiver will put the first IF at 40-90MHz[1]. The image frequency will also be at VHF and so can be rejected by a simple 35MHz low-pass filter at the receiver input.

Image frequency rejection is specified as the ratio in dB of an unwanted signal above $1\mu V_{EMF}$, to give the same output as a wanted (on-tune) $1\mu V_{EMF}$ signal. 60dB of rejection is a poor performance: 90dB or more is good.

IF rejection

Intermediate frequency, or IF, interference occurs when a strong signal at a receiver's IF directly breaks through the early receiver stages and into the IF amplifier. IF rejection is specified similarly to image rejection, with 90dB being the target.

Internal spurious responses

Internal spurious responses (spurii or spurs) are responses of the receiver to self-generated noises and whistles. Problems are caused when they occur at the signal frequency or an intermediate frequency.

Oscillators and mixers may act as noise generators as can digital circuitry – especially the drive lines to multiplexed displays. Other causes are power supply harmonics, parasitic oscillations in amplifiers, and even sub-harmonics of any up-conversion IFs.

Frequency synthesisers and other digital circuits produce large numbers of frequencies, and most waveforms are digital square waves with fast rise-times rich in harmonics.

Careful circuit design, with adequate low-pass and bandpass filtering, keep spurious outputs 100dB down on the main output, ensuring that all spurious responses are no more than 3dB above the receiver noise floor in a 3kHz bandwidth.

Stability

Stability is the measure of frequency drift of a receiver with time and temperature. A fully synthesised receiver can have a stability approximately equal to that of its temperature controlled frequency reference source[1]. An oven-controlled temperature-stabilised crystal oscillator can achieve a stability of less than one part in 10^8/°C (0.1Hz/°C at 10MHz).

Sometimes stability is specified as a short-term (temperature) drift plus a long-term (crystal ageing) drift. With partial synthesis the stability is normally governed by the stability of the VFO, but with cool, buffered solid-state designs short term drift (after a three hour warm-up) of 50Hz/hour is possible.

Dynamic performance

So far, only 'static' performance parameters have been dealt with. This section looks at dynamic performance, which relates more closely to real-world conditions.

Dynamic effects are generally caused by large off-tune signals, making the receiver operate nonlinearly.

Two unwanted signals can intermodulate to produce a product at the same frequency as the wanted signal (intermodulation); or modulation from an unwanted signal can be transferred to the required signal (cross modulation). Alternatively an unwanted signal can reduce the sensitivity of (or block) the required signal (blocking).

One problem is that activity on the bands (especially on HF and VHF) has increased to such an extent that many large off-tune signals are always present at the receiver's input stages. It is these dynamic effects rather than the traditional sensitivity/selectivity/stability parameters that largely determine performance of the communications receiver under real-life signal conditions.

Intercept point

Intermodulation, cross modulation, and blocking are caused by second and third order products, as the receiver responds to these at a greater rate than it responds to the fundamental signal input (**Fig. 3**).

Second-order products cause the output to increase as the square of the input – twice as many dB – and third-order products as the cube of the input – three times dB. Forth, fifth, and higher order intermodulation products are normally ignored as second and third order effects predominate.

Arguably the single most useful performance parameter of all is the intercept point, where two extrapolated responses cross. Third-order effects are generally more significant than second-order. Figure 3 shows how the third-order response crosses the fundamental response which is extrapolated at

120dBμV or +7dBm.

Most amplitude measurements are defined using voltages (μV, mV, dBμV, etc.). But the intercept point is usually specified as a power ratio, the dBm, where a dBm is a dB relative to a power of 1mW into the receiver input impedance.

The third-order intercept is so important because it is a single number giving a good indication of the intermodulation, cross-modulation, and blocking performance. +5 to +35dBm is considered good.

Dynamic range

Dynamic range is the span of signal amplitudes – from smallest to largest – to which the receiver responds.

The "single signal" dynamic range is limited at the low end by noise, and at the upper by gain compression: amplifier outputs start hitting the supply rails and the outputs can increase no further.

Definitions of dynamic range are often of limited value in the real situation of a large number of signals – some of which are very large in amplitude. It is the large signals that really limit the dynamic range (again due to the receiver's nonlinearities).

Dynamic range is best described as the range of input signals over which dynamic interference effects produce non-significant outputs, at or below the noise floor. A useful working definition is that it is two-thirds of the difference in level between the noise floor and the intercept point in a 3kHz bandwidth. Or, it is the difference between the fundamental response input level and the third-order response input level as measured along the noise floor (sometimes defined as 3dB above the noise floor) in a 3kHz bandwidth, Fig. 3. Reducing the bandwidth improves dynamic range because of the effect on noise.

Using this definition, dynamic range for the receiver depicted in Fig. 3 is 90dB, compared with more like 130dB when a single signal definition is used.

Clearly great care must be taken in interpreting manufacturer's figures. Using our preferred definition, a dynamic range of 90 to 110dB for 3kHz bandwidth with an intercept point of 120 to 150dBμV (or +7 to +37dBm) is good.

Intermodulation

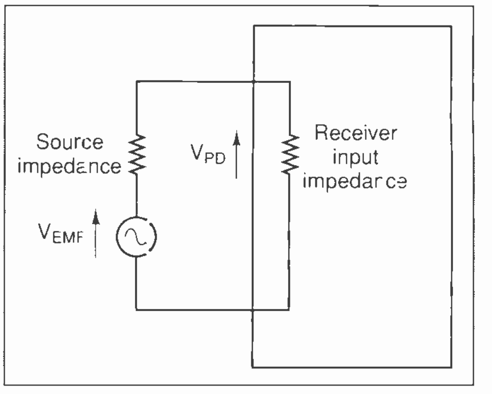
Second-order intermodulation products are simply equal to $f_1 \pm f_2$, where f_1 and f_2 are the two unwanted frequencies. An example, **Fig. 4**, is where the two unwanted signals are at 11 and 21MHz causing a beat at 10MHz. Other pairs of signals at (say) 6 and 16MHz, or 3 and 7MHz would produce a similar product at 10MHz.

For second-order intermodulation to occur, one of the signals must be far removed from the wanted signal and can easily be rejected by any reasonably tight tuning – including the passband of any octave or sub-octave block front-end filter fitted to many modern communications receivers[1].

Input/output isolation around these filters

Decibel definition

The dBμV is a decibel relative to 1μVEMF. Decibels relative to 1mW into a system with a nominal 50Ω impedance are referred to as dBm. Again in a 50Ω impedance system, 0dBm equates to 224mVPD, or 113dBμV. To convert from dBμV to dBm, simply subtract 113. For example, 0dBμV=1μVEMF=0.5μVPD=-113dBm.



Note that RF voltages in this article are electromotive forces unless otherwise stated. Recently, manufacturers are more commonly specifying sensitivities and other parameters using potential difference instead.

Whether you use PD or EMF is not too important provided that the distinction is made clear. Often this is not the case, which usually implies that potential differences are intended. Of course the use of potential differences makes many parameters, sensitivity for example, look twice as good, i.e. a 6dB improvement. This is because in a matched impedance system, PD is always half EMF!

must be good, or second-order intermodulation can be a real problem. On some low cost general coverage HF receivers, third-order intermodulation performance is quite good, but second-order performance is poor if using a wideband antenna without an antenna tuning unit (ATU.)

Third-order intermodulation tend to be equal in frequency to $2f_1 \pm f_2$. For example, the second harmonic of a 6MHz signal (at 12MHz) beats with a 22MHz signal to produce a 10MHz third-order product at the wanted frequency (Fig. 5). Front-end tuning should easily reject both signals. But where, say, the second harmonic of a 10.4MHz signal (at 20.8MHz) intermodulates with a 10.8MHz signal to produce the 10MHz interfering signal (**Fig. 6**), both unwanted signals are very close to the wanted signal, and well within the rf passband regardless of RF tuning.

Third-order intermodulation is normally considered more important than second-order. This is because it cannot be rejected by front-end tuning.

Intermodulation performance (IMP) is typically specified as the levels of two unwanted signals not less than (say) 20kHz off tune to give a 0dBμV (1μV_{EMF}) response.

A good HF receiver will have a third-order intermodulation performance of 80–100dBμV. Second-order performance should be similar, but is often not stated – which can be misleading. Statistical analysis of the actual signals received over the whole HF band using wideband (rhombic) antennas indicates that at least 90dB of third-order intermodulation performance is required[2, 3]. That level corresponds to 32mV_{EMF} and at almost any time there will be tens of broadcast (and other) stations putting 10–100mV_{EMF} onto a wideband HF antenna, with hundreds of others in the range 1–10 mV_{EMF}.

A simple example should help put everything into perspective.

Take the 10dB NF receiver, with its noise floor at –16 dBμV for 3kHz bandwidth, and a good IMP of 90dB (indicated by the line at the 0dBμV level on **Fig. 7**). Third order response will have a slope three times that of the fundamental response, with its position defined by the 90dB IMP line. The intercept occurs at 135dBμV or +22dBm (50Ω) where the extrapolated responses cross. (In practice the actual responses bend over before crossing as shown due to gain compression.)

Calculated dynamic range turns out to be 100.67dB.

In-band intermodulation

In-band intermodulation, when two signals within the IF passband intermodulate to produce extra products, is normally of little significance except where multichannel "voice frequency telegraphy (VFT)" systems such as "Piccolo" are in use. It is specified as the level of an unwanted intermodulation product relative to two equal wanted in-band signals (a product of 40dB below two equal in-band signals is good).

Cross–modulation

Cross modulation occurs when modulation from a single unwanted amplitude modulated signal transfers itself across, and modulates the wanted signal (**Fig. 8**). Non-linearities in the early receiver stages are the cause, and sometimes the same modulation may reappear on each adjacent signal tuned in. The parameter may be specified as the level required, in dBμV, for a 30% modulated car-

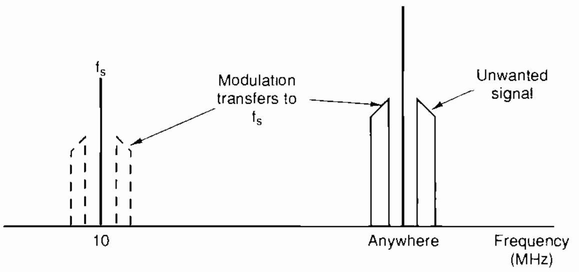


Fig. 8. Cross modulation where a single unwanted amplitude-modulated signal transfers itself across and modulates the wanted signal.

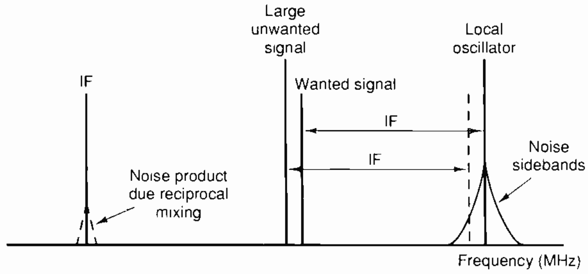


Fig. 9. Reciprocal mixing reduces the selectivity of the receiver in a way not revealed by selectivity figures.

rier greater than (say) 20kHz off-tune, to cause an interfering signal 20dB below a wanted signal, greater than some specified level, in a 3kHz bandwidth for example.

As cross–modulation is a third-order effect, good third-order intermodulation performance will tend to mean good cross modulation performance. The level of an interfering signal will normally have to be higher than for intermodulation. The signal will be within the front-end tuning bandwidth of the receiver, so will typically be in the same or adjacent broadcast band to the band being received. 100-120dBμV is good.

Blocking

De-sensitising, or blocking, occurs when the large off-tune interfering signal causes a reduction in wanted signal output, through a product generated by the non-linearities of the receiver front-end.

It is specified as the level of an unwanted signal, removed from the wanted channel by at least (say) 20kHz, required to reduce a wanted output by 3dB. Blocking can often be caused by a strong CW signal, causing gain to go up and down with the keying. 90–110dBμV for a 3dB reduction is good, for a wanted 1 mV_{EMF} signal.

A value of at least 20kHz is specified for this and other dynamic performance parameters, to ensure that the unwanted signal will be outside the passband of the receiver IF stages. While it is suitable for a HF receiver with a good roofing filter (which might have a nose bandwidth of 12kHz or so), 50kHz might be a better figure for a VHF or UHF receiver.

Causes and cures of non-linearity effects

The only really effective solution to improving performance is to improve front-end linearity.

Linearity of bipolar transistors in rf amplifiers and mixers is not good. But fets are approximately square-law devices and modern designs invariably use fets (often mosfets) for good third-order performance, with sub-octave front-end filters to ensure good second-order performance.

Linearity can be further improved by using high voltage supplies, and by keeping pre-roofing filter gain to a minimum.

Almost anything imaginable can be a cause of non-linearity, and all components normally considered to be linear, passive, and reciprocal must be carefully checked to ensure they really are. But, with careful consideration, very good linearity can be achieved with an intercept point of 140dBμV (+27dBm).

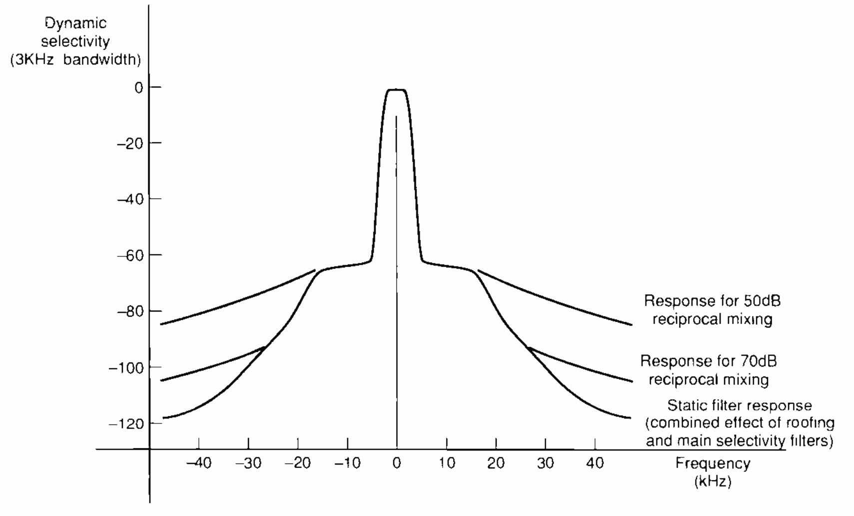


Fig. 10. Selectivity of a receiver in a "real life" situation of a band full of signals.

Reciprocal mixing

Reciprocal mixing is due to high levels of unwanted signals mixing with the noise sidebands of the local oscillator/synthesiser, producing unwanted products at the wanted frequency (**Fig. 9**).

Its importance is that it reduces selectivity of the receiver in the presence of large close-in signals, in a way not revealed by "selectivity" figures quoted in specifications. The off-tune signals are introduced into the IF at levels proportional to their distance from the wanted signal. **Figure 10** indicates dynamic selectivity in a "real life" band full of signals. As can be seen, it is the stopband of the filter response that has been changed, and with 50dB of reciprocal mixing, a considerable loss of performance occurs. Improving it to 70dB considerably reduces its effect on filter response.

Reciprocal mixing is specified as the dB of an unwanted signal at (say) 20kHz off-tune, above a wanted signal, to produce a noise product 20dB down on the wanted signal level, in a specified bandwidth (3kHz).

The unwanted signal, fairly close to the wanted signal, cannot be rejected by front-end filtering, and as it is not caused by front-end non-linearity, the above cures are no use. The only solution is to design oscillators with very low noise outputs, especially close-in phase noise, by employing high "Q" in the oscillatory circuit, and also by using high powers in the oscillator to improve S/N.

Phase locked loops (PLLs) in frequency synthesisers can be very poor in this respect, especially single-loop designs which have low loop gain resulting in high levels of noise. Also PLL's frequently use low Q and low power VCOs in the output.

The noise produced is phase modulated and cannot be removed by limiting. Good design can produce a frequency synthesiser output noise of 90–100dBc (referenced to the carrier output), and a good fet crystal oscillator can give 110dB, ensuring a reciprocal mixing performance of 70dB.

Sometimes reciprocal mixing is specified as a 3dB reduction of sinad of the wanted signal, rather than a product 20dB down on the wanted signal. In this case the figure will look almost 20dB better, at around 90dB. ■

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O/P CURRENT	12	14	30	40
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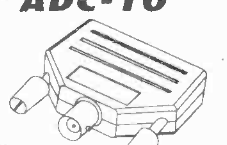

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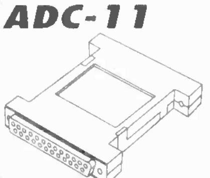

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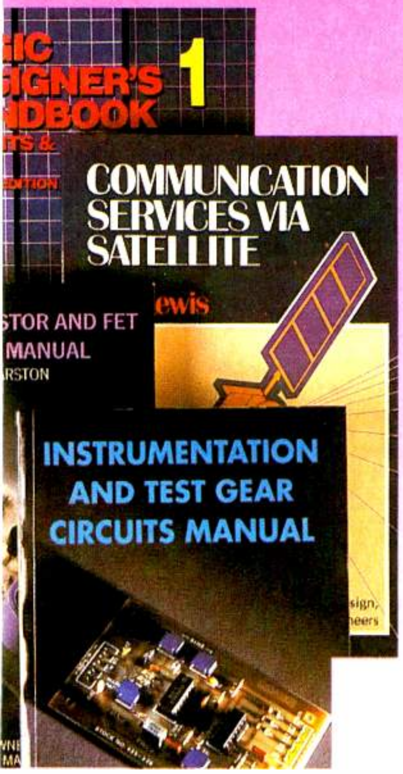

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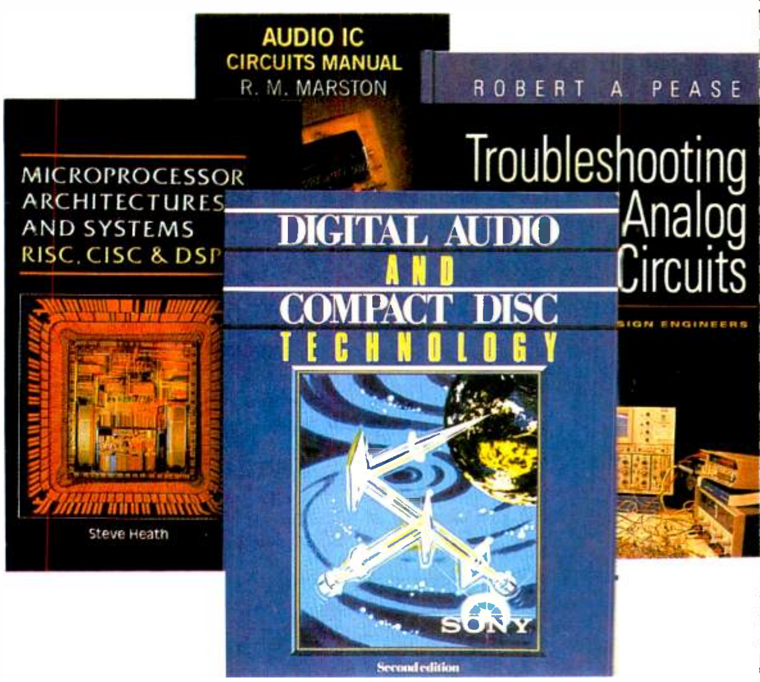

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Power factor controller

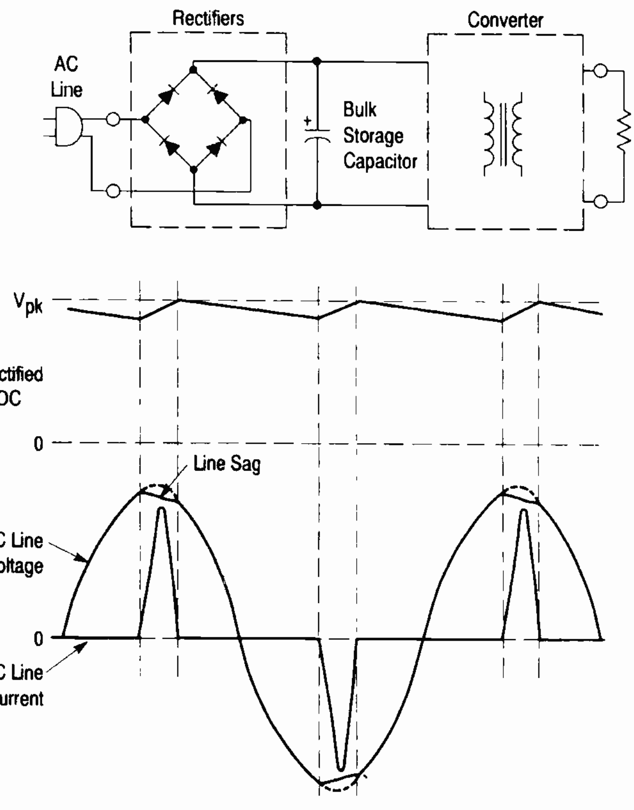
Demand for economical ways of making switch-mode supplies and electronic ballasts exhibit a unity power factor is growing. Having a non-unity power factor introduces harmonic distortion on the mains – a nuisance that electricity suppliers are becoming increasingly concerned about.

Designed for minimal component count, the new *MC34262* forms the heart of a preconverter that sits between the mains supply and a switch-mode supply or ballast, **Fig. 1.** In the circuit configurations outlined in the preliminary data sheet, the IC has the ability to bring the power factor up to between 0.989 and 0.999. Switch-mode supplies typically exhibit power factors of 0.5 to 0.7.

Most electronic ballasts and switch-mode power supplies incorporate a bridge rectifier and reservoir capacitor directly connected to the mains. This provides raw DC to drive the main power converter circuitry.

A simple rectifier only draws current at the peaks of the mains sinusoid, where the voltage at the input exceeds the voltage over the capacitor. As a result, the current waveform comprises spikes which are rich in harmonics, Fig. 1.

Fig. 1. In switch-mode power supplies, straight forward mains rectifiers only draw current when input voltage rises above voltage over the reservoir capacitor. This introduces unwanted harmonics into the mains supply.



Power factor correctors can be passive or active. Passive types usually contain a combination of large capacitors, inductors and rectifiers. Active types incorporate some form of high-frequency switching converter for the power processing. This is usually a boost converter configuration of the type shown in **Fig. 2**.

Since active circuits operate at much higher frequencies than their passive counterparts, they are much smaller, lighter and more efficient. With proper control of the preconverter, almost any complex load can be made to appear resistive to the mains.

Figure 3 shows a complete 175W converter circuit. This is one of three in the note, the remaining two being similar but designed for 80W and 450W. The circuit is a peak detecting boost converter configured in current mode. It operates in critical conduction mode with a fixed on time and variable off time, **Fig. 4**.

A major benefit of critical conduction mode is that the current loop is inherently stable which eliminates the need for ramp compensation. This circuit operates over a wide input range of 90 to 268V AC without adjustment.

Built into the *MC34262* is an overvoltage comparator to stop output voltage rising too high if the load is removed. There is also a undervoltage lock-out, maximum peak switching current limitation and a pulse metering latch. Output clamping prevents damage to the mosfet gate.

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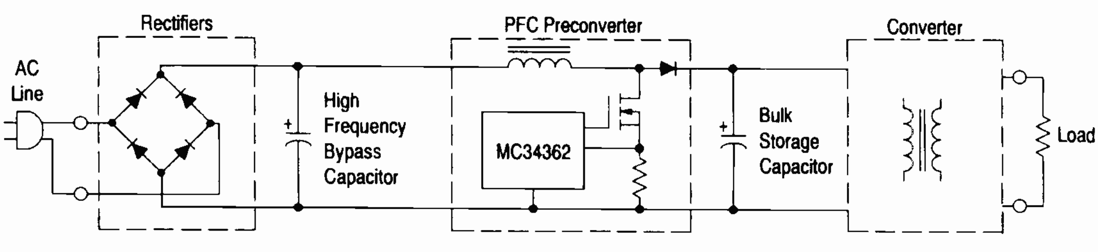
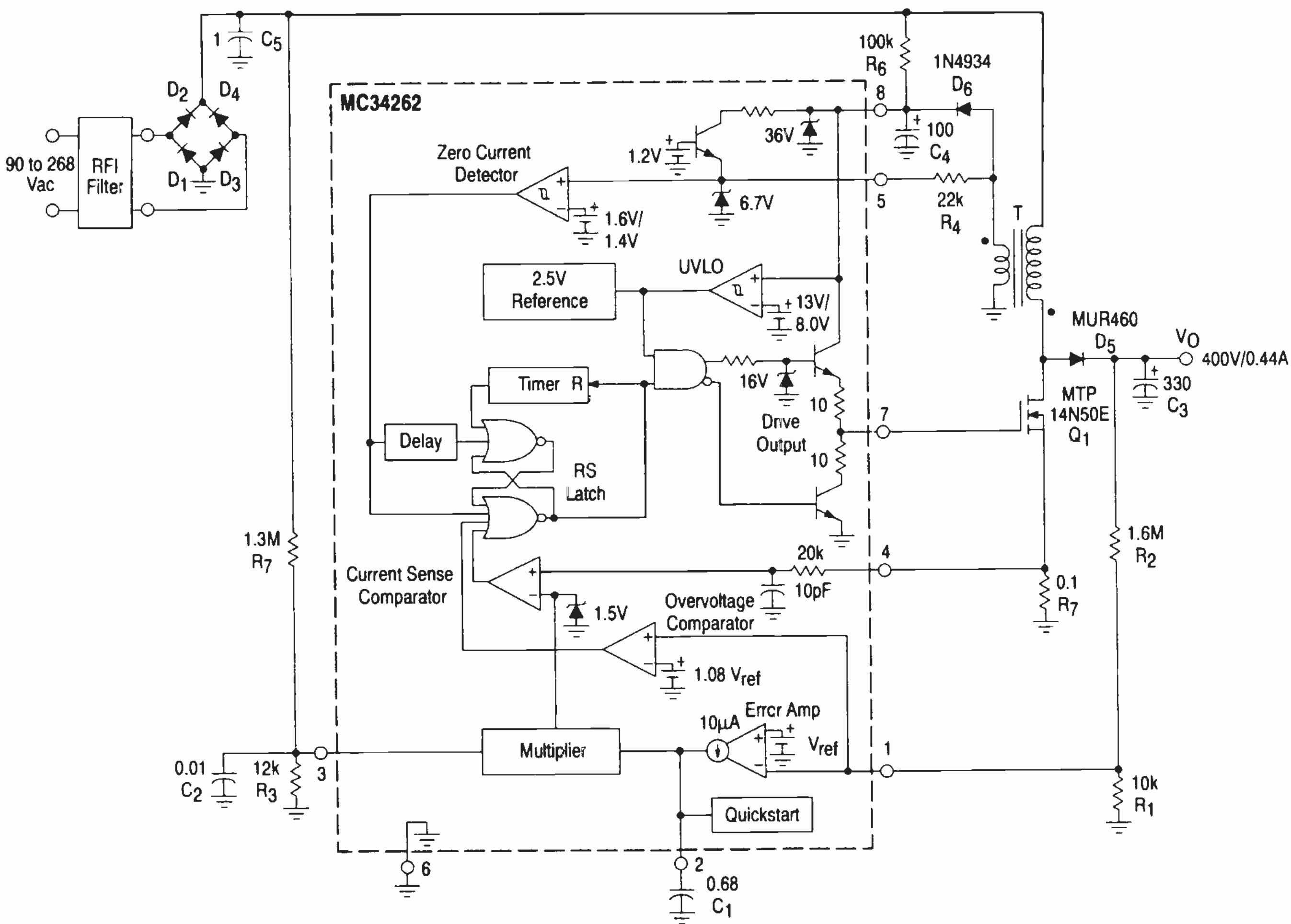


Fig. 2. Active power factor controllers for switch-mode power supplies and electronic ballasts sit between the mains rectifier and storage capacitor. Switching at high frequency, they share the current loading on the mains over the full cycle, resulting in desirable unity power factor.



Power Factor Controller Test Data

				AC Line Input					DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(p\text{-}p)}$	V_O	I_O	P_O	η(%)
90	193.3	0.991	2.15	2.8	0.18	2.6	0.55	1.0	3.3	402.1	0.44	176.9	91.5
120	190.1	0.998	1.59	1.6	0.10	1.4	0.23	0.72	3.3	402.1	0.44	176.9	93.1
138	188.2	0.999	1.36	1.2	0.12	1.3	0.65	0.80	3.3	402.1	0.44	176.9	94.0
180	184.9	0.998	1.03	2.0	0.10	0.49	1.2	0.82	3.4	402.1	0.44	176.9	95.7
240	182.0	0.993	0.76	4.4	0.09	1.6	2.3	0.51	3.4	402.1	0.44	176.9	97.2
268	180.9	0.989	0.69	5.9	0.10	2.3	2.9	0.46	3.4	402.1	0.44	176.9	97.8

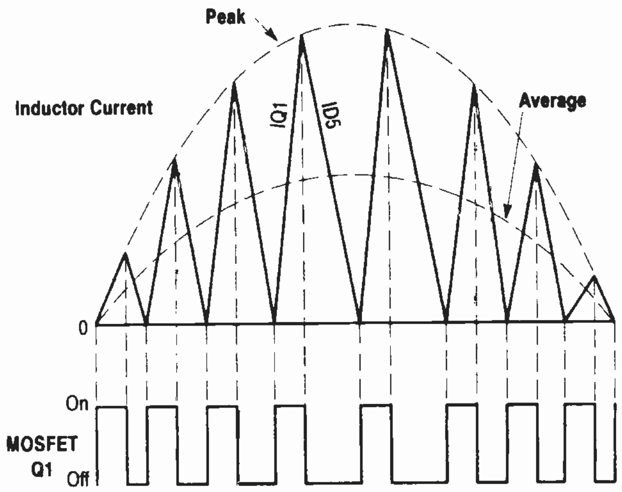
This data was taken with the test set-up shown in Figure 24.

T = Coilcraft N2880-A
Primary: 78 turns of # 16 AWG
Secondary: 6 turns of # 18 AWG
Core: Coilcraft PT4215, EE 42-15
Gap: 0.104" total for a primary inductance (Lp) of 870 μH

Heatsink = AAVID Engineering Inc. 590302B03600

Fig. 3. At 240V input, this universal input circuit brings power factor of a switch-mode PSU up to 0.993 from typically 0.5 to 0.7. It delivers up to 175W.

Fig. 4. This diagram shows inductor current and MOSFET gate voltage waveforms. It illustrates how the power factor corrector circuit of Fig. 3 spreads loading over the full mains cycle to obtain an almost unity power factor.



Switching regulator

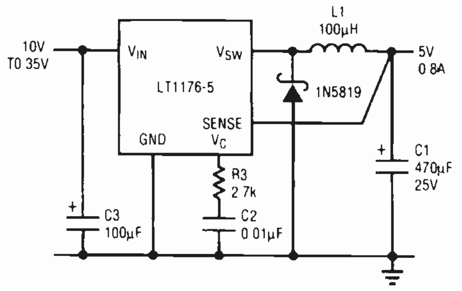
Despite its very low component count this switching regulator is around 85% efficient given 0.5A loading and a 10V supply.

Designed primarily for step-down applications, the *LT1176* can also be used as a positive-to-negative power converter or in flyback mode. It has a true analogue multiplier in its feedback loop, making its responses to changes in input voltage levels nearly instantaneous.

Output current is up to 0.8A and quiescent current is just 8mA. Pulse by pulse current limiting at 1.7A is built in, as is a 100kHz oscillator. When configured as shown, the input voltage range is from 8 to 35V. In inverting and boost configurations, a self-boost facility built in to the IC allows input voltages as low as 5V.

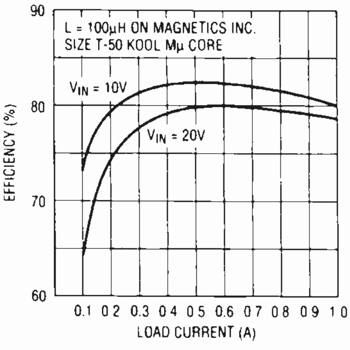
Used as a buck converter, the IC has an output voltage range of 2.5 To 30V. Note that there are two versions of the IC, one with a fixed 5V output, the other adjustable.

Basic 5V Positive Buck Converter



***Linear Technology**, 111 Windmill Road, Sunbury-on-Thames, Middlesex TW16 7EF. Telephone 0932 765688.*

5V Buck Converter Efficiency



One eight-pin IC provides a 0.A, 5V switching power supply with fairly high efficiency and short-circuit protection. Running at 100kHz, the circuit requires a relatively small inductor and smoothing capacitor.

PABX chip handles two trunks with twelve extensions

All telephone transmission, reception and call-progress circuits for mixing voice and control signals are contained in a new highly integrated chip from Sierra. This chip forms the heart of a PABX capable of handling up to five external lines and twelve extensions.

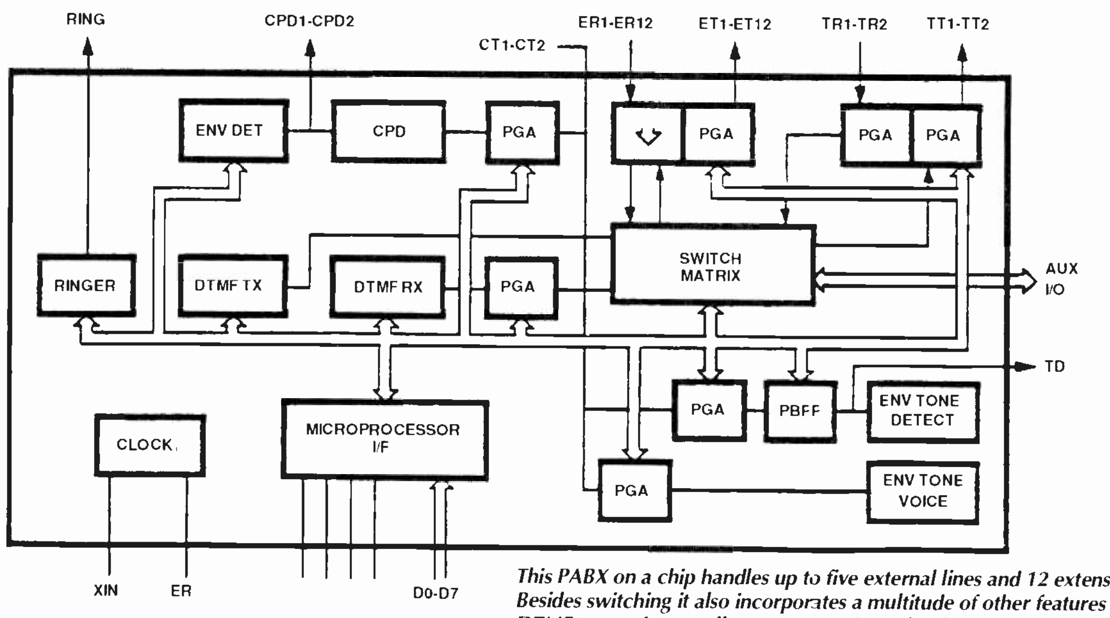
A complete evaluation system for this private automatic branch exchange IC is detailed in the *SC11391391 integrated telephone systems hardware design manual*. Software is also available and the manual includes PCB details.

Key elements of the chip are two matrixes, one 20 by 23 and the second 4 by 4. There are also two DTMF transmitters, two DTMF receivers, a ring generator and programmable call progress monitors. Additionally, the device can handle conference calls, differentiate between fax and voice and connect to tape or ram for recording speech.

Besides switching between the various lines, the matrixes connect various control devices. These include programmable gain circuits, the DTMF transmitters and receivers, call progress monitors, voice detectors and programmable bandpass filters.

Since the circuit diagrams run to fourteen A4 pages, there is only enough room to publish the block diagram.

***Sierra Semiconductor**, Terminal 3, 3B2 Stonehill Green, Westlea, Swindon, Wiltshire SN5 7HB. Tel. 0793 618492.*



This PABX on a chip handles up to five external lines and 12 extensions. Besides switching it also incorporates a multitude of other features like DTMF transceivers, call-progress monitors, fax detection and digital gain.

Techniques for 92% efficient fluorescent backlight driving

Comprehensive information on driving fluorescent backlighting for LCDs is presented in *Techniques for 92% efficient LCD illumination* from Linear Technology. Since backlighting can be responsible for as much as 80% of battery drain, drive circuit efficiency is very important.

Cold-cathode fluorescent lamps present a complex load. Power conversion efficiency is affected by the lamp's current, temperature, dimensions, gas constituents and proximity to nearby conductors. Drive waveform characteristics also play a role.

As the curves shown imply, predicting lamp behaviour under various operating conditions is difficult. Maximum electrical efficiency does not necessarily correspond to the best optical efficiency. It is possible to build a 94% electrically efficient circuit that produces less light output than one with only 80% efficiency. For this reason, electrical *and* photometric evaluation of a circuit is advisable. Methods for both are covered in the booklet.

Other factors greatly affecting efficiency are lossy display enclosures and excessively long connecting wires. Display enclosures with too much conducting material near the lamp can have huge losses due to capacitive coupling. Poorly designed enclosures can easily account for 20% efficiency degradation while high-voltage wire runs typically cause a fall of 1% per inch.

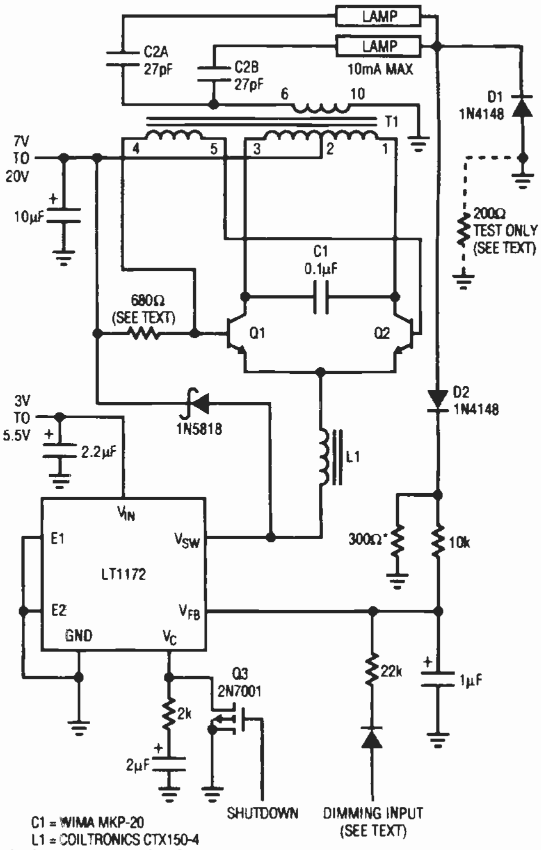
Cold-cathode fluorescent lamps represent a complex load. The voltage needed to force them into conduction, around 1kV, is significantly higher than their operating voltage which is typically 300 to 400V. Until their firing voltage is reached, fluorescent lamps exhibit a very high resistance but after firing, their resistance falls considerably. To compound the problem, the resistance transition is fast.

Due to the combined effects of the cold-cathode fluorescent lamp's resistance characteristics and the frequency compensation problems associated with switching regulators, severe loop instabilities can arise. These are a particular nuisance at start-up. Once the lamp is on, it assumes a linear load characteristic, easing stability criteria.

Although fluorescent lamps can be powered from DC, it is inadvisable to do so since migration inside the lamp will quickly damage it. Typically, lamp operating frequencies are 20 to 100kHz. A sinusoidal drive waveform is preferred since it minimises RF emissions while maximising efficiency.

The design shown here is one of many solutions described and offers a 92% efficient supply for 10mA loads. With this particular circuit, drive is provided for two lamps – a typical requirement for current LCD laptop colour displays. Other features are dimming and remote shutdown which are essential for minimising battery power consumption.

Further information in the note deals with LCD biasing, low-power cold-cathode fluorescent lamps, and feedback stability. There are full chapters on mechanical design considerations, efficiency measurements and power saving techniques. There is also a well-supported section challenging a number of existing lamp driver circuits.



C1 = WIMA MKP-20
L1 = COILTRONICS CTX150-4
Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
T1 = COILTRONICS CTX110600-1 OR SUMIDA EPS-207
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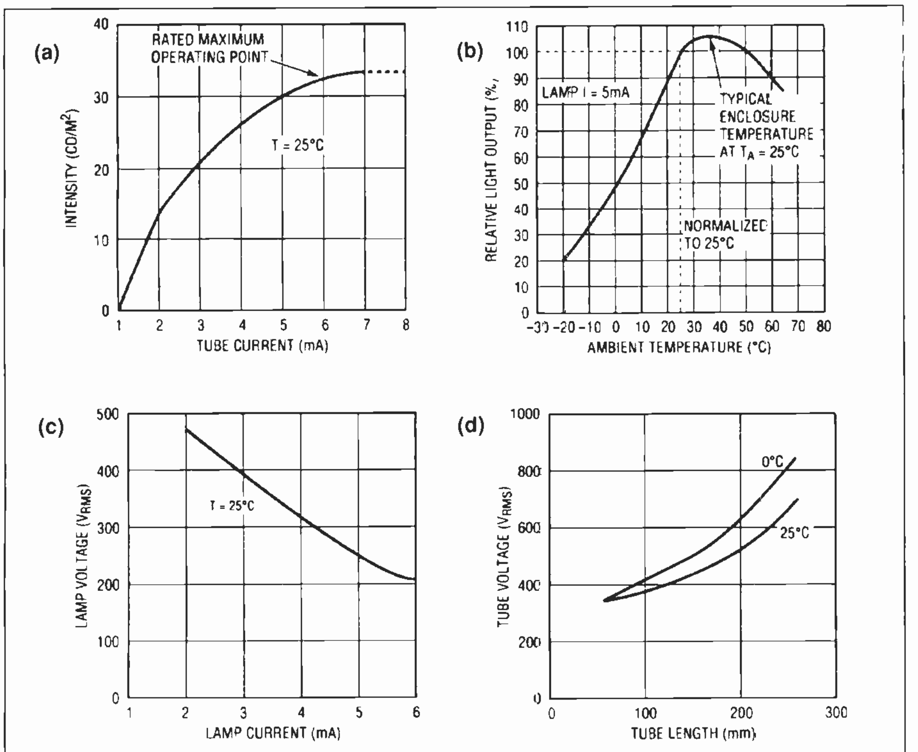
COILTRONICS (305) 781-8900, SUMIDA (708) 956-0666

Many liquid crystal displays operate from battery supplies so power consumption is an important issue. This circuit drives two cold-cathode fluorescent backlighting lamps at 92% efficiency. It also features dimming and shutdown facilities to help maximise battery life.



Cold-cathode fluorescent lamps for LCD backlighting present a complex load, as these charts show. Emissivity for a typical 6mA lamp shows how excessive current is wasteful, (a). Curve (b) illustrates how worthwhile it is to ensure that the lamp does not overheat while (c) indicates that voltage over the lamp falls rapidly with increasing current. How tube length affects operating voltage is outlined in (d) for normal and cold operating temperatures.

Linear Technology, *Coliseum Business Centre, Riverside Way, Camberley, Surrey GU15 3YL. Tel. 0276 677676.*

AMSTRAD DMP4000 Entire printer assemblies including printhead, platen, cables, stepper motors etc. Everything bar the electronics and case. Good stripper!! Clearance price just £5 REF: MAG5 or 2 for £8 REF: MAG8

VIEWDATA SYSTEMS Brandnew units made by TANDATA complete with 1200/75 built in modem, infra red remote controlled keyboard BT approved, Prestel compatible, Centronice printer port, RGB colour and composite output (works with any TV) complete with power supply and fully cased. Price is just £20 REF: MAG20 Also some customer returned units available at £10 each REF: MAG10

PPC MODEM CARDS. These are high spec plug in cards made for the Amstrad laptop computers. 2400 baud dial up unit complete with leads. Clearance price is £5 REF: MAG5P1

INFRA RED REMOTE CONTROLLERS Originally made for hi spec satellite equipment but perfect for all sorts of remote control projects. Our clearance price is just £2 REF: MAG2

TOWERS INTERNATIONAL TRANSISTOR GUIDE. A very useful book for finding equivalent transistors, leadouts, specs etc. £20 REF: MAG20P1

SINCLAIR C5 MOTORS We have a few left without gearboxes. These are 12v DC 3,300 rpm 6"x4", 1/4" OP shaft. £25 REF: MAG25

UNIVERSAL SPEED CONTROLLER KIT Designed by us for the above motor but suitable for any 12v motor up to 30A. Complete with PCB etc. A heat sink may be required. £17.00 REF: MAG17

VIDEO SENDER UNIT. Transmits both audio and video signals from either a video camera, video recorder, TV or Computer etc to any standard TV set in a 100' range! (tune TV to a spare channel) 12v DC op. Price is £15 REF: MAG15 12v psu is £5 extra REF: MAG5P2

***FM CORDLESS MICROPHONE** Small hand held unit with a 500' range! 2 transmit power levels. Reqs PP3 9v battery. Tuneable to any FM receiver. Price is £15 REF: MAG15P1

LOW COST WALKIE TALKIES Pair of battery operated units with a range of about 200'. Ideal for garden use or as an educational toy. Price is £8 a pair REF: MAG 8P1 2 x PP3 req'd.

***MINATURE RADIO TRANSCEIVERS** A pair of walkie talkies with a range of up to 2 kilometres in open country. Units measure 22x52x155mm. Complete with cases and earpieces. 2xPP3 req'd. £30.00 pair REF: MAG30.

COMPOSITE VIDEO KIT. Converts composite video into separate H sync, V sync, and video. 12v DC operation. £8.00 REF: MAG8P2.

LQ3600 PRINTER ASSEMBLIES Made by Amstrad they are entire mechanical printer assemblies including printhead, stepper motors etc etc In fact everything bar the case and electronics, a good stripper! £5 REF: MAG5P3 or 2 for £8 REF: MAG8P3

PHILIPS LASER 2MW helium neon tube. Brand new full spec £40 REF: MAG40. Mains power supply kit £20 REF: MAG20P2. Fully built and tested unit £75 REF: MAG 75.

SPEAKER WIRE Brown two core, 100 foot hank £2 REF: MAG2P1

LED PACK of 100 standard red 5mm leds £5 REF: MAG5P4

JUG KETTLE ELEMENTS good general purpose heating element (about 2kw) Ideal for all sorts of heating projects etc. 2 for £3 REF: MAG3

UNIVERSAL PC POWER SUPPLY complete with flyleads, switch, fan etc. Two types available 150w at £15 REF: MAG15P2 (23x23x23mm) and 200w at £20 REF: MAG20P3 (23x23x23mm)

OZONE FRIENDLY LATEX 250ml bottle of liquid rubber, sets in 2 hours. Ideal for mounting PCB's, fixing wires etc £2 each REF: MAG2P2

***FM TRANSMITTER** housed in a standard working 13A adapter!! the bug runs directly off the mains so lasts forever! why pay £700? or price is £26 REF: MAG26 Transmits to any FM radio.

***FM BUG KIT** New design with PCB embedded coil for extra stability. Transmits to any FM radio. 9v battery req'd. £5 REF: MAG5P5

***FM BUG BUILT AND TESTED** superior design to kit, as supplied to detective agencies etc. 9v battery req'd. £14 REF: MAG14

TALKING COINBOX STRIPPER originally made to retail at £79 each, these units are designed to convert and ordinary phone into a payphone. The units we have generally have the locks missing and sometimes broken hinges. However they can be adapted for their original pupose or used for something else?? Price is just £3 REF: MAG3P1

100 WATT MOSFET PAIR Same spec as 2SK343 and 2SJ413(8A,140v,100w) 1 N channel and 1 P channel, £3 a pair REF: MAG3P2

VELCRO 1 metre length of each side 20mm wide (quick way of fixing for temporary jobs etc) £2 REF: MAG2P3

MAGNETIC AGITATORS Cosisting of a cased mains motor with lead. The motor has two magnets fixed to a rotor that spin round inside. There are also 2 plastic covered magnets supplied. Made for remotely stirring liquids! you may have a use? £3 each REF: MAG3P3 2 for £5 REF: MAG5P6

TOP QUALITY SPEAKERS Made for HI FI televisions these are 10 watt 4R Jap made 4" round with large shielded magnets. Good quality general purpose speaker. £2 each REF: MAG2P4 or 4 for £6 REF: MAG6P2

TWEETERS 2" diameter good quality tweeter 140R (would be good with the above speaker) 2 for £2 REF: MAG2P5 or 4 for £3 REF: MAG3P4

AT KEYBOARDS Made by Apricot these quality keyboards need just a small modification to run on any AT, they work perfectly but you will have to put up with 1 or 2 foreign keycaps! Price £6 REF: MAG6P3

XT KEYBOARDS Mixed types, some returns, some good, some foreign etc but all good for spares! Price is £2 each REF: MAG2P6 or 4 for £6 REF: MAG6P4

PC CASES Again mixed types so you take a chance next one off the pile £12 REF: MAG12 or two identical ones for £20 REF: MAG20P4 component pack bargain 1,000 resistors +1,000 capacitors (all same value) £2.50 a pack REF: MAG2P7

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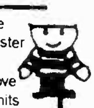

COMMODORE MICRODRIVE SYSTEM mini storage device for C64's 4 times faster than disc drives, 10 times faster than tapes. Complete unit just £12 REF: MAG12P1

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HEADPHONES 16P These are ex Virgin Atlantic. You can have 8 pairs for £2 REF: MAG2P8

PROXIMITY SENSORS These are small PCB's with what look like a source and sensor LED on one end and lots of components on the rest of the PCB. Complete with fly leads. Pack of 5 £3 REF: MAG3P5 or 20 for £8 REF: MAG8P4

FIBRE OPTIC CABLE Made for Hewlett Packard so pretty good stuff! you can have any length you want (min5m) first 5m £7 REF: MAG7 thereafter £1 a metre (ie 20m is £22) REF: MAG1 Max length 250m

SNOOPERS EAR? Originall made to clip over the earpiece of telephone to amplify the sound-it also works quite well on the cable running along the wall! Price is £5 REF: MAG5P7

DOS PACKS Microsoft version 3.3 or higher complete with all manuals or price just £5 REF: MAG5P8 Worth it just for the very comprehensive manual! 5.25" only.

DOS PACK Microsoft version 5 Original software but no manuals hence only £3 REF: MAG3P6 5.25" only.

FOREIGN DOS 3.3-German,French,italian etc £2 a pack with manual 5.25" only. REF: MAG2P9

MONO VGA MONITOR Made by Amstrad, refurbished £49 REF: MAG49

CTM644 COLOUR MONITOR Made to work with the CPC464 home computer. Standard RGB input so will work with other machines. Refurbished £59.00 REF: MAG59

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HAND HELD TONE DIALLERS Ideal for the control of the Response 200 and 400 machines. £5 REF: MAG5P9

PIR DETECTOR Made by famous UK alarm manufacturer these are hi spec, long range internal units. 12v operation. Slight marks on case and unboxed (although brand new) £8 REF: MAG8P5

WINDUP SOLAR POWERED RADIO AM/FM radio complete with hand charger and solar panel! £14 REF: MAG14P1

COMMODORE 64 Customer returns but ok for spares etc £12 REF: MAG12P2 Tested and working units are £69.00 REF: MAG69

COMMODORE 64 TAPE DRIVES Customer returns at £4 REF: MAG4P9 Fully tested and working units are £12 REF: MAG12P5

COMPUTER TERMINALS complete with screen, keyboard and RS232 input/output. Ex equipment. Price is £27 REF: MAG27

MAINS CABLES These are 2 core standard black 2 metre mains cables fitted with a 13A plug on one end, cable the other. Ideal for projects, low cost manufacturing etc. Pack of 10 for £3 REF: MAG3P8 Pack of 100 £20 REF: MAG20P5

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MICROWAVE TIMER Electronic timer with relay output suitable to make enlarger timer etc £4 REF: MAG4P4

PLUG 420? showing your age? pack of 10 with leads for £2 REF: MAG2P11

MOBILE CAR PHONE £5.99 Well almost! complete in car phone excluding the box of electronics normally hidden under seat. Can be made to illuminate with 12v also has built in light sensor so display only illuminates when dark. Totally convincing! REF: MAG6P6

ALARM BEACONS Zenon strobe made to mount on an external bell box but could be used for caravans etc. 12v operation. Just connect up and it flashes regularly) £5 REF: MAG5P11

FIRE ALARM CONTROL PANEL High quality metal cased alarm panel 350x165x80mm. Comes with electronics but no information. £15 REF: MAG15P4

SUPER SIZE HEATSINK Superb quality aluminium heatsink 365 x 183 x 61mm, 15 fins enamble high heat dissipation. No holes! £9.99 REF: MAG10P1P

REMOTE CONTROL PCB These are receiver boards for garage door opening systems. You may have another use? £4 ea REF: MAG4P5

LOPTX Line output transformers believed to be for hi res colour monitors but useful for getting high voltages from low ones! £2 each REF: MAG2P12 bumper pack of 10 for £12 REF: MAG12P3.

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0.7μm cmos gate arrays. GPS announces the *CLA80000* 0.7μm cmos family of low-power gate arrays, having a power dissipation of 1.3μW/MHz at 3V. Largest in the series has 300 000 usable gates. Delay of a two-input Nand is 210ps and novel core cell design allows a compact design of elements such as static rams. Mixed voltages supply the core and i/o to minimise power consumption. GEC Plessey Semiconductors, 0793 518510.

Telecomms switching. TI's *TGB2000E* gate array is meant for the telecommunications market, in which it allows switching systems to run high-level functions at 60% less power. It is derived from the standard *TGB1000* BiCMOS array, but is for 622.08MHz systems (STM-4). Embedded macros enable signal conditioning on-chip, eliminating the separate ECL or GaAs chip formerly needed. Texas Instruments, 0234 223252.

A-to-D & D-to-A converters

Low-power A-to-Ds. Two analogue-to-digital converters from Micro Call, *LTC1286/1298*, are in 8-pin, small-outline packages and draw 3μA standby current. These 12-bit devices are successive-approximation types, using 80μA when active and shutting down when not converting. S/H is on-board and conversion time is 48μs at 15kHz sampling rate, interfacing to most 3-wire serial ports. Micro Call Ltd, 0844 261939.

Discrete active devices

GaAs power fets. Harris Microwave Semiconductors introduce the *HMF-12020* gallium arsenide power fet, which offers 2-12GHz frequency range and output power at 1dB compression of 27.5dBm at 12GHz, gain at this frequency being 5dB. *HMF24020* has a similar range, but increased power output of 30.5dBm and gain of 4dB. Packaging is metal/ceramic. Anglia Microwaves Ltd, 0277 630000.

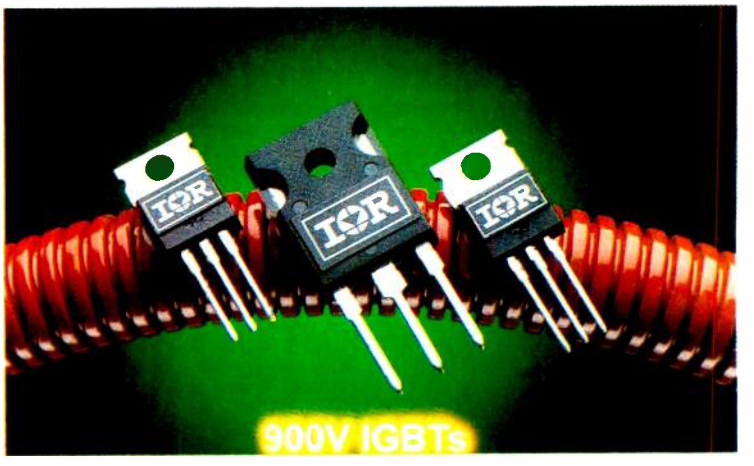
Fast, 500V mosfet. With switching times of 5ns and a 500V breakdown voltage, Harris's *RFV10N50BE* mosfet handles 10A and switches eight times faster than comparable devices, in which a 40ns fall time has been the fastest. The package contains the high-voltage mosfet, a control mosfet, a separate source Kelvin terminal and protective zeners. On resistance is 0.48Ω and input capacitance 3800pF. Harris Semiconductor (UK), 0276 686886.

Green/yellow led. Producing a greenish-yellow light, HP's *HLMA-CP00* 1000mcd led has an 8° viewing angle at 20mA. The company has, with this addition to the range of high-brightness devices, all three of the popular colours for indicators, all being suitable for outdoor use. Hewlett-Packard Ltd, 0344 362277.

Blue leds. Silicon carbide leds by IMO generate true blue light peaking at 470nm. They are available in clear or diffused 3mm or 5mm packages with viewing angles of 16 and 28° in the clear versions or 34 and 42° in the diffused type. Also announced are 3mm GaAlAs and GaP leds emitting red or green light at sufficient brightness for outdoor use. IMO Precision Controls Ltd, 081 452 6444.

Small, 60V mosfets. Three devices, the first in the Siliconix *Little Foot* family of surface-mounted power mosfets, are on release. All rated at 60V, the single p-channel *Si9407DY*, the dual n-channel *Si9945DY* and the *Si9948DY* dual p-channel offer 100mΩ-250mΩ on resistance and are designed for 4.5V gate drive. Siliconix, 0344 485757.

P-channel IGBT. Zetex's *ZCN0545* n-channel insulated-gate bipolar transistor now has a p-channel stablemate – the *ZCP0545A*, in a TO92 package. Both are 450V devices and have turn-on and turn-off times of 150ns and 350ns, handle a continuous 0.37A and have an input capacitance of 120pF. Gate/source threshold is 3.5V and drain/source saturation is 3V at 0.5A, with 6Ω on resistance. Zetex plc, 061-627 5105.



900V IGBT. IR now has a family of fast 900V insulated-gate bipolar transistors, providing power dissipation of 60-200W at a case temperature of 25°C. *IRGBF20F/30F/40F/50F* are in TO-220 and TO-247 and take 31-51A in the latter package, switching losses being 2.9mJ and 1.57mJ for 51A and 31A devices. International Rectifier, 0883 714234.

Linear integrated circuits

LDO voltage regulators. A surface-mounted low dropout 5V regulator, the Allegro *A8181*, provides a fixed 5V at over 500mA or 1A at 20% duty cycle, while input/output differential can be less than 300mV. Consumption is 120μA and line input between 5.5V and 10V. Flint Distribution Ltd, 0530 510333.

Phase control. GEC Plessey's *TDA2086* phase-control device is meant for use in AC closed-loop or open-loop circuitry with either resistive or inductive loads. Its –15V shunt regulator can be powered by AC or a 12V DC supply and a –5V output is provided. On-chip average or peak load-current limiting is included, as is a ramp generator to give controlled acceleration. Output triac pulses are negative. Gothic Crellon Ltd, 0734 788878.

Current-mode multiplier. Two high-speed current-mode, four-quadrant multipliers from Elantec, the *EL4083/4*, provide high isolation switching, low distortion and operation from ±5V to ±15V rails. They are said to be the first current-in/differential current-out devices to be produced and are intended mainly for HDTV gain control use. Kudos Thame Ltd, 0734 351010.

3-state op-amp. TI claims its *TLE2301* to be the first wide-band op-amp in a single package to have a three-state output. It will sink and source 1A and has a gain/bandwidth of 8MHz; THD is 0.04%. Texas Instruments, 0234 223252.

Voltage references. Five IC precision references in the Zetex *ZRT* series cover the 2.5-9.8V range, producing only 50μV of output noise and with a temperature coefficient of 15ppm/°C. Current handling of the 5V device is 0.15-60mA and there is a pin for output trim by an external potentiometer. Zetex plc, 061-627 5105.

Logic building blocks

DDS+DAC chip. Analog's *AD7008* is a direct digital synthesis circuit with an integral D-to-A converter for high-performance frequency synthesis. It combines a numerically controlled oscillator with a 32-bit phase accumulator, sine and cosine look-up tables and a 10-bit D-to-A converter. Clock rate is up to 50MHz and serial and parallel interfaces operate independently and asynchronously from the DDS clock. Spurious-free dynamic range is –70dB, S:N 50dB and THD –55dB. Analog Devices Ltd, 0932 253320.

Prescalers. For use on portable equipment, GEC Plessey's *SP8714/5 1.1* and 2.1GHz prescalers take only 3.6mA and 6.8mA, reducing to less than 30μA on standby. A "push-pull" output stage allows a nearly 50:50 M:S ration at the output, with no load resistor. Modulus control input signal is latched with the device output to improve setup time. *SP8714* offers 32/33 and 64/65 division, while *SP8715* divides by 64/65 and 128/129. GEC Plessey Semiconductors, 0793 518510.

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3.2ns logic. IDT's *E-Speed* double-density logic devices offer propagation delays of 3.2ns and use less power than any other logic family. *IDT74FCT16XXXT* devices have high current output and the *IDT74FCT162XXXT* types balanced output drive, the former possessing a power-off disable allowing power to be applied to inputs, outputs or i/os even when the supply rail is absent and the ±24mA balanced drive type has integrated series terminating R for capacitive loads, also reducing ground bounce to 600mV. Integrated Device Technology, 0372 363734.

Dual fifos. Features and performance of two synchronous first-in-first-out registers are contained in one 20ns 4K by 9 by 2 *IDT2841*, the first member of IDT's double-wide 9-bit wide dual *SyncFIFOs*, available in 64-pin thin quad flat packs. Integrated Device Technology, 0372 363734.

Single-chip EIA-232. *SN75LBC187* and '241 by TI support the 9-pin D-type EIA232 serial interface, containing multiple drivers and receivers and forming a one-chip solution. The '187 supports data rates beyond 116kb/s and both devices have internal charge pumps and a shutdown facility to 10μA. Packaging is the 28-pin wide-body SOIC for the '241 and 28-pin SSOP for the '187. Texas Instruments, 0234 223252.

Memory chips

4Mb video rams. Toshiba's range of video rams is augmented by the 0.6μm 4Mb rams, *TC524 162/262/165/265 SF/FT/TR* x16-organised memories. Access times are 60ns at 5V or 80ns at 3.3V. By using the pipe-lined fast page mode, cycle times can be reduced from 115ns to 40ns. A 512 by 16 serial memory is included. 2Mb types are also offered. Toshiba Electronics (UK) Ltd, 0276 694600.

Mixed-signal ICs

MPU supervisors. AD's *ADM69X* series monitor microprocessor power supplies and take necessary action when they drop below specified levels. Pin-compatible chips are available, but these use 80% less power at 5mW and give 100mA output current, in addition to a 5ns chip-enable propagation delay and 50ms supply-to-reset response. Functions include backup battery switching, watchdog timing, cmos ram write protection and power failure alert. Analog Devices Ltd, 0932 253320.

Oscillators

SM clock oscillator. AVX's *K50* series of ceramic-packaged, surface-mounted clock oscillators are claimed to be the world's smallest at 7 by 5 by 1.8mm and come in cmos, TTL and 3.3V versions. These tri-state devices cover the 1.5-50MHz range with stabilities of 50-100ppm. Supply current at 50MHz is between 30 and 40mA, depending on model. AVX Ltd, 0252 336868.

S-band VCO. In the range 2.6-3GHz, the *C-810* voltage-controlled oscillator by Z-Comm offers a 400MHz tuning bandwidth for a 0-12V tuning voltage, with 90% linearity. An output of 15dBm±2dBm into 50Ω suits low-level mixers and phase noise is –95dBc/Hz at 10kHz. Eurosource Electronics Ltd, 081 977 1105.

Clock oscillators. IQD's clock oscillators are now specified at 25°, rather than an overall frequency tolerance quoted between 0 and 70°C. Adjustment can be as close as ±5ppm for 3V and 5V types at frequencies in the 250kHz-70MHz range (3V types from 4MHz). IQD Ltd, 0460 77155.

Programmable logic arrays

FPGAs. Actel's *ACT 2* family of field-programmable gate arrays now costs less and performs better, after a process shrink from 1.2μm to 1μm resulted in a 25% speed improvement. As an example, the *A1225A-2 2500* reaches data-path speeds of 105MHz, 66MHz in a 16-bit counter a system speed of 50MHz. Actel Europe Ltd, 0256 29209.

Fast 84-pin EPLD. Latest member of Altera's *MAX7000* family of erasable programmable logic devices is the 64-macrocell *EPM7064*, which offers 7.5ns single-level logic delays and 125MHz in-system performance. It is supported by the *MAX+PLUS II* development software for PCs. Altera UK Ltd, 0628 488811.

APLA. Intel's *iFX780* field-programmable gate array is the first in the company's *FLEXlogic* family and incorporates flexible memory and logic options in a low-power chip, as easy to use as a conventional PLD. Eighty macrocells are organised as eight independently configurable function block, internal logic carrying out the configuration. Pin-to-pin delays are 10ns and there are 12 clocking options. I/o of each block is independently operable at either 3.3V or 5V. Jermyn Distribution, 0732 743743.

Fastest 28-pin PLD. Lattice Semiconductor's *GAL 26CV12C* is claimed to be the fastest 28-pin PLD available, running at clock frequency of 142.8MHz. It takes a typical 90mA supply current and provides 1.2 times the logic density of the standard *GAL 22V10*, being contained in either 28-pin dip or PLCC packages with centre-pin supply and ground. Micro Call Ltd, 0844 261939.

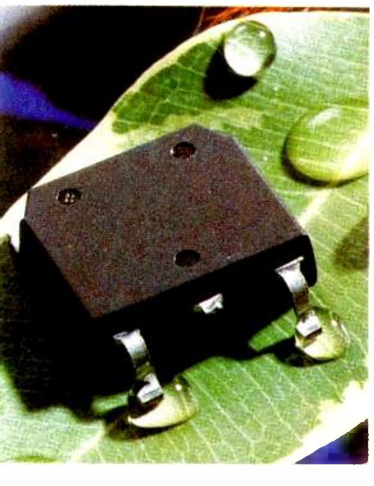
Power semiconductors

Step-down switcher. Maxim's *MAX727/8/9* are 5V, 3.3V and 3V DC-to-DC switching regulators working from 8-40V input and rated at 2A. An on-chip oscillator removes the need for a large number of external components. Cycle-by-cycle current limiting protects against overcurrent and output shorts and there is micropower shutdown and adjustable current limiting. Maxim Integrated Products Ltd, 0734 845255.

Micropower LDO regulator. National says its *LP2956* is the first dual, micropower, low dropout regulator, with 470mV dropout, 170μA quiescent current and 250mA output and provided with shutdown pin, error flag pin, auxiliary comparator and an additional 75mA regulator to ensure data retention during system shutdown. *LP2957* is a fixed 5V, 250mA LDO regulator in a TO-220 package for higher power. National Semiconductor, 0793 697592.

IGBTs. A new silicon structure developed by Toshiba is used in the *MG30/90/180V2YS40* and *MG240/360V1US41* insulated-gate bipolar power transistors to provide operating voltages of 1700V at up to 360A. The 30, 90 and 180A types are dual half bridges and the 240 and 360A versions single IGBTs. These devices hard switch at up to 20kHz. Saturation voltage is 3.2V. Toshiba Electronics (UK) Ltd, 0276 694600.

Power mosfet. Housed in the new *HDPAK* surface-mounted package for high-power transistors, Hitachi's *2SK2174* is rated at 500V and 20A, but has an on resistance of 0.22Ω at 10V and high-speed switching. Hitachi Europe Ltd, 0628 585000.



PASSIVE

Passive components

Ceramic capacitors. New packages for Kyocera's ceramics designed for use in switched-mode power supplies are in radial, four-terminal and dual-in-line form in both through-hole and SM types. Finish is dipped, lacquered, back-fill boxed or uncoated. Other types such as screw fixing being available to order. AVX Ltd, 0252 336868.

Thick-film resistors. When high-voltage transients occur, as in inductive switching, laser trimming across the resistor body can cause localised hot spots and cracking. Murata's new components are trimmed longitudinally, leaving no weak points and achieving a tolerance of ±0.2%. Components are made to customers' requirements. Murata Electronics (UK) Ltd, 0252 811666.

Chip coil. *LQP21A* ultra-miniature chip coils by Murata are made in thin-film form to obtain a ±5% tolerance and low stray capacitance. Self-resonant frequency is over 2GHz at 8nH, minimum Q is 10 at 500MHz, resistance is between 1Ω and 2Ω, depending on value and maximum current 100mA. Package size is 2 by 1.25 by 0.5mm, surface mounted. Murata Electronics (UK) Ltd, 0252 811666.

3.3F backup capacitor. NEC's *Supercaps* are extremely high-value capacitors intended to replace batteries in backing up cmos circuitry. Values are as high as 3.3F and a 256-bit ram, for example, can be supported for 50 hours by a 2.2F *Supercap*. Reliability is ensured by the method of charge storage – at the interface between activated carbon and sulphuric acid – and NEC claim that there is no limit to the number of allowable charge/discharge cycles. NEC Electronics (UK) Ltd, 0908 691133.

Crystals. *Micro-Crystal* oscillators are made by means of an advanced photolithographic technique, which results in increased resistance to shock and vibration and confers low ageing characteristics. Oven-controlled, voltage-controlled and standard clock oscillators are offered in the range 100kHz-50MHz, depending on model, and the oscillators are contained in dil or ceramic packages. The company offers a custom design service. Stanler Components Ltd, 0376 340902.

Line-match transformers. *MTLM-1200* series line-matching transformers from microSpire feature a return loss specification that exceeds BS415, 624 and 6301 and are approved to BABT/EN41003. Transformer return loss is 16dB or better over 0.2-4kHz, (24dB in-network) and 26dB over 0.2-3kHz. Distortion is 0.1% or better. At DC, dielectric strength in 1min tests is 7kV – 4kV RMS. As standard, impedance is 600Ω, but others are available. Surtech Interconnection Ltd, 0256 51221.

EMI filters. The smallest member of TDK's *ACB* range of compact, surface-mounted, interference-suppression filters measures only 1.6 by 0.8mm and provides 120Ω impedance at 100MHz. Other models in the range exhibit 40-600Ω at 100MHz. Resistance of 0.3-1.3Ω and current ratings of 0.1-0.5A enable their use as signal-line noise suppressors. TDK UK Ltd, 0737 772323.

EMC protection. *FiltAr* by Telematic combines RFI filtering, surge and ring suppression, which eliminates ringing caused by surges and transients. Telematic Systems Ltd, 0727 833147

Displays

Display evaluation kits. Lascar's *DMXC3* is a complete dot-matrix and graphics controller, acting as an Ascii terminal for character modules or producing a bit pattern for the graphics module. An optional second rom allows stored messages or pictures to be displayed by way of the serial or parallel port. *EVAL3* and *EVAL3G* are evaluation kits including graphics and character LCD, the *DMX3C*, cable, bezel kits and software. Connection to the PC is via an RS232 port. Verospeed, 0703 644555.

Hardware

PCB milling. Gravograph's *VXM* and *IS* engraving and milling machines will produce prototype and small batch circuit boards when driven by Gerber files from a PC, no photography or chemicals being involved. The machines are also suitable for milling, cutting and engraving front panels. Gravograph Ltd, 071-511 5901.

PCB repairs. Royel has a device to assist with the replacement of components on multilayer boards, avoiding copper delamination and glass-fibre breakdown. The ramp-up Hot Air Preheater *PH9000* supplies hot air/gas through a small aperture, its temperature being closely controlled by thermocouple. An audible signal indicates that a threshold temperature is reached, whereupon a soldering iron supplies the small extra temperature for the repair. Production Equipment Sales Ltd, 0323 811694

Instrumentation

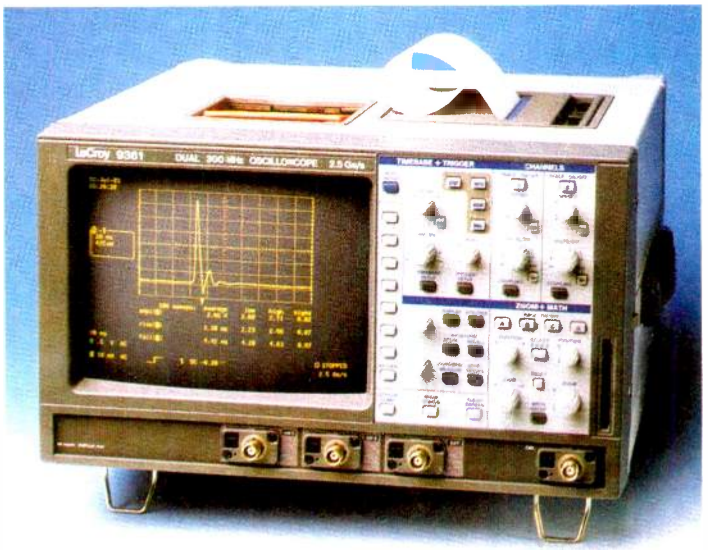
DSO/logic analyser. A low-cost digital storage oscilloscope and logic analyser made by Link Graphics Inc. samples at up to 200Msample/s with eight 100MHz logic channels. The triggering circuitry allows analogue events affecting logic and vice versa to be captured and shown for correlation. A 4K-deep sample buffer stores data and analogue information before, after or either side of the trigger. PC card based the unit is supplied with a software interface that will save configuration and waveform data to disk. Computer Solutions Ltd, 0932 829460.

60MHz oscilloscope. Hitachi Denshi's *V-680* 60MHz cursor-readout real-time oscilloscope has three channels, six traces and delayed sweep and cost £750. Setting values are displayed on-screen and the cursors provide direct readout of voltage, time and frequency. Maximum sweep speed is 5ns/div. and Y sensitivity 100mV/div. Trigger hold-off is provided, as is a tv sync. separator. Hitachi Denshi (UK) Ltd, 081-202 4311.

Current-sensing shunts. Four-terminal current-sensing shunts in the *PLV* range by Kynmore covers the 0.005Ω-100Ω range with 0.005% tolerance at 25°C, temperature coefficient 0±15ppm/°C and temperature span 65°C to 275°C. A typical component of 10mΩ±1% at 10W carrying 30A changes resistance by less than 0.1%, with no measurable EMF change between the copper terminals. Kynmore Engineering Co. Ltd, 071 405 6060.

Oscillographic recorder. Martron's *ORP1200* recorder is the first of a range designed to use thermal paper rather than the more expensive ultra-violet-sensitive type, producing A4 or A5 output. *ORP1200* offers 100ksample/s sampling, 14-bit resolution and a range of recording, display and memory functions. It is available with four or eight channels, with a high-voltage AC module and a high-sensitivity 14-bit input module with signal conditioning, an additional option being the recording of 16 channels of logic alongside the analogue traces. Martron Instruments Ltd, 0494 459200

Functional test. *TR-6* from R&S is a single PC expansion card, combining digital multimeter, counter/timer, function generator, DC source, relay switching and digital i/o, the card working as a stand-alone unit or with the *TR-4* Checksum manufacturing defects analyser to form a low-cost system. Software is supplied. Rohde & Schwarz UK Ltd, 0252 811377.



Literature

AT&T. AT&T Microelectronics's 140-page selection guide lists components concerned with telecomms, computers, cellular and data comms and disk drives. Circuit application is included. AT&T Microelectronics 0732 742999.

SMPS catalogue. Calex has split its catalogue into three parts, covering linear, DC-to-DC and switched-mode units, this being the last. Notable in the new publication is the *72000* series, which is flexible in configuration and produces up to 250W. Calex Electronics Ltd, 0525 373178.

Power supplies

Low-noise PSUs. Gresham's *GEM 392* and *393* miniature power supplies use linear techniques rather than switched-mode methods to achieve a 1mV RMS output noise. Three outputs are 5V-1A, +12V-150mA and 5V-1A and ±15V-150mA, with stabilisation of 0.05% and regulation 0.2% for a full-load change. Chassis or PCB-mounted versions are available and solder-pin spacing is to European or US standards. Gresham Power Electronics Ltd, 0722 413060.

PSU chips. Voltage detectors and voltage regulators used in Seiko's watches are now offered to the industrial market. In the SOT89 package (4.5 by 4.25mm footprint), the *SCI 7700* detectors cover 0.9V to 5.3V at a quiescent current of 2µA, while the *SCI 7710* regulators produce –5V to 5V at a similar quiescent current on inputs up to 15V. A free copy of Seiko's catalogue is on offer. Hero Electronics Ltd, 0525 405015

300MHz DSO. By virtue of its two 2.5GS/s independent digitisers, LeCroy's *9361* dual-channel digital storage oscilloscope digitises all waveforms in one shot, instead of by repetitive sampling, also ensuring the accuracy of inter-channel time measurement. A range of trigger modes is available and options include basic or more advanced maths functions and an FFT package. Storage is by DOS-compatible floppy disk and a built-in printer is a further option. LeCroy Ltd, 0235 533114.

Faster radio modem. A new model of Wood & Douglas's *Surtel* 1200 and 2400baud radio modems, the *DGX450*, uses Gaussian minimum-shift keying to reach 9600baud in a 25kHz channel (4800baud in 12.5kHz). It operates on a single channel in any 20MHz band in the 400-500MHz region with a ±3ppm frequency stability, putting out 500mW from 12V. Packaging is either a desk-top type or dust and moisture-proof. Wood & Douglas Ltd, 0734 811444.

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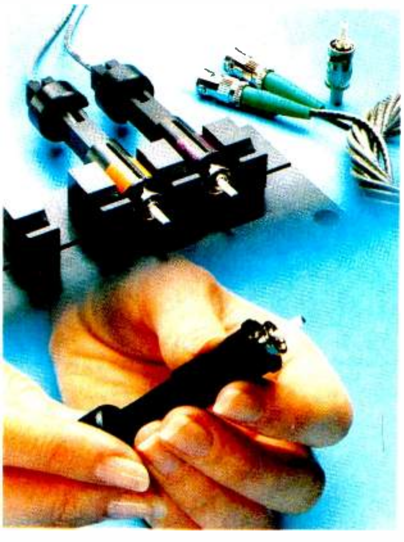


Connectors and cabling

Optical-fibre connectors. *Quick Shot* ST-compatible ramped-bayonet connectors by ITT Cannon offer fast, simple and safe termination of the fibre. A special holder eliminates the danger of burnt fingers, a stripped fibre being placed in the holder, which has temperature indicators, the whole going into an oven. When the epoxy is molten, the holder is taken out of the oven, a stripped fibre inserted and the assembly left to cool. The use of blue epoxy allows quick, one-stage polishing. ITT Cannon, 0256 473171.

Flat NiCd cells. Energy density of Saft Nife's flat prismatic nickel-cadmium cells is now increased by at least 5% to give over 30% better than cylindrical types. With 1.2V nominal voltage, the smallest *GP4* type now has 380mAh rated capacity and measures 47.5mm by 16.4mm by 5.6mm. The cells are now more freely available to industry. Saft Nife Ltd, 081 979 7755.

Radio communications products

SM power dividers. Leaded, surface-mounted two-, three-, and four-way power dividers by Synergy Microwave are available in bandwidths from 2MHz to 1000MHz, with 0.7dB typical insertion loss above the theoretical split loss. The *SLD* series has amplitude unbalance of 0.4dB, phase unbalance of 3° and isolation of 18-25dB between outputs. *SLQ* devices offer 3-1900MHz bandwidth with 0.2dB insertion loss and better amplitude and phase balance. Chronos Technology Ltd, 0989 85471.

Quadrature hybrids. *DQP* series quadrature hybrids from Synergy Microwave cover 10-500MHz with 5:1 bandwidths, offering 1dB insertion loss in the 5:1 band with a amplitude unbalance of 0.8dB. Phase balance is 4°, isolation 20dB and VSWR 1.5:1 on all ports. Chronos Technology Ltd, 0989 85471.

Discoidal filters. Oxley's *dBZ2* range of discoidal feedthrough filters provide up to 65dB of loss at 10GHz in a 50Ω system, without resonances. They fit a 3.5mm hole, are solder mounted and are hermetically or epoxy sealed. Voltage handling is 200V DC up to 85°C, derating to 100V up to 125°C. Values are 10pF-5nF. Oxley Developments Co. Ltd, 0229 52621.

Switches and relays

Solid-state relays. C P Clare has released the *140 Series* of solid-state relays, which are in 1 Form A and 2 Form A, handling 400V load (DC or AC peak), 250mA local current and having an on resistance of 6Ω. Switching speed is 1ms at 5mA drive current and the units are in 6-pin and 8-pin dips. C P Clare Corporation, 0460 41771.

Transducers and sensors

Digital pots. Control Transducers's *500 Series* of *Digipots* now includes models providing 540, 1000 and 1024 lines per revolution. These devices are non-contacting shaft encoders which convert rotary movement to digital form for input to counters or controllers, working continuously at up to 10 000rev/min, if necessary. Output is two-channel quadrature at TTL levels. Control Transducers, 0234 217704.

Tilt sensor. Dual sensitivity in the *Cline* angle transducer, selected by jumper, transforms the normal sensitivity of ±45° to ±10° when sensitivity is increased from ±60V/° to ±200mV/°. Two versions offer plus and minus analogue output or analogue ratiometric output. Accuracy is ±0.1% up to 10° and about 1% of reading at ±45°, with a 300ms time constant and frequency response of 0.5Hz. Kynmore Engineering Co. Ltd, 071 405 6060.

COMPUTER

Development and evaluation

HPVEE for Windows. H-P's *Visual Engineering Environment*, originally a Unix application, now runs under Windows for PCs. *HPVEE* is a programming language that allows users to create test programs by connecting icons with a mouse to give a speed increase over text entry as in Basic or C, although code written in that way can be integrated into *HPVEE*. Either 386/486 machines are needed. Hewlett-Packard Ltd, 0344 362277.

80C166 debugger. 80C166 family debuggers from Hitex come in at less than £2000 and are claimed to be the first at this level. *ROMlink166* does not use CPU serial ports, simply replacing an eprom or ram in the target to provide a direct connection to a PC printer port, via which code can be down-loaded to the *166* and debugged in situ. Source-level debugging of Keil and Tasking C compilers is possible via the *Turbo*-style *HiTOP* user interface. Hitex (UK) Ltd, 0203 692066.

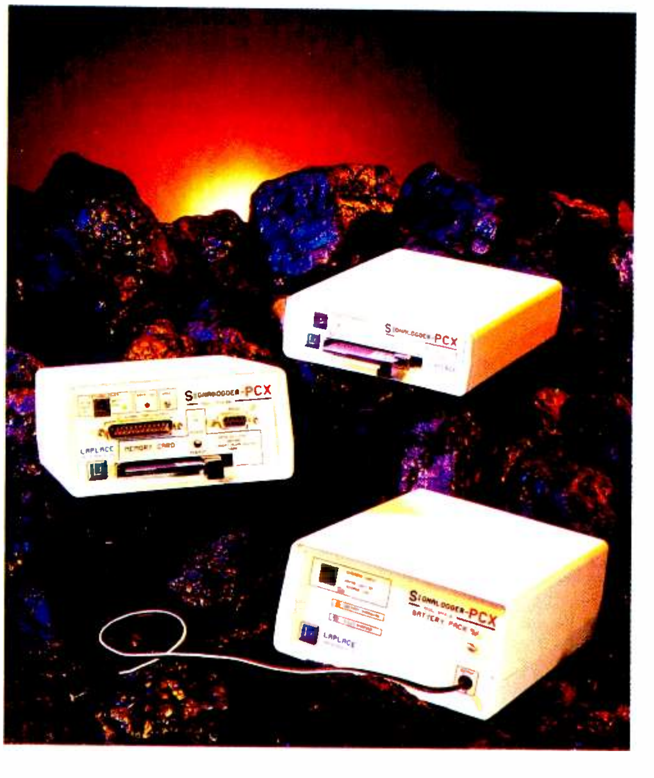
8051 development. *SDT-51* is a developer's kit for the 8051 microprocessor, produced by Logicom at a cost of £549. It includes a C compiler, relocatable macro-assembler, source language debugger and in-circuit emulator, needing only a PC with a text editor of some kind. The ICE supports single-step and continuous emulation, in which up to 800 break points are settable. Logicom Communications Ltd, 081 756 1284.

Software

FPGA synthesis. Actel's *Designer* field-programmable gate array software is now offered with the Innovative Synthesis Software *ACTMap* FPGA fitter, which provides a simple route from PALs to FPGAs. ACTMap converts *Palasm* or *EDIF* output into binary decision diagrams which are then decomposed into BDD representation of Actel's logic modules. Output is passed to automatic place-and-route software. Upgrades of *Designer* and its Windows version carry no additional charge. Actel Europe Ltd, 0256 29209.

Logic compiler. Stag claims to supply the "world's fastest and friendliest logic compiler" – *CUPL for Windows*, which is an FPGA and PLD compiler, the *CUPL* language supporting combinations of state-machine, truth table and Boolean entry methods. There are four different minimisers at varying levels, including Quine-McCluskey, and polarity optimisation. Output is in several formats, including *Open PLA*, *Palasm* and *XNF* for Xilinx. Stag Programmers Ltd, 0707 332148. ■

Data loggers. An entirely new range of data loggers, the *S-PCX* and associated equipment, is announced by Laplace Instruments. Two types of logger have eight analogue inputs, with an external battery pack, optional card reader and 64Kbyte-512Kbyte memory cards. Both are programmed and interrogated from a PC via the software provided. Any combination of 5, 1 and 20mA, thermistor, 1, 10 and 100mV and thermocouple can be handled, depending on model, with resolutions of 1 part in 1000 to an accuracy within ±1%. Laplace Instruments Ltd, 0692 500777.



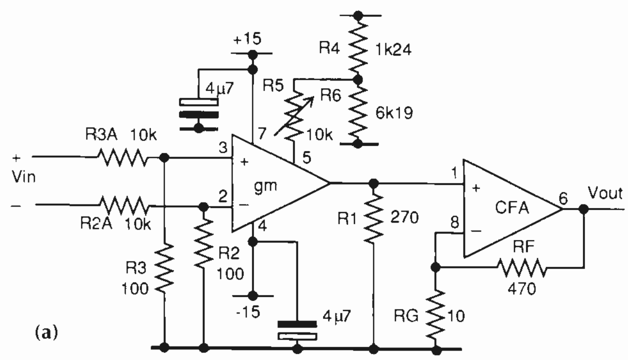
DESIGN BRIEF

Versatile twin amplifier has many uses

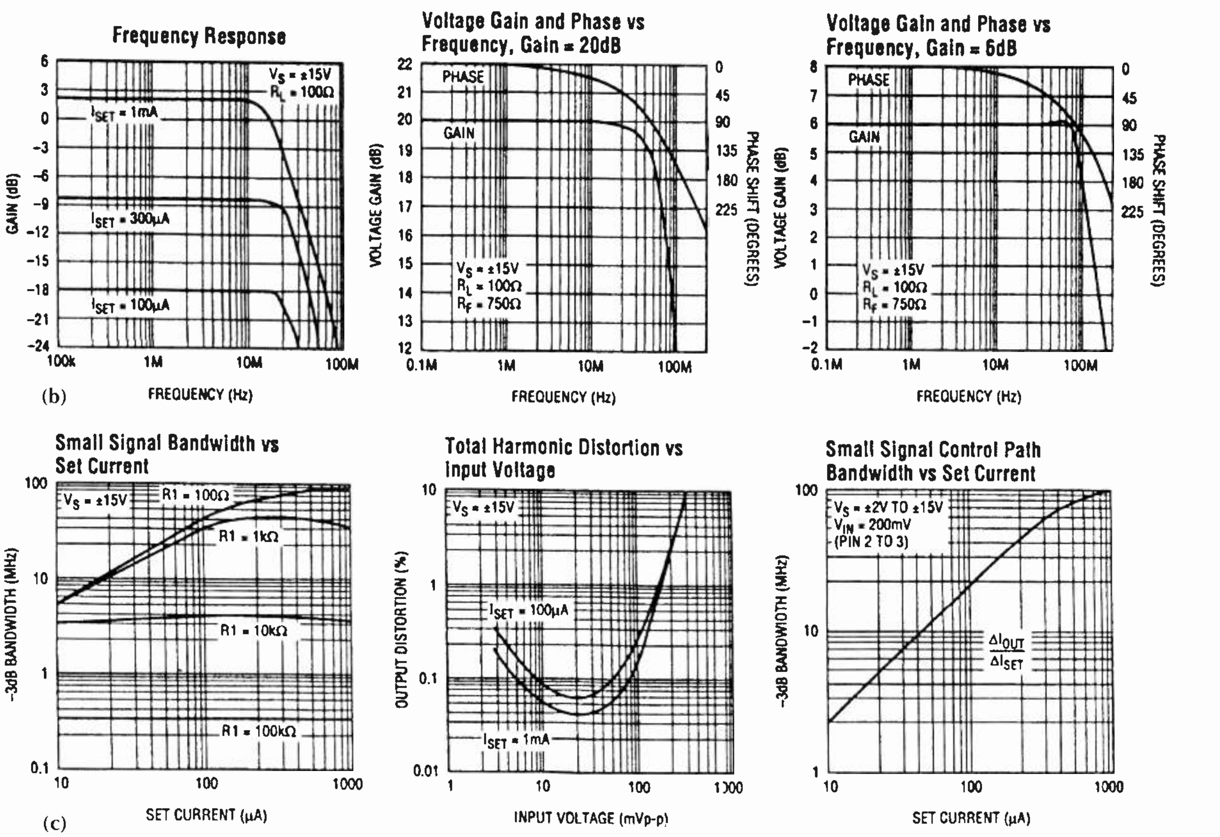
Combining a current-feedback amplifier in the same package as a transconductance amplifier produces a versatile building block, as Ian Hickman explains.

There are many dual op-amps available, but the subject of this design brief is not a dual, but rather a twin amplifier. The eight-pin *LT1228* from Linear Technology contains an operational transconductance amplifier (OTA) with a maximum bandwidth of 75MHz. Its second element is a useful current feedback amplifier, or CFA, with a bandwidth of 100MHz.

Single-ended current output of the transconductance amplifier is tied internally to the non-inverting input of the current-feedback amplifier, which can act as a buffer. This junction is also brought out to a pin. Since the non-inverting input resistance of the CFA is very



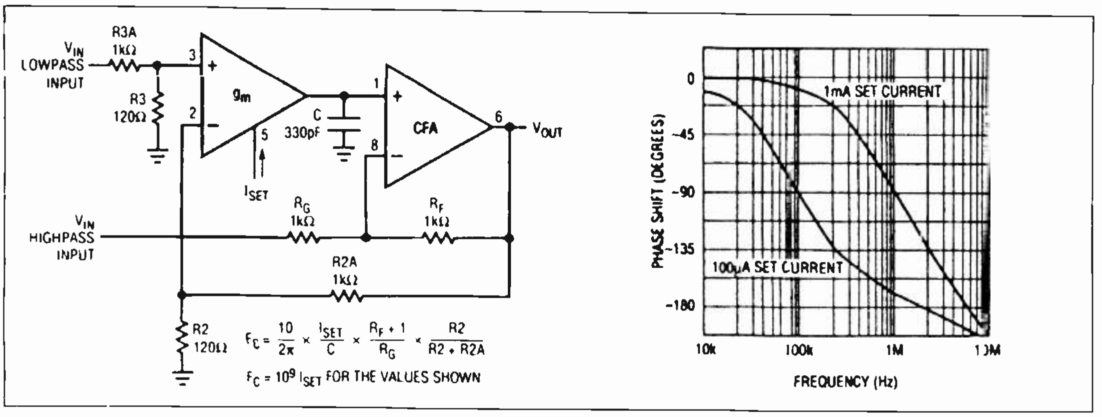
(a)



(b)

(c)

Fig. 1a. Electronic gain control is an ideal application for operational transconductance amplifiers. This design has a bandwidth of around 20MHz and is adjustable from –18 to +2dB. Curves in (b) show frequency characteristics for three CFA gains. Bandwidth of the OTA section is presented in (c)i, THD versus input level is illustrated in (c)ii and small—signal control—path bandwidth versus I_{set} is shown in (c)iii.



$$f_C = \frac{10}{2\pi} \times \frac{I_{SET}}{C} \times \frac{R_F+1}{R_G} \times \frac{R2}{R2+R2A}$$

Fig. 2. Operational transconductance amplifiers simplify single pole low, high and all-pass filter design. For low-pass operation the high-pass input is grounded and vice versa for high-pass. With the two inputs tied together, an all-pass response is obtained.

high, at typically 25MΩ, it may be ignored and the OTA used on its own if desired.

One of the more obvious applications for an OTA is as an electronically-controlled variable gain stage. **Figure 1a** shows such a circuit with an input resistance of 10kΩ, a gain range of −18 to +2dB and a −3dB bandwidth of around 20MHz. Its input may be differential as shown, or unbalanced, inverting or non-inverting, in which case R_{3A} or R_{2A} respectively may be omitted. Gain is directly proportional to I_{set}, the current into pin 5 of the device.

Compensation for two internal diode drops in the gain setting section is provided by the Thévenin source arrangement, R_4 and R_6. Assuming stabilised 15V rails, this arrangement ensures that any set gain remains constant within 1% over the device's full temperature range of −55 to +125°C.

Resistor values need changing if a different negative supply rail voltage is used. If the negative rail is not stabilised, compensation may be achieved via an *LT1004* negative 2.5V reference. Alternatively, for more accurate and linear control of gain, I_{set} may be supplied by a single op-amp voltage-to-current converter circuit.

The input attenuator ensures that the circuit can accept inputs up to 10V pk-pk. Mutual conductance g_m (output current divided by the voltage between pins 2 and 3, in mA/V) is $10xI_{set}$. In the circuit shown this flows in R_1, buffered by the high input impedance of the current-feedback amplifier.

At low frequencies, voltage gain of the current-feedback amplifier is $(R_f+R_g)/R_g$. This applies up to the frequency where the CFA's gain bandwidth product of about 1GHz becomes significant. How bandwidth of the CFA varies with demanded gain is shown in Fig. **1b**.

Overall, the gain A_v in Fig. 1a is given by

$$A_v=R_3/(R_3+R_{3A})\text{x}10\text{x}I_{set}\text{x}R_1\text{x}(R_f+R_g)/R_g.$$

If maximum expected input is less than 10V pk-pk, the 10kΩ resistor(s) at the input may be reduced, giving an increased A_v. If an increase in A_v is not needed, R_g may be increased. This demands less gain from the CFA and increases the circuit's bandwidth. However, any substantial increase in bandwidth may be limited by the bandwidth of the transconductance amplifier section, which is shown in Fig. **1c i**.

Total harmonic distortion of the transconductance amplifier as a function of input signal amplitude is shown in Fig. **1c ii**. In the application in Fig. 1a, I_{set} is basically a direct current whose value is adjustable for any desired gain. In some applications, such as **Fig. 6**, high-frequency signals may be inserted in the control path input at pin 5. Figure **1c iii** shows the small signal control path bandwidth versus I_{set}.

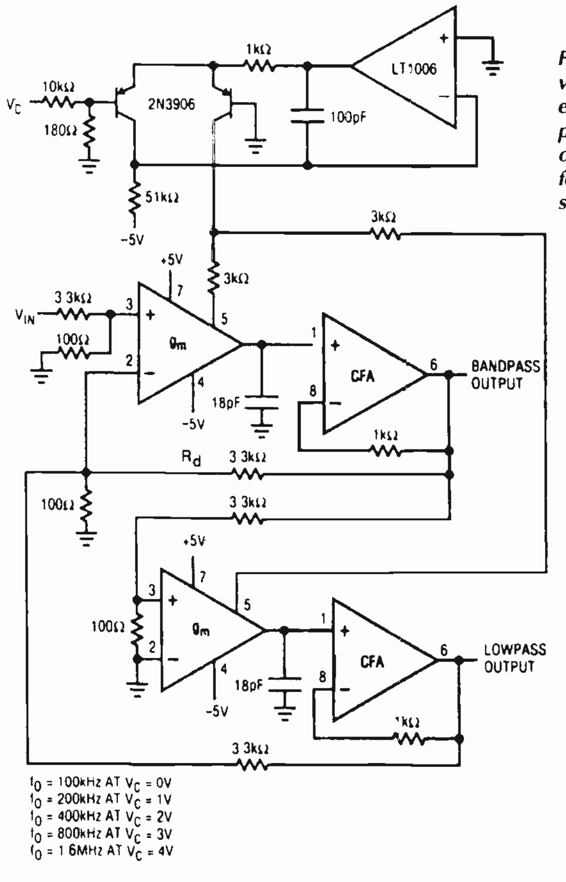


Fig. 3. Second-order state variable filter with electronic tuning and low-pass and band-pass outputs. This design features logarithmic tuning sensitivity.

Electronically tunable filters

Another major application for transconductance amplifiers is electronically tuned filters. A single-pole filter is the simplest possible type, offering a flat pass-band with a −6dB/octave roll-off in the stop-band. Such a filter can be electronically controlled over a wide range, as **Fig. 2** illustrates.

For operation as a low-pass filter the high-pass input should be grounded, and *vice versa*. Considering the low-pass case, at high frequencies where C is almost a short circuit, there is little output and what there is will be in quadrature. On the other hand, at low frequencies, where C is effectively open circuit, voltage gain of the OTA is indefinitely large. It is included along with the non-inverting gain of two of the CFA (the high-pass input is grounded) within an overall negative-feedback loop to the OTA's inverting input, pin 2.

As the two voltage dividers at the OTA inputs have the same ratio, there is unity non-inverting gain from the low-pass input to the output. The −3dB point where the phase shift through the circuit is −45° can be set by

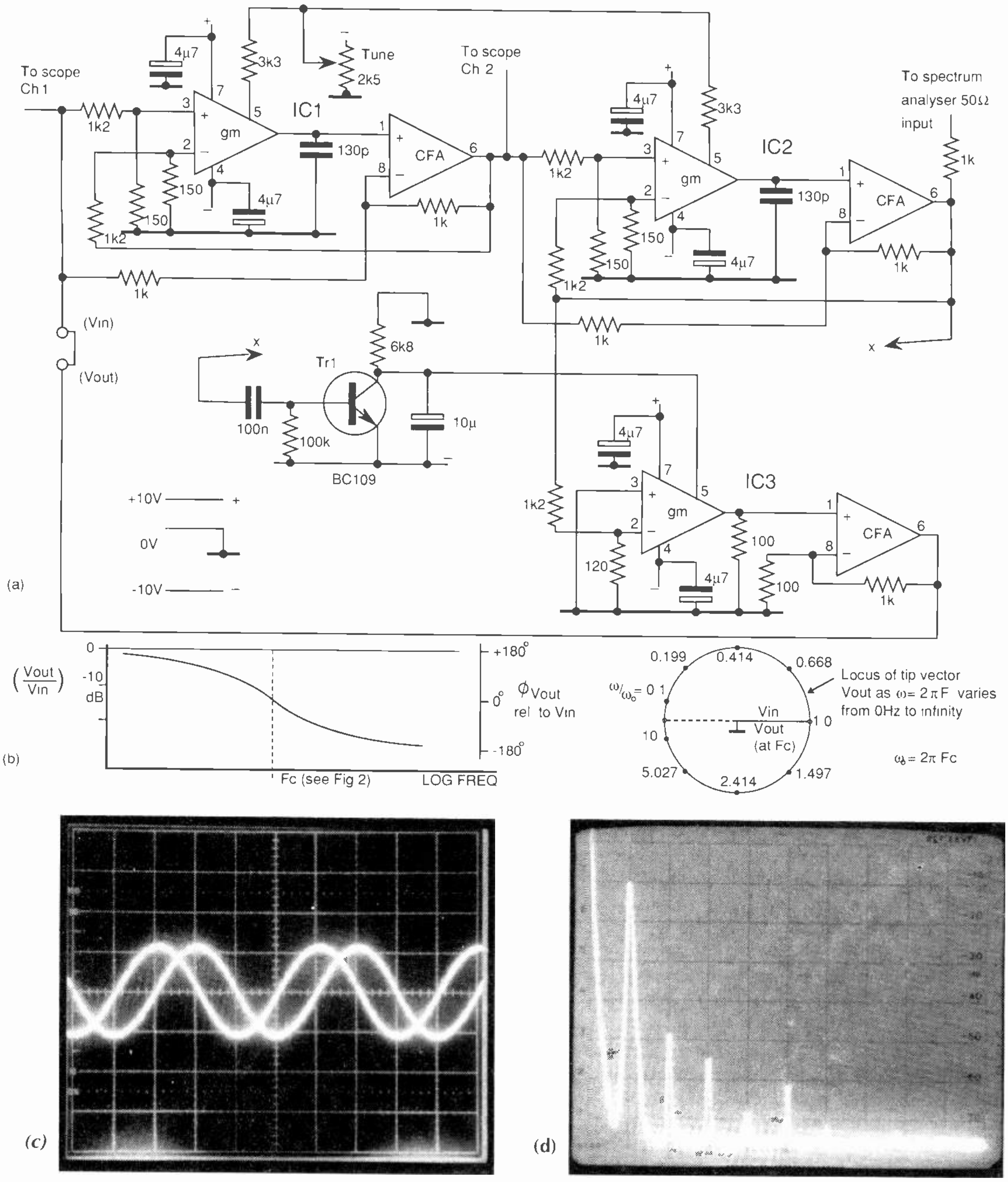


Fig. 4. In the all-pass filter based oscillator, (a), the 0.6V Vbe of Tr1 stabilises amplitude at 1.2V pk-pk. It does this by robbing Iset from IC3 until the loop gain just equals unity. Curve (b) shows open loop gain and phase as Bode and vector plots while (c) gives output waveforms of IC1 and IC3. Scales are horizontal 125ns/div vertical and 500mV/div. In (d), output spectrum from IC2 shows second harmonic content 38dB below the fundamental 2MHz output. All other harmonics are greater than 40dB down. Scales horizontal 2MHz/div; vertical 10dB/div.

adjusting the current I_{set} into pin 5.

If the low-pass input is grounded instead, a high-pass response is obtained, with the same –3dB corner frequency and unity *inverting* gain in the pass band. With the two inputs tied together, an all-pass response is obtained. This is as predicted by the Theorem of Superposition, passing from zero phase shift at 0Hz through 90° at the corner frequency to 180° at high frequencies.

Two *LT1228*s can be configured to give electronically tunable versions of any of the standard second order filter sections. Part of the data is the ingenious circuit shown in **Fig. 3**, which accepts inputs up to 3V peak to peak.

Unlike circuits designed with conventional integrators, this version of the state-variable filter does not need a third inverting op-amp. This is because the OTA integrators have both inverting and non-inverting inputs available. If one were used, then a high-pass output would also be available.The circuit provides the novel feature of logarithmic tuning sensitivity. As a result, it could be turned into a logarithmic sweep generator. To do this, the value of the damping resistor R_d would have to be raised and antiparallel diodes connected in series with it. Oscillation would also need to be ensured by including negative damping to the non-inverting input, pin 3, of the upper OTA.

Oscillators

All-pass circuits can also be configured as oscillators. The first such example probably predates WWII and several such designs having appeared in this journal. One of these[1] was a very low distortion audio oscillator covering 20Hz to 20kHz and using an ingenious distortion out- phasing scheme.

Figure 4a shows the circuit of an all-pass oscillator I have experimented with. Since both of the all-pass stages are non-inverting at dc, a third ***LT1228*** was added to give the necessary inversion. This addition permits overall negative feedback and hence stability at 0Hz. It also stabilises oscillation amplitude. Figure **4b** shows the gain and phase of the circuit with the loop broken,

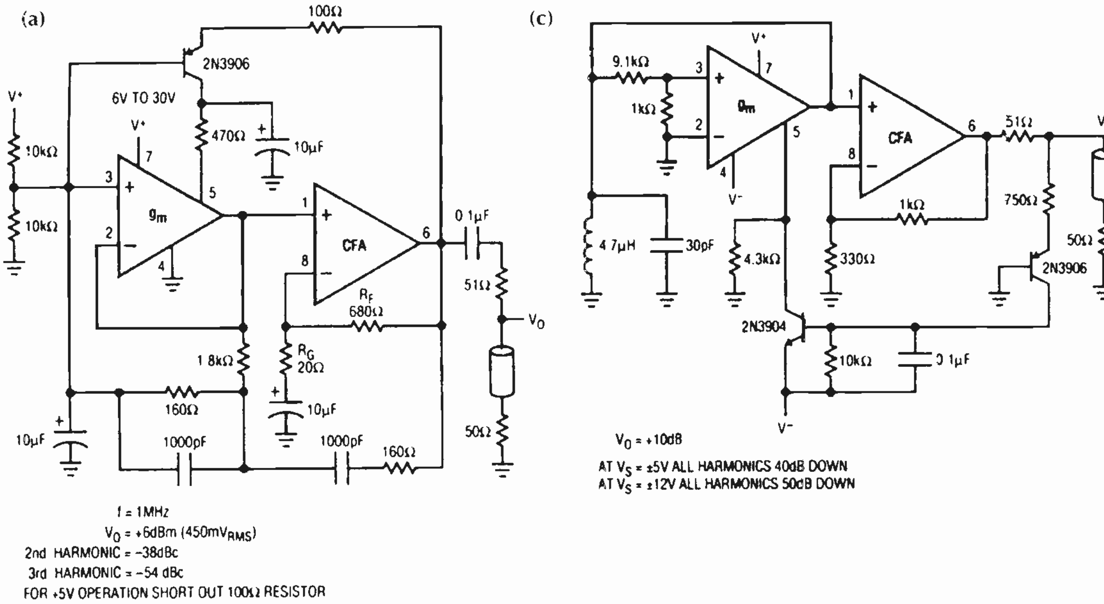
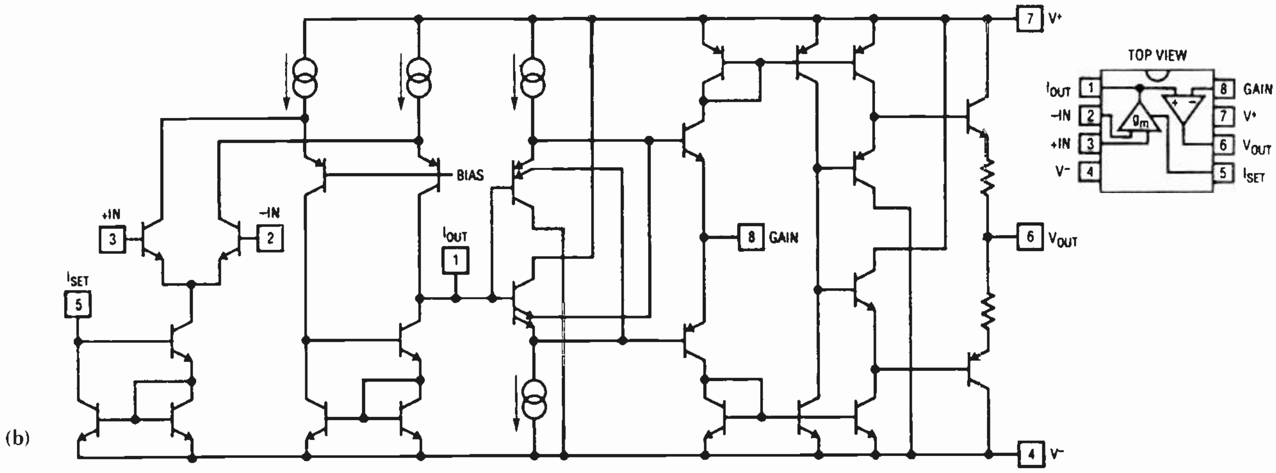


Fig. 5. Fixed frequency Wien Bridge oscillator (a) using LT1228. Oscillation is maintained by the current-feedback amplifier. Transconductance amplifier functions only as an electronically controlled attenuator to stabilise oscillation amplitude. Circuit (b) is a simplified diagram of the LT1228 operational transconductance amplifier with combined current feedback amplifier. In (c), the OTA forms an electronically controlled negative resistance connected across an rf tank circuit. This cancels losses and maintains a constant oscillation level.



but with I_{set} applied to pin 5 of IC_3 equal to what it is when the loop is closed.

At the corner frequency of the two all-pass stages, each contributes 90° phase shift, giving a total loop gain of exactly unity, non-inverting, and hence stable oscillation. This occurs at a level which just turns on Tr_1 on positive-going peaks, reducing the I_{set} available to IC_3 as necessary.

Figure **4c** shows output waveforms of IC_3 (leading trace) and IC_1 with tuning control RV_1 set for a 2MHz output. Low distortion and accurate quadrature are both evident. The circuit operates from well below 1MHz to beyond 5MHz. By 5MHz the quadrature phasing is less than 90°, due to the onset of additional loop phase shift in the inverting stage IC_3.

Beyond about 7MHz, the quadrature phasing becomes so marked that the circuit switches to a different mode of oscillation. There is around 60° of phase shift in each of the three stages and operation in this mode continues to 25MHz or more. Figure **4d** shows the output spectrum of IC_2 at 2MHz (horizontal division=2MHz, start = 0Hz). At 1MHz and below all harmonics are more than 40dB down.

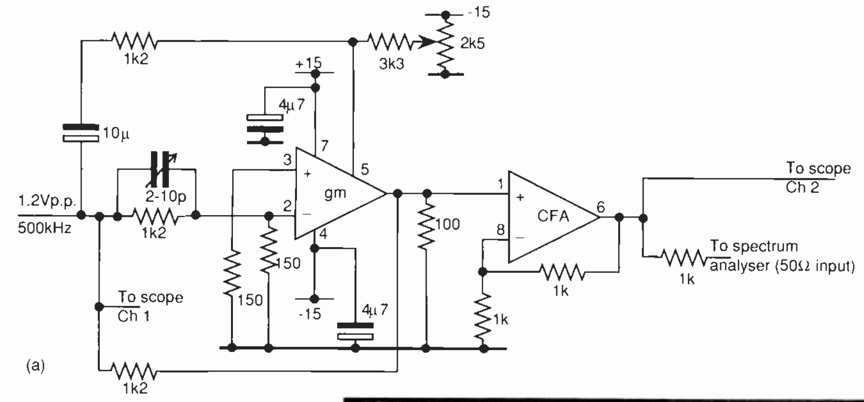
The OTA is versatile. Among other things, it allows an electronically-controlled resistor to be simulated by grounding its non-inverting input and connecting its inverting input to its output. If the output is taken positive relative to ground, the OTA will sink current, or source if taken negative, just as a resistor would.

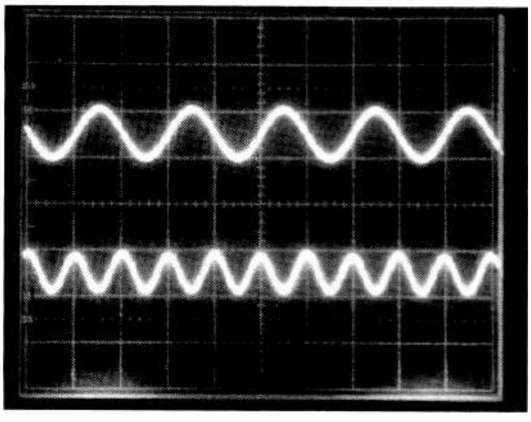
Figure 5a shows this arrangement used as part of a spot frequency Wien Bridge oscillator operating from a single supply. The OTA acts as an attenuator to stabilise the oscillator's output amplitude.

To avoid distortion due to overdrive, the gain of 34 supplied by the CFA keeps the swing at the input to the OTA down to 15mV. This precaution is necessary since for lowest distortion the *LT1228*, like all OTAs, can only accept a limited input swing.

Total harmonic distortion reaches 0.2% at 30mV rms input. An OTA's permissible input voltage swing is limited. This is because there is no emitter to emitter degeneration in the input stage, as is clear from Fig. **5b**. Operational transconductance amplifiers are frequently required to operate with no overall feedback to keep the inverting to non-inverting input voltage to a small value.

Grounding an OTA's inverting input and connecting its non-inverting input to its output also simulates a resistance, a negative one in this case. Figure **5c** shows such a negative resistor. It is connected across an rf tank circuit, so as to cancel the losses and raise the tuned circuit's dynamic resistance R_d to infinity. Here, the 9.1kΩ/1kΩ network at the OTA's input keeps the drive to a level that the device can handle linearly. Again, a transistor is used as a detector to sense output amplitude from the CFA buffer. It also adjusts the I_{set} of the OTA to stabilise oscillation amplitude.





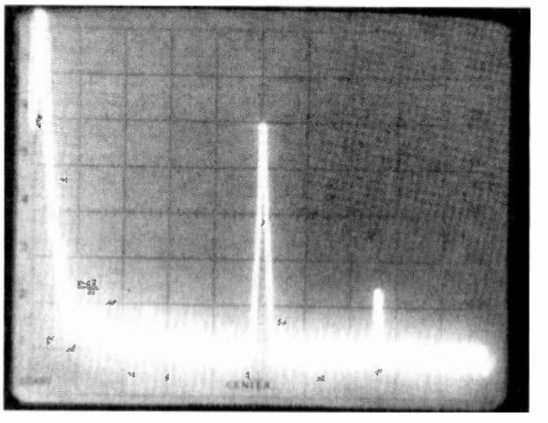


Fig. 6. Frequency doubler using an LT1228 for four quadrant multiplication (a). Circuit works by phasing out residual of the input waveform in the output. Oscillograph (b) shows 500kHz sinewave doubled to 1MHz. Upper trace input at 1V/div, lower trace output at 50mV/div. Horizontal scaling is 1μs/div. Trace (c) shows output spectrum. The 500kHz input is suppressed by 40dB. At 1MHz, input third harmonic at 1.5MHz is 35dB down relative to the wanted doubled output. All other outputs were at or below analyser noise level.

An intriguing possibility is the use of this circuit to maintain a constant very low level of oscillation in the tuned circuit of a simple radio receiver. Level would remain constant over the entire tuning range and the circuit would act both as an automated reaction control and as AGC. Such a receiver could handle both AM and SSB signals, offering very good selectivity due to the tuned circuit operating at a very high Q.

Sinewave frequency doubling

An OTA can also function as a squarer, and hence as a frequency doubler. Current swing at the output of an OTA is proportional to the amplitude of the signal applied to the inverting or non-inverting input. It is also proportional to the magnitude of I_{set}, and therefore to the product of the two quantities.

If a signal is applied simultaneously to both the inverting and I_{set} inputs, output current will contain a component representing the square of the input voltage. The resulting circuit is a two quadrant multiplier. Signal input can be bipolar but the I_{set} current must always be greater than zero, or the device simply cuts off. So the input merely modulates the magnitude of I_{set}, which is always positive. The dc component of I_{set} is responsible for a component in the output current corresponding to the original input.

To try the scheme out, I made up a doubler circuit using the *LT1228* on the lines described but with a crucial addition, **Fig. 6**. Since the signal is applied to the *inverting* input, pin 2, all components of the voltage developed across the 100Ω load resistor at the output are inverted in phase relative to the input. As a result, the component of the input voltage in the output can be phase cancelled by adding in a component from the input via the upper 1.2kΩ resistor, leaving just the squared component. Since the square of sin(wt) is (1–sin(2w*t*))/2, the circuit will thus double the frequency of an input sinewave to 2wt radians per second. Due to phasing, it will have no component at the original w*t*. The circuit is purely aperiodic. Apart from the trimmer at pin 2, no frequency sensitive components are involved.

Trimming extends the operating frequency range of the circuit by compensating for slight phase shift in the OTA at higher frequencies. Output will therefore be a pure sinewave at twice the frequency of the input, assumed to be a sinewave, over a wide range of frequencies. However, it would be wise not to rely on as much suppression of the fundamental input as illustrated in Fig. **6c**.

As a final example of the many applications for this versatile part, **Fig. 7** shows the circuit of a video cross fader. This uses two *LT1228*s in the feedback loop of an *LT1223* CFA. Each of the two video inputs is applied via a 1kΩ resistor to the OTA section of an *LT1228*, the CFA sections being unused.

Both OTA output currents are connected to the *inverting* input of a further CFA. This input is a low-impedance current-driven type. Negative feedback is applied from the output of the CFA to the non-inverting input of each OTA via a 1kΩ resistor. In this way, unity gain is given to each signal when the wiper of the 10kΩ potentiometer is at mid-travel.

The amount of signal from each input passing to the output is set by the ratio of the set currents of the two *LT1228*s – not by their absolute value. Both set currents remain high over most of the potentiometer's range. This keeps the bandwidth of each signal in excess of 15MHz, even when attenuated by 20dB. By this time, the other signal is dominant in the output video, and as the pot reaches the end of its travel, the attenuated signal is turned off completely. ■

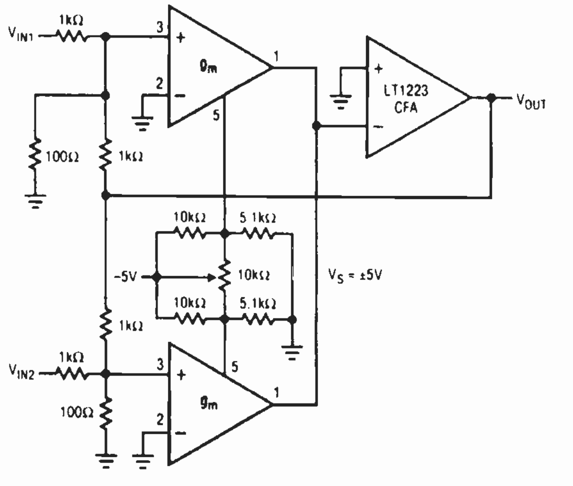


Fig. 7. Video cross fader. Relative to unity gain (potentiometer at mid travel) a 15MHz bandwidth to each signal is maintained down to an attenuation of 20dB. Suppression of one or other signal at each end of the potentiometer travel is complete.

Reference

1. Phase-shifting oscillator, R Rosens, *Wireless World* Feb. 1982 pp 38-41.

USING RF TRANSISTORS

Choosing the right device

How does the intended application affect transistor choice? And what type of device would give the best performance? In this extract from their book* RF Transistors: Principles and practical applications, *Norm Dye and Helge Granberg answer both questions.

Looking first at low power, and the needs of a low noise amplifier, the main transistor selection criteria are operating frequency and noise figure. The most practical consideration is probably to choose a transistor characterised by the manufacturer with the necessary noise parameters. These are minimum noise figure at a given frequency, noise resistance, and source resistance for minimum noise.

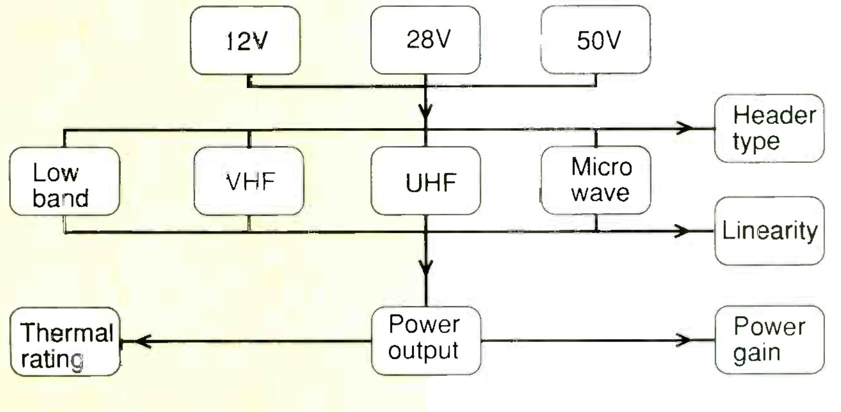
Manufacturers frequently plot gain and noise figure contours for a specified bias condition and frequency of operation. These are extremely helpful in making the necessary trade off between optimum gain and optimum noise when designing the low noise stage.

Choosing a transistor for other low power applications is generally simpler than for either low noise or high power because the choices are fewer. Most low power transistors have similar breakdown voltages although a few are designed for higher voltage use.

Occasionally, a special low power transistor designed to operate at very low voltages and low current will crop up. But generally all that need be done is to select a low power transistor with sufficient current rating for an intended application and with a high enough cut-off frequency to provide the desired gain at the operating frequency. Where switching is involved, the higher the cut-off frequency, the faster the switching capability of the device.

Package type can be an important consideration when choosing a low power transistor. The same die is frequently offered in metal can, plastic stripline opposed emitter (SOE), surface mount, and hermetically sealed metal-ceramic packages. Usually, the smaller the package, the lower the package parasitics and the better the RF performance of the die – especially at higher frequencies.

Fig. 1. One way to select an rf transistor for a specific application. Usually, voltage is predetermined. When considering frequency, you also need to consider gain. Power selection is the most straightforward.



High power applications

A wide choice of high power rf transistors, i.e. devices greater than 1W, presents additional problems in selection. The major distinctions are in voltage of operation, operating frequency and output power, **Fig. 1**.

Assuming the application is an amplifier, other factors include linearity and bandwidth required, efficiency, thermal requirements for reliability and, of course, the type of package. Ruggedness, defined as the ability to withstand unfavourable load environments, is also a factor.

Voltage. Operating voltage is usually a predetermined specification, but in some applications – such as fixed location transmitters – there may be a choice. In these cases, designers must determine the advantages and disadvantages of low and high voltage designs. There is no significant difference in input impedance and matching. But output impedance is highly dependent on operating voltage and power output level.

Depending on power level, the operating voltage that gives the lowest impedance transformation required of the load impedance, usually 50Ω, should be selected. In multistage designs, the drivers and predrivers are often operated at a lower supply voltage than the power amplifier stage – partly due to their naturally higher output impedances. The result is a closer match to the input of the following stage.

Frequency. Choice of operating frequency is more straight-forward. Manufacturers generally grade high-power rf transistors by frequency as well as voltage. Also, a transistor with adequate gain at the desired operating frequency should be selected.

High-frequency transistors can always be used at lower frequencies, although special attention needs to be paid to stability, ruggedness, and cost. Normally, gain in rf transistors decreases with increasing frequency. When used at frequencies below their normal operating range, the gain will be higher and may create instabilities.

High frequency transistors are built using shallower diffusions, lower collector resistivity, and less emitter ballasting – all necessary to achieve greater amplification at higher frequencies. Unfortunately, these are also the opposite of what is needed to improve ruggedness of a transistor. Gain and ruggedness at a given frequency are a trade off in device design.

Finally, high frequency transistors cost more than lower frequency transistors, all other factors being equal. So, choose a transistor that will give the desired gain, but no more, at a given frequency.

Power. The third major factor, output power, is an easier choice – simply select one that will give a sufficient level. Design of an amplifier line-up should always start at the output stage, working back from that point to select transistors. Gain available from the output transistor then sets the requirements for the driver stage.

Bandwidth considerations

Circuit design usually determines bandwidth. But at higher frequencies, the Q of the input impedance of a power transistor increases. This makes it more difficult to achieve broad band circuit designs. As the transistor's power rating and operating frequency increase, input and output impedances of the device decrease.

Think of it this way. Higher power transistors are simply low power transistors connected in parallel. Resistors in parallel result in a lower overall resistance; capacitors in parallel result in a higher overall capacitance. The net result is an input impedance for high-power, high-frequency transistors that is too low to be practical for circuit designers having access only to the terminals of the transistor.

Manufacturers have alleviated the problem of low input impedance and high Q of high-power, high-frequency transistors by placing impedance matching networks inside the device package, near to the die. These not only raise the impedance of the transistor as seen at the edge of the package but also transform impedance values to reduce the reactive components, and hence Q.

Impedance matching

An internally-matched transistor causes less difficulty in broad band circuits over its specified frequency range. In general, bipolar transistors designed for VHF and rated for 40-50W or higher use internal matching techniques. At UHF the corresponding numbers are 10-20W and at 800MHz about 5W.

Internal matching networks are low-pass filters usually optimised for the high end of the specified spectrum range, where power gain and impedance levels are lowest. Most rf power devices for operating below 1GHz have only internal input matching. But internal output matching is also applied to higher power UHF transistors and most microwave devices.

Normally, the input matching network consists of an *LCL* combination, where *L* is the distributed inductance of the die bonding wires and *C* is a mos capacitor, **Fig. 2**. The same guidelines are used for output matching network designs.

Obviously, these internal matching networks place some bandwidth limitations on device operation, particularly at frequencies above the rated limits of operation. For example, a matched transistor designed for operation in the 225-400MHz range should perform well within this band.

Above 400MHz, power gain will drop sharply and the base-to-emitter impedance will increase in its reactive component. There comes a point where the given drive power cannot be transferred to the die itself. At an even higher frequency, the internal matching network will have a point of resonance where the input impedance becomes extremely high and the device's power gain is minimal.

Below the low end of the specified operating range, the internal matching network has a diminishing effect. However, at some intermediate frequency, 100-200MHz in this case, the matching network may produce an even lower input impedance than without internal

Table 1. Summary of specific characteristics of each device type. Note that the table focuses only on silicon mosfets in the fet category and some of the characteristics may not apply to jfets and other depletion mode fets. Similar electrical sizes for each are assumed for the impedance comparison.

Characteristic	Bipolar	Mosfet
$Z_{in}R_s/X_s$ (2.0MHz)	3.80 — j2.0Ω	19.0 — j3.0Ω
$Z_{in}R_s/X_s$ (150MHz)	0.40 + j1.50Ω	0.40 + j1.50Ω
Z_{Ol} (load impedance)	Nearly equal for each transistor, depending on supply voltage and power output.	
Biasing	Not required, except for linear operation. High current (I_C/h_{FE}) constant voltage source necessary.	Required for linear operation. Low current source, such as resistor divider is sufficient. Gate voltage can be varied to provide an AGC function.
Linearity	Low order distortion depends on electrical size of die, geometry and h_{FE}. High order intermodulation is a function of type and value of emitter ballast resistors.	Low order distortion worse than with bipolars for a given die size and geometry. High order intermodulation better due to lack of ballast resistors and associated non-linear feedback.
Stability	Instability mode known as half f_0 troublesome because of varactor effect in base-emitter junction. Lower ratio of feedback capacitance versus input impedance.	Superior stability because of lack of diode junctions and higher ratio of feedback capacitance versus input impedance.
Ruggedness	Usually fails under high current conditions (over-dissipation). Thermal runaway and secondary breakdown possible. h_{FE} increases with temperature.	Over-dissipation failure less likely, except under high voltage conditions. g_{FS} decreases with temperature. Other failure modes: gate punch through
Advantages	Wafer processing simpler, making devices less expensive. Low collector-emitter saturation voltage makes low voltage operation feasible.	Input impedance more constant under varying drive levels. Better stability, better high order intermodulation, easier to broadband. Devices and die can be paralleled with certain precautions. High voltage devices easy to implement.
Disadvantages	Low input impedance with high reactive component. Internal matching required to increase input impedance. Input impedance varies with drive level. Devices or die can not easily be paralleled.	Larger die required for comparable power level. Non-recoverable gate puncture. High drain-source saturation, which makes low voltage, high power devices less practical.

matching. This is due to the lesser effect of the series Ls and the remaining shunt C.

Dropping further in frequency, the effect of the internal Ls and Cs will reach a point where a normal input impedance is approached. As a result, the internally matched transistors may not be suitable for bandwidths wider than those that the transistor was originally designed for.

There are certain design techniques for external circuitry that allow matched transistors to be used at lower frequencies and for extended bandwidths, with somewhat compromised performance. But such matching circuitry is usually complex. Furthermore, the device impedance profile at these frequencies – not given in most data sheets – must be known.

Mosfets versus bipolars

It appears that extremely wideband amplifier designs are only possible with mosfets. For rf power purposes, the technology has been available for approximately fifteen years, although most of the breakthrough has occurred within the past five.

No internal impedance matching is used with mosfets, except in rare cases at 800-900MHz and higher frequencies. Such data sheet bandwidth specifications as 2-175MHz, 100-500MHz, and 390MHz are misleading since all unmatched mosfets, as well as bipolar transistors, are operable down to DC if stability can be maintained. They can also be used at higher than the specified frequency limit, keeping in mind the normal 5dB per octave power gain roll off.

Since the input impedance of a mosfet is several times higher than that of a comparable bipolar transistor without internal input matching, multi–octave bandwidths can easily be realised with proper circuit design. But because a mosfet is a high voltage device by its nature (high $R_{DS(on)}$ compared to bipolar $V_{CE(sat)}$) its performance in low voltage applications may be challenged by its bipolar counterpart.

Fet or BJT?

There are now two basic types of rf power transistor – bipolar junction and field effect. Bipolar junction transistors, or BJTs, yield superior performance in some applications. In others, field effect transistors do a better job. Only two types of bipolar junction transistor are commercially available today, NPN and PNP.

Despite their inferior performance over NPN types, PNP transistors are primarily used in land mobile communications equipment requiring a positive ground system. All UHF and higher frequency devices are NPN due to their higher mobility of electrons as majority carriers, translating into higher cut-off frequency and improved high-frequency power gain.

Far more types of fet are commercially available for RF power use. The static induction transistor, or sit, is a version of a depletion–mode junction fet and metal gate Schottky fet, or mesfet. Usually, the mesfet is made of gallium arsenide and is also a depletion-mode type.

Another depletion-mode device is the standard junction fet. But this is only practical in low power pre-drivers and mixers, etc. The most common RF power fet is the vertical channel silicon mosfet. This device comes in a number of varieties of die structures, each having slightly different characteristics of $R_{DS(on)}$ and the various capacitances. It has been available since around 1975, and numerous improvements have been made in its performance and manufacturability.

There is also a lateral channel power mosfet in existence, consisting of a series of small signal fets connected in parallel on a single chip. Due to its lateral channel structure, it consumes more die area for a given power rating than the vertical channel device. As a result it is cost effective. However it has extremely low feedback capacitance, C_{RSS}, resulting in increased stability and higher gain at high frequencies.

Both these silicon mosfets are enhancement-mode devices. For the drain-source channel to conduct, their gates require positive voltages with respect to the sources. Conversely, a depletion mode fet conducts when the gate and source are at an equal potential, and requires a negative gate voltage for turn off (depletion).

Comparing parameters

With rf amplifiers, a major difference between a BJT and a mosfet is the need for base/gate bias voltage. A BJT only needs base bias for linear operation. There is very little difference in its power gain between a biased (class A, AB, or B) and an unbiased condition (class C).

In an unbiased enhancement-mode fet, gate input voltage swing must overcome the gate threshold voltage to turn the fet "on" with its positive peaks. Some fets have their gate threshold voltages specified as high as 6V. If the dc gate voltage is brought closer to its threshold level, a smaller voltage swing is needed to overcome it. Since in each case the gate-source rf impedance is about the same, the actual power gain can vary as much as 5-6dB depending on the initial threshold voltage and frequency of operation.

For linearity, a fet also needs to be biased in class A or AB operation. Since no dc current is drawn, the bias source may be a simple resistor divider, whereas a BJT requires a constant voltage source of 0.65-0.70V with a current capability of $IC_{(peak)}/h_{FE}$.

Most RF power design engineers accustomed to circuit design with BJTs are beginning to look at fet designs and learn about the differences in parameters and behaviour between the two types of semiconductors, **Table 1**. Circuit design with each is very similar. The same rf design practices – grounding, filtering, bypassing, and creating a good circuit board layout – all apply.

For each type of device, some precautions must be taken. Fets are sensitive to gate rupture. This is caused by excessive dc potential or an instantaneous transient between the gate and the source. The effect can be compared to exceeding the voltage rating of a capacitor, usually resulting in a short or leakage.

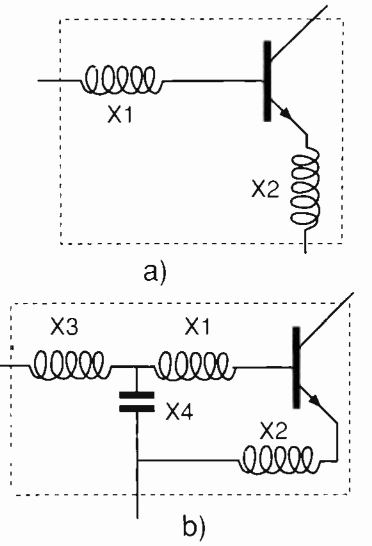


Fig. 2. Electrical models of an unmatched transistor (a) and one with internal input matching (b). Components X1 and X2 represent the standard base and emitter wire bonds. In (b), X1 and X3 represent wire bond loops whose height must be closely controlled. Component X4 is a mos capacitor with typical values of 150–500pF for UHF and up to 2000pF for VHF.

A power fet can be "restored" in some instances by applying a voltage lower than the rupture level between the gate and the source. The current must be sufficient, but not higher than 1-1.5A, to clear the gate short. A higher current would fuse one of the bonding wires to the area of the short on the die.

Some cells will always be destroyed, but with larger devices – 30W and higher – no difference in performance may be noticed. However, long term reliability can be jeopardised, and the practice is not recommended where high reliability is required.

A weak spot with the BJT is the possibility of thermal runaway. Devices with diffused silicon emitter ballast resistors are less susceptible than those having nichrome resistors. The diffused silicon resistors have a slight positive temperature coefficient; the nichrome ones have near zero coefficient. However, the diffused resistors are non-linear with current. Devices using them are less suitable for applications requiring good linearity.

The main reason for thermal runaway of a BJT is that h_{FE} increases with temperature. In a mosfet, g_{FS} goes down, trying to turn the device off. In contrast, the gate threshold voltage decreases by about 1mV/°C, making the temperature profile of a gate-biased device dependent on the initial value of g_{FS} and the voltage of operation.

Figures of merit for a BJT and fet are defined as the emitter periphery/base area and gate periphery/channel length respectively. In practical terms these relate to the ratio of feedback capacitance to input impedance. This is because finer geometries produce lower feedback capacitance for common emitter and common source configurations.

It appears that devices with higher figures of merit are more stable. This would be true, except that power gain is also higher, leading to instabilities through stray feedback. At a high frequency, feedback capacitance produces positive feedback due to phase delays.

One more BJT instability mechanism is a result of a varactor effect in its diode junctions, mainly the collector-base. This "half f_0" is usually a steady spurious signal at half the frequency of the excitation. Lack of junctions in a fet mean this phenomenon is unknown in mosfet power circuits.

Matching impedance

The largest difference in impedance matching can be seen in the base-emitter and gate-source impedances. At dc the mosfet has an infinite gate-source impedance, whereas the BJT exhibits the impedance of a forward-biased diode.

At higher frequencies, depending on the device's electrical size, the gate-source capacitance, C_{ISS}, is enhanced by the Miller effect. This, together with the wire bond inductances, forms a complex impedance which may be lower than that of the BJT. Output capacitance C_{OB}/C_{OSS} is almost equal for both types, of equivalent electrical size. Output capacitance has a large effect on the efficiency of an amplifier. This is because it must be charged, to around twice the supply voltage, and discharged again during each cycle of the operating frequency. Power used in charging is dissipated in the amplifying device. At a single frequency, a part — but not all — of the capacitance can be tuned out since its value varies with the output voltage swing.

Power loss due to output capacitance for a single ended BJT amplifier, for example, can be defined as,

$$P_s=(2C_{ob})(V_{CC})^2(f)$$

where P_s is power loss, f is frequency and efficiency is $P_{out}/(P_{out}+P_s)$.

Power loss is directly related to capacitance and to the square of the supply voltage. So a higher operating voltage does not always result in higher efficiency, as commonly thought.

Equivalent parameters and their designations for bipolar transistors and mosfets are compared in **Table 2**. Note that all parameters are not applicable to both types of devices. ■

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Table 2. "Equivalent" parameters of bipolar and mosfet transistors.

Bipolar	mosfet	
BV_{CEO}	BV_{DSO}	Breakdown avalanche voltage, measured with the base open. Not specified or measurable with mosfets. In case of any drain-gate leakage, the gate can charge to voltages exceeding the V_{GS} rating.
BV_{CES}	BV_{DSS}	Breakdown avalanche voltage, measured with the base and emitter or gate and source shorted. Normal method of measuring mosfet breakdown voltage.
BV_{CBO}	BV_{DGO}	Breakdown avalanche voltage, measured with the emitter open. Not specified or measurable with mosfets. Gate-source rupture voltage could be exceeded.
BV_{EBO}	V_{GS}	Reverse breakdown voltage of the base-emitter junction. Not specified or measurable with mosfets unless dene carefully at low current levels. Gate rupture can be compared to exceeding a capacitor's maximum voltage rating.
V_B(forward)	V_{GS}	Not specified or necessary in most cases for a BJT. For a mosfet this parameter determines the turn-on gate voltage, and must be known for biasing the device.
I_{CES}	I_{DSS}	Collector-emitter or drain source leakage current with base and emitter or gate and source shorted. BJT and fet parameters are equivalent and normally the only effects of leakage are wasted dc power, increased dissipation and long term reliability.
I_{EBO}	I_{GS}	Base-emitter reverse leakage current and gate-source leakage current. Not normally given in BJT data sheets, but important for mosfet biasing. Both affect their associated devices's long-term reliability.
V_{CE}(SAT)	V_{DS}(SAT)	Device saturation at dc. Not usually given in BJT data sheets but important in certain applications. With power mosfets this parameter is of great importance. The mosfet numbers are higher than those for a BJT and are dependent on several factors in processing the die.
h_{FE}	g_{FS}	These are parameters for low frequency current and voltage gain, respectively. In a mosfet the g_{FS} is an indication of the device's electrical size. To a certain extent, it depends on device type and die geometry.
f_T	(f_T)	Unity current or voltage gain frequency. Not given in many BJT or mosfet data sheets. The value can be two to five times greater for the mosfet for equivalent geometry and electrical size.
G_{PE}	G_{PS}	Power gain in common-emitter or common-source configurations. This figure is roughly the same for both types of devices. It is normally regarded as current gain for the BJT and voltage gain for the mosfet.
C_{ib}	C_{iss}	Base-emitter or gate-source capacitance. Rarely given for a BJT. In rf power fets the C_{iss} has a greater effect on the gate-source impedance.
C_{ob}	C_{oss}	Collector-emitter or drain-source capacitance. Both are usually specified, and are approximately equal in value for a given device rating and voltage. Both tare combinations of mos and diode capacitance.
C_{rb}	C_{rss}	Collector-base or drain-gate capacitance. Rarely specified for BJTs. Normally referred to as the feedback capacitance for mosfets.

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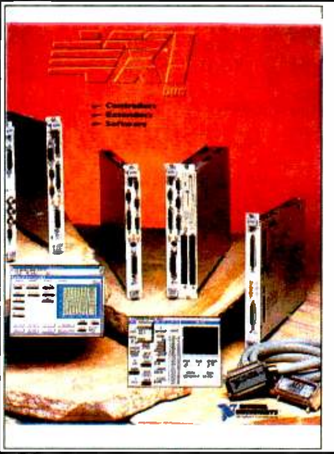

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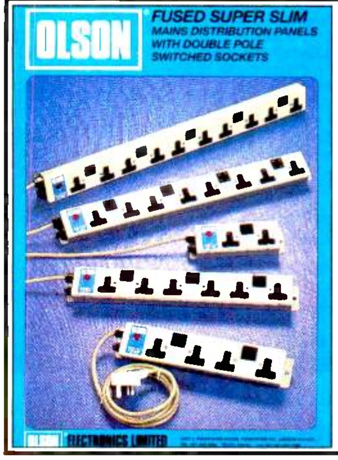

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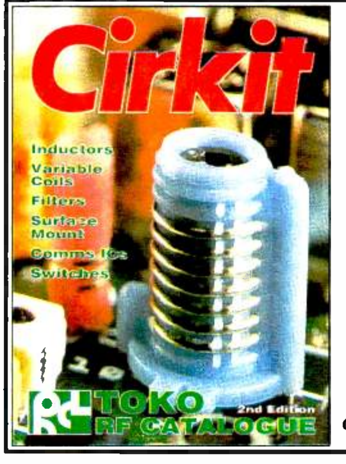

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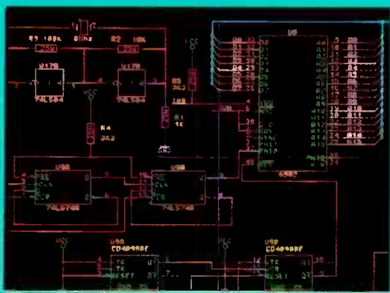

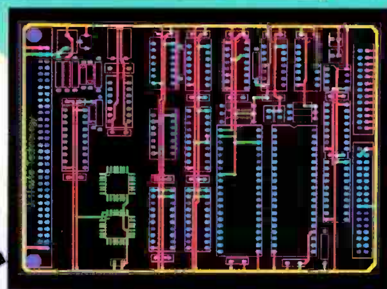

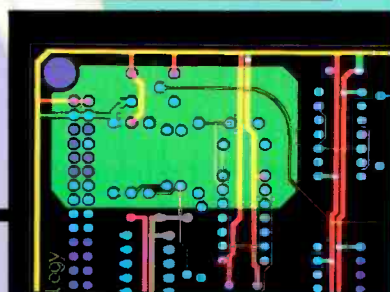

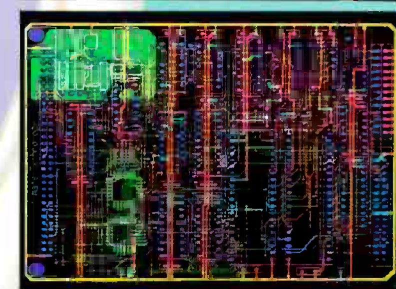

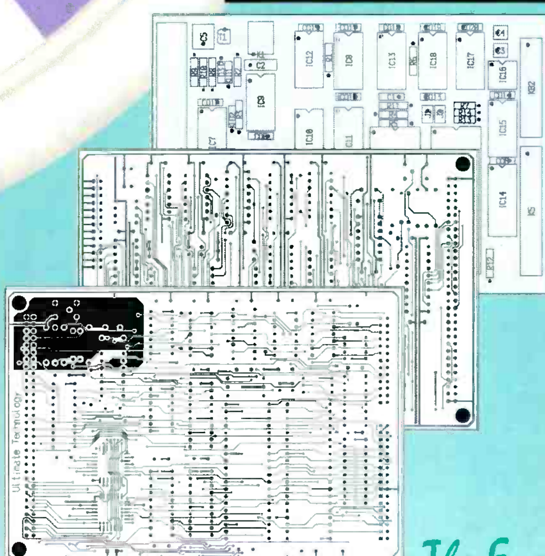

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