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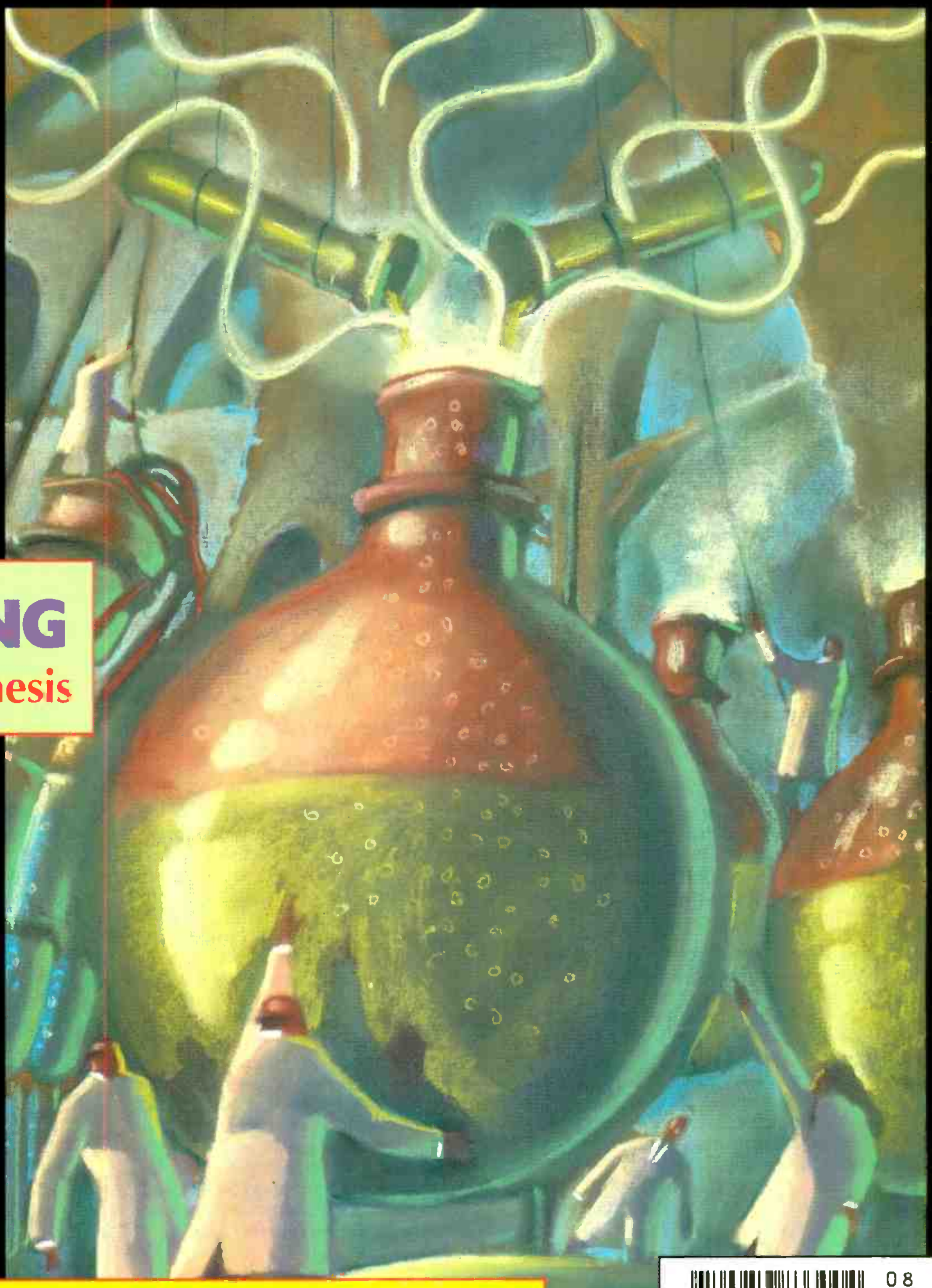

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SEPTEMBER ISSUE ON SALE FROM AUG 27

Flights of fantasy

How on earth could the British, Italian and Spanish governments consider continuing with the European Fighter Aircraft project? This particular piece of euro-madness looked more like a turkey than an aeroplane even before the Germans decided to press the ejector button. After all, it was conceived five years before the Berlin wall came down as a singular response to a specific military threat from the old Warsaw Pact.

Examining UK domestic politics for a moment, EFA has welded together some extraordinary domestic alliances: the Foreign Office says it remains a good idea because it proves that we in the UK are good Europeans; the Department of Trade and Industry says that it is a good idea because it believes what British Aerospace told it about 40,000 job losses; the Ministry of Defence says that EFA is a good idea because the old soviet defence industry is still selling some pretty mean warplanes to the rest of the world. But most surprising of all, the Labour opposition supports the government in this £20 billion job creation scheme, presumably because it thinks that is what it is.

Few people would suggest that a government has no responsibility to promote high technology, even for defence purposes, but the sort of money which EFA will gobble up is almost unimaginable; it could pay for the equally anachronistic Trident submarine defence system in its entirety.

Just a fraction of the £20 billion spend could launch a global class electronics initiative to research, design and produce the sort of products which the rest of the world wants to buy: a fully digital broadcast television system is such an example. Associated programmes for chip research and display technology would spin off far more widely than overpriced, esoteric airframes and weapons systems.

UK electronics desperately needs inducement on a scale that only a massive government programme can provide but EFA is definitely the wrong programme. So how can our politicians be so stupid or corrupt in failing to recognise this? It is simply that the aerospace/defence industry led by British Aerospace and GEC enjoys an incredibly effective lobbying system in which retiring Forces personnel are engaged by these companies to promote corporate interests in their old Ministry departments. The result has been a run of spectacularly expensive defence contracts followed by equally spectacular failures. For example, GEC's Nimrod programme wasted £800 million EFA will make this look like petty cash. The economist John Maynard Keynes was only half joking when he suggested that the easiest way of involving industry in public spending programmes was to dig a large hole, fill it with old banknotes, cover them with earth, and then issue companies with licences to dig them out again.

But it isn't just the money which lunatic programmes consume. They distort the entire industry infrastructure – or that which remains – because defence contracts do not encourage the commercial discipline which participating electronics companies need in servicing wider markets.

If there is a real defence requirement for a new fighter aircraft, this should be put out to tender in a free competition which includes Mikoyan and Sukoi. Who knows, the result could be a MiG-29 airframe stuffed with British electronics. This would put the wind up the boardroom gangsters who currently control the UK defence industry, give concrete help to the struggling CIS, provide defence of the realm and save the taxpayer vast sums of money.

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REGULARS

UPDATE

Big names design single chip PC

US semiconductor makers are racing to produce a single chip processor combining all the logic and processing required for a 32-bit PC.

Recent talks between Intel and VLSI Technology Incorporated (VTI) may be aimed at developing just such products, according to insiders. Intel executives have already said that the company plans to compress all the logic needed for a 32-bit PC onto a single chip by 1993. Intel recently announced it was working with IBM in this area.

Texas Instruments and chipset vendor Chips & Technologies are also working on single chip PCs which should appear next year.

Such devices will produce powerful new laptop and palm top computers and cut the cost of desktop machines, as well as fusing microprocessor and chipset sales into a single $1.5bn-plus annual market.

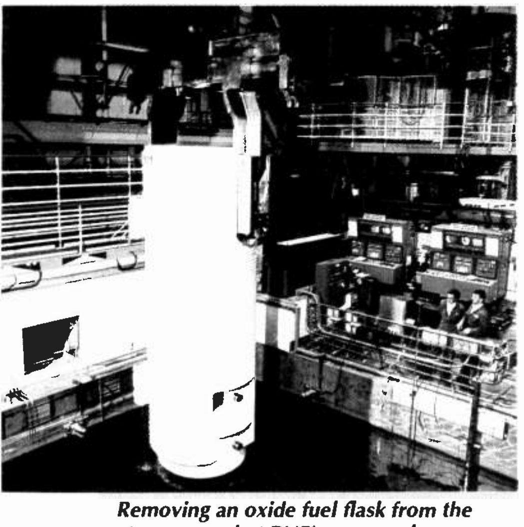
VTI already makes house-keeping chipsets for *386* and *486* microprocessors which are being redesigned to operate on 3.3V power supplies. Low power single chip devices combining Intel *386* and *486* microprocessor cores with VTI chipset circuitry could result from an agreement.

Meanwhile TI plans to integrate the *486* clone microprocessor licensed from Cyrix with its own 32-bit PC chipsets using a 0.5μm cmos semiconductor process.

Single chip PCs will increase competition for stand-alone *386* and *486* microprocessors and clones. But Intel rival AMD will not undermine sales of *386* clone products with integrated chipsets unless it can add value, according to UK chief Dave Brand.

However, Intel will be able to protect profits from stand-alone processors by ramping up production of a new device, code-named *P5*.

Leon Clifford, *Electronics Weekly.*



Removing an oxide fuel flask from the storage pond at BNF's new nuclear reprocessing plant. Safety at the 750 acre site relies on integrity of information, from field transmitters, ensured by signal conditioning equipment from Rochester Instrument Systems.

Racing performance from battery micro

A microprocessor claiming the highest available ratio of computing performance to power consumption has been launched by US chip maker VLSI Technology Incorporated (VTI).

VTI's implementation of the *Arm610* 32-bit risc micro delivers around 18Mips or 29kDhrystones at 25MHz with a power dissipation of less than 600mW.

It is aimed squarely at portable and hand-held applications, according to VTI's new product director Jeff Hendy. The chip is fully compatible with Sun, Dos and Macintosh operating systems.

Based on advanced samples, US computer maker Apple designed the chip into its *Newton* hand-held battery powered computer, launched recently, because of its combination of performance and low power – according to Apple *Newton* chief Larry Tesler. Apple reportedly clocks the chip at 20MHz so that it can run at 3.3V on 90mA of current supplied by batteries.

Based on the architecture developed by VTI-backed Cambridge-based Advanced Risc Machines, the *Arm610* includes a 32-bit processor core, on-board memory management, 4kbytes of cache and a write buffer. It is functionally identical to the recently announced *Arm600* but comes without support for a coprocessor.

Made on VTI's 1μm cmos process samples are available now. A 0.8μm implementation will be sampled in September delivering 25Mips at 35MHz running on a 5V supply.

●Cambridge-based Acorn Computers is planning to launch a new generation of Archimedes PCs based around the *Arm600* risc microprocessor. The machines will deliver between 20 and 25Mips.

By integrating key logic circuitry, Acorn plans to cut the chip count and keep prices down. Plans involve eventually integrating memory control, video and i/o together with the processor core on a single chip.

LC

Electronic holograms colour our world

A combination of computers and holograms may provide colour images in three dimensions suitable for designing cars and viewing holographic TV as a result of work carried out at Massachusetts Institute of Technology.

The MIT method relies on eliminating image details not essential in creating the image. To achieve this, a description of the information contained in a holographic image is transmitted from a supercomputer database in a type of semantic image encoding.

The computer takes these simplified image codes and converts them into signals representing the optical fringe patterns which will display a hologram made up of 192 horizontal lines. Each of the lines

GeorgiaTech: looking for a third dimension.

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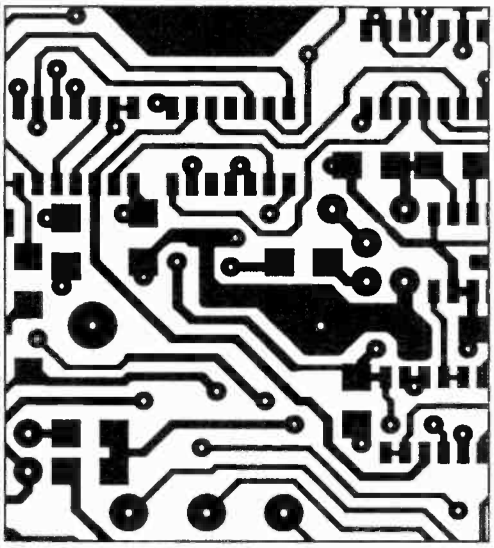

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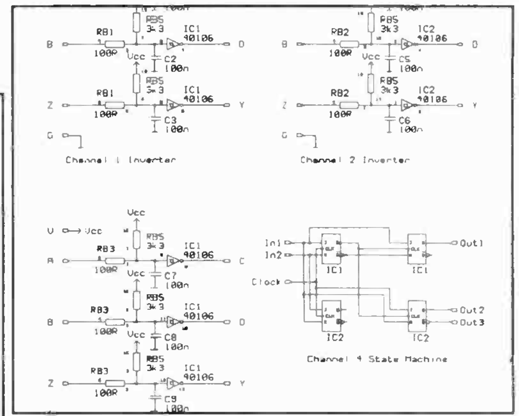

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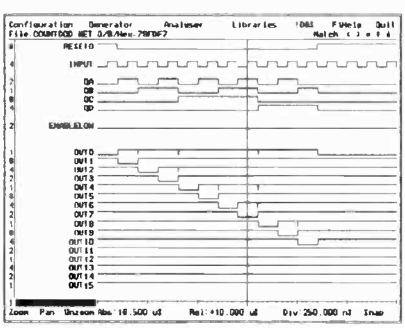

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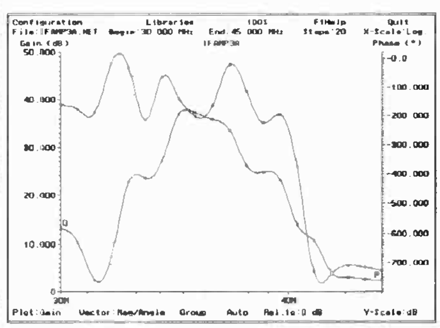

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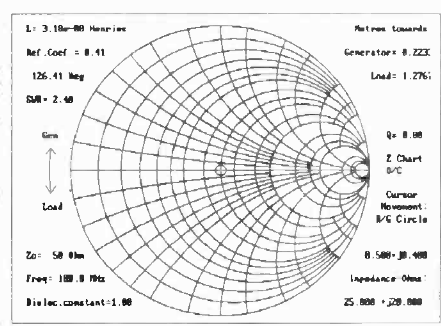

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contains 16 other lines to create 32,000 picture elements.

After removal of unnecessary holographic data, the light signals modulate radio frequency signals. These are then amplified and applied to three transducers connected to a tellurium dioxide, acousto-optical crystal. The resulting ultrasonic waves travel through the crystal, thus changing the refractive index as the pitch changes and the wavefront moves forward.

A laser sends light through the crystal which is diffracted. The laser beam hits a polygon mirror which freezes the information by spinning in the opposite direction and at the same speed as the sound waves. At every 16 lines, a vertical scanner moves down a step for the scan line that follows. Finally, a lens focused on the spinning mirror magnifies the scan lines into a holographic image that appears to "float" in a background of black.

To date, the images have been simple ones such as three-dimensional cubes. More complex detail in a scene will require more complex code to achieve a holographic effect using the computer.

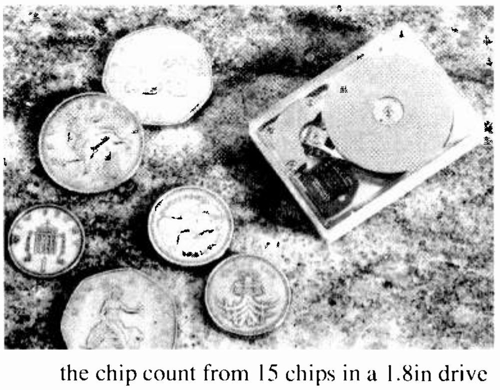
The Multimedia Laboratory at the Georgia Tech is also developing 3-D with an optical digitiser which automatically provides detailed computer descriptions of three-dimensional objects. The device is intended to replace the tiring work currently done in manually digitising objects using a pen and other basic tools.

GeorgiaTech's scanner uses three video cameras to obtain data about an object's contours as it slowly rotates on a turntable. Proprietary electronic equipment converts the video input to the basic mathematical description that models complex objects. This information is stored in a standard .DXF format file which can then be manipulated in colour, form and texture. **Martin Cheek**.

Wristwatch technology opens up mini hard disc market

Hewlett-Packard has launched a 1.3in 21Mbyte drive measuring 10.5mm by 36.5mm by 50.8mm. For the first time mini hard drives are appearing that rival the space and power advantages boasted by more costly memory chips – vital to the emerging generation of handheld electronic gadgets. Other drive makers led by US-firms Seagate and Conner are set to follow. Indeed, two weeks ago Seagate unveiled a 65Mbyte 1.8in drive.

Mini drive makers will be helped by the appearance of highly integrated disk drive control chipsets. Chip maker AT&T Microelectronics collaborated in developing the control chips for the HP drive – slashing



the chip count from 15 chips in a 1.8in drive down to eight – and has now launched its contribution as a stand-alone product called Reach 2.

With the annual worldwide market for mobile computer memories expected to reach $20bn a year by the end of the decade, the race is on to develop cheap and small non-volatile mass storage.

Solid state memory gained an edge back in the early 1980s when the semiconductor arm of Japanese giant Toshiba developed flash memory chips which retain data when the power goes off. However, flash is still expensive. A 20Mbyte flash-based plug-in computer memory card costs around $600. Compare that with the $250 apiece volume price offered by HP for its 21Mbyte Kittyhawk 1.3in drive. That works out $30 per Mbyte for flash as against $12 per Mbyte for Kittyhawk. US chip maker Intel is predicting that flash will reach $10 per Mbyte sometime in 1995.

HP is confident mini drive costs will fall even further as production volumes increase.

HP is highlighting the built-in shock-sensing chip-based technology analogous to the air-bag crash systems being fitted to modern cars. The chip can sense a fall and brace the drive for the shock before it happens: it will survive a 1m drop on to concrete.

Manufacturing techniques borrowed directly from the watch making industry contribute to shock resistance. Indeed, HP has signed up Japanese watch maker Citizen to manufacture its new generation of mini hard drives..

The reliability of mini hard drive technology is also improving. HP is claiming a mean time between failures of 300,000 hours – over 34 years. Seagate claims 250,000 hours for its 1.8in drive.

The Kittyhawk mechanical module is designed to perform 100,000 start/stops without failing, over 100 times a working day for five years. This compares directly with the 100,000 read-write cycles available to eeprom type memory.

The use of different materials adds to the ruggedness and reliability of the mini drive. HP has opted to use sputtered, thin film glass-based media to make the double deck 1.3in diameter disks rather than conventional aluminium substrate media. Glass is stronger than steel in its unblemished form.

The material also has the advantage that it is inherently smoother than aluminium allowing the read/write heads to fly round closer to the surface.

But semiconductor mass memory scores in power consumption. Both HP's and Seagate's newly launched mini drives require 5V power supplies rather than the 3.3V standard that is emerging for battery powered handheld electronic devices.

"Its our firm intention to go to 3.3V as soon as we can," said HP market development manager Dayrell Drake. This will happen as soon as we can implement the full drive control chipset on a 3.3V process, he said. And Seagate president Alan Shugart said that his company is also developing drives capable of running off 3.3V power supplies.

Flash also offers quicker access than hard drives. But the new HP mini drive powers up in 0.75s, has an average seek time of 18ms, a data transfer rate of 0.9Mbyte/s and a latency of 5.6ms. These should all improve as mini drives shrink further.

Capacity of mini drives also looks set to grow. The use of glass disk media has helped push the along track storage density up to 20,000 bits per linear cm and a track density of 945 tracks per cm. (Compared with 18,900 bits per inch and 780 tracks per inch on 1.8in drive technology).

That works out at a storage density of around 20Mbits per square cm. Densities of 330Mbits per square cm have been achieved in the laboratory and will eventually lead to 350Mbyte capacity double-platter mini drives. Currently, Kittyhawk only makes use of three of the four available storage surfaces, although new small head technology should allow all four surfaces to be used and may even make four-platter gigabyte drives possible.

Mini drives will be battling with flash memory for control of the potentially huge market for plug-in memory cards as well as going into the traditional hard drive market for built-in mass storage.

HP is already said to be working on a 0.9in version. **LC**

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Are you still waiting for your *LM12458* sample pack? We know that quite a few people are and the reason is simply that National Semiconductor has been overwhelmed by the response to this offer.

Please have patience. All requests will be honoured although it might take another eight weeks to do so.

Meanwhile, if you have a commercial application which is being held back through lack of a sample pack, you are invited to contact National Semiconductor at its Swindon office: the company has held back a few packs for this contingency.

Editor

Shining prospect for cheap lasers

A research team at Bell Northern Research, a division of Northern Telecom, Canada, claims to have made a breakthrough in semiconductor laser design which will result in powerful, low cost devices for all branches of the public switched network.

The new device, smaller than a grain of salt, is called a circular-grating surface emitting laser. It emits a powerful, collimated circular column of light from its top surface that notably improves the coupling efficiency of laser light into optical fibres. In contrast, conventional lasers generate a divergent light beam that requires a precise positioning of the fibre to capture the light efficiently.

The new laser uses a circular grating, similar in appearance to the tracks of a compact disc, to reflect light upward. The grating, only a fraction of a millimetre in diameter, consists of hundreds of concentric grooves, critically spaced to collimate the beam from an area 10,000 times larger than conventional lasers. The resulting low-divergence beam closely matches the numerical aperture (acceptance angle) of the fibre and facilitates the transfer of optical signals.

The active device is a multilayer laser structure of indium-gallium-arsenide-phosphide (InGaAsP), grown on an indium phosphide (InP) substrate that produces a wavelength of 1.3μm.

Because its surface emitting design can be fabricated as laser arrays, circular grating lasers could be integrated into advanced applications such as optical switching, optical computing, and optical backplanes.

BNR estimates that its new laser could reduce the price of telecomms quality lasers to tens of dollars, an order of magnitude reduction.

***Remote sense:** Fresh air, solitude and a healthy life-style. What more could the villagers of Kilchiaran on the remote and beautiful Scottish island of Islay want? A digital telecommunications network it seems. That at least is the view of BT and the Highlands and Islands Enterprise. In a joint exercise they are spending £16 million to link the Islands into the digital world. Surely only the introduction of multi-story car-parks now stands between the islanders and complete integration into the 1990s.*

Air robots fail challenge

The 1992 International Aerial Robotics Competition, organised by the Georgia Institute of Technology brought teams from eight colleges, more than twice as many as joined the first event in 1991. Four of the machines were able to fly at least briefly under their own computer control, and only one crashed.

The task of finding, retrieving and flying metal disks across a three-foot barrier was still too difficult for the student-built craft, which were designed to fly without a human operator.

But Georgia Tech is not discouraged: "We had more vehicles flying this year, and more vehicles flying autonomously for at least a portion of their flights," said Rob Michelson, vice-president of the Association for Unmanned Vehicle Systems, the event's sponsor. "They are moving toward longer and longer flights in which the vehicles are using their own sensing and intelligence to fly by themselves."

The armada of air vehicles assembled in Georgia Tech's Bobby Dodd Stadium included several helicopters, a billowing grey blimp, a "tailsitter" aircraft and the top scoring vehicle: a "flying gyroscope" based on a toy store hula-hoop and built for $700.

After nine hours of flying and attempting to fly under the blistering sun, a panel of judges awarded prize to three home town teams: $5000 to the Georgia Tech builders of the "flying gyroscope," $3000 to the student builders of a helicopter from the Southern College of Technology in Marietta, and $2000 to a second Georgia Tech team also fielding a helicopter.

Virtual certainty for space

Scientists at Nasa's Ames Research Center are researching the possibilities of virtual reality as a tool for planetary exploration. A prototype multi-sensory virtual workstation contains a custom-built, head-mounted stereo video display, fibre optic gloves and magnetic motion trackers. It recognizes voice commands and can talk in its own electronic speech.

Researchers hope that virtual-reality tools will allow astronauts and scientists to get a feel for computer-generated worlds. For example, it will let scientists plan optimal routes for robots and humans to explore the surface of the Moon and Mars. Astronauts can also try out space repair tasks and perfect their skills before they launch.

With Nasa's developing technology, researchers can also study the flow of air over an airplane or spacecraft from any angle, or take a supposedly realistic voyage into the heart of a black hole.

The virtual system contains a computerised description, known as the database, in which a user can study and manipulate objects. This database can be a physical place, such as a planet's surface created from digitised images sent back by space probes but it can also be abstract ozone levels at various heights in the Earth's atmosphere.

Nasa's system is capable of rendering 4000 flat-shaded polygons in 1/30th of a second, thus allowing smooth real-time animation of scenes of moderate complexity.

MC

MISSING...

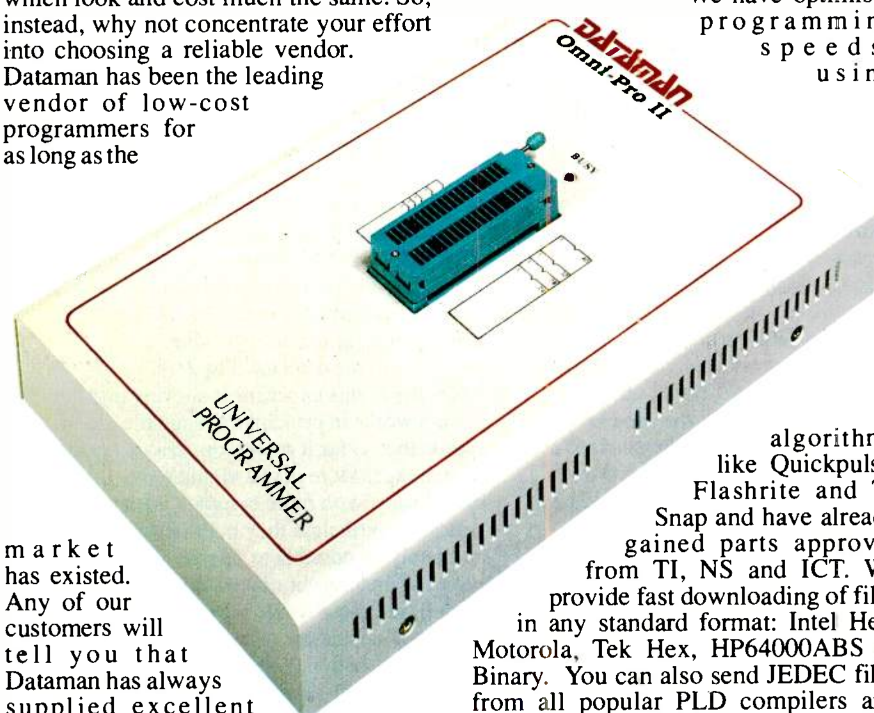
CUTTING ANTENNA TESTING DOWN TO SIZE – *July issue*: Those who read Mike Christieson's excellent article about antenna modelling in last month's issue may have been left wondering about the identity of the supplier of the equipment which formed the basis for the article. It was Feedback Instruments Ltd of Crowborough, 0892-663719 without whose assistance this article would not have been possible.

...LINK

ABI ELECTRONICS: Last issue subscribers missed out on an information insert prepared by ABI Electronics and circulated with newsstand copies. This issue we have included that information in the details of the Professional Sertvices offer - see p.658.

Editor

Omni-Pro II - The Next Generation



When you get a new product, what are your main concerns? Freedom from frustration is certainly one important consideration, for your time is valuable. You will want a product which is reliable and sophisticated, yet simple to use, with clearly written documentation. You will be looking for a high standard of technical support and regular upgrades for the product.
We at Dataman recognise how difficult it can be to choose between programmers which look and cost much the same. So, instead, why not concentrate your effort into choosing a reliable vendor. Dataman has been the leading vendor of low-cost programmers for as long as the market has existed. Any of our customers will tell you that Dataman has always supplied excellent well-supported products. That's why we're still here! We take technical support seriously. We give you your money back, if you're not satisfied. These are important points to consider. But now let's take a look at some of the special benefits of owning Omni-Pro II.

What Benefits?
Well, for instance, the interface is not via the computer's parallel port, which is speed-limited, and probably connected to your printer. A dedicated plug-in half card performs fast data transfers.
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RESEARCH NOTES

How to sneak up on a submarine

A new "silent" method of detecting underwater objects offers the chance to track submarines without the submariners being aware that they are under observation. The technique is entirely passive – unlike sonar, the acoustic equivalent of radar – and no sound is emitted from the equipment itself, making it ideal for any covert form of monitoring.

Fundamental to the new technique – described by researchers from the Scripps Institution of Oceanography in La Jolla, California, and Florida Atlantic University (*Nature*, Vol 356 No 6367) – is the presence of a continuous and continual spectrum of underwater background noise. At all frequencies up to around 50kHz there is a constant wash of sound created by breaking waves and by wind on the sea surface (Fig. 1).

Because of the obvious analogy with white light the researchers describe it as acoustic "daylight", and what they are now working on is the acoustic equivalent of daylight photography.

But compared with photography, the use of natural underwater noise is fraught with difficulties, the most limiting of which is sound absorption in the ocean. Although acoustic energy travels better in water than in air, the team reckons that a useful detection range for their system would be about 1km at 20kHz. Lower frequencies suffer less attenuation, but would offer much less in terms of angular resolution.

Even at 50kHz – considered the maximum practical limit where thermal noise swamps ambient noise – the wavelength of sound in seawater is around 3cm. This is around 100,000 times longer than the wavelength of green light in air. The researchers admit in their paper that an acoustic system would need an aperture of around 600m to achieve a similar resolution to the human eye!

Nevertheless they say that a very useful performance could be achieved by image enhancement techniques of the sort used in synthetic aperture radar and infra red remote sensing. They add that, unlike active sonar systems, acoustic daylight techniques would actually benefit from unwanted noise sources and from multipath reflections underwater. This would make them idea for use in harbours, estuaries and in the vicinity of oil rigs.

To test the principle, a 1.22m diameter parabolic reflector fitted with a low-noise hydrophone was lowered off the end of the Scripps pier. Three rectangular plywood targets 0.9m x 0.7m were then lowered into the sea about 7m from the reflector; they could be rotated on a vertical axis, thus making them alternately "visible" and invisible' to the detector (**Fig 2**).

Results of this experiment showed that the system works in principle, though the group admits that so far it represents just one pixel of an image. More pixels would require more beams with more complex acoustic optics. Nevertheless they believe it should ultimately be possible to display a colour image of underwater objects on a screen. Such false colour would represent the frequency-dependent reflectivity of the objects in question. Even without the colour, an acoustic daylight system would offer what no current active systems offer – a pictorial output that can be interpreted by untrained operators.

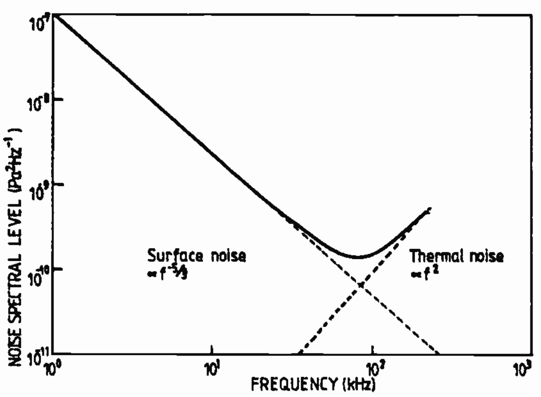


Fig. 1. At all frequencies up to around 50kHz there is a constant wash of sound.

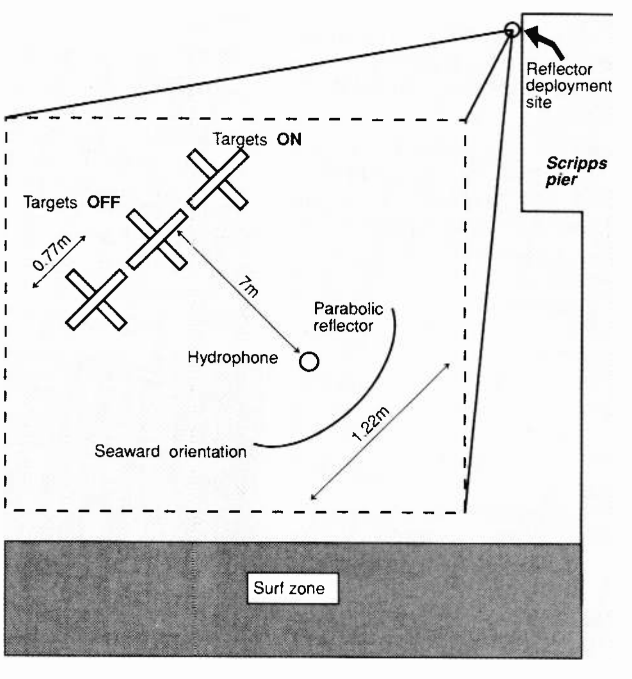


Fig. 2. Evaluating underwater testing using ambient sound.

Hot tip for a Braille interface

Blind people may find it a little easier to make more effective use of computers thanks to a development by electronics engineer Gilbert De May and psychologist Andre Vandierendonck of the University of Ghent in Belgium. De May and Vandierendonck have built a new output device that translates electrical signals into Braille that can be read with the fingers. But unlike existing electromagnetic readers or Braillers that use paper or raised pins, the Belgian device translates the signals into heat.

De May says that the technology is really nothing more than thick film resistance elements printed onto a ceramic substrate. The individual elements are dots 0.25mm across and arranged in the standard Braille pattern, ie a vertical 3 x 2 matrix. The eventual idea is to stack the units so as to make 80 characters available at once. Each character is switched off immediately it has been read so as to prevent the substrate heating up and destroying the heat differential.

At the moment the researchers are testing prototypes on both blind and sighted people and the results are encouraging. They reckon that the use of eight instead of six resistors will enable the system to create not just Braille, but also normal english characters and mathematical symbols. Given several rows of characters, it should also be possible to make graphics that are readable by blind people.

Depending on how much support is forthcoming from industry, De May believes it ought to be possible to produce a whole screen thermal reader for no more than £350. This compares with several thousand for current 80-character electromagnetic device.

Sensitive technology: blind computer users could benefit from a new device which makes use of heat to convey alphanumerics and graphics.

Reversing the effects of electric shock

Future victims of high voltage industrial accidents may have a better chance of recovering from the associated severe tissue damage. The possibility has been opened up by researchers at the University of Chicago Medical Center who claim to have demonstrated, for the first time, the ability to repair damaged cell membranes in the body.

Their treatment, described in a paper published in May in the *Proceedings of the National Academy of Sciences*, depends on intravenous injection of an industrial emulsifier – a poloxamer – to prevent and even reverse much of the damage caused by severe electrical trauma.

Dr Raphael Lee, author of the paper, says that although the work has so far only involved animal organs there is clear evidence from tissue culture studies that the substance is just as effective at restoring the damaged membranes of human cells. Clinical trials in humans with life-threatening or limb-threatening injuries caused by high-voltage electrical energy are expected to begin next year.

In a series of studies, Lee and colleagues Philip River, Fu Shih Pan and Robert Wollman, exposed muscles, which were still attached by the artery and vein to the hind legs of rats, to high-voltage supply, simulating a typical industrial accident. The shocks were strong enough to cause severe damage to the muscles – the tissue most vulnerable to electrical trauma – but brief enough to avoid the excess tissue heating caused by extended contact.

Each rat showed immediate evidence of tissue damage in the shocked limb. Electrical impedance, a sensitive measure of all membrane damage, fell abruptly by 50%.

Twenty minutes after the shock, the rats were injected with either poloxamer, a saline solution or a solution of saline plus neutrally charged dextran. Rats which received the poloxamer showed dramatic and lasting recovery. Within 15min, the electrical impedance in the isolated muscles returned to 77% of normal, enough of a recovery to rescue the tissue. "The recovery was not complete," says Lee. "But the critical defect, damage to the cell membrane, was apparently repaired and the cells remained viable."

Although an estimated 2500 Americans each year are victims of industrial accidents resulting in severe electrical trauma and another 1000 to 1500 are hospitalised for injuries caused by lightning, fundamental research into the precise mechanism that causes those injuries is still in its infancy.

Mechanism revealed

Progress in treating electrical trauma has long been hampered by misunderstanding of the basic mechanism of tissue damage caused by an electrical current. Until recently, the damage was primarily attributed to thermal mechanisms, excessive heating in the region through which the current passed. In many electrical trauma victims, the thermal injury may be less important; cell-membrane damage resulting from exposure to a strong electric field is probably the central event leading to tissue death.

Cells in a current's path, Lee has demonstrated, are damaged by a process called electroporation. Electric forces bore minute pores into the cell's membrane, which allows substances outside the cell, primarily calcium and sodium ions, to flow in unregulated. If the pores become large enough, the cell ruptures, spilling out its contents like a water-filled balloon pricked with a pin.

The timing of cell death is also unusual; tissues damaged by pure electrical forces can appear perfectly healthy hours after the injury and still not survive.

While nothing can salvage the charred cells near the points of contact with a powerful electrical current, there is a window of opportunity for cells damaged primarily by electroporation. From 30min to as long as a few hours after contact, even perforated cells can be saved. The injected poloxamer is taken up by damaged cells, where it apparently seals the tiny leaks in the membranes and allows the repair process to begin.

Details of timing, dose and methods of delivery of poloxamer – as well as new diagnostic tools to assess electrical damage prior to treatment and measure the effects of therapy – are still being refined. Lee and his colleagues hope to begin clinical trials of poloxamer for electrical trauma victims once the precision of these diagnostic tests has been confirmed.

Since the chemical has long been approved by the Food and Drug Administration for other medical uses, this finding sets the stage for the development of effective medical therapy for victims of high-voltage electrical shock.

The magnetic attraction in all of us

Molluscs, bacteria, honeybees, pigeons and salmon all have it – and so do human beings according to a team at the California Institute of Technology: magnetic sense.

Researchers, led by Dr Joe Kirschvink, have reported isolation of microscopic crystals of the magnetic mineral magnetite from samples of human brain tissue. Presence of the magnetite may explain a variety of observations from the apparent existence of a primitive human magnetic sense, right through to some of the possible biological effects of electromagnetic fields that have been hotly debated in these pages.

Kirschvink's paper: "Magnetite Biomineralisation in the Human Brain," has been accepted for publicity in the *Proceedings of the National Academy of Sciences* and was recently revealed at a news conference hosted by Caltech.

The presence of magnetite in biological materials is something that has been known for a long time, and the fact that it has now been demonstrated in human tissue is therefore no great surprise. But it does provide a plausible mechanism for the ability of humans to sense or react to electromagnetic influences. This is especially so since the magnetite crystals are not only permanently magnetised, but also exhibit metallic-type electrical conductivity.

The scientists obtained samples of human brain material from the Alzheimer's Disease Research Center Consortium of Southern California. The samples came from autopsies of seven patients within 12 to 24 hours after their deaths. (Four of these patients were suspected of having Alzheimer's Disease, and three were not. The researchers noted no systematic differences between the brains of the Alzheimer's patients and the others in their magnetic characteristics.)

To avoid possible metallic contamination, brain samples were dissected using ceramic or Teflon-coated instruments. The samples were transported to a magnetically shielded, dust-free clean room within Kirschvink's Caltech laboratory. In this room elaborate precautions are taken to keep microscopic dust particles, some of which are magnetic, from contaminating the samples or the chemicals used in their preparation.

Kirschvink says he is struck by the similarities between the human magnetite and the magnetite found in magnetic bacteria. Magnetic bacteria sometimes have long strings of magnetite crystals organised in cellular organelles called magnetosomes. These bacteria clearly use the magnetosomes to sense the Earth's magnetic field. Bacteria swimming in a pond could use information about the Earth's magnetic field to tell up from down, as long as the pond wasn't right on the equator, since magnetic field lines descend into the Earth's interior. A bacterium that wanted to go down, away from the surface and toward the nutrient-rich mud on the bottom, would follow the north pole of its magnet in the northern hemisphere and the south pole of its magnet in the southern hemisphere."

Kirschvink emphasises, however, that the amount of magnetite in the human brain is tiny – less than 70ng/g of tissue. It is so little that he doubts if it will ever be found *in situ*.

He is also unsure about the practical significance of his discovery. "Our studies of the magnetite crystals we isolated from human brain tissue show that they could be moved around by magnetic fields only slightly stronger than the Earth's natural magnetic field. If, for example, these crystals are coupled to ion channels within human cells, electromagnetic fields could be opening and closing these channels, with unknown biological consequences."

Kirschvink says he knows his study has the potential to be misunderstood. "I want to be absolutely clear about what I am saying and what I am not saying. Yes, there is magnetite in human brain tissue. Yes, it is possible that the presence of magnetite may mediate any health effects of electromagnetic fields. But in my opinion, the jury is definitely still out on whether electromagnetic fields actually do have health effects."

He also states, explicitly, that he as yet sees no evidence that humans have a magnetic sense. ■

Research Notes is written by John Wilson of the BBC World Service

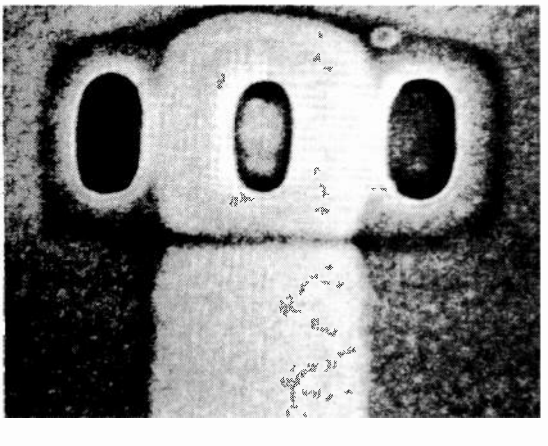
World's smallest mosfets

A team from IBM's Thomas J Watson Research Center in Yorktown Heights, NY, claim to have made the world's smallest transistors. These experimental devices – n-channel mosfets – are a mere 700nm by 150nm and are enclosed by an isolation trench 150nm wide. Within this structure is a gate electrode of 100nm by 150nm, while source, drain and gate contacts measure 150nm by 200nm.

The IBM team, who presented details of their achievement at the 36th International Symposium on Electron, Ion and Photo beams, in Orlando, says that overlay and fabrication tolerances need to be within 25nm for all levels of the device. These tolerances were achieved using special electron beam nanolithography fabrication techniques which IBM says are not necessarily appropriate for mass production at the present time.

The new transistors, which operate at room temperature, are scaled down versions of conventional mosfets and work along entirely conventional lines. This is in spite of the fact that the dimensions are in the size range where quantum effects would be expected.

Work is now going on to optimise the device characteristics and to test them as part of prototype high speed logic and memory circuits. The intention is to implement them in cmos and eventually to create 4Gbit dynamic random access memory chips within the first decade of the 21st century



Smaller than a wavelength of visible light. IBM's mosfets may eventually find themselves in gigabit memories.

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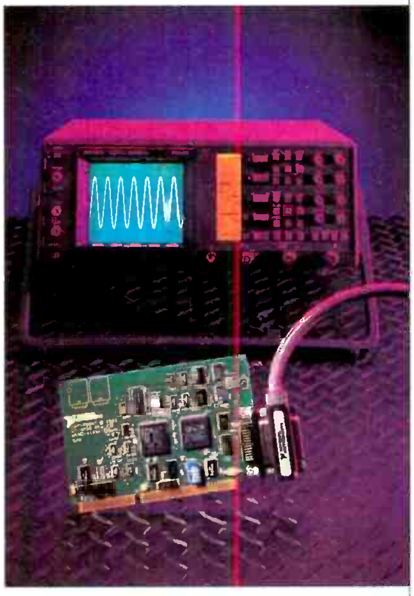

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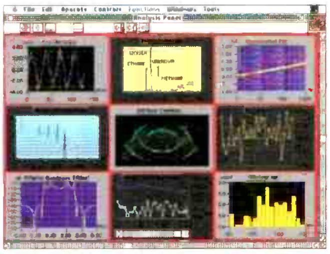

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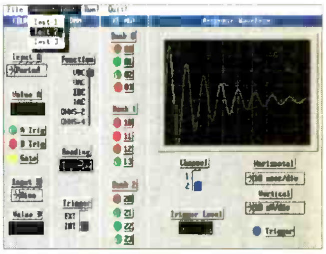

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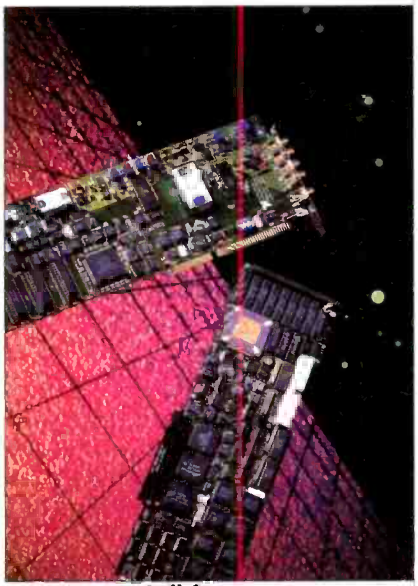

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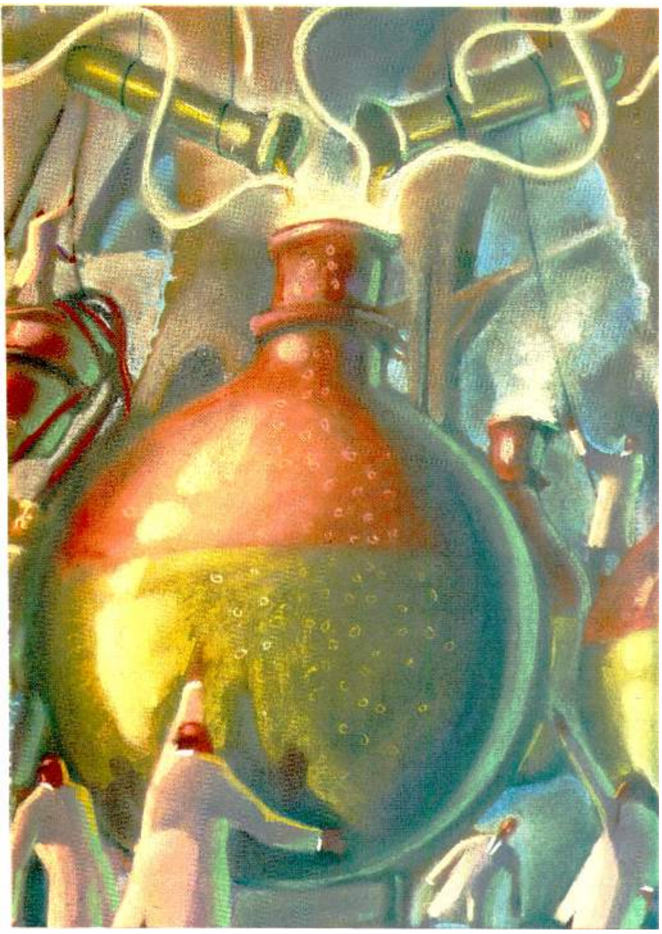


DIRECT DIGITAL SYNTHESIS

Direct digital synthesis is changing the way that RF engineers design radio systems. Capable of producing stable, clean carrier waves well into the UHF spectrum, these systems lend themselves to chip integration and require few, if any, conventional RF components. A new design series by ***Ian Hickman.***

There has been a steadily increasing degree of interest, especially in recent years, in direct digital synthesis. The technique emerged in the early '80s and was probably known in principle for several years before that.

In those early days, the highest output frequency attainable was no more than a few MHz, limited by the performance of the logic ICs and dacs (digital to analog converters) then available. A prototype DDS at the Roke Manor laboratories of the then Plessey company in 1981 occupied several complete boards of logic laid out on the bench and, being clocked at 10MHz, provided an output frequency of up to about 3MHz, with all spurious responses about 40dB down on the wanted output.

Since then, with advances in semiconductor technology, the attainable performance has increased by leaps and bounds: DDS chips realised in gallium arsenide now provide output frequencies of over 400MHz. Silicon technology delivers output frequencies in excess of 300MHz. However, at least when operating at the top end of their frequency range, the worst case levels of spurious outputs have not changed much, still being in the region of 40 to 45dB down on the wanted output. The reasons for this will be covered later on but, before looking at the advantages and limitations of DDS in detail, it will be useful to compare it with the various other methods used for the generation of an RF carrier.

The temperature and long term frequency stability of an LC oscillator is generally poor; it is difficult to construct a small inductor with a stability of much better than 0.01%, while its spectral purity (noise sidebands) can only be reduced by increasing the operating Q of the tuned circuit. This again is not easy especially in miniaturised equipment: a working Q in excess of 100 is good going at HF, although at V/UHF and microwave where cavity resonators become feasible, a Q of thousands is possible.

In fixed frequency applications, the situation is much more rosy; a crystal resonator can have a Q in the range 10000 to a million, making it possible to design oscillators with very low sideband noise and excellent temperature and long term stability, especially if the crystal is maintained at a constant temperature in an oven.

Direct synthesis

The ideal carrier generator would be one with the tuning capability of an LC oscillator but the stability and purity of a crystal oscillator – and the next major advance in frequency generation provided just this.

Clearly, with just two crystals, at frequencies f_1 and f_2, one can obtain four different frequencies by mixing them so as to provide also $(f_1 + f_2)$ and $(f_1 - f_2)$, while if you use harmonics or subharmonics of f_1 and f_2 as well, the possibilities rapidly increase. This principle can be extended to any frequency to be generated and with any desired degree of resolution.

This system was called a direct synthesiser, since ultimately the output frequency was obtained from one master crystal oscillator and had almost the purity of this master. A good example was the General Radio *1160 series* of lab bench synthesisers, where additional decade plug-in units could be added to provide as many significant digits of resolution as required (at a price). The term "direct analogue synthesiser" is sometimes now used to describe this type of instrument, to distinguish it from the direct digital synthesiser. The basic operating principle of the direct synthesiser is ingenious, see **Fig. 1**.

Although different manufacturers used frequencies differing from those shown, the principle was the same. It can be seen that the output frequency is the same as the input frequency, but that the resolution has been increased by a factor of ten. So if the output is used as the input to another similar block of circuitry, a 1MHz tuning range with 10kHz resolution is available. This scheme can then be further extended with additional blocks to obtain whatever resolution is required. Note that Fig. 1 only uses seven fixed frequencies to obtain the ten output frequency steps, and that all additional modules will use only these same seven frequencies, all of which can be obtained from the synthesiser's internal 10MHz reference source, or from an external 10MHz frequency standard if required. The divide by ten stage at the output of the block reduces by 20dB any phase noise and spurious outputs which may have been introduced in obtaining the reference frequencies and in the mixing processes.

The scheme can be simplified somewhat by adding resolution a factor of two (one bit) per stage, instead of a factor of ten per stage and this scheme was adopted in the Ailtech *model 360* signal generator and derivatives, now out of production. The result was exceptional output purity – sideband noise of –100dB at 10Hz off tune and 1Hz resolution over a 1GHz range. The only disadvantage was cost; also size and weight if you had the job of moving it from one lab to another! Other advantages of direct synthesis include a very fast frequency change capability (switching speed in the microsecond region) and very low non-harmonically related spurious outputs, typically -80dB.

Where high purity, low spurious outputs and fast switching are all required, direct synthesis is an attractive route, at least in the case of lab and ATE equipment, but the size and cost make it difficult to apply in portable, military or OEM equipments.

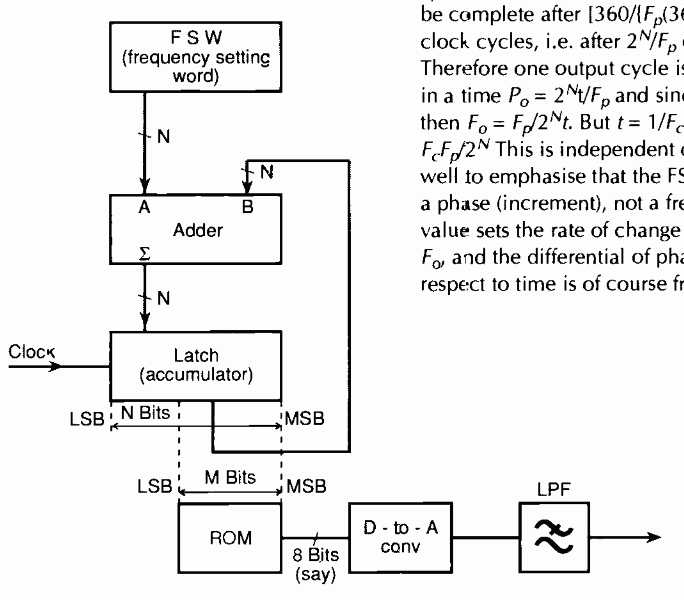
The phase locked loop

The next technology for carrier generation was the PLL (phase lock loop) technique. This is widely applied in space applications, e.g. for synchronising a receiver to a space craft signal with Doppler shift, or a varying shift if the craft is tumbling or spinning, an application described in Reference 1. An even earlier application was in the NTSC system, to lock a crystal oscillator in the receiver, operating at the frequency of the colour sub-carrier, to the burst of colour sub-carrier at reference phase occurring on each line of the transmitted television signal; in this case the locally generated signal is at the same frequency as the incoming or reference frequency.

SETTING THE RELATIONSHIPS

Designate the clock frequency as F_c with $t = 1/F_c$ being its period, the output frequency as F_o with $P_o = 1/F_o$ being its period, and the current value of the FSW as F_p. Let the accumulator be N bits wide and let the most significant M of these control the rom (which it is assumed holds one complete cycle of sinewave). Thus $2M$ bits correspond to 360° so that (referring to the figure) the MSB of M (and N) corresponds to 180° and the LSB of M corresponds to $(360/2M)°$.

Likewise, the LSB of N corresponds to $(360/2^N)°$. $(360/2^N)°$ is thus the smallest possible phase increment and the phase of F_o must advance by at least this amount in time t. The value F_p of the FSW thus corresponds to a phase increment of $F_p(360/2^N)°$ and one cycle will therefore be complete after $[360/\{F_p(360/2^N)\}]$ clock cycles, i.e. after $2^N/F_p$ clock cycles. Therefore one output cycle is completed in a time $P_o = 2^N t/F_p$ and since $F_o = 1/P_o$, then $F_o = F_p/2^N t$. But $t = 1/F_c$, so $F_o = F_cF_p/2^N$ This is independent of M. It is as well to emphasise that the FSW is actually a phase (increment), not a frequency. Its value sets the rate of change of phase of F_o, and the differential of phase with respect to time is of course frequency.



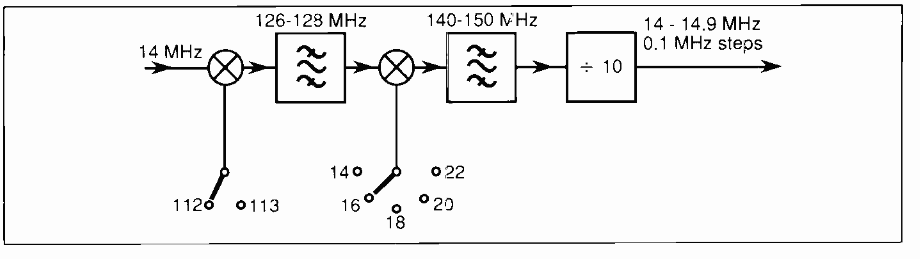


Fig. 1. Principle of the conventional direct synthesiser. The mix\filter\divide block provides 100kHz steps. Using the output as the input to another similar block provides an output with 10kHz steps. Further blocks can be added to provide any required degree of resolution. High performance filters and careful screening within and between blocks enable all non-harmonically related spurious to be held at 80dB down on the wanted output, at a price.

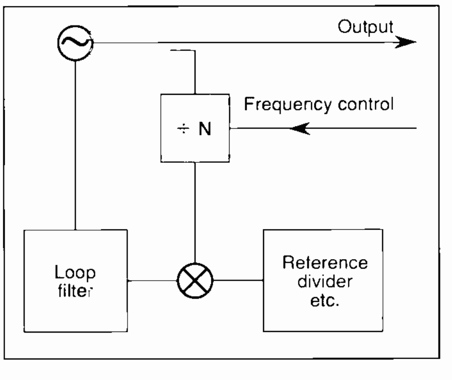


Fig. 2. Principle of the phase-lock loop synthesiser. A sample of Fout, the output of the VCO, is divided by N and mixed with a reference frequency F_{ref}. When these two frequencies are exactly equal the loop is said to be in lock with a DC component in the mixer's output. This is extracted by the loop lowpass filter and applied to the VCO's tuning input: the overall loop feedback is negative and maintains equality between F_{out}/N and F_{ref}. Additional measures are often employed to assist loop lock-up and further arrangements can enable N to be effectively non-integer.

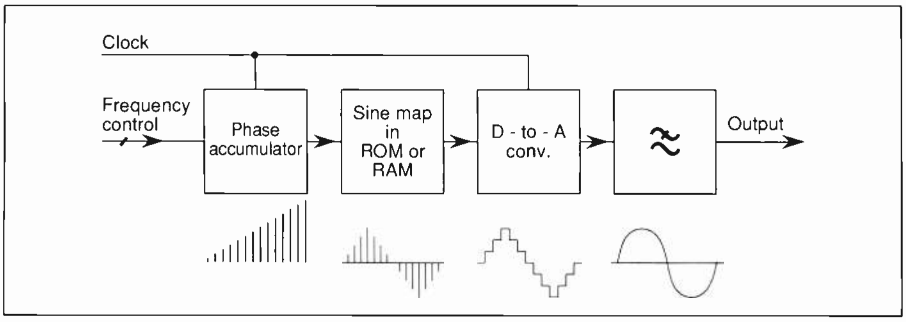


Figure 2 shows the block diagram of a system for producing an output at N times the reference frequency, which may itself be obtained directly from a crystal oscillator, or be a sub-harmonic of it obtained by divider circuits. When the loop is in lock, the output of the divide by N stage is at exactly the same frequency as the reference, but there will be a small phase offset, leading or lagging, resulting in a DC component in the output of the mixer. This is applied (often after amplification) via a lowpass filter to the varactor in the voltage controlled oscillator and results in exactly the desired output frequency.

If N is set to a different value, the output frequency will change; thus if N is changed to, say $N + 2$, the output frequency will increase by twice the reference frequency. Special arrangements, not considered here, are used to ensure that the loop locks up at the desired frequency. Figure 2 shows an elementary single loop indirect or PLL synthesiser, where the step size is equal to the reference frequency. Enhancements of the technique such as dual modulus prescalers and a multiple loop architecture enable fine resolution to be obtained comparatively cheaply. A "fractional N" approach enables the performance/price ratio to be improved even further making the PLL synthesiser currently by far the most commonly encountered scheme. PLL synthesisers can offer fine frequency resolution and very low levels of spurious outputs at comparatively low cost, but cannot achieve the same very low levels of close-in phase noise as the direct synthesiser. furthermore it has inherently slow switching times, due to loop filter settling time.

Fig. 3. Principle of the direct digital synthesiser. A frequency control number is added into the phase accumulator on every clock cycle. The most significant bits of the accumulator address a sine look-up table in rom or ram. The output of this is passed to a dac, whose output is a stepwise approximation to a sinewave. Lowpass filtering exerts a flywheel effect, smoothing the waveform and suppressing harmonics.

Direct digital synthesis

This brings us back to the latest carrier generation technology, DDS. The basic procedure is shown in outline in **Fig. 3**. With the exception of the output lowpass filter, the whole scheme is entirely digital and eminently suitable for large scale integration onto a single chip. The output frequency is directly proportional to the magnitude of the frequency setting word, labelled frequency control in Fig. 3.

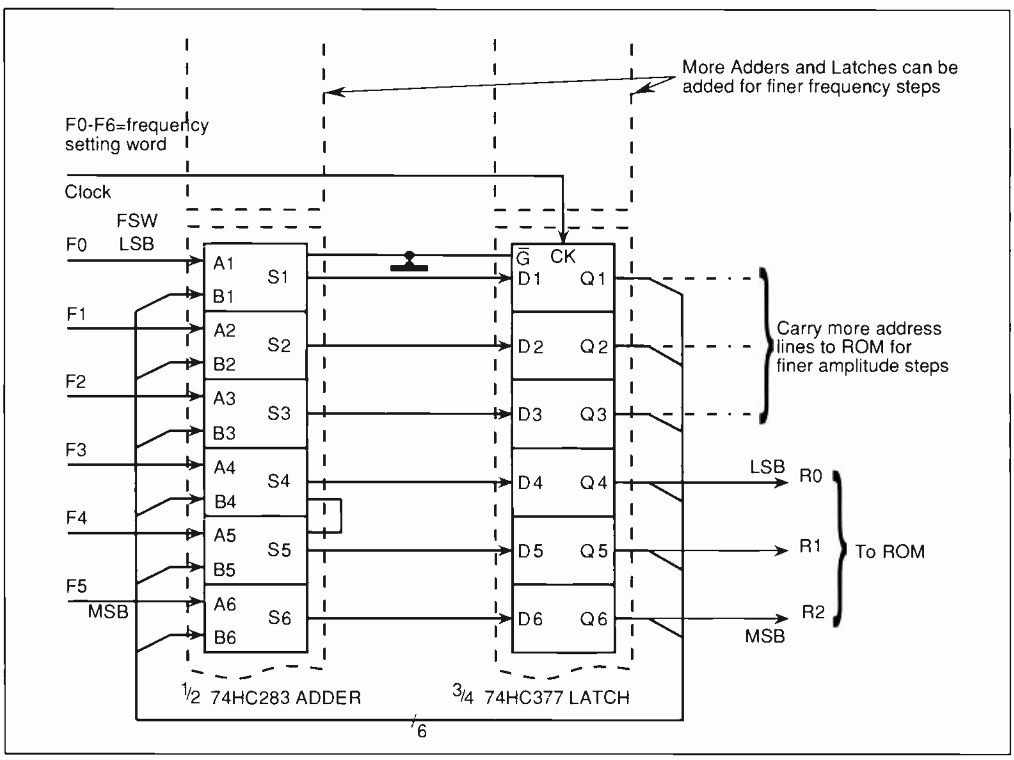


Fig. 4. Part of a practical but, for the sake of explanation, exceedingly rudimentary DDS – the phase accumulator. The lowest possible output frequency results when the frequency setting word is 000001. In this case, every eighth clock pulse advances the rom address by one.

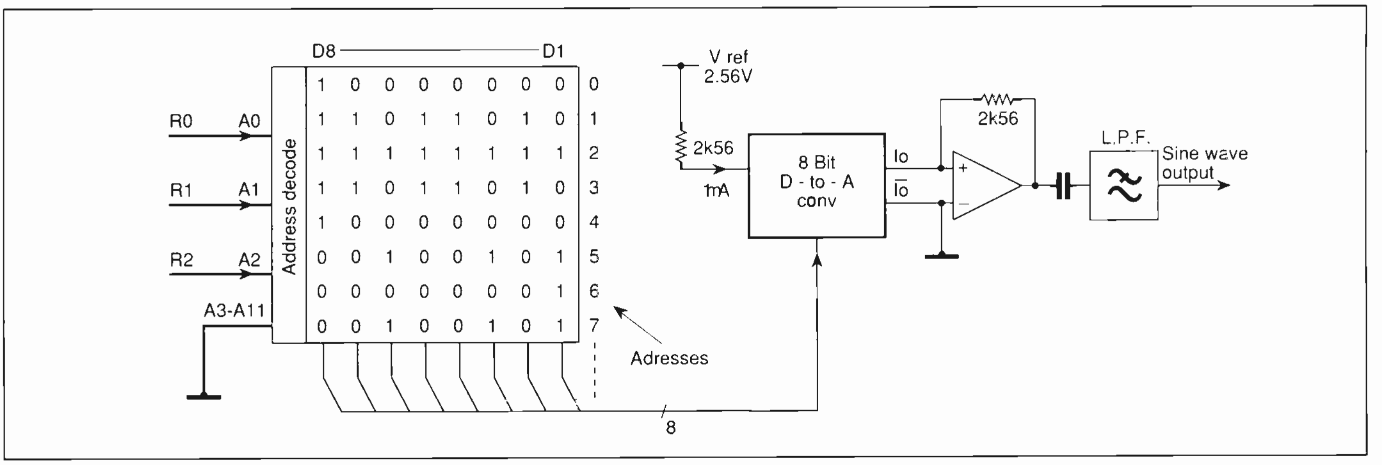
Figure 4 shows how the phase accumulator works. For simplicity, a 6-bit accumulator with the three most significant bits (MSBs) controlling a read only memory with just eight memory locations has been assumed. The three MSBs output from the latch to the rom need to represent one complete cycle of the output waveform, so the eight values in the rom need to represent the amplitude of a sinewave at 45° intervals. The higher the value of the frequency setting word, the fewer clock cycles will be needed to cycle through the rom once, and hence the higher the output frequency.

Figure 5 shows the rest of the rudimentary system, the rom, dac and output filter. (Only the three least significant rom address lines have been used in this system, which is deliberately crude for purposes of explanation. In a real DDS system, there would probably be between 18 and 32 frequency setting input lines, with the top eight or more addressing the rom.) The values stored in the rom range from one, representing the negative peak of the sinewave to 255, representing its positive peak and define points on a sinewave in offset binary, where the value 128 corresponds to the 0V mean level of the waveform. One to 255 represents an odd number of levels and this is convenient since a sinewave is symmetrical about the mid level, this is one of the subtle points that many explanations of DDS tend glibly to gloss over or ignore entirely. Of course one could use the 0 level as well, but an even number of levels can land you in difficulties, for example if you want to economise on high speed rom by storing only half or a quarter of a sinewave, as is done in some commercial DDS chips.

When using two roms and dacs to produce quadrature sinewaves, one should be at its peak when the other is exactly at mid level – but with an even number of levels this cannot be. However, this is no real problem as long as the two roms are addressed with an address offset corresponding to 90°. It just means that the sinewave is not centred in the rom, and that no address corresponds exactly to peak of the sinewave.)

Operation

Imagine the 6-bit latch clocked at 64Hz and the accumulator (Figure 4) loaded with 000001, i.e. just a 1 in the LSB. Whatever the current value held in the latch, the output of the adder will exceed this by one. So on the next clock pulse this new value will be loaded into the



latch, and so on repeatedly. Starting from the state where the latch content is all zeros, the three rom address lines will all be zero so the rom will output 10000000, causing the dac output to be 1.28V, corresponding to the zero value of a sinewave at 0°. The output of the LPF (lowpass filter) will indeed be 0V, due to the blocking capacitor between it and the op-amp, the purpose of the latter being to turn the dac's current output back into a voltage. Eight clock cycles later, the accumulator contents will be 001000; R_0 is now a 1 so the rom will output 11011010, corresponding to the offset binary representation of the value of a sinewave at +45° and accordingly the dac output becomes 2.18V. After 64 clock cycles the accumulator is full and the dac will have delivered a complete cycle of a stepwise approximation to a sinewave. Thus the lowest non-zero output frequency is 1Hz, or generally $f_{clock}/2^N$ where N is the number of accumulator bits. This is illustrated in **Fig. 6**. If the FSW (frequency setting word) is changed to 000010, the whole process will complete one output cycle in half as many clock periods, so $f_{clock}/2^N$ is also the smallest frequency increment available.

For those wishing to experiment with a rudimentary DDS system (Figs 4 and 5) built using standard logic, this could be made using two 74HC283 4-bit binary full adders and an 74HC273 or 74HC377 8-bit D flip-flop. The CO – carry out – pin of the less significant adder must be wired to the CI – carry in – pin of the more significant adder, the CO pin of which is unused. The scheme is readily extended using more of the same ICs to a 16 bit register with, say, the eight MSBs controlling the rom. Clocked at 6.5536MHz, this would provide outputs up to about 2MHz with 100Hz resolution.

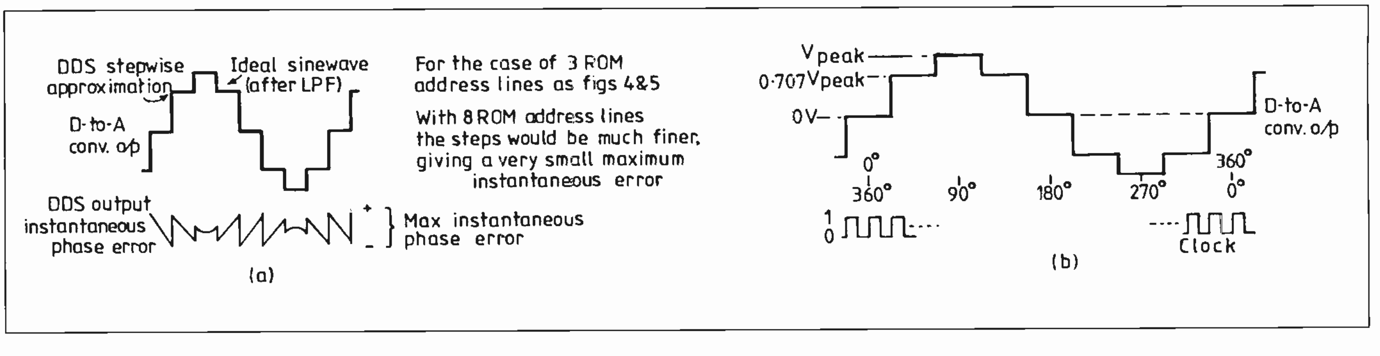
Fig. 5. The rest of the rudimentary DDS. After 64 clock cycles, one complete cycle of (stepwise) sinewave has been delivered from the dac, dwelling for eight clock periods at each step. In practice, an 8-bit latch would probably be interposed in the line between the rom and the dac, loaded by the other edge of the clock waveform from that which increments the accumulator. This would benefit very high speed operation, by preventing any glitches, as the rom output settles, from reaching the dac.

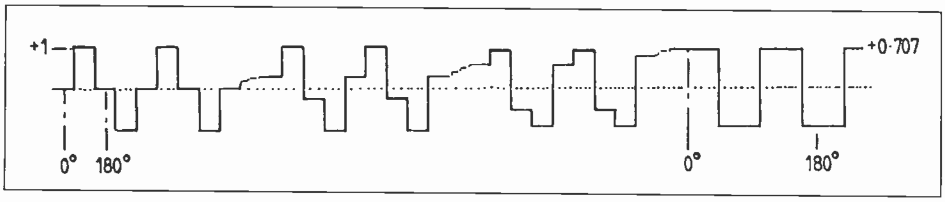
Any byte wide prom such as a 2716 would do, together with the inexpensive dac, the DAC08, though the clock frequency would need downrating somewhat on account of the rom. The values loaded in the rom cause the dac to deliver a peak negative voltage of +10mV, +1.28V representing the sinewave's zero mean level and 2.55V for the positive peak. If you check the intermediate values you will find that 11011010 (binary) or 218 (decimal) is just about what it should be: (218-128)/127 = 0.70866 which is within 0.2% of the correct value of sin(45°), and similarly for 00100101 (sin(25°)).

This raises the important point of the accuracy of the representation in rom of the values of a sinewave. Clearly they must be rounded to the nearest value that can be represented in binary, given the width of the rom, in our example, just eight bits. However accurate the dac, there will be truncation errors in the representation of the sinewave's amplitude, and these will be worse at some steps than others. For a rough and ready sinewave this wouldn't matter, but one would like all spurious frequency components in the output to be 60 or 80dB or more down; remember the DDS has to compete with PLLs, which are very good in this respect. But let's confine attention for now to basic DDS operation.

Figure 6 also shows the instantaneous departure of the output stepwise approximation from a continuous sinewave Clearly these phase perturbations occur at a rate equal to the clock frequency which is well above the highest output frequency and so they can be suppressed by the LPF (which in this case would have a sharp cut-off at about 30Hz), at least if we had a perfect dac with infinite resolution. Amplitude truncation errors will cause the sinewave representation to be imperfect, resulting (in this case) in harmonics in the output: whether these appear in the output depends upon whether they are higher than 30Hz, i.e. on the commanded output frequency. Apart from this possible harmonic content (and harmonics are a fact of life with any other sort of oscillator anyway), the output of the 6 bit DDS is perfect at frequency settings of 1,2,4 and 8Hz. In DDS terms, these are "good" frequencies; at other frequencies, the operation becomes a little more complicated and much more interesting. There are many

Fig. 6. 8Hz and 4Hz outputs from the DDS of Figs 4 and 5, with a 64Hz clock. With eight rom address lines the steps would be much finer, giving a very small maximum instantaneous phase error.
a) FSW (frequency setting word) = 001000, rom address increments by 1 each clock cycle, one cycle of output for each 8 clock pulses: 8Hz output.
b) FSW = 000100, the dac output dwells at each level for two clock periods: 4Hz output.





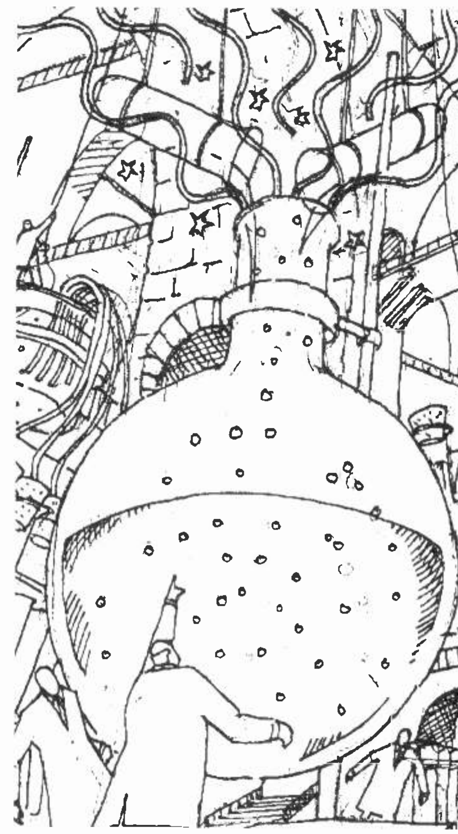
other mechanisms capable of producing unwanted, non-harmonically related spurious outputs. These will be examined in a later article, but for the moment note that when the demanded frequency is so high that the rom only outputs a subset of its contents on each cycle, the waveform into the LPF can take various quite different forms from a sinewave. This is illustrated in **Fig. 7** which shows some of the shapes the waveform can take (when many more than three accumulator lines address the rom) at a good frequency where the rom address is incrementing so as to output just four equally spaced locations. Fourier analysis shows that the amplitude of the fundamental component of all the waveforms shown (which are computer generated and hence to scale) is the same.

Fig. 7. When the output frequency of a DDS equals $f_{clock}/4$, any of the above waveforms (or other intermediate versions) may be delivered from the dac, depending upon the accumulator contents at the instant the FSW was set to produce this output frequency. Many DDS chips include an accumulator reset input, enabling the output to be forced to a given phase after setting the FSW.

References:

1) Phaselock Techniques F *M* Gardner John Wiley and Sons Inc 1966

Next month: operation of a DDS at frequencies other than the good ones that have been considered so far. Unwanted non-harmonically related spurious components in the output; how they arise and what can be done about them.



Even when linear parameters are known, different manufacturers' devices show considerable variation. Terence Finnegan examines operation of power mosfets from first principles to show how linear characteristics can be determined.

Going linear with power mosfets

part 1 of 2

Almost all power mosfets available today have been developed and characterised for their use as resistive on-off switches, and specifications stress the relevant parameters of $R_{DS(on)}$, peak drain current, gate charge, avalanche rating etc.

These parameters maybe vital when the device is used as a simple switch and components external to the mosfet usually control the drain current. But they do not apply at all in linear analogue design. Indeed, an examination of the data sheets shows that linear parameters such as threshold voltage, mutual conductance and dynamic drain resistance are hardly defined at all. Even when these parameters are known for a device, there is a considerable variation between manufacturers.

But we can determine useful linear characteristics, both in theory and practice, by examining the operation of a power mosfet from first principles, using straightforward semiconductor physics. Here we concentrate on the gate threshold voltage V_T, the mutual conductance G_{fs}, the drain-source output admittance G_{os}, and the variation of these parameters with temperature, for both n-channel and p-channel units. Linear high frequency performance is also discussed briefly.

Present design goals

The expression: area x on-resistance = (breakdown voltage)$^{2.5}$ defines the fundamental limitation of power mosfet switching performance. The product of the resistance of a block of silicon and its surface area plotted against breakdown voltage determines this limit – assuming that 100% of the silicon surface is injecting carriers and 100% of the theoretical breakdown voltage of silicon is obtained. But both these assumptions can never apply in real devices and **Fig. 1** shows the present state-of-the-art, including the performance of various contemporary mosfets. The practical limit, defined by the dotted line, assumes an 85% surface utilisation efficiency, to account for bonding pads etc. We can show (see drain current box) that:

$$R_{DS(on)} = \frac{L}{\mu_n C_{ox} W(V_G - V_T)}$$

and manufacturers are concentrating all their efforts on improving the fabrication processes to come ever closer to the silicon limit and reduce $R_{DS(on)}$ to an absolute minimum at the lowest cost for a given breakdown voltage. Different techniques are used to achieve this aim; connecting many cells in parallel to increase W and reducing the channel length L are obvious ones. Unfortunately reducing L has adverse effects on G_{os}, a parameter rarely specified for power mosfets, and there is little or no control over the threshold voltage V_T, the transconductance G_{fs} or the unspecified

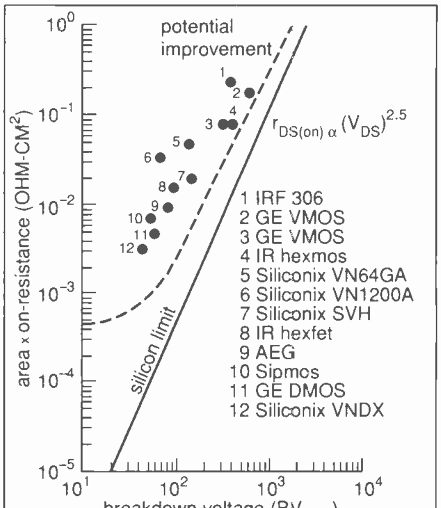


Fig. 1. Review of characteristics showing theoretical performance limits against the characteristics obtainable from a selection of real devices

but fundamental gain parameter β. For example, a comparison of the published data for the *IRF720* from IR has G_{fs} typically 2.7A/V at 1.8A drain current, while the *IRF720* from Siliconix has G_{fs} typically 1.2A/V at 1.5A drain current. The mosfet gain β is a fundamental performance parameter and yet this is

List of symbols

C_{ak}	Anode-cathode capacitance (of valve)
C_{Dch}	Total capacitance from the drain to the active channel
C_{Gch}	Capacitance from gate electrode to active channel
Cgk	Grid-cathode capacitance (valve)
C_{in}	Gate-source input capacitance ($=C_{iss}$-C_{rss})
C_{iss}	Input capacitance (data sheet)
C_{oss}	Output capacitance (data sheet)
C_{rss}	Reverse transfer capacitance from data sheet
C_{ox}	Dielectric capacitance per unit area across the insulating gate oxide
C_{tox}	Total oxide capacitance
E_{G0}	Band-gap energy at 0°K
Gfs	Mutual conductance
G_{os}	Incremental drain conductance in saturated region
I_D	Drain current
I_{Dsat}	Drain current in saturation region
k	Boltzmann's constant
L	Channel length
q	Electronic charge
N_a	Acceptor doping concentration
N_d	Donor doping concentration
n_i	Intrinsic concentration
Q_d	Charge density/unit area associated with depletion region
Q_n	Total charge in the channel
Q_{ss}	Fixed positive charge density per unit area at the silicon silicon dioxide interface
$R_{DS(on)}$	Drain-to-source on-resistance
T	Absolute temperature °K
T_{ox}	Oxide thickness
T_{tr}	Channel transit time
V_D	Drain voltage
V_{Dsat}	Drain voltage at which current saturation occurs, also known as pinch-off voltage
V_G	Gate voltage
V_{G0}	Gate voltage at which I_D has zero temp coefficient
V_{Gch}	Voltage between gate and channel
V_R	Reverse bias across drain junction
v_{drift}	Channel drift velocity
v_{sat}	Carrier saturation velocity
V_T	Gate threshold voltage
W	Channel width
β	Mosfet gain factor
ε_o	Permittivity of free space
ε_{ox}	Permittivity of insulating layer
ε_s	Permittivity of silicon
ε_r	Relative permittivity of material
θ	Channel mobility modn factor
ϕ_F	Fermi potential
ϕ_{MS}	Metal-semiconductor work function difference
μ	Amplification factor
μ_n	Electron mobility in channel
μ_p	Hole mobility in the channel

different by a factor of over four in this instance, showing that the fundamental parameters needed for analogue design are not controlled.

Theoretical power mosfet performance

In the following text all terminal voltages such as V_G, V_T etc are "with respect to the source terminal" unless otherwise specified.

Let us start by reviewing the gate and drain characteristics of a power mosfet, before considering the semiconductor physics which give rise to them. The gate transfer curve of **Fig. 2** defines the variation between the saturated drain current and the applied gate voltage, for a constant drain voltage. There are three distinct regions on this curve and each results from differing conduction phenomena.

In the region *A* to *B*, a small drain current flows, with the gate voltage V_G below the mosfet threshold voltage V_T. Since the magnitude of the current that flows in this sub-threshold region is negligible compared with the maximum current of a device, very little work has been done to characterise power mosfets here. But theory suggests that the drain current increases exponentially with gate voltage. In the region *B* to *C* on the transfer curve, the drain current is proportional to $(V_G{-}V_T)^2$. This square-law is characteristic of all mosfets, both enhancement-mode power devices and depletion-mode small signal devices. After point *C*, the curve gradually becomes linear because the charge carriers tend to reach a saturation velocity, when the gate voltage becomes high enough.

The drain transfer curve of **Fig. 3** defines the variation between the drain current and the applied drain voltage, for a constant gate voltage above threshold. This curve has obviously two distinct regions. In the region below "pinch-off", defined as the saturated drain voltage V_{Dsat}, the drain current increases parabolically with increasing drain volts until a maximum is reached. Above V_{Dsat}, the drain current remains nearly constant at the maximum or saturated value, and is nearly independent of the applied drain voltage thereafter.

Action of the gate

In construction, a typical n-channel power mosfet (**Figs. 4a** and **4b**) is essentially an NPN transistor with the drain junction having an extra lightly doped n$^-$ epitaxial layer inserted between the more heavily doped p$^+$ substrate and the n$^+$ drain layers. (The superscripts denote doping concentration, not polarity). A metal electrode is placed over the p$^+$ substrate and insulated from it by a layer of silicon dioxide. This electrode forms the gate and controls the current flow through the device. To be fully effective, the gate must have low resistance. It was usually aluminium in the early days but heavily doped polysilicon is now preferred.

The p-type substrate beneath the gate is doped with acceptor impurities, so there are a majority of holes and a minority of electrons uniformly dispersed through it. When the voltage on the gate is zero, no current will flow

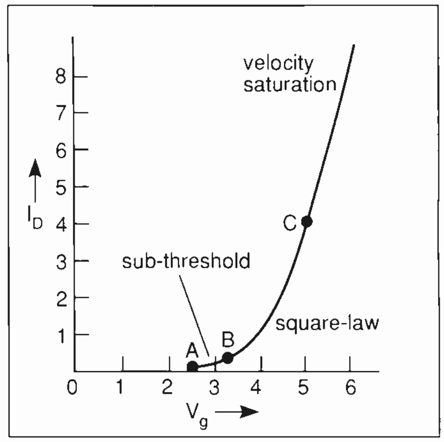


Fig. 2. Gate transfer characteristic

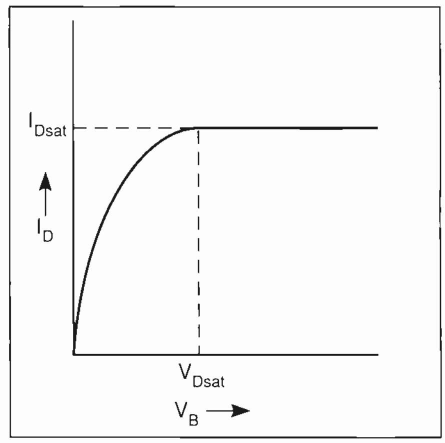


Fig. 3. Drain output characteristic

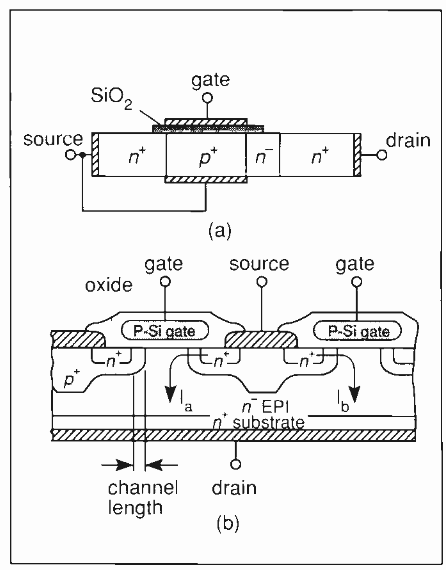


Fig. 4a. N-channel mosfet structure
b. Modern planar vertical double-diffused mosfet

because the device looks like two back-to-back diodes. However when the gate voltage is gradually increased positively, the semiconductor surface goes through several distinct changes which characterise mosfet operation.

Stage 1. The increasing gate voltage first overcomes the "contact potential" existing between the gate electrode and the silicon surface. The metal gate-silicon dioxide-silicon surface system forms a capacitor which has a built-in reverse potential across it, due mainly to the difference between the work functions of the gate metal and of the silicon surface. This built-in potential varies with the substrate doping as well as with the specific metal used for the gate. Small manufacturing imperfections during the oxide formation (eg. Na^+ ions in the washing water) which develop fixed charges in the oxide also add to this voltage.

Stage 2. As the gate voltage increases, the in-built reverse bias potential is gradually overcome and the metal-silicon dioxide-silicon surface system will eventually reach a charge neutral condition. Because the energy bands are all flat in this charge neutral condition, the total voltage needed to reach this state is usually known as the flat-band voltage.

Stage 3. After the flat-band voltage has been passed, any increase in gate voltage will now require a negative charge at the silicon surface to balance the increasingly positive gate charge. Hence electrons in the p-type substrate will drift to the surface, attracted by the positive gate charge, and the holes will be repelled. The surface will thus gradually invert to form an n-type channel in the p-type substrate, which will then allow conduction between the source and drain in either direction. Electron concentration at the surface will increase progressively as the gate-source voltage increases. This in turn will progressively increase the depth and conductivity of the n-type channel, allowing normal drain current to flow.

Before conduction can begin and drain current can flow, the applied gate voltage must reach the level needed to strongly invert the surface (**Table 1**). This voltage level is referred as the threshold voltage and is controlled to lie between 2 and 4V for both n-channel and p-channel power devices. The threshold is positive for n-channel and negative for p-channel devices.

Table 1. Surface changes which take place in an n-channel device as the gate voltage is gradually increased.

Gate voltage	State of semiconductor surface
Zero	Accumulative; positive charges accumulate making the silicon surface positive with respect to the gate, due to the difference in the work functions.
"Flat-band"	Neutral; the gate and silicon surface potentials are now equal.
Positive	Depletion; small negative charge with the surface electron density less than the surface hole density and both less than the acceptor doping.
Positive (more)	Intrinsic; surface electron and hole densities now equal.
Positive (more)	Weak inversion; surface electron density greater than intrinsic but less than acceptor doping. *Sub-threshold state.*
Positive (more)	Onset of strong inversion; surface electron density equal to acceptor doping. *Threshold state definition.*
Positive (more)	Strong inversion; surface electron density much greater than acceptor doping, forming a well-defined n-channel. *Normal conduction state.*

Gate transfer characteristics

If the drain voltage is large enough for the drain current to reach its saturation value I_{Dsat}, then the simplified expression (derived in drain current box) shows the familiar square-law variation of drain current versus gate voltage, ie $I_{Dsat} = 0.5\beta(V_G-V_T)^2$ where

$\beta = \mu_n C_{ox} W/L$.

Differentiating this expression relative to V_G gives the value for transconductance G_{fs} as:

$$G_{fs} = \beta(V_G - V_T)$$

after substituting for (V_G-V_T).

$$G_{fs} = \sqrt{2\beta I_{Dsat}}$$

This typical square-law relationship applies to all mosfets and holds quite accurately when (V_G-V_T) is small. But as the voltage increases, the square-law gradually changes into a linear law, so for high values of (V_G-V_T), $I_{Dsat} \rightarrow k(V_G-V_T)$

The carriers move in the channel under the influence of both a normal field produced by the gate voltage and a tangential field produced by the applied drain voltage. The voltage at the source end of the channel is zero, while at the drain end it equals V_{Dsat} or (V_G-V_T). The tangential field produced by the differential voltage increases the carrier velocity, and it also reduces the carrier mobility as well. When the field strength reaches a value of about 3 x 10^4V/cm, the carrier velocity reaches the limiting or saturation value of about 7 x 10^6cm/s for electrons in silicon. In addition, the normal field produced by the gate further reduces the mobility by increasing the free carrier scattering at the silicon dioxide interface.

The effects of these two fields apply at all values of gate voltage above threshold and the following expression will more accurately model the saturated drain current in practical devices throughout the operating range where θV^{-1} is a mobility modulation factor:

$$I_{Dsat} = \frac{\beta}{2}\frac{(V_G - V_T)^2}{\left[1+\theta(V_G - V_T)\right]} \qquad (1)$$

This factor accounts for both the normal and the tangential field effects and usually lies between 0.03 and 0.5, with 0.1 being typical. θ will also account for small parasitic resistances in series with the source terminal, which reduce β from its theoretical value. (See: Effect of source resistance.)

As the gate voltage increases, the carrier velocity approaches the saturation value vsat and the above expression simplifies to:

$$I_{Dsat}=0.5C_{ox}W.v_{sat}(V_G-V_T)$$

so the drain current in velocity saturation is now directly proportional to (V_G-V_T) and the transconductance approaches a constant value of $G_{fs}=0.5C_{ox}.W.v_{sat}$.

The transconductance thus varies linearly with V_G in the square-law region, but then levels off to a constant value when the carrier velocity saturates. The effect is a characteristic of all short channel mosfets. No other device shows such a linear relationship between input voltage and output current and the relationship can often prove beneficial in linear design. The electric field needed to achieve saturation velocity is easily generated. Effective channel length is in the 1-2µm range and gate voltages just a few volts above threshold are sufficient to achieve the necessary field strength.

For p-channel devices, the limiting velocity for holes in silicon is about 4 x 10^6cm/s and velocity saturation is much more common. Further differences are discussed in a later section.

Determining V_T, β, θ and G_{fs}.

Threshold voltage is the value of V_G at which the drain current becomes meaningful in a

Table 2. Mosfet characteristics at 25°C. (Taken from International Rectifier data)

Part	Die size	Rating	Theoretical gain, β (A/V^2)	Actual gain, β (A/V^2)	Mobility mod^n factor, θ (1/V)
IRF510	Hex 1	100V, 5A	1.8	1.3	0.11
IRF710	Hex 1	400V, 1A	1.8	1.1	0.03
IRF045	Hex 5	60V, 53A	28.0	16.5	0.11
IRF460	Hex 5	500V, 21A	28.0	18.1	0.02

Part	Mutual cond G_{fs} (A/V)	Amp factor μ	Intercept voltage V_q (V)	Threshold voltage V_T (V)	dV_T/dT (mV/°C)
IRF510	$1.2\sqrt{I_D}$	$3000/\sqrt{I_D}$	-2400	3.4	-6.3
IRF710	$1.3\sqrt{I_D}$	$13000/\sqrt{I_D}$	-9800	3.3	-4.8
IRF045	$4.0\sqrt{I_D}$	$5000/\sqrt{I_D}$	-1300	3.5	-6.0
IRF460	$6.0\sqrt{I_D}$	$50000/\sqrt{I_D}$	-8400	3.6	-6.4

Effect of a source resistance R_s

In the practical mosfet, accurately modelled by the circuit in Fig. 6, the actual voltage between the gate and the channel V_{Gch} is given by $V_{Gch} = V_G - I_D R_s$.

But

$$I_D = \frac{\beta}{2}(V_{Gch} - V_T)^2$$

and after substituting and neglecting R_s^2

$$I_D = \frac{\beta}{2}\left\{\frac{(V_G - V_T)^2}{1+\beta R_s(V_G - V_T)}\right\}$$

or

$$I_D = \frac{\beta'}{2}(V_G - V_T)^2$$

where $\beta' < \beta$ is the practical measured value of β. Equating the two expressions gives :

$$\frac{\beta}{\beta'} = 1 + \beta R_s(V_G - V_T)$$

$$\frac{\beta}{\beta'} = 1 + R_s G_{fs}$$

Hence I_D is modelled as

$$I_D = \frac{\beta}{2}\frac{(V_G - V_T)^2}{\{1+\beta R_s(V_G - V_T)\}\{1+\theta(V_G - V_T)\}}$$

$$I_D \approx \frac{\beta}{2}\frac{(V_G - V_T)^2}{\{1+\theta'(V_G - V_T)\}}$$

Thus the source resistance R_s reduces the value of β from its theoretical value to the practical measured value and $\theta' \cong \theta + \beta R_s$, so if this is derived from the published transconductance data, the value determined will automatically include any effects due to the source resistance.

For example, R_s is given by IR as 0.02Ω and its effect is minimal at low current. But for a device like the *IRF044*, G_{fs} = 24A/V at a current of 40A and β'/β=1.48. This is a 32% reduction from the theoretical value of β and the performance of the higher current devices is limited more by the connections than by the semiconductor itself.

Assuming a typical oxide thickness of 1000Å and a relative permittivity of 3.9, then C_{ox}=3.45 x 10^{-8}F/cm^2 and the theoretical value for β is 1.82A/V^2, considerably greater than the 0.87A/V^2 estimated from the $\sqrt{I_D}$ plot. The difference between the theoretical and measured values of β is usually due to the parasitic resistances of the source connections and the source depletion region. Proper choice of the value for θ will usually account for this parasitic resistance in practice (see Effect of source resistance).

The transconductance curve is usually a much better starting point, if one is available, as data from this can give good values for both β and θ for modelling purposes. If we assume that equation (1) accurately models the device, then after differentiation, we have equation (2). Assuming that θ is small allows considerable simplification to this expression giving equation (3). Substituting for (V_G–V_T) gives alternate expression equation (4).

$$G_{fs} = \frac{\beta}{2}\left\{\frac{2(V_G - V_T) + \theta(V_G - V_T)^2}{[1+\theta(V_G - V_T)]^2}\right\} \quad (2)$$

$$G_{fs} = \frac{\beta}{2}\left\{2(V_G - V_T) - 3(V_G - V_T)^2\right\} \quad (3)$$

$$G_{fs} = \sqrt{2\beta I_{Dsat}} - 3\theta I_{Dsat} \quad (4)$$

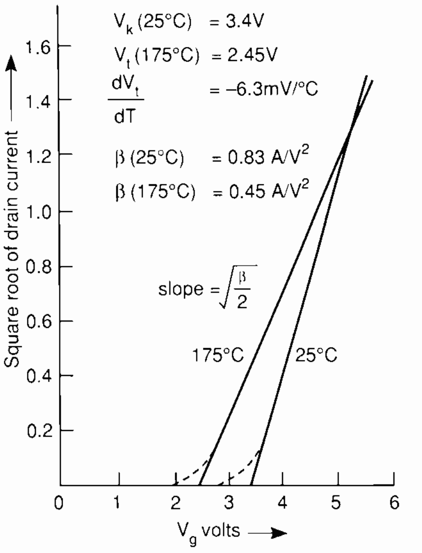


Fig. 5. Plot of $\sqrt{I_{Dsat}}$ versus V_G for the IRF510 showing the variation in transconductance and theshold voltage with temperature.

Note also the square law relationship between gate voltage and drain current: the x-axis is plotted as linear gate volts while the y-axis depicts the square root of drain current. When plotted in this way, the result should be a straight line for perfect devices.

practical sense. V_T can be accurately determined in practice by measuring corresponding values of I_D and V_G up to perhaps 250mA and then plotting a graph of $\sqrt{I_D}$ against V_G. The extrapolated intercept of the straight line portion of the curve onto the V_G axis gives the true value of V_T. The slope of the line is √0.5β, from which the mosfet gain at low current, and the transconductance G_{fs} can be derived. Unfortunately, the value for β obtained in this way does not always give the best results for modelling purposes and it is often much smaller than the theoretical value. As an example, the curves in **Fig. 5** show the $\sqrt{I_{Dsat}}$ versus V_G curve of the *IRF510* at both 25°C and at 175°C. The extrapolated intercept onto the V_G axis gives the true device threshold of 3.4V and the slope of the line yields a gain β of 0.87A/V^2, with a corresponding transconductance of 1.32$\sqrt{I_D}$ A/V, at 25°C.

However for the *IRF510*, the IR data sheet gives the following information:
μ_n=450cm^2/Vs, W=14.2cm and L=1.2 x 10^{-4}cm.

Theoretical behaviour of the drain current with increasing drain-source voltage and gate-source voltage

For low drain voltages, the equations representing mosfet action are derived in a straightforward manner by using a simplified charge control analysis, which assumes that the electric field lines within the gate insulator are perpendicular to the surface of the silicon and that Gauss' law leads to a charge neutral condition. The drain current I_D is related to the total charge in the channel Q_n and the channel transit time T_{tr} by $I_D = -Q_n/T_{tr}$. Because the current in the channel is primarily a drift flow, T_{tr} is just the channel length L divided by the drift velocity v_{drift}. But v_{drift} equals the mobility multiplied by the voltage across the channel per unit length, V_D/L:,

$$T_{tr} = \frac{L^2}{\mu_n V_D}$$

The total channel charge Q_n is given by

$$Q_n = -C_{OX}WL(V_G - V_T)$$

Hence for low drain - source volts

$$I_D = \frac{\mu_n C_{ox} W}{L}(V_G - V_T)V_D$$

$$I_D = \beta(V_G - V_T)V_D$$

where β, theoretical mosfet gain, is defined as

$$\beta = \frac{\mu_n C_{ox} W}{L} = \frac{\mu_n \varepsilon_{ox} W}{T_{ox} L}$$

The expression for I_D represents an effective resistance between drain and source of:

$$R_{DS(on)} = \frac{V_D}{I_D} = \frac{1}{\beta(V_G - V_T)}$$

This defines the mosfet "on resistance" for low drain voltages and is the chief parameter of interest when the device is used as a switch.

If V_D is now increased so that it is no longer negligible compared to V_G, the above simple analysis fails because V_D acts to reduce Q_n. A more comprehensive distributed analysis gives a more accurate though still simplified expression for I_D as:

$$I_D = \beta\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \quad (1.1)$$

Therefore, as V_D is increased from zero with $V_G > V_T$, I_D increases parabolically with V_D until it eventually reaches a maximum at a drain voltage defined as V_{Dsat}. For drain voltages above V_{Dsat}, the drain current maintains a constant value and is said to be in current saturation. Ideally when this occurs, the slope of the drain voltage versus drain current curve should be zero and the effective drain-source resistance should be infinite. But this does not occur in practice due to second order effects, which limit the drain resistance. V_{Dsat} is obtained from (1.1) by differentiating and equating to zero. Differentiating (1.1) gives:

$$\frac{dI_D}{dV_D} = \beta(V_G - V_T - V_D)$$

For a maximum value, dI_D/dV_D = 0 and hence $V_{Dsat} = V_G - V_T$. If this value is now substituted back into Equation (1.1) for V_D, we finally derive the expression for the saturated drain current I_{Dsat} in the square-law region as:

$$I_{Dsat} = \frac{\beta}{2}(V_G - V_T)^2 \quad (1.2)$$

Equation (4) has a maximum when $I_{Dsat} = \beta/18\theta^2$ and provides a quite accurate model for G_{fs}, particularly for those devices which show a maximum in the transconductance curve.

The values for both β and θ can now be derived, by choosing corresponding low and high values for G_{fs} and I_{Dsat} from the transconductance curve and substituting into the above expression. For example, from the curve for the *IRF510*, G_{fs}=1A/V when I_{Dsat}=0.5A and G_{fs}=2A/V when I_{Dsat}=4A. From these values, β=1.34A/V^2 and θ=0.11/V. This value for β is much closer to the theoretical value of 1.82A/V^2 and the expression

$$I_{Dsat} = \frac{0.67(V_G - V_T)^2}{1 + 0.11(V_G - V_T)}$$

accurately models both the V_G versus I_{Dsat} curve and the G_{fs} versus I_{Dsat} curve for the *IRF510*, perhaps better than the International Rectifier data given for *Spice* modelling.

If the transconductance curve is not available, there are two options. Either the designer can derive β from the slope of the $\sqrt{I_{Dsat}}$ plot and assume that θ equals zero; or can assume that θ equals 0.1 and then choose a value for β which gives a best fit to the available data. The value for θ can also be adjusted, depending on the shape of the gate transfer curve. If this follows a square-law over the desired operating range, then θ should be low perhaps 0.03; if there is a tendency to saturation, then a higher value for θ, perhaps 0.3 is more appropriate.

Designers should not attempt to extract the value for β from the $R_{DS(on)}$ saturation characteristics, because it is impossible to know how much of $R_{DS(on)}$ is actually due to the channel. For high voltage devices, most of the on-resistance is in the epitaxial layer; for low voltage devices, an unknown percentage lies in parasitic elements – such as the internal lead resistances – as well as in the epitaxial layer.

The circuit of **Fig. 6** accurately models real devices. R_d represents the resistances of the epitaxial layer and connections, varying from 0.05Ω to 3.5Ω depending on voltage rating, and is of little interest in linear design. R_s is the resistance of the source n$^+$ region plus connections and is about 0.02Ω for *TO-220* packages. This resistance will reduce the value of β and G_{fs} from theoretical (see box: Effect of source resistance) and is automatically taken into account when deriving β and θ from the G_{fs} curve.

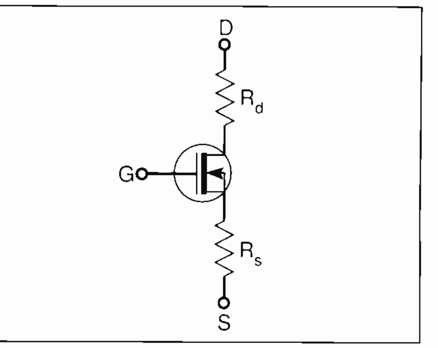


Fig. 6. Circuit showing source resistance.

Variation of the transfer characteristic with temperature

We have already derived the saturated drain current in the square-law region to a first order (see Theoretical behaviour of drain current). Now both V_T and μ_n and hence β vary with temperature and so the variation of I_{Dsat} with temperature can be defined by

$$\frac{\partial I_D}{\partial T} = I_D\left(\frac{1}{\beta}\frac{\partial \beta}{\partial T} - \frac{2}{V_G - V_T}\frac{\partial V_T}{\partial T}\right) \qquad (2.1)$$

partial differentiation of equation (1.2) as: Theoretical analysis indicates that the mobility of both holes and electrons should decrease with absolute temperature in proportion to T^{-n}. As the free carriers move through the silicon under the influence of an applied field, they are scattered by interaction with the crystal lattice and these collisions become more effective as the temperature increases, thereby reducing the carrier mobility. For bulk silicon, n varies between 1.66 and 2.5 and depends quite strongly on the doping level, with the higher values of n applying to the lower doping levels. However, since the carrier mobility in a mosfet channel is only about 35% of that in bulk silicon, temperature variation of the mobility is also less.

Experimental studies have concluded that in the temperature range from –55°C to +125°C, the value of n lies between 1.5 and 2. Higher voltage mosfets have a substrate doping of about 10^{14} atoms/cm^3 and the gain β is proportional to about $T^{-1.9}$, while lower voltage mosfets have a substrate doping of about 5x10^{15} atoms/cm^3 and β is proportional to about $T^{-1.8}$. These figures apply to n-channel devices, with the temperature in °K and they correspond to a change in gain at 25°C of about –0.5%/°C.

For p-channel devices, the temperature variation of β is slightly different; for 200V units, β is proportional to $T^{-1.3}$, while for 50V units, β is proportional to $T^{-1.2}$, giving an average change in gain at 25°C of about –0.6%/°C.

Variation of V_T is much more complex as a large number of factors contribute. It is well to start discussion from the theoretical expression for V_T, which for an n-channel device is:

$$V_T = -\phi_{MS} - \frac{Q_{ss}}{C_{ox}} + \frac{Q_d}{C_{ox}} + 2\phi_F$$

The voltage required to create strong inversion must first be large enough to achieve the flat-band condition (ϕ_{MS} and Q_{ss}/C_{ox} terms), then accommodate the charge in the depletion region (Q_d/C_{ox}) and finally to induce the inverted region ($2\phi_F$). This equation accounts for all the dominant voltage effects in typical mos devices and all the terms except Q_{ss}/C_{ox} depend on the substrate doping. Now both Q_{ss} and ϕ_{MS} can be considered to be independent of temperature and differentiation of the remaining terms in the above equation with temperature yields the following expression,

$$\frac{dV_T}{dT} \approx \frac{1}{T}\left\{\left(\phi_F - \frac{E_{G0}}{2q}\right)\left(\frac{Q_d}{2C_{ox}\phi_F} + 2\right)\right\}$$

after considerable manipulation and simplification:

An analogous expression can be determined for p-channel devices.

For a typical mosfet the following figures apply: p-region body doping with N_a=4x10^{16} atoms/cm^3, Q_{ss}/q=5x10^{10}/cm^2, ϕ_{MS}=0.5V and Q_d/q is adjusted to 8x10^{11}/cm^2. Assuming a pure oxide thickness of 1000Å, then C_{ox}=3.45x10^{-8}F/cm^2 and ϕ_F=0.383V. This gives a value for V_T of 3.36V and a value for dV_T/dT of -5mV/°C. Experimental results for both n-channel and p-channel devices show a threshold voltage temperature variation between –3mV/°C to –8mV/°C, depending on geometry and cell size. The larger cell sizes tend to have the larger values of V_T and larger values of dV_T/dT. The variation is probably due to the adjustment of the depletion charge term Q_d made during fabrication by ionic bombardment to set the threshold voltage.

Variation of threshold voltage with temperature for p-channel devices also falls into the 3mV to 8mV/°C range, and so the variation for the two types is about equal – but of opposite sign.

These theoretical expressions have been included to show that both V_T and dV_T/dT are dependent only on the lattice parameters and on manufacturing geometry. Thus both can be fairly accurately predicted and values for a given device are quite stable over time.

Since the derivatives of n-channel mosfet gain and threshold voltage with temperature are both negative, the change in drain current with temperature will be zero at a specific value of applied gate voltage. This is clearly seen in all published gate transfer characteristics, where the curves at different temperatures cross at a specific value of gate voltage. In the square-law region, this zero

$$V_{G0} = V_T + \frac{2\beta \frac{dV_T}{dT}}{\frac{d\beta}{dT}}$$

TC gate voltage is derived by setting the term in brackets in (2.1) to zero. This yields: An *IRF510* has the following parameters at 25°C: V_T = 3.3V; β = 1.34A/V^2; dV_T/dT = –6mV/°C; dβ/dT = –0.55%/°C (which equals -7.4mA/V^2-°C). Substituting these figures into the above expression gives a value for the zero TC gate voltage of 5.5V, which agrees well with the published curves.

Subthreshold region

When the gate voltage is less than the conventional threshold voltage, the inversion charge can produce only a small drain current – primarily a diffusion current and not a drift current as is normal for I_D above threshold. In this region, I_D varies exponentially with gate voltage in a manner defined by:

$$I_{Dsat} = I_0 \exp k(V_G - V_T)$$

I_0 depends on the size of the mosfet die and is about 0.01A for low current devices and about 0.1A for high current devices. k is reasonably independent of size and a value of 4.6/V fits the available data. Little is known about operation in this region and it is rarely used. But it maybe of practical interest to calculate the variation of I_{Dsat} with temperature for a mosfet operating in the threshold region, with a fixed gate bias voltage near V_T, as this is the effective bias condition in class AB output stages. In the threshold region:

$$\frac{dI_{Dsat}}{dV_G} = kI_0 \exp(V_G - V_T)$$

$$= kI_0 \text{ when } V_G \approx V_T$$

and

$$\frac{dI_{Dsat}}{dT} \approx -5kI_0 \text{mA}/{}^\circ\text{C}$$

because dV_T/dT is approximately –5mV/°C (See: *Variation of transfer with temperature*). The variation of I_{Dsat} at threshold is of the order of –0.23mA/°C for small die sizes and –2.3mA/°C for large die sizes. Bias conditions should therefore be defined at the operating junction temperature and temperature compensation used, if necessary

Properties of silicon, mosfets and insulators at 300°K

Lattice mobility, electron	μ_n		1367cm²/V-s
Lattice mobility, hole	μ_p		478cm²/V-s
Channel mobility, electron			450cm²/V-s
Channel mobility, hole			150cm²/V-s
Permittivity of free space	ε_o		8.854x10^{-8}F/cm
Relative dielectric constant	ε_r	silicon	11.7
		SiO_2	3.9
		Si_3N_4	7.5
Electron charge	θ		1.602x10^{-19}C
Boltzmann's constant	k		1.381x10^{-23}J/°K
			8.617x10^{-5}eV/°K
Energy gap at 0°K	E_{G0}		1.205eV
Temp coefficient of E_{G0}			-2.7x10^{-4}eV/°K
Intrinsic concentration	n_i		1.45x1010 /cm³
Thermal voltage	kT/q		0.02586V
Typical fixed positive charge density	Q_{ss}/q		5x10^{10} /cm²
Nominal thickness of SiO_2	T_{ox}		1000Å

Doping
Donor, or n-type impurities: antimony, arsenic, phosphorus
Acceptor, or p-type impurities: boron, gallium, indium
Typical doping concentrations vary from 10^{14} to 10^{16} atoms/cm³.

Useful dimensions
1 micron = 10^{-6}m
1Å (Angstrom) = 10^{-10}m

NEXT ISSUE: Drain transfer characteristics; Determination of the drain output conductance; Amplification factor; Differences between n-channel and p-channel; High frequency performance.

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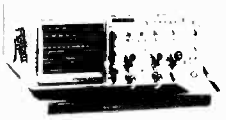

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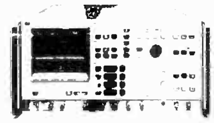

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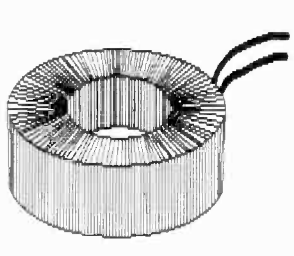

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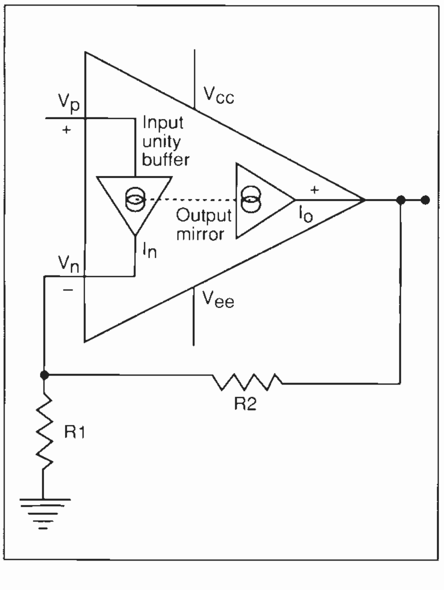
The current alternative to operational amplifiers

Current mode amplifiers maintain their performance over a much wider frequency span than conventional operational amplifier alternatives. Although the application circuits look similar, the mechanisms which produce the performance are very different.

By Frank Ogden.

Compare the pinout of a typical current mode amplifier with a standard pattern op-amp and things look very similar. Pins 2 and 3 are marked as inverting/non-inverting, pin 6 delivers the output while pins 4 and 7 hook up to the power supply. A typical application circuit will use the standard virtual earth resistive feedback connection. Yet, although it seems unlikely, a current mode amplifier shows little degradation of bandwidth with set gain.



Compare this with the typical 6dB/octave degradation in open loop gain with frequency of a standard op-amp. A 741 for instance will begin to roll off in gain from about 5Hz. By contrast the HA-5020 current mode amplifier from Harris Semiconductor enjoys a typical full power bandwidth of 12MHz and performs usefully up to 50MHz. The output will slew around 800V/µs. It exhibits the sort of gain and phase flatness which broadcast engineers look for when designing video facilities.

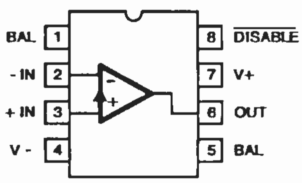
Fig. 1. Conventional and current mode amplifiers differ in one particularly fundamental respect: where a conventional op-amp has two true input terminals, the current mode device possesses only one. The non-inverting (V_p) terminal, the input to an internal current follower, exhibits an input impedance in the order of 20MΩ which has its output connected to the 'inverting' terminal, V_n, a very low impedance node. If V_n is connected to ground via a resistor, a current will flow dependent on the value of the resistance and the voltage present at the V_p terminal. A multiplying current mirror reflects this current flowing into or out from the V_n terminal at the output of the device. If the multiplying factor is very large, the effective system gain will be determined almost entirely by the current flowing in the network connected to the inverting terminal. Thus for an ideal current mode amplifier used in the circuit shown above, the voltage gain from V_p to the output terminal is simply $(R_2 + R_1)/R_1$

A conventional op-amp relies on possessing enough internal voltage gain such that its output voltage will reduce the voltage difference between its inverting and non-inverting inputs close to zero. Thus large signals produce large internal voltage swings within the device, usually at high impedance nodes. Collector-base capacitance in voltage amplifying devices inevitably leads to frequency dependent feedback; the equivalent shunt capacitance is equal to the collector-base capacitance multiplied by the gain of the stage. Thus what might have a very small value actually presents a capacitive drag of many times this value. If the op-amp possesses a number of gain stages, individual Miller (for that is the name of the multiplying effect) capacitances produce enough collective phase shift to make the device unstable at low values of the closed loop gain (where the level of feedback is high). "Internally compensated" is actually a euphemism for adding a comparatively large internal capacitor to lump all the phase shift into a single, dominant pole. But its effect on performance is a disaster.

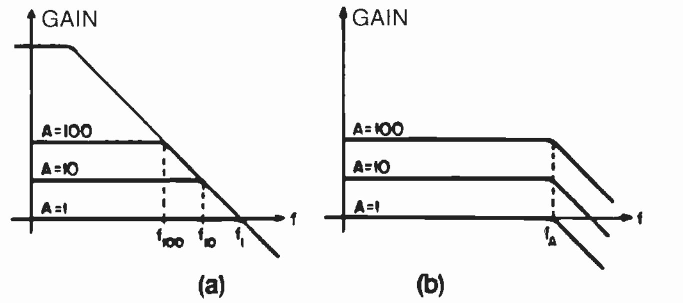
Conventional op-amps are just as bad at handling step changes in voltage: all this internal Miller capacitance needs to be charged up – or down – before the device output can reg-

HA-5020 KEY SPECIFICATIONS

Unity gain bandwidth	100MHz
Full power bandwidth	12MHz
Slew rate	800V/µs
Output current	±30mA
Output voltage swing	±12V
Open loop gain	70dB‖400Ω R_L
Drive capability	3.5V‖75Ω
Differential gain	<0.02%
Differential phase	<0.03%
Rise/fall time	5ns
Input noise voltage	4.5nV/√Hz
Supply current	10mA
Supply voltage	±5V to ±15V



HA-5020 pinout



Conventional op-amps suffer a linear reduction in open loop gain vs frequency (a). CM amplifers by contrast exhibit very low internal voltage swings which dramatically reduces the fall in open loop gain with frequency (b).

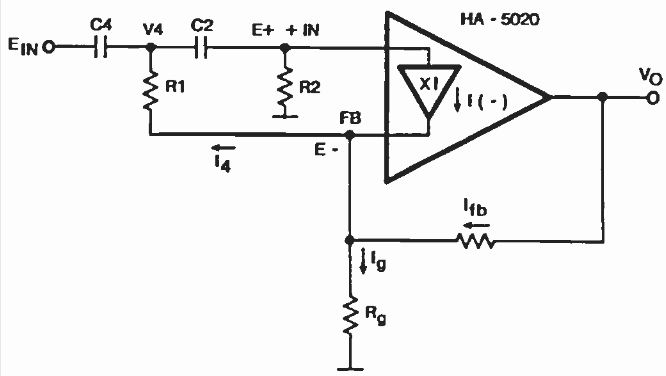


Fig. 2. The HA-5020 connected as a high pass active filter. This circuit will function effectively up to 12MHz with appropriate passive component values.

ister the change. The slew rate is set by the maximum current available from the internal voltage amplifiers in charging or discharging the internal Miller capacitance.

The current alternative

A current mode amplifier comprises two sections: a non-inverting unity gain input buffer with its high impedance input connected as the non-inverting input while the buffer output, a complementary emitter follower, brought out as the "inverting" terminal. The second section comprises an output complementary current mirror, the output value and polarity of which depends on the current flowing into or out from the "inverting" amplifier terminal sensed by a current mirror in the unity gain input buffer.

None of this looks particularly promising at first glance for commonsense seems to suggest that the output of a low impedance buffer (marked input unity buffer in **Fig. 1**) could not readily serve as an inverting input connection to a precision amplifier.

Neglecting the maths for a moment, look at the amplifier function this way. Apply a positive input voltage to the high impedance (20MΩ) input terminal V_p relative to ground. This will cause the same output voltage – give or take a few microvolts – to be delivered to the inverting terminal V_n but at an impedance of just a few ohms. Thus the full input voltage is developed across R_l causing a current to flow in the buffer proportional to the input voltage and inversely proportional to the value of R_l, i.e. Ohm's Law.

The input unity buffer measures the current flowing into or out from the terminal V_n through a complementary current mirror integrated into the buffer circuit. The mirror current in turn drives an independent output current mirror with a current transfer ratio of several thousand. Effectively this means that a current of microamps flowing into or out of the inverting terminal V_n produces a current of milliamps (I_o) at the output terminal of the amplifier.

By coupling this output current back to the inverting input terminal via R_2, two things happen. Firstly, an output voltage is developed proportional to the value of $I_o \times R_2$. Secondly, the current flowing in R_2 acts in a sense to reduce the current flowing into or out from the unity gain buffer. Thus, provided that the current transfer ratio between the input and output mirrors is very large, the overall system voltage gain approximates to $(R_2 + R_l)/R_l$.

This type of circuit configuration derives its gain/bandwidth independence through a complete absence of internal signal voltage nodes. Even the largest signal swings are restricted to internal voltage changes in the order of 100mV or so. Thus the Miller effect cannot apply to current mode amplifiers. Compare this situation to the large voltage swing inside a conventional op-amp. The only place in a C-M amplifier where large swings occur is the output node; first order bandwidth is determined by the time constant formed between the device output capacitance and the feedback resistor, R_2.

Second order effects do result in reduced bandwidth with increasing open loop gain but these are small when compared with conventional devices. For instance a C-M amplifier set up for unity gain might deliver a –3dB turnover at 100MHz, a figure which falls to 65MHz when the system gain is increased to 10. By contrast, a conventional 100MHz op-amp would suffer a bandwidth reduction to 10MHz as its closed loop gain was increased to 10.

The HA-5020

This device uses current mode operation and was designed for video applications at system gains of between 1 and 10, for instance in video mixers and multiplexers. For instance, it will drive up to two 75Ω lines at video levels with very low distortion and an accompanying gain flatness of 0.1dB. Other applications include high frequency active filters and IF amplifiers. The general form follows the organisation of Fig. 1. Typical values for R_2 would be around 1kΩ. Gain variation would normally be achieved by choosing an appropriate value for R_l.

The device also includes a disable function which significantly reduces supply current and forces the output to a true high impedance state. This allows multiple amplifiers to be wire OR'd as amplifying video multiplexers.

The availability of a high impedance buffer at the font end of a C-M amplifiers in general and the HA-5020 specifically allows the easy construction of Sallen & Key 12dB/octave active filters. The general form is shown in **Fig. 2**. ■

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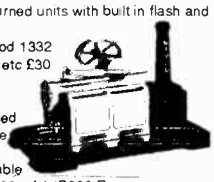

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UPDATING the choice for handling data in the lab

How does the updated LabWindows meet current data acquisition demands? Allen Brown measures the improvements.

System requirements
386/486 PC
4Mbyte extended ram
Mouse coprocessor (for 386 PC)
VGA graphics

Supplier details
LabWindows 2.1 £695; Advanced analysis £1495, National Instruments UK Ltd, 21 Kingfisher Court, Hambridge Road, Newbury, Berkshire RG14 5SJ. Tel: 0635 523545.

National Instruments updated *LabWindows* data acquisition and processing package is not so much an improvement but an extension to the previous version, and a much broader range of options is now on offer.

The basic product is essentially a software development environment, producing code for processing data derived from instruments via the *IEEE488*, the *RS232* or PC expansion cards.

Two programming languages are available, *QuickBasic* and *C* – though the version of *C* does not entirely conform to the ansi standard and so programs ported into *LabWindows* may require some modification to be accepted by its *C* compiler. For example, it does not recognise float x ; .

Powerful library

It is *Labwindows*' impressive library containing a large variety of subroutines for performing data acquisition, data processing and display that makes the package so attractive.When creating code in *LabWindows* the designer in, effect, assembles a list of library subroutines to perform the required task. Appearance is very similar to the standard Microsoft language development packages with mouse driven drop-down menus and easy access to help files and compiler facilities. Code produced by the designer may have the constructs of *C* (or *QuickBasic*) but all functional i/o operations and analysis consists of subroutines drawn from the extensive library.

Prompting the subroutine to do what is needed is achieved by entering a series of dialogue boxes which present the user with the various options and are clicked with the mouse.

When complete, *LabWindows* generates the appropriate code and this is attached to the user's own code.

For example the code shown in the top half of **Fig. 1** generates a sine wave with added noise (pseudo random). Having created the data, it can be displayed graphically by entering the appropriate dialogue boxes from the drop down menu. By responding to the various options the original code is duly amended (bottom half Fig. 1).

Evoking the run option from the appropriate drop-down menu makes the source program compile and execute (provided there are no errors) with the resulting graphical display (**Fig. 2**). Users can single step through the source code in one window while watching the progress of variables in another.

Programming in the *LabWindows* environment is not too different from object oriented design where the library subroutines may be referred to as pre-designed and tested objects. Programming is therefore performed at quite a high level, allowing the user to concentrate on design aspects of the code and avoid low level problems such as interfacing, storage and display.

Part of the *LabWindows* library is an extensive set of device drivers for commonly used test instruments with the *IEEE488* interface. It is even possible to reproduce with relative ease the front panel of an instrument (**Fig. 3**).

Exploiting the *386* PC

One of the main drawbacks of early versions of *LabWindows* was a constraint on memory, where the package was expected to work entirely within the normal dos 640K. The problem was that though the source language is *C* (or *QuickBasic*), the technique of attaching routines from the run-time libraries renders *LabWindows* coding as high level programming. Like all high level languages, large executable programs could be produced. But in the new version the 640K boundary has been removed by employing a dos/16M

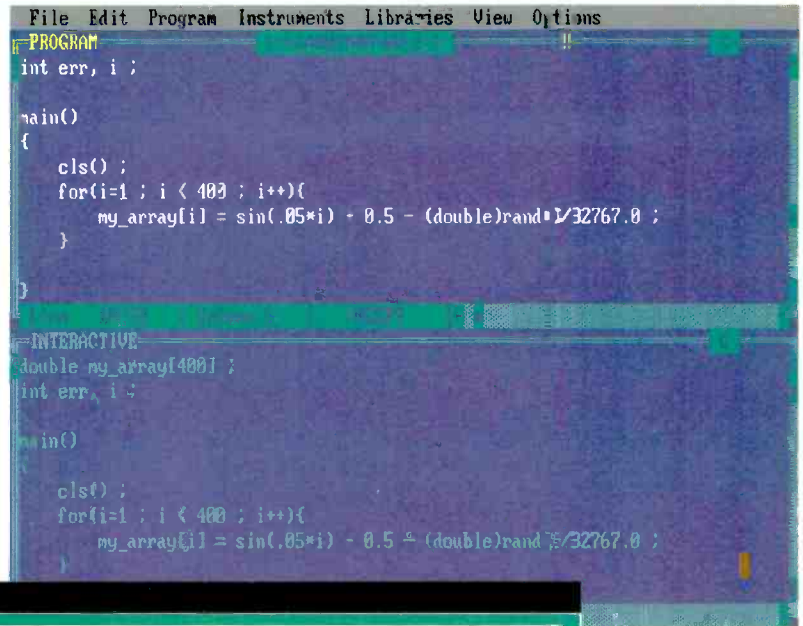


Fig. 1. LabWindows offers a standard PC software development environment.

extender and the virtual memory manager (VMM) from Rational Systems. The dos/16M allows programs greater than 640K to be run on a PC with extended memory. When there is inadequate extended memory the VMM comes into play by exchanging segments of program between ram and hard disc. As a result the package now fully utilises the advanced features of the *386* and *486* PCs – it can run on *286* PCs but the operational speed makes this combination quite unattractive.

For computational intensive needs National Instruments also supplies an advanced analysis package containing routines specifically for the *80387* maths coprocessor (though this is generally expected these days with high performance PCs based on *80486* CPUs).

A few years ago no-one would complain about waiting a minute or two for a 2048-point FFT; today we expect this to take only a couple of seconds at most. But since intensive computation is now a general requirement for data processing, the advanced analysis option really should be a standard part of the *LabWindows* package.

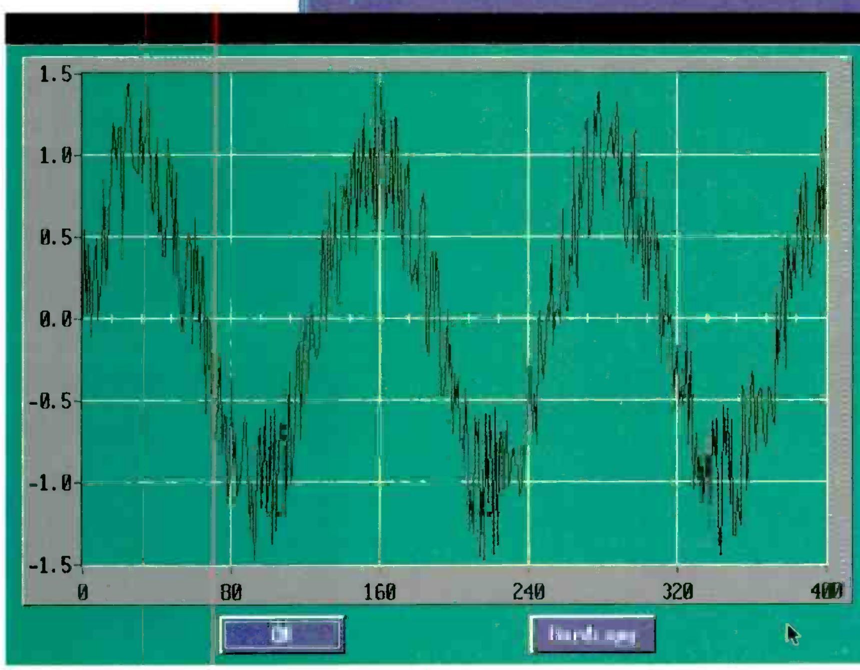


Fig. 2. Graphics display exploits the full resolution of the VGA standard.

Added power

LabWindows has been designed primarily as a package for development of data acquisition from laboratory instrumentation. But to complement this, the product is supplied with an extended library of device drivers for a wide range of well known instruments which have the *IEEE488* interface. HP instruments feature strongly among the library entries. Access to the facilities offered by the library instruments can be gained with relative ease: users need not rely on low level programming to configure remote instruments as this is achieved by options in the device drivers.

Since VGA has become a universal standard in PCs the need for numerous fonts often arises. *LabWindows* has a variety of fonts which can be used to great effect to enhance the quality of the graphics displays and the full resolution offered by the VGA standard has been used to create quite pleasing display effects. Of course these effects can easily be evoked by accessing the library subroutines.

For development of a data acquisition systems *LabWindows* must rate among one of the most attractive products on the market – not only for its ease of use but also for its extensive range of device drivers for instruments and expansion cards out in its library.

So what *LabWindows* does, it does well and there is no doubt that it is a sensibly-designed, quality product. But with the trend towards real-time processing, it might be more appropriate for the processing to be off-loaded to an auxiliary expansion card hosting a high performance DSP processor. This feature is already available with Display-XL and future versions of LabWindows should really move in this direction. One final point is that with the emergence of *Numerical C*, National Instruments will have to look very carefully at their particular version of *C*. ■

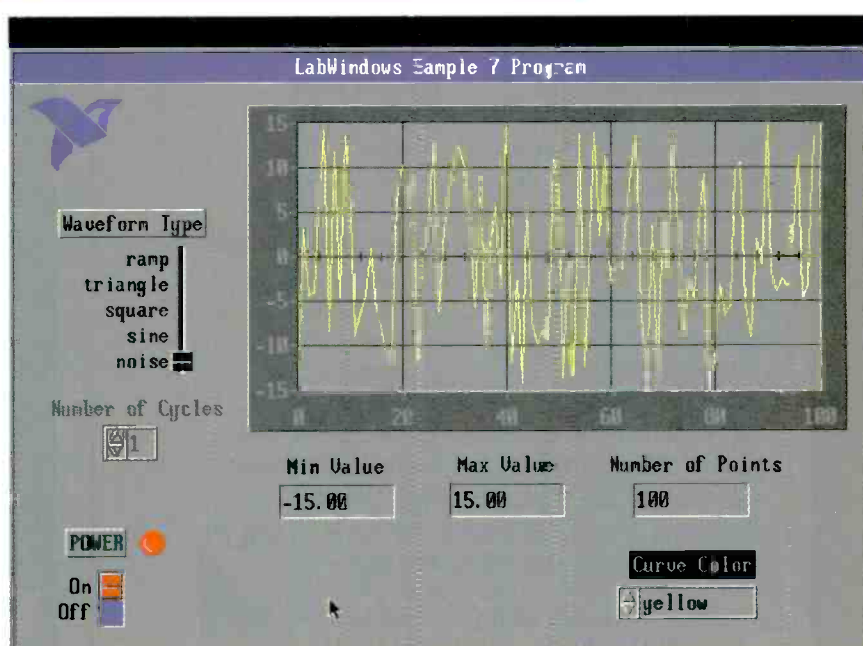


Fig. 3. A front panel instrument set-up for remote access purposes can be set up with ease.

Don't say goodbye to the design engineer – yet

EE Designer III is an electronic design engineering system – according to the literature. John Anderson puts those claims to the test.

EE Designer claims to be an integrated electronic design engineering system. So is the electronic designer redundant? Not yet, but the package is certainly comprehensive, blending tasks as diverse as layout design and logic simulation. Functionality of the product is good too, though it does have a less than ideal user interface and the sound system is guaranteed to turn the user into the least popular person in the design office.

One undoubted plus is that the software is available on rental at 10% of the purchase price per month enabling the unsure to use the it and understand its capabilities at leisure, with a minimal outlay.

Origins of *EE Designer* itself are complex. Author Visionics is based in Singapore and Sweden, and sales literature is clearly targeted at an American market. But Betronex has been its agent in the UK for many years, so support should be good.

Visionics has built its system around front annotation and back annotation. Front annotation is where definitions of the system components occur at the schematic capture stage. But back annotation is usually offered by only the better PCB design products and allows decisions such as gate allocations made on the PCB to be translated back to the schematic. An amazing claim by the authors is that *EE Designer* can be used to back annotate a complete design from PCB (though this was not checked during the review).

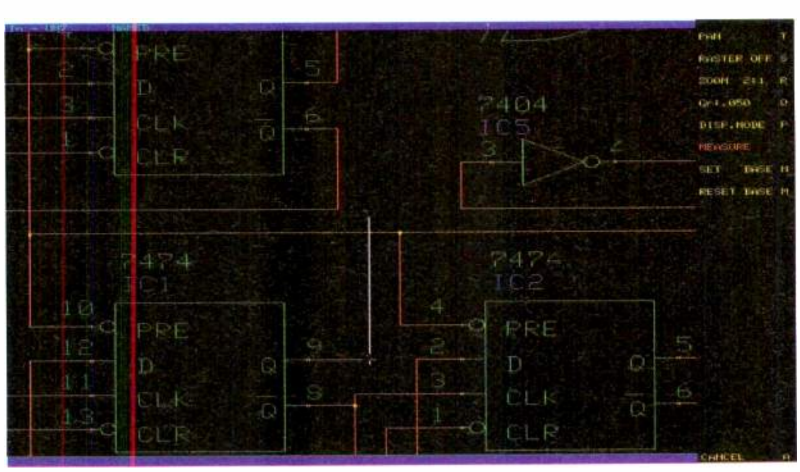
On execution, the package presents the user with a textual selection menu, traversed by the mouse-controlled highlight, with the menu controlling execution of a number of editor environments and processing programs.

Connection between the various parts of the program is through the databases, so the schematic capture database is used to produce the bill of materials, netlist and circuit simulation data, and the PCB database is used to produce the final artwork and thermal analysis with inputs from a netlist.

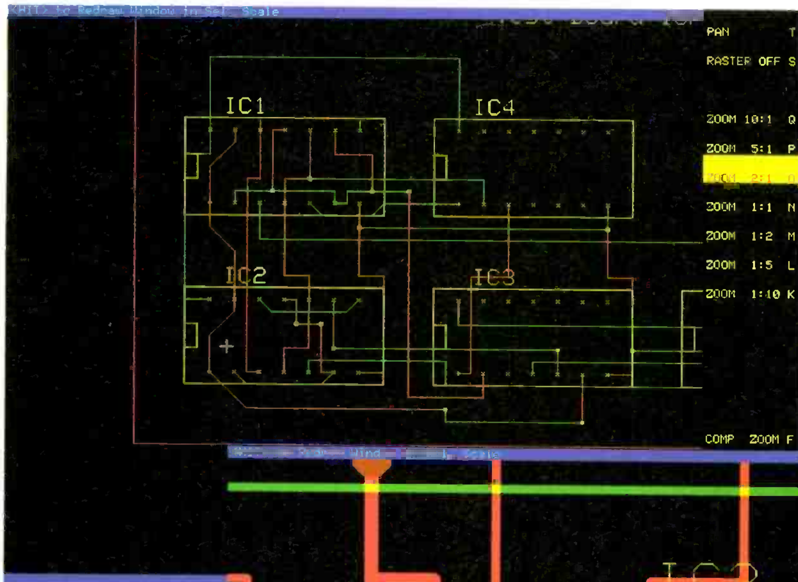
Main menu contains a large number of options

SYSTEM REQUIREMENTS

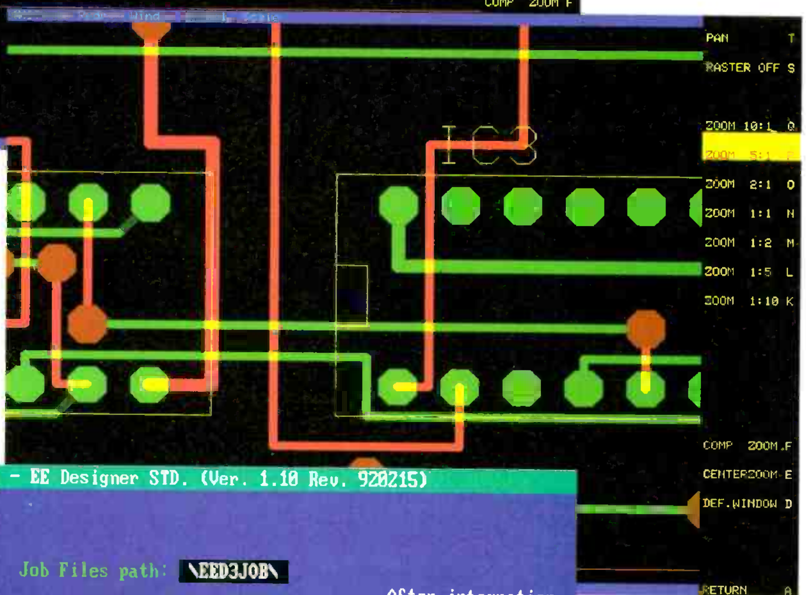
- XT or AT with 640K
- Optional use of expanded memory recommended (Lim 3.2 or above)
- Hard disc (essential) with at least 8Mbytes free
- Colour display and adapter (CGA through VGA and others)
- Parallel port for dongle
- Serial port for asynchronous communications
- Mouse
- A variety of printers and plotters are supported, including laser printers and Gerber photoplot.



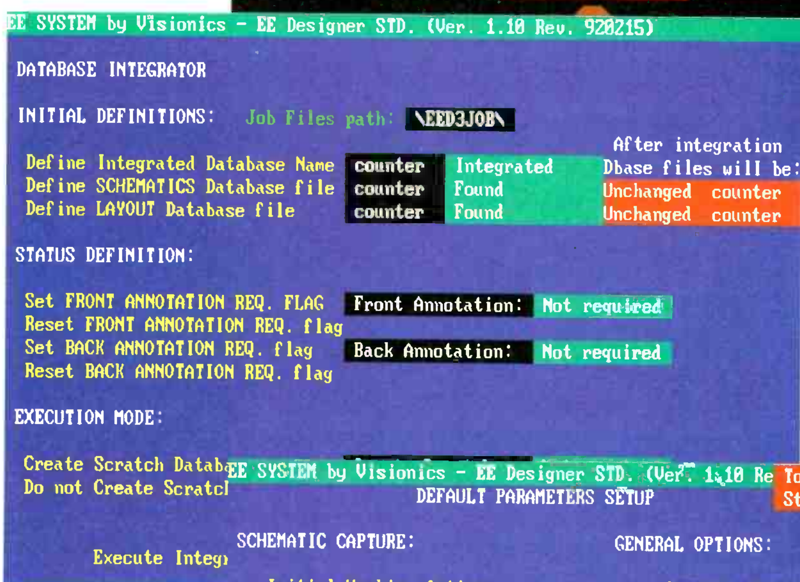
EE Designer's schematic editor: the white trace is in the process of being moved.



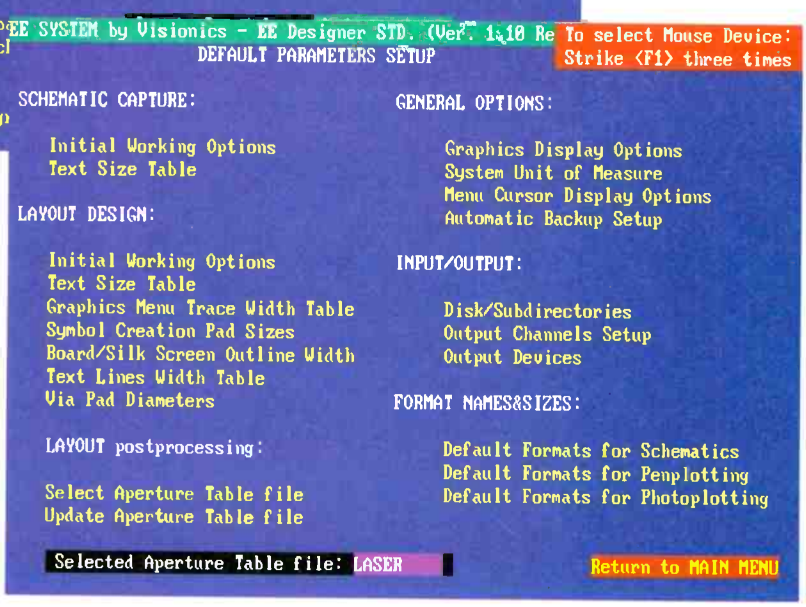
High speed option for PCB, with tracks replaced by single lines, allows faster redraw.



EE Designer's full PCB representation



All files generated in the design process are linked through the database integrator



A bewildering list of default parameters

All the files generated in the design process are linked together though the database integrator system. Thus when moving from schematic to PCB or back there is no question about the name of the file - this is all defined by the integrated system.

A competent graphics editor, with a keyword menu on the right hand side of the display, is used for all the various schematic, PCB and component editing. Operations are carried out through a hierarchy of such menus – which can make some operations a bit slow. But this is mitigated by a series of single keystroke short-cuts; for example traversing three menus can be achieved by pressing just three keys. Unfortunately, the chosen key letters appear to have little if any relevance to the function selected (r is the short cut for zoom), so it is something of an uphill struggle to learn the short cuts, though prompts are available on each menu.

A crucial measure of graphic editors for PCBs is how fast they can redraw. I tested the software on a 33MHz 486 machine but found that even a small PCB of five ICs was taking about a second to redraw with the full representation of the tracks – though when switched to single line representation the redraw was acceptably fast.

Throughout operation, sound is brought into play – and it is terrible! A beep might be expected to indicate an error, but the package insists on bleeping and burbling during normal operation and I could not find any way to turn it off.

Design rule check

EE Designer's comprehensive design rule check system operates either manually or automatically. In manual mode, the user selects two items, and the program displays the clearance; no remedial action is taken.

The automatic design rule checker allows checking of the whole board, or indeed just a window of the board. Errors spotted during the design rule check are written on the PCB layout directly.

Distances defining the minimum clearances are defined by a separate menu, allowing definition of track to track

SPECIFICATIONS

Schematic:
Sheet size to 64in x 64in
Up to 100 sheets
Up to 1500 components
Real time dragging of parts
Automatic bus increment
PCB layout:
32in x 32in maximum board size on 0.001in grid.
32 user definable track widths
64 user definable pad sizes
curved track routing and fills
Automatic via insertion
12 routing layers
Track repeat
Electrical conductivity checking

(referred to in the US as trace to trace), track to pad, pad to pad and via clearances.

Unusual features

Two unusual features are the package's communication and simulation. Communication is to some extent over the top! The idea is that files generated by *EE Designer* can be sent via a modem to specialist photoplot houses. But re-inventing the modem communications wheel is only helpful if you do not already have a proper modem and file transfer software.

For simulation, the package can be supplied with mixed mode simulation, advanced shove and sweep autorouter and thermal analysis, with interfaces to *PSpice* and *Autocad* via DXF – though my review copy had none of these features.

Fighting the system

Lack of a proper library data base and manager is a real weakness and using the dos filing system is a very inefficient way to store this type of data.

But overall, all the functionality is there – if you are prepared to fight the system. Unfortunately, the signposts in the manual needed to unravel operation are chaotic making learning more of a struggle than it should be, and productivity in the early stages will remain low. The short-cut single key strokes and excellent autorouter should eventually reap benefits. But despite claims in the sales literature, the package can hardly be described as friendly, and there is no help let alone a modern context sensitive scheme.

There is integration between component parts, and the package's ability to integrate mixed mode simulation as well as thermal predictions distinguishes it from its competitors. None the less I tested only the PCB schematic capture and layout facilities and found them no better than lower priced products and typically more tedious to use.

INSTALLATION AND DOCUMENTATION

Installation is something of a drawn out affair with the install routine unpacking files and creating directories. Component libraries are stored on hard disc as thousands of little files creating a severe problem. Each file comprises only a few hundred bytes, but on hard disc this is rounded up to the nearest cluster of say 2K. Result is that *EE Designer* eats disc space in a big way, with 3.5Mbytes for the programs and a further 7Mbytes for three (of the ten or so) libraries that I loaded. Be warned, during the installation process, *EE Designer* fiddles with your CONFIG.SYS file.

The software comes with five spiral bound manuals and a parallel port dongle. The Libraries manual is a 200 page list of the components supported - very impressive. A supplemental manual describes the changes of the various releases and details the database formats and primitives.

Of all the manuals, only the Users Guide has an index, and bearing in mind the complexity of the system, this is not helpful for the new user.

One small example PCB is supplied, and this did not really test the system, though all aspects of the example were described in the tutorial manual.

Absence of a context-sensitive help system makes learning a slow task.

SUPPLIER DETAILS

EE Designer Standard (as reviewed) £995. From Betronex Ltd, 1 Wells Yard, High Street, Ware SG12 9AS. Tel: 0920 469131

Top of the range is *EE Designer Elite* at £3990, offering mixed mode simulation, shove and sweep autorouter, thermal analysis interface to *PSpice*

Is it a fully integrated electronic design system? Hardly design, but reasonably competent for PCB layout, with the promise of upgrades for logic and analogue simulation using the same captured data. ■

SMALL SELECTION ONLY LISTED – EXPORT TRADE AND QUANTITY DISCOUNTS – RING US FOR YOUR REQUIREMENTS WHICH MAY BE IN STOCK

Tektronix 475 – 200Mc/s oscilloscopes – tested from £400 less attachments to £500 C/W manual probes.
Marconi TF2008 – AM-FM signal generator – Also sweeper – 10Kc/s – 510Mc/s – from £350 tested to £500 as new with manual – probe kit in wooden carrying box.
HP DC Current source type 6177C – £200.
HP Frequency comb generator type 8406A – £400.
HP Sampling Voltmeter (Broadband) type 3406A – £200.
HP Vector Voltmeter type 8405A – £400 to £600.
HP Synthesiser/signal generator type 8672A – 2 to 18GHzS old or new colour £4000.
HP Oscillographic recorder type 7404A – 4 track – £350.
HP Plotter type 9872B – 4 pen – £300.
HP Sweep Oscillators type 8690 A & B + plug-ins from 10Mc/s to 18GHz also 18-40GHz. P.O.R.
HP Signal Generators type 612 – 614 – 618 – 620 – 628 – frequency from 450Mc/s to 21GHz.
HP Network Analyser type 8407A + 8412A + 8601A – 100Kc/s – 110Mc/s – £500–£1000.
HP 432A–435A or B Power Meters + Powerheads – 10Mc/s-40GHz – £200–£650.
HP Down Converter type 11710B – .01-11Mc/s – £450.
HP Pulse Modulator type 11720A – 2-18GHz – £1000.
HP Modulator type 8403A – £100-£200.
HP Pin Modulators for above-many different frequencies – £150.
HP Counter type 5342A – 18GHz – LED readout – £1500.
HP Signal Generator type 8640B – Opt001 + 003 – .5-512Mc/s AM/FM – £1200.
HP Spectrum Display type 3720A £200 – HP Correalator type 3721A £150.
HP 37555 + 3756A – 90Mc/s Switch – £500.
HP Amplifier type 8447A – .1-400Mc/s £400 – HP8447F .1-1300Mc/s £800.
HP Frequency Counter type 5340A – 18GHz £1000 – rear output £800.
HP 8410 – A – B – C Network Analyser 110Mc/s to 12GHz or 18GHz – plus most other units and displays used in this set-up – 8411A – 8412 – 8413 – 8414 – 8418 – 8740 – 8741 – 8742 – 8743 – 8746 – 8650. From £1000.
HP Signal Generator type 8660C – .1-2600Mc/s. AM/FM – £3000. 1300Mc/s £2000.
HP Signal Generator type 8656A – 0.1-990Mc/s. AM/FM – £2250.
HP 3730B Mainframe £200.
HP 8699B Sweep PI – 0.1-4GHz £750 – HP8690B Mainframe £250.
HP Digital Voltmeter type 3456A – £900.
Racal/Dana digital multimeter type 5001 – £250.
Racal/Dana Interface type 9932 – £150.
Racal/Dana GPIB Interface type 9934A – £100.
Racal/Dana 9301A-9303 RF Millivoltmeter – 1.5-2GHz – £350-£750.
Racal/Dana Counters 9915M – 9916 – 9917 – 9921 – £150 to £450. Fitted FX standards.
Racal/Dana Modulation Meter type 9009 – 8Mc/s – 1.5GHz – £250.
Racal – SG Brown Comprehensive Headset Tester (with artificial head) Z1A200/1 – £450.
EIN 310L. RF Power Amp – 250KHz – 110Mc/s – 50Dbs – £250.
Marconi AF Power Meter type 893B – £300.
Marconi Bridge type TF2700 – £150.
Marconi/Saunders Signal Sources type – 6058B – 6070A – 6055B – 6059A – 6057B – 6056 – P.O.R. 400Mc/s to 18GHz.
Marconi TF1245 Circuit magnification meter + 1246 & 1247 Oscillators – £100-£300.
Marconi microwave 6600A sweep osc., mainframe with 6650 PI – 18-26.5GHz or 6651 PI – 26.5-40GHz – £1000 or PI only £600.
Marconi distortion meter type TF2331 – £150, TF2331A – £200.
Thurlby convertor 19 – GP – IEEE – 488 – £150.
Philips logic multimeter type PM2544 – £100.
Microwave Systems MOS/3600 Microwave frequency stabilizer – 1 to 18GHzs & 18 to 40GHzs – £1000.
Bradley Oscilloscope calibrator type 156 – £150.
Tektronix Plug-ins 7A13 – 7A14 – 7A18 – 7A24 – 7A26 – 7A11 – 7M11 – 7S11 – 7D10 – 7S12 – S1 – S2 – S6 – S52 – PG506 – SC504 – SG502 – SG503 – SG504 – DC503 – DC508 – DD501 – WR501 – DM501A – FG501A – TG501 – PG502 – DC505A – FG504 – P.O.R.
Ailtech Stoddart receiver type 17/27A – .01-32Mc/s – £2500.
Ailtech Stoddart receiver type 37/57 – 30-1000Mc/s – £2500.
Ailtech Stoddart receiver type NM65T – 1 to 10GHz – £1500.
Gould J3B Test oscillator + manual – £200.
Image Intensifiers – ex MOD – tripod fitting for long range night viewing – as new – £1500-£2000.
Don 10 Telephone Cable – ½ mile canvas containers or wooden drum – new – Mk2-3 or 4.
Infra-red Binoculars in fibre-glass carrying case – tested – £100. Infra-red AFV sights £100.
ACL Field intensity meter receiver type SR – 209 – 6. Plugs-ins from 5Mc/s to 4GHz – P.O.R.
Systron Donner Counter Model 6057 – 18GHz – £800.
Tektronix 491 spectrum analyser – 1.5GHz-40GHz – as new – £1200 or 10Mc/s 40GHz.
Tektronix Mainframes – 7603 – 7623A – 7633 – 7704A – 7844 – 7904 – TM501 – TM503 – TM506 – 7904 – 7834 – 7104.
Knott Polyskanner WM1001 + WM5001 + WM3002 + WM4001 – £500.
Ailtech 136 Precision test RX + 13505 head 2 – 4GHz – £350.
SE Lab Eight Four – FM 4 Channel recorder – £200.
Ailtech 757 Spectrum Analyser – 001 22GHz – Digital Storage + Readout – £5000.
Dranetz 606 Power line disturbance analyzer – £250.
Precision Anerold barometers– 900-1050Mb – mechanical digit readout with electronic indicator – battery powered. Housed in polished wood carrying box – tested – £100-£200-£250. 1, 2 or 3.
B & K Sound Level Meter type 2206– small – lightweight – precision – ½" microphone – in foam protected filled brief type carrying case with windshield & battery + books + pistol grip handle – tested – £170. Carr: £8. – B & K 2206 Meter + Mike + Book – less carrying case etc. – £145. Carr: £8. **DISCOUNT ON QUANTITY**.
HP 141T Spectrum Analysers. All new colours supplied with instruction manuals.
HP 141T-8552B – 8556A – 20Hz to 300kHz. £2000.
HP 141T-8552B – 8553B – 1kHz to 110Mc/s. £1750.
HP 141T-8552B – 8554B – 100kHz to 1250Mc/s. £2250.
HP 141T-8552B – 8555A – 10Mc/s to 18GHz. £3000.
HP 141T – old colour mainframe + 8552A; 8553B – 1kHz to 110Mc/s. Instruction manuals – £1250 or 8552B £1500.
HP 3580A LF-spectrum analyser – 5kHz to 50kHz – LED readout – digital storage – £1600 with instruction manual – internal rechargeable battery.
Spectrascope 11 SD335 (S.A.) realtime LF analyser – 20Hz to 50kHz – LED readout with manual – £500 tested.
Tektronix 7D20 plug-in 2-channel programmable digitizer – 70 Mc/s – for 7000 mainframes – £500 – manual – £50.
Datron 1065 Auto Cal digital multimeter with instruction manual – £500.
Racal MA 259 FX standard. Output 100kc/s–1Mc/s–5Mc/s – internal NiCad battery – £150.
Tektronix TR503 tracking generator – 10Mc/s to 1800Mc/s + manual – £1500.
Aerial array on metal plate 9"×9" containing 4 aerials plus Narda detector – .100–11GHz. Using N type and SMA plugs & sockets – **ex eqpt** – £100.
EIP 451 microwave pulse counter 18GHz – £1500.
Marconi RF Power Amplifier TF2175 – 1.5Mc/s to 520Mc/s with book – £100.
HP 8614A Signal Generator 800Mc/s to 2.4GHz – old colour – £300. New colour – £600.
HP 8616A Signal Generator 1.8GHz to 4.5GHz – old colour – £200. New colour – £400.
HP 8620A or 8620C Sweep Generators – £400 or £900.
Marconi 6155A Signal Source – 1 to 2 GHz – LED readout – £600.
Schlumberger 2741 Programmable Microwave Counter – 10Hz to 7.1GHz – £750.
Schlumberger 2720 Programmable Universal Counter 0 to 1250Mc/s – £600.
HP 37203A HP-IB Extender – £150.
PPM 411F Current Reference – £150.
HP 5363B Time Interval Probes – £150.
HP 8900B Peak Power Calibrator – £100.
HP 59313A A/D Convertor – £150.
HP 59306A Relay Actuator – £150.
HP 2225CR Thinkjet Printer – £100.
TEK 178 Linear IC Test Fixture – £150.
TEK 576 Calibration Fixture – 067-0597-99 – £250.
HP 4437A 600 Ohm Attenuator – £100.
HP 8006A Word Generator – £150.
HP 1645A Data Error Analyser – £150.
Texscan Rotary Attenuators – BNC/SMA 0-10-60-100DBS – £50-£150.
HP 809C Slotted Line Carriages – various frequencies to 18GHZ – £100 to £300.
HP 532-536-537 Frequency Meters – various frequencies – £150-£250.
HP 3200B VHF Oscillator – 10MC/S-500MC/S – £200.
Barr & Stroud variable filter EF3 0.1Hz–100kc/s + high pass + low pass – mains – battery – £150.
Krohn-Hite Model 3202R filter – low pass, high pass.
Krohn-Hite 4100 oscillator.
Krohn-Hite 4141R oscillator – .1Hz–10,000kHz.
Krohn-Hite 6880 programmable distortion ANZ-IEEE-488.
Krohn-Hite 3750 filter, low pass, high pass – .02Hz–20kHz.
Parametron D150 variable active filter, low pass – high pass – 1.5Hz–10kHz. £100.
S.E. Lab SM215 Mk11 transfer standard voltmeter – 1000 volts.
Fluke 4210A programmable voltage source.
Ailtech Stoddart P7 programmer – £200.
Fluke 8500A digital multimeter.
H.P. 3490A multimeter.
H.P. 6941B multiprogrammer extender. £100.
Fluke Y2000 RTD selector + Fluke 1120A IEEE-488-translator + Fluke 2180 RTD digital thermometer + 9 probes. £350 all three items.
H.P. 6181 DC current source. £150.
H.P. 59501A – HP-IB isolated D/A/power supply programmer.
H.P. 3438A digital multimeter.
H.P. 61775 DC current source.
H.P. 6207B DC power supply.
H.P. 741B AC/DC differential voltmeter standard (old colour) £100.
H.P. 6209B DC power unit.
Fluke 80 high voltage divider.
Fluke 887AB AC – DC differential voltmeter.
Fluke 431C high voltage DC supply.
H.P. 1104A trigger countdown unit.
Tektronix M2 gated delay calibration fixture. 067-0712-00.
Tektronix precision DC divider calibration fixture. 067-0503-00.
Tektronix overdrive recovery calibration fixture. 067-0608-00.
Avo VCM163 valve tester + book £300.
H.P. 5011T logic trouble shooting kit. £150.
Marconi TF2163S attenuator – 1GHz. £200.
PPM 8000 programmable scanner.
H.P. 9133 disk drive + 7907A + 9121 twin disk.
Fluke 730A DC transfer standard.
B&K level recorder 2307 – £500.
B&K 2113 audio frequency spectrometer – £150.
B&K 4815 calibrator head.
B&K 4812 calibrator head.
B&K 4142 microphone calibrator – £100.
B&K 1022 band FX oscillator – £100.
B&K 1612 band pass filter set – £150.
B&K 2107 frequency analyser – £150.
B&K 1013 BFO – £100.
B&K 1014 BFO – £150.
B&K 4712 FX response tracer – £250.
B&K 2603 microphone amp – £150.
B&K 2604 microphone amp – £200.
B&K 2019 analyser – £350.
Farnell power unit H60/50 – £400 tested.
H.P. FX doubler 938A, also 940A – £300.
Racal/Dana 9300 RMS voltmeter – £250.
A.B. noise figure meter 117B – £400.
Ailtech 360D11 + 3601 + 3602 FX synthesizer 1Mc/s-2000Mc/s. £500.
H.P. sweeper plug-ins – 86240A – 2–8.4GHz – 86260A – 12.4–18GHz – 86260AH03 – 10–15GHz – 86290B – 2–18.6GHz. 86245A 5.9–12.4GHz.
Telequipment CT71 curve tracer – £200.
H.P. 461A amplifier – 1kc–150Mc/s – old colour – £100.
H.P. 8750A storage normalizer.
Tektronix oscilloscopes type 2215A – 60Mc/s – c/w book & probe – £400.
Tektronix monitor type 604 – £100.
Wiltron 560 network scaler + 2 heads + book – £1000.
Marconi TF2330 or TF2330A wave analysers – £100–£150.
HP5006A Signature Analyser £250 + book.
HP10783A numeric display. £150.
HP239A oscillator – £250.
Ailtech 7009 hot–cold standard noise generator.
HP 3763A error detector. £250.
Cushman CE-15 spectrum analyser – LED Readout – 1000Mc/s £650.
Tektronix 5L4N spectrum analyser – 0–100kc/s £500.
HP1742A 100Mc/s oscilloscope. £250.
HP1741A 100Mc/s oscilloscope. £250.
Tektronix 7104–7A29–7A24–7B15–7B10 – £2K.
Racal/Dana signal generator 9082 – 1.5–520Mc/s – £800.
Racal/Dana signal generator 9082H – 1.5–520Mc/s – £900.
Claude Lyons Compuline – line condition monitor – in case – LMP1 + LCM1 £500.
HP1815B T.D.R. sampler + 1817A head – 1104A trigger + 1106B TD mount £500.
Texscan AL-51A spectrum analyser – 4–1000Mc/s – £750.
Efratom Atomic FX standard FRT – FRK – .1–1–5–10Mc/s £3K.
Muirhead fax receivers K649 – TR4 – solid state – speed – 60–90–120–240–auto – IC 288-576 – auto. £250 with book.
Racal 4D recorder – £350.
HP8350A sweep oscilloscope mainframe + HP11869A RF PI adaptor – £2.5K.
Ailtech – precision automatic noise figure indicator type 75 – £250.
Adret FX synthesizer 2230A – 1Mc/s. £250.
Tektronix – 7S12–7S14–7T11–7S11–S1–S52–S53.
Rotek 610 AC/DC calibrator. £2K + book.
Tektronix 7L12 analyser – 1Mc/s–1.8GHz. £1500.
Clark Scam Heavy Duty 40' Telescopic Pneumatic Masts – retracted 7'8" – head load 40lbs – with or without supporting legs & erection kit – in bag + handbook – £200-£500.
Clark Scam Heavy Duty 70' Telescopic Pneumatic Masts – retracted 13'5" – head load 90lbs – with or without legs + erection kit + handbook – £500-£800.

ITEMS BOUGHT FROM HM GOVERNMENT BEING SURPLUS. PRICE IS EX WORKS. S.A.E. FOR ENQUIRIES. PHONE FOR APPOINTMENT OR FOR DEMONSTRATION OF ANY ITEMS. AVAILABILITY OR PRICE CHANGE. VAT AND CARR., EXTRA.

Johns Radio, Whitehall Works, 84 Whitehall Road East, Birkenshaw, Bradford BD11 2ER. Tel. No. (0274) 684007. Fax 651160.

CIRCLE NO. 118 ON REPLY CARD

Hybrids at the heart of radio-frequency combiners

Several VHF or UHF broadcasting channels can be transmitted simultaneously from a single antenna. Dick Manton explains the combining role of hybrids.

Early VHF television transmissions in the UK used separate antennas for vision and sound channels. But today all UK television stations combine at least two vision and sound channels into a single antenna. At most stations the transmission authorities cooperate to combine all four local channels. Similarly, at least three FM channels are combined into most of the FM broadcasting antennas in the UK.

At the heart of most of these channel combiners is a pair of hybrids.

The illustration shows part of A Band 2 combiner which has been manufactured by Alan Dick & Co Ltd to combine five 20kW FM channels. The hybrid shown in the foreground has 6.125in IEC ports and a body diameter of 15in (381mm) to deal with high peak voltage and output power.

We have already seen (Split personality of hybrid directional couplers, *EW + WW*, July, pp. 556-559) how some radio-frequency hybrids are able to split power, reasonably equally, between two output loads over a wide frequency range while maintaining a very well matched input impedance. The same hybrids are also capable of combining two phase-locked signals into a single output load – provided that the relative phases applied to their input terminals are taken into account.

Hybrids can also be used to form two-channel-combining networks if the two channels are within the working band of the hybrid (**Fig. 1**). Here we will consider only the "3dB" hybrid which (see July article) is formed when a quarter-wavelength of a pair of parallel transmission lines are coupled in a particular way. The physical and corresponding symbolic arrangements, showing the phase differences between ports, are illustrated in Fig. 1. Power entering at *A* is split equally between *B* (phase lag 90°) and *C* (no phase lag); no power reaches *D*. Similarly, power entering *D* is split equally between *B* (no phase lag) and *C* (phase lag 90°); notice that in the latter case the phase relationship between *B* and *C* has been reversed.

Channel combiners with no resonators

One type of channel combiner that is widely used at low-power television transmitting stations in the UK makes use of the *B* and *C* phase reversal, when either *A* or *D* is used as the input port.

The combiner consists (**Fig. 2**) of two hybrids connected back-to-back by two unequal lengths of coaxial transmission line. If f_1 and f_2 are the two input frequencies in MHz, the two transmission lines (velocity factor v) have to differ by a length d, in m, equal to $150v/(f_2-f_1)$. If the difference in electrical path lengths at f_1 is n wavelengths, the difference at f_2 is then $n+0.5$ wavelengths. By tracing out electrical path lengths for f_1 and f_2 in Fig. 2, we can see that f_1 and f_2 both combine in phase when they reach port *D* of the second hybrid and cancel out at the load on port *A*. Other frequencies apportion themselves between *A* and *D*, with a result that the input impedance remains constant with frequency. There are two other major advantages with this type of combiner: the combiner contains no resonators, so there is no voltage or current magnification at any point in the circuit and there is a constant group delay (linear phase change with frequency) across each input band.

Also, the frequency of any 3rd-order intermodulation product such as $2f_2-f_1$, which may be generated in the f_2 transmitter, is such that it is absorbed in the load *A* on the second hybrid.

Where four channels at the same transmitting site are reasonably spaced it is usually possible to combine them by means of three units similar to those shown in Fig. 2. Frequencies f_1 and f_3 are combined in one unit and f_2 and f_4 in another. Both pairs of channels are then fed to the input ports of a third unit

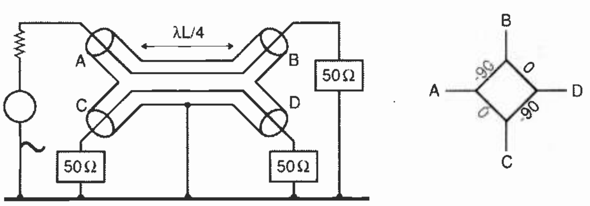


Fig. 1. 3dB coupler hybrid and its symbol showing phase relationships.

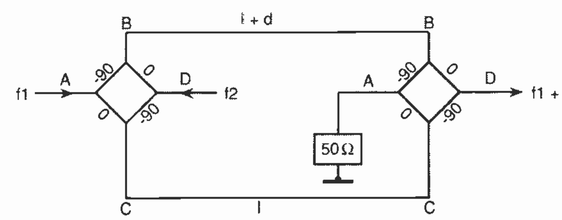


Fig. 2. Multichannel combiner using two hybrids and unequal lengths of interconnecting feeders, widely used at low-power television transmitting stations.

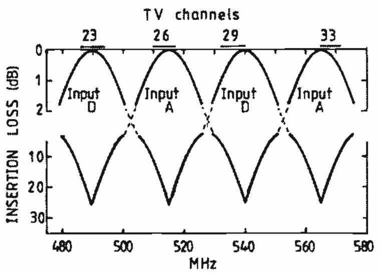


Fig. 3. Insertion loss characteristics of the combiner shown in Fig. 2, designed to combine two pairs of television channels. (d = 3.9m; velocity factor of feeder = 0.67)

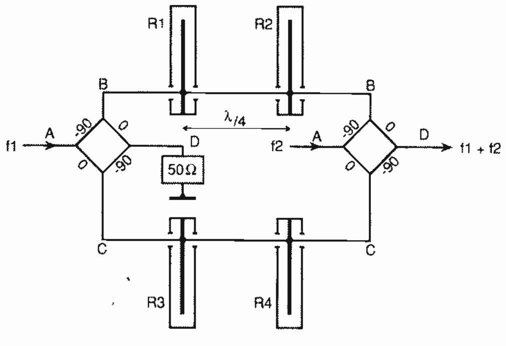


Fig. 4. A narrow-band/wide-band combiner. R_1, R_2, R_3 and R_4 are f_1 bandpass resonators. The f_1 input is narrow-band and the f_2 input is wide-band.

where d is a compromise for establishing suitable phase differences between paths – path lengths at alternative frequencies must differ as closely as possible by a half-wavelength.

At a UK television station, where channels with mid-band frequencies of 490MHz, 514MHz, 538MHz and 570MHz have to be combined, suitable feeder length differences d (when v = 0. 67) for 490MHz and 538MHz would be 2.1mm; 514MHz and 570MHz require 1.8m and the four-channel combiner requires 3.9m. Through-loss characteristics of the final four-channel combiner for these frequencies demonstrate (**Fig. 3**) that though the bandwidths of all channels are the same, they are slightly displaced relative to the desired centre frequencies because of the irregular channel spacing. All losses between input ports are dependent on the construction of the hybrids, but they will normally be in excess of 25dB. (Some bandpass filters in the outputs of the transmitters may be needed to keep intermodulation products down to an acceptable level.)

Channel combiners with resonators

Another type of channel combiner employs back-to-back hybrids, but uses resonators to provide frequency-dependent paths.

In **Fig. 4**, R_1, R_2, R_3 and R_4 are resonators attached in pairs one quarter-wavelength apart along the equal interconnecting coaxial lines between the hybrids.

The resonators are band-pass circuits, designed so that they resonate at frequency f_1 and so allow free access along the interconnecting lines only at that frequency. Power at frequency f_1 which enters port A of the first hybrid, splits then recombines at port D of the second hybrid. Because the loaded Q_L of each resonator is relatively high (typically 100 for an FM combiner) each resonator creates a near short-circuit (ie approx 100% 180° voltage reflection) across the line for frequencies far removed from f_1. As a consequence, any power at these frequencies entering port A of the second hybrid emerges at B and C, where it is 100% reflected and also recombines at output port D. By symmetry, any frequency other than f_1, such as an intermodulation product, entering port A of the first hybrid will be transferred to the resistive load on port D of the first hybrid. The result is that matched input impedances are again seen at all frequencies.

Cross-loss between input ports at frequency f_1 is determined by the balance of the hybrids, and is typically better than 30dB. At other frequencies the cross-loss is supplemented by the very high susceptance of the resonators.

Figure 5 shows the through-loss characteristics of this type of channel combiner using four resonators, each with Q_U = 10,000 and Q_L = 100. The Q_Ls of the resonators in each arm determine the shape of both the narrow-band and wide-band input characteristics, while the Q_Us determine the absolute levels of losses. As stated earlier, the use of resonators leads to a sloping group-delay curve – noticeable on both the narrow-band channel and on the wide-band channel close to the frequency of the narrow-band signal. Broadcasting authorities sometimes impose tight restrictions

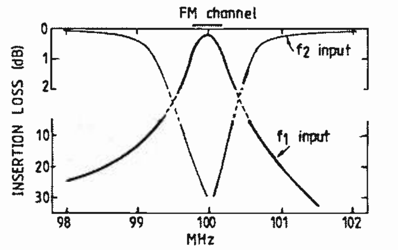


Fig. 5. Insertion loss characteristics of the combiner shown in Fig. 2 when it is designed to combine a 100MHz FM channel with several others. (Each resonator has Q_U = 10,000 and Q_L = 100.)

on the change of group delay across a channel to preserve pulse shapes and colour information in TV, or integrity of subcarrier information on FM. It can be modified by increasing the number of resonators or by changing to different combinations of loaded Qs.

The usual mechanical layout of a 3dB coupler hybrid does not lend itself readily to a symmetrical combiner layout. But this disadvantage is easily overcome by arranging a 180° twist in the coupled lines or their end-connections within the casing of the hybrid (**Fig. 6a**). Several wide-band/narrow-band channel combiner units can be coupled in series to combine more than two channels (**Fig. 6b**). The maximum peak RF voltage in a combiner of this type is developed in the resonators closest to the last wide-band input port and is (1.1 to 1.4)$\sqrt{Q_L}$ multiplied by the peak RF voltage of the narrow-band input carrier – depending on the internal construction of the resonators – plus about twice the sum of the peak RF voltages of the remaining carriers. There are correspondingly high currents at the other end of each of the resonators. ■

In a future article Dick Manton will describe one further type of channel combiner, using ordinary directional couplers instead of hybrids. The device is probably more interesting from the point of view of power multiplication than for its practical use.

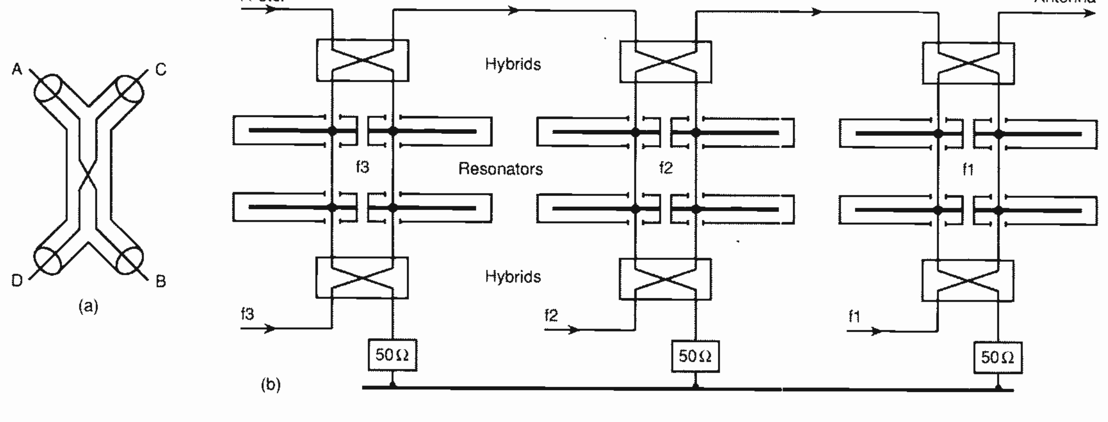


Fig. 6(a). Crossover 3dB coupler hybrid having symmetrically-disposed outputs on the same side of the coupler. (b) Multichannel FM combiner using crossover 3dB coupler hybrids and band-pass resonators.

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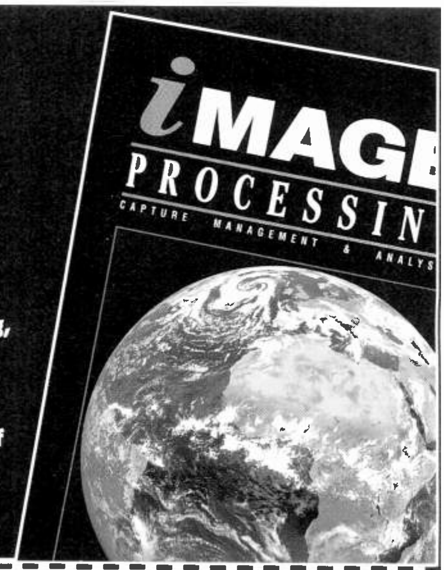

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Distorted logic

Having followed recent debates on crossover distortion (*EW + WW*, October 1990 and *EW + WW*, Letters, April 1992) I have become perturbed that Mr McLoughlin has devoted so much energy in attempting to solve a non-problem in such an unpromising way. It has been taken as fact that the best way to design a good amplifier is to make it as linear as possible before applying feedback. Admittedly this is rather easier said than done. But McLoughlin has deliberately introduced discontinuity into input/output characteristics, and negative feedback is not very good at coping with such defects.

Thermal runaway in power amplifiers has been almost unheard of since silicon power transistors became established and it is quite wrong to portray average amplifiers as balancing on the edge of thermal doom. Quiescent current is a critical parameter in usual class B amplifiers, but it can be set in a second or two by using a distortion analyser and letting crossover spikes sink placidly into residuals. Even with good thermal feedback to an amplified diode, compensation for level and hence dissipation changes is only approximate. It is made much easier, as Mr Ellis ably pointed out in his letter (*EW + WW*, January 1991), if complementary feedback-pair configuration is chosen so only driver junction temperatures (which can be kept much lower) are allowed to get into the act. Why does the Darlington version still persists? It seems to have no countervailing advantages. With thermal feedback it is theoretically possible for a little crossover distortion to get through for short periods, but it is greatly preferable to a circuit which guarantees lots of it all the time.

McLoughlin takes 6mV crossover spikes on his audio far too casually. Crossover distortion has been recognised for a long time as a distortion mechanism to be feared most. It is always present at any signal level, its percentage increases sharply in quiet musical passages, and it produces high-order harmonics more subjectively disturbing than second or third.

McLoughlin's circuit leaves easily visible crossover spikes on output waveform, even when running with 100% negative feedback, and suggests a poor starting point for amplifier design. Normal class-B biasing keeps combined

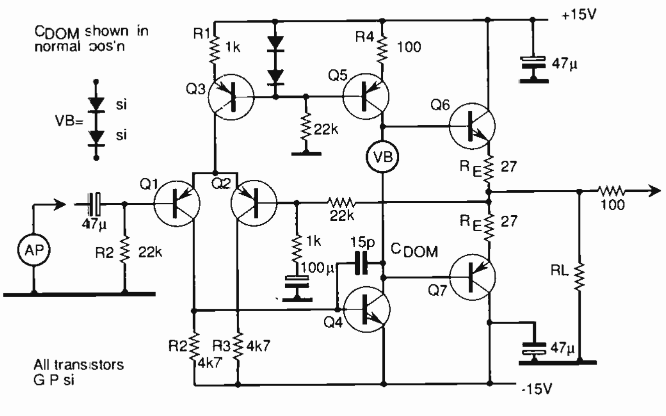


Fig. 1. Test circuit.

transconductance of an output pair roughly constant, but in this circuit each one traverses the most non-linear part of its characteristic, where it begins to turn on, in splendid isolation.

Circuits modelled using small-signal transistors often prove quite impossible to translate to realistic power levels, as power transistors are so much slower. If McLoughlin's amplifier was scaled up to produce say 30W, it would prove very difficult to stabilise with 100% NFB. How much ordinary non-linear distortion is generated by this circuit?. Reported figures are absent so we are surely justified in fearing it may be truly diabolical.

Driving a dominant-pole compensation capacitor C_{dom} from output rather than voltage-amplifier-stage (VAS) collector is not a new idea – it was advocated by Cherry in 1982[1] and others. But current through it must be sunk as well as sourced, and in the circuit shown can only go through the VAS base or R_3. It is limiting sinking current that causes slew-limiting.

Output-driving of C_{dom} reduces high frequency distortion effects at the output stage as this is now included with the local feedback loop to provide stabilisation. Practical effects are very small unless HF distortion is deliberately introduced as crossover spikes by under-biasing, as shown. I used a small-signal circuit (**Fig. 1**), which

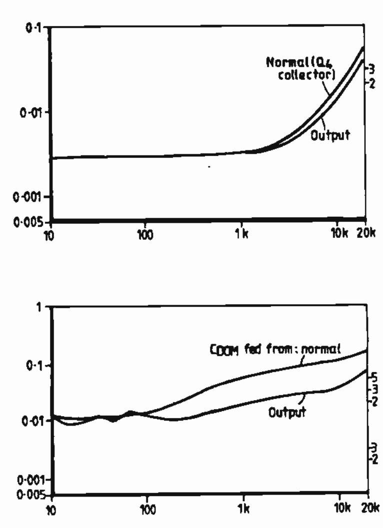


Fig. 2. O/p stage correctly biased (a), and underbiased (b) to give a peak reading of 0.05% (1kHz). Very narrow crossover spikes: Cherry is right.

is representative in many ways of real power amps, and can easily be turned into one by adding power output devices. Under-biasing is arranged to give 0.05% THD Peak at 1kHz, reading 0.003% RMS, showing just how narrow such spikes are, feeding C_{dom} output reduced it to 0.02% Peak. But spikes were clearly present on the residual

Audio interest revitalised

My interest in audio amplifier design had waned – until I read Greg Ball's letter "Distorted truth" (*EW + WW*, May 92). Now I realise a whole new area of discovery lies ahead; power supply and PSRR, and I know why some people can hear fuses and mains cable, maybe they are not crazy after all.

Here are some ideas which might solve the problem.

Don't use supply rails as references. How many amps use common emitter output stages or quasi-complementary connections?

Use differential amps before the power stage with stiff current sources. Use separately regulated supply rails for these stages.

Finally, as a professional switched-mode power supply designer I have long been looking at an excuse to use this sort of supply in an audio power amp. Regular linear supplies produce volts of audio frequency ripple at supply rails, large magnetic fields, have poor regulation, high output impedance and are big and ugly. But look at the SMPS; tightly regulated rails, low impedance, recoverable short-circuit protection, small size and above all noise and ripple outside the audio spectrum. Excuse me, I must find my ferrite data book!

A M Wilkes
Brentwood

and in no way could such an amplifier be considered for high-quality audio.

Circuit results (**Fig. 2**) appear to put driving C_{dom} from output into a "can't hurt-might help" category – but there is a real snag. Such a connection tends to induce parasitic VHF oscillation in its drivers, and can be very hard to cure without compromising other parameters.

I am sorry to appear negative towards McLoughlin's efforts, but I was prompted to write because he intends to put his circuit into a school textbook. I am afraid he will do his readers a disservice if this happens.

Douglas Self
London

References

1. Cherry, "Nested Differentiating Loops." Journal of the Audio Engineering Society; Vol 30, #5, May 1982.

Dingled angle on physics

It is now some 20 years since a British physicist (the late professor H Dingle) wrote his astonishing book, "*Science at the Crossroads*", in which he *proved*, that Einstein's theory of Special Relativity is wrong!

Unfortunately Dingle made the tragic mistake of not putting his fantastic discovery into mathematical language. Special Relativity violates common sense, but one can hardly stomach a theory that violates mathematics too! Putting Dingle's discovery into mathematical form instantly reveals Einstein had got a sign wrong in his calculations, and would have been fatal for his relativity theory.

But Dingle's neglect of the mathematics meant his book, the most important in physics this century, now lies forgotten on library shelves, classified under "History of Physics".

We owe a great debt to Dingle. It is high time his incredible discovery is recognised. Inevitably, it will take us back to his crossroads, and an evolution of entirely new physics.

Why not call that new discipline, Post Dingle Physics. That's the least we can do to honour a forgotten pioneer.

A H Winterflood
North London

Power politics and the knowledge gap

Alasdair Philips' article "Power Politics: playing with children's lives"(*EW +WW*, April 1992) demonstrates just how fluid the situation is regarding health effects of electromagnetic radiation. New evidence and theories appear regularly, yet there is still no prospect of a definitive statement about real hazards due to exposure to low level EM fields. Between epidemiological studies on one hand, and a plethora of cellular-level research and theories on another, there is a yawning knowledge gap.

Knowledge gaps allow those with responsibility and authority, but who have interests vested in promoting growth of electricity consumption, to continue to prevaricate. It also allows an uninformed public to speculate about health hazards in a way which is stressful to individuals concerned and creates suspicion and mistrust of expert opinion.

But epidemiology can only take us so far. There are confounding factors, such as possible exposure to toxic chemicals in electrical/electronic occupations which have an apparently elevated risk, or possible exposure to exhaust fumes in a case study which showed an elevated risk associated with wiring configuration and road traffic density. There are immense difficulties in assessing actual doses received, surrogate measurements cannot give even an approximate indication of complex time- and spatially-dependent dose factors which apply to people moving in real time-varying fields. Only a prospective cohort study in which subjects were constantly monitored could do this which would be prohibitively lengthy and expensive to achieve any degree of statistical significance.

Published research papers regarding cellular interactions and animal behaviour claim and disprove observable effects of field interaction. But few are independently replicated to claim scientific consensus because detail levels are insufficient. If environmental synergies are responsible for the effect – such as geomagnetic field or chemical promoter presence – it is not surprising that the effects cannot be replicated under different conditions, if parameters of original environments were not noted. Nevertheless continuing research, although better co-ordinated, will overcome many of these objections.

An approach is needed which recognises variable susceptibility and researches factors affecting sensitive people, to gain a better picture of the real hazards.

Authorities have problems admitting any kind of hazard which will open floodgates to all kinds of litigation.

Research funded by interested parties, such as the National Grid Company, will produce biased results. Credibility needs to come from a disinterested source of funds or independent administration. All those addressing the issue must be encourage to keep open minds to all available evidence.

Tim Williams
Elmac Services
Chichester

Please explain

We are told by nearly all experts there is no ether – but surely fields must have some existence.

The speed of light is said to be constant for an observer, but no one has satisfactorily explained to me how the Doppler effect operates when an observer is moving towards a source of light or radio waves. Surely if received frequency rises, it means an observer is catching up faster with peaks and troughs.

It is also claimed that the magnetic monopoles exist. I feel magnetic fields are movements of ether, or something similar, from North to South Poles and must always have entry and exit. If so, no monopole could exist because there would be no return for "Fluid".

I must admit I still think of electrons as little bullets rather than waves.

But perhaps a *EW + WW* readers could help clear up these puzzles – in non-mathematical terms.

A J Quinton
Victoria
Australia

Unity mark-space ratio

Most text books on digital logic contain a statement such as: "To obtain an exact unity mark-space ratio, generate a signal at twice the frequency required and divide by two."

If only that were true! A perfect square wave contains only desirable odd harmonics, and there is no difficulty in suppressing third and higher harmonics by passive filtration.

I attempted to make a spectrally pure VHF signal source using a *74AC74* as a divider, but with disappointing results. The second harmonic was significantly present. Close inspection of data sheet small print shows why. (I am quoting from Texas data for centre-power type *74AC11074*). Time given of the propagation low-high (t_{PLH}) as ranging from 1.5 to 8.2ns and t_{PHL} as 1.5 to 7.5ns. So a greater proportion of each cycle will be spent in output low-state rather than high.

At a clock frequency of 100MHz, the output period is 20ns. A few tenths difference of a nanosecond is significant in terms of second harmonic content. The effect is readily seen in Fig. 3 of my article "Spectrum Analysis on the Cheap" (*EW + WW*, March 1992).

It is a shame to dispose of this old myth, but as clock frequencies move constantly higher now seems to be time to do so.

Nick Wheeler
Surrey

Impulsive comment

Professor Grundy's idea of structured analogue blocks is a good one ("Structured Analogue Design Builds perfect filters", *EW + WW*, May 1992) but I do not think it will work for filters. His claim that analogue filtering is made easier is tenuous and Grundy offers no solid arguments in justification. He dismisses a very serious problem of

component tolerances in a single sentence by stating they "should not be a problem". Surely he should have analysed possible errors and given more definite conclusions.

But, my main criticism is that he has not attempted to analyse filter response in a rigorous way.

Grundy's fundamental argument – that double differentiating a signal results in an amplitude scaling with no phase shift – is fatally flawed. Whatever his filters do (and they are non-linear systems for a start) they certainly do not perform like a low pass filter with no phase shift. His problem is that the real world is not made up of sine waves, but impulses. Contrary to Grundy's introduction, digital filters *do* introduce a phase shift, or at least a constant delay. Put an impulse into a low-pass filter with no phase shift at all and it will not be stable.

David Gibson
Leeds

Caution casual reader

David Grundy's article entitled "Structured Analogue Design Builds Perfect Filters" (*EW + WW*, May 1992) proposes two non-linear filter designs. Type II design is based on the equation

$$V_{out} = \frac{V_{in}^{N+1}}{V_{in}^{N} + \left(-\frac{d^2}{dt^2}V_{in}\right)^{N}}$$

and the type I is based on

$$V_{out} = \frac{V_{in}^{N+1}}{\left(V_{in} - \frac{d^2}{dt^2}V_{in}\right)^{N}}$$

While these designs will work as advertised for single frequency sinusoidal input signals, their performance will be quite different when subjected to multiple frequency inputs and are due to large amounts of intermodulation distortion caused by the non-linear exponentiation process.

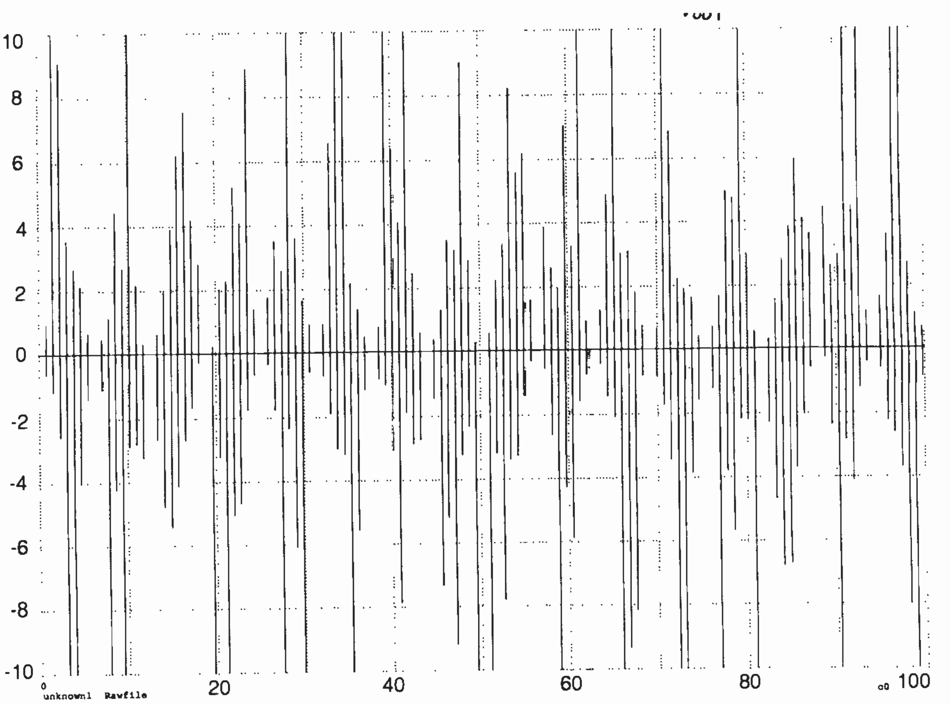
If an input signal is the sum of two sinusoids whose respective frequencies place one in the passband an a second in the stopband, then an ideal filter would have only the pass band signal present at its output. Unfortunately, this does not occur for these filters. To illustrate, consider Grundy's type II N=5 design with an input of V_{in} = sin0.5t + sin4t

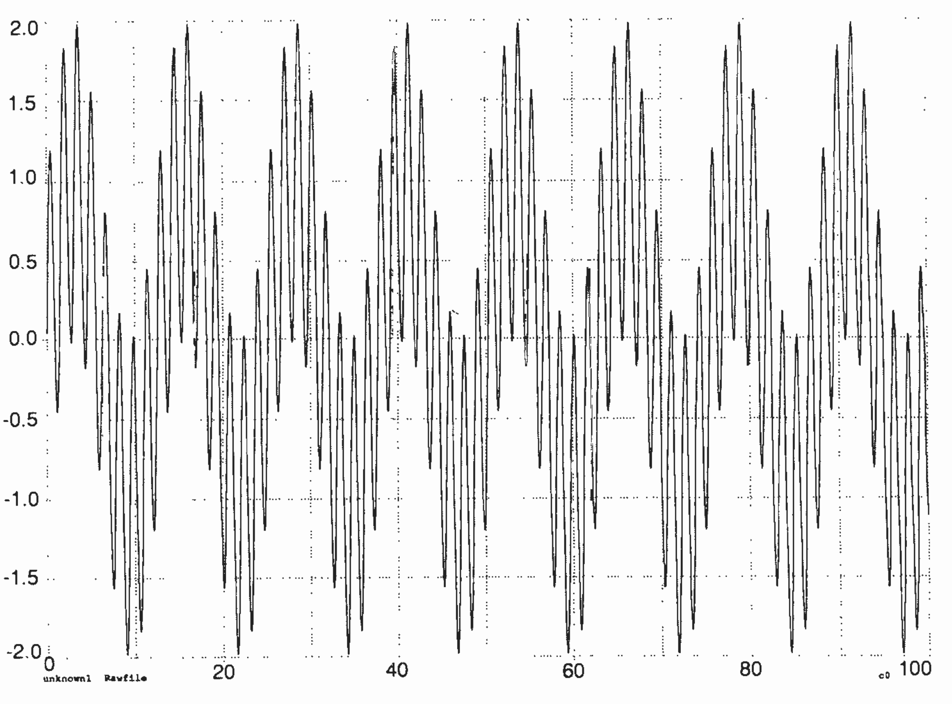
Output will be given by:

$$V_{out} = \frac{(\sin 0.5t + \sin 4t)^6}{(\sin 0.5t + \sin 4t)^5 + (0.25\sin 0.5t + 16\sin 4t)^5}$$

In plots detailing V_{in} and V_{out}, notice that the output does not represent the desired response but contains many high order mixing products.

While there may be valid real world applications for these types of filters, casual readers should be cautioned against their generalised application.





Plots detailing V_{in} (top) and V_{out} (above). Output does not represent desired response but contains many high order mixing products.

Jim Mittel
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Florida

SQUEEZING INTO THE PICTURE

Much has happened since the Fractal Transform emerged as a contender for commercial image compression and decompression products. OEM products using the technique have appeared, and the technique now has gained wide endorsement. But the technique has yet to prove itself for motion picture compression. Andy Wright reports.

Fractal image compression and decompression exploits the mathematics of fractals to provide very high compression ratios together with resolution independence. Despite its youth compared with industry standards like JPEG, the Fractal Transform is rapidly winning fans throughout the industry. According to Greg Riker, director of product development at Microsoft's multimedia publishing group: "Fractal technology offers the highest usable compression on the market." Microsoft has now licensed Iterated Systems' software and fractal products are scheduled to appear on the market later this year.

Image compression has long been a vital tool in computer graphics and digital video. Until recently, techniques based on the discrete cosine transform (DCT) have set the standard. It is estimated that around 90% of applications use the DCT, incorporated as it is in international standards such as the ISO Joint Photographic Experts Group, JPEG.

Details of the DCT are explained in a previous article in *EW + WW* (Vol. 97, No. 1675, p. 431, June 1992). Briefly, it is a particular type of discrete Fourier transform, which maps the image into frequency space. A predefined set of cosines is applied as 'basis functions' to the image, resulting in a set of amplitudes (DCT coefficients) that, together with the basis functions, reproduces the original image in frequency space. Large-scale features form low-frequency components, whilst smaller-scale features become high-frequency components.

Finding DCT coefficients does not in itself lead to any data compression. However, as the human eye is less sensitive to high-frequency components, these can be eliminated to compress the image.

One disadvantage is that, at large compression ratios, pixelation becomes apparent; the decompressed image looks 'blocky'. Furthermore, artifacts begin to appear, such as the Gibbs phenomenon; rippling that appears where there is a high degree of contrast

Standard compression (left) vs Fractal Transform compression. Detail from a larger picture blown up to demonstrate the resolution enhancement available with the Fractal Transform process.

between areas of the original picture.

Such artifacts can be reduced by variations on the DCT, such as wavelet image compression. Here more complex functions than simple cosines are applied as the basis functions. But there is a further drawback. JPEG and other standards have fixed on the 8 x 8 pixel block as the basic unit for compression, resulting in 64 DCT coefficients for each block. Decompression has to be performed at the same resolution.

Nevertheless, the development of special hardware, dedicated silicon and improved calculation techniques have produced substantial progress. Most crucially, there is substantial applications, development and silicon support. Its commercial progress is virtually unstoppable. However there are fundamental limitations to how much improvement is possible with the DCT.

Not so with the Fractal Transform, say its proponents. New it may be, but many believe it has a promising future because of its scalability and resolution independence, ability to produce 'pleasing' images even at high compression ratios together with a fundamentally limitless scope for improvement. These are all features uniquely inherent in the Fractal Transform.

Central to the algorithm is the idea that many parts of an image are self-similar: regions of the image can describe each other when twisted, distorted and shifted by an affine transformation, a type of linear transform. For example:

$$W(x,y) = (x/2 + y/4 + 1, x/4 + y/2 + 2).$$

The more general form is:

$$W(x1, x2) = (ax1+bx2+e, cx1+dx2+f)$$

where a, b, c, d, e and f are real numbers. Expressed as percentages (i.e. multiplied by 100) they are referred to as Iterated Function System codes.

A collection of contractive affine transformations, known as an iterated function system (IFS), describes a unique fractal image called an attractor. Applying the affine transformation to its attractor produces the original fractal image.

Quite complex images can be generated by taking a dot, performing an affine transformation on it, overlaying the second dot, then performing the same transformation on the new shape in its new location, and so on.

The resulting image can therefore be stored very compactly by simply storing its IFS codes. Decoding the image is simply a matter of repeatedly applying the affine transformation. All very well for decompression, but how to find the IFS codes for a complex real-world image?

Solving that problem was the pioneering breakthrough of former mathematics professor, and Iterated Systems' founder, Dr. Michael Barnsley.

His company's solution first breaks the image up into areas called domain blocks. For each domain block, it then scans the rest of the image and identifies so-called 'range regions', areas that are best described by an affine transformation from the domain block. The result is a series of affine maps, each not only describing the shrinking, twisting and deformation of the image within the range regions, but also changing brightness and contrast relative to the original. The compressed data also carry a header defining the domain block geometry of the original image.

The next stage is to store the resulting IFS codes. It is here of course that the compression comes in; identifying similar data and discarding redundant pieces of information.

The technique only works because many affine redundancies are found. In fact, it is basic tenet of Fractal Transform that real world images exhibit a high level of affine redundancy, that is, they contain many self-referencing objects. The success of the technique bears out the truth of this axiom.

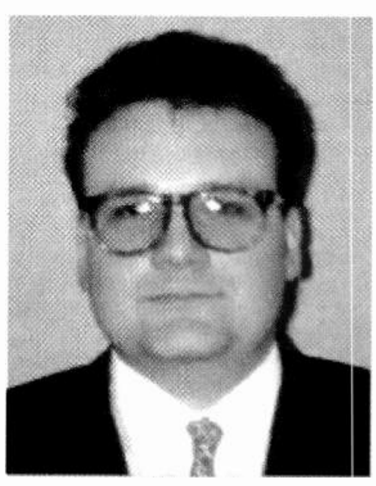
Decompression is computationally much easier using a technique known as pixel chaining. For example, take two images of equal size. Call them A and B. They can be any image, even random data. Transform the contents of A into B using the IFS codes generated from the original image. B is divided into domain blocks according to the header of the compressed file, and for each domain, locate and transform the range block data from A. B becomes a completely new image.

Next, transform the data from B into A, again using the affine maps from the compressed image. This time, A is divided into domain blocks and B has the range data.

Keep on doing this repeatedly until there are no significant differences between A and B. At this point, we are back to the original image: a consequence of Fractal geometry.

The beauty of pixel chaining is that it can start with any images, at any resolution. All video and graphics standards can be accommodated.

How closely the result matches the real-life original depends on how accurately the range regions had matched the domain blocks in the original compression process.



Right hand picture is detail extracted from a 4kbyte Fractal Transform file compared with the same detail taken from the 301k original file.

Improving on 1000 years

Refinement of the Fractal Transform method has been largely the refinement of fractal theory to improve the probabilistic search routines and enhance this match. To get a perfect match would take many years of calculation. Indeed when the Fractal Transform was first proposed, it was estimated that the calculation time would be of the order of 1023 years.

To get to a more realistic time scale, it is necessary to make approximations. Iterated Systems' skill is largely attributed to knowledge of when errors of approximation are important; being an iterative process, even small discrepancies could be amplified explosively. The art is to make approximations where the computation will damp errors rather than multiplying them.

With such research, there is no theoretical limit to the amount of improvement possible. One could go on improving the probabilistic search routines, modifying the geometry of domain blocks – all in the search for greater affine redundancy.

The company has now refined the process to the extent that it is now able to offer compression as well as decompression in software. Previously, compression required special optimised hardware.

Naturally compromises have had to be made. The software compression algorithms perform less of the deep searches that dedicated hardware can make but, at the end of the day, the result is only 5% worse than is possible with dedicated hardware in terms of image quality.

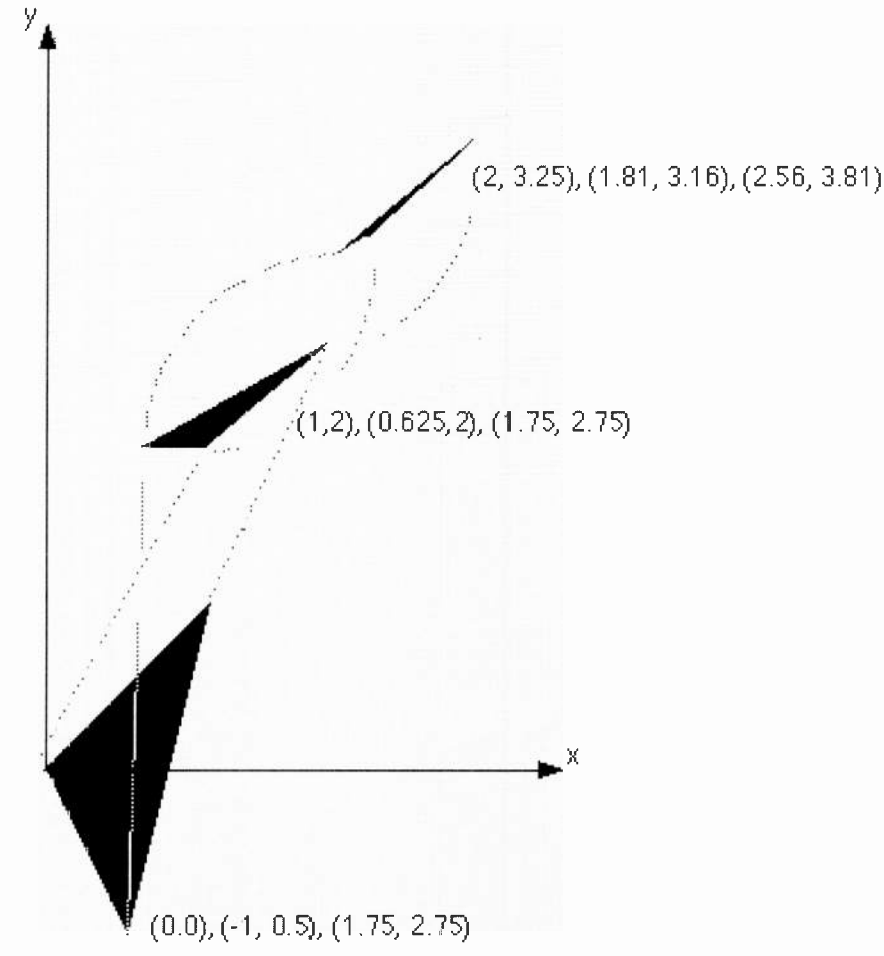
The process is still highly asymmetrical: where decompression can be processed on the fly at frame rate, with a 33MHz '386 compression typically takes several minutes.

A further demonstration of its potential came about with Racal Radio's announcement of PICTOR, a system for transmitting images over HF radio links. With PICTOR, the Fractal Transform is used to compress 768Kbyte images down to just 10Kbytes. As a result, images that would normally take hours to transmit can be sent in just six or so minutes. The system has obvious applications with security services and civilian authorities.

Endorsements like this, together with improvements in the technique itself, bode well for the future of fractals. A recent research report from the Gartner Group of market analysts predicts that the Fractal Transform has a 50% probability of becoming the *de facto* image compression standard. Previously it had given the technique a 20% chance.

Silicon support for the Fractal Transform has recently received a boost in the form of a $2million grant from the US government. Under its Advanced Technology Program, the National Institute of Standards and Technology is funding research into devices for fractal based high-fidelity image compression. The ultimate aim is silicon that could be used in high definition TV applications.

Whether based on DCT or Fractals, real image compression systems incorporate further lossless techniques to code the data more compactly. Run-length coding squeezes data by contracting strings of similar values; for example the sequence 1, 1, 1, 2, 2, 2, 2, 2, 5, 5, 5, 5, 1, 1, 1 is expressed as 3, 1, 4, 2, 4, 5, 3, 1. Huffman coding is a technique where patterns of data are assigned a compact code. The most frequently-occurring patterns have the shortest codes, whilst uncommon patterns have longer codes. Hence this is variable-length coding, more generally referred to as statistical coding. Thus the JPEG standard applies various techniques in following order: DCT; quantisation; run-length code; Huffman code.



Central to the Fractal Transform is the idea that many parts of an image are self-similar: regions of the image can describe each other when twisted, distorted and shifted by an affine transformation, a type of linear transform. For example this drawing shows a triangle undergoing successive affine transformation derived from the function $W(x,y) = (x/2 + y/4 + 1,\ x/4 + y/2 + 2)$

Moving images

For moving images, additional techniques are employed, which can be combined with various types of lossy and lossless compression.

Although fractals are pacing JPEG for still pictures – coding times are measured in minutes while decoding takes seconds – they have yet to make an impact on moving pictures. Clearly, since a moving picture can be broken down into a series of still images, applying any of the standard image compression techniques to each frame will provide a degree of compression, say a factor of 10 or 20 would be acceptable. But the computational and bandwidth constraints are much greater for displaying moving pictures.

For instance a compact disc player is capable of transferring data at 1.4Mbyte/s. Even TV-standard images are equivalent to 260 lines of 350 pixels, at 50Hz frame rates, an order of magnitude greater than this.

Fortunately, most real-world moving images already have a degree of redundancy built-in. The image changes little between successive frames, so compression can be achieved by storing differences between successive frames, rather than the whole image.

This is the approach adopted in Intel's RTV and PLV standards used for its Digital Video Interactive (DV-I) technology. Here, a reference frame is stored, then subsequent frames are subtracted from it and coded as differences known as delta frames. The reference frame is refreshed after around 60 frames.

Further compression is achieved by storing colour information only for every fourth pixel. Hardware interpolates between pixels to avoid blockiness.

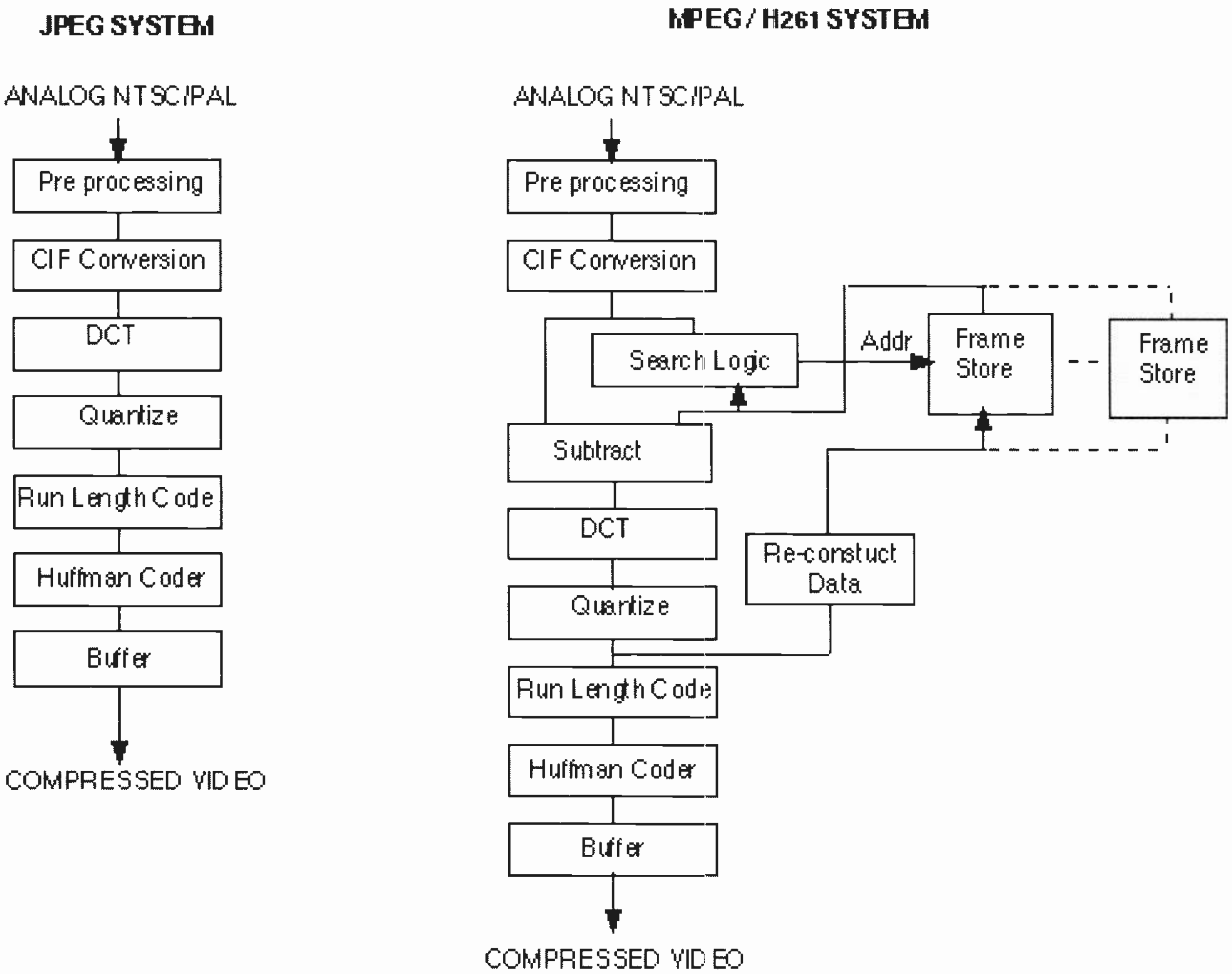
The motion estimation principle undergoing standardisation by the ISO Motion Picture Experts Group likewise exploits the fact that images do not change much between frames. However, it improves on the delta frame concept by making the reasonable assumption that changes between successive frames can be described by groups of pixels moving within the image. In other words, parts of the current picture are translations of parts of another picture at another time.

Inter-frame coding with MPEG-1 works on 16 x 16 blocks of pixels. It searches adjacent frames for a macro block of pixels that match the macro block of pixels in the current frame, and derives a motion vector defining the relative position of the matched macro block.

It works both forward and backward in time. For areas that exist in a previous frame, it uses an earlier reference, whilst for an area uncovered by a subject moving, it can use a later reference

In practical applications, there will still be differences between the predicted image produced by motion estimation, and the actual current image. Small errors can be smoothed by filtering through a loop filter, and the errors still present can also be coded as differences. Thus the MPEG compressed video image is a complex combination of an intra-frame coded base image; inter-frame coded motion vectors and intra-coded difference data.

Where JPEG is symmetrical, applying DCT and coding one way, the inverse DCT and decoding in the reverse path, the MPEG approach is asymmetrical with moving images. More computational power is required for compressing the data than decompressing it, the latter having only inverse DCT as its main computational requirement.



Pictures in silicon

With standards very much under development, it is not surprising that image compression and decompression have moved slowly to silicon.

Intel's DV-I is perhaps the furthest advanced. The i750 video processor chips use DSP technology, with a pixel processor implementing video and graphics compression routines via an on-chip microcode instruction ram. Being programmable, the processor can implement a range of compression algorithms, and can be reprogrammed to accommodate evolving standards.

Closely coupled to an associated display processor chip, both devices use on-chip hardware to perform frequently-used operations such as filtering and statistical decoding. There is extensive support including JPEG for still images, and improved routines for motion estimation. RTV can also be ported to other processor architectures.

MPEG has less direct support in silicon. But major vendors have separate devices performing individual image manipulation tasks, and are moving towards single chip solutions.

SGS-Thomson, for example, has discrete cosine transform processors for JPEG-standard 8 x 8 pixel blocks, as well as multi-pixel block size operation from 4 x 4 to 16 x 16. Its most recent offering is a motion estimation processor capable of computing motion vectors and mean absolute errors for matching blocks. It conforms with CCITT and MPEG standards, but requires additional circuitry for a full MPEG solution. Needless to say, more integrated solutions are in the pipeline.

The principal difference between JPEG – intended for still images – and MPEG involves the motion detection mechanism which records only the differences from frame to frame to reduce data rate. Although the MPEG compression process is computationally more intensive, decompression is essentially the same for both systems.

GEC Plessey Semiconductors is into the second generation of image compression and decompression devices. Its activities currently focus on low cost applications such as video telephony, and plans are well advanced to introduce a highly integrated encoder for H.261 – effectively a subset of MPEG standards specifically for video phones. First silicon should be sampling as you read this.

The H.261 encoder will incorporate motion compensation as well as lossy transmission. A cell-based silicon design approach has been adopted to combine flexibility with optimised performance. Such versatility means much of the design effort could be reused in developing future JPEG and MPEG devices.

Conversely Motorola addressed the MPEG ISO standard directly with its recent announcement of a single-chip full motion video (FMV) decoder, which has all the functionality required to implement Level 1 of the MPEG standard, plus interface circuitry to ease development of multi-media applications. This is specifically directed at Compact Disc Interactive (CD-I) players. Rather than going the programmable route, Motorola has benefited from close ties with multi-media market leaders like Philips, and gone straight to an optimised solution. ■

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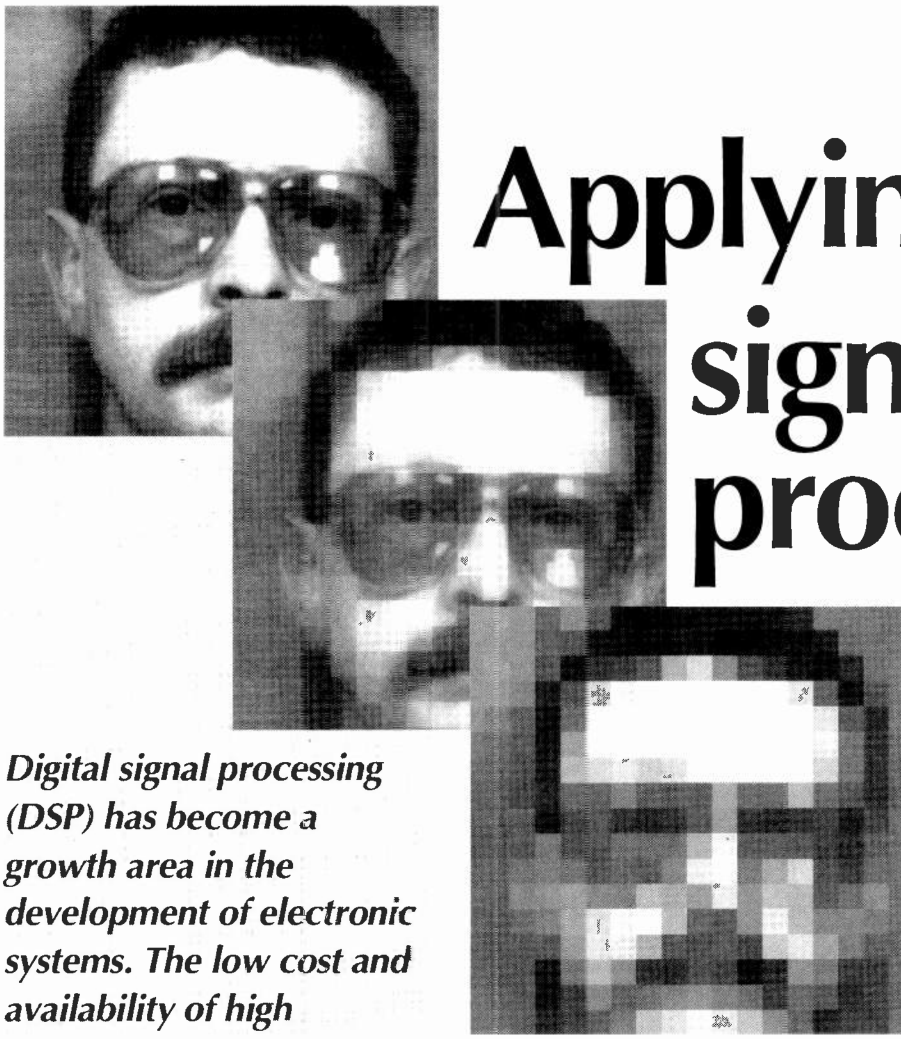
Iterated Systems	0734-880261
Motorola	0296-395292
SGS-Thomson	0628-890800
Zoran (Amega)	0256 843166



Applying digital signal processing

Digital signal processing (DSP) has become a growth area in the development of electronic systems. The low cost and availability of high performance digital signal processors has enabled the system designer to use many of the DSP techniques developed over a decade ago. Allen Brown examines a couple of the most widely used applications for the technique.

Ten years ago the execution of the Fast Fourier Transform was limited to main frames and mini computers. Today it is a standard algorithm run on all digital signal processors. The slow acceptance of digital signal processors over the past six years has been in part due to the difficulty of programming them in assembly language and the generally poor understanding of DSP algorithms.

Although many applications of digital signal processors are for real time systems where assembly language programming is usually a must, there are many applications where batch processing is the order of the day. This lifts the burden off the software because C can be used instead of assembly language.

As a programming high level language (HLL) C has increased in popularity over the past few years. There are several reasons for this: all advanced microprocessors and digital signal processors have C compilers; C has become the defacto standard programming language; C is machine independent; it is easier to maintain and design for test a C program than an assembly language program; once a C program has been debugged and is functional then it is reusable, even if the target processors are upgraded; the application of software engineering methods is generally easier for code sourced in a HLL.

However the merit of C is only part of the equation. The target hardware characteristics also merit attention. The second generation of digital signal processors were mainly fixed point devices and many useful DSP algorithms coded in C require floating point precision and arithmetic. Although C compilers for these processors have provision for coping with floating point arithmetic (through the calling of subroutines) the resultant code is often excessively long and inefficient in using the processor's on-board resources. As a result, it is common place to avoid the use of floating point numbers when trying to implement DSP algorithms in C.

In general this is poor practice since the HLL code becomes fashioned for a restrictive class of target processors and would therefore not be ideally reusable. However with the recent appearance in the market place of several floating point digital signal processors (FP-DSPs) the appeal of coding DSP algorithms in C for non real-time applications has been enhanced greatly. The FP-DSPs which are currently available from the four main processor manufacturers are given in **Table 1**. Each of the processors in the table has an optimised C compiler which naturally employs the architecture of FP-DSPs. The principal feature is the 32-bit by 32-bit floating point multiplier and accumulator (FP-MAC) which performs its calculation in a single clock cycle. The C compilers should therefore produce assembly language code which contains instructions relating to the FP-MAC thereby ensuring minimum assembly language code generation during the C compilation phase.

Manufacturer	Family and device Number
Texas Instruments	TMS320C30
	TMS320C31
	TMS320C40 (multiprocessing)
Analog Devices	ADSP-21020
	ADSP-21010 (low cost)
AT&T	DSP32C
	DSP3210(Multimedia processor)
Motorola	DSP96002

Table 1. Floating point digital signal procesors from the four main manufacturers

Many DSP algorithms have been coded in C and the availability of floating point devices opens up new opportunities for applying DSP techniques. A suitable text which contains many listings (complete with floppy disk) has been published by Embree and Kimble [1].

Applications

The Discrete Cosine Transform (DCT) is a useful DSP algorithm for image storage and transmission. For image storage purposes, a compression of at 4:1 can be achieved with relative ease using the DCT.

An image is subjected to a DCT to produce a DCT image which is then compressed before storage. To recover the image, its stored DCT version is decompressed and the resultant image is subjected to an inverse DCT (i-DCT) thus producing a good rendition of the original image.

When discussing images one uses the concept of spatial frequencies. A spatial frequency is related to the rate at which contrasts change. If one area is totally black and the adjacent area is totally white, then the spatial frequency on the boundary between the two areas is high. On the other hand if the adjacent area is dark grey, then the spatial frequency on the boundary between the black and the dark grey areas is low. Therefore when there are sharp contrasts, the spatial frequencies are high. However in most photographs and images the relative distribution of high spatial frequencies is low and this fact is used to determine the amount of data area allocated to each spatial frequency.

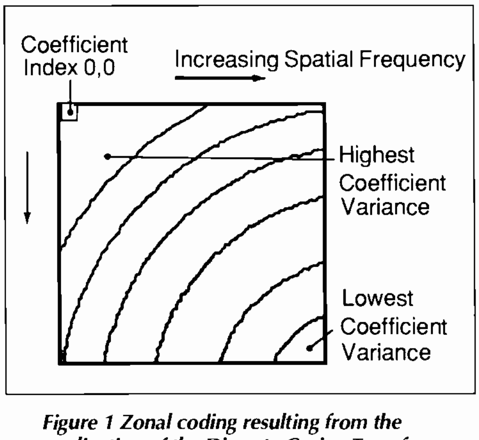


Figure 1 Zonal coding resulting from the application of the Discrete Cosine Transform on an image.

An image can be represented by a two dimensional set or an array of elements $\{f[m,n]\}$. The function $f[m,n]$ is the intensity (or greyness) of the image at the coordinate m,n. Coloured images will consist of three elements for every coordinate m,n and these will give rise to three distinct arrays which are processed separately, one for each primary colour. In the following discussion only one array will be considered (monochrome) but the argument is applicable to colour images. On a screen the image would be made up from M X N pixels (picture elements) and the Discrete Cosine Transform is defined (1) as:

$$F[u,v]=\frac{1}{NM}\sum_{m=0}^{m=M-1}\sum_{n=0}^{n=N-1}f[m,n]C_M[m,u]C_N[n,v]$$

where

$$C_M[m,u]=\cos\left[\frac{(2M+1)u\pi}{2M}\right]$$

In general the images (and their DCT) tend to be square therefore $N = M$. u,v are the spatial frequency variables (coordinates in the frequency domain) which have values ranging from 0, 1, ...(N-1) and $\{f[u,v]\}$ is the image result of performing the process in Equation 1. The i-DCT, which is the restored image is defined (2) as:

$$\tilde{f}[m,n]=\frac{1}{N^2}\sum_{u=0}^{u=M-1}\sum_{v=0}^{v=N-1}F[u,v]c[u]c[v]C_M[m,u]C_N[n,v]$$

where, $c[k] = 1$ when $k = 0$ and 2 for all other values of k. Data compression can be achieved because of the large degree of redundancy in images. Normally each value of $\{f[u,v]\}$ is stored as a byte. However much of $f[u,v]\}$ contains very little information from the original image $\{f[m,n]\}$ therefore a lot of $\{f[u,v]\}$ is redundant and can be discarded.

How do we measure the information content of a set of pixels? One way is to measure the variance of $f[u,v]$ over a set of images. If the variance is low then the information content is also low. When a DCT is performed on an image, the variance values tend to have a contour profiles as seen in **Fig. 1**. The variance tends to be a maximum for low index values (u,v) of $\{f[u,v]\}$ and a minimum for large index values of $f[u,v]$. This is actually true for the majority of images. Therefore redundant data can be by discarded by applying a discrimination quantisation scheme based on the variance profiles which is referred to as zonal coding. The quantisation value (number of bits used to store each pixel) depends on the index values of $f[u,v]$. Eight bits are allocated to store low index values of $f[u,v]$ whereas the high index values are discarded completely (0-bit allocation) with graduated values between 8 and 0 for the intermediate indices. According to the zonal coding of Fig. 1 the distribution of quantisation levels is shown in **Fig. 2**. This is equivalent to low pass spatial filtering. Using this technique a compression ratio of the order of 4:1 can be achieved – an average 8-bit pixel can be compressed into 1.5 bits.

Having established a technique for image compression, the next hurdle is to implement efficiently the DCT. It is well known that the discrete Fourier transform (DFT) requires N^2 calculations (where N is number of pixels) and when the Fast Fourier Transform is used the number of calculations is reduced to $N\log_2(N)$. When applied to the DCT the number of calculations is reduced from N^4 to $[N\log_2(N)]^2$.

To implement a fast transform in 2-dimensions a block coding method is used such that an image $\{f[m,n]\}$ can divided into many sub-images of 16 X 16 pixels (the size of the zonal coding in Fig. 2) and the DCT and zonal coding is applied to each sub-image. When starting with an image of 256 X 256 pixels, by using block coding the improvement in speed is a factor 256. However the problem with this method is that, during the reconstruction, the sub-image boundaries become perceptibly visible thus degrading the appearance of the image. But for many applications (fax machines for example) the added degradation is acceptable.

For colour images this process is performed for each primary colour. It is quite possible to code a fixed point digital signal processor using C to perform this image compression technique. However to ensure efficient compilation, it will be necessary to remove all references to floating point numbers and divisions from the source code. In effect it will be necessary to tailor the code to the target hardware. By using a floating point DSP, this restriction is removed leaving the software engineer to use the full range of options offered by the ANSI C standard. Specific application areas where image compression can be used include the manufacture of fax machines which emphasise the fast transmission of images.

Continued over page

8	8	8	7	7	7	5	5	4	4	4	4	4	4	4	4
8	8	7	6	5	5	3	3	3	3	3	2	2	2	2	2
8	7	6	4	4	4	3	3	2	2	2	2	2	2	2	2
7	6	4	3	2	2	2	2	1	1	1	1	0	0	0	0
7	5	4	2	2	2	2	1	1	1	0	0	0	0	0	0
7	5	4	2	2	2	1	1	0	0	0	0	0	0	0	0
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4	3	2	1	0	0	0	0	0	0	0	0	0	0	0	0
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4	2	2	0	0	0	0	0	0	0	0	0	0	0	0	0
4	2	2	0	0	0	0	0	0	0	0	0	0	0	0	0
4	2	2	0	0	0	0	0	0	0	0	0	0	0	0	0

Fig. 2. In zonal coding, the variance zones are allocated different quantisation values. Most of the image information is contained in the low index (top left) values hence they have the quantisation values of 8-bits

CD-ROMs are essential components of Multimedia systems and efficient methods of image compression are vital. Although signal compression process outlined above can be performed by the 80486 CPU in a PC, the throughput would be unnecessarily slow. This type of intensive processing task is best off-loaded with relative ease to an auxiliary expansion card hosting a FP-DSP.

Other uses

Signal generation is another application well suited to FP-DSPs, in the realisation of a two phase quadrature oscillator based on recursive processing [2]. This can be represented by the expression (3):

$$R(n+1) = R(n)e^{j2\pi\alpha}$$

and

$$R(n) = C(n) + jS(n)$$

where the frequency is set by the phase factor $2\pi\alpha$. The frequency is given by $f = \alpha/t_s$ where t_s is the time for one iteration of the difference equation given in Equation 2. Expanding Equation 3 gives two recursive equations (4):

$$C(n+1) = C(n)\cos(2\pi\alpha) - S(n)\sin(2\pi\alpha)$$

$$S(n+1) = C(n)\sin(2\pi\alpha) + S(n)\cos(2\pi\alpha)$$

which can implemented with relative ease in assembly language or in C as shown in **Listing 1**. If the program is executed on a fixed point processor (after tweaking to avoid the floating point calculations) there are problems. There is a slight growth in signal amplitude due to the round off effects. However when implemented on a FP-DSP directly, this effect does no occur on the same scale. **Figure 3** shows the output of the algorithm in the form of a Lissajous Figure consisting of 512 data samples.

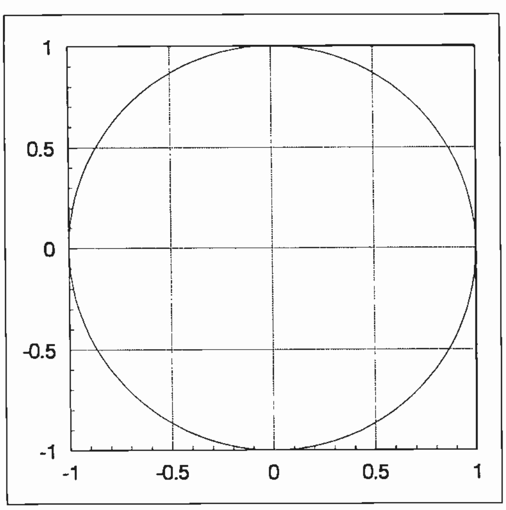


Fig. 3. Lissajous figure generated from combining the output from the quadrature algorithm Eq:4.

This algorithm can be used to great effect in several applications, some of these are: quadrature amplitude modulation (QAM) requires the generation quadrature signals of precision frequency and low harmonic distortion; generating the twiddle (phase) factor when excising an FFT; as a frequency generator with precision frequency and amplitude control.

When designing a DSP based system using a floating point processor, consideration should be given to the software engineering aspects together with savings in cost. This will necessitate careful attention to the advantages offered by C language compilers. The imminent announcement from the ANSI group of the new version of C especially devised for mathematical programming is an interesting development. Referred to as Numerical C, it is designed to deal with matrices and vectors. For example, to convolve two matrices, the following code would be used:

```
float a[100], b[100], c[100] ;
void vector_convolve() {
c[:] = a[:] @@ b[:] ;
}
```

The new version of C will make DSP algorithm coding much easier and Analog Devices are in the process of producing a version called DSP/C for their ADSP-210xx processors and this will be reviewed is a later edition of *EW + WW*. ■

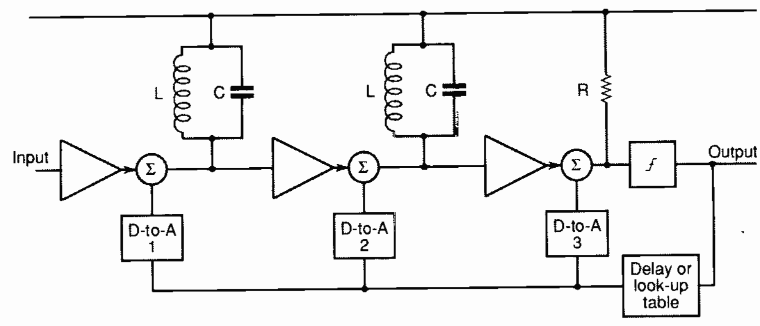
Refrerences

[1] P M Embree & B Kimble, C Language Algorithms for Digital Signal Processing, Prentice Hall 1991.

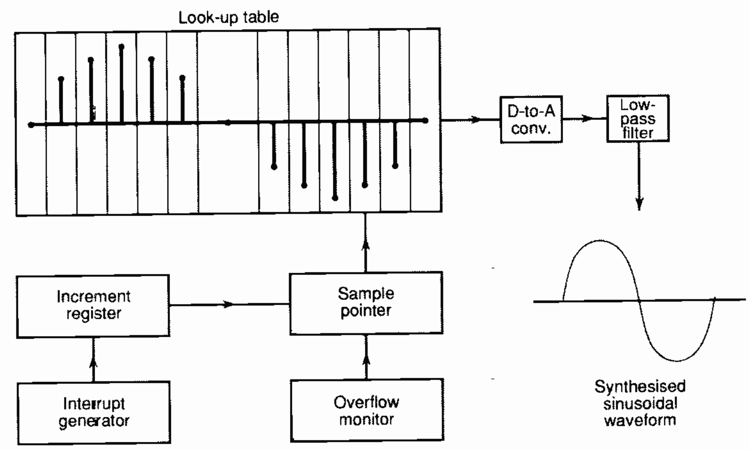
[2] R J Higgins, Digital Signal Processing in VLSI, Prentice Hall 1990.

Listing 1

```
/*Two phase quadrature oscillator */
#include<math.h>

#define PI 3.141592653
#define alpha 0.01 /* define the
frequency */
float C[2], S[2], cosine, sine ;
main()
{
cosine = cos ( 2 * PI * alpha )
sine = sin(2 * PI * alpha);
C[0] = 1.0 ;
S[0] = 0   ;

loop:
C[1] = C[0]*cosine – S[0]*sine
S[1] = C[0]*sine + C[n]*cosine;
/ * output C[1] and S[1] here * /

C[0] = C[1];
S[0] = S[1];
goto loop;
}
```



Practical implementation of a bandpass sigma-delta A-to-D converter (source A M Thurston and M O J Hawksford).



A flexible look-up table-based synthesiser for Piccolo-type data modem (source P D J Clark and M Darnell)

been recognised for specific elements of terminals, there has been neglect of the concept of a complete radio system design using these new techniques. Development of a systems architecture that would rationalise and enhance the optimal use of embedded processing is seen as offering benefits to system designers. A generic architecture was outlined that provides the benefit of linking the system performance independently so increasing computational power (both for the DSP devices and the general purpose computer host) as well as improving signal interface technology.

Professor J E Pearson (King's College London) presented a paper on behalf of Jianjun Wu and A H Aghvami on implementation of an IF adaptive equaliser for digital radio communications. The equaliser has already been shown to be capable of providing significant compensation for multipath selective fading and, by increasing the number of stages of the Bode bell network, being applicable to high-capacity digital radio communications systems. It is controlled by a microprocessor with improved Kalman algorithm to update the gain of the Bode networks. A four-stage Bode bell network equaliser has been implemented using parameters given by cad.

DSP pros and cons

At an IEE tutorial colloquium –"Circuit theory and DSP" earlier this year, Professor L F Lind (University of Essex) reviewed the pros and cons of DSP. Among the advantages, he listed:

Precision: no drift with time; 32-bit floating point arithmetic available, an absolute repeatability from unit to unit.

Versatility: ability to perform both linear and non-linear functions; chips with a powerful instruction set.

Limited time delay: Whereas analogue coils and capacitors have a (theoretically) infinite memory of past events, a finite impulse response filter has a limited memory which may be useful in avoiding pattern dependent errors such as timing jitter.

Linear phase: can be achieved with FIR filters.

One-way operation: There is no unwanted effect on input samples from output values.

Pitfalls include the need for support hardware (crystal clock, read-only-memory, A-to-D and D-to-A converters, power supply, shift registers, input and output conditioning filters). Also, to amplify an analogue signal by ten, the cost of support hardware is larger than that of a complete op-amp solution. Currently, analogue circuits work at higher speeds too, although DSP chips are improving, with higher clock frequencies and multi-action instructions.

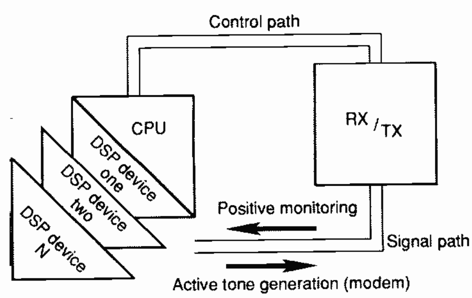
Another drawback is that to achieve optimum performance from DSP, microcode must be used – which takes a long time to learn. A complicated system code can take months to write, is then difficult to change and the chip (and instruction set) may suddenly become obsolete. The delay time of an FIR filter (some 16ms with 256 taps) may present difficulties for two-way speech.

But with the improved DSP chips now becoming available, the pluses can much exceed the minuses. Further benefits of DSP presented by Prof Lind included: time multiplexing enabling one DSP to be used as a multisection transmit filter, a multisection receive filter, and a peak detector circuit; noise immunity giving freedom from crosstalk, mains hum etc with perfect regeneration of noisy pulses; the increasingly-digital environment makes it natural to use DSP processing algorithms as additional system software.

Cost/performance trade-off

As DSP chips continue to evolve and become less costly a variety of cost/performance trade-offs are now available, making it possible to have several chips in a system working in parallel and opening new vistas for system designers. High-level software is improving – easing the design burden – and floating-point computation, increased speed, lower power consumption, lower cost, and more bits/dataword are all factors receiving attention of the chip designers.

Professor Maurice Bellanger (CNAM, Paris) stressed that virtually all forms of digital signal processing techniques can and will find application in communications and broadcasting (digital filters, filter banks, adaptive filters and vector quantisation-code representation where a set of signal samples are represented by a code). He concluded that: "The most striking point is the ever-increasing processing which is being considered for more and more diverse and demanding applications: speech coding, computer data compression, HDTV coding, hands-free telephony. While the technology is more and more ready to offer the necessary computation power, the designer has to cope with the complexity of operations. To handle these challenges successfully, the designer needs good computer-aided-engineering cae tools as well as regular contacts with current research in order to be aware of the latest results." ■



Proposed generic architecture for multi-functional terminal (source M Gallagher and M Darnell).

DESIGN BRIEF

Handier interfacing for data communication on the move

In portable applications, the 25-way D-connector specified in RS232D is a distinct embarrassment. SN75C185 allows implementation of the DB9S nine-way D-connector

Some technologies – like communications using the HF band – never seem to die, despite repeated predictions of their imminent decease. The *RS232* standard is a prime example: it just goes on and on, because it is so useful.

As a result, most semiconductor manufacturers produce ICs specifically designed to implement the interface, in place of the discrete component interface circuits originally used.

The *SN75C185* is particularly aimed at size/cost/weight/power consumption sensitive applications such as hand-held test and medical equipment, and laptops. In these applications, the size of the 25-way D-connector specified in *RS232D* (see box) is a distinct embarrassment, and a *de-facto* standard has grown up around the *DB9S* nine-way D-connector. The *SN75C185* provides just the driving and receiving elements needed to implement this version of the *RS232D* interface. Built-in circuitry provides 30V/μs limiting for the transmitters and lowpass input filters reject spikes and impulsive noise for the receivers.

Figure 1 shows the device's three transmitters and five receivers connected to a nine-pin D connector, and indicates clearly the simple

Developing the standard

RS232 was introduced by the Electronic Indutries Association in 1962, originally as an attempt to standardise the interface between data terminal equipment (DTE), such as the serial communications port of a computer, and associated data communications equipment (DCE), eg a modem interfacing to a telephone line or whatever.

But, other applications were quick to adopt the standard and its use in PCs rapidly ensured that it became the industry specification for all low-cost serial interfaces between a DTE and a peripheral – mouse, plotter, printer etc. The *C* revision, *RS2323C*, appeared in 1969 and is still often referred to though it was superseded by *RS232D* in 1986.The revision largely brought it into line with CCITT *V24* and *V28*, and with ISO IS2110.

In addition to defining line signal characteristics in terms of voltage levels, impedances and rates of change, *RS232D* also specified the mechanical interface as a 25-way D-connector.

Under the standard, a fully interlocked handshaking system controls the exchange of information over the link.

V24 defines many more lines than *RS232D*, but those that are common are compatible, and few practical applications use, or even implement, all of the lines, the most commonly used being listed in **Table 1**.

Characteristics of the signals over the communication link – an unbalanced line – are summarised in **Fig I**. Note that while *RS232C* specified a maximum line length of 15m, *RS232D* does not specify a maximum length. Instead, a maximum cable capacitance for any line of 2500pF is specified. Assuming a typical 150pF/m, the specification comes to much the same thing. With this length of line and given the specified maximum data rate of 20kb/s

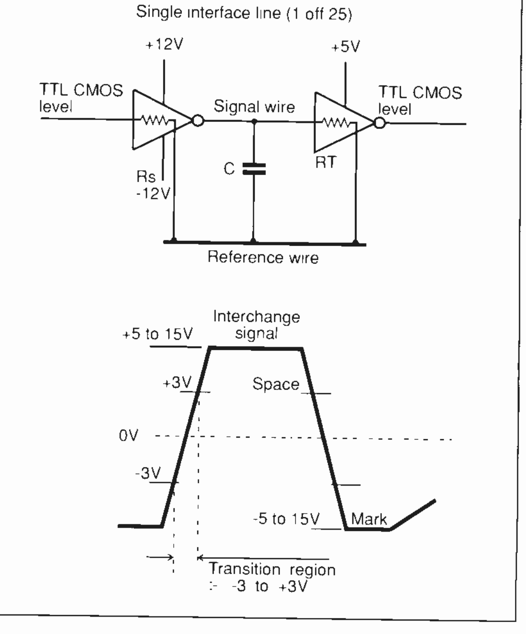


Fig. I. Electrical details of the 232D. Maximum data rate 20kb/s; max cable length depends on capacitance; single ended system; receiver input impedance R_T=3-7kΩ; driver power-off impedance R_S>300Ω; load capacitance <2500pF; output rise/time falls within the transition region: 1ms below 40b/s, 4% of pulse duration (50%) 40 to 8000b/s and 5μs >8000b/s; slew rate 30V/μs max.

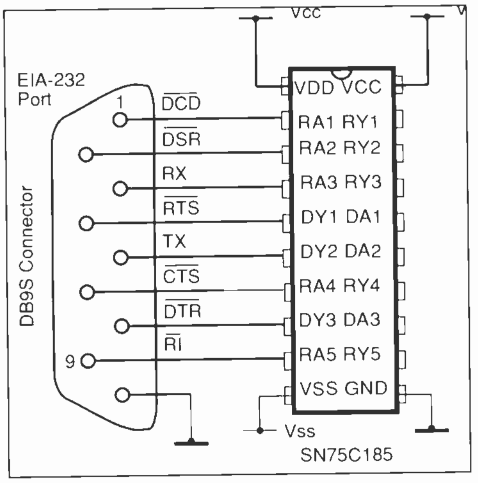


Fig. 1. SN75C185's three transmitters and five receivers connect to a nine-pin D connector. Simple interfacing is provided by the flow-through pin-out architecture.

interfacing provided by the flow-through pin-out architecture. A quick check on how the device operates is made possible by the fact that the drivers and receivers are inverting (**Fig. 2**). Logic 1 becomes a negative level on the line and a logic 0 a positive level (perhaps dating back to the days of holes and lack of them, in perforated paper tape). Connecting the three drivers in series with three of the receivers and then closing the loop back to the input of the first via one of the spare receivers (**Fig. 3**) puts the output of a receiver at logic levels, nominal ground or +5V. One receiver will quite happily drive another because, with its single +5V supply, the receiver's threshold voltages are typically +2.1V and +1.0V (positive-going and negative-going respectively, the 1V or so of hysteresis providing additional noise rejection to supplement that provided by the input lowpass filter).

The resultant odd number of inversions round the loop represents negative feedback, acting to make the devices all sit half-on and half-off. But the propagation delay round the loop ensures that the loop phase shift is way in excess of 180° at the frequency at which the loop gain has fallen to unity. In other words, we have a ring oscillator.

Figure 4 shows the output of line driver three at pin eight; the frequency of oscillation is 31kHz. With 3000pF capacitors from each driver output to ground (in lieu of the rated 2500pF maximum capacitive load), the edges slow down and as a result, the oscillation frequency is pulled down to 21.7kHz (**Fig. 5**). However, for both positive and negative going edges, the transition time through the ±3V range is a shade over 1.5μs, easily meeting both the *RS232D* and *-C* specs at 20kb/s and, with the rated 2500pF rather than 3000pF, doubtless also the 1.5μs *V28* spec. The *SN75C185* is only one of a range of *RS232D* interface devices available from the same

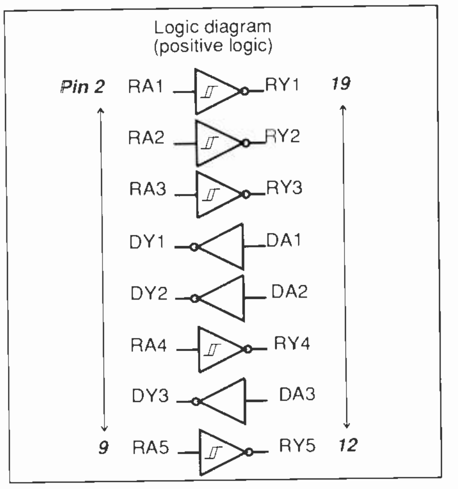


Fig. 2. A quick check on how the device operates is made possible by the fact that the drivers and receivers are inverting.

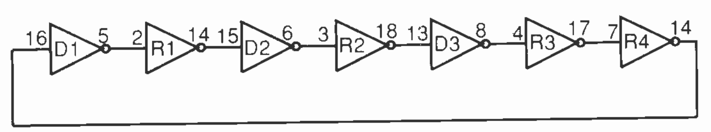


Fig. 3. SN75C185 under test as a seven-stage ring oscillator.

Fig. 4. TX and RX waveforms of a ring oscillator.

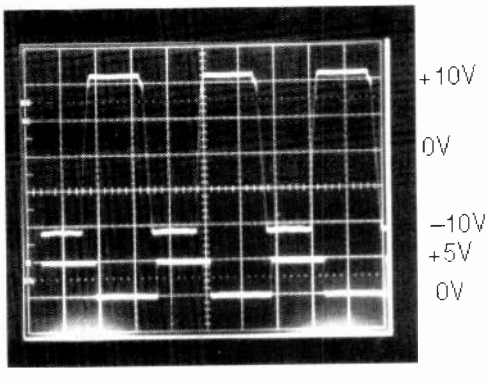


Table 1. RS232 signal designations.

Designation		DB25S pin	Common usage
Signal ground	SG	Pin 7	Interface ground reference
Signal out	SOUT	Pin 2	From the DTE to the DCE
Signal in	SIN	Pin 3	From the DCE to the DTE
Request to send transmit.	RTS.	Pin4	DTE informing the DCE it wants to Also used to control direction of communication in half-duplex system
Clear to send	CTS	Pin 5	DCE informs the DTE that the DTE may transmit. This is usually in response to a RTS and its own ready condition
DCE ready	DSR	Pin 6	The DCE informing the DTE that it is connected to a communications channel and all dialling, talking, testing etc is over. (Also called data set ready.)
DTE ready	DTR	Pin 20	The DTE informing the DCE that it is ready to transmit or receive data
Received line signal detector	DCD	(Pin 8)	The DCE informing the DTE that it is receiving valid signals over the channel. Sometimes called carrier detect
Ring indicator	RI	(Pin 22)	The DCE informing the DTE that a ringing signal is being received on the communication channel. (Used in auto-answer systems)

(more likely 19.6kb/s in practice), reflections are not a significant problem. So the line's characteristic impedance is not specified and terminating resistors are not used.

Traditionally, to meet the specified minimum driver output swing of ±5V, the output stage uses +12V and −12V supplies. But a single +5V supply suffices for the receiver, even though, in principle, positive and negative supplies would permit a slightly greater noise immunity margin.

V28 specifies that for data lines, the time taken for the line voltage to pass through the ±3V transition region should not exceed 1ms or 3% of the nominal element period, whereas *RS232C* and *-D* both specify 1ms or 4% (or 5μs above 8kb/s, in the case of *RS232D*). Any device meeting the *V28* spec will easily meet both *RS232C* and *-D*.

Transition time should not exceed 1ms for control signals, but for all signals, the minimum transition time (200ns) is set by the maximum permitted slew rate of 30V/μs, to minimise crosstalk and radiation.

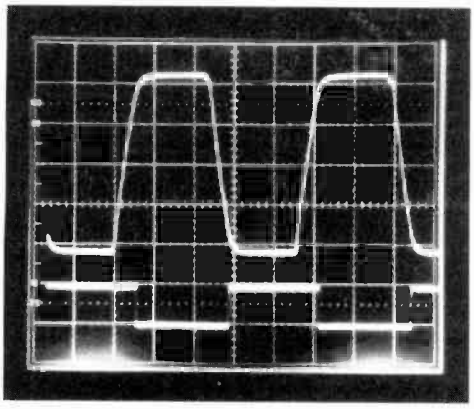


Fig. 5. TX and RX waveforms with 3000pF loading on each TX output, pins 5, 6 and 8.

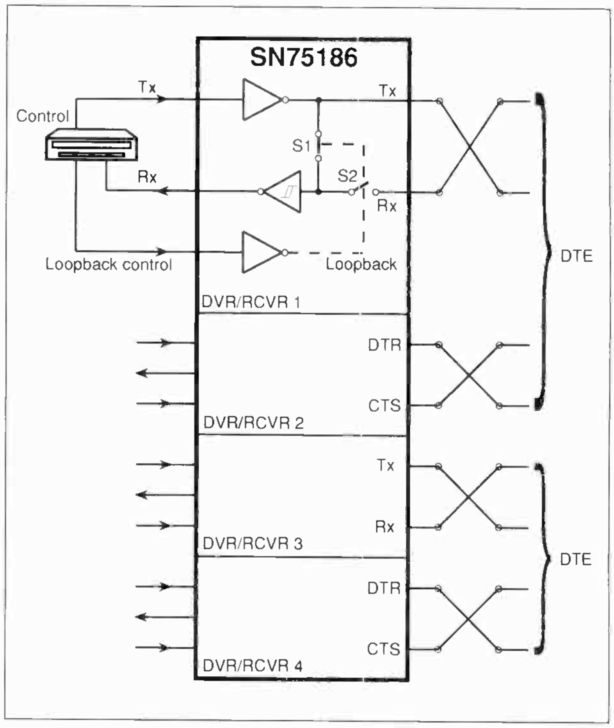


Fig. 6. SN75C185 incorporates a loop-back test facility, providing a powerful diagnostic test.

manufacturer. The *SN75C198/189* ICs are four line drivers and receivers offering unusually low dissipation when driving a fully loaded *RS232D* interface, while the *SN75186* is a really bomb-proof device with some extra very useful facilities. The *186* will withstand a short from a ground referenced + or –30V supply to any of its EIA *RS232* input or output pins, and furthermore has an ESD (electrostatic discharge rating) in excess of 4000V when tested per MIL-STD-833C (method 3015). Four transmitters and four receivers – all conforming to *V28* and *RS2323D* – 30V/µs driver slew-rate-control and preset 1µs receiver filtering are all included on chip.

The extra plus is loop-back control, permitting any receiver to be disconnected from the incoming line and patched to the TX output of its associated transmitter by a loop-back control-input pin. So fault-finding routines can be built in, using the intelligence available in an associated DTE (**Fig. 6**).

These Texas Instruments ICs can be used with voltages other than the usual + and –12V V_{dd} and V_{ss} supplies. For example, + and –5V can be used, permitting V_{dd} to be common linked with the +5V V_{cc} rail used to power the receivers. Of course, the TX outputs can not then quite meet the *RS232D* specified +5V to +15V and –5V to –15V space and mark level voltages. But at ±4.5V typical (±4V min) they come close. Indeed, this represents a very minor departure from the standard compared to some of the naughty (non-)implementations of RS232 that exist.

Some cut-price versions even dispense with the negative-going aspects entirely, relying on the fact that the receiver thresholds are both positive. ■

ACTIVE

Asics

Cmos 3μ prototyping. For several years, Mietec Alcatel has run a low-cost protoype service for 2μ cmos, using the multi-project method of processing several devices on one wafer. The method is now available for 40V and 100V bicmos devices, providing low cost since masks and fabrication are shared between several projects;low lead time; flexibility of design and manufacture in the same environment as for volume production. High-voltage bicmos gives 150gates/square mm; 18V cmos, 40V bipolar and 100V dmos; mixed analogue and digital circuits; and 320pF/mm^2 for the thin oxide capacitors. Mietec Alcatel, +33 146 32 53 86.

Fast 3V gate arrays. Gate delays of 0.21ns (about the time it takes a ray of light to travel 2.5 inches), are obtained in Toshiba's new sea-of-gates arrays, which use the dram-type 0.5micron cmos process. The *TC180G* series uses a 3.3V supply, the new standard, and consumes 65% less power than 5V types. 800,000 raw gates are available (560,000 usable gates) and the cell library is compatible with the earlier *TC163G* series of arrays. Orders are being taken from September 1992.

A-to-D & D-to-A converters

PCM audio D-to-A. A new member of Analog's Soundport family is the *AD1866*, a stereo 16-bit PCM audio D-to-A converter operating from one 5V supply and needing only a few externals. It has two independent references, output amplifiers and converters and DC bias pins position the output signal at 2.5V to eliminate the need for false-ground circuitry. Distortion plus noise at 990.5Hz is between 0.005% and 2% for inputs of 0dB to -60dB. Dynamic range is 90dB and channel separation 115dB. Analog Devices, 0932 253320.

Low-power A-to-Ds. Crystal Semiconductor have a new family of 1.5mW (50μW standby) 16-bit and 20-bit analogue-to-digital converters, *CS5505/6/7/8*, intended for use in low-frequency measurements or where low power consumption is needed. No integrating capacitors are needed, so the devices are suitable for intrinsically safe working. The delta-sigma oversampling technique is used to give better performance than found in V-to-F converters or the multi-slope integrating type. Special attention has been paid to line-frequency elimination. Sequoia Technology Ltd, 0734 311822.

Discrete active devices

Transient suppressor. *SA* series transient voltage suppressors protect equipment against spikes from 5V to 170V. These are glass passivated chip junction devices with a surge capability of 500W at 1μs and a response time from zero to minimum breakdown voltage of less than 1ps. Steady state power derating is 5W and operating temperature is -65 to 175°C. General Instrument (UK) Ltd, 0895 272911.

RF power transistors. Philips's *BLV101A* and *B* are chip transistors with input and output matching networks for operation at 800-900MHz and 900-960MHz respectively. Both are high-gain n-p-n types delivering 50W at 960MHz and at over 50% efficiency. Power gain for the A version is 8.5dB minimum at 900MHz and 7.5dB at 960MHz for the B. Collector/emitter rating is 26V. Philips Semiconductors Ltd, 071 436 4144.

Beefy transistor. Zetex has a new version of the Super E-line transistor, the *ZTX688*, which has a saturation voltage of 0.35V maximum at 3A and a minimum gain of 400; at 0.1A, saturation voltage is 0.04V – up to four times lower than a darlington. Peak current is 10A, at which gain is 100, while power dissipation is 1.5W free-standing. Transition frequency is 150MHz. Zetex plc, 061 627 4963.

Linear integrated circuits

Temperature sensor. Seiko's *S-8100B* cmos temperature sensor comprises the sensor, a constant-current circuit and an op-amp, all on the same chip, to give a linear output voltage of –8mV/K. Operating voltage is 3V-5.5V, repeatability ±0.3% and temperature range -40 to 100°C. Linearity is claimed to be much better than in other types such as thermistors. Amega Electronics Ltd, 0256 843166.

VCOs. Fujitsu's *D300* series of voltage-controlled oscillators are meant for use in satellite receivers, CD players and digital audio tape machines. The oscillators conform to EIAJ standards and use a single lithium tantalate crystal, which offers a frequency variability of 0.1% and 100 times better stability than LC or TTL IC VCOs. Fundamental oscillation frequency lies in the 4-30MHz range, three sampling frequencies of 32kHz, 44.1kHz and 48kHz being selectable by cmos logic levels. Fujitsu Microelectronics Ltd, 0628 76100.

Video amplifier. Linear's LT1227 current-feedback video amplifier has a 140MHz bandwidth, diff gain of 0.01% and diff. phase of 0.01°. Output current is 30mA. With a supply voltage range of ±2V to ±15V at 10mA, slew rate is 1100V/μs. A shutdown pin switches the amplifier into a high-impedance mode with a supply current of less than 200μA, which allows several devices to be parallel connected and selected by a logic level in 4μs. Linear Technology (UK) Ltd, 0276 677676.

Tunable LP filters. Maxim's *MAX291/2/5/6* are eighth-order, switched-capacitor low-pass filters, which are tuned by the frequency of the clock. The 291 and 295 exhibit a Butterworth profile and the other two a Bessel type. Ratio between corner frequency and clock is 100:1 for the *291/2* and 50:1 for the *295/6*, so that tuning ranges of 0.1Hz-25kHz and 0.1Hz-50kHz are available. Alternatively, an external clock can be used, for example for a swept characteristic. An inverting op-amp is provided for use as a low-pass post or anti-alias filter. Maxim Integrated Products Ltd, 0734 845255

Frequency generators. All the many clock frequencies needed on a large motherboard can be supplied by an Avasem frequency generator IC. A reference frequency drives PLL circuitry, the division ratios being stored in rom, so that different frequencies are derived from the same reference. The range includes a device with seven clock frequencies for VGA displays and LCDs and motherboard type with four clock generators and eleven output clocks, selected from mask-programmed frequencies. Microelectronics Technology, 0844 278781.

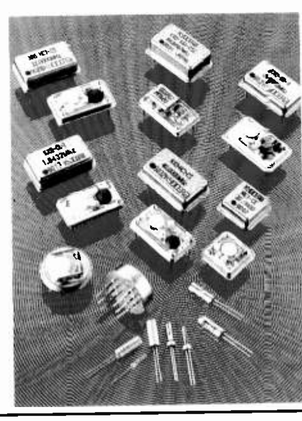
Small voltage reference. New voltage references from National Semiconductor, the *LM4040* family, are accurate to within 0.1% and come in the SOT-23 pack. Curvature correction provides an output voltage drift of around 20ppm/degC over the full –40°C to 85°C operating range and output noise is about 35μV RMS. No external stabilising capacitor is needed. Outputs in the family are 2.5V, 4.096V, 5V, 8.192V and 10V. National Semiconductor, 0793 697 428.

Frequency synthesiser. *UMA1014T* from Philips is a low-power synthesiser meant for use in cellphones, pagers and the like and forms part of the new chipset for mobiles. It includes prescalers and programmable dividers, with a view to avoiding the problems of interfacing with external circuitry: the phase/frequency comparator is on-chip. Comparator output settles rapidly and needs very little filtering before the VCO and, since charge-pump current is stable, few external components are needed. Active and powered-down current requirements are 13mA and 2.5mA. Philips Semiconductors Ltd, 071 436 4144.

Logic building blocks

Fast, dense fifo. Running at 40MHz, the *Am7205A* cmos first-in-first-out memory is claimed to be the only 8K by 9 fifo with an access time of 15ns. It also, AMD says, has the lowest operating current in the industry and provides empty, half-full and full flags. Advanced Micro Devices UK Ltd, 0483 740440.

35V LCD drivers. *HI8010/20/40* from Holt Integrated Circuits are cmos display drivers which drive dichroic and twisted-nematic LCDs and vacuum fluorescent displays of up to 35V at 2MHz. They are cmos and



Oscillators. Four new clock oscillators are on offer by AVX. *HC1* is a cmos device compatible with cmos or TTL circuitry and with an enable/disable pin; *EH* is designed to withstand mechanical shock and offers a frequency accurate to within 100ppm from 0-70°C; *K680S* produces a direct drive for the Motorola *MC68040* microprocessor, for which it generates a stable symmetry with temperature; and *386-HC* is for use with the Intel *80386* microprocessor. AVX Ltd, 0252 336868.

TTL compatible and need only clock, data in and load inputs. *HI8010/20* drive up to 38 segments and the *HI8040* up to 85, the latter also having test inputs for display testing, optional negative display voltage converter and a fail-safe circuit. Britcomp Sales Ltd, 0372 377779.

Data comms controller. Providing transfer rates of up to 12Mb/s at 16.7MHz, the *HD64570* serial communications adaptor from Impulse carries out protocol processing for lan servers, gateways, multiplexers, PBXs and modems. Its two-channel,multi-protocol, serial comms interface supports a range of comms protocol modes, including asynchronous, byte synchronous and bit synchronous modes such as HDLC and SDLC. Fifo buffers in the interface are 32byte deep. Impulse Electronics, 0883 347011.

Rapid comparators. Single and dual comparators from Maxim, the *MAX905* and *MAX906*, offer a 2ns data-to-clock setup, are edge-triggered and ECL-compatible. Architecture is of the master/slave type for oscillation-free, 3mV resolution and propagation delay of 2ns for 500MHz clocking. Analogue and digital power lines are separate; requirement is either ±5V or one negative supply. The *MAX906* is the dual version. Maxim Integrated Products Ltd, 0734 845255.

3.3V logic. Semiconductor announces a range of 3.3V logic devices designed for a low noise signature. The Low Voltage Quiet (LVQ) devices are in cmos and consists of gates, multiplexers, flip-flops and octal transceivers, intended for battery-powered computing equipment. It is estimated that a typical notebook computer motherboard in LVQ will draw about 4W against the usual 8W. Devices are said to generate up to 20% less EMI than other 3V logic. National Semiconductor, 0793 697 428.

Microprocessors and controllers

200ns microcontroller. Single-cycle, single-word instruction times of 200ns and an i/o speed of up to 5MHz give the Microchip *PIC16C5X* device a speed of up to ten times that of other 8-bit microcontrollers. As an example, these units will generate high-speed PWM in software for motor control and can transmit and receive data at 1MHz. They are available with up to 80 by 80 ram and 2K by 12 eprom. Arizona Microchip Technology, 0628 850303.

Fast Zilogs. Speed increases for the Zilog *Z80180* and *Z80181* microprocessors are from 12.5MHz to 15MHz and from 10MHz to 12.5MHz respectively. *Z80180* is based on an enhanced *Z80* and includes memory management, two DMA controllers, two uarts, two 16-bit timer channels and an oscillator. *Z80181* is the *Z80180* with one channel of the *Z85C30 SCC*, two 8-bit parallel ports and a pair of memory-configurable ram and rom chip-select pins. Gothic Crellon Ltd, 0734 788878.

8-bit microcontroller. *K4* is a new member of the Motorola *MC68HC11* family of microcontrollers and is an eprom-based, high-speed, low-power type running at up to 4MHz. It has power-saving stop and wait modes, 24Kbyte of eprom, 640byte of eeprom and 768byte of ram. 512Kbyte of memory is available by means of memory-mapping logic on-chip. *K4* comes in either eeprom or one-time-programmable form. Macro Group, 0628 604383.

Mixed-signal ICs.

Analogue multiplexer. 12-bit settling times of 17ns to within 0.1% and an adjustable noise bandwidth make the *CLC532* 2:1 analogue multiplexer from Joseph suitable for use in IR imaging, CCD, HDTV and radar application. Channel isolation is better than 80dB at 10MHz and harmonic suppression 80dBc at 5MHz. Other features include a noise level of 32μV RMS from 0 to 100MHz, diff. gain and phase of 0.01° and 0.05% and a slew rate of 130V/μs. Joseph Electronics Ltd, 021 643 6999.

ADPCM codec. Motorola's *MC145540* adaptive differential pulse-code modulated codec is now available and is meant for digital cordless telephone use in which it offers a 2.7V-5.25V supply range and 65mW dissipation at 3V. The device encodes analogue signals to digital ADPCM form at bit rates of 32, 24 or 16kb/s or to PCM at 64kb/s, simultaneously decoding digital code back to analogue. An evaluation board, the *MC145537EVK*, is also available. Motorola Ltd, 0908 614614.

Programmable logic arrays

85MHz FPGA. Actel's *A1225-1* is a 2500-gate field-programmable gate array with a 75MHz system speed and enables the design of 16-bit counters working at 85MHz. It is claimed to be the fastest 2500-gate FPGA available and can be designed and programmed by the Actel Action Logic system (new version available). Actel Europe Ltd, 0256 29209.

Power semiconductors

Frugal DC converter. For application where 50mA at 5V is needed, Linear's *LTC1046* replaces *ICL7660* ICs pin-for-pin, using only 300μA of supply current. Output impedance is one third that of the *ICL7660* and output drive is 2.5 times greater. Supply voltage is 1.5V-6V and there is a boost pin to allow a higher conversion frequency. Power conversion is 95% efficient. Linear Technology (UK) Ltd, 0276 677676.

Step-up converters. MAX731/2/3/5 form a new series of current-mode PWM step-*up converters* which are meant for small and 80%-95% efficient power supplies. Inputs are between 2V and 4V, outputs either 125mA or 200mA at 5V, 12V, 15V or adjustable from 2.7V to 15.75V. All have a logic-compatible shutdown pin that reduces quiescent current to 6μA. PWM pulse-width current-mode operation is at 170kHz. Maxim Integrated Products Ltd, 0734 845255

Passive components

Video filters. Range of RF and video filters from Active Labs in dil and sil packages are phase and amplitude equalised, with high attenuation in the stop band. Sin*x*/*x* correction for D-to-A processing is incorporated. This range is for low-pass filtering, but other configurations are available. The company provides a specification chart for ease of ordering. Active Electronic Labs, Ltd, 0926 484050.

SM resistor network. 20-pin, surface-mounting resistor network from Bourns is meant to provide balanced IC terminations or improved damping when used with memories and comes in isolated-resistor, bussed-resistor or dual-termination forms. The *4820P* is in EIA SOGN-0002 pack and resistance range is from 10Ω to 1MΩ. Bourns Electronics Ltd, 0276 692392.

Sealed rotary switch. Rotary switches in the Grayhill series *50/51* feature a range of throw angles in one device, the choice being 35°, 45°, 60° or 90° in the series *50* and 30° in series *51*. They are 0.5in in diameter and are completely sealed, with shaft grounding to assist shielding. Four poles are available on each deck, with up to 12 positions per switch. Highland Electronics Ltd, 0444 245021.

Miniature chip Cs. Murata's range of chip capacitors now includes 200pF Class I and 33nF Class II components in the *0402* size and 750pF Class I and 220nF Class II types in the *0603* size. All have nickel-barrier terminations to prevent solder leaching. *0402* capacitors measure 1 by 0.5mm to give a mounting density of 70 per square centimetre, that for the *0603* size being 35. Working voltages are in the 16-50V range. Murata Electronics (UK) Ltd, 0252 811666.

Displays

Led lamps. China Semiconductor Corporation now offer a range of led lamps in addition to their led displays. There round types from 2mm to 10mm diameter and rectangular ones from 5mm by 1mm to 8mm by 8mm, with superbright and bi-colour types as well as the standards. CSC also provide a custom design service. Clere Electronics Ltd, 0635 298574.

Instrumentation

'Scope into spectrum analyser. By means of Thurlby-Thandar's *TSA250* adaptor, an ordinary oscilloscope becomes a spectrum analyser whose centre frequency is adjustable over the range 400kHz-250MHz and is digitally displayed. Scan width and rate can be adjusted over the range; amplitude range is -70dBm to 0dBm. B K Electronics, 0702 527572.

Real-time spectra. PC-hosted spectrum analyser by Bores displays data in time anf frequency domains, auto and cross-correlation and transfer function measurement, with sample rates to 50kHz on dual channels – 400kHz as an option. Stimuli for transfer function and frequency response measurement are generated in real time and include pure tones and flat random noise, synthesis and analysis being carried out simultaneously. System is capable of updating by development kits and associated software. Bores Signal Processing, 0483 740138.

EMI testing. Chase's EMI Signature Scope allows manufacturers to examine the noise output of their products. *ESS7500* is connected to a standard oscilloscope with a low-cost

Radio data modem. *RM1200* is a single-unit UHF FM synthesise transceiver, which incorporates a 1200b/s FFSK baseband modem. It operates in bands from 430MHz to 468MHz, putting out 500mW in half-duplex mode. Its serial data interface allows data interchange at clock speeds up to 1MHz and facilitates control functions such as channel, power level and signal strength indication. Radio Data Technology Ltd, 0376 501255.

line network to display the noise signature in the range 3kHz-30MHz. A broad-band field probe is also available. Up to fifteen limit lines can be set to give an alarm if they are exceeded. Chase EMC Ltd, 081 878 7747.

Lightweight FFT analyser. Diagnostic Instruments's *PL202* fast Fourier analyser offers a frequency up to 40MHz, 1Mbyte static ram and up to 80 times zoom; it will dump to a printer via *RS232* and stores data for review –and yet it weighs only 3kg. For acoustics, full and third-octave analysis with A weighting is avaiable; for transients, there is comprehensive triggering; in vibration, the integral spectrum process is used with directly connected accelerometers; and in machinery analysis, orbital plots are standard. Chase Electronics Ltd, 081-878 7747.

Windows oscilloscope. In conjunction with a PC running *Windows 3*, the Nicolet Multipro is a multi-channel waveform analyser, with its display on the PC screen. Triggering has received much attention, since it is often necessary to record once-only and highly expensive events and a missed or false trigger would be a catastrophe. The *Windows* data is portable to other programs such as spreadsheets, word processors and the Nicolet *Famos*, which is a set of waveform-processing utilities. Memory length is 3Mwords/channel for occasions when event timing is indeterminate. Systems range from a seven-slot tower to a 500-channel rack. Nicolet Instruments Ltd, 0926 494111.

RCL meter. In less than one second, the Philips *PM6303A* resistance/capacitance/inductance meter indicates the value of the component to within 0.25% and provides the component dimension and one of seven equivalent circuit diagrams. If the component is totally unknown, a "green" button gives an immediate display of dominant value (R,C or L) with no need for further setting up. *PM6303A* offers readings of series and parallel *R, Z, C, L*, dissipation, *Q* and *C* of electrolytics under DC bias. A trim key compensates for strays in various test adaptors, which include a surface-mount type. Philips Test & Measurement, 0923 240511.

Interfaces

Digital pots. Optical encoders are used in the DP 16 digital "potentiometer" to give an output of 16 two-phase pulses per revolution, or 64 binary code changes. Devices in the range offer from 50 to 2048 pulses/rev, or 200-8192 changes. Applications are seen in manual data input to computers or in digital feedback from servos. Control Transducers, 0234 217704.

VGA/PAL converter. *VGAPAL* from Research Development Application Ltd converts the output from a VGA graphics card into pal video in real time, for viewing or recording on video tape. It is a simple add-on and does not interfere with the PC's graphics functions. The card plugs into any spare slot and needs no setting changes to the graphics card, being connected between the graphics card output socket and the monitor plug by means of a special plug provided with *VGAPAL*. RDA Ltd, 0495 224098.

Waveform monitor/vectorscope. Model *5783* from Thurlby-Thandar is virtually the same as the *5871*, but has the phase reference facility deleted for those people who use only one signal source. Colour television vector and waveform displays are seen either alternately or simultaneously on the 16kV PDA tube. Line-selector function can be used with vertical interval test signal, v. interval reference, Teltext and insert test signal, up to nine line numbers and fields being stored in memory. Thurlby-Thandar Ltd, 0480 412451.

Literature

Semiconductor database. Data Business Publishing have produced a PC AT database which identifies components and gives the manufacturer, local sales offices and distributors. The details of over 400,000 active devices from more than 500 makers include maker, address and telephone number, part number and key, description, availability and how to find the operating data in the library. This "low-cost" database, ISD, costs £249 plus vat and comes on 3.5in or 5.25in floppies for installation on a hard disk or in a Novell network. HTI Ltd, 0277 375000.

Bus driving. Three new application notes from NI discuss new features in the *IEEE-488.2* driver software (*340056-01*), sharing local ram with the VXIbus (*340059-01*) and using NI-VXI software to configure and program a VMEbus system (*340060-01*). All notes are free. National Instruments UK, 0635 523545.

Materials

Conductive foil tape. *Cho-mask II* tape for anti-EMI measures comes with a peel-off paint mask. A 0.07mm tin-plated copper foil has a conductive, pressure-sensitive adhesive on one side and a 0.076mm nylon paint mask on the other for ease of use in EMI gaskets or earthing, the mask being removed after paint or bake cycles. Used with Monel mesh, shielding performance is better than 100dB at 1GHz. It comes in rolls or in die-cut form. Chomerics (UK) Ltd, 0628 486030.

Production equipment

Water-washable solder cream. Series *400* creams from ESP for use on ceramic or epoxy glass boards leave residues that are easily removable in water, eliminating the costs of solvents and their reclamation. They are equivalent in performance to standard RMA fluxes. The creams can be dispensed, screened or stencilled and they do not slump, so that they are particularly suitable for fine-pitch use. Moisture resistance, eight hours of screen life, thermal stability, a 48-hour tack time and storage life of 12 months are offered. ESP, 0234 211582.

Power supplies

Boxed power. Three ranges of general-purpose power supplies from Davtrend are meant for soak testing, battery simulation and goods-inward testing. *DL* types are of the linear variety providing stabilisation and regulation of ±0.1% and ±0.5%; *DS* units are secondary switchers and there are also unregulated versions. Davtrend Ltd, 0705 372004.

Four-output, 150W SMPS. Power General's *FLU4-150* series of open-frame switchers are contained in a 4 by 9.5 by 2in area of board. Each model has a +5V output and there is a choice of 5V, 12V, 15V or 24V for the other three, all of them with a zero minimum load. Inputs between 90 and 265V AC are automatically accepted, as are those between 100 and 370V DC. Line filtering eliminates conducted noise and MTBF is 165,000 hours. Stabilisation is 0.3% for the 5V output and 0.5% for the others; regulation is 1%. Dowty Power Electronics, 0722 413060.

30W DC converters. *3000LP* series DC-to-DC converters, intended by Conversion Devices for OEM use, are contained in a 0.375in high package for 0.5in board mounting.There are single, dual and triple outputs, working over a 2:1 input voltage range, all with pi-type input filters and input/output isolation. All six sides are continuously shielded. Devices can be paralleled for more power or connected in master/slave configuration for increased input voltage. Outputs are 5, 12 and 15V DC; ±12, ±15V DC and 5; and 5,±12V DC or 5,±15V DC. Eurosource Electronics Ltd, 081 977 1105.

Radio communications products

Saw filters. Kinseki is a Japanese company, new to the UK, which manufactures quartz crystal devices. Recently, saw filters have been introduced in versions for pagers and general telecomms work, types for the Global System Mobile Phone (GSM) system now being in development. Kinseki (UK) Ltd. 0454 614638.

Radio data network. RDI have introduced *Versanet*, which it says is the first deregulated radio data network to use a frequency-agile system to avoid interference automatically, listening to the permitted channels and selecting a clear one. VersaNet includes an *RS232* serial data highway port to exchange data with PCs or PLC equipment. Radio Data Technology Ltd, 0376 501255.

Transducers and sensors

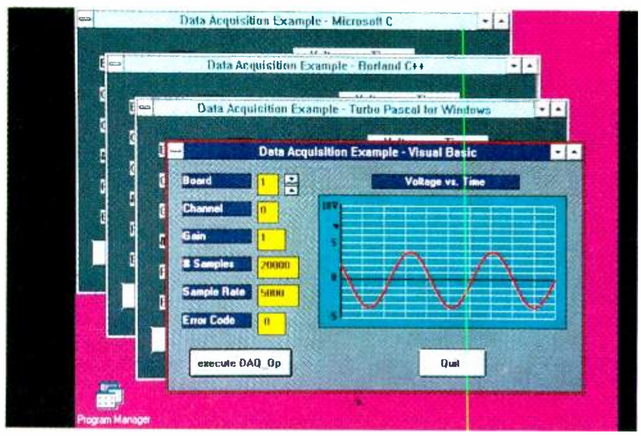
Load-measuring washer. Load washer Model *LW* from Control Transducers measures bolt stresses to determine overloads and to ensure clamping forces. Capacities are from 100kg to 100,000kg in sizes from 25mm diameter and 9mm thick to 76mm and 32mm. A domed load button and load base are supplied as standard and spherical washers for use on uneven surfaces or in the case of misalignment are optional. Temperature range is up to 200°C; repeatability, non-linearity and hysteresis are all 0.15% of full scale. Control Transducers, 0234 217704.

Proximity detectors. A range of

proximity detectors by Crouzet, the *V3* series, will cope with both metallic and non-metallic substances. They work normally, in that the approach of a metallic object activates the *V3*, but the addition of a metal lever enables the detector to react to the touch of a non-metallic object, becoming in effect a non-mechanical limit switch without the contacts. A led indicates switch status; switching capability is 200mA continuous. Crouzet Ltd, 0252 513211.

Accelerometer. Weighing less than 1g, Endevco's model *7264A* piezoresistive accelerometer uses a silicon microsensor in full Wheatstone bridge form with fixed R_s for calibration. Full-scale range is 2000g, at which output is 400mV with 10V DC supply. Resonant frequency is 65kHz and measurement frequency range is 0 to 13kHz. Endevco UK Ltd, 0763 261311.

Proximity sensor. *IP67* inductive proximity sensors from EuroSensor offer a reproducibility of 10μ, come in p-n-p and n-p-n forms and indicate activity by a led. They measure 4mm in diameter by 26mm, accept between 6V and 35V DC supply and draw less than 5mA when idling. Kynmore Engineering Co. Ltd, 071 405 6060.



COMPUTER

Computer board level products

Frame grabber. Amplicon's *VDIGI* frame grabber board plugs into a PC XT/AT to provide real-time video signal capture and storage. It includes a 64K frame buffer and 4-bit TTL i/o for external control and monitoring. Resolution is 256 by 256 by 7bit and there is internal/external sync., horizontal and vertical sync output and a low pan filter for noise and colour. Operation is interactive by menu, including setup and lighting conditions and output is in PCX or TIF file form. Amplicon Liveline Ltd, (Free)0800 525 335.

Open local bus. *Scim* is an open-architecture local bus by Arcom, which offers lower-cost, yet powerful expansion for industrial computing. Choice of modules includes those for VMEbus, STEbus and PCbus host carrier boards. The bus accommodates 16 data and 24 address lines, four interrupts, DMA and serial lines. Two connectors are used for data and address, with STEbus and PCbus in mind, but dual connectors can be used for 16-bit transfers. In the range of modules are analogue input and output, *RS232* serial i/o, *RS485* serial i/o, 40-line programmable digital i/o, Ethernet interface, flash rom/ram, comms and VGA/EGA/CGA graphics. Arcom Control Systems Ltd, 0223 411200.

Eight-i/o PC card. Data acquisition and control card for PC ATs will hold up to eight different input/output modules, so enabling choice of the required channels on one card and taking up fewer expansion slots in the PC. Modules already available include multi-channel analogue, digital and comms versions. Intek Electronics Ltd, 0352 85603.

S-B computer for logging. Logicom's single-board computer is based on the Siemens *SAB80C535* microcontroller and in meant for OEM use in data logging, monitoring and control. It offers eight extended-resolution analogue inputs, 16 digital i/o lines and an *RS232* port. There is 32K of battery-backed ram, 64K of eprom, a watchdog and Power supply supervisor. Programming is in C, Basic or assembler. Logicom Communications Ltd, 081 756 1284.

Analogue output. Two analogue output boards for the PC AT have either six (AT-AO-6) or 10 (AT-AO-10) high-speed multiplying *DAC82222* digital-to-analogue converters. Each channel on these NI boards has 4-20mA output and a bipolar or unipolar voltage output. DMA capability allows operation at conversion rates up to 200kHz and there is an 8-bit DIO port for additional control. For programming, there is NI-daq dos and NI-daq Windows driver software and LabWindows software development, the software being free with each board. Boards will be available from December 1992. National Instruments UK, 0635 523545.

Data acquisition. *AT-DSP2200* from NI is a DSP accelerator board for the PC AT, delta-sigma modulating A-to-D and D-to-A converters. It performs scientific calculation faster than the PC's *80X86*. *AT-A2150* is a further plug-in board to provide four channels of audio-frequency analogue input with low noise and low differential non-linearity. National Instruments UK, 0635 523545.

Development and evaluation

Low-cost ICE. Nice 51 is claimed to be the cheapest *8051* hardware in-circuit emulator available. This new ICE from Comsol has the ability to substitute emulated for target memory and to stop execution on a combination of internal and external events while running at speed. The PC program allows memory, registers and SFRs to be displayed and modified and it will assemble code changes to allow mods to be tested. Execution speed is 12MHz. Computer Solutions Ltd, 0932 352744.

Programmer. *Softy-Four* is Dataman's new programmer, designed to cope with eproms, eeproms and flash eproms. *S4* has large nicad batteries and will program up to 1000 proms on a one-hour charge, although its lithium battery backup preserves data even when the nicads run down. Built-in memory emulation allows the development and debugging of microsystems. 1Mb of user memory, upgradeable to 4Mb. Dataman, 0300 20719.

Eprom programmers. Hilo eprom/eeprom programmers by Nohau will download a 4Mbit file in a few seconds and program eight 27256 eproms in 20s. An interface card in the PC shares the PC's CPU, memory, i/o, keyboard, display and disk to achieve the speed. Eproms of up to 8Mbit can be programmed. Software includes a hex-to-binary converter, 2 or 4-way binary file splitter and "dump file to console". Nohau (UK) Ltd, 0962 733140.

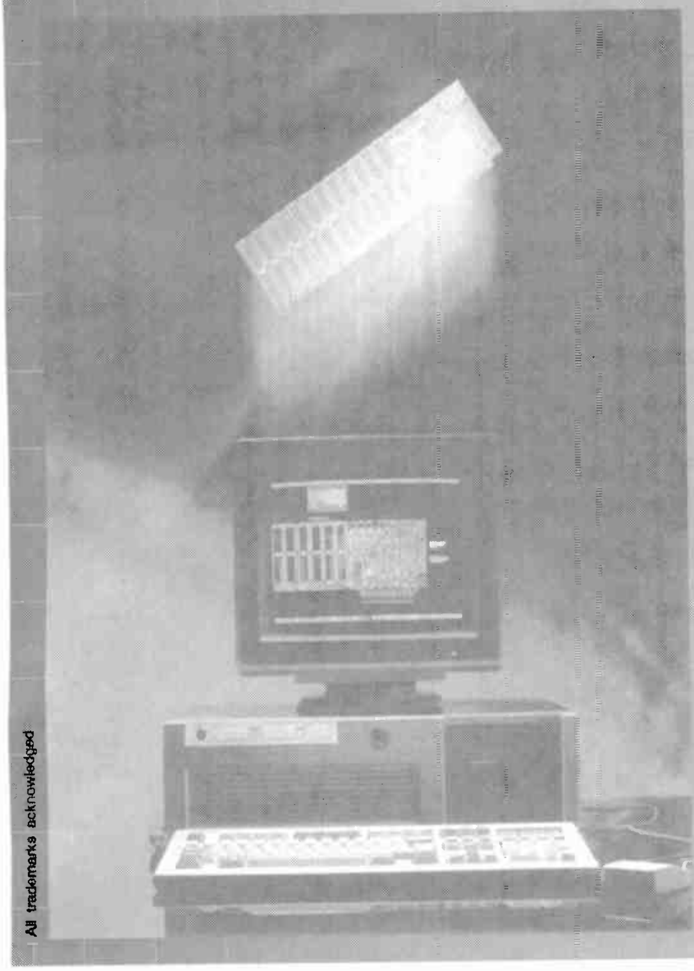
Transputer kits. *Transkits* from Sunnyside contain hardware and software needed to familiarise engineers with the use of transputers by turning their PCs into "virtual instruments" – an oscilloscope and a spectrum analyser. *TransKit 500* is the first, consisting of a two-channel, 16-bit A-to-D transputer module (tram), a two-channel D-to-A tram and a compute tram mounted on a single-slot AT card. Accompanying software turns the PC into a combined dual-channel digital storage oscilloscope and function generator. An enhanced version has C source code of the system software, a C compiler and debugger. Sunnyside Systems Ltd, 0506 460345.

Software

Abel 4.1. Version 4.1 of Data I/O's Abel programmable-logic design tool allows the compilation and simulation of larger PLD designs by means of dos extended memory and now supports Intel's *85C22V10*, the Lattice *GAL6002*, Atmel's *ATV5000* and other devices by Cypress, Ricoh and Toshiba. Abel-FPGA is also announced in its 4.1 version. Data I/O Ltd, 0734 440011.

Gate array programming. Actel have made the route to field-programmable gate arrays easier by introducing an entry-level Action Logic System, which is a combined software/hardware kit including Viewlogic schematic capture, Viewlogic/Orcad interface libraries, validation, place-and-route and timing analysis. The hardware is an Activator 1 programmer with sockets for *68PLCC*, *84PLCC* and *84PGA*. The kit is for Actel *Act1* logic, but is upgradeable to *Act2* and *Act3*. MMd Ltd, 0734 313232.

PC graphics editor. Integrated Circuit Editor is a PC AT/XT-based graphics editor for IC layout, featuring fast refresh, auto-open and nested view commands, input and output stream (Calma-*GDS II*) and CIF files, as well as definable commands and technology files. Compatible with most plotters, laser and dot-matrix printers and will handle polygons up to circles with text for annotation. Silicon Microsystems Ltd, 0666 824844. ■



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Hameg HM605 60MHz O'Scope £400.
Hitachi V212 20MHz O'scope £230.
Hitachi V202F 20MHz O'scope Calto 1-92 £230.
Hitachi V509 50MHz O'Scope £400.
Tektronix 455 O'scope £350.
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CIRCLE NO. 137 ON REPLY CARD

Two mic-amp tips

This electret microphone preamplifier is of fairly standard form, but contains input and output arrangements of particular interest.

As well as giving an on/off indication, the led in the input provides bias for the electret module, since led forward voltage is essentially constant; the 4.7kΩ microphone load, selected experimentally, gives best output.

At the output, the 100Ω resistor in series, but inside the feedback loop of the stage, allows the use of long, capacitive cables.

D M Bridgen
Racal Mexico
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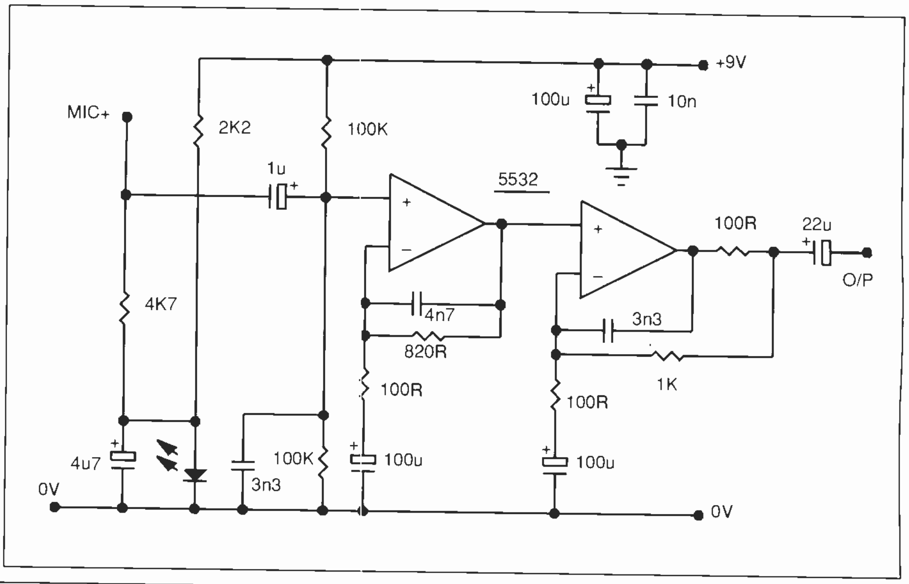
Mexico



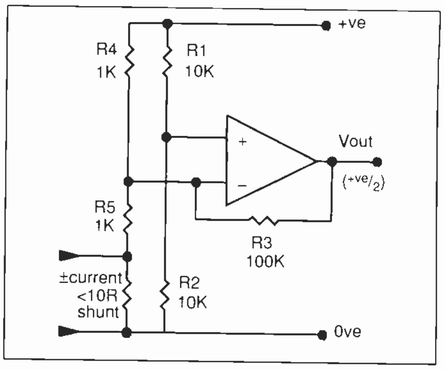
Led at the input and small resistor at the output of this electret microphone amplifier provide bias for the microphone module and drive for long cables.

Current-shunt amplifier for bipolar inputs

Operating from a single supply, this amplifier copes with both positive and negative low voltages derived from a high-current shunt.

Gain in the shunt feedback arrangement is set by $R_{5,6}$ and centre bias voltage by $R_{1,2}$. The current-shunt resistor is taken directly to ground where the voltage developed across it produces a current in R_5, which is amplified; no decoupling capacitor is needed. To balance the offset voltage caused by the shunt ground connection, a balance current flows through R_4 – which must be equal to R_5 – whatever gain is needed. With no input, the output voltage sits at half the supply voltage. An *OP07* op-amp has a low offset voltage and is particularly suitable for this design.

Norman Jones
Cobridge
Staffordshire



Voltages produced by both positive and negative direct and alternating currents flowing through the shunt are amplified by this single-supply circuit.

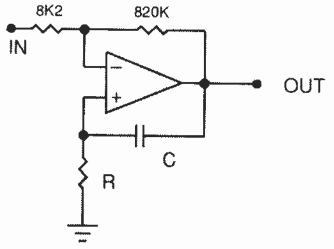
Positive-feedback op-amp booster

Since the gain/bandwidth product of an op-amp is a constant f_1, increasing closed-loop gain reduces its bandwidth and therefore rise time in direct proportion. This circuit reduces the effect by counteracting the increased voltage at the summing mode when the input frequency increases.

The effect is achieved by means of the simple CR circuit in a positive-feedback connection, which makes the circuit a second-order system with its complex pole pair higher than the first-order bandwith $G = f_1/B$. To avoid oscillation, the -3dB point of the CR must be greater than f_1.

The plots show the greatly improved rise time with $R = 470\Omega$ and $C = 150\text{pF}$; measured bandwidth is improved to 160kHz from 25.7kHz.

D Baert
Rijksuniversiteit Gent
Ghent Belgium



Judicious application of suitably shaped positive feedback improves bandwidth and rise time of an op-amp. Roll-off frequency of CR must exceed op-amp cut-off frequency for stability.

One-gate memory

Non-inverting gates – Ands, buffers, Ors – will make single-element memories, using one resistor.

In effect, the gates are made to latch by applying positive feedback via the resistor and forcing the input to either state by switches or logic levels. Resistor value is not critical, but is related to the response time.

Figure 1 shows the principle using a buffer and one input; in **Fig.2**, an And gate gives the same effect, but the two inputs are used as set and reset. Using a capacitor instead of the resistor produces curious monostable flip-flops.

D J Long
Brighouse
West Yorkshire

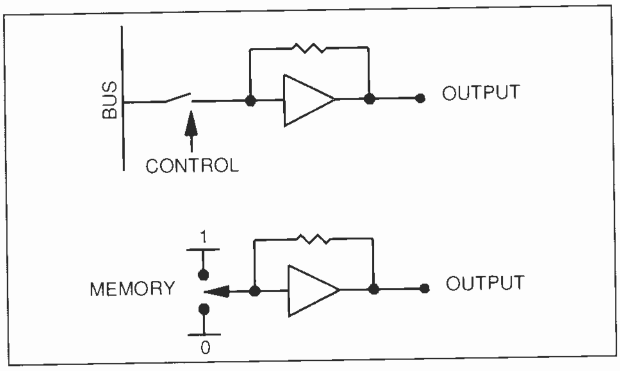


Fig.1. Making a buffer latch up produces a one-bit memory. Once its input is forced to one state, it will stay there.

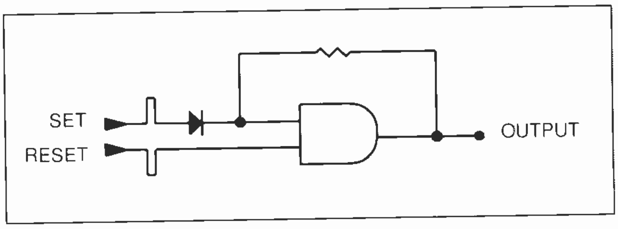


Fig.2. Using a two-input gate such as a Nand allows set and reset inputs. Diode isolates set input from further pulses until reset.

Latched oscillator

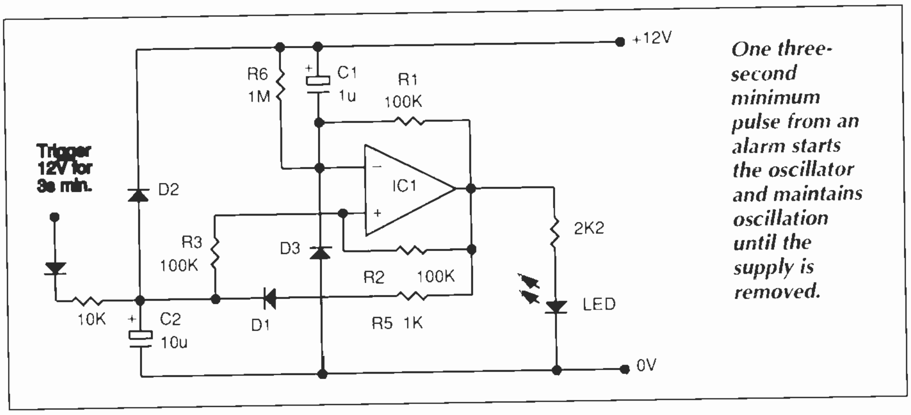
In an alarm system, an operation from which a three-second supply-voltage trigger pulse was available was required to flash a led – reset being by means of removing the supply voltage. I had available an *LM358N* op-amp, a type that allows inputs down to the negative rail, and combined an oscillator and latch using the single device.

Resistors $R_{1\text{-}4}$ and C_1 with the op-amp form a relaxation oscillator starting in the off condition when power is applied; R_5, D_1 and C_2 provide a latching action to maintain the alarm condition after the trigger pulse ends. In the inactive state, the voltage on the non-inverting input is lower than that on the inverting input and the oscillator is off. On receiving a trigger, C_2 goes to 12V, less a diode drop, and the oscillator starts; D_1 and R_5 keep the voltage on C_2 high after the trigger.

To avoid spurious triggers, R_6 keeps the inverting input above the non-inverting input in the standby condition. Diodes $D_{2,3}$ discharge $C_{1,2}$ when the supply is removed.

Time constant C_1R_1 must be much less than $R_{2\text{-}4}.C_2$ to eliminate the possibility of C_2 discharging during the low state to the point where the non-inverting input is always higher than the inverting input, stopping oscillation.

M J Brettle
Potton Marine Equipment
Gamlingay Bedfordshire



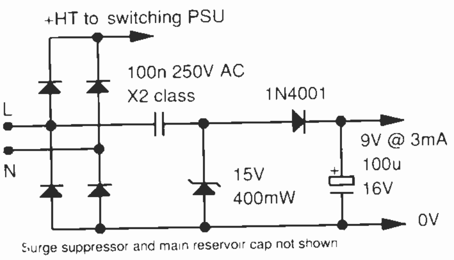
One three-second minimum pulse from an alarm starts the oscillator and maintains oscillation until the supply is removed.

Low-loss voltage dropper feeds S-M controller

Low power consumption switched-mode controllers can be fed from the rectified input, thereby avoiding the need for a separate transformer winding, but a simple dropper resistor wastes power. This circuit uses a capacitor and has minimal loss.

Its feed is taken across the SMPSU input bridge and gives a 9V, 3mA output, sufficient for low-power mos controllers driving a power mosfet. The circuit must only be used where there is no chance of a user gaining access to it, since it is live, and an isolation transformer should be used during test.

A M Wilkes
Brentwood
Essex



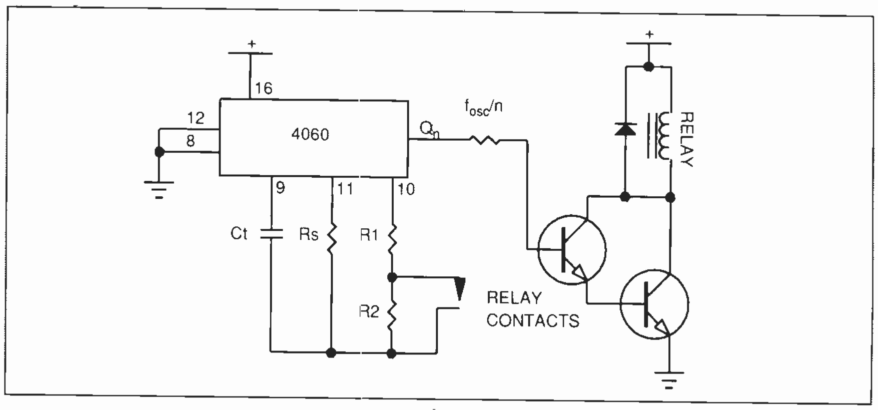
Low-loss voltage dropper replaces a resistor when powering low-consumption switched-mode power supply controllers from the rectified mains input.

Asymmetrical on/off for 4060

An internal oscillator and 14-stage ripple counter in the *4060* make a useful long-duration on/off timer, but with a possibly inconvenient symmetrical output duty cycle.

This circuit avoids any complication of additional circuitry by splitting the oscillator frequency-setting resistor and shorting on part of it by a relay driven by the output of the timer. Timing now becomes, with the relay on, $2.2CR_1 2^n$, and with it off, $2.2C(R_1+R_2)2^n$, n being the divider output driving the relay. You could use an analogue switch in place of the relay.

J V Sawant
Haffkine Institute
Bombay
India



Relay or analogue switch driven by a counter output allows asymmetrical on/off times in this long-duration timer.

Programmed Nand/Nor or And/Or gate

Using a pair of triple, two-channel multiplexer/demultiplexers, you can make a logic gate which is selected as an And/Or gate or a Nand/Nor under the control of two inputs.

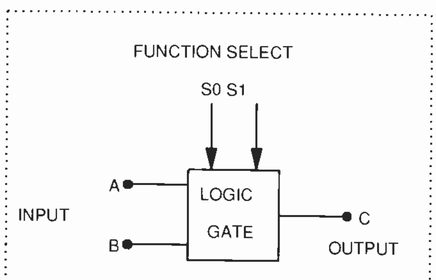
In **Fig.1**, the logic inputs are *A* and *B* and the function-select inputs S_1 and S_2, the four combinations of the two giving four logic functions. An advantage of this scheme is that the output impedance is low, being the on impedance of two analogue switches in series or less than 200Ω.

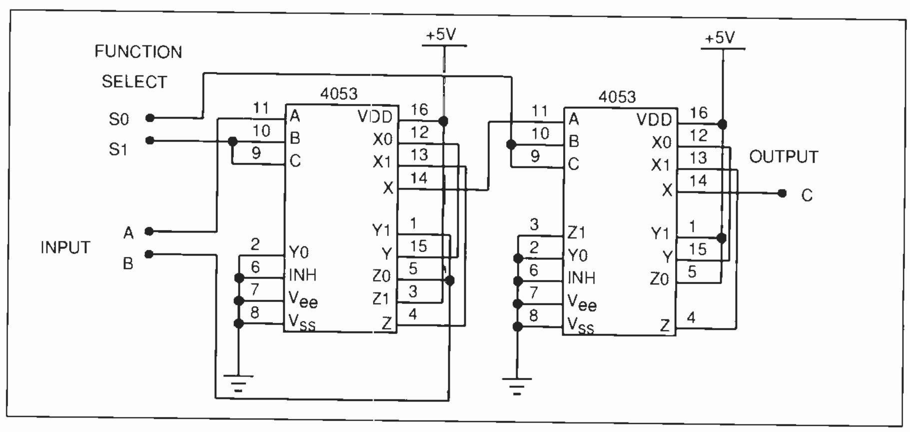
Figure 2, taken from a data sheet, shows the arrangement. When, for example, input *A* is low, S_1 is on; and when *A* is high, S_2 is on and so on.

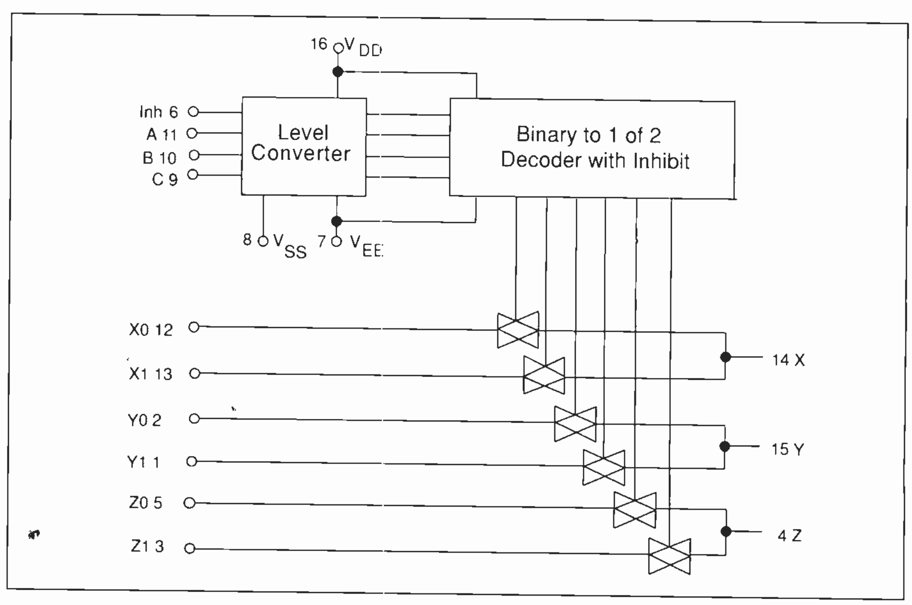
Emad Hamdoon Said
Baghdad
Iraq

Fig.1. Function-select inputs S_1 and S_2 configure the two 74HC4053s as an And, Or, Nand or Nor gate.

Fig.2. Internal block diagram of 74HC4053 multiplexer/demultiplexer.







Marconi in his steam yacht Elettra. In 1923 he sailed westward to test the range of shortwave transmissions

UNITING THE EMPIRE

Connecting Britain with its Empire by means of 1000 mile wireless links was an idea that had been put forward by the Marconi company as early as 1906. But the project did not take root until the Imperial Wireless Conference of 1911, following which Marconi was awarded a contract by the Post Office to supply a series of long-wave, high-power stations.

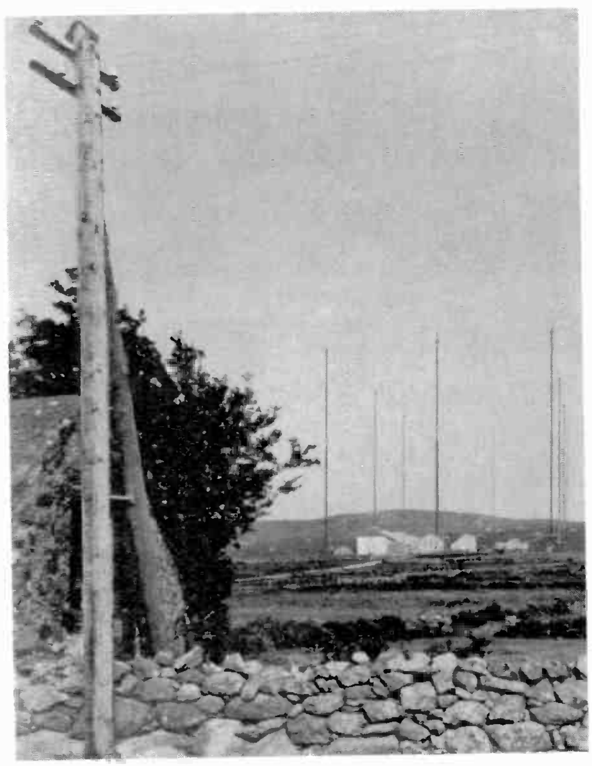
Unfortunately start of the work was severely delayed by a complicated political row (the so-called Marconi scandal, where members of the government were accused of favouritism and improper share dealing), and then cancelled due to outbreak of the first World War.

Following the war, work on a European network progressed, including the building, in 1921-2, of a transmission station at Ongar and a receiving station at Brentwood. These were linked to a central telegraph office, Radio House, in Wilson Street, London.

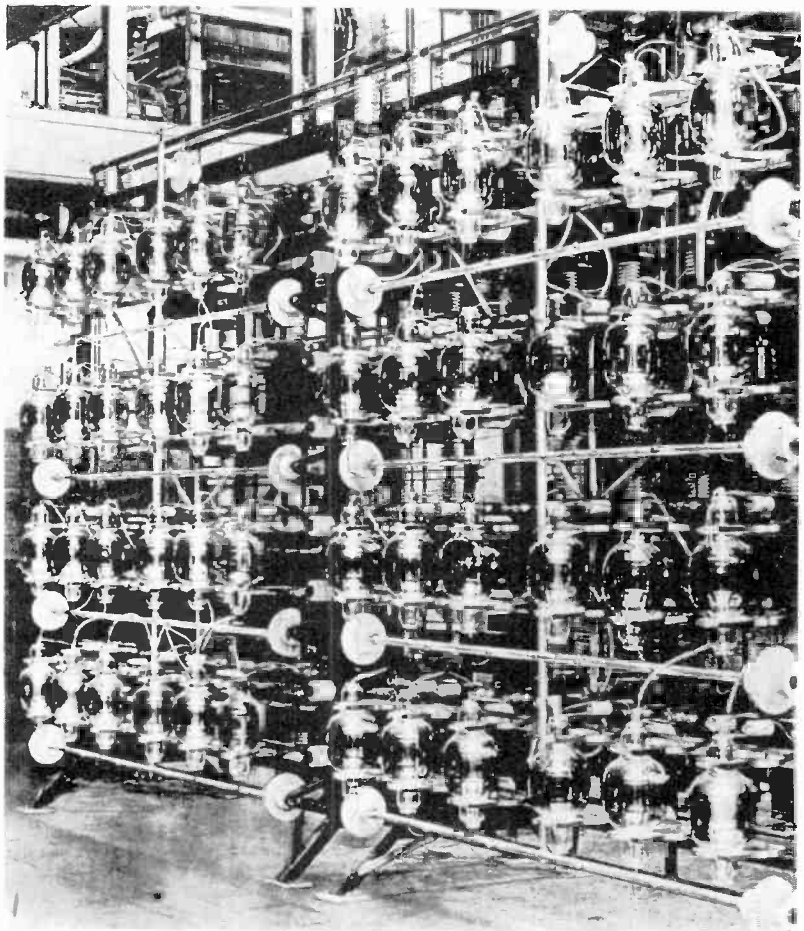
But the Imperial scheme was held up by continuing wrangles within the UK government and between it and those of the dominions. The Post Office embarked on a high-power station in Rugby, while Australia and South Africa commissioned stations from the Marconi company. But by 1924, a coherent plan of action had still not emerged.

Short wave experimentation

The one unquestioned assumption was that the chain would use long-wave frequencies. Longer wavelengths



Caernarvon station – high power transmissions to America.



The high-power transatlantic transmitting station at Caernarvon, was, with its companion receiving station at Towyn, commissioned before the 1914-18 war. In 1922 they took over traffic from Clifden, destroyed in the struggle for Irish home rule. Caernarvon had three transmitting systems in its time. First was a timed-spark disc, joined in 1920 by a 200kW Alexanderson high frequency alternator. A valve transmitter was added in 1921. It employed 56 air-cooled Marconi MT2 valves, powered by two or three direct-current generators in series, supplying up to 15,000V.

A contemporary account noted: "The constancy of frequency of the valve generator is very remarkable, being of an order altogether higher than that of the alternator, and no highly complicated means is necessary to ensure it."

A European transmitter at Ongar (with receiver at Brentwood) was opened in 1922, and also took over some transatlantic traffic. Together with Caernarvon they were operated by remote control over landlines from the newly-opened Radio House, the Central Telegraph Office in Wilson Street, London.

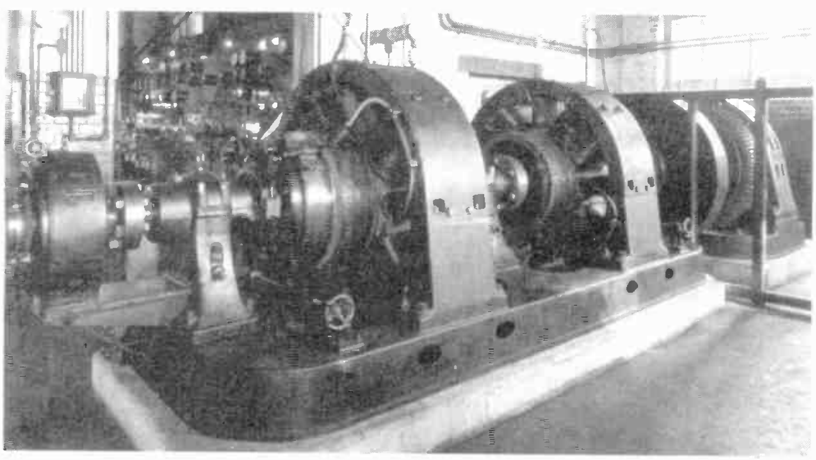
and higher powers were accepted as the recipe for covering longer distances. But since 1916, Marconi had been experimenting with shorter-wave transmissions, initially for naval signalling over line-of-sight distances. In 1917, he lost a £5 bet with one of his staff, CS Franklin, who succeeded in demonstrating, despite his employer's scepticism, a short wave (15m) link between London and Birmingham. Another Marconi man, HJ Round, noted freak long- distance reception of 100m signals.

Amateur radio enthusiasts, working post-war in sub-200m wavebands, were also finding that they could occasionally make transatlantic contact.

Marconi set up a shortwave transmitter at Poldhu in 1923 and, as in 1902, sailed westwards – this time in his steam yacht Elettra – to test reception. Ranges of 1400 miles were achieved in daylight, and signals received in New York after dark.

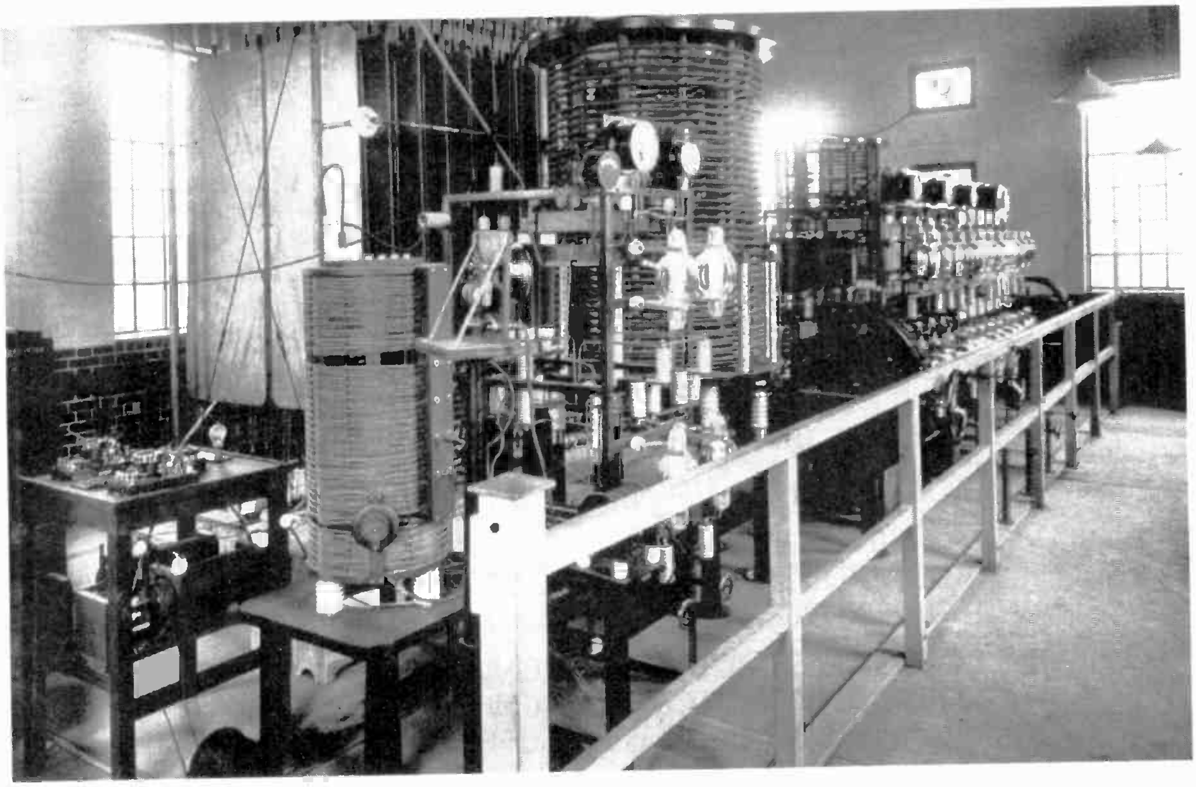
By May 30, 1924, following further experiments and improvements, the signal to

Caernarvon's 1921 valve panel – 56 air-cooled MT2 valves.



Up to three DC generators, in series, supplied 15,000V to the Caernarvon valve panel

The Brentwood receiving station, companion to Ongar.



One of the three European transmitting stations at Ongar, opened in 1923.

Sydney, on 92m, was so strong that Marconi was able to speak from Poldhu to Australia by wireless telephone. This presented the company with a dilemma: although successful in experiments, directional shortwave transmission was far from being a proven, marketable system. Contracts for British government was at last on the verge of reaching a decision on the Imperial scheme.

Yet the shortwave beam system's potential cost-benefits over longwave were enormous, requiring a fraction of the transmission power, so meaning smaller, cheaper stations and lower running costs. The company decided that to conceal the shortwave progress, while pressing ahead with costly longwave installations would be to break faith with its customers (and also, perhaps with its own technological integrity).

Australia and South Africa readily agreed to modification of the already- started stations, and, under pressure from the dominions, the British government reached a decision on July 2.

The Imperial Wireless Chain, with Marconi as contractor, would go ahead, and would use the short-wave beam system in a contract loaded with penalty clauses, though these proved unnecessary.

The expensive irony of C&W

Ironically, it was success of the system that was to cost the company most dearly. The wireless chain quickly attracted traffic from the cable links, being both three times as fast, in terms of words-per-minute (these were still the days of telegraphy) and cheaper to operate and maintain. Nevertheless cable had some advantages over shorter distances, and was regarded as a strategic defence necessity by the UK and Dominion governments.

The upshot, in 1929, was a government-induced merger – the creation of a new company which would buy-out the communications interests of the Marconi company and the cable companies. This was Cable and Wireless. In view of the weakness of the cable group's position, and the strength of Marconi's, it is odd that the voting rights in the new company were 56.25% to the cable group and only 43.75 to Marconi.

For the company, the merger marked the end of its involvement in transmitting messages as a business and a return to its origins as a research, invention and manufacturing operation. Marconi himself saw the beam system as the culmination of his ambitions – from experimental transmission of a few yards to a worldwide communications system in 30 years. ■

Central Telegraph Office at Radio House.

Simple, precision timer

Analogue and digital circuitry come together in the GEC Plessey *ZN1034* to generate time intervals from 16ms to hours, without the use of excessively large components. Repetition accuracy is within 0.01% and stability with temperature is 0.01%/°C.

Figure 1 shows its essentials; a precision oscillator with external RC timing components drives a 12-stage binary counter to give a 4096:1 division ratio. After either the trigger pin or the supply voltage changes state, 4095 cycles of the oscillator occur before the output pin sees a change — for 3MΩ and 10µF, that means a twenty-four-hour wait. And, of course, you can trim the timing resistor to obtain the exact time delay needed. GEC Plessey's Consumer IC handbook presents a great deal of information on the components in the timing circuit.

Figure 2 is the basic idea. You can get a variation of 1500:1 in time delay by choosing the timing components for that purpose, but it is pointed out that a more restrained range of 400:1 (1.5s-10m) gives better control linearity, ±2% instead of ±8%. Switched decades of resistance can be used in the R_T position and the note gives a table of correction factors and errors, with values of shunt resistor needed.

Starting the process going is a matter of either keeping the supply on and taking the trigger pin low or keeping the trigger low and switching on the supply; **Fig. 3** shows the process. Supply dropouts during operation cause an increase (supply initiated) or

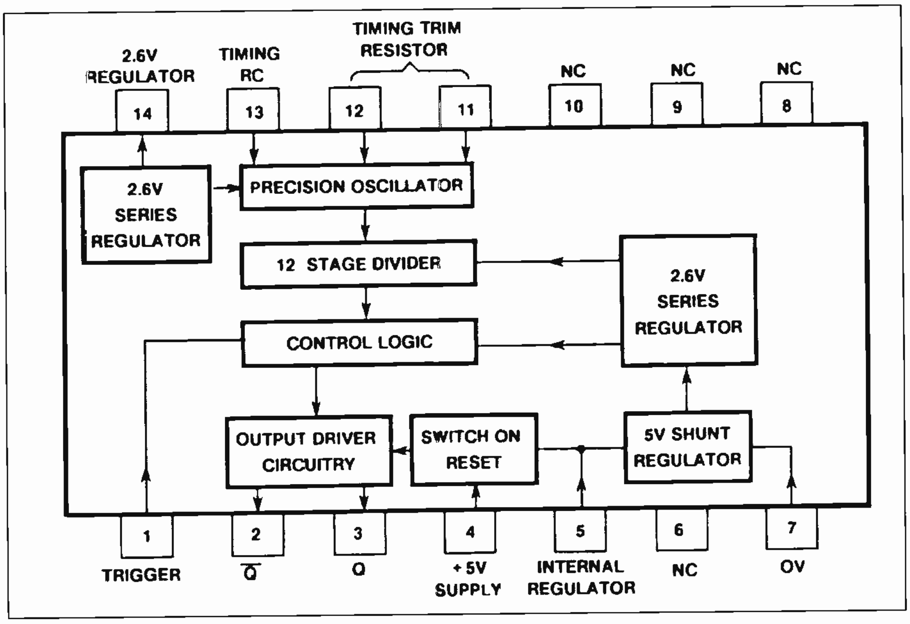


Fig. 1. GEC Plessey's ZN1034 precision counter/timer, which will generate an accurate time interval of up to many hours duration with relatively small timing components.

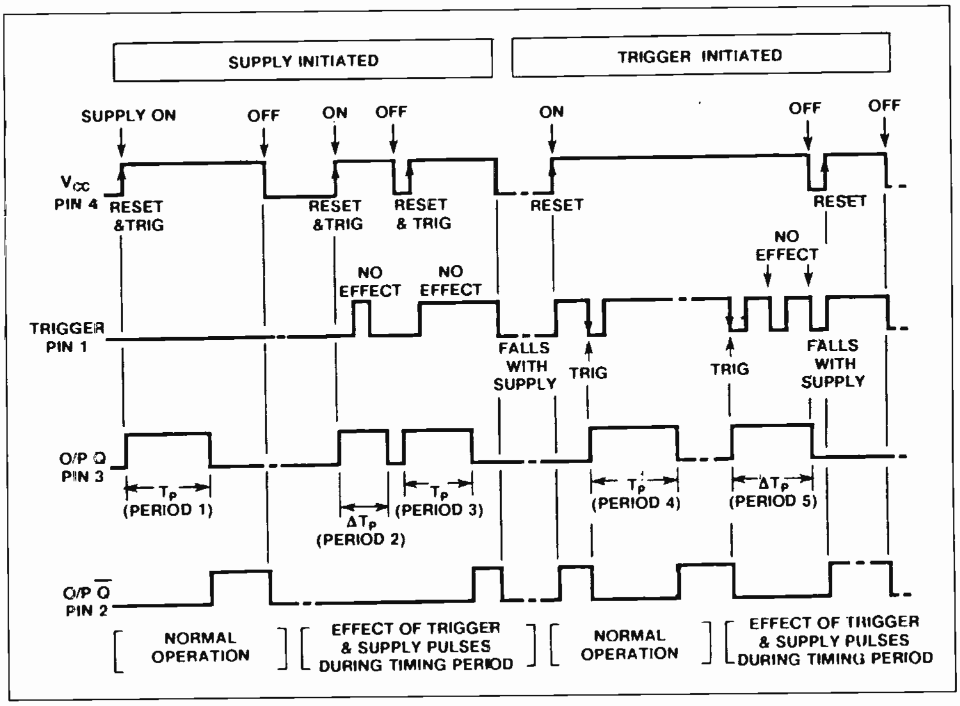


Fig. 3. Methods of setting the ball rolling. Initiation is either by trigger input or by switching the supply.

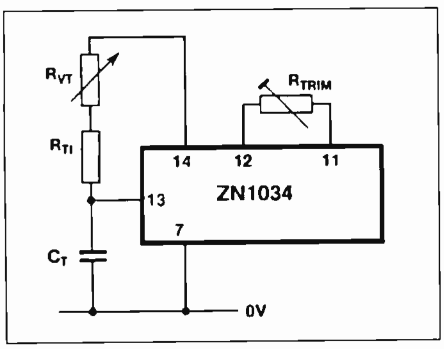


Fig. 2. Basic timing circuit using the ZN1034. Timing range is 1500:1, or 400:1 with a little better control linearity. Minimum delay is 16ms; maximum 24 hours.

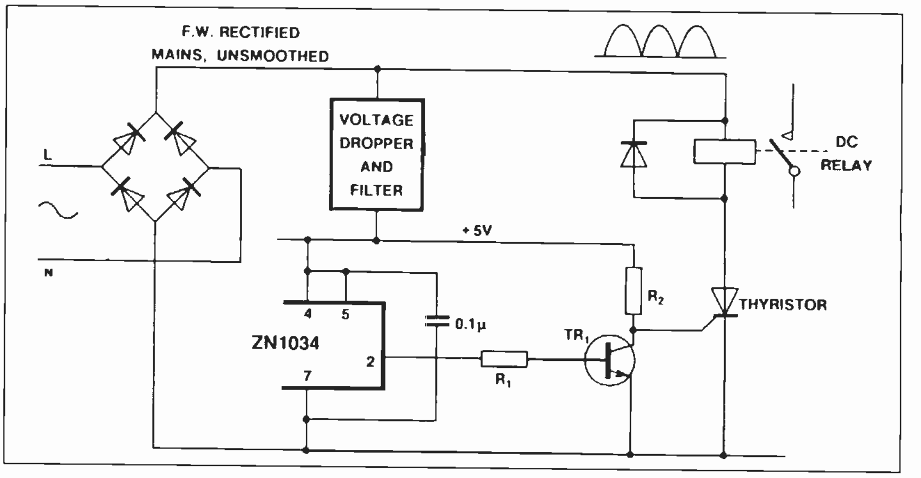


Fig. 4. Typical circuit for a delay-to-off using a thyristor and a DC relay. Pin 2 will supply up to 25mA, but R1 should be high enough to just saturate the transistor.

decrease (trigger initiated) in the time delay.

Figure 4 shows a typical application – a delay-to-off timer using a thyristor. For 240V mains, you might have to use a 100V DC relay with a dropper, 220V DC relays being thin on the ground.

A complete design for a mains delay-to-on plug-in timer is shown in **Fig. 5**, which also indicates methods of avoiding the effects of mains and EM noise spikes. The smoother R_1C_1 combines that function with spike reduction, further efforts in this direction being made by R_2C_2. A shunt regulator is built into the chip and also reduces mains noise – in the circuit shown it reduces the noise by 15000:1. Of course, a 5V supply designed to power logic as well as the *ZN1034* will not present much of a problem even without the regulator, since noise spikes should not be present. As regards EM noise, pin 13 must be screened and the note gives a recommended PCB layout for that purpose.

GEC Plessey Semiconductors, *Cheney Manor, Swindon, Wiltshire SN2 2QW. Telephone 0793 518000.*

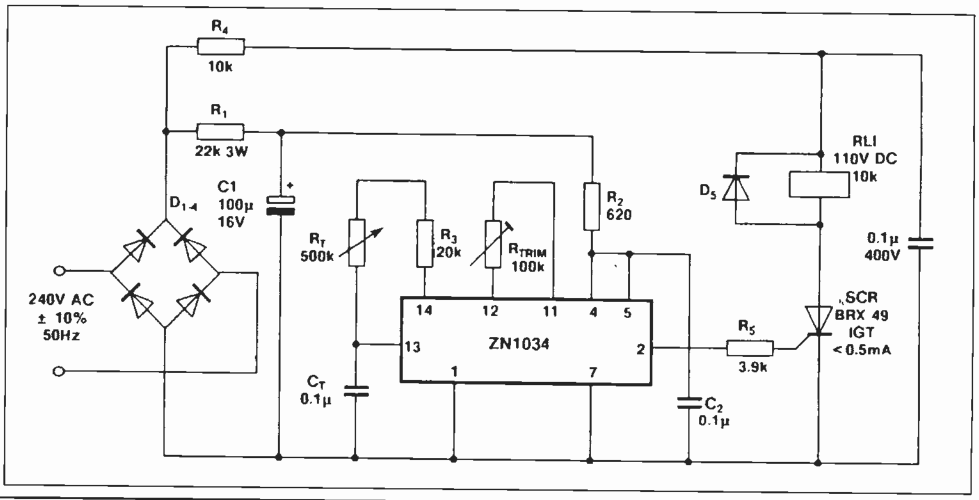


Fig. 5. Delay-to-on plug-in timer module, showing methods of rendering mains and EM noise harmless.

Pressure measurement

Motorola's *MPX2000* series of pressure transducers are temperature-compensated and calibrated on-chip; the *MPX5100* has, in addition, its own amplifier. These units are therefore well suited to use without much extra work; indeed, the *MPX5100* can be connected directly to a microprocessor to make a direct-reading pressure meter. *MPX2000* units have full scales ranging from 1.5 to 100psi and the *MPX5100* measures up to 15psi, the former producing 40mV full scale and the 5100, 4V. Linearities are of the order of ±0.1 to ±0.2%.

Motorola's booklet BR121/D "Pressure Sensors" includes the circuit shown in **Fig. 1**, a portable manometer in which the pressure sensor provides a differential output to a digital panel meter. This will give a moderate performance, being limited to some extent by the amplifiers and power supply; for greater precision, you could use a more exotic instrumentation amplifier and replace the zener by a voltage regulator.

Figure 2 is the circuit of a pressure switch, meant to control compressor and pump motors and heaters in liquid level applications.

In **Fig. 3**, the amplifier and *MC1455*, which is a 555 timer replacement, form a voltage-to-frequency converter which could be driven directly by an *MPX5100* but which driven in the *MPX2000* case by temperature compensation and amplification circuitry. The amplified and compensated output of the pressure

Fig. 1. Portable manometer using one of Motorola's MPX2000 series of pressure transducers to give a direct digital indication of pressure on the internally compensated sensor.

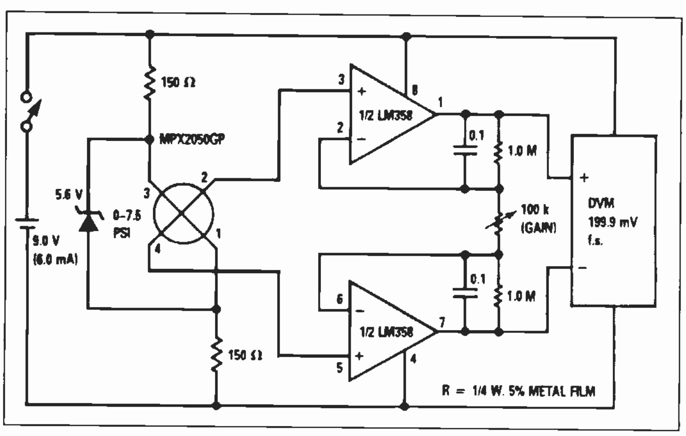
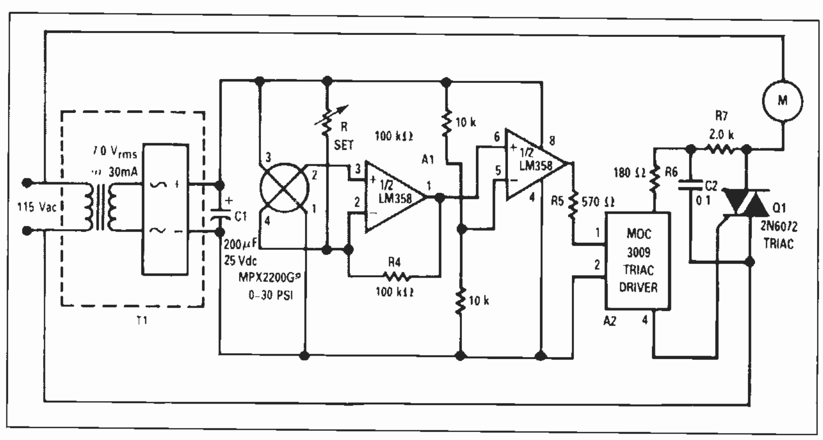


Fig. 2. Pressure switch for motor control, switch point being set by R_{set}.



sensor drives an *LM258*, which acts as a constant-current source to the charging capacitor on the *MC1455*, so that the output frequency is a linear representation of pressure — 6V into the *LM258* gives a 0-14kHz change.

Application Note AN1305 describes an evaluation board to familiarise engineers with the direct interfacing of the *MPX5100* to a microprocessor. **Figure 4** is the circuit of the *DEVB-114* board, which shows very few externals indeed; there are simply the sensor, clock components, a few bias resistors and an LCD to provide a direct reading in pounds per square inch in 0.1psi increments. No manual calibration is needed, since the offset voltage of the sensor without applied pressure is computed at every power-up and stored in ram. *MC34064P-5* is an under-voltage detector used to reset the system at switch-on and the jumpers *J1* and *J2* are for a slight tailoring of span by ±1.5%. The application note gives full details of setting up and the microprocessor software listing in C source code.

Motorola Ltd, *European Literature Centre, 88 Tanners Drive, Blakelands, Milton Keynes MK14 5BP. Telephone 0908 614614.*

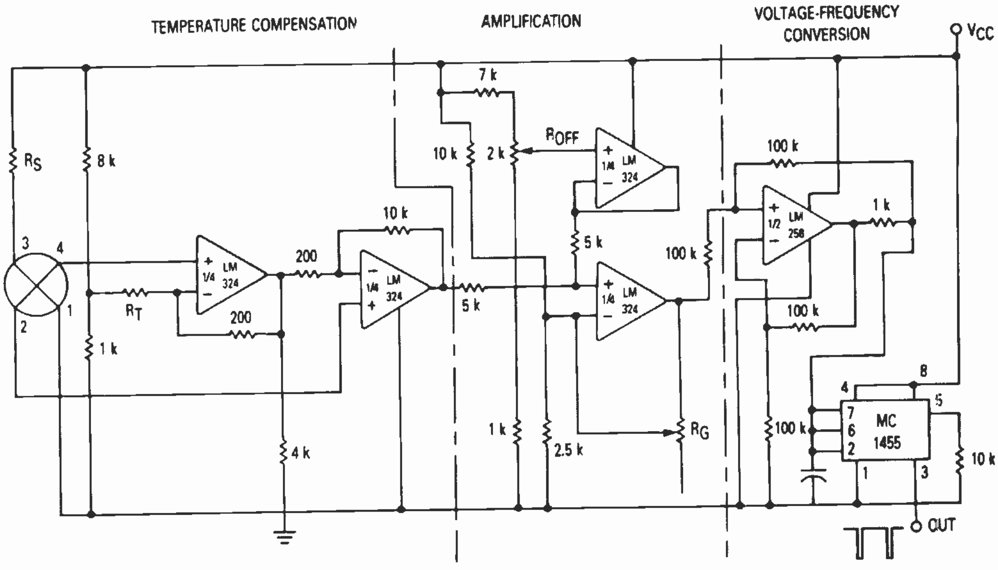


Fig. 3. Pressure-to-frequency converter using MPX2000 series. MC1455 is a direct 555 timer replacement and is used as an astable multivibrator, its frequency directly controlled by the constant-current source of the LM258.

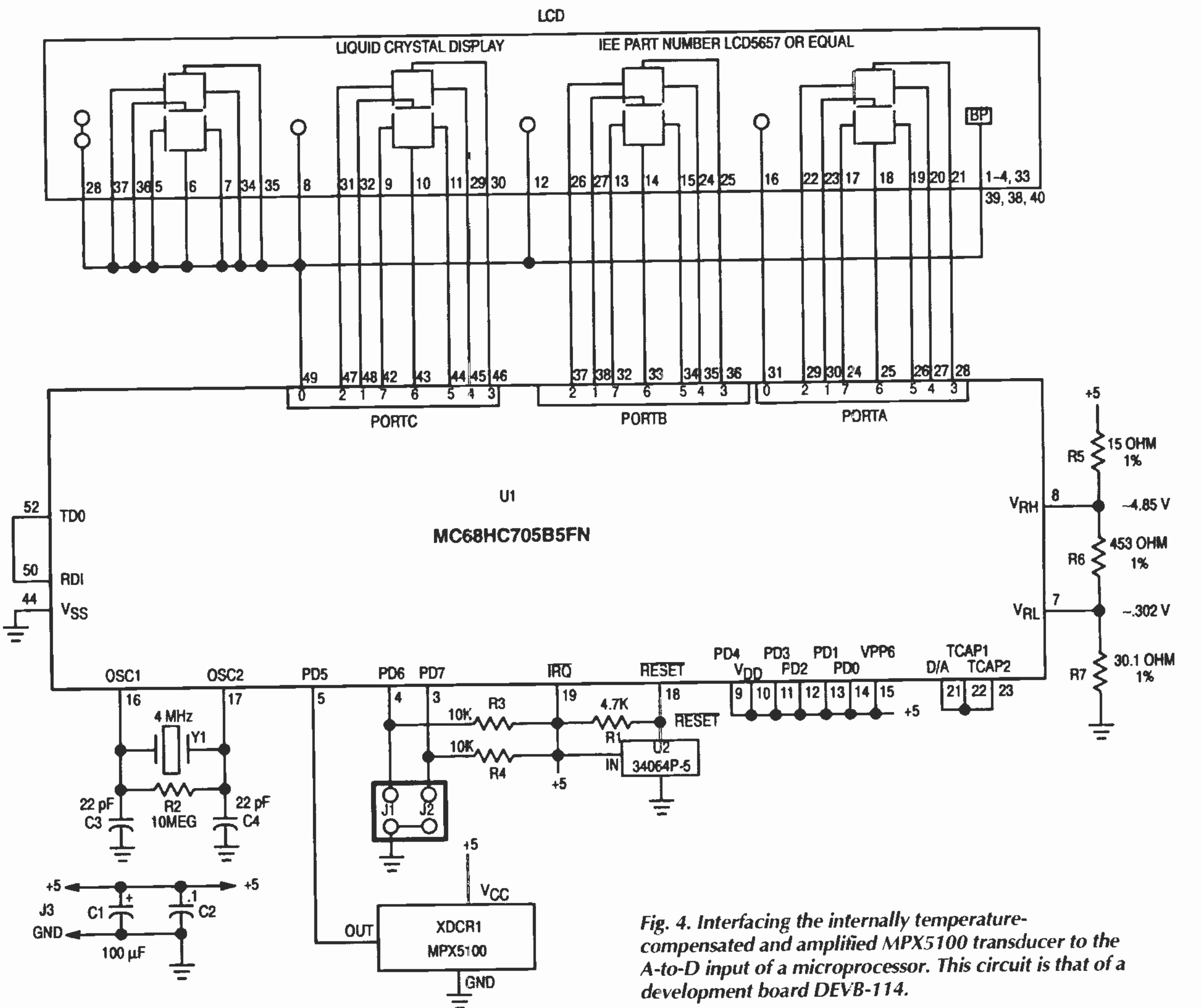


Fig. 4. Interfacing the internally temperature-compensated and amplified MPX5100 transducer to the A-to-D input of a microprocessor. This circuit is that of a development board DEVB-114.

BARGAINS – 10 New Ones This Month

SUPER MULTIMETER Ex British Telecom, this is a 19-range 20k o.p.v. top grade instrument, covers AC & DC voltages, current and resistance, very good condition, fully working and complete with leads **£8.50**. Carrying case £2 extra (batteries not included but readily available).

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ULTRA THIN DRILLS Actually 0.3mm. To buy these regular costs a fortune. However, these are packed in half dozens and the price to you is **£1** per pack, Order Ref. 797B.

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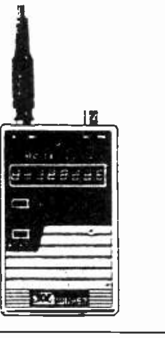

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Circuits, Systems & Standards

First published in the US magazine EDN and edited here by Ian Hickman

Nonlinear components lower settling time of noise reduction filters

Most common method of improving S/N ratio is noise reduction by filtering. But the attendant increase in settling time can be a serious disadvantage in certain applications, such as high-speed data acquisition. A nonlinear filter is a simple way to achieve a four-to-one improvement in settling time over conventional filters.

First, consider the dynamics of a single-pole RC filter (**Fig. 1a**). Filtering reduces broadband or white noise by the square root of the bandwidth reduction, according to the following equations, where e_n is the total noise in V_{RMS}, e_B is the broadband noise in V/√Hz, and f_1 to f_2 is the filter's frequency range in Hz:

$$e_n^2 = \int_{f_1}^{f_2} e_B^2 \mathrm{d}f$$

$$= e_B^2 \cdot f \Big|_{f_1}^{f_2}$$

and thus

$$e_n = e_B \sqrt{f_2 - f_1}$$

These equations show that if the frequency range is reduced, f_2-f_1, by a factor of 100, the total noise decreases by a factor of 10.

Unfortunately, the settling time increases as the bandwidth decreases. For a single-pole filter, the time needed for the signal to settle to any given accuracy can be calculated using the following equations, where t_s is the settling time in seconds, % is the percent of accuracy at time t_s and R_1C_1 is the RC time constant in ΩF. At time t_s

$$\frac{V_{out}}{V_{in}} = 1 - e^{-\left(\frac{t_s}{R_1C1}\right)}$$

and

$$-\left(\frac{V_{out}}{V_{in}} - 1\right)100 = \%$$

Therefore

$$t_s = -\ln\left(\frac{\%}{100}\right)R_1C_1$$

> **Fast settling filters**
>
> Filters are often incorporated at the input of an instrument to reduce noise, for example in a DVM to clean up the DC input ahead of the measuring circuit. However, they frequently increase the settling time by an embarrassing amount: this can be substantially reduced by incorporating nonlinear techniques, as the following article shows.
>
> **IH**

To determine the number of time constants required for the signal to settle within 0.01%, simply calculate ln(0.01/100), which equals –9.2. Thus, it takes 9.2RC time constants for an input step to settle to within 0.01% of its final value.

A simple, diode-clamped nonlinear filter (**Fig. 1b**) can improve the settling time of a simple RC filter. When a large input step is applied to V_{in} the filter capacitor, C_1, charges faster through the forward-biased diode's low impedance than it can through R_1. When the difference between the input and output voltages becomes less than the forward-biased diode's drop (about 0.6V), the diode stops conducting, and C_1 and R_1 are the only active components. At this point, the circuit behaves like a normal, single-pole RC filter.

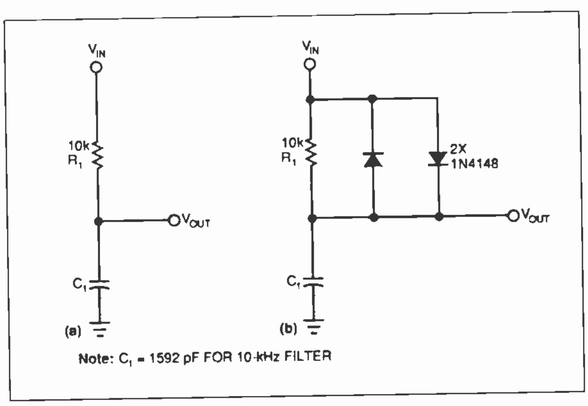


Fig. 1. Settling time of the standard RC filter (a) by adding two diodes (b). C_1 charges and discharges much faster through the diode's low on-resistance than it can through R_1, thus improving settling time.

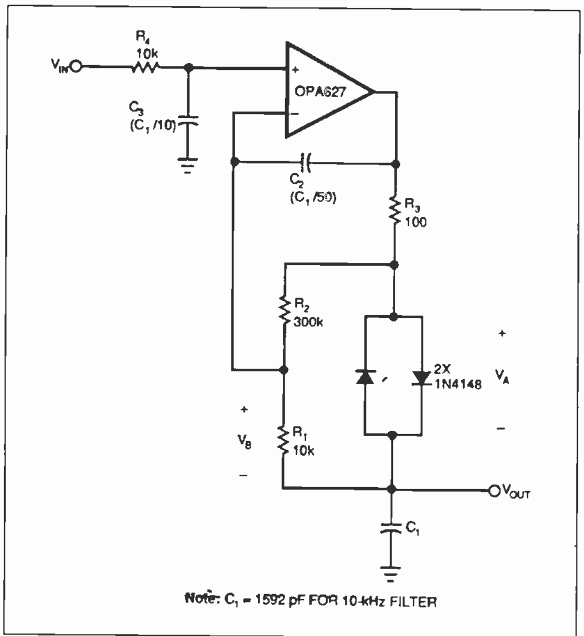


Fig. 2. To improve settling time for small inputs, as well as large inputs, this circuit allows setting of the noise threshold by choosing the values of R_1 and R_2.

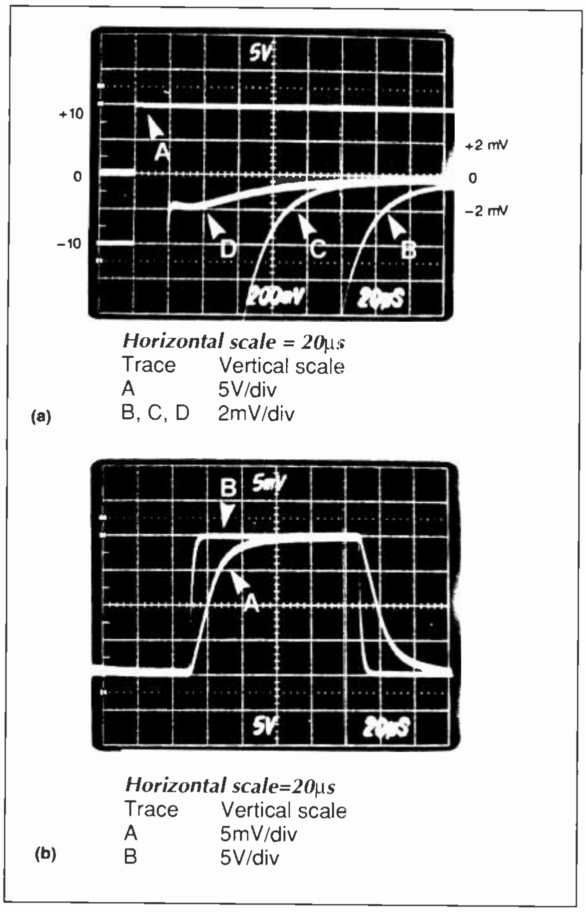


Fig. 3. Response of each filter (a) to an input step (trace A) shows the graduated settling-time improvement from the simple RC filter (trace B) to the improved non-linear filter (trace D). The double-exposure scope photo in (b) contrasts the small-signal (trace A) and large-signal (trace B) settling times of the improved non-linear filter.

Assuming that the diode's R_{on} is very small and thus negligible, this filter's improvement in settling time depends on the ratio of the input step and the forward-biased diode's voltage. For a 20V step, −10 to +10V for example, the filter improves settling time by ln(0.6/20), or 3.5 time constants. In other words, for a 20V step, the simple, diode-clamped nonlinear filter shortens the normal *RC* filter's 0.01% settling time from 9.2 time constants to 9.2–3.5=5.7 time constants. However, as the ratio between the input voltage and the diode's forward voltage decreases, so does this circuit's advantages. The settling-time improvement decreases for smaller input steps. When the input step equals the forward-biased diode's voltage drop, the circuit provides no improvement in settling time.

Lower the threshold

By reducing the threshold to below 0.6V, settling time can be improved for even smaller inputs. The improved nonlinear filter shown in **Fig. 2** allows adjustment of the clamp threshold by choosing the values of R_1 and R_2.

Figure 2's op amp forces the voltage at its inverting input to be the same as the signal at the non-inverting input. Small voltage differences between the input and the output voltages appear across R_1, because the diodes don't have adequate forward bias and are therefore off. Under these conditions, the filter behaves like a single-pole filter with a time constant determined by the values of R_1 and C_1.

The voltage divider formed by R_1 and R_2 forces the voltage V_A to equal

$$V_A=V_B[(1+(R_2/R_1)]$$

When the input voltage increases (applying a step voltage, for example), V_A increases. When the voltage difference between the input and output approaches $0.6V/(1 + R_2/R_1)$, the diode that corresponds to the input's signal polarity will begin to conduct, and the capacitor will rapidly charge through that diode.

To determine Fig. 2's component values, noise-reduction requirements of the filter must considered. For example, to filter the noise of a 20V step to 0.01% resolution, filter the signal's peak noise to less than 0.01% of 20V, or 2mV peak. A clamp threshold of ten times this peak, or 20mV, is an arbitrary but ample nonlinear threshold. The component values shown in Fig. 2 set the filter's threshold to 20mV. The time constant of the filter is very small, regardless of which diode is on, and the settling time is limited only by the op amp's slew rate or current limit. For a 20V step, Fig. 2's improvement in settling time is ln(0.02/20)=6.9 time constants.

In other words, the improved nonlinear filter can improve the 0.01% settling time of a 20V step from 9.2 time constants to 9.2-6.9, or 2.3 time constants – a four-to-one improvement. Further reducing the 20mV threshold provides little additional settling-time improvement.

To use this filter successfully, noise content of the input signal must be known. If the noise of the signal is greater than the threshold – 20mV in this case – the filter will mistake the noise as a step input and fail to filter it out. Thus, Fig. 2 only behaves as the desired filter for noise signals below the threshold that is set.

If the noise exceeds 20mV, Fig. 2's circuit will not behave as an *RC* filter with the desired 10kHz cutoff. To prevent this situation, ensure that the noise signal at the op amp's input does not exceed 20mV by using C_3 and R_4 to prefilter the input.

To reduce the prefilter's effect on settling time, the values of R_4 and C_3 set the prefilter's bandwidth ten times higher than the bandwidth of the noise filter. At this higher bandwidth, the prefilter's effect on settling time is negligible, and the noise at the prefilter's output is $\sqrt{10}$ times greater than 2mV, or a little over 6mV peak. (Recall that noise is proportional to the square root of the bandwidth.) A noise level of 6mV provides a comfortable margin for a 20mV threshold.

Choose the right filter ingredients

Op amps tend to become unstable and to oscillate when driving large capacitive loads. The network comprising C_2 and R_3 in Fig. 2 ensures circuit stability when the op amp is driving large values of C_1 through the low impedance of the forward-based diode network. This network may not be needed if C_l is a small value.

When choosing the op amp for the improved filter, make sure it has enough output-drive capability to charge C_l. Also, the op amp's bandwidth, slew rate, settling time, and DC precision must be adequate for the necessary filter response. Choose an op amp such as the *OPA627*, which combines DC precision, high slew rate, fast settling time and high output-drive capability. Also, notice that any unity-gain op amp's noise adds noise to the signal. If a low-noise op amp is chosen, the op amp's noise contribution is usually negligible. For example, the *OPA627* adds only 6% of the 10kΩ resistor's theoretical minimum noise to the total system noise. Remember that noise adds as the square root of the sum of the squares. Therefore, to determine how much the 4.5nV√Hz noise of the op amp adds to the 12.8nV√Hz noise of the resistor, calculate the square root of the sum of the squares of the combination and compare that to the noise of the resistor alone. In this case, $\sqrt{(4.5^2+12.8^2)}/12.8=1.06$, or a 6% increase.

Figure 3a shows the responses of the standard *RC*, diode-clamped, and improved nonlinear filters to a –10 -to +10V input step. Bandwidth of each filter is 1kHz. The measurement circuit adds a gain of 100 between the scope and the circuit, so each horizontal division for traces *B*, *C*, and *D* represents 2mV, or 0.01% of a 20V step. Thus, the filters settle to within 0.01% when their corresponding traces lie within one division below the centre line of the scope.

For a 10kHz filter, one *RC* time constant is 15.9s. **Table 1** displays the theoretical settling times of each filter.

Table 1. Theoretical time constants and settling times.

Filter type	Theoretical settling time (time constants)	Theoretical settling time (μs)*
Single pole RC	9.2	147
Diode clamped nonlinear	5.7	91
Improved nonlinear	2.3	37

*Time required to settle within 0.01% of the final value for a 10kHz filter.

These tabulated settling times ignore the input slew rate and the diode forward resistance, which are good approximations for the *OPA627*-based, 10kHz filter. The actual measurements closely match the theoretical calculations.

Figure 3b is a double-exposure scope photo of the improved nonlinear filter operating with a low (trace *A*) and high (trace *B*) input signal level. The filter's response to a ±10mV step looks like the response of a standard, 110kHz, single-pole *RC* filter. This response is expected, because the input is equal to the threshold voltage. When the circuit operates with a high input level (a ±10V input step), the settling time greatly improves.

*Rod Burt and R Mark Stitt, **Burr-Brown Corp***

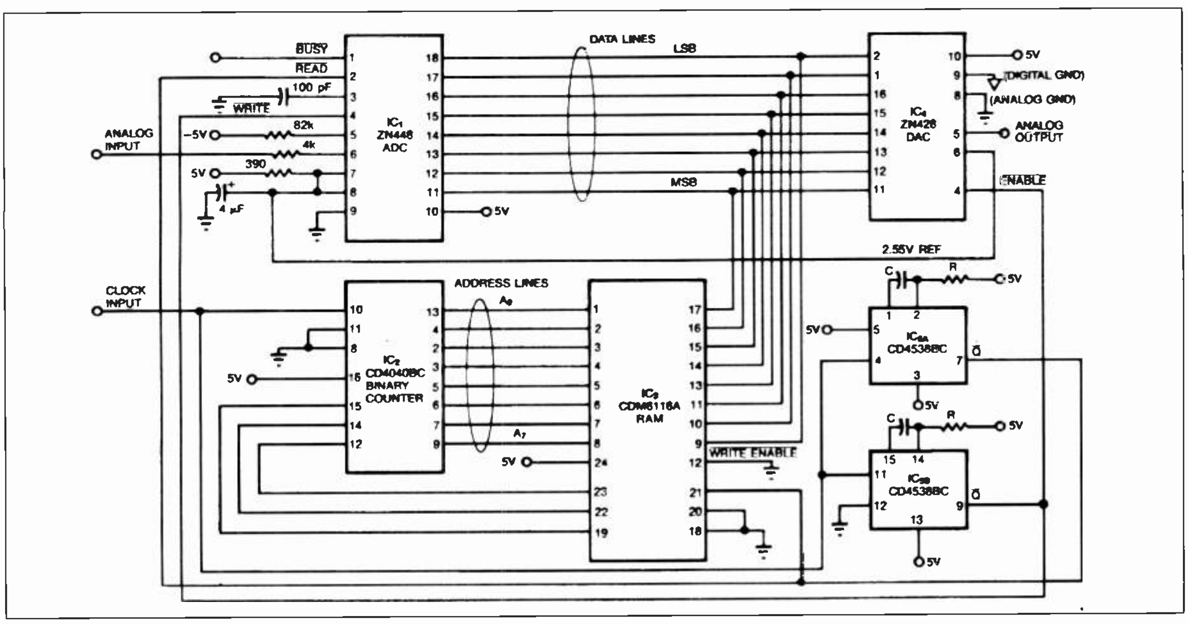
Analogue delay line uses digital techniques

The analogue delay line in the figure uses a digital technique to delay an analogue signal for as long as 2s, reconstructing the signal with 8-bit resolution. The product of the delay time and the bandwidth is a constant: For a 1.024kHz clock frequency (2s delay), the analogue bandwidth is 100Hz; for the maximum 40.96kHz clock frequency (50ms delay), the analogue bandwidth is 4kHz. There is no lower limit for the clock frequency.

The clock signal drives a binary counter (IC_2), which

Digital analogue delay line

This circuit will produce a delayed exact replica of a sampled input signal, without any of the approximations involved in schemes designed to handle speech – such as delta modulation and its derivatives – which cannot handle large signal energies in the upper part of the passband. By using a counter providing more address bits, in conjunction with an 8K x 8 sram or larger, the time delay product can be extended as required. **IH**



Analogue delay digitising a signal once per clock cycle, storing the result in a 2048 word ram, and converting one sample per clock cycle with a D-to-A converter. The resulting delay equals 2048 divided by the clock frequency.

then scans the address inputs of a 2048-byte x 8-bit ram (IC_3). The ram writes the contents of each memo location to the D-to-A converter (IC_4) and then reads out the results of a just-completed conversion by the 8-bit A-to-D converter IC_1. The ram reads out each data sample 2048 cycles after it is read in, so the delay is 2048 times the clock period, or 2048 divided by the clock frequency.

The clock signal also drives two monostable multivibrators in parallel (IC_{5A} and IC_{5B}). IC_{5A} triggers on the clock's rising edge; IC_{5B} triggers on the clock's falling edge. The timing components R and C can be chosen so that each device produces a pulse of approximately 1µs. These pulses have the proper polarity and phase to control the A-to-D converter, D-to-A converter, and ram as shown.

The analogue input should be scaled for a range of 0 to 2.5V. The 100pF capacitor sets the A-to-D converter's internal clock to its maximum rate of 900kHz; the /busy signal (pin 1) should be monitored and capacitor value adjusted as required to achieve 900kHz. Both converters include a 2.5V voltage reference. But to improve accuracy use the A-to-D convertor's reference for both. Power consumption is 120mA from the 5V supply and 50µA from the –5V supply. The current drain from the positive supply can be greatly reduced by adding logic to control the ram's chip-enable input (pin 18).

TG Barnett and J Millar, *The London Hospital Medical College, London.*

Transistor powers low-dropout regulator

The monolithic regulator chip in the figure, combined with an external PNP transistor, forms a very-low dropout regulator, and can apply several hundred milliamps at 5V from an input as law as 5.3V. Such low-dropout performance suits battery-powered applications, because it extends the useful life of batteries having sloping discharge curves – such as sealed lead-acid and lithium batteries.

The monolithic regulator derives its supply current from the base circuit of the external PNP transistor. The feedback-resistor ratio sets the output voltage:

V_{out}=1.3Vx(R_1+R_2)/R_1

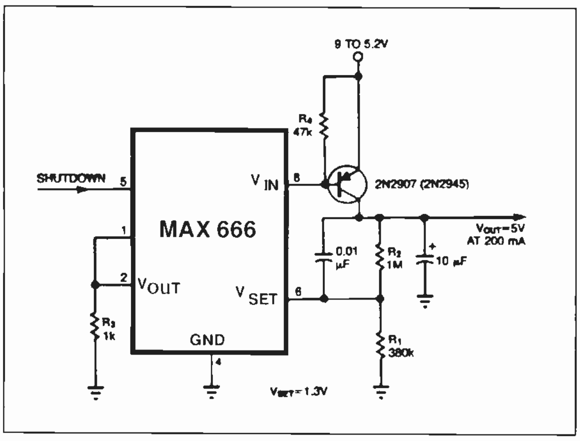
If the output-voltage feedback to the chip's V_{set} input is below the bandgap-reference voltage (1.3V), the supply current into V_{in} – the PNP transistor's base current – increases. The transistor multiplies this base current by β and delivers it to the load. The circuit's quiescent current is a function of the transistor's β and load current. When there is no load, the quiescent current is typically 10µA. For larger load currents, the quiescent current is simply the load current divided by the transistor's β. The regulator chip can sink 40mA max, and when the chip's shut-down input is enabled, the circuit consumes 6µA typically. R_4 supplies current to the chip under no-load conditions.

R_3 can limit the transistor's base current. The chip's V_{out} pin will try to raise its voltage level to that of the V_{in} pin when the output voltage of the chip is low. Reducing R_3 has the effect of supplying larger base currents to the external transistor.

A *2N2945* can be substituted for the *2N2907* shown in the figure. With this substitution, the circuit will supply a 5V, 100mA max output from a 5.1V input. ■

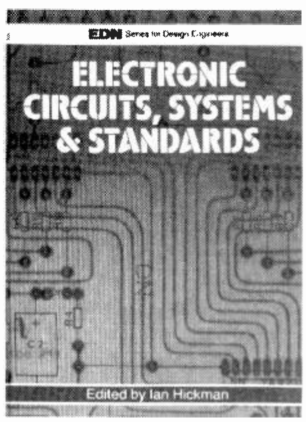
Low headroom regulator

In battery-powered instruments, a regulator needing very little headroom can substantially extend the useful life of primary batteries, or allow less frequent recharging of secondary (rechargeable) batteries. This circuit can provide 100mA at 5V from an input as low as 5.1V.
IH



A monolithic regulator chip driving a dummy load sets the base current of an external, series-pass PNP transistor; the result is a very-low-dropout regulator for batteries whose output voltage drops under load.

James E Dekis, *Maxim Integrated Products, Sunnyvale, Ca and* ***Terry Blake,*** *Motorola, Schaumberg, Il.*



Getting a word in edgeways

Pat Hawker reports on development success in reducing the bit-rate of digital speech

As telecommunications assume an increasingly digital aspect, the question of just how much material can be squeezed into a low-rate bit stream without excessive cost and quality degradation has become crucial. Decisions on standards and algorithms made now will have implications well into the 21st century.

Today, the packaging of speech and video, with their high degrees of redundancy, has moved on a long way from basic PCM. Professor C Xydeas, University of Manchester, emphasised the current level of development at a recent IEE colloquium *Speech coding - techniques and application*: "Present day techniques seek to exploit the intrinsic properties of speech signals in order to remove redundancy and thus achieve improved compression/speech quality performance."

Mean opinion scoring

In an overview of the subject, Xydeas described use of the 1-5 scale of mean opinion score (mos) for assessing speech quality of 200Hz to 3.4kHz channels. For network (toll) channels, a mos of 4.0 or better is needed and for communication channels a score of 3.5 to 4.0. Mos values in the region 2.5-3.0 imply "synthetic" quality speech. Although still highly intelligible, this quality has a reduced naturalness and speaker recognisability, but can be transmitted at bit rates of less than 2.4kbit/s, making such vocoders suitable for HF radio circuits. For "broadcast-quality" speech a baseband of 50 to 7000Hz "offers a dramatic improvement in naturalness and intelligibility (unvoiced sounds) compared with conventional telephone speech... voice applications such as ISDN teleconferencing and loudspeaker telephones are based on broadcast quality speech and require codecs that can produce a mos score equal or better than 4.0".

Several presentations stressed that decoded speech quality is closely linked to output bit-rate and the codec complexity. As the required bit-rate decreases, codecs become ever more complicated, with algorithms having a direct impact on implementation costs and power consumption.

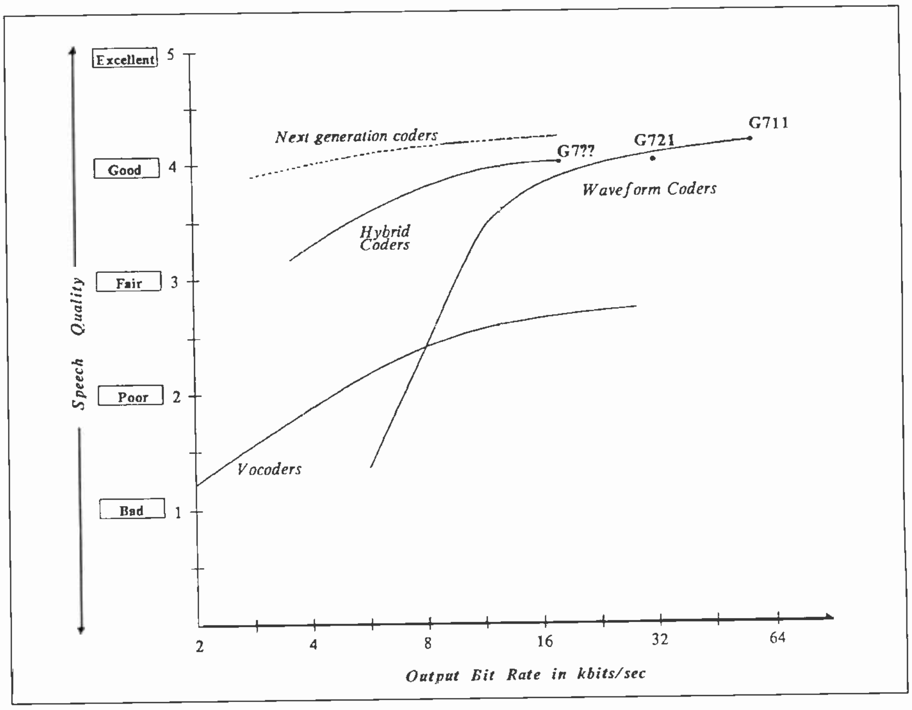
To achieve good quality at the lowest bit rate requires complex processing that may introduce excessive time-delay for real-time, two-way speech. But where the material is to be stored, good-quality speech can be recorded using repeated processing. D Y-K Wong (Ensigma Ltd) demonstrated a variable rate linear prediction coder which works on four major types of segment. Wong explained how very high coding efficiency and good quality speech reproduction on material recorded at an average bit-rate of 3.5kbit/s (peak rate of 7kbit/s) were possible, achieving a perceptually weighted SNR of 17.5dB in the voiced region. This would, for example, enable a "voice dictionary" to be recorded on compact disc.

Real-time communications

For real-time communications, Liverpool University and BT are jointly developing a pitch synchronous scheme for voiced frames and celp (codebook excitation linear prediction) for coding unvoiced speech frames. The scheme has been tested in simulation, obtaining good communications-quality speech at 3.1kbit/s. The simulated coder produces reconstructed speech of good and natural quality.

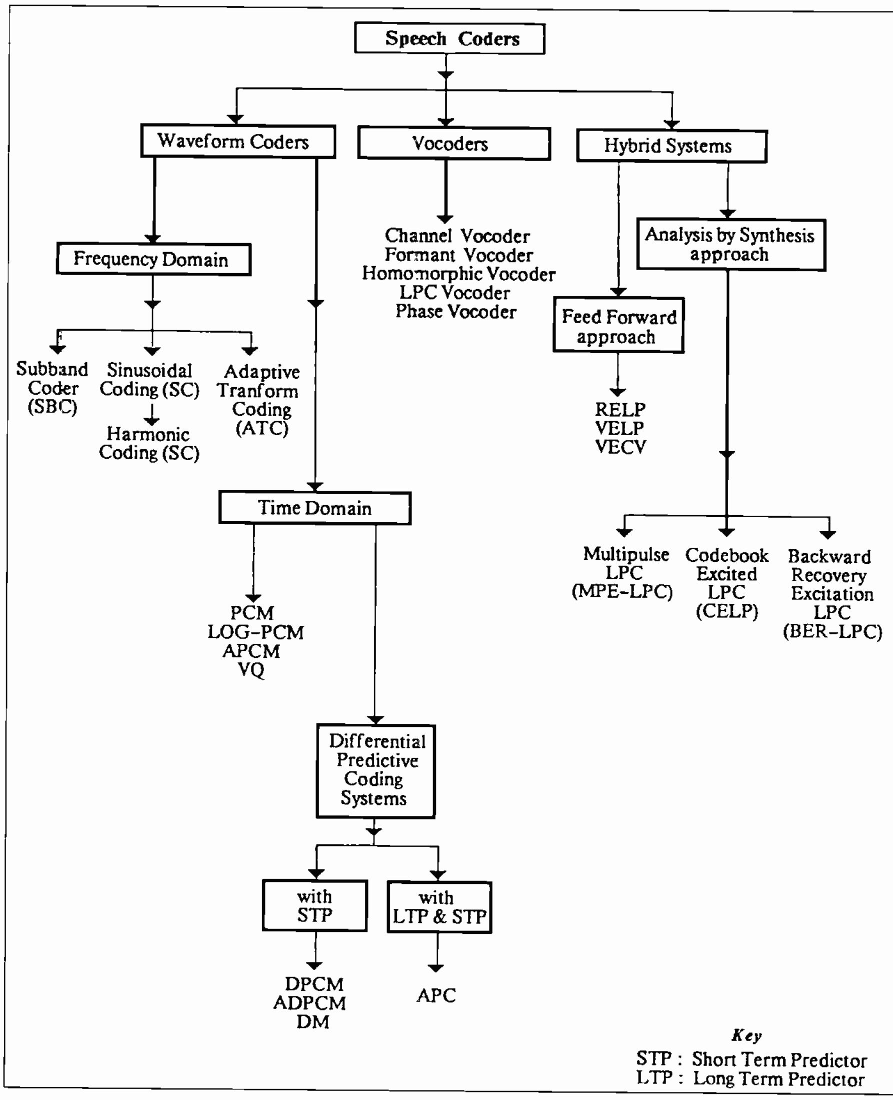
Nigel Sedgwick (Cambridge Algorithmica) described a formant vocoder being developed to operate at 600bit/s. Such vocoders are mainly of interest for military use where communication bandwidth is at a premium, for example over tactical HF radio using frequency hopping as an electronic counter-counter-measure where users would be prepared to accept the disadvantages of increased cost and lower speech quality compared with vocoders operating at 2.4kbit/s. The work is supported by a contract from RSRE Malvern covering specification, design and implementation of a non-real-time

Speech quality versus bit rate for telephone bandwidth speech codecs: from** An overview of speech coding techniques, **C Xydeas.



software simulation of the vocoder.

The formant analysis adopted draws on investigations, later abandoned, by the Joint Speech Research Unit (GCHQ) at Eastcote and Cheltenham in the 1970s and early 1980s. It includes variable frame-rate (VFR) coding using a dynamic programming algorithm to select, simultaneously, the optimal sequence of frames to transmit, plus the use of a vector-quantised codebook of formant frequencies and amplitudes. As part of the codebook generation software, there has been an early implementation of a scalar-quantised VFR vocoder but with less complex coding of the side information and with an effective data rate of 1320bit/s. At this level, speech from good quality recording remains intelligible but leaves much to be desired. With parameter tuning etc a VQ/VFR vocoder at 600bit/s should be better.



Speech coding methodologies. C Xydeas.

Broadcasting in bits

Simon Shute (BBC) gave a rather different meaning to "low" in speaking of "low bit-rate digital audio broadcasting (dab)". He noted that the accepted standard for coding audio in studio applications uses a sampling frequency of 48kHz, with up to 20bits per audio sample – although most current equipment can handle only 16bit. This AES/EBU digital audio interface standard when implemented for a stereo pair and multiplexed with the necessary framing, signalling and control information represents a bit rate of 3.072Mbit/s. It is against this yardstick that broadcast engineers judge their "low bit-rate" coding systems.

Shute concentrated on musicam, the coding system chosen for audio coding for the European musicam/cofdm dab system developed by the Eureka 147 Group as a means of delivering to listeners CD-quality stereo at a bit-rate of around 200bit/s per stereo channel. He emphasised the advantages of using cofdm transmission with its high resistance to multipath problems that continue to place severe limits on the performance of pilot-tone FM received in moving vehicles.

Incidentally, he admits that the addition during the 1980s of a vertically polarised component to BBC VHF/FM transmission has "to some extent" proved counter-productive. (His comments fulfilled the fears I expressed in *Multipath distortion – does polarisation matter?*, *Wireless World*, April 1981, pp. 83-85 which brought on my head the wrath of the Directors of Engineering of both the BBC and the IBA!)

The musicam/cofdm system is also much more spectrum-efficient than analogue FM, permitting six multiplexed stereo-channels to be accommodated in a bandwidth of 1.5MHz compared with 2.2MHz per single national channel for FM. Because cofdm is intrinsically immune to delayed echoes resulting from reflections, it is equally immune to co-channel signals arriving from other transmitters in adjacent areas, and can thus be re-used for as many transmitters as are needed to provide national coverage.

Shute admits that the BBC is seeking a VHF channel for terrestrial dab (possibly in Bands I or III) with the original proposal for direct reception from a non-synchronous-orbit satellite now on the back-burner, although national distribution of the digital signals would most likely be based on a satellite. The BBC believes that dab may eventually supersede FM for national services in Band II, although FM transmissions are likely to continue for a number of years.

He says that a number of hurdles remain before dab can be introduced in the UK. But its technical and economic attractions are such that he is convinced that the necessary steps will be taken and that we can look forward to a dab service beginning in the mid-1990s, with significant area coverage and affordable receivers for home and car reception. ■

Cryptic beginnings

It is now almost 45 years since Claude Shannon defined, in the *Bell System Technical Journal*, the intellectual framework for efficient packaging and transmission of electronic data. As noted recently by John Hogan in *IEEE Spectrum*, Shannon's classic paper "The Mathematical Theory of Communication" still stands as a beacon of the communications age.

Shannon, like our own Dr Alan Turing, gained an insight into digital communications during his wartime work in the field of cryptography – in his case while working on the "Green Hornet" (project X or Sisaly) long-range HF secure speech system in which "one-time" keys in the form of digital bits were distributed on disc recordings.

Green Hornet was used, for example, in the later years of the war to provide a secure telephone link that was almost certainly the first-ever crude implementation of Alec Reeves's pulse code modulation patent, between London and Washington DC. Built around thermionic valves, the London terminal behind Selfridge's required 30 racks of equipment and consumed many kilowatts of electricity to provide a few milliwatts of just-intelligible speech.

But Shannon has acknowledged that it was his cryptographic work that led him to develop his theory of communication. He realised that, just as digital signals could protect information from prying eyes and ears so codes could also be used to package information more efficiently, allowing more of it to be carried over a given channel.

Signal receiver for satellite broadcast. In UK patent 2235340 Funal Electric Engineering Co Ltd. describes a signal receiver. It has probe antennas provided in a waveguide for receiving differently polarised waves such as vertical and horizontal polarised waves. The probe antennas are arranged to intersect at right angles in the waveguide where each antenna is connected to input terminals of an amplifier. According to the structure, it is possible to receive both vertical and horizontal polarised waves simultaneously without using a rotational probe antenna. In a modification, clockwise and anti-clockwise circular polarisation waves can be received. The amplifiers may each include a gallium arsenide field effect transistor selectively switched on to receive the required vertical or horizontal polarised waves.

FMCW intruder alarm system. In U.K. patent 2236926 GEC-Marconi Ltd. describes a range-sensitive intruder alarm system using FMCW radar. A sinusoidal FMCW signal is generated and mixed with reflected signals to produce an output signal comprising a series of frequency components which correspond to sidebands of the FMCW signal. Each frequency component has a unique amplitude variation with the range of the source of the return signal. Selected frequency components are filtered and their amplitudes compared to define a range limit of the system. The alarm is triggered by the output of a threshold circuit which monitors the amplitude of one of the frequency components. Triggering of the alarm is inhibited if the comparison reveals a disturbance occurring outside the defined range limit. A second range limit may be defined by comparing the amplitude of a third frequency component with one of the first two.

Detection circuitry. In UK patent 2221294 Formula Systems Ltd describes detection circuitry with improved range and signal-to-noise ratio. It includes a number of light emitting diodes connected in series and powered by a current source gated by an oscillator and a number of photodiodes. Each photodiode has its own separate detection circuit which is gated by the oscillator and AC decoupled by capacitors to filter out the DC content of sunlight and the AC content of fluorescent artificial lighting. Summing means sum the outputs of the detection circuits so the resultant output signal is increased by a factor equal to the product of the number of light emitting diodes and the number of photodiodes, over the situation where only one diode of each type is used.

Capacitance measuring. In UK patent 2223320 Northern Engineering Industries describes the measurement of line capacitance, eg of a telephone line, using a known capacitance in series with the line conductors. An oscillatory signal sent to the conductors through the known capacitance and an output current signal is obtained, dependent on the line capacitance. After passing the output through amplifying and phase sensing stages the output signal in phase with the input is obtained and is scaled to drive a meter. An output voltage signal from the line conductors is used to determine line capacitance.

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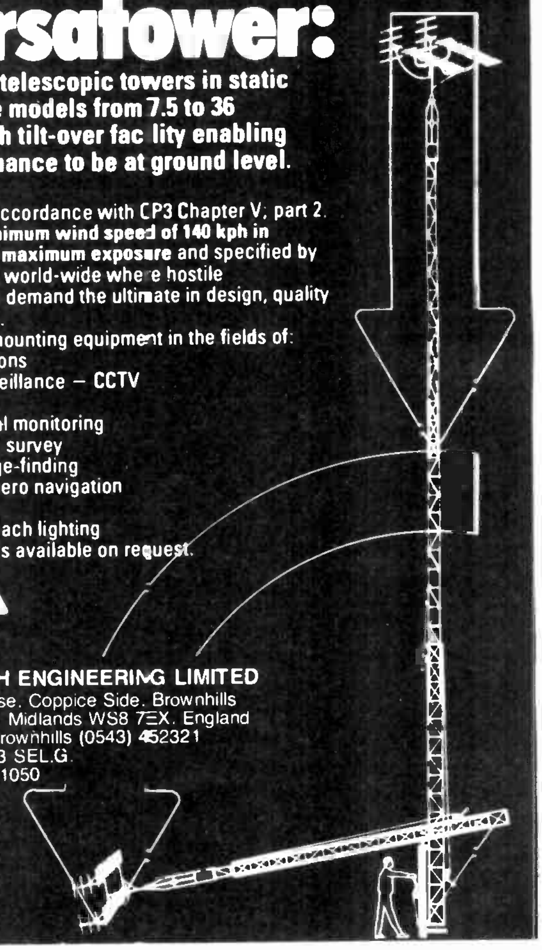

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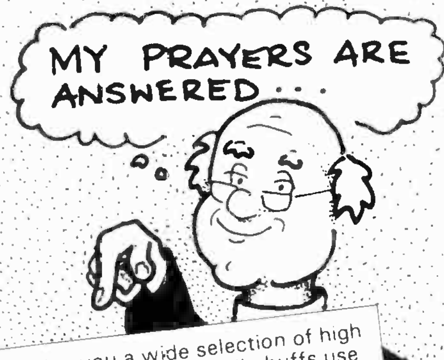

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DIGITAL SIGNAL PROCESSING YIELDS NEW HARDWARE

DSP is no longer seen as just a way of obtaining analogue performance at lower costs. Pat Hawker reports on how DSP is opening up entirely new applications.

The all-digital communications receiver, with incoming signals converted into digits at the signal frequency, still seems some way off. But analogue-to-digital conversion as a prelude to digital signal processing, at either base band or increasingly at a bandpass intermediate frequency, is undoubtedly opening the way to an increasing number of novel hardware implementations.

It is already some six years since the Rockwell-Collins VLF/HF receiver *EF2050* was introduced – a pioneering effort using the concept of flexibility of final receiver bandwidth, ripple and selectivity being determined by programmed data within VLSI signal processors. Even then it was recognised that further advantages would come with development of more linear A-to-D chips working at higher speeds. The aim was (and remains) a receiver with an overall performance in no way inferior to that of the best conventional analogue receiver, but offering advantages such as accurate, calculable multiple bandpass filter, a lower component count, and easier assembly – all pointing to lower costs.

Front-end signal processing in receivers is only one of the many applications of digital signal processing currently attracting attention. DSP is not only about achieving similar performance at lower cost than conventional analogue circuitry; now it is seen as opening the way to new systems, incapable of implementation in purely analogue electronics. For example, in video and speech coding and compression, and HF direction-finders (with relatively simple installations able to distinguish between signals separated in bearing by only about 2° using beam-forming techniques).

Implementing novel hardware

An IEE colloquium "*Implementations of novel hardware for radio systems*" concentrated on currently-sponsored university research projects involving DSP techniques. The paper presented by A M Thurston of GEC-Marconi Research (jointly authored by M O J Hawksford of the University of Essex) set out to show the advantages of IF converters used to digitise signals in high-performance receivers, over use of baseband converters to encode I and Q signal components. IF conversion can overcome the disadvantage of achieving two accurately matched mixers fed with precise in-phase and quadrature carriers to minimise images, and the problem that DC offsets and low-frequency $1/f$ noise at the mixer outputs produces components which cannot be distinguished from signals at the IF centre frequency. Both problems can be overcome by encoding the IF signal directly.

Thurston showed the various advantages that can stem from use of bandpass delta-sigma A-to-D converters. He explained how these can be designed by first converting the baseband modulator into its bandpass equivalent and then designing a system of D-to-A converters and analogue loop filters for which the pulse response at the sampling instants is identical to the impulse response of the bandpass digital filter. The approach is commonly known as "impulse invariant design".

Thurston stressed that practical results have demonstrated the high linearity which may be achieved with sampling and subsampling converters. Simulation results show the extended performance which should result from an interpolating carrier (**Table 1**).

Table 1. Extended performance through an interpolating carrier

Performance	Sampling	Subsampling	Interpolative
Noise power density/Hz	−117dB0	−114dB0	−130dB0
Third order intercept	26dB0	24dB0	32dB0
Spurious free dynamic range in Hz (single tone)	95dB	92dB	108dB

Long distance modem

In the first of two papers from members of the Hull/Warwick Communications Research Group, P D J Clark described a flexible MFSK data modem based on an AT&T *DSP32C* processor integrated within an IBM PC compatible host and employing a novel data-derived synchronisation scheme. The adaptive modem has been based on the original 32-tone Piccolo concept as developed in the 1960s by the Diplomatic Wireless Service (now Foreign & Commonwealth Communications Branch).

The modem exhibits a far greater degree of responsiveness to both user requirements and channel state than previous implementations. It is capable of transmitting and receiving up to 32 signal tones in simplex mode, independently agile within a 2kHz bandwidth with a resolution of 1Hz.

Symbol transmission rate may be configured from 10symbols/s to 500symbols/s. The work is supported by the Farnborough defence research establishment and a possible application is for long-distance aeronautical HF communication.

Recent work on a multi-functional radio system terminal at Hull University – including the generation of low-cost ionograms – was reported by M Gallagher.

With professor M Darnell, he believes that although the benefits of DSP technology have