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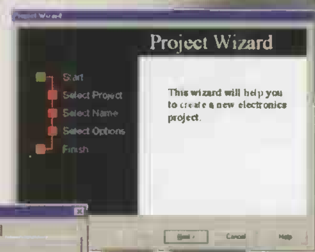

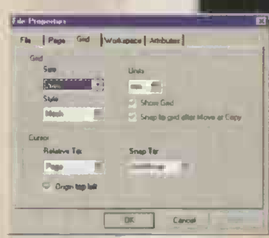

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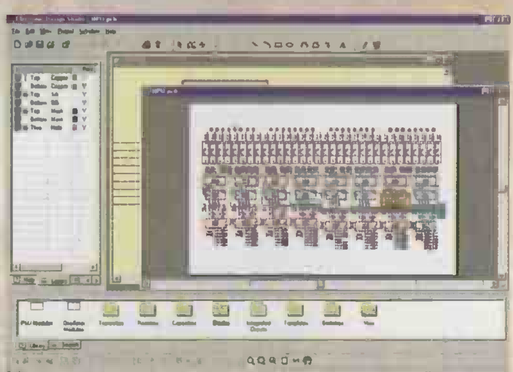

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CIRCLE NO. 101 ON REPLY CARD

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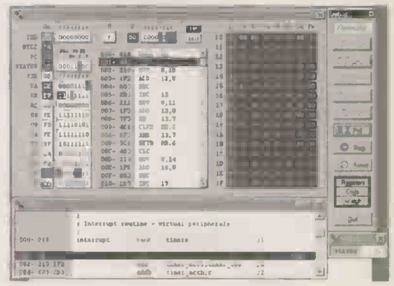
1049 HANDS ON INTERNET: The perfect transistor
Cyril Bateman looks at the nearest thing to a perfect transistor. Its output swings negative for negative base signals and vice-versa for positive ones. It has a 700MHz bandwidth, 737nV/√Hz noise and low distortion – even at 10MHz.

Joe Carr looks inside some commercial instruments for measuring RF power and explains how they work – on page 1000.



Save 18% on an emulation and development kit for the world's fastest 8-bit micro – £139 fully inclusive. See page 992.

550MHz spectrum analyser add-on, PC voltage generator, Christmas lights and an 'in-use' indicator – will any of these Circuit Ideas win one of £3500 worth of prizes from National Instruments? See page 1006 onwards.

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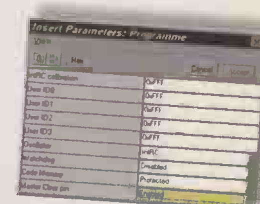

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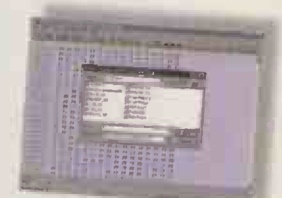
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CIRCLE NO. 104 ON REPLY CARD

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REED BUSINESS INFORMATION

Musical numbers

You might expect the head of a government watchdog body to get his facts right. But not the unfortunate Don Cruickshank, former director-general of OFTEL.

Addressing GMTV viewers on 13 April 1995, Cruickshank stated specifically that from Easter Sunday 1995, nobody's UK phone number starting 01 would ever change again.

On BBC2's *Newsnight* programme, under intense questioning from Jeremy Paxman, he repeated this assertion; it was the last time that anyone's phone number would be altered.

Five short years later – and once again in April – some 10 million telephone subscribers will nevertheless have new numbers forced upon them. The renumbering doesn't end there either; all mobile and pager numbers that do not already begin with 07 will change as well, as will many freephone, local-rate and premium rate 'non-geographic' numbers.

Those living in London will feel particularly hurt since, setting aside the loss of the more memorable alphanumeric numbers such as WHItehall 1212 and ABBey 1234 some 35 years ago, they have 'enjoyed' four different numbers in just ten years.

London's 01 zone was split between 071 and 081 in May 1990, renumbered 0171 and 0181 in April 1995, and will recombine under the new 020 code next year.

The cost of change is not trivial either; the true cost of the 1995 code change was £3.25 billion according to the Telecommunications Managers Association (TMA). This time around, it could be much more – not to mention user confusion. Despite a £20 million information campaign, nearly 40 per cent of the population remained unaware of the changes in a September survey conducted by the British Market Research Board.

Phone users will have to learn and dial the new numbers, while printed literature and stationery as well as shop fronts, vehicles and all other signage will need alteration. Memory telephones and repertory diallers in automatic fire and burglar alarms will need reprogramming.

Look-up tables used in smart sockets and call connect systems for call routeing and management will need changing, while the code lists programmed into privately owned payphones for assessing call charges will also need alteration.

So why the change? And what had OFTEL not foreseen in 1995? Contrary to popular perception, the answer is not growth in demand for telecommunications services *per se*. The unabated demand comes from competing operators wanting their own number blocks, plus heel dragging by all parties over introducing number portability.

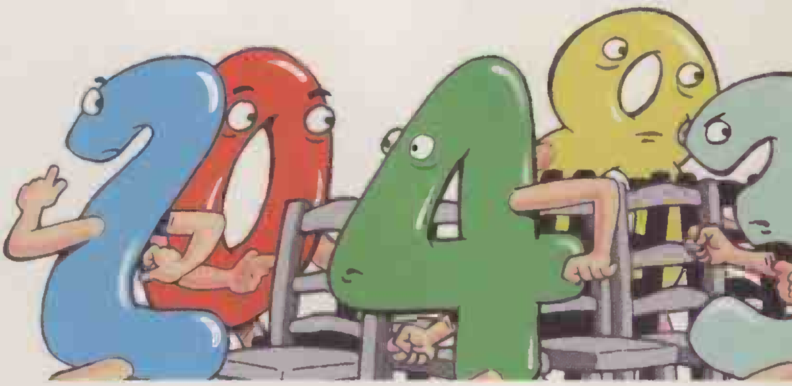
The huge take-up of mobile phones – and the transfer from old subscription accounts to new pay-as-you-talk numbers – are putting the existing system under further strain. This could have been minimised if transferring customers had been allowed to retain their old numbers. The service providers, whom OFTEL does not regulate, have declined to play ball, so the profligate solution is the creation of nine billion new numbers.

One thing Cruickshank's successor, David Edmonds, will not be doing is claiming this code change will be final. Not by a long chalk. Even though the 1995 code change was hailed by OFTEL as a numbering scheme for the 21st century, that was an impossible dream. All major cities that are not changing to 02 codes now will need to do so over the next decade. But two additional factors will inevitably bring further fundamental changes.

The first is the plan by the European Telecommunications Office (ETO) for a pan-European numbering scheme. According to the ETO, numbering is seen as, "a facilitator of telecommunications services," and a long-term numbering strategy should provide the means with which to achieve the goals of EU's telecommunications policy.

The strategy is also needed in order to prevent any initiatives that may impede the future implementation of this policy. Considered opinion sees this as a political pipedream that simply won't happen but it cannot be ruled out.

A more fundamental consideration is whether a telephone number should be treated as a name or an address. If I need to ring the editor of this magazine, I must first establish whether he's at home, in the office or perhaps on his mobile – and then ring a different *number* for each. If I send him an e-mail, however, a single *address* will reach him regardless of current location.



With the build-up of network intelligence in the telephone system, there are strong arguments for redefining phone numbers as addresses that are entirely location-independent. As well as providing greater user convenience, it would also provide much greater flexibility for conserving number resources but further change is inevitable and the pundits will have their work cut out to avoid making fools of themselves and of the users.

One man who was right all along, however, was Nick White, chairman of the TMA back in 1992. With considerable foresight he then said, "The topic of telephone numbering and code changes does not attract widespread attention but the planned changes are widespread and will hit every customer's pocket. Therefore any changes must be optimised by an expert planning and consultation process to minimise the cost of the changes to the customer and to deliver a solution that will last well into the next century." ■

Andrew Emmerson

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UPDATE

PCB makers worried over green tax plans

Circuit board manufacturers have warned the government of the impact on UK factories of its plans to introduce an environmental tax levy in April next year.

PCIF industry trade association director, Brian Haken said that the Chancellor's plans to collect £1.9bn in the first year means that manufacturers could go offshore and board makers will go with them.

Haken said that the government was not sufficiently aware of the contribution made by the smaller PCB manufacturers. "The industry is restructuring rapidly. There were 450 PCB companies in 1990. Now there are 135, and by 2005 there could be between 15 and 20,"he said.

He added: "The increasing costs of production equipment has meant that the number of companies that can afford to stay in the business will fall."

Haken, who was talking at the launch of an environmental best practice guide, does not disagree with the EU's Waste from Electrical and Electronic Equipment Directive in principle but he believes the way it is being implemented will cost UK PCB manufacturers dear.

"It is estimated that compliance costs around two per cent of total (manufacturing) cost already, and this rises to seven per cent for the PCB sector - off the bottom line, bringing the UK industry total to around £40m a year," said Haken.

The guide highlights areas of cost saving, such as recycled water and the reduction of tin and lead.

Kingston launches ADSL-based television service

Europe's first ADSL-based interactive TV service was launched by Kingston Communications recently.

The Kingston Interactive Television service provides digital TV broadcasts, video on demand, fast Internet access and interactive services.

Initially 1550 Kingston customers will receive the service. A phased rollout to Kingston's 155 000 customers in Hull and east Yorkshire will then follow.

"This announcement maintains our position at the forefront of ADSL," said Steve Maine, Kingston Group's chief executive. "It is a universal technology – there are 800 million copper telephone lines globally – and we believe the kind of services we are offering will be adopted worldwide."

Newbridge Networks is providing the media distribution systems which combines ATM switching, ADSL technology and IP routeing. The services will be provided at data rates of up to 4.5Mbit/s.

● Kingston has just announced its interactive tv pricing structure, which includes the UK's first tv-based untimed high-speed Internet service – log on at up to 256kbit/s for £15 a month with no phone-call charges.

Multimedia future for phone networks

The end of traditional telephone networks based on circuit-switched transmission technology has been predicted at the world's biggest telecoms technology showcase Telecom '99, which took place last October.

According to Yoshio Utsumi, secretary general of the International Telecommunication Union, the future development of the global telecoms industry lies in multimedia services and packet-switched data networks.

"Circuit-switched voice will disappear as the basic architecture of future telecommunications networks and be replaced by packet-switched data," said Utsumi, speaking at the opening of Telecom '99.

The main reasons for this fundamental change in network technology, says Utsumi, are the increasing convergence of voice and data telecoms traffic on networks and the growth of multimedia services. "Instead of having independent communication and information infrastructures we will see increasing competition between different multimedia services," he added.

Utsumi also hoped this technology change would mean that the most advanced telecoms systems would be, "...available, accessible and affordable for all the world's people rather than today's minority."

The exhibition, which is held every four years, has almost 1200 exhibitors and is expected to attract over 200 000 visitors.

Melanie Reynolds *Electronics Weekly*

Ten-fold density boost for optical storage

An Israeli company has begun demonstrating a new type of 3D optical data-storage technology with its fluorescent multi-layer card (FMC) technology. The company called C3D claims a standard 120mm optical disk using the FMC technology could hold hundreds and potentially thousands of gigabytes of data. It is planning to demonstrate the system in the US to build support for its technology which it claims is cheaper than current optical data storage systems by as much as ten to a hundred-fold.

Pentium look-alike clocks 700MHz

Advanced Micro Devices (AMD) will announce this week its 700MHz Athlon microprocessor as it tries to maintain a performance lead over rival Intel. The announcement of the chip is expected to be accompanied by design wins from IBM and Compaq Computer. Intel is close behind AMD and will introduce 700MHz and 730MHz Pentium III chips towards the end of this month.

Analog Devices' latest 16-bit DSP: there's more to power than a high clock speed

Kevin Leary is rarely surprised when it comes to digital signal processors. A member of Analog Devices' DSP division for 17 years, he has seen "a lot of things come and go".

For him if there is any significance to the current era, it is that DSP has reached a critical mass. "The marketing people don't like me saying it, but it is becoming commoditised," said Leary, Analog's DSP program manager.

In light of this, he argues that when judging a DSP, the issue is no longer its raw processing performance but myriad other factors too. This is what he believes Analog has achieved with its ADSP-219x family of DSPs.

In addition to its peak processing performance of 300Mips, the architecture builds on the existing software base by being code compatible with Analog's existing 16-bit 218x family. It has also been developed with design reuse in mind: "We need a core that is reusable across multiple groups within Analog, and potentially outside," said Leary.

The 219x family retains its forebear's single cycle instruction execution, zero-overhead looping and single-cycle context switch. What is new are compiler and processing enhancements.

To aid the compiler, the 219x provides up to 16Mword paged memory support. "This allows large data sets to be addressed. For Internet routers, the URLs and IP addresses can be ported directly onto the DSP," said Leary. The 219x treats memory as unified rather than segmented, making programming large systems easier. Five data address generation modes have also been added to improve compiler support.

The family's architectural enhancements include a doubling of the instruction pipeline depth to create a six-stage pipe with two-cycle delay. The adding of a transparent, 64-location two-way set-associative instruction cache enables an extra data operand to be loaded each cycle.

Tackling design reuse, Analog has chosen the open-standard ARM advanced high performance bus (AHB). "The state of intellectual property reuse is worse than people admit," said Leary.

He describes the bus as a synthesisable wrapper around the hard 219x core to which peripherals are interfaced. The bus has very good performance, said Leary: "Up to 100Mword/s [16-bit] and it is scalable to 128-bits wide."

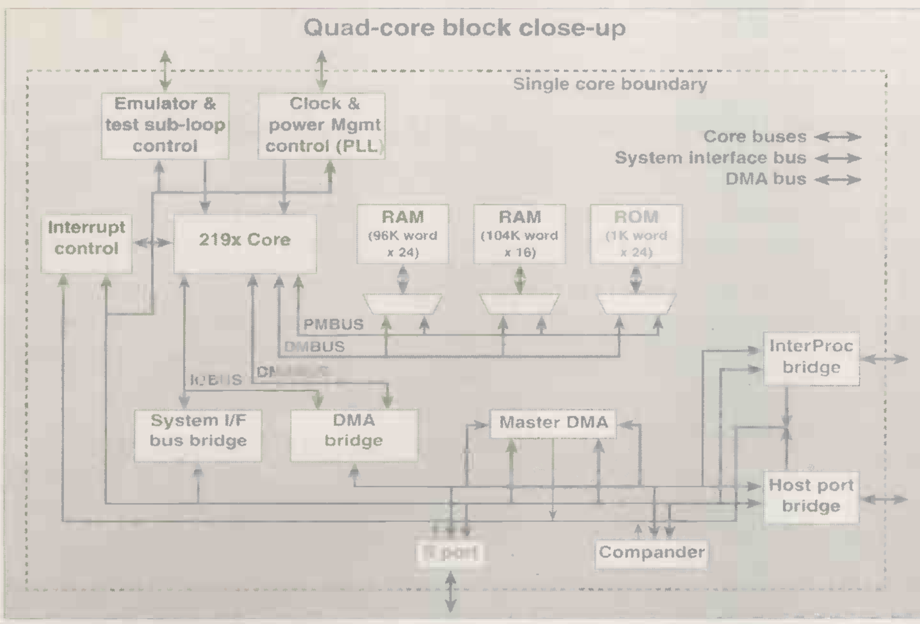
Analog has used the bus for its 10mm x 10mm mini-BGA IC which comprises four 219x 300MHz/300Mips cores and 16Mbit of embedded DRAM. The device is aimed at "ultra high subscriber applications", offering a processing performance of 1.2 billion multiply-accumulate operation/s.

Using this device, a processing density of 150 V.90 modem channels/in^2, or 200 Voice over IP channels/in^2 is achieved. Samples of the device are expected next March with volume production in a year's time.

Roy Rubenstein *Electronics Weekly*

ADSP-219x AT A GLANCE

- Up to 300MHz/300Mips processing performance
- Six stage hardware interlocked instruction pipeline
- Uses the ARMadvanced high performance bus (AHB) to aid design reuse
- The ARMAHB supports burst transfers, split transactions and single clock edge operation



Quad blockbuster... Analog Devices has put four ADSP-219x cores on a single chip. Each core is surrounded by a synthesisable wrapper – the ARMAHB bus – and has 4Mbit of local embedded DRAM.

Cheaper prototype PCBs

If you ask a PCB maker to produce you a prototype board, the chances are you will be charged for a piece of board big enough to hold nine Eurocards, regardless of the size of your prototype.

BetaLAYOUT is offering a service known as PCB-Pool. If you want just one Eurocard, Beta simply lays your design alongside that of other customers' and all share the cost of the raw board.

The first question you will probably ask is, "How long might I have to wait before Beta has enough customers to fill a board?" "Not long," is the answer – the company is currently fulfiling 1200 PCB-Pool orders a month. pcb-pool@beta-layout.com.

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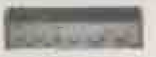

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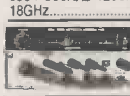

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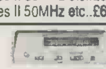

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Stretched memory capacity starts to hit supply...

Computer memory capacity may have to come down because the memory makers have no new factories coming on-stream – except for one.

At Infineon Technologies, Hans Pieter Bette, vice-president for memories, said: "We are 100 per cent full. We will do what we can, but to increase capacity quickly is impossible. We are not changing our initial plans." Infineon is relying on shrinks to increase output rather than new factory building. It is implementing a 'hefty' shrink from 0.22 to 0.19μm at its White Oak fab in the US.

At Hyundai/LG, Andrew Norwood said: "We have no extra capacity to bring on-line. The issues are: What effect will it have on the PC industry? And: Will we see PCs shipping with less memory?"

Agreeing, Helmut Schock, Toshiba's European memory boss, said: "If synchronous pricing goes much higher it will start to affect the number of megabytes used per PC. We will not increase production in big quantities because we're already running at high capacity." Toshiba had been running Rambus wafers, squeezing synchronous DRAM production, but now these are unsellable following Intel's Camino hitch.

Samsung is suffering similarly. "Like a lot of memory makers we were making Rambus DRAM but all that output now has to be stocked because we can't sell it", says Ken Jones, vice-president for marketing at Samsung, "Synchronous DRAM will be really tight in Q4 but what happens in Q1?" Samsung is building another fab but it won't produce product until the Spring.

Micron Technology is also full, but says it has the capacity to add another 20 000 wafers at its fabs in Avezzano, Italy and Miho, Japan – but, again, not until next Spring.

The one exception is NEC which opened a brand new fab in Shanghai in February. It is currently running 5 000 wafers per month, but this will be upped to 10 000 wafers per month from November 1999.

... and problems with Intel's Camino aren't helping

Intel's failure to bring out the Camino chip-set to implement the Rambus memory architecture has caused confusion in the PC industry and losses to dynamic RAM manufacturers who have been making Direct Rambus DRAMs. It has also worsened the existing shortage of conventional synchronous DRAM.

"A lot of memory makers were producing Rambus DRAMs," Ken Jones, v-p of marketing at DRAM market leader Samsung, told *EW*, "but the capacity now has to be stocked because we can't sell it. Because we've been making Rambus, we have had less capacity for synchronous.

"However, personal computer companies have gone off Rambus because, without Camino, they can't make Rambus PCs. As a result, demand for synchronous has gone up. Synchronous will be really tight in the fourth quarter of 1999."

At Toshiba the situation is much the same. "We've been making Rambus but it's been delayed for some time – maybe for another quarter – so we are moving production to synchronous," said Helmut Schock, Toshiba's memory boss for Europe.

According to DRAM price trackers ICIS-LOR, the price of a 64Mbit synchronous DRAM rose from $6.50 in the first week of September to over $17 last week. With every DRAM manufacturer at full capacity and much of Taiwan off-line for the time being, prices may increase.

One result is, says Schock: "It will start to affect the Mbytes per PC". Andrew Norwood of Hyundai asked: "Will we see PCs shipping with less memory?"

Camino was originally supposed to ship in August. Technical hitches delayed it. Then Intel announced last week, on the same day it was due to roll it out, that Camino still had problems.

The result is confusion. "What's going to happen in Q1 in 2000," asked Samsung's Jones, "will Rambus be fixed? Should we be making Rambus DRAMs or synchronous? It takes a couple of months from wafer-in to product output."

Controllers go wireless

Texas Instruments has announced a microcontroller and RF chipset aimed at adding low cost wireless links to products such as utilities meters, security systems and consumer products.

A combined standby power consumption of only 4μA makes it possible to build metering applications that can operate for more than five years from a single lithium battery, TI claimed.

Combining a 16-bit Risc processor and an 850 to 950MHz RF transceiver, the two chip system will enable data rates of up to 200kbit/s.

TI claims the chipset allows designers to build a complete system with a bill of materials costing under $6.

Mobiles to outstrip fixed

Mobile phone users will out number fixed line telephone users in the world as early as 2001, according to figures published by the International Telecoms Union (ITU).

In a report the ITU predicted that the number of mobile phone users will overtake fixed telephone lines around the world sometime between 2001 and 2007.

It stated that there will be more than half a billion mobile phones in the world by the end of next year, this is almost double the number just a year ago.

Transistors reach physical limit

Intel research engineers are warning that the chip industry faces a potential problem in shrinking the size of transistors as they approach fundamental physical limits. In a recent article in *Science* magazine, Paul Packan, a research engineer at Intel, said that there is as yet no way around basic physical limits to shrinking transistor features.

This could mean a slowing of Moore's law, which describes a doubling of chip transistor counts every 18 to 24 months. ■

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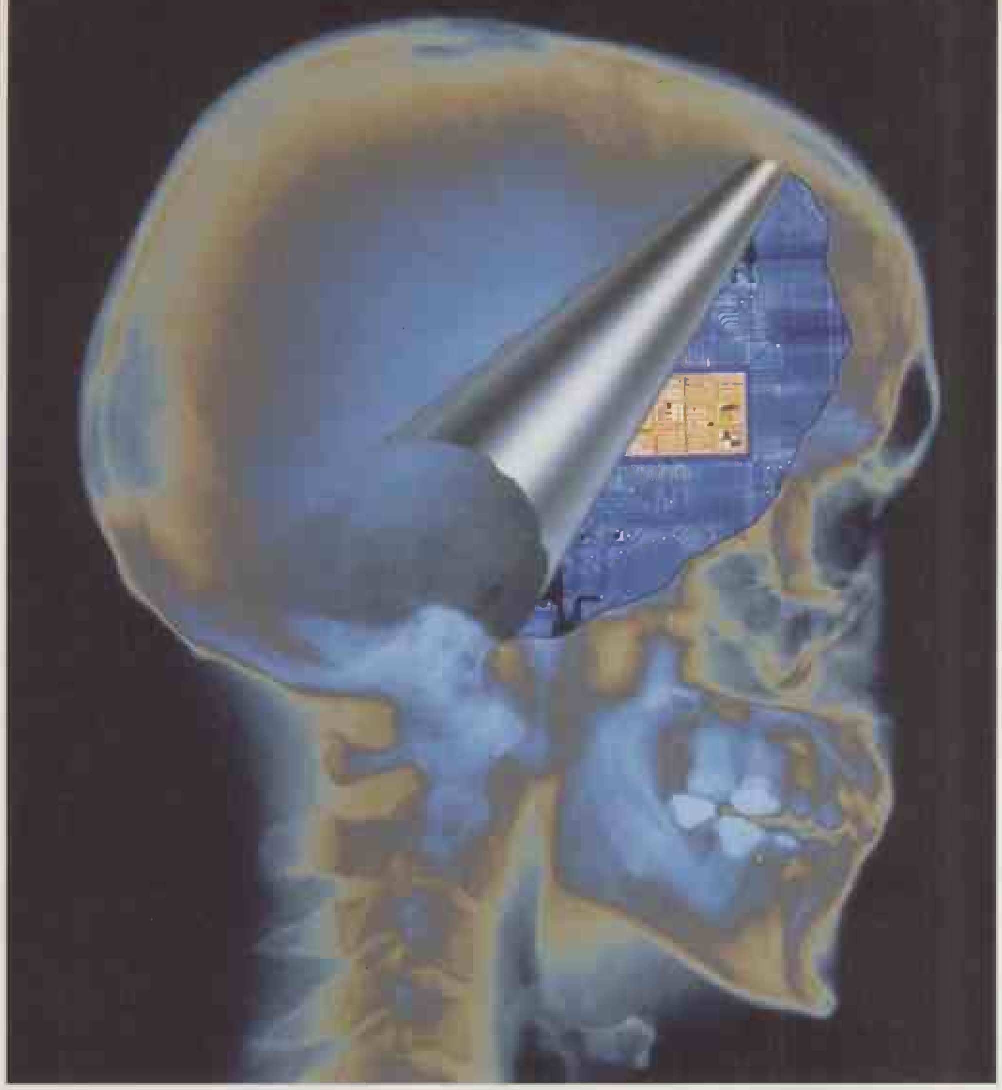

Intelligent signal processing

DSP, neural networks and time series – Chris MacLeod and Grant Maxwell look at how artificial neural networks can benefit signal processing.

Artificial neural networks are one of the corner stones of modern artificial intelligence, or AI. Over the past year we have written two articles in *Electronics World* on their relationship with the more familiar aspects of electronics.

The first article in the June 1998 issue, dealt with their connection with digital electronics. The second, in the November 1998 issue, discussed how modern techniques are bringing us closer to systems that display real intelligence.

In this article we look at their relationship with signal processing technology – in particular with digital signal processing – and the importance of time-series signals to AI in general. These areas are of critical and growing importance to modern electronics. We will also tie up a few loose ends and try and show the 'big picture' of how the various technologies relate to each other.

Neural networks and DSP

In analogue electronics we use filters such as Sallen and Key circuits to process signals, in the digital domain the equivalent functions are performed by digital filters.

One of the most basic digital filters is the simple finite-impulse-response system. Several different filtering structures may be based on it. Such an FIR system can perform low-pass and high-pass type functions, **Fig. 1.** Those of you not familiar with DSP or wanting to brush up your skills should refer to the excellent book by Ifeachor and Jervis[1].

The difference between the filter and a standard neuron of the type commonly used in artificial neural networks is simply the delay line with unit delays Z^{-1} and the fact that the filter operates without a threshold or activation function. You might find it interesting to refer back to our first article to look at the model of the artificial neuron. In the case of the filter, the coefficients h(n) are found using one of the standard design methods; in the artificial neural network they are learnt by the system.

A closer look at this system will help us to understand, at a much deeper level, what is happening. Previously, we pointed out that the artificial neural network was a mapping system; it takes one data distribution and maps it onto another – as combinational logic does – but with two important differences. Firstly, it maps continuous data and secondly, it can learn the mapping without need of a designer. This mapping capability is often used to produce artificial neural networks, which can recognise patterns by mapping the pattern onto a predetermined set of answers.

The effect of the unit delays in the filter above is to provide a 'snap shot' of the data, sampled at unit intervals, to the summation unit, i.e. neuron. In other words, it converts a time-varying signal into a spatial signal. The neuron can now process this data according to the mapping it has learned.

It should be quite clear that the artificial neural network and the FIR filter are therefore simply the same system viewed from different technology perspectives. One maps spatial data patterns, the other – with the aid of time delays – maps temporal or time series data.

Extending these basic ideas

By understanding the fundamental relationship described above, one can expand the ideas behind DSP filters and artificial neural networks further.

For example, you can use a network of neurons. This allows the system to produce more complex mappings than the single neuron[2]. This idea is shown in **Fig. 2**. In the literature, it is sometimes referred to as a 'time-delay artificial neural network'; another appropriate term might be 'neuro-filter'. In fact, all the common DSP functions from comb filters to autocorrelation functions may be represented as neuro-filters.

The system can learn the mapping

using one of the common artificial neural network training rules such as back propagation[3]. In fact the algorithms that have been developed for implementing adaptive filters – filters which can change their parameters in use – are identical to back propagation[1,3]. This is another example of technological convergent evolution.

It is also possible to map one time series to another, as in **Fig. 3**.

Benefits of more layers

Adding another layer of neurons into the system allows more complex mappings to be performed. A three-layer network can theoretically perform any mapping – provided that there are enough neurons present. However, there are practical problems with this because of limitations in the learning algorithms.

The networks discussed so far have no feedback loops; the infinite impulse response (IIR) filter is the equivalent of the Hopfield neural network[4]. The importance of the Hopfield type of network is its ability to store a mapping and recall it when presented with an incomplete version: compare this to sequential digital logic. In other words, apply a corrupted signal to a Hopfield-based neuro-filter and assuming that the filter has learnt the correct version, it will reproduce it.

Adding another layer of neurons into the same structure will allow one time series to map onto another, independent series. This is the equivalent in artificial neural network terms of the network known as a 'bidirectional associative memory, or BAM[5].

These ideas can extend the use of DSP beyond its current application in filtering to much more complex mapping functions.

Filtering in the brain?

The brain is a mass of 100 billion neurons; its structure has been formed by evolution over hundreds of millions of years. Because evolution is 'blind', it will simply form the best structures to perform a function regardless of their topology.

A small amount of thought shows that it is very likely that temporal filtering structures of the type discussed above are present in the nervous system. They could certainly be implemented quite easily, as in **Fig. 4** for example.

You can see from this that, to make a general neural network, another component is required – that of the time delay.

The dynamics of the mind

Quite apart from the filtering illustrated in the previous section, time series signals also play a deeper role in the operation of the brain and are perhaps vital to consciousness itself.

Information in the nervous system is transmitted as pulses called 'action potentials', **Fig. 5**. These encode information by pulse frequency modulation[6] – and possibly pulse position modulation. This is in marked contrast to the way signals are represented in most artificial neural networks. As we will show, the difference may be critical, both to understanding the nature of thought and to synthesising electronic circuits that can mimic it.

The story starts with W. J. Freeman who was studying the olfactory (smell) system in rabbits[7]. He found that each smell was encoded as a distinct pattern of pulses moving around the network, never exactly repeating itself – a chaotic attractor.

It has been suggested that thought itself may be just such a pattern of pulses evolving and changing over time or in response to sensory input. In this view of the brain, therefore, it is not the wiring of the system that is important, or even the functionality of the building blocks. Rather it is the dynamics of the signals and how they interact with each other and the outside world.

We know that dynamic signals are important in the nervous system. Just think of how you breathe or how your heart always beats – a good example of a neuro-generated pattern.

Sensory deprivation

Further illustration is given by, for example, sensory deprivation. When the human body is deprived of sensory input, the brain goes wild, causing vivid dreams and even hallucinations. This can only be explained if the brain generates its own activity in the absence of sensory input.

Notice the marked contrast with artificial neural networks, which are usually designed to be stable and damp down any dynamic activity. They generally use a data representation not suitable for this type of activity anyhow.

A train of thought or a stream of consciousness is then a moving and

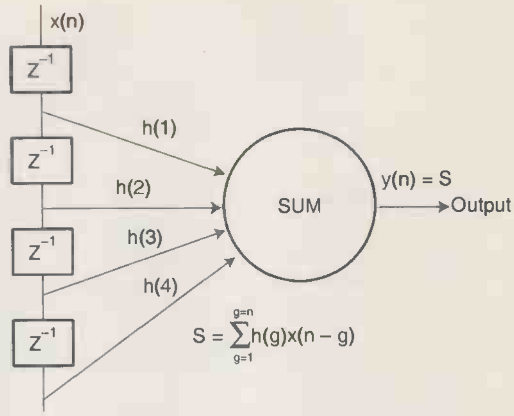

Fig. 1. A simple FIR filter shown in its transversal form. Variable n *is the number of delay units.*

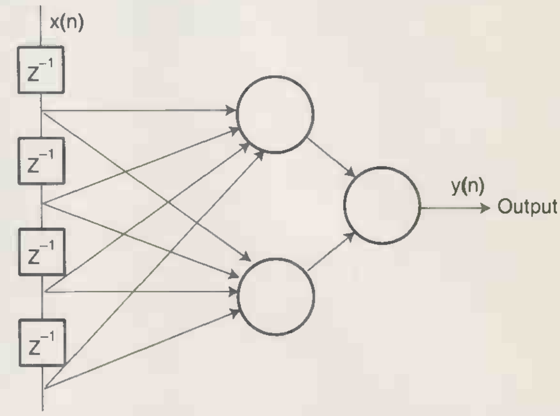

Fig. 2. A signal processing system using several neurons.

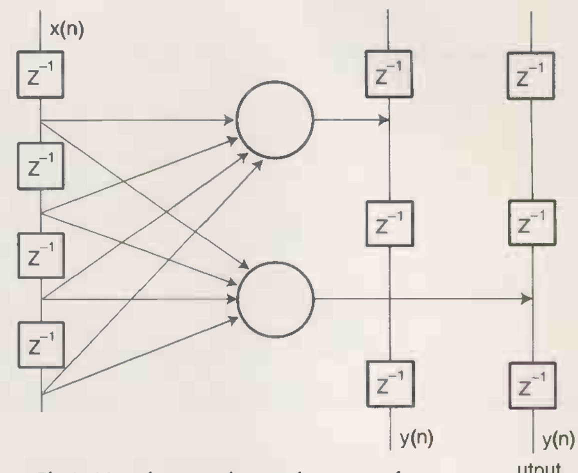

Fig 3. Mapping one time series onto others.

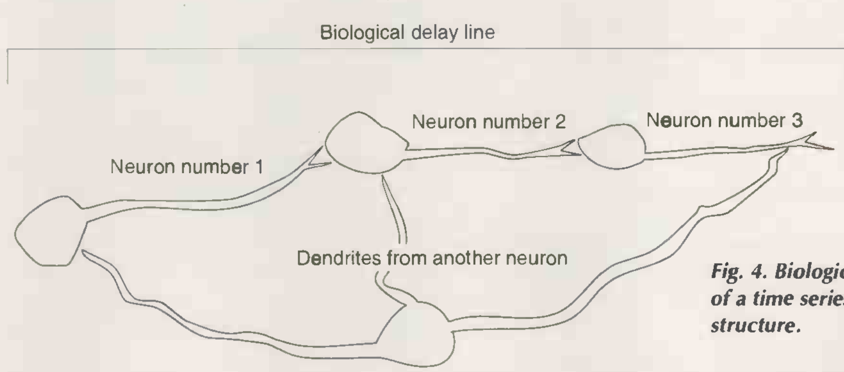

Fig. 4. Biological equivalent of a time series filtering structure.

changing pattern of pulses, themselves made up of individual action potentials rushing hither and thither through the network. These pulses and therefore patterns may be altered in a number of different ways:

- By sensory input. This may have the effect of clamping the signals into a more rigid pattern.
- By the connections between the neurons themselves strengthening or weakening.
- By other feedback learning mechanisms.

Simulating complex dynamic patterns like these may help us to further understand the operation of the mind and also open applications and systems in advanced electronics.

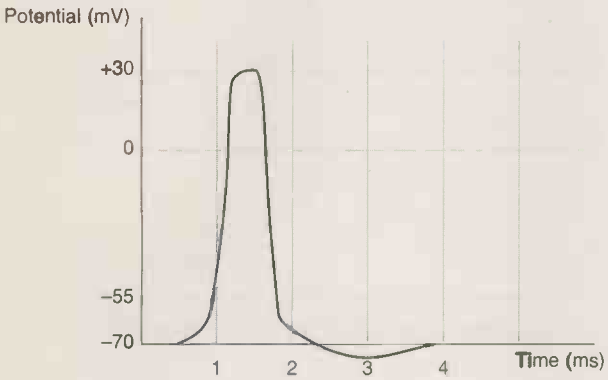

Fig. 5. An action potential – the brain's information carrier.

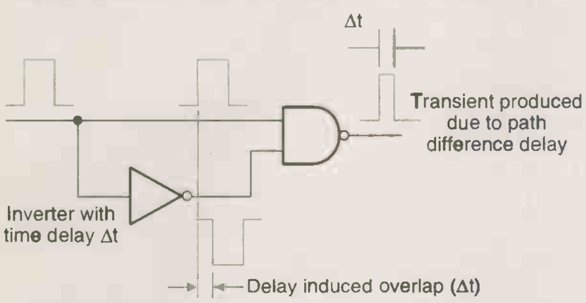

Fig.6. A timing induced glitch. Normally something we would try to avoid.

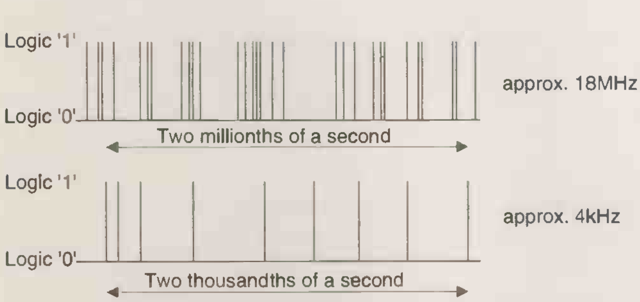

Fig. 7. At the start of the evolution process, the waveform looks like that shown in the top diagram. After evolution we have a good 4kHz oscillator. After Thompson, reproduced with permission.

Simulating complex dynamics using digital electronics

In our previous article, we described how Adrian Thompson of the University of Surrey (http://www.cogs.susx.ac.uk/users/adrianth/ade.html) has used a technique called the 'genetic algorithm' to synthesise interesting digital circuits[8].

The circuits that Adrian produced are unusual in that to create their signals they operate asynchronously and use gate delays to produce complex outputs, as shown in **Fig. 6**. In other words they are not so much using the normal AND, OR and NOT functions, as the spikes, glitches and hazards that we normally strive to avoid!

These anomalies interact to produce the required output. The genetic algorithm is effectively designing the circuit.

Figure 7 shows how the outputs change as the circuits evolves. In this case the object was to produce a 4kHz oscillator; **Figure 8** shows the actual circuit evolved. The circuit itself is difficult to analyse, its function having been dictated by evolution rather than design. Of course it is also possible to program the genetic algorithm to select networks that display programmability and stability.

The operation and output of these circuits bears a striking resemblance to the action potentials rushing around the brain. More importantly, this type of system may give us the opportunity to explore exactly the type of dynamics that were discussed above. This in turn may lead to a better understanding of brain function and the role of dynamics in biological and artificial intelligence.

Although Thompson uses gates to achieve this effect, further development of these ideas may be made easier by using specially constructed combinational elements of other types and variable delays.

A changing dynamic can also be added into this type of simulation by making the circuit delays variable. These delays can then be effected by outside learning signals, re-enforcement type strengthening or sensory input, so causing the patterns themselves to change in response to sensor and learning influence.

Tying it all together

We hope that in this, and the previous articles, we have managed to show that the different technologies – spatial mapping in the first article and temporal mapping and complex dynamics in this current one – are all aspects of the same general system. They are all synthesised from simple, basic building blocks.

Electronics can learn much from these natural examples and the relationship between the functions should be considered an important topic for research[9].

We said in our first article that there is a general theory of electronics, a new electronics, hiding behind the individual parts. Electronics can also learn other important lessons from biology. For example, current trends are for research into smaller and faster chips. Biology shows that where we should really be heading is for three dimensional circuit layout. This is what gives the brain its amazing packing density, although this may require a paradigm shift, for example in the development of self-wiring, or self-routeing circuits.

In the case of biology, evolution knows only that it must define networks which work and so different levels of the system may operate in different ways – some as simple mapping networks and others as complex dynamic systems.

It is likely that biology uses them all. There are certainly indications that many of the lower, reflex-type actions are carried out by simple mapping networks, while the higher functions are complex dynamic systems; evolution is blind, it knows not which are which. It will use them all – and so will any technological attempts to design truly intelligent circuits.

For more discussion, visit our web site:
http://www.eee.rgu.ac.uk/research/neural/welcome.htm

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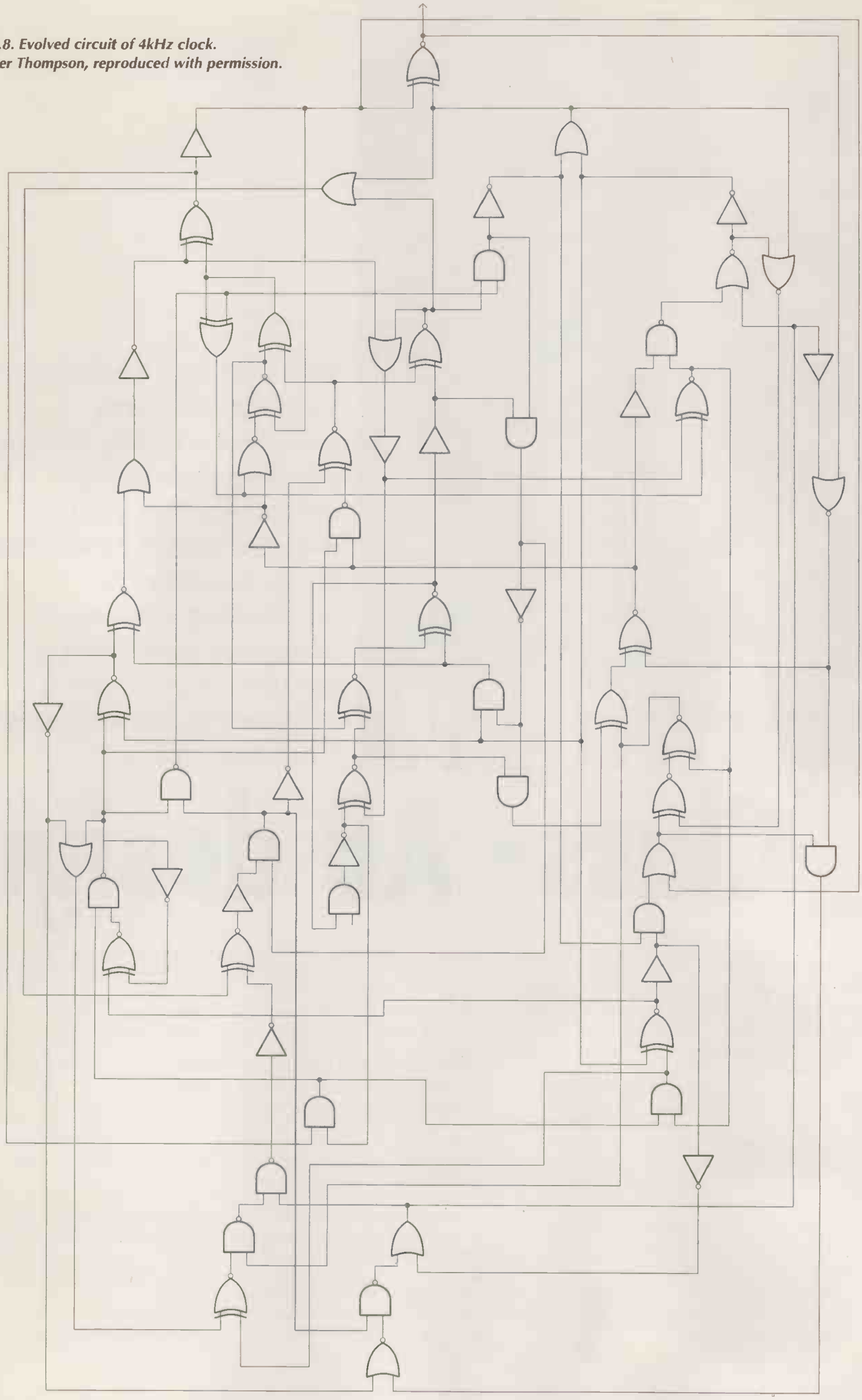
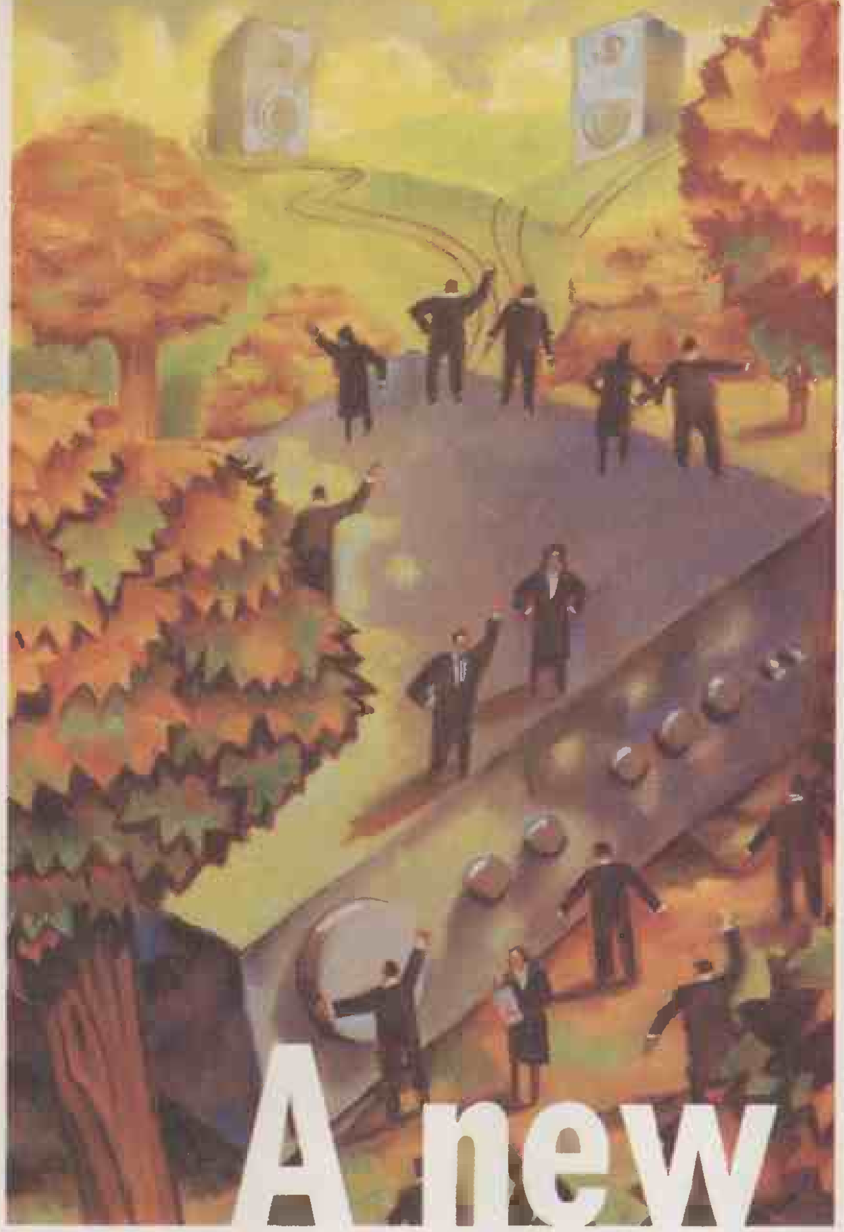
Fig.8. Evolved circuit of 4kHz clock.
After Thompson, reproduced with permission.





This Class-AB audio power amplifier features excellent stability without needing stabilising networks. The design incorporates a new driver-stage topology for eliminating crossover distortion and it has a saturation-preventing scheme for fast recovery from clipping.

A new Class- AB design

The authors...
Wim de Jager,
Erik van der Ven and Ed van Tuyl, University of Twente, Enschede, The Netherlands.

An important problem encountered in class-AB audio amplifier design concerns the bias-control loop. Often, a complementary common-collector output stage is used[1] and the power transistors are included in the bias control loop. This can easily cause thermal instability due to the large temperature variations in the output transistors.

Thermal coupling of all diodes and transistors in the class-AB control loop can improve the thermal stability of the quiescent current in the output stage, but this is in most cases too slow to react to burst signals. As a result, emitter resistors are usually added to the power transistors to improve thermal stability. However, the voltage drop across the emitter resistors can switch off the transistor that is conducting the residual current.

Because of the limited bandwidth of the distortion reduction by means of using negative feedback, transistor switching can be a source of high-frequency distortion. Additional circuitry is necessary to prevent this[2]. Moreover a common-collector stage is not able to reach a rail to rail voltage output swing due to the base-emitter voltages.

Common-emitter output stages are usually based on a complementary feedback pair[1]. However the local feedback loop around the pair can be a source of HF oscillation.

In order to achieve thermal stability without switching problems, and to allow maximum output voltage swing, we designed a common-emitter power amplifier based on a new current-mode class-AB driver circuit. Due to the absence of local feedback at the output, the stability of the amplifier is only dependent on the global feedback-loop.

The design encapsulated

This is a three-stage class-AB common-emitter power amplifier using discrete bipolar transistors.

Thermal stability is achieved and switching distortion is avoided by using a new current mode class-AB driver circuit.

Total harmonic distortion varies from 0.01% at 20Hz to 0.1% at 20kHz driving 30W into 8Ω.

A phase margin of 85° for a β of 1/34 guarantees excellent stability without load stabilising networks.

Saturation of the power transistors is prevented, resulting in fast recovery from clipping.

Common-emitter design

The open-loop output impedance of a

common-emitter amplifier is inherently high, but can be lowered by applying negative feedback.[3] As a result, the output resistance becomes inversely proportional to the transconductance, g_m, and the feedback factor,

$$R_{out} = \frac{1}{g_m \beta} \qquad (1)$$

In order to obtain a closed-loop gain of 34, the feedback factor must be 1/34.

For an output resistance of 30mΩ the transconductance should be approximately 1000A/V. This requires a cascade of at least three gain stages: an input transconductance stage and two current gain stages.

How it works

The simplified circuit diagram of the amplifier is depicted in **Fig. 1**. Its input stage, consisting of a differential transistor pair, $Tr_{1,2}$, and a current mirror, $Tr_{3,4}$, converts the differential input voltage to a single output current. This current feeds the base of driver transistor Tr_9 and via the common base transistor Tr_8 feeds the base of the driver transistor Tr_{10}. The driver transistors supply their emitter currents to power transistors Tr_{11} and Tr_{12} respectively.

Biasing and class-AB control are achieved by means of a bias-control loop formed by $Tr_{6\text{-}9}$. Due to the buffer function of Tr_6 the base-emitter voltage of the power transistor Tr_{11} is isolated from the bias control loop. This is done to avoid thermal or HF switching distortion problems mentioned earlier.

This design is based on complementary n-p-n/p-n-p transistors. Their parameters can be assumed equal to make the equations easier. The class AB control is based on the well-known geometric class-AB control law,

$$I_{C8} \times I_{C9} = I_R^2 \qquad (2)$$

The DC collector current of the driver transistors is given by,

$$I_{C9} = I_{C10} = I_R \sqrt{h_{FE}} \qquad (3)$$

Collector terminals of the driver transistors $Tr_{9,10}$ connect to the output terminal to minimise driver dissipation and to prevent the power transistors $Tr_{10,12}$ from saturating.

Power dissipation in the bias-control loop transistors is low compared to the dissipation in the output transistors. Hence, if $Tr_{6\text{-}9}$ share a small heat sink, thermal stability is achieved without emitter degeneration and switching distortion.

The remaining dominant source of temperature dependence is the temperature coefficient of the power transistor forward current gain. This coefficient

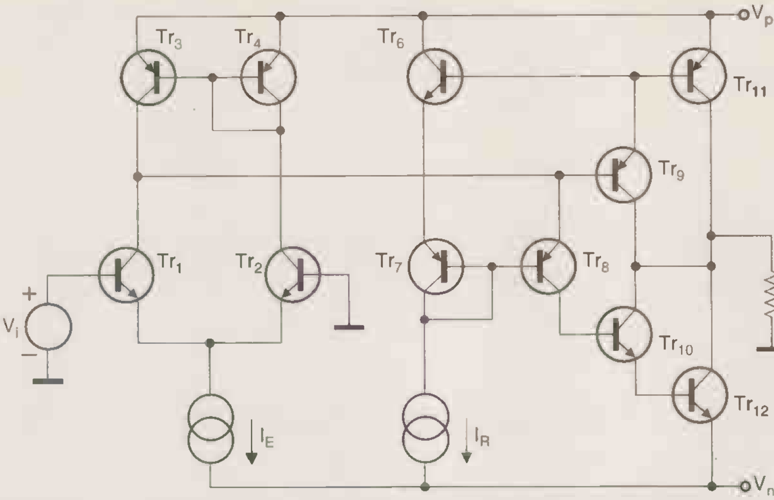


Fig. 1. Simplified circuit diagram of the Class-AB amplifier featuring new driver stage.

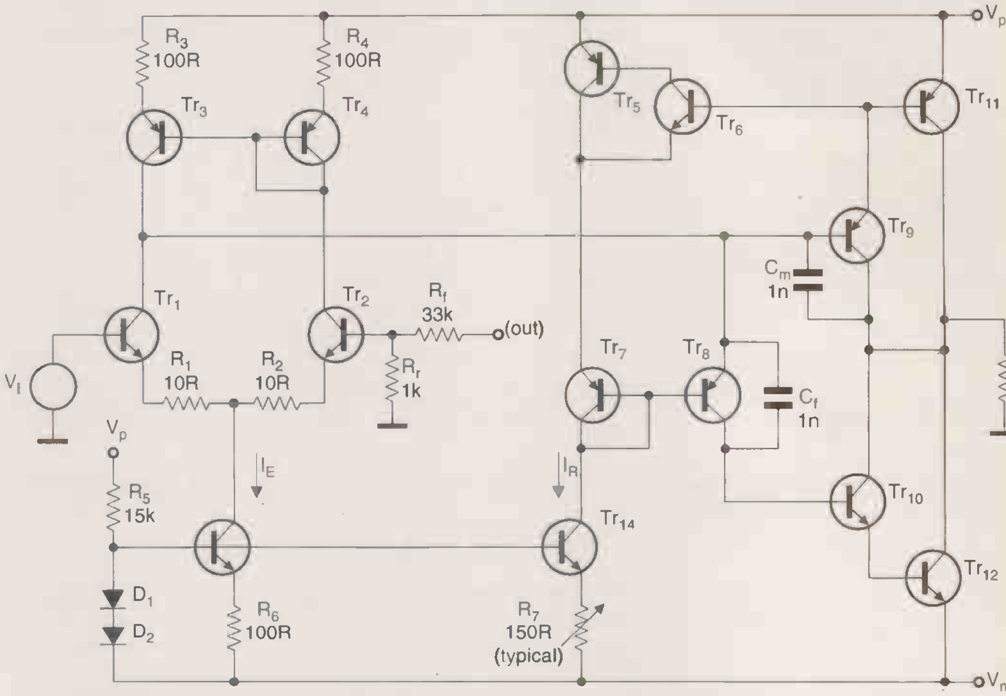


Fig. 2. Complete amplifier, as used for the PSpice simulations discussed in the article.

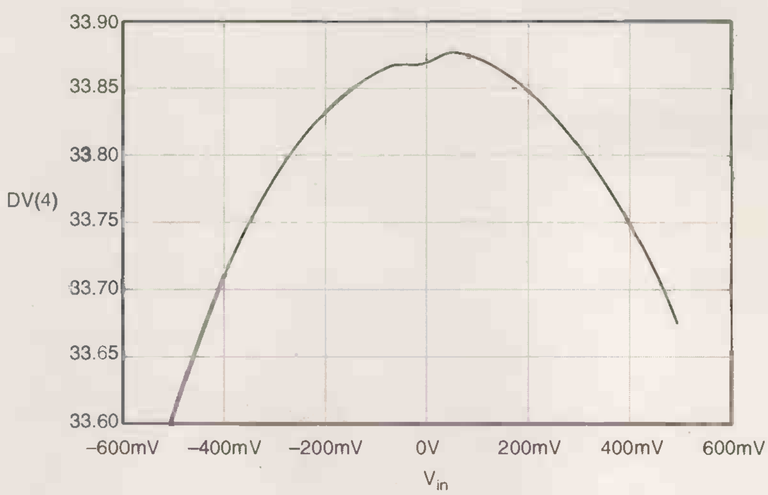


Fig. 3. Closed-loop voltage gain simulated using PSpice.

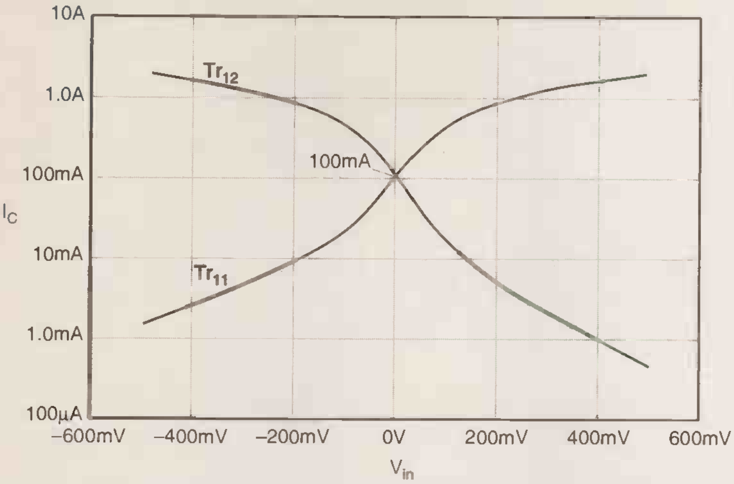


Fig. 4. Residual currents in the output transistors are well controlled.

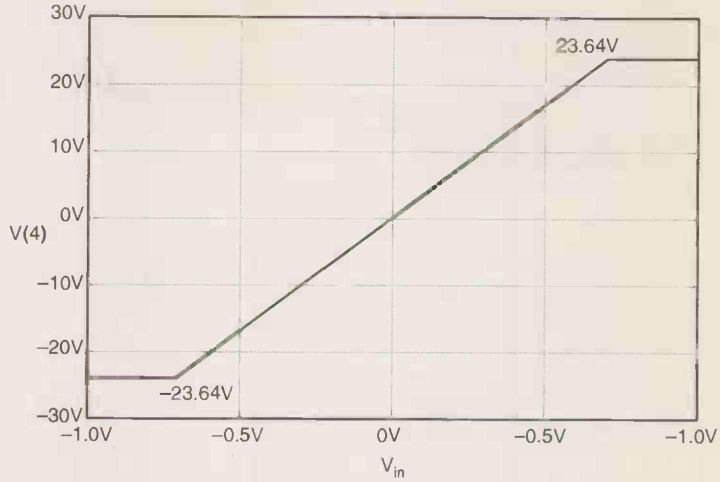


Fig. 5. Curve for output voltage swing shows that this design can drive close to the ±25V supply rails.

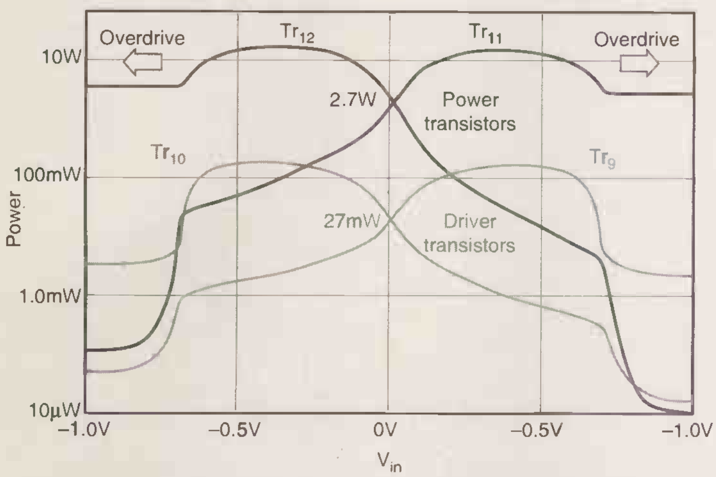


Fig. 6. Dissipation of the power transistors when overdriven illustrates the efficiency of the bias control loop.

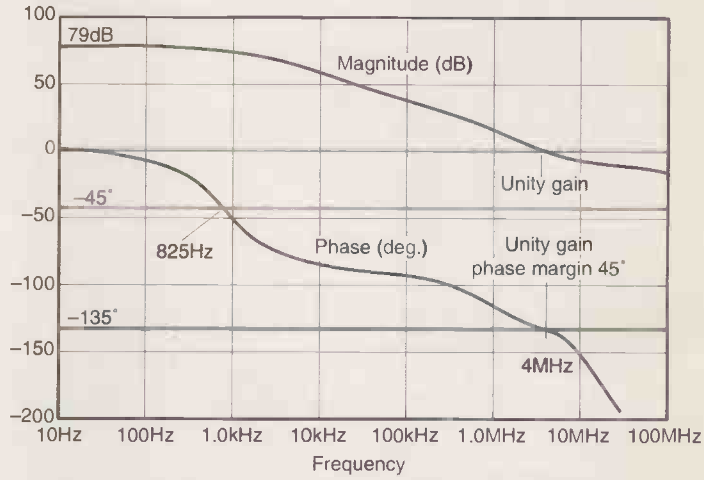


Fig. 7. Open-loop gain and phase characteristics for the amplifier.

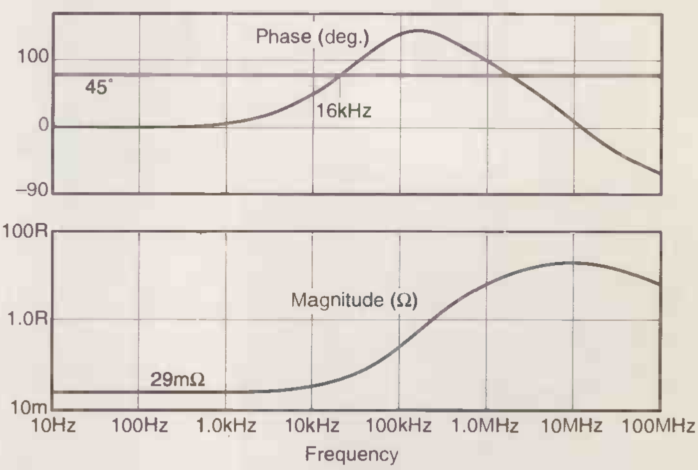


Fig. 8. Magnitude and phase plots of the output impedance.

is approximately 0.6%/K[4]. Maximum output current is determined by emitter current and the current gain of $Tr_{9,11}$ or $Tr_{10,12}$ respectively,

$$I_{O(\max)} = \pm I_E h_{FE}^2 \qquad (4)$$

It can be seen that, in contrast with many other designs, the maximum output current capability is symmetrical.

Optimisation

Figure 2 shows the complete amplifier as used for our PSpice simulations. Adding Tr_5 simplifies equation (3) to,

$$I_{C9}=I_{C10}=I_R \qquad (5)$$

As a result, the quiescent current of the output stage is,

$$I_{C11}=I_{C12}=h_{FE}\times I_R \qquad (6)$$

Note that the maximum available base current for Tr_8 is increased with a factor square-root h_{FE} and the accuracy of the bias control loop is increased too.

Capacitors C_m and C_f perform frequency compensation. Capacitor C_m is a Miller capacitor, compelling the open-loop transfer to a first-order frequency behaviour. Capacitor C_f forms feed-forward frequency compensation around the common-base connected level-shift transistor Tr_8.

Currents I_E and I_R are determined by V_{diode}/R_6 and V_{diode}/R_7 respectively. Emitter degeneration – R_1 and R_2 added to Tr_1 and Tr_2 respectively – is used to increase the amplifier's input voltage range to reduce transient intermodulation distortion.

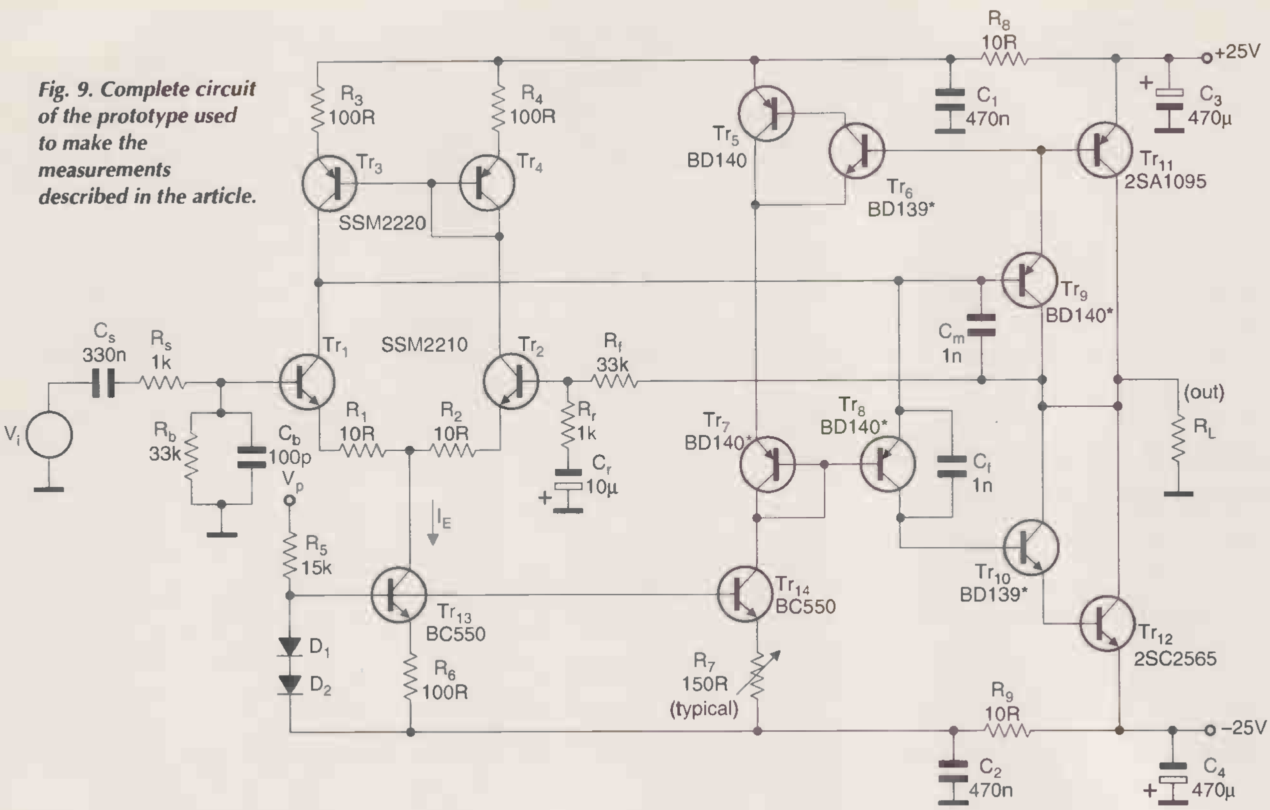


Fig. 9. Complete circuit of the prototype used to make the measurements described in the article.

Simulations and measurements

For a 40W/8Ω design of the common-emitter power amplifier of Fig. 2, the supply voltages are: V_p=25V and V_n=–25V. For R_6=100Ω, giving an emitter current of around 6mA, and a Miller capacitor of 1nF, the calculated slew-rate is 6V/µs. The corresponding full-power bandwidth is approximately 40kHz.

We simulated the circuit of Fig. 2 using PSpice. By adjusting R_7 the quiescent current of the power transistors Tr_{11} and Tr_{12} was set to 100mA.

Using equation (4), the peak output current is approximately 20A. The closed-loop voltage-gain of the circuit is depicted in **Fig. 3**. The nearly sym-

Fig. 10. The authors' prototype amplifier.

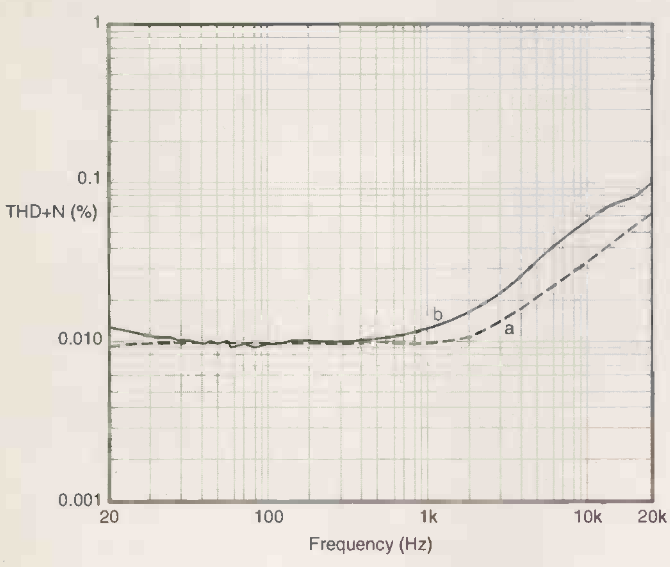
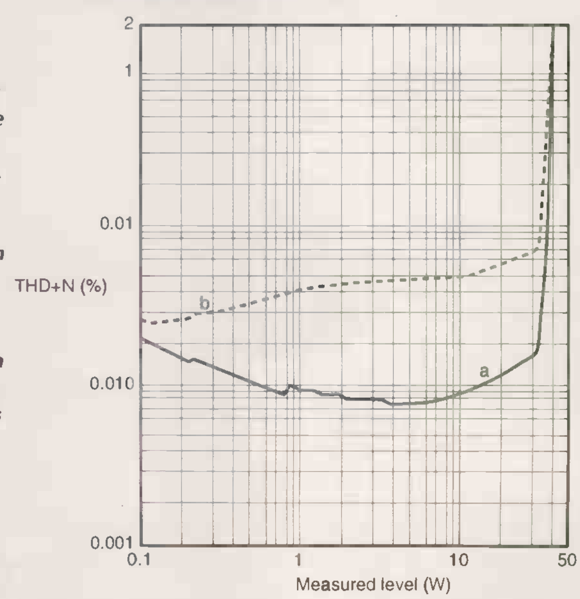


Fig. 11. Measurement of THD+noise versus frequency, a), and THD+noise versus level in watts, b). Curve a in a) is 1W, b is 30W. In b) on the right, a is 1kHz and b is 10kHz.



metrical shape of the gain-curve of the common-emitter amplifier is mainly determined by the h_{FE} roll-off of the driver- and power transistors.

Table 1. Measured performance versus PSpice simulation.

	PSpice	Measured
Open-loop gain	79dB	77dB
Open-loop –3dB b/w	825Hz	1150Hz
Closed-loop o/p imp. (mΩ)	29	30
Closed-loop o/p imp. 3dB	16kHz	14.5kHz

Residual currents in the output transistors of the common-emitter amplifier are well controlled, see **Fig. 4**.

As you can see in **Fig. 5**, the maximum output voltage of the common-emitter amplifier is close to the rail to rail limit. The dissipation of driver and power transistors in overdrive is shown in **Fig. 6**. This illustrates the low power dissipation of the bias-control loop used in the common-emitter amplifier.

Open-loop gain and phase characteristics, **Fig. 7**, show a unity gain phase margin of 45°. The phase margin for β of 1/34 is 85°. Magnitude and phase of the output impedance are given in **Fig. 8**.

Setting up

We implemented **Figure 9** on a pcb, **Fig. 10**, and used it for measurements.

By adjusting R_7, the quiescent current of the power transistors $Tr_{11,12}$ was set to 100mA. Note that due to the spread in transistor parameters, a manual control of the quiescent current is necessary. This is usual for power

Mathematical AC analysis of a common-emitter amplifier

In order to gain insight into the common-emitter amplifier, a mathematical AC analysis on a macro model like **Fig. A** can be used. Frequency-dependent behaviour of the open-loop transfer, the closed-loop output impedance and distortion are studied here.

The macro model of the common-emitter amplifier consists of a voltage to current converter, A_1, representing the input stage, followed by a current controlled current source, A_2, representing a two-stage current amplifier.

Miller capacitor C_m connects across the current-gain stage. The dominant source of distortion in A_2 is the current gain dependence of the emitter current – h_{FE} roll-off. This distortion is modelled by a current source connected in parallel with the output current source. The open-loop transfer function of the common-emitter amplifier can be written as,

$$H_C(s) = H_{C0}\frac{1-\frac{s}{z_{HC}}}{1+\frac{s}{p_{HC}}} \qquad (7)$$

where,

$$H_{C0}=G_1F_1R_L \qquad (8)$$

$$p_{HC} = \frac{1}{(R_L + F_1R_L + R_p)C_m} \qquad (9)$$

$$z_{HC} = \frac{1}{\frac{R_p}{F_1}C_m} \qquad (10)$$

Closed-loop output impedance is given by,

$$Z_{Cout} = Z_{C0}\frac{1+\frac{s}{z_{ZC}}}{1+\frac{s}{p_{ZC}}} \qquad (11)$$

where,

$$Z_{C0} = \frac{1}{G_1F_1\beta} \qquad (12)$$

$$z_{ZC} = \frac{1}{R_pC_m} \qquad (13)$$

$$p_{ZC} = \frac{1}{\left(\frac{F_1+1-G_1R_p\beta}{F_1G_1\beta}\right)C_m} \qquad (14)$$

Closed-loop frequency dependence of the distortion is given by,

$$\frac{V_{out}}{I_d} \propto \frac{1+\frac{s}{z_{DC}}}{1+\frac{s}{p_{DC}}} \qquad (15)$$

where,

$$z_{DC}=z_{ZC} \qquad (16)$$

$$p_{DC} = \frac{1+G_1F_1R_L\beta}{\frac{1}{z_{ZC}}+\frac{G_1F_1R_L\beta}{p_{ZC}}} \qquad (17)$$

Note that the pole frequency of the open-loop transfer, see expression (9), differs from the closed-loop zero frequency of the output impedance and the variation of distortion with frequency, see the expressions (13) and (16) respectively.

This is in accordance with the results found in simulations and measurements and verified by making a comparison between macro model results and simulations/measurements. Therefore numerical values used for the variables in the macro model expressions are derived from the PSpice output files,

G_1=50mA/V, R_p=4kΩ
F_1=driver h_{fe}.power h_{fe}=20000 (product of h_{fe}s)

The macro-model results on gain, bandwidth and output impedance fit quite well in with those found in PSpice and measurements in Table 1. The deviating value of the 3dB frequency of the output impedance and the frequency dependence of the distortion – 40kHz instead of 16kHz in PSpice – is caused by the simplification of leaving out the parallel capacitance at the input of A_2. This is carried out in order to make the expressions 7-17 simpler.

Adding C_p=800pF – extracted from PSpice – in parallel of R_p yields the far more satisfactory corner frequency of 20kHz.

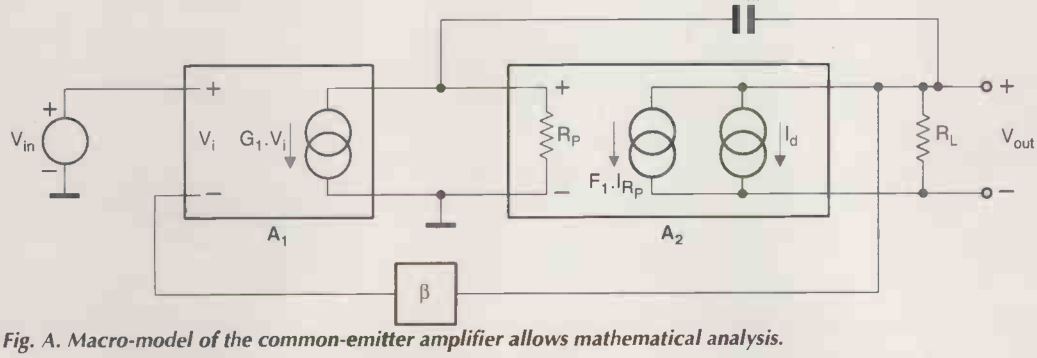


Fig. A. Macro-model of the common-emitter amplifier allows mathematical analysis.

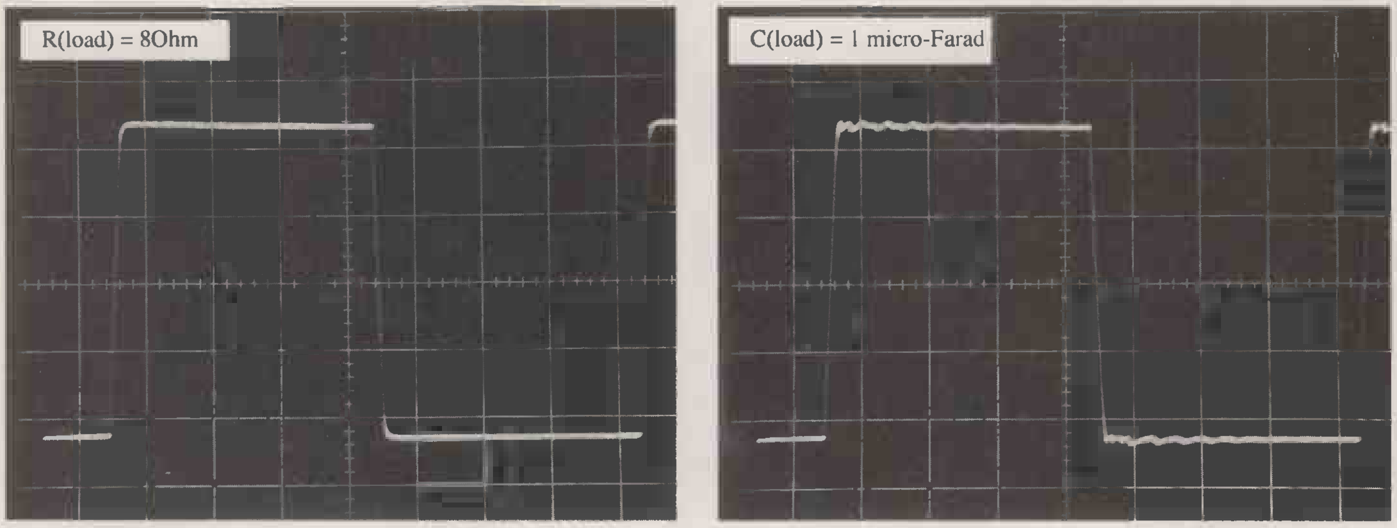


Fig. 12. These photographs of the square-wave response demonstrate the amplifier's stability. On the left, load is 8Ω, on the right, 1μF.

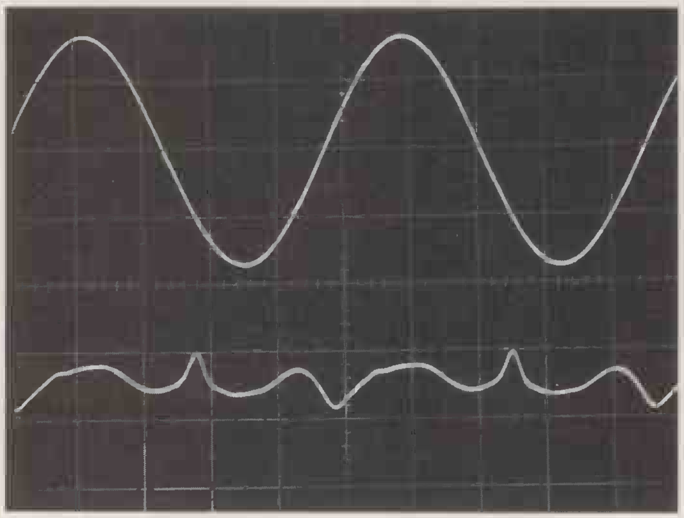


Fig. 13. Waveform resulting from driving the amplifier at 30W with a 20kHz sine wave illustrates the absence of switching distortion.

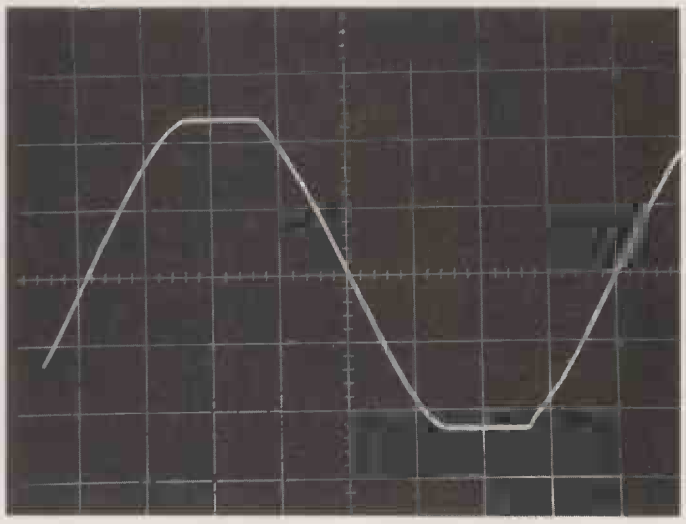


Fig. 14. Overdrive and recovery waveforms using a 5kHz input signal.

amplifiers based on discrete components.

Matched dual transistors, $Tr_{1,2}$ and $Tr_{3,4}$, a decoupling capacitor C_r, and equal values for R_b and R_f are used to minimise the DC offset.

A problem with power transistors driven by a current source is that there is no turn-off resistor for them. Under high-frequency, high-amplitude drive there will be a tendency for the effective bias current to rise dynamically.

By using HF power transistors with an f_T of 80MHz, this bias current rise is reduced to 60% at 20kHz at full drive.

Summary of measurements

The DC offset is 3.5mV and the slew rate 7V/μs. Distortion curves are presented in **Fig. 11**. Photographs of the square-wave response, in **Fig. 12**, demonstrate the amplifier's stability.

In the THD waveform at 30W, 20kHz, **Fig. 13**, no switching distortion occurs. The residual signal only contains low harmonics which are not very audible. Overdrive and recovery at 5kHz are shown in **Fig. 14**.

Thermal performance has been tested with an output power of 100W using a 1kHz sine wave and 2Ω load, which is 2.5 times the nominal value.

After two hours, the bias current rise was limited to 44 %, mainly due to the temperature coefficient of the current gain of the output transistors. This test confirms the thermal stability of the amplifier.

Table 1 is showing approximately equal results for PSpice simulations and measurements.

In summary

This class-AB common-emitter power amplifier incorporates a new current-mode class AB driver circuit to obtain good thermal stability of the quiescent current in the output stage. It also guarantees non-zero currents in the output transistor that is conducting the residual current, avoiding HF switching distortion.

Maximum output voltage is near to the rail-to-rail limit. Saturation in power transistors is avoided, resulting in fast recovery from clipping. The circuit has an excellent stability due to a phase margin of 85° with a β 1/34.

Finally, we would like to thank Elbert Kelholt, Eric Klumperink, Clemens Mensink, Rien van Leeuwen and Henk de Vries for their help in preparing this article. ■

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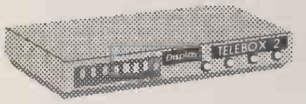

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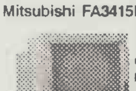

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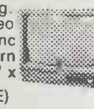

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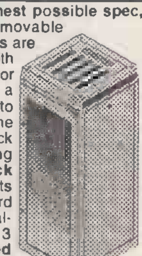

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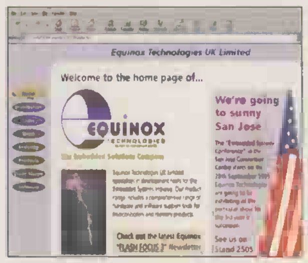

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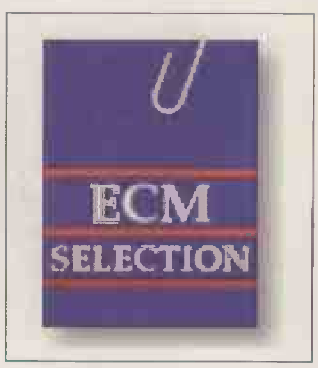

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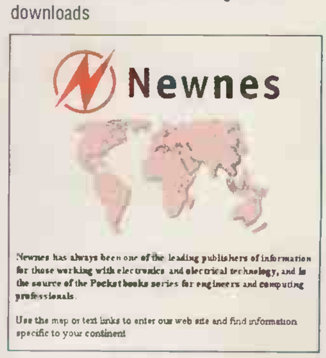

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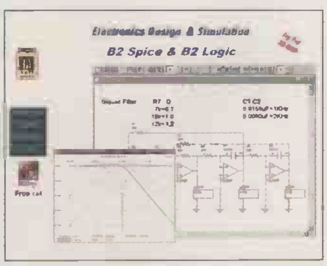

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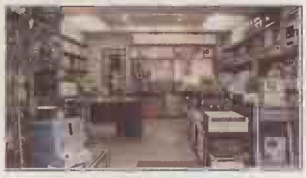

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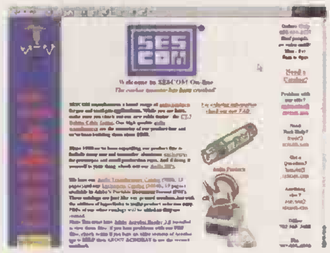

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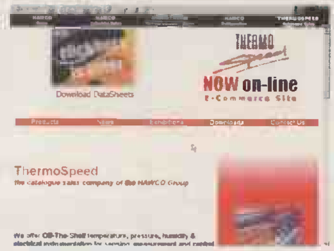

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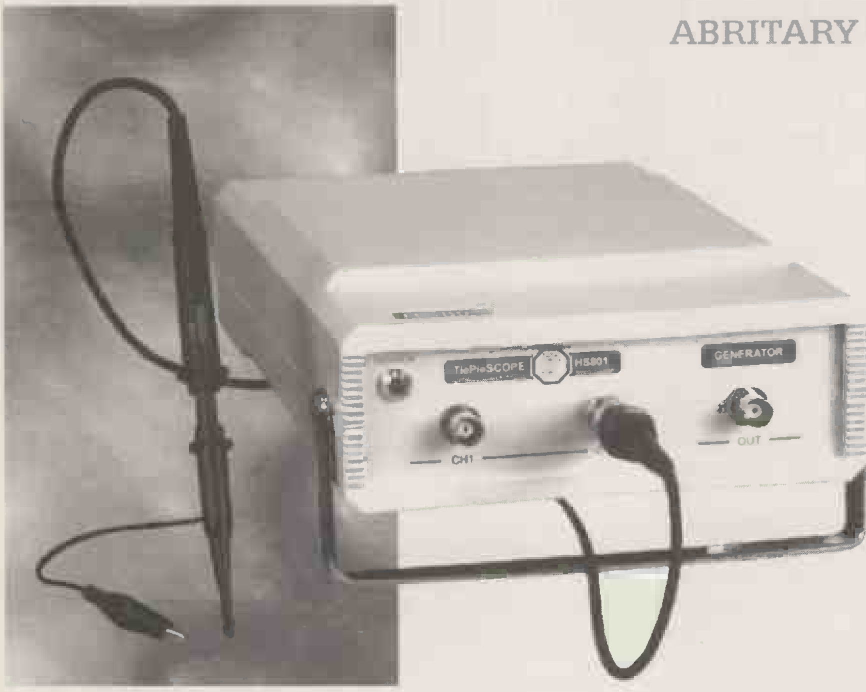

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Low-voltage design: round up

It is well known that by placing two complementary differential pairs in parallel, it is possible to obtain a rail-to-rail input stage. The nMOS pair conducts while input common-mode voltages are high, in particular if,

$$V_{in,cm} > V_{ss} + V_{gs1,n} + V_{ds3,n}$$

When input common-mode voltages are low, the pMOS pair is in conduction,

$$V_{in,cm} < V_{DD} - V_{gs1,p} - V_{ds3,p}$$

From these two equations, it is clear that both differential pairs can operate together for middle values of the input common mode voltage. In this case, the total transconductance of the input stage is not constant.

It is possible to bring the supply voltage down as far as the point where it starts to affect g_m by making the two edges that delimit the nMOS and pMOS operating regions coincide.

From the previous equations, this implies,

$$V_{DD}(-V_{ss}) = V_{gs1,n} + V_{gs1,p} + V_{ds3,n} + V_{ds3,p}$$

If the input transistors work in saturation, considering also a saturation voltage of about 0.2V and threshold voltages of 0.7-0.75V, a supply voltage of 1.9V results. But this value needs to be lower.

By simply reducing V_{DD}, a constant transconductance can be obtained: for low input common-mode voltages, only the pMOS pair is active, where for high ones only the nMOS pair is in conduction.

For values between, both pairs are 'on', the nMOS pair gradually taking over from the pMOS pair as the input common-mode voltage rises.

Constant-g_m operation with low supply voltages is achieved by designing input transistors with large aspect ratios – W=1000µ, L=1.2µ for example – operating in weak inversion.

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Four leading researchers in the field of low-voltage, low-power analogue building blocks present the culmination of their work – a low voltage rail-to-rail operational amplifier implemented in CMOS with a constant-g_m. New applications for low-voltage building blocks are also discussed, and there's an outline of a new Spice model specifically for low-voltage design.

Variables W and L – i.e. width and length – refer to the channel width and length of the MOS transistor. Their ratio, W/L, called the aspect ratio, is fundamental because the drain current is proportional to it.

Normally we design a transistor by selecting W and L. The minimum value of L is limited by the technology available. A typical value is 0.35μm.

The value of L is also important for the output resistance value. Resistance R_{out} is inversely proportional to L.

Tail transistors M_{3n} and M_{3p} work in the linear region for mid-range input values and in weak inversion for low and high input voltages. In this manner, being in weak inversion, g_m is proportional to current, it is enough to keep the sum of the tail currents constant to perform the constant-g_m operation. Under these conditions and from the circuit analysis, the previous equation becomes,

$$V_{DD}(-V_{ss}) \cong V_{Th.p} + V_{Th.p} + nU_T\left[\ln\frac{I_{ds.n}}{2\times I_{d01n(M1)}} + \ln\frac{I_{ds.p}}{2\times I_{d01p(M1)}}\right]$$

where U_T is thermal voltage and n the slope factor.

The above equation gives the direct relationship between the total drain current of the input pairs $I_{ds,n}$ plus $I_{ds,p}$, and the corresponding supply voltage that ensures constant transconductance operation under the imposed conditions.

For example, for a given total current of 20μA, the supply voltage for the used technology is about 1.33V.

The complete low-voltage OTA

The complete OTA is shown in **Fig. 1**. Its feedback circuit gives an equal value of transconductance for low and high inputs. Two dummy circuits have been placed operating respectively at high input levels, M_{d1n}-M_{d2n}, and low input levels, M_{d1p}-M_{d2p}.

A feedback MOS transistor, M_{5n}, controls the current in the pMOS input stage and makes it equal to the nMOS stage. The transistors are working in weak inversion.

To take into account the influence of the slope factor, transistor M_{6p} is designed with a slightly higher value of W of 1080μ instead of 1000μ.

Two secondary feedback loops appear on the dia-

Table 1. Measured results obtained from a prototype of an operational transconductance amplifier for very low voltage operation. These results were obtained using a 1.5V supply and 15pF load.

Input stage swing	Rail-to-rail (from V_{ss} to V_{Int} + 0.5V)
Output stage swing	Rail-to-rail
Input transconductance	Constant ($\Delta g_{m(max)}$=6%)
Gain bandWidth (GBW)	1.3MHz (PM=64°)
Low-frequency gain	84dB
Power consumption (total $I_{quiescent}$ in input stages, 10μA; in output stage, 90μA)	0.46mW (215μW in main stage, 230μW in biasing and feedback loops, only 15μW in regulator)
Slew rate	1V/μs
Total harmonic distortion (1kHz, V_{pp}=60% V_{AL})	1%
Equivalent input voltage noise	25nV/√Hz (1/*f* noise negligible)
Input offset voltage	Typical 0.8mV; 3σ value, ±0.2mV
Settling time	0.38μs (1%) ; 0.58μs (0.1%)
Overload recovery	100ns
CMRR	56dB @ 10Hz; 52dB @ 100kHz
PSRR+	48dB @ 10Hz; 26dB @ 100kHz
PSRR–	51dB @ 10Hz; 32dB @ 100kHz
Chip area	1.2mm^2

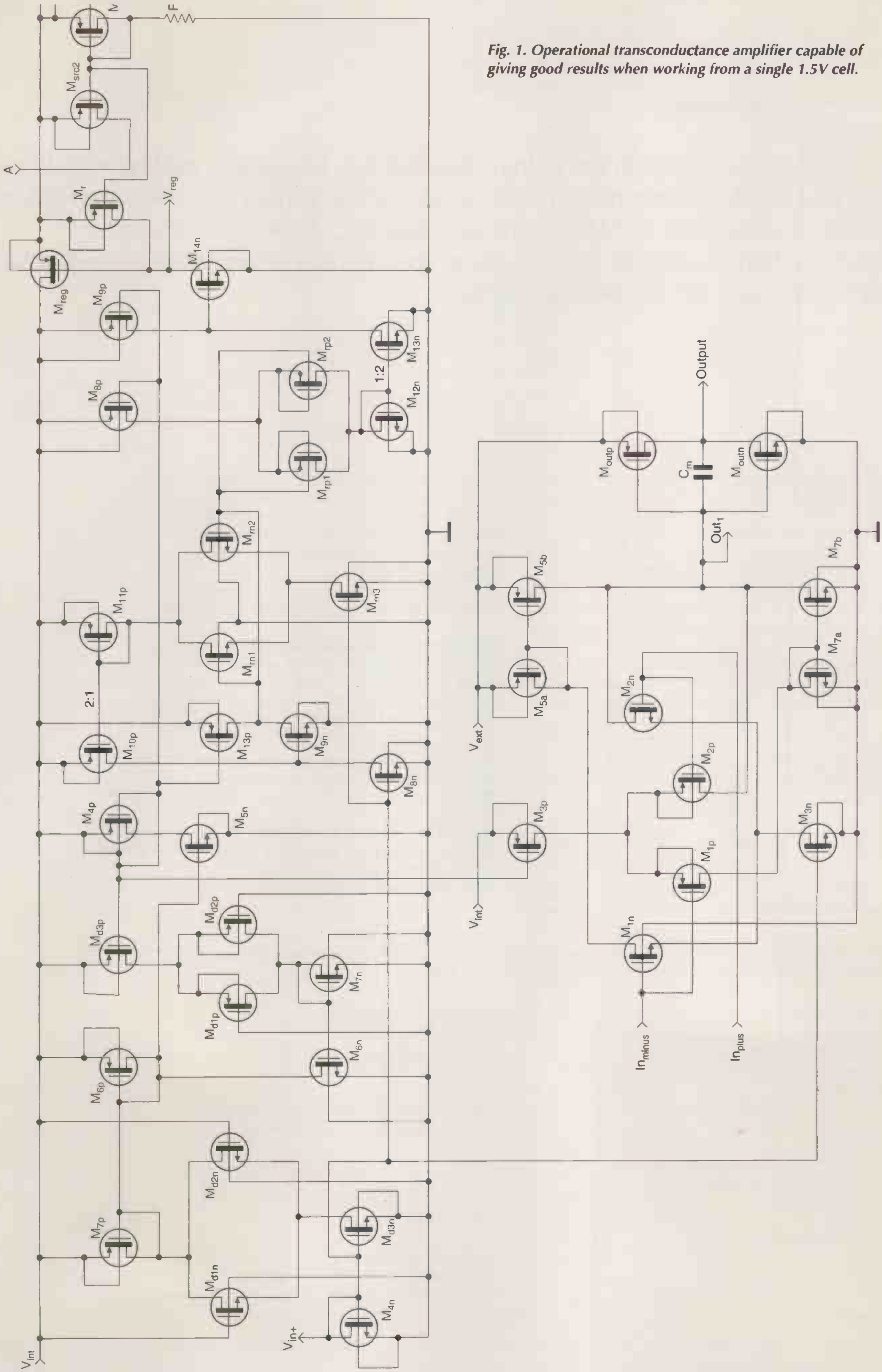


Fig. 1. Operational transconductance amplifier capable of giving good results when working from a single 1.5V cell.

gram. These ensure a constant supply voltage by sensing the 'crossing-point' condition, implemented via equal transistors M_{9n} and M_{13p}.

The loops are formed by two duplicate circuits, M_{rn1}-M_{rn2} and M_{rp1}-M_{rp2} working in the 'crossing-point' condition; two current mirrors, M_{10p}-M_{11p}; M_{12n}-M_{13n}; two feedback transistors, M_{9n} and M_{14n}, and a regulating MOS transistor, M_{reg}, working in its linear region.

The left-hand loop detects the 'crossing-point' condition and compares the mirrored current I_D of M_{11p} with a reference current flowing through M_{8n}. In the right-hand loop is a voltage regulating system which, by means of external supply voltage V_{ext} controls the internal supply voltage V_{int} and keeps it constant. The external supply voltage may be a battery.

In this manner, the whole circuit is robust to possible discharges of the external supply. The feedback circuitry can work with values of external supply voltages V_{ext} in the range 1.3-2.2V.

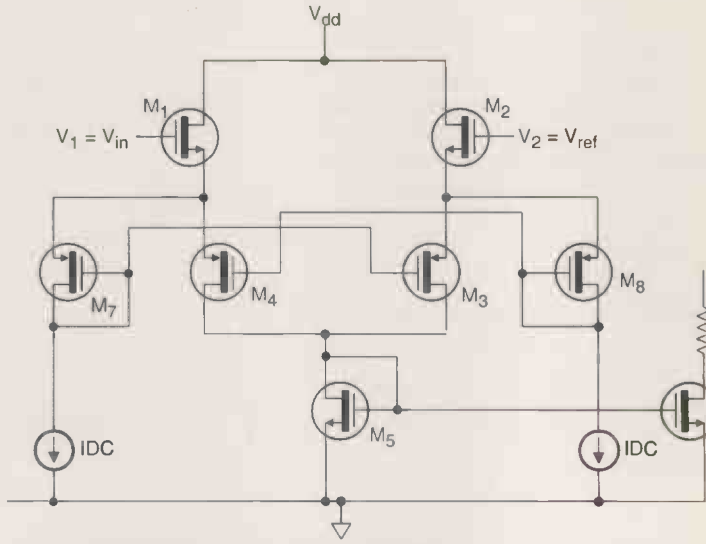


Fig. 2. Adaptive biasing – a means of reducing power consumption without affecting performance.

Circuit details

The diagram gives the main schematic of the op-amp. It is formed by the input stage, described in a previous article, a summing stage comprising M_{5a}, M_{5b}, M_{7a} and M_{7b}, which realises the inversion of some currents, and a traditional common source rail-to-rail output stage, $M_{out,n}$, $M_{out,p}$. The compensation of the op-amp doesn't need nested loops, being performed by a Miller capacitance C_m of 20pF.

The operating principle is the following. For low input common-mode voltages, only the pMOS input pair is active. Current flowing on M_{1p} and M_{2p} is given by the drain current of M_{3p} (*I*ds,p). Transistors M_{1n} and M_{2n} are both off and no current flows in M_{3n}.

For high input common-mode voltages, only the nMOS pair is active. In this case, the input current flows into M_{1n}, M_{2n} and, hence, into M_{3n}. This total current is kept equal to $I_{ds,p}$ by means of the feedback circuit. Since the input transistors are in weak inversion, the input transconductance is the same for low and high input common mode voltages.

For mid-way values of common-mode input voltages, a reduced value of current flows in both the input pairs. This current, in the 'crossing-point' condition, is exactly half of the value compared to low and high common inputs. But the total current flowing in the input transistors and, consequently, the input transconductance is always the same.

The input voltage that causes the 'crossing-point' condition is strictly linked to the value of V_{int}. In fact,

Spice and low-voltage transistors – a brand new model

The performance of analogue circuits depends heavily on transistor characteristics. In analogue design, an important aspect when developing a transistor model is that it is not only suitable for simulation, but also that it offers the possibility for exploring new circuit topologies.

The model has to contain hierarchical levels, in order to give both simple analytical expressions to support simple circuit and detailed expressions for precise simulations.

A good model for analogue design has to hold at low supply voltages. In this case, the model has to describe, in a continuous manner, the transistor behaviour from very low currents – weak inversion or sub-threshold operation – to large currents.

Initially, MOS transistor models involved only a few parameters such as the threshold voltage, the current parameter K*P*, and the body-effect parameter gamma.

Reducing channel length has increased the number of parameters necessary for suitable transistor modelling. In Spice there is always a different model for the weak and strong inversion regions. Consequently, modelling in the transition region from weak to strong inversion is poor.

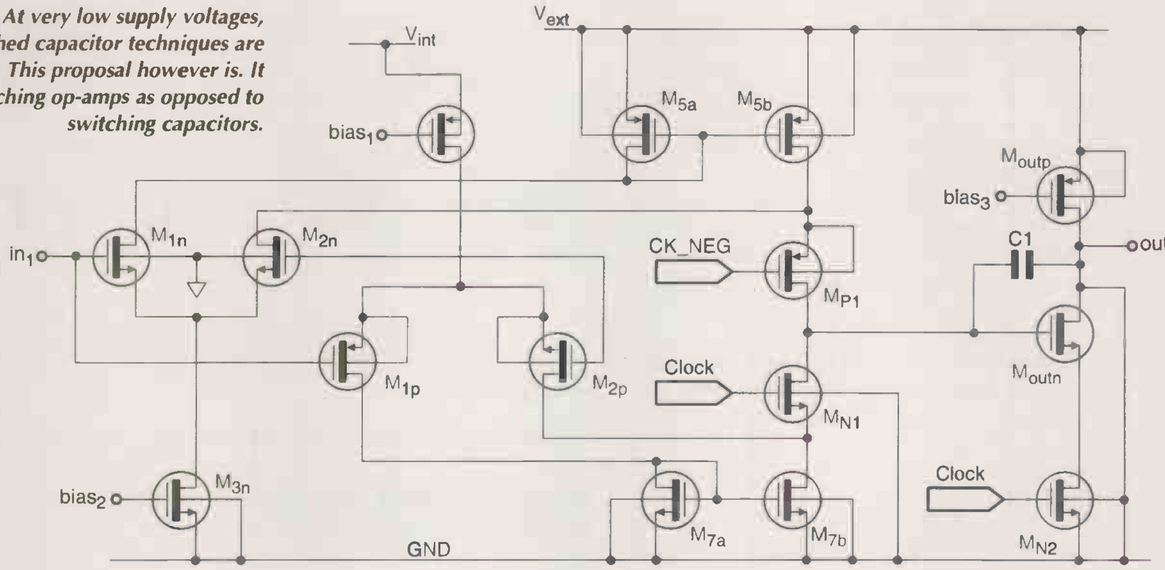
Recently a new model has been proposed – namely EKV, produced by Enz, Krummenacher and Vittoz – that gives a unique set of equations for the MOS transistors. However, it has not yet beenimplemented in commercial Spice.

In this model, weak and strong inversion are tightly linked to each other in a physical and continuous way. The new model is physically based, hierarchically structured and offers several coherent hierarchical levels. These range from simple analytical expression to support for creative synthesis and even more detailed expressions for precise simulations.

In particular, the new model is well suited for the design of circuits operating at low currents and voltages.

For more information, see 'An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications' by C. Enz, F. Krummenacher, E. Vittoz, *'Analogue Integrated Circuits and Signal Processing – Special Issue on Low Voltage and Low Power Circuits'*, Vol. 8, July 1995, pp. 83-114.

Fig. 3. At very low supply voltages, switched capacitor techniques are unusable. This proposal however is. It involves switching op-amps as opposed to switching capacitors.



it is about half of it. The secondary feedback system described earlier prohibits variations in V_{int} and, consequently, fixes the 'crossing-point' condition.

Such a chip has been implemented in 0.7μm standard CMOS technology. The minimum channel length is 1.2μm and the threshold voltages about 0.7V. **Table 1** shows experimental results obtained using a 1.5V supply and 15pF load capacitance. These values can be considered valid for 1.3-1.8V.

More information on this development can be found in G. Ferri and W. Sansen's article, 'A rail-to-rail constant gm low voltage CMOS operational transconductance amplifier', *IEEE Journ Solid-State Circuits*, Vol. 32 No 10, Oct. 1997, pp. 1563-1567.

New applications for new low-voltage circuits

Here we describe two examples of novel circuits working at low supply voltages.

The first example involves an adaptive biasing technique, Fig. 2. This allows power consumption to be reduced without degrading the performance.

Output current of the circuit – typically the biasing current of an op-amp input stage – depends on the applied input differential voltage.

Making up the device are two nMOS input transistors, $M_{1,2}$; two transistors for detecting the differences between the input voltages, M_{34}, and a current mirror, M_{56}, giving the output current to the load resistance R

If $|V_1 - V_2| \le V_{th}$, M_3 and M_4 are both 'off' and output current is zero.

Introducing transistors $M_{7,8}$ and two equal current sources, I_{DC}, improves the sensitivity of the circuit to input voltages near the reference voltage, where the output current is close to zero.

In this case, if V_1 is near V_2, the current flowing in R is minimised to the biasing current of twice I_{DC}. If V_1 is not equal to V_2, transistors M_3 or M_4 conducts, giving an output current whose value increases with the input differential voltage.[1]

A switched-capacitor alternative

Our second example involves switched-op-amps. Switched-capacitor techniques allow a number of analogue functions to be realised conveniently and precisely. These include filters, sample-and-hold circuits and a-to-d or d-to-a converters.

However, using switched capacitor techniques at extremely low voltages – less than 1.5V – needs a particular attention to the switches.

At such low voltages, solutions proposed in the literature – low-threshold devices and voltage multipliers for the clock drivers – are no longer feasible. In fact, technologies with low-threshold devices are costly and often not available. Similarly, voltage multiplication is not possible in scaled technologies.

To overcome these problems, we propose the switched op-amp approach. The basic idea is to avoid the critical switches connected in series to the output of the op-amp. These switches turn the op-amp on and off and don't operate correctly when the supply voltage is lowered.

The new technique guarantees that the output switches have sufficiently high conductance for any output signal conditions.

Figure 3 is an example of the main stage of a switchable op-amp .[2] ■

This is the final article in a four-article set discussing the state-of-the-art in low-voltage analogue ICs. The three previous articles, in the September, October and November issues, covered bipolar building blocks, CMOS input stages and CMOS output stages respectively.

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2. G. Ferri, A. Costa, A. Baschirotto, 'A 1.2V rail-to-rail switched buffer,' ICECS'98. Lisbon, 7-10 Sept. 1998.

Measuring RF power

Joe Carr looks at commercial equipment for measuring RF power and explains how it works.

(Photo courtesy of Bird Electronics Corporation)

Here I take a look at some popular commercial products, as well as the calorimetry approach to high power measurements, and some methods for making low power measurements. Error and uncertainty sources in RF power measurements are discussed too, later in the article.

The Bird 'Thruline' sensor

Bird Electronics' Thruline sensor is shown in **Fig. 1a)**, while an equivalent circuit is shown in Fig. **1b)**. The sensor consists of a coaxial transmission-line section, and a wire-loop directional coupler that connects to a diode detector, D_1.

Consider the equivalent circuit in Fig. 1b). The factor M is the mutual coupling between the loop and the centre conductor of the coaxial line section, as well as the voltage divider consisting of R and C.

Potential E is the voltage between the inner and outer conductors of the coaxial line, while E_R is the voltage drop across the resistor, e_M is the voltage across the inductor and e is the output potential.

Voltage divider R/C produces a potential given by equation (1), provided that $R<<X_C$ and $e_m=Ij\omega\pm M$.

$$e_r = \frac{RE}{X_c} = REj\omega C \qquad (1)$$

The output voltage is,

$$e = e_R + e_M = j\omega(CRE \pm MI) \qquad (2)$$

Values of the components are selected such that $R<<X_C$ and $CR=M/Z_o$. It is now possible to state that the DC output voltage is,

$$e = j\omega\left[\frac{EM}{Z_o} \pm MI\right] = j\omega M\left(\frac{E}{Z_o} \pm I\right) \qquad (3)$$

At any point along a transmission line the voltage appearing between the centre conductor and outer conductor E is a function of forward voltage E_F and the reflected voltage E_R.

By combining equations, it is evident that when the directional coupler is pointed at the load, the output voltage of the sensor reads the forward voltage, and produces an output voltage of,

$$e = \frac{j\omega ME_F}{Z_o} \qquad (4)$$

And when pointed at the source,

$$e = \frac{j\omega ME_R}{Z_o} \qquad (5)$$

Thus, this sensor produces a voltage that is a function of the direction of the RF signal flowing in the transmission line.

Figures 2 and 3 show two examples of Thruline instruments. The one in Fig. 2 is the Model 4410A. It is based on the classic Model 43 design*. It offers an insertion voltage-standing-wave ratio of 1.05:1 up to 1GHz.

The sensor elements are plug-in. Each element has an arrow on it to indicate the direction of the measurement – pointed towards the load or the source, depending on whether you measure P_F or P_R. Once you know P_F and P_R, you can computer the VSWR from equation (6),

$$VSWR = \frac{1+\sqrt{\frac{P_R}{P_F}}}{1-\sqrt{\frac{P_R}{P_F}}} \qquad (6)$$

One difference between this instrument and earlier instruments is that there is a calibration factor control on the meter to optimise performance for the specific sampling element inserted.

The **Bird** APM-16 Advanced Power Meter is shown in Fig. 3. This meter is similar in concept to the older Model 43, but is considerably advanced. While the Model 43 measures RMS CW power, the APM-16 will measure analogue and digital complex waveforms, as well as CW – for example CDMA, TDMA, FDMA, COFDM and other modulations. It will measure both peak and RMS power levels.

Figure 4 shows a different approach. This meter uses a remote sensor head connected in-line between the source and load, and a multi-range digital readout display. It also has a computer interface that will permit running power-versus-frequency curves.

* My Model 43 has been banging around my toolkit for about 30-years and still works well.

Calorimeters

Calorimeters are capable of making very accurate measurements of RF power – especially at high power levels where other methods tend to fall down. These instruments measure the heating capability of the RF waveform. In this way, they produce an output proportional to the RMS power level that is independent of the applied waveform.

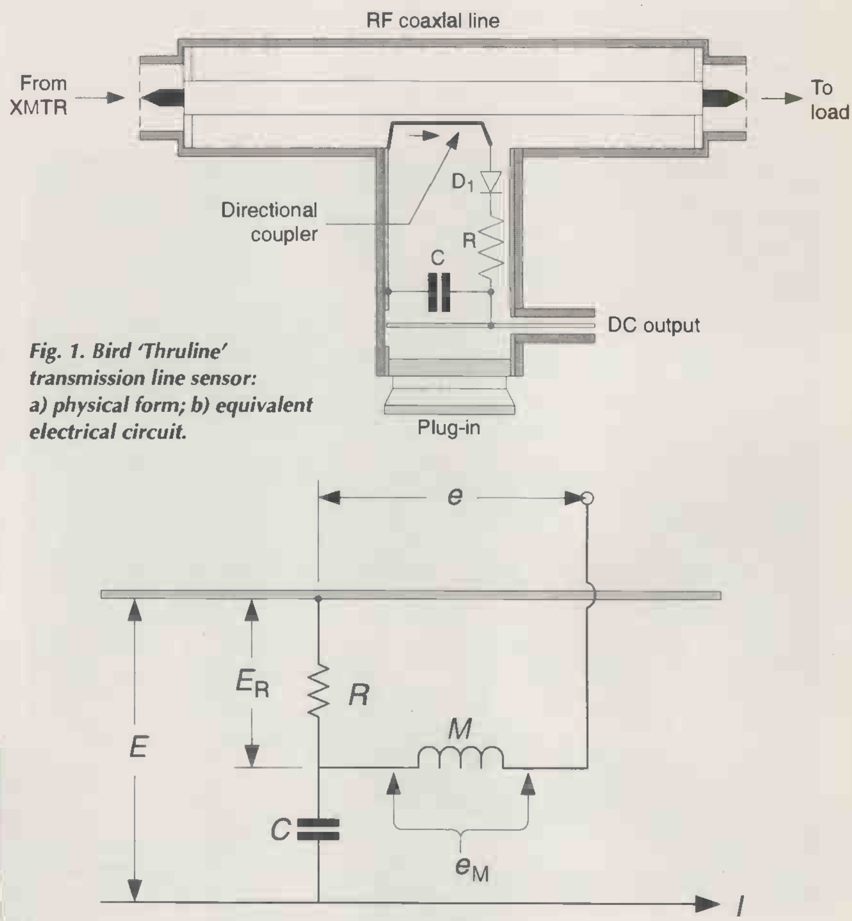


Fig. 1. Bird 'Thruline' transmission line sensor: a) physical form; b) equivalent electrical circuit.

Fig. 2. Bird Model 4410A RF wattmeter. Photo courtesy Bird Electronics Corporation.

Fig. 3. Bird Model APM-16 RF wattmeter. Photo courtesy of Bird Electronics Corporation.

The First Law of Thermodynamics† is the basis for the operation of calorimeters: energy can neither be created nor destroyed, only changed in form.

There are two basic forms of RF power calorimeter: dry and flow (or wet). Dry calorimeters are used at lower power levels, and are represented by the thermistor and thermocouple methods discussed in last month's article. Flow calorimeters are used at higher power levels.

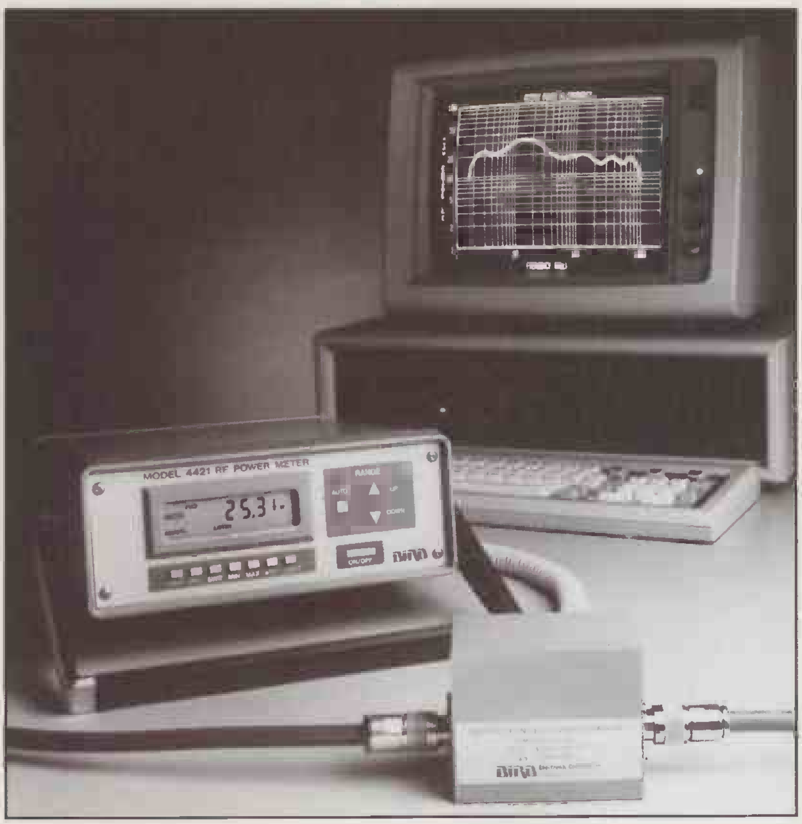
Flow calorimeters come in two varieties: substitution flow and absolute flow. Power can be measured using the following relationship,

$$P = F_{mass} \times (T_{out} - T_{in}) \times C_P(T) \quad (7)$$

where P is the power level, F_{mass} is the mass flow rate of the fluid used in the calorimeter, T_{OUT} is the fluid temperature after being heated by the RF load resistor, T_{IN} is the fluid temperature before being heated by the RF load resistor and $C_p(T)$ is the fluid specific heat as a function of temperature T.

† I am told that numbering of the laws of thermodynamics differs in various parts of the world. In the USA we start with the "0th law".

Fig. 4. Bird Model 4421 RF power meter with remote sensor head. Photo courtesy of Bird Electronics Corporation.



Substitution-flow calorimeters. This form of RF power meter, Fig. 4, uses two fluid loops. Each fluid loop is heated by a separate termination resistor. Termination 'A' is heated by a low-frequency AC power source, and the power applied to this termination is measured by an AC power meter. The unknown RF power is applied to termination 'B'. The differential temperature, $T_{OUT}-T_{IN}$, is measured by a differential thermocouple.

When the temperatures of the two fluids are equal to each other, then the output of the thermocouple is zero. When the AC power is adjusted to balance the temperatures while RF is applied, producing a zero output voltage from the thermocouple, the RF power is equal to the more easily measured AC power. A temperature stabiliser and heat exchanger returns the temperature of the fluid to base level after it is used to measure power.

This method will produce error of 0.28 percent or better, up to RF power levels of one kilowatt. Both water and oil are used as fluid coolants in various instruments.

Absolute-flow calorimeters. Figure 6 shows the absolute flow calorimeter. This type of RF power meter measures the mass flow rate of the coolant, as well as the temperature before the RF load resistor, T_{IN}, and after it, T_{OUT}. The mass flow rate is,

$$F_{mass} = f \times W_S(T_{IN}) \quad (8)$$

where W_S is the specific weight of the fluid at the input temperature and f is the volume flow rate (litres/min). All other terms are as previously defined.

Combining equations gives the equation for measuring RF power by this means,

$$P = k \times f \times W_S(T_{IN}) \times C(T_{AVE}) \times (T_{OUT} - T_{IN}) \quad (9)$$

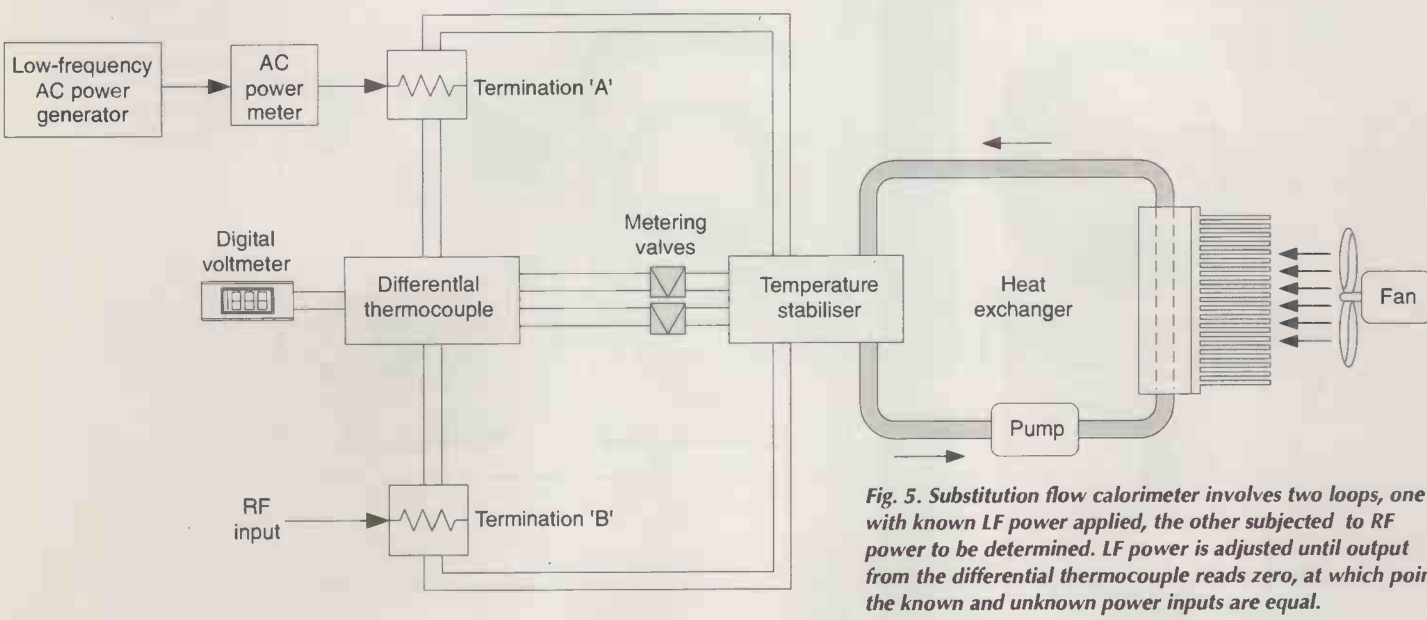


Fig. 5. Substitution flow calorimeter involves two loops, one with known LF power applied, the other subjected to RF power to be determined. LF power is adjusted until output from the differential thermocouple reads zero, at which point, the known and unknown power inputs are equal.

Here, T_{AVE} is $(T_{OUT}-T_{IN})/2$ and all other terms are as previously defined.

One of the advantages of the absolute flow approach is that it does not depend on nulling or calibration of a low frequency power source, yet it produces good accuracy at high power levels up to 80kW.

Figure 7 shows a commercially available calorimeter RF power meter made by Bird Electronics Corporation.

Micropower and low-power measurements

At very low power levels the diode output voltage drops very low. At –70dBm for example, the diode produces about 50nV output potential. This level is too close to the noise and drift values of typical DC amplifiers to be useful. A solution is to use a chopper circuit, **Fig. 8**.

A chopper is an electronic switch that turns the DC signal from the diode output on and off at a high rate – typically 100 to 10 000 times per second. Either a square wave or sine-wave 'carrier' applied to the toggle input of the electronic switch creates the switching action.

The chopped signal is essentially an AC signal, so it can be amplified in an AC amplifier, which has a much smaller feedback-controlled drift than a DC amplifier. Also, the AC signal can be band-pass filtered to remove noise. The band-pass filter is centred on the frequency of the carrier oscillator.

The chopped, amplified and filtered signal is applied to a synchronous detector that is controlled by the same carrier oscillator that performed the chopping action. A low-pass filter following the synchronous detector removes residual components of the switching action at the carrier frequency. Finally, a DC amplifier provides scaling to the correct DC level, or as level translation for an analogue-to-digital converter.

Micropower measurements pose special problems because they are made at levels below the range of most practical RF power sensors. In some cases, the chopper approach can be used with a diode detector. At lower levels, however, some other method is needed.

Figure 9 shows a comparison method using a calibrated RF signal generator. The instrument selected must have a calibrated output attenuator that provides accurate outputs in dBm or microvolts.

The signal generator and the unknown micropower source are connected to a receiver equipped with an S-meter through a hybrid coupler. The coupler must have either equal port-to-port losses for the two inputs, or at least accurately known different losses.

Optional calibrated step attenuators are also sometimes used to balance the power levels. The receiver acts as a micropower wattmeter or voltmeter because it will produce an S-meter reading of even very weak signals.

Two methods can be used, namely 'equal deflection' or 'double deflection'. In the equal-deflection method, the unknown source is turned on, and the S-meter reading noted. The unknown source is then turned off, and the signal generator is turned on.

Next, the output of the signal generator is adjusted to produce the same S-meter deflection. The power level of the unknown source is therefore equal to the calibrated signal generator output level.

The double deflection method sets the signal gen-

Fig. 7. Bird calorimeter RF wattmeter (Photo courtesy of Bird Electronics Corporation).

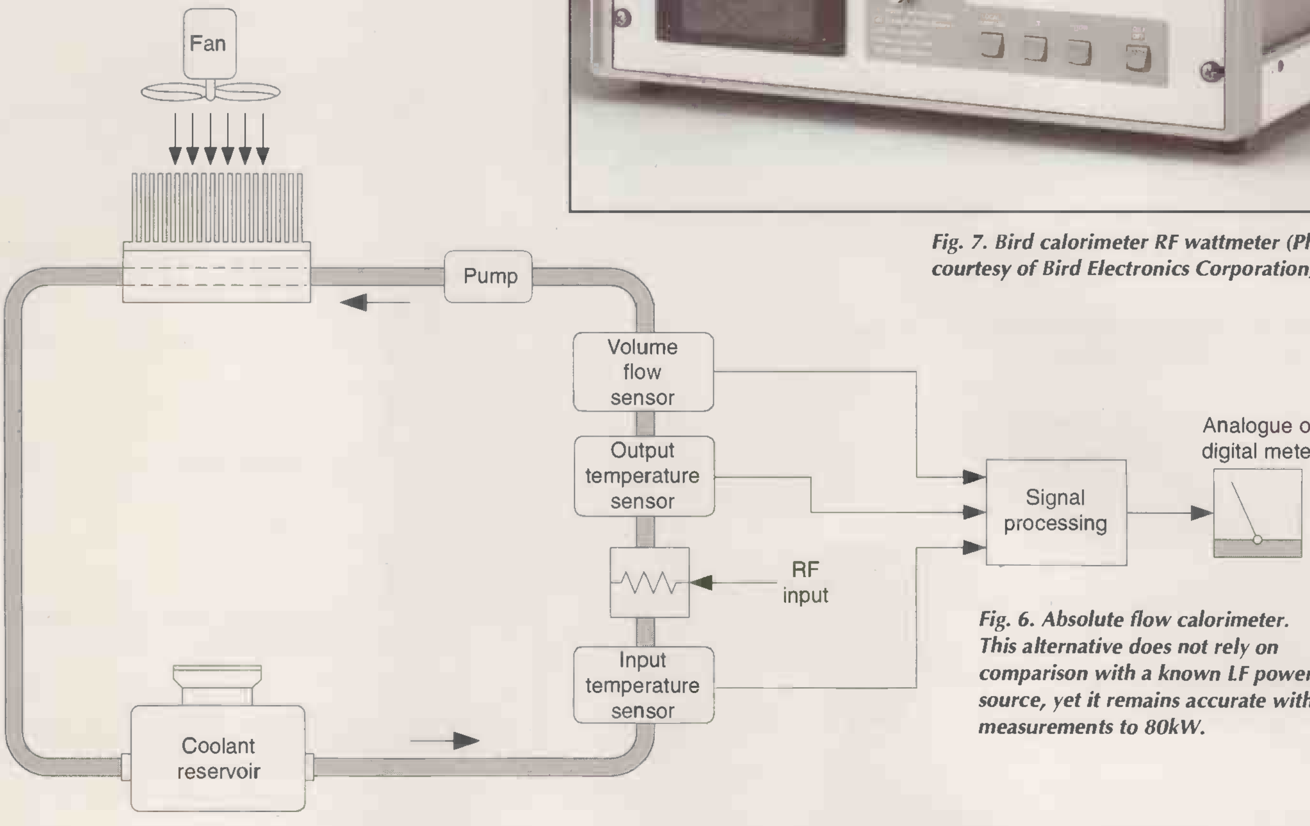


Fig. 6. Absolute flow calorimeter. This alternative does not rely on comparison with a known LF power source, yet it remains accurate with measurements to 80kW.

erator output to zero, and then applies the unknown RF power to the receiver. The S-meter reading is noted; for practical reasons, adjust the attenuator to let the meter fall on a specific indicator marking).

Next, the signal generator output is increased until the S-meter reading goes up one S-unit, which will be either 3dB or 6dB, depending on the design of the receiver. The output level of the signal generator is therefore equal to that of the unknown power source.

Error and uncertainty sources

All measurements have some basic error, i.e. a difference between the actual value of a variable and the value read from a meter. The three dominant classes of error in RF power measurements are mismatch uncertainty, sensor uncertainty and meter uncertainty.

Meter uncertainty is error due to problems in the meter indicating device itself. It might be a measurement error, i.e. a difference between the actual output voltage and the displayed output voltage, which represents power. You might see zero set error, zero carryover, drift, noise and other sources of instrument error.

On analogue meters there are also additional error sources. For example, the width of the pointer covers a certain distance on the scale, so creates a bit of ambiguity. Also, there may be a parallax error if the meter is read at an angle.

Digital meters exhibit quantisation error and last-digit bobble error. The quantisation error comes from the fact that the digital representation of a value can only assume

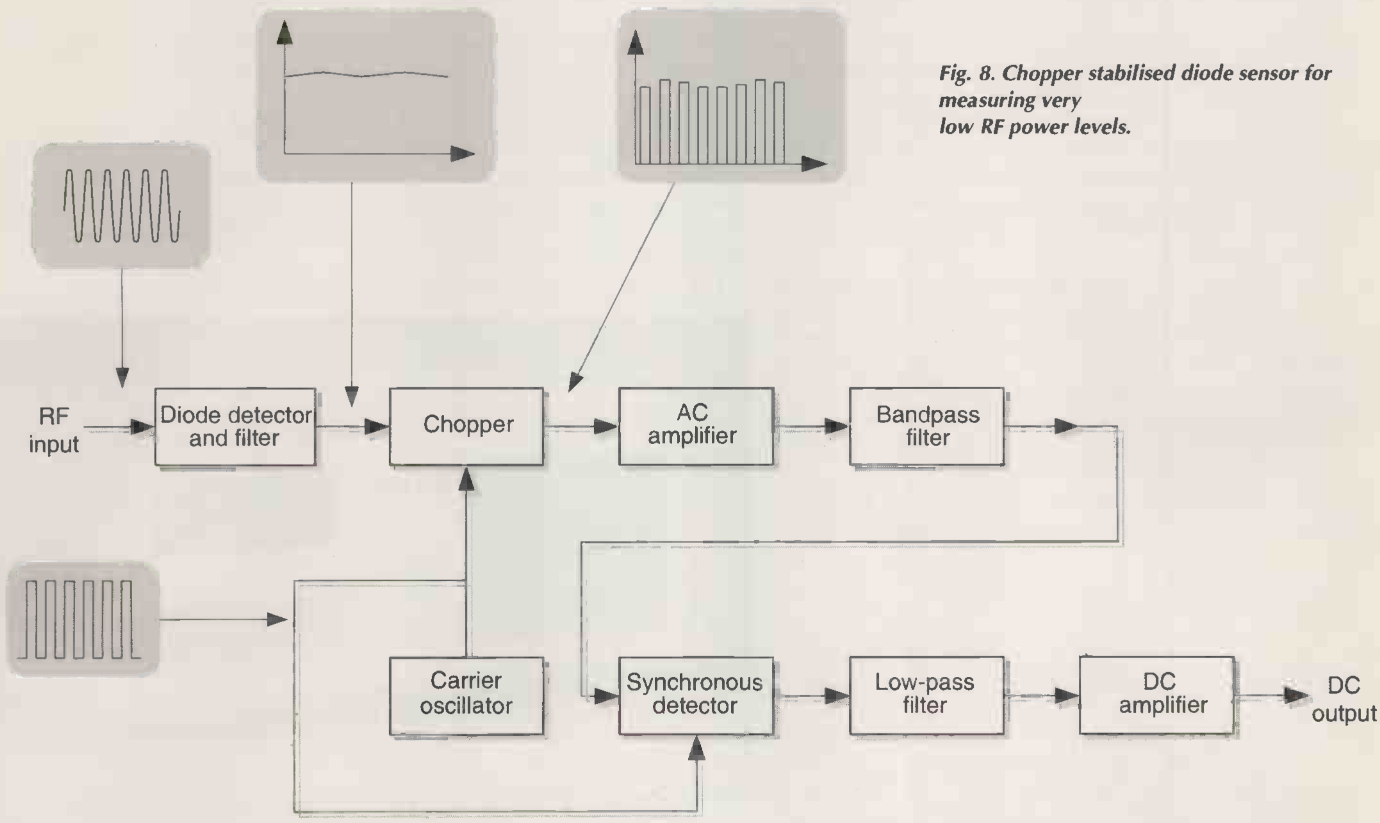
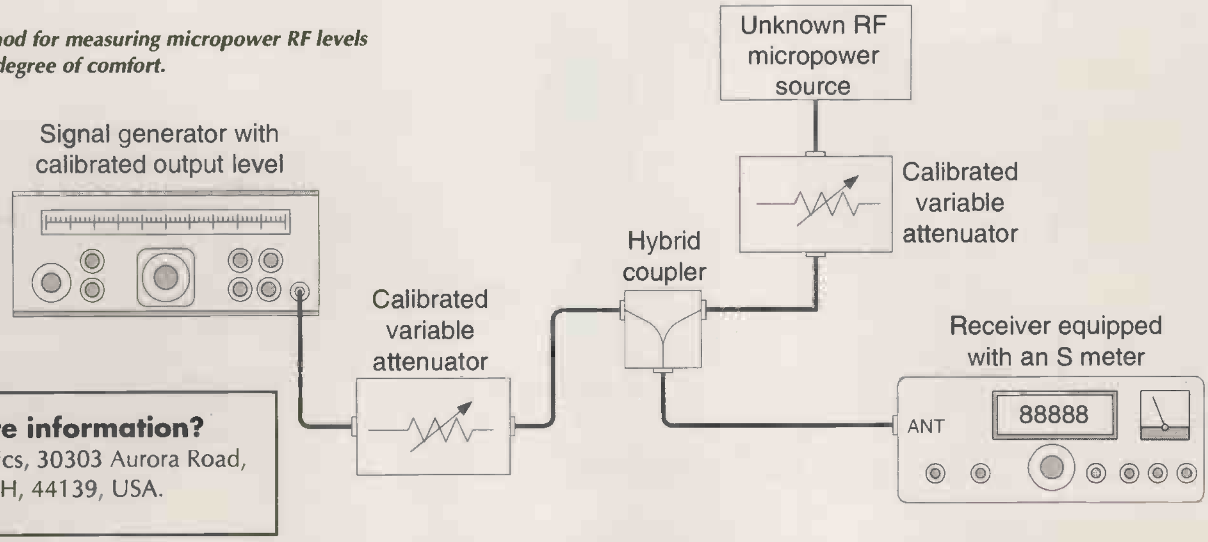


Fig. 8. Chopper stabilised diode sensor for measuring very low RF power levels.

Fig. 9. Method for measuring micropower RF levels with some degree of comfort.



Need more information?
Bird Electronics, 30303 Aurora Road, Cleveland, OH, 44139, USA.

certain discrete values, and an actual value might be halfway between the two authorised levels. Last digit bobble – a ±1 count error – results from the fact that the least significant digit tends to bounce back and forth between two adjacent values.

Sensor error may come in a variety of guises, depending on the nature of the sensor. Thermistors and thermistors, for example, have different forms of error. Most sensors, though, exhibit an efficiency error due to losses in the sensor. This occurs when some of the applied RF energy is radiated as heat rather than being used to affect the output reading. The manufacturer of the sensor may express this problem as a calibration uncertainty or calibration factor.

Mismatch loss and mismatch uncertainty. The mismatch loss occurs when a voltage standing wave ratio – SWR or VSWR – exists in the system. Maximum power transfer occurs when a source impedance and a load impedance are matched. If these impedances are not matched, then a portion of the power sent from the source to the load is reflected.

The reflection coefficient, ρ, is,

$$\rho = \frac{VSWR - 1}{VSWR + 1} \quad (10)$$

Table 1 shows the reflection coefficient for VSWR values from 1:1 to 3:1. Single-ended mismatch loss in decibels is,

$$L_{mismatch} = 10\log\left(1 \pm \rho^2\right) \text{ dB} \quad (11)$$

If the system is mismatched on both ends, mismatch loss is,

$$L_{mismatch} = 20\log\left[1 \pm \left(\rho_1 \times \rho_2\right)\right] \quad (12)$$

The mismatch uncertainty, expressed as a percent,

$$L_{uncert.} = \pm 2 \times \rho_1 \times \rho_2 \times 100\% \quad (13)$$

Assume that there is a 1.75:1 VSWR at the source end, ρ_1=0.27, and a VSWR of 1.15:1, at the sensor/load end, ρ_2=0.07. The mismatch uncertainty is,

$$L_{uncert.} = \pm 2 \times 0.27 \times 0.07 \times 100\% = 3.78\% \quad (14)$$

Total uncertainty. The total uncertainty in the measurement involves the mismatch uncertainty, calibration factor uncertainty and instrumentation uncertainty. If a reference power source is used in a comparison measurement, it also involves power source uncertainty .

There are several ways to state the total uncertainty. Two of these are worst-case uncertainty and root-sum-square uncertainty. The worst-case uncertainty is the sum of all individual uncertainties in the direction that maximises the overall uncertainty. For example, imagine a system with,

Mismatch uncertainty	3.78%
Calibration factor uncertainty	1.76%
Instrumentation uncertainty	0.95%
Power reference uncertainty	1.35%

The worst case uncertainty is their sum:

Uncertainty=±(3.78%+1.76%+0.95%+1.35%)=±7.84%

Real errors are rarely worst case, but rather are uncorrelated to each other. The root sum squares, or RSS, method allows a single error term to represent the average errors of the system. For a system with four sources of error, as above, E_1, E_2, E_3, E_4 and E_5, the RSS error is,

Table 1. Reflection coefficients for VSWR values from 1:1 to 3:1.

dB(μV)	dBm	Watts	V	μV
7	–100	1.000E–13	2.236E–06	2.24
12	–95	3.162E–13	3.976E–06	3.98
17	–90	1.000E–12	7.071E–06	7.07
22	–85	3.162E–12	1.257E–05	12.57
27	–80	1.000E–11	2.236E–05	22.36
32	–75	3.162E–11	3.976E–05	39.76
37	–70	1.000E–10	7.071E–05	70.71
42	–65	3.162E–10	1.257E–04	125.74
47	–60	1.000E–09	2.236E–04	223.61
52	–55	3.162E–09	3.976E–04	397.64
57	–50	1.000E–08	7.071E–04	707.11
62	–45	3.162E–08	1.257E–03	1 257.43
67	–40	1.000E–07	2.236E–03	2 236.07
72	–35	3.162E–07	3.976E–03	3 976.35
77	–30	1.000E–06	7.071E–03	7 071.07
82	–25	3.162E–06	1.257E–02	12 574.33
87	–20	1.000E–05	2.236E–02	22 360.68
92	–15	3.162E–05	3.976E–02	39 763.54
97	–10	1.000E–04	7.071E–02	70 710.68
102	–5	3.162E–04	1.257E–01	125 743.34
107	0	1.000E–03	2.236E–01	223 606.80
112	5	3.162E–03	3.976E–01	397 635.36
117	10	1.000E–02	7.071E–01	707 106.78
122	15	3.162E–02	1.257E+00	1 257 433.43
127	20	1.000E–01	2.236E+00	2 236 067.98
132	25	3.162E–01	3.976E+00	3 976 353.64
137	30	1.000E+00	7.071E+00	7 071 067.81

$$RSS = \sqrt{E1^2 + E2^2 + E3^2 + E4^2} \quad (15)$$

In terms of the values above,

$$RSS = \sqrt{3.78\%^2 + 1.76\%^2 + 0.95\%^2 + 1.35\%^2}$$
$$= \sqrt{14.29 + 3.1 + 0.9 + 1.82\%} = \sqrt{20.11\%}$$
$$= 4.48\%$$

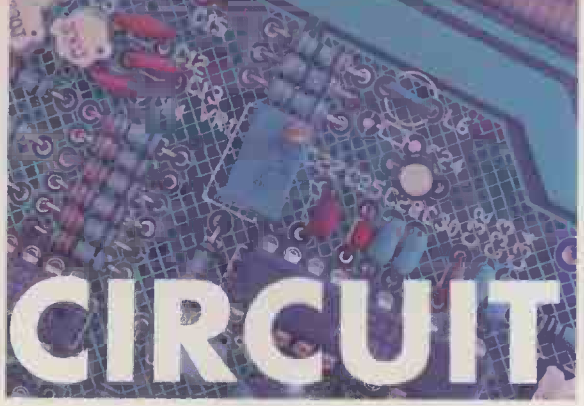
Compare the worst case error of 7.84% with the RSS error of 4.48%. Expressed in terms of decibels, the RSS percent loss is,

$$RSS(\text{dB}) = 10\log\left[1 \pm \left(\frac{RSS\%}{100}\right)\right] \quad (16)$$

In summary

This article, and its more background-oriented counterpart that appeared last month, has dealt with the technology of RF power measurement, from very low micropower levels to the multi-kilowatt levels used by broadcasters. ■

Last month, Joe discussed some of the basic methods for measuring RF power, and some of the more common in-line bridge circuits.



CIRCUIT IDEAS

Fact: most circuit ideas sent to *Electronics World* get published

The best circuit ideas are ones that save time or money, or stimulate the thought process. This includes the odd solution looking for a problem – provided it has a degree of ingenuity.

Your submissions are judged mainly on their originality and usefulness. Interesting modifications to existing circuits are strong contenders too – provided that you clearly acknowledge the circuit you have modified. Never send us anything that you believe has been published before though.

Don't forget to say why you think your idea is worthy.

Clear hand-written notes on paper are a minimum requirement: disks with separate drawing and text files in a popular form are best – but please label the disk clearly.

All-silicon Christmas lights

The idea behind these lights is to create a less flashing decoration than the usual intermittent Christmas lights: something a bit like stars in the sky. They consist of many small and bright light points that change slowly in colour and intensity.

The light points are LEDs, directly controlled by a small eight-pin microcontroller, namely a PIC 12C509. Each module consists of a small circuit with the PIC and a Blue LED mounted on it. Two independent series of two bi-colour LEDs each are connected to the module through short wires.

The two LEDs in each series are mounted together in opposite directions so they can be viewed from all angles, and can be considered a single point of light. This way, each module controls three separate points of light. A tiny prototype circuit with three stripes at 0.1in is useful to solder the LEDs and wires to.

The bi-colour LEDs used here produce green or red light depending on which way the current flows.

LEDs connected between two ports of the PIC are intensity modulated by PIC's PWM ON/OFF function and colour modulated by PWM +/-. Applying the two modulations at the same time and slowly changing their values produces simultaneous changes in intensity and colour. They even twinkle depending on the relative values of PWM frequencies!

The blue LED on the board is only intensity modulated. It needs so much voltage that a port output at 5V is not enough to light two in series.

Due to the blue LED's high price, or availability problems, it can be substituted by a series of two non-blue LEDs. In this case the limiting series resistor needs also to be changed.

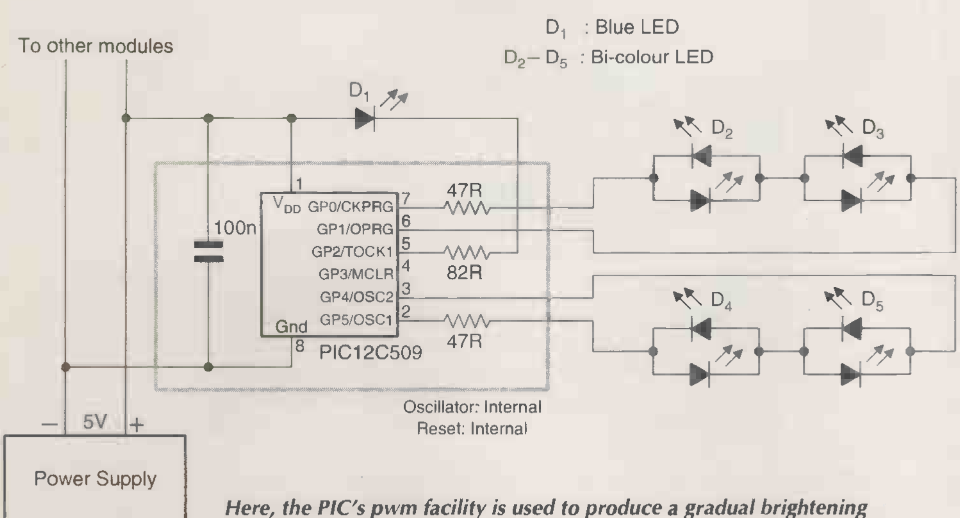
A set of lights is created by connecting as many modules as needed to a two-wire bus that distributes 5V all of them.

Two hex files are given. They differ only in the speed at which the intensity and colour of LEDs is changed. Mixing slow and fast modules gives a bit more variety.

The PIC12C509 must be programmed to run on its internal oscillator and reset.

Merry Christmas.

Albert Pijuan
Girona
Catalonia



Here, the PIC's pwm facility is used to produce a gradual brightening and dimming of LEDs to give a less garish effect than the usual on/off Christmas lights.

Slow twinkling hex for the PIC.

```
:100000002C0A2000110098002800430029002003D
:1000100041006C006200650072007400200050016
:100020006900 6A00750061006E002000310039002F
```

```
:100000002C0A20001100980028004300290020003D
:1000100041006C00620065007200740020005000 16
```

```
:100000002C0A20001100980028004300290020003D
:1000100041006C0062006500720074002000500016
:1000200069006A00750061006E002000310039002F
:1000300039003800200061007000690006A00750016
```

```
:100000002C0A20001100980028004300290020003D
:1000100041006C0062006500720074002000500016
:1000200069006A00750061006E002000310039002F
:10003000390038002000610070006900 6A00750016
:1000400061006E00400069006E0061006D00650097
:100050002E0063006F006D001F0C270007022400B4
:100060006000E700070C870043072E0A6700400C7A
:100070002A00800C2D00400C2900800C2C00C00CA4
:100080002F000400080C0600840C02000A02810004
:1000900010C0306020C28000D028100100C03065F
:1000A000200C2B00040C2E006607630AB002090224
:1000B00090000306680000C02900003066B000F021C
:1000C00090000 3066E0008020B010E012600E107F6
```

Code removed here to save space. Removed lines follow on with sequential addresses and zeros as in the previous three lines. The last byte for each line in turn is: `1F, 0F, FF, EE, DE, CE, BE, AE, 9E, 8E, 7E, 6E, 5E, 4E, 3E, 2E, 1E, 0E, FE, ED, DD, CD, BD, AD, 9D, 8D, 7D, 6D, 5D, 4D, 3D, 2D, 1D, 0D`. Then:

```
:1003F00000000000000000000000000000002C0AC7
```

And more zeros with last bytes: `EC, DC, CC, BC, AC, 9C, 8C, 7C, 6C, 5C, 4C, 3C, 2C, 1C, 0C, FC, EB, DB, CB, BB, AB, 9B, 8B, 7B, 6B, 5B, 4B, 3B, 2B, 1B, 0B, FB, EA, DA, CA, BA, AA, 9A, 8A, 7A, 6A, 5A, 4A, 3A, 2A, 1A, 0A, FA, E9, D9, C9, B9, A9, 99, 89, 79, 69, 59, 49, 39, 29, 19`. And finally,

```
:1007E000000000000000000000000000000000009
:0E07F000000000000000000000A304C3048D
:021FFE000E00D3
:00000001FF
```

And more quickly twinkling hex for the PIC...

```
:100000002C0A20001100980028004300290020003D
:1000100041006C0062006500720074002000500016
:1000200069006A00750061006E002000310039002F
:10003000390038002000610070006900 6A00750016
:1000400061006E0040006900 6E0061006D00650097
:100050002E0063006F006D001F0C270007022400B4
:100060006000E700070C870043072E0A6700400C7A
:100070002A00800C2D00400C2900800C2C00C00CA4
:100080002F000400080C0600840C02000A02810004
:1000900010C0306020C28000D028100100C03065F
:1000A000200C2B00040C2E006607630AB002090224
:1000B0009000030668000C02900003066B000F021C
:1000C000900003066E0008020B010E012600E107F6
:1000D0006B0AE705C80AE707C80AE704F102800AC5
:1000E000010C3100090C0706790A8A0003067F0A11
:1000F0007C0ACA0103077F0A010CA7010A022A0031
:10010000F202920A010C3200020C27068B0A8D00C3
:100110000306910A8E0ACD010307910A020CA7017A
:100120000D022D00F302A40A050C3300040C47064F
:1001300009D0A89000306A30AA00AC9010307A30AAE
:10014000040CA70109022900F402B60A020C3400CB
:10015000010C6706AF0A8C000306B50AB20ACC018F
:1001600000307B50A080CA7010C022C00F502C80A07
:10017000010C3500010C8706C10A8F000306C70A6F
:1001800 00C40ACF010307C70A100CA7010F022F00F2
:1001900 0410A000000000000000000000000000014
:1001A000000000000000000000000000000000004F
:1001B000000000000000000000000000000000003F
:1001C000000000000000000000000000000000002F
```

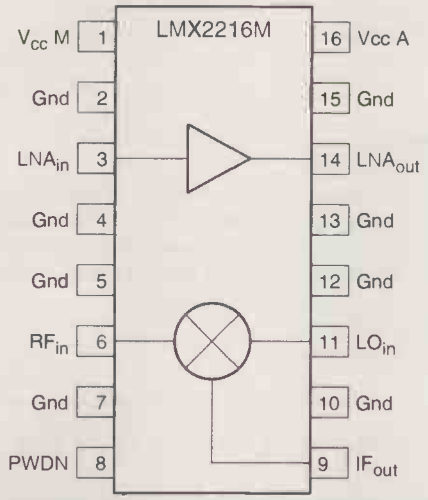
The remainder of the code is identical to that of the slow-twinkling routine. E-mail jackie.lowe@rbi.co.uk for both dumps complete, or send a blank disk with return postage to the editorial offices.

£100 winner

10MHz spectrum analyser monitors 550MHz signal

Needing to monitor the output of a 500-600MHz amplifier and only having a 10MHz spectrum analyser brought to mind an article on the use of gates as oscillators†. The design works reliably, but it is not without its limitations and could easily be improved.

A *74AC04* inverter forms the oscillator, whose frequency is determined by the supply voltage,



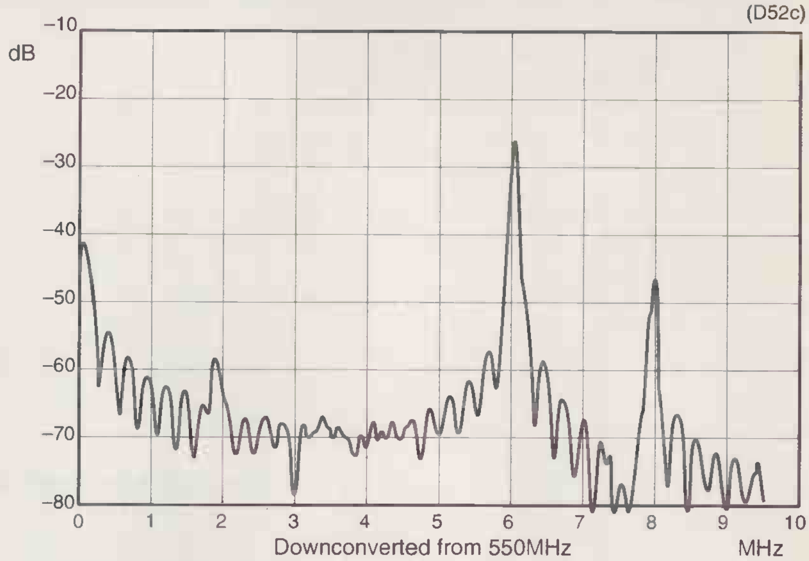
(D52b)

varying between 80MHz and 250MHz for a supply variation of 2-5.5V. Third harmonic is 750MHz, the fundamental at 16dBm being filtered out.

The mixer is based on the National *LMX2216*, which contains a low-noise amplifier, not used here. Output from the mixer goes through a simple band-pass filter to reduce aliasing on the spectrum analyser. Harmonics and sum-and-difference frequencies from the oscillator mean that one must take care in measurement to observe the correct signal.

Mixer and oscillator should be mounted on copper-clad board with all ground connections soldered to the copper. Any tracks should be kept few and short (a 1in wire represents 25nH). Active devices should be decoupled on supply pins. Small capacitors are s-m COG types and rf connections should be made via 50Ω connectors.

(D52c)

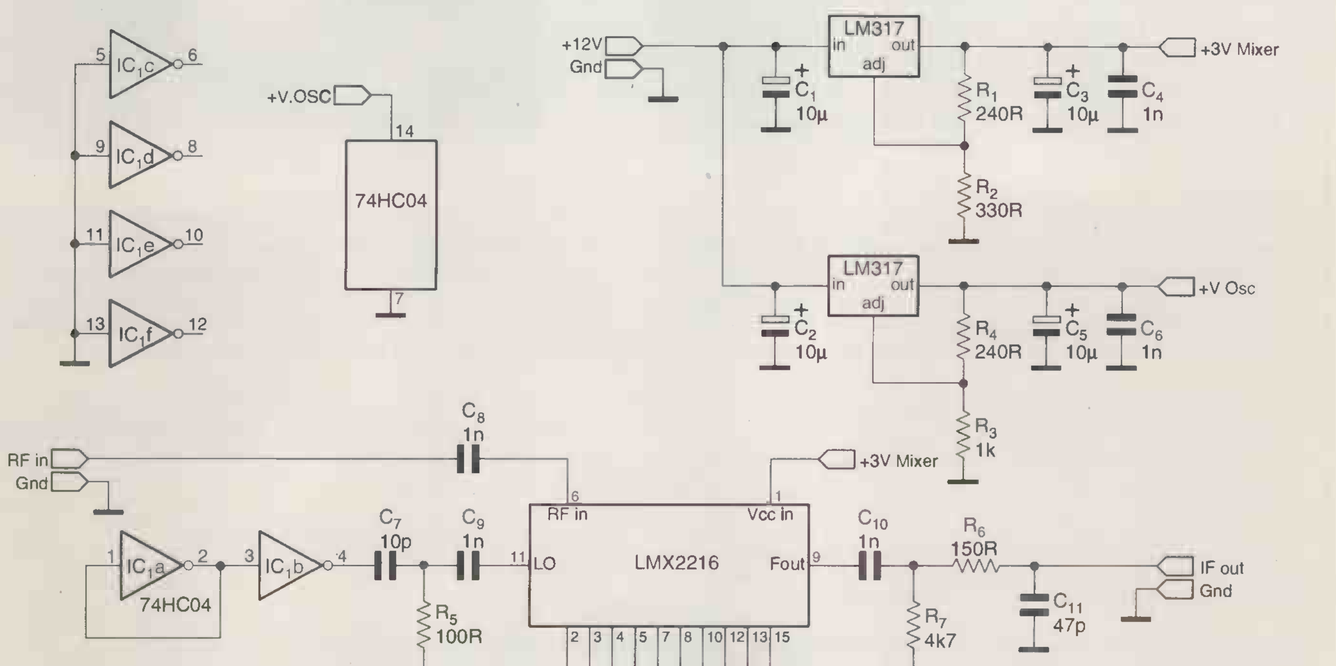


Richard Jacklin
Midhurst, West Sussex
D52

†. Forster, I, 'When is a gate not a gate?', *Electronics World*, December 1996, p.956.

V_{supply}	Frequency	V_{supply}	Frequency
2	80	4	209
2.5	121	4.5	225
3	157	5	239
3.5	186	5.5	5.5

Using a 10MHz spectrum analyser to monitor a 550MHz signal. Inverter gates used as an oscillator produce the necessary harmonics.



(D52a)

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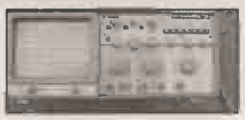

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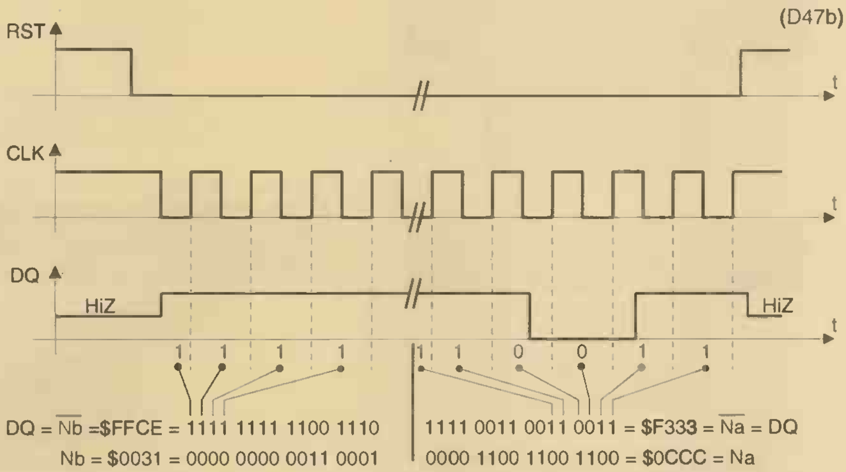
Needing two reference voltages to be pc-controlled, this simple and inexpensive circuit came into being. Only a single power supply is needed and there is an internal reference voltage in the *AD7243* a-to-d converters.

Communication with the converters is by way of the pc parallel port, the converters being in series with sync. and LDAC connections to allow the use of only three wires from the pc.

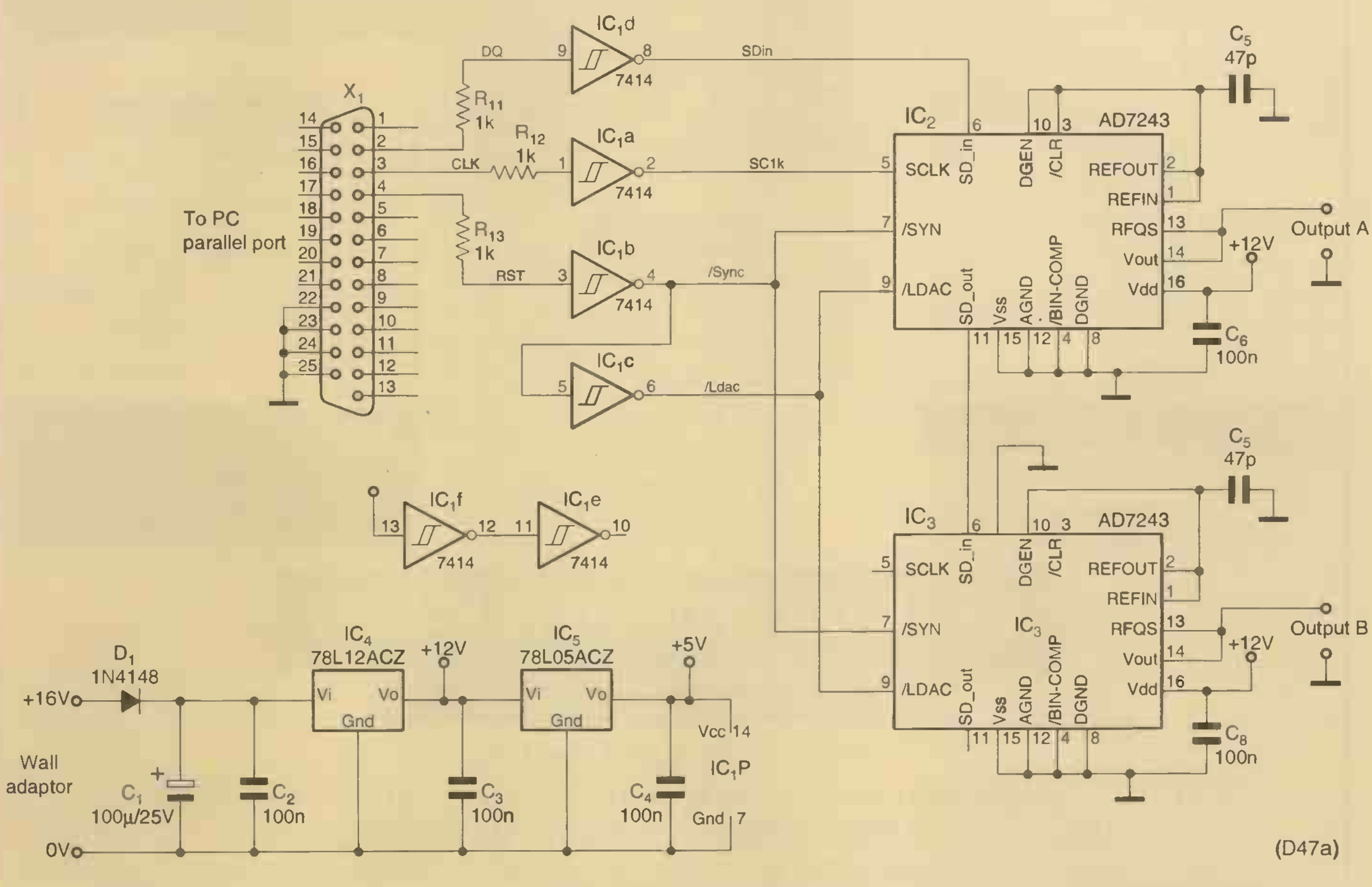
You can see from the timing diagram that N is between zero and 4095, as the converters are 12-bit types, and the reference voltage is 5V. N is determined by $N = V(4095 / 5)$, where V is the required output voltage. As an example, to obtain a voltage of 4V at B and 30mV at A, $N_B = 3276$ and $N_A + 49$.

In the diagram, the data sent is the inverse of the calculated N, since it is inverted in the *7414* schmitt inverters. Firstly, the converters are validated by reset going low, the clock also going low as data input is active on rising edges, the converter reading data bits on positive-going edges. The data word for the second converter is sent first, being a 16-bit word to include four zeros, most significant bit first, the data word for the first converter then following. Reset and clock then return high and the transmission stops.

J M Terrade
Clermont-Ferrand
France
D47



Output voltage is adjustable from zero to 5V by data transmitted from pc's parallel port.



Simple routine, written in standard C, for controlling the interface.

```
/*----------------------------------*/
/* 12-bit d-to-a for PC V1.01    -NA4PC-   */
/*----------------------------------*/
#include <stdlib.h>
#include <stdio.h>
#include <dos.h>
#include <bios.h>
/* Datas declaration and initialisation *********************/
short LPT=0;                    /* short for short integer : 16 bits */
char  RST=0, CLK=0, DQ=0;       /* char  for byte          :  8 bits */
short initLPT()                 /* Find parallel port address */
{
 LPT = peek(0x0040, 0x0008);  /* initialisation of port adresses */
 if( LPT == 0 )   printf("No parallel port available.\n");
 else             printf("Parallel port installed at $%X\n", LPT);
 outportb(LPT, 0);              /* port outputs initialisation */
 return(LPT);
}
void outLPT()                   /* write RST, CLK and DQ to LPT port */
{
 unsigned char byte;
 byte = (RST<<2) + (CLK<<1) + DQ;
 outportb(LPT, byte);
}
void out16b(short number)      /* test and send each of 16 bits */
{
 register unsigned short masque=0x8000;
 do
   {
    if( number & masque )   DQ=0;   /* data bit is 1 */
    else                    DQ=1;   /* data bit is 0 */
    outLPT();                       /* write bit DQ to LPT port /
    CLK=1;  outLPT();               /* Clock active edge */
    CLK=0;  outLPT();               /* Clock return down */
    masque >>= 1;
   }
 while( masque );                  /* 16 loops */
}
void writeval(short Na, short Nb)  /* transmits Na and Nb to converters */
{
 RST=1; CLK=0; DQ=1; outLPT();      /* Start of transmission */
 out16b(Nb);                       /* write Output B */
 out16b(Na);                       /* write Output A */
 RST=0; CLK=0; DQ=1; outLPT();      /* End of transmission */
}
#define ESC    0x001B
void main(short nbarg, char *tabarg[])  /*----------------------*/
{
 short  quit;        /* program output flag */
 char   car;         /* key entered */
 short  Na, Nb;      /* numbers to be write into converters */
 printf("\n\n12 bits D/A for PC V1.01 - CopyRight (C) - J.M.TERRADE - 1998\n");
 if( !initLPT() )   exit(0);
 quit=0;  Na=0;  Nb=0;
 printf(" A     : Modify the value for output A.\n"\
        " B     : Modify the value for output B.\n"\
        " ESC   : Exit Program.\n\n");
 do
  {
   while( !bioskey(1) );           /* keyboard scan */
   car = ( bioskey(0) & 255 );
   switch(car)
     {
      case ESC:  sortie=1;   break;
      case 'a':
      case 'A':  printf("Enter Value output A : "); fflush(stdout);
                 scanf("%i", &Na);
                 if( Na<0 ) Na=0;    if( Na>4095 ) Na=4095;
                 break;
      case 'b':
      case 'B':  printf("Enter Value output B : "); fflush(stdout);
                 scanf("%i", &Nb);
                 if( Nb<0 ) Nb=0;    if( Nb>4095 ) Nb=4095;
                 break;
      default :  break;
     }
   writeval(Na, Nb);
  }
 while( !quit );
}
```

Software description

According to Analog Devices' datasheet, in order to write a 12-bit number, the algorithm has to follow these rules :

```
/Ldac=1        wait state
/Sync=0        data transmission validation
/Sclk=0        reset the clock

do 16 times :  (16 bits to write : 4 zeros and
12-bit number)
   Sclk = 1    set clock
   Set SDin    MSB first, LSB last
   Sclk=0      reset clock

/Sync=1        stops transmission
/Ldac=0        data transmission inhibition
/Ldac=1        return to wait state
```

Since the 74HC14 is an inverter, the following relations are to be considered before reading the simple C program witch is used to drive the converters.

```
RST = /Ldac = //Sync = Sync
CLK = /Sclk
DQ = /SDin
```

The structure for the C program is:

```
Main loop :
  Read numbers to be sent : Ng et Nb
  Set RST=1
  Send data for Ng    /* call sub-routine */
  Send data for Nb    /* call sub-routine */
  Reset RST=0
End

Sub-routine (Send word N) :
  Set Numbit = 15    MSB first    /* Numbit is
the rank of the actual bit */
  do :                    /* 16 bits : 16 times */
    CLK=0
    If Numbit=1   then DQ=0
    If Numbit=0   then DQ=1
    wait
    CLK=1   (write 1 bit)
    wait
    Numbit = Numbit - 1
  while Numbit # 0
end of sub-routine
```

Automatic bathroom light and 'in use' indicator

This is for use in bathrooms with automatic door closers; it switches the light on and off and indicates whether anyone is in there. It uses one 5V supply, has no mechanical contacts and has proved reliable, **Fig. 1**.

On the door frame are an infrared led and detector, separated by an opaque strip that moves with the door. As the door opens, the strip uncovers the led and detector and the voltage across D_2 falls to a low level.

Comparator IC_{2a} output is therefore high when the door is closed and low when it is open; C_1 prevents any uncertainties while the door is opening and closing. For each closure of the door, there is therefore a low-to-high transition at A, as in **Fig. 2a**. Comparator IC_{2b} performs the reverse function, as seen in Fig. **2b**.

The *7474* D-type flip-flop IC_{1a} indicates a presence behind the door, being driven by rising edges from U IC2a, while IC_{1b} drives a relay to turn the light on and off and is driven by rising edges from IC_{2b}.

At switch-on, R_3C_3 clear the flip-flops and, since both Q outputs are low, the relay turns the light on, regardless of whether the door is open or closed, and the occupancy light is off.

When someone goes in, the door opens and closes, or just closes, and the light stays on and the indicator turns on. When the person leaves, the position reverses so that the light is turned off and the indicator goes out.

A R Jayan
Electronics Research and Development Centre
Vallayambalam
Thiruvananthapuram
D53

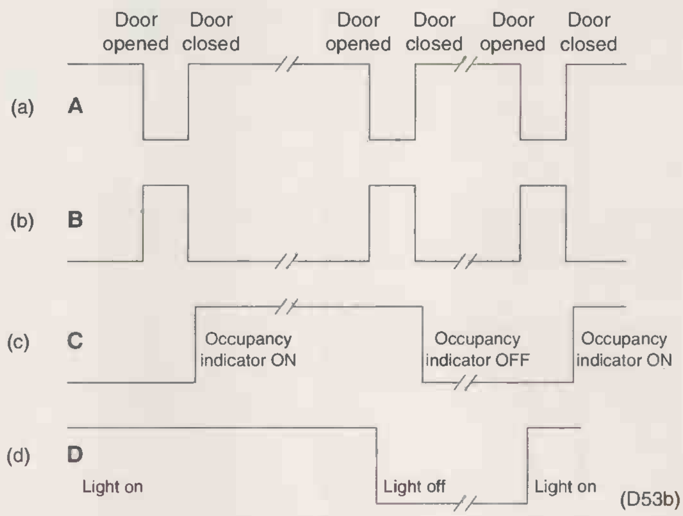


Fig. 2. Logic for the relationship between door openings/closings and indications.

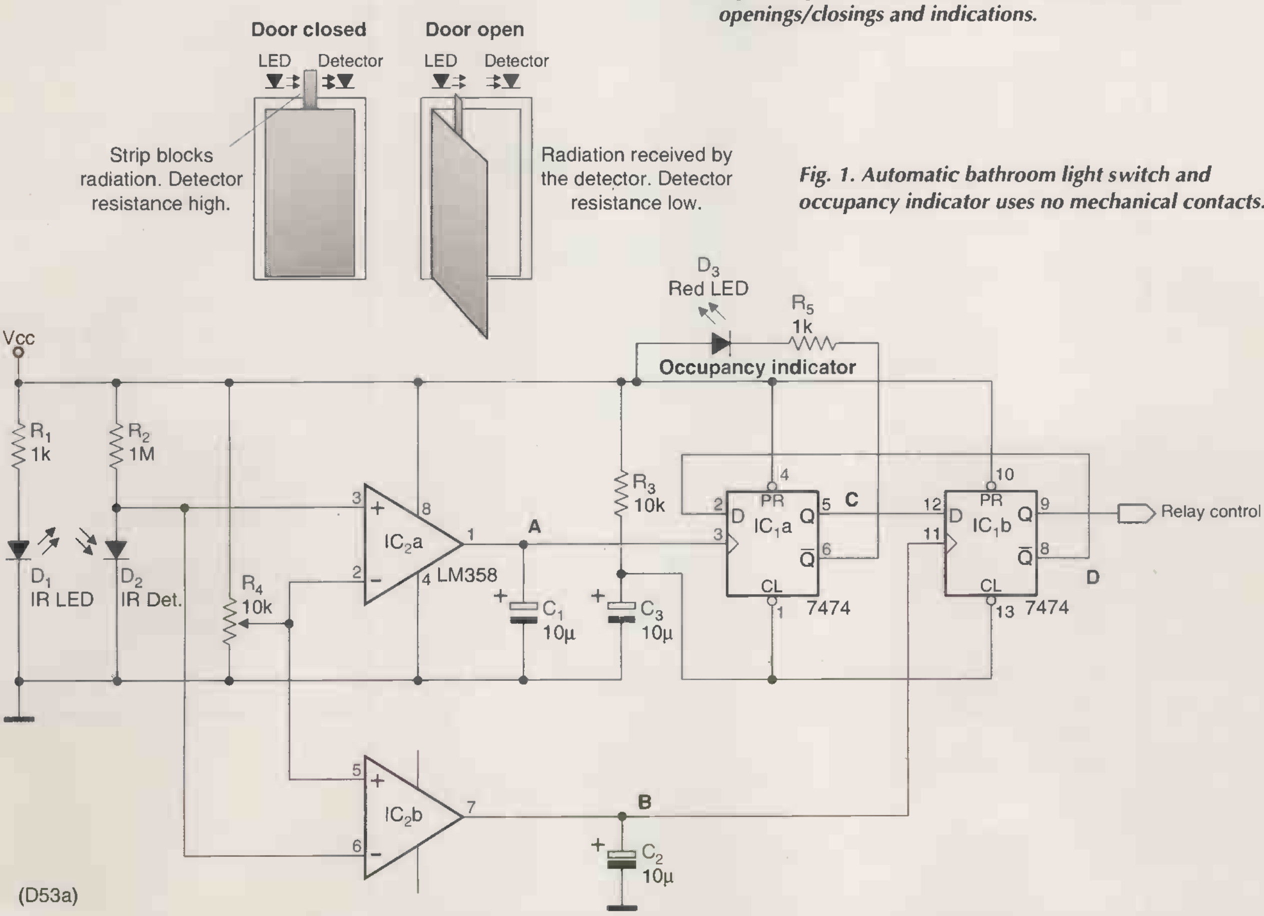


Fig. 1. Automatic bathroom light switch and occupancy indicator uses no mechanical contacts.

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Specifications

Switch position 1

Bandwidth	DC to 10MHz
Input resistance	1MΩ – i.e. oscilloscope i/p
Input capacitance	40pF+oscilloscope capacitance
Working voltage	600V DC or pk-pk AC

Switch position 2

Bandwidth	DC to 150MHz
Rise time	2.4ns
Input resistance	10MΩ ±1% if oscilloscope i/p is 1MΩ
Input capacitance	12pF if oscilloscope i/p is 20pF
Compensation range	10-60pF
Working voltage	600V DC or pk-pk AC

Switch position 'Ref'

Probe tip grounded via 9MΩ, scope i/p grounded

NEW PRODUCTS

Please quote *Electronics World* when seeking further information

Clock adapter

A single-chip, dual phase-locked loop for synthesising two simultaneous output clocks synchronised to a reference clock for WAN systems has been introduced by Exar. The XRT8001 has an ST Bus capability for WAN and ISDN applications. It synthesises two low-jitter clocks with standard frequencies, phased-locked to the system reference timing. Input frequencies accepted include 8kHz, nx56kHz, nx64kHz, nxT1 and nxE1. It can be programmed to generate output frequencies from 1.544 to 2.048MHz and one, two, four or eight times 2.048MHz.
Exar
Tel: +33 1 3458 7676
Enquiry No 501

Schottky diodes

Seven Schottky barrier diodes launched by Zetex include three single-diode devices in the surface-mount SOD323 package. Dual-diode devices are available in the SOT323 package, in either common cathode

or series pair configurations. Breakdown voltage is a minimum 70V for the ZUMD70-04 and ZMS2800 parts at a current of 10μA. Power dissipation at 25°C is 250mW for the SOD323 devices and 330mW for the SOT323 packages. Forward voltage is 410mV maximum at 1mA, except for the 320mV ZUMDS4C. Capacitance is 2.0pF at 1MHz for the ZMS2800.
Zetex
Tel: 0161 622 4422
Enquiry No 503

Ethernet control on single-chip

To provide Ethernet capability for networking products and information appliances, National Semiconductor has launched the DP83815CVNG MacPhyter single-chip 10/100 PCI Ethernet controller and physical layer transceiver. It is for implementing 10 and 100Mbit/s Ethernet LANs for adapters, LAN-on-motherboard and information appliance applications such as set-top boxes and Windows terminals. The chip is capable of error-free reception at upwards of 140m and has a power consumption of 170mA (560mW) during full operation and 10mA (33mW) in sleep mode. Remote management features include wake-on-LAN and PXE 2.0 support.
National Semiconductor
Tel: 08702 402171
Enquiry No 502

Op amp

Distributor Silicon Concepts has introduced Burr-Brown's OPA635 voltage-feedback operational amplifiers. They have single supply operation and rail-to-rail output for use in communications, consumer video and battery-powered applications. The family consists of the OPA631, OPA632 and the higher bandwidth OPA634 and OPA635 (150MHz for a gain of two). Features include +3 and +5V operation and zero power disable (OPA632 and OPA635). They are suitable for analogue-to-digital converter buffering and video line driving. The OPA631 and OPA634 are available in SO-8 and SOT23-5 packages. The OPA632 and OPA635 come in SO-8 and SOT23-6 packages.
Silicon Concepts
Tel: 01428 761603
Enquiry No 504

DC/DC converter

Newport has introduced 2W, 2:1 input range DC/DC converters for input voltages between 9 and 18V. Supplied in 7-pin SIPs with dimensions of 21.8 x 11.1 x 9.2mm, the NDL converters are for portable applications operating with non-

standard voltages or voltages that can fluctuate with time. Available with single-ended output voltages of 5, 9, 12 and 15V, the devices have 1kV DC galvanic isolation between input and output.
Newport Components
Tel: 01908 615232
Enquiry No 506

Op amp

Samsung now has 38 and 43cm TFT LCDs with viewing angles of up to 80° in all directions using coplanar electrode technology. Brightness is up to 200cd/m² and they can show 16 million colours. Supply voltage is 5V. The 38cm LTM150XS and 43cm LT170E2 have display sizes of 304.1 by 228.1mm and 337.9 by 270.3mm respectively, and power consumption of 13 and 30W.
Samsung Semiconductor
Tel: 0208 380 7200
Enquiry No 505

Combined memory

Combomemory, introduced by SST, is a monolithic integration of flash and SRAM in a standalone device. For handheld, battery powered applications, products are available with up to 4Mbit of flash and 1Mbit of SRAM on one chip. Also available is the MCP multi-chip package product combining 8Mbit of flash and 2Mbit of SRAM. The monolithic (31 series) and MCP (32 series) products are for use in pagers, cell phones, GPS systems, PDAs, portable DVD players, digital cameras and camcorders.
Silicon Storage Technology
Tel: 01932 221212
Enquiry No 507

CPU modules

The MOPSlcd4 open PC system CPU with XGA graphics onboard has recently been launched by SST. Available in PC/104 size, it has a processing performance equivalent to a Pentium P75. There are two RS232C, plus LPT, floppy and EIDE interfaces. Boot counter and real-time clock are integrated as standard control functions. The 4Mbyte of onboard main memory can be expanded with standard DIMM modules up to 36Mbyte using the lower DIMM socket. The upper socket is a Jumptec intelligent panel adaption interface for connecting LCD

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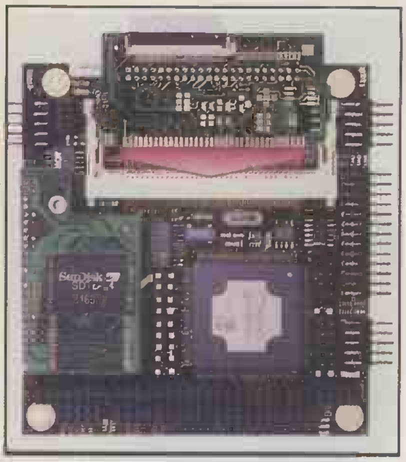


flat panels. The onboard PC C&T graphics controller supports mono-LCD, TFT and STN displays with resolutions up to 1280 x 1024. The 2Mbyte of video memory allows colour depths up to 16 million colours. A bootable bios compatible flash hard disk with 1.6Mbyte is onboard.
Diamond Point
Tel: 01634 722390
Enquiry No 508

Media bay connector

For media bay applications, a vertical board-to-board connector from JAE is a 0.6mm pitch device that integrates power and signal contacts. The PD3

lets peripherals such as CD-ROMs and floppy disc drives be connected to a bay slot on a notebook computer while it is in use. Due to the shape of the insulator, the connector makes a click to confirm locking of the peripheral has happened. It has eight contacts for power and 80 for signals, with respective current ratings of 3 and 0.5A. Two mating heights are available – 5.5 and 7.5mm – from receptacle board to the centre of mating. It will allow a mating dislocation of more than ±1.5mm for width and ±1mm for height.
JAE Europe
Tel: 01276 404000
Enquiry No 510

ATM SAR controller

Toshiba Electronics has announced an ATM Forum compliant 155Mbit/s segmentation and reassembly (SAR) chip. The TC358561F has multiple virtual path (VP) level rate shaper and individual 4095 virtual channel (VC) level rate shaper. For high-speed servers, routers and switches, the device connects legacy LANs to the ATM backbone and shapes VP and VC channel with arbitrary VPIs.
Toshiba Electronics
Tel: 00 49 211 52960
Enquiry No 511

Scart switching devices

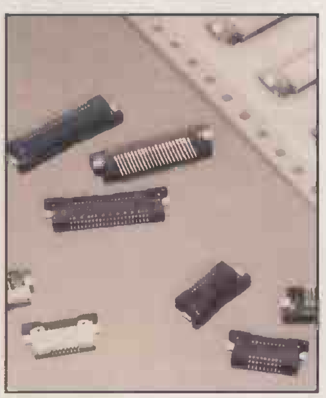
A second device for managing scart switching functions has been launched by TDK. The Avpro 5002 provides two scart interfaces that support Canal+ and BSkyB applications. Switching functions for analogue audio and video signals are performed. Applications include VCRs, televisions and set-top boxes for digital TV, satellite and cable. The device complements the 5003, introduced last year as a single chip way to get a three-scart interface with control. The 5002 includes an encoder-DAC interface, audio and video drivers and a –5V power supply rail that eliminates the need for AC coupling capacitors on the audio outputs. Features include programmable RGB gain and flexible audio routing. The 5002B adds audio switching functions for the BSkyB digital satellite service, including the control and summing of two external audio signals used with the on-screen programme guide.
TDK Semiconductor
Tel: 0208 443 7061
Enquiry No 512

DC-to-DC converter

Vicor has Increased the output power of the 24V (21 to 32V) input VI-200 DC-to-DC converters from 150 to 200W. The increase applies to output voltages of 5, 10, 12, 15, 24, 28 and 48V. For output voltages under 5V, output current is increased from 30 to 40A. There are 11 standard input ranges from 10 to 400V and nine standard output voltages from 2 to 48V.
Vicor
Tel: 01276 678222
Enquiry No 513

Infra-red module

Scenix has added a module to its virtual peripheral library that lets system OEMs incorporate standard wireless infra-red communications. The software module uses an SX microcontroller as a hardware platform and implements the lower levels of the IrDA standard and the high-level Ircomm interface protocol, providing short-range wireless communications for embedded applications. Its uses range from giving portable devices, printers and PCs IR connectivity capabilities to allowing communications with toys. The module uses the SX's ability to re-send data on request to eliminate large data buffers. It also uses the 50Mips performance of the MCU to shape the IrDA pulses without external hardware.
Scenix Semiconductor
Tel: 001 408 327 8888
Enquiry No 514



Digital Voice Systems

Digital Voice Systems has made available the AMBE-2000 vocoder chip for commercial, consumer and military communications applications. It delivers speech at 4kbit/s and can operate at user-defined bit rates between 2 and 9.6kbit/s. An integrated convolutional FEC encoder with a built-in Vitterbi decoder is capable of 4-bit soft-decision decoding and operation at bit error rates of 10 to 20 per cent using R=0.25. Power consumption is 3V. Features include full or half-duplex operation, automatic voice and silence detection, adaptive comfort noise insertion, DTMF and call progress tone.
Digital Voice Systems
Tel: 001 781 272 4830
Enquiry No 509

Right angle connectors

AVX now has right angle, fixed single sided contact connectors for enclosures in the handheld and portable electronics markets. The 6250 and 6252 0.5mm pitch surface mount connectors are 0.9mm high. The 6250 has a single sided bottom contact and the 6252 a top contact. Both are ZIF connectors with between six and 30 contacts each capable of handling up to 0.4A and 50V. Packaging options include taped and reeled for SMT production.
AVX
Tel: 01252 770000
Enquiry No 515

3.3V preamplifier

Microcosm Communications has announced the MC2007 transimpedance amplifier for small form factor transceiver applications. Made with a digital CMOS process, the amp's performance is equivalent to GaAs ICs. It is for use with modules with 65mW power consumption at +3.3V supply and continuous operation to over 0dBm. Its 1mm square die size fits into TO cans. It supports a 140MHz bandwidth, allowing an operating range suitable for 100, 125, 155 and 200Mbit/s, typically more than 35dB power supply noise rejection and a typical –39dBm sensitivity at 155Mbit/s.
Microcosm Communications
Tel: 01179 302400
Enquiry No 516

Cable extension

Black Box has launched the Cat 5 KVM Micro Extender to let a workstation be placed away from its CPU. Extension can be up to 50m using a standard Category 5 cable. It can handle resolutions up to 1280 x 1024 and it is suitable for kiosks and service tills.
Black Box Catalogue
Tel: 0118 965 5100
Enquiry No 517

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256Mbit SDRAMs

Toshiba is producing 256Mbit SDRAMs on its 0.18µm process for applications in servers, mainframes, networks and notebook computers. They are suitable for use in 1Gbyte DIMMs and 256Mbyte SO-DIMMs.
Toshiba Electronics
Tel: 00 49 211 52960
Enquiry No 518

TV processors for digital video

Two processors for use with its Nexperia digital video platform for high-definition TV receivers and set-top boxes are launched by Philips. The NX-2600 and 2700 are system-on-silicon ICs based on an embedded 32-bit Trimedia VLIW processor core. They can handle transport stream demultiplexing, audio and video decoding including MPEG-2 MP@HL, reverse communications channel, Java and Internet browser applications. They support multiple digital broadcast standards, including all 18 ATSC DTV formats and the DSS digital satellite system.
Philips Semiconductors
Tel: 00 31 40 272 2091
Enquiry No 519

Digital Ethernet physical interface

Texas Instruments has added Mysticom's Mystiphy 110 digital Ethernet physical interface to its DSP-based Timebuilder Asic family. When used with DSPs, the phy will let networking users integrate multiple Ethernet phys onto a digital Mac, making it suitable for applications such as network interface cards, hubs, routers, switches and voice-over-IP systems.
Texas instruments
Tel: 01604 663000
Enquiry No 520

Interactive video display

Digital View Interactive has an integrated LCD-based interactive video kiosk, 35mm thick and operating from a 12VDC power supply. Designed as a single chassis, the Viewstream has an integrated video delivery system. It integrates full colour TFT LCD flat screens (from 6.4in. to 18in.), with all panel control electronics, interactive touch screen and a video playback system into a 35mm deep unit offering.
Digital View
Tel: 0181 236 1112
Enquiry No 521

Interactive video display

Diamond Point is offering JUMPtec's 80486-based DIMM-PC. It integrates the complete functionality of an 80486SX motherboard with CPU, system BIOS, 16Mbyte DRAM, keyboard controller and real time clock. The module runs at clock speeds of 33MHz or 66MHz and incorporates 16Mbyte IDE compatible flash hard disk. It measures 68 x 40mm.
Diamond Point
Tel: 01634 722390
Enquiry No 522

High value electrolytic cap

Designed for mounting directly onto a PCB, the high C/V, GK-HH series of electrolytic capacitors from Nichicon (Europe), is available in a range of sizes: 35mm dia x 63mm long to 40mm dia x 100mm long. Auxiliary terminals are provided which ensures secure, anti-vibration mounting on the PCB. The series has an operating temperature range of –40 to +105°C (16 to 250V) and –25 to +105°C (400V). This provides a high load life,

60V DC/DC converter

The PKG 48 to 60V input DC/DC 60W power modules from Ericsson are for low voltage digital and broader analogue applications. They deliver power without needing a heatsink, and withstand case temperatures up to 100°C. Weighing 75g, the PKG 4319 P1 provides a 2.5V 15A output, while the PKG 4625 PI offers dual 15V outputs, with either output capable of sourcing up to 3.2A within a total output of 60W. Protection and control facilities are included as standard for IT and telecoms systems. The 4625 PI can maintain 86 per cent efficiency from 25 to 60W output and the 4319 PI 78 per cent efficiency from 20 to 100 per cent of full load. Both can be operated in parallel and include overcurrent and short circuit protection. As well as remote control and automatic shutdown under low input voltage conditions, the output voltage can be adjusted using an external resistor. The output can be adjusted between 2.25 and 2.75V for the 4319 PI and 12.0 and 16.5V for the 4625 PI.
Ericsson
Tel: 01793 488300
Enquiry No 520

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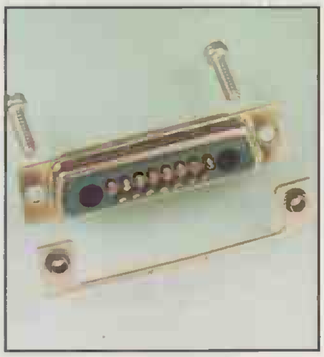
which for this series is 64,000 hours at 55°C. Performance characteristics are working voltage 16 to 400V and capacitance range 560 to 68000pF, tolerance ±20 per cent.
Nichicon
Tel: 01276 685393
Enquiry No 523

Power resistors

Metal film moulded power resistors with a novel termination feature have been released by Vishay. The Vishay Dale SM power metal film resistors are available at both five per cent and one per cent tolerances. The three resistors include 0.5W (WSF2012), 1W (WSF2515), and 2W (WSF4527) versions offering a resistance range from 5Ω to 10Ω. The company says the resistors can be used as SM replacements for higher-wattage axial leaded components. A flexible wrap around terminal has been especially designed for automotive applications and eliminates the solder fillet cracking issues that are common to larger-sized thick film components.
Vishay Intertechnology
Tel: 00 49 9287 71 2282
Enquiry No 524

D-type speedy nut plates

Available from KEC is a range of D-type nut plates that is designed for speedy panel mounting of all sizes of D type subminiature connectors. Manufactured by Fastener Specialty, these CostSaver nut plates can be used for assembling both circular and D type connectors and other components in confined spaces behind panels, inside boxes and in awkward bulkhead areas. The D-type nut plates consist of a stamped aluminium alloy plate, shaped and fitted with captive nuts to avoid the need for separate nuts and



washers. Because tools are not required, less space is needed behind the panel and connectors can be assembled closer together.
KEC
Tel: 01189 811571
Enquiry No 525

RFI fieldbus connector

Radiatron is stocking three additions to the Erni bus interface connector range of field-wireable bus connectors. The original colour coded bodies, the established method for

identifying CAN, Bitbus, Interbus and Profibus connectors, are available with an internal RFI screen coating, an expanded range of cable entry options, and an ESD version which fully insulates all exposed elements, including mounting screws.
Radiatron
Tel: 01784 439393
Enquiry No 526

EEPROM in small package

The first in a range of serial EEPROMs housed in the SBGA chip scale package has been launched by STMicroelectronics. The M24C16-REA6T has an area of 3.3mm² and a height of 0.7mm. The memory provides 16kbits of non-volatile storage organised as 2048 x 8 bits. In addition to byte-level read/write operation, the device also offers a page write mode (up to 16 bytes). The device operates over a 1.8-3.6V power supply range.
STMicroelectronics
Tel: 00 33 450 402532
Enquiry No 527

Digital multimeter

Fluke's latest range of digital multimeters, announced earlier this year, extended the capabilities of the firm's 80 series meters. Designated the 87 and 89 series IV, it adds dBm, 100kHz bandwidth and true rms AC+DC voltage and current measuring capabilities. The meter supports 0.025 per cent accuracy and over 50000 counts of resolution on a

multiple reading display that includes a secondary display and a real-time clock to time-stamp critical measurements. Another feature is the meter's improved startup sequence. In addition to the AC capabilities, the DMMs measure V and mVdc, ohms, amps, capacitance, conductance, frequency, and temperature.
Fluke
Tel: 01923 240511
Enquiry No 528

300MHz Cat 6 cable tester

Networking distributor Wadsworth is offering its first handheld tester to offer users and installers the ability to test structured cabling networks up to and beyond the draft Category 6 specifications. The Wavetek LT8600 is a 300MHz, Level III accuracy tester that exceeds the requirements for the emerging Category 6/Class E 250MHz testing standards and that can perform all power sum measurements up to 300MHz. To simplify testing the unit stores up to 1500 records and incorporates special 'hard keys' that allow the user to perform single tests without scrolling through a series of menus. Providing up to 15 different tests that can be performed either individually or as part of a test suite, the unit supports two-way return loss, power sum, NEXT, ACR and ELFEXT tests.
Wadsworth
Tel: 0181 268 6500
Enquiry No 529

Data logger card

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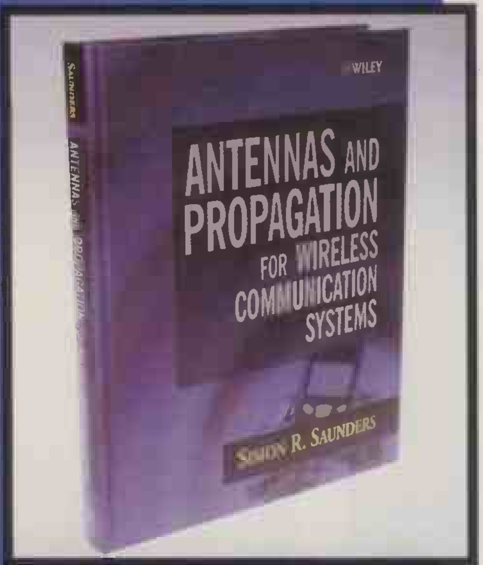

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Tektronix has announced a plug-in module for its TDS200 digital real-time oscilloscope. The TDS2MM module adds fast Fourier transform analysis and four extra measurement functions – automatic rise-time, fall-time, positive pulse-width and negative pulse-width capabilities. It includes serial (RS232), parallel (Centronics) and GPIB ports for printing and remote control of the oscilloscope. The module plugs into the back of the TDS200. Applications include tests on DC power supplies, noise in mixed digital and analogue systems, line-current harmonics, signal distortions and vibration systems
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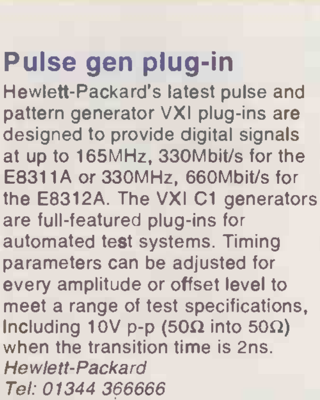

Signal analyser

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500MHz scope

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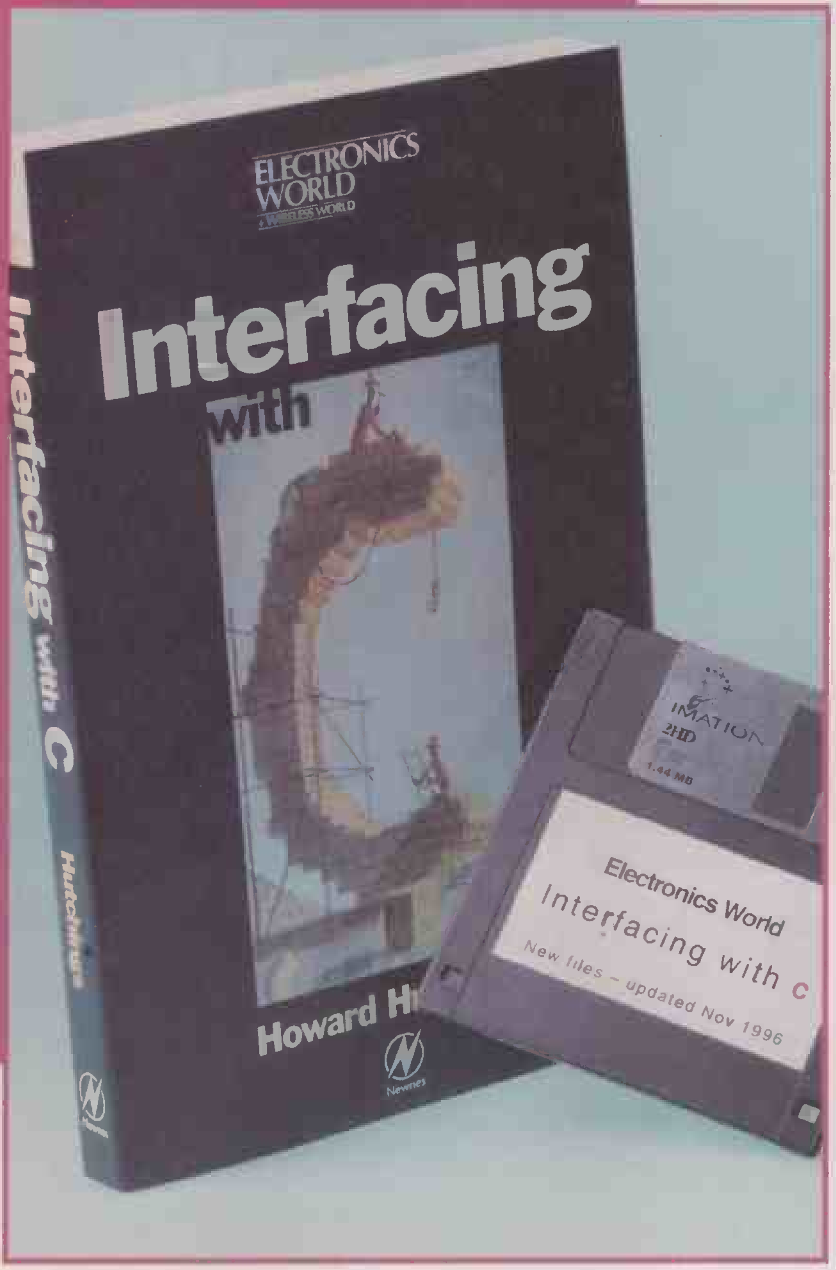

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Interfacing digital audio

Patrick Gaydecki describes hardware and software issues relating to interfacing two new stereo audio converters to a microprocessor via serial links. Patrick's description revolves around a DSP56k processor, but the information will help anyone wanting to design with these high-performance, easy-to-interface audio d-to-a and a-to-d converters.

In this article is information for interfacing the CS5330/31 stereo analogue-to-digital converter and CS4330/31 stereo digital-to-analogue converter to a DSP56002 digital signal processor. Technical issues include the hardware interconnection, critical system timing signals and software modules for receiving and transmitting digital data.

The CS5330/31 is a stereo a-to-d converter while the CS4330/31 is a stereo d-to-a converter. Both are 18-bits wide. We chose the DSP56002 digital signal processor for our design example since it's an industry standard. There are many hardware and software strategies that could be used to interface these ICs, but we have narrowed our discussion down to the more straightforward techniques.

Analogue-to-digital conversion

The CS5330 and 31 are complete 18-bit stereo a-to-d converters. They perform anti-alias filtering, sampling, and analogue-to-digital conversion, generating binary data for both left and right inputs in serial form.

Alternate left and right channel data are transmitted via a single output. The sampling frequency can be adjusted infinitely between 2 and 50kHz, according to the frequency of a master-clocking signal.

These a-to-d converters use sigma-delta, shortened to ΣΔ, modulation with an oversampling rate equal to 128 times the equivalent sampling frequency. The sigma-delta stage is followed by digital filtering and decimation circuitry, which remove the need for an external anti-alias filter.

The linear-phase digital filter has a pass band to 21.7kHz, 0.05dB pass band ripple and greater than 80dB stop-band rejection. These devices contain a high-pass filter to remove DC offsets, which at a sampling rate of 48kHz, has a –3dB point of 3.7Hz.[3]

Digitising analogue signals

Complementary to the CS5330/31, the CS4330/31 are complete stereo digital-to-analogue converter systems. They include an interpolator, a 1-bit d-to-a converter and an output analogue filter.

Analogue signals generated by these devices are output to separate pins. In essence, these d-to-a converters perform the inverse operations to those of their a-to-d converter counterparts described above.

A digital interpolation filter first up-samples the incoming digital data by a factor of 128. A ΣΔ modulator then generates a 1-bit data stream, which is input to a linear analogue switched-capacitor low-pass filter. This enables infinite adjustment of the sampling frequency between 2 and 50kHz.

Output analogue signals require a simple first-order *RC* filter to eliminate images of the input signal at multiples of 128x the input sample rate.[4]

The CS5330 and the CS5331 differ only in the output serial data format. The CS4330 and the CS4331 differ only in the input serial data format. All devices are available as eight-pin plastic SOICs – a 5.28mm wide surface-mount package – with low power consumption, making them particularly attractive in power-conscious applications or in designs where space is at a premium.

Hardware interconnection

Figure 1 illustrates a simple interconnection strategy between the DSP56002, the CS533x and the CS433x. Both of the data converters are clocked by an external master-clocking signal, fed to their respective MCLK inputs. The serial data out pin of the CS533x, SDATA, connects to the SRD input of the processor.

In addition, the serial output connects to the ground rail by a 47kΩ resistor. This ensures that the CS5330/31 operates in master mode.

In master mode, the serial data clock, or bit clock, SCLK, and the left-right clock, LRCK, are generated as outputs

Patrick is with the Department of Instrumentation and Analytical Science at the University of Manchester Institute of Science and Technology (UMIST).

by the CS5330/31, derived from the the a-to-d converter clock MCLK input.

The LRCK output connects to the SC2 input of the DSP56002, used to accept the frame sync. The SCLK output of the CS5330/31 connects, via an inverter, to the SCK input of the DSP56002. The inverter is necessary because the DSP56002 samples the data present on the SRD input on the negative edge of the bit clock[5], whereas the data generated by the CS5330/31 are valid on the rising edge of the SCLK.

Since the CS5330/31 is operating in master mode, both the LRCK and the SCLK are fed directly as input signals to the CS4330/31, which is operating in slave mode. Because this uses the same clock protocol as the CS5330/31, no inversion of the SCLK signal is necessary.

Finally, the digital data generated as an output by the DSP56002 are fed from the STD pin to the SDATA input of the CS4330/31.

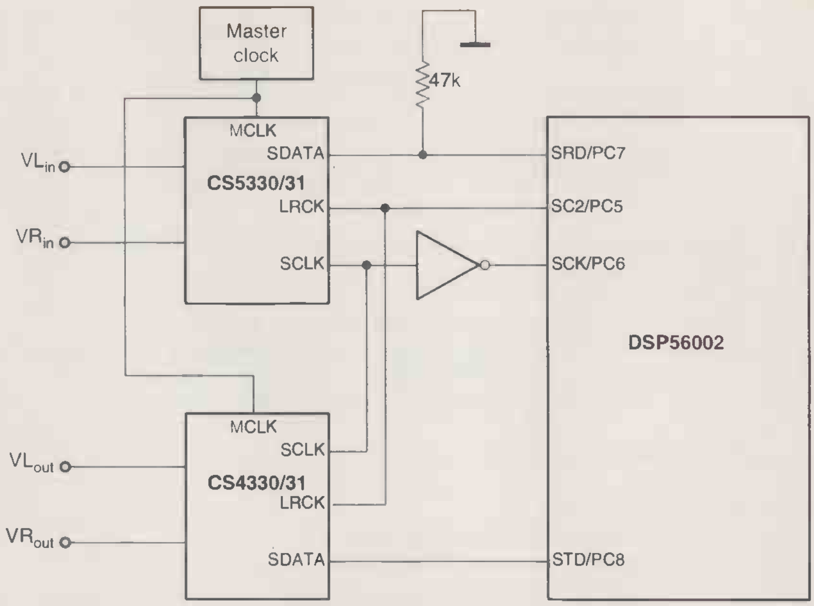


Fig. 1. Simple interconnection method between the DSP56002, the CS5330/31 and the CS4330/31.

Timing considerations and data formats

In master mode, the input clock rate of the CS5330/31 is 256 times the LRCK. This represents an over-sampling ratio of 128 for each channel.

In order to sample each channel at an effective rate of 48kHz for example, a clock frequency of 12.288MHz is required. Similarly, the CS4330/31 expects the same over-sampling ratio when driven by the CS5330/31, Fig. 1.

Figure 2 shows the output data format of the CS5330/31 as used here. Data for the left channel are output during the first half of the LRCK period, and data for the right channel are output during the second.

A total of 32 bits is generated during each half period, and the data are left justified, with the most-significant bit appearing first, on commencement of each half of the LRCK cycle.

Since the CS5330 has 18-bit resolution, the final 14 bits are redundant. This may be viewed another way; as far as the DSP56002 is concerned, the data for each channel occupy four time slots, each one eight bits in length. Hence eight time slots period characterise the entire LRCK.

The data format for the CS5331 is similar, except that it uses the I^2S format. Here, the first most significant bit is delayed by one bit clock period, for handshaking purposes. Figure 2 also shows the input data format expected by the CS4330 and CS4331.

In the case of the C4330, the data are right justified; hence the first 14 bits of any LRCK half-cycle are redundant. For the CS4331 with an externally supplied LRCK – the case discussed here – the data are left justified using I^2S format, i.e. the most-significant bit commences after a delay of one bit clock period.

Reading and writing in network mode

The SSI of the DSP56002 may be configured in normal mode or in network

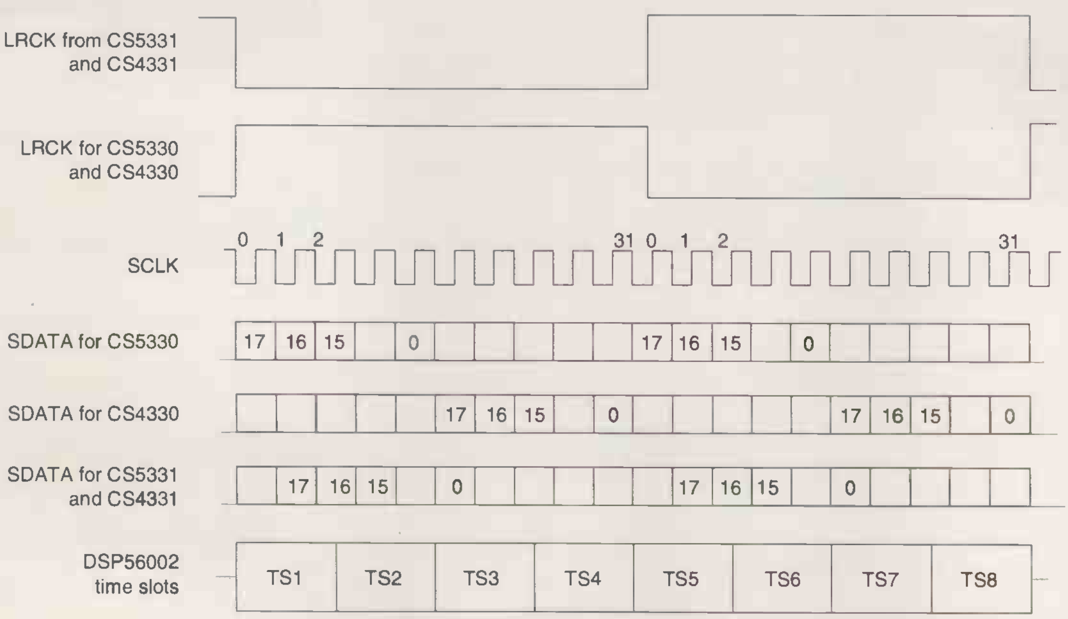


Fig. 2. Timing waveforms for the CS5330/31 and the CS4330/31. These assume the CS5330/31 is operating in master mode, and the CS4330/31 is clocked externally.

mode. In normal mode, a signal input to the SC2 pin is considered a framing signal, i.e. it frames the start and end points of one datum word.

Individual bits are clocked in using the SCK input as a bit synchronisation signal. In network mode, it is assumed that within any one frame, a number of data words are being transmitted in packets termed time slots (TS).

In the case outlined here, the SSI of the DSP56002 is configured in network mode, assuming a time-slot length of 8 bits. The SSI can be configured to accept words that are 8, 12, 16 or 24 bits in length.

In the CS5330/31, the data are left justified. Hence, since the device has 18-bit resolution, only the first three slots of any channel are required.

Furthermore, only the first two bits of the CS5330, or first three bits of CS5331, time-slot 3, are used. These represent the two least-significant bits of the a-to-d converter word. The 8 bits from TS 1 and TS 2, together with the two bits from TS 3 are then combined into a single 18-bit word.

The procedure for writing to the CS4330/31 is similar, with the stages reversed. First, an 18-bit word is decomposed into three 8-bit time slots. For a CS4330, the most-significant bit commences at bit six of TS 2 for the left channel, TS 1 being blank. Lower-order bits follow accordingly in TS 3 and TS 4.

If instead, a CS4331 is being used, the most-significant bit commences at bit 1 of TS 1. The data are shifted one place right since bit 0 is ignored in I^2S format. Lower order bits follow accordingly in the remainder of TS 1, TS 2 and TS 3.

Polled-network mode

Whether in network or in normal mode, data may be clocked into the SSI using polled or interrupt-driven communication.

In a network-mode polled system, the program waits in a loop while the program tests the status of a flag in a status register. When true, this flag indicates the start of the LRCK sequence – the start of the left channel.

The program then proceeds to wait in another loop, testing the status of the flag that indicates a word has been received into the data register. When this is true, it reads and stores the data corresponding to that time slot – time-slot 1 initially.

The program now continues to wait for and read the data words corresponding to subsequent time slots. To use the SSI, it must first be enabled as a synchronous interface, since it has a dual function; it may also operate as a general-purpose i/o port.

Thus, the appropriate bits must be set in the port-C control register, PCC. In this case, the upper five bits must be set. Next, the device must be configured for a particular mode by loading the appropriate words into the SSI control registers A and B (CRA and CRB), located at X:FFEC$_{16}$ and X:FFED$_{16}$ respectively.

For network-mode polled communication, in which the DSP56002 operates as a slave, the bits are set as in **List 1**.

List 2 shows an assembly code fragment that reads data from the CS5330/31 and writes data to the CS4330/31 during all eight time slots using network-mode, polled communication.

Important flags are the receive-frame

List 1. For network-mode polled communication, in which the DSP56002 operates as a slave, bits are set as follows.

Register	Bits	Function
CRA	0-7	Pre-scale modulus: set to 0 (only used if DSP is master).
CRA	8-12	DC: set to 7, since this equals the number of time slots minus 1.
CRA	13-14	WL: set to 0, since this gives a word length of 8 bits.
CRA	15	PSR: set to 0, as this is not needed in slave mode.

Hence CRA = $0000011100000000_2 = 700_{16}$.

Register	Bits	Function
CRB	0-3	Set to 0, as they are not used.
CRB	4-5	Set to 0, external frame + bit clocks supplied by CS5330/31.
CRB	6	Set to 0, as MSB in/out is first and the LSB is last.
CRB	7-8	Set to 0, as the WL bit clock is used for both TX/RX.
CRB	9	Set to 1 for sync clock control, ignored in network mode.
CRB	10	Set to 0 for continuous clock.
CRB	11	Set to 1 for network mode.
CRB	12-13	Both set to enable RX and TX.
CRB	14-15	Not set since interrupts not required, i.e. polled-mode is used.

Hence CRB = 0011101000000000_2 = $\$3A00_{16}$.

The DSP side

Motorola's DSP56002 is an advanced 24-bit fixed-point general-purpose digital signal processor, with 56-bit intermediate resolution. It has a highly parallel architecture, in that it treats program memory space separately from data memory space. This is known as Harvard Architecture.

Harvard Architecture has been extended further in the DSP56002 by sub-classifying the data space into X-data memory and Y-data memory – so-called Super Harvard Architecture. This is because many signal-processing algorithms use two distinct signal vectors. For example, FIR filters need memory to hold the incoming signal, and memory to hold the filter coefficients; FFT routines need memory to hold the real and imaginary Fourier components, and so on.

Each of the three memory areas – program, X and Y data – has its own data and address bus, and all of these connect to the outside world via bus multiplexers. The processor has 256 words of X-data RAM, each 24-bits wide, 256 words of Y-data RAM, and 512 words of program RAM (24 bits). This may not seem very much, but remember that the device is hardware oriented.

Operations that traditionally require many instructions can be implemented here using a single instruction, since the details are implemented in hardware. For example, a complete FFT routine needs only 40 words, i.e. 120 bytes.

In contrast, an FFT routine written on a conventional PC might require several thousand bytes. Since the 56002 uses hardware multipliers and pipelining, it can perform multiplication, accumulation and instruction fetching in a single instruction cycle, i.e. two clock cycles.

The fastest version of the 56002 can be clocked at 80MHz, which means it operates at 40 mega-instructions per second, i.e. 40MIPs. Also incorporated in the device are peripheral system components, including parallel and serial i/o ports. A host interface allows the processor to communicate with other computing devices and peripheral circuitry such as analogue-to-digital converters, digital-to-analogue converters, voice-band codecs and other devices.

For high-speed serial data transfer, its synchronous serial interface, or SSI, is often the preferred choice. It is readily compatible with many other products and it needs only a small number of signal connections and a minimum of glue-logic.[1,2]

sync flag RFS, bit 3 of the SSISR (X:$FFEE_{16}$), and the receive data register full flag RDF, which is bit 7 of the SSISR. When RFS is set, it indicates the start of a frame or LRCK cycle. When RDF is set, it indicates a datum word is present in the receive-data register, RX, located at X:$FFEF_{16}$.

The datum word may be transferred to an appropriate arithmetic register in the CPU or placed into memory. The code here simply reads the data repeatedly into register X0, but does nothing with it.

Once RX is read, the RDF flag is automatically reset. The transmit-data-register-empty flag TDE, bit 6 of the SSISR, is not required in this and all subsequent code described here. This is because the CS4330/31 is operating in slave mode, and data are transmitted by the DSP56002 within the time slots defined by the CS5330/31.

Interrupt-driven network mode

Interrupt-driven i/o can be more efficient than polled i/o since the processor is only interrupted when a specific condition occurs; since the CPU is not locked in a polling loop, it can continue processing data until the status of a specific flag becomes true. When this occurs, the program automatically jumps to an interrupt service routine, which deals with the condition as required.

In order to use interrupt-driven i/o, bits 15 of the CRB, the receive-interrupt enable bit RIE must be set. Register CRA remains the same. When the RIE bit is set, an interrupt is generated when the RDF flag becomes true, i.e. the receive-data register holds a new datum word. Hence,

$$CRB=1011101000000000_2=BA00_{16}.$$

The necessary bits in the interrupt-priority register IPR, located at X:$FFFF_{16}$ must now be set for the SSI; these are bits 12 and 13, i.e. the IPR must be loaded with 3000_{16}.

The interrupts must then be unmasked. This is achieved by ANDing the MR register with FC_{16}, i.e. the lowest two bits are set to 0, enabling all interrupts. When an interrupt occurs, control passes to the interrupt vector whose address is at a specific area in program memory.

For the SSI receive data interrupt used here, the two-word vector space lies between P:$000C_{16}$-P:$000D_{16}$. Hence a JSR instruction is simply placed here to the start of an interrupt service routine whose purpose will be to read the data.

In the program fragment shown in **List 3**, network-mode interrupt-driven communication is used to read the data as each time slot generates an interrupt. However, the code as it stands is incomplete, since the program cannot distinguish the occurrence of the *first* time slot – i.e., it has no knowledge of the time slot order.

In order to be of practical use, the code

List 2. Reading all eight time slots in network mode, polled configuration.

```
        ORG P:$0
        MOVEP #$1F0,X:$FFE1     ;Enable upper 5 bits of SSI
        MOVEP #$700,X:$FFEC     ;Configure CRA
        MOVEP #$3A00,X:$FFED    ;Configure CRB
LRCK    JCLR #3,X:$FFEE,LRCK    ;Wait for LRCK sequence start
TS1     JCLR #7,X:$FFEE,TS1     ;Wait for first datum word, ie TS1

        MOVEP X:$FFEF,X0        ;Read 1st word into register X0 from a-to-d converter
        MOVE A1,X:$FFEF         ;Send data to d-to-a converter
TS2     JCLR #7,X:$FFEE,TS2     ;Wait for second datum word
        MOVEP X:$FFEF,X0
        MOVE A1,X:$FFEF
TS3     JCLR #7,X:$FFEE,TS3
        MOVEP X:$FFEF,X0
        MOVE A1,X:$FFEF
TS4     JCLR #7,X:$FFEE,TS4
        MOVEP X:$FFEF,X0
        MOVE A1,X:$FFEF
TS5     JCLR #7,X:$FFEE,TS5
        MOVEP X:$FFEF,X0
        MOVE A1,X:$FFEF
TS6     JCLR #7,X:$FFEE,TS6
        MOVEP X:$FFEF,X0
        MOVE A1,X:$FFEF
TS7     JCLR #7,X:$FFEE,TS7
        MOVEP X:$FFEF,X0
        MOVE A1,X:$FFEF
TS8     JCLR #7,X:$FFEE,TS8
        MOVEP X:$FFEF,X0
        MOVE A1,X:$FFEF
        JMP LRCK                ;All eight time slots read. Go and wait for
        END                     ;Start of next LRCK.
```

List 3. Reading/writing of all eight time slots in network mode, interrupt-driven configuration.

```
        ORG P:$0
        JMP MAIN                ;Skip interrupt vector space
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        JSR ISR                 ;Jump to ISR. Executed when RDF=1
MAIN    MOVEP #$1F0,X:$FFE1     ;SSI mode
        MOVEP #$700,X:$FFEC
        MOVEP #$BA00,X:$FFED    ;Enable REI for SSI
        MOVEP #$3000,X:$FFFF    ;IPR for SSI
        ANDI #$FC,MR            ;Unmask interrupts
LOOP    JMP LOOP                ;This loop represents the main program
ISR     MOVEP X:$FFEF,X0        ;Start of interrupt routine. Read data
        MOVE A1,X:$FFEF         ;Write to d-to-a converter
        RTI                     ;Return from interrupt
        END
```

List 4. Reading/writing of all eight time slots using interrupts and LRCK identification.

```
        ORG P:$0
        JMP MAIN                ;Skip interrupt vector space
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        JSR ISR                 ;Jump to ISR. Executed when RDF=1
MAIN    MOVEP #$1F0,X:$FFE1     ;SSI mode
        MOVEP #$700,X:$FFEC     ;
        MOVEP #$BA00,X:$FFED    ;Enable REI for SSI
        MOVEP #$3000,X:$FFFF    ;IPR for SSI
        ANDI #$FC,MR            ;Unmask interrupts
LOOP    JMP LOOP                ;This loop represents the main program
ISR     MOVEP X:$FFEF,X0        ;Start of interrupt routine. Read data
        INC A                   ;Increment the TS counter
        JCLR #3,X:$FFEE,IGNORE  ;Find LRCK start, ie RFS=1
        CLR A                   ;If frame start, reset TS counter (a)
IGNORE  MOVE A1,X:$FFEF         ;Write to d-to-a converter
RTI                             ;Don't reset counter if not start of LRCK
        END
```

List 5. For single channel, normal-mode polled communication, in which the DSP56002 operates as a slave, bits are set as follows:

Register	Bits	Function
CRA	0-7	Pre-scale modulus: set to 0 (only used if DSP is master).
CRA	8-12	DC: set to 0, since this equals number-of-words/frame–1.
CRA	13-14	WL: both set to 1, giving a word length of 24-bits.
CRA	15	PSR: set to 0, as this is not needed in slave mode.

Hence CRA=0110000000000000_2=6000_{16}.

Register	Bits	Function
CRB	0-3	Set to 0, as they are not used.
CRB	4-5	Set to 0; ext. frame and bit clocks supplied by CS5330.
CRB	6	Set to 0; MSB i/o is first and the LSB is last.
CRB	7-8	Set to 0, as the WL bit clock is used for both TX/RX.
CRB	9	Set to 1 for synchronous clock control.
CRB	10	Set to 0 for continuous clock.
CRB	11	Set to 0 for normal mode.
CRB	12-13	Both set to 1 to enable RX and TX.
CRB	14-15	Not set since interrupts not required; polled-mode is used.

Hence CRB=0011001000000000_2=3200_{16}.

List 6. Reading a single channel of the CS5330 and writing to the CS4331 in normal mode.

```
        ORG P:$0
        MOVEP #$1F0,X:$FFE1    ;SSI mode
        MOVEP #$6000,X:$FFEC   ;Configure CRA and CRB for 24-bit
        MOVEP #$3200,X:$FFED   ;data, normal mode
LOOP1   JCLR #7,X:$FFEE,LOOP1  ;Wait for 24-bit word
        CLR A
        MOVE X:$FFEF,A1        ;Read data into a
        LSR A                  ;Shift right 1 place for CS4331
        MOVE A1,X:$FFEF        ;Send to CS4331
JMP LOOP1
END
```

shown in **List 3** should be capable of determining the start of the LRCK. This may be achieved by testing the status of the RFS flag when an interrupt occurs. If it is set, this means the LRCK has just commenced a new cycle and the data correspond to the first time slot.

A time-slot counter that records the current time slot should then be initialised to zero. If RFS is not set, then data corresponding to a later time slot are present in the receive data register. In this case, the time-slot counter should be incremented.

This scheme is very similar to the one described on page 6-137 of the DSP56002 Digital Signal Processor User's Manual[1]. **List 4** provides a code fragment which uses interrupts and polling of the RFS to both determine the start of the LRK cycle and read the data with a positional knowledge of the time slots.

Reading and writing a channel in normal mode

The above examples omitted code details dealing with recombination of data after its reception from the CS5330/31, processing and decomposition of the data prior to transmission to the CS4330/31.

Recombination involves weighting and summing the 8-bit words associated with, in this case, the three relevant time slots. Decomposition involves shifting to isolate the appropriate segments of the 18-bit word, and sending these segments out as eight-bit words corresponding once more to the time slots appropriate for the CS4330/31. This requires processing time and may limit the speed of the DSP environment – especially in situations where critical real-time operations are being performed.

One way of removing this difficulty is to treat the CS5330 as a single-channel device – i.e. left channel only – using it in normal mode. Similarly, data can be sent to the right-channel only of a CS4331. The channels switch because the LRCK signal is inverted for the CS4331, Fig. 2.

Since the only difference between the CS5330 in master mode and the CS4331 when clocked externally is a single bit-pulse delay – due to the I^{2}S format involved – a single right-shift operation is all that is required to make the input datum word compatible with the output.

When operating in normal mode, the CRA and CRB registers must be configured to accept 24-bit data. Trailing bits are simply ignored by the system. The LRCK signal is treated as a true framing signal, with only the leading edge of significance to the SSI.

Once this framing signal has been detected, the SSI clocks in all 24 bits of the datum word generated by the CS5330 which may then be processed, shifted one place right and transmitted to the CS4331. For normal mode polled communication, in which the DSP56002 operates as a slave, the CRA and CRB are set as in **List 5**.

The code fragment in **List 6** allows the DSP56002 to read in a full 18-bit word from the CS5330, shift it one place right, and output it to the CS4331. If processing is to be performed, the code would be included immediately after reading the data from the input register.

In summary

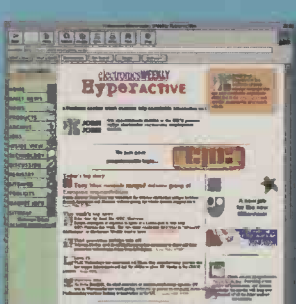
The interfacing strategies described here represent a small number of variations within a wide range of possibilities. In particular, it is possible to configure the DSP56002 as the master device.

Alternatively the expected data input format of the CS4330/31 may be altered by changing its default configurations through the use of a control word. This word is sent via the SCLK input. This is described in detail in reference 4.

However, if you do not wish to change these, the code given here should provide a starting point for successfully exchanging data between these devices. ■

References

1. *DSP56002 Digital Signal Processor User's Manual* Motorola Inc. Document DSP56002UM/AD (1993)
2. *DSP56000 Digital Signal Processor Family Manual* Motorola Inc. Document DSP56KFAMUM/AD (1995)
3. *CS5330/31 8-Pin, Stereo A/D Converter for Digital Audio* Cirrus Logic Inc. Data sheet, document DS138F1 (1997)
4. *CS4330/31/33 8-Pin, Stereo D/A Converter for Digital Audio* Cirrus Logic Inc. Data sheet, document DS136F1 (1997)
5. *DSP56002/DSPL56002 24-bit Digital Signal Processor*, Motorola Inc. Data sheet, document DSP56002/D (1995)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Audio power analysis

Doug Self's investigations into dissipation in audio power systems reveal startling information about the real efficiency of Class-A, and suggest that Class-G is worth a second look now that multi-amp audio systems are becoming the norm.

My last article on this topic showed how the power consumed by amplifiers of various classes was partitioned between internal dissipation and the power delivered to the load.[1] This was determined for the usual sinewave case.

The snag with this approach is that a sinewave does not remotely resemble real speech or music in its characteristics. In many ways it is almost as far from it as you could get.

In particular, it is well-known that music has a large peak-to-mean ratio, or PMR, though the actual value of this ratio in decibels is a vague quantity. Signal statistics for music appear to be in surprisingly short supply.

Very roughly, general-purpose rock music has a PMR of 10dB to 30dB, while classical orchestral material – which makes very little use of fuzz boxes and the like – is 20 to 30dB. The Muzak you endure in lifts is limited in PMR to 3 to 10dB, while compressed bass material in live PA systems is similar.

It is clear that the power dissipation in PA bass amplifiers is going to be radically different from that in hi-fi amplifiers reproducing orchestral material at the same peak level. The PMR of a sinewave is 4.0dB, so results from this are only relevant to lifts...

Recognising that music actually has a peak-to-mean ratio is a start, but it is actually not much help as it reduces the statistics of signal levels to a single number. This does not give enough information for the estimation of power dissipation with real signals.

To calculate the actual power dissipations, two things are needed; a plot of the instantaneous power dissipation against level, and a description of how much time the signal spends at each level. The latter is formally called the 'probability density function,' or PDF, of the signal; more on this later.

The instantaneous power partition diagram, or IPPD, is obtained by running the output stage simulation with a sawtooth input and no per-cycle averaging. Instantaneous power dissipation can therefore be read out for any input voltage fraction simply by running the cursor up the sawtooth.

Figure 1 is the instantaneous power partition diagram for the Class-B complementary-feedback pair case, where the quiescent current is very small. This looks very much like the averaged-sinewave power partition diagram in reference 1, but with the device dissipation maximum at 50% voltage rather than 64% for the sinewave case.

The instantaneous powers are much higher, as they are not averaged over a cycle. There is only one device-power area at the bottom as only one device conducts at a time. Output device dissipation at the moment when the signal is halfway between rail and ground – input fraction 50% – is 76W, and the power in the load is 75W. This totals to 151W, on the lower of the two straight lines, while the power drawn from the supply is shown as 153W by the upper straight line. The 2W difference represents losses in the driver transistors and the output emitter resistors.

All the IPPDs for various output stages look very similar in shape to the averaged-sine PPDs in reference 1, but the peak values on the Y-axis are higher. The IPPD can be combined with any PDF to give a much more realistic picture of how power dissipation changes as the level of a given type of signal is altered.

The probability density function

The most difficult part of the process above is obtaining the probability density function. For repetitive waveforms the PDF can be calculated[2], but

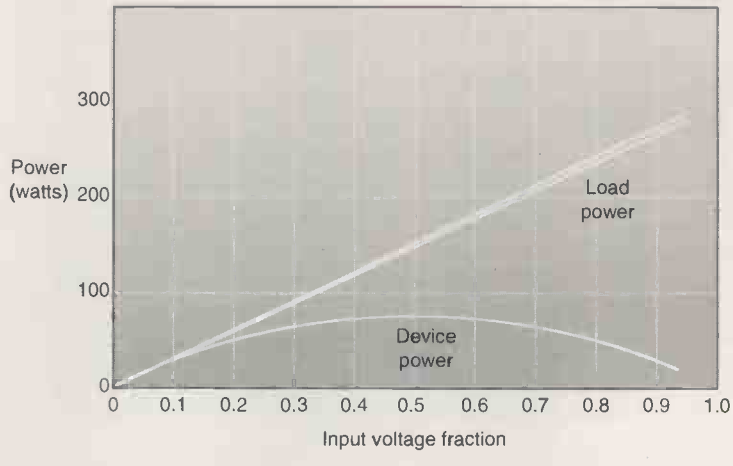

Fig. 1. Instantaneous power partition diagram for Class-B complementary-feedback pair. Power in the output devices peaks when output is at half the rail voltage.

music and speech need a statistical approach. It is often assumed that musical levels have a Gaussian (normal) probability distribution, as the sum of many random variables.

Positive statements on this are however hard to find. Benjamin[3] says, "music can be represented accurately as a Gaussian distribution" while Raad[4] states, "music and mixed sounds typically have Gaussian PDFs". It appears likely this assumption is true for multi-part music which can be regarded as a summation of many random processes; whatever the PDF of each component, the result is always Gaussian as indicated by the Central Limit Theorem.

If the distribution is Gaussian, its mean is clearly zero, as there is no DC component, which leaves the variance – i.e. width of the bell-curve – as the only parameter left to determine. The Gaussian distribution tails off to infinity, implying that enormous levels can occur, though very rarely.

In reality the headroom is fixed. I have dealt with this by setting variance so the maximum value, 0dB, occurs 1% of the time. This is realistic as music very often requires judicious limiting of occasional peaks to optimise the dynamic range.

The PDF presents some conceptual difficulties, as it shows a density rather than a probability. If a signal level ranges between 0 and 100%, then clearly it might be expected to spend some of its time around 50%.

However, the probability that it will be at exactly 50.000% is zero, because a single level value has zero extent. Hence the PDF at x is the probability that the signal variable is in the interval $(x, x+dx)$, where dx is the usual calculus infinitesimal.

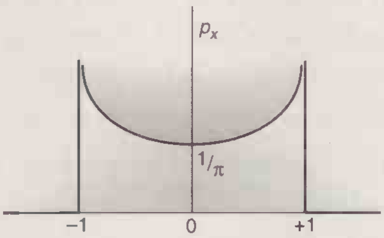

Fig. 2. Probability density function, or PDF, of a sinewave. Peaks at each end go towards infinity.

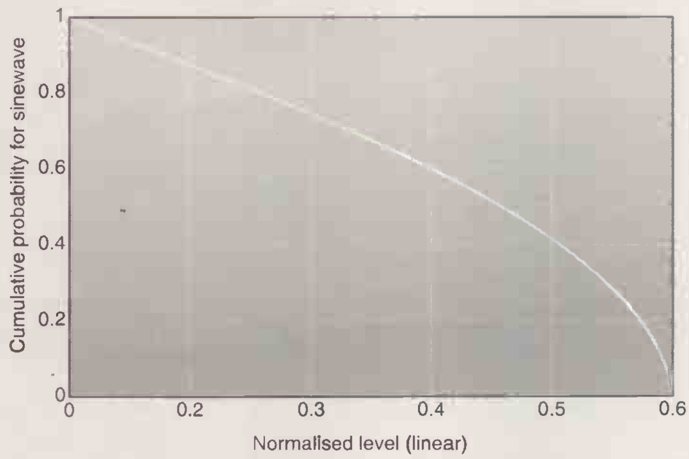

Fig. 3. Cumulative distribution function, CDF, of a sinewave. Drawn with measured data from the circuit of Fig. 4 as a reality check.

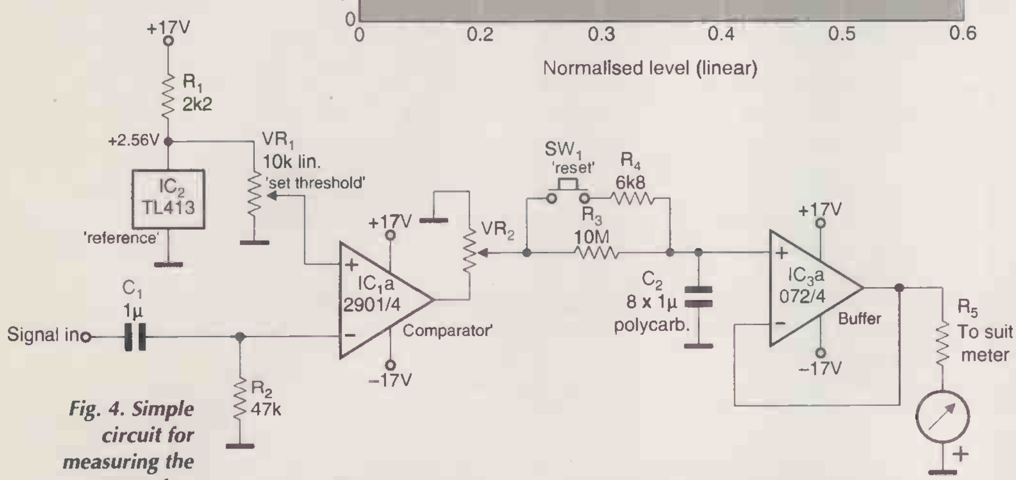

Fig. 4. Simple circuit for measuring the CDF of an audio signal.

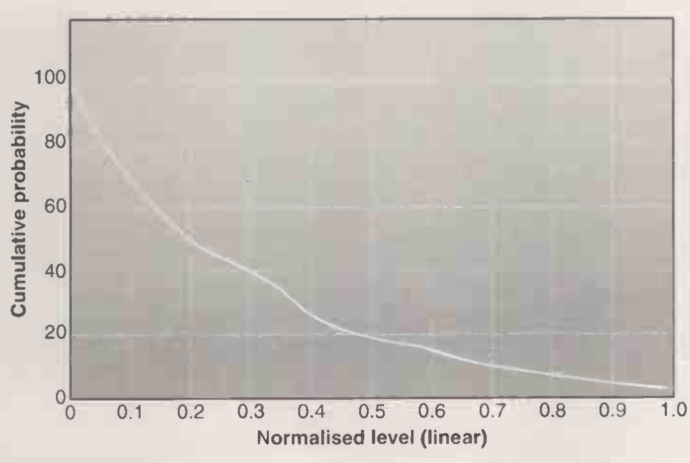

Fig. 5. The cumulative distribution function obtained from the PDF of Alannah Myles performing 'Black Velvet' by Fig. 4.

The cumulative distribution function

If the probability that the instantaneous voltage will be above – not at – a given level is plotted against that level, a cumulative distribution function, or CDF, results. This is important as it is easier to measure than the PDF.

If the variable is x, then the PDF is often called $P(x)$ and the CDF called $F(x)$. These are related by:

$$P(x) = \frac{d}{dx}F(x)$$

or,

$$F(x) = \int_0^x P(a)da$$

where a is a dummy variable needed to perform the integration. The integration starts at zero in this case because signal levels below zero do not occur.

Generating a CDF by integrating a given PDF is straightforward, but going the other way – determining the PDF from the CDF – can be troublesome as the differentiation accentuates noise on the data.

Some probability density functions

Figure 2 shows the calculated PDF of a sinewave. As with every PDF, the area under the curve is one, because the signal must be at some level all of the time.

However, the function blows up – i.e. heads off to infinity – at each end because the peaks of the wave are 'flat', and so the signal dwells there for infinitely longer than on the slopes where things are changing. These 'flat' bits are infinitely small in time extent though, and so the area under the curve is still unity. This shows you why PDFs are not always the easiest things to handle.

The CDF for a sinewave is shown in **Fig. 3**; the probability of exceeding the level on the axis falls slowly at first, but then accelerates to zero as the rounded peaks are reached.

Measuring probability density functions

But is all music Gaussian? I was not satisfied that this had been conclusively established from just two brief references.

I decided it was essential to make some attempt to determine musical PDFs. In essence this is simple. The first thing to decide is the length of time over which to examine the signal. For most contemporary music the obvious answer is 'one track', a complete composition lasting typically between three and eight minutes.

Very simple circuitry can be used to determine a CDF, and hence the PDF, though the process is protracted. A variable-threshold comparator is driven by the signal to be measured, and its output applied to a long-period averaging time-constant, **Fig. 4**.

A comparator, IC_{1a}, rather than an op-amp, is used to avoid inaccuracies due to slew-rate limiting. Reference IC_2 is an inexpensive 2.56V bandgap type, while VR_1 sets the comparator threshold. When the signal level is below this threshold, the comparator open-collector output is off, and the voltage seen by the averaging network is zero.

When the signal exceeds threshold, the comparator output is pulled low, so this point carries an irregular rectangular waveform while signal is applied. The average value of this is derived by R_3 and C_2, buffered by IC_{3a}, and drives a moving-coil meter through a suitable resistance R_5.

Switch SW_1 and R_4 enable a quick reset when no signal is present. A moving-coil meter allows much easier reading of a changing signal, though not to any great accuracy.

Potentiometer VR_2 sets the scale so that the meter deflects to full scale for a 100% reading. This is done with no input, so it is essential to check that the circuit offsets have put the comparator in the right state – i.e. output low; if not the inverting input will need to be pulled fractionally negative by a high-value biasing network.

The circuit only measures one polarity of the waveform, in this case the positive half, so signal symmetry is assumed. This is safe unless you plan to do a lot of work with solo instruments or single a cappella voices; the human vocal waveform is notably asymmetrical.

This minimal system is simple, but it only yields one data point at a time. Set the threshold level to say 50%, play the track – I'd pick a short one – and as it finishes the reading on the meter shows the percentage of time the signal exceeded the preset level.

Since twenty data points are required

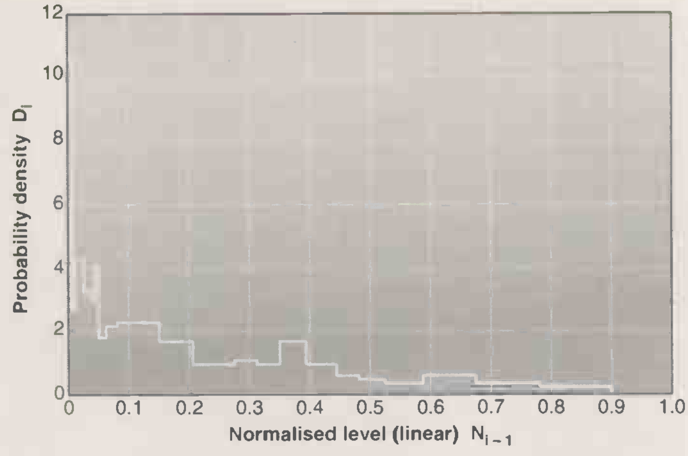

Fig. 6. Probability density function derived from Alannah Myles performing 'Black Velvet'.

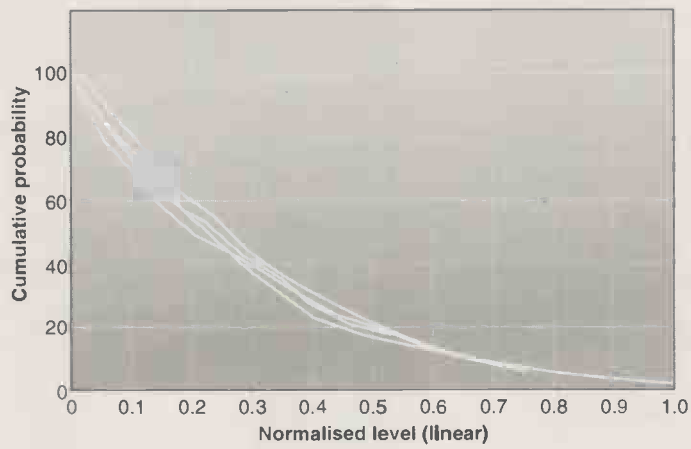

Fig. 7. The CDFs of 3 rock and 1 classical tracks, showing only small differences. The classical track (Bach) is marked with round data points.

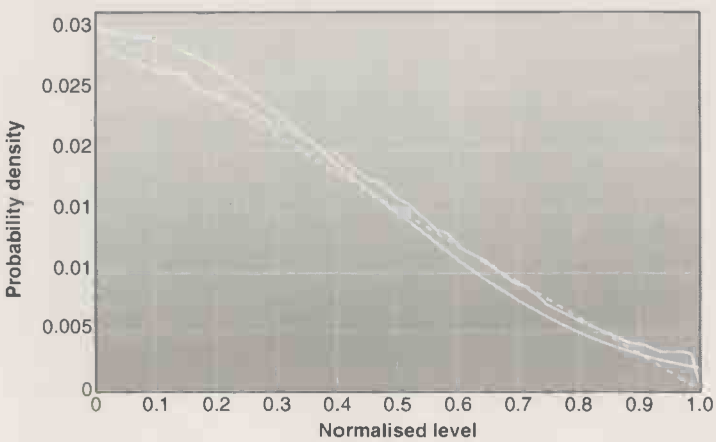

Fig. 8. The PDF of disco music, sorted into 65 amplitude bins by DSP. Also shown are a Gaussian distribution (smooth curve) and a triangular distribution (dotted line).

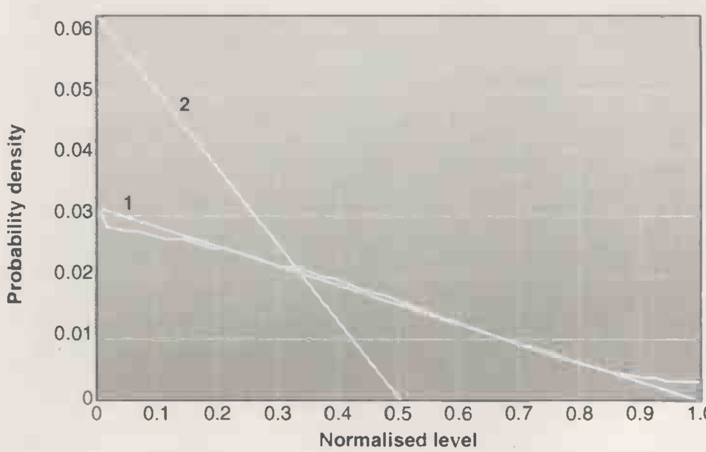

Fig. 9. The triangular PDF, and how level changes affect it. Line 1 is full volume, and Line 2 half volume.

for a good graph, this gets pretty tedious. The four comparators of IC_1 could give four points, if the time-constant section was also quadrupled, and some means of freezing the output voltages provided.

The CDF thus obtained for Alannah Myles' 'Black Velvet' is **Fig. 5**, and the PDF derived from it is **Fig. 6**. It comes complete with some rather implausible ups and downs produced by differentiating data that is accurate to ±1% at best.

I measured several rock tracks, and also short classical works by Albinoni and Bach. The results are surprisingly similar; see the composite CDF in **Fig. 7**. This is good news because we can use a single PDF to evaluate amplifiers faced with varying musical styles. However, I decided the method needed a reality check, by deriving the PDF in a completely different way.

Probability density functions via DSP

A digital signal processor offers the possibility of determining as many data points as you want on one playing of the music specimen. In this case a very simple 56001 program sorts the audio samples into 65 amplitude bins.

The result for 30 seconds of disco music is **Fig. 8**, which is somewhere between triangular and Gaussian, if the latter has appropriate variance. The important point is that the difference between them is very small, and either can be used. The triangular PDF simplifies the mathematics, but if like me you use Mathcad to do the work, it is easy to plug in whatever distribution seems appropriate.

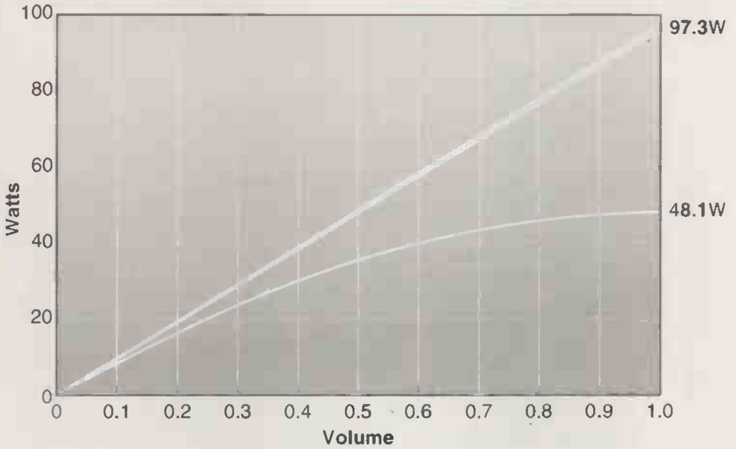

Fig. 10. Class-B complementary feedback pair power partition versus level. The Class-B IPPD has been combined with the triangular PDF. Device dissipation (lower area) now increases monotonically with volume.

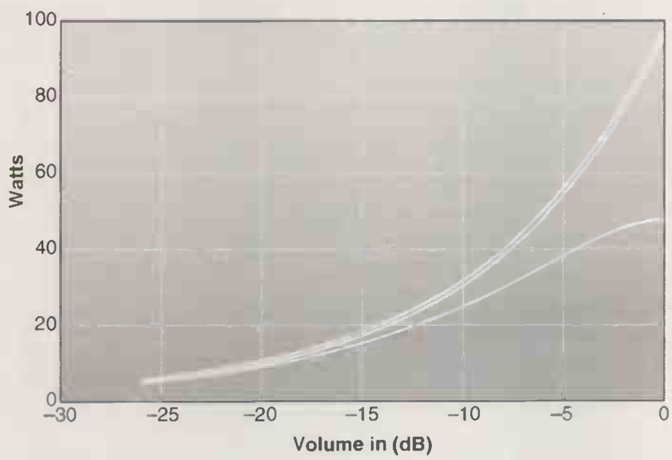

Fig. 11. Class-B complementary feedback pair plotted with volume on a more useful logarithmic (decibel) X-axis. The shape looks quite different from Fig. 10.

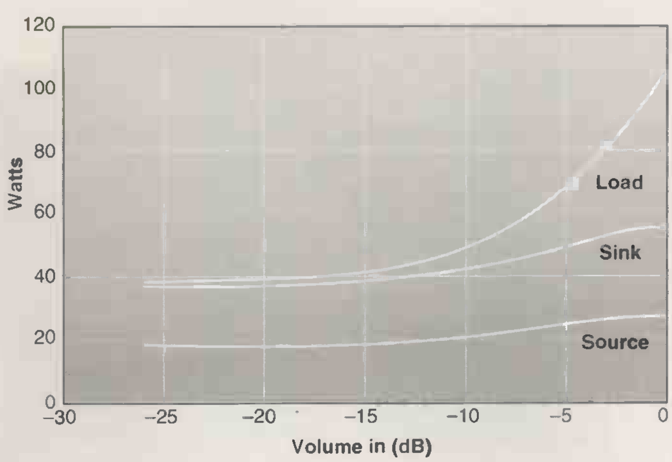

Fig. 12. Class-AB Power Partition Diagram, stage biased to give Class-A up to 5W. Averaged over whole cycle.

Deriving actual power

Having found the PDF, it is combined with the power partition diagram. In this case the IPPD is divided into twenty steps of voltage fraction, and each one multiplied by the probability the signal is in that region.

The summation of these products yields a single number – the average power dissipation in watts for a real signal that just reaches clipping for 1% of the time. An obvious extension of the idea is to plot the average power derived as above, against signal level on the X-axis. This gives an immediate insight into how amplifier power varies as the general signal level is reduced, as by turning down the volume control.

Figure 9 shows how level changes affect the PDF. Line 1 is maximum volume, just reaching full volume at the right. Line 2 is half volume, –6dB, and so hits the X-axis at 0.5; it is above Line 1 to the left as the probability of lower levels must be higher to maintain unity area under it.

This process continues as volume is reduced, until at zero volume the zero-level probability is 1 and all other levels have zero probability. Having generated twenty PDF functions, the powers that result for each one are plotted with the volume setting – not the output fraction – as the X-axis. The results for some common amplifier classes are as follows.

Class-B. The instantaneous power plot for Class-B complementary feedback pair combined with a triangular PDF of **Fig. 10** illustrates how the load and device power varies with volume setting. A signal with triangular PDF spends most of its time at low values, below 0.5 output fraction, and so there is no longer a dissipation maximum around half output. Device dissipation at bottom increases monotonically with volume. Load power increases with a square-law, which is a reassuring check on all these calculations.

Figure 11 is Fig. 10 replotted with a logarithmic X-axis, which is more applicable to human hearing. Domestic amplifiers are rarely operated on the edge of clipping; a realistic operating point is more like –15 or –10dB. The plot reveals that here the efficiency is low, with much more power dissipated in the devices than reaches the load.

Class-AB. A decibel plot for Class-AB, biased so Class-A operation is maintained up to 5W RMS output is shown in **Fig. 12**. Quiescent current is now 370mA, so there is greater quiescent dissipation at zero volume. There is also substantial conduction overlap, and so sink and source would be different if the plot only considered voltage excursions in one direction away from 0V. When positive and negative half-cycles are averaged, symmetry is achieved. The total device dissipation is unchanged but the boundary between the source and sink areas is half way, as in Fig. 12.

Class-A push-pull. I have stuck with the same ±50V rails for ease of comparison, and this yields a very powerful Class-A amplifier. The power drawn from the load is constant, and as output increases dissipation transfers from the output devices to the load, giving minimum amplifier heating at maximum output.

The result for sinewave drive is bad enough,[1] but **Fig 13** reveals that with real signals, almost all the energy supplied is wasted internally – even at maximum volume. Class-A has always been stigmatised as inefficient; this shows that under realistic conditions it is hopelessly inefficient, so much so that it grates on my sense of engineering aesthetics. At typical listening volumes of –15dB the efficiency barely reaches 1%.

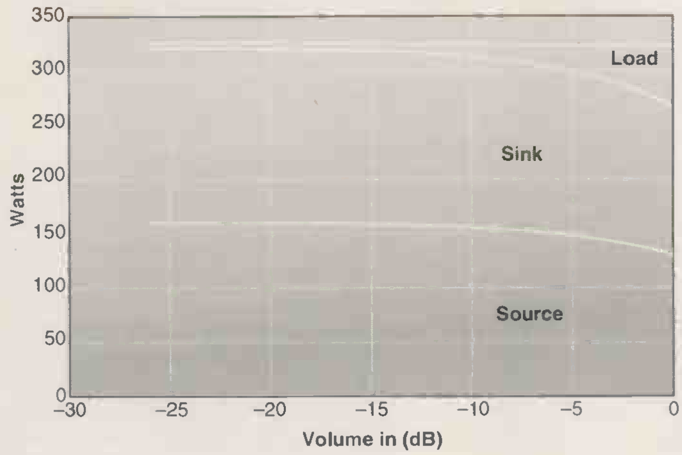

Fig. 13. Class-A push-pull, for 150W output. The internal dissipation completely dominates – even at maximum volume.

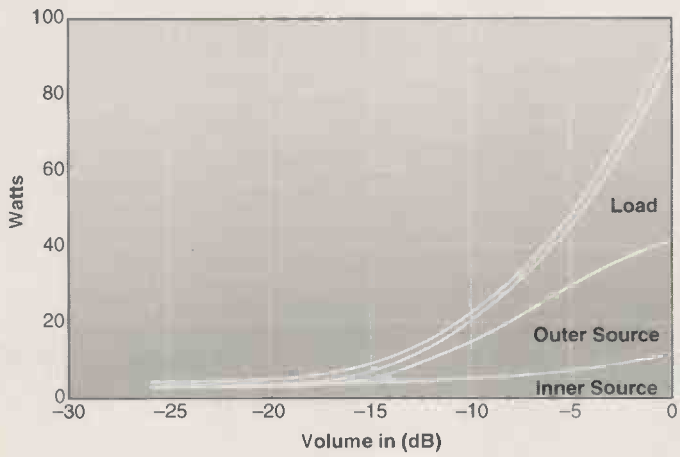

Fig. 14. Class-G-30%. Low rail voltage is 30% of the high rail. Rail-switching occurs at about –15dB relative to maximum output.

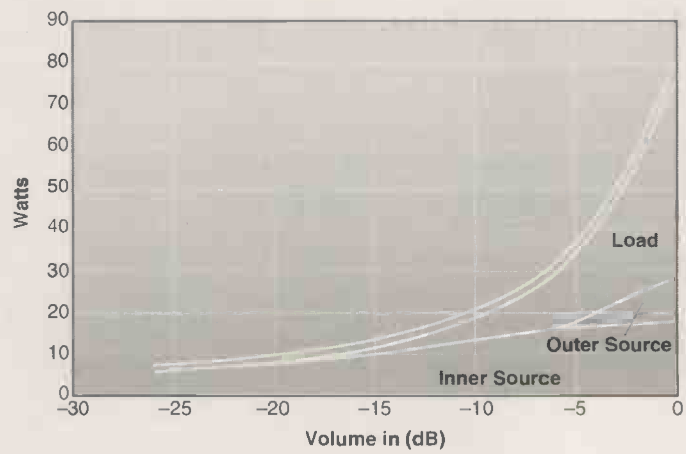

Fig. 15. Class-G-60% The low rail voltage is now 60% of the high rail. This reduces both dissipation and power consumed, compared with Fig. 14.

Class-G. This class of amplifiers was introduced by Hitachi in 1976 to reduce amplifier power dissipation by exploiting the high peak-mean ratio of music[5]. Class-G made little headway in the hi-fi market as the power saving does not outweigh the increased circuit complexity, but the rise of five-channel home theatre applications has caused a revival of interest in improved amplifier efficiency.

I recently explained Class-G in reference 6. At low outputs, power is drawn from low-voltage rails; for the relatively infrequent excursions into high power, higher rails are switched in.

In Fig. 14 the lower rails are ±15V, 30% of the higher ±50V rails; I call this Class-G-30%. The lower area is the power in the inner devices – i.e. those in all the time. The larger area just above is that in the outer devices, i.e. those only activated when running from the higher rails. This is zero below the rail-switching threshold at a volume of 0.2.

Total device dissipation is reduced from 48W in Class-B to 40W, which is not a good return for twice as many power transistors. This is because the lower rail voltage is poorly chosen for signals with a triangular PDF.

If the low rails are increased to ±30V this becomes Class-G-60% as in **Fig. 15**. Here the low-dissipation region now extends up to a voltage fraction of 0.5, but inner device dissipation is higher due to the increased lower rail voltages.

The overall result is that total device power is reduced from 48W in Class-B to 34W, which is a definite improvement. I am not suggesting that 60% is the optimum lower-rail voltage. The efficiency of Class-G amplifiers depends very much on signal statistics.

Reactive loads

The disadvantage of using instantaneous power is that it ignores signal and circuit history, and so cannot give meaningful information with reactive loads. The peak dissipations that these give rise to with real signals are difficult to simulate; it would be necessary to drive the circuit with stored music signals for many cycles; and that would only cover a few seconds of a CD or concert. The anomalous speaker currents examined in reference 7 show how significant history effects can be with some waveforms.

Table 1. Device dissipation, worst-case volume.

	Sinewave	PDF	Factor
Class-B CFP	64W	48W	0.75
Class-AB	64W	55W	0.78
Class-A, push-pull	324W	324W	——
Class-G-30%	43W	40W	0.93
Class-G-60%	56W	34W	0.61

Table 2. Power drawn, worst-case. Always maximum output.

	Sinewave	PDF	Factor
Class-B CFP	186W	97W	0.52
Class-AB	188W	105W	0.58
Class-A, push-pull	324W	324W	——
Class-G-30%	177W	93W	0.52
Class-G-60%	169W	81W	0.48

In summary

Tables 1 and 2 summarise how a triangular-PDF signal – rather than a sinewave – reduces average power dissipation, and the power drawn from the supply.

These economies are significant; the power amplifier market is highly competitive, and it is essential to exploit the cost savings in heat-sinks and power-supply components made possible by designing for real signals rather than sinewaves.

In particular, Class-G shows valuable economies in device dissipation and power-supply capacity, though to reduce dissipation, the lower supply voltage must be carefully chosen. This approach is unlikely to reduce the number of power devices required as real signals give no corresponding reduction in peak device power or peak device current. ■

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LETTERS

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Distorted or not?

I feel compelled to comment in Ian Hickman's latest distortion analyser in the August 1999 issue, p. 628.

The article places great emphasis on the notch filter design and little regarding the rest of the circuit. A few years ago, Mr Linsley-Hood also published a design for a complete distortion analyser, again placing emphasis on filter design.

I have no argument regarding both articles' filter design techniques. However, I must part when it comes to 'What comes after the notch filter' and hence the rectifier stage.

All the rectifiers published use two diodes, or four as in Mr Hood's design, which if studied closely, reveals that there will be a modulus hysteresis level of 1.2V due to the two diode drops.

In Hickman's design, Fig. 4 will have a hysteresis level of 0.6V. This means IC_{2B}'s output will go into slew rate limiting between +0.6 and –0.6V when driven by an output signal amplitude of the same or below this level.

If the input of IC_{2B} is grounded, you would expect the output to be 0V, but it will be +0.6V or –0.6V.

The above implications mean that any AC signal below the 1.2V differential threshold will be highly distorted – both designs are flawed.

I came across this problem when trying to design my own distortion analyser a few years ago. The solution is to use a true full-wave envelope detector or modulus detector, as found in AM receivers.

I also notice that Mr Hickman does not worry too much about op-amp drift compensation. I refer to IC_2's biasing resistors R_{10} and R_7 which are hopelessly imbalanced.

Meter M_1 is a current measuring device, hence 0-1mA, but it is driven by a voltage source as in Fig. 4, IC_{2D}. For high accuracy, it should be driven by a 0-1mA current source or via V-to-mA converter.

Darren Heywood
Buckley
Flintshire

Ian replies

I do not quite understand Mr Heywood's reservations concerning the meter circuit in my THD meter.

The use of diodes in a negative feedback loop to implement a linear scale voltmeter is well established, and applied in many commercial instruments. The only drawback is that the response is average-of-modulus, rather than true rms. This point was covered in detail in the article.

As Mr Heywood points out, between each half cycle, the op-amp output will traverse the dead space due to the diodes, in slew rate limit. But given an adequate slew rate, this is of no consequence. Tests show that a 20dB drop in input level causes the meter reading to fall from FSD to exactly one tenth of FSD at 200Hz.

Thanks to the excellent performance of the Burr-Brown *OPA4134* op-amp, this is duplicated exactly at input frequencies of 2kHz and 20kHz.

Due to the very low input bias current of the *OPA4134*, in the absence of any input, the output of IC_{2B} in the prototype sits at +250mV; a 1N4148 is not a complete open circuit below 0.6V.

Of course it could have been –250mV, or some other figure in that region, depending on component tolerances. But the exact figure is irrelevant: at inputs down to well under 10% of FSD, the action of the high loop gain takes charge.

The output of IC_{2B} is certainly highly distorted, but the input to R_{14} or R_{15} is either an exact copy of a half cycle of the input, or zero on the other half cycle.

Mr Heywood notes that R_7 and R_{10} are very different. At room temperature, input bias current of the OPA4134 could be as much as ±100pA, though it is typically 5pA. Thus the worst case contribution to the input offset voltage due to this unbalance is ±100μV.

The device's worst case input offset voltage V_{io} – room temperature again – is ±2mV and even the typical figure is ±0.5mV, so Mr Heywood need not concern himself with the imbalance.

Mr Heywood's point about the meter being a current operated device, driven from a voltage source, is a little obscure. The voltage ranges on an AVO meter model 8 are displayed on a moving coil meter, but no-one complains. In conjunction with 1kΩ resistor R_{18}, meter M_1 of my circuit simply forms a voltmeter with a sensitivity of 1000Ω/V.

A resistor of 1kΩ was adequate to mask the 0.4%/°C temperature coefficient of the particular meter used – with its 100Ω resistance – reducing that of the meter circuit as a whole to 0.04%.

Why digital tv is better

Recently we've had rather poor TV reception. A bolt of lighting took out the Bromsgrove transmitter a while ago. When it eventually came back, it was as though it was working on reduced power.

I waited for the signal to come back up to strength, but after several weeks it didn't. When I looked on Ceefax for transmitter information, I found that Bromsgrove wasn't listed as being on low power. When I approached the BBC about it, I was glibly told that I was experiencing "digital interference."

I was astounded by this. If digital tv signals spoil analogue TV, this is bound to make digital TV pictures *appear* better but without actually having to *be* better.

Another serious complaint I have with current TV is the inter-program sound – announcements and adverts. It is much, much louder than the programs. This is so annoying that we often have to mute the sound.

RF Price
Worcester

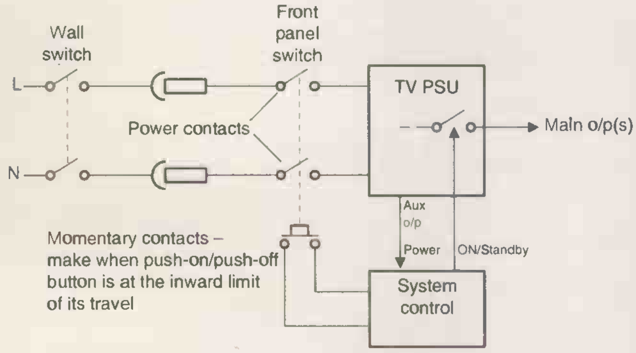
Standby switching for mains equipment

In Douglas self's excellent article on speaker protection circuits, he laments the lack of a mains switch suitable for mechanical detection of powering-off.

Most TV sets, if switched on at the wall with the front-panel switch already on, will power up in standby mode; if switched on at the front panel with the wall switch on, they power up fully.

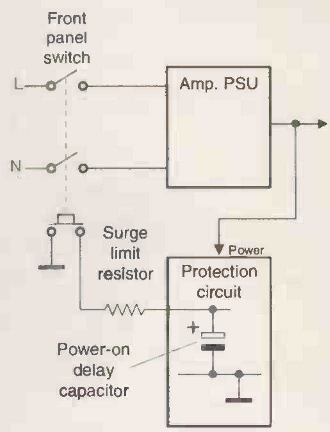
Since the panel switch and the wall switch are electrically indistinguishable, the panel switch is fitted with momentary contacts that make shortly after the power contacts close, and tell the system control to switch from standby to on. The diagram makes this clearer.

The momentary contacts also make shortly before the contacts open when switching off. This has no effect on the TV set, but could be useful in an amplifier to reset Mr Self's power-up timer and so drop out the protection relays. Due to the length of the power-up delay, there would be no significant effect at switch-on.



Note, however, that in a sound system composed of several bits of kit, each with its own power switch, it is much more convenient to plug all the power leads into a multi-way adaptor, leave all the individual power switches on and turn the whole lot on and off at the wall. This also allows the use of a time switch to make timed recordings or as an alarm clock. Electronic detection of power loss is therefore still necessary (and input protection maybe).

These switches are not generally available from the usual component suppliers, but spare-part suppliers such as CPC in Preston have a wide selection.



Should anyone want their TV set to power up fully when switched on at the wall, a permanent short across the momentary contacts usually does the trick.

Chris Bulman
Bedford

Picturing Schmitt's trigger

Bryan Hart takes an in-depth look at a sixty-year-old device that most designers today take for granted – the Schmitt trigger.

In digital system design the normally preferred shape of a waveform resembles that of **Fig. 1a)**. The waveform is 'clean'. When the digital signal v_S represents a '0', in the positive logic convention, it has a constant level V_{OL} in the acceptable '0' range. Similarly, a '1' is represented by a constant level V_{OH} in the acceptable '1' band.

Furthermore, transitions between levels are 'smooth'. Mathematically, the signal is said to increase monotonically from '0' to '1' and decrease monotonically from '1' to '0'.

However, as a result of crosstalk in interconnecting wires a practical waveform could resemble that shown in Fig. **1b)**. Noise 'spikes' p, q, are shown as occurring after the main transitions but they could appear during the transitions themselves as a result not only of crosstalk but also of ringing on interconnection paths.

Spikes p and q might jeopardise intended system operation, so how can they be eliminated? The use of a differential voltage comparator might seem to be appropriate, so consider **Fig. 2**, in which Fig. 1b) is repeated for convenience. The noise-contaminated waveform is applied to the non-inverting input of the comparator, C_O, in Fig. **2b)**: C_O is assumed to have ideal static and dynamic characteristics.

If the comparator reference level V_R, applied to the inverting input, is set at V_X then the output is as shown in Fig. **2c)**. Spike q is ignored but p causes two output pulses to appear instead of the single one required.

Similar conditions hold when $V_R = V_Y$, but in that case p is ignored not q. For the waveform illustrated, with $v_P < v_Q$, it is not possible to eliminate the effects of both p and q using a comparator as a straightforward clipper/limiter.

The problem can be solved using a scheme known as a Schmitt trigger[1]. Long before the advent of modern digital electronics, this name was given to a particular comparator circuit based on a pair of cathode-coupled thermionic tubes.

Originally, the Schmitt trigger was designed to produce abrupt changes in output voltage for slowly varying input signals. Nowadays the name is used to describe a generic circuit function, rather than a particular component assembly, though some form of comparator with a long-tailed pair input stage is commonly employed in bipolar transistor designs.

The purpose of this article is twofold: to explain some features of Schmitt-trigger operation which, though important in innovative design, are ignored in the general literature; to show how the Schmitt trigger can be designed to eliminate the effects of spikes p and q in Fig. 1b.

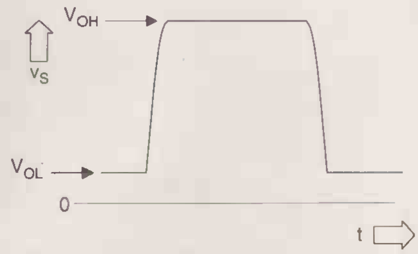
How the trigger works

Whatever the details of the internal circuitry, the Schmitt trigger may be regarded, from a system viewpoint, as a differential voltage comparator with positive feedback. **Figure 3** shows this for the case of inverting-mode operation; the non-inverting case is mentioned, briefly, later.

Potential differences V_S, ϵ, V_O are the d.c. values of the signal voltage, differential input voltage and output voltage respectively.

A three section piecewise-linear approximation to the static transfer characteristic, of C_O itself, is shown in **Fig. 4** and a d.c. equivalent circuit for each region of operation is shown in the box above it.

In Regions 1, 3 corresponding to saturation, the output can be modelled by the batteries V_{HL}, V_{LL}, respectively. In Region 2, the linear or active region, the output is modelled by a voltage-controlled voltage generator. For simplicity the



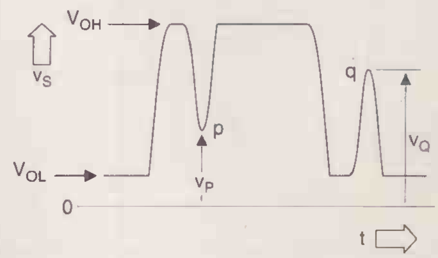
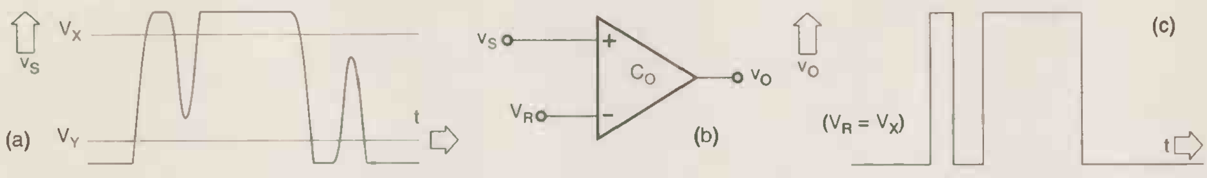


Fig. 1. Preferred shape of a binary signal, a), and possible shape, b), with noise spikes p, q.



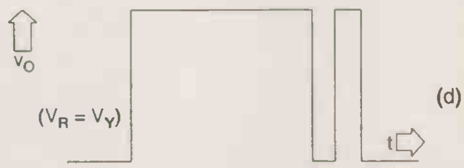


Fig. 2. Applying v_S, in (a), to ideal differential comparator C_O in (b) produces (c) when $V_R = V_X$ and (d) when $V_R = V_Y$.

input is assumed to impose no loading effect on the drive circuit. This assumption does not affect the general conclusions that are reached regarding system operation.

With the help of Fig. 3, it can be determined that,

$$V_S = \epsilon + \beta V_O \qquad (1)$$

where,

$$\beta = \frac{R_1}{R_1 + R_2} \qquad (2)$$

Rearranging eqn 1,

$$V_O = -\frac{\epsilon}{\beta} + \frac{V_S}{\beta} \qquad (3)$$

When plotted on the transfer characteristic, eqn 3 represents a straight line, with a slope $-1/\beta$, that passes through the axis point $\epsilon = V_S$. I will call this the operating line.

See what happens for various values of V_S. Line 'a', in Fig. 5, shows conditions for an arbitrarily large negative value, V_{S1}, of V_S. The line cuts the transfer characteristic at a single point P_1, where $V_O = V_{HL}$. Following a small momentary change in ϵ, owing to circuit noise, the operating point returns to P_1 so this is a stable position of equilibrium.

Line 'b', for V_{S2} ($>V_{S1}$), cuts the transfer characteristic at three points. The stable operating point is P_2, where V_O is still equal to V_{HL}. The other two intersections do not yet represent possible operating points because the comparator can exist in only one of its three regions at a given time. Until V_S is sufficiently positive for C_O to operate in Region 2, that is presently in Region 1.

For $V_S = V_{S3}$ ($>V_{S2}$) the operating line meets the transfer characteristic at two points P_3, P'_3. At P_3, line 'c' is tangential to the transfer characteristic at one edge of Region 2 and C_O behaves as a linear amplifier with positive feedback.

A momentary positive change in ϵ, once again due to circuit noise, now causes a regenerative switching action to occur as Region 2 is traversed. This action ceases when V_O reaches a limit and the circuit settles down into a stable state, at P'_3 in Region 3. What happens in the switching process will be discussed later.

The words used to describe V_{S3} are 'upper trip' (or, trigger)

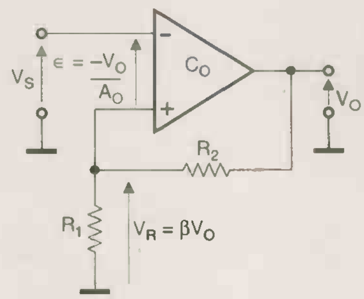


Fig. 3. Comparator configured as an inverting Schmitt trigger.

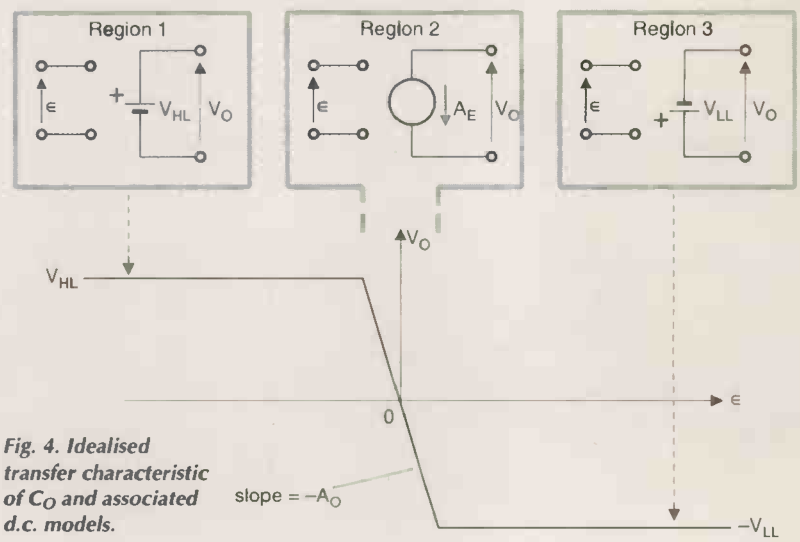


Fig. 4. Idealised transfer characteristic of C_O and associated d.c. models.

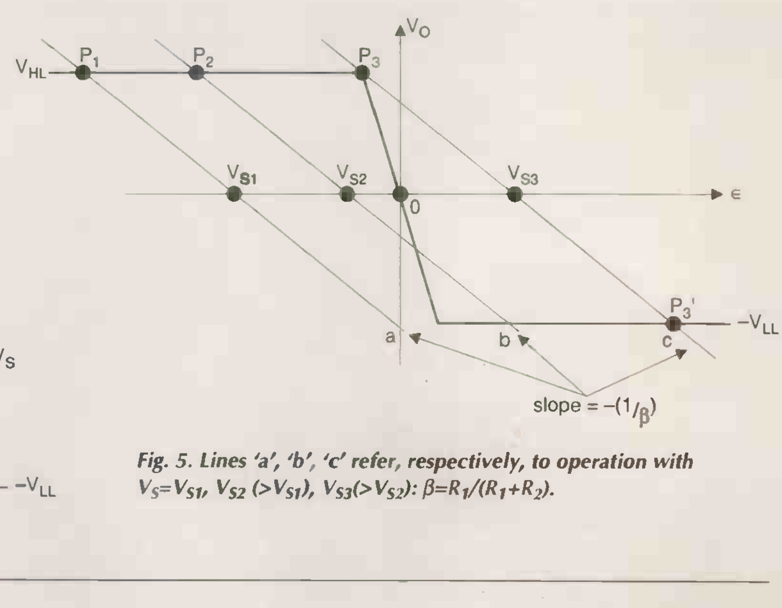


Fig. 5. Lines 'a', 'b', 'c' refer, respectively, to operation with $V_S = V_{S1}$, V_{S2} ($>V_{S1}$), V_{S3}($>V_{S2}$): $\beta = R_1/(R_1+R_2)$.

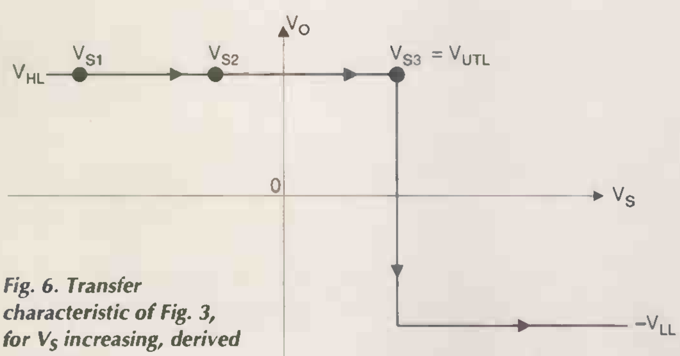


Fig. 6. Transfer characteristic of Fig. 3, for V_S increasing, derived from Fig. 5.

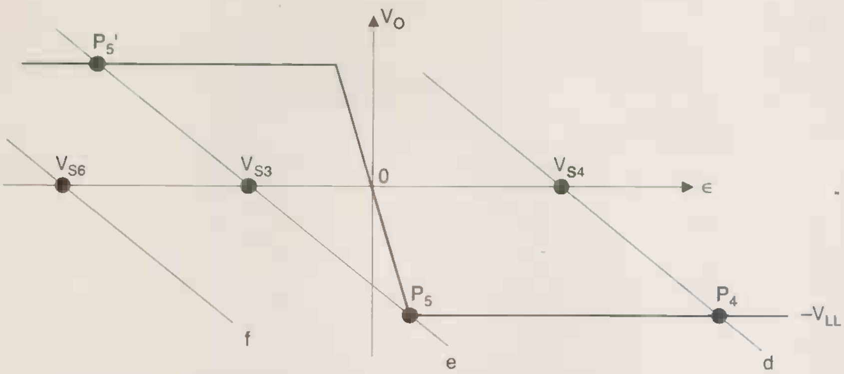


Fig. 7. Lines 'd', 'e', 'f', refer respectively to operation with $V_S=V_{S4}$, $V_{S5}(<V_{S4})$, $V_{S6}(<V_{S5})$.

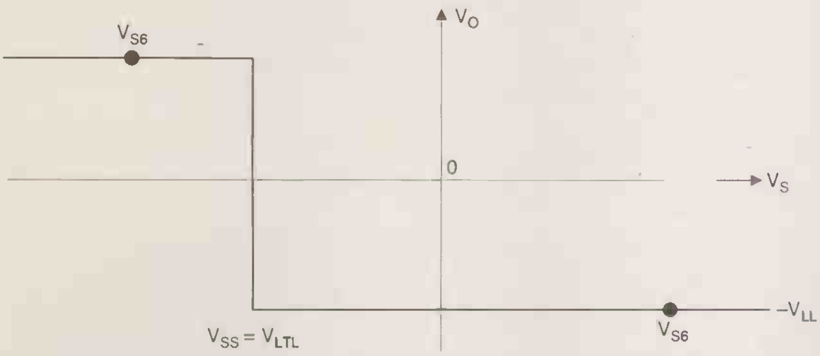


Fig. 8. Transfer characteristic of Fig. 3 for V_S decreasing, derived from Fig. 7.

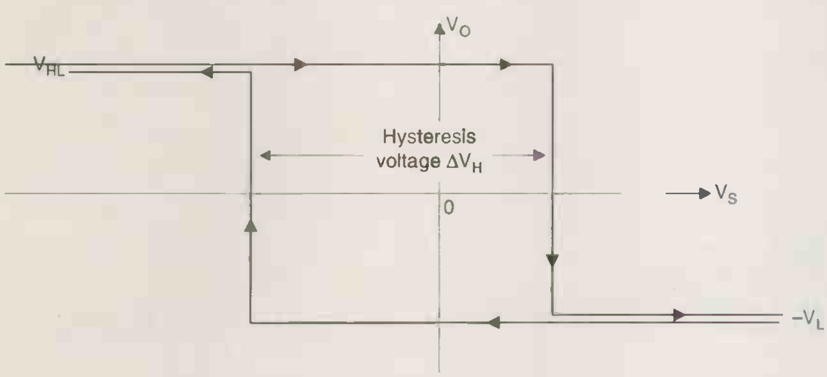


Fig. 9. The hysteresis characteristic is a composite plot of Figs 6, 8: the horizontal sections for $V_S<V_{LTL}$ and $V_S>V_{UTL}$ are shown slightly separated for clarity.

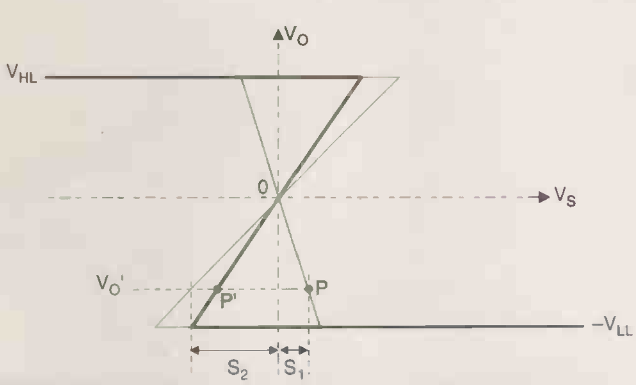


Fig. 10. Static transfer characteristic for Fig. 3 is shown bold. Line sections S_1, S_2 refer to terms in eqn 8.

level', and the letter subscripts UTL are used: thus, $V_{S3}=V_{UTL}$.

Substituting,

$$\in=-\frac{V_{HL}}{\beta}$$

in eqn 3 and rearranging gives,

$$V_{S3}=V_{UTL}=-\frac{V_{HL}}{A_O}+\left(\beta V_{HL}\right) \quad (4)$$

For the normal case $\beta>>(1/A_O)$,

$$V_{UTL}\approx\beta V_{HL} \quad (5)$$

Derived from Fig. 5, **Figure 6** shows an apparent static plot of V_O *versus* V_S. The arrow direction indicates increasing V_S, and, if the input voltage is changing, increasing time, t.

In **Fig. 7**, which should be compared with Fig. 5, lines 'd', 'e' and 'f' show what happens when V_S decreases from a value V_{S4} ($>V_{S3}$). The output remains at $-V_{LL}$ till $V_S=V_{S5}$; then, 'e' is tangential to the transfer characteristic at point P_5 on the other edge of Region 2.

A tiny change in $\in$ 1 due to circuit noise, is sufficient to initiate a regenerative switching action which ends when the point P'_5 in Region 1 is reached. **Figure 8** is derived from Fig. 7 in the same way that Fig. 6 is derived from Fig. 5. The arrow direction indicates successively decreasing values of V_S. If the input voltage is continually changing, this also corresponds to increasing t.

Voltage V_{S5} is designated 'lower trip (or trigger) level' and from reasoning similar to that which produced eqn 5,

$$V_{S5}=V_{LTL}\approx-\beta V_{LL} \quad (6)$$

Figure 9, a composite plot of Fig. 6 and Fig. 8, is the apparent static transfer characteristic of the system. The horizontal line sections for $V_S<V_{LTL}$ and $V_S>V_{UTL}$ should be shown coincident, but one is slightly displaced with respect to the other on this particular diagram to clarify the confusion that can arise when oppositely directed arrows are shown adjacent on the same line section.

The system exhibits 'memory', characterised by a hysteresis, or deadband, voltage ΔV_H,

$$\Delta V_H=\left(V_{UTL}-V_{LTL}\right)\approx\beta\left(V_{HL}+V_{LL}\right) \quad (7)$$

Instead of the graphical procedure that led to Fig. 9, you can obtain a plot of V_O versus V_S as follows.

At any point $V_S=V'_S$, $V_O=V'_O$ in Region 2, where,

$$\in=-\frac{V'_O}{A_O}$$

Equation 1 can be rewritten as,

$$V'_S=-\frac{V'_O}{A_O}+\left(\beta V'_O\right) \quad (8)$$

Figure 10 shows a plot of the transfer characteristic, on which is constructed a line, with slope $1/\beta$, which passes through the origin. This line characterises the effect of feedback. At $V_O=V'_O$, V'_S is obtained by the algebraic addition of the horizontal line sections S_1 and S_2 that represent the two terms on the right-hand side of Fig. 8. Thus, point P′ on the overall system characteristic corresponds to P on the transfer characteristic and the locus of points such as P′ is the Z-shaped characteristic shown bold.

The central section is a straight line of slope A′.

$$A'=\frac{-A_O}{1-A_O\beta} \quad (9)$$

This equation follows from a rearrangement of eqn 8, or from the standard relationship for an amplifier with feedback[2]: for $\beta>>(1/A_O)$, $A'\approx1/\beta$. It now seems that two different graphs describe the voltage transfer relationship for the

Schmitt trigger. Which one is correct?

Figure 10 relates to a d.c. model, only, of the system, i.e., the existence of energy storage elements is ignored. Hence, the effect of the regenerative action at $V_S=V_{UTL}$ and $V_S=V_{LTL}$ is not evident.

Figure 9, with the horizontal sections lying outside the hysteresis loop shown coincident, indicates the actual form of the trace observed in a practical sweep test designed to show V_O(Y) *versus* V_S(X), using a pen recorder or oscilloscope.

Incidentally, following on from Fig. 10, a three-dimensional plot of V_O (Y-axis) *versus* V_S (X) and β (Z) produces a folded surface similar to that encountered in elementary Chaos theory.

Some analogues in other areas of engineering science offer useful insight into the phenomenon of hysteresis. These are touched on next.

Analogues of hysteresis

The *BH* curve of a ferromagnetic material provides a familiar example of hysteresis. In that case it can be attributed to the 'remembered' angular orientation of domain magnetic moments.

An equivalent of hysteresis is the 'backlash' encountered in mechanical transmission systems, particularly those involving worn gear wheels, when the input drive is reversed. However, a more illuminating mechanical analogue is a see-saw with a sliding load.

Consider **Fig. 11**: this is a plan view of a light, rigid, beam pivoted in the middle. A smooth metal rod is attached to the side of the beam, like a curtain rail fixed to the wall above a window. A circular metal weight, *m*, similar to those used by weight-lifters, can slide freely along the rod between the end-stops situated at a distance L_1 to the left of the pivot and L_2 to the right.

Figure 12 is a side view of this see-saw scheme. A person, *n*-times heavier than weight *m*, walks from one end, G, towards the pivot, J, which is a height *h* above ground level. At this time the other end, K, is 2*h* above ground level.

When the person reaches a point L_1/n to the right of J, the beam starts to tip down on that side. This follows from the Principle of Moments. As it does so, *m* slides towards J, further aiding the motion of K towards the ground.

As the person walks back, **Fig. 13**, K does not move upward until he reaches a point L_2/n to the left of J. A 'transfer characteristic' for the mechanical operation is shown in **Fig. 14**: in this particular drawing, n=2.

Switching and stability

Referring back to Figs 5, 7 it is necessary to use a dynamic model of C_O to understand Schmitt-trigger behaviour on reaching points P_3, P_5. The simplest model, but one which highlights the main features of operation, is that shown within the broken-line triangular outline in **Fig. 15**.

The use of lower case letters indicates that voltage *changes* are being considered. Components *R* and *C* define a single-pole frequency response in Region 2. Thus,

$$A' = \frac{-A_o}{1 + j\dfrac{\omega}{\omega_c}} \tag{10}$$

or,

$$A' = \frac{-A_o}{1 + j\omega\tau_c} \tag{11}$$

where,

$$\omega_c = \frac{1}{\tau_c} = \frac{1}{CR} \tag{12}$$

The input is shown connected to signal-earth because the switching process is governed by the parameters of the feed-

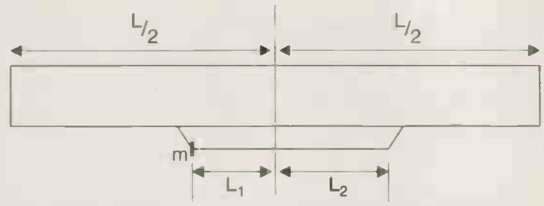


Fig. 11. Plan view of a see-saw, with weight m at an end-stop on a side rail.

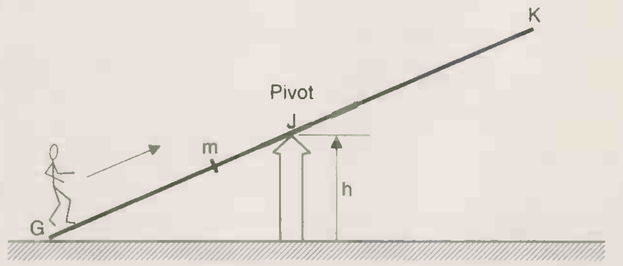


Fig. 12 . Side view of see-saw, with person starting to walk from G to K.

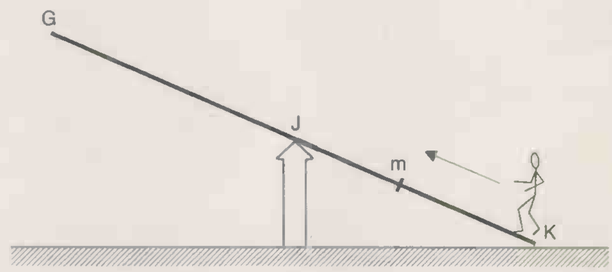


Fig. 13. The person starts to walk back from K to G.

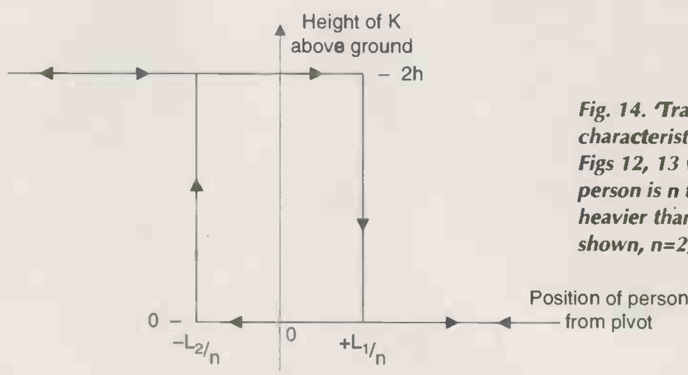


Fig. 14. 'Transfer characteristic' for Figs 12, 13 when person is n times heavier than m. (As shown, n=2).

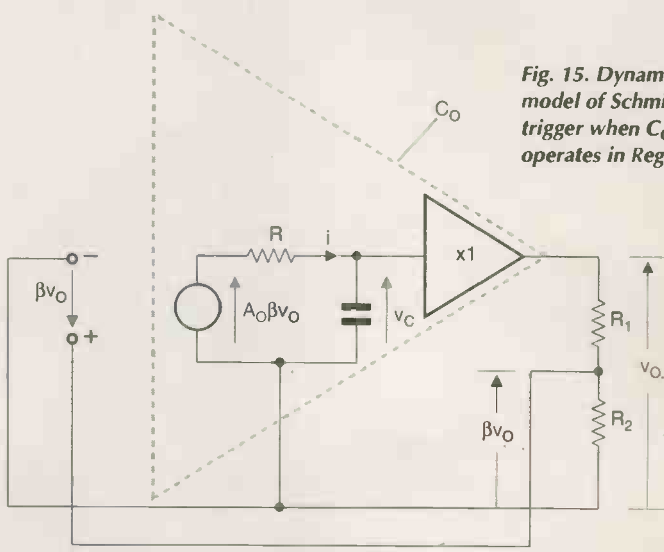


Fig. 15. Dynamic model of Schmitt trigger when C_O operates in Region 2.

back loop, not the input signal.

The charging current, i, for C is given by,

$$i = C\frac{dv_C}{dt} = \left(A_o\beta - 1\right)\frac{v_O}{r} \qquad (13)$$

or,

$$\frac{dv_O}{dt} = \left(A_o\beta - 1\right)\frac{v_O}{\tau_C} \qquad (14)$$

Equation 14 follows from 13 by using eqn 12 and the fact that v_O=v_C.

A general solution of eqn 14 is of the form,

$$v_O \propto \exp\left(A_o\beta - 1\right)\frac{t}{\tau_C} \qquad (15)$$

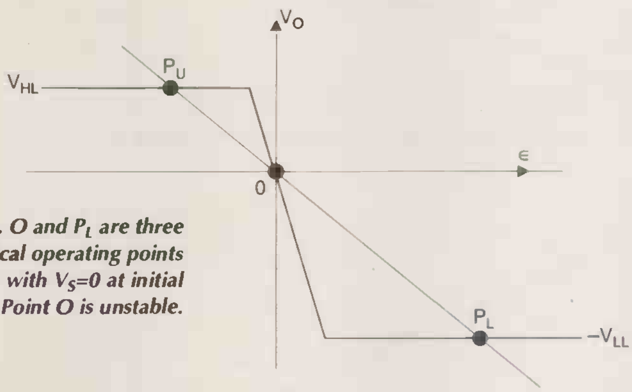


Fig. 16. P_U, O and P_L are three theoretical operating points for Fig. 3 with V_S=0 at initial switch-on. Point O is unstable.

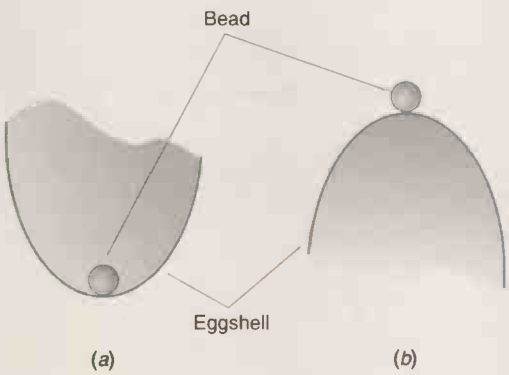


Fig. 17. (a) and (b) are mechanical analogues for stable and unstable equilibrium, respectively.

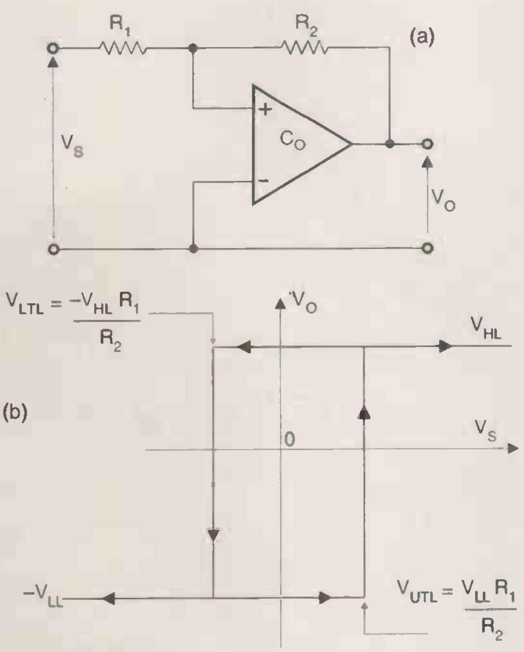


Fig. 18 . A non-inverting Schmitt trigger, (a), its transfer characteristic, (b), and its preferred, unambiguous, symbol, (c).

Provided the loop-gain factor $A_O\beta$ exceeds unity, as is the case here, this equation describes an exponential growth once Region 2 is reached. In fact, eqn 15 is characteristic of the switch-over process not only in bistables but also monostables and astables.

Switch-over time t_S is proportional to the time constant $\tau_C/(A_O\beta-1)$, but $\Delta V_H \propto \beta$ so t_S and ΔV_H are inversely related. It is *not* possible to have, simultaneously, zero hysteresis and regenerative switching – a fact overlooked by some authors.

The condition $A_O\beta >> 1$ implies $A_O >> 1/\beta$. A graphical interpretation of this is that the fastest switching is obtained with the greatest angle between the slope of the operating line and the slope of the transfer characteristic in Region 2.

For the circuit of Fig. 3, there is a remaining problem to consider. What happens if V_S=0 when the circuit is initially switched on?

Direct-current conditions are satisfied at point O in Fig. 16. However, this is not stable. Referring to eqn 14, if v_O>0 then (dv_O/dt)>0 and operation moves to P_U: if, however, v_O<0, then (dv_O/dt)<0 and operation moves to P_L. So, following switch-on, V_O=V_{HL} or V_O=$-V_{LL}$. It is impossible to say which it will be in advance. This is true at switch-on for any V_S lying between V_{LTL} and V_{UTL}.

In practice, eqn 15 is only approximately true because there is a non-linear relationship between V_O and ∈ in Region 2, which leads to daunting mathematics.

The differing conditions of stability at points P_1, P_3, in Fig. 5, are well-illustrated by the mechanical analogues in Fig. 17. In Fig. 17a), corresponding to P_1, a small spherical bead rests inside the bottom of a half-eggshell. It is a stable position of equilibrium because the bead returns to its initial position following a small disturbance.

Figure 17b) corresponds to operation at P_3. The bead cannot be stable on top of the inverted eggshell because, even if it was possible to balance it there initially, it would fall down the side after a small disturbance.

Design considerations

The operation of a Schmitt trigger in the non-inverting mode, Fig. 18a), is similar to that described for the inverting mode. Its graphical analysis resembles that associated with Fig. 5.

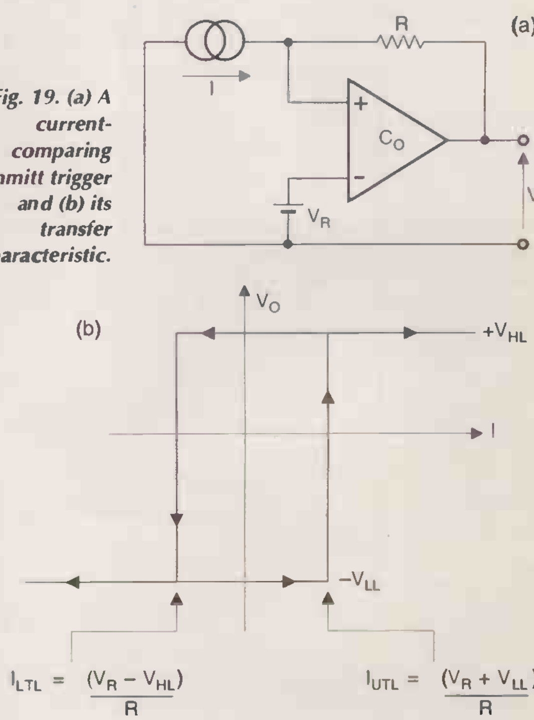


Fig. 19. (a) A current-comparing Schmitt trigger and (b) its transfer characteristic.

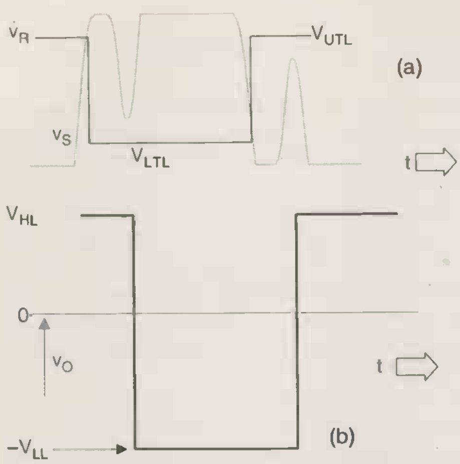


Fig. 20. Diagram (a) shows required location of V_{UTL} and V_{LTL} on comparator switched-reference level v_R to eliminate spikes p, q of Fig. 1b) while (b) shows the spike-free output waveform.

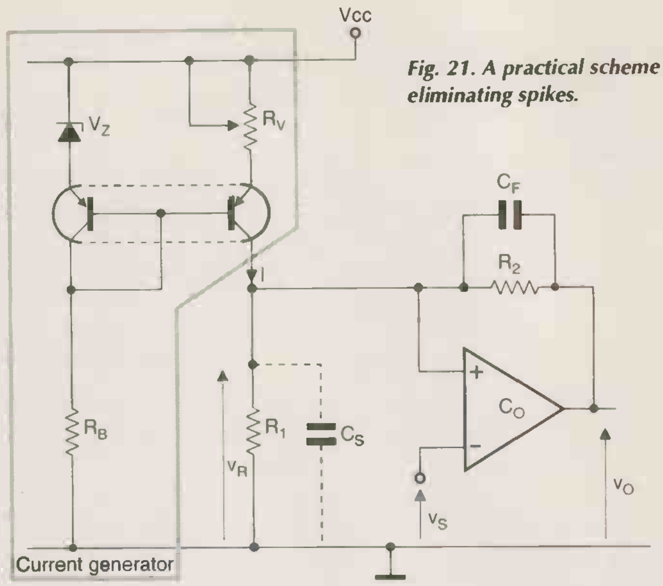


Fig. 21. A practical scheme for eliminating spikes.

For a given V_S, the operating line, still has a slope $-1/\beta$ but it passes through a point $\in = -V_S(R_1+R_2)/R_2$ on the horizontal axis rather than $\in = V_S$.

With increasing V_S, the line moves from right to left and *vice versa*. Consequently, $V_{UTL}=V_{LL}(R_1/R_2)$ and $V_{LTL}=-V_{HL}(R_1/R_2)$ and the hysteresis characteristic is shown in Fig. **18b)**. An unambiguous block schematic representation[3] is shown in Fig. **18c)**. The hysteresis symbol in the box is reversed for inverting operation.

The non-inverting scheme does not provide the same degree of isolation from the driving source as the inverting configuration. This is because the output resistance, R_S, of the source must be included with R_1 for trip level calculations. When R_S is very large or poorly defined, a better procedure is to design for inverting operation and follow with an inverting buffer stage.

Applying a fixed reference potential to the inverting input of Fig. 18a) has the effect of shifting the hysteresis loop bodily along the horizontal axis as is evident with the current-comparing trigger shown in **Fig. 19**.

Returning now to the problem of logic spike elimination mentioned at the beginning of this article, the effect of p, q in Fig. 1 can be avoided if the waveform is applied to an inverting trigger circuit with trip levels located as shown in **Fig. 20a)**: the output is then as shown in Fig. **20b)**.

It might be possible to achieve this using a standard monolithic Schmitt trigger such as the TTL 7413, which has V_{UTL} fixed at 1.9V and V_{LTL} at 0.9V. When a standard unit is not applicable a suitable scheme[4], a development of Fig. 3, is shown in **Fig. 21** in which v_S is the waveform of Fig. 1b).

Resistors R_1, R_2 are chosen so that,

$$V_{UTL}-V_{LTL}=\Delta V_H>(v_Q-v_P).$$

Current I is approximately V_Z/R_V. It is supplied by the circuit within the contour shown and provides a facility for shifting the hysteresis loop along the axis by a voltage $I(R_1//R_2)=IR_X$ without changing ΔV_H.

The design equations and design procedure are as follows.

$$V_{OH}>V_{UTL}>v_Q \qquad (16)$$

or,

$$V_{OH}>(IR_X+\beta V_{HL})>v_Q \qquad (17)$$

and,

$$v_P>V_{LTL}>V_{OL} \qquad (18)$$

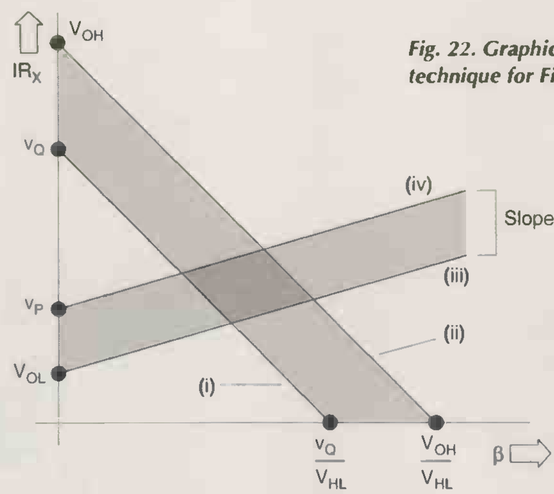


Fig. 22. Graphical design technique for Fig. 21.

i.e.,

$$v_P>(IR_X-(V_{LL})>V_{OL} \qquad (19)$$

On a plot of IR_X versus β, **Fig. 22**, condition (17) is satisfied if the operating point lies between the parallel lines (i), (ii) and condition (19) is satisfied for operation between parallel lines (iii), (iv).

The cross-hatched area thus defines parameter choices for satisfactory operation. To allow for tolerances in R_1, R_2, I, etc., it is advisable to operate at a point in the centre of the permitted area. If this area encompasses the β axis it is possible to design for I=0.

This procedure only works precisely if C_O has a low output resistance at both of its output levels, as is the case with the long-established 710 comparator. The 311 requires an output pull-up resistor but, provided this is less than one tenth the resistance of R_2, the procedure given is still a useful starting point.

One further point; the speed-up capacitor C_F, in Fig. 21, is chosen to make the feedback network a compensated potentiometer so $C_FR_2=C_SR_I$, capacitance C_S being the total capacitance appearing across R_1.

Reversing the roles of the current generator and the feedback network in Fig. 21 gives the circuit variation in **Fig. 23**. The design equations in this case are:

$$V_{UTL}=\beta V_{CC}+IR_X \qquad (20)$$

$$V_{LTL}=\beta V_{CC} \qquad (21)$$

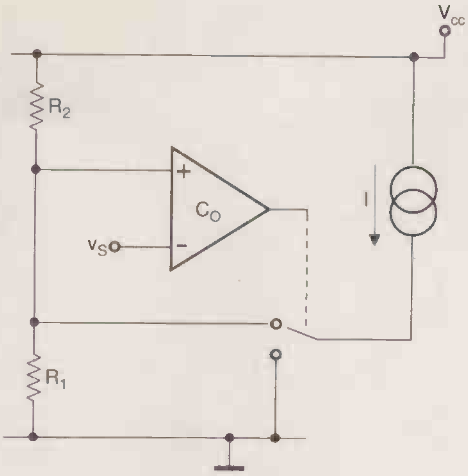


Fig. 23. A circuit variation of the technique of Fig. 21.

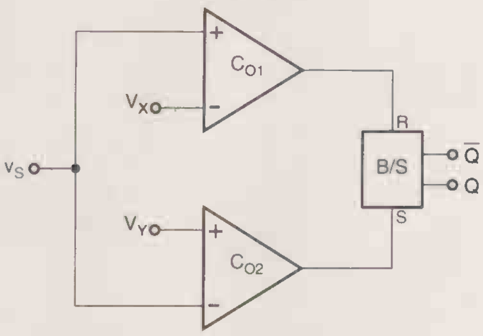


Fig. 24 . Alternative Schmitt trigger configuration for spike elimination: V_X, V_Y are the voltage levels shown in Fig. 2a).

A graphical procedure, similar to that of Fig. 22, is applicable.

The design problems associated with Fig. **3** are eased and the resulting circuit is made more versatile if its two functions, trip-level definition and bistable-action, are performed separately as in the scheme of **Fig. 24**.

The common input signal for the comparators C_{O1}, C_{O2} is the waveform of Fig. 1b). The comparison potentials applied to them are, respectively, V_X, V_Y shown in Fig. 2a).

When $v_S < V_Y$ the bistable is set and remains set till $v_S > V_X$, when it is reset. This scheme allows free choice of V_{LTL}, V_{UTL} and provides both polarities of output. It is at the heart of the popular 555 timer IC.

When the device is used as an astable, the hysteresis voltage serves to define the voltage swing across a timing capacitor connected to the common input to the comparators. ■

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1. Schmitt O.H., 'A thermionic trigger', Journal of Scientific Instruments, 15, pp. 24-26 (1938).
2. Hart B.L., 'Introduction to Analogue Electronics', Arnold, Chapter 8 (1997).
3. IEE, 'Units and Symbols for Electrical and Electronic Engineering', IEE Guide (1997).
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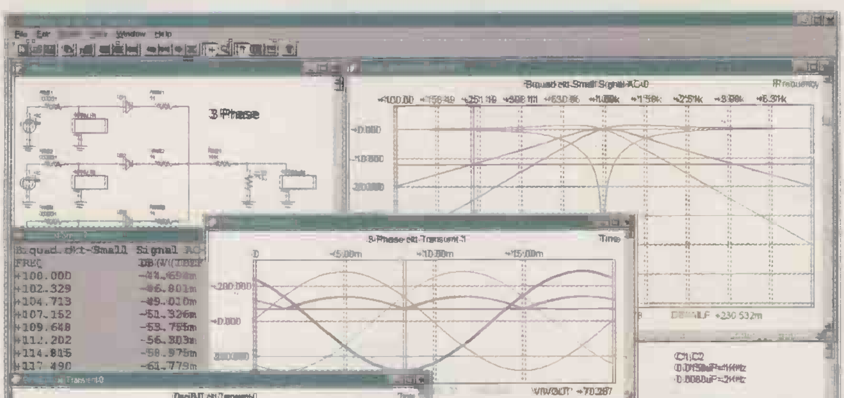


Hands-on Internet

The 'perfect' transistor

Cyril Bateman looks at the nearest thing to a perfect transistor. Its output swings negative for negative base signals and vice-versa for positive ones. It has a 700MHz bandwidth, 7.7nV/√Hz noise and low distortion – even at 10MHz.

In the October issue, I discussed some circuit functions using transconductance amplifiers. A transconductance amplifier's gain can be set by altering its transconductance and load resistance. It can also provide a differential input instrumentation amplifier, without needing the carefully matched resistor networks needed for the conventional three op-amp circuit.

I chose to investigate this particular attribute when searching for a circuit I could use to design a balanced input probe for my oscilloscope. Many commercial instrumentation amplifiers provide excellent performance at lower frequencies, but I really hoped not to restrict my oscilloscope's 100MHz capability.

Prior to searching Internet, I already had one particular integrated circuit in mind – the AD830 from Analog Devices[1].

My Internet searches revealed several interesting transconductance amplifier designs and applications, some of these were described in the October issue.

This time I will concentrate mainly on one particular versatile integrated circuit, which comprises an unusual wideband transconductance amplifier and an open-loop, wideband, unity gain buffer.

Burr-Brown[4] produces the OPA660 integrated circuit. It has been named the 'diamond transistor' because of the complementary symmetry of the transistors used in its design.

The OPA660 provides a unity-gain, open-loop voltage buffer amplifier and a transconductance amplifier in an eight-pin package. This buffer amplifier provides low differential gain/phase errors at video frequencies, a 700MHz bandwidth and 3000V/µs slew rate.

An ideal transistor?

The operational transconductance amplifier, or OTA, section can be viewed as a quasi-ideal transistor. Like a transistor it has three terminals, a high impedance input (base), a low impedance input/output (emitter) and a current output (collector).

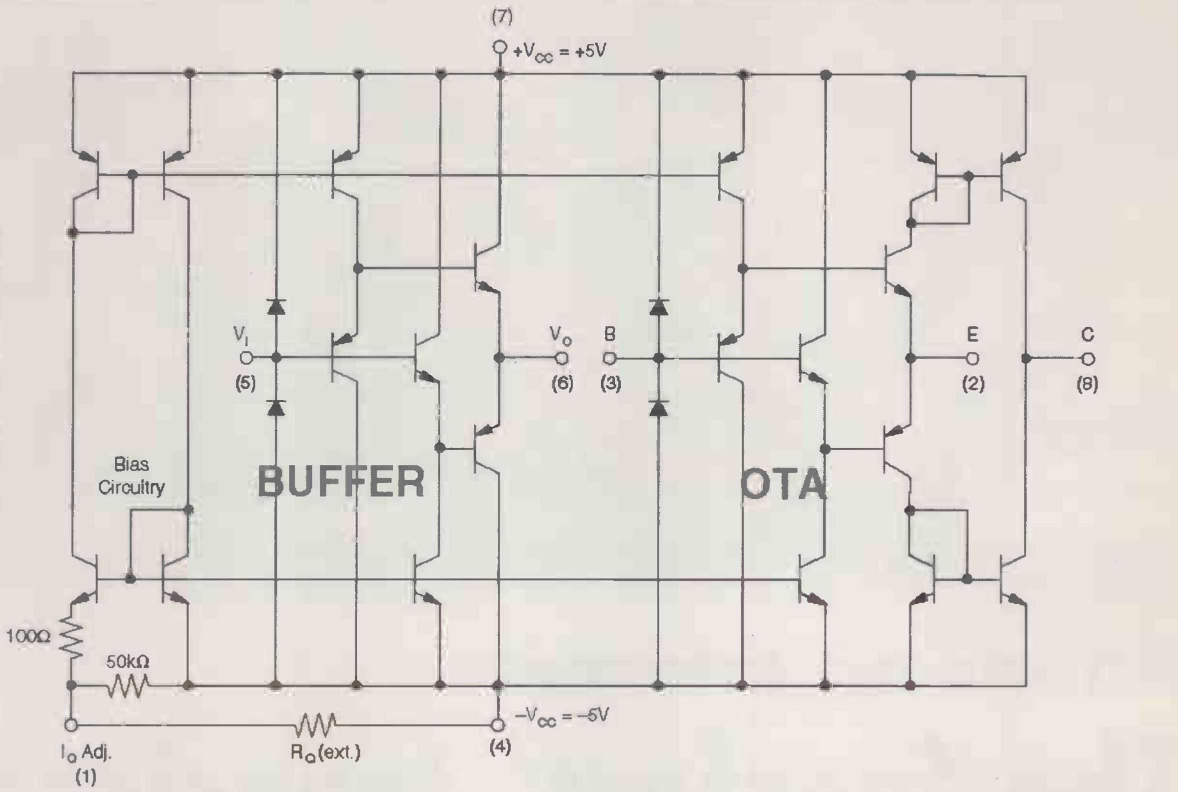
This OTA however differs from a transistor in that it is self biased and bipolar in that it exhibits a combined p-n-p/n-p-n characteristic. The output current is zero for zero differential input voltage. Alternating inputs centred on zero volts produce a bipolar output current also centred on zero volts.

This OTA can provide a consistent transconductance of 106mA/V at frequencies to 100MHz, reducing to some 10mA/V at 250MHz. The actual transconductance can be adjusted via an external resistor, allowing bandwidth, quiescent current and gain trade-offs to be optimised.

The three OTA terminals are labelled B, E and C to draw attention to the device's similarity to an ideal transistor.

With a positive base-to-emitter input voltage, current flows out of the collector terminal. Current then flows into the

Fig. 1. Simplified schematic drawing of Burr-Brown's OPA660 'Diamond Transistor' integrated circuit. This OTA is self biasing and with bipolar input signals, it provides a bipolar output.



Bugs

I reported on the Happy99.exe virus, which can be received via e-mail, in the August 99 issue. Perhaps like me, not having previously been troubled by e-mail viruses, you have wondered whether they exist or are simply alarmist propaganda.

Well on 24 August, I received an unwanted e-mail from <remember 132550@usa.net> which was complete with the Happy99.exe attachment.

Since I use only OS/2 and the OS/2 version of Netscape 2.02 for all my Internet accesses, this attachment could not automatically run or be accidentally opened. Needless to say, I deleted it completely.

Other operating systems are more vulnerable. This week two new viruses have been reported. 'Toadie' sometimes called 'Termite' is now common in the e-mail freeware communities. It has been classified by Network Associates as of medium damage level risk. If activated it can infect as many as 100 executable files, in both DOS and Windows systems.

The virus has four variants with code sizes from 6585 bytes to 7585 bytes. It will run in DOS and attach itself to the executable files of 16 or 32 bit applications, including all Windows operating system executables.

Any modification to an infected file's time/date stamp, and the file will no longer run. Data files are not damaged, but application programs on infected machines will not run and the computer may crash. Most antivirus companies now have fixes available for this virus.*

IE5 can leave Internet surfers vulnerable in two ways. According to Georgi Guninski,† a security hole within ActiveX, allows hostile code buried in a Web page or in an e-mail message, to run on a user's computer without the user's knowledge, **Fig. A.**

Simply accessing an infected Web page, or reading an infected e-mail or news-group message, allows this code free access to your computer's files. It can then plant a Trojan Horse program into your computer, or overwrite your system files, unless ActiveX controls, plug-ins and scripting features have previously been disabled.

As I write, Microsoft had not posted a patch or an advisory notice, for this problem.

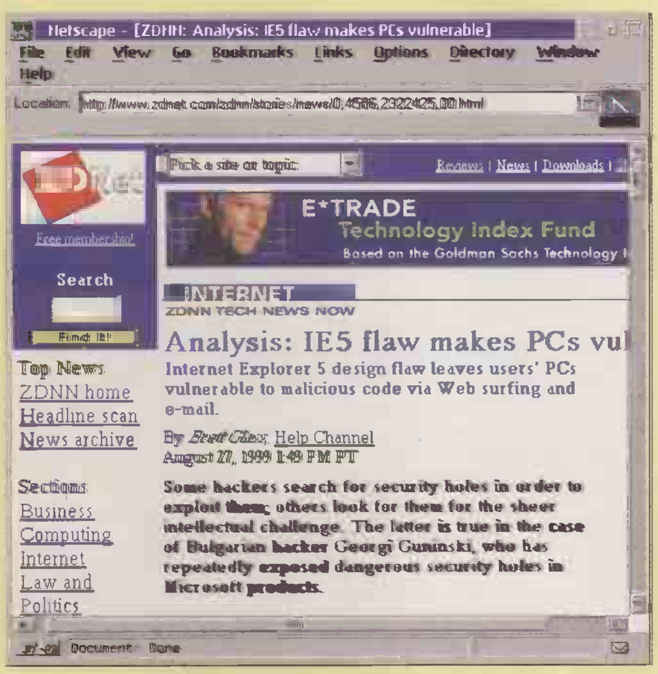


Fig. A. If you use Explorer 5 to access Internet, review your Active Desktop security and ActiveX scripting settings before logging on.

* 'Toadie' virus raises concerns in freeware community. http://www.zdnet.com/pcweek/stories/news/0,4153,1016141,00.html

† Analysis: IE5 flaw makes PCs vulnerable. http://www.zdnet.com/zdnn/

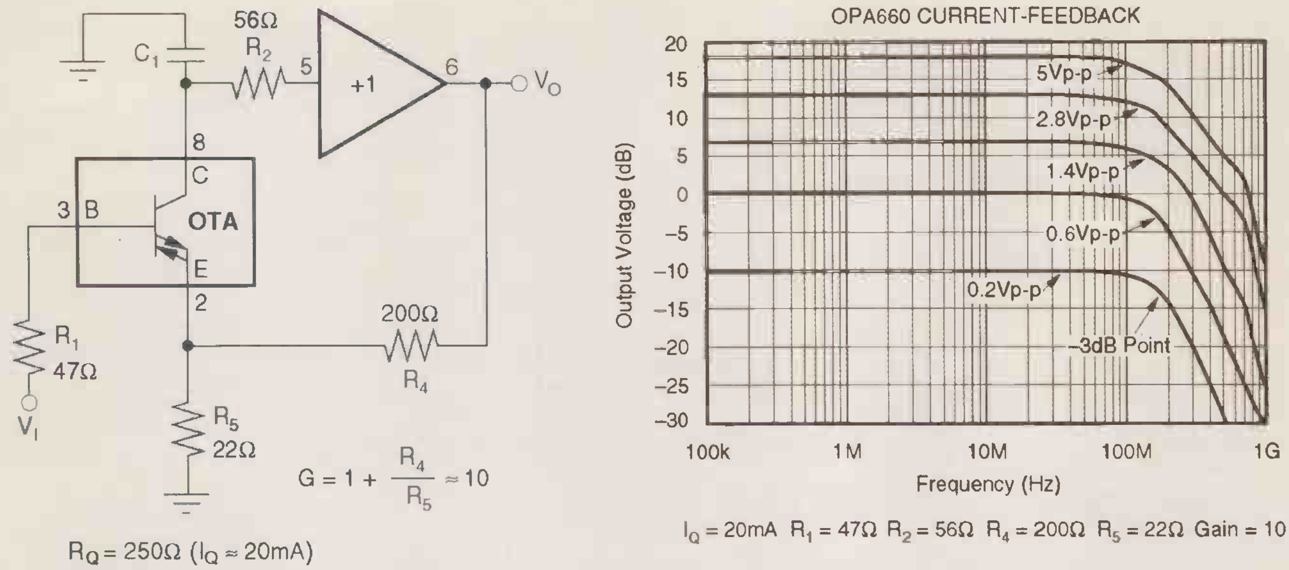


Fig. 2. The OPA660 configured as a current feedback amplifier with a gain of ten. For clarity the R_q resistor, which controls quiescent current, is not shown. It connects between pin 1 and the negative supply rail.

collector terminal for negative base-to-emitter input voltages.

Benefits of the OTA

Unlike a transistor, this OTA configuration is self-biasing, simplifying design and reducing external components. It is far more linear than any discrete transistor, providing a constant transconductance over a wide range of collector currents and frequency.

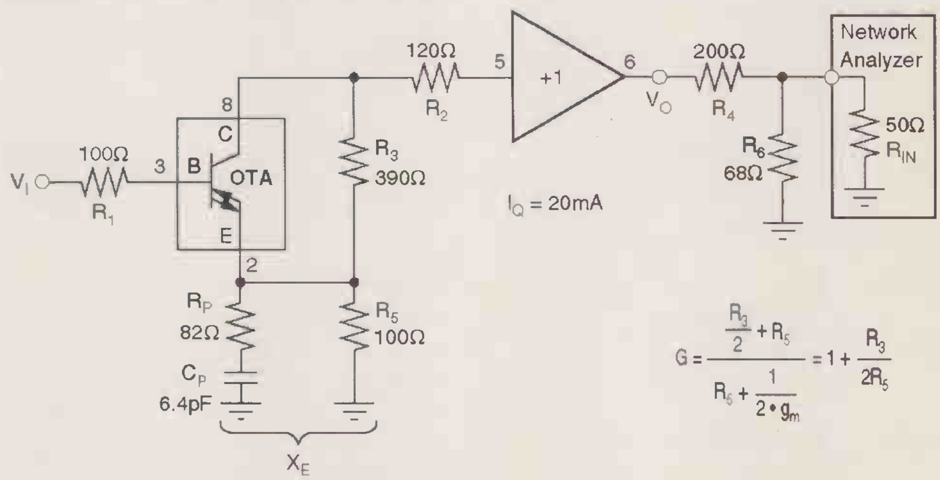
As you can see in **Fig. 1**, both the unity-gain buffer and the OTA have similar configurations, apart from their final output stages. The buffer uses emitter-output drive while the OTA has an additional stage with collector output drive.

These two blocks can be arranged as a wideband current-feedback amplifier, with input going to the OTA. The buffer output is coupled back, via 200Ω, to the emitter terminal of the OTA. Set to a gain of 10, this arrangement provides an almost flat response to 100MHz at a 5V pk-pk output, Fig. 2.

Even wider bandwidth is available by using the buffer outside the feedback loop and direct feedback from collector to emitter of the OTA. With a gain of three, this combination provides a flat response to more than 500MHz at 2.8V pk-pk output, **Fig. 3**.

To assist circuit development using this integrated circuit, Burr-Brown provides three different, pre-assembled demonstration boards using the DIL package. These provide both current and direct feedback amplifiers also the diamond-transistor/buffer configurations.

Two other boards provide layouts suitable for these applications, using the surface mount SOIC and the DIP packages.



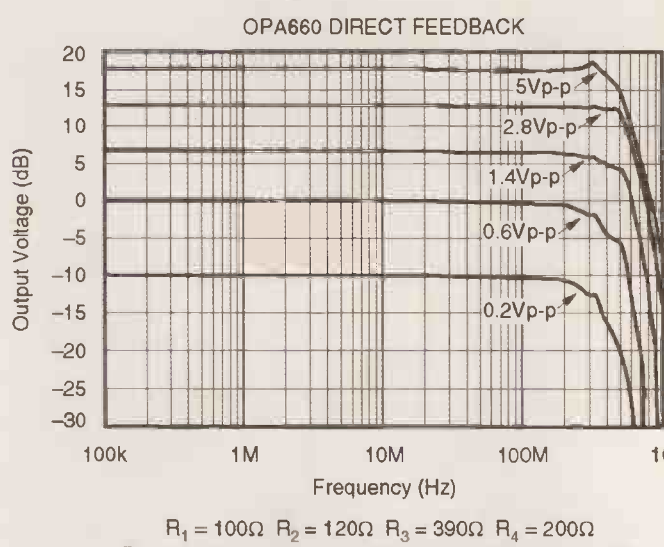


Fig. 3. Extended high-frequency performance is possible using the 'direct-feedback' connection. In this, the unity gain buffer is outside the feedback loop. Feedback is directly from collector to emitter of the OTA.

Background details and performance results of the experimental test circuits, which led to the final design of the OPA660, are described in application note AB-181. This can be downloaded from Burr-Brown's Web site.

Ultra-high-speed circuits

Application note AB-183, entitled 'New ultra high-speed circuit techniques with analog ICs' provides a good overview of the various high-speed applications possible using the

Fig. 4. The above, basic circuit arrangement functions as a multiplier. With R_{qc}=250Ω, g_m=67mA/V and R_{out} of 2.08kΩ, provides a multiplication factor of 35kΩ. Gain G=35kΩ/250Ω or 140 times. Varying the value of R_{qc}, changes the multiplication factor.

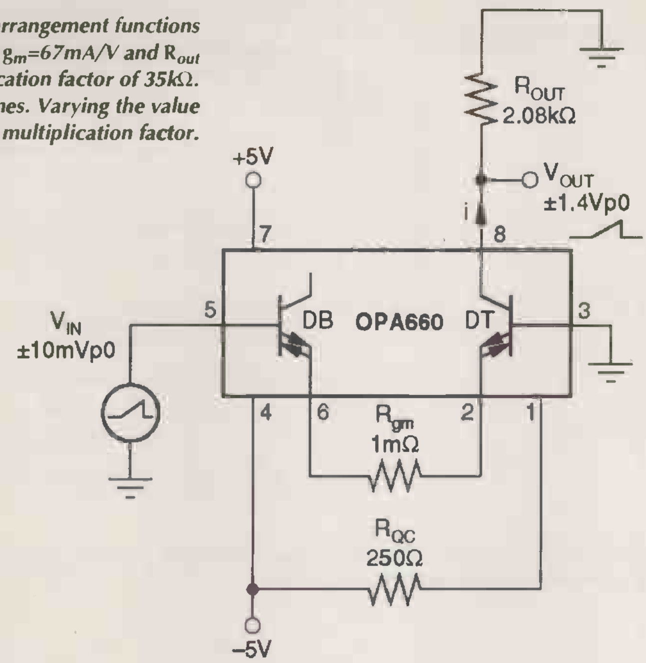
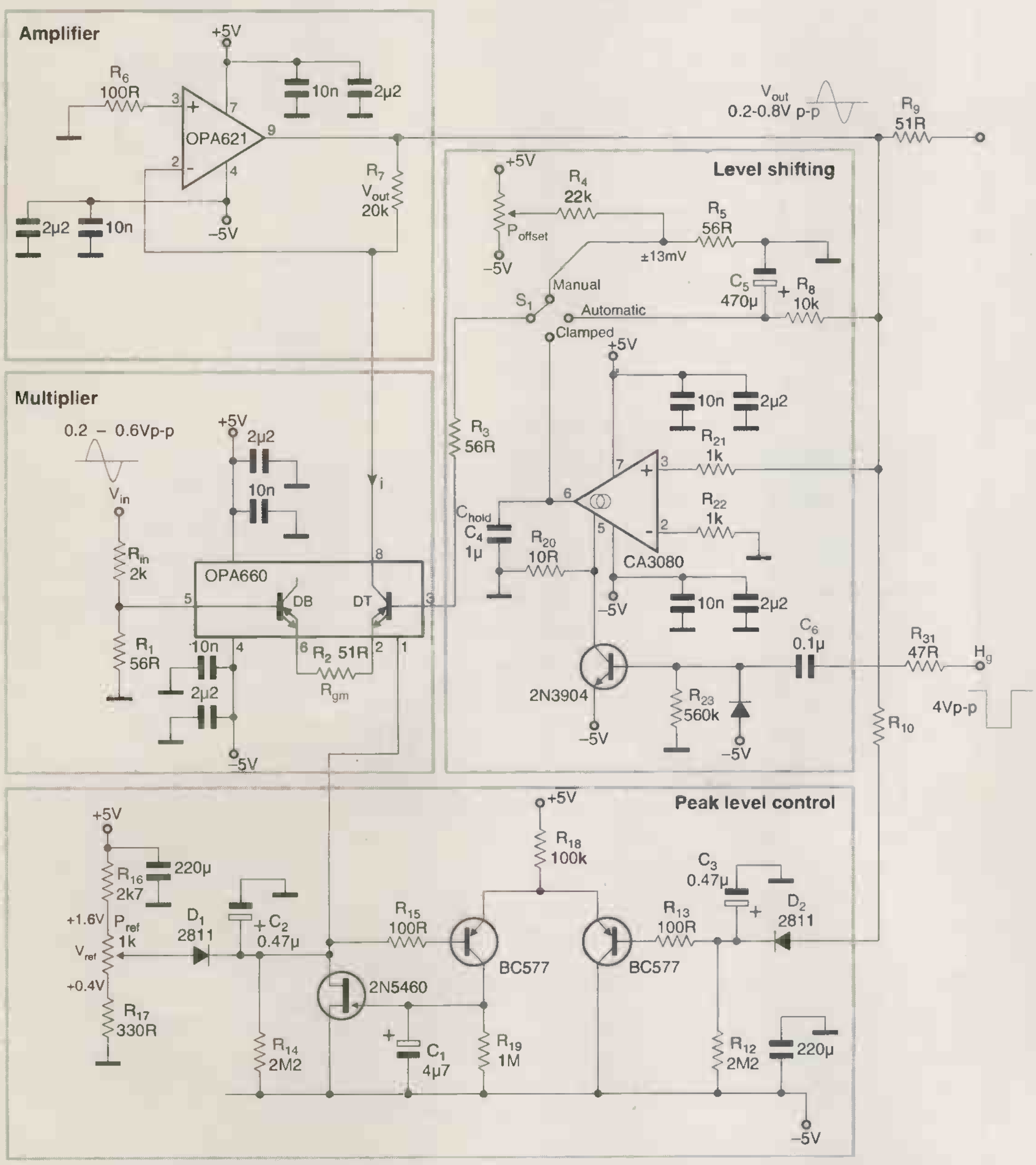


Fig. 5. Final schematic of the Burr-Brown AGC amplifier demonstration board. The peak level control section, at the bottom of the drawing, provides the variable R_{qc} needed to maintain a constant output voltage. Replacing the OPA621 amplifier with an OPA622 can extend bandwidth above this circuit's 80MHz limit.



OPA660. These include fast integrators usable with 8ns input pulses and low jitter, fast comparators working to 10MHz. RF signal rectifiers that work down to millivolt levels, variable-gain amplifiers and high-frequency active filters can also be made.

Design of an AGC system usable above 80MHz is discussed in application note AB-185. This design uses the OPA660 together with a peak detector, to control its own gain, maintaining a constant output voltage without using a multiplier IC. This AGC is achieved by using the OPA660 quiescent-current control input pin to vary its transconductance, **Fig. 4**.

A self-contained AGC circuit using this approach, can be evaluated using the dedicated demo board. A full description of the function of each of the four circuit blocks shown in this schematic, appears in application note AB-185, **Fig. 5**.

Active filter designs are usually restricted to relatively low frequencies. Application note AB-190, entitled 'Designing active filters with the Diamond Transistor' discusses the design of high-frequency active filters having a stop-band performance exceeding 100MHz, **Fig. 6**.

At these high frequencies, package parasitics, component parasitics and input/output coupling, dominate circuit design.

Wideband differential amplifier

This final application note returns us to the original reason for my Internet searches. It is entitled 'Building a 400MHz wideband differential amplifier: it's a breeze with the Diamond Transistor OPA660'.

In just four pages, application note AN-188 describes a differential amplifier having a flat gain of 6dB up to 400MHz. It has low power consumption, so can be battery powered.

Other aspects of its performance are also excellent. At 2V pk-pk output at 10MHz, harmonic distortion is low, first and second harmonics being at –57 and –55dB respectively.

The device's common-mode gain at 10MHz is –43dB and its pulse response rise and fall times are around 1ns. Resulting from its low noise density of 7.7nV/√Hz, the circuit is equally usable with much smaller signals, **Fig. 7**.

Should you prefer to roll off circuit gain below this 400MHz maximum, small changes of C_5, shown as 18pF in the schematic, should be evaluated.

A number of integrated differential amplifier circuits are available in

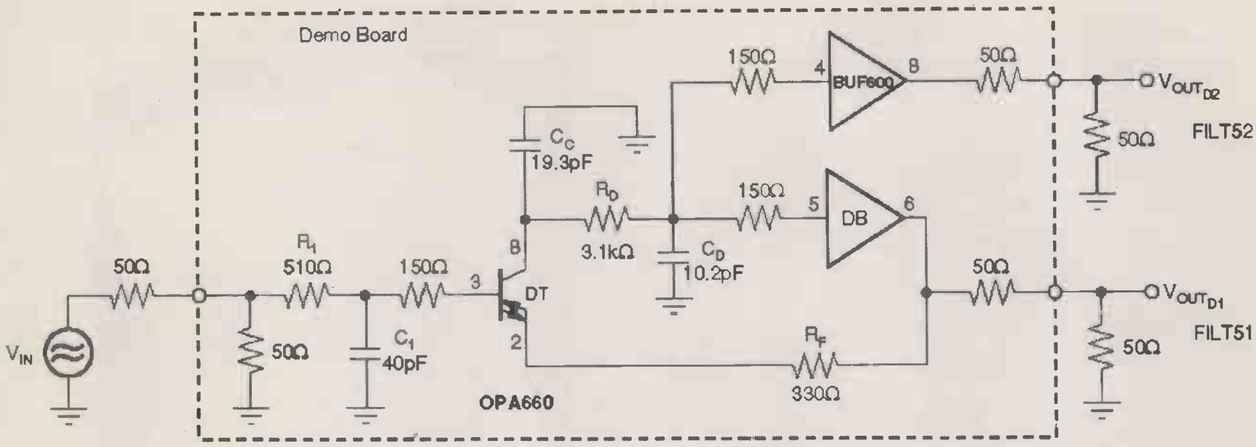


Fig. 6. Illustrating the OPA660 demonstration board used to build a third order, 10MHz low-pass filter having extended stop-band performance using the BUF600 output.

addition to those I have detailed. Not being transconductance types though, they were not identified in my Internet searches.

Other worthwhiles...

While I do not intend to list all the possibilities, a small family of amplifiers from Linear Technology should be mentioned[3].

Classified as video difference amplifiers and typified by the LT1193, these were designed as cable-sense amplifiers that could be used to 'tap' into coaxial cable runs, without disturbing the cable's loading.

The LT1189 amplifier, developed from the LT1193, is a gain-of-ten-stable, 35MHz bandwidth version. By increasing its feedback and using a small capacitor, typically 5pF, as a feedback zero across the feedback resistor, a stable gain of four up to 100MHz can be achieved. This application can be found in the data sheet for the LT1189.

Which circuit did I chose?

Superficially at least, the OPA660 circuit could produce my desired differential oscilloscope probe, except for two final requirements.

To accommodate the desired input voltage ranges, it may be necessary to attenuate the input voltage into the differential amplifier, then use gain after the differential stage, to restore signal levels.

To properly display small differential signals, it may also be necessary to provide a means of offsetting their DC levels.

If you are interested in building a similar, differential scope probe, you will find a number of helpful documents on Internet. These have been written by authors who work for companies manufacturing oscilloscope systems and probes. A small sample is appended in the reference. ■

Where to look...

1. Analog Devices Inc.	http://www.analog.com
2. Burr-Brown Corporation.	http://www.burr-brown.com
3. Linear Technology Corporation.	http://www.linear-tech.com
See also: Answers to frequently asked questions.	http://preamble.com/faq.htm

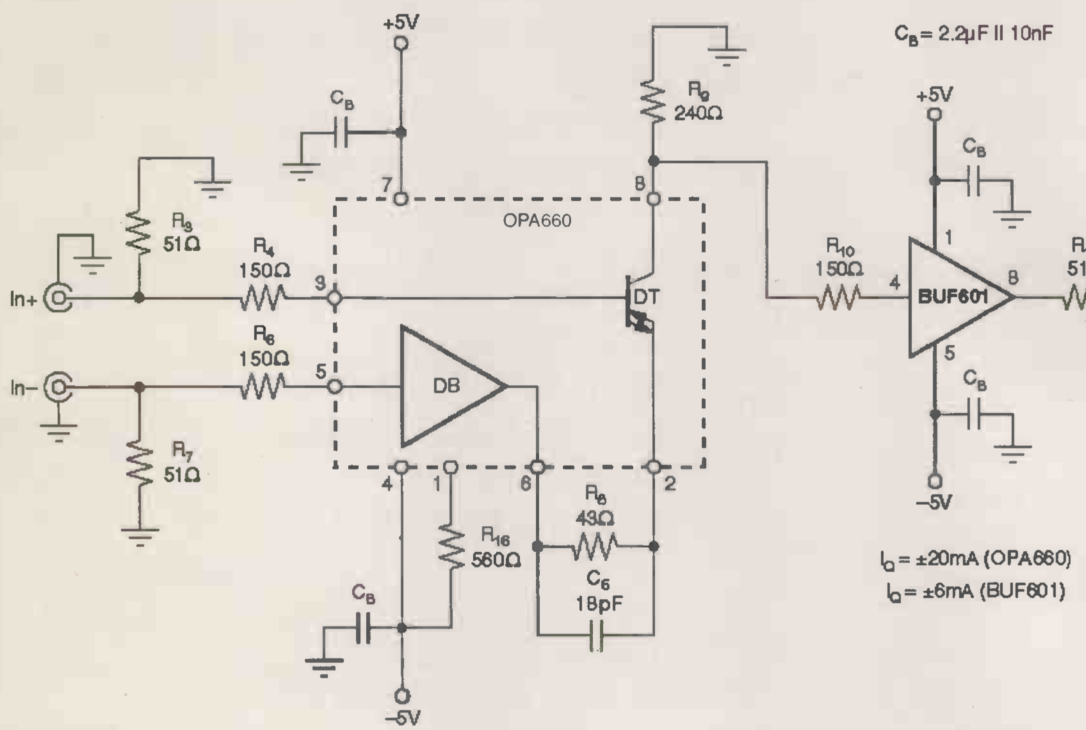


Fig. 7. The 400MHz wide-band differential amplifier built on the OPA660 demonstration board has a gain of four at the input to the BUF601 buffer output. Using a doubly-terminated 50Ω transmission line reduces overall input/output gain to 6dB. Using an 18pF for C_5 as shown, the 3dB frequency is 400MHz.

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