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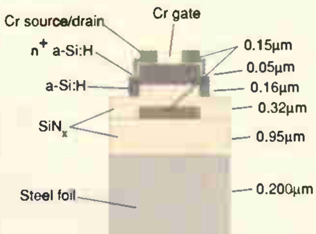


*Could steel outperform glass and polymers as a substrate for flat-panel displays? See page 274.*



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REED BUSINESS INFORMATION

# Modem mayhem

Just as you have forked out £200 for the latest 33.6kbit/s data modem – or probably twice as much to go ISDN – you're told you have got it wrong. You should have waited for the new 56kbit/s modem.

Or should you? All is not what it seems and this proposal for a new 56kbit/s modem 'standard' looks distinctly shaky. For a start, it's not a standard, more like two proprietary and mutually incompatible contentions for a standard. What is more, it is debatable whether it is truly the advance it claims to be. It could even become one of those glorious side-alleys, like PAL-Plus, DCC and the Sony Elcaset – technically ingenious but ignored by most users.

Ingenious these modems certainly are, achieving higher speed (in one direction) by eliminating one digital-to-analogue conversion process. What is not so clear is whether most users will actually benefit thereby. And if not, why upgrade to the new 'standard'?

Two competing developers have announced modems that achieve line speeds of up to 56kbit/s, but in the downstream direction only. The data that you transmit has a maximum transfer rate of 28.8 or 33.6kbit/s. Moreover, the two protocols, x2 from US Robotics and K56Flex being developed by Lucent and Rockwell are not mutually interoperable. While each vendor is attempt to grab market share – and sell their expensive equipment to Internet service provider hosts – the fact remains that they are not mutually compatible. If your host does not support the new standard your transmission will drop back to your previous standard speed, probably 28.8kbit/s.

The speed increase applies only for connections made to host modems equipped with the same 'flavour' of 56kbit/s as your own, which more or less restricts it to Internet connections. Point-to-point data transfer and connections to bulletin boards or your friends' PC parented on analogue lines will be restricted to 28.8 or 33.6kbit/s.

In many situations, too, any speed increase is illusory. On Internet connections at least, there is little to be gained from a lightning-speed connection to your nearest point of presence if the real log-jams prevail the other side. For the average user slow downloads will remain a fact of life until extra bandwidth is installed along the main arteries of the Internet.

For some users upgrading to 56kbit/s will involve minimal expense and might even be worthwhile. This is because US Robotics says that all of its products that currently support software downloads can be easily upgraded to x2. This does not apply to its older products, though.

Whether the upgrade turns out to be worthwhile or not really depends on take-up of the x2 protocol by Internet service providers. It remains to be seen whether they opt to support x2; currently K56Flex counts more companies – but not necessarily more market share – on its side.

***The notion that the new 56kbit/s modems represent an ISDN-killer is entirely false.***

Meanwhile, don't hold your breath waiting for either new standard to be ratified. In fact they may even be defeated on purely regulatory grounds. A report in the *Los Angeles Times* of 24th January suggests the 28.8kbit/s modem standard may well remain the norm for some while longer. The USA's regulatory body, the Federal Communications Commission, currently has a regulation that limits the amount of power used to send data through a telephone line – which could compromise the legality of faster modems.

The report argues that because newer, faster modems will require more power for data transmission than the existing rules allow, the FCC must grant a waiver before 56k modems can be released. Whichever viewpoint prevails, it is clear that asymmetrical 56kbit/s modems are an interesting way-station along the route to high-speed data transfer – but not the ultimate end-station. The notion that these new modems represent an ISDN-killer is entirely false. ■

*Andrew Emmerson*

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# Europe too slow on ISDN technology

Tardy telecommunications network operators are delaying the potential of networked computing by their slow implementation of ISDN and successor digital subscriber line (xDSL) technologies.

That was the message coming from the chairman and CEO of Intel, Dr Andy Grove, at a London seminar recently. "Technically there's nothing on the way to move us to higher bandwidth better than ISDN," said Grove. However, except for Germany, the implementation of ISDN is "very slow", he said.

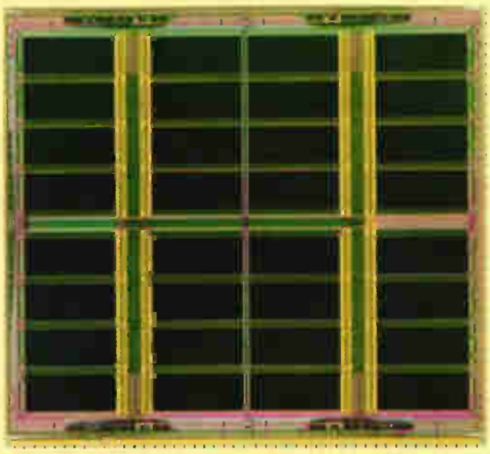
Driving networked computing forward was the fact that up to 200m people across the world have PCs that can be connected to the communications networks. But hobbling its progress is the limitation of the network. "We need improving bandwidth and declining prices and neither trend is being served sufficiently," said Grove.

"The computer industry does its stuff in delivering increased performance and reducing prices because it's a competitive and open industry", said Grove, "but the telecommunications industry has a government monopoly legacy which is not used to delivering its services in a competitive economy."

America is far in advance of Europe in using PCs for communications – 40m Americans have e-mail access, only 8m Europeans. A continuation of that gap could lead to a 'technology deficit' for Europe, said Grove.

However, he quoted a survey suggesting that the UK was far ahead of Continental Europe in plans to add Internet access to its business computers – 30 per cent of UK IT managers are intending to add it, compared to 12 per cent in Germany and only 6 per cent in France.

Grove reiterated Intel's commitment to keep its microprocessors compatible with all past software written for them. "Backwards compatibility is an immutable definer of our road map", said Grove, "it has been for fifteen years and it's going to be for a long, long time".

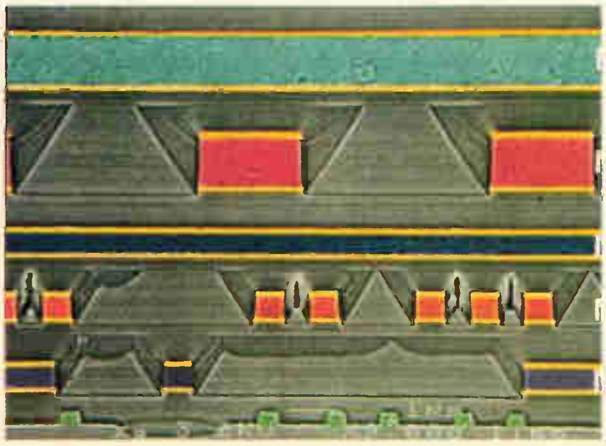


## 2Gbyte/s static ram holds 4Mbit

NEC has developed a 4Mbit, 500MHz static ram capable of a 2Gbyte/s data transfer rate. Designed for use as level two cache for microprocessors, the ram has a pipeline-burst architecture where data is transferred as a sequence of four, 32-bit words. The 12×11mm chip is fabricated in 0.25μm c-mos. Its current consumption is 270mA. An additional 40mA is needed to drive the 4cm path to the processor.

# New process delivers 0.18μm geometries

*LSI's G11 process uses five metal layers. Layers one to three are 0.85μm wide, while four and five have twice the width.*



LSI Logic launched its latest semiconductor process for Asic and c-mos devices this week. The G11 process uses transistors with an effective gate length (Leff) of 0.18μm, or 0.25μm drawn.

G11 devices will be able to integrate over eight million logic gates and 8Mbytes of s-ram on the same die, says the company. This corresponds to dies containing 64m transistors. Three-transistor d-ram and mixed signal circuits are also available.

Logic gate count has increased by 60 per cent over the previous G10 process. Speed is up by a claimed 30 per cent while power dissipation is a quarter of G10's.

Ronnie Vasishta, marketing manager for G11, said: "We see market needs separated into three distinct areas." These are low power, battery applications such as mobile phones; the high performance area including workstations and the 'balanced' market such as consumer goods.

LSI is providing two different libraries for G11: one for high performance, and the other tailored to high density and low power. The third market area would use a mixture of the libraries depending on a product's specific needs.

Initial G11 production is expected this year. Full production at LSI's 8in Gresham, Oregon fab is due in 1998.

LSI has joined a growing list of manufacturers offering 0.18μm devices. Texas Instruments and IBM have both announced a 0.18μm Leff process. NEC is believed to be waiting until March to release details of its process.

# Sensor detects acceleration in 3D

The University of California, Berkeley and Sandia National laboratories have described their three-axis micromachined accelerometer that includes on-chip servo and signal conditioning circuitry.

Both Analog Devices and Motorola already produce single-axis devices and Analog's has on-chip circuitry, so what is remarkable about this design?

"Apart from sensing all three axes, not just one or two, our accelerometer is different because it has fully differential signal conditioning throughout," said Mark Lemkin of Berkeley's team: "This increases its noise immunity to the point where a microprocessor could be placed on the same chip without disrupting the accelerometer's operation." The noise immunity requirement is bought into focus by the sensors output voltage of 7μV/mg (g is gravitational acceleration).

X and Y axes are sensed using two comb finger arrays similar to Analog's and Z-axis (out of the plane of the chip) measurements are made using a moving flat plate mass above a fixed plate. In this sense it is less sophisticated than Motorola's which has fixed plates above and below the moving mass, but simplifying the structure has allowed the use of a single polysilicon layer process. A capacitor with two fixed plates provides compensation.

Acceleration is measured by determining how much force is required to keep the moving masses in a fixed position relative to the substrate. The same capacitive electrodes are used both to sense the mass position and provide a restraining force. To separate the functions, the tasks are performed sequentially, the inertia of the plate integrating the force pulses.

The control loops use noise shaping. Lemkin said: "This idea is not new, but noise shaping, using a ΣΔ loop, provides a direct digital output. This kind of loop can be difficult to stabilise and we have included forward path compensation using a discrete time FIR lead filter."

Sandia built the device using its buried micromachine technology where the micro-accelerometer is built in a trench on the wafer and covered with $SiO_2$ while the c-mos circuitry is fabricated.

James Smith of the Sandia team said: "The etch resist for the c-mos circuitry is spun out onto the wafer. Unless the wafer surface is completely flat, and micromachines are too high at around 6μm, it does not flow to a consistent thickness. Unfortunately, the c-mos cannot be made first because it is damaged by the temperature needed to anneal the micromachine."

Annealing the machine first, then burying it, leaves a flat surface for c-mos fabrication and the $SiO_2$ is etched away at the end to uncover the machine and free its working parts.

## Sticky problem with subscribers

Sincere apologies to UK subscribers who did not receive their cover mount gift of a pack of Resintech adhesive. At the eleventh hour, the Post Office decided that the cover mount was unsuitable to travel through the post. Apologies to Resintech too, who pulled out all the stops to manufacture the packs. Would any subscriber wishing to obtain their gift please write to Electronics World Glue Offer, Simmonds, 82-84 Peckham Rye, London SE15 4HB. Please include your name, address, subscriber number and telephone number if possible.

# 23GHz transistors promise to reduce phone costs

Philips Semiconductors has developed a way to make bipolar junction transistors (bjts) for the mobile phone market.

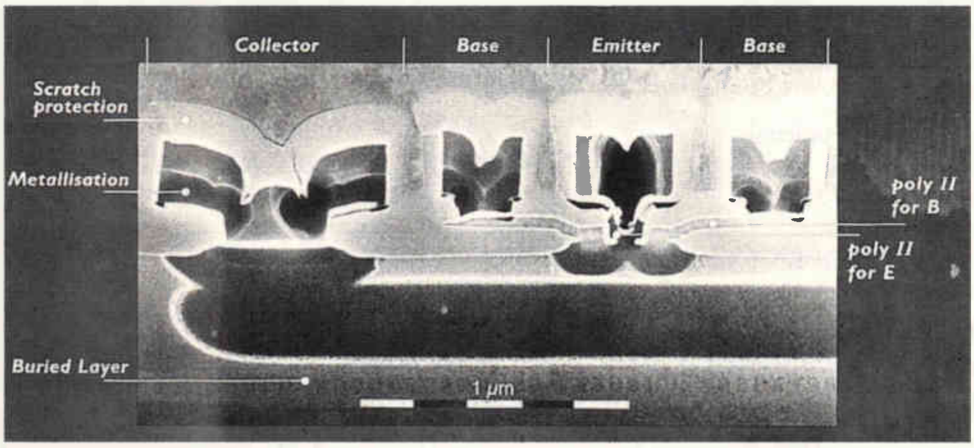
Operating at up to 23GHz, these fifth-generation silicon devices are claimed to be faster than the previous process. Being easier to make, they also promise to reduce the cost of the rf portion of cellular and cordless phones.

Wout Bijker, product marketing manager at Philips, said:"To enable the mobile phone market, handset manufacturers need to offer low cost, smaller and lighter phones."

Much of the recent research in mobile phones has focused on their shift to the higher 1.8 and 1.9GHz operating frequencies. Receiver and transmitter stages need transistors for amplifiers working at these frequencies.

Gallium arsenide (GaAs) devices have the appropriate speed, low noise and power characteristics, but are expensive. Philips claims its bjts have the right gain, noise and power characteristics, and are cheaper than their GaAs counterparts.

**Richard Ball,** *Electronics Weekly*




*Mobile transistors... The double poly process has all connections to the top layer of metal. In older processes, the emitter and base were on one side of the substrate, the collector on the other. The active region of the device is grown epitaxially using chemical vapour deposition. Base and emitter connections are made via two layers of polysilicon. In the earlier process, the base metal lines and pad formed a capacitor with the collector on the opposite side of the substrate. Now the base-collector capacitance is reduced, speeding up the bjt.*

# Terabit memory chips produced using quantum wells

Single electron memories are frequently talked about among the storage literati, but Professor Hans Ludwig Hartnagel of the Technical Institute of Darmstadt, Germany points out a flaw in these devices: "The time taken to transfer, and therefore to read, an electron is non-deterministic, it cannot be predicted. It is like radioactive decay, it could happen after a picosecond or only after a whole second." The consequence, if Hartnagel is to be believed, is that a single electron per bit memory is not a practical proposition.

"The time distribution of a single-electron transfer event makes using Boolean logic impossible. Instead, some kind of statistical, fuzzy logic is required," said Hartnagel: "However, if a reasonable number of electrons is transferred, say 100, the time distribution of electron transfers is statistically far more certain. The time of peak electron flow is almost entirely predictable."

His argument is, that single electron storage cells have to be surrounded by a statistical decision making logic, wasting their size advantage. Far more sensible, he claims, to use around 100 electrons and be sure that the bit exists and can be manipulated with certainty.

Hartnagel proposes a quantum well charge coupled approach analogous to that used in charge-coupled device (ccd) cameras.

His device uses quantum wells, made of GaAs, in a AlGaAs substrate. Electrons in the GaAs do not have enough energy to escape into the AlGaAs, even with the additional thermal excitation that room temperature gives them. They are therefore trapped, or stored.

By placing a potential difference across two electrodes, one at each end of the cell, an energy gradient can be created to 'tip' the electrons into an adjacent cell. Once the gradient is removed the electrons are stored in the adjacent cell.

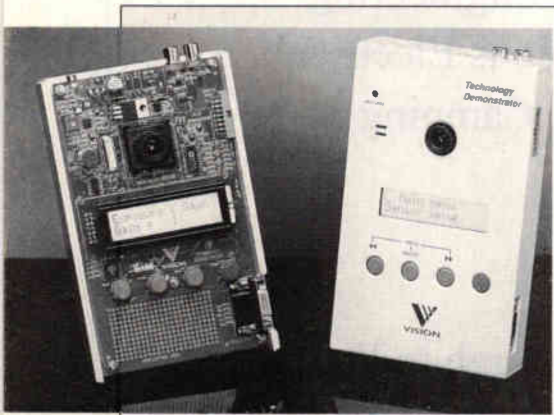
In his memory, the quantum wells are placed in a square matrix with X electrodes running in one direction between the cells and Y electrodes in the other.

While maintaining all other electrodes at a 'hold' potential, operating a pair of X electrodes tips a whole column of cells into their neighbours. Operating a pair of Y electrodes tips a whole row. By manipulating both X and Y electrodes, a single cell can be tipped into its diagonal neighbour. The plan is to use diagonal tipping to turn the whole matrix into a single serially-addressed storage cell chain.

Hartnagel has high hopes for quantum memories: "Conventional 1Gbit memories will be with us in two to three, perhaps five, years. Quantum terabit memories should around in 10."

His team has so far made larger cells transfer successfully and has modelled the 100 electron cells.

**Steve Bush**, *Electronics Weekly*



***Smile please... Edinburgh camera-on-a-chip company, Vision, has developed a technology demonstrator based on its medium resolution 5400 monochrome image sensor. Potential customers can evaluate the sensors and use the design as a basis for their own systems. The unit includes the sensor, lens, a-to-d converter, audio circuit, microcontroller and RS232 port for pc connection. The mode of operation is controlled through panel buttons and the lcd. Vision's 5400 devices use a c-mos process to integrate the image sensor and processing circuitry on the same die. The 384 by 287 image can be output directly as an EIA or CCIR composite video signal.***

# Will network computers overtake pcs?

Half the UK's large companies believe that network computers (NCs) will replace pcs as the choice for corporate desktop computing within the next five years, according to City market analysts, Durlacher Multimedia.

Meanwhile, IT industry analyst Robin Bloor says that enthusiasm for the NC is mounting in the UK. "The 'buy in' for this is very strong," he told *EW*, adding that "there are a number of beta sites where NCs are being used which have already noticed significant reductions in administration costs."

The Durlacher Intranet Report 1997, which is based on interviews with 100 IT directors and managers from top 1000 UK companies, cites that corporate Intranets will help to drive the change to NCs.

But Bloor argues that the savings in PC software and hardware upgrade costs will be the key driver. "In the business environment you want the tools to do the job," he said. "The last thing you want is the tools to keep changing for you."

This claim is backed by BT, which was the first European company to deploy Sun Microsystems' JavaStation NC. Terry Carlin, head of systems at BT Customer Service said: "We believe that with NCs the support costs can be reduced quite considerably."

Bloor maintains that NCs will be the obvious choice for business in years to come, while PCs will be mainly used in the home. "The home pc market and the corporate market have been provided with the same product for years. It's wrong," he said.

**Jon Mainwaring**, *Electronics Weekly*

## MGS wins MOD contract to supply surplus equipment

Distributor MGS (UK) Ltd has won a contract to trade Ministry of Defence surplus electronics equipment that has been traditionally been sold via auction and tender.

Part of the MOD's 'Partners in Enterprise' initiative, the contract is a new concept, giving MGS access to almost all surplus electronics equipment becoming available from the UK's most important military bases.

In the past, dealers in surplus equipment have been forced to bid at auctions. From March this year, they will be able to buy their requirements from MGS. This will make it possible for dealers to update their stocks as they deplete, rather than having to take their chances at auction.

According to MGS's Director, Tommy Hedges, "This means that surplus dealers, who have previously had to pay varying, and sometimes inflated, prices at auction can now buy from us at standardised prices – giving the customer a better deal. And because MGS will be holding large stocks in its warehouse, it will be easier for dealers to provide their customers with more continuity in product ranges."

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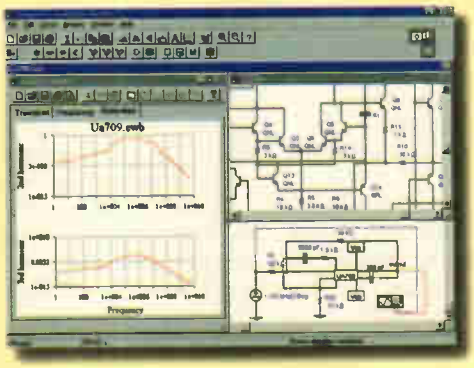


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INTERACTIVE

# RESEARCH NOTES

Jonathan Campbell

## How too much Sun killed a satellite

Earlier this year, AT&T's Telestar 401 satellite suddenly stopped sending signals to Earth. Scientists are still not exactly sure why this happened, but they believe the event was just one effect of a massive solar storm. However the difference to previous odd events connected with solar activity is that this time researchers had in place a fleet of satellites that was able to observe the storm – the biggest ever documented – as it blew around the Earth.

In fact the storm is one of the best-documented space weather events ever. It began when, on 6 January, the Soho satellite took a picture of the Sun that showed the edge of a huge eruption called a coronal mass ejection (cme). Four days later, the disturbance was recorded as it sped by another satellite, called Wind, that is designed to monitor the solar wind just up-stream from Earth. Then, hours later, the Polar satellite recorded the effects on energetic particles in Earth's radiation belts. Over the next several days, the intensity of the radiation belts increased more than 100 times over their previous levels.

The three satellites – Soho, Wind, and Polar are part of the International Solar-Terrestrial Physics program, a collaboration of NASA, the European Space Agency and the Japanese Institute of Space and Aeronautical Science. From ground observatories, satellites, spacecraft and computer simulations and models, ISTP is building a comprehensive picture of Earth's magnetosphere and how it interacts with the sun.

"We compiled the most complete data available on conditions in the magnetosphere during the event," says Geoff Reeves, project leader for Polar's energetic particle instrument at Los Alamos National Laboratory.

"Combined with information from the other satellites, now we can better understand why and how these solar events sometimes produce big effects."

## Could steel replace glass in flat panel displays?

Dramatic improvements in the durability and lightness of flat panel displays could be on the horizon following announcement of successful devices built on a steel foil substrate instead of glass. The development has been announced by two researchers at Princeton University, who have fabricated high-quality thin film transistors (tfts) on 200μm-thick stainless steel.

Rigorous mechanical stressing of the devices – including dropping from a height of 16m onto a hard surface, and flexing the substrate in multiple orientations – are reported to have produced no change in the characteristics of the tft ('Amorphous silicon thin-film transistors on steel foil substrates', *IEEE Electron Device Letters*, Vol. 17, No 12, pp. 578-560).

The advantages of steel foil in terms or durability are pretty clear. But although stainless foil has been used in photovoltaic devices, its use as a substrate in display electronics has not been attempted before.

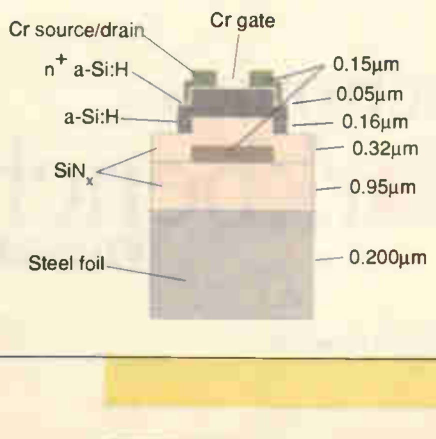
However, as the researchers point out, while the opacity of metal foils limits tft circuit applications to reflective or emissive displays, metal surfaces can be modified by coatings to achieve a wide range of optical properties. Moreover, the thermal coefficient of steel is a much better match to that of silicon. By adjusting the alloy, complete matching is possible.

This is a far more preferable situation than exists with the other great hope for more durable devices – plastics. Thermal coefficients of polymers are around 20-50 times that of silicon, and there are several other engineering problems that have to be overcome before plastics can be seriously considered.

But the current research shows that stainless-steel substrates could be the breakthrough needed in the fabrication of non-breakable tft backplanes, and would greatly reduce the substrate thickness and weight in comparison to traditional glass substrates.

So far, though the devices have shown a relatively high quality, no attempt has been made by the Princeton engineers to optimise substrate or film parameters. This leads to optimism that the metal-foil alternative has the potential to offer a very robust process, easily transferable to industrial applications.

*More information contact: SD Theiss, Department of Electrical Engineering, Princeton University, Princeton, NJ 08544, USA.*

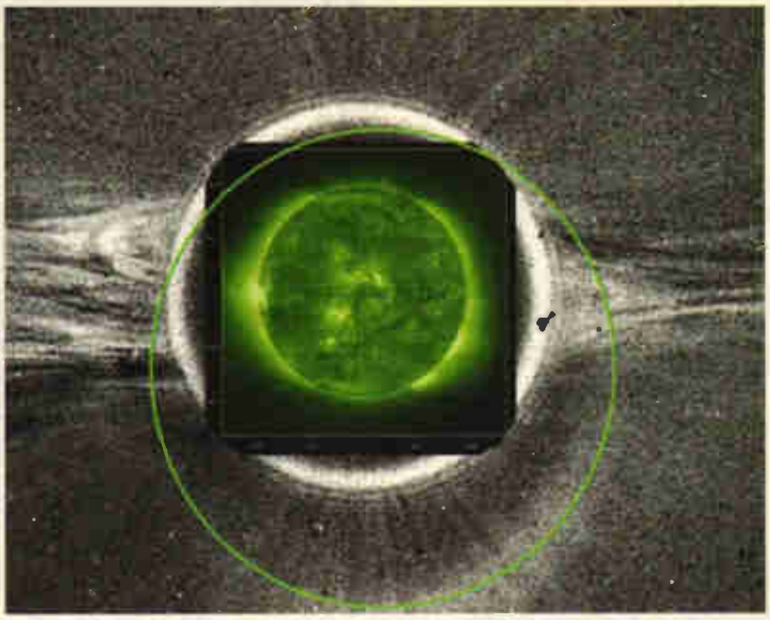



*Stainless steel foil substrates can open the way for a new generation of rugged devices.*

Coincidentally, at the time of the solar event scientists and satellite operators from across the country were meeting to discuss ways better to forecast the 'weather' in space that affects satellites.

Over phone lines, fax machines and the world wide web, scientists with space weather data frantically downloaded the information onto their laptops. The result is that researchers were able to build up a preliminary but remarkably complete picture of what happened on the sun. It showed how the disturbance travelled to Earth, what it did to the magnetosphere when it got here, "and how that might have killed a $200 million satellite," adds Reeves.

*More information contact: Gary Kliewer, Los Alamos National Laboratory, Los Alamos, New Mexico 87545, USA.*



***Start of the storm that killed a satellite: The cme, or coronal mass ejection, observed by the large angle spectrometric coronagraph aboard Soho, at the start of its journey Earth-wards at speeds between 400 and 500km/s. The image is a projection of the cme halo onto an extreme ultraviolet telescope image of the sun.***

# Putting the μ back into microphone

University of California engineers have produced an on-chip microphone that demonstrates greater sensitivity than any previous similar device and can also double as a loudspeaker. Key to design of the microfabricated device is a cantilever diaphragm that produces less residual stress than previous diaphragm microphones, while the relatively large deflections of the free end can produce a significant acoustic output ('Piezoelectric cantilever microphone and microspeaker,' SS Lee *et al*, *Journal of Microelectromechanical Systems*, Vol. 5 No 4, pp. 238-242).

Microphones are basically pressure sensors that detect airborne sound pressures that are ten orders of magnitude lower than ambient pressure. So the microphone needs an extremely compliant diaphragm to have an acceptable sensitivity.

This latest development reflects growing interest in the micromachining of microphones. Among the advantages of micromachining over conventional fabrication are improved control, extreme miniaturisation, the ability to integrate with on-chip circuitry, and potential low-cost as a result of batch processing.

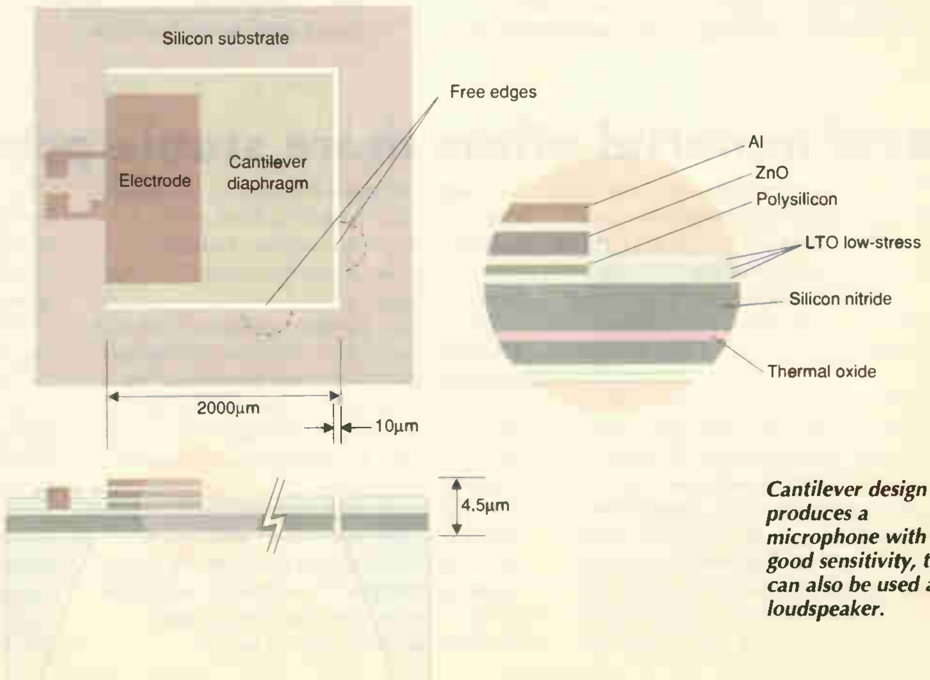
The 2000 by 2000 by 4.5μm California cantilever diaphragm has a zinc-oxide piezoelectric thin film on a supporting layer of low-pressure chemical-vapour-deposited low stress silicon nitride. By controlling distribution of residual stress, out-of-plane deflections were typically no more than 35μm.

Measured sensitivity of the microphone is around 3mV/μbar in the low frequency range, rising to 20mV/μbar at the lowest resonant frequency of 890Hz.

Using the device as a loudspeaker produced a sound pressure level (spl) of 75dB at 890Hz, increasing to approximately 100dB at 4.8kHz.

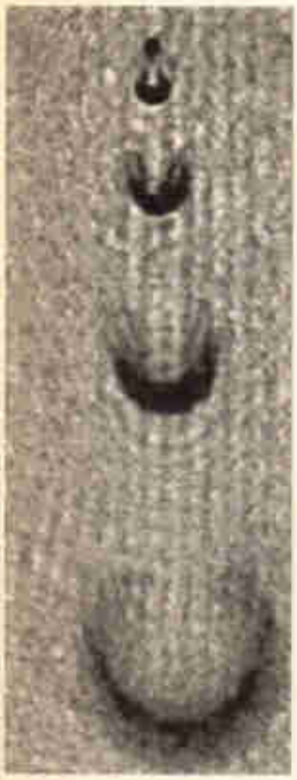
The researchers say that the technique used to manufacture a flat, multilayer cantilever, involving patterning different thicknesses of ZnO film, could also hold relevance to production of other micromachined structures.

*More information contact: Seung Lee, Berkeley Sensor & Actuator Center, Department of Mechanical Engineering, University of California, Berkeley, CA 94720, USA.*




***Cantilever design produces a microphone with very good sensitivity, that can also be used as loudspeaker.***

# New laser knocks atoms into line



The new atom laser emits pulses of coherent atoms. Each pulse contains 100,000 to several million coherent atoms and is accelerated downward by gravity. The curved shape of the pulses was caused by gravity and forces between the atoms. (Field of view 2.5 mm × 5.0 mm.)

Physicists at MIT have created the first atom laser, a device that resembles an optical laser but emits atoms instead of light. The atoms have the remarkable property of coherency – moving in phase to form a single giant matter wave – and the resulting beam can be focused to a pin-point or made to travel large distances with minimal spreading. Already, researchers are speculating how the laser might be used to deposit atoms onto computer chips, creating much finer patterns than currently possible.

The atom laser has been a long-sought goal in physics, but there were many doubts whether it could be realised. An important intermediate step towards its development was the creation of a Bose-Einstein condensate (bec). This was achieved by chilling a gas of atoms to such a low temperature that the atomic matter waves overlap, and the atoms lose their individual identities.

*Michael Andrews, Marc-Oliver Mewes, and Wolfgang Ketterle gather around the machine they and their MIT collaborators used to demonstrate the first atom laser.*

The MIT group cooled the gas in two stages. In the first stage, laser cooling, the atoms were bombarded with optical-laser light. Frequencies and polarisations of the laser beams were chosen in such a way that photons emitted by the gas atoms were slightly more energetic than photons absorbed by the atoms. The energy difference is responsible for the cooling effect. After absorbing and emitting about 100,000 photons, the atoms reached a temperature of about 100 microkelvin.

The atoms were then cooled using evaporative cooling. In this technique, the hottest atoms are removed from the atomic sample, thus reducing the average energy – and therefore the temperature – of the remaining atoms. In addition to being cooled, the atoms also had to be very well insulated from the room-temperature environment. This was accomplished by confining the atoms in a special magnetic trap inside an ultra-high vacuum chamber.

Once the bec has been formed, the beam of Bose-condensed atoms is extracted from it by applying an oscillating magnetic field. In this way, the new laser emits multiple pulses of Bose-condensed droplets, each 'droplet' containing 100,000 to several million coherent atoms.

The last remaining obstacle was to demonstrate coherence. For this, the group applied a standard method used to show the wave nature of particles or radiation. In this technique, two samples are overlapped. If the photons or atoms in the separate samples are indeed coherent, each sample behaving as a giant wave, then the samples will interfere with each other, in the same way that happens when two waves meet in a pond. The result: a periodic pattern, or standing wave, that can be photographed.

To their jubilation – and after 20 hours of aligning and focusing their instruments – this is exactly what the MIT team found.

# Novel material offers more stable pcbs

Zirconium tungstate, the wonder material that contracts instead of expands when heated, could be used in a composite form to produce circuit boards that expand at the same rate as the silicon devices it contains. This is just one of the many applications currently being considered for this peculiar material.

Since the discovery of zirconium tungstate's odd behaviour last year in the Center for Advanced Materials Research at Oregon State University, scientists have been rushing to find out more about it and to look for potential applications. So far, more than 40 private companies are said to have requested material samples from OSU, and Arthur Sleight, the Milton Harris Professor of Materials Science at the University says that applications are now being considered across a whole range of technologies, including electronics, optics, fuel cells, oxygen sensors, thermostats, and even new dental filling products.

The negative thermal expansion, from near absolute zero to about 800°C of zirconium tungstate has never before been observed. It's now known to be caused by oxygen atoms in the material 'vibrating' when heated, pulling the zirconium and tungsten atoms closer together.

The latest reported advance that has caused surprise its behaviour under pressure. At near 1000bar its crystal structure collapses, forming molecular 'cross braces' and losing much of the negative thermal expansion characteristic that makes it unique.

But when heated moderately, the material then regains its property of shrinking when heated, leading Sleight to suggest a possible use in some type of composite that could serve as a 'shock absorber.'

The material also offers unusually high oxygen mobility, suggesting possible uses in fuel cells or oxygen sensors.

As yet, all future applications are still on the experimental drawing board. But Sleight says he is "more optimistic than ever" about the potential for real world uses.

*Contact: Arthur Sleight, Milton Harris Professor of Materials Science, Center for Advanced Materials Research, Oregon State University, Corvallis, Oregon, USA. Tel 00 1 541 737 6749.*

Jamel Akib

**Building on his earlier fast driver amplifier work, Giovanni Stochino has now developed what is possibly the fastest high-power audio amplifier of its type. More impressively, he has done so without sacrificing audio purity.**

# 300V/μs power

In my previous article[1] I described how the basic architecture of high-speed voltage feedback amplifiers can be applied to the design of high-performance audio-power equipment. Detailed design information for a non-slewing 100 watt into 8Ω mosfet power amplifier was given. It featured a linear output speed of ±170V/μs and its rated output power total harmonic distortion figures were 0.004% and 0.045% at 1kHz and 20kHz, respectively.

Subsequent investigations have shown that further evolution of the basic architecture can provide higher speed and better thd figures – comparable with top-class hi-fi amplifiers – relative to the basic configurations.

This article reports the results of my recent investigations and experiments and provides design details for a new low-distortion, very high speed 100W into 8Ω audio power amplifier, which features a slew rate higher than ±300V/μs and rated power thd figures of less than 0.002 % and 0.020% at 1kHz and 20kHz, respectively.

## Improved high-speed architectures

In my last article, I demonstrated that the thd and speed performances of the basic high speed voltage-feedback architectures appear to be influenced by the low, i.e. unity to two, current gain of the intermediate stage. This implies that a substantial improvement of both thd and speed figures can be obtained when a higher current gain class AB intermediate stage is incorporated in the original schemes[1].

The problem here is that this change has to be done without degrading the other performances and, more importantly, the robustness of the basic design.

With this requirement in mind, my investigations have focused on the topologies shown in Figs **1** and **2**.

The input stages are designed to provide class AB operation and the simultaneous availability of large push-pull currents, $I_R$ and $I_L$, with the appropriate phase, at nodes A and B, Fig. 2. I have already shown [2] that this feature is very important to avoid the dangerous simultaneous conduction of the upper and lower half of the intermediate stage. During simultaneous conduction there is a risk of driving intermediate stage transistors out of the dynamic safe operating area.

Avoiding simultaneous conduction contributes to the robustness of the amplifier. It is particularly important in very fast high-power amplifiers, where the feedback loop forces the intermediate stage to provide high peak currents during large/fast input transients.

Another key feature of these schemes is the use of common-base transistors $Tr_{10,11}$. These play a twofold role:

- to allow the use of low voltage high current gain transistors $Tr_9$ and $Tr_{12}$, which increases the available gain and peak current of the intermediate stage;
- to improve amplifier linearity.

Relative to Fig. 2, the configuration of Fig. 1 potentially provides higher input stage large signal transconductance and less power consumption. As is well known, large signal transconductance in both schemes is determined mainly by cross coupling resistor *R*. However, while in Fig. 2 the value of *R* is mainly governed by the need to provide the level shifting voltage with reasonable power consumption, in Fig. 1 this limitation does not apply. As a result, *R* can be set as low as convenient.

Because of the above, Fig. 1 promises better speed and lower power consumption than Fig. 2, although at the expense of offset and noise precision and distortion performance. Differences in the two schemes are only in the input stage. Intermediate and output stages are exactly the same for both designs.

Compared with the simplified circuit diagram presented in my March '96 article, the clamping network at the output of the input stage in these designs shows one additional diode, which has been introduced to increase the intermediate stage peak output current to about 80mA. Accordingly, higher maximum output rates of change are to be expected. In order to produce comparable results, the two amplifiers are designed with as close as possible phase margins and unity gain frequencies under closed-loop conditions.

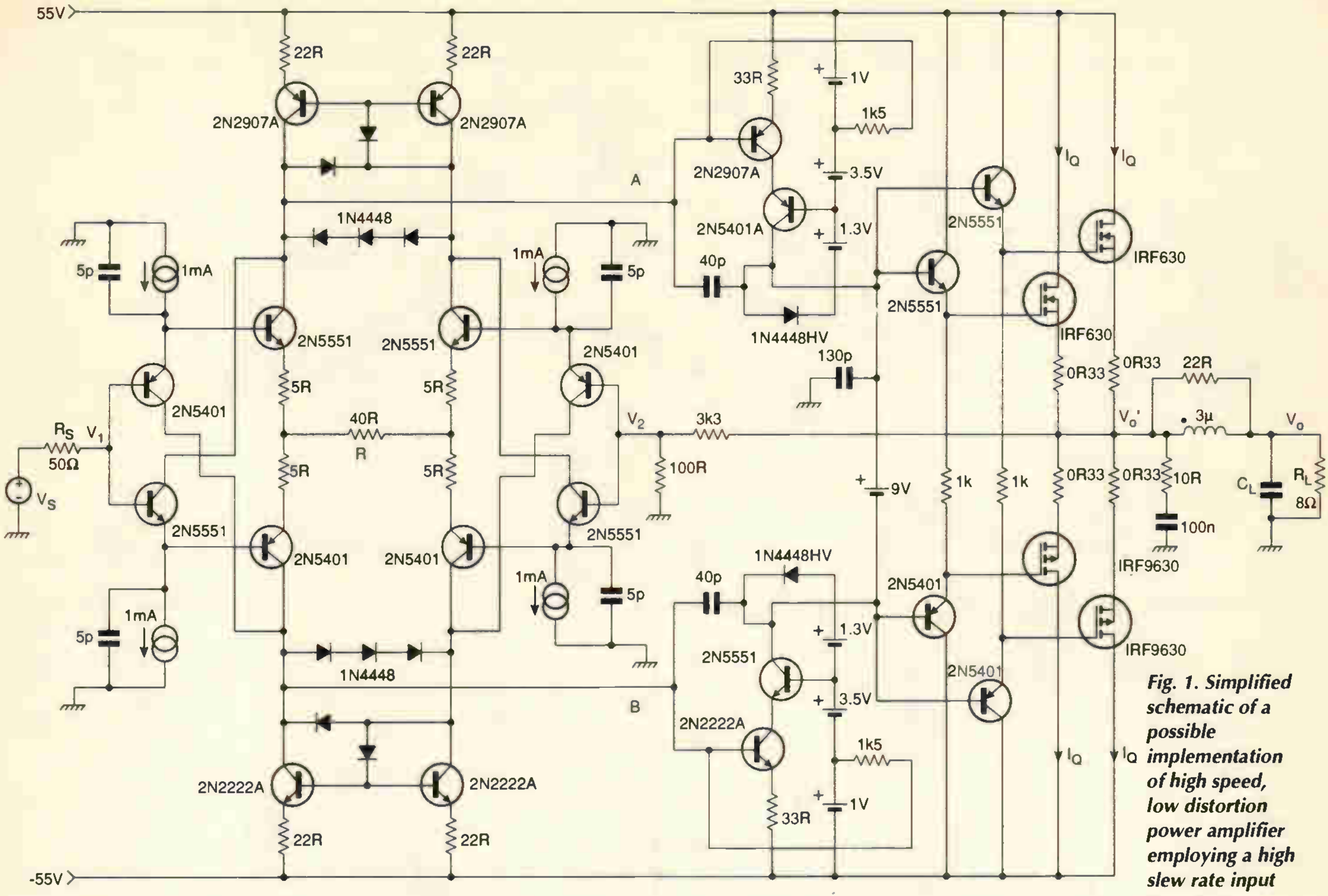



*Fig. 1. Simplified schematic of a possible implementation of high speed, low distortion power amplifier employing a high slew rate input stage.*

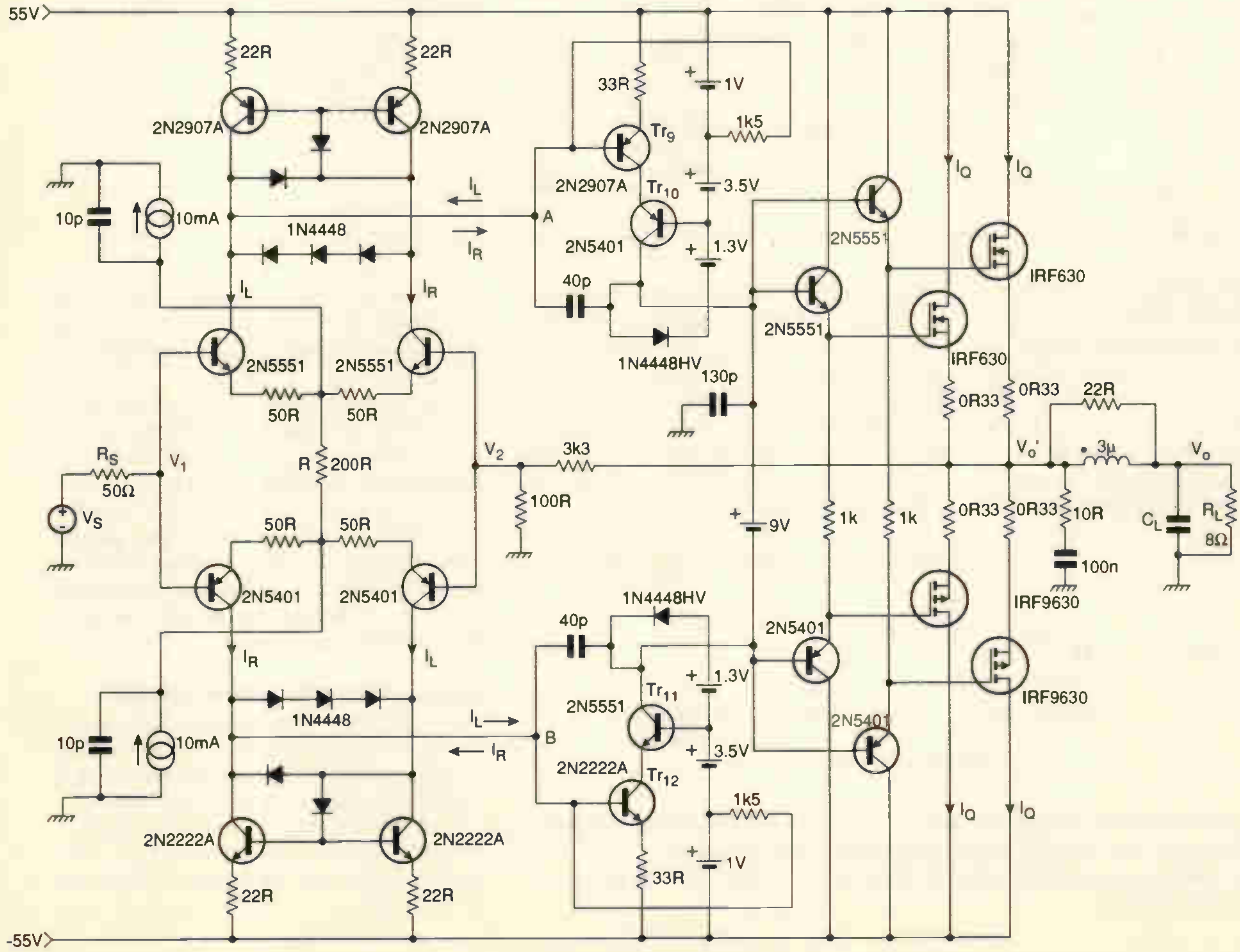



*Fig. 2. In this preferred implementation of a high speed, low distortion power amplifier, a non-slewing input stage is the main difference relative to Fig. 1.*

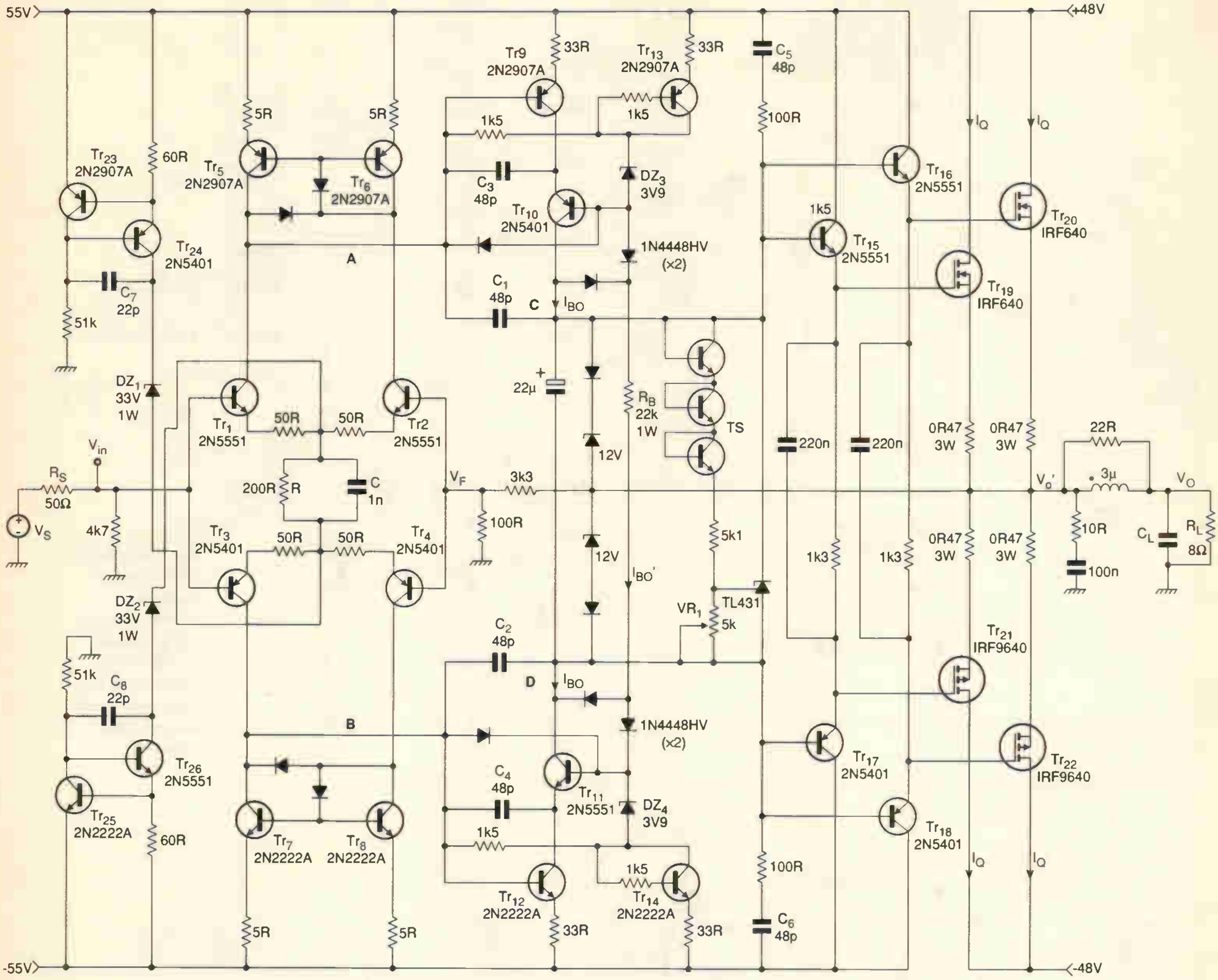



*Fig. 3a). Detailed circuit diagram of the final 100W/8Ω audio-power amplifier, featuring a speed higher than ±300V/μs, and a rated power thd of 0.002% at 1kHz and 0.018% at 20kHz. Note that all diodes are 1N4448 Diodes 1N4448HV are 1N4448 selected for a reverse voltage higher than 120V. Add 100μF//100nF decoupling to each 55V rail and 1000μF//2×100nF to each 48V rail.*

Some Spice simulation results are reported in **Tables 1** and **2**. Here, the main characteristics of the two new amplifier configurations are compared with the basic non-slewing architecture, with similar characteristics.

It is clear that the new implementations provide better speed and thd performances than the basic non-slewing architecture design, confirming the theoretical predictions.

Figure 1 and 2 have very similar closed-loop performances. However, due to the reduced number of transistors in the input stage, Fig. 2 offers better open-loop performance, in terms of frequency response and phase margin, as well as less noise.

In the light of the above, Fig. 2 seems to represent the best candidate for the design of a high-performance audio power amplifier, although power consumption is higher due to the level shifting current needed to bias the input stage. Moreover, this topology can be expected to provide reduced sensitivity to layout and parasitics, as well as load impedance variations. Consequently it will simplify design and implementation.

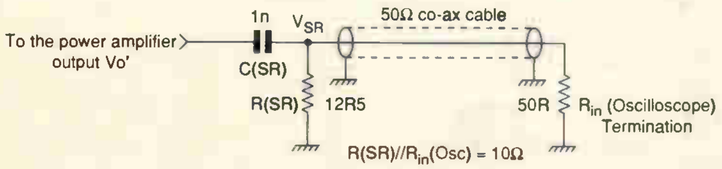



*Fig. 3b). Slew rate test circuit from D. Self[3]. Component values and circuit have been adapted to high-speed measurement. Slew rate, SR, can be determined by the following; $SR \approx V_{SR(max)}/(C_{SR}R_P)=100\times V_{SR(max)}$, in V/μs, where $R_P=R_{(SR)}//R_{IN(OSC)}=10\Omega$. Oscilloscope bandwidth is higher than 200MHz.*

## Implementing the power amplifier

Design has been optimised through intensive simulation work and verification tests on the experimental prototype. Measurements have substantially confirmed simulation results.

Discrepancies only occur when simulation data are close to or below the limits of available test equipment, the readings from which include noise, as well as thd. This is the case

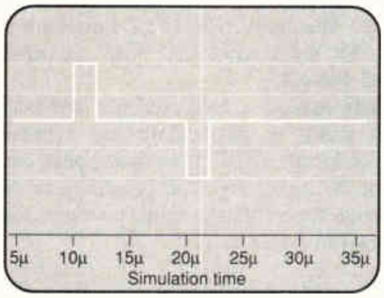



*Fig. 4. Input stimulus type used for verifying the amplifier's speed, during simulation and experiments. Vertical scale is 3V/div. Maximum speed measurements were made using both standard and Self methods.*

*Table 1. Characteristics of Fig. l and Fig. 2 fast audio-power amplifiers. Test conditions are $I_Q$=120mA, $R_s$=50, Load=8Ω//0.5µF.*

| Characteristic | Basic nsa[1] | Fig. 1 | Fig. 2 |
|---|---|---|---|
| Best input offset voltage[2] | 350µV | 180µV | 170µV |
| DC gain, open loop | 80dB | 110dB | 111dB |
| Unity-gain frequency | 22.5MHz | 19MHz | 22MHz |
| Open-loop gain at 20kHz | 64.5dB | 67dB | 68dB |
| Open-loop amplifier phase margin[3] | –81° | –127° | –93° |
| Closed-loop amplifier phase margin[4] | +82° | +79° | +76° |
| Slew rate, 10V pp square wave input | ±160V/µs | ± 210V/µs | ±185V/µs |
| Output noise, bandwidth 80kHz | 34µV rms | 50µV rms | 31µV rms |

*Table 2. THD of amplifiers in Fig 1 and Fig 2 with same test conditions as Table 1.*

| $V_{out}$ (Vpp) | Basic nsa[1] design | | Fig. 1 | | Fig. 2 | |
|---|---|---|---|---|---|---|
| | 1kHz | 20kHz | 1kHz | 20kHz | 1kHz | 20kHz |
| 20 | 0.0018 % | 0.0240% | 0.0008 % | 0.0140% | 0.0006% | 0.012 0 % |
| 80 | 0.0090 % | 0.0380% | 0.0005% | 0.0100% | 0.0004% | 0.0080 % |

Notes
1. Non-slewing amplifier
2. In the simulation phase, devices and components have been considered perfectly matched.
3. Amplifier only, i.e. without the feedback network.
4. Amplifier plus feedback network. Closed loop gain is 30.6dB.

for thd at 1kHz. The differences at 20kHz can be explained by layout problems in the experimental prototype and/or by the influence of component mismatches.

## Final design

**Figure 3a** shows the complete circuit diagram of the final low thd, high speed 100W, 8Ω audio power amplifier.

Compared with Fig. 2, extra capacitors $C_3$ to $C_8$ are introduced in the assembled prototype. These components compensate for layout parasitics and achieve a clean step response in all operating conditions, **Figs 4, 5** and **6.**

The diode clamping network on the collectors of the input stage transistor has been simplified. Two diodes connected to zener diodes $DZ_3$ and $DZ_4$ perform the same task of the original circuit. Here, positive and negative peak currents of the intermediate stage are slightly higher and symmetrical than in Fig. 2.

The biasing network of the intermediate stage is made from $Tr_{13}$, $Tr_{14}$, $DZ_3$ and $DZ_4$, in addition to current setting resistor $R_E$. Nominal bias current, given by,

$$I_{BO} \approx I_{BO}' = (V_{CC}+V_{EE}-2V_Z-4V_{BE(on)})/R_B$$

and is about 6mA.

Bias setting and stabilisation of output power mosfets is achieved by means of the *TL431* shunt regulator and temperature sensing network *TS* in Fig. 3a. This network consists of three diode-connected *2N5551*s and is mounted very close to the output mosfets on the same heatsink to provide thermal coupling.

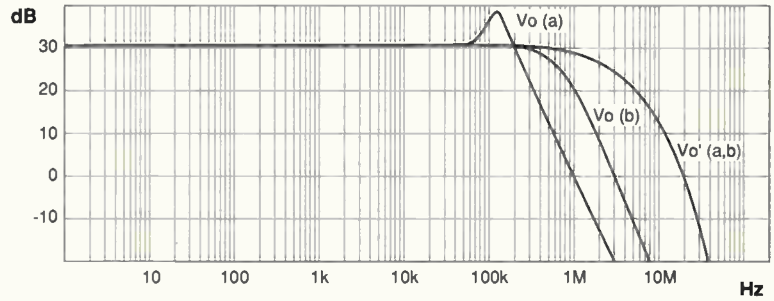



*Fig. 5. Simulated frequency response – i.e. magnitude – of the power amplifier in Fig. 3. Test conditions are $V_o$(a) load=8Ω//0.5µF, $V_o$(b) load=8Ω//0.05µF, vertical scale is 10dB/div and frequency range is 1Hz to 100MHz.*

This scheme provides a stable working point for the temperature sensor *TS*, which is insensitive to $I_{BO}$ variations. This is because current $I_{TS}$ is kept constant by the *TL431*'s 2.5V internal reference, through the relationship $I_{TS}=V_{ref}/R(T_1)$.

Since, as is well known, each transistor provides a $\Delta V_{be}/\Delta T$ of about –2 mV/°C, *TS* yields a total $\Delta V_{TS}/\Delta T$ of –6 mV/°C. This has been found adequate to compensate for the intrinsic $I_Q$ changes with temperature of power devices.

Bias current $I_Q$ of each mosfet is set at 120mA via trimmer $VR_1$, after a reasonable

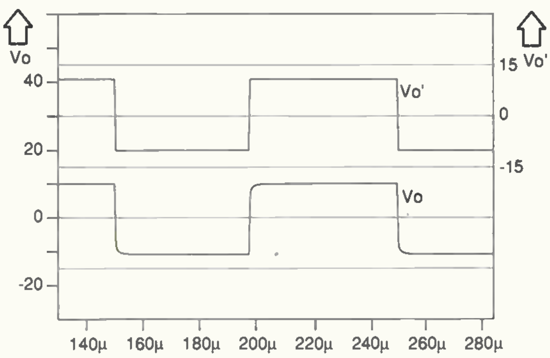



*Fig. 6a). Simulated voltage step response of the power amplifier in Fig. 3. Test conditions are $V_o'$=20V peak-peak, load=8Ω//0.005µF, vertical scale is 15V/div and frequency is 10kHz.*

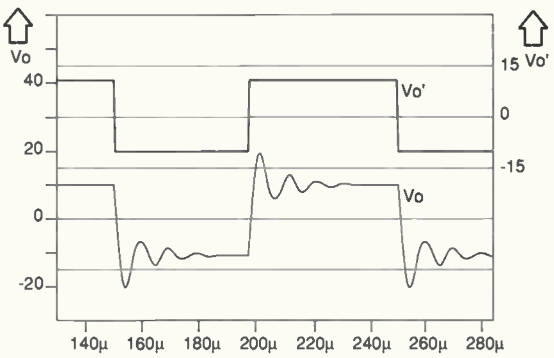



*Fig. 6b). Simulated voltage step response of the power amplifier in Fig. 3. Test conditions in this case are the same as for 6a), except for the load, which is 8Ω//0.5µF.*

amplifier warm-up time. Make sure to set this trimmer to its highest value before applying power to the amplifier. Measured $I_Q$ variations during operation are less than 20%.

## Supplying power

To increase the amplifier's efficiency, separate unregulated ±48V supply rails are used for the output power devices, which are *IRF640* and *IRF9640* types from International Rectifier. The rest of the amplifier is powered by two regulated +55 and –55 V supply rails.

**Tables 3** and **4** demonstrate the notable improvement of harmonic distortion figures. At 1kHz, measured thd is mainly limited by the available instrumentation, as illustrated by the fact that it remains virtually unchanged when load impedance reduces to 4Ω.

The maximum rate of change of the output voltage results in excess of 300V/μs, confirming that the new architecture is viable for reliable high-speed power amplification. Measurements of slew-rate were made both in the traditional way, and in accordance with the practical method suggested by Douglas Self,[3] with appropriate adaptations.

The test circuit is shown in Fig. 3b. Assuming $V_O' >> V_{SR}$, the maximum rate of change $SR$ is determined by,

$$SR \approx \frac{V_{SR(\max)}}{C_{SR} R_P} = 100 \times V_{SR(\max)} \text{ V/}\mu\text{s}$$

where $R_P = R_{SR} // R_{IN(osc)} = 10\Omega$.

To the best of my knowledge, this speed is the highest ever reported for a high power audio amplifier, which makes use of voltage-feedback.

The theory behind the speed performance of this architecture can be basically explained as follows. The maximum current available at nodes A and B depends on the maximum input voltage, $V_{max}$, which can be safely applied to the input of the amplifier. This is given by equation 4 of my March '96 article,

$$I_{A(\max)} = \frac{V_{(\max)} - 2V_{be(on)}}{2R_e + R} = \frac{V_{EBO} - V_{be(on)}}{2R_e + R}$$

This current amounts to about 18mA for the component value and active device types used in Fig. 3a.

Since capacitance at nodes A and B in Fig. 3a is about 50pF, the maximum slew rate across $C_1$ and $C_2$ is $SR_{A,B}$=360V/μs. Capacitors $C_3$ and $C_4$ do not play a major role in this context because the voltage variation across them is limited to a few volts.

On the other hand, the current available at the output of the intermediate stage, nodes C and D, is about 80mA. Total node capacitance, including the reflected capacitance of the output power devices, is less than 230pF. Slew rate at the input of the output stage will therefore exceed $SR_{C,D(min)}$=350V/μs.

## Bias current considerations

It is worth pointing out that this high value of slew rate can be sustained by the amplifier only if biasing current $I_{BO}$ is large enough to charge/discharge at the same rate the base-collector capacitances $C_{bc}$ of $Tr_{10}$ and $Tr_{11}$, which equal 5-8 pF. This means that $I_{BO} \geq SR_{CD(min)} C_{bc}$ has to be set at 2.8mA.

A safety margin is recommended for taking into account parasitics and base drive requirements, which equals,

$I_{B(peak)}/\beta_{(min)}$=80mA/30=2.7 mA.

The minimum output slew rate $SR_{(min)}$ will be slightly less than $SR_{CD(min)}$, due to the gate driving requirements of the output power devices. The above theoretical values are in line with simulation, and with measured results, Table 4.

In this design, a 1nF capacitor has been added across $R$ to increase the dynamic transconductance and the available peak current of the input stage corresponding to the maximum expected input signal transients, say 3V peak. In such a case,

$$I_{A(peak)} = \frac{V_{in(peak)} - 2V_{be(on)}}{2R_e} \leq 18\text{mA}$$

This results in a slight increase of speed for input signals within the linear dynamic range of the amplifier and in a further reduction of the already low residue of dynamic intermodulation distortion.

Cross-coupling capacitor $C$ needs to be treated very carefully. In fact input transistors $Tr_1$ to $Tr_4$, under large signal conditions, behave like a full wave rectifier of the voltage difference $V_{IN}-V_F$. Current flowing in $C$ is thus unidirectional. This results in a dynamic charge build-up across $C$, which is particularly important at high frequencies and during transients, when $V_{IN}-V_F$ is usually larger.

The charge build-up could end by producing undesirable bias and gain modulation of the input stage, and, consequently, increased high frequency thd and intermodulation distortion. This effect is also evident from the fact that while $C$ can truly help to boost the linear speed of the amplifier during occasional transients, it does not produce the corresponding improvement of the linear power bandwidth and of the dynamic intermodulation distortion.

## Minimising charge build-up

In order to minimise the above side effects, a low value of capacitance should be chosen. Definition of the right value of $C$ is not an easy task, since its influence on the circuit performance is both amplitude and frequency dependent. The following rule of thumb has proved effective in many applications,

$$C \leq \frac{1}{10(2\pi R F_M)}$$

where $F_M$ is the maximum input frequency, which is 20kHz for audio applications. This implies that the zero introduced by $R//C$ in the large signal frequency response of the amplifier has to be located far above the audio frequency range. According to the above empirical inequality, $C$ should be lower than 3.9nF. As a matter of fact, the value employed in this design, 1nF, has not produced measurable effects on thd performance. ■

***Table 3. Total harmonic distortion of final amplifier in Fig. 3a, with $R_s$=50Ω, $I_Q$=120mA and 80kHz bandwidth.***

| $V_{out}$ ($V_{pp}$) | Spice simulation 8Ω load | | Measured 8Ω load* | | Measured 4Ω load* | |
|---|---|---|---|---|---|---|
| | 1kHz | 20kHz | 1kHz | 20kHz | 1kHz | 20kHz |
| 5 | 0.00010% | 0.0040% | 0.0031% | 0.005% | 0.0035% | 0.007% |
| 10 | 0.00025% | 0.0140% | 0.0024% | 0.008% | 0.0029% | 0.010% |
| 20 | 0.00070% | 0.0190% | 0.0020% | 0.011% | 0.0023% | 0.013% |
| 40 | 0.00060% | 0.0145% | 0.0023% | 0.015% | 0.0023% | 0.018% |
| 80 | 0.00060% | 0.0110% | 0.0021% | 0.018% | 0.0023% | 0.026% |

*Instrumentation limit, thd+noise): 0.002% at 1kHz; 0.003% at 20kHz.

***Table 4. Further characteristics of Fig. 3a amplifier, $R_s$=50Ω, load=8Ω, $I_Q$=120mA***

| Characteristic | Spice simulation | Measurement results |
|---|---|---|
| Input offset voltage | .... | 1.6 mV |
| Slew rate†, $C$=0pF | +336/–297V/μs | +310/–360V/μs |
| Slew rate†, $C$=1nF | +360/–304V/μs | +360/–370V/μs |
| Output noise, bw=80kHz | 31μV (rms) | 39μV (rms) |

† ±6V peak pulse input, as in Fig. 4.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1. Stochino, G, "Non-slewing Audio Power Amplifier", *Electronics World*, March 1996, pp. 256-259.
2. Stochino, G, "Ultra-fast Amplifier", *EW*, October 1995, pp.835-841.
3. Self, D, "High Speed Audio Power", *EW+WW*, September 1994, pp.760-764.

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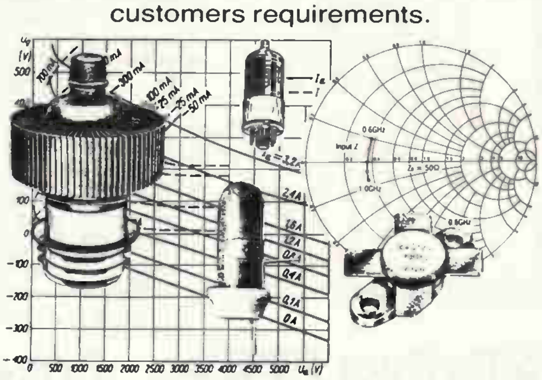

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CIRCLE NO. 116 ON REPLY CARD


Hashim Akib

**To successfully re-use alkaline cells, recharging is best done while the cell is still has about two-thirds capacity. But how do you know when the cell is ready for recharging? Rod Cooper explains how, and expands on the charger circuit presented last month.**

# Battery-low warning

**Warning**

**Never attempt to recharge alkaline cells with anything other than a charger that is specifically designed to recharge alkaline-cells. Such a charger was described in last month's issue.**

The question most frequently asked is how many times an alkaline-manganese cell can be recharged? On the bench, I have achieved ten times original capacity – that is over 30 recharge/discharge cycles at 30% discharge, plus any remaining charge. But these tests used consecutive discharge/charge cycles, so they do not represent everyday use.

In practice, without a timer to tell you when to recharge, you can expect to get ten recharges at 30% discharge, but this depends a lot on the type of usage. Considering that mains electricity costs 7p per kWh and alkaline-manganese cells cost about £55 per kWh this is still very good economics.

With a timer, you could reasonably expect double this figure, but a lot depends on the ageing effect that all electrochemical storage is subject to. If there are numerous charge/discharge cycles in a short period the results are better. For this reason, is it not a good idea to recharge clock batteries for example.

## Implementing the charger

Readily available AB range aluminium cases are ideal for housing the charger described in last month's issue. The lid can be easily arranged to swing open to insert cells. Being all-metal, the enclosure gives a fair degree of shielding from electromagnetic interference which my article last month showed could trigger the comparator prematurely.

With this type of aluminium case it is possible to use the base as a heat-sink for the output transistor, $Tr_2$. Not a lot of heat is generated, so the point of using a generous area of

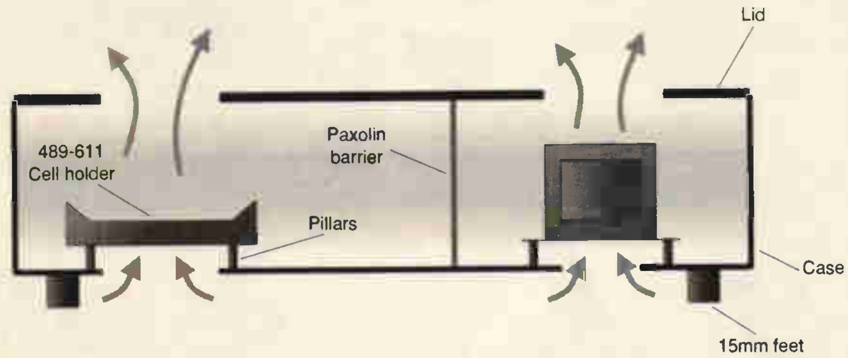


*Fig. 1. Cross section of a housing suggested for the alkaline-cell charger described last month.*

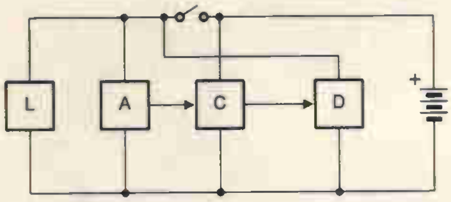


*Fig. 2. Elements of the timer circuit for helping determine when a cell is 1/3 depleted.*

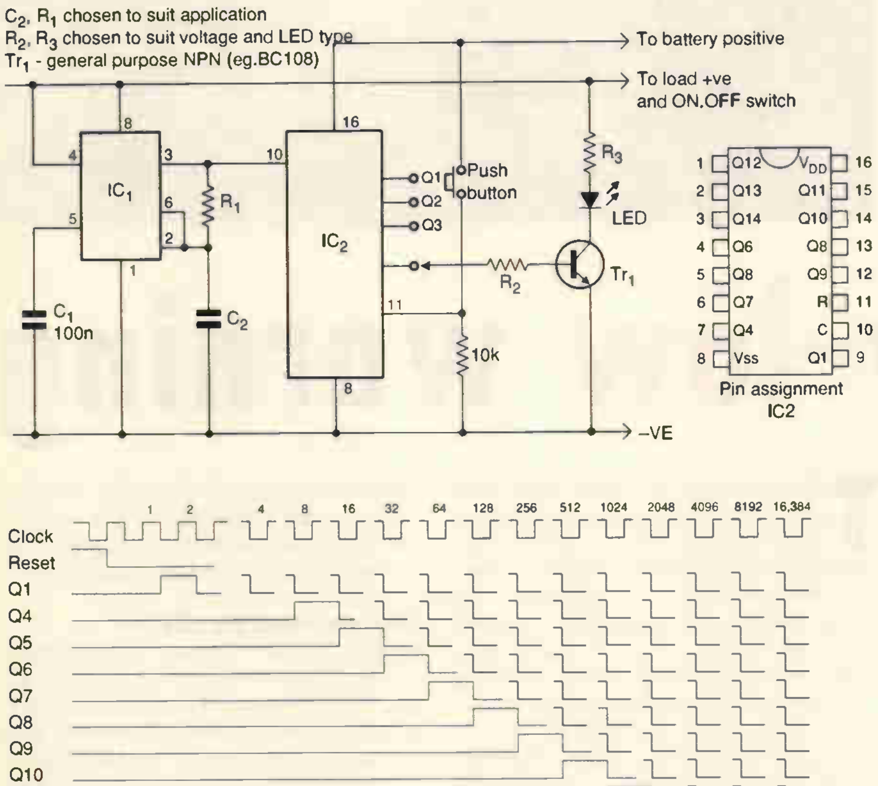


*Fig. 3. While the battery-operated appliance is switched on, the counter counts. Once the timer is tailored to suit the current drain of the appliance and capacity of the cell, this method gives an accurate indication of when the cell needs recharging – extending its useful life.*

metal like the case is to keep the inevitable small amount of dc drift due to temperature change to a minimum.

The *7805* regulator was chosen so that it too could be clamped to the metal case. It is deliberately over-rated; However, I have used a *78L05* regulator with a metal clip-on heat sink as an alternative and this gives comparable results.

It is best to put a thermal barrier between the mains transformer and the rest of the circuit and to give this section its own ventilation path. A piece of Paxolin is satisfactory, as shown in **Fig.** 1. Some transformers on the market, of third world manufacture, get quite hot even when not under load, so plenty of ventilation slots are needed. When the lid is down, the heat from the transformer will not then warm up the rest of the charger.

Efficient ventilation can be achieved by mounting the transformer and cell holders on pillars and putting some ventilation slots directly underneath and above them. The holders must be of an open-frame design, such as RS 489-611, not the enclosed type like the Bulgin cylindrical series. I must emphasise that good ventilation is essential.

Although not mentioned in the first part of the article, the indicator led should be a low-current variety such as RS 826-515. If any difficulty is experienced getting $Tr_4$ to remain hard on, this indicator led can be removed and transferred to an emitter-follower attached to the comparator output. In addition, when charging D cells, with some low-gain specimens of *ZTX450* the value of $R_9$ may need to be reduced to keep $Tr_4$ hard on. Although it doesn't dissipate much power, this transistor should also have a clip-on heat sink to reduce the effects of thermal drift.

Also not shown in the first article, resistors $R_3$ and $R_{10}$ both need a trimming resistor in parallel to get a reasonable position on the preset pots for the balance point. To put the wiper within a reasonably central position, try values around 56kΩ. This method compensates for component tolerances and also avoids having to buy precise values for the resistive divider.

To make the preset pots more sensitive, you could try dropping the value to 470Ω and adjusting these trimmer resistors to suit.

If you use a tungsten lamp, as suggested, for showing how much current is passing, then the filament must be in direct view. It is no good covering it with a diffuser lens – you will not see any glow at low current. If the lamp holder has such a lens, remove it.

## Discharge timer – the missing link

Fitting a discharge timer to the battery-powered appliances is the key to successful alkaline-manganese recharging. The lack of a simple, cheap timer which can be easily fitted to appliances has held back the progress of commercially-available chargers. Results have been reported as generally disappointing. The reason is that in many cases the 30% limit cannot be easily estimated by the average member of the battery-using public.

It is not difficult to add a timer to appliances, where there is sufficient space. Although it is easy to find a small space in things like hand lanterns and portable radios, items such as battery shavers and the smaller hand-torches pose a problem.

The timer described here can be miniaturised if necessary by using an smd design. I have tried designing odd-shaped pcbs to fit around corners and into circular spaces. But what is really needed for use in small or densely-packed appliances is a purpose-built timer – a thick-film hybrid or asic.

The principle of the timer is very simple, Fig. 2. Oscillator A is driven in parallel with the load L – i.e. it only runs when the switch is on. It drives a multi-stage ripple counter C from which various outputs can be tapped to give a range of times. When the chosen output changes state, warning device D is turned on.

Note that, like the oscillator, D is powered only when the switch is on. It would most likely go unobserved if powered when the appliance is not switched on, possibly taking the battery beyond the 30% limit.

Counter C is maintained by being permanently connected to the battery during the time the batteries are in the appliance, but as it is a cmos device the drain is tiny – typical quiescent current is 5nA at 5V for the i.c. shown. For the vast majority of applications this can be ignored.

A practical version of this circuit is shown in Fig. 3. Timer $IC_1$ is a *555* which supplies a rough square-wave to $IC_2$, a *4020* binary ripple counter. There are 14 stages to $IC_2$, so the output from one of these is picked off to give a time suit the cell type and load current. At the end of the chosen time period the output goes high, Tr1 turns on, which powers the led.

The choice of timing components $R_1$ and $C_2$ for the *555* is dictated by the type of application so specific values are not shown, but this timer can be set for a few hours or up to a day or so. For longer periods, a second counter could be added or alternatively there are single ics available with even more stages.

Whenever the cells are replaced after charging, the reset button should be pressed to zero the count.

The *4020* works down to 3V. There are *555*-type timers which will work down to 2V, such as the *ICM7555IPA*. ■

## Charging NiCd cells

Because the charge currents for alkaline-manganese are by coincidence near the C/10 rate used for the equivalent sizes of NiCd cells, the charger described in last month's issue will also recharge these. As it uses periodic current reversal, the charger will do this job better than some commercially available chargers. Note that the end-of-charge cut-off will not operate if you charge NiCd cells.

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# Monitoring MAINS

**Nick Wheeler shows how to monitor mains current using a simply made current transformer.**

The traditional method of current measurement is to measure the voltage drop across a suitable series resistor. This is no good for monitoring the mains current, as a resistor giving reasonable sensitivity for the small always-on loads, such as timers and answering machines, would be far too large to cope with heavy, intermittent, heating loads, refrigerators and so on. The latter can come on at any time unless switched off, which would make measurements very tedious.

## The current transformer

Traditionally, current transformers comprise a secondary winding of many turns wound on a toroidal core. The primary is the conductor being monitored, which is passed through the central hole.

For increased sensitivity, the primary conductor can be threaded through the hole two or more times. This arrangement is fine for original installations, such as for motor control, but is unsuitable for retrospective domestic installation, as it means breaking the circuit, which stops all the clocks, etc, around the house.

There are 'clamp' meters, in which the core can be broken open against a powerful spring. With these the conductor can be encircled without disconnecting it. They are, however, costly. In any case I was also interested in current waveforms.

## Implementation

I used one of the small do-it-yourself transformer kits, which are available from many sources. These have a fully insulated mains winding, usually consisting of two 120V windings which can be connected in series or parallel. This forms the secondary of the current transformer.

The window provided for the d-i-y secondary in normal application is large enough to accommodate a single pass of the thick cable connecting the meter to the fuse box, usually easily accessible. The clamping plates which carry the mounting lugs will have to be sawn open at a suitable point and threaded over the cable, if required. I did not do this as provided the assembly bolts are applied after the laminations have been assembled the transformer can be reused for another purpose subsequently. The laminations are of the E & I form in all examples I have seen, and can be put in in stacks of five alternately.

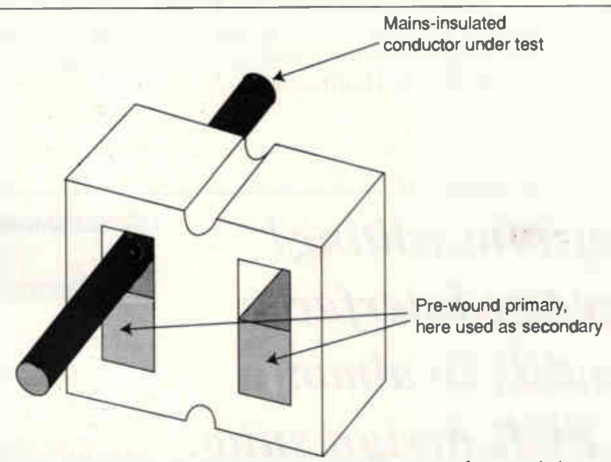



*Fig. 1. Using an off-the-shelf do-it-yourself mains transformer, it is possible to monitor mains current through a cable without the usual penalty incurred when investigating it via the voltage drop over a series resistor. The bobbin has been omitted for clarity. The grooves at top and bottom are for fixing bolts.*

**Figure 1** is a sketch of the assembly.

## Making measurements

A current transformer must always be operated with a secondary load. Otherwise a heavy current surge in the monitored conductor can induce very high voltages in the secondary – possibly leading to flashover and breakdown.

Calibration is carried out by connecting a heavy resistive load, such as a heater, via a shunt lead threading the core, as in Fig. 1. The current can be measured with a digital multimeter, and the secondary load adjusted to give a convenient voltage. The meter should be shorted until the heater is at operating temperature. Otherwise the cold surge may blow the meter fuse.

Values in the region of 1kΩ are suitable and will yield secondary voltages of the order of ten. Ordinary low-wattage resistors should be adequate.

Calibration is most conveniently done in the laboratory, even though this involves disassembling the transformer before final use.

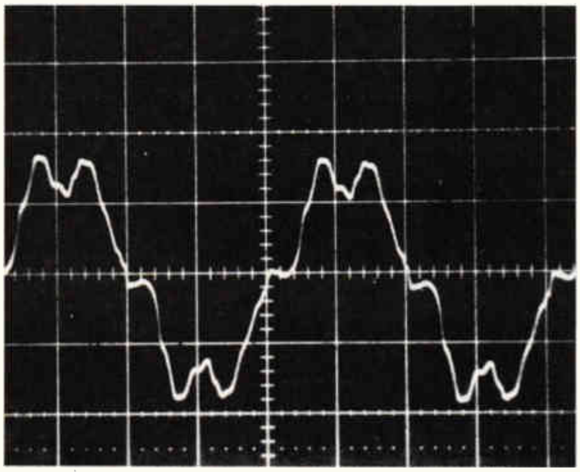


*Fig. 2. Mains current waveform resulting from 125μF across 240V mains. Current observed on a moving-coil meter was 9.7A.*

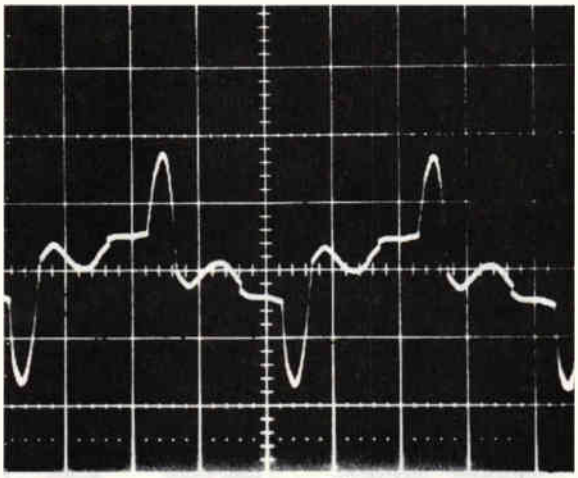


*Fig. 3. Current waveform resulting from a load of about 100VA in the form of two switch-mode power supplies.*

### Waveforms

Because the transformer is operated at far below the usual flux levels the observed waveforms across the load resistor can be assumed to be accurate. The voltage waveform across my mains is apparently a good sinusoid, with occasional transients. The current waveform through 125μF indicates that it is actually quite rich in harmonics, **Fig. 2.**

**Figure 3** was observed when my pc and my oscilloscope, both of which use switch-mode power supplies, were the main load. Horrible, isn't it?

### In summary

This article has shown that useful information about the quality of the mains signal, and current being drawn, can be obtained with little trouble or expense.

There is a small penalty, however. The secondary load of the current transformer appears as a tiny resistance in series with the power line. It is tiny, since it equates to the load resistance divided by the square of the transformer ratio. For 1kΩ and a ratio of 1000:1, values which are quite typical, insert a resistance of 1mΩ. ■

# Whose heterodyne?

**John Belrose and George Elliott set the record straight as to who invented the heterodyne.**

Professor Reginald Aubrey Fessenden

Tom O'Dell[1] recently surveyed the archives to find out where the real credit belongs for the birth of the heterodyne principle, which is the basis of nearly all radio receivers today. He attributes the coining of the word heterodyne to John Erskine-Murray. Tom's reference is the Oxford English Dictionary.

But Erskine-Murray is only a source reference. In the Appendix of his translation of Ernst Ruhmer's book on 'Radio Telephony', in a section detailing Fessenden's work, he states that "one of the most interesting of Professor Fessenden's many inventions is what he (Fessenden) calls the 'heterodyne' receiver..."[2]

Continuing, O'Dell concludes that while Fessenden's original patents (1050441 and 1050728 which we discuss below) describe the idea of producing a beat frequency, it is unlikely that his device(s) ever worked at radio frequencies. O'Dell attributes the "first successful" heterodyne receiver to Rudolf Goldschmidt, who devised a curious mechanical type of synchronous detection and heterodyning receiver in 1913.

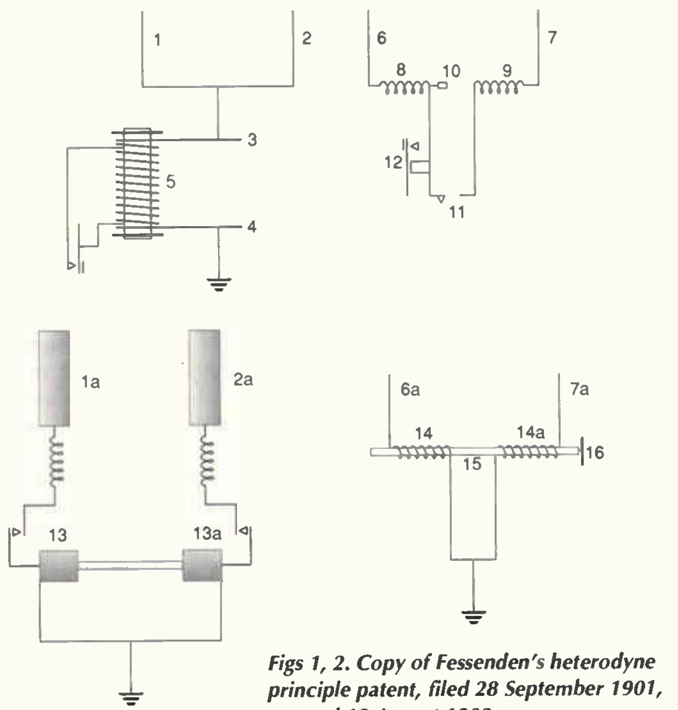
In our view O'Dell does not attribute proper credit to Reginald Aubrey Fessenden, the radio pioneer who invented radio as we know it today. He did indeed devise the heterodyne principle, as well as coining the word heterodyne. Below is our survey of Fessenden's contributions to the birth of the heterodyne principle.

## Fessenden's heterodyne principle

The Canadian/American radio pioneer and inventor Reginald Aubrey Fessenden (1866-1932) was granted almost 300 United States patents – most of them in telecommunications. His most notable invention was the heterodyne principle, which is fundamental to all radio today. Being trained in the classical languages, he coined the term —heterodyne— from two Greek words inferring the mixing of two forces.

The Fessendens were an old-line North American family having emigrated from Germany to Cambridge, Massachusetts Bay Colony, in about 1628. Reginald's family branch moved from the USA to what is now Quebec Province about the year 1800.

Born and educated in Canada, he moved permanently to the United States just prior to his 21st birthday, becoming an immediate US citizen. In 1921 he was awarded the Medal of




*Figs 1, 2. Copy of Fessenden's heterodyne principle patent, filed 28 September 1901, granted 12 August 1902.*

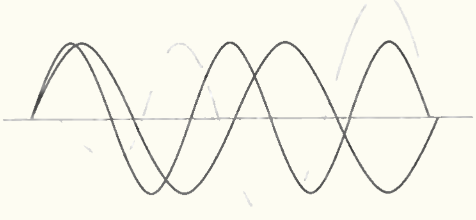


*Fig. 3. The solid sine waves illustrate phase relationship between incoming signals of different frequencies. Grey sine wave shows resulting beat frequency.*

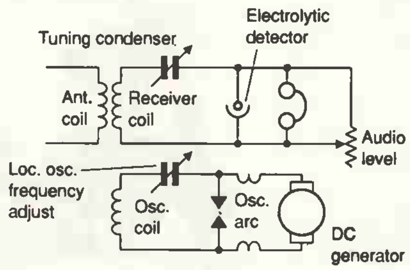



*Fig. 4. Sketch of Fessenden's advanced heterodyne receiver system.*

Honor of the Institute of Radio Engineers for his discovery of the heterodyne principle.

During the 1890's Fessenden considered the then standard wireless detector, the coherer, to be a severe obstacle to radio's long-term future. In effect he was saying the spark transmitter/coherer-detector communication system then in use must succumb to the efficiencies apparent in the continuous wave, or cw, method of wireless communication.

No such system was in sight in 1900, so Fessenden came up with methods to generate and receive cw. He devised a new type of detector – an electrolytic detector for rectifying and detecting cw signals; and the 'heterodyne principle', which led to cw wireless telegraphy, radio telephony and the many modes of telecommunications which we enjoy today.

The patent covering Fessenden's heterodyne principle was US No 706740, filed 28 September 1901 and granted 12 August 1902. Further related heterodyne method patents were US No 1050441, filed 27 July 1905 and granted 14 January 1913, and US No. 1050728.

The specification applicable to US No 706740 includes a continuous wave transmitting station emitting two different frequencies at the same time. The system also includes a receiver which combines the rf signals into a usable, single, audio-range frequency tone, suitable for the ear of the listener.

**Figures 1** and **2** – close likenesses of diagrams from Fessenden's original patent, granted 12 August 1902 – show his heterodyne transmitter and receiver. In Fig. 2, two high-frequency alternators, 13 and 13a are shown connected by a common drive shaft to permit rotation by a common drive source.

The alternators that Fessenden anticipated were to be in accordance with those specified in his patent application US No 62301, filed 29 May 1901. Alternator 13a was to be adjusted for a frequency output about 3% greater than alternator 13. The two transmitting antennas are shown as 1a and 2a, with 2a being tuned to a frequency about 3% greater than 1a.

In Fig. 2, the two receiving antennas 6a and 7a of the heterodyne receiver are tuned to the same frequencies as were transmitting antennas la and 2a. Detail 16 is an earphone diaphragm with a common iron-core 15. The received signals of different frequencies appear as voltages across earphone coils 14 and 14a. The result is a 'beat' frequency in the audible range, actuating diaphragm 16.

This is the arrangement that has been critically commented on by O'Dell. Whether this crude method worked efficiently is unimportant. Figure 2 represents Fessenden's cw transmitting and receiving system in its simplest form.

In **Fig. 3**, the solid sine waves illustrate the phase relationship between two incoming signals of different frequencies. The grey sine wave is meant to show the resultant beat frequency. Fessenden's 'heterodyne principle' was a brilliant conceptual discovery earning him a place in radio history even without his notable other inventions.

## Fessenden's heterodyne method

Remarkably, Fessenden was able to conceive the heterodyne principle without the wonders of the vacuum tube. He had to work with what was available at the turn of the century – in further development with the arc oscillator, the primitive detectors, the hf alternator, etc.

During 1902, Fessenden improved his heterodyne receiver by placing the second-frequency transmitter right at the location of the receiver site. The second signal was now under the control of the receiver operator, making the system easier to manage, **Fig. 4**. This led to his advanced heterodyne patent No 1050441.

The advanced heterodyne system was easily adjusted by the receiving site operator and did not involve the sending transmitter operator as did the initial version. Fessenden produced the locally generated frequency with an oscillating arc, or an alternator. Both these methods were in use until 1914/15 when the triode took over, but the arc was preferred.

In the words of Dr Sam Kintner[3], a member of the original Fessenden team, "This (the heterodyne principle) was another bold stroke of Fessenden, in which he departed from methods practiced by others. Like other great inventions, it was made before he had suitable equipment with which to practice it. He required a source of local oscillations of adjustable frequency, and an hf alternator or oscillating arc was all that was available.

"The term heterodyne was coined by (Prof.) Fessenden and has a technical meaning which may in general be explained as follows:

*If currents of two different frequencies 'beat' in the same circuit they will produce a new frequency and are said to heterodyne (from the Greek words, heteros – other or different, and dynamis – power) and the new frequency is called the heterodyne frequency. Further to simplify the matter: if frequencies being received are of such rapidity as to be beyond the human ear, such as 300kHz, in order to hear the 'heterodyne' one would generate in the receiving apparatus a frequency of 301kHz. The result of combining the two would be that the 'beat' note would equal the difference between the two or 1kHz which could easily be transformed into tones suitable for the ear of the listener. Mysterious and magical no doubt but scientific fact nevertheless.*

"Fessenden, who devised and named, the heterodyne system applied for a letters patent in 1905. His triumph was more theoretical then real for he was years ahead of the industry. His own cw apparatus was the only system capable of using the heterodyne system. Not until 1912 when the triode tube of DeForest became practicable for the general public did Fessenden's heterodyne invention assume its true importance in radio technology".

## But others used heterodyning too...

As radio moved onward after 1915, Fessenden's heterodyne patents became essential for all forms of wireless communications. Numerous lawsuits were fought in the US courts during the 1920's over the heterodyne patent rights.

Unfortunately, Fessenden did not receive any significant financial benefit from his patents. He lost control of the patents prior to 1911, through a series of legal manoeuvres by his partners and his lawyer. He was a first-class scientist, but an unwary business-man.

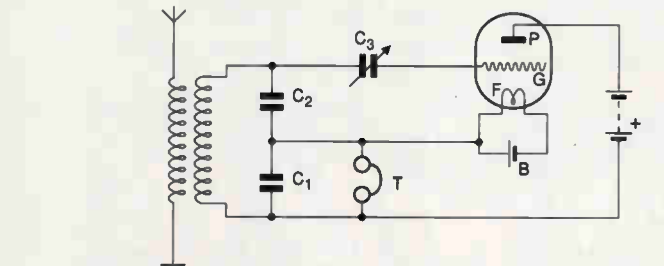
The following is a summation of one of these classic heterodyne US lawsuits. It was fought during 1924-25 and the plaintiff was the National Electric Signaling Company (NESCO) and the US Government was the defendant. The plaintiff, NESCO, sought to recover compensation for the unlicenced use of the Fessenden's heterodyne patents, by the

US government. Fessenden was a co-founder and an officer of NESCO but had been ejected from this firm by his partners, prior to 1911.

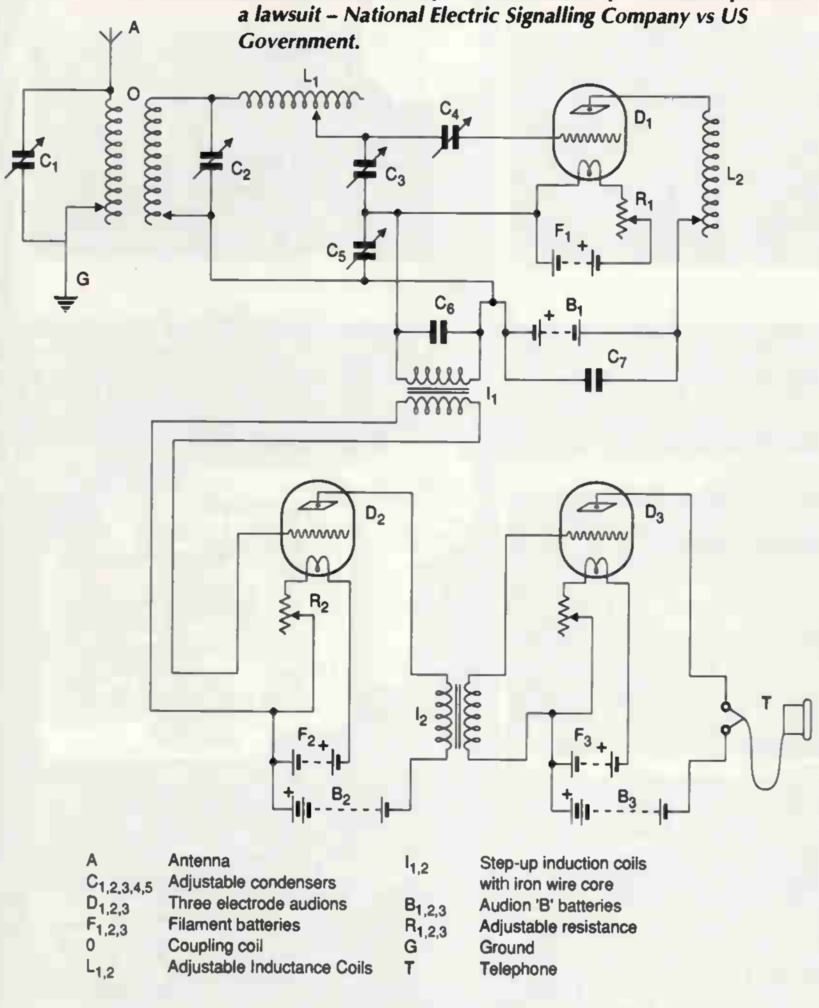
The plaintiff, NESCO, engaged the services of a number of expert witnesses, who became legends in the history of early American radio, to appear on their behalf. One of these witnesses was Haraden Pratt who was born in California in 1891. In his teens became an amateur radio operator. Before he was 21 years old he was employed by the United Wireless Telegraph Co. and the Marconi Company.

Pratt graduated from the University of California in 1914 as an electrical engineer. At various times during his years at the University he served as radio operator on a number of ships in the Pacific and at the Marconi port station at San Francisco. After graduation, Pratt was appointed 'assistant-engineer-for-construction' for Marconi Wireless at their Pacific high-power stations.

In 1915 he was placed in charge of the US Navy Radio Laboratory at Mare Island, California. In 1917, when the US entered WW 1, the US Navy assumed control of the US west coast commercial wireless stations and placed the maintenance of them under Pratt's laboratory. In 1918 he was transferred to Washington DC and placed in charge of the US Navy's high power radio stations.




***Figs 5 and 6. Copy of Fessenden's heterodyne based on sketches in Pratt's deposition, dated 7 April 1924, as part of a lawsuit – National Electric Signalling Company vs US Government.***




| | | | |
|---|---|---|---|
| A | Antenna | $I_{1,2}$ | Step-up induction coils with iron wire core |
| $C_{1,2,3,4,5}$ | Adjustable condensers | $B_{1,2,3}$ | Audion 'B' batteries |
| $D_{1,2,3}$ | Three electrode audions | $R_{1,2,3}$ | Adjustable resistance |
| $F_{1,2,3}$ | Filament batteries | G | Ground |
| 0 | Coupling coil | T | Telephone |
| $L_{1,2}$ | Adjustable Inductance Coils | | |

In December 1919, Pratt left the Navy and became Chief Engineer of the Federal Telegraph Company of California. This company operated commercial radio stations on the US west coast and in the Hawaiian Islands as well as designing and constructing high-power radio stations for the US Navy. Pratt's deposition in the NESCO *vs* US Government heterodyne lawsuit, is dated 7 April 1924 and was heard in a Pittsburgh PA courthouse.

Pratt testified he operated with a heterodyne receiver for the USN at Mare Island, California, copying traffic mainly from the Panama Canal Zone during the summer of 1915. This particular receiver had been made by Lee DeForest for the USN. He said he understood, in 1915, Fessenden's heterodyne principle to be – a "method of reception involving the generation locally at the receiver of a source of continuous electrical oscillations with such a frequency that an interaction will occur with the received high frequency current of the radio signal, due to association of local oscillatory means with the receiving set, which will produce beats which can be adjusted to be audible to the human ear".

Pratt testified he became aware of the existence of Fessenden's heterodyne principle following the USS SALEM heterodyne tests at sea in 1913. He said the use of the heterodyne system greatly extended the range of communication over that which would have been possible by the use of other means.

Pratt said **Fig. 5** was a fair, simplified representation of the Fessenden heterodyne receiving circuit used by the US Navy in the years 1917-18-19. This was a self-heterodyne set. Pratt was asked to explain the cause of the local oscillations, and how are they caused interaction with the received signal oscillating currents. His reply follows:

> *"The vacuum tube with its associated circuit generates an hf current in a coil, which is associated with the antenna circuit, so that this coil not only carries these hf currents but also those impressed upon it by the virtue of the current in the antenna system, due to the presence of the latter in the distant electrical field of the transmitting station being received. The two currents so impressed in this coil, being in the same circuit, combine when the adjustments are properly made, into an electrical current of which these two electrical currents are components. This new current has the necessary characteristics, which when rectified by a rectifying device, would produce an audible sound in the telephone receiver properly connected. The rectifying device in Figure 5 was incorporated in the same vacuum tube as was used to generate the local hf current, which is one of the other functions performed by this tube".*

## The heterodyne receiver comes into use

By mid 1913, the US Navy was convinced it had a unique cw communications system at hand with Fessenden's heterodyne receiver and the Federal oscillating arc transmitter. The USN's plan to dispense with the British Marconi, and the German Telefunken and Arco-Slaby systems was successful.

By March 1914 the vacuum tube method had been incorporated in Fessenden's reception method using the self-heterodyne circuit in which the detector and local oscillator are in the same tube envelope. In mid-1914, orders for these sets were placed by the USN with DeForest, Marconi, Wireless Specialties, etc. Fessenden and NESCO were not on the bidders list.

When the United States entered WW 1 the USN seized the huge German-owned commercial transmitting station at Sayville, NJ, where the USN immediately installed a Fessenden heterodyne principle receiver. It was a single-tube self-heterodyne set with two stages of audio amplification, **Fig. 6**.

The wisdom of the US Navy to move from 'spark' to cw wireless systems beginning in 1912-13 was significant. By 1918, high-power,Navy stations were in service at Annapolis, MD, Panama Canal, Philippines, Hawaii, France, San Diego, etc. These cw stations had Federal oscillating arc transmitters with power outputs from 100 to 1000kW, and employed Fessenden's heterodyne principle receivers.

The system was awe-inspiring, allowing the USN to communicate with its ships at any location on the high seas. This 1918 wireless cw communication network far surpassed what Britain, Germany, France or any other country could claim. Built in a relatively short five-year period, the US Navy system was much superior to the Marconi's 'spark' system.

### In summary

The Fessenden heterodyne patents, US Nos 706740, 1050441 and 1050729, cover a basic radio invention that is fundamental to signal reception. Some historians consider that Fessenden's heterodyne principle is his greatest contribution to radio science. It has been argued that both Armstrong (US) and DeForest (US) based their feedback regenerative detector patents on these Fessenden heterodyne patents. It is without question that both Armstrong and Levy (Fr.) incorporated Fessenden's heterodyne principle in their superheterodyne circuits, which are used today in all forms of telecommunications.

Through a series of corporate transactions, these Fessenden heterodyne patents came to be controlled by the Radio Corporation of America/General Electric Company. For years, those companies would not licence them for use by others. Fessenden did not receive any payment or fee from this 'radio trust'.

As the 1920's came to a close, this restraint-of-trade business method was judged illegal. As a side issue, Fessenden was awarded a relatively small compensatory sum by the US courts almost 30 years after filing his first heterodyne invention. After this legal settlement he left the United States forever, taking up residence in Bermuda where he passed away in 1932 at the age of 66 years.

Fessenden – a genius, and a mathematician – was the inventor of radio communications as we know it today[4,5].


### References

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# Message beacon

**Bill Francis' PIC-based wireless message system is kept simple by having pre-determined messages in eprom at the receiving end.**

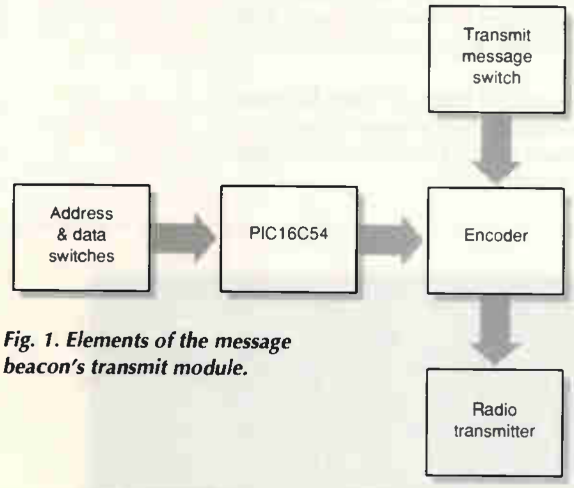


*Fig. 1. Elements of the message beacon's transmit module.*

On occasions, it is useful to have information conveyed to a number of display stations throughout a given area. In an office block, for example, it may be necessary to have a message display showing pricing information, periodically updated, in every room in the building.

The solution described here simplifies the task by storing pre-written messages in eprom within each remote display unit. It incorporates existing remote control ICs – namely the *M145026* and *27* – to translate receiver and message information.

The requirement here is for a message display system capable of displaying predetermined messages on one of several display units, all controlled from a central transmitter via a wireless link. The link is achieved using a uhf transmitter module and matching receiver, namely the *TXM-418-A* and *SILRX-418-A* respectively.

## Transmitting messages

Circuitry for the transmitter is relatively simple. **Figure 1** shows its block diagram. Control is carried out by a *16C54* PIC, programmed to read two switches connected to port B bits $PB_5$ and $PB_6$. Switch $SW_1$ is the 'address count'. When this switch is made, the PIC increments the address input to the *M145026* encoder up to a maximum of 31. Further increments cause the address count to 'roll over' to zero. The address identifies one of 31 receiver units.

In a similar way, $SW_2$ operates the 'data count' corresponding to the message to be displayed. The maximum value for the data count is 15. Again, any further increment causes the data count to roll over to zero.

The address and data values are output on the PIC port B bits $PB_0$ to $PB_4$ and port A respectively. These values are connected to the corresponding inputs of the *M145026* encoder and leds via inverters indicating the address and data values to the user. Passive components around the encoder set the IC's clock frequency to a relatively slow 8.53kHz.

Switch $SW_3$ is the transmit switch. When this switch is made, the IC outputs the code on its data out pin 15. Data output connects to the input of the radio transmitter module via comparator, $IC_5$, which provides a 12V logic level to the transmitter. Code is then transmitted.

A number of options are available in the choice of antenna. The one used here is a helical type, constructed from 34 turns of 0.5mm diameter enamelled copper wire close wound on a 2.5mm former. This gives the best compromise is terms of performance, ease of use and immunity to de-tuning. **Figure 2** is the circuit diagram.

The number of functions available on the transmitter is dictated by the software for the PIC microcontroller,

## PIC emulation on a shoe string

Developing a microcontroller-based system can be very expensive. For this design, a new PIC development system called *PIC-DATS* was used. This allowed the development investment, excluding that for the host pc, to be kept below £300 – and that price includes in-circuit emulation.

Capable of handling Microchip's *16C54, 55, 56, 57* and *84* microcontrollers, the unit interfaces to any pc compatible via the serial port. Interface software provided with the unit carries out a number of functions, all operating seamlessly. Programs are written via the user's own editor, such as MS-DOS EDIT. They are then assembled using Microchip's cross-assembler and debugged – all from within the same environment.

An add-on provides the facility to program the microcontroller when program development is complete. This add-on can also program the *16C71* and erase the *16C84* since it has electrically-erasable prom for both program and data.

One of the features of *PIC-DATS* is that PIC programs are simulated on the pc, but when the programs make reference to input and output, data is read and written to and from a 40-way connector on the development unit. This means that programs can be developed and debugged with real i/o.

Taking this a stage further, it is possible to connect the 40-way connector to a chip header that can be plugged into the PIC IC socket on a pcb under development. This means that the only difference between the *PIC-DATS* and a true in-circuit emulator is that the *PIC-DATS* cannot operate at true speed. Since the programs are simulated on the pc, the speed at which the program runs depends on the standard of pc being used.

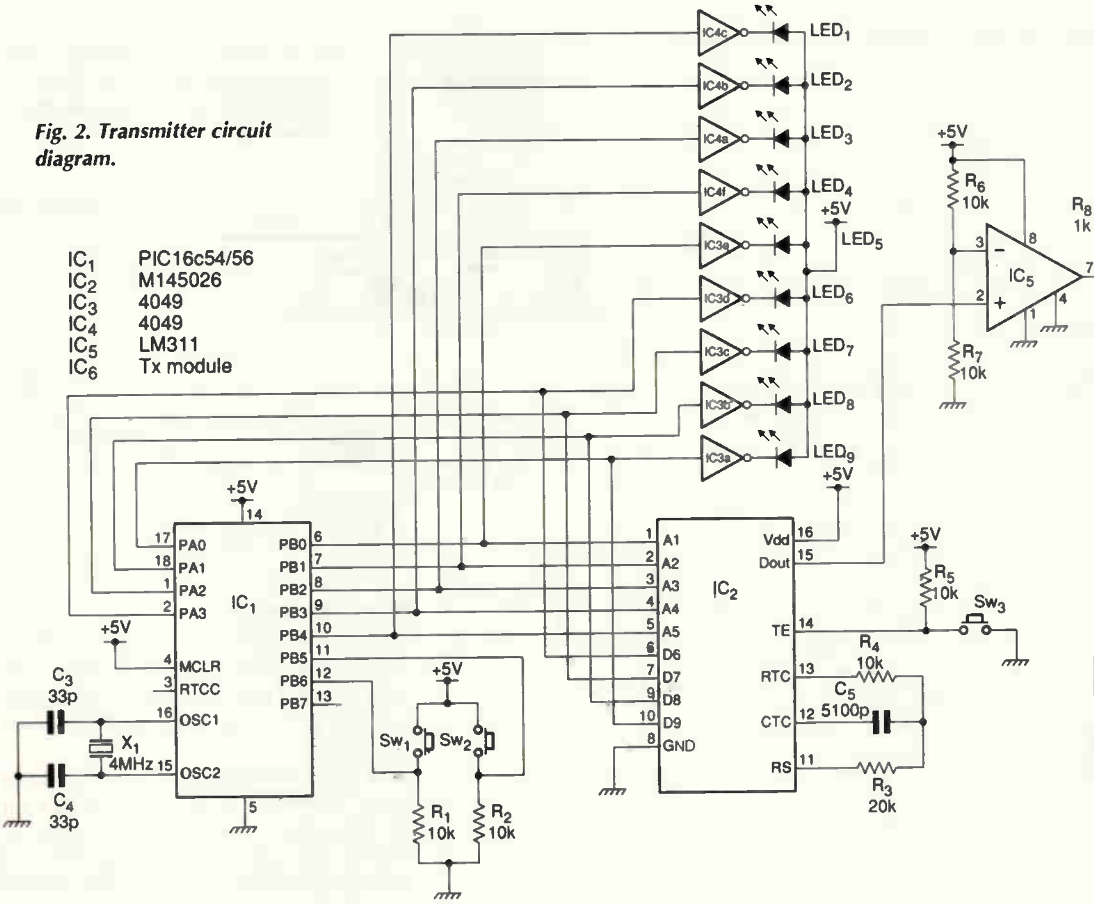
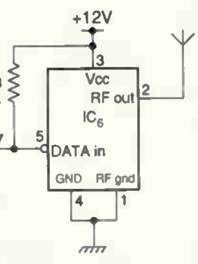


*Fig. 2. Transmitter circuit diagram.*

which is relatively simple. The program has two main functions. One is to read the address count switch, $SW_1$. If the switch is made, the address counter is incremented and the value is output on the appropriate port. The other is to read the data count switch, $SW_2$. If this switch is made, the data counter is incremented and the value is output on the appropriate port.

Using a PIC for the control functions reduces the chip count to one. If standard logic were used, the chip count could easily be four or five. This microcontroller approach makes pcb design much simpler and puts less demand on the power supply. It also gives more flexibility since the software can easily be modified.

## Transmitter software

Even the relatively simple program for the transmitter microcontroller requires some thought before coding is attempted. First, the individual functional blocks must be isolated. The functional blocks described here are:

- Microcontroller and variable initialisation
- Switch de-bounce
- Increment address count and output
- Increment data count and output

You may not need all of the blocks depending on your application. Remember that these are subroutines. A main control program is also required to coordinate the routines.

**Initialisation.** Usually, the microcontroller requires initialising only once. This is normally the first operation to be performed on power up.

The ports have to be set to input or output, or a combination of both, and the option register has to be initialised to set the real-time-clock, or rtc. In this case, the rtc is used on the internal clock and has the pre-scaler assigned to divide-by-256. This division is used in a delay routine for de-bouncing the switches.

Finally, the outputs will need to be set to their initial values and any variables, or file registers, initialised. The flow chart is shown in **Fig. 3** and the corresponding code is shown in the full listing under the label INITP.

**Switch de-bounce.** A simple delay routine debounces the switches. This delay is derived from the rtc, which is set to increment via its internal clock through a 256 pre-scaler. The rtc register is cleared then the program loops until bit 7 of the rtc is set. Further flow charts are not shown here, but the complete program listing is given in Fig. 3.

**Increment address counter.** When the increment address switch, $SW_1$, is made the UP_ADDRESS routine is called. The delay routine is called immediately, in order to de-bounce the switch. On return from the delay routine the switch is tested again. If it is not still made, the routine returns taking no action. This guards against spurious noise and spikes.

If the switch *is* still made, the address counter is incremented if the present value is less than 31, otherwise it is set to zero. The routine then waits until the switch is released and again is de-bounced by calling the delay routine. The address value is then output on the appropriate port.

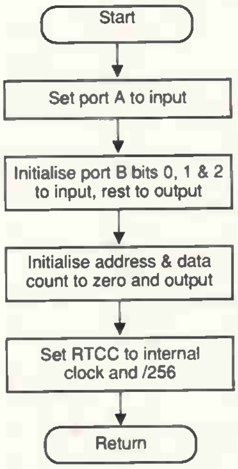


*Fig. 3. Transmitter software flow.*

**Increment data counter.** Operation of this routine is identical to that of the increment address counter with three exceptions: it reads increment data switch, $SW_2$, whose maximum value is 15, and the data is output to a different port.

## The control program

To begin with, the main or control calls the initialisation routine then enters a never ending loop, continually testing the two switches. If one of the switches is pressed, the program is directed to the appropriate routine as can be seen in the program listing.

When the program is complete, it requires testing. Using the *PIC-DATS* programmer (detailed later) allows each routine to be tested individually, first in simulation only, then, when necessary, using the in-circuit emulator cable in order to reflect real input and output.

Once the *PIC-DATS* is connected to the pc, and the associated software started, the user is presented with an information screen on the pc. The in-circuit emulator cable is then connected between the *PIC-DATS* unit and the PIC IC socket on the circuit board, **Fig. 4**. The assembled program is then loaded onto the programmer system allowing the user to run, trace or single step any part or all of the program.

*List 1. Transmit control subroutines. Routines are called when a switch is pressed.*

```
;########## EXP1.ASM ############################
;FILE SAVED AS              TXMOD.ASM
;FOR PIC 16C55              18 PIN DEVICE
;RESONATOR                  4MHz
;INSTRUCTION CLOCK          1.00 Mhz T= 1uS
;WATCHDOG                   DISABLED
;CODE PROTECTION            OFF
         PROCESSOR 16C54
         TITLE "Transmitter module program"
INCLUDE EQUATES.ASM
DATA     EQU      10H       ;IC DATA WORD
ADDRESS  EQU      11H       ;IC ADDRESS WORD
         ORG      1FFH      ;CHANGE ADDRESS DEPENDING ON PIC TYPE
RESET                       ;SEE RESET VECTOR SECTION
GOTO     START              ;THE PROGRAM STARTS HERE
; ********** THE ROUTINES START HERE *********
         ORG      00
START    CALL     INITP             ;INITIALISE PORTS
REPEAT   BTFSC    PORTB,6           ;TEST FOR UP ADDRESS
         CALL     UP_ADDRESS        ;IF ON INCREMENT ADDRESS
         BTFSC    PORTB,5           ;TEST FOR UP DATA
         CALL     UP_DATA           ;IF ON INCREMENT DATA
         GOTO     REPEAT            ;DO FOREVER
DELAY    CLRF     RTCC              ;SET DELAY
DEL_LOOP BTFSC    RTCC,6            ;TEST BIT 6
         GOTO     NEXT              ;IF SET JUMP TO MEXT
         GOTO     DEL_LOOP          ;ELSE JUMP TO DEL_LOOP
NEXT     RETLW    0                 ;RETURN
UP_ADDRESS
         CALL     DELAY     ;DEBOUNCE SWITCH
         BTFSS    PORTB,6           ;TEST IF STILL PRESSED
         GOTO     END_UP_ADDRESS    ;IF NOT PRESSED THEN DO NOTHING
WAIT_AS  BTFSC    PORTB,6           ;WAIT TILL SWITCH RELEASED
         GOTO     WAIT_AS           ;WAIT ADDRESS SWITCH
         CALL     DELAY             ;DEBOUNCE SWITCH RELEASE
         MOVLW    1                 ;SET W=1 FOR ADD
         ADDWF    ADDRESS           ;ADDRESS:=ADDRESS+1
         BTFSC    ADDRESS,5         ;TEST IF > 31
         GOTO     ADDRESS_ZERO      ;IF > 31 SET TO ZERO
CONT_ADDRESS
         MOVF     ADDRESS,W         ;GET ADDRESS
         MOVWF    PORTB             ;AND OUTPUT
END_UP_ADDRESS
         RETLW    0                 ;RETURN
ADDRESS_ZERO
         CLRF     ADDRESS           ;SET ADDRESS TO 0
         GOTO     CONT_ADDRESS      ;AND CONTINUE
UP_DATA
         CALL     DELAY             ;DEBOUNCE SWITCH
         BTFSS    PORTB,5           ;TEST IF STILL PRESSED
         GOTO     END_UP_DATA       ;IF NOT PRESSED THEN DO NOTHING
WAIT_DS  BTFSC    PORTB,5           ;WAIT TILL SWITCH RELEASED
         GOTO     WAIT_DS           ;WAIT DATA SWITCH
         CALL     DELAY             ;DEBOUNCE SWITCH RELEASE
         MOVLW    1                 ;SET W=1 FOR ADD
         ADDWF    DATA              ;DATA:=DATA+1
         BTFSC    DATA,4            ;TEST IF > 15
         GOTO     DATA_ZERO         ;IF > 15 SET TO ZERO
CONT_DATA
         MOVF     DATA,W            ;GET DATA
         MOVWF    PORTA             ;AND OUTPUT
END_UP_DATA
         RETLW    0                 ;RETURN
DATA_ZERO
         CLRF     DATA              ;SET DATA TO 0
         GOTO     CONT_DATA         ;AND CONTINUE
         RETLW    0                 ;RETURN
INITP    MOVLW    0                 ;MAKE PORT A OUTPUT
         TRIS     PORTA             ;DO IT
         MOVLW    #0E0H             ;PORT B BITS 7, 6 & 5 INPUT, REST OUT
         TRIS     PORTB             ;DO IT
         MOVLW    0                 ;CLEAR W
         MOVWF    DATA              ;DATA = 0
         MOVWF    ADDRESS           ;ADDRESS = 0
         MOVWF    PORTA
         MOVWF    PORTB
         MOVLW    7                 ;SET RTCC PRE-SCALER = 256
         OPTION                     ;DO IT
         RETLW    0                 ;RETURN
         END
```

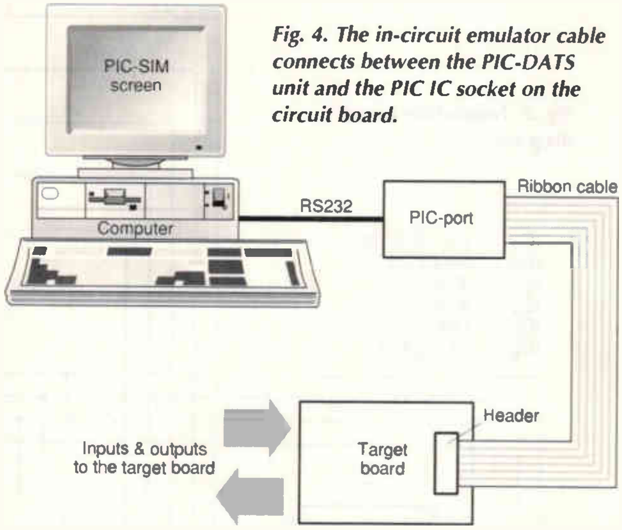


*Fig. 4. The in-circuit emulator cable connects between the PIC-DATS unit and the PIC IC socket on the circuit board.*

The *PIC-DATS* system is menu driven so operation is largely intuitive. For example, to single-step the main program, simply select the 'debug' pull down menu using the keyboard or mouse, select single step and press enter. The user is then prompted for a start address, 'R' specifies the reset address, and reset condition.

Subsequent single steps are then executed by pressing the return or 'S' key. This continues until any other key is pressed. The last line of code executed is shown on the user screen and the next line to be executed is shown in the top right-hand corner of the user screen.

As single stepping continues, the values read from the switches are 'real' values and can be seen in the appropriate file register .In the *PIC-DATS* system, if the program is found to perform incorrectly, it can be edited, cross-assembled and reloaded, all from within the programmer system. This allows rapid program development.

## Receiver details

Messages for displaying by the receiver are stored in an eprom. The content of the actual messages will vary depending on the particular application. Programming of the eprom is up to you.

As a guide, the messages for the eprom used in the development unit were written on a microprocessor cross-assembler using the 'define message' assembler directive. The eprom was then programmed. The maximum length of the message in this application is 127 characters, which is adequate for most liquid-crystal display modules.

The PIC is not designed for interfacing to external memory, but an eprom can be interfaced using the PIC's i/o ports. This approach does, however, require that data transfers are performed under program control. Addressing the eprom and retrieving the data involves 8 data lines and 11 address lines.

The PIC used in the receiver is the *16C55* which has 20 programmable i/o pins. Clearly, some sharing of i/o resources is needed. To accomplish this, part of the eprom address is latched using a *74LS374* octal data latch. In effect, a bus system is created. This bus uses port C of the PIC to transfer data and bits 0-2 and 4-7 of port B to control the data transfers, **Fig. 5**. A block diagram of the receive and decode section is shown in **Fig. 6**.

## Software and circuit operation

The radio receiver module receives the encoded transmission and passes the digital data to the input of the *M145027* decoder. If the transmitted address matches the address set up on the address select switches, the decoder issues a valid transmission, VT, signal and outputs the transmitted code.

This allows up to 32 receiver modules to be used individually with one transmitter unit. The VT signal connects to port B bit 3 of the PIC which, under program control, waits till the VT signal goes active low.

When the PIC receives an active VT, again under program control, the PIC reads the code from the decoder via port A. This code is then used as the upper four bits of the eprom address thus forming the 'base address' of the message to be displayed. In order to display the message the PIC must perform the following actions:

- The base address – the code received – must be output on address lines $A_{7\text{-}10}$ ($A_{8\text{-}10}$ via port B bits 0-2, and $A_7$ latched from port C, bit 7).
- Lower order address lines are set to zero and latched on to $A_{0\text{-}6}$ of the eprom. Data is read from the eprom. If the data is zero, the processes is ended (null terminating string).
- The data is written to the lcd module.
- The address is incremented.
- Go to step 2.

As mentioned in the description of the transmitter, each operation must be isolated and coded individually. The receiver module is more complex than the transmitter unit so great care must be exercised in isolating and developing each operation, or sub-routine.

When a particular solution is developed, it is important that its operation is tested as much as possible before moving to the next task. This can be achieved using the *PIC-DATS* unit since it is possible to run each subroutine using the in-cable and monitor the various signals on the receiver unit as the routine is stepped through. Here, the following individual requirements were isolated:

- Initialise PIC
- Delay
- Wait for 'not busy' from lcd module
- Write data to lcd module
- Clear lcd module
- Initialise lcd module
- Clock address latch
- Read eprom
- Main control routine

The program listing shows that each one of the above operations corresponds to a subroutine. As the programs are developed, each subroutine is tested as a self contained item. When the routine operation is acceptable, that routine is used as required within a program. This is the best way to develop.

**Initialising the PIC.** Initialisation of the PIC divides in to two parts – the operation of the ports and the OPTION register. The ports are set to input or output and assigned an initial value as indicated in **Table 1**.

In this case, the OPTION register is used to set the prescaler to 256 and assign it to the rtc with internal clock. The routine performing these operations can be seen in the program listing under the name INITP.

**Delay.** The delay routine is a general purpose delay for use by other routines. It is similar to that described in the transmitter section of this project and therefore will not be further described here.

**Wait for not busy from lcd module.** The lcd module control signals are interfaced as indicated in Table 1. Port C is used as the data bus while the three control bit are derived from port B and have functions as shown in **Table 2**.

The lcd module carries out commands internally following a command instruction. While the command is being executed, no further commands or data may be written to the module. The display module uses the 'Busy' signal to indicate the current status of the device and is accessed by performing a read cycle and examin-

*List 2. Routines for the PIC-controlled message receiver module.*

```
;########## RXMOD.ASM ##############################
;FOR PIC 16C55               28 PIN DEVICE
;RESONATOR                   4MHz
;INSTRUCTION CLOCK           4.00 MHz T= 1uS
;WATCHDOG                    DISABLED
;CODE PROTECTION             OFF
          PROCESSOR 16C55
          TITLE "Receiver module program"
INCLUDE EQUATES.ASM
LCD_EN    EQU      7H        ;LCD ENABLE BIT
LCD_WR    EQU      6         ;LCD W/notW BIT
LCD_RS    EQU      5         ;LCD REG SEL BIT (SAME AS LATCH EN)
LATCH_EN EQU       5         ;LATCH ENABLE ACTIVE HIGH
EPROM_OE EQU       4         ;EPROM OUTPUT ENABLE ACTIVE LOW
VT        EQU      3         ;VALID TRANSMIT BIT
EPROM_DATA         EQU      11H       ;STORE FOR EPROM DATA
MESSAGE_CODE       EQU      12H       ;STORE FOR RECEIVED CODE
ADDRESS            EQU      13H       ;STORE FOR ADDRESS
                   ORG      1FFH      ;RESET ADDRESS
RESET                                 ;RESET VECTOR
GOTO               START              ;PROGRAM START
;********** THE ROUTINES START HERE *********
          ORG      00
START     CALL     INITP              ;INITIALISE PORTS
          CALL     DELAY              ;ALLOW POWER UP TIME
          CALL     INIT_LCD           ;RESET LCD MODULE
REPEAT    BTFSS    PORTB,VT           ;TEST VALID TRANSMIT BIT
          GOTO     REPEAT             ;AND WAIT TILL NOT VALID
WAIT_VT_VALID
          BTFSC    PORTB,VT           ;TEST VALID TRANSMIT BIT
          GOTO     VALID_TX           ;RECEIVED A TRANSMISSION!
          GOTO     WAIT_VT_VALID      ;WAIT FOR VALID TRAN
;**********SUBROUTINES****************************
;************DELAY********************************
DELAY     CLRF     RTCC               ;SET DELAY
DEL_LOOP BTFSC     RTCC,7             ;TEST BIT 7
          GOTO     NEXT               ;IF SET JUMP TO MEXT
          GOTO     DEL_LOOP           ;ELSE JUMP TO DEL_LOOP
NEXT      RETLW    0                  ;RETURN
;***********WAIT FOR NOT BUSY BIT*******************
WAIT_BF   MOVLW    #0FFH              ;SET PORT C TO INPUT
          TRIS     PORTC              ;DO IT
          BSF      PORTB,LCD_WR       ;SET READ
          BSF      PORTB,LCD_EN       ;ENABLE LCD
WAIT_BF1 BTFSS     PORTC,PB7          ;TEST BF
          GOTO     BF_GONE            ;IF 0, LCD MOD NOT BUSY
          GOTO     WAIT_BF1           ;ELSE TRY AGAIN
BF_GONE   BCF      PORTB,LCD_EN       ;DISABLE LCD MOD
          BCF      PORTB,LCD_WR       ;PUT BACK TO WRITE
          MOVLW    #0                 ;SET PORT C BACK TO OUTPUT
          TRIS     PORTC              ;DO IT
          RETLW    0                  ;RETURN
;********WRITE CHARACTER TO LCD MODULE FROM LOC'N EPROM_DATA *******
WRITE_LCD          CALL     WAIT_BF   ;WAIT TILL FREE (ALSO SET C TO O/P)
          MOVF     EPROM_DATA,W       ;GET DATA
          MOVWF    PORTC              ;AND O/P
          BSF      PORTB,LCD_RS       ;SELECT DATA REG
          BSF      PORTB,LCD_EN       ;ENABLE LCD MOD
          BCF      PORTB,LCD_EN       ;& CLOCK
          BCF      PORTB,LCD_RS       ;RESTORE INIT COND
          MOVLW    #0FFH              ;SET PORT C BACK TO I/P
          TRIS     PORTC              ;DO IT
          RETLW    0                  ;& RETURN
;*********INIT LCD MODULE****************************
INIT_LCD MOVLW     0                  ;SET PORT C TO O/P
          TRIS     PORTC              ;DO IT
          MOVLW    #38H               ;SET COMMAND
          MOVWF    PORTC              ;& OUTPUT TO PORT C
          BSF      PORTB,LCD_EN       ;ENABLE LCD MOD
          BCF      PORTB,LCD_EN       ;& CLOCK
          CALL     DELAY              ;WAIT
          BSF      PORTB,LCD_EN       ;ENABLE LCD MOD 2ND TIME
          BCF      PORTB,LCD_EN       ;& CLOCK
          CALL     DELAY              ;WAIT
          BSF      PORTB,LCD_EN       ;ENABLE LCD MOD 3RD TIME
          BCF      PORTB,LCD_EN       ;& CLOCK
          CALL     DELAY              ;WAIT
          MOVLW    #38H               ;FUNCTION SET
          MOVWF    PORTC              ;O/P IT
          BSF      PORTB,LCD_EN       ;ENABLE LCD MOD
          BCF      PORTB,LCD_EN       ;& CLOCK
          CALL     DELAY
          MOVLW    #8                 ;DISPLAY OFF
          MOVWF    PORTC              ;O/P IT
          BSF      PORTB,LCD_EN       ;ENABLE LCD MOD
          BCF      PORTB,LCD_EN       ;& CLOCK
          CALL     WAIT_BF
          MOVLW    #1                 ;DISPLAY ON & CLEAR
          MOVWF    PORTC              ;O/P IT
          BSF      PORTB,LCD_EN       ;ENABLE LCD
          BCF      PORTB,LCD_EN       ;& CLOCK
          CALL     WAIT_BF
          MOVLW    06H                ;ENTRY MODE
          BSF      PORTB,LCD_EN       ;ENABLE LCD
          BCF      PORTB,LCD_EN    ;& CLOCK
          CALL     WAIT_BF
SET_LCD   MOVLW    0                  ;SET PORT C TO O/P
          TRIS     PORTC              ;DO IT
          MOVLW    #38H               ;FUNCTION
SET
```

*Continued over page*

```
          MOVWF    PORTC                ;O/P IT
          BSF      PORTB,LCD_EN         ;ENABLE LCD MOD
          BCF      PORTB,LCD_EN         ;& CLOCK
          CALL     WAIT_BF
          MOVLW    #0EH                 ;DISPLAY ON
          MOVWF    PORTC                ;O/P IT
          BSF      PORTB,LCD_EN         ;ENABLE LCD MOD
          BCF      PORTB,LCD_EN         ;& CLOCK
          CALL     WAIT_BF
          MOVLW    #6H                  ;ENTRY MODE SET
          MOVWF    PORTC                ;O/P IT
          BSF      PORTB,LCD_EN         ;ENABLE LCD MOD
          BCF      PORTB,LCD_EN         ;& CLOCK
          CALL     WAIT_BF
          MOVLW    #1H                  ;CLEAR DISPLAY
          MOVWF    PORTC                ;O/P IT
          BSF      PORTB,LCD_EN         ;ENABLE LCD MOD
          BCF      PORTB,LCD_EN         ;& CLOCK
          CALL     WAIT_BF
          MOVLW    #0H                  ;
          MOVWF    PORTC                ;O/P IT
          BSF      PORTB,LCD_EN         ;ENABLE LCD MOD
          BCF      PORTB,LCD_EN         ;& CLOCK
          MOVLW    #0FFH                ;SET PORT C BACK TO
INPUT
          TRIS     PORTC                ;DO IT
          RETLW    0                    ;RETURN
;********GO TO NEXT LINE (LINE 2)*********************
LINE_2    CALL     WAIT_BF              ;WAIT FOR NOT BUSY,(SET
C TO O/P)
          MOVLW    #0C0H                ;SET DD RAM TO 40 (LINE
2)
          MOVWF    PORTC                ;O/P IT
          BSF      PORTB,LCD_EN         ;ENABLE LCD MOD
          BCF      PORTB,LCD_EN         ;& CLOCK
          MOVLW    #0FF                 ;SET PORT C TO INPUT
          TRIS     PORTC                ;DO IT
          RETLW    0                    ;RETURN
;*****CLOCK LATCH DATA TO EPROM LATCH*****************
CLOCK_LATCH_DATA
          CLRW                          ;SET PORT C TO OUTPUT
          TRIS     PORTC                ;DO IT
          MOVF     ADDRESS,W            ;GET DATA TO LATCH
          MOVWF    PORTC                ;AND OUTPUT
          BSF      PORTB,LATCH_EN       ;CLOCK LATCH
          BCF      PORTB,LATCH_EN       ;
          MOVLW    #0FFH                ;SET PORT C TO INPUT
          TRIS     PORTC                ;DO IT
          RETLW    0                    ;RETURN
;***********READ_EPROM AND STORE DATA**********************
READ_EPROM          BCF      PORTB,EPROM_OE    ;EPROM OUTPUT ENABLE
          NOP                           ;WAIT
          MOVF     PORTC,W              ;READ DATA
          MOVWF    EPROM_DATA           ;AND STORE
          BSF      PORTB,EPROM_OE       ;DISABLE EPROM OUTPUT
          RETLW    0                    ;AND RETURN
;*********INITIALISE I/O**************************
INITP     CLRF     PORTC                ;PORT C = 0
          CLRF     PORTA                ;PORT A = 0
          CLRF     PORTB                ;PORT B = 0
          MOVLW    #0FFH                ;MAKE PORT A INPUT
          TRIS     PORTA                ;DO IT
          MOVLW    #08H                 ;PORT B BIT 3 INPUT,REST OUT
          TRIS     PORTB                ;DO IT
          MOVLW    #10H                 ;INIT PORT B
          MOVWF    PORTB                ;DO IT
          MOVLW    #0FFH                ;SET PORT C TO INPUT
          TRIS     PORTC                ;DO IT
          MOVLW    #7                   ;SET RTCC DIVIDE FACTOR
          OPTION                        ;DO IT
          RETLW    0                    ;RETURN
;***********MAIN CONTROL ROUTINES
VALID_TX                                ;GOT A TRANSMISSION
          CALL     SET_LCD              ;INITIALISE LCD MODULE
          MOVF     PORTA,W              ;READ MESSAGE CODE
            MOVWF  MESSAGE_CODE         ;AND STORE
;SET UP ADDRESS
            CLRF   ADDRESS              ;SET ADDRESS TO ZERO
            BTFSC  PORTA,W              ;TEST LSB OF CODE
            BSF    ADDRESS,7            ;IF SET, SET MSB OF ADDRESS
            RRF    MESSAGE_CODE         ;MOVE CODE 1 TO RIGHT
NEXT_CHAR CALL     CLOCK_LATCH_DATA     ;LATCH ADDRESS ONTO EPROM
            MOVLW  #0F8                 ;CLEAR BASE ADDRESS BITS
            ANDWF  PORTB                ;DO IT
            MOVF   MESSAGE_CODE,W       ;GET BASE ADDRESS
            IORWF  PORTB                ;SET UP 3 LSB'S LEAVING OTHER BITS
            CALL   READ_EPROM           ;READ EPROM DATA..DATA IN EPROM_DATA
;TEST FOR ZERO (EOL)
            MOVF   EPROM_DATA,W         ;RETRIEVE DATA
            IORLW  #0                   ;TEST FOR ZERO
            BTFSC  STATUS,ZERO          ;IF NOT ZERO CARRY ON
            GOTO   REPEAT               ;ELSE END
            MOVLW  #1                   ;SET UP INCREMENT
            ADDWF  ADDRESS              ;INCREMENT ADDRESS
            MOVLW  #10H                 ;TEST FOR END OF LINE 1
            SUBWF  EPROM_DATA,W         ;
            BTFSC  STATUS,ZERO          ;IF NOT LINE TO SKIP
            GOTO   NEW_LINE             ;ELSE NEW LINE
            CALL   WRITE_LCD            ;ELSE WRITE DATA TO LCD
            GOTO   NEXT_CHAR            ;DO NEXT
NEW_LINE    CALL   LINE_2               ;GO TO LINE 2
            GOTO   NEXT_CHAR            ;AND CONTINUE
            END
```

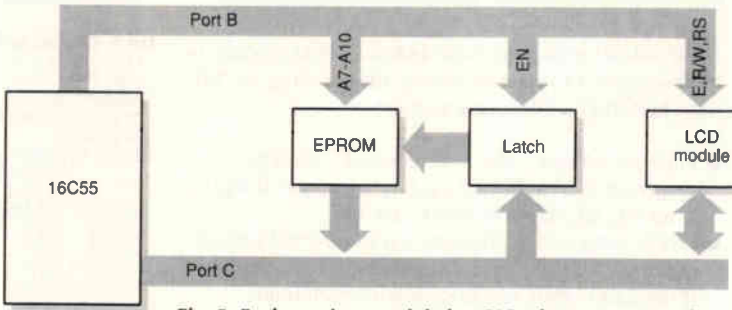


*Fig. 5. Each receiver module has PIC whose ports B and C are used as control, address and data buses for the message eprom and display. The latch allows the eprom address range to be extended.*

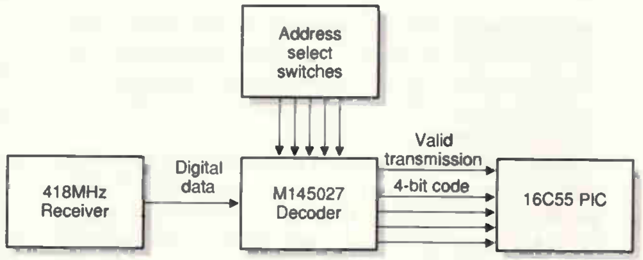


*Fig. 6. Overall system diagram of the receiver module shows how the low-power radio receiver feeds the decoder module, which in turn sends the received information to the PIC.*

ing the state of bit 7 – the busy signal. If the busy signal is high, then an internal operation is in progress and no further information may be written to the device.

**Wait for not busy.** This routine performs the following sequence:

Port C is made input.
The lcd module is set to 'read' by setting the R/W bit and enabled by setting the enable bit.
The data bus – port C of the PIC – is then read and bit 7 tested.
If Bit 7 is a logic 1, step 3 is repeated.
The read and enable bits are cleared.
Port C put back to output.

The routine associated with this process can be seen in the program listing under the label 'WAIT_BF'. As it's name suggests, this subroutine cycles waiting till the lcd module is not busy before a return is executed.

**Write data to lcd module.** This routine writes data held in a file register, named EPROM_DATA, to the lcd module. In this application, the data is the data previously retrieved from the eprom and stored by the READ_EPROM routine, described later. The write operation is accomplished by performing the following steps:

Call the WAIT_BF routine. This makes sure that the lcd module is ready to receive data. Note also that port C is left as output.
Data held in register file EPROM_DATA is retrieved, placed it in the W register, and output it to port C, which is connected to the data pins of the lcd module.
Set the RS bit of the lcd module to logic 1 to select data, and enable the lcd module by placing a logic zero on the enable pin.
Clock data into the lcd module by clearing the enable bit followed by disabling the lcd module.
Set port C to input.

*Table 1. Port allocation table for the message receiver module.*

| Device | Port A A3 | A2 | A1 | A0 | Port B B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Port C C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Decoder | D9 | D8 | D7 | D6 | | | | | VT | | | | | | | | | | | |
| Eprom | | | | | | | | OE | | A10 | A9 | A8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Display | | | | | EN | R/W | RS | | | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Latch | | | | | | | EN | | | | | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Input/output | I | I | I | I | O | O | O | O | I | O | O | O | I/O | I/O | I/O | i/o | I/O | I/O | I/O | I/O |
| Initial i/o | I | I | I | I | O | O | O | O | I | O | O | O | I | I | I | I | I | I | I | I |
| Initial Value | x | x | x | x | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x |

*Table 2. Control bits used for the liquid crystal display module.*

| Level | Port B bit 5 RS | bit 6 R/W | bit 7 E |
|---|---|---|---|
| 0 | Inst. i/p | Read | Disable |
| 1 | Data input | Write | Enable |

*Table 3. Command order for the liquid crystal display.*

| Command order | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| Code | $38_{16}$ | $38_{16}$ | $38_{16}$ | $38_{16}$ | 8 | 1 | 6 |

To use this routine, the control program has to send display data to the lcd module in the appropriate register file. In this case register file $11_{16}$ equates to the label EPROM_DATA.

Note that the name chosen, WRITE_LCD, is meaningful. This makes programs more easily understood and hence easier to debug and maintain, see **List 2**.

**Initialise lcd module.** This routine is essentially writes a series of commands to the lcd module as detailed by the lcd module specification – in this case the Hitachi *LM032L*. A command is written to the lcd module by performing the following steps:

Set port C to output and send the appropriate command code.

The device is enabled by setting the enable bit and the command clocked in by clearing the enable bit. Note that the RS bit is left in the default condition, logic 0, which selects the command mode.

Wait until command complete. Note that the wait for not busy cannot be used until the device is initialised.

This process is repeated with the appropriate command codes, with a call a delay routine between successive commands. The command code sequence used in this instance is shown in **Table 3**.

Referring to List 2, he name used for the routine is INIT_LCD. Notice also that the last four code sequence can be called by calling the SET_LCD routine which is in fact part of the INIT_LCD routine. The SET_INIT routine is used when the lcd module has previously been initialised but the operation requires modifying, or as in this case clearing and the cursor moved to the beginning of line one.

**Clock address latch.** Before the eprom data can be retrieved the correct address must be

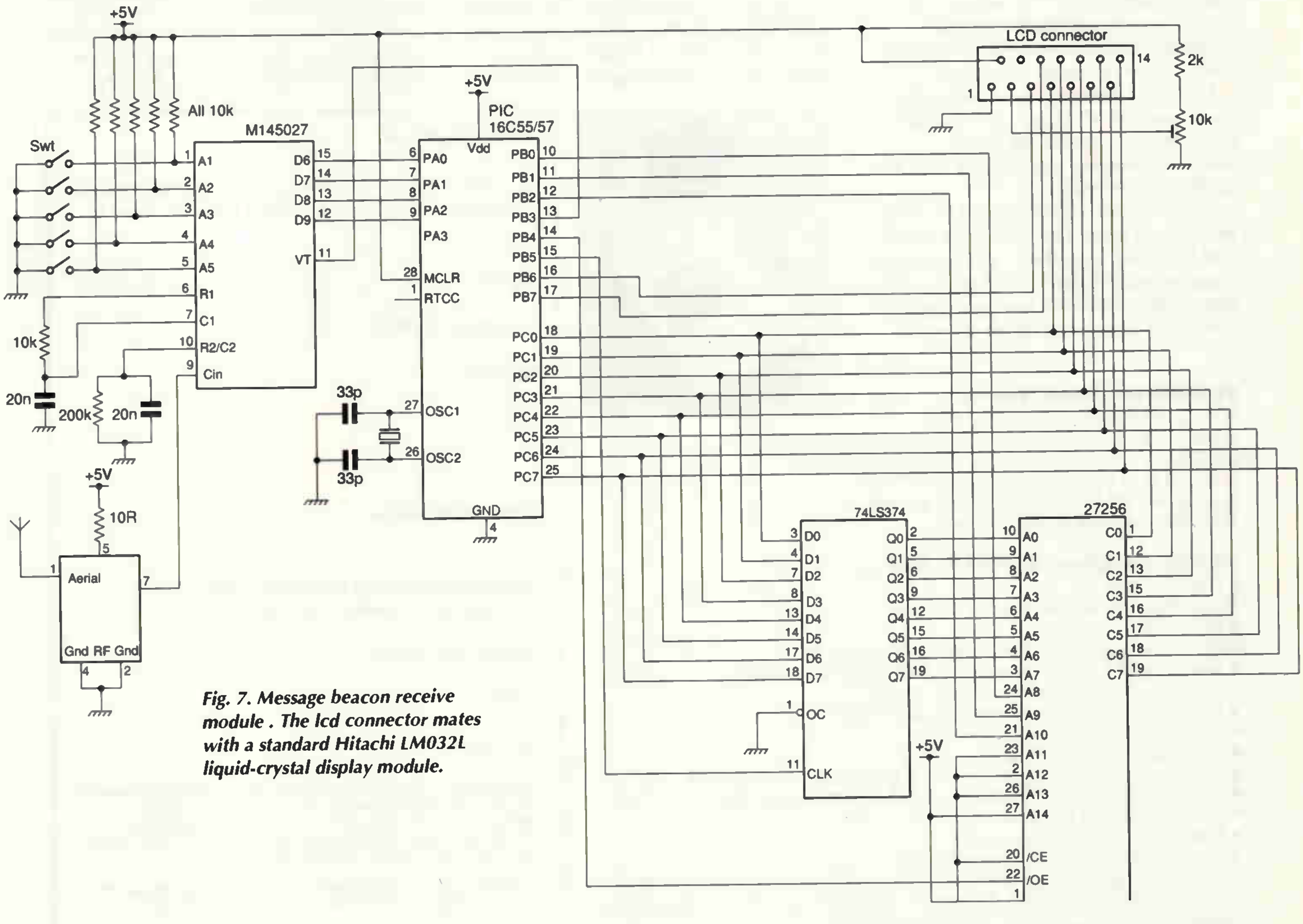


*Fig. 7. Message beacon receive module . The lcd connector mates with a standard Hitachi LM032L liquid-crystal display module.*

applied to the address lines, this is achieved by latching the address into the address latch. The required sequence is as follows:

Set port C to output.
Retrieve current address and send to port C.
Set then clear latch enable bit to clock latch. This bit is port B bit 5, called LATCH_EN.
Restore port C to input.

In the program listing, this subroutine is called 'CLOCK_LATCH_DATA'.

**Read eprom data.** In normal operation data is read from eprom automatically when a microprocessor performs a read operation. All the control signals are provided by the microprocessor. In this case the data transfer must be performed under program control by producing the following sequence:

Enable the eprom outputs by clearing the output enable which is connected to port B bit 4, labelled LATCH_EN.
Read port C which now has the EPROM data applied.
Disable the EPROM outputs by setting the output enable high.

This sequence is carried out by the READ_EPROM routine in the program listing. The main program simply calls each subroutine as required. One facility not mentioned so far is the ability to include a new line control within the stored message. The line-feed code $10_{10}$ is used to indicate that the cursor on the lcd module should be moved to the start of line two. As each code is read from the eprom, it is tested for a new line. If a new line is required the subroutine LINE_2 is called.

## Circuit details

The complete circuit diagram is shown in **Fig. 7**. Note the way port C of the PIC is used as a bus system. Each device on the bus is capable of being tri-state which allows each device to be selected under program control. It should be apparent that it is very important that programmer is especially careful to enable only one device at a time to avoid bus conflict.

The receiver is tested using the same approach as the transmitter, each routine tested and proved individually using the *PIC-DATS* with or without the in-circuit emulator cable, then the program is tested as a whole.

As the program is traced – or run – and with the optional in-circuit emulator cable fitted, each character of the message can be seen as it is transferred from the eprom to the lcd module. The process is complete by programming the PIC, probably a one-time programmable version, using a PIC programmer, then inserting the chip in the socket on the circuit board.

One transmitter is capable of controlling up to 32 receiver units. The transmitter and receiver were designed to be 'stand alone' so the system can be used in almost any environment. ■

The low-power transmitter and receiver mentioned in this article are available from Radiometrix at a 50% discount to readers mentioning this article – until 30 May. Call Radiometrix on 0181 4281220 or fax on 4281221. Further information, including full data, can be found on http://www.radiometrix.co.uk.

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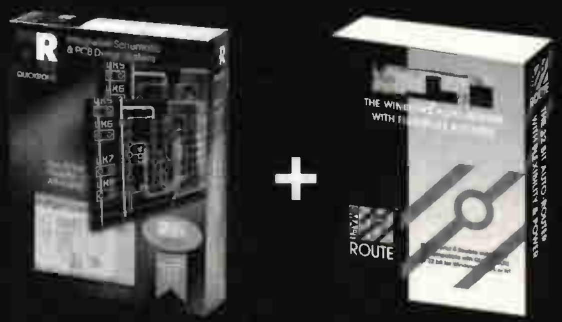


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# A balanced view

**Douglas Self explains how to get signals from A to B with the best possible integrity using balanced line input and output techniques**

Balanced inputs and outputs have been used for many years in professional audio, but profound misconceptions about their operation and effectiveness still survive. Balanced operation is also making a slow but steady advance into top-end hi-fi, where its unfamiliarity can lead to further misunderstandings. As with most topics in audio technology, the conventional wisdom is often wrong.

A practical balanced interconnect is not always wholly straightforward. Some new variations on input and output stages have emerged relatively recently. For example, a 'ground-cancelling' output is not balanced at all, but actually has one output terminal configured as an input. This can come as a surprise to the unwary.

Despite its non-balanced nature, such a ground-cancelling output can render a ground loop innocuous even when driving an unbalanced input. But even an audio professional could be forgiven for being unsure if it still works when it is driving a balanced input. The answer – which in fact is yes – is explained in a second article on this subject, details of which are given later.

## Electronic versus transformer balancing

Electronic balancing has many advantages. These include low cost, low size and weight, superior frequency and transient response, and no problems with low-frequency linearity. While it is sometimes regarded as a second-best, it is more than adequate for hi-fi and most professional applications .

Transformer balancing has some advantages of its own – particularly for work in very hostile rf/emc environments – but many serious drawbacks. The advantages are that transformers are electrically bullet-proof, retain their common-mode rejection ratio performance forever, and consume no power even at high signal levels. Unfortunately they also generate low-frequency distortion, have high-frequency response problems due to leakage reactance and distributed capacitance. Transformers are also heavy and expensive.

The first two objections can be surmounted – given enough extra electronic circuitry – but the last two cannot. Transformer balancing is therefore rare, even in professional audio, and is only dealt with briefly here.

## To balance...

Balancing offers the following advantages

- Discriminates against noise and crosstalk.
- A balanced interconnect – with a true balanced output – allows 6dB more signal level on the line.
- Breaks ground-loops, so that people are not tempted to start 'lifting grounds'. This is only acceptable if the equipment has a dedicated ground-lift switch, that leaves the metalwork firmly connected to mains safety earth. In the absence of this facility, the optimistic will remove the mains earth – which is not quite so easy now that moulded plugs are standard – and this practice must be roundly condemned as dangerous.

## ...or not to balance

Balancing also brings with it the following disadvantages.

- Balanced connections are unlikely to provide much protection against rf ingress. Both sides of the balanced input would have to demodulate the rf with exactly the same effectiveness for common-mode cancellation to occur. This is not very likely.
- There are more possibilities for error when wiring up. For example, it is easy to introduce an unwanted phase inversion by confusing hot and cold in a connector. This can go undiscovered for some time. The same mistake on an unbalanced system interrupts the audio completely.

## Balancing basics

Balanced connections in an audio system are designed to reject both external noise, from power wiring etc, and also internal crosstalk from adjacent signal cables.

The basic principle of balanced interconnection is to get the signal you want by subtraction, using a three-wire connection. In many cases, one signal wire – the hot or in-phase conductor – senses the actual output of the sending unit. The other, the cold or phase-inverted, senses the unit's output-socket ground, and the difference between them gives the wanted signal.

Any noise voltages that appear identically on both lines, ie common-mode signals, are in theory completely cancelled by the subtraction. In real life, the subtraction falls short of perfection, as the gains via the hot and cold inputs will not be precisely the same. The degree of discrimination actually achieved is called the common-mode rejection ratio, or cmrr.

The terms hot and cold, for in-phase and out-of-phase respectively, are used throughout this article for brevity.

While two wires carry the signal, the third is the ground wire which has the dual duty of both joining the grounds of the interconnected equipment, and electrostatically screening the two signal wires by being in some way wrapped around them. The 'wrapping around' can mean:

- A lapped screen, with wires laid parallel to the central signal conductor. The screening coverage is not perfect, and can be badly degraded as it tends to open up on the outside of cable bends.

- A braided screen around the central signal wires. This is more expensive, but opens up less when the wire is bent. Screening is not 100%, but certainly better than lapped screen.

- An overlapping foil screen, with the ground wire – called the drain wire in this context for some reason – running down the inside of the foil and in electrical contact with it. This is usually the most effective as the foil cannot open up on the outside of bends, and should give perfect electrostatic screening. However, the higher resistance of aluminium foil compared with copper braid means that rf screening may be worse.

## Electrical noise

Noise gets into signal cables in three major ways.

**Electrostatic coupling.** An interfering signal with significant voltage amplitude couples directly to the inner signal line, through stray capacitance. The situation is shown in **Fig. 1**, with *C,C* representing the stray capacitance between imperfectly-screened conductors; this will be a fraction of a picofarad in most circumstances. This coupling is unlikely to be a problem in hi-fi systems, but can be serious in studio installations with unrelated signals going down the same ducting.

The two main lines of defence against electrostatic coupling are effective screening and low-impedance drive. An overlapping foil screen – such as used on Belden microphone cable – provides complete protection. Driving the line from a low impedance, of the order of 100Ω or less, means that the interfering signal, having passed through a very small capacitance, is a very small current and cannot develop much voltage across such a low impedance.

For the best results, the impedance must remain low up to as high a frequency as possible; this can be problem as op-amps invariably have a feedback factor that begins to fall from a low, and possibly sub-audio frequency, and this makes the output impedance rise with frequency.

From the point of view of electrostatic screening alone, the screen does not need to be grounded at both ends, or form part of a circuit.[1] It must of course be grounded at some point.

Electrostatic coupling falls off with the

**List 1. Line output arrangements.**
- Unbalanced output
- Impedance-balanced output
- Ground-cancelling output, or ground-compensated output.
- Balanced output
- Quasi-floating output
- True floating transformer output

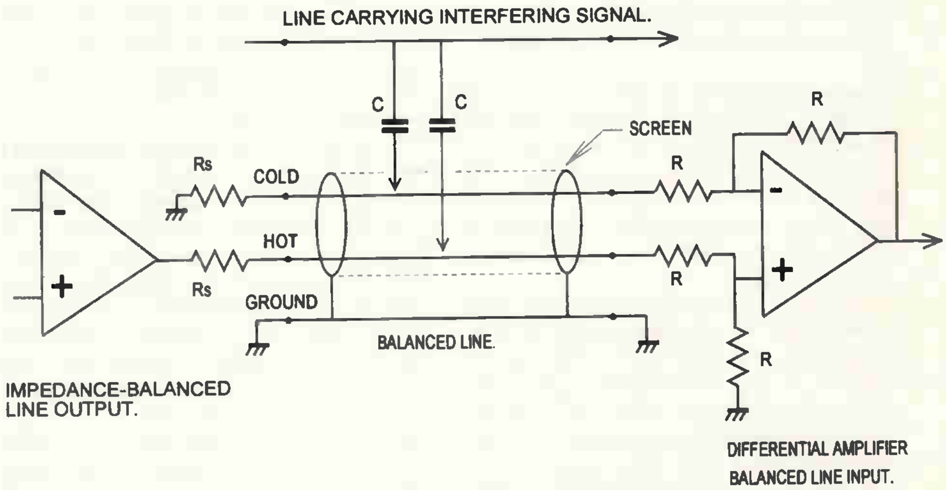


*Fig. 1. Electrostatic coupling into a signal cable. $R_s$ is 100Ω and R is 10kΩ. The second $R_s$ to ground in the cold output line makes it an impedance balanced output.*

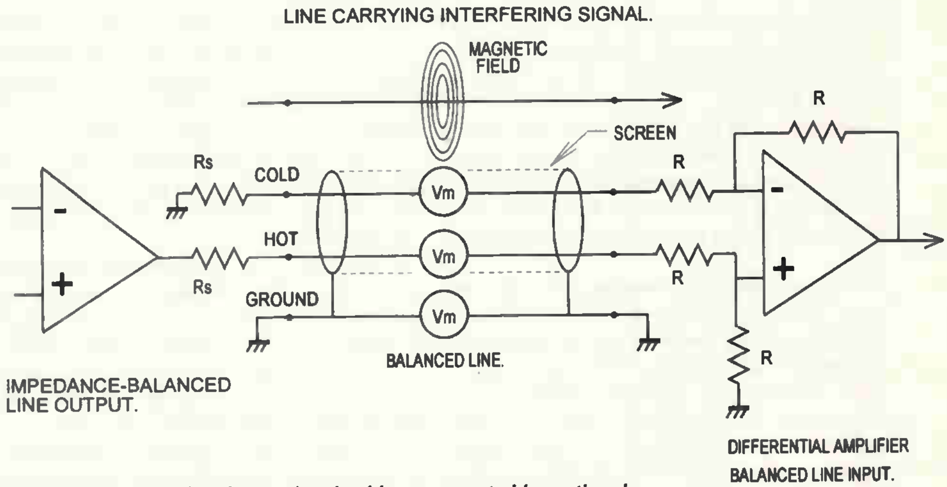


*Fig. 2. Magnetic coupling into a signal cable, represented by notional voltage-sources $V_m$.*

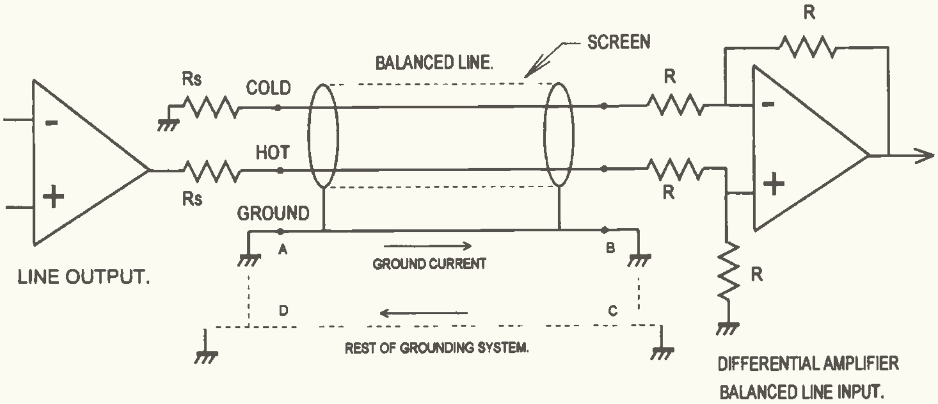


*Fig. 3. Ground-voltages coupling into a signal cable. The ground voltage between A and B is due to ground currents flowing around ABCD.*

square of distance. Rearranging the cable-run away from the source of interference is more practical and more effective than trying to rely on very good common-mode rejection.

**Magnetic coupling**. An emf, $V_m$, is induced in both signal conductors and the screen, **Fig 2**. According to some writers, the screen current must be allowed to flow freely, or its magnetic field will not cancel out the field acting on the signal conductors. Therefore the screen should be grounded at both ends, to form a circuit.[2]

In practice, the field cancellation will be far from perfect. Most reliance is placed on the common-mode rejection of the balanced system, to cancel out the hopefully equal voltages $V_m$ induced in the two signal wires. The need to ground both ends for magnetic rejection is not a restriction, as it will emerge that there are other good reasons why the screens should be grounded at both ends of a cable.

In critical situations, the equality of these voltages is maximised by minimising the loop area between the two signal wires, usually by twisting them tightly together. In practice most audio cables have parallel rather than twisted signal conductors, and this seems adequate most of the time.

Magnetic coupling falls off with the square of distance, so rearranging the cable-run away from the source of magnetic field is usually all that is required. It is unusual for it to present serious difficulties in a domestic environment.

**Common-impedance coupling**. Ground voltages coupled in through the common ground impedance; often called 'common-impedance coupling' in the literature.[3] This is the root of most ground loop problems. In **Fig. 3** the equipment safety grounds cause a loop ABCD; the mere existence of a loop in itself does no harm, but it is invariably immersed in a 50Hz magnetic field that will induce mains-frequency current plus odd harmonics into it. This current produces a voltage drop down the non-negligible ground-wire resistance, and this once again effectively appears as a voltage source in each of the two signal lines. Since the cmrr is finite a proportion of this voltage will appear to be differential signal, and will be reproduced as such.

A common source of ground-loop current is the connection of a system to two different 'grounds' that are not actually at the same ac potential. The classic example of this is the addition of a 'technical ground' such as a buried copper rod to a grounding system which is already connected to 'mains ground' at the power distribution board. In most countries this 'mains ground' is actually the neutral conductor, which is only grounded at the remote transformer substation. The voltage-drop down the neutral therefore appears between 'technical ground' and 'mains ground' causing large currents to flow through ground wires.

A similar situation can occur when water-pipes are connected to 'mains ground' except that interference is not usually by a common ground impedance; however the unwanted currents flowing in the pipework generate magnetic fields that may either create ground loops by induction, or interfere directly with equipment such as mixing consoles.

In practice, ground voltages cause a far greater number of noise problems than the other mechanisms, in both hi-fi and professional situations.

Even there is no common-impedance coupling, ground currents may still enter the signal circuit by transformer action. An example of such a situation is where the balanced line is fully floating and not galvanically connected to ground – which is only possible with a transformer-to-transformer connection.

The shield wire or foil acts as a transformer primary while the signal lines act as secondaries; if the magnetic field from the shield wire is not exactly uniform, then a differential noise voltage appears across the signal pair and is amplified as if it were a genuine signal. This effect is often called shield-current-induced-noise, or SCIN, and cables vary in their susceptibility to it according to the details of their construction.[4]

Fortunately the level of this effect is below the noise-floor in most circumstances and with most cables, for once a differential-mode signal has been induced in the signal lines, there is no way to discriminate against it.

From this summary I deduce there are two principle effects to guard against; electrostatic coupling, and the intrusion of unwanted voltages from either magnetic coupling or ground-loop currents.

Electrostatic interference can be represented by notional current-sources connected to both signal lines; these will only be effectively cancelled if the line impedances to ground are the same, as well as the basic cmrr being high. The likely levels of electrostatic interference current in practice are difficult to guess, so the figures I give in the second article are calculated from applying 1mA to each line; this would be very severe crosstalk, but it does allow convenient relative judgements to be made.

Magnetic and ground-voltage interference can be represented by notional voltage-sources inserted in both signal lines and the ground wire; these are not line-impedance sensitive and their rejection depends only on the basic cmrr, as measured with low-impedance drive to each input. Similarly ground-voltage interference can be represented by a voltage-source in the ground wire only.

Both input and output are voltages so the cmrr can be quoted simply as a ratio in decibels, without specifying any level.

## Line outputs

A line output is expected to be able to drive significant loads, partly because of a purely historical requirement to drive 600Ω, and partly to allow the parallel feed of several destinations. Another requirement is a low source impedance – 100Ω or less – to make the signal robust against capacitive crosstalk, etc.

There are many line output and input arrangements possible, and the results of the various permutations of connection are not always entirely obvious. An examination of the output types in use yields **List 1**.

**Unbalanced output**. There are only two physical output terminals – signal and ground, **Fig. 4a**). A third terminal is implied in Fig 4a, emphasising that it is always possible to connect the cold wire in the cable to the ground at the transmitting (output) end.

The output amplifier is almost always buffered from the line shunt-capacitance by a resistor $R_s$ in the range 33 to 100Ω, to ensure stability. This unbalances the line impedances. If the output resistance is taken as 100Ω worst-case, and the cold line is simply grounded as in Fig 4a, then the presence of $R_s$ degrades the common-mode rejection ratio to –46dB, even if the balanced input at the other end of the cable has perfectly matched resistors.

**Impedance balanced output.** There are now three physical terminals, hot, cold, and ground, Fig. **4b**). The cold terminal is neither an input nor an output, but a resistive termination with the same resistance $R_s$ as the hot terminal output impedance. This type of output is intended for use with receiving equipment having balanced inputs. The presence of the second $R_s$ terminated to output ground makes the impedance on each signal line almost exactly the same – apart from op-amp output impedance limitations – so that good rejection is achieved for both common-mode ground voltages and electrostatic interference.

If an unbalanced input is being driven, the cold terminal on the transmitting (output) equipment can be either shorted to ground locally or left open-circuit without serious consequences. Either way all the benefits of balancing are lost.

The use of the word 'balanced' is unfortunate as this implies anti-phase outputs, which are not present.

**Ground-cancelling output.** Also called a ground-compensated output, this arrangement is shown in **Fig. 5a**.

This allows ground voltages to be cancelled out even if the receiving equipment has an unbalanced input. It prevents any possibility of creating a phase error by miswiring. It separates the wanted signal from the unwanted by addition at the output end of the link, rather than by subtraction at the input end.

If the receiving equipment ground differs in voltage from the sending ground, then this difference is added to the output so that the signal reaching the receiving equipment has the same voltage superimposed upon it. Input and ground therefore move together and there is no net input signal, subject to the usual resistor tolerances.

The cold pin of the output socket is now an input, and must have a unity-gain path summing into the main signal output going to the hot output pin. It usually has a very low input impedance equal to the hot terminal output impedance.

It is unfamiliar to most people to have the cold pin of an output socket as a low impedance input, and this can cause problems. Shorting it locally to ground merely converts the output to a standard unbalanced type. If the cold input is left unconnected then there should be only a very small noise degradation due to the very low input impedance of $R_s$.

Ground-cancelling outputs would appear to be very suitable for hi-fi use, as they are an economical way of making ground-loops innocuous. However, I am not aware that they have ever been used in this field.

**Balanced output.** The cold terminal is now an active output, producing the same signal as the hot terminal but phase-inverted, Fig. **5b**. This can be simply done by using an op-amp stage with a gain of minus one to invert the normal in-phase output. Phase spikes are shown on the diagram to emphasise these phase relationships.

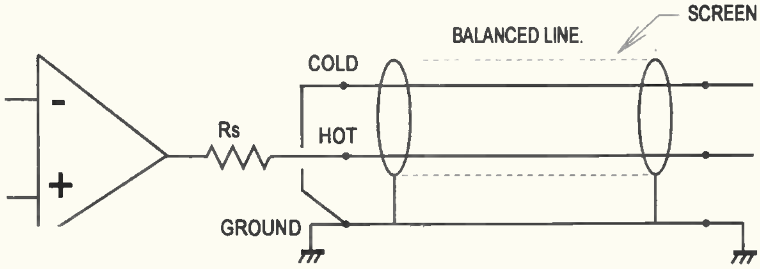


*Fig. 4a. An unbalanced line output. The cold output – if it exists at all – is connected directly to ground.*

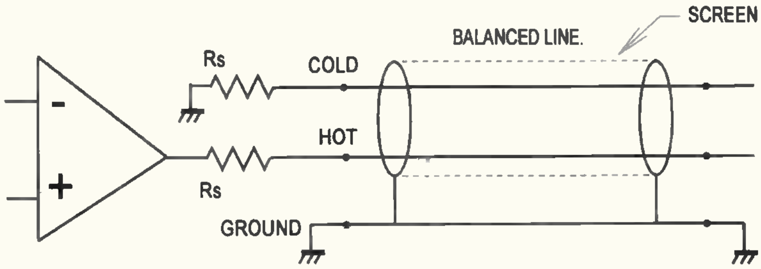


*Fig. 4b. An impedance balanced output. The cold output is connected to ground through a second Rs of identical value.*

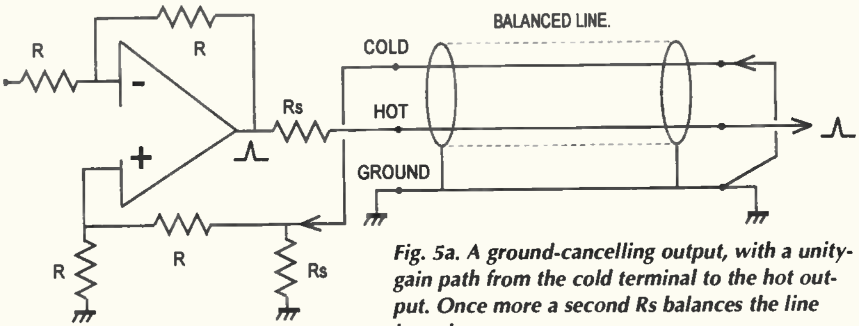


*Fig. 5a. A ground-cancelling output, with a unity-gain path from the cold terminal to the hot output. Once more a second Rs balances the line impedances.*

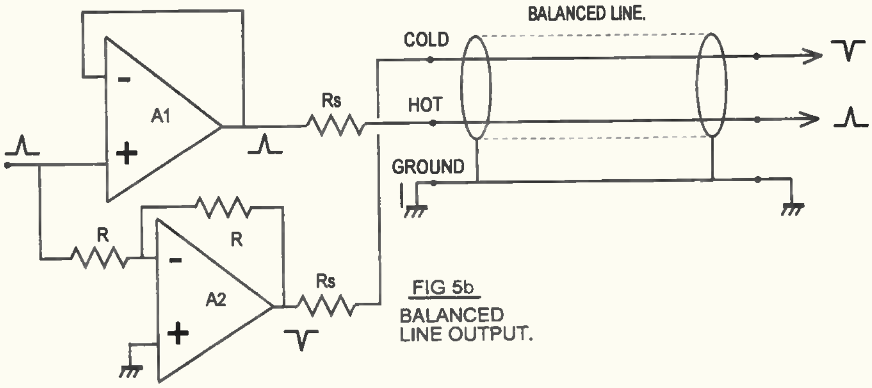


*Fig. 5b. A balanced output. A2 is a unity-gain inverter driving the cold output. Line impedances are balanced.*

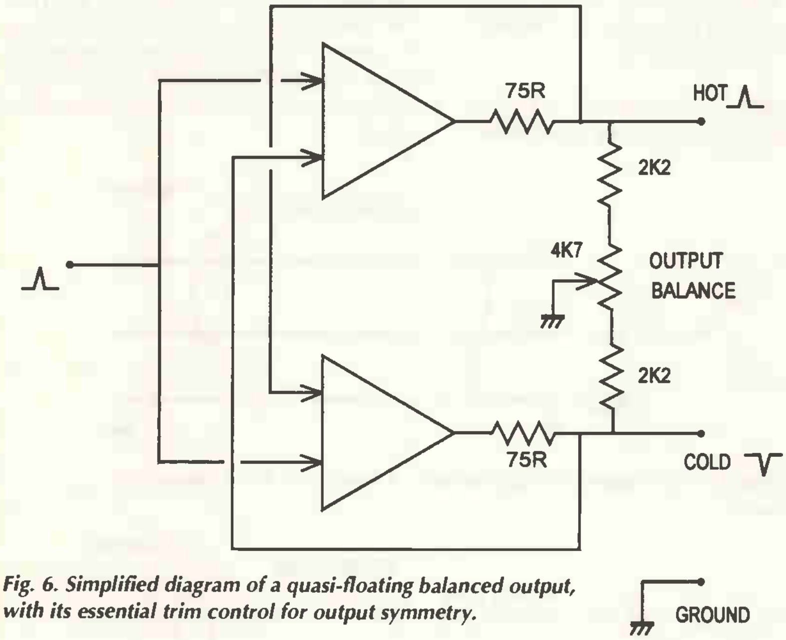


*Fig. 6. Simplified diagram of a quasi-floating balanced output, with its essential trim control for output symmetry.*

The in-phase signal itself is not degraded by passing through an extra stage and this can be important in quality-critical designs. The inverting output must not be grounded; if not required it can simply be ignored.

Unlike quasi-floating outputs, it is not necessary to ground the cold pin to get the correct gain for unbalanced operation, and it must not be grounded by mistake, because the inverting op-amp will then spend most of its time in current-limiting, probably injecting unpleasant distortion into the preamp grounding system, and possibly suffering unreliability. Both hot and cold outputs must have the same output impedance $R_s$ to keep the line impedances balanced.

A balanced output has the advantage that it is unlikely to crosstalk to other lines, even if they are unbalanced. This is because the current injected via the stray capacitance from each crosstalking line cancels at the receiving end.

Another advantage is that the total signal level on the line is increased by 6dB, which can be valuable in difficult noise situations. All balanced outputs give the facility of correcting phase errors by deliberately swopping hot and cold outputs. This tactic is however a double-edged sword, because it is probably how the phase became wrong in the first place.

This form of balanced output is the norm in hi-fi balanced interconnection, but is less common in professional audio, where the quasi-floating output gives more flexibility.

**Quasi-floating output**. This kind of output, **Fig. 6**, approximately simulates a floating transformer winding; if both hot and cold outputs are driving signal lines, then the outputs are balanced, as if a centre-tapped output transformer were being used.

If, however, the cold output is grounded, the hot output doubles in amplitude so the total level is unchanged. This condition is detected by the current-sensing feedback taken from the outside of the 75Ω output resistors. Current driven into the shorted cold output is automatically reduced to a low level that will not cause problems.

Similarly, if the hot output is grounded, the cold output doubles in amplitude and remains out of phase; the total hot-cold signal level is once more unchanged. This system has the advantage that it can give the same level into either a balanced or unbalanced input without rewiring connectors. 6dB of headroom is however lost.

When an unbalanced input is being driven, the quasi-floating output can be wired to work as a ground-cancelling connection, with rejection of ground noise no less effective than the true balanced mode. This requires the cold output to be grounded at the remote (input) end of the cable. Under adverse conditions this might cause hf instability, but in general the approach is sound. If you are using exceptionally long cable, then it is wise to check that all is well.

If the cold output is grounded locally, ie at the sending end of the cable, then it works as a simple unbalanced output, with no noise rejection. When a quasi-floating output is used unbalanced, the cold leg must be grounded, or common-mode noise will degrade the noise floor by at least 10dB, and there may be other problems. In both of the unbalanced cases the maximum signal possible on the line is reduced by 6dB.

Quasi-floating outputs use a rather subtle circuit with an intimate mixture of positive and negative feedback of current and voltage. This performs the required function admirably; its only drawback is a tendency to accentuate circuit tolerances, and so a preset resistor is normally required to set the outputs for equal amplitude; the usual arrangement is shown in Fig. 6.

If the balance preset is not correctly adjusted one side of the output will clip before the other and reduce the total output headroom. After factory setting this preset should not need to be touched unless the resistors in the circuit are replaced; changing the op-amp should make no difference.

The balancing network consists of a loading resistor to ground on each output; in this respect the output characteristics diverge from a true floating output, which would be completely isolated from ground. These loading resistors are lower than the input impedance of typical balanced inputs. So if simple differential amplifiers are used with unequal input impedances, (see the section on line inputs, below) the output balance is not significantly disturbed and clipping remains symmetrical on the hot and cold outputs.

Quasi-floating outputs are often simply referred to as 'balanced' or 'electronically-balanced', but this risks serious confusion as the true balanced output described earlier must be handled in a completely different way from quasi-floating.

**True floating transformer output**. This can be implemented with a transformer if galvanic isolation from ground is required. The technique is rarely used.

The second article in this pair looks at line inputs in detail, examines what happens when the different kinds of input and output are connected together, and deals with the philosophy of audio system wiring. ■

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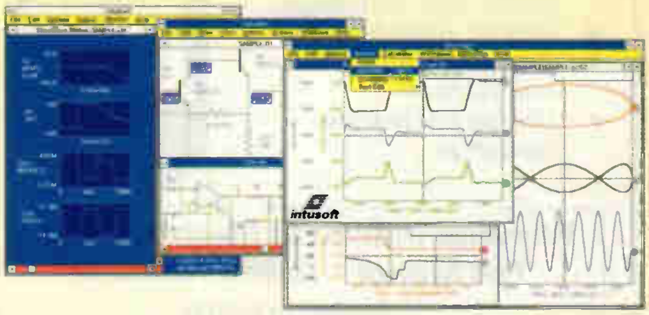


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# LETTERS

**Letters to "Electronics World"
Quadrant House, The Quadrant,
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## Simpler outphasing

In the April 1996 issue of *Electronics World*, David Gibson describes the use of all-pass filters in the outphasing methods used for ssb generation. He describes the use of a cascade of two first order all-pass filters in one leg – producing the in-phase output, and another two in the other leg, producing the quadrature output.

A letter published subsequently mentioned a simpler method using fewer op-amps, but I cannot recall the exact details. I think he may have been referring to Shirley's work*. Published as long ago as 1970, this article gives a full design with component values, for a quadrature network covering five octaves, with a peak deviation from 90° of ±3.8°. The values given are for a design covering 70Hz to 2.1kHz, but adjusting it for the communications bandwidth of 200Hz to 3kHz is only a matter of scaling the capacitor values. Allowing for an equal (geometric) overlap at each end, the range becomes 168Hz to 5.366kHz. This is $N$=1.79 times up on 3kHz and $N$ times down on 300Hz, since $N$ squared times ten equals two to the power five. One could select a range not of five octaves but only 3.33 octaves (300Hz to 3kHz). But the extra range at each end is useful to provide a little leeway for rolling off the response outside the three-decibel points of 300Hz and 3kHz. Otherwise brickwall filtering of the baseband signal will be needed, to prevent frequencies outside that range reappearing in the other – supposedly – suppressed sideband.

Shirley's article gives a graph showing the peak deviation from quadrature for an outphaser using two all-pass filter sections in each leg, against the desired span, e.g. 3.8° for five octaves as already mentioned. If the speech baseband is however known to be already band-limited to 300Hz to 3kHz, the graph shows that for a design covering just a 10:1 frequency ratio, the peak deviation from quadrature becomes just ±1.1°. The article also gives a Basic program listing which will calculate the required component values for any given bandwidth, returning in addition the resultant peak phase deviation from quadrature.

Using two first order all-pass filter sections per leg as in David Gibson's design, the component requirement runs to a total of twelve resistors, four capacitors and four op-amps. The circuit mentioned Shirley's article, which uses second order all-pass filter sections, needs the same tally of passives, but only two op-amps. As dual op-amps have a smaller footprint than quads, there is a minor advantage where space is at a premium.

In ssb speech communication links, measures such as vogads, IF clipping etc. are used to try and increase 'talk power', by increasing the mean to peak power ratio of the transmission.

A further useful method is to 'brighten' the speech with a 'blue' filter – one where the response increases by 6dB per octave as the frequency rises. This emphasises the lower level unvoiced sounds such as sibilants, fricatives, plosives and the like (ess, elf, pea, tea), which are crucial to intelligibility. Such a filter will of course shift the relative phase of the higher and lower frequencies of the baseband signal.

Fortunately, the relative phases are unimportant and indeed not perceived at all by the ear. However, such a blue filter, and indeed the all-pass filters used in outphasing methods, will have a very pronounced effect on any digital traffic that one sends over the link.

***Ian Hickman***
*Waterlooville*
*Hants*

*Shirley, F. R., 'Shift phase independent of frequency', *Electronic Design* No 18, Sept. 1 1970.

## On the wire

I read Cyril Bateman's article regarding loudspeaker cables with great concern. Despite his request, I have no interest in, "shooting these findings down in flames". There is little doubt that what Mr Bateman measured was repeatable.

However, there is a great step between making a repeatable measurement – however unsurprising – and giving a coherent theory which explains the measured results. My concern is that Mr Bateman has not made that step. His arguments are so flawed and his misuses of technical terms are so frequent that I have difficulty knowing where to begin putting them right. There is no justification whatsoever for treating loudspeaker cables as transmission lines and they do not have a characteristic impedance at audio frequencies.

Mr Bateman's use of the term transmission line is at variance with the accepted definition employed by the great body of electronic engineers. If technical definitions can be varied at will in this way it will not be long before communication is rendered impossible.

Existing circuit theory predicts the error due to loudspeaker cable very well, but even if it did not there would not be a problem. Loudspeaker design has moved on and the traditional passive loudspeaker fed by cable from a remote wideband amplifier is a bit of a dinosaur. Passive crossovers simply cannot meet modern performance criteria. With modern active designs there is no loudspeaker cable at all and it is difficult to see how Mr Bateman's findings advance the art.

The editor cannot be blamed for printing the articles in question. If *Wireless World* – for we still call it that – had been a peer review journal, many valuable articles would never have been printed. The down side of this freedom is that occasionally something regrettable is printed. *Wireless World* has a long standing tradition of doing the peer review in the letters page after publication.

As the author of some tens of *WW* articles I am acutely aware that one's work is well scrutinised and erroneous statements are usually set right by readers. If one is humble enough to heed readers comments, one can learn a great deal and I would commend this course to Mr Bateman.

***John Watkinson BSc MSc FAES***
*Reading,*
*Berkshire*

***Cyril replies***

May I thank John Watkinson for agreeing with my conclusion that the best speaker cable is to avoid using one i.e. to have no cable at all. Perhaps this is no surprise since these words were in fact used by Nelson Pass in his 1980 *Speaker Builder* article I referenced.

However, I must disagree with John in that the vast majority of hi-fi listeners do in fact listen to two or

## Electricity without magnetism

Your July 1992 issue included an article entitled 'Electricity without Magnetism'. That article prompted me to write a somewhat disparaging letter in September of 1994. As I had hoped, the letter resulted in a response in the November 1994 issue from one of the co-inventors, Dr. Harold Aspen, in which he advised that the invention/discovery was being further investigated by a group at MIT, USA.

We are just entering 1997 but to date no further information appears to have trickled out regarding where the invention now stands. Is it a non-starter? Many years ago I was deeply involved with both thermocouples and low-power ultrasonics, in totally separate applications. The ultrasonics work used thermionic valves because transistors had not then been invented. Since the device in question appears to take advantage of both technologies it is of considerable interest to me. I have endeavoured to obtain a small quantity of the PVDF material referred to in the article but have failed. That has prevented me from trying to duplicate the co-inventors work.

So, I will be delighted if someone is willing to bring me up to date with the present position. If Dr Aspen reads this letter, then perhaps he will now appreciate that my letter of July 1992 to *EW* was written with the sole intention of provoking a reply from one of the inventors – which it did. I had earlier written direct to his co-inventor, Mr. J. S. Strachan, Edinburgh University, but that proved to be abortive.

***R L Tufft***
*Thirsk*
*North Yorkshire*

# 25% reader discount


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Please mail this coupon to Vann Draper Electronics, together with payment. Alternatively fax credit card details with order on 0116 2773945 or telephone 0116 2771400. Address orders and all correspondence relating to this order to Vann Draper Electronics at Unit 5, Premier Works, Canal Street, South Wigston, Leicester, LE18 2PL. Overseas readers can also obtain this discount but details vary according to country. Please ring, write or fax to Vann Draper Electronics three way passive crossover speaker systems driven via several metres of cable. This indeed was the basic assumption used for all three of my recent articles, consequently his comments regarding active designs are not relevant to this series.

It seems my use of the transmission line equation at audio frequencies causes him discomfort. Perhaps it is worth recalling this equation was originally called the 'Telegrapher's' equation and was developed to quantify audio frequency transmission along telegraph lines. It was mathematically defined by Kennelly and Steinmetz in 1893, and while neither I nor the contents of my library are quite that old, I believe this predated its use for radio-frequency transmission. It is also perhaps worth recalling this mathematical derivation results from considerations of extremely short lengths of line.

Obviously, as stated in the articles, the commonly used rf simplification of $(L/C)^{1/2}$, which assumes that the ac resistive portion is negligibly small, is not applicable at audio frequencies since regardless of cable lengths, this resistive term dominates.

I didn't originally set out to prove cable impedance was relevant. Having performed the various measurements, which John accepts are repeatable, and using the accepted dogma of series resistance and inductance, I was totally unable to explain the voltage changes with frequency from 1kHz to 10kHz and change of cable, for the mosfet amplifier, Fig. 1, January 1987 issue, p. 55. These measurements for both amplifiers have recently been repeated over the extended frequency range 1kHz to 1MHz, with exactly the same results.

If John can offer an alternative more acceptable explanation as to how amplifier/cable/speaker damping performance can increase with frequency, when both the series impedance of the cable and the amplifier output impedance increase with frequency, I and I'm sure many other readers, would be more than pleased to be so informed.

If John also has access to better supporting evidence as to the behaviour of speaker cables, again it would be beneficial if other readers could be so updated. For my part, I shall continue to rely on my copy of 'Reference Data for Radio Engineers', published by Sams & Co, which states the full transmission line equation $((R+j\omega L)/(G+j\omega C))^{1/2}$, as quoted in my articles, is an 'accurate equation applicable from dc up to such frequency when higher modes appear'.

## Marconi sell out

Does it matter when we disperse at auction a major archive of scientific and technical papers, photographs and historic artefacts, encapsulating the very origins of a major science-led industry?

Some might think not, but that is exactly what GEC will shortly do with the complete archive and museum of the Marconi Company – at Christie's in London, on April 24 and 25.

It is clear from Christie's press release that this material is an unparalleled record of the origins and development of 'wire-less' communications, world-wide, and as such would be of first importance to maritime, military and general historians – as well as a source of inspiration to radio and electronic engineers. Part of the tragedy is that this collection has been so little studied, and that no attempt was made to display it during the Marconi Centenary Year. Nor has any worthwhile monograph seen recent publication.

International interest in this auction will be very great; and in the absence of intervention, dispersal abroad is likely. The Royal Commission on Historic Manuscripts, National Heritage Memorial Fund and Heritage Lottery Fund should consider this case as a matter of urgency.

Meanwhile, where are our national museums and professional institutions who should surely be exercising a watching brief?. And if this sale goes through – what other major institutions, some also concerned with broadcasting and telephony, will see fit to follow in taking the car boot sale approach to their – and our – historical inheritances?

***Dr Thomas Going***
*Southend*
*Essex*

## Irate communication over cable

I knew it! The March issue of *EW has* the now inevitable crop of letters which endlessly discuss the pros and cons of loud speaker cable construction; a subject whose boredom is only exceeded by that of a general election campaign:

While I appreciate that your editorial staff cannot influence the quality and quantity of letters submitted on any particular subject, you surely could draw a line under this one now and say 'enough is enough'

I realise that there just may be quite incredibly sensitive individuals in the population who can detect aurally the minutiae of distortion in their hi-fi systems; the difference for example between 0.001 and 0.01% of thd. However, since the signals subject to the minuscule distortion, if any, of loud speaker cables are also subject to the passage through innumerable acoustic, electric, electronic, modulation, demodulation and conversion processes on their way from source to loud speaker, one is tempted to dismiss as trivial the effect of speaker cables which are constructed from anything less sophisticated than multistranded bus-bars made from ultra pure, oxygen-free electrolytic platinum.

Do you remember the days gone by when your letter pages resounded with discussions on gravity, relativity, cosmology, the speed of light, Michelson and Morley, the Catt anomaly, Silvertooth, Aspden and the ether and so on and so on? Oh dear, what has gone wrong with *EW*? Or is it that something has gone wrong with your readers?,

***M G T Hewlett***
*Midhurst*
*W Sussex*

# Q&A

## 90° phase shift made easy

A In the February issue of *Electronics World*, a reader searches for a method of producing 90° phase shift. A QBasic program published in the 13 September 1976 issue of *Electronic Design* does exactly that.

***Dave Hayes***

## Led backwards

Q Why do light-emitting diodes have such a low reverse voltage? Often, only a few volts is specified. Many circuits would be simplified if the rating was 15V or so. Is the restriction to do with the manufacturing process?

***P Gascoyne***
*Wantage*
*Oxfordshire*

## Sound-driven car?

Q Does one of your more mature readers remember reading a constructional article, circa 1936, which appeared, I think, in *Car Mechanics* or *Car Illustrated*, both American publications (an English publication would at that time have used 'supersonic' not 'ultrasonic'). It used a mechanical ultrasonic generator, which was basically a close pair of perforated metal discs one being rotated at high speed, to generate high powered ultrasonics. These ultrasonics vapourised water contained in a sealed tank, which in turn, so it was claimed, developed sufficient pressure to operate a small steam engine with which to propel a car.

No doubt such a system could set up cavitation and vapourise water, but how to cope with the attendant noise of what was essentially a crude siren is difficult to understand. Perhaps one of your readers – probably deaf since 1936 – having built the contraption, might have some information.

Magneto-striction technology using frequencies above audibility might be a means of designing a modern equivalent for an ancient proposal. Who knows? Perhaps we might be able to discover from where many politicians get their 'hot air'.

***R L Tufft***
*Thirsk North Yorkshire*

## Wireless Service Manual?

Q Does anyone have a copy of the Wireless Service Manual, published by Iliffe around 1950? I am interested in details of an oscilloscope that incorporated an indicator unit known as a 'plan-position indicator'.

***C M Lindars***
*Providence Cottage*
*Unity Lane*
*Misterton*
*Crewkerne*
*Somerset TA18 8NA*

## Circuits for j-fets please

Q Does anyone know where I can get hold of application circuits for *MPF102* or similar j-fets please?

***W D Nicholson***
*13 Devanham Road*
*Handforth*
*Cheshire SK9 3QE*

## Cross over crossover

Bill Teleki's article 'Crossover Networks Made Simple' on pp. 548–550 in the July/August 1996 issue includes simulated responses for various orders of passive crossover networks computed on the basis of a purely resistive load. However, Bill has omitted to mention that the impedance of typical loudspeaker drive units is usually reactive in nature. This can significantly affect the performance of any filter networks that have been designed on the assumption that the impedance of a loudspeaker driver behaves like a pure resistor.

Here I will give an example of the effects of impedance mistermination on the response of a two-way third-order Butterworth crossover. Crossover frequency is chosen to be 3000Hz, and component values are computed using the assumption that the low-frequency and high-frequency drivers are each 8Ω resistive loads.

For the purpose of this discussion, the sound-pressure response of these drivers is assumed to be ideal, in the sense that it is completely flat from dc to infinite frequency.

Resulting low and high-pass filter response functions, together with the summed response, are shown in **Fig. 1**. The –3dB crossover point at 3000Hz is clear, as is the ±135° phase shift of the low and high-pass filtered responses, respectively.

**Figure 2** shows impedance response curves of two typical loudspeaker drivers, where one curve is for a woofer and the other is for a tweeter. The woofer's impedance response rises at high frequencies because of the inductance of the voice-coil and eddy current losses in the magnetic motor.

Note that the phase shift of the woofer impedance asymptotes to a value slightly greater than 45° at high frequencies. This impedance behaviour cannot be modelled by a simple inductance, as many people assume, as this would lead to an asymptotic phase shift of 90°. Because the lower limit of the plotted frequency range is 100Hz, the peak in the woofer impedance at the free air resonance frequency of the woofer is not displayed. The tweeter's impedance curve shows a peak at this driver's free air resonance frequency, while staying relatively constant elsewhere in the frequency range.

When the lowpass and highpass sections of the third-order Butterworth crossover network are terminated by the actual woofer and tweeter impedances, a number of interactions occur, and the results are shown in **Fig. 3**. Filtered and summed responses are quite different from those obtained when the drivers were assumed to be simple resistive loads, and the overall result can only be judged as being unacceptable. It is clearly evident that the lowpass filtered response no longer follows the desired response characteristic of a third-order Butterworth filter frequency response function.

A large peak at about 2500 Hz is evident, and the roll-off rate between 10kHz and 20kHz is only 13 dB/octave instead of the expected 18 dB/octave. The high-pass filtered response is much less affected, although it does show minor response anomalies, such as approximately 1dB of boost in the 12kHz frequency region. As a result, the magnitude of the summed response is far from flat, which is not the desired result.

This simple example illustrates that it is not a good idea to assume that a crossover network designed on the basis of constant resistive loads will perform adequately when the true driver impedances are connected to the filter network.

In this instance, the problems occurring with the woofer can be greatly reduced by the use of an *RC*

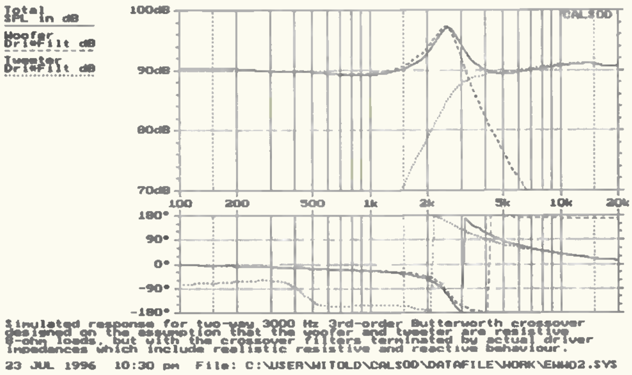


*Fig. 3. Low-pass (dashed line), high-pass (dotted line) and summed (solid line) frequency response functions obtained when the theoretical filter design is terminated with typical woofer and tweeter impedances.*

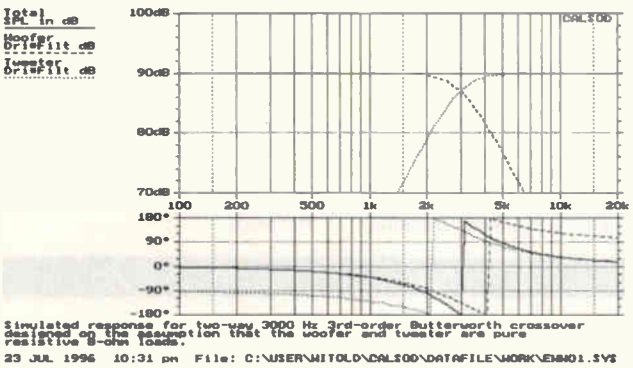


*Fig. 1. Simulated response for ideal purely resistive 8Ω drivers using a two-way third-order Butterworth crossover plotted over the frequency range from 100Hz to 20kHz.*

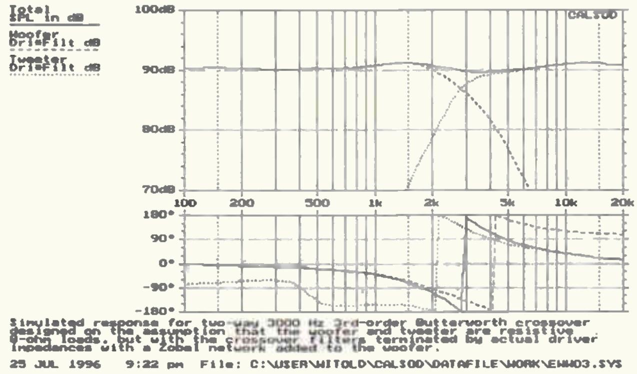


*Fig. 4. Low-pass, high-pass, and summed responses obtained when a Zobel network is added to equalise the woofer impedance.*

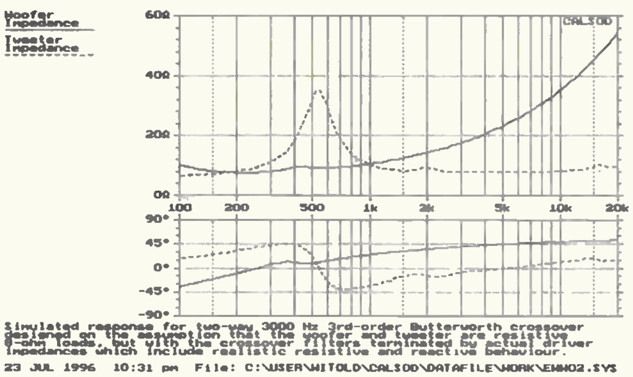


*Fig. 2. Typical impedance response curves for a woofer (solid line) and tweeter (dashed line).*

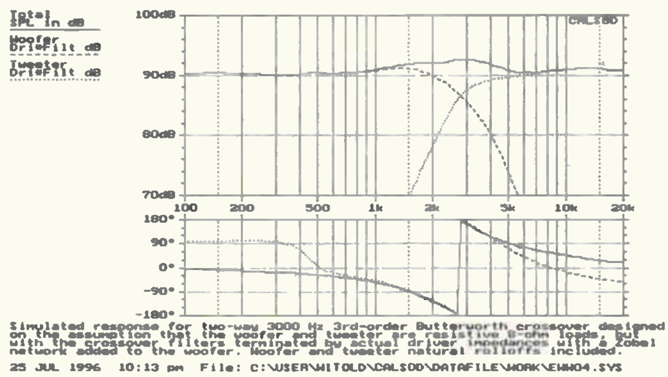


*Fig. 5. Low-pass, high-pass, and summed responses obtained when driver natural roll-offs are added to the model for the crossover with the Zobel network.*

impedance equalisation network connected across the terminals of the woofer. This serves to flatten the woofer's impedance at high frequencies, making it behave much more like a constant resistance. Such a network is referred to as a Zobel network, and is often used by designers of crossover networks.

**Figure 4** shows the results that can be achieved when a Zobel network comprising $R=8\Omega$, $C=10\mu F$ is connected across the terminals of the woofer. It is evident that the results are much better than those that were achieved without the use of the Zobel network. The low-pass response is now much smoother and closer in shape to the ideal third-order Butterworth response, and combines relatively well with the high-pass response to produce a reasonably flat summed response.

Another factor that was not mentioned in Bill's article that also needs to be accounted for in any crossover design is the natural response of each of the drivers. For example, the woofer might have a high-frequency roll-off that could typically be modelled by a second-order Butterworth response with a –3dB cut-off at 5kHz, while the tweeter's low-frequency roll-off might be simulated using a second-order Butterworth response with a –3dB point of 1.2kHz. **Figure 5** shows the responses obtained when these natural driver roll-offs are added to the simulations involving the crossover network with the Zobel network.

In this particular case, a slight boost in summed response in the crossover region is introduced. This results mainly from the fact that the lowpass and highpass responses shown in Fig. 5 are now acting in phase through the crossover region, whereas in Fig. 4 there is a phase difference of about 90°.

You should also remember that inter-driver time delays between the output from the woofer and tweeter also affect the summed response of the loudspeaker system. These time delays are caused by the physical offsets in the locations of the driver acoustic centres.

Depending on the actual loudspeaker system, the inter-driver time delays may improve or adversely affect the initial crossover design. Because of this, they should be understood to be an important factor affecting the performance of the completed loudspeaker system. For example, at 3kHz the wavelength of sound is 0.115m. A horizontal offset between the acoustic centres of the drivers of 1/4 of this, 0.029m, will lead to an additional phase shift of 90° between the outputs from woofer and tweeter.

Depending on the crossover topology chosen, this can have serious consequences for the quality of summed response. If a third-order acoustic Butterworth crossover topology is chosen, an additional 90° of phase shift will lead to a significant dip in the summed response at the crossover frequency.

I hope that these examples help to make it clear to you that there is no simple method of crossover design that will produce good results. Indeed, many different factors need to be taken into account if the selected crossover filter is to perform to the desired specification. This is the reason why it is unlikely that prebuilt crossover networks will produce worthwhile results when used with drivers for which they have not been designed.

All of the above simulations were performed using the Calsod loudspeaker design program developed by me in my spare time. It comes in two editions. Calsod 1.40 is the 'budget' edition (retail price AUD$119), while version 3.10 is the full featured edition (retail price AUD$449 with printed manual, AUD$379 with on-disk manual). When purchased from Audiosoft, all prices include air mail postage and handling. Both versions of the programme are capable of carrying out the simulations described in the text of my letter, and the program has many other useful features that would be of assistance to crossover network designers, including a network optimiser.

The package is available from Audiosoft, Melbourne, Australia, fax: +61 3 9497 4441 or e-mail: audiosoft@netwide.com.a, or from Marton Music in the UK on 01282 773198, fax 01282 773198.

***Witold Waldman***
*Melbourne*
*Australia*

## Pioneers of broadcasting

In their interesting article 'Making Continuous Waves', Tom Ivall and Peter Willis mention the early work of Canadian-born Professor Reginald Fessenden who broadcast speech and music in an historic 'first broadcast' on Christmas Eve 1906 using a steam-driven high-frequency alternator at Brant Rock, Massachusetts, USA. They also mention the start of regular programmes by KDKA in 1920 and "in the same year" regular broadcasts began in Europe from The Hague.

This seems a little unfair to the Dutch engineer Kanso Henricus Schotanus à Steringa Idzerda who in fact began his Hague Concerts from his PCGG valve transmitter almost a year before KDKA launched its service.

I will summarise briefly what I wrote in an article 'The Hague Concerts from PCGG – the bitter-sweet story of Hanso Idzerda' published in Radio Bygones, April/May 1990.

There are several claims and counter-claims surrounding the birth of radio broadcasting but there can be no doubt that for British listeners full credit belongs to Hanso Idzerda who launched the first of his 'musical evenings' on Thursday, 6 November 1919, with broadcasts specifically intended for British enthusiasts from April 1920. His broadcasts preceded the experimental radiotelephony 'broadcasts' from Chelmsford by the Marconi Company from February 1920.

On a wavelength of 670 metres, PCGG began almost a year before KDKA Pittsburgh (27 October 1920) and is often credited with being the world's first broadcasting station.

There were earlier experimental transmissions of speech and music – Fessenden, in 1906, was almost certainly the first. De Forest and his Radio Telephone Company made experimental transmissions from about 1908-12 and again in 1916-17.

An authenticated claim can also be advanced on behalf of a group of Belgian experimenters including Raymond Braillard and Robert Goldschmidt who set up a transmitter in the grounds of the Royal Castle at Laeken and broadcast programmes of music for public reception every Saturday from 28 March 1914. This continued until August 1914, when their transmitter was hurriedly destroyed shortly before the Germans entered Brussels.

Idzerda, however, seems to have been the first to build a transmitter specifically for broadcasting on a semi-commercial basis with the firm intention of expanding the sale of the crystal sets, valved amplifiers and components made or marketed by his own firm (Ned Radio-Industrie, or N R-I).

It seldom pays to be a pioneer. Hanso Idzerda and PCGG were gradually squeezed out as the popularity of wireless grew. From about 1924 PCGG broadcasts virtually ended and he drifted out of the public eye.

Twenty years later, during WW2, he was found trespassing on a prohibited area, apparently searching for fragments of an exploded V2. He was arrested by the Germans on suspicion of espionage or possibly held purely as a hostage. He was executed by shooting during the night of 3/4 November 1944.

***Pat Hawker, G3VA***
*London SE22*

## Preamp design thoughts

I have read with interest recent articles on low noise audio preamplifiers. This shift of emphasis away from what seems near obsessive examination of audio power amplifier distortion to the subtleties of small signal manipulations is welcome. My tin ears will tolerate modest distortion in listening at sociable levels, but are perhaps as sensitive to hum and noise levels as any auric articles, so any improvement in these parameters should be welcomed. I make the following observations on two particular pieces.

Simon Bateson's design in the May Issue is headlined as the ultimate microphone preamp, and the purpose designed late eighties *SSM2016* IC at its heart is undoubtedly excellent at its job. How unfortunate it is then that the apparent obsolescence (letters July/August) of the IC has meant an early revision of Mr Bateson's 'final microphone preamp'. Perhaps surprisingly the revised design employs the *SSM2017*, which has a much lower specification than the *2016*, and this with an undesirable and improperly polarised electrolytic. This latter inclusion apparently makes no audible difference, but I suspect that this component now becomes the most critical in respect of noise (and distortion?) performance in the amplifier.

The *INA103*, whose use he rejects in his letter, actually exhibits greatly superior dc precision to both *2016* and *2017*. It certainly would not require capacitor coupling. The noise figure of the SSM devices, as in most instrumentation amplifiers, is a function of gain and falls to around 2.5dB at a gain of 100 from 1dB at a gain of 1000.

The *INA103* would give a 1.5dB noise figure with 150Ω input ($1nV/\sqrt{Hz}$) at $G$=1000, 3dB at $G$=100; ie only marginally poorer. Actual noise performance of the amplifier will be highly dependent on the impedance spectrum of the microphone. Are these important curves readily available? They need to be to make proper objective design decisions.

The 'no-compromise' disc preamp by Douglas Self in the July/August issue purports to use the latest of op-amps, but resigns itself to being a revision of his earlier 1983 design. The rather complex moving coil

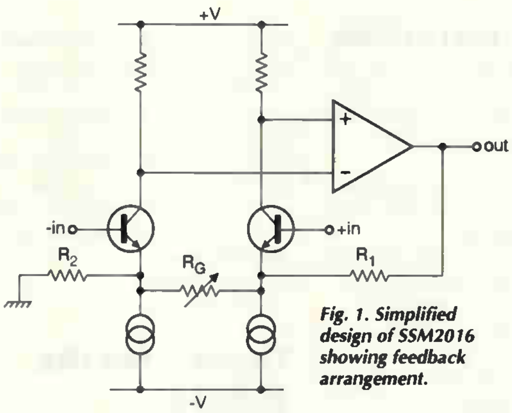



*Fig. 1. Simplified design of SSM2016 showing feedback arrangement.*

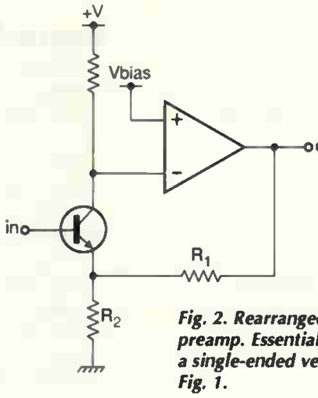



*Fig. 2. Rearranged Self preamp. Essentially this is a single-ended version of Fig. 1.*

stage as shown resists full analysis as the negative rail voltage is omitted and therefore the transistor operating point is uncertain. Assuming 70µA as shown in Table 2, the three *2SB737* devices in parallel should give approximately 1nV/√Hz (1.7/√3) voltage noise density. This figure can be slightly bettered using the *LT1028* op-amp (0.85nV/√Hz) or the *AD797* (0.9nV/√Hz) with a much simpler circuit. The excellent dc characteristics of these modern devices obviates the need for capacitor coupling and their power supply rejection ratio recommend their use in this role. The *LT1028* can drive a 100Ω load while maintaining 1V/µV open-loop gain. As a result, it should maintain very low distortion.

In the presented design, some of the available gain is thrown away, and distortion increased from the lower resultant feedback presumably due to the inability of the *5532* to drive less than 600Ω – the total feedback resistance. Additional device cost (*circa* £7; 1 off) would be offset by reduced associated component cost and pcb surface area. It is practically negligible compared with the cost of top-rate pickup cartridges. I wonder if these recent devices have been considered and/or tested and rejected?

The topologies of the two preamplifiers are actually identical except that the *2016* device offers balanced operation. The *2017* is, I believe, similar internally. **Figs 1** and **2** show the essentials with an n-p-n in the Self case for readier comparison.

Figure 1 is actually simpler in its practical implementation due to its precision dc balance, and offers a very desirable advantage from a common-mode rejection angle where the cartridge can be suitably connected.

Similarly the *INA103* should again prove ideal here. I am sure Robert Pease (Letters, Jul/Aug 1996) would be interested in any improvement to (perceived) sound quality of using these relatively exotic but affordable and available devices.

Finally, a couple of general queries. Can Mr Self provide references or the measured data on capacitor induced distortion in filter circuitry to which he refers? Secondly, perhaps he can explain why it is advantageous to follow the RIAA curve to within ±0.05dB? It is practically a truism to state that loudspeaker and room colouration show response flatness at least an order of magnitude poorer. Vacuuming the carpet would likely give as insubstantial a difference. I look forward to further preamplifier articles in *EW* to remain abreast of the state-of-the-art in this esoteric field.

***Michael Hutchings***
*Fareham*
*Hampshire*

***Douglas replies***

Anyone who publishes a design in *Electronics World* must expect a bracing shower of criticism, and so I was not surprised to read Mr Hutching's unenthusiastic assessment of my preamp in the April Letters column. I was sorry though that there appeared to be nothing at all he liked about it. I also regret he finds my studies of power amplifier distortion "obsessive". For my own part I rather dislike the current trend for labelling anyone who shows any interest in anything as "obsessed".

Where Mr Hutchings got the idea that my preamplifier purported to use the latest of op-amps I do not know. I said explicitly in the article that the *5534* might be a relatively ancient design, but the laws of physics have not decayed over the years, and neither has its superb audio performance. It is used almost to the exclusion of anything else in professional audio all round the world, so clearly there is a good reason. It is simply not possible to buy anything better at anything like the price.

As for noise, if Mr Hutchings had examined my article more closely he would have seen that an $I_c$ of 70µA for the *2SB737* transistor is for the moving magnet case. The $I_c$ for the moving-coil stage is 1mA per device, which is a bit different. This gives a voltage noise density, $e_n$, of 0.29nV/√Hz and a current noise density, $i_n$, of 2.5pA/√Hz – much less than his figures, and voiding most of his argument. The *LT1028* now calculates as at least 7dB noisier than my version.

Mr Hutchings also seems to have based his calculations solely on $e_n$; this can lead you grievously astray. It is essential to add the effects of $i_n$, which is high for the op-amps Mr Hutchings prefers. The $i_n$ is just as important as $e_n$ in a moving-magnet stage, due to the high source impedance at high frequencies of the cartridge inductance.

The *LT1028* calculates as 0.7dB noisier than the *5532* in an RIAA stage, allowing for both $e_n$ and $i_n$. However, its worse than that, Jim. The application of op-amps to audio is even less straightforward than it appears.

Take the *OP27*, which on paper (adding in both $e_n$ and $i_n$) is 2.3dB quieter in an RIAA stage with a real cartridge load. If you measure it, you will find it is actually 2dB *noisier* than the despised 5532 it replaces. The resolution of this paradox is that most op-amps are optimised for dc performance rather than audio. The *OP27* is no exception, and so it has a bias-current cancellation system strapped to the inputs. This generates extra common-mode noise, and if the impedances at the two inputs are not the same – and they are very different in an RIAA stage – the extra noise is not cancelled. The *LT1028* incorporates a similar bias-cancel structure.

From the data sheet, the *LT1028* seems to generate significant (>0.01%) distortion, and I suspect it will be a lot worse into 100Ω – even at modest levels.

I agree entirely that the *AD797* is a superb op-amp, and it was in fact my original intention to use it in the preamp. However, I found that hf stabilisation, particularly with high negative feedback factors, could be very tricky, and placing such a design in front of the public would be to open a veritable oil-drum of worms.

In view of Mr Hutchings' lack of enthusiasm for distortion reduction, as expressed at the start of his letter, I was surprised that he feels the sub-0.002% thd of the moving-coil stage is too high. I agree that it looks wrong 'to throw' away gain and hence negative feedback factor, but the vital point is that my circuit has a discrete input stage. This has gain of its own, and when added to that of the op-amp, open-loop gain is not lacking.

The alternative approach Mr Hutchings suggests – which I assume has not actually been built and tested – apparently costs seven times as much as my solution. There is no way you are going to get that back by saving a square inch of pcb area. As for equalling the performance – well, I will be interested to see if it can be done.

Finally, what is the advantage of an RIAA curve accurate to ±0.05dB, when scratching your nose causes a bigger change in room response? Well, what is the point in trying to do anything better? I wasn't designing a living-room, I was designing a preamp.

My philosophy is to get the best possible performance without spending significantly more money. The RIAA scheme gives remarkable accuracy for a modest outlay, and does it in a way that I thought would be interesting to readers.

A purely electronic system jolly well ought to be orders of magnitude better than a complicated electro-mechanical-acoustic system, because the problems are so much easier to solve.

One rationale for designing better and better amplifiers is to spur the loudspeaker community into designing better speakers. I detect that this trend has already begun, as I see more and more technical papers about the measurement and simulation of speaker non-linearities in *JAES*, etc.

As for non-electrolytic capacitor distortion, I do have a few nuggets of data to offer. If my third-order subsonic filter is tested at 8V rms in isolation, the thd above 100Hz is below 0.0004%. At 20Hz, third-harmonic distortion rises sharply to 0.004%, corresponding to the –3 dB point of the filter. It continues to rise as frequency falls – despite the roll-off in output level. This is with standard 63V polyester capacitors.

Changing all three to 100V polyester (as per prototype) reduces the 20Hz thd to 0.0006%, though there is still a steep rise below this frequency. I think this proves, a) that the distortion originates in the

## 15Hz subwoofer – missing resistor

In the phase splitter of Fig. 1b, resistor $R_3$ has no annotation on the diagram. It is 10kΩ.

capacitors, and, b) that it depends on the capacitor dielectric. As is usual with third-harmonic distortion, the thd is proportional to voltage squared. There is no such effect in the RIAA stage, so I can only assume that polystyrene is better from this point of view.

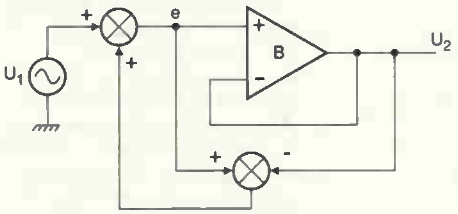
I am grateful to Marcel van de Gevel for pointing this out.

***Doug Self***
*London*

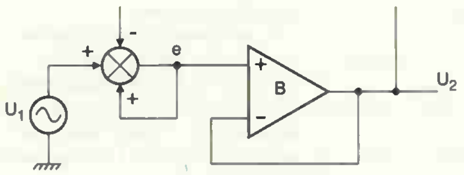
## Error cancelling in audio

In last December's Letters column, p. 688, K.H. Ellis shows the 'Hawksford' error cancellation technique for power amplifiers. The following analysis shows that 'error cancellation' is too optimistic a description.

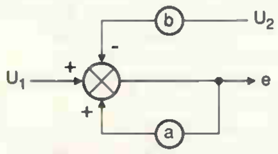
According to this technique the error of an output-stage (B) is substracted from the input signal:




This can be simplified to,



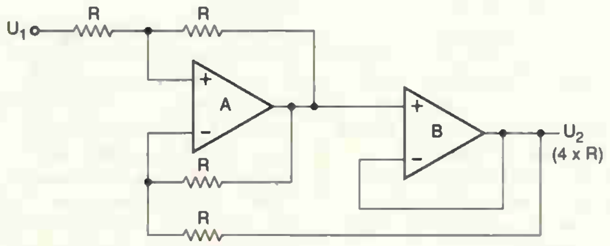

Physical realisation of the summing device can be modelled as,



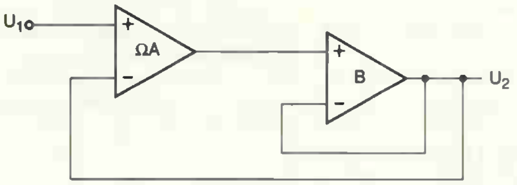

$$Gain = \frac{e}{u_1 - bu_2} = \frac{1}{1-a}$$

where elements 'a' and 'b' represent the non-ideal behaviour of the summing action (a,b=0.9... to l).

For 'a' approaching 1, the gain approaches infinity so the summing device acts like an open-loop op-amp. This can also be seen with a realistic implementation, such as:




Due to cancellation of the negative and positive feedback around amplifier 'A', this circuit simplifies to:




Thus the proposed system behaves like an ordinary feedback amplifier.

***Nanno Herder***
*University Groningen*
*The Netherlands*

## Sounds incredible

There are some questions that arise from the interesting article by Reg Miles 'Sonics from Ultrasonics' on pp 14-15 in the January 1997 issue.

It is a very old misconception to imagine that the simple sum of two sinusoidal variations such as $\sin(2\pi f_1 t)+\sin(2\pi f_2 t)$ will produce a pair of new 'sum and difference' signals of frequency $(f_1+f_2)$ and $(f_1-f_2)$. In fact these 'sidebands' appear only when subsequent non-linear or multiplicative signal processing is effected.

The misconception is encouraged both by the fact that many systems spuriously contain sufficient non-linearity to supply some processing and also by misinterpretation of a bit of mathematics (often published in early textbooks) describing the purely notional envelope of the waveform of the simple sum.

In practice, the ear can supply the non-linearity, but even then, you would not wish to rely upon this oddity to reproduce high quality sound, and certainly not to apply high intensity ultrasonic stimulation to such a sensitive and valuable human sense organ.

The report that "...polyurethane filters had to be hung between the people and the (loud)speakers to selectively absorb the ultrasound..." to prevent 140dB levels from damaging people, demonstrates what a bad idea it is. If the ultrasound is at a high level it is dangerous. If it is reduced before reaching the ear, it will not work and there was no point in producing such high power – unless there is some curious nonlinear effect taking place in the absorbent curtains.

***Bob Pearson***
*Bourne*
*Lincolnshire*

## CAD inadequacies

May I thank Ralph Riegler for his complimentary comments on the "Route to pcb-CAD" series of articles?

The via problem he mentions is a common one. No-one likes vias, so most autorouters have a via minimiser strategy. The Ares level II autorouter from Propak has such a minimiser, so has the Ares III from Proteus. You can choose a hole size and via pad size to suit yourself, but if you pick a size which is too large you will make it more difficult for the autorouter, as the obstruction will then restrict its choice of routes.

I have tried miniature eyelets and conductive epoxy paste for vias, as well as Veropins, short wires and the plating-through process. For making vias on one-offs, none of them is very good. I use link-pins (RS part no. 435-383) which are designed for this job and can be very rapidly inserted. They come in sticks of 50 pins and, at only £10 per box of 1000, are not too expensive. Using them saves a lot of time and effort.

***Rod Cooper***
*Sutton Coldfield*
*West Midlands*

## Thanks for the debate

Cyril Bateman appears to say that an increase in conductor separation changes the voltage drop in a cable from about 40mV pk-pk to nearer 50mV – the drop due to the amplifier output impedance appears to increase as well, which is suspicious, but I'll let that pass.

How many volts are being produced by the driving amplifier? Far more than a few millivolts, I'll wager, though he does not actually say. In reality a change of a few millivolts is irrelevant when the voltage across the speaker terminals is measured in volts.

Secondly, Cyril does a PSpice analysis using an exponentially damped sine wave. The sharp change in slew rate at the start of the waveform introduces high frequency components which stimulate ringing at 50kHz and upwards. This only lasts 100µs at most. There is a much higher level and longer lasting 10kHz signal present at the same time. The idea that the quieter, shorter, and ultrasonic component should be "clearly audible" is laughable. More importantly however, his claim that the waveform used is representative of audio transients is quite wrong. Real sounds recorded on real recording equipment do not contain components at 50kHz and above to stimulate such ringing.

In the third article, Geoff Williams tells us that putting things near speaker cable seriously affects sound quality, bare wire outperforms insulated wire, the only real answer is Litz wire, and cable ratings may well need to be of the order of 50A... Heaven help us! It never ceases to amaze me that people can seriously write such twaddle.

Still, it all makes for a very entertaining read, so I thank you for printing it all. I would especially like to thank Eric Forth for pointing out that taking a blowtorch to lawnmower cable improves its high frequency performance.

***Alan Robinson***
*Holgate*
*York*

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## Rms-to-dc converter reads in decibels

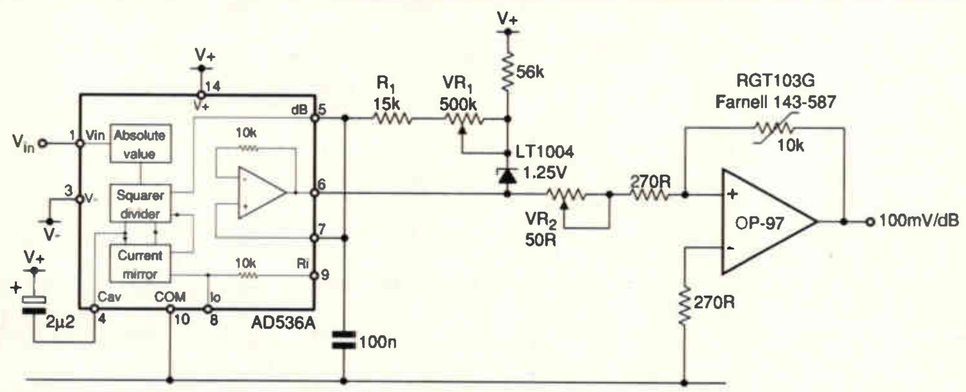
Analog Devices's data sheet for the *AD536* shows an rms-to-dc converter with a decibel output. I have experienced difficulty in obtaining proper logarithmic conformance over the full dynamic range and also the *Q81* or *PT16* temperature-compensating resistors specified.

Reference current for the converter is usually produced by a resistor to the supply rail from the decibel output on pin 5, the resulting current being $I_{ref}=(V-\Delta V_{be})/R$, since $\Delta V_{be}$ is the subject of the measurement, there is now a little non-linearity as $I_{ref}$ varies with $V_{be}$. My solution is to use a constant-current source: an *LT1004* diode and the uncommitted, unity-gain buffer in the *AD536*. Logarithmic conformance is improved and $I_{ref}$ is independent of supply variations. Potentiometer $VR_1$ sets zero so that 1V rms is equivalent to 0dB, and $VR_2$ sets the output to +100mV/dB.

My temperature sensing resistor is the *TG2103G* by VTM Ltd, obtained from Farnell.

***Alex Birkett***
*London SE22*

*Offering improved performance over the Analog Devices suggested circuit, this conforms well to a log. law and, as a bonus, reduces the effect of supply variation.*



# Active three phase rectifier features 0.1V drop

This circuit reduces the normal 1.2V forward voltage drop of a bridge rectifier to around 0.1V. It makes use of the little know fact that power fets work backwards as well as forwards, allowing the inherent reverse biased diode in their structure to be shorted by turning the transistor on.

With all the transistors off, the source-drain diodes in the fets rectify the incoming three phases, providing dc at the output which is subject to the diode drops.

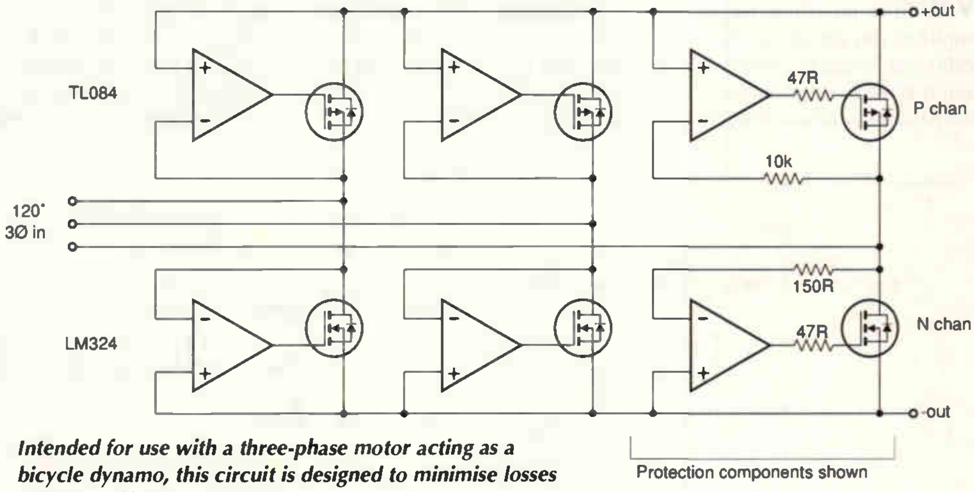
When the output reaches about 4V the op-amps, wired as comparators, begin to operate.

Taking $IC_{1a}$ and p-channel $Tr_1$ as an example, the comparator senses the voltage across the fet. While the phase voltage is lower than the positive rail, the output of the comparator will be high because the voltage at the non-inverting input of the comparator is higher than that at the inverting input.

As the phase voltage increases above the rail voltage, the inverting input becomes the more positive and the output goes low. This causes the transistor to turn on, shorting out its diode. Current flowing through the on-resistance of the fet creates a voltage drop that maintains the comparator output low, keeping the transistor on.

When the phase voltage drops below the output rail, current begins to flow back through the fet. This reverses the voltage drop across the fet which causes the output of the comparator to swing high, turning the fet off. Positive feedback ensues, ensuring that only a brief pulse of reverse current flows.

All the positive side switches are the same and the negative side switches are similar, but use n-channel fets.




***Intended for use with a three-phase motor acting as a bicycle dynamo, this circuit is designed to minimise losses due to rectifier voltage drop.***

The op-amps have to work with their inputs outside their supply voltages, so they are chosen specifically. The *LM324* input voltage range includes the negative rail and its output defaults low when its inputs are pulled above the positive rail. The *TL084* input range includes the positive rail and its output defaults high when its inputs are pulled below the negative rail. The minimum working voltage of *TL084*s varies from maker to maker. Motorola's seem to work at 4V.

The op-amp output series resistors are there to suppress oscillation in the unlikely event that it should occur because of fet gate capacitance.

Once the rectifier is working actively, the op-amp inputs do not stray far outside the voltage rails, but at voltages below active operation, or if a fet fails, they can be pulled more than a volt to the wrong side.

**£100 WINNER**

The *LM324* is adequately protected by limiting its current to less than 50mA using a resistor. The *TL084* is more difficult. If an input is drawn more that 0.3V below the negative rail damage can be done whatever the series resistance is. Including a diode from the positive rail catches the non-inverting input 0.6V below the positive rail and the 10kΩ resistor limits the diode current.

Transistor turn-off depends on the op-amps detecting the reverse voltage across the transistors in the on state. To guarantee this, the op-amp input offset voltage must be less than the $R_{DS(on)}$ of the fet multiplied by the maximum desired amplitude of the reverse current pulses.

**Steve Tree**
*Epsom*
*Surrey*

# Simple, economical and low power water detector

Existing water detectors possess several drawbacks. If direct voltage is used on the probes, they oxidise. If alternating voltage is applied at 5-10kHz, the current drawn is high and the accompanying diode pump and comparator increase the component count. There are dedicated ics for the purpose, but they also draw high currents – even when water is not present.

The circuit shown uses three gates, three resistors and a capacitor. It operates from 5V to 15V dc and does not oxidise its probes.

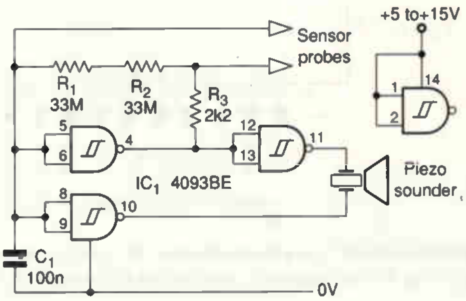
One gate from the *4093BE* works as an oscillator, the frequency of which is 0.1Hz by virtue of the 66MΩ feedback resistance and 0.1μF capacitor; you can hear a click from the piezo sounder every few seconds, which is useful in confirming operation.

However, when the probes touch water, the reduced resistance across the feedback chain causes an increased oscillation frequency and an audible tone from the sounder.

Two of the remaining gates are buffers for the signal to the sounder and $R_3$ prevents shorts between gate input and output if the probes become shorted.

The circuit draws about 75μA in standby; 1.5mA when it finds water.

**Philip Male**
*Drake's Broughton*
*Pershore*
*Worcestershire*




***Very simple circuit overcomes the problems with conventional water detectors: probe oxidisation, high currents and complication.***

# Voltage-controlled output common-mode

While behaving as a normal differential input/output amplifier, this circuit has the additional feature of controllable common mode at the output; it is independent of input common-mode voltage.

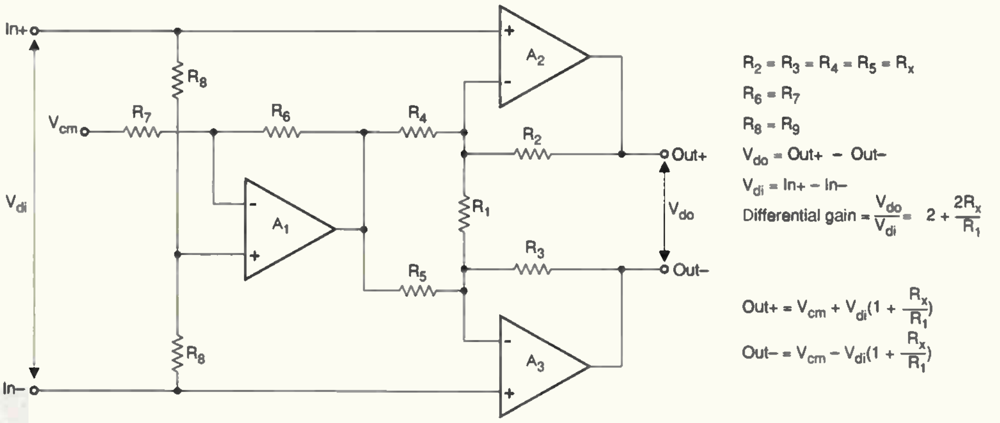
For example, if the control input voltage $V_{cm}$ is 0.9V and $V_{do}$ 0V, then both $V_{out+}$ and $V_{out-}$ will be 0.9V; for a $V_{do}$ of 1V, $V_{out+}$ will be 1.4V and $V_{out-}$ 0.4V.

Differential gain is $V_{do}/V_{di}=2+(2\times R_x/R_1)$;
$V_{out+}=V_{cm}+V_{di}\times(1+R_x/R_1)$;
$V_{out-}=V_{cm}-V_{di}\times(1+R_x/R_1)$
where $R_x=R_2=R_3=R_4=R_5$.

In comparison with a normal differential amplifier, input impedance is reduced by the effect of $R_{8,9}$. If this poses a problem and if a precise setting of output common mode in unnecessary, then eliminate $R_{8,9}$ and take the positive $A_1$ input to either of the inputs, which will apply a small offset to the output. Otherwise, for a low-frequency input, again eliminate $R_{8,9}$ and take $A_1$ input from half-way down $R_1$; the input is across $R_1$, so the effect is the same. The only slight problem is possible instability, which can be cured by a capacitor across $R_6$.

One can envisage several applications for this circuit; it does, of course, provide absolute values of output signals. It could also, perhaps, be used in a pulse-width modulator.

***Albert Pijuan***
*Girona*
*Catalonia*




***This differential amplifier has its output common-mode voltage defined by a voltage input. Output excursions are independent of the input common-mode level.***

# Manually loading serial data

Figure 1 shows a method of manually programming a 16-bit word and transmitting it on an SPI or QSPI serial interface. In this way, serial data peripherals such as data converters, memory and display drivers may be exercised before the system is complete. It serves write-only peripherals updating on the rising edge of /CS.

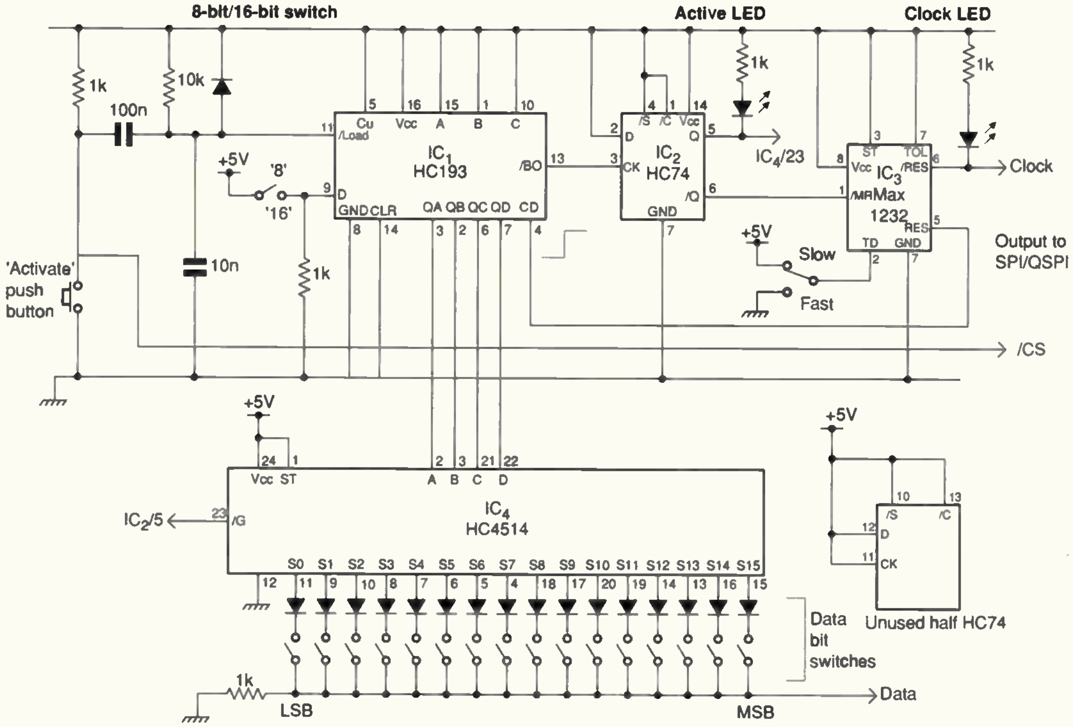
The *HC193*, $IC_1$, is a synchronous up/down counter, $IC_2$ an *HC74* D-type flip-flop and the *HC4514*, $IC_4$, a 4-to-16 line decoder – all common cmos devices also in the 4000 series. Microprocessor monitor $IC_3$ is a *MAX1232* that gives a low-frequency, two-phase clock inhibited at logic level at the /MR input, and two speeds set by the switch on the TD pin.

Depressing switch $S_{16}$ starts a count down by pulsing /LOAD on $IC_1$, the count starting at 16 or 8 depending on the position of $S_{17}$, and $Led_2$ flashes. Each output of $IC_4$ pulses high in turn, he resulting serial data output depending on which of the $S_{0\text{-}15}$ switches are made; a closed switch produces a 1 output.

Data is set up on the rising RES output of $IC_3$ and clocked out on the rising edge of /RES. When the count on the ABCD inputs of $IC_4$ reaches zero, $IC_1$'s /BORROW output produces a negative pulse to send the /Q output of $IC_2$ low, which stops the clock by the manual reset input of $IC_3$. $Led_2$ stops flashing to indicate the end of the cycle; it is normally on, but flashes when this circuit or another bus master is active. $Led_1$ lights when this circuit transmits.

Data output is compatible with cmos inputs of most SPI peripherals and a simple buffer makes it ttl-compatible. $IC_4$ is only enabled by $IC_2$ Q output during writing, the bus therefore being otherwise free for use by other interface controllers, which will overdrive /CS and clock outputs.

***Kevin Bilke***
*Maxim Integrated Products, Reading*




***To load serial data into SPI peripherals before the system microcontroller or software are working, this circuit allows a 16-bit word to be manually entered and transmitted along the SPI bus.***

# Locking an *LC* oscillator

You can lock an *LC* oscillator parametrically by periodically varying the damping of the tuned circuit. In this circuit, frequency $f_1$ may be synchronised by an external signal at the same frequency or by a sub-multiple of it.

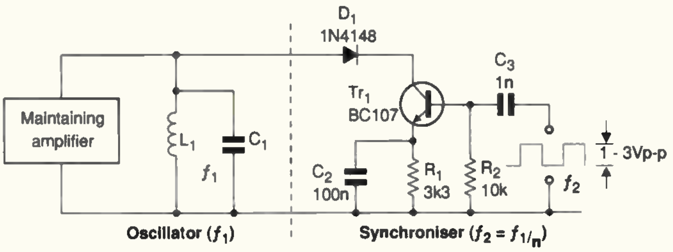
Behaviour is similar to that shown when an oscillator is locked by injecting an external signal: as the tuning point is approached a beat appears and the system locks near zero beat, locking over a small range of tuning.

Operation is at its best when $f_2$ is a square wave having a short rise time. Differentiator $C_3R_2$ produces spikes to turn $Tr_1$ on, current pulses then flowing from the tuned circuit into $C_2$, charging it and periodically damping the tuned circuit. In the circuit shown, this happens during positive half cycles across the tuned circuit.

Output appears across $R_1$, as does a direct voltage which goes through a minimum near the middle of the locking range; at this point, there is only a small disturbance of the tuned circuit by locking pulses. The circuit locks, in the short term, for $f_1/f_2$ up to about 100.

Component values are not critical, but $R_1$ should be about equal to the tuned circuit dynamic resistance.

***George Short***
*Brighton*




***Positively locking an LC oscillator by using the locking signal to damp the tuned circuit. Values shown are suitable for frequencies up to a few tens of kilohertz.***

# Voltage-controlled oscillator

Inspiration for this circuit came from an article by Ayers in 1994, in which the properties of operational transconductance amplifiers were discussed. In this case, otas are used in a controllable sinewave generator to cover the audio band, 20Hz-22kHz, in one sweep.

Two operational transconductance amplifiers, $IC_{5a,b}$, form a state-variable filter whose frequency response is made variable by means of the input from $P_1$. Output from the filter goes back to its input via $IC_3$ and the limiter, so that the circuit oscillates at the filter frequency.

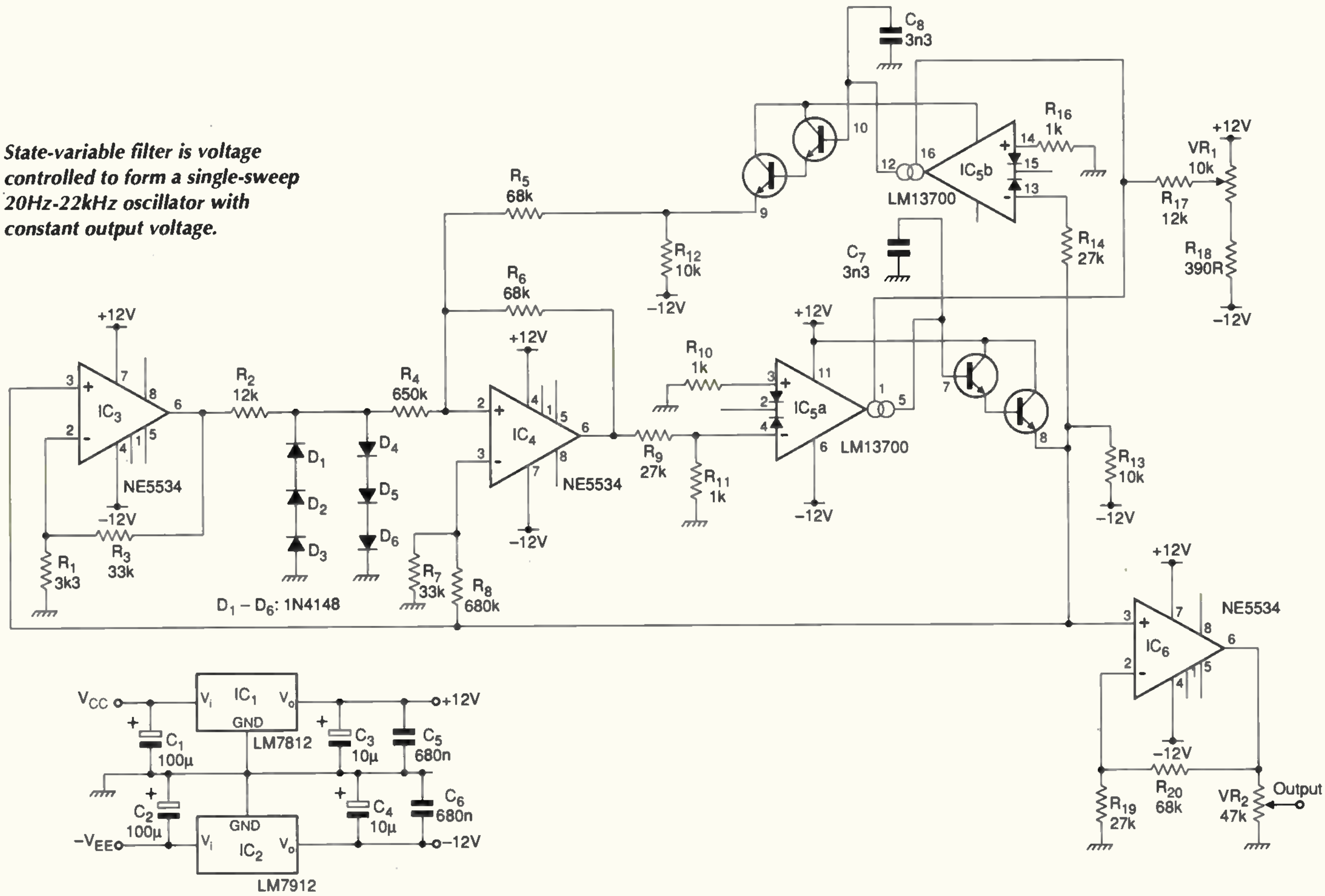
Since the feedback signal is limited, the output voltage of the filter is virtually constant with frequency and no level control is needed. Buffer $IC_6$ gives 10Vpk-pk of sinusoid, which is not entirely distortion-free; my application could tolerate a little distortion, but the circuit had to be simple.

***Bernard Van den Abeele***
*Evergem*
*Belgium*

### Reference

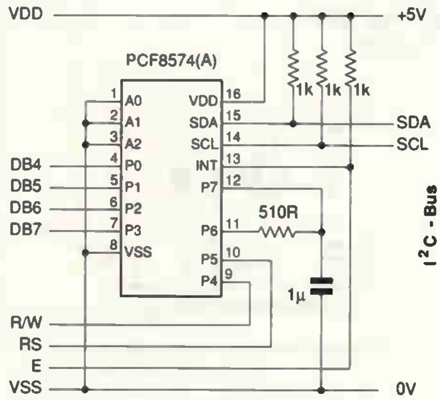

1. Ayers, D. 'The Versatile world of OTAs'. *Electronics World + Wireless World*, March 1994, p197.


***State-variable filter is voltage controlled to form a single-sweep 20Hz-22kHz oscillator with constant output voltage.***



# Simple I²C-to-lcd interface

For small lc displays, driving can hardly be simpler than this method, which uses one *PCF8574* 8-bit i/o port with interrupts and five passive components to drive a four-bit display




*Simple and frugal I²C interface for liquid-crystal display modules.*

module, freeing four port lines for control.

Writing to the port when /INT is set resets /INT high, any change of state on any input setting /INT low again, the change occurring after data is transferred so that the data is recognised. An *RC* network between output $P_6$ and input $P_7$ effects this timing, shifting the output signal past the end of data transfer. Toggling $P_6$ on every input causes this interrupt S/R sequence to form an E signal for the display.

Two consecutive calls to the I²C port effects a complete data transfer of eight data bits; data, msb first, in the lower nibble and control bits in the upper, E being generated automatically, as above, if $P_6$ changes state in succession. Observing the timing of the display instruction cycles means that there is no need to read the BUSY flag, but set E high by not toggling $P_6$, set the device for input, read from the display and toggle E low again, twice. Make sure to track the state of $P_6$.

The bus address of the *PCF8574* is 0100xxxw and for the 8574A 0111xxxw, xxx being set by hardware and w being the write bit. To initialise the display for four-bit working on two lines, with cursor shift rightwards and visible, send the following hex sequence to the I²C device:

C3 83 C3 83 C2 82 C8 80 CE 80 C1 80 C6,

the first five being for external and internal sync. followed by byte pairs for function set, display on, clear display and entry mode set.

The word 'wireless' results from:

A7 E7 A6 E9 A7 E2 A6 E5 A6 EC A6 E5 A7 E3 A7 E3.

80 $C_1$ clears the display.

***Dipl. Ph. Detlef Mahr***
*Freiburg*
*Germany*

# Noisy supply for aircraft radio testing

Electronic equipment in aircraft running on 12V dc must work in the presence of supply noise of 2V pk-pk; this circuit is meant to test aircraft radio.

Essentially, the tester takes the form of an oscillator applied to the adjustment pin of an *LM317* voltage regulator. Since the 'noise' waveform did not have to be anything too wonderful, I used an oscillator consisting of two gates from a *4811* drive a *4817* counter with weighted outputs to produce a sinusoid in the 30-3500Hz range. This output goes to a *741*, which also sets the output direct voltage level between 5V and 15V, to modulate the supply.

Aside from radio testing, the circuit can be used to test the equivalent series resistance of an electrolytic capacitor by setting the dc bias and modulating the source, the series resistor being steel wire, measured by length.

***J D Ingram***
*Gawler*
*South Australia*

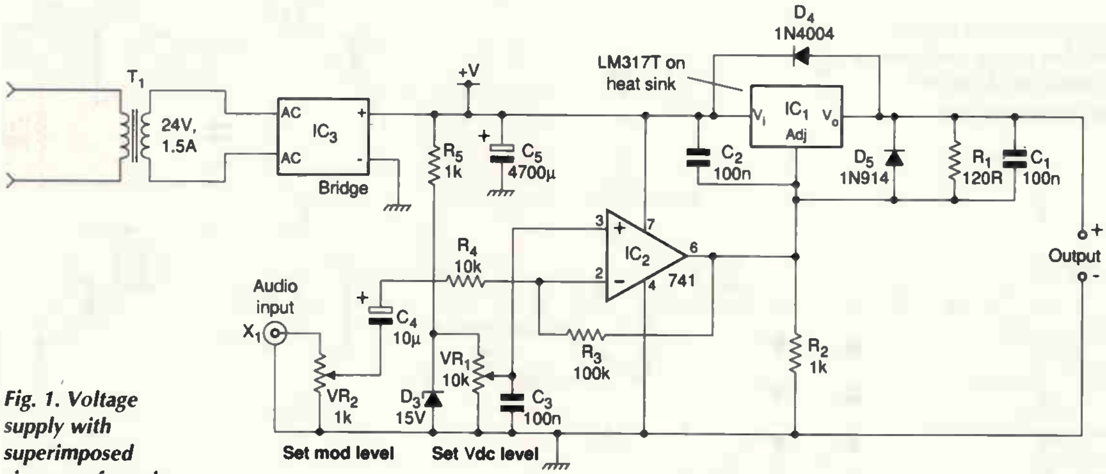



*Fig. 1. Voltage supply with superimposed sinewave for noise testing. Output voltage is settable from 5V to 15V and the 'noise' is 2V pk-pk. Oscillator output is 30Hz to 3.5kHz.*

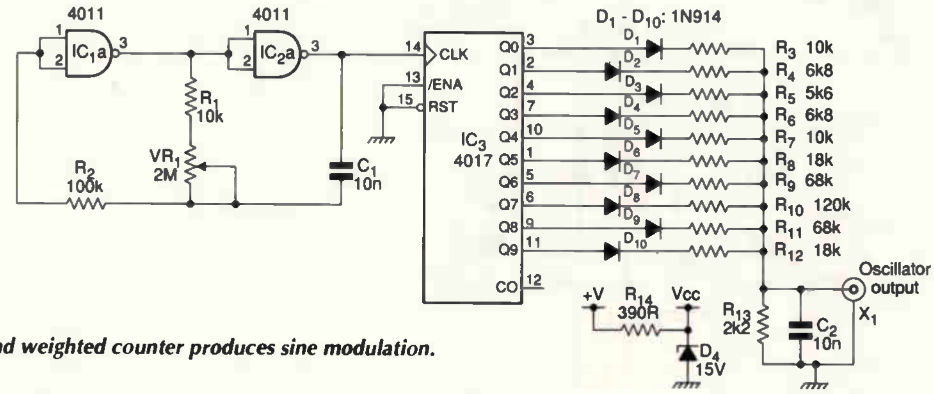



*Fig.2. Oscillator and weighted counter produces sine modulation.*

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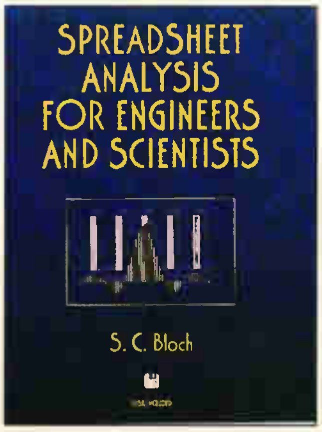


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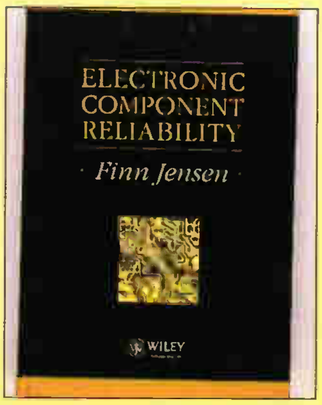


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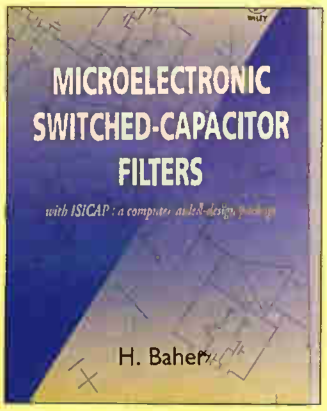


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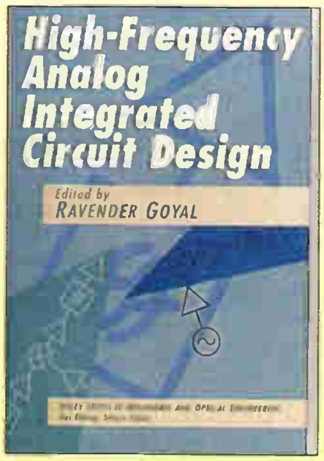


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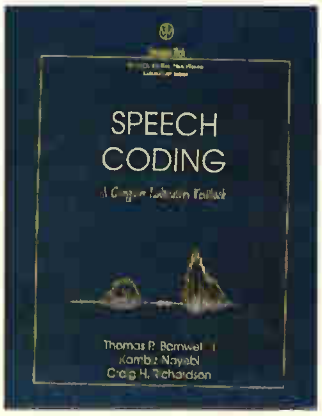


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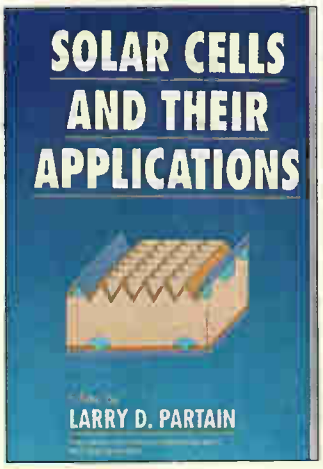


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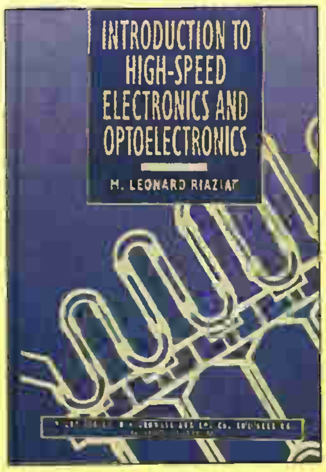


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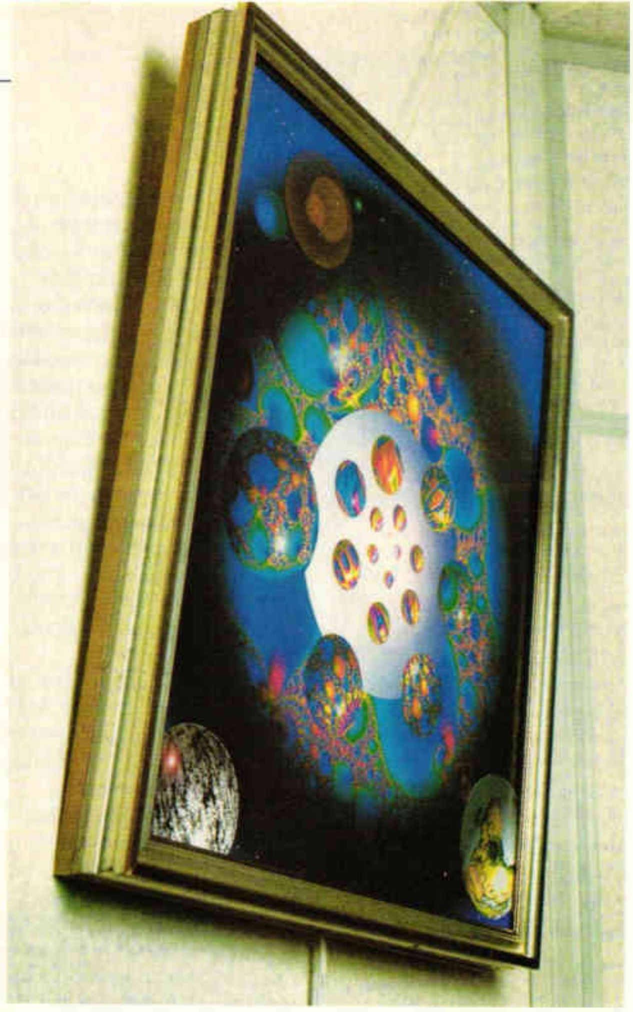
*One of the most useful attributes of flat panel speakers is their ability to be disguised, in this case as a picture.*



# Sound from pictures

**Richard Ball reports on a further new flat-panel loudspeaker technology, this time involving piezo-electric drivers.**

Noise Cancellation Technology, also known as NCT, is one of two companies proving the popular bus theory – wait for years and then two come along at the same time. In this case the 'bus' is flat panel loudspeaker technology which NCT has developed along similar lines to another company, NXT, a subsidiary of Verity (see *EW*, January 1997, p. 33).

Although the technologies may at first appear to be remarkably similar, the final products have been arrived at through apparently different research.

Malcolm McDonald, managing director of NCT in the UK, said: "We started with car headliners about two years ago."

The headliner is the material covering the inside of the roof of the car. This is a much better place to site loudspeakers than down by the passengers' ankles or behind the rear passengers' heads. For proof of this, sit in the back seat of the average 18 year old's car. Asking for a bit more bass could result in serious haemorrhaging.

## Low-frequency response

However, NCT had a problem with low-frequency response. To solve its problem, the company went to the State College in Pennsylvania, and a US company called Oxford Speakers, experts in active noise control. Between them, McDonald says, "they managed to work out how to couple piezos [piezo-electric transducers] to panels to create low frequency sound."

The low frequency crossover point is around 180Hz, so a subwoofer is used to fill out the bass below this frequency. The flat speakers were placed in the car headlining. Because the subwoofer is non-directional, it can be placed in any convenient position.

But McDonald says: "Psychologically, all the sound coming from the top is not what you are used to." For this reason the best results come from some speakers being placed near the floor.

A speaker set up like this can reduce weight and cost while saving space the company claims. To prove its point, in the UK, NCT has fitted out a Vauxhall Vectra and a Ford Mondeo with the flat speaker setup for demonstration purposes.

Much of the car headlining work has been carried out in conjunction with Johnson Controls, one of the world's largest manufacturers of car fittings.

The same principles of coupling piezo transducers to panels has been applied in other areas including ceiling tiles and pictures. The ceiling tiles are aimed at exhibitions, factories and offices. Pictures can be used in just about any conceivable environment, but they are most suited towards home entertainment.

## A baffling problem

With the pictures, there were initial problems placing them close to the wall. Any closer than a few inches and the sound from the rear interfered destructively with that from the front. This was solved by framing the active panel, and using a heavy back panel to reduce sound from the rear. In this way, the destructive interference is avoided.

It is interesting to note that this out-of-phase sound leading to destructive interference from the rear is the opposite of the claims from NXT, the other flat speaker company. In NXT's case, sound from the rear is claimed to be in-phase with sound from front.

For both car headliners and pictures, finding the right panel material was an experimental process. Lots of different materials were tried, but the best in terms of sound quality and cost was to use standard poster board fixed in a frame. This is rather convenient as poster board is one of the cheapest materials available, although its long term resistance to the constant vibration has yet to be established.

The next problem was that of coupling power from the piezo-electric transducer into the panel. With a single piezo transducer, McDonald says an insufficient amount of power is transferred to the panel.

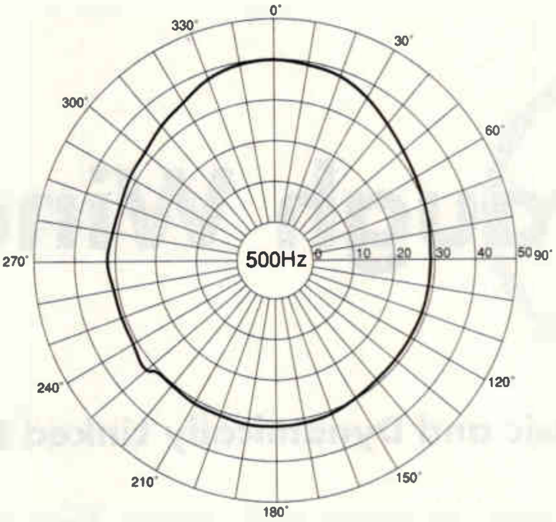
"We use multiple actuators to control the modal response," says McDonald. "Several transducers help to smooth the low frequency modes" and to provide the power.

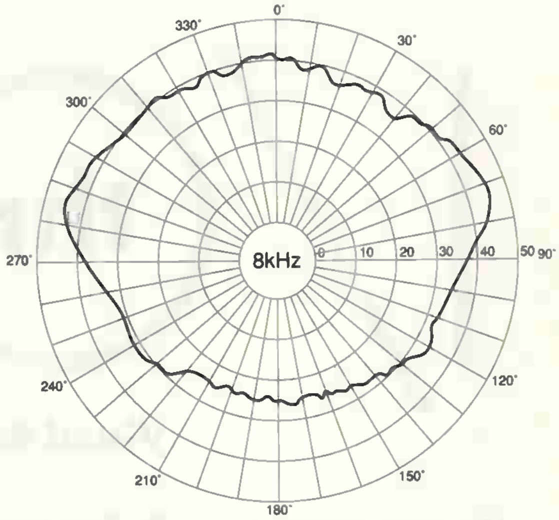
To decide exactly how many piezo actuators to use and where to site them, the company used a mixture of mathematical modelling and experimentation.

The behaviour of the panel is "very hard to model at high frequencies", says McDonald. This is because the fixing of the panel in a frame leads to complex boundary conditions which preclude modelling.

Therefore, the panels are modelled at low frequencies and experimented on at higher frequencies.

The result is a panel with a flat frequency response from 180Hz to 20kHz – the company claims within ±1.34dB. For home theatre, in the same way as the car headliner example, a subwoofer is used for very low frequencies.




*The polar plots, taken with a microphone at two metres, show sound pressure levels at two frequencies, 500Hz and 8kHz. The relatively constant level at all angles is in marked contrast to polar plots of older flat panel speakers, particularly the electrostatic type, and of conventional cone loudspeakers. These tended to be highly directional in nature. The directivity of conventional cone units is especially bad at high frequencies.*
*These plots from NCT are very similar to those from NXT – the other recent designer of flat panel loudspeakers.*

For pictures, the final product typically measures 600 by 650mm, and is driven by eight actuators.

### So why use multiple transducers?

Piezo-electric transducers have a high impedance, the opposite of most amplifier outputs. They can be modelled as capacitors, so their low frequency impedance is high, making them inefficient at coupling power from the amplifier to the panel at audio frequencies. Therefore, several transducers are distributed around the panel to provide enough energy. At high frequencies the modal density increases so more actuators are needed here to control the modes.

NCT claims the speakers are approximately ten per cent efficient. This may not appear brilliant, but it is better than conventional moving coil loudspeakers. These typically have efficiencies of a few per cent.

"We use transformer coupling in cars to cover the impedance mismatch," said McDonald. And the company is designing a direct drive amplifier to suit a capacitive load.

The use of piezo-electric devices as the actuators for the panels has led to good high frequency performance. This is opposite to electromagnetic transducers which roll off at higher audio frequencies.

The company claims to have measured up to 50kHz from the panels in an anechoic chamber. This is limited to 20kHz in products.

McDonald says this means there is no phase change at the higher frequencies. Because of this, he says, "the mid range transient response is very fast. If anything we have to calm it down at high frequencies." ■

# I/O through Windows

## Visual Basic and Dynamically Linked Libraries

**Windows was not designed with control engineering in mind, but it is possible to perform i/o tasks by writing your own Dynamically Linked Libraries, as Colin Attenborough explains.**

Visual Basic lets you write a program with a Windows graphical user interface with minimum effort. The usual Windows paraphernalia of buttons, check boxes, list boxes and radio buttons – and more – are available by drawing them onto a background 'form'.

What happens when, say, button1 is clicked, is determined by what you put in the 'Button1–Click()' subroutine, which becomes available when the Button1 is added to the form. All 'controls' offer subroutines for all the possible events that can happen to them. And the remainder of the language is comprehensive, too.

### Visual Basic weakness

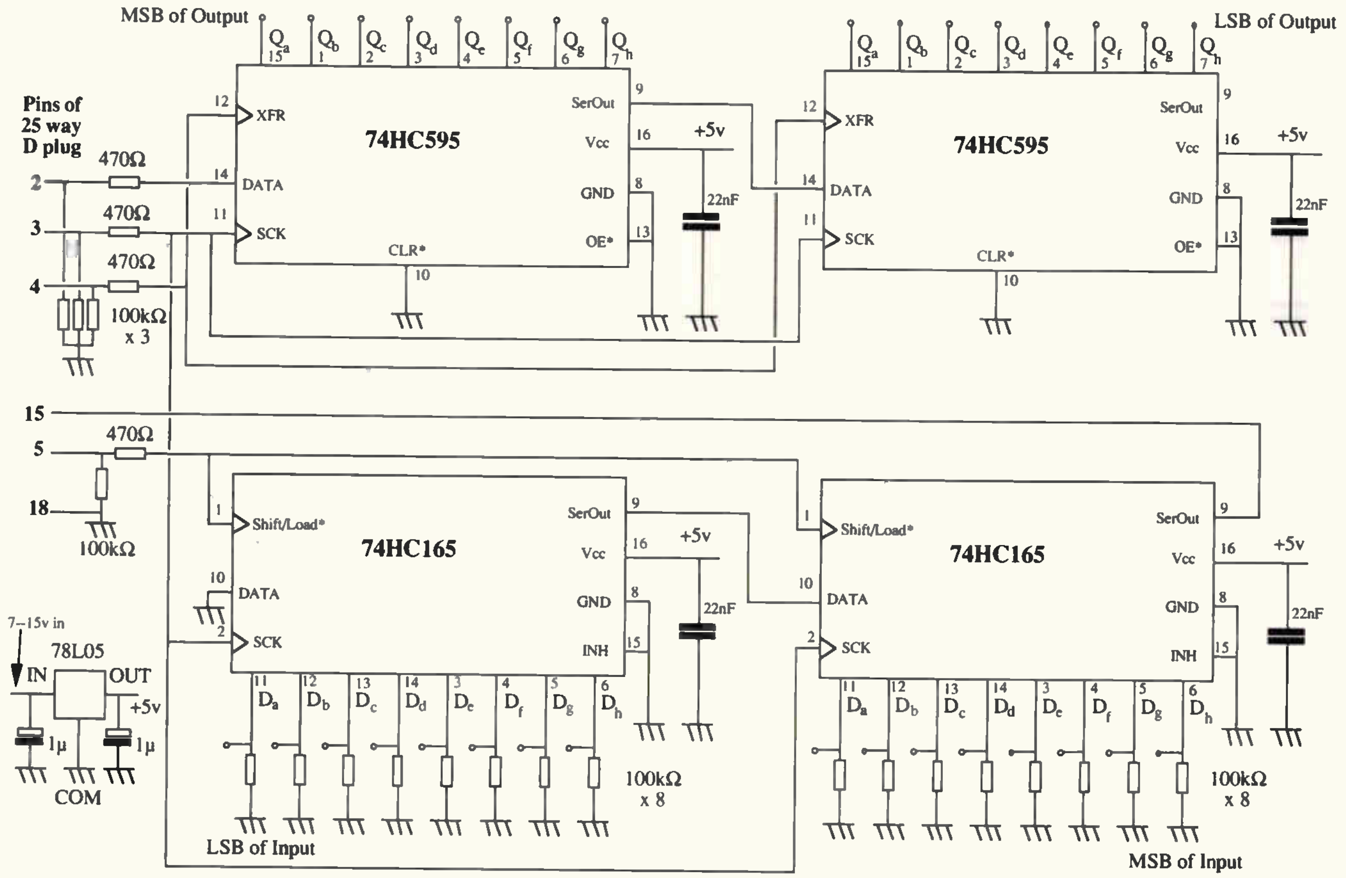
A problem with Visual Basic is that it cannot access hardware directly; there is no equivalent to QuickBasic's INP and OUT functions, no PEEKs, POKEs or the like.

This is a disappointment. Hanging peripherals on the printer port is an honourable pastime, but doing it with Visual Basic needs an intermediate step – which is the subject of this article. The intermediate step is, in its simplest form, a dynamically linked library, or dll, which can be written in C and called from Visual Basic.

### DLL for LPT read/write

The simplest useful dll is generated from a .def file and a '.c' file, **List 1**.

A dll generated from these files is on the article disk detailed later; it is used in Visual




*Connected to a pc's LPT port, this interface can be used to clock 16-bit parallel words in both directions.*

Basic by including the line,

```
Declare i_o Lib "<full path
name>\IO8.dll" (ByVal ip As
Integer, ByVal op As Integer,
ByVal Written) As Integer
```

in the "general [declarations]" section of the forms where it is to be used, and is called by

```
Rval%=i_o(&H379, &H378, <value
to write to &H378>)
```

***List 1. The simplest useful dll is generated from a .def file and a .c file.***

IO8.c

```
#include <windows.h>
#include <stdio.h>
#include <stdlib.h>
#include <conio.h>

int FAR PASCAL LibMain (HANDLE hInstance,
WORD wDataSeg, WORD cbHeapSize, LPSTR
lpCmdLine)
{
        return 1;
}

/* the function made available to the user */

int FAR PASCAL _export i_o(int inport,int out-
port,int poked)
{
int data;
/* here are the C outp() and inp() functions */
/* at the heart of the dll */
/* write the value 'poked' to the address 'outport'*/
outp (outport,poked);
/*assign the value read from the address 'inport' to
the variable 'data'
data=inp(inport);
return(data);
}
```

IO8.def

```
LIBRARY          mylib
```

***List 2. Producing your own dll using Turbo C++ for Windows.***

To generate a dll called 'my_dll' in directory 'c:\my_dir'
Project/New Project
Select Target type Dynamic Library .DLL
Under "Project Name and Path" enter c:\my_dir\my_dll.ide
Under "Standard Libraries" select "Static" and Runtime
Open Advanced: deselect .rc; select .c or .cpp as desired.
Close Advanced
Click "OK"
Now enter the code needed for the dll you want to write in the file my_dll.c or my_dll.cpp.

## 16-bit input and output

The virtue of the dll in List 1 is that it allows writing of eight bits, (or twelve bits including the port at base address+2, see the appendix) and reading five bits, from the printer port with no added hardware. For a wider i/o port, you need to use serial techniques and external circuitry, as in the diagram.

Output data are shifted into two cascaded *74HC595* dual-rank shift registers; when the data are in place, a transfer pulse moves them to the output pins, thus avoiding transient changes as the data are clocked in.

Data for input are loaded into two cascaded *74HC165* parallel in/serial out shift registers, and then clocked into the pc. A total of five signals to and from the pc are needed – namely clock, data, data output strobe and data input strobe from the pc, and data input to the pc.

## Writing your own dlls

No C compiler is needed to use the dlls on the disk available. Those of you with Windows C compilers may want to write your own dlls, however. Here's a brief outline of how to do so using Turbo C++ for Windows.

List 2 shows how to generate the dll which is placed in a specific directory. By default the .def and .c files will be named my_dll. The trivial example already given will serve as a .def file. To add further source files, right click the mouse on the dot to the left of the .dll icon in the Project window. Select Project/Build All to generate the dll.

You can safely ignore the warnings about the variables hInstance, wDataSeg, cbHeapSize and lpCmdLine being unused. Alternatively, you can add #pragma argsused just after the #includes. The _export keyword is of course not needed for functions internal to the dll which are not visible to the dll user.

If you're using C++ rather than C, you'll need to add extern 'C' to the start of the definitions of exported functions, eg,

```
extern "C" int FAR PASCAL
_export i_o(int inport,int
outport,int poked)
```

## Printer port address and connections

The printer port's address can be found using the MSD.EXE utility found in the MSDOS 6 folder. Address $378_{16}$ is the usual base address, where there's an eight bit output port. A five bit input port is at base address+1, and a four bit output port at base address+2. Table 1 gives the connections to the 25-way printer socket. ■

I am grateful to Cambridge Consultants for permission to publish this article – in particular to Paul Cox for help in the generation of dlls.

***Table 1. Printer port pins together with addresses These numbers correspond to those on the left-hand side of the circuit diagram.***

| Pin | Address | Bit | I/O |
|---|---|---|---|
| 1 | 0x37A | 0 | Out |
| 2 | 0x378 | 0 | Out |
| 3 | 0x378 | 1 | Out |
| 4 | 0x378 | 2 | Out |
| 5 | 0x378 | 3 | Out |
| 6 | 0x378 | 4 | Out |
| 7 | 0x378 | 5 | Out |
| 8 | 0x378 | 6 | Out |
| 9 | 0x378 | 7 | Out |
| 10 | 0x379 | 6 | In |
| 11 | 0x379 | 7 | In(inverted) |
| 12 | 0x379 | 5 | In |
| 13 | 0x379 | 4 | In |
| 14 | 0x37A | 1 | Out |
| 15 | 0x379 | 3 | In |
| 16 | 0x37A | 2 | Out |
| 17 | 0x37A | 3 | Out |
| 18 | Earth | | |
| 19 | Earth | | |
| 20 | Earth | | |
| 21 | Earth | | |
| 22 | Earth | | |
| 23 | Earth | | |
| 24 | Earth | | |
| 25 | Earth | | |

### Software on disk

A disk supporting this article is available. It contains two directories, one for the 8-bit, no-added-hardware port and one for the 16-bit port using added circuitry as shown in the diagrams. Each of these directories is further split into two directories: C_bits containing the dll and the source files needed to make it, and VB_bits, containing the Visual Basic program to use the dll.

The Visual Basic programs are the simplest ones that will demonstrate the dll's abilities. Both use an array of check boxes to define the state of the output lines: both include a software timer. In the 8-bit version, the inputs are read, and the outputs written, at the end of each timer period; the 16-bit version writes the outputs when the boxes change state, and reads inputs at the end of each timer period.

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# ACTIVE

## Discrete active devices

**Pin-diode switches**. KDI *SWX Series* miniature, high-isolation pin diode switch modules are for use in cellular and PCS base stations, providing up to 60dB of isolation to guard against lightning strikes and switching spikes. The range covers the 200-2400MHz range, isolations being from 24.5dB to 51dB at 2GHz, according to type, with insertion losses of 0.6dB and 0.9dB respectively. Power handling lies between 20dBm and 35dBm, depending on reverse bias. Packages have a full ground plane underneath, so that board space there can be used for other things. Anglia Microwaves Ltd. Tel., 01277 630000; fax, 01277 631111.

**Miniature flash cards**. *Flash Miniature Cards* by Smart come in 2Mbyte and 4Mbyte form in the size supported by the Miniature Card Implementers' Forum. They are essentially matchbook-sized flash memories to store voice, images or data that fit into an adapter to go into a pc or notebook card drive slot, complying with MCIF specifications and working from 3.3V and 5V supplies. Access time is 100ns at 5V. One application envisaged is storage in digital still cameras. Smart Modular Technologies. Tel., 01908 234030; fax, 01908 234191.

## Microprocessors and controllers

**Metering controller**. Using 400μA (active) and 1.6μA (standby), TI's *MSP430* metering microcontroller family has several low-power modes down to 0.1μA. The device contains a 16-bit risc cpu, a range of programming and memory options, a 14-bit a-to-d converter and an lcd driver. There are 51 instructions with seven address modes and the structure allows register-to-register instructions to be carried out in 300ns at 3.3MHz clock speed, each instruction being usable with each address mode. Memory options include rom, eprom and otp versions from 4K to 16K capacity, and either 256 or 512byte of ram. *MSP430x310* is designed for use with resistive sensors, providing dual-slope conversion, and the *320* version includes a full, six-input successive-approximation converter. Arrow-Jermyn. Tel., 01234 270027; fax, 01234 214674/791501.

**8-bit microcontroller**. An 8-bit microcontroller by Toshiba, the *TMP87PM29U* has 32Kbyte of one-time-programmable memory and 1Kbyte of ram. It works on 2.7V at low power and is therefore well suited to battery equipment using lcd screens. It has an lcd driver, a uart, an a-to-d converter, an 8-bit timer, four 8-bit timers and interval and watchdog timers and is also available in masked-rom versions with 16, 24 and 32Kbyte of rom. Toshiba Electronics UK Ltd. Tel., 01276 694600; fax, 01276 694800.

## Power semiconductors

**Fast, 7A/600V igbts**. Unusually, Harris's *HGTP7N60C3* insulated-gate field-effect transistor is happy working in the frequency range 50-100kHz, with losses down to 600μJ. It is rated at 7A, 600V at 110°C (14A at 25°C) and fall time when switching 7A at 480V at 150°C is 275ns. Harris Semiconductor UK. Tel., 01276 686886; fax, 01276 682323.

# PASSIVE

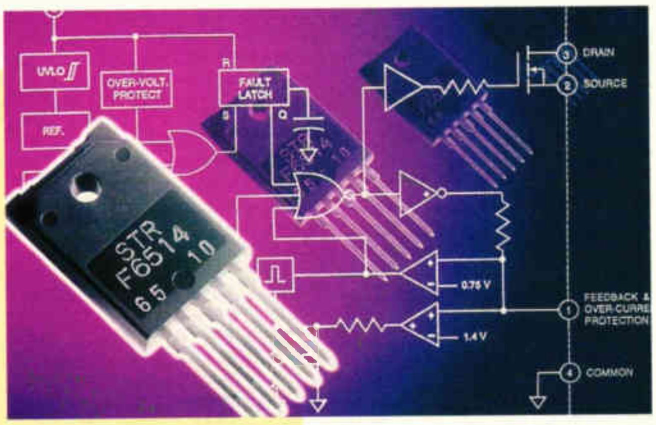
## Passive components

**Multi-gang pots**. *ECO* 16mm conductive-polymer potentiometers, made with recyclable plastic, are now available in multi-gang versions. Compared with the company's metal-cased models, the plastic construction confers the advantages of compactness, the provision of a locating spigot for angular alignment, better sealing and lower cost. A notched backplate accepts a spring clip to replace the normal nut and washer fixing. Dual-gang units can have matched tolerances for stereo or have different values and laws, the range of values being 1kΩ to 1MΩ, 0.25W for linear types and 4.7kΩ to 470kΩ, 0.12W for the non-linear variety. All can be fitted with rotary switches. Omeg Ltd. Tel., 01342 410420; fax, 01342 316253.

**Precision resistors**. Rhopoint offers a range of conformally coated metal-foil resistors that exhibit a temperature coefficient of ±2.5ppm/°C. *Alpha FL* components have a thickness of 6.2mm and possess a long-term stability of ±0.0005% per 1000h over a temperature range of –25°C to 155°C. Power ratings are 0.125W for the *FLA* and *FLC* types, while the *FLB* is rated at 0.25W. Values are 5Ω to 150kΩ in tolerances down to ±0/02% can be supplied, but for off-the-shelf ordering, the range is 50Ω to 100kΩ at ±0.1%. Rhopoint Components Ltd. Tel., 01883 717988; fax, 01883 712938.

**Resistor networks**. *MiniNet* silicon-based resistor networks are said to be the smallest such devices currently available, being some 25-30% smaller than ordinary ones. They are made in ic-type packages and consist of a thin film of tantalum nitride on a silicon substrate. Values range from 10Ω to 100kΩ in tolerances from ±5% to ±1% and temperature coefficients of ±250ppm to ±50ppm. Maximum voltage is 50V dc and power rating 0.1W-0.9W at 70°C. Arrow-Jermyn. Tel., 01234 270027; fax, 01234 214674/791501.

**Miniature capacitors**. *CapXon* miniature electrolytics are now available in the UK. There are seven voltage ratings between 4V dc and 50V dc in values between 0.2μF to 220μF and in sizes from 3mm diameter by 5mm long to 6.3mm diameter by 5mm long, the latter being for a 220μF, 4V type. Europa Components & Equipment plc. Tel., 0181 953 2379; fax, 0181 207 6646.

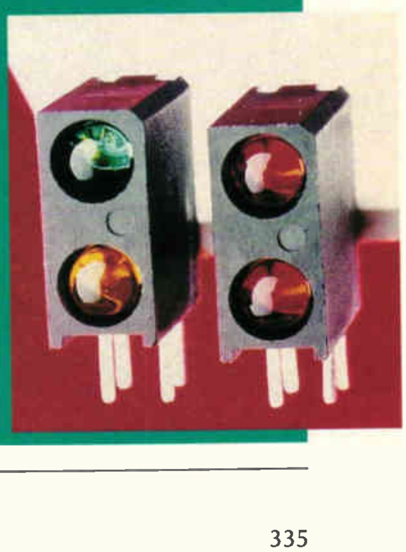



## Mixed-signal ics

**Switched-mode ic**. Allegro's *STR-F6500* is a switched-mode power-supply ic for requirements in the 30-300W range. It contains an off-line mosfet power switch and controller in a 5-pin package forming, with few external components, a complete supply module. This is a flyback converter with quasi-resonant soft switching to reduce switching losses and conducted and radiated interference. Protection is undervoltage lockout with hysteresis, overvoltage shutdown and thermal shutdown to protect the ic and following components. Switching frequency is reduced during startup to control dissipation, all startup components being included. Allegro MicroSystems Inc. Tel., 01932 253355; fax, 01932 246622.

## Displays

**Backlighting leds**. From Dialight, the *553-22xx-100* led indicator, which is optimised for backlighting use, being space-saving in that two leds are mounted in one assembly. To reduce stray light from the assembly to other positions and to obtain maximum output on the viewing axis, the housing is extended and the leds fitted with tinted, non-diffused lenses. Leds in red, yellow or green produce 12mCd at 10mA. Gothic Crellon Ltd. Tel., 01734 788878; fax, 01734 776095.



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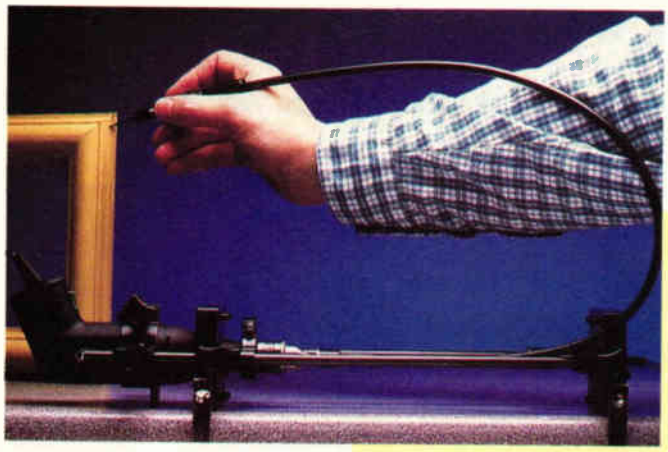
## Connectors and cabling

**Optical connectors.** Framatome has a new series of lightwave connectors for lans, fibre cable management and distribution, ATM and premise installation. They incorporate a dome-shaped zirconia ferrule and exhibit low insertion loss, simple connection and nickel-plated zamack bayonet coupling. Cable diameters accepted are 0.9mm-2.8mm with a fibre diameter of 126µm, variability after connection being under 0.2dB after 1000 test cycles. Cable retention is 15.9kg and temperature stability ±0.1dB between –40°C and 80°C. Assemblies are available. Framatome Connectors UK Ltd. Tel., 01582 475757; fax, 01582 476203.

**Power connectors.** Rendar has a full range of power connectors meeting EN60 320 and rated at 10A, 250V ac, with variants for the US being rated at 15A, 125V ac. Connectors in the range are approved to UL, CSA, VDE and BSI and any not covered by international safety regulations are tested to BS 5733. In the range is a variety of inlets with choices of mountings, rewireable plugs and connectors and outlets. There are also the *Twinbloc* and *Quadbloc* multi-outlet blocks and the *Stripbloc*, which carries power and signal lines. Rendar Ltd. Tel., 01243 866741; fax, 01243 841486.

**Cable screen clamps.** Emc requirements have made for an increase in the usage of screened cables, and focused attention on the need for a reliable and simple method of making connection to the screen. Wieland Electric now has three sizes of clamps to a busbar fixing rail for use with cable of 7-16.5mm in diameter, the clamps having stainless steel contact springs to avoid damage to the screen and to provide corrosion resistance. The rails are insulated and can be fixed directly to a panel and can also be used as pure screen connectors remotely from the terminals. Wieland Electric Ltd. Tel., 01483 31213; fax, 01483 505029.

**VME backplane.** Vero has started production of backplanes to the latest draft of the VME64 Extensions standard. Twelve-layer stripline backplanes come in widths of 7-20 slots with smt terminations for lower crosstalk. J1 and J2 slots have the new 160-pin, 5-row DIN connectors, which are compatible with existing 3-row, 96-pin connectors, and an optional 2mm J0 connector has an extra user-defined 95 pins; a further 35 ground returns are available. There are a 3.3V and two user-defined ±V1 and ±V2 rails, which can be used together to give 48V telecomms supply. Total power is about 2kW. Vero Electronics Ltd. Tel., 01489 780078; fax, 01489 780978.



**Drill/lathe/drive-shaft kit.** Minicraft's lathe and drill kit, the *MB6001*, is now sold with a free flexible drive shaft, the *MB720*, until the end of April. The whole kit, which costs £139.99, consists of the 100W drill; a variable-speed transformer which is usable with all Minicraft 12V tools; a lathe attachment, three chisels and cutting, polishing, grinding accessories; and the drive shaft. Minicraft. Tel., 01388 420535; fax, 01388 817182.

**400 contacts on double Eurocard.** *Erni* has an interconnection method that provides up to 400 contacts on a double-width Eurocard using the standard DIN format. This is done by combining two *Erni E160* connectors, which each have five rows of 32 pins, with an *Erni E80* of five rows with 16 pins a row to give a continuous 2.54mm pitch for a standard layout. Features include early make/last break of 0.8mm for male contacts, precentring for male connectors; press-fit termination; and wave soldering. Radiatron Components Ltd. Tel., 01784 439393; fax, 01784 477333.

**Cordsets.** Clarke Cable's mains cordsets are available from Roxburgh. These are 100% tested, 2m cables with a range of UK and European standard connectors, various cable colours and other terminations being supplies as needed. Roxburgh Electronics Ltd. Tel., 01724 281770; fax, 01724 281650.

## Filters

**Solder-in emi filters.** New emi filters by Syfer are suitable for soldering directly to a panel, are smaller than threaded equivalents and are shorter. The type for soldering into a 3.5mm hole has capacitance values to 33nF, while the 5.8mm type goes to 470nF. Voltage rating is 500V dc and current rating 10A. Syfer Technology Ltd. Tel., 01493 440047; fax, 01493 440048.

**Emi filters.** These bidirectional chip filters from Murata, the *EMIFIL NFMM839R* series, are for use on clock or interface lines and possess a smooth change of impedance with frequency, reducing waveform distortion and reflection. There are two cut-off frequencies: 20MHz and 50MHz, insertion loss being typically 8dB at 100MHz and 20dB at 500MHz for the 20MHz device. Minimum insulation resistance is 1GΩ and the filters are rated at 50V dc, 25mA. Murata Electronics (UK) Ltd. Tel., 01252 811666; fax, 01252 811777.

## Hardware

**Fan.** Miniature radial fans from Papst in the *RE38 Series* mount straight onto a pcb and are meant for localised cooling. They operate from 12V dc at temperatures between 40°C and 90°C, supplying 1.5 or 3.5ft$^3$/ minute, depending on the model. Challenger Components Ltd. Tel., 01795 477255; fax, 01795 477259.

## Test and measurement

**Portable dsos.** *TDS200 Series* oscilloscopes from Tektronix are low-cost, portable digital storage oscilloscopes with backlit lc displays, the reason for a back-to-front dimension of 11cm. Tek's Digital Real-time technology provides a response similar to that of an analogue instrument. Bandwidths are in the 60-100MHz range, sampling being at 1Gsample/s simultaneously on both channels. The user interface (controls) are similar to those of analogue types, but with a collection of automatic measurement features, storage and instrument setups; automatic peak detection reduces the possibility of aliasing. There is provision for optical communication to give hard copy output or via GPIB/RS232 to a pc. Thurlby Thandar Instruments Ltd. Tel., 01480 412451; fax, 01480 450409.

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**Function generator.** In seven ranges, the *GX245* portable function generator by Metrix covers 0.5Hz-5MHz and contains a frequency counter to measure up to 120MHz. Both internal and external sweeps are available with start/stop control in linear, log., dc level and single-shot modes. Square-wave rise time is under 40ns and less than 12ns for ttl loads. Frequency resolution is 0.001Hz at the lower frequencies, output frequency being shown by a 5-digit lcd. Metrix Electronics plc. Tel., 01384 402731; fax, 01384 402732.

**40GHz spectrum analysis.** Rohde & Schwarz announces two new spectrum analysers: the 26.5GHz *FSEM* and the *FSEK* for 40GHz, both being modular in form to allow customisation for a number of uses, although all models in the *FSE* range include as standard functions for work on digital radio and television measurements in development, production and service. Synchronised tuning up to the 5ms full span sweep ensures high accuracy at every point and the gap sweep function and 200ns/division resolution at zero span allows pulse rise and fall time measurement simultaneously. Phase noise is typically –128dBc/Hz at 10kHz offset. Rohde & Schwarz UK Ltd. Tel., 01252 811377; fax, 01252 811447.

**Four-channel temperature monitor.** *Tempscan T100*, intended for small temperature-controlled stores, incorporates variable high and low alarm limits for each channel, defrost and door-open inputs and selectable recording intervals from 15m to 1h, operation being controlled by a lockable function switch. An internal tally-roll printer provides reports and functions are selected by either front-panel keypad or, optionally, by an RS-232 interface to a computer using software supplied or users' own. Danesbury Data Systems. Tel., 01438 712041; fax, 01438 712900.


**Rail-mounted kWh meter.** *RM303* from Northern Design mounts on a DIN rail, six modules wide, and provides a readout on a large backlit lcd to better than IEC 1036 Class 1 for both single and three phase inputs, also offering an optional pulse output, as required for building energy management applications. It is a single-function instrument with standard current-transformer inputs for connection to loads from a few watts to several hundred kilowatts, readings being stored in the event of a power failure. Northern Design (Electronics) Ltd.Tel., 01274 729533; fax, 01274 721074.

**Optical preamplifier.** EG&G Instruments has a new optical-input preamplifier, the *Model 5188*, designed for use as a light-to-voltage converter. Two versions exist: the *5188A*, with an InGaAs input detector for near-infrared radiation, and the *5188B*, which uses a silicon device for the visible part of the spectrum. Sensitivity extends to fractions of a picowatt with no noise degradation, to 18mW without overload. Ac and dc signal components are processed separately and give independent outputs. Input is by way of an FC/PC connector. EG&G Instruments Ltd. Tel., 01734 773003; fax, 01734 773493.

## Interfaces

**Laptop-to-Fieldbus.** From National, the *PCMCIA-FBUS*, which is a Foundation Fieldbus interface for pcs running Windows NT and having PCMCIA slots; the interface includes NI-FBUS driver software for Win NT. There is also a network 'configurator' – a 32-bit Windows application to deal with the configuration of fieldbus segments. National Instruments UK. Tel., 01635 523545; fax, 01635 523154.

## Literature

**Microcontroller design guides.** Toshiba's three new design guides cover 1-bit, 8-bit and 16-bit microcontroller families, providing application examples and lists of available development software. Toshiba Electronics UK Ltd. Tel., 01276 694600; fax, 01276 694800.

**Virtual instruments.** National Instruments has a new catalogue, the 1997 Instrumentation Reference and Catalogue, which contains nearly 700 pages and is free. National is well known for its range of pc-based instruments and the publication offers tutorials on data acquisition, GPIB, VXI and automation in industry, in addition to the normal functions of a catalogue. National Instruments UK. Tel., 01635 523545; fax, 01635 523154.

## Materials

**Emc kit.** A kit of materials from Vacuumschmelze, the EMC KIT, consists of 17 toroidal cores and 22 common-mode chokes using high-permeability, nano-crystalline *Vitroperm 500 F*, to assist engineers to design small, flat mains filters for the 1-25A (single-phase) or 3-40A (three-phase) ranges. The kit also contains a disk with Excel Work Sheet VACSIM 3.0 to help with dimensioning chokes and simulating insertion loss in a 50Ω system between 10kHz and 100MHz. Vacuumschmelze GmbH. Tel., 0049 61 81/38-26 29; fax, 0049 61 81/38-28 60.

## Power supplies

**Switching regulators.** Micrel Semiconductor has two new regulators, the *MIC2570/1* one and two cell boost regulators, both being constant duty-cycle, gated-oscillator types. The *2570* is for two-cell working from 1.3V to 15V input, the *2571* being for single-cell use and works on inputs down to 0.9V. This one is in a new 8-lead Mini8 package, which is less than half the size of SO-8s. Both devices have selectable output of 2.85V, 3.3V or 5V or adjustable output up to 36V. An n-p-n switch in the unit avoids the need for a series-pass component for peak inductor currents to 800mA. Micrel Semiconductor Europe. Tel., 01635 524455; fax, 01635 524466.

**Earth tester.** PIDA members can now supply the Norma *Handy Geo*, a compact, handheld, battery-powered tester for two-pole and three-pole earth resistance and noise voltage measurement. Its large lcd provides legends and an analogue scale, backlighting being switchable. The instrument will detect external ac and dc volts, will define probes and has an adjustable limit. PIDA. Tel. and fax., 0756 799737.

**15 and 30W dc-to-dc converters.** Improved versions of Vero's *DC15100* and *DC30100* converters exhibit input tolerance of –25% to 50% about nominal inputs of 12V, 24V or 48V. Single and dual regulated outputs of 5V, 12V, ±12V and ±15V are available at efficiencies of around 85%, with cmos/ttl compatibility and full rfi screening. Both types meet the ETSI for telecomms. Vero Electronics Ltd. Tel., 01489 780078; fax, 01489 780978.

**Programmable supply.** TTi's *TSP3222H* is a GPIB-controlled supply giving dual independent 0-32V, 0-2A outputs. Rapid response to output demand, regardless of load current, is provided by active circuitry that sinks current when required. All functions, including output configuration, overvoltage trips and meter damping are bus-controlled and outputs are readable via the bus to a 12-bit resolution. Each output operates in constant-V or constant-I mode with auto crossover and mode indication; serial or parallel combination is programmable. There is also keyboard setting for all functions with memory to save up to 25 settings. Thurlby Thandar Instruments Ltd. Tel., 01480 412451; fax, 01480 450409.

**Rechargeable batteries.** Thirteen models of *Eleckson* batteries cover the range 6V, 1.3Ah to 12V, 44Ah and 0.33kg to 14kg, most popular

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sizes being included. Lower-power types use standard push-on terminations, with heavier nut-and-bolt fastening for the larger batteries. There is no corrosive gas discharge and the batteries are suitable for constant, float charge or cyclic use. Camden Electronics Ltd. Tel., 01727 864437; fax, 01727 855400.

## Radio communications products

**Superhets at superegen prices.** Low Power Radio Solutions has introduced the *SuperReceiver* – a superhet for low-power links using the Plessey *KESRX-01* chip. It meets the 2nW emc limit under RES0908 and is made in the same sil package used by the earlier superegen. receiver. Frequency is either the pan-European 433.92MHz or the UK 418MHz, both crystal-controlled. There is a received signal-strength indicator pin and the unit is meant for use in battery-powered systems, taking 2.5mA when active. Data rate is 10kb/s and sensitivity better than –103dB. Low Power Radio Solutions Ltd. Tel., 01993 709418; fax, 01993 708575.

## Protection devices

**Resettable fuses.** *PolySwitch* resettable fuses from Raychem come in five ratings from 3A to 11A, each with a 16V, 100A surge rating. They are conductive polymer devices with metal electrodes, the polymer increasing its resistance in the presence of overload and latching in this state until the fault is removed, when the device resets after cooling down. Raychem Ltd. Tel., 01793 572692; fax, 01793 572209.

Ferrite cores. Murata cores for emi suppression provide 'excellent noise suppression' which is effective at frequencies up to 500MHz. Data lines may be passed through the cores or wound round them several times. Surtech Interconnection Ltd. Tel., 01256 51221; fax, 01256 471180.

## Switches and relays

**Relay module.** Matsushita has a DIN-rail-mounted safety relay module that is provided with quick-connect terminals, power indication and the choice of a range of operating voltages. These are rotating-armature *SF2/4* relays for safe switching in the presence of malfunction or contact problems. Each module has two or four sets of mechanically interlocked normally open or normally closed contacts in a sealed package, contacts being rated to break 1500VA at up to 44V, 6A. Matsushita Automation Controls Ltd. Tel., 01908 231555; fax, 01908 231599.

**Load-break switches.** Crompton Greave has a new series of load-break switches with a new handle having a positive stop to prevent the switch overthrowing. These UL/CSA-approved switches have isolated double-break contacts with seals to IP65. Thirty variants offer three, four or five poles and current handling from 25A to 63A. Front and base mounting is available, with locking facilities, and there is a front-panel marking system for accurate alignment of door interlock handles. D S Hodgson Ltd. Tel., 01923 859191; fax, 01923 859794.

**GPIB-controlled relay module.** ICS Electronics has produced the *Model 4864* GPIB-to-relay interface for the ATE market, offering different combinations of contacts and isolated inputs to control external devices from a GPIB bus. There are 16 outputs, all of which can be controlled individually, run as a single or multiple scanner or all switched at the same time. Eight isolated inputs are usable to sense signals or contact closures or to verify an external response to a control output. Three types are produced: the *4864-11* has 0.5A contacts; *4864-12* 1A types; and *4864-14* solenoid/relay driver outputs to connect larger relays. Amplicon Liveline Ltd. Tel., 0800 525 335 (free); fax, 01273 570215.

**Miniature snap switch.** Cherry *Hirose* snap switches take up 10% of the space normally needed for a switch of this type, measuring 12.8 by 13.8 by 5.8mm. The range includes versions for 50mA to 3A, with silver alloy, silver or gold contacts. A variety of actuators is available and straight, left or right terminations. Cherry Electrical Products Ltd. Tel., 01582 763100; fax, 01582 768883.

## Transducers and sensors

**Pressure sensors.** Schaevitz *P3000* pressure sensors from Lucas are meant for use in the measurement of very low vented gauge, absolute or wet/dry differential pressures in a variety of fluids, the lowest range being 0-5mbar and the highest 0-5bar. The pressure-sensing element includes an all-welded Ni-Span C capsule for low hysteresis and constant scale factor with temperature, a linear variable differential transformer measuring the displacement of the capsule. Lucas Control Systems Products. Tel., 01753 537622; fax, 01753 823563.

**Led shaft encoder.** Using red, green or orange 31-led arrays, the 20mm diameter, low-profile shaft encoder from ALPS provides 15 pulses per revolution for each phase (two click, one pulse), having an expected life of 15,000 revolutions at 500rev/hour. Operating current is 10mA. Roxburgh Electronics Ltd. Tel., 01724 281770; fax, 01724 281650.

## Vision systems

**Cctv Rx/Tx.** *VideoWave* video transmitter and receiver are low-power, single-band components that may now be used without licensing. The system provides a real-time, secure radio link using a unique, scrambled, monochrome closed-circuit tv output at a fraction of the cost of other methods. Units are for fixed or mobile use from 12V dc, using one-to-one, multiplexed or broadcast video transmission. Both units measure only 160mm by 90mm by 60mm. Radio Data Technology Ltd. Tel., 01376 501255; fax, 01376 501312.

## Computers

**Fireproof computer.** Well, perhaps not, but the *TMI Hardbody* is a lightweight, handheld pc that will take the kind of punishment development engineers have nightmares about. It has a splash-resistant case, a pen-based interface (you use a pointer instead of a keyboard) and a long-life battery. It will survive a 20g shock for 6ms, 2g vibration between 5Hz and 200Hz and 0-95% non-condensing relative humidity. Temperature range is –10°C to 50°C. Insides consist of a 66MHz 486DX, 32Mbyte of ram, a 260Mbyte hard disk and a VGA lcd with a 2048 by 2048 touch screen. There are two PCMCIA slots, two RS-232 ports and comms ports for peripherals, rf lan and wan connection is via optional adaptors. Crellon Microsystems. Tel., 01734 776161; fax, 01734 776095.

# COMPUTER

## Data acquisition

**96-channel analogue VME input.** Newest member of Pentland Systems' *VGX* family is the *VGD4*, which consists of 96 12-bit analogue-to-digital converters in two VME slots to give high channel-density simultaneous sampling, accuracy being maintained by a calibration rom. Data transfer can be by VME or VSB or straight to dsp modules by way of *TMS320C4X* comms ports or front-panel data ports. Pentland Systems Ltd. Tel., 01506 464666; fax, 01506 463030.

## Data communications

**Lan/wan transceiver.** Developed by Triquint in the US, the *TQ8105*

*Sonet/SDH* atm transceiver runs at 622Mb/s, dissipates 2.3W and is contained in an 100-pin JEDEC quad flatpack. Its claim to fame stems from the provision of three alarm signals which indicate imminent loss of data before it happens. Flags are waved if there is a loss of local reference signal; at a loss of received signal after 128 zero transitions; or if the data has started to drift because of trouble at the other end. It is compatible with ecl, pecl or ttl clocks running at between 19.44MHz and 155.2MHz and it holds its end up in temperatures between –40°C and 125°C. Pronto Electronic Systems Ltd. Tel., 0181 554 5700; fax, 0181 554 6222.

## Software

***Datataker* programmer.** Data Electronics' *Datataker* series of data loggers is now augmented by the introduction of a Windows programmer and supervisor to retrieve and present its results. *Delogger Pro* offers the choice of a gui or text window for entering commands, data being shown as charts or in text form. Programming requires little use of the keyboard, most being carried out by clicking on icons, all without the presence of loggers. The program has its own relational database with up to eight filter parameters to create reports and will work with other databases such as Foxpro and Microsoft Access for more complicated work. Charting functions show data in real time and the package also supports a modem manager for remote data collection. Data Electronics. Tel., 01462 481291; fax, 01462 481375.

**Datacomms analyser.** *COM-Watch 2000* allows a user to visualise and analyse data communication simultaneously on up to 16 channels and will communicate with a device to test its data; test programs may be written in the Script command language. The facility is used to start, debug and service links and in software development. In its passive mode, *COM-Watch* uses the RS-232 adaptor to see data communication, trigger functions determining which data to monitor, subsequent analysis being concerned with crc calculation, checksums and searching for patterns, strings and signal errors. Amplicon Liveline Ltd. Tel., 0800 525 335 (free); fax, 01273 570215.

**Analogue circuit simulator.** *SIMetrix*, from Newbury Technology, is a Windows-based circuit simulation package costing £245. Features include an integrated circuit editor with multi-level undo, waveform analysis and real-time waveform display. It is based on Spice 3 and supports transient, dc, dc sweep, ac, noise and transfer function analysis and recognises lossy transmission lines, arbitrary sources and GaAs fets.The model library contains 1300 devices, a new mosfet model being designed for vertical devices with non-linear gate/drain capacitance. Newbury Technology Ltd. Tel., 01635 966395; fax, 01635 868322. ■


**Development and evaluation**
***PIC* emulation.** *ICEPIC2* from RF Solutions is a modular in-circuit, real-time emulator, Windows-based, for all types of Microchip's PIC microcontrollers at up to 25MHz. Code can be debugged at source level in assembler or C, a 4K (expandable to 8K) hardware trace buffer being provided. There are unlimited hardware trigger break points on any address or range of addresses and the emulator performs single steps or procedure steps. Standard 8K of *PIC16CXX* emulation memory is expandable to 16K. Units are complete with power supply, RS232 interface and software. RF Solutions Ltd. Tel., 01273 488880; fax, 01273 480661.

# Resistors in C

**Calculating the value of parallel resistors normally involves a chart-type calculator or an electronic calculator and time-consuming equations. John Lavender describes an alternative solution offering convenience, speed and – above all – accuracy.**

Written in 'C', this short program calculates series and parallel combinations of standard value resistors for any required value with an accuracy of less than 0.25%.

There many reasons for using series or parallel resistor combinations. Achieving voltage and power ratings are not the least of these. But when a non-standard value is required, or the required standard value is not to hand, parallel or series resistor combinations are the only solution.

Whereas series pairs can usually be worked out using mental arithmetic, for most people, parallel pairs require at least a pen and paper. There are some helpful rules of thumb, but if you don't know them, or can't remember them, the only resort is lots of calculations.

The two better known formulae used to calculate parallel resistance are, for two resistors,

$$R_t=(R_1\times R_2)/(R_1+R_2)$$

and for multiple resistors,

$$1/R_t=1/R_1+1/R_2+1/R_3+...+1/R_n$$

The first formula may be transposed to give,

$$R_1=(R_2\times R_t)/(R_2-R_t)$$

when the value of one resistor and the total resistance is known.

The second formula may also be transposed to,

$$R_t=(R_1\times R_2\times R_3...R_n)/(R_1\times R_2)+(R_1\times R_3)+(R_2\times R_3)...+(R_1\times R_n)+(R_2\times R_n)+R_3\times R_n), \text{ etc}$$

for calculators without a reciprocal function.

Having for many years used the above formulae and a parallel resistance calculator chart[1], I found that I required greater accuracy and flexibility when calculating resistor combinations. It was to this end that a short 'C' program was written that displayed a range of parallel-pair combinations within predetermined limits of the required value.

These limits are referred to as the accuracy range – or perhaps more precisely the 'inaccuracy range'. This is the degree of variation from the required value; the larger the variation, the greater the number of combinations displayed.

The reason I decided to display a range of combinations rather than simply the most accurate is that it gives you the opportunity of selecting,

- The most accurate combination,
- A pair with close values for current sharing – or voltage sharing, in the case of series pairs,
- A high/low value combination for applications where trimming may be required, or,
- The values of resistors on hand.

The program was found to be invaluable, saving many hours of manual calculations. Over a period of time the original program has been modified, added to, and generally improved, both series and parallel combination pairs being calculated.

*Fig. 1. Simulation of a screen produced using the c resistor calaculation program.*

```
Enter EIA range - 96, 48, 24, 12, 6. 96

Enter resistors percentage tolerance. (e.g. 1) .1

Enter accuracy range. (e.g. .25) .025

Enter value of required resistor in ohms or 0 (ZERO) for change. 4440

121R + 4k32 = 4441.0000 0.023%, 4436.56 to 4445.44 –0.077 to 0.123% error
221R + 4k22 = 4441.0000 0.023%, 4436.56 to 4445.44 –0.078 to 0.123% error
1k43 + 3k01 = 4440.0000 0.000%, 4435.56 to 4444.44 –0.100 to 0.100% error
1k5 + 2k94 = 4440.0000 0.000%, 4435.56 to 4444.44 –0.100 to 0.100% error
4k53 || 221k = 4439.0103 –0.022%, 4434.57 to 4443.45 –0.122 to 0.078% error
4k53 || 226k = 4440.9839 0.022%, 4436.54 to 4445.42 –0.078 to 0.122% error
4k75 || 68k1 = 4440.2881 0.006%, 4435.85 to 4444.73 –0.094 to 0.106% error
4k99 || 40k2 = 4438.9907 –0.023%, 4434.55 to 4443.43 –0.123 to 0.077% error
5k49 || 23k2 = 4439.4561 –0.012%, 4435.02 to 4443.90 –0.112 to 0.088% error

Enter value of required resistor in ohms or 0 (ZER0) for change.          _
```

## Any EIA range can be selected...

Any EIA range from E6 to E96 can be selected, and the calculation parameters of resistor tolerance and accuracy range may be varied. Maximum and minimum resistance, due to resistor tolerance, is displayed both in ohms and as a percentage difference from the required value.

Another feature that has been added is that the resistor values are displayed in the generally accepted form of 0R22, 6R8, 10R, 560R, 1k2, 47k, 330k, 1M0, etc., which makes for easier reading. Figure 1 shows a typical screen display from thsi program. The listing for this program is beyond the scope of this article, but the program is available, as detailed later.

**List 1** is a modified version of the original program. It is easy to use, and calculates series pairs as well as the parallel combinations. The range of resistor values used in the calculations are the E24 values from 0.01Ω to 91MΩ, which covers the majority of the readily available resistor values.

The accuracy range is pre-set by the 'percentage=0.25' declaration at the end of line 7 of the listing. This value can be changed to suit your requirements, but I have found 0.25% to give the best range of results.

In use, the program could not be simpler. Load the program, enter the required resistor value, in ohms, hit the enter key and the results appear on screen. Other values are entered as required, then, when finished, press the zero key to exit the program.

If more than 24 combinations are found, "MORE –" is displayed at the bottom of the screen. Hit a key and the next screen of combinations is displayed.

Series combinations are displayed in the form of,

3300.00+6800.00=10100.0000 0.0000% error.

and for parallel combinations:

3300.00||6800.00=2221.7822 –0.0098% error.

Although this program will run on any pc compatible, it is advisable to use at least a 486DX. This is because the program makes some 57,600 sets of calculations for each required value.

Calculations are made for every resistor value, paired with every value for both series and parallel combinations. A lesser pc will take several minutes to run through this number of calculations.

For those of you who do not have access to a 'C' compiler, a disk with a DOS-executable program (E24.EXE) is available. The disk also contains an E96 version of the program (E96.EXE) and the 'C' listings of both versions. As a special offer, the executable file for the more comprehensive program referred to in the text is included on the disk for the all-inclusive price of £15. Send your request to: J. E. Lavender, 5 Shackleton Avenue, Yate BS17 4NW, enclosing a cheque or money order for £20 ■

## References


1. Hammond, M. A., Parallel resistance calculator, p45, *Electronics World* April 1962 (This is an American magazine, not related to *Wireless World*). (EIA 24 values and improved version of the 'Resistors in parallel' chart, by the same author, published on p339 of the July/August 1959 issue of *Wireless World*.


***List 1. Calculate parallel resistances in C with speed and accuracy.***

```
1     #include <stdio.h>
2     #include <conio.h>
3     main()
4     {
5        float mult"10"={0.01,0.1,1.0,10,100,1000,10000,100000L,1000000L,10000000L},
6        value"24"={1.0,1.1,1.2,1.3,1.5,1.6,1.8,2.0,2.2,2.4,2.7,3.0,3.3,3.6,3.9,4.3,
7        4.7,5.1,5.6,6.2,6.8,7.5,8.2,9.1}, r1, r2, rc, rs, rt, e, percent=.25;
8        int ra, ma, rb, mb, ctr;
9        printf("\nEnter the required value of resistor in ohms\n");
10       scanf("   %f",&rc);
11       do
12       {
13          ctr = 0;
14          for (ma = 0; ma < 10; ma++)
15          {
16             for (ra = 0; ra < 24; ra++)
17             {
18                for (mb = 0; mb < 10; mb++)
19                {
20                   for (rb = 0; rb < 24; rb++)
21                   {
22                      r1 = (value"ra" * mult"ma");
23                      r2 = (value"rb" * mult"mb");
24                      rs = r1 + r2;
25                      if (r1<=r2&&rc<=rs+(rs*percent/100)&&rc>=rs(rs*percent/100))
26                      {
27                         if (rc != r1 && rc != r2)
28                         {
29                            e = ((rs - rc)/rc) * 100;
30                            printf ("\n%.3f + %.3f = %.4f %.4f %% error.",r1,r2,rs,e);
31                            ctr++;
32                         }
33                      }
34                      rt = ((r1 * r2)/(r1 + r2));
35                      if(r1<=r2&&rc<=rt+(rt*percent/100)&&rc>=rt-(rt*percent/100))
36                      {
37                         if (rc   !=   r1 &&   rc   !=   r2)
38                         {
39                            e = ((rt - rc)/rc) * 100;
40                            printf ("\n%.3f || %.3f = %.4f %.4f %% error",r1,r2,rt,e);
41                            ctr++;
42                         }
43                      }
44                      if (ctr   >=   24)
45                      {
46                         printf ("\nMORE –");
47                            ctr = 0;
48                         getch();
49                      }
50                   }
51                }
52             }
53          }
54          printf ("\n\nENTER ANOTHER VALUE OR ENTER '0' (ZERO) TO EXIT\n");
55          scanf (" %f",&rc);
56       }
57       while (rc   !=   0);
58       return 0;
59    }
```

# Programmable logic

**Building on his earlier articles, Geoff Bostock now looks at more complex programmable logic devices involving large-scale integration.**

One approach to making programmable logic devices with a higher logic content is to integrate several small programmable-array logic ICs into one package. Different manufacturers may differ in detail in the way they do this, but they all have certain features in common. **Figure 1** shows the basic structure of a large-scale integration programmable-array logic device, or PAL. Such devices are also called complex PLDs, or CPLDs.

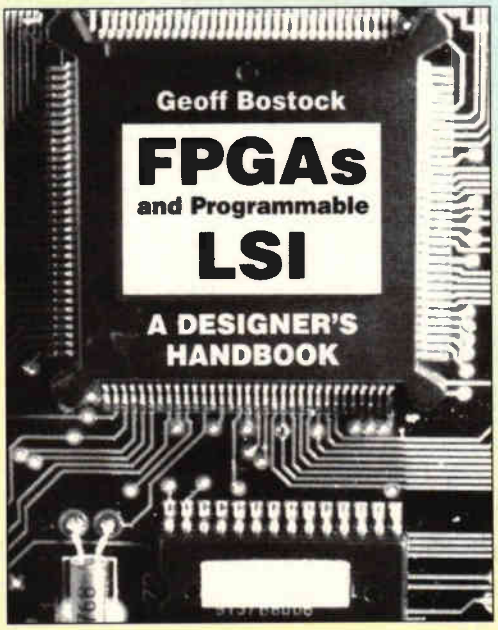
There are four blocks to consider in each device. These are the input cells, an interconnection matrix, the logic blocks and the i/o cells.

Input cells and i/o cells may be taken together as some families have no, or only a few, separate inputs and use i/o cells for this function. In general, an i/o cell connects the logic blocks to the outside world and features a ttl or c-mos interface. Most devices operate with 0.4V and 2.4V output logic levels. This means that they need level conversion if they are to drive true c-mos logic; they have high impedance inputs and can be driven by c-mos without any problem.

The outputs always have a tri-state capability which can be permanently enabled or disabled, or controlled by internal logic. They can function as dedicated inputs, dedicated outputs with optional feedback or as bussable outputs. The advantage of being able to choose the function of all inputs and outputs is that the input and output sites are not pre-determined and this gives extra flexibility to the pcb layout.

In small PLDs, every input to the device may be connected to every product term. Even a quite large PAL, such as the *22V10*, will have a manageable number of fuses with this universal connectivity. The *22V10* has 132 product terms

This article is derived from Geoff Bostock's new book 'FPGAs and programmable LSI – a designer's handbook'. The work covers designing FPGAs, large PAL structures, RAM and antifuse-based FPGAs and FPGA selection. Comprising 215 pages, this book is available by sending a postal order or cheque with a request for the book to Electronics World, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS. The fully-inclusive price is £27.50 UK, £30 Europe or £33 rest of world. Alternatively, fax your full credit card details and address on 0181 652 8956 or e-mail jackie.lowe@rbp.co.uk.




Geoff Bostock runs his own FPGA/PLD Design Consultancy, and may be contacted on 01380 828241, or by e-mail at geoff.bostock@zetnet.co.uk

with 44 potential connections to each, giving a total of 5808 fuses not counting configuration sites.

A PLD in a PLCC84 package may have 72 input/outputs; if each i/o has an average of just four product terms there will be 4 by 72 by 144, or 41472, programmable cells. This does not allow for any buried logic cells. If each i/o has a buried macrocell associated with it the total number of fuses is quadrupled.

While such a total is not outside the possibilities of technology, there are performance penalties with this approach. The more fuses there are, the more expensive the chip, and the longer it takes to program. The solution is an interconnection matrix which selects a reduced number of inputs to feed each logic block. It is best, therefore, to consider each logic block as an individual PAL within the larger PLD, each PAL being connected to the others via the interconnection matrix.

Looking at each logic block as an individual PAL simplifies the description of the architecture. Discrete PALs contain at least eight, and up to sixteen, product terms per output. Very often, only two or three terms are actually used in many applications.

This variability gives the PLD manufacturer a problem; how many product terms need to be provided with each macrocell? In many cases the answer is to incorporate some method where terms may be shared between macrocells within each logic block. In this way, if a function does not need all its available terms, they can be used by one of its neighbours.

Another area where product terms are wasted in discrete PALs is the i/o macrocell used as a dedicated input. In many CPLDs, there are two feedback paths to the interconnection matrix; one goes from the i/o pin and the other from the macrocell output. In this case, if an i/o pin is used as a dedicated input the logic terms can still be used as a buried macrocell which cannot be accessed directly from the outside. Some PLDs also include macrocells which are always buried as a way of increasing the logic capability without increasing the i/o count.

## Performance criteria

The two principal measures of performance affecting selection of a logic device are speed and power consumption, but the balance between them varies according to the application. Clearly, in a fast computer, speed is the most important factor. In a portable telephone on the other hand, power would be the controlling consideration. In many cases a compromise can be achieved, as 'it must be faster than 15ns but the less power it takes the cheaper we can make the power supply'.

Propagation delay, the most common measure of speed, is almost entirely determined by the time taken to charge and discharge the capacitance associated with the components and interconnections used to build the device. Once again, you can split a PLD into sections to see which areas are critical and reliant on the design of the chip rather than just processing.

Starting with the input, this is probably the simplest part of the PLD as its function is just to buffer external logic levels to the internal levels. Delay time will be largely process-

## Generic PLDS, FPLAs and FPLSs

It is a drawback to the range of PALs described in the previous article that the designer is restricted to fixed architectures with eight, six, four or no flip-flops. The introduction of generic macrocells made PLDs more flexible architecturally. The diagram top right shows a typical macrocell; the flexibility is achieved by the use of programmable multiplexers to route the output signal through different paths.

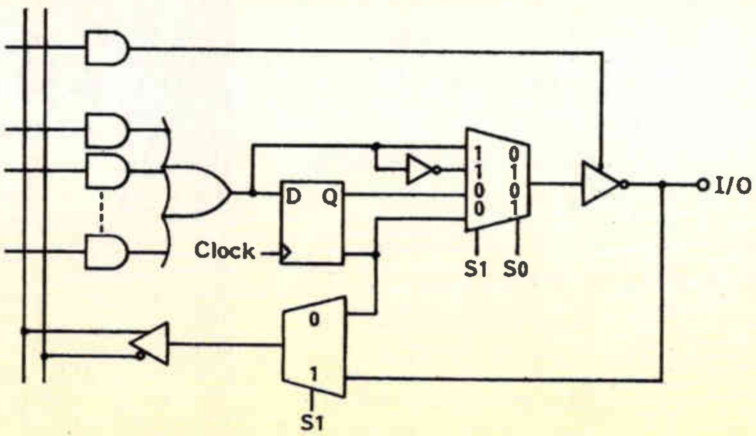
The design of the macrocell varies slightly from device to device; this example is actually used in the *22V10* device. There are four possible sources for the output signal. These are combinational, combinational but inverted, registered and registered/inverted. The same programmable bit that selects the registered or combinational signal for the output also routes it back to the AND array, but always inverted.

Generic PLDs can cover most programmable logic applications in a given package size, simply because of the range of input/output configurations which can be programmed into each device. The *GAL16V8* (generic array logic with versatile outputs) can perform the same function as the PALs *16L8*, *16R4*, *16R6* and *16R8* plus innumerable other i/o combinations which are not found as standard PALs. The *GAL16V8* is a 20-pin device and there is a 24-pin *GAL20V8* which has similar features, but with four more inputs.

The most likely problem with fitting a logic circuit into a *GAL16V8* or *GAL20V8* is the number of product terms available. Combinational outputs have seven terms and registered outputs eight terms each and, if the function requires more terms, a different solution will have to be found.

The first approach would be to try logic minimisation, but most logic compilers incorporate a minimiser anyway. It might be worth trying to invert the output sense and minimise, but there is no guarantee that would be successful either.

The 24-pin *GAL22V10* has more product terms, a variable number from eight to sixteen depending on which output is being used, and this will cope with most logic designs.




***Macrocell for the PALCE22V10. Here, flexibility is achieved by using programmable multiplexers.***

dependent as the input buffer will be designed to the minimum geometry allowed by the process. No heavy drive is needed to interface to the internal logic.

Some devices do feature input latches or registers, which will be optional and, therefore, add no delay when by-passed. When they are being used it is, again, most likely that they will be a minimum geometry design and their time penalty be entirely process-dependent.

Outputs determine the drive available for interfacing to external circuitry and, in this way, are no different from any other logic device. The drive capability of an output stage is usually characterised by the output short-circuit current.

One section of a CPLD whose performance can be affected by the way in which the chip is designed is the interconnect matrix. This matrix is an array of switches with as many inputs as there are device inputs, i/os and macrocell feedbacks. There are outputs to each of the logic blocks.

Each switch is like a small capacitor hanging on the input line, whether it is connected to a logic block, or not. As a result, the number of inputs to all the blocks determines the capacitance of the interconnect matrix.

The time taken to charge and discharge a capacitor is determined by the current which is used for this, so one way to speed up the matrix would be to increase the current driving each of the block inputs. This would also have the effect of increasing the power consumption of the whole chip. There are two consequences of doing this; firstly it increases the size, and hence cost, of the power supplies in the overall system. Secondly it increases the heat produced by the chip and, therefore, its running temperature. It may also have implications in the cooling needed for the system in which it is being used.

An alternative approach is to limit the number of signals which are switched into each of the logic blocks. This will reduce the total capacitance loading each AND term and hence the delay time for a given level of current drive. It also means that some of the input and feedback signals are not available for use by some of the AND terms.

The logic block itself offers only a little scope for performance optimisation. Limiting the number of terms in each block will save power, or allow more power to be used for each term, but this also limits the complexity of the logic function which can be implemented. At the heart of the block is, usually, a flip-flop with surrounding switches to mute the logic signal, as in the *22V10*.

Many large-scale-integration PAL devices also include product term switching which can allocate some or all of the product terms to adjacent logic blocks. This reduces the waste when blocks are only partially used, or used as direct inputs.

Although the product terms consume power in normal operation, some devices contain a 'turbo' switch. In non-turbo mode, the logic array is only powered when input signals are changing, the output signals being latched. An activity detector switches on the array power and enables the output latches when a change is detected at any input. Because this causes extra delay through the device, setting the turbo on keeps power applied permanently giving high speed at the expense of high dissipation, **Fig. 2**.

The features characterising CPLDs, then, are logic blocks with wide input gating, a central switch matrix, one-to-one correspondence between logic blocks and i/o pins and a compromise between speed, power and internal connectivity.

## Logic cell arrays

Although the term 'logic-cell array' is strictly applicable to one manufacturer's product, it does describe the second generic programmable LSI structure quite accurately, The layout of a typical LCA is shown in **Fig. 3**, and contains three basic elements, i/o cells, logic cells and routing channels. Most devices in this class use ram cells for configuration and signal routing.

Signals enter and leave the device through i/o cells with connections to the busses in the routing channels. The logic cells also have programmable connections to the routing lines which run past them. In this way, the signals are propagated round the chip. The logic blocks themselves are usually more complex than a typical PAL-type macrocell, but with far fewer inputs, typically only four or five. Thus, the logic structures can be fabricated from pure c-mos.

Unlike CPLDs, whose i/o pins are usually associated with a particular logic block, LCA i/os are independent of the internal logic. Any pin can be an input or an output and all the i/o cells are identical, although they may share their function with the signals needed to set the device up in the configuration phase. Complexity of the i/o cell varies according to device family, but they will normally have the usual function such as tri-state capability on outputs and the possibility of hitching or registering input signals.

As mentioned earlier, the logic cells themselves tend to have the possibility of implementing quite complex functions but with no more than six inputs. Implementing wide gating functions may require cascading over two or more levels of logic.

A CPLD can usually cope with a width of twenty or more signals in a single level of gating. An LCA design will, therefore, look more like a discrete logic design than a PAL, and logic minimisation may be performed more profitably with this in mind.

The routeing channels in an LCA owe more to masked ASICs than PALs also. Most LCAs include different lengths of muting within a device for, as we shah see, many of the

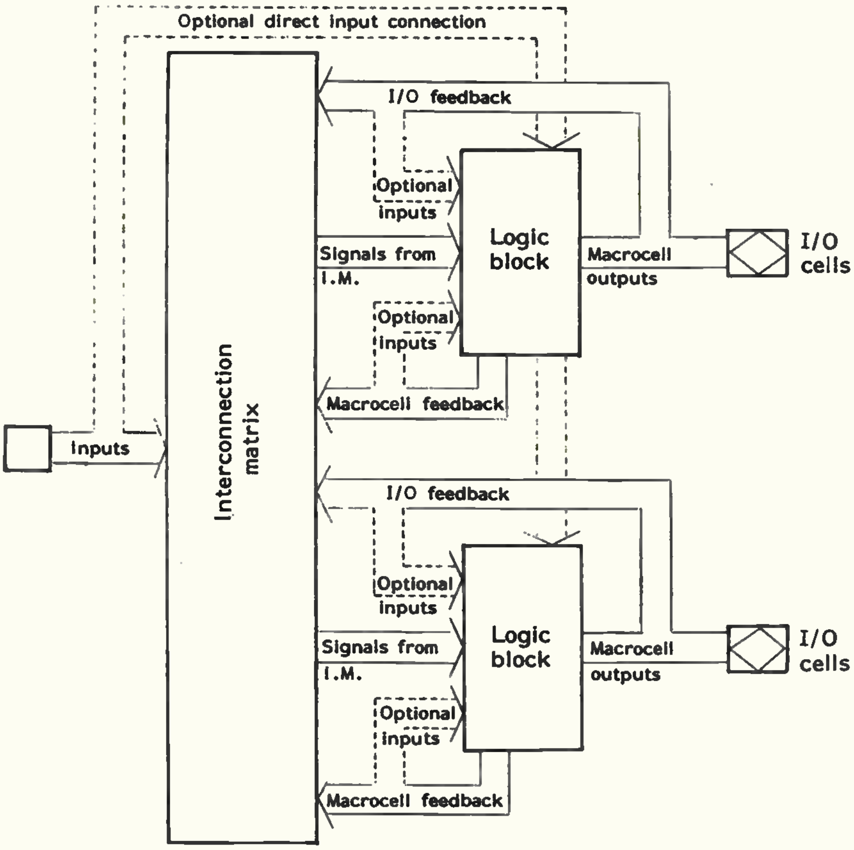



***Fig. 1. Basic structure of a large-scale integration PAL, also called a complex PLD or CPLD.***

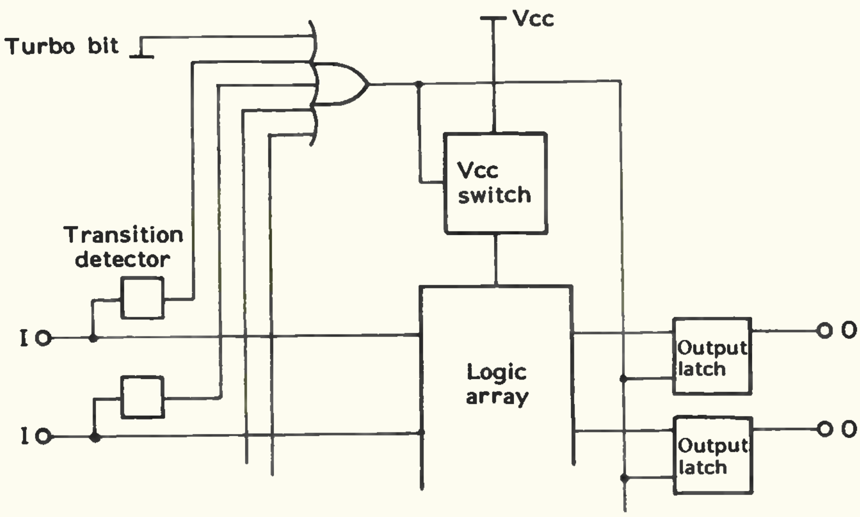



*Fig. 2. Turbo switch circuit. In turbo mode, the device is permanently powered but in non-turbo mode, it is only powered while an input signal is present.*

factors which determine device performance are connected with routing. Short tracks are usually available for routing signals between adjacent cells while longer tracks may be needed for carrying signals across larger areas of the chip. One or more additional tucks may be provided for clocks and other global signals, which may need a high fan-out.

The longer a routing track the higher its capacitance so performance is optimised by keeping track lengths as low as possible, which is helped by placing cells close together when their logic functions are closely associated in the circuit schematic. Often, repeaters or drivers are inserted along long tracks to help improve the delay due to track capacitance. Where horizontal and vertical muting channels cross they may be connected by programmable switches in order to divert signals to other rows or columns.

## Performance factors

As before, I will focus on speed and power consumption as the most important measures of performance. In practice, propagation delays between the different elements in an LCA can only be inferred from measurements made with different circuit configuration. For example, the difference in delay time between a single-level logic circuit and a two-level logic circuit should give the delay through a logic cell. The problem in making a judgement between two different circuits lies in other factors, such as the interconnect delay. Performance will depend as much on the way in which circuits are laid out as on the delay through circuit elements.

Furthermore, different arrays have logic cells of different complexity, so performance can also depend on the appropriateness of the logic function and the logic capability of the target device. At a simple level, a six-input gate may need two stages of gating in one array but only one in another, making the second appear faster irrespective of the intrinsic delay of the two devices. One good measure of the true speed of the internal logic is the maximum frequency at which a flip-flop will operate. This can be gauged by configuring a cell as a divider and finding the frequency at which the output disappears.

Because the internal logic cells in most LCA devices use relatively narrow gating, true c-mos circuitry is used in building the internal logic cells. Stand-by power is therefore comparable, in most cases, to that of the same circuit built in discrete c-mos logic. The only factor which usually causes a problem is any level shifting needed to interface the inputs to ttl levels.

As with discrete c-mos logic, power consumption starts to rise as soon as signals in the circuit start to change, and internal and external nodes need charging and discharging. Because the capacitance involved with internal connections is significantly lower than that of external connections, an LCA will usually dissipate less power during docked operation than the equivalent discrete circuit.

Actual power will depend on the number of nodes which are switching at any one time and will need some complex analysis to make an accurate prediction of power. It is often possible to calculate the predicted power consumption from within the design environment.

## Device configuration

The devices in this class of FPGA usually hold their configuration data in a shadow ram. Every interconnection site and every logic configuration bit is defined by one bit of this ram. Because static ram is a volatile storage medium, on power-up, an LCA will not be configured at all. The configuration data must be stored in some non-volatile device, such as an eprom, or it may be booted from disk in the same way as a computer operating system.

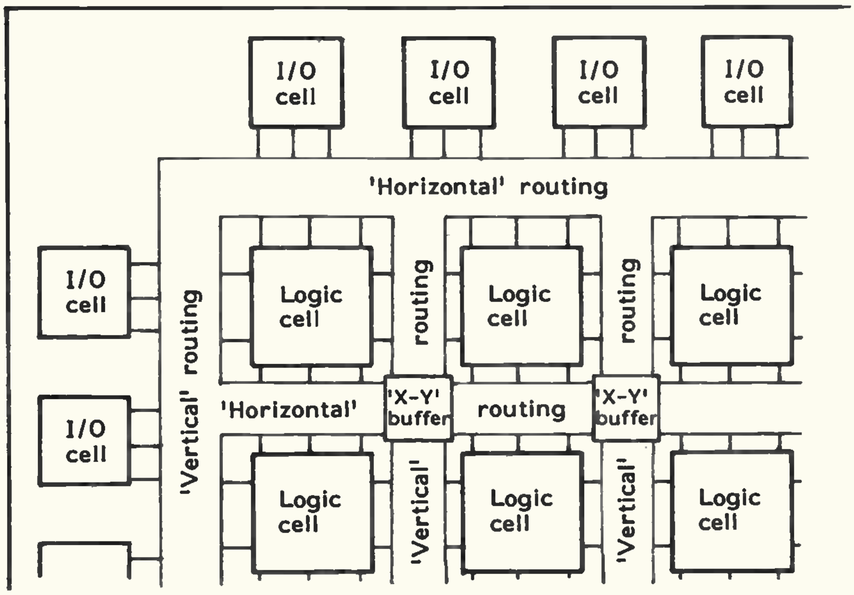
Some devices can use standard components, such as 27Cxxx eproms, while others are tailored to a specific memory. A typical configuration set-up is shown in **Fig. 4**.

There are two issues raised by the use of external memory components to configure LCAs. Firstly there is the problem of security; one of the attractions of programmable logic devices is the ability of most of them to read-protect the data after programming, making it difficult to copy the function programmed into the PLD. If the programming data has to be read in each time the system is powered up, this principle is defeated at the outset. Even if the data in the external store is protected somehow, a logic analyser will soon decipher the bit stream used to program the LCA.

A less contentious issue is the use of two devices to perform a logic function which, in other families, is contained within a single device. This may be overcome by combining the data for LCA configuration with some other data, such as the operating program for a microprocessor. But it still leads to complications in the hardware design for the overall system. If several LCAs are used in one system they can share a single eprom, in most cases, which reduces the hardware overhead to a fraction of a device.

The upside of this arrangement is that reconfiguration of a system can be managed by software even, in many cases, while the system is actually operating. This may be a simple change, such as redefining a memory map to re-allocate resources, or a partial or complete change of logic function. In Atmel devices, part of the device can be reconfigured while the rest is still functioning; the name *Cache Logic* has been coined to describe this function, by association with

*Fig. 3. Logic-cell array contains three basic elements – i/o cells, logic cells and routeing channels.*



cache memory, which buffers and speeds up data exchanges in computer systems.

## Antifuse FPGA technology

The architecture of antifuse FPGAs is practically identical to LCAs. Uncommitted i/o cells surrounding logic cells and routeing channels. Any differences are due mainly to the two different technologies involved. The main difference is in the resistance of the transmission elements. LCAs use a mos transistor, which has a relatively high on-resistance compared with an antifuse, once it has been blown.

Whenever a signal passes through a fuse element, it must charge up the capacitance of the component to which it is connected. The capacitance of tracks and gate inputs will not differ significantly between the two technologies. As a result, the series resistance of the fuse makes a significant difference to device performance. Antifuse devices can, therefore, use an architecture which has longer connecting tracks than LCAs.

In practice they are often supplied with tracks of differing lengths within a single routing channel. The actual track length required for any specific connection can be optimised by choosing an appropriate path in the routing channel. By minimising interconnect capacitance and series resistance, in this way, the interconnect delays are minimised and there is no need for repeaters or drivers within the connection structure.

Another trade-off is the size of the logic cell and the amount of interconnection. In a practical device it must be possible to connect the logic cells together even when approaching 100% utilisation. One way to improve connectivity is to make the logic modules quite complex; by incorporating more logic in each module, fewer connections between modules are needed. This is the trend in LCAs.

If track delays are less significant, the logic modules may be made simpler, and complex functions built by using short lengths of track to connect them. Module usage is likely to be improved in this way, with less wasted logic functions and silicon area. Antifuse FPGAs are, therefore, able to use a smaller grained structure than LCAs and, usually, offer a less wasteful solution to most logic circuits.

Although this approach may need more interconnects, the antifuse technology helps to reduce the cost impact of the on-chip area. Antifuses occupy about a square micrometre and fit inside the aluminium tracks, thereby taking up no extra space in the array. Ram-based FPGAs need a ram cell and mos transistor at each crossing point, and these add to the area occupied by the interconnect.

Granularity is an important feature of ASICs as it determines the efficiency with which logic functions can be implemented. Mask-programmed ASICs, for example, are usually fine grained as they have low resistance vias to connect logic blocks to the tracks. A logic cell is just a small gate and more complex functions are easily built without incurring much speed penalty from the interconnect.

Antifuse FPGAs have a more complex basic cell; a flip-flop with some universal gating is quite common. A typical LCA logic block has two flip-flops driven by some fairly complex combinatorial logic.

By way of example, a 4000-gate LCA, namely the Xilinx *XC4004A*, has 144 logic blocks while a 4000-gate antifuse FPGA like the Actel *A1240A*, has 684 modules. In order to achieve 4000 routable gates, a sea-of-gates gate array may need 7000 gates in its basic array, where one gate in the array corresponds to a single cell but also has to act as part of the routing resource.

## Performance of antifuse FPGAs

Most of the remarks about LCA devices also apply to antifuse FPGAs. The logic cells are true c-mos and consume 'zero power' at zero frequency. Logic circuits are not very useful at zero frequency and as soon as signals begin to switch, power is dissipated by the charging currents for the parasitic capacitances. In practice, this current is negligible below 1 MHz but becomes significant above this frequency.

Within an FPGA there are two sources of power dissipation, the active circuit elements and the interconnects. For a given feature size, capacitance of circuit elements will be practically the same, irrespective of architecture. Any difference in consumption will be due largely to the interconnect capacitance.

Antifuse FPGAs tend to use more tracks than LCAs, as the LCA logic cells can perform more complex functions. On the other hand, LCAs may use longer tracks and higher capacitance connections between tracks, so the comparison may well depend on the actual logic being implemented.

The same arguments also apply to dynamic performance, with the added factor of the resistance of the two types of programmable connection. Logic requiring the connection of large numbers of gates will usually perform better in antifuse FPGAs, because of the superior performance of the antifuse.

Where logic function can be concentrated into the more complex LCA cells, antifuse devices will probably use more interconnects and show a poorer dynamic performance. If we extend the argument to include CPLD structures, the trend is more pronounced. They will perform well in highly structured circuits, where the macrocells can implement a whole logic function, but deteriorate badly as soon as repetitive feedback has to be introduced in more fragmented circuits.

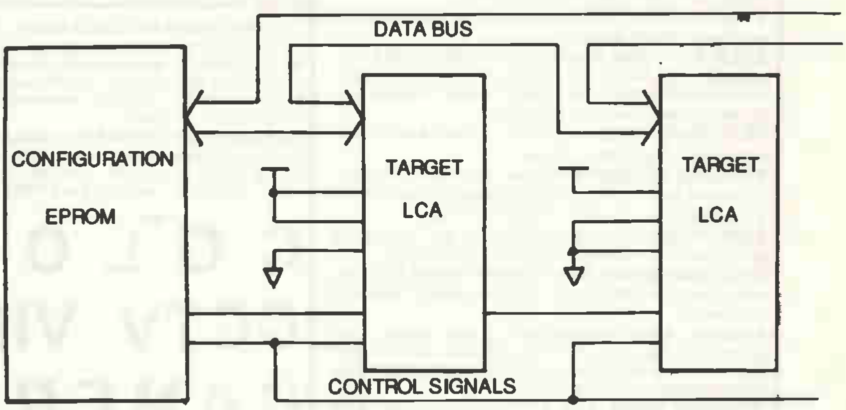



*Fig. 4. Typical LCA configuration circuit. Some arrays take standard eproms while others are tailored to a specific type.*

## Using antifuse FPGAs

The main drawback with antifuse FPGAs centres on the programming situation. Even a small circuit can take three minutes to programme while the larger devices may take ten minutes. This compares with a few seconds for most CPLDs structures and no time at all for LCAs, which are programmed in-circuit each time they are powered up. A single programming station, with four sockets, is limited to between 200 and 600 circuits a day and, therefore, adds a significant overhead to the basic cost of the device.

The upside to this limitation on production throughput and increased cost is a double benefit. A circuit using an FPGA will start working the instant it is switched on, and requires no overhead in program storage or extra design work in arranging for the device configuration function.

The other advantage is security. It is difficult to read back some FPGAs, but they also contain security fuses to prevent this from being done. Complex PLDs also contain security cells to prevent direct reading, although sophisticated analysis may defeat device security. LCAs are much more difficult to keep secret. ■

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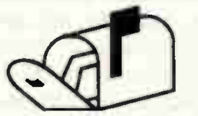

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**RECHARGE ORDINARY BATTERIES UP TO 10 TIMES!** With the Battery Wizard! Uses the latest pulse wave charge system to charge all popular brands of ordinary batteries AAA, AA, C, D, four at a time! Led system shows when batteries are charged, automatically rejects unsuitable cells, complete with mains adaptor. BS approved. Price is £21.95 ref EP31.

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**3" DISCS** As used on older Amstrad machines, Spectrum plus3's etc £3 each ref BAR400.

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**3-30V POWER SUPPLY KIT** Variable, stabilized power supply for lab use. Short circuit protected, suitable for profesional or amateur use 24v 3A transformer is needed to complete the kit. £14 Ref 1007.

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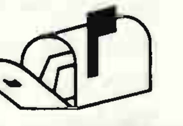

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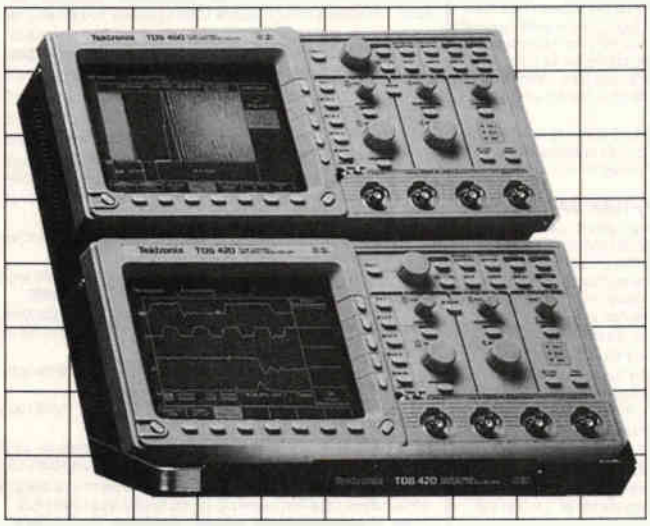


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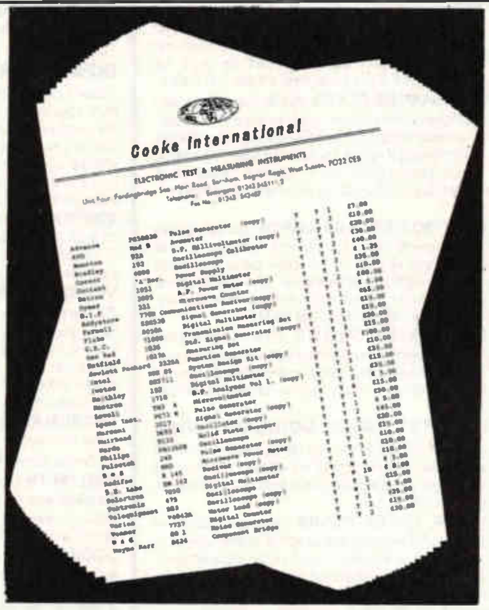


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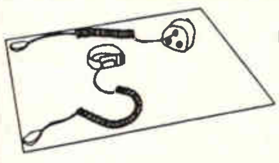

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| BRUEL& KJAER 2307 level recorder | £1000 |
| BRUEL & KJAER 2308 analogue X-Y pen recorder | £750 |
| CHASE LFR1000 interference measuring receiver 9kHz-150kHz | £1000 |
| DATRON 1061 & 1061A – various, digital multimeter & 1065 – call | from £500 |
| DATRON 1065 digital multimeter all ranges plus IEEE | £500 |
| FARNELL SSG2000 synthesized signal generator 10Hz-2000MHz | £2500 |

CERT. 95/613

***ISO9002 ACCREDITED STOCKIST MEASUREMENT & TEST EQUIPMENT***

| | |
|---|---|
| PHILIPS PM5167 1mHz-10MHz function generator | £275 |
| RACAL-DANA 9300 milli-voltmeter | £400 |
| RACAL-DANA 9301A true RMS RF milli-voltmeter | £350 |
| SCHLUMBERGER 7081 precision voltmeter 8.5 digits | £2750 |
| TEKTRONIX P6201 FET PROBE | £350 |
| WANDEL & GOLTERMANN WM30 level tracer | £500 |
| WANDEL & GOLTERMANN PJM-4S jitter meter for SONET & SDH | £5500 |
| WAVETEK 23 synthesized function generator 0.01Hz-12MHz | £1250 |
| WAVETEK 1067 opt 522 1-500MHz sweep generator | £500 |
| WAYNE KERR 3220 20A bias unit (for 3245 inductance analyser) | £1250 |
| TEKTRONIX AM503/P6303 current probe | £1500 |

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| 3335A synthesizer/level generator | £2000 |
| 3235A switch/test unit | £1000 |
| 3324A synthesized function generator | £2000 |
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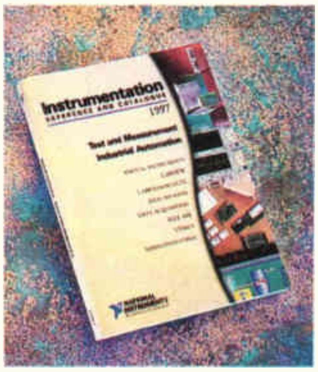


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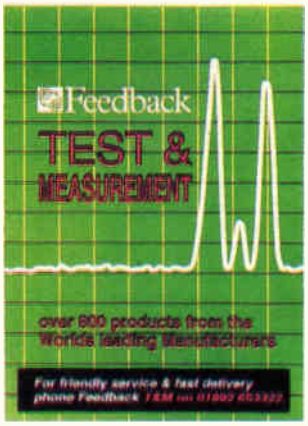


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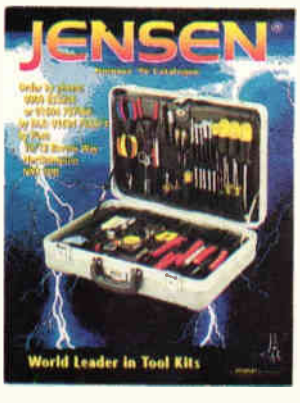


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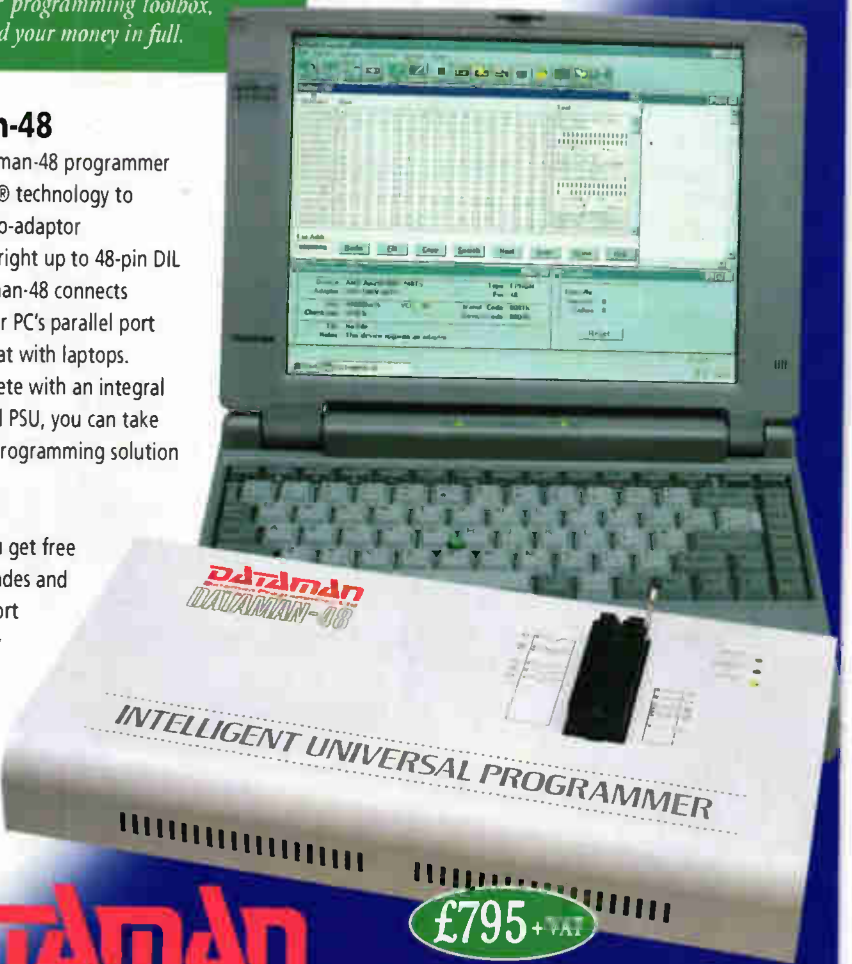


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