THE JOURNAL FOR PROFESSIONAL ENGINEERS

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NOVEMBER 1987

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Single-board computers

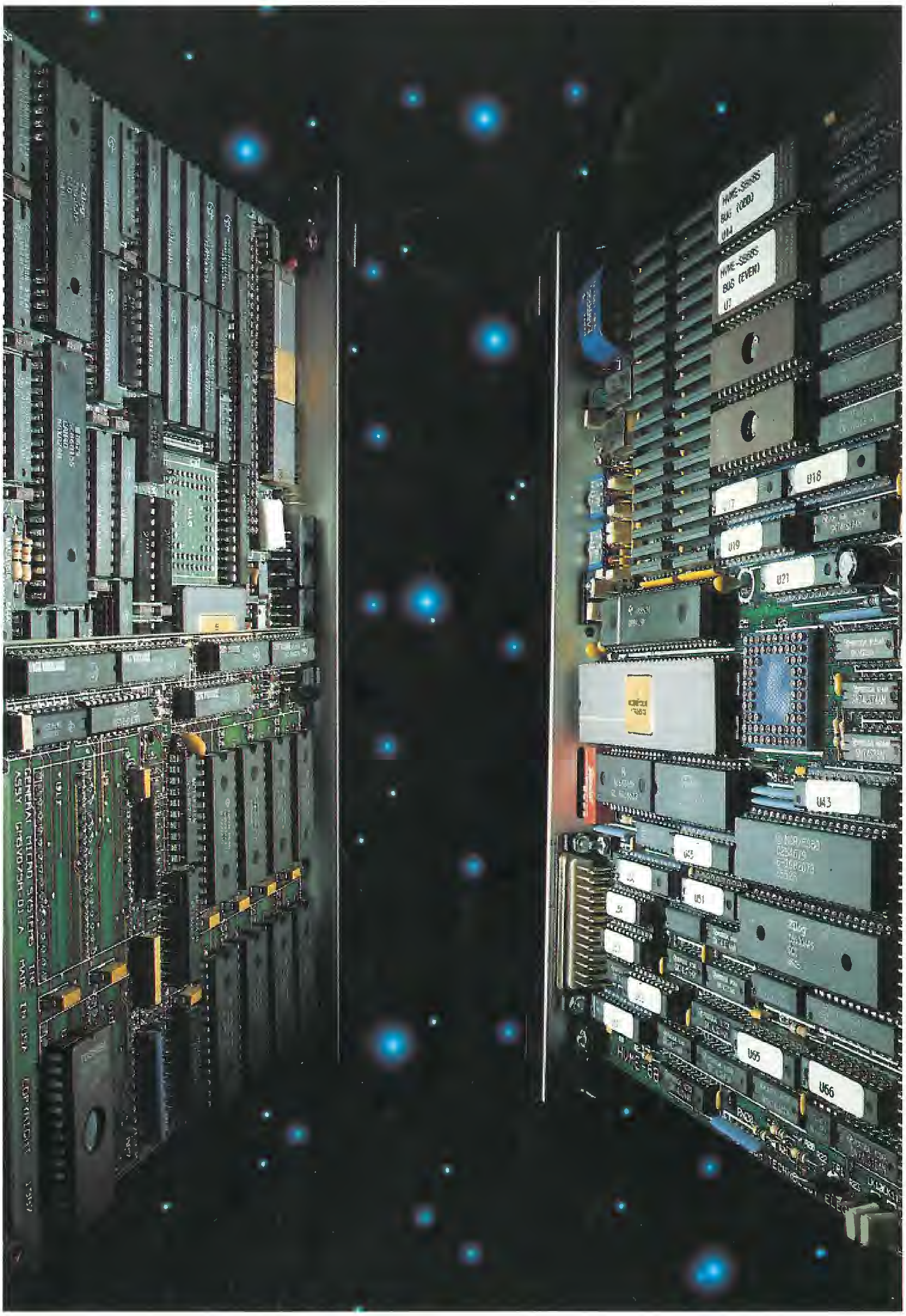
Integrated processor – the 68030

E.H. Armstrong – genius of radio

Two channels – one link

Op-amp precision rectifier

PC and XT enhancements



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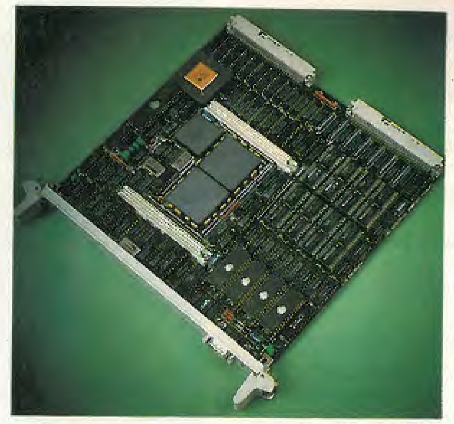

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COMMENT

IT is still a miss

"Shortages of skilled staff are a more significant obstacle to the effective use of IT than finance, lack of awareness or any other identified factor". Thus the opening remark of an NCC report on what needs to be done to get people to work with "information technology", whatever the current definition of that is.

Five years ago, Mrs Thatcher's government had the light of IT in its eyes: Kenneth Baker, her Minister for Information Technology, espoused the cause with verve and gusto and was rarely to be seen when not on some platform preaching the new religion. Perfectly innocent schoolchildren were bombarded with BBC micros in the hope that, by a process of "osmosis" (ILEA's term), familiarity would breed familiarity.

Assuming that the micros were given to 16-year olds, some of these youngsters should soon be coming out of university and be in a position to demonstrate the success or otherwise of this policy, but it must be said that, in the case of those who went straight into employment rather than to higher education, familarity appears to have bred the more conventional reaction of contempt.

It all depends on what the NCC means by information technology. The official definition during IT Year in 1982 was "the acquisition, processing, storage, dissemination and use of vocal, pictorial, textual and numerical information by a microelectronics-based combination of computing and telecommunications", which seems to cover pretty well everything from working out one's expenses on a pocket calculator to forecasting the weather. Since Philip Virgo, who wrote the report, asserts that "the bulk of the skills in short supply can be acquired from scratch in under 18 months, given adequate programmes of intensive training and structured experience", the skills referred to are those concerned with something a little more advanced than simple word-processing. He goes on to say that the shortages are in the areas of "technology and application-specific software and/or project management". Plainly, the training required is an industry matter, rather than the concern of schools, except insofar as schools can instil the relevant attitudes.

The report maintains that the main reason for the failure of employers to train staff is not one of cost, but rather the fear that trained staff will be enticed away by bigger companies for bigger salaries. That being so, it is a little difficult to understand the need, expressed in the report, for tax incentives to encourage employers to train their staff.

A fear of losing trained staff is easier to understand, but is surely not unique. If employers were to decide not to train their workforces in other, equally esoteric skills, because of a fear of a mass exodus to the opposition, the road to ruin would be very clearly defined.

Better information from government is needed, says the report, meaning information on the training courses now available. This is probably so, but the smaller companies, who are in greatest need of assistance, also need information on the technology itself. As the MD of a small firm in the Midlands remarked recently, "It's all very well all these smoothies coming here telling me I need to use more IT, but what do they mean by IT? I've got a minicomputer for the payroll and billing, I've a raft of n.c. machine tools and half a dozen w.ps and still they tell me I'm behind the times". If someone can tell him how to make widgets faster and cheaper, he will be interested, but he has to rely on IT manufacturers for information, which is hardly unbiased.

Electronics & Wireless World is published monthly USPS687540. By post, current issue £2.25, back issues (if available) £2.50. Order and payments to 301 *Electronics and Wireless World*, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS. Cheques should be payable to Reed Business Publishing Ltd. **Editorial & Advertising offices:** *EWW* Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS. **Telephones:** Editorial 01-661 3614. Advertising 01-661 3130 01-661 8469 **Telex:** 892084 REED BP G (EEP) **Facsimile:** 01-661 3948 (Groups II & III) **Beeline:** 01-661 8978 or 01-661 8986. 300 baud, 7 data bits, even parity, one stop-bit. Send ctrl-Q, then EWW to start; NNNN to sign off. **Subscription rates:** 1 year (normal rate) £23.40 UK and £28.50 outside UK. **Subscriptions:** Oakfield House, Perrymount Road, Haywards Heath, Sussex RH16 3DH. Telephone 04444 59188. Please notify a change of address. **USA:** $116.00 airmail. Reed Business Publishing (USA). Subscriptions Office, 205 E. 42nd Street, NY 10117. **Overseas advertising agents: France and Belgium:** Pierre Mussard, 18-20 Place de la Madeleine, Paris 75008. **United States of America:** Jay Feinman, Reed Business Publishing Ltd, 205 East 42nd Street, New York, NY 10017. Telephone (212) 867-2080 Telex 23827. **USA mailing agents:** Mercury Airfreight International Ltd, Inc., 10(b) Englehard Ave, Avenel N.J. 07001. 2nd class postage paid at Rahway NJ. Postmaster – send address to the above.

ISSN 0266-3244

Single board computers and the VME bus – a practical design system

STEVE HEATH

The combination of an industry standard bus and processor family such as VMEbus and the 68000 family provides a powerful architecture suitable for both simple and complex multiprocessor systems. The industry has responded in providing a large number of VMEbus boards which should be treated as functional blocks in a manner similar to that of components in a discrete microprocessor design.

Systems components offer advantages in providing a base of ready built hardware and software allowing system designers to concentrate on adding their particular expertise to the design. As a result, the trend has been to use single board computers instead of building a discrete design for low run rate or very complex applications. The availability of suitable s.b.cs has exploded in the last five years because of this demand in the marketplace, and can offer 68020-based processor boards that rival minicomputers in terms of performance.

For simple applications using one s.b.c., very little consideration to the overall system design is required. However the use of multiple s.b.c. components allows the design of very sophisticated multiprocessor systems, whose success is dependent on the correct interaction between the software and hardware interfaces of the s.b.cs used. Thus a good design requires a methodology to define these interactions, to use their effect on the overall architecture to provide the required performance. The major difference with a s.b.c. design is that it cannot be split into separate hardware and software phases which so often happens with discrete designs. An s.b.c. system designer has to be aware of this interplay between the two factions.

In an effort to guide designers some s.b.c. design principles with practical observations will be defined, explained and illustrated with two examples. The aim is to provide a system that can be used to highlight potential problems.

Although based on VMEbus and 68000 processors, the design method is applicable to other systems.

DESIGN SYSTEMS

The design system described is an iterative process, using new detail determined later in the chain to further define the original specification used at the start.

1. ***Define the functional blocks required to fulfill the basic system requirments.*** Define the functions that are required. The initial specification will be the main source of information. Do not try and be all-encompassing at first; the detail will appear as the methodology is followed through. Be prepared to reiterate the process as either problems are highlighted or a better understanding of the system is obtained.

2. ***Define the time critical functions/ mechanisms within the system and their importance to the system.*** Analyse each block in turn and determine where possible time critical functions or system bottlenecks may occur. Define if possible the minimum and maximum times, speeds etc. for these operations.

3. ***Decide the hardware/software required for each functional block and check that it meets the performance requirements defined in 2.*** This is where the theoretical requirements are matched against data sheets. From this, details such as minumum processor speed required, disc access, memory access and software techniques will come out. If a new point arises, repeat step 1 and use the information to improve the initial definition. It is here that the decision to design and build may be taken if, after many iterations, an off the shelf solution is not available.

4. ***What resource i.e. memory, interrupts etc does each function require ?*** This is the most difficult aspect of a multiple design. It is now that full system definitions are required and this must cover both the hardware and software aspects as well as the more esoteric interaction between the two. It is here that potential problems are often overlooked due to misconceptions.

The common misconceptions have been described as a set of observations:

"In terms of the hardware interface and requirements, any intelligent board that is capable of starting and transferring data across the VMEbus should be classed as an s.b.c. and its bus, interrrupt and memory needs taken into consideration." The majority of disc controllers, graphics boards and serial communications boards are all single board computers but have been dedicated to a particular function. This means that even a simple VME system is often a multiprocessor system.

It is important that bus arbitration and interrupt requirements are supported. A design may require a four level VMEbus arbitration scheme while the s.b.c. acting as a system controller may only support a single level option. Within a distributed interrupt handler scheme, where different s.b.cs handle different interrupt levels, care must be taken to ensure that all levels are handled and by a unique handler. Designing and debugging a system where interrupts can be left hanging or answered at random by different handlers is not to be recommended.

"To achieve maximum performance, the VMEbus should be used as a medium for passing messages between s.b.cs and not as a replacement for the microprocessor bus." The modularity of VMEbus boards allows their use as building blocks by using the bus as a micro processor bus replacement. The

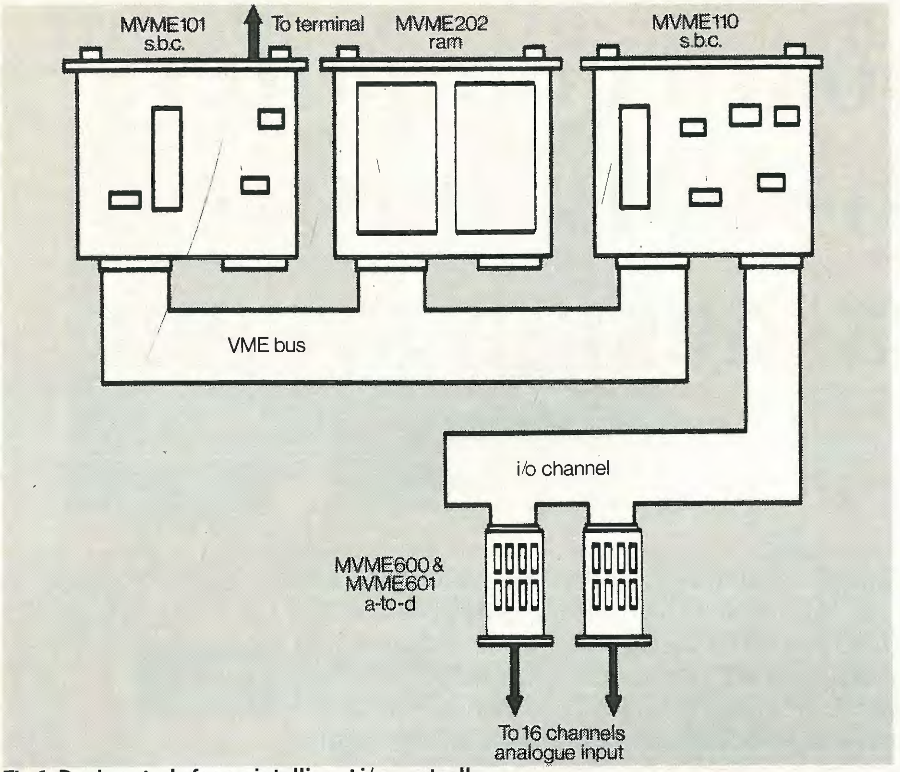


Fig.1. Design study for an intelligent i/o controller

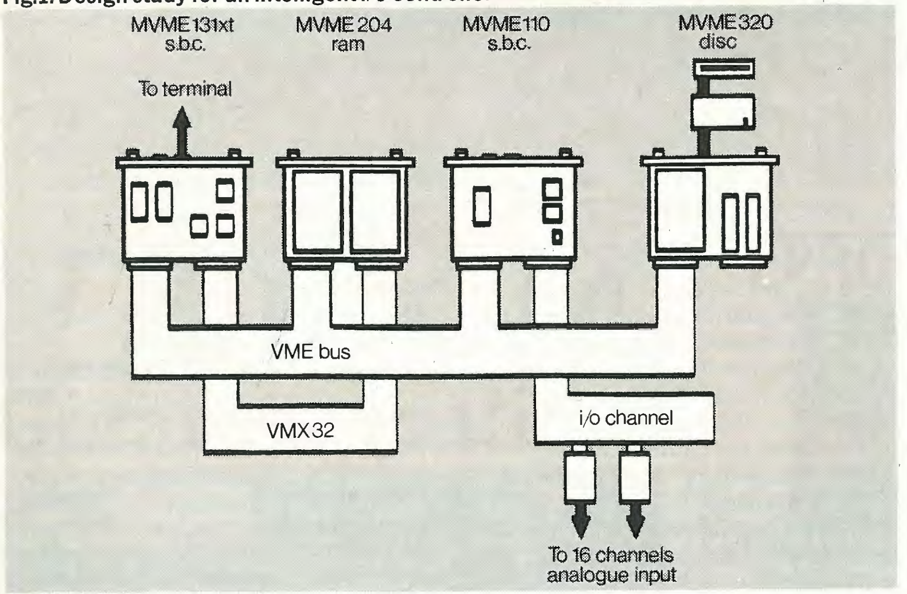


Fig.2. The first solution to the i/o controller design

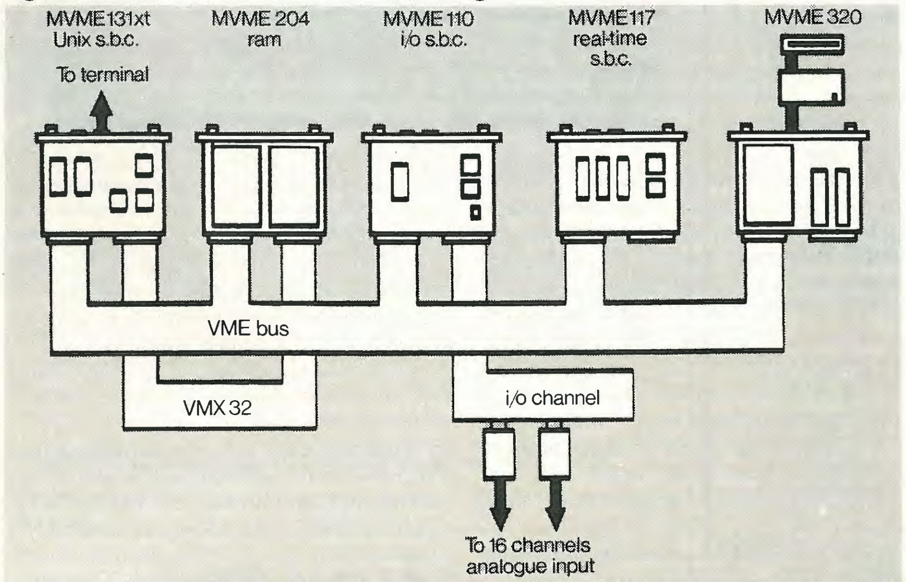


Fig.3. The final version of the controller.

problem is that a 68000, through its prefetch and pipeline mechanism, uses about 80% of the external bus bandwidth. So where the majority of bus use is processor traffic, the scope for multiprocessing is reduced due to the small bus bandwidth available. This processor need can be reduced by the use of 32 bit processors such as the 68020 and 68030 which use on chip caches to reduce bandwidth requirments to about 50-65%, and by the use of extension memory buses or increasing local resource.

It follows that the use of 'intelligent' boards is recommended to reduce the bus bandwidth burden of dealing with i/o functions. The use of 'dumb' boards should be restricted to low performance designs.

However the influence of poor software design can cripple an otherwise good hardware architecture. If, through its software, the processor spends a large amount of time using global memory, system performance will be reduced through the consumption of bus bandwidth. This can be caused in many ways: overuse of polling routines, operating systems using global memory as default task memory, etc.

"Every s.b.c. on the VMEbus has its own memory map which may overlap or be localised: i.e. memory may appear at different locations in different s.b.cs memory maps and may be local or globally available." It is important that memory maps are determined. Within a VMEbus system, memory and i/o devices may either be local to a processor on a s.b.c. or be globally available via a bus. In addition, memory may be multiple mapped within a system or may be addressed differently depending on which path is used to access it.

Add to this the address modifier codes which indicate either 16, 24, or 32-bit addresses and there is a potential for much confusion. Defining individual memory maps gives the view that each s.b.c. has of its memory. This allows checking to prevent duplicate memory addressing, and all required accesses can be done.

Again software has a large influence over the hardware implementation: address modifiers will change depending on which state, user or supervisor, the programe is running in. On board registers may need initialisation to allow certain memory pathways and enable hardware facilities.

"Interrupt response is the result of not just the interrupt level but also bus arbitration request level and the local processor interrupt level and mask." The interrupt mechanism within VMEbus involves the interrupt handler successfully arbitrating for the bus prior to acknowledging the interrupt. The handler processor may further delay the process due to an internal or external interrupt mask, or because of some higher priority exception processing. Therefore for the fastest response, a combination of high bus arbitration request, VMEbus interrupt level and local interrupt level is required to reduce the response time throughout the whole interrupt chain. Time critical functions which are not allocated these resources will be impacted.

"Every SBC has equal potential for enhancing the system or degrading it." Every

time a s.b.c. is added to a design, certain checks must be performed to make certain that its addition does not degrade the overall system or introduce new error conditions. There must be sufficient bus bandwidth for its requirements and such that it does not cause other s.b.c. watchdog timers to time-out through bus unavailability. Its effect on memory maps must be checked to prevent memory duplication etc.

5. ***How does the system handle errors or system failures?*** Very often little consideration is given to what happens to a system if it fails. Failure in a multiple s.b.c. system can be at various levels, and usually results in either a high level interrupt or a VMEbus cycle being terminated by the bus error signal. Both of these conditions require exception handling by the s.b.c. concerned.

The most common cause of a "system failure" is the incorrect setting of bus watchdog timers which will generate a bus error signal if a data transfer is not completed within a certain time period. This facility is necessary to prevent system hangs due to the truly asynchronous nature of the VMEbus and 68000 family interface. However if this value is too short or a s.b.c. holds the bus then a bus error will be generated which would be interpreted as a system failure. Thorough checking of timers is therefore recommended.

6. ***How much performance is not being used? Is this sufficient to give confidence that hardware/software can meet requirements?*** This is always difficult to predict as the only proof of this aim being met is in the end product. To gain performance improvement either to meet the original requirement or to allow additional functionality can only be achieved by improving software or executing it faster. Single board computers are often offered in different processor speed options which allow the upgrading of a system with little or no software modification. The 68000 family, through its object code compatibility and common operating system environments, such as Versados and System V/68, allows upgrades from the 16-bit 68000/68010 to the 32-bit 68020 and 68030 systems. This upgrade path is also applicable to cost reduction or the improvement of facilities through a design's life.

These principles are now illustrated with two system designs.

SIMPLE MULTIPROCESSING: AN INTELLIGENT I/O CONTROLLER

In this requirement, the initial design brief was for a data logger that could take data from 16 analogue channels at a 2kHz sample rate and provide statistical analysis on the incoming data in real time. The resolution of the analogue channels to be 12-bit or greater and no data was to be lost through out the measurement period. It was unacceptable to lose any incoming data.

The first stage is to block out the basic system requirements: a processor to fetch the data and analyse it, 16 channels of analogue to digital i/o and some memory. The next stage is to determine what are the most critical functions. Obviously the capture of data is the most important and requires a heavy processor load. To capture 16 channels at a 2kHz sampling rate requires 32000 separate data transfers which if polled for 30μs (a typical conversion time), would take 960000μs or 96% of the bus bandwidth. The use of a 32-bit processor with its wider data path would not be advantageous because the data is less than 16 bits wide and is not available concatenated. If an interrupt software scheme was adopted and each interrupt routine took on average 15μs (again a typical figure) then bus bandwidth used would be 48%. If some data loss could be tolerated, then the analysis routines could be interleaved into the polling routines. However if the analysis overran or some other exception took place polling would be delayed with the subsequent data loss. Simply placing a dumb a-to-d board on the bus would dissent from the second observation by using the VMEbus as a replacement microprocessor bus.

Obviously the solution is to put some intelligence with the a-to-d board to remove this overhead. The chosen solution was to use a MVME110 s.b.c. which has its own local 8-bit i/o bus called the i/o channel. On the i/o channel is a MVME600 with an MVME601 extender providing 16 channels of a-to-d conversion. The combination of these units gives a single intelligent a-to-d unit.

The adopted solution is shown in Figure 1. The delegation of system functions is straight forward: the MVME110, with the MVME600/601 a-to-d boards, collates the information from the a-to-d converters, preprocesses it, and then writes that information into global VMEbus memory. A second s.b.c. a MVME101, takes that information, analyses it and displays the data on a terminal. Both these boards have 8MHz 68000 processors with local memory on board.

The addition of the MVME110 enhances the system providing consideration is given to its requirements. From the memory maps, the only area of commonly accessable memory is provided by the MVME202 ram board. Therefore data must be stored in this global memory using circular buffers of sufficient depth. Access is required by both processors but priority should be given to the MVME110 to ensure data is stored without loss. The MVME110 should thus have the higher bus arbitration request level. If the MVME101 had the higher level then access to the global buffers would only be given to the MVME110 when the MVME101 had finished using the bus. No guarantee of access would certainly result in data loss and system degredation.

The rest of the system design is straight forward: both s.b.cs have their code stored in on board rom and use some local scratchpad ram. Synchronization between the two processors is achieved by polling a memory semaphore. VMEbus interrrupts are not used due to the lack of a bus interrrupter function on either s.b.c. Only local interrupts are processed.

Error handling is simplified by disabling the SYSFAIL VMEbus line such that neither processor recognises it. A bus error signal is treated as an indication of a global error: the MVME101 sends a message to the terminal indicating possible data loss, and the MVME110 holds as much data locally as it can. Both boards will retry the access periodically to see if the system will recover.

The second example is based on an upgrade to the first system:

MULTIPROCESSING SINGLE BOARD COMPUTERS

The requirements here are similar to that of the first example: again 16 channels of analogue data need to be sampled at a 2kHz rate and analysed. However the data instead of being sent to a terminal for display, is to be stored on some form of mass storage and is required for a data base and other analytical software running under a Unix type environment.

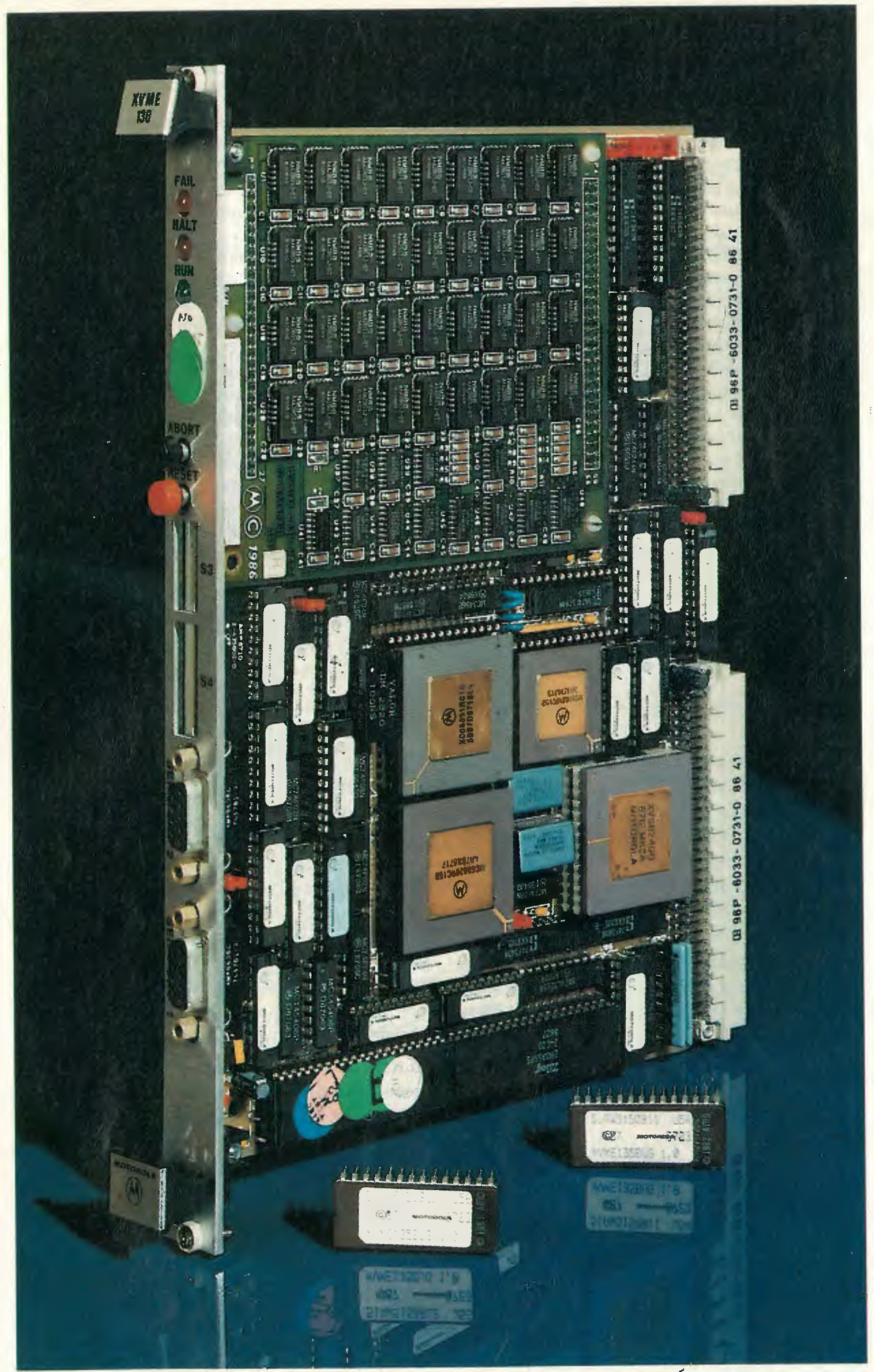
WHAT IS A SINGLE-BOARD COMPUTER?

Paradoxically, single-board computers are rarely used for the more usual tasks associated with computers. That is, they are not used for purely manipulating text or numbers. Most desk-top computers are in fact built on single p.c.bs, but the term 's.b.c.' has come to mean a board with a processor and some memory and an operating system, usually on eprom. Such board are used chiefly in control systems and can be subdivided into 'Development' and 'Target' boards.

The development system is used to explore an application. At the end of the development phase the program can be downloaded to the target board which can be tailor-made to provide only the functions needed for an application. Such boards usually have no display or keyboard, unless these are needed for their function, instead they are programmed from a host computer through a link (RS232). Depending on the application, they may have special facilities such as digital-to-analogue and/or a-to-d converters, and timing, including a real-time clock. As it is important for a control system to function properly, a 'watchdog' program, or a speciific integrated-circuit, monitors the supply rails and makes sure that on switch-off or power-up that all switches are in a 'safe' condition.

A second area for application of s.b.cs is the addition of functions to an existing computer system. It may be a display controller that offers higher resolution graphics than is provided on the host system; or interfacing with external analogue or digital signals in test, measurement and control applications. The essential difference between these and other plug-in cards is the on-board processor which can relieve the host computer of those tasks associated with the function.

Finally, s.b.cs can be used as part of a plug-in system with a number of cards added to a backplane bus (for example, VMEbus). Various cards with differing functions can be linked to provide specific functions in, say, a cad/cam workstation, a complex control system or test facility.



In terms of the basic functionality, the MVME110/MVME600 intelligent a-to-d sub-system can be used and offers similar advantages to that described in the first example. Obviously a Unix system is required which demands the presence of a processor with memory management, disc controller for mass storage and in excess of 1Mbyte of memory. The disc system could perform the additional function of storing the digitised analogue data. By using a 68020 32-bit processor with its minicomputer performance to run Unix, the original role performed by the MVME101 could be achieved as a process runing under Unix.

This initial draught, shown in figure 2, appears to be quite sound and from the hardware considerations eminently practical, but unfortunately the interaction between software and hardware has not yet been considered.

The critical routine of receiving and analysing the data requires a guaranteed response and access to physical resource such as global memory and possible interrupts. The Unix environment uses its hardware memory management to prevent processes running under it from accessing these resources. Simply writing some code which accesses location $100 will compile and run but the physical memory location accessed will be translated and not be $100.

The 68020 s.b.cs such as the MVME131 and MVME136 series have global bus interrupters which allow processor to processor communication via an interrupt mechanism. This again is advantageous in terms of reducing bus traffic: the MVME110 can transfer a block of data and then interrupt the 68020 to indicate that the data is available. Unfortunately the characteristics of Unix are such that there is no guarantee when the interrupt would be serviced and the appropriate process started. Unix does not have such a real-time characteristic.

Fortunately there is a shared memory mechanism built into Motorola's System V/68 Unix port which allows access via a system call to an area of physical memory. This allows a shared memory communication path between the s.b.cs but does not solve the requirement for real-time response.

The obvious solution is to add another self contained s.b.c to act as a real time interface to the MVME110 and to provide data on a non real-time basis to the application software running under System V/68. This third s.b.c. requires to be self contained so that it does not use or influence the Unix environment. It therefore requires that its on board memory is local and has some global memory for comunication with the MVME110 or it has local dual ported memory. This should be addressable at a different location to prevent memory addressing conflicts within the overall system.

Taking these points into account, the functional design is expanded to provide three s.b.cs and is shown in figure 3. System V/68 runs on a MVME131XT which accesses global memory via VMEbus or through the MVX32 subset of the VMEbus subsystem bus. In addition to further reduce bus traffic this processor has a 32-KByte on board cache. Mass storage is provided by MVME320 disc controller. This meets the System V/68 need and allows the analysed data to be stored via the System V/68 file system.

The MVME110 with the MVME600/601 performs the intelligent a-to-d function and transfers the preprocessed data into global memory ready for the third s.b.c, a 68010 based MVME117 board. This board is available in two versions: the standard version has 512Kbytes of local memory, and an A version which has 2 Mbyte shared memory. The standard version was chosen so that there was no possibility of memory conflict with the System V/68 memory map.

While it is straight forward to configure the hardware to provide the correct accesses, the System V/68 kernel will search and size memory within certain boundaries and will use any memory it thus finds. Therefore these boundaries must be modified to prevent the use of certain global memory by System V/68 and use it for MVME110 to MVME117 communication. Another aspect often overlooked in systems using both 16 and 32-bit processors is how a full 32-bit address must be generated to access the VMEbus short i/o area by the MVME131XT while a 24 bit address is valid for either the MVME117 or MVME110. The effect of software not specifying the full correct address would be a bus error which the system would probaly interpret as a failure.

STOP PRESS
Motorola have just announced what they call a new generation of software standards to allow the development and execution of real-time software under a Unix environment. The new operating system, which solves the long-established problem of forcing a choice between real-time or Unix systems, provides communication and memory control between the two processes, and allows close coupling through the use of system calls. Further details in December's issue.

Design of a single board computer

A study of design considerations for the construction of an s.b.c. for industrial use.

MIKE PARRY

The single board computer, s.b.c, is one of the fastest growing sectors of the European electronics market. By the year 1989 it is expected to be worth in excess of $500m, Germany and the UK having the lion's share with more than 50% of this market split between the two countries, Germany having 30% and the UK 27%.

It was with these figures in mind that I formed a company to design, build and market a range of simple, easy to use, s.b.cs.

USE AND USER

Single board computer applications can be divided into two broad categories – data processing and control and instrumentation. Design considerations can be similarly divided. A configuration that is ideal for data processing will be of little use to the control and instrumentation engineer, and vice versa.

In data processing, large amounts of data are to be manipulated at high speed, with disc storage, display systems and hard-copy being the normal requirements. It follows that many s.b.cs designed for this market use hardware based on, or compatible with, the many models or variations of the IBM-PC.

Control and instrumentation applications are quite different, requiring large quantities of i/o, analogue-to-digital converters, digital-to-analogue converters, communication ability, ruggedness, environmental protection etc.

Another consideration in the design of control and instrumentation s.b.cs is that the primary discipline of the engineers who will be using the products may well be anything but computing, their primary interest being hydraulics, chemical engineering, medicine or any other science or occasionally art.

With this in mind the term "user friendly" can take on quite different interpretations from its normal use in computing and must reflect the nature of the "user".

DECISIONS

With the above thoughts in mind, it may be instructive to look at one type of application – control and instrumentation–and discuss some of the design considerations that were relevant during the recent design plan for a family of s.b.cs.

A number of major decisions have to be made before any real work can commence. The order in which they occur depends upon one's point of view on the design, but this is how they appeared to me.

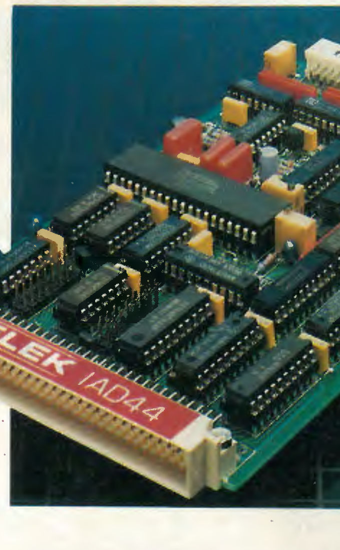
Which processor to use.
Board size.
Memory size, type.
How much i/o, which type.
Expansion facilities.
Power requirements.
Protection.
Housing.
Terminations for i/o.

As well as all the above technical considerations for the s.b.c. manufacturer there are the following major overriding requirements at each of the above stages.

Can I make it work at a reasonable cost?

Can I sell it in the right quantity at a reasonable profit?

In short; "Is my design what the world wants?" If it isn't, it doesn't matter how good the design is.



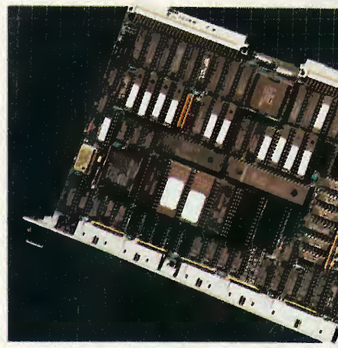
CHOOSING THE PROCESSOR

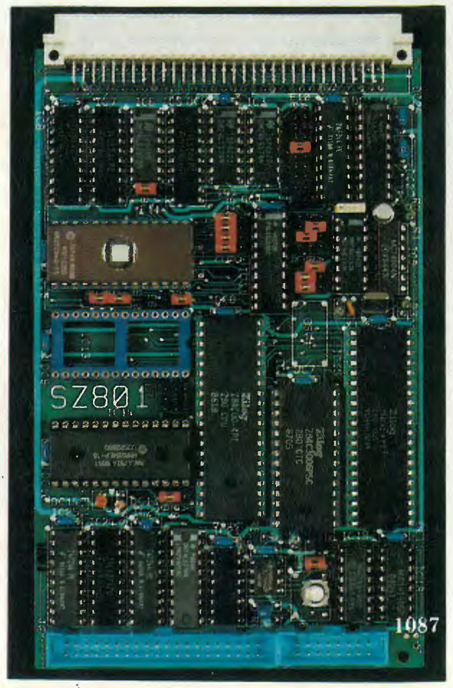
There are a considerable number of processors on the market today from which to choose. Some are very powerful state-of-the-art machines, others have been around for some time; but are still in common use. There are good arguments for the use of any of them, but some processors are more suitable than others for a specific application. Each processor is designed with a range of applications in mind and therefore should be selected primarily on this criterion.

With a short list of all suitable processors, the following criteria may be used to make the final decision i.e. manufacturer, cost, guarantee of supply, second source, power requirements and such like. As well as these obvious features the following should also be considered; technical support from manufacturer or supplier, the availability of in-circuit emulators, development systems and software.

With all this in mind the decision was made in favour of the MCS 8051 family from Intel for the following reasons:

- The MCS 8051 family has the world's highest volume sales for any 8-bit microcontroller and is available from a large number of second sources.
- The MCS 8051 devices have been available for some time and are all proven and tested, they are available in h.mos and c.h.mos for power saving and all run at speeds up to 16MHz.





The 8051/2 can be mask programmed devices while the 8031/2 use external eprom and the 8752 uses an internal 4K eprom which makes it ideal as a development tool.

The 8052AH Basic, which is an 8052 that incorporates an 8k control Basic mask programmed into its internal rom.

On technical support, considerable help was given by Intel's distributor Rapid Silicon of Nantwich, even extending to suggesting design improvements and extra features.

Whilst considering the many avenues opened to us during the development of this family of boards one anomaly in the support available for the chosen processor began to play on our minds. This was the lack of a low cost development system suitable for use by engineers wishing to experiment with these processors.

There are expensive in-circuit emulators, development systems, cross compilers and many other development tools available but they cost many thousands of pounds and are not cost-effective to the engineer wishing to develop a one-off project or a small company with limited funds, developing its first products. The more thought that was given to this, the more uses were discovered for such a system including the very considerable uses that the educational market could put to such a product. This eventually prompted a deviation from the original plan to build a number of fixed functional boards and instead design our own low-cost development system on which the rest of our boards would then be prototyped.

MCS51 family

Part	Technology	On-Chip Program Memory	On-Chip Data Memory
8051	HMOS	4Krom	128
8031	HMOS	none	128
8751H	HMOS I	4 Keprom	128
80C51	CHMOS	none	128
80C31	HMOS	8 Krom	256
8032	HMOS	none	256

BOARD SIZE

Once a decision has been taken as to which processor to use, the next problem for consideration is that of board size and format.

There are many existing board standards and in conjunction with these there are bus standards which must also be considered. In the present case the decision has been made to design s.b.cs for simple industrial use. It has been decided not to include an expansion bus but to provide a sufficient choice of i/o devices on the p.c.b. to satisfy most applications.

There are other pertinent reasons for not providing a bus system.

(a) Extra components are required on every board to interface to the bus, they all take up space and power.

(b) If not used properly, a bus can be a source of interference both to the s.b.c. and to other equipment in close proximity.

(c) Extra costs are incurred in the overall system implementation if numbers of small boards are joined by a bus structure. These costs manifest themselves in cases, racking and increased component count.

The size of the board used can generate a requirement for bus expansion if it is too small, and enough capacity cannot be accommodated on the one p.c.b. On this basis we have taken the double Eurocard format which gives 372cm^2 of board space with dimensions of 233 by 160mm. If a smaller board had been used the features would have been limited, the board less versatile and therefore less marketable.

A recognised standard board size as opposed to a board size just fitting the component space requirements, was chosen because enclosures, racking, and other associated hardware are available economically. All of this helps to keep overall project costs down for the end user.

MEMORY

Now the design is taking shape, the processor has been chosen and the board size and structure are set. The next step taken is to determine the remaining components required to make the circuit work. The choices are now limited within the minimal requirements of the processor and the maximum facilities that will fit into the space economically without complicating and cluttering the design.

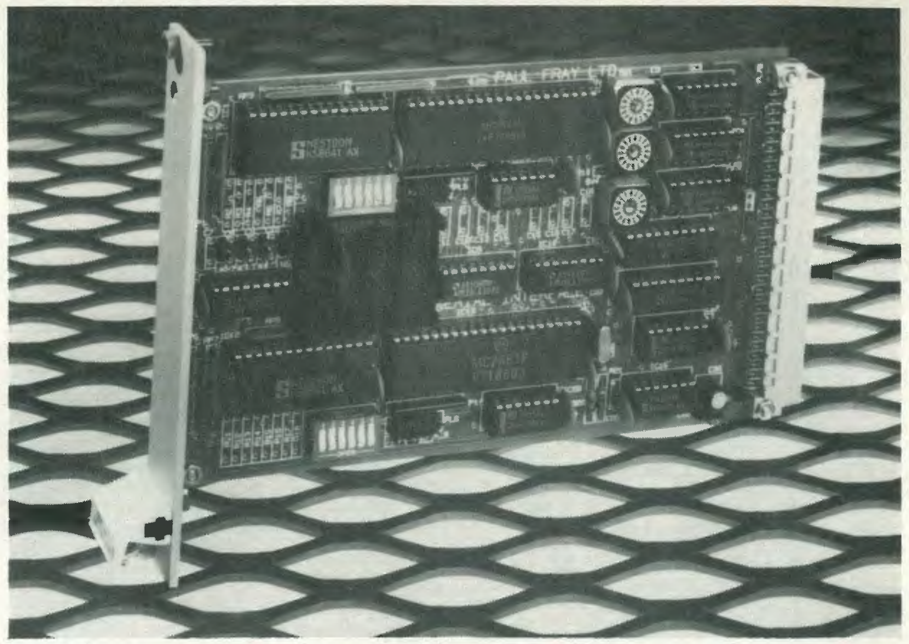
The 8052 Basic requires a minimum of 1K ram for it to work and can address a maximum of 64K in one address space. 1K is insufficient to be of any real use on a general purpose board. 64K of ram only, would not allow any permanent program storage and is too much for most applications. A compromise was made to give an equal split between ram and eprom so that there would be 32K of each.

The 8052 Basic has the unique facility of segregating assembly code program space and basic code program space, so the decision was made to include a further 16K eprom facility reserved solely for assembly code. 16K was thought to be quite adequate, as assembler code, written properly, is both compact and efficient, when compared with Basic.

As we only require a relatively small amount of ram (32Kbytes) static ram was chosen because of its simplicity of use and that 32K is now available in one 28-pin Jedec device.

Permanent program storage can now be accommodated by either, eproms or eeproms the decision on cost grounds was taken in favour of eproms despite the requirement for extra circuitry to program them as opposed to eeproms.

Another factor governing the decision, on both ram and eprom is that they are all packaged in Jedec-standard 28-pin devices which makes the layout of the p.c.b. much simpler than if a variety of devices had been used.



INPUT/OUTPUT

The amount of i/o and what types to employ are very much dependent upon the final use of the board. One can design a board suitable for use as a sequence controller and therefore have only digital i/o on the board. If temperature or pressure measurements are to be made then some form of analogue-to-digital conversion is necessary.

It is impossible to create a perfect solution to every possible problem on one s.b.c, there is just not the space. A compromise must be made or a number of different boards must be designed to cover the possible variations.

The one other solution is to make a board with minimal i/o and have a large amount of wire wrap prototype area so that the end user may add whatever circuits are required. This system is satisfactory for prototypes, very low volume and experimentation but where large volumes are required then a fixed-function board should be used.

It is impossible to satisfy all the market requirements in just one board so the decision was made that a number of boards would be designed. The processor section would stay the same on all of them but the main i/o area would change from board to board and therefore a family of boards would grow from the basic concept. Certain requirements are constant regardless of application, the components that form this part of the basic "engine" are, RS232 communications, list device output, ram, eprom, real time clock, non-volatile ram and processor.

A basic digital i/o device was included because even an analogue board might be required to control relays or monitor switches.

A new choice now emerged. If a common processor engine was to be employed, how does one plan ahead for all the possible i/o requirements, such as in decode logic? Fixed t.t.l. devices can be employed to decode addresses if the requirement is simple, but if the requirement is complex then large amounts of t.t.l. are undesirable and not very flexible, this is where programmable logic arrays come into there own.

By linking the top 12 address lines with the inputs of a programmable logic array and programming it accordingly the, decoding down to 64-byte boundaries can be achieved. If a large number of i/o devices are to be used they can be compacted together so as to release address space. With very little extra logic even tighter packing can be achieved.

The othere big advantage of pal's is the ability to re-program so that a totally different decoding pattern can be achieved from one basic component.

POWER

This is another subject where there are two schools of thought:
Off board power supply unit.
On board power regulation.

Both have their merits, but it was the latter that was chosen for this design.

With off board power supply units there is more space on the p.c.b. for components directly associated with the application and processor support, less noise on the power rails and possibly less heat. By having on board regulation one does lose a small amount of board space but on a double Eurocard this is very small in percentage terms. The main benefit is that external components are kept to a minimum and therefore so is cost. One power rail is brought onto the p.c.b. and all other voltages are derived from it. In many industrial applications there is often a low voltage d.c. supply available in the equipment racks that will have spare capacity.

PROTECTION

Due to the risk of inadvertently connecting a d.c. power source to the board in reverse polarity a large general purpose diode is connected across the power input terminal in its reverse bias mode. Therefore under normal conditions this diode will not conduct and is invisible to the system. If the board were to be connected incorrectly then the diode would conduct and pass all the power to ground. As long as there is a fuse, rated at a lower current than the diode, between the power supply and the s.b.c, then the fuse will blow thus protecting the s.b.c.

THE WAY AHEAD

The design for the intelligent prototype card is now basically complete. There is a common "processor engine" that can be used on a number of fixed function boards, thus reducing the design time and cost for each of them. Over the next few months a number of these boards will emerge.

This prototype board will be the first to be marketed and will lead the way for the rest in the following months.

There are no doubts that there is a market for them. As it was stated at the opening of this article, the market is huge, $500M by 1989.

This market can be broken down further into SBC types. Research suggests that there are four main areas of use for s.b.cs:

High performance technical, 27%
Low cost general purpose, 26.6%
Very high performance, 22.5%
Miniature military, 19.6%
Others, 4.3%

The low cost general purpose board at 26.6% represents $35m in the UK alone, or $133m in Europe.

The s.b.c. market is going to be with us for some considerable time and, it is hoped, will prove to be lucrative to the UK electronics industry.

Mike Parry is the director of a new company, Pinna Electronics, of Stevenston, Ayrshire, founded to produce a range of s.b.cs.

Enhancing IBM PCs, XTs and clones

These simple 'no-slot' additions to IBM PCs, XTs or their clones enhance performance without affecting software compatibility.

B. J. SOKOL

With a few minor modifications and a little additional hardware it is possible to speed up your IBM PC, XT or clone and add a reset button to provide more elegant recovery after a software failure. In many models, equally simple modifications increase memory capacity. This first section of 'the enhancing of the clone' discusses increasing the speed of PCs or XTs at minimal cost.

If your system board carries the usual 150ns drams and a faster c.p.u. is provided, a 6.67MHz clock can be substituted for the original 4.77MHz processor clock without causing problems (PC Technical Journal, February 1987, p.142).

Increasing clock speed though is not simply a matter of changing crystals because the clock generator of all members of the PC/XT/AT family has to produce a signal known as PCLK at 2.385MHz (half of 4.77MHz) in addition to the processor clock. System timers, dram refresh and serial communication with the keyboard are controlled by this signal so of course it cannot be varied.

A documented but little-known aspect of the Intel 8284 clock i.c. takes care of PCLK. With the help of a little medium-scale t.t.l., the clock i.c. is switchable between normal operation (PCLK=CPUCLK/2) and another mode in which it can produce two unrelated clocks, one for the processor and one for peripherals.

First it is necessary to replace the 5MHz 8088 c.p.u. found in most standard 4.77MHz PCs, XTs or clones. An 8MHz 8088-2 can be used, and is quite inexpensive. However for a little more money you can use instead a software and hardware-compatible 8MHz NEC V20 which further improves performance, Table 1. It also has an 8080 emulation mode and some extra instructions which can be used to advantage if you write your own software. No other chips in the computer need to be replaced for 6.67MHz operation.

After the c.p.u. is changed, and the system tested with the new processor, the 8284 must be removed from its socket and placed in a special adapter which then replaces it, as shown in Fig. 1. The adapter can be built with a socket and header arrangement, which is quite easy to make.

A small drill removes pin 2 of the header and a file removes pins 13 and 14 of the socket, after which the two are soldered together. The adapter connects to a small board carrying the switch, etc., by means of a six-way cable. This completes the 'turbo' speed-up modification.

Alternatively, you can use a small printed-circuit board to carry the 8284 and associated components, and connect it using an i.d.c. header and ribbon cable to the 8284 socket. This method, unlike the one using the special adapter, puts crystal and processor clock connections through a length of wire so the cable must be no more than 50-75mm long to avoid excessive capacitance and skew. The board can then be mounted on a drilled blanking plate.

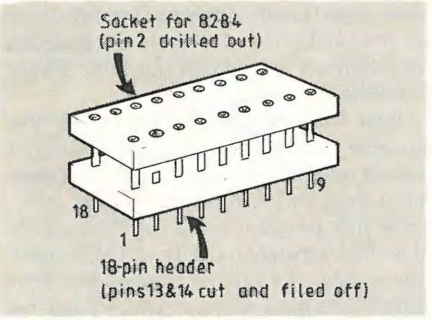
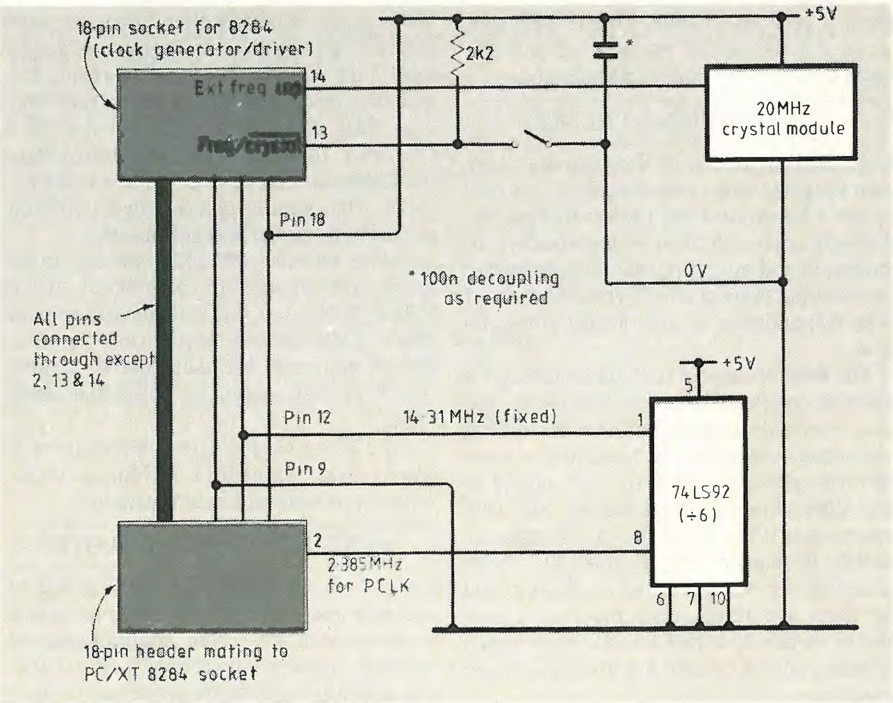


Fig. 1. This adaptor plugs into the 8284 socket to provide modified clock signals (above and below). Opening the switch selects high-speed mode.

With either modification method the functions of the added circuit are as follows. Note that the 8284 is still connected to its original 14.31MHz crystal so it still produces output on pin 12 at three times 4.77MHz. This signal connects to the second, slower, divide-by-six input of the 74LS92. This input accepts frequencies up to 16MHz, which is adequate for the 14.31MHz applied, and has the advantage over the faster option of producing a 50% output duty cycle. A symmetrical waveform is specified for PCLK.

With the switch closed (pin 13 earthed) the 8284 ignores the 20MHz signal from the module and produces a 33% duty cycle processor clock at 4.77MHz as usual. Normally pin two of the 8284 supplies the processor clock divided by two to pin two for PCLK, but this signal is replaced with the LS92 divide by six output. The result at pin two is



still 14.31MHz divided by six with 50% duty cycle. That makes PCLK the same as usual, and since the processor clock is still 4.77MHz also, the computer runs at its normal speed.

If the switch is in the turbo position the 8284 accepts the 20MHz module as the three-times source for the processor clock signal, giving a processor clock of 6.67MHz with a 33% duty cycle. However the 8284 still oscillates the 14.31MHz crystal on the PC system board and the 74LS92 chip produces PCLK with no alteration from the normal 2.385MHz.

The switch can usually be changed from normal to turbo mid stream, but a change in the other direction requires resetting. This is of little importance since normal speed is hardly ever needed. Very few programs use software timing loops which of course vary with processor speed; these require the switch to be placed in the normal rather than turbo position. The only such program I have found is the DOS format utility!

Speed improvement in turbo mode depends on the application; if there is intensive disc or other i/o, performance gain through extra processor speed is less significant. Of course if you use a ram disc the processor speed counts again, as discussed later.

With this accelerator in turbo mode in an XT, Norton Utilities' SYSINFO program indicates 2.6 times normal IBM speed. That is flattering but not very realistic; my own system-timing software described in my article about a processor-adapting eprom programmer (*E&WW*, July 1987) reports that the systems is running at only 1.48 times IBM speed.

Results of speed measurements vary with the mixture of instructions used in the test. Practical benchmark results are listed in Table 1. Note the increase of speed for heavily processor bound applications. A long cross compile or a Turbo Lightning spelling cleck (with dictionaries in memory), exceeds the actual proportional increase in processor speed, thanks probably to the V20.

Subjectively, the perceived increase in speed is very worthwhile. This is especially so as I have found no loss of full PC compatibility, and the cost is moderate.

A MORE ELEGANT RESET

If you add the turbo, or if you have a clone with the provisions to be described, it is easy to add a hardware reset button to your PC. Without such a button it is necessary to switch off and on again if the system freezes in a way that prevents the keyboard interrupt from responding to a 'cntrl-alt-del' combination.

The disadvantage of turning off then on is the wear and tear on your power supply – and your nerves if you do much software writing and experience crashes. Including a reset involves adding a switch to earth pin 11 of the 8284 chip described earlier. For IBM computers this must be a changeover switch. In many clones, a simple RC circuit produces the PWRGOOD signal on this pin and for these a normally-open monentary contact to earth will do just as well. Clones often provide pads for connecting this type of reset pushbutton.

Table 1. Benchmark results.

Test	Unmodified 8088 at 4.77MHz	NEC V20 at 4.77MHz	Turbo with 6.67MHz V20	Improvement turbo vs unmodi–fied
Batch file, heavy use of disc i/o	13.9s	13.8s	12.6s	10.3%
Cross assembler X6502 on 8K source file	57.1s	54.5s	39.3s	45.3%
Turbo lightning spelling checker on one page of text with 2 errors	19s	17.5s	12.4s	53.2%
Go to end of file (∧ QC)	11s	10.8s	8.6s	27.9%
Go to start of file (∧ QR)	25s	24.2s	20.8s	20.2%
Move paragraph from end to start	38.9s	36.6s	29.4s	32.3%
Move paragraph from start to end	37.3s	35.4s	28.3s	31.8%

Note that the bottom four tests are all using New Word III word processor with large text file.

A simple software tool can add to the usefulness of the reset button. The power-on-self-test or post routine executed after resets checks absolute memory location 472_{16} and if it finds data word 1234_{16} there it proceeds to a short rather than a long self-test routine.

This reset flag is set when you use cntrl-alt-del. It can be set also using a simple program to load the bytes into the flag location, so that the short test follows use of the reset button. Just include the program name (mine is called POST) on a line of your AUTOEXEC.BAT file.

Other software almost as simple as this can also enhance system performance. I include source code, List 1, and can supply object code, for 192.EXE and PK.EXE.

The first program resets the 8250 uart to allow data transfer on COM1: at 19 200 baud. This violates the rule on page 1-200 of the IBM XT Technical reference which reads, "in no case should the data rate be greater than 9600 baud", but if your software can cope with the increased rate there is no problem.

There is certainly no problem with *sending* data from the PC at a higher rate than 9600 baud, although there may be with receiving an uninterrupted stream at a high rate if the input processing overloads the system capacity (a higher clock rate may help this). I use 192.COM with my word processor to send text and control data (including fonts) to a laser printer at double speed. That greatly reduces the frustration caused by the serial port bottleneck.

Before you use 192.EXE first set up all serial communications parameters using MODE.COM. Any subsequent running of MODE.COM to set asynchronous parameters will reset the data rate to a value specified, that cannot be more than 9600 baud.

PK.EXE is a hard-disc parking program. It simply seeks cylinder 614. Its unusual virtue is its size, of only 0.5Kbyte assembled.

MORE MEMORY IN NO SLOTS

I found myself frequently running out of memory and unable to use some programs together with my usual configuration of memory-resident software and a virtual disc. I looked into the memory organization of my

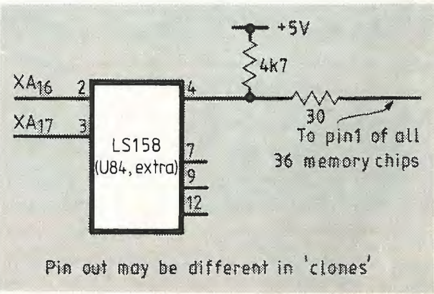


Fig. 2. Refresh circuit for 256K dynamic rams. This LS158 is in addition to the two used for 64K drams.

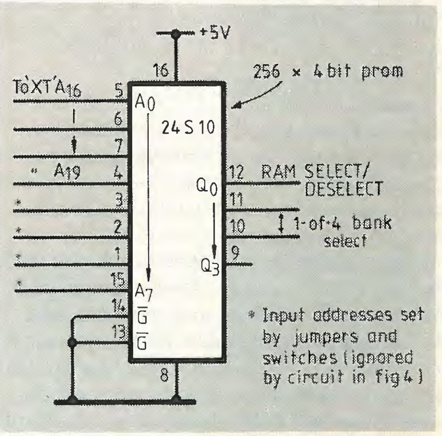


Fig. 3. Memory decoding is done by a 24S10 prom. This device breaks the 1Mbyte address space into 16 blocks of 64Kbyte according to the table below.

24S10 contents for a 640Kbyte system

24S10 inputs A_3 A_0	PC address range (64K)	Decoder o/p for 640K on main board using dram in 2 rows of 64K and 2 rows of 256K Q_3 Q_0	
0000	00000-0FFFF	0 0 1	Row 0 256K dram selected
0001	10000-1FFFF	0 0 1	
0010	20000-2FFFF	0 0 1	
0011	30000-3FFFF	0 0 1	
0100	40000-4FFFF	0 1 1	Row 1 256K dram selected
0101	50000-5FFFF	0 1 1	
0110	60000-6FFFF	0 1 1	
0111	70000-7FFFF	0 1 1	
1000	80000-8FFFF	1 0 1	Row 3 64K dram sel.
1001	90000-9FFFF	1 1 1	Row 4 64K dram sel.
1010	A0000-AFFFF	0 0 0	All deselected
1011	B0000-BFFFF	0 0 0	
1100	C0000-CFFFF	0 0 0	
1101	D0000-DFFFF	0 0 0	
1110	E0000-EFFFF	0 0 0	
1111	F0000- FFFFF	0 0 0	

XT clone and found to my surprise that the main board can hold much more memory than stated in the IBM specification.

Here I must restrict discussion to XTs and near clones, as memory is organized differently in different members of the PC family. Although it is undocumented, even older IBM XTs delivered with a 'maximum' of 256K memory on the system board can actually take 640K of dram. In fact, they and all XTs can hold even more ram on their system boards than is found in a full system. One consequence is that there is no need to buy memory boards to have a full system, and another is that one can go beyond a full system.

The trick is to use 256K drams in place of some or all of the 64K drams on the system board. IBM has partially done this with recent XTs, but older models and all clones I have seen are also suitable for this upgrade. This is because the larger memory chips are pin compatible with the smaller one, except for pin one which on the 256K type carries two additional address bits multiplexed, thus increasing addressing capacity by four. Refresh requirements for the larger dram type are identical to those for 64K type so there again the two types are plug-in compatible.

The IBM XT and all the XT clones that I have seen have pin one of the system-board memory array wired to hold 256K drams in all 36 sockets, and all have at least an empty socket for the multiplexer chip required to serve pin one. This multiplexer is a 74LS158 which fits into XT empty socket U_{84} (numbered the same on my clone).

Look for the LS158 connected to the memory array in the manner shown in Fig. 2; if it is an empty socket, supply this chip. Now your XT is ready to become a 640K system with no additional memory boards (set the system-board switches for '256K'). the next step is to replace the 64K dram chips and change a decoder rom.

Many clones and recent XTs are sold with the extra LS158 already installed and with 640K of dram on the system board. Even with these systems you can go further and replace all 36 drams with 256K devices to provide 1Mbyte of parity-checked memory.

This memory is fully functional in terms of refresh, and it is properly placed on the address and data buses, but it cannot be accessed because a decoder prom tells the system that memory beyond 640K is not ram. This prom reserves 384K of the processor's 1Mbyte address space for roms, video buffers and so forth. If some of these are not used, the extra memory *can* be accessed.

Modifying the decoder is not difficult. On the PC XT, and on my clone, it is U_{44} – a 24S10 fuse-link prom. This decoder breaks down the entire 1Mbyte of 8088 addressing space into 16 blocks of 64Kbyte each. For each block it chooses one of the four banks of ram (one of the four rows of nine devices), or no ram at all. Of the rom's four output bits, only three are used, two to encode which of four device banks is addressed (by RAS and CAS), and one to deselect ram for unwanted blocks Fig. 3.

Conveniently the IBM XT rom contains several different decoding schemes selectable by jumper. One of these allows the use

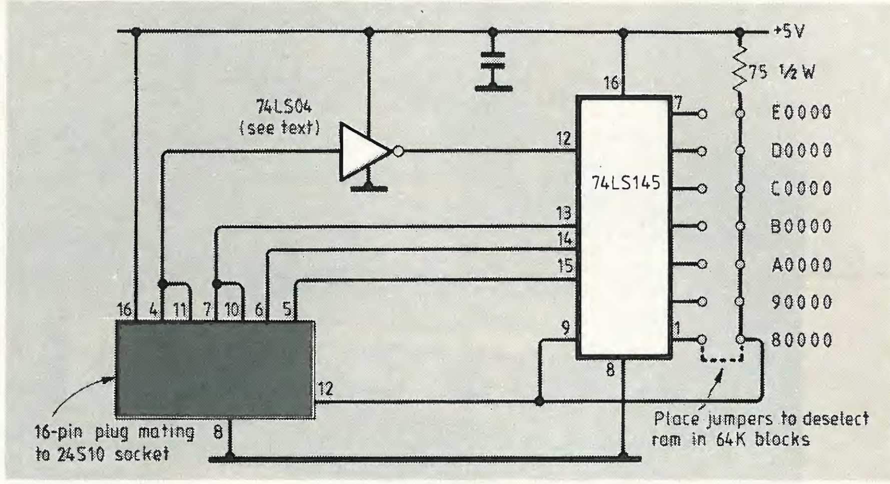


Fig. 4. This replaces the 24S10 (U_{44} in the XT) to allow the use of 256K drams in all memory sockets. You need an LS158 in empty socket U_{84} but no jumpers are needed.

of 640K on the system board of 256K systems; it is selected by connecting together positions one and two of system-board jumper E. To use this option you have to change the memory i.cs in banks zero and one for 256K drams.

That takes care of updating older XTs, but to go further you can replace not only two but either three or all four banks of memory with 256K drams. Then by using an appropriate decoder rom you can take advantage of as much of the 1Mbyte processor memory space as your system configuration allows.

First you have to decide which of the sixteen 64K blocks in the 1Mbyte space can be used for ram. It is always all right to use the first ten blocks, the ones starting at

List 1. Source code for high-speed serial transfer on COM1: and seeking hard-disc cylinder 614.

```
CODE    segment
        assume cs:CODE, ss:STACK
START:
MOV AH,0CH
MOV AL,01H
MOV DH,00H
MOV DL,80H
MOV CH,66H                      ;THIS AND
MOV CL,91H                      ;THIS MAKES CYL NO = 266H OR 614, SECTOR=17
INT 13H
MOV AH,4CH
INT 21H
CODE    ends

STACK   segment stack
        assume ss:STACK
        dw      10 dup(?)
STACK   ends

        end     START
**********************************************************************
DATA    segment AT 0000
org     400h                    ;stores com1 base address
PORT    label   word
DATA    ends

CODE    segment
        assume cs:CODE, ds:DATA
START:
        mov     AX,0000
        mov     DS,AX
        mov     DX,DS:PORT
        add     DX,3            ;giving line control register
        in      AL,DX
        mov     BL,AL           ;save lcr
        or      AL,80h          ;set DLAB bit
        out     DX,AL           ;send it
        sub     DX,3
        mov     AX,0006
        out     DX,AX           ;sets 19200 baud for Com1
        mov     AL,BL
        add     DX,3
        out     DX,AL           ;restore lcr
        mov     AH,4Ch
        int     21h
CODE    ends

STACK   segment stack
        assume ss:STACK
        dw      64 dup(?)
STACK   ends

        end     START
```

addresses 00000 to 90000, for those are within the 'legal' 640K DOS limit. Beyond 640K typical uses of memory space are:

Block beginning	Function
A0000	EGA buffer in APA mode
B0000	Mono and color-video buffers
C0000	Hard disc control
D0000	Not usually used
E0000	Not usually used
F0000	Boot, BIOS and Basic roms.

These functions occupy much less than the 64Kbyte (10000_{16}byte) bands, but because the decoder sees only 64Kbyte blocks, if any part of a block is used for non-ram purposes then all of its 64K address range must exclude ram. Altering the allocation by changing only the socketed decoder chip wastes a lot of usable ram space, which is a pity, but this must be accepted because any other solution would require much more difficult hardware alterations.

To access the extra memory you must replace the existing decoder prom either with a new prom or with the circuit in Fig. 4. Programming services can make 24S10 decoders, and it is easy to design them to control any combination of 64K and 256K dram. If only 256K devices are used however, the two-chip circuit shown in Fig. 4 gives more flexibility. Slide-on jumpers configure this circuit to emulate any decoder prom that you may need.

Using all 256K drams allows address lines 18 and 19 to be used directly for chip selection. Pin pairs 7/10 and 4/11 of the 24S10 socket are simply tied together. The remaining job, to decode out unwanted blocks, is achieved in a somewhat unusual way.

Normally the 74LS145 acts as a 1-of-10 display driver; it can sink 80mA at any of its open-collector outputs. This drive capability must be used to obtain a response time matching the 55ns maximum switching time of a 24S10 – the 75Ω value for the pull-up resistor in Fig. 4 is not a misprint. A 74ALS, S or F type '04 would speed response although I have not found it necessary. The purpose of the '04 is to force all input addresses below 80000_{16} to produce invalid or unnoticed codes. The result is that jumpers placed in the appropriate positions send pin 12 low, emulating the function of the 24S10 when it decodes corresponding 64K sections of ram.

What can be done with the extra memory? Rather surprisingly, added memory contiguous with the usual 640K ram area, the 64K from A0000 to AFFFF, is automatically picked up by PCDOS; the sign-on message reports 704K of memory and the availability of this memory is confirmed by CHKDSK, by the diagnostic disc, and by the Norton Utilities SYSINFO program (which calls it 734K). DOS is apparently ready to use as much contiguous ram as you offer it.

However the 64K block beginning at B0000 is normally used for video buffers, and that effectively stops DOS from accepting memory beyond 704K. Only PCDOS version one could use non-contiguous memory. Moreover if you use an e.g.a. card in full-graphics mode, the block starting at A0000 is also used for video, which restricts DOS to 640K. Some clone Bios's may prohibit the use of ram between A0000 and AFFFF, or they may require use of the F1 key at boot time. But none of these problems are terminal, for there is a use for the extra ram even if the DOS won't recognize it.

The ram that DOS cannot recognize is usable as a ram disc. I use the section of memory from C0000 to EFFFF in my clone to provide such a very-fast and totally-silent disc. This requires a special driver I have written called RD.SYS; the ordinary DOS VDISC driver cannot access memory between C0000 and FFFFF. I have also written software (RD128.SYS) to configure a ram disc extending from D0000 to EFFFF to provide room for a hard-disc controller.

In order to provide low level DOS services while applications programs are in progress these programs must be memory resident. I have written them not as ordinary terminate-and-stay-resident programs, but rather as installable device drivers. These drivers link to the DOS in such a way that virtual discs are added without the need to alter system-board dip switches. That in turn allows other special disc device drivers (such as multi-disc format programs) to be installed without conflict.

Installable device drivers are initialized and put in memory at reset by inclusion of the line

DEVICE=RD.SYS (or DEVICE =RD128.SYS)

in the CONFIG.SYS file in the root directory of the boot disc. The driver then becomes an extension of DOS and coexists with any other discs or software discs that DOS currently recognizes.

The RD.SYS program code is less than 1K in length, and once it is resident the RD driver occupies only 333 ram bytes. It is constructed by creating, assembling and renaming a special EXE program whose origin is zero. This program starts with a special header recognized by DOS as the start of a device driver; its purpose is to respond to a number of requests sent by DOS through pointers to data blocks. Details of the header, request blocks, and the disc organization to be emulated are all in the DOS technical-reference manual.

The enhancements described produce a system that is compatible with all PC hardware and software, and which offers unusual capacity, speed, and silence.

The author is supplying RD.SYS, RD128.SYS, 192.EXE, POST.EXE, and PK.EXE programs in exchange for £15, a formatted 5¼in DOS disc, and an addressed disc mailer. The software includes source and execution code for the vox program described in the August issue on p.807. Printed-circuit boards for these enhancements may also be available. Write to B. J. Sokol at 47 Grafton Road, London NW5.

The Janus link: two for the price of one?

This trick was devised as a modification to a radio-coupled stimulation system, to enable two independently-adjustable stimuli to be delivered. It may have application in quite other signalling systems.

P. E. K. DONALDSON

Stimulation of nerves is most usually achieved using nearly-rectangular pulses of current, but capacitor-coupled so that there is no net transfer of charge through the load impedance (two metal electrodes in contact with nervous tissue). Absence of net charge transfer helps to prevent destructive electrochemical processes at the electrode-tissue interface (Fig. 1).

Pulse durations are typically in the range 10-500 µs. Over this range, nerve fibres will be stimulated if the charge displaced by the pulse exceeds a threshold.

Since charge=current×time, a pulse can be made more potent by making it either taller or wider. So the pulse carries redundant information. It is characterized by two parameters, amplitude and duration, only one of which need be used to specify the shock strength. The other is normally wasted and could be used to do something else.

A useful 'something else' would be control of another stimulus, delivered by a separate pair of wires to a separate pair of electrodes. Consider the circuit shown in Fig. 2, which is an adaptation of a separation-insensitive-link receiver[1,2,3], having two secondary windings on the transformer instead of one. C_4, R_3 and C_7, R_7 have relatively long time constants. Their job is to prevent net passage of charge through the tissue load resistance; otherwise they play little part in the action of the circuit.

If a rectangular pulse of r.f. is intercepted by L_1, then, at the front edge of the pulse, C_3 charges (partly through R_2, but mainly via D_1), the first tissue load (about 500 ohms) and C4, with time constant 50µs. At the end of the pulse, D_1 cuts off. A minute current, controlled by R_3, flows back through the load as C_4 discharges; meanwhile C_3 discharges through R_1 and R_2, leaving the circuit dead and awaiting the next pulse.

Furthermore, at the front edge of the pulse Tr_1 cuts off and C_6 charges partially, via R_5, D_2 and R_6. D_4 cuts off and nothing happens at the load. At the end of the pulse, D_2 cuts off, Tr_1 is turned on hard and C_6 discharges, mostly via D_4, C_7 and no. 2 tissue load, but partly through R_6. When C_6 has discharged, a minute current flows back through the load as C_7 discharges through it and R_7. The circuit is then dead, awaiting the next pulse.

The effect is to produce a pair of exponential-discharge-type pulses, one coincident with the beginning of the r.f. burst and one with the end. Janus-like, the receiver looks forward to get one output and backward to get the other. Both pulses vary in amplitude with the amplitude of the r.f. burst, but the second pulse is $[1\text{-}\exp(-t_0/T)]$ of the size of the first, where t_0 is the pulse duration and is the charging time constant of C_6, which can be trimmed by adjusting R_5 (Fig. 3).

Although this arrangement has the merit of giving two outputs with some independence, using a conventional pulse generator to modulate the r.f., it is not at all convenient in practice: one has to know in advance that one will always want the first output larger than the second; and to hold the second

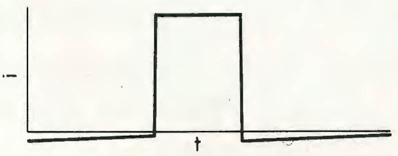


Fig.1 The nearly-rectangular pulse, a popular form for nerve stimulation.

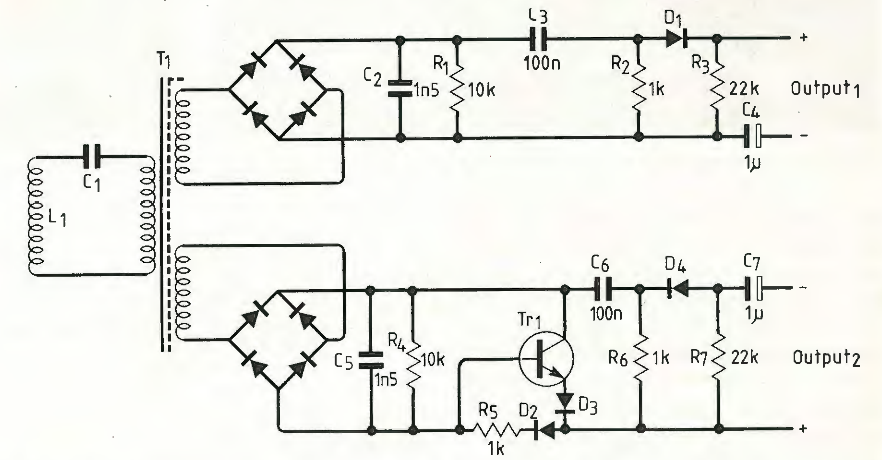


Fig.2 (above) Janus receiver. Electrode geometry is such that the tissue load resistance is about 500Ω.

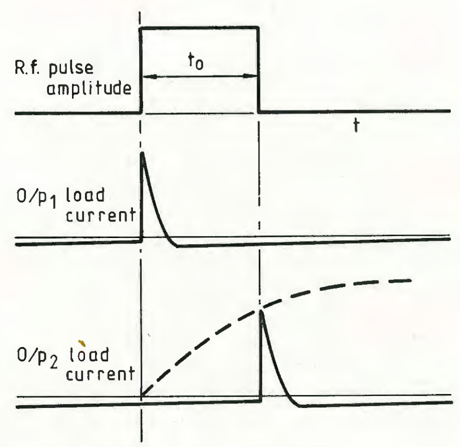


Fig.3. Outputs of a Janus receiver fed with a conventional rectangular burst of r.f.

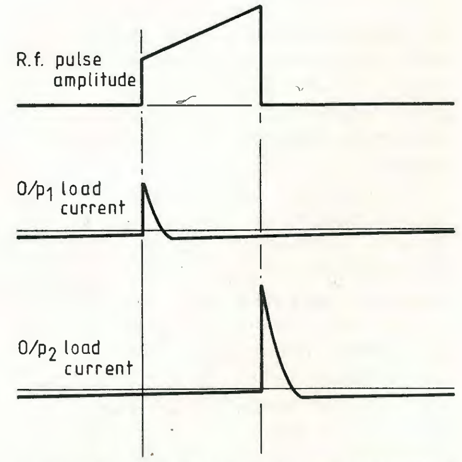


Fig.4. Outputs of a Janus receiver fed with a penthouse-modulated burst of r.f.

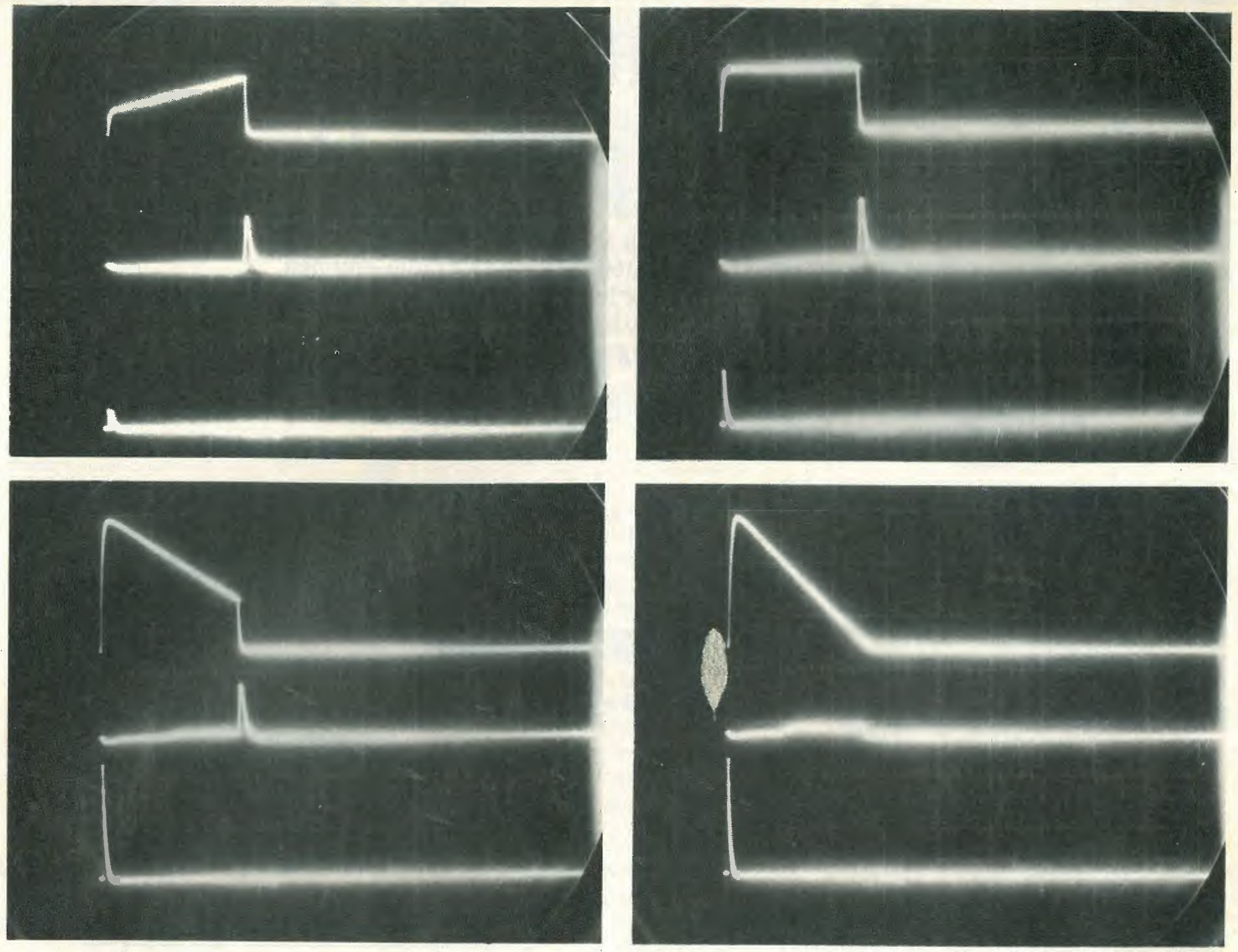


Fig.5. Penthouse generator waveforms with corresponding receiver outputs. Timebase velocity: one division per millisecond.

pulse constant while adjusting the first requires a means of altering the amplitude and duration of the r.f. burst in opposite directions and in correct proportion.

A much better arrangement is to use a penthouse modulating waveform of long (3ms) duration so that C_6 charges fully, and to arrange that the front and back edges of the penthouse are separately adjustable.

Output of the first receiver will then be proportional to the step at the front edge, and that of the second will be proportional to the step at the back edge (Fig. 4, 5).

If A is the front-edge step up and B the back edge step down again, and V the instantaneous value of the penthouse required, then V=0 when $t<0$, $V=A+(B-A)(t/t_0)$ when $0<t<t_0$ and V=0 when $t>t_0$, which can be made by elementary analogue computing methods, Fig. 6.

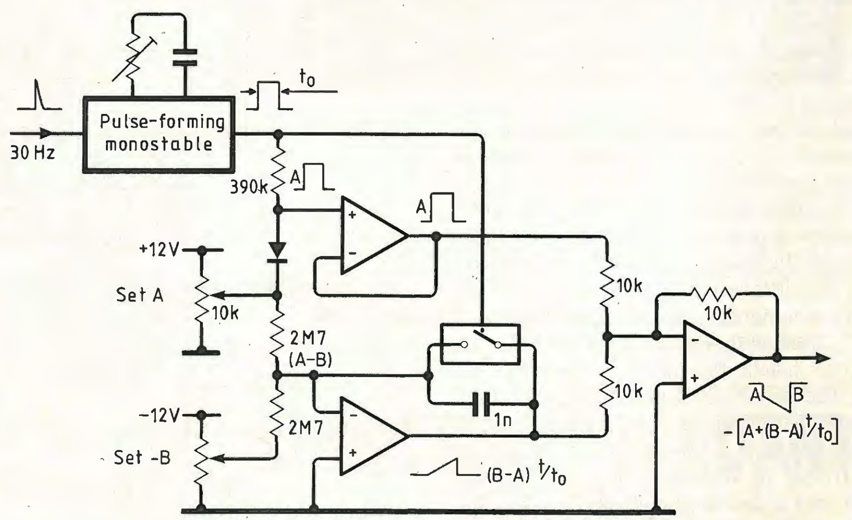


Fig.6. Penthouse waveform generator. A further polarity inversion is provided by a type 165 power operational amplifier acting as modulator. Adjust the monostable pulse duration so that, with B set to zero, the generator output is also zero just before the end of the pulse.

Two legitimate questions are, "Are the receiver outputs determined only by the steps at the beginning and end of the penthouse? Won't the ramp part of the wave cause some sort of output?" The answer to these is: when the ramp is positive-going, the second output is unaffected because D_4 is cut off; similarly when the ramp is negative-going, the first output is unaffected because D_1 is cut off. When the ramp is positive-going, output 1 has a very slightly disturbed baseline: C_2,R_2,C_4 and tissue load 1 form a second-order filter which, after an initial transient, will produce no output for a constant rate of change at the input. Similarly for negative-going ramps and output 2 a corresponding second-order filter is formed by C_6, R_6,C_7 and tissue load 2.

Peter Donaldson is with the Medical Research Council's Neurological Prostheses Unit.

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RESEARCH NOTES

One-electron electronics

Is it possible to build a computer which uses lone electrons to store and process information? It is, according to experiments staged by Leonid Kuzmin and Konstantin Likharev of Moscow State University and reported by the Novosti Press Agency.

According to quantum physics, when a layer of insulator is sufficiently thin, there is a probability that an electron may cross it from one conductor to the other by means of tunnelling. The tunnel effect has, of course, been known for a long time and is applied in many devices. What Kuzmin and Likharev are exploiting is the fact that electrons penetrate the barrier one by one. Their experiments indicate that it should be possible to measure such single-electron transitions.

Two conductors separated by an insulator are nothing but a capacitor, and a change in its charge causes a jump in the voltage across it. The smaller the capacitance of the capacitor the greater the jump. Today it is possible to have a tunnel junction spread over an area of 10^{-8}mm^2. Its capacitance is so small that the voltage drop caused by a single electron can be readily measured.

Electrons tunnel across such a junction in a somewhat unusual way. As soon as one particle seeps through it, a voltage jump is registered in the junction, preventing the movement of the next electron. Even more curious is the movement of electrons across two series-connected junctions. An example of such a system is a microscopic bit of metal separated by thin insulating layers from the conductors connected to it on either side. It appears that if this bit of metal is not initially charged, and the voltage applied between the conductors is not very great, no current will flow through the system. If, however, an extra conductor imparts this bit a charge, however infinitesimal, the path will be free for current to flow. In this way, two series-connected jumps represent a one-electron analogue of the transistor – a device capable of amplifying electric signals.

The electric characteristics of such a transistor when measured by the Soviet physicists proved to be in full accord with theoretical calculations. Similar experiments have now also been staged by two groups in the US – AT&T Bell and the University of Notre Dame, Indiana.

An interesting application for one-electron electronics would be computer memories. Since the presence or absence of an electron in a conducting cell would determine the movement of particles across neighbouring junctions, a system could be made capable of processing information. In the absence of external impulses, the electron would remain in the cell where it was. This means that such a system could be used as a large memory, storing information without energy loss.

World's smallest transistors

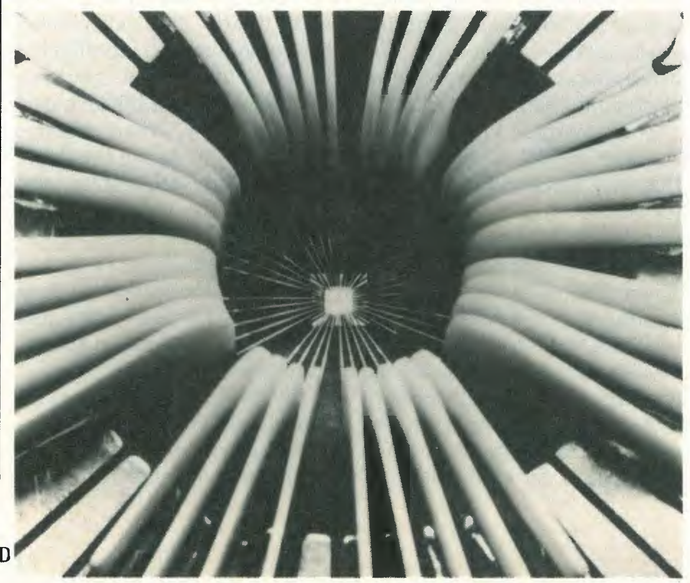
Scientists at the IBM Thomas J. Watson Research Centre, Yorktown Heights, N.Y., have obtained the first device-performance results from experiments designed to assess fet technology in the 0.1 micron gate-length regime.

Until these latest results, it wasn't known for sure whether transistors could be made with parts so small and yet with good performance characteristics. Although others have made transistors in which an individual key part has been this size, IBM scientists claim to be the first to have miniaturized all the critical parts – some to less than a tenth of a micron, or only a few hundred atoms wide.

In their latest report (*IEEE Electron Device Letters,* 1987) the IBM scientists report device characteristics in excess of 750mS/mm transconductance (a basic factor of transistor speed), which is the highest value obtained to date in silicon fets. The experimental transistors are nmos field-effect transistors (designed with the high performance needed for ultra-large-scale-integration (u.l.s.i.) in mind. Logic chips based on tenth-micron technology could hold millions of logic elements that switch in as little as 10 picoseconds, ten times faster than those commonly used today.

Experimental techniques used to make and test the transistors include advanced lithography for writing ultra-thin lines and cooling the devices during operation to – 196°C in liquid nitrogen. The basic design technique for microelectronic circuits, called scaling theory, was developed in the 1970s. Scaling theory predicts the geometric and electrical constraints that must be observed as device size decreases. For tenth-micron technology, scaling theory predicted that physical limits were being approached: at room temperature, voltages large enough to switch the tenth-micron transistors on and off would, in time, damage them. The IBM solution was to change the physical characteristics of the devices by operating them in liquid nitrogen where a lower voltage is required for proper switching. Also, at this temperature the speed of signal-carrying electrons significantly rises, allowing the transistors to operate faster.

The electron-beam lithographic tools used to make the tenth-micron transistors are capable of writing lines many times smaller than those possible with conventional optical lithographic methods. The e-beam tools IBM used are capable of writing patterns with dimensions several times smaller (0.02-0.05microns) than the tenth-micron fet linewidths. These tools are currently used to explore the characteristics of structures – for example metal conduction lines – in this even smaller range.



Multipath-resistant direction finding

A direction-finding system that will identify and locate radar emissions to an angular accuracy of better than 1° is described in Philips' Annual Review. What is novel is the ability of this experimental system to maintain its accuracy in the presence of strong multipath reflections.

Existing direction-finding systems achieve their angular accuracy by means of very long baseline interferometry. Identical receivers are set up several km apart and log the time of arrival of radar pulses from the transmitter whose bearing is being plotted. A long baseline means that the time difference is relatively large and can be measured without the need for extreme precision. The disadvantage is that multipath or interfering pulses are likely to arrive within the measurement time window, hence causing confusion.

The Philips system uses receivers spaced only a few metres apart on a single site. This means that pulses from a single transmitter are bound to arrive at all the receivers within a time window of less than about 100ns. The probability of reflected signals or signals from a second transmitter arriving within this time window is vanishingly small.

The equipment developed by Philips consists of several wideband r.f. receivers, all coupled to e.c.l. circuitry capable of measuring time differences of 1ns. Because of the potential ease of integrating all these elements, the researchers believe that it offers the possibility of cheap, light and accurate commercial d.f. equipment.

To validate their claims, Philips conducted experimental trials on the south coast of England using a computerized data-collection and validation system. The signal path was over the horizon from a radar located at Caen in France. With a baseline of 17.5m, positional accuracies of 0.2 – 0.4° were regularly obtained in the presence of strong multipath propagation.

High temperature superconductor

A way of increasing the transition temperature of yttrium barium copper oxide superconductors by more than 30 degrees is described by four researchers from the University of New South Wales, Sydney. (*Nature* vol.328 no 6133). The technique is to soak a sample of the ceramic material in gaseous nitrogen for several hours. One sample which, when first prepared, had a transition temperature of 88K, could be turned into a superconductor by cooling to only 131K after the nitrogen treatment, a finding replicated with a second sample.

While this development appears to have no great practical importance, it should be a valuable pointer to the reasons why these materials become superconducting in the first place.

Daresbury 25th anniversary

This year the Science and Engineering Research Council's Daresbury Laboratory is 25 years old.

Alongside the large experimental facilities, Daresbury has always been a strong centre for scientific computing, the development of electronics and for high-quality engineering to support academic research.

The most recent project in scientific computing at Daresbury is intended to develop ways of using the latest generation of transputer-based processors based on the FPS series of 'supercomputers'. To exploit this technology for UK computational scientists, an Advanced Research Computing Group has been set up to develop the new kinds of software that will be needed.

Central to the project will be a T-20 machine with a highly parallel architecture based on 16 interconnected transputer-based nodes. The task of the Daresbury group will be to develop ways in which this architecture can best be exploited for advanced scientific research. Numerical modelling in quantum chemistry, geophysics, fluid dynamics, meteorology and particle physics are all areas in which distributed processing could play a valuable part by increasing the speed of operation by several orders of magnitude over today's best sequential computers.

How electrostatic discharge does its damage

The extent to which random electrostatic discharges can damage electronic devices and systems during production and therefore affect their reliability in service continues to be a major source of concern to the electronics industry.

In an effort to overcome the problem, ERA Technology has launched a new research project which will compare proprietary electrostatic discharge test equipment and identify the type which simulates best the discharges associated with a statically charged operator. The equipment will then be used in the development of an effective test strategy for identifying the most sensitive device pin and determining its vulnerability to electrostatic damage.

The new study follows earlier research by ERA which revealed that the susceptibility characterstics of many systems are poorly defined, due to the variability of the devices themselves and to uncertainties in existing test methods. Priority will be given, therefore, to the development of an effective test for comparing the efficiency of system protection methods. The results of the programme, which will include an examination of the immunity measures required for typical electronic equipment, will facilitate the selection of cost-effective protection measures.

For further information on this multi-client sponsored project, contact Brian Roberts, Electronic Materials and Components Department or Tony Maddocks, Electromagnetic Compatibility Department, at ERA Technology Ltd, Cleeve Road, Leatherhead, Surrey, KT22 7SA.

Translating speech by computer

People who cannot speak a word of each other's language could soon be able to exchange a limited amount of information over the phone using a system developed by British Telecom.

What is claimed to be the world's first rapid translation of speech by computer was unveiled recently by British Telecom's Research Laboratories at Martlesham. Simple sentences of business English were translated into French and vice-versa. The prototype equipment can translate English into German, Spanish, Swedish and Italian and the reverse capability is being developed. This will then also make possible translation between any pair of these languages, such as French-German, Swedish-Italian.

For the demonstration, each speaker had a microphone linked to a Merlin 5200 personal microcomputer, the computers being connected together by an RS232 data link. The first participant spoke a sentence in English into his microphone, saying each word clearly and deliberately. The computer then repeated the sentence in its own synthetic voice to check that it had understood correctly. When this was confirmed – by saying the single word 'yes' – the originating computer sent the message to the other computer which translated and spoke it in French in its own synthetic voice. When the French speaker replied, the process was repeated in the reverse direction.

The system is based on a set of more than 400 phrases in common business use stored in each computer's memory. Although this involves a vocabulary of more than 1000 words, the computers are programmed to recognise only 100 key words. These are used to identify the appropriate phrases, reducing the word-recognition task required. Studies have shown that speech recognition is especially prone to error, but that errors can be avoided if the domain of discourse is restricted.

The system also recognises spoken proper names - such as John Smith, for example – and makes no attempt to translate them, e.g. rendering "Mr White" into "Monsieur Blanc". Instead the names are repeated in the original speaker's voice embedded in the synthesized translation.

Speaker-dependent isolated-word technology is at present used, which means that the system will not yet accept normal speech. The recogniser must also be trained to the voice of each speaker if an acceptable performance is to be obtained.

Phrase parameters such as dates are processed by first identifying the basic phrase using key word recognition. The position of the date in the phrase can then usually be deduced, and a second recognition scan is carried out over a recording of the original utterance, but this time only recognising "date" words. This manoeuvre increases the effective vocabulary of the recogniser without degrading performance.

In future, speech recognition devices are expected to become speaker-independent and handle continuous speech with large vocabularies. Recognition of intonation and stress will reveal additional levels of meaning which are all used in day-to-day speech and may need to be translated. Synthesizers are also likely to produce more natural-sounding speech which can be matched to the voice of the original speaker.

B.T. say that all these advances could be built into their system offering a considerable increase in versatility. As for practical applications, it would depend on the eventual degree of miniaturisation. B.T. don't discount the possibility of a pocket-sized black box that could be carried around by tourists. Comment allez vous?

Research notes is compiled by John Wilson.

Bessel and his functions

"What's so special about Bessel?"

Joules Watt

During a discussion of loudspeaker design with a group of students, the mention of Bessel functions prompted one student to respond with, "Oh those – we covered them in the course on special functions. I keep the notes in a file called 'very special functions' together with other notes that I cannot understand." A touch of cynicism I thought, but yes, Bessel functions do have that reputation.

I can imagine that Bessel himself had quite a struggle with an integral that turned up in his work on Kepler's problem. The particular expression,

$$J_n(x)=\frac{1}{2\pi}\int_0^{2\pi}\cos(n\theta-x\sin\theta)d\theta$$

does look a little awesome and no solutions have been found for it using elementary methods. By elementary I mean the solution of many simpler integrals by standard methods, which really amount to differentiating the answer to get back to the integrand in the integral.

What enables you to call the method elementary is the closed form of the solution. The problem is that even sine and cosine, in other words ordinary trigonometrical functions, are non-algebraic, or trancendental functions that do not fit comfortably into the simple definition just given. They should also be in the special function category, but have become so widely used that we place them squarely into the elementary group.

This continues to be true if we handle sine and cosine as complex number powers of e via Euler's identity which I discussed earlier[1]. But all these functions come from power series and are transcendental, in the same way that Bessel functions are.

SERIES YET AGAIN

Bessel proceeded to find a series-type solution of the previous equation that fitted the problem. Hence he obtained actual values for the special functions $J_n(x)$. He investigated their properties and drew up tables of them. I am sure that some of you have come across $J_n(x)$ in articles and lectures – or even looked up a solution in tables of these rather formidable Bessel functions. Therefore taking a deep breath I thought we might plunge in and see how far we could retrace some of the steps Bessel might have taken.

FRIEDRICH BESSEL

Friedrich Wilhelm Bessel, born at Minden on 22 July 1784, became an astronomer, who in effect inaugurated the modern era of precision work in that field.

At fifteen, he started studying accountancy at Bremen, but soon left to go to sea, studying navigation, mathematics and then astronomy. By 1804 Bessel had calculated the orbit of Halley's comet from Thomas Harriot's 1607 observations.

In 1810 the King of Prussia appointed him director of the new observatory at Konigsberg, where he did all his remaining work. His peak successes include measurement of a stellar parallax amounting to 0.31" for the start 61 Cygni, which showed that many star distances could be found directly. The attack he made on Kepler's problem in 1817 had systematically produced the solutions we now call the Bessel functions, $J_n(x)$., Seven years later Bessel fully developed these functions in research on planetary perturbations (Transactions, Berlin Academy, 1824).

As usual, Bessel shares some of the glory with other mathematicians who form a surprisingly tightly-knit group. Thus Daniel Bernoulli had in effect obtained $J_0(x)$ (the zero order Bessel function) in work on oscillations of a chain suspended at one end. Yet again in 1764 Leonhard Euler used the functions of zero and integral orders in analysis of vibrations of a stretched membrane (which apply to the loudspeaker cone problem). The functions have proved remarkably fruitful in the whole field of electronics.

Fourier[2] used similar methods in his thinking about the heat flow along bars (applied now to the theory of heat sinks among other things). By analogy W. Weber, G. Riemann and S. Poisson investigated the flow and surface density of electricity, later leading to skin effect, and distributions on cylindrical conductors. Sir J.J. Thomson, H. Hertz, Oliver Heaviside and Lord Rayleigh, treated electromagnetic waves on wires and in tubes, (transmission lines, aerials, waveguides, etc.).

Therefore, Bessel's systematic treatment of one integral, permeates the whole field of modern technology.

FINDING THE SERIES

When j arose for discussion[1] I pointed out that Euler had given us the well known relationship between the exponential series and the trigonometrical series,

$$e^{j\theta}=\cos\theta+j\sin\theta.$$

From this, we found that the cosine has a series,

$$\cos\theta=1-\frac{\theta^2}{2!}+\frac{\theta^4}{4!}-\ldots$$

and so on. Also,

$$\sin\theta=\theta-\frac{\theta^3}{3!}+\frac{\theta^5}{5!}-\ldots$$

But the other remarkable series of great worth in nearly all electronics theory arose from Fourier's work on heat[2]. As you know, he showed that a complicated periodic wave is made up of numerous simple sinewaves added together, which we call the harmonics. Written out Fourier's series looks like,

$$f(t)=\frac{a_0}{2}+a_1\cos\frac{\pi t}{\tau}+a_2\cos\frac{2\pi t}{\tau}+\ldots+a_n\cos\frac{n\pi t}{\tau}+\ldots$$

$$+b_1\sin\frac{\pi t}{\tau}+b_2\sin\frac{2\pi t}{\tau}+\ldots+b_n\sin\frac{n\pi t}{\tau}+\ldots$$

in which the first term gives the constant, or in our parlance the d.c. value. In the rest of it, the cosine terms yield the even part of the expansion, and the sine terms give any odd part.

THE BASIS OF THE PROBLEM

A look at the inside of the Bessel integral, called the integrand, shows that

$$y=\cos(n\theta-x\sin\theta)$$

so

$$y=\cos n\theta\cos(x\sin\theta)+\sin n\theta\sin(x\sin\theta)$$

by expanding the cosine. The first term gives us the even part and the second, the odd portion of the original function.

Note that both terms of this expression go through periodic variations as θ changes; the terms repeat every 2π radians. I have computed a few possibilities and plotted them in Fig.1, making parameter x take on a number of values. This periodically means Fourier's theorem applies[3], so that we can expand each of the terms in a Fourier series of harmonics such as the following,

$$\cos(x\sin\theta)=a_0x+a_1x\cos\theta+a_2x\cos2\theta+\ldots$$

and

$$\sin(x\sin\theta)=b_1x\sin\theta+b_2x\sin2\theta+\ldots$$

The next move determines the Fourier components in the usual way, therefore

$$a_0(x)=\frac{1}{2\pi}\int_0^{2\pi}\cos(x\sin\theta)\theta.$$

and

$$a_n(x)=\frac{1}{\pi}\int_0^{2\pi}\cos(x\sin\theta)\cos n\theta d\theta.$$

together with

$$b_n(x)=\frac{1}{\pi}\int_0^{2\pi}\sin(x\sin\theta)\sin n\theta d\theta.$$

The next step involves knowing the solution to a particular integration, still a standard elementary one, but not so common as some. It is obtained by means of a reduction formula[4] and the result it gives is,

$$a_0(x)=\frac{1}{2\pi}\int_0^{2\pi}[1-\frac{1}{2!}(x\sin\theta)^2+\frac{1}{4!}(x\sin\theta)^4-\ldots]d\theta$$

If you add these three equations, Bessel's integral re-emerges. This means that so far all I have done is to argue in a circle, via Fourier.

But now expand the integrand of the first integral as a power series for cosine[1],

$$\int_0^{2\pi}\sin^m x dx=\frac{1.3.5.\ldots(m-1)}{2.4.6.\ldots m}.2\pi$$

where m has to be an *even* integer. 2,4,6, etc. Use this result in the previous equation and you get,

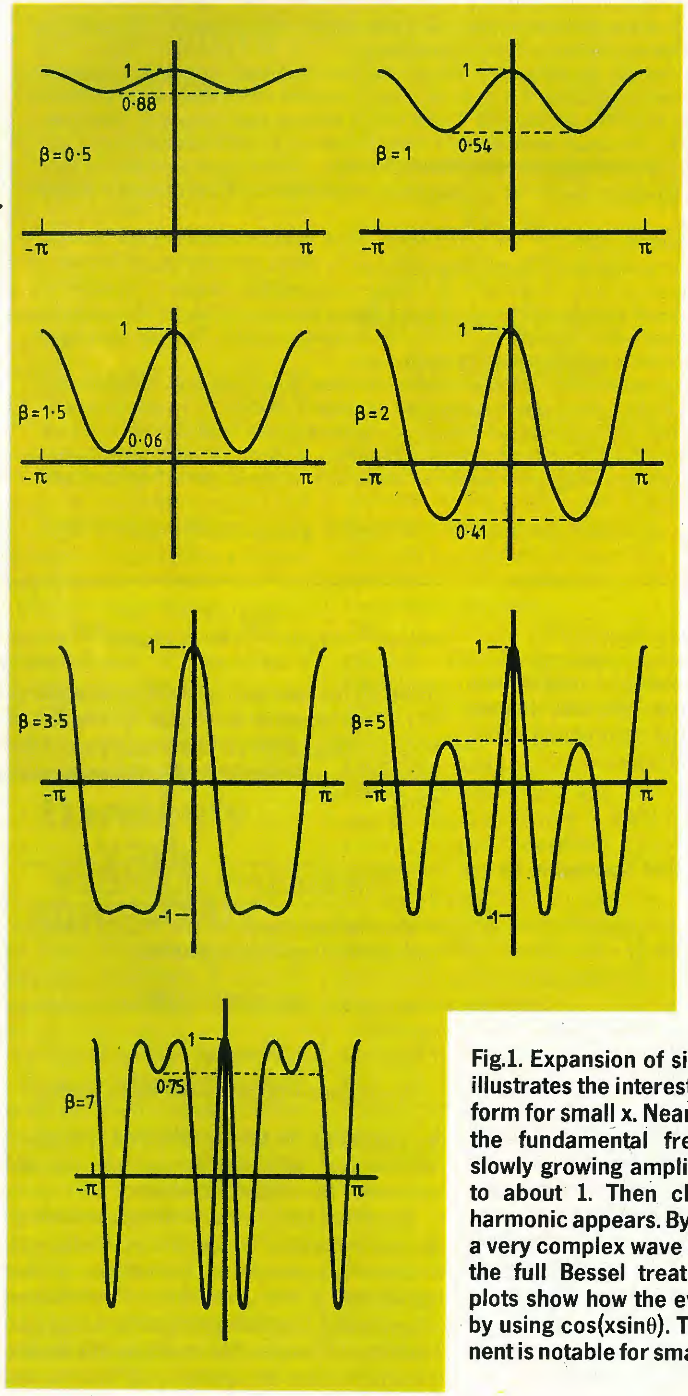
$$a_0(x)=1-\frac{1}{2_2}x^2+\frac{1}{2^24^2}x^4-\frac{1}{2^24^26^2}x^6+\ldots$$

Have a go at this on the back of an envelope – and if your envelope is big enough, do the next one to find a_n in a similar way. The result should be,

$$a_n(x)=2\left\{\frac{x^n}{2^nn!}\left[1-\frac{1}{2(2n+2)}x^2+\frac{1}{2.4(2n+2)(2n+4)}x^4-\ldots\right]\right\}$$

But only *even* n's apply, because when n is odd, $a_n(x)=0$. You can get a_0 directly from this result, so it is one of those zero-order terms we need not have found separately[3].

You need a similar treatment to handle the equation for b_n. Then we have all three results, but note first that the running harmonic integer n can only be 'odd' this time.



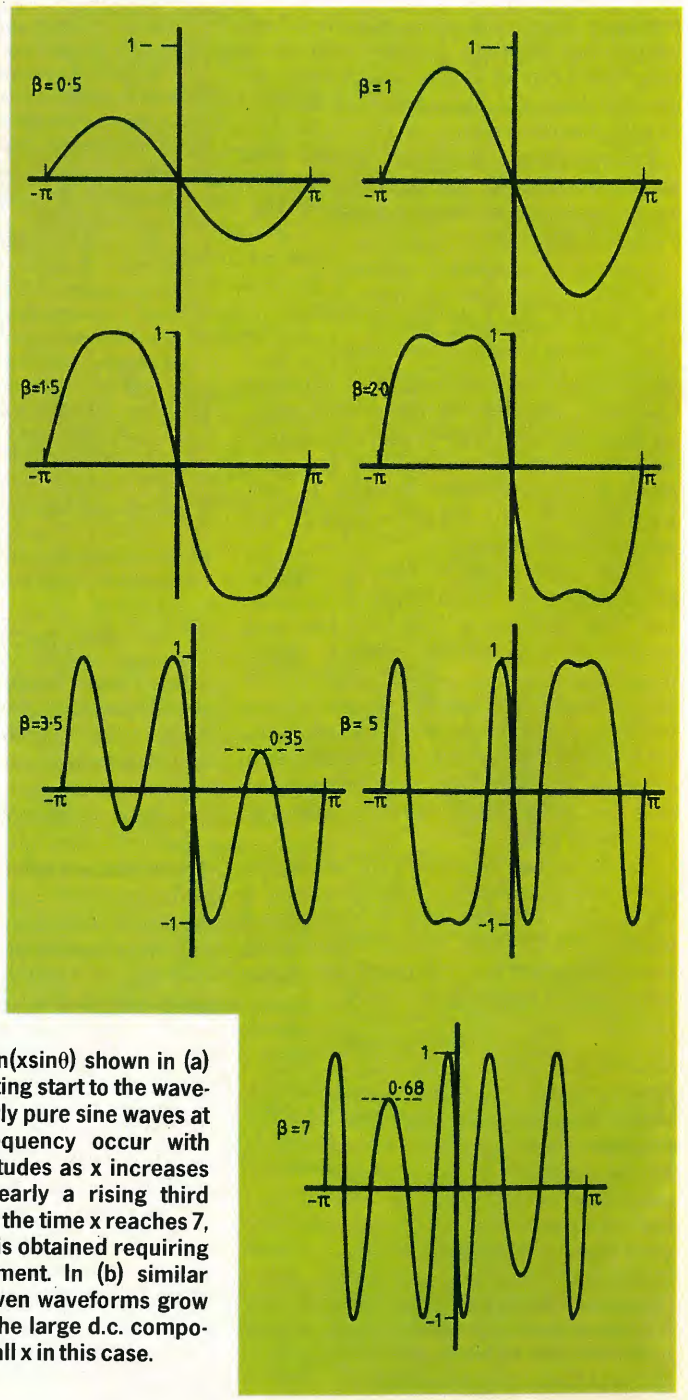


Fig.1. Expansion of sin(xsinθ) shown in (a) illustrates the interesting start to the waveform for small x. Nearly pure sine waves at the fundamental frequency occur with slowly growing amplitudes as x increases to about 1. Then clearly a rising third harmonic appears. By the time x reaches 7, a very complex wave is obtained requiring the full Bessel treatment. In (b) similar plots show how the even waveforms grow by using cos(xsinθ). The large d.c. component is notable for small x in this case.

IDENTIFY THE SERIES

Few students would say that these series look particularly simple. Yet arising as they do as solutions to Bessel's problem, earlier workers summed them and published tables, which we look up for solutions to particular problems. We label them $J_n(x)$, 'Bessel's functions of order n'.

If you differentiate these series functions and substitute the results into the differential equation,

$$\frac{d^2y}{dx^2}+\frac{1}{x}\cdot\frac{dy}{dx}+\left[1-\frac{n^2}{x^2}\right]y=0$$

you find it satisfied. So, not surprisingly we call this Bessel's equation of order n. In the kind of mathematical modelling I am discussing, both approaches usually apply. You can attempt to solve a problem by solving the differential equation, or alternatively look at the integral form.

Returning to the two series for a_n and b_n, half the Bessel functions come from the first series, where n is 2,4,6, etc., and the other half from the second series, where n goes through integers 1,3,5 and so on. For convenience the series for n=0 is kept separate to give $J_0(x)$, which is the zero-order Bessel function.

Summing up we have,

$$a_0(x)=J_0(x)=\frac{1}{2\pi}\int_0^{2\pi}\cos(x\sin\theta)d\theta$$

and

$$\frac{1}{2}a_n(x)=J_n(x)=\frac{1}{2\pi}\int_0^{2\pi}\cos(x\sin\theta)\cos n\theta d\theta$$

when n is even,

$$\frac{1}{2}b_n(x)=J_n(x)=\frac{1}{2\pi}\int_0^{2\pi}\sin(x\sin\theta)\sin n\theta d\theta$$

when n is odd. Finally, all together

$$J_n(x)=\frac{1}{2\pi}\int_0^{2\pi}\cos(n\theta-x\sin\theta)d\theta$$

for all n, which is the solution of the problem we started with, because we now know $J_n(x)$ as the series established above, and the actual values read from tables of numerical results published from summing them.

WHAT DO THE $J_n(x)$ LOOK LIKE?

Of course, there is a whole set of J's, an infinite number in fact as n steps through all the integers.* Once n is picked, J_n can be plotted as a function of x. For example, J_0 starts at one when x is zero, then oscillates in ever decreasing amplitudes as x gets bigger, as shown in Fig.2. You are quite right to notice that the plot looks like a damped cosine oscillation. But the intervals between the zero crossings show differing values, so the frequency is not constant. The decay does not follow the expotential law as a damped wave would do. Therefore the resemblance is only superficial.

Higher orders also oscillate and again show non-harmonic periodicity. Also the very high orders start off slowly, rise to a peak, then oscillate away with decreasing amplitudes, see Fig.3. You will find all manner of books about these properties, and a whole range of subtle results appear.

*There are Bessel functions for n fractional as well as other functions called, e.g., associated Bessel functions.

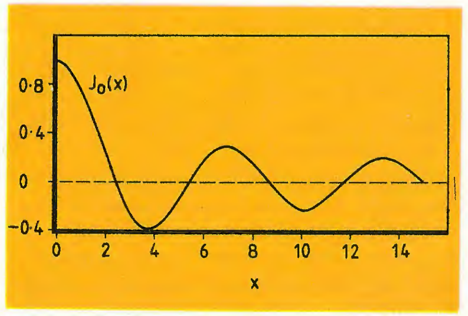


Fig.2. Plot of $J_0(x)$ shows an irregular damped oscillatory form. In theory, $J_0(x)$ yields carrier amplitude, which for some modulation indices disappears entirely.

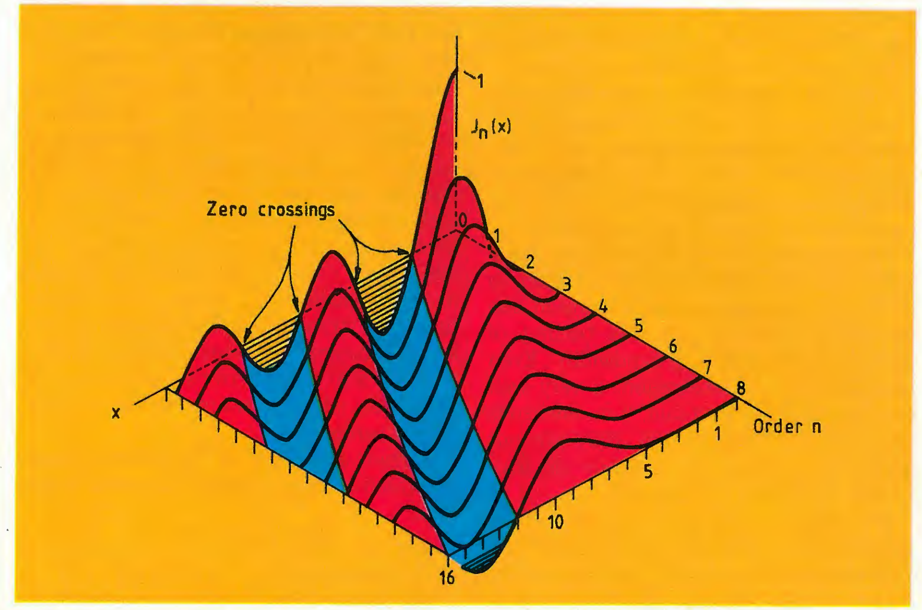


Fig.3. All orders of Bessel functions of the first kind oscillate, but high orders take a long time getting off the mark.

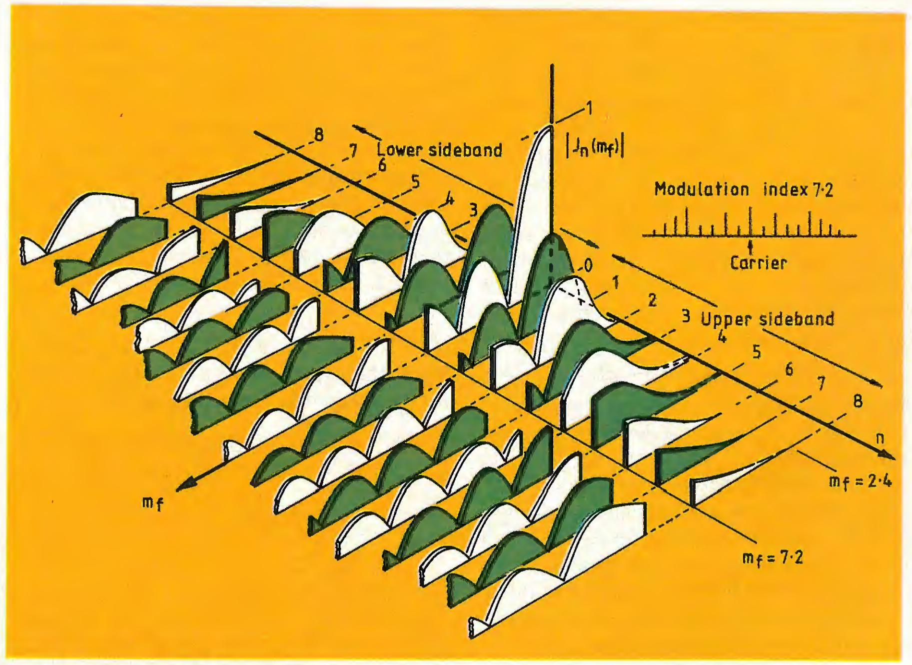


Fig.4. This double sided plot tries to illustrate how the sidebands proliferate in f.m. as the modulation index increases. By taking a slice across the plots at the appropriate index and looking into the "cut ends" (for example, shown here for m_f=7.2) you can visualize the magnitude of the single-tone modulation sideband spectrum.

GETTING THE SIGNALS THROUGH

One example in which these special functions arise in our work in a way beyond Bessel's wildest dreams, involves radio-signal transmission using f.m.

Despite being reasonably well understood for a long time, frequency modulation still causes a great deal of misconception and argument. Only recently I heard the following snippet of conversation among a group of radio technicians. "I tell you, a.m. has sidebands and requires a wide channel to fit them in, so noise is high, especially when you consider the detector is sensitive to amplitude spikes.

"Frequency modulation, in particular narrow band, can be designed to have only a slight deviation – 100Hz say – so it requires much less channel. As the carrier amplitude is constant, the a.m. sidebands aren't there, nor is there any sensitivity to noise spikes."

I inwardly smiled at this hoary fallacy. My thoughts went back to stories from early this century when eminent engineers and scientists were locked into the same old argument until John Carson showed that f.m. has *more* sidebands than a.m. and spreads further.

He also showed that its noise reducing properties arise because the channel is wider; the wider the better[5]. Shannon discussed at greater depth this trading of signal-to-noise-ratio with bandwidth[6]. Even after Carson's demonstration, a very well known British physicist said, "f.m. sidebands are a mathematical fiction, they are not really there." They are, but how do they arise?

Of course, we all see how a.m. arises, including the radio technician who held forth about it. We start with the carrier wave,

$$v(t)=\hat{V}_c(t)\cos\omega_c t.$$

The modulation alters the peak or envelope amplitude $\hat{V}_c(t)$ as a function of time. The channel position of the carrier, in other words its frequency, is f_c, where as usual, $\omega_c=2\pi f_c$.

In f.m. on the other hand, $\hat{V}_c$ remains constant, with the instantaneous value of ω_c now changing with the modulation as a function of t. You can also think of this alteration as swinging the phase, or instantaneous angle of the carrier. This means that there are two ways of modulating the angle. We can modulate it directly, giving phase modulation, or by modulating its rate of change, in other words the frequency, giving f.m. Therefore put,

$$\omega(t)=\omega_c+\Delta\omega\cos\omega_m t$$

so that ω_c, the carrier frequency, wobbles each side by a maximum deviation $\Delta\omega$, at a sinusoidal rate ω_m. The factor ω_m describes the modulating test frequency or tone.

We have to find instantaneous angle $\phi(t)$ from the previous equation for $\omega(t)$ to insert it into the carrier equation before it. An integration does this job. You often find an integrating circuit inside the f.m. transmitter, at least in Armstrong systems[7], so.

$$\phi(t)=\int\omega(t)dt=\omega_c t+\frac{\Delta\omega}{\omega_m}\sin\omega_m+\phi_0.$$

Term ϕ_0 is some constant phase chosen for convenience as zero.

We write $\Delta\omega/\omega_m$ as m_f, calling it the modulation index for f.m. You can see m_f means the ratio of the maximum deviation to the modulating frequency. The f.m. signal radiated becomes,

$$v(t)=\hat{V}_c\cos\phi(t)=\hat{V}_c\cos(\omega_c t+m_f\sin\omega_m t)$$

where $\hat{V}_c$ is the maximum carrier value.

Now compare this result with the integrand of the Bessel integral and notice it is the same thing, except for a plus sign. If you expand the cosine on the right hand side, you see that when m_f is very small, two miniscule sidebands at $\pm\omega_m$ occur each side of a carrier just as in a.m. You can see this mathematically by remembering that cos (small angle) approximates to one while sin (small angle) is approximately the small angle (if it is in radians). The first term gives the carrier – the second yields the sidebands (after expanding the "sin x sin", keep an eye on your trigonometry!) but if you increase m_f, a glance at Fig.4 shows that a much more complicated situation arises. All the even (cosine) components give rise to sidebands each side of the carrier at even harmonics of the modulating frequency, ω_m. Similarly the odd (sine) components give all the odd harmonic sidebands. Even the carrier amplitude does strange things; it sometimes disappears completely. (This is very paradoxical, as in "a.m." the carrier stays *constant* in amplitude, whereas in f.m. the carrier amplitude *varies.*)

Carrier and sideband amplitudes arise from all the orders of Bessel functions listed here,

$$\begin{aligned}v(t)=&\\ &\hat{V}_cJ_0(m_f)\cos\omega_c\\ &+\hat{V}_cJ_1(m_f)\cos(\omega_c+\omega_m)t-\hat{V}_cJ_1(m_f)\cos(\omega_c-\omega_m)t\\ &+\hat{V}_cJ_2(m_f)\cos(\omega_c+2\omega_m)t+\hat{V}_cJ_2(m_f)\cos(\omega_c-2\omega_m)t\\ &+\hat{V}_cJ_3(m_f)\cos(\omega_c+3\omega_m)t-\hat{V}_cJ_3(m_f)\cos(\omega_c-3\omega_m)t\\ &+\hat{V}_cJ_4(m_f)\cos(\omega_c+4\omega_m)t+\hat{V}_cJ_4(m_f)\cos(\omega_c-4\omega_m)t\\ &+\ldots\end{aligned}$$

The results show that the theoretical width of an f.m. signal is infinite! Fortunately, the higher order Bessel coefficients rise very slowly as I mentioned above, so that the amplitudes of the higher harmonics beyond a certain point drop off very quickly and the effective width of a signal remains finite. A few examples of f.m. spectra appear in Fig.5. A good working rule for the bandwidth required in an f.m. channel remains the empirical expression quoted by Carson,

$$B_{fm}=2f_m(1+m_f)$$

where f_m is the maximum frequency component in the modulation spectrum and m_f is the modulation index as before.

So once again, the work of an early mathematician still continues to have up to the minute consequences in our field, beyond those wildest dreams to which I referred. Remarkable really, when you stop to think how mathematics keeps on modelling so well, what seem to be disparate natural phenomena...

1. Joules Watt, *Electronics and Wireless World,* p.938, Sep. 1987.
2. J.B. Fourier, Analytical theory of heat, English translation, Freeman.
3. Joules Watt, A series of remarks on – Fourier, *Electronics and Wireless World,* p.1000, Oct. 1987.
4. The result of the reduction formula is sometimes known as Wallis's formula, a discussion of which can be found in G. Stephenson's Mathematical methods of students, chapter 4, p.49 (Longmans).
5. J.R. Carson, Notes on the theory of modulation, *Proc. IRE* 10, p.57, Feb 1922.
6. C.E. Shannon, A Mathematical theory of communication, *BSTJ* 27, Nos. 3&4, 1948.
7. E.H. Armstrong, *Proc. IRE*, May 1936.

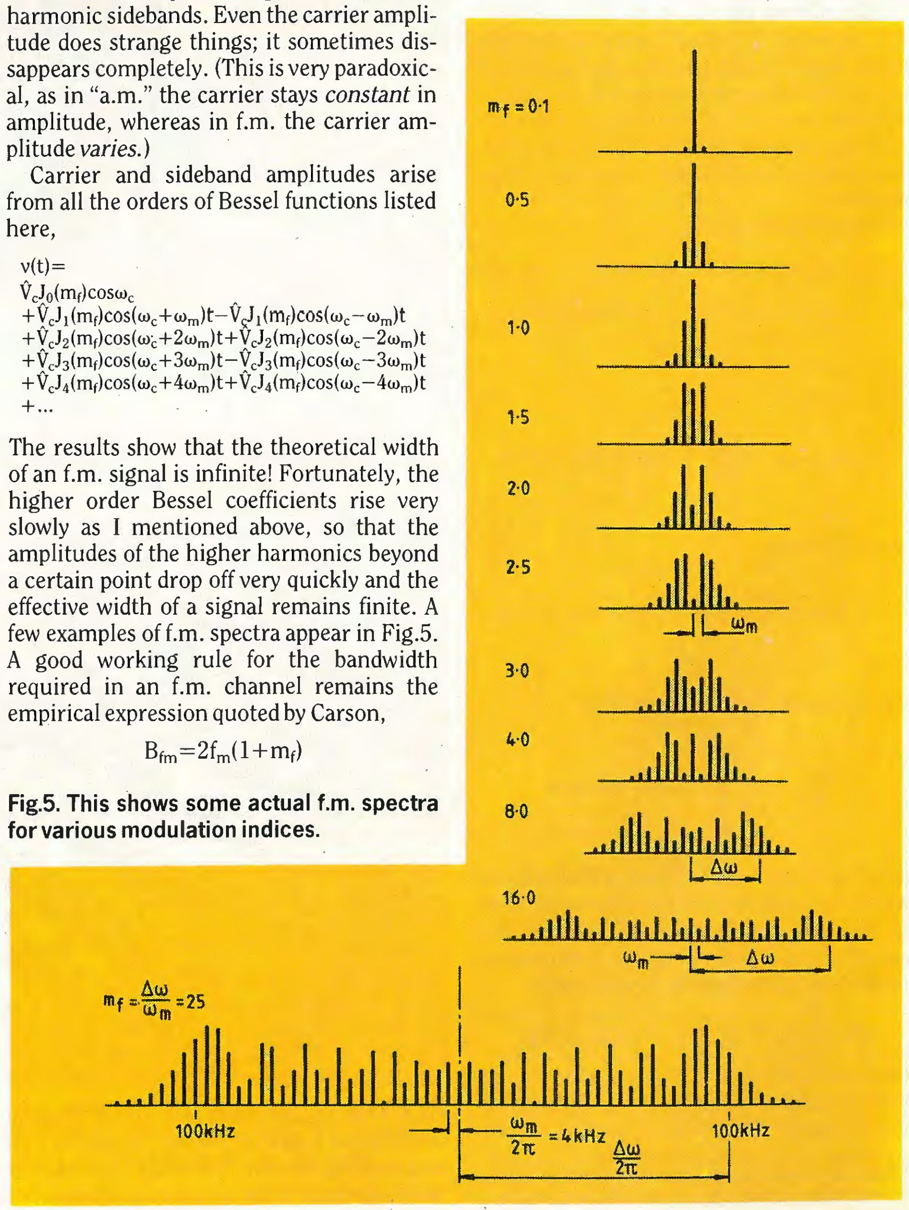


Fig.5. This shows some actual f.m. spectra for various modulation indices.

Multiprocessing with VMEbus

How VMEbus allows 32 bit processors and higher d-ram integration to be used in very sophisticated and powerful systems.

BY STEVE HEATH

From its conception, the VMEbus was designed to support multiprocessor system architectures. However, the techniques used have evolved to exploit the advances in package and silicon technology to complement the powerful architectures within VMEbus.

MULTIPROCESSOR REQUIREMENTS

Multiprocessor system architectures need certain resources to be present to provide the mechanisms for basic multiprocessing. For example, it is essential that bus access is controlled to prevent multiple bus accesses causing system failure. However, the key to any successful design is the ability to send and receive messages between processor nodes without corruption, and to be able to prioritise such resource to provide the system response required.

The usual technique for message passing of large or low to medium priority messages is to use shared memory as a mailbox. The problem with this is that certain hardware mechanisms are required to make sure that this information is not corrupted or that simultaneous access is not attempted resulting in a bus lock-up and system crash.

To prevent such a catastrophe, access to the shared memory must be controlled such that only one processor node has the right of access. This control has both software and hardware components. Software control is normally achieved by the use of a semaphore. This technique requires a processor to test and set a memory bit to confirm that no other processor is accessing the shared memory. If the bit is set, this indicates that access is not available. If it is clear, access is allowed and the processor immediately sets the bit to lock out other processors. With a multiprocessor architecture, however, it is possible that between the test and setting cycles, another processor could access the semaphore, find it is clear and erroneously think that it has access. Both processors now access the shared memory resulting in its corruption and ultimate collapse of the system. Therefore a mandatory requirement is a secure semaphore system.

This article is based on a paper presented at BUSCON/UK, October 1987, the proceedings for which are available from 17100 Norwalk Blvd, Suite 116, Cerritos, CA90701-2750, USA.

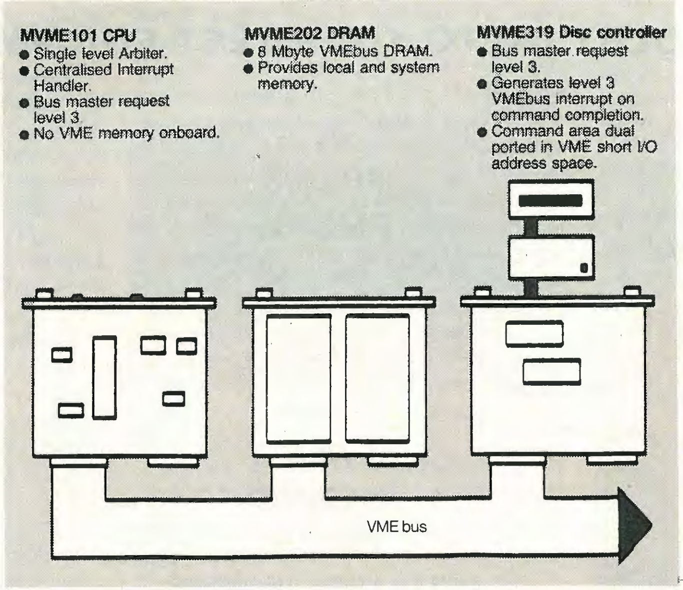


Fig.1. This example of simple VMEbus architecture is in fact a multiprocessor system.

For high priority messages, the normal solution is to generate an interrupt which allows the service routine to receive or send a message. Care has to be taken here to provide mechanisms to provide sufficient different interrupt identities. Failure to do so results in software overheads within the service routine in identifying what task the routine has to perform to get the message.

VMEbus was conceived and designed to support multiprocessing techniques. It provides the basic fundamentals to build the framework for various complexities of architectures previously limited by available hardware technology. As this technology has improved, the trend has been to supplant software solutions with hardware implementations.

With the continued development of hardware support for multiprocessing, currently embodied in the MVME135/6 family, VMEbus multiprocessing designs may be said to have come of age heralding a new era for the system designer.

Consideration must also be given to which processor node responds to a particular interrupt to prevent an unwanted multiple response or bus access.

Both the 68000 processor family and VMEbus have been designed to provide these fundamental concepts.

FUNDAMENTAL FACILITIES

The 68000 microprocessor family test-and-set instruction performs a bit test and set operation as a single indivisable bus cycle. This read-modify-write cycle is supported on VMEbus and provides a secure semaphore for multiprocessor applications.

Simultaneous bus access is prevented by the four-level bus arbitration scheme. Prior to a master using the VMEbus, it must first request it by asserting one of the four bus request lines ($\overline{BR0}$ to $\overline{BR3}$). The master must then wait for the system bus arbiter to acknowledge his request by asserting the bus grant signal for that level. These signals are daisy-chained down the backplane using the $\overline{BGIN}$ and $\overline{BGOUT}$ signals. This means, that in addition to the overall bus arbitration scheme, there is an hierachy based on slot position.

VMEbus provides a mechanism where interrupt handling can either be centralised on one master card or distributed throughout the system. An interrupt is started by asserting one of the seven interrupt request lines ($\overline{IRQ1}$ to $\overline{IRQ7}$).

The appropriate processor card's interrupt handler will then respond by requesting the bus, and once received, starts the acknowledge cycle.

This asserts $\overline{IACKIN}$ and places the interrupt level as a three bit code on the address bus. This tells the system which level is being acknowledged. The interrupter recognises this and places a vector number (1 from 256) on the bus for the handler to use. Distributed interrupt handling is achieved by having multiple handlers which respond to different interrupt levels. The $\overline{IACKIN}$ daisy-chain provides slot priority within a level.

SIMPLE SYSTEM

Often the most simple VME system is actually a multiprocessor system. Consider the Motorola SYS319 system (Fig.1). It comprises of a MVME101 68000-based processor card, some dynamic memory and a MVME319 disc controller. Although this is a single processor system, the disc controller is intelligent and is capable of accessing the bus as a master and generating interrupts. Communication between these two cards demonstrates the fundamentals of multiprocessing.

The disc controller is controlled by writing command packets into an dual-ported memory area and setting a semaphore bit in a status byte to start the controller. The controller accesses the packet, and performs the required function. Within the packet is a pointer to the buffer area in global VME memory into which the controller will dma the data sectors from the required disc. This operation requires a successful bus arbitration just as any processor would require. After completion of the command, the disc controller writes a completion message with a command identity and can then either generate an interrupt to the MVME101 processor card or set another semaphore bit and wait for it to be polled.

There are restrictions to what multiprocessing will achieve within such a simple system. In this example, VMEbus has replaced the normal microprocessor bus as the mechanism for accessing local memory so that all this additional overhead is placed on the bus. In addition, the single level arbitration scheme means that only slot position determines the hierachy. Therefore, the disc controller can only access the bus when the MVME101 is not using it, which, due to heavy local traffic, is not often. Consequently disc performance suffers so impacting operating system performance and ultimately that of the system as a whole.

Using VMEbus simply as a replacement for the local processor bus does allow the use of VME boards as modular units. However, this role dissents from the original design concept of VMEbus as a message passing medium and prevents the full utilisation of its multiprocessing facilities.

THE SECOND GENERATION

To reduce the problems encountered with the first generation process boards such as the MVME101, several new concepts were used. Firstly, the advances in d-ram packing density and programmable array logic devices allowed large amounts of dual-ported dram to reside on board. This removed local bus traffic from the VMEbus as well as reducing the overall board count. Often system controller functions and bus arbitration were removed from the processor card to a separate controller which could also provide a global VMEbus interrupter in addition to other functions such as real time clocks, global memory and i/o functions.

The large amounts of memory, typically 512 Kbytes, were ample for most applications. However with the advent of memory hungry software such as Unix, this proved to be insufficient. Local memory expansion again had to go on the VMEbus so recreating the previous limitations. As disc access speed is also key to these type of applications, the disc controller must have high priority access to the VMEbus and to provide this requires a trade off against processor access and performance.

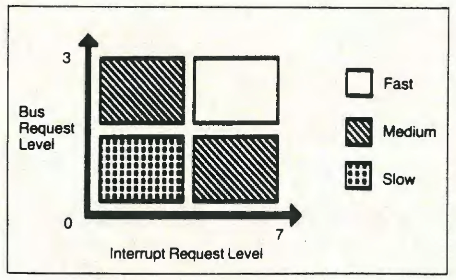


Fig.2. VMEbus interrupt response times for a priority arbitration scheme

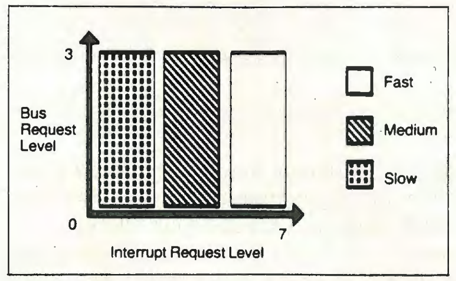


Fig.3. VMEbus interrupt response times for round robin arbitration scheme

This trade off was solved on the MVME121 processor board series by implementing a cache, a technique used on mini and mainframe computers.

The MVME121 has a 4Kbyte wait state free cache memory on board in addition to its 512 Kbyte dual ported dynamic memory. The cache hardware is transparent to the user and provides wait state free access to either data or instructions contained in it. If the information is not available from the cache, then the resulting miss starts a normal VMEbus cycle. The cache content is automatically updated from such VMEbus accesses to preserve its coherence. Typically a 4Kbyte cache gives a "hit" rate of about 80%, depending on software.

Table 1. Performance figures of an MVME121 processor board with cache

System configuration	Time to execute 1 million single precision floating point multiples
A. MVME/121in a VME-10 Workstation, running code in VME-10 RAM. MVME121 cache disabled.	136 seconds
B. As for system A, but MVME121 cache enabled	42 seconds
C. MVME121 running code in on-board RAM, cache disabled.	55 seconds
D. As for system C, but MVME cache enabled.	42 seconds

1. Benchmark code written in 68000 assembler.
2. The MVME121 uses a 68010mpu with a 68451 mmu running at 10 MHz

The cache advantage is that it can supply data or instructions to the onboard 68010 processor without actually accessing the bus or incurring wait states. This means that delays in requesting the bus etc can be dramatically reduced, resulting in improved performance and provides increased bus bandwidth for use in multiprocessor systems.

An example of the improvements that can be achieved is given in Table 1. The slow performance times for system A are caused by the VMEbus memory within the VME-10 workstation acting as local memory for the disc controller, graphics controller and processor, as well as being accessed by the MVME121. This is an example of the use of VMEbus as a replacement microprocessor bus leading to consequent system degradation.

Now that local bus traffic has been reduced or removed, true multiprocessing systems can be implemented. Consideration must now to be given to other aspects of the architecture.

WHO HAS THE BUS?

Decisions must now be made on how bus ownership is determined. Two schemes are frequently used. The first establishes a hierachy where priority levels are determined by the request levels and the slot position (priority arbitration) and the second grants bus ownership by rota so that each level receives it in turn (round robin).

What is often overlooked is that the bus arbitration scheme will affect the VMEbus interrupt latency. This is because the bus is required by the interrupt handler prior to acknowledging the interrupt. Therefore to achieve the best response time an interrupter must generate a high priority interrupt and the handler must have a high bus aribitration priority. Simply generating a high priority interrupt is insufficient if the handler has to wait for the bus before acknowledging it.

For systems that require fast interrupt response, priority arbitration is usually implemented with the critical interrupts being generated at level 7 and being handled by a handler with a level 3 bus request priority. The effect of arbitration and interrupt levels on interrupt response of such a system is shown in Fig.2. It is necessary to choose the right combination to achieve the required response.

Where a round robin arbitration scheme is used, each bus request level waits for its turn to obtain the bus and so the response time becomes dependent on the interrupt level alone. This is shown in Fig.3.

VMEbus allows individual interrupt handlers to be assigned to one or more of the seven interrupt levels for acknowledgement and servicing. Such a distributed interrupt handling system (Fig.4) has distinct advantages for a multiprocessor system over its centralized counterpart (Fig.5), which provides just a single handler for all interrupt levels. Distributed interrupt handling

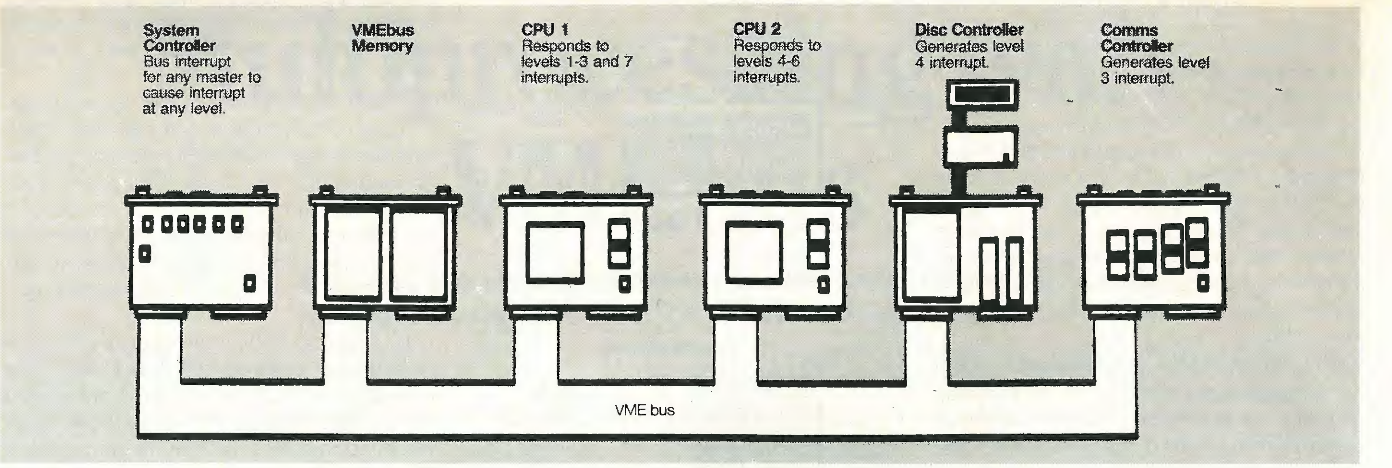


Fig.4. Distributed interrupt handling VMEbus system has distinct advantages over its centralized counterpart shown in Fig.5.

provides mechanisms for high speed message passing and processor synchronisation.

With every processor assigned its own interrupt, processors can pass high speed messages by generating a specific VMEbus interrupt for the receiving processor. Within a centralized system this is not possible so message passing has to rely on software techniques such as semaphore polling to ensure its arrival. Such techniques increase processor overhead and are often slow in operation.

Synchronization of a multiprocessor system is usually performed by a single controlling processor, referred to as a master. It synchronizes the other slave processors in a distributed interrupt handling design by generating an interrupt for each slave which brings the processor out of its waiting state (usually a software loop). Within a central interrupt handler, this initialization can only be performed through the constant inspection of global semaphores by the slave processors while in their waiting loops, a method that can be very wasteful of VMEbus bandwidth. This semaphore method is also applicable to distributed architectures if the number of processors exceeds seven, where it is impossible to assign a unique interrupt level to every processor.

The next evolution had similar aims so that previously described: reduction or removal of local bus traffic from VMEbus. The advent of 32 bit microprocessors such as the 68020, doubled the normal 16 bit data width and, coupled with faster clock speeds and shorter memory cycles, gave dramatic improvements in processing speed. Table 2 shows typical performance figures.

It is interesting to note that the cache technique, used on the MVME121 to reduce bus loading and the dampening effect on processor throughput of memory wait states, has been implemented on chip with the 68020 and its successor the 68030. Bus bandwidth used by a 68000 is about 85-90% compared to about 65% for a 68020 with its cache.

Software also evolved: the extra throughput and large memory addressing capability meant that high memory intensive packages were being developed where even several megabytes of local ram would be insufficient. The obvious solution is to define and use a local memory extension bus.

Table 2 Performance of 68020 vs 68000

Hardware environment	Time to execute 1 million floating point multiples.
8 MHz 68000 running code in VMEbus memory.	85 s
12.5 MHz 68020 with VMX32 memory, no on-chip cache.	24 s
12.5 MHz 68020 with VMX32 memory, on-chip cache enabled.	19 s

Code written in 68000 assembler.

VME SUBSYSTEM BUS

The VME subsystem bus (VSB) was developed from Motorola's VMX32 expansion bus used on the first generation 68020 based VME processor cards, the MVME130 family. Through its fast 32 bit data and address paths, with dynamic bus sizing and cache control, it provided a local path over which processor, memory and peripheral modules could communicate. It evolved into VSB by the addition of a simple bus arbitration and interrupt scheme.

VSB is implemented via the user-defined i/o pins on the P2 connector. It provides an elegant mechanism for removing local memory traffic from VMEbus, and for increasing local available resource such as memory. This is an important feature because implementing a VSB interface, in particular bus drivers, consumes a large amount of board real estate. Local resource has to be reduced to provide space for the 15 or so discrete logic packs.

Due to these trade-offs, the decision to implement such a bus can be difficult to take. The effect that VSB has on overall system performance is often quite dramatic. If the VMX32/VSB bus was disabled on a MVME131 processor within a SYS1131 running Unix, an immediate performance reduction of about 20% occurs. From the system architecture in Fig.6, the reason is apparent. The MVME131 has very little local memory and uses its VMX32/VSB bus to extend that resource. Disabling the extension bus puts the entire processor load onto VMEbus resulting in system degradation. Fortunately the degradation is reduced due to the action of the 68020's on-chip instruction cache.

SEMICONDUCTOR TECHNOLOGY

Fortunately semiconductor technology has not stood still: the advent of 256 Kbit and 1 Mbit dynamic memories in zip and sil high density packages have increased local memory and reduced space requirements. In addition, improvements in gate array technology have allowed bus interface circuits to be designed and used. The MVSB2400, developed by Motorola, is an example of this. It is a low powered bipolar lsi gate array which contains all the VSB address/data multiplexing circuitry, a VSB requester and arbiter with associated timeout module, status and control registers and the capability to provide 48 mA drive to the VSB lines directly within a single 14 by 14 pin grid array package.

As a result, the hardware designer no longer has to compromise. He can offer 32 bit processors with large amounts of memory (1 to 4Mbytes), local bus expansion via VSB and have board space available to offer hardware facilities specifically for multiprocessing systems.

The next obvious evolution is to provide hardware solutions for requirements such as processor synchronization and global interrupts. While they can be implemented using software techniques, further, unwelcome, burdens are placed on the software design. Hardware solutions can provide very elegant solutions to the type of problems described earlier without placing any artificial limitation on the overall design.

The MVME135/136 processor family demonstrates what can be achieved.

STATE OF THE ART MVME135/136

What makes the MVME135/136 processor family so interesting is not its 32 bit processor, its 4Mbyte local memory or its VSB and VME bus interfaces, but its multiprocessor support. By using the MVSB2400 gate array and surface mount memory, sufficient board space has been freed to provide hardware support for global access and control of several processor functions, virtual interrupts to selected processors, simultaneous interrupts to multiple processors and message broadcasting to a group of processors. This is achieved by a set of registers accessable from VMEbus called the multiprocessor control and status register. Its organisation is shown in Table 3.

Processor status information is given by a status register which can be checked via VMEbus either during confidence tests or initializing local resource. BSY indicates the board is not ready to operate at system level, SCON indicates that the board has been configured as a system controller, FAIL indicates a local processor failure and WDT shows that a local watchdog timeout has occurred. Checking of these bits throughout the system during initialisation could identify a serious problem and allow a recovery plan to be executed. Without these facilities, similar schemes have to be implemented in software with an inevitable increase in overhead.

The third register has a bit ISF which can be set locally or by other bus masters to prevent the processor from asserting sysfail on the VMEbus as a result of a local failure and so locking the bus. The LKTR bit however can do the opposite and when asserted maintains bus mastership for its processor until cleared. This allows whole software routines to be treated in a similar way to the TAS instruction and become indivisible bus operations.

The remaining bits KING, LM1, LM2 and LM0 are location monitors. The VMEbus is monitored and when their address appears the bits are set or cleared on all boards within the group simultaneously. This broadcast can cause various results: setting LM0 results in a local interrupt being generated on the board, LM1 and LM2 simply record the current status and the KING bit is used during initialization to determine which processor is the master or system initializer.

The ability to use LM0 to generate a local interrupt provides a mechanism to efficiently poll a semaphore. The processor that is using the resource clears LM0. The other processors, on finding LM0 clear, perform other tasks and wait until the first processor is finished and sets LM0. This immediately indicates to the others, via the generated interrupt, that the resource is available. One of the processors will then poll successfully and the cycle repeats. This means that the waiting processors, instead of wasting their time polling, can use that time usefully. Again this demonstrates the constant theme of using hardware to reduce software overhead and maximize system throughput.

Fault tolerant designers now have a simple mechanism to software reset a processor card without having to generate a system reset via VMEbus. The R&H and H&H bits allow other processors to control the local c.p.u. directly. When R&H is set, the local c.p.u. will reset and hold until a system reset or the bit is cleared, thus allowing individual processors to be reset under software control. By using the H&H bit, the local processor can be halted to allow code downloading into local dram. Other applications include synchronizing processors where a processor initializes itself, sets up its reset vector to point to its code, and then resets and holds using R&H. The system initializer (determined using the KING bit) can then start the processor at will by clearing R&H. This is far more effective than using a software mechanism such as polling semaphore or generating multiple interrupts.

RONR changes the processor's bus requesting algorithm to that of request-on-no-request. The procesor will only request the bus if no other requests are pending thus allowing access to processors further down the daisy-chain. This provides a more "democratic" arbitration scheme which can be activated under software control when required and means arbitration schemes are no longer dependent on slot position.

Writing to the SIGHP or SIGLP bits generates either a high or low priority local interrupt to the onboard processors. This allows high speed message passing as described in section 2 to be performed without generating a VMEbus interrupt with its subsequent time overheads in acknowledging the interrupt.

Steve Heath, who is UK field applications manager for Motorola, develops this theme for single board computers on page 1083.

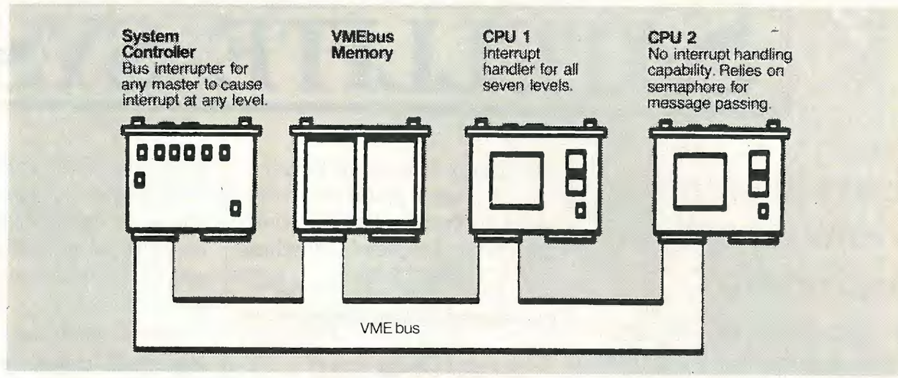


Fig.5. Centralized interrupt handling VMEbus system has only a single handler.

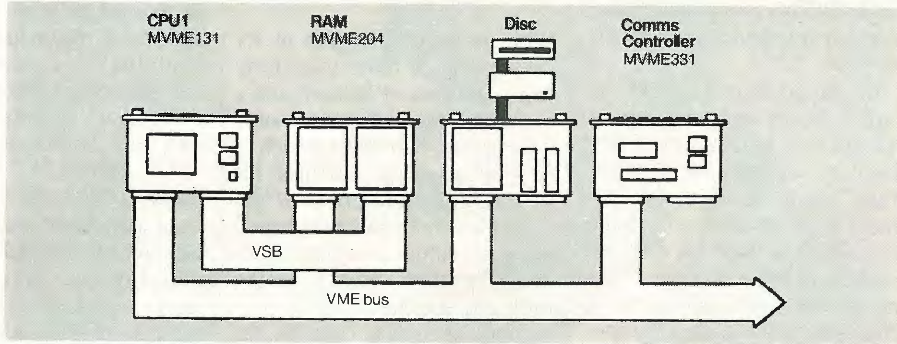


Fig.6. In the SYS1131 VME system all the local access is via the VSB subsystem bus, and all the global access, message handling and interrupts is via the VME bus.

Table 3 Organization of multi-processor control and status registers for MVME135

Address Offset	D7	D6	D5	D4	D3	D2	D1	D0
1 ID BYTE								
3	BSY	SCON	FAIL	WDT		Undefined		
5	KING	LM2	LM1	LM0	ISF	LKTR	Undefined	
7	R&H		Undefined		RONR		Undefined	
9	H&H				Undefined			
B	SIGLP				Undefined			
D	SIGHP				Undefined			
F					Undefined			
11	MP0				Undefined			
13	MP1				Undefined			
15	MP2				Undefined			
17	MP3				Undefined			
19					MP COMM BYTE			
1B					Undefined			
1D					Undefined			
1F					Undefined			

SATELLITE SYSTEMS

European ultra-violet astronomy

A satellite carrying an ultra-violet observatory is being considered by the European Space Agency, which has just commissioned British Aerospace to do a one-year feasibility study on the proposal.

The observatory would be an Earth orbiting spacecraft equipped with a grazing incidence telescope serving a set of ultra-violet spectrographs. Its aim would be to explore u.v. radiation which cannot be detected from Earth because of the filtering effect of the atmosphere. Operating in the largely unexplored lower u.v. regions (wavelengths 10 – 200 nm), the mission would provide information on the chemical composition and physical characteristics of stars, galaxies and other celestial objects.

The project has been named 'Lyman', after Theodore Lyman, a professor of Harvard University, USA, who pioneered investigations into the far ultra-violet spectrum. Proposed launching date is the mid 1990s.

Canada's big domsats

With its huge land mass of 3.7 million square miles (over forty times the area of Britain) and a coast-to-coast distance of some 3,000 miles, Canada has much to gain from using satellites for internal communications. It was in fact the first country to have a domestic communications satellite in geostationary orbit – the Anik A-1, launched in 1972.

Since then the country has had a further eight geostationary domsats in operation. All have borne the name Anik, the Eskimo word for 'brother', with series identification letters ranging from A to D. At present there are five Aniks in use (Cs and Ds), four of which were launched by the US space shuttle and one by a Delta rocket. This domestic satcom service is run by Telesat Canada, a corporation set up for the purpose in 1969 and jointly owned by government and industry.

Now Telsat has announced that it will be launching its tenth and eleventh domsats in 1990, namely Anik E1 and E2. These, it is claimed, will be the "largest and most powerful spacecraft built and launched to date" for domestic communications. They will operate in both and C band (6/4 GHz) and the Ku band (14/12 GHz), using 24 C-band and 16 Ku-band transponders.

As such, the domsats will provide telephone and data communications, plus broadcast radio and television distribution signals, for Telesat's customers throughout Canada and between Canada and the USA. For television distribution, each C-band transponder will carry one 27-MHz bandwidth signal, while each Ku-band transponder will provide two such channels, making a total capacity for each satellite of 56 tv signals.

The new Aniks, to be constructed by the Canadian firm Spar Aerospace Ltd as prime contractor, will measure 23.7m × 8.5m when their solar panels are extended and will weigh 2500kg on the ground. Each C-band transponder will have a solid-state transmitter output amplifier giving an r.f. power of 11 watts. The Ku-band transponders, however, will use t.w.t. output amplifiers, each providing 50W of r.f. power. To supply these transponders, the solar panels in each satellite will generate about 4 kW.

When completed in 1989, the satellites will be sent to Kourou, French Guiana (S. America), where they will be separately launched in the spring and autumn of 1990 by the latest and most powerful Ariane-4 rockets (Ariane type 44P). Anik E1 will come into service in 1990, while E2 will be held in storage orbit till 1992. both are expected to have an operational life of ten years.

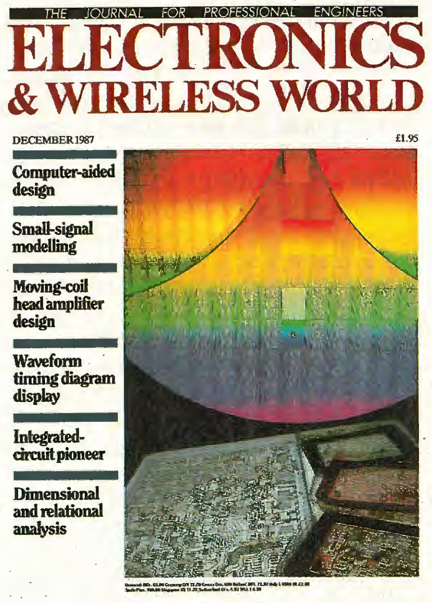
Satellite Systems is compiled by Tom Ivall

NEXT MONTH

Computer-aided design. From simple drawing packages through to simulation, testing and verification of circuit design, cad applications are increasing in variety and complexity. Our December feature describes some of the available systems and techniques.

Noise in electronic systems – an overview. Noise in an electronic system sets an absolute limit to the performance of the system, be it in communication or measurement. With the benefit of 50 years experience, Professor D A Bell presents an overview of the subject in which he discusses thermal, shot, avalanche and 1/f noise.

Head amplifiers for moving-coil cartridges. Doug Self surveys the problems involved in the design of m.c. head amplifiers and describes a new approach, which results in exceptional linearity, high headroom and a noise performance that is within 6dB of the theoretical minimum.



Equivalent circuits. Joules Watt explains the convenience of using equivalent circuits – the kind with shorted supply lines! Single-stage, small-signal analysis is needed, even though the stage under consideration is inside an integrated circuit.

Pioneers – J. S. Kilby. In 1959, Kilby joined Bardeen, Shockley and Brattain in the company of those who have changed the face of modern living by his development of the integrated circuit, "wherein all components of the electronic circuit are completely integrated into the body of semiconductor material".

Relational analysis. In contrast to the method of dimensional analysis, this method of system analysis, described by J A Corbyn, depends on the mathematical laws or relationships which determine system behaviour.

Pioneers

11. Edwin Howard Armstrong (1890-1954): genius of radio

W.A. ATHERTON

Institution of Electrical Engineers.

"Seldom can an inventor look philosophically upon the bane of his existence, patent litigation, and find much good therein" – Armstrong, 1942.

No doubt there are some around, but I have never met an undergraduate who has made a major invention. Yet E.H. Armstrong did just that whilst a student at Columbia University in New York. He went on to make at least two other great electronic inventions. They brought him fame, fortune – and patent misery.

Edwin Howard Armstrong was born in New York City on December 18, 1890, the son of John and Emily Armstrong. His father ran the American branch of the Oxford University Press and when his son was about 14 years old he gave him a copy of The Boy's Book of Inventions. It was then, it is said, that the boy announced his intention of becoming an inventor.

Whatever the truth of that, Armstrong's attention had certainly been gripped by Marconi's adventures with radiotelegraphy. The attic of the family home in Yonkers became littered with electrical components as Armstrong began to teach himself about radio.

At Columbia University, an establishment with which he was to have a long connection, he was fortunate to study under Professor Michael Pupin, who had patented the loading coil used in long-distance telegraphy and telephony.

Armstrong graduated in 1913 and became an assistant teacher at Columbia, so continuing his association with Pupin. By then he had already made the first of his great inventions: the regenerative or feedback circuit.

POSITIVE FEEDBACK

The first electronic valve was the vacuum diode. It was invented in 1904 in England by J.A. Fleming and was used as a radio-wave detector. A couple of years later in America Lee de Forest added a third electrode (the grid) to make the triode, or, as he called it, the audion. Of course the triode became immensely important, but in its early years it was just another radio-wave detector and not even the best. In a legal wrangle in 1912 it was described as worthless.

In 1912-13 Armstrong studied the uses of the triode. He discovered that if part of the anode output was fed back to reinforce (regenerate) the input at the grid then the whole circuit became a very good amplifier as well as a detector.

If even more current was fed back then the circuit oscillated and could be used for generating a sinewave carrier for radio or telephony. Its inventor was soon known as "Feedback Armstrong".

This discovery was one of the birth pangs of electronics and its patent rights were of immense value.

Unfortunately for Armstrong, others had made the same discovery – in particular Lee de Forest, who had just sold telephone repeater rights to the triode amplifier for $50,000. Later he sold the radio receiver rights for $90,000. Further claimants to the invention of the regenerative circuit were Irving Langmuir of General Electric in the USA and Alexander Meissner in Germany.

Armstrong was to discover that making and keeping inventions is a far more complex business than was portrayed in The Boy's Book of Inventions.

Aged only 22, he was slow to patent his invention and he soon found himself in a legal battle with de Forest which was to last 20 years and to cost a fortune. One commentator bewailed the money spent on lawyers which could have been better invested in electronics.

The American Institute of Radio Engineers (IRE) awarded him its Medal of Honor in 1917. When the Supreme Court eventually found in favour of de Forest in 1934, Armstrong offered to return the medal. But the IRE reaffirmed the award: in its members' eyes Armstrong was the true inventor, whatever the courts said.

Shortly before his death Armstrong gave $50,000 to Columbia University for a research project on the success and failure of law courts in deciding complex technical matters. Patent disputes were the bane of his life.

THE SUPERHET

When America entered the First World War, Armstrong became an Army Signals Corps officer and was sent to France. There he pondered the gunnery problem of how to locate enemy aircraft. The solution seemed to lie in detecting the high-frequency radiation emitted by the aircraft's ignition system. But how could such high frequencies be amplified?

The heterodyne (or mixing) principle was well established, having been invented by R.A. Fessenden in 1905. Armstrong decided to heterodyne the received signal twice, first to an inaudible intermediate frequency which could be amplified, then to a lower audible frequency. He called the circuit the superheterodyne, now more usually abbreviated to superhet. Though it was not in fact used to locate aircraft, it improved the stability and sen.-.ivity of radio receivers and enabled them to be tuned to a wide range of frequencies. It became the continuing basis of most radio reception.

Armstrong patented the superhet in 1920. It was indisputably his own invention, and this time there were no patent challenges. He sold the patents for the superhet, and for his regenerative and other circuits, to Westinghouse in 1920 for over $335,000. Some of that money was needed to pay debts to lawyers. Looking back on the deal one has to say that Westinghouse got a bargain, even though Armstrong retained the royalties earned from amateur use.

SUPER-REGENERATION

The following year he applied for a patent on his next invention – super-regeneration. This was a method of defeating the main problem of the regenerative circuit which was its tendency to burst into unwanted oscillation. This time the patent was snapped up by the Radio Corporation of America (RCA), whose general manager was still smarting from the previous Westinghouse coup on the superhet. The deal gave Armstrong a large block of RCA shares and made him a millionaire.

Ironically, RCA did better commercially from a patent exchange agreement with Westinghouse which gave it access to the superhet patent.

Meanwhile Armstrong the millionaire had become a married man, having taken the RCA boss's secretary as his bride. He did very well all round from the RCA deal!

FREQUENCY MODULATION

Whilst the court cases with de Forest still dogged him, Armstrong somehow found the time and energy to make one more amazing radio invention, frequency modulation.

One problem that had plagued radio from its earliest days was 'static'. Static appears as a variation in the amplitude of the received signal and so any amplitude modulation (a.m.) receiver is prone to static interference. It was natural for radio engineers to try to reduce this interference. Many had tried and failed. Pupin had summed up the problem: "God gave men radio and the devil made static".

With Pupin, Armstrong had studied the matter as early as 1914. In the early twenties he called it a terrific problem, "the only one I ever encountered that, approached from any direction, always seems to be a stone wall".

In 1933 he surmounted that wall, acquired four new patents and opened a Pandora's Box of new tribulations which eventually drove him to suicide.

Yet frequency modulation (f.m.) was not new. It had been studied in 1902 and again in the 1920s but it was usually treated in a manner not unlike a.m. The bandwidth was kept as narrow as possible so as to restrict the passage of interference whilst still letting through the signal. Used in that way, f.m. was felt to have little to offer and was discarded. Mathematical investigations had dubbed it totally useless.

Armstrong's eventual answer was to step outside the existing state of the art and go the other way. In his own words, "The invention of the f.m. system gave a reduction of interfering noises of hundreds or thousands of times. It did so by proceeding in exactly the opposite direction that mathematical theory had demonstrated one ought to go to reduce interference. It widened instead of narrowed the band".

Armstrong himself paid for the construction of a transmitter and receiver. A demonstration was given in November 1935 at a frequency of 110MHz. The signal-to-noise ratio of around 100:1 was a lot better than the 30:1 of the best a.m. stations.

Then the troubles began. The US radio industry showed little interest. New transmitters and more expensive receivers would be needed. It was alleged that f.m. would not work beyound the horizon and that a.m. would be as good if the same high frequencies were used.

Armstrong offered the new system to RCA, which refused it and instead announced an intention to pursue electronic television, which would compete for the same frequency bands.

Armstrong had a stubborn streak. He sold a block of his shares and withdrew to go it alone. Using his own money he built his own station outside New York City. In July, 1939 he went on the air and proved that f.m. radio really did work and was superior in quality to a.m. radio.

An ally was found in a New England network which was suffering badly from static. F.m. broadcasting began to take off.

By January 1940, some 150 applications had began made to operate f.m. stations and 20 were either on the air or nearing completion. Westinghouse, General Electric and Zenith were among the companies queuing up for licences to make receivers and to meet Armstrong's condition of paying a royalty on each one. RCA offered a $1 million single payment with no royalties. Armstrong refused.

Then came more problems. World War Two delayed everything. At its end the Federal Communications Commission moved f.m. radio broadcasting to a new frequency band and restricted transmitter power to one tenth of the pre-war level. Over 50 f.m. transmitters and half a million receivers became obsolete.

Meanwhile RCA refused to recognise Armstrong's patents, depriving him of further fame and fortune. Smaller companies followed big brother's lead.

Armstrong began legal proceedings against RCA in 1948. More years of court battles loomed ahead. Five years later a further 20 actions were begun against other manufacturers whilst the RCA case was still far from settled.

Suddenly it was all too much. On a cold night at the end of January 1954 he put on his overcoat and jumped from the window of his 13th floor apartment in New York. It was a terrible indictment of the treatment meted out by parts of the radio industry to one of its greatest inventors.

Sixteen months later in Britain, the BBC began broadcasting a high-quality f.m. radio service.

Across the Atlantic, Armstrong's widow, Marion, rejected legal advice and fought on. She settled with RCA for the same million dollars her husband had rejected and used the money to fight the rest.

Thirteen years after his death it was finished. Ten million dollars of outstanding royalties and settlements were received. Armstrong was vindicated.

Next in this series of pioneers of electrical communication will be Jack S. Kilby, the man who made the first integrated circuit.

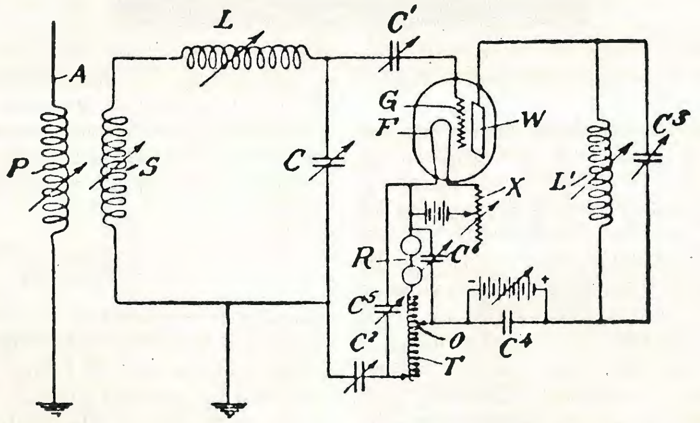


Fig.1. Armstrong's regenerative circuit, from the patent of 1912. Note the unfamiliar symbol for the triode.

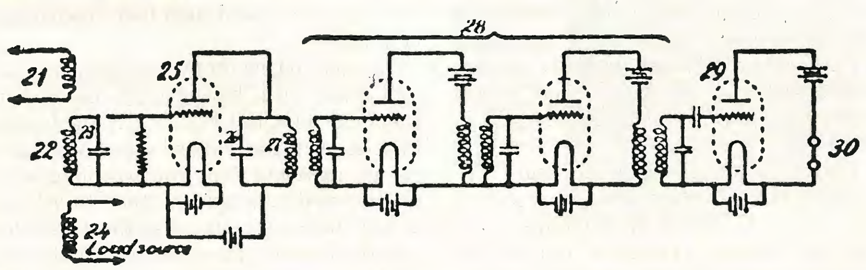


Fig.2. The superhet, from the 1920 patent – mixer, i.f. amplifier, detector and audio amplifier. The legend at bottom left identifies the local oscillator injection point.

Fast current-mode precision rectifier

Op-amps with supply-current sensing create a new fast precision rectifier.

CHRIS TOUMAZOU and JOHN LIDGEY

Op-amp supply current sensing is a technique widely used in the design of current-followers[1] and current-conveyors[2]. Current-mirrors are used to sense the op-amp output current via its supply leads. Positive output current is sensed by a current-mirror in the positive supply lead and negative output current is sensed by a second current-mirror in the negative supply lead. Our new current-mode precision rectifier exploits this output current phase-splitting action obtained with op-amp supply current sensing.

The basic circuit of a precision positive half-wave rectifier is shown in Fig. 1. It consists of two op-amps $IC_{1,2}$ and two current-mirrors $CM_{1,2}$. Wilson's current-mirror symbol[2] has been used to simplify the diagram. The driven side of the current-mirror is indicated by the arrow. Op-amp IC_1 and R_1 form a voltage-to-current converter at the input side of the circuit and IC_2 and R_2 form a current-to-voltage converter at the output.

Assume that both op-amps are ideal and that the phase of IC_1 output current exactly splits between the two supply leads. Positive supply current, I_1, is reflected to node x by the action of CM_1. Bias current, I_2, provided by CM_2 and R_p, is adjusted so that I_x is zero when the input is zero and hence output voltage, V_o, will be zero.

For positive input voltages I_1 will increase by V_{IN}/R_1, I_x will become V_{in}/R_1 and hence the output voltage V_o is given by

$$V_o=\frac{R_2}{R_1}.V_{IN}$$

Any inaccuracies in the current-transfer performance of CM_1 can be adjusted by changing the ratio of R_2 to R_1. For negative input voltages, the input current is now drawn by the negative supply lead of IC_1 to the negative d.c. supply and the circuit output is therefore zero, hence the circuit provides half-wave rectification.

The circuit can be extended to full-wave rectification, Fig. 2, by the addition of a third current-mirror CM_3. Negative output current from IC_1 sensed by CM_3 is added to the positive output current of IC_1 by CM_1. The net result is full-wave rectification of the input signal. Note that the bias current I_2 should be approximately doubled since the d.c. bias current through CM_1 is now doubled.

Although a natural development of Fig. 1 to the circuit of Fig. 2, this full-wave rectifier suffers from asymmetrical output unless the current mirrors CM_1 and CM_3 are identical. This is difficult to achieve in practice as they are complementary current-mirrors.

A better solution is shown in Fig. 3. The input of this circuit is effectively the differential input voltage-to-current converter that we previously described[3]. For positive input voltage, current I though resistor R is V_{IN}/R and this current is steered by IC_3 into CM_1. Output of CM_1 drives the transresistance circuit of IC_2 and R′.

As before it is necessary to include bias

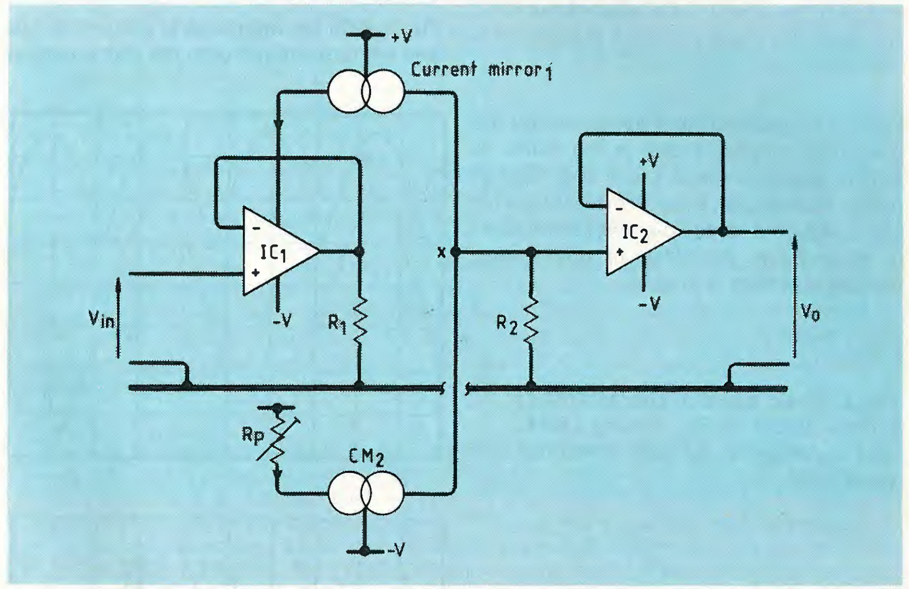


Fig. 1. Precision half-wave rectifier using current mirrors.

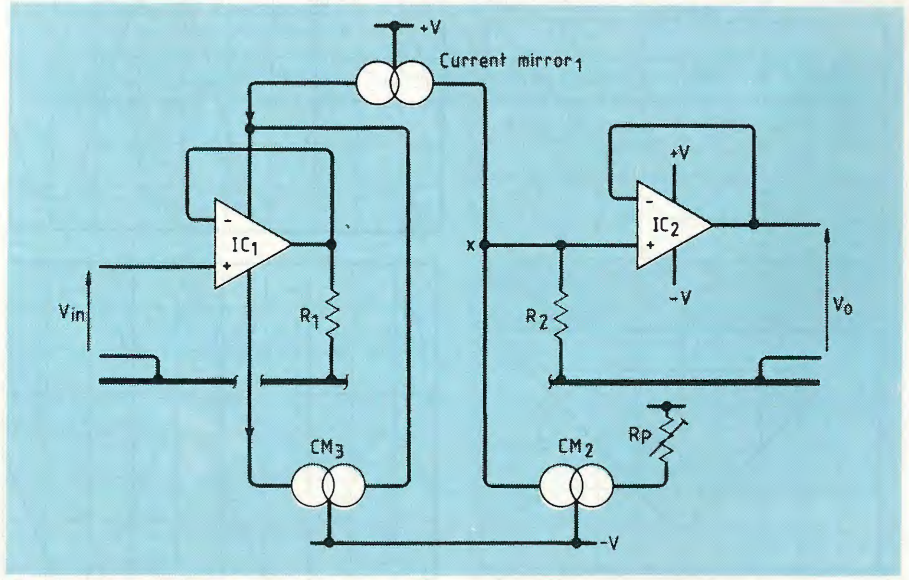


Fig. 2. Adding a further current mirror to Fig. 1 produces a precision full-wave rectifier.

current cancellation at node x, which in this case is provided by resistor R_p. For negative input voltage, current I flows in the opposite direction and is now steered by IC_1 into CM_1. Current into CM_1 over the full cycle is unidirectional and therefore the output voltage of IC_2, V_o, is given by,

$$V_o = \frac{R'}{R} \cdot |V_{IN}|$$

This circuit has three major advantages over the previous full-wave rectifier of Fig.2. Firstly, two well matched complementary current-mirrors are not required, as only one mirror is used in the signal path.

Secondly, the previous circuits used a current-mirror source in the signal path. This would inevitably be constructed with lateral p-n-p transistors, which have relatively poor high-frequency performance. The only current-mirror in the signal path of Fig. 3 is CM_1, which may be constructed using n-p-n devices.

And thirdly, since node x is held at zero potential by the negative feedback action of IC_2, the d.c. potential across the output of CM_1 is constant. This is an advantage over the two previous circuits because distortion is minimized if the output of a current-mirror is maintained at a fixed potential, as discussed in reference[2].

STATIC CHARACTERSTICS

In the explanation of how the circuit works we assumed that signal current of V_{IN}/R was perfectly phase split between each of the op-amp supply leads. However, this is not strictly true unless the magnitude of this current is substantially greater than quiescent bias current I_s of $IC_{1,3}$ and less than the output current limit, $I_{o(max)}$, of the op-amps, that is

$$I_s \ll V_{IN}/R < I_{o(max)}.$$

This equation shows that the best choice of op-amp to be one with a low quiescent bias current I_s. Clearly when the input signal falls to zero the inequality is not satisfied. Best performance can be obtained for a given range of input signal voltages, with appropriate choice of R so that the op-amp operates fairly close to the current limit of $I_{o(max)}$ at the maximum input-voltage level. A detailed analysis of this aspect of the rectifier's performance can be found in reference 4.

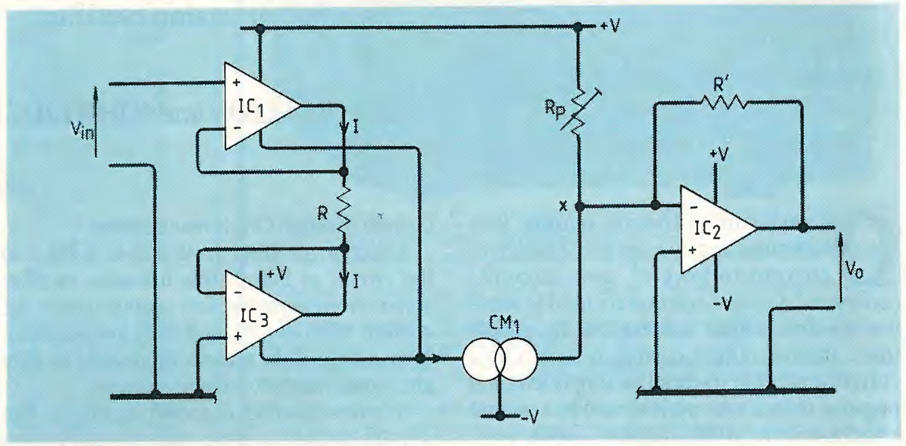


Fig. 3. With the improved precision rectifier, matched current mirrors are unnecessary and the current mirror in the signal path can be made using n-p-n devices.

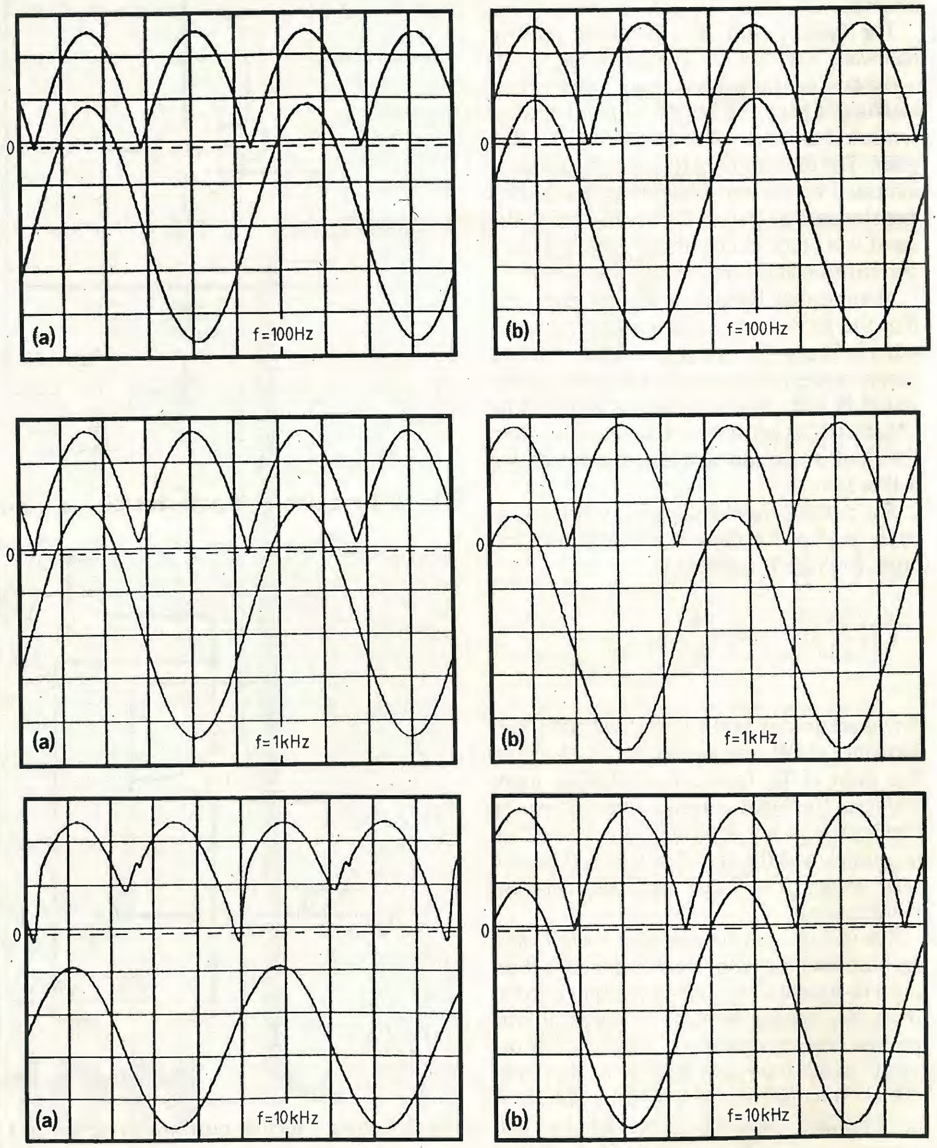


Fig. 5(a). Output and input waveforms for the traditional rectifier shown in the panel. At 100Hz output is clean but it degrades at higher frequencies. Waveforms at (b) are for Fig. 3, using the same op-amps; rectification is clean even at 10kHz. In both cases, vertical sensitivity is 5 div./V.

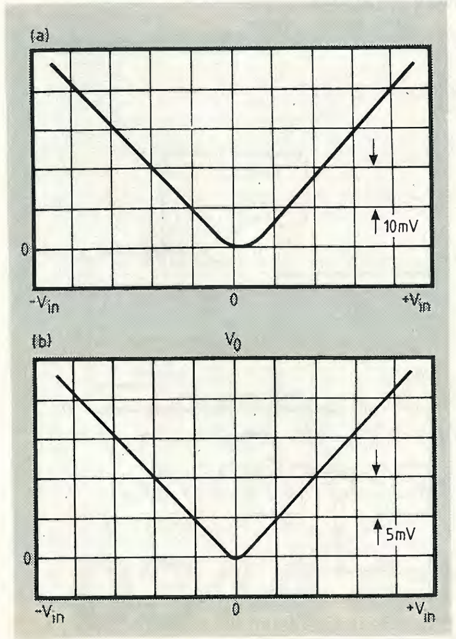


Fig. 4. Static transfer characteristics for the circuit of Fig. 4 using LM741 type op-amps at (a) and LF441 devices at (b).

We constructed and tested the circuit of Fig. 3 using two different types of op-amp, these being a LM741 and LF441. The high-performance four-transistor current mirror was used for CM_1, which was constructed using an RCA 3096 transistor array.

Static transfer characteristics are shown in Fig. 4. In each case resistor R was chosen to be 10Ω and R′ set nominally at 10Ω and adjusted until precise unity gain was obtained. This low value of resistance was selected to demonstrate the performance of the rectifier with input voltages of a few millivolts. Output current limits at approximately 11mA for the LF441 and 14mA for the LM741: should rectification performance be required at higher values of input voltage it would be necessary to select appropriately higher values for R and R′.

Figure 4 shows that the LF441 with a measured quiescent bias current of 0.14mA provides greater accuracy at low input signal levels than the LM741 op-amp, which was measured to have a bias current of 0.88mA, as expected from the previous equation for quiescent bias current. Resistor R_p was selected in each case to zero the output d.c. offset voltage.

HIGH-FREQUENCY PERFORMANCE

To test the comparative performance of the existing rectifier shown in the panel and the one in Fig. 3 at high frequencies, the op-amps were changed for LM308 devices with 50pF feed-forward compensation capacitors. These devices are ideal as they have wide open-loop bandwidth together with a relatively low quiescent bias current of about 0.3mA.

Values used in the existing circuit shown in the panel for R_1, R_2, R_3 and R_5 were well matched 20kΩ resistors and R_4, nominally 10kΩ, was adjusted to give unity gain. Diodes D_1 and D_2 were fast small-signal silicon diodes. Values used for the circuit of Fig. 3 were R=R′=100Ω to obtain an optimum rectifier performance for a 1V peak-to-peak input signal used. In both cases the power supplies were set at ±15V.

Waveforms of the two circuits are shown in Fig. 5. The LM308 op-amps that were used in the traditional circuit were then removed from that circuit and used in the improved rectifier of Fig. 3 for $IC_{1,3}$ so that an accurate comparison could be made between these two circuits.

Low frequency traces of 100Hz shows there

EXISTING PRECISION RECTIFIERS – A REVIEW

The most common precision full-wave rectifier, shown here, is called precision because it works even if its input voltage is less than the voltage drop across a forward-biased diode, unlike simple diode rectifier circuits with no op-amps.

For a positive input voltage, output of IC_1 becomes negative, diode D_1 is forward biased, and diode D_2 is reverse biased. Voltage at node x, V_x, is,

$$V_x = \frac{-R_2}{R_1} V_{IN}. \quad (1)$$

Op-amp IC_2 is configured as an inverting summing amplifier and output voltage V_o is given by,

$$V_o = -R_5(i_4 + i_3) \quad (2)$$

Since $i_3 = V_{IN}/R_3$ and $i_4 = V_x/R_4$ then

$$V_o = \left(\frac{R_2}{R_1} \cdot \frac{R_5}{R_4} - \frac{R_5}{R_3} \right) V_{IN} \quad (3)$$

for $V_{IN} > 0$.

If V_{IN} is negative, then output of IC_1 goes positive, D_2 conducts, D_1 is reverse biased and node x will be virtually zero, making i_4 zero. Output voltage of the circuit is again given by equation (2) and can be written as

$$V_o = -R_5/R_3 V_{IN} \quad (4)$$

for $V_{IN} < 0$. It is clear that if,

$$\left(\frac{R_2 R_5}{R_1 R_4} \right) - \left(\frac{R_5}{R_3} \right) = \left(\frac{R_5}{R_3} \right) \quad (5)$$

then, $$V_o = \frac{R_5}{R_3} |V_{In}|. \quad (6)$$

Equation (5) can be simplified to,

$$\frac{R_2}{R_1} \cdot \frac{R_3}{R_4} = 2. \quad (7)$$

This condition may be satisfied using equal value resistors by making $R_1 = R_2 = R_3 = R$ and $R_4 = R/2$, i.e. two R value resistors in parallel. As you can see from equation (6), R_5 will control the voltage gain of the rectifier. Note that for half-wave rectification, all that is needed is IC_1 with R_1, R_2 and the two diodes.

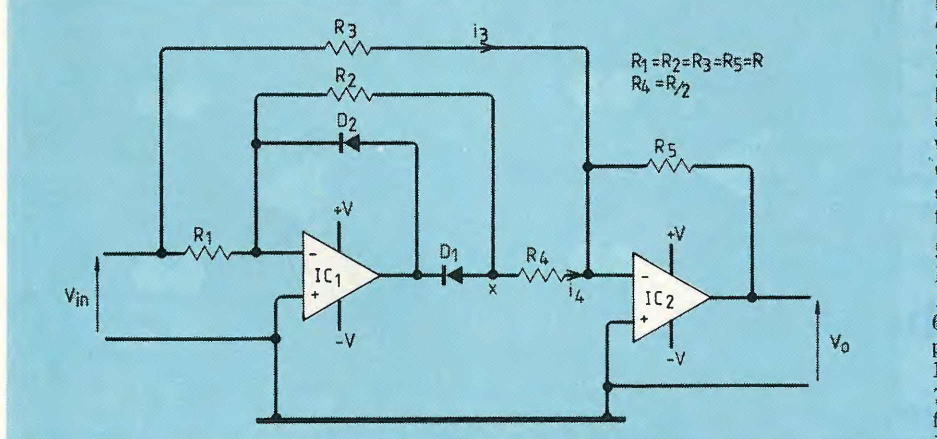
Although this circuit is faster than other diode/op-amp precision rectifiers, since it avoids undesirable output saturation delays, it suffers from two major problems.

(i) During the cross-over as the input changes polarity, there is a period when both diodes are off and IC_1 is therefore open-loop. This causes output signal distortion at surprisingly low frequencies. One might expect the time, t_d, during which IC_1 is open-loop to be approximately given by

$$t_d = 2V_D/SR \quad (8)$$

where V_D is the forward voltage drop of a single diode, approximately 600mV, and SR is the slew rate of IC_1. But the actual delay time can be much greater than this depending on the magnitude of the input signal. By definition, the slew rate is the maximum rate of change of output voltage with time. To reach the slew rate, the input stage of IC_1 must be driven with a voltage large enough to saturate the input stage; for example a typical long-tail pair bipolar input saturates with about 200mV difference between the inverting and non-inverting inputs[5]. If the input voltage at IC_1 is less than this the resultant delay time will be much longer than that given by equation (8) and as a consequence output distortion for low amplitude inputs is quite severe.

(ii) The second problem with this circuit is resistor matching. It is apparent from equation (7) that four precisely matched resistors are essential for correct rectifier operation. We have evaluated this circuit experimentally using several different types of op-amp in an attempt to obtain optimum performance. Results show significant output-signal distortion at frequencies well below the full-power frequency capabilities of each op-amp used, as explained above.



Several alternative schemes can provide precision rectification without diodes in the circuit. Perhaps the most versatile of these schemes is the one first reported by Barker and Hart[6] and recently resurrected by Lewis[7]. This circuit provides good linearity at low frequencies, but the class-B mode in which this circuit operates results in similar output distortion to the precision rectifier shown, and again the high-frequency performance is limited.

5. Lidgey, F. J., The tale of the long-tail pair, part I, *Electronics & Wireless World.* September 1985, pp.74-76.
6. Barker, R. W. J. and Hart, B. L., Versatile precision full-wave rectifier, *Electronics Letters,* 1977, No.13, pp. 143-4.
7. Lewis, K., Level-translating full-wave rectifiers, *Electronics & Wireless World.* March 1986, vol. 93, No. 1601, pp. 22-4.

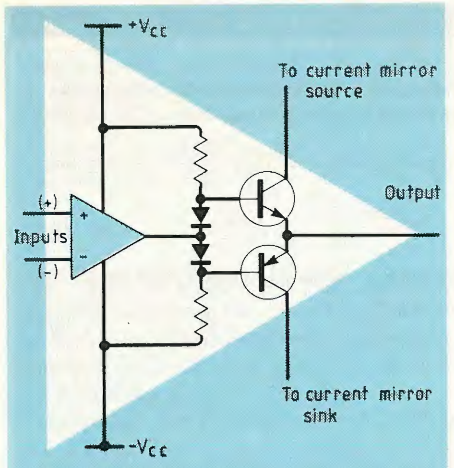


Fig. 6. Seven-terminal op-amp created using discrete components and an op-amp – such an i.c. would be a useful building block.

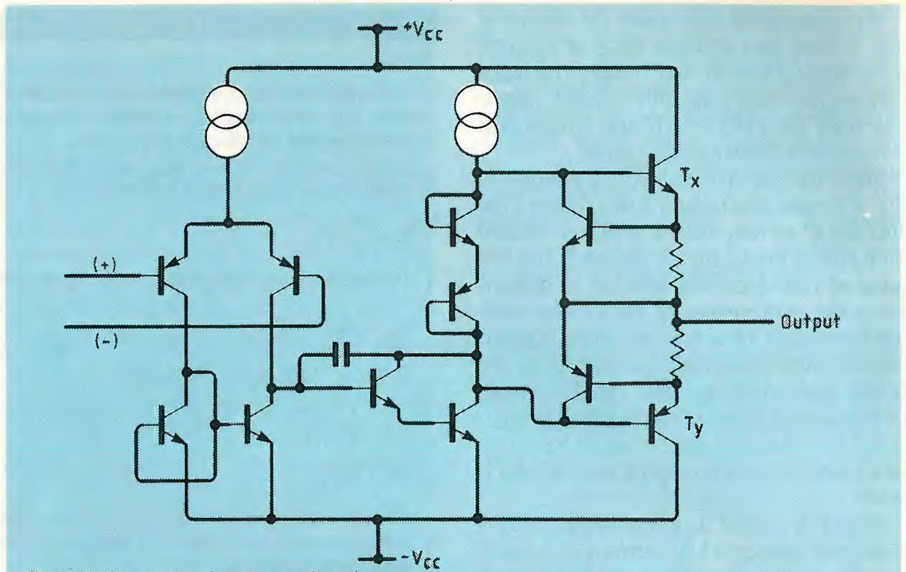


Fig. 7. Schematic of a conventional op-amp.

to be very little difference between the two circuits. However, at a frequency of 1kHz there is some distortion occurring for the traditional circuit which becomes extremely distorted at the highest frequency shown of 10kHz.

As you can see, performance of the improved rectifier of Fig. 3 is shown unchanged in the waveforms in Fig. 5(b). Further tests showed the circuit continued to perform well as the frequency was increased to about 1MHz.

A SEVEN-TERMINAL OP-AMP?

Rather than the five-terminals of a conventional op-amp, it would be very useful if a seven-terminal op-amp were available, the additional two terminals being the collectors of the output push-pull pair. This would then allow direct output current sensing, rather than sensing the whole of the op-amp supply current.

If such an op-amp were available the dynamic range of the precision rectifier from the equation for quiescent bias current would be much greater since the effective value of I_s is now only the bias current in the output transistors.

To verify this proposition we extended a conventional op-amp by adding an additional push-pull output stage to simulate the proposed seven-terminal op-amp, shown in Fig. 6. As expected, when using the seven-terminal op-amp of Fig. 6 to replace $IC_{1,3}$ in the precision full-wave rectifier of Fig. 3, the dynamic range was extended and better accuracy achieved at low input-signal levels.

A schematic of a conventional op-amp is shown in Fig. 7. The required seven-terminal op-amp is created simply by taking the output collector of Tr_x and Tr_y to two external pins instead of being connected, as shown in Fig. 7, to the common d.c. supply lines. Such a modification could easily be carried out by the manufacturers of op-amps and the versatility of the op-amp extended to allow true output current sensing. There are many other very useful applications based on supply current sensing, several of which are referred to in section 9 of reference 4, and most would benefit if a monolithic seven-terminal op-amp were available.

CONCLUSIONS

The novel precision rectifier we have described is clearly far superior in performance to conventional op-amp based precision rectifiers. The circuit is easy to design and construct from readily available low-cost components, and provides excellent precision rectifier performance over a wide band. In addition, we propose that semiconductor manufacturers should consider making a seven-terminal op-amp, rather than the conventional five-terminal device, to further improve the performance of this precision rectifier and other applications based on similar op-amp supply-current sensing techniques.

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1. Lidgey, F. J. and Toumazou, C., Accurate current follower, *Electronics & Wireless World*, April 1985, vol. 91, No. 1590, pp. 17-19.

2. Wilson, B., Using current-conveyors, *Electronics & Wireless World*, April 1986, vol. 93, No. 1614, pp. 28-32.

3. Toumazou, C. and Lidgey, F. J., Floating impedance converters using current-conveyors, *Electronics Letters*, 1985, No.21, pp. 640-642.

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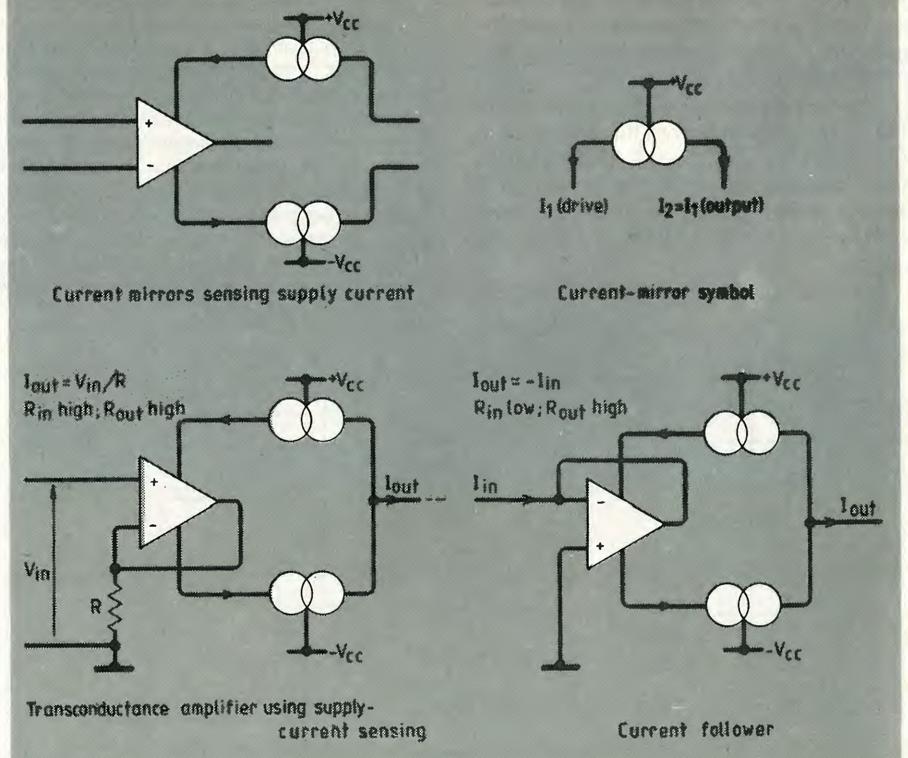
Chris Toumazou BSc, PhD, and John Lidgey BSc, PhD, CENG, MIEE.

Supply current sensing extends op-amp capabilities

Two further applications of this supply-current sensing technique are the transconductance amplifier and current follower shown here. Creating these circuit functions using conventional op-amp techniques results in poorer performance and increases circuit complexity.



Current mirrors sensing supply current — Current-mirror symbol — Transconductance amplifier using supply-current sensing — Current follower

THE 68030

New architecture, higher integration and improved chip layout result in a 32bit processor that runs twice as fast as the 68020 in some systems.

DAVID JONES and DAVID BURNS

Towards the end of this year, the 68030 32-bit microprocessor will be in production. This device, a member of the Motorola 68000 family, is similar to its predecessor the 68020 but it has additional features to enhance performance. These features include on-chip Harvard-type architecture, and integrated data cache and memory-management units.

Hardware and software compatibility with other devices in the 68000 family is retained. The 68030 user programming model is identical to the 68020 model, that is the 68030 runs all 68020 instructions and has the same addressing modes. Due to integration of the memory-management unit, the supervisor programming model is similar to that of a 68020 with 68851 memory-management coprocessor.

Layout within the chip has been modified, partly to accommodate the coprocessor and caches of course, but also to reduce the internal data and instruction paths so that the chip can operate at higher speeds.

ON-CHIP FEATURES

Built into the chip are a memory-management unit functionally similar to the 68851 coprocessor, and data and instruction caches; the 68020 has only an instruction cache. This integration reduces hardware design costs; further, the 68030 will be cheaper and give higher performance than a 68020 with separate 68851 m.m.u.

Like the 68851, the 68030 memory-management unit accommodates multiple-level translation tables, limit fields and software programmable page sizes. It also has a 22-entry address-translation cache for holding most-recently-used logical-to-physical address translations. Hence the 68030 memory-management unit is software compatible with the 68851.

Unlike the 68851 though, the 68030 memory manager allows windows to be set up in the memory map within which addresses are not translated in the normal way. Instead, addresses falling within the windows are given a one-to-one address translation. Typical applications for this feature include manipulation of large data stores such as bit-field graphics.

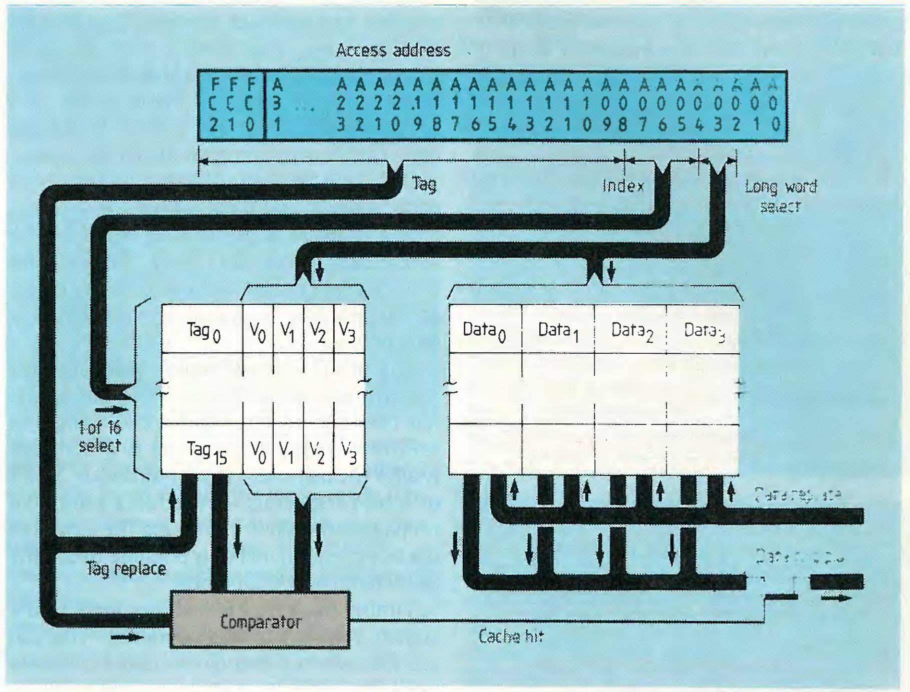


Fig.1. Data and instruction cache organization. Each cache entry is four long words. Validity of each long word is represented by the associated V bit. In total there are sixteen entries of four long words.

An instruction cache of 256 bytes is built into the 68020; on the 68030, this memory is supplemented with a 256byte data cache. In the 68030 both caches are organized as sixteen entries of four long words (sixteen bytes) whereas in the 68020, the instruction cache is organized as 64 long-word entries (only four bytes per entry), Fig.1.

This difference in organization has a significant effect on cache performance since it allows a sixteen-byte data block to be loaded into the cache on any update. Using nibble-mode dynamic rams for example, block filling can be very fast and efficient.

A cache is a section of memory designed for very high-speed access. All caches operate on the principle of temporal loclaity of reference for information, i.e., if a location is accessed by the processor then there is a high probability that the same location will be accessed again in the near future. By storing the location's information in high-speed cache memory, subsequent accesses to it will be performed in a shorter time.

In addition to this principle, 68030 caches apply spatial-reference locality which involves multiple-word entries and burst filling. If a location is accessed by the processor, there is a high probability that an adjacent location will be accessed in the near future. The 68030 takes advantage of this probability by burst filling a block of four long words on each cache update. Program code sequences, where subsequent instructions usually follow in a sequential manner, are a good example of where this technique is advantageous.

Internal structure of the 68030 is shown in Fig.2, which also illustrates the Harvard-style architecture. Program and data spaces have their own separate address and data buses so they can operate concurrently. It is possible for the processor to access instruction and data caches simultaneously on separate internal buses.

Also at the same time, the bus controller can be accessing external memory using a physical address produced by the memory manager. Being on chip, the memory-management unit can perform address translations concurrently with internal cache accesses so the logical-to-physical address translation is effectively instantaneous.

IMPROVED BUS CONTROLLER

Having instruction and data caches on chip, the 68030 can execute many operations without any use of the external bus. Increasing the rate at which instructions and data are transferred between cache memory and the c.p.u. significantly improves processing speed.

You will notice that many of the 68020 signals are the same as those of the 68030, yet the two devices are not pin compatible. In fact only twelve pins on the 68030 package are in the same place as those on the 68020. This is because the new processor is more

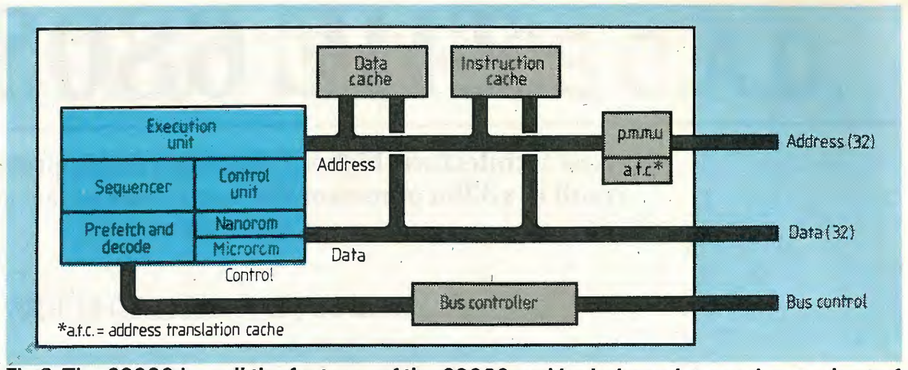


Fig.2. The 68030 has all the features of the 68020 and includes a data cache, a subset of the 68851 memory-management unit, an improved bus controller and on-chip Harvard-style architecture.

scrupulously laid out internally. Room had to be made for the extra cache and m.m.u. but data and instruction path lengths have also been shortened to reduce their RC time constants.

Shortening signal-path lengths made it possible to construct the 68030 to 20MHz design rules. The 68020 was designed according to 16MHz rules and devices operating at 25MHz are now being made; as a result we expect to see higher frequency 68030 processors being produced very soon.

Reducing the time it takes internally to drive address and data buffers for external pins has made it possible to improve the 68030 bus controller. Now, rather than fetching data or instructions over the external bus in three clock cycles, it is possible to do it in two.

To control this faster fetch, a signal called synchronous termination, STERM for short, has been included. Dynamic bus sizing – a feature allowing the processor to dynamically alter the bus width to accommodate 32, 16 or 8 bit peripherals – introduces additional propagation delays, increasing the length of the bus cycle, so it is only possible to use the faster fetch over a 32bit bus.

Timing diagram Fig.3 shows some of the signals relevant to bus operation. You can see that when a two clock period synchronous bus cyle is executed, STERM replaces $DSACK_{0,1}$ to terminate the bus cycle.

In an asynchronous design, no assumptions are made concerning the processor clock and all bus cycles are performed with respect to strobes AS, DS, $DSACK_X$, etc. For the synchronous operating mode, the clock is an important part of the system design and all references are relative to the clock position; this permits the design of very fast systems.

When a 68020 bus cycle starts, operand-cycle start signal OCS and early cycle start signal ECS are asserted.* But since ECS and OCS can be asserted when there is a hit in the instruction cache and no external bus cycle follows for that address the address strobe must be used to indicate that a valid address is on the bus.

With the 68030 the bus structure is the same except that AS does need to be used to indicate a valid bus cycle when the two clock period synchronous bus cycle is executing. This is because the 68030 is designed to only

recognize signal STERM while the address is being strobed, In Fig. 4, the instruction cache has a hit followed by a hit in the data cache before an external synchronous bus cycle is executed using STERM.

Any mixture of the three types of bus cycle is possible with the 68030 bus controller. It can be dynamically configured for each bus cycle depending on the states of signals STERM or $DSACK_X$. The only limitation is that STERM and $DSACK_X$ are not asserted during the same cycle.

Chip-select logic for a very fast memory area accommodating two clock cycle read and write activity is outlined in Fig. 5. The address bus and/or function codes produce chip-select and STERM is asserted continuously during the address-space access.

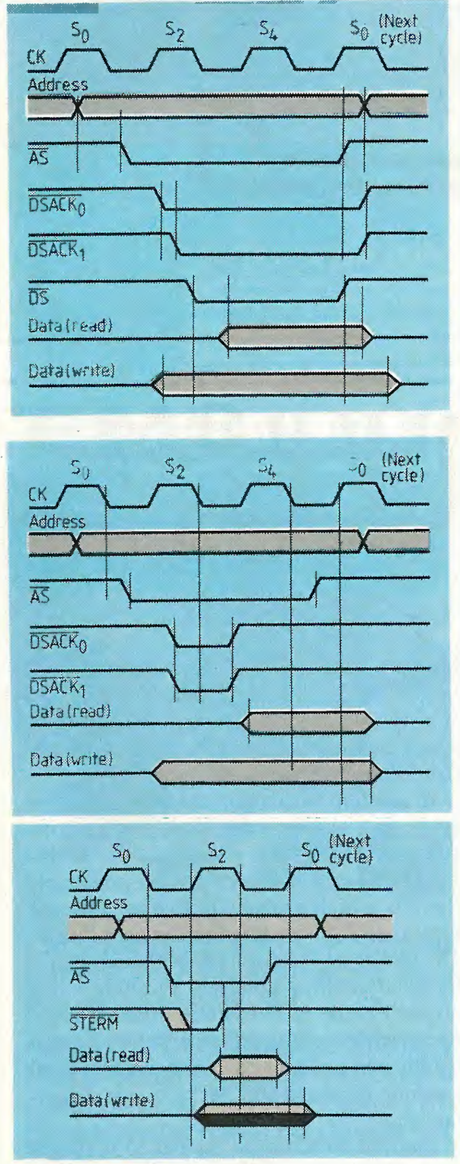


Fig.3. Using the new STERM signal, the 68030 bus controller can operate and control three types of bus cycles, (a) aysnchronous bus cycle, (b) three-clock (or more) synchronous bus cycle and (c) a two clock period (or more) synchronous bus cycle STERM.

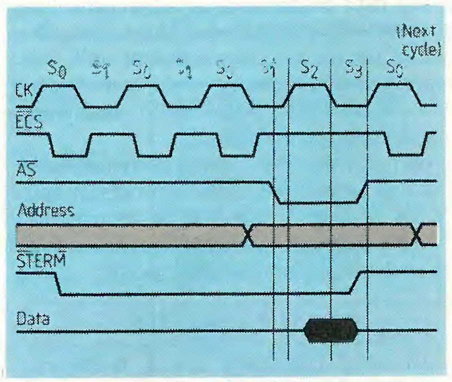


Fig.4. Bus operation using STERM. This signal is sampled on or before a rising clock edge in this time period. The cycle shows an instruction and data cache hits followed by an external bus cycle.

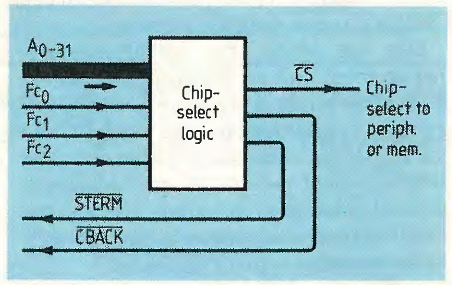


Fig.5. Chip select logic to peripherals or memory accessed in two clock cycles. The 68030 uses STERM to terminate a bus cycle in two clock periods. Address strobe AS is not required in the chip-select logic as STERM is only recognized during the period that AS is asserted. The CBACK signal is only recognized during the same period as STERM and when the 68030 has issued CBREQ.

*To avoid ambiguity in signal level descriptions, the term asserted is used to describe when a signal is active low or active high.

As with 68020 and 68030 $DSACK_X$ signals, STERM can be used to both terminate and lengthen a bus cycle. Under normal operation the 68030 can change the length of the bus cycle by monitoring the $DSACK_X$ signals.

The processor senses $DSACK_X$ signals on the falling edge of the bus cycle S_2 state. If the $DSACK_X$ signals are asserted before the falling edge then the data is valid in the case of a write cycle or is latched on the falling edge of S_4 in the case of a read cycle. If the $DSACK_X$ signals are not asserted at this edge then the processor waits, inserting extra clock periods into the bus cycle until they are asserted prior to a falling clock edge; this state then becomes S_2.

When used with a 32bit bus, STERM operates in a similar way to the $DSACK_X$ signals. If STERM is not asserted on or before the rising edge of S_2 then the processor waits, inserting extra clock periods until STERM is asserted on a rising clock edge. At this point, the next state becomes S_2.

For three clock-cycle 32bit bus, replacing $DSACK_X$ with STERM allows extra time for memory decoding, cache tag comparison or data error detection and correction, Fig. 6. Signal STERM can also be used for termination of a data read from external memory during the cache burst-filling operation.

When there is a cache miss, or all four of the valid bits are invalid in the data or instruction caches, the processor asserts the cache-burst request signal CBREQ during the bus cycle S_1 period. If the memory can accommodate burst filling of the caches then the memory control logic should acknowledge this request by asserting the 68030 cache-burst acknowledge signal CBACK.

Acknowledge signal CBACK should be asserted during the same period as CBREQ but in some systems, it may not be possible to assert CBACK following CBREQ. For this case, CBACK can be continuously asserted for the memory areas that can accommodate burst filling in much the same way that STERM is used in Fig. 5. Here, CBACK is only recognized during address strobing.

During burst filling, the 68030 can read up to four long words into the cache. If CBACK is negated before the four long words have been read then only three, two or one long words will be placed in the cache.

Instruction or data fetches can be used by the c.p.u. as they are loaded into the cache during burst-filling. Advantages of this are that the c.p.u. is not idle during the burst filling and that the caches are updated very quickly.

Each long word is terminated by the STERM signal. If STERM is asserted on or before the rising edge of the clock then the data is latched on the next falling edge. Therefore if STERM is asserted for the whole duration of the burst fill then no wait states are inserted. In this situation, four words can be fetched in only five clock cycles, Fig. 7.

From Fig. 7 you can see that CBREQ is negated after only three long-word fetches. The reason for this is that CBREQ is used to indicate that the bus controller can accept one more long word. Therefore at the end of the third long word, if an acknowledgement is present, then there are no more words to be fetched.

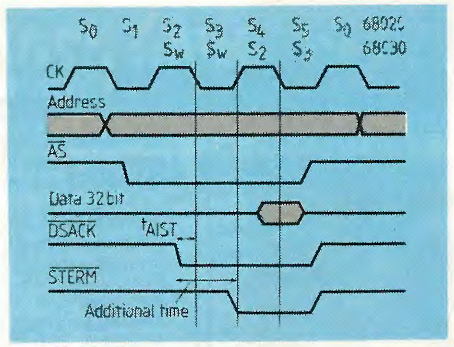


Fig.6. Timing diagram showing additional decision time when STERM is used instead of the $DSACK_X$ signals. Replacing $DSACK_X$ signals with the STERM signal on a 32-bit data transfer using normal three clock cycle accesses allows additional decision time for error detection/correction, parity checking etc. Time gained is equal to one state time plus asynchronous set-up time t_{AIST}.

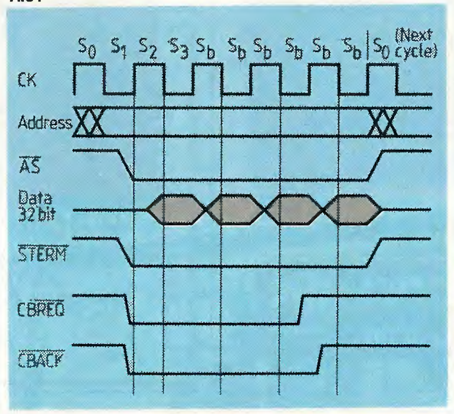


Fig.7. Using a two-clock-period synchronous bus cycle the 68030 can handle a complete burst fill of four long words into the instruction or data caches in only five clock cycles. This gives the 68030 a maximum data transfer rate of 64Mbyte/s at 20MHz.

The same situation applies to the CBACK signal indicating that the memory can supply one more aligned long word of data on the data bus. However CBACK can still be asserted for the whole duration of the burst filling operation without affecting it.

CACHE AND M.M.U. CONTROL SIGNALS

Several signals are provided for the control of the on-chip caches and memory-management unit. Signals CDIS and MMUDIS allow external hardware to disable the caches and memory manager respectively. Further cache control is provided by the CIIN signal which prohibits specific memory accesses from being cached, and CIOUT which is sent out by the memory management unit to indicate that the accesses should not be captured by any external caches.

These signals are especially useful for maintaining the integrity of input/output peripherals whose control registers, etc., must not be cached.

PREVIOUS 68000 ARTICLES

Trends in the 68000 family, December 1986 pp. 106-109.

Within the 68020 I, January 1987 pp. 103-106.

Within the 68020 II, February 1987 pp. 209-212.

68020 display processing, March 1987 pp.333-334.

68020 coprocessors (68881/2 maths units), May 1987 pp. 535-537.

68020 coprocessors (68851 m.m.u.), June 1987 pp.614-616.

Cache memory design, July 1987 pp. 727-730.

CONCLUSION

Performance improvement of the 68030 in relation to the 68020 depends on the type of system that the processor is used in; in some cases a doubling of performance is possible. Relative cost savings are possible too if the on-chip memory-management unit is used. Board area and design time are reduced and the 68030 will cost less than a 68020 and 68851 combination.

Time taken for the 68030 memory manager to perform logical-to-physical address calculations is considerably less than that taken by a 68020/68851 combination because of the pipelining facility.

Burst filling of the caches speeds up memory operations significantly. Current 1Mbit dynamic rams permit very fast burst filling in page, static-column and nibble modes. Using the Toshiba TC11001P/CJ-10 for example, nibble-mode accesses can be performed in 40ns. Before dynamic rams with these modes were available, the only way of operating memory with no wait states at these high speeds was to use expensive and lower-density static rams.

With the improved bus controller, on-chip Harvard-style architecture and data and instruction caches, extra performance is gained with less hardware than that required for a 68020 systems.

David Jones and David Burns are applications engineers at Motorola, East Killbride.

New floating point coprocessor

Samples of the 68882 floating-point coprocessor described in the May issue are now available. Like its predecessor – the 68881 – the 68882 links to the main 68000 family processor through the coprocessor interface and it conforms to the IEEE 754 standard for floating-point arithmetic, introduced in January 1985.

Unlike any competitive device the 68882 provides in hardware the fullest selection of transcendental and non-transcendental functions, including root values, trigonometric functions, exponentials, hyperbolics and logarithmics.

Mnemonic	Function
FSIN	Sine
FASIN	Arc sine
FSINH	Hyperbolic sine
FCOS	Cosine
FACOS	Arc cosine
FCOSH	Hyperbolic cosine
FSINCOS	Simultaneous sine/cosine
FTAN	Tangent
FTANH	Hyperbolic tangent
FATAN	Arc tangent
FATANH	Hyprbolic arc tangent
FETOX	e to the power x
FETOXM1	e to the power x – 1
FTENTOX	10 to the power x
FTWOTOX	2 to the power x
FLOG10	Logarithm base 10
FLOG2	Logarithm base 2
FLOGN	Logarithm base e
FLOGNP1	Logarithm base e of x+1

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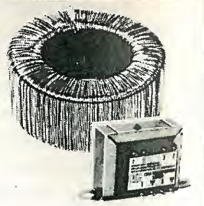

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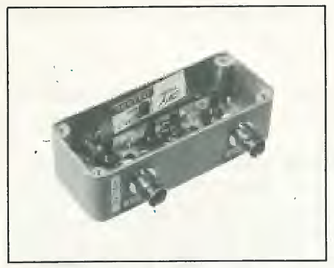

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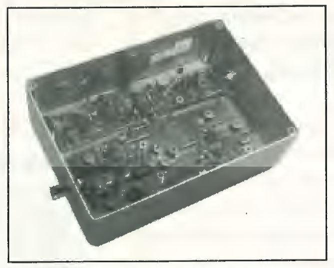

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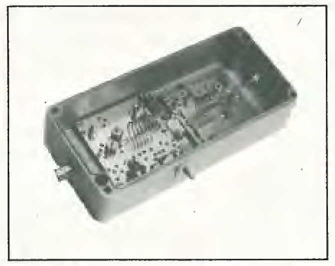
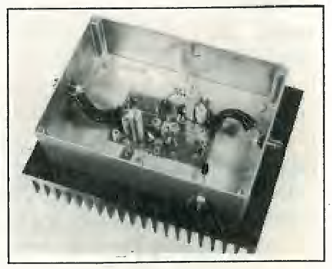


TUNED AMPLIFIER



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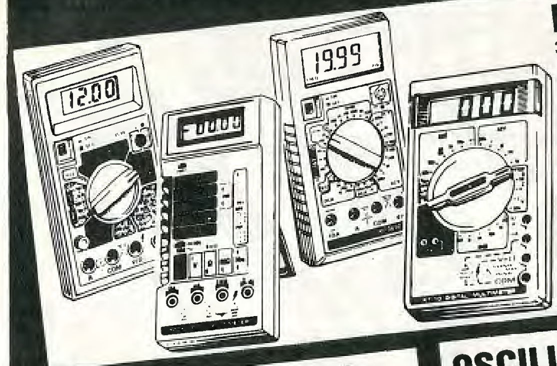

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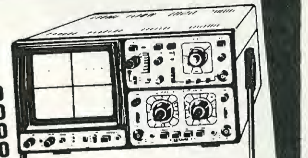

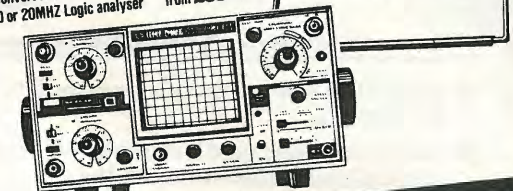

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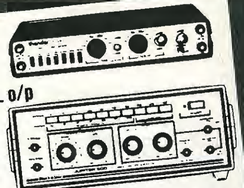

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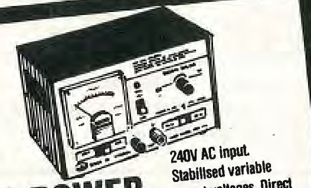

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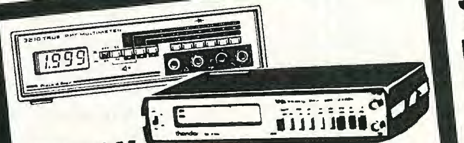

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Gyrators in band-pass filter design

Gyrators facilitate the design of LC filters without the need to wind inductors

R. H. TROUGHTON

Laboratory development work occasionally requires the use of small-signal bandpass filters, but many engineers regard their design as a black art which must be left to specialists. This need not be so, as will be demonstrated, and it is hoped to encourage others to circumvent delay to their project caused by reliance on specialized design services.

The procedure to be described utilizes "classical LC ladder sections without suffering their major inconvenience, the need to wind inductors. Filters based on simulated inductors can be easily designed and implemented, offering the following advantages:

- the noise associated with switched capacitor filters is eliminated;
- long term stability is inherent and superior to universal active filter structures (Ref 2.);
- the use of "gyrators", formed from standard operational amplifiers, permits realisation in a compact form, ideal in v.l.f. applications;
- normalized tables already exist for all the commonly required transfer functions, Butterworth, Chebyshev, Gaussian, Bessel, etc., so that only simple arithmetic is required to produce a usable circuit.

There are two prerequisites for the design procedure which follows. Firstly, the upper frequency of operation is limited to approximately 50kHz. This constraint is due to increasing phase disparities between dual or quad packaged amplifiers as the operating frequency is raised. "Dedicated" gyrator i.cs can be obtained for higher frequencies, but they are expensive and often single-sourced. Secondly, normalized tables must be available for the desired filter type. Those contained in Reference 1 are particularly recommended, as indeed is the book itself, which must surely be regarded as the definitive work on filter theory, design and construction.

SELECTING THE MOST SUITABLE TYPE OF FILTER

In broad terms there must be a trade-off between the desirably abrupt transition, when passing from stop to passband, versus its concomitant penalty, amplitude ripple and phase non-linearity. A reasonably gradual transition, e.g. Butterworth, gives good phase response (near-equal time delay to all frequency components within the passband) combined with a flat-topped passband amplitude characteristic. Conversely, the Chebyshev functions give a sharper transition, with steep skirts but also passband phase non-linearity combined with amplitude ripple, due to cascading high-Q sections. In comparison, Bessel and Gaussian filters give improved phase linearity and are useful where known group delays are required, but extra sections are needed to achieve skirt-shape characteristics approaching that of the Butterworth response. The disadvantages of the Chebyshev response can often be tolerated, since in most cases a small amount of ripple (say 0.1 dB) combined with some phase non-linearity is insignificant compared to the sharpness of the filter response obtainable with a modest number of sections.

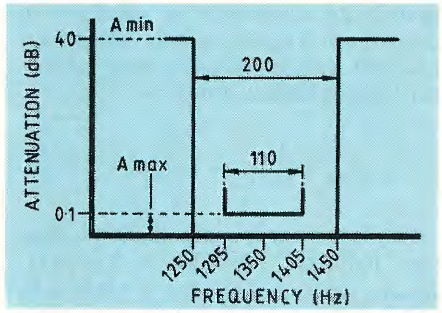


Fig.1. Characteristics of band-pass filter under discussion.

DESIGN EXAMPLE

An audio bandpass filter is required having the following characteristics:

(a) centre frequency, $F_m = 1350$Hz.
(b) 3dB bandwidth, BW, = 110 Hz ($F_m \pm 55$ Hz).
(c) input/output resistance, R_1, $R_2 = 600\Omega$.
(d) permitted insertion loss, i_L, ≈ -10dB.
(e) skirt shape: −40 dB at $F_m \pm 100$ Hz.
(f) permitted passband ripple = 0.1 dB.

The basic requirements, in stylized form, are shown in Fig. 1.

The skirt shape specification for the filter will determine the type of transfer function selected and, since this is relatively steep (e), Chebyshev would seem appropriate, since 0.1 dB ripple is tolerable (f), and there are no particular phase-linearity requirements stated. The transition ratio, 200/110=1.8, obtained from Fig. 1 (skirt BW at specified attenuation/3dB BW) will determine the number of sections (N) within the filter. The N/attenuation graph, Fig. 2, accompanying the tables in Ref. 1, indicates that a six-section Chebyshev 0.1 dB ripple filter will give approximately 45 dB attenuation at the

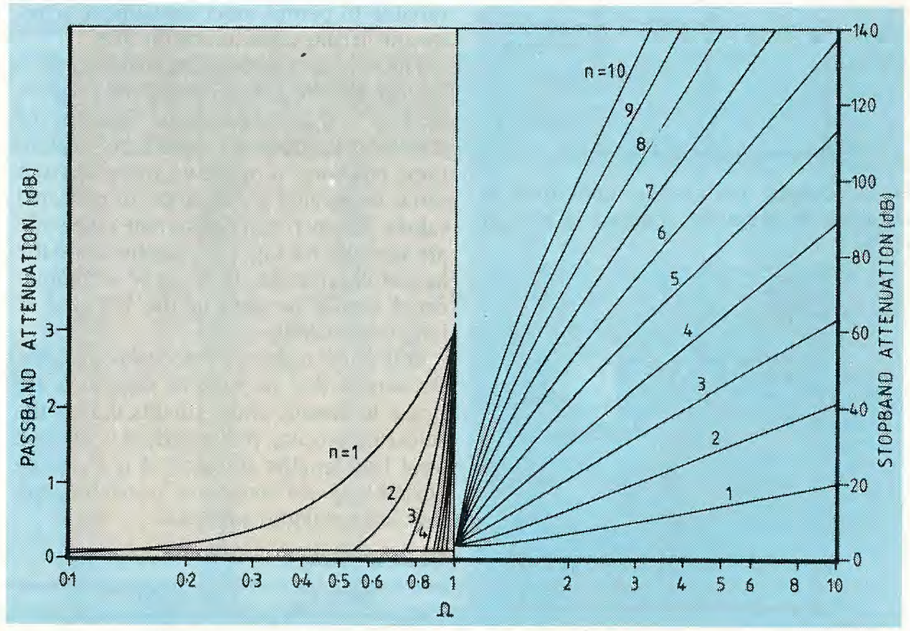


Fig.2. Attenuation characteristics of Chebyshev filter with 0.1dB ripple. A six-section filter (N=6) gives 45dB attenuation at a transition ratio of 1.8.

specified transition ratio, and we can now refer to N6 0.1 dB look-up tables (Ref. 1). A choice of q_o is available and selection is governed by the working Q obtainable from the filter inductors. Though the Q of simulated inductors can be high (500 is readily achievable at a.f.) it is good practice to use a lower Q and make up for the increased insertion loss by the inclusion of a gain stage, which can also serve to buffer the

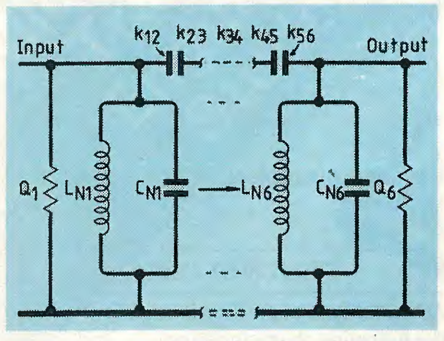


Fig.3. The positions of circuit elements found from published tables.

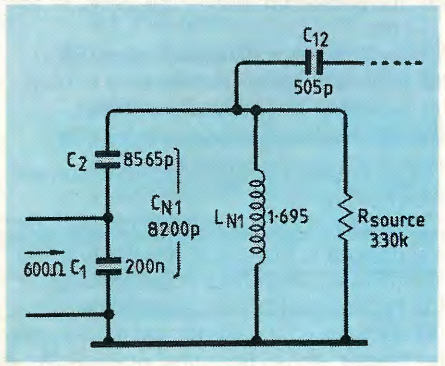


Fig.4. Input resistance of 600Ω is obtained by tapping the element C_{N1}.

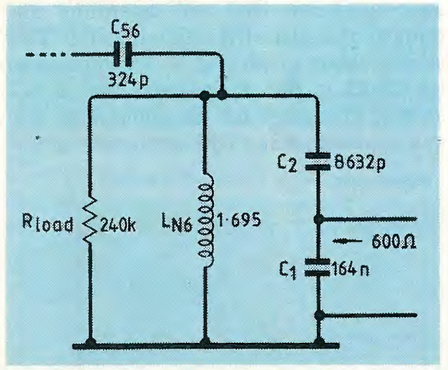


Fig.5. Output resistance specified is obtained in a similar manner to that of Fig.5.

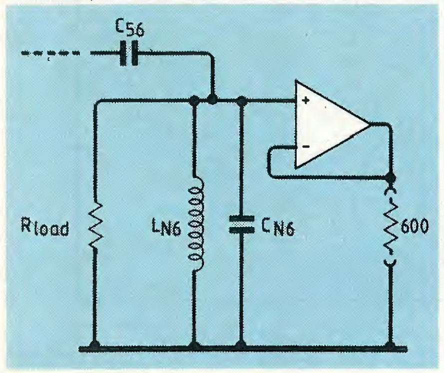


Fig.6. Alternative to output circuit of Fig.6, using voltage follower.

filter. $Q_{min}=q_oF_m/BW$, where Q_{min} = the minimum acceptable loaded Q of any inductor in the filter, and choosing q_o = 13.613 requires that Q_{min} = 167. An insertion loss of 11.122 dB is also predicted for this tabulation. The normalized values selected are:

q_o	I_L	q_1	q_6	k_{12}
13.613	11.122	1.8774	1.3512	0.7557

k_{23}	k_{34}	k_{45}	k_{56}
0.2319	0.7866	0.4525	0.4836

and Fig. 3 shows their conventional positions in the basic filter circuit.

At this point it is necessary to assign values to L_N and C_N, the parallel resonant circuit nodal reactances. There are two main considerations governing their selection: the practical convenience and economy of preferred values; and the need to obtain reasonable values of Q in the gyrator elements which will simulate $L_{N1}-L_{N6}$.

The gyrator circuit employs four resistors, one capacitor and two operational amplifiers contained in a common package, and its effect in this application is to "rotate" the reactance of the capacitor, C_g, by 180°, to appear as an equivalent inductive reactance at its output terminals.

Considering (b) first, provided all resistors (R) in the gyrator are made equal, then the simulated inductance $L_g = R^2C_g$, and for maximum Q the reactance of C_g should equal R. In the practical case, only an approximate equivalence is necessary to achieve good Q values and trial calculations show that if C_N is arbitrarily made 8200pF, then L_N, (and hence L_g) must be

$$\frac{1}{F_m{}^2 4\pi^2 C_N} = 1.695\text{H}$$

If C_g is arbitrarily made 10,000pF, then $R=\sqrt{1.695/(10000\text{-}12)}$ = 13019Ω, allowing the preferred value of 13kΩ to be used in the gyrators, which also gives reasonable correspondence with the reactance of C_g at F_m, 11.8kΩ. Note that one resistor in each gyrator circuit will be variable to permit exact adjustment of resonant circuits when tuning the filter.

The inter-section coupling elements, $k_{12}-k_{56}$, can now be de-normalized and replaced by C_{12} – C_{56}, respectively. Two-percent polystyrene capacitors should be used in these positions, if necessary made up from series or parallel combination of preferred values. Five-per-cent polystyrene capacitors are adequate for $C_{N1}-C_{N6}$ positions and the largest physical size that can be accommodated should be used in the interests of long-term stability.

It is worth making a practical point here. Be warned that polystyrene capacitors are prone to develop short circuits during the soldering process, particularly if very short axial lead lengths are used; it is therefore advisable to use temporary heatshunt grippers when making connection.

Denormalizing

$$C_{12}=\frac{BW\times C_N}{F_m}k_{12}=\frac{110\times 8200^{-12}}{1350}\times k_{12}=$$

$$6.66815^{-10}\times k_{12} \quad =505\text{pF}$$

$$C_{23}=6.6815^{-10}\times k_{23}=155\text{pF}$$
$$C_{34}=6.6815^{-10}\times k_{34}=527\text{pF}$$
$$C_{45}=6.6815^{-10}\times k_{45}=303\text{pF}$$
$$C_{56}=6.6815^{-10}\times k_{56}=324\text{pF}$$

Input and output resistance

Source and load resistances for the input and output sections of the filter must first be obtained using q_1 and q_6 values from the table in reference 1.

$$Q_1=\frac{F_M}{BW}\cdot q_1=\frac{1350}{110}\times 1.8774=23.04$$

$$R_{SOURCE}(R_s) = \omega LQ_1=2\pi\,1350\times 1.695\times 23.04=330\text{k}$$

$$Q_6=\frac{F_M}{BW}\cdot q_6=\frac{1350}{110}\times 1.3512=16.582$$

$$R_{LOAD}\,(R_L)=\frac{Q_6}{Q_1}\cdot R_S=\frac{16.582}{23.04}\times 330000=240\text{k}$$

Input resistance

This is specified as 600Ω and can be matched to R_{source} by capacitively tapping C_{N1} in the first resonant circuit (Fig.4);

$$C_1=C_N\sqrt{\frac{R_s}{R_1}}=8200\sqrt{\frac{330000}{600}}=192388\text{pF}$$

$$C_2=\frac{C_1}{\sqrt{\frac{R_s}{R_1}-1}}=\frac{192388}{\sqrt{\frac{330000}{600}}}-1=8565\text{pF}.$$

Output resistance

In a similar manner, R_L can be matched to the required 600Ω (Fig.5);

$$C_1=C_N\sqrt{\frac{R_L}{R_2}}=8200\sqrt{\frac{240000}{600}}164000\text{pF}$$

$$C_2=\frac{C_1}{\sqrt{\frac{R_L}{R_2}-1}}=\frac{164000}{\sqrt{\frac{240000}{600}-1}}=8632\text{pF}.$$

Polycarbonate capacitors of 20% tolerance are adequate for C_1 positions at input/output ports; polyester dielectrics should be avoided due to their comparatively inferior loss factors at higher audio frequencies. An alternative output arrangement, shown in Fig. 6, is convenient if a spare amplifier can be used as a voltage follower, reducing filter insertion loss.

The circuit of the filter, prior to substitution of gyrators for inductors, is shown in Fig. 7. Each nodal inductor, L_N in Fig. 7, will now be replaced by a grounded negative-impedance converter (gyrator) based on the Antoniou circuit (Ref. 3) and the principal merit of the procedure will now be appreciated; it is not necessary to wind six high-Q inductors, each 1.695 henries, to realise the filter in its practical form.

GYRATOR OPERATIONAL AMPLIFIER

The choice of op-amp for use in the gyrator is not critical, provided both amplifiers associated with each gyrator are in the same package, since phase tracking *is* important. The industry standard type 4136 is perfectly adequate and most other commonly available types will do; i.cs can also be used but do not offer any particular advantage. Quad packaging is suitable and convenient since pairs can be used for adjacent sections of the filter without interaction.

The values for R and C in the gyrator have been previously arrived at (13kΩ and 10,000pF) and Fig. 8 shows its complete circuit. The stability of the simulated inductance is practically independent of the op-amp characteristics, but heavily dependent on the long-term stability of R and C_g, since $L_g = R^2C_g$. Metal-oxide and polystyrene types are suitable, of 2% and 5% respectively, and for the reason previously mentioned, the largest physical sizes that can be accommodated should be used. Resistances R_a, R_b and R_c combine to approximate R at the mid-adjustment position of R_c, allowing individual inductance trimming when each section of the filter is resonated during the tune-up procedure. The complete circuit, including gyrator for inductor substitution is shown in Fig.9.

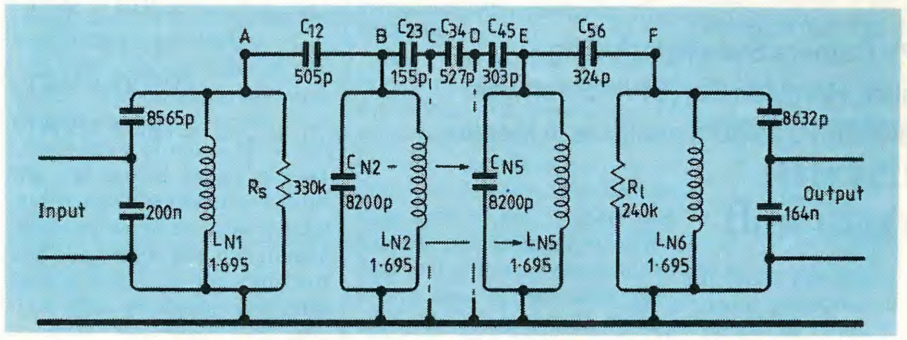


Fig.7. Circuit of filter, using calculated values of inductor to be replaced by gyrators.

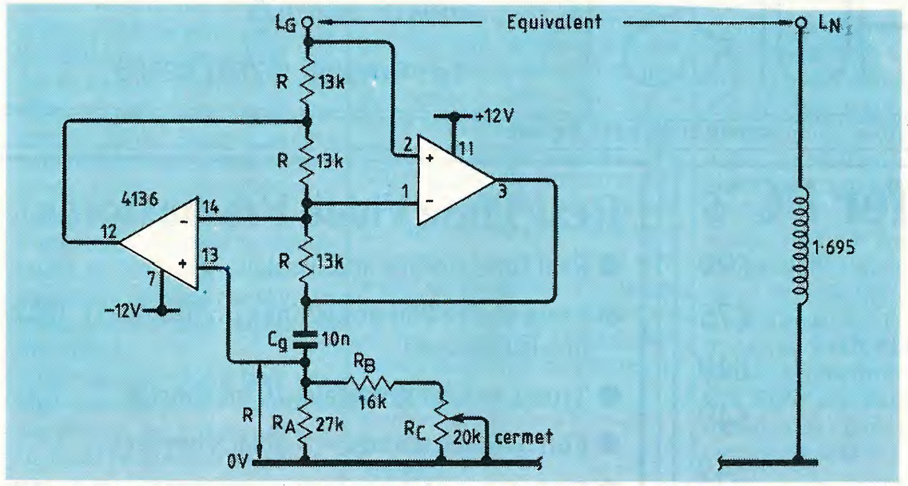


Fig.8. Circuit of gyrator, equivalent to an inductor of 1.695H.

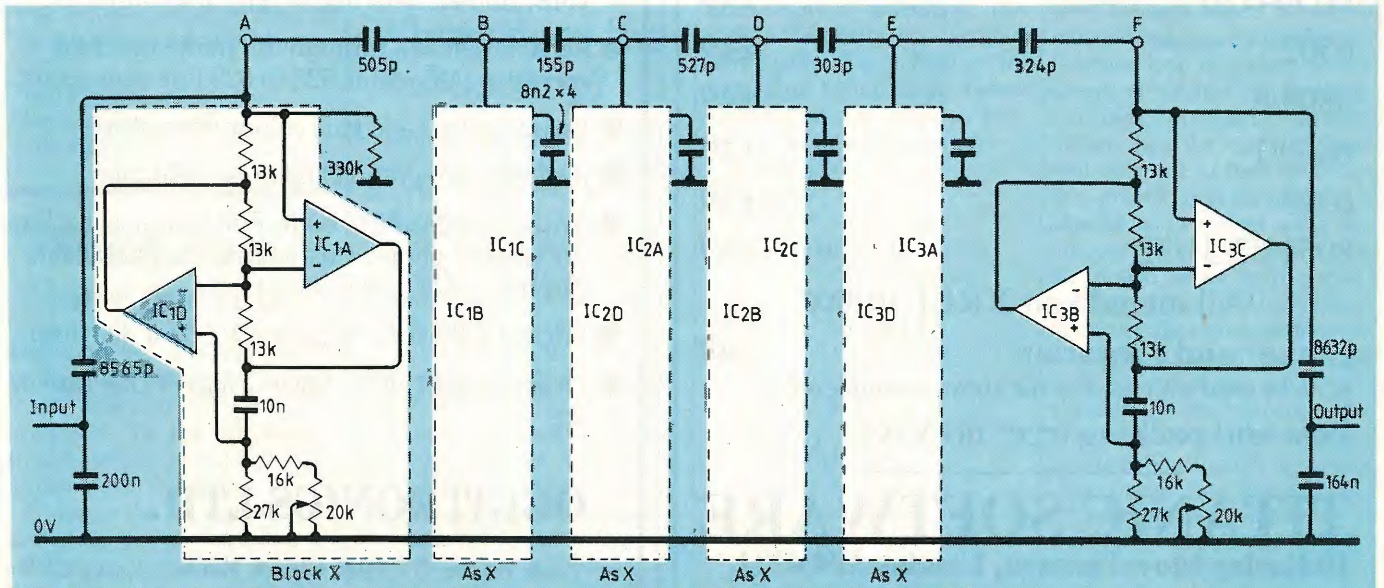


Fig.9. Complete final circuit of filter, using gyrators.

FILTER TUNING

Referring to Fig.9, apply an 0.5V pk-pk 1350Hz signal from a 600Ω source to the filter input. Earth points B, C, D, E and F. Connect an a.c. v.t.v.m. via 56pF to A and tune L_{g1} cermet for maximum indication. Check for correct damping on the input stage by measuring the 3dB bandwidth, 1350 ± 55Hz – if necessary adjust R_s to obtain it.

Leaving the meter at A, unground B and adjust L_{g2} cermet for minimum indication. Unground C, D, E and F in turn, obtaining max., min., max., min. in that order, as L_{g3} to L_{g6} cermets are trimmed sequentially. Ground E and transfer the meter via its 56pF series capacitor to F. Transfer the input signal to the output terminal of the filter and again check for the required 3dB bandwidth at F, adjusting R_L as necessary.

Remove all earths and with source and load resistances of 600Ω check the overall filter response, which should approximate that of Fig. 11.

Excessive passband ripple can be reduced by lightly damping the internal filter nodes (points B, C, D, E) with, typically, 1MΩ resistors.

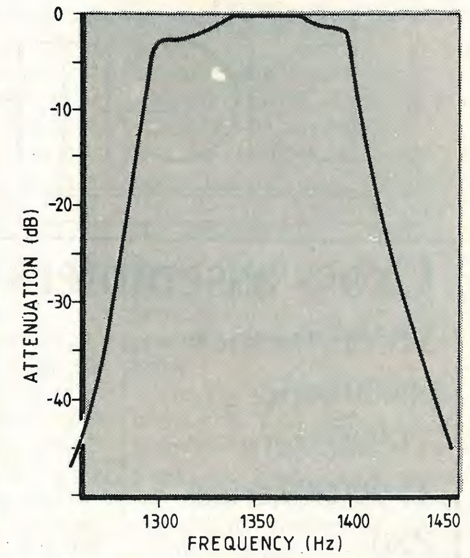


Fig.10. Steady-state response of filter.

References:

1. Zverev, Anatol. I., Handbook of Filter Synthesis, John Wiley & Sons new York 1967.
2. Lynch. T.H., The Strength of LC Filters, *Electronics* July 21st, 1977 – p116.
3. Antoniou. A., "Modelling of a Gyrator Circuit", *IEEE Trans. Circuit Theory*, Vol CT-20 No.5 pp. 533-540, September 1973.

FEEDBACK

Marx generator

I just finished reading the recent article entitled "Marx Generator for High Voltage Experiments". It brought back memories of my construction of a Van deGraff based linear accelerator in high school during the early 1960's. I have thought of a possible solution to the problem of smoothing the aluminium foil inside the plastic drain pipe to form the high voltage capacitors.

If one were to take an old bicycle inner tube and cut it such that the valve were located close to one end (but not so close that the end cannot be folded over and clamped between two short pieces of wood to make a seal) and the length was determined by the length of the capacitor tube plus an appropriate extra length to be clamped off. The aluminium foil could be coiled loosely around the inner tube, inserted into the pipe, the end of the inner tube clamped off, and the inner tube expanded slowly using a hand air pump. If one were to lightly spray a contact cement or clear acrylic artists spray into the plastic tube before this operation is undertaken, the aluminium foil would be tightly sealed to the inside circumference of the tube and not likely to cause problems with bubbles or sharp points.

One question I did have was what constitutes thin-wall plastics pipe in Dr Richley's mind, i.e. could he specify a wall thickness. Also has he tried c.p.v..c (chlorinated poly-vinyl chloride) pipe as that is easiest to obtain at the plumbing supply in Minnesota?

Brad Phillips
Bloomington
Minnesota

Short arms, long pockets

The report "Mobile radio update" in your July issue truly establishes piracy as a respectable profession in the spectrum. Irresponsibility prancing naked on communal resource.

Through the familiar shallow subterfuge of arms length consultancy – such short arms – there lies this specious attempt to blur the issue, shift responsibility and arbiter away the plunder to the Frequency Pillaging Organisations (FPO's). Our very own public jacks-in-office pandering to and platforming with them, commissioning (God knows what sort of alleged) consultancy expertise (how *do* you patent the universe?) to varnish over the rough and the ready. To lift from the ether a million or two a meg, melt down the corpse, discard the dross and fence the plate.

Just one of the glittering opportunities overlooked was the public self immolation of those functionaries left without function. No function, no job, no pay...? (how many kids can we sack today?). But I expect that having relinquished function they will still have the grace to attend office in ceremonial robes and add yet another hereditary layer to our national pageant of discards.

Come, Minister, whoever you are, be bold, positive, serious, decisive, enterprising. Drop into the public pocket – so deep – those benefits that accrue from this spectral leap forward. The 500 staff, the 40 computers, the vehicle fleets, the £20 million p.a. After all, they have abdicated responsibility and publicly confessed shortcomings. The bright new Cayman man management of the spectrum (FPO's) will surely need this corporate experience?

Yours (with the black eyepatch)
D E Kershaw
Blackpool

Where does the bus stop?

Replying to the leter from L. J. Silver in *EWW* May 1987, the material I have published on this matter is as follows:

1. Catt, Walton and Davidson, Digital Electronic Design Vol.1. pp.87 et seq., pub. C.A.M. Publishing 1978.
2. I Catt, Death of Electric Current, pp.23 et seq., pub. C.A.M. Publishing 1987.

Some of the this material was previously printed in *Wireless World.* The above should also be reference material in the Hardie-Hayward-Morris discussion currently under way in Feedback.

Paul Borrill is one of the (possibly few) people in the "Standards generating sub-culture", possibly a very limited, exclusive group, who fully understands all the relevant factors. When I last looked at the situation, he was having a hard fight against the knuckle-heads, but that was some years ago. Speaking more generally, you get what you pay for. Our industry does not remunerate the people who put effort into the generation of standards, and so it gets the rotten standards that it deserves.

Ivor Catt
St. Albans.

Attractive flow diagrams

If David Sweeney comes across many programs like the little sample he offers, I am not surprised that he is driven to devise improved flow diagrams! I know plenty of programmers, and not one of them finds flow diagrams to be of any use in coding; disciplined top-down structured programming with good style will do far more for you. (1) Don't clutter the code with redundant BEGIN ENDs. (2) Use spaces to make it like English, not Bequals9 (B:=9;) but B equals 9 (B := 9;). (3) Use indenting to show the structure of loops and branches; THEN ELSE are completely symmetrical (as are BEGIN END) and must be equally indented. (4) Link pairs by tiny comments; ELSE { a } belongs to THEN { a }, not to THEN { B }. (5) Put Boolean expressions in brackets in IF statements; this makes for clarity just as good punctuation does in English. (6) Get rid of typing errors before anyone else sees what you have done – not C:I+B/5. So we get

```
IF (B > 27)
   THEN { a }
      IF (I < 50)
         THEN { b }
            CALCYVAL (Q)
         ELSE { b }
            BEGIN { 1 }
               B := 9;
               I := 5
            END { 1 }
   ELSE { a }
      BEGIN { 2 }
         B := B + 1;
         C := I + B/5;
         X := B * 7;
         CALCXFACT (X)
      END { 2 }
```

There ought to be a few comments, because identifiers like B and I give no hint of their meanings. In general, never skimp the source code. Spreading yourself may use up a little extra dirt cheap space on a floppy, but it will save time in debugging and in maintenance by someone else, and it will not enlarge the object code which resides in expensive ram. By choosing a sufficiently, unrealistically bad example of source code you can always make a flow diagram look attractive!

J. G. D. Pratt
West Horsley
Surrey

Class B crossover distortion

I would like to thank Mr Sage for showing interest in my work. While he was correct about the Blomley circuit it can be easily shown that my circuit works just the other way round. I understand that Mr Sage is capable to analyse this without my help if only he would care to give it a second glance, but for other readers a few words might be in order.

The main problem in traditional class B as well as in Mr Blomley's circuit is that at crossover one transistor is being switched off while the other that was off is too slow to be switched on immediately, therefore a situation exists when both devices through which the signal must propagate are off and so the feedback loop is broken. In my circuit all devices are active at crossover. At output currents higher than the quiescent current only one of the transistors that provide bias compliance is allowed to switch off while the other stays on. This means that the region where both transistors are active is overlapping! Moreover, the signal needs not to propagate through the closed transistor as it has a free path through the base resistor to the base of the output device which is active. So although my circuit diagramme looks much like Blomley's, functionally it is much more like the one of Tanaka (see ref. 12 of my article).

Now the output devices are not necessarily of the Blomley

FEEDBACK

compound type. I was using those mainly to prevent other distortion mechanisms to be confused with crossover distortion behaviour. Also, please note that transistors shown in the shaded area in my circuit idea (October 1985) are not part of the compound stage in the Blomley sense! Their function is solely to provide compliance to the bias voltage, and once you have succeeded in configuring the output device as a constant current source when the other device is handling the load you have all the compliance you need (as clearly demonstrated in Fig. 7 of my article).

What I was trying to say with my article was that small cross-over spikes might not be so harmful by themselves, as they carry most of the energy at and beyond the upper limit of the audio band. A more serious problem could be the phase error produced as a consequence of crossover distortion, so it just might show up that an equivalent solution would be a switching system with the phase error removed in some way.

If you still insist in disliking the switching-off action of my circuit there is a simple way to avoid it but I do not see any sense in such complication as I was unable to detect any spikes in its performance (Figs 9 & 10) Thus I will continue to believe the circuit to be a successful solution for crossover distortion, but I would be grateful to Mr. Sage to inform me what other errors I have committed.

Erik Margan
Ljubljana
Yugoslavia

Design in isolation

The letter from F. B. Kyle (*EWW* August), refers to designers concerning themselves "only with the functioning of equipment in isolation", and quotes the Viceroy switchboard system as an example.

This strikes a particular chord with me, because whilst Mr Kyle observed that the Viceroy radiates nasty r.f. interference, I have had the converse problem of such switchboard systems failing to operate in my company environment.

We sell and service a great deal of h.f. communications equipment, and therefore on occasions radiate modest amounts of r.f. from external aerials. The power levels involved range from 100W to a maximum of 1kW, on frequencies between 3 and 30MHz.

I have yet to find a single so-called "smart" internal telephone system which will carry on working in the r.f. fields generated, and despite several assurances from sales engineers (BT and others), I have to continue to use a simple old fashioned key-operated switchboard, because r.f. doesn't stop it working.

"Design in isolation"; I couldn't agree more.

John Wilson
Lowe Electronics

What has happened to clock chips?

During the 1970s, semiconductor manufacturers were almost falling over themselves to produce increasingly sophisticated clock chips, and new ones were constantly appearing. Now they all seem to have disappeared. Although some markets are ephemeral, created by an artificial demand, I can't really see that clocks and timing devices belong in this group. We still need to tell the time, and most people still (or increasingly) want to be able to switch devices on and off. I wonder, therefore, whether you can say anything of what clock chips are available now? Are there any that equal, or preferably better, the facilities of, say, the CT 7001 clock or the MM 57160 timer?

(What I am looking for, in fact, is some means of producing a timer to switch at least four outputs, as the MM 57160, but at definitely more than four times a day.)

I wonder, too, while on the subject, whether you can provide any help in tracing a replacement CT 7001 chip? I have had one in use for several years, but one display segment and the alarm have now failed, and I haven't been able to find anyone who still supplies it. Do you know of any supplier, either in this country or, presumably, in the US of A? Or is there any pin-for-pin replacement for it?

Neil Muir
Shrewsbury

Maxwell's e.m. theory revisited

In his article in July, 'Joules Watt' paraphrased 'The Structure of Scientific Revolutions' by T.S. Kuhn as follows;

> "Yet the developed theory of electromagnetism still holds sway. If there are some phenomena such a theory does not explain, then any new model must explain all that has gone before – plus the new aspects. At least that is the way Thomas Kuhn outlined the situation."

Kuhn's message is diametrically opposed to the above, as I plan to demonstrate with excerpts from his book in a future article. Meanwhile, it would be useful if 'Joules Watt' were to confirm that he is in fact stating Bohr's Correspondence Principle (see Electromagnetic Theory Vol 2 by I Catt, C.A.M. Publishing, p295), and not Kuhn. (See entry "Correspondence principle", Dictionary of the History of Science, 1981, page 83.)

Ivor Catt
St. Albans

Real & imaginary

In his September article 'Real Thoughts on the Imaginary Axis' dealing with complex numbers 'Joules Watt' presents them in a way that would have been perfectly familiar to mathematicians of a century ago. However mathematics, like electrical engineering, has moved on since then, and today they are better introduced simply as ordered pairs of real numbers, written (a,b) instead of a+jb. The product of (a,b) and (c,d) is *defined* as (ac-bd, ad+bc), so that complex numbers obey the commutative rule which says that

$$(a,b)\,(c,d) = (c,d)\,(a,b)$$

as well as all the other rules of algebra. Thus they can be used wherever real numbers are used, for example as coefficients in a quadratic equation, or even as coordinates in coordinate geometry. In addition a complex number of the form (a,0) behaves in almost all respects like the ordinary number 'a'.

In this way the main difficulty of the older presentation is avoided. The ordinary number –1 has *no* square root, despite repeated statements to the contrary, but the number pair (–1,0), which in most respects behaves like it, has the square root (0,1). In calculations (0,1) shows all the properties normally attributed to 'j'.

Joules Watt mentions the development of vector analysis in the latter half of the last century, and its imporatance in electromagnetic theory. Now vector algebra is defective, since the definition in three dimensions of a 'vector product' of two vectors mysteriously fails to yield a 'vector ratio'. In the more general tensor calculus, vectors appear as a particular kind of tensor of rank one. Between tensors two kinds of products, 'inner' and 'outer', are defined, and both generalise to spaces of higher dimension. The first applied to two vectors gives the familiar scalar product. The second applied to two vectors gives a tensor of rank two, with skew-symmetric components. In three dimensions this product has three independent components, so that it is just possible to regard it as representing a vector. The divergence operator applied to a vector gives a quantity which behaves like an inner product, while the curl operator gives a quantity which behaves like an outer product. Since Relativity deals with four dimensions rather than three it almost has to be expressed in terms of tensors and tensor operators rather than vectors and vector operators.

Electronic engineers do not expect to make do with the electronic techniques of even twenty years ago. Why should some be content to ignore developments in mathematics over the last century?

C F Coleman
Grove
Oxfordshire

Fifth generation

As the UK's Alvey programme draws to a close its retiring director analyses recent progress, identifying both strengths and weaknesses as well as looking to the future

BY BRIAN OAKLEY

We look at the technical progress, the quality of co-operation, the drive and quality of plans for exploitation and the quality of the project management of the Alvey programme. We also look at the quality of our monitoring officers, which turned out to be almost universally good.

In general the technical progress appeared good and much more encouraging this year, perhaps primarily because recruitment difficulties are largely overcome, and co-operative teams have settled down and learnt how to work together. It is dangerous to generalise of course and there are some significant differences in the progress of projects in those subject areas analysed in this article.

There have been wide variations in the quality of co-operation, with in general a very encouraging picture emerging. Perhaps not surprisingly at this stage, there are a considerable number of projects where progress is described as good, very good, or even exceptionally good between all partners, but there are also a number of projects where co-operation is described as weak or even bad, with usually only one partner seeming to be the black sheep.

Looking at the assessment by the monitoring officer it is clear that there is a significant correlation between management performance and technical progress. This is hardly surprising, but perhaps it is less to be expected that there is a strong correlation between the performance of the project management and the quality of the co-operation and collaboration. A good project manager seems to be an essential element in a good co-operative project, and the reverse very often seems to be true too. When we started four years ago there was very real doubt if good collaboration could be achieved. There can now be absolutely no doubt that good collaboration can be and has been achieved.

But there is a price to pay, both in terms of the overhead in learning to work together, in travel time, in report writing, in frustration over collaboration agreements, and above all in the quality required of the individual manager and the effort that has to be put into management. Virtually all project teams agree that this overhead is amply repaid by the benefits of collaboration. One clear lesson of this type of dispersed collaboration that emerges from the programme is that it needs good management. But then what successful project does not?

The Alvey Committee referred to the programme that it proposed as one of pre-competitive R&D. I'm not sure if I have ever really understood what that means, and have described it previously as "anything on which teams are prepared to co-operate". However, I have come to recognise during the past year that the term has its dangers, as it seems to be related in some people's mind with research that has no useful end product. Such people tend to refer to the programme as one of academic research, where the term "academic" clearly is intended to have pejorative overtones, associating "academic" clearly with "useless" or at best of too long term in nature to have any economic benefit to the nation.

I am pleased to say that this is far from the truth as time and experience has shown. Even in the early days we were concerned to select projects where the potential exploitable product or process was clearly visible and where the route to exploitation was clear. The reason the Directorate insisted on collaborative agreements was because we believed that drawing up these agreements clarified the management and exploitation responsibilities and so focused attention on what was, after all, the purpose of the work – in the long run something of the nations, the participating bodies, and the individuals directly involved.

We have just published a brochure that sets out in brief the exploitation plans for some 90 of our projects. This does not mean that nothing of benefit is coming out of the other half of the programme. Those projects may have started later, may be producing vital new knowledge that it is premature to exploit but that will lead to products in the next programme. Some of the products and processes thar are outlined in the brochure are already on the market or in service in the firms involved. All have outlined something of economic benefit with clearly identified plans for bringing that to fruition in the market in due time.

It must be remembered that most projects are only half-way through, and many have two or more years yet to run. Though some products can come to the market close on the heels of the project prototypes, and especially with software the step from innovative work in the programme projects to packages on the market can be short, in most cases the projects will be followed by a development stage where the firms are likely to have to expend considerably more than in the "pre-competitive" R&D stage.

So in general we are very pleased with the exploitation plans of the companies and with the successes that have already been achieved. One has only to look at the brochure, or have visited our exhibition where the work of over 100 projects was on display* – often with working prototypes in use – to appreciate that the work of the programme is being exploited. But I would be less than honest if I did not sound one general note of warning. Almost everywhere I look amongst our projects I find exploitation plans that look in some danger of frustration, not through lack of drive or will to bring the end product to the market place, but through lack of financial investment to ensure success.

All firms have to be selective about what they back. Real success in the market place requires considerable investment, not least to tackle the US and other overseas markets early and with vigour. It is the difficulty we often face in carrying through our exploitation on a large enough scale that encourages me to believe that programmes like Esprit, Race, and Eureka which bring together the talent, investment, and markets of Europe are very important for us as we face the scale of the industrial investment that can be made by the US and Japanese industries. However, having indulged in that piece of pontification, let me return to the theme that Alvey projects are producing products and processes that are being, and will be, exploited with real commercial benefit to the firms and all those involved, and to the nation as a whole.

A few are highlighted on pages 1140/5.

VLSI

From the monitoring officers' reports it would seem that progress in the v.l.s.i. field, taken as a whole, has been very satisfactory, and better than in other sectors of the programme. This may be deceptive because the targets have tended to be of rather shorter term nature than in other sectors, and the subject is, in many ways, more mature. Nevertheless it is very encouraging that technical targets are largely being met and that work is resulting in projects and processes that in some cases have already appeared on the market or entered service.

The v.l.s.i. instrument industry is proving very impressive, in its relatively small and fragmented way. In particular this is a field where the excellence of our University techniques work, developed in aid of basic physics, has proved of very considerable value in helping the instrument industry to tackle the highly sophisticated equipment required to support the fabrication of sub-micron v.l.s.i.

With our last major cad project we have brought almost all the players in the UK v.l.s.i. cad industry together in a concerted attack. This is not the development of a single system because the previous investment by the individual players, and the somewhat different design rules for the different processes precludes this. But it does harmonise the work, ensuring common interfaces and the use of common standards, which is very much in the interest of the users. If we can continue to make a co-ordinated drive on cad development this should prove of great value to our users as well as to our fabrication industry. The common development and use of standards, for example in specification languages like Ella out of RSRE, has been one of the bright stars in the whole programme.

In technical terms, it seems that our position is not significantly behind that of our major competitors abroad. And in some fields such as analogue bipolar circuits, and niche markets such as silicon-on-sapphire we may actually be up with the hunt or even ahead. But it is when one comes to look at the investments that are being made by our competitors that one wonders whether our current position can be sustained where it matters in the market place, despite the large investments by UK standards that are being made by some of the UK firms. This is not the time and place to enlarge on this, but looking to the future considerations of our market position leads me to believe that

- the industry has reached the point in co-operation where the basic technology work should be largely carried out on a shared or pooled basis
- whole process development should no longer be supported by public funds except on a basis that would lead to shared investment in production. This suggests the field should be left to Esprit and Eureka.
- support that brings the advanced basic work in the Universities to bear on the future developments of the instrument industry should be encouraged, though there must be some concern at the financial backing of that excellent set of relatively small firms.
- considerably increased support should be put into the cad developments, with specific attention being given to bringing to bear advanced software engineering techniques and personnel.

SOFTWARE ENGINEERING

In some ways the software engineering part of the programme is relatively disappointing. There are fewer projects with good progress, more projects with weak progress than in other parts of the programme. To some extent this is because we judge our software engineering work by world standards, where we know we are at or near the front, which may not be so true for say, v.l.s.i. And one must remember that co-operation is entirely a new phenomenon for this relatively new industry, so the programme had to bring about partnerships from scratch. One of the best features of the scene is the excellent co-operation that has developed between our outstanding academic community and industry, of which the highlight is the progress in bringing 'formal methods' from the academic world into use in industry and commerce. When the history books come to be written this may well be seen as the outstanding contribution to the UK economy of the whole Alvey programme.

The tool set work has developed well, and it will be interesting to see what impact these have on the market at home and overseas. An excellent co-operation has gradually built up with Esprit and the use of the emerging European standard, PCTE, must be seen as one of the key developments in recent years. It has come as something of a shock to our friends in the USA to find Europe uniting behind a more advanced standard than has yet appeared in the US scene. This is a measure of the advantage of co-operation, engendered and encouraged by programmes like Esprit and Alvey.

Looking to the future emphasis needs to be placed on getting the techniques of software engineering widely adopted wherever software is written in the UK. This requires a national drive on awareness and training. I am not suggesting that continued research work is not required in fields like formal methods, but the emphasis now needs to be turned on getting the techniques widely used. We now have the means at our disposal of improving the quality, productivity, and the rate of production of our software, but it will require a determined and concerted effort to get the techniques widely used. On future developments, I would place renewed emphasis on reusability and metrics, and despite our intentions neither subject has made much progress in the Alvey programme. Yet the two related subjects would handsomely repay increased high-quality effort. In looking at our progress in software engineering it is important to remember that the goals and priorities of the Alvey software engineering programme have been widely adopted and emulated throughout the world. To copy is to flatter.

KNOWLEDGE-BASED SYSTEMS

In the i.k.b.s. field we started with a high quality but thin academic community, and very little manpower and experience in industry. So we can claim that one of the achievements of the Alvey programme has been very considerably to increase the pool of people who are expert in the techniques of i.k.b.s. both in the academic world and industry. The academic teams have been overwhelmed by the demands from industry, and it is most encouraging to see that this co-operation has led to the widespread establishment of teams in the major firms, and the emergence of a rack of new expert firms.

The expert systems awareness part of the programme has been a great success. Some 200 firms, in all walks of commercial and industrial life have taken part in the expert system community clubs, and so learnt about the capabilities, problems, and techniques of expert systems. One measure of the success is that, so far, five of our nine expert system clubs have taken the decision to continue on to produce commercial products with entirely their own private funding. And within the rest of the i.k.b.s. programme 20 or more expert systems are being developed, of which the work of the ICL large demonstrator in applying the techniques to the problems of the administration of the social security regulations in the DHSS deserves special mention. It is probably no exaggeration to say that the UK in general now knows more about, and is doing more about, the application of expert systems than anywhere else in the world outside the USA.

The logic programming initiative is a good example of a concentration of attention on a facet of work that was previously the domain of a rather small school of academics. It is too early to say what will emerge from this, but if we were right to select this area for priority attention, as of course I believe we were, then the rewards should emerge in due course. But I would raise one note of caution. It is no use developing techniques and programmes unless the packages get widely adopted. And unless our software industry can mount a determined attack overseas, especially in the USA, much of the benefit of the work to our i.t. industry will be lost, as distinct from the benefit to those in the UK who adopt the techniques.

For the future I would not keep i.k.b.s., or a.i., as a single subject. One of the encouraging features of the past year is that the convergence of the software engineers with the i.k.b.s. community has accelerated, and I would encourage that by handling the two subjects as one for strategy making and administrative purposes. I would continue to support some of the less developed techniques of i.k.b.s., such as rule induction, but I would reduce the awareness campaign for expert systems while continuing to support some of the pioneering applications that help to pull through the techniques from the academic community.

One field that I consider deserves special attention in a future programme is that of natural language. The eventual applications of the subject are so wide that one can envisage a major industry evolving, for the conquest of natural language processing will give computers the power to understand meaning, not just to recognise words. There are aspects of the subject like adaptive dialogues that show promise of short-term applicability. But in general it is a very difficult subject and not one that is likely to be solved in the short term. For excellence, it is an example of a subject that demands a multidisciplinary approach and by that I embrace linguistics and lexicographers, philosophers and psychologists, as well as logicians, computer scientists, and mathematicians. It is one of the few subjects in the i.t. field that really would benefit from concentration primarily in a very few, one or at the most two, largish centres of excellence.

SYSTEMS ARCHITECTURE

It was a mistake not to recognise systems architecture as a subject in its own right from the beginning, though we did correct this in the second year. The work in the UK in this field is excellent, especially in the academic world, and the Alvey programme has served to pull the academic work through to the i.t. industry. Co-operation between industry and the academic world has gone very well: co-operation between firms is not a key feature of this part of the programme, though the co-operation in projects like Ansa, Dactyl, Parlog and Parsifal contradict this. In the short term the problem is to take the standards projects on to the European and world scenes. In the long run, the co-operation of the firms of the UK and beyond in Ansa may be seen to be one of the seminal features of the Alvey programme for the i.t. industry.

This is one area of the programme where much remains to be done to take the work from the prototype stage through to commercial application. There can be no question that parallel architectures are going to become very important in the future. In some parts of the systems architecture programme, continuing public support, perhaps on a European basis through Esprit and Eureka, will be required if Europe is to remain a key player. In a sense what is now needed is the spur of development for, and use in, the market to feed back to what remains a major problem for academic attention if means of using parallel architectures efficiently and easily are to be developed. I would especially concentrate in the future on the systems, software, and standards aspects of architectures.

MAN-MACHINE INTERFACE

It was a mistake to gather together under the man-machine interface heading topics that do not have all that much in common, when some parts of the subject have much in common with other parts of the programme. The speech part of the programme has brought the limited effort in the UK together, which must be welcomed. The market in relatively limited-vocabulary, limited-domain speech recognition is now developing, but there is still much to be done before the error rates in connected-dialogue, unlimited-domain speech recognition systems become acceptable. This will require considerable progresss in natural language work. For the future I would reduce the effort on front-end signal processing, perhaps tackling the subject in future on a European basis, but would increase the effort on natural language processing.

Some of the best research work in the programe has been done in one or two of the image processing projects. This is an important subject, with a wide range of potential applications. I am not entirely convinced that it is a single coherent subject, but the subject deserves increased support in a future programme, perhaps with a concentration on pulling through the techniques to practical applications. I would look very critically at the variety of different 'front-end' architectures that are under study, probably playing down this aspect until application specific architectures can be developed.

One of the successes of the Alvey programme has been the attention it has drawn and the respectability it has given to the human interface in virtually all i.t. work. There is now much more awarenss of the importance of this subject. But I cannot say that the actual work on human interface in the projects has made much progress. Maybe it is too early to judge, but I do not see a coherent community of quality emerging, which knows what the priorities are and how to tackle them. For myself, I would insist that the human interface was tackled seriously wherever one appeared in any future programme.

In planning the future programme there is one theme largely missing from the Alvey programme, that I believe should feature in the future and that is security. Security of data, of transmission, of display is becoming a crucial topic and deserves priority.

ADMINISTRATION

It is the view of virtually all of us who have been involved in the Directorate that this process of having a team drawn from industry, the academic world, SERC, and the government departments, DTI and MoD has been a great success. We have all enjoyed the chance enormously, despite the hard work, long hours, and inevitably frustrations. We all believe that it would be right to continue this process, for we believe the Directorate has provided a focus, and to some extent a voice, for the i.t. community. We believe the time has come for someone from industry to lead the Directorate in the future.

The active participation of SERC and the academic community in the Directorate process and in the programme has been welcomed by one and all. In continuing, I hope this will be extended to more active participation in the Esprit programme and the focal point that the Directorate provides for the UK input to Esprit. It will be the responsibility of a future Directorate to try to co-ordinate Esprit II and the future Alvey programme to a great extent than we have been able to do, for the good of the UK i.t. community but also for the good of Europe as a whole.

The need for an emphasis on applications in a future programme will inevitably mean some changes in a future Directorate structure, with much greater co-ordination being required with the sponsor divisions of DTI and with other government departments. This will be a new challenge for my successor, which will require tact and forbearance – but also I believe leadership – not just on his part but also in the leaders of the divisions with whom he will work.

The part played by our Research Establishments in helping to administer, guide, and glue the programme together should not be ignored. I have particularly in mind RAL and RSRE, but others have also helped. The benefit of the expert in the neutral corner in a co-operative programme between commercial rivals is obvious. In the early days British Telecom also played an important part in this respect, but that of course has had to change, as their status has changed. I hope that the research establishments will continue to play this role in the future, but I should warn that that does require that their owners or primary sponsors have got to ensure that they are given the chance to keep their high quality people at the frontiers of their subjects.

It is true that the lion's share of the programme has been taken by the so-called large firms, which are themselves small on the international scale. But there are 115 firms in the programme, many of them small, and it is unlikely that the lions, the large firms, have an undue share, judged on the criterion of their share of the market. It would be ridiculous to ban hte large firms from the programme, for not only have they the large research teams, they also dominate the i.t. market in various fields. Without them, the v.l.s.i. and displays parts of the programme would hardly exist, and almost every other part of the programme would look ridiculous. This is not to say that small, high technology, firms have not played an important, indeed crucial part in the programme. In future I hope there will be someone on the Directorate, himself seconded from industry and preferably with small firm experience, who will have special responsibility for helping small firms to play their part in the programme, and to overcome the inevitable problems of dealing with the bureaucracy in the start up phase of a project. But we have to face the fact that our overseas competitors would be astonished and delighted if we kept our large firms out of the programme.

We can rightly claim that Alvey has played its small part in seeking to overcome manpower shortages in the advanced subjects. Indeed in some of the key new fields our actions in providing and encouraging the provision of distance learning material, journeyman schemes, research studentships, and fellowship has been crucial. But it has to be acknowledged that the Alvey programme, and programmes like it, will be wasted if adequate supplies of highgrade manpower are not maintained. The Alvey programme has played its part in improving the quality of the education and training provided by the universities and polytechnics, if only because the relevance of the teaching is much improved if the lecturer and tutor is exposed to the technical and economic affairs of industry on a day-to-day basis. But it is crucial that the supply of high quality trained manpower has to be kept up if the UK is to thrive.

I have always seen it as important that the Alvey Programme should be evaluated by teams of independent but informed people, experienced in the difficult task of evaluation. I am pleased to see the work of the teams from SPRIL at Sussex University and PREST at Manchester University growing in quality and authority as the programme continues. I should like to see the teams tempered with more people with direct experience in industry, both users and suppliers of i.t. And I feel that the evaluation teams in the UK have to learn to get their message over. It is no use if the evaluators learn the lessons from the Programme, but fail to make their voice heard in the community. So I hope that their work will continue in independence, growing in authority and in the success of their attempts to convey the lessons they uncover to those who have responsibility for improving things for the future. I believe we are setting an example not just in the UK but also throughout Europe in the thoroughness and independence of our evaluation work.

Brian Oakley is retiring director of the Alvey programme

Alvey showcase

A time-limited sampling of i.t.-related hardware projects seen recently in Manchester

Held at the University of Manchester Institute of Science and Technology last July, the 1987 Alvey conference had the aim of exposing the technology to potential users and exploiters. How successful it was at this is difficult to assess; it is easier to say that the concurrent exhibition was probably the largest collection of advanced high technology projects ever assembled in the UK. Here we are restricted to highlighting just a few of the 90 demonstrations, selected from the total of over 200 projects.

With a growth of 30% a year and sales of $3bn representing 13% of the total semiconductor market, application-specific i.cs are seen to be a key factor in redressing the imbalance in Britain's import/export of i.t. production. The £130 million Alvey v.l.s.i. programme was thus designed to give the UK local access to asic technology.

Its silicon fabrication processes are scheduled to mature in the late 1980's and access is being provided by a range of new cad tools designed to handle complexities of up to a million active devices. Two of the six v.l.s.i. whole processes are already in production – see table – but full exploitation is likely to require further investment by industry – Plessey's new 6in wafer fabrication plant at Roborough for the 1 and 1.5μm cmos processes is a case in point.

One of the first products from the programme results from the ultra high-speed bipolar technology project at Plessey's Caswell research centre. The new process, dubbed HE by Caswell, has produced devices with gate delays as low as 50ns, and a sample prescaler on display and working at the exhibition toggled at 6.4GHz.

The process for the test samples is quite different from that used in the 3GHz prescalers currently in production at Swindon and reported in July's issue (page 699). Those devices resulted from a first generation process using reversed-biased p-n junctions for isolation, whereas the new process is described as 'third-generation' (second generation refering to oxide isolation). The HE process combines trench-isolated dielectric infils with a double polysilicon deposition (one n, one p onto an epitaxial layer) and allows transistors to be made with very low collector size and hence Miller capacitance, as well as with lower base resistance and higher f_T.

The interim development on show used a 'relaxed' metallization of 5μm – the main object was to get the transistor right – but the final dimension of 3.5μm and of 1μm a feature size should allow both analogue and digital circuits to operate up to 11GHz. The process is believed to be unique in Europe, though Japanese researchers have also been reporting work in this area.

First production will be of interim 1.5μm devices, expected early next year and a range of s.s.i. products will be announced shortly comprising a high-speed limiter and comparator, latched converter, flip-flop, various gates, and gate array as well as dividers. But final spec. devices are expected to reach a chip complexity of 36,000 gates/cm² leading to a figure of merit over 400THz-gate/cm².

The new cmos processes listed in the table have already been demonstrated and evaluated at Caswell, and the 'intermediate' process of 1.5μm will be in production now at the new 6in wafer plant near Plymouth. Production of the final 1μ devices and analogue devices and similar element density is set for late next year.

STC's high density cmos devices went into production earlier this year making it the first Alvey project to bear fruit, described as a 'technology pathfinder' although stepping-stone devices based on 2μm feature size have been manufactured for two years for a variety of both standard and specific products.

The attraction of the 1.25μm process of course is the improved yield that accompanies the smaller chip area required. Then in 16K static ram, target access time for the part was set at 20ns, though the process is capable of 15ns, and engineers at STC were pretty pleased when they measured 12ns.

The other bipolar project, for Ferranti's c.d.i. process, has already brought 1.5μm gate arrays into pilot production; 1.2μm devices are set for next year, with 0.8μm for December 1989.

DISPLAY PROJECTS

The display programme claims significant advances toward replacing the c.r.t. with flat A4 panels. Though some progress had already been made in this direction by commercial developers, most notably overseas, the Alvey projects are aimed at high resolution displays, in colour. Present efforts do not support a high information density, nor are they fast enough for real-time video applications, and if they are there is invariably some snag – single-colour operation being the most common.

At GEC's Hirst Research Centre a new process and circuit architecture are demonstrated in a small but high definition display with 224 by 208 elements at 0.4mm pitch, though not yet in full colour. The approach uses the active matrix principle in which a thin-film transistor is associated with each element picture (so the display contains

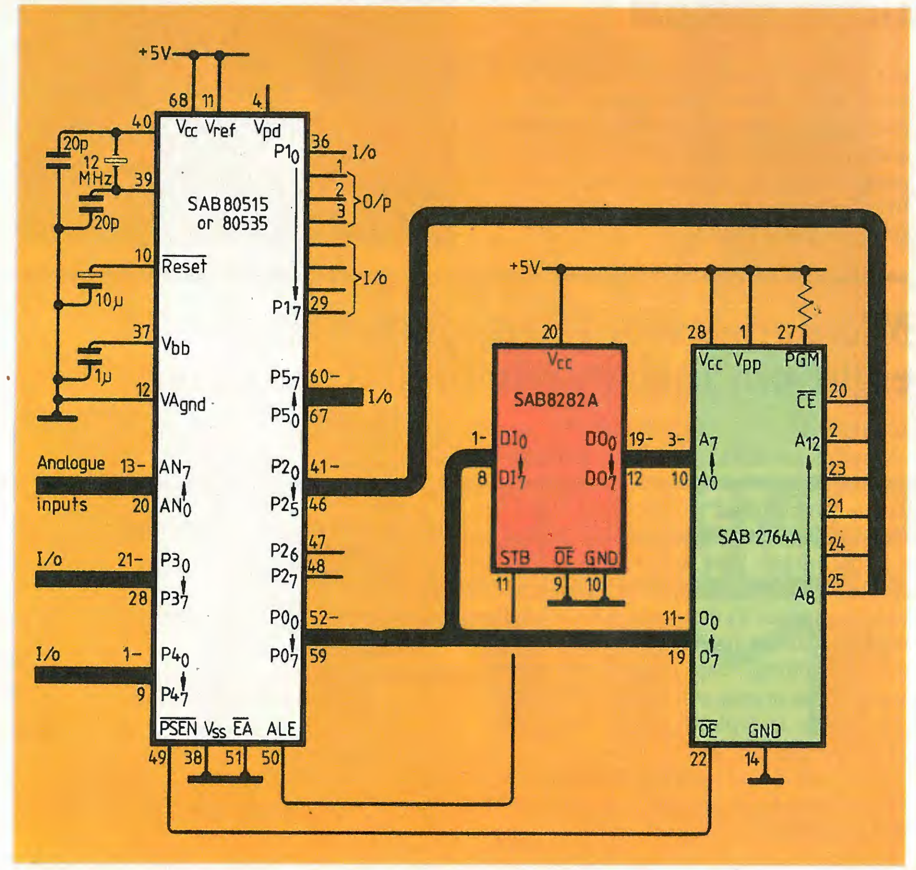
continued on page 1145

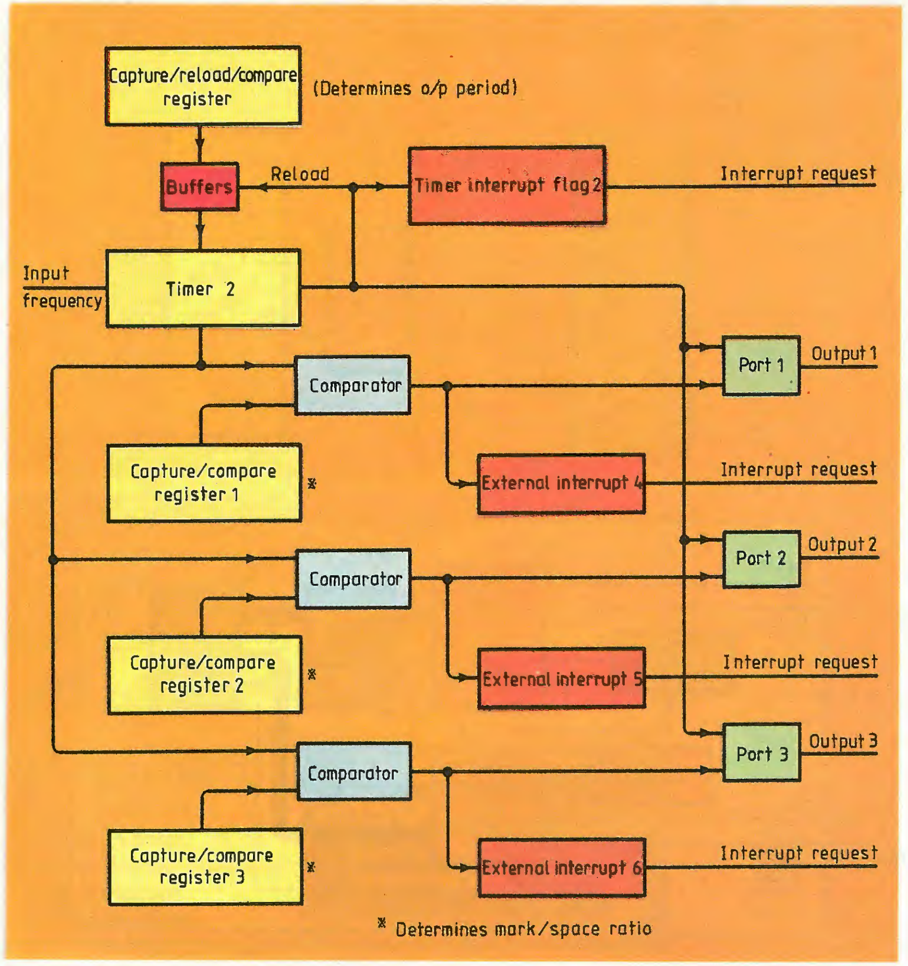
ALVEY VLSI PROCESS SUMMARY

Technology type		Bipolar CDI		UHS	Complementary m.o.s. Digital		Digital	Analogue		SOS*	
Participants		Ferranti		Plessey Southampton Oxford Univs	BA Racal STC		Plessey	GEC (MEDL) Plessey		GEC (MEDL) RSRE	
Minimum feature size (micron)		1.2	0.8	1.0	1.25	1.0	1.5	1.0	1.5	1.5	1.0
Maximum toggle frequency (MHz)		650	1200	11000	165	210	450	900	375	410	600
Effective circuit density (logic gates/cm²)		5×10^4	2.2×10^5	3.6×10^4	8×10^4	1×10^5	1.6×10^5	6.2×10^5	1.8×10^5	2.25×10^5	6.25×10^5
Figure of merit (gate Hz/cm²)		3.2×10^{13}	2.6×10^{14}	4×10^{14}	1.3×10^{13}	2.1×10^{13}	7.2×10^{13}	5.6×10^{14}	6.7×10^{13}	9.2×10^{13}	3.8×10^{14}
Availability	Prototype silicon	July 1987	July 1988	June 1987	Mar 1987	June 1988	Feb 1987	June 1988	Dec 1987	June 1988	July 1989
	Production	April 1988	Dec 1989	Oct 1987	July 1987	Dec 1988	Oct 1987	April 1989	Sept 1988	Mar 1989	Feb 1991

* Radiation sensitivity: transient upset = 10^2 rad/s

APPLICATIONS SUMMARY





Pulse-width modulation is widely used in microcontroller applications, particularly for motor driving. A common method of modulating pulse width is to use a timer and i/o line but this wastes processing time when the mark/space ratio remains constant for long periods because the timer needs to be constantly updated.

A Siemens note called 'pulse-width modulation using SAB80515' describes how capture and compare registers within the 80515 microcontroller provide more efficient p.w.m. During periods of constant pulse-width the timer is reloaded automatically from a 'capture/reload/compare' register and intervention by the c.p.u. is unnecessary.

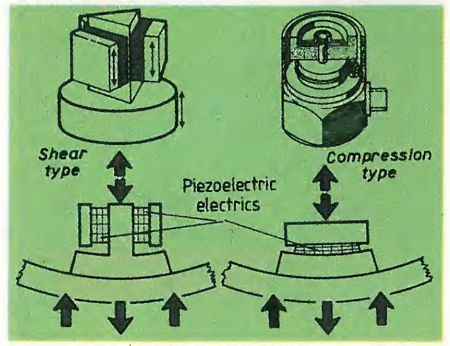
The circuit simply shows how rom is connected to the controller and how the ports are used; a very short assembly language program included in the note provides a maximum pulse width of 65ms and 1ms mark/space ratio resolution given a 12MHz crystal. A prescaler can be used for a maximum pulse width of 130ms.

Accelerometer developments

Piezoelectric accelerometers have become more popular than traditional vibration transducers for measuring shock and vibration because they permit higher-resolution measurements and wider dynamic and frequency ranges.

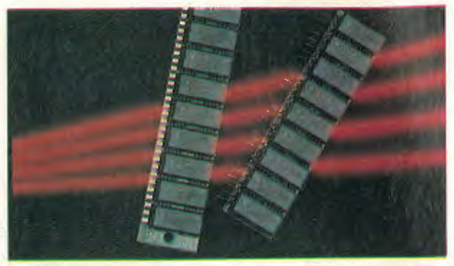
When using piezoelectric accelerometers, temperature transients and base bending cause most problems. Brüel and Kjær Technical Review No. 2, 1987 discusses measurement of these effects for different types of accelerometer designs. In particular, the recently developed shear accelerometer is compared to the compression type.

A large section of the review is devoted to accelerometer calibration.

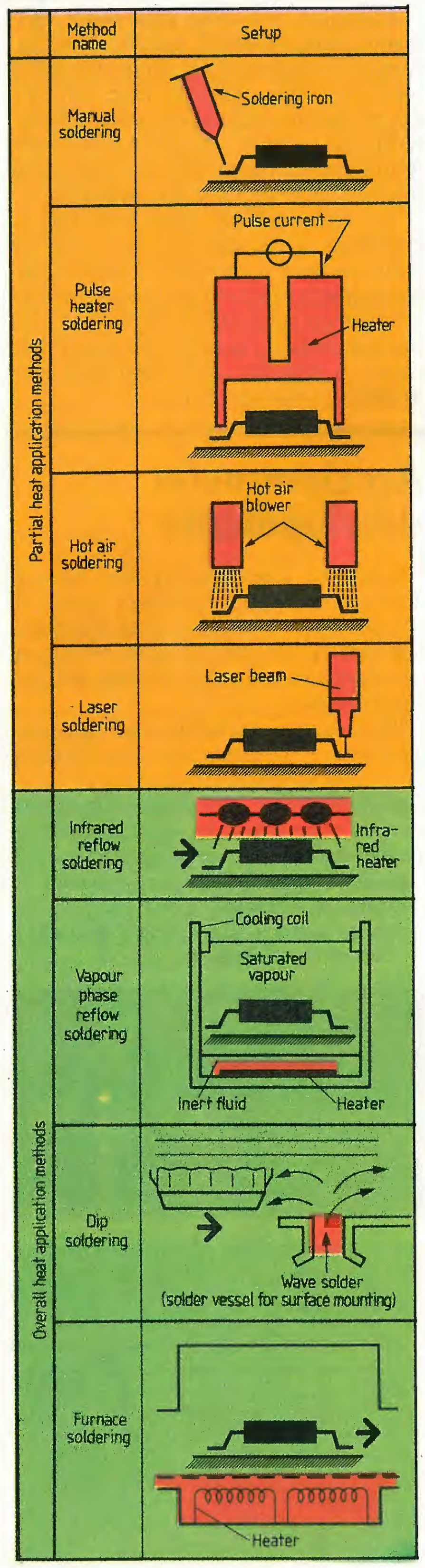


APPLICATIONS SUMMARY

Surface mounting techniques manual



In relation to insertion type packages, surface-mount types are vulnerable to heat stress because of their size and so require different mounting and operating conditions. Hitachi's Surface-mount package user's manual forms a good introduction to surface-mounting techniques, outlining packaging, soldering methods, reliability and inspection. It also contains sections on packaging of the packaging and e.s.d. and lists major suppliers of surface-mount soldering equipment.



Microprocessor interfacing of an eight-pin analogue-to-digital converter

Interfacing of the TLC549 eight-bit a-to-d converter to 8051, TMS7000, 6800-series and 6502 microprocessors is described in Texas Instruments publication SLAA001, with software control examples.

Little more than address decoding is needed to interface the converter to a microprocessor since its data output is serial. The eight-pin device has its own clock, sample-and-hold circuit, data register and control logic. Total access and conversion time of the device is typically 19µs; the similar TLC548 is slightly faster at 12µs.

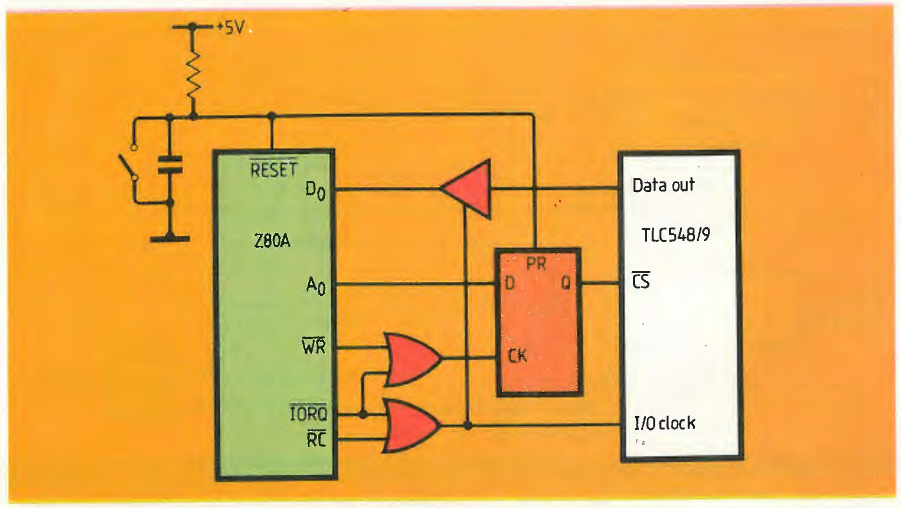
Kits including brief specifications, a TLC549 and p.c.b. are available to designers free of charge.

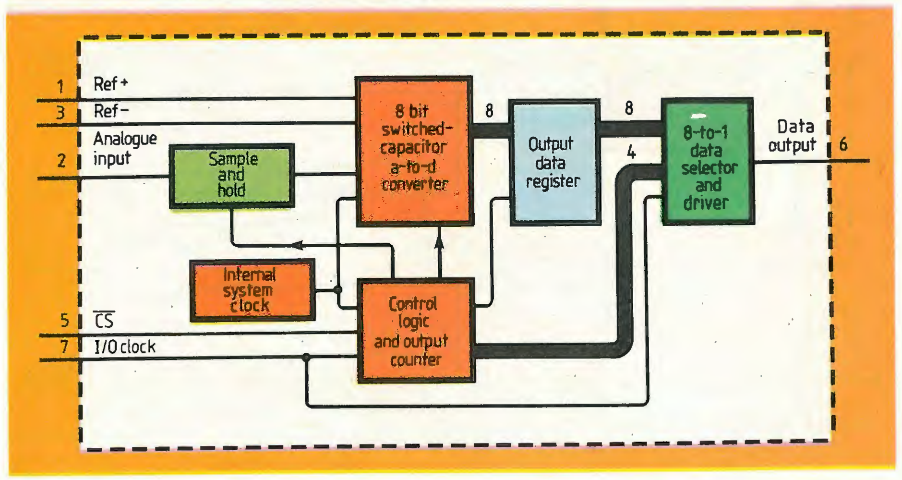
Siemens House, Windmill Road,
Sunbury-on-Thames, Middlesex TW16 7HS
0932 785691

Brüel and Kjær, Harrow Weald Lodge,
92 Uxbridge Road, Harrow,
Middlesex HA3 6BZ
01 954 2366

Hitachi Electronic Components,
21 Upton Road, Watford,
Hertfordshire WD17TB
0923 46488

Texas Instruments, DC Distribution
Hitchin Road, Arlesey
Bedforshire SG15 6SG
0462 834444

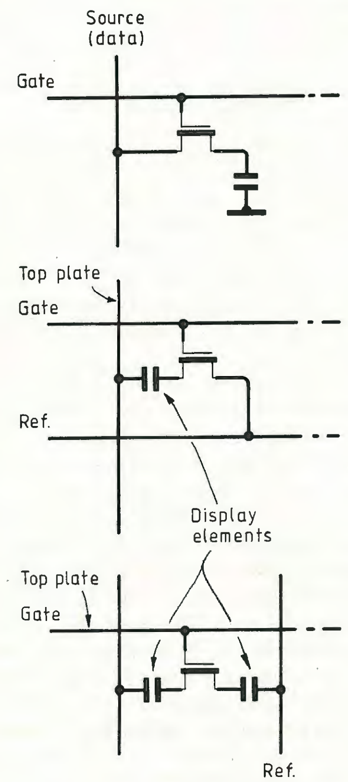




more transistors than a 68000 processor chip). The idea is to avoid the contrast reduction that would result from crosstalk between elements in conventional displays.

GEC's work has been with polycrystalline silicon, rather than silicon of the amorphous kind, to achieve a higher carrier mobility ($10cm^2/Vs$) high enough to allow driver circuit to be included around the display. It involved experimenting with a new technique of low pressure chemical vapour deposition – reported earlier this year – to get round the problem of the relatively low melting point of glass.

An improvement to the wiring technique usually found in displays of this kind has been developed. In the conventional method of driving active matrix displays, as used in those of Japanese origin, 'horizontal' gate lines and 'vertical' source lines when energized switch an m.o.s. transistor to allow charging of a capacitor (top diagram). The straightforward technique is borrowed directly from m.o.s. dynamic ram technology, except that the capacitor that would be the memory element becomes the display element. The control line metallizations are on one side of the display – the bottom plate – while the top plate is made from a conductive transparent oxide, and the liquid crystal forms the dielectric.



The weak point of this approach is the metal crossover, and direct short circuits are the main source of element failure. And when a short does occur it puts out the whole line. The simple expedient of moving one set of control lines to the other face – the vertical lines to the front plate – at the same time arranging for the capacitance to be in the other arm of the mosfet (middle diagram), means that the crossover weakness is removed. This would allow a significant improvement in manufacturing yield.

Manager for the project at GEC's Hirst Research Centre, Dr P Migliorato, explained how they took the idea further. By bringing in another pixel the crossover can be electrically isolated (bottom diagram), which means that a transistor short will not put the whole line out of action. This is achieved by arranging for a further pixel capacitance to appear in the other mosfet arm – again formed with the liquid crystal as dielectric – thus the reference track is no longer directly connected to the mosfet. As the display is a dynamic one, it doesn't need to be.

Next step in the development is an A5 panel containing 100,000 elements, incorporation of colour and greyscale, and experimentation with other types of liquid crystal-material.

A novel ferroelectric liquid crystal display has been developed that will switch at rates suitable for use in video and tv applications, and with high resolution. Though only a small screen test sample was on show, its developers are confident that large arrays will be successfully marketed. Based on a smectic storage principle it avoids the limitation of conventional fast-scan multiplexed displays in which speed or viewing angle deteriorate when the number of rows exceeds about 200. A fast-response 'surface stabilized' electro-optic effect, first demonstrated in 1980 by Clark and Lagerwall, is the basis for the display and uses ferroelectric chiral smectic-C liquid crystal. Switching with 32μs pulses has been achieved in two new materials and tests show that over 1000 rows can be multiplexed with excellent contrast (35:1) and viewing angle (±45° for 20:1 contrast).

A great deal of effort over the last few years has been directed at the problem of producing "three-dimensional" films and television displays.* In general, these methods work by taking two separate views of the original scene and then combining the two images. They are thus inconvenient to use, and largely incompatible with existing two-dimensional systems.

Research at the University of Cambridge has shown, however, that an effective sensation of depth can be created using a single image. The basis of the technique is that, if the brain can be duped into thinking that a picture is not flat, the monocular information in the image will create a sensation of depth. It is not necessary to add correct depth cues.

One method of producing the effect is to view the image through a pair of cardboard frames, of slightly different size, one in front of the other. A good-quality moving colour image is needed, and although computer graphics have been used successfully, a real-life scene is much more effective. The shapes of the frames and the optimum positions have been tested using a panel of subjects.

Another method, which appears to work in a similar way, uses a lenticular lens to create a virtual image but requires electronic pre-distortion; while a third method, currently under investigation, uses chromatic aberration.

*See for instance, Video displays-2, *EWW* August 1985, pages 22,23.

MANCHESTER I.T.

Exhibiting at the same time were some of Manchester's own i.t.-related research projects. UMIST's electrical engineering department is researching a low-cost expert system for speech processing. Unlike other approaches to speech analysis – dynamic time warping or statistical modelling techniques – this one relies on the ability of a researcher to devise a set of rules for recognizing patterns and matching routines that have previously been tested in hard copy printouts of digitized speech. Two low-cost recognition methods have been tested with average scores of 95% but vocabulary is presently small and response time long. The system offers potential the researchers believe since the knowledge-based approach would interface smoothly with the syntactic and semantic processing of continuous speech recognition.

Research has been underway for several years into non-procedural languages in the department of computation. Although it is possible to give a formal definition of an n.p.l., according to Dr T. Scheurer we are still far from understanding the full significance of the concept and its implications. "All that can be said about an n.p.l." he says "is that a program in it is immensely more powerful and easier to write than its procedural counterpart."

In the same department, the Clark Laboratory is pioneering a B.Sc (MEng) degree course in microelectronics systems engineering. The nine companies which sponsor 45 students have a direct involvement in the curriculum of the course, which is for 12 terms at UMIST and three with the industry sponsor. The Lab claims to provide an integrated support environment for the design, production and testing of hardware and software.

The chemistry department has two programs in i.t., one involving preparation of superlattices in which thin alternating layers of semiconductors have their lattice mismatches taken up by strain rather than by dislocation. In another, dynamic molecular modelling by computer simulation has predicted behaviour in LB films, and the work is said to explain the adsorption of hydrocarbon molecules at the water-air interface, as well as defect behaviour.

Also at UMIST is the surface analysis research centre, set up to be self-funding in its basic and applied research into materials surface analysis. Research there on bimetallic and metal-on-oxide catalysts and oxide and organic semiconductor gas detectors for instance is aided by newly developed analysis techniques. Mass spectroscopy by fast atom bombardment was developd there, and the centre has acquired the world's first imaging time-of-flight secondary-ion spectrometer, which extends both sensitivity and mass range. Scanning secondary-ion spectrometry with liquid metal as the ion source allows chemical mapping and secondary-ion imaging of sub-micron features, while dynamic s.i.m.s. allows rapid depth profiling and trace elements analysis.

S.m.p.s. input filters made simple

Modelling the noise sources represented by switch-mode power supplies gives a valuable insight into the design of mains e.m.i. filters.

IAIN ROSE

Filter performance, particularly at the lower frequencies of the filter's desired stop band, depends heavily upon the impedance characteristics of both the noise source (a switch-mode power supply,) and the load (line impedance stabilization network, l.i.s.n.). Unfortunately, whilst the equivalent circuit of the l.i.s.n. is well known, those for the noise source represented by the s.m.p.s. are not.

Consequently, Corcom has developed techniques for measuring the impedance characteristics of switch-mode power-supplies in action. Measurements performed on several supplies became the basis of an equivalent circuit model, which this article will present.

A recent project for Corcom was to develop a mains interference filter which would bring the emissions of most switch-mode power supplies into compliance with VDE 0871B all the way down to 10kHz. Iain Rose of Corcom describes a design tool for estimating the effectiveness of filters and presents a practical example created with it.

THE MEASUREMENT PROBLEM

The first task was to measure the complex source impedance of the non-filtered supply at several frequencies, and in both common mode and differential mode[1] configurations. The result was to be first order common mode and differential mode equivalent circuits for the noise source. And because the major filtering challenge was in the lower frequency range, impedance measurements were to be performed primarily between 10kHz and 1MHz.

Unfortunately, virtually none of the available complex impedance measuring test equipment could operate in the high noise, 240V a.c. environment of the a.c. input of a non-filtered s.m.p.s. An additional complication was that the a.c. input port of the s.m.p.s. is parametric. Since the impedance to be measured is a function of diode conduction, and also possibly the coupling mode, any technique using an *injected* signal would not correctly describe these characteristics. A better approach would be to determine impedance through the use of the noise products generated by the supply.

One possible method involved comparing the noise measured with two different values of load impedance, and then using the results to calculate the complex source impedance. But this called for noise voltages to be measured vectorially, and the a.c. input environment proved just as hostile to vector voltage measurement as it had been to impedance measurement. Hence although this method could provide qualitative source impedance magnitude information if scalar voltage measurement was used, the need for complex measurement forced it to be abandoned.

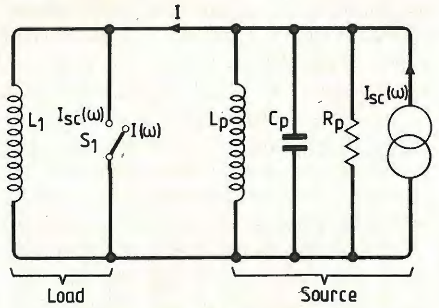


Fig.1. Resonance measurement circuit. A wideband current probe inserted between source and load will produce a noise signal which can be measured with great accuracy on a spectrum analyser.

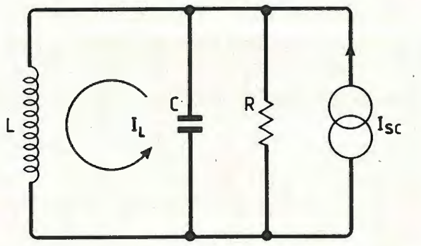


Fig.2. S.m.p.s. at resonance: A simple parallel tuned circuit.

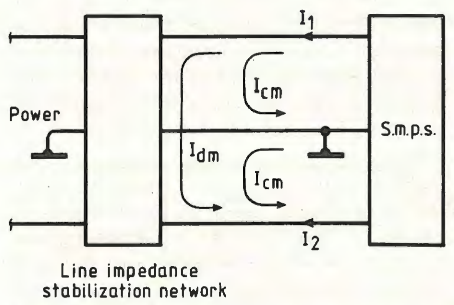


Fig.3. Network to show the difference between the common mode and differential mode noise components.

In the end, a technique was developed to solve the problem: one which allowed scalar measurement of the noise spectrum but could also provide determination of the real and imaginary parts of the source. In this technique, the frequency of resonance of a reactive load was determined over several frequencies in the range of interest, and the results were then used to determine whether the source reactance was entirely capacitive, entirely inductive, or a combination of both. The real part was determined from the magnitude of the peak of noise current at resonance.

THEORETICAL BASIS

Consider the ideal resonance measurement circuit (Fig. 1). The noise source is shown for convenience as a Norton equivalent circuit, because currents are being measured. Noise source current has a value of $I_{sc}(\omega)$ and this represents the short circuit current. L_p, C_p and R_p are components of the noise source. An inductive load L_1 has been selected for this example.

If a wideband current probe is inserted between the source and the load, it will provide a signal which is proportional to the current. This signal can be measured with great accuracy on a spectrum analyser.

A switch S_1 is also shown in Fig. 1. In its closed position, all the source current flows through the short circuit and is measured through the current probe, giving the value I_{sc}. When the switch is open, the current flowing through L_1 is measured. At resonance, this current is larger than I_{sc}. Consider the simple parallel tuned circuit of Fig. 2. Here I_L is the current circulating between L and C.

At resonance (ω_0), $|I_L| = Q|I_{sc}|$

$$\text{where } Q = \omega_0\frac{L}{R} = \frac{1}{\omega_0 CR}$$

Thus R can be determined from ω_0, L and the ratio of I_L to I_{sc} at ω_0. Note that I_L (Fig. 2) is the current circulating between the inductive branch and the capacitive branch of the network.

Now in Fig. 1, the current which is measured is the current which circulated between the source and the load. Thus the load must be either inductive or capacitive at network resonance, while the source is opposite. In practice, realizable load components may not be pure L or pure C, although as long as the load is implemented such that it is net L or net C over the frequency range of interest, this approach may be used.

Let L'_1 or C'_1 be the net values of parallel load inductance or capacitance at network resonance, and let R' be the combination of all the equivalent parallel resistances in the network.

Then $|I_L| = Q'|I_{sc}|$ for $Q' \geq 3$

$$\text{where } Q' = \frac{\omega_0 L'_1}{R'} \text{ or } \frac{1}{\omega_0 C'_1 R'}$$

The approximation is due to the possibility that part of R' is in the load. Thus I_L would include a real component in the shunt load resistance and an imaginary component in the shunt load reactance. Of course, effort should be applied to maximize the value of load Q.

Note that an alternative measurement technique could have been developed using open circuit voltage and load voltage comparisons. This so-called Thevenin technique requires a.c. power to be provided to the s.m.p.s. through a network with very high, wideband, source impedance. However, such an impedance is much more difficult to realize than the wideband low impedance required by the previous approach.

For the network discussed above, the noise source was a one-port network. However, an s.m.p.s. having line, neutral and ground terminals actually has two a.c. line ports. These ports may be individually filtered, but it is much more efficient to reduce them to their common mode and differential mode equivalent circuits, each with a one-port noise source. The total noise on each port is the sum of its common mode and differential mode components.

COMMON AND DIFFERENTIAL MODES

Consider the network of Fig. 3. Common mode current, I_{cm}, is that current which appears at the same magnitude and phase on either a.c. line. It returns on the ground lead. Differential mode current, I_{dm}, is the current which circulates between the line and neutral leads. The total current on either the line or the neutral lead is the sum of its common mode (c.m.) and differential mode (d.m.) components.

Common mode current is in phase on both sides of the line while the phase of the d.m. current on one side is opposite to that on the other side. Now if the line and neutral leads are enclosed in a current probe such that they add, the resultant is $2I_{cm}$. If one lead is then reversed such that the currents subtract, it will result in a measure of $2I_{dm}$. In practice, both common mode and differential mode currents are sensed with wideband current probes, and all measurements are performed at 220V a.c.

Using the techniques described here, Corcom has investigated 14 switching power supplies ranging in output from 50-1000W. For this article, new complete characterizations were performed on four supplies. The first and second were closed frame types with separate circuit boards for input, inverter and output. They are rated at 300W and 150W d.c. output respectively. The third was an open frame unit rated near 200W. Its level of conducted emissions was the highest in the survey. The fourth, with substantially lower levels of emission, was another open frame supply, rated at 116W.

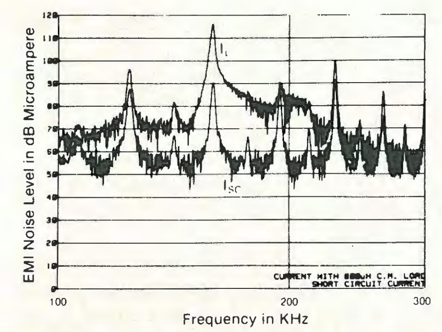


Fig.4. A demonstration of common mode resonance in power supply unit no.1.

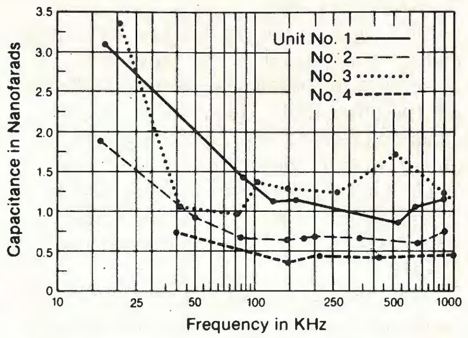


Fig.5. Comparison of common mode parallel capacitance versus frequency for the four power supply units tested.

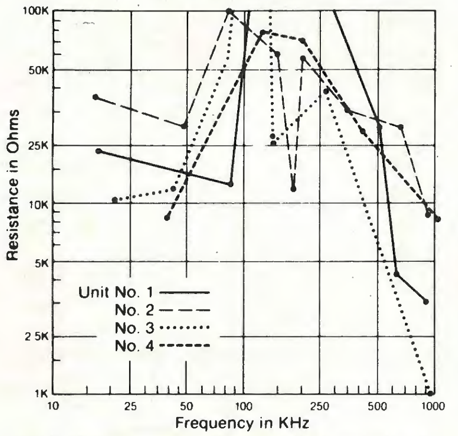


Fig.6. Common mode parallel resistance versus frequency for the four power units.

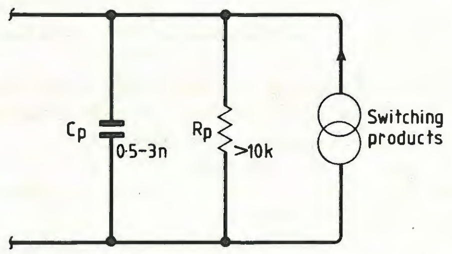


Fig.7. Common mode noise source model.

COMMON MODE RESULTS

Common mode noise is essentially composed of harmonics of the switching frequency. For these products, throughout the 10kHz to 1MHz range, common mode resonance was established exclusively with inductive loads. Thus the c.m. noise source of the supply was capacitive.

To increase resolution, calibrated variable capacitors were a.c.-coupled between ground and both a.c. line terminals at the power supply so that a given switching product could be precisely tuned. The difference between the calculated resonating capacitance and the value of the external variable capacitor is then the actual C_p of the supply. Figure 4 shows an example of c.m. resonance on supply number 1. The lower curve is I_{sc} while the upper curve is I_L.

These experiments were repeated on each of the supplies throughout the 10kHz to 1MHz range. The behaviour of C_p over frequency is shown in Fig. 5. It can be seen that the value remains relatively constant over the frequency range with the exception of an increase in value at the lower end.

The ratio of I_L at resonance to I_{sc} was used to calculate the total circuit conductance, from which the conductance in the load inductor and variable capacitor were subtracted. This provided the value for source R_p. Such resistance data was collected over the 10kHz to 1MHz frequency range for each of the four supplies analysed (Fig. 6).

As a confirmation, a second method of determining R_p was also used. In general, reasonable agreement was found between the two.

Note that as R_p is not constant with frequency, a parallel model is not precisely correct. Calculations of the equivalent series resistance (e.s.r.) of the c.m. noise source indicated that a series model would be better for values of e.s.r. which were relatively constant with frequency. Nevertheless, the calculations showed large variation of e.s.r. with frequency, starting as high as 700Ω at 16.5kHz and falling to 6Ω at 907kHz on the same supply. Less variation was observed on R_p over frequency, indicating that most of the resistance is parallel. Hence the parallel model will be used here.

The Q of the noise source was never found to be less than 4 and was typically 6 to 40. Thus the source is predominantly capacitive and the equivalent capacitance is essentially the same for either a series or a parallel representation.

The resultant common mode noise source model is shown in Fig.7. Resistance R_p is greater than 10kΩ below 500kHz at least.

DIFFERENTIAL MODE RESULTS

Differential mode noise consists of both wideband noise and harmonics of the switching frequency. Figure 8 compares differential mode I_L for a 3Ω load and for a much higher load impedance (300Ω in parallel with 1mH). Note that the noise components are not all equally affected. The switching harmonics portion increases load current by as much as 32dB when the load impedance is reduced, while the wideband noise current is not changed. This indicates that these different components have different source impedances: the wideband noise has a high impedance while that of the switching products is very low. These different characteristics appear to coexist at the same frequency and thus can only occur if they are alternatively switched – for example by the input rectifier.

The d.m. source impedance of the significant switching products was found generally to be quite low and of very low Q. Therefore, attempts to resonate it with reactive loads were unsuccessful. Instead, it was found preferable to a.c.-couple a non-inductive

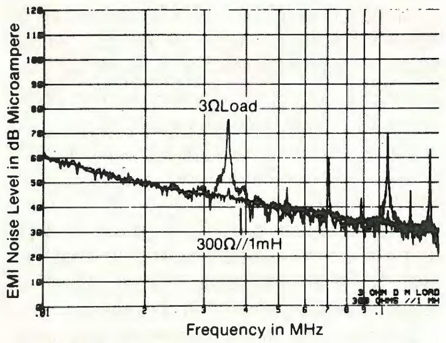


Fig.8. Differential mode source impedance characteristics for a 3Ω load, and for a load of 300Ω in parallel with 1mH. Impedance of wideband noise is shown to be high, while that of the switching products is very low.

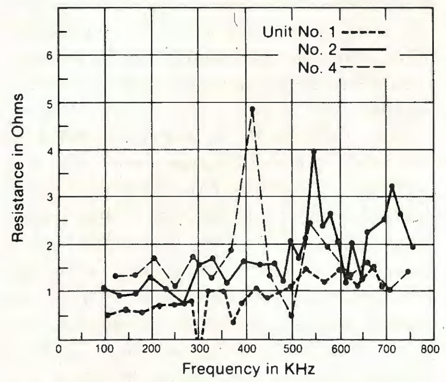


Fig.9. Apparent differential mode source resistance.

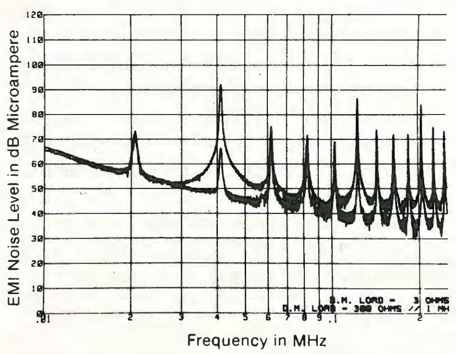


Fig.10. Comparison of I_L for the loads in Figure 8. Switching frequency is 21kHz.

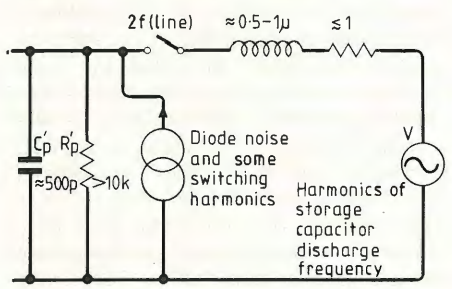


Fig.11. Differential mode noise source model showing alternate switching.

resistor across the supply terminals, and record the resultant drop in d.m. output voltage. This was repeated between 100kHz and 750kHz (Fig. 9). Results on units 1, 2 and 4 show low frequency impedances of 0.5 to 1Ω which increase slightly with frequency; thus a series R L circuit is suggested. The value of L was calculated to be of the order of 0.5 to 1μH.

In the data on each of these supplies there are one to three inconsistent points. On unit 1, R_s at 307 kHz, which was found to be regenerative with high impedance d.m. loads, was only 0.36Ω. Regeneration is suspected for similar points of unusually low R_s in the other units.

On supply 3, the typical d.m. switching harmonics (second, sixth, tenth etc.) followed the low impedance behaviour found on the other units. However, several other harmonics were also present and these had a much higher source impedance. This is evident in Fig. 10 in which I_L is compared for a 3Ω load and a parallel 300Ω and 1mH load. The fundamental switching frequency is 21kHz.

Note that the second, sixth and tenth harmonic currents increased dramatically when the load impedance was reduced. However, others changed very little. These products have much higher source impedance. Two such harmonics (fifth and seventh) were identified and their source impedance was evaluated through resonance. Their measured C_p was 502pF and 429pF respectively and their R_p was 26kΩ and 10.6kΩ respectively. Thus the source impedance of these products was quite similar to that of the wideband noise.

The dual nature of the differential mode noise source impedance can only be explained by the two sources being switched alternatively. Figure 11 incorporates this switching in the d.m. noise source model.

COMPARING C.M. AND D.M. MODELS

The elements of a switching mode power supply directly involved in conducted emissions are shown in Fig. 12. When the switching transistor turns off, its collector to emitter voltage rapidly rises to as much as 500V and this generates a current which flows through the stray path between the collector and ground, and which returns through the l.i.s.ns and the diode bridge. This current, which is pulsed at the switching rate, is the common mode noise.

The stray path between collector and ground includes two parallel capacitances: one between the switching transistor case and its heat sink (if earthed), the other between the primary and the (typically earthed) secondary windings of the transformer. Over the intended noise source model frequency range (10kHz to 1MHz) the capacitive part of the noise source loop has a much higher impedance than any other element. This predicts a capacitive common mode noise source model, which is consistent with the empirically-derived results above.

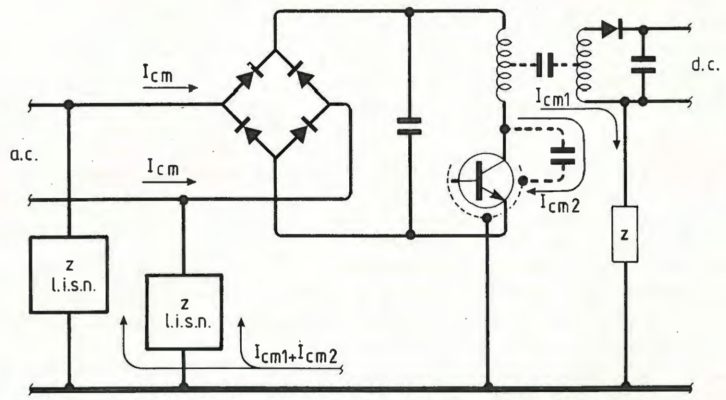


Fig.12. Elements of a switched mode power supply which are directly involved in conducted emissions. The capacitive part of the noise source loop has a much higher impedance than any other element.

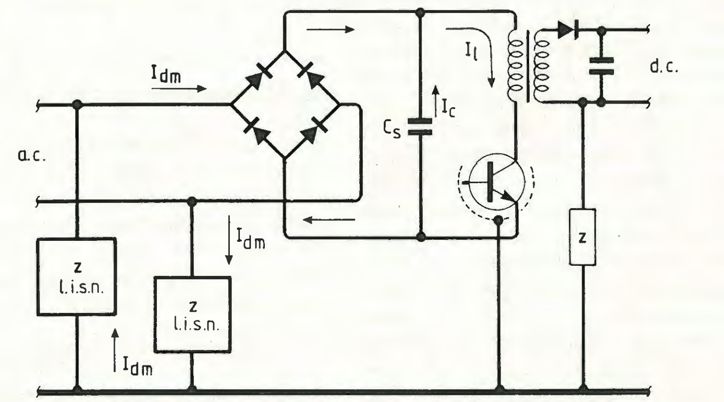


Fig.13. Origin of the predominantly differential mode emissions. A low source impedance is predicted.

Figure 13 shows the origin of the predominant differential mode noise emissions. Capacitor C_s stores the energy supplied by the a.c. line and bridge rectifier. This energy is coupled to the converter through the action of the switching transistor which repeatedly discharges the capacitor through the transformer. For this circuit, the repetition rate is the switching frequency and the current waveform I_L is a series of pulses. Its spectrum consists of harmonics of the switching frequency. If the pulses are largely symmetrical about the average value, the spectrum will be primarily odd-numbered harmonics.

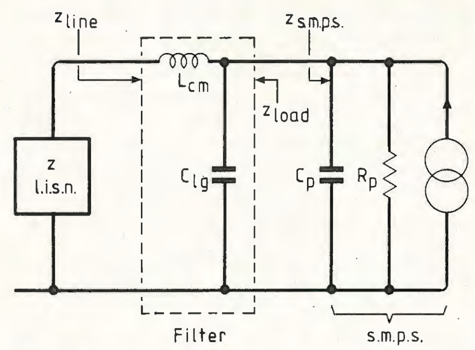


Fig.14. Common mode filter model for a.c. mains filters.

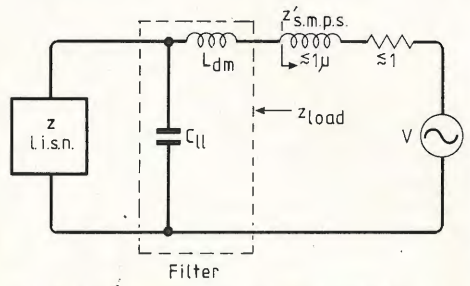


Fig.15. Differential mode filter model for low impedance products.

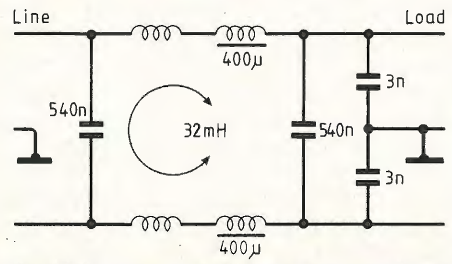


Fig.16. The complete filter – a composite of the common mode and differential mode ones.

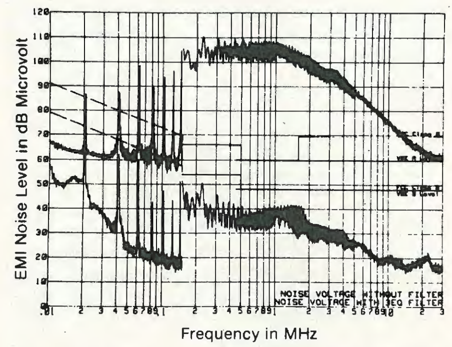


Fig.17. Conducted emissions of power supply unit no.3, with the composite filter (below) and without (above).

The storage capacitor is not an ideal element because it has series resistance and inductance. The pulsed discharge current, I_L, develops a voltage across the impedance presented by the L, R and C of the storage capacitor. When the diode bridge is conducting, the voltage appears across the line terminals of the supply. This is the principal source of differential mode emissions of switching products. The source impedance is composed of the impedances of the storage capacitor and the diodes. Thus a low source impedance is predicted, consistent with the empirical results.

When the diodes in the input rectifier switch off, a current spike is generated. This repeats with the frequency of the a.c. mains and therefore generates harmonics of the main frequency. But because the diodes are not forward-biased when this occurs, their series impedance (and thus the noise source impedance) is high. The high source impedance for diode noise and the low source impedance for I_L harmonics cannot exist at the same frequency and time; they are alternatively switched by the diodes. Thus it is correct to model them as switched parallel sources, although many converters use more complicated switching circuits than the single device shown here.

FILTER CIRCUIT CONSIDERATIONS

The power line e.m.i. filter is an LC low pass device. For maximum attenuation throughout its stop band, the magnitude of the impedance of the filter at each port should be opposite that of the device connected to it. Thus, for a low impedance noise source, the filter impedance should be much higher (large series inductance), while a high impedance noise source would require a low filter impedance (large shunt capacitor). These approaches can be applied to the common and differential mode models for a.c. power line filters (Fig. 14, 15 respectively).

In the circuit shown in Fig. 14 the noise source impedance of the supply, Z_{smps}, is capacitive. Thus the issue of mismatching the load-side c.m. impedance of the filter to Z_{smps} depends upon the lowest desired frequency at which the filter is effective. To meet the VDE B level emissions specification, filter attenuation is required down to 10kHz.

Even with C_{lg} and C_p in parallel, one must be concerned about network resonance. Power transfer between the supply and the l.i.s.ns is maximized when they are conjugately matched. This occurs at network resonance when the e.s.r. of the l.i.s.n. is matched to an equivalent parallel resistance appearing at Z_{Load} and equal to R_p. The filter configuration of Fig. 14 at the frequency of network resonance (f_0) does match e.s.r. up to a much higher equivalent parallel resistance, and it is important to place f_0 at a frequency where it will do no harm.

Applying the same reasoning to a filter for d.m. low impedance switching products results in the circuit of Fig. 15. Here, L_{dm} provides a much higher impedance than the typical 1Ω + 1μH of the noise source model. Also C_{LL} may be selected to be much smaller than Z_{lisn}. This circuit, however, matches the R_p of the l.i.s.ns down to a lower value at resonance, again in the direction of reducing attenuation at network attenuation at network resonance.

The d.m. filter must also accommodate the high source impedance presented by wideband noise and by switching products which are not related to the discharge rate of the storage capacitor. For these products, Z_{load} should be low. This is solved by adding another C_{LL} at the load side with a high impedance noise source. Again, this circuit performs impedance transformation at resonance.

The actual filter is the composite of the common mode and differential mode filters. (Fig. 16).

Figure 17 includes two plots of composite conducted emissions of power supply number 3. The VDE and FCC limits for emissions are also included. The upper curve is taken without a filter. The lower curve was taken with the Corcom 3EQ filter, and it can be seen that it is extremely effective in reducing conducted e.m.i. throughout the entire range.

Reference

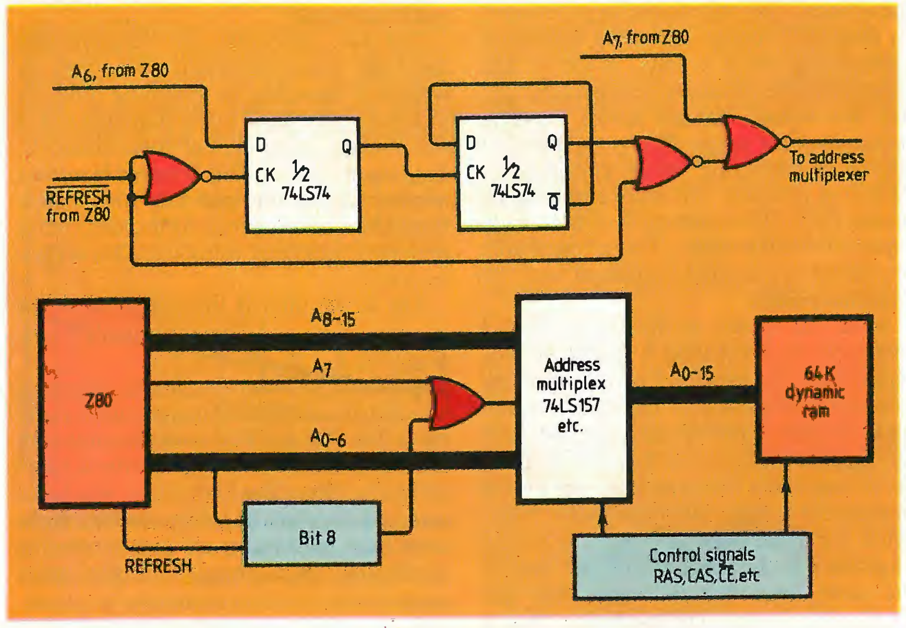
1. L M Schneider, Power line EMI filter insertion loss. *IEEE Symposium on Electromagnetic Compatibility*, Santa Clara, California, Session 5c, September 1982.

Iain Rose is managing director of Corcom UK Ltd.

Above it all

BT riggers have installed the highest dish antenna ever to be erected in the UK on the IBA's Chillerton Down tv mast on the Isle of Wight. It is one of two new antennas mounted at a height of 750 feet (230m) to span the 130km path of this trial microwave link to Alderney. This height is required to allow for the curvature of the earth.

From Alderney the link will go on to Jersey and Guernsey so as to supplement new optical fibre submarine cable soon to be laid from the UK. Both are part of a programme to strengthen communications between the Channel Islands and the mainland. It is also augmented by the recently reported new digital routes across France.



Extra bit for Z80 refresh

I recently built a spare board for my Z80-based SC84 using Samsung KM4164A dynamic rams with 8bit refresh. Only 7bit refresh is provided by the Z80 and as a result the system died after two or three minutes. An easy way of providing the extra refresh bit is to toggle address line A_7 in each complete refresh cycle.

At refresh time, the first bistable i.c. latches A_6 and feeds the state to the second bistable device, which is configured as a one-bit counter. Every 128 refresh cycles, this counter changes state. A Nor gate ensures that the extra bit is only active during the refresh strobe and a further gate combines the extra bit with address line A_7.

Note that A_7 is inverted. When addressing rams this is not a problem but other circuits may require a true A_7. If so, there is a spare gate left in the Nor package.

Kenneth S. Termie
Leicester

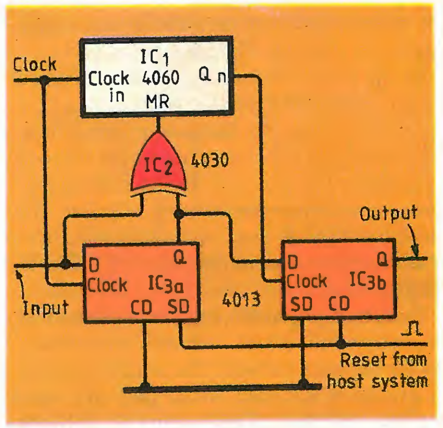
Glitch filter

In industrial applications where long wires are used, this data receiver eliminates spikes and other brief input-level changes.

Devices $IC_{2,3a}$ sample input, resetting counter IC_1 should an input change or spike occur. Input level is copied to the output if the counter can count up far enough to activate the clock pin of IC_{3b}, i.e. input level was stable for at least 2^{14} clock periods.

In most cases, the delay between input and output will not be a problem. Sampling rate and delay time is easily modified by choosing an appropriate clock frequency and changing the number of counter stages.

Stephen Rétallér
Budapest
Hungary



Remote-sensing room thermostat

In the September issue on page 909, the table on the right called port and bit allocations was inadvertently published instead of this eprom data for the remote-sensing room thermostat.

Add.	Data	Add.	Data	Add.	Data
00	30	0B	FF	16	13
01	19	0C	09	17	FF
02	0B	0D	FF	18	33
03	FF	0E	14	19	1C
04	34	0F	FF	1A	11
05	37	10	31	1B	FF
06	12	11	1A	1C	0A
07	FF	12	0C	1D	FF
08	32	13	FF	1E	18
09	1B	14	0B	1F	FF
0A	10	15	FF		

Eprom programmer for the CPC6128

This programmer for the Amstrad CPC6128 is a compromise between low-cost units suitable for only one eprom type and those that allow full software control. As shown it can program 2716, 2764 and 27128 eproms and 6116 rams with battery back-up, but the design lends itself to modification.

Programming voltage and pulse time are software controlled. Pulse time is controlled through the 40103 presettable counter which is clocked by the 4060 oscillator/divider at approximately 0.5ms intervals.

Normally, counter pins 2 and 9 are high. At the end of a time pulse, counter pin 14 goes low, holding the oscillator in reset through pin 12. To start a new pulse, the preset time is loaded into port P_{1A} and counter pin 9 is taken low momentarily. This loads the time value into the counter, sending its pin 14 high and removing the reset signal from the oscillator.

At the end of the period, counter pin 14 goes low, stopping the oscillator. Bit zero of port P_{1C} senses the pulse so that software can recognize when the pulse has ended. A pulse of 50ms requires a count of 102. Holding counter pin 2 low holds the program pulse on by clearing the device.

Programming voltage is derived from the computer 5V rail using a switched-mode power supply with programmable outputs of 12.5, 21 and 25V. My circuit idea in the August 1985 issue shows how you could modify this p.s.u. for the 6V rail needed for intelligent programming.

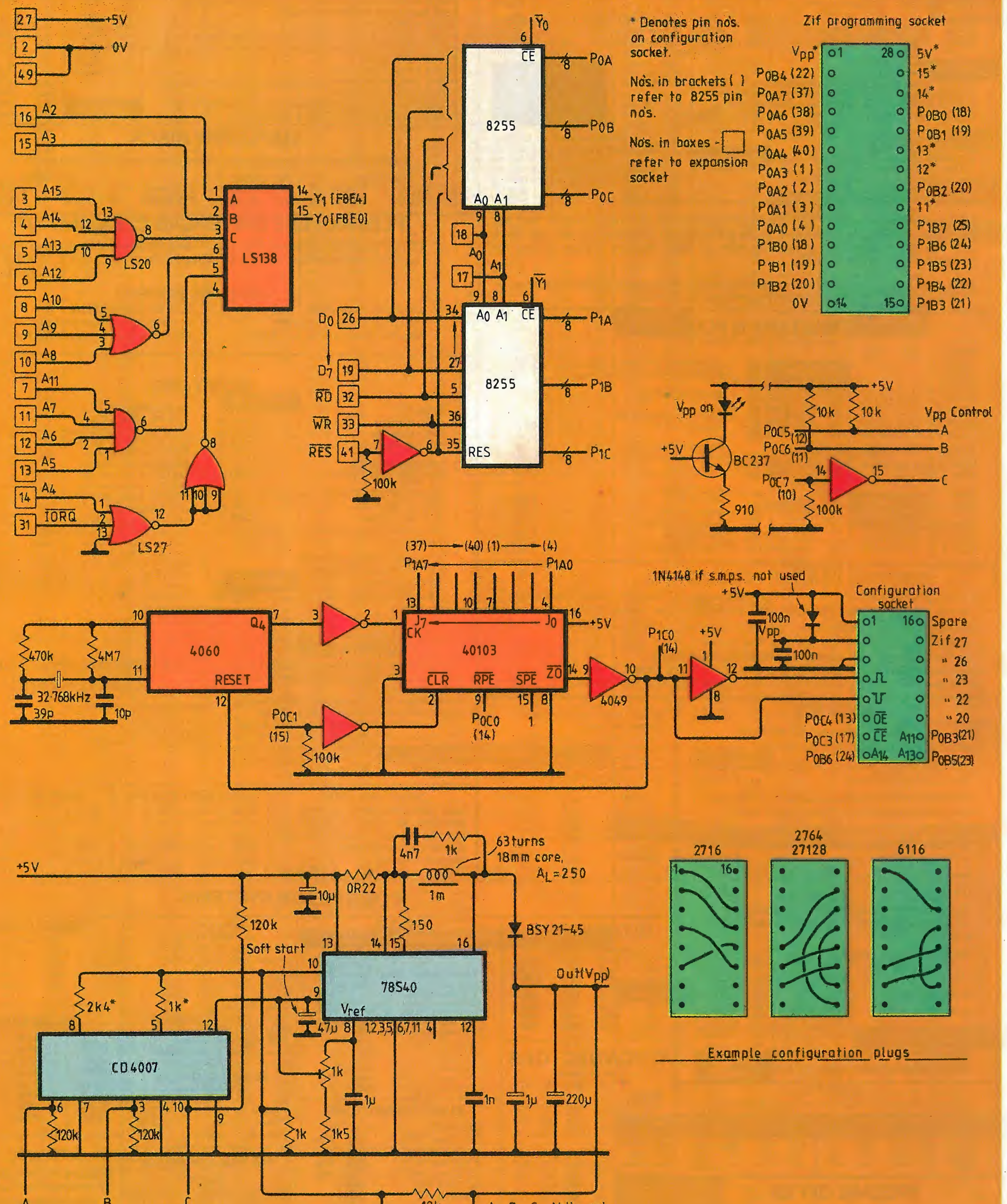
Note that the V_{pp} on led forms a small constant load, without which the supply would be unstable. Careful layout is needed to ensure that high current from the inductor, switch transistor and diode are not coupled into the regulator circuit. My prototype p.c.b. had a ground plane.

J.R. Hunt
Doncaster

Port and bit allocations.

Port	Status	Bit 7	6	5	4	3	2	1	0
P_{0A}	W	← Eprom address low →							
P_{0B}	W	sp	← Eprom address high →						
P_{0C}	W	V_{pp} control →			$\overline{OE}$	$\overline{CE}$	sp	CLR	JAM
P_{0D}	W	← PIO control →							
P_{1A}	W	← Time preset →							
P_{1B}	R/W	← Eprom data →							
P_{1C}	R	sp	sp	sp	sp	sp	sp	sp	$\overline{PROG}$
P_{1D}	W	← PIO control →							

All output bits of port P_{1A} and (potentially) P_{1C} are set low when the data direction P_{1B} is reversed. Spare lines are indicated by sp.



A	B	C	Volts out
0	0	0	12·5
0	1	0	21·0
1	1	0	25·0
–	–	1	4·7

* Reduced by 300Ω from theoretical value to allow for $R_{ds(on)}$ of 4007

CP/M+ software for this programmer, including sources in HiSoft C, can be obtained by sending £2 and a formatted 3in disc to J.R. Hunt at 30 Whitton Close, Bessacarr, Doncaster DN4 7RD.

Mercury extends satellite coverage

Mercury Communications has ordered two additional Standard A satellite Earth stations from Marconi Communications Systems Ltd at a cost of £3.7 million ($5.9M). When installation is completed, Mercury will be operating six systems from its Whitehill, Oxfordshire site. In addition to the existing complement of a Standard A, B and C satellites C, an eight-metre standard F2 Earth station has recently been brought into operation to accommodate the rapid growth in transatlantic Intelsat Business Services (IBS) traffic.

The first of the two new 15.5m systems will provide voice and data services to Hong Kong and the Far East via the Intelsat Indian Ocean Regional Satellite. It is scheduled for completion next February. The second, due to enter service early April 1988, will provide transatlantic voice and data service to the USA via the Atlantic Ocean Intelsat. It will also provide diversity routing capabilities for Mercury's transatlantic digital leased services.

Cable & Wireless consortium applies for Japanese licence

International Digital Communications Planning Inc. (IDC), the consortium in which Cable & Wireless is a partner, is establishing an operating company to apply for a licence to offer international telecommunications services to Japan. This follows the breaking down of merger talks between IDC and ITJ (International Telecomunications of Japan) and the announcement by the latter that it proposed to file a separate licence application.

It was intended that the application would be filed by the end of September. The Ministry of Posts and Telecommunications (MNP) would then be able to decide on its recommendation by the end of the year and so allow the licence to be issued. If this is the case there will be very little delay in the introduction of the leased circuit services by Intelsat and existing cables which were originally scheduled for the end of 1987. This was to be followed, in early 1989, by the switched service.

The full range of switched and leased digital services will then be provided by the beginning of 1990 via the North Pacific Cable, previously known as Private Pacific Cable (PPAC).

As well as Cable & Wireless, the IDC consortium includes Pacific Telesys and Merrill Lynch together with a number of Japanese companies including C. Itoh, Toyota, NEC, Fujitsu and Hitachi.

Jonathon Solomon, Cable & Wireless's director for corporate strategy, who is responsible for directing the group's efforts in Japan, said: "The Japanese way of decision making is unique and complex, but it always allows wisdom to prevail. IDC owes its survival to the invaluable support of many brave and forward-looking people in Japan, the United Kingdom and the United States. IDC's future progress will be determined by the MNP in Japan and IDC looks forward to working closely and cooperatively with the Ministry so that it can contribute to serving the people of Japan in creating a new era of telecommunications in the Pacific basin."

Continuity for Vodafone and Cellnet

The two existing cellular radio operators, Cellnet and Vodafone, will provide the UK part of the pan-European digital cellular radio service due to come into service in 1991. These two companies, together with operators from continental Europe, have signed a memorandum of understanding committing the signatories to a detailed timetable for the procurement and establishment of the new networks to allow the service to take place.

To enable the two operators to enter into this commitment with confidence, the Government has made it clear that it is they who, as from 1991, will be allocated on an equal basis the 400 channels in the 900MHz band currently held in reserve for the introduction of the pan-European system.

Auto line testing in London

British Telecom has placed a further order, worth £15.7M, with Teradyne for the supply of 4Tel automated subscriber line test systems. They will be used to equip BT's six districts in Greater London, which together serve over four million customer lines. Delivery completion is scheduled for April 1989.

The 4Tel system will perform nightly tests of all subscriber lines and execute a series of on-demand diagnostic tests and computer-guided fault location sequences. In addition a number of enhancements, required by BT in London, will be supplied as part of the contract. These include the Teradyne voice response system and a series of upgrades tailored to BT's emerging digital switching environment.

Mercury switching access to Italy

Mercury Communications Ltd and the Italian PTT have reached an agreement with regard to switched telephone and telex services between Italy and the UK. This is the first such agreement that Mercury has obtained with a country in continental Europe. It will allow Mercury to offer customers a greater discount than the 3% that it provides at present.

Gordon Owen, Mercury's managing director, said "This agreement is an historic breakthrogh for Mercury and a bold initiative by the Italian PTT. I hope that this recognition by the Italian administration of Mercury's growing international position will encourage other European PTTs to conclude service agreements with us. This latest agreement will mean that Mercury's business and residential customers will be able to benefit from even cheaper calls to Italy". He continued: "The wishes of the Italian Administration were decisively influenced by Mr John Butcher on behalf of the British Government, who visited Italy in February 1987. We are very grateful to Mr Butcher for his effective support. Mr Butcher has since written to all European Telecomunications Ministers encouraging a positive response from PTTs in their negotiations with Mercury and we have high hopes of further agreements in the near future."

Korea poised for telecom export surge

'Korea Inc.' is poised to launch a large scale export drive in telecom markets. As well as using the momentum she has gained in the US keyphone, tv and personal computer markets to attack the p.b.x., office automation, carrier transmission and videophone markets in the USA (and then, no doubt, Europe), Korea has set her sights on the market for public network equipment in developing countries.

These findings appeared in a recently published report from Pyramid Research of Cambridge, Massachusetts, USA (telephone: 617-868 4725) entitled "Korea Inc.'s Telecom Strategy". According to the authors, in both areas, the government of the Republic of Korea will play a major role by co-ordinating, directing and supporting Korea's telecom industry. In addition, the study finds that Korea is overbuilding capacity with the intention of entering telecom market as aggressively as she did the consumer electronics field.

Band Three Radio opens for service

Band Three Radio, the new national mobile radio network is open for public service this month (October). It is planning to offer its service in most major cities over the next nine months by which time it expects to cover 60% of the population.

The new service offers business users the ability to communicate with their own staff and other network users via a new generation of mobile radios. These use trunking techniques which allow channels to be shared and yet still enjoy adequate privacy. The service offers far higher capacity and much better channel availability than is at present offered by other types of mobile radio.

Users subscribing to the network will be able to select the geographic coverage required for each vehicle in their fleet. There will be no call charges or licence fees and so costs will be totally predictable. Band Three has appointed seven national and twelve local service provider companies. These are important to the development of the network as they are able to offer customers everything that they need to stay on the air.

IBM and Ericsson plan for the future

IBM and Ericsson are to explore ways in which IBM's expertise in database and data network management can be combined with Ericsson's switching technology to provide telephone customers with a wide array of new or improved services.

Some telephone companies offer, or plan to offer, such services using the technology of today's digital networks. However, if such services are provided through dedicated central facilities, they can be better managed and offer users greater flexibility as well as the potential for lower costs. Such a concept has come to be called the 'feature node' approach or the 'intelligent network'. Today, many organizations have their offices linked by private telephone networks using leased lines. With the intelligent network they could have the benefits of a private telephone network by using a 'virtual private network' service. In this situation, the intelligent network would recognize the particular user's call as private, and automatically connect it over a normal switched line to the other business location.

The aim of the joint study is to develop technical solutions for the intelligent network concept, specifically for advanced network features. These solutions will be based on standard IBM and Ericsson systems and specialized software from the two companies to implement the concept. The non-exclusive agreement provides for architecture definition activities between IBM systems and Ericsson switches; connectivity switches between IBM equipment and the AXE switches using standard interfaces; and product opportunity evaluation. It also calls for the study of interface implementations to allow for the provision of competitive services by PTTs and other service providers.

Jan Stenberg, Ericsson executive vice-president and head of its Public Telecommunications Business Area, said: "This agreement to co-operate comes at a time when the providers, and the users, of telecommunications services are loooking for innovative services that can best be created by complementary expertise. The agreement is a logical move for both companies."

According to Helmut Schmidt, vice president, telecommunications, IBM Europe, "This agreement is in line with IBM's efforts to provide solutions to emerging requirements in the field of telecommunications services. We believe that the contribution of our technology to this co-operative effort will bring significant value to the users of such services."

EEC Open Networking study

Scicon Ltd is undertaking a six-month study for the European Commission into Open Network Provision (ONP) which will affect future telecommunications standards throughout the Community. The company's communications consultancy group is investigating usage conditions and interface arrangements to be adopted by telecommunications administrations within the Community to stimulate the pan-European value added services market.

ONP will open up the connections to the administrations' basic networks for use by value-added service operators and other private network providers. Value-added services include electronic mail, electronic data interchange, electronic funds transfer and some bureau operations.

Service providers are connected to customers through switched public telecommunications networks or through leased lines. At present, the rules governing such connections and their associated technical and operational standards differ from country to country. The study aims to overcome this situation by adopting European-wide standards. Over the past three years, the Commission has taken initiatives in telecommmunications on ISDN, wideband services and mobile radio. These have resulted in a Green Paper on the future liberalization of telecommunications in Europe.

The study, commissioned by the Telecommunications, Information Industry and Innovation Task Force of the EC in Brussels, will be carried out jointly by Scicon in the UK and its sister companies in Germany and in France.

DEC moves closer to OSI

In a move aimed at bringing its networking technology closer to international communications standards, Digital Equipment Corporation (DEC) has announced a series of networking products and strategies worldwide. The announcement includes the availability of Ethernet on twisted pair cable; a suite of network applications software that follows the CCITT X.400 recommendations for electronic mail and messaging; and a general statement on the evolution of the architecture.

When making the announcements in London, David Clarke, Market Development Group Manager, pointed out that "Customers don't want networks, they want the consequences of them. That is, they want to be able to make things happen." They need an open system which is easy to install, operate, change and use – the target being unrestricted connectivity.

DNA/OSI Phase 5 is fully OSI Layers 4 and below. It is the latest phase of EDC's architecture in their move towards interoperability with OSI. Thus DECnet products will embody the lower levels of OSI: only the upper levels will differ between DECnet and OSI. This provides for easy development of applications to run unchanged in either environment.

The rapidly growing business requirements of networks indicates that unrestricted connectivity will only be achieved if networks can grow exceedingly large, as allowed for by the routing, or network. The ISO addressing structure will result in networks being able to expand to millions of nodes in size – well beyond the current network limit of 64,000.

Bank orders Philips Sopho-S

The Royal Bank of Scotland has become the first UK bank to choose a Philips digital PABX. The contract, worth over £300,000, is for a 1400 line Sopho-S 2500 machine which is the first of a planned network covering the bank's principal locations throughout the UK.

According to Allan Brownie, Project Leader in the bank's Telecommunications Planning Department, one of the factors influencing the decision was the Sopho-S's flexible approach to networking which offers several powerful methods for linking systems using digital or analogue circuits. "We also had to look to the future," he said; "in particular, the migration to digital public networks (ISDN) will occur during the life of the switch. Philips demonstrated that, because of its modern design, the Sopho-S can provide both internal ISDN facilities and connection to future networks."

Telecomms Topics is written by Adrian Morant.

Orbital elements

For readers who are not familiar with the terminology of orbiting satellites, and do not have text-books or dictionaries handy, the accompanying diagram may be helpful in understanding some of the more frequently used terms in this regular feature. The terminology is largly derived from that of lunar and planetary orbits.

Measurements defining the paths of artificial satellites orbiting the Earth are normally made with respect to the plane of the Earth's equator, or **equatorial plane.** This lies at an angle of 23.4° to the plane of the Solar system (e.g. as delineated by the path of the Earth about the sun), called the **ecliptic.** For simplicity the ecliptic plane is omitted here.

The diagram shows the Earth with two satellite orbits. The large, outer one is circular and lies on the Earth's equatorial plane. At an altitude of about 35,700 km above the equator this path would constitute a **geostationary orbit.** The inner one is an **elliptical orbit** and lies on an **orbital plane** which has an angle of **inclination** relative to the equatorial plane.

Where this orbital plane intersects with the equatorial plane a line is formed called the **line of nodes.** On this line the point where the satellite's orbit crosses the equator from south to north is the **ascending node,** while the opposite point where the same orbit crosses from north to south of the equator is the **descending node.**

In an elliptical orbit the point farthest from the Earth's centre is the **apogee,** while the point nearest to the Earth's centre is the **perigee.** A satellite travelling in such an orbit has its maximum **orbital velocity** at the perigee and minimum orbital velocity at the apogee. The time taken for a satellite to make one complete orbit around the Earth is the **orbital period.**

A **circular orbit** is considered as a special case of an elliptical orbit in which the **eccentricity** of the 'ellipse' is zero, so that the height of the orbit is constant. A **sun-synchronous orbit** is one in which the orbital plane remains at a constant angle to the sun while the Earth is moving round the sun.

Any single orbit of a satellite can be uniquely defined by six **orbital elements.** These measurements, listed below, are related to the equation of orbital motion given on p.159 of the February 1987 issue.

Semi-major axis of the ellipse is one of two orbital elements which give the size and shape of the orbit. This distance is defined as half the length of the major axis of the ellipse.

Eccentricity of the ellipse is the second element giving size and shape information. It is a measure of the amount of elongation of the elliptical orbit and is a number equal to the distance between the ellipse foci divided by the length of the ellipse major axis. For elliptical orbits this number is always less than unity (e.g. the eccentricity of the moon's nearly circular orbit round the Earth is 0.0549).

Inclination is the angle between the orbital plane and the equatorial plane.

Longitude of ascending node fixes the orbital plane with respect to zero degrees longitude. It is the angle of longitude of the point at which the orbit passes through the ascending node.

Argument of perigee is an angle specifying the position of the perigee and hence the orientation of the orbit in the orbital plane. It is the angular distance of the perigee from the ascending node on the orbital plane.

Time of passing perigee. This orbital element determines the position of the satellite within its orbit. The interval between two consecutive times of passage is, of course, the orbital period.

The position of the orbital plane with respect to the 'fixed' stars can also be defined by measurements.

Molniya orbits for car and mobile radio?

West European researchers are now looking afresh at highly elliptical orbits of the type used by the Soviet Union since 1965 for its Molniya ("Lightning") comsats. They have in mind the advantages of this kind of orbit for both sound broadcasting and land mobile radio, particularly in North European and other high-latitude countries. Sound broadcasting has to provide a good service to car radios, especially in the richer countries, and here the reception problems and equipment/price constraints are similar to those of land mobile radio.

The highly elliptical orbit used by the Russian Molniya comsats has an orbital plane with an inclination of 63.4° and an apogee at about 40,000 km (see item on 'Orbital elements'). This apogee lies above the USSR while the perigee, only about 500 km high, is above the Earth's southern hemisphere. Several series of these comsats have been in operation over the years.

A Molniya satellite's orbital period is 12 hours, so each spacecraft appears above a given place at the same times every day, but of course it has to be tracked by the earth stations as it passes overhead. In fact each satellite is visible for about 8 hours over the service area concerned (the velocity being slowest at the apogee end of the orbit). So several of them are used, following one after another in the same orbit, to provide continuous communications coverage throughout the 24-hour day. Typically four are used, travelling at intervals of 90° or 6 hours.

The principal advantage of the Molniya orbit for northern regions is that the satellite appears directly overhead. This means that earth station antennas, whether fixed or on vehicles, are pointed upwards with a high angle of elevation. Line-of-sight is direct with no solid obstacles and a minimum of atmosphere to pass through. In contrast, comsats in the geostationary orbit are a long way south from these regions. Consequently earth antennas must be pointed at low angles of elevation, so that their beams may well encounter obstacles such as buildings or trees and pass through a greater length of atmosphere and rain.

Antennas on vehicles need to be as small and simple as possible. It would be extremely difficult for an antenna on a moving vehicle, travelling in varying directions over changing terrain, to continuously track a geostationary satellite positioned somewhere above the southern horizon. With the Molniya type of orbit, however, the antenna could be a low-gain, broad beamwidth design mounted on the roof of the vehicle and pointing more-or-less vertically upwards.

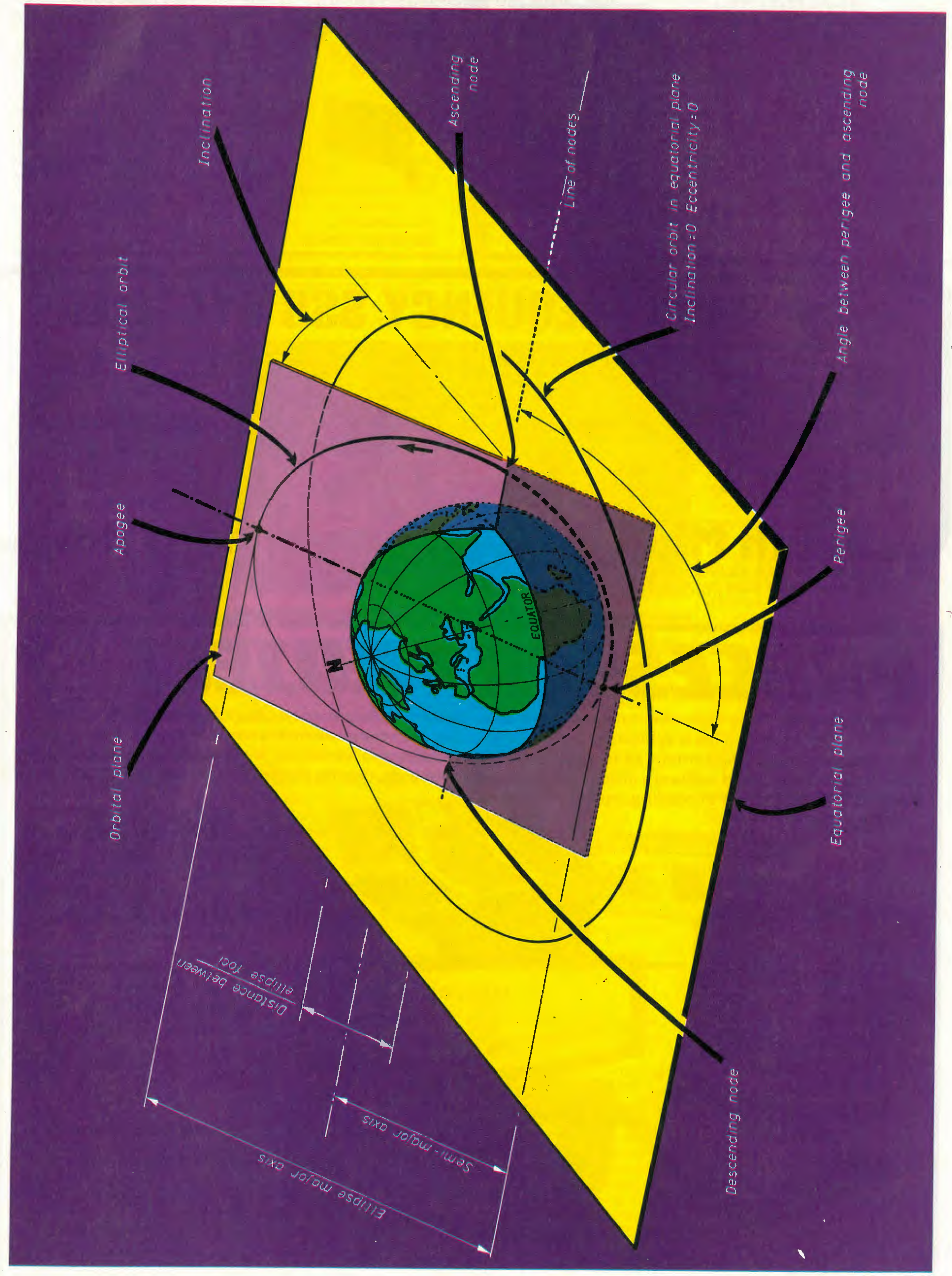
The European Space Agency is one organization interested in the possibilities of such elliptical orbits for land mobile satellite communications. It has recently commissioned British Aerospace to lead a feasibility study for a comsat system for mobile users including occupants of trucks, cars and other vehicles. The study will investigate a number of elliptical orbits, including the Molniya one, and will take eight months. As part of it, Racal-Decca will look into the design of a mobile terminal and the possible application of such orbits for terrestrial navigation.

As for sound broadcasting to car radios via satellites, the BBC Research Department has studied this idea as an important part of the general possibility of using d.b.s. for sound radio alone. A discussion paper on the subject was presented by J. H. Stott at the 1986 International Broadcasting Convention in Brighton. In general he felt that the method had advantages over terrestrial sound broadcasting in two respects. For developing countries it avoided the difficulties of building up a network of transmitters. For developed countries it offered the possibility of using digital modulation techniques and a chance to provide new services with better sound quality and greater flexibility.

Among other technical factors, the paper dicussed antenna gain and link margin in relation to car radio. The link margin, measured in dB, is a 'safety factor' included in the power budgets of satcom links to allow for the propagation losses resulting from obstacles and absorption in the line-of-sight to the satellite. Its value depends on antenna beam elevation, among other things. Mr Stott said that the advantage of the high elevation resulting from Molniya type orbits was not confined to the link margin. Not only was the link margin less for high elevations but the receiving antenna could have a greater gain as well.

Satellite Systems is written by Tom Ivall.

SATELLITE SYSTEMS



NEW PRODUCTS

Fast recovery for power transistors

Power darlington transistor modules in the Semikron SK-DB range have the addition of 100 and 150A versions. The new transistor modules incorporate a parallel-connected fast-recovery inverse diode to minimize the need for additional external components. Available with voltage ratings of 600 or 1000V, the modules are suitable for high-power switching applications in uninterruptible power supplies, d.c. servo and robot drives, and a.c. motor controls.

The modules feature an isolated metal baseplate to simplify the mounting of one or several modules on to a heatsink, and all electrical connections are situated on top of the package to facilitate interconnection to busbars or p.c.bs. Semikron Ltd, 4 Marshgate Drive, Hertford SG13 7BQ.

Service tool-kit for electronics

An electronic servicing kit includes a range of integrated-circuit handling tools as well as screwdrivers and nutdrivers. The CSK-8 kit contains an i.c. insertion tool with pin straighteners for 14-16pin devices, a three-claw parts holder, assembly tweezers, a selection of screwdrivers, two nutdrivers, and a torque screwdriver.

The kit is supplied in a zipped vinyl case measuring 9 × 6 × 1½in, and costs £22.50. Global Specialties, Shire Hill Industrial Estate, Saffron Walden, Essex, CB11 3AQ.

Infra red detectors

The devices in the LTR500 range of infra-red detector diodes are housed in opaque plastics packages to eliminate interference from stray visible light. Sensitivity of these devices is maximum at a wavelength of 950nm and their fast risetime of 50ns and low inherent capacitance of 25pF makes them suitable for switching at megahertz frequencies. Design of the drive circuitry is simple; typically, a photocurrent of 40μA is produced at a luminance level of only 1mW/cm^2. Sensitivity and all other electrical parameters are warranted at a cumulative AQL of 65% as a result of 100% testing.

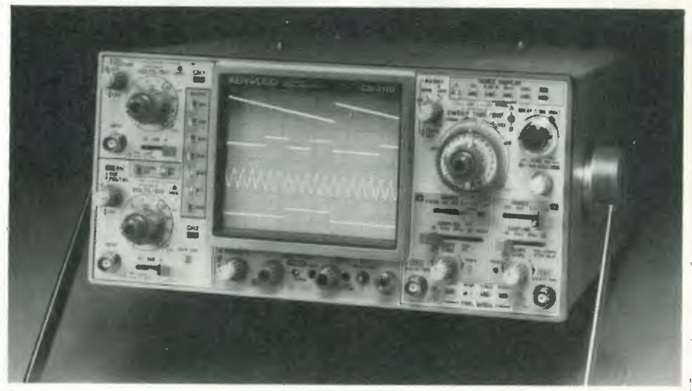
Three versions are available: LTR526 is housed in a TO72-style D-package, LTR536 is in a top-sensitive rectangular pack and LTR546 is the corresponding rectangular device with the diode oriented sideways. All withstand the typical flow-solder temperature of 260°C for five seconds. Selectronic Ltd, 46 Market Square, Witney, Oxon, OX8 6AL. Tel: 0993 73888.

Four-channel 100MHz oscilloscope

The Kenwood CS-2110 is a low-cost 100MHz oscilloscope with four input channels. Each channel has its own vertical position control, and accurate timing measurements are assured by guaranteed time differences figures of less than 0.5ns between the first two channels and less than 1ns for channels 1 and 2 to channels 3 and 4.

The CS-2110 has a maximum 'sensitivity' of 1mV/div and a maximum sweep 'speed' of 2ns/div. Full dual timebases with separate and comprehensive controls for the B trigger signal are provided. Alternate sweep operation, with optional 'B ends A', provides a convenient method of viewing both the expanded and non-expanded waveforms simultaneously.

A 20kV acceleration potential provides a sharp, high-intensity trace even in bright lighting conditions and with low duty cycle waveforms. The rear panel sockets include an intensity input, a channel 1 output socket for driving a frequency counter, and gate signals for the A and B timebases. A calibration loop is also provided for use with the current probes. The auto-switching power supply unit can operate from line voltages between 90 and 264V without adjustment. Thurlby Electronics Ltd, New Road, St. Ives, Huntingdon PE17 4BG. Tel: 0480 63570.



Computer chip with eprom and 6502 codes

Erasable and non-erasable prom versions of the Mitsubishi M50747 have become available. Using 6502 architecture the single-chip computer offers engineers easy access to the application of such devices.

The M50747 features: 256bytes of ram, 40 data programmable i/o lines, eight input and eight output lines, uart with data rate generator, two eight bit timers with prescalers and 8Kbytes of r.o.m.

Development support includes a range of assemblers to run on PCs, a 740 series designers' board based on the M50734 extended microprocessor part from the same family and tools for in circuit emulation in conjunction with a PC host.

To assist designers in applying these devices RCS Microsystems are offering the M50747 designer's kit which provides a ceramic-window version of the part, a programming adaptor which allows it to be programmed as a 2764, and a pitch converter, to simplify prototyping with a standard matrix board. The kit which includes full documentation is on offer at an introductory price of £99.50. RCS Microsystems Ltd, 141 Uxbridge Road, Hampton Hill, Middx TW12 1BL.

Compact control computer

Siemens' SKC 515 single board computer is based on the 80515 8-bit micro-controller. It has six 8-bit ports for input/output; two being isolated via opto-couplers. There are eight multiplexed analogue/digital inputs and a real-time clock. Memory capacity extends to 64K bytes of eprom and 8K bytes of cmos ram.

The 80515 allows reductions in circuit complexity to be made compared with the 8051. Integrated on the chip are three 16-bit timers, seven external interrupts, four priority levels, an a/d convertor, as well as multiplexers and registers. Also provided are the ram (256-bit) rom (8Kbyte).

To simulate an eprom version of the 80515, a processor module can be used in a 68-pin socket. The serial interface is RS232 or 20mA loop; two 64-way DIN connectors serve as the hardware interface. Isolation of the two input/output ports ensures that voltage peaks in the controlled peripherals cannot interfere with the operation of the board. Siemens Ltd, Windmill Road, Sunbury on Thames, Middlesex TW16 7HS.

Low cost 2GHz signal generator

A new 2GHz signal generator is thought to be the first to use single-loop phase-lock technology and a low-frequency direct digital synthesizer to provide outstanding performance at a very low price.

Model 2520 offers the frequency accuracy, stability and programmability previously only available in high-cost laboratory type synthesizers. It features a broad range of output power, from -137 to +13dBm, making the instrument suitable for driving high-level mixers or for testing low-level receiver sensitivity, with a resolution of 0.1dB throughout the full range of output levels. It has an error of 0.00025% over a 0 to 50°C operating range. Higher stability references to 0.00001% are available as options.

Both internal and external amplitude and frequency modulation capability are standard features with phase, pulse and f.s.k. modulations as options.

The instrument features a wide range of self-diagnostic and calibration routines. Autocal mode accesses a machine-prompted calibration procedure for frequency, deviation, and output level. This extends the laboratory interval to the allowable drift of the crystal reference.

Frequently used test parameters may be stored and recalled from 64 non-volatile ram locations. Remote programming of the instrument is possible via an optional GPIB which controls all functions except on/off, Autocal and diagnostics. Wavetek Electronics Ltd, Tag Lane, Hatch, Reading, Berks RG10 9LT. Tel: 073522-4121.

Surface mount flux

A non-corrosive flux paste specifically designed for surface-mount applications is thixotropic and remains tacky for several hours after application, unlike conventional fluxes. Populated boards may be handled without disturbance. The flux, Tacflux, does not dry out, disperse or shrink. It holds components firmly according to Dage and maintains registration, permitting delayed reflow.

Rosin-based Tacflux is suitable for small or large production batches and useful in repair situations. Application methods include screening, dispensing, and stencilling.

The flux is supplied in 25, 50, and 1000g sealed, manual or auto-dispense cartridges. It is available in standard and high-tack options. Flashpoint is 78°C. Dage (GB) Ltd, Intersem Division, Rabans Lane, Aylesbury, Bucks, HP19 3RG. Tel: 0296 393200.

Graphics computer on a single board

A high performance single-board graphics computer from Micro Concepts combines a 68010 16/32-bit processor with the Intel 82786 graphics coprocessor. Called Image-10 it packs all the components of a complete computer system onto a standard double Eurocoard-sized board at the price of many less capable graphics-only boards.

Designed specifically for applications that demand high graphics performance in terms of speed, resolution and visual quality, Image-10 is claimed to provide the graphics capability formerly available only on expensive workstations and dedicated graphic subsystems. The board provides variable resolutions up to 768 by 576 points with the number of displayed colours being selected by the user from a choice of up to 256 from a total palette of 256,000. Drawing operations are performed by the dedicated 16-bit graphics processor within the 82786, minimizing overheads on the 68010 c.p.u. Functions supported by the graphics processor include: point, line, arc, circle, polygon and polyline operations with facilities to define colour, logical operation, texture and clipping. Bit block transfers within windows or between memory and windows allow fast image manipulation.

A second 16-bit processor within the 82786 is dedicated to video generation including the maintainance of an almost unlimited number of displayed windows at speeds up to 100 times faster than by traditional software methods.

Included as standard are all the other circuit modules required of a complete single-board computer design including 576K bytes of ram and provision for up to 256K of eprom. Another version of the board will have 2Mbytes of ram.

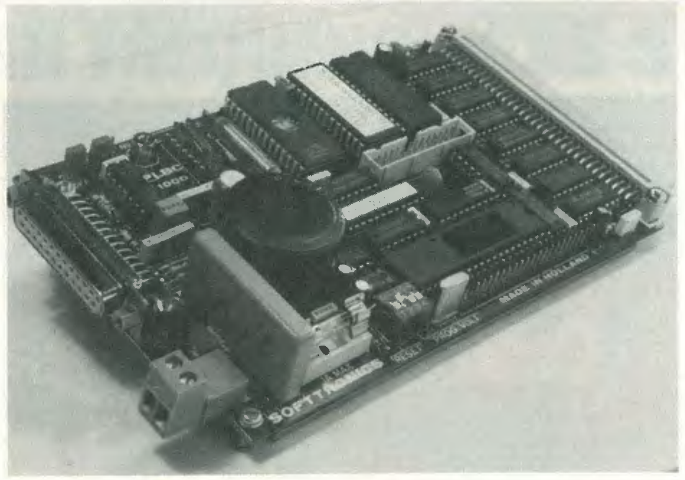
Mass storage is catered for by interfaces for two floppy disc drives and a hard disc drive. Of particular interest is the inclusion on the board of an Inmos 20Mbit/s serial link enabling the Image-10 board to communicate with Transputer based systems. Additional i/o is catered for by a full 16-bit buffered expansion bus. A battery backed realtime clock/calendar and stereo sound generator complete the hardware facilities.

The board is supplied with firmware containing system services, diagnostics and utilities including facilites to download programs from a host development system. Alternatively it can be used as its own development system with a choice of popular disc operating systems. Currently running on the board are OS-9/68000, and CP/M-68K. Micro Concepts, 2 St Stephens Road, Cheltenham, Glos. Tel: 0242 510525

Programmable logic basic controller

An industrial single board controller from Softtronics, Netherlands, can be programmed on an IBM/PC. Based on Intel's 8052 c.p.u. the PLBC1000 development computer features two RS232 ports for terminal and printer, autodata-selection up to 9600baud (XON/XOFF), 24Kbyte sram on board, 38 cmos inputs, 24 t.t.l or o.c. outputs, and an eprom programmer for 32Kbyte eproms. The PLBC1000 is equipped with a line-up and stabilization circuit.

The 8052AH Basic c.p.u. has a full 8Kbyte interpreter designed for process control and instrumentation. Programs can be stored in eprom to create systems which autostart from power-up. The Softtronic Basic statements are specially designed for interfacing keypad and dot-matrix l.c.d. modules to enter and display process values. A simple Basic statement can make them behave as standard i/o devices. For communication handling with IBM PC a special software package is available. Softtronics, Dr Schaepmanstraat 38, 7557 JC Hengelo (o), Netherlands.



Low cost STEbus s.b.c.

A powerful 8-bit 8052 c.p.u. with built-in Basic, four memory sockets, eprom programmer and serial i/o are combined on Arcom's new SC52 STEbus board. The module offers all the facilities necessary to implement a simple control system, with unlimited expansion potential via the STEbus interface for more complex applications. Moreover, programs can be developed and blown into Eprom using the board's built-in Basic interpreter and Eprom programmer. All that is needed to develop target system code is access to a standard v.d.u. and a working knowledge of Basic.

The module provides a low cost solution for simple applications, and a learning vehicle for companies new to STEbus or processor-based systems design. At £212, the SC52 is claimed to be the lowest-cost complete entry to STEbus applications available anywhere.

SC52 is based around Intel's new 8052AHBASIC, a mask-programmed version of the 8052 single-chip microcomputer with an 8k Basic interpreter. This chip also offers 256 bytes ram, three counter-timers, a u.a.r.t, and interrupt inputs. Arcom integrates it onto a single STEbus Eurocard with four 28-pin eprom sockets, a high-voltage regulator for on-board programming, RS232 lines to a terminal, a serial printer port, and an STEbus interface. The SC52 is designed to perform asychronous STEbus accesses to data memory and i/o.

The resident Basic interpreter offers full floating point capability, trig. functions, the ability to deal with interrupts, an internal realtime clock, and eprom programming algorithms. Its 'tokenized' operation provides a dramatic increase in execution speed. Arcom Control Systems, Unit 8 Clifton Road, Cambridge CB1 4WH. Tel: 0223 411200

Communication board doubles STE i/o capacity

A high-performance serial communications board offers on a single Eurocard eight RS423 channels, effectively doubling the i/o capability of any single slot on the STEbus. The board is based on the Zilog 8350 serial communcications controller and provides protocols and synchronous clock capabilities on all eight channels and supports vectored and non-vectored interrupts. The integrated circuits can cope with a varitey of synchronous and non-synchronous protocols and include digital p.l.l. data recovery as well as n.r.z.i., f.m. and Manchester data coding with a Baud-rate generator of wide range. DSP Design Ltd, 100 St Pancras Way, London NW1 9ES. Tel: 01-482 1773.

S.b.c. with 386 for Multibus II

High-performance multiprocessing capabilities are possible with the M-CP 386/016 single-board computer.

The board is built around the Intel 80386 processor operating at 16MHz and offering a data transfer rate of up to 32Mbyte/s. The processor incorporates a memory mangagement unit and all devic access routines can be pipelined. Also on the board is a direct memory access controller, a floating-point coprocessor, sockets for up to 1Mbyte of eprom and eight more for 1MByte of no wait sram. A message-passing processor, dual-port memory, and on-board extension slots for extra memory provide full Multibus II facilities. Concurrent Technologies Ltd, Fairfax House, Causton Road, Colchester, Essex CO1 1RJ. Tel: 0206 42996.

Designers' board

For engineers to be able to get a system 'up and running' in as short a time as possible, RCS Microsystems have come up with their 50734 Designers board, based on the Mitsubishi M50734. The board may be used with any of the 740 series of single-chip computers for the purpose of evaluation and development.

The 50734 board consists of the processor, an address latch, address decode, 8Kbyte ram, 16Kbyte eprom which contains a 2Kbyte monitor program, clock circuit, reset circuit with systems watchdog, RS232 interface and voltage regulators. Several i/o sockets allow for system expansion and are provided with data and address lines, chip-select and control signals. The onboard ram is battery backed.

The monitor provides the usual de-bug facilities including memory and register examination and alteration, starting a program from a specific address, break-point setting, up and downloading of programs and data, and some extra utilities such as converting between decimal, hex, and ASCII formats.
RCS Microsystems TW12 2BL.
Tel: 01-979 2204.

Futurebus backplanes

The first in a range of hardware support for Futurebus, from BICC-Vero, are the 10 and 21-slot backplanes. Other slot widths are currently being designed and are to follow.

Complying fully with IEEE P890 draft 7.5 the Futurebus backplanes offer the reliability of multilayer construction, and the constant characteristic impedance of buried microstrip signal tracks which, in addition, are screened by 'guard tracks'.

The backplanes are fitted with pressfit 96/96 way connectors along with 6.3 mm (0.25in) tab connectors for power pick-up. "Off-board" termination is incorporated, with rear-pluggable terminator modules available separately.

Futurebus is architecture and processor-independent and uses a true asynchronous protocol as the means to preserve technology independence – giving it its attractive 'futureproof' feature. BICC-Vero Electronics Ltd, Flanders Road, Hedge End, Southampton SO3 3LG. Tel: (0703) 266300.

6809 board with video controller

The single-board computer from Dominic Evans Industries is claimed to break new ground in Eurocard systems. The board is intended for industrial control systems, colour display systems or terminals.

A single Eurocard includes the 68B09 processor, clocked at 8MHz, a 40/80-column semi-graphic colour display controller with 8K of private ram, 32Kbyte of non-volatile ram, 32Kbytes of eprom, real-time clock/calendar, RS232/485 serial port, parallel printer port and an l.c.d. display driver with an i/o port for keyboard connection.

A monitoring watchdog ensures the correct operation of the power supply and software and there is also an eprom-based de-bug monitor.

A fully buffered systems bus allows for expansion. Memory boards up to 1MByte can be plugged in as well as digital or analogue i/o cards and others. Dominic Evans Industries, Systems Division, AAC Building, Leighswood Grove, Aldridge, Walsall, W.Midlands WS9 8SY.
Tel: 0922 57853.

PC into supercomputer?

The addition of a co-processor board to an IBM PC (or clone) can turn it into a computer capable of running at 4 to 8 mips. The particular co-procssor that makes this possible is the Novix NC4016 chip (as featured in this journal earlier this year). The chip was designed by Forth Inc and runs the high-level language. Forth as to operating language. This and the parallel processing structure within the device is what gives it the speed. Complex instructions can be completed in a single clock cycle.

The board that incorporates the chip, PC4000 inlcludes seperate memories for the data and return stacks as well as 512Kbytes of d.ram. A multiplexer, bus arbitration logic and buffers are used for communicating with the IBM i/o bus. PCX software is used for the development and running of user programs as well as the comunications between the PC and the board.

Up to six of the PC4000 boards can be run in paralled. With all six running it is possible to achieve speeds of up to 40mips, claimed to be six times as fast as a Cray II. The software can be configured to run other high-level languages and a version of C (Sc-C) has been developed to take full advantage of the board's speed. On a PC-AT, such programs can be run as background tasks. Silicon Composers, 210 California Avenue, Suite K, Palo Alto, CA 94306. Also available in the UK through Computer Solutions Ltd, Tel: 09323 52744.

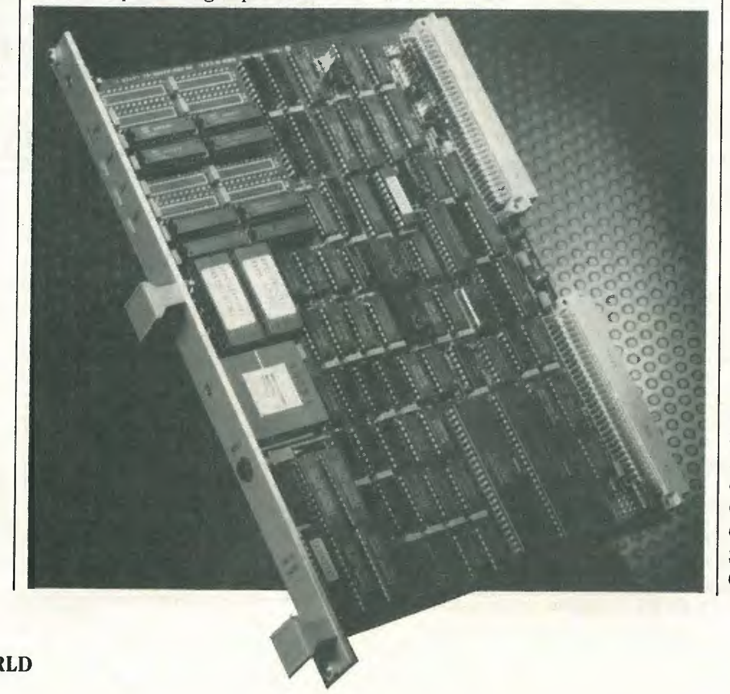
Ten mips VME bus s.b.c.

The V4000 s.b.c. is claimed to be the only single board computer to provide 10 mips performance, specifically targeted to real-time, embedded processor applications. The computer is made in the USA by VME Inc. It is a standard, double-height VMEbus card that occupies only one card slot. Based on the Novix stack-oriented microprocessor, it is the first in a family of VME boards designed to implement the high level Forth computer language for the VMEbus. The cmFORTH language is provided as standard, together with optimising compiler and software development tools, while polyFORTH, with many extras, can be supplied as an option.

Combining on-board multi-tasking facilities with full VMEbus master and slave capabilities, all integrated onto a single board, the V4000 permits the user to create a significant number of separate, interrrupt-driven tasks to support real-time processing requirements (15 to 20 in a typical application). It can switch tasks in less than 5µs, whereas standard VMEbus processors can take more than 30 times longer.

Aimed at high speed data acquisition, machine control and robotics applications, the V4000 includes serial and parallel i/o, timer, local program and data storage, as well as VMEbus system controller functions and full interrupt and interrupt handler facilities, which support multi-master configurations.

As a VMEbus master, the V4000 can access any address modifier set in the 16M byte global memory (including block transfer) and will perform program i/o transfers at up to 4M bytes per second. As a VMEbus slave, the V4000 dual ports all on-board data and program memory asynchronously, thus supporting high speed d.m.a. operations. Computer Solutions Ltd, Canada Road, Byfleet, Surrey. KT14 7HQ. Tel: 09232 52744.



Upgrade for Solo control computer

An improved version of the Kemitron Solo computer features a new single board processor which holds all of the basic computing components. This includes a Z80A processor, memory, serial ports, real time clock, counter timers and disc controller.

A single 3.5in microfloppy disc with 600Kbyte is fitted as standard although a twin disc option is available. Whatever the format, CP/M provides the operating system which can also support hard discs.

Solo is packaged in a small metal case with optional carrying handle. As well as the new processor card, power supply and floppy disc this houses a six-slot backplane allowing i/o cards to be plugged into the back of the unit. Cards available include digital cards with opto-isolation, Darlington drivers, pulse counter timers and serial communications. Analogue input and output cards are also available, and a number of specialist cards with high-speed converters, thermocouple inputs and strain gauge conditioning.

Kemitron claims that using its multi-function board increased reliability and reduces cost, They have datasheets on the computer and plug-in input/output boards. Kemitron Ltd, Hawarden Industrial Park, Manor Lane, Deeside, Clwyd CH5 3PP. Tel: 0224 536123.

Relay Ladder

A specific language, 'Relay Ladder' has been developed by Cavendish Automation for their range of industrial controllers.

The c.p.u. is designed to stand alone and can be programmed via its serial port, taking advantage of direct connection to any computer terminal. As well as most standard commands available on modern controllers, the Cavendish card has additional commands and a number of other advantages, particularly its flexibility, in that it will allow the programmer to escape from Ladder language into user-defined code. This enables a Relay Ladder sequence, for example, to be easily integrated with l.c.ds or keyboard scans, and other devices.

The standard package allows 2000 programme lines, 60 timers, 60 counters and 144 output channels (72 implemented on card), each of which can be designated as an input or output, using the same pin under software control. CA provides numerous types of digital and analogue interface cards, and the Relay Ladder package is fully compatible with all cards in the Cavendish Automation 7000 Series. Cavendish Automation, 45 High Street, St. Neots, Huntingdon, Cambs PE19 1BN. Tel: 0480 219457.

NEW PRODUCTS

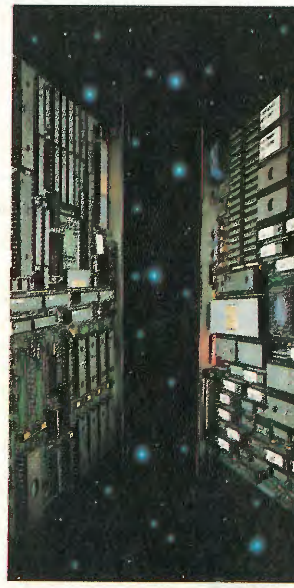
High-speed single board computer

Ultra-high speed data movement is possible with the GMSV07 single board computer, claimed to offer performance of a minicomputer at a fraction of the cost.

Based on the 32-bit 68020 and running at 20MHz, the board features up to 1Mbyte no-wait-state RAM, optional advanced memory management and high-speed floating point maths. A real-time clock calendar is standard. Plug-in options provide VSB(MVMX32) compatibility, as well as a wide range of i/o possibilities.

Available software includes self-test diagnostics, debugger, PDOS, Uniflex, Unix and Forth.

Universal Engineering and Computing Systems Limited, 5 Tower Street, Newtown, Birmingham B19 3UY. Tel: 021-359 1749.



Versatile board for real-time computing

The HVME-SB68S is a general-purpose board designed for real-time computing environments. It provides a versatile i/o bus particularly suited to disk drive, back-up and graphics peripherals.

The board is 68010-based and runs at 10MHz or 12.5MHz with no-wait states, from 512Kbyte or 1Mbyte of dynamic ram. features include SCSI interface, parallel printer port, four independent timers, three level bus arbiter and seven level interrupt handler. A 68881 floating point coprocessor is an option. 265Kbytes of eprom can be installed, and 8Kbytes of battery-backed s.ram is available.

High Technology Electronics Ltd, 303 Portswood Road, Southampton SO2 1LD. Tel: (0703) 581555.

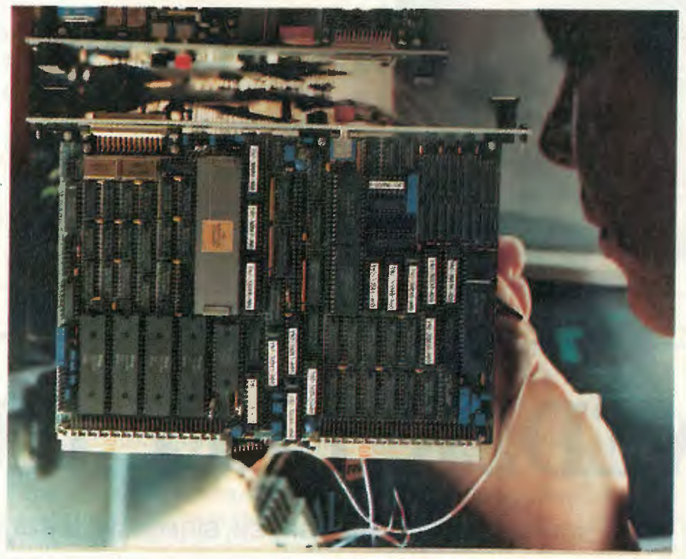
Fast communications on VME

A 68010 processor and 520Kbyte of ram are included on the VME input/output card from HTEC. This running at 10MHz, allows the card to achieve what is claimed to be the fastest synchronous communications available for the VME bus. The HVME-SERO8 is functionally compatible with the MVME331/333, but offers two extra ports, improved performance and the advantage of no wait, dual-port ram. Applications include interprocessor communications, message switching and message routing.

Serial communications are handled by four Z8530 controllers providing eight channels configured by the user. One channel can be used to connect to a terminal for debugging. Any of the ports can be used to support multi-protocol synchronous or asynchronous communication at data rates of up to 1Mbit/s. Optimum speed for the simultaneous operation of all eight channels is 9600bit/s.

Priority is given to local use of the on-board ram and there is additional space for more ram and rom.

The board can be used in a VME chain as either a master or slave as part of a multiprocessor system. Options include a d.m.a. controller, a floating-point processor and an X.25 communications port. HTEC Ltd, 303 Portswood Road, Southampton SO2 1LD. Tel: 0703 581555.



STE-bus master card

Titan is the first of a series of STE-bus processor cards. It is based on the Z-80-compatible HD64180 processor and incorporates an STE system controller and interface, together with two serial communications channels on a single Eurocard. It has provision for a battery-backed real-time clock, sockets for three memory devices and a maths coprocessor. The system can access the full 1Mbyte of memory and has access to the 4049 i/o locations of the STE system.

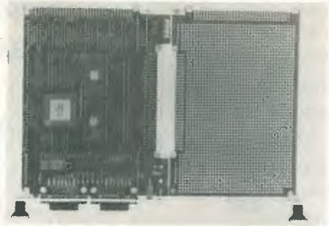
Titan can be used as an intergrated processor for the bus, or, combined with a Booster add-on card can form a complete development system with floppy and hard disc interfaces, a printer port and up to 1Mbyte of memory.

The Hitachi processor adds 2 d.m.a. channels and the wider memory access to the Z80 architecture. It can operate at 6MHz with a 9MHz version in the offing, providing three times the processing speed of the Z80.

Software support is provided by Industrial Basic for the rapid development of applications. Booster-card versions can run 'Z-system' a successor to CP/M. Such a combination can also run Turbo Modula-2 language and has a wide range of utilities readily available. JB Design Ltd, 15 Market Street, Cirencester, Glos GL7 2PB. Tel: 0285 68122.

Video amplifier chip

A two-channel video amplifier/multiplexer from Hitachi has a 100MHz bandwidth and is intended to simplify the mixing of standard and graphic video signals. The device (HA11505) has been designed to offer on-screen functions for high-resolution display systems and includes a high output current (250mA) and a special contrast circuit. One of the major benefits of the new amplifier is that its low impedence output can directly drive video transistors, thus enabling designers to produce system with fewer components. The amplifier offers direct video feedback leading to a higly stable video output signal. The dual video signal input greatly simplifies video selection/mixing. The device will find applications in any system that has a high resolution display, such as a v.t.r. mixer, where it can offer on-screen display functions including, for example, transparent graphics windows. Hitachi Electronic Components (UK) Ltd, 21 Upton Road, Watford, Herts WD1 7TB. Tel: 0923 246488.



VME board for asics

Two boards, mother and daughter, linked by a 96-way connector, provide a test-bed for application-specific i.c.s. The mother board conforms to Thomson's 'intelligent peripheral controller' architecture and includes a 68010 processor running at 10MHz with 64Kbytes of no-wait-state ram, six 28-pin sockets for furthe ram/rom and two RS232 ports. The prototyping daughter board has access to all the processor's buffered signal and a number of addition pre-coded signals. Wire-wrap versions of the daughter board are available. The TSVME controller is made by Thomson Microsystems and is available through Pronto Electronics Systems Ltd. Orbit House, Heyes Lane, Alderley Edge, Cheshire SK9 7LW. Tel: 0625 582637.

RADIO BROADCAST

A.m. stereo for Europe?

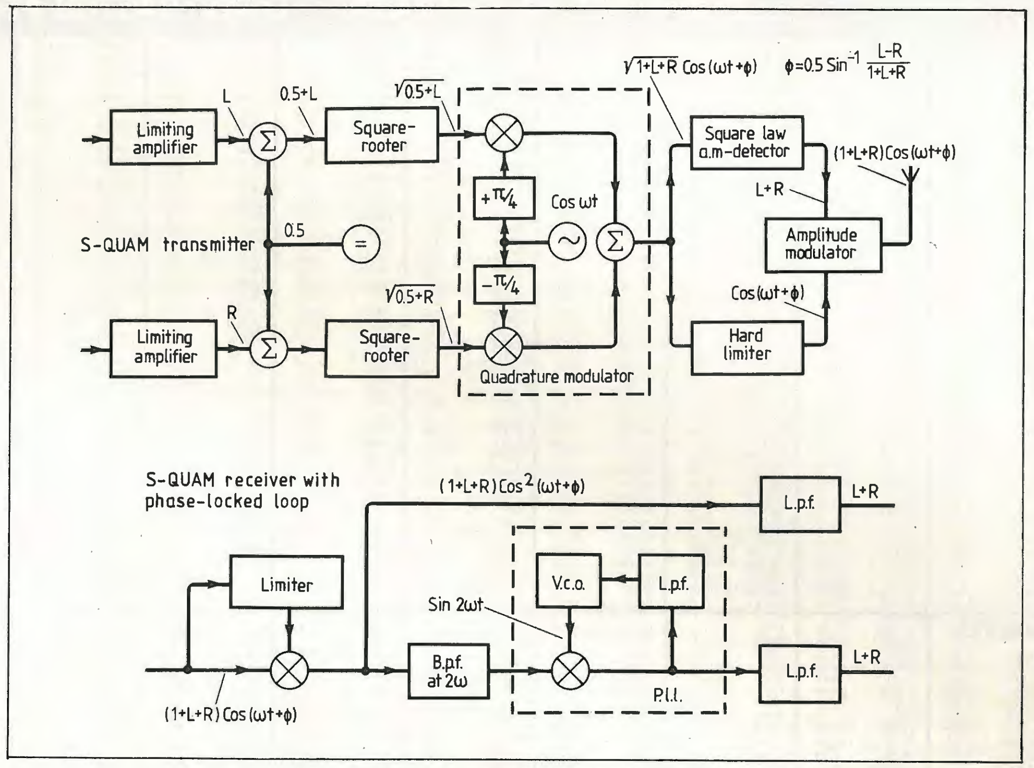
In 1982, the FCC formally authorized American radio stations to begin using stereo on medium-wave stations while leaving it to the market place to choose between four largely non-compatible systems developed by Harris, Kahn/Hazeltine, Motorola and Magnavox. This followed an abortive earlier attempt to standardize on Magnavox.

The refusal to specify a single technical standard slowed the general acceptance of a.m. stereo. However the Motorola C-QUAM system (which had come third in the FCC's own assessment) has gradually established itself as the leading system in many US cities and also in Australia and South America. C-QUAM is based on amplitude modulation of two carriers separated in phase by 90°, using non-linear hard limiting to improve mono compatibility.

The crowded state of the medium-wave band, the widespread use of simulcasting (duplication of the same programmes on v.h.f. stereo and m.f./l.f. mono), the widespread use of 5kHz cut-off filtering on m.f. and the 9kHz carrier separation between channels (compared to 10kHz in the Americas) have all combined to dampen, almost to vanishing point, interest in a.m.-stereo in Europe. However, the Home Office consultative document "Radio: Choice and Opportunities" (HMSO, Cm 92) firmly recommended the ending of simulcasting in the UK within the next few years. With the majority of listening (an overwhelming majority in the case of in-car entertainment) is still on medium/long waves, this recommendation, if implemented, seems likely to renew interest in a.m. stereo in the UK.

In 1983, the Polish radio engineer, Andrzej Lugowski, submitted to the FCC "A proposed stereophonic system for a.m. broadcasting" recently published in *IEEE Transactions on broadcasting*, June 1987, pages 43 to 47. This system, designated S-QUAM, would he claims, offer useful advantages for European broadcasting. It is a compatible system, utilizing quadrature modulation and suitable for stereo recovery with the aid of either a Costas detector or a phase-locked loop. It belongs to the non-linear group of systems with the phase deviation reduced. The primary aim is to reduce the disadvantages connected with the use of an a.m. stereo transmission based on the non-linear approach.

The American systems include both linear and non-linear systems. The Harris system, for example, is a linear system but in all such systems the maximum phase deviation has had to be narrowed in order to improve the monophonic compatibility of the envelope; the Polish proposal belongs to the non-linear group with the phase deviation similarly reduced by this time to decrease undesirable out-of-band radiation. It produces a signal with a compatible envelope featuring a negligibly low-level of out-of-band radiation but, owing to the quadrature modulation, maintains the desired noise characteristics. This, it is claimed, makes the system more suitable for use in Europe, where the high level of radio interference and narrow bandwidths have tended to create opposition to the introduction of a.m. stereo. Andrzej Lugowski believes that the introduction of this system would not impair existing monophonic reception but, on the contrary, add a new dimension to a.m. broadcasting.



Flea-power broadcasting

A few years ago the Home Office agreed to authorize, on an experimental basis, a limited number of 'special-event' stations permitting the use of low-power, medium-wave transmitters at events where conventional public-address facilities were of restricted value because of the high cost of cabling large areas for a temporary event. The stringent power restrictions (usually 50 milliwatts e.m.r.p. or less), the equipment and installation cost of a flexible broadcast facility and the hassle over licences have tended to limit the number of stations.

Norman McLeod of Wireless Workshop, Brighton, has recently sent an interesting report of the experience of providing technical facilities for "Radio Sandhurst", organized by Studio 6 Marketing in conjunction with the periodical *Yachting World* throughout Cowes Week. His firm, with experience of providing such facilities at about 15 special event stations, has an ex-library van (a large windowed vehicle) converted to provide studio, reception and hospitality areas.

At Cowes, this was authorized to broadcast daily (8am to 8pm) throughout Cowes Week on 1602 kHz but the power was limited to a minuscule 25mW, limiting reception to a small part of Cowes. Some listeners less than a mile from the transmitter experienced reception difficulties. The 66dBμ contour enclosed less than one-fifth of the town.

It is difficult to understand why such special-event facilities should be regarded by the Home Office as little more than a glorified non-wired public address facility. There appears to be a marked reluctance to issue permits for events where the public interest cannot be clearly marked off by a fixed boundary as, for example, at a racecourse. The first special-event station, before the introduction of the special permits, was for the Liverpool Garden Festival and involved an IBA transmitter providing almost 1 kilowatt to an 80ft mast. Why a professionally equipped and manned facility, subject to DTI inspection, for an event of considerable interest to the local townsfolk and beyond should be limited to a radiated power of only 25 milliwatts seems a remarkable example of bureaucracy triumphing over common sense.

Radio Broadcast was written by Pat Hawker.

TELEVISION BROADCAST

At the crossroads

Television broadcasters in the UK still seem worried out of their wits over the future impact of 'new technology' and government intervention. Few seem prepared to admit that change tends to occur relatively slowly and that the most successful innovations, such as Channel 4, are those for which viewers need no new equipment.

Cable and the video recorder have both found wide acceptance in some countries, including the USA where more than half the homes are cabled, half have video recorders, and many have both. The video disc has so far had virtually no impact and it is questionable whether the introduction of CDV with five minutes of video on what is basically a 5-inch CD audio disc will pave the way for a revival of interest.

NHK in Japan, since 4 July, 1987, has at last become the first broadcaster to introduce an exclusive "d.b.s.-only" 24-hour service from 100-watt transponders to an initial 150,000 homes equipped to receive the earlier experimental and duplicated-terrestrial broadcasts. But in view of the widely-quoted BSB estimates of UK terminals costing initially £200, and reducing to £50 in volume production, it is interesting that a receiving system in Japan with a dish antenna less than one-metre in diameter and tuner still costs more than 200,000 Yen (over £850) with a forecast that mass production could cut this by half, still more than £400 for an NTSC-type unit.

But what has been the effect of cable and video recorders on the established American broadcasters? Undoubtedly their audience-share has declined, but only gradually and far from dramatically. *TV World* quotes the following data: 98% of US homes have television sets; 95% colour; 59% with two or more sets; 49% subscribe to basic cable channels; 27% subscribe to one or more premium cable channels; 2% have large satellite dishes aimed at C-band distribution satellites. In May, adults viewed for an average of 4h 5min daily, teenagers for 2h 45min, children for 2h 47min. During prime-time (evenings) 69% of the audience watched the networks, 21% the "independents", 4% the "public broadcast stations", 9% basic cable channels and 5% pay (premium) cable channels.

Thus while the former overwhelming dominance of the major networks has been reduced, they still command more than two-thirds of prime-time viewing after more than a decade of multichannel cable.

In the UK, multichannel cable with its requirement for enormous capital investment has advanced at a snail's pace. Cable programme providers using distribution satellites to feed programmes to UK and European cable networks have all accrued heavy losses, none is yet operating profitably, 'churn' rates on UK cable have proved high. The BSB business plan estimates for future d.b.s. audience build-up have been strongly challenged by market consultants; the main use of video recorders appears still to be to provide time-shift viewing of broadcast programmes.

Expanding horizons

Engineers need to do more to inject an air of reality into the debates on the future of new technology. Back in 1982, at a time when Government ministers and others were enthusing over the revolutionary prospects for cable, I attempted in an industry journal to look a little more realistically at the expanding horizons of television as follows:

"We must be careful that in our enthusiasm for the expansion of television by new technology and with new programme sources to compete for viewers' screens, we do not lose sight of the basic fact that television programmes are for *viewing*. Laudable as the intention may be on the part of Governments to seize on new technology as a means of countering the decline of employment in traditional industries, and to build up new labour-intensive opportunities in the field of electronics, data-processing, electronic mail and information technology, this needs to be done with care, and not necessarily by wholesale destruction of existing systems, evolved over many years.

"It is virtually certain, and few would wish otherwise, that television broadcasting will evolve gradually to provide more choice for the individual viewer. But the long-term interests of viewers and of the *whole* industry should be taken into account. In attempting to assess the impact of new technology on television broadcasting the following are among the questions that need to be asked – and answered:

1. Does the development represent an entirely new direction or is it part of a continuing process?

2. Does the development offer the promise of a new service for the viewer or improvement to an existing service?

3. Does it permit new categories of programmes to be provided that are not possible on the existing services for technical, industrial, administrative or regulatory reasons?

4. If widely adopted will it eat into existing audiences or attract a new audience? For example, will it lead the viewer to avoid the more serious programmes with consequent repercussions on their financing?

5. Does it enable existing broadcast services to operate more effectively, or at lower cost, or to reach smaller segments of the population (more localized or those with more specialized interests)?

6. Is it likely to increase or decrease revenues of existing systems?

7. Will it directly compete with or complement existing services?

8. Would such a development be welcomed or opposed by the industry and the broadcasting unions?

9. How well or badly is it suited to the specific requirements and/or broadcasting structures of the U.K.?

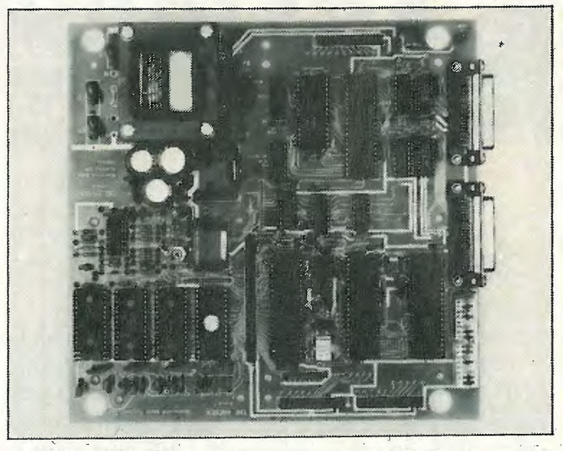
10. Realistically, what untapped potential exists for financing additional services by licence fee, subscription, advertising, sponsorship etc? Would new legislation be needed (always a slow process)? Does a potential audience already exist or would viewers need to buy or rent new receivers, aerials, converters, etc?"

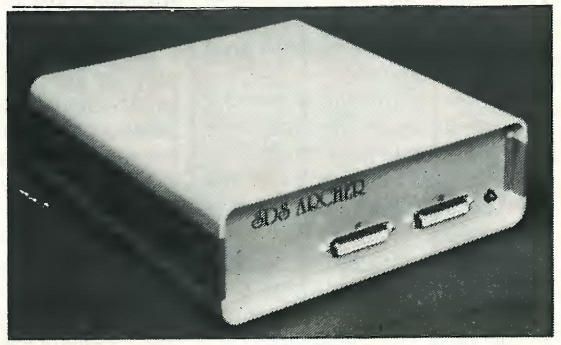
Data services

Teletext is an example of an entirely new service made economically possible by the 'new technology' of very large scale integration. After an extremely shaky start, it has gradually become an established and useful part of the television scene with the Oracle service now self-financing, even though penetration of homes is only about half that of the later video recorder. For those who take the trouble to learn to cope with the remote control units it is an efficient free service. The main drawback has always been that it is far from being a granny-proof system for an ageing population. Some control units have puzzling dual-function push-buttons with far from clear legends. Users need to learn not only the functions and use of the many push buttons but also to retain awareness of the topics covered in more than 500 pages on four channels. Some control units automatically reset to page 100 whenever a channel is changed temporarily. One needs preferably to memorize often-required page numbers in order to reduce the need to consult a sequence of index pages. In time, extra memory and extra lines will eliminate the once major drawback of access time. The fastext (fast access teletext) system with its four linked pages is a step in the right direction but a complete frame-store memory giving instant access to all pages is the ideal, though still not overcoming the need to know what you are looking for.

The enormous data capacity available on television channels, particularly d.b.s. channels, is encouraging another look into the possibilities of closed-user data services in which, unlike the existing subscriber user group services, complete confidentiality of broadcast data transmissions could be ensured. The IBA has recently commissioned market research into closed-user services by IFC Research to assess the potential demand for such services which would require amending the existing legislation covering IBA services.

Television Broadcast was written by Pat Hawker.





RADIO COMMUNICATIONS

Spectrum surveillance

The continued revival of interest in the use of the h.f. spectrum for medium-distance communications by the Defence Service, paramilitary organizations, diplomatic and civil communications and the growing complexity of electronic counter and counter-counter measures on both h.f. and v.h.f. are encouraging the development of new generations of communications receivers and allied systems. Racal, for example, has recently announced its new RA3700 series of modular communications receivers, in which the modular concept will be applied throughout the spectrum range v.l.f. to u.h.f. but with the first models (RA3701-4) covering 15kHz to 30MHz in 1 or 10Hz steps. The same frame is arranged to accommodate single or dual receivers with either front panel control or remote control. Built-in test equipment locates faults to module level and repairs can be carried out down to component level with the modules *in situ* or alternatively modules can be changed by the operators without the need for re-alignment or adjustment, claimed to result in exceptionally low mean time-to-repair figures. The need in some circumstances for improved pre-mixer selectivity is recognized by optional availability of a sub-octave r.f. filter module.

Rohde & Schwarz have been developing an automatic link system processor (ALIS) roughly along the lines of the Plessey system described last month. This can provide adaptive reaction to interference by automatic frequency changes and can elicit messages from unattended h.f. terminals. The system has been successfully tested on a German diplomatic rtty circuit between Bonn and Athens in conjunction with 150-watt transceivers although many of the tests were successfully carried out at power levels of 10 watts.

R&S have also responded to the increasing use of rapid frequency hopping on military systems that make up to 1000 frequency changes per second in a pseudo-random sequence. They have developed an intercept d.f. system capable of identifying the presence of a fast frequency hopper and providing an unambiguous bearing on it. This is the PA2000 system designed for the interception of short-duration signals from h.f. to u.h.f.

Basically the system utilises a Watson-Watt type of quasi-monopulse d.f. system in conjunction with an Adcock antenna array. The operator selects the frequency range to be scanned (for example the military tactical band of 30 to 88MHz). The receiver is then synchronously scanned at a rate of 1600 frequency changes per second across this range. If one or more frequency hoppers are operating, the receiver is certain to hit the transmission from time to time. Every short duration signal received is displayed as a dot on a bearing-versus-frequency display. After a few seconds lines of dots on the same bearing will appear, indicating that transmissions on different frequencies are coming in on the same bearing representing single frequency hoppers or a network of such stations. Presumably by detailed analysis of hit times it would be possible to crack the pseudo-random sequence of frequency hops permitting interception of the traffic.

For such applications as surveillance and monitoring of the v.h.f. and u.h.f. bands, Eddystone Radio has introduced a 1995 series of communication receivers which features the use of surface-mounted components, modular construction, built-in test equipment and offering various remote control techniques. It complements an existing h.f. range.

Attracting teenagers

Although in most countries the number of amateur radio licences in force is still at an all-time high, the past few years have seen a marked falling off in the number of newcomers, particularly teenagers who appear to find computer hobbies more attractive. The young who do qualify often drop out quite quickly.

The national amateur-radio societies, including the RSGB in the UK, ARRL in the USA and WIA in Australia, are actively seeking ways of making the hobby more attractive to the younger generation. But in so doing they face the risk of upsetting their older members who often resent any attempt to make it easier to obtain licences, and the increasing emphasis on communication as an end in itself (contests, awards etc.) rather than on self-training, technical investigation and experimentation. Modern solid-state technology and increasing systems complexity do not encourage home construction and it sometimes appears that only a minority of amateurs are now interested, other than superficially, in the technical and scientific aspects of radio communication or in acquiring operating crafts.

There is a real danger of national societies being forced by economics to place emphasis on quantity rather than quality if only to meet their spiralling administrative and publishing costs. It is now several years since the RSGB has been able to report a revenue surplus. During September, the society opened discussions with the DTI in respect of the promised radical revision of the terms of the UK amateur licence. The draft proposals put forward by the society include many useful and long-overdue changes. Nevertheless they fail in some respects to meet the constant requirement for the Amateur Service to justify clearly its requirements, in face of the pressures on the r.f. spectrum, the need to minimize electronic pollution and to improve compatibility in a domestic environment. The hobby needs always to justify its use of a not insignificant part of the radio spectrum.

The RSGB is asking that all amateur licences should permit the r.f. power delivered to the radiating element of the antenna to be raised from the current maximum of 26dBW (400 watts p.e.p.) or 20dBW (100 watts) for c.w. modes to a common figure of 30dBW p.e.p. (i.e. 1000 watts peak envelope power). After taking into account the losses in transmission lines and antenna matching networks, a newly-licensed amateur would immediately be authorized to use transmitters rated appreciably over 1kW output possibly with high-gain directive antennas giving effective radiated powers, along the beam, of tens of kilowatts.

The UK remains one of the few countries that eschews any form of "incentive licensing" other than the morse requirement for changing from a Class B (h.f. only) licence to Class A, and it could be argued that a number of amateurs are already running powers in excess of 30dBW. The RSGB takes the view that new recruits to the hobby need to be offered "a lot more than just the basic ability to communicate. Communication from virtually anywhere isn't a novelty anymore." But does this justify the use of 1kW-plus transmitters on the questionable basis of a pass mark of the current Radio Amateurs' Examination?

Apart from such experimental applications as moonbounce it is difficult to show any need for such high powers even when used by experienced and technically qualified amateurs. In practice few newcomers, particularly teenagers, could afford such high-power installations and would feel disadvantaged. To press for 30dBW p.e.p. would thus seem to be counter-productive.

Past experience suggests that making it easier to obtain high-power licences or to make the morse-free Class B licence more attractive does little to create long-term enthusiasts with a genuine interest in the technical aspects of radio communication and/or an interest in radio physics. In their efforts to increase revenues, the societies must be careful not to turn a self-educating scientific hobby into a purely fun pastime. It is worth remembering that interest in amateur radio has always tended to follow the sunspot cycle and may revive now that this is beginning to climb towards the maximum of Cycle 22.

Radio Communications was compiled by PAT HAWKER.

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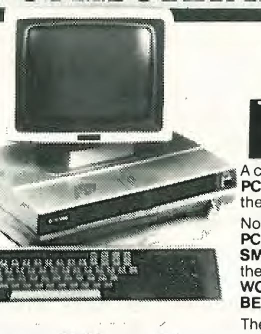

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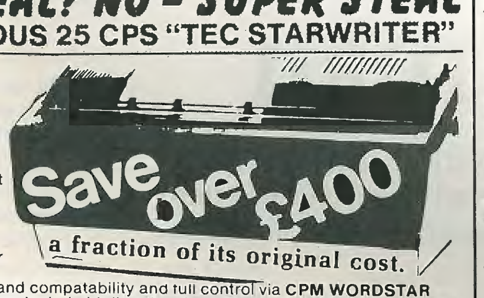

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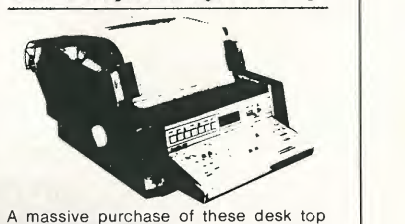

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Oliver Heaviside – the man

Dr G.F.C. Searle's recently published biography of Heaviside gives, says Mervyn Hobden, a rewarding yet all too brief insight into the man who established circuit theory as a rigorous discipline.

M.K. HOBDEN

It is one of the tragedies of the history of science that few biographers have bothered with the human character of their subject. Too many scientific biographies engage in violent hagiolatry, as the biographer relentlessly delineates a Great Life Well Spent, basking the while in the reflected glory of a Magnificent Human Spirit in the vain hope that a little of that aura will remain about him once he has laid down the pen.

Now Oliver Heaviside would have hated this. He would have expressed his contempt for such shallow appreciation in terms far rounder and more explicit, as G.F.C. Searle, the author of this present biography, makes clear. In a letter written in 1950, he states

> "Anyone who writes about him as he was will have no material but what is queer. 'Impish' is the term to describe him... There seems to be some sort of aversion to having O.H. described as he actually was. It seems to be thought that all that is wanted is for people to be told what is in his books... If they don't understand the Operational Calculus, they might find some entertainment in learning why O.H. went about for a month in the headress of the Tuaregs of the Sahara."

Searle, and later his wife, were close friends, perhaps the closest friends that O.H. had from 1892 until his death in 1925. What unfolds in his narrative is a tale at times outlandish, at others hilariously funny, yet always penned with a deep affection for one of the most astonishing characters in the history of British science. It would be too easy to record the eccentricities of O.H.'s behaviour as the vagaries to which genius is prone. Searle never stoops so low and allows us real insight into a man who was a delightful companion (most of the time!) and an amusing and voluminous correspondent. It is the correspondence that comprises the bulk of the book.

Searle first visited Heaviside at Paignton in Devon in September, 1892. At that time, O.H. was living with his parents. Charles Heaviside, his father, owned a music business, which was managed by Oliver's brothers, Frank and Charles junior. Searle was to return in the September of the two following years, establishing the pattern of correspondence and visits that was to continue for the next thirty years.

Both of Oliver's parents died, his mother in 1894 and his father in 1896. He later said in a letter to Searle, after his own serious illness in 1913, "I have nursed my parents night and day, half asleep all the time". After their death, he remained for a few months in Paignton, then moved to his own house, Bradley View in Newton Abbot. Searle was again a frequent visitor, which allowed them both to exercise a passion for cycling, leaving us with this splendid vision of Heaviside, arms folded and feet on the front forks, disappearing from view down steep Devon hills.

Another visitor during this period was G.F. Fitzgerald, the physicist, with whom O.H. established an instant rapport. On hearing of Fitzgerald's illness in January 1901, he wrote to Oliver Lodge,

> "I am grieved to hear of the illness of our friend of brilliant ideas. I will take care not to worry him"

On being informed of Fitzgerald's death in February, he wrote again to Lodge:

> "...a post card from [Professor] Perry, 'Fitzgerald is dead' came as a great shock. I understand and sympathise with your grief, for knowing him so much better than myself. I only saw him twice but we had a lot of correspondence at one time and I got to love the man. There was a considerable mutual understanding...
>
> The premature death of a man of brilliant genius and wide sympathies is a national misfortune, though of course the nation won't know anything about it."

O.H. wrote to Mrs Fitzgerald, expressing his sympathies and reported to Searle,

> "Got receipt from Mrs F. instantly. Regular woman's letter. Pride; and joy; not forgotten; loss hard to bear; etc. Well, very glad to have given her the pride and joy but I won't recommend her to study the work to find consolation. She might go out of her mind in the process."

DOMESTIC PROBLEMS

Lest this gives too harsh a character to O.H.'s humour it is necessary to look at some of the other examples which Searle freely quotes. O.H.'s housekeeper at Newton Abbot suffered a stroke in 1899 and left him to manage his domestic affairs alone.

> "Poor women sent away. No good for hard work again, I fear...Quite independent and have whatever I like for dinner. Stone broth, ditchwater soup...You mustn't pour anything hot into a glass dish. Catastrophe. Bang goes sixpence! If a pound of beef is used to make soup and is kept boiling day after day how long will it take to disappear? Haven't found out yet. Big lump left."

His domestic problems multiplied:

> "I have adopted the Principle of Least Action. It is a most clumsy machine in electromagnetics; but splendid in the house; assisted by the older principle that Prevention is better than Cure. E.g., nasty job blacking boots. Don't black 'em; use tan boots. Fires is a most horrid nuisance, with the dirt and work. Abolish them, use gas fires, no more trouble and labour. I have four, a gas cooker in the kitchen and gas fires in the sitting room and bedroom.
>
> It is such a blessing that I am always thinking how to get gas or something to do the rest of the housework."

This love affair with gas did not last. Some years later, an abortive attempt to tamper with the gas meter in his house in Torquay led to burns to the hands and face. For the next month he greeted visitors with a large bed blanket over his head, secured around his neck with a rope. It was this curious costume which led Searle to liken his appearance to that of a desert Tuareg. He them proceeded to address the following letter to the gas company.

> "From Oliver Heaviside – W.O.R.M.
> 'Wormfield', Torquay.
> To the Manager, Torquay Gas Company.
> Please send one new gas meter of strong constitution to replace the present one which is corroded inside and out by the rotten gas which you are supplying me."

This humorous missive, (which, incidentally, was successful) must be contrasted with his sharply-drawn remarks on his peers and mathematical science, to the British Association for the Advancement of Science in 1913.

> "I don't think pure mathematics a suitable subject for section A. I think there should be a separate section for Mathematics. And I don't like their superior tone. It is a well-known fact Physics has created Mathematics and you have to go back to Physics to make new work, not mechanical development of old work...
>
> I appreciate the beauty of Mathematical theorems occuring in Physics. I generally dislike the way they are 'proved', as they say. Most mathematical books are a hodge-podge of formulas, without distinct connection to make a theory, or to exhibit it plainly and made as repulsive and unintelligible as a legal document by attempts to be too precise and perfect."

THE TORQUAY MARRIAGE

By 1908, O.H.'s finances and health, neither of them very secure at any time during his friendship with the Searles, had deteriorated to the point where his brother Charles suggested a new arrangement. His wife's sister Mary was living alone in a house in Torquay. She was in somewhat straitened circumstances, having lost money in what Oliver termed 'speculations'. It was considered by the Heaviside family to be sensible for O.H. to abandon his solitary existence and move in with Miss Way as a paying guest. This was the beginning of what O.H. was to term 'the Torquay Marriage'. He reports in a letter to Oliver Lodge,

> "At last, however, I have no house; I am only a lodger; I have lost my independence like Mr Pecksniff's pupils. If I want anything more, I am at liberty to mention it! And such an odd landlady, who has to be 'mentioned' to over and over again and finally gets waxy before she does it. Yet she is a very good woman for all that; much too kind hearted and free in her kindness. When she has money, lends it out to flatterers who don't pay it back."

In view of O.H.'s later opinion of his landlady, whom he christened The Baby (she was by various estimates he made, between 66 and 69 years old when he moved in), this may seem a little surprising. It is difficult, however, via the medium of his wildly exaggerated accounts of domestic affairs at Homefield, to fathom his real opinion. Here is a brief taste of a saga that must have had the Searles oscillating helplessly between uncontrollable laughter and indignation at the treatment which Oliver seemed to wish them to believe was the daily diet of the hapless Miss Way. The affair concerned food, an ever-present subject of concern in the O.H. correspondence.

> "Tuesday 30th January, 1912. The Great Lentil Question cropped up today, (not the first time). Shall I when I want Pork and Pease pudding hot, this being the proper time for this wholesome and vulgar fare, to make the system able to resist the cold, shall I be diddled into eating lentils instead on the plea that they are much nicer and so nutritious?"

It appears that Miss Way had fallen under the (baleful, in O.H.'s opinion) influence of a vegetarian niece and he describes how he banished such uncalled-for delicacies as cabbage stalk soup.

> "She wasn't amenable to my very civil remonstrance that I knew lentils very well; I wanted pease. 'Oh! You know everything!' she replied, with some temper. 'I assure you they are very nutritious.' But they are not pease pudding."

The sobriquet of 'Torquay Marriage', which O.H. chose to describe the curious relationship between himself and Miss Way, is perhaps not far from the truth.

It was not a physical marriage of the flesh, but was consummated verbally by both parties and at great length. To the Searles as outside observers, and to the Heaviside family at Torwood Street, Oliver appeared tyrannical in his behaviour. On one visit, Searle cornered O.H. in his study and upbraided him for his ingratitude. He records, "One lesson in 'manners' satisfied him and it was a year or more before he asked me into his study again. He felt safer behind the skirts of Miss Way and Mrs Searle".

The coalition government at Homefield thundered on through many curious episodes for some seven or eight years. Finally, the Heaviside nieces arrived one day in a car to carry their beloved Aunt Polly off to the safety of Torwood Street, where she spent her remaining years.

HEAVISIDE IN DISTRESS

O.H. was once again alone and prey to the twin horrors of domestic affairs and shaky finances. The Searles did their best to support their friend with loans and gifts of money, often from admirers of Heaviside's work who were distressed at his parlous condition. Searle had the diplomatic task of accounting to Oliver for these miscellaneous sums which appeared on his bank statements. The donors often wished to remain anonymous and, O.H. would demand, not unnaturally, that Searle reveal their names. This is, perhaps, the most distressing aspect of the whole book: the picture of a man, whose contributions to the science of electromagnetics far outweighed those of his contemporaries, battling to suppress his embarrassment at the necessity of being dependent on charity to survive. It would be impossible not to sympathize with Searle and the difficult, tactful path he had always to tread.

In 1920 a number of American engineers and physicists proposed that a collection be made amongst those companies in America which had benefited most from O.H.'s work with a view to supplementing his income. The Americans were shocked to learn of his poverty and had great difficulty in understanding how a man of his obvious worth could become so neglected.

Searle had the delicate task of communicating their proposals to the recipient. Oliver was not pleased, and became very angry when Searle refused to reveal the names of the proposed benefactors. Searle realized later that this was a terrible mistake. O.H., although their correspondence continued, imposed a ban on any further visits to Homefield.

By 1921, owing to a bank error, his finances had sunk to an all-time low. A distraint warrant was issued on his property; and a police inspector together with the local constable, Brock, who was a good friend to Oliver, were sent round to serve it. Even here, an element of high farce entered as O.H. insisted on being allowed to help them label the property subject to the warrant. Fortunately, he was able to extend his overdraft at the bank and Searle once again was able to find new finance for his friend.

The Institute of Electrical Engineers, on hearing of his condition of near-bankruptcy, promised to arrange a supplement to his annual income. The President, J.H. Highfield, sent a cheque for £100, together with a letter which is a model of tact and understanding.

The Searles did not see their old friend again until January, 1924; he was obviously unwell. On returning the next day, they received no reply to their knocking at his door.

He had been discovered that morning by his faithful friend Brock, the policeman, unconscious on the floor. As it was impossible to nurse him at Homefield, he was removed to a local nursing home and the Searles visited him every day for tea, until the end of their holiday on January 19th.

Even in this last illness, Heaviside's sense of fun made him a favourite with the nurses. However, his initial recovery, made in the conditions of comfort and good food which the nursing home provided, was not sustained. The Searles' beloved friend of 33 years died on February 3, 1925.

REVOLUTIONARY CONCEPTS

The picture of Oliver Heaviside which emerges from Searle's account is a complex one. Yet it is difficult to put the book down without a sincere feeling of regret that you will never meet the character whose friendship meant so much to the Searles. Their privilege of coming down in the morning to find on the hall carpet a bulky envelope containing yet more terrifying revelations of domestic affairs at Homefield is one we shall never enjoy. Neither will we be asked to join that exclusive institution that allowed its members to use the letters W.O.R.M. after their names. No mere review can do justice to the act of human honesty and affection with which Searle engages our attention.

There can be no doubt that Heaviside felt that the true value of his work was not appreciated, and that the revolutionary concepts which formed the backbone of his understanding of electromagnetism would be doomed to oblivion by those who preferred neat algebra to physical rigour. To a younger generation of electronic engineers, the contribution O.H. made has been obscured by the substitution of the name Laplace on the approach to circuit theory which he pioneered.

I suspect, however, that the Marquis de Laplace would be the first to recognise O.H's priority, in the application of what was originally a simple trick to avoid secular terms in the calculation of planetary orbits, to the far greater remit of the vector calculus of electromagnetic circuits. It is difficult to avoid the conclusion that this singular man, who gave us the concepts of reactance and impedance, was

> "...far loftier than the world suspects, living and dying."

Mervyn Hobden is chief development engineer at Marconi Electronic Devices Ltd, Lincoln. He is researching a semi-historical perspective on electromagnetic theory.

Oliver Heaviside, the Man, by the late Dr G.F.C. Searle, is published by C.A.M. Publishing in hard covers, 80 pages. The book is available at £12 post free from the publishers at P.O Box 99, St Albans AL3 4HQ.

An article outlining Heaviside's scientific achievements appeared in W.A. Atherton's Pioneers series, in *Electronics & Wireless World*, August 1987.

Prize for radar pioneer

The 1987 Royal Society Appleton Prize for Ionospheric Physics has been awarded to Professor S. Kato, director of the Radio Atmospheric Science Centre at Kyoto University, Japan, in recognition of his distinguished contributions to the study of the dynamics of the ionosphere and the middle atmosphere, and for his development of an advanced radar system to observe the atmosphere.

One of Professor Kato's major achievement was the development of a large-scale MST Radar Observatory, in Kyoto, capable of measuring the three-dimensional structure of the middle atmosphere and ionosphere over the range of 2 to 300 km. This equipment proved invaluable in his studies of the dynamics of the ionosphere and the energy/momentum flow from the former to the latter by way of atmospheric tides and internal gravity waves from major atmospheric disturbances such as typhoons.

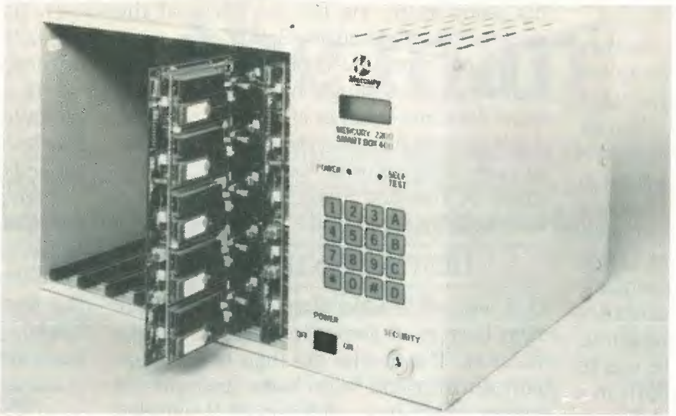
During the last six years, Professor Kato has made significant contributions to theoretical and observational studies on lunar tides, non-migrating tides, tropical stratospheric and mesospheric tides and ionospheric tidal theory. He had developed appropriate hardware and software for measuring both the middle and ionospheric heights by the MST Radar in Kyoto.

More recently, he had initiated systematic observations of the ionospheric wind system by the meteor techniques in a wide range of altitudes from 2 km upwards and had developed an electronically controlled phase array radar for measurement of atmospheric wind and waves and of the ionospheric wind system.

Band III radio

The Band III radio service has undergone successful tests in London. The service, licenced to National Mobile Radio Ltd will operate in the larger conurbations in the UK to begin with, but rapid expansion is planned for full nationwide coverage to get ahead of other Bank III competitors. NMR, a consortium of BT, Motorola and National Radiofone, is using the Storno Starnet trunked radio system which has been in use for over a year for British Rail, using signalling protocols almost identical to the Band III system.

Meanwhile, the other National system, Band Three Radio Ltd, has issued an interim specification for equipment to run on its network. Many manufacturers have said that they can provide sets that will comply. The network has eight sites transmitting in London and the South East with more planned very soon. They forecast 60% coverage of the UK population by March 1988.



Mercury have developed the Smart Box, a system which analyses the first few digits of a telephone number being dialled and if it is a Mercury distribution area will automatically connect to the Mercury network, otherwise to BT. Two versions cater for the user with up to five lines or the Smart Box 400 for any number of lines. Mercury are also commencing a paging service and have appointed Vanderhoff to be the distributor of equipment and to undertake the billing of air time to the customers.

Machine learning in Massachusetts

Siemens and the Massachusetts Institute of Technology are to co-operate in long-term research into machine learning. Approximately one third of $16m budget earmarked by Siemens will be spent at MIT during the next five years. The focus of the research will be methods and systems that can progressively acquire new knowledge through interaction with their environment, rather than through pre-programming. Potential applications span nearly all computer uses and include the recognition and processing of images, sounds, text and speech. Research may also yield insights and ideas towards a new generation of computer architecture with learning capabilities.

The project is intended to pursue research into machine learning on a broad interdisciplinary basis that includes computer-related, biological and cognitive research at MIT's Laboratory for Computer Science.

European satellite tv circuits

Three European companies will cooperate to meet the requirements of European MAC receiver systems; Plessey Semiconductors will manufacture the Nordic v.l.s.i. designd MAC decoder chips which will be completed by bipolar circuits and systems controllers manufactured by Philips.

It will be the first multistandard conditional-access chip set able to decode C, D and D2-MAC and provides data transmission capability. This will mean that it can accept the Astra, BSB, TDF, TV-SAT and Tele-X transmissions and any future signals using the MAC packet family.

In brief

Work on laying the first optical transatlantic telecommunications cable started with the floating ashore of the UK end at Widemouth bay in Cornwall. The main section is to be lain in spring by a British Telecom International cable ship which will use a special plough to cut a channel in the ocean bed and bury the cable and protect it against trawl nets and anchors. The UK section of the cable is to be connected with a similar link to France by special junction which will join both branches to the main cable. TAT 8, with a capacity for 40,000 telephone calls or their equivalent in text graphics or tv signals, is due to start operation next summer.

'Parallel subsystem bus of the IEC 821 bus' is the title of the specification for the VMEbus subsystem. This publication of the IEC working group 1 of subcommittee 47B includes a detailed description of P2 connector on the VMEbus for users and designers. Available through the Vita User Group UK, 37 Hamlet Court, Westcliffe-on-Sea, Essex SS0 7EY. Tel: 0702 330830.

Sir Clive Sinclair returns to the high street with the Cambridge Computers' Z88 lap-top computer. With a built-in word-processor, spreadsheet, calendar and diary, a real-time clock and plug-in mass memory, the computer has been described as an 'electronic Filofax'. An optional link and software allows communications between the Z88 and other PCs. The computer is lightweight, uses a supertwist l.c. display and the internal batteries can keep it going for a few hours continuous use or a year on standby. On sale in Dixons and Comet.

IBM and Cambridge University have together announced a joint project to investigate setting up a network for campus-wide distributed computing. The scheme is aimed at integrating the wide range of computers and communications devices that are appearing in classrooms, laboratories, offices and student rooms, and so increase the power and function available to every user on the university campus.

Under the terms of the study contract, the IBM UK contribution will include staff, hardware and software for the project, which is initially expected to last between two and four years. The University will host the project and provide staff and facilities.

Pan-European digital cellular radio

Two British celllular service providers, Racal Vodaphone and Telecom Securicor, have agreed to conform to, and to institute the UK part of, the European cellular radio service.

Racal says its analogue cellular network will increase from the current 100,000 subscribers to six times that by 1992. The company aims to become "a world leader in operating a digital cellular network and a major manufacturer of digital cellular infrastructure and subscriber equipment."

Low-power radio type approval

The Department of Trade and Industry has prepared performance specifications for the type approval of low-power radio devices. The specification is necessary to maintain a standard for devices that will be free from licensing. The equipment covered includes induction systems, telemetry and telecommand devices, wireless microphones and hearing aids, Doppler and field disturbance alarm sensors, and emergency alarms for the elderly and infirm. Such equipment is subject to updated versions of the existing specifications but new regulations have been introduced for some types of radio alarms, for general-purpose low power devices using the 49MHz band and the microwave bands. These are newly assigned frequencies and provide further outlets for manufacturers. Further details from the DTI Radiocommunications Division library, Waterloo Bridge House, Waterloo Road, London SE1 8UA. Tel: 01-215 2000.

Land-mobile satellite communications

Successful trials have been carried out by Inmarsat and the Centre Nationale d'Etudes des Telecommunications involving the reception of messages transmitted to a moving vehicle by satellite. The receiver equipment installed in a small van travelling through France and Spain is housed in a small box with a conical antenna 190mm in diameter. This conforms to the equipment available to maritime users for use with Inmarsat Standard-C to be introduced next year. This is a data-only system for the transmission of text at 600bit/s. Mobile users are connected via satellite to the standard Telex or other data networks.

Measurements were taken in various locations to assess the quality of reception. On motorways and open roads, for example, 96% of messages were received the first time. As messages are repeated until received, the reception of a specific message is virtually guaranteed. Such obstcles as bridges, overhead electrical lines and trees caused practically no degradation of reception.

The first automatic aeronautical ground station is to be installed at Goonhilly to connect the BT telephone network directly to aircraft over Europe and the Atlantic via satellites operated by Inmarsat. Passengers will be able to dial direct air-to-ground calls. Pilots can also have continuous contact with air-traffic controllers and operational centres.

Copper on ceramic

A technique of depositing copper tracks onto an aluminium oxide substrate has been developed by British Aerospace. The method enables i.cs in leadless chip carriers to be mounted directly on to multilayer p.c.bs by reflow soldering. Each board (up to 150 by 165mm) can have up to six conducting layers with copper track as fine as 0.18mm wide. A high density of interconnections between the layers is possible.

The AlO_2 substrate can be made in any shape and is a good thermal conductor. Addition heat dissipation can be provided by mounting a ceramic board on either side of an aluminium plate, with the advantage of providing structural support. Alternatively, edge connectors for backplane connection could give the required support.

A commercial service covering the design and manufacture of multilayer copper on ceramic modules has been instituted at BAe's Microelectronics Technology Centre at Hatfield.

Many Londoners will appreciate this silent digital radio system for motorcycle messengers. A warning light on the handlebars tells the rider that there is an incoming message. To get the details, the rider must dismount, open the top-box and read the message on a scrolling display. Routine acknowledgement messages are transmitted silently, using a numeric keypad on the telephone handset. Data Link has been developed jointly by Storno and Relcom Communications of London.

EXHIBITIONS & CONFERENCES

October 26 to November 6
IBM 87. Exhibition organized by IBM to show their latest range of PC and mid-range computers together with authorized dealers and agents, and software vendors. London Business Design Centre, Islington Green, London.

October 27 to 30
BIAS 87; 27th International automation, instrumentation and microelectronics conference and exhibition. Milan. Organisers: EIDM, Viale Premuda 2, 20129 Milano, Italy.

October 30 to 31
Women's Engineering Society annual conference, promoting the Women In Science and Engineering (WISE) campaign. University of Manchester Institute of Science and Technology. Details from the WES, Imperial College, London SW7 2BU.

November 3 to 5
Comex 87; conference and exhibition on mobile communications, services and products. Sandown Park International Exhibition Centre, Esher, Surrey. Organizers: Frametrack. Tel: 01-653 2657.

November 9 to 10
Digital electronic design. Seminar by C.A.M. Consultants. Details from Ivor Catt, Tel: 0727 64257. To be held in St Albans and again in Manchester on November 12-13.

November 10
CRT Displays; symposium by the Society for Information Display at the M-O Valve Company, Brook Green, Hammersmith, London WC6.

November 10 to 12
Drives, motors, controls and PC interface exhibitions. NEC, Birmingham.

November 11
PC 87; Programmable Controller conference and exhibition. NEC, Birmingham.

November 16 to 20
Composants Electroniques 87, Salon international of electronics components. Paris-Nord parc d'expositions.

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Reporting to the ITV Association's Head of Engineering Services, the successful candidate will assist in the preparation of technical publications. These include equipment specifications, detailed reports on engineering developments (in conjunction with design engineers), articles for the technical press and booklets on broadcasting matters for staff in the ITV companies. Other major duties are the preparation of minutes of technical meetings and researching for industry briefings with minimum supervision.

The ITV Association wishes to hear from candidates who:

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- have an understanding of digital communication and control techniques applied to broadcasting;
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Printed in Great Britain by E.T. Heron (Print) Ltd, Crittall Factory, Braintree Road, Witham, Essex CM8 3QO, and typeset by Graphac Typesetting, 181/191 Garth Road, Morden, Surrey SM4 4LL, for the proprietors, Reed Business Publishing Ltd, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS. © Reed Business Publishing Ltd 1987. *Electronics and Wireless World* can be obtained from the following: AUSTRALIA and NEW ZEALAND; Gordon & Gotch Ltd. INDIA: A. H. Wheeler & Co. CANADA: The Wm, Dawson Subscription Service Ltd., Gordon & Gotch Ltd. SOUTH AFRICA: Central News Agency Ltd; William Dawson & Sons (S.A.) Ltd. UNITED STATES: Eastern News Distribution Inc., 14th Floor, 111 Eighth Avenue, New York, N.Y. 10011.

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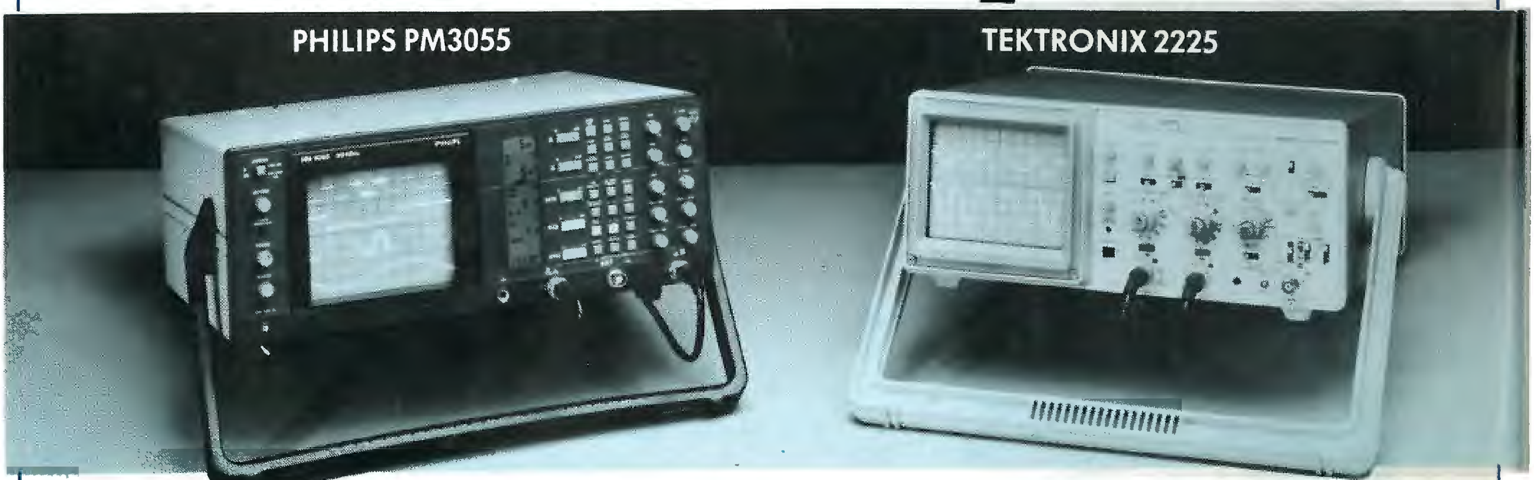

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