VOLUME 114, ISSUE 1872

DECEMBER 2008 £4.60
www.electronicsworld.co.uk

ELECTRONICS WORLD

THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

Design for Power:

- ACTIVE FILTERS FOR SUPERIOR FILTERING
- KIT-BASED APPROACH TO POWER
- PMICS FOR PORTABLE POWER

MCU-BASED PLC: THE SERIES CONTINUES INSIDE

TECHNOLOGY
INTEL'S 2009 MICROPROCESSORS ROADMAP

ELECTRONICA 08
THE COUNTDOWN TO THE EVENT HAS STARTED

PRODUCTS
THE LATEST CROP OF COMPONENTS AND SYSTEMS

ALSO IN THIS ISSUE: THE TROUBLE WITH RF @ TIPS 'N' TRICKS @ ROHS

The New Oscilloscope Experience Is Here

Quick Insight. Deep Insight.

Experience the New LeCroy Oscilloscopes.

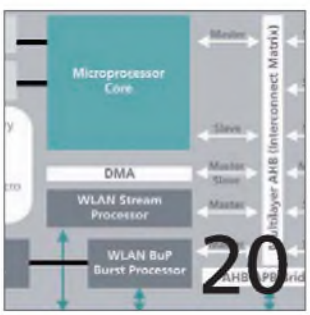
www.insightwithconfidence.com

LeCroy

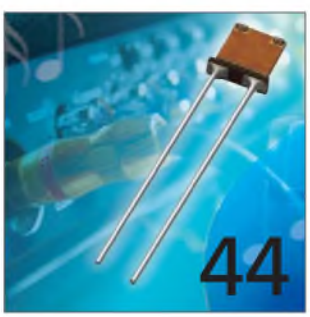
Phone 01235-533114 | www.lecroy.com/europe

Page 13 - the place to find more about Yokogawa's DLM200 oscilloscope family

FEATURES



REGULARS



QUASAR electronics

Quasar Electronics Limited
PO Box 6935, Bishops Stortford
CM23 4WP, United Kingdom
Tel: 08717 177168
Fax: 07092 203496
E-mail: sales@quasarelectronics.com
Web: www.QuasarElectronics.com

All prices INCLUDE 17.5% VAT.
Postage & Packing Options (Up to 2Kg gross weight): UK Standard 3-7 Day Delivery - £3.95; UK Mainland Next Day Delivery - £8.95; Europe (EU) - £6.95; Rest of World - £8.95 (up to 0.5Kg).
!Order online for reduced price UK Postage!
Payment: We accept all major credit/debit cards. Make cheques/PO's payable to Quasar Electronics.
Call now for our FREE CATALOGUE with details of over 300 kits, projects, modules and publications. Discounts for bulk quantities.

08717 Credit Card Sales 177 168

Ho! Ho! Ho! Christmas 2008 is on it's way

BUT DON'T PANIC!!

We have some fantastic gift ideas for young (and old) enquiring minds

Electronic Project Labs

An electronics course in a box! All assume no previous knowledge and require NO solder. See website for full details

30 in ONE - £16.95
Order Code EPL030KT

130 in ONE - £39.95
Order Code EPL130KT

300 in ONE - £59.95
Order Code EPL300KT

500 in ONE - £149.95
Order Code EPL500KT

Robot Sensor - £19.95
Order Code EPLR20KT

Digital Recording Laboratory - £29.95
Order Code EPLDRKT

Solderless Electronic Project Kits

AM-FM Radio Kit - £6.95
Order Code ERKAFKT

Short Wave Kit - £6.95
Order Code ERKSWKT

Crystal Radio Kit - £6.95
Order Code ERKCKT

Electronic Bell - £8.95
Order Code EAKEBKT

Electronic Motor - £8.95
Order Code EAKEMKT

Generator - £8.95
Order Code EAKEGKT

Room Alarm - £4.95
Order Code EAKRAKT

Hand Held Metal Detector - £7.95
Order Code ELMDX7

Metal Detector - £7.95
Order Code ELMDKT

Robot & Construction Kits

Future engineers can learn about the operation of electronics, robotics and transmissions systems.

Moon Walker - £33.95
Order Code 4015KT

Robot Arm - £54.95
Order Code 4017KT

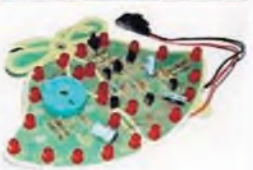
Robomech - £12.95
Order Code C21-603KT

go online for Special Offers

Trainmech—£12.95
Order Code C21-606KT

Tyrannomech - £12.95
Order Code C21-601KT

Festive Electronic Project Kits



Musical LED Jingle Bells - £17.95
Order Code 1176KT

Flashing LED Christmas Tree - £5.95
Order Code VMK100KT

See our website for even more great gift ideas!

No.1 for KITS

www.QuasarElectronics.com

Secure Online Ordering Facilities • Full Product Listing, Descriptions & Photos • Kit Documentation & Software Downloads

ELECTRONICS WORLD

EDITOR:
Svetlana Josifovska
Email: svetlana.josifovska@stjohnpatrick.com

PRODUCTION EDITOR/DESIGNER:
Tim Wesson

DISPLAY SALES EXECUTIVE:
Matthew Dawe
TEL: +44 (0) 20 7933 8999
Email: matthew.dawe@stjohnpatrick.com

SALES DIRECTOR:
Chris Cooke

PUBLISHER:
John Owen

SUBSCRIPTIONS:
Dovetail Services
800 Guillat Avenue,
Kent Science Park,
Sittingbourne,
Kent, ME9 8GU
TEL: +44 (0) 844 844 0230
Email: saintjohnpatrick@servicehelpline.co.uk

SUBSCRIPTION RATES:
1 year: £46 (UK); €120 (Europe);
$145 (US & worldwide)

MISSING ISSUES:
Email: GoldeneyeTeam@servicehelpline.co.uk

NEWSTRADE:
Distributed by Seymour Distribution Ltd,
2 East Poultry Avenue, London, EC1A 9PT
+44 (0) 20 7429 4000

PRINTER:
William Gibbons Ltd

St John Patrick Publishers

THE ELECTRONICA SHOWCASE

Two years have gone by and Electronica – the biggest two-yearly electronics components and systems event in the world – is on again at the New Trade Fair in Munich, Germany, between 11th and 14th November.

But something feels amiss. Unlike any of the previous years, the buzz preceding the event has been somehow lacking. Previously, participant companies would start announcing new products and events or trying to organise meetings even in August. This year, things have been rather quiet. I hope it's not a reflection on how the event is going to pan out.

It'll be interesting to see what Electronica brings this year, however. As usual, I am expecting the buzz, the adrenalin, the hype, once the show opens its doors to visitors. But, it will also be a good indication of how European, American and even Asian electronics firms are doing. So far, we've seen that businesses have been cautious.

Expectations are that Electronica 2008 will be attended by some 3,000 exhibitors and 78,000 visitors. There are 14 exhibition halls in total, and this trade fair for components, systems and applications promises to present the complete spectrum of electronics, ranging from semiconductors, embedded systems, displays, sensor technology, test and measurement equipment, and electromechanics/system peripherals (previously classified at Electronica under interconnection systems/components, switches, relays, keyboards and casing technology) through to electronic design.

According to the event organisers, this year's exhibition will focus on the growth markets of automotive and wireless. In addition to these two, other focus areas for Electronica 2008 will be on embedded systems und micro-nano systems, all of which will be presented as separate exhibition sections and a series of talks. Automotive and wireless will have their own two-day conferences.

This year, like two years ago, *Electronics World* magazine will have its own stand. We'll be in Hall A5 – more precisely A5.175/3. As last time, if you are at the Electronica 2008 event, we'd like to invite you to come by the stand, join us for a drink and share your views and announcements with us.

Svetlana Josifovska
Editor

Check out Electronics World's new website by clicking on **www.electronicsworld.co.uk**

"THIS YEAR, LIKE TWO YEARS AGO, ELECTRONICS WORLD MAGAZINE WILL HAVE ITS OWN STAND. WE'LL BE IN HALL A5 – MORE PRECISELY A5.175/3"

Electronics World is published monthly by **Saint John Patrick Publishers Ltd**, 6 Laurence Pountney Hill, London, EC4R 0BL.

Intel's 2009 Roadmap

At the recent San Francisco Intel Developer Forum, Pat Gelsinger, senior VP and general manager Digital Enterprise Group and Jim Brayton, Intel Nehalem prcject manager, are showing off the next-generation 45nm microarchitecture (codenamed Nehalem) wafer

Intel continues to march toward pervasive, higher performance and power-efficient computing, said Pat Gelsinger senior VP and general manager at the Intel Digital Enterprise Group, during his keynote speech at the recent San Francisco Developer Forum.

He detailed Intel's 2009 roadmap, disclosing a raft of new features of the next-generation processor family, including a new turbo mode that shifts the processor into a higher gear for greater performance and yet without the heat penalty.

The company's first desktop PC chips branded Core i7 processors and initial energy-efficient, high-performance server products (codenamed Nehalem-EP) will be first to production. Intel is also planning to manufacture a second server derivative designed for the expandable sever market (Nehalem-EX), and desktop (Havendale and Lynnfield) and mobile (Auburndale and Clarksfield) client versions in the second half of 2009.

"Our engineers have put together an incredible processing family that will include a tremendous amount of new processor features, all centered on delivering faster computer performance and terrific energy efficiency," said Gelsinger.

The next-generation Core microarchitecture also features Intel Hyper-Threading Technology delivering up to 8-threaded performance capability on four cores in the initial versions and best-in-class memory bandwidth, thanks to the new QuickPath Interconnect. QuickPath connects processors, chipsets and memory together, and delivers up to three times the memory bandwidth of previous generation Core microarchitecture solutions.

Gelsinger also discussed the industry's first many-core Intel Architecture (IA) based design, codenamed Larrabee. Expected in 2009 or 2010, the first product based on Larrabee will target the personal computer graphics market, support DirectX and OpenGL, and run today's games and programs. Larrabee is expected to kick-start an industry-wide effort to create and optimise software for the myriad of cores expected to power future computers.

In addition, Gelsinger said that another growth opportunity for Intel and the high-tech industry is the Internet (which Intel calls the Embedded Internet), where some 15 billion devices are expected to be connected to it in the near future. Among them will be the devices for the emerging markets in the embedded computing space such as IP networking and security, video intelligence, medical, in-vehicle infotainment and home automation, which will greatly benefit from the always-on Internet connectivity.

IN BRIEF

Researchers from the Hitachi Central Research Laboratory in Japan and the Advanced Technology Institute of the University of Surrey, UK, report that nano-designed transistors for the large area display and sensor application field benefit hugely from quantum size effects. The unexpected superior switching performance (low leakage current and steep sub-threshold slope) shown experimentally and analysed theoretically, demonstrate hitherto unexplored routes for improvements for transistors based on disordered silicon films.
By making the conduction channel in these disordered transistors very thin, the team has shown this technology will enable the design of low-power memory for large area electronics, based on a low-cost industry standard material processing route.

Inside Contactless and Saetic are working together to incorporate Inside's MicroPass contactless technology into an upcoming family of contactless EMV products from Saetic that will be available in both plastic card and contactless sticker form-factors for the Spanish market.
The MicroPass platform is based on the RISC architecture and is designed to power open-standard contactless and dual-interface bank card payments along with other value-added applications.

The Media Oriented Systems Transport (MOST) Cooperation, which standardises the MOST automotive multimedia network has demonstrated how this technology can be used as an automotive Ethernet physical layer. The multimedia demonstration showed MOST at 150Mbps bandwidth with high-speed Ethernet packet transport, multi-channel video streaming from HDD, as well as isochronous streaming of HDTV and SDTV. In addition to higher bandwidth, MOST150 features an isochronous transport mechanism to support extensive video applications, as well as an Ethernet channel for efficient seamless transport of IP-based packet data. The Ethernet channel can transport unmodified Ethernet frames as specified by IEEE 802.3. This enables software stacks and applications from the consumer and IT realms (where the speed of innovation is much faster) to be seamlessly migrated into the car.

avionics

CONFERENCE AND EXHIBITION

4th–5th March 2009, Passenger Terminal Amsterdam (city centre), Amsterdam, Holland
www.avionicsinternational.com

MOVING ON TO NEW HEIGHTS

Avionics Expo is the only commercial and educational platform for discussing civil and military related avionics in Europe; bringing together the most influential and high-ranking members from the market and has become the 'must attend' event on the Avionics calendar.

Avionics Expo allows key decision makers, scientists, technologists, engineers and procurement specialists from within the leading avionics manufacturers, integrators, airframers and airlines to discover and discuss the latest issues and developments affecting avionics technology.

WHY EXHIBIT?

- Showcase your products and technologies and develop new customer bases
- Unique access to avionics purchasing & procurement professionals from across the region and the globe
- Discuss trade ventures and meet new partners in dynamic surroundings
- Promote products and services to the worlds leading press figures
- Unrivalled platform to create sales leads and make lasting relationships with clients
- Access to the industries most influential decision makers over 2 days

Please direct exhibition sales enquiries to:

Gareth Watkins
Exhibition Sales Manager
Avionics Expo 2009
Email: GarethW@pennwell.com
Tel: +44 (0) 1992 656 672
Fax: +44 (0) 1992 656 700

Owned and Produced By:

PennWell®

Gary Nevison is chairman of the AFDEC RoHS team, and Customer Support Manager, Legislation and Environmental Affairs at Premier Farnell. As such he is our industry expert who will try and answer any questions that you might have relating to the issues of RoHS, WEEE and REACH. Your questions will be published together with Gary's answers in the following issues of Electronics World.

BACKYARD OR ROADSIDE RECYCLING

Europe now finds itself in the centre of the contentious issue of "backyard recycling".

Organohalogen compounds are, in general, non-hazardous but a ban is being considered in an attempt to prevent uncontrolled and unsafe recycling practices that are carried out in India, China and Africa.

The fact that this happens is not in question and many people, especially the young, are harmed by the toxic chemicals that are emitted when some of these substances are burnt over open fires to recover materials such as copper, silver and aluminium from electronic waste that has reached end-of-life.

The export of WEEE (Waste Electrical and Electronic Equipment) from the European Union to countries where these practices occur is illegal as the recycling processes do not meet the requirements of the WEEE Directive, while it is also against the requirements of the Basel Convention on trans-border shipment of hazardous waste. The Basel "ban" was also based around an attempt to stop the developed world shipping e-waste to developing countries, in particular for recycling. While Europe signed up to this convention it still happens. The US has yet to ratify the agreement and still ships significant amounts of e-waste at end of life to China and India, probably as the recycling costs are one tenth of those back home.

Dr Thuppil Venkatesh, advisor to the National Referral Centre for Lead Poisoning in India states that "53% of the children under 12 have levels of lead in their blood that is causing brain damage and restricting their ability to learn". He goes on to talk about one of the contributing factors saying: "We are seeing an increased number of cases because more and more electronic waste is being handled by our people."

Dr Venkatesh, in his address to a Hazardous Materials Seminar in Bangalore earlier this year explained that the estimated cost of lead poisoning among children in India is over $600m per year. Additional costs for adults excluded gastrointestinal disorders, anaemia, reproductive effects (including birth defects), cancer, kidney damage and cardiovascular disease (resulting from elevated blood pressure), which is 100% preventable.

While e-waste is burnt over open fires, acid baths are used to strip cable and PCBs for earnings of around $100 to $150 per month.

However, hazardous materials such as lead, cadmium, chromium, flame retardants and other toxins are found in e-waste. Inhaling, or regular handling of e-waste can result in damage to the brain, nervous system, lungs and kidneys, can cause cancer and even be fatal.

The raw materials in a computer for example, such as gold, copper coils, aluminium and other metals are worth money but to extract these, the motherboards are basically cooked, releasing arsenic, mercury, lead and other toxins which harm the body.

Despite the Basel Convention it is estimated that 50% of all US e-waste is "dumped" in India, China or Africa. Europe is far from blameless either, and an inspection of 18 ports around two years ago found that 47% of e-waste destined for export was illegal.

THE RAW MATERIALS IN A COMPUTER FOR EXAMPLE, SUCH AS GOLD, COPPER COILS, ALUMINIUM AND OTHER METALS ARE WORTH MONEY BUT TO EXTRACT THESE, THE MOTHERBOARDS ARE BASICALLY COOKED, RELEASING TOXINS

Dr Venkatesh summed the problem up by requesting that developed countries stop sending their old computers to help with education. "Please, no charity, do not send your old computers and cell phones to us – you are killing the children", which is a sobering thought.

However, with a high demand for computers and people willing to do the painstaking work to recycle them for low pay, the industry is growing despite the dangers. Experts claim that as many as five million people work in this trade in India, often with minimal protection. Greenpeace in India, for example, is well aware of the problem and understand how dangerous the recycling is and the primitive procedures in use. Dismantling often takes place by bare hand with no protection at all, a spokesperson said. They go on to say that while the lawmakers in India are aware of the problem they are loathed to implement rules that would remove jobs for the poorest people.

The problem is not consigned to India as many countries, in particular China, receive a share of the millions of tonnes of e-waste that disappears from the developed world every year only to reappear in developing counties, despite the international bans.

In Europe, the WEEE Directive has been introduced and focuses on the funding and safe disposal of electronic equipment at end-of-life that was placed on the market after August 2005.

There are very few regulated recycling plants in the developing world. However, without the necessary investment in such facilities the e-waste problem is likely to grow, not least because of the increasing number of computers sold around the world and the attraction to the developed world of recycling a PC for $2 rather than $20 back home.

Please email your questions to:
svetlana.josifovska@stjohnpatrick.com
marking them as RoHS or WEEE.

development

production

specialised

Whatever your programming needs, you'll find the solution at Dataman

Dataman's next generation programmers are built to meet the demands to support all device technologies and designed to achieve the highest speed of programming required for todays production.

Features...

- USB 2.0 and parallel connectivity
- Universal ZIF socket up to 8 x 48 pins
- Intelligent pin drivers allow varying voltages to be applied to any pin
- Multi-Programming support
- ISP capability with JTAG Interface
- Concurrent and Semi-concurrent gang programming
- Stand-alone operation with touch screen control
- Easy to use software supporting over 45,000 devices
- Free software upgrades and technical support for the life of the product
- All goods are ex-stock ready for same day despatch
- 30 day money back guarantee (returns during trial period are less than 1%)

from £295+VAT

For over 25 years Dataman have been at the forefront of supplying high quality, reliable programmers and this is maintained by offering up to three years parts and labour warranty on programmers.

DATAMAN

Dataman Programmers Ltd. Station Road
Maiden Newton, Dorset DT2 0AE UK
Tel (01300) 320719 Fax (01300) 321012

www.dataman.com

OLSON

Meter Range

Power Monitoring and Switching PDU

Part of the Extensive Range of Olson Electronics PDU with Local Ammeters and Power Meters, Remote Power Monitoring or Remote Power Switching and Monitoring

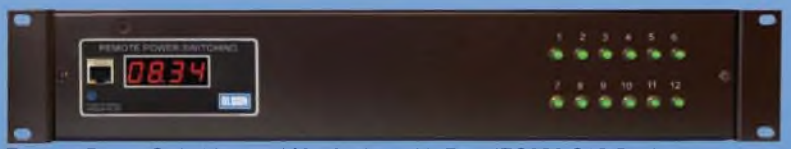
AM3262. Ammeter with Individually Switched Rear Facing IEC320 C13 Sockets

PM3280. Power Meter with IEC320 C13 Sockets, Individually Fused and Neons

AM/GER/6/R. Ammeter with German Sockets

RM1026. Remote Power Monitoring with UK 13A Sockets

RM1043. Remote Power Monitoring with UK 13A Sockets



Remote Power Switching and Monitoring with Rear IEC320 C13 Sockets

Ambox. In-line Ammeters and Power Meters with UK 13A and IEC309 Sockets

In-line Remote Power Monitoring with 32A IEC309 Sockets

Available with a range of sockets including:
IEC320 C13 and C19, UK 13A, International, IEC309 (BS4343) 16A and 32A

CALL OUR SALES HOTLINE

020 8905 7273

OLSON ELECTRONICS LIMITED

OLSON HOUSE, 490 HONEYPOT LANE, STANMORE, MIDDX HA7 1JY

TEL: 020 8905 7273 FAX: 020 8952 1232

email: sales@olson.co.uk web site: http://www.olson.co.uk

LOW DUTY CYCLE?

by Myk Dormer

The phrase 'low' ('limited' or 'restricted') duty cycle appears in a large number of ISM band allocation descriptions, as a favourite method of allowing multiple users without calling for the complicated radio hardware that other access schemes (multiple channel, spread spectrum or listen before talk) require.

The principle behind a low duty cycle system is very simple: by restricting the duration and rate of repetition of any one user's transmissions it becomes statistically unlikely that they will coincide (collide) with those of other, similarly limited, systems.

In practice, the actual restriction is specified as a 'duty cycle', usually between 0.1% and 10%, depending on the band and the intended usage. In layman's terms this reduces to "you stab the button at random and hope like hell that you're the only one transmitting at that instant".

There are certain implications that result from this type of operation: The transmitter must be designed for efficient use of the available time. It must switch on and off cleanly (not generating AM splatter, like a GSM cellphone does) and the switching needs to be as fast as possible to maximise the time allowed for data transmission. The data coding must minimise the amount of time lost in preamble and synchronising sequences, and the overall data rate should be as high as practical (within other limitations, such as channel bandwidth).

At some point, a collision with another transmission and resulting loss of data is inevitable. The overall design of the link must allow for this.

In the simplest case, this is handled by 'user feedback re-transmission' (the light doesn't turn on, so press the button again). Although amusingly simple, this is sufficient for a large proportion of simple control systems, including almost all car radio-keys.

Where more sophisticated systems are considered, and data integrity must be maintained, then a more effective means of dealing with data loss is needed.

Sending the same data more than once will reduce (but not eliminate) the probability of completely losing a vital piece of information. In such a case, the interval between re-transmissions must not be constant (a randomising function is required), or there is the risk of another, identical system in close proximity falling 'in step' and the re-transmissions always colliding.

Where no data loss is allowable (for example, in a data download application from a data logger), then a transmit/acknowledge protocol must be used. This requires transceivers at both ends of the link (opposed to the transmitter/receiver pair used by the simpler methods) and the transmission of a 'data received successfully' message by the destination end after each burst. The failure to receive such a message within a given time window will then cause the originating unit to re-send the same data. In this way, the transmission will be repeated until successfully received.

Additionally, once the complexity of a transceiver system has been implemented, then the user has the option of using other protocols beyond transmitting at random, as required (such as master/slave polling or master synchronised time slots), provided the actual transmission durations are within the spec limits.

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd
www.radiometrix.com

European Duty Cycle Limited SRD Bands

169MHz 0.1% to 10%, depending on the sub-band and transmit power.
433MHz 10% duty cycle, wideband (> 25kHz channel) 10mW transmitters.
(no restrictions on sub-1mW units, or narrowband systems).
868MHz Variously 0.1% to 100%, depending on the sub-band.
2.45GHz RFID allocation 15%.
See **ERC-REC 70-03** for more information.
In addition to the duty cycle limits, this specification also states absolute transmission time limits too (otherwise a "10% duty cycleî system could transmit constantly for a year and then stay quiet for nine...!)

Maximum total time on in any hour:

3.6 seconds	0.1% duty cycle
36 seconds	1 %
360 seconds	10%

Maximum length of any given transmission:

0.72 seconds	0.1% duty cycle
3.6 seconds	1 %
36 seconds	10%

Minimum 'off' time between transmissions:

0.72 seconds	0.1% duty cycle
3.6 seconds	1 %
36 seconds	10%

INTRODUCING

THE NEXT GENERATION OF OSCILLOSCOPES

The next generation of oscilloscopes designed by engineers who understand the needs of all engineers

Dont delay! See an online demo now at www.dlm2000.net

Or for further information, e-mail us at tce@nl.yokogawa.com

- Bandwidths 200-500 MHz
- Switchable 8 bit logic (mixed signal) input
- Memory up to 125 Mpoints
- Waveform acquisition rates up to 450,000 per second
- Sample rate up to 2.5 GS/s

Higher performance, lower cost

QUALITY ■ INNOVATION ■ FORESIGHT

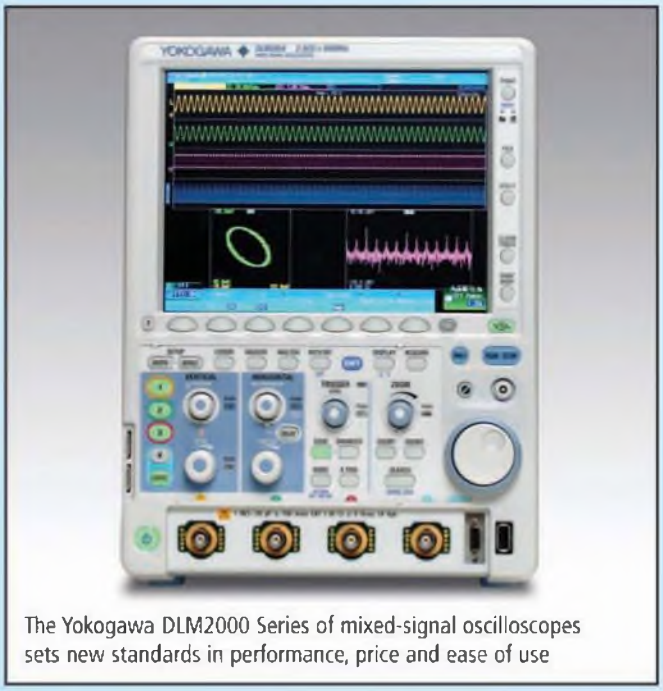
YOKOGAWA

YOKOGAWA EUROPE B.V.
The Netherlands,
Tel: + 31 (0) 33 464 1858
Fax: + 31 (0) 33 464 1859
tce@nl.yokogawa.com
www.yokogawa.com/tm

Yokogawa launches DLM2000 mixed-signal oscilloscope family

The new Yokogawa DLM2000 Series is a new family of mixed-signal oscilloscopes (MSOs) that represent a major step forward in terms of price/performance specification and ease of use.

With up to 500 MHz bandwidth and 2.5 GS/s sampling speed, the new oscilloscopes have the longest memory (up to 125 M points) and fastest update rate (up to 450,000 waveforms per second) in this class of instrument. In addition, the combination of flexible analogue and digital inputs, plus a large-screen display in a compact ergonomically styled body, makes the instruments exceptionally easy to use.



The Yokogawa DLM2000 Series of mixed-signal oscilloscopes sets new standards in performance, price and ease of use

In addition to the key performance specifications, the DLM2000 Series features a number of advanced measurement and analysis features, including histogram and trending functions, up to 20,000 history memories, digital filtering, zoom windows, user-defined mathematics and serial bus analysis.

The DLM2000 Series consists of six models: three with two channels and three with four, each covering the bandwidths 200, 350 and 500 MHz, respectively. Mixed-signal oscilloscope operation is enabled on the 4-channel models by converting the fourth channel of analogue input to 8-bit logic, so that the instrument then functions as a 3-channel analogue plus 8-bit logic MSO. A high-resolution mode (up to 12-bit) is also available. This logic capability is complemented by the availability of new logic probes with individual bit threshold setting and 100 kilohm input impedance at 250 MHz.

The new instruments feature a large (8.4 inch, 21.3 cm) high-resolution (XGA) display in a compact 'portrait' format package that occupies only two thirds of the area of a single A4 sheet on the benchtop. The display is enhanced by a fine grid, high luminance and viewing angle, and on-screen markers with simultaneous display of cursors and automatic parameters. Other features include backlit buttons, additional knobs and jog shuttle, on-screen information in English, German, French, Italian and Spanish languages, two zoom windows with 80:20 or 50:50 zoom/main area split, and a choice of first-cycle or screen average mode for frequency measurement.

The combination of long memory and the history function, along with sophisticated trigger and search capabilities, means that the chances of missing elusive or intermittent waveforms are minimised. Using the /M2 option, up to 125 M points of storage capacity is available, allowing, for example, 10 kHz signals to be recorded for up to 5000 seconds. Even at a sampling rate of 1.25 GS/s, waveforms down to 0.1 sec can be captured.

With the history function, up to 20,000 previously captured waveforms can be saved in the acquisition memory, and any one or all of them can be displayed on screen with the ability to carry out cursor measurements and other analysis operations including FFT analysis and comprehensive user-defined maths. Waveforms can be displayed one at a time, in order, or automatically played back, paused, fast-forwarded or rewound.

CAN waveform of 12.5 M points (5 sec duration) showing use of the zoom window

The DLM2000 Series comes with a variety of easy-to-configure triggers combining analogue and logic inputs such as edge, enhanced and B-triggers. These include dedicated trigger functions for CAN, LIN, UART, I2C and SPI serial bus patterns as well as the ability to perform simultaneous analyses on two different buses operating at different speeds. This capability is enhanced by the extensive search facilities, allowing the user to look for specific data in the very long memory. The 4-channel models in the DLM2000 Series are also able to import the CAN DBC database and either trigger on, or decode, a physical value.

Prices for the DLM2000 Series start at €3300.

A dedicated web site has been set up for the Yokogawa DLM2000 Series at www.dlm2000.net

ACTIVE FILTERING FOR LOWER LOAD CAPACITANCE IN NOISE-SENSITIVE APPLICATIONS

CHESTER FIREK, PRODUCT MARKETING MANAGER, AND **BOB KENT**, APPLICATIONS ENGINEER, BOTH FROM PICOR, DISCUSS A TYPICAL OFF-THE-SHELF ISOLATED DC-DC CONVERTER TO DEMONSTRATE HOW AN ACTIVE FILTER WILL PROVIDE SUPERIOR FILTERING BUT ALSO A SIMPLE SOLUTION TO MEET TRANSIENT RESPONSE REQUIREMENTS

Power architects engaged in designing systems requiring low output noise and fast transient response, such as RF transmitters, power amplifiers, test systems, displays and designs supporting low voltage ASICs and laser diode transmitters, understand that when attempting to tailor power systems to meet both requirements using passive components, the two objectives become diametrically opposed. Minimising periodic and random deviations (PARD) requires filtering, whereas fast transient response is impeded by filtering.

The characteristics of the DC-DC converter, the load, the electrical characteristics of the passive components and the available PCB area all present additional design constraints that further limit the designer's options. This task becomes more difficult if the designer is unable to begin the design with an optimised DC-DC converter, to match the transient and noise requirements. This may be due to either lack of in-house design resources, a short design window, or the desire to use products already on their approved vendor list. In this instance, a high efficiency off-the-shelf DC-DC converter may be used.

This article uses a typical off-the-shelf isolated DC-DC converter to demonstrate how an active filter will not only provide superior filtering, as compared to the passive approach, but will also provide a simple turn-key solution to meet challenging transient response requirements. This approach can either eliminate the need for load capacitance all together for noise reduction, or reduce the amount required by as much as a factor of ten for equivalent transient capability. The performance improvements demonstrated here would also apply to applications using optimised custom DC-DC converters.

DC-DC CONVERTER CONSIDERATIONS

In order to properly understand the issues involved in optimising a "power system" for low noise and fast transient response, it is important to first establish the base-line performance of the DC-DC converter. Many of today's off-the-shelf high-density switch-mode power converters are designed to optimise for power density and efficiency, two of the most commonly used criteria for converter selection. DC-DC converters are only part of the total power system.

Although the output ripple and noise levels from some converters are adequate for the needs of today's end systems, they may not be adequate for some of the more sensitive analogue or digital systems. And as a power component, the DC-DC converter will generally provide a good current-source "engine" to support load transients, but will generally not have much internal energy storage capability. Parameters such as low ripple and fast transient response are design trade-offs for density and efficiency and, because specific needs may vary from application to application, the DC-DC manufacturer will provide methods to further optimise these parameters with the use of external components, rather than add them internally to the converter.

The ability of the converter to be optimised (with external components) for low noise and fast transient response will depend on the converter topology, switching frequency and any limitations the converter manufacturer may impose on use of external components; i.e. maximum load capacitance.

OPTIONS FOR REDUCING RIPPLE

The two major sources of ripple and noise on the output of a DC-DC converter are the switching noise generated by the converter and the line ripple from the

	Output Voltage		
	5 V	12 V	24 V
No Additional Filter	100 mV	150 mV	240 mV
Low ESR Cap	50 mV	75 mV	120 mV
LC Output Filter	20 mV	35 mV	50 mV
QPO and uRAM Series Active Filters	<10 mV	<10 mV	<10 mV

Table 1: *Output ripple specifications for isolated DC-DC converters with various filter solutions*

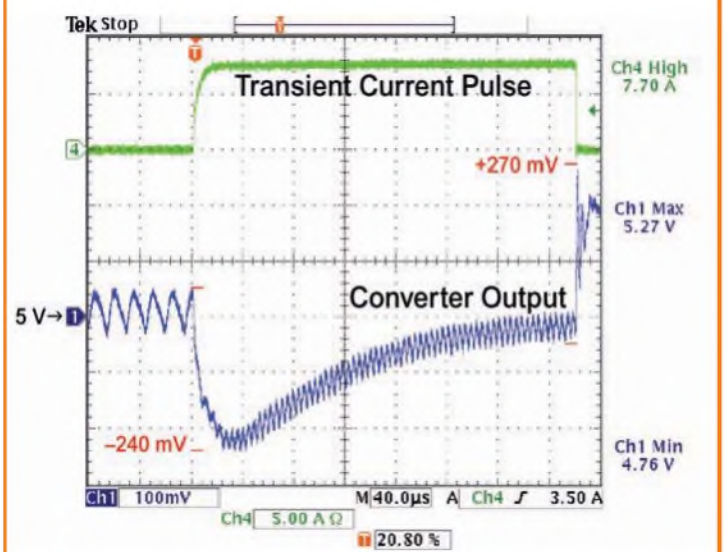


Figure 1: *Transient load current with a 5V output converter*

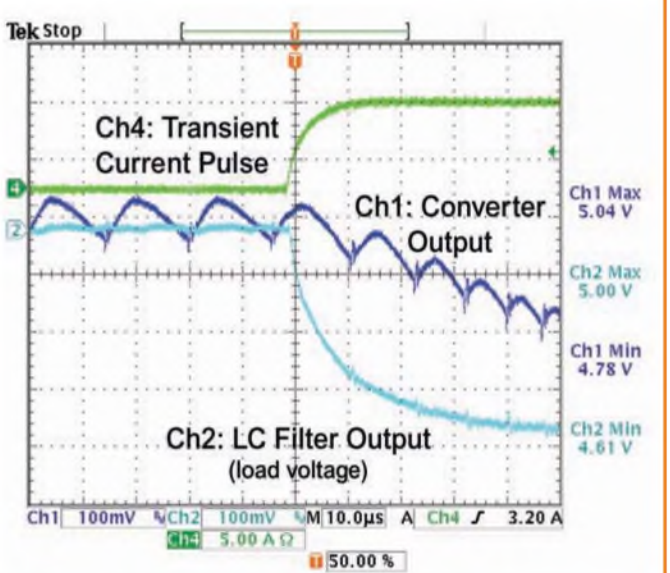


Figure 2: *Test setup, DC-DC converter with LC filter*

converter source (usually 120Hz if powered by an off-line source). For the line ripple, a DC-DC converter will provide some level of ripple rejection; any remaining ripple will appear at the load.

In general terms, the output ripple specification for a regulated DC-DC converter can range anywhere from 100mVp-p (5V output) to 240mVp-p (24V output) or more, depending on the converter. As a percentage of output voltage, the range could be 2% for a 5Vout converter and 1% for a 24Vout converter (see **Table 1**). The addition of low ESR (Equivalent Series Resistance) capacitors can reduce the ripple by up to 50%; using the previous examples would yield a range of 50mV to 120mVp-p.

Further reduction in ripple can be achieved by adding an inductor, with low DC resistance, in series. Adding an inductor can provide up to an additional 50-60% improvement; reducing the ripple to roughly 20mVp-p for a 5Vout converter and 50mVp-p, or more for a 24Vout converter. Although the improvement is significant, an application using a 28V RF Power Amplifier (PA) may require the ripple levels to be as low as 10mVp-p or less, to prevent sideband frequency peaks. Further improvements to reduce input line reflected ripple would require better attenuation at low frequencies, which requires the use of larger inductors and more capacitance. For space savings, the more practical approach to attenuate the remaining lower frequency noise is to use active filtering.

TRANSIENT RESPONSE

Noise-sensitive applications such as RF power amplifiers and laser diode transmitters also require very fast transient load response. In the case of an RF power amplifier, the system may operate steady-state at 10% load and then have the load increase to nearly 100% almost instantaneously. For the average DC-DC converter the response to a large load step can take a few hundred microseconds, where the PA may require the load to recover in less than one hundred microseconds. For an off-the-shelf isolated DC-DC converter, the response time for the control feedback loop (approximately equal to 1/5 the converter switching frequency) is far too slow to be able to recognise a transient event and respond to it in enough time to avoid a significant droop in output voltage.

Adding passive components further slows down the converter loop response. Active filters provide a buffer between the DC-DC converter and the load as opposed to passive solutions that do not offer this capability. The load response is provided primarily by the active filter, which can provide a loop response several orders of magnitude faster than the DC-DC converter. The waveforms in **Figure 1** depict a typical converter's response to a 7.7A transient load current with no external filtering or capacitance.

For the converter in Figure 1, the steady-state output ripple is approximately 100mVp-p, far too high for most noise-sensitive applications. However, the larger concern for system designers may be the droop in output voltage. In the example shown, the output droops when the load transient event begins and then overshoots at the end of the transient event when the load current falls creating an overall output voltage deviation of approximately ±250mV, which once again will be an issue in a sensitive application.

In order to provide a quicker response to load transients, additional output hold-up capacitance usually needs to be added as a source of current to satisfy the additional load. Depending on the transient requirements, this could mean that a very large amount of extra capacitance would need to be added. The drawbacks to adding extra capacitors are the cost of the components, the board space they occupy and the impact of additional capacitors on system reliability.

Furthermore, capacitors do not provide an ideal solution as there will still be an inherent transient voltage drop due to a capacitor's internal ESR. The ability of this

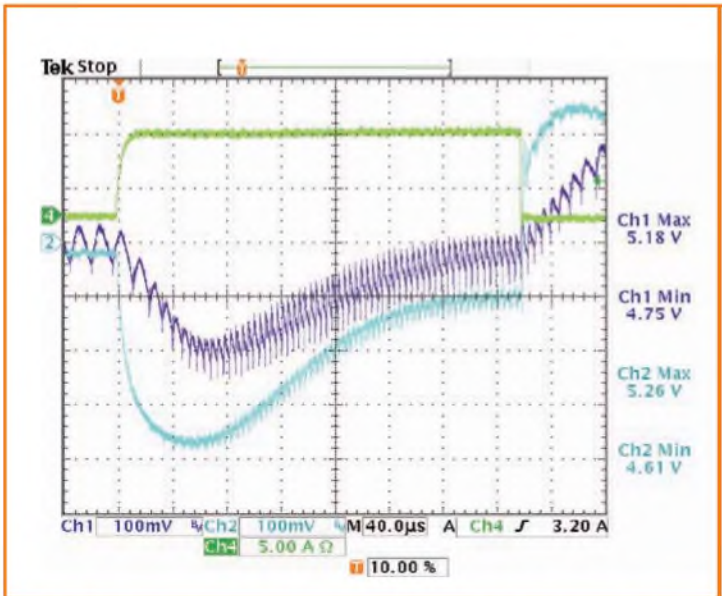


Figure 3: Ripple and load response of a 5V out converter using a LC filter on the output

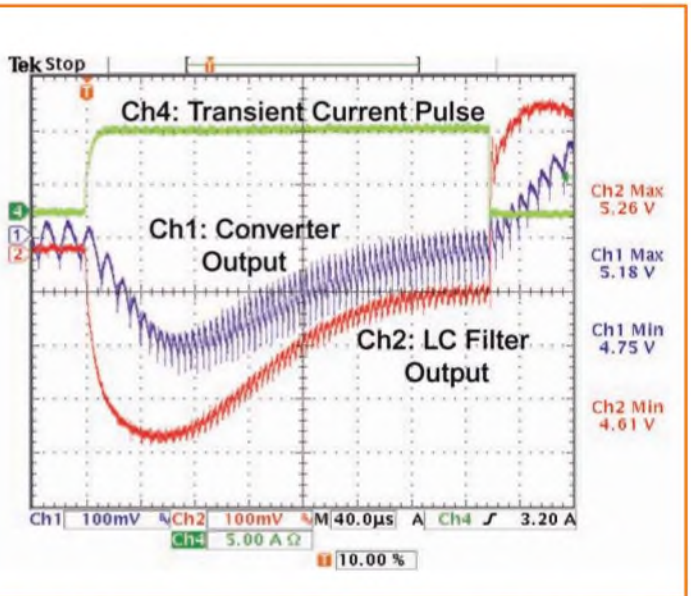


Figure 4: Complete transient load event with a 5V out converter and LC network

configuration to maintain a clean stable output voltage during a transient is dubious.

LC FILTER NETWORKS

The most common method of filtering output ripple is to add inductance in series and capacitance in parallel at the output of the converter, commonly referred to as an "LC network", as shown in **Figure 2**. As illustrated in Table 1, the inductor in the LC network helps provide better ripple attenuation than the capacitor alone.

The inherent problem with adding inductance is that when a transient load occurs, the current through the inductor cannot change fast enough to provide current to the load, so all the energy must be supplied by the load capacitor(s). The amount of capacitance that is required will depend on the system requirement and change in load current versus time [di/dt]. But as the capacitors provide the necessary current, there may still be an unwanted drop in output voltage due to the non-ideal parasitic factors. It's equal to the value of the transient current multiplied by the equivalent series resistance (ESR) of the capacitor(s) and the frequency dependent drop across the electrical series inductance (ESL).

The waveforms in **Figures 3** and **4** show the results of the LC network filtering on the converter output ripple (Ch2). Although the ripple is significantly reduced the transient drop in load voltage has increased. At the start of the transient there is a sharp drop in the output voltage from the filter. Since the current through the inductor cannot change instantaneously, the current for the transient load must come from the output capacitors. This initial voltage drop is the result of the transient current multiplied by the capacitor ESR.

To reduce the voltage drop, the overall ESR of the output capacitance would have to be reduced by either careful selection of lower ESR caps or by using more capacitors to parallel the ESR component. In this instance, the voltage at the load droops by more than 300mV before the converter starts to recover, and bring the output up to the regulation voltage.

The waveforms in Figure 4 show the complete transient event and the resulting undershoot and overshoot of the LC filter, due to the LC filter ringing at its resonate frequency. By the end of the transient, the current through the inductor is providing the transient load current. When the load transient ends, the current through the inductor remains the same, since it cannot change instantaneously, and gets dumped into the load capacitors. Forcing this stored energy into the capacitors raises the output voltage by about 300mV, resulting in a peak to peak variation of 600mV due to the transient load change.

ADDING "HOLD-UP" CAPACITANCE

To compensate for such a dramatic variation in output voltage, additional capacitance needs to be added at the load to "hold-up" the voltage at the load. To consider the affects of load capacitance, the same circuit will first be demonstrated without the inductor. The waveforms in **Figure 5** show the same converter output voltage during the transient load with an additional 8mF of capacitance on the converter output.

In this instance the added capacitance reduced the voltage droop to roughly 100mV, rather than 300mV with the LC filter. As expected, the amplitude of the ripple has reduced (to approximately 40mVp-p) as compared to the stand-alone DC-DC converter; even though the ripple is higher than with the LC filter.

Using this approach's results improved overall performance, but still they should be weighed against the total size of the solution, as well as any potential reliability issues relating to compatibility with the converter. (Note: Most DC-DC manufacturers place limits on the amount

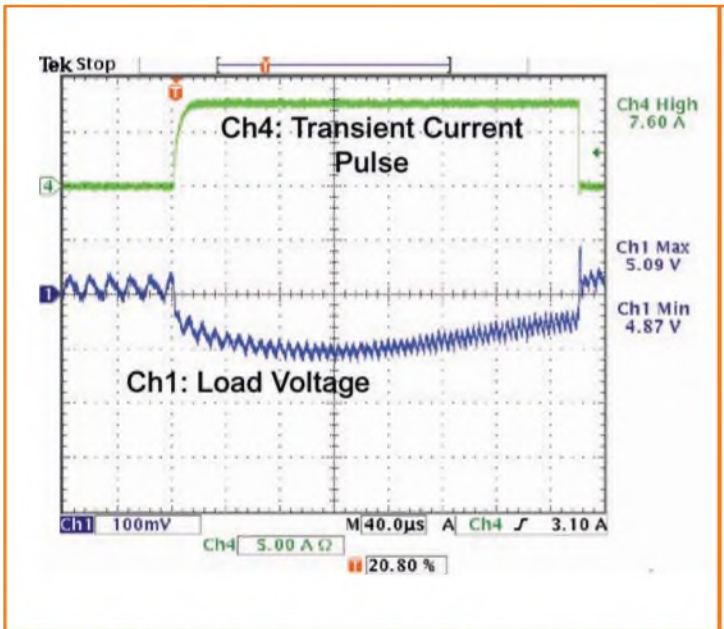


Figure 5: *Transient load current with a 5V out converter and eight parallel 1mF caps (8mF total)*

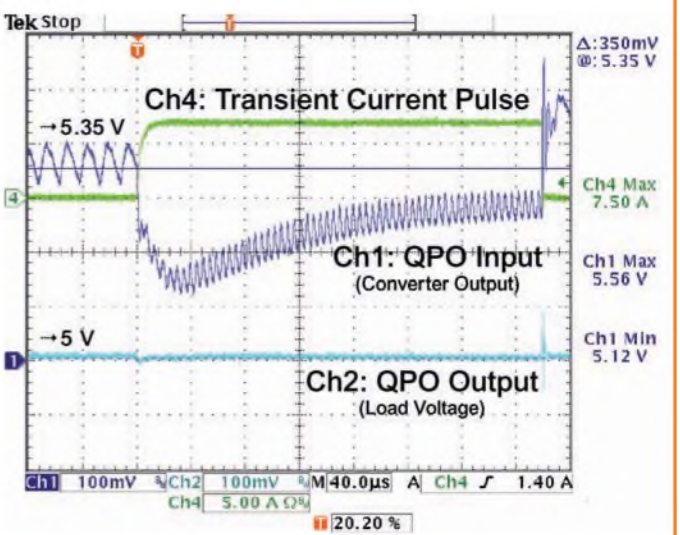


Figure 6: *Test setup, 5V out converter with 1.4µH inductor and 8mF of load capacitance*

of capacitance that can be added to the output of the converter in order to avoid loop stability issues. In the example shown above the maximum capacitance value set by the converter manufacturer was exceeded in order to demonstrate an extreme case. Always refer to the manufacturer's DC-DC converter specifications to determine acceptable capacitance levels.)

COMBINING HOLD-UP CAPACITANCE WITH INDUCTANCE

Figure 6 shows a test circuit combining the 1.4µH inductor from the LC filter with the 8mF of hold-up capacitance from the previous example. The resultant waveforms in **Figure 7** show that the output ripple has improved but the transient response has degraded slightly. Since the resonant frequency of the LC filter is much lower with the 8mF of capacitance, it is clear that the first step in voltage is due to the capacitor's ESR and the reactance of the inductor.

In this example, the load capacitance was increased by more than ten times the amount used in the first LC filter example shown in Figure 2; the benefit of hold-up capacitance appears to have been maximised. Adding the inductor has, once again, reduced the ripple levels. Further reduction in ripple may be possible with larger inductors. These nearly optimised results of a passive design can now be compared to the performance of an active filter.

ACTIVE FILTERING AND TRANSIENT RESPONSE

As illustrated in the previous examples, the primary drawbacks in the passive approach are the effect of the inductance on transient response, and the voltage drop across the hold-up capacitance. Active filters provide improved transient response by replacing the passive inductance, which has inherently slow di/dt, with much faster and smaller active components as shown in **Figure 8**.

In the active approach the inductor reactance is replaced by a power FET and a high speed controller device that modulates the FET to create linear resistance. During a transient condition, the loop gain of the filter increases the effect of capacitance at the input to the filter by a ratio of the change in the input voltage of the filter divided by the change in the output voltage of the filter (ΔVin/ΔVout), drastically reducing the amount of capacitance required while decreasing transient di/dt response time.

Active filters, such as Picor's QPO and uRAM models, are able to respond to transients much faster than converters by decreasing the internal resistance path between its positive input and output pins. Since the voltage is greater on the QPO input than its output, this voltage difference can be used to compensate for the additional load requirements of the transient. This voltage difference (ΔVhr), referred to as the headroom voltage, is selected by the user, providing an output voltage on the converter that is greater than the desired load voltage. During the transient, the output of the converter will droop and the active filter will compensate by reducing the headroom voltage, to maintain a constant output voltage, provided that the voltage droop is not greater than the selected ΔVhr. The minimum voltage drop by the active loop of the QPO is based on the QPO minimum resistance.

The waveforms in **Figure 9** demonstrate the ability of the QPO to filter both the ripple voltage from the converter, as well as the voltage droop of the converter during a transient load event.

In this example the QPO test board was designed to have 350mV of headroom voltage under low-load

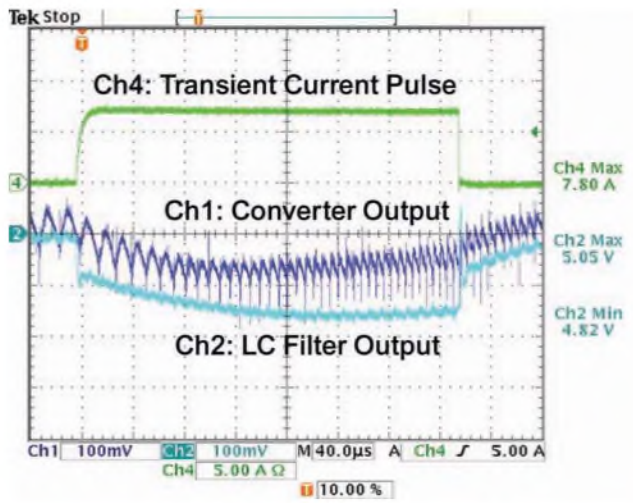


Figure 7: *Transient load current with 1.4µH inductor and 8mF of load capacitance*

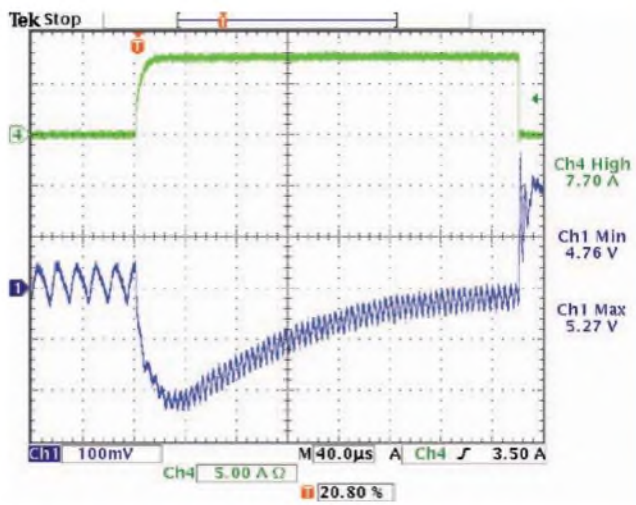


Figure 8: *Test set-up, 5V out converter with QPO-1 active output filter*

conditions, which for this test was a 1A constant load. Ch1 is the voltage seen on the QPO input; Ch2 is the QPO output voltage. Both channels are DC measurements with a 5V offset and referenced two divisions down from centre.

In Figure 9 the load step (Ch4) monitors the transient current only and does not include the static 1A load. Examining the plot, starting with the left edge of the waveforms, the average DC voltage difference between Ch1 and Ch2 is 350mV. After about 80µs, the transient current event occurs (~ 1A/µs) and the voltage from the converter (Ch1) droops. The QPO output voltage (Ch2) remains constant at 5V for the entire duration of the transient. As a result the QPO filter virtually eliminates the ripple and the load voltage drop associated with the 7.7A transient, with no additional capacitance, significantly outperforming all of the passive scenarios.

ANALYSING THE POWER SYSTEM

When designing power systems that require low noise and fast transient response, it is important to understand the trade-offs and limitations of all the components that will make up the "power system", i.e. the DC-DC converter, filter and hold-up capacitors. The DC-DC converter will produce the base-line from which to improve upon.

Adding passive filter components to the output of the DC-DC will reduce ripple but this will result in a negative affect on transient response and may potentially create stability issues. More capacitance will be needed to improve transient response. Depending on the amount of ripple and transient response improvement needed, the passive solution may also become very large, potentially making the solution space prohibitive.

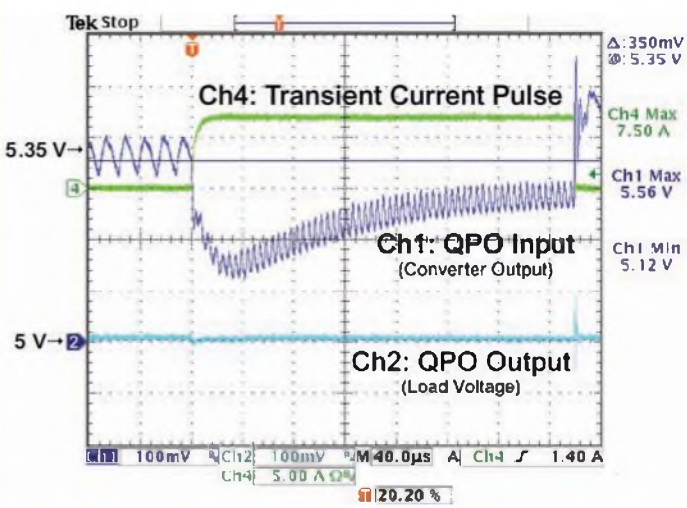


Figure 9: *Transient load with the same 5V out converter and a QPO active output filter*

As demonstrated in the previous examples, active filtering provides better overall filtering and load transient performance than a passive approach due to faster loop response and lower resistance. In the example provided in Figures 8 and 9, the QPO-1 demonstrated a significant improvement in transient response with no additional load capacitance present. By reducing the amount of load capacitance required in low noise, high transient load systems, the power design can become optimised for both performance and size.

KIT-BASED APPROACH FOR ACCELERATED ADOPTION OF LOW-POWER TECHNIQUES

NEIL HAND DESCRIBES THE CONCEPT OF A "LOW-POWER KIT" THAT ENABLES DESIGNERS WITH AND WITHOUT LOW-POWER EXPERTISE TO ADOPT ADVANCED LOW-POWER TECHNIQUES EFFICIENTLY AND EFFECTIVELY

In recent years, power consumption has moved to the forefront of ASIC and system-on-chip (SoC) development concerns. The combination of higher clock speeds, greater functional integration and smaller process geometries has contributed to significant growth in power density. Furthermore, with every new process generation, leakage power consumption increases at an exponential rate.

A wide variety of low-power design techniques have been developed to address the various aspects of the power problem, including the use of clock gating, multi-switching threshold (multi-Vt) transistors, multi-supply multi-voltage (MSV), substrate biasing, dynamic voltage and frequency scaling (DVFS) and power shut-off (PSO).

ADDRESSING LOW POWER

However, "Low power" isn't just something that can be "bolted on" at the end of the development process. Power, timing and area are overlapping and potentially conflicting goals that need to be balanced throughout the flow.

To meet aggressive design schedules, it is no longer sufficient to consider power only in the implementation phase of the design. The size and complexity of today's ICs make it imperative to consider power throughout the design process, from the chip/system architectural phase, through the implementation architecture phase, through design (including micro-architecture decisions), and all the way to implementation with power-aware synthesis, placement and routing. Similarly, to prevent functional issues from surfacing in the final silicon, power-aware verification must be performed throughout the development process.

To address low power issues, today's design environments boast a wide variety of sophisticated power-aware tools and methodologies. However, even with the high level of automation that such tools provide, applying these techniques can require substantial effort, introduce risk and can increase the complexity associated with design, implementation and verification.

In order to ensure smooth adoption of low-power techniques, we need a way to enable all team members regardless of low-power experience to utilise the capabilities at their disposal, without needing to become low-power experts, or to learn by trial and error.

This article describes the concept of a "low-power kit" that enables teams with and without low-power expertise to adopt advanced low-power techniques efficiently and effectively. A low-power kit gathers expert knowledge and best practices to: eliminate common problems, establish flows to ensure tools and technologies are applied to achieve the best results, and establish processes to ensure predictability.

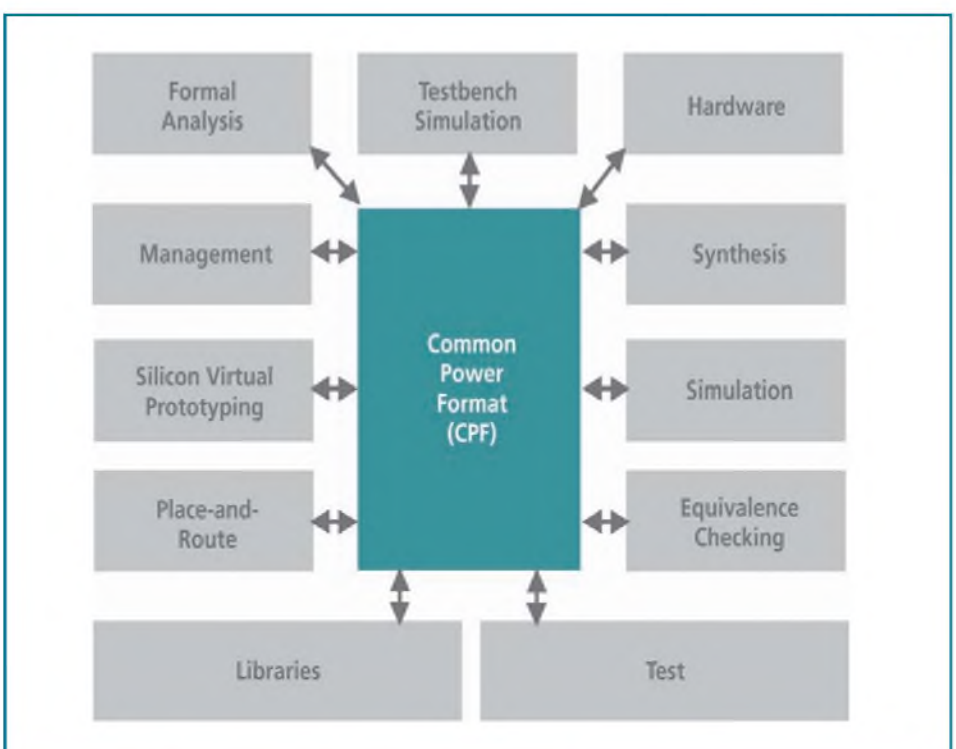


***Figure 1:** CPF provides a holistic specification of power intent used throughout design, implementation and verification*

THE COMMON POWER FORMAT

Common Power Format (CPF), managed under the auspices of the Silicon Integration Initiative (Si2) consortium's Low-Power Coalition, provides a mechanism to capture architects' and designers' intent for power management, enables the automation of advanced low-power design techniques and allows "what if" exploration to take place without RTL changes.

The benefit of using CPF within a low-power kit is the ability to drive the design, verification and implementation from a single "golden" power intent description (**Figure 1**). A high level of automation within the tools around this central description eliminates many of the error prone tasks typically associated with low-power design.

A REPRESENTATIVE DESIGN

A variety of different considerations must be taken into account when creating a low-power kit. First and foremost, it is necessary to create a representative design that embraces all the low-power aspects of the typical designs you will be working on. This allows the different aspects of the kit to be proven out and demonstrated, and provides adopters with a well defined sandbox in which to experiment and learn. Additionally, this design can act as a pipe-cleaner whenever tool or silicon vendor changes are made.

As an example, consider an IEEE 802.11-based wireless access device comprising various interfaces and peripherals. At the core of this device will be a SoC containing a variety of functional blocks. A block diagram of the functions comprising such a representative design is shown in **Figure 2**. This will typically include some hard macros such as a microprocessor core, as well as a variety of first and third-party IP (both Verilog and VHDL) – many of which may utilise power-saving techniques.

In addition to all of the purely digital logic, there will likely be a number of analogue/mixed-signal (AMS) blocks that must be accommodated by our design environment, such as a phase-locked loop (PLL) in the clock generator and any physical-layer (PHY) interfaces.

To facilitate understanding, the kit should be partitioned into a number of

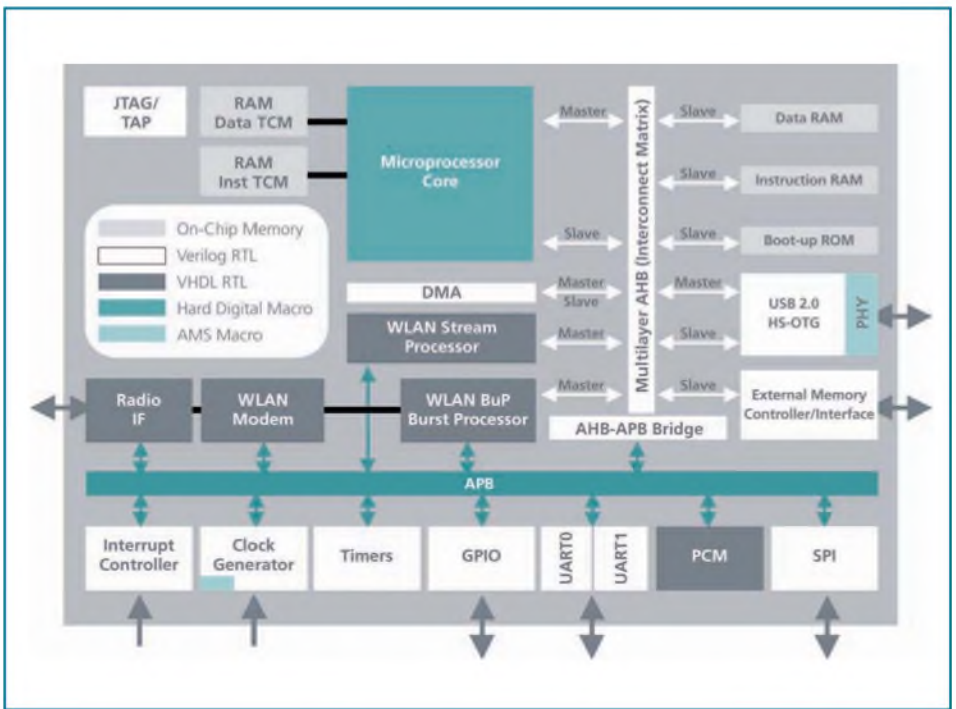


***Figure 2:** Functional block diagram for an example representative design*

main categories; for example: Design Environment, Low-Power Techniques, Design Creation, Physical Implementation, Verification and Management. In turn, each of these categories should comprise a number of discrete modules and flows (**Figure 3**). Design and verification teams then need to use only those modules appropriate for their particular design.

Where applicable, each module should include background information pertaining to this aspect of the design, best practices, checklists, recommended flows, scripts to demonstrate the flows, training material and documentation.

DESIGN ENVIRONMENT

This category should cover everything required to establish a complete low-power design environment for a new project, including infrastructure, tools, IP components and detailed checklists and dependencies.

Some example modules are:

Library Ensures the necessary view and databases

Qualification are available for successful low-power flows

Process Defines how low-power affects process selection

Selection and what is needed based on design requirements

Infrastructure Provides data management and system infrastructure to ensure a smooth low-power implementation.

LOW-POWER TECHNIQUES

This category should cover the various low-power techniques that may be employed in a design and that are supported by the design environment. Tradeoff analysis should also be performed to determine the most appropriate techniques to apply.

Some example modules are:

Multi-Threshold Voltages When and how to use this highly automated technique effectively.

Low-Power Clocking As a major contributor to power consumption, managing clocks effectively is key to a low-power implementation.

Multi-Supply Voltages Defines the benefits and pitfalls of MSV and what is needed to implement it in a design.

Power Shut-Off (PSO) PSO has substantial power benefits, but it needs to be applied appropriately as it affects all areas of the design process.

Dynamic Voltage and Frequency Scaling (DVFS) techniques may also have substantial power benefits, but ensuring that the performance-voltage-frequency feedback mechanism works correctly can be a challenge.

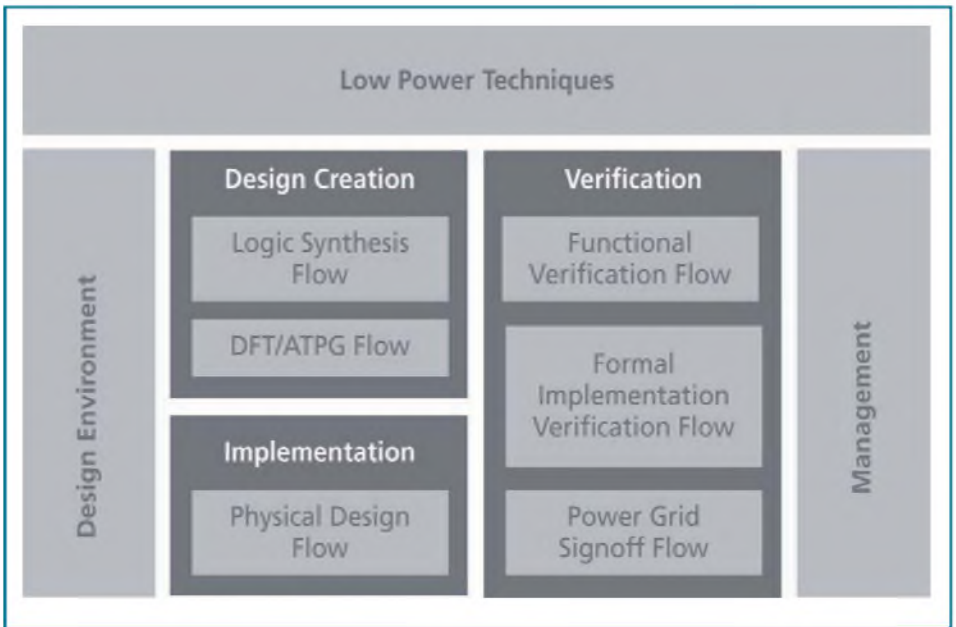


Figure 3: The low-power kit should feature a number of categories, modules and flows

MANAGEMENT

This category should cover the various facets of managing a low-power design, from planning a verification strategy, defining metrics and estimation techniques, to implementing a low-power engineering change order (ECO) methodology.

Some example modules are:

Low-Power ECO Track all data and flow dependencies to ensure that late-stage changes do not cause problems.

Methodology, Planning, Metrics and Analysis Predictability is ensured through proper metrics and planning, and must be considered throughout the design process.

DESIGN CREATION

This category should cover all design creation aspects of the flow, including performing architectural tradeoffs among power, timing and area, along with best practices for success with designs employing MSV and/or PSO techniques.

The modules included in this category might be as follows:

Architecture Tradeoff Compare different techniques and how they affect total power within your class of designs.

RTL Design Covers what can be done in RTL to affect power consumption, as well as how the different techniques are codified.

CPF Creation Effective power intent representation using the Common Power Format including templates for your design styles.

Low-Power Synthesis How synthesis affects the power process and how to implement the most effective synthesis for a low-power design.

Power-Aware DFT Power affects both normal modes of operation and test and must be considered throughout.

The flows covering these modules should utilise the golden RTL and CPF files together with simultaneous optimisation of all constraints (timing, area and power) to create an optimised netlist that includes all of the relevant low-power structures including level-shifters, isolation cells and retention logic.

PHYSICAL IMPLEMENTATION

This category should cover all the aspects of physical design from netlist through design signoff. As with Design Creation, the golden CPF file should be used to communicate power intent throughout the flow.

Some example modules are:

Prototyping and Parasitic Correlation Many iterations of floorplan optimisation may be needed on the road to timing closure. Accurate parasitic scaling between detailed extraction and prototyping extraction speeds this up.

Power Planning Proper selection of a power distribution scheme (grid or ring) must be taken into account for low- and non-low-power blocks.

Low-Power Floorplanning Determine the best location for sensitive blocks. Rules may govern that blocks with the same voltage are located in close proximity or closer to pad I/Os, for example.

Timing and Signal Integrity Closure Even if power intent is considered to be the most important, timing and SI specifications must be met to obtain a functional design.

VERIFICATION

The importance of verification within a low-power flow can best be illustrated by considering just a few of the challenges when utilising the PSO technique.

At the functional level we need to ensure that powered-down logic does not cause invalid data to propagate, that any necessary state is retained during power down and that power sequencing ensures successful power-up.

During implementation we need to verify that the appropriate isolation cells and other power structures are in place.

Finally, during power grid signoff, we need to make sure that any in-rush current during power-on of the PSO block does not corrupt surrounding logic.

Some example modules are:

Low-Power Functional Verification Power intent can directly affect functional intent, so functionality must be verified in the context of the final power implementation using techniques such as simulation and assertion-based verification.

Low-Power Formal Implementation Verification Defines a process to ensure that the low-power implementation chosen is correct and consistent through all design transformations.

Power-Grid Signoff Prior to signoff, verify that the static and dynamic behaviour of the power grid meets all requirements for correct operation.

AN EFFECTIVE WAY

Utilising a kit-based approach to low-power design as described here, together with a common power format such as CPF, is a highly effective way to capture and communicate low-power knowledge throughout an organisation, allowing designers of different experience levels to effectively and efficiently adopt advanced low-power techniques. ■

YAMAICHI ELECTRONICS

Innovations from another dimension

Yamaichi Electronics is the specialist for advanced connection technology. We are committed to our service quality, to the development of specific products and the quality of our products. Our reaction is also the key to our success.

www.yamaichi.eu

Another Dimension

Connector systems

YAMAICHI ELECTRONICS
Great Britain Ltd.

Unit 4,
Woodlands Business Village
Coronation Road, Basingstoke
Hampshire RG21 4JX, England
Phone: +44 / 1256 / 463 131
Fax: +44 / 1256 / 463 132
sales@yamaichi.co.uk
www.yamaichi.eu

POWER MANAGEMENT ICS
OPTIMISE BEST-IN-CLASS CIRCUIT BLOCKS

STEVE KNOTH, PRODUCT MARKETING ENGINEER AT LINEAR TECHNOLOGY CORPORATION, LOOKS AT POWER MANAGEMENT INTEGRATED CIRCUITS (PMICS) OPTIONS AVAILABLE TO DESIGNERS TODAY

Unprecedented challenges face designers of today's battery-powered portable electronic products. Among these are the demands for high performance power management systems to accommodate growing system complexity and higher power budgets. These systems strive for an optimum balance among long battery run-time, compatibility with multiple power sources, high power density, small size and effective thermal management.

A new breed of power management integrated circuits (PMIC) is available to efficiently power these systems – much smaller in footprint and much higher in performance than the "traditional" PMIC. This is changing the way product designers can configure and partition their systems

The PMIC arose primarily from the need to save PC board space via higher levels of integration of multiple discrete power IC functions, such as low dropout regulators, switching regulators, interface circuits and, in some cases, even battery chargers. Over the past five to ten years, these "system on a chip" (SOC) type ICs have become commonplace. However, they are quite large and many come with "hidden" costs and performance limitations for the designer.

However, there are now more optimised solutions – a new generation of PMICs that consolidate the "hard to do" functional circuit blocks such as power path management, high efficiency synchronous switching regulators, USB On-the-Go, over-voltage protection, high voltage input capability and full-featured battery chargers, while at the same time raising the overall performance bar. Their small form-factor, low-profile packaging and minimal external components allow for simple, compact and cost-effective solutions for handheld electronic devices, especially those utilising USB power.

DESIGNING AROUND "OVER-INTEGRATION"

Let the "buyer beware!": some PMICs may save board space, but many come with hidden costs, additional required design time and performance limitations for the designer. The industry standard PMIC has been relatively large in form-factor, generates lots of localised heat and contains a number of functions that are not necessarily needed by the application, thus adding complexity and causing the need to "design around them".

In many design cases, even if integration was absolutely necessary, designers had no choice but to pay for the extra functionality, even though they would use only a subset of the total chip's functionality. Many customers comment that they spend more time designing around what they do not need, rather than what they do want. The alternative has been to use multiple ICs plus a discrete component approach, which in turn takes more board space, adds cost, increases manufacturing complexity and grows the bill of materials.

REDUCING HEAT

Many industry-standard PMICs come with a variety of linear regulators onboard However, linear regulators, if not managed

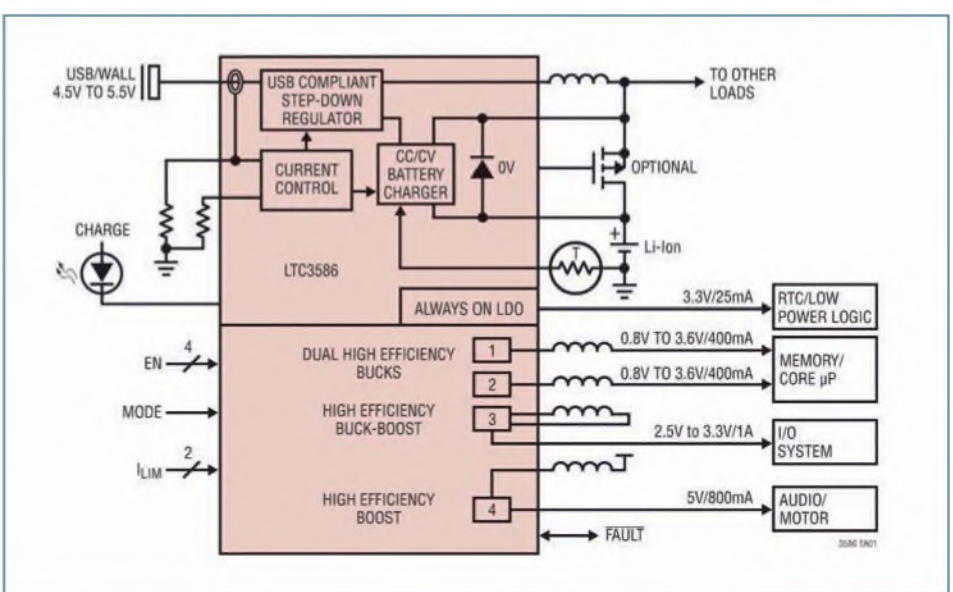


Figure 1: *LTC3586 simplified block diagram*

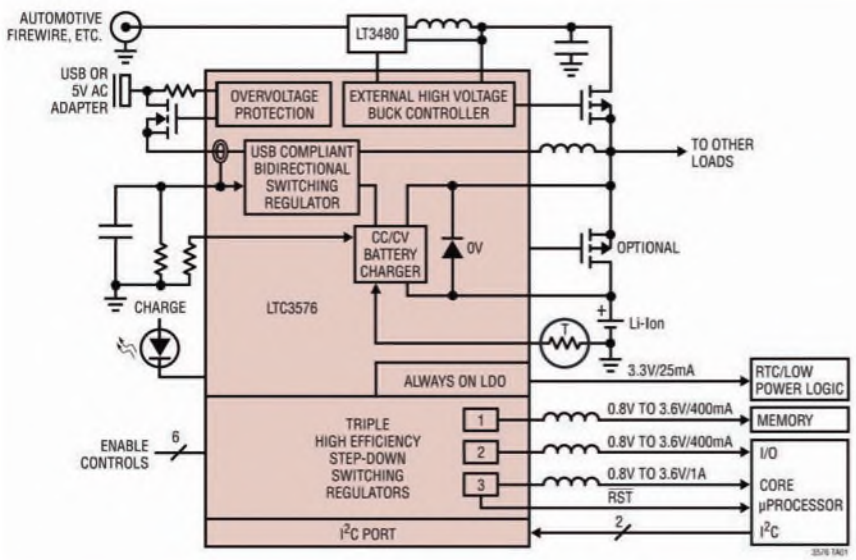


Figure 2: *LTC3576 simplified block diagram*

properly with sufficient copper trace routing, heat sinks, or well-designed input/output voltage and output current levels, can generate a lot of localised heat or "hot spots" on the PC board.

Alternatively, switching regulators provide a more efficient way to step down and convert voltages when the differential between input and output voltage is high and/or if the output current is high. This is commonplace in today's feature-rich devices with low-voltage microprocessors on board. So implementing switchmode power supplies for the majority of voltage rails is increasingly necessary.

Additionally, linear battery chargers may be another source of heat, depending on the input voltage to battery voltage differential and charging current. In principle, linear chargers act like a linear regulator in terms of power dissipation. So, LDOs combined with linear chargers on the same chip may present a real thermal issue to contend with.

GENERATING INTERMEDIATE VOLTAGE RAILS FROM A LITHIUM BATTERY

Many of today's modern feature-rich portable electronics still require voltage rails around +3.3V, to power I/O or an HDD, for example. LDOs alone are clearly not sufficient to generate these system voltages from a Li battery input, as they may only step voltages down. Even the usage of buck switching regulators may not be sufficient (bucks are no better than LDOs for dropout – and sometimes worse) depending on the input supply, i.e. if the rail is powered off a Lithium battery (which has a typical voltage range from 4.2V at full charge, down to ~ 3.0V when depleted).

Applications that take advantage of the entire Li battery range may require a buck-boost regulator, which can efficiently provide a fixed output voltage, regardless of the input being above, below, or equal to this output. This is also true for systems that have high pulsed current requirements – the buck or LDO can lose output regulation without a large input capacitor present to prevent droop on V_{IN}.

MANAGEMENT OF MULTIPLE INPUT POWER SOURCES

Managing power flow, while minimising heat generation in a portable handheld product, presents a significant design challenge. An increasing number of portable battery-powered products can be powered from low voltage sources such as a 5V wall adapter, a USB port or Li-Ion/Polymer battery, and also high-voltage sources such as automotive adapters and Firewire ports.

Autonomous management of the power flow between these input sources and the battery while efficiently providing power to the load presents significant technical obstacles. Traditionally, designers have performed this function discretely, using a handful of MOSFETs, op-amps and other components, but have faced difficult problems with hot plugging, excessive heat generation, large inrush currents and large voltage transients to the load, which can cause system reliability problems.

EFFICIENTLY EXTRACTING POWER FROM USB

USB technology has increased the convenience of electronic devices. It is convenient to be able to charge the device from this same USB port that performs the data transfer, eliminating the need for a separate wall adapter. However, there are power limitations (2.5W max) when the USB is used for charging the device's battery. USB-capable battery charging in many cases means more convenience to the user, but it poses the constraint of USB current limits (500mA max). Thus, a battery charger must efficiently extract power from the USB port without exceeding the thermal limitations of the end product.

Key challenges for the system designer include:

- Designing around unnecessary PMIC functions
- Minimising power dissipated as heat
- Maximising battery run-time
- Generating low and intermediate voltage rails
- Managing power flow between multiple input sources, the battery and the load
- Maximising current delivered from the USB port (2.5W available)
- Minimising solution footprint and profile.

SIMPLE SOLUTION

There is no longer the need to work around the performance deficiencies of the traditional "large PMIC". Linear Technology's PMICs with PowerPath management and other best-in-class integrated functional blocks solve these problems simply and easily. In fact, in many systems one such PMIC is sufficient to power the entire system. This is possible because Linear Technology has taken a different approach to its PMIC development, utilising a more selective integration level that offers a compact solution without any performance compromises.

A key feature of these PMICs is the so-called PowerPath control. This automatic load prioritisation offers the ability to autonomously and seamlessly manage

power flow between multiple input sources such as USB ports, wall adapters and the battery, all while preferentially providing power to the system load.

In a traditional battery-fed charging system, the user must wait until there is sufficient battery charge and voltage level to obtain system power. Conversely, PowerPath control allows the end product to operate immediately when plugged in, regardless of the battery's state of charge, commonly referred to as "instant-on" operation. PowerPath control circuits may be found in both linear and switching topologies. Benefits of the linear PowerPath topology include Bat-Track adaptive output control capability with an external high-voltage buck and improved thermal performance with power flowing to the system load.

Switchmode PowerPath technology preserves these advantages while improving power delivery efficiency to the load/system and to the battery. It eliminates the power lost in the linear battery charger element, especially critical when the battery voltage is low and/or input power is limited (i.e. USB), giving it excellent thermal properties.

A second big advantage is its ability to extract up to 700mA battery charge current from a standard USB port (~ 2.3W) when battery voltages are low. In **Table 1** is a summary and comparison of the three different USB charging system topologies.

INTEGRATED BUCK-BOOST AND BOOST REGULATOR CAPABILITY

Low voltage rails with moderate to high output current, for instance down to 0.8V to power uP cores, may be efficiently generated from synchronous buck regulators. However, many of today's modern feature-rich portable electronics still require an intermediate voltage rail of either +3V or +3.3V.

Integrating synchronous buck-boost switching capability into the PMIC allows 3.3V (for example) regulation across the entire Li-ion/Polymer input battery range (sometimes as wide as 2.7V to 4.2V), with high efficiency, resulting in increased operating margin. So, at 3.3V a buck-boost regulator can "ride through" battery voltage or load current transients that would cause a step-down buck to lose regulation.

In addition, synchronous boost regulators allow "step-up" conversion to rails above the Lithium battery voltage range with good efficiency > 80%. Further, high switching frequencies reduce the size of external components and stability with ceramic capacitors reduces output ripple.

LONGER BATTERY LIFE AND RUN TIMES

Accurately charging a Lithium Ion/Polymer battery to its final float voltage has a heavy influence on battery life. This is managed by selecting an appropriate battery-charging IC with tight float voltage accuracy and accurate termination algorithms, all of which maximise battery runtime while not over-charging the cell. Furthermore, low system standby (quiescent) current and high switching regulator conversion efficiencies via synchronous rectification allow small system current consumption, further increasing battery run-time. Burst Mode operation, for example, automatically reduces switching regulator quiescent current (Iq) at light loads to help reduce device current consumption.

THE LTC3586 PMIC

The LTC3586 PMIC integrates a switching PowerPath manager, a stand-alone battery charger, four high-efficiency synchronous switching regulators (1 buck-boost, 1 boost, and 2 buck regulators) and an always-on LDO, all in a low-profile 38-pin 4mm x 6mm QFN package (see **Figure 1**).

For fast charging, the LTC3586's switching input stage converts nearly all of the 2.5W available from the USB port to charging current, enabling up to 700mA from a 500mA limited USB supply or up to 1.5A when wall powered.

The LTC3586's buck-boost regulator can deliver up to 1A continuously and is ideal for efficiently regulating a 3.3V output over the full Lithium battery voltage range, down to 2.75V input. The LTC3586's two buck regulators feature 100% duty cycle operation and are capable of delivering output currents of 400mA each, with adjustable output voltages down to 0.8V. The boost regulator is capable of at least 800mA output current and is programmable up to a 5V output.

The LTC3586's internal low $R_{DS(ON)}$ switches enable switching buck and buck-boost efficiencies as high as 94%, maximising battery run-time. In addition, Burst Mode operation optimises efficiency at

Attribute	Battery-Fed	Linear PowerPath	Switching PowerPath
Size	Small	Moderate	Larger
Complexity	Simple	Moderate	More complex
Solution Cost	Low	Moderate	Higher
USB Charge Current	Limited to 500mA	Limited to 500mA	NOT limited to 500mA (~ 2.3W)
Autonomous Control of Input Power Sources	No	Yes	Yes
Instant-ON Operation	No	Yes	Yes
System Load Efficiency (Ibus<USB limit)	Poor (VBAT/VBUS)	Poor (VBAT/VBUS)	Excellent (>90%) Very Good (~ 90%)
System Load Efficiency (Ibus=USB limit)	Poor (VBAT/VBUS)	Poor (VBAT/VBUS)	Poor (VBAT/VBUS)Very Good (~ 90%)
Battery Charger Efficiency	Poor (VBAT/VBUS)	Poor (VBAT/VBUS)	Very Good (~ 90%)
Thermal Dissipation	High	Moderate	Low
Bat-Track Adaptive Output Control/Interface to HV Buck	No	Yes	Yes

Table 1: Comparison of USB battery charging system topologies

Power Management ICs with Li-Ion/Polymer Battery Chargers							
Part Number	PowerPath Topology™	Interface	Buck(s)	Buck-Boost	Boost	LDO	Package (mm²)
LTC3576	switching	I²C	1A, 400mA x 2	-	-	25mA	4x6 QFN-38
LTC3586	switching	-	400mA x 2	1A	0.8A	25mA	4x6 QFN-38
LTC3555/-1/-3	switching	I²C	1A, 400mA x 2	-	-	25mA	4x5 QFN-24
LTC3556	switching	I²C	400mA x 2	1A	-	25mA	4x5 QFN-28
LTC3567	switching	I²C	-	1A	-	25mA	4x4 QFN-24
LTC3566	switching	-	-	1A	-	25mA	4x4 QFN-24
LTC3577 *	linear	I²C	600mA, 400mA x 2	-	-	150mA x 2	4x7 QFN-44
LTC3455	linear	-	600mA , 400mA	-	-	controller	4x4 QFN-24
LTC3557/-1	linear	-	600mA, 400mA x 2	-	-	25mA	4x4 QFN-28
LTC3558	-	-	400mA	0.4A	-	-	3x3 QFN-20
LTC3559/-1	-	-	400mA x 2	-	-	-	3x3 QFN-16
* future product - contact LTC Marketing for information.							

Table 2: *Linear Technology's PMIC family*

light loads with a quiescent current of only 25uA for the buck-boost regulator and only 35uA for each buck regulator (< 1uA each in shutdown for all).

The high 2.25MHz switching frequency allows the use of tiny low-cost capacitors and inductors less than 1mm in height while achieving very low output voltage ripple. Furthermore, all regulators are stable with ceramic output capacitors enabling a small footprint without thermal problems.

THE LTC3576 PMIC WITH USB OTG SUPPORT

The LTC3576 features a bidirectional switching power manager with input overvoltage protection and USB On-The-Go (OTG) functionality, a stand-alone battery charger, three high efficiency synchronous buck regulators, an ideal diode, I²C control, plus an always-on LDO, all in a low-profile 38-pin 4mm x 6mm QFN package (see **Figure 2**).

The LTC3576's USB-compatible bidirectional switching regulator features programmable input current limits of 100mA and 500mA, as well as a 1A wall adapter input current limit. The IC can also take power from the battery to generate the 500mA at 5V needed for USB OTG applications, without any additional components, allowing the device to act as a host.

For fast charging, the LTC3576 converts nearly all of the 2.5W available from the USB port to charging current, enabling up to 700mA from a 500mA limited USB supply. Charging current may be as high as 1.5A from a wall adapter from a second external source. The IC provides an overvoltage protection (OVP) control circuit that prevents damage to its input from the accidental application of voltages as high as 66V. The OVP circuit can protect the USB port even when the IC is providing power for USB OTG.

The LTC3576 provides Bat-Track control of a companion Linear Technology high voltage switching regulator for efficient charging from high voltage inputs, while minimising heat dissipation and providing a seamless transition between USB and the higher voltage power source.

The LTC3576's three integrated synchronous buck regulators are ceramic capacitor stable, feature 100% duty cycle operation and are capable of delivering output currents of 1A/400mA/400mA, respectively, with adjustable output voltages down to 0.8V. The internal low $R_{DS(ON)}$ switches enable efficiencies as high as 94%, maximising battery run time. In addition, Burst Mode operation optimises efficiency at light loads with a quiescent current of only 20uA per regulator (< 1uA in shutdown).

All three of the step down switching regulators can have their voltage adjusted "on-the-fly" via the I2C interface for voltage margining or optimising the performance/power tradeoff in micro-processors. Finally, the high 2.25MHz switching frequency allows the use of tiny low-cost capacitors and inductors less than 1mm in height.

A MYRIAD OF END APPLICATIONS

The discussed PMIC family has been a great fit for consumer handheld USB-powered products such as personal media players (PMPs), personal navigation devices (PNDs), electronic book readers and smart phones. However, the addition of new functional blocks and higher voltage and power capability has allowed these new PMICs to penetrate into other market spaces. For example, industrial portables such as tablet and rugged PCs or portable data entry terminals benefit from high input voltage capability and over-voltage protection from line transients of industrial system bus voltages. Medical devices benefit from a variety of voltage rail combinations and low quiescent currents. Portable automotive diagnostic and personal navigation device (PND) units benefit from high-voltage input capability to effectively power the unit from high voltage sources such as automotive adapters, in addition to USB. Even military applications such as vision systems and battlefield condition sensor systems benefit from the PMIC's rugged design and high voltage capabilities.

Table 2 highlights some of Linear Technology's high performance PMICs, ranging from lower-level integrated battery-fed topology ICs to linear PowerPath based ICs, to more sophisticated and higher level integrated switchmode PowerPath based PMICs.

CHOICES

System designers now have new choices for their portable power needs. Instead of using discrete power IC components or traditional large PMICs, Linear Technology offers a new generation of compact PMICs that integrate key power management functions for a new level of performance and smaller, simpler solutions. This growing family of compact battery-fed, linear or switching PowerPath PMICs makes the product designer's job much easier.

The ICs feature the ability to extract more power from a USB port, seamlessly manage power flow between input sources, provide effective thermal management, increase efficiency via Bat-Track adaptive output control, provide low, intermediate and high voltage rails across the entire Lithium battery input range and simplify designs by utilising fewer and smaller external components.

Finally, these ICs also enable benefits for the product's end device as well, including USB charging and USB On-the-Go convenience, higher reliability, instantaneous system power with a dead battery, longer battery run-times and faster charge times.■

PEAK
electronic design ltd

Peak Electronic Design Limited
West Road House, West Road,
Buxton, Derbyshire, SK17 6HF

tel. 01298 70012 fax. 01298 70046
www.peakelec.co.uk sales@peakelec.co.uk

Handheld Test Gear - Cool, Smart.

Atlas DCA £55

Atlas DCA - Model DCA55
Semiconductor Analyser
Identifies type and pinout! Connect any way round.
Measures gain, junction characteristics and more.

Atlas ESR £85

Atlas ESR - Model ESR60
ESR and Capacitance Meter
Measures capacitance, ESR (in-circuit too!).
Automatic controlled capacitor discharge feature!

Atlas LCR £79

Atlas LCR - Model LCR40
Inductor, Capacitor, Resistor Analyser
Automatic part identification, automatic frequency selection and auto ranging!

Atlas SCR £99

Atlas SCR - Model SCR100
Triac and Thyristor Analyser
Connect any way round, auto lead identification.
Auto gate test current from 100uA to 100mA.

UK: Please add £1.00 p&p to your order. Prices include UK VAT.
Please see website for overseas pricing.

PLC WITH PIC16F648A MICROCONTROLLER PART 2

ASSOCIATE PROFESSOR **DR MURAT UZAM** FROM NIGDE UNIVERSITY IN TURKEY PRESENTS A SERIES OF ARTICLES ON A PROJECT THAT FOCUSES ON A MICROCONTROLLER-BASED PLC. THIS IS THE SECOND ARTICLE OF THE SERIES AND IT COVERS THE BASIC SOFTWARE STRUCTURE OF THE UZAM_PLC

The basic software of this programmable logic controller (PLC) called UZAM_PLC makes use of general purpose 8-bit registers of RAM data memory of PIC16F648A. For the sake of simplicity, we restrict ourselves to use only BANK 0, i.e. all macros, including the basic definitions explained here, to be defined by means of 8-bit registers of BANK 0.

The file "definitions.inc" (all the files explained here including "definitions.inc" can be downloaded from **http://host.nigde.edu.tr/muzam/**). It contains all of the basic macros and definitions necessary for UZAM_PLC. In this article we will explain the contents of this file. First of all, let's have a look at the file called "UZAM_plc_8i8o_1.asm" shown in **Figure 1**. It is well-known that the PLC's scan cycle includes the following: obtain the inputs, run the user program, update the outputs. This cycle repeats as long as the PLC runs.

Before getting into the endless PLC scan cycles, the initial conditions of the PLC are set up in the initialisation stage. These main steps can be seen from Figure 1, where "initialise" is a macro for setting up the initial conditions; "get_inputs" is a macro for getting the inputs; and "send_outputs" is a macro for updating the outputs. The "user PLC program" must be placed between "get_inputs" and "send_outputs". The endless PLC scan cycles are obtained by means of the label "scan" and the instruction "goto scan".

UZAM_PLC is fixed to run at 4MHz with PIC16F648A's internal oscillator. The watchdog timer is used to prevent user-program lock-ups. As will be explained later, the hardware timer TMR0 is utilised to obtain free-running reference timing signals.

```
;-------------------------------------------------------------;
;     Filename:   UZAM_plc_8i8o_1.asm                         ;
;     Date:       28 January 2008                             ;
;     Author:     Assoc. Prof. Dr. Murat UZAM                 ;
;     Company:    Niğde Üniversitesi                          ;
;                 Mühendislik-Mimarlık Fakültesi              ;
;                 Elektrik-Elektronik Mühendisliği Bölumu     ;
;                 Kampus, 51200, Niğde, TURKEY                ;
;                 http://host.nigde.edu.tr/muzam/             ;
;                 murat_uzam@nigde.edu.tr                     ;
;                 murat_uzam@hotmail.com                      ;
;                 Tel: ++ 90 388 225 22 82                    ;
;                 Fax: ++ 90 388 225 01 12                    ;
;-------------------------------------------------------------;
;    Notes:       This is the basic program                   ;
;                 for PIC16F648 microcontroller               ;
;                 based UZAM PLC with                         ;
;                 8 Inputs and 8 Outputs                      ;
;                 and 32 Memory Bits (Internal Relays)        ;
;-------------------------------------------------------------;
      list      p=16F648A           ;list directive to define processor
      #include <p16F648A.inc>       ;processor specific variable definitions
      #include <definitions.inc>    ;basic PLC definitions, macros, etc.
      __CONFIG _CP_OFF& _DATA_CP_OFF& _LVP_OFF& _BOREN_OFF& _MCLRE_OFF& _WDT_ON
& _PWRTE_ON& _INTOSC_OSC_NOCLKOUT

      org   0x00                ;Reset Vector
main
      initialize
scan
      get_inputs
;--------------- user program starts here -------------------------


;--------------- user program ends here ---------------------------
      send_outputs

      goto  scan
      end                       ;directive 'end of program'
```

Figure 1: *The view of the file "UZAM_plc_8i8o_1.asm"*

FILE DEFINITIONS

Next, let's consider the inside of the file "definitions.inc". The definition of 8-bit variables to be used for the basic software and their allocation in BANK 0 of RAM data memory are shown in **Figure 2a** and **2b** respectively. Although we can define as many inputs and outputs as we want, for the sake of simplicity we define four 8-bit input registers and four 8-bit output registers (Q0, Q1, Q2, Q3).

It is well-known that inputs taken from

It is also necessary to define and initialise all variables used within a PLC. Necessary functions are all described as PIC Assembly macros to be used in UZAM_PLC. The macros described in this article could be summarised as follows: "HC165" (for handling the inputs), "HC595" (for sending the outputs), "dbncr" (for debouncing the inputs), "initialise", "get_inputs", "send_outputs".

```
---------- VARIABLE DEFINITIONS -----------------
CBLOCK 0x20         ;Currently 4 Bytes are
bI0,bI1,bI2,bI3     ;reserved for 4 (bouncing)
endc                ;Input Registers (74HC165 ICs)
CBLOCK 0x24         ;Currently 4 Bytes are
I0,I1,I2,I3         ;reserved for 4 (debounced)
endc                ;Input Registers
CBLOCK 0x28         ;Currently 4 Bytes are
Q0,Q1,Q2,Q3         ;reserved for 4
endc                ;Output Registers (TPIC6B595 ICs)
CBLOCK 0x2C
M0,M1,M2,M3         ;4x8=32 Memory bits(Internal Relays)
endc
CBLOCK 0x30         ;Currently 8 Bytes are
DBNCR               ;reserved for 8
endc                ;Debouncer Registers
CBLOCK 0x38
DBNCRRED,Temp_1,Temp_2,Timer_2
endc
-------------------------------------------------
```

20h	bI0
21h	bI1
22h	bI2
23h	bI3
24h	I0
25h	I1
26h	I2
27h	I3
28h	Q0
29h	Q1
2Ah	Q2
2Bh	Q3
2Ch	M0
2Dh	M1
2Eh	M2
2Fh	M3
30h	DBNCR
31h	DBNCR+1
32h	DBNCR+2
33h	DBNCR+3
34h	DBNCR+4
35h	DBNCR+5
36h	DBNCR+6
37h	DBNCR+7
38h	Temp_1
39h	Temp_2
3Ah	Timer_2
3Bh	DBNCRRED

BANK 0

Figure 2: *(a) above – The definition of 8-bit variables to be used for the basic software,*
(b) below – Their allocation in BANK 0 of RAM data memory

```
;------------------- BANK macros --
BANK0 macro
      bcf STATUS,RP0
      bcf STATUS,RP1
      endm
BANK1 macro
      bsf STATUS,RP0
      bcf STATUS,RP1
      endm
BANK2 macro
      bcf STATUS,RP0
      bsf STATUS,RP1
      endm
BANK3 macro
      bsf STATUS,RP0
      bsf STATUS,RP1
      endm
;-----------------------------------
```

Figure 3: *BANK macros*

contacts always suffer from "contact bouncing". To circumvent this problem we will define a "debouncing" mechanism for the inputs and this will be explained later. In the "get_inputs" stage of the PLC scan cycle, the input signals are serially taken from the related 74HC/LS165 registers and stored in the registers. As a result, bI0, bI1, bI2 and bI3 will hold these bouncing input signals. After applying the "debouncing" mechanism to the registers bI0, bI1, bI2 and bI3, we obtain "debounced" input signals and they are stored in registers I0, I1, I2 and I3 respectively.

We don't have to use all of these registers. For example, if we use just the "main board", then we have 8 inputs and therefore we can just use bI0 and I0. Similarly, if we use the "main board" with an "I/O extension board", then we have 16 inputs and, therefore, we must use bI0, bI1 and I0, I1. Currently, for the sake of simplicity we restrict ourselves to the main board and, therefore, we need to use bI0 and I0.

In the "send_outputs" stage of the PLC scan cycle, the output information stored in the 8-bit registers Q0, Q1, Q2, Q3 are serially sent out to and stored in the related TPIC6B595 registers. This means that Q0, Q1, Q2, Q3 registers will hold output information and they will be copied into the TPIC6B595 registers at the end of each PLC scan cycle. We don't have use all of these output registers. For example, if we use just the "main board", then we have 8 outputs and, therefore, we can use just Q0.

Similarly, if we use the "main board" with an "I/O extension board", then we have 16 outputs and, so, we must use both Q0 and Q1. Currently, for the sake of simplicity we restrict ourselves to the main board and therefore we need to use only Q0. Four 8-bit registers, namely M0, M1, M2 and M3, are defined for obtaining 32 memory bits (internal relays, in PLC jargon).

To be used for the debouncer macro we define eight 8-bit registers (DBNCR, DBNCR+1, ..., DBNCR+7). In addition, the register DBNCRRED is also defined to be used for the debouncer macro. Temp_1 is a general temporary register declared to be used in the macros. Temp_2 is declared to be used especially for obtaining special memory bits as will be explained later. Timer_2 is defined for storing high byte of the free-running timing signals.

```
;--------- Definitions for 74HC165 --------
#define data_in   PORTB,0
#define clock_in  PORTB,6
#define shft_ld   PORTB,7
;------------------------------------------
;--------- Definitions for TPIC6B595 ------
#define data_out  PORTB,4
#define clock_out PORTB,3
#define latch_out PORTB,5
;------------------------------------------
;--------- LOGIC VALUES -------------------
#define LOGIC0    Temp_2,0
#define LOGIC1    Temp_2,1
;------------------------------------------
;--------- SPECIAL BITS -------------------
#define FRSTSCN   Temp_2,2
#define SCNOSC    Temp_2,3
;------------------------------------------
;---------- 8 INPUTS ----------------------
#define bI0.0  bI0,0    ;b:bouncing
#define bI0.1  bI0,1
#define bI0.2  bI0,2
#define bI0.3  bI0,3
#define bI0.4  bI0,4
#define bI0.5  bI0,5
#define bI0.6  bI0,6
#define bI0.7  bI0,7

#define I0.0  I0,0      ;I0 = debounced bI0
#define I0.1  I0,1
#define I0.2  I0,2
#define I0.3  I0,3
#define I0.4  I0,4
#define I0.5  I0,5
#define I0.6  I0,6
#define I0.7  I0,7
;------------------------------------------
;---------- 8 OUTPUTS ---------------------
#define Q0.0  Q0,0
#define Q0.1  Q0,1
#define Q0.2  Q0,2
#define Q0.3  Q0,3
#define Q0.4  Q0,4
#define Q0.5  Q0,5
#define Q0.6  Q0,6
#define Q0.7  Q0,7
;------------------------------------------
```

Figure 4: *Definitions of one-bit variables*

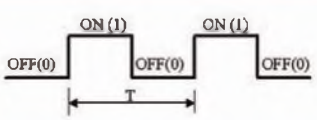


Figure 5: *Timing diagram of the free-running reference timing signals (T = 0.512, 1.024... 16777.216ms)*

The low byte of free-running timing signals is stored in TMR0 (recalled as Timer_1).

For accessing the RAM data memory easily, BANK macros are defined as shown in **Figure 3**. The definitions of one bit variables are depicted in **Figure 4**. The following definitions are self explanatory: 74HC165, TPIC6B595, 8 INPUTS, 8 OUTPUTS, 32 Memory Bits. Let us now have a look at the others.

```
;-------------------- Macro HC165 ---------------------------------------
HC165 macro num,var0        ;This macro can be used for 74HC/HCT/LS165
      local i=0,j=0         ;parallel to serial shift register ICs
      bcf   shft_ld         ;latch
      nop                   ;the inputs
      bsf   shft_ld         ;of all 74HC165's
        while j < num       ;carry on while j < num
          while i < 8       ;for each 74HC165, 8 times do the following
          rlf   var0+j,f    ;rotate the register "var0+j" one position left
          btfss data_in     ;if the data_in is set then skip
          bcf   var0+j,0    ;if the data_in is reset then reset "var0+j,0"
          btfsc data_in     ;if the data_in is reset then skip
          bsf   var0+j,0    ;if the data_in is set then set "var0+j,0"
          bcf   clock_in    ;generate
          nop               ;a clock_in
          bsf   clock_in    ;pulse
i += 1                      ;increment "i"
          endw          ;after 8 iterations end the while loop for "i"
i=0                     ;i=0            : get ready
j += 1                  ;increment "j"  : for a new 74HC165
        endw            ;after 'num' iterations end the while loop for "j"
      endm              ;end macro HC165
;------------------------------------------------------------------------
```

Figure 6: *The macro "HC165"*

OTHER VARIABLES

The variable "LOGIC0" is defined to hold logical "0" value throughout the PLC operation. At the initialisation stage it is deposited with this value. Similarly, the variable "LOGIC1" is defined to hold logical "1" value throughout the PLC operation. At the initialisation stage it is deposited with this value.

The special memory bit "FRSTSCN" is arranged to hold the value of "1" at the first PLC scan cycle only. In the other PLC scan cycles following the first one it is reset. The other special memory bit "SCNOSC" is arranged to work as a "scan oscillator". This means that in one PLC scan cycle this special bit will hold the value of "0", in the next one the value of "1", in the next one the value of "0" etc. This will keep on going for every PLC scan cycle. Let us now consider the 16 reference timing signals.

As seen later, TMR0 of PIC16F648A is set up to count the $^1/_4$ of 4MHz internal oscillator signal, i.e. 1MHz with a prescaler arranged to divide the signal to 256. As a result by means of TMR0 bits (also called Timer_1) we obtain eight free-running reference timing signals with the "T" timing periods starting from 0.512ms to 65.536ms. We'll see later that the register "Timer_2" is incremented on Timer_1 overflow. This also gives us (by means of Timer_2 bits) eight more free-running reference timing signals with the "T" timing periods starting from 131.072ms to 16777.216ms.

Timing diagram of the free-running reference timing signals is depicted in **Figure 5**. Note that the evaluation of TMR0 (Timer_1) is independent from PLC scan cycles, but Timer_2 is incremented within the "get_inputs" stage of PLC scan cycle on Timer_1 overflow. This is justified as long as the PLC scan cycle takes less than 65.536ms.

THE MACROS

The macro "HC165" is shown in **Figure 6**. The input signals are serially taken from the related 74HC/LS165 registers and stored in the registers such as bI0, bI1, bI2 and bI3 by means of this macro. The "num" defines the number of 74HC/LS165 registers to be considered. This means that with this macro we can obtain inputs from as many 74HC/LS165 registers as we wish.

However, as explained before, we restrict this number to be 4 at most for the sake of simplicity; "var0" is the beginning of the registers to which the state of inputs taken from 74HC/LS165 registers will be stored. This implies that there should be enough RAM locations reserved after "var0" and, also, there should be enough 74HC/LS165 registers to get the inputs from. There are some explanations within the macro to describe how it works.

As can be seen, this macro makes use of previously defined "data_in", "clock_in" and "sfht_ld" bits to obtain the input

```
;-------------------- Macro HC595 ----------------------------------------
HC595 macro num,var0     ;This macro can be used for 74HC/HCT/LS595
      local i=0,j=num-1 ;or TPIC6B595 serial to parallel shift register ICs
        while j >= 0     ;carry on while j >= 0
            while i < 8  ;for each TPIC6B595, 8 times do the following:
            rlf var0+j,f ;rotate the register "var0+j" one position left
            btfss  STATUS,C  ;if the Carry flag is set then skip
            bcf    data_out  ;if the Carry flag is reset then reset data_out
            btfsc  STATUS,C  ;if the Carry flag is reset then skip
            bsf    data_out  ;if the Carry flag is set then set data_out
            bsf    clock_out ;generate
            nop              ;a clock_out
            bcf    clock_out ;pulse
i += 1                       ;increment "i"
            endw             ;after 8 iterations end the while loop for "i"
      rlf   var0+j,f         ;rotate the register "var0+j" one position left
i=0                          ;i=0           : get ready
j-= 1                        ;decrement "j" : for a new TPIC6B595
      endw                ;after 'num' iterations end the while loop for "j"
      bsf   latch_out     ;Latch the serially shifted out data
      nop                 ;on all
      bcf   latch_out     ;TPIC6B595's
      endm                ;end macro HC595
;-------------------------------------------------------------------------
```

Figure 7: *The macro "HC595"*

```
;-------------------- macro: debouncer ------------------
dbncr macro num,regi,biti,t_reg,t_bit,tcnst_01,tcnst_10,rego,bito
      local   L1,L2,L3,L4
      btfsc   rego,bito
      goto    L4
      btfsc   regi,biti
      goto    L2
      clrf    DBNCR+num
      goto    L1
L4    btfss   regi,biti
      goto    L3
      clrf    DBNCR+num
      goto    L1
L3    btfss   t_reg,t_bit
      bsf     DBNCRRED,num
      btfss   t_reg,t_bit
      goto    L1
      btfss   DBNCRRED,num
      goto    L1
      bcf     DBNCRRED,num
      incf    DBNCR+num,f
      movf    DBNCR+num,w
      xorlw   tcnst_10
      skpnz
      bcf     rego,bito
      goto    L1
L2    btfss   t_reg,t_bit
      bsf     DBNCRRED,num
      btfss   t_reg,t_bit
      goto    L1
      btfss   DBNCRRED,num
      goto    L1
      bcf     DBNCRRED,num
      incf    DBNCR+num,f
      movf    DBNCR+num,w
      xorlw   tcnst_01
      skpnz
      bsf     rego,bito
L1
      endm

;-------------------------------------------------------
```

Figure 8: *The macro "dbncr"*

signals from 74HC/LS165 registers.

The macro "HC595" is shown in **Figure 7**. The output signals are stored in the 8-bit registers such as Q0, Q1, Q2 and Q3 in RAM locations, and serially sent out to and stored in the related TPIC6B595 registers by means of this macro. The "num" defines the number of TPIC6B595 registers to be used. This means that with this macro we can send output data serially to as many TPIC6B595 registers as we wish.

However, as explained before, we restrict this number to be 4 at most for the sake of simplicity; "var0" is the beginning of the 8-bit registers such as Q0 in RAM from which the state of outputs are taken and serially sent to TPIC6B595 registers. This implies that there should be enough RAM locations reserved after "var0" and, also, there should be enough TPIC6B595 registers to hold the outputs.

There are some explanations within the macro to describe how it works. As can be seen, this macro makes use of previously defined "data_out", "clock_out" and "latch_out" bits to send the output signals serially to TPIC6B595 registers.

The macro "dbncr" is shown in **Figure 8**. It can be used for debouncing eight independent buttons, switches, relay or contactor contacts etc. The timing diagram of one channel of this debouncer is provided in **Figure 9**. It can be seen that the output changes its state only after the input becomes stable and waits in the stable state for the predefined debouncing time "dt1" or "dt2". The debouncing is applied to both rising and falling edges of the input signal.

In this macro, each channel is intended for a "normally open contact" connected to the PIC by means of a pull-down resistor, as this is the case with UZAM_PLC. It can also be used without any problem for a "normally closed contact" connected to the PIC by means of a pull-up resistor.

The "debouncing times" such as 20ms, 50ms or 100ms can be selected as required depending on the application. It is possible to pick up different debouncing times for each channel. It is also possible to choose different debouncing times for rising and falling edges of the same input signal, if necessary. This gives a good deal of flexibility. This is simply done by chancing the related time constant "tcnst_01" or "tcnst_10" defining the debouncing time delay for each channel and for both edges within the assembly program.

Note that if the state-change-of-the-contact is shorter than the predefined "debouncing time", this will also be regarded as bouncing and it will not be taken into account. Therefore, no state-

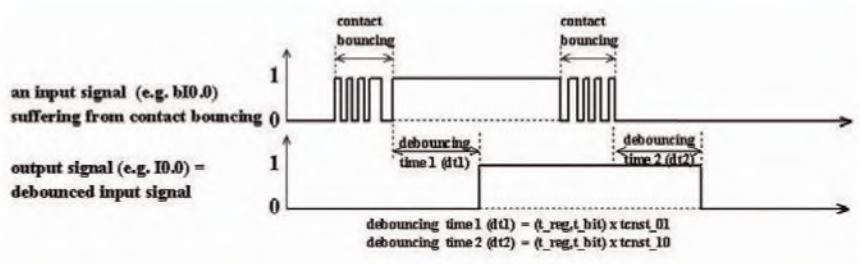


Figure 9: *Timing diagram of one channel of the debouncer*

change will be issued in this case. Each of the eight input channels of the debouncer may be used independently from other channels. The activity of one channel does not affect the other channels.

THE MACRO "DBNCR"

Let us now briefly consider how the macro "dbncr" works. First of all, one of the previously defined reference timing signals is chosen as "t_reg,t_bit" to be used within this macro. Then, we can set up both debouncing times dt1 and dt2 by means of time constants "tcnst_01" and "tcnst_10" as dt1 = (t_reg,t_bit) x tcnst_01 and dt2 = (t_reg,t_bit) x tcnst_10 respectively.

If the input signal (regi,biti) = 0 and the output signal (rego,bito) = 0 or the input signal (regi,biti) = 1 and the output signal (rego,bito) = 1, then the related counter "DBNCR+num" is loaded with "00h" and no state-change is issued. If the output signal (rego,bito) = 0 and the input signal (regi,biti) = 1, then with each "rising edge" of the reference timing signal "t_reg,t_bit" the related counter "DBNCR+num" is incremented by one. In this case, when the count value of "DBNCR+num" is equal to the number "tcnst_01", this means that the input signal is debounced properly and then state-change from 0 to 1 is issued for the output signal (rego,bito).

Similarly, if the output signal (rego,bito) = 1 and the input signal (regi,biti) = 0, then with each "rising edge" of the reference timing signal "t_reg,t_bit" the related counter "DBNCR+num" is incremented by one. In this case, when the count value of "DBNCR+num" is equal to the number "tcnst_10", this means that the input signal is debounced properly and then state-change from 1 to 0 is issued for the output signal (rego,bito). For this macro it is necessary to define the following 8-bit variables in RAM: Temp_1, and DBNCRRED. In addition, it is also necessary to define eight 8-bit variables in successive RAM locations, the first of which is to be defined as "DBNCR". It is not necessary to name the other seven variables. Each bit of the variable DBNCRRED is used to detect the "rising edge" of the reference timing signal "t_reg,t_bit" for the related channel.

```
;------------------- macro: initialize ----------------
initialize  macro
      BANK1               ;goto BANK1
      movlw b'00000111'   ;W <-- b'00000111' : Fosc/4 --> TMR0, PS=256
      movwf OPTION_REG    ;pull-up on PORTB, OPTION_REG <-- W
      movlw b'00000001'   ;PORTB is both input and output port
      movwf TRISB         ;TRISB <-- b'00000001'
      BANK0               ;goto BANK0
      clrf  PORTA         ;Clear PortA
      clrf  PORTB         ;Clear PortB
      clrf  bI0           ;Clear bI0
      clrf  bI1           ;Clear bI1
      clrf  bI2           ;Clear bI2
      clrf  bI3           ;Clear bI3
      clrf  I0            ;Clear I0
      clrf  I1            ;Clear I1
      clrf  I2            ;Clear I2
      clrf  I3            ;Clear I3
      clrf  Q0            ;Clear Q0
      clrf  Q1            ;Clear Q1
      clrf  Q2            ;Clear Q2
      clrf  Q3            ;Clear Q3
      clrf  M0            ;Clear M0
      clrf  M1            ;Clear M1
      clrf  M2            ;Clear M2
      clrf  M3            ;Clear M3
      clrf  DBNCR         ;Clear DBNCR
      clrf  DBNCR+1       ;Clear DBNCR+1
      clrf  DBNCR+2       ;Clear DBNCR+2
      clrf  DBNCR+3       ;Clear DBNCR+3
      clrf  DBNCR+4       ;Clear DBNCR+4
      clrf  DBNCR+5       ;Clear DBNCR+5
      clrf  DBNCR+6       ;Clear DBNCR+6
      clrf  DBNCR+7       ;Clear DBNCR+7
      clrf  DBNCRRED      ;Clear DBNCRRED
      clrf  Timer_1       ;Clear Timer_1
      clrf  Timer_2       ;Clear Timer_2
      clrf  Temp_1        ;Clear Temp_1
      movlw 06h           ;W <--- 06h
      movwf Temp_2        ;Temp_2 <--- W(06h)
      endm
;-------------------------------------------------------
```

Figure 10: *The macro "initialise"*

THE MACRO "INITIALISE"

The macro "initialise" is shown in **Figure 10**. There are mainly two tasks carried out within this macro. In the former, first TMR0 is set up as a free-running hardware timer with the $^1/_4$ of 4MHz internal oscillator signal, i.e. 1MHz, and with a prescaler arranged to divide the signal to 256. In addition, PORTB is initialised to make RB0 (data in) as input and the following as outputs: RB3 (clock out), RB4 (data out), RB5 (latch out), RB6 (clock in), RB7 (shift/load). In the latter, all utilised RAM registers are loaded with initial "safe values". In other words, all utilised RAM registers are cleared (loaded with 00h) except for Temp_2, which is loaded with 06h. As explained before, Temp_2 holds some special memory bits, therefore, the initial values of these special memory bits are put into Temp_2 within this macro. As a result, these special memory bits are

```
;---------------------- macro: get_inputs ----------------
get_inputs  macro
      local Nzero
      HC165 .1,bI0                        ;obtain the 8 inputs from input
      dbncr 0,bI0.0,T00,.40,.40,I0.0      ;register (74HC165) and
      dbncr 1,bI0.1,T00,.40,.40,I0.1      ;put them into bI0
      dbncr 2,bI0.2,T00,.40,.40,I0.2      ;register within PIC16F648A.
      dbncr 3,bI0.3,T00,.40,.40,I0.3      ;Then debounce all bits of
      dbncr 4,bI0.4,T00,.40,.40,I0.4      ;bI0.
      dbncr 5,bI0.5,T00,.40,.40,I0.5      ;The debounced input signals
      dbncr 6,bI0.6,T00,.40,.40,I0.6      ;are stored in the register
      dbncr 7,bI0.7,T00,.40,.40,I0.7      ;I0

      btfsc   Timer_1,7             ;
      bsf     Temp_2,4              ;Increment Timer_2 on Timer_1 overflow
      btfsc   Timer_1,7             ;
      goto    Nzero                 ;
      btfss   Temp_2,4              ;
      goto    Nzero                 ;
      incf    Timer_2,f             ;
      bcf     Temp_2,4              ;
Nzero
      endm
;--------------------------------------------------------
```

Figure 11: *The macro "get_inputs"*

```
;-------------------- macro: send_outputs --------------
send_outputs      macro
      local   L1,L2
      HC595 .1,Q0       ;take the 8 bits from Q0 register within PIC16F648A
                        ;and put them into output register Q0 (TPIC6B595)

      clrwdt            ;clear the watchdog timer

      bcf     FRSTSCN   ;reset the FRSTSCN bit

      btfss   SCNOSC    ;toggle
      goto    L2        ;the SCNOSC bit
      bcf     SCNOSC    ;after a program
      goto    L1        ;scan
L2    bsf     SCNOSC    ;
L1
      endm
;--------------------------------------------------------
```

Figure 12: *The macro "send_outputs"*

```
;---------------- user program starts here -------------------------
      movfw       I0
      movwf       Q0
;---------------- user program ends here ---------------------------
```

Figure 13: *A fraction of the first example program "UZAM_plc_8i8o_ex1.asm"*

```
;---------------- user program starts here -------------------------
      movfw Timer_2
      movwf Q0
;---------------- user program ends here ---------------------------
```

Figure 14: *A fraction of the second example program "UZAM_plc_8i8o_ex2.asm"*

loaded with the following initial values: LOGIC0 (Temp_2,0) = 0, LOGIC1 (Temp_2,1) = 1, FRSTSCN (Temp_2,2) = 1, SCNOSC (Temp_2,3) = 0.

THE MACRO "GET_INPUTS"

The macro "get_inputs" is shown in **Figure 11**. There are mainly three tasks carried out within this macro. In the first one, the macro "HC165" is called with the parameters ".1" and "bI0". This means that we will use only the "main board" and, therefore, the macro "HC165" is called with the parameter ".1". As explained before, the input information taken from the macro is rated as "bouncing" information and, therefore, this information is stored in "bI0" register. For example if we decide to use the "main board" connected to three of the "I/O extension board" then we must call the macro "HC165" as follows: "HC165 .4,bI0". This will take four 8-bit bouncing input information from the 74HC/LS165 ICs and will put them to the four successive registers starting with the register bI0.

In the second task within this macro, each bit of bI0, *i* (*i* = 0, 1... 7) is debounced by the macro "dbncr" and each debounced input signal is stored in the related bit I0, *i* (*i* = 0, 1... 7). In general, 20ms time delay is enough for debouncing both rising and falling edges of an input signal. Therefore, to achieve these time delays, the reference timing signal, obtained from Timer_1, is chosen as T00 (0.512ms period) and both "tcnst_01" and "tcnst_10" are chosen to be "40". Then we obtain the following: dt1 = T00 x tcnst_01 = (0.512ms) x 40 = 20.48ms, dt2 = T00 x tcnst_10 = (0.512ms) x 40 = 20.48ms.

Note that in this series of articles for the sake of simplicity we use just 8 inputs and 8 outputs. If we want to add more inputs and to debounce these inputs, then we must organise the macro "dbncr" and locate necessary number of registers within the RAM.

The last task is about incrementing the Timer_2 on overflow of Timer_1. In this task, "Timer_2" is incremented by one when the falling edge of the bit "Timer_1,7" is detected. In order to detect the falling edge of the bit "Timer_1,7", "Temp_2,4" bit is utilised.

THE MACRO "GET_OUTPUTS"

The macro "send_outputs" is shown in **Figure 12**. There are mainly four tasks carried out within this macro. In the first one, the macro "HC595" is called with the parameters ".1" and "Q0". This means that we will use only the "main board" and, therefore, the macro "HC595" is called with the parameter ".1".

As explained before, the output information is taken from the register Q0 and this macro sends the bits of Q0 serially to TPIC6B595 register. For example, if we decide to use the "main board" connected to three of the "I/O extension board" then we must call the macro "HC595" as follows: "HC595 .4,Q0". Then, the macro "HC595" will take four 8-bit output information stored in Q3, Q2, Q1 and Q0 and send them serially to the four TPIC6B595 register ICs respectively.

In the second task within this macro, the watchdog timer is cleared. In the third task, the "FRSTSCN" special memory bit is reset. As the final task, within this macro the "SCNOSC" special memory bit is toggled after a program scan, i.e. when it is "1" it is reset, when it is "0" it is set.

EXAMPLES

Up to now we have seen the hardware and basic software necessary for UZAM_PLC. It is now time to consider a few examples. Before you can run the two simple examples considered here, you are expected to construct your own UZAM_PLC hardware by using the necessary PCB files and producing PCBs with its components.

For the first example, include the user program shown in **Figure 13** within the "UZAM_PLC_8i8o_1.asm" and then save it as "UZAM_PLC_8i8o_ex1.asm". The next thing to do is to open it by MPLAB IDE and to compile it. After that, by using the PIC programmer software take the compiled file "UZAM_PLC_8i8o_ex1.hex" and by your PIC programmer hardware, send it to the program memory of PIC16F648A microcontroller within the UZAM_PLC.

After loading the "UZAM_PLC_8i8o_ex1.hex", switch the 4PDT in "RUN" and the power switch in "ON" position. Now, you are ready to test the first example program. You can see that all the inputs are transferred to the respected outputs. That is to say that if I0.0 = 0 then Q0.0 = 0 and, similarly, if I0.0 = 1 then Q0.0 = 1. This applies to all 8 inputs and 8 outputs.

For the second example, please include the user program shown in **Figure 14** within the "UZAM_PLC_8i8o_1.asm" and then save it as "UZAM_PLC_8i8o_ex2.asm". Next open it by MPLAB IDE and compile it. After that by using the PIC programmer software take the compiled file "UZAM_PLC_8i8o_ex2.hex" and by your PIC programmer hardware send it to the program memory of PIC16F648A microcontroller within the UZAM_PLC.

After loading the "UZAM_PLC_8i8o_ex2.hex", switch the 4PDT in "RUN" and the power switch in "ON" position. Now, you are ready to test the second example program. In this case the contents of "Timer_2" register are transferred to 8 outputs.

Of course, in these two examples the user programs include only PIC Assembly instructions, but we will start using our own macro-based PLC instructions in the next article. ■

ELECTRONICA IS THE LARGEST ELECTRONICS INDUSTRY EVENT, TAKING PLACE EVERY TWO YEARS IN MUNICH, GERMANY. THIS YEAR IT RUNS FROM 11TH TO 14TH OF NOVEMBER, AT MESSE MUNCHEN, GERMANY

Wide Range of Frequency Control Products

Euroquartz is exhibiting its widest ever range of products at Electronica 2008. Exhibiting alongside its German distributor, WDI, Euroquartz will show the new range of XpressO configurable oscillators and voltage controlled crystal oscillators (VCXO) from Fox Electronics, high temperature and high shock surface-mount oscillators from Statek and a new surface mount temperature-compensated crystal oscillator (TCXO) from Greenray Industries.

The company is also exhibiting examples of products from its wide portfolio of frequency control devices including the latest SST (spread spectrum technology) oscillators offering low EMI emissions.

XpressO crystal oscillators and VCXOs from Fox Electronics represent a breakthrough in configurable frequency control solutions, featuring proprietary ASICs designed and developed with a key focus on noise reduction techniques.

New Statek CXOMHT surface mount oscillators are high temperature versions of the CXOM range and offer high stability and fast start up.

The T1220 is a new surface mount TCXO from Greenray Industries that offers temperature stabilities more usually associated with oven controlled temperature compensated (OCXO) devices.

Euroquartz's EQHM range is a cost-effective solution for clock oscillator generated EMI problems without the need for expensive and time consuming PCB redesign phases.

www.euroquartz.co.uk

Electronica Location B6.156

Industrial, Railway and Military Connectors Display

PEI-Genesis will be featuring a comprehensive line-up of leading manufacturers' industrial, railway and military connectors, all of which are available with the company's 48-hour connector assembly service.

For industrial applications, PEI-Genesis will be showing the Amphenol 62IP range of miniature bayonet-lock connectors, which offer IP67 environmental protection and a moulded thermoplastic construction with a smooth, low-lustre black finish that requires no additional plating. Neoprene rubber is used for the insert material and the connectors are supplied with gold-plated solder-bucket contacts.

Demonstrating PEI's rail-industry capability will be ITT's versatile CIR series multi-pin connectors, which can be configured with a wide variety of inserts and contacts to provide electrical, fibre-optic or pneumatic interconnections. Designed specifically for the hostile environment of railway applications, the VEAM CIR connectors feature a positive-lock/quick-disconnect bayonet coupling mechanism and achieve high shock and vibration resistance without the need for lock wires.

The display of military connectors on the PEI-Genesis stand will be spearheaded by ITT's VEAM PT (Pattern 105) range of military audio connectors, which are widely used in fighting vehicles and ground-based military communications equipment such as the MoD's Clansman and Bowman radio systems.

www.peigenesis.co.uk

Electronica Location B3.133

New Commercial Digital Media Player

Digital View's new ViewStream 400 is a digital video player designed for use with High Definition (HD) LCD and Plasma displays for various environments. Applications include, but are not limited to, point-of-purchase (POP) messaging and promotions, product demonstration videos, digital menu boards, customer information kiosks, employee training role playing and museum information displays.

The ViewStream 400 is designed to be used as a standalone player without network connectivity. Content is updated via the USB port and a USB memory stick. Standard configuration will allow the ViewStream 400 to store more than 50 hours of content via a SATA hard drive. Content scheduling and play list management is handled using DV Studio Plus, which is supplied free of charge.

Supported media formats include, MPEG-1, MPEG-2 and MPEG-4 video in standard definition and MPEG-2 in high-definition resolution. MP3 audio and JPEG file formats are also supported.

The ViewStream 400 is compact, measuring 180mm x 235mm x 60mm, and weighs only 1.2kg. Video output is through the ARGB port. Audio Output is via a 3.5mm stereo audio jack.

An OEM version of the ViewStream 400 is also available.

www.digitalview.com

Electronica Location A3.120

New Range of Vandal-Proof Keypads

Lorlin Electronics will be previewing their new range of vandal-proof keypads at Electronica 2008. The new KP range offers 1, 2, 3, 4, 12 and 16 button versions for applications requiring a simple push button control to complex alpha numeric security entry systems. The keypads are available in black or chrome finishes to meet system design requirements and may be LED illuminated with a wide range of colour options. The weather and dust resistant IP rated keypads may be front or rear mounted and the keys feature an anti-pull design for improved security.

Lorlin's vandal-proof metal keypads are ideal for security switching or access control in public and industrial environments, environmental controls and service access.

Also on display will be Lorlin's wide range of spring return key switches commonly used for security gates and shutters for commercial and industrial premises. Single and double impulsion versions are available to suit individual requirements.

On show also will be a wide range IP67 rated key switches for secure access to electrical control boxed and panels, telecoms street furniture, electrical machinery and industrial equipment, as well as some of Lorlin's customisable push-rotate potentiometers.

www.lorlinelectronics.com

Electronica Location B4.643

Extended Intelligent Colour Display Platform

Anders Electronics is announcing an extension to its UMR (User Machine Relationship) family of intelligent colour display platforms. The latest platform will significantly extend the range of functionality and price points for designers and integrators looking to incorporate colour TFT-LCD and enhanced features into embedded applications.

The Anders UMR family of intelligent colour display platforms has been developed to help designers and system integrators deliver the ultimate user experience in a wide variety of display-based applications. The range currently includes the UMR-X10-70 and UMR-X10-35, both of which will also be on display at Electronica 2008.

UMR display platforms easily 'plug' into developers' application hardware, as a ready-to-use, highly optimised embedded display interface on which to run a dedicated Graphical User Interface (GUI) that brings the product to life for the end user. Through adopting a UMR display platform, developers can avoid the common integration challenges that they must usually solve independently and can free up resources to focus on their core domain expertise and specific application development. The end result is a shorter time to market, a more cost-effective solution and an easy-to-use product.

www.anders.co.uk

Electronica Location A3.431

CleanTech 100 Award for Nanotecture

Nanotecture, the energy technology company, has been named as one of the CleanTech 100 companies by The Guardian/Library House.

The CleanTech 100 is an award which aims to highlight a group of the most promising private companies in Europe focusing on clean technology, with – companies selected on the basis of their potential for future growth and – beneficial environmental impact. With climate change and energy use nudging the top of political and commercial agendas, these are companies that have a stake in how the world develops, states CleanTech 100 literature.

Nanotecture was awarded the CleanTech 100 status in the Energy Storage sector for its ground-breaking work to produce next generation energy storage products utilising Nanotecture's unique nanoporous materials.

Bill Campbell, Nanotecture's CEO said: "This award is strong endorsement of both the company's technology and its potential contribution to clean, highly efficient energy storage."

Nanotecture Ltd is a UK-based nanomaterials company, engaged in product development of innovative energy storage products for the automotive and portable electronics industries.

www.nanotecture.co.uk

Electronica Location B2.133

The UK group presentation at Electronica is managed by Tradefair on behalf of Intellect, the UK trade association for the IT, telecoms and electronics industries; and supported by UK Trade & Investment, the government body responsible for promoting exports from and inward investment into the UK. Tradefair assists more than 700 firms every year at over 40 trade shows across the world. The company believes it offers "more than just exhibition space and logistics – helping clients not only plan their globalisation but also integrate real-world and virtual strategies and get the best out of limited budgets".

PCB-POOL®.COM

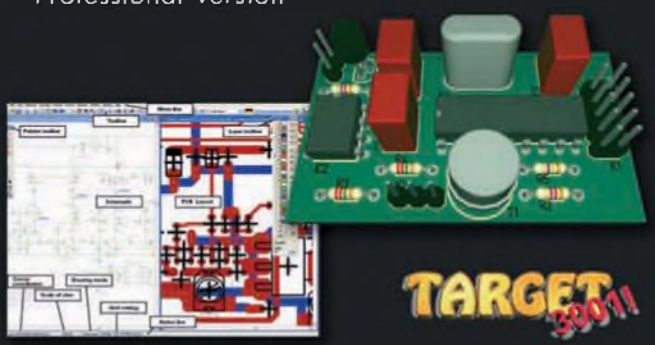
Low Cost PCB Manufacturing Service

- Prototypes manufactured from original designs
- Professional quality for a discount price
- The PCB-POOL service supplies professional quality Prototypes to the entire electronics industry (including students & hobbyists)

Simply send us your files & receive your prototypes in a few days!!!

Download our FREE PCB Layout Software!

- Schematic Capture
- PCB Layout
- Auto Router & Auto Placer
- Complete Component Library
- Professional Version



www.free-pcb-software.com

WATCH UR PCB®

View your PCB as it gets manufactured!

We send HD images at each protuction stage so you can track its progress!!

- *Drilling*
- *Exposure*
- *Tin Stripping*
- *UV curing*
- *Hot air levelling (HAL)*

www.pcb-pool.com

Email: sales@pcb-pool.com Free Phone UK: 0800 389 8560

Simply send your files & order ONLINE **WWW.PCB-POOL.COM**

p-cad TARGET Protel EDWin orcad GraphiCode PRITEL Electronics Easy-PC Sprint Layout

Beta LAYOUT

CIRCUIT PROVIDING A SAFE SHUTDOWN FOR A BACK-TO-BACK PWM CONVERTER

In a variable speed wind energy system, two back-to-back PWM converters are usually connected between the induction generator (IG) and the three-phase grid, as shown in **Figure 1** (right). In this configuration, the power flow of CONVERTER 2 is controlled in order to keep the dc-link voltage constant, while CONVERTER 1 is set to meet the magnetisation demand of the IG and the fixed reference speed.

During the disconnection of the grid, or if there is a fault in the power system, both converters are disconnected. Should this occur, the energy stored in the stator of the IG cannot be supplied to the grid and the current can only flow through the rectifier diodes of CONVERTER 1 to the dc-link capacitor, making the voltage rise to a dangerous level. To avoid this problem, a shutdown block that discharges the dc-link capacitor is required.

The circuit in Figure 1 implements this shutdown with few components, with a command signal generated by the control card which is isolated from the power system. Some of these circuits are implemented using a thyristor as a switching element. By using a thyristor the activation can only be controlled in the case of a shutdown, but this would not be so in the case of de-activation. The proposed shutdown block uses an IGBT to control both the activation (shutdown mode) and de-activation (normal mode).

In normal mode, the command is set, Q_1 is on and the optocoupler turns off the IGBT (Z_1). In shutdown mode, a low logic level is applied to the command, Q_1 is switched off, the optocoupler output goes to a high-impedance state and the pull-up resistor R_3 turns on the IGBT by pulling the gate high.

The R_{ON} of the IGBT, together with the R_{damp} resistor, acts as a voltage divider at the collector of the IGBT (V_{CE}). This voltage V_{CE} is used to charge the equivalent gate-capacitor of the IGBT through R_3. Once the steady-state is reached and the gate-capacitor is charged, the current through R_3 goes to zero and V_{GE} equals to V_{CE}.

The voltage V_{CE} is designed to be higher than the IGBT gate threshold voltage and, thus, to keep the IGBT activated. This imposes a maximum value of R_{damp} for a given value of the dc-link voltage and the R_{ON} of the IGBT. Moreover, the R_{damp} value fixes the discharge time constant of the dc-link capacitor.

In this particular case, the dc-link voltage is regulated to 300V, the dc-link capacitor value is 5mF and the R_{damp} resistor is selected of 1kΩ. This provides an initial collector current of approximately 0.3A, which gives a R_{ON} of tens of ohms for the selected IGBT (IRG4PC50KD), which increases as the dc-link capacitor discharges. If the R_{ON} of the selected IGBT is too big and/or a fast discharge of the dc-link capacitor is needed (small R_{damp}), the resultant gate-voltage can overcome the maximum rating. For this reason, a zener diode (D_1) of 15V has been included at the gate of the IGBT.

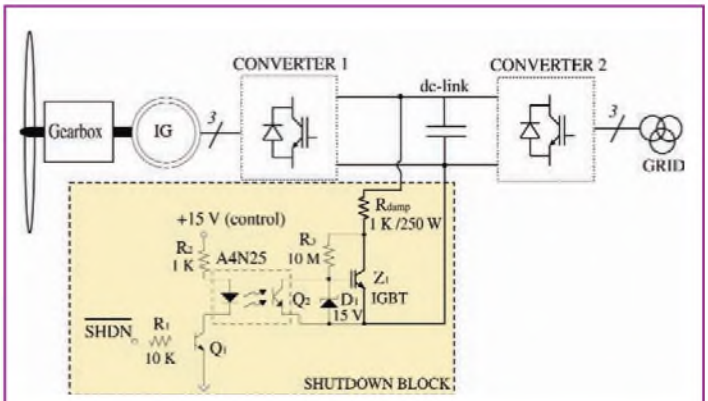


Figure 1: *This circuit provides safe shutdown when grid disconnection is required, or if there is a fault in the power system*

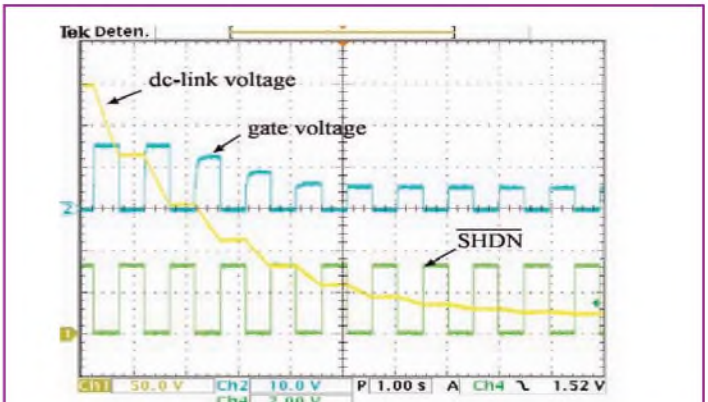


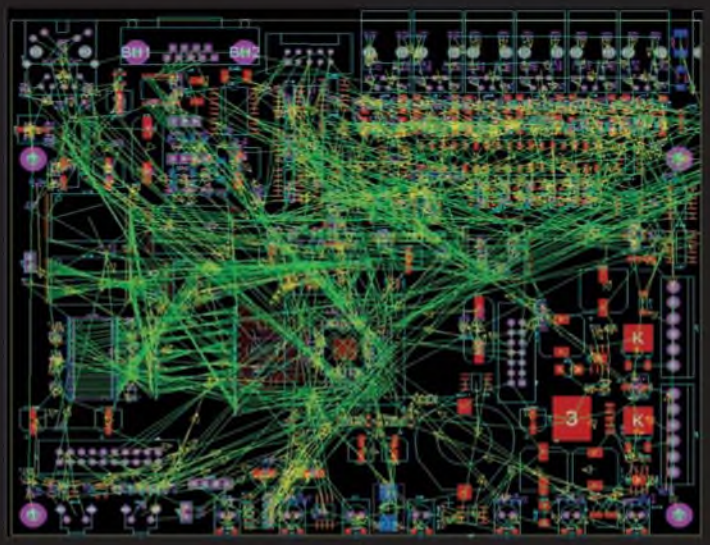
Figure 2: *These curves show the discharge voltage of the dc-link capacitor and the gate-voltage of the IGBT when a sequence of pulses is applied in the command*

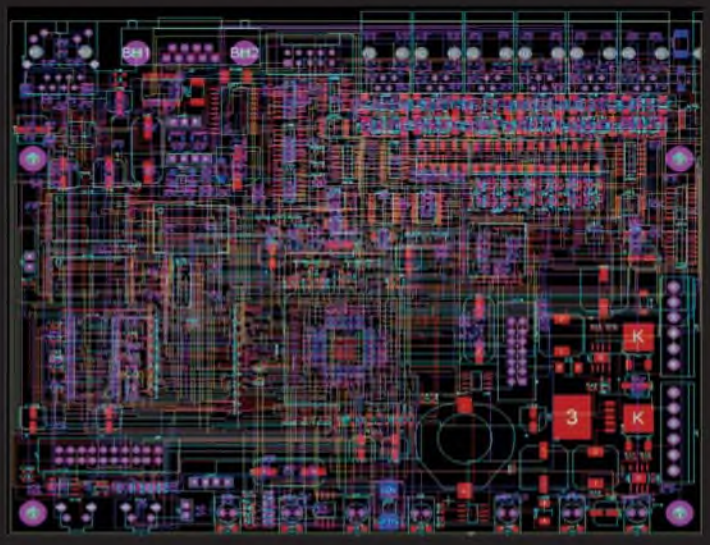
A value of 10MΩ has been selected for R_3, so that in normal mode (Q_2 on and Z_1 off) the dc-link capacitor has in parallel a very high resistor. On the other hand, in shutdown mode, the R_3 value, together with the equivalent gate-emitter capacitor of the IGBT, gives a slow switching-on but adequate for this application.

Figure 2 shows the experimental waveforms when successive changes are applied between normal mode and shutdown mode.

J. Castelló, R. García-Gil and **J. M. Espí**
University of Valencia
Spain

Our new autorouter will turn this... into this...



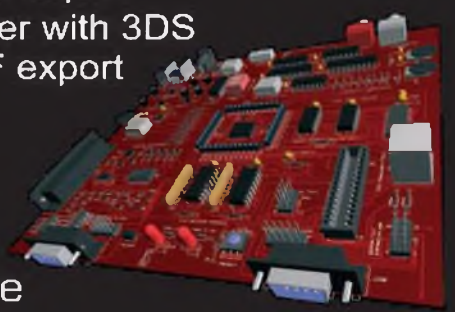


in less than 5 minutes!

All levels of the **Proteus Design Suite** now include a world class fully integrated shape based autorouter at **no additional cost**.

The **Proteus Design Suite** also incorporates:

- Professional schematic capture
- Publication quality schematics
- Fully configurable bill of materials
- Large component libraries for both simulation and PCB layout
- Mixed mode SPICE circuit simulation
- Co-simulation of PIC, AVR, 8051 and ARM7 microcontroller firmware
- Automatic component placement and gateswap optimization
- Highly configurable design rules
- Interactive design rule checking
- Polygonal and split power planes
- RS274X, Excellon and ODB++ database export
- 3D Viewer with 3DS and DXF export



Prices start from **just £150*** - visit our website for full details or to download a free demo.

labcenter Electronics

www.labcenter.com

20 Years

Labcenter Electronics Ltd. 53-55 Main Street, Grassington, North Yorks. BD23 5AA.
Registered in England 4692454 Tel: +44 (0)1756 753440, Email: info@labcenter.com

*exc. VAT & delivery

TIP: CMRR NOT CREATED EQUAL FOR ALL INAS

By Bonnie C. Baker, Senior Applications Engineer, Texas Instruments

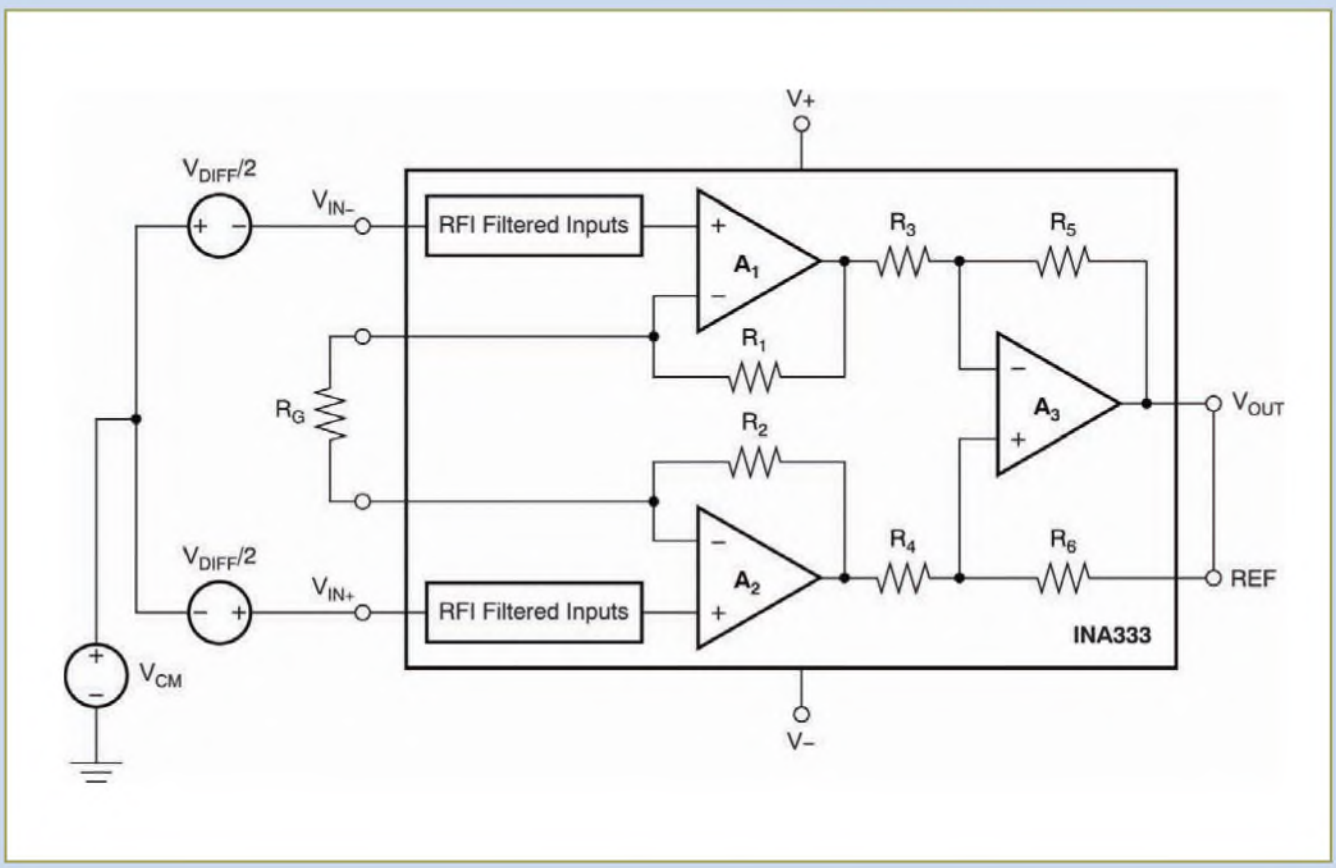


Figure 1: *Classical 3-operational amplifier style instrumentation amplifier*

DOES CMRR CHANGE WITH GAIN?

With each type of INA, is the common mode rejection ratio (CMRR) independent of gain? CMRR compares a change in common-mode input voltage to a change in system offset (decibels):

$$CMRR = 20 \times \log_{10} \frac{\Delta V_{CM}}{\Delta V_{OFFSET}} \qquad (1)$$

Manufacturers usually specify CMRR with an INA gain of one. This provides a good point for comparison from INA-to-INA. Don't assume CMRR is independent of gain. While CMRR in **Figure 1** is independent of gain, the CMRR in **Figure 2** is dependent on gain.

NO SHORT ANSWER

Consider the INA design in Figure 1 as it lends itself to a more straightforward analysis. With this circuit the two input signals see the high-impedance, non-inverting inputs of the amplifiers (A_1 and A_2). The first stage also gains the two incoming signals. Adjust the gain with the gain resistor, R_G. Following the first stage of this circuit is a difference amplifier (A_3). This portion of the circuit rejects the common-mode voltage of the two input signals, as well as subtracts them.

The majority of the common-mode error for this type of topology at lower gains comes from a resistor mismatch in the back-end, difference-amplifier. Any mismatch between the ratios of R_3:R_4 to R_5:R_6 will generate a common-mode rejection error. For instance, let's assume the CMRR of the device in Figure 1 is 80dB. If a one-volt, common-mode input (V_{CM}) change occurs, the output voltage changes by 100μV (per **Equation 1**). If you put the INA333 in a gain of 10V/V (R_G = 11.11kΩ, R_1R_2 = 50kΩ), the difference-amplifier resistors still contribute the same fixed error and produce an output error of 100μV.

If you refer this error to the input of the device, the change is equal to the output change divided by the gain or 10µV. Since the

CMRR specification is input-referred, the CMRR of this circuit in a gain of 10V/V is 100dB.

This theory works until the common-mode rejection of the front gain stage begins to dominate the system CMRR. For the INA333, at a gain of 100V/V the CMRR is 106dB, versus 120dB. This is because at higher gains, the mismatch of the difference-amplifier resistors (A_3) no longer dominates the error term. The error term becomes more a function of the CMRR of the individual front-end op-amps (A_1 and A_2).

The INA configuration in Figure 2 has a different CMRR behaviour. The gain of this circuit is equal to:

$$GAIN = (1 + \frac{R_F}{R_{IN}}) + (1 + \frac{R_F}{R_{IN}})(\frac{R_2}{R_1}) \qquad (2)$$

By following the series path of the input signal, you can see that the gain is set with the back-end amplifier (A_3). With this configuration, the change in offset of A_1 and A_2 will be gained by $(1+R_F/R_{IN})$ and summed to the offset change of A_3. This combined offset voltage from A_1, A_2 and A_3 scales directly to the output by $[1+ (R_2/R_1)]$. Regardless of the gain set by R_1 and R_2, the resistor mismatch around A_1 dominates the common-mode error.

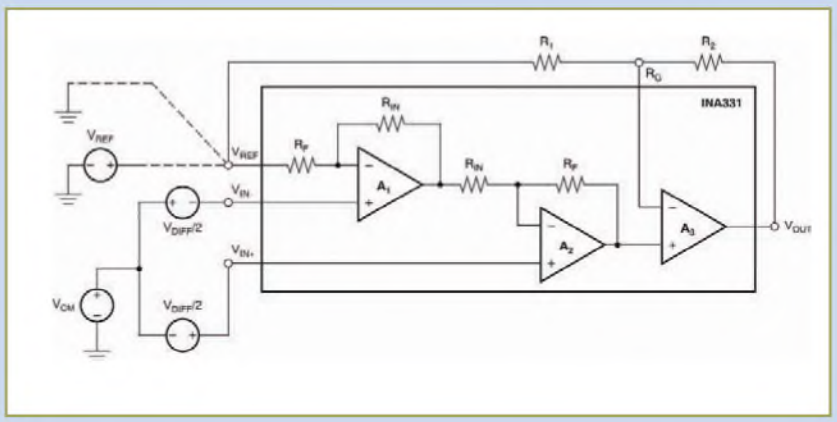


***Figure 2:** Baseband PR-ASK pulses at 64kbps*

For instance, let's say we configure the INA in Figure 2 in a gain of five (i.e. R_1 = open; R_2 = short) and we apply a 1V common-mode (ΔV_{CM}) change at inputs of A_1 and A_2. If this one volt common-mode input change creates a change of 500μV at V_{OUT}, the corresponding referred to the input offset change is 100μV. This is equivalent to a CMRR of 80dB.

If we increase the gain, the offset scales linearly to the output. Dividing the output by gain to obtain the input-referred offset does not change CMRR.

[Special thanks to Matthew Hann for his INA insights]

electronics growth
the way forward for electronics

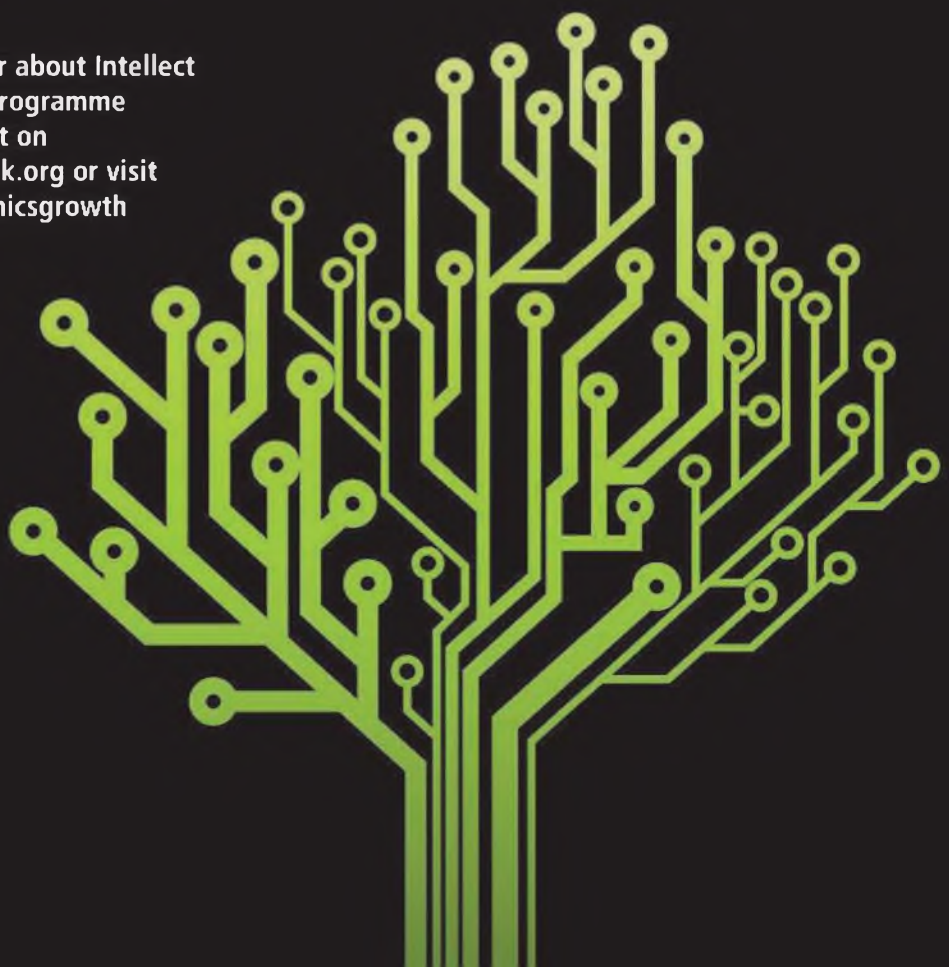
intellect
REPRESENTING THE UK TECHNOLOGY INDUSTRY

Intellect is the UK trade association for the IT, telecoms and electronics industries. Together these sectors make up 10% of UK GDP and 15% of UK exports. Our 800 members, from SMEs to large international corporations, account for over 80% of their markets.

We are here to help the UK electronics sector and supply chain to be as successful as they can be. We provide a powerful, unified voice for the sector to government. Our members are able to benchmark themselves against, and network with, major competitors and gain access to a wide range of markets. Provision of market key performance indicators is major focus for our programme.

As part of our efforts to promote and develop the UK electronics sector, we will be leading a delegation of British companies to electronica, the leading trade fair for the electronics industry, which takes place in Munich, between 11-14 November 2008. Visit Intellect on stand A5.175/2.

For more information on the delegation or about Intellect in general, please contact Henry Parker, programme manager - technology markets, at Intellect on 020 7331 2000, E henry.parker@intellectuk.org or visit our website, www.intellectuk.org/electronicsgrowth



COM Express Family Module Based On Intel Atom Processor N270

German-based congatec AG has enhanced its highly successful COM Express product family with the unveiling of the economically priced conga CA945 module. The new module features the Intel Atom processor N270 and the full-featured Mobile Intel 945GSE Express chipset in conjunction with the Intel I/O Controller Hub 7-M.

The complete design of this compact (95x95mm) COM Express module delivers excellent performance-per-watt at optimised price levels. The total thermal design power (TDP) of the processor/chipset combination is only 8 Watts, making applications that typically require less than 5 Watts ideal for this module. Combining this low power consumption with ACPI 3.0 battery management also provides the ability to create fully-featured mobile embedded applications.

The conga-CA945 supports three PCI Express Lanes, eight USB 2.0 ports, two serial ATA, two Express Cards, one IDE Interface and Intel High Definition Audio. Additionally, it features a 32-bit PCI bus, multi-master IÇC bus, LPC bus, fan control and Gigabit Ethernet. A DDR2 SODIMM socket allows for flexible memory configuration up to 2 GBytes in size.

The conga-CA945 is equipped with 512 kByte L2 cache. It operates at 1.6GHz clock speed and utilises a 533MHz front-side bus.

www.congatec.com

Smallest GPS Antenna Around

Alpha Micro Components announced that it has added Taoglas's smallest ever GPS Patch Antenna to its portfolio of embedded technologies. The new AP10 antenna patch, designed for use in smartphones, PDAs, personal tracking, navigation devices and mobiles phones, is one of the most compactly designed GPS receivers around.

Originally, developed for use in a touch-screen Smartphone device, this compact GPS antennae needed to be small, efficient and specifically tuned to the embedded GPS receiver, enabling location-based services and navigation capabilities to be added to the handset. Demand for such functionality in similar handsets is now rising, with requirement for all components including the antenna to be as small as possible, to sit comfortably within ever shrinking devices. In response, Taoglas has designed this miniature antenna and further ensured compatibility with all GPS receivers on the market by making the patch available in two formats: high-gain 2-stage LNA (Low Noise Amplifier) and low-gain 1-stage LNA.

The GPS patch antenna is available with a cable and connector which can be used for direct connection to a module or an onboard connector. Users requiring on-board integration have the chance to opt for the Surface Mountable (SMT) format.

www.alphamicro.net

Naked Z-Foil Resistor Virtually Eliminates Distortion in Audio Applications

Charcroft announces the immediate availability of a new, naked ultra-high-precision resistor for high-end audio, multimedia and broadcast applications. Based on Vishay's Bulk Metal Z Foil resistor technology, the Charcroft CAR resistor is supplied with a protective coating, rather than moulding or encapsulation, to deliver virtually distortion-free signal processing for the highest level of perceived sound clarity.

The resistors are built on the performance achieved by the previous generation of foil resistors to establish a new benchmark for clarity and purity. They have been designed to improve signal processing integrity when replacing conventional resistors in differential amplifiers or power supplies for high-end audio products. CAR resistors can also be used in the feedback, loading and gain stages of audio circuits.

In addition to a low current noise of less than -40dB, CAR resistors achieve an excellent temperature coefficient of resistance (TCR) and power coefficient of resistance (PCR), whilst offering a fast rise time of 1ns without ringing. They also feature a non-inductive non-hot-spot design and withstand electrostatic discharges of over 25kV.

CAR resistors can be trimmed to any tolerance and any value within the resistance range of 10Ω to 100kΩ and are available now.

www.charcroft.com

Expanded Offering of Next Generation Half-Brick DC/DCs

Murata Power Solutions has added two new ranges of single output, half-brick, isolated DC/DC converters to its product portfolio. The HPH series is a family of ultra-high output converters with different models capable of delivering up to 360W of power and 70A output current. The UCH series comprises modules that deliver between 50W and 150W of output power and a maximum output current of 40A – at a very low cost.

Both the HPH and UCH series are isolated to 2250VDC with an open-frame construction and are designed for PCB mounting. Both series are in compliance with RoHS legislation and have UL60950-1 and EN60950-1 safety approvals.

HPH DC/DC converters offer a choice of fully regulated single outputs, ranging from 3.3VDC to 12VDC. A wide input voltage range of 36VDC to 75VDC, combined with an industry standard pinout and package measuring 61mm x 58.4mm x 10.2mm, simplifies the use of the modules in low-voltage/high-current OEM applications. The new converters utilise a full-bridge, fixed-frequency topology along with synchronous output rectification that enables levels of efficiency up to 91% to be achieved. Operating temperature range is -40°C to +85°C. An optional baseplate further enhances thermal performance.

www.murata-ps.com

New UM Series Ultra-Compact PCB Mountable Supplies

Spellman High Voltage Electronics Corporation has announced the extension of its modular product line with the introduction of the UM Series. These printed circuit board mountable, high voltage modules offer easy form, fit and functional replacement for units presently available on the market. Utilising proprietary power conversion technology and high voltage packaging techniques, and aided by Spellman's advanced encapsulation techniques, the SMT-based UM series provides additional features compared to competitive models, at reduced cost.

The UM Series spans the output voltage range of 62 volts to 6kV in three power offerings of 4, 20 and 30 watts. An optional enhanced interface provides current programming capability and positive polarity, buffered, low output impedance voltage and current monitor signals. A second voltage programming input is also provided for negative polarity units, eliminating the programming inversion on the standard interface.

Current programming allows the user to set the unit's current limit, anywhere from 0 to 103% of maximum rated current. The UM can be used with confidence in demanding applications as these robust modules are fully arc and short-circuit protected.

www.spellmanhv.com/um

Cable Configurator For Ethernet Cabling

Harting has added a new cable configurator for Ethernet cabling to its Harkis catalogue information system.

With the new system, users can access and select the appropriate configuration of Ethernet cables and cable assemblies with only a few clicks. It also allows users to send an inquiry about the selected products directly to the company's sales department.

The cable configurator includes products for four poles (Category 5) and eight poles (Categories 5 and 6), as well as hybrid applications. The product portfolio comprises system cables in IP20 and IP65/IP 67 versions.

The new cable configurator can be found at **www.harkis.harting.com/harkisng/en/series/rji.**

The Harting Group develops, manufactures and distributes electrical and electronic connectors, network components, pre-assembled system cables and backplane assemblies. These products are capable of withstanding the harshest

demands in industrial environments and provide high data rates for electronic applications.

Harting connectors and network components are used in mechanical engineering and plant manufacturing, in automation systems, energy generation and distribution, and in electronic and telecommunication markets.

www.harting.com

Latching USB Cable Assemblies from GTK Ensure Secure Mating

Interconnect and opto-component manufacturer GTK has just announced the availability of latching USB cable assemblies that provide higher mating retention forces without having to specify any different connector sockets. Featuring side-mounted squeeze latches that mate with any standard USB A socket, the assemblies are available in USB 1.1 and 2.0 with cable length and the opposite end connector to meet customer specifications.

The new cable assemblies deliver all the usual speed and size benefits of the USB standard interface yet suit applications where a more secure latch is required. For example, if the application is subject to shock or vibration latching is a real benefit. Similarly, with consumer items such as iPods leads are quite likely to be trodden on, so a more secure attaching mechanism is highly beneficial.

GTK's new secure matching USB cable assemblies are available in any configuration for volume requirements.

The company has ISO 9000-certified manufacturing facilities in China, and now delivers a comprehensive range of standard and custom interconnection components to European and American OEMs.

www.gtk.co.uk

Mixed-Signal Oscilloscope Family For Ease of Use

The new Yokogawa DLM2000 Series is a new family of mixed-signal oscilloscopes (MSOs) that represent a major step forward in terms of price/performance specification and ease of use.

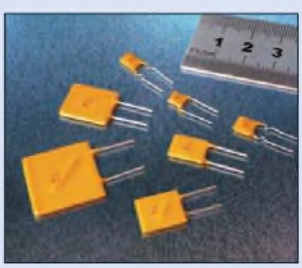
With up to 500MHz bandwidth and 2GS/s sampling speed, the new oscilloscopes have the longest memory (up to 125M points) and fastest update rate (up to 450,000 waveforms per second) in this class of instrument. In addition, the combination of flexible analogue and digital inputs, plus a large-screen display in a compact ergonomically-styled body, makes the instruments exceptionally easy to use.

In addition to the key performance specifications, the DLM2000 Series features a number of advanced measurement and analysis features, including histogram and trending functions, up to 20,000 history memories, digital filtering, zoom windows, user-defined mathematics and serial bus analysis.

The DLM2000 Series consists of six models: three with two channels and three with four, each covering the bandwidths 200, 350 and 500MHz, respectively. Mixed-signal oscilloscope operation is enabled on the 4-channel models by converting the fourth channel of analogue input to 8-bit logic, so that the instrument then functions as a 3-channel analogue plus 8-bit logic MSO. A high-resolution mode (up to 12-bit) is also available.

www.yokogawa.com

Polyswitch RKEF Device Designed For Smaller Electronic Equipment



Tyco Electronics has introduced a new line of PolySwitch circuit protection devices. Designed for use in a wide variety of general electronic products, ranging from industrial controls to battery packs, the new PolySwitch RKEF devices are functionally equivalent to the company's existing RXEF overcurrent protection devices, but are available in a significantly smaller form-factor.

Key device parameters for the PolySwitch RKEF series include hold-current ratings of 0.5A to 5A and trip-current ratings of 1A to 10A. All devices have a maximum operating voltage rating of 60V and can operate at up to 85°C – the same maximum operating temperature as the RXEF series.

PolySwitch RKEF devices are of through-hole construction and many of the radial-leaded devices have the same lead spacing as the RXEF devices. This facilitates easy replacement of RXEF devices and can help designers optimise board space and improve thermal conditions. Lead spacing for the RKEF250 and RKEF300 devices is half that of the equivalent RXEF parts, yielding even more space.

PolySwitch RKEF devices are EU ROHS and ELV compliant, are compatible with industry standard installation procedures and are available in tape and reel packaging for compatibility with high-volume manufacturing.

www.tycoelectronics.com

Flexible, High Performance 50MHz Arbitrary Waveform/ Function Generator

Keithley Instruments has introduced the Model 3390 50MHz Arbitrary Waveform/Function Generator, featuring the highest waveform resolution and best price-to-performance value in its class. The Model 3390 is a flexible, easy-to-use programmable signal generator with advanced function, pulse and arbitrary waveform capabilities. Superior signal integrity, faster rise and fall times, lower noise and greater waveform memory combine to provide high quality output signals.

Among its many useful features, the Model 3390 includes 50MHz maximum sine wave frequency; 25MHz pulse frequency with 10ns minimum width; arbitrary waveform generator with 256k-point, 14-bit resolution; built-in function generator capability including sine, square, triangle, noise, DC etc; precision pulses and square waves with fast (< 10ns) rise/fall times; built-in 10MHz external time base for multiple unit synchronisation; built-in AM, FM, PM, FSK, PWM modulation; frequency sweep and burst capability; LXI Class C-compliant Ethernet, TMC compliant USB and standard GPIB interfaces; digital pattern output port and control capabilities; and industry-leading sample speed and memory depth.

The Model 3390 can perform six different key functions in one package, saving valuable rack space and eliminating the need to purchase separate instruments.

Keithley is offering the Model 3390 for a special introductory price.

www.keithley.com

High Density AC/DC Switching Power Supplies

The CF series from Murata Power Solutions is a new range of high density AC/DC switching power supplies. The single main output 200W and 350W open-frame units offer industry standard form-factor and high density. They are ideal for use in distributed power architecture applications, redundant (N+1) operations, information technology equipment and industrial applications.

The series comprises a 200W model with a 12V (16.6A) main output and a choice of three 350W models, giving designers the choice of a 12V (29A), 24V (14.5A) or a 48V (7.2A) main output. All power supplies in the CF range offer a universal input (85 to 265VAC) with active power factor correction (PFC). They also feature an auxiliary 5V standby output to allow for system housekeeping and monitoring.

The 200W CF200-A12C has a high power density of 8W/in^3 that helps minimise the space required in customer applications. Synchronous rectification allows an efficiency level of over 80% to be achieved. Built to meet 1U height restrictions, the ruggedised open frame, U-channel package CF200-A12C has compact overall dimensions of 127mm x 84mm x 39.6mm.

350W models (CF350-A12C, A24C and A48C) achieve a power density of 9.5W/in^3 and similar levels of efficiency to 200W variants.

www.murata-ps.com

Pressure Sensors in New SMT Housings

Sensortechnics's new HDO series is based on proven micromachined silicon elements to ensure highly stable and reliable pressure measurements. These sensors offer a wide selection of absolute, differential and gage pressure ranges from 10mbar up to 10 bar and feature an excellent price/performance ratio.

The HDO pressure sensors are precision calibrated and temperature compensated and intended to be used with air and non-corrosive gases. Innovative SMT housings allow for easy PCB-mounting and maximum OEM design flexibility. For all HDO sensors Sensortechnics can provide custom-specific pressure ranges and calibrations on request.

Due to its high accuracy and very wide measuring range Sensortechnics's new HDO series can be ideally used in many demanding OEM device applications like medical devices, instrumentation, environmental controls and HVAC.

www.sensortechnics.com

World's First USB 3.0 Protocol Analyser Exerciser System

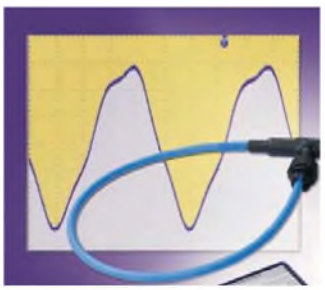
LeCroy Corporation announced its Voyager verification system, the world's first protocol analyser for USB 3.0, also known as SuperSpeed USB. Using custom front-end circuitry developed in conjunction with LeCroy's 5Gbps PCI-Express platform, the Voyager analyser provides simultaneous protocol capture of both USB 2.0 and USB 3.0 signaling. Available with an integrated exerciser option, this sixth generation verification platform is LeCroy's complete solution for testing USB devices, systems and software.

The USB 3.0 specification development was announced in September 2007 offering ten times the speed of USB 2.0 and backward compatibility with legacy devices. It features physical layer characteristics similar to PCI Express 2.0, including 5GHz signaling, that relies on link training to synchronise communication between devices. Aggressive power management represents an additional challenge for 3.0 validation teams as they contend with devices that frequently enter and exit low-power states.

To provide accurate data capture at 5GHz, the analyser must follow each link state transition and achieve bit lock in less than 1μs (when moving from idle to the active state). Any delay in signal lock can cause the analyser to miss data.

www.lecroy.com/europe

New LFR Complements CWT From PEM



A new LFR AC current probe with market leading low frequency performance has been introduced by Power Electronic Measurements Ltd (PEM). This compact, low-cost, clip-around probe is both flexible and dual-range, while being optimised to give minimal phase measurement error at frequencies from 45Hz to 20kHz. This is a Rogowski current probe, similar to PEM's highly successful CWT range, which covers 1Hz to 20MHz.

The LFR unit is ideal for use as a general purpose power frequency AC current probe and can be used with oscilloscopes, acquisition cards, data loggers, power analysers and meters. Other typical applications include power measurement, leakage current and power quality, where minimal phase error, low noise and good accuracy are key measurement criteria.

All Rogowski current probes generate noise, but the noise floor of the LFR is very small, and the LFR1/15 model is only 2.0mVrms on the 300A range. The rated output voltage is 6Vpeak for a 300A peak current, thus at 20% rated current the noise contributes less than 0.1deg additional uncertainty to the phase error. This is better than a measuring class 0.5 current transformer. The same unit with peak current rating 300A/3000A and coil length of 300mm has minimal phase measurement error at 50Hz of < 0.35deg and at 20kHz of < 1.8 deg.

www.pemuk.com

BestCap Series Addition for Wireless Applications

AVX Corporation has expanded its BestCap Series to include an ultra-low ESR double layer capacitors with an expanded temperature range from -40° to 75°C. Ideal for wireless applications, the capacitor series features high capacitance values and power pulse characteristics for high current, short pulse applications including GSM/GPRS wireless-based systems, USB modems, automatic meter reading systems, handheld scanners, battery chatter, dying gasp and memory back-up systems.

The BestCap double layer capacitors are available in three different standard sizes with voltage ratings from 3V to 15V and a capacitance range from 6.8 milli-Farad to 1 Farad.

The three standard sizes for the BestCap capacitor include BZ05 (20*15 mm), BZ01 (28*17 mm) and BZ02 (48*30 mm). The BZ05 size offers the most aggressive capacitance value offering of 68 milli-Farads at 5.5V and 6.8 milli-Farads at 15V. The BZ02 has the largest capacitance value with 1 Farad at 5.5V and 68 milli-farads at 15V.

Typical pricing for the double layer capacitors start at $2.90 each with delivery from stock to 10 weeks.

www.avx.com

www.stewart-of-reading.co.uk

OSCILLOSCOPES ON EXTRA SPECIAL OFFER

(For Limited Period Only)

TEKTRONIX

465	Dual Trace 100MHZ Delay Sweep	£75
465B	Dual Trace 100MHZ Delay Sweep	£95
466	Dual Trace 100MHZ Analogue Storage	£75
468	Dual Trace 100MHZ Delay Sweep Digital Storage	£125
475	Dual Trace 200MHZ Delay Sweep	£110
2214	4 Ch. 20MHZ Analogue 1 MS/S	£95
2215A	Dual Trace 60MHZ Delay Sweep Dual TB	£95
2220	Dual Trace 60MHZ Digital Storage. Cursors	£125
2225	Dual Trace 50MHZ	£95
2230	Dual Trace 100MHZ Digital Storage. Cursors	£195
2235	Dual Trace 100MHZ Dual TB	£150
2235A	Dual Trace 100MHZ Dual TB	£175
2236	Dual Trace 100MHZ Dual TB with Counter Timer & DMM	£175
2236A	Dual Trace 100MHZ Dual TB with Counter Timer & DMM	£195
2245A	4 Ch. 100MHZ Dual TB Delay Sweep. Cursors	£195
2430	Dual Trace 150MHZ 100 MS/S	£250
2445	4 Ch. 150MHZ Delay Sweep. Cursors etc	£195
2445A	4 Ch. 150MHZ Delay Sweep. Cursors etc	£225
2445B	4 Ch. 150MHZ Delay Sweep. Cursors	£250
2445B	With DMM 4 Ch. 150MHZ Delay Sweep .Cursors	£250
2465	4 Ch. 300MHZ Delay Sweep. Cursors etc	£300

2465A	4 Ch. 350MHZ Delay Sweep. Cursors etc	£400
2465B	4 Ch. 400MHZ Delay Sweep. Cursors etc	£500
2465B	Rack Mount 4 Ch. 400MHZ Delay Sweep. Cursors etc	£400
2467	4 Ch. 350MHZ Delay Sweep. Cursors etc	£400
TAS 465	Dual Trace 100MHZ Delay. Cursors	£195
TAS 485	4 Ch. 200MHZ Delay. Cursors	£275

HP

54501A	Digitising 2+2 Ch 100MHZ 10 MS/S	£150
54502A	Digitising 2 Ch. 400MHZ 400 MS/S	£250
54600A	Dual Trace 100MHZ 20 MS/S	£195
54600B	Dual Trace 100MHZ 20 MS/S	£225

PHILLIPS

PM3052	Rack Mount Dual Trace 60MHZ	£75
PM3055	2+1 Ch. 60MHZ dual TB/Delay. Autoset	£95
PM3065	2+1 Ch. 100MHZ dual TB/Delay. Autoset	£125
PM3084	4 Ch. 100MHZ Delay TB	£140
PM3335	Digital Storage Dual Trace 60MHZ 20 MS/S	£125
PM3337	Rack Mount Digital Storage Dual Trace 60MHZ 20 MS/S	£125
PM3365A	Digital Storage Dual Trace 100MHZ 100 MS/S	£150

HITACHI

V222	Dual Trace 20MHZ DC Offset, Alt. Mag	£50
V522	Dual Trace 50MHZ DC Offset, Alt Mag	£65
V665	Dual Trace 60MHZ Delay Sweep. Cursors etc	£75
V1065	Dual Trace 100MHZ Delay Sweep. Cursors etc	£85
V1065A	Dual Trace 100MHZ Delay Sweep. Cursors etc	£95
V1150	4 Ch. 150MHZ Delay Sweep. Cursors. DVM etc	£125

HAMAG

203.4	Dual Trace 20MHZ Component Tester	£75
203.6	Dual Trace 20MHZ Component Tester	£85
305	Dual Trace 03MHZ Analogue/Digital 40 MS/S per Channel Component Tester	£140
604.2	Dual Trace 60MHZ Component Tester	£125

STEWART of READING
17A King Street, Mortimer, Near Reading RG7 3RS
Telephone: (0118) 933 1111
Fax: (0118) 933 2375
www.stewart-of-reading.co.uk
9am-5.00pm Monday to Friday

See our website for 1,000's of items currently in stock

Used Equipment – GUARANTEED.
Most Manuals supplied
Please check availability before ordering or calling.
Prices plus carriage and VAT

WEBSITE DIRECTORY

Beta Layout Ltd

www.pcb-pool.com

The Best Value Online PCB Prototyping Service Available:
Instant on line quotations & ordering (no pre registration).
We offer the following:
• No minimum quantity. • No tooling charges. • No drill Limitations. • 1 to 6 layers (prototype quantities) • 2 layers (small production batches) • Fr4,1.6mm,35 um,HASL (Pb free/Rohs/Weee) • Soldermask / Silkscreen (optional) • Leadtimes from 2 -8 working days • Full DRC on all orders (we manually check every file !!!). • PCB-POOL®

accepts direct outputs from 15 major layout softwares (see our website for details)
Download our fully functional PCB LAYOUT software FREE of charge.
Free Phone : 0800 3898560

Sky systems ltd

www.sky-pcb.com

Sky Systems Ltd. was established with the vision and promise of providing manufacturing high quality, cost effective solution and one-stop service to meet the most demanding of our customers' requirements.
We offer the followings:
• 1-12 Layers • Fr-4 / Cem-3 • HAL(Lead Free),Flash Gold, Electroless Gold Plating, OSP ,Immersion Silver, Immersion Tin • Gold Finger • Soldermask • Silkscreen • Routing / Punching / V-Cut • Online quotation • FREE PCB Prototype with quantity orders • Short

lead time • Fast worldwide delivery • Flexible quantity • CHINA Factory
For more information or request a quote today from our web site.

Designer Systems

http://www.designersystems.co.uk

Professional product development services.

• Marine (Security, Tracking, Monitoring & control)
• Automotive (AV, Tracking, Gadget, Monitoring & control)
• Industrial (Safety systems, Monitoring over Ethernet)
• Telecoms (PSTN handsets, GSM/GPRS)
• AudioVisual ((HD)DVD accessories & controllers)
Tel: +44 (0)1872 223306

Microchip Technologies

http://www.microchip.com/

Microchip Technology Inc. is a leading provider of microcontroller and analogue semiconductors, providing low-risk product development, lower total system cost and faster time to market for thousands of diverse customer applications worldwide. Microchip designs, manufactures, and markets a variety of high performance components for high volume, cost-effective embedded control solutions, including 8- and 16-bit PIC® microcontrollers; dsPIC® digital signal

controllers; development kits; serial EEPROMs, more than 350 mixed-signal analogue and interface products; KEELOQ secure data transmission products; and the PowerSmart® family of smart battery management products. Microchip's product solutions feature compact size, integrated functionality, and ease of development.

Colour screen shot and text is just £350 + vat for 12 months

ADVERTISING ENQUIRIES CONTACT MATTHEW ON: 020 7933 8980

ADVERTISING

PCB DESIGN

PRODUCT DEVELOPMENT

TRANSFORMER MANUFACTURE

Increased Focus on Power Supplies and DC/DC Converters

Arrow Electronics has expanded its power technology portfolio by signing a distribution agreement with Recom, a leading global supplier of DC/DC and AC/DC converters. Arrow will sell and support Recom's complete power converter product range throughout Europe.

The new agreement is in line with Arrow's strategy to provide the widest possible range of power supply and converter technologies to designers across Europe. For Recom, the agreement will expand the penetration of its product ranges into European markets and ensure that customers have access to products and support at a local level.

Available in single, dual, and triple rail outputs and a wide variety of input and output voltage configurations, power ratings, and isolation voltages, Recom converters are used in most industries requiring low- to medium-power voltage conversion in the 0.25W to 60W range. The company also offers the largest range of safety agency-approved converters from any manufacturer.

www.arrowne.com

PCB DESIGN

Harwin Names Abacus Pan-European "Distributor of the Year"

High-reliability interconnect company Harwin has named Abacus Group plc as Pan-European Distributor of the Year, citing "outstanding commitment" as the differentiating factor which resulted in the Newbury UK-headquartered company being given the award.

Abacus Group Plc is one of the leading distributors of electronic components in Europe, with directly-owned group companies in every major European electronics market. "Abacus has been a vital part of our distribution network for many years, providing exemplary customer service through a wide number of regional offices in the UK, Germany, Austria, France, Italy, Benelux and Scandinavia. They have demonstrated very high levels of focus in taking our new and existing product portfolio to market and we are delighted to name them Pan-European Distributor of the Year," said Harwin's MD, Andrew McQuilken.

"Harwin is a fine example of what you can achieve if you continue to manufacture in Europe. The company is quick to market with innovative new products and – because it retains all manufacturing processes in-house – is very quick to respond to requests for full custom or modified parts. We are honoured to receive this award," said Michelle Burns, Product Manager Emech at Abacus.

Harwin is a manufacturer of standard and custom interconnect components.

www.harwin.co.uk

Fanless Systems

Panel PC
Systems
Chassis
Mini-ITX
EBC
SBC

1.2GHz VIA Esther

EPC-4853

- VIA Esther 1.2GHz
- Up to 1GB DRAM
- MPEG4/WMV9
- Dual LAN
- Compact Flash Socket
- Mini-PCI
- Internal HDD option
- PXE Discless Boot

500MHz ULV

EPC-500

- 500MHz VIA Eden ULV CPU
- VESA mounting option
- Low Power < 15Watts
- CompactFlash
- 10/100MBS LAN
- 3xUSB
- 2xRS232
- HDD option

1GHz VIA Eden

CMB-365

- 1GHz VIA Eden
- Wall or Desk mounting
- Internal HDD option IDE or SATA
- Up to 1GB DDR2 memory
- DVI or LVDS options
- Two Mini-PCI Slots
- GigaBit Ethernet

1.6GHz Core 2

EPC-6200

- 1.6GHz Low Voltage Core 2 Duo
- GME965 & ICH8M
- Up to 3Ghz SDRAM
- Dual GigaBit LAN
- Dual IEEE1394
- Dual DVI Ports

Core 2 Bare Bones

CMB-371

- Core 2 ULV CPU
- Intel 945GM chipset
- Up to 2 GB DDR2
- GigaBit Ethernet
- LVDS, TV and DVI outputs
- Intel Graphics Media Accelerator 950
- 4xUSB2.0
- Mini-PCI slot

For more details of LCDs, touch panels and embedded boards and systems visit www.bvm-store.com or call 01489 780144.

BVM
Embedded Intelligence

BVM Limited, Hobb Lane, Hedge End, Southampton, Hants, SO30 0GH
Tel: 01489 780144 Web: www.bvm-store.com Email: info@bvm-store.com

Microsoft Windows Embedded Partner

SGS UKAS

ISO9001:2000

PMC | VMEbus | Embedded | Systems

Microelectronic solutions from Sharp

Sightseeing in Munich in November

[LED] [IC] [LCD] [RF] [OPTO]

You can walk for miles round Munich, but the direct route to success takes you straight to the Sharp stand at electronica 2008 (**Hall A3, Booth 207**). This year's innovative highlights include LED solutions, blue lasers and e-signage LCDs of various sizes up to an impressive 108" and including a brand-new 82" high brightness display with a maximum luminance of 1500 cd/m². Sharp will also be represented at the cutting-edge electronica e-Signage Forum. Sharp's wide range of system solutions means you can start planning for success with your next-generation applications. We look forward to welcoming you at Sharp's electronica 2008 stand.

E-mail: info.sme@sharp.eu
Phone: +49 (0)180 507 35 07

electronica
Visit us at the electronica 2008
from 11 to 14 November in Munich: Hall A3, Booth 207.

SHARP | Microelectronics