VOLUME 113, ISSUE 1855

JULY 2007 £4.60

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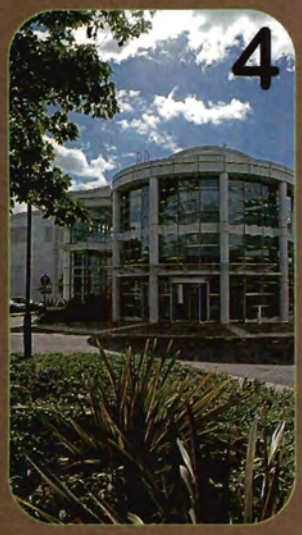

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EDITOR: **Svetlana Josifovska**
EMAIL: svetlana.josifovska@stjohnpatrick.com

PRODUCTION EDITOR/DESIGNER: **Tania King**
EMAIL: tania.king@stjohnpatrick.com

DISPLAY SALES EXECUTIVE: **Matthew Dawe**
TEL: +44 (0) 20 7933 8999
EMAIL: matthew.dawe@stjohnpatrick.com

SUBSCRIPTIONS: **Dovetail Services**
800 Guillat Avenue,
Kent Science Park,
Sittingbourne,
Kent, ME9 8GU
TEL: +44 (0) 870 428 1426
EMAIL: saintjohnpatrick@servicehelpline.co.uk

SUBSCRIPTION RATES:
1 year: £46 (UK); €120 (Europe);
$145 (US & worldwide)

PRINTER: **William Gibbons Ltd**

NEWSTRADE:
Distributed by Seymour Distribution Ltd,
2 East Poultry Avenue, London, EC1A 9PT
+44 (0) 20 7429 4000

PUBLISHER: **John Owen**

St John Patrick Publishers

The Emperor's new clothes

The process of digitisation is unstoppable. It is just about everywhere: our homes, cars, factories – everywhere but one place where the doors seem to have been firmly shut until now. That sector is Energy. It seems to have been left to its own devises since pretty much its inception. But, an interesting development between IBM and CenterPoint Energy from Houston, Texas, is heralding a new era – the digitisation of electrical grids.

CenterPoint plans to upgrade its switches, equipment and meters at its power substations across Texas in an effort that will cost it some $750m over five years. With the help of IBM, the utility firm will implement a so-called broadband-over-powerline (BPL) network which will gather and carry information of real-time energy usage or overloaded distribution points to make power distribution grids more reliable.

In turn, this is expected to help consumers tailor their energy usage better but also save on their bills. CenterPoint's $750m expenditure equates to some $2.50 per customer per month, which undoubtedly will be absorbed into the customer rate payments. However, analysing the benefits this will bring overall, it is a small price to pay.

IBM's digital equipment will allow energy distributors to introduce more services, such as time-of-use pricing, leading to better managed demand. The accompanying software will help collect the information but also it will double up as an analytical tool for measuring usage patterns, for example.

Clearly, this is just the beginning. There have been talks of automated metering for a couple of years now, and companies like LEM are already producing the systems needed to monitor energy usage and meter it.

Utility firms have been testing the equipment and installing it. Clearly, the revolution has begun, but different regions will go though it at different times. The US for example is going to lead in this field, even though Europe and Asia are also expected to digitise their energy services soon.

The direction is clear, however: The effective monitoring of energy consumption has become critical in today's environmentally-conscious world. It is also a way forward in managing the increasing energy prices and meeting the new directives that are being placed to reduce global energy consumption. Digitisation of the grids is a good starting point to help consumers take greater responsibility for their energy consumption.

Svetlana Josifovska
Editor

Electronics World is published monthly by **Saint John Patrick Publishers Ltd,** 6 Laurence Pountney Hill, London, EC4R 0BL.

IMEC demonstrates feasibility of 3D-stacked IC integration

Eight-channel wireless IC system

IMEC (Interuniversity Microelectronics Centre) researchers in Belgium have demonstrated the potential of three dimensional (3D) integration using standard front-end techniques for via fabrication. Functional 3D via chains through silicon were realised at densities of up to 10,000 per mm^2, with via pitch of 10µm for via diameters of 5µm and via heights of under 20µm.

By using copper to fill the 3D vias and direct copper-to-copper thermo-compression bonding to interconnect the die, the resistance of the vias was consistent with bulk copper resistivity, without significant contact resistance at the bonded interface. Extremely thin bulk silicon die containing the silicon vias were stacked and interconnected.

Within the 3D-stacked IC process, copper vias are processed immediately after the contact layer and before processing the back-end-of-line (BEOL) metal layers using regular single damascene techniques. Vias are subsequently opened at the back of the wafer by aggressively thinning the silicon wafer down to 10-20µm. The thinned wafer is diced using a regular blade dicing process, after which dies are attached and electrically interconnected to a copper/dielectric substrate. The process is inherently extendible to wafer-scale stacking.

IMEC claims that the 3D-stacked IC approach has several advantages over other advanced 3D approaches. It achieves far higher via densities than integration schemes using packaging-type technologies, where wide vias are made after completion of BEOL layers. The copper vias are processed before applying BEOL metallisation, leaving the BEOL routing capabilities unaffected. The direct copper-to-copper bonding avoids the formation of intermetallics at the bonded interface.

These results were obtained within IMEC's core program on sub-32nm CMOS.

NPL time signal transmitter relocates

Extremely accurate time signals have been transmitted from Rugby, Warwickshire, since 1927, with the National Physical Laboratory (NPL) being responsible for them since 1950. From April 1 this year these signals will be transmitted from Anthorn on the west coast of Cumbria and will be known as "The time from NPL". They are accurate to better than one thousandth of a second and are used to support a wide range of professional services, including 999 communications, train companies, cash machines and mobile phone billing systems.

The time signal is derived from the NPL atomic clocks at Teddington, London, which is one of just five laboratories worldwide using the latest caesium fountain clock to contribute to Coordinated Universal Time (UTC). The 60kHz frequency at which the signal is broadcast is so accurate that it is used by frequency calibration laboratories to tune and standardise equipment and by television and audio repair companies as a standard.

NPL time-teller moves to new premises in Cumbria

Ultra-fine lithography developments

Recent progress in water immersion lithography means it is fairly certain that this technique will be used for the production of chips with 55nm and 45nm features. The optical resolution limit is set by the refractive index of water, yet it seems unlikely that this limit can be overcome by the use of other liquids and systems in the time scale required to meet the demand. We can only hope for some evolutionary step that will enable immersion technology limits to keep up with Moore's law.

Double patterning technology (DPT) may be the most probable next lithography technique to achieve 32nm features, but there is a choice involved. Double patterning is distinct from the double exposure method that is much used with alternating phase shift masking. Higher resolution through double patterning technology requires the sequential exposure and development of different resist films with multiple etch steps to transfer the resist patterns into the substrate. Some of the double patterning techniques form the final circuit by interdigitating and stitching together the results of individual exposures. Although double patterning still needs much developmental work, it appears almost inevitable it will be adopted in the fairly near future, as other next generation lithography techniques, such as EUVL, seem unlikely to be ready for production early enough to meet the demand.

Transistor is just one atom thick

A group working in the School of Physics and Astronomy at the University of Manchester has created transistors that are only one atom thick and less than fifty atoms wide. These transistors are based on graphene, which is a single layer of carbon atoms densely packed into hexagonal cells with a benzene structure. It can be made into one of the thinnest materials available.

This work suggests that it may be possible to form some of the electronic circuits of the future on a single sheet of graphene. Such circuits could include a central element, semi-transparent barriers to control the movement of individual electrons, interconnect devices and logic gates.

Consumer market demand affects SOI trends

Massive changes in the gaming and PC industry require new technologies and materials

The effect of massive changes in the gaming and PC industry are spurring the need for new technologies and materials, said Andre Jacques Auberton Herve, president and CEO of Soitec in Grenoble, France.

Speaking at the Industry Strategy Symposium (ISS) organised by SEMI in Zürich, Switzerland, in March, he said the technologies and materials are needed to break through traditional barriers of capacity, cost, implementation and market potential. He noted that just 10% of transistor performance improvement in IBM's 0.18μm devices was due to traditional scaling, with the remainder coming from innovation. However, in 32nm devices that ratio is changed to less than 10% improvement coming from traditional scaling. Advancing substrate engineering with silicon-on-insulator (SOI), strained SOI and new materials such as germanium-on-insulator (GeOI) are enabling successes including increased clock frequency and the merging of the consumer and PC products. Beyond Moore's Law, Herve sees a need for the collective treatment of nano-objects: DNA cells, quantum dots, memory nanocrystals, etc.

Herve concluded by saying that bulk silicon is reaching its limits and material innovation is now needed to extend Moore's Law. SOI is breaking through traditional barriers in terms of capacity, cost, implementation and market potential. The expanding SOI ecosystem and increasing manufacturing volumes are further enhancing the SOI value proposition, driving greater adoption.

He expressed the view that SOI tackles the industry's current challenges head on, offering significant performance and cost of ownership advantages. He referred to the future as an "Innovator's Dilemma" with the electron, photon and bio on the same chip.

This year, some 117 firms won a Queen's Award for Enterprise. Among them are CSR for its BlueCore family of single-chip Bluetooth ICs; Motorola for its point-to-point fixed wireless solution (gained through the recent acquisition of Orthogon Systems); Tacktick for its Micronet range of wireless, solar-powered marine electronics devices; 4i2i Communications for video coding and error correction IP and Quantum Research for its embeddable touch sensor technology. The awards include those for innovation, sustainable development and international trade among others.

* * *

The smartcard industry is expected to reach a new record in 2007 with four billion cards shipped, says Eurosmart, the international association of the smart secure technology industry. This means that in 2007, the smartcard will continue its growth at the 16% rate. Of these four billion cards, some 500 million will be contactless, including memory-only with basic security to the secured contactless devices used for as e-Passports, e-ID cards and EMV contactless cards. In 2006, the largest user of smartcards was Asia with 45.5% of total shipments received, followed by Europe with 40.9% and the Americas with 13.7%.

* * *

A survey of 320 companies conducted by Infosecurity Europe has found that 26% of organisations do not enforce a wireless security policy, even though most of the Chief Security Officers have expressed concern over the security issues of pervasive wireless networking. Most of the dangers lurk when corporate users access wireless networks out of the office and unwittingly connect to wireless networks that are insecure or even malicious. Phil Cracknell, President of ISSA UK, says that among the equally important security measures to be taken by any firm is to scan for new devices, rogue access points and drifting client cards that might choose to connect to networks nearby for a variety of reasons.

Industry is ready for 100GB transmission rate

After carrying out a study of high speed data transmission, the IEEE 802.3 working group formed the Higher Speed Study Group (HSSG), which has now decided that the time is appropriate to develop 100Gbit/s Ethernet standards. The supporters of Ethernet argued that it is not sensible to change its 10Gbit/s system to only 40Gbit/s, if 100Gbit/s can be attained.

The major telecommunications carriers say there is a demand for ten times more capacity, however the necessary technology has yet to be developed. Judging from the difficulties met in advancing from 10Gbit/s to 40Gbit/s transmission, these problems will be severe. For example, chromatic dispersion scales exponentially with bit rate, so even a 40Gbit/s rate requires one-sixteenth of the dispersion needed by the 10Gbit/s rate.

A serial single wavelength 100Gbit/s stream could utilise the available spectrum and bandwidth most efficiently, but many experts feel that a parallel approach will be the quickest way to achieve 100Gbit/s rates. Hence, it may well be that initially this rate will be achieved using multi-channels operating at lower bit rates to keep dispersion and similar problems within manageable limits.

Single-pixel camera aims to improve digital counterpart

Researchers at the Rice University in Houston, Texas, have created a single-pixel camera specifically designed to counteract the modern digital camera's inefficiencies and cost.

According to Dr Richard Baraniuk, who is part of the team, digital cameras are very wasteful as they require microprocessors and massive battery power to capture an image – most of which will not be used in displaying the picture.

"What is so inefficient about it is that we acquire all these numbers – for example 10 megapixels – only to throw away 80-90% when we do the compression process," he said. Although a digital camera picture may contain many millions of pixels, most photos can be described with far fewer because there is a lot of redundant or duplicate information in an image.

The researchers' single-pixel camera in turn uses micromirrors, similar to those used in Texas Instruments's Digital Light Processing (DLP) display technology. "Instead of taking the light from an object through a lens and focusing it on a pixel array, we actually reflect it off an array of mirrors," said Dr Baraniuk. "From that mirror array, we then focus the light through a second lens on to one single photo-detector – a single pixel."

The mirrors turn on and off as the light passes through the system. The 'camera' is connected to a computer, which runs an algorithm that interprets the signals and assembles a high resolution image from the thousands of sequential single-pixel snapshots – a process that takes several minutes to complete.

However, at this stage the set-up is still experimental and is very large. Once its size has been reduced, it could make digital cameras more efficient and dramatically improve battery life by doing away with the need to process and compress each image.

China to launch satellite navigational system

The recent launch of a fourth Beidon navigational satellite by China may indicate that it is to have a rival system to the US Global Positioning System (GPS) and to the European Galileo system in which it is already a partner. The latest Beidon satellite is joining three other Beidon craft in geo-stationary orbit.

China plans to launch a number of satellites that will form a "Compass Navigation Satellite System" offering high positioning accuracy to within 10m. China has said little about its plans, but has now announced that it intends to launch other navigation satellites this year to create a network covering all of China and some of its neighbours by next year. On an unannounced timescale, it will then expand the system to provide truly global coverage with the use of 30 medium earth orbit satellites.

As China has become a partner in Galileo with a contribution of the order of €200m, there is speculation that it may become a competitor as well as a partner. The Beidon satellites could use the same frequencies as Galileo, which would make it more difficult for its enemies to interfere with the transmissions in the event of hostility.

TOP 10 TIPS

PROFESSIONAL INDEMNITY INSURANCE

1 – Professional Indemnity Insurance is an essential cover for knowledge-based professionals – from sole traders to multinationals.

2 – You may be contractually obliged to have Professional Indemnity cover by your customers or to win contracts.

3 – It provides indemnity for losses you are legally liable for if you make a mistake or are negligent.

4 – It covers costs arising if your product or service is defective, inadequate or fails to perform.

5 – It includes legal costs or mediation costs for defending disputes over delays and failures in your products or services.

6 – It can also pay for compensation awards made against you.

7 – It can pay to rectify your mistake, in order to avoid a claim and litigation.

8 – It covers costs to your clients arising from any negligence or breach of duty of care on your part, breach of contract, accidental loss of their documents/data, defamation, dishonesty by your employees and intellectual property infringement.

9 – It helps minimise disruption to your business – an experienced claims handling team will provide access to a panel of specialist litigation lawyers so you can get on with your business knowing that the legals are all being handled professionally.

10 – In some cases, it will pay your fees if a dissatisfied client simply refuses to pay up.

This month's Top Ten Tips were supplied by Hanna Beaumont, La Playa Technology Division. For more information contact *www.laplaya.co.uk*

If you want to send us your top five or ten tips on any engineering and design subject, please write to the Editor: svetlana.josifovske@stjohnpatrick.com.

UK researchers have shown for the first time that knowing the structure of the surface layer of a multi-layer carbon nanotube is not enough to predict its electronic properties. The contribution of inner layers is crucial, which has serious implications particularly when it comes to fabricating electronic devices such as transistors and molecular interconnects. Single-wall carbon nanotubes can be regarded as individual sheets (one atom thick) of graphite which are wrapped up to form tubes. It is the diameter of the tube and the degree of helicity in this wrapping which determine the electronic properties. Different configurations can result in the tube behaving either as a metallic conductor or as a semiconductor.

* * *

Researchers at the University of Birmingham's School of Engineering are working towards achieving less interference for mobile phone users in built-up areas or easier access when phone traffic is very heavy, by using a novel class of materials called ferroelectrics.
The team has built thin ferroelectric films, less than 1 millionth of a metre thick, with a wafer of advanced superconducting material on the top. The structure combines ferroelectrics and superconductors – materials with no electrical resistance – that can be built into mobile phone basestations to enable them to function far more effectively in difficult circumstances.

* * *

US researchers have created a tiny robot that can move across the heart, delivering treatment and removing damaged tissue (see below).
The co-called HeartLander is only a few centimeters long, but moves at a speed of 18 centimeters per minute, controlled by "push and pull" wires from outside the body. It uses two sucker-like feet with which it moves across the heart.
Typically, it is inserted below the ribcage by keyhole surgery and is attached to the heart via a vacuum line to the suckers. The procedure can be carried out without having to stop the heart.
The research team now plans to add a radio-frequency probe to the robot to treat faulty heart rhythms by killing damaged tissue.

Is the glass half full or half empty?

Dr Anil Kumar, Director of Education and Policy at the Engineering and Technology Board emphasises that the Government, the industry and academia need to focus on attracting more students into engineering courses if the UK is to remain competitive in the medium to long-term future

During 2006, the ETB undertook several pieces of research examining some of the key issues surrounding labour supply. In particular, we focused on vocational engineering and technology provision within Further Education (FE).

Our research showed that there has been a startling 26% decline over the past three years in the number of 16-18 year old students on engineering and technology courses within FE.

Colleges are the training ground for tomorrow's technicians and a growing tributary for the Higher Education (HE) sector. Technicians make up 7% of the UK workforce (some two million jobs) and contribute to the design, development, manufacture, commissioning, operation or maintenance of all kinds of products, equipment, processes and services within UK industry. Consequently, this fall in student numbers gives real cause for concern.

Conversely, at the HE level, on the surface it appears that the supply of engineers and technologists is not a cause for concern. It's only when you analyse the data by discipline that issues appear.

Over the past five years, the number of home acceptances onto engineering and technology degree courses has increased by 12% within the engineering disciplines. This translates to a 52% increase in civil engineering, 18% increase in mechanical engineering, 16% increase in chemical, process and energy engineering and 15% increases in general engineering and aerospace respectively. But there have been decreases. Electronics and electrical engineering home acceptances have fallen by nearly 16% and 35% within production and manufacturing engineering.

Indeed, if we assume that the employment 'market' is working efficiently then we could even conclude that the demand from employers is fairly stable, particularly if we take the small increases in graduate starting salaries and similar small increases in employee average salaries as a proxy for demand (average graduate starting salaries for engineers and

technologists rose by 6% to just under £21,000 in 2005, compared with the 4% rise across all other subjects).

However, if we look to the medium-term future, the picture is not as assuring. By 2020, we will have a 12% demographic fall in 16 to 18 years olds who are currently the staple diet of the engineering and technology graduate courses. We have an ageing workforce within engineering and technology (the overall age profile of registered engineers in 2004 has a median age of over 55) and we have an increasing projected demand for intermediate and high skills (Source: Sector skills agreements for SSCs such as SEMTA).

Set this along side the real threat from China and India in particular, who in addition to their economic growth (10.2% and 9.2% respectively in 2006) and their increased STEM graduate output (124% in China over the past decade), are already confronting and moving resources to produce high value-added goods and services, all of a sudden Leitch's recently published ambitions for the long term skills needs of the UK is beginning to look like a prediction rather than a warning.

Within his recent report, Lord Leitch articulates that, "without increased skills, we would condemn ourselves to a lingering decline in competitiveness, diminishing economic growth and a bleaker future for all".

Whilst is it not yet clear what lies beneath the dramatic drop within FE or why there has been a fall in HE Electronic Engineering applications (the Institution of Engineering and Technology is planning to conduct a major study in this area), I believe that all prospective students should take heed of a recent survey undertaken by the Chartered Institute of Personnel and Development.

This report suggests that a third of graduates believe they studied the wrong course at university. Most of these said, with hindsight, they would have taken a more scientific or technical course, a business-based or a professional qualification. Add to this the identified positive monetary benefit to a student over their working life if they go onto study science and engineering subjects at university compared to other subjects (engineering comes out very favourably at increased lifetime earnings of £220,000 compared to the average £129,000), then the message is clear – study engineering and technology.

Individual aspirations aside, what is clear is that the future economic and social wellbeing of the UK will be primarily fuelled by its success from the science, technology, engineering and maths sectors. It is clear that implementation of the Government's 10-year science and innovation framework must continue apace and that Leitch's recommendations are equally rapidly discussed and implemented by Government, employers and individual learners – time is not a luxury we have.

A THIRD OF GRADUATES BELIEVE THEY STUDIED THE WRONG COURSE AT UNIVERSITY. MOST OF THESE SAID, WITH HINDSIGHT, THEY WOULD HAVE TAKEN A MORE SCIENTIFIC OR TECHNICAL COURSE, A BUSINESS-BASED OR A PROFESSIONAL QUALIFICATION

As a born optimist I would always suggest that the glass is half full, but as a realist I would observe that at the moment it has a large crack in it.

This information alongside other key statistics is available in 'Engineering UK 2006', published by the ETB and available for free on the website at ***www.etechb.co.uk/engineeringuk2006***

The core purpose of the Engineering and Technology Board (ETB) is to ensure UK business and industry has access to an adequate supply of innovative and skilled individuals, so the phrase "evidence-based action" is one we use frequently. We want to identify the areas most at risk from engineering skills shortages and work together with the engineering community to develop solutions.

GERMAN EFFICIENCY.

Built by Siemens, the world's fastest series production train will soon be travelling from Madrid to Barcelona

ELECTRICAL, ELECTRONICS AND INDUSTRIAL GIANTS DON'T COME ANY BIGGER THAN SIEMENS, SAYS JUAN PABLO CONTI

Perhaps to the degree that no other engineering organisation has been able to match, Siemens AG is one of those extremely rare companies whose actions inevitably touch the daily lives of practically the entire world population.

Some might argue Microsoft may have a similar claim. But even if Bill Gates's empire is actually managing to permeate the lifestyles of the same number of people Siemens is, it would still be doing so on a very one-dimensional aspect: the software running on their computers.

The combination of sheer scale (475,000 employees spread over 190 countries) and diversification of its business (built over a period of 160 years) put this German powerhouse of electrical, electronics and industrial equipment and services in a league of its own.

Still not convinced Siemens products are part of your daily life? Check the brand of your car's headlight lamps – chances are they are Osram, a Siemens company and the world's largest maker of lighting products. So among the light bulbs, halogen and fluorescent lamps illuminating your home and office too, there's bound to be a Siemens product.

Even if your lighting hasn't been built by the German company, there's a fair chance the power needed to operate them is being generated by one of the many fossil fuel power plants Siemens has helped equip around the world. Apart from power generation, electricity transmission and distribution is another area where the vendor enjoys a strong presence.

And this is still only the tip of the iceberg. Next time you board a train, metro, tram or any type of electric-driven carriage that runs on a rail track, look for the name of the manufacturer. Ever since it built the world's first electric train in 1879, Siemens has been a well known supplier of railway technology.

In the healthcare space, the company is at the forefront of information technology. Its computed tomography, magnetic resonance, molecular imaging, ultrasound and radiology devices are in the vanguard of medical imaging innovation.

The world's largest supplier of water treatment products and systems, more than 200,000 locations worldwide use Siemens expertise to help purify their water. Telecommunications; automotive electronics and mechatronics; industrial automation and control; corporate IT infrastructure; building technology and security; airport baggage handling; road traffic control... whether you like it or not, your paths will just keep crossing with those of Siemens.

Smartening Things Up

If one were to search for a common thread running through each of the 11 business units that form the operations part of the Siemens group, a certain pattern would emerge. This would reveal a systematic approach to taking advantage of the latest advances in electronics to try and improve the performance and efficiency of conventional electrical and mechanical based devices, systems and processes.

So when it comes to power transmission and distribution, for example, the focus would be on adding intelligence to the operation of national grids and high-voltage lines in order to more

..and multiplicity


A Fujitsu Siemens tablet PC


New software allows Siemens MR tomographs to deliver sharp images even if scanned patients move


New lithotripter for Siemens's mobile urology platform

efficiently meet the growing demand for electricity. The same basic concept goes for the operation of manufacturing automation equipment, electrical equipment in buildings, railway systems or lighting products.

Enno Pflug, a spokesman for the company's automotive arm (Siemens VDO), tells *Electronics World* the same principle is driving many of the innovations currently being developed and marketed by his unit. And he gives two examples. The first one is a revolutionary electronic wedge brake system that has proven during recent winter testing near the Artic Circle in Sweden to reduce stopping distances on ice and snow by an average of 15% compared with vehicles equipped with conventional hydraulic brakes.

"The system exploits the wedge principle's self-energising effect," Pflug explains. "It uses the kinetic force of the moving car to make it stop faster. A highly efficient electronic control unit and electric motor coordinates the braking mechanism." The system was entirely developed by Siemens VDO in a process that has taken so far seven years since the idea originally emerged from its R&D labs. Series production is scheduled to start in 2010, although a number of car manufacturers are already testing the unit.

The winter tests in Sweden showed that, by the time it took a mid-range class vehicle equipped with prototype electronic wedge brakes to come to a complete stop from a speed of 80km/h, the same car using state-of-the-art hydraulic brakes, modern ABS and winter tires was still travelling at 30km/h. "Each wheel has its own intelligence and, should some form of electronic failure occur, they can still stop for themselves," says Pflug.

The other example he gives is a technology called "Piezo direct injection", which injects the fuel directly into the vehicle's engine using high pressure. "The system turns the fuel into spray, which burns more easily and reduces CO2 emissions and fuel consumption by up to 20%," says Pflug. Siemens VDO was the first company to bring the technology into series production for diesel engines, while last year BWM became the first automaker to incorporate a gasoline version.

Asked about the electronic components controlling the Piezo system, Pflug said: "This powertrain technology has a 32-bit microcontroller that needs enough processing power to predict extremely quickly what kind of injection, airflow and so on is constantly required".

Urban Jungle

Not surprisingly, Siemens is benefiting from two major global trends currently shaping our world – increasing urbanisation and growing demand for electricity.

Asia Pacific in general and China in particular (Siemens's third largest individual market after the US and Germany) are seeing rapid industrialisation, in part fuelled by the off-shoring of manufacturing activities by American, European and Japanese companies. This is in turn, driving demand for the vendor's factory and process automation solutions.

Meanwhile, in the developed world, demographic changes such as aging populations are playing to the German vendor's strengths in areas such as medical diagnostics and automobile safety. Older drivers are indeed ideal marketing targets for vendors of cars that brake faster, feature lane departure warning systems or can park themselves.

But not all is plain sailing for Siemens. One of the group's most turbulent business areas as of recent times has been that of telecommunications (or 'Com', as the company used to name it). Communications have been at the heart of what Siemens does from the very beginnings. In fact, when the company was founded on the

Cars that park themselves, a Siemens VDO invention

Siemens VDO's electronic wedge brake system

1st October 1847, it was done based on the prospects of a new telegraph machine invented by Werner von Siemens, which featured a more user-friendly interface than the Morse code.

For 159 years, telecommunications technology remained one of the engineering flags most proudly flown at Siemens. Not that long ago, when David Beckham was playing in his first couple of seasons for Real Madrid wearing a Siemens Mobile sponsored shirt, it wasn't rare to hear the business media referring to the German vendor as "the mobile phone maker".

Then, by the end of 2006, the unthinkable had happened. Not only had the mobile handset division gone bust after recently been sold to Taiwanese electronics group BenQ following tumbling market share, but the entire emblematic Com unit of Siemens was being dissolved – with a growing corruption scandal involving some of its senior staff only serving to further muddy the waters (see the panel "Tarnished Image" for more information).

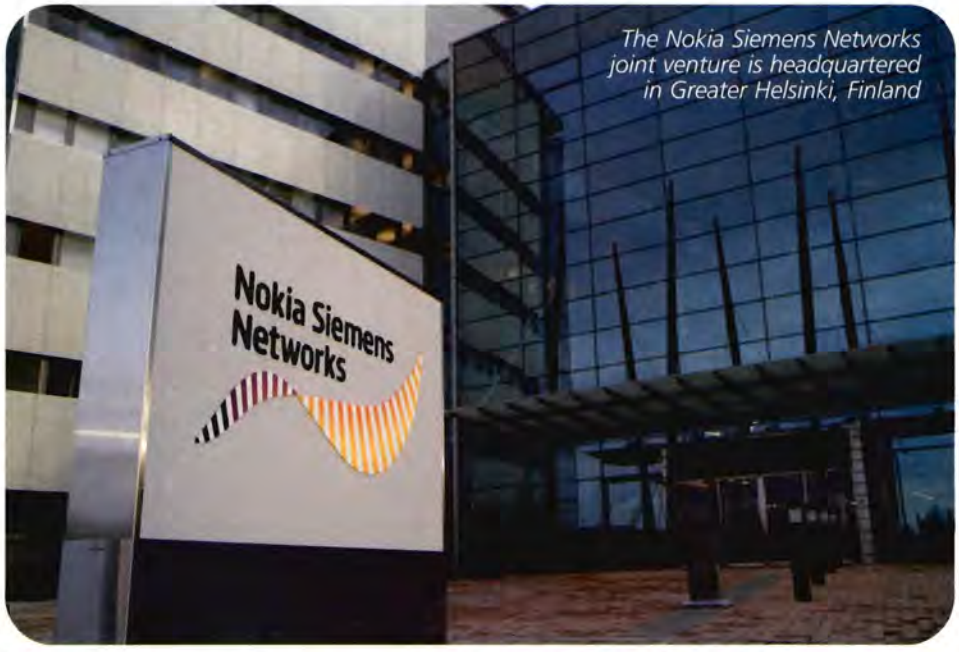
The now defunct Com group – Siemens's biggest revenue generator with sales of €13bn during fiscal 2006 – was until recently the home of not only the Mobile Devices unit, but also of the Carrier Networks, Enterprise Networks, Wireless Modules and Home & Office Communications Devices (SHC).

However, revenue alone is rarely what really counts. Of the €13bn that Com generated last year, only €283m translated into profit (and that's after Siemens Mobile had been sold to BenQ). Either poor profit margins or the realisation that the two largest businesses within Com were not actually large enough to compete in an increasingly consolidating telecoms market prompted the company to hold them for disposal, while the smaller (Wireless Modules and SHC) businesses were relocated to other internal units.

Hello, Nokia

Eventually, at least for one of the company's key businesses, a solution was found. The carrier networks and services division was merged with that of Nokia, in a joint venture that was announced back in mid-2006 but became officially operational on 1st of April 2007.

According to Dana Cooperson, practice leader of network infrastructure at research firm Ovum-RHK, what ultimately motivated the formation of Nokia Siemens Networks (NSN, as the company was called) was the need for larger scale created by growing convergence. "Siemens had been trying to decide for some time what to do with its carrier group. It did not seem prepared to invest to the point really needed and there were



The Nokia Siemens Networks joint venture is headquartered in Greater Helsinki, Finland

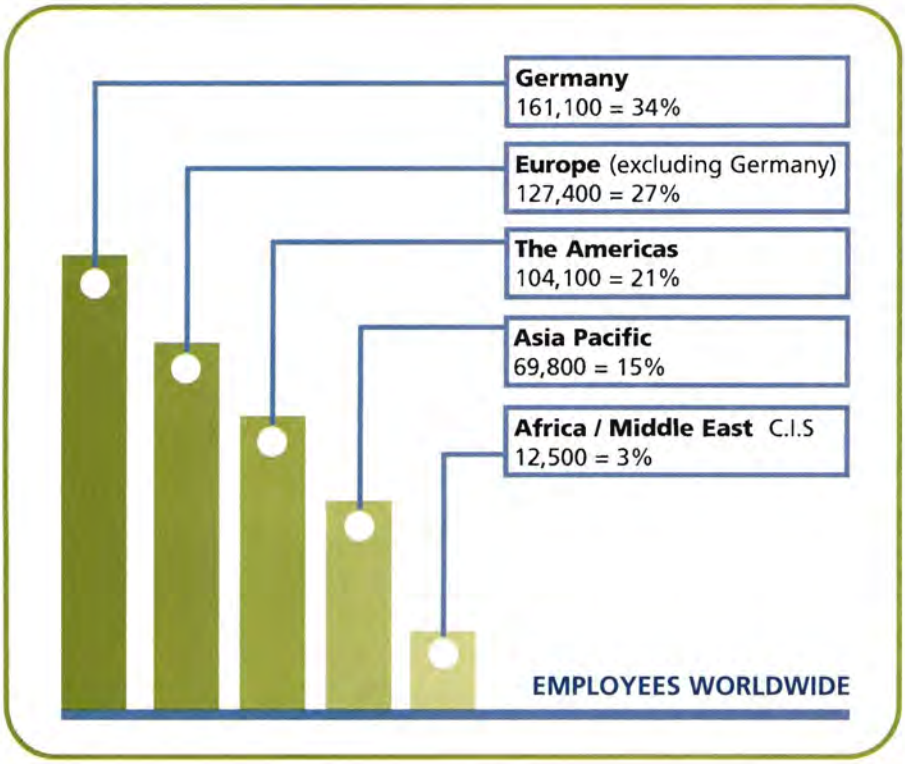
rumours that the group was not making money," he said.

"Scale is becoming increasingly important in telecom infrastructure, with many of the largest vendors becoming full-line suppliers and trusted partners to their carrier customers. They provide equipment, design help and other services – even to the point of running their customers' networks. And as fixed and mobile begin to converge so customers can have more seamless communications, there is some sense in the industry that a telecoms vendor needs both a wireless and a wireline play."

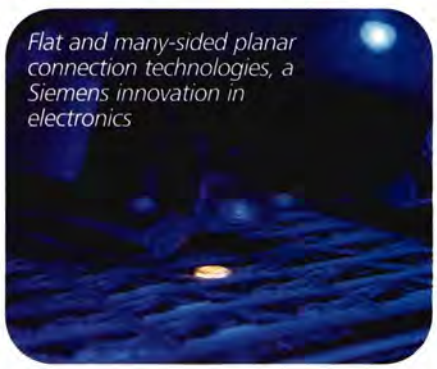
So what benefits can NSN expect from the joint venture? "The first one is cost savings," thinks Cooperson. "Of the €1.5bn in savings expected by the companies from the merger, a fully 40% is to come from rationalisation of the two companies' mobile product lines. Instead of both companies building and supporting a product for a given application, they will join forces and produce one. A similar goal was a key reason behind the Alcatel and Lucent merger."

"A second benefit relates back to scale. NSN becomes a stronger number two challenger to Ericsson and begins to have the scale to mount an assault on the number one spot," continued Cooperson. "NSN takes essentially all of Siemens's wireline product lines (which include optical networking, access and switching and routing gear, along with voice switches) and adds the two firms' rationalised mobile product lines together to become one of only several companies that have wireline, wireless and services – with Alcatel-Lucent, Huawei and ZTE its main competitors," says the analyst.

WiMAX technology, after a few years of hype and talk, is finally gathering speed in terms of




A new protective layer for Siemens's gas turbines received an internal 'Invention of the year' award


Flat and many-sided planar connection technologies, a Siemens innovation in electronics

SIEMENS IN BRIEF

Founded: 1847 by Werner von Siemens and Johann Halske

Headquarters: Berlin & Munich, Germany

President and CEO: Klaus Kleinfeld

Employees: 475,000 in 190 countries

Annual sales: €87.3bn (Fiscal 2006)

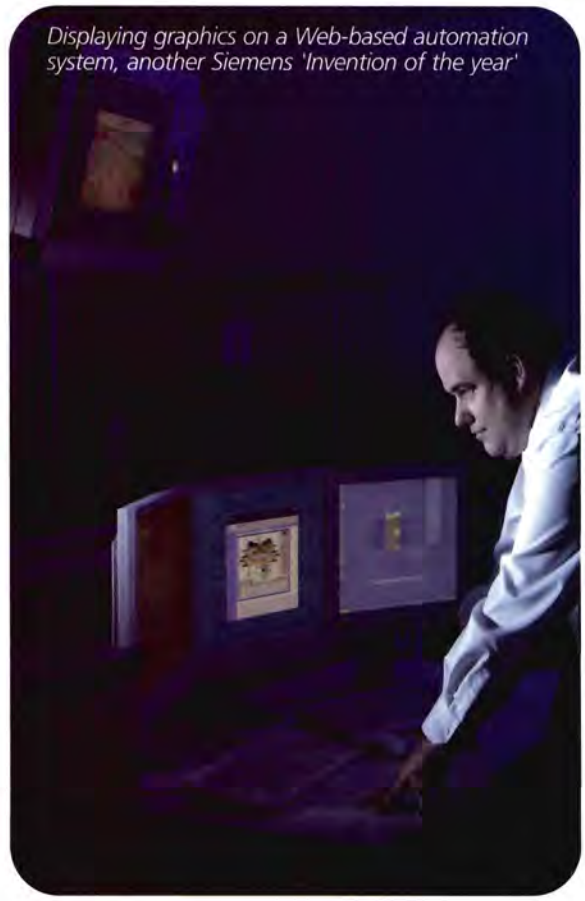
Net income: €3.0bn (Fiscal 2006)

R&D expenditure: €5.7bn (Fiscal 2006)

R&D team: 50,000 employees

Patent portfolio: over 62,000 (Europe's second largest patent applicant)

Listed: Frankfurt & NYSE



Displaying graphics on a Web-based automation system, another Siemens 'Invention of the year'

network deployments. Julien Grivolas, a senior telecoms analyst for the Mobile@Ovum advisory service, says the strategy that NSN has adopted to address the burgeoning WiMAX market was only obvious: "On one hand, Siemens developed its own fixed WiMAX (based on the IEEE 802.16-2004 standard) portfolio, called WayMAX@vantage. On the other hand, Nokia has always focused its efforts on mobile WiMAX (based on the IEEE 802.16e-2005 standard) and, consequently, not developed fixed WiMAX products. As a result, NSN logically selected Siemens's product line for fixed WiMAX and Nokia's platform for mobile WiMAX."

With Com definitely gone from Siemens's corporate structure, Nokia Siemens Networks is now part of a newly formed segment within the German corporation, called Strategic Equity Investments. There, NSN is cohabiting with Fujitsu Siemens Computers (a joint venture formed in 1999 to sell computer products in Europe) and Bosch und Siemens Hausgeräte, another joint venture specialising in household appliances. Which, by the way, means your microwave oven or washing machine, too, may prove to be that missing link between you and Siemens.

TARNISHED IMAGE

"Unfortunately, it has now become clear that our compliance measures [with internal conduct guidelines] are not yet sufficient. Several former and current company employees are under investigation regarding allegations of embezzlement, bribery and tax evasion."

Clearly, not the type of phrase any president and CEO would like to have to write in a letter addressed to shareholders. Yet this is exactly what Klaus Kleinfeld was forced to admit when Siemens published its latest Annual Report.

On 15 November 2006, Munich public prosecutors searched some of the company's premises and several private homes in Munich, Erlangen and Austria. They were acting in connection with an ongoing investigation of employees suspected of criminal offences. Arrest warrants were issued for several employees working for Siemens's now dissolved Communications business unit, including its former chief financial officer.

A parallel internal investigation carried out by Siemens identified – among other irregularities – "a multitude of payments made in connection with [a number of business consultancy contracts] over the course of approximately a seven-year period for which we have not been able to either establish a valid business purpose or clearly identify the recipient. These payments raise concerns under the legislation of the US, Germany and other countries," the document states.

Innovative Analog Components

Innovative Analog Components from the Leading Supplier of 8-Bit Microcontrollers

In response to ever increasing requirements to minimise power, space and noise, and maximise accuracy in embedded system designs, Microchip has integrated its CMOS design and manufacturing expertise into a broad range of analog and interface components.

The products include a large family of operational amplifiers and comparators, alongside Microchip's innovative Programmable Gain Amplifiers (PGAs); power management and conversion devices; thermal measurement and management devices; mixed signal products and interface devices.

Key attributes across the product families include low power operation and standby capabilities, high accuracy and low noise operation, wide operating voltage and temperature ranges, tiny packaging options and innovative design features.

Key Product Families:

- Temperature Sensors
- Voltage Regulators
- Charge Pumps and Switching Regulators
- System Supervisors
- Power MOSFET Drivers
- Battery Chargers
- Operational Amplifiers
- Programmable Gain Amplifiers
- Comparators
- A/D Converters
- D/A Converters
- Digital Potentiometers
- CAN Interfacing Products
- Infrared Interfacing Products

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HOW DO YOU USE multiple channel radios?

by Myk Dormer

If you browse the catalogues of any of the major telemetry module suppliers, you will become familiar with the two main classes of conventional radio module: the inexpensive, short range, high data-rate, wideband units, and the far longer ranged, but lower speed, narrowband types.

But, closer inspection will show a few of the wideband – and a higher proportion of the narrowband units – offer multiple channel operation. It's obvious what this facility is (the ability of the radio to operate on one of a range of pre-programmed channel frequencies, usually generated by a phase locked frequency synthesiser), but the implications and potential uses of multiple channel radio deserve examination.

Multiple channel units do not require custom channel crystals (or resonators) to be sources, and there is no need to keep stock of frequency variants for a given band. By selecting (manually or automatically) an unoccupied channel, in-band interferers which would otherwise jam a single channel link can be avoided.

Several links can operate simultaneously in the same area (within mutual interference limits set by the adjacent channel, blocking and intermodulation performance of the receivers).

In making good use of the multi-channel function, there are a number of choices:

• **Factory set-up of operating channel frequency to customer order.** The radio is treated as a single channel unit by the end user, but the channel is programmed according to the customer order, at final test or goods dispatch.

• **Manual channel selection.** The user sets the operating channel (either by means of a physical switch on the unit, or by sending a command to the radio's serial port from an external controller, which is usually a simple set-up program running on a laptop or PDA). This gives the user absolute control over the operating channel of each unit, but requires him to adhere to a consistent band plan and, if possible, conduct a simple survey of occupied channels at installation.

• **Automatic channel selection.** This simple-sounding option requires the application's processor to command the radio module to operate on a given channel at power-on. This is the tip of a very large iceberg: At its simplest this can be an automation of the manual selection process, with a channel being selected according to the identity of the unit communi-cated with. More sophisticated techniques include forms of unoccupied channel detection and interference avoidance (see **Note 1**), right up to true frequency hopping methods, which usually require specifically designed radio hardware.

For the user, the choice must be made between the low cost of a single channel unit and the higher cost (and usually greater size) of the more capable and sophisticated multiple channel module.

Note 1: Some examples of automatic channel select algorithms. All have their strengths and weaknesses.

a) Band scanning. The master/controller conducts a scan of the signal level (by monitoring the RSSI level of the receiver) in each available channel in turn, on power-up or reset. It then selects an unoccupied channel, changes frequency to it and commences to transmit.

The slave/remote unit(s) scan the available channels on power-up, looking for a valid transmit burst from the master on each channel. When found, the remote remains on that channel. If no master transmissions have been received within a given time-out

“Multiple channel units do not require custom channel crystals (or resonators) to be sources, and there is no need to keep stock of frequency variants for a given band”

period, the remote repeats the scan process.

This method is best used in high reliability control systems, where a constant master transmission is allowable, i.e. industrial machine controllers. It requires a transceiver in the master unit, but receives only in the slaves. During scan periods, the slave unit must enter a fail safe/stop mode.

b) Command channel. As in method (a) the master/controller begins with a band scan. It identifies a usable channel. It transmits an 'acquire' command burst, which includes the selected operating channel, on a pre-determined command channel before moving frequency to the operating channel and listening for an 'acknowledge' burst from the remote. After a given time-out period without a valid 'acknowledge' burst, the master restarts the process.

The slave/remote unit listens on the command channel until an 'acquire' burst is received, then moves to the operating channel and transmits an 'acknowledge'. From this point on, the master and slave alternately exchange command and acknowledge bursts. In the event of either unit failing to receive a burst within its time-out period, the entire process is repeated.

This method requires transceivers at both command and remote ends and can only synchronise one remote to the master. If the acquire burst duty cycle is kept short, then multiple systems can use the same command channel and the system gives positive indication of signal reception by the remote. Unfortunately, a fixed interferer on the command channel will disable the system.

c) Semi-automatic band scan. In this method the remote (receiving) unit conducts a band scan on reception of a user command, which is a specific 'reset' button, or on power-up. It then outputs the identity of a suitable, unoccupied channel via a secondary bi-directional data link (a serial cable or an infra-red link) to the controller (transmitting) device. After a successful 'handshake' between the units, both change frequency to the new channel.

This method is an automation of the user site survey process and requires only minimal additional hardware. It requires manual intervention in the event of a new interferer appearing in band.

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd
www.radiometrix.com

IN THIS ISSUE WE ARE STARTING A SHORT SERIES ON ETHERNET AND RAPIDI/O INTERCONNECT TECHNOLOGIES: TYPES, TECHNICAL COMPARISONS AND OVERVIEW, PRACTICALITIES AND DESIGN CONSIDERATIONS. IN THIS FIRST ARTICLE, GREG SHIPPEN, SYSTEM ARCHITECT FOR FREESCALE SEMICONDUCTOR'S DIGITAL SYSTEMS DIVISION, AND A MEMBER OF THE RAPIDI/O TRADE ASSOCIATION'S TECHNICAL WORKING GROUP AND STEERING COMMITTEE, EXPLAINS HOW TO GO ABOUT CREATING AN EFFICIENT SYSTEM-LEVEL INTERCONNECT FABRIC

IMPLEMENTING AN EFFICIENT SYSTEM-LEVEL INTERCONNECT FABRIC

The rising complexity of many of today's networking and communications systems has led to a corresponding increase in the variety of interconnects to bind them together in an efficient manner. Data pipelines extend between ICs, boards and chasses out to the LAN and worldwide networks, with each step in the overall system-level fabric requiring an interconnect protocol to manage and protect the transfer of data.

In order to act upon data, each stage in the pipeline must either terminate or encapsulate protocols as data passes the boundary into new systems or subsystems (see **Figure 1**). Ethernet, for example, introduces many layers and protocols as data passes through the network. At each stage in the network, the encapsulated data from the previous stage is the raw data payload for the current stage. This architectural model is similar for even simple embedded communications systems.

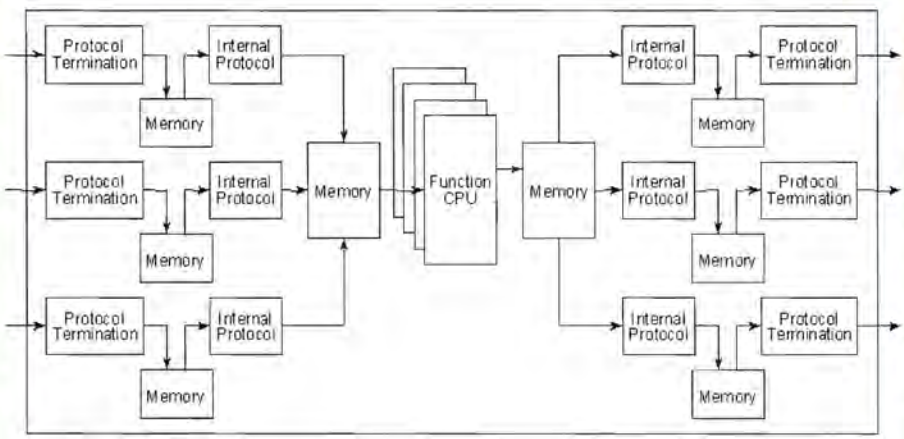

Figure 1: *Each stage in the data pipeline must either terminate or encapsulate protocols as data passes the boundary into new systems. Each protocol that has to be resolved, however, must be temporarily stored in memory and processed multiple times, leading to increased processing load and latency*

As systems grow in complexity and connectivity, so does the impact of interconnect on performance and cost. Even a single-board design to a large degree resembles a typical enterprise network, just with different protocols serving between the various sub-systems. As Moore's Law drives the speed and complexity of the silicon processing data in these systems, interconnects can become a bottleneck, at all stages. Furthermore, the wide variety of interconnect technologies and layers that

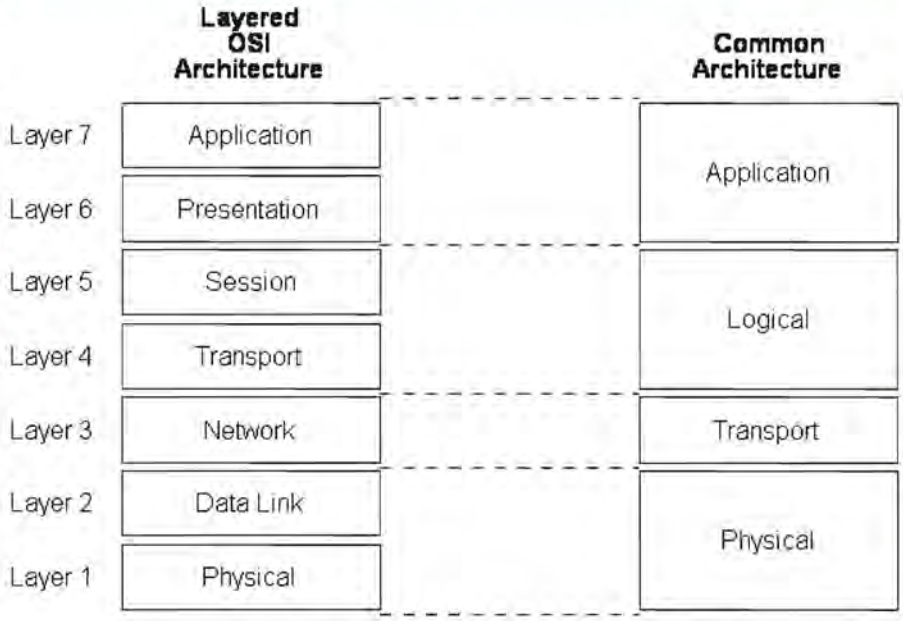

Figure 2: *The different ways in which a protocol is partitioned between layers has an impact on performance, flexibility and efficiency. This figure shows the partitioning of Ethernet, based on the layered OSI architecture, compared to RapidIO's common architecture approach*

must be supported significantly increases engineering complexity and cost. And clearly, inefficiencies at each interconnect stage reduce the actual achievable throughput of the data pipeline and, thus, the performance of the overall system.

One way of avoiding bottlenecks and bringing more benefits to the system or project is to select industry standards. They can reduce costs, encourage competitiveness and lower the number of different interconnects within a system through consolidation. For example, an interconnect that is flexible enough to provide both IC-to-IC and board-to-board interconnections can remove an entire layer of protocols and associated processing, memory and latency within the data pipeline.

Fortunately for developers, there are a good number of standard interconnects available. Some of the first such standards to be introduced and utilised include 10/100Mbps Etherent, TDM and VME. More recently, many other standards, including CSIX, HyperTransport, Infiniband, PCI Express, RapidIO and SPI4-2, have achieved a critical momentum of general industry support. Each of these has been intentionally designed to meet the specific requirements of particular applications.

Looking Beyond

Developers, however, have to be wary of attempting to extend a standard interconnect technology too far as the farther it stretches from its original scope of service, the more generalised and flexible it must be to meet the feature requirements at different stages in the pipeline. Generalisation tends to lead to inefficiency, which reduces the effectiveness of an interconnect. Here, Ethernet is a good example. In order to adequately service the vast number of endpoints present in the LAN, Ethernet has to support a larger ID field than is required for chassis and board-level communications. As a consequence, this reduces the efficiency of Ethernet for these types of interconnect.

Generalisation also affects the types of optimised services and features a standard interconnect offers. For example, IC-to-IC communications often involve transfers of data that are more efficiently handled as read or write transactions. At the LAN level, transfers of data are more efficiently handled as simple packet handoffs. Making read and write transactions part of the interconnect standard increases efficiency at the IC-to-IC stage of the data pipeline because they more compactly represent common transaction types. These same transactions, however, are rarely used at the LAN level and, so, making them part of the interconnect standard actually introduces inefficiencies with every transaction. Conversely, if read and write transactions are not part of the standard, LAN transactions are more efficient but only at the expense of every IC-to-IC communication.

For reasons such as this, it simply isn't feasible to attempt to stretch the capabilities of a single interconnect across an entire system. At some point, the benefits of eliminating another layer of interconnect are outweighed by the overhead required to accommodate all of the features and services that must be implemented in a less efficient way. For example, Ethernet can support read and write transactions but only at the expense of introducing RDMA, a whole new protocol layer.

System-Level Interconnect Requirements

Overall, a system-level interconnect technology must be balanced for the data pipeline stages it supports, since each stage in the system-level fabric involves a different subset of requirements. When selecting a standard upon which to base a system-level fabric, developers must balance the relative importance of each of these requirements for a particular application and choose the technology that provides the best balance of efficiency, cost and reliability.

DATA PLANE AND CONTROL PLANE REQUIREMENTS:

Typically, networking and communications systems utilise two distinct system architectures and fabrics. The data plane transfers data across high bandwidth pipelines from a remote source to a remote destination. Typically, a data plane must carry traffic with some degree of Quality of Service (QoS) and minimum bandwidth guarantees. It must also be able to sustain high bandwidth while minimising packet loss, latency jitter and end-to-end latency.

For carrier-grade applications, mechanisms must be in place to control congestion and partition available bandwidth on a fine-grained basis. Common data plane services include data streaming, remote DMA, encapsulation and traffic management. In contrast, control plane traffic is processor-oriented and often directed between dedicated compute resources performing complicated system-level control and management algorithms, making low latency and guaranteed delivery key requirements.

Many control plane interconnects are derived from processor front-side or I/O buses designed to carry a combination of processor, memory and I/O traffic utilising usage paradigms, such as address-based read/write transactions and messaging to minimise processor overhead. Robust error detection and correction are essential to reduce the impact of soft errors and packet loss. Common control plane services also include distributed computing functions and multicasting.

In order to simplify design and minimise system cost, developers would ideally like to use a single interconnect to move both control and data plane traffic. Such an interconnect must provide guaranteed delivery with low latency for control traffic and efficient transport with QoS and minimum bandwidth guarantees for data traffic without either plane disrupting the reliability of the other.

LOGICAL LAYER REQUIREMENTS

System-wide transaction ordering policies implemented at the logical layer (Ethernet layers 4 and 5) are determined by application-layer requirements and affect both overall performance and compatibility with existing software. Strict ordering, where transactions must occur in sequence, is compatible with most software mechanisms. As ordering rules become looser and less strict, opportunities to reorder traffic arise, leading to increased performance. Consider that a read operation is expected to reflect updates from previous write transactions. For a fabric employing strict ordering, a read request cannot pass earlier writes but must instead push them ahead. However, there is no real need to hold back a read request that is independent of previous writes.

Reordering, such as is supported by RapidIO, enables independent requests to pass each other as well as grouping of unassociated but similar transactions (i.e. to the same block of memory) to improve channel efficiency. Transactions are independent when they deal with different blocks of data or when multiple but independent entities are utilising the same interconnect. Thus, strict ordering rules imposed on a fabric can reduce performance while increasing protocol complexity. Ethernet, for example, requires large buffers and increased latency tolerance in order to be able to reorder packets while a dropped packet is being resent.

TRANSPORT LAYER REQUIREMENTS:

The transport layer defines how endpoints are addressed as well as how packets are routed across the fabric. A point-to-point interconnect must be able to address the appropriate number of nodes, use destination-based routing and simplify the underlying switching architecture.

For a chassis-based interconnect, support for up to thousands of nodes offers the best trade-off between header overhead and addressable space, whereas a LAN-based interconnect requires support for millions of nodes. Extending a chassis-based interconnect up to the LAN requires modifications to source and destination headers. Extending a LAN-based interconnect such as Ethernet down to the chassis or board level, on the other hand, introduces inefficiencies since source and destination headers are larger than they need to be and cannot be reduced in size.

Destination-based routing is often implemented as lookup tables at switching elements. The alternative to destination-based routing is path-based routing, where the desired route is carried in the packet header. Path-based routing requires that all endpoints know the system topology, a difficult requirement to maintain in systems that support hot-insertion or extraction. Consider that hot-inserting a switch in a path-based network would require changes to every endpoint of the system rather than just adjacent switches as is the case with destination-based routing.

To connect more than two endpoints, shared bus interconnects require little more than additional copper on the board while implementing such connectivity in a point-to-point interconnect requires a low-cost switch device. Key to controlling interconnect cost is avoiding involved header parsing and excessive modification as packet pass through the switch.

Another important consideration is how dropped packets are handled. Certainly, real-time data such as voice and video can suffer some data loss without overtly affecting quality. However, the possibility of the loss of a control plane message must be accommodated by long upper-layer timeouts that can introduce unacceptable control-loop latencies impacting QoS and system availability. Ideally, correcting for packet loss should be implemented in hardware rather than in software stacks which inject considerable latency.

This introduces challenges for Ethernet as a system-level interconnect since Ethernet requires higher layer protocols to harden its best-effort transport mechanisms to guarantee delivery of control data as well as manage its latency. This increases both protocol complexity and latency, effectively cutting into the efficiencies gained by collapsing the data and control plane into a single fabric. Protocols such as RapidIO avoid these inefficiencies and undesirable latency by managing packet loss directly in hardware.

PHYSICAL LAYER REQUIREMENTS

The physical layer defines how data payloads are transported from one link to another, providing the link protocol as well as the signalling used over the electrical channel. A key consideration in the cost of a physical layer implementation is the maximum length the channel needs to support; transporting a 1Gbps stream over hundreds of meters of unshielded cable requires a different approach than that same stream passing over a one meter backplane.

For most networking equipment, the physical channel across a standard rack-mounted backplane is typically less than 100cm and up to 10m to span chasses. One of the disadvantages of extending Ethernet as a chassis and board interconnect is that Ethernet is speced for more than 100m and, since Ethernet cabling assumes bundling with many other similar pairs, it must tolerate more crosstalk, resulting in significantly higher PHY complexity than is actually required for backplane applications.

In order to minimise the number of signals required, the physical layer often utilises a serialised embedded clock signalling scheme with a differential pair in each direction. For the most flexibility, scaling data rate can be achieved by increasing or decreasing individual lane rates as well as increasing the number of lanes supported. Flexibility to reduce lane rate by a relatively small amount is also desirable as the ability to do so late in the development cycle can sometimes enable a system to ship even though the physical channel comes up short of the anticipated design margin.

Finally, as lane rates stretch the limitations of electrical signalling technology, minimising bit error rates becomes increasing difficult. Hardware support for link-level error correction becomes a necessity in order to guarantee packet delivery and maintain QoS.

QUALITY OF SERVICE REQUIREMENTS

As real-time multimedia services continue to proliferate, QoS mechanisms must be in place to guarantee minimum bandwidth with low end-to-end latency and jitter. To provide these capabilities, an interconnect protocol must be able to identify individual traffic streams between two endpoints, provide differentiated levels of service on a stream-by-stream basis and control congestion across the fabric. Complicating identification of individual traffic streams is the fact that many endpoints aggregate multiple traffic flows so mechanisms must be in place to identify individual flows within streams as well.

The ability to guarantee bandwidth is closely tied to effective flow control mechanisms since the existence of a bandwidth guarantee for one stream implies that other streams have the potential to be held up. Over provisioning a fabric – providing more bandwidth than is actually allocated – can alleviate many congestion problems but significantly increases system cost and still does not completely eliminate congestion when multiple traffic flows converge on a single link or if head-of-line blocking occurs.

Given that congestion is a dynamic phenomenon lasting from nanoseconds to milliseconds, a fabric interconnect must support a hierarchy of flow control methods. Flow control loop latency between the detection of congestion and corrective action must be faster than the event attempting to be controlled, necessitating very tight flow control loops. For longer congestion events, flow control methods must range from link level to end-to-end across the fabric. The most effective flow control anticipates congestion and proactively controls traffic flow at entry points. Mechanisms that are invoked only after congestion negatively affects network performance are the least effective.

HIGH AVAILABILITY REQUIREMENTS

Many networking and communications applications must continue operation even in the presence of failures. To provide high availability of this nature, fabrics must have no single point of failure, provide robust fault detection at the link level and from end-to-end, enable hot swapping of interconnect and other system components and support full error recovery, isolation and containment with logging and notification.

All layers of the protocol must contribute to failure detection, including supporting link-level error checking and correction, detection of errors in data payload and control messages, recovery from lost response transactions and offering logical layer end-to-end transaction timeouts. Because soft errors should be the most common error event, highly available fabrics must be able to correct and recover from soft errors.

Extending Standard Interconnects

One significant advantage of standard interconnect technologies is that they have been designed to efficiently serve across multiple data pipeline stages. Proprietary implementations on the other hand are typically optimised for a single stage. Attempting to utilise these proprietary interconnects elsewhere typically involves significant reengineering, as well as substantial performance losses and increased product cost.

Ethernet, for example, was originally designed to connect a large number of endpoints, typically computer workstations, with a flexible and extensible architecture. As a consequence, Ethernet utilises a simple header and support for a single transaction type. Because endpoints could be expected to possess significant processing resources, a relatively large software stack is required to manage protocol processing; hardware is only required to identify packet boundaries. In high-speed embedded applications, however, the choice of this particular hardware/software trade-off imposes formidable performance bottlenecks for board-to-board and chassis-to-chassis interconnections. For example, at 1Gbps and 10Gbps, Ethernet implementations must employ TCP/IP Offload Engines (TOEs) to reduce the protocol processing load on the main application processor. Unfortunately, there is no standard for implementing TOEs, forcing developers to take what are effectively proprietary approaches.

In comparison, RapidIO was originally designed to serve as a next-generation front-side bus for high-speed embedded processors. Its designers, however, recognised early on in the specification process that a front-side bus that could also function as a system-level interconnect would be of more value to developers. As a result, RapidIO took a different approach than Ethernet, focusing rather on embedded in-the-box and chassis control plane applications that required reliability with minimal latency, limited software impact, protocol extensibility and simplified switching.

To further improve its efficiency, protocol processing takes place in hardware and directly supports common features required for these interconnects layers, including read/write operations, messaging, data streaming, QoS, data plane extensions and protocol encapsulation, all while achieving effective data rates from 667Mbps to 30Gbps. In this way RapidIO has to stretch less, so to speak, than Ethernet to act as a viable system-level interconnect. As a result, RapidIO can consolidate more levels of interconnect more efficiently and reliably than Ethernet.

Balancing Requirements

Today's complex systems bring together many subsystems that need an efficient fabric to interconnect them. In order to control cost, developers need to seek ways to reduce the number of interconnect protocols in use by consolidating layers where possible. While the most prominent standards – those with the largest markets – might seem to be the best choice, developers need to delve deeper to compare the capabilities of each interconnect standard with the specific needs of the application at hand. For example, the majority of Ethernet's volume is in the LAN and neither these cost economies nor capabilities carry forward as Ethernet stretches down to the board and chassis levels in high-performance embedded applications.

Merging interconnect layers merges both capabilities and requirements. By understanding the underlying requirements of each interconnect layer in a system, developers can make informed decisions about which interconnect technology will offer the best performance, cost-efficiency and reliability for their applications. For more information visit **www.RapidIO.org**

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IN LIGHT WE BELIEVE

K. FAWZI IBRAHIM, A SENIOR LECTURER AT THE COLLEGE OF NORTH WEST LONDON AND DIRECTOR OF KFI TRAINING AND CONSULTANCY, HERE PRESENTS A SERIES OF ARTICLES BASED ON HIS FORTHCOMING 4TH EDITION OF NEWNES GUIDE TO TELEVISION AND VIDEO TECHNOLOGY. IN THE FIRST ARTICLE SEEN HERE, HE DESCRIBES THE CONSTRUCTION AND OPERATION OF A DIGITAL LIGHT PROCESSING SYSTEM

Plasma and LCD television receivers have long enjoyed the singular billing as the "Big Thing" in consumer electronics. Recently, other new display technologies have begun to make some headlines of their own, among them Digital Light Processing (DLP).

DLP is a video projection technology that has recently been available as rear projection large screen domestic television receivers. The technology took decades to become a viable technology for the ever expanding consumer market. It was developed by Larry Hornbeck at Texas Instruments (TI) in the 1970s, perfected in the 80s and finally introduced to the public in 1996. Since then, DLP TV has started making waves in the fixed pixel display market by meeting the surging demand for less expensive, but no less capable, large-screen TVs.

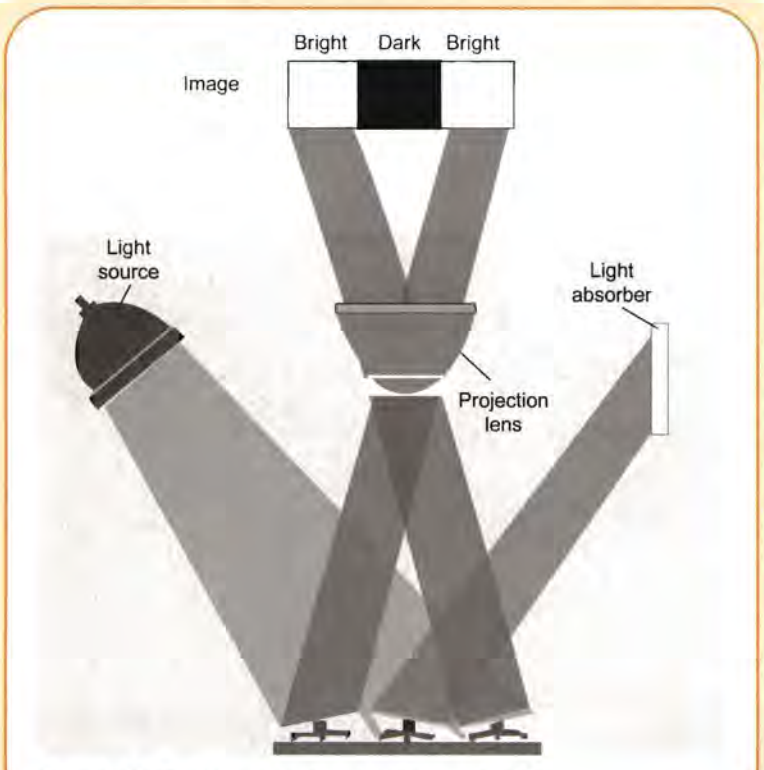

Figure 1: *The component parts of a simple DLP*

DLP DISPLAY

Central to the DLP display is the Digital Micromirror Device (DMD) developed by TI. The DMD is a thumbnail-size semiconductor light switch. It consists of an array of millions of microscopic-sized mirrors, each mounted on a hinge structure so that it can be individually tilted back and forth. **Figure 1** shows the basic components of a simple DLP system composed of a light source and a projection lens.

Light from the lamp is reflected off the micro-mirrors and directed towards the projector lens if the mirror is tilted in one direction and away from the lens, and towards a light absorber if tilted the opposite way. In the diagram, the two end-mirrors are tilted so that the reflected light goes through the lens to be projected on an external surface as two bright square dots. These two mirrors are said to be 'on'.

The middle mirror is tilted in the opposite direction and its reflection avoids the lens to be absorbed by a light absorber. It is said to be 'off'. The absence of light reflection from the middle mirror appears as a dark square dot on the screen. The top view of the micromirrors is shown in **Figure 2**.

Now imagine thousands of these tiny micro-mirrors, arranged in a matrix. The result is an image with a resolution determined by the number of micromirrors with each micromirror corresponding to one pixel. Thus a VGA-resolution image requires DMD matrix of 640 x 480, an XGA a matrix of 1024 x 768, and so on. To produce a moving image, the micromirrors have to be addressed and set to one position or the other and refreshed every frame.

Figure 2: Top view of the micromirrors shown in Figure 1

GREYSCALE GENERATION

The simple operation described here does not provide for shades of grey as the operation of the micromirrors is purely digital. A mirror can only be turned 'on' for full brightness or 'off' for no brightness or black. To produce greyscale, light has to be modulated using a technique known as binary-weighted pulse width modulation (PWM).

In the binary-weighted PWM the frame period is divided into a number of binary-weighted intervals or bit intervals. The weighting for each interval reflects the binary code of the pixel value, a technique known as bit plane weighting in which the pixel's least significant bit (LSB) consumes 1/(2n-1) and the LSB+1 bit consumes double that, and so on, where n is the number of bits used to describe the luminance or value of the pixel.

The most significant bit (MSB) consumes (n-1)/(2n-1) of the frame interval. The human eye integrates the pulsed light to an average intensity. The greyscale perceived is proportional to the proportion of time the mirror is 'on' during the frame refresh cycle. The MSB addresses (i.e. tilts and holds) the mirror in position for 'half' (128/255) the frame period, 10.04ms for PAL and 8.38ms for NTSC. The MSB-1 bit addresses the mirror for a 'quarter' (64/255) of the frame period and so on up to the LSB which addresses the mirror for the smallest bit interval, or 1/255th.

A pixel value bit of 1 would turn the mirror 'on' and a 0 would tilt the mirror in the opposite 'off' position. For maximum light intensity, the pixel value would be 11111111 (all 1s) which sets the micromirror 'on' throughout the frame period. For minimum intensity or black, all bits would be 0 and the micromirror would be 'off' throughout the frame. Other combinations of 0s and 1s would produce different shades of grey, a total of 28 = 256.

Figure 3 shows a typical binary-weighted PWM frame period for an 8-bit pixel value, depicting the bit intervals, as well as the 'on' and 'off' sequence for two different light intensities, 60% and 35.5%.

Current DLP systems are either 24-bit colour (8 bits giving 256 grey levels per primary colour) or 30-bit colour (10 bits giving 1024 grey levels per primary

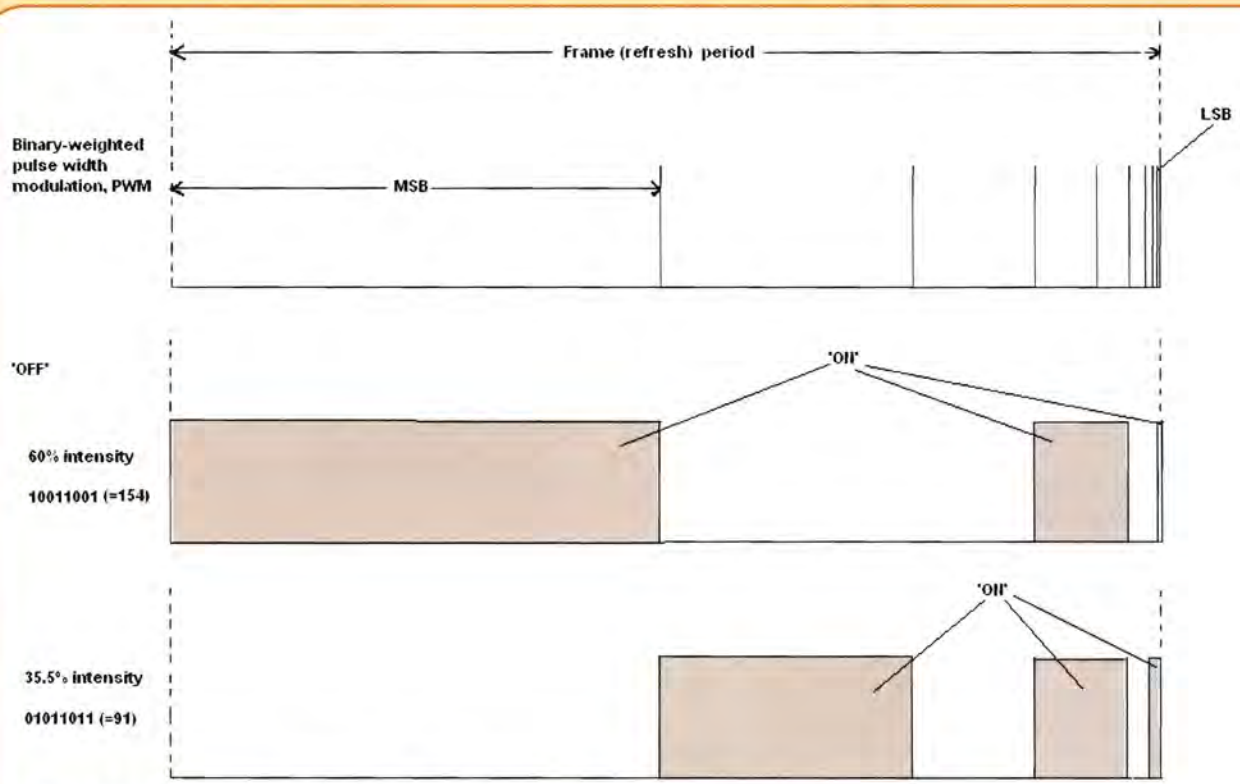

Figure 3: Binary-weighted pulse width modulation

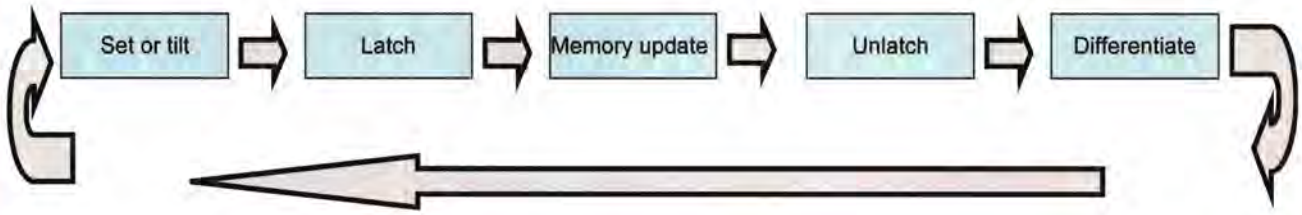

Figure 4: *Addressing the DMD*

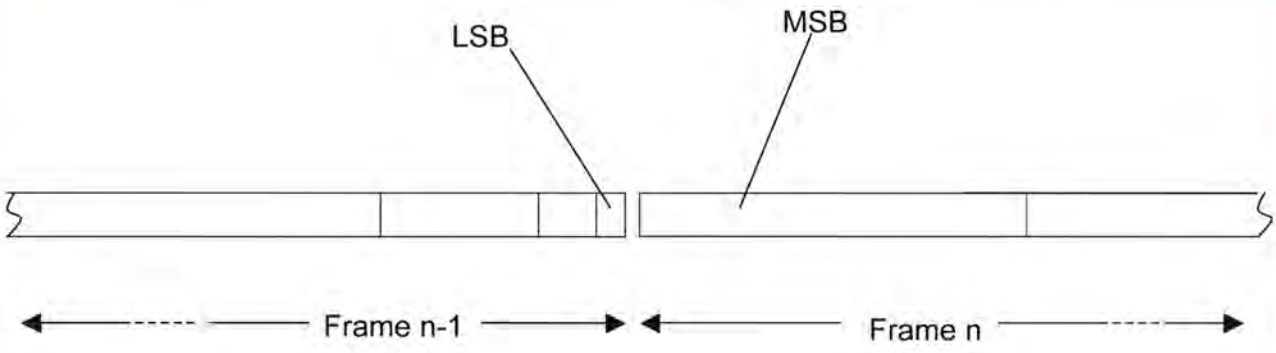

Figure 5: *Traditional addressing*

colour). In the simple binary PWM addressing, spatial and temporal artefacts can be produced because of imperfect integration of the pulsed light by the viewer's eye. These artefacts can be reduced to negligible levels by what is known as "bit-splitting". In this technique, the longer duration bits are subdivided into shorter durations and these split bits are distributed throughout the video frame time. DLP displays combine pulse width modulation and bit-splitting to produce analogue-quality projection systems.

DMD DRIVE

At the beginning of each frame, the value of each pixel is fed, bit by bit, into the corresponding SRAM cell starting with the MSB. All mirrors remain in the MSB state for half of a frame time. The next most significant bit is then loaded and held for one quarter and the bit after that for one eight of a frame time, and so on until all the bits have been loaded. The process is then repeated for the next frame.

The logic state of a bit in an SRAM cell is fed to an embedded driver to create an electrostatic torque between the mirrors and address electrodes. This works against the restoring torque of the hinges producing a rotation of the yoke and mirror in the positive or negative directions, depending whether the content of the cell is a 1 or a 0. The mirror and yoke rotate until the yoke comes to rest (or lands) against mechanical stops that are at the same potential as the yoke. Because geometry determines the rotation angle, as opposed to a balance of electrostatic torques, the rotation angle is precisely determined.

Once the memory array has been updated, all the mirrors in the array are released simultaneously and allowed to move to their new positions by a bias address voltage. They stay latched in that position by applying a higher bias latch voltage. This prevents the mirrors from responding to changes in the memory while the memory is being written with updated video data. While the mirrors are latched, the memory cells are updated with new data.

DMD ADDRESSING CYCLE

The DMD addressing scheme takes advantage of the "mechanical latching" feature of the DMD. If a bias (latch) voltage in excess of the address voltage is applied to the array of DMD mirrors after the 1 or 0 address voltages are set, the mirrors will stay latched (tilted) in the selected state, even if the address voltage changes. Only if the bias (latch) voltage is removed will the mirrors be free to respond to any changes in the address voltage.

The complete address cycle is shown in **Figure 4**. The mirrors are set or tilted into position determined by the contents of their corresponding cells and stay in that position for the bit interval. To keep them into that position, a bias (latch) voltage is applied. While the mirrors of the array are latched, the underlying memory array is refreshed or updated by the next bit of the pixel value for the next bit interval. At the end of the bit interval, the latch bias is turned off to release mirrors allowing them to rotate, if necessary. However, the stickiness of the mirrors keeps them in position.

The next phase, the differentiation phase, is to identify which mirrors are to remain in the same state and which are to cross over to a new state for the next bit interval. The latter are then released by applying a retarding field to the yokes and mirrors.

Having done that, the rotationally separated mirrors are set by applying an address bias voltage and rotate them to their new states. The others remain in their previous states. A bias latch voltage is then applied and so on.

MULTIPLEXED ADDRESSING

The traditional addressing technique described above suffers from two drawbacks. The first is a result of the manner in which the SRAM chip is refreshed and the other is the relatively low throughput of the manufacturing process. In the traditional addressing technique, the MSB of a new frame must be loaded into the DMD SRAM during the LSB bit interval of the preceding frame as shown in **Figure 5**. As the LSB bit interval is the shortest interval in a frame, the bit rate associated with loading the MSB is at a peak. The lowest bit rate is when the MSB-1 data is loaded during the long MSB bit interval. The DMD device and its drivers must therefore have high bandwidths to cope with the highest bit rate even though the data rate is essentially zero throughout the 50% of the frame time represented by the MSB time period and the average bit rate is relatively low. The second drawback is the difficulty in achieving defect-free SRAM substrate reducing the manufacturing throughput. DMD throughput would be improved if the SRAM cell count is reduced below the pixel counts, i.e. if one cell can service more than one pixel. To increase throughput and improve the bandwidth requirements multiplex addressing was developed.

In the traditional addressing technique, the mirrors share a single bias voltage which is applied to all the mirrors simultaneously. The mirrors are latched, released and rotated simultaneously. In multiplex addressing, the DMD mirror array is divided into a number of separate sections, normally 16, each with its own separate source of bias voltage. The mirrors are addressed section by section. In this way, 16 mirrors, one from each section can be addressed by the same SRAM cell thus reducing the number of SRAM cells required.

GENERATING COLOUR

Colour DLP optical systems have been designed in a variety of configurations, distinguished by the number of DMD chips (one, two, or three) used. The one-chip and two-chip systems rely on a rotating colour disk to time-multiplex the colours.

The one-chip configuration is used for lower brightness applications and is the most compact. Two-chip systems yield higher brightness performance but are primarily intended to compensate for the colour deficiencies resulting from spectrally imbalanced lamps (e.g. the red deficiency in many metalhalide lamps). For the highest brightness applications, three-chip systems are required.

In the one-chip configuration (**Figure 6**), white light is focused onto a colour wheel filter system. The colour wheel spins shining a sequence of red, green and blue light onto the DMD mirrors to produce the red, green and blue frames, bit interval by bit interval. The DMD SRAM memory cells are thus fed with red, green and blue pixel values, bit by bit in the same sequence as the spinning colour. The eye integrates the sequential images and a full colour image is seen.

The data, as well as the mirrors' transition rates, are increased by three times as the DMD cells are refreshed by the full pixel depth three times for each video frame. This was made possible with improvements in the optical and mechanical switching times of the DMD. Single-chip DLP systems made small size projectors a possibility. The drawback is a reduced brightness level compared with the three-chip type.

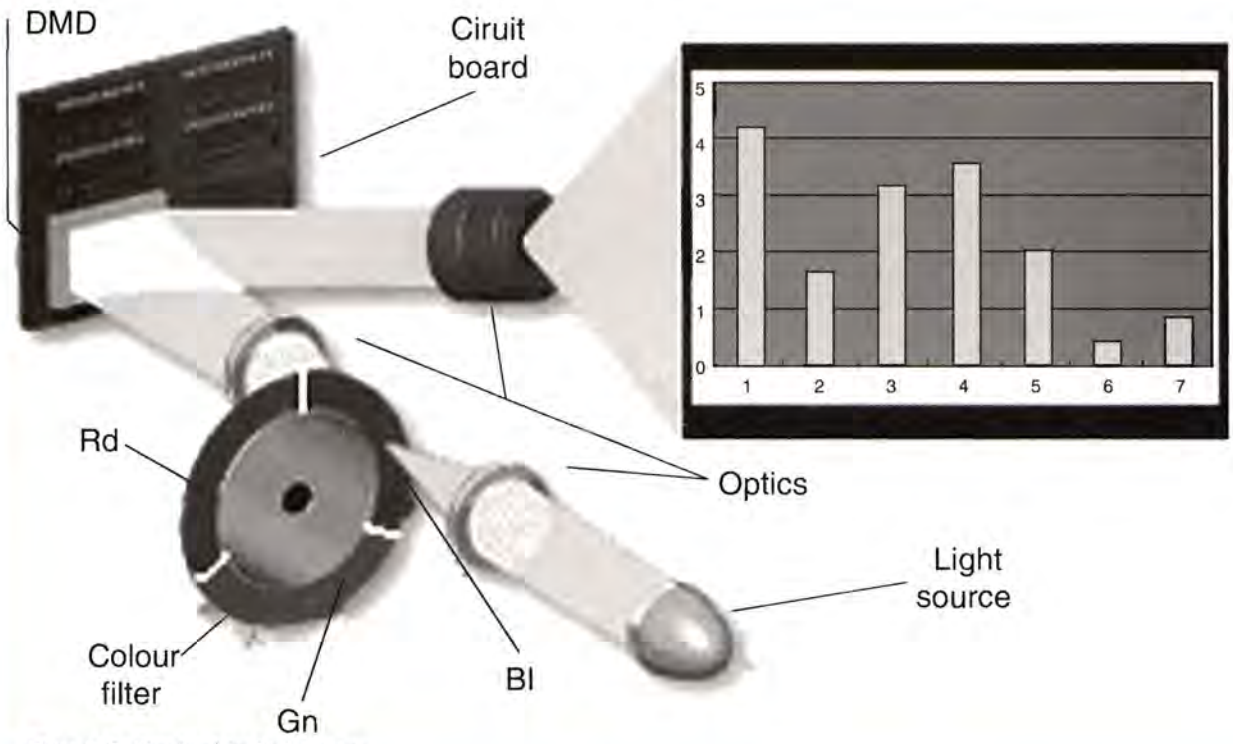

Figure 6: *Single-chip DLP system*

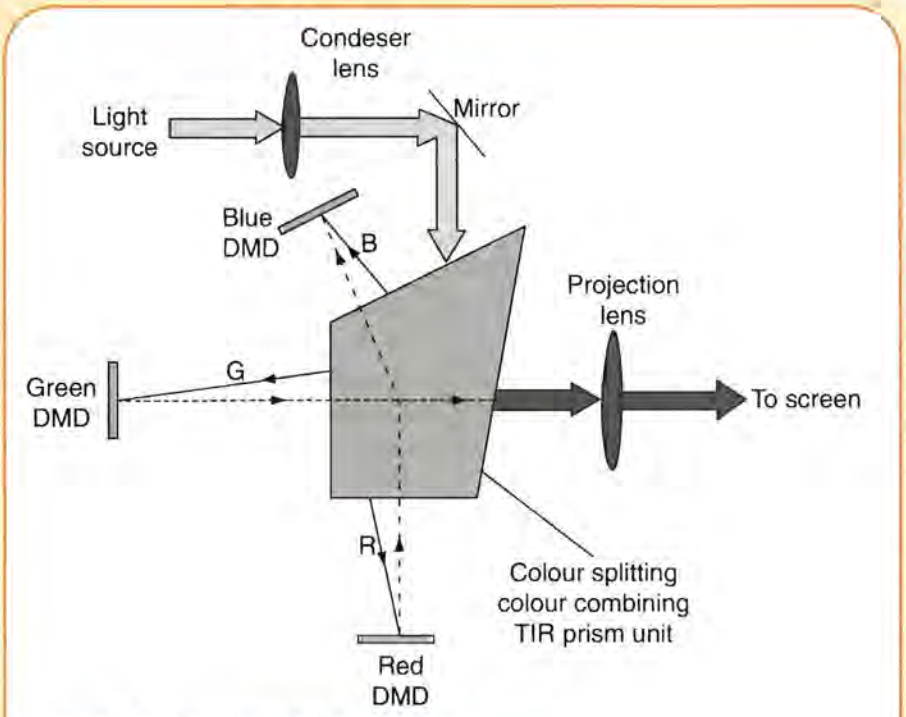

Figure 7: *An outline of a three-chip DLP system*

THE RAINBOW EFFECT

If there is one single issue that people point to as a weakness in DLP it is that the use of a spinning colour wheel to modulate the image has the potential to produce a unique visible artefact on the screen, commonly referred to as the 'rainbow effect'. This is simply due to colours separating out in distinct red, green and blue because of the sequential colour updating from the wheel. (Three-chip DLP projectors have no colour wheels and, thus, do not manifest this artefact). Basically, as the colour wheel spins the image on the screen is either red, or green, or blue at any given instant in time – and the technology relies upon your eyes not being able to detect the rapid changes from one to the other. Unfortunately some people can see it. Not only can some see the colours break out, but the rapid sequencing of colour is thought to be the culprit in reported cases of eyestrain and headaches. Since LCD projectors always deliver a constant red, green and blue image simultaneously, viewers of LCD projectors do not report these problems.

How big of a deal is this? It is different for different people. Most people cannot detect colour separation artefacts at all. However, for some who can see the rainbow effect, it is so distracting that it renders the picture literally unwatchable. Others report being able to see the rainbow artefacts on occasion, but find that they are not particularly annoying and do not inhibit the enjoyment of the viewing experience.

TI and the vendors who build DLP-based projectors have made strides in addressing this problem. The first generation DLP projectors incorporated a colour wheel that rotated sixty times per second, which can be designated as 60Hz, or 3600RPM. So with one red, green and blue panel in the wheel, updates on each colour happened 60 times per second. This baseline 60Hz rotation speed in the first generation products is known as a "1x" rotation speed.

Upon release of the first generation machines, it became apparent that quite a few people were seeing rainbow artefacts. So in the second generation DLP products the colour wheel rotation speed was doubled to 2x at 120Hz, or 7200RPM. The doubling of the colour refresh rate reduced the time between colour updates and, so, reduced or eliminated the visibility of colour separation artefacts for most people.

Today, as noted above, many DLP projectors being built for the home theatre market incorporate a six-segment colour wheel which has two sets of red, green and blue filters. This wheel still spins at 120Hz or 7200RPM, but because red, green and blue are refreshed twice in every rotation rather than once, the industry refers to this as a 4x rotation speed. This further doubling of the refresh rate has again reduced the number of people who can detect them.

For the large majority of users the six-segment, 4x speed wheels have solved the problem for home theatre or video products. Meanwhile, due to the higher lumen output requirements for business presentation use, most commercial DLP units still use the four-segment, 2x speed wheels.

THE THREE-CHIP DLP

In the three-chip configuration, three separate DMDs are used, one for each colour in the arrangement shown in **Figure 7**. Light from a metal halide or xenon lamp is collected by a condenser lens. The light must then be separated into its three primary components red, green and blue. This is carried out by a set of colour-splitting and colour-combining prisms. Furthermore, these light waves must be directed at 20 degrees relative to their DMD chip. This must be accomplished in a way that eliminates mechanical interference between the illuminating and projecting waves. This task is performed by a 'total internal reflection' (TIR) prism, which is interposed between the projection lens and the DMD colour-splitting/colour-combining prisms.

The colour-splitting/colour-combining prisms use dichroic filters deposited on their surfaces to split the light into red, green and blue components. A dichroic filter has significantly different properties at two different wavelengths that can be used to selectively pass light of a small range of colours only. The red and blue prisms require an additional reflection from a TIR surface of the prism in order to direct the light at the correct angle to the red and blue DMDs. Light reflected from the 'on' mirrors of the three DMDs is directed back through the prisms and the colour components are recombined. The combined light then passes through the TIR prism and into the projection lens.

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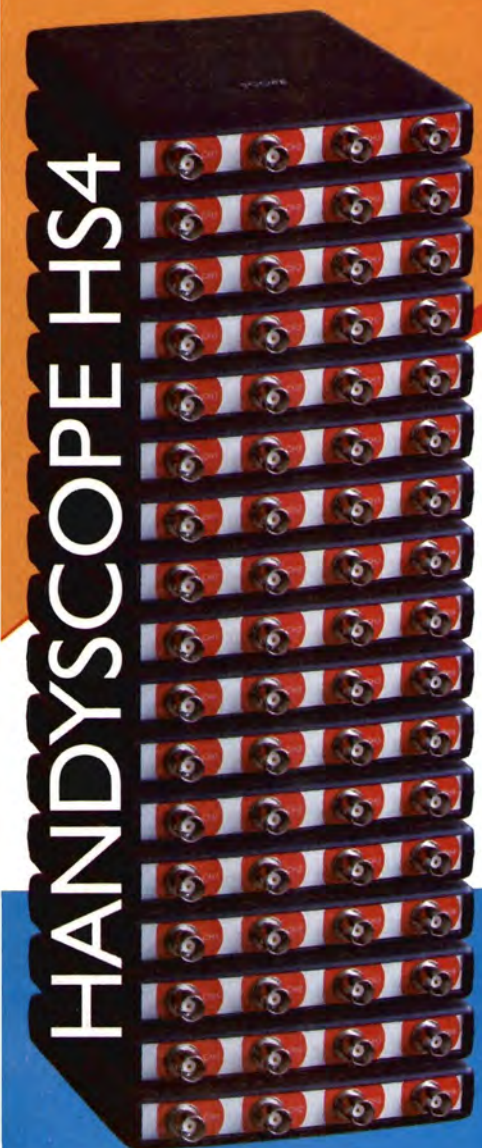

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Cambridgeshire, PE17 3WJ, UK
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SWITCHER EMI INSURANCE THROUGH FREQUENCY SPREADING

GREG ZIMMER, PRODUCT MARKETING ENGINEER WITH THE SIGNAL CONDITIONING GROUP AT LINEAR TECHNOLOGY,

DISCUSSES TECHNIQUES FOR MINIMISING ELECTROMAGNETIC INTERFERENCE IN THE INCREASINGLY USED SWITCHING REGULATORS

Switching regulators are steadily expanding into new applications, replacing linear regulators because they offer significant improvements in space and efficiency. One trade-off, however, is the potential for electromagnetic interference (EMI) due to the internal switching current. The resulting EMI has peak energy concentrated at the switching frequency and is traditionally minimised by careful attention to grounding, shielding and filtering. These EMI reduction techniques are focused on the control and containment of emissions generated by the switching currents inside the regulator. Reducing the amplitude of the switching current and modifying the frequency can also provide EMI improvements. Specifically, multiphase synchronisation and Spread Spectrum Frequency Modulation (SSFM) provide two powerful tools for EMI reduction.

Tremendous growth in the use of portable electronics has increased the potential for EMI between devices. EMI can be a nuisance, as in the case of noise in a television or radio receiver. EMI can impair electronic device operation, such as avionic equipment, which is why airlines ban the use of portable electronics during take-off and landing.

Underscoring the importance of this issue, government regulations have established EMI limits and test methods to ensure that products operate without experiencing interruptions and without interrupting other devices. Testing and tracking down EMI requires a lot of time and effort, so taking a proactive design approach to avoid last minute modifications and time-consuming retests is always a good idea.

Multiphase Synchronisation

Replacing a single switcher with multiple synchronised switchers can reduce peak switching current. This technique, known as multiphase synchronisation, is achieved by externally driving the switchers with a clock that has a phase shift placed between each regulator. This staggers the turn-on for each switcher such that there is input current where previously there was a dead band.

Figure 1 illustrates the supply current of two switching regulators operated with a single 200kHz clock. The figure on the left shows the current when no clock synchronisation is used. The figure on the right shows what happens when a 180° phase-shift is placed on the 2nd regulator clock. The result is smaller current peaks at twice the

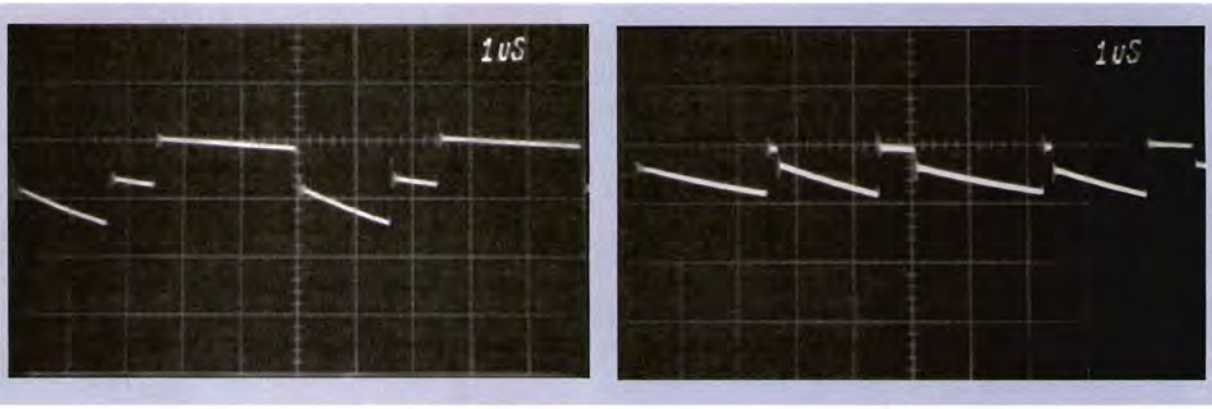

Figure 1: *Supply current for two switching regulators operated without and with phase synchronisation*

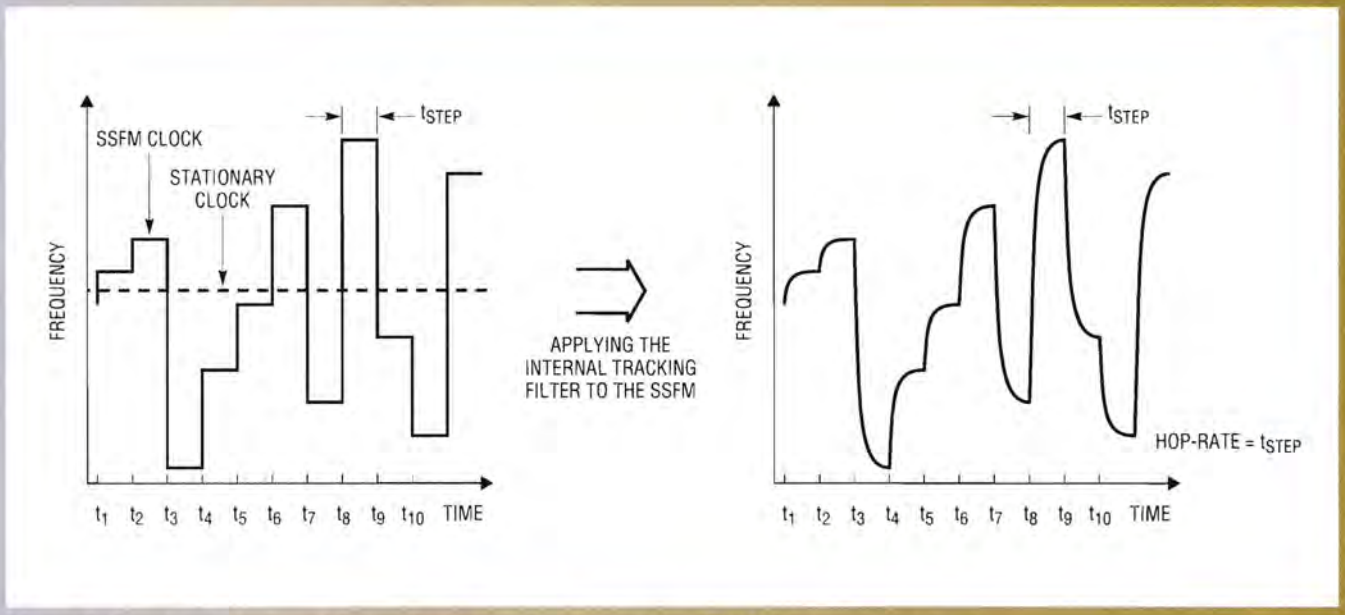

Figure 2: *Pseudo-random modulation illustrating the effect of the LTC6908 internal tracking filter*

frequency (400kHz) and, therefore, smaller peak EMI. Since EMI is now at twice the frequency, it is further reduced because filtering is more effective at higher frequencies.

By dividing the clock signal into more phase increments, additional regulators can be synchronised where each additional regulator provides diminishing EMI improvement. Many dual and multiphase regulators take advantage of multiphase synchronisation by including built-in clock phase shifting.

Using an external clock for multiphase synchronisation allows multiple dual or multiphase regulators to be synchronised and is also sometimes necessary when power requirements dictate the use of separate regulators. Silicon oscillators can be ideal for these applications since they can provide multiple outputs with programmable frequencies and phases.

It should be noted that multiphase synchronisation provides benefits well beyond EMI improvement. Using synchronised parallel regulators has a net effect of cancelling ripple currents on the input and output, allowing for a significant reduction in input and output capacitors. A multiphase solution has a smaller equivalent inductance and, therefore, can provide a higher current slew rate. A multiphase solution also has less switching time delay for a load transient. As a result of the improved load transient response, the needed output capacitance is further reduced.

Spread Spectrum Frequency Modulation

The most dramatic improvement to EMI may be achieved by continuously varying the switcher's clock frequency. The technique, referred to as SSFM, improves EMI by not allowing emitted energy to stay in any receiver's band for a significant length of time. The effectiveness of SSFM with switching regulators depends upon the frequency spreading amount, typically ±10%, and the modulation profile.

Most switchers exhibit ripple that varies with frequency; more ripple at lower switching frequencies and less at higher switching frequencies. As a result, a switcher's ripple will exhibit an amplitude modulation if the switching clock is frequency modulated. If the clock's modulating signal is periodic, such as a sine or triangle wave, there will be a periodic ripple modulation and a distinct spectral component at the modulating frequency. Since the modulating frequency is much lower than the switcher's clock, it may be difficult to filter out. This could lead to system problems such as audible tones or visible display artifacts do to supply noise coupling or limited power supply rejection of the downstream circuitry.

A pseudo-random frequency modulation can avoid this periodic ripple. Using this technique, the switching regulator clock shifts from one frequency to another in a pseudo-random fashion. Since the switcher's output ripple is amplitude-modulated by

Regulatory Agency EMI Test Bandwidths (per CISPR 16-1)	
Band A (9KHz to 150kHz):	BW = 220Hz
Band B (150kHz to 30MHz):	BW = 9kHz
Band C (30MHz to 1000MHz):	BW = 120kHz
Real World System Bandwidths	
Voice:	BW = 3kHz
GSM:	BW = 8kHz
AM Radio:	BW = 9kHz
Audio:	BW = 20kHz
FM Radio:	BW = 75kHz
TV:	BW = 6-8MHz

Table 1: *Real-world bandwidths*

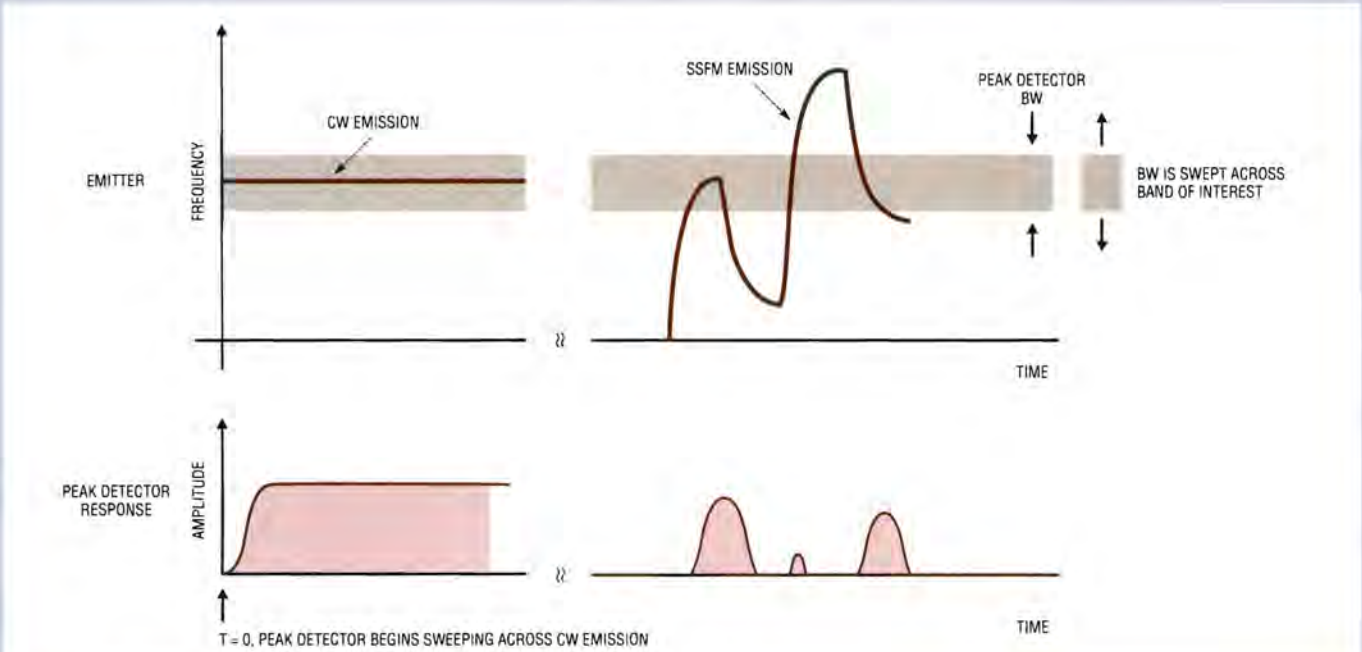

Figure 3: *Peak detector response from a CW emission and an SSFM emission*

a noise-like signal, the output looks as if there is no modulation and the downstream system implications are negligible. The higher the rate of frequency shifting, or the hop-rate, the less time the switcher is operating at a given frequency (see **Figure 2**) and the less time EMI will be "in-band" for a given receiver.

There is a limit, however, to the rate of frequency change (dF/dt) that a switcher can track. With abrupt clock frequency changes, output spikes will occur at the clock frequency transition edge (much like a load step response). Lower bandwidth switchers have more pronounced spikes.

Does It Really Work?

In the world of EMC (electromagnetic compatibility) switchers are almost always emitters and everything else is a potential receiver. At any instant in time, peak emissions from a switching regulator appear to be the same, whether or not SSFM is enabled. The amplitude of the instantaneous emission is unchanged but it does move around in frequency. So, how does this work?

The effectiveness of SSFM depends on the amount of spreading and the frequency modulation rate relative to the bandwidth of the receiver. To receive an "instantaneous snapshot" of emissions requires a receiver that has infinite bandwidth and, fortunately, every practical system has a limited bandwidth. The system's bandwidth determines two important characteristics: the range of frequencies for which the receiver will respond and how quickly the receiver will respond (its response time) when subjected to EMI. If the emitting signal enters the measurement system's band infrequently and for short periods relative to the system's response time, significant EMI reduction occurs. Of course, any performance enhancement must be determined on a system-by-system basis and while SSFM may yield improvements, it is not a substitute for standard layout, filtering and shielding practices.

In addition to in-system EMC concerns, all systems are required to pass regulatory agency EMC tests before they are allowed for sale in the market. During regulatory agency EMC testing, the bandwidth of the test equipment is set to strictly defined standards (per CISPR 16-1) chosen to reflect the real world bandwidths of interest. Regulatory agencies first use an envelope detector called a peak detector. Peak detector measurements above the pass/fail limit are further processed with a quasi-peak detector, which weighs the signal measurement according to its repetition rate. Many agencies also test with an average detector, which is simply the peak detected output processed through a very low frequency, low pass filter.

The same mechanisms discussed earlier are at work here. Specifically, SSFM lowers the peak detector measurements by limiting the amount of time for which the emissions are in the measurement band. It provides further improvement with the quasi-peak detector if the emissions enter the measurement band infrequently and yields even more substantial improvement with the average detector, since the average in-band time is reduced.

Example

To illustrate, let's consider an emitter with a continuous, steady state, stationary emission (also known as a CW or Continuous Wave Signal). As illustrated in **Figure 3**, the peak detector scans across the band of interest (Band B, for example).

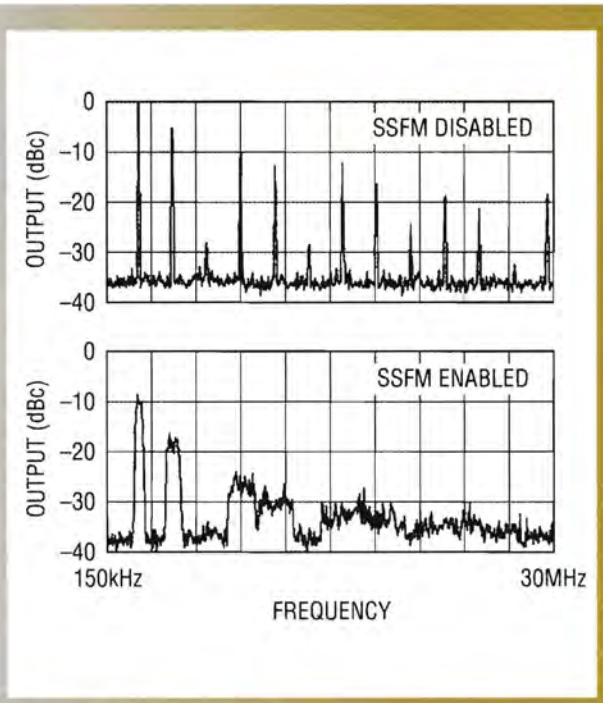

***Figure 4:** Switching regulator output emissions using a 9kHz resolution bandwidth, peak detector (LTC6908)*

As the frequency of the emissions enters into the bandwidth of the peak detector, the output of the peak detector will rise up to a steady-state DC signal. With a DC peak detect signal as an input, both the quasi-peak detected signal and the average detector signal will result in the same DC value. In other words, a CW signal will give the same result from the peak detector, quasi-peak detector and the average detector.

If we apply SSFM to the test device such that we no longer have a CW emission, the peak-detected signal will have "blips" of response as the emitted signal sweeps through the peak-detector bandwidth. Because of limited time in-band, these blips never reach the same amplitude of the original CW signal. The charge and discharge time constants of the quasi-peak detector result in further attenuation and the combined attenuated peak detector signal with reduced in-band time results in a much smaller average detector result.

Harmonics

One additional benefit of SSFM should be noted. In some systems, the harmonic components of an emission can be more problematic than the fundamental frequency. For example, some systems may be more effective radiators at higher harmonic frequencies. This is not a problem for SSFM, since it is even more effective at reducing EMC from harmonics than from the fundamental frequency.

To see this, consider that a 10% SSFM technique will spread the fundamental and all of the harmonics by 10%. For example, a 200kHz fundamental will be spread ±20kHz and the 9th harmonic at 1.8MHz will be spread ±180kHz. Since the receiver or regulatory test equipment has a fixed bandwidth, a wider frequency spread translates to less in-band time. The result is better EMC reduction for each successively higher harmonic frequency. **Figure 4** shows the result of a switching regulator with and without SSFM from a 9kHz resolution bandwidth, peak detector enabled. Notice that the harmonics show a dramatic improvement in emission reduction.

Clear Benefits

When the use of multiple switching regulators is appropriate, multiphase synchronisation offers clear benefits, including reduced EMI. As for the EMI benefits of SSFM, it depends on the bandwidths of interest. SSFM is not a substitute for proper design, but it may offer the improvement that achieves EMC compliance.

Both multiphase synchronisation and SSFM are very straightforward to implement.

AS EASY AS FLIPPING A SWITCH

Linear Technology's newest SSFM oscillator, the LTC6908, includes a proprietary tracking filter to smooth the transition from one frequency to the next. Most switchers have a bandwidth of 1/10th to 1/20th of the nominal switching frequency, which is suitable for the LTC6908's default modulation rate of 1/16th of the nominal clock frequency. For limited bandwidth switchers, the LTC6908's modulation rate can be decreased to 1/32nd or even 1/64th of the nominal clock rate to ensure proper regulation. The internal filter tracks the hop rate to provide optimal smoothing for all frequencies and modulation rates.

Using Linear Technology's LTC6908, the nominal switching frequency is set with a single resistor, the percentage of frequency spreading is fixed at ±10% and the phase relationships between outputs are fixed. Since SSFM is enabled when the user selects one of three modulation rates, realising the benefits of SSFM is as easy as flipping a switch.

BOARD LAYOUT & HIGH-RESOLUTION ADCs

ADC clock and board layout design can be applied to test instrumentation, industrial measurement and telecommunication systems, says Paul McCormack, Senior Applications Engineer at the Data Conversion Division of National Semiconductor Europe

High speed ADCs (Analogue to Digital Converters) are the key analogue processing component in a diverse range of applications, including mass spectrometry, ultrasonic inspection, LIDAR/RADAR and telecommunication transceiver modules. Whether the application be time or frequency domain based, ADCs with the highest possible levels of dynamic performance are required. Faster and higher resolution ADCs enable ultrasonic systems with sharper images and telecommunication systems with higher data handling capacity.

As ADC sampling rates continue to increase in the hundred of mega samples range at resolutions equal to or greater than 14 bits, the challenges for system designers become increasingly difficult. System designers must become experts in topics such as clock design and distribution and board layout.

This article examines these critical areas of system design, taking a particularly close look at printed circuit board (PCB) ground and power plane layout techniques. State of the art converters require state of the art board design! Without a precision clock source or carefully designed board layout, a high performance Porsche-like converter will have the performance of an old Fiat.

Single IF heterodyne receiver architectures and sophisticated power amplifier linearisation algorithms are imposing challenging requirements on ADC performance. Such systems are pushing the converter's inherent jitter performance well below half a picosecond. Likewise, test instrumentation engineers demand very low noise performance over a wide bandwidth for sophisticated spectrum analyser development.

As a result, one of the most important sub-circuits within a high-speed data conversion system is the clock source. This is because the timing accuracy of the clock signal can directly affect the dynamic performance of the ADC.

To minimise this influence, an ADC clock source must exhibit very low levels of timing jitter or phase noise. If this factor is not considered when choosing a clock circuit, the system dynamic performance will be poor, irrespective of the quality of the front-end analogue input circuitry or the converter's inherent jitter performance. A perfect clock will always deliver edge transitions at precise time intervals.

In practice, clock edges will arrive at continuously varying intervals. As a result of this timing uncertainty, the signal-to-noise ratio of a sampled waveform can be compromised by the data conversion process.

The maximum clock jitter that can be tolerated from all jitter sources before the noise due to jitter exceeds the quantisation noise (1/2 LSB) is defined from the following equation:

$$T_{j(rms)} = (V_{IN(p-p)} / V_{INFSR}) * (1/(2^{(N+1)} * \pi * f_{in}))$$

If the input voltage (V_{IN}) is optimised to equal the full scale range of the ADC (V_{INFSR}), then the jitter requirement becomes a factor of the ADC's resolution (N bits) and the input frequency being sampled (f_{in}).

For an input frequency of 70MHz, the total jitter requirement is:

$$T_{j(rms)} = 1 * (1/(2^{15} * \pi * 70 * 10^6))$$

$$T_{j(rms)} = 140\,fs$$

Since many systems distribute the reference clock via backplane or another connection that degrades the signal quality, usually a local oscillator (a low phase noise VCXO) serves as the timing source for the ADC. **Figure 1** shows an implementation using National Semiconductor's LMX2531 clock synthesiser. The LMX2531 is shown connected to a timing generator capable of dividing the synthesiser output by a programmable divisor while providing jitter performance in the order of less than a hundred femto seconds.

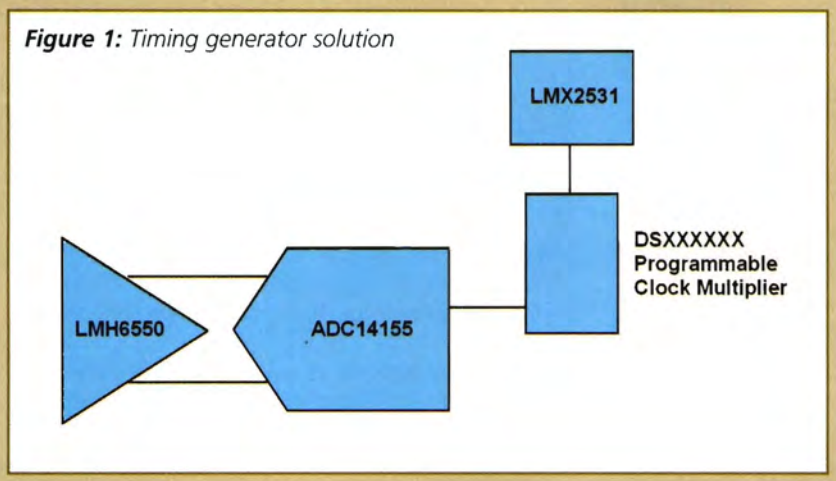

Figure 1: *Timing generator solution*

Layout Considerations

There are many advocates for and against and many heated discussions and long hours have been spent on the subject. One point is clear: proper grounding and routing of all signals is essential to ensure accurate signal conversion.

The results of our internal experiments and evaluation board developments have shown that split ground planes work well up to about 50MSPS for 10-bit ADCs and to about 30 to 35MSPS for 12-bit ADCs. Beyond that excessive circuit noise is evident and the split ground plane can also lead to signal radiation. Problems occur when the lines carrying signal currents cross the split between the planes.

Of course, analogue components should be kept in the analogue area of the board and digital components in the digital area. This keeps analogue and digital return currents away from each other (**Figure 2**) whilst **Figure 3** shows a board with a split ground plane. It makes an attempt to isolate analogue and digital ground currents and can be effective in minimising ADC noise but ignores EMI effects. Additionally, when supply traces are used to control the analogue and digital power paths, the return ADC current must deviate from the outgoing current path. This produces a current loop area that can radiate.

We can eliminate the loop area problem and minimise the radiation problem by using both a separate ground plane and power plane. This allows the outgoing and return currents to flow close to each other and minimise RFI/EMI problems. The problem now, however, is that component placement relative to each other is very important as common analogue and digital return current paths can lead to digital noise in analogue circuits. As we know, high frequency or high edge rate signals see a high resistance, even in a ground plane, so we know the need to keep analogue and digital return currents separated from each other.

Remembering that the proximity effect causes outgoing and return currents to flow as close to each other as they can, we realise that we can control the path of return currents in the ground plane by careful component placement and thoughtful routing of all traces, including those of the power supply. Ground return currents will follow their respective outgoing traces and thus it is possible to keep analogue and

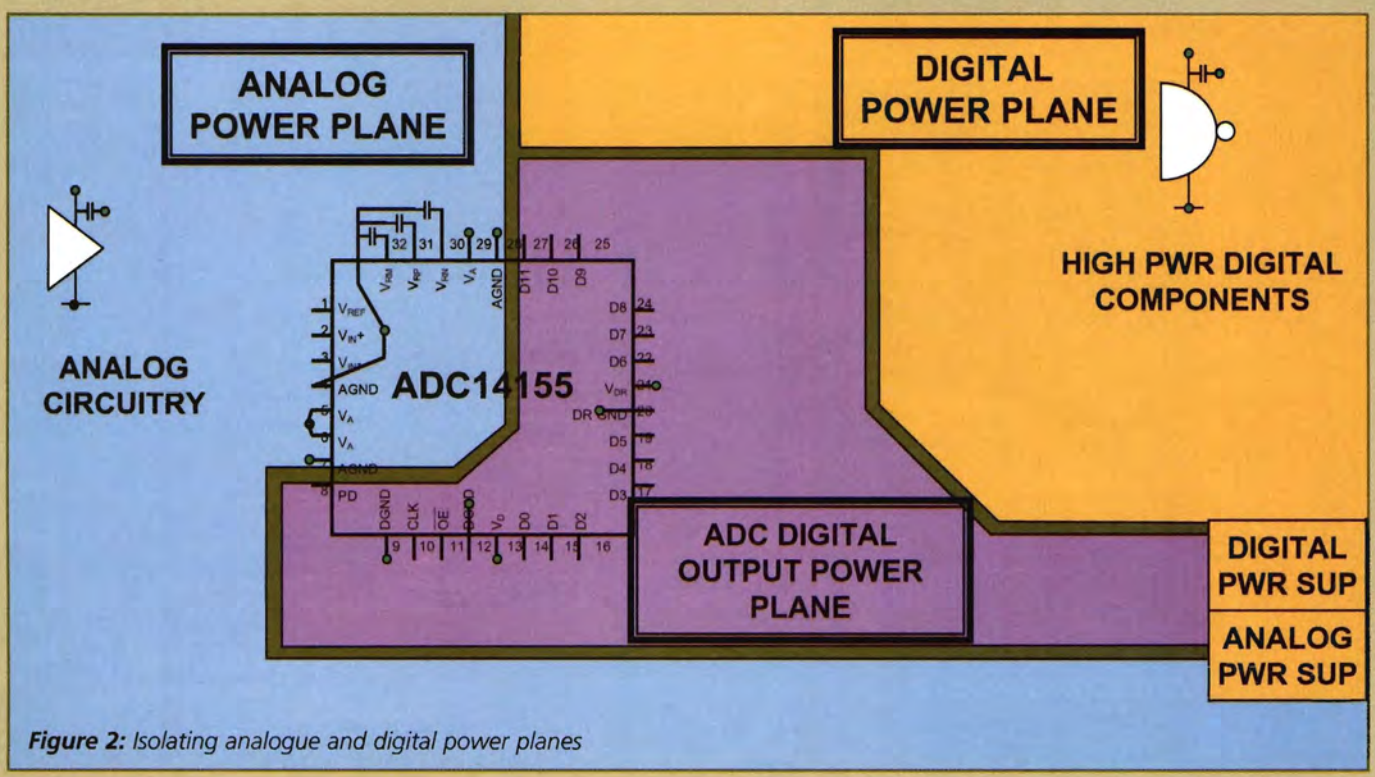

Figure 2: *Isolating analogue and digital power planes*

digital return currents away from each other.

The single ground plane eliminates loop areas and the signal and power traces control current flow, even in the ground plane.

Analogue and digital components should be located in their own, dedicated areas of the PCB. The power supply should be located at a board edge or corner and between analogue and digital areas.

Layout of power supplies is also critical for noise performance. Digital components (especially high speed, high powered digital components) must not be placed on or near the path that analogue return currents follow in getting back to the power supply. That is, they should not be located near lines carrying analogue currents or power supply lines to analogue or mixed-signal components. Remember that power supply lines carry signal currents because they recharge bypass capacitors on the board. Their return currents must go through the common junction of a split ground plane, flowing away from the outgoing (power) trace/path. This forms a loop area that will radiate. Sometimes this radiation can be picked by analogue circuits.

This recommended layout will allow the best performance that the ADC can provide. To summarise the requirements:

- Use a solid, unified ground plane. DO NOT split the ground plane. If there are ground planes in more than one board layer, connect them all together with a grid of through-holes (vias) on a spacing of about 2cm or less.
- Split the power plane, keeping each power plane in the same board layer. There should be separate power planes for (1) analogue circuitry, (2) digital circuitry, and (3) the ADC digital output drivers.
- Use analogue power for the ADC digital core supply, but NOT for the ADC digital output drivers.
- The power for the ADC digital output drivers may be the same supply as for the component(s) driven by the ADC outputs.
- Locate all analogue components and lines over the analogue power plane and all digital components and lines over the digital power plane.
- Use separate power sources for each plane. The ADC digital output power can come from either power source, but should be decoupled with a series choke. It is generally best to use a linear voltage regulator for the ADC analogue power source.
- If any digital circuitry is powered by the same supply as the ADC output drivers and has signal lines going to the other digital area of the board, use capacitors between the two power planes. Locate these capacitors very close to the signal lines.

ADC14155 Tips

The ADC14155 is a 14-bit 155MSPS ADC with a 1.1GHz analogue input bandwidth enabling high intermediate-frequency (IF) architectures. In wireless communication systems, the ADC14155's high input bandwidth allows it to digitise the first IF, eliminating the need for a second IF down-conversion stage.

The ADC14155's dynamic performance is 85dB spurious free dynamic range (SFDR) and a 72dB signal-to-noise ratio (SNR) at an input frequency of 70MHz, which is commonly used in communications receivers.

The ADC14155 has a timing jitter of only 80fs. To prevent SNR degradation by the external clock source, its additive jitter should be limited to 60fs for an analogue input frequency of 70MHz. This is very difficult to achieve in practice.

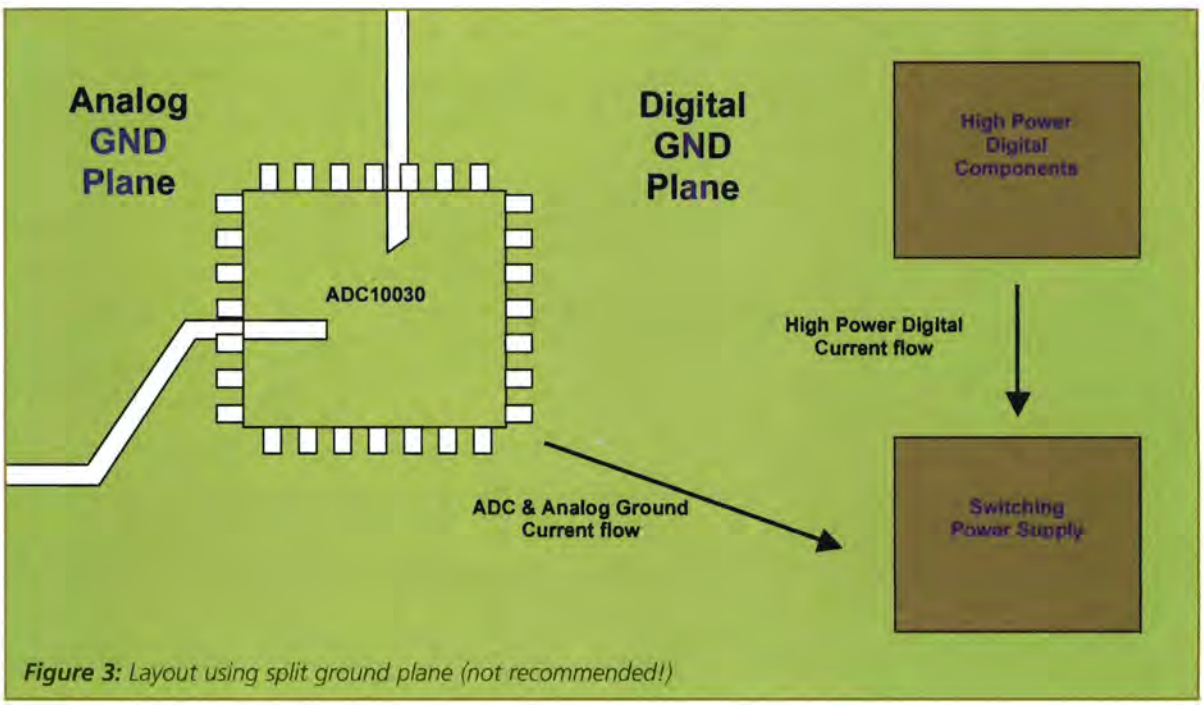

Figure 3: *Layout using split ground plane (not recommended!)*

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PROVING BENCH TEST DESIRABILITY OF EMC

Ian Darney writes about testing EMC in system design, based on his own experiences and gives a detailed description of a pair of transformers as essential components in the process

Back in the time when I worked for British Aerospace, there were many occasions when I needed to liaise closely with the team at the local EMC facility. This gave me an opportunity to observe, listen and learn.

Being partly responsible for the design of the Equipment-Under-Test (EUT), I was naturally interested in identifying ways in which the circuit design could be improved. The first thing that became evident was that, unlike every other aspect of system design, there was no way of checking EMC before the equipment was subjected to the mercies of the test house. Electro-Magnetic Compatibility (EMC) was always the last characteristic to be verified. Since this process was always scheduled to occur after the performance, vacuum, vibration and thermal tests had been completed, the cost impact of a failure to meet the EMC requirements could be quite dramatic.

There were many committees involved in defining the best way to design equipment to achieve EMC. As far as I am aware, none of them ever reached any sort of agreement. The subject is as fruitful a source of disagreement as any religious controversy.

Objectives, Problems and Solutions

It seemed to me that the only way forward was to develop a way to carry out bench tests of equipment in the early development stage and to use the results to predict the performance of the system before formal EMC tests took place. Two problem areas were immediately identified: EMC test equipment was hideously expensive and its use was confusingly complex.

There was no obvious way of modelling the coupling mechanisms involved.

However, the similarity between conducted emission and conducted susceptibility tests did seem to offer a way forward. Both involve the measurement of currents and voltages – the parameters circuit designers work with every day.

In the conducted susceptibility test, the EUT is installed on a test bench and a voltage transformer is clamped around one of the cables. During the test, a high amplitude, variable frequency, common-mode current is caused to flow in the cable. If the EUT performs normally throughout the process, it is deemed to have passed that particular test.

In the conducted emission test, a current transformer is clamped around one of the cables. The EUT is caused to function normally and the common-mode current is monitored over a wide range of frequencies. If none of the peaks in the response exceeds a predefined limit, then the equipment is deemed to be compliant with one of the requirements.

It seemed to me that equipment designers have one distinct advantage over the engineers in the EMC test facility – they can probe inside the EUT; they can modify the design of the circuitry behind the cable/connector interface. Special equipment could be built to monitor the signals at any input. The interconnecting cables could be assembled in exactly the same way as the planned formal tests. The information gained from the bench tests could be used in all sorts of ways.

The same approach can be applied to analyse the conducted emission. If necessary, the design of the system-under-review could be modified. All this can be done at a very early stage in the development process.

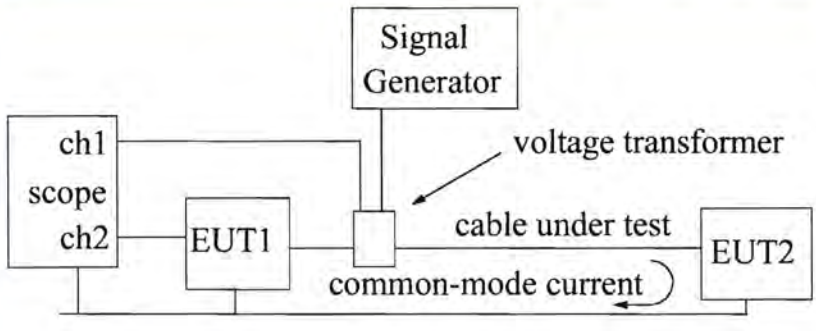

Figure 1: *Measuring the conducted susceptability characteristic*

Conducted Susceptibility and Emission

Using the setup of **Figure 1**, measurements can be made of the transfer characteristic between common-mode source and the

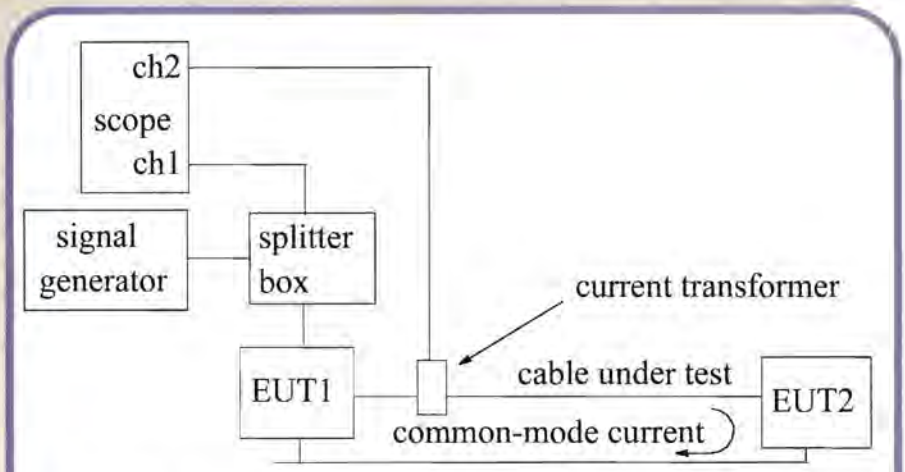

Figure 2: *Measuring the conducted emission characteristic*

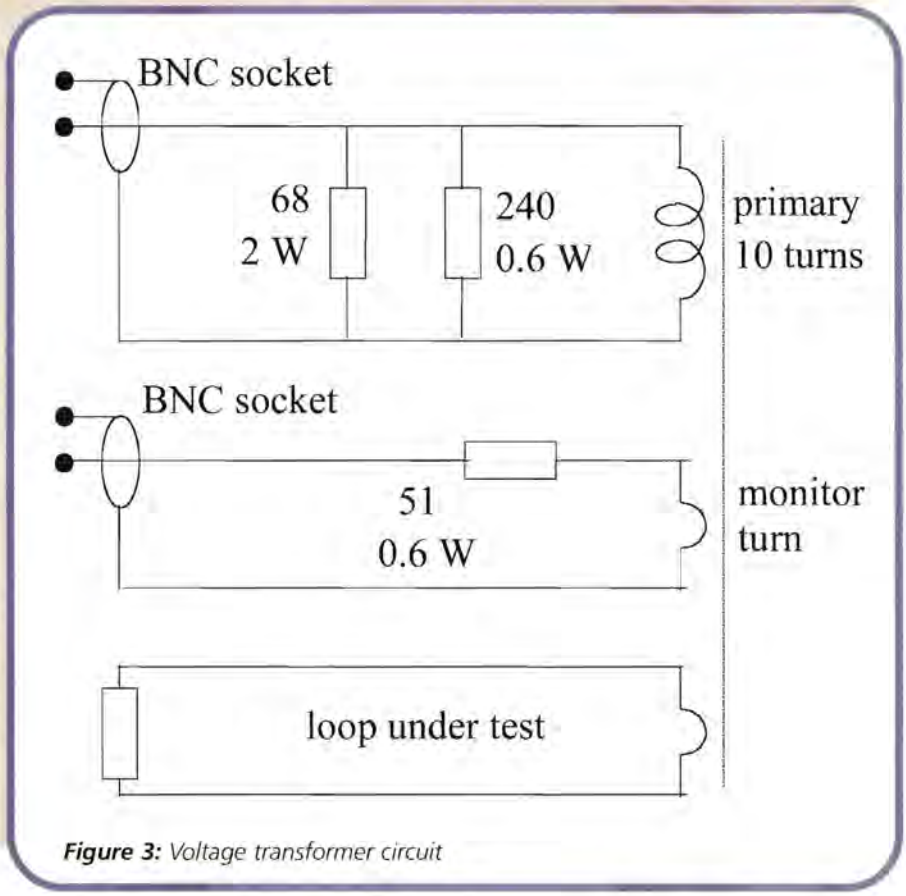

Figure 3: *Voltage transformer circuit*

differential signals appearing at the EUT input. These measurements can be used to determine the frequency and amplitude of the differential-mode interference.

Once the transfer characteristic is known, it becomes possible to inject differential-mode interference directly into the interface circuitry and observe how the equipment responds. It becomes possible to create a model which defines the relationship between common-mode and differential-mode signals due to cable coupling. It becomes possible to simulate the performance of the EUT when it is subjected to interference.

The same approach can be used to analyse the emission characteristics of the system. The setup for this type of test is illustrated by **Figure 2**. Here, a sinusoidal source is used to apply a pre-defined signal to the circuitry at the interface between EUT1 and the cable under test. This will cause a differential signal to be transmitted to EUT2 via the cable.

Electromagnetic effects will cause a common-mode current to flow in the loop formed by the return conductor and the structure. This current is monitored by Channel 2 of the oscilloscope. The amplitude of this current can be compared to the amplitude of the input source, as measured by Channel 1 of the scope.

Transfer Admittance

In the setup of Figure 1, a single turn is used to monitor the output of the voltage transformer. This is the same voltage that is injected into the common-mode loop. The differential signal appearing at EUT1 interface could be monitored as a current or as a voltage.

In the setup of Figure 2 the output signal is the current in the common-mode loop. The differential-mode source could be measured as either a current or as a voltage.

In both cases, it is possible to define and measure the input signal in terms of a voltage and to define and measure the output in terms of a current. In both cases, the measured parameter could be the ratio between output current and input voltage – the transfer admittance.

If the transfer admittance is used as the defining parameter, it allows a fundamental relationship to be established between the conducted susceptibility test and the conducted emission test. Moreover, the transfer admittance is a direct indicator of the unwanted output created when a constant voltage signal is used as the interference source. A graph illustrating the variation of transfer admittance with frequency provides an extremely informative picture of the interference characteristics.

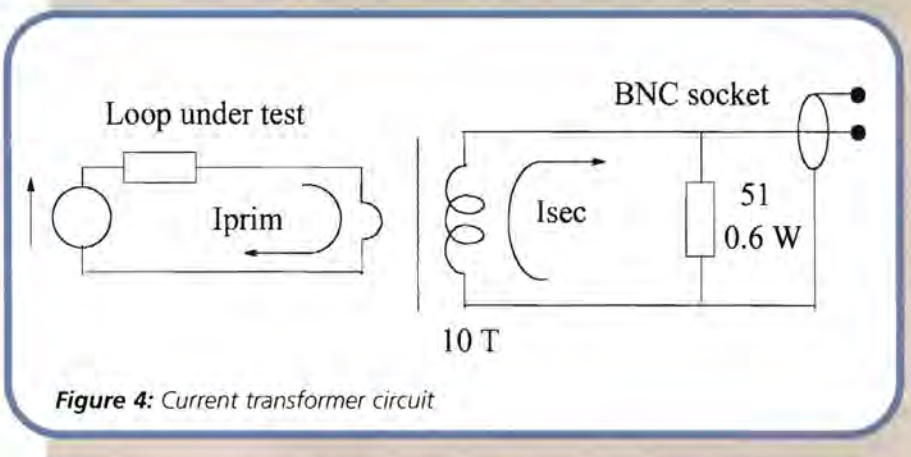

Figure 4: *Current transformer circuit*

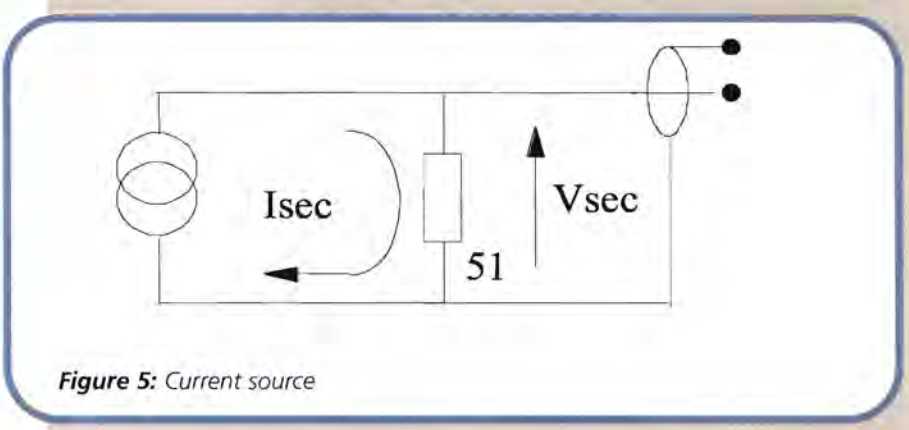

Figure 5: *Current source*

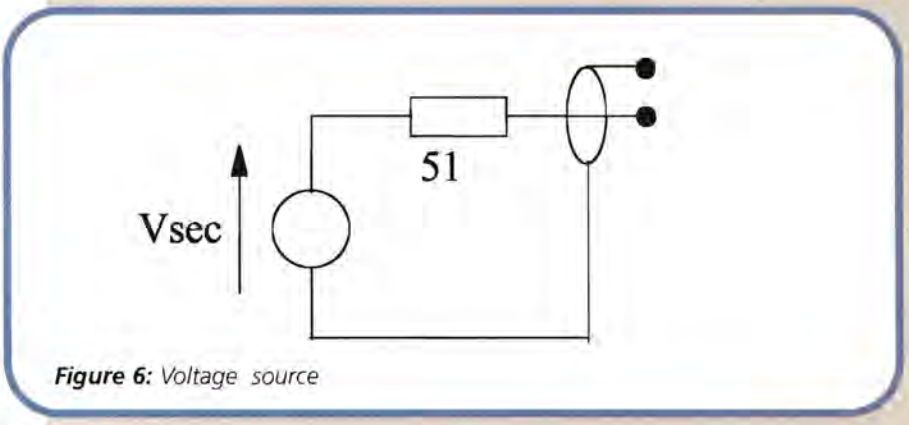

Figure 6: *Voltage source*

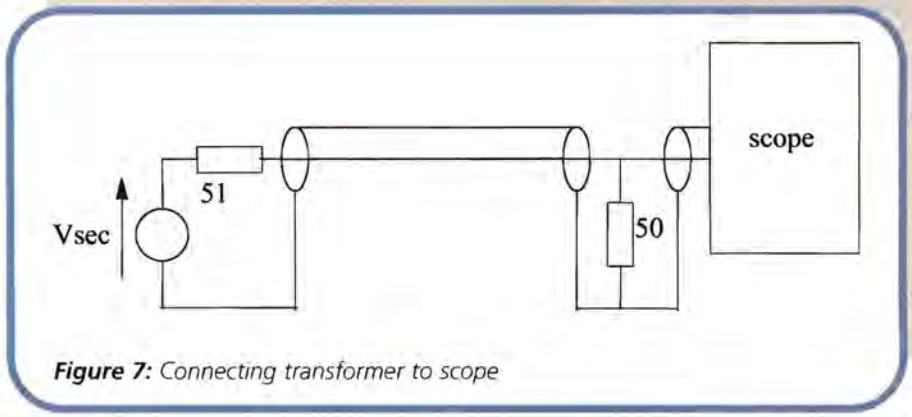

Figure 7: *Connecting transformer to scope*

Transformer Requirements

A review of the transformers used in formal EMC testing will reveal their most significant characteristic, as far as the average equipment designer is concerned. They are extremely expensive.

From the point of view of the engineer at the bench, the need is for a pair of low-cost transformers that can be used in the setups of Figures 1 and 2. The basic requirements, as indicated by the design of the transformers already in use, are that the magnetic core should be of ferrite material and should be able to clamp around the cable-under-test.

For several years now, the basic components for such transformers have been available and can be purchased from at least one reputable supplier. Fair-Rite Products (*www.fair-rite.com*) supply a number of "cable suppression core assemblies" that are designed to suppress interference at frequencies up to 500MHz. Although other manufacturers supply similar products, this was the first example of low cost, split-core assemblies that I had come across.

Each assembly consists of two identical ferrite cores. When placed together, they form a closed magnetic path. The cores are mounted in a plastic case which provides a hinged assembly. This can be opened to clamp around the cable. When closed, the plastic case snaps shut.

Voltage Transformer

It did not take long to construct a voltage transformer from this component. Ten turns of 20 gauge, enamelled, copper wire were wound on one side of core assembly part number 04 31 173 951. This constituted the primary winding, as shown on **Figure 3**. Resistors were added to make the primary winding 'look' like approximately 50Ω over most of the operating bandwidth. The 68Ω resistor is rated at 2W to handle a 10V peak-to-peak input signal.

The monitor winding consisted of a single turn of 20-gauge, enamelled, copper wire on the opposite core. A 51Ω resistor was added in series with this, to make the monitor winding 'look' like a 51Ω source.

Terminations were provided by a terminal block and the back terminals of two BNC connectors were fitted directly into the block. The block was tied to the core with a piece of string and a section of a small potting box was used to provide stress relief to the BNC terminals. Inserting and removing a bayonet plug does incur a significant torsion.

In use, the two halves of the core can be held firmly in place by a releasable tie-wrap wrapped around the assembly. Although the final assembly cannot be described as rugged or elegant, it has survived repeated use for three years.

Current Transformer

The current transformer uses exactly the same core assembly as the voltage transformer and has exactly the same number of turns of 20-gauge ECW. As illustrated on **Figure 4**, this winding acts as the transformer secondary.

The primary winding is the loop under test. Since there are ten turns on the secondary, I_{sec} is one-tenth that of I_{prim} and the input impedance to the load resistor is extremely high. The 51Ω resistor is effectively supplied by a current source, as illustrated by **Figure 5**.

Applying Thevenin's Theorem to this circuit model results in the model of **Figure 6**.

Since the output impedance of this configuration is 51Ω, it provides a good match to the characteristic impedance of a 50Ω co-axial cable. If such a cable were connected to the BNC connector and the other end terminated by 50Ω at the input to an oscilloscope, the circuit model would become as shown on **Figure 7**.

Since the 50Ω cable is transparent in this configuration, the amplitude of the input voltage to the oscilloscope is proportional to the amplitude of the current in the loop-under-test.

The current transformer can be calibrated by applying a known current to the input and monitoring the signal at the scope input. For any such configuration, the transfer impedance can be defined as the ratio of the voltage at the scope input, divided by the amplitude of the current in the primary loop. For the configuration described in this article, this characteristic is as shown on **Figure 8**.

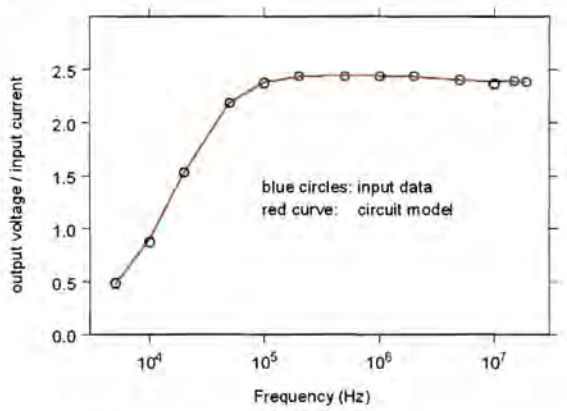

Figure 8: *Calibration curve for current measurements*

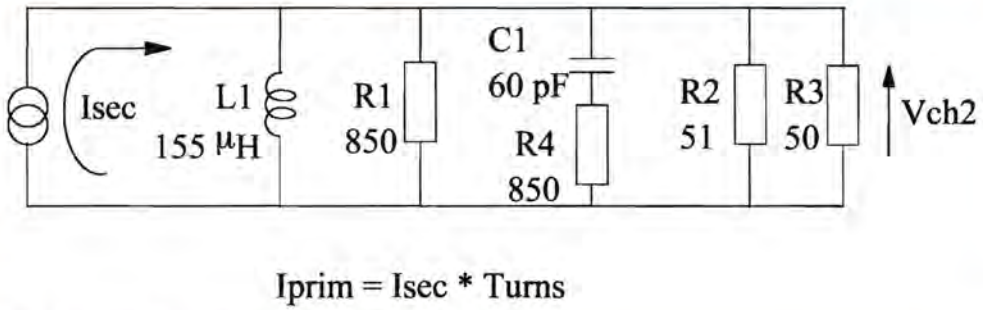

Figure 9: *Circuit model for secondary loop*

Using this data, it is not difficult to construct a circuit model of the setup. This is illustrated in **Figure 9**. Using this circuit model, it becomes possible to measure the amplitude of any current in the loop-under-test. The response of this model is shown as a solid red line in the graph of Figure 9, whilst the data points are circled.

Since the bandwidth of the response is quite wide, the monitored current need not be sinusoidal.

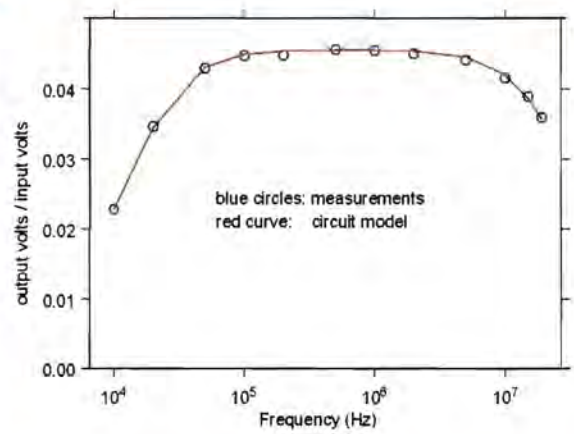

Figure 10: *Voltage transformer characteristics*

Voltage Transformer Calibration

The voltage transformer can be calibrated in much the same way. This resulted in the characteristic of **Figure 10** for the transformer described here.

There is no need to create a circuit model in order to use the voltage transformer. The monitor winding gives an accurate measure of the

voltage induced in the loop under test. It also compensates for any voltage drop in the primary winding due to high current in the load.

Figure 11 is a picture of both assemblies, showing the terminal blocks and BNC connectors. The jaws of the voltage transformer are open. The current transformer is closed, with a tie-wrap ensuring firm connection of the two cores.

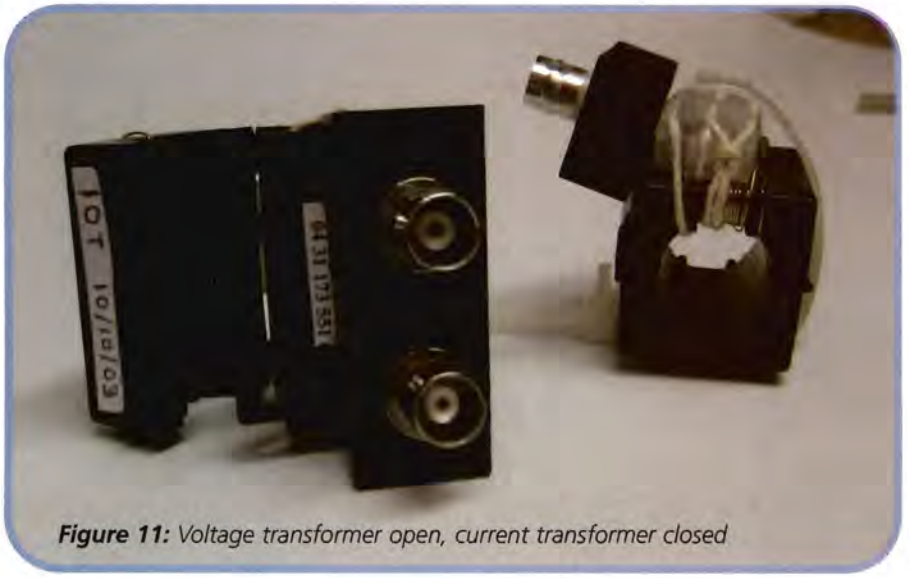

Figure 11: *Voltage transformer open, current transformer closed*

Desirable Bench Tests

This article has outlined why it is desirable to carry out bench tests of the EMC of equipment under development and has indicated how such tests can be carried out. Essential components in the process are a wideband voltage transformer and a wideband current transformer. A detailed description of such a pair of transformers has been provided and it has been shown how they can be calibrated.

The ready availability of a pair of EMC transformers is an essential starting point in any attempt to analyse the performance of any system. There is no space in a short article to illustrate how they can be used to create circuit models of different cable assemblies, gain an understanding of the coupling mechanisms, create design guidelines based on that understanding and develop solutions to the various problems raised by electromagnetic effects. However, there is a fair amount of such information available at **www.designemc.info**

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THE RIGHT NFC TAG FOR THE JOB

Near Field Communication (NFC) is ready for adoption across a range of applications. However, to ensure a mass market and create profitable opportunities around the technology, designers and manufacturers need to make the right technology choices, especially when it comes to the NFC tag. Features and capabilities must match application needs and the price must be right for mass-market deployment.

NFC opens up new product and service opportunities for everyone from network operators and device manufacturers to service providers. For users, NFC will make it easier and more intuitive to access new media and content services, synchronise and share information and utilise smart ticketing and cashless payments.

Main NFC Applications

The initial mass-market applications of NFC are likely to build on existing payment and communications infrastructure and user behaviour, where the user benefits are most compelling, the business case is strongest and the commercial risks are lowest. This implies a need for low-cost NFC integrated circuits (ICs) that can be applied to a broad range of uses cost-effectively, in a way that is compatible with the broadest range of pre-existing devices and reader infrastructure.

Developers today have a choice of four NFC Forum mandated tag types to choose from. But how do you choose the right tag for the job?

It's likely that the first mass-market applications for NFC will be in relatively low-financial value applications – with low risk of fraud – that do not require large back-end infra-

NFC in a 'smart poster' application

A recently-launched White Paper from NFC/RFID IC design and solutions provider Innovision Research & Technology on the subject of NFC tags highlights several interesting aspects that designers should know when making the right choice. Ian Keen, project manager and a technical contributor to the NFC Forum, outlines the key points from this paper

structure investment. These fall into three main categories: peer-to-peer, payment and ticketing, and service initiation.

Peer-to-peer NFC is used to set up local communication between two devices. When the content transferred is relatively small (up to a few kilobytes), NFC is used to transmit the data itself. For larger amounts of data, NFC is likely to be used to establish a separate wireless connection – like Bluetooth – to carry the content. A good example is printing photos from a mobile phone.

Payment and ticketing: For merchants, NFC-enabled payments are much easier and cheaper to handle than cash or other traditional payment methods. Initially, NFC-enabled devices are likely to be used for vending machines and parking meters and other quick-pay environments, such as kiosks or fast food outlets.

Service initiation: If the user touches an NFC-enabled device against a tag, it transfers a small amount of information to the NFC device. This could be plain text, a web address (URL) or phone number. An example is the 'smart poster' application, where users touch their mobile phones against a tag embedded in the poster – this triggers the transmission of a URL to the phone and opens a web browser to the specified URL.

So these are the first wave of possible applications, but what types of NFC tags are available to make these happen?

Mandated Tag Types

In June 2006, the NFC Forum announced the initial set of four tag formats that all NFC Forum-compliant devices must support. Tags compatible with these mandatory formats are available initially from Innovision, Philips and Sony. They were selected to cater for the broadest possible range of applications and device capabilities:

Type 1 – based on ISO 14443 A, has a 96-byte memory capacity

Type 2 – based on ISO 14443 A, has half the memory capacity of Type 1 tags

Type 3 – based on FeliCa, has a larger memory (currently 2 kbyte) and operates at a higher data rate (212kbit/s), suitable for more complex applications

Type 4 – fully compatible with ISO 14443A/B, this offers large memory-addressing capability with read speeds of between 106kbit/s and 424kbit/s, making it suitable for multiple applications.

With initial mass-market deployments likely to be in low-financial value, low-risk applications, it's important that NFC tags meet the requirements with the right balance of cost and performance.

In smart poster applications, you would need a tag that is small and low-cost enough for mass deployment, but with sufficient memory to contain a reasonably long URL and additional security features.

For MMS or ring tone downloads, where users touch their phones to a product or promotional piece, for example, to obtain a picture message or ring tone, small size again is important, but so are sufficient memory and security. The larger the memory capacity on the tag, the more information can be transferred directly to the phone. However, there are limitations arising from the short 'touch time' between the NFC device and the tag. In practice, this sets an upper limit for the amount of data exchanged to a few kilobytes during the touch.

In shortcut applications, users can automatically send an SMS or phone number by touching their phone against a tag embedded in objects, such as a photo frame, and used to provide the number of the person in the picture, as a fun or practical application for the elderly or disabled. Here, small size and low cost are the main considerations.

Bluetooth pairing between a mobile phone and a headset, or digital camera and printer is simplified by NFC. Only a small amount of memory is required, and small size, low cost – with low risk of 'tearing' the data transfer – are key requirements.

First NFC Market Cases

So, what we are currently seeing is the first mass-market applications for NFC, which will build on existing infrastructure, initially in relatively simple shortcut, identification, service discovery/initiation or device pairing applications.

For these, it is clear developers need a standardised tag format that is small, low-cost and flexible enough to be successfully integrated into existing form-factors and integrated circuitry.

Letters

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ELECTRONICS WORLD RESERVES THE RIGHT TO EDIT ALL CORRESPONDENCE

Excellent article, but one minor mistake

As always, I also enjoyed reading the February 2007 issue of *Electronics World*.

Has anyone pointed out that there is a misprint/error in Dogan Ibrahim's excellent article, '*Measuring Mutual Inductance Using the Atlas LCR Analyser*' on page 38?

On page 39 just below Equation 7, "*the permeability of free air/space*" should read 4*pi*10(-7) where pi = 3.14159. But because this equation is not used, all calculations are correct.

With this choice of permeability, the unit of current defined by the Biot Savart law is the Ampere (the unit we can all relate to!). Equation 7, using this permeability, is not used for calculation purposes but sets the scene for what follows.

It is a very minor point but it is one which threw me into a panic because I had been using this permeability in a lot of theoretical analysis.

Dogan Ibrahim's article is presented superbly and I found it extremely interesting. His Equation 7 with n1 = n2 = n becomes a very well known theoretical formula for self-inductance of an air wound coil (L=u0(n^2)A/l) and Wheeler's formula (1) involves an experimental correction to this formula (which I replaced by l+0.9a). Wheeler did not have this theoretical result when he obtained this formula using published experimental/tabulated data in 1925. He published Equations 1 and 3 in 1928 Proc IRE journal.

Tim Hunt
UK

Right Book Review, wrong author

In our June issue of Electronics World magazine, the author of the Book Review should have read Mark Shuttleworth and not Doug Taylor.

Ed

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UKDL COLUMN

Alphabet spaghetti ELECTRONICS

By Chris Williams, UKDL

Question: If I say to you that two major LCD manufacturers have announced that they will introduce TN versions of their AMTFT LCD cells for use in TVs would you:

1. Jump for joy and say: "That should see at least £60 off the selling price in the shops"
2. Moan and say: "That will reduce the image quality back to the old days of the late 90s."
3. Look with a blank expression and say: "What are you on about?"

My guess is that most of you would opt for option 3 because to the uninitiated, the casual use of industry-specific acronyms is a real killer. Without a proper understanding of what these words mean – the TLAs, or Three Letter Abbreviations (although some have four letters), so loved by our industry, we risk being taken for an expensive ride by the manufacturers, distributors and retailers of electronic goods. The younger generation today think they own the world with the use of innovative texting language to deliver abbreviated messages – forget it kids – we industrialists have got you beaten from the start.

What I said in the opening sentence was that two major Liquid Crystal Display manufacturers are proposing to introduce Twisted Nematic (TN) versions of their Active Matrix Thin Film Transistor Liquid Crystal Display (LCD) cells for use in televisions. The cognoscenti would groan at this point – Twisted Nematic AM TFT LCDs were the 1st generation AMTFT LCD displays introduced back in the late 80s and early 90s. Characterised by poor viewing angles and poor colour reproduction as the viewing angle increases from zero, they were surpassed in the mid-90s and beyond by Vertically Aligned Nematic (VAN) displays that offered much wider viewing angles.

Of course, in this fiercely protective world of ours, any major invention is closely guarded and protected by Intellectual Property (IP) registration, usually in the form of patents. The inventors of the VAN technology don't want to share it too widely and support their competitors, so alternative versions of this vertical alignment of the liquid crystal molecules were developed, patented and introduced to the market. This gave us Multiple Vertical Alignment (MVA) and a variety of other alternatives for what is essentially the same thing: liquid crystal molecules in the display cell are initially aligned perpendicular to the plates of the display cell, whereas in the older Twisted Nematic, the liquid crystal molecules are aligned parallel to the plates of the display cell. Scientists found that by having the LC molecules mounted in the perpendicular position, light waves being transmitted through the cell along the LC chains maintained integrity over a wider range of angles than before, hence allowing displays with much wider viewing angles to be developed.

There is of course a further option to disprove the rule. Hitachi developed an In-Plane Switching system (IPS), which allowed it to build displays using LC molecules in the original parallel plane.

But, back to the main point, although VAN (and MVA, MVD, etc) displays give much better image quality than TN displays do, the actual liquid crystal fluid used by them is protected by patent and only available from one supplier. Twisted Nematic fluids are available from several suppliers hence they are generally much cheaper. So, if you want to make a cheap, cheerful TV set to stack high and sell in volume, chances are you will be tempted to go for the lowest cost bill of materials and opt to use TN fluids instead of VAN. Shame about the image quality, but look at the price.

Conclusion of this little story is that not every development is a positive step forward and even the most innocuous TLA might hide a myriad of design compromises implemented to make the product you buy just that little bit cheaper.

I am not saying that everyone should automatically go out and buy the most expensive product on offer – that can be just as bad, since you are spending a high percentage of the purchase price on the "brand name" and not on the cost of the equipment, but I do urge you to spend just a few more moments, or preferably minutes, to look into the exact specifications of the product you want to buy and don't rely on the TLAs to be telling you the truth.

Try this – when you have a few minutes to spare, walk into any store selling TVs and computers and look at the details on the advertising promotional materials. Count the TLAs and then try and decide exactly what they tell you and more importantly – what they don't. You may see that AM TFT LCD can show 16 million colours – but how many pixels does that show? And if it is a TV, what standards is it compatible with – how does it look with a standard TV transmission, DVD transmission, full HDTV?

Get the full specification and see the device working, showing the type of information or programme you want

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to watch. If you are happy, go with it – if you're not – walk away.
Enjoy the visit!

Below is a table of some of the more popular TLAs in use in our industry at present. Amuse yourself by seeing how many of them you know the meaning of. *Answers next month.*

Chris Williams is Network Director at UK Displays & Lighting KTN (Knowledge Transfer Network)

LCD	LED	OLED	FED	CRT
TN / STN	VAN	FLCD	CCFL	CPT
SSL	FET	OFET	OSC	SAM
ALD	PET	PEN	TG FET	BG FET
A-Si	P-Si	x-Si	TFT	HCFL

REACH

Gary Nevison is chairman of the AFDEC RoHS team, board director at Electronics Yorkshire and head of product market strategy at Farnell InOne. As such he is our industry expert who will try and answer any questions that you might have relating to the issues of RoHS, WEEE and REACH. Your questions will be published together with Gary's answers in the following issues of Electronics World. Please email your questions to: ***svetlana.josifovska@stjohnpatrick.com****, marking them as RoHS or WEEE.*

This month we are focusing on the new REACH legislation. Before we do, however, I wanted to answer the following question from an Electronics World reader:

Q: What are the requirements of RoHS with respect to the supply of electronic kits for self-assembly?

Stephen Ridgway
UK

A: This is not a straightforward one. However, it is my understanding that it depends on the function of the parts and who does the assembly. If assembly is carried out by anyone other than the user, then the status will depend on the function of the assembled product. Clearly, if parts are sold to the user, each part needs to be assessed, not the assembled product. This is because the RoHS directive applies to "finished products" that are "put on the market". The EC's guide to the implementation of directives, commonly known as the 'Blue Book', says that a product has not yet been put on the market if further assembly work is required.

Turning to REACH.....

Q: What is REACH?

A: REACH (Registration, Evaluation and Authorisation of Chemicals) is a major new body of legislation, which is set to be in force across Europe from 1 June 2007. It replaces over 40 existing directives and regulations that have been implemented since 1967, when the first Dangerous Substances Directive was introduced.

REACH is an integrated system for Registration, Evaluation and Authorisation of Chemicals across the EU and it extends the stringent testing which has been required for chemicals introduced since 1981 to those already in use (estimated at 30,000 substances).

Q: Why is it needed?

A: REACH aims to improve the protection of human health and the environment while maintaining competitiveness and enhancing the innovative capability of the EU chemicals industry. REACH also ensures that animal testing is kept to the strict minimum and that alternative methods are encouraged.

Q: Why should I be concerned?

A: REACH is one of the most significant and challenging pieces of environmental law to emerge from the European Commission to date and has far-reaching and potentially costly implications for everyone in the supply chain. It gives greater responsibility to industry to manage the risks from chemicals and to provide safety information. The responsibility for providing sufficient information and taking effective risk management measures will lie principally with manufacturers or importers of chemicals. Obligations will also be introduced further down the supply chain particularly in terms of the safe use of chemicals.

It's important that all manufacturers, importers and downstream users of chemicals are fully aware of the impact this new legislation will have on their business.

Q: How will REACH work?

A: Enterprises which manufacture or import more than one tonne of a chemical substance per year will be required to register it in a central database administered by the new EU Chemicals Agency. REACH will require a registration, over a period of 11 years, of some 30,000 chemical substances. The registration process requires the manufacturers and importers to generate data for all chemical substances produced or imported into the EU above one tonne per year. The registrants must also identify appropriate risk management measures and communicate them to the users.

The onus will move from the authorities to industry. In addition, REACH will allow the further evaluation of substances where there are grounds for concern and foresees an authorisation system for the use of such substances. This applies to substances that cause cancer, infertility, genetic mutations or birth defects, and to those which are persistent and accumulate in the environment. The authorisation system will require companies to switch progressively to safer alternatives where a suitable alternative exists. All applications for an authorisation need to include an analysis of alternatives and a substitution plan where a suitable alternative exists. Current use restrictions will remain under the REACH system.

The European Chemicals Agency (ECHA) is being established to take a central role in the implementation of REACH.

Q: Which chemicals does REACH cover?

A: There is no definitive list of chemicals likely to be covered by REACH. Chemicals are currently covered by EINECS (European Inventory of Existing Commercial – chemical – Substances), which lists 70,000 to 100,000 chemicals subject to pre-1981 legislation. This list is clearly out of date and many of the chemicals may no longer be on the market.

Chemicals subject to post-1981 legislation are covered by the EUCLID list. As mentioned, a new list will replace around 40 existing regulations. Implementation will be staggered and it is expected that the entire process will take about 11 years to complete.

MINIMUM COMPONENTS CURRENT-MODE SINUSOIDAL OSCILLATOR

The current mode oscillator of **Figure 1** was published by C. M. Chang et al in Electronics Letters, September 2002, Vol. 38 No. 9, where the proposed circuit employs one fully differential current conveyor (FDCCII), two grounded capacitors and three grounded resistors.

It could provide the following features: (i) use of a single active element; (ii) the use of only two grounded capacitors and three grounded resistors; (iii) non-interacting controls for the frequency of oscillation (FO) and condition of oscillation (CO); (iv) a simple CO and unconstrained tuning law for the FO. However, it is well known that a second order oscillator, which offers the minimum number of components, is based on only one current conveyor, two grounded resistors and two grounded capacitors.

A new circuit idea is described in **Figure 2** and this circuit also exhibits all of the above features. Furthermore, the proposed new oscillator circuit employs the minimum number of components, unlike the circuit in Figure 1 which uses more than one passive component.

Moreover, the proposed new circuit exhibits two high output impedance current sources with 90° phase difference, which is better than that of the circuit in Figure 1.

Circuit Description

Figure 2 employs a single FDCCII, two grounded capacitors and two grounded resistors, which are the minimum number of active and passive components to realise a second order sinusoidal oscillator. The port relations of the FDCCII can be characterised as:

$I_{Y1} = I_{Y2} = I_{Y3} = I_{Y4} = 0$, $V_{X+} = V_{Y1} - V_{Y2} + V_{Y3}$, $V_{X-} = V_{Y2} - V_{Y1} + V_{Y4}$, $I_{Z+} = I_{X+}$ and $I_{Z-} = I_{X-}$

The analysis of the proposed oscillator of Figure 2 has the following characteristics:

$$S^2 C_1C_2 + S(C_1 - C_2)G_2 + G_1G_2 \quad (1)$$

The condition of oscillation (CO) and the frequency of oscillation (FO) are shown in **Equations 2** and **3**, respectively.

$$\text{CO: } C_1 = C_2 \quad (2)$$

$$\text{FO: } f_o = \frac{1}{2\pi}\sqrt{\frac{1}{C_1C_2R_1R_2}} \quad (3)$$

These equations show that the FO of the oscillators can be controlled by R1 or R2.

The output current transfer function of I_{o2} to I_{o1} is shown in **Equation 4**.

$$\frac{I_{o2}}{I_{o1}} = -\frac{1}{sC_2R_1} \quad (4)$$

The phase difference of I_{o2} to I_{o1} is just 90°, based on the above equation.

It is obvious that the relation of I_{o2} and I_{o1} in Figure 2 has the quadrature feature.

Conclusions

A new current-mode oscillator circuit has been presented. The proposed circuit employs the minimum number of active elements and passive components and still has the following advantages: use of all grounded capacitors, use of all grounded resistors, non-interacting controls for the frequency of oscillation and condition of oscillation. Moreover, it offers the highly attractive feature where two high output impedance current sources with 90° phase difference can control many applications.

Hua-Pin Chen *and* ***Ming-Tzau Lin***
De-Lin Institute of Technology,
Tu-Cheng,
Taiwan.

Figure 1: *Current-mode oscillator circuit proposed in Electronics Letters 2002*

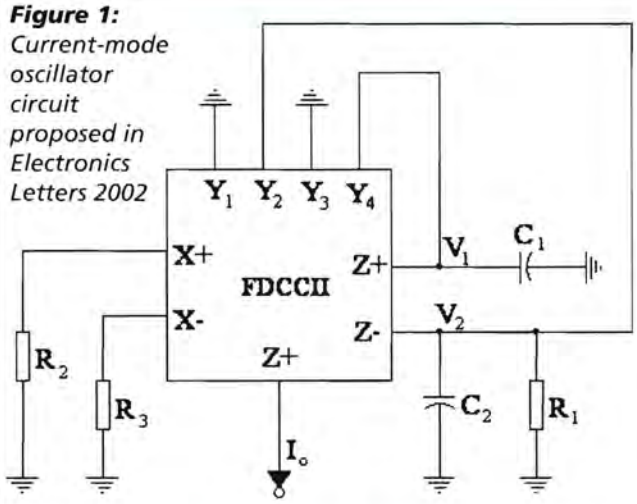
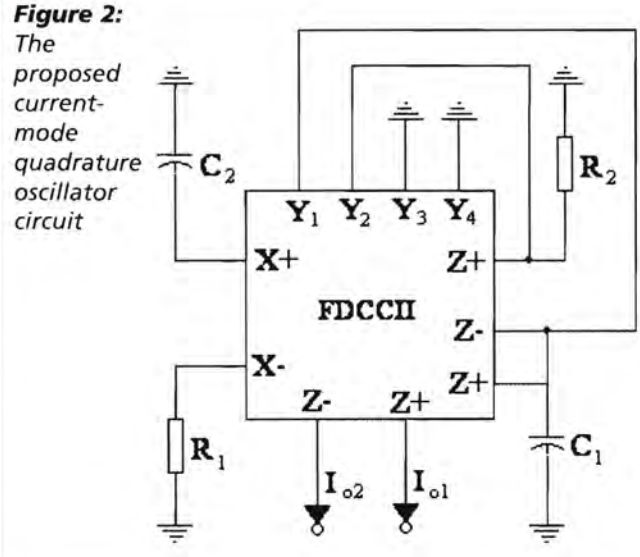
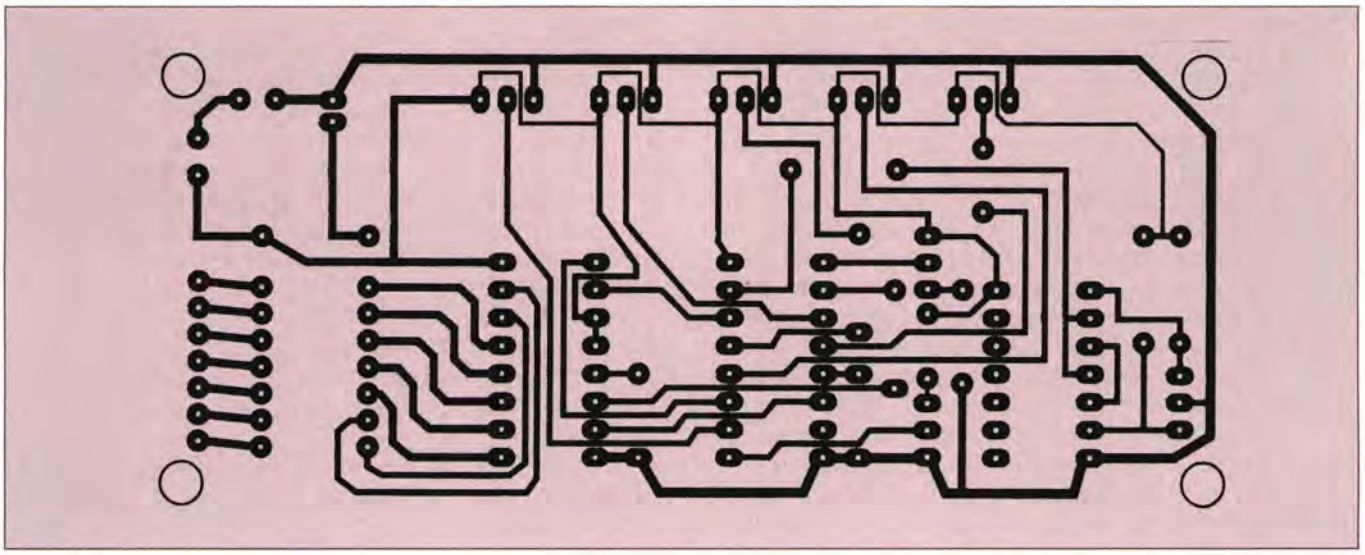


Figure 2: *The proposed current-mode quadrature oscillator circuit*



DIGI-KIT COUNTER AND DISPLAY



Objective

A counter whose output's logic status increments in steps on receiving clock pulses at its clock input is used for a variety of counting and timing applications. It forms the heart of digital clock circuitry and other similar timing devices.

A 4-bit binary counter will count in its natural binary sequence from 0000 to 1111 in the first 15 clock cycles and then reset back to 0000 in the 16th clock cycle, before repeating the sequence again. A decade counter counts from 0000 to 1001 and then resets.

There are 'up' counters that count upwards, where every count increments the counter output, and there are 'down' counters where the counter output decrements with every clock pulse. There are 'presettable' counters where any predetermined logic input loaded onto the program inputs can be made to appear at the output when desired. The counters also have a 'clear' facility where the counter output can be reset to 0000 (in case of 4-bit counters) when necessary.

The majority of the popular counter ICs have all the above facilities built into them. There are selection pins from where you can select the counter mode (up/down, preset mode, clear mode). Construction of this simple project will enable you to have a feel of the different aspects of commonly used counter ICs. The counter chosen for the purpose is IC CD4510 that is a BCD decade counter that has the up/down, program and clear facilities.

Circuit Description

The heart of this circuit is a BCD decade counter (Type number: 4510) whose output is fed to another IC (Type Number: 4511), which is a decoder/driver IC – it converts the BCD output of the counter into a decoded output for the seven-segment display. For instance, initially, the counter output is 0000, the decoded outputs are such that the display segments a, b, c, d, e, and f are lit up to numeral 3.

With the help of switches SW8 to SW5, any desired logic input can be loaded onto the program inputs P1, P2, and P3 and P4. Logic '1' on the 'preset enable' input transfers the binary number preset on the program inputs onto the output with the occurrence of the clock pulse. In fact, all operations are performed with the occurrence of the clock pulse.

The clock here is a manual one and is generated by the micro switch followed by a debouncing circuit formed by NAND gates in IC-1.

The up/down count-mode control would count in the forward mode when this pin is applied logic '0'. For example, if the counter output (Q4 Q3 Q2 A1) at a particular instant of time is 1000, then the next pulse will make it 1001 if the counter is in the up mode and 0111 if it is in the down count mode.

Testing Guidelines

The project should be tested on the following lines:

1. Close switch SW9 to connect a 9V battery to the circuit. See that the LED-1 lights up, indicating the appearance of 9V after switch.
2. Keep switch SW2 to GND position and switch SW3 to

Component List

Semiconductors:
IC 1 CD4011
IC 2 CD4510
IC3 CD4511
LED 1 Red LED
DIS 1 LT543 seven-segment display

Resistors:
R1-R2 22K
R3, R9 470
R10 2.2K

Miscellaneous:
SW1 micro-switch
SW2-SW8 SPDT, 9V battery, IC bases 16-pin

Email your circuit ideas to:
svetlana.josifovska@stjohnpatrick.com

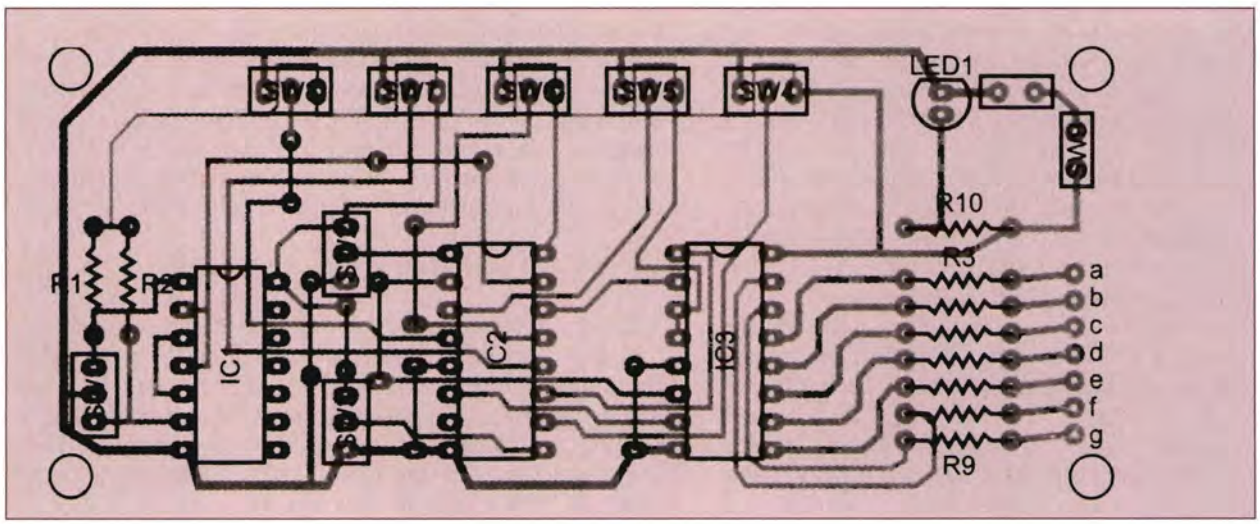
the 9V position. The seven-segment display should read '0'.

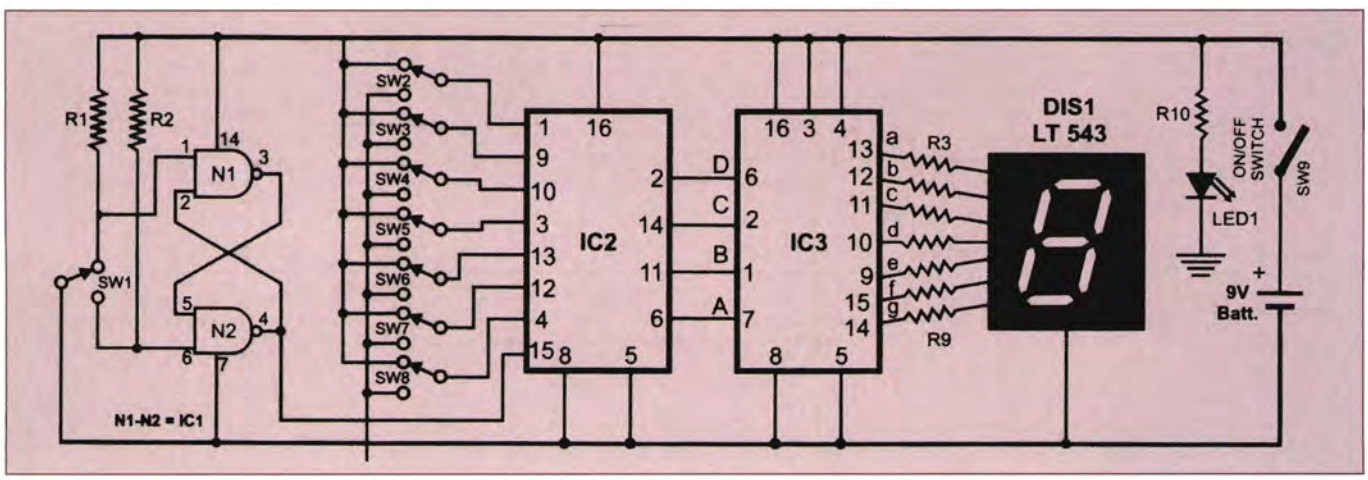
3. Change the switch SW3 to GND position. Keep switch SW4 at the 9V position thus selecting the up-count mode.
4. Now press the release of the micro switch SW1 once, thus sending one clock pulse. The display should read '1'.
5. Continue pressing and releasing the microswitch and you will notice that each clock pulse increments the seven-segment display by one digit. Continue this exercise until you have reached '9'. The next press-and-release operation will change the display to '0', indicating that the counter has been reset and that it has completed its one cycle.
6. Now change the switch SW3 position to GND. Give a clock pulse from the micro switch. The display will show '9'. This indicates that the counter has now started counting backwards because a forward counting would have taken the display to '1'. Reverse counting is justified as we have already selected the down count mode. The display reading corresponding to next four pulses will be 8, 7, 6, 5.
7. Next, select any count mode (up or down) and let the display be at any count. Change the switch SW3 over to the position 9V. You will find the display going to '0'.

   Once the switch SW3 is kept at the 9V position, the subsequent clock pulses have no effect on the display reading, which stays '0'.
8. Change the switch SW3 back to GND position. Change the switch SW2 to 9V position. Load any input to the program pins P1 to P4. Let us assume that P4 P3 P2 P1 are 0101. You will observe that the display changes to '5' on applying the next clock pulse.

Thus we have seen the functioning of all terminals one by one.

Raj Ghorkali
Nepal





HOW TO GET AN EXTRA PWM OUTPUT

A problem that occurs from time to time is how to control two motors from a single MCU, using two related PWM signals. Microchip's PIC16F616 14-pin MCU is an ideal device for motor control, but only has a single PWM output. So, how can two PWM signals generate when you only have one CCP module?

The solution lies in a technique called 'pulse swallowing'. The same PWM pulse is applied to both motor drivers. Evenly-spaced PWM pulses are then 'swallowed' (shorted out) on the drive that is running at the slower rate. **Figure 1** shows an example pulse chain and **Figure 2** shows an example circuit.

In this example (see below), motor B is initially losing every other pulse. This is achieved by RC3 being made to output a LOW during the pulse to be swallowed. When the pulse is to be passed to motor B, RC3 is tri-stated and the pulse passes through to the MOSFET driver and then to the output. Because the inertia of the motor acts as a low-pass filter, the missing pulses are mechanically averaged with the pulses that are present, effectively reducing the average duty cycle. In this example, the duty cycle of motor A is effectively twice that of motor B.

The trick is in shorting out specific pulses from the PWM. We start with the Timer2 interrupt, which fires at the start of every pulse generated by the CCP. In the interrupt service routine, a decision is made to swallow the pulse, or not, and the output is either driven low or tri-stated. However, the latency time of the interrupt and the variable nature of the determination function make it impossible to shut down the pulse accurately before it starts.

To overcome this, the interrupt service routine uses a flag, which passes from one interrupt to the next. If the flag is set, the routine shorts out the next pulse. If it is not set, the pulse is allowed to pass. By shorting out the pulse by using data from the last interrupt to start the 'swallow', and then making the determination for the next interrupt, the latency time is minimised and, more importantly, kept consistent.

Even when this interrupt-to-interrupt flag system is used, some portion of the pulse will be generated before the interrupt service routine can 'swallow' it. Fortunately, as can be seen in **Figure 3**, any portion of the pulse that is accidentally generated will be subtracted from the next pulse due to the same interrupt delay.

So far, we have seen how to short out evenly-spaced pulses and reduce the average duty cycle, but how do we determine which pulses should be shorted? This is easily achieved by adding an offset to an accumulator register at each interrupt. When this overflows, the next interrupt swallows a pulse. If the offset value is large, the accumulator overflows more often, resulting in a greater number of pulses being swallowed. If the offset is small, it takes longer for the accumulator to overflow and fewer pulses are swallowed. Listing 1 shows a pseudo code example of how this is implemented.

All that remains is to determine the value used in the offset. This is calculated using:

Offset = Full_duty_cycle – slow_duty_cycle

So, if the period is 200 cycles (0-199 counts) and the full duty cycle is 50 (0-49), with a full cycle of 45 (0-44), the offset is five counts. If five counts are added to the accumulator at every pulse, it overflows on every 40 pulses. Therefore, five evenly-spaced pulses out of every 200 are missing on the slower motor PWM, providing us with two PWM channels with one CCP.

Figure 1

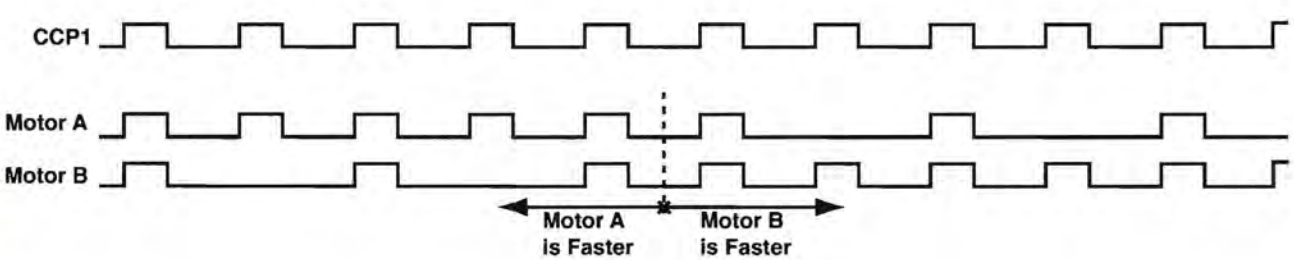
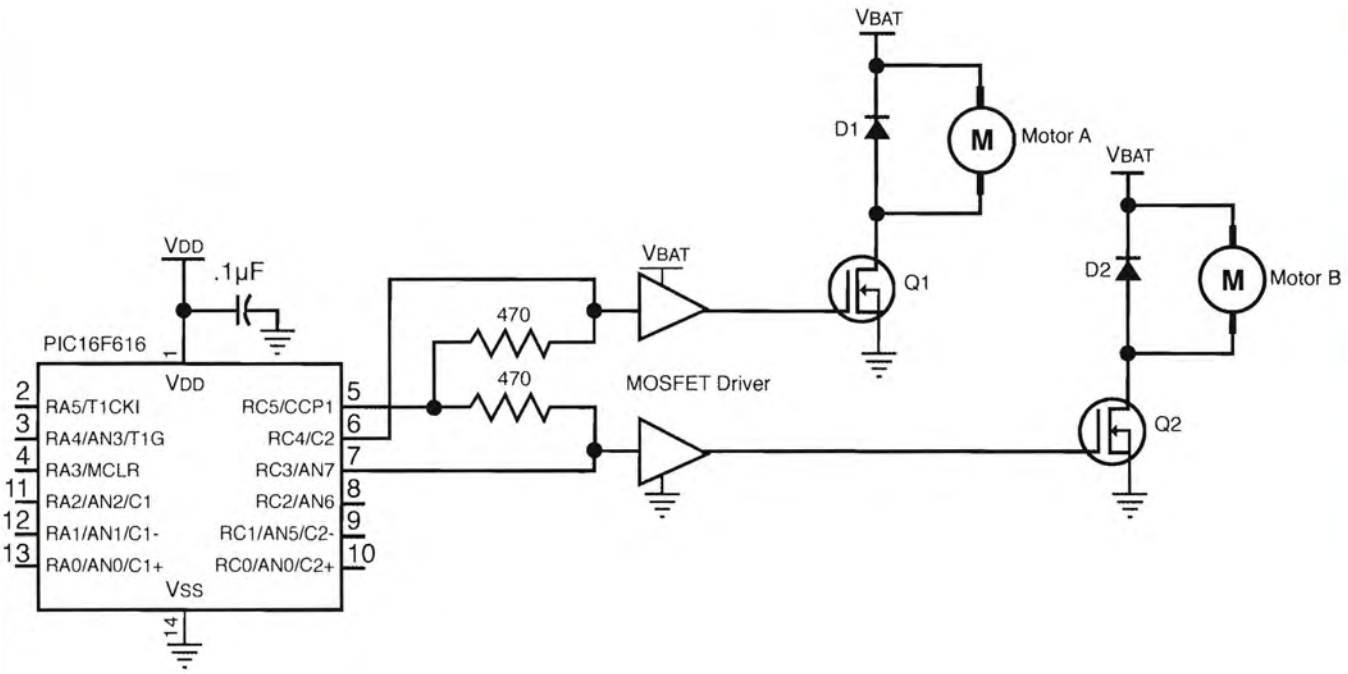


Figure 2



List 1

```
Accumulator = Accumulator + Offset
If (Accumulator > Period)                    /* an over flow condition*/
      Swallow_pulse_flag = true
      Accumulator = Accumulator - period
Else                                         /* no over flow condition*/
      Swallow_pulse_flag = false
Endif
```

FAST, SIMPLE ONE-SHOT PULSE STRETCHER DETECTS NANOSECOND EVENTS

by Cheng-Wei Pei of Linear Technology

Resolving fast events, such as pulses from a photodiode or transistor avalanche events, requires a detector with enough bandwidth to handle the pulse. The Linear Technology's LT1711 high speed comparator can switch in 4.5 nanoseconds in response to such events (because of its nanosecond rise time and propagation delay) but what if information needs to be relayed to a microprocessor or DSP that is unable to resolve such short-duration events? **Figure 1** shows a simple one-shot circuit that stretches any high excursion output into a 2.5 microsecond or longer pulse.

Circuit Description

The key to the circuit in Figure 1 is the latch function of the LT1711. Capacitor C1 (1000pF) conveys an output rising edge directly to the latch pin of the comparator. After a 1.5ns typical set-up time, the output of the comparator latches high and stays high until the resistor R1 (20kΩ) bleeds away the charge on C1, with a time constant of 20μs (R1 x C1). Once the voltage at the latch pin reaches its threshold voltage, the output unlatches and returns low until the next event occurs.

Figure 2 shows the comparator's output pulse (bottom trace) in response to an 8ns input pulse (top trace).

Figure 3 shows a zoomed-in version of both the input pulse and the comparator's output rising edge.

Figure 4 breaks down the events that occur at the output of the comparator as well as the voltage at the latch pin. Upon a rising edge of the output (A), the latch pin rises by the same voltage (B). When the latch pin decreases to the latch threshold voltage (C), the output switches low (D). This, in turn, imposes the same negative voltage on the latch pin, forcing it below ground (E). The 1N5712 Schottky diode prevents too large of a negative excursion. If this negative voltage on the latch pin is not given sufficient time to recover back to zero before the next event, the one-shot pulse width is reduced.

Measured Results

With a 3.3V supply, the measured one-shot interval (stretched pulse width) is approximately 8μs. Changing the values of R1 and C1 can alter that interval. Over temperature, with the variations of the latch pin threshold and Schottky diode forward voltage, the minimum pulse width can drop to about 2.5μs. Design this minimum pulse width to meet your minimum requirements by changing R1 and C1.

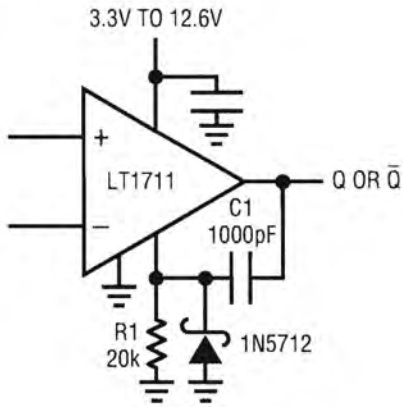


Figure 1: *A simple one-shot circuit with a high-speed comparator and three external components. Any event that triggers the comparator will cause the output to go high and stay high for a minimum of 2.5 microseconds*

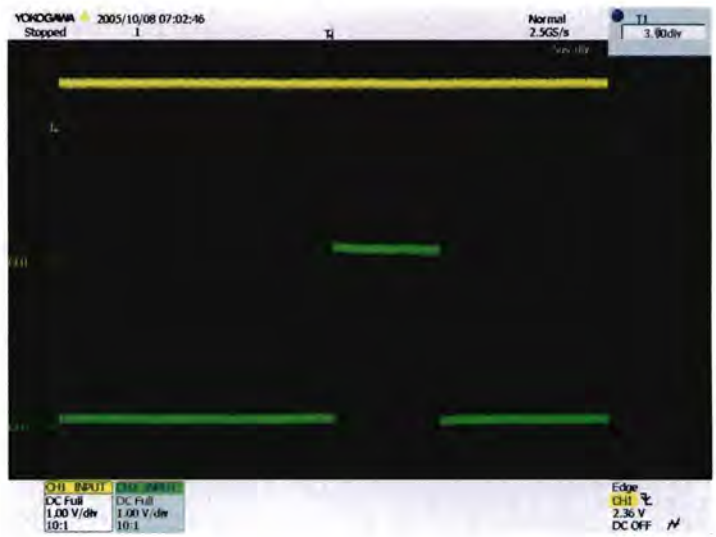


Figure 2: *Output of the comparator in response to a 8ns pulse at the input. Pulse length is approximately 8 microseconds*

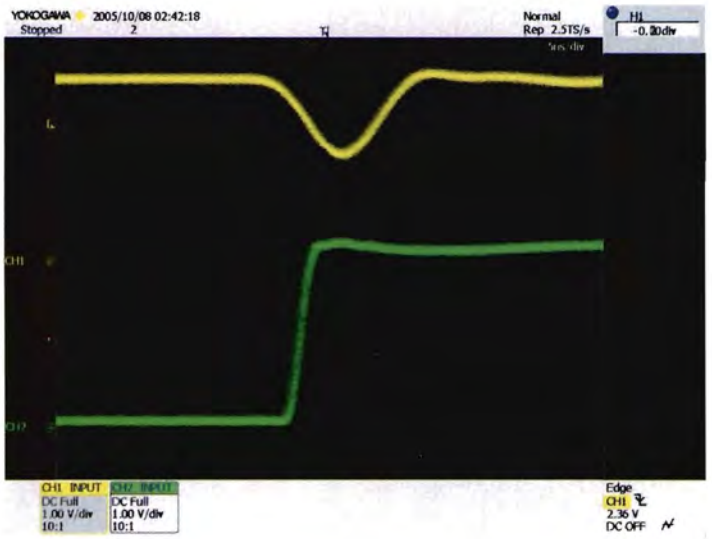


Figure 3: *Zoomed-in view of the input pulse (top) and the comparator's output rising edge (bottom)*

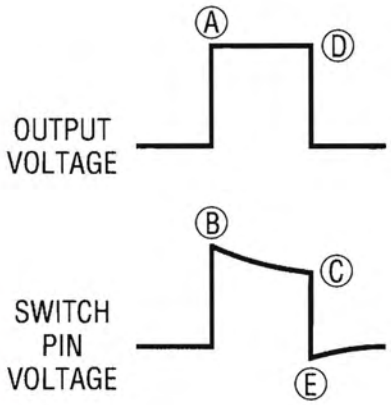
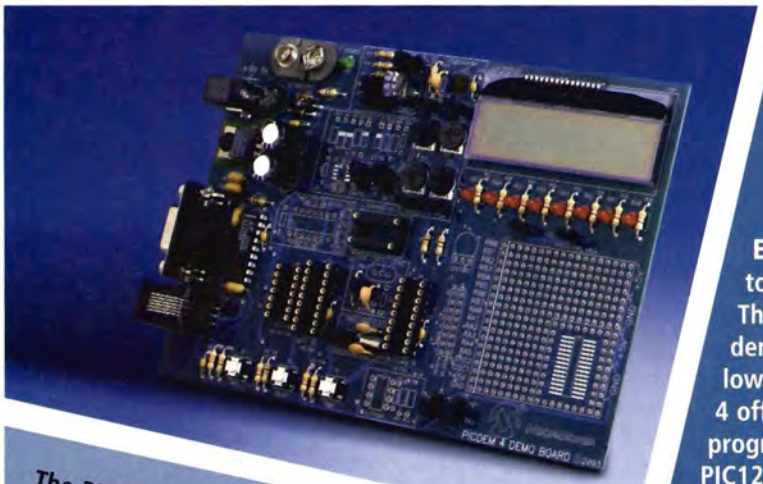


Figure 4: *Diagram of output voltage and latch pin voltage in response to an input event*



Win a Microchip PICDEM 4 Demo Board!

Electronics World is offering its readers the chance to win a Microchip PICDEM 4 Demonstration Board. The Demo Board helps engineers to evaluate and demonstrate the advanced capabilities of Microchip's low pin-count PICmicro Flash microcontrollers. PICDEM 4 offers multiple socket options for immediate programming and debugging of 8-, 14-, and 18-pin PIC12F, PIC16F and PIC18F microcontrollers. The board demonstrates many of the features of low pin-count parts, including Local Interconnect Network and motor control capability using the enhanced capture/compare/PWM module. Low-power operation is achieved with a supercapacitor circuit and jumpers allow the on-board hardware to be disabled to eliminate current draw. It also includes provision for crystal, RC or canned oscillator modes and a 5-volt regulator for use with a 9-volt supply, or hooks for a 5-volt, 100 mA regulated DC supply. Additional features include an RS-232 interface, an EEPROM footprint, 2x16 liquid crystal display, PCB footprints for an H-Bridge motor driver, LIN transceiver, and a connector for programming via In-Circuit Serial Programming technology and developing with the MPLAB ICD 2 in-circuit debugger.

The PICDEM 4 Demonstration Board includes two PICmicro Flash microcontrollers and a CD-ROM containing sample programs, application notes and user guide. The MPLAB ICD 2 is available as a stand-alone unit and Microchip's MPLAB IDE (interactive development environment) software can be downloaded for free from Microchip web site.

For the chance to win a PICDEM 4, log onto www.microchip-comp.com/ew-picdem4 and enter your details into the online entry form.

Packaging audits made-to-measure

Protective packaging specialist Interactive Packaging Solutions (IPS) is keen to engage with customers on improving all aspects of their transit packaging systems. The company has over 30 years' experience of providing companies with protective packaging solutions, in materials ranging from advanced protective foams to simple corrugated cardboard and composites, and is well placed to advise customers from many industrial sectors and to provide practical long-term solutions, adding value to the total product handling process.

IPS packaging audits look at the effectiveness of current packaging activities and how these can be improved. Examples may include: reconciling the sometimes contradictory aims of the protective and promotional aspects of packaging; resolving design issues with flexible in-house resources to reduce tooling and set-up costs, as well as improving lead times; and assessing the suitability of current packaging materials. To arrange an audit of your companies transit and protective packaging procedures, visit IPS

www.ips-uk.co.uk

HiTek Power launches X-ray power supply short-form

HiTek Power has published a new short-form catalogue summarising details of its wide range of X-ray power supplies and its custom capability in this field. HiTek's eight standard families of X-ray supply offer output powers from 50W to 2kW and the company's 30 years of experience in this market enable it to offer unrivalled capability in the custom design of systems for industrial and scientific equipment.

HiTek Power's X-ray power supplies offer maximum output voltages up to 90kV and are offered in variants that can be powered from the mains or a DC input. They incorporate features such as tube protection, short-circuit and overload protection, high stability and low ripple. High-accuracy filament control is incorporated into some models, as is the option of an analogue or RS232 interface for monitoring and control.

HiTek Power's X-ray power supplies are used in many areas, including industrial X-ray checking and inspection systems, X-ray diffraction (XRD) and X-ray fluorescence (XRF) analysis as well as in food inspection systems.

www.hitekpower.com

Power Supply Family with Better Energy Rating

SL Power Electronics has announced a new family of 70W external switch-mode power supplies. The Ault PW174 series is single output with a power range of 40 to 70W, available in seven voltage models.

As an Energy Star partner, SL Power Electronics Corporation launched the specification for Energy Star-qualified external power adapters in January 2005 to address the growing energy consumption by a proliferation of consumer and office electronic products requiring power adapters.

The Ault PW174 series is a low-cost option for leading OEMs in the data communications, telecommunications, or ITE markets. Priced at $18 in OEM quantities of 1000, the Ault PW174 gives users added versatility because it is available in 5, 9, 12, 15, 18, 24 and 48 Volt models. The PW174 single output series is available in a desktop style up to 70W.

The CE-compliant Ault PW174 meets UL60950-1, IEC/EN60950-1 and EN55022 /55024 61000 to help reduce OEM product design-to-production cycle time. In addition, the efficiency level meets Energy Star and EU COC guidelines. All Ault PW174 models have low output ripple and a three-year warranty. SL Power Electronics also offers modified and custom designs to meet specific OEM requirements and private label marking needs.

www.slpower.com

Spectrum Analysers with Digital Demodulation

Ideal for wireless design, research and development and production test engineers, the Aeroflex 3280 Series spectrum analysers now offer digital demodulation for the analysis of 802.11a, b and g wireless networks.
Digital demodulation in the 3280 Series is easily operated in one of two modes. Full-frequency mode links the rear panel IF output at 421.4MHz to the demodulator input, allowing the user to demodulate signals over the full frequency range of the spectrum analyser (3GHz, 13.2GHz or 26.5GHz). The frequency range for the direct input of the demodulator is 300MHz to 3GHz.
Although the 3280 Series's digital demodulation hardware option does not include direct I/Q outputs, users who require it can access a direct digital I/Q output in streaming serial format by adding the optional low-voltage data signal (LVDS) output cable. This optional cable is fitted internally between the demodulator LVDS output and the spectrum analyser rear panel.

The systems' accuracy is ±0.15dB up to 3GHz. Other performance features include an excellent local oscillator (LO) phase noise < -115dBm/Hz, 1GH/10kHz offset and +18dBm third order intermodulation performance. Digital intermediate frequency (IF) offers resolution bandwidths from 5MHz to 1Hz.
www.aeroflex.com

New Version of SPICE from Kemet

Kemet has released an improved and updated version of its Simulation Program for In-Circuit Emulation (SPICE) software. The package allows design engineers to simulate the effects of Kemet capacitors over frequency, temperature and bias, helping them to determine the most appropriate device for their application.
The latest version of the SPICE software introduces several new features, which allow designers to view and compare responses for up to ten different part types at one time, build a complex filter by selecting multipliers for each part type involved and then see the cumulative impedance response for all elements combined, view the effects on one device at multiple DC bias conditions or multiple temperatures (up to ten each) and see voltage coefficients for MLCCs.
In order to maximise flexibility and ease of use, the SPICE modelling software has been designed such that it can combine capacitors of different chip styles and dielectrics in a single analysis.
Kemet's SPICE software can be accessed via the home page of the company's website.
www.kemet.com

20A DIN-Rail Power Supply Eliminates Inrush Current

Puls introduced its latest model in the Dimension Q series of DIN-rail power supplies. The QS20.241 provides 24VDC at 20A from a 85-276V wide range AC single-phase input and is 1/3 the size of other comparable DIN-rail power supplies.
The QS20.241 uses synchronous rectification topology and digital control to reduce the size of the unit but also improve efficiencies to 93.9%, significantly reducing heating effects and overall energy consumption. The design also provides 150% peak load capacity for load peaks such as motor starting and virtually eliminates start-up inrush current which reduces system cabling, fusing requirements and general over sizing of the power supply. Further, the unit will start up at -25°C and work at full rating through to +70°C making the power supply suitable for very harsh environments including outdoor control cabinets.
Other features include active power factor correction, LED status indicators, DC input from 88-375VDC, DC-OK relay contact, high reliability quick-connect spring-clamp terminals and a three-year warranty. With dimensions of just 82 x 124 x 127mm an N+1 redundant power system will now only take up the same space as an existing single, unsupported, power supply.
www.puls.co.uk

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Leading supplier of advance solutions and service in wire, cabling and tubing, Alpha Wire International, has announced the launch of a new website dedicated solely to its range of hazard-matched cables, XTRA•GUARD® that provide extreme performance for extreme environments. The new website www.xtraguard.com represents an industry first for a website dedicated solely to a single brand of cable. The site offers an intuitive selection aid to help engineers correctly specify cable for their

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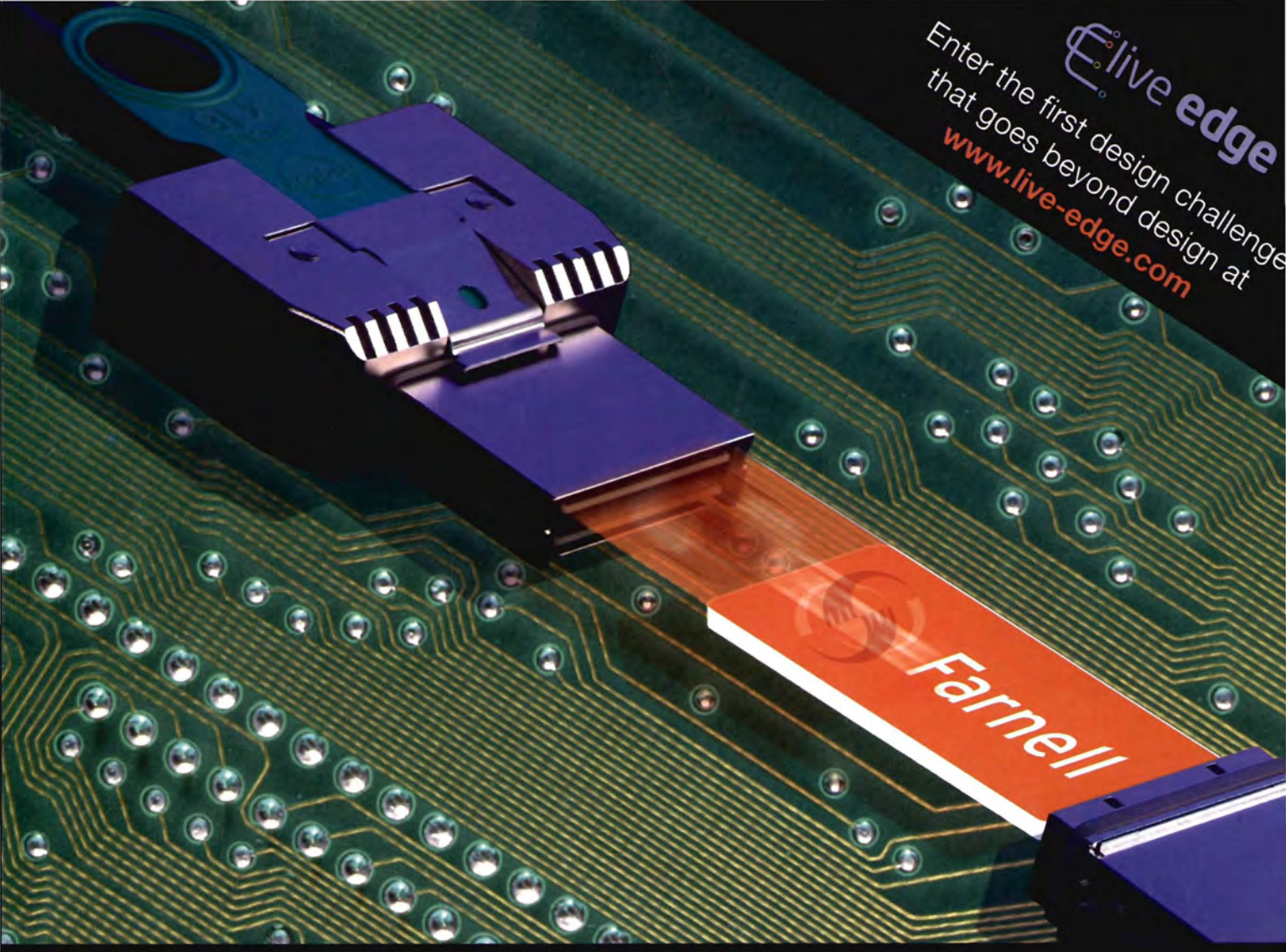

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