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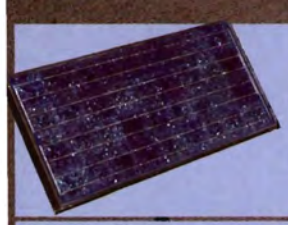

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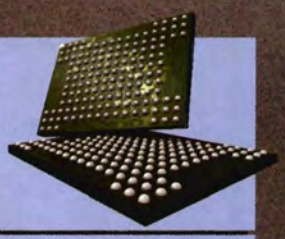

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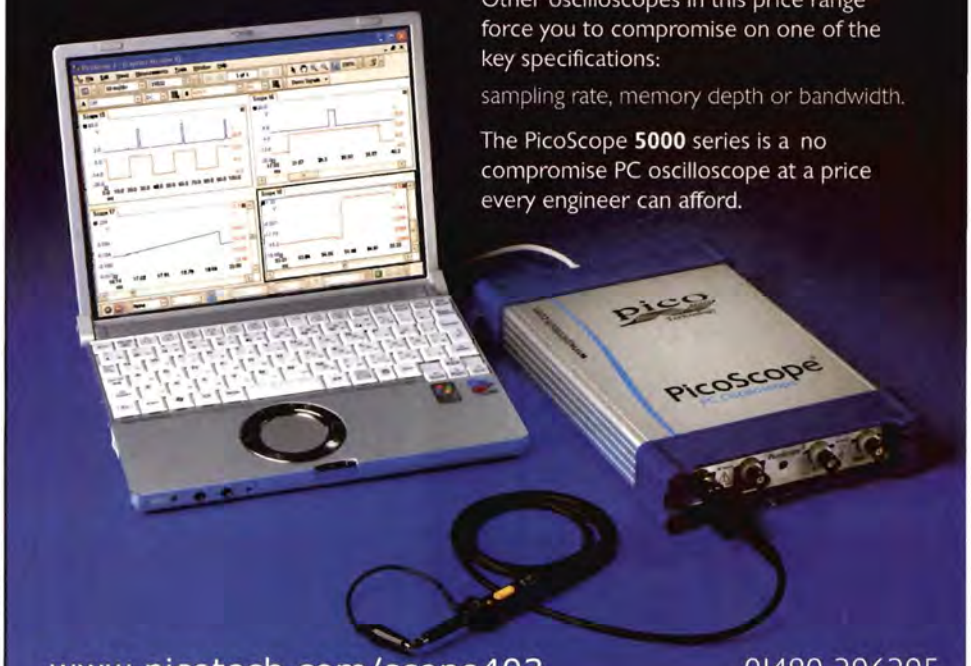

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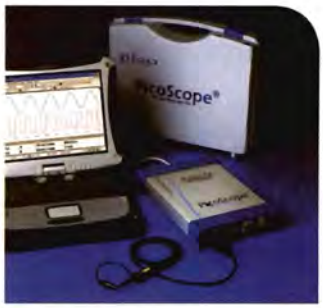

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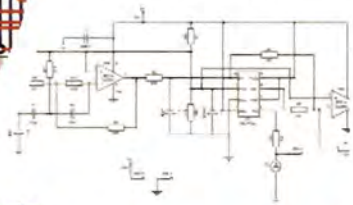

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Books, books and more books!

Dear Readers,

It's that time of year again when we have a new selection of technical books for reviewing. Please have a look at the choice below and if interested in any of them send me an email at **svetlana.josifovska@stjohnpatrick.com** stating the book's title. The way book reviewing normally works is that you initially register your interest in the book of your choice, but please do so as quickly as you can as we send the books on a 'first come, first serve' basis.

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Svetlana Josifovska
Editor

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Semiconductor players are going fab-lite and gut-less, says analyst

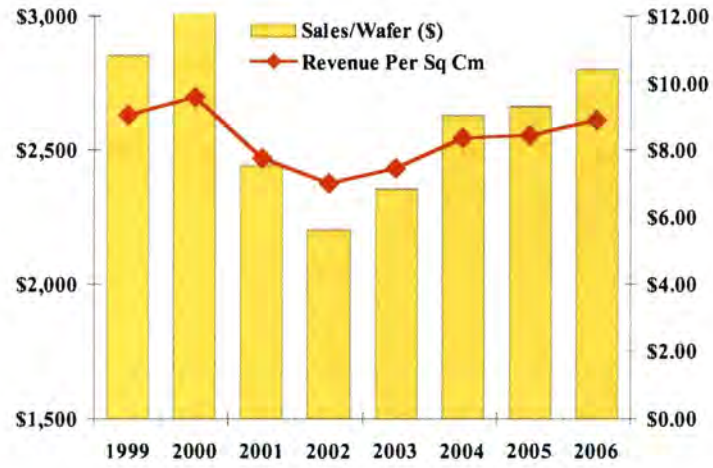
The current trend among semiconductor makers, starting with European firms ST Microelectronics, NXP and Infineon, is to go fab-lite. This means that after a certain process node, say after 65nm, they are going fabless and their semiconductor devices will be manufactured by one of the independent, giant fabrication facilities in the Far East.

This trend, however, has been severely criticised by Malcolm Penn, chairman and CEO of industry analyst house Future Horizon, who's been involved in this business for over thirty years. "We are still very much in a cost-driven engineering business, where profitability is $8 per cm^2, even though it takes only 90 cents to make it. We are selling technology on an acreage basis!" he said. "There's so much room to manoeuvre and play the prices, before you even start thinking you're going to lose money. So it goes as a counter-argument to 'should I have a fab'."

According to Penn, typically 18-21% of revenues of a large semiconductor company go into building a fab. He says: "This is the exact same percentage it took in the 70s, in the 80s and 90s. It's just that we've lost the stomach for it. In the 70s we used to joke that, with the fab you bet the company. Nowadays you can't say that – nobody is betting their compa-nies any more."

Predictions are that at some point in the future, once the bigger players decide to place all of their orders with the semiconductor fabs, the semiconductor business landscape will be entirely different. We will see less differentiation in devices, but potentially also the demise of technology R&D hubs the likes of IMEC in Belgium. "IMEC is feeding the technology infrastructure [in Europe], but what happens when its customers go fabless?! It'll be a significantly different semiconductor world in Europe [in the future] than it was ten years ago," said Penn.

Industry profitability – '$8 per cm^2'



Second generation serdes offers innovations

Fairchild Semiconductor has launched its second generation serialiser/deserialiser (serdes) device, part of the µSerDes family, which offers much lower power than other devices through several innovations.

For a start, the firm's designers removed two internal phase-locked loop (PLL) timing circuits in this device – the FIN324C. The first PLL was initially cut out in the deserialiser two years ago in Fairchild's first serdes generation. "In the second generation we came up with the innovative technique to eliminate the second PLL. This removes the need to use external clocks, which in turn lowers the device's power consumption," said Mike Fowler, technical staff at Fairchild.

"Dynamic power does not depend on the frequency, but on the [clock] edges. For our design this meant significant power savings as we eliminated the PLL." According to Fowler, with a current consumption of around 4mA at 5.44MHz, the FIN324C offers at least a ten-fold power saving on other solutions currently on the market.

Instead of using clock edges to mark the data word flow, Fairchild applied edges to the data itself. "We stopped the clock edge but added edges to the data – this is unique in our industry," said Fowler.

Fairchild has also applied a proprietary differential signalling I/O technology to lower the 24 or 12 LVCMOS signals in designs to a serial signal. "Our differential I/O was unique in the industry. We sensed the current direction which allowed us to lower the voltage – now at nearly 100mW. The current is 1mA, which is a lot lower than a standard LVDS at 2.5mA," said Fowler.

In addition, the serdes device supports dual-displays – helping designers to save battery power and reduce part count in applications.

InGaAs HEMT transistors could replace silicon devices

In preparation to silicon reaching its performance limits within fifteen years, the MIT Microsystems Technology Laboratories have applied indium gallium arsenide (InGaAs) in transistors, since it offers much higher electron mobility than silicon.

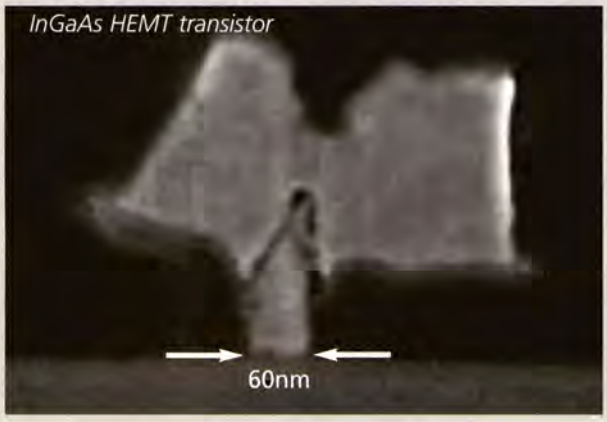
The devices could be potential successors to silicon transistors in fast logic ICs.

Although InGaAs can be used in High Electron Mobility Transistors (HEMTs), they have previously been limited to MOSFETs with gate lengths of about 100nm. A much thinner InAlAs barrier layer helped to form devices with a length of only 60nm, somewhat similar to the most advanced 65nm silicon technology currently available. The resulting devices carried up to three times more current than the present state-of-the-art silicon transistors, and at a supply voltage of only 0.5V.

However, according to Professor Jesus del Alamo of the MIT's Laboratories, InGaAs transistor technology is still in its infancy. He said: "Unless we do something very radical quite soon, the microelectronics revolution that has enriched our lives in so many different ways might come to a screeching halt."

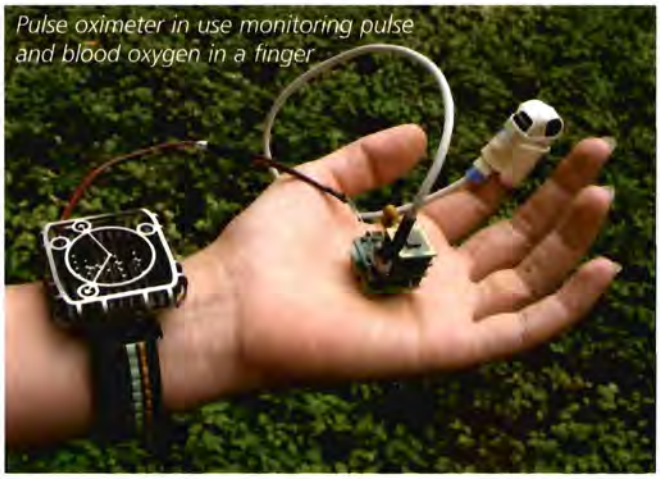
He admitted that manufacturing InGaAs transistors in commercial quantities presents many challenges, as this material is far more easily fractured than silicon. However, he said that with more work, the technology of this material could greatly surpass silicon.

Del Alamo forecast that prototype InGaAs devices of the required dimensions for use at microwave frequencies will be developed within the next two years and that the technology will generally take off commercially within the decade. Intel was among the sponsors of the work.



InGaAs HEMT transistor

IMEC develops medical sensor powered by body heat


Pulse oximeter in use monitoring pulse and blood oxygen in a finger

IMEC, the Inter-University Microelectronics Centre in Leuven, Belgium, has built a device whose power is obtained from the heat of the human body.

The system uses a wireless pulse oximeter sensor for the non-invasive monitoring of the pulse and oxygen levels in the blood, and a thermoelectric generator which contains some 5,000 thermocouples. It is based on the IMEC 'system in a cube' technology and is combined with a thermoelectric energy scavenging system that is integrated into a device similar to a wrist watch.

All of the signal processing is carried out in a three-dimensional sensor cube, which requires only 5% of the system power needed for the radio transmission. A measurement can be made every 15 seconds, with a 26% duty cycle, in which case the entire system consumes only 89µW. This is well below the 100µW that the thermoelectric generator can produce at an ambient temperature of 22°C in the worst possible case of a person undergoing a minimum of physical activity. A small coin-type supercapacitor can be used as a temporary energy buffer to supply any peak current that may be needed. In conjunction with a surface-mounted tantalum capacitor, the need for a battery is thus completely eliminated.

The device is claimed to be the first complex biomedical sensor that is fully powered by the heat of the human body. It serves as a 'proof of concept' for devices for use in many other fields.

It is expected that the use of wireless sensor nodes will grow as an invasive technology within the next ten years, but it is not economic to have a large network of distributed sensors that all need regular recharging.

Toshiba Corporation, Shibaura Mechatronics and Chlorine Engineers have worked together on an environmentally-friendly semiconductor resist stripping technology used in IC fabrication.
The new technology uses electrolysed sulphuric acid and allows it to be recycled. It also eliminates the use of hydrogen peroxide. The new process is more efficient than the previously used one and contributes to improved productivity by shortening resist stripping time by 20%.
Resist is a masking material used in the lithographic process that forms semiconductor circuits on a chip substrate. Once circuits are etched, the resist must be removed, which is typically done with peroxymonosulphuric acid, produced by mixing sulphuric acid with hydrogen peroxide.

* * *

Showa Denko KK (SDK) has developed a new process for making high-quality compound semiconductors based on gallium nitride (GaN) and other nitrides to meet growing demand, mainly for use in blue and white LEDs. The new process, named the "Hybrid PPDTM" is a combination of the conventional metal organic chemical vapour deposition (MOCVD) process and SDK's proprietary plasma-assisted physical deposition (PPDTM) process for growing nitride-based semiconductor crystals.
With the same process SDK also succeeded in developing blue LEDs with one of the highest-level brightness around. SDK will start commercial shipments of these blue LEDs this year.

* * *

IBM, in cooperation with Sony, Toshiba and AMD, has announced that it has found a way to construct a critical part of the transistor with a new material, called "high-k metal gate," which controls the transistor's primary on/off switching function. The material provides superior electrical properties compared to its predecessor, enhancing the transistor's function, while also allowing the size of the transistor to be shrunk beyond limits being reached today.
Equally important is that this technology can be incorporated into existing chip manufacturing lines with minimal changes to tooling and processes, making it economically viable.
This is the first fundamental change to the basic transistor in forty years and it is expected to lead to a whole new generation of chips.

Solar panels threaten the semiconductor industry

Malcolm Penn, CEO and chief analyst of the UK-based market research firm Future Horizons, predicts that the semiconductor industry will see a 12% market growth this year.

However, one blemish in the business could be the supply of polysilicon, which is used in substrate fabrication, and which now has to be shared with the increasingly demanding photovoltaic industry that uses it heavily in the production of solar panels.


The PV industry is growing at a very high pace

"A thing we should worry about this year is the supply of polysilicon," said Penn.

Although the semiconductor industry continues to grow steadily, the PV industry is growing even faster, threatening to eclipse the semiconductor market.

"Solar [panel production] used to be a by-product – now it isn't," said Penn. "It's as big as the semiconductor market and it grows twice as fast. Not only that, they [the PV firms] are prepared to pay decent prices for polysilicon. This has an effect on ramping up the prices of wafers as substrates increase in price."

Last year, the total market for polysilicon was 42,000 tonnes, 18% up on year 2006. The average sale price of 'solar grade' silicon jumped from $45 per kilogram in 2005 to $60/kg this year.

Germanium on insulator used to better performance of CMOS

Following the success of Silicon on Insulator (SOI) and strained SOI (sSOI) in CMOS, a collaborative work in France between Soitec, CEA/LETI and ST Microelectronics has now investigated the use of Germanium on Insulator (GeOI) to improve its performance.

GeOI offers high mobility charge carriers, combined with the advantages of a layered structure like that of SOI. Its low lattice mismatch with gallium arsenide enables optoelectronic products to be integrated onto GeOI wafers, as can transistors consisting of III-V compound semiconductors.

Sub-micron fully depleted MOSFETs on GeOI have shown that the material can be used at the 32nm node technology and beyond. Functioning n-FETs on GeOI have been demonstrated, with better n-channel mobility enhancement than those for p-channel.

The researchers say that germanium is not just a high mobility material, but its optical absorption coefficient is attractive for photodetectors and other optoelectronics applications. Furthermore, the small lattice mismatch with gallium arsenide enables high quality III-V epitaxial layers to be monolithically integrated with silicon and this should open the paths to future high-performance electronic and optoelectronic applications.

Wafer-level GeOI structures can be cut into various diameters and thickness ranges down to less than 50nm, and there's a potential to move to 300mm wafer diameters or above.

HYMNE project tackles need for high yield

The High Yield driven Manufacturing Excellence in sub-65nm CMOS project, known as HYMNE, aims to develop software and hardware methods to enable chipmakers to shorten production cycle times and improve device yields for sub-65nm devices. This will be achieved through increased automation and the use of new materials.

Increasing miniaturisation means that electronic devices are becoming ever more difficult to produce competitively at industrial levels, a problem which is especially acute in Europe where much semiconductor manufacture focuses on short run, application specific devices (ASICs) in a wide range of technologies.

The Medea+ HYMNE project is thus set to develop methods, software and hardware that will enable chip makers to shorten production times and improve device yields. This will result in significant gain in competitiveness in advanced technology manufacture, thus boosting global sales and improving European employment prospects.

HYMNE sets out to show cycles can be shortened for the latest generation of sub-65nm devices with yields of over 78% within 13.5 months of the first silicon. It aims to reduce cycle times from two to one day per mask layer and from 0.75 to 0.35 of a day for fast prototyping in an operating 300mm plant. It also intends to attain an additional 5% cut in defects, as well as yield increases in the mature production stage.

The supply of new materials and contamination-free wafer handling is important to reduce the time for the integration of new process modules, materials and chemistry for sub-65nm CMOS production in high volume chip production. Facility development and tool cleaning procedures to reduce wafer contamination are required. New material precursors and slurries for chemical mechanical polishing will be developed, validated and delivered with appropriate quality for 65nm and 45nm technologies. Zero defect and advanced yield learning will involve the examination and elimination of systematic and random defects for sub-65nm technologies that could affects yields.

The project runs from February 2005 to December 2008 under the leadership of Joost van Herk, Philips, involving over 20 partners.

CSR supports front end unification

Cambridge Silicon Radio (CSR), the largest supplier of Bluetooth chipsets, wants to simplify the functionalities of mobile phones, by combining several front ends into one.

"By 2012 some 300 million cellphones will be enabled with Wi-Fi. Today, users switch the Wi-Fi functions off on their phones because they waste a lot of battery. Therefore, some of the functions in the phone will need to be combined to make it easier for users," said Simon Finch, head of the Wi-Fi business unit at CSR.

CSR's latest launch is the UniVox Mobile reference design which contains all the additional hardware and software to wirelessly enable mobile handsets for making Voice over Wi-Fi (VoWi-Fi) calls. The hardware element of UniVox Mobile is based on UniFi, CSR's single chip Wi-Fi solution, and also includes the Bluetooth functionality.

UniVox Mobile also allows Wi-Fi to be used as the bearer for other services, such as web browsing and multimedia streaming.

Within a decade the Internet will be able to deliver smells as fast as it does data, says a report produced by the South Korean government. The technology experts panel behind the report said that, by 2015, the Internet will be used to deliver data about smells to a fragrance cartridge sitting next to a computer or other device accessing the Internet.

The report also predicted that by 2012 batteries in mobile phones will last up to two months between recharges and that by 2018 robots will be routinely carrying out surgery, some of which tiny enough to be injected into the human body to find and heal health problems they come across.

* * *

Texas Instruments and Ideaworks3D will cooperate on extending the capabilities of the OMAPT Gaming Platform to support the OpenKODE 1.0 specification for high-end multimedia handsets. This platform is deemed one of the first in the industry to incorporate the OpenKODE Khronos Open Development Environment to further simplify the development and deployment of new games across multiple mobile phone segments, creating a larger market opportunity for game publishers.

* * *

Visitors to fast food outlets in Japan will soon be able to pay for their burgers with their mobile phones. Japanese mobile phone operator NTT DoCoMo has teamed up with McDonalds to offer electronic payments and special promotions for mobile users as of July this year. The joint venture between the two firms is worth 300 million yen, where McDonalds Japan holds a 70% stake and DoCoMo the rest.

Using mobile phones to pay for goods is an enormous growth area as operators look for new ways to make money. Japanese mobile owners are leading the way, paying for food and train tickets via their handsets already.

DESIGN TROUBLESHOOTING

ⓘ Capturing elusive glitches:

In high-speed digital designs, elusive glitches and random anomalies can cause circuits to fail. While finding these glitches has never been easy, the task is greatly simplified by using oscilloscopes with a 'peak detect' feature. This determines the highest and lowest values of captured signals for each sample interval and which then displays all the samples between the two values. As a result, the user can see any extremes that occurred during the sample interval: in particular, narrow glitches, even when they occur on low-frequency signals.

ⓘ Debugging digital timing problems:

Digital designers need to quickly find and analyse a wide range of circuit timing problems such as race conditions and transients, which can cause circuits to perform inaccurately. Here, a versatile oscilloscope technique known as 'pulse width trigger' can help to troubleshoot such situations by triggering when a signal pulse width is less than, greater than, equal to or not equal to a specified pulse width.

The 'less than' pulse width trigger is one of the fastest ways of finding suspected transient pulses on a bus or device output, while the 'greater than' trigger can help to find 'stuck bits' and other signals that fail to return to their default state after some transaction. The 'equal to' trigger offers an alternative to voltage threshold triggering approaches when the available trigger signals (such as output enables) are affected by transients or noise.

ⓘ Verifying timing relationships:

Electronics engineers often need to verify that their circuits are working as designed. One of the most common types of oscilloscope measurements are timing measurements, such as pulse width, period and frequency. Such measurements are very straightforward as a result of the on-screen cursors used on the modern instrument.

Making timing measurements is simply a matter of pressing the 'cursor' button and selecting 'time' from a menu of parameters. To measure the timing relationship between two signals, one cursor is placed on the first edge of interest and the second cursor on the second edge, at approximately the same voltage. The cursor readouts indicate the timing of the cursors relative to the trigger point.

ⓘ Checking signal integrity:

A wide array of unintentional electrical events will make a difference in how circuits function in the real world. To characterise these events, engineers can measure criteria such as overshoot, ringing, ground bounce, crosstalk and other signal-integrity issues. Again, the use of on-screen cursors and automatic measurement modes makes such measurements very straightforward.

To make a signal-integrity measurement such as peak ringing below ground using cursors, the 'amplitude' mode is selected. One cursor is placed at 0V and the other on the negative peak, and the absolute voltage measurements appear on the cursor readouts at the side of the display.

ⓘ Debugging digital system lock-up:

One common cause of digital system lock-ups is an intermittent clock. The versatile triggering systems used in modern digital oscilloscopes can quickly and easily identify unexpected interruptions in the clock signal. Again, this involves a straightforward menu system to select pulse triggering and adjust the timing and pulse width to the appropriate levels to capture the clock signal.

ⓘ Checking unintentional circuit noise:

Developers need to check for unintended noise in their prototypes. However, noisy signals can be difficult to analyse in the time domain. As a result, many engineers and technicians use the Fast Fourier Transform (FFT) to break down signals into component frequencies. The oscilloscope can then display a graph of the frequency domain of a signal rather than the standard time-domain graph. Developers can then associate these frequencies with known system frequencies such as system clocks, oscillators, read/write strobes, display signals or switching power supplies.

ⓘ Power-line harmonic analysis:

Power circuit designers often need to analyse the effects of their circuits on the power line. Although an ideal power supply would present a constant load on a power line, real power supply circuits do not, and create harmonics on the power line. Simple oscilloscope-based tools are now available to measure power supply currents and analyse the harmonics on a power line.

To display power-line harmonics on a current waveform, menu controls are used to select current-probe support and the appropriate current-probe scale factor.

Built-in mathematical software allows FFT techniques to be used for measuring amplitudes accurately. The FFT display provides a frequency-domain display of the power-line signal, including the fundamental power-line frequency and the harmonics at integer multiples of the fundamental frequency.

ⓘ Documentation of results:

Design engineers in the laboratory and technicians in the field often need to document the work they do with oscilloscopes. Traditionally, screen images have been saved to a removable memory device and the files manually copied to a PC. These tasks are now greatly simplified by easy-to-use OpenChoice Desktop software which directly transfers screen images to a PC over a USB connection. The oscilloscope will copy the image to a clipboard from which it can then be pasted into the appropriate documentation program.

ⓘ Waveform measurement logging:

A common task for engineers and technicians is to make measurements on an oscilloscope and then manually record these measurements to document circuit performance variations over time. However, this is a time-consuming process and can lead to inconsistent quality of documentation. This is another area where the PC connectivity via a USB link can be put to good use.

ⓘ Waveform analysis:

Although modern digital oscilloscopes provide significant on-board analysis capabilities, there are applications where the analysis requirements are better met with PC-based applications. For example, the National Instruments SignalExpress software can be used to provide advanced PC-based analysis capabilities with the 'plug and play' ease of use of the USB interface.

Using this facility simply involves connecting the oscilloscope to the PC using a USB cable and then launching the SignalExpress program. The software will then open with the instrument automatically connected and transferring data to the PC.

This combination of OpenChoice PC and SignalExpress software provides quick and easy capture and storage of waveform data and images directly onto a PC, as well as providing the ability to generate reports with Microsoft Word and Excel and with software-specific interactive windows.

This month's Top Ten Tips were supplied by Trevor Smith, EMEA Market Development Manager for Oscilloscopes and Signal Sources at Tektronix.

If you want to send us your top five or ten tips on any engineering and design subject, please write to the Editor at svetlana.josifovske@stjohnpatrick.com.

Think Closer to Home

The recent trend to outsource the manufacturing of electronics overseas has had a significant impact on the UK EMS industry. **Martin Woodburn**, Managing Director of Endmoor Electronics insists that there is a future for the EMS market in the UK and explores the benefits of outsourcing closer to home rather than overseas

Increasing levels of competition in the electronics industry has led to a growing number of firms outsourcing their manufacturing activities on a much larger scale. And why shouldn't they? Contract manufacturing is proven to save on product costs and offers further benefits to OEMs, such as improved efficiency, cost reduction, flexibility and faster time to market whilst allowing companies to concentrate their internal efforts on developing their core competency areas of expertise, such as product marketing and development.

However, the rush to find someone somewhere else that does it much cheaper has meant that more and more companies are turning their attentions overseas instead of investing in UK businesses. This, as we all know, has had a profound impact on the high volume manufacturing industry in the UK, which inevitably has witnessed a severe decline as companies continue to seek low-cost solutions from Eastern Europe and the Far East to fulfil their high level requirements.

This outlook on the benefits of outsourcing overseas is, however, naive and short-sighted. Although the knowledge that offshore outsourcing may be cheaper can be an attractive prospect, it is also necessary that decision makers are made aware of some of the risks, as mistakes can be very damaging, especially if they impact directly on customers. By completely outsourcing manufacturing, companies risk losing valuable technical support and product knowledge.

The highly competitive electronics market at the moment has meant that time to market is a significant driver to a company's overall success. After all, development time has a direct impact on the revenues and profits they generate. OEMs want products out very quickly and look for swift turnarounds and flexibility in the production process from contract manufacturers. UK EMS providers have the advantage of being able to provide immediate access to deal with short-term schedule changes, improvements and modifications, thus making them generally more flexible to orders and market demands.

In comparison, foreign EMS providers require far more forward planning to accommodate large orders and, consequently, design changes can impact heavily on lead times. A continuously open channel to communication is a considerable strength of UK EMS suppliers, something which can't always be guaranteed by distant centres, particularly if you take into account the difference in time zones in areas such as the Far East. Imagine if a critical issue

arises and you're unable to address it due to the fact that the Far East sleeps, this could potentially have serious knock-on effects for the production process.

In addition, once you take into account the time it takes to ship products to the UK, which is usually five to six weeks, and the time it takes for goods to get through customs, it remains to be seen if return on investments and cost savings of offshore outsourcing are as appealing as many are led to believe.

Above all, though, is the fundamental issue of quality. The cost of products in the UK may be greater, as it struggles to compete against lower cost regions around the world, but the assurance of excellence through British standards in design and production techniques far outweighs the short-term cost benefits from overseas suppliers and it is this which keeps us in good stead.

British manufacturing is known for its quality of production and innovation and its investment into the latest design and production techniques. However, the demand for cheaper prices and increases in production costs means if the UK government and, indeed, the British industry does not start to look closer to home then the demise of manufacturing within the electronic industry in this country will continue further.

IN COMPARISON, FOREIGN EMS PROVIDERS REQUIRE FAR MORE FORWARD PLANNING TO ACCOMMODATE LARGE ORDERS AND, CONSEQUENTLY, DESIGN CHANGES CAN IMPACT HEAVILY ON LEAD TIMES

I can't deny that manufacturing outside the UK offers plenty of attractive and cost-effective solutions. However, it does seem to carry with it a certain level of risk and pursuing operations within the UK region should be encouraged and not overlooked.

Not all products are suitable to outsource abroad and, with today's market remaining heavily reliant on lead times, consistent quality and immediate response to developments, it may be well worth looking at building partnerships a little closer to home.

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A million APPLES a day...

JUAN PABLO CONTI FOLLOWS APPLE'S TRANSITION FROM THE COMPUTER TO THE CONSUMER ELECTRONICS WORLD

Whenever you set out to profile a company, you are invariably confronted by a long list of facts that are either stemming from its past, shaping up its present or auguring a certain future. When it comes to Apple, everything these days seems to be about its present, with the new iPhone inexorably grabbing all the headlines. You might be more or less familiar with Apple's website, but if you had tried the usual **www.apple.com** at any time between 9th of January and the 30th of January 2007, all you would have got was a large picture of the gadget that has everybody talking in the consumer electronics industry.

So much so is the company's attention devoted to the iPhone right now that when CEO Steve Jobs finally announced the eagerly-anticipated handset on 9th of January he even decided to change the name of the company for the first time in its history. No more 'Apple Computer'; just 'Apple'. He argued that the prominent role played by the iPod + iTunes first, coupled with the guaranteed success he now believes awaits the iPhone (due to hit US store shelves this June), were not properly reflected any more in a company name which suggested its main business was selling computers.

But when you leave the hysteria currently surrounding the iPhone for a minute and move just a couple of steps back into Apple's past, it is obvious that – for most of its history – it has been, indeed, all about making and selling computers.

From top:
- *Corporate headquarters in Cupertino, California*
- *Apple's iconic 'Cube' Store on New York's Fifth Avenue*

Hello, I'm A Mac

It all started back in April 1976, when three young men (Steve Jobs, Steve Wozniak and Ronald Wayne) living at the heart of what later became known as Silicon Valley founded a company to build personal computers. The first product they launched, Apple I, was hand-built in a garage belonging to Steve Job's parents. Far from a fully-fledged computer, it consisted really of a basic motherboard – no case, no keyboard, no monitor or power source were provided.

By the time Apple II hit the market the following year, Wayne – who had lost faith in the project after only a few months – had already sold his share of the company to his two other partners for only $800. Now reportedly working as an engineer for a defence contractor in California, it has been calculated that his stake in the company could have been worth up to $6bn.

The Apple II not only outsold its competing Commodore PET and TRS-80 models, but it also came to symbolise the nascent personal computing market. Apple designed a few other models between the late

Clockwise from top left:

- *Apple TV wirelessly links iTunes video content on PCs with HDTV screens*
- *The iPod brought Apple's sleek design and ease of use to a wider customer base*
- *OS X Leopard will power the next generation of Macs*
- *The latest Mac Pros can store up to three terabytes of data*

1970s and early 1980s (some with more success than others), until the legendary Macintosh was announced with a famous TV commercial aired during the 1984 Super Bowl football game.

While the 'Mac' quickly established a reputation as the most reliable computer for desktop publishing applications – a reputation that today extends to an even larger portion of the creative professional industry – there was a particular decision made during its development process that Apple came to regret badly: letting the then modest Microsoft write part of the software.

In 1983 Bill Gates was given access to a Mac prototype so that his company could adapt its BASIC and MultiPlan spreadsheet programmes to the Mac operating system, which sported one of the word's first implementations of a graphical user interface (GUI) in a personal computer. Two years later, Microsoft launched the first version of Windows, bringing the GUI concept to IBM PCs. Apple wasn't happy at discovering that much of the 'look and feel' of Windows seemed so familiar. But it still waited until 1988 to file a lawsuit against Bill Gates's firm, by then already firmly on track to becoming the dominant operating system (OS) maker that it is today.

Apple lost the long legal battle, while in the process giving birth to one of the technology sector's bitterest rivalries. Microsoft's huge market presence has since forced Apple into a sort of love-hate relationship with the Redmond giant. This was first evidenced in 1997, when Jobs surprised hardcore Mac fans by announcing a version of Microsoft Office designed for Macintosh computers, as well as Internet Explorer being made its default browser.

It was a time when Apple found itself at one the darkest periods of its existence. Strong competition from the IBM/Windows/Intel PC camp and increasingly complex customer demands meant the Cupertino firm was immersed in a difficult search for a more sophisticated OS. After exploring a series of external alternatives (which included even Windows NT), Apple decided the best available option was that offered by

Above and right:

- *The iPhone was designed by Jonathan Ive, who also created the iPod and the iMac*
- *iPhone will launch in Europe before the year's end*

NeXTSTEP OS. In early 1997, it acquired the company that had created it: NeXT, which had curiously been founded by Steve Jobs when he had been forced to leave Apple in 1985.

The move saw him return to Apple, where he remains CEO and an inspirational figure for the company. The core of NeXTSTEP OS was used to design the acclaimed Mac OS X platform. Undoubtedly, one of the elements responsible for Apple's revival of fortunes in the computer space (together with the industrial design icon that became the iMac workstation introduced in 1998), the operating system has since seen versions 10.0 ("Cheetah"), 10.1 ("Puma"), 10.2 ("Jaguar"), 10.3 ("Panther") and 10.4 ("Tiger") released.

Mac OS X 10.5 ("Leopard"), its next iteration, is scheduled for a Q2 2007 launch. But demonstrating that Apple continues to regard Bill Gates's company as a not particularly original software creator, Steve Jobs recently declared: "While Microsoft tries to copy the version of OS X we shipped a few years ago [referring to Microsoft efforts that led to the now available Windows Vista], we're leaping ahead again with Leopard."

The iPod Economy

With its mid-1990s troubles firmly behind it, Apple is now widely regarded as a success story. And while the resurgence of both its desktop and laptop product lines played an important role, it wasn't really until the iPod portable digital music player came along that Apple began its definitive transition from its personal computing roots to the more glamorous world of consumer electronics. "When we introduced the first iPod in 2001, it didn't just change the way we all listen to music; it changed the entire music industry," Jobs says.

Before changing the entire music industry, though, the iconic gadget started by changing Apple's bank account. During its fiscal 2005 period, for example, iPod sales grew by 248% compared with what already was a strong 2004. One year later, the combined revenues of iPod and its closely associated iTunes online music store exceeded for the first time those generated by desktop and portable Macs. When looked at in terms of unit sales, the 2006 figures are all the more contrasting: just over five million computers sold, versus 39.4 million iPods.

Overall, more than 88 million of them have been shipped since 2001, while the iTunes software has been used to legally download over two billion songs, 50 million TV episodes and more than 1.3 million feature-length films.

The term 'iPod generation' is used by social scientists and newspapers alike to refer to the children and young people of today. Apple has also coined another term, the 'iPod economy' – sometimes also 'iPod ecosystem' – to illustrate the fact that there are now over 3000 accessories specifically made for the three available versions of the device (the iPod, which includes a video player, iPod nano and iPod shuffle).

Even major carmakers and airlines have to adjust the way they manufacture their vehicles or install their

From top:

- *CEO Steve Jobs reveals the features of the iPhone on 9th of January*
- *Apple has used the iTunes software mainly to drive its hardware sales*

in-flight entertainment systems in order to make room for the demands of the iPod generation. Seven in ten new cars manufactured in the US during this year will be iPod-ready, where drivers and passengers will be able to control their iPod sound features via their vehicle's stereo system.

On the airline front, a list of carriers that includes Air France, Emirates, KLM, Continental, Delta and United will soon start offering passengers an iPod-friendly seat. Apart from being able to power/recharge their music players mid-flight with the connectors provided, they will have the chance to use the plane's seat-back displays to reproduce their stored video content in a larger screen.

Apple – The Phone Maker

A little less than 12 months ago I was writing an article about the potential threat that a new breed of mobile phones equipped with powerful hard disk drives was likely to pose to MP3 players in general, and the iPod in particular. I remember asking an ABI Research analyst whether it was possible for Apple to try and counter this threat by going the other way around and adding mobile phone functionality to the iPod.

"The possibility obviously exists," he then replied. "However, when we talk about an iPod, you have to remember this is a standalone device, which has inside everything for a consumer to take it home and play music. A cell phone, on the other hand, relies on a complex ecosystem that includes operators, a wireless infrastructure, handset makers and semiconductor devices. If you look at companies like Sony Ericsson, Nokia or Motorola, they've been doing this for 20 years. And for a new company just to use a brand name in order to get into this space it wouldn't be simple."

As it's turned out, of course, this is exactly what Apple has done now with the upcoming iPhone. If one were to reduce the thousands and thousands of speculative press reports and analysts' opinions currently being published, broadcast and – mainly – 'blogged' to the main point they are all discussing, we would be left with a very simple question: How successful will Apple really be as a mobile phone maker?

The answer varies wildly depending on whom you ask; ranging from guaranteed handset making leadership to sorry catastrophe. My personal view after watching Steve Jobs's presentation of the device (and many years following the telecommunications industry) is that the iPhone will – if not perhaps dethrone Nokia, Motorola and Samsung straight away as the most popular handset makers – certainly leave a large majority of consumers wondering why on earth their 'non-iPhones' still have those archaic, plastic, mechanical buttons.

The most revolutionary aspect the iPod phone brings to the handset industry is – without a doubt – its clever interface. Named 'multi-touch', this evolutionary form of touchscreen technology fundamentally changes the way users interact with applications on a phone. Everything is executed using one or more fingers. This, coupled with the iPhone's accompanying software (a stripped down version of OS X Leopard) not only makes physical buttons unnecessary and, therefore, considerably extends the size of the screen, but it also brings a level of intuitive interaction and ease of use unheard of in the mobile phone business.

Jobs claims multi-touch is "far more accurate than any touch display that's ever been shipped. It ignores unintended touches; it's super-smart; you can do multi-finger gestures on it and... boy, have we patented it!" He points to Apple's track record of introducing revolutionary interfaces that have made possible highly successful products: the mouse (which popularised computers); the click wheel (which left all non-iPod MP3 players looking hopelessly disadvantageous); and now multi-touch, which he insists places the iPhone five years ahead of any other smartphone on the market today.

Apart from the issue of competition with other handset makers, an even more interesting development to keep an eye on once the iPhone starts shipping will be the extent to which it will diminish the power of the mobile operators in a way that no other hardware vendor has so far been able to do.

That it will diminish it is out of the question. In fact, it already has, way before the first commercial iPhone has even been assembled. Cingular, the operator that was chosen by Apple to exclusively provide the cellular connectivity element for iPhone users in the US, was actually Apple's second choice of carrier. The first one was Verizon Wireless, which found unacceptable Steve Jobs's unprecedented demand that Apple should get a share of call revenues, apart from controlling the distribution channels and having the sole power to deal with all faulty device claims.

Cingular, one is forced to conclude, didn't have a problem with such requests. Meanwhile, Apple is intent on replicating the same, one-operator-per-market business model when it launches the iPhone in Europe in late 2007 and Asia at some point during 2008.

APPLE IN BRIEF

Founded: April, 1976 by Steve Jobs, Steve Wozniak and Ronald Wayne

Headquarters: Cupertino, California (US)

CEO: Steve Jobs

Employees: 20,186

Annual sales: $19.3bn (Fiscal 2006)

Net income: $2bn (Fiscal 2006)

R&D expenditure: $712m (Fiscal 2006)

Listed: NASDAQ, London & Frankfurt

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HOME AUTOMATION a luddite view

by Myk Dormer

"The degree of sophistication suggested by some of the gurus in this field makes me deeply suspicious: networking all of the home's control functions through the same central processor sounds clumsy at best and hazardously unreliable at worst"

At the risk of being labelled a 'luddite', may I quietly ask "why"?

Low power radio systems have a very long – and distinguished – pedigree. Their use in the home has seen application as diverse as the iconic, if frivolous 'garage door opener' right through to life-saving fire alarms and nurse call applications. With the increased availability of 2.4GHz radio solutions from major silicon vendors, these roles have expanded to include wireless Internet access, high quality wireless audio transmission and even video re-broadcast.

In all these cases, I can see the need for the product, but 'home automation' is a different case entirely. At first glance, the idea seems attractive. Implement a wireless communication network between all the electrical products and services in your home to extend the convenience you associate with operating, for example, your video by its remote control to all the other functions previously worked by 'local' controls.

It has undeniable benefits: a temperature sensor network can monitor room temperature and remotely control heating settings for each radiator accordingly. Infrared sensors can monitor room occupancy and turn off unused lighting, as well as having secondary intruder alarm and fire detector roles.

But the degree of sophistication suggested by some of the gurus in this field makes me deeply suspicious: networking all of the home's control functions through the same central processor sounds clumsy at best and hazardously unreliable at worst, while programming 'everything' through one convenient hand-held terminal (normally described as a PDA or an advanced phone) becomes a nightmare when the terminal is misplaced, left at work or when more than one person lives in the home.

(Enough jokes are made against men who 'hog' the television remote: now imagine if the same remote programs the heating, the patio lights and the coffee maker too.)

And, at the extreme end of this spectrum are the suggestions of systems which, for instance, allow the control of your stove from your mobile phone and where appliances can detect a shortage of a product and either send messages advising I should purchase more, or can place on-line orders to make up the deficit themselves.

So, as I drive home from the airport, I can turn on the oven – containing a roast that's been decaying in there all weekend – and hope that my inbox isn't full of messages from my fridge.

There is an engineering aspect to this trend. Without the allocation of significant segments of new bandwidth (at frequencies low enough to achieve significant penetration of internal walls) and the negotiation of new communication usage standards, the proliferation of these unnecessary communication links will, sooner or later, over-use the available bandwidth allocated to existing wireless products. In high-density residential areas this could rapidly result in a form of radio 'gridlock'.

And there is another detail: It's only recently being advertised extensively, but consumer white goods use a significant amount of energy in their standby states. Adding an extra layer of wireless transceivers, and extending them to include every light switch, radiator and utensil, could easily cancel out any savings made by improved, intelligent control of heating and lighting.

I think I'll get up off the couch and turn the kitchen light off – by hand!

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd
www.radiometrix.com

FULL STEAM AHEAD FROM CHIP TO CHIP – Serial IOs, why all that overhead?

IN THIS ARTICLE, **MARTIN KELLERMAN**, STRATEGIC APPLICATIONS ENGINEER FROM XILINX, BASED IN MUNICH, DISCUSSES SOME OF THE TECHNIQUES USED IN HANDLING HIGH-SPEED SERIAL INTERFACES AND GIVES A DETAILED EXAMPLE IN HOW TO CHANGE A PARALLEL INTERFACE TO A SERIAL INTERFACE

With the rise of high-speed serial interfaces additional techniques for coding, handling and transmitting data are more and more present. Comparing those techniques to "traditional" parallel interfaces, all the effort spent seems cumbersome. This article discusses some of the reasons why those techniques are being used, starting with the idea of changing a parallel interface to a serial interface.

In this article we will use "word" in the sense that it is a parallel piece of data with a defined width and not a 32-bit word.

Parallel Data Transmission

We start with the "old fashioned" parallel interface, 5V TT, 32-bit wide, running at 50MHz over a distance of 20cm from one chip to another. The clock for the two devices is a central oscillator on the board as in **Figure 1**.

This approach is relatively simple with the central clock being routed to all appropriate components on the board with similar delay. Taking into account that 16cm on the board approximate to a delay of 1ns, a similar delay on the clock lines is possible without major issues.

To guarantee that setup and hold times on the data lines are not violated, the easiest way is to clock the data out of the sender on one clock-edge and clock it in at the receiver on the opposite edge. This approach also allows for variation on the length of the data lines, see **Figure 2**.

This is a very simple system which works reliably and has a data throughput of 32-bits x 50MHz = 1.6Gbit/s.

Serial Data Transmission

Now the decision is made to change this system to a serial interface, which has to transmit the same amount of data.

The first step is to take the existing parallel data and serialise it. This means that on one line 32 bits have to be transmitted within one 50MHz period. The duration of one serialised bit is 625ps.

As can be seen in **Figure 3**, having the 32 bits within one clock-period automatically means having a clock of a much higher frequency. If double-data rate techniques of clocking data at both the rising and falling edge are used, a clock of 50MHz x 16 = 800MHz is needed.

To achieve this clock frequency, a Phase-Locked Loop (PLL) is the first component to incorporate into the system. Once the high clock-frequency is present, a parallel/serial converter or Parallel-In/Serial-Out (PISO) is necessary at the transmitter. The first two additional components over a parallel interface are added, a PLL and a PISO.

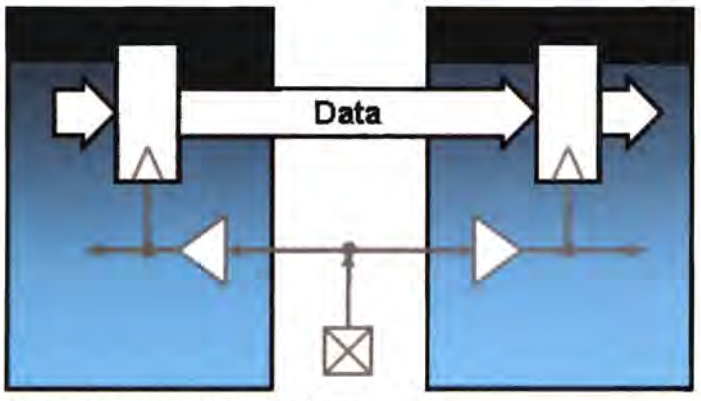


Figure 1: *System with central clock*

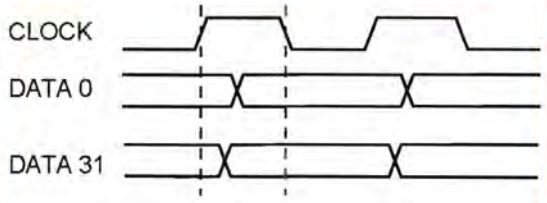


Figure 2: *Clocking data between devices with central clock*

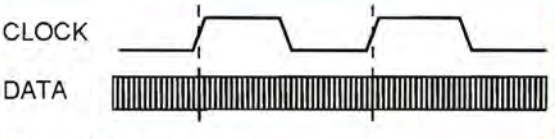


Figure 3: *Serialised data*

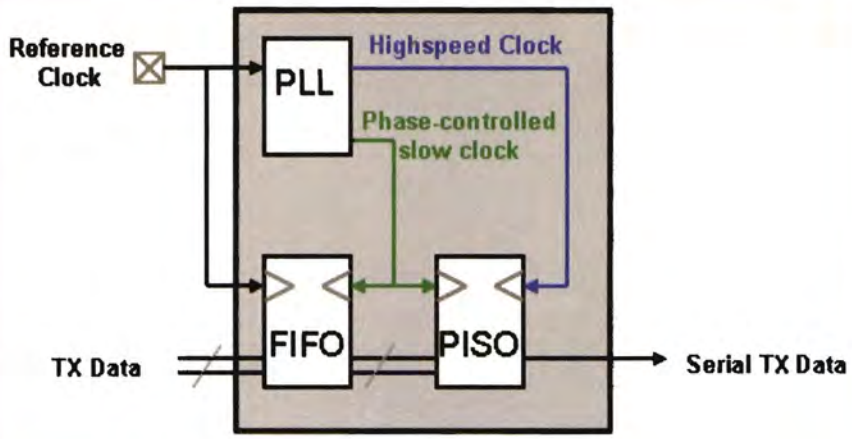


Figure 4: *Basic components for serial transmission*

The parallel data and its clock have an unknown phase to the high speed clock generated by the PLL. A transition directly from the parallel to the fast clock-domain is therefore not possible. To solve this, a shallow FIFO (First In First Out) needs to be added into the data path, written to by the slow reference-clock and read out with a slow phase-controlled clock derived off the high speed clock. This FIFO only needs to compensate the phase difference between the reference clock and the internal slow clock, hence, it can be shallow with only a few entries.

Figure 4 shows the basic building blocks for transmitting high-speed serial data.

Receiving Serial Data

The next step is the reception of the serial data at the second device. There, the data with a bit-width of 625ps needs to be reliably clocked into the device. Taking the 50MHz clock and multiplying it up to 800MHz using a PLL is surely the first idea. However, the phase relationship of this multiplied clock and the incoming data is unknown, hence clocking the serial data into the device using this fast local clock is not feasible. Additionally, when transmitting data over a longer link with independent oscillators at the sender and receiver, those two oscillators will have a slightly different frequency.

Forwarding the original high-frequency clock is also not practical as the skew involved between data and clock gets too high and other effects as jitter and attenuation on the line close the available timing window for clocking the data reliably into the receiver.

So, to get the incoming data into the receiver properly, something needs to be added that allows the local circuitry to know when it is safe to sample at the first flip-flop stage. This is typically done using a clock recovery, working on the edges of the incoming data. Multiple ways of doing this are possible. A relatively simple Clock Data Recovery (CDR) works on multiple phases of the fast local clock and samples the bit with the phase that is furthest away from an edge.

With a continuous tracking of the one phase furthest away from the edges, it is also possible to track the frequency within a given limit, typically within some 100s ppm off the local frequency. So the next thing is added, the clock recovery at the receiver.

After the data has been sampled, it needs to be de-serialised in a Serial In, Parallel Out (SIPO) converter which is typically build as a shift register. This SIPO is written to with the fast clock generated by the CDR and read with a slower version of this clock, called a recovered clock. This recovered clock is locked in frequency to the incoming data.

Coding of Data

For the CDR to work properly, a sufficient amount of edges must appear in the incoming data-stream. The more edges appear in the data stream, the easier it is for the CDR to track the data correctly. The CDRs have an upper limit of how many non-toggling bits they can withstand, which is depending on their actual implementation.

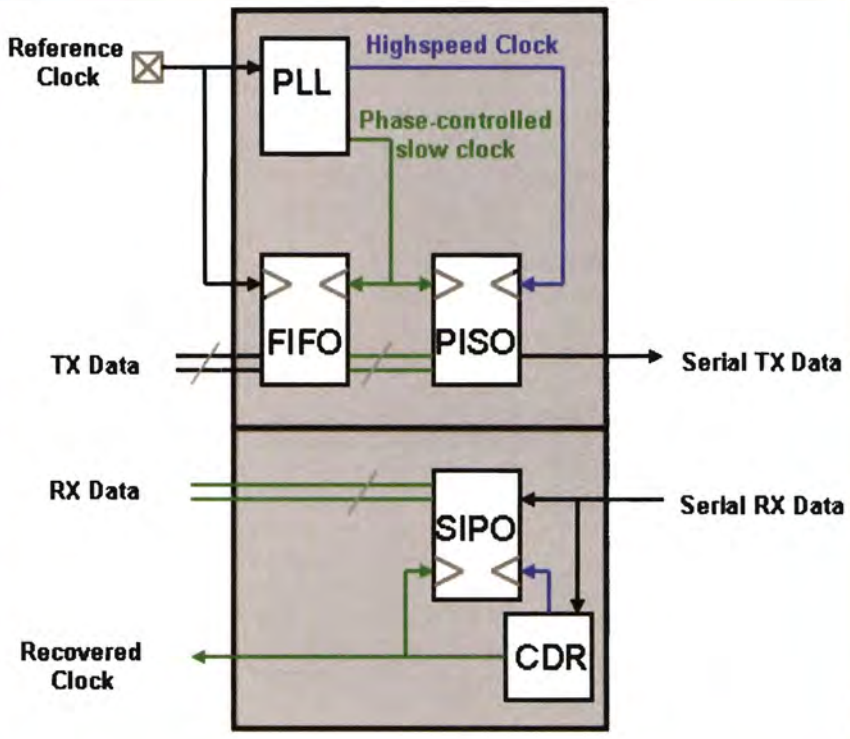


Figure 5: *Transceiver with the basic blocks for TX and RX*

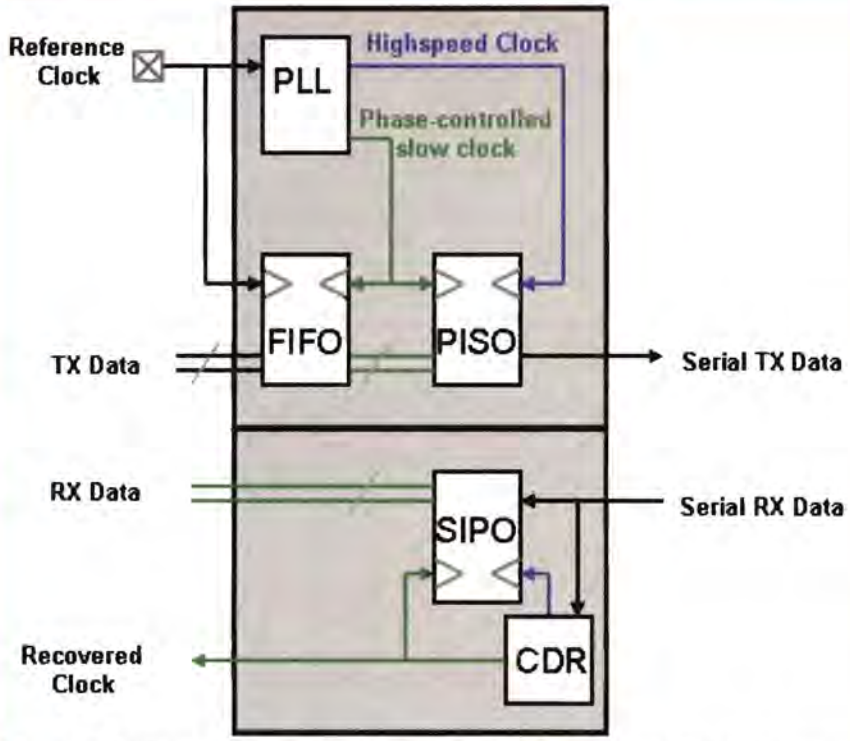


Figure 6: *Coding blocks added for sufficient amount of edges in the data stream*

However, as with normal user-data, it is very hard to guarantee a maximum number of equal bits, something again needs to be added: some coding of the transmitted data, in order to have the maximum amount of equal bits well below the limits of what the CDR can withstand.

Several types of coding exist, either real 1:1 coding, where for every transmitted piece of data (e.g. byte) a fixed bit-pattern with a high amount of edges is used, as in 4B5B or 8B10B coding or scrambling of the data with a given polynomial as for OC48.

This coding leads to the next two necessary blocks, a coder for the transmitter and a decoder for the receiver.

The coder can sit in two positions, either in front of the FIFO and being clocked from the reference clock or, alternatively, after the FIFO and being clocked with the phase-controlled slow clock.

Interpreting Serial Data

At this point in time, we have enough edges in the incoming data-stream for the CDR to track it properly. However, after the de-serialiser the data is not word-aligned but appears just as the de-serialisation starts, shown in **Figure 7**.

Just feeding this data into a 1:1 decoder does not help. With the unaligned data fed into the decoder, the decoding tables would not match up and, hence, the decoding only generates wrong decoded data. In order to have the data properly aligned, some form of alignment to the original word-boundaries needs to happen. This can be either some kind of self synchronisation of the incoming data-stream or an explicit alignment on special bit-patterns present in the data stream.

A typical example of an explicit alignment is 8B10B encoding. All 256 possible combinations of 8 bits have a given fixed encoded result. Additionally, a control signal is fed into the encoder for information, if the data should encode normally or if one of 12 special codings should happen. Those 12 special codings are referred to as K-characters and have an encoding that is not present on the encoded data-characters. These special bit-patterns of the K-characters allow the receiver to detect single words in the incoming serial data stream and align the word boundaries accordingly. It is the responsibility of the user to include those bit patterns in the serial data-stream, however, protocols based on 8B10B encoding (e.g. Gigabit Ethernet, FibreChannel, PCI Express, etc.) have this already incorporated.

Figure 8 shows the specially encoded data in italic blue. Initially, after the de-serialiser, the special bit-pattern is typically present over word boundaries of the received data. The aligner looks at the present and the previous words, and detects if the special bit-pattern is present. If it is present, the word boundaries are adjusted accordingly and after the aligner the data is presented in the order that it was sent in.

An example for self-synchronisation is 64B66B coding, used for 10Gigabit Ethernet. In every block of 66 bits, the known position of a 1-0 pattern is checked. If this pattern is correctly present at the correct location, alignment is achieved, if not – a bit-slip of one bit is done. This mechanism is performed until alignment is achieved.

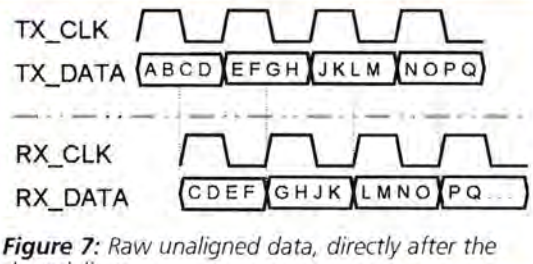


Figure 7: *Raw unaligned data, directly after the de-serialiser*

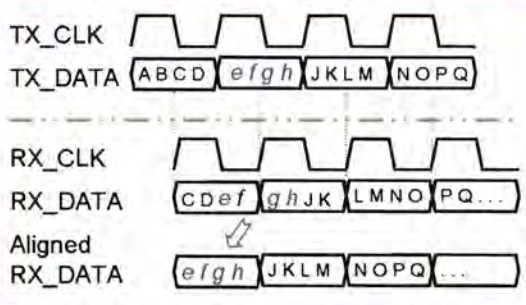


Figure 8: *Alignment of data to explicit bit-patterns*

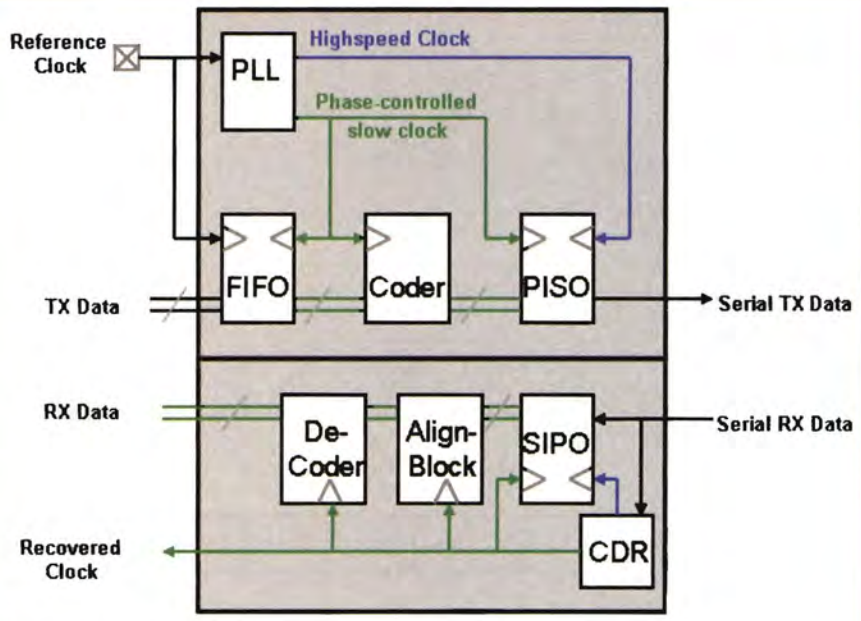


Figure 9: Block diagram with an alignment block added to find original word boundaries

Independent of the type of encoding used, the alignment block is located directly after the SIPO, as shown in **Figure 9**.

Handing Data Over to the Local Clock Domain

As the serial data is now properly inside the serial receiver – aligned and decoded, it needs to be forwarded to the rest of the device. Several options exist to do that.

The easiest way is to use the recovered clock in the rest of the RX design. This means the recovered clock must be phase-controlled and must not have an excessive delay after it is supplied out of the transceiver, otherwise the data will be corrupted.

An easier way around the phase and delay controlling of the recovered clock is to add a similar FIFO as on the TX side. This allows easy routing of the recovered clock out of the receiver and also allows for delay on the clock routing to dedicated clock-buffers (see **Figure 10**). For this use-model a shallow FIFO is sufficient, however, additional functionality is often needed.

Another use-model for the receiver is that it should be delivering data into the receiving system, which is clocked by a local clock and, hence, will have a slightly different frequency than the incoming data. If no action is taken then this frequency difference will corrupt the incoming data by either a FIFO overflow or underflow.

As the clock frequencies are fixed in this use-model, the only available option is to work on conditioning the data. If "enough" dummy-words are inserted that can be either skipped or repeated when reading, the FIFO can avoid the corruption condition. **Figure 11** shows the situation of the write pointer advancing slower than the read pointer. Normally, this leads to the underflow of the FIFO. However, when the read pointer reaches the defined dummy-word, it does not advance to the next FIFO entry as it recognises being away from a desired half-full condition but reads the dummy twice. During this double reading of one word, the write-pointer advances normally, getting back to the typical half-full condition of the FIFO.

The same functionality works for the opposite condition, the read pointer advancing slower than the write pointer. In that condition, the dummy word is simply skipped.

The important bit for the clock correction is, it must be 100% sure that the dummy characters cannot accidentally be mistaken with real data-characters. One way of providing this security is to define a combination of words that do not only consist of data words but also of out of K-characters already mentioned before. This allows for a combination that does not appear in a normal data-stream consisting of only data words.

Error Checking

Up to now we have made sure that we can send and receive the data properly. However, we don't know if the received data is really correct. Despite the fact that 8B10B coding allows to recognise if an incoming data-word after alignment is not part of the decoding table,

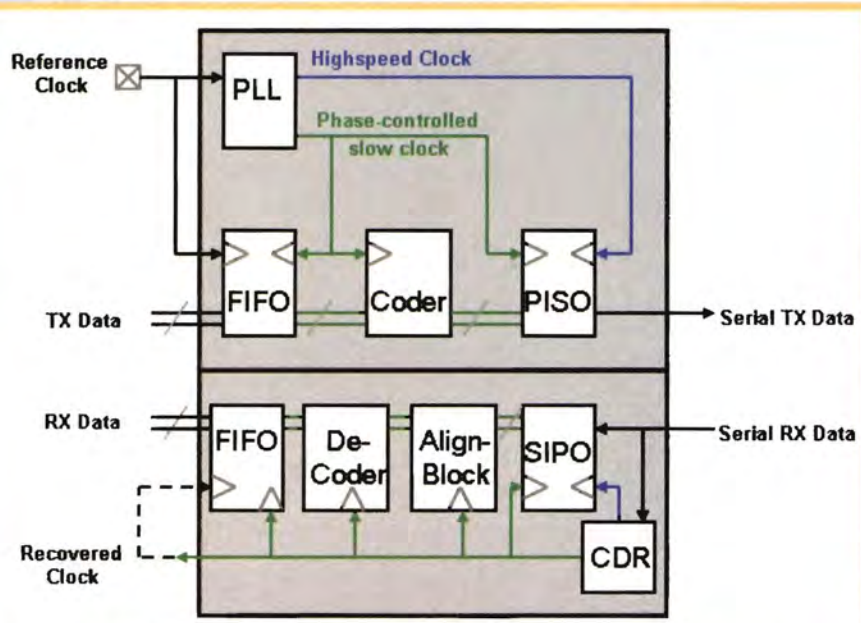


Figure 10: Block diagram with RX-FIFO added for phase compensation on recovered clock, routed in fabric

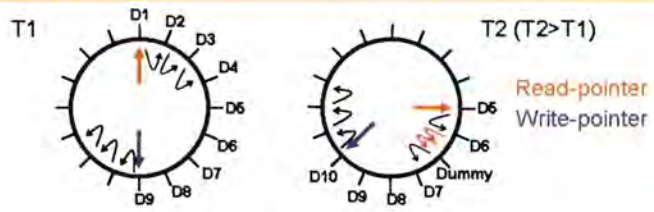


Figure 11: *Ring buffer FIFO with read pointer catching up over time, clock correction active*

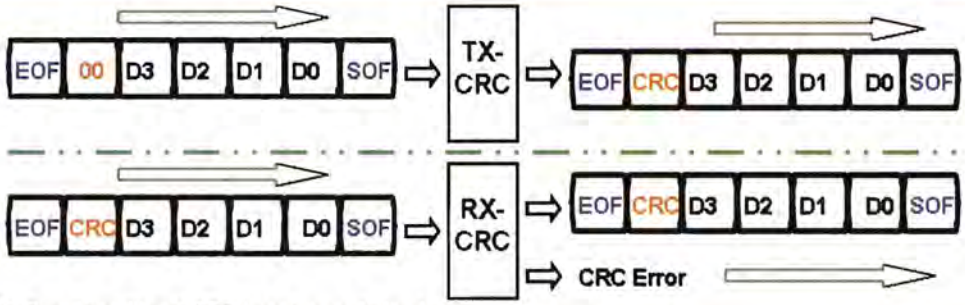


Figure 12: *Functionality of CRC inserter and checker*

it is still possible to get bit-flips that change one valid 10-bit combination into another. Even though the new 10-bit code may be part of the decoding table, the result is still wrong.

As it is not acceptable for most applications to work on the corrupted data, some way must be found in order to reliably detect if data was received that does not match the originally sent data. A reliable way to detect this kind of error is to add some check-sum to the transmitted data.

As soon as the idea of a check-sum is brought up, it automatically means some kind of data framing, so that the check-sum logic knows where to start calculating, where to stop and, also, where to store the result. The principle functionality is shown in **Figure 12**; the user data is sent into the CRC generator, starting with a "Start Of Frame" (SOF) symbol and followed by normal user-data. The CRC generator runs this data through a fixed internal polynomial but also outputs the data normally. Just before the "End Of Frame" (EOF), some empty words must be supplied by the user; those are the locations where the CRC generator places the result of its polynomial.

The CRC checker works similarly. It also starts working on the SOF, generating the same CRC as the generator. When the checker reads the EOF, it compares its internally-generated CRC pattern with the one transmitted in the frame. If they match, no errors occurred in the transmission; if they are different, the data was corrupted, a CRC error is asserted and the frame data typically cannot be used anymore.

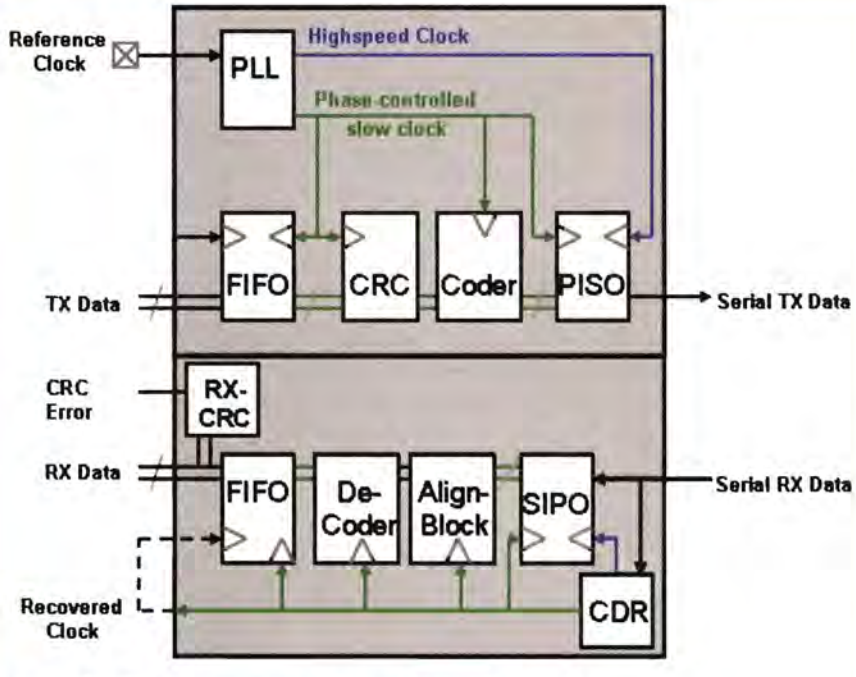


Figure 13: *Block diagram with CRC added on TX and RX*

Resulting Data Rate

At this point in time, let's have a calculation on what we already have as intermediate data-rate with following items:

- 32 bits of data at 50MHz
- 8B10B encoding
- Framing and CRC
- Clock correction with two bytes between frames.

The 8B10B encoding brings the 32 original bits up to 40 bits. This leads to a data-rate of 40 bits x 50MHz = 2000Mbit/s.

To calculate the effect of framing on the data rate, it needs to be taken into account how long the individual frames are. Longer frames can potentially transmit more data at a given data-rate, however, in the event of a corrupted frame with CRC error, also more data needs to be re-transmitted. Vice versa, shorter frames limit the amount of user data that can be transmitted, however,

on corrupted frames less data needs to be re-sent. However, the maximum packet-length is something a user typically does not have to worry about, it is given by the standard.

For this discussion an arbitrary maximum frame-size of 256 bytes is chosen. Of those 256 bytes, two are taken off for SOF and EOF and four more bytes to store the CRC information. This leaves 250 bytes of user-data to be transmitted in one frame. Additionally to the data within the frames, two bytes for clock correction are transmitted.

So, for every 250 bytes of encoded user-data, 258 10 bit-words need to be transmitted on the line. The data rate needed to transmit this amount of user data is now 258/250 * 2000Mbit/s = 2064MBit/s, a significant increase from the original 1600Mbit/s.

However, what is not included is some margin for the re-transmitting of corrupted frames.

Data Bundling for Higher Bandwidth

What has been shown up to now is aimed at one serial transmitter. But what happens if the bandwidth of this one link is not enough to transport all the necessary data?

In a "traditional" parallel system you have two possibilities of getting more throughput: increasing the transmission frequency and/or increasing the number of parallel bits.

For a serial link, the maximum throughput is a defined value which cannot be changed. So, the only other possibility is to increase the number of parallel bits transmitted. This leads to the need for the parallel data to be split up and transmitted over two independent transceivers.

However, as the two channels are independent from each other, the data coming out at the parallel side of the receiver will not be matching to each other as shown in **Figure 14**. What can be seen at the receivers is some skew between the received words. This is caused by skew between the transmitters, skew on the transmission lines and skew in the receiver.

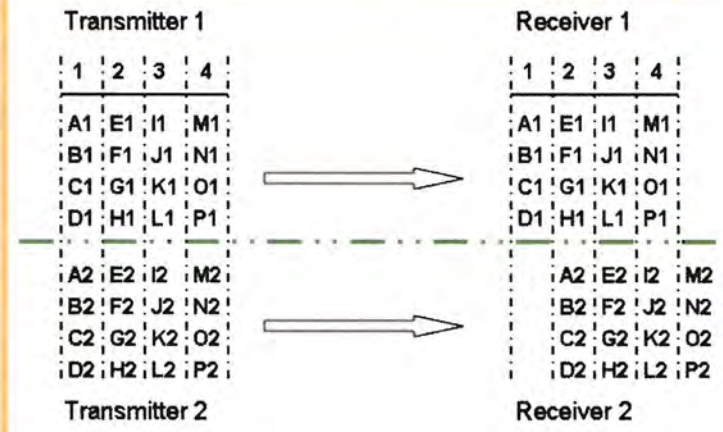


Figure 14: *User data transmitted over multiple independent links without any bonding mechanism*

Typically, the FIFOs' read-pointers are at the same position, however, differently timed data is present there, illustrated in **Figure 15**. Even though the read pointers are at the same location in this example, the data present there does not match together.

One way to solve this situation and get the data out of the receiver as it was supplied to the transmitter is to put special markers into the data. These markers can be recognised by logic in the receiver, which adjusts the position of the read pointer as shown in **Figure 16**. The FIFOs are read normally until defined markers are found in them. When this happens, the receivers have to communicate between each other and then adjust their read pointers to the positions of the markers in their memory. After this so called "channel-bonding" has occurred, the data at the two receivers is in sync again.

As usual, the markers used for channel bonding must be different from normal data to avoid wrong bonding. Typically, they consist of some known "violation" of the protocol, be it using control characters or intended violations of disparity (number of 1s and 0s on the line).

Electrical Modifications (Pre-emphasis)

Up to now we have had a lot of blocks already brought into the serdes (serialiser/deserialiser). Taking what we have and running it in a real situation, shows that we have good chances of not getting any data over the link. The reason for that comes up a bit later.

A measurement is performed at the receiver and the results put on top of each other. This shows how clearly defined the electrical signals are at the receiver. A superposition of an ideal data-stream, as shown in

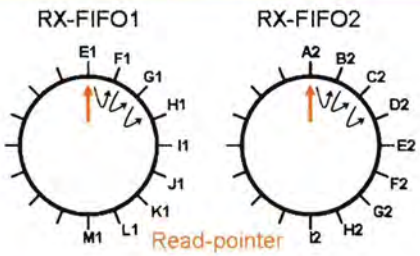


Figure 15: *Two FIFOs of independent receivers with differently delayed data*

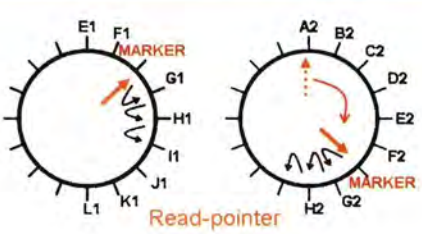


Figure 16: *Two FIFOs of independent receivers with channel-bonding markers in the data stream*

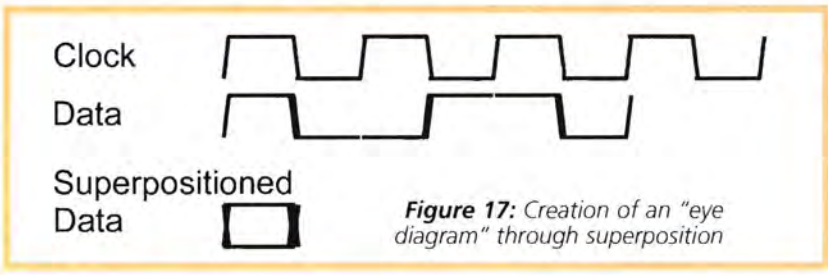


Figure 17: *Creation of an "eye diagram" through superposition*

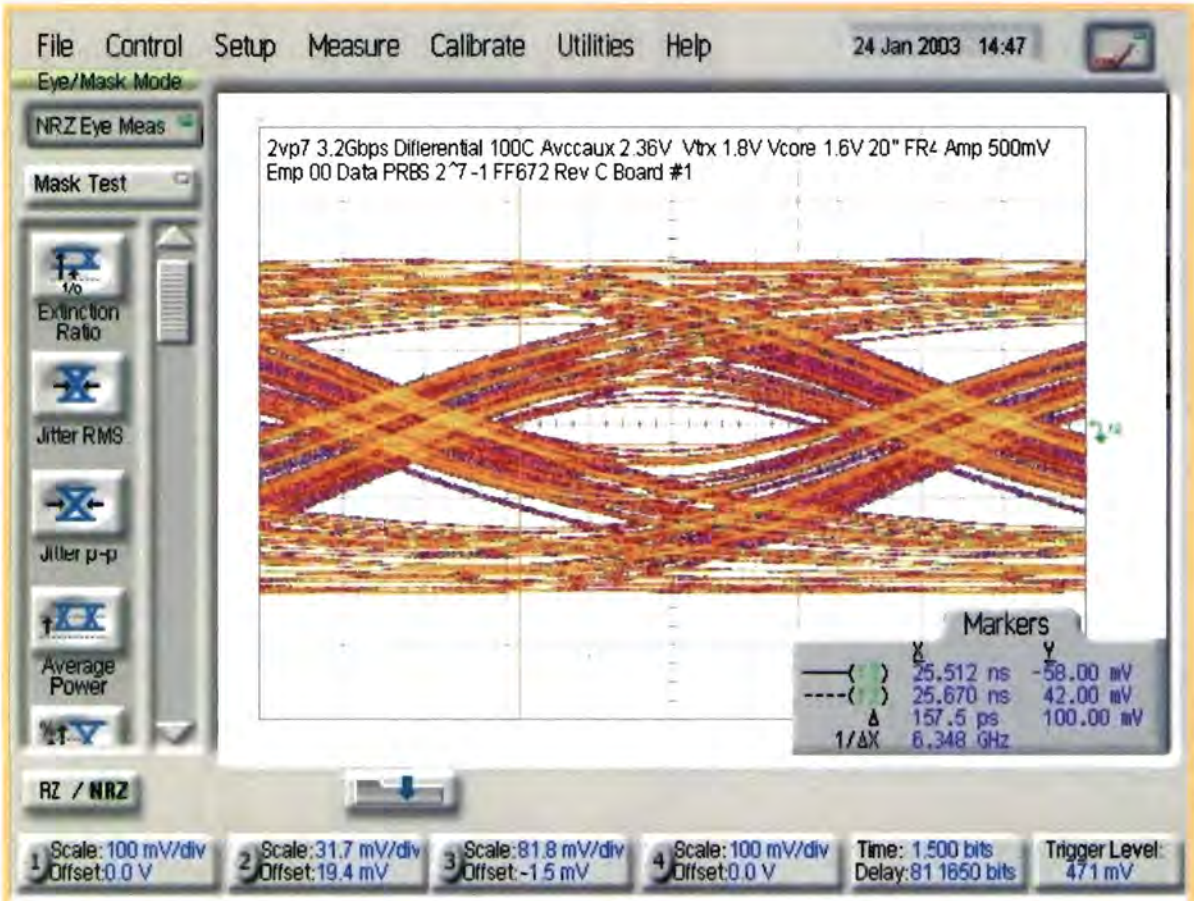


Figure 18: *Measurement of superpositioned serial data after longer transmission line*

Figure 17, shows an opening in the middle where the signal can be reliably sampled.

A real measurement on such a signal, generated with our discussed serdes, would lead to a completely different result. At the high transmission frequencies, effects from attenuation, influences between data bits and reflection severely influence the signal. A result of our virtual measurement is shown in **Figure 18**. The targeted opening in the middle of the so-called "data eye" is very small, the transition of consecutive bits is blurred and, hence, a reliable clocking of the data bits into the receiver is not possible. One of the main reasons for the bad signal quality is the strong attenuation of, especially, the higher frequencies.

Not all effects can be compensated however, the interesting frequencies can be amplified by either defined distortion at the sender or filtering and amplifying at the receiver. The simplest solution is the so-called "Pre-Emphasis" at the transmitter, which emphasises the high frequency content of the signal. When bits change at the sender, the amplitude of the signal is deliberately driven over the nominal 1 or 0 values and returned to the nominal value after the duration of one bit, as shown in **Figure 19**.

The result at the sender is a signal that looks much worse than before. However, at the important point – the receiver – the signal is so much improved that a reliable sampling is possible, see **Figure 20**.

The alternative, equalising at the receiver, is not discussed in this article. The working principle, however, is similar: the attenuated high-frequency content is band-pass filtered at the receiver and then amplified and, hence, the eye opened inside the receiver.

Basic Rules Followed

As was shown in this article, the basic concept of serial transmission is quite straight forward. Even if a block diagram of such a serdes device may look very complicated at the beginning, they follow the same basic rules despite differences in their architecture.

References:

UG 024: Rocket IO Transceiver User Guide
UG 076: Virtex-4 Rocket IO Transceiver User Guide

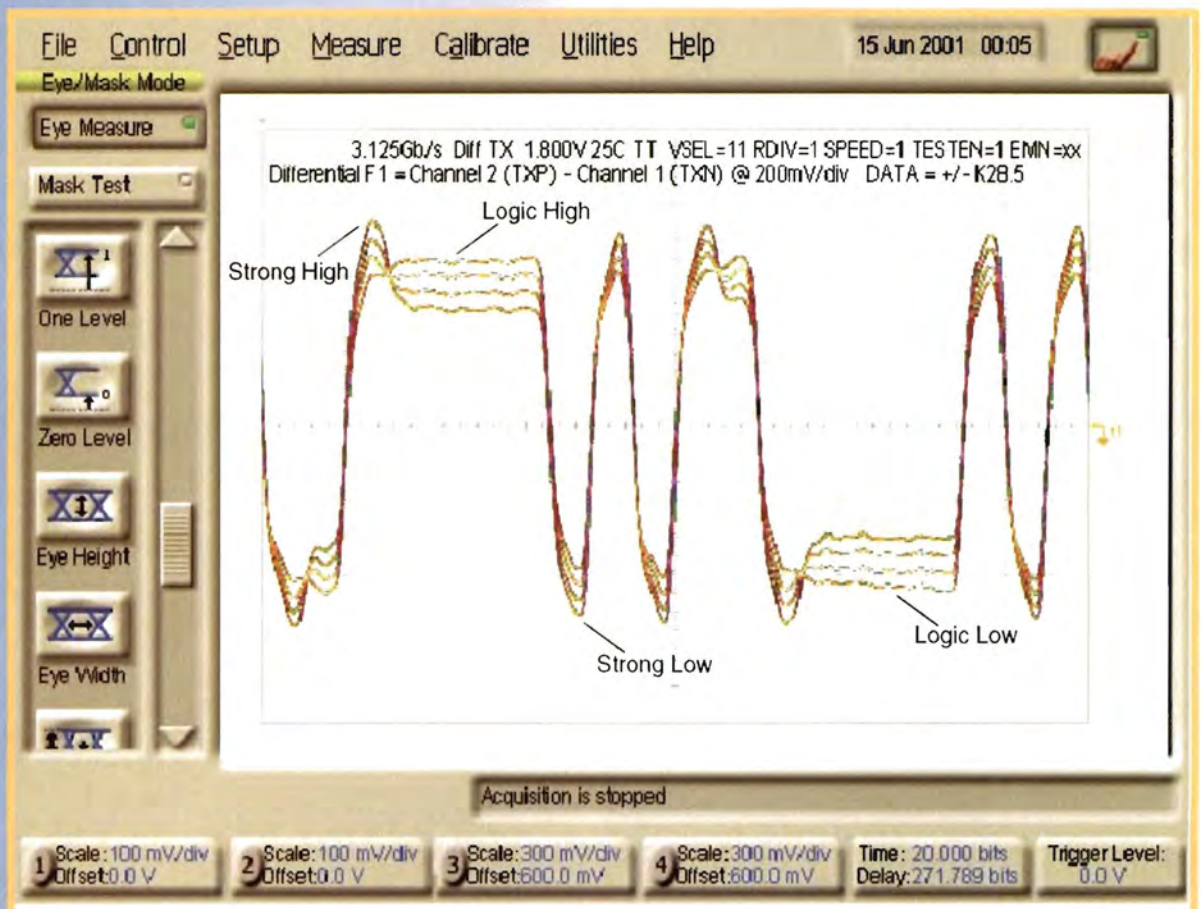


Figure 19: *Serial bit-pattern with several stages of pre-emphasis*

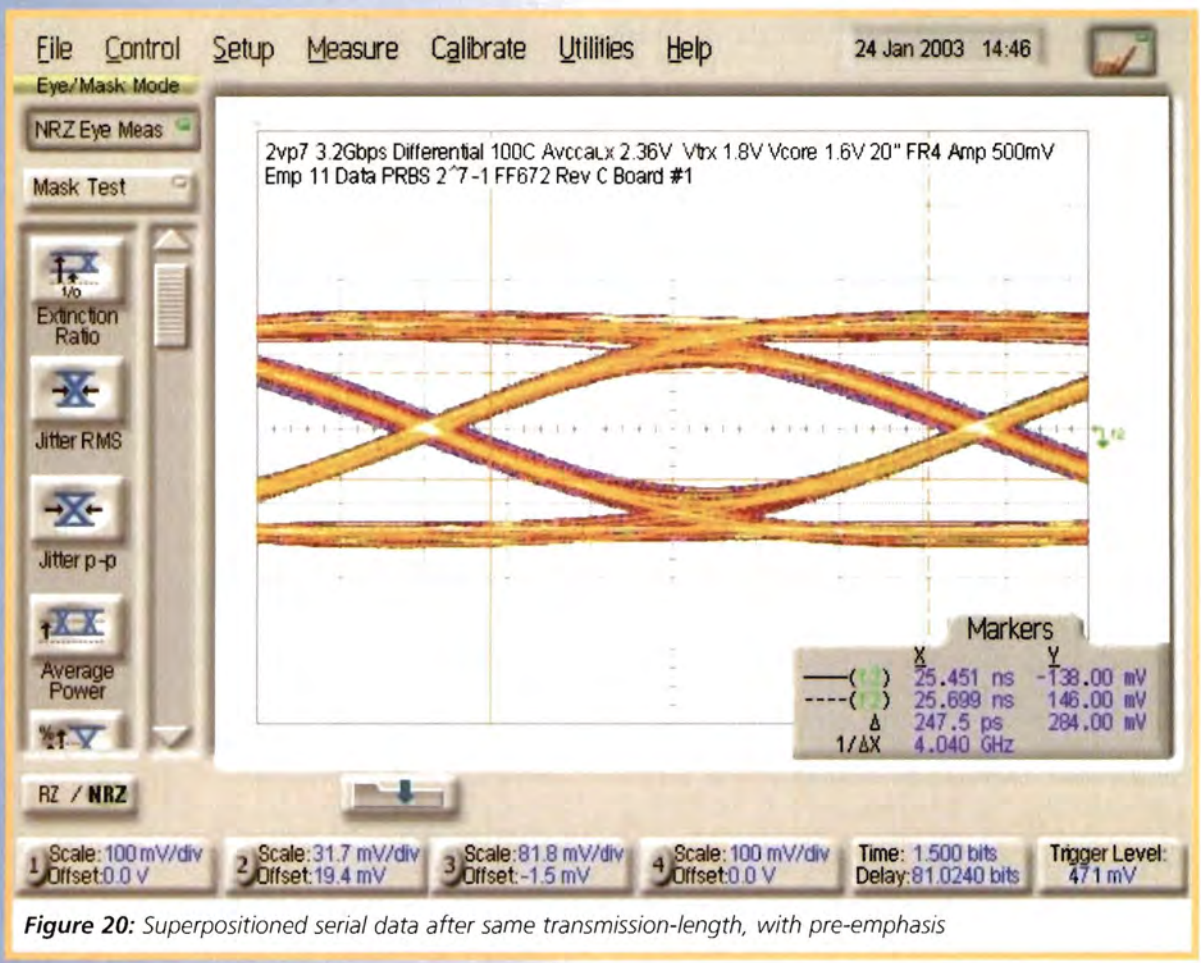


Figure 20: *Superpositioned serial data after same transmission-length, with pre-emphasis*

DEVELOPING HIGH-SPEED

A COMMON PROBLEM FOR TODAY'S SYSTEM DESIGNERS IS TO RELIABLY INTERFACE TO NEXT GENERATION HIGH-SPEED MEMORY DEVICES. IMPLEMENTING HIGH-SPEED, HIGH-EFFICIENCY MEMORY INTERFACES IN PROGRAMMABLE LOGIC DEVICES SUCH AS FPGAS HAS ALWAYS BEEN A MAJOR CHALLENGE FOR DESIGN ENGINEERS, SAYS SID MOHANTY, STRATEGIC MARKETING MANAGER AT LATTICE SEMICONDUCTOR

Memory devices are an integral part of a variety of electronic systems. However, differing applications do have different memory requirements.

For networking infrastructure applications, the memory devices required are typically high density, high performance, high bandwidth, memory devices with a high degree of reliability. In wireless applications, low power memory is important, especially for handset and mobile devices, while high performance is important for base station applications.

Broadband access applica-tions typically require memory devices where there is a fine balance between cost and performance. Computing and consumer applications require memory solutions like DRAM modules. This article will focus primarily on memory applications in networking and communications.

Memory can be on-chip or off-chip. Next generation FPGAs may have several Megabits of RAM on chip. These are useful for simple FIFO structures for nominal buffering requirements. Cost is the primary factor defining the amount of memory on chip. For large memory (buffer) requirements, off-chip memory is typically used. On-chip memory is always faster, but has size restrictions due to the cost it adds to the FPGA.

Large, fast memory devices are required in networking and communications applications, with tasks ranging from simple address lookups to traffic shaping/policing to buffer management. Each of these tasks comes with a unique set of requirements. Networking system architects have traditionally turned to Static RAM (SRAM) to solve latency issues, while incurring greater cost. For instance, low and medium bandwidth applications require low-latency memory, so RAMs like ZBT (Zero Bus Turnaround) SRAM and Quad Data Rate (QDR) SRAM are ideal. RAMs improve memory bandwidth by eliminating wait states or idle cycles between read and write cycles. Recently, system architects have turned to SDRAM for networking architectures, where reduced latency meets low cost.

Figure 1 illustrates a typical networking architecture. At 10Gbps, address lookups with a typical read-write ratio of 1000:1 could easily be handled with Double Data Rate (DDR) SRAM. Link list management, traffic shaping and statistics gathering tasks typically have balanced a 1:1 read-to-write ratio, requiring higher-performance QDR SRAM. On the other hand, larger buffer memories are typically implemented in DDR SDRAM (Synchronous DRAMs). A replacement for DRAM, SDRAM synchronises memory access with a processor clock for faster data transfer. Faster speeds are also achieved because SDRAM allows one block of memory to be accessed while another is being prepared for access. Unlike DRAM, SDRAM relies on static current flow rather than a dynamic stored charge, eliminating the need for continual refreshing.

Another new contender has entered the high-performance memory arena. Reduced Latency DRAM (RLDRAM) provides an SRAM-type interface with non-multiplexed addresses. RLDRAM technology provides

MEMORY INTERFACES

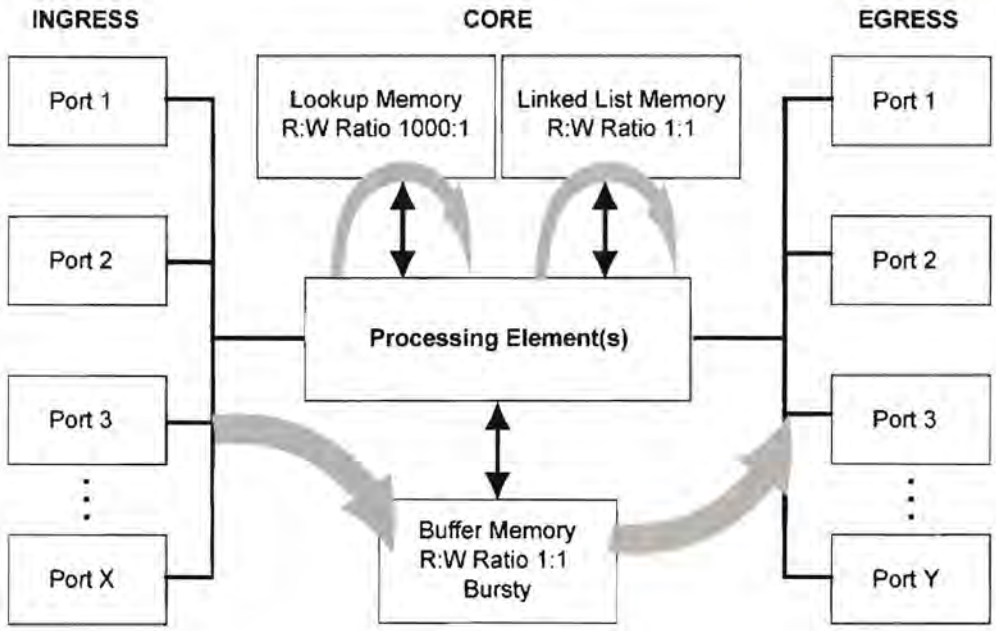


Figure 1: *Typical networking architecture*

minimised latency and reduced row cycle times that are very suitable for applications requiring critical response time and very fast random accesses, like next generation (10Gbps and beyond) networking applications.

Memory Controller Challenges

Current memory interfaces often require clock speeds in excess of 200MHz to achieve the throughput requirements of line and switch cards. This is a major challenge in FPGA architectures. Phase Locked Loops (PLLs), Delay Locked Loops (DLLs) and low-skew clock networks on chip are essential to allow control of the clock-data relationship.

Next generation memory controllers operate at HSTL (High-Speed Transceiver Logic) or SSTL (Stub-Series Transistor Logic) voltage levels. This lower voltage level swing is required to support high-speed data operation of the inputs and outputs of the memory device (and the memory controller). HSTL is the de facto I/O standard for high-speed SRAM memory devices, while SSTL is the de facto I/O standard for high-speed DDR SDRAM memories.

When multiple output drivers switch simultaneously, the relative ground voltage within the device is raised momentarily and the power supply drops, resulting in the phenomenon known as ground bounce or Simultaneous Switching Noise (SSN). With memory data rates on the rise and package pin-counts continuously increasing, this issue will continue to be more and more prevalent.

DDR/DDR2-SDRAM

DDR2 memory devices pose a bigger challenge due to their higher speeds and the bi-directional DQS signal. Double Data Rate (DDR) memory interfaces pre-fetch two data bits per clock cycle from the memory core to the I/Os and then output the data on both the rising and falling edges of the clock. DDR can transfer two data words per clock cycle, as opposed to SDRAM's one word per clock cycle, effectively doubling the speed at which data is transferred. The data is sampled using a clock that accompanies the data so that skew due to I/O buffers and board trace delays is automatically nulled out.

DDR2 employs several enhancements that increase bus bandwidth and simplify operation. Lower supply voltages permit smaller design geometries and hence higher speeds; memory architecture changes permit larger storage capacity per device; "posted CAS" support simplifies instruction execution; and On-Die Termination (ODT) reduces support device count.

Quad Data Rate (QDR) SRAM

QDR SRAMs are very popular in low latency applications requiring simultaneous reads and writes. QDR2 SRAMs provide separate buses for read and write operations.

There are three sets of clocks associated with QDR2 SRAM devices: K and K# clocks are input clocks to the QDR2 SRAM device and are sent from the memory controller to the QDR2 SRAM device. C and C# are output clocks from the QDR2 SRAM device and are not

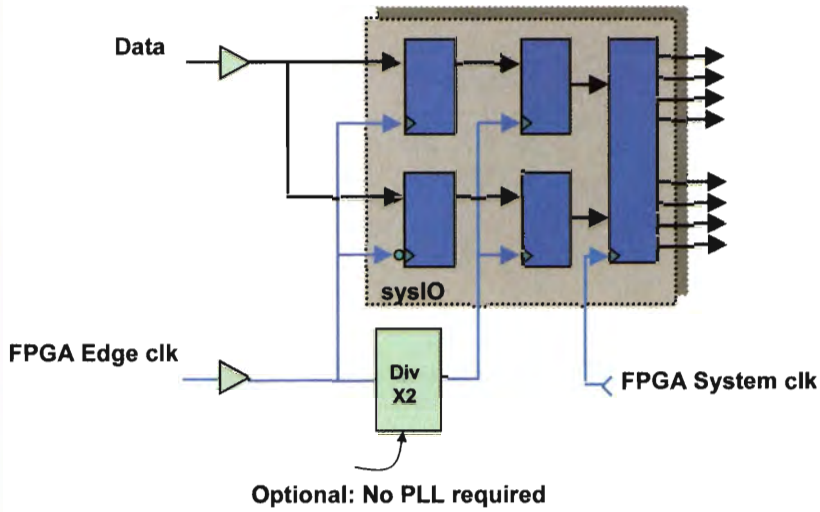


Figure 2: I/O block

used. CQ and CQ# are echo clocks that are better suited to capture the read data, especially at higher frequencies because they are timed exactly like the output data Q signals and can be treated as valid data indicators.

Since Q data and CQ clock are edge-aligned coming from the QDR2 device, CQ needs to be delayed (ideally centred to Q) to effectively capture the data. Methods such as using matched trace delays or preset input delay blocks can be used to delay the CQ with respect to the data, but using a DLL to delay the CQ signals by 90° gives the greatest timing margin over PVT and is independent of the interface speed.

Board Layout

Good board layout techniques are important on any high-speed design; in particular QDR-II SRAM designs have also some specific requirements. High-speed memory interfaces require stringent control in order to ensure the uncorrupted transfer of data. Here follow a number of considerations, which need to be taken into account when laying out the design.

- Trace lengths on buses must match to each other and their associated clocks to within 0.5 inch. There are two groups of buses and trace lengths must be matched to others in that group.
- All traces are uncoupled. In particular, "K" and "KN" are not a differential pair.
- Power rails, such as "VTT", must be planes, not traces.
- Care must be taken to keep reference voltages, such as the QDR-II SRAM's "VREF", noise-free.
- Simultaneous Switching Outputs (SSO) are a real concern in QDR-II SRAM designs, since usually there are no design constraints on how many signals can switch simultaneously.

Reduced Latency (RL) DRAM

Reduced Latency DRAM (RLDRAM) provides an SRAM-type interface with non-multiplexed addresses. RLDRAM II technology provides minimised latency and reduced row cycle times that are very suitable for applications requiring critical response time and very fast random

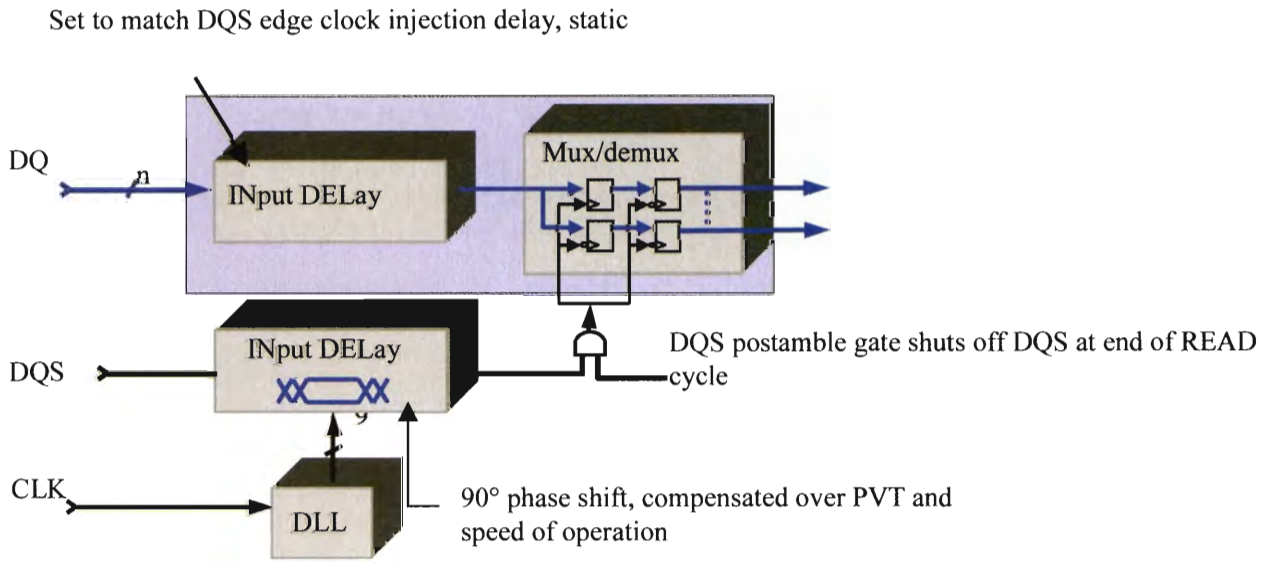


***Figure 3:** The memory controller uses on-chip PLLs and DLLs, along with programmable delay elements at the input buffers to align the DQS and DQ signals*

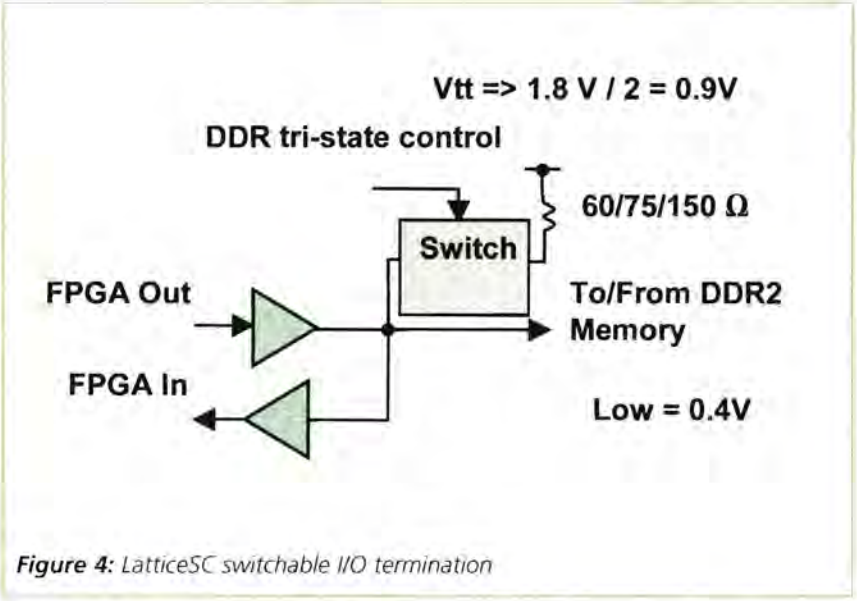


Figure 4: LatticeSC switchable I/O termination

accesses, like the next generation (10Gbps and beyond) networking applications.

Solutions

As previously stated, the high-speed clocks and data transfer rates are seriously challenging to today's design engineers. Lattice Semiconductor has taken a two-tier approach to the problem.

LatticeSC and LatticeSCM devices implement dedicated high-speed I/O circuitry to facilitate implementation of memory controllers supporting the various high-speed memory devices. The LatticeSCM in addition implements dedicated high-speed memory controllers on chip in hard logic ASIC technology to support these standards. The on-chip controllers are full-featured, fully tested controllers, providing users a low-risk time to market solution for high-speed memory interfaces.

The LatticeSC/SCM FPGAs feature innovative I/O technology termed "Purespeed" by Lattice. These I/Os include digitally controlled, on-chip linear input terminations and output impedance resistors. Inputs (input-only or bi-directional) feature the ability to provide internal termination. Two termination configurations are available: termination directly to VTT via programmable impedance, or termination via a Thevenin-equivalent resistor network across VDDIO and VSS. For DDR2 memory interfaces, the terminations can be switched on/off under tri-state control to support memory bus turnaround requirements. On-chip digital terminations provide the following benefits: they alleviate board layout considerations for the termination resistor and multiple modes and values are available, providing users with the flexibility to select the appropriate continuous return paths.

The LatticeSC I/Os contains five blocks (**Figure 2**): input register block, output register block, tri-state register block, update block and a control logic block. These blocks contain registers for both DDR data transfer and the necessary clock and selection logic. The input register block also contains delay elements and registers that can be used to condition signals before they are passed to the FPGA. The delay block allows users to align signals; it uses four blocks of 32 tapped delay lines to obtain coarse and fine delay resolution. These delays can be adjusted automatically via DLLs because the delay line in this block matches the delay line that is used in the 12 on-chip DLLs.

The delay line can be set via configuration bits, or driven from a calibration bus that allows the setting to be controlled either from one of the on-chip DLLs or user logic. Controlling the delay from one of the on-chip DLLs allows the DQ and DQS delay to be calibrated to the memory chip reference clock and so automatically compensated for the variations in process, voltage and temperature and system speeds.

DQ/DQS Implementation

Implementing high-performance DDR memory interfaces requires careful design of the read and write interface blocks of the memory controller. DDR2 memory devices pose a bigger challenge due to their higher speeds and the bi-directional DQS signal. The LatticeSCM memory controller utilises on-chip PLLs and DLLs, along with programmable delay elements at the input buffers to align the DQS and DQ signals (**Figure 3**). These elements work together to compensate for process, voltage and temperature variations, providing reliable operation at all operating conditions and various frequencies. These devices also contain dedicated DDR register structures in the inputs (for read operations) and in the outputs (for write operations). All these blocks are critical for implementing reliable high-speed DDR and DDR2 SDRAM controllers.

Switchable I/O Termination

DDR2 memory (and RLDRAM2 in common I/O mode) standards require that the on-chip termination to VTT to be turned on when a pin is an input, and off when the pin is an output (see **Figure 4**).The LatticeSC I/O also implements the DDR2 ODT control. The written signal enables the tri-state buffer while driving DQ out of the core to the memory. Termination is on all the time and is switched off only during writes to the DDR2 memory device. This mode is also used for DDR input to save power.

Embedded Memory Controller Advantages

The embedded memory controllers on the LatticeSCM devices provide customers with high performance, low risk solutions for interfacing to their external memory chips. Customers do not need to design a memory controller using FPGA gates, saving time and FPGA real estate while designing high-speed designs requiring high-speed external memory interfaces.

The embedded ASIC controllers also provide much higher performance than can be achieved by FPGA soft IP implementations. The power consumption for the ASIC implementation is approximately half the equivalent FPGA implementation.

ROCK'N'ROLL IN THE FPGA – EFFICIENT IMPLEMENTATION OF AUDIO ALGORITHMS

Philipp Jacobsohn, a Field Applications Engineer is responsible for providing technical support for all RTL synthesis, signal processing, ASIC prototyping and debugging products at Synplicity Deutschland. Here, he presents the Sinplify tool which can be used in the mapping of FPGA designs by the way of an example of a sampling rate converter used for all audio frequencies

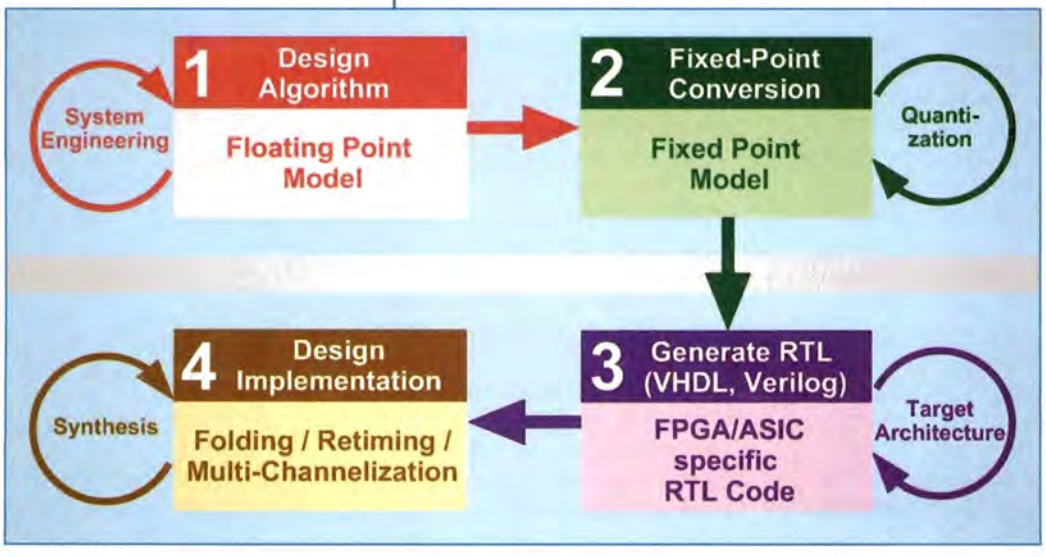
Today, even low-cost FPGAs provide far more computing power than digital signal processors (DSPs). Current FPGAs have dedicated multipliers and even DSP blocks (MAC) that enable signals to be processed with clock speeds in excess of 250MHz. Until now, however, these capabilities have had no impact on audio signal processing.

An implementation of an audio algorithm working in the kilohertz range uses exactly the same resources required for processing signals in the three-digit megahertz range. Consequently, programmable logic components such as PLDs or FPGAs are rarely used for processing low-frequency signals. This is because parallel processing of mathematical operations in hardware does not provide any benefits when compared with an implementation based on classical signal processors.

In fact, audio applications are characterised by such a high number of multiplications that they can only be implemented using highly complex FPGAs. So until now, applications with low sampling frequencies can be implemented more efficiently using DSPs, with lower costs and proven software support.

However, there are tools, such as the Synplify DSP tool, that allow even algorithms with many multiplications and a low sampling rate to be efficiently mapped onto FPGAs. Sunplicity's tool is based on the industry standard software Matlab/Simulink from The Mathworks. The algorithm is defined using a special block-set and/or a description in the proprietary "m" scripting language and later translated into the RTL hardware description language. The block-set allows both single-rate and multi-rate systems to be implemented. It not only generates VHDL and Verilog code but also handles tasks such as quantisation and connects to block-sets of the Simulink development environment required for simulation.

Figure 1: *The model is implemented, quantified and verified in Matlab/Simulink. Synplify DSP is used to convert the model into RTL code. The code can be optimised for space or speed*



Application Example: Sampling Rate Conversion

A sampling rate converter for audio frequencies is used as a practical example. This converter can be used to convert any low-frequency clock speed to any other

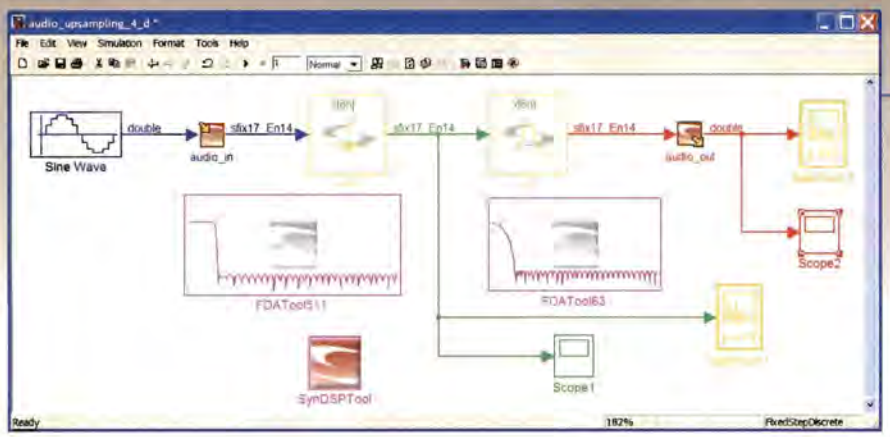


Figure 2: *Modules from the Synplify DSP block-set and the Simulink FDA tool are used to implement the sampling rate converter. Verification is also performed using Simulink block-set elements*

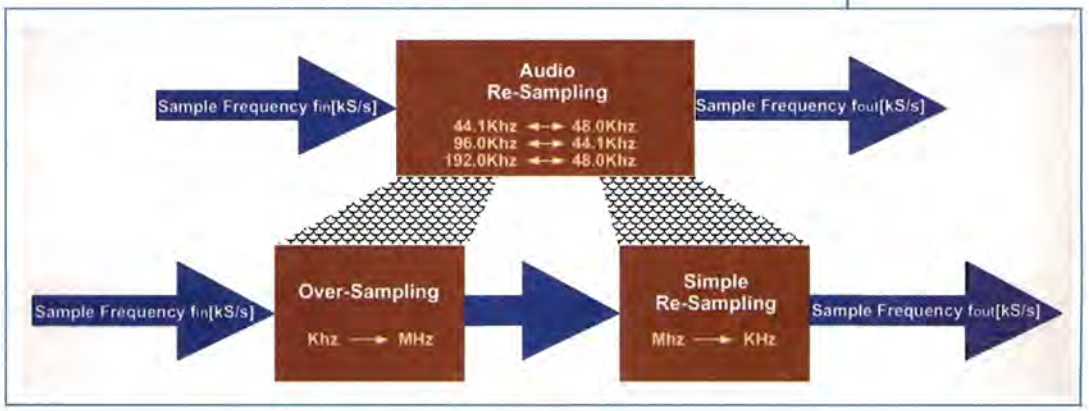


Figure 3: *The sample-rate converter is implemented in two steps to improve efficiency. Step 1: oversampling; Step 2: linear interpolation*

frequency. These converters are required to handle signals with different sampling rates. For example, European and US TV signals use different frame rates (fps) for image processing. If data is to be converted from one format to the other, playing the source data with the new sampling rate is not sufficient. Both the associated audio data and the video sequences would be out of sync. For this reason, the sampling rate must be converted.

When processing audio signals, sampling frequencies of 44.1kHz, 48kHz, 96kHz and 192kHz are used. A sampling rate of 44.1kHz is used for CDs. Professional applications use a sampling frequency of 48kHz to record signals on digital audio tapes (DAT). During conversion, care must be taken to maintain signal integrity between 0 and 20kHz. Changes to the information contained in the signal should be kept to a minimum to limit quality losses.

Not surprisingly, the implementation of the sampling rate converter for audio frequencies raises two issues in the FPGA:

1. **The algorithm issue**
   a. Highest possible signal-to-noise ratio
   b. Minimum possible change in the information carried by the original signal
   c. Efficient description of the algorithm. The resource load in the FPGA results from the quality of the description
   d. Quantisation
2. **The implementation issue**
   a. Logically correct implementation of the algorithm
   b. Space requirements
   c. Speed-optimised implementation
   d. Latency

This type of conversion requires a high clock-speed because the implementation requires/depends on adequate/sufficient oversampling. The difference between the FPGA system frequency and the frequencies to be converted must be correspondingly high. For CD quality audio signals, the signal-to-noise ratio must also be at least 100dB. Professional applications even require audio signals of > 120dB. Other low-frequency signals (e.g. control electronics algorithms) are far less demanding than audio signals when it comes to signal quality.

Algorithm

Signals with different sampling rates must be converted to enable processing. Audio signals normally have sampling rates of 44.1kHz (CD sampling rate) or 48kHz (DAT).

A polyphase FIR filter structure is used to convert the frequencies (asynchronous re-sampling). The algorithm consists of two steps. In the first step, frequencies are oversampled. The second step (linear interpolation) is required to generate a different frequency from a given frequency. The two frequencies are asynchronous to each other. Re-sampling the signal in a single step would require far more resources because the filter would be far more complex. This type of implementation would cause several million multiplications. Such a description is inefficient and must be avoided. If a linear interpolation is implemented for the second step, the resulting structures are far simpler.

Oversampling (the first step) must be described as efficiently as possible. This is the only way to achieve a resource-saving FPGA implementation. The number of computing operations required can be reduced dramatically if this part of the circuit is implemented in several cascaded stages rather than in a single computing step.

When implementing the algorithm, the designer must decide on the target architecture that will perform the computation (DSP, FPGA). Unlike digital signal processors, FPGAs are limited by their resources when implementing large numbers of individual multiplications. The number of multipliers required increases with the level of the filter. Each "tap" of the filter results in the use of a DSP block or 18 x 18 multiplier.

When cascading re-sampling stages, each filter must perform far less complex functions. In theory, an optimal implementation of the filter would result from as many

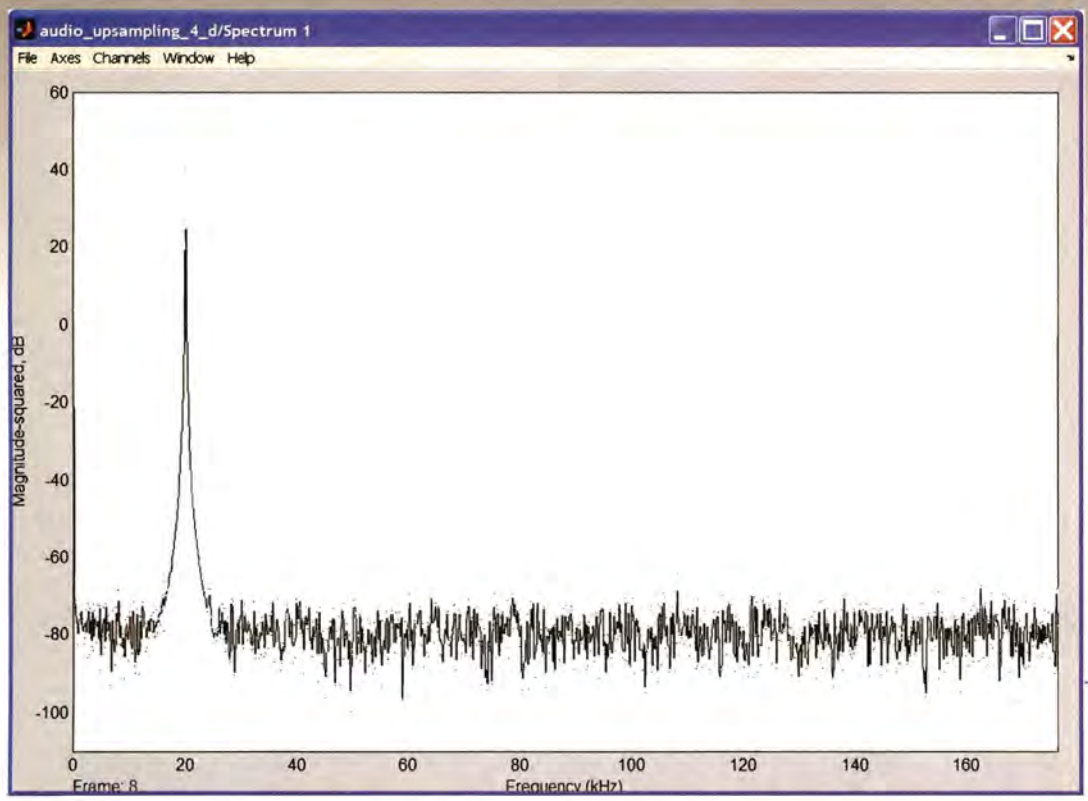
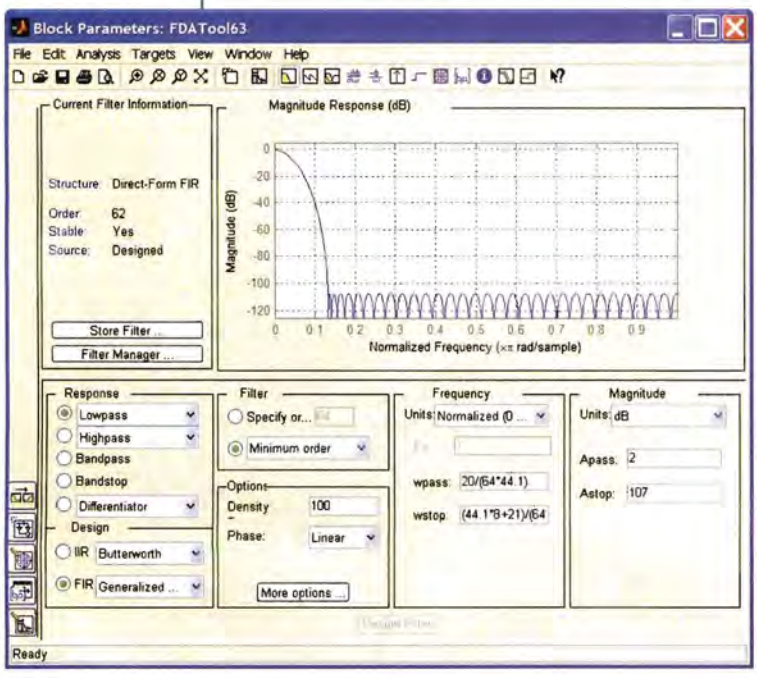


Figure 4: *Signal-to-noise ratio > 100dB. The algorithm meets all quality requirements for implementing audio sampling frequencies*

individual stages as possible. The mathematical deduction of how computing operations are reduced has been described extensively in the corresponding technical literature and will not be discussed here. However, practical results show that, while it is really necessary to cascade re-sampling stages, the number of cascades must be limited. If too many cascaded stages are introduced, more resources are needed because additional logic is required for the implementation. If an FPGA is used as the target architecture, the number 2 has proved to be optimal for the individual oversampling steps.

The entire circuit consists of two relatively simple filters for oversampling and a simple linear interpolation. This structure can be efficiently mapped onto an FPGA.

Figure 5: *The filters are implemented using Simulink's Filter Design and Analysis (FDA) tool*



Implementation

The circuit is implemented in Simulink using the Synplify DSP block-set and Simulink's Filter Design and Analysis (FDA) tool. The FDA tool allows FIR and IIR filters of any kind to be generated and verified. It is part of Simulink's Signal Processing Toolbox that Synplify DSP uses to implement filter structures.

All circuit components from the Synplify DSP block-set or the FDA tool which are defined between a PortIN and a PortOUT description, generate VHDL or Verilog code. FFT and SCOPE elements from Simulink block-sets are used for spectrum analysis and verification of the dynamic response. These blocks are exclusively used for functional verification including floating point to fixed point conversion effects (quantisation) and are not implemented in hardware.

The first part of the algorithm implementation consists of two FIR filters, the first of which has 512 and the second 64 taps. The RTL code resulting from oversampling, therefore, contains a total of 576 multiplications, which is why using FPGAs does not appear to be commercially viable. A highly complex FPGA costs several thousand Euros. Even the most complex programmable logic components do not provide sufficient multiplication resources to implement the circuit (Altera Stratix-2 EP2S180: 384 18 x 18 multipliers, Xilinx Virtex-4 XC4VSX55: 512 18 x 18 multipliers).

All multiplications that are not mapped onto dedicated hardware structures (DSP blocks) must be built from logic resources (LUTs, registers). This results in a high component load, as well as a low maximum clock speed.

Optimisation

Synplify DSP's folding option allows the number of multipliers used to be minimised virtually as desired.

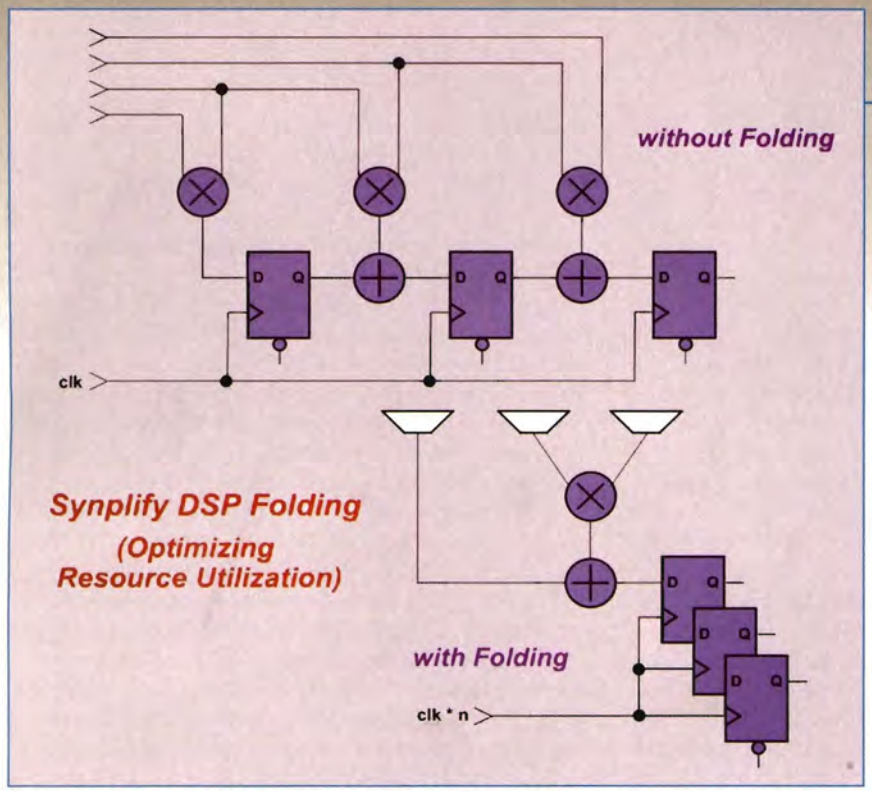
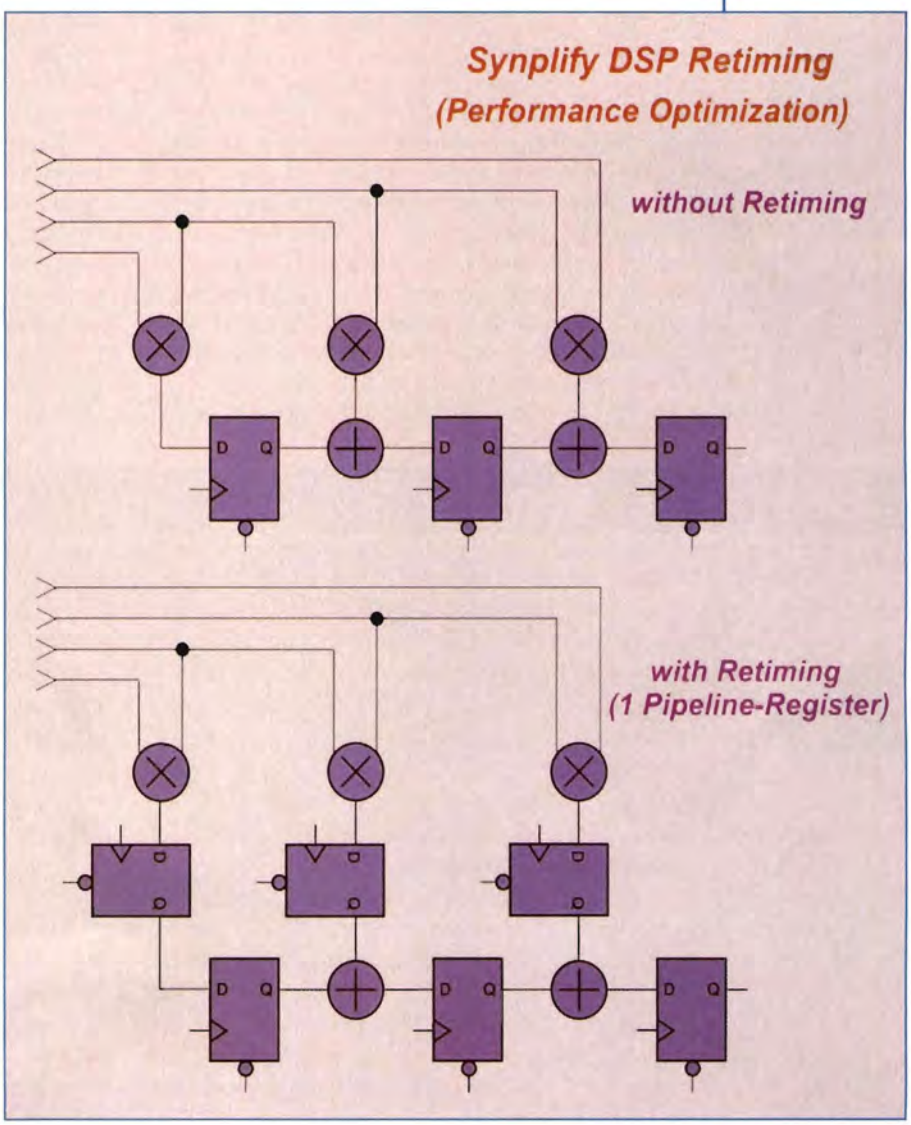


Figure 6: *The FPGA resources required can be reduced dramatically by using the folding feature*

Figure 7: *Using the retiming feature, the user can define the maximum latency allowed for the circuit. Synplify DSP then automatically adds pipeline stages until the desired frequency is achieved*



Particularly those circuits operating at low sampling frequencies can benefit from this optimisation. The idea is simple: Normally, one hardware multiplier is used for each multiplication, even when the sampling frequency is in the kilohertz range. However, FPGAs can operate with clock speeds in the double-digit megahertz range and, often, even in the three-digit megahertz range. If the hardware multiplier operates at the system frequency of the FPGA, multipli-cations can be processed sequentially using a time multiplex process.

Here's a practical example: If the sampling frequency of the circuit is 3MHz and the FPGAs can run at a maximum of 120MHz, each hardware multiplier can perform 40 computing operations if the system frequency is used for multiplication. The necessary hardware is, therefore, reduced by a factor of 40. But audio signals are not processed with megahertz sampling frequencies. Standard sampling frequencies are 44.1, 48, 96 or 192kHz. This means that a sampling rate converter as described above (or any other circuit using low sampling frequencies) can be "folded" to the point where only very few hardware multipliers are required. Therefore, this can also be implemented in the smallest available low-cost FPGAs.

Offered by all FPGA makers at low cost, these components represent a real alternative to DSPs. Of course, it is also possible to offload particularly compute-intensive algorithms from a DSP to an FPGA, thereby reducing the load on the processor.

Since the folding feature in Synplify DSP also supports multi-rate systems, the number of multipliers required can be reduced even more than in a system with a single sampling frequency.

Oversampling is performed using two FIR filters. These two filters run at different sampling frequencies. The filter running at a higher sampling frequency is folded using a folding factor specified by the user. The filter with the lower sampling frequency is folded using a correspondingly higher factor. This factor is obtained by multiplying the difference between the sampling frequency of the two filters by the folding factor defined by the user. For example, if the sampling frequency of one filter is eight times higher than the sampling frequency of the other filter, the faster filter is folded by a factor of eight and the slower filter is folded by a factor of 64.

In this way, it is even possible to produce space optimised circuits running at very high sampling rates, which normally cannot be folded. For example, if a system runs at a sampling rate of 200MHz and a folding factor of two is used, the system frequency increases to 400MHz. This speed can hardly be achieved even with top-performance FPGAs.

There's an alternative, where a folding factor of one is defined. Those circuit components running at the highest sampling rate are not folded. However, all circuit components of a multi-rate system running at slower sampling frequencies benefit from folding and space-optimised implementation. The user only needs to define the folding factor for the system as a whole. Folding is then propagated automatically across all sampling frequencies.

The folding feature can be combined with an additional optimisation functionality, the re-timing feature. If a system does not meet the target frequency requirements, pipeline stages can be added until the desired rate is achieved. This is particularly important for circuits with a significant folding factor which need to operate at a correspondingly high system speed. Of course, re-timing can also be used for circuits with little or no folding but where the performance limit of the FPGA is reached.

Adding pipeline stages allows the number of combinatorial gates between two registers (logic levels) to be reduced to the point where the combinatorial gate delays no longer slow down the clock speed. When generating the RTL code, Synplify DSP performs a timing analysis that takes the desired sampling frequency, the folding factor and the target architecture of the FPGA into account. A circuit mapped to a fast FPGA, for example Xilinx Virtex-4 or Altera Stratix-2, can be optimised using fewer pipeline stages than an identical circuit implemented in a slow low-cost FPGA such as Lattice ECP-2 or Xilinx Spartan-3 for example.

FPGAs provide large numbers of registers that can be used for this optimisation. Unlike multipliers or LUTs (look-up tables), which can rapidly be used up, registers are available in abundance, which means that the system clock speed can be increased significantly with little effort using registers. Of course, adding pipeline stages increases system latency. By introducing a re-timing factor of eight for example, the result of the computation will appear eight system clock cycles (not sampling frequency cycles!) later at the FPGA's output. This must be taken into account when embedding a circuit in a system.

It is particularly important to ensure that the optimisations described previously do not impact the model described in Matlab/Simulink. The algorithm is implemented and verified in Simulink. Verification allows the algorithm to be validated and the impact of quantisation effects to be represented. The Synplify DSP software block-set allows floating to fixed point conversion to be performed either using truncation (elimination of irrelevant bits), rounding (in case of underflow) or saturation (in case of overflow). As soon as the simulation shows that the algorithm works as intended, the RTL code can be generated. Optimising the VHDL or Verilog code may change latency, but not the operation of the circuit.

THE SYNPLIFY TOOL

Synplify DSP is based on the industry standard software Matlab/Simulink from The Mathworks. A block-set provides a library of standard components that can be used to implement complex algorithms. Apart from basic components such as Add, Gain and Delay, the library contains many complex functions such as FIR or IIR filters and Cordic algorithms.

All features, including the highly complex FFT or the Viterbi decoder, can be parameterised as desired. It is also possible to create user-defined libraries or integrate existing VHDL or Verilog code into a Simulink model.

Synplicity also provides a wide range of reference circuits from applications such as image processing, software defined radio and audio, free of charge. The application described in this article, i.e. the sampling rate converter, which can be used for all audio frequencies, is available for free as a reference design.

The tool allows both single- and multi-rate systems to be implemented. Using folding, multi-channelisation or re-timing, the code can be optimised for either space or speed. The RTL code generated is always generic, non-encrypted code that can be synthesised using all popular tools. For best results with FPGAs, Synplicity recommends its own synthesis product, Synplify Pro, which supports FPGAs of all major manufacturers – Actel, Altera, Lattice, Quicklogic and Xilinx.

An ASIC variant of the development environment is also available.

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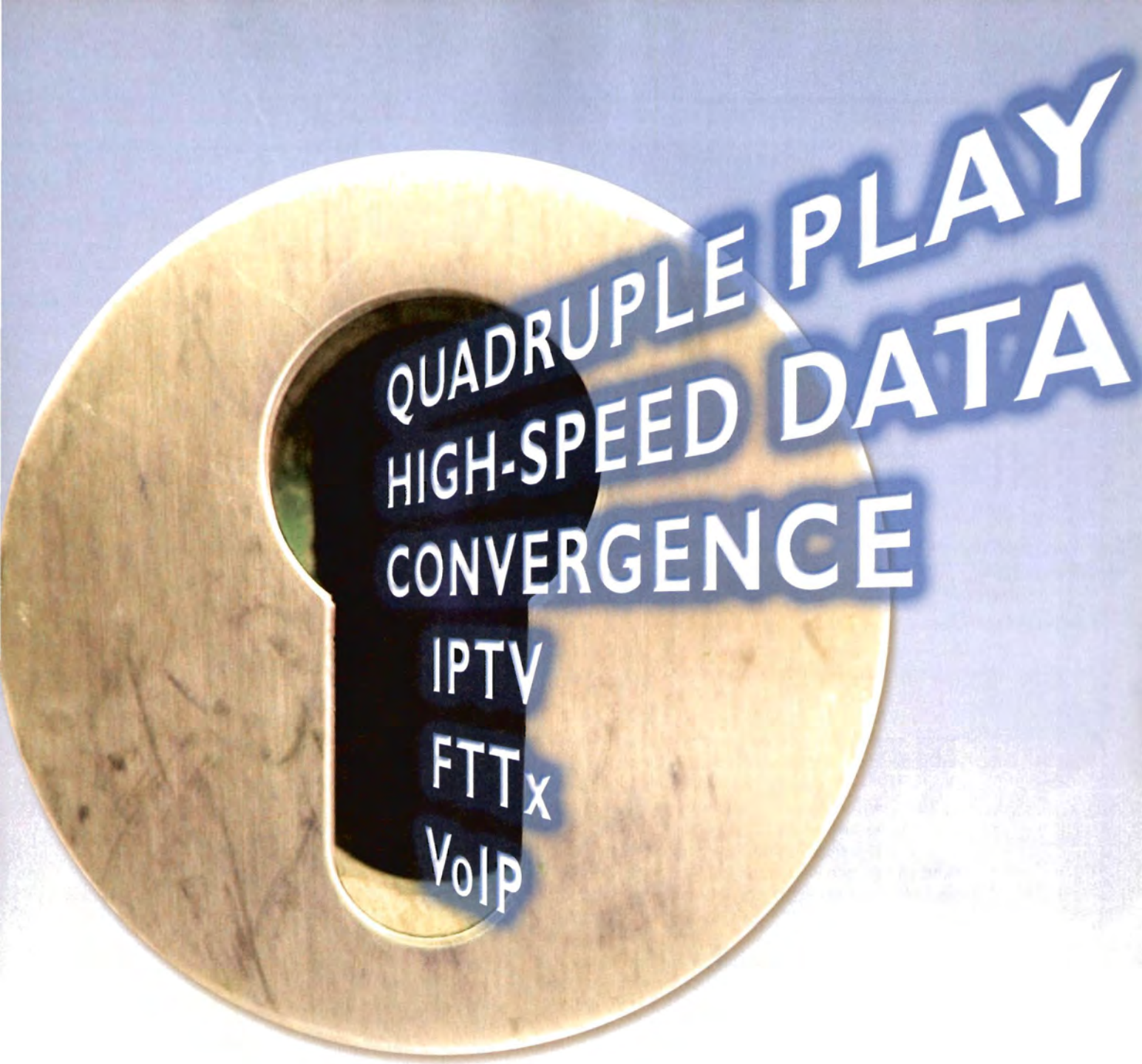

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Mixing it with **FPGAs** and **DSPs** in **WIRELESS BASESTATIONS**

DEEPAK BOPPANA, TECHNICAL MARKETING ENGINEER AT ALTERA'S WIRELESS BUSINESS UNIT, PRESENTS AN EFFICIENT SYSTEM DESIGN PLATFORM FOR WIRELESS BASESTATIONS THAT MAKE THE MOST OF FPGAs AND DSPs

"Intelligent partitioning" between FPGAs and DSPs allows wireless systems designers an optimal combination of features and cost-effectiveness. Currently there is no 'one fits all' design solution. Applying a mix of DSPs and FPGAs brings future proofing as well as risk-free cost-reduction benefits. System partitioning combining programmable logic with DSPs for wireless basestations leads to greater design and market success.

The need for higher data rates are driving the evolution of wireless cellular systems from narrowband 2G GSM, IS-95 systems to current-generation, W-CDMA based 3G and 3.5G systems supporting peak data rates of up to 10Mbps. Future 3GPP long-term evolution specifications point to complex signal processing techniques such as Multiple-Input Multiple-Output (MIMO), along with new radio technologies like Orthogonal Frequency-Division Multiple Access (OFDMA) and multicarrier Code Division Multiple Access (MC-CDMA). These approaches will be key to achieving target throughputs in excess of 100Mbps.

Alternate OFDM-based broadband wireless systems such as WiMAX are now achieving transmission speeds in excess of 70Mbps. This improvement in data rates has been enabled by higher order modulation techniques and variable rate channel coding. Complex spatial signal processing schemes, including beam forming and MIMO antenna techniques, are also paths to increasing data rates at the expense of additional hardware. However, these technologies create challenges for basestation designers requiring scalability and cost-effectiveness, as well as flexibility across multiple evolving standards.

Multiple Moving Targets

Wireless systems designers need to meet a number of critical requirements, including processing speed, flexibility and time-to-market. These all ultimately drive hardware platform choices. The major variables include processing bandwidth, flexibility and a cost-reduction path.

Processing bandwidth: WiMAX broadband wireless systems have significantly higher throughput and data rate requirements than W-CDMA and cdma2000 cellular systems. To support these higher data rates, the underlying hardware platform must have significant processing bandwidth. Additionally, several advanced signal processing techniques such as turbo coding/decoding and front-end functions including Fast Fourier Transform/Inverse Fast Fourier Transform (FFT/IFFT), beamforming, MIMO, Crest Factor Reduction (CFR) and Digital PreDistortion (DPD) are computationally intensive, requiring several billion multiply and accumulate (MAC) operations per second.

Flexibility: WiMAX is a relatively new market and is currently in the initial development and deployment stages. Similarly, 3GPP LTE is being defined and will go through numerous revisions before being finalised. It is still unclear which of the many "mobile broadband technologies" (i.e. WiMAX, Wibrow, Super 3G, LTE, Ultra 3G, etc.) will be heavily adopted.

Currently, end-product flexibility and reprogrammability are essential to a standard-agnostic or multi-protocol basestation. Systems offering this flexibility can significantly reduce the capex and opex costs for wireless system makers and operators while alleviating risks posed by ever evolving standards.

Cost-Reduction Path: A valuable lesson learned from designing and deploying 3G systems is the importance of establishing a long-term cost-reduction strategy in the beginning. Evolving WiMAX and LTE standards are expected to stabilise. This is likely to lead to a situation where the cost of the final product will be more important than flexibility in order to remain competitive for OEMs and service providers. Choosing the right hardware platform for prototyping that provides a seamless cost-reduction path to production will save millions in engineering costs otherwise required for system re-design.

System Architecture Logic Task Partitioning

Control, signal-processing and data path operations make up the bulk of the processing load in a wireless basestation. Most approaches accomplish these with combinations of microcontrollers (MCUs), FPGAs and programmable DSPs. The MCU controls the system, while the FPGA and DSP handle the data-flow processing. Systems with light processing demands and control-oriented tasks are implemented in software on a DSP; heavier loads are best implemented in FPGAs with their significant parallel processing abilities.

Combining DSPs and FPGAs ensures complete system flexibility and offers reprogrammability to fix bugs or even support different standards. The partitioning strategy between them depends on the processing requirements, system bandwidth as well as system configuration, and the number of transmit and receive antennas. **Figure 1** shows a typical DSP/FPGA partitioning for baseband physical layer (PHY) functions in an OFDMA-based system such as WiMAX or LTE.

By incorporating advanced multiple antenna technologies, the throughput offered by such systems is expected to be between 75 and 100Mps. The baseband PHY functionality can be broadly categorised into bit-level processing and symbol-level processing functions.

Bit-Level Processing

The bit-level blocks include randomisation, Forward Error Correction (FEC), interleaving and mapping to Quadrature Phase Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM) functions on the transmit side. The corresponding receive processing bit-level blocks are symbol de-mapping, deinterleaving, FEC decoding and de-randomisation.

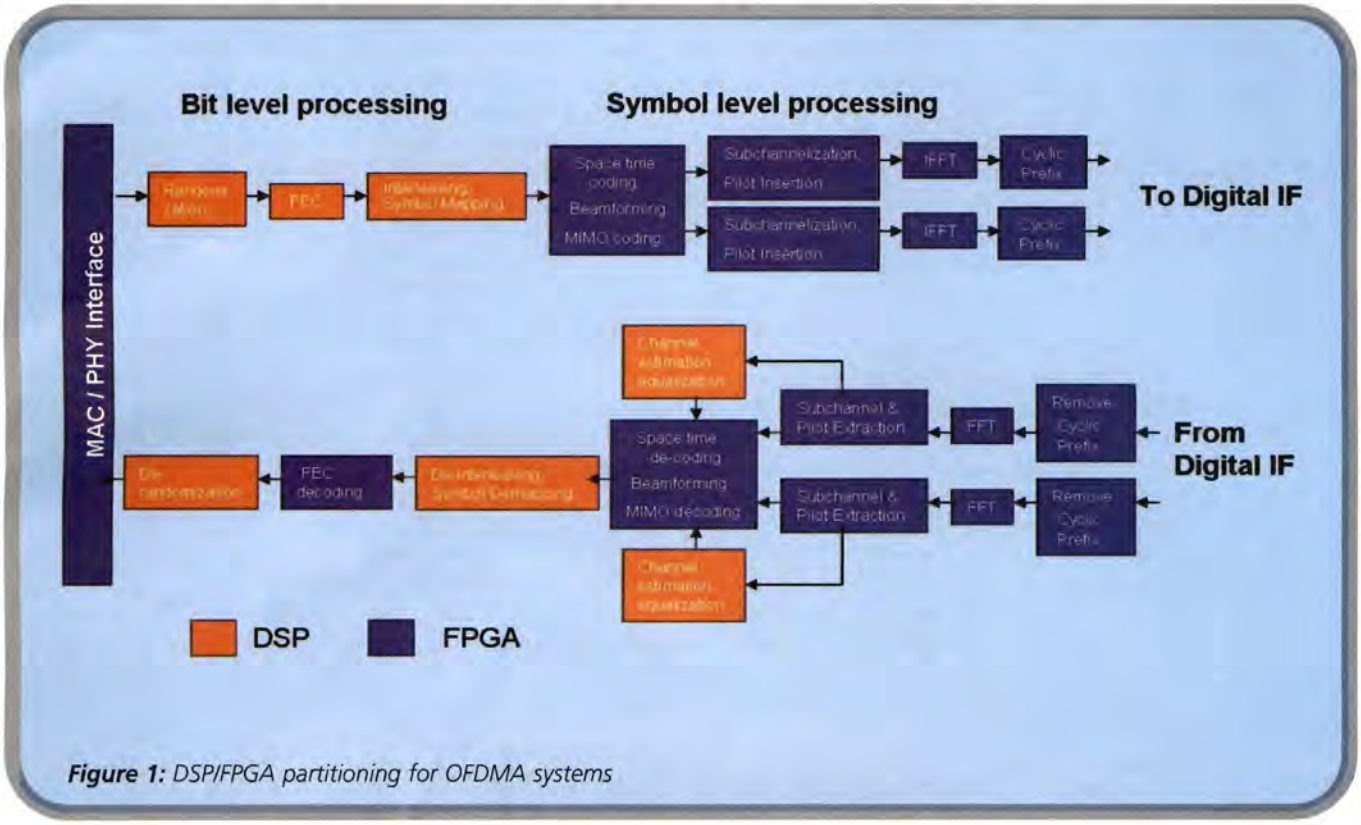

Figure 1: *DSP/FPGA partitioning for OFDMA systems*

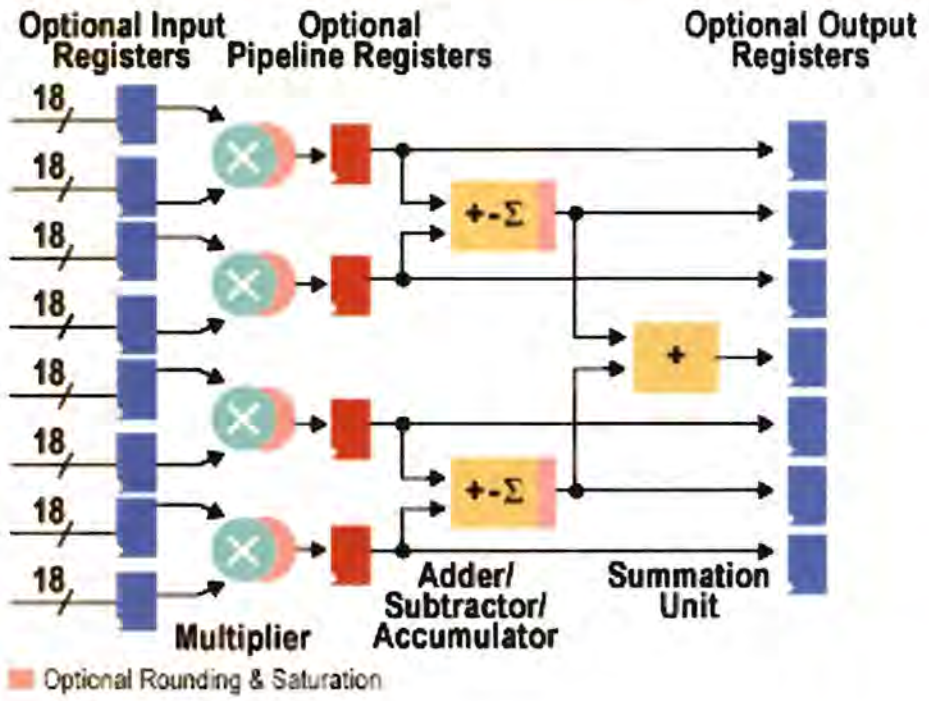

Figure 2: *Embedded DSP blocks in FPGAs*

All bit-level functions, except FEC decoding, are relatively straightforward and not computationally-intensive. For example, randomisation involves modulo-2 addition of the data bits with the output of a simple pseudo-random binary sequence generator. Although FPGAs offer more flexibility for bit-level manipulations than DSPs with fixed bus widths, the low computational complexity allows DSPs to manage these functions. Conversely, FEC decoding – including Viterbi decoding, Turbo convolutional decoding, Turbo product decoding and LDPC decoding – are computationally intensive and consume significant bandwidth when done with DSPs.

FPGAs are widely used to offload these functions and free DSP bandwidth for other functions. The same FPGA can also be used to interface to the MAC layer as well as implement certain lower MAC functions such as encryption/decryption and authentication.

Symbol-Level Processing

Symbol-level functions in OFDMA systems include sub-channelisation and de-subchannelisation, channel estimation, equalisation and cyclic prefix insertion and removal functions. The time-to-frequency domain conversion and vice versa are implemented using FFT and IFFT, respectively.

Channel estimation and equalisation can be performed offline and involve more control-oriented algorithms that are better suited for DSPs. Conversely, FFT and IFFT functions are regular data path functions involving complex multiplications at very high speeds and are better suited for implementation on FPGAs.

Figure 2 shows the embedded DSP blocks contained in a high-end FPGA (Altera Stratix II device). DSP processors typically have up to eight dedicated multipliers, whereas Stratix II devices offer up to 384 18 x 18 dedicated multipliers providing throughputs of up to 346GMACs; an order of magnitude higher than currently available DSPs.

Such a massive difference in signal processing capability between FPGAs and DSPs is further accentuated when dealing with base-stations employing advanced, multiple antenna techniques such as Space Time Coding (STC), beamforming and MIMO schemes. The combination of OFDM-MIMO is widely regarded as a key enabler of higher data rates in current and future WiMAX and LTE wireless systems.

Figure 1 shows multiple transmit and receive antennas employed at a basestation. In this configuration, symbol processing functions are implemented separately for each antenna stream before MIMO decoding is performed, producing a single bit-level data stream. The symbol-level complexity grows linearly with the number of antennas when implemented on DSPs that perform operations in a serial manner. For example, when two transmit and two receive antennas are used, the FFT and IFFT functions consume approximately 60% of a 1GHz DSP when the transform size is assumed to be 2048 points. In contrast, a multiple antenna-based implementation scales very efficiently when implemented with FPGAs. FPGAs provide parallel processing and time-multiplexing between the data from multiple antennas.

Multiple antenna schemes provide higher data rates, array gain, diversity gain and co-channel interference suppression. Beamforming and spatial multiplexing MIMO techniques are also computationally-intensive, involving matrix decompositions and multiplications. Specifically, Cholesky decomposition, QR decomposition and singular value decomposition functions are useful in solving the linear set of equations common in these systems. While these functions quickly exhaust DSP capabilities, they are well suited for FPGAs using well-known systolic array architectures that provide a more cost-effective solution by exploiting FPGA parallelism.

Digital IF Processing

Figure 3 shows data from a baseband channel card being sent to a RF card for subsequent digital Intermediate Frequency (IF) processing, including Digital Up-Conversion (DUC), CFR and DPD. Digital IF extends the scope of digital signal processing beyond the baseband domain to the antenna – to the RF domain. This increases the flexibility of the system while reducing manufacturing costs. Moreover, digital frequency conversion provides greater flexibility and higher performance (in terms of attenuation and selectivity) than traditional analogue techniques.

CFR and DPD functions are required to improve the efficiency of power amplifiers used in basestations. These functions also help to significantly reduce the total cost of the RF card. Both CFR and DPD involve complex multiplications at sample rates as high as 100+ MSps. Similar to DUC, Digital Down-Conversion (DDC) is required on the receive side to bring the IF frequency down to baseband. Both DUC and DDC use complex filter architectures including Finite Impulse Response (FIR) and Cascaded Integrator-Comb (CIC) filters. Advanced FPGAs provide hundreds of 18 x 18 multipliers running at speeds as high as 350MHz. Not only does this provide a platform capable of processing multiple channels in parallel, it also yields a cost-effective, integrated single-chip solution.

Effective Design Approach

As standards stabilise, the initial need for flexibility in basestations should subside while cost becomes a major success factor. Choosing FPGAs that have a risk-free migration path to low-cost structured ASIC technology will enable significant cost savings. As an example Altera's HardCopy II technology provides a seamless, risk-free migration path from Stratix II FPGAs to significantly lower cost HardCopy II structured ASICs, while also increasing system performance and decreasing power consumption.

Hybrid FPGA/DSP based platforms provide an effective design approach for wireless basestations. What's essential to product success is intelligent partitioning between the FPGA and DSP based on system throughput requirements and long-term cost considerations. This will ensure final products that are not only scalable and cost-effective, but flexible and reconfigurable across multiple evolving standards.

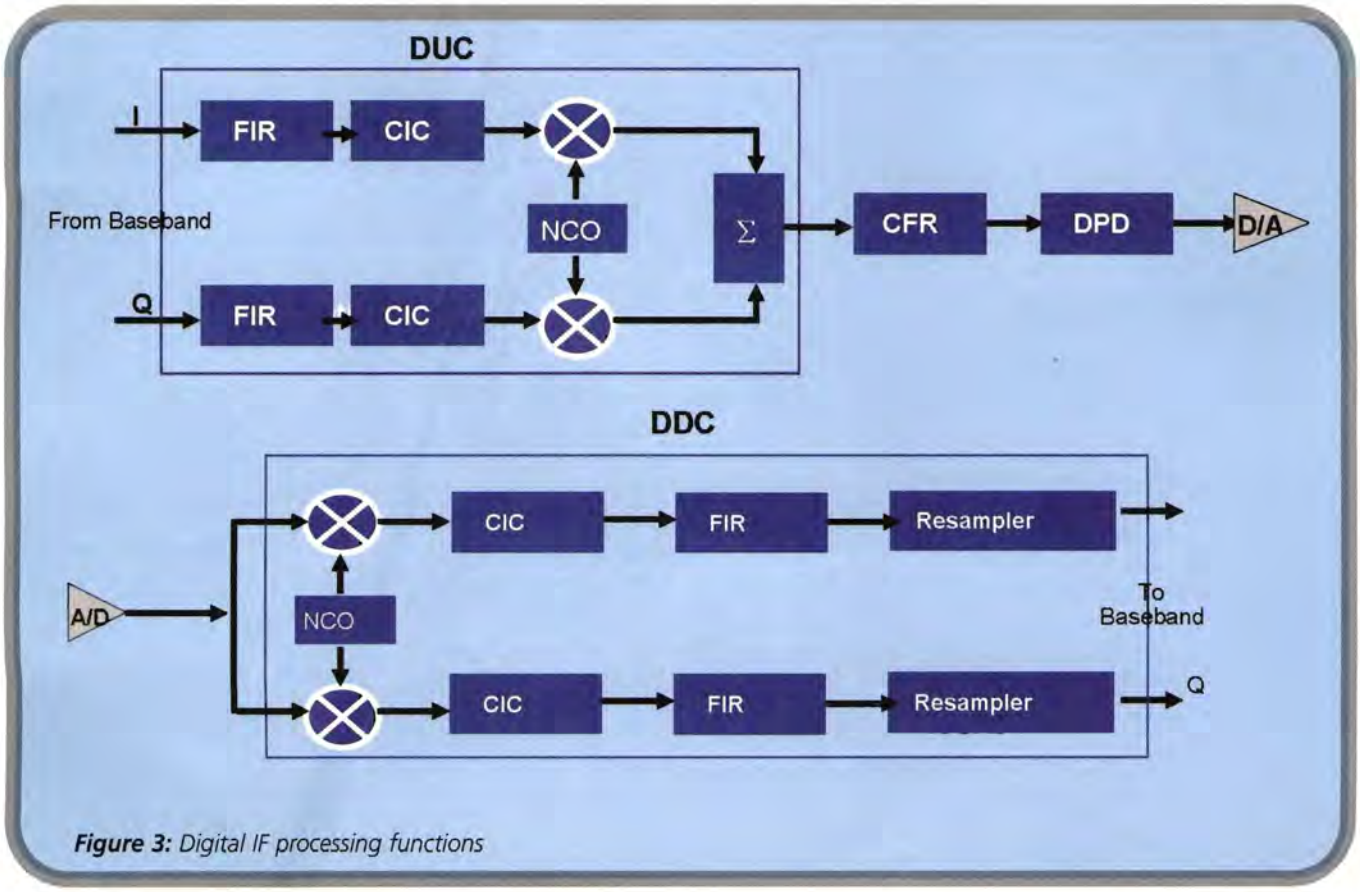

Figure 3: *Digital IF processing functions*

A DOUBLE-FEEDBACK CONSTANT CURRENT SOURCE SUITABLE FOR LDs AND LEDs

In this article we present a type of frequency adjustable current supply, which originally has two kinds of feedback patterns – the current and the light power feedback patterns – to achieve the goal of constant output light power.

Compared to the current feedback pattern, the experimental results showed that the light power output was more stable through the light power feedback pattern. This device is suitable for light emitting diodes (LEDs) and laser diodes (LDs) with or without photo a diode (PD).

Since the laser diode (LD) and light emitting diode (LED) have been invented, due to their advantages, such as small volume, high efficiency, merits and low price, they have been used in widespread applications. One of LD and LED's characteristics is that their output light can be modulated by the drive current directly.

Because the output light power and the input current have linear relations, the LD and LED may use the analogue or digital signal to modulate the frequency output directly. This, instead of the expensive modulator, make the applications of LD and LED more economical. Now the design of the frequency modulation, constant-current source becomes a major problem for the applications of LD and LED. This article introduces a kind of frequency modulation constant current source which has two feedback patterns to choose from: current and light power feedback patterns. This device is suitable for LDs and LEDs. For the LED and LD without PD, the current feedback pattern can be selected. For the LD with PD, the light power feedback pattern is better for getting a more stable light power output.

The Circuit

Figure 1 depicts the principle block diagram of the circuit. What the entire system realises is to control the output current or the output light power. The power supply module (1) provides the power this device needs. The power output feeds the actuation module (2) to produce the actuation current.

Here, different feedback patterns could be selected through the pattern choice module (3). When the current feedback pattern is chosen, the actuation current, which is provided by the actuation module (2), will pass the current sample resistor as a feedback signal. Then, the current feedback signal will be sent to the feedback quantity processing module (7) to obtain the final feedback quantity.

The final feedback quantity is sent to the feedback quantity control module (4). It will compare with the input control signal to produce the final control signal. This signal will be fed back to the actuation module (2) to control the actuation current. So, the goal of steadying and modulating the actuation current will be achieved.

The main principle to keep the output current constant in this circuit is as follows:

$$I_O \uparrow \xrightarrow{R_f \rightarrow,\ V_{\square} \uparrow, V_{\square} \uparrow,} V_f \uparrow \xrightarrow{\text{The input increases, the output reduces}}$$

$$V_C \downarrow \xrightarrow{\text{The control voltage and the output current are proportional}} I_O \downarrow$$

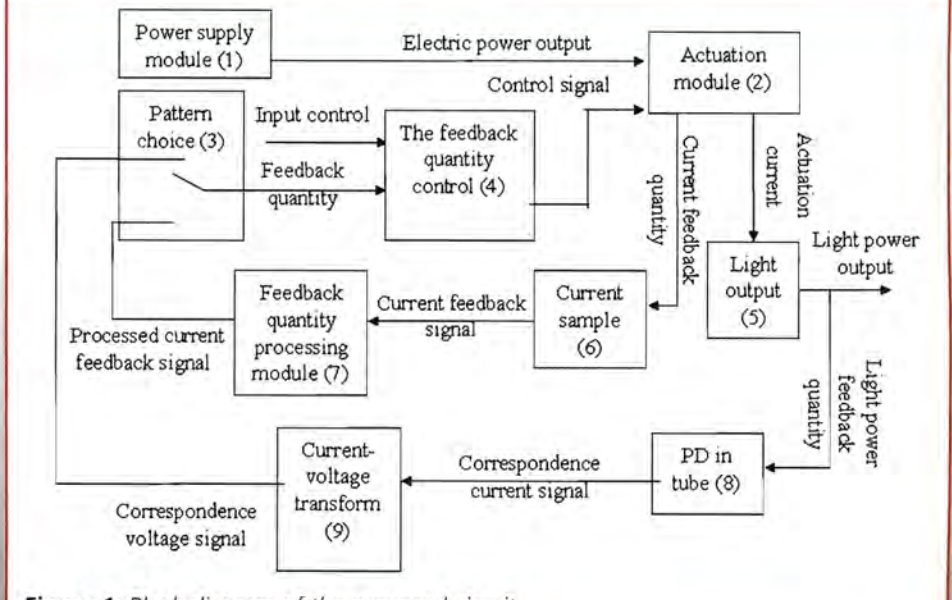

Figure 1: *Block diagram of the proposed circuit*

JIANG BOSHI, JIA HONGZHI AND FAN XUETING FROM THE COLLEGE OF OPTICAL AND ELECTRONIC INFORMATION ENGINEERING AT THE UNIVERSITY OF SHANGHAI, CHINA, PRESENT A TYPE OF FREQUENCY ADJUSTABLE CURRENT SUPPLY

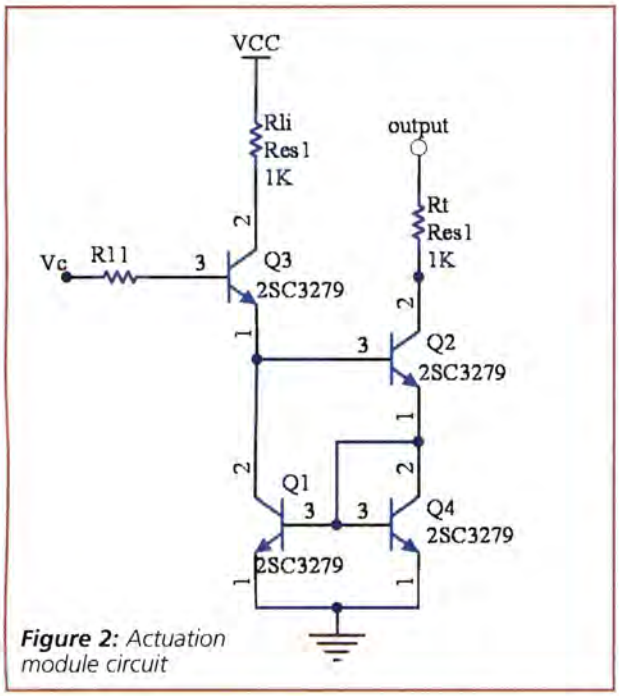

Figure 2: *Actuation module circuit*

Here, I_0 is the actuation current, V_{f1} and V_{f2} are the voltages between the two ends of the sample resistor R_t, V_f is the voltage before processing and Vc is the voltage after processing.

When LD with PD is driven by this device, the light power feedback pattern can be chosen in the pattern choice module (3). The PD (8) receives the light power output and produces correspondence current signal. This signal is changed to a corresponding voltage signal by the current-voltage transform module (9). The voltage signal is sent to the feedback quantity control module (4) as feedback quantity, and compared to the input control signal to produce the final control signal. This final signal controls the actuation current in the actuation module (2). Then, the light power output can be steadied and modulated.

Power Supply and Actuation Module

The ring transformer is chosen to obtain the suitable power supply voltage. Each rectifier tube is connected with a small capacity in parallel to avoid the high frequency damage.

Figure 2 is the actuation module circuit. Vcc is the power input voltage. R_t is the sampling resistor. In fact, the structure of the actuation module is a Wilson current supply that is connected in series with a triode Q3 at its input. The input voltage Vc controls the output current. Here Vc is the control signal that is produced in the feedback quantity control module.

Current Sampling

Experiments proved that, in the current sources, the precision level of sampling resistor affects the stability of the current output directly. In the experiment, 5.1Ω precision metal membrane resistor is used, whose temperature drift is less than 5ppm/°C and rated power is 5W.

* **Feedback processing module**

Figure 3 is the circuit of feedback processing module. This part mainly processes the feedback quantity to enable the circuit to obtain the appropriate sample signal. The main question of this part is the saturated problem in the operational amplifier circuit.

Two groups of coordinated resistors R1~R4 pull down the voltage between the two ends of the sample resistor to half

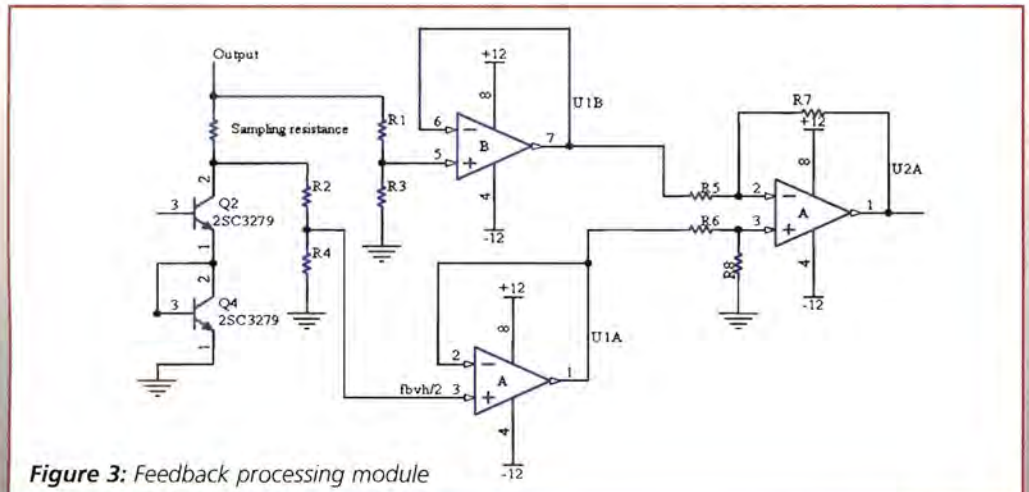

Figure 3: *Feedback processing module*

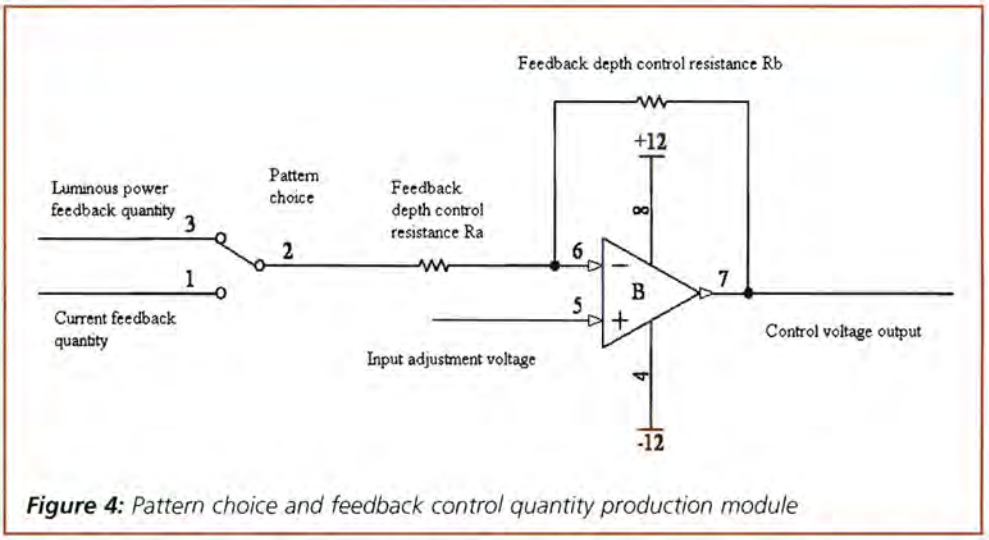

Figure 4: *Pattern choice and feedback control quantity production module*

value. This is mainly because the operational amplifier is not ideal. Therefore, when the difference voltage between positive and negative input ends is too big, the output voltage will be saturated. These resistors make the greatest output voltage of the operational amplifier to be smaller than the half of supply voltage. Then, the saturated problem is solved.

After passing through two followers, which are composed by the operational amplifier, the pulled down sample voltages are sent to the differential input ends of the amplifier.

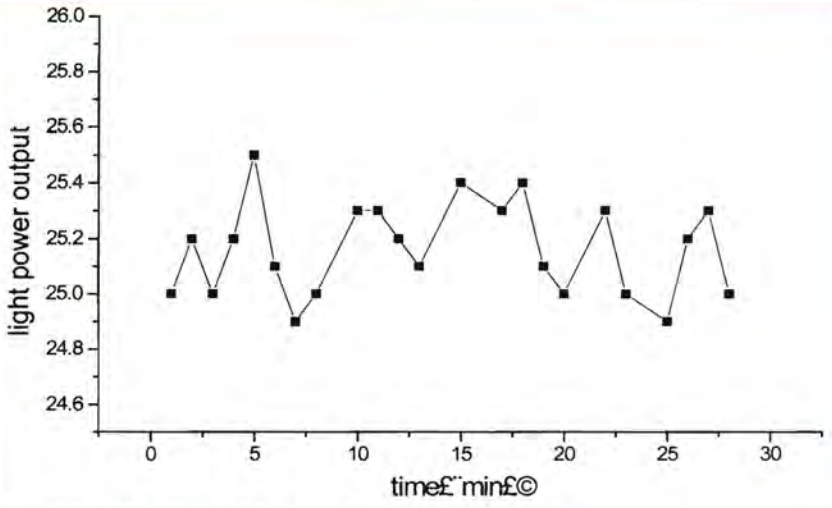

Figure 5: *The time stability of LED light power output*

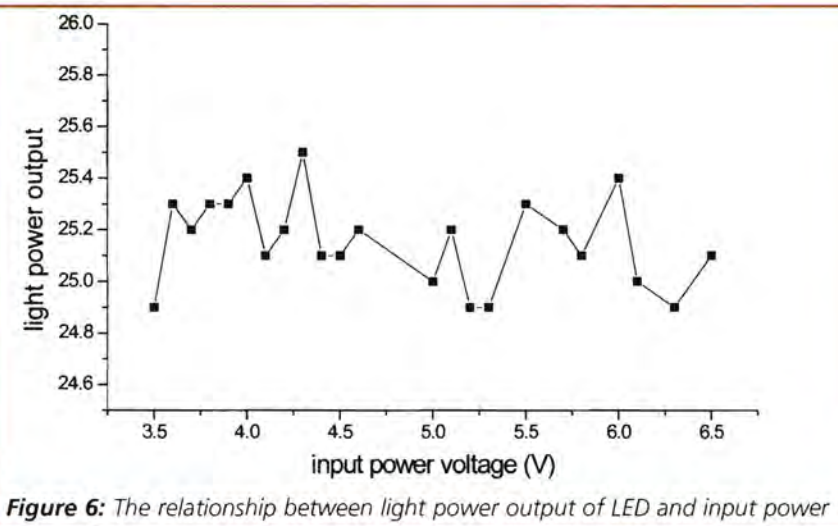

Figure 6: *The relationship between light power output of LED and input power*

*** Output and feedback pattern choice module**

The output device may be the LD or LED with or without PD. We can choose the pattern depending on whether it has a PD with it. For the light power feedback pattern, we use a simple resistor to transform the current signal to voltage signal. We already have a voltage value from the output light power or the output current. Either of them can be chosen as the feedback quantity. Here, a single pole, double throw switch is used to choose the feedback pattern.

Figure 4 is the circuit of pattern choice and feedback control quantity production module. It produces the control quantity output directly. This circuit is a differential amplifier. It enlarges the difference between adjustment voltage and the feedback voltage. Ra~Rb are feedback depth control resistors; they can control the depth of feedback by changing their resistance value.

Experimental Results and Analysis

Ordinary red LED and LD are used to test this device. The CA1640-20 signal generating device from Caltek Corporation provides the control signal. The GI-3D light power meter from Guilin Laser Communication Research Institute is used to measure the output light power. The experimental results are as follows:

(1) LED

Figure 5 is the time stability of LED light power output. The LED output light power is steady within 30 minutes. Its stability degree is 2.3% (from 24.9μW to 25.5μW).

Figure 6 is the relationship between light power output of the LED and the input power voltage. It shows that when the power input voltage is increasing from 3.6V to 6.0V, the output light power stability degree is 2.7% (from 24.8μW to 25.5μW).

(2) LD

The LD used in our experiment is integrated with a PD. Under the light power feedback pattern and current feedback pattern, the output light power of the LD is measured.

Figure 7 is the time stability of LD light power output. The light power output stability degree is 1.7% (from 4.05mW to 4.12mW) with light power feedback pattern, and 2.9% (from 4.02mW to 4.14mW) with current feedback pattern.

Figure 8 shows that when the power input voltage is increasing from 3.5V to 6.0V, the light output power stability degree is 1.9% (from 4.05mW to 4.13mW) with light power feedback pattern, and 3.1% (from 4.02mW to 4.15mW) with current feedback pattern.

Figure 9 is the characteristic of the frequency response for the LD. From this figure, we can see that when the modulation frequency is about 1MHz, the output light power of the LD drops to half value of the direct current.

LED and LD Suitable

A double-feedback, frequency-adjustable, constant current source suitable for LD and LED is produced. Because of its double feedback patterns, it is suitable for LEDs and LDs with or without a PD. Experimental results show that the output light powers of the LED and LD have high stability. The time stability degree and the stability degree under different voltages with output light power feedback pattern are better than with the current feedback pattern. The response frequency of this device is about 1MHz.

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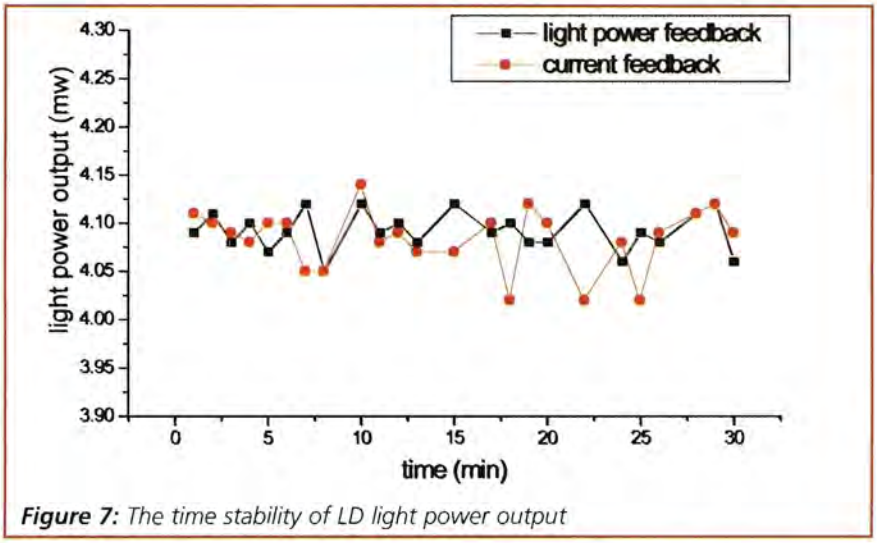

Figure 7: *The time stability of LD light power output*

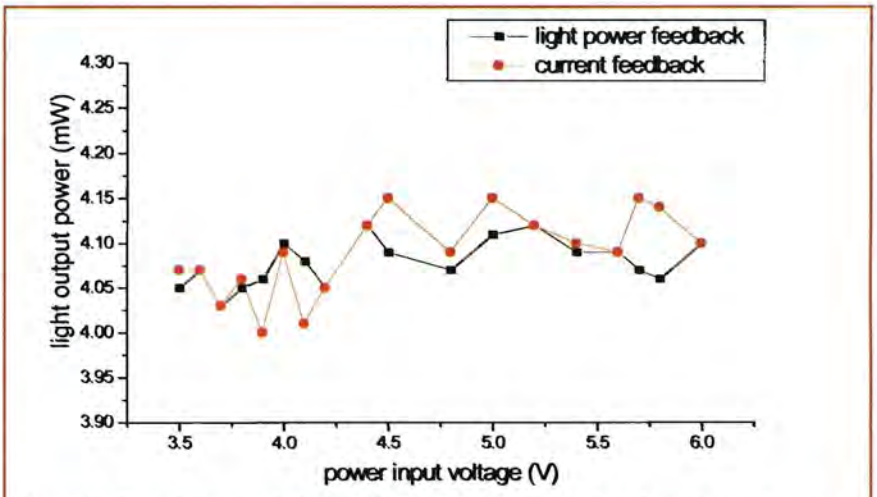

Figure 8: *The relationship between light power output of LD and input power voltage*

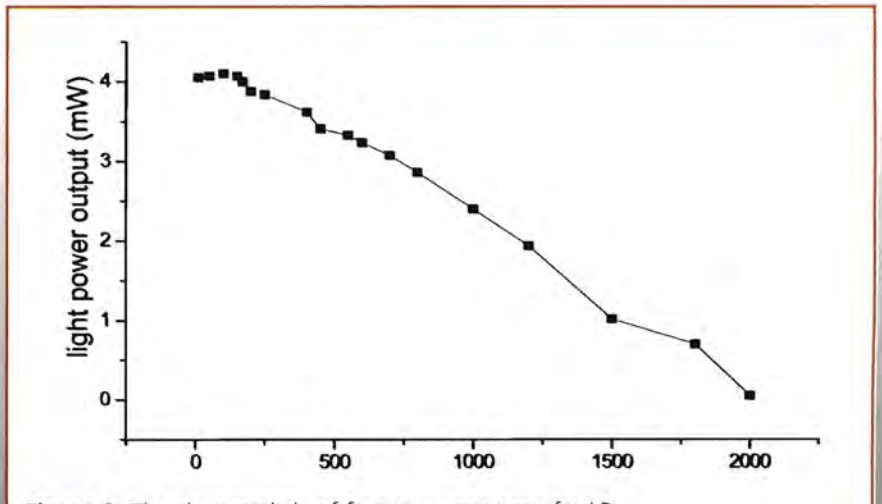

Figure 9: *The characteristic of frequency response for LD*

Letters

PLEASE EMAIL YOUR LETTERS TO:
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ELECTRONICS WORLD RESERVES THE RIGHT TO EDIT ALL CORRESPONDENCE

Looking for the right friend or foe

Thank you for a great magazine.

I have just been reading the book review on Military Avionics Systems, (March 2007, page 44), reviewed by Carl Holden. I couldn't help chuckling to myself at the suggestion that 'IFF' is short for 'Intercept Friend or Foe'.

Did this actually come out of the book, I wonder; a book written by somebody who spent "20 years in the Royal Air Force".

IFF actually stands for 'Identify Friend or Foe'. Rather a different concept – you'd have to agree.

For what it's worth, I will still be buying the book!

Simon Beer
Technical Director
Integrated Circles Ltd

It's in the language

Ian Moir and Allan Seabridge's book clearly states in the Glossary: IFF – Identification Friend or Foe (Simon you are vindicated!).

Some other external sources also give: IFF – Interrogation Friend or Foe.

There are references to the common heritage between military IFF and civilian aviation transponder equipment, which is primarily referred to as being used for aircraft "identification". Words or speech are used to communicate between two entities. Provided those entities have a common mode of expression and understanding – correct communication will occur – whatever the language.

In my professional life, I have used the abbreviation IFF without the realisation that my concept of the real words that make up the acronym may not be "common". It's enough to make me go and fiddle with my CRM-114.

Simon, thanks for the opportunity to become aware of other alternatives and share our views with other readers... and enjoy your book!

Carl Holden

Old philosophers and the Universe structure

Recently I received a book from my relative from India who is a Hindhuism researcher. It is a religious book, containing sutras written by a Hindhu saint named Maharishi Jaimini, who is believed to have lived around 4000 years before Christianity started.

I was attracted to the way he presented his sutras, which come accross as very scientific. As such, I thought that Electronics World readers might be interested to know about it.

One of the branches of Jaimini's philosophy discusses the structure of the Universe. According to his theories, the Universe is exact in structure as that of the atoms. One example is the solar system, in which the negatively charged elements (electrons) are moving around the positively charged elements (protons). The Sun is considered to be a 'proton' as it radiates positively-charged particles and the other planets around the Sun are seen as electrons, which are held by it.

This theory applies to Earth as well. Everything on Earth is made of atoms. But, if we break down further the atomic structure, it becomes nothing. So, the other messages that come from Jaimini are: "Everything that exists comes from nothing" and "Energies are neither created nor destroyed". Thirdly, the groups of atoms can be manipulated without losing the elements (protons/electrons). To break the links between them, they have to be 'forced' with some sort of energy; voltage, for example. Whichever electron splits away, it is classified as a movable particle (current) and the static/unmovable particles become an obstruction to the flow of movable particles. These are effectively the 'electric resistance'; hence, Jaimini reveals that "Nothing is an insulator when the force is infinite". As we know, the relationship of voltage, current and resistance are defined by Georg Simon Ohm as Ohm's Law, but it was explained only for Electrical Engineering purposes rather than as a universal analysis.

The same principle is applied to the magnetic field, as well as the optical field. But Jaimini did not write much about the magnetic field. However he did state

that the Universe has three major fields – electric, magnetic and luminous.

A simple natural phenomenon was defined by Jaimini as follows: The clouds are positively charged because they are pulled by Sun as vapour (X changes its characteristic when closed to something strong Y). When the clouds hit one another, this produces a lightning, which then travels to Earth to establish the shortest closed loop.

The Sun is designated as positive potential and the Earth (including the other planets) is designated as the negative potential. The medium of conduction is the atmosphere, which all fulfill the rules of electricity.

The beauty of Jaimini's work is actually defining the structure of the Universe and then compares it to that on Earth. What wonderful theories!

Adapted from "*Jaimini Philosophy, 4000 BC*".

Nachimani Charde
Malaysia

Fantastic plastic

In the February 2007 issue of Electronics World magazine, we run a Focus article discussing plastic electronics entitled 'Fantastic Plastic' (page 12). We omitted to mention that this article was written by Faiz Rahman.

Ed

The equipotential ground plane

In their article on Signal Integrity (EW April 2007, page 32), Kannan Srinivasagam and Jayasree Nayar make some good points on the design of printed circuit boards to minimise crosstalk. They identify the need to add resistors to the terminations of transmission lines to minimise reflections. They emphasise the fact that current flows in a closed loop. Traces must have a return path. That return path is the ground plane; "This is the path of least inductance and results in the smallest current loop possible".

However, they failed to take the all-important next step in their reasoning – to question the concept of the equipotential ground plane.

If it is accepted that the ground plane possesses the property of inductance, then it follows that a voltage must exist along it when a transient current flows in the transmission line. There will be a significant voltage between the reference terminal of the output driver and the reference terminal of the input receiver. If there is a voltage along the length of a conductor, it cannot possibly be equipotential.

This being so, it is vitally important that the return conductor be included in the circuit diagram.

By its very nature, **Figure 1** includes the assumption that each terminal represented by an earth symbol is at the same potential as the zero-volt terminal of the associated output driver.

When the functional diagram of Figure 1 is modified to include a return conductor, as shown in the interconnection diagram of **Figure 2**, the picture becomes much clearer.

Since it is accepted that the return conductor possesses inductance, it becomes possible to create a circuit model which includes inductors. Then it becomes possible to identify the inductance which couples the aggressor circuit with the victim circuit; and then it becomes possible to include capacitive coupling in the circuit model. **Figure 3** illustrates the result. Invoking electromagnetic theory to relate electrical properties to physical construction then allows parameter values to be assigned to all the components.

When values have been assigned to all the components of the circuit model, it becomes possible to utilise circuit theory to analyse the transient response of the system and predict the precise waveform and amplitude of the interference that exists between one signal and another.

When we are able to analyse the coupling in detail, it becomes possible to handle the problem of crosstalk as a matter of routine.

However, none of the above possibilities will become fact while we continue to hold on to the concept of the equipotential ground plane.

Ian Darney
UK

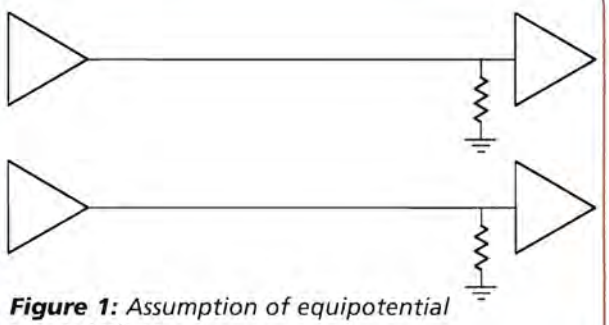


Figure 1: *Assumption of equipotential ground plane*

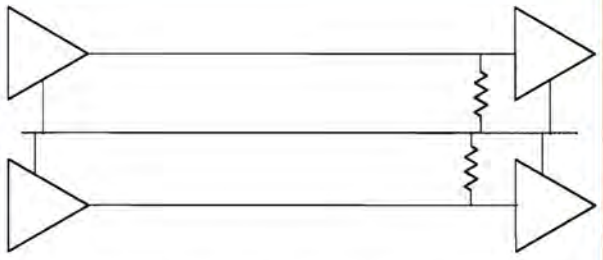


Figure 2: *Identification of return conductor*

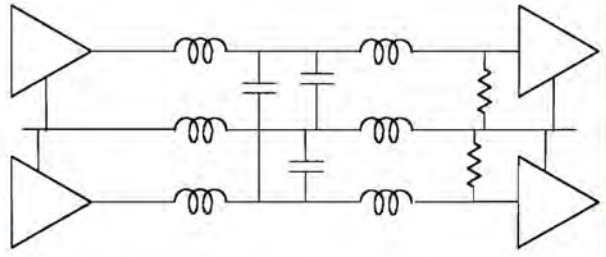


Figure 3: *Circuit model of cross-coupling*

Engineering Disasters – Lessons to be Learned

Don Lawson

Professional Engineering Publishing

In July 1983, an Air Canada Boeing 767 ran out of fuel during a scheduled flight from Ottawa to Edmonton. With both engines out and only limited hydraulic power available, the pilot still managed to glide the aircraft to a remote and long disused military airfield at Gimli where he made an emergency landing. Miraculously, nobody was killed or seriously injured and even the aircraft suffered relatively minor damage. However, had it not been for a combination of good fortune and the skill of the aircrew, the outcome of this incident, which was later nicknamed the 'Gimli Glider', might have been far more serious.

The reason the aircraft ran out of fuel stemmed from an intermittent malfunction of the onboard computer-controlled fuel quantity indication system (which was subsequently traced to a bad solder joint and an underlying system design fault). Because the system on this particular aircraft was known to be faulty, ground staff and air crew had followed a manual procedure to determine the amount of additional fuel required for the flight. Unfortunately, they made an arithmetic error in their calculations and, as a consequence, loaded insufficient fuel onto the aircraft. Meanwhile, the pilot mistakenly believed it was still permissible to fly the aircraft, even though he had noticed that the fuel gauges in the cockpit were quite obviously blank.

However, it would be wrong to suppose that the only factors which led to the incident were an equipment malfunction and human error. The official enquiry that followed found a number of other, less immediately obvious, contributory factors including organisational weaknesses, an underdeveloped safety culture, unclear maintenance documentation, a limited stock of spare parts and deficiencies in staff training.

THE OFFICIAL ENQUIRY THAT FOLLOWED FOUND OTHER CONTRIBUTORY FACTORS, INCLUDING ORGANISATIONAL WEAKNESSES, AN UNDERDEVELOPED SAFETY CULTURE, UNCLEAR MAINTENANCE DOCUMENTATION, A LIMITED STOCK OF SPARE PARTS AND DEFICIENCIES IN STAFF TRAINING

This incident is an example of what Don Lawson describes as an 'engineering failure' in the sense that something or someone did not perform as expected. However, had the outcome led to catastrophic and tragic consequences then he would have used the more emotive term 'engineering disaster'.

In the first and major part of his book Lawson describes a series of incidents – most of which are well known and related mainly to aeronautical, civil or mechanical engineering – to illustrate his premise that the study of past failures can teach engineers valuable lessons, on the basis that it is always cheaper and less painful to learn from the mistakes of others. Few engineers, especially those working in electronics, are likely to disagree with this sentiment given that learning from failures is very much a hallmark of the profession.

However, learning anything of value from a failure requires a clear understanding of what caused it and there are two difficulties in achieving this. The first is that most failures are actually caused by a combination of interconnected factors, some of which are not always immediately obvious. For example, in the Gimli Glider incident it was organisational factors rather than simply an equipment malfunction and human error that led to the failure. Indeed, what might loosely be termed 'organisational' and 'management' shortcomings feature prominently in virtually all the failures Lawson describes.

The second difficulty is that the investigations and enquires, official or otherwise, which inevitably follow in the wake of failures, sometimes draw conflicting or erroneous conclusions as to their respective causes. For instance, two separate investigations were held after the Zeppelin disaster of 1937 when the German airship Hindenburg, while on a scheduled flight from Frankfurt, burst into flames on landing in New Jersey during a thunderstorm, with the loss of 36 lives. The first investigation, conducted by the US Chamber of Commerce, concluded that the conflagration was started when hydrogen leaking from the airship was ignited by a spark. However, the second investigation, undertaken by the Germans, denied there had been a hydrogen leak and postulated instead that St Elmo's fire (an electrostatic discharge) had ignited flammable dope on the surface of the airship's fabric covering. It was not until the 1990s that the discrepancy was finally resolved, at least to the satisfaction of most commentators, when independent investigators revisited the evidence and with the aid of various laboratory tests found in favour of the German explanation.

Lawson has drawn on a wide variety of sources in the course of his research, which no doubt has helped overcome both these difficulties. Quite sensibly, he has chosen to present each failure in a consistent way beginning with a description of the failure itself, followed by his own comments and concluding with a summary of what he believes can be learned from it. The last are particularly useful in that they offer practical advice as to what should be done to avoid repeating similar mistakes.

Unfortunately, the same cannot always be said of either the descriptions or his comments, both of which tend to be overburdened with superfluous detail. For example, in his analysis of UK railway accidents, which include the 1997 collision at Southall and the express train derailment of 2000 in Hatfield, Lawson begins with a rather overlong history of the rail network and, at one point, takes a highly technical detour to explain the mechanical properties of the wheel-rail interface.

Even worse in this respect are his descriptions of the Space Shuttle Challenger and Columbia accidents, which between them extend to more than fifty pages. The problem is not that his elaborations and technical detours are uninteresting, it is just that, in most instances, abridged versions would have been sufficient.

In fairness to Lawson, this is not true of all the examples he covers. For instance, he presents a succinct account of the Gimli Glider incident, mentioned earlier, and a reasonably concise treatment of a selection of bridge failures, such as the Tay railway bridge disaster of 1879 and the Tacoma Narrows suspension bridge which was shaken apart by the wind in 1940.

However, it has to be said that this part of the book, which runs to some 270 pages, is a little fatiguing to read. Lawson mentions in the introduction that, by writing less about each failure, he could have included more examples but decided against doing so because he felt more detail was needed to "draw out the lessons". Then again, it is not entirely inconceivable that a failure in editing might have influenced that decision. On balance, including more examples would have been preferable as would drawing on failures from a broader range of industries, such as information technology and defence.

In contrast to the first part of his book, the second is essentially a self-contained collection of essays on various topics related to engineering failures. In one, entitled '*Words of Wisdom*', Lawson sketches the thoughts of several notable engineers including Sir Alfred Pugsley, Trevor Kletz and Hyman Rickover on why failures occur and how to avoid them. Another essay includes a cogent summary of high reliability theory and useful insights into risk analysis, decision making and human error.

Lastly, under the title '*What does it feel like to be associated with a disaster?*' Lawson reproduces an extract from a poignant article written in 2002 by Leslie Robertson, who was the lead structural engineer for the World Trade Centre in New York, reflecting on his own experiences.

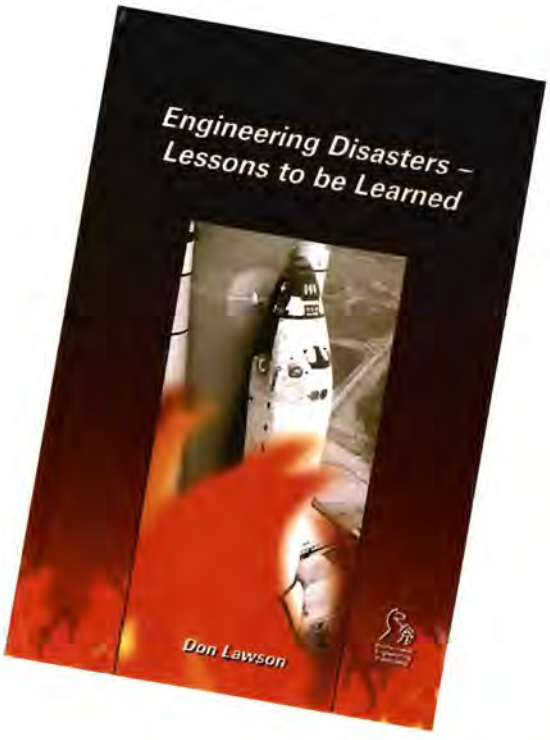
The third and last part of the book, in which Lawson presents his conclusions and final comments, is perhaps the most interesting. In particular, he argues that the majority of engineering failures follow a distinct pattern and identifies a number of common casual factors such as technical, human error, lack of robustness, failure of foresight, time and cost pressures.

To support his argument, Lawson lists the failures previously described in the first part of the book and indicates which factors were involved in each. Whilst the result looks slightly contrived and cannot be considered as conclusive, given the relatively small number of failures he covered, it is nevertheless fairly convincing. Lawson's overall conclusion is that the best way to minimise the risk of failure is through sheer human effort and by striving to attain high reliability in both the technical and organisational spheres. Engineers, he says, should at all times maintain the highest professional and ethical standards and never tolerate sub-standard performance in design, operations or management.

ENGINEERS, HE SAYS, SHOULD AT ALL TIMES MAINTAIN THE HIGHEST PROFESSIONAL AND ETHICAL STANDARDS AND NEVER TOLERATE SUB-STANDARD PERFORMANCE IN DESIGN, OPERATIONS OR MANAGEMENT

This is not a book about electronics and the emphasis on machines, metal and concrete may not appeal to you. Nevertheless, it does offer many useful insights which are pertinent to most engineering disciplines including electronics. Therefore, borrow a copy of the book and read the last part first and then, if your interest is aroused, peruse the two earlier parts.

Douglas Taylor



RoHS

Living with RoHS – the big questions

Now that RoHS is law, there are more questions than ever about how to cope with it. Recent research showed that the UK wasn't prepared for the deadline. Only 12% of design engineers, buyers and MRO engineers were fully compliant in readiness, ahead of RoHS officially coming into force. Whilst 37% of respondents revealed that they were "close to becoming compliant", a further 28% confessed that they had only just "started to become compliant".

There's still clearly a lot that needs to be done by the design engineering community, but the main thing for engineers to realise is that they aren't alone in their quest to become compliant. Wide ranges of support services exist to help people along the way, such as those on offer at www.rohs.info. The fact that the deadline has passed means that it is even more important to access the help that exists.

The research – which was conducted amongst 263 UK design engineers, buyers and MRO engineers – shows that distributors are playing a vital role in ensuring compliance is achieved. Around 46% of those surveyed had chosen to approach a distributor for reliable RoHS support, followed by 22% who preferred to directly approach the manufacturer. Interestingly, only 9% have been relying on the government for RoHS support.

By its nature, online support is the fastest way to find out about the latest RoHS complaint products. Signing up to automatic email notification or online 'Bill of Materials' conversion services are effective ways to get new part numbers for old non-compliant components and upgrade to the latest RoHS offerings. But being able to speak to experts is also proving key for engineers who have achieved compliance.

Whilst 53% of respondents from the research considered online technical help and support services to be either "extremely" or "very" important, 39% also considered telephone technical help and support services to be "extremely/very important". There are still many grey areas around the new legislation that people are unsure about – exemptions and due diligence are just two of the 'hot potatoes'. Being able to access expert opinion over the coming months on these issues will be hugely important as the real effects of RoHS start to take place.

There are still many questions that need answering about the scope of the legislation and it will be essential to keep on top of the products that are under review for exemption. A recent example of this is semiconductor evaluation boards. Distributors and manufacturers alike believed these to be out of scope but the National Weights and Measures Laboratory, the body responsible for policing RoHS, has decided they're in.

It often isn't clear if a product is within the scope of RoHS or not. The situation for many types of industrial product will depend on how they are used. Equipment that is not dependent on electricity is also excluded such as gas boilers and petrol lawnmowers.

Q: My products are EU-RoHS compliant, so will they comply with China-RoHS?

A: To be compliant with China-RoHS all EIPs must be marked. At present no substance restrictions apply but, if RoHS substances are present this must be indicated by the markings. One difference between EU and China-RoHS is that China-RoHS marketing requirements do not have exemptions; the substance is either present or not. A product can be EU-RoHS compliant by exemption, which allows the RoHS substances to be present at levels above the MCV.

Q: How do I label the packaging?

A: The China-RoHS legislation states that a label with the "codes" for the main packaging materials will be compulsory for EIPs. The packaging of EIPs must be marked to indicate which materials are used. Material codes from Chinese Standard GB 18455-2001 that indicate which materials are present, must be applied by printing on, or applying a label to, the outside of the packaging.

Q: How do I produce the table of hazardous substances and what format should be used?

A: The first step is to determine which RoHS substances are present in each of the main parts of the equipment. Some will be known but for most it is best to ask the supplier. Remember, there are no exemptions so it is possible EU-RoHS compliant products may contain China-RoHS substances above the MCV.

Then create a table, in Chinese, clearly indicating which part of the equipment, such as the PCB, enclosure etc, contain hazardous substances. This is very black and white, an "X" for included or "O" if none are present above the MCV. The table must also include a definition of the symbols.

Q: How do I determine the environmentally friendly use period (EFUP)?

A: A draft standard has been published which describes several options for determining the EFUP. These include: by an experimental method, from the safe-use period if known, from the "technical life" or based on the EFUP of similar products. Currently, the last of these appears to be the most useful and the draft standard gives a few examples such as a mobile phone (five years), colour television (seven years) etc. It is likely that the final version will include a much longer list. The numbering system is 1, 2, 3, 4, 5 years then 10, 15, 20, 25 and so on (rounded to the nearest five, so the TV at seven years will be rounded to five).

Q: How will China-RoHS affect the design of products?

A: China-RoHS legislation will introduce compulsory design standards for EIPs. It is believed that this measure could adopt some of the principals of the EU Eco-design approach. The Chinese government will also introduce compulsory standards to define the recyclability of products. No drafts are available as yet, but it is expected that toxic and hazardous materials should be avoided and only materials that can be recycled should be used.

Q: How do I find out if a component contains a RoHS substance?

A: The easiest method is to ask the supplier. If you are told that the part is EU-RoHS compliant, beware, as this does not necessarily mean that there are no RoHS substances present, if the part is used in exempt forms. It is increasingly important for electrical equipment manufacturers to know where hazardous substances are used.

Gary Nevison is chairman of the AFDEC RoHS team, board director at Electronics Yorkshire and head of product market strategy at Farnell InOne. As such he is our industry expert who will try and answer any questions that you might have relating to the issues of RoHS and WEEE. Your questions will be published together with Gary's answers in the following issues of Electronics World. Please email your questions to svetlana.josifovska@stjohnpatrick.com, marking them as RoHS or WEEE.

Linear Capacitance-to-Time Converter Using -R

It is interesting to note that while capacitors are often used in timing circuits, it is a rarity to find linear capacitance-to-time converters. We found this circuit useful in measuring the values of many electrolytics lying around in the lab; an application which does not necessitate absolute accuracy.

To better understand how the capacitance meter works, let us first refer to the circuit in **Figure 1**. By nodal analysis:

$$(V_1 - V_2)/R_1 = V_2/R_2 + CdV_2/dt \qquad (1)$$

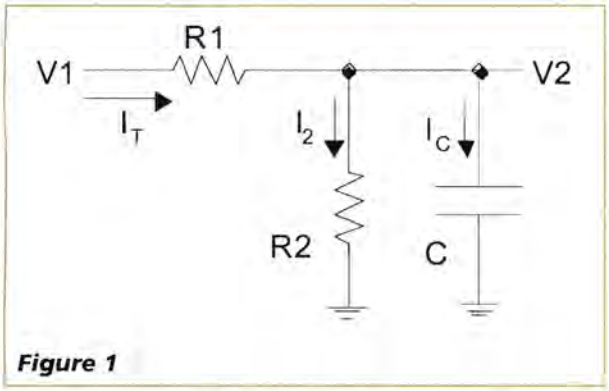


Figure 1

If we let R = R1 = –R2, **Equation 1** simplifies to:

$$dV_2/dt = V_1/RC \qquad (2)$$

This means that instead of the exponential rate of change of the capacitor voltage (V2), it increments linearly according to the values of V1, R and C. This idea is employed in the circuit of **Figure 2** where V1 is the buffered output of U1a. U1b along with R2, R3 and R4 combine to form a negative resistor whose magnitude is equal to R1. Cx is the unknown capacitance. Lastly, U2 is a comparator whose threshold voltage (VT) is set by R5 and R6.

The operation is fairly simple. While the toggle switch is at position B, the Cx is discharged and the LED is on. Flicking the switch to position A, the LED turns off and the voltage across Cx linearly rises according to **Equation 2**. At a certain point, when its voltage (V2) exceeds VT, the LED turns on again. The length of time that the LED was off is numerically equal to the unknown capacitance, Cx.

For the given component values, the circuit is useful in measuring capacitances between 1-100μF. With its VT at 1V, it is found that the voltage across Cx rises at a rate of (1/Cx)V/s. As such, a 1μF capacitor causes the LED to light up 1s after switch is toggled to position A. Similarly, a 100μF cap will take 100s for it to make the LED light. Hence, the capacitor value (in μF) is easily measured by using a stopwatch.

The graph of **Figure 3** shows a test run of 51 capacitance values from 1-100μF. This typical result shows a fairly close match between rated values and their measured counterparts.

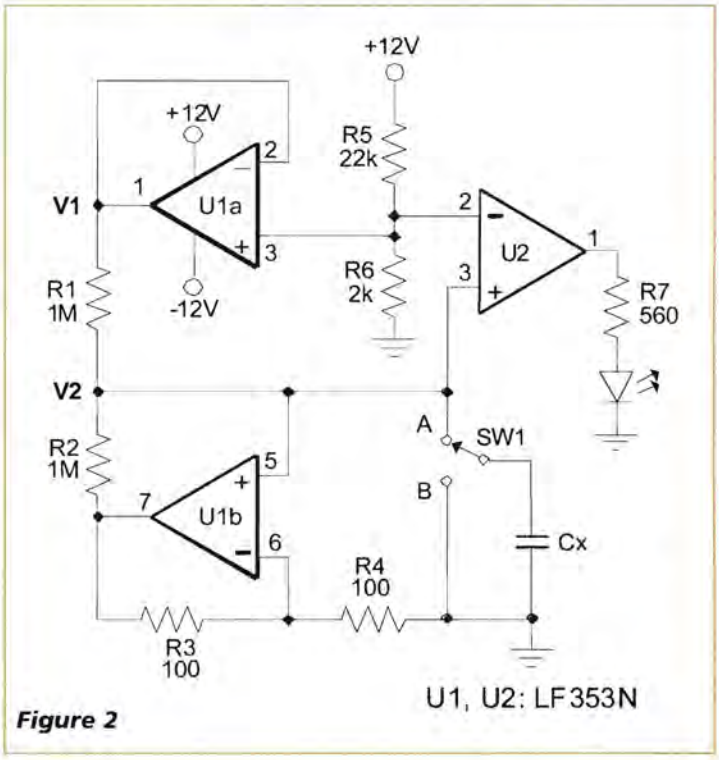


Figure 2

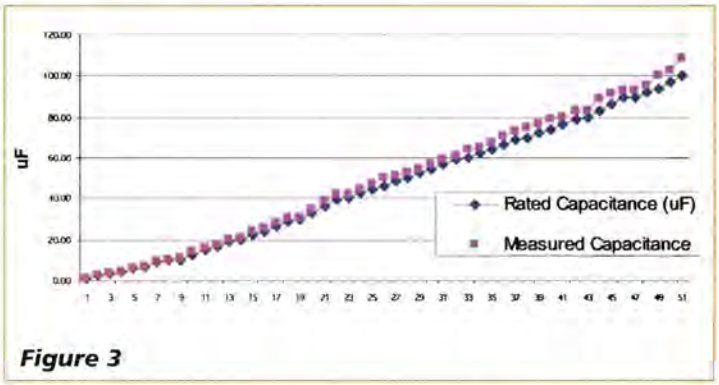


Figure 3

Arthur E. Edang *and* ***Alexander Lawrence C. Gan***
Don Bosco Technical College
Philippines

Precision Anti-RIAA

To test the reproduction of the RIAA transfer (amplitude and phase) of any kind of MM or MC phono pre-amp, you need a measuring system that creates the inverse RIAA transfer [e(f)] with high precision: an anti-RIAA encoder with a deviation of less than ±0.1dB relative to the exact transfer. The output of this encoder has to be connected to the input of the RIAA transfer [r(f)] equalised phono-amp under test. The encoder's input is fed by a constant-amplitude sine wave sweep from 20Hz to 20kHz.

In the best case, the output of the phono-amp will show a flat frequency response like [o(f)] at 0dB in **Figure 1** as well as a flat phase response.

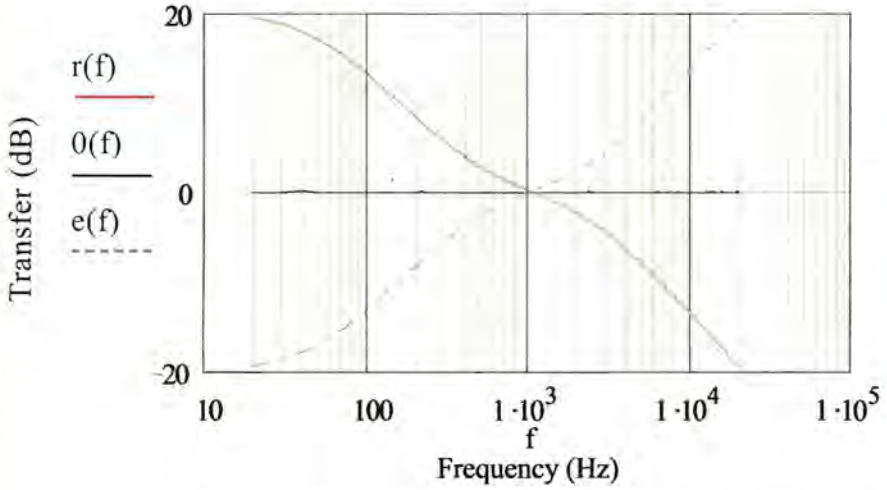


Figure 1: *Transfers: encoder output [e(f)], phono-amp transfer [r(f)] and output [o(f)]*

Passive solutions are not that precise, especially in conjunction with MC pre-amps and their rather low input impedances. The most simple and most precise approach can be designed with the active configuration of **Figure 2**. The inverse RIAA transfer describing formulae are based on RIAA's transfer time constants T1 = 3180µs, T2 = 75µs, T3 = 318µs. In the chosen four-component network Zin(f) that consists of two resistors and two capacitors, the respective formulae look as follows:

T1 = R1*C1, T2 = R2*C2, T3 = (C1+C2)*(R1 || R2), R1 = b*R2, b = 11.$\overline{7}$ (repetend) C1 = a*C2, a = 3.6, Gain G(f) = –|Zin(f)/Rf| = –(in/out) (with components of **Figure 3**: –26dB at 1kHz).

The detailed circuit diagram of the RIAA encoder is shown in Figure 3. This instrument is capable to drive MM-phono amps with input sensitivity of approximately 5mVrms as well as – via a TI power buffer BUF634 – MC-phono amps with input sensitivity of approximately 0.5mVrms and a minimum input impedance of ≥ 50R. The buffer should be wired in narrow bandwidth mode. The power lines must be carefully bypassed with 100n polypropylene and 10µ tantalium capacitors positioned as near as possible to all op-amps (see data sheets). R4 and C3 ensure stable conditions for the capacitor loaded output of OP1. All resistors (E24-E96 metal) and capacitors (E12 polypropylene) should have tolerances ≤ 1%. OP4 keeps the output free of dc-offset. For direct-coupled pre-amps only (= no capacitor inside the signal path) with the components indicated only P1 has to be adjusted: after a warming-up period of approximately 15 minutes trim P1 to 0.00mVdc output voltage. Power supply can be generated with 7815/7915 voltage regulators. Calculated values for Zin(f) and Rf are: R1 = 883k$\overline{3}$, R2 = 75k0, C1 = 3n6, C2 = 1n0, Rf = R7 = 4k841

In a frequency band of 20Hz-20kHz the comparison of the built-up instrument with the exact inverse RIAA transfer ended up with a maximum deviation of less than ±0.1dB from the exact transfer. In the same frequency band the calculated maximum deviation is ±0.1018dB between 460Hz and 485Hz. It is most unlikely to hit this special combination of R1, R2, C1, C2 tolerances. In nearly all cases one will end up with deviations somewhere between ±0.1dB. While

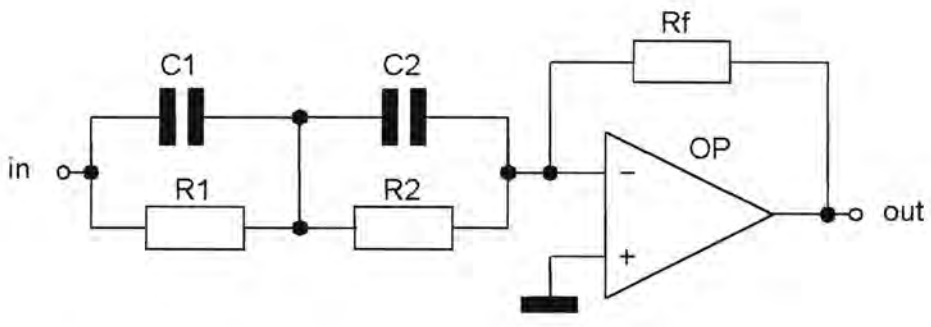


Figure 2: *Active inverse RIAA transfer*

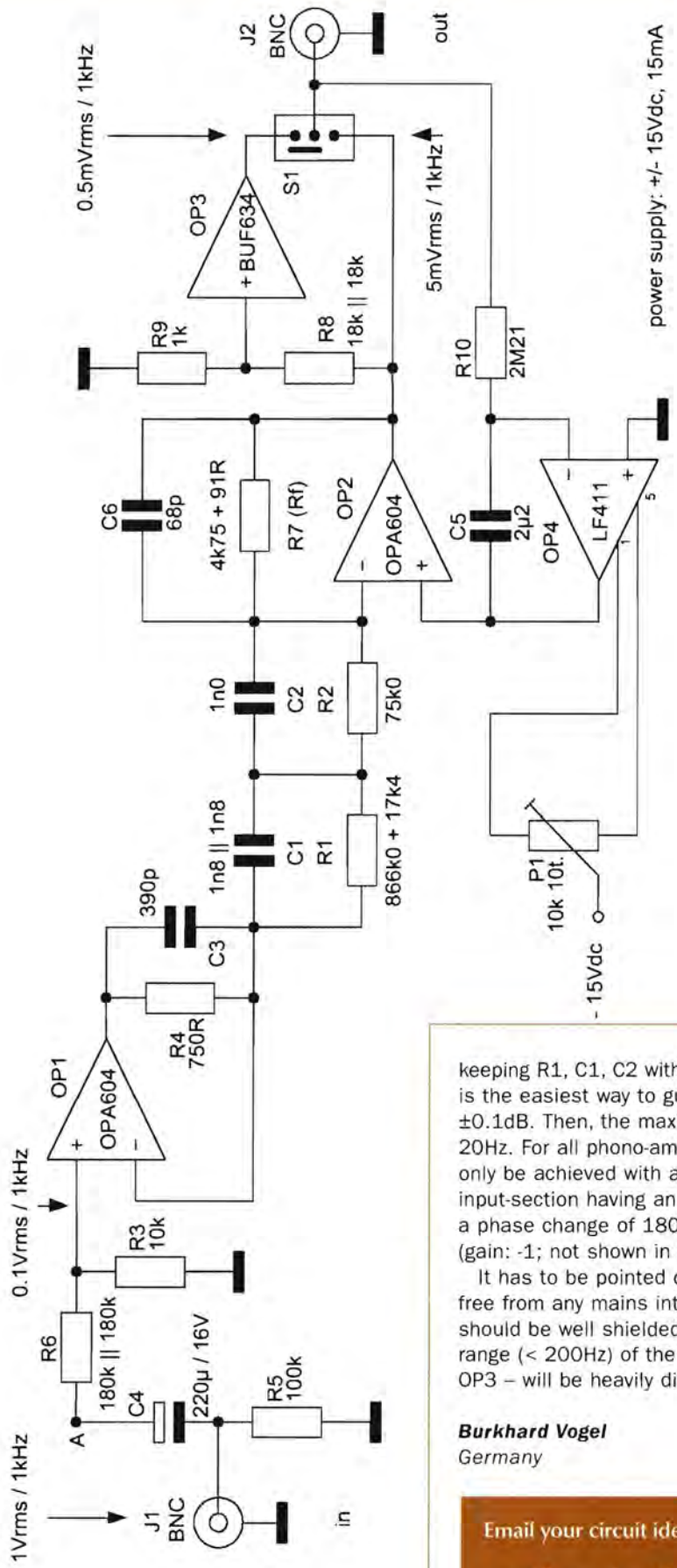


Figure 3: *Precision anti-RIAA*

keeping R1, C1, C2 within 1% to find R2 with tolerance of ≤ 0.1% is the easiest way to guarantee a deviation of less than ±0.1dB. Then, the maximum deviation will be ±0.076dB at 20Hz. For all phono-amps, a flat phase response of ±0.5° can only be achieved with a capacitor-free or capacitor-coupled input-section having an hp-corner-frequency ≤ 0.01Hz. To avoid a phase change of 180° between input and output an inverter (gain: -1; not shown in Figure 3) should be inserted at point A.

It has to be pointed out that the power supply must be kept free from any mains interferences and the whole instrument should be well shielded too. Otherwise, the lower frequency range (< 200Hz) of the transfer – especially at the output of OP3 – will be heavily disturbed.

Burkhard Vogel
Germany

Email your circuit ideas to:

svetlana.josifovska@stjohnpatrick.com

The Future begins -

By Chris Williams, UKDL

Sometime in the future we are likely to say that Plastic Electronics in the UK was established in April 2007 when (subject to last minute Governmental glitches!) the Department of Trade and Industry launched a call for "projects that demonstrate the integration of different functions onto a common flexible substrate" to be submitted to the April '07 competition of the Technology Programme.

For the first time, companies and universities are being encouraged to work together to submit project proposals for product demonstrators that show what might be accomplished using the all-embracing concept of Plastic Electronics.

Projects will be invited for submission to the competition that could have several or all of the following attributes:

- Printed photovoltaic and voltaic circuitry to demonstrate self-powered designs that can recharge themselves in available light;
- Printed circuitry to allow contactless power transfer from an external electrical power source to the flexible substrate;
- Printed sensor circuitry to offer gas, liquid, temperature, humidity or other sensing functions that integrate into the rest of the system;
- Printed organic electronic transistors (to perform telemetry, data storage and/or data manipulation functions and other electrical circuit functions such as active matrix backplane drivers);
- Printed electro-optic effects to deliver display functions or light modulation/ light emission functions;
- Integration of "rigid" components into a printed electronic device. This could include integrating conventional silicon IC chips onto a flexible substrate using printed wiring techniques.

Each of the above topics is generally available around the UK in 'proof of principle' demonstrator form, but no-one has yet succeeded in developing a demonstrator that can integrate several functions onto a single flexible substrate. That is the key focus of the April competition – to show what can be done and then we can unleash the minds of designers from all industries to determine what should be done.

The value of this competition will be incalculable. Proving by demonstration that complete electrical devices and systems can be created by additive printing onto a common flexible substrate will underpin the emerging Plastic Electronics industry and encourage many new players to engage with this fascinating technology. The materials that are used for organic photovoltaics, organic transistors and organic light emitting materials can be very similar in nature, but it remains to be shown that they can be deposited together to make a sophisticated electrical device.

Think of the applications that might be addressed if we can easily integrate electrical circuitry of different functions onto plastic or paper substrates:

- "Smart packaging" that can monitor the environment and actual physical condition of their contents and feed back this information using telemetry, or by optical display, the actual status of those contents.
- "Smart medical sensors" that detect health status, but are printed on wholly disposable substrates. These can be printed on site in a pharmacy, which will also help reduce stock levels of multiple devices that are needed, as well as reduce delivery time to the time needed, for a printer to warm up and accept the data request from the computer that ordered the sensors.
- Electronic product packaging that "tells" you about the contents before you purchase.
- "Self-powered" electronic newspapers/magazines, books etc. Instead of buying tonnes of paper per year in the form of "added value" printed matter, we will buy a small number of flexible electronic display devices that have on-board Wi-Fi through which we can download whichever newspaper/magazine information we have subscribed to.
- "Self-powered" paper-based electrical devices – how about restaurant menus that allow you to choose the language you read the information in?

The list is limited only by imagination and the inevitable restrictions placed on the technology in its early years. Winston Churchill preached that we should "Study history! Study history!". His comments are valid today in the new world of Plastic Electronics. The first volume produced products that can be easily manufactured by "non-specialist" manufacturers (by which I mean manufacturers who haven't invested £100s of millions into production equipment and technology know-how) will be based on very simple circuits. If we go back to the early days of the transistor, we can find very many examples of functional electronic circuits that were assembled using small numbers of discrete components and which performed to an extent that was

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"good enough" for the purpose.

The invention of the integrated circuit and subsequently the microprocessor, and then the embedded PC, has diluted the circuit design skills of the average electronics engineer. Most system designs today are based around standard 'chip sets' put together and controlled by software to achieve their final functionality. Much of this development will be unavailable to the new pioneers of Plastic Electronic devices and products since the current 'state of the art' in printed transistor topography does not allow the same transistor size, packing density or device performance as conventional solid state silicon.

The prize of market success will go the engineers who revisit old ideas of simple design and low component count and then configure these using printed functional inks.

Dig out those old lab books buried in the attic and see what you could do with today's emerging technologies. The early adopter market profits will go to the inventors who implement in practice, build and then sell the products based on the ideas from old texts that might have titles such as "a thousand circuits or more that a designer can build with 100 transistors or less".

Chris Williams is Network Director at UK Displays & Lighting KTN (Knowledge Transfer Network)

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Agilent (HP) 53131A Frequency Counter	£750	Various other calibrators in stock. Call for stock / prices	

Power Managed Family Featuring nanoWatt Technology

Microchip continues to provide innovative products that are smaller, faster, easier to use and more reliable. The Flash-based PICmicro microcontrollers (MCU) are used in a wide range of everyday products, from smoke detectors, hospital ID tags and pet containment systems, to industrial, automotive and medical products.

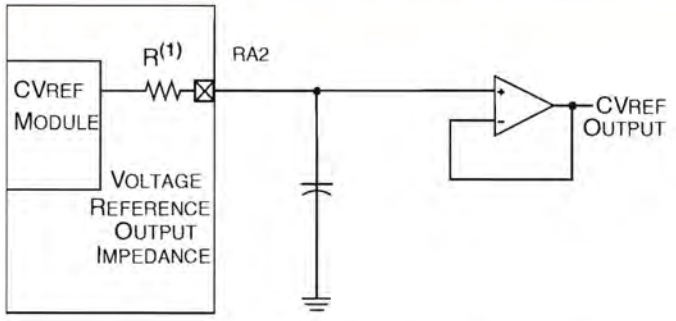
The PIC16F/18F power managed family featuring nanoWatt Technology merge all of the advantages of the PICmicro MCU architecture and the flexibility of Flash program memory with several new power management features. The devices become a logical solution for intelligent small systems, or complex systems that require extended battery life and energy-efficient operation.

The flexibility of Flash and an excellent development tool suite, including a low cost In-Circuit Debugger, In-Circuit Serial Programming and MPLAB ICE 2000 emulation, make these devices ideal for just about any embedded control application.

The following series of Tips 'n' Tricks can be applied to a variety of applications to help make the most of the PIC16F/18F power managed family featuring nanoWatt Technology.

TiP 1: HOW TO USE A COMPARATOR REFERENCE AS A D/A

The voltage reference module normally used to set a reference for the comparators may be used as a simple D/A output with limited drive capability on pin RA2. Set the CVROE bit (CVRCON<6>) and configure the pin as an analogue input. Due to the limited current drive capability, an external buffer must be used on the voltage reference output for external connections to VREF.



Note 1: R is dependent upon the Voltage Reference Configuration CVRCON<3:0> and CVRCON<5>.

TiP 2: HOW TO DETECT A LOSS OF CRYSTAL/RESONATOR OSCILLATOR

The fail-safe clock monitor feature can be used to detect the loss of a crystal/resonator oscillator or other external clock source. When loss is detected, an internal clock source will provide system clocks, allowing for either a graceful shutdown or a "limp-along" mode if shutdown is not needed.

Just set the FCMEN bit in the configuration word (CONFIG1H<6>). A higher "limp-along" speed can be selected by setting some of the IRCF bits (OSCCON<6:4>) before or after the loss occurs.

TiP 3: ENABLING IDLE MODES

The PIC18F nanoWatt family of devices features multiple IDLE modes that can be used to reduce overall power consumption. By setting the IDLE bit (OSCCON<7>) and executing a SLEEP instruction, you can turn off the CPU and allow the peripherals to keep running. In these states, power consumption can be reduced by as much as 96%.

TiP 4: HOW TO ELIMINATE AN EXTERNAL CRYSTAL, RESONATOR, OR RC TIMING NETWORK

If a precision frequency clock is not required, use the internal clock source. It has better frequency stability than external RC oscillators and does away with the external crystal, resonator or RC timing network.

The internal clock source can also generate one of several frequencies for use by the controller, allowing for reducing current demand by reducing the system frequency. When higher speed is required, it can be selected as needed under program control.

TiP 5: CLOCK SWITCHING PIC16F DUAL CLOCK

The PIC16F62X family of devices is equipped with a second low speed internal oscillator. This oscillator is available when the configured clock source is one of internal RC (INTRC), External RC* (EXTRC) or External Resistor** (ER) modes. The internal oscillator can be used to operate the microcontroller at low speeds for reduced power consumption. The actual speed of this oscillator is not calibrated, so expect 20-40% variability in the oscillator frequency.

To change oscillators, simply toggle bit 3 (OSCF) in the PCON register. When OSCF is clear, the low speed oscillator is used. When OSCF is set, the oscillator selected by the CONFIG bits is used.

* EXTRC mode only available on A parts

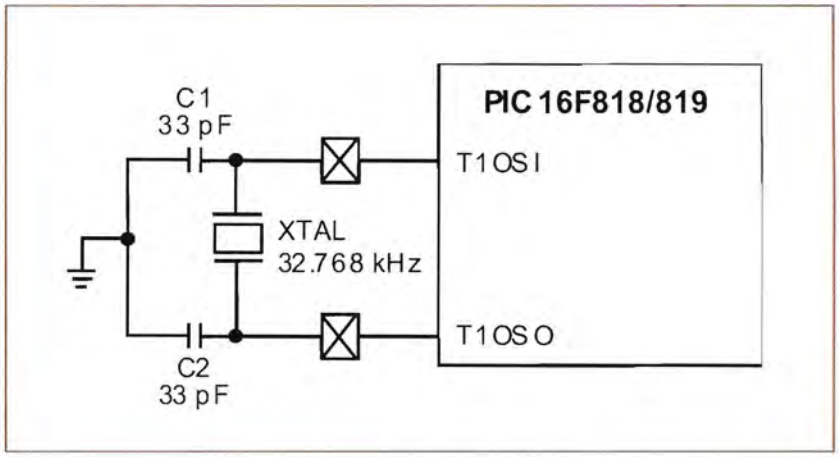
** ER mode only available on the non-A parts

Newer devices have a multi-speed internal clock. They can switch from 8MHz down to 31kHz in eight steps. The speed is selected using the OSCCON register.

TiP 6: CALIBRATION

An internal RC oscillator calibrated from the factory may require further calibration as the temperature or VDD change. Timer1 can be used to calibrate the internal oscillator by connecting a 32.768kHz clock crystal. Refer to AN244, "*Internal RC Oscillator Calibration*" for the complete application details.

The calibration is based on the measured frequency of the internal RC oscillator. For example, if the frequency selected is 4MHz, we know that the instruction time is 1µs (FOSC/4) and Timer1 has a period of 30.5µs (1/32.768 kHz). This means within one Timer1 period, the core can execute 30.5 instructions. If the Timer1 registers TMR1H:TMR1L are pre-loaded with a known value, we can calculate the number of instructions that will be executed upon a Timer1 overflow.



This calculated number is then compared against the number of instructions executed by the core. With the result, we can determine if re-calibration is necessary, and if the frequency must be increased or decreased. Tuning uses the OSCTUNE register, which has a ±12% tuning range in 0.8% steps.

Congratulations to Nick King of MBDA, Herts, England – WINNER of the Microchip 16-bit Explorer Development Board

CG635 Now Available From TTi

The Stanford Research Systems CG635, now available in the UK from TTi (Thurlby Thandar Instruments), is a low-jitter clock generator which can provide a wide range of clean, precise clocks for the most critical timing requirements.

The instrument generates extremely stable square-wave clocks between 1μHz and 2.05GHz. Its high frequency resolution, low jitter, fast transition times and flexible output levels make it ideal for use in the development and testing of virtually any digital component, system or network.

The CG635 has several clock outputs. The front-panel Q and -Q outputs provide complementary square waves at standard logic levels (ECL, PECL, LVDS or +7dBm). The square-wave amplitude may also be set from 0.2–1V, with an offset between –2V and +5V. These outputs operate from DC to 2.05GHz, have transition times of 80ps and a source impedance of 50Ω, and are intended to drive 50Ω loads. Output levels double when these outputs are unterminated.

The output may also be set to any amplitude from 0.5–6V. The CMOS output has transition times of less than 1ns and operates at up to 250MHz.

It has 50Ω source impedance and is intended to drive high impedance loads at the end of any length of 50Ω coax cable.

www.tti.co.uk

Minisens ASIC Transducer

LEM's Minisens is a miniature, integrated circuit transducer for AC and DC isolated current measurement up to 100kHz. This new component offers full isolation (no optocouplers required) and high sensitivity (from 20mV to 200mV per Amp of primary current) with no insertion losses. It is mounted directly onto a printed circuit board (PCB) as an SMD device, reducing manufacturing cost.

Minisens integrates, within one mixed signal ASIC, Hall-effect sensors with a magnetic concentrator to allow direct current measurement, without the need for an additional magnetic core. The non-contact measurement enables an almost unlimited current level as it eliminates the need for current to flow through the device. The only limiting factor is the thermal capacities of the primary conductor. The current can be carried either by a track (or tracks) located on a PCB underneath the Minisens, or by a cable or bus bar under or above the IC. The unlimited design possibilities for the primary conductor allow current measurement up to 70A or even higher.

Many parameters of the ASIC can be configured by on-chip non-volatile memory, including adjustment of the transducer's gain, offset, polarity, temperature drift and gain algorithm (proportional to, or independent of VDD). Two outputs are available: one filtered, to limit the noise bandwidth; and one unfiltered, which has a response time of less than 3μs.

www.lem.com

Single-Channel Video Filter/Driver

Fairchild Semiconductor now offers a 4th order, single-channel filter/driver with an 8kV ESD rating and SC70 package option – the FMS6141. This device's active filtering approach improves system reliability and image quality compared to passive solutions, and also lowers component count by approximately 20% to help reduce test time, design time and inventory costs. The FMS6141 is ideal for applications that require single-channel video filtering and driving such as portable DVD players and printers for digital still cameras.

Key benefits of the FMS6141 include image quality – as a 4th order video filter/driver the FMS6141 replaces 2nd or 3rd order passive devices typically used in digital consumer applications; versatility – with an 8MHz cut-off frequency and 48dB of stopband attenuation, the FMS6141 meets standard definition (SD) video requirements and is flexible enough for use as an anti-aliasing or reconstruction video-out filter/driver; and space saving – the FMS6141's high level of integration and tiny SC70 package option reduce board space compared to typical solutions. By driving either AC or DC-coupled single (150Ω) or dual (75Ω) coaxial cable loads it eliminates the need for expensive output coupling capacitors.

In addition, the device offers reliability by providing built-in 8kV ESD protection the FMS6141 increases reliability while lowering component count, compared to discrete designs that require external ESD-protection diodes.

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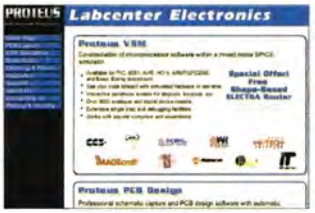

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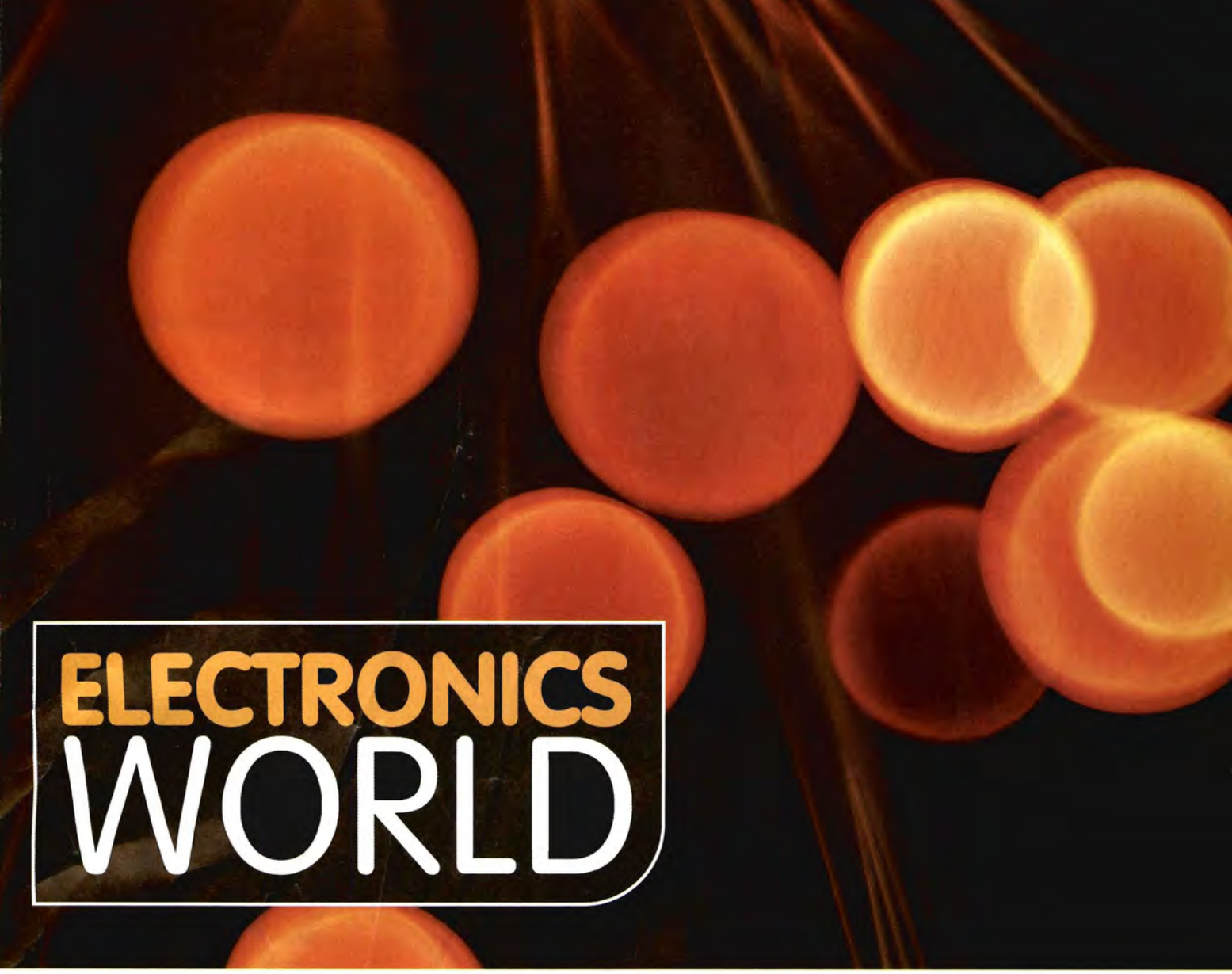

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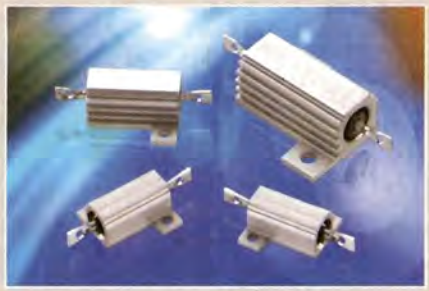
Power Resistors Based on HS Series

Recently added to Tyco Electronics's CGS range of power resistors are the new aluminium housed THS series power resistors, which are based on the high performance HS series devices, featuring same basic performance levels but at lower costs.

Encapsulated in silver aluminium housing, THS series power resistors are extremely stable, high quality wire wound resistors capable of dissipating high power in a limited space with relatively low surface temperature. Power is rapidly dissipated as heat through the aluminium housing to a specified heatsink.

Designed for heatsink mounting, latest THS series components are available with power ratings from 10W up to 50W and with ohmic values ranging from 0.01Ω up to 50kΩ. THS devices are able to withstand pulse energies of up to 320J and overloads of up to 25 times rated power.



Terminations are solderable tags but they can be modified to feature cable, threaded or fast-on connections. Standard inductances are kept to a maximum of 50ppm. Low inductance versions are available by using Ayrton Perry windings.

Target applications are vehicle braking and balancing resistors, capacitor charging and discharging, crowbar, filters and general electrical machinery.

www.tycoelectronics.com

High-Performance Diversity Antennas

UR announced a new line of high-performance ceramic diversity antennas from its partner Pulse Technitrol. These antennas enable high data-rate transmission, yet are small enough to fit in mobile terminals such as multimedia phones, notebook computers, PDAs, media players, WLAN routers, data cards and other wireless devices.

Their ceramic composition provides a high degree of signal immunity, enabling them to be placed close to other antennas for high-performance diversity operation in small devices. Using diversity antennas in close proximity enables them to be switched within microseconds if one antenna experiences noise, providing improved signal quality with fewer drop-outs.

The series consists of six products: the 850MHz RX, 900MHz RX, 1.8GHz RX, 1.9GHz RX, 2.1GHz RX and 2.4GHz RX based on standard diversity platforms. These light weight omnidirectional radiation antennas feature low profiles and compact sizes. Sizes are 10 x 3.2 x 2mm and 310mg for the 1.8, 1.9 and 2.1GHz antennas, 10 x 3.2 x 4mm and 600mg for the 850 and 900MHz, and 3.2 x 1.6 x 1.1mm and 33mg for the 2.4GHz antennas.

Pulse's new line of diversity antennas are RoHS compliant and are compatible with lead-free, surface mount processes. All products are field tested to ensure quality and reliability.

Antennas are available in tape-and-reel packaging.

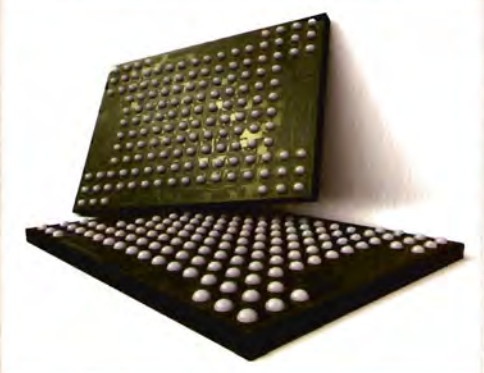
www.ur-home.com

Debut of a New Line of Camera Phone Image Sensors

A new line-up of image sensors is now available from Micron Technology. They have been developed using a 1.75-micron pixel design and range in resolution from 5, 3 and 1.3-megapixel.

The new sensors join Micron's previously announced 8-megapixel image sensor, also developed on the 1.75-micron pixel. Additional key features include the following: The 5-megapixel (product number MT9P012) fits into a 1/3.2-inch optical format and captures video at 60 frames per second (fps) at 720p, and 30fps at 1080p for high-definition video capture.

The 3-megapixel (product number MT9T013) fits into the standard camera phone 1/4-inch optical format and captures VGA video at 30fps.



The 1.3-megapixel (product number MT9V113) is a completely integrated camera system on-chip and fits into an ultra-small 1/6-inch optical format. This sensor also captures VGA video at 30fps.

General customer sampling for the 5- and 3-megapixel sensors is planned for the second quarter 2007 and the 1.3-megapixel sensor is expected to sample in late first quarter 2007. Mass production is expected this summer.

www.micron.com/products/imaging

EPIC Board for Standard PC/104 I/O Assemblies

With the EPIC/PM series Kontron introduces its second family of EPIC standard boards. It is based on the 90nm Intel Pentium M 745 processor and offers complete PC/104-Plus functionality with both PCI and ISA expansion.

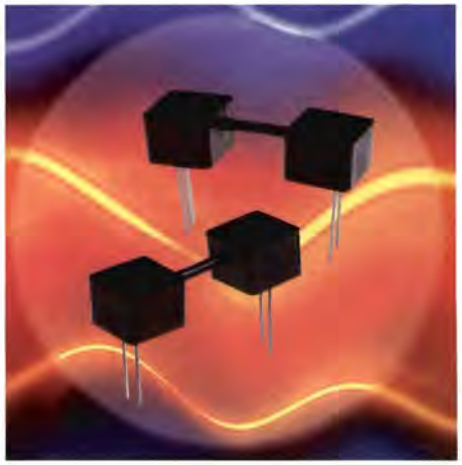
The processor is a 1.8GHz version with 2MB L2 cache. For cost-sensitive applications or fanless operation, the EPIC/PM is also available in ULV Celeron M 373 with 1GHz (512 KB L2) or Intel processor Celeron 800MHz (0KB L2) versions.

There's a high number of front-mounted I/O connections for reduced cabling and ease of accessibility. The boards include four high-speed USB 2.0 interfaces and two 10/100 BaseT LAN ports among others. For solid state operation, a compact flash socket is also provided. Additional on-board interfaces include two USB 2.0 interfaces, three COM ports, an 8-pin GPIO interface, EIDE, floppy and a Compact Flash socket. System memory of up to 2GB is possible with two DDR SODIMM sockets.

A watchdog timer, real-time clock, LANBoot and DarkBoot round out the feature set. These features are part of the software tool suite EVA, which is included with every Kontron EPIC product.

www.kontron.com

Optical Isolators for Industrial, Medical and Office Equipment



TT Electronics Optek Technology has developed a family of optical isolators – the OPI1270, OPI1280 and OPI1290 series, consisting of a visible red LED with photo-transistor or photologic sensor.

The isolators are designed for applications that require high voltage isolation between input and output, as well as signal communication over short distances. They offer high noise immunity and a heavy duty opaque housing to shield the optical signal from dust.

Able to mount each end of the isolator at different locations in the system, the design of the OPI1270, OPI1280 and OPI1290 optical isolators maintains excellent data transmission characteristics while being available in a variety of custom lengths.

The isolators feature an isolation voltage of more than 20kV with 0.05" (1.27mm) lead spacing. Power dissipation rating is 100mW, with an operating temperature range of –40°C to +100°C. Optek will also produce devices to meet customer requirements. Custom electrical specifications, wire and cabling, and connectors are also available.

www.optekinc.com/products/opto_isolators.asp

High-Power Fibre Optic Combiners

AMS Technologies has announced the availability of a wide range of new, high-power, fibre optic combiners from SIFAM Fibre Optics Ltd.

The systems are used either directly in metal cutting and welding or to pump the latest generation of high-power fibre lasers for precision marking or industrial and medical machining applications.

The latest products from SIFAM include state-of-the-art 6+1x1 high power combiners with single mode (SM) or polarisation maintaining (PM) fibre feed-through. SIFAM has also introduced new and novel combiners featuring large mode area (LMA) feed-throughs.

Availability of LMA fibre in the combiners enables higher brightness amplifier outputs with reduced distortion and improved beam quality.

All multimode fibre combiners from SIFAM can now be supplied with up to 19 input fibres and with larger diameter 220µm input and 400µm output fibres. This enables matching to a wider range of double clad fibres and the use of increased pump power, so that system designers can continue to improve fibre laser and amplifier output power, beyond 100W.

www.ams.de

"The **secret** to **success** is to know something nobody else **knows**."

Aristotle (384 BC - 322 BC)

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