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May 2006 **Volume 113** **Number 1841**

Front cover image: supplied by Techtronix

Books, books, books!

It's that time of year again when we have a new selection of technical books for reviewing. Please have a look at the choice below and if interested in any of them write an email to the Editor at EWeditor@nexusmedia.com, stating the book's title. The way book reviewing normally works is that, as a reader, you select the book of interest to you (it is normally done on a 'first come, first serve' basis, so be certain to register your interest quickly). Once you receive the book and finish reading it, write us a short review, anything between 800 and 900 words — or longer if you feel the book merits it, and you can then keep the book for your library.

- RFID Toys – Cool projects for Home, Office and Entertainment *Amal Graafstra*
- Engineering Disasters – Lessons to be Learned *Don Lawson*
- Advanced Manufacturing Technology for Medical Applications *Ian Gibson*
- Military Avionics Systems *Ian Moir and Allan Seabridge*
- Bosch Automotive Handbook (Sixth Edition) *Robert Bosch GmbH*
- Automotive Electrics/Automotive Electronics (Fourth Edition) *Robert Bosch GmbH*
- Electric Relays – Principles and Applications *Vladimir Gurevich*
- The Definitive Guide to How Computers Do Math *Clive 'Max' Maxfield*
- Wear – Materials, Mechanisms and Practice *Edited by Gwindon W Stachowiak*
- PIC in Practice – a Project-Based Approach *D W Smith*
- Practical Process Control for Engineers and Technicians *Wolfgang Altmann*
- The Design Warrior's Guide to FPGAs – Devices, Tools and Flows *Clive 'Max' Maxfield*
- Advanced Systems Design with Java, UML and MDA *Kevin Lano*
- Software Design for Engineers and Scientists *John Robinson*
- Building Interactive Worlds in 3D *Jean-Marc Gauthier*
- Software Defined Radio – Baseband Technology for 3G Handsets and Basestations *Edited by Walter Tuttlebee*
- The Digital Consumer Technology Book – A Comprehensive Guide to Devices, Standards, Future Directions and Programmable Logic Solutions *Amit Dhir*

In addition, we also have a few books to give away, without the 'hard' work of you having to review them. If interested, please let us know which one you'd like to have and the lucky few whose names will be drawn at random will receive these free of charge. Please use the same email address as above. Good luck!

- 1 x Engineering the World – Stories from the First 75 Years of Texas Instruments
- 1 x Antenna Toolkit *Joe Carr*
- 4 x Self on Audio – past content from Electronics World magazine *Douglas Self*

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Infrared is being edged out by Bluetooth

Infrared communication between devices is being replaced by wireless communication, and especially Bluetooth. Whilst not so long ago IrDA used to dominate the sector for portable peripherals such as printers, now it is Bluetooth.

"Even though we used two IrDA cones in our portable printers to enlarge the angle of communication, in 2005 it [the demand for these systems] changed. A lot of terminal [PDAs, mobile phones, laptops etc] manufacturers are using Bluetooth and we have no choice but to follow. In 2005, 60% of all our installations were Bluetooth enabled. This year it will be even more," said Antony Revis, general manager at Extech Data Systems.

Extech was one of the first portable printer makers to introduce Bluetooth in its products. It uses the Bluetooth module from the Swedish supplier called connectBlue. This is a serial port adapter that allows any device with a UART/RS232/RS422 or RS485 port to communicate wirelessly, without additional software installation in the device. It supports Bluetooth 1.1 and Bluetooth 2.0, short range or long range, point-to-point or multipoint communication, depending on the product requirements. A feature named Wireless Multidrop enables the product to simultaneously communicate with up to seven remote Bluetooth devices and to automatically form a wireless multidrop network.

This module is also used in Extech's latest portable printer — Andes 3, which also accepts contact and contactless smartcards.

Andes 3 — the latest, rugged portable printer from Extech

High-speed cellular data captures the imagination

High Speed Downlink Packet Access (HSDPA) is becoming the new buzzword of the mobile phone business. Downlink data rates of 1.8 and 3.6Mbit/s, and even 7.2Mbit/s in both directions, with the coming High Speed (HSUPA) for 3G mobiles, is the next challenge, and eight chip and IP suppliers announced solutions at the recent 3GSM World Congress.

Qualcomm is one of them. It has been sampling an HSDPA chipset with a digital baseband and separate RF front-end since the end of 2004, well ahead of any services that are just starting to roll out. In addition, the firm is combining the digital baseband with an applications processor. The dual chip will sample in the middle of this year on a 65nm, says Terry Yen, marketing manager. Then, the company will move on to combine the baseband with the RF for a true single chip HSDPA/HSUPA solution, potentially sampling after 2008.

Momentum for HSDPA technology is gathering. Strategy Analytics predicts 70% of 3G handsets will use HSDPA by 2010, and Qualcomm claims 120 design wins so far. It started sampling a new version in March 2005, with higher data rates.

Competing with the digital baseband is a UK start-up, Icera. It developed a reconfigurable baseband modem called Livanto, which can be used for all three speeds with just a software upgrade. Other players are Agere, which launched a 3.6Mbit/s HSDPA baseband chip — the X455 — with a bill of materials of under $75 for mid-range phones; Infineon Technologies with its 7.2Mbit/s S-GOLD3H baseband processor; Freescale Semiconductors, which has demonstrated HSDPA software running on its dual core 1.300 EDGE chip, and plans to run HDSPA on its single core mxc.300; and Cambridge-based TTPcom.

According to Michael Dimelow, product marketing director at TTPcom, the firm taped out a core for the current generation WEDGE chips in February and plans to add HSDPA and HSUPA hardware by the middle of this year. Similarly, Israeli design house Comsys is working with a partner to implement an HSDPA system. It has already licensed its EDGE technology to Texas Instruments for a low-cost GSM phone in India and China, and it is adding the HSDPA/UPA baseband alongside. This will go up as far as 14.4Mbit/s, says the company.

UK firms – be cunning, says Lord

Lord Alec Broers (right) from the Royal Academy of Engineering is calling on the UK semiconductor industry and universities to be "cunning, creative and clever" to succeed in the new era of applying old technologies to new "combinations" and, as such, become a competitive world player.

"We [in the UK] have been going down hill [in the semiconductor business] since 1984. It's essential that we keep some expertise in silicon in the UK. We have to be a part of that," he said. "We can't realistically touch the Intels, Hitachis, Samsungs and STs of this world, but that doesn't mean we can't have a presence. What we are seeing now is novel combinations of old technologies, things like GPS, sensors and silicon in, say, biomedical applications. So, we need to come up with a strategy of how to participate effectively in this era. We have to be cunning, creative and clever. We need to see what's the best way of bringing this country overall competitiveness."

Lord Broers criticised the way money is currently being spent at universities, for what he said is irrelevant research. What he'd like to see is closer links between UK firms and academia to spawn more commercial research instead. "A lot of the money spent on science and technology in this country has to be spent on something real, central and important – not cosmology etc."

"In 1984, it was still the large research labs dominating technology. In the last 15 year things have changed. Things became too expensive for a single company to maintain. We've seen the rise of the monopolistic companies like Microsoft, IBM and Intel. The rest of the world has to accept that things are global and universities play a key part in that. University research has to be tightly coupled with the work of the industry," he added.

Lord Broers continued to say that despite the difficulties in merging research activities from universities with those of local companies, it's the only way forward. "It's a difficult era; it's [a] fragmented [industry] and it's difficult enough to port a technology from one department to another in one company, never mind get it from a university and into industry and make it effective. But, there we are – this is where the world has gone and we need to work with that."

Silicon's time is not up just yet

Bulk silicon cannot be replaced with novel devices as their electric and other properties do not match that of silicon, say semiconductor experts.

"The emerging devices will not replace silicon technology one day – it's misleading. The switching frequency for silicon is the best and so is energy dissipation, compared to other devices. Carbon nanotube [for example] has a very bad sub-threshold behaviour, which is not good for our industry," said Dr Thomas Skotnicki, advanced programme director at STMicroelectronics, based in Crolles.

Prof Mike Kelly from Cambridge University agrees. "No alternative technology comes remotely near to what CMOS is doing. We're going to be stuck with CMOS for a long time to come. No molecular transistor, tunnelling device or SET can compete with silicon, and if anybody comes up saying that one of them can, they'll have to pull something else out of the hat."

Indeed, the SIA roadmap states that CMOS will remain the industry workhorse until at least 2020, but after that its future becomes blurred. Bulk silicon has been scaled down mercilessly, despite resolution problems experienced on the way. However, further scaling down will be fraught with many other, potentially insurmountable problems.

"In R&D we are approaching the atomic resolution and scaling will end. Bulk silicon was successful when scaling it to 100nm, but at 65nm we had to add straining, then we moved to SoI and SoN, and by adding a metallic gate through silicide we can go to 32nm. To go beyond that point we need more engineering. We need to work on fringing capacitances and metallic junctions to move to 22nm. This is what we need to work on to be successful [in scaling silicon further down]," he said.

There are five key criteria that need to be met by any new device in order to be as successful as silicon has been in this industry: design productivity, low power consumption, manufacturability, reliability and low interference. But, if novel devices cannot equal silicon and silicon scaling is going to stop at one point, then what should the industry do? According to Dr Skotnicki, it is both.

"We need to, instead, complement CMOS with other devices' functions rather than substitute it totally. Therefore, we need to start turning on system level; we need to work on system level to make future advances."

IBM researchers have found a way to extend a key chip-manufacturing process to generate smaller chip circuits. They have created the smallest, high-quality line patterns ever made using deep-ultraviolet (DUV, 193nm) optical lithography used in "printing" circuits on chips. The distinct and uniformly spaced ridges are only 29.9nm wide, which is less than one-third the size of the 90nm features now in mass production and below the 32nm that industry consensus held as the limit for optical lithography techniques. IBM's new result indicates that a "high-index immersion" variant of DUV lithography may provide a path for extending Moore's Law further, thus buying the industry time.

Ω

The top two IT-related problems are operational incidents and staffing issues, states a global survey commissioned by the IT Governance Institute (ITGI). Security and compliance were reported to be the least important problems. Other findings include: 56% of the organisations surveyed understand and support the business users' needs; IT outsourcing is no longer seen as the most beneficial way to resolve IT problems – some 45% respondents believe it is ineffective and the number of companies that indicated they had no IT problems increased from 7% in 2003 to 21% in 2005.

Ω

Over 100 million RFID tags were shipped in China in 2005, says market research house In-Stat. It forecasts a figure exceeding 2.9bn tags to be shipped by 2009. During this period, the main RFID application will be for human ID through China's second-generation Resident ID Card program, in a country with population of over 1.3 billion.

Ω

The Innovation Advisory Service is looking for ambitious electronic firms to take part in a programme designed to help growth companies in the South East gain access to resources and funding for innovation. Support would include helping firms apply for funding, secure new business opportunities, investigate new technologies and access the latest research. To contact an Innovation Advisor businesses can call 0800 288 8807 or visit www.iasse.co.uk

Alunimum oxide useful in 'sticking' new types of nanotubes together

Researchers at the Weizmann Institute of Science in Israel have discovered that using aluminium oxide templates allows various particles to stick to each other, hence creating different types of nanotubes.

"We expected the nanoparticles to bind to the aluminium oxide template that had been done before; but we did not expect them to bind to each other, creating the tubes," said Prof Israel Rubinstein, head of the research team.

So far, nanotubes have been created by using carbon atoms. With the aluminium oxide method, the Israeli scientists created a nanotube built of gold and silver, which exhibits different electric and optical properties to that of carbon nanotubes. Although not mechanically strong as the carbon nanotube, the different materials nanotubes can be used as building blocks, tailoring them for diverse applications. The properties can be altered by choosing different types of nanoparticles or mixes, thus creating composite tubes. Moreover, the nanoparticle building blocks can serve as a scaffold for various add-ons, such as metallic, semiconducting or polymer-type materials, thus further expanding the available properties.

The tubes are produced at room temperature in a three-step process. A nanoporous aluminium oxide template is chemically modified to make it bind readily to gold or silver nanoparticles. When a solution containing the nanoparticles (each only 14nm in diameter) is poured through, they bind both to the aluminium oxide membrane and to themselves, creating multi-layered nanotubes in the membrane pores. In step three, the aluminium oxide membrane is dissolved, leaving an assembly of free-standing, solid nanotubes. The team has succeeded in creating various metal and composite nanotubes, including gold, silver, gold/palladium and copper-coated gold tubes.

"The tubes are porous and have a high surface area, distinct optical properties and electrical conductivity. Collectively, the tube's unusual properties may enable the design of future sensors and catalysts — both requiring high surface area, as well as microfluidic, chemistry-on-a-chip systems applied in biotechnology, such as DNA chips (used to detect genetic mutations and evaluate drug performance)," said Prof Rubinstein.

Custom liquid displays

TOP 10 TIPS

- Consider what useful information needs to be displayed on the custom LCD and the combination of alphanumeric and custom icons that will be necessary.
- Understand the environment in which the LCD will be required to operate. Operating voltage and temperature can heavily influence the contrast of the LCD and potentially limit the type of LCD that can be used.
- Determine the number of segments necessary to achieve the desired display on the LCD and reference the PIC microcontroller LCD matrix for the appropriate LCD PIC microcontrollers.
- Create a sketch/mechanical print and written description of the custom LCD and understand the pinout of the LCD. (Pinout definition is best left to the glass manufacturer due to the constraints of routing the common and segment electrodes in two dimensions.)
- Send the proposed LCD sketch and description for a written quotation to at least three vendors to determine pricing, scheduling and quality concerns.
- Take into account total NRE cost, price per unit, as well as any setup fees.
- Allow a minimum of two weeks for formal mechanical drawings, pin assignments and revised counter drawings.
- Request a minimal initial prototype LCD build to ensure proper LCD development and ensure proper functionality within the target application. Allow typically 4-6 weeks for initial LCD prototype delivery upon final approval of mechanical drawings and pin assignments.
- Upon receipt of prototype LCD, confirm functionality before giving final approval and beginning production of LCD.
- Be sure to maintain good records by keeping copies of all materials transferred between both parties, such as initial sketches, drawings, pinouts, etc.

This month's Top Ten Tips were sent in by Microchip.

If you'd like to send us your top five or top ten tips on any subject you like, please write to the Editor at **EWeditor@highburybiz.com**

Wi-Fi heads for the embedded market

Developers of wireless networking chips are heading for the mobile phone and embedded markets with new modules and chips. Market research firm InStat predicts that shipments of Wi-Fi enabled consumer devices, including cellular handsets, PDAs, game consoles and other handheld products, will exceed 180 million units by 2009.

US-based broadband chips supplier Marvell is developing a low power IEEE802.11 Wi-Fi module based on a variant of the ARM processor core. "We have been working with module vendors in Asia to create an 802.11b/g package that measures 9.6mm x 9.6mm," said Todd Tokubo, director of applications engineering for the embedded wireless business."

Conexant focuses on low power with its Wi-Fi chips

It is using a variant of the Feroceon core, an ARM-compatible core developed by Marvell, where the memory interface and instruction pipeline have been modified for lower power operation, and power down modes have been added to all the blocks in the core.

At the same time, Conexant Systems has been working with Sharp Electronics on a Wi-Fi module. This uses Conexant's CX3110X silicon and Sharp's packaging technology for a module under 10mm x 10mm in size.

"Low power and small form-factor are critical parameters for embedded mobile applications," said Chee Kwan, vice president and general manager at Conexant.

Marvell is also launching its first new standalone processor for embedded applications, also based on Feroceon. The 400MHz Orion processor is made in 0.15um technology.

DNA harnessed to create nanoscale transistors

Scientists at the Technion Israel Institute of Technology have harnessed the power of DNA to create a self-assembling nanoscale transistor. This is an important step in the development of nanoscale devices.

According to Professor Erez Braun of the Faculty Physics at the Technion, science has been intrigued with the idea of using biology to build electronic transistors that assemble without human manipulation. However, until now, demonstrating it in the lab has remained elusive.

To get the transistors to self assemble, the Technion research team attached a carbon nanotube onto a specific site on a DNA strand, and then made metal nanowires out of DNA molecules at each end of the nanotube.

To attach the nanotube to the DNA, Prof Braun coated it with protein and then added bacteria protein to the test tube. Proteins naturally bond together, hence the carbon nanotube bound to the DNA strand at the bacteria protein. The tiny metal nanowires were then created by coating DNA molecules with gold. In this step, the bacteria protein served another purpose: it prevented the metal from coating the bacteria-coated DNA segment, creating extending gold nanowires only at the ends of the DNA strand.

Out of 45 nanoscale devices created in three batches, almost a third emerged as self-assembled transistors. They can be switched on and off by applying voltage to them.

Prof Braun believes that initially these devices will be used in computers followed by tiny sensors to perform diagnostic tests in healthcare.

Texas Instruments (TI) has joined the High-Definition Audio-Video Network Alliance (HANA), a cross-industry collaboration focusing on connected, home entertainment products. The group was established in October last year and includes many consumer electronics makers, content and service providers, information technology providers as well as film studios. They are working together to create a design guideline for secure AV networks and user-friendly HD products. Among them are Mitsubishi Digital Electronics America, JVC, Samsung, Sun Microsystems, Oxford Semiconductor, Marvell, Freescale and many more.

Ω

LSI Logic has joined the Storage Bridge Bay (SBB) working group, an industry initiative set up to define a low-cost standard for storage controller slots. Dell and Intel are already members. Initially, the SBB working group will focus on developing and distributing specifications for the standardisation of external disk subsystem technologies. The specifications will define a mechanical/electrical interface between a passive backplane drive array and the electronics packages linked to the array. It is expected that the first release of the specification will be completed by mid-2006.

Ω

IBM and Dassault Systèmes announced a new cross-industry initiative aimed at fostering innovation and transforming the way their customers design, manufacture and deliver products to the market. The set of solutions is particularly aimed at industries where responding to customers on demand is critical, such as the electronics and consumer packaged goods industries.

Ω

The GSM Association (GSMA) and Intel announced an initiative to drive the adoption of GSM in laptop computers. Jointly they will develop guidelines for integrating 3G modems and SIM cards into laptop computers, enabling automatic connection to both 3GSM networks and Wi-Fi networks around the world — using the same SIM card technology used by mobile phones.
The alliance will seek to engage mobile operators, PC manufacturers and network infrastructure providers.

3G operators fight with DVB-T broadcasters over mobile TV

The European standard for mobile TV over digital terrestrial television networks is gaining momentum with several new chip announcements, but other technologies are emerging to challenge its dominance in the mobile phone market.

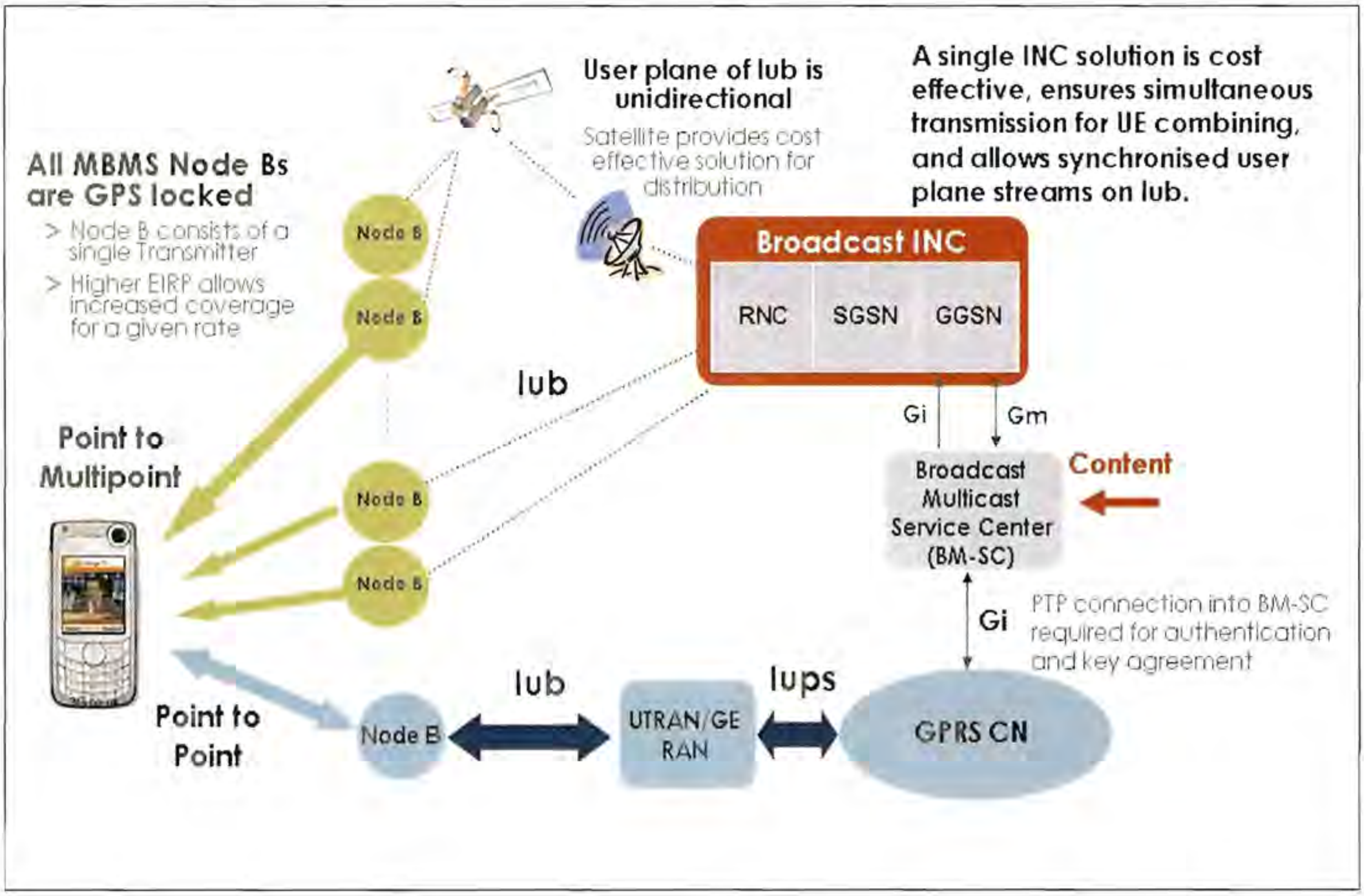
Philips Semiconductor, Micronas, Microtune, Siano Mobile Silicon and TTPcom all launched either a DVB-H tuner, a multi-standard chipset supporting DVB-H, DVB-T, T-DMB, DAB or development platforms for MDTV. All of them rely on partnering with a broadcaster to use existing digital terrestrial transmitters. DVB-H (Digital Video Broadcasting – Handheld) is based on the DVB-T standard for digital terrestrial television but tailored to the special requirements of the pocket-size class of receivers.

But, IPWireless, which has a large development centre in Chippenham in the UK, is offering operators a different way of sending TV to phones, this time using the 3G network instead. It has developed TDtv, which combines IPWireless's commercial UMTS TD-CDMA technology and the latest Multimedia Broadcast and Multicast Standard (MBMS) from the 3GPP standards body supporting 3G.

This allows TV to be sent via satellite to a basestation and then multicast direct to multiple 3G handsets, without having to set up many point-to-point calls. This dramatically reduces the cost of providing TV but keeps the operators in control of the content. UK operator Orange is now testing the technology and IPWireless is integrating the baseband chips into a PC card and into a single chip for 3G phones, where it will compete directly with DVB-H.

"It would be a terrible irony if the next big opportunity in mobile services didn't use 3G or put the mobile operators in control of the service offering," said Chris Gilbert, chief executive officer of IPWireless. "We have received a tremendous reaction to TDtv from operators because they see the opportunity to deliver a fantastic mobile media service experience to customers and show regulators and investors that they are using and getting a return on their 3G spectrum."

IPWireless's TDtv architecture based on the TV-CDMA standard



Russia enters high-tech stratosphere

Russia is keen to start competing in high-tech and is creating economic zones to kick-start the process.

Head of the Russian government, Mikhail Fradkov, signed a decree for the creation of six special economic zones at the beginning of this year. Four of these will be focusing on high-tech applications and two on industrial production. The high-tech zones will be established in Dubna and Zelenograd (both near Moscow), and Saint-Petersburg and Tomsk. The industry zones will be set up in Elabug (Tatarastan) and Lipetsk.

Zelenograd will cover microelectronics, Saint-Petersburg information technologies and the development of analytical devices, Dubna nuclear physics and Tomsk new materials. Lipetsk will specialise in the production of electronic consumbles.

Mikron, a chipmaker based in Zelenograd, has already agreed three projects with foreign firms. These include the manufacture of chip cards in cooperation with Giesicke & Davrient, which began operation in March this year; a chip modules packaging line to be launched in June this year in partnership with Infineon; and a future upgrade of the chip cards production line, scheduled for 2007.

Mikron is considered a leading Russian chip manufacturer, which was founded in 1964. Its high-tech design centre opened in May last year.

Tsarskoye Selo, St. Petersburg

Peter-Paul fortress, St Petersburg

Spansion aims for secure smartcard market with HD-SIM

Flash memory maker Spansion is preparing a new range of secure smartcard chips. It is combining a 32-bit ARM processor with its Mirror Bit flash memory and an encryption engine licensed from M-Systems of Israel to allow user data to be stored on the smartcard, removing the need for an extra memory card slot in cost-sensitive mobile phone designs.

The HD-SIM also includes hooks for digital rights management and 'sensors' to control access to the different system blocks, to protect the content on the smartcard. "I believe that the smartcard is the best place to put DRM," said Jean-Marc Julia, vice president and general manager for Europe at Spansion. "It has all the appropriate watchdogs."

This will also allow content providers to pre-load music and games on the phone to reduce the subsidies paid by operators.

MirrorBit is a NOR memory array with a NAND interface, which lends itself well to integrating with logic and interconnect, says Julia. It stores data in two memory locations in the cell, making it more secure than multiple bits in one cell, without an area penalty. A 1Gbit device is 82 to 90mm^2 in a 90nm process, similar to 83mm^2 for NAND flash. The chip also includes interfaces for USB for high speed access.

Partners for the technology – which will only be supplied as a chip, not a module – will be announced in the autumn, with the first 64Mbit single chip at the beginning of 2007 and higher densities later next year.

Bridging the skills Gap

"Keep university research alive" is the message from **Keith Attwood**, CEO, e2v technologies

With UK manufacturing under-performing as an industry group, its leaders have been debating the way back to health for some time. Some believe it is down to businesses themselves to adapt to global competition and others argue that the responsibility lies with the government. No matter what view you may take, increasing investment in skills is essential if the UK is to secure a positive manufacturing future.

Increasingly, less developed countries are acquiring the know-how to make many of their own products, rather than importing them. This is just one reason the UK has been struggling to maintain its competitive advantage. The UK's stronghold in high-tech, high-end sectors is now under threat and companies need to ensure business structures are correct to enable a continued stream of well qualified technologists and prevent a critical skills gap.

Meanwhile, major capital projects such as Heathrow T5 and Stansted T2 have shown we face shortages right across our practical skills base. Looking ahead, one can only wonder how we are going to fare when it comes to the Olympics in 2012.

So what can we do?

The education system has to become more appropriate to the needs of world-class businesses, which means delivering competent people from the ground up. We need to stimulate the interests of young people in science, technology and engineering or we will struggle in the future. UK-based firms face competition in countries with relatively low labour costs and where education and skills levels are high, for example, hourly labour costs in South Korea are just over half UK levels, but the proportion of graduates in the working age population is almost identical. But if more British businesses make long-term commitments to education and strategic partnerships, the UK will remain at the cutting edge of manufacturing and the future will be more appealing.

Indeed, academic collaboration has historically proved successful across the globe. Strategic partnerships like these help develop innovative technologies that inevitably aid growth. In turn, discoveries made help customer's maintain their world leading positions in their respective markets.

Without a constant feed of new ideas and technology from the academic world many firms would not have been able to maintain their market positions. For example, e2v collaborated with Brunel University to launch a Centre for Electronic Imaging, which concentrates on transforming R&D activity into new imaging technology and developing products for new markets.

"Without a constant feed of new ideas and technology from the academic world many firms would not have been able to maintain their market positions"

Partnerships with government are another means to ensure that the necessary level of research flows through the industry and fuels growth. After much delay, the British government has begun to realise the importance of businesses and universities coming together to boost the countries ability to compete in this knowledge-based global economy.

Knowledge Transfer Partnership schemes (KTP) have replaced the old Teaching Company Scheme, and are a successful tool that enable the transfer of strategic technology and knowledge from universities into UK industry. Bright ideas come from stimulated and involved people and KTPs and academic collaboration enable this. However, more can be done. It's generally accepted that the future for British industry depends on skills and innovation, and bringing this innovation to the marketplace is totally intertwined with the knowledge resources available at universities. Such development needs funding and requires that companies shouldn't turn away in the mistaken belief that it's only about high-tech, and therefore is not for them.

Companies must innovate right across their businesses. People are much as part of this as anything else. It is of paramount importance that manufacturing companies and government act more strategically to address current skills shortages. Innovation results in the technology that brings exciting new products and services to the market place. Innovation results in high quality jobs, successful businesses, better goods and more efficient processes. Innovation must not be ignored.

Research consistently demonstrates the positive correlation between innovation and company performance. By increasing investment in skills and creating a culture of innovation, the UK will inevitably be in a better position to achieve and maintain competitive advantage in the increasingly global market place.

Keith Attwood, CEO, e2v technologies

Philippines: More Than Just Call Centres

By Steve Rogerson

The Philippines is often not at the top of company lists when looking for opportunities abroad, but **Steve Rogerson** discovered that for many sectors, the country is worth a closer look

The Philippines can provide a base for exporting to other countries in south-east Asia

A first look at the Philippines gives the impression that the only opportunities for western companies, including those from the UK, are in outsourcing, whether manufacture or, increasingly, call centres; the country had more than 70,000 call centre seats by autumn 2005 and is increasing that number all the time. While it is true that the country does provide a ready source of cheap, well-trained labour, and that the outsourcing path is one actively supported by the Philippines government, it would be a mistake to view this as the only opportunity the country provides.

One such area for exports actually stems from the cheap labour. A number of companies, including some large electronics companies, have set up manufacturing plants there, and these plants need raw materials. The UK has a number of producers of such electronics components, from quite sophisticated devices down to basic connectors, all of which are needed in the manufacture of, say, laptop computers and other electronics goods. Though these will eventually be re-exported from the Philippines as part of a finished product, there is still an opportunity for British companies to sell their wares and many are already doing so.

Another key market is in mobile communications. The mobile market in the Philippines is relatively small compared not just with Europe but with other countries in south-east Asia. As mobile penetration grows, there is a lot of scope for investment. Though the low income of many in the country may prevent this penetration hitting the dizzy 80% plus heights seen in some countries, there is room for the penetration to increase rapidly in the next few years. Penetration stood at 40% by the end of 2004.

This, ironically, is helped by the poor infrastructure in the country. Fixed telecommunications does not reach every home and so provides an opportunity for mobile operators to make their products the technology of choice for communications. This is a pattern that has already been seen in some Eastern European countries and it is likely that the Philippines will follow that route.

The opportunities this presents lies not in hardware – the global handset market is well tied up between the big players such as Nokia, Motorola, Sony Ericsson and the like – but in software. The trend now is for mobile phones to become all-in-one communications devices and electronic personal assistants, and these require software. Popular everywhere is games software and there is a shortage of such applications in the Philippines. In fact, they are actively looking for providers of gaming software for mobile devices.

There is also an increase in fixed broadband as residential users sign up to ADSL, as well as a number of companies in the corporate sector, including the important SME market. The main use in the corporate market seems to be for IP VPNs.

The country is also dipping its toes into the wireless LAN market and there is likely to be significant growth in this area in the next few years. Wireless LAN hot spots are already available in selected shopping malls and other commercial areas. Also, as everywhere, the corporate sector is starting to consider wireless LANs as a cheap, efficient way of networking an office.

Where western countries such as the UK have an advantage here is in experience. Though this technology is hardly past its infancy in the Philippines, there is now a wealth of experience in setting up corporate wireless LANs and solving the security problems that go with them. This is expertise that could be sold to the Philippines.

Where the country is seriously lagging behind other countries is in Internet access, though this is growing with the proliferation of Internet cafes. Also, many hotels are now providing Internet access in their rooms as a matter of course.

UK companies already have a good track record in exporting educational software to south-east Asia and should therefore be looking to adding the Philippines on their radar. This may be a slow process but the opportunity is there to establish a foothold early on.

Another potential area for the selling of expertise is in energy conservation and environmental protection. Europe is well advanced in both these areas, whereas the Philippines is only just beginning to realise its importance.

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Oscilloscope Measurements of Power Dissipation in Switch-mode Power Supplies

In this article, **Hans-Peter Fleischheuer** describes how a Digital Phosphor Oscilloscope (DPO) equipped with appropriate power measurement software can be used to carry out the necessary measurement and analysis of key parameters in switch-mode power-supply applications

With demand for power driving architectural changes to switching power systems, the ability to measure and analyse the power dissipation in next-generation switch-mode power supplies (SMPS) is critical. New power supply architectures with much higher data speeds and Gigahertz-class processors that need higher current and lower voltages are creating new pressures for power-supply designers in the areas of efficiency, power density, reliability and cost.

To address these demands, designers are adopting new architectures incorporating synchronous rectifiers, active power-factor correction and higher switching frequencies. These techniques, in turn, create new challenges, like high power dissipation at the switching device, thermal runaway and excessive EMI/EMC effects.

A key parameter in understanding these effects is the power loss that occurs during the switching process. During the transition from 'off' to 'on' state, the power supply experiences higher power loss. The power loss at the switching device while in the 'on' or 'off' state is lower because the current through the device or the voltage across the device is quite small.

The inductors and transformers associated with the switching device isolate the output voltage and smooth the load current. These inductors and transformers are also subjected to switching frequencies, resulting in power dissipation and occasional malfunctioning because of saturation.

Because the power dissipated in a switch-mode power supply determines the overall efficiency of, and the thermal effect on, the power supply, the measurement of power loss at the switching device and the inductors and transformers assumes great importance – especially for indicating power efficiency and thermal runaway. Therefore, it will be extremely useful to accurately and rapidly measure and analyse instantaneous power loss under changing load conditions.

Talking challenges

Among the challenges faced by designers to achieve such measurements and instantaneous analysis of power loss for different devices are:

- Establishing a test setup for accurate power-loss measurement
- Correcting errors caused by propagation delay in the voltage and current probes
- Computing power loss at a non-periodic switching cycle
- Analysing power loss while the load is changing dynamically
- Computing core loss at the inductor or transformer.

Fortunately, sophisticated power analysis software is now available, which runs on the latest generation of Digital Phosphor Oscilloscopes (**Figure 1**), sharing a common 'look and feel' with the oscilloscope user interface to provide intuitive navigation and ease of use. This power measurement and analysis application software helps switch-mode power-supply designers to accurately perform power-loss analysis on the switching devices and magnetic components, as well as performing detailed input/output analysis. Key features of the software include a facility known as 'Hi-Power Finder' (described in more detail later), sophisticated report generation, a ripple finder, the ability to make magnetic measurements, and a quick and efficient automatic de-skew capability.

Test setup for accurate power-loss measurement

Figure 2 shows a simplified circuit for a switch-mode power supply. The metal-oxide semiconductor field-effect transistor (Mosfet), driven by a 40kHz clock, controls the current. The Mosfet in Figure 2 is not connected to the AC main ground or to the circuit output ground. Therefore, taking a simple ground-referenced voltage measurement with an oscilloscope would be impossible because connecting the probe's ground lead to any of the Mosfet's terminals would short-circuit that point to ground through the oscilloscope.

Making a differential measurement is the best way to measure the Mosfet's voltage waveforms. With a differential measurement, it is possible to measure the drain-to-source voltage (VDS), which can ride on top of a voltage ranging from tens to hundreds of volts, depending on the range of the power supply.

There are several possible methods of measuring V_{DS}:

- Float the oscilloscope's chassis ground. This is not recommended because it is highly unsafe and endangers the user, the device under test and the oscilloscope.
- Use the two conventional passive probes with their ground leads connected to each other and use the oscilloscope's channel mathematics capability. This measurement is known as 'quasi-

differential'. However, the passive probes in combination with the oscilloscope's amplifier lack sufficient common-mode rejection ratio (CMRR) to adequately block any common-mode voltages. This setup cannot measure the voltage accurately, but it allows the use of existing probes.

- Use a commercially available probe isolator to isolate the oscilloscope's chassis ground. The probe's ground lead will no longer be at ground potential, and the probe can be connected directly to a test point. Probe isolators are an effective solution, but are expensive, costing two to five times as much as differential probes.
- Use a true differential probe on a wideband oscilloscope for the accurate measurement of V_{DS}.

For current measurements through the Mosfet, the user first clamps on the current probe. The next step is to fine-tune the measurement system. Many differential probes have built-in DC offset trimmers. With the device under test turned off and the oscilloscope and probes fully 'warmed', the oscilloscope is set to measure the mean of voltage and current waveforms, using the sensitivity settings that will be used in the actual measurement. With no signal present, the trimmer is adjusted to null the mean value for each waveform to 0V. This step minimises the chance of a measurement error resulting from quiescent voltages and currents in the measurement system.

Figure 1: The Tektronix DPOPWR power measurement and analysis software runs on the company's DPO7000 series of Digital Phosphor Oscilloscopes (DPOs)

Correcting errors caused by voltage and current probe propagation delay

Before making any power loss measurement in a switch-mode power supply, it is important to synchronise the voltage and current signals to eliminate propagation delay. This process is called 'de-skewing'. The traditional method calls for calculating the skew between the voltage and current signal, and then manually adjusting the skew using the oscilloscope's de-skew range.

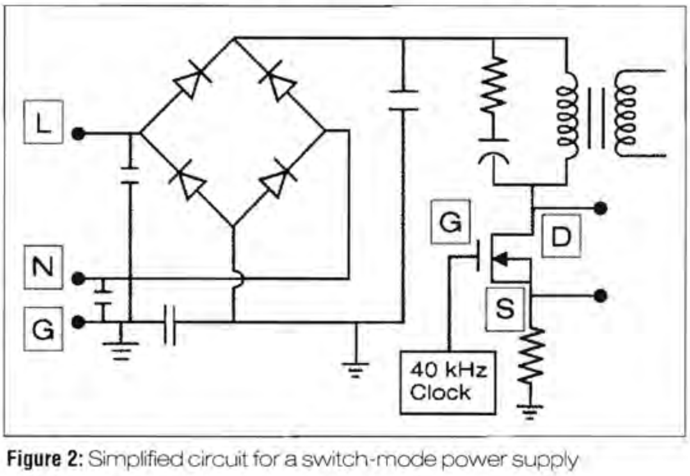

Figure 2: Simplified circuit for a switch-mode power supply

However, this is a time-consuming process.

The process can be greatly simplified by using a high -bandwidth DPO equipped with a de-skew fixture and power measurement software. To de-skew, the differential voltage probe and the current probe are connected to the de-skew fixture's test point. The de-skew fixture is driven by either the auxiliary output or the calibration output signal of the oscilloscope. If desired, the de-skew fixture can be driven by an external source. The de-skew capability of the power analysis software will automatically set up the oscilloscope and calculate the propagation delay caused by the probing. The de-skew function then uses the oscilloscope's de-skew range and automatically offsets for skew. The test setup is now ready for accurate measurements. **Figures 3** and **4** show the current and voltage signal before and after de-skew.

Computing power loss at a non-periodic switching signal

Measuring the dynamic switching parameter is simple if the emitter or the drain is grounded. But, with a floating voltage, a differential voltage must be measured. To accurately characterise and measure a differential switching signal, a differential probe is required. A Hall-effect current probe allows the current through the switching device to be viewed without breaking the circuit. The automatic de-skew feature of the power analysis software is then used to eliminate the propagation delay caused by the probes.

The 'switching loss' feature in the software automatically computes the power waveform and measures minimum, maximum and average power loss at the switching device for the acquired data. This is then presented as turn-on loss, turn-off loss and power loss, as shown in **Figure 5**. This is useful data for analysing power dissipation at the device. Knowing power loss at turn-on and turn-off allows the user to adjust the voltages and current transitions to reduce the power loss.

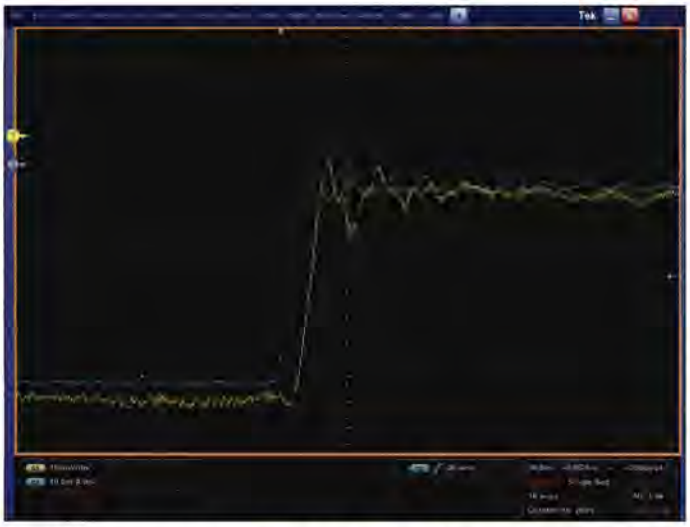

Figure 3: Propagation delay for a voltage and current signal

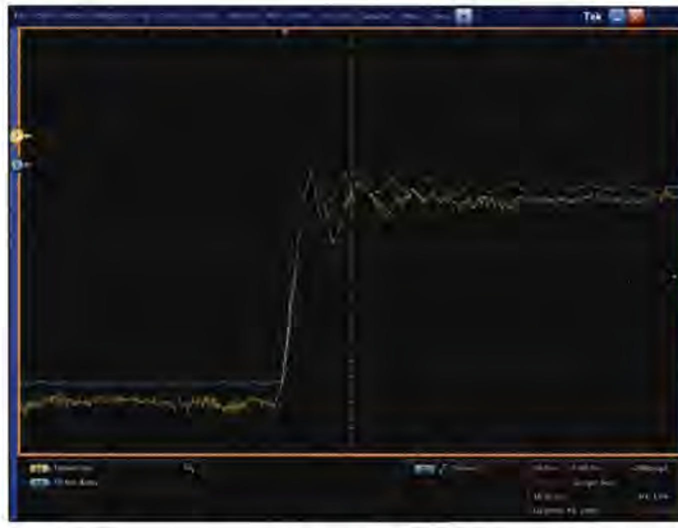

Figure 4: The signal shown in Figure 2 after the automatic de-skew operation

During the load change, the control loop of the switch-mode power supply changes the switching frequency to drive the output load. **Figure 6** shows a power waveform when the load is switched. Note that the power loss at the switching device also changes as the load is switched. The resulting power waveform will be non-periodic in nature.

Analysing the non-periodic power waveform can be a tedious task. However, the advanced measurement capabilities of the power analysis software automatically compute the minimum power loss, maximum power loss and average power loss, providing additional information about the switching device.

Analysing power loss while load is changing dynamically

In a real-world environment, the power supply is continuously subjected to a dynamic load. **Figure 6** shows that the power loss that occurs at switching also changes during the load change. It is very important to capture the entire load-changing event and characterise the switching loss to make sure that it does not stress the device.

Today, most designers use an oscilloscope with deep memory (2Mbyte) and a high sampling rate to capture events with the required resolution. However, this presents the challenge of analysing a huge amount of data from the switching loss points. The 'HiPower Finder' feature of the power analysis software eliminates this challenge of analysing the deep memory data. A typical result is shown in **Figure 7**, while **Figure 8** goes a step further by showing a summary of the number of switching events and the maximum and minimum switching losses in the acquired data. It is then possible to view the desired switching loss points by inputting a particular range of interest. All the user has to do is to choose the point of interest within the range and ask the HiPower Finder to locate it within the deep memory data. The cursor will link to the requested area. On locating the point, the software can be used to zoom in around the cursor location and see the activity in more detail. This, combined with the previously mentioned switching-loss capabilities, quickly and effectively analyses the power dissipation at the switching device.

Computing power loss at the magnetic component

Another way to reduce power dissipation comes in the magnetic core area. From the typical AC/DC and DC/DC circuit diagram, the inductor and transformer are the other components that will dissipate power, thereby affecting power efficiency and causing thermal runaway.

Typically, inductors are tested using an LCR meter which produces a sine-wave test signal. In a switch-mode power supply, the inductors will be subjected to high-voltage, high-current switching signals, which are not sinusoidal. As a result, power-supply designers need to monitor the inductor or transformer behaviour in a live power supply. Testing with an LCR meter may not reflect a real-life scenario.

The most effective method of monitoring the behaviour of the core is through the B-H curve, which quickly reveals inductor behaviour in a power supply. The power analysis software allows rapid B-H analysis to be carried out on an oscilloscope without the need for expensive and dedicated tools.

The inductor and transformer will have different behaviour during the turn-on time and steady state of the power supply. In the past, to view and analyse B-H characteristics, designers have had to acquire the signals and conduct further analysis on a PC. The oscilloscope software now enables the B-H analysis to be performed directly on the oscilloscope, providing instantaneous viewing of inductor behaviour as shown in **Figure 9.**

This magnetic analysis capability also automatically measures power loss and inductor value in a real-world power-supply environment. To derive the core loss at the inductor or transformer, all that is required is to make power-loss measurements at the primary and the secondary. The difference of these results is the power loss at the core. Also, under no-load conditions, the power loss at the primary is the total power loss at the secondary, including the core loss. These measurements can reveal information on the power dissipation area.

The necessary tools

Key features of the power measurement and analysis software described in this article, including the ability to measure the

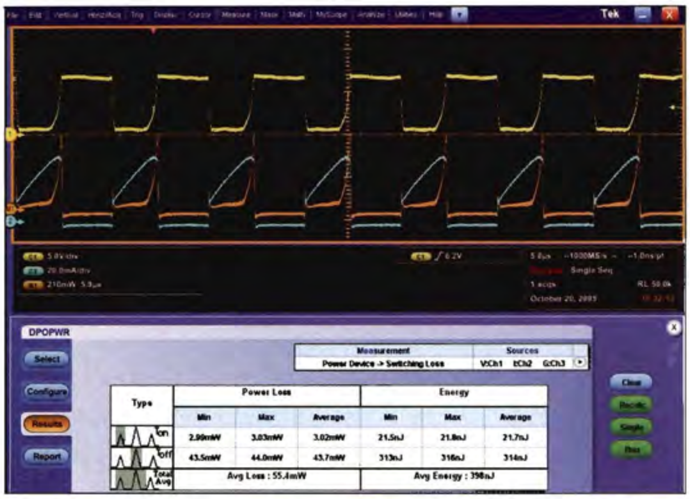

Figure 5: Minimum, maximum and average power loss during turn-on at the switching device

Figure 6: Minimum, maximum and average power loss at the switching device during the load change

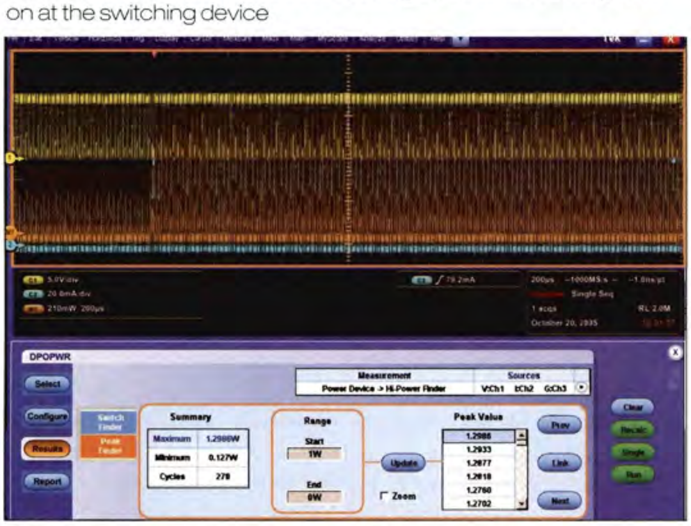

Figure 7: The result of using HiPower Finder, showing power waveform at the switching device at load change

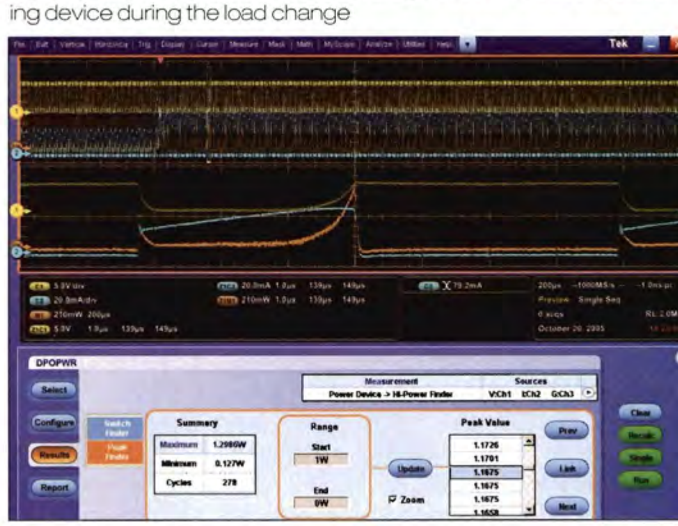

Figure 8: Using HiPower Finder and oscilloscope zoom for further analysis

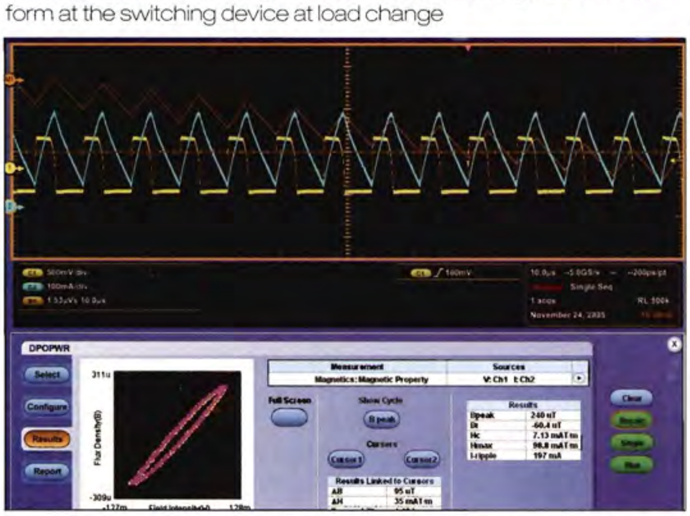

Figure 9: Instantaneous B-H plot for the acquired waveform, showing cursor linkage

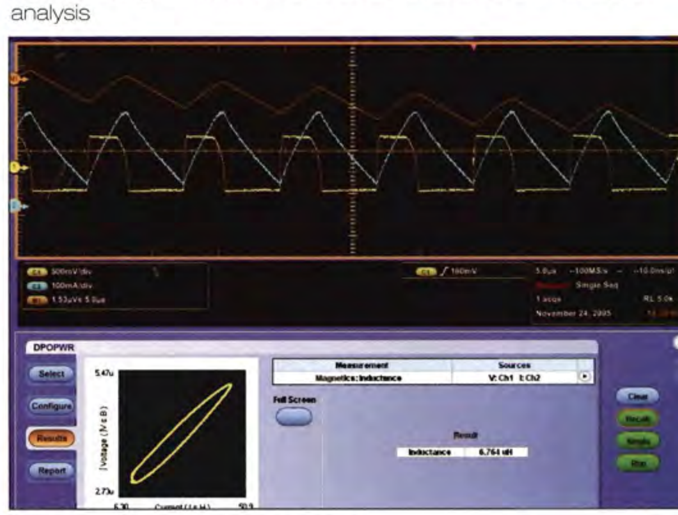

Figure 10: Inductance measurement

power loss at the switching device, the 'HiPower Finder' capability and B-H analysis, provide the tools necessary to make rapid measurements on switch-mode power supplies. When using a DPO, the software allows users to quickly locate the power dissipation areas of interest and to view the behaviour of power dissipation in a dynamic situation.

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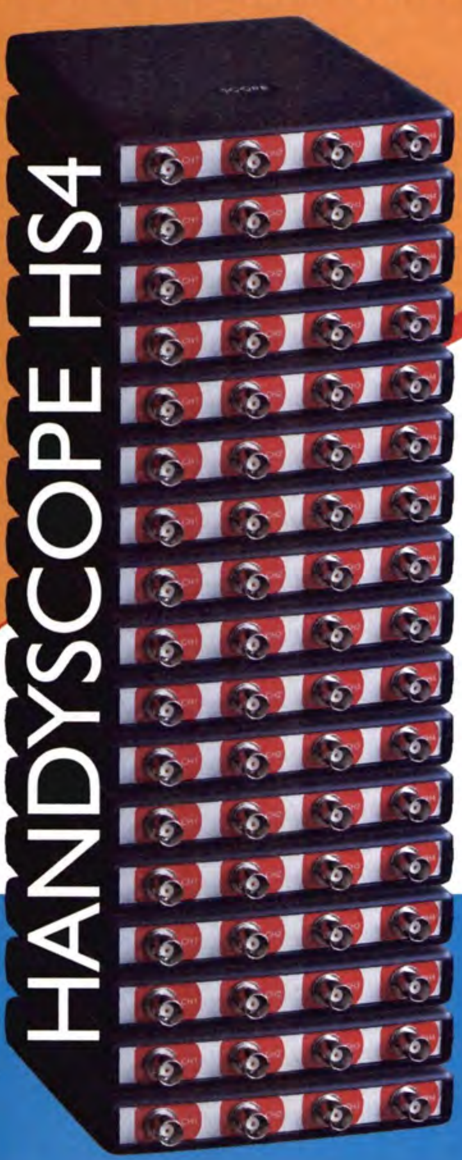

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SOI Process Pushes Boundaries for Low-power and Precision Amplifiers

Process technology has become a key differentiator for state-of-the-art analogue products.

Dr. Huibert Verhoeven, Senior Design Manager for Precision Amplifiers at National Semiconductor explains how the company created VIP50

Analogue and digital process technologies are on rapidly diverging paths. Digital process technology has focused on economies of scale. Large wafer diameters, currently up to 12 inches, and decreasing feature sizes have enabled an enormous increase in digital circuit complexity. Deep submicron circuit technology's extremely high development and implementation costs have driven standardisation in digital process capability.

At the same time, maximum allowable supply voltages have come down significantly due to the increased circuit density. Maximum operating voltages of 1.8V and below are common in today's digital processes. Integration of high-performance analogue circuits in an ASIC or application-specific semiconductor product (ASSP) utilising a state-of-the-art digital process is becoming less and less feasible.

Complex worlds

The analogue world is more complex. Supply voltage requirements are typically dictated by system considerations. Many industrial test and measurement systems still operate with 10V power supplies due to signal-to-noise and legacy system design considerations. Automotive systems, which are operated directly off an unregulated car battery, need to be able to operate at 12V and be able to survive voltages of up to 27V to accommodate jump-starts and temporary system fault conditions. Future automotive systems that may include battery voltages up to 42V will further complicate the analogue landscape.

In addition to a higher supply voltage, a number of industrial and automotive systems also require operation up to 150°C. Leakage currents inherent to semiconductor devices increase by a factor of approximately two for every 10 degrees of temperature increase, limiting circuit performance when using standard IC technologies. 150°C temperature operation also pushes the limits of IC packaging technology and will require more bare-die solutions.

Medical systems, on the other hand, require high accuracy and an increasingly high level of integration. Medical imaging systems, for example, often consist of a large number of parallel channels in a small footprint. Obtaining high bandwidths and low noise at the lowest possible power level is crucial in these applications.

National Semiconductor decided two years ago to develop an analogue IC process specifically optimised for high-performance amplifier applications. Key focus was put on obtaining a wide operating voltage range, a wide operating temperature range, excellent speed-to-power ratios and world-class accuracy.

Precision analogue

The efficiency of integrated transistors is limited by the parasitic capacitances between the terminals of the devices and the substrate, which is the bulk material of the silicon wafer in a traditional process. Power is wasted charging and discharging these parasitic capacitances. The bulk of the wafer also effectively connects all circuit elements together. Undesirable current conducting paths and, in extreme cases, circuit latch-up can occur during power sequencing or when voltages exceeding the power supply rails are applied to the inputs.

The VIP50 process eliminates the efficiency and latch-up downsides of conventional bulk silicon-based IC processes by using a silicon-on-insulator (SOI) starting material. The use of SOI technology is common in modern, high-speed IC processes but has, so far, not been used in processes optimised for precision analogue applications.

Additional benefits of SOI technology are the ability to process high-voltage signals outside of the normal process maximum operating voltage, as well as the reduction of crosstalk between analogue and digital blocks in mixed-signal solutions.

A potential downside of SOI technology is the reduced power rating, since generated heat is now effectively isolated from the substrate handling wafer through the electrically and thermally insulating oxide layer. Design, layout and packaging techniques can be employed to minimise the reduced power handling capability.

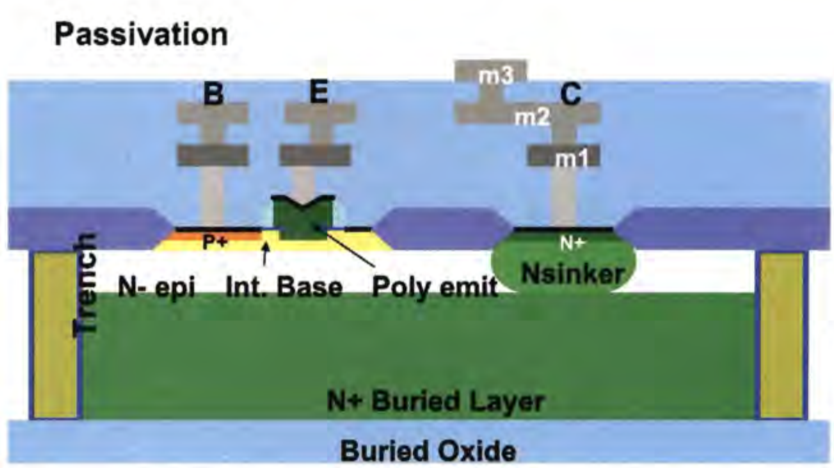
The next choice to be made in the development of an analogue IC process is the active elements that are to be available. Over the last two decades, digital circuitry has typically been implemented using CMOS technology, while bipolar processes dominated the high-performance analogue domain. Each transistor type offers its own set of benefits and drawbacks.

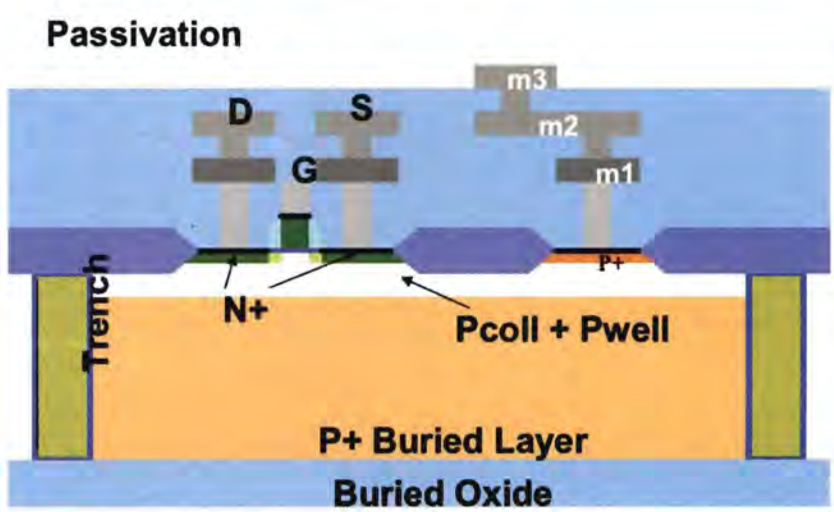
Bipolar benefits

Bipolar transistors generally offer a higher speed-to-power ratio than their CMOS counterparts when used in analogue applications. Voltage noise performance also tends to be superior for a given amount of supply current. Lastly, bipolar transistors, in most cases, offer better DC accuracy due to superior transistor matching characteristics. Matching is the driving factor behind many precision amplifier circuits. National Semiconductor used the SOI expertise it gained in the development of its VIP10 high-speed bipolar process and applied it to a lower speed, but highly accurate, VIP50 technology.

High-speed processes typically focus on the highest attainable transit frequency (Ft). This frequency is reached at high collector currents, typically in the milliampere range. The VIP50 process is optimised for peak performance at much lower collector currents. As a result, operational amplifier circuits with a total supply current of less than 700nA have been demonstrated.

A benefit of optimising the poly-emitter VIP50 process for lower supply currents is that the significant low-frequency noise, traditionally associated with high-speed poly-emitter processes, is greatly reduced. **Figure 1** shows a cross section of an NPN transistor implemented in the VIP50 process. The PNP transistor is fully complementary to the NPN transistor. The identical topology of the NPN and PNP transistors enables the design of well balanced and highly efficient amplifier output stages.





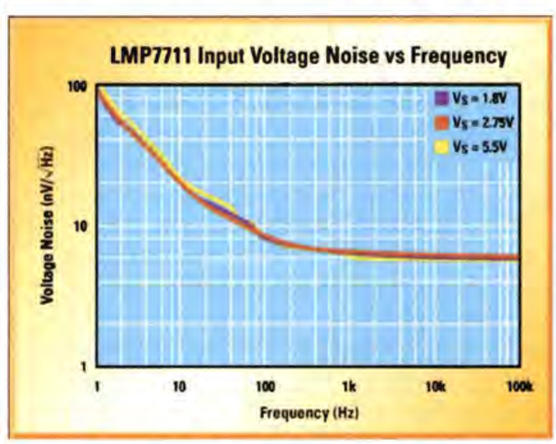


Figure 1 – Top: Cross section of an NPN bipolar transistor in the VIP50 process.

Figure 2 – Middle: Cross section of a NMOS transistor in the VIP50 process

Figure 3 – Bottom: Voltage noise curve of a typical MOS input operational amplifier in the VIP50 process

MOS benefits

MOS transistors, however, offer the area-efficient integration of large amounts of digital or mixed-signal circuitry. Mixed-signal capability is becoming increasingly more important as the integration level of precision analogue circuits transitions from the single amplifier level to more complex functional blocks, such as programmable gain sensor interface circuits with bus programmability.

MOS transistors also offer a number of attributes that can be extremely valuable in analogue circuitry. MOS devices exhibit extremely high input impedance. In many test and measurement applications, a high input impedance is important to eliminate errors caused by an error current flowing into the input pin of the first amplifier of the signal chain. Transimpedance amplifiers, as are commonly used in photodiode readout circuitry, also greatly benefit from the inherently high MOS transistor input impedance. In addition, MOS devices offer a superior output swing in rail-to-rail amplifier output configurations. **Figure 2** shows an NMOS transistor implemented in the VIP50 process. The PMOS transistor is again fully complementary to the NMOS device.

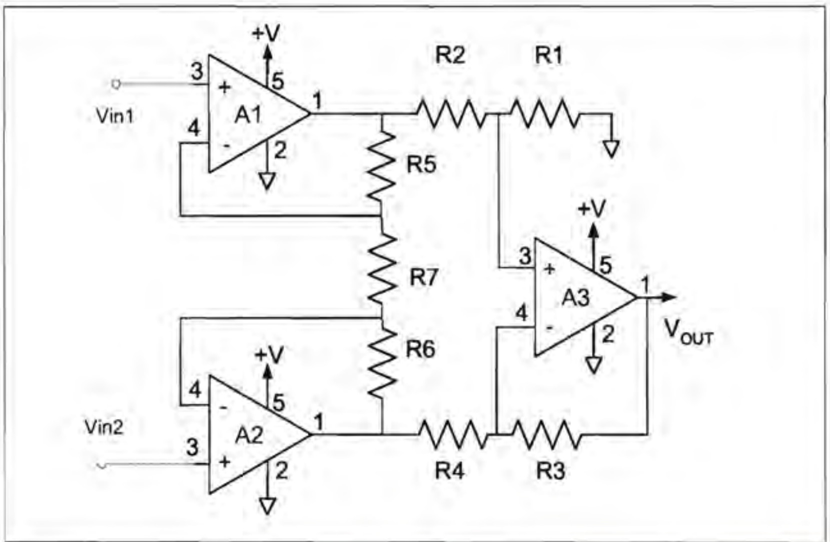
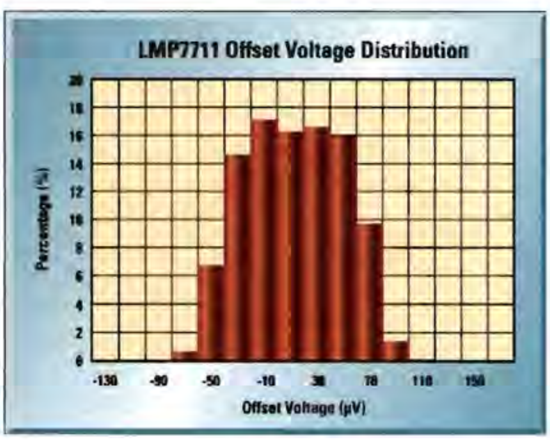


Figure 4 – Above: Basic diagram of an instrumentation amplifier

Figure 5 – Right: Offset voltage distribution of a typical MOS input operational amplifier in the VIP50 process



Optimising VIP

In the case of the VIP50 process, a BiCMOS technology was chosen to enable the use of bipolar and CMOS transistors in the same circuit. The bipolar transistors are optimised to operate well under a wide range of operating currents, thus enabling a diverse product range including sub-microampere operational amplifiers and comparators, as well as operational amplifiers that offer a ten times higher speed-to-power ratio over previous generations and competitors' solutions. The bipolar transistors are also capable of operating at supply voltages of up to 12V for use in many industrial, medical and automotive applications.

The MOS transistors were specifically optimised for analogue performance. Two parameters targeted were the transistor matching of MOS transistors, which is of great importance for MOS input amplifiers, as well as the voltage noise performance at low frequencies. MOS transistors suffer from a phenomenon called 1/f noise. Below a certain operating frequency, called the corner frequency, the noise of a MOS input amplifier will start to rise significantly. Pushing down the frequency at which this 1/f phenomenon kicks in is critical to allow the use of MOS transistors as a front-end to sensitive sensor readout circuitry.

Figure 3 shows a typical voltage noise curve of a MOS input operational amplifier created in the VIP50 process. Note that the 1/f noise corner is well below 1kHz, enabling accurate low-frequency amplification. The MOS transistors can also operate at voltages of up to 12V through a combination of process and design techniques.

A final critical element in a high-performance analogue process is an extremely accurate resistor. Resistors determine the accuracy of many amplifier-based applications. The VIP50 process offers highly matched, low-temperature-coefficient thin-film resistors. Resistor matching of better than 0.01% can be obtained. Resistor matching of this level is obtained through a combination of processing techniques, layout techniques and wafer-level laser-trim techniques.

The extreme accuracy of the thin-film resistors enables the integration of feedback resistors in fixed-gain and programmable-gain amplifier applications with a resulting gain accuracy that exceeds the accuracy that can be obtained through the use of conventional matched precision resistor pairs. **Figure 4** shows a basic block diagram of a typical instrumentation amplifier. The accuracy of this amplifier is largely dominated by the matching accuracy of the resistors. **Figure 5** shows an offset voltage distribution of one of the MOS input operational amplifiers created in the VIP50 process.

Input offset voltage levels previously achievable only through the use of bipolar transistors have now been obtained through a combined use of analogue-grade MOS devices and laser-trimmed thin-film resistors. The low parasitic capacitance and resulting parasitic coupling of on-chip precision resistors also enable higher-speed and extremely noise-sensitive applications that can not easily be addressed through the use of external resistors.

Differentiating factor

In summary, process technology is a strong differentiating factor for today's high-performance amplifier products. The VIP50 technology combines the advantages of bipolar and MOS devices in one process. Accurate resistors and the ability to use laser trim to change resistor values are available.

A silicon-on-insulator technology is used to increase the speed-to-power ratio of many amplifier solutions tenfold. Many high- performance analogue applications will benefit from the power efficiency and precision levels the VIP50 process offers.

Analogue and Digital Approach to Power Management

Dr Nazzareno (Reno) Rossetti from Fairchild Semiconductor has 30 years of experience in design, applications and marketing in the analogue and mixed signal semiconductor segments. Here he outlines the pros and cons of choosing analogue vs digital design for power management applications

The age long debate of digital versus analogue has recently come to the power arena, generating at time concerns and emotional responses from the analogue bastions. Digital is still flourishing but the real world remains analogue. And a power supply is no different than any other real world system: its output is analogue (voltage, current, power, etc.) the same way that digital TVs, digital still cameras and digital cell phones yield analogue outputs (moving video, still pictures, sound etc). Beyond the obvious communications aspects, which have been around for quite some time and are eminently digital, digital power simply refers to the progressive digitalisation of some processing elements at the centre of the power conversion system. However, there should be no doubt that the outer shell (the power train, the voltage reference, etc), namely the interface to the analogue world, will remain analogue.

Generally speaking, an analogue circuit is a device in which data is represented by continuously variable, measurable, physical quantities, such as length, width, voltage, or pressure.

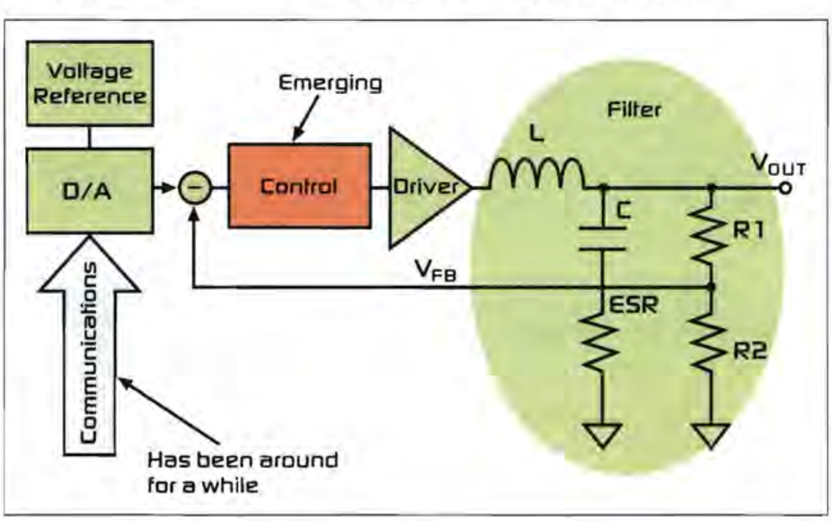


Figure 1: Power conversion and management plant

However, under the analogue market classification we find data conversion and interface products, which are classes of devices with high content of digital data and circuitry. Evidently, there is more to the analogue market than the eye beholds.

Indeed, under the analogue label we find a broad array of mixed signal applications, ranging from pure analogue to digital, as well as from power to signal. Analogue is indeed a rich primordial soup that spawns new circuits, architectures and solutions at every turn of the technological journey. As demonstrated by the market intelligence companies' data reporting, analogue has grown into a big mixed signal giant, spanning the full spectrum of circuitry from purely analogue to digital.

Analogue continues to grow and outgrow the total market despite the very real phenomena of digitalisation. This happens because of the reasons discussed earlier and because analogue remains a realm of unmatched creativity: there were no capacitive regulators (charge pumps) 10 years ago, no LED drivers 5 years ago, and the list goes on. In the end, digitalisation of pure analogue circuits remains a home-grown phenomenon within the broadly defined analogue market, confirming the leading creative capacity of analogue. After all, there cannot be digitalisation of analogue without analogue.

Limits to digitalisation

Figure 1 shows a block diagram of a generic power conversion and management system. All the blocks in green (voltage reference, D/A, driver, filter) are the characteristic elements interfacing the 'external' analogue world and, hence, will remain analogue for the reasons explained above. The communications block has been around for a long time and has always been digital (serial or parallel communication bus). The control block, traditionally implemented in analogue, has in the recent five years been revisited in terms of digital implementations.

Current industry trends indicate that digitally-controlled architectures for power conversion (the servo control algorithm circuitry) especially, and power management (communications via new serial or parallel bus protocols, sequencing circuits etc.) are coming into their maturity. In the coming years, predictions are that these architectures will be capable, in some cases, of displacing their analogue counterparts.

Again, these claims need to be read in the right context. A power supply remains a rough environment, submitting the semiconductor materials to great stresses. The inductor in a switching regulator or the coil in a motor will stress cyclically the electronics with voltage spikes well above the V_{CC} power supply and well below ground. Such over and under-voltage excursions tend to awake parasitic transistors in the semiconductor device that have a detrimental effect on the system. These ugly aspects of interfacing with the real world are not the realm of digital electronics. This is rather frontier territory that constitutes a non-trivial challenge for even the most experienced analogue designer. In fact, parasitics are probably what makes power/analogue design an art rather than a science. There are no SPICE simulators today capable to model the three-dimensional effects of parasitic transistors and, as long as this remains the case, analogue will continue to be "black magic" in the hands of a few adept designers.

Analogue and digital architectures

Figure 2 illustrates a typical analogue control implementation of a voltage regulator, where a Pulse-Width-Modulated (PWM) switching regulator is built around a modulator. The analogue modulator, at the heart of this modulation scheme (**Figure 3)** is composed of a comparator, having at one input a periodic piecewise-linear (triangle or saw-toothed) modulation waveform V_{ST} of period T, and at the other input the error signal Vε. As the quasi-stationary error signal Vε falls between the minimum and the maximum of the modulation waveform, the intersection of these two waveforms determines the duration of the 'on' pulse TON. Accordingly, the comparator output produces a square wave VSW whose average value coincides with the DC output voltage VO. In this scheme, the PID (Proportional-Integral-Differential) block can be implemented with an op-amp and external passives (compensation resistor, Rc, and capacitor, Cc); or, alternately, it can be fully monolithic by integration of the Rc, Cc compensation network.

Figure 4 illustrates a digital control architecture in which the input error signal (Vfb-Vref) is converted to digital via an analogue-to-digital con-

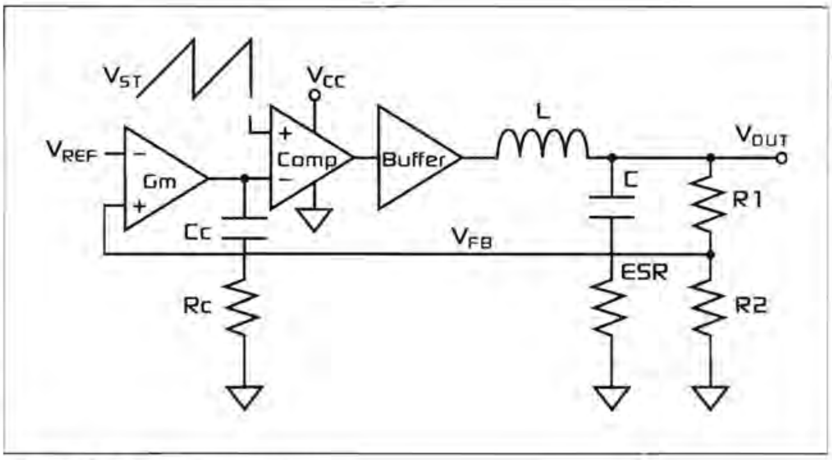


Figure 2: Analogue control loop

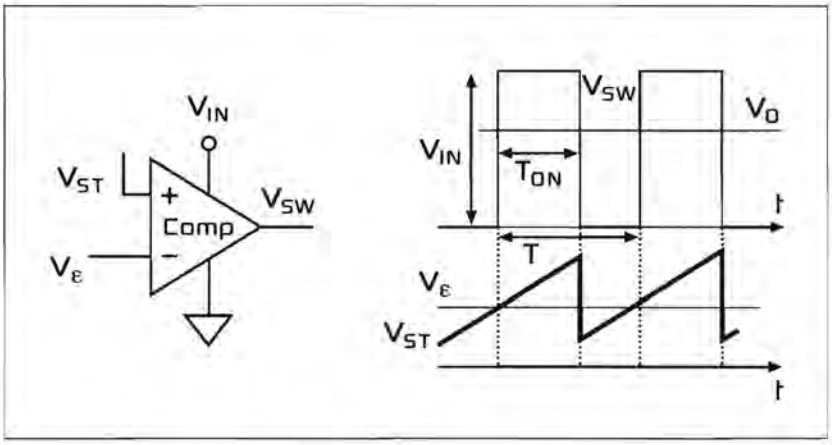


Figure 3: Implementation of the analogue modulator

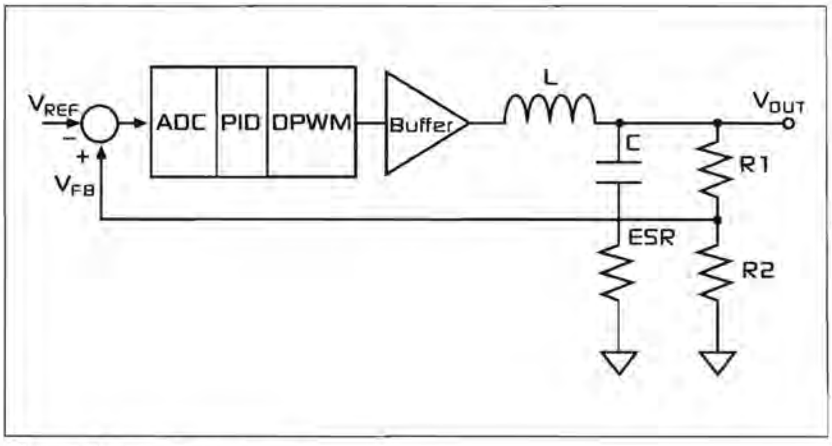


Figure 4: Digital control loop

verter (ADC) and, hence, the PID compensation and digital modulation (DPWM) is all done in the digital domain.

At the heart of the digital power conversion control loop is the digital modulator. **Figure 5** illustrates a simple and effective way to implement a digital modulator via a ring oscillator. In this example, the ring oscillator runs at 1MHz fre-

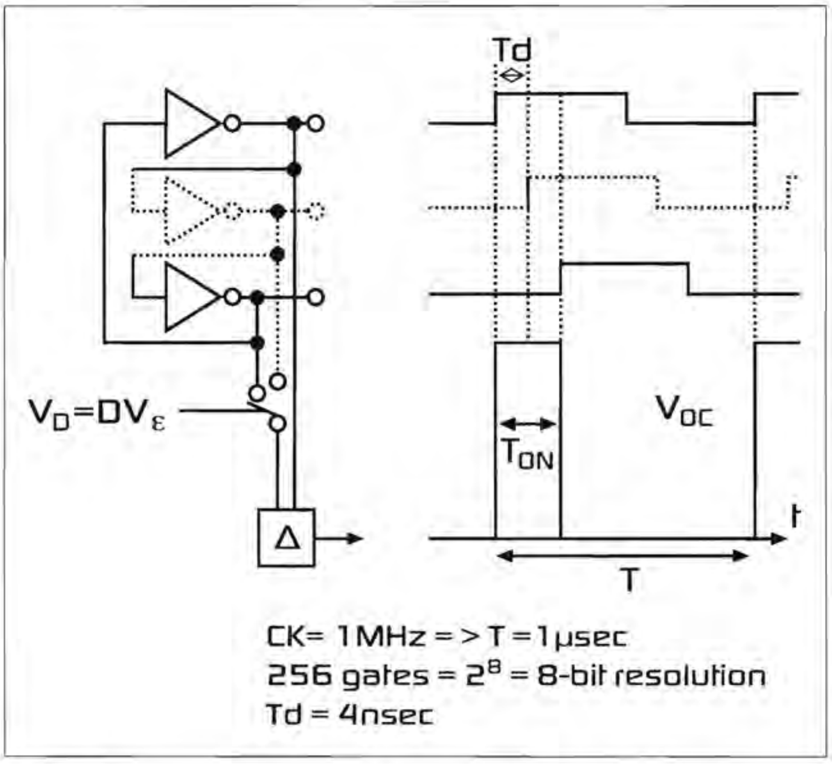


Figure 5: Digital modulator

quency (T=1us), which is also the clock frequency of the digital PWM system, and is made of 255 gates (the number must be odd in the simplest implementation for the ring to oscillate), corresponding to 8 bits of resolution. It follows that each gate output has a square waveform that is delayed from the preceding gate of 1/255 of the clock period or roughly 4ns.

The 'on' pulse at the output of the digital modulator is formed by proper selection of the time delay between a given subset of gates, with the selection done via a digital selector driven by the digital error signal voltage DV_ε.

Selecting the control algorithm

If the system to be regulated is truly linear, meaning continuous and invariant in its mode of operation, or else is smooth, then analogue is generally the way to go. This is true in the case of a desktop CPU voltage regulator whose output must be controlled continuously by the same algorithm from no load to full load. If, on the other hand, the system is non-smooth, meaning discontinuous and variable in its mode of operation, then digital may be a better option.

For example, digital might be better justified in the case of a notebook or mobile phone voltage regulator application where, due to the necessity to save power at light loads, a mode change is required. This scenario typically occurs from a PWM algorithm to PFM (Pulse-Frequency Modulation). PFM is a mode in which the frequency adjusts with the load, thereby yielding lower frequencies and hence lowering switching losses at lighter loads.

Such a mode change in an analogue system would require an abrupt commutation from one control loop, say PWM, to the other (PFM), typically at the time that the load is changing. This type of algorithm discontinuity would invariably lead to some degree of temporary loss of regulation of the output.

By contrast, a digital control is inherently equipped to handle discontinuities and, therefore, would be capable of handling mode changes within a single control algorithm.

Power management and conversion applications

The obvious benefit of digital power management is ease of communication, programmability, status reporting, etc. A classic example of this type of digital control in an application is a smart battery charger powering a notebook in a smart battery system. This system comprises a smart charger, smart battery and host microcontroller. In this case, the smart charger "slave" device receives commands from the "master" host controller via the System Management Bus (SMBus). It then adjusts its parameters to provide the required current, voltage and power to the smart battery, and then reports its values back to microcontroller.

In power conversion applications, a microcontroller-based digital architecture has many useful purposes thanks to its flexibility, especially in applications where not only programmability, but current- and voltage profiling is also required.

Current profiling applications

Current profiling is required in lighting ballast applications, where the intensity and duration of the current can be flexibly set for different lamps, as well as for the three operational phases of pre-heating, ignition and dimming. Current profiling is also required in PFC applications, where the current drawn by a load from the wall outlet must be in phase with — basically have the same shape of — the line voltage. If we repetitively apply the sinusoid rectified line voltage across the PFC boost inductor for a constant "on" time, we can build a train of pulses of current (each single pulse actually having a triangular shape) proportional to the line voltage. This construction works well during the build-up phase of each current pulse.

Unfortunately, the decaying phase of the inductor current, governed by the difference between the quasi-constant PFC output voltage and the widely varying rectified sinusoidal input voltage, abnormally stretches each current pulse.

This produces an overall distortion of the current pulse train (3rd harmonic distortion). However, the amount of distortion is completely predictable and can be entered into a ROM table and used to vary the "on" time of the PFC stage enough to compensate for such error.

Complementing analogue

By analysing the power semiconductor market, we see that the digitalisation phenomenon is limited and complementary to analogue rather than in competition to it. Analogue design is indeed a mixed digital/analogue endeavour and traditional analogue designers will not have difficulty to add in their toolbox the new architectural elements that digital can contribute with, including its ability to change, on the fly, parameters like the loop compensation and, hence, withstand wider load changes and poor layouts. It may also be able to calibrate out-errors in the system, especially external, low-cost component tolerance errors. The advantage is the potential for better yields, lower testing costs and lower BOM costs. With all of these possible advantages, one may wonder why digital power has caught big share of attention but little market share. The answer lies in the fact that the market has made it very clear that digital will be preferred over analogue, but only at cost parity or below. Therefore, the only successful digital power products will be those that continue to solve a customer's problem by utilising slick architectures with minimum overhead, and that do not result in a cost penalty versus their analogue counterparts.

A March 2005 report from Darnell called "Emerging Markets in Digital Power Electronics: Component, Converter and System Level Opportunities, First Edition" (page 114) shows that digital POL (point of load) has a CAGR of 155%, going from 0.2MUs (million units) in 2005 to 6.8MUs in 2008, while analogue POLs will grow at 15%, from 21MUs to 36MUs, in the same period. This and other data confirm that digital control will assert itself gradually, while still leaving plenty of room for analogue or mixed analogue/digital control algorithms.

Power management needs to be more sophisticated

Andrew Repton, Principle Design Engineer at Dialog Semiconductor looks into the ways of optimising efficiency in ever more complex system designs

Today, the battery chemistry of choice for most consumer and professional mobile applications is based on lithium technologies, such as lithium ion or lithium polymer cells. These exhibit excellent capacity characteristics and also have terminal voltages in the region of 3.3 to 4.2 volts, allowing efficient power management in systems using ICs with 3V nominal supplies.

As IC voltage requirements continue to fall to maximise operating times, many systems now also need multiple power domains and more sophisticated power management functions. In order to meet this need, designers have traditionally been able to choose from a wide variety of off-the-shelf low integration power management parts from multiple vendors, enabling rapid product development. Quite often, the power sub-systems for even the most complex circuits comprised just one or two supplies and some discrete components such as LDOs (low drop out regulators) and buck converters.

The increasing complexity of some systems designs, especially in the realms of portable electronics equipment, means that more control is required and the designer then needs to consider how to optimise efficiency by turning off unused functionality and also to ensure correct and stable operation when running multiple supplies, often to the same IC.

The result is that it is no longer enough to use multiple discrete components. Together with increased design complexity, there is the parallel need to take a system level approach to designing the power management sub-system — an approach which adds complexity to the basic functions of voltage generation and regulation. This could be met by adding additional devices to the collection of parts already used but this invariably increases cost and in many cases — more importantly — PCB area.

By considering higher levels of integration, it must also support the overall functionality required in the system. From the power management perspective, this requires more thought to be put into defining the functions of a power management sub-system, and whether all the functions can be integrated without compromising technical performance. For example, a typical handheld application has a lithium power source, processor controlling the main functionality, memory, external peripherals such as a display, memory expansion such as SD or MMC card and some analogue functionality such as data conversion or sensor interfacing. Such a system requires a number of different power domains as each function has different requirements. The processor may typically require two supplies, a low voltage for its core to save power consumption and higher voltage to interface with the other devices. Analogue functions tend to require higher voltages to guarantee operating headroom or provide powerful output drivers, and display drivers tend to require higher voltages as display size and complexity increases.

Other issues that should be considered in an integrated power management sub-system include:

- Turning the system on: is a mechanical switch sufficient or is an electronic method needed, such as an output from a sensor circuit or an alarm signal? Also, how does this interface to the controller (a classic example is a dual function key which combines power and another function)?
- Battery supply going out of range (under and over voltage).
- Sequencing of individual supplies: a problem with multiple voltage domains where the highest supplies need to be activated first to prevent IC latch up.
- Are any permanently active supplies required for data retention or sleep functionality?

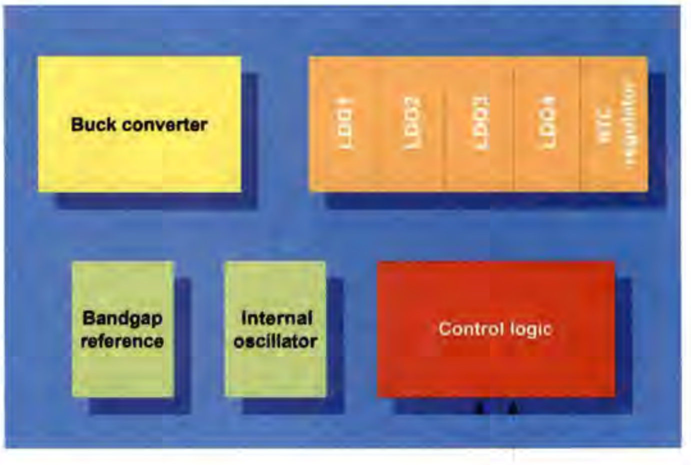


Figure 1: Typical block diagram of a power management sub-system IC providing core functionality for lithium powered portable applications. This architecture is based on the DA9025 power management IC

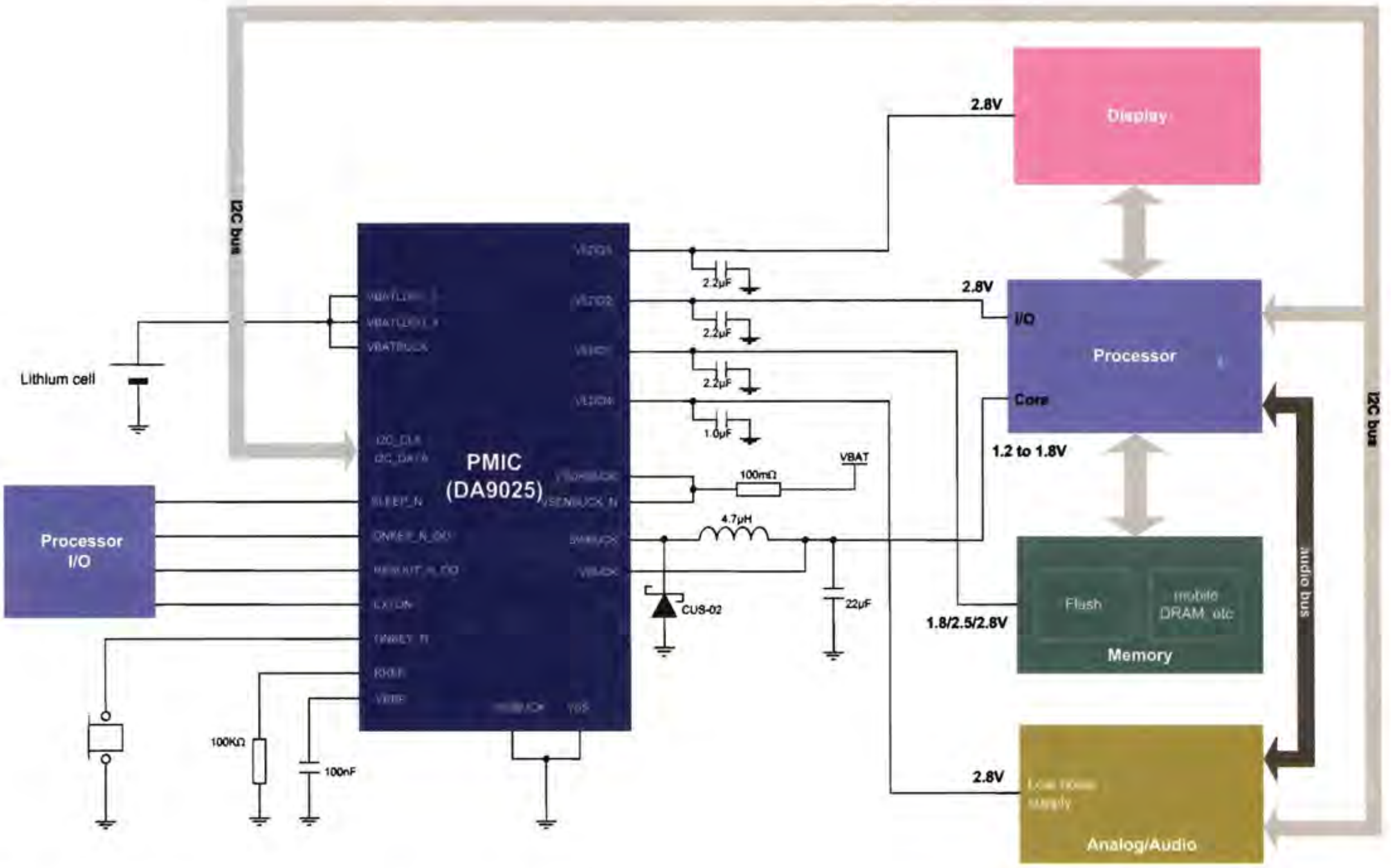


Figure 2: A typical portable media player system and the role of the PMIC

- Switching the system off without removing the battery.

Issues such as these can be addressed using standard parts such as POR (power-on-reset) circuits, battery monitor IC and PLDs (programmable logic devices); however, this adds components to the system, adding cost and taking additional PCB area.

System-level view

Alternatively, a system-level view might help to integrate a higher level of functionality into the IC. A power management sub-system IC (PMIC) would meet this need, fitting in between the simple single function device such as a low dropout regulator (LDO) or switching converter, and a sophisticated system-on-chip IC containing many functions including power management.

The purpose of such a PMIC (see **Figure 1**), is to provide the core functionality for lithium powered portable applications, providing efficient operation in order to maximise battery life. The core functions would typically be a high efficiency buck converter and a number of low quiescent current low dropout linear regulators (LDOs).

Looking at a PMIC in a typical system (see **Figure 2**), there are several different external issues it would need to take care of. For example, the power management IC needs to interface directly with a battery pack – typically a single lithium ion power source – and operate with or without a controller, generating and controlling a number of system supplies. In the simplest of systems (where, say, no controller is present but multiple supply domains are required) applying a suitable battery voltage and enable signal will start the device, activating all regulators. The PMIC could continue to operate until either the user turns off the device using the ONKEY pin or an error condition occurs, such as low battery voltage.

From a control and programmability point of view, the more the options the greater the flexibility in terms of regulated output voltage. Interfacing to a microcontroller using simple control via dedicated pins might be a simple option, or more comprehensive control using an I2C bus could be offered for programmable output voltages.

Minimising current consumption

Typically, the PMIC will contain a number of low dropout voltage regulators (LDOs), DC-DC buck converter and other functions.

LDO voltage regulators are a central part of the power management system, creating a stable, low noise supply voltage for other ICs in the system. Important specification parameters for the LDO are power supply rejection ratio (PSRR) and quiescent current, of which the latter will directly impact standby time. The quiescent current of each single regulator may seem small but in systems with multiple regulators and other functions, when magnified by 10 or 20 times, this becomes significant.

The PSRR is a measurement of the level of disturbance still present on the power supply line once regulation has taken place. If these transients are not suppressed they can appear in the audio band as unpleasant tones. Even worse, they can add modulation on the RF signals, which can cause spurious transmissions that require additional filtering (and cost) to remove.

To achieve high PSRR across a wide frequency band, the LDO error amplifier usually has its bias current set for the highest output current, which is the worst case operating condition. As this bias is fixed, and so independent of current demand, this results in the amplifier being over-biased and consuming a higher quiescent current than required even at low current demands. For this reason, high performance LDO designs usually need to have a low power sleep mode to reduce the inefficiency at low current demands.

A unique approach to the problem, patented by Dialog Semiconductor, utilises a design technique known as the Smart Mirror LDO regulator, a part with higher PSRR performance compared to other regulators available today.

The Smart Mirror regulators mirror the output current demand back to the bias generator, which allows the bias to be reduced automatically as demand falls and gives dynamic quiescent current control (see **Figure 3**). This gives a regulator with high PSRR and dynamic performance over a wide range of operating currents, without being constrained by the usual design compromise of being over-biased under all conditions, except when under maximum load. Having an autonomous adaptive bias control also removes the need for a low power operating mode and, hence, any user intervention to switch to a lower power mode at low current demands.

Supplying 10mA, an LDO using this technique offers typically 99% current efficiency, consuming less than 20 microamps. In addition, power supply rejection is maintained at higher levels over higher bandwidths – at 217Hz, a Smart Mirror regulator offers more than 80dB PSRR; at 10kHz the PSRR is still above 60dB.

In addition to multiple high-performance LDOs, other components of a very highly integrated PMIC would typically include high-efficiency buck converters with programmable output voltages, individually selectable LED drivers, programmable battery charger, audio drivers, and possibly other functions.

Buck converters improve the efficiency of the circuit and reduce thermal power dissipation. A DC-DC buck converter with integrated switches can provide a high current, low voltage supply to the baseband circuit, with synchronous and asynchronous modes ensuring efficiency across a wide range of current demands. Power efficiencies of more than 90% can be achieved (see **Figure 4**) compared to approximately 50% for an LDO in typical applications. Obviously, this has an impact on standby time and talk time of a mobile handset.

Typical application 1: portable media player

As more systems require multiple supply rails, the task for the designer is made more complicated, and finding a simple or easy to use power management solution can become a critical part of the overall system development cycle.

A basic PMIC might be suitable for low power systems such as a portable media player (see Figure 2), which typically includes both digital and analogue functions, and in systems using advanced microcontrollers or DSPs, which require separate core and peripheral supplies. In fact, the basic PMIC can be used anywhere where the system employs a single lithium

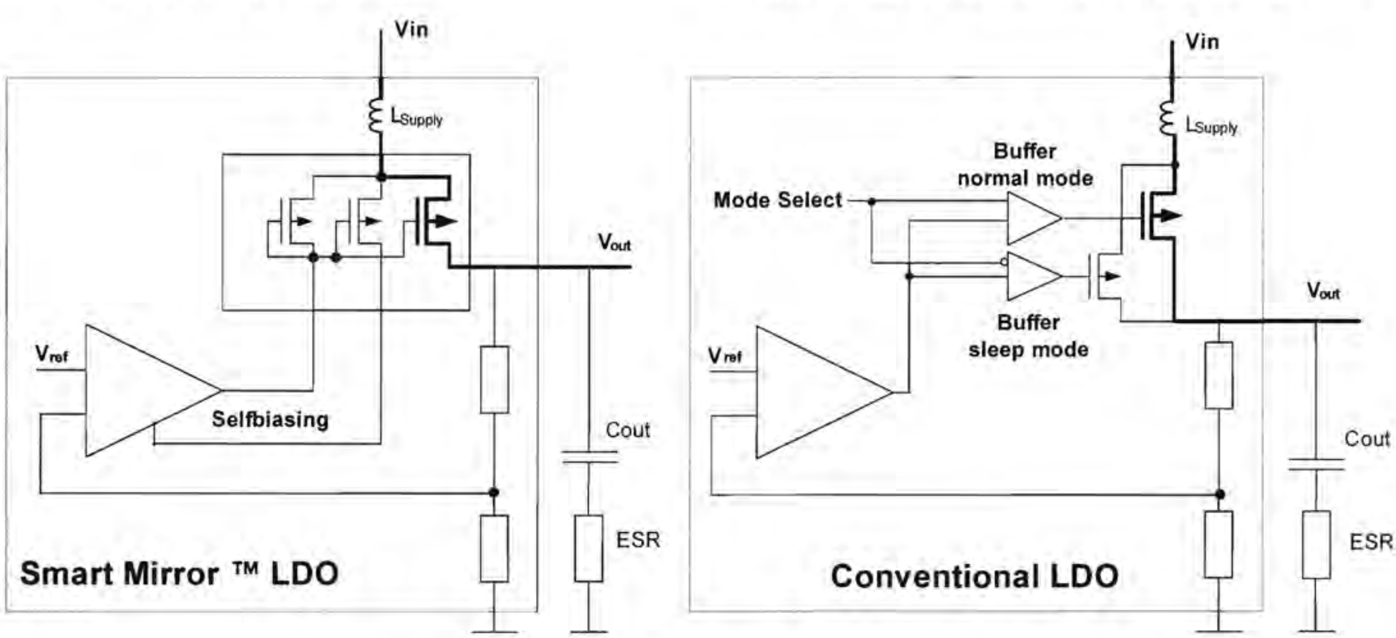
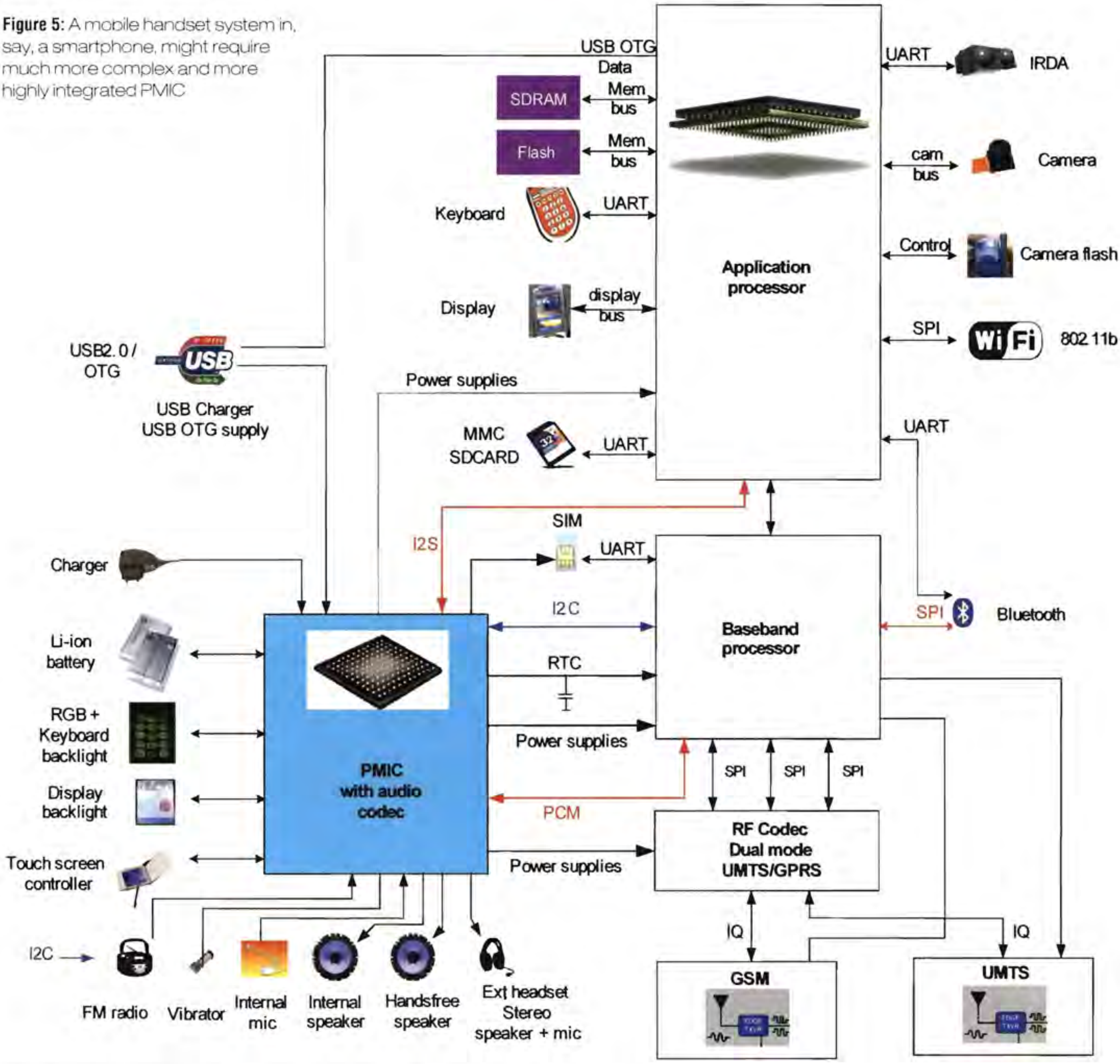


Figure 3: The Smart Mirror regulator compared to a conventional LDO. The former mirrors the output current demand back to the bias generator, which allows the bias to be reduced automatically as demand falls and gives dynamic quiescent current control

Figure 5: A mobile handset system in, say, a smartphone, might require much more complex and more highly integrated PMIC



battery supply or where a 3.3V supply is available, for example in many computer interfaces such as PCMCIA, SD, MMC, compact Flash and mini PCI.

By providing a basic system level power management solution, handling ON/OFF control, power sequencing and battery monitoring, the PMIC can enable the core of a more complex system. Additional functionality, such as extra regulators or battery charging, can be added using readily available standard components, allowing the designer to quickly configure a complete system.

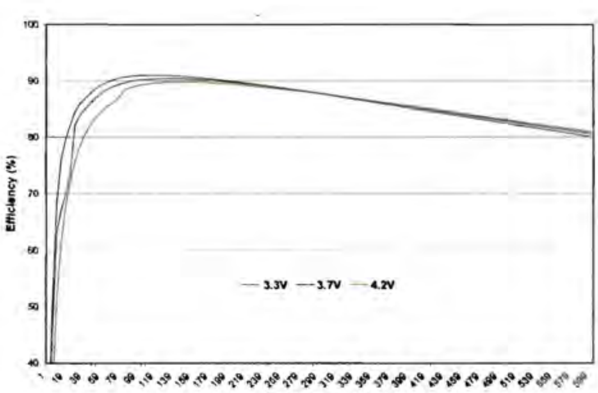


Figure 4 (Right): Power efficiencies of more than 90% can be achieved with a DC-DC buck converter

Typical application 2: mobile handset

PMICs with much higher levels of integration can offer all power management functions for an applications processor, such as the Intel PXA27x processor and communications processor within a mobile handset system (see **Figure 5**).

In this system, the PMIC enables power supply, battery management and sleep-mode functions to be effectively designed, and supports the wireless Intel SpeedStep technology to enable significant power savings by intelligently managing voltage and frequency changes.

The high level of integration in such a PMIC reduces overall system cost and size significantly when compared to an equivalent discrete solution. The applications processor controls all system related peripheral functions whereas the communication controller predominantly focuses on the radio communication part.

The application processor and the PMIC can be interconnected to build an efficient power-supply system with few additional components. A typical configuration will be set up for dynamic-voltage management when running applications as well as for supporting sleep mode whilst in standby.

Most handheld systems need to operate with lowest possible power consumption in order to keep the operating time high. The integrated PMIC can offer several operating modes such as power down, power on start-up, active and sleep as a single point solution, all in a small form factor and with minimum PCB area.

Integrated IC vs discrete components design

In this article, we have demonstrated some of the issues that need to be considered when looking at power management from a system-level approach rather than considering an array of discrete components. We have looked at how such an integrated IC can typically minimise quiescent current consumption in order not to provide significant extra drain on the power source, and looked at a couple of typical applications for a completely integrated PMIC – from very basic to fairly complex.

Power management is one of those issues that are often only considered mid-way through the product development phase. But by considering the overall system and the power needs, the system-level PMIC is a strong alternative to following the full SoC (system on chip) route to developing the complete system, enabling functionality that is flexible enough to be used in many different applications, plus giving designers the freedom to easily add additional functions as required.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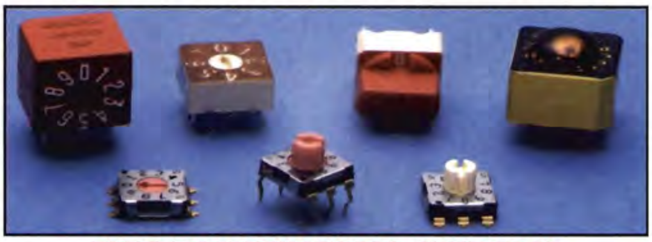


Using Supercapacitors

to Solve LED Flash Power Issues for High Resolution Camera Phones

Pierre Mars, VP of Applications Engineering for CAP-XX based in Sydney, Australia, here presents two solutions that can provide high LED flash currents without straining a battery

Greater than 2M pixel camera phones require a high intensity flash in medium to low light conditions to ensure good pictures. However, the battery presents the system limitation, as it cannot deliver the high current pulse required for adequate LED light output for high-resolution images.

A traditional LED Flash driver uses a boost converter in current controlled mode as shown in **Figure 1**. As an example, consider the case of driving 1A each through two LEDs in parallel, such as the Lumileds Luxeon PWF1, which would generate approximately 20 lux at 2m using a high uniformity optic. The output voltage at the boost converter = LED forward voltage + voltage across current sense resistor. The maximum forward voltage = 4.8V and, assuming 200mV across the current sense resistor, then the boost converter output voltage = 5V. Assuming the camera phone battery voltage = 3.3V under load, and the boost converter is 85% efficient, the battery current in this case would = 5V/3.3V/85% x 2A = 3.6A, which exceeds the typical phone battery's capability.

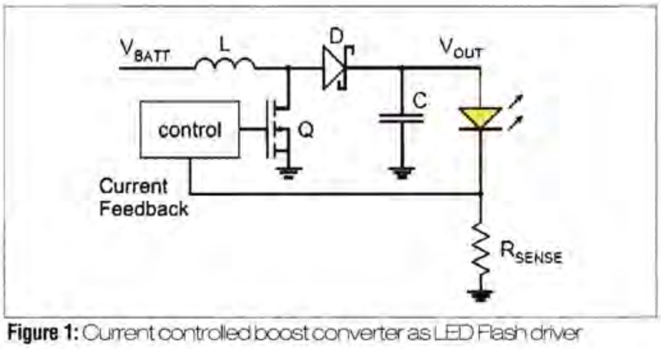


Figure 1: Current controlled boost converter as LED Flash driver

The alternative solution is to use a xenon flash, but this requires: 1) a storage capacitor that is very bulky for mobile phone form-factors and 2) high voltage, resulting in circuit and safety issues. Also, with LED flash, the same LED circuit can be used at lower current for the video capture/torch function.

To overcome the power limitation, some camera phone suppliers have used long flash exposure times to compensate for the lack of light, thereby increasing the total light energy, but this results in blurry photos.

Design solutions

There are two solutions, among others, that provide enough LED flash power to eliminate dark and blurry photos from a lack of light. CAP-XX supercapacitors, with their high C (1F or more) and low ESR (< 100mΩ) are able to support the battery and provide the pulse power required by the LED, while their thin (1 to 3mm), prismatic form-factor works in a space-constrained application such as a camera phone. Solution 1 places a supercapacitor at the output of a buck-boost converter while solution 2 uses a supercapacitor in series with the battery.

Solution 1: Supercapacitor at the output of a boost converter or charge pump

Figure 2 shows a block diagram of the CAP-XX solution, while **Figure 3** shows a circuit implementation. A small, low-cost, current-limited charge pump pre-charges the supercapacitor to ~5.5V. Once the supercapacitor is charged, the current switch is enabled to deliver a high current flash pulse, with the energy and power coming from the supercapacitor rather the battery and charge pump. During the flash pulse, the charge pump can either be enabled or disabled. The charge pump is current limited to ~300mA. In Torch mode, the charge pump is left enabled and the battery and charge pump can deliver a constant current which is less than the charge pump current limit.

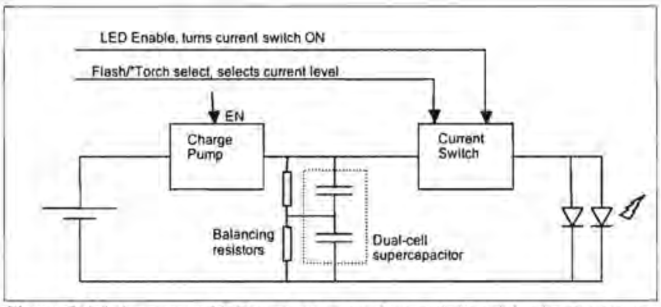


Figure 2: High power LED supercapacitor solution block diagram

For the reference design, CAP-XX chose the highest power bright LEDs, Lumileds LXCL-PWF1, which can handle a peak pulse current of 1A for < 200ms. We drove 4 x PWF1, at 900mA each. The total LED current of 3.6A was limited by the Micrel

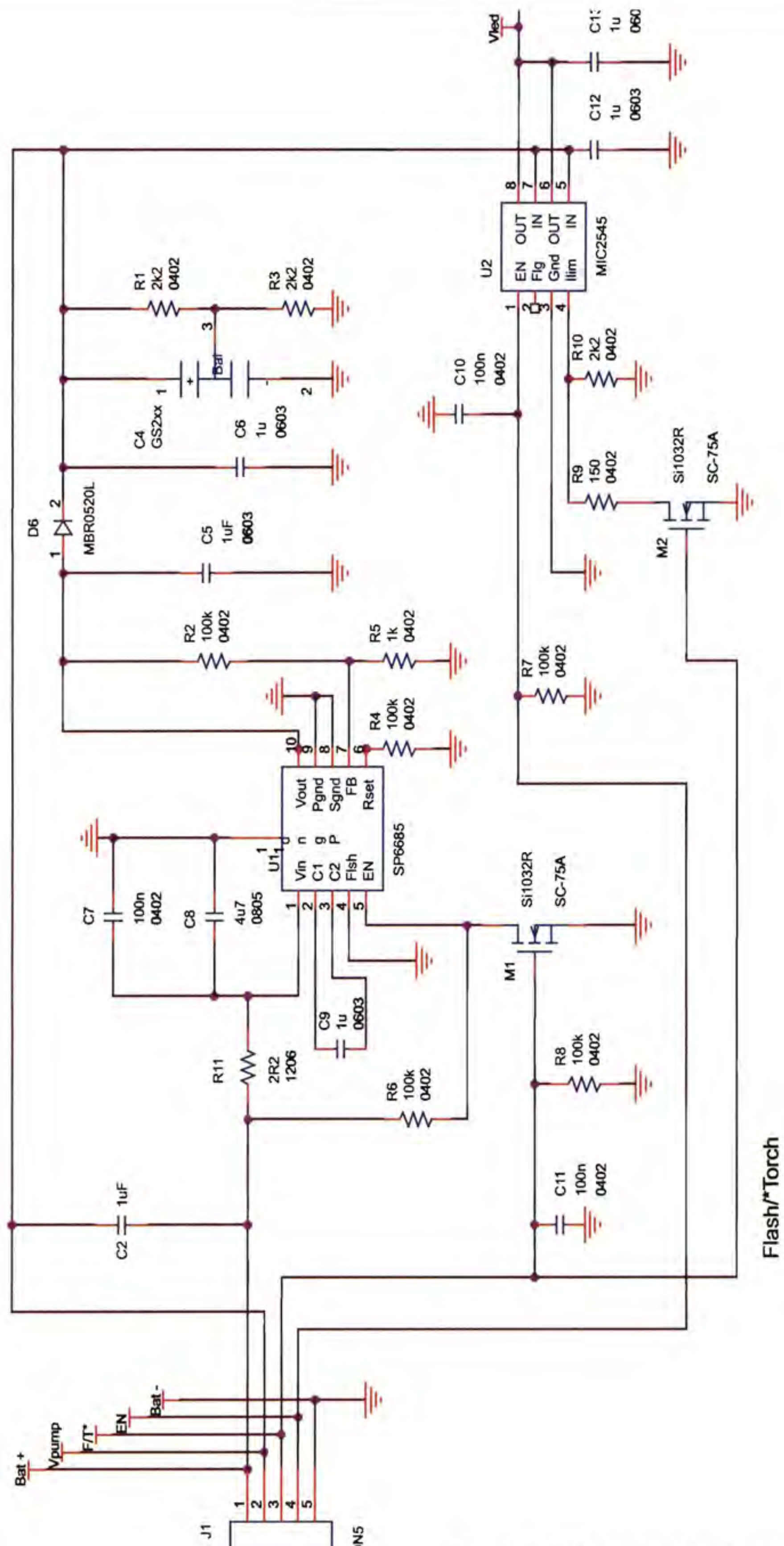


Figure 3: CAP-XX supercapacitor solution circuit implementation

Figure 4: Photos in low light with normal phone (left) and phone modified with CAP-XX supercapacitor-based solution (right)

MIC2545 current switch, which was chosen for its current capacity and relatively small size.

The following circuit description refers to Figure 3. When power is first applied, the Flash/Torch select must be low or floating so that U1 (SP6685 charge pump) is enabled. This turns M1 is OFF and U1 pin 5 (EN) is pulled high through R6. Depending on the size of the supercapacitor, you will need to wait 10-15s before the supercapacitor is fully charged from 0V. There is a high inrush current when the supercapacitor is at 0V, since until it is charged to a voltage ≥ Vin, it looks like a short circuit on the output of the charge pump. R11 was added to the circuit to limit the initial inrush current to < 750mA.

Note that the SP6685 is only used to charge the supercapacitor so it is always in its Torch mode (pin 4, Flsh connected to Gnd).

Once the supercapacitor has been charged, select Flash or Torch mode. When this signal is Hi (Flash mode), M2 is ON, which sets the current setting resistor for U2 (MIC2545) = R9//R10. This sets the LED Flash current.

The LEDs are on while the Enable input (U2 pin1) is held Hi. This turns on U2. Due to the very large capacitance of the supercapacitor, the flash pulse discharges the supercapacitor only a relatively small amount, typically < 1V. This means the time to recharge the supercapacitor between flash photos is short, typically ~2s. This is shorter than time the LEDs require between flashes to cool down. **Figure 8** shows the supercapacitor voltage, battery current and LED current during and after a flash pulse. D6 was added to prevent the supercapacitor discharging into the battery through U1 when U1 is disabled.

The supercapacitor C and ESR are selected as follows:

Total LED current (I_{LED}) = 3.6A for a 150ms flash pulse, denoted by PW_{FLASH}.

- From the Lumileds datasheet, at 0.9A nominal LED forward-voltage = 3.75V, allow 4.2V
- From the Micrel datasheet, the R_{dson} resistance < 50mΩ, so the voltage drop across the MIC2545 current switch < 180mV
- Therefore, the minimum voltage at the supercapacitor at the end of the flash pulse must be ≥ 4.2V + 0.18V = 4.38V ≥ 4.4V
- Vout (charge pump voltage) is set to 5.3V, therefore, the total voltage drop allowed at the supercapacitor is Vd = 5.3V – 4.4V = 0.9V
- Supercapacitor voltage drop, $Vd = I_{LED} \times (ESR + PW_{FLASH}/C)$
- Or, re-arranging terms, $C \geq I_{LED} \times PW_{FLASH} / (Vd - I_{LED} \times ESR)$
- In the above example, C ≥ 2A x 0.15s/(0.9V – 2A x ESR)
- Assume a supercapacitor ESR = 100mW, then C ≥ 2A x 0.15s/(0.9V – 2A x 0.1W) = 0.43F. Select a supercapacitor with ≈ $^1/_2$ the assumed ESR to allow for ageing over life.

CAP-XX GS206 (0.55F, 50mW) meets the requirements. Note that two supercapacitor cells are used in the circuit to achieve the necessary voltage rating of 5.5V maximum voltage. 100mΩ is a good starting guess for ESR. You may need to iterate between C and ESR to find a suitable supercapacitor. Set the charge pump output voltage to the lowest possible, while still having sufficient headroom for the solution.

CAP-XX supercapacitors have very low leakage current, typically < 1μA. However, when two cells are used in series, a cell balancing circuit is required to ensure that any difference leakage current between the two cells does not cause the midpoint voltage to drift such that one of the two cells goes over-voltage. The simplest cell balancing circuit is a pair of balancing resistors, which are shown in Figures 2 and 3. For a cell phone camera flash implementation, where the supercapacitor will be charged to > 5V prior to a flash pulse, a suitable value would be 22kΩ resistors. This would result in a total leakage + balancing circuit current of ~80μA if the supercapacitor were normally held at better voltage (~3.6V). CAP-XX recognises that this may be too high for good battery standby times. The possible remedies for this are: 1) disable the charge pump when the phone is not in camera mode – this means there is no supercapacitor + balancing circuit leakage drain while the phone is in standby; 2) use of an active balancing circuit using a high impedance low current op amp – a reference design is available from CAP-XX with total current < 2μA.

Charge pump selection is not critical. We selected the SP6685 for its small size. Note that the soft start function of most charge pumps will not properly handle a supercapacitor at the output, since a discharged supercapacitor will look like a short circuit for several seconds until the supercapacitor voltage approaches the charge pump output voltage. A simple solution is to add a current limit resistor at the input to the charge pump (R11 in Figure 3).

Results

CAP-XX was able to place two supercapacitor cells, the circuit of Figure 3 and four replacement LEDs in a leading brand camera phone and put it back together with no changes in external appearance. **Figure 4** shows photos taken using the unmodified and CAP-XX-modified phone. The unmodified phone delivered 1W of flash power for 160ms, while the modified phone delivered 15W of flash power for 160ms.

Figure 5 shows the battery current, LED current and supercapacitor voltage during a Flash pulse and supercapacitor re-charge after the pulse. Note that battery current never exceeds 300mA even though the flash pulse is 4A. The supercapacitor provides the 3.7A difference.

Solution 2: Supercapacitor in series with the battery

Figure 6 shows the solution 2 block diagram. The supercapacitor is in series with the positive terminal of the battery. The advantages of this configuration are:

- Only a single cell supercapacitor is required
- This is ~half the volume of the dual cell supercapacitor required for solution 1 and is lower cost
- Since the supercapacitor +Ve terminal voltage is always ≥ than the battery voltage, there is no supercapacitor inrush current
- Since there is only a single cell, no balancing circuit is needed

The disadvantage of this configuration is:

- The battery current = LED flash current, unlike solution 1 where battery current = supercap charge current only (and can = 0 during LED Flash).

This configuration enables you to achieve much higher LED current for a given battery current than would be possible using a "standard" topology of a current controlled boost converter or charge pump to directly drive the Flash LEDs. Consider a charge pump driving an LED at 70% efficiency with the LED current = 1A. Assume the LED maximum forward voltage = 4.8V and the battery voltage under load = 3.3V.

Then, without the supercapacitor, battery current = 1A x 4.8V/3.3V /70% = 2A which is too much for the battery to comfortably deliver and still power the rest of the phone. With solution 2, battery current is only 1A or a 100% improvement.

Refer to **Figure 7**, a circuit implementation for solution 2. In the same manner as for solution 1, when power is first applied, the Flash/Torch select must be low or floating so that U1 is enabled. Depending on the size of the supercapacitor, you will need to wait 3-6s before the supercapacitor is fully charged from the battery voltage (0V across the supercapacitor) to the starting value of Vled (~5.1V or 1.2V across the supercapacitor). Peak battery current is limited to ~300mA during charging. This reduces quickly as the supercapacitor charges. The charge pump behaviour in solution 2 is different to solution 1 because Vout ≥ Vin always and the charge pump never sees the supercapacitor as a short circuit. Like solution 1, the charge pump, U1, is only used to charge the supercapacitor so it is always in its Torch mode (pin 4, Flsh connected to Gnd).

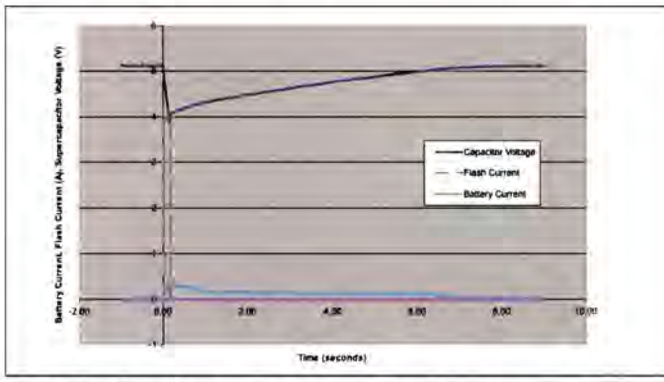


Figure 5: Solution 1 battery, LED Flash current, supercapacitor voltage during and after a flash pulse

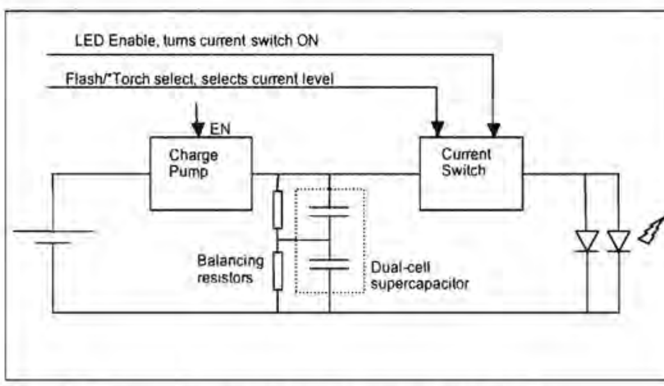


Figure 6: The configuration block diagram of solution 2

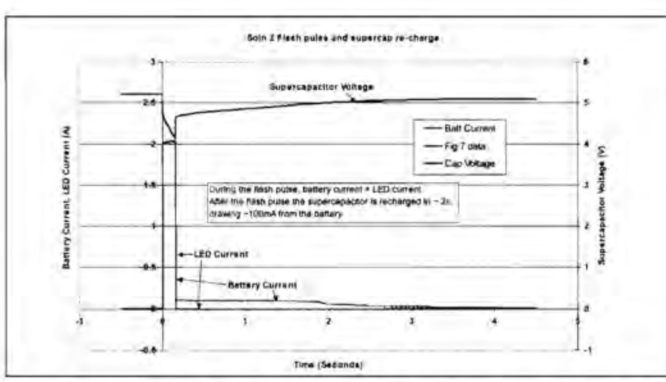


Figure 8: Battery, LED Flash current, supercapacitor voltage during and after a flash pulse

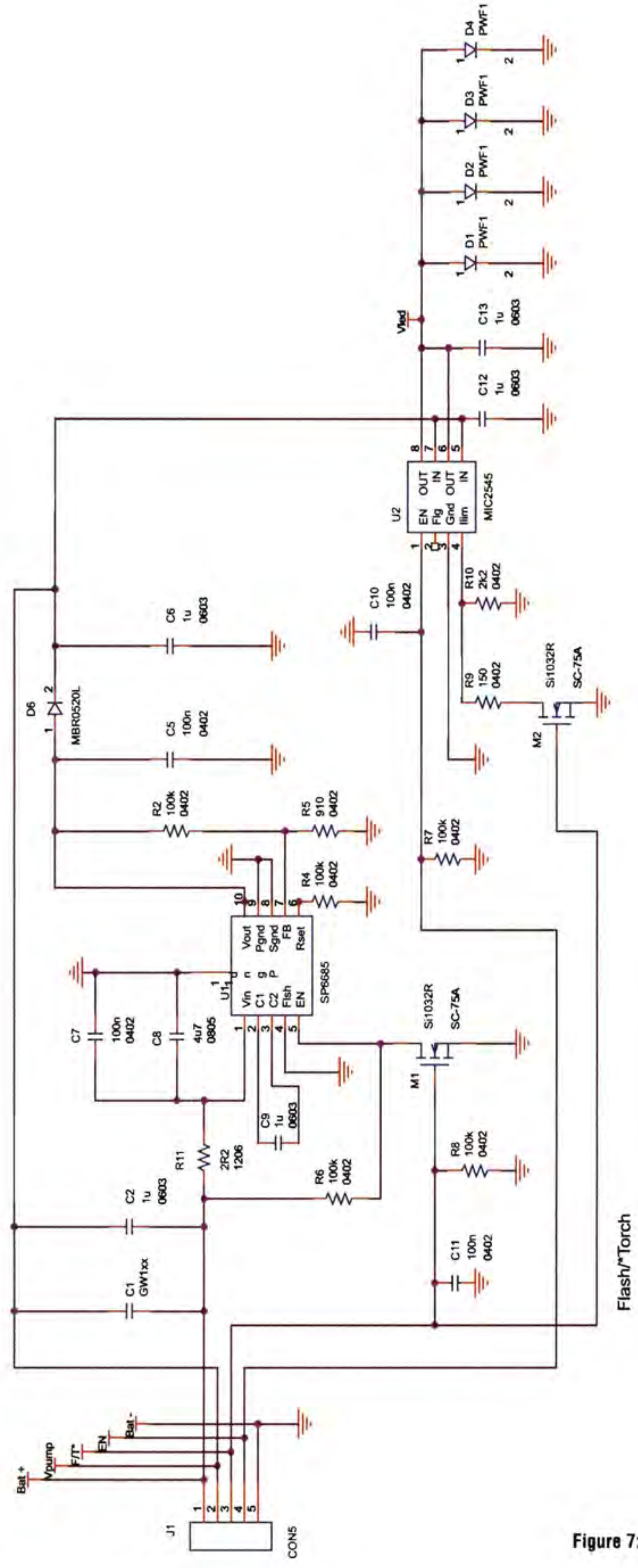


Figure 7: Solution 2 circuit implementation

Once the supercapacitor has been charged, select Flash or Torch mode. When this signal is Hi (Flash mode), M2 is ON, which sets the current setting resistor for U2 (MIC2545) = R9//R10 = 120W//1150W ≈ 110W. This sets the LED current ≈ 2A. Flash/Torch Hi also turns ON M1, which disables the charge pump (pulls U1/pin5 Lo). This is done in solution 2, since the battery is already supplying the LED current through the supercapacitor. Leaving the charge pump enabled would cause the battery to provide > LED current with efficiency < 100%.

As in solution 1, the flash pulse discharges the supercapacitor only a relatively small amount, so the time to recharge the supercapacitor between flash photos is short, typically shorter than the time the LEDs require between flashes to cool down (~2s). Figure 8 shows the supercapacitor voltage, battery current and LED current during a flash pulse and immediately after the pulse, when the battery supplies charging current to the supercapacitor in preparation for the next flash photo. Supercapacitor C and ESR are selected as follows:

- Drive 1 x Lumileds LXCL-PWF1 at 0.8A for a 250ms flash pulse.
- From the Lumileds datasheet, at 0.8A the forward voltage = 3.7V, allow 4.1V
- From the Micrel datasheet, the R_{dson} resistance < 50mW, so the voltage drop across the MIC2545 current switch < 40mV
- Therefore, the minimum voltage at the supercapacitor at the end of the flash pulse = 4.1V + 0.04V = 4.14V
- Vout (charge pump voltage) is set to 5.2V, therefore, the total voltage drop allowed at the supercapacitor, Vd = 5.2V – 4.14V = 1.06V
- Assume a supercap ESR = 50mW, therefore C ≥ 0.8A x 0.25s/(1.06V – 0.8A x 0.05W) = 0.196F. Choose GW109, C = 250mF, ESR = 35mW. Allow for ESR to double, so substitute 70mΩ and 250mF for ESR and C in the expression for Vd and check the voltage drop is < 1.06V:
  Vd = 0.8A x (70mΩ + 0.25s/0.25F) = 0.8 x 1.07 = 0.86 < 1.06V
- Therefore, choose GW109 (250mF, 35V)

Load Transient Boost Applied to Multiphase DC-DC Converters

Osvaldo Zambetti and **Alessandro Zafarana** from STMicroelectronics in Italy are presenting non-linear control for improving the transient controller performances without changing total system efficiency of microprocessors

Recently, there has been a huge increase of current rate drawn by new Intel and AMD processors. Multimedia applications, dual core architecture and electrical performances of 65nm node make it more and more difficult to control the core voltage during load transients.

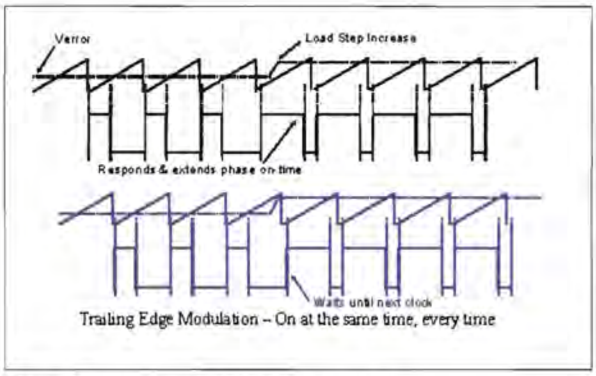


Figure 1: Trailing edge PWM modulator

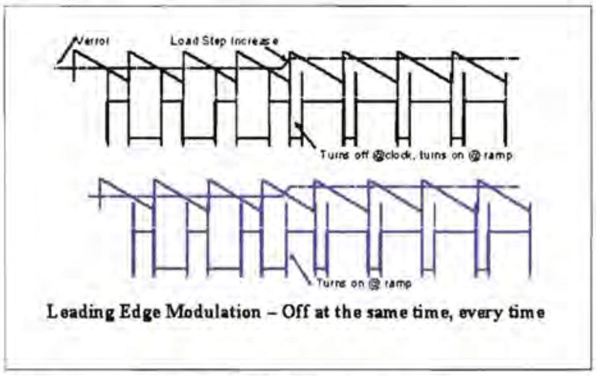


Figure 2: Leading edge PWM modulator

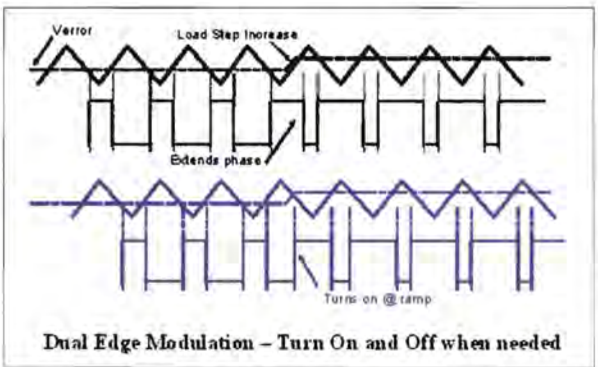


Figure 3: Dual-edge PWM modulator

High-performance microprocessors require a low voltage, high-current power supply with fast transient response. Therefore, interleaved multi-phase synchronous buck converters have gained popularity as the VRM for these microprocessors because they allow faster system control in small signal condition, reduce output voltage ripple and decrease cost of input and output capacitors. However, interleaving phase shift during large and steep load transients can negatively affect output voltage.

System stability and small signal behaviour are studied on the basis of ac variables related to output power; state variables for the system are total current flowing through the equivalent inductor and voltage drop across the output capacitor. It is possible to show that a multi-phase interleaving system is totally characterised by such variables and it is equivalent to only one single phase DC-DC converter, where the coil is substituted by the parallel of all inductors (equivalent inductor), and the equivalent switching frequency is N times the single phase switching frequency (where N is the number of phases).

This model demonstrates why it is possible to implement a faster control system with much higher GBWP than a single phase system. Of course, this helps to keep the output voltage stable and well regulated even during load transients. Unfortunately, recent electrical CPU specifications increase the load transient rate to 1200A/µs (100A with 50ns) making it almost impossible for the control system to respond on time to such steep variations. The result is a cost increase of the output filter capacitors above all mid-frequency range capacitors such as the 22µF MLCC capacitors.

Action delay

Controller architectures used today are typically either Trailing Edge or Leading Edge. Each of these architectures has advantages and disadvantages. Controllers using the Trailing Edge control architecture (**Figure 1**) turn ON at the beginning of each clock cycle. The controller is able to respond to any transient event that occurs while the controller is on, however it must wait until the next clock cycle to respond if a transient occurs while it is off. Controllers using the Leading Edge architecture (**Figure 2**) turn OFF at the clock cycle and can respond to transients that occur while it is off, but must wait for the next clock cycle to respond if the transient occurs while it is on. In both architectures, a latch that is typically placed at the output of the PWM comparator creates a one-cycle delay when responding to a transient event.

The dual-edge modulator (**Figure 3**) is not constrained by clock cycles when determining when to turn on or off. The signal to turn on is determined by the error signal.

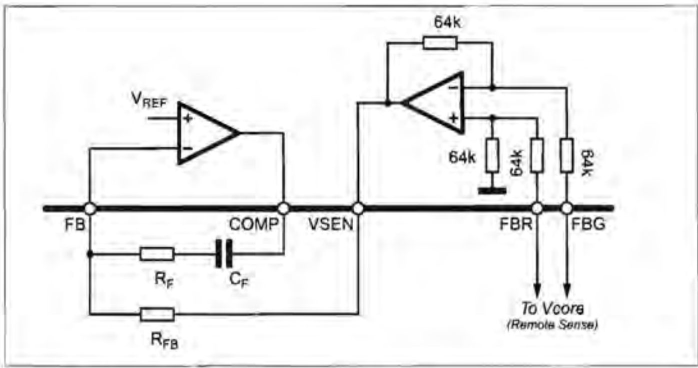


Figure 4: Full differential CPU remote sense

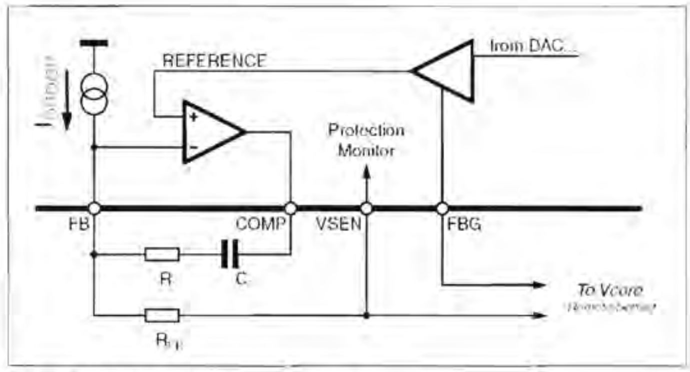


Figure 5: CPU ground remote sense

Similarly, the error signal tells the controller when to turn off. This architecture, coupled with fast output feedback, allows all phases to simultaneously respond to a transient event. While the basic dual-edge modulator will enable system improvements, it is also important to address other pieces of the architecture that introduce delays in the system response and hinder the ideal instantaneous response. If we consider "action delay" as the time a controller takes between realising that a load transient occurred and commanding the turn on of all high-side power Mosfets; we recognise that there are at least the following contributions:

1. Remote sense is used to sense in a full differential way the voltage across the CPU. It is implemented with an operational amplifier that introduces a delay T_{rb} that is $1/GBWP_{rb}$ (T_{rb}=100ns) where $GBWP_{rb}$ is around 10MHz. The remote sense amplifier must be moved away from the feedback path. This can be done by simply sensing only the remote core ground, thus losing high frequency CMRR.

Figure 4 shows traditional remote buffer connection. Here the remote buffer introduces a delay T_{rb} because it is along the feedback path.

In **Figure 5** the remote sense is implemented outside the feedback path; so T_{rb}=0.

2. Dual-edge implementations that utilise latches throttle the system response and limit the benefits that would otherwise be seen with pure dual-edge architecture. To achieve the full benefits of dual-edge architecture, the clocks and latches must be eliminated from the system. However, cost driven solutions are dominated by controllers that embed power Mosfet drivers. These drivers produce noise at every switching edge, reducing noise immunity of the analogue front-end with high risk of jitter conditions. There are several methods to limit substrate noise (by accurate IC design, noise insulated silicon components, etc). Two of these methods have a large PWM ramp and latched PWM pulses.

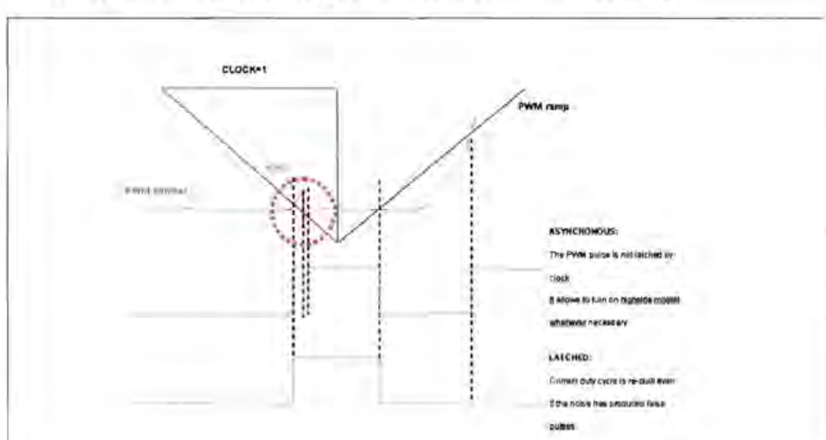
The latched dual-edge PWM modulator has great noise immunity characteristics, but it produces a long action delay T_a proportional to the switching period. It also depends on the instant where a load transient occurs.

In **Figure 7** you can see that in the latched dual-edge PWM modulator, the worst action delay is given when the load transient happens during low-side power Mosfets turning on. An action delay of about T/2 is possible, where T is the switching period. The dual-edge modulator without latch greatly improves the action delay canceling T_a.

3. The error amplifier local loop must be pulled away from the steep output voltage drop when a load transient occurs. In this way the control loop can fly over the PWM ramps forcing all PWM pulses at "1" to turn on high-side power Mosfets at the same time. It is required that the control voltage is saturated. To produce the error amplifier saturation, a capacitor C_p is inserted into the feedback network as shown in **Figure 8**. C_p gives a derivative component to control voltage (COMP). The big C_p capacitor makes the saturation of COMP faster and easier above PWM ramps, but it makes the system unstable or it may produce jitter (therefore, enlarging output voltage ripple requires more output capacitors). If C_p is small the system is stable but there is the risk that COMP voltage may not rise high enough above the PWM ramp.

Anyway, the time needed to push the control

Figure 6: Dual-edge: noise immunity of latched and asynchronous PWM modulator



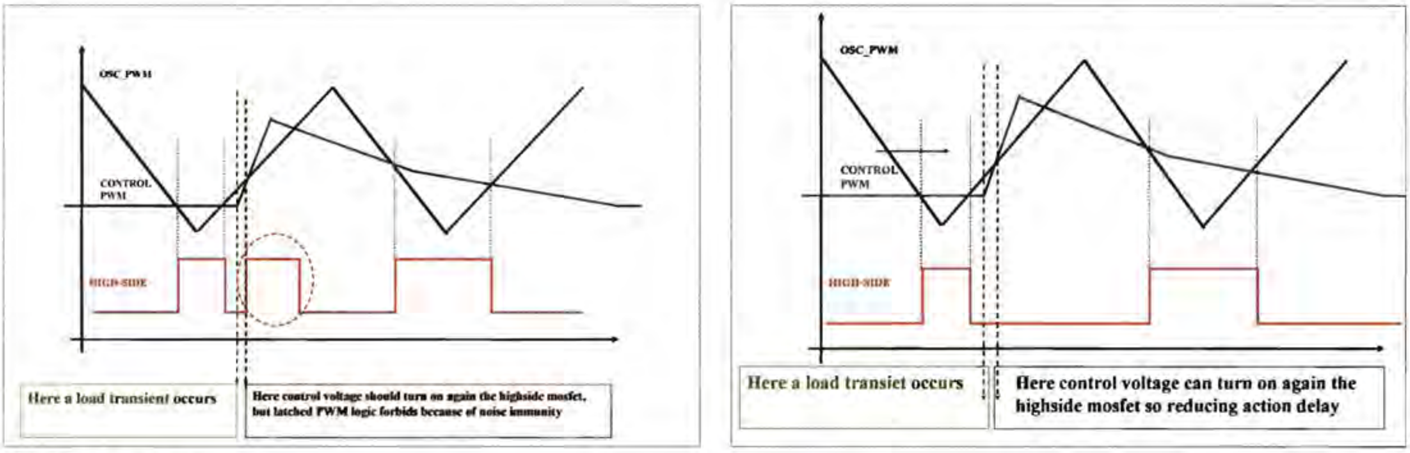


Figure 7: Dual-edge PWM modulator: action delay

voltage above the PWM ramp depends on how tall the PWM ramp is and how much is the error amplifier slew rate (and GBWP): usually slew rate is 10V/μs and the PWM ramp is 2V. We have T_{sr}=200ns delay from slew rate. Usually slew rate (and GBWP) is very difficult to guarantee in a datasheet because it can spread significantly. Such spread makes this part of action delay unpredictable. C_p value must be chosen considering that even in the worst slew rate condition (even not known), the COMP voltage can rise above the PWM ramp. As can be seen in **Figure 9**, an increase of C_p creates jitter (it increases output voltage ripple), thus creating system instability. The steady state condition is recovered after much time has passed since the load transient.

There is also a contradiction about the C_p choice: it should be chosen, taking into account that even in worst slew rate condition the COMP voltage can rise above PWM ramp, but the C_p value also sets the amount of energy transferred after the load transient. The overestimate of C_p brings too much energy to the output, thus producing a large voltage ring-back and an increase in recovery time for the steady state as shown by the simulations reported in Figure 9. We will show that a new class of non-linear control response will solve this issue, cancelling delay T_{sr} and getting a large improvement of the box-shaped core voltage response.

4. Power drivers are the hard transducers of the controller decisions. It is crucial that power drivers run the command with minimum delay. This delay is the sum of time T_1 between the turning off of low-side power Mosfets turning on of high-side power Mosfets and the time T_2 needed to transfer the logic command to the driver itself.

Controllers having embedded drivers usually minimise this delay because they do not have T_2. This delay comes from the quite low speed of digital buffers inside the controller and the high wire capacitance between controller and external driver. Usually digital buffers of commercial controllers have a saturated driving resistance of about 1kΩ, while the trace wire of about 5" shows a capacitance of about 100pF, thus we can conclude that T_2~ 100pF x 1kΩ = 100ns.

Delay T1 is the sum of driver internal delay and the T_{fall} low-side and T_{rise} high-side. T_2 delay can be 100ns and T_1 (**Figure 10**) can be 100ns as well.

Figure 8: COMP saturation during load transient

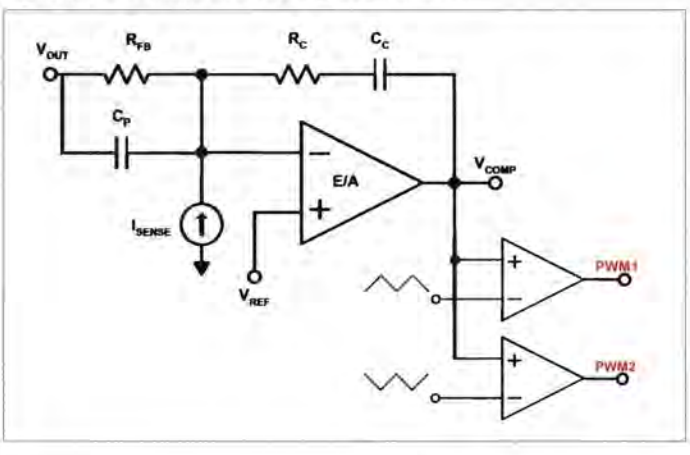
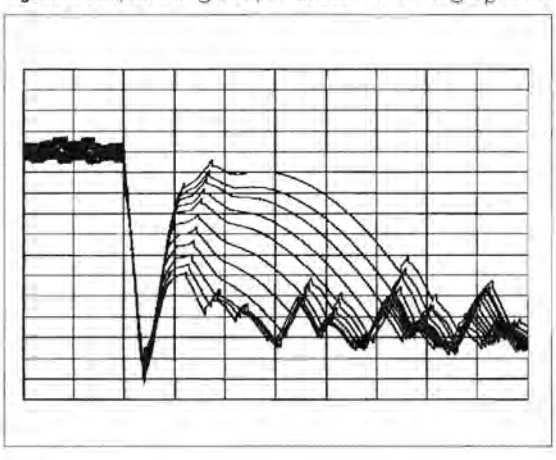


Figure 9: Output voltage response with increasing C_p value



Collecting all the contributions, we can compare the most significant values:

Parameter	Symbol	Value [ns]
Remote sense	T_{rb}	~100ns
Dual-edge PWM	T_a	~T/2 (if latched)
E/A slew	T_{sr}	~200ns
External driver	T_2	~100ns
T_{fall} LS, T_{rise} HS	T_1	~100ns
Action delay	AD	~1.5μs with T=2μs

LTB

The action delay has several contributions: T_{rb}, T_a, T_{sr}, T_1+T_2. We saw how to minimise all these contributions with the exception of T_{sr}. We described also all the concerns related to pure dual edge modulator without latch. Load Transient Boost (LTB) solves all these issues and cancels T_{sr}.

LTB uses a "load transient sensor", which is a circuit that gives a glitch when the dv/dt exceeds an internal threshold. The sensibility of the circuit can be set by changing the external network at the LTB pin. The sensor recognises both applied and released load transient. When a load transient occurs (applied load), a voltage (red) at the output of LOAD APPLY PWM RAMP is set to the lower basement of dual edge PWM ramps; from that value a ramp is initiated with a slope m.

When the load is released, a voltage (blue) at the output of LOAD RELEASE PWM RAMP is set to the upper basement of dual edge PWM ramps; from that value a ramp is initiated with a slope -m (**Figure 11**). Referring to **Figure 12**, each LOAD APPLY\RELEASE PWM RAMP is then compared to control voltage (COMP) producing a proper PWM pulse whose length represents the correct amount of energy needed by the system. As a consequence, the error amplifier will continue to work in "small signal" condition. For load release, the pulse will turn off all the power Mosfets, particularly the low-side power Mosfets. This greatly improves the output voltage response.

For applied load the pulse named "PWMBOOST" is or-ed with each PWM pulse for every phase. The "or" operation cancels the interleaving phase shift and transfers the correct amount of energy commanded by the error amplifier. The "LTB BRAKE" is a digital filter that allows the closest interleaved PWM pulse to be skipped to PWMBOOST. This filter greatly improves the output voltage response that really looks as a box waveform.

The action delay related to the LTB technology is a few ns: it acts directly in a digital way, resetting the interleaved phase shift. The delay is caused mainly by the sensor comparator (around 10ns).

So, LTB technology reduces T_{sr} from 100ns to 10ns and, above all, makes the system insensitive to a parameter spread that is not guaranteed. It also makes the system more "linear", as the energy transferred by LTB is commanded directly by an error amplifier that continues to work like an operational amplifier and not as a comparator pulled away by C_p capacitor.

The action delay we get now is summarised in the following table:

Parameter	Symbol	Value [ns]
Remote sense	T_{rb}	~0ns
Dual-edge PWM	T_a	~0ns
E/A slew	T_{sr}	~10ns
External driver	T_2	~0ns
T_{fall} LS, T_{rise} HS	T_1	~100ns
Action delay	AD	~110ns

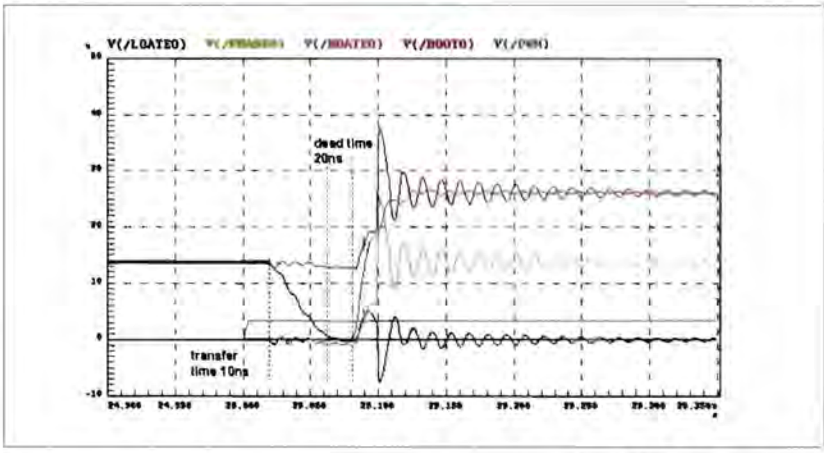


Figure 10: Driver command delay to turn on the high-side power Mosfet

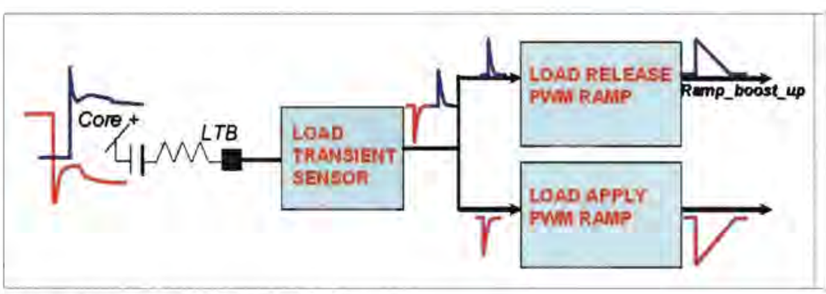


Figure 11: Load Transient Boost scheme

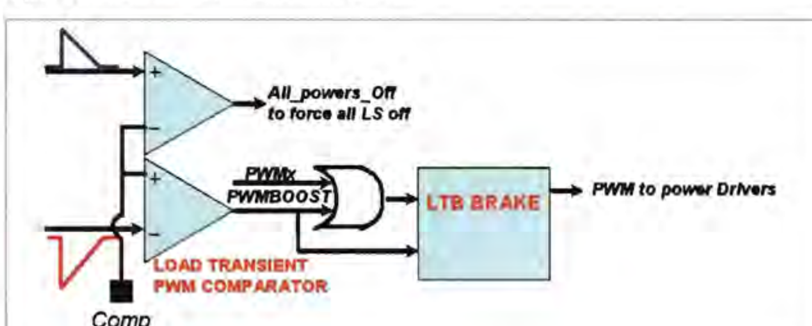


Figure 12: Load Transient Boost commands

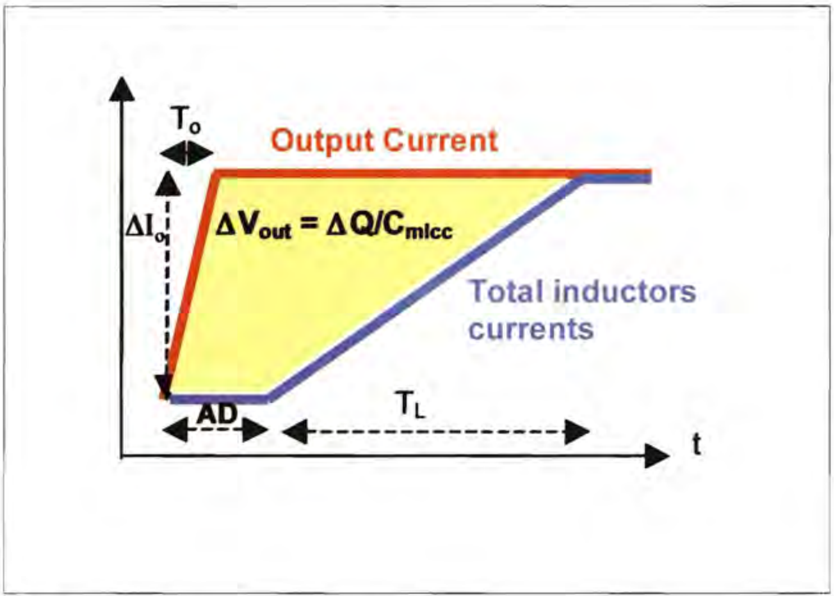


Figure 13: Total load transient charge calculation

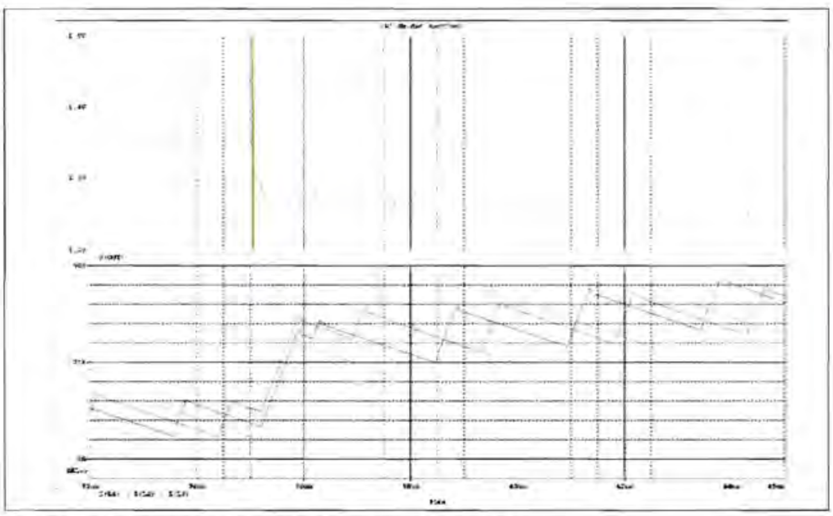


Figure 14: Simulation with applied load step 50A, 50ns

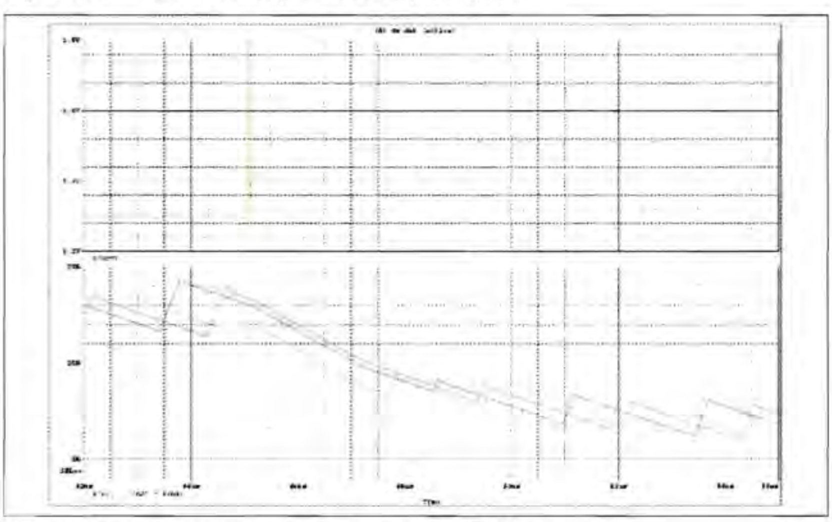


Figure 15: Simulation with released load step 50A, 50ns

When all high-side power Mosfets are turned on to increase the inductors current, the whole charge is brought to sustain the output voltage in just AD time; this means that only mlcc capacitors (usually 90%) can bring up the output voltage because the total mlcc capacitors have an equivalent esr much less than the total bulk capacitors (i.e. 15 x 10mF mlcc have a total esr of 0.16mΩ, while 4 x 560μF bulk have a total esr of 1.5mΩ the ratio is 1 to 10, so 90% of needed charge is delivered by mlcc capacitors).

Figure 13 shows that from AD, it is possible to calculate how many mlcc capacitors are necessary to keep the output voltage within a given drop ΔV_{out} after a load transient ΔI_o with a time length T_o. After action delay, the inductor currents grow up in T_L, where:

$$T_L = (L \times \Delta I_o) / [N \times (V_{in} - V_o)] \quad (1)$$

L = inductance value

N = number of phases

Vin = multiphase input voltage

Vo = output voltage

From a geometrical calculation, we have:

$$\Delta Q = AD \times \Delta I_o + 0.5 \times \Delta I_o \times T_L - 0.5 \times T_o \times \Delta I_o \quad (2)$$

90% of this charge is sustained by mlcc, while 10% is given by bulk capacitors; so we get:

$$C_{mlcc} = 0.9 \times \Delta Q / \Delta V_{out} \quad (3)$$

The action delay and, thus, the number of mlcc capacitors, is very important because it is directly related to cost.

Simulations and experimental results

The simulation results are based on the following bill of material and specifications:

- BTX motherboard model with Intel socket 775
- N=3 phase interleaved controller with embedded drivers and remote sense out of feedback path
- switching frequency at 450kHz
- load transient between 15A and 65A (ΔI_o =50A) within T_o =50ns
- inductor L=200nH with 0.5mΩ DCR
- bulk capacitor Oscon 4 x 560μF, esr 6mΩ
- mlcc capacitor 15 x 10μF and 3 x 22μF
- system output resistance (droop) R_d = 1mΩ
- highside 1 x STD55NH30LL per phase
- lowside 1 x STD95NH30LL per phase
- Input voltage V_{in} = 12V
- Output voltage V_o=1.4V
- Output voltage ripple <10mV p-p

The simulation results show very well how the interleaved phase shift is cancelled. When the interleaved phase shift is zeroed the output voltage is sustained by mlcc capacitor and above all by 22μF mlcc capacitors. As can be observed in **Figure 14**, to get rid of any ring-back or excess of transferred energy, the LTB brake mechanism reduces the current flowing into one of the three inductors; so the output voltage features a real output impedance (box waveform). The slight undershoot after 4-5µs is the time needed for the control loop to recover the steady state condition; it is related both to the total GBWP of the system and to current sharing loop gain. At this slow frequency the system is also sensitive to the number of bulk capacitors.

If we use equation (1, 2, 3) with the electrical specifications reported earlier, we have:

$\Delta V_{out} = R_d \times \Delta I_o = 1m\Omega \times 50A = 50mV$

$T_L = 314ns$

$\Delta Q = 12\mu C$

$C_{mIcc} = 216\mu F$

This equivalent capacitor corresponds to 15 x 10µF and 3 x 22µF.

At load release, the LTB pulse turns off all power Mosfets. This feature reduces the extra-charge of output bulk capacitors because the slope of inductor currents are greatly increased from V_o/L to $(V_o+V_d)/L$ where V_d is the voltage drop of the body-drain diode of low-side power Mosfets. This feature also avoids that negative current flows into inductors, thus cancelling negative ring-back of the output voltage.

The experimental measures have been collected using the first commercial product implementing LTB technology and now available on the market. STMicroelectronics's L6713A features for the first time all the mechanisms to reduce the action delay: remote sense out of feedback path, asynchronous dual-edge modulator, LTB technology and embedded drivers. The device can be used with two or three interleaved phases and is suitable for Intel VR10.x, Intel VR11 and AMD K8-F processors.

The experimental results are related to the same bill of materials and same specifications of the simulated results.

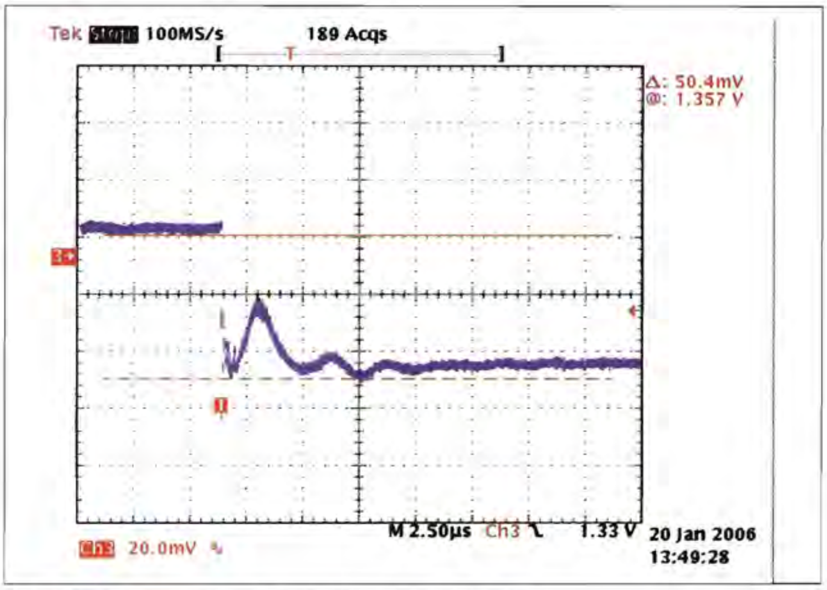


Figure 16: Experiment with applied load step 50A, 50ns

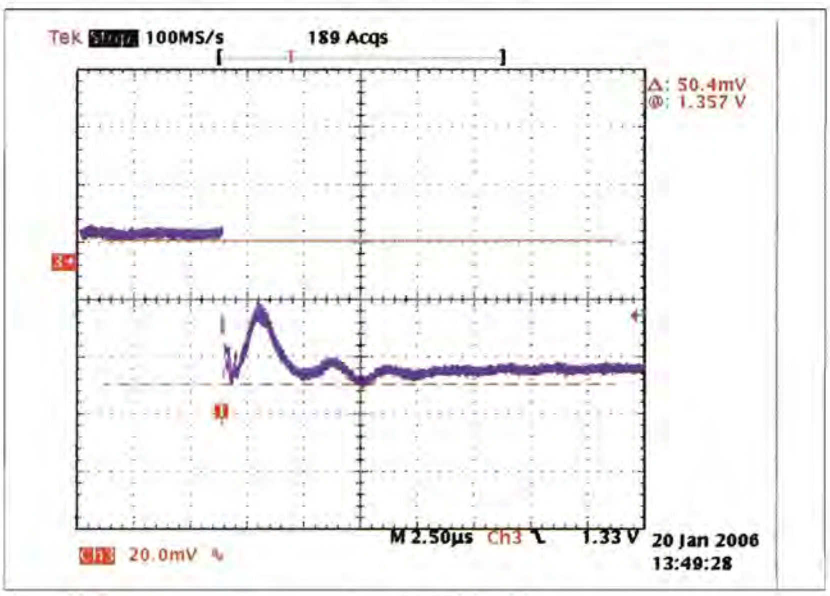


Figure 17: Experiment with released load step 50A, 50ns

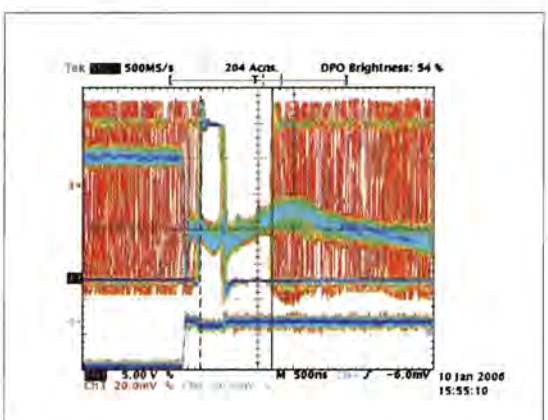


Figure 18: Applied load transient with infinite persistence: LTB pulse is visible at signal "Phase3". Action delay is about 100ns

The small ring-back comes from a not perfectly modeled motherboard parasitic (**Figure 16**).

For the same reason, the output voltage spike is also higher than the simulation. The response time (time needed to recover steady state condition) for applied load and released load are the same for simulation and experimental measures (**Figure 17**).

Figure 18 highlights the LTB pulse that is revealed by infinite persistence. The action delay is effectively around 100ns. It is also possible to observe the result of "LTB Brake": it blanks the phase switching activity to reduce the ring-back of the output voltage.

LCD PICmicro Microcontrollers

Using an LCD PICmicro microcontroller for any embedded application can provide the benefits of system control and human interface via an LCD. Design practices for LCD applications can be further enhanced through the implementation of these suggested Tips 'n' Tricks. These tips describe basic circuits and software building blocks commonly used for driving LCD displays.

TIP 1: LCD PICmicro microcontroller segment/pixel table

This segment matrix table shows that Microchip's 80-pin LCD devices can drive up to four commons and 48 segments (192 pixels), 64-pin devices can drive up to 32 segments (128 pixels), 40/44-pin devices can drive up to 23 segments (96 pixels) and 28-pin devices can drive 14 segments (60 segments).

TIP 2: Resistor ladder for low current

Bias voltages are generated by using an external resistor ladder. Since the resistor ladder is connected between VDD and VSS, there will be current flow through the resistor ladder in opposite proportion to the resistance. In other words, the higher the resistance, the less current will flow through the resistor ladder. If we use 10K resistors and VDD = 5V, the resistor ladder will continuously draw 166m A. That is a lot of current for some battery powered applications.

How do we maximise the resistance without adversely affecting the quality of the display? Some basic circuit analysis helps us determine how much we can increase the size of the resistors in the ladder. The LCD module is basically an analogue multiplexer that alternately connects the LCD voltages to the various segment and common pins that connect across the LCD pixels. The LCD pixels can be modelled as a capacitor. Each tap point on the resistor ladder can be modelled as a Thevenin equivalent circuit.

The Thevenin resistance is 0 for VLCD3 and VLCD0, so we look at the two cases where it is non-zero, VLCD2 and VLCD1.

The circuit can be simplified as shown in **Figure 2**. RSW is the resistance of the segment.

The Thevenin voltage is equal to either 2/3 VDD or 1/3 VDD for instances where the Thevenin resistance is not zero. The Thevenin resistance is equal to the parallel resistance of the upper and lower parts of the resistor ladder. See **Figure 1**.

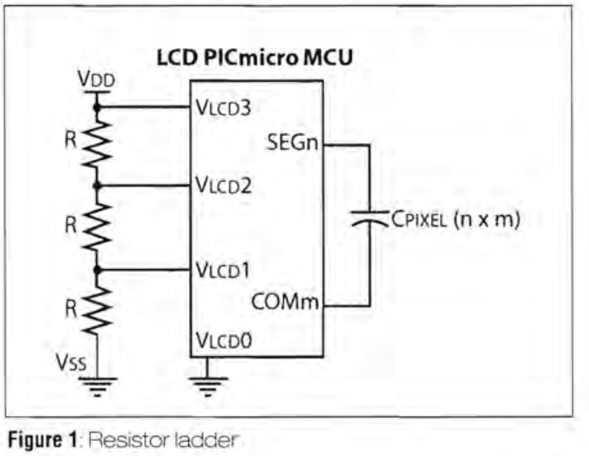


Figure 1: Resistor ladder

As you can see in Figure 1, we can model the drive of a single pixel as an RC circuit, where the voltage switches from 0V to VLCD2. For LCD PIC microcontrollers, we can estimate the resistance of the segment and common switching circuits as about 4.7K and 0.4K, respectively. See **Figure 3**.

Table 1: Segment matrix table

Multiplex Commons	Maximum Number of Segments/Pixels					
	PIC16F913/916	PIC16F914/917	PIC16C92X	PIC18F6XXX	PIC18F8XXX	Bias
Static (COM0)	15	24	32	32	48	Static
1/2 (COM1:COM0)	30	48	62	64	96	1/2 or 1/3
1/3 (COM2:COM0)	45	72	90	96	144	1/2 or 1/3
1/4 (COM3:COM0)	60	96	116	128	192	1/3

Figure 4 indicates that the time required for the voltage across the pixel to change from 0 to VTH will depend on the capacitance of the pixel and the total resistance, of which the Thevenin resistance of the resistor ladder forms the most significant part. The step response of the voltage across a pixel is subject to the following equation:

$$V_{PIXEL} = V_{TH} (1 \,.\, e^{-t/RC})$$

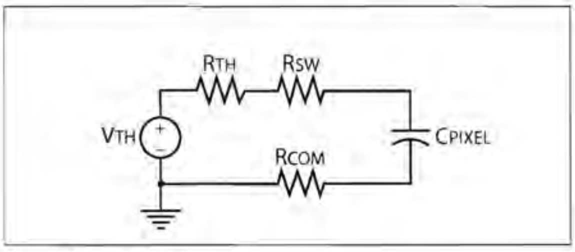


Figure 2: Simplified circuit

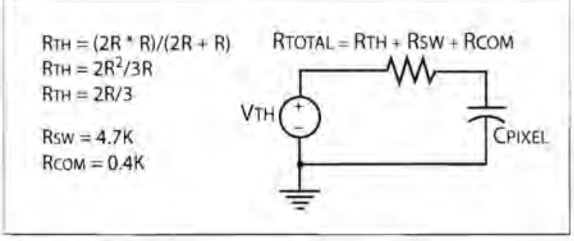


Figure 3: LCD circuit resistance estimate

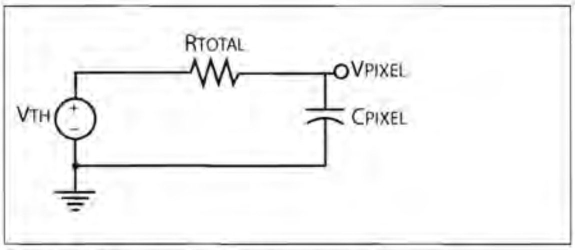


Figure 4: Voltage charge across pixel

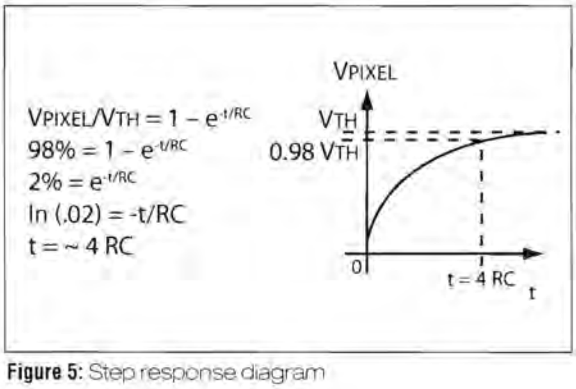


Figure 5: Step response diagram

By manipulating the equation, we can see that it will take a time equal to four time constants for the pixel voltage to reach 98% of the bias voltage. See **Figure 5**.

Now we need to estimate the capacitance. Capacitance is proportional to the area of a pixel. We can measure the area of a pixel and estimate the capacitance as shown in Equation 2. Obviously, a bigger display, such as a digital wall clock, will have bigger pixels and higher capacitance.

$$C_{PIXEL} = 1500 \text{ pF/cm}^2$$
$$AREA_{PIXEL} = 1 \text{ mm} * 3 \text{ mm } 03 \text{ cm}^2$$
$$C_{PIXEL} = 45 \text{ pF}$$

We want the time constant to be much smaller than the period of the LCD waveform, so that rounding of the LCD waveform will be minimised. If we want the RC to be equal to 100m S, then the total resistance can be calculated as shown the following equation:

$$R_{TOTAL} = 100\ \mu S/45 \text{ pF} = 2.22 \text{ m}\Omega$$
$$R_{TH} = 2.2M - 5.1K = 2.2M$$

The resistance of the switching circuits within the LCD module is very small compared to this resistance, so the Thevenin resistance of the resistor ladder at VLCD2 and VLCD1 can be treated the same as RTOTAL. We can then calculate the value for R that will give us the correct Thevenin resistance.

Now we can calculate the current through the resistor ladder if we used 3.3mΩ resistors.

$$R = 3\ R_{TH}/2 = 3.3M$$

$$R_{LADDER} = 9.9M,$$
$$I_{LADDER} = 5V/9.9M = 0.5\ \mu A$$

Use this process to estimate maximum resistor sizes for your resistor ladder and you will drastically reduce power consumption for your LCD application. Don't forget to observe the display over the operating conditions of your product (such as temperature, voltage and even humidity) to ensure that contrast and display quality are good.

Win a Microchip rfPIC Development Tool

See overleaf

Win a Microchip rfPIC Development Tool

Electronics World is offering its readers the chance to win a Microchip rfPIC Development Kit. The kit provides an easy way to evaluate low-power RF communication links for embedded control applications. Designed to work in tandem with the PICkit 1 Flash Starter Kit, the rfPIC Development Kit 1 includes transmitter and receiver modules supporting frequencies of 315MHz and 433MHz.

The receiver modules feature an rfRXD0420 device that plug directly into the PICkit 1 development board. The modules are available separately so designers can create several prototypes based on the same module, without having to develop an actual RF design. All the design files are available, offering users the ability to migrate their module design into the application for lower cost volume production. Target applications for the rfPIC family include remote control, wireless sensors, automotive and home security.

The self-contained rfPIC12F675 transmitter modules are based on a PICmicro 20-pin Flash microcontroller that features an integrated UHF RF transmitter. The transmitter modules feature button inputs for remote control functions and analogue input that can be used for the evaluation of the microcontroller A/D converter peripherals. Code can be developed using Microchip's MPLAB Integrated Development Environment. Programming the microcontroller is easily accomplished by plugging the modules into the PICkit 1 Flash Starter Kit.

For the chance to win, log onto
www.microchip-comp.com/ew-rfpic

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RoHS

WHAT'S ALL THE FUSS ABOUT?

RoHS (the Restriction of the use of certain Hazardous Substances) and WEEE (Waste Electrical and Electronic Equipment) is the equivalent of Y2K for the electronics industry. The upcoming EU environmental directives are the most significant developments in electronics legislation to happen in many years and will completely revolutionise the way electrical and electronic products are designed, sold, recovered and recycled. Worryingly, many design engineers are still not fully aware that the upcoming legislation will affect them. For those who are, many questions remain unanswered. Complicated exemption rules, uncertainty about how the directives will be enforced, obsolescence and component availability has left engineers unsure of what they need to do and when. The clock is ticking. With only several months to go, there's no time to lose in the transition to RoHS. If compliant components aren't already part of the design cycle it could well be too late.

Q: Are there any specific guidelines for physical PCB designs?

Bob Williams, UK

A: *There are no specific guidelines published on PCB design at the moment, but that does not mean that designs can remain unchanged. This is an area that ERA Technology is likely to look at in its 4th edition Guide to Compliance with RoHS. Watch this space.*

Q: My product is bolted down in use. Does this mean that it is a fixed installation that would be excluded from RoHS?

A: *No, just being fixed is not sufficient to mean a product is excluded. The intention of the fixed installation exclusion follows the same principles as the exclusion for vehicle mounted equipment. Products that become part of a product that is outside the scope of the directive are themselves outside the scope of the directive. In the case of fixed installations, the intention is that the product becomes part of the fabric of a building. You need to ask, once fitted is the equipment discernible from the rest of the building or has it become part of the building? If a business was to move, is it likely to move or leave the product? Lifts, electronic doors and gates etc are fixed installations, fitted kitchen appliances, large fixed equipment, CCTV camera systems are not.*

Q: What does the BSI 'RoHS Trusted' kitemark mean?

A: *The kitemark is probably one of the best known and respected certification marks in the world. The independent assessment is on an on-going basis and provides reassurance that relevant requirements have been met or exceeded. It is voluntary and companies are not obliged to seek it. However, those that do are making a public commitment to quality and have confidence in their products and processes. The kitemark will help build confidence around the RoHS Directive and will have significant impacts throughout the electronics and electrical industries through:*

- *Assisting sourcing of electronics and electrical materials, components and equipment throughout the supply chain*
- *Giving confidence to manufactures, producers and their customers*
- *Building a network of 'RoHS Trusted' suppliers.*

Q: What about the 'Primary Function' rule?

A: *The 'primary function' can affect whether a product is affected by RoHS or not. The key is whether the item relies on electronics in order to fulfill its purpose. For example, a teddy bear with a voice box that talks when it is squeezed is still a toy that can be 'used' even without its voice. Compare this to a toy designed for educational purposes — in the support of lessons — if the electronics function wasn't there it would be useless.*

Q: What is the RoHS and WEEE position on batteries?

A: *All batteries are excluded from RoHS as they are covered by the batteries directive. The current batteries directive requires certain labelling for toxic substances and bans mercury in batteries except button cells. The proposed new batteries directive is likely to have additional substance restrictions but as yet it is not decided what these will be.*

As far as WEEE is concerned, this requires batteries to be removed from equipment at end of life and separately recycled. When providing sales data to WEEE registration bodies, exclude the weight of batteries if the producer is also registering for the battery directive.

It is worth noting however, that battery chargers do fall within RoHS, the category being determined by the application.

Q: Can you define "infected" products?

A: *The WEEE directive does exclude infected medical products but does not define infected. In the healthcare industry, any equipment that has come into contact with "body fluids"— blood, etc. — is "infected" but many products can be decontaminated by hospital staff. If it is not possible to decontaminate equipment by normal hospital procedures, then they are incinerated and so cannot be recycled. The medical trade associations are developing a definition of infected products along these lines. As far as producers are concerned, this may not be important because when they register, they will need to provide sales data – irrespective of whether the products become infected or not – to WEEE registration bodies. If products are supplied to consumers or hospitals, then the fee paid to compliance schemes (if one is used) should take into account the proportion that reach end of life and are available for recycling.*

Q: Where can I find details of military exclusions?

A: *The European Commission's guidance on this is that Military equipment is excluded from the WEEE Directive (categories of Annex IA) and, therefore, not covered by the RoHS Directive.*

Q: What is Orgalime?

A: *Orgalime is a European Engineering Trade Association representing the interests of the mechanical, electrical, electronic and metalworking industries. It tries to help the industry draw up adequate contracts and give practical advice on frequently occurring legal questions. It has produced its own guide to the scope of WEEE and RoHS. This is available on its website www.orgalime.org.*

Gary Nevison is chairman of the AFDEC RoHS team, board director at Electronics Yorkshire and head of product market strategy at Farnell InOne. As such he is our industry expert who will try and answer any questions that you might have relating to the issues of RoHS and WEEE. Your questions will be published together with Gary's answers in the following issues of Electronics World. Please email your questions to EWeditor@nexusmedia.com, marking them as RoHS or WEEE.

Sinusoidal Oscillator Using OTAs and Grounded Capacitors

Sinusoidal oscillators are increasingly becoming important in many areas such as instrumentation, communication measurements and others. The uses of OTAs in developing oscillators are attractive because they offer highly linear electronic tunability and wide tunable range of transconductance gain, besides their operatation at high frequency.

Moreover, these oscillators are suitable for IC implementation either in bipolar or CMOS technology as they are devoid of resistors. For IC implementation, the grounded capacitors are highly suitable as they require less silicon area and absorb parasitic capacitances. Several OTA-C oscillators have already been reported. They use either three or four OTAs and grounded capacitors, or two OTAs and floating capacitors. Besides, for the two OTA-C oscillators, oscillation and frequency of oscillation are a condition of the transconductance gain.

Here, I introduce a new OTA-GC oscillator that uses two OTAs and grounded capacitors. The proposed oscillator is suitable for IC implementation in bipolar or CMOS technology. The proposed oscillator offers the following salient features:

- use of OTAs
- high frequency operation
- grounded capacitors
- electronic tunability
- suitable for IC implementation
- independent adjustability of frequency of oscillation (FO) and condition of oscillation (CO).

OTA is differential voltage controlled current source (DVCCS) and is characterised by the following equation:

$I_o = g_m(V^+ - V^-)$

where g_m is the transconductance gain, which is function of the bias current used to control frequency of oscillations, thus lending electronic tunability to the circuit, which is highly desirable in IC technology. The expression for g_m is given by:

$$g_m = I_b/2V_T \quad (1)$$

where I_b is the bias current and V_T is the thermal voltage equals to 26mV at room temperature.

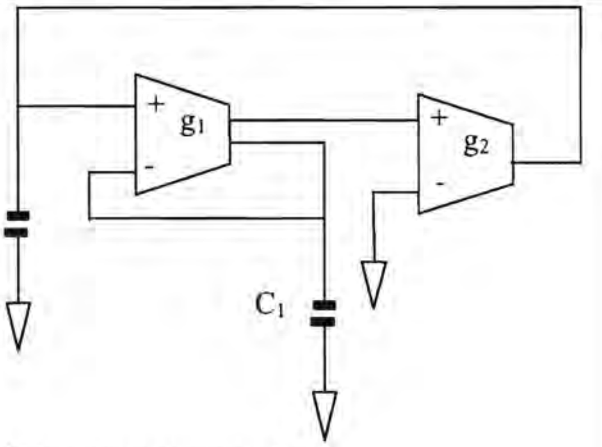

Figure 1: Electronically tunable oscillator

The proposed oscillator is shown in **Figure 1**. Routine analysis yields the following characteristic equation:

$$s^2C_1C_2 + sg_1(C_1 - C_2) + g_1g_2 = 0 \quad (2)$$

The condition of oscillation (CO) is:

$$\text{CO} \qquad C_1 = C_2 \quad (3)$$

and frequency of oscillation (FO) is:

$$\text{FO} \quad \omega_0 = (g_1g_2/C_1C_2)^{1/2} \quad (4)$$

For $g_1 = g_2 = g$, and $C_1 = C_2 = C$, the FO is given by:

$$\omega_0 = g/C \quad (5)$$

from equation (3) and (4), it is clear that the CO and FO are independently adjustable.

Moreover, the FO is linearly tunable through the transconductance gains of OTAs and in terms of bias current the FO is given by:

$$\omega_0 = I_b/2V_TC \quad (7)$$

From equation (7) it is clear that the frequency is linearly and electronically tunable through the bias currents of OTAs over a wide range.

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India

Electronic Audio Balun

The circuit in **Figure 1** can be used to convert balanced audio signals to unbalanced audio signals and vice versa and to eliminate ground loop. It works much like a signal transformer, but it is considerably cheaper than a good transformer, it has a flatter transfer and it doesn't short-circuit the signal source at low frequencies. It was designed and built for Haarlem 105, a Dutch local FM radio station.

Haarlem 105 has a very low-budget studio using a mixture of professional, semi-professional and consumer equipment. The professional equipment is usually earthed and has balanced inputs and outputs. The consumer equipment is usually double isolated with unbalanced inputs and outputs. Some of the semi-professional gear and the computers combine the worst of both worlds: earthed with unbalanced audio inputs and outputs, making ground loop problems inevitable.

The circuit is based on indirect voltage feedback. The voltage between the positive and negative inputs is converted into a current by the degenerated differential pair Q1-R1-R2-Q2. The voltage between the positive and negative outputs is also converted into a current by an equal differential pair Q3-R3-R4-Q4. The signal currents are subtracted and their difference drives the balanced output stage Q5-Q6. Hence, the feedback loop tries to make the

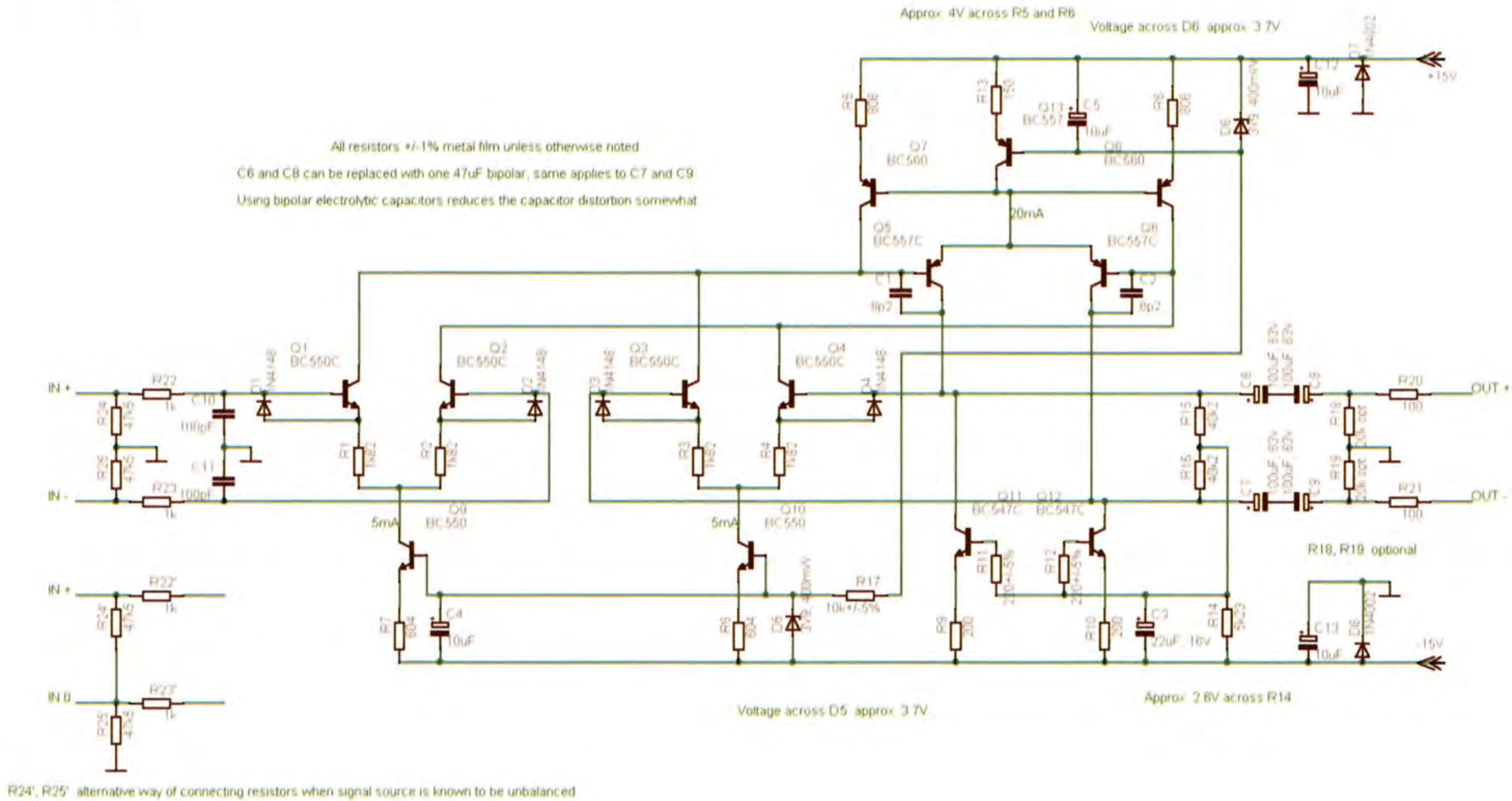

Figure 1: The schematic diagram

difference between the output voltages equal to the difference between the input voltages. The distortion of the degenerated differential pair at the input, which is already quite small, is largely cancelled by the equal distortion of the differential pair in the feedback path.

The feedback loop only sets the voltage difference between the positive and negative outputs. Therefore, the amplifier output basically acts as a floating voltage source, just like the secondary of a signal transformer driven by a voltage source. When the negative output is connected to the ground of an unbalanced load and the positive output is connected to the hot side of this unbalanced load, the amplifier develops the correct signal voltage across the load, regardless of any ground voltage differences between the amplifier and the load.

The circuit is designed to have a signal handling capability of about 9V peak, well above the +4dBu or 1.228V RMS, 1.737V peak level normally used in professional audio and well above the 2.828V peak full-scale normally used in consumer CD players.

If clean clipping is of importance, it is advisable to bias the feedback stage at a slightly higher current than the input stage. This can be done by increasing R7 to 634 ohm and reducing R8 to 590 ohm.

In order to keep everything properly biased, some sort of common-mode loop is required to set the common-mode voltage at the collectors of Q5 and Q6. Unfortunately, this common-mode loop makes the amplifier output look less like a floating voltage source, reducing its effect. A slow and weak common-mode loop is used to keep the common-mode output impedance as high as possible at audio frequencies. The circuit around Q11 and Q12 acts as the weak common-mode loop. Due to the filtering provided by C3, the common-mode loop does not do much at audio frequencies.

R18 and R19, which keep the outputs biased at 0V, also reduce the common-mode output impedance to some extent. If the load is not sensitive to the DC voltage anyway, it is best not to place R18 and R19.

The ground of the amplifier can be connected to either the ground of the signal source, or the ground of the load. If the purpose is to break ground loops, it should obviously not be connected to both.

Marcel van de Gevel
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Send new circuit ideas to:
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Basic Engineering Mathematics

John Bird

Newnes (Elsevier)

Before opening this book, I wanted to get clear in my mind what I would be expecting from it as a young student who might not be 'that good' at maths. I decided I wanted lots of realistic examples, minimum of jargon and a lively text. By 'realistic' I mean plausible real-life problems that I might actually encounter. By looking for a 'minimum of jargon' I was hoping to find mathematical processes called by names I would easily recognise, with no undefined acronyms. By 'lively text' I would be looking for a conversational style which sought to include me and not simply seek to impress me with the author's knowledge.

The subject matter in this book covers a broad range of topics from basic arithmetic, through formula manipulation and algebra to more complex topics like vectors and waveform addition. Some might regard some of the earlier chapters as too basic, but my own personal experience has shown that young students are not always as competent as I would have expected them to be. Some students seem to leave school with a blind spot for maths, which can actually steer them away from quite rewarding careers in engineering. I was pleased to see that this book addresses some of these basic issues that can be such a stumbling block when trying to comprehend some of the more difficult concepts.

The format adopted for each chapter, and there are thirty-four in all, has an introductory section, a number of worked examples to illustrate the techniques involved at each stage as the topic develops, followed by exercises for students to try on their own. Some of the chapters are quite short and I found this helpful. The exercises are supported by answers at the end of the book, so that the student isn't left high and dry, and I was pleased to see that acronyms, such as HCF (highest common factor) are highlighted and defined on first use.

Lets take 'Chapter 26 – Triangles and Some Practical Applications' as an example. This chapter starts by looking at 'solving a triangle' to find its properties of side lengths, area and angles, and introduces the sine and cosine rules and area equations for any triangle. This is followed by six different worked problems for a whole variety of different triangles. But, and this is important, the student isn't just left wallowing in theory but a number of real-life practical problems are introduced and worked through. These cover applications in mechanics, surveying and electronics, so there is something for everyone to relate to. The chapter concludes with a summarising assignment of exam style questions.

There is a summary of formulae at the end of the book, which is very helpful as quick reference to such things as volumes and surface areas and standard integrals. They are all formulae that probably come to mind as second nature with time, but it is still useful to have all these collected in one place to save having to delve into the text.

So how did this book fare against my original criteria? Well, pretty good, actually. I found it easy to read, although at times some of the explanations for the processes were rather long and I had to re-read sections. It can be hard to avoid this in a printed text, and some concepts can be so much easier to convey through an animated diagram – computers do spoil us. There are a lot of diagrams and a lot of mathematical expressions, which are all well laid out, but, occasionally, I felt I needed a little more. For example, when manipulating equations, the use of arrows to point to where coefficients should move would reinforce the text-based description of the process. It might also have been helpful to use some colour highlighting in the text to brighten things up a little, but this carries a premium and there has to be a compromise to keep the cost within reach of young students. I'm probably being very critical here but I'm aware how easy it is to 'lose' students if the subject matter gets too dry.

However, I'm sure that most students at this level will find this book meets their needs and will be worth hanging on to for reference, throughout their careers. I have tried to review the book from a student's standpoint, but teachers will also find the book very useful as a resource. There is a separate instructors manual available although I have not seen this. The theory sections are sub-divided into readily digestible chunks and there would be plenty of opportunity for getting students to work on their own. I know I will find it useful.

John Wood

Introduction to AutoCAD 2005 2D and 3D Design

Alf Yarwood

Elsevier

Yarwood has authored many books on successive releases of AutoCAD and this book maintains the standard. It's an update to his Introduction to AutoCAD 2004.

Autodesk's AutoCAD is a bit like Microsoft Office in that it's not the cheapest in its class and it's not the most elegant available. But, it is the industry standard for technical drawing. If you are an engineering student, you'll need to master AutoCAD. If, like me, you've been working with a rival CAD system, then you probably need to convert to AutoCAD. Either way, this book is for you.

The book is primarily intended as a tutorial. It contains a structured set of exercises that will take you from being a complete novice through to being competent on all key aspects of drawing in AutoCAD 2005. It doesn't pretend to make you an AutoCAD expert, after all Autodesk's own documentation is at least 10 times as thick.

The book aims to cater for CAD units of the UK BTEC Higher National and BTEC National Engineering schemes from Edexcel, and the City & Guilds 4351 qualification.

Advanced topics like programming in AutoCAD Visual Basic for Applications, obtaining parts lists/bill-of-materials and interfacing with other CAD/CAE systems or computer aided machining are not covered.

Most of the tutorials and exercises in the book have a machine part orientation. Some are architectural. But you shouldn't have any trouble applying what you can learn from this book to AutoCAD's main applications in electronics — laying out equipment floors, designing rack layouts and designing equipment chassis, cases and packaging. Chapter 9 has two pages on using blocks to create electronic circuit symbols for use in schematics.

The author has a simple easy to follow writing style, illustrated with copious screenshots and drawing fragments. You won't have any trouble following it.

A typical chapter is structured around:

- Aims of the chapter
- Introduction
- 5-12 sections focused on learning a tool (e.g. scale, move, extrude etc, or drawing components (e.g. blocks, sectional views, etc)
- Revision notes
- Exercises

I found this structure helped me remember what I'd learnt.

Chapter 1 provides the basics on starting AutoCAD, using the mouse, using dialogues and toolbars, and introduces the reader to templates.

Later chapters cover :

- Drawing simple outlines
- Positioning (object snap, autosnap etc.)
- Drawing (arcs, ellipses, rectangles etc.)
- Zoom and pan
- More on templates
- Modify tools (object copy, mirror, offset, array, move, scale, trim, stretch, break, extend, chamfer and fillet)
- Dimensioning and tolerancing
- Adding text
- Orthographic (3-view 1st and 3rd angle) and isometric drawing
- Hatching and gradient shading/tinting
- Blocks and inserts (drawings inserted as components or symbols in other drawings)
- Sheet sets (all drawings associated with one item can be defined and managed as a set)

Nine chapters cover 3D modelling to considerable detail-drawing, manipulating, surfacing and rendering. There are also a few miscellaneous topics such as typical product design process, using email and the Web, and AutoCAD 2005 enhancements over AutoCAD 2004. An appendix gives a basic overview of printing/plotting.

The publishers have created a companion website at http://books/elsevier.com/companions/0750667214, where you can view and download step-by-step solutions for all of the exercises in the book. Solutions are provided as PDF files; drawing files as DWG files. You can also download all material belonging to any chapter as a ZIP file. Some files in Microsoft Word format explain step-by-step how to do the exercises.

Note that Autodesk is already selling AutoCAD 2006.

Pam Creed

Small PC Enclosures DC Blower

The ADDA AB4505 DC blower from Aerco is built in a 45 x 45mm square frame and is only 7.5mm thick. As such, it is ideal for mounting in small PC enclosures.

Operating from a 5 or 12 volt DC supply and running at a maximum speed of 5,700rev/min, the AB4505 provides 0.85litres/s (1.8CFM) airflow in free air and, because of its compact size, is ideal for chip and hot spot cooling. Either a ball and sleeve combination or the ADDA patented HYPRO bearing system can be specified, both of which provide a life expectancy in excess of 50,000 hours at 25°C.

Standard two-wire and three-wire tachometer speed sensor signal is provided for fan failure protection and special lengths of supply cables are available fitted with customer specified connectors to simplify installation and reduce production costs.

The AB4505 is RoHS compliant and CE approved.

www.aerco.co.uk

Molex's New Interface Modules

The new 39170 series of interface modules from Molex are clamed to provide a cost-effective method to interface field wiring to PLCs and other control devices. Molex's new DIN-rail mounted devices have been developed to connect a high-density cable from a PLC or electronic control system to terminal blocks where wiring from field devices is terminated.

The connections between the high-density PLC cable and the terminal blocks are pre-wired on a printed circuit board. The result is a reduced wiring time as much as 50%, as well as a quicker checkout of new control systems and faster troubleshooting of installed systems. The 39170 series also offers space savings of up to 60% compared to standard DIN rail terminal blocks.

The new modules are ideally suited for a vast range of applications from industrial control equipment such as PLCs and motion controllers, to machine builder applications such as packaging and milling machines, and are also tailored for material handling equipment including conveyor systems and elevators, or transportation applications such as signal control, railway switching and jetway systems.

Interface Modules support from 9 to 50 circuits per module. The modules are available with fixed or pluggable terminal blocks, and the PLC/controller interface is available with a ribbon cable connector or a D-sub connector.

www.molex.com/product/interface_modules.html

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The XF range, with outputs ranging from 25kV to 50kV, has the high voltage section encapsulated in silicon rubber, for long term protection against dust and moisture. Control of output voltage and current is by internal potentiometers or external 10V analogue control voltages.

Output ripple is less than 1% peak to peak for both ranges, which are rated at 100W. Their high reliability has been achieved through particular attention being given to arc hardness and high voltage stress. Full turn-on sequencing is provided with both ranges, to minimise stress on the tube and power supply.

www.appliedkilovolts.com

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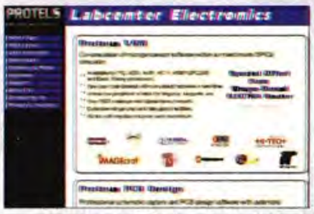

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