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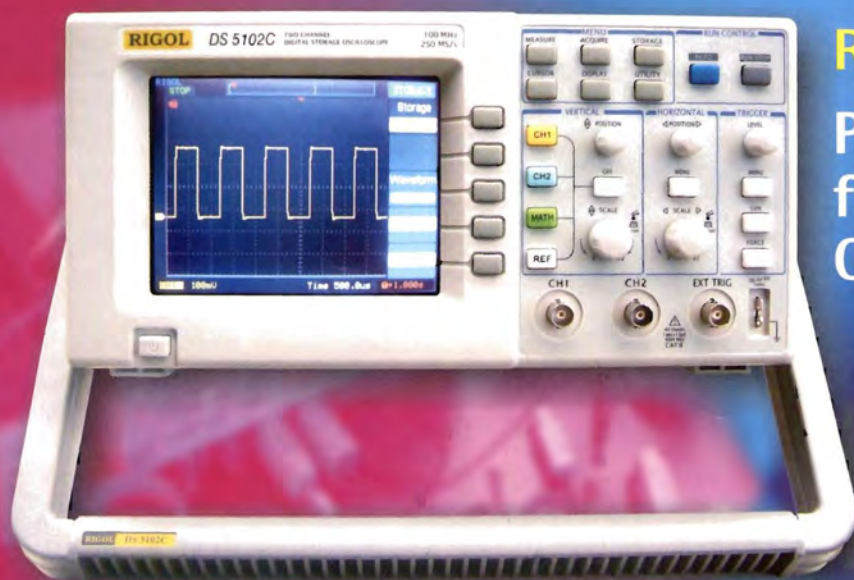
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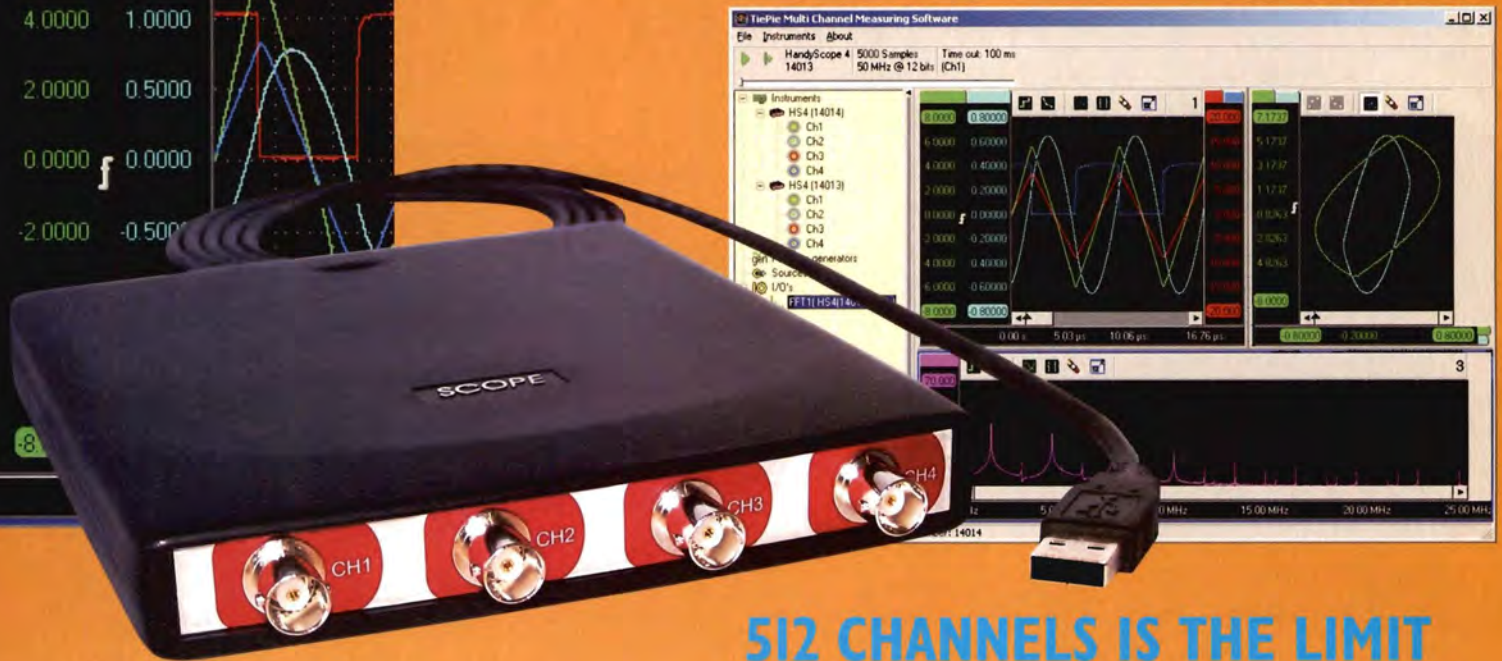
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## Four channels not enough



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# Let's Talk Rubbish

The beginning of this coming New Year does not have to start, as per usual, with cheer and thoughts of happy beginnings. This is the year when the Waste Electrical and Electronic Equipment (WEEE) directive kicks in. By that time, the directive would have been almost four years in the making. And it all started because the electrical and electronic waste is the fastest growing in the EU.

This is not surprising considering how easy – and relatively inexpensive – it is to replace old equipment; 'replacement' being a notion that our parents would have thought wasteful only a few years ago. Nowadays, most electronic equipment has a very short lifetime and the simplest thing to do when it expires – especially with small items such as electric shavers, electric toothbrushes and mobile phones – is to dump them in the bin without much thought. After all, what could one do with them? Store them in a plastic bag in the garage forever?!

Recently, the Royal Academy created a man-sized sculpture made solely out of dumped electrical and electronic equipment, called the WEEE Man. It is said that each of us on this earth dumps as much equipment in our lifetime to create such a sculpture. The mind boggles when one starts thinking about the size of the population and what that equates to in terms of electrical and electronic rubbish. Effectively, each of us has a WEEE duplicate.

Calculating the size of the problem has made the EU get on to the case, which is when the WEEE directive concept was born.

The idea is laudable, but is it practical and cost-effective? First comes the registration of each producer of electrical and electronic equipment. This in itself, apart from being costly, is time-consuming. The form, it is said, contains a thousand data-fills.

However, if you don't register, you are perpetrating a criminal act. Then follow the issues

related to the type of materials used in the manufacturer's product. At the point of disposal of such equipment, we still do not understand – as individuals or businesses – where to 'bin it' (with relative piece of mind).

Similar conundrums will dog every landfill and recycling firm, as well as local authority and retailer that needs to deal with WEEE.

Each EU member government has to collate its country's data and supply it to the EU. This includes household and business goods, but also all such equipment that has been exported to other EU member states. The EU will count a market share based on how much WEEE a manufacturer creates.

These are just some of the requirements we know of that need to be met from 2006 onward.

But what are about all the unknowns? Who is going to declare, qualify and assess the directive's effect on the goods sold by all the Dell Boys of the EU; the versatile merchants who one day sell apples and tomatoes and the next DVD players? Do they register? Who controls them?

What about all the goods that are returned from the retailer to the manufacturer? When will declaration take place: at the point of return, collection or disposal? Will that be at the retailers' site or the manufacturer?

In addition, there will be no accounting as to the amount of WEEE that will continue to crop up in landfills. How will that be approached?

There are so many questions that, for the time being at least, remain unanswered. Most of them relate to the detail – so much detail, in fact, that it will be difficult to pin down and even more difficult to deal with. It'll be interesting to see how the directive fares once it is in place. I suspect not so well: as the saying goes, "the devil's in the detail".

Svetlana Josifovska  
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## Mobile services ready?

The mobile phone has perhaps been the most successful product of the past twenty years. The base 2G GSM telephone has created a highly successful market with voice and, specifically, text services, building a new model for person-to-person communications. The much-trumpeted 3G was meant to take this to a new level with its high speed and increased bandwidth but, in reality, the model has not changed.

What has not happened is the rush of third party application providers producing a host of new services that can be used over the networks. This is partly the operators' fault because they are scared of the openness that IP provides. If everyone has easy access to the network, then there can be security issues with hackers and spamming, as experienced on the Internet, which will be difficult to control and, therefore, profit by. The operators have spent a lot of money upgrading their networks and they want a share of whatever money is made from them; they don't want to be just carriers. A totally open network could leave them in that situation.

In addition, there is no standard framework for third party developers to work with. Applications that do appear have their own way of working, with their own log-on systems. There is just too much for the average user to learn.

Wave the magic wand and something called IMS (IP Multimedia Subsystem) appears that could solve all the above problems, though

the cynical see it as just another way for equipment providers to sell more kit now that all the operators have bought into the 3G infrastructure.

For a relatively modest investment – say, £3m to £4m for a small operator – IMS promises to allow the operators to keep control of the network while providing a standard interface that can link all the applications together, not just on mobile and fixed phones but across platforms such as desktop PCs and PDAs. It is a bit like an operating system for mobiles.

IMS first appeared in release five in early 2002 of the 3GPP's constant upgrading of the mobile standards. Release six early last year advanced the IMS part and release seven, which is in progress, looks like taking this even further. It is basically part of the 3G version of SIP (Session Initiation Protocol).

But, as delegates at IIR's recent IMS Global Congress in Budapest discovered, life is not that simple with interoperability and quality of service issues still to be resolved, on top of which is the problem of planning the transition to IMS.

The IMS standard, as written by the 3GPP, also calls for operators to be running IP version six, but nearly all currently use version four. Opinion is split on whether to move to IPv6 first or test the water with IMS on IPv4. Upgrading to both IPv6 and IMS at the same time may be too much for some operators.

## Without quality, users may reject new services

However good the new services that IMS brings, customers will not accept them if the quality is low. This means operators must be able to guarantee a certain bandwidth for IMS services so that they control the likes of delay, jitter and information loss. The problem is that operators will have to support thousands of IMS services simultaneously.

For example, services such as television over mobile are very bandwidth-hungry and could become popular during, say, major sporting events. As David Neale, vice president for service development at Rogers Communications, pointed out: "You don't need many people watching TV over your network to ruin it."

If IMS takes off the way it is hoped, then the networks are going to have to support a mixture of real and non-real time services. Two users talking over their phone may exchange pictures, video and documents while they are talking, and this could be across different networks, operators and countries. A typical call could, therefore, start

with the first operator passing its requirements for the session to the second operator in terms of video and audio in real time, and document exchange in non-real time. The other operator responds with what it can handle, which may be different. If the two operators can agree on the requirements for the session, then the call is initiated. All of this has to be done in the time it takes to make the call and be transparent to the user.

"Once the session is agreed, both networks then reserve the resources for the duration of the session," explained David Moro, project manager for IMS at Telefonica. This creates a balancing act for the operators. They do not want to tie up such resources on a call that ends up not using them and, yet, they know that if the resources are not there when needed, then users may start rejecting the new services.

"To get end-to-end QoS [quality of service] you need to request and reserve resources, and the session has to be managed to control how the resources are allocated," said Moro.





# IMS trials are well on their way

The GSM Association has started conducting SIP (Session Initiation Protocol) and early IMS (IP Multimedia Subsystem) interoperability tests with the biggest trial taking place at Scandinavian mobile operator Telia Sonera. "We are bringing together mobile operators and vendors to try out SIP-based services," said David McDonald, director of technology and standards at the GSM Association. "Telia Sonera is leading the trials."

Although it will be some time

before IMS is working on real networks, he said that it was important to sort out problems before it was launched rather than going back to sort them out later. Early action will avoid IMS from creating "islands of services" that will not work with other services or on different networks and handsets. Standards, added McDonald, do not guarantee interoperability.

So far, more than 20 companies have participated in three trials, two in Europe and one in

Asia, the first of which started in January 2005 and focused on basic SIP inter-working between multi-vendor IMS systems. It managed to get core IMS systems from different vendors working together and demonstrated actual IMS services from Nokia, such as video sharing, gaming and multimedia instant messaging.

The second took the results from the first trial but added various technical extensions, including converting from IP version four to six. This is

important because when IMS is launched, some operators will have moved over to version six but many will still be on version four and any system has to work across both versions.

The tests were remarkably successful with no service-affecting bugs or problems nor issues over standards.

There were however problems found with tunnelling IMS through existing non-IMS networks and some bugs within the applications.

## How to get to where we want to go

Though just about every mobile operator agrees that IMS is the way forward, there is still much scratching of heads when it comes to how to do it and when. Bill Chapman, chief platform designer at BT, gave a stark warning to the IIR's IMS delegates when he said it was going to be "an extremely long haul".

One of the problems is that IMS is still a moving target with many varying definitions of what it will mean in practice, and it may be some years before this is stable.

Meanwhile, operators know that if they are not going to be left behind they have to start the move soon; most are looking to install equipment next year and begin trials.

Also, existing services must continue to be supported, which effectively means living with a hybrid network. The goal is for the hybrid situation not to last too long.

"The danger is that you end up with two networks that your customers are using," said Coert de Boer, director of worldwide services at Lucent

Technologies, "and you end up having to support both".

Even when an operator has moved to a full IMS network with an IMS application server, it will still have to support legacy networks at other operators, which will mean gateways and translation protocols.

"Migrating to IMS is not trivial," said Kristofer Kimbler, president of equipment provider Appium. "It is a big investment and a big operation."

While the initial trials of IMS

should be kept separate from the core network, to avoid having to support two networks for the long term, operators should start thinking about deploying a platform than can handle services across different networks.

But even before the trials have begun, new services being introduced today must be IMS ready if the operator is to protect their investments.

Mark Tubinis, vice president for IMS at Alcatel, suggested a

four-step approach for the migration to IMS. The first is getting ready. Work out what services you want initially and when, and start using enablers such as presence that will be key to the IMS offering.

Secondly, build the service delivery environment and implement changes that need to be made to the legacy services. This means buying application servers to tie in the existing services with the new IMS services. "Let's pick the services and start converting them," he said.

Step three is where the operator starts to take advantage of the easy integration of third party applications. This is also where tight quality of service (QoS) needs to be introduced to control new applications that may have been developed without QoS in mind.

The final step is to integrate fully all the services so that they are provided in a consistent fashion to the end user.

"We will get to IMS, the question is how," he said. "The way to prove it is by doing it."





BAE Systems in Australia is developing a sensor that will allow safe landing of helicopters in conditions currently considered too dangerous or impossible. Three-dimensional synthetic vision will be used in addition to a laser radar, based on the Eagle-OWL obstacle-warning sensor, to help pilots maintain orientation and situational awareness. The 3D synthetic vision will be a part of the existing pilot displays, where the landing area will be presented in an intuitive form.

Ω

StarCore has unveiled its latest MPU architecture – the StarCore V5, which is scalable to over 1GHz and suitable for multimedia handsets and basestations. Among its latest additions are 47 new instructions, which improve support for compilers and operating systems, enhance single-instruction multiple-data (SIMD) processing and deliver enhanced Viterbi performance. The new V5 instruction set, built on StarCore's proprietary variable length instruction set (VLES) technology is based on a combination of DSP performance and code density of the most efficient microcontrollers.

Ω

Exception PCB has developed a new process to enable microvias to be towered within the inner layers of high density PCBs. This helps designers to maximise real estate and add new features and functions, but it also allows greater heat dissipation. The development involves creating the microvia of just 0.1mm with a laser. Exception's new technique can work within the tolerances required to form tiny wells within the boards that enable towered microvias to be created.

Ω

Maxell's new battery – the CR17450 – owes its high capacity and long life to a combination of spiral type batteries and bobbin type batteries. It inherits its high power from the spiral batteries, and high capacity and long lifetime from the bobbin battery. The new structure is an environmentally friendly lithium battery, with a unique 'spiral wound' construction and improved electrical conductivity. It has high-rate discharge capabilities (maximum pulse discharge current 1,000mA) and a high temperature tolerance (-40°C to +85°C).

## Biometrics technologies fail on certainty but not on popularity

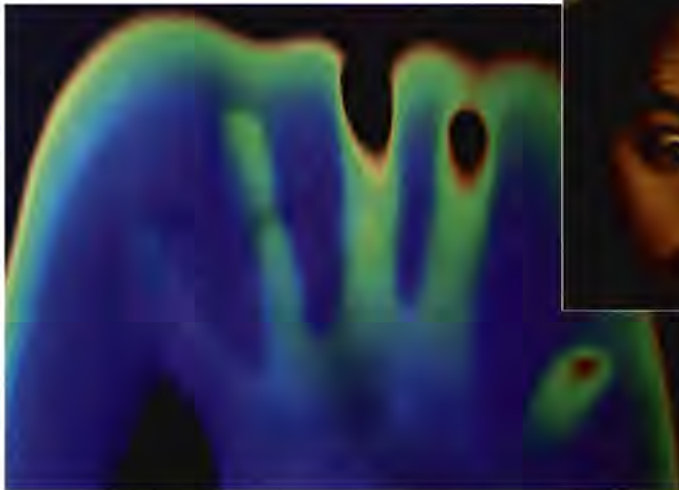
Biometric technologies are not perfect for verification and identification, nevertheless, governments are still going ahead by introducing them in passports and ID

tively efficient – if you don't equate efficient to perfect," said J. C. Burgelman, head of the ICT unit at the IPTS, who carried out a study on elec-

them, due to disfigurements, for example. Still, the EC believes that their introduction will create a "vibrant European

industry sector".

"If we have more digital environments around us, the need for identification will only increase," said Burgelman. Forecasts



predict that global biometric revenues will more than double in three years, to reach \$4.64bn by 2008. Biometrics technologies will be used for verification, identification and screening – deciding if a person is wanted in a country or not. Electronic technologies range from scanning the face, fingerprints, iris, DNA, voice, hand geometry and palmprints to checking more 'exotic' human traits such as gait, ear shape, retinas and facial thermograms.

cards to combat terrorism as well as benefits fraud.

"Biometric technologies are not the solution or the only solution to implement security. They are not perfect technologies – but, then, which one is? However, it is increasingly inevitable [that they will be used], it's convenient and rela-

tronic identification for the European Commission's Directorate-General Joint Research Centre.

Although biometrics technologies are seen as convenient and difficult to forge, they do not always deliver a 100% certain identification and not everyone will be able to use

## Non-compliant companies will be in line for prosecution

Prosecutions on the non-compliance of the Restriction of the use of certain Hazardous Substances (RoHS) directive in the electronics sector are likely to start in the middle of next year, and yet many electronic system designers are still wondering what RoHS is.

"What's scary is that there are six months away from the legislation [starting date] and design cycles last up to 18 months and, yet, some designers are still questioning,

"What is RoHS?," said Kevin Yapp, marketing director at components distributor Farnell InOne. "There are still those who are sitting on the fence until the first prosecutions take place," he added.

The RoHS directive kicks into play on July 1st, 2006. Many organisations are already announcing RoHS compliant products, but there will be others who will be 'flushing out' stock in the meantime, which means that

products and systems containing them will not be compliant past this date.

Farnell InOne is an international distributor of electronic components. Last month it launched a new catalogue consisting of some 25,000 RoHS-compliant components, which is "enough to populate a board", as Yapp says.

"We tried to improve our proposition to the design engineer, as they will need to worry about RoHS a lot sooner than anybody else," he added.



# WiMax is hype, says Nokia

**W**iMax cannot deliver today what it has been promising for some time, as it is hype. "WiMax is hype at the moment. It's a great technology and it has industry backing. It will offer wireless broadband, but, at the moment, it is all hype," said Markku Höllstrom, head of WiMax development at Nokia.

He said that any firm that labels its product as WiMax compatible "is lying". "There is no WiMax in the world," he added.

Gartner analysts have also branded WiMax as hype. They are carefully watching promising technologies, aiming to predict their deployment. According to Eric Paulak, a managing vice president at Gartner, WiMax's massive infrastructure will need to

be built by someone, but "currently, companies are too busy buying each other to make the financial commitment that WiMax would require".

Many of WiMax's backers have envisaged that this technology will compete with DSL and cable modems for residential and small business broadband access by 2008. Nokia's Höllstrom explained the likely adoption curve: "Fixed WiMax cost of connectivity will be fairly expensive - thousands of euros - and there's no alternative for self-installment, so this will be a niche technology. A [cheaper] alternative would be a modem, then PCMCIA cards are coming in 2006/2007, which will bring costs down. Then, it will come to high-end mobile phones."

He said that Nokia is particularly betting on the mobile WiMax standard - the IEEE802.16e. However, although already expected by now, its ratification will not take place until early next year. Even then, Höllstrom says, the standard will be 1300 pages long and most of it unimplementable. "You need subsets, agreed by the industry first," he said.

WiMax uses a widespread wireless spectrum to provide fixed and mobile broadband access across distances of up to 50km. It is based on the OFDM (orthogonal frequency division modulation) scheme and, as such, it is very good for delivering data, and more efficiently than 3G. Although 3G can be milked for data it is not broadband, which WiMax can do with

ease. WiMax is also a good technology for wireless broadband services as it offers embedded security and quality of service.

Average data rates of 70Mbit/s are achievable at distances of up to 50km, but the peak data rate is specified at 268Mbit/s.

Nokia and Intel are expected to announce WiMax joint products in the near future. According to Höllstrom: "We'll be selecting our technology partners by the end of 2005 and early 2006. We're comparing notes [now] with Intel. Commercial trails will start during 2007 and commercial networks and devices will be available in 2008, especially in the Americas and Asia, but not necessarily in Europe."

## The WEEE directive could be helped with protocols

**T**he industry needs protocols if the European Union (EU) is to make success of the Waste Electrical and Electronic Equipment (WEEE) directive. So says David Hulse, public affairs advisor with S. Norton and Co. and an ICER (Industry Council for Electronic Equipment Recycling) representative.

"It will be desirable for some protocols to be established when it comes to the materials that are going into WEEE," he said. "Protocols are created by industry and verified by the Environmental Agency."

The protocols - similar to the Packaging Protocol established in 1997 - will help identify and categorise the type of hazardous and non-hazardous materials that are present in

WEEE at the point of collection and after disassembly. The industry could specify what types of materials and to which percentages are used in their products, which range from small and large household and consumer goods to business equipment. Based on those expectations, a range of recovery methods for such materials could easily be established, which will help all the parties involved, but also the governments who are meant to report their data collected over a period of at least two years into the EU.

"The benefits of protocols are manifold: there'll be less effort going into weighing and measuring (of WEEE); lower costs of monitoring and reporting [of hazardous and



non-hazardous materials] and they enable concentration on the difficult areas of [these] materials' recovery and disposal," said Hulse.

The drawbacks, however, lie with how to attract all of the electrical and electronics equipment makers - and even retailers - to join such a scheme.

The WEEE directive kicks off

in January 2006. By then, all producers of electrical and electronic equipment are expected to register.

According to Adrian Harding from the Policy and Regulation at the Environmental Agency, the registration forms contain no less than 13 categories or over 1000 data-fills. However, registering late will be a criminal offence.



Three emerging chip-to-chip interconnection technologies – HyperTransport, PCI Express and RapidIO – are being increasingly integrated into semiconductors and systems, with shipments predicted to grow dramatically over the next several years, reports In-Stat.

PCI Express is expected to experience the highest growth of the three, rising from 8.7 million systems in 2004 to 283 million in 2009. HyperTransport will grow with a CAGR of 28%, fuelled by its success in computing and routing applications, whilst telecom applications require RapidIO, keeping it in third place.

However, In-Stat says, although each interconnect has roadmaps to higher speeds and bandwidth, they all face challenges overcoming jitter using current circuit board technology. These challenges may eventually force a transition to optical interfaces.

Ω

One in four electronics manufacturers have taken a hit on margins to maintain sales levels, says Plimsoll Research. A study into just how desperate to cling on to sales the UK's Top 987 electronics manufacturers have become has revealed that 26% have accepted a reduction in margin or have fallen into loss as a sacrifice for maintaining or increasing sales levels. The study has found that 29% of companies are already selling at a loss, 18% are losing money for the second year, 52% of companies' margins have fallen, 3.3% is the average margin in the industry and 3% is the average return on investment.

Ω

IBM has created a custom chip especially for the Microsoft Xbox 360 games console. The chip is based on three 64-bit PowerPC cores, each with two simultaneous threads and clock speeds greater than 3GHz. It features 165 million transistors and is fabricated using IBM's 90nm Silicon on Insulator (SOI) technology to reduce heat and improve performance. The chip's innovative 21.6GB/s Front Side Bus (FSB) architecture was customised to meet the demanding throughput and latency requirements of the Xbox 360 gaming software.

## OEMs get a single-chip device for entry-level mobile phones and above

The first single-chip GSM/GPRS device packed with everything necessary to make a mobile phone handset has been introduced by Silicon Laboratories. The AeroFone Si4905 contains the analogue and digital basebands, RF circuit and power management unit – circuits that do not necessarily like each other – in a single monolithic IC.

The RF circuitry is typically sensitive to the noisy digital circuits, audio and high power management, even when discrete solutions are used. Bringing all of these in close vicinity would inevitably make matters worse, resulting in degraded RF performance.

The greatest interference mechanism disturbing the RF subsystem is the clocking of the larger digital subsystems such as the DSP and the microcontroller. Coupling mechanisms can result in spu-

rious noise, poor blocking performance, degraded sensitivity, distortion of the output modulation spectrum and other.

"The system partitioning was optimised internally to manage the DSP and MCU MIPS, which has a direct effect on the digital clocking activity that can disturb sensitive RF circuits. Layer one software and DSP algorithms had to be carefully written to help manage this. Specific circuit design and layout techniques were employed to provide isolation and interference attenuation throughout the various blocks of the IC," said James Kimery, marketing director for wireless products at Silicon Laboratories.

Now, the AeroFone promises OEMs to reduce component count from 250 to only 60 to build a complete quad-band handset. External ICs and passive components that typically

accompany the PMU, charging circuit and battery interface, as well as the VC-TCXO, are not necessary with the AeroFone, which has the PMU and DCXO (digitally-controlled crystal oscillator) with the associated software on-board.

Equally, the protocol stack, which is responsible for establishing and maintaining communication with the network, has undergone some changes.



It doesn't get smaller than this – Silicon Laboratories's AeroFone Si4905 in a 12x12mm BGA package

## PMR's days are not over yet

Professional Mobile Radio (PMR) networks including Tetra will continue to exist as long as emergency services do. So says Mike Norfield, managing director of Team Simoco, a Derby-based radio communications firm.

"We believe there's future for the PMR industry. There's no way you'll get an emergency service via a public network. Sometimes the public networks are switched off – as in the case of suspected terrorism, for example."

"With private networks you get full security. It's your network – you control it. When it

comes to public safety they [emergency services] don't like losing control. PMR has found its niche – security, privacy and safety."

PMR has recently gone digital, continuing the trend of digitisation in public networks. "We wanted to give it digital and advanced features," said Norfield, referring to Team Simoco's latest product – the XFin blade trunking system. "XFin is the gateway from analogue to digital."

The XFin technology is a combination of Analog Devices's BlackFin DSP and Intel's processor XScale. The

XFin blade integrates a system controller and base station in just 1U. It uses digital techniques for voice and data communication over an IP backbone and it has its own IP address for remote diagnostics and support. CAT5 Ethernet connectivity allows remote configuration, monitoring and call logging, together with rapid voice and data routing. Wireless connectivity is available using an optional Wi-Fi router. "XFin can be integrated into PABXs, with the Internet and WiMax. We have a unique signalling that we use – and the DSP allowed us to do that."



## Actel introduces ARM core in its FPGAs

The most popular embedded soft core – the 32-bit ARM7 – has found its way into Actel's flash-based FPGAs. "This chip turned out to be the 8051 of the RISC world. We knew for a long time it was the biggest selling and it will remain so for a long time," said Dr Yankin Tanurhan, senior director at Actel. "Now we have added CoreMP7, a soft ARM7 core optimised for use in our FPGAs, which will enable a typical system developer to pick it up and run with it."

The "pick up and run with" aspect does however depend on whether the designer has an ARM licence. "If they have an ARM licence, life's good," said Dr Tanurhan. For those who

don't have a license they'll need to go to ARM. As for the tools, these can be purchased from ARM or, indeed, Actel. "Our RealView Development Kit [originally an ARM develop-



ment tool] licence is significantly cheaper than ARM's," added Dr Tanurhan.

Actel sees an easy route between FPGAs (used mainly for prototyping) and ASICs

(used for large volume production) via its CoreMP7 chip. "With it you don't need to do much to go between FPGAs and ASICs," said Dr Tanurhan.

Even though hard and soft processor cores have been added to FPGAs before, such as the Power PC core in Xilinx's Virtex range and the proprietary Nios in Altera's devices, this is the first time that ARM has been embedded in them. "ARM are happy with our architecture as it is secure enough and no one can tamper with their code," added Dr Tanurhan.

CoreMP7 operates at up to 25MHz.

## Don't worry about China, says boffin

China's growing strength in the electronics sector is not to be feared just yet. So says Dr Mike Tubbs, one of the authors of this year's DTI-funded R&D Scoreboard.

"China is in the early stages of development. They are doing manufacturing very well but not R&D. They are either copying or making already well-known products," said Dr Tubbs, who then added: "I think this will change in the next five or six years."

China did not make it into this year's Scoreboard, even though the focus is on the top 70 sectors globally. "Today, most of them [firms in China] have less than £22m of R&D investment, that's why they didn't enter our report," said Dr Tubbs.

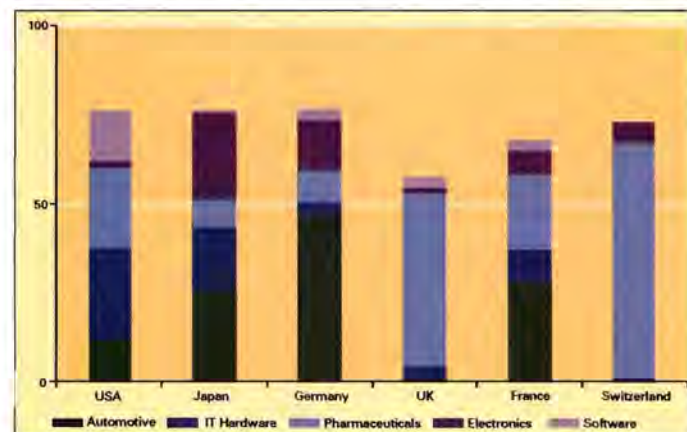
The DTI consultants have already cut the qualifying R&D investment level from £37m to £22m, which allowed an additional 300 firms to be analysed. "We thought we were

cutting out some interesting companies if we focused on such a high level of R&D funding," said Dr Tubbs.

The Scoreboard also highlighted that South Korea was leading with a 40% increase in R&D investment on last year. This country is strong in the automotive and electronics sectors and among its strong representatives are Samsung Electronics, LG Electronics

and Hyundai Motors.

However, no US firms featured in the top ten of R&D investors in the electronics and electrical sector, where R&D investment grew 5% globally. Dr Tubbs believes this is likely to change in the near future. "The US are rather keen on developing military robots. If they decided to invest in that, the electronics and electrical firms will get that funding."



Proportions of the six major countries' R & D, contributed by the five largest global sectors



## Prototyping ASIC/SoC in FPGAs

For all prototypes:

- ▶▶ Always use the biggest capacity, latest FPGA in the fastest speed grade and the package with the most pins. Anything else is false economy.
  - ▶▶ For debug, consider in advance how many and which internal signals you want to observe.
  - ▶▶ Make enough prototypes. Who will want an early functioning version via this prototype (software development, outside partners, potential customers, trade-show demo, etc)?
  - ▶▶ ASIC RTL runs slower in FPGA. Board speed of 25MHz is typical and over 50MHz is hard work. Compromise on prototype speed rather than push FPGA speed too hard.
  - ▶▶ Keep your RTL source "golden" – let the tools convert ASIC RTL into FPGA equivalents rather than change source code.
- If building your own multi-FPGA board:
- ▶▶ For reliability and reduced risk, consider an off-the-shelf board before deciding to build your own.
  - ▶▶ Why prototype standard interfaces? Consider a modular/daughtercard approach to interface to or test bus access.
  - ▶▶ Use intelligence in allocating on-board tracks between FPGAs. You always run out of inter-FPGA connections before running out of logic or RAM.
  - ▶▶ Take care in distributing clocks and resets across multiple FPGAs to minimise skew and keep FPGAs in sync.
  - ▶▶ Use multiple instances of the same FPGA device: mixing families or vendors creates unnecessary partitioning problems.

This month's Top Ten Tips were supplied by John Gallagher (Director of Marketing for ASIC Products) and Doug Amos (Director of European Business Development) of Symplicity Inc. If you'd like to send us your top five or ten tips on any subject, please write to the Editor at

[EWadmin@nexusmedia.com](mailto:EWadmin@nexusmedia.com)





# Medical Devices: Choice and Use

Science and technology bring new medical devices to life. Before they are put to good use in treating patients, hospitals need to address management and quality issues first, says

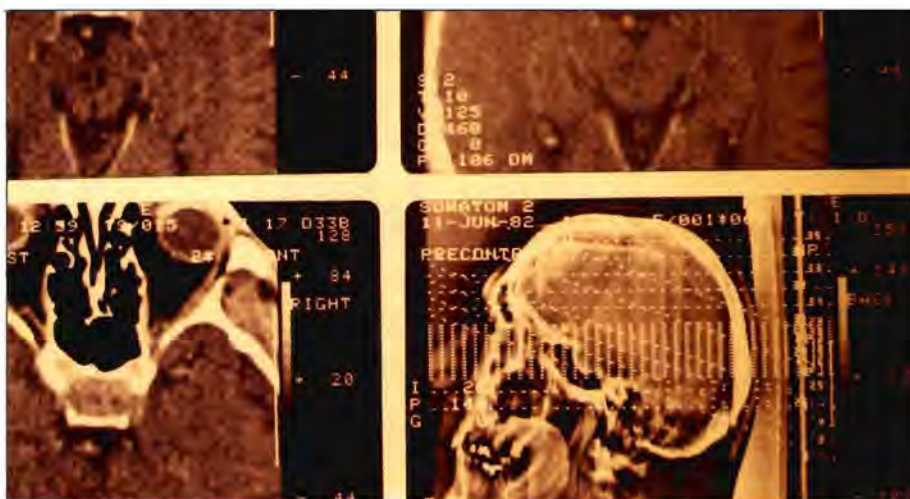
**Dr. G. D. Green**

Computers have been making their impact on medical devices for a long time. Major improvements in diagnosis and treatment came about by the use of X-rays in the development of computer-assisted tomography scanners (CAT or CT scanners), which give three-dimensional pictures of the body.

Likewise, magnetic resonance imaging (MRI) owes its success to the application of computer technology.

Millions of patients have benefited from these two applications alone, not to mention the thousands of other devices made for patient care enabled by science and technology. One other example is a relatively simple and inexpensive device such as the 'pill camera' that can be swallowed by a patient and is now used for wireless-capsule endoscopy. As the camera passes through the patient's body, it photographs the gastro-intestinal tract, and transmits pictures to a receiver outside the body. This device allows the gastroenterologist to examine parts of the body that are otherwise impossible to reach.

Advances and applications of modern science and technology continue unabated. However, when developing and manufacturing such devices it is of highest importance to collect and rely on objective evidence. This is quite different from opinions, which often differ amongst professionals. Good professionals should



*“ Good professionals should always welcome open discussions to obtain the relevant facts ”*

always welcome open discussions to obtain the relevant facts and come to a conclusion as to what is best for patients.

The cost of a device is clearly one factor to be considered, but it rapidly becomes unimportant if in the light of clinical trials the outcomes are not acceptable. The Medronic (of American origin) pacemakers used in Glasgow many years ago cost four times as much as British pacemakers. These were used because their implant lifetime, calculated very carefully from objective evidence, was very good. Hence, Glasgow patients and the Greater Glasgow Health Board had the benefits of fewer pacemaker re-operations. The collection and analysis of 'objective evidence' is key to such decisions.

Another point to be borne in mind when thinking about developing and using medical devices is that expensive ones should be in use, if not round the clock, certainly in evenings and at weekends. When purchasing highly sophisticated medical equipment, hospital manage-

ment needs to ensure that it is fully used.

What is also needed is much better management of our NHS hospitals. The application of ISO 9001 to the whole hospital rather than a few departments would put top management in control. ISO 9001 is not about perfection, it is about getting things right every time. All of us make mistakes from time to time. ISO 9001 is about striving to get things right and striving to do things better – all the time, whether it is in a factory, designing and manufacturing medical devices, or in a hospital, diagnosing and treating patients.

Some half a million medical organisations worldwide already have the ISO 9001 certification.

Oddly enough, the writer does not know of one single NHS hospital that has achieved ISO 9001 certification, although some hospital departments have done so.

*Dr Dennis Green is an international consultant and principal auditor on ISO 9001*



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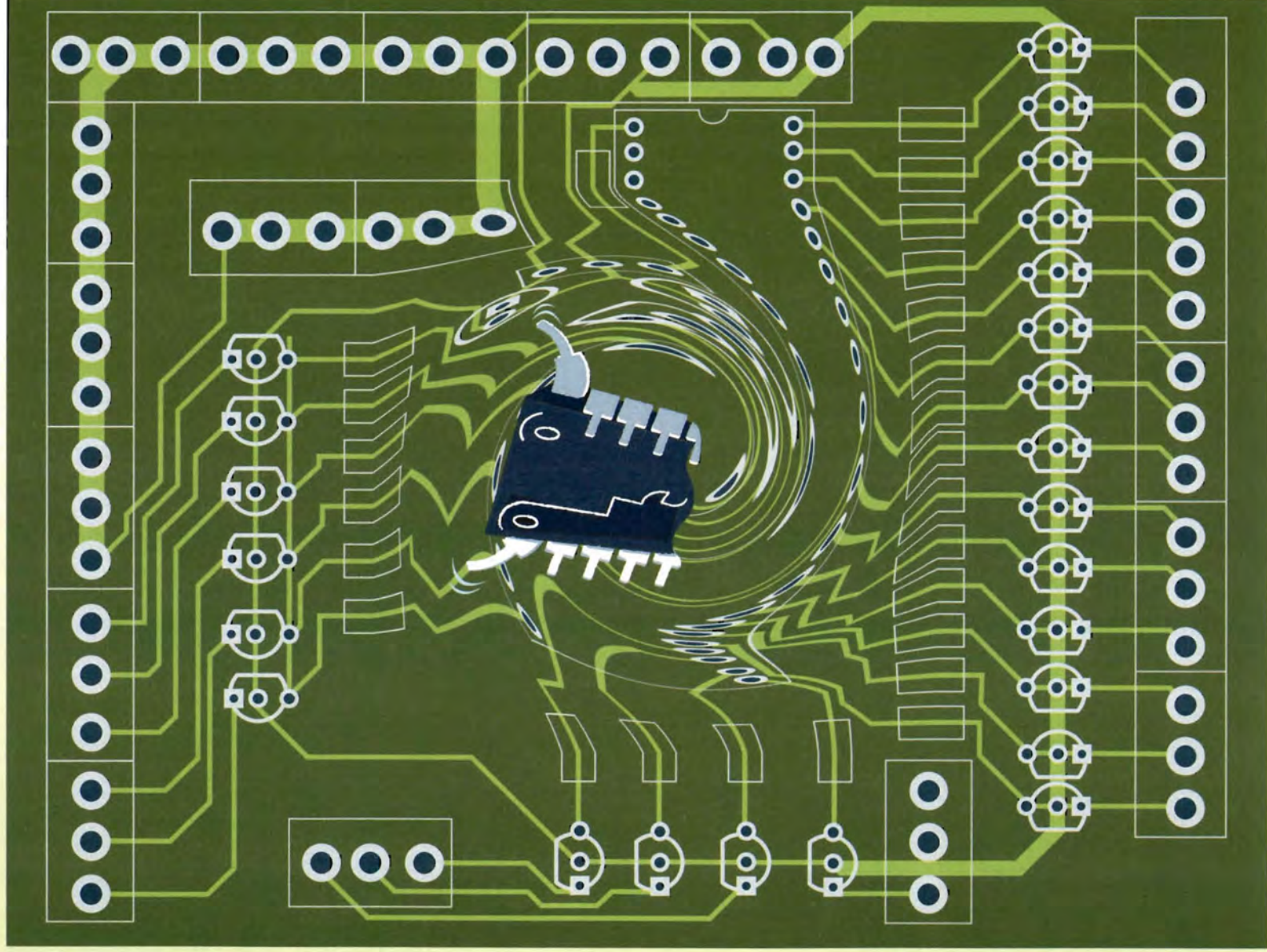
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# The Case of the





# e Vanishing ICs

By Keith Gurnett and Tom Adams

We are so accustomed to seeing components surface-mounted on boards that one's first glance at a board having embedded chips is a bit startling: the surface of the board has no components at all and is featureless, except for a faint rectangular dimple over each embedded IC.

Questions immediately come to mind: is this the end of surface mount? Will reflow ovens become obsolete? Can we gain even more performance per unit area by mounting additional components on top of this naked thing? Are there other advantages to what is being called "vertical miniaturisation?"

The development of board-embedded components has already reached serious levels in work carried out by a European consortium, whose members are cooperating in the Hiding Dies project ([www.hidingdies.net](http://www.hidingdies.net)). Academic and commercial partners are Fraunhofer IZM, the Technical University of Berlin, Nokia (Finland), Philips (Netherlands), AT&S (Austria), Datacon (Austria), CWM (Germany) and IMEC (Belgium). The goal of the consortium is to make the technology feasible and cost-effective for the production of consumer products. In addition, at least one European manufacturer has separately undertaken its own research.

Production of an "embedded" board begins with the board itself, to which components and additional layers are added. Currently, the consortium uses a board having a double-layered core and made from halogen-free FR4 board material, one of the somewhat more costly versions of FR4 that have been marketed in order to meet RoHS requirements. In the next few months, the consortium will begin assembling coreless boards, using two layers of resin-coated copper, or RCC.

An important property of this board material is its relatively high glass transition temperature ( $T_g$ ) of 170, compared to the normal FR4  $T_g$  of about 140. The higher  $T_g$  enables the board to withstand Pb-free reflow temperatures, should reflow be required.

As a first step, the uncut wafer of tested ICs is thinned down to 50 microns, and in some cases less than that. The aluminum contact pads on top of the chip need to be modified to accept microvias that will be formed later. Modification is done by sputtering the pads with 0.2 microns of T/W/Cu, structured by a lithography step, and by reinforcing this metallisation with the electroless deposition of a 5-micron copper layer. This two-step process will eventually be replaced by less costly single-step copper bumping.

After the wafer is singulated, the individual good die is bonded to the board using printed adhesive or die-attach film. It is important at this point to avoid irregularities in the bond line beneath the chip, which must lie perfectly flat, since dielectric layers will later be laid over the chip. "This is a rule from PCB manufacturing," explains Fraunhofer IZM physicist Andreas Ostmann. "You should always try to have a symmetrical build-up; if you don't do that, then you have a warped board."

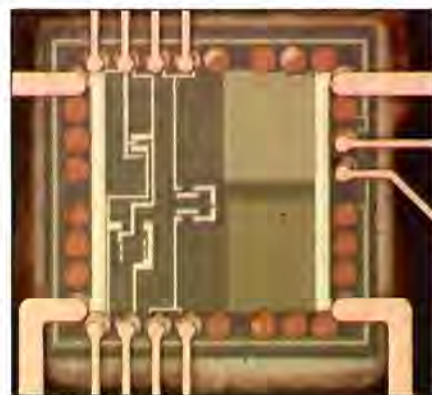
Conventional die-bond equipment places the die. Throughout development, the consortium has used conventional equipment so that existing production lines would be able to move into embedded production without huge investments in new equipment.

In the next step, high-Tg resin-coated copper (RCC) is vacuum-laminated onto both sides of the core. The dielectric thickness of the RCC is 70 microns, while the copper is five microns thick. In the final steps, microvias are drilled down to the bond pads on the chips, and are plated with PCB-compatible copper (see **Figure 1**).

As yet, there is no extensive reliability-data for embedded chips, so – aside from simulations – no one knows how well they will last. But Ostmann points out that the chip being

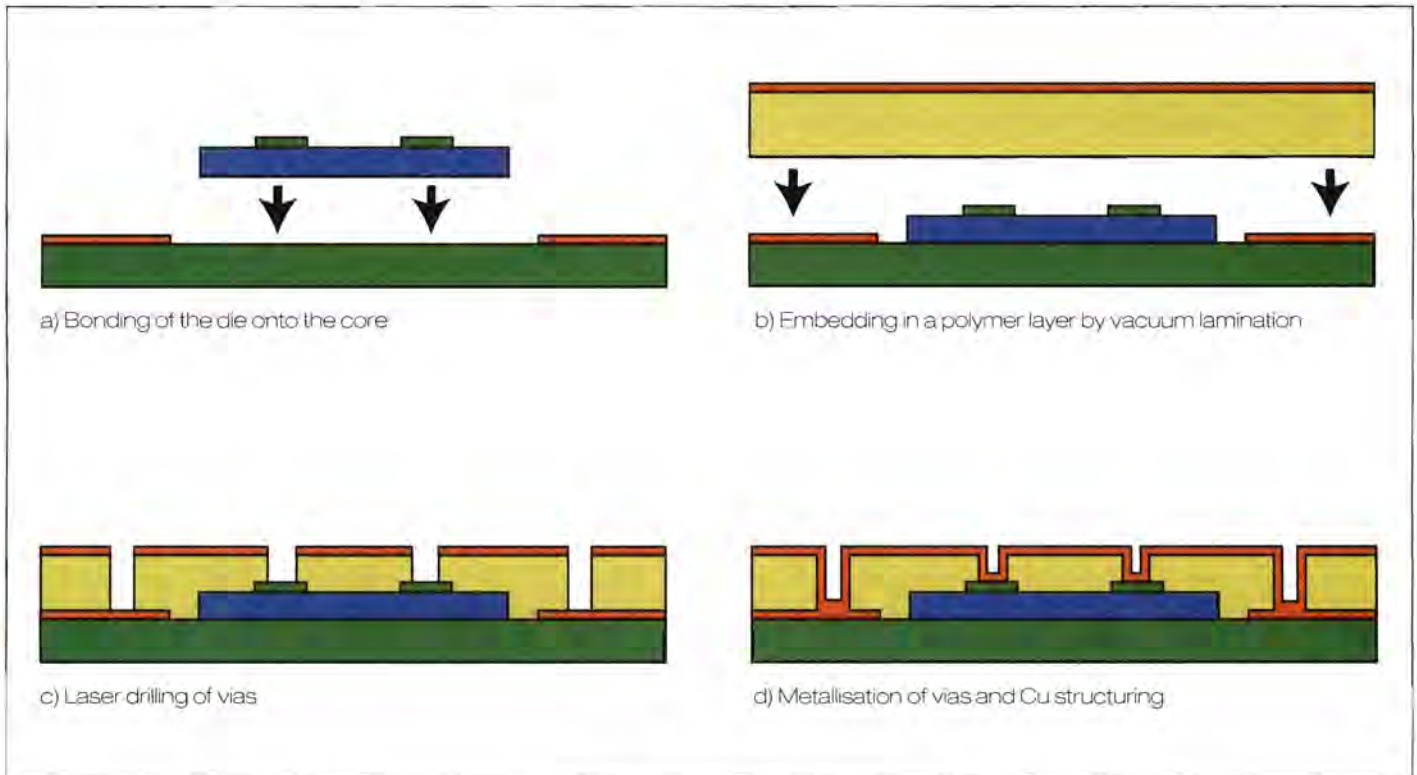
“At AT&S in Austria, they have begun manufacturing the parts on 18 x 24 inch panels. It's still in the engineering phase, but it is now feasible to do this in the production line”  
**Andreas Ostmann, physicist, Fraunhofer IZM**

supported by a polymer on all sides should make the construction fairly rugged. Aside from the lack of wires, he points out that it is not too different from Chip-on-Board assemblies, where the chip is covered by an epoxy glop-top. And Chip-on-Board assemblies,



Embedded chip from Fraunhofer IZM





he notes, are used in low-cost items like handheld calculators, where they have an excellent reliability record.

One of the key factors determining reliability is the response of any electronic assembly to thermal changes. Because they contain layers of woven fibreglass, FR4 boards are, a sort of, thermal oddity – they expand relatively little in the X and Y dimensions, but much more in the Z dimension. To some extent, the boards used to date for embedding have avoided Z-dimension problems by being very thin. But there is always some internal movement during thermal excursions.

"We have discovered some processing tricks," explains Ostmann, "and we have found that after lamination of the RCC on top of the chip that there is a bending of 10 microns, which is acceptable." He also points out that their current designs are inherently asymmetrical because they place chips only on one side of the board. During the next year, they plan to make two-sided boards.

One of the attractions of the embedded concept are the extremely short interconnections. Demands for higher performance can benefit from those short distances, of course, but perhaps not with epoxy FR4 boards, which have relatively high dielectric losses. "The estimate is that at 5GHz that's the limit [for FR4]," Ostmann explains.

However, his group has been working with other materials that have far lower losses.

Although there is as yet no hard data to back him up, Ostmann suspects that the embedded chip design will prove to be remarkably resistant to shock and vibration because of the superb protection provided for the chip. One company interested in the concept is Nokia, for the very mundane but

practical reason that people tend to drop mobile phones on hard surfaces.

It seems likely that good applications for embedded chip designs will include small, performance-driven applications, some of which handheld, like mobile phones. "We do not believe that you will make complicated devices," says Ostmann. A board may have a single chip, somewhat like a flip chip on a substrate, but is not likely to resemble a large motherboard. "Maybe, later on, one single chip, and a smart interposer, and another chip on top as a flip chip." He can foresee applications where a small board might have four embedded chips, but not many more – certainly not as many as 20.

"We have samples now that have passed 1,000 hours of humidity cycling," notes Ostmann. His team is also conducting long-term reliability tests, and testing materials for moisture sensitivity levels. "At ATS in Austria, they have begun manufacturing the parts on 18 x 24 inch panels. It's still in the engineering phase, but it is now feasible to do this in the production line – everything is done with production tools."

It may be possible, after the chips are embedded, to surface-mount passive components, such as resistors and capacitors, on the top of the board. It depends on the amount of space available and on the routing capabilities, which may be limited if there is only one routing layer. But Ostmann points out that several companies are currently developing both thin-film and printable capacitors and resistors that can be placed inside the board layers, effectively placing all of the components out of sight within the board.





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# IV and CV Measurement in Parametric Test

You may be confused as to why you need IV and CV measurements in semiconductors nowadays, but **Alan Wadsworth**, Product Marketing Specialist from Agilent Semiconductor based in Santa Clara, the US, describes why you can't do without them

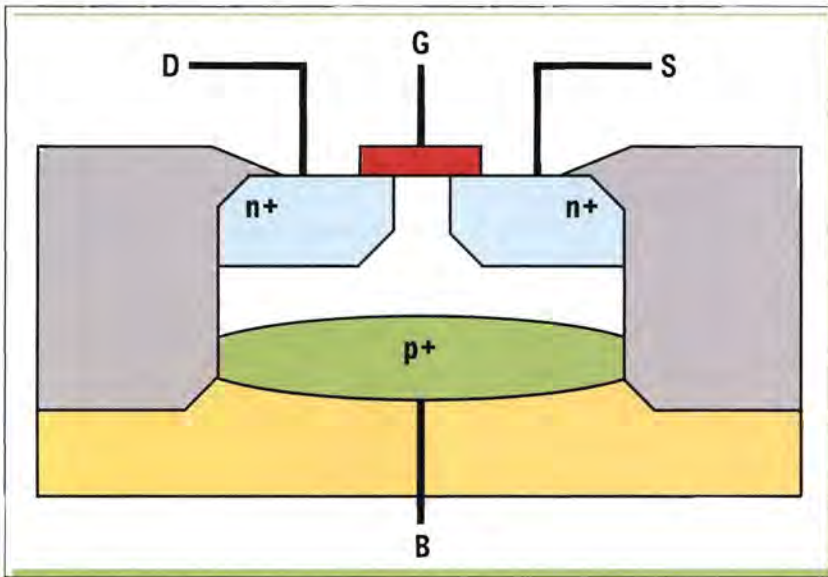


Figure 1: Idealised MOSFET cross-section

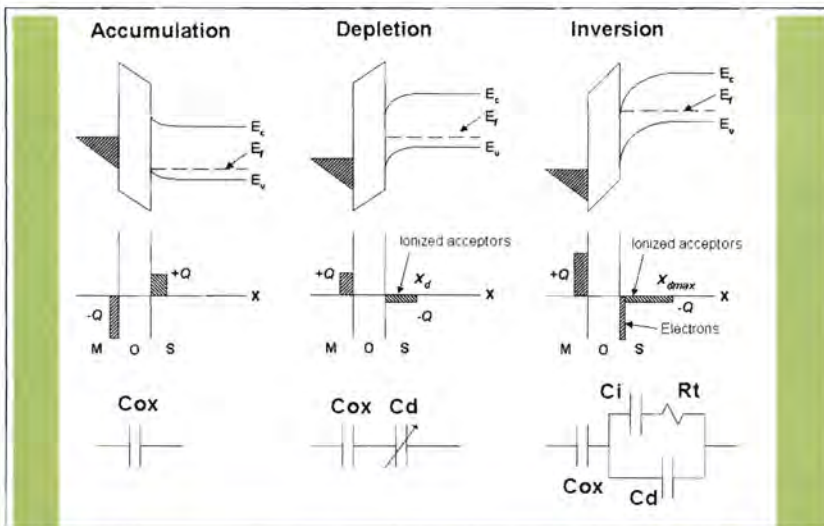


Figure 2: The MOS structure has three states: accumulation, depletion and inversion

Accurate characterisation of modern semiconductor processes requires both current versus voltage (IV) and capacitance versus voltage (CV) measurement. While the need for IV measurement is obvious, the need for CV measurement is less so. To understand why CV measurement is important to the integrated circuit (IC) industry, it is worthwhile to review the structure of a MOSFET (metal-oxide-semiconductor field effect transistor).

Of course, most modern MOSFET devices do not use metal for the gate material and some do not use oxide as the gate insulating material; however, the same physical principles apply, regardless of the exact materials used. **Figure 1** shows a simplified cross-section of an idealised n-channel MOSFET.

When no voltage is applied to the gate, the drain and source regions are isolated from each other and no electrical current can flow. When a sufficiently positive voltage is applied to the gate, channel inversion occurs and the drain and source regions are then connected together (enabling the transfer of electric current). This electrical behaviour is the basis for all of the integrated circuit industry.

The gate is separated from the channel region via a thin insulating layer. The first transistors of this type used metal for the gate and oxide for the insulating material, which gave rise to the term metal oxide semiconductor (MOS). Now, note that the structure of the MOS "sandwich" is very similar to that of a classic parallel plate capacitor. In fact, it turns out that the MOS structure behaves exactly like a capacitor, except that the value of the capacitance depends upon the applied voltage. The MOS structure has three states: accumulation, depletion and inversion as shown in



**Figure 2.** Note that here a p-bulk (NMOS) structure is depicted.

If the silicon is held at ground and a negative voltage is applied to the gate, the MOS capacitor will begin to store positive charge at the silicon surface. The surface density has a greater density of holes than  $N_a$  (the acceptor density). This condition is known as surface accumulation. In this condition, the mobile charge can respond rapidly to changes in applied voltage and the device behaves just like a parallel plate capacitor with a capacitance of value  $C_{ox}$ .

If a positive gate voltage is applied to the gate relative to the silicon, the built-in positive voltage between the gate and silicon is increased. The silicon surface becomes further depleted of carriers as more acceptors become exposed at the surface, resulting in the condition known as surface depletion. In this condition, the total MOS capacitance consists of the series combination of  $C_{ox}$  and the capacitance across the surface depletion region,  $C_d$ . The series combination of these two capacitors (which depends upon applied voltage) results in a total capacitance that is lower than the value of  $C_{ox}$ .

If the positive gate voltage is further sufficiently increased, the energy bands bend away considerably from their levels in the bulk of the silicon. The depletion region reaches a maximum width,  $x_{dmax}$ , and all of the electron acceptors within this region are fully ionised. In the surface region, generation of carriers exceeds recombination and the generated electrons are swept by the electric field into the oxide-silicon interface, where they remain due to the energy barrier between the conduction bands of the silicon and the oxide. Thus, the total charge in the silicon consists of the sum of these two charges. The total MOS capacitance can be modelled as the oxide capacitance in series with the parallel combination of the depletion capacitance and the series combination of inversion charge capacitance,  $C_i$  and the depletion resistance,  $R_t$ .

In the inversion regime, the minority carrier electrons at the oxide surface can only be supplied as fast as they can be generated in the p-bulk material. If an applied voltage is varied slowly enough to allow the generation rate to respond to it, or if a nearby source of minority carriers is made available, then the depletion charge is not a factor in the incremental capacitance. The inversion capacitance is typically much larger than either the depletion capacitance or the oxide capacitance (i.e.  $C_i \gg C_d$  and  $C_i \gg C_{ox}$ ). Assuming  $R_t$  is negligible, basic circuit theory shows that, in this case, the total capacitance is very close to the value of the oxide capacitance,  $C_{ox}$ . This is typi-



**Figure 3:** QSCV and HFCV curves

cally referred to as quasi-static CV (QSCV) behavior. However, if the applied voltage is varied too rapidly or there is not a nearby source of available minority carriers, then the electrons cannot respond and the depletion charge must modulate in response. The inversion charge cannot form, so once again the total capacitance consists of the series combination of  $C_{ox}$  and  $C_d$ . This is typically referred to as high-frequency CV (HFCV) behaviour. The appearance of these two plots is shown in **Figure 3**.

### Extracting the physics

From device physics considerations, many of the important physical characteristics of the MOSFET can only be extracted after first plotting the capacitance versus voltage curve of the MOS structure. Typical parameters extracted from this data include gate oxide thickness ( $t_{ox}$ ), substrate impurity concentration ( $N_{sub}$ ), flat-band capacitance ( $C_{fb}$ ), flat band voltage ( $V_{fb}$ ), surface charge density ( $Q_{ss}$ ), and threshold voltage ( $V_{th}$ ). All of these parameters affect the behaviour of the MOSFET device, so understanding their values is important to determining if a semiconductor process is meeting its design targets.

With a basic understanding of the significance of CV measurement to parametric test, it is now important to understand the measurement challenges that CV measurement presents. The first point to comprehend is that capacitance measurement requires an AC signal as opposed to the DC signals used for the IV portion of parametric



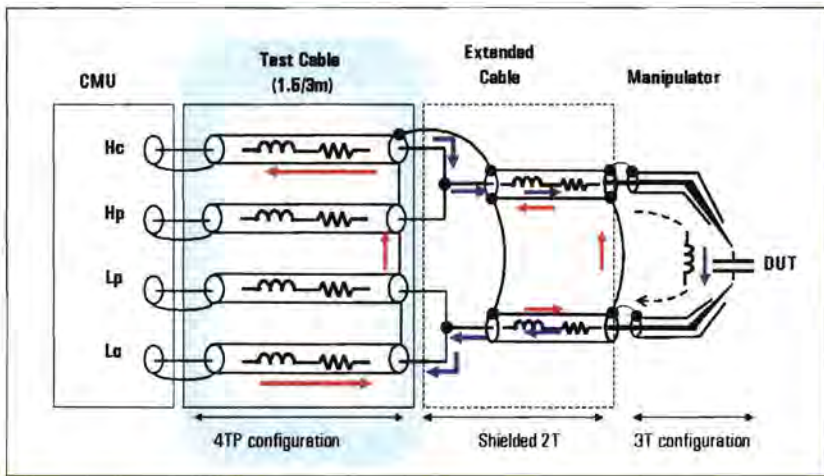


Figure 4: Capacitance current return path issue

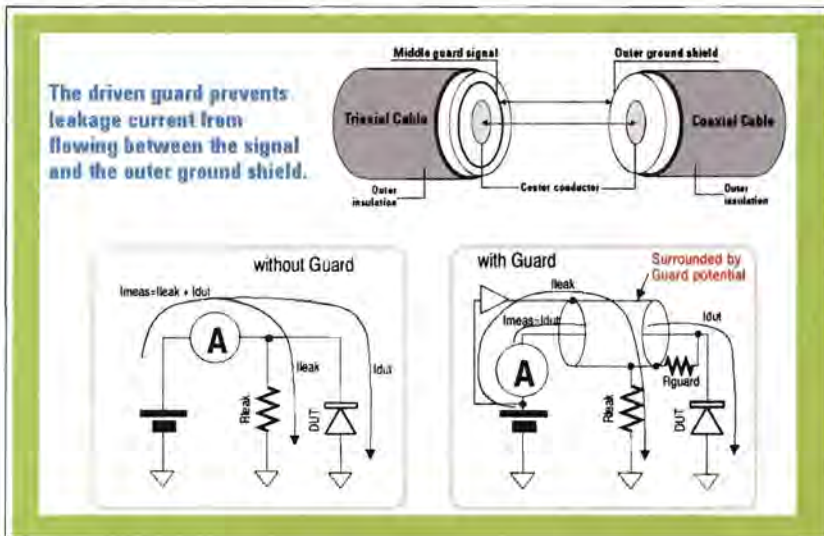


Figure 5: Measurements down to attoamps are possible using triaxial cables current

test. This arises from the fact that capacitance only has significance for AC measurements, as illustrated by the fundamental relationship between capacitance, current and voltage shown in Equation 1.

$$i = c \frac{dv}{dt} \quad (1)$$

### Understand the cables

The dependence of capacitance measurement on an AC signal (typically a sine wave) introduces several new factors of measurement complexity. The most important single issue is that the length of the cable coming from the capacitance measurement unit (CMU) to the device under test (DUT) has a significant impact on the capacitance measurement. Any measurement cable possesses some innate capacitance per unit length, and this

capacitance will distort the total capacitance measured by the CMU, unless this distortion is somehow "compensated". The process of compensation is simply a mathematical operation performed on the measured capacitance values to remove the effects of the cable capacitance.

In addition to compensating for the cable length, there is one other factor that is often ignored by many otherwise experienced engineers. This is the issue of capacitance current return path (refer to Figure 4). The CMU will inject current (shown as blue arrows) into the capacitor under test. If the "Extended Cable" portion of the cabling setup has its outer ground shields connected together close to the DUT, so as to create a "Shielded 2 Terminal Pair" or Shielded 2T configuration (as shown), then an induced current (shown as red arrows) will flow through the ground shield in opposition to the injected current. This induced current flow seals the magnetic flux and stabilises the series inductance of the Extended Cable. Making this outer ground shield connection is crucial, since if this is not done, the induced current cannot flow and the series inductance of the Extended Cable will vary randomly with the spatial arrangement of the cables. In this case, large fluctuations in the effective cable inductance can occur.

These fluctuations affect the capacitance compensation, which in turn affects the accuracy of the capacitance measurement. Therefore, it is also important to have the outer ground shields of the measurement cables connected together close to the DUT and, unless this is done, the inductance instability will become worse and worse as you measure at higher frequencies.

The source/monitor unit (SMU) utilised for the IV portion of parametric test use triaxial cables. As the name implies, these cables have three layers: a centre force/sense line, a middle guard and an outer ground shield. The reason that SMUs use triaxial cables rather than BNC cables is as follows. Ultra-low current measurements (down to the femtoamp range) are not possible using BNC cables for the simple reason that no insulator is perfect. Leakage currents between the inner conductor and the outer ground shield of a BNC cable limit these types of cables to measurements of 1nA or greater. However, the triaxial cable isolates the inner conductor from the outer ground shield via a middle guard shield. The SMU has an active circuit that always keeps the voltage potential of the driven guard the same as that of the inner conductor. Since there is no voltage difference between the driven guard and the inner conductor, by Ohm's Law there can be no leakage current (the voltage difference = 0V). Therefore, using triaxial cables current measurements down



to even the sub-femtoamp (attoamps) range are possible (refer to **Figure 5**).

One issue with integrating IV and CV measurements is that these two types of measurement resources (SMU and CMU, respectively) do not use the same types of cables and, hence, have incompatible connectors. SMUs use triaxial cables and CMUs use BNC cables. Since (as already explained) parametric measurements require both types of measurements, this has been an unpleasant problem for engineers involved in parametric test. One solution is to use an external switching matrix, which takes care of converting between the two connector types. However, especially for positioner-based wafer probing setups, a switching matrix adds a lot of expense and complexity. It also introduces additional issues with capacitance compensation (since the user then has to compensate for the additional path length through the matrix).

### Supporting parametric test

The B1500A supports a single-slot, multi-frequency capacitance measurement unit (MFCMU). Besides integrating CV measurement into the device analyser mainframe, the MFCMU possesses many measurement capabilities not available on comparable external capacitance meters. The MFCMU can measure capacitance at up to 5MHz and it can also provide  $\pm 25V$  of dc bias. In addition, the combination of the MFCMU and SMUs within the same instrument enables these measurement resources to be more tightly coupled. When joined using the B1500A SMU CMU Unify Unit (SCUU), the MFCMU and SMU combination supports capacitance measurement with  $\pm 100V$  of dc bias. The SCUU is shown in **Figure 6**; its form factor coincides exactly with the CMU and two of the SMUs.

The B1500A SCUU accepts a cabling fixture that connects to two of the SMUs and to the MFCMU. The cable assembly connects to the SCUU, which is typically located close to the DUT. The outputs of the SCUU consist of two pairs of Kelvin (Force and Sense) triaxial connections, which connect directly to the wafer prober positioners. A Guard Switch Box (GSWB) unit connects to the SCUU via another cable and the GSWB then connects to the outer ground shields of the wafer prober positioners. **Figure 7** shows schematically how the B1500A SCUU enables you to switch between CV and IV measurement without having to change any cables.

Once these simple connections are made, the B1500A software takes care of all of the IV-CV switching, compensation and capacitance measurement current return path issues. You only



Figure 6: B1500A SMU CMU Unify Unit (SCUU)

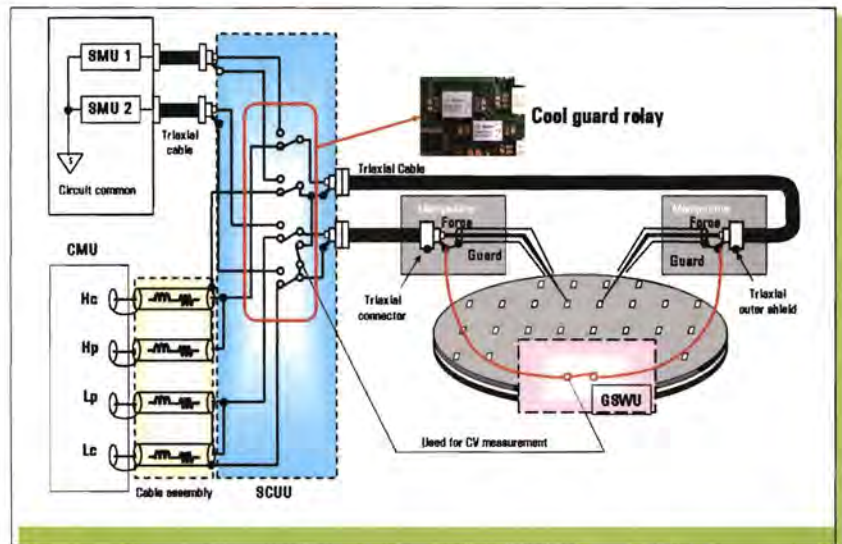


Figure 7: Schematic of how the B1500A SCUU can enable you to switch between CV and IV measurement without having to change cables

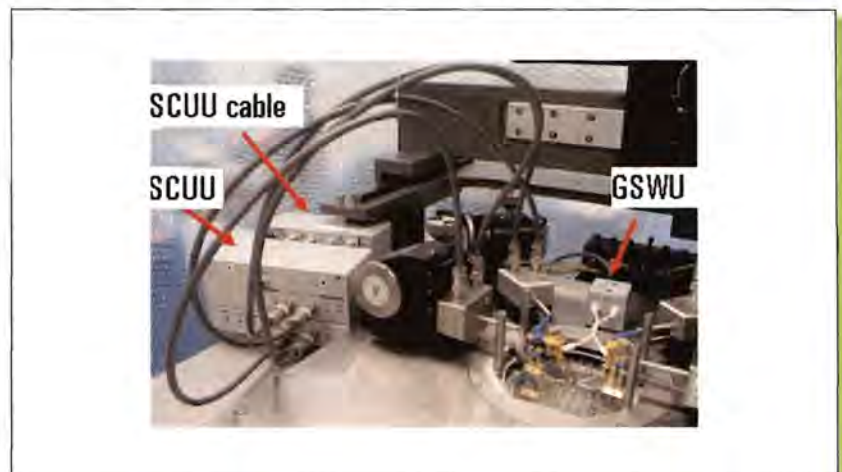
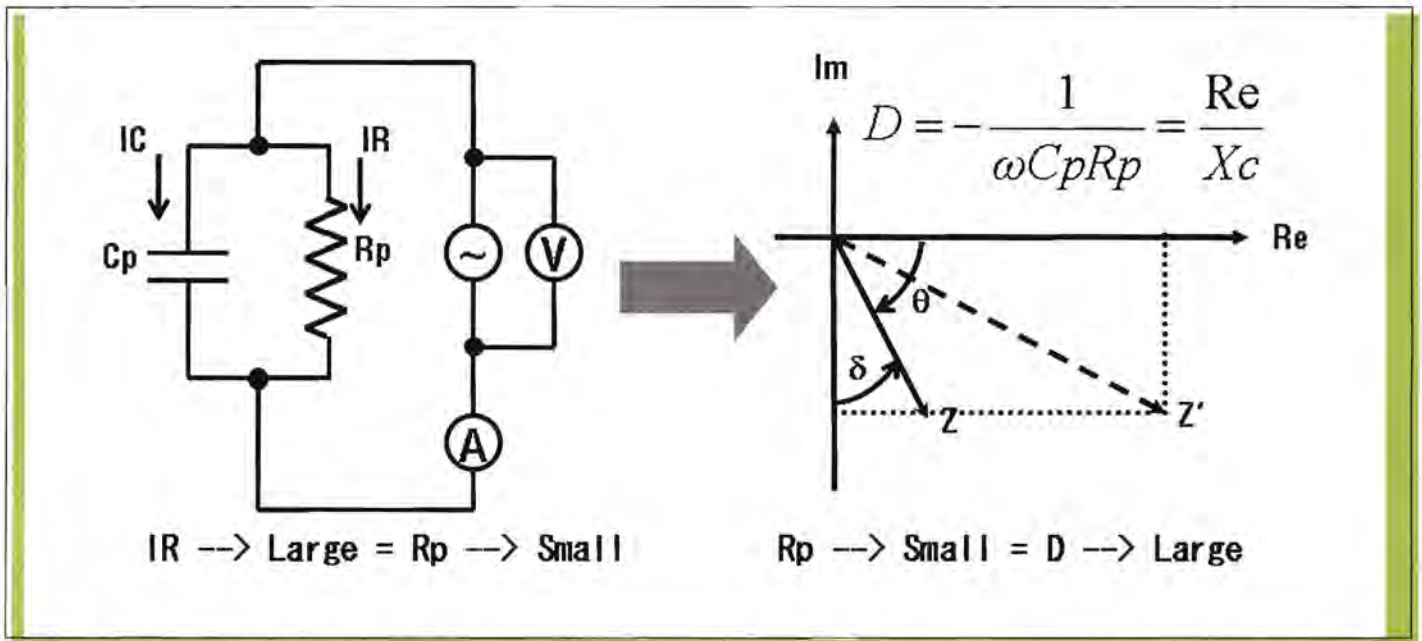


Figure 8: Connecting the SCUU and GSWB on an analytical wafer prober





**Figure 9:** The effect of electron tunnelling is typically modelled as an additional resistance in parallel with the standard device capacitance

have to select an IV or CV algorithm and push a button in order to begin making accurate measurements.

**Figure 8** shows how you would connect the SCUU and GSWU on an analytical wafer prober. By mounting the SCUU close to the DUT, you minimise the additional cable lengths going from the SCUU to the positioners. This, in turn, reduces the deleterious effects of excessive cable length on the CV measurement. The B1500A has built-in OPEN-SHORT-LOAD routines that support calibration of the entire measurement system down to the tips of the probes.

### Thin gate dielectrics

Many modern MOSFET devices have extremely thin gate dielectrics (less than 20 Angstroms). These devices introduce additional challenges for CV measurement. Thin gate dielectrics no longer act as insulators due to the quantum mechanical effect of electron tunnelling through the insulating gate material. The effect of this electron tunnelling is typically modelled as an additional resistance in parallel with the standard device capacitance as shown in **Figure 9**. The Dissipation Factor, D, is a commonly used metric to evaluate the quality of a capacitance measurement. Values of D much higher than 1 indicate problems with the capacitance measurement. The only means to reduce the value of D for thin gate dielectrics is to increase the measurement frequency, since **Figure 9** also shows that D is inversely proportional to the measurement frequency.

The B1500A CMU has a maximum frequency of 5MHz. This enables the B1500A to measure a broader range of devices than the typical LCR meter, which usually only goes to 1MHz or 2MHz. However, for measurements beyond 5MHz it is not possible to obtain good quality results through any sort of switching relays; a direct connection to the measurement equipment is required.

Moreover, standard DC probes also no longer give satisfactory measurement results beyond 5MHz. For measurements beyond 5MHz, RF style probes with a GROUND-SIGNAL or GROUND-SIGNAL-GROUND type of probe are necessary. Therefore, for thick to medium thickness gate dielectrics requiring frequencies up to 5MHz, the B1500A CMU provides a single-box, integrated measurement solution.

For thin gate dielectrics requiring frequencies greater than 5MHz, a tool like Agilent's 4294A Precision Impedance Analyser can help tremendously, which can go up to 110MHz. The 4294A can be controlled from the B1500A EasyEXPERT software interface.





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# IC Wafer Fault Elimination System

Inspecting semiconductor wafers that contain thousands of components poses a great challenge for inspections, but there's a way around that, says **Mike Phillips**

**M**any resistor manufacturers such as State of the Art Inc, supplier of thick and thin film resistive components to the biomedical, communications, aerospace and defence industries based in Pennsylvania, US, have a bottleneck in their production processes when it comes to quality control inspections of wafers. Wafers are an array of resistors made from a blank alumina substrate, which is sputtered with tantalum nitride and gold to a pattern made by UV light being shone through a glass plate onto the receptive material.

According to Chris Pezanowski of State of the Art: "There may be many tiny defects in each wafer, such as voids and bridging, which are caused by contamination by fibres in the production process. There are also other defects, such as scratches, which can be caused during handling."

"At the moment, each wafer is inspected by the human eye through a microscope and this is a highly labour-intensive process. Where there are single wafers with several thousand components, an operator may only be able to inspect one or two wafers a day and there is always the risk of human error as operators tire. We need inspection to be carried out to repeatable exacting company standards and far quicker than is possible at present, with labour re-allocated to other production departments."

### Checking for defects

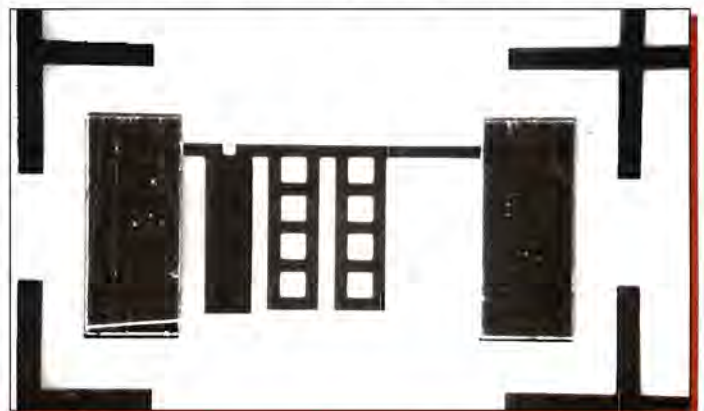
Envisage Systems, the makers of the CAPVIS visual inspection system, have come up with a new, low-cost wafer inspection module, which enables electronic component manufacturers, like State of the Art, producing ceramic or silicon wafers to automatically inspect each wafer optically for faults. Typical defects such as broken or breached tracks, scratches, extra material or contamination can be detected, without human intervention and to exact, repeatable, company standards. The system is available with or without an integrated faulty chip destruction laser. The complete system including laser will typically cost in the region of \$87,000, or \$55,000 without the laser.

The system consists of a wafer movement mechanism – an X/Y table fitted with a robust overhead gantry for the mounting of the high resolution industrial camera and laser equipment, high magnification optics, twin light sources (rear and top illumination), Yag laser, protective shielding for the marking and inspection area and an industrial 19" cabinet for housing all the system electronics and the control PC.

The operator will log into the system and enter wafer related information. This process will automatically load the parameters required for the wafer to be inspected as well as setting up the file structure required for the storage of inspection results. The wafer will then be loaded in to the custom-built location jig.

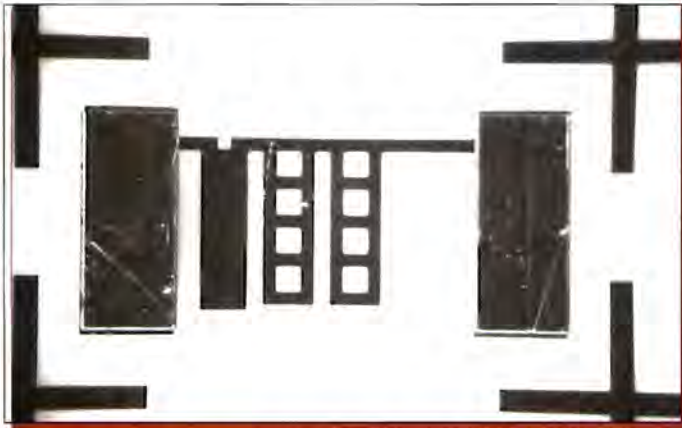
The system will automatically move the jig to inspection position one (this position will be dependant on chip size), where the operator will be asked to confirm that the part is correctly located under the camera. A fixture fine-adjustment menu will be available, should any small adjustments be necessary at this stage. As soon as the position is confirmed, the system will commence its inspection cycle, which will involve following a pre-programmed pattern as dictated by the control PC. At each chip position the camera will either take a single image or up to four images (if necessary, in order to get the required resolution), which will be quickly processed to identify defects. As soon as a pass or fail result is determined, the system will move on to the next inspection position.

Any fail results will be written to a file for subsequent device destruction. It is intended to have a third result category, which will contain images, and



Photos: Microscopic faults in IC wafers





this may require some manual intervention in order to arrive at a pass/fail decision. These images will be presented to the operator at the end of the inspection cycle at which time he/she will be expected to either set a pass or fail the units. The failure results will be written to the destruction file.

### To keep or destroy

Once results are available for all components, the wafer will be moved to a static laser position. The co-ordinates of all failed components will then be fed to the laser, which by means of its scanning head will destroy all faulty units. The scanning head option has been chosen to minimise the time of the destruction cycle as it negates the requirement to move the wafer once it is in its set position. The actual laser mark only takes a fraction of a second and will be programmed with a known pattern, in order to cause maximum destruction.

A warning device will signal to the operator that action is required. This will mean that the operator is free to complete other duties whilst the inspection cycle is taking place. A mode will be available which will store all device images so that the system can be checked for efficient operation, although it is strongly recommended that the system is not left in this mode due to the high storage medium requirements.

During initial tests, a dual lighting system has proved to be the most effective at identifying the defects. This means that mounted immediately beneath the location jig will be a rear light source. This will be a flat LED device, designed to give completely even illumination over the complete field of view. This will be supplemented by a second light source mounted from the lens of the camera. These lights will be switched on and off as necessary by the system.

The camera moves from component to component, building up a map, in memory, of any faulty components. When the inspection is complete, the wafer moves to the destruction position under the laser, which fires a series of tiny pulses to destroy the faulty components and prevent them from con-

tinuing in the production process.

Because of the vast number of unit designs, it is not practical or cost-effective for the vision system supplier to pre-program all of the available variations. The software has, therefore, been designed to enable the end user to program individual component designs into the system. This has been achieved by evaluation of many different drawings of components and establishing that all designs are based on what are essentially common components. Typically, these will include simple tracks, lad-

ders, solid blocks etc.

Once a suitable defect detection algorithm has been written for the individual sub-component type and all of the relevant parameters have been extracted to appear as operator variables (supplied with the system), this may be applied to any area of the device by simply defining the area around that particular feature and setting the relevant parameters for the level of defect detection requirement. This means that similar features can be inspected to different quality levels by setting different parameters for different parts of the device.

### The proof is in the pudding

A checking mechanism is built into the software, which will run a test once an area has been assigned, in order to ensure that the vision check will work as it is supposed to. This overcomes the potential problem of an operator including, for instance, part of a solid block within a ladder section. Once all of the sections have been applied and the parameters set, the component design is automatically saved and can be recalled by use of a simple on-screen drop down list.

According to Envisage Systems: "This new system closes the loop on the inspection process for those companies yearning to produce perfect, zero defect chips. Instead of the labour-intensive process of an operator having to inspect each wafer with a microscope, this system, which has a cycle time of only 15 minutes per wafer, depending on component size, can be operated virtually unmanned, saving both time and manpower. Users can then employ our integrated laser or use the co-ordinate map output function to mesh with their own existing laser destruction system."







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# PC-to-PC Communication via RS-232 Serial Port Using C

**Varun Jindal** from the Panjab University's Institute of Engineering and Technology delves into programming via an RS-232 port in C



An endeavor has been made in this article to bring forth a simple, easy and novel way of implementing PC-to-PC communication via RS-232 serial port using C language. Implementing the asynchronous serial communication this way does not require the reader to be familiar with serial port registers and their programming, and there is no need for constructing user-defined functions for setting the baud rate and format of data, parity and stop bits. Moreover, the speed of data transfer is also greater and the function used for serial programming along with its arguments makes its purpose self-explanatory.

A PC can accommodate, at most, four serial ports but usually a PC has two RS-232 serial ports, COM1 and COM2. Any one of the serial ports can be used in each PC for linking them together. A serial port at the back of a PC is in the form of 9-pin (or sometimes 25-pin) D-type male connector.

**Table 1** shows pin configurations of 9-pin D-type male connector, which is depicted in **Figure 1**.

## Serial communication

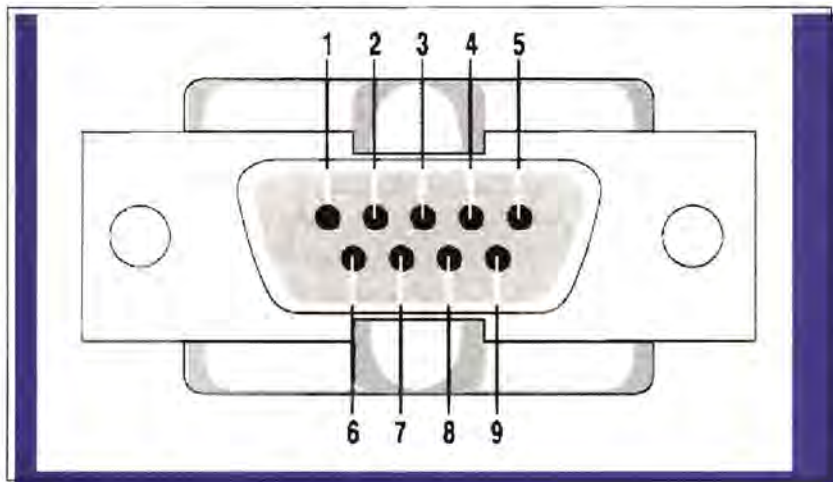
Data transfer within a system is generally in parallel. All the bits of the data word are transferred in parallel at the same instant. In some cases, particularly in transferring data over long distances, it is preferred to transfer the data in serial form. The data word from a transmitting system is converted to stream of bits by parallel to serial conversion, and one bit at a time is transferred on a single line to a receiving system. At the receiving end, the word is reconstructed by serial to parallel conversion. The speed of data transfer in serial communication is specified by baud.

The baud unit is named after Jean Maurice Emile Baudot, who was an officer in the French Telegraph Service. He is credited with devising the first uniform-length 5-bit code for characters of the alphabet in the late 19th century. What baud really refers to is modulation rate or the number of times per second that a line changes state. This is not always the same as bits per second (bps). If we connect two serial devices together using direct cables then baud and bps are, in fact, the same. But when modems are in question, this isn't the case.

### Asynchronous serial communication

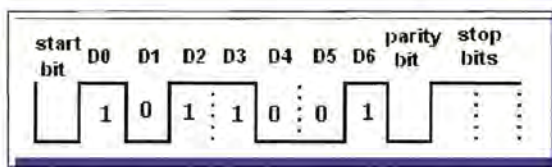
Asynchronous data transfer is used for low speed communication, typically at standard rates such as





**Figure 1 (Above):** 9-pin D-type connector of an RS-232 serial port

**Figure 2 (Left):** Asynchronous data transmission format



2400, 4800, 9600, 19200 baud etc. The asynchronous communication format does not use any synchronising clock or timing signal.

**Framing** – Transmission of a character starts with a start bit (logic 0), followed by the character bits (LSB first), a parity bit and ends with one or two stop bits (logic 1). This is referred to as one frame. Process of adding the start, parity and stop bits with character bits is referred to as framing. When no character is sent, the transmitter outputs logic high. The line remains in logic 1 (idle state) till the transmission of next character begins with another start bit. **Figure 2** shows transmission of a 7-bit ASCII character 'M'.

The parity bit is included in the frame for the receiver to check errors that may occur during transmission. The bit is made 0 or 1, so that the number of 1s in the character plus the parity bit is always odd in odd parity systems or even in even parity systems. Since, the character 'M' has even

**Table 1: Pin functions of a 9-pin connector of RS-232 serial port**

Pin number	Description
1	DCD (data carrier detect)
2	RxD (receive data)
3	TxD (transmit data)
4	DTR (data terminal ready)
5	GND (signal ground)
6	DSR (data set ready)
7	RTS (request to send)
8	CTS (clear to send)
9	RI (ring indicator)

number (4) of 1s, the parity is made 0 for the even parity system and 1 for the odd parity system.

**Error detection** – Error in asynchronous communication is detected in three ways, by checking parity error, framing error and overrun error. The parity error informs that the received data has wrong parity, indicating that the noise was encountered during reception. The framing error informs that the received data does not have the start and stop bits at their proper places. The overrun error indicates that a new data has been received before the previous data could be taken away.

## RS/EIA-232

Short for Recommended Standard-232, a standard interface approved by EIA (Electronic Industries Association) for connecting serial devices, specifies signal voltages, signal timing, signal function, a protocol for information exchange and mechanical connectors. To ensure reliable communication and to enable the interconnection of equipment produced by different manufacturers, the interfacing standard RS-232 was set by EIA in 1960. Since then it has gone through a number of modifications, including a change in its name. RS-232A, RS-232B, RS-232C, EIA-232D and EIA-232E are the subsequent versions of this standard. The standard has been referred to as RS-232 (instead of EIA-232) throughout this article due to its popularity.

The RS-232 standard supports two types of connectors – a 25-pin D-type connector (DB-25) and a 9-pin D-type connector (DB-9). The type of serial communications used by PCs requires only nine pins, so either type of connector will work equally well. Since modern PCs employ only 9-pin D-type connectors, only this configuration has been discussed in this article, including connections and programming.

In RS-232 parlance, the device that connects to the interface is called Data Communications Equipment (DCE) and the device to which it connects is called Data Terminal Equipment (DTE). This standard was mainly designed to connect DTE that is sending and receiving serial data (such as a computer) and DCE that is used to send data over long distances (such as a modem).

### To distinguish between DTE and DCE:

- Measure the DC voltages between (DB-9) pins 3 and 5 and between pins 2 and 5. Be sure that the black lead is connected to pin 5 (GND) and the red lead to whichever pin you are measuring.
- If the voltage on pin 3 (TxD) is more negative than -3V, then it is a DTE, otherwise it should be near zero volts.
- If the voltage on pin 2 (RxD) is more negative than -3V, then it is a DCE.
- If both pins 3 and 2 have a voltage of at least 3V,



then either you are measuring incorrectly, or your device is not a standard RS-232 device. Call technical support.

- In general, a DTE provides a voltage on TxD, RTS & DTR, whereas a DCE provides voltage on RxD, CTS, DSR & DCD.

## Programming an RS-232 serial port using C Library File Inclusion

```
#include<bios.h>
```

### Function

```
_bios_serialcom();
```

### Function Declaration/Syntax

```
Unsigned _bios_serialcom(int cmd, int port, char  
abyte);
```

### Brief Description

The function `_bios_serialcom()` uses BIOS interrupt 0x14 to perform various RS-232 communications over the I/O port given in the port. The function arguments along with their significance are given in **Table 2** below.

**Table 2: Various function arguments and their significance**

Argument	Significance
abyte	OR combination of bits that specifies COM port settings
cmd	Specifies the I/O operation to perform
port	Identifies the I/O port

### Function Argument Specifications

**Port argument** – The serial port that is selected for RS-232 communication is specified in the port argument as given in **Table 3**.

**Table 3: Port argument specification**

Value of 'port' argument	Port selected
0	COM1
1	COM2
2	COM3
3	COM4

**Cmd Argument** – The I/O operation to be performed is specified by means of 'cmd' argument as given in **Table 4**. When the value of 'cmd' argument is set to either `_COM_RECEIVE` or `_COM_STATUS`, the value in 'abyte' argument is ignored.

**Abyte argument** – When the value of 'cmd' argument is set to `_COM_INIT`, the COM port settings are specified by the 'abyte' argument. The 'abyte' argument is an OR combination of the following values (one from each group in **Table 5**).

**Table 4: Cmd argument specifications**

Value of 'cmd' argument	Function performed
COM_INIT	Sets the communication parameters to the value in 'abyte' argument
_COM_SEND	Sends the character in 'abyte' argument out over the communications line
_COM_RECEIVE	Receives a character from the communications line
_COM_STATUS	Returns current status of the communications port

**Table 5: Abyte argument specifications**

Value of 'abyte' argument	Meaning
_COM_CHR7	7 data bits
_COM_CHR8	8 data bits
_COM_STOP1	1 stop bit
_COM_STOP2	2 stop bits
_COM_NOPARITY	No parity
_COM_ODDPARITY	Odd parity
_COM_EVENPARITY	Even parity
_COM_110	110 baud
_COM_150	150 baud
_COM_300	300 baud
_COM_600	600 baud
_COM_1200	1200 baud
_COM_2400	2400 baud
_COM_4800	4800 baud
_COM_9600	9600 baud

### Return value

For all values of 'cmd' argument, the function `_bios_serialcom()` returns a 16-bit unsigned integer.

The upper 8 bits of the return value are status bits.

- ✓ If one (or more) error status bit(s) is (are) set to 1, an error has occurred.
- ✓ If no error status bit is set to 1, the byte was received without error.

The lower 8 bits vary depending upon the value of 'cmd' argument specified as given in **Table 6**.

The following format shows the details of all the return bits:

#### Lower Byte of Return Value

- D0 = Received line signal detect
- D1 = Ring indicator
- D2 = Data set ready
- D3 = Clear to send
- D4 = Change in receive line signal detector
- D5 = Trailing edge ring indicator
- D6 = Change in data set ready
- D7 = Change in clear to send

#### Upper Byte of Return Value

- D8 = Data ready



**Table 6: Significance of lower byte of return value**

Value of 'cmd' argument	Lower 8 bits of return value
<code>_COM_INIT</code> or <code>_COM_STATUS</code>	Lower bits are defined as shown in format given below.
<code>_COM_SEND</code>	...
<code>_COM_RECEIVE</code>	Byte read is in the lower bits of the return value (if there is no error i.e. no upper error-bits are set to 1)

- D9 = Overrun error
- D10 = Parity error
- D11 = Framing error
- D12 = Break detect
- D13 = Transmit holding register empty
- D14 = Transmit shift register empty
- D15 = Time out (set to 1 if a byte value could not be sent)

### Description steps

**1. Objective** – To implement PC-to-PC communication by inputting the data through one port and receiving the same through another and vice-versa (Turbo C++ version 3.0).

**2. Connection diagram** – The connection diagram (Figure 3) shows the wiring of the null-modem that is intended for RS232 asynchronous communications (most PC-based systems). This configuration is called so because each PC terminal detects as if some modem is connected to it rather than the other PC.

The two PC terminals are connected through TxD, RxD and GND pins. The Data Terminal Ready (DTR, pin 4) is looped back to Data Set Ready (DSR, pin 6) and Data Carrier Detect (DCD, pin 1) on both PCs. When DTR is asserted active, then the DSR and DCD immediately become active. At this moment, the computer thinks the virtual modem to which it is connected is ready and has detected the carrier of the other modem. The lines Request to Send (RTS, pin 7) and Clear to Send (CTS, pin 8) have been linked together. When the computer wishes to send data, it

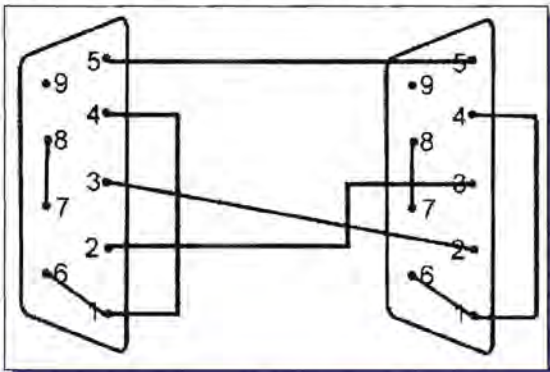


Figure 3: Null modem cable configuration

### 3. Source code

```

/* PC-to-PC communication – by VARUN JINDAL */
/* B.E. (E&C) - final year, Panjab University, Chandigarh */
#include<stdio.h>
#include<conio.h>
#include<bios.h>

#define SETTINGS (_COM_9600 | _COM_CHR8 | _COM_NOPARITY |
COM_STOP1)
/* baud rate = 9600, 8 data bits, no parity bit, 1 stop bit */

void main(void)
{
    unsigned in,out,status;
    int port;

    clrscr();
    printf("Select Port(Enter '0' for COM1 and '1' for COM2):");
    scanf("%d",&port);
    printf("Press ESC to exit");
    textcolor(YELLOW);
    printf("\n\rData Received:");

    _bios_serialcom(_COM_INIT,port,SETTINGS);

    for(;;)
    {
        status=_bios_serialcom(_COM_STATUS,port,0);
        if (status & 512)
            printf("\n\t\a Overrun Error");
        if (status & 1024)
            printf("\n\t\a Parity Error");
        if (status & 2048)
            printf("\n\t\a Framing Error");
        if(status & (512|1024|2048)) /* if any error */
            break;

        if(status & 256) /* if data ready */
        {
            if((out=_bios_serialcom(_COM_RECEIVE,port,0) & 255)!=0)
                putchar(out);
        }

        if(kbhit()) /* if a keystroke is currently available */
        {
            in=getch(); /* get a character without echoing onto the screen */
            if(in==27) /* if ESC */
                break;
            _bios_serialcom(_COM_SEND,port,in);
        }
    }
}

```

asserts RTS high, which in turn asserts CTS high, meaning thereby that the virtual modem has the room for storing the data and the computer can send it.



**4. Testing** – It is usually difficult to work on both PCs when a programmer wishes to check his/her source code for PC-to-PC communication. The best possible way to overcome this problem is to use a loopback connector (shown in **Figure 4**), which enables the programmer to write source-code for programming serial port with single PC.

A loopback connector usually consists of a connector without a cable and includes internal wiring to re-route signals back to the sender. When the computer receives data, it will not know whether the signals it receives come from a remote DCE device set to echo characters, or from a loopback connector. Using loopback connector, proper operation of the computer's serial port can be checked.

#### 5. Data transfer procedure

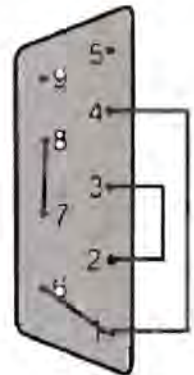
- Connect the two PCs together using the 3-wire link.
- Run the program given in the source code on both PCs.
- Before sending the data, set both the sending and receiving PC terminals to the same baud rate, and same format of data bits, parity bits and

stop bits using the macro (pre-processor directive) 'SETTINGS' in the source code.

- When the source code is compiled and run on both PCs, the characters typed in one computer should appear on the other computer's screen and vice-versa.

**6. Limitations** – Here, we are using RS-232 serial asynchronous communication, so the communication speed is less than that of parallel data transfer, where 8-bit data is sent at a time rather than bit by bit.

**7. Applications** – On the guidelines presented in this article, useful functions such as file transfer, chatting etc can be implemented. By using hardware circuitry employing infrared/laser diodes, even wireless PC-to-PC communication can be easily implemented.



**Figure 4:** Loopback connector

#### Designers' note:

The executable code is available on request

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Agilent (HP) 4274A LCR Meter	£1750	Agilent (HP) E4404B (opts 1D5,1DN,A4H) Spectrum An. (9kHz-6.7GHz)	£10000
Agilent (HP) 4275A LCR Meter	£2750	Agilent (HP)34401A 6.5 Digit Bench DMM	£550
Agilent (HP) 4276A LCR Meter	£1400	Agilent (HP) 4194A (50 ohm) Impedance/Gain Phase Analyser	£10750
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Agilent (HP) 8924C CDMA Mobile Station Test Set	£6000	Wavetek 9100 Universal Calibrator (Opts 100 / 250)	£9000
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# An Alternative To

Peter Grundy of P G Engineering (Sussex) Ltd explains the benefits of automating vs cheap labour, despite many firms deciding to manufacture offshore

The economic rush to outsource assemblies to low cost areas such as Asia has had a profound effect on the manufacturing bases of Europe and the Americas. Many products have a relatively high labour content and if they are to be built in volume, the scale of the Asian operations offers better margins and a competitive edge. But does this apply universally? Let us use an example of an electronic sensor.

Ostensibly, it would seem to be a natural fit to a low-cost assembly environment, but is that an automatic choice?

Manual assembly workers can easily perform most of these tasks and the output can be prodigious, but the electronics assembly flow shown in **Figure 1** includes flip-chip that would almost certainly cause huge quality problems for manual assembly. The original design included wire-bonded

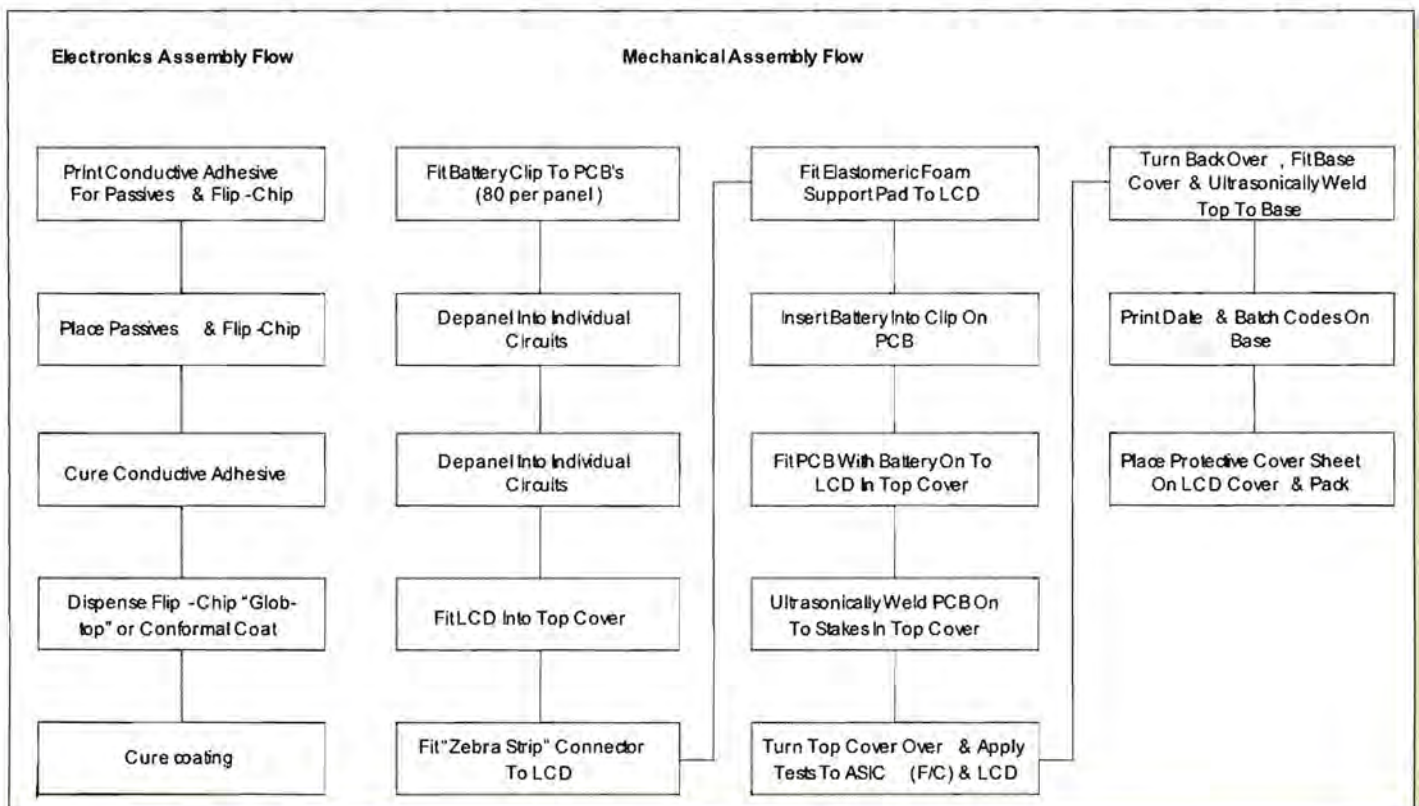
chip-on-board and could be assembled in a low cost area using semi-automatic wire-bonders. Once the design changes to incorporate flip-chip, the whole operation becomes more difficult to achieve overseas.

### Long range pitfalls

It has long been known that a stable product that does not require much engineering input during its lifetime of manufacture can be successfully built at extremely long range. This does not mean that the product must be simple; Asian manufacturers are now very capable of building sophisticated and highly technical assemblies.

However, if regular design re-issues occur or if constant process changes are necessary, there needs to be a close co-operation between the design team and the manufacturing unit. If solid Design-For-Manufacture rules are in place then the

Figure 1: Product assembly flow





# Cheap Labour

difficulties are lessened but they do not go away.

The response times for a design change when the product is built remotely can have a severe impact on the time-to-market requirements of the product and it can be necessary for a team of designers or product/process engineers from the home design authority to be sent to the remote build area. This, of course, increases costs.

It may even be necessary for an OEM to organise a team of ex-patriots on rotating shifts, typically two months away followed by two months at home. This way the costs of keeping the 'away team' remain high but, also, the effectiveness of the team when on home duty is diluted, as they cannot spend more than two months on tackling an issue.

Many of the favourite Asian sites are positioned relatively close to financial centres or established communities but, increasingly, the lowest cost sites are being pushed further afield. Not all operations have the extreme consequences mentioned above but it is necessary to evaluate the need to manufacture offshore much more seriously than to copy the competition or show a "knee-jerk" reaction to the stampede abroad.

## Labour pool

It is true that the availability of highly trained local engineers that speak the appropriate languages is improving but, in time, they will seek a higher standard of living and drive up wages. This has happened in Singapore, which is still slightly cheaper than Europe or America but much more expensive than most of the rest of Asia.

Those countries that are actively seeking electronics assembly work are also aware that they must provide fully trained personnel. They also acknowledge that there is a time delay between capturing the new large volumes of business and providing that necessary trained workforce. The cost of all this training is not free and the cost of doing it must be amortised across a variety of tax and business structures.

One of the great attractions to manufacturing in Ireland in the 1970s through to 2001 was the good fortune of Ireland investing in a strong educational structure. Although the overall population of this

country is low, the proportion of highly trained engineers was, and still is, very high. With the advent of the European Union and a gradual increase in wage rates to reach the levels of the rest of Europe, Ireland became less attractive to outside investors who often moved to Asia or Eastern Europe for short-term gain.

Today, in Europe and America, there are still large numbers of highly skilled and trained engineers who are more than capable of handling the problems and issues of high technology products.

## Maximum automation impetus

As mentioned earlier, there will always be products with a relatively high labour content that will always suit low cost manufacturing areas, regardless of geographical issues. However, there are also many products that have a low labour content, or can be automated as such that the labour content is negligible. Even if the production volumes are high and the design is stable with very few changes, one can build a case for automating the whole assembly to a very high level and some interesting possibilities emerge.

— **Labour:** It may be possible to automate the assembly to the point where only three operational staff are required per shift to run the line. One electronic/electrical operational technician, one mechanical assembly/test engineer and one supervisor capable of handling both tasks. Clearly, these people will need to be very highly trained and capable. Many such personnel exist in Europe and the US. Although the individual staff costs will be high per person, the overall staff cost for the build operation will be very small, even insignificant, once the operation runs at high volumes.

— **Equipment:** The equipment costs for high levels of automation will be very high from the start but can be easily amortised over a perceived run lifetime. Usually, volume increases can be handled by the addition of extra modules if the original line specification was thought out properly and the cost of extra modules can be built into business models for the future expansion of the facility. Adding extra



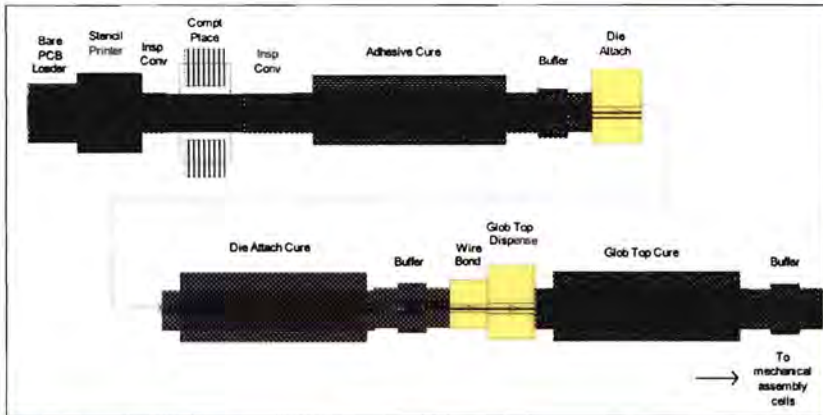


Figure 2. Floor area of a workflow for a sensor

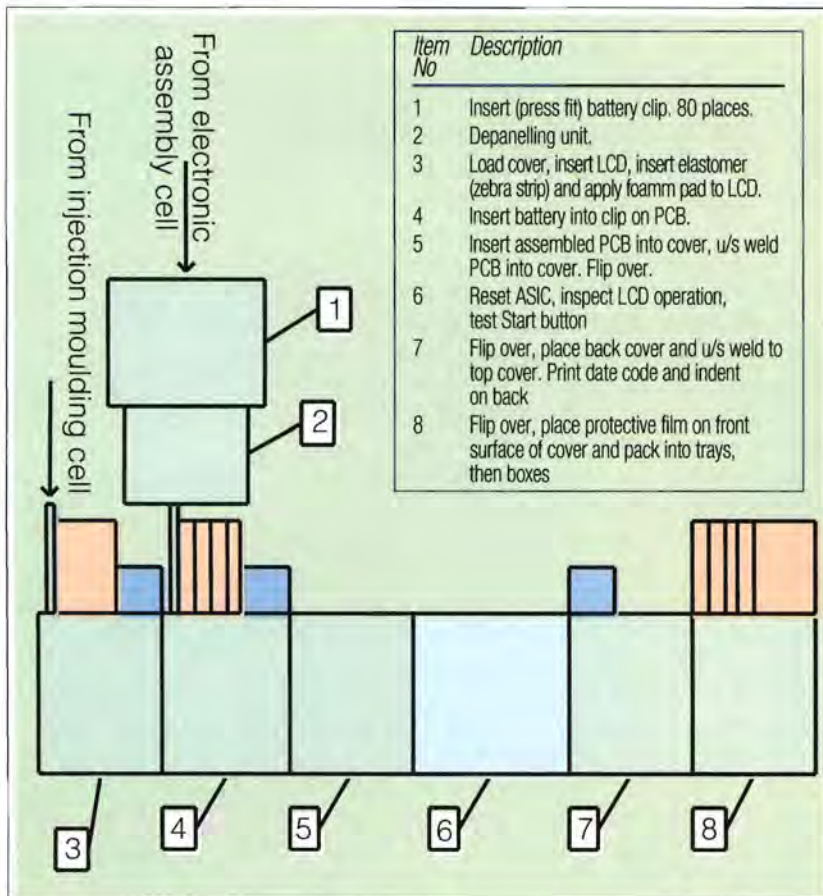


Figure 3. Block diagram of the assembly flow

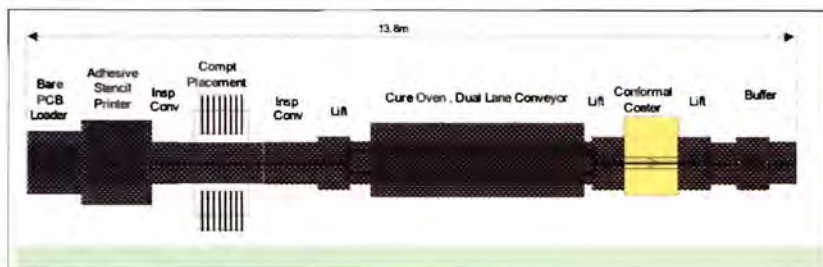


Figure 4. Optimum electronics assembly cell

labour in a low cost area will allow the manufacturer to react to increased volumes but with added training, time and quality implications.

**Quality:** Once the automated line has been specified, installed and commissioned successfully and the required staff are fully trained, the product quality will be consistent to a predetermined level. Process variations can either be handled by the skills of the staff or by designing into the line automated checking and closed loop feedback systems to instantly and automatically correct minor defects, before they have a chance to create scrap or volumes of rework.

**Customer geography:** So far, the suggestions above indicate a large manufacturing operation but that does not need to be the case. The production volumes could be broken down into sizes that suit particular customers and highly efficient but compact operations could be sited very close to the end customer. So, for example, the concept of Design-in-Britain, Build-in-Vietnam and Ship-to-North America could be replaced by a concept of Design-in-Britain and Build-in-North America.

**Change response:** When building at long range and using low levels of automation, the response time to a change instigated by a customer will be lengthy and may need teams of ex-patriot professionals to handle the change. If the automated manufacturing site is next door to the end customer and the staff running it are high-level professionals, the response time will be minimal, with no need to send out engineers to plan and implement the change.

**Shipping:** Obviously, the shipping time is virtually zero if the manufacturing site is close to the customer and the shipping costs are correspondingly low. Insurance costs should be lower and the risks lower.

## Business model

Let us return to our particular example.

The design and development base in the UK is under pressure to modify or create new sensors as quickly as possible but suffers from delays or problematic new product introductions. There are also serious costs associated with these delays and problems. The best way forward to develop a good relationship with the customer and react very quickly to changing needs is to consider automation linked to the customer's geography and infrastructure.

The electronics workflow is quite short but has some serious floor area considerations if wire



bonding and three reflow ovens are needed (one for adhesive cure, one for die attach cure and one for "glob-top" cure). See **Figure 2** for details. The whole line is 26m long, so, would this be suitable automation?

Although this particular product type can adopt some exotic production methods, the general philosophy will apply to a wide range of products.

A 26m long line with so many elements is hard to justify on staffing grounds but it is also expensive in terms of equipment. It can, however, be shortened considerably and most of the reflow units can be combined into one operation. Once the decision to use flip-chip instead of wire-bonded chip-on-board has been made, it becomes noticeable that the curing characteristics of the glob-top and the conductive adhesive are almost identical. With some careful use of dual conveyors and lift units, a single reflow oven can be used for all operations.

Before we look at the probable equipment diagram, we need to consider the mechanical assembly criteria. The assembly flow shown earlier indicates that there are many steps in the process but some of these can be combined and a typical assembly block diagram would look something like **Figure 3**.

### Mechanical needs

This article is focused on electronics manufacturing but we still need to comment briefly on the needs of the mechanical assembly.

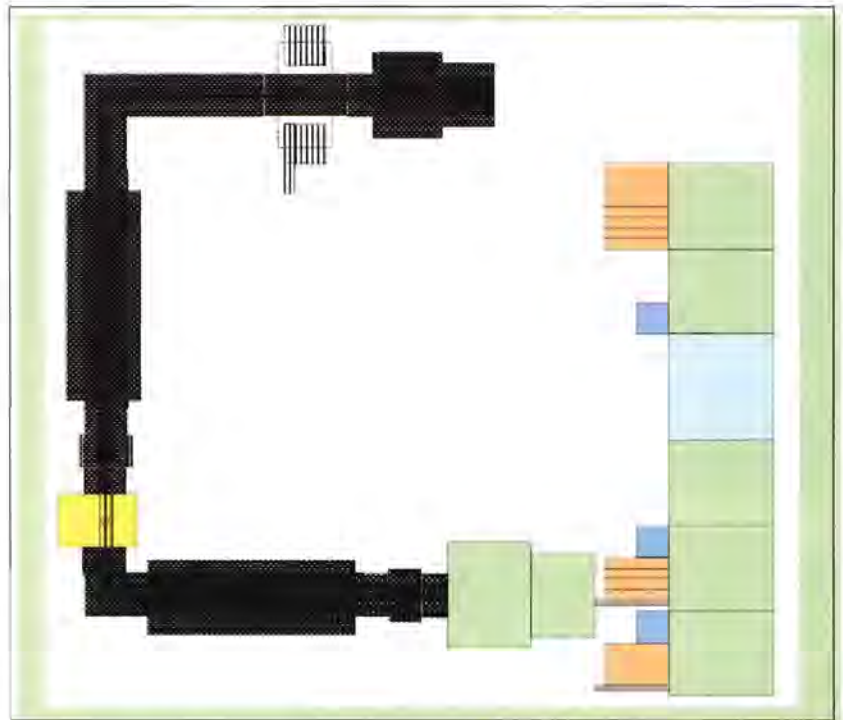
The inputs to this cell come from two sources. One is the electronic assembly cell and the other is the plastic moulding cell that supplies plastic casings. This article will not explore such criteria.

The work flow requires adhesive deposition, component placement, adhesive cure, glob top application and glob top cure as its focus where the adhesive and glob-top have almost identical cure characteristics. Sophisticated automation can be used to take advantage of these characteristics.

The optimum line configuration can now consist of only one cure/reflow oven and some clever conveyors. See **Figure 4**.

The first thing to notice is that the line length is 13.8m and that is almost half the original concept. But it is also important to see that a lot of the elements are conveyors and that means that the line can be "bent" around corners. This means that we can fit the whole assembly system into a small space. It relies on the concept of lift conveyors and the oven having a dual lane construction so that the first pass allows adhesive curing and the second pass allows glob-top curing to take place. The final concept could look like **Figure 5**.

This line occupies approximately 15m x 16m



**Figure 5.** Optimum line

floor area but it also needs to be fed with plastic mouldings. These can either be bought from external suppliers or input from a separate plastic moulding department. The moulding department will have its own floor area requirements and that is not a consideration here. Let us suppose that the area for moulding is the same as the assembly department, therefore, the total floor area will be about 30m x 17m, allowing for office space etc.

The beauty of a system like this is that it requires very few staff to look after it. Per shift, the assembly department will need three people. One will be a supervisor and the other two are specialists in electronics and mechanical assembly. It is acknowledged that these will be expensive people, however. If the plastic mouldings are produced on site, then there will be extra staff involved. The mini-factory needs administration staff then we will need to consider the numbers involved.

The theory behind all of this is to make it easier for OEMs to place their mini manufacturing units next door to their customers and avoid long-range engineering difficulties and support. This is an increasingly European issue as more and more manufacturers decide to move manufacturing off-shore to Asia, without contemplating the overall customer frustrations. It is well worth considering high levels of automation to allow the end customer to benefit without forcing him to use overseas supply routes.





# Real DTMF Generator

Microcontrollers can be used for generating DTMF tones. **Bijan Poorghafour** explains how a low-cost, low-speed MCU, such as AT89C2051-24PI, can generate high-accuracy DTMF tones

After the development of the 'Pure Sinewave Generator', described in the August issue of Electronics World, page 22, it's easy to generate a wide range of frequencies. The algorithm is so simple that a microcontroller can run it.

The algorithm can generate frequencies that are multiples of the base frequency, or 250Hz. With this algorithm, many tones can be generated in the range from 250Hz to 10kHz in steps of 250Hz.

The algorithm is flexible and it can be modified to generate tones other than multiples of the base frequency. Sinewave samples are generated by high sampling rate as 50kHz. So, filtering sampling noise can be done with a simple filter.

### What is the DTMF?

DTMF is one of the most popular and historical ways for in-band signalling in a telephone line. It is so robust and powerful that many engineers are using it in telecommunication and data transceivers.

Each DTMF tone is a combination of two frequencies, in the low frequency and high frequency range. These frequencies are added with each other to make a DTMF frequency.

We analyse the DTMF as a simple tone telephone dialler. Tone dialler has 16 keys. They are arranged in a formation of four rows by four columns. Each row and column is associated with a frequency. The rows correspond to the frequencies 697Hz, 770Hz, 852Hz and 941Hz, and the columns to the frequencies 1209Hz, 1336Hz, 1477Hz and 1633Hz. The row frequencies represent the "low group" and the column frequencies the "high group".

When a key on the keypad is pressed, the column and row frequencies are combined in equal portion to generate a DTMF tone. It is better to name this a DTMF "code" rather than a DTMF "tone". Such dialler is fast and a telephone centre can easily and quickly detect such code.

For example, when we touch number "8" on the keypad, the 852Hz and 1336Hz are generated and added to each other. The tones must be pure and accurate.

### DTMF frequencies

DTMF frequencies are very hard to generate. Generation of two of them cannot be done by a low frequency and standard XTAL source, for example.

The frequencies are such that harmonics of a tone are not considered to be a valid tone.

The frequencies have been selected since the human voice does not contain them. This makes DTMF signalling in a telephone line very robust and powerful.

### Generation methods

There are various ways to generate DTMF and, here, I describe some of them:

□ Using an IC, such as the TP5089. This IC is using an XTAL as a high-accuracy clock source. This chip has an acceptable error range and a receiver can detect its tones. It has a built-in keypad scanner and it is ideal as a single tone dialler.

The DTMF generator is connected to the microcontroller unit (MCU). This means that the MCU generates the needed DTMF code and then the IC generates the frequencies of a corresponding code. These types of ICs are fairly popular.

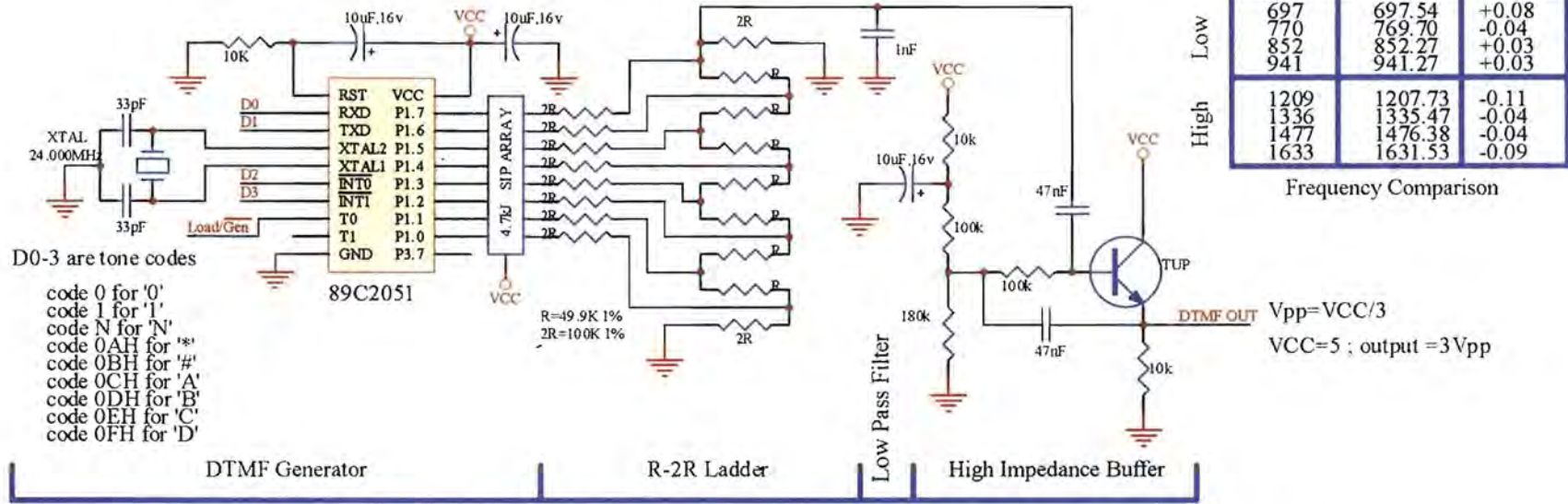
□ Once I heard that Atmel has supplied a code to generate DTMF by an MCU through a single pin, with PWM techniques. I have not tested this yet but one obvious problem is that we have to filter out the sampling through a high-degree active filter. In this instance, timers sometimes cost more than the MCU itself.

□ The genius way: I heard one engineer has saved a "voice" of DTMF tone in a sound-recording chip, popularly used in answering machines. When the code is dialled, the chip plays the recorded sound, which, in fact, is a DTMF tone. This is a very good idea for a designer to apply in telephone systems.

Unfortunately, it also means that the recorded sounds can easily be erased from the chip. In addition, there's plenty of noise in these chips. In which case, we need a noiseless source for minimum noise recording.

□ Some low price systems are using internal microcontroller





## DTMF Generator

- \*- DTMF Generation with 8051 MicroController Family.
- \*- Real Synthesize of Low and High Group Sine Waves.
- \*- Very Low Harmonics and Distortion.
- \*- Very High Accuracy ( Error less than 0.1% ) and Stability.
- \*- Very High Sampling Frequency (31.250KHz ).
- \*- Now Available on AT89C2051-24PI.
- \*- Less Than 1600 Bytes Program Space Requirement.
- \*- Very Easy Interface to Micro.
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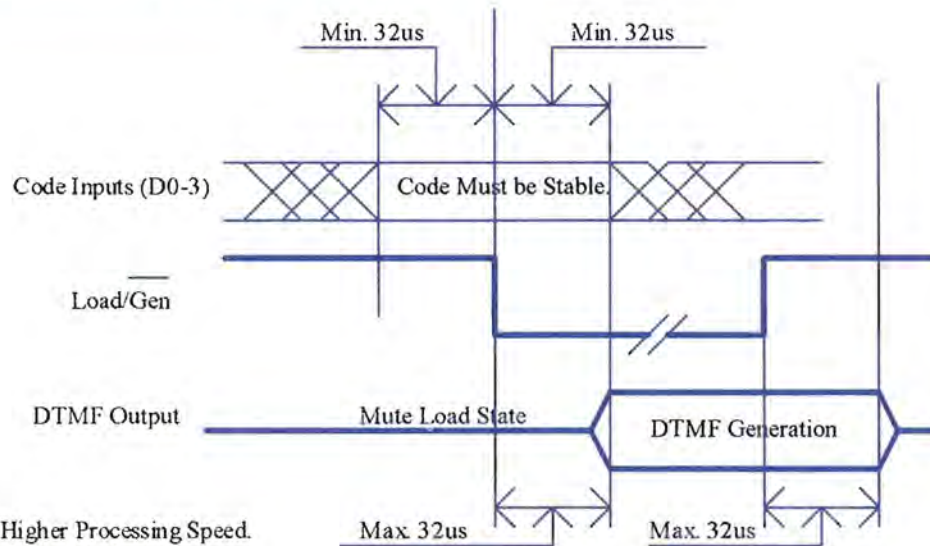


Figure 2: The DTMF-generating circuit



timers to fit DTMF frequencies. These use pulses with rich harmonic content, which adds more frequency errors.

□ In very expensive systems, a DSP generates DTMF frequencies by running floating-point instructions.

## What is new?

This is the first time that a microcontroller such as AT89C2051 has been used to generate real DTMF frequencies with very low harmonics and high accuracy. It also generates real samples of frequency for each group of DTMF frequencies.

By means of the Pure Sine Wave Generation Algorithm, it is now possible to generate a set of frequencies that are not related to each other. When a DTMF code is sourced to the MCU, then it generates frequencies of corresponding code. The MCU generates sine samples of a high frequency group and low frequency group separately and adds them to make the final sample. This sample is then fed to a D/A converter and a voltage sample is generated. A simple filter (R and C) can eliminate the sampling frequency.

## Main features:

- 1 Low speed and cost controller can generate DTMF frequencies. The controller used here is an AT89C2054-24PI.
- 2 A very popular 24.000MHz XTAL is also used.
- 3 Sinewaves for high group and low group are synthesised purely and accurately.
- 4 Harmonic distortion is less than -37dB.
- 5 Frequency error is less than 0.11% and it is highly stable.
- 6 The sampling rate is very high at 31.250kHz.
- 7 The total program code space is 1600 bytes.
- 8 The chip interfaces easily with the microcontroller.
- 9 It can start and stop generation as fast as 32us.

## THD measurements

I have analysed samples generated by a simulations program for each tone of DTMF. I have calculated THD over a 4kHz bandwidth (see Table 1).

The main tone is also very stable within the frequency band and there is very low ripple (0.2%) in the band.

The frequency measured is highly accurate; it's even better than the readily available commercial DTMF generators.

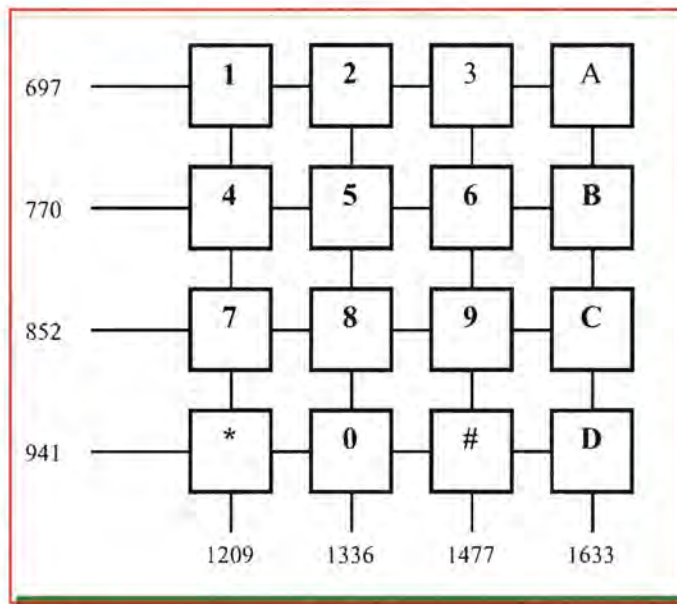


Figure 1: Tone dialer, row and column frequency associated to each key

Table 1: Frequency comparison and THD			
Standard (Hz)	Designed (Hz)	THD (dB)	Error (%)
697	697.54	-41.97	+0.08
770	769.70	-37.19	-0.04
852	852.27	-41.66	+0.03
941	941.27	-46.47	+0.03
1209	1207.73	-42.44	-0.11
1336	1335.47	-39.68	-0.04
1477	1476.38	-45.23	-0.04
1633	1631.53	-44.97	-0.09

## Minimum system design

When I developed the DTMF generator, I was asked to design it at a minimum cost (please see Figure 1).

At the heart of the board is a microcontroller that generates the tone samples. It uses a low price 24.000MHz XTAL for the oscillator. Samples are fed to R-2R ladder to convert digital samples to voltage samples. All pins of port P1 must be pulled up by resistors much lower than the R-2R ladder. Here, I have selected a pull-up resistor of 4.7kΩ and R-2R ladder to 49.9kΩ-100kΩ. Note that this will generate some distortion in the signal, but it is very small and cannot corrupt the reception of the DTMF receiver.

Since the sampling frequency is much higher than the maximum DTMF frequency (1633Hz), the filter is very simple and only a 1nF capacitor is applied. The impedance of the R-2R ladder and 1nF capacitor make a low pass filter to filter out the sampling frequency.

In the buffer, I have designed a simple emitter follower with some feedback to boot the input impedance, known as bootstrap. When 5V is supplied, the output is 3V peak-to-peak. Generation

of DTMF starts when the line Load/Gen is forced low. It needs a maximum of 32us to detect this activation. When this line is deactivated, it takes 32us to stop the generation.

## Applications

- 1 Many designers will find my design suitable for a minimum design cost application using a microcontroller. They can implement DTMF code with their code. That's why the DTMF code is less than 1600 bytes so it can be implemented in many designs.
- 2 Microcontroller makers can implement my code as a firmware in the chip, which will add DTMF capability to the device.

**Designer's note:** I cannot supply the code to an end user but I can send programmed and locked microcontrollers for further testing and qualification.

Please contact the magazine's editor by email,

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# RoHS WHAT'S ALL THE FUSS ABOUT?

**R**oHS (the Restriction of the use of certain Hazardous Substances) and WEEE (Waste Electrical and Electronic Equipment) is the equivalent of Y2K for the electronics industry. The upcoming EU environmental directives are the most significant developments in electronics legislation to happen in many years and will completely revolutionise the way electrical and electronic products are designed, sold, recovered and recycled. Worryingly, many design engineers are still not fully aware that the upcoming legislation will affect them. For those who are, many questions remain unanswered. Complicated exemption rules, uncertainty about how the directives will be enforced, obsolescence and component availability has left engineers unsure of what they need to do and when. The clock is ticking. With only six months to go there's no time to lose in the transition to RoHS. If compliant components aren't already part of the design cycle it could well be too late.

## **Q:** What are the facts about RoHS?

**GN:** RoHS will come into force on the 1st July 2006. From that date no electrical or electronic equipment placed on the market will be allowed to contain levels of lead, cadmium, mercury, hexavalent chromium, polybrominated biphenyl and poly-brominated diphenyl ethers above the maximum concentration values set out by the directive. This applies to finished equipment that falls into eight broad categories: • Large household appliances • Small household appliances • IT and telecommunications equipment • Consumer equipment • Lighting equipment (including light bulbs and luminaries in households) • Electrical and electronic tools (except large scale stationary industrial tools) • Toys, leisure and sports equipment • Automatic dispensers

## **Q:** Are there any exemptions?

**GN:** There are some exemptions. At the time of writing there are four significant batches of exemptions, either in place or under review, totalling over 60 product categories, and more are expected. Several areas do not currently fall within the scope of the RoHS Directive, although medical devices and monitoring and control equipment (categories 8 and 9 of the WEEE Directive) are currently under review and may well be added to RoHS in a few years' time. Areas of exemption currently include: • Medical devices, monitoring and control equipment • Maintenance and repair – spare parts for repair, upgrade or reuse of electrical and electronic equipment on the market before 1st July 2006 • Electrical and electronic equipment that is part of another type of equipment not covered by RoHS. Examples include a car radio (a car does not fall within RoHS, so neither does the radio), equipment on a train, boat, aircraft, electronics in a lift etc • Batteries, there is separate legislation in the pipeline for this, but not battery charges – the latter will fall within

RoHS depending on their application • Military – where the only use is military or national security.

One of the biggest impacts of the legislation is in the area of lead-free soldering, where higher melting point temperatures are often required. Over 70 lead-free alloys are available and, while experts appear to be comfortable with the SAC (tin-silver-copper) alloys when soldering either tin-lead or lead-free terminations, many of the others, due to varying characteristics, may require further investigation by the engineer.

## **Q:** How to achieve compliance in time?

**GN:** Sourcing compliant product quickly and ensuring it is risk free are other challenges currently facing the engineering world. Design engineers must avoid a part number lottery by using distributors that are changing part numbers and clearly segregating compliant and non-compliant stock. The need to ensure suppliers are providing complete documentation and, where appropriate, material testing is also key, as is traceability and the steps required to ensure due diligence, accompanied by robust internal procedures.

For many, the web is proving to be an invaluable tool in each of these areas. Compliant product listings and new part numbers are continually being updated as stock becomes available in the marketplace. The web is clearly the fastest and most efficient way to source the latest RoHS components, download certificates of compliance and access the latest news on RoHS and WEEE.

## **Q:** Does it really bring any environmental benefits?

**GN:** Although the driver for environmentally friendly products has been prevalent for some time, it has only been in the last few years that the need to produce such equipment has moved from being consumer-led to a legal requirement. With more and more electrical and electronic items becoming affordable, coupled with the shorter life cycle of these products, it has become critical that the problem is recognised in legislation.

RoHS was born out of the WEEE directive, whereby producers will have to register with the appropriate authorities across Europe to cover their obligations to arrange, and finance the recovery, treatment, recycling and environmentally safe disposal of electronic and electrical equipment.

With millions of tonnes sent to landfill sites throughout Europe every year, the WEEE directive encourages product design to take into account repair, reuse and recycling at end-of-life. Coupled with the RoHS directive banning hazardous substances, the legislation will play a significant role in reducing the risk to human health and the environment. Complying with RoHS and WEEE will bring real environmental benefits. It's time to embrace the legislation.



Gary Nevison is chairman of the AFDEC RoHS team, board director at Electronics Yorkshire and head of product market strategy, Farnell InOne. As such he is our industry expert who will try and answer any questions that you might have relating to the issues of RoHS and WEEE. Your questions will be published together with Gary's answers in the following issues of Electronics World.

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# Dawn of a Brave New World

By Mike Brookes

For generic Short Range Devices (SRDs), a new era is starting. For years, the standard used for SRD parameters in the frequency range 25MHz to 1000MHz has been ETSI EN 300 220 in three parts.

Following an extensive review that took two years, this hoary, old work-horse has been substantially changed and is now a conventional two-part standard. Part 1 gives the complete, voluntary technical parameters; Part 2, the 'harmonised section' incorporating the essential requirements necessitated by the provisions of the R&TTE Directive.

The major changes relate to the use of the 868/870MHz band. The new version of EN 300 220 now incorporates details of the requirements for the use of the spectral efficiency techniques 'Listen Before Transmit' and 'Adaptive Frequency Agility' (LBT/AFA).

The adoption of LBT/AFA has opened up the band from 868-870MHz to 863-870MHz – a huge increase, giving SRD module/chip designers much more space to work in and marketers confidence in a less crowded future.

Before the 'new' standard was released, extensive compatibility studies for co-channel interference were carried out by the Spectrum Engineering Group of the European Communication's Committee, which concluded that LBT/AFA would create an "open road" concept to allow better sharing and more flexibility, in contrast to the old concept of strict band usage definitions and complex band plans.

The existing band plan for 868-870MHz remains in place to protect and support legacy systems with 'channel exclusivity' retained for alarm systems. Indeed, a further 100kHz (869.3-869.4MHz) in the 868-870MHz band have been allocated solely to alarm systems, adding to the 50kHz already in place, to ensure that compliance with CENELEC rules, where LBT/AFA is perceived to give problems, does not restrict sales development.

When using LBT/AFA, duty cycle restrictions are removed, though there are limits on transmission dialogue length and there is no band plan.

Compatibility studies considered 25, 50, 100 and 200kHz channels, concluding that an

optimum of 100kHz, working at a maximum ERP (effective radiated power) of 25mW would be the best 'general' solution. This gives 70 available "channels".

Duty cycle is retained for non LBT/AFA single-channel products and for DSSS (Direct Sequence Spread Spectrum) and FHSS (Frequency Hopping Spread Spectrum) equipment at 1% or less.

Concurrent with the revision to the standard are the necessary changes to its 'twin' regulatory document CEPT/ERC Recommendation 70-03, which sets out the conditions and technical parameters for the use of SRDs. Amendments to Annex 1 (generic SRDs) and Annex 7 (alarms) have already been put into practice.

The advent of LBT/AFA is the first clear sign that SRDs have moved from the simple single channel products, first introduced in the early 1990s and used as 'door openers' or 'car key fobs', to the realms of sophistication associated with mainstream products. Coupled with this new approach is financial change. Ten years ago, SRD products ranged in price from £10.00 for the simplest wideband devices to

£200.00 for high-quality, narrow-band modules.

Today, chipsets incorporating LBT/AFA and additional intelligence are available at volume prices of £5.00 or less. Wi-Fi and Bluetooth have hugely increased public awareness of short range radio and its capabilities, now that appetite will be fuelled by availability of low-cost and highly versatile generic devices.

With chip-sized radios and high-capacity, low-cost batteries arriving at the market place simultaneously, an explosion of new, portable SRD products is anticipated. And this is only the start. The next move, software-based or cognitive radio, is set to give even greater SRD capability. LPRA is already heavily involved with ETSI to derive new standards for a flexible future and with the regulators to ensure that spectrum policies of the future promote the success of the SRD industry.

The Low Power Radio Association is a European trade body that represents manufacturers and users of short range devices (SRDs).

Mike Brookes is LPRA's chairman.

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## PICmicro Microcontroller CCP and ECCP

The Capture, Compare and PWM (CCP) modules that are found on many of Microchip's microcontrollers are used primarily for the measurement and control of time-based pulse signals. The Enhanced CCP (ECCP), available on some of Microchip's devices, differs from the regular CCP module in that it provides enhanced PWM functionality – namely, full-bridge and half-bridge support, programmable dead-band delay and enhanced PWM auto-shutdown.

The ECCP and CCP modules are capable of performing a wide variety of tasks. The tips below describe some of the basic guidelines to follow when using these modules, as well as suggestions for practical applications.

### TIP 1: Measuring RPM using an encoder

Revolutions per minute (RPM) or how fast something turns, can be sensed in a variety of ways. Two of the most common sensors used to determine RPM are optical encoders and Hall Effect sensors. Optical encoders detect the presence of light shining through a slotted wheel mounted to a turning shaft (see Figure 1). As the shaft turns, the slots in the wheel pass by the eye of the optical encoder. Typically, an infrared source on the other side of the wheel emits light that is seen by the optical encoder through slots in the wheel.

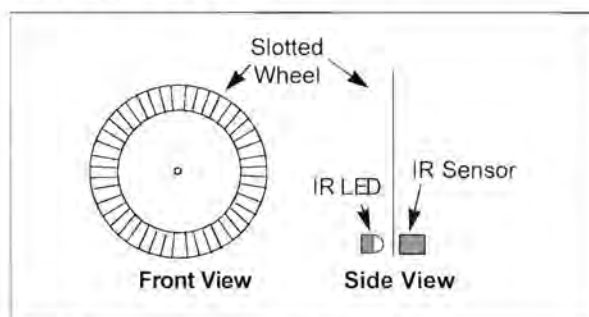


Figure 1: Optical encoder

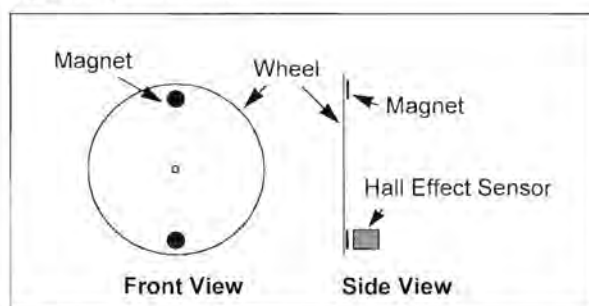


Figure 2: Hall Effect sensor

Hall Effect sensors work by sensing the position of the magnets in an electric motor or by sensing a permanent magnet mounted to a rotating object (see Figure 2). These sensors output one or more pulses per revolution (depending on the sensor).

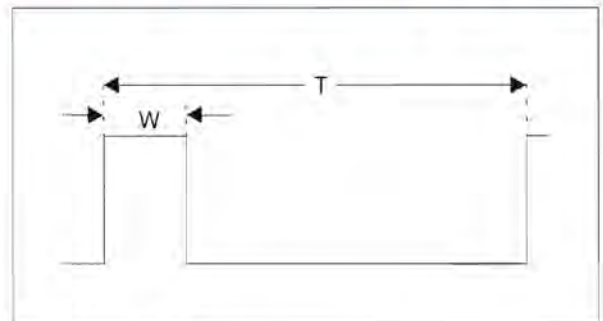


Figure 3: Low RPM

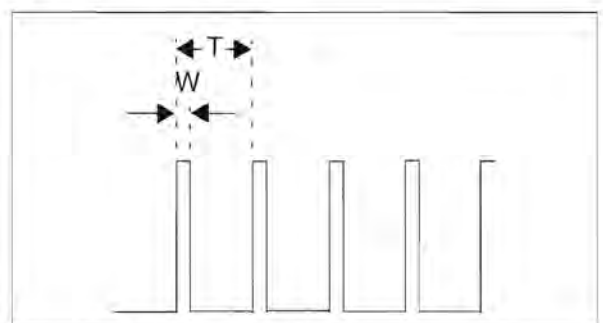


Figure 4: High RPM

In Figure 3 and Figure 4, the waveform is high when light is passing through a slot in the encoder wheel and shining on the optical sensor. In the case of a Hall Effect sensor, the high corresponds to the time that the magnet is in front of the sensor. These figures show the difference in the waveforms for varying RPMs. Notice that as RPM increases, the period ( $T$ ) and pulse-width ( $W$ ) become smaller. Both period and pulse-width are proportional to RPM. However, since the period is the greater of the two intervals, it is good practice to measure the period so that the RPM reading from the sensor will have the best resolution. See TIP 1 in the "Tips 'n' Tricks – PICmicro Microcontroller CCP and ECCP" booklet (DS41214) for measuring period. In addition, see Tip 2 (also shown in the DS41214 booklet), which features a technique for measuring period with averaging, but is also useful for measuring high RPMs.

### TIP 2: Measuring the period of an analogue signal

Microcontrollers with on-board analogue comparator module(s), in addition to a CCP (or ECCP) module, can easily be configured to measure the period of an analogue signal. Figure 5 shows a circuit using the peripherals of the PIC16F684.

R3 and R4 set the threshold voltage for the comparator. When the analogue input reaches the threshold voltage, VOUT will toggle from low to high.

R1 and R2 provide hysteresis to ensure that small changes in the analogue input won't cause jitter in the circuit. Figure 6 demonstrates the effect of hysteresis on the input. Look



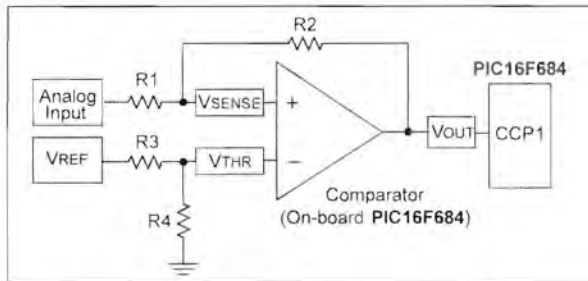


Figure 5: Circuit using the PIC16F684

specifically at what VSENSE does when the analogue input reaches the threshold voltage. The CCP module, configured in Capture mode, can time the length between the rising edges of the comparator output (VOUT.) This is the period of the analogue input, provided the analogue signal reaches VTHR during every period.

In Compare mode, the 16-bit CCPRx register value is constantly compared against the TMR1 register pair values. When a match occurs, the CCPx pin is driven high, driven low, remains unchanged, or toggles based on the module's configuration. The action on the pin is determined by control bits CCPxM3:CCPxM0 (CCPxCON<3:0>). A CCP interrupt is generated when a match occurs.

### Special event trigger

Timer1 is normally not cleared during a CCP interrupt when the CCP module is configured in Compare mode. The only exception to this is when the CCP module is configured in Special Event Trigger mode. In this mode, when Timer1 and CCPRx are equal, the CCPx interrupt is generated, Timer1 is cleared and an A/D conversion is started (if the A/D module is enabled).

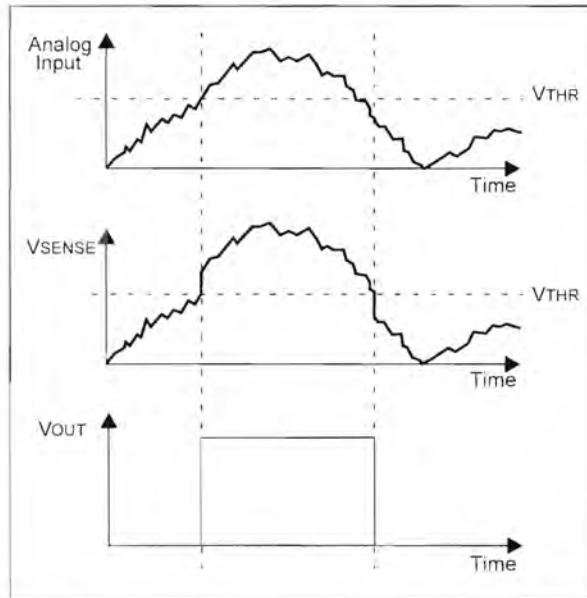


Figure 6: Signal comparison

### “Why would I use Compare mode?”

Compare mode works much like the timer function on a stopwatch. In the case of a stopwatch, a predetermined time is loaded into the watch and it counts down from that time until zero is reached. Compare mode works in the same way with one exception – it counts from zero to the predetermined time. This mode is useful for generating specific actions at precise intervals. A timer could be used to perform the same functionality, however, it would mean pre-loading the timer each time. Compare mode also has the added benefit of automatically altering the state of the CCPx pin, based on the way the module is set up.

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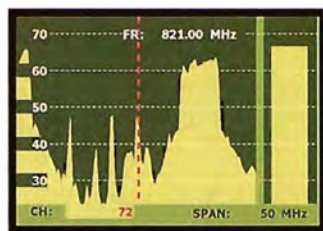
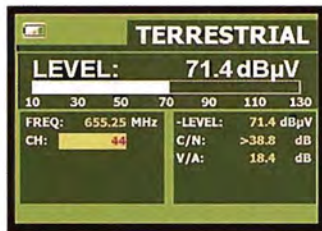
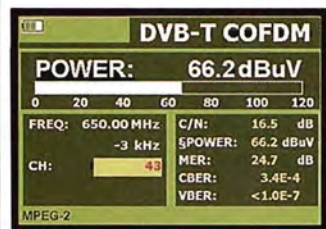
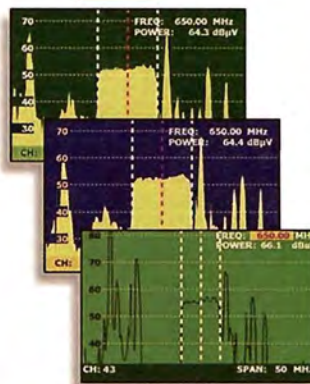
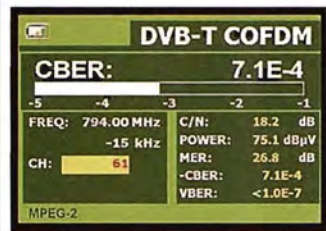
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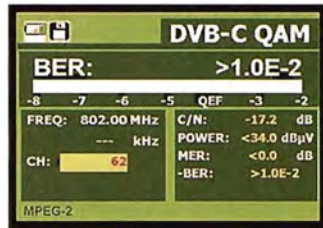
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**Metal film labelling**

I have just read Mr. Beukes letter referring to my article, which appeared in *EW* for July, 2005 ('Auto-light controller', p14).

Mr Beukes is quite right in saying that I should have labelled R2 as a metal film component (in this day and age I would be surprised if anyone would consider using any other kind of resistor in a similar design), but he is incorrect in saying that it need be something other than 0.25W. MR25 type resistors have a maximum working voltage of 300V and an overload voltage of 600V. These figures are more than adequate.

Mr. Beukes will not allow me to connect R3 to the junction of D1 and C1 but advises that there is a suitable connection at another point in the circuit. There is, of course, but I prefer mine and would point out that, with any luck, simply leaving pin 10 of IC1 disconnected would probably do just as well. Again, I agree I should have labelled R3 as metal film.

I cannot understand Mr Beukes next points. The PCB layout included in my article shows track spacing which is more than adequate for carrying mains voltage without flash-over. The usually recommended minimum distance is 1mm per kV. Similarly, his fourth point would over-egg the pudding when he declares (without explanation) that wires need to be soldered along certain tracks. I assume he is concerned about their current carrying capacity. The 2mm (0.08inch) tracks illustrated will run a 750W lamp without additional copper being necessary. My original parameters were extrapolated from standard tables that state that on PC board material, faced with standard copper (35 micrometer),

tracks of 2.5mm width will carry 4A with no more than a 5.5°C increase in temperature. His associated comment about the earth connection might just as well be applied to the equally unlikely event of the earth wire breaking inside the cable.

Finally, coating the board with lacquer and using a transient suppressor (if there were room to fit such a component) maybe nice but not necessary. In fact, random spray from an aerosol can of protective lacquer is more likely to damage the sprayer's health than using an un-lacquered PCB if it is correctly fitted.

**David Ponting**  
UK

**Noticeboard**

I have been a reader of *Wireless World* and *Electronics World* and, also, *Television World* magazine since 1974. A few years ago, you used to have a page for your regular readers to write in, ask for help, make requests from other readers or advertise items, related to electronics. May I suggest that you reintroduce this page in *Electronics World* for your dedicated readers, as I am quite sure it will be beneficial to both, your company and us.

For example, I am at nearly retiring age and I have most of the issues since I started buying the magazines, which I wish to dispose off – at a fair price, of course – to anyone interested.

Thanking you for your excellent magazine and wishing you many more years of first-class service.

**Spyros Jacovides**  
UK

**Editor's reply:** Thank you Mr Jacovides for such an inspiring suggestion. We would like to take this opportunity to invite anybody who needs help with a technical or practical

problem to write to us at [EWletters@nexusmedia.com](mailto:EWletters@nexusmedia.com) and we will publish the material – or indeed identify experts – to deal with such queries.



**EMF problems?**

In the September issue (p16), Alasdair Philips suggested at the end of a very interesting article that mobile phone signals should be included in proposals to reduce exposure to (the possibility of) harmful effects of EMF, but a recent paper by Hamada in the *New Scientist* suggests that this may cause accidents by distracting drivers, due to the effects of more frequent switching between base station Tx's when signal strengths are weaker. This was suggested in a recent letter (*EW*, May 2005, "Going lower in frequencies") where Mayer waves (0.12Hz) are of the same order as those reported by Hamada ("roughly six times a minute"); silent trigger frequencies in brain process may be distorted or confusing.

Hamada's data is interesting because 3.3Hz is close to the first period-doubling of 1.87Hz, first reported – as a FREQUENCY – by Electronics World, in di Mario's article on low frequency counter he had constructed. This frequency (3.3) is on the boundary between  $\delta$  (deep sleep) and  $\Theta$  (hypnopomic and hypnagogic states) brainwave ranges,

which are beneficial; as is 15Hz, which Elizabeth Davies discussed in her article in *EW* (April 1993, pp 318-320). This is a "third" period-doubling of 1.87Hz (x8), in the "chaos" – according to Non Linear Dynamics theory ("two period – doublings, then chaos"), but it's still there and illustrated how sensitive these brain-body mechanisms are (sensitive dependence on initial conditions has been referred to as the Butterfly Effect).

This data may form part of theory (f) which Roger Penrose suggests is necessary (Road to Reality, page 786 et seq) involving objective reduction-gravitationally induced (GOR) in complex projective twister 8-space (t,x,y,z, real and imaginary components), which is a "passive" thing "painted" on "space manifolds, distorting space as it dries ("leakage") – page 995 (PR), under non-linear graviton. "Yet at some point, the theory will have to say something about the real-number aspects of physics..." (page 1006, RR), which is a long-held belief (e.g. Peano's set {0,1} only). We suggest that 1.87Hz is the basis on the new theory, that is: set {0, 1.87Hz, only} and there's good evidence for it!

Greg Hodowanec's letter ([www.padrak.com](http://www.padrak.com) or [www.SchumannResonance.com](http://www.SchumannResonance.com)) reports a 'Resonant frequency of the Aether' as being 1.855 x 10<sup>43</sup>Hz, before listing 1.855Hz (slightly off our value of 1.8655, from 4.669/2.502, bifurcation constant quotient) and period-doublings: 3.710Hz and 7.42Hz (NB no 5.565), ignoring the log of the mantissa (43), base 10! He then goes on, reporting 3.710kHz et al, all measured experimentally in coil tests.

**A G Callegari**  
UK

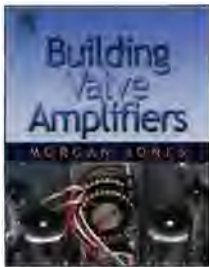




## Building Valve Amplifiers

Morgan Jones

Elsevier (Newnes)



I have worked with and built valve amplifiers for many years; I also have the author's other, more theoretical, books in my collection.

This book is to be highly recommended as it brings together all the necessary details to enable even the novice to build satisfactory valve amplifiers. More than that, it is a primer for electronic construction, setting out the correct way to do things so that, if followed, there is a very high chance that the equipment will work first time. This should give a tremendous boost to the novice constructor who may be apprehensive about valve technology and the high voltages involved. The princi-

ples here can also be applied to modern solid-state circuitry as well.

The book is logically laid out and starts with the design and layout (physical) of the equipment to be built. There are one or two examples of special circuitry but theory is kept to the absolute minimum and explained well where used. Several practical examples are shown, which should lead the reader to functionally sound as well as a pleasing layout.

The next section then covers the practicalities of metalworking, with minimal equipment, and the techniques required to achieve good results.

Once a chassis is ready, the builder will often wire the unit quickly in an effort to "get it working". The book cautions against this and sets out the logical sequence to be followed, to achieve both a neat and trouble-free wiring layout. There is an excellent section on the correct method of soldering; if followed, it should obviate 98% of soldering problems.

In addition, valuable hints are given on

the initial "powering up" of the equipment and where to look for faults. A comprehensive section follows this on the use, choice and building of test equipment.

Final sections have a commentary on various classical amplifiers as well as "performance tuning" of the reader's finished circuit. At the end of each chapter there is comprehensive bibliography giving further reading.

My only reservation was continued emphasis on safety, which experienced readers may find breaks things up a bit. That said this is essential for the novice in case the writer kills off his readership!

This book can be thoroughly recommended for experienced builders and novices alike. It will hopefully find its way into the Christmas stockings of many young electronics enthusiasts to encourage them in their hobby.

Ed Dinning

## Bebop to the Boolean Boogie, 2nd edition

Clive "Max" Maxfield

Elsevier (Newnes)



The famous book by Clive "Max" Maxfield is truly "an unconventional guide to electronics fundamentals, component and processes" as said by the subtitle.

The book is structured in two sections and a number of appendices, including a CD-ROM.

The first section's content covers all the aspects of contemporary digital electronic circuits. The book begins with the basics of electronics (voltage, current, Ohm's law) and semiconductor devices technology, but then progresses through the principles of Boolean algebra and the principles of digital circuit design.

Building up on such foundations, the second part is devoted to components and processes. It deals with IC technology (with emphasis on programmable logic circuits and ASICs), with circuit board fabrication and assembly, and then

focuses on multichip modules and some leading-edge processes such as optical interconnections, reconfigurable hardware, diamond substrates and nanotechnology.

The appendices are an integral part of the book's framework. They go in-depth of the digital design methodology, including positive vs. negative logic, Gray codes and linear feedback shift registers.

A large and well-done glossary ends the book, which then restarts in the companion CD-ROM, which is a gem in itself. In addition to the full content of the book, there is a bonus chapter devoted to the history of electricity, electronics and digital computers.

Here, Maxfield shows the best of his style, mixing deep knowledge of technical history with a great sense of humour and a strong passion for finding some (almost) unbelievable nuggets of trivia.

This chapter is of interest not only to students and professionals in the field of digital electronics but everyone who has some interest in electronics or computer science.

Maxfield's writing style is very similar to that of Robert Pease. Pease, chief scientist at National Electronics, is an acclaimed guru of analogue electronics. They both have a vast know-how in their

field of work and a light and entertaining way of writing and exposing even the most involved subjects.

In addition, I would also like to highlight the unconventional nature of this book.

Maxfield is a master in explaining the most complex concepts and theories in a few words. What makes him unique is the ability to "talk" to readers rather than give an academic lecture.

Of course, the colloquial and often humorous tone is not a cover for lack of knowledge or understanding of the theory behind each topic. Instead, it is a style of teaching that reveals, not only a vast knowledge of the digital electronics field, but also a great skill in teaching and explaining electronics.

On the whole, this is a book that deserves the acclaim it has received since the very first edition and it should be on the desk of everybody who is interested in digital electronics design.

Alberto Lobina

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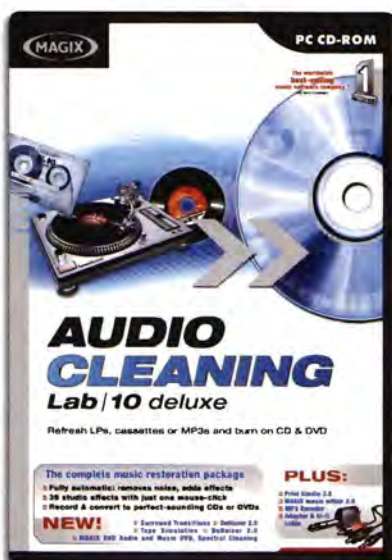
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Bridging the gap between games console and media hub, the Xbox 360 allows video streaming, video chatting, PC connectivity and will allow anything with a USB connection to talk to the machine; enabling hundreds of services. Also offering music and progressive scan DVD playback, Microsoft aims to break the mould with High Definition being the standard for the next generation of consoles. The machine will be available in two different packages; the base model and the premium package; which includes extended media functionality, wireless game-play and a hard drive. Available December 2nd.

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# Simple RAM programmer

The circuit diagram here is of a simple RAM programmer, which can be used for various purposes, usually in small robotics, automation and artificial intelligence applications.

- The 2114 is 1024\*4 memory
- 1024 memory location\*4bit data.

Here, all the addresses used are in decimal format rather than hexadecimal. In the circuit, the number of memory locations used is only 100, with 3 data bits each, leading to 100\*3 memory.

The RAM programmer performs very well if the circuit has been rigged up as shown.

This programmer is low cost and does not require a PC for programming it.

### Dos and don'ts

- Connect all the +5v terminals to the output of 7805.
- Until the RAM has been programmed don't switch off the main power, which will lead to a complete loss of data.
- Ideally, use battery cells, due to the use of step down transformers and home soldered diodes and capacitors.

### Changing of address

Sw1 is the switch used for address transition, such that it points to the memory locations. By continuously pressing the switch, the address of the memory location automatically changes one after the other, at a time period of approximately 0.65278 seconds.

### Writing into the RAM

First, the write switch Swr has to be in the write position.

Then by using Sw1, we can go to one of the memory locations. For example, if the bit

switches b1, b2, b3 are kept at the ground point, the data stored at the memory location is 000. Similarly, by removing the bit switches from the ground point b1, b2, b3 respectively, the data stored in the memory location is 111 in the same way. If only b3 is kept at ground point then the data stored is 110. That way, data can be stored into the RAM from 000 to 111. Using the switch Sw1 you can move on to different memory locations and write different 3-bit data into different memory locations from 00 to 99.

The switch Sw1 is only used for address transition. It has to be kept closed until the address location changes.

After the address changes to the next memory location, the Sw1 has to be opened to complete the writing part.

While writing, the "wr" has to be kept at write position until the complete program is written. After that has been completed – from address 00 to 99 – only then the "wr" can be moved to the read position for reading the data.

### Reading the information

First, all the b1, b2, b3 switches have to be moved away from the ground point. Then, the write switch has to be removed and kept at the read position. By pressing the Sw1 without releasing we can enable the 'read' of the information that has been written into the RAM.

Here, instead of driving LEDs, you can drive power transistors or opto couplers.

In this case, 8 LEDs are used to denote 000 to 111.

**S. Vinay Kumar**  
Janatha Nagar  
Indi

### Example 1:

Write the data as described to the respective memory location. Writing and reading the data is as above (keep Sw1 closed until reading takes place from address 00 to 99). You'll notice that the LEDs begin to shift toward the right of each other (it's a seven-segment display).

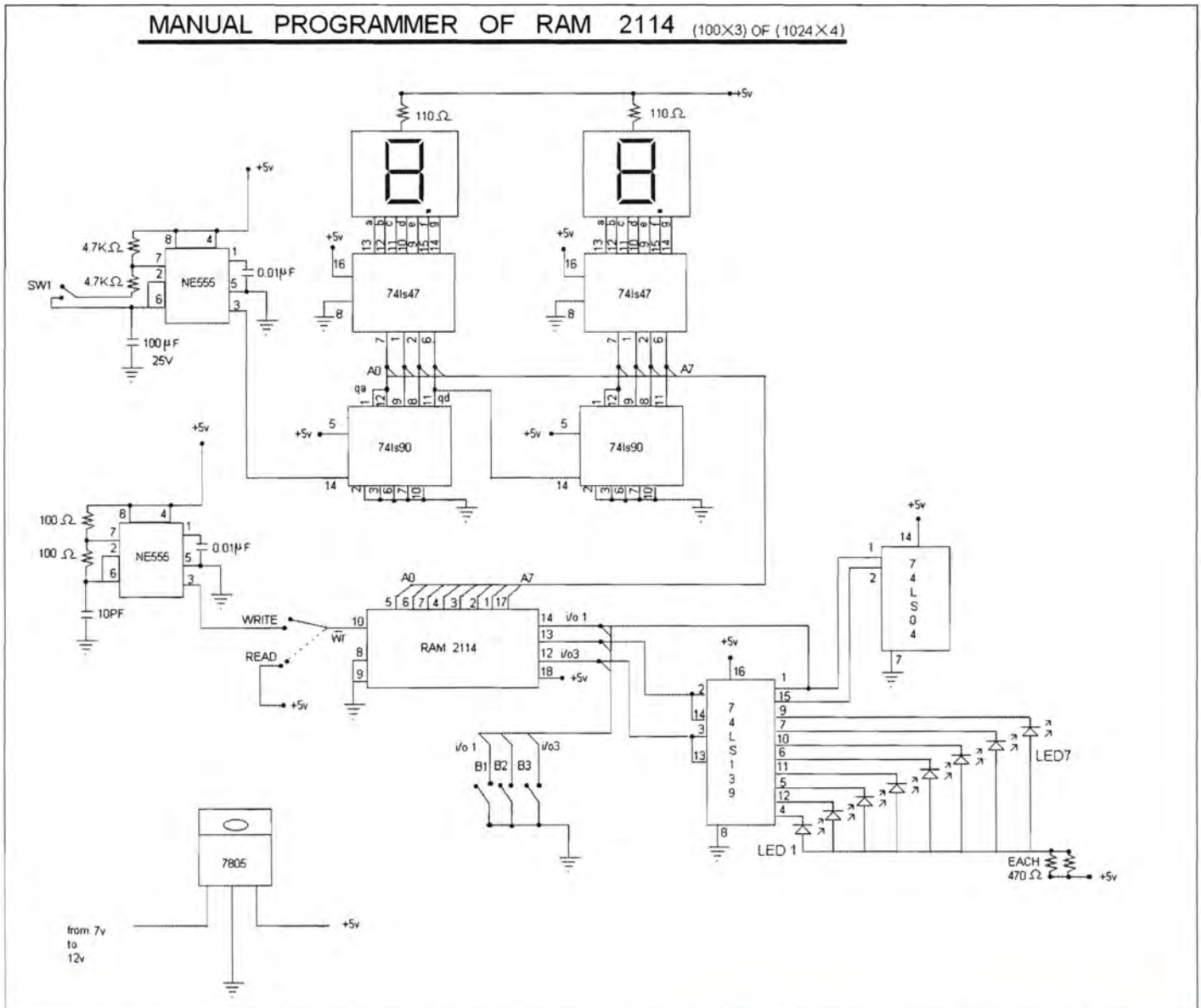
Pulses are created by Sw1. The LEDs begin to shift on the left when each clock pulse has finished with the 7-segment display. After shifting right and left to the next clock pulse, the first LED begins to glow for the next 10 clock pulses or so.

Similarly, shifting one location requires 10 clock pulses and this continues up to the 99th memory location and, then, the cycle continues. While reading takes place, you'll notice that at 000 the first LED will always glow, at 001 the second LED glows, at 010 the third, at 011 fourth, at 100 fifth, at 101 sixth, at 110 seventh and, finally, at 111 the eighth LED will glow.

This example is for the complete usage of 100 memory locations 3 data bits.

Memory address	data	Memory address	data	Memory address	data
00	000	33	001	66	101
01	001	34	001	67	101
02	010	35	010	68	101
03	011	36	010	69	101
04	100	37	010	70	101
05	101	38	010	71	101
06	110	39	010	72	101
07	111	40	010	73	101
08	111	41	010	74	101
09	110	42	010	75	110
10	101	43	010	76	110
11	100	44	010	77	110
12	011	45	011	78	110
13	010	46	011	79	110
14	001	47	011	80	110
15	000	48	011	81	110
16	000	49	011	82	110
17	000	50	011	83	110
18	000	51	011	84	110
19	000	52	011	85	111
20	000	53	011	86	111
21	000	54	011	87	111
22	000	55	100	88	111
23	000	56	100	89	111
24	000	57	100	90	111
25	001	58	100	91	111
26	001	59	100	92	111
27	001	60	100	93	111
28	001	61	100	94	111
29	001	62	100	95	000
30	001	63	100	96	000
31	001	64	100	97	000
32	001	65	101	98	000
				99	000





**Example 2:**

In this program we are using only 8 memory locations out of the 100 3-bit memory.

Here, the LEDs glow in the order 1,3,5,7 and then 2,4,6,8. After writing the program read the data at the memory locations 00 to 07.

Memory address	data
00	000
01	010
02	100
03	110
04	001
05	011
06	101
07	111





# Printer port based, wide-ranging, low current meter

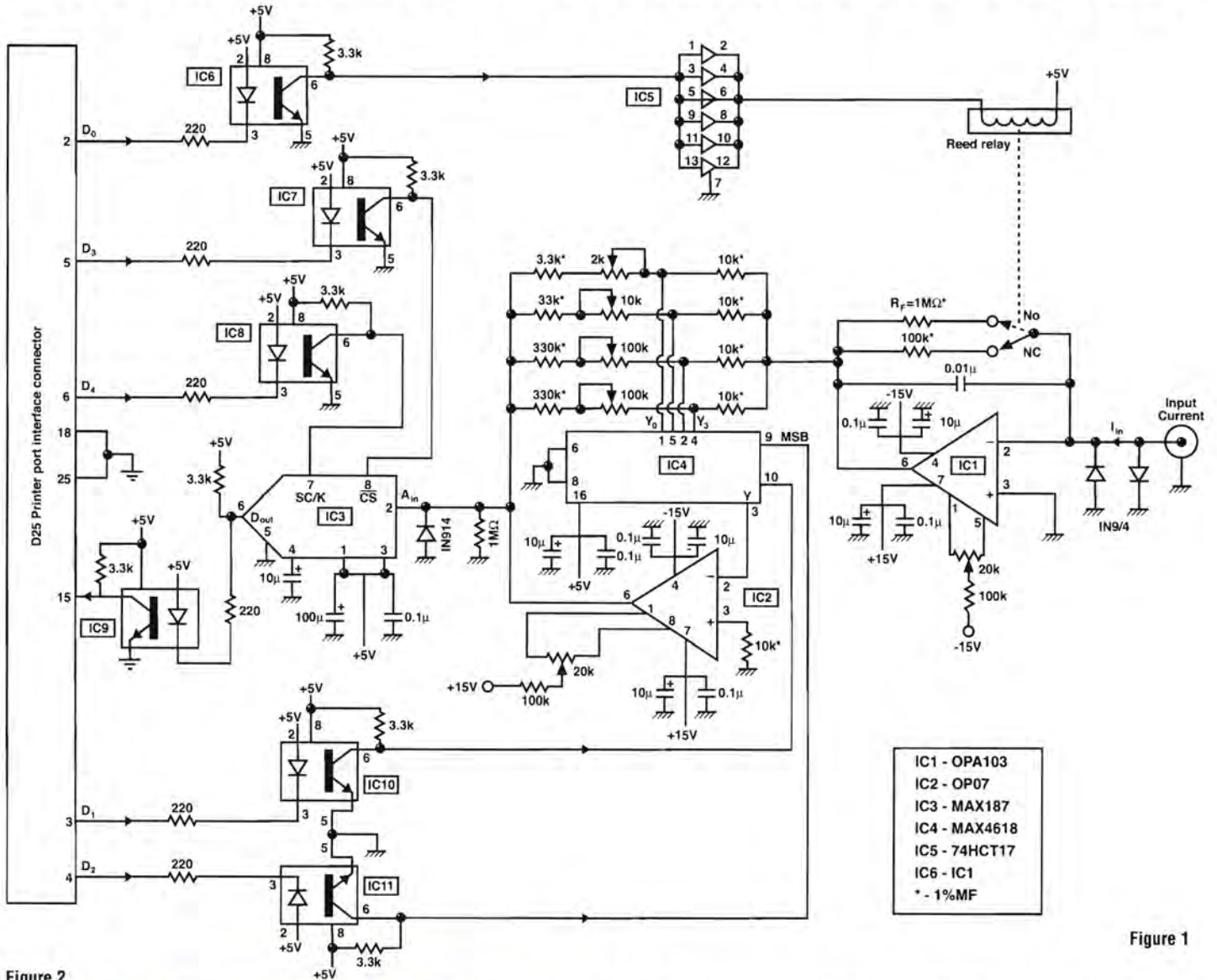


Figure 1

Figure 2



Measuring very low currents in the range of nA to mA is one of the prime requisites in many of the R&D experiments, like semiconductor device characterisation, ion implanters, vacuum measurements, etc.

On many occasions, very costly multi-purpose, stand-alone, low current meters with RS232/GPIB connectivity are used for making computerised low current measurements. Alternatively, for such applications one can use a simple wide-ranging low current meter as shown in Figure 1.

This inexpensive low current meter uses readily available components and the printer port of a PC, enabling computerised measurements without requiring any general purpose or tailor-made DAQ board or IEEE488 interface board.

Using this circuit, we can measure wide ranging low currents, spanning from 0.1nA to 100uA in four user-selectable ranges of 0-100nA, 1uA, 10uA, 100uA with a resolution of better than 50pA. The circuit employs electrometer principle of low current measurement and uses IC<sub>1</sub> (OPA103), a



very high input impedance and low input bias current op-amp in the current to voltage converter (CVC) topology, which accepts the input current and produces an output voltage as depicted in **Equation 1**.

$$V_{out} = -(I_{in} \times R_F) \text{ Volts} \quad (1)$$

where  $I_{in}$  is the current to be measured in Amperes and  $R_F$  is the feedback resistance in Ohms. By switching  $R_F$  to different values like  $1M\Omega$  and  $100k\Omega$ , an output of  $100mV$  to  $10V$  is obtained at the CVC output.

In the  $0-100nA$  current range, with  $R_F = 1M\Omega$ , an input current of  $0-100nA$  results in an output voltage range of  $0-100mV$ . For other ranges,  $R_F$  is set at  $100k$ .

Selection of the  $R_F$  is achieved by a  $5V$  Reed relay driven by a hex buffer ( $IC_5 - 74HCT17$ ), which is controlled by  $D_0$  line of the DATA PORT (@  $0x378$  address) of the printer port. A logic 0 at  $D_0$  powers the relay and selects

$R_F = 1M\Omega$ , while a logic 1 sets  $R_F = 100k\Omega$ . The output of the CVC is further amplified by a programmable gain amplifier (PGA), realised by a precision inverting amplifier ( $IC_2 - OP07$ ), a 4:1 low voltage CMOS analogue multiplexer ( $IC_4 - MAX4618$ ) and a gain setting resistor network.

The gain ( $G$ ) of this stage is software settable to 41, 4.1 and .41 by controlling the address inputs of the multiplexer from  $D1$  and  $D2$  lines of the DATA PORT. The combined gain of the CVC and the programmable gain amplifier is chosen such that an output of  $0-4.096VDC$  is produced at full-scale currents on all ranges. This output is fed to a 12-bit serial ADC ( $IC_3 - MAX187$ ), selected for features like on-board reference, built-in S/H, low power consumption ( $10\mu A$ ) and low conversion time ( $8-10\mu s$ ). The data communication between the printer port and the circuitry are opto-isolated ( $IC_6 \dots IC_{11}$ ,  $6N136$ ) for PC

safety and for floated current measurement.

A Windows-based graphical program, LOWIMEAS.VI, developed using LabVIEW6i is used for computerised measurements, although many other languages like C can also be used for the program development. Its user interactive front panel is shown in **Figure 2**.

This software supports user-selectable AUTO and MANUAL measurement modes. For making the current measurement in the AUTO mode, initially the PC selects the highest current range ( $0-100\mu A$ ) by selecting  $R_F = 100k\Omega$  and  $G = 0.41$ . After a  $50ms$  relay settling time,  $/CS$  of the MAX187 is pulled low, initiating an A to D conversion. Upon detecting end-of-conversion by low to high transition at  $D_{out}$  of the ADC, the PC acquires the 12-bit serial digital data from MSB to LSB by sending 12

clock pulses serially to SCLK and reading the  $D_{out}$  at every falling edge of the SCLK. The 12-bit serial data acquired is then related to the input current as per the following relationship:

$$\text{Input Current} = (\text{decimal value of acquired 12-bit data}) \times 4.096 \times (\text{conversion factor}) / 4096.$$

The measured value is graphically displayed on a current meter as well as on a numerical indicator. If the measured current value is less than 10% of the full scale of the present current range, the PC selects the next lower range and the measurement is repeated. However, if the current measured is  $>100\%$  of the full scale, the next higher current range is selected.

**Suresh Kannappan**  
Materials Science Division  
Indira Gandhi Centre for  
Atomic Research  
Kalpakkam  
India

## 1.5V dry cell tester

Users of battery-operated equipment are frequently confronted with the problem of when to renew the batteries, or at least check their condition. One might suggest a DMM, but to obtain an indication of the state of the battery it must be tested under load. The circuits shown here illustrate two design approaches that use LEDs as a 'state of condition' indication.

Circuit 1 uses three LEDs, green for good, red for bad and orange as the transition state from good to bad. The battery type is selected by means of a 4-position rotary switch and this provides suitable loading to indicate the condition of the battery under load. Two comparators with reference volt-

ages  $V_{ref1} = 1.10V$  and  $V_{ref2} = 1.40V$ , determine the trigger levels for the red and the green LEDs to become active. The orange LED controlled by transistor  $Q_1$  only lights up if the battery voltage is between the pre-selected reference voltage levels of  $V_{ref1}$  and  $V_{ref2}$ . Hysteresis has been applied to both comparators to prevent oscillations when changing states. Once the battery type has been selected, all the user has to do is to hold the two measurement probes to the battery under test. The circuit operates from a  $\pm 5V$  power supply (not shown).

Circuit 2 uses a dual colour LED to indicate the three states of the battery. This circuit employs a quad op-amp

TL084 to implement a  $30Hz$  square wave oscillator, a  $1.25V$  reference voltage and two comparators. The square wave oscillator output is attenuated to  $300mV$  p.p. and is AC-coupled to the  $1.25V$  reference voltage. This provides a square wave with voltage levels of  $1.40V$  (GOOD) and  $1.10V$  (BAD), which is applied to Comparator 1. The  $1.25V$  reference voltage was selected to fall midway between the GOOD and BAD condition indication thresholds. Therefore, a battery voltage of  $>1.4V$  will cause the output of comparator 1 to go 'low' and the output of comparator 2 to go 'high', operating the green LED.

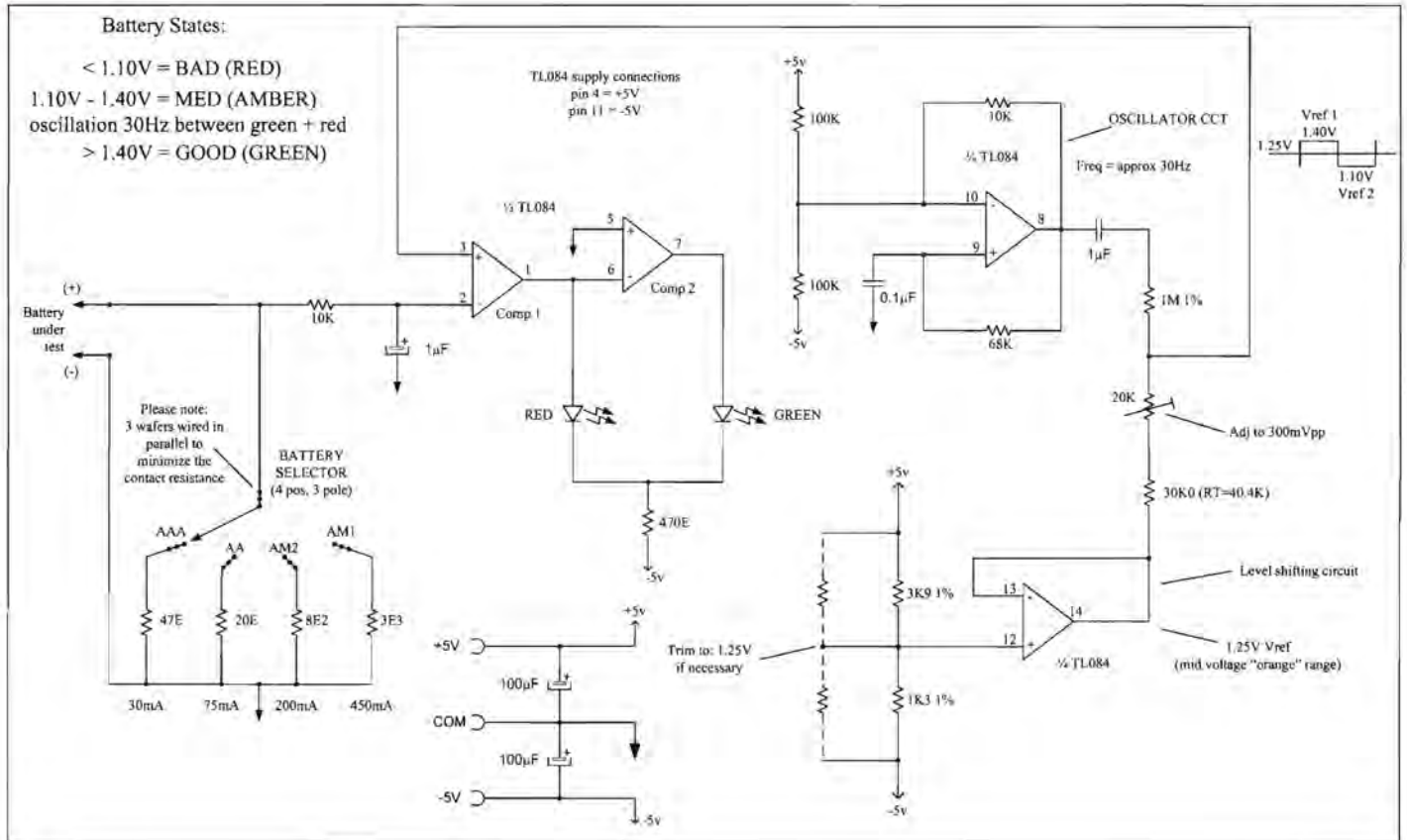
A battery voltage level of

$<1.1V$  will cause the output of comparator 1 to go 'high' and the output of comparator 2 to go 'low' thus operating the red LED. Battery voltage levels between  $1.1$  and  $1.4V$  will cause both comparators to change state, switching at a frequency of approximately  $30Hz$ , hence alternating between the red and the green LEDs. The human eye averages the alternating LED colours and interprets them as orange i.e. indicating the transition state of the battery between good and bad. Like circuit 1, the circuit operates from a  $\pm 5V$  power supply (not shown).

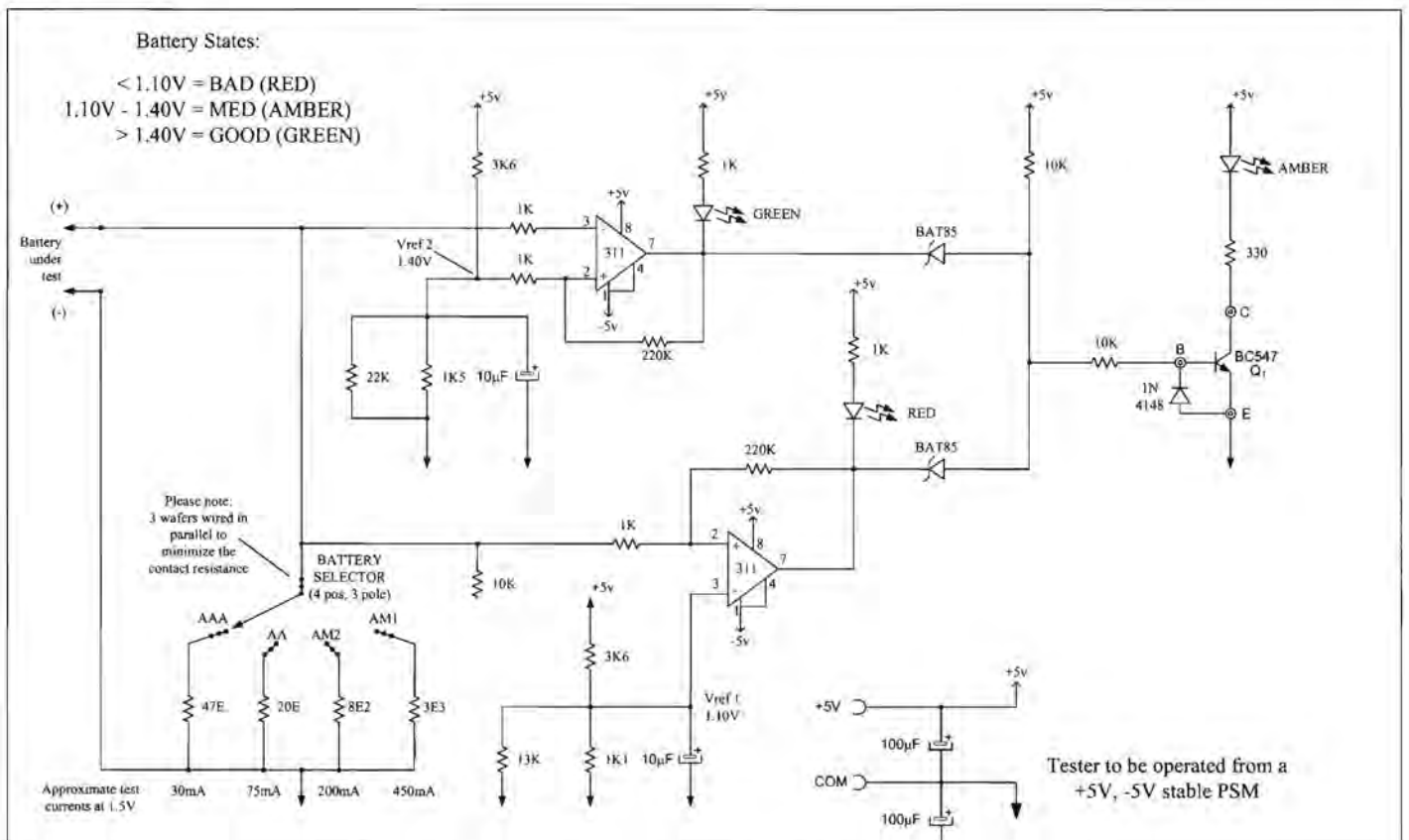
**See diagrams on the following page**



# Circuit Ideas



Circuit 1



Circuit 2

**Gunter Vath**  
 School of Electrical, Electronic and Computer Engineering  
 University of KwaZulu-Natal  
 South Africa





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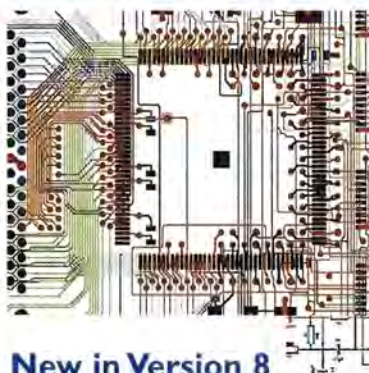
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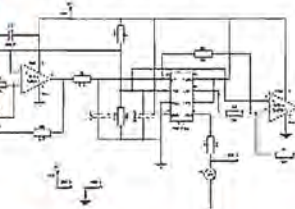


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### EMC cabinet for electronic and networking applications

Enclosure Solutions has introduced the Verak EMC range, which provides more than 80dB attenuation at 100MHz. Intended for use in electrically noisy environments, such as switch rooms and the factory

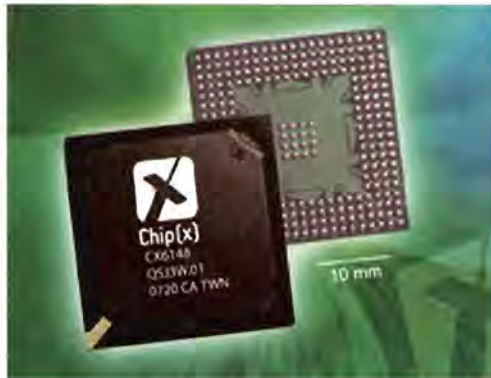
floor, and available in heights of 27 to 42U, and 600 x 600, 600 x 800, 800 x 600 and 800 x 800 plan sizes, the Verak EMC is rated at 750kg static load capacity.

The 2mm steel framework is exceptionally strong and rigid. The EMC steel panels and doors are double skinned and the EMC glass door is a 4mm-thick laminated construction with a fine metal mesh encapsulated between the two glass sheets. Both steel and glass doors have a unique closing mechanism to ensure the integrity of the EMC seals; a swing handle controls a four-point over-centre cam closure that exerts the correct pressure on the gaskets, thereby avoiding over-compression and ensuring that screening performance does not degrade over time with repeated door openings.

Cables can be brought into the rack from the top, through the bottom and through 5U or 10U high cable entry panels above or below shortened front or rear doors. Screened gland plates enable cables to enter without compromising the EMC performance.

[www.apw.com/enclosuresolutions](http://www.apw.com/enclosuresolutions)

### Structured ASIC with embedded PCI Express PHY



Structured ASIC firm ChipX launched the CX6100 family of devices, fabricated in eight-metal 0.13µm process and integrating a silicon-proven PCI Express (PCIe) PHY core.

The new CX6100 family comprises twelve devices for a wide range of applications, ranging from computing, storage and instrumentation to networking. The embedded PCIe PHY is compliant with the current 1.1 version of the specification and is available in 1, 4 and 8-lane options. Along with the embedded PHY, ChipX is offering an optional PCIe compliant controller. The PHY offers

complete PIPE interoperability for customers wishing to use their own PCIe controller. With the optional PCIe 1.0a compliant controller, designers can quickly develop root port, bridge and endpoint

designs. The controller supports up to 8 VCs and up to 6 BARs. It features configurable retry buffers and support for up to 4kB payload sizes. The controller is supplied complete with simulation models, driver software examples and all documentation.

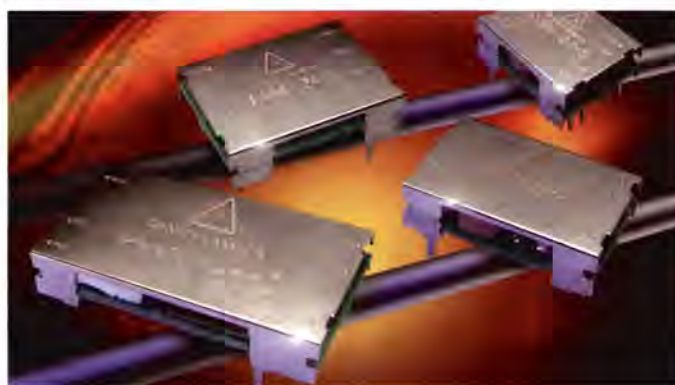
Device densities range from 240k to 1.8M ASIC gates, up to 1.1Mbits of embedded SRAM and maximum operating frequencies up to 250MHz across the die. Four on-chip, configurable, low-jitter PLLs support output frequencies from 10MHz to 1GHz.

[www.chipx.com](http://www.chipx.com)

## Surface mount version of PSS & PSD DC-DC converters now on

Lambda's successful PSS and PSD series of ultra compact single and dual DC-DC converters are now available in surface mount technology (SMT), announced the power supply manufacturer. In this version they will be ideal for applications where reduction of size and weight are critical, which, combined with their extensive features, makes them particularly suitable for the telecommunications, datacommunications and instrumentation sectors.

The converters can accept a range of input voltages and are



fully self-contained, requiring no external components and allowing easier system integration. The range offers 48 dif-

ferent models in the single output PSS series range and 20 models in the dual output PSD series range. Both series are

available in 5V, 12V, 24V and 48V input versions, each with a nominal output voltage of 3.3V, 5.0V or 12/15V and with output currents ranging from 0.4A to 2.5A, depending on the model selected.

The units operate with an output voltage accuracy of ±5% and with a typical efficiency of 73-84%, depending on the model chosen. The dimensions of the PSS and PSD series range from 20x16x8mm up to 41x26x8.5mm.

[www.lambda-europe.com](http://www.lambda-europe.com)



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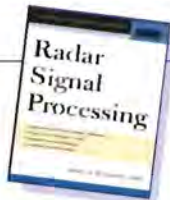


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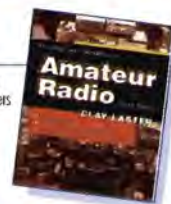
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Clay Laster

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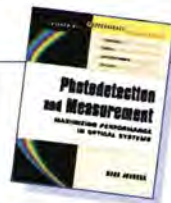
Mark Johnson

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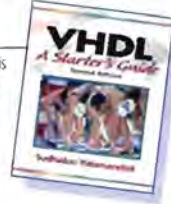
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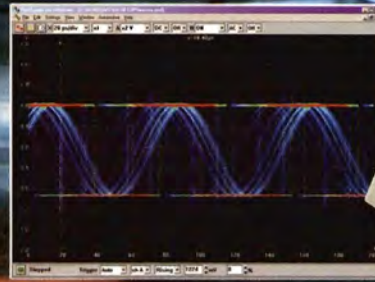
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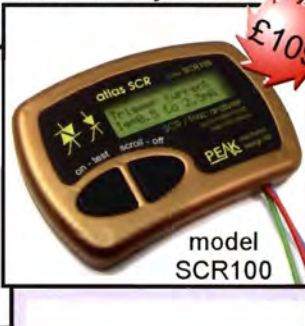


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<b>LOGIC ANALYSERS</b>						W&G PFA-35 2MB/s Digital Communications Analyser	3950	119		
Agilent/HP 16500C Logic Analyser Mainframe	1650	55				<b>TV &amp; VIDEO</b>				
Agilent/HP 1650B 80 Channel Logic Analyser	950	55				Minolta CA-100 CRT Colour Analyser	1950	59		
Agilent/HP 16510B 100MHz Timing 35MHz State 80Ch Card	890	35				Philips PM5418TSX/Y/C TV Pattern Generator	3250	98		
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