ELECTRONICS WORLD

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EMF: danger to our health?

Multithreading in the new crop of game consoles

INSIDE: mixed signal and analogue design • image processing • implementing RAID storage • medical electronics and more...

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Front cover image by Gary Weston

Electronics and medicine: who needs whom first?

A recent Medical Devices Technology Innovation Forum produced several interesting observations. First came the surprise. When invited to attend the Forum, the first thought that came to my mind was "Isn't this gathering for doctors only?" The surprise (a pleasant one!) was that the event was well attended by electronics engineers – researchers, practicing developers, managers and even company directors. Clearly, this is an area that keeps us electronics folk intrigued.

The second observation was: We are trying to push something that not many medical personnel and consultants are familiar with. Technologies on show ranged from piezo "legs" to Bluetooth-enabled sensors. But, after many roundtable discussions, it was obvious that not many in the medical profession – or those involved in spending on behalf of the hospitals – knew their Bluetooth from their ZigBee, Wi-Fi from their NFC. They knew that they wanted a non-invasive, continuous, low-power glucose monitoring device, but once that info is gathered, where do you send it, who to, for what purpose (if you are in the park suffering an arrhythmia, and your wireless gadget sends this information off 'somewhere', will your doctor give you a phone call asking you to pop into your local hospital or will he come and look for you in the park?) and how can it be put to good use.

The third observation was, (surprise, surprise!), there's not enough money to spend on new, all-encompassing technologies in the health care sector. One mobile communication expert said that a way forward would be to "rip apart the old hospitals and build new ones equipped with communications systems and smart devices". I can't see this happen for three reasons: lack of money is the first and biggest reason – nobody has that kind of money to spend, it seems. The second and third reasons are the medical sector is slow to develop (so unlikely to adopt the latest techy developments) and it is highly fragmented (nothing can be re-built unless parties unite). Medical personnel are highly sceptical of whether a new technology will bring patient benefits and, hence, unlikely to spend money on solutions unless they bring direct benefits. And to see whether there are direct benefits, they need data first. Data cannot be had unless somebody starts installing these systems or large-scale trials begin.

The fourth observation is: This is a tricky sector for us engineers. There are far too many regulatory issues that take a very long time to go through, which leaves a solution almost obsolete by the time it is approved. Who wants to work on a product that may or may not be approved for use – in ten years' time!

The fifth observation that follows from observation four is: We (in the engineering sector) have many interesting technologies that could bring many benefits and advantages to the medical sector. But, these are likely to enter this sector from the patient's side first, rather than from hospitals. Health-monitoring mobile phones and sensor-laden clothing will entice many individuals to go out and buy them, but then there will be the need to send that data off to a health 'place' for dissection and intervention. Hospitals are unlikely to drive this one forward.

Sixth observation (and to me the most baffling one): Many of the communications protocols proposed for uses in the health sector are working in the microwave range – 2.4GHz. Medically, this is the frequency most absorbed by the body, hence potentially the most dangerous one. The jury is still out whether mobile phones pose a danger to our health and, yet, there were discussions to have foetal monitoring and data transmission based precisely on this range.

Who'd like to handle this one ...?

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Bluetooth stays out of CPE

Bluetooth might be a success story for silicon supplier CSR, but this technology's penetration looks limited to certain applications only.

"Bluetooth is not appearing as a requirement [in integrated broadband firmware] – we have the capability but the customers don't want it," said Adam O'Hare, business director at the privately owned Voice Integration over Network Edge (ViNE) solutions developer DataFlex.

"We find that Bluetooth is centred around the mobile environment, but not for businesses and its integration into CPE [customer premise equipment]," he added.

CSR from Cambridge did state that, to date, Bluetooth has entered 1000 products, but so far, that's been only in a variety of mobile phones. "Mobile phones remain by far the largest single market for Bluetooth silicon," was written in a recent CSR press release.

On the other hand, WiMax, the farther-reaching wireless communication standard that is a bit less established than Bluetooth, seems to be attracting more attention, even though no customers have committed to spending on integrating it into boxes just yet either. "Several customers have asked for WiMax; we have a couple of projects for broadband, but not to integrate it into our devices yet. We have the capability but nobody is asking for its integration."

Bluetooth is a 2Mbit/s wireless standard that connects devices within a 10m radius. It promises to remove the need to connect single environment systems with wires. WiMax is a 280Mbit/s wireless standard, which aims to connect users to broadband services within a 30-mile radius and whilst in motion. The two technologies do not compete.

Lone workers in part responsible for rise in IMS use

The number of lone and home workers is rising and, as such, this trend is partly responsible for fuelling IMS (IP Multimedia Subsystem) solutions. So says TeleWare, the firm that pioneered 'intelligent number', where a person can be contacted on the same number, irrespective of location, connection medium or device, anywhere in the world. TeleWare launched the concept over ten years ago but recently ported it to a SIP (Session Initiation Protocol) based architecture that lies at the core of IMS.

"When companies adopt such services, they find that accessibility, accountability and productivity of their [lone and home] workers increase," said Leslie Hansen, TeleWare's marketing director. "The market [for IMS services] will grow as the number of home and lone workers and desk sharers increases."

IMS combines IP and traditional telephony but is access-agnostic. It supports any type of IP session over a network, whether parts of it are either of the fixed, LAN-based, mobile, CDMA or GSM type.

"Vendors such as Nortel, Lucent, Motorola, Siemens and Ericsson are all moving towards an IMS solution, although, for many of them, this is very challenging since their hardware and software architecture is, in most cases, highly inter-dependent," said Geoff Haworth, TeleWare founder and chairman.

Intel recently launched its second generation, AdvancedTCA (ATCA) blades focused on IMS.

"We are moving on to a [telecoms] model with customer-defined, 100s of services, selectable and available when asked for. A Service Delivery Platform will deliver this service agility and at the core will be IMS," said Richard Lissenden, infrastructure director at Intel.

IMS uses SIP, specifically developed for multimedia communication. SIP establishes IP connections between terminals. This can then be used to carry any IP traffic, for example interactive game sessions, push-to-talk over cellular, instant messaging or video and multimedia messaging.

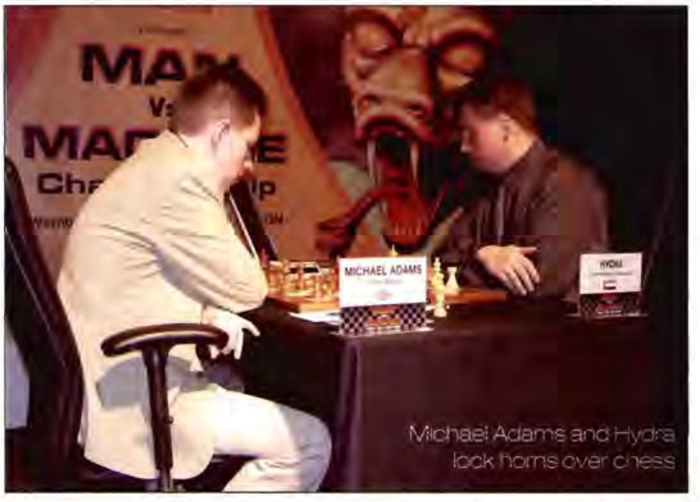
When a subscriber makes an initiative to talk, chat or videoconference, it's completely left to the network to figure out where the subscriber is and his/her preference for completing the session.

Machine beats man in chess

The most powerful chess computer ever developed – Hydra – made a worldwide debut by beating the UK's leading chess grandmaster, Michael Adams, in a six match tournament.

Hydra was created specifically for this reason. It is a Linux supercomputer cluster that uses 64 Intel 64-bit Xeon 3.2GHz processors made in 90nm process technology. The result is a processing power of over 200 standard PCs. The cluster comprises 16 nodes of four computers, each with 32GB of memory available. However, the difference from other computers such as IBM's Big Blue for example, is that each of the 64 processors in the cluster relies on an FPGA Virtex-II Pro 70 card from Xilinx for acceleration.

Hydra's chief developer, Chrilly Donninger, said: "We use the FPGAs as accelerator cards. The beauty of FPGAs, unlike ASICs, is that they are reprogrammable hardware. Every evening, after the chess tournaments take place, I go and reprogam the FPGAs."



Michael Adams and Hydra lock horns over chess

It takes Hydra only one second to analyse 200 million chess moves and select the best one. This includes projecting the game ahead by 18 to 40 moves, which is six more than what Deep Blue did.

"The tournament between Deep Blue and Kasparov of several years ago was a publicity stunt for the two of them. We are trying to prove that our concept of a mixed Linux system with FPGA accelerators works. This is the first FPGA-based supercomputer that exists and works. Chess is hard to parallelise because it is evolutionary, so this is done on the PC and accelerated with the FPGAs," said Donniger.

The Hydra system is applicable to other uses too, including security, DNA and fingerprint matching, code breaking, space travel calculations and complex systems simulations among others.

Smart clothing firm seeks partners

A two-year old spin-off from the University of Manchester is looking for commercial and technology collaborators and partners for its intelligent clothing. Smartlife Technology uses its homegrown sensors, specifically developed to be integrated into everyday clothing, such as undergarments for example, to monitor the wellbeing of the wearer.

"We use a range of sensors – ECG [heart], temperature, movement, pressure – to measure a range of body statistics. These are seamlessly integrated into clothing – and the wearer cannot notice anything different – to monitor the heart, muscle distortion and even brainwaves, if integrated into hats," said Mark Pedley of Smartlife Technology.

"The integrated garments are totally flexible and washable."

The original idea was the brainchild of two departments at the University of Manchester – Biomedical Engineering and Textiles. To date, funding has come from the Asia Pacific, but the company is now looking for partners to commercialise its solution in two specific areas: for the so-called 'first responders' – firefighters, ambulance staff etc, and in sport and wellbeing.

The first commercial prototype is expected in six to twelve months' time.

Electronics companies are being invited to apply for a chance to win a Queen's Award for Enterprise. The Awards are open to any UK-based organisation with two or more people, which has excelled in any of three categories: international trade, innovation or sustainable development. The deadline for applications is October 31st 2005. This year, 789 applications were made and 137 business awards were announced – the highest total for 10 years. Stephen Brice, Secretary of The Queen's Awards Office said: "Unlike other award schemes, there is no set number of Queen's Awards made each year and it costs nothing to enter." www.queensawards.org.uk

Ω

MEDEA+, the industry driven pan-European programme for innovation and advanced cooperative R&D in nano- and microelectronics is inviting interested parties to propose projects that could potentially start in the first half of 2006. Project outlines can be submitted at any time and will be evaluated continuously. Project outlines submitted before August 20, 2005, if found eligible, will pass the full evaluation and selection process and will receive the MEDEA+ label before the end of this year. MEDEA+ expects that an open call for projects with a continuous evaluation process of proposals will enable all stakeholders to better exploit synergies in trans-border cooperation. www.medeaplus.org

Ω

Britain has the ability to finance, develop and launch its own mission to find life on Mars. So said Prof Colin Pillinger at a recent Yorkshire Science and Technology Network (YSTN) event. Prof Pillinger led the Beagle 2 mission to land a probe on the red planet. He said that British industry and the government could finance a mission that will cost around £200m, but decision-makers would have to "be brave" and get behind it.

He added that he is currently negotiating with the European Space Agency to seek support for a second mission in 2011. YSTN was launched earlier this year by regional development agency Yorkshire Forward to improve links between academics and the business world and raise levels of innovation.

A team of international scientists has created a prototype that demonstrates a single charged atom on a silicon surface that can regulate the conductivity of a nearby molecule. The team tested the transistor potential of a molecule by using the electrostatic field emanating from a single atom to regulate the conductivity of a molecule, allowing an electric current to flow through the molecule. These effects were easily observed at room temperature, in contrast to previous molecular experiments that had to be conducted at temperatures close to absolute zero, and with much smaller current amplification. Computers and other technology based on this concept would require much less energy to power, would produce much less heat and run much faster.

Ω

NEC and the MIRAI project (Millennium Research for Advanced Information Technology) jointly development a low dielectric constant (low-k) film that will lead to power reduction in advanced LSIs. The low-k film contains very tiny, molecular-scale pores introduced by a novel molecular-pore-stacking technique. This will allow to double the interconnect density on LSIs compared to that of 65nm-LSIs and reduce interconnect parasitic capacitance by 16%. Such characteristics make suitable for use in future 45nm-node LSIs (70nm spacing).

Ω

Freescale Semiconductor and the University of Florida have created the industry's first double-gate transistor model or FinFET. It is engineered to pack more computing power into less space and reduce power consumption, while using existing semiconductor manufacturing processes. FinFET is an innovative design of a MOSFET, where the silicon is etched into a fin-like shaped body of the transistor and the gate is wrapped around and over the fin, hence a double-gate structure. As conventional planar transistors continue to shrink, so does the chance to control the charge carriers moving through the transistor when using only a single gate. The double-gate transistor mitigates this difficulty by introducing an additional gate to enhance control, paving the way to continued shrinkage.

Dial M for medical

Vodafone, one of UK's largest mobile phone operators is actively promoting the handset as the perfect health monitoring and data-storing device. "We see the mobile phone as a gateway in health," said Robert Childs, research manager in the R&D group at Vodafone. "In a discreet way, it collects data off the user and by just pressing a few buttons that information is sent securely over our network."

However, since the health service does not have a standard allocated to the collection of data from body sensors just yet, this proves to be the main stumbling block for Vodafone and the handset makers. "The problem is the lots of sensors and number of technologies [they can use for communication] such as NFC – promoted by Sony and Philips, RFID, ZigBee, Bluetooth, Wi-Fi and others. For us, it'll be tricky to include chipsets in the mobile phone to operate with all those standards. So, we'll need to think standards," said Childs.

Vodafone is at present involved in a health trial in Maastricht, The Netherlands, where the mobile phone's Subscriber Identity Module (SIM) acts as a backup to the health card called Gesundheit. Childs says that the user's mobile phone's SIM card acts as an information holder for prescription and health information that doctors and pharmacists can share.

New member joins R&S SMU signal generators

Rohde & Schwarz is fading out its SMIQ vector signal generator range, which fits in the upper midrange category, to replace it with the SMJ100A. The SMJ200A was built from the ground up, based on new synthesiser technology. It offers a high signal quality and a wide range of real-time signals. With a frequency band of between 100kHz and 6GHz, it covers all of the important aspects of digital RF transmission. The internal optional baseband generator can handle a large number of digital standards including 3GPP FDD, HSDPA, CDMA2000, WLAN IEEE 802.11a/b/g and WiMax.

Rohde & Schwarz's SMJ100 vector signal generator

The R&S SMJ100A is part of R&S's SMU family of vector signal generators, of which the SMU200A series offers two fading paths and a great degree of flexibility for R&D applications and testing base stations. The SMATE200A is also a high-end instrument, suitable for chip tests in production. Like the SMU200A but at a lower price range of £13,000, the SMJ100A is also good for carrying out tests on mobile phone base stations, WLAN cards and handsets.

Wireless communication systems are not reaching hospitals

Wireless communications and telemetry are not as widely used in hospitals and clinics as first envisaged. Even though communication protocols could be used to collect and transmit patient data on to various networked devices that medical personnel can use, or even remotely control, it is rarely applied.

"Wireless [in hospitals] is doable, but I can't see it as something that the NHS will be buying," said Steven Matthews, from Plextek, Cambridge-based electronics design house that specialises in systems design for medical applications.

"Then, there're the spectrum issues," he added. "In the US, the FCC has a specifically allocated spectrum for medical telemetry. We've just installed a wireless system in the 600MHz range there. Here, we are using the ISM band in 2.4GHz spectrum, which is getting very crowded."

Jason Martin, product manager at the recently created medical group at NEC Electronics has been promoting his company's ZigBee products. He says that ZigBee has automation qualities suitable for hospitals. "Although I've been doing this for only a couple of weeks, I don't see a great need for wireless [among the medical community]. I only see a slight market but there isn't a great level of discussion going on."

Although ZigBee is becoming popular in industrial automation, the jury is still out whether it will be the protocol of choice for hospitals.

"Bluetooth and ZigBee are disastrous when it comes to power. They are claimed to be low power standards, but the current is some 20mA for ZigBee and 30-40mA for Bluetooth, so they are a real disaster for current consumption [in battery-operated devices]. Also, the ZigBee frequency is at 2.4GHz. This is the main frequency that is absorbed highly by the body," said Richard McPartland of electronic systems design firm Toumaz Technology.

Medical design is largely avoided by engineers, says consultant

Designing electronic devices for the medical field is an area avoided by many electronic developers because it is fraught with regulatory and cost challenges. So says Dr Kevin Yallup from the UK-based Technology For Industry Ltd, an independent consultancy that draws on 25 years of experience in the microelectronics industry.

"All the regulatory issues [necessary to get the device through to market] can take seven years. This is for anything [any type of device] that goes through the body, that's why so many [designers] stay clear of it," he said.

Electronics-type devices that may be used in-vivo could be microfluidic pills in diagnostics, intelligent catheters or, indeed, implants. This will also have implications for a new generation of nanotechnology devices most of which are aimed at going through the body, for example for identifying cancerous cells and destroying them by applying medication locally.

These and any new devices will also face a struggle to be accepted by doctors and hospitals. This is cited as another reason why electronic designers avoid spending years on developing devices for the medical field, says Dr Yallup. "These devices have to be accepted by the medical community; it is all linked to costs and patient benefits. Then, the medical market is slow to develop and it's fragmented."

However, for all of those designers who are keen to get involved in supplying medical solutions, there's a light at the end of the tunnel. "Any [electronic or mixed type] device [in medicine] that operates externally from the body is easier to regulate, so you see more of them [around]," added Dr Yallup.

Healthy Aims project requires commercial partners

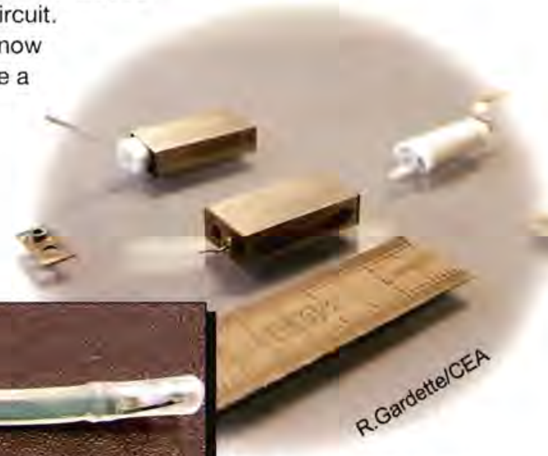
EC-funded, €26m, four-year health care project called Healthy Aims is looking for new partners to extend research and commercialise developments into areas such as implantable wireless communications devices, sensors and batteries.

Dr Diana Hodgins, project coordinator for Healthy Aims and the managing director of a microsystems design company European Technology for Business, said that the project needs to develop a wireless communications standard for a Body Area Network, where implants can communicate from inside the body to distances of up to 3m. "We are interested in partnering on this project and others, such as commercialising intra-cranial pressure sensors, for example. Anybody interested should go on to our website and find out more." (www.healthyaims.org)

Healthy Aims currently has 26 EU participants. It was set up eighteen months ago to develop medical implants and accompanying low power sources.

The project has already seen successes, especially in the creation of a secondary, rechargeable, implantable battery for cochlear implants and the Functional Electrical Stimulator (FES). It was developed in conjunction with Saft Batteries and French firm CEA/Liten, which developed the charging circuit. Saft Batteries now intends to have a qualified battery to commercially exploit into medical implants.

This project has spawned another research avenue for biofuel cells, where the energy from the body or metabolic by-products are used to power various sensors and devices for medical use.



Above: Implantable battery
Left: Implantable sensor

Combating counterfeiting

- With an estimated £30 million worth of counterfeit electrical products reaching the UK annually, combating the devious 'masterminds' behind them is a serious issue. Jobs, profitability, market share, reputations – and, importantly, public safety – are at stake.
- Positive action – customs and market authorities, the WTO, exhibition organisers and brand owners must work more closely together to halt the advance of counterfeit electrical products. It is a growing problem. In some countries, counterfeit products represent 50% of the market.
- Communication – governments and manufacturers must communicate effectively the message that counterfeit electrical products are potentially dangerous and stress it is a criminal offence to trade in them.
- Vigilance – everyone in the electrical and electronic goods supply chain must ensure the authenticity of the products they buy or install. The alternative could be extremely costly to them and kill their customer.
- Enforcement – a new European Directive seeks to enforce intellectual property rights with retailers facing jail for knowingly selling counterfeit or copied goods.
- Register logo/brand – manufacturers should register their logo and brand in all markets where products might be sold/counterfeited, especially China. Country of origin and brand name should be stamped (embossing is more effective) on the products.
- Evidence – logo/brand registering ensures crucial evidence if counterfeit tooling is discovered. It can then be seized/destroyed. Products with branded adhesive labels are no deterrent – they can be copied and sent separately from the goods to the seller.
- Authenticity – products should only be purchased from an authorised supplier/distributor. If anyone doubts a product's authenticity they should immediately check with the manufacturer. If the price seems too good to be true, it's probably counterfeit.
- Responsibility – the responsibility for ensuring that only genuine quality products are used lies with all those specifying, purchasing and installing electrical equipment. How do you ensure only genuine products are installed on your project? Leaving it to others is not good enough.
- Decisive action – we urge all manufacturers affected by this illegal counterfeiting 'trade' to join with us and take group action. BEAMA Installation anti-counterfeit campaigns have seized 10+ million counterfeit products and hundreds of tools. Working together works.
- Empowerment – governments should empower whatever controls they have to be effective, before someone is killed. There are huge safety and moral issues here.

This month's Top Ten Tips were supplied by David Dossett, chief executive of BEAMA (British Electrotechnical and Allied Manufacturers' Asso.)

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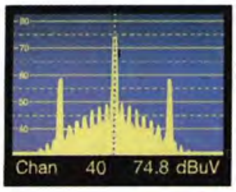

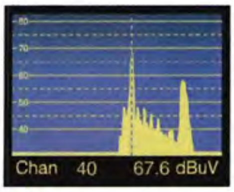

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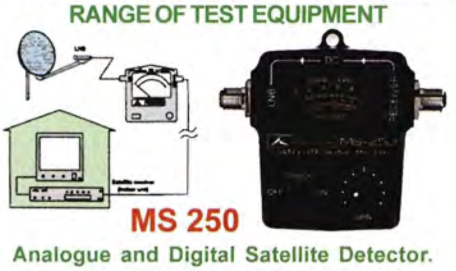

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Wireless... but where ?

Christos Papakyriacou comments on the ever increasing – and scary for some – developments in wireless technology

In the last couple of years, wireless technology has taken a huge leap forward, both in terms of mass deployment and in market acceptance. But how are all these new technologies going to benefit business?

WiMax is about to bring wireless broadband to the masses. Currently, Wi-Fi hotspots have been popping up all over the place, giving us the opportunity to access the Internet whilst eating lunch in McDonald's or having a coffee in Starbucks. A number of train companies and airlines have also hit on to the idea that business people might want to work whilst travelling, and Wi-Fi, which provides a local access via the Ethernet, enables travellers to do just that. WiMax is Wi-Fi's big brother and will provide Ethernet access to a radius of up to 30 miles. However, in reality, the signal will only cover an area of 3-5 miles.

Technology such as WiMax promises to bring so many advantages for businesses. Fixed workstations could become a thing of the past. Businesses would be able to equip their workforce with laptops, allowing employees to work anywhere in the building, helping to build stronger teams and a more cohesive workforce.

As of yet, WiMax is still at the conceptual stage, however, Intel is working on bringing the technology to the first residential community in Georgia, US. If successful, we might all be able use our laptops anywhere within a WiMax city and have all the benefits of broadband Internet, wirelessly.

Over the last year, Bluetooth has finally gained market acceptance. When it first emerged, there were numerous problems with interoperability. But now, it seems these issues have been ironed out and Bluetooth will finally make its move onto the mass market. It seems that all major players in the wireless market are currently clamouring to get on to the Bluetooth bandwagon, with Nokia and Microsoft incorporating the technology into their mobile devices.

“3G is just gaining acceptance, but it is going to be some time until the majority of the public feel confident in using it”

The last 15 years have seen wireless technology change beyond recognition. Gone are the days when people carried around mobile phones the size of bricks and struggled to receive a decent reception. The networks have become far more sophisticated and the speed of data transfer enables the streaming of live feeds.

Next year sees the launch of 4G in Japan, and with it comes data transfer rates of between 20-40Mbps. Delivering more advanced versions of the improvements offered by 3G, such as enhanced multimedia and smooth video stream. But the next problem we have to overcome is user fear. 3G is just gaining acceptance, but it is going to be some time until the majority of the public feel confident in using it.

Wireless technology is at a stage where it is so highly developed that users are scared of it. It has moved forward at such a pace that the majority of people don't understand the benefits it can bring. Rather than spend time continually developing new technologies, maybe it should be time for the industry to get back to basics and educate the public at large about wireless technology and how it can help make our lives more efficient.

Christos Papakyriacou is the Managing Director of Alpha Micro Components, an independent distributor of electronic components.

Game cons

are playing to

By Keri Allan

The Electronics Entertainment Exhibition (E3) in Los Angeles this year played host to an interesting unveiling of next generation games consoles from Sony, Microsoft and Nintendo. Approximately every five years the console market is flooded with new hardware, re-invigorating sales and improving technology. The difference this year is the power of the hardware and the complexity of the circuitry involved.

While Microsoft and Sony were happy to release specifications of their respective machines, due for launch in November and Spring 2006 respectively, Nintendo chose only to release sparse information on its, admittedly, less powerful system (also due for a Spring 2006 launch).

The first obvious point is that the console developers have departed from their previous attempts to make the console architecture similar to that of the PC. This is because they've realised there's a greater need for power for a single application rather than the PC standard of multitasking.

The second obvious point is that they've all taken different routes to getting that power for their respective games consoles. Even when Microsoft and Sony started preliminary design work on their next generation consoles by choosing a similar path, in the end, the respective outcomes were very different.

Taking a look at the specifications in **Table 1**, first impressions of the next generation hardware indicates Sony's PlayStation 3 (PS3) as a more capable machine than Microsoft's Xbox 360. However, closer inspection reveals this may not be the case.

Table 1

	XB360	PS3
CPU	3x 3.2GHz VMX 128 Vector Unit 1MB L2 Cache	1x 3.2GHz core 7x SPE 3.2GHz 7x 512kB per SPE L2 Cache
Memory	512MB of GDDR3 RAM @700MHz	256MB XDR @ 3.2GHz 256MB GDDR3 VRAM @700MHz
GPU	500MHz	550MHz
Bandwidth	22.4GB/s memory interface bus bandwidth 256GB/s memory bandwidth to EDRAM 21.6GB/s front-side bus	Main RAM 25.6GB/s VRAM 22.4GB/s RSX 20GB/s (write) + 15GB/s (read) SB 2.5GB/s (write) + 2.5GB/s (read)
FPP	1 Teraflop	2 Teraflop

Both Sony and Microsoft have adopted a multi-core, multi-threading system based on some of the latest technology and custom CPUs, in this case both designed by IBM. Patents have been filed by each company for their specific intellectual properties, to ensure that their respective machines outperform anything currently available on console, or indeed in the PC marketplace.

The PS3 system, for example, uses technology called 'The Cell', which was developed jointly by Sony, Toshiba and IBM. The architecture comprises one Power Processing Element (PPE) and eight Synergistic Processing Elements (SPE). The PPE is a custom power-processing core and is essentially a graphics-processing unit (GPU), which carries out the main control of the circuit, as well as the main game engine routines. The eight SPEs (one of which is reserved for redundancy) are digital signal processors (DSP).

Sony sees the PPE as the conductor, being used for less frequently repeated tasks and random access data access, while the PPEs are the orchestra, using data flow trends to orchestrate data execution. Each SPE has more bandwidth and power than the PPE. The interesting and most beneficial aspect of the

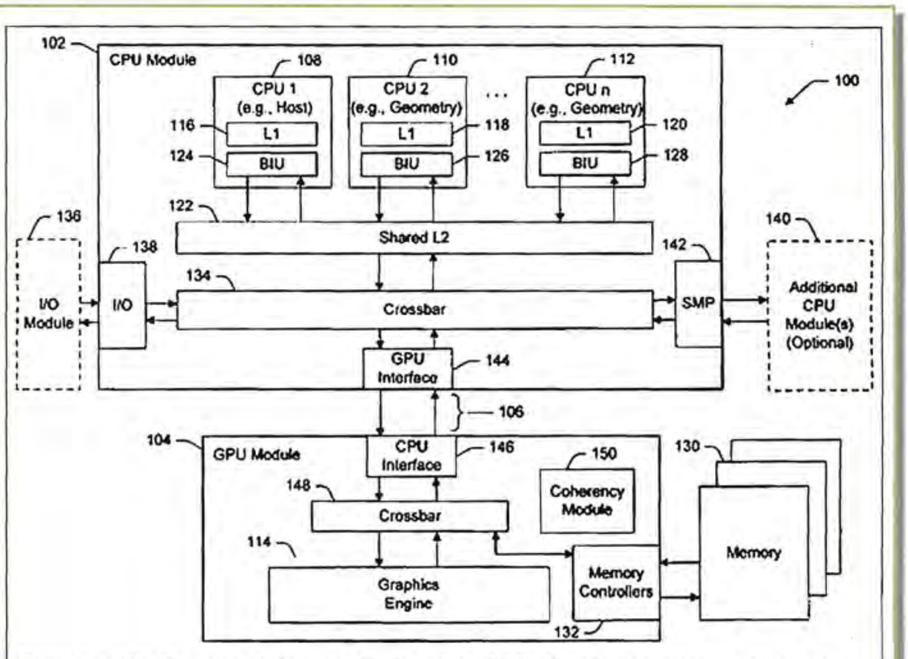
oles

Sony plans to launch the PlayStation 3 in the spring of next year

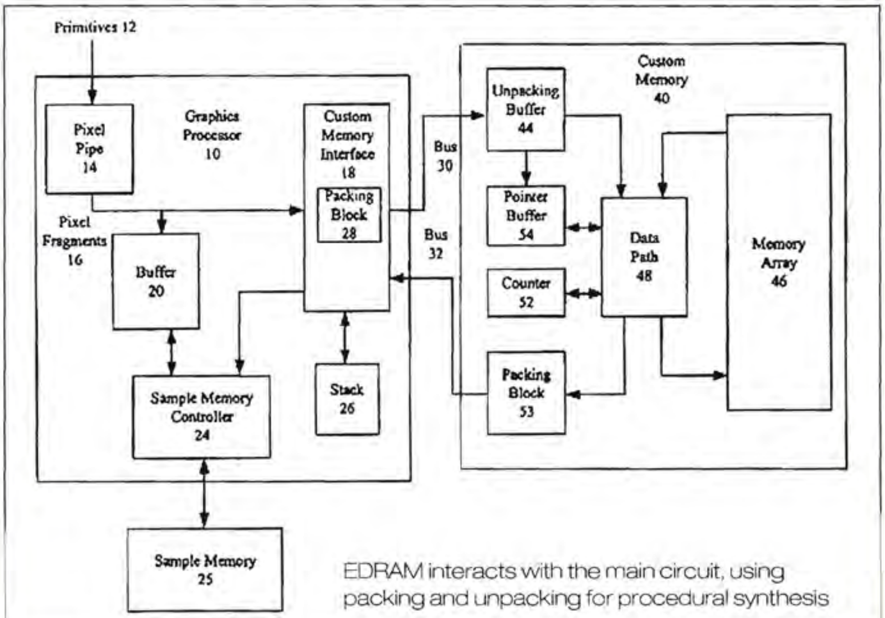
new tunes

design is the ability of each SPE to individually access the main random access memory (RAM) of the system, as well as being able to access the cache of other SPEs to handle data more efficiently.

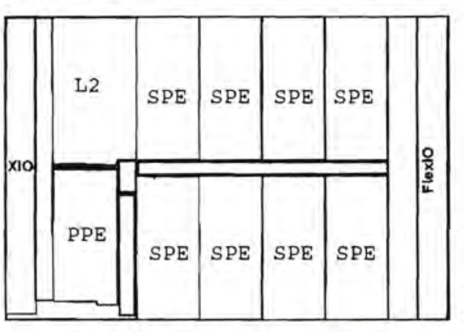
Both, the PS3 and Xbox 360, have clock speeds of 3.2GHz on each processing chip. However, it is not the speed that makes the difference; it is the amount of processing power. The Cell design is a multi-threading system and the way the SPEs achieve this is fairly straightforward. Each SPE can take in two instructions at a time, check to see if they can operate in parallel and then issue commands either in program order or in parallel. These instructions then travel down one of two pipes – 'even' or 'odd' – to be executed. After execution, they're placed back in sequence (if necessary) by the very simple commit unit and their results are written back to local memory.



Patent application circuit diagram for the Xbox 360, showing how the system uses unified architecture and procedural synthesis



EDRAM interacts with the main circuit, using packing and unpacking for procedural synthesis



Basic architecture layout of the Cell processing system, incorporating the L2 Cache, eight SPEs and one PPE

Basically a controller, the commit unit determines which routines need to be run over again, so causing less strain on system bandwidth and memory. Thus, all of the Cell's 'intensive routines' can reside on the PPE core, while the SPEs just do the work that's assigned to them. This creates ease of use for programming, but essentially, multi-threading isn't a common feature in games just yet due to the fact that hardware didn't support it previously. This is due to PCs and consoles using single core processors only. So, assigning a different thread to different SPEs and running the code simultaneously may indeed cause a problem due to developers' non-familiarity with multi-thread coding. It may take time for programmers to familiarise themselves with a multi-core hardware structure.

The PlayStation 2 (PS2) featured the 'Emotion Engine', a graphics chip designed by Sony specifically for the console. In essence, this is a general purpose graphics processor equivalent to the graphics cards found in PCs of the time. The Emotion Engine also had powerful vector processing units, making it very difficult to programme because of the inability to programme directly to the processors in anything but Assembler. On the new hardware however, that has been addressed with the addition of widespread Application Programming Interfaces (API) and each SPE/PPE programmable in C/C++, each having built-in compiler intrinsics, enabling Single Instruction, Multiple Data-stream (SIMD) access. Also, Open GL ES software has been utilised, rather than Open GL, due to the smaller memory footprint along with its focus on 3D applications, making it more suitable for games programming. Furthermore, rather than using shader technology supported in most PC-orientated games, which is a way to individually control effects and mapping onto individual pixels or environments, Sony has chosen CG Shader in conjunction with Nvidia, predominantly due to Nvidia designing the GPU being used in the PS3.

Whilst with the Xbox 360, Microsoft started work on the follow-up to its original console in 2002. After listening to developers and analysing technology that might be available in 2005, it designed the prototype Xbox 360 to run without a hard drive and only 256MB of RAM. Once the final design of the system itself was realised, it only made sense to increase the RAM to 512MB, in line with Sony and Nintendo's offerings.

The Xbox 360 is a three core system, with each core based around a custom-built power PC CPU, designed by IBM. Each core runs at the same frequency as the Cell, but is a more general purpose processor. Although Sony may indeed claim to have twice the floating point performance of the Xbox 360, only 10% of videogame code is floating point calculations. Some 80-90% of code focuses on the geometry and main engine code, meaning that developers will find the transition to Xbox 360 a lot easier to manage. That said, Microsoft's machine does things very differently, with a patent filed for a term called 'Procedural Synthesis'.

The Xbox 360 stores high-level descriptions of objects in main memory and has the CPU procedurally generate the geometry (i.e. the vertex data) of the objects on the fly. Imaging a forest, main memory stores information about the trees, such as type, size, location of leaves etc, along with other relevant data, like the direction of the prevailing wind. This information is passed into the Xbox 360's CPU, where the vertex data that defines the polygons out of which the tree is made, are generated by one or more running threads. These threads then feed that vertex data directly into the GPU. The GPU then takes that vertex information and renders the trees normally, just as if it had gotten that information from main memory.

This is a change from before, when artists had to pass high level geometry data directly to the GPU, taking up valuable GPU or system memory and only allowing a small number of individualised geometric shapes. As in the example above, the forest previously could be made from individual trees, but it would depend on the memory of a system and how much of the GPU's resources were used.

While this doesn't appear anything more than ordinary, the same amount of data used in today's games can create a much wider variety of animations and environments.

The end result is that the amount of data stored in main memory and moved into the CPU is much less than the amount of data that the CPU puts out and that the GPU ends up processing. Microsoft refers to this ratio of stored scene data to rendered vertex data as a 'compression ratio', the idea being that

PlayStation 3 with controller

Microsoft's Xbox 360

main memory stores a 'compressed' version of the scene, while the GPU renders a 'decompressed' version of the scene.

The technique of compressing scene data for storage in main memory and then decompressing it by means of procedural synthesis allows game developers to do more with a console's limited system memory. They haven't reduced system memory, but are using it more efficiently. The console provides plenty of CPU-to-GPU bandwidth and enough computing power to procedurally render objects in real time. In addition, the developer provides higher-level scene descriptions that allow a richer, more realistic world to be described using less storage space.

The Xbox 360 can also use the CPU to tessellate curves in real-time. The higher order curves can be stored in compact form in main memory and then transferred to the CPU where they're tessellated into vertex data. As with the procedural geometry generation described above, this dynamically generated vertex data is then passed directly to the GPU for rendering.

Real-time tessellation has a few advantages. First, storing models as collections of higher order curves is more compact than storing them as vertex lists. This is especially true for high-polygon-count models, where the higher number of polygons approximates the original curves better, but also makes for more vertex data. So real-time tessellation is another form of data compression that lets developers use a limited amount of source data, main memory and bus bandwidth to render a highly detailed, data-intensive scene.

The second upside to dynamic tessellation is that a model that is tessellated in real-time can be rendered using a variable number of polygons depending on the demands of the particular scene that's rendering. This allows the software to control the level of detail (LOD) of each model dynamically.

Dynamic LOD, which has appeared in various forms of 3D games for some time, is useful for keeping the total number of polygons in a scene under control. Objects that are far away from the viewer can be rendered with a low LOD (i.e. with fewer polygons), while objects that are closer can be rendered with a higher LOD.

While more information on each console will be released as time passes, each system will try to create a new way to process, store and use data more efficiently. While the PlayStation 3 outperforms the Xbox 360 on floating point operations, the Xbox 360 has a much more powerful GPU, as well as game-specific uses for its triple core system. However, it must be noted that although hardware's role is important, without custom, exclusive, software libraries designed to take advantage of each system, none will gain a distinct advantage in today's console marketplace.

Do we ha

Can low levels of ElectroMagnetic Field (E
Alasdair Philips, Director of consultancy Power

Bioelectromagnetics research is now seriously challenging conventional wisdom in biology, the physical sciences and engineering. Since the first reports of physiological responses to low levels of EMF exposure appeared over 35 years ago, there has been an ongoing fierce and dismissive opposition from scientists holding orthodox views and from industries fearing "unreasonable" restrictions being placed on their activities.

If we are ever to understand the complex way that electric and magnetic fields interact with living beings, we need to know what to measure. It is interesting to note that the EMC susceptibility regulations for equipment mainly specify frequency, electric and magnetic signal strengths and not power densities. For RF susceptibility, equipment has to be tested at 3 Volts/metre (V/m) (10V/m for life critical systems) at mobile phone frequencies, whereas we allow humans to be exposed to over 60V/m. Are we really that less susceptible to interference?

If your house isn't close to a radio transmitter (e.g. mobile phone base station) then an easy experiment to try is to turn off all the house electricity supply at the main switch. It is surprising how many people report feeling, after 10 to 30 minutes, that a "pressure" has lifted when all the power is off.

There's a growing belief that the modulated 'electro-smog' that we are increasingly submerged in is having a profound effect on the lives of many people. The wellbeing of some people is already been affected and ailments range from headaches through chronic fatigue to cancer. However, despite living in "the information age", the official view of the interactions of EMFs with people is still based on a model that equates us to a dead slab of meat with a built-in cooling system (the circulating blood) exposed to a continuous wave (CW) signal. The latest bioelectromagnetics research shows this is incorrect (see References). Even the old ionising/non-ionising argument is flawed when considering living beings. The argument is based on the energy to break a covalent or ionic bond, yet almost all the forces at work when DNA replicates or is repaired are about 100 times weaker – hydrogen bonds, Van der Waals and hydrophobic forces.

Challenging conventional wisdom

It is often stated that there is "no known mechanism" whereby cells could detect and demodulate electromagnetic signals. In fact, conventional standard science cannot yet explain human and animal sensitivities to light, sound, taste or smell. For example, the auditory threshold of a healthy young person with good hearing involves a hair cell vibration of 10-11 meters, or about the diameter of a single hydrogen atom. The ear suppresses the vastly larger noise of its thermal atomic and molecular collisions by an as yet unknown mechanism, functioning as an almost perfect amplifier close to 0°K.

Excitation in biological systems has been traditionally thought of in terms of equilibrium thermodynamics. This assumes that the potential effectiveness of an exciting agent could be assessed by its ability to transfer energy to the receptor in excess of its random thermal atomic and molecular collisions. Thus, the Boltzmann expression (kT) has been regarded as setting an immutable threshold below which an exciting agent would not be physiologically effective. Low-frequency magnetic fields, now proven to be able to act as effective physiological stimuli, would also fall below this thermal barrier. The complexity of living biological organisms demands our careful consideration and we are still a long way from knowing what "life energies" really are. From a scientific viewpoint, answers need to be sought in non-equilibrium thermodynamics and in multi-cellular cooperative states, as suggested by Herbert Fröhlich [1].

The genome is like a recipe book that can both photocopy and read itself. It unwinds and winds up again using very weak electromagnetic forces. It is transcribed into messenger RNA and then converted into strings of amino acids that fold up into proteins. Conformational changes in protein folding is one of the repeatedly reported effects of EMF exposure. Almost everything in our bodies is either made of proteins or by proteins. Every protein is a translated gene. Both single- and double-strand DNA breaks have been shown to become more common when living cells are exposed to quite low levels of man-made, time-varying EMFs.

e an EMF problem?

exposure affect human and animal health?
h, brings together some of the latest developments

The Reflex

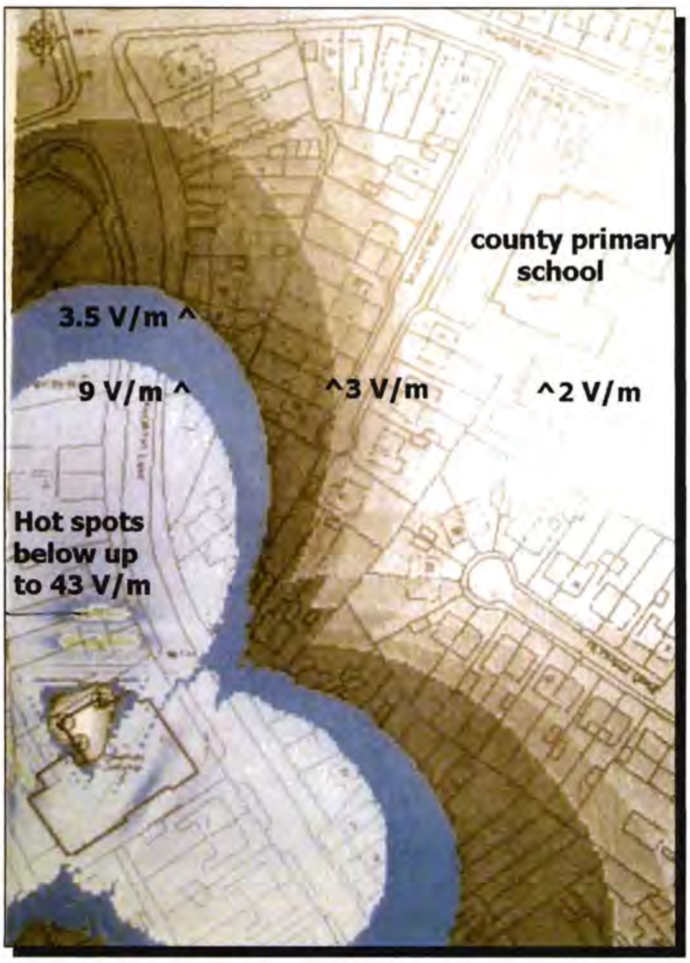
The recently published REFLEX project report [2] has made a substantial contribution to known biological effects of EMFs on in-vitro cellular systems. Twelve institutes in seven countries found genotoxic effects and modified expressions on numerous genes and proteins after low level exposure of living cells in-vitro to EMFs well below current international safety guidance. Gene mutations, deregulated cell proliferation and suppressed or exaggerated programmed cell death (apoptosis) that are caused by, or result in, altered gene and protein expression are such critical effects. They found that genotoxic effects and a modified expression of numerous genes and proteins after EMF exposure could be demonstrated with great certainty, while effects on cell proliferation, differentiation and apoptosis were much less conclusive.

Since all these observations were made using in-vitro studies, the results neither preclude nor confirm a health risk due to EMF exposure, but they support such a possibility. The study concluded that in-vitro damage due to low-level EMF exposure is real and that it is important to carry out much more research, especially monitoring the long-term health of people.

International guidance levels vary

Current UK maximum Public Exposure Levels (PEL) for 50Hz are set at 100 microtesla (mT) and 5000V/m. However, there have been many calls for a much more precautionary stance. Switzerland currently requires a PEL of no more that 1mT for new installations. Some regions of Italy set guide levels around 0.4mT and 500V/m. Some large multinational companies, including the World Bank, have been setting design guides for buildings at about 0.25mT and 100V/m for about the last ten years. One industry source stated that it had over 10 international clients in the late 1990s lone that wanted low EMF environments to be designed in their new buildings.

Professor Michael Kundi of the University of Vienna recently compared the EMF regulation setting process with that used by the World Health Organisation (WHO) for controlling air pollution [3]. He derived a maximum magnetic flux guidance level of 0.21mT. With good electrical design of wiring and appliances, there is no reason why this should not be universally achievable at little cost, apart from near to high-power lines and some electrical appliances.



From operator 3's own documentation supplied to residents. They come close to ICNIRP levels in places (61V/m approx at 2.1GHz)

The average 50Hz UK background magnetic flux level in houses is about 0.04mT and about double this in flats. The two main causes are (i) local electricity distribution system wiring and (ii) "ring" circuits within buildings. Common supply practice in the UK is to: (a) connect electricity substations in parallel, so that circuits share load and connectivity problems, and this leads to fewer customer complaints and (b) Protective Multiple Earthing (PME) is used; this connects Neutral to physical Ground/Earth every few hundred metres. Both these practices lead to stray "net-error" currents, where outgoing current takes a different return route and this causes elevated magnetic fields over extensive areas from what effectively becomes a large single-turn transformer loop. Ring circuits are a problem, especially as they age and new sockets are added, etc. Any imbalance in loop impedances will result in an imbalance in current flows. 0.01-0.1W is just as bad as 0.1-1W in causing the 'single-turn transformer effect'.

Power frequency electric fields in buildings using earthed metal conduit are effectively zero, but this was abandoned years ago for houses. Lighting circuits are now the worst offender for generating high electric fields. Modern practice is looping line (230V) around all lighting fittings and then taking this to and from the switch results in a live spiders web – with 230V on most cables even with all the lights switched off. This capacitively couples with wall and ceilings and causes typical E-field levels between 15 and 100V/m within the room.

Recent microwave and health reports

In September 2004, ICNIRP issued an epidemiology overview [4] that ignored most of the most relevant recent reports of ill health related to microwave exposure. In January 2005, the UK National Radiological Protection Board (NRPB) issued an update [5] of the original Stewart Report (2000) [6]. This expresses concern about a number of aspects of microwave emissions with regard to health [7].

An Israeli study [8] found a 7-fold increase in cancers in a population living within 350 metres of a small mobile phone base station, compared to a similar population away from the mast. A report by German doctors on a group of 1000 patients in the town of Naila showed a 3-fold increase risk of cancer in those living within 400m of a base station when compared to people living further away [9]. These are disturbing findings.

A 2004 paper reporting ill health in Spain near to a base station showed a 59-fold increase in depression, a 40-fold increase in fatigue and a 20-fold increase in concentration problems in people living in measured GSM field strengths between 0.25-1.3V/m when compared with people living in field strengths below 0.05V/m [10].

In December 2004, Microwave News brought out a special issue [11] on EMF and health setting out a wealth of evidence to justify more precautionary exposure policies.

Recent initiatives

It is now increasingly being recognised that, at power supply frequencies, there is enough evidence of possible harm to start to actively reduce public exposure on the ALARA (As Low As Reasonably Achievable) principle. In the UK there is now an advisory working group that has been established under the secretariat of the UK Department of Health and with the support of the Health Minister, that brings together the main stakeholders – industry, academics, government and others – to discuss ways of reducing the public's exposure to power frequency electric and magnetic fields. This includes all sources: high-voltage overhead transmission lines, electricity substations, railways, distribution and building wiring and appliances.

Hopefully, the same will happen for mobile phone signals.

Essex: Mobile phone base stations with houses in the background

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Analogue CMOS, low-voltage, current-mode implementation of digital logic gates

Muhammad Taher Abuelma'atti and **Munir Ahmad Al-Absi** from the King Fahd University of Petroleum and Minerals, Saudi Arabia present a new approach for implementing basic logic functions using analogue current-mode techniques

Mixed analogue/digital electronic circuits are becoming increasingly important. Digital electronic circuits are mostly designed in CMOS technology. To be able to integrate the digital and analogue parts on to one chip, high performance analogue CMOS circuits are required and a large number of mixed analogue/digital VLSI integrated circuits realised in state-of-the-art digital CMOS technologies are now available.

In reality, the emergence of ICs incorporating mixed analogue and digital functions on a single chip has led to an advanced level of analogue design. Of particular interest here is the current-mode approach for designing analogue ICs. It is well known that current-mode analogue signal processing offers some important speed advantages over the traditional voltage-mode signal processing.

At present, current-mode implementations are available for a wide range of analogue electronic circuits including A/D and D/A converters, continuous time filters, neural-networks, sampled data filters and microwave and optical systems. This raises the following question: Can digital ICs be realised using current-mode analogue techniques? Analogue-based realisations of digital logic circuits may result in avoiding the traditional problems of fan-in and fan-out, inherent in digital implementations, less complexity, low-voltage as well as higher speed of operation.

In an attempt to answer this question, the translinear principle has been used to realise a digital inverter circuit, a bistable element and NOT/OR/NAND/XOR functions. All of these realisations use bipolar technology. No attempt has been made to use CMOS technology in designing digital circuits using analogue techniques. This paper is an attempt to present such a realisation.

Power series representation of logic functions

Using their truth tables, it is easy to show that the input-output relations of the basic digital logic functions can be expressed as:

$$z=1-x \qquad (1)$$

for the NOT operation,

$$z=1*x \qquad (2)$$

for the AND operation,

$$z=x+y-x*y \qquad (3)$$

for the OR operation, and

$$z=x+y-2x*y \qquad (4)$$

for the XOR operation. In Equations 1 to 4 the signs +, - and * carry their normal mathematical meanings, that is add, subtract and multiply, respectively. Using Equations 2 to 4 in combination with Equation 1, the digital logic functions NAND, NOR and XNOR can be realised.

Analogue implementation of the basic logic functions in Equations 1 to 4 requires analogue multipliers, inverters and summers. Using a modified version of the four-quadrant multiplier, voltage mode analogue implementation of two-input AND, NOT and OR functions have been reported. However, these implementations have been built around voltage-mode operational amplifiers and analogue switches, use a large number of resistors and require relatively large supply voltages. This paper presents alternative current-mode analogue implementation of the digital logic functions. Using no resistors (except for realising constant current-sources), switches or operational amplifiers, and only a small number of transistors, the proposed implementation requires low supply voltages and is attractive for integration. The proposed implementation is designed for CMOS technology, which is now the most preferable technology for integrated circuit fabrication.

The proposed circuit

Figure 1 shows a block diagram for the possible implementation of Equations 1 to 4. It appears from Figure 1 that the analogue current-mode implementation of the logic functions INV/OR/AND/XOR requires current multiplication, addition and subtraction. In current-mode operation, addition and subtraction can be easily obtained by joining the current-carrying wires. While many current-multipliers are available in the literature, here we propose to use the current-multiplier circuit shown in **Figure 2**. Transistors M_1 - M_4 form a traditional

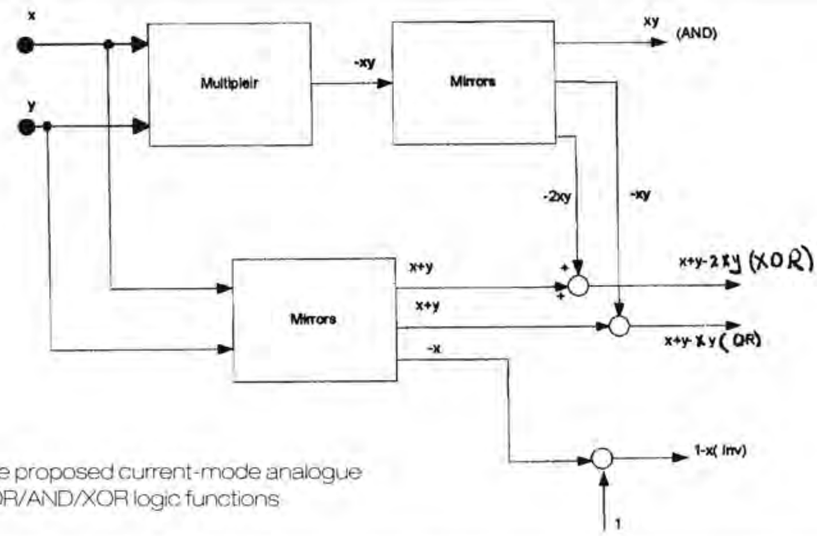
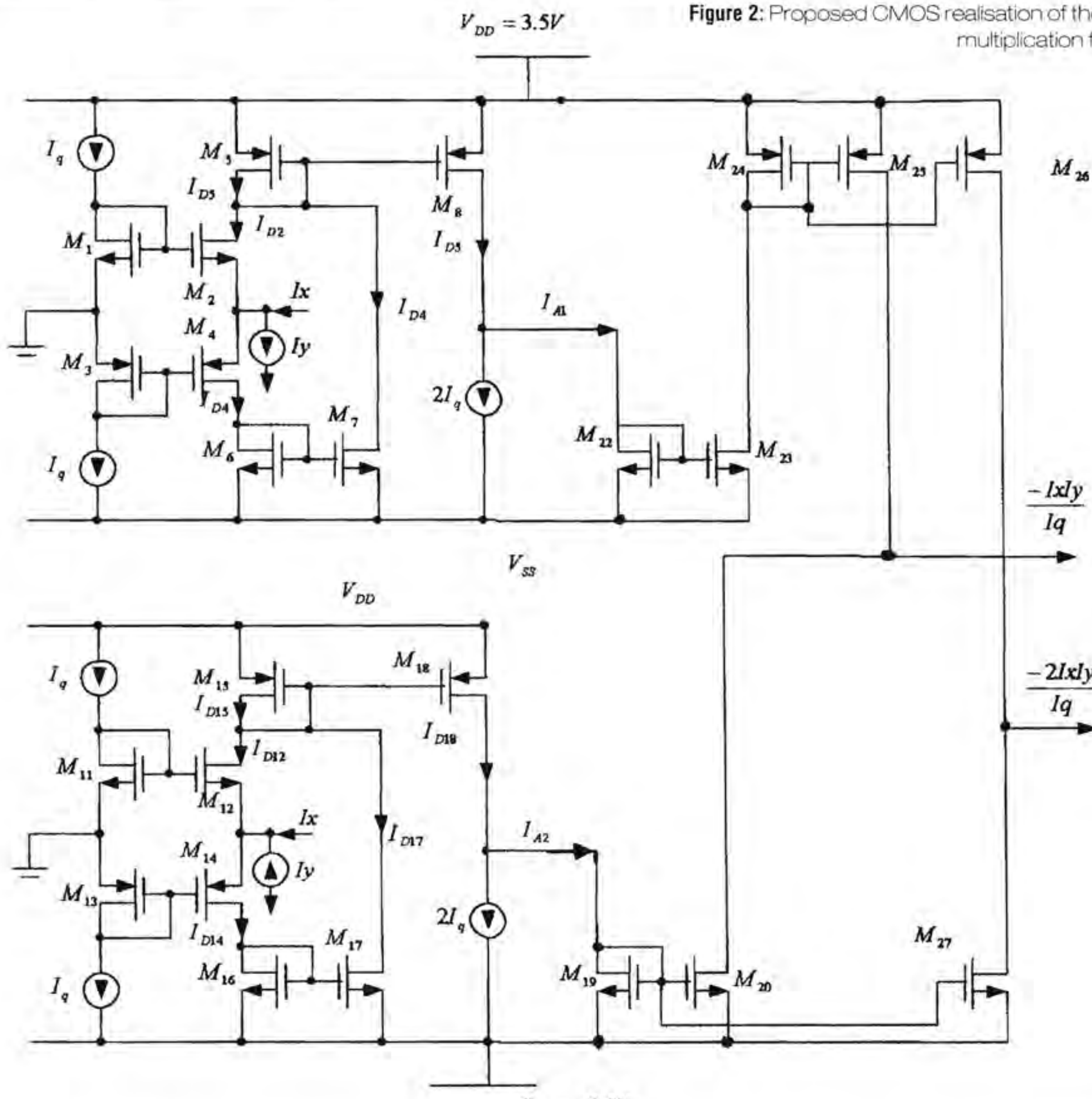


Figure 1: Block diagram of the proposed current-mode analogue implementation of the INV/OR/AND/XOR logic functions

Figure 2: Proposed CMOS realisation of the current multiplication functions



class-AB current mirror. Assuming that transistors M_1 and M_2, as well as transistors M_3 and M_4, are well matched and that all transistors are operating in their saturation region and having the same value of the transconductance parameter, that is $\beta_n=\beta_p$, then applying the translinear principle, we obtain

$$2\sqrt{I_q} = \sqrt{I_{D2}} + \sqrt{I_{D4}} \quad (5)$$

Combining Equation 5 with $I_{D2}+(I_x-I_y)=I_{D4}$ (6) and using simple mathematical manipulations, the currents and can be expressed as

$$\frac{I_{D2}}{I_q} = 1 - \frac{1}{2}\frac{(I_x - I_y)}{I_q} + \left(\frac{I_x - I_y}{I_q}\right)^2 \quad (7)$$

and

$$\frac{I_{D4}}{I_q} = 1 + \frac{1}{2}\frac{(I_x - I_y)}{I_q} + \left(\frac{I_x - I_y}{I_q}\right)^2 \quad (8)$$

From Equations 7 and 8 we get

$$\frac{I_{D5}}{I_q} = \frac{I_{D2} + I_{D4}}{I_q} = 2 + \frac{1}{8}\left(\frac{I_x - I_y}{I_q}\right)^2 \quad (9)$$

By subtracting a constant current = 2 Iq from I_{D5}, the current I_{A1} can be expressed as

$$\frac{I_{D2}}{I_q} = 1 - \frac{1}{2}\frac{(I_x - I_y)}{I_q} + \left(\frac{I_x - I_y}{I_q}\right)^2 \quad (10a)$$

Following the same procedure, assuming that transistors M_{11} and M_{12}, as well as transistors M_{13} and M_{14}, are well matched and that all transistors are operating in their saturation region and having the same value of the transconductance parameter, that is $\beta_n = \beta_p$, the current I_{A2} can be expressed as

$$\frac{I_{A2}}{I_q} = \frac{1}{8}\left(\frac{I_x + I_y}{I_q}\right)^2 \quad (10b)$$

Using current mirrors with transistors having appropriate aspect ratios, the current I_C can be expressed as

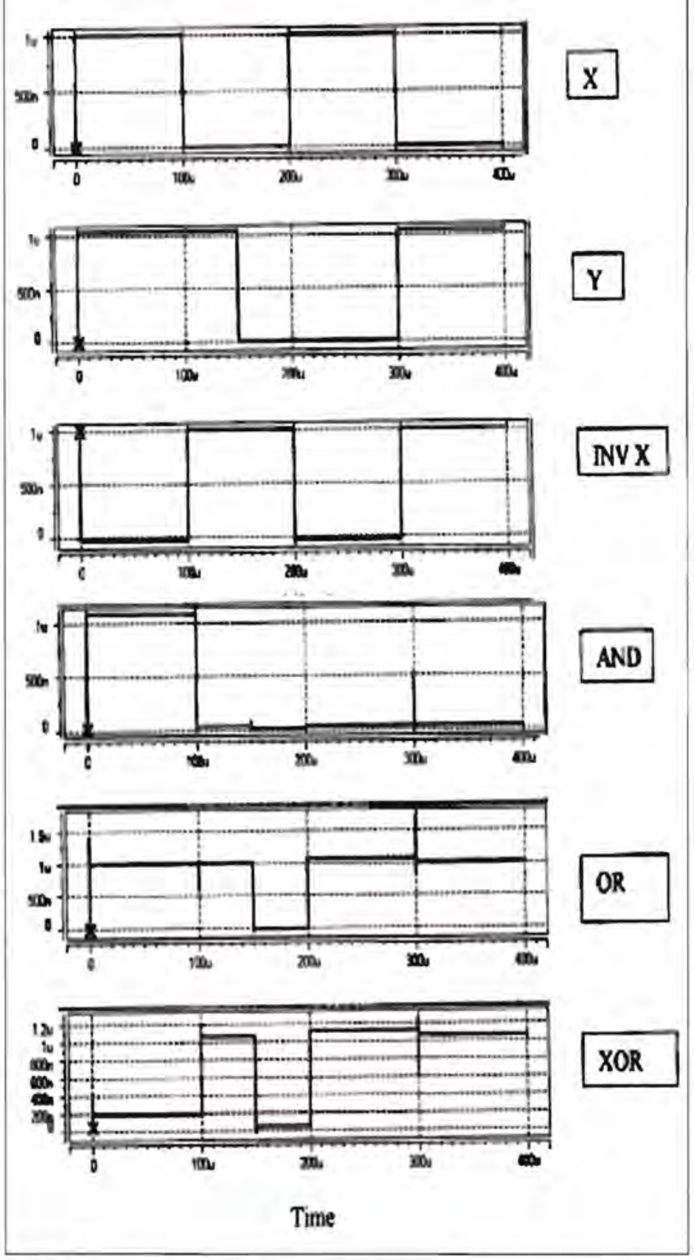


Figure 3: Results obtained from the proposed implementation of Figure 1 with DC supply voltage of ±3.5V

$$I_C = -\frac{I_x I_y}{I_q} \quad (11)$$

Thus, a multiplier circuit can be realised. Current mirroring, using transistors with appropriate aspect ratios, yields the currents

$$I_{out1} = \frac{1}{I_q} I_x I_y \qquad (12)$$

and

$$I_{out2} = \frac{2}{I_q} I_x I_y \qquad (13)$$

Using Equations 12 and 13, it is easy to verify that the output currents I_{NOT}, I_{OR}, I_{NAND} and I_{XOR} realise the logic functions NOT, OR, NAND and XOR given by Equations 1 to 4. Realisation of the logic functions NOR, AND and XNOR is a straightforward extension of the implementations of Figure 1.

Simulation results

The proposed implementation of Figure 1 was simulated using the HSPICE level 49 simulator and the transistors were modeled using BSIM3v3 model of AMS 0.8μm process technology, with supply voltage $V_{DD} = -V_{SS} = 3.5V$. The results obtained from the NOT, OR, NAND and XOR operations are shown in **Figure 3**, where the currents are sensed using load 1kΩ resistances. From Figure 3, it appears that, the results obtained are in excellent agreement with the theory presented in the Equations 1 to 13.

This shows that, starting from the truth tables of logic functions, it is possible to obtain power series expansions of the basic logic functions and it is possible to implement the basic logic functions using analogue current-mode techniques. Not only that the proposed circuit can be easily extended to realise the functions NOR, AND and XNOR, an extension of it to realise basic logic functions with number of inputs greater than two is also possible and straightforward.

It is expected that using this approach for implementing more sophisticated logic circuits, for example encoders/decoders, will result in simpler and faster realisations. Finally, by realising analogue and digital circuits using the same basic building blocks, it is expected that simple design procedures for mixed analogue/digital circuits and systems may emerge.

Insight into the gain-bandwidth product of amplifiers

By K Hayatleh, B L Hart and F J Lidgey

The gain-bandwidth product (GBP) of a conventional op-amp is a constant, or so we are led to believe. But does this mean that an inverting op-amp setup to attenuate with a voltage gain of 1/10 (-20dB) will operate successfully up to a frequency of ten times the op-amp's GBP? This seems unlikely and, indeed, it is not true.

Another puzzle is why is it that the bandwidth of an op-amp unity-gain inverter stage is only one-half that of the same op-amp connected to operate as a unity-gain non-inverting amplifier, i.e. a voltage-follower?

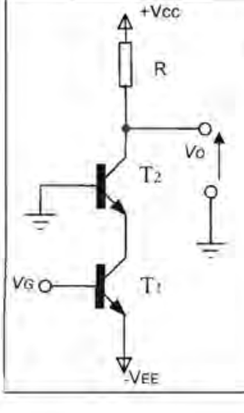
To answer these conundrums we must delve into the subtleties of the GBP. In seeking to obtain insight into GBP, we will need to analyse some amplifier circuits but we do so without resorting to advanced mathematics. With this objective in mind, an analysis employing phasor diagrams is used. These show, at a glance, the relative phases and magnitudes of signal currents and voltages in a circuit. All that needs to be recalled is that for sinusoidal signals the magnitude of the impedance of a capacitor, C, at a radian frequency, $\omega = 2\pi f$, is $1/\omega C$ and that capacitor current leads capacitor voltage by a phase angle of 90°.

Following a review of reasons for the existence of GBP constancy with a single-stage amplifier, there is a discussion of its relevance in voltage-feedback op-amp configurations and an explanation of the non-applicability of GBP constancy to current-feedback op-amps.

Single-stage voltage amplifier

Consider the cascode amplifier of **Figure 1a**, in which V_G is a sinusoidal input signal of angular frequency and rms amplitude V_G. V_o is the output signal. The voltage gain of T1 is close to unity and the only high impedance node is at the collector of T2. A simple small-signal model the amplifier can now be drawn (see **Figure 1b**). In this equivalent circuit $g_m(= 40mS/mA)$, the trans-conductance of T1 is proportional to the d.c. collector current; $\alpha(\approx 1)$ is the current gain of T2; C is the sum of the collector-base capacitance, C_{bc}, and the collector-earth stray capacitance, C_S, of T2. A phasor representation of the currents I_R, I_C in R and, C respectively, is shown in **Figure 2a**. $I_R = V_o/R$, represented by line OP, is in phase with V_o, which is taken here as the reference phasor. Since the current in C leads V_o by 90°, I_C is shown by the line PQ drawn perpendicular to I_R, and of magnitude of $V_o/_{(1/\omega C)}$, i.e $\omega C V_o$.

Figure 1a: A cascode amplifier and **Figure 1b (below)** its small signal equivalent circuit



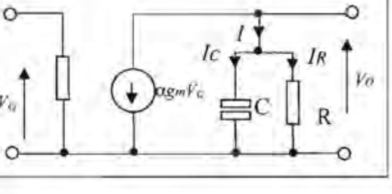


Figure 2a: A phasor plot for Figure 1b

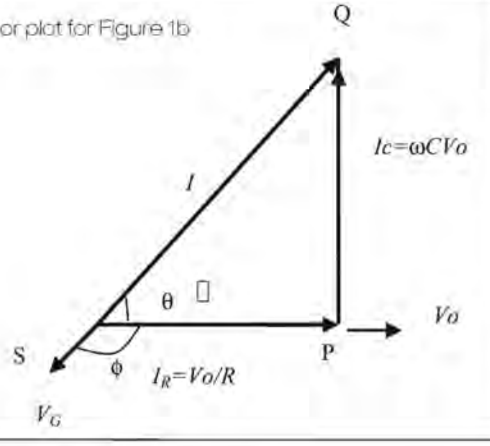
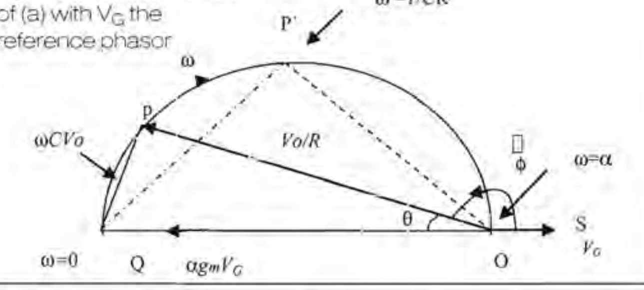


Figure 2b: Another version of (a) with V_G the reference phasor



The rule for the combination of phasors is the same as that in mechanics for the combination of differently directed forces. The line OQ represents $I = -g_m\alpha V_G$: as g_m and α are positive quantities the sign indicates for V_G a phasor OS oppositely directed to I. Using Pythagoras's theorem,

$$\left(V_o/_R\right)^2 + (\omega C V_o)^2 = (\alpha g_m V_G)^2 \tag{1}$$

and, hence, the small-signal voltage gain, $G(\omega)$ is given by

$$|G(\omega)| = \left|\frac{V_o}{V_G}\right| = \alpha g_m R \Big/ \sqrt{1 + (\omega CR)^2} \tag{2}$$

Also, V_o leads V_G by ϕ, since phase is reckoned in the anti-clockwise direction.

Rotating Figure 2a in an anti-clockwise sense, so that V_G is our new reference phasor, gives **Figure 2b**.

If V_G remains constant as ω varies then OQ is fixed, in length, but OPQ is a right angle, hence the locus of point P as ω varies

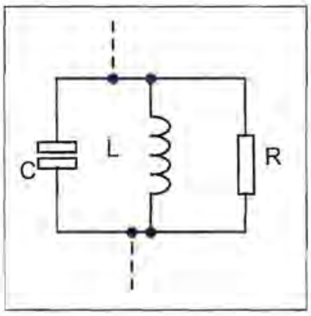
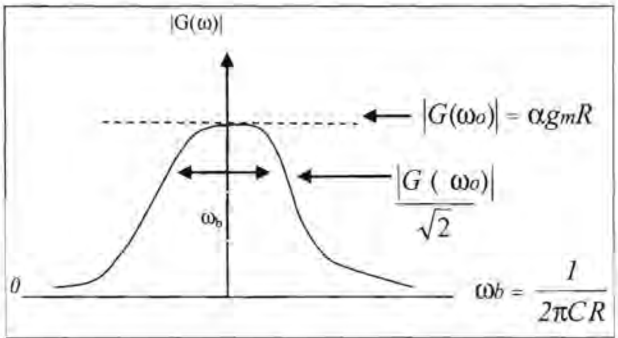


Figure 3a (Left): A tuned-circuit load, instead of R by itself

Figure 3b (Below): Showing the frequency-dependent voltage gain for (a)



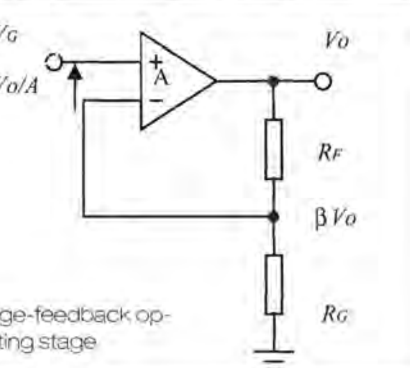


Figure 4: A voltage-feedback op-amp non-inverting stage

from O to ∞ is given by a semicircle constructed on diameter *OQ*.

From Equation 2, for $\omega \to 0$,

$$|G(o)| = \alpha g_m R \qquad (3)$$

Also, from Equation 2, $|G(\omega)|$ falls to $|G(0)|/\sqrt{2}$ for $\omega = \omega b$, where $\omega bCR = 1$ corresponding to point P'
or,

$$fb = \frac{1}{2\pi RC} \qquad (4)$$

By definition, the cut-off frequency defines the -3dB bandwidth for voltage gain.
At fb, $\theta = 45^o$, so $\phi = 135^o$
Combining Equations 3 and 4,

$$GBP = |G(o)| \times fb = \frac{\alpha g_m}{2\pi C} \qquad (5)$$

This means that GBP is constant because $|G(0)|$ is proportional to R and the frequency function determining fb has R in its denominator, and so GBP is independent of R.

Historical note

Before the advent of transistors, the figure of merit g_m/C was often used as a criterion for the selection of pentode valves in video amplifier design. In that case, C referred to inter-electrode capacitance and g_m the mutual conductance of the valve.

With respect to bipolar transistors, all types working at a specified temperature and collector current, in the low milliampere range, have effectively the same g_m, but C_{bc} is smaller for high frequency devices, which have smaller junction areas.

In this discussion, so far, the frequency response of the transistors has been ignored in the calculation of f_b. This is justified because the characteristic, or transition frequency, which even for run-of-the-mill devices is likely to be 500MHz or above. For a discrete device design in which R=5kΩ and C=2pF Equation 5 gives $f_b \approx$ 16MHz which is negligible compared to 500MHz.

In circuit theory terms, the load circuit produces a dominant pole, corresponding to $f_b \approx$16MHz, in the system response.

In concluding this review of the single-stage amplifier, it is noteworthy that the constancy of GBP also applies to the simple tuned amplifier which results when R is replaced by the parallel RLC circuit of **Figure 3a**; the response for this is shown in **Figure 3b.**

A voltage op-amp non-inverting stage

Consider the op-amp non-inverting stage of **Figure 4**. Subject to the usual op-amp assumptions we can write, by inspection,

$$Vo\left[\beta + \left(\frac{1}{A}\right)\right] = V_G \qquad (6a)$$

Where $\beta = R_G/(R_F+R_G)$ is the feedback factor and A is the open-loop gain of the op-amp.

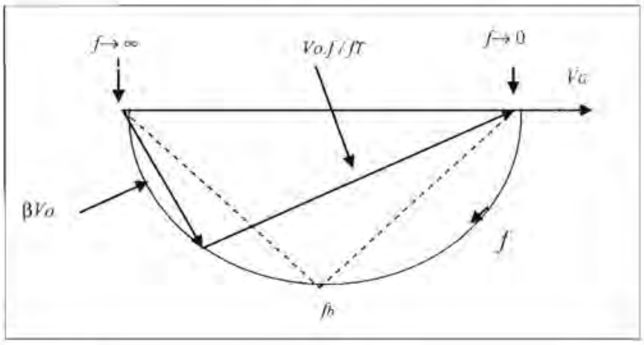
Equation 6a can be rearranged to give an expression for the voltage gain G that is used in later discussion, or

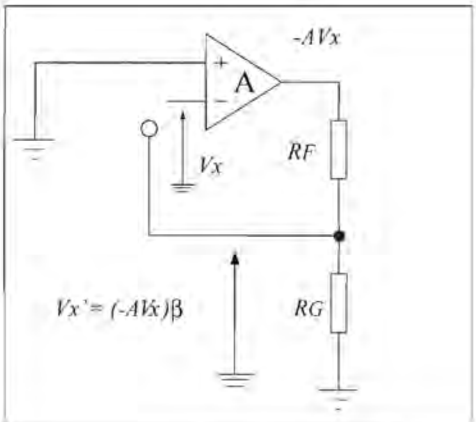
$$G = \left(\frac{Vo}{V_G}\right) = \left(\frac{\frac{1}{\beta}}{\left[1 + \left(\frac{1}{A\beta}\right)\right]}\right) \qquad (6b)$$

For low frequencies well below the cut-off frequency, fo, of the open-loop op-amp, that is $f << fo$, then A is given by $A = A0 >> 1$, so $|G(0)| \cong (1/\beta)$

$$A = A_0 >> 1, \text{ so } |G(o)| \cong \left(\frac{1}{\beta}\right)$$

From the data sheet characteristics of commonly used op-amps it is evident that, for $f >> fo$,





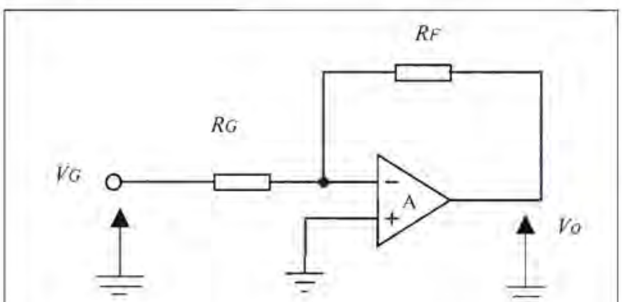


Figure 5 (Top): Phasor diagram for Figure 4 (for $A_O >> 1/\beta$)
Figure 6 (Middle): The loop gain for Figure 4 is $\left(\frac{Vx'}{Vx}\right)$
Figure 7 (Bottom): A voltage-feedback inverting amplifier

$$A = \left(\frac{A_0 f_O}{f} \right) \angle -90^0 \tag{7}$$

$|A| = 1$ when $f = f_T$, say, so $f_T = A_O f_O \approx 1MHz$ for the 741 op-amp
Hence,

$$\frac{Vo}{A} = Vo\,\frac{f}{f_T} \angle 90^0 \tag{8}$$

A phasor plot for Equation 6a using Equation 8, constructed in a *similar manner* to that in Figure 2b, is shown in **Figure 5**. The cut-off frequency f_b, as previously, occurs at the mid-point of the semicircle, so $\beta V_0 = V_0 f_b / f_T$. (Note that the semicircle is now below the horizontal axis because we are dealing with a non-inverting amplifier).

Consequently,

$$f_b * \left(\frac{1}{\beta} \right) = f_b * |G(o)| = f_T = \text{constant} \tag{9}$$

The GBP is constant for a reason similar to that for a simple amplifier. In this case, $|G(0)|$ is dependent on a resistor ratio and the same resistor-ratio occurs in the denominator of the frequency function determining f_b.

This can also be seen by examination of Equation 6b: the frequency variation of the closed loop gain is dependent on $1/A\beta$. Now $-A\beta$ is the voltage loop-gain for the circuit as in **Figure 4**. It is a property of the loop alone and not related to the input signal, so it applies to the inverting amplifier configuration of **Figure 7** as well as Figure 4. It is determined by cutting the loop at some convenient point, inserting a test signal, Vx' , and finding the signal, Vx', occurring at the other side of the cut: loop gain = Vx'/Vx (see **Figure 6**). Thus, for the non-inverting op-amp configuration, the GBP is constant because the loop-gain is proportional to β and the closed-loop gain is inversely proportional to β. At $f = f_b$ the magnitude of the voltage loop-gain is unity.

A voltage op-amp inverting amplifier

For the inverting amplifier stage in Figure 7, the well-known and easily derived expression for $G = (Vo/V_G)$ is

$$G = -\frac{\left(\frac{R_F}{R_G} \right)}{\left[1 + \left(\frac{1}{A\beta} \right) \right]} \tag{10}$$

It is apparent that the frequency response is governed by the same factor $1/A\beta$ as in the case of the non-inverting stage. However, there is a difference because the low frequency closed-loop gain $|G(0)|$ is equal to RF/RG, not [assuming as before, that $A_O >> 1$]

But,

$$|G(o)| = \left[\frac{R_F + R_G}{R_G} \right] - 1 = \left[\left(\frac{1}{\beta} \right) - 1 \right] \tag{11}$$

hence

$$\left(\frac{1}{\beta} \right) = \left[|G(o)| + 1 \right] \tag{12}$$

As before, from equation (9), $f_b(1/\beta) = f_T$

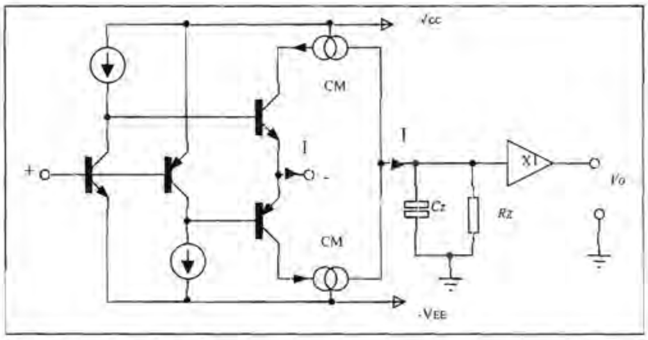
Substituting for $(1/\beta)$ from Equation 12,

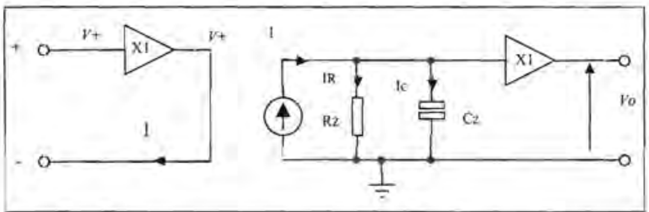
$$f_b * \left[|G(o)| + 1 \right] = f_T \tag{13}$$

For large values of $|G(0)|$ there is a little difference between this and Equation 9. However, for low values of $|G(0)|$ there is a significant difference.

In the case of a non-inverter, strapped as a voltage-follower, $f_b = f_T$, however, for a unity-gain inverter. What is the physical explanation for this?

The answer to this question, which was posed at the beginning





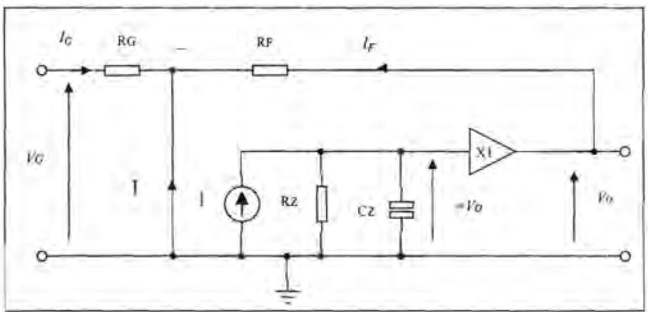
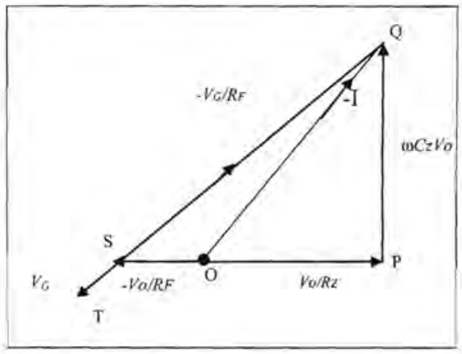
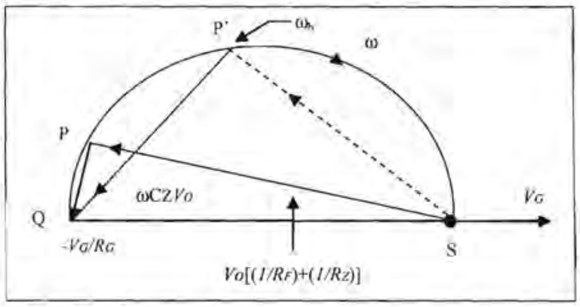


Figure 8 (Top): Basic schematic of a CFOA

Figure 9 (Middle): Small signal equivalent circuit for Figure 8

Figure 10 (Bottom): Equivalent circuit of a CFOA, based on Figure 9





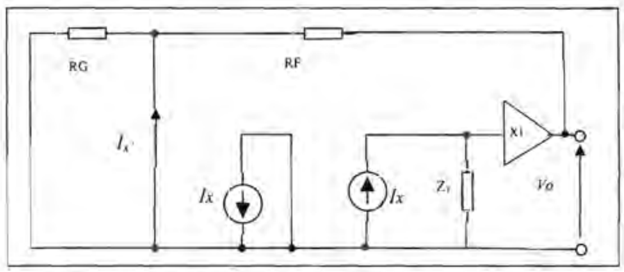


Figure 11a (Top): Phasor plot for Figure 10

Figure 11b (Middle): Another version of (a) with VG as the reference phasor

Figure 12: The loop-gain for the CFOA is $\left(\frac{I_x'}{I_x}\right)=-\left(\frac{Z_T}{R_F}\right)$ for test signal Ix (ZT represents RZ in parallel with CZ)

of this article, is that for the voltage follower, $\beta=1$, i.e there is a maximum feedback, but for the unity-gain inverter $\beta=0.5$, i.e. less feedback and, consequently, less closed-loop bandwidth.

Current-feed back op-amp configurations

A schematic of a simple current-feedback op-amp (CFOA) is shown in **Figure 8**: R_Z, C_Z are not necessarily added components but represent the effective resistance and capacitance seen at the input of the output voltage-follower stage. A simple small-signal equivalent circuit for the inverting configuration is shown in **Figure 10**. The analysis is similar to that presented earlier.

Referring to **Figure 11a** (not shown to scale), OP represents the current in R_Z and PQ the current in C_Z. These sum to $-I$ represented by OQ. However, by inspection of Figure 10, the error-current I is given by

$$I=-I_G-I_F=-\left(\frac{V_G}{R_G}\right)-\left(\frac{V_O}{R_F}\right) \tag{14}$$

In **Figure 11a**, OS= $-(V_O/R_F)$ so $-(V_G/R_F)$ must be SQ is in order to satisfy Equation 14: ST, oppositely directed to SQ, must therefore represent the direction of V_G. Rotating the diagram, anti-clockwise, as in the case of Figure 2b, gives **Figure 11b**.

Again, as ω varies, the locus of P is a semicircle on the diameter QS. The -3dB bandwidth frequency, f_b, occurs at P' where $\omega_b(=2\pi f_b)$is given by

$$\omega_b C_Z V_O = V_O\left[\left(\frac{1}{R_F}\right)+\left(\frac{1}{R_Z}\right)\right] \tag{15}$$

or,

$$f_b=\frac{1}{2\pi C_Z R_Q} \tag{16}$$

where, $R_Q=R_F/R_Z$ so,

For the reason discussed below, $R_Z>>R_F$, normally, so

$$f_b\approx\frac{1}{2\pi C_Z R_F}$$

This means the current in R_F is equal in magnitude to the current in C_Z at $f=f_b$, or the magnitude of the current loop-gain is unity. This is independent of R_G, so the product of the low frequency closed loop gain and f_b is not constant. The gain can be varied by changing R_G , but this does not effect f_b. This is true for the non-inverting configuration, as well.

Glancing again at Figure 11b, it is apparent that altering R_G changes the diameter of the semicircle but does not alter the relative position of P' on its perimeter.

Another way of appreciating the non-constancy of GBP is to look at the general expression for gain. If in Figure 10 we replace R_Z and C_Z by an equivalent impedance Z_T, then we can rewrite Equation 14 as,

$$I = \left(\frac{V_O}{Z_F}\right) = -\left(\frac{V_G}{R_G}\right) - \left(\frac{V_O}{R_F}\right)$$

Rearranging this gives,

$$G = \frac{V_O}{V_G} = -\frac{\left(\frac{R_F}{R_G}\right)}{\left[1 + \left(\frac{R_F}{Z_T}\right)\right]} \qquad (17)$$

In this, $-(Z_T/R_F)$ is the current loop-gain (see **Figure 12**), so Equation 17 is similar in form to Equation 10. However the frequency-dependency of the low frequency loop-gain magnitude (R_Z/R_F) does not involve R_G. We normally require that (R_Z/R_F) be large for good definition of low frequency closed-loop gain.

However, a limitation on the magnitude of R_Z, normally specified by the op-amp manufacturer, is required for Nyquist stability. It has to be remembered that Figure 9 is a simplified schematic and that in addition to the pole introduced by R_Z and C_Z there are additional CFOA poles due to the frequency response of the constituent current-mirrors and voltage-followers of the CFOA.

The constant GBP limitation for the simple voltage amplifier and voltage-feedback op-amp configurations is circumvented with current-feedback op-amps, because the factor governing low frequency loop-gain does not appear in the frequency-dependent expression that determines the bandwidth.

Conclusions

The above analysis shows how the GBP for a conventional transistor voltage amplifier, whether it is a single stage transistor amplifier or an op-amp, is constant. Also, it has been shown that the feedback factor is the same whether an op-amp is used in an inverting or non-inverting configuration. It is left to the reader to work out the expected bandwidth of the -20dB inverting attenuator. Finally, the current-feedback op-amp analysis shows that in this architecture of op-amp, the constant GBP rule of the voltage amplifier can be broken, with the gain and bandwidth separately controllable.

Switch-mode audio power amplifier performance measurements

Bruce Hofer, Audio Precision, and John Cornwell, Thurlby Thandar Instruments

Switch-mode audio power amplifiers are becoming increasingly popular because of their small size, low weight and good efficiency. Their advantages are obvious in low power, battery operated, personal audio players and laptop computers. However, they are also progressively displacing more traditional linear designs in mainstream applications such as home entertainment systems, automotive sound systems and professional installations, where high-quality audio is important.

Measuring the performance of switch-mode amplifiers presents some new and unique challenges. They inherently generate ultrasonic artefacts and spurious signals with slew rates that can provoke non-linear behaviour within the input stages of high-quality audio test and measurement equipment. Worthless and inaccurate results can result, unless effective measures are taken to prevent this non-linear behaviour.

Switch-mode amplifiers

Switch-mode amplifiers operate by using the output power devices as switches. Power amplification is accomplished by modulating the switching duty cycle of semiconductors (or vacuum tubes) as they alternate between high conduction and off states. Subtle differences in topology and how the switches are modulated has led to a plethora of amplifier classifications such as 'Class D', 'Class T', 'switching' and even 'digital' (although this is somewhat inaccurate). Other trademarked names are also being used. The term 'switch-mode' is used in this article to refer to all types.

Because switch-mode amplifiers operate by switching the output between power-supply rails, the raw time-domain output signal is not a linear replica of its input. It contains considerable amounts of high-frequency energy in the form of pulses and fast slewing edges. In the frequency domain, this signal can be separated into two regions. Within the intended passband, the output signal is a reasonably amplified version of the input. Beyond the passband, the output signal contains strong spectral components at the switching frequency and its harmonics. In some designs, the switching frequency may be purposefully varied to spread the high-frequency energy into a more noise-like spectrum.

In all cases, the switching frequency must be sufficiently high to ensure feedback stability of the amplifier and to prevent modulation sidebands of the switching frequency from folding down below the upper end of the desired audio passband. These constraints, plus other practical design considerations, usually require the switching frequency to be many times the maximum intended audio signal bandwidth. Switching frequencies of 250-750kHz are commonly used in full range 20kHz audio amplifiers.

Switch-mode amplifiers often include an output LC low-pass filter. The LC filter prevents power from being wasted due to the switching artefacts. The LC filter also prevents the amplifier from becoming an unlicensed transmitter of AM band energy, since the loudspeaker wires will act as antennas. This is a formidable task because real LC filters lose their effectiveness above a certain frequency. All inductors have a parallel capacitance, thus exhibiting self-resonance. Capacitors also have both series parasitic resistance and inductance that limit the filter's attenuation at high frequencies. Amplifier designers must often resort to controlled-risetime switching circuits and other clever design techniques to limit the high-frequency content in the switched output signal before it is filtered.

The LC filter also serves to prevent several potentially nasty problems when driving acoustic transducers. Switching artefacts can easily cause over-dissipation in tweeters and crossover elements, unless they are significantly attenuated. Asymmetric forms of non-linearity within loudspeakers and crossover elements also raise the possibility of intermodulation distortion (IMD) products appearing within the audio band. Inductors used in the crossover networks of many inexpensive loudspeaker systems are often very non-linear.

External passive filter

All commercial audio analysers employ precision low-noise, low-distortion operational amplifiers in their input and signal-processing stages. These devices have typical slew-rate capabilities of only 5-10V/μs compared to the thousands of volts per microsecond that can be present in the unfiltered output of a switch-mode amplifier. Connecting an audio analyser directly to the unfiltered output of a switch-mode amplifier is a recipe for measurement disaster. Once the input stage of the analyser is provoked into non-linear behaviour by fast-slewing signal components, all subsequent measurements will be invalid.

The inherent input slew-rate susceptibility of audio analysers is not the result of poor design. Mother Nature confounds us with practical tradeoffs between fast response and precision. Within the current state of the art, it is simply not possible to design a high-impedance analogue input stage having audio-worthy distortion and noise performance without incurring a practical slew-rate limitation. The input stages of oscilloscopes and laboratory-grade digital voltmeters may appear to contradict this statement.

However, the residual distortion and noise performance of these types of instruments is typically orders of magnitude worse than those of a low-end audio analyser.

Audio analysers should not be expected to respond linearly to analogue signals containing gross amounts of fast-slewing pulses or high-frequency energy.

The output LC filters contained in most switch-mode amplifiers vary greatly in their effectiveness in removing fast-slewing artefacts. Some do an admirable job. Others do not reduce the fast-slewing signal components to the point, where an audio analyser is totally free of non-linear effects. This can be especially true when measuring low-level output signals or noise, because the high-frequency switching artefacts tend to be more constant in amplitude. The only reliable solution to ensure measurement validity is to introduce a passive low-pass filter between the output of the switch-mode amplifier and the inputs of the audio analyser. Active filter designs will not work for the same reason that audio analysers are susceptible in the first place.

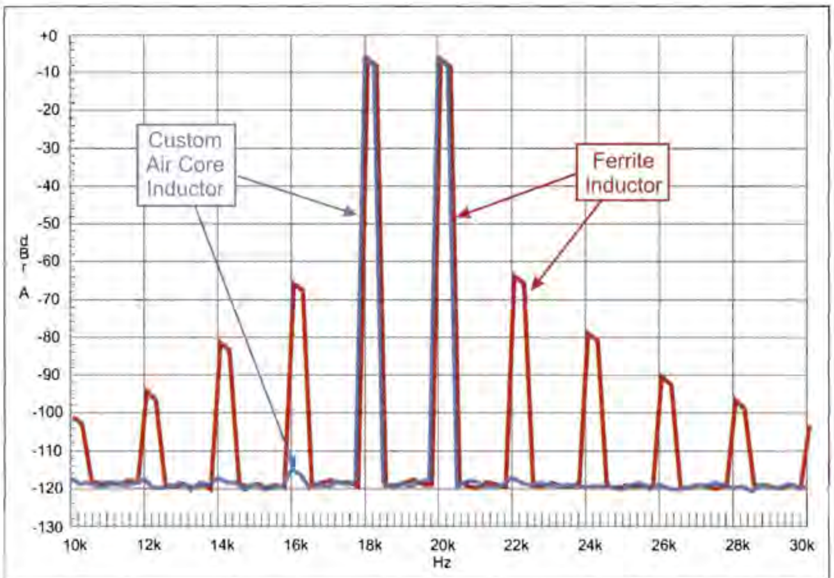


Figure 1: The effect of inductor core material on filter distortion. The red curve shows distortion with a typical ferrite core design. The blue curve shows virtually no filter distortion using a custom air-core design

The simplest passive filter design is the RC network. Because the output impedance of power amplifiers is very low within the audio band, the input impedance of the passive filter can be much lower than would otherwise be acceptable for the input of the audio analyser. It only needs to be large in comparison to a test load of between 2Ω and 8Ω.

Unfortunately, the performance tradeoffs of a single-stage RC filter are not very good. The RC filter values described above give a significant 19dB of attenuation for a 250kHz switching artefact, but at the price of 1.75dB roll-off at 20kHz (-3dB at 28.4kHz). This magnitude of response error will cause noise and distortion measurements to be lower than they actually are. It will also prevent the direct measurement of the amplifier's frequency response, without compensating for the RC filter's roll-off characteristic. As a point of reference, an RC filter must have a -3dB point above 131kHz to keep its response error below 0.1dB at 20kHz.

A multiple-stage LCR passive filter is much more desirable for this application. A single-stage filter may not give sufficient attenuation of all switching artefacts owing to limitations of inductor self-resonance and capacitor series resistance (ESR) and inductance (ESL). The LCR filter topology must be carefully chosen so that its input impedance does not become purely capacitive at high frequencies. This could cause excessive shunting currents to be drawn from the amplifier under test at its switching frequency, thus upsetting measurements of efficiency. Within the audio band, the input impedance of the filter must also be sufficiently high in comparison to a typical 2-8Ω resistive test-load so that it does not absorb significant amounts of signal power.

LCR filter inductors and capacitors must be extremely linear to prevent the unwanted introduction of harmonic and intermodulation distortion products. Air-core inductors are mandatory; iron and ferrite core designs simply will not give satisfactory performance. **Figure 1** shows the effect of inductor type on filter distortion in response to a twin-tone test signal of 18kHz and 20kHz. The red trace resulted from the use of an inexpensive off-the-shelf ferrite core inductor. The blue trace shows the same filter with custom air-core inductors of the same value.

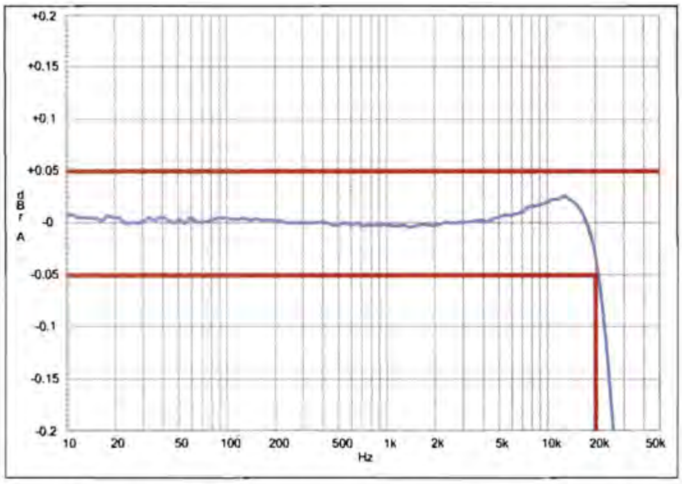
Measurement filter accessory

A filter accessory is now available to meet the demanding needs of measuring switch-mode amplifiers (**Figure 2**). The unit illustrated is a dual-channel, passive, multi-stage LCR filter, providing more than 50dB attenuation from 250kHz to 20MHz, ±0.05dB flatness over the 20kHz audio passband and only 0.05dB of insertion loss when connected to an analyser with a 100kΩ input impedance. It also features vanishing low distortion so it will pass audio signals with negligible degradation.

Figures 3 and **4** show typical passband and attenuation curves. Each side of both inputs is filtered with respect to ground, so that the stopband attenuation characteristic applies to both differential- and common-mode signals.

Figure 2: Audio Precision AUX-0025 switching amplifier

The input impedance of the filter can be modelled as a 10nF capacitor in series with 500Ω (each side of the input to ground) with reasonable accuracy up to about 30kHz. At higher frequencies, the 10nF reactive component will vary somewhat as resonances of the internal LC filter stages are reflected back to the input. The equivalent series input resistor limits energy absorption of the switching components of the amplifier's output and guarantees that the input impedance will never be less than 500Ω. It also minimises



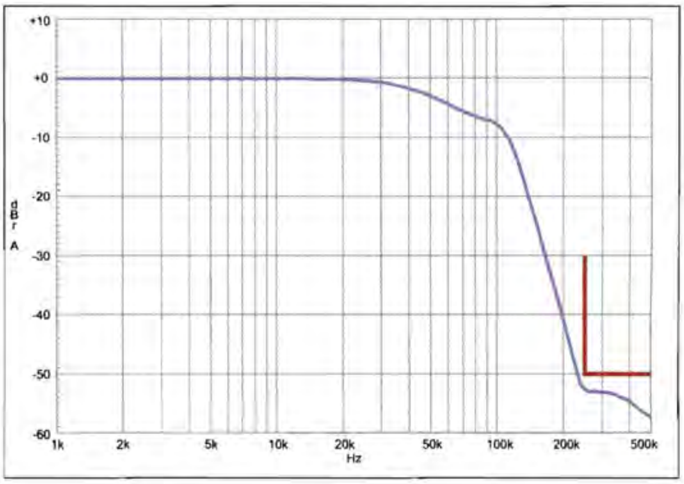


Figure 3: Typical passband response of the Audio Precision AUX-0025

Figure 4 (Above right): Typical high-frequency attenuation characteristic of the Audio Precision AUX-0025. The response above 500kHz is typically greater than 50dB to at least 20MHz

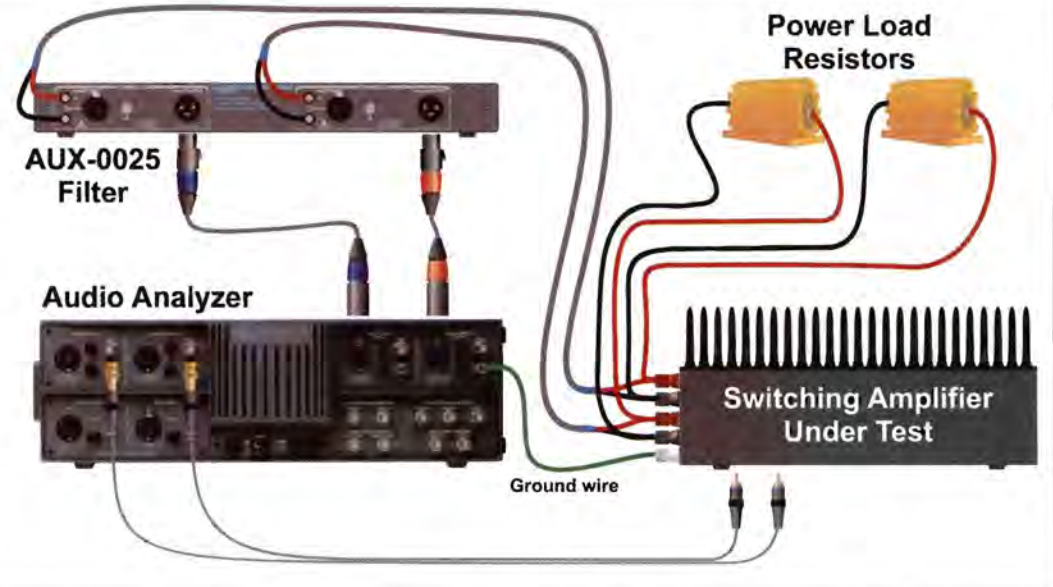


Figure 5: Recommended test setup using the AUX-0025. Note that the connections to the load are independent of the connections to the filter and analyser.

complex interactions with the LC filters that may be present behind the outputs of many switch-mode amplifier designs.

Compared to a typical 2Ω to 8Ω test load and the very low output impedance of the power amplifier, the loading effects of the device are practically negligible. The passband response characteristic remains valid with source impedances up to 2Ω. Usage with higher source impedances is possible, but it will cause additional filter roll-off at 20kHz. It should not be connected to typical line-level audio outputs.

Figure 5 shows the recommended connection of the filter in relation to the test load, the amplifier under test and the audio analyser. It is compatible with both single-ended and bridged amplifier output configurations, and with audio analysers having either unbalanced or balanced inputs. It is not designed to pass high-power, high-current signals through its input connectors.

Switch-mode amplifiers tend to have very noisy grounds that will impose unwanted common-mode potentials on both the amplifier and analyser input circuits. These can seriously limit the accuracy of audio measurements at low levels. Whenever possible, a short, multi-strand bonding wire should be connected directly between the ground of the amplifier under test and the analyser chassis. If shielded cables are used to connect the inputs of the AUX-0025 to the test load, the shields should be left unconnected at the test load end.

Conclusion

Switch-mode amplifiers offer significant power efficiency and size advantages. When properly designed, they can result in audio performance that rivals the very best obtainable with linear amplifiers. Measuring this performance can be very challenging, owing to the high slew-rate artefacts that can be present in some amplifiers' outputs. As this article has shown, a passive LCR filter is highly effective in eliminating measurement errors caused by the inevitable slew-rate limit effects within all audio analysers.

3D and video in a single core

By Borgar Ljosland

When mobile phones were first introduced, few could have predicted a future beyond simple text messaging. Yet, the time is fast approaching when consumers will expect their mobile phones to handle the same range of 2D, 3D and video formats that play on their desktop, with comparable quality. This presents unique challenges compared to those of the power-rich computer desktop. And since in the mobile environment chip size and battery life are of critical importance, this requires new approaches to implementing graphics and video.

Effective FSAA

One might think that with the small, limited resolution LCD panels on mobile phones, image quality might not be as important as with a desktop PC. Actually, the reverse is true, primarily because mobile phone users hold the display close to their eyes. This proximity to the screen makes it easier to spot artifacts due to under-sampling of geometry, commonly called 'aliasing' or 'jaggies'.

Almost all graphics core vendors use Full Scene Anti-Aliasing (FSAA) to minimise jaggies. While undeniably effective (see **Figure 1**), FSAA is generally quite memory and memory bandwidth intensive, because bandwidth requirements scale linearly with the number of samples per pixel used for anti-aliasing (4x the data for 4x FSAA). For this reason, most graphics core vendors offer only 2x FSAA or none at all.

As depicted in **Figure 2**, Falanx's Mali architecture uses four parallel pipes, each processing one sub-pixel for four. While this approach would seem to require increased gate count for the 4x FSAA renderer pipeline, that is not the case. Instead, by using the relative positions between the sub-samples down the pipeline, thin data-paths are required to handle the sub-pixel calculations. For 4x FSAA, this is utilised to perform one averaged texture look-up per pixel, which is carefully filtered and applied to all the sub-pixels. This technique is commonly known as multi-sampling and does not introduce additional texture bandwidth.

Finally, all sub-pixels use on-board memory for z-reads and writes, thereby eliminating the linear increase in bandwidth per sub-pixel, inherent in traditional immediate mode rendering pipelines.

For 16x, on-chip circuits up-sample the geometry to effectively produce 16 virtual sub-pixel pipelines. This technique does, however, add to bandwidth usage, increasing power consumption and slowing the frame rate.

Note that irrespective of image complexity, 4x FSAA frame rates are virtually identical to frame rates without FSAA and 4x FSAA produces minimal bandwidth spikes. Even with 16x FSAA enabled and the Mali100 core running at 40MHz, frame rates start at a respectable 60fps and remain above 20fps during the displaying of the most complex frame.

The availability of 16x FSAA means that mobile phones can deliver exceptional image quality for 3D game play at compelling frame rates. But can they do it with minimal power consumption?

Addressing power efficiency

The three major power consumption culprits in an embedded graphics system are gate count, software and memory bandwidth. Gate count is, more or less, a function of the total amount of gates in the design. Techniques like clock gating are either automated during the integration phase, or embedded directly into the core implementation. In the Mali architecture, the critical feature is that the core can detect when it has finished rendering a frame and automatically turns itself off. This can dramatically improve power savings, especially for frame rate locked applications. As these techniques are already in wide use, further reductions in power consumption come down to a function of gate count.

That said, the greatest power consumer in a graphics system is memory bandwidth. In addition, high bandwidth usage tends to slow other mobile phone functions that also require bandwidth. For these reasons, low bandwidth consumption is a critical feature for graphics cores.

At a high level, there are two stages of 3D processing that impact overall graphics bandwidth:

Figure 1: The improved visual quality produced by 4x and 16x FSAA. Note the significant reduction in jaggies surrounding the frame between no FSAA and 4x FSAA, and the additional detail in the wallpaper and painting with 16x FSAA

transform and lighting (geometry) and rendering (pixels). Geometry is either handled by the device CPU or a geometry co-processor like the MaliGP, with the output then transferred to the 3D processing unit for final rendering. Either way, when evaluating graphics technologies, it's critical to analyse and measure bandwidth consumption in both stages.

Traditional rendering schemes

Traditionally, there are two common ways to design 3D graphics processors: immediate mode rendering and tile-based rendering. With immediate mode rendering (**Figure 4**), operation during the geometry stage is relatively efficient, since the geometry engine simply sends all raw vertices to the raster engine. Once there, the raster engine renders, shades and textures each pixel, then sends it to an off-chip external z-buffer and colour buffer after it has determined if the pixel is actually visible in the frame and not obscured by other pixels. This method of handling z- and colour-values uses an enormous amount of bandwidth per rendered pixel and can easily bottleneck performance, especially when considering the additional per-pixel bandwidth required for texturing and alpha blending. The situation worsens with higher overdraw (depth complexity of the scene), because bandwidth is expended for pixels that will never be visible (reading textures and z-values for each pixel, times the overdraw, to check if the pixel will be visible).

With FSAA enabled, the already high per-pixel bandwidth in an immediate mode renderer increases linearly by the number of samples per pixel (e.g. two times for 2x FSAA, four times for 4x FSAA). This spikes memory bandwidth and power consumption significantly and often slows the display rate beyond acceptable levels. This is the reason why you seldom see more than 2x FSAA in immediate mode renderers for mobile phones.

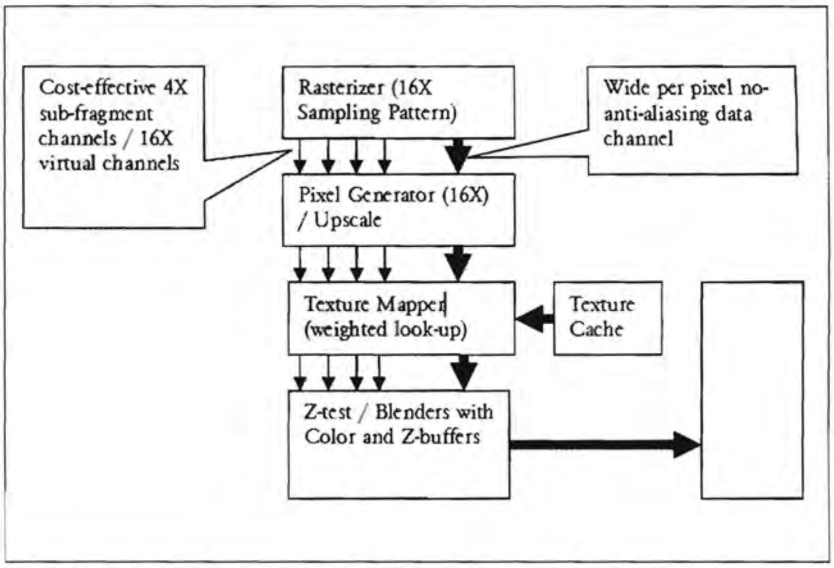


Figure 2: Block diagram for 4x/16x FSAA rendering

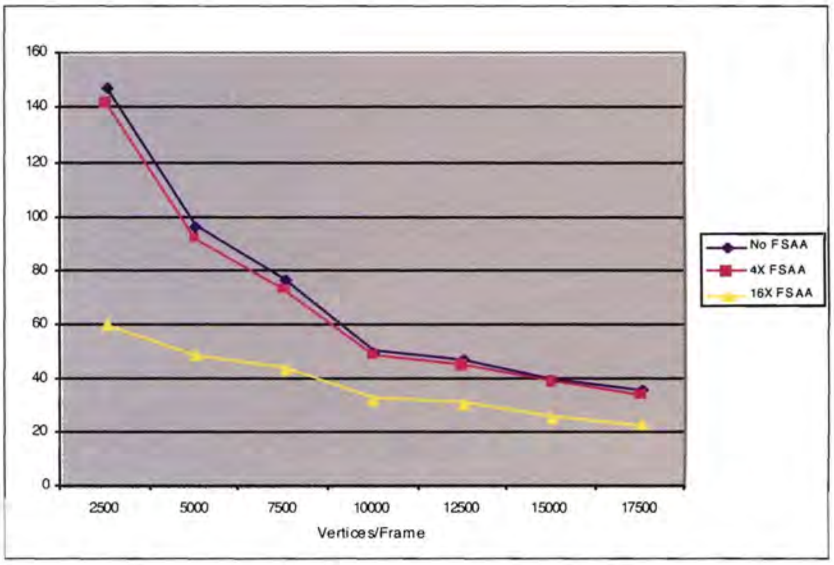


Figure 3: Frame rates with no FSAA and with 4x and 16x FSAA

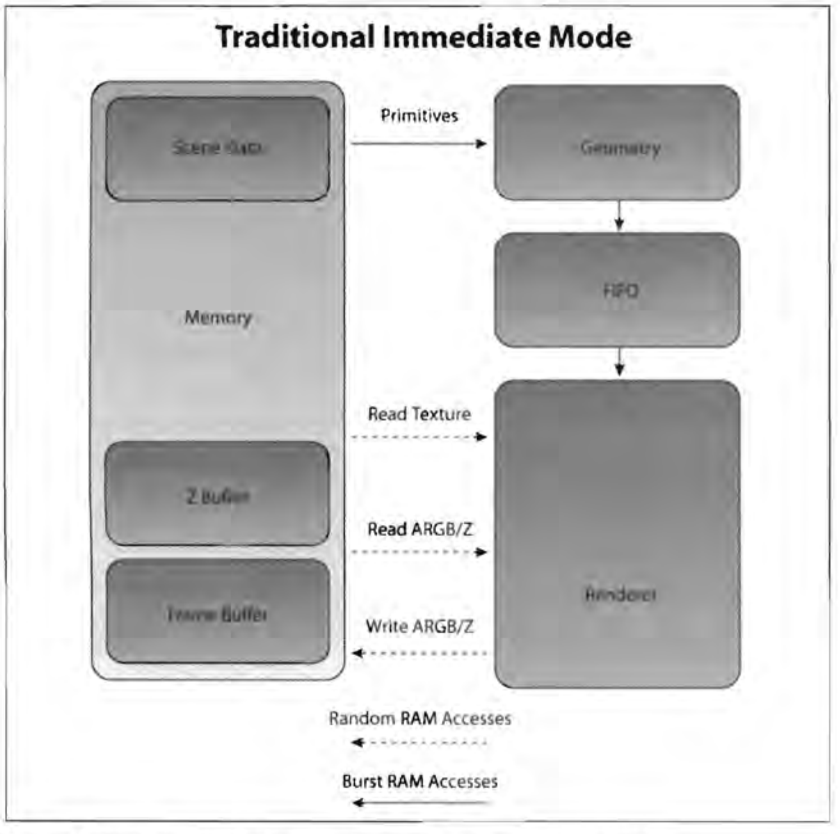


Figure 4: Block diagram of pipeline for immediate mode renderer

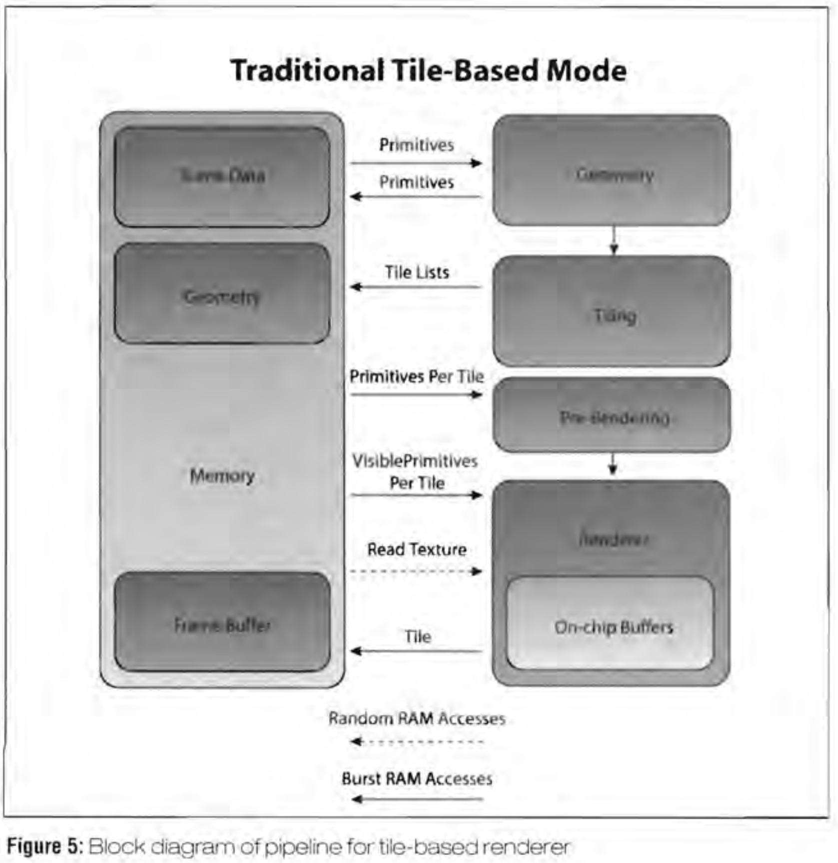


Figure 5: Block diagram of pipeline for tile-based renderer

Overall, traditional immediate mode rendering is a brute force approach that works acceptably well in the personal computer environment, where bandwidth is plentiful and power consumption largely irrelevant. However, in the bandwidth limited, power-starved mobile cell phone environment, it's clearly not the optimal architecture.

Tile-based renderers

Tile-based rendering (**Figure 5**) reduces per pixel bandwidth inefficiencies by breaking each frame into separate blocks called tiles, rendering them independently and then assembling them together before display. This enables tile-based renderers to perform z-buffer calculations on-chip, eliminating traffic to the z-buffer. The cost is added bandwidth per primitive, though this is seldom mentioned.

An enhancement to tile-based rendering is so-called Hidden Surface Removal (HSR), which introduces a pre-rendering pass and fills the z-buffer with values that track which pixels are visible. Then, in a second pass, the chip can render and fetch the textures for only those visible pixels. This reduces texture bandwidth per pixel because of reduced overdraw, but potentially doubles vertex bandwidth, and requires increased gate count over typical immediate mode renderers.

With FSAA enabled in a traditional tile-based architecture, the numbers of pixels that must be analysed for visibility increases linearly with the number of samples (e.g. 2x for 2x FSAA), again boosting the bandwidth usage per vertex to unacceptable high levels. However, since bandwidth has been saved on texture data because of HSR and the on-chip z-buffers, FSAA will often require lower bandwidth than in an immediate mode renderer.

In sum, traditional tile-based renderers offer better bandwidth utilisation than immediate mode renderers in low complexity games, but as scene complexity increases, the bandwidth saving per pixel is eroded by the additional bandwidth usage for geometry. HSR increases the gate count and, when anti-aliasing is enabled, memory bandwidth usage increases significantly over that required for non-FSAA display.

Hybrid approach

The Falanx Mali architecture (**Figure 6**) is a hybrid between tile-based and immediate mode renderers. In the geometry phase, the Mali architecture operates like most tile-based renderers, dividing the image into tiles but using a proprietary method that reduces per vertex bandwidth and memory usage. Rather than performing all z-ordering before retrieving textures (HSR), Mali relies on two cost-efficient techniques to reduce texture bandwidth.

First is a proprietary and highly efficient Early Z implementation that is virtually free in terms of gates and typically eliminates approximately 50% of occluded pixels, reducing texture bandwidth by the same percentage. Then, Mali applies high-quality two bits per pixel texture compression, FLXTC, a method that virtually eliminates the need to reduce texture bandwidth any further.

The hybrid of immediate mode and tile-based renderer techniques is significantly more bandwidth-efficient compared to a single approach, even without considering the added efficiency of 4x FSAA. With 4x FSAA enabled, the hybrid approach requires even less bandwidth under a broad range of operating conditions.

Without FSAA, the tile-based architecture requires less bandwidth than immediate mode for the geometry complexities that can be expected by advanced 2006 mobile games, which will be about 10-15k polygons. The hybrid architecture is even more efficient. As scene complexities approach roughly 20,000 polygons, however, immediate mode becomes the preferred approach.

It's clear that the power-hungry graphics technologies that work on desktop computers are poorly suited for mobile phones. So the race is on to implement graphics technology that allows mobile phone users to enjoy new classes of content, while meeting the size and power consumption requirements of mobile phone vendors.

Whatever the outcome, it's a safe bet that the 'plain vanilla' voice-only phone will soon join the rotary phone and the manual typewriter in the museum of obsolete technologies.

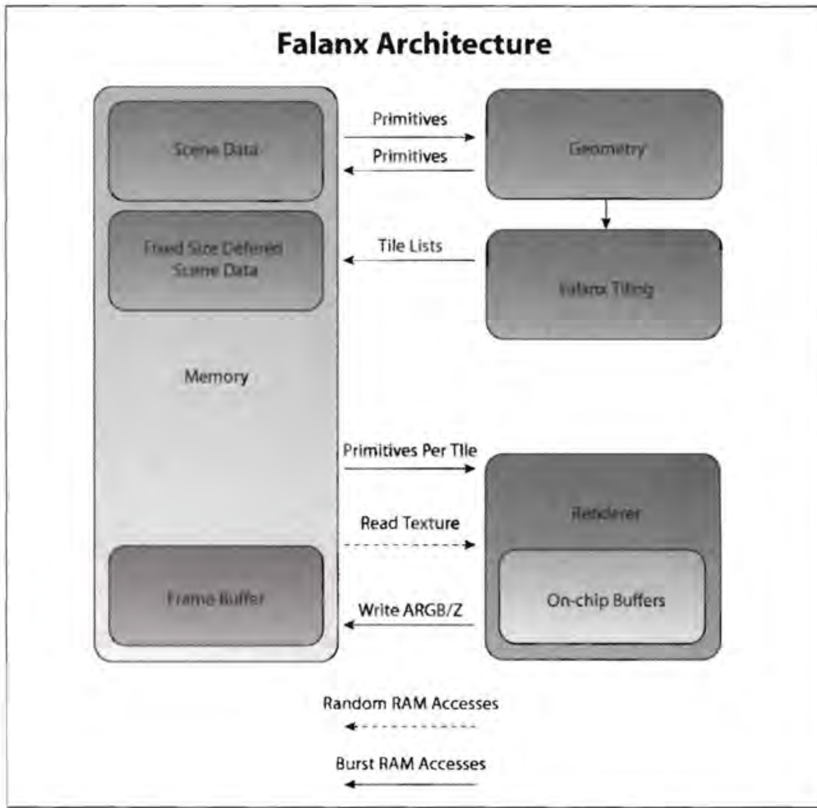


Figure 6: Block diagram of pipeline for the Falanx Mali architecture

Mali cores

The Mali IP Cores are single pipeline 2D/3D/Video IP rasteriser cores that deliver 30fps encode and decode of video, along with 16x Full Scene Anti-Aliasing (FSAA) support and texture filtering. In a bid to lower gate count, Falanx has designed methods for re-using 3D gates for video encoding and decoding. Originally designed in 1998 to meet the OpenGL 2.0 standard, the Mali architecture has been streamlined to conform to OpenGL ES1.1.

The Mali55 offers the lowest gate count, designed to match the ARM9/ARM11 cores for transform and lighting (T&L). The Mali55 can also be matched with MaliGP for higher video performance and reduced power consumption for 3D graphics. The Mali110 is designed for high-performance 3D graphics and video with performance matched with MaliGP, a programmable vertex shader/DSP architecture for T&L and acceleration of video encoding and decoding algorithms.

Implementing RAID storage with a 4-port FC controller and PCI

Brian L'Ecuyer, Engineering Scientist, Systems Architecture, Semiconductor Products Group, Agilent Technologies

This article takes the reader through a system design for implementing a RAID controller using the Fibre Channel protocol. Specifically discussed is an implementation of an Agilent Tachyon 4GB/s four-port Fibre Channel protocol IC to attach multiple disk links to one computing system delivering RAID applications.

The introduction provides an overview of an overall system using RAID storage, including Fibre Channel topologies and options, FC termination, disk links and processor functionality.

RAID system architecture overview

Data storage is increasing in application space. Formerly benign devices now contain or produce relatively large amounts of digital information. The time to create such dense data drives the need for secure storage of information. As data is archived over time, the cost for re-archiving lost data becomes enormous. Systems for making data access reliable are employed as data is archived or stored. As the need for securing data increases, the need for RAID solutions also increases. RAID provides several options for increased data retrieval success. Data storage is currently focused on mechanical drive media, though RAID techniques can be applied to any digital storage medium where reliable retrieval is needed.

For a complete system to implement RAID the following points need to be considered:

- A controller-processing complex of one or more CPUs.
- Some number of disks need to be connected to the complex. The connection of the disks is normally accomplished via a protocol specifically for drive attachment. There are several popular disk protocols. Here, we will focus on the Fibre Channel protocol as employed in most high-end storage array designs.
- An efficient connection cannot be made directly between the drives and the processors. A protocol converter is used to provide an API to the processors on one interface and connections to the drives on another interface.

Figure 1 shows a typical system comprising four CPUs, a processor complex consisting of a memory controller and interface device, a protocol controller and an array of multiple Fibre Channel links. There are many variations and tradeoffs associated with disk controller architectures that are not discussed in this article. This is the simplest general architecture, which will serve to describe normal functionality in a RAID controller.

RAID overview

The concept of a RAID implementation is not only the storing of data for later retrieval but the employment of one or more of several levels of RAID as described below:

RAID-0: Striping – Striping does not add security but rather performance. A file is stored across multiple drives. Sector sizes of the file are written to successive disks to spread and overlap the write latency of a single drive.

RAID-1: Mirroring – All of the data on one disk is copied exactly onto a second disk. This requires data to be written to separate disks involving two separate write operations. Neither disk is the master or primary; the disks are clones. For writes to be deemed complete, they must make it to both disks. If one disk fails, its peer keeps functioning, without interruption. With RAID-1, it's very easy to manage and it does not require significant levels of CPU for normal operations or for recovery. The downside to RAID-1 is the expense: For every gigabyte of disk you wish to protect, you need a second, matching gigabyte. In other words, RAID-1 requires twice as much disk space as unprotected disks.

RAID-2: Hamming code error correction – RAID-2 uses the same hamming encoding method for checking the correctness of disk data that error correcting code memory (ECC) uses.

RAID-3, RAID-4, and RAID-5 are all variations on a theme of parity-based RAID. Instead of keeping a full copy of the data as in RAID-1, these levels spread the data over several disks with an additional disk added. The data on the additional disk is calculated (using Boolean XORs) based on the data on the other disks. If any disk in the set is lost, its data can be recovered through calculations on the data on the remaining disks. These implementations are less expensive than RAID-1 because they do not require the 100% disk overhead that RAID-1 requires.

However, because the data on the disks is calculated, there are performance implications associated with any writing, and with recovering after a disk is lost.

RAID-3: Virtual disk blocks – In RAID-3, every write is split (striped) across all of the disks (usually four or more) in the RAID array. Since every write touches every disk, the array can only be writing one block of data at a time that can cause poor performance from the RAID. RAID-3 performance varies based on the nature of the writes: Small writes scattered all over the disks will have very poor performance. Larger sequential writes will result in better performance.

RAID-4: Dedicated parity disk – In a RAID-4 array, there is a set of data disks, usually four or five (although there could be more, at a significant performance penalty), plus one extra disk that is dedicated to managing the parity for the data on the other disks. Since all writes must go through the parity disk, that disk becomes a performance bottleneck slowing down all write activity to the entire array.

RAID-5: Striped parity – RAID-5 is virtually identical to RAID-4 except that instead of all of the parity being concentrated on a single disk, it is divided up, with a share being given to each disk in the array. This sharing will balance and reduce the performance impact that is evident in RAID-4 implementations. In software implementations of RAID-5, which are fairly common, performance will often become unacceptably slow if writes make up any more than about 15% of disk activity.

In order to implement any combination of RAID, several functions need to be considered. For RAID implementations above level zero, multiple disks are generally connected. In order to achieve striping, mirroring and parity, multiple disk accesses or operations are used. For example, to implement RAID-1 two drives could be written to successively. A write or read operation is referred to as a disk I/O. This can be any protocol for communicating to a drive or multiple drives. This functionality is implemented in software operating on one or more of the processors in the system. The flow is to execute a high-level write to disk while implementing RAID and communicating through the protocol controller API.

It is preferred to have a protocol controller that manages as much of the disk link as possible, to allow the processing complex to work on RAID applications and system management functions. For complex protocols like Fibre Channel, where connections state and multiple drive links are deployed, a high-end controller like the Tachyon series offers the highest total system performance.

Tachyon architecture

The Tachyon family of Fibre Channel protocol controllers implements 1GB, 2GB and 4GB Fibre Channel links, and connects to the system through PCI, PCI-X or PCI Express interfaces, depending on the device.

Despite significant advancements in both Fibre Channel technology and system bus interconnect technology, the architecture of the Tachyon protocol engine scales directly with improvements in semiconductor process technology. The architecture is based on a Finite State Machine (FSM) design, which uses numerous independent state machines operating in parallel, to

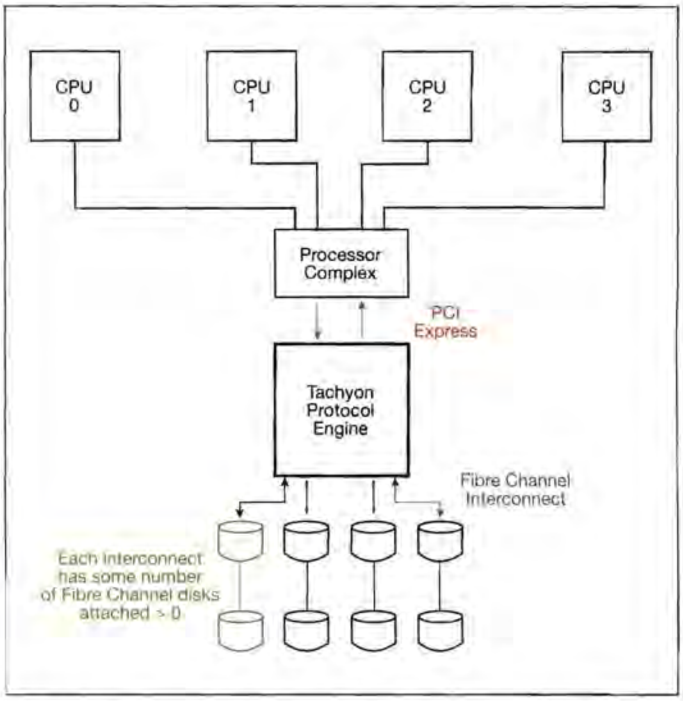
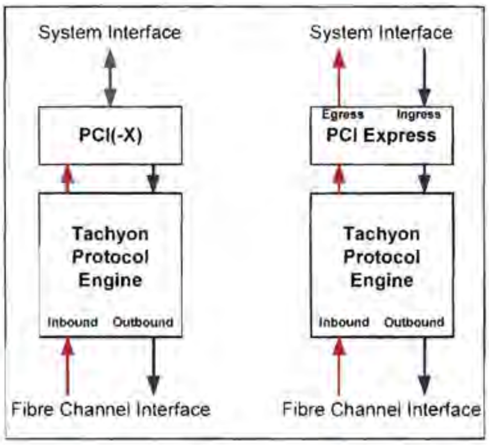


Figure 1: A typical system representing the simplest general architecture for describing functionality in a RAID controller

Figure 2: Comparing the bi-directional bus system interface of PCI and PCI-X with the independent Ingress and Egress paths provided by PCI Express



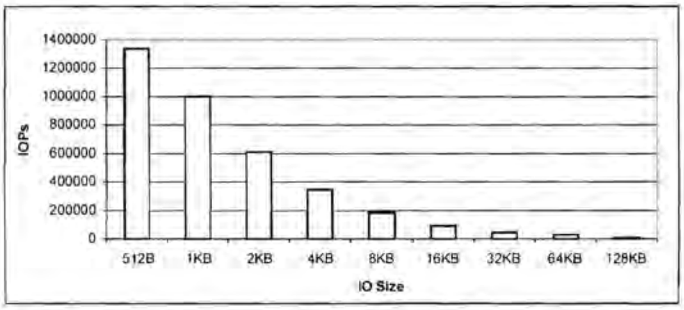


Figure 3: Sequential read IOPs vs I/O size, using currently-available PCI Express chipsets with a single Agilent QX4 Tachyon Fibre Channel controller IC

obtain significantly higher performance than a firmware or software solution can achieve. As frequency increases, the performance of Tachyon increases proportionately, compared to a firmware-based solution, where circuit frequency does not directly improve algorithm performance.

The Tachyon architecture permits inbound and outbound data paths to operate independently and simultaneously, allowing full duplex operation at full Fibre Channel link rates. Additionally, the control requirements of the I/O operations are handled concurrently with data movement, maximising the use of the data movement machines.

The Finite State Machine (FSM) architecture performance scales with clock frequency. The FSM design can make decisions on every clock cycle and does not rely on memory access speed for instruction and data fetches, as do embedded microprocessors. In addition to scaling with process technology for link performance, Tachyon uses technology improvements in the system interface bus, increasing I/O per second performance capability.

PCI Express suitability

In the past, the shared resources of a bi-directional system bus interface, such as PCI and PCI-X, limited the full duplex capability of the Tachyon architecture. The two independent data movement machines in Tachyon contend with each other for bus tenancies on the PCI or PCI-X system interface.

PCI Express, with independent Ingress and Egress data path links, creates a perfect match for the Tachyon architecture. The coupling of the Express Ingress data path with the Tachyon outbound data path and the Express Egress data path with the Tachyon Inbound data path, permits data to flow freely in both directions simultaneously, just as the original Tachyon architecture intended.

Moving from a bidirectional-directional system bus to a pair of unidirectional links also removes lost bus cycles associated with connected transactions, where a request (i.e. register read) would wait on the bus for data to return. Additionally, because PCI Express is a serial link technology, requests can be pipelined. A number of pipelined requests will achieve higher utilisation of the target device capabilities.

Now that PCI Express provides pairs of bidirectional-directional serial links, the same as the Tachyon Fibre Channel controller, bandwidth capability can be described in terms of bytes transferred per second per link direction. A single lane of PCI Express consists of two unidirectional serial links operating at 2.5GB/s capable of 250MB per second per direction after encoding/decoding. The Tachyon family on PCI Express (QX4 and QX2) can be configured for 1, 4, or 8 lanes of PCI Express, giving it up to 4GB of aggregate bandwidth or 2GB bandwidth in each direction.

Table 1 shows how the Tachyon family bandwidth requirements map into the PCI Express capabilities.

The table shows that eight lanes of PCI Express are theoretically capable of supporting all four functions of a QX4 (four 4GB Fibre Channel links) at full link rate with 80% utilisation of the PCI Express interface. A PCI Express root complex that supports multiple four lane Express links can connect to two QX2 devices (four lanes of PCI Express for each device) and achieve full Fibre Channel link rate at 2GB/s on all eight ports at 80% utilisation.

The serial link nature of PCI Express, combined with Express's flexibility, makes it the optimal system interface bus for the Tachyon Fibre Channel protocol controller family. The backward compatibility of the PCI Express protocol simplifies the decision to migrate from PCI or PCI-X system interface bus to PCI Express as driver compatibility is maintained.

With highly integrated devices like Tachyon, it is possible to construct high performance RAID system with the remaining components being off-the-shelf products. The variability of processor and memory design can tune a solutions performance for target system application from low-end SMB to high-end data centre arrays, all leveraging a common system software investment.

Current PCI Express performance

The previous tables describe the raw bit-rate performance of the PCI Express bus. It does not take into account any PCI Express associated overhead. PCI Express traffic primarily

Table 1: The mapping of Tachyon bandwidth requirements into PCI Express capabilities

	Bandwidth (Full duplex)	*Bus type & and width*	*# Functions*	*Aggregate Bandwidth*
PCI Express	500 Mb/s per lane	Serial 8 lanes	N/A	4.0 Gb/s
PCIX 1.0	1066 Mb/s total	Parallel 64-bit	N/A	1.0 Gb/s
PCIX 2.0	2131 Mb/s total	Parallel 64-bit	N/A	2.0 Gb/s
4G FC	800 Mb/s per port	Serial 1 lane	1	0.8 Gb/s
4-port 4G FC	800 Mb/s per port	Serial 1 lane	4	3.2 Gb/s

Table 2: Measured QX4 performance vs theoretical PCI-Express bandwidth, with various TLP sizes

PCI-Express Configuration	*Theoretical bandwidth without DLLPs and PLPs*	*Measured QX4 1.1*	*PCI Express bus efficiency*
64-byte TLP half-duplex	1.52 Gb/s	1.43 Gb/s	94%
128-byte TLP half-duplex	1.73 Gb/s	1.53 Gb/s	88%
Full- duplex (with 64-byte TLP Read and 128-byte TLP Write)	3.25 Gb/s	2.75 Gb/s	84%

consists of Transaction Layer Packets (TLPs). Every TLP contains the associated data, as well as a header and other sequence tracking/error detection information. In addition to TLPs, there are Data Link Layer Packets (DLLP). These DLLPs are primarily used for the ACK/NAK protocol, as well as Flow Control Mechanisms. Physical Layer Packets (PLPs) are also present, but are primarily used for low-level functionality and non-performance path operations, such as link training and low power states.

There is a considerable amount of overhead on every TLP. Every TLP contains a header, CRCs and other framing information. Because every TLP has a fixed overhead, a larger TLP size will translate into higher bus utilisation. If we assume that the quantity of DLLPs and PLPs is negligible in comparison to the number of TLPs, we can calculate a theoretical maximum PCI-Express bandwidth based solely upon the TLP size.

Table 2 compares measured QX4 performance with the theoretical PCI Express bandwidth and various TLP sizes supported by a readily available (Jan 2005) PCI Express Root Complex.

Table 2 assumes no overhead associated with FCP traffic, Tachyon data structures or Tachyon register accesses. The theoretical numbers also assume zero latency within the PCI-Express root complex. The measured QX4 1.1 numbers include FCP traffic overhead, Tachyon data structure and register access overhead, and PCI Express latencies.

During half duplex traffic (tops are only transmitted in one direction), Link Control DLLPs are sent in the opposite direction of the data TLPs and, therefore, will not degrade performance. Once full duplex traffic is introduced, Flow Control DLLPs and Data TLPs are now sharing the same PCI Express lanes; any Flow Control DLLP will cause a delay in the transmission of a data TLP. Again, all theoretical bandwidth numbers assume a negligible impact by DLLPs and PLPs.

The above bandwidth discussion demonstrates how well PCI Express scales with 4GB Fibre Channel devices. An IOPS (I/O per second) number is defined by the number of 512-byte I/0s a device may complete within one second. IOPS measurements also scale well with PCI Express.

Using currently available PCI Express chipsets and a single Agilent QX4, we have measured IOPS numbers in excess of 1.3 MIOPS (**Figure 3**). As processor speeds – as well as supported TLP sizes – increase, we expect to see even higher performance.

PICmicro: Microcontroller CCP and ECCP

TIP 1: Repetitive phase shifted sampling

Repetitive phase shifted sampling is a technique to artificially increase the sampling rate of an A/D converter when sampling waveforms that are both periodic and constant from period-to-period. The technique works by capturing regularly spaced samples of the waveform from start to finish of the waveform's period. Sampling of the next waveform is then performed in the same manner, except that the start of the sample sequence is delayed a percentage of the sampling period. Subsequent waveforms are also sampled, with each sample sequence slightly delayed from the last, until the delayed start of the sample sequence is equal to one sample period. Interleaving the sample sets then produces a sample set of the waveform at a higher sample rate. **Figure 1** shows an example of a high-frequency waveform.

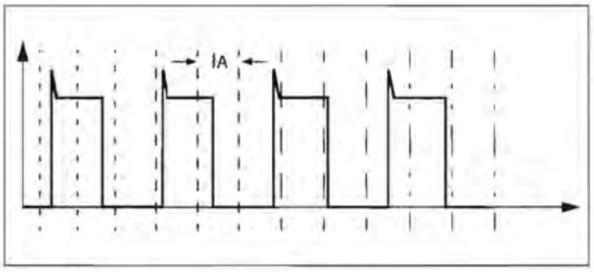


Figure 1: High frequency periodic waveform

As indicated in the key, the finely dotted lines show where the A/D readings are taken during the first period of the waveform. The medium sized dashed lines show when the A/D readings are taken during the second period and so on. **Figure 2** shows these readings transposed onto one period.

The CCP module is configured in Compare Special Event Trigger mode to accomplish this task. The phase shift is implemented by picking values of CCPRxL and CCPRxH that are not synchronous with the period of the sampling waveform. For instance, if the period of a waveform is 100µs, then sampling at a rate of once every 22µs will give the set of sample times in **Table 1** over 11 periods (all values in µs).

When these numbers are placed in sequential order, they reveal a virtual sampling interval (IV) of 2µs from 0µs to 100µs, although the actual sampling interval (IA) is 22µs.

Pulse-width modulation tips

The ECCP and CCP modules produce a 10-bit resolution Pulse Width Modulated (PWM) waveform on the CCPx pin. The ECCP module is capable of transmitting a PWM signal on one of four pins, designated P1A through P1D. The PWM modes available on the ECCP module are:

- Single output (P1A only)
- Half-bridge output (P1A and P1B only)
- Full-bridge output forward
- Full-bridge output reverse

One of the following configurations must be chosen when using the ECCP module in PWM full-bridge mode:

- P1A, P1C active-high; P1B, P1D active-high
- P1A, P1C active-high; P1B, P1D active-low
- P1A, P1C active-low; P1B, P1D active-high
- P1A, P1C active-low; P1B, P1D active-low

"Why would I use PWM mode?"

As the next set of Tips 'n Tricks demonstrates, Pulse-Width Modulation (PWM) can be used to accomplish a

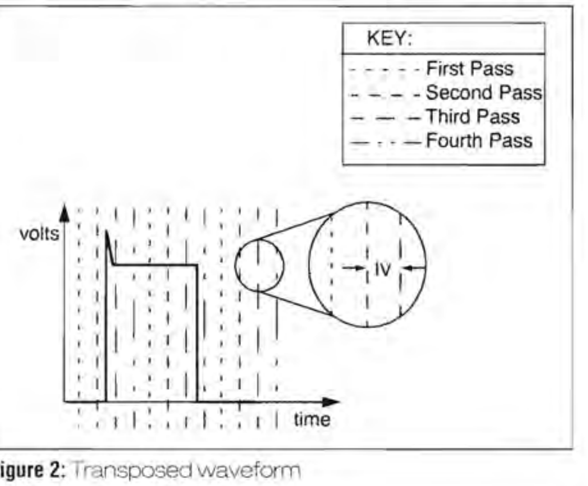


Figure 2: Transposed waveform

Table 1: Set of sample times

1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th
0	10	20	8	18	6	16	4	14	2	12
22	32	42	30	40	28	38	26	36	24	34
44	54	64	52	62	50	60	48	58	46	56
66	76	86	74	84	72	82	70	80	68	78
88	98		96		94		92		90	

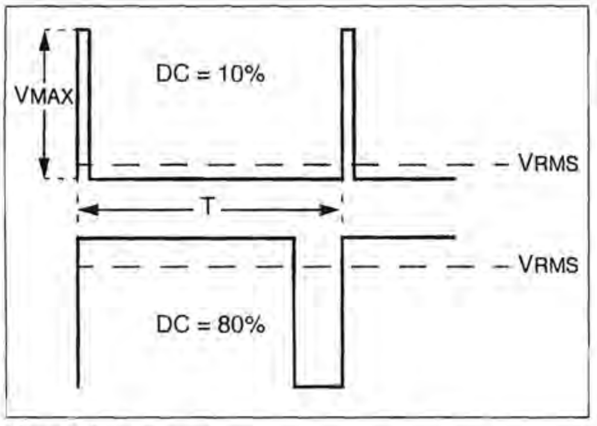


Figure 3: PWM signal

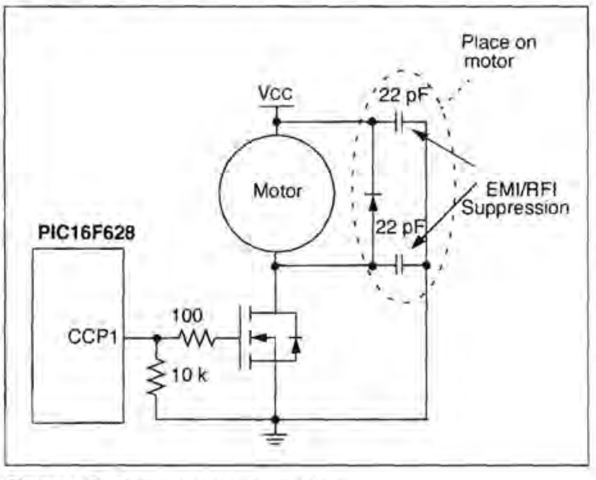


Figure 4: Duty cycle relation to V_{RMS}

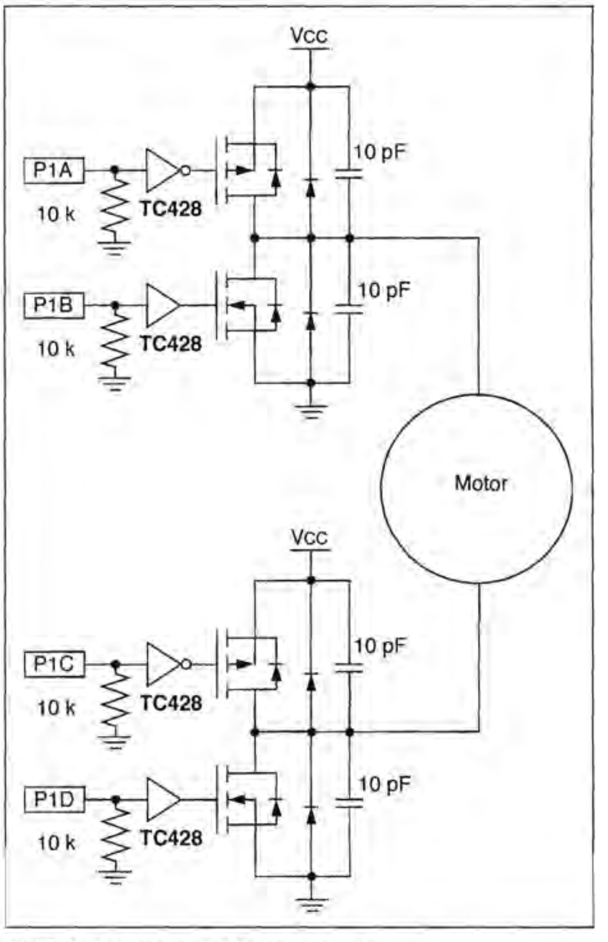


Figure 5: Full-bridge BDC drive circuit

variety of tasks, from dimming LEDs to controlling the speed of a brushed DC electric motor. All these applications are based on one basic principle of PWM signals – as the duty cycle of a PWM signal increases, the average voltage and power provided by the PWM increases. Not only does it increase with duty cycle, but also it increases linearly. **Figure 3** illustrates this point more clearly. Notice that the RMS and maximum voltage are functions of the duty cycle (DC). The following equation shows the relation between VRMS and VMAX.

$$VRMS = DC \times VMAX$$

TIP 2: Deciding on PWM frequency

In general, PWM frequency is application-dependent, although two general rules-of-thumb hold regarding frequency in all applications. These are:

1. As frequency increases, so does current requirement due to switching losses.
2. Capacitance and inductance of the load tend to limit the frequency response of a circuit.

In low-power applications, it is a good idea to use the minimum frequency possible to accomplish a task in order to limit switching losses. In circuits where capacitance and/or inductance are a factor, the PWM frequency should be chosen based on an analysis of the circuit.

Motor control

PWM is used extensively in motor control due to the efficiency of switched drive systems as opposed to linear drives. An important consideration when choosing PWM frequency for a motor control application is the responsiveness of the motor to changes in PWM duty cycle. A motor will have faster response to changes in duty cycle at higher frequencies. Another important consideration is the sound generated by the motor. Brushed DC motors will make an annoying whine when driven at frequencies within the audible frequency range (20Hz-4kHz.) In order to eliminate this whine, drive brushed DC motors at frequencies greater than 4kHz. (Humans can hear frequencies at upwards of 20kHz, however, the mechanics of the motor winding will typically attenuate motor whine above 4kHz).

LED and light bulbs

PWM is also used in LED and light dimmer applications. Flicker may be noticeable with rates below 50Hz. Therefore, it is generally a good rule to pulse-width modulate LEDs and light bulbs at 100Hz or higher.

TIP 3: Unidirectional-brushed DC motor control using CCP

Figure 4 shows a unidirectional speed controller circuit for a brushed DC motor. Motor speed is proportional to the duty cycle of the PWM output on the CCP1 pin. The following steps show how to configure the PIC16F628 to generate a 20kHz PWM with 50% duty cycle. The microcontroller is running on a 20MHz crystal.

Step #1: Choose Timer2 prescaler
a) FPWM = FOSC/((PR2+1)•4•prescaler) = 19531Hz for PR2 = 255 and prescaler of 1
b) This frequency is lower than 20kHz, therefore, a prescaler of 1 is adequate.

Step #2: Calculate PR2
PR2 = FOSC/(FPWM•4•prescaler) - 1 = 249

Step #3: Determine CCPR1L and CCP1CON<5:4>
a) CCPR1L:CCP1CON<5:4> = DutyCycle•0x3FF = 0x1FF
b) CCPR1L = 0x1FF >> 2 = 0x7F, CCP1CON<5:4> = 3

Step #4: Configure CCP1CON
The CCP module is configured in PWM mode with the Least Significant Bits of the duty cycle set, therefore, CCP1CON = 'b001111000'.

TIP 4: Bi-directional brushed DC motor control using ECCP

The ECCP module has brushed DC motor control options built into it. **Figure 5** shows how a full-bridge drive circuit is connected to a BDC motor. The connections P1A, P1B, P1C and P1D are all ECCP outputs when the module is configured in "Full-bridge Output Forward" or "Full-bridge Output Reverse" modes (CCP1CON<7:6>). For the circuit shown in Figure 5, the ECCP module should be configured in PWM mode: P1A, P1C active high; P1B, P1D active high (CCP1CON<3:1>). The reason for this is the Mosfet drivers (TC428) are configured so a high input will turn on the respective Mosfet. **Table 2** shows the relation between the states of operation, the states of the ECCP pins and the ECCP configuration register.

Table 2: Relation between the states of operation, ECCP pins and ECCP configuration register

State	*P1A*	*P1B*	*P1C*	*P1D*	*CCP1CON*
Forward	1	Tristate	Tristate	mod	'b01xx1100'
Reverse	Tristate	mod	1	Tristate	'b11xx1100'
Coast	Tristate	Tristate	Tristate	Tristate	N/A
Brake	Tristate	1	1	Tristate	N/A

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Microchip is offering readers of Electronics World the chance to win a PICSTART Plus Programmer. The latest version of Microchip's popular microcontroller programmer kit includes the PICC Lite ANSI-C Compiler for use with the PIC16F84A Flash microcontroller. The PICSTART Plus supports all existing Microchip 8-bit OTP and Flash MCUs including the popular PIC12CXXX, PIC16cXX and PIC17CXX devices.

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The value of involvement

By Mike Brookes

Previously, we reported on the activities of a Project Team (PT 43) set up by the Frequency Management Group (WG FM) of the European Communications Committee (ECC).

PT 43 is devoted to obtaining views from both industry and radio regulators on the usefulness of current Short Range Device (SRD) standards and regulations and on the progress of frequency harmonisation.

The Report from PT 43 is intended to satisfy the requirement of the second EC mandate for Short Range Device issued by the European Commission (EC). The mandate objectives are to get data from which to derive a strategy for the future of SRDs.

While this might sound like another dose of Euro babble, it is actually of vital importance to the SRD industry – makers and users alike. This is because EC's decisions and directives are binding on EU member states, so that the resulting EU-wide radio strategy will have major effects for 10 years or more after absorption of the PT 43's final report in mid-2006.

This may seem a long time off, but because of the meeting timescales of ECC/EC bodies the interim (skeleton) report will be finalised in September 2005 and 'final' data must be in PT 43 by spring 2006.

If you think this is of no importance for anyone, but only the big companies and Eurocrats have a say, it is not the case. Excluding Wi-Fi and UWB (which are excluded from PT 43's scope), for SRDs, the vast majority of work by the industry to produce standards and regulations is done by small to medium size enterprises (SMEs). You can make a real impact on your future by making your views known. If you don't, you have no one to blame but yourselves for the 'wrong' policies being produced.

The main questions being asked by PT 43 are:

1. Frequency harmonisation
Are the current, licence-exempt, frequency bands/powers/duty-cycles satisfactory or inadequate?

If inadequate, what changes would you want to see? For example, broader bands, more VHF spectrum etc.

2. Regulations
CEPT/ERC recommendation 70-03 is the 'handbook' for the SRD industry in Europe. Is it too complicated – should it be more generic?

> *"Are the current, licence-exempt, frequency bands/powers/duty-cycles satisfactory or inadequate?"*

Individual EU member states still have their own regulations. Is this right? What should be done to simplify procedures?

Three organisations have been requested to collect the views of the industry. EICTA, ETSI and LPRA and all three welcome input. Of these, the LPRA (info@lpra.org) welcomes views from all comers, not only its members. Please contact Karen Braem if you want to use the LPRA route.

LPRA will also be staging its "Radio Solutions" conference at the ETSI HQ near Nice on 12/13 October 2005. The conference this year is devoted to the PT 43 objectives.

Speakers from many sectors of the Short Range Device Industry, manufacturers and users, will present papers aimed at the influencing the form of the new strategy after an introduction to the mandate from an EC speaker.

If you have any strong views on the future for SRDs in Europe, PT 43 is your one chance to get that right – don't miss it.

EICTA – European Information and Communications Technology Industry Association (www.eicta.org).

ETSI – European Telecommunications Standards Institute (www.etsi.org).

The LPRA (Low Power Radio Association) is a European trade body that represents manufacturers and users of short range devices (SRDs).

It is active in the production of SRD Radio standards and regulations.

Mike Brookes is LPRA's chairman.

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www.ntius.com and www.element5.com

James Bond would be envious of this jacket that offers integrated electronic devices with controls made of fabric. Ski gear supplier Spyder has already launched it with an integrated music and photo iPod, but mobile phones - and even PDAs - can always be added to the range at a later stage. The jacket's sci-fi capabilities have been enabled by Eleksen's patented conductive fabric touch-pad technology, called ElexTex. It transforms a mere sleeve into an electronic control panel, which also remains waterproof.

Available in shops from September for around $2850

Torches are the next household essential to be given the contemporary look. The Ixion from the Tango Group combines an ultra-bright LED light beam with a cool design. The Ixion is a sealed unit making it waterproof. A magnetic switch set in a sculpted groove operates a completely contained solid-state system, which illuminates the ultra bright LED and lens array at the end of its slender body. Ixion is powered contactlessly via an induction base. The device's operating life is 10 hours.

Available from the Tango Group, at 0870 6091541 or sales@tangogroup.net

Had enough of lugging your bags around? Power Assistance is set to change that. With its pan wheel motors and ingenious engineering, it has made power-assisted luggage a reality. The DC motors and electronics are fitted into the wheels to optimise weight. It's powered by rechargeable lithium-ion cells, which offer a continuous 1.5 hours in a worst-case scenario - or up a hill. The rechargeable battery pack can go up to 2.5 miles between charges.

The motor, which has no switches but a pressure transducer in the handle, is activated when the Anti Gravity handle is pulled out.

In one, the design is light, strong and reliable.

Available from November this year, prices start from £397

www.liveluggage.com

Water level indicating alarm

Here is a low cost circuit to give an alarm when the water has reached the desired level in a tank. The different levels of water can be set using a knob provided with a scale. A pivot, which is easily available in the market, operates this device.

The block diagram of the unit in **Figure 1** depicts the mechanical arrangement required for rotating the potentiometer knob P2. The rise in water level forces the pivot to rise upwards, which in turn rotates the potentiometer.

As depicted by the circuit's block diagram in **Figure 2**, there are two potentiometers – P1 and P2 – connected in parallel to a 5V supply. The outputs of these two potentiometers are connected to the inverting and non-inverting terminals of the operational amplifier UA741. The output of the op-amp is connected to a transistor BC547 that inverts its input. The alarm is driven by this inverted output, which is about 12V. The detailed circuit diagram is shown in **Figure 3**.

Initially, the different voltages across the potentiometer P2 for different levels of water are noted down by practical observations while setting the potentiometer P1 at any arbitrary point. Then, a scale is prepared so that it indicates different voltages across potentiometer P2 for different levels of water. This scale is used to set the desired level of water at the potentiometer P1.This makes the voltage across it equal to the voltage across the potentiometer P2 when the water is at the desired level.

The working of the circuit is as follows. When the water rises up, the voltage across potentiometer P2 keeps increasing and when the water has reached the required level, the voltage across the potentiometer P2 becomes equal to the voltage across potentiometer P1. This is because the voltage level of the potentiometer P1 is set in accordance with the scale, which gives the voltage across the potentiometer P2 when the water is at the required level. These equal voltages, which are the inputs to the op-amp UA741, make its output zero. The zero output of the op-amp is inverted to a high voltage of 12V, which powers the alarm connected at the output of the inverting transistor.

This circuit drives a 12V alarm but, if an alarm of a higher voltage is to be used, we can use relays at the output to drive them.

The circuit can be used not just in a tank but also in other water storage systems like dams, for example. Unlike any other circuit, this circuit can be used for other types of liquids, such as petroleum, benzene etc, as well as water.

N.C.Karunya
Hyderabad, India

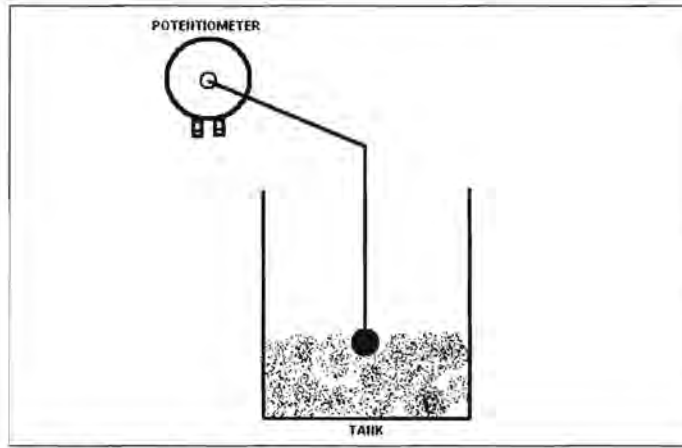


Figure 1: Mechanical arrangement (pivot)

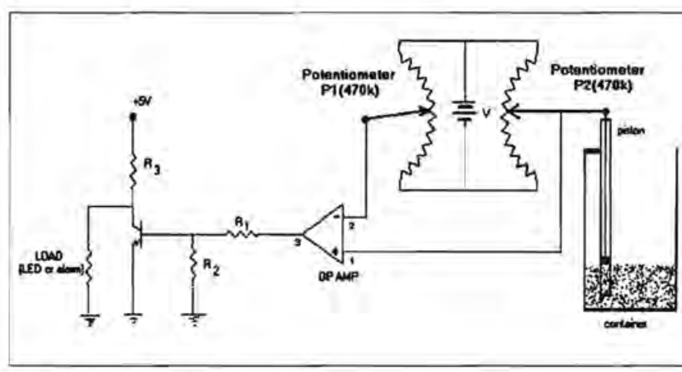
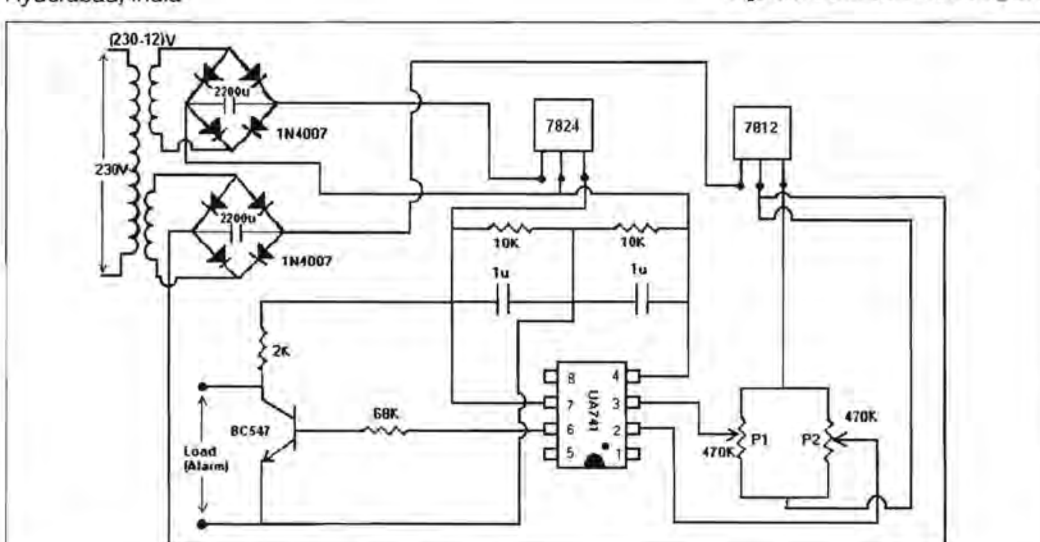
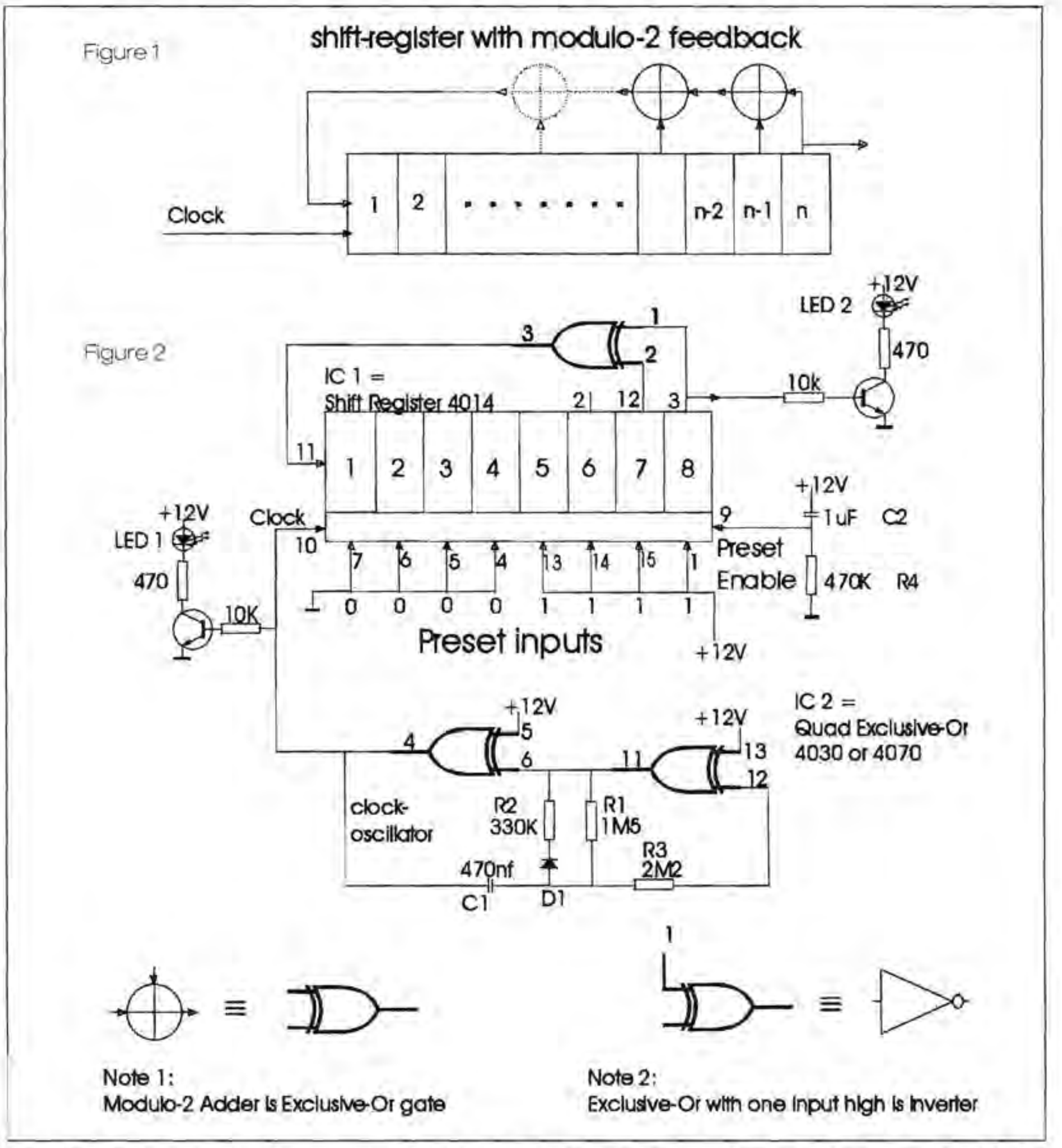


Figure 2: Block diagram

Figure 3: Detailed circuit diagram



Random flasher in crime fighting



Thomas Scarborough's Random LED Flasher (Circuit Ideas, EW, March 2004) had indeed this menacing mutant character that makes it useful for crime prevention. Alarm systems such as in cars usually show just the steady fixed frequency flash, which only indicates its 'on' condition. An additional random flasher suggests that several safety functions are sequentially being checked. It may discourage prospective car breakers.

Apparently, random series of pulses can be generated with a shift register with modulo-2 feedback, as shown in **Figure 1**. The outputs of two or more bits are combined with modulo-2 adders or Exclusive-Or gates. Bit n must be included. The output of bit n produces a series of ones and zeroes known as Digital Pseudo Random Noise. (Pseudo, because the series repeats after many clock pulses.) The n-bit word in the register steps through a number of different states. An n-bit register can be in 2n different states. With a proper choice of bits to take part in the feedback, the register steps through 2n-1 states, as the state with all zeroes is excluded. (If the register was in a state with all zeroes 000...0000, then the mod-2 adders would produce a zero to the shift input and leave the register in that state forever). This longest possible series of ones and zeroes from output n is called a Maximum Length Series.

Practical setup

The circuit diagram in **Figure 2** shows a practical setup with two CMOS ICs: IC1 is the 8-bit shift register 4014 and IC2 is a Quad Exclusive-Or 4030 or 4070.

Two gates in IC2 function as clock oscillator with approximately 1Hz frequency, also driving LED 1 with the well-known predictable flash-flash-flash. Its frequency is mainly determined by R1 and C1. D1 and R2 give the waveform approximately 20% duty-cycle.

The preset function is used to prevent the 00000000 state, which might otherwise occur at power-up. The preset inputs are connected to ground and plus supply in a random way, including at least one "1". Here, the choice of the connections had been dictated by the PCB layout. At power-up C2 keeps the PE (Preset-Enable) input high during approximately half a second to preset the register contents at 00001111, after which the shifting process takes over.

The output signal from bit 8 (pin 3) of IC1 is fed to LED2 via a transistor.

An 8-bit shift register could have 255 states. The 4014, however, has only output pins available for bits 6, 7 and 8. With these, a series length of no more than 63 states can be obtained with modulo-2 adder feedback from bits 7 and 8. As the series starts to repeat after 63 clock pulses or approximately 1 minute, this is more than enough to make LED 2 look like flashing in a totally random way.

Mount the two LEDs side by side in your car's instrument panel and hope for the burglar to move away.

Note: The PCB design is available on request.

Jaap Verrij
Drachten
The Netherlands

Voltage controlled current switch with short circuit protection

This invention is directed to current switches and, in particular, to current switches for batteries. In order to extend the life of rechargeable lead acid storage batteries, it is important that they are switched off if their operating voltage drops below a predetermined level. It is equally important that they are switched off when the load current is higher than a predetermined design value, due to a short circuit or some other adverse condition.

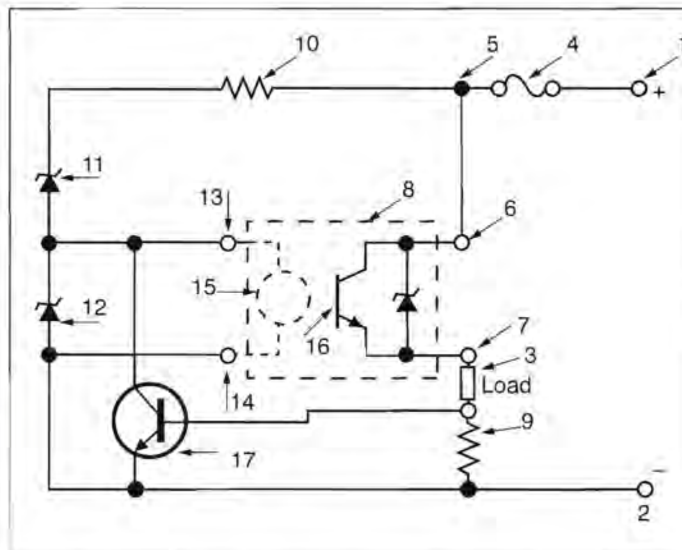
A large number of circuits have been developed for use with batteries to monitor and control their charging and discharging cycles. Among these are US Pat. No. 3,543,043 that was issued to D.L. Dunn on November 24, 1970, and which describes a battery protection circuit that includes a power transistor between the battery and the load. US Pat. No. 6,576,488 was issued to W.J. Zug et al on April 27, 1971, and describes a battery discharge monitor for industrial trucks. US Pat. No. 4,086,525 was issued to O. N. Ibsen et al on April 25, 1981, and describes a circuit that senses the rate of discharge and determines a safe discharge voltage for a battery. US Pat. No. 4,280,097 was issued to R.L. Carey et al on July 21, 1981, and describes a system for monitoring the DC voltage of a source while electrically isolated from it.

These systems, though useful for particular applications, do not have all of the attributes desired in a current switch and include a simple control circuitry, a low quiescent power dissipation, a low "on" resistance of the switch i.e. less than 0.25Ω from half to full load, a low value between "on-off" load voltages, i.e. <2.5V, a high speed short circuit protection of the switch and an electrical isolation between load and control circuitry.

Summary of the invention

It is therefore an object of this invention to provide a voltage controlled current switch having overcurrent and undervoltage protection for a battery. This and other objects are provided in a battery switch and undervoltage and overcurrent protection. The switch includes an opto-isolated switch with a pair of input signal terminals and a pair of power terminals.

The power terminals are connected in series with the battery, a current sensing resistor and a load. The pair of avalanche breakdown diodes are reverse-connected in series across the battery. The input signal terminals of the opto-switch are connected across one of the diodes to close the opto-isolated switch, when they battery voltage is above a predetermined value, and to open the opto-switch, when the voltage falls below this value. A further switch senses the current in the series battery-load circuit. This current-sensing switch is connected across the input signal terminals to open the opto-isolated switch, when the sensed current is above a predetermined value. The sensing switch includes the current sensing resistor in the battery-load circuit and a transistor with its base connected to the resistor and its emitter-collector connected across the input signal terminals.



Description of the drawings

The figure illustrates the battery current switch in accordance with the present invention. Terminals 1 and 2 represent the positive and negative terminals, respectively, of the battery to be controlled. The load 3 is to be connected across the battery terminals 1 and 2, and, conventionally, it is connected in series with fuse 4 and a manual switch 5. In addition, in accordance with the present invention, the power terminals 6, 7 of an opto-isolated switch 8 and a predetermined low value resistor 9 are also connected in series with the load 3 between the battery terminals 1 and 2. The opto-isolated switch 8 could the photoisolated, solid state, power relay type, manufactured by International Rectifier.

The control circuit for the opto-isolation switch 8 includes a second resistor 10 in series with two reverse-connected avalanche breakdown or Zener diodes 11 and 12. This control circuit is connected across the series power circuit, excluding the fuse 4 and the manual switch 5. The voltage across the second diode 12 is connected to the signal input terminals 13 and 14 of the opto-isolated switch 8, which are terminals for the LED 15 in the switch. The LED 15 controls the optical responsive power transistor 16 in the switch 8. A transistor 17 is connected across terminals 13 and 14 of the switch 8, and the emitter-base terminals of the transistor 17 are connected across the resistor 9.

Diodes 11 and 12 are selected so that the sum of their breakdown voltages is the minimum voltage required to provide the full load current by the battery. When the battery load voltage drops below the predetermined value, the current to the LED 15 input of the opto-switch 8 is cut-off by the diode 11 and the opto-switch 8 is de-energised. Access to the battery is thus switched off when the voltage is undesirably low.

In addition, resistor 9 produces a voltage at the base of transistor 17 that is proportional to the current through it. When the load current is undesirably high, the voltage across resistor 9 triggers transistor 17, which shorts out the input terminals to the opto-switch 8 thereby opening the opto-switch 8 to protect the battery. A continuous undesirably high load current will activate the fuse 4. For faster action, a circuit breaker may replace fuse 4.

For a standard 12V lead-acid battery, a circuit having the following component values provided protection for voltage below ~10.58V, and for currents above ~5.5A:

Opto-isolated switch (8) S430 (Crydom-IR)
Transistor (17) 2N 2219
Resistor (9) 0.1W/3W
Resistor (10) 120W ±5% /W
Diode (11) Zener V =5.6V
Diode (12) V =3.3V

Many modifications in the above described embodiments of the invention can be carried out without departing from scope thereof and, therefore, the scope of the present invention is intended to be limited only by the following claims.

I claim:

1. A current source switch for undervoltage and overcurrent protection in combination a circuit having a source and a load comprising:

➢ Opto-isolated switch means having a pair of input signal terminals and a pair of power terminals, where the pair of power terminals is connected in series with the current source and the load;

➢ A pair of avalanche breakdown diodes reverse connected in series across the current source, the input signal terminals being connected across one of the 10 diodes to close the opto-isolated switch means when the current source voltage is above a predetermined value; and

➢ Switch means for sensing the current in the series current source-load circuit, the sensing switch means being connected across the input signal terminals to open the opto-isolated switch means, when the sensed current is above a predetermined value.

2. A current source switch as claimed in 1, where the sensing switch means includes resistor means in the current source-load circuit and a transistor having a base circuit connected across the resistor means and an emitter-collector connected across the input signal terminals, whereby voltage developed across the current sensing resistor switches the transistor when the load current exceeds the predetermined value.

Uses

This circuit can be used as an adjustable (series-parallel) voltage-current DC power switch for DC to AC inverters, electrical cars etc.

John Ayer
Canada

Linux version of Spice

Here's a Linux version of a Spice circuit emulator. Spice is available as a free download, but I found spice 3f4 on my Suse Linux CDs. It requires { linux and } gnuplot to be installed, and I use Slackware. Having installed it rpm – recompile spice.spm, I found it a bit daunting, but did find that I needed an operational amplifier.

A .cir file is made by drawing the circuit and adding in unique node numbers on circuit connections

```
"              r3
"           +-ww-+
"       r1  |    |
"   2—ww-4-|\___5_
"   1—ww-3-|/
"       r2
```

and creating an ascii file from this {see example}. This 709 has five pins, that's just the way I made it.

```
" +in -in +v -v out
" 1  2  8 9 16 {these nodes are internal to the sub-circuit}
```

The plot uses gnuplot, and the results depend on the input info being in the file. { man spice }

.ac oct 12 20 20000 Freq response

.dc vin -0.04 0.04 0.001 or transfer char

To try it, type:

```
spice3 name.cir
run
plot ( log(v(5)/v(1)) ) # or as required
plot ( v(5)/v(1) )
quit
```

I hope this may be of some use or help.

Example:

```
* op-amp oscillator (c)jdg 12/03 ; run plot v(4) v(9)
*
.tran 1000ns 100000ns
*
v1 vpp 0-15V
v2 vmm 0 -15V
*
Ru 0 1 5k
R1 1 2 5k
R2 3 8 10k
X1 2 3 vpp vmm 4 oa709
C2 3 4 1000pf
*
R4 6 0 10k
R3 4 5 20k
X2 5 6 vpp vmm 9 oa709
R5 5 8 20k
R6 9 8 1k
R7 8 0 500
C3 8 0 500pf
*
* oa709 - - +in -in +v -v op
.subckt oa709 1  2  8  9  16
Q1 3 1 5 qp
R1 9 3 30k
C1 9 3 20pf
C2 9 4 20pf
R2 9 4 30k
Q2 4 2 5 qp
R3 9 6 80k
Q3 5 6 7 qp
Q4 6 7 8 qp
R4 7 8 5000
R5 9 10 10k
Q5 11 4 10 qn
Q6 12 3 10 qn
Q7 12 12 13 qp
Q8 14 14 13 qn
Q9 14 11 15 qp
R6 8 15 1200
R7 8 17 800
Q10 11 11 17 qp
Q11 19 12 16 qp
R8 8 18 22
R9 9 19 22
Q12 18 14 16 qn
.model qp pnp(bf=400 rb=80 ccs=1pf tf=0.2ns tr=5ns cje=1pf cjc=1pf va=50)
.model qn npn(bf=400 rb=80 ccs=1pf tf=0.2ns tr=5ns cje=1pf cjc=1pf va=50)
.ends oa709
.end
```

John David Gray
London
UK

There's more life in fuel rods yet

The letter ["Invisible breed"] by Bryce Kearey in the July 2005 issue of Electronics World magazine [p47] brought up the safe use of nuclear power. Recently, I was at a symposium where Dr. Claudio Filippone presented his work on the CAESAR project at the University of Maryland, US (www.caesar.umd.edu).

He has developed a process that uses steam as the moderator for the nuclear chain reaction in a power reactor. This has several good results. Fuel rods that no longer work, because the uranium 235 has been spent, can now be used many more years until the uranium 238 (98% of the rod) has been converted into nuclear waste. A side advantage is that by using the steam moderator correctly, the spent rods will not have any plutonium left.

Dr. Filippone is currently trying to get $2m dollars and a test reactor to run a proof-of-concept test. Governments and companies that create the nuclear fuel do not seem to be interested in using up all the old fuel rods, which now sit at every nuclear power plant.

Thomas Flink
US

What a spin

From quantum mechanics, electrons have a magnetic moment and a spin angular momentum of s = half a quantum spin unit (Planck's constant, h divided by twice pi).

If the stationary electron spins at light speed as implied by electric energy transfer speed (Electronics World, April 03), then s = mcr, where r is the spin radius. So, r = 10^{-13} m. The model of electron as the negative electric field half of a gamma ray discussed in March 05 letters (the full ray is half negative and half positive like a sine wave) implies that gravity confines the energy in a loop of black hole radius (Electronics World, August 02), R = 2GM/c2.

Since force is energy per unit distance moved, the strong force that causes pair production divided by the gravity force proportional to r/R. The electron spin radius is therefore larger than the electron loop core by a factor similar to the ratio of the strong force to the gravitational force (Electronics World, April 03).

The continuous motion of non-periodic energy in an electron along its electric field lines is the mechanism by which the central core of the electron influences – and is influenced by – the outside.

These facts are not speculative as all are established on strong experimental evidence. It does not conflict with the mainstream model for an electron is an unexplained core surrounded by virtual particles that affect the spin and partly shield the core.

Nigel Cook
UK

When a jolt it's a jolt

There are many product claims that go unchallenged – perhaps, through public ignorance.

Often such claims come about through the enthusiastic ignorance of marketing departments but these claims should not get reproduced in journals that should know better.

My offering is the claim repeated in the New Scientist where the Taser is described as causing a "debilitating 50,000V jolt".

Assuming a bulk body resistance of 10000Ω, if there was really a 50kV "jolt", this would give rise to a current through the body of 5A – clearly more detonating than debilitating.

The reality probably is that the Taser generates a potential of 50000V to break down air resistance through clothing etc. It may be assumed that it is limited in its capability to supply current such that the "jolt" produced would be sufficient to give rise to a body current of 50mA, any more would cause ventricular fibrillation in some and could be fatal if continued.

Once the current flow is established, 50mA would only give rise to a "jolt" of 500V across the body.

Douglas Dwyer
UK

Shorter and easier to handle

I found Reza Moghimi's article "Signal conditioning for optimum noise performance" in the July 2005 issue of Electronics World, page 28-31, very interesting and informative. Nevertheless, one always can find things that can be improved. In this case, the suggested improvement would make Equation 1 on page 29 shorter and easier to handle: two terms of that equation could be cut down to one new term, which looks as follows:

$$4kTR1*\left[\frac{R2}{R1+R2}\right]^2+4kTR2*\left[\frac{R1}{R1+R2}\right]^2=4kT*\left[\frac{R1*R2}{R1+R2}\right]$$

Explanation: The resulting input referred noise voltage of the feedback resistor network R1 and R2 is nothing else but the noise voltage of these two resistors in a parallel configuration. If you divide the output referred noise voltage of (R2*In-) by the noise gain G = (1+R2/R1) then you'll end up with the input referred noise voltage [In-*(R1*R2/(R1+R2))].

It is self-evident to check if the parallel configuration of R1 and R2 might as well play a role in the calculation of the Johnson noise voltage for the two resistors. It does! Summing up the noise voltages of R1 and R2 after they passed through the R1-R2 voltage-divider arrangement at the (-) input of the op-amp will mathematically end up with the short term at the right side of the above shown formula.

Burkhard Vogel
Germany

Batteries for Portable Devices

Gianfranco Pistoia

Elsevier

This book give a broad overview on battery systems for portable electric and electronic devices, featuring all battery systems currently in use and majoring on those most appropriate for portable electronics. Extensive details are given on the chemistry of each cell-type featured, the materials used, the cell construction and the performance of the systems and their appropriate applications. Examples are given of current, commercially available batteries, along with the devices they are typically used for. Additionally, the book gives useful safety guidance on each cell type and extensive information on charging systems.

Unusually for a book on battery systems, the author also includes chapters on small fuel cells and supercapacitors, with tips on how these can be combined with the previously discussed battery systems to enhance performance. Additional chapters deal with the difficult issue of 'spent battery collection and recycling' and general trends in the world battery market. Extensive appendices and references are provided for anyone who wishes to take their research further.

Chapter 1: Basic battery concepts:
How cells work chemically, typical construction of cells and their assembly into batteries.

Chapter 2 : Characteristics of batteries for portable devices:
Different battery systems currently available and their characteristics considered for portable device use.

Chapter 3: Battery standards and sizes:
IEC designation explained

Chapter 4: Primary Batteries:
Zinc-carbon, zinc-chloride, alkaline-manganese, zinc/silver-oxide, zinc/air and numerous lithium chemistries are explored.

Chapter 5: Rechargeable batteries:
Lead-acid, nickel-cadmium, nickel-metal hydride, alkaline and lithium devices are extensively examined.

Chapter 6: Batteries for medical and special applications:
Zinc-mercury, zinc-silver oxide, zinc-air and numerous lithium systems are considered and some typical uses given.

Chapter 7: Battery safety, management and charging:
Correct handling and storage, mechanical and thermal safety systems, electronic battery control, 'smart' batteries, examples of commercially available chargers, also test and certification schemes.

Chapter 8: Energy sources supporting or substituting batteries:
Small/miniature fuel cells and small supercapacitors are discussed, along with how they might be used together with battery systems to best effect.

Chapter 9: Spent battery collection and recycling:
Full life cycle from manufacture to recycling is considered, along with human health considerations of the toxic materials used in battery manufacture. Different recycling schemes are discussed, along with regulatory issues in the US and EU.

Chapter 10: World battery market:
General trends of the past two decades are revised.

For any chemist requiring a background on modern battery systems this book would, no doubt, be a useful starting point. As a non-chemist, I found the constant use of chemical abbreviations (e.g. $LiMn2O4$) made a difficult read, even though I understand the use of the symbols. However, you can skip most of the chemical details and concentrate on the overall discussion to understand which battery system might help with your specific application.

Whilst not exactly 'bedtime reading' material, Gianfranco Pistoia's book comprehensively covers the 'state of the art' today. Chapter 9, especially, should be mandatory reading for anyone considering the problem of discarded batteries. (Did you know that around one million tonnes of batteries are produced per year in the EU alone? And guess where most of them end up?)

Graham J. Field

Lead-free assembly for miniature optical encoders

Agilent Technologies introduced a series of reflective optical encoders in a lead-free surface-mount assembly. The new devices replace the popular Agilent HEDR-8000 series in SO-8 packaging.

Their small size, which is 6.2x4.4mm, with a choice of 3.2 or 2.7mm height, makes them one of the smallest reflective encoders around. The Agilent AEDR-8000 series reflective encoders feature an LED light source, a special photodetector IC with integrated electronics and integrated optics. They can be used with a reflective code wheel to sense rotary position and velocity, or with a linear code strip. The devices offer either one or two-channel TTL-compatible digital outputs in quadrature, which provides both count and direction information.

They are available with encoding resolutions of 7.09 lines per mm, 5.91 lines per mm, 2.95 lines per mm and 1.42 lines per mm. They are insensitive to axial play and maintain performance and accuracy over a wide variation in the gap between sensor and code wheel or strip. The encoders operate at rated performance for frequencies of up to 30kHz.

www.agilent.com

PMB MX solution to Sifam's masterbatch requirement

Sifam produces customised and colour coded knobs and push-buttons among other products. Control knobs are injection moulded, using a number of different polymers. Colour-coding is used for fast, accurate identification in complex equipment, so ensuring a consistent colour match is critical. Sifam needed a supplier with a universal carrier that could provide consistent colour quality in small injection moulding using different polymers, so it joined forces with PMB in 2003.

PMB developed the MX carrier for 0.3mm sheet applications where any inconsistency in the distribution of colour will result in a streaky or shaded appearance. This technology was equally applicable to injection moulding of small components.

"PMB's MX carrier blends very well even in the small quantities we require for moulding control knobs. The result, when seen on a professional sound mixing desk with hundreds of knobs, displays no colour variability at all," said Wayne Shaw, purchasing manager at Sifam.

Sifam has a library of approximately 75 masterbatch colours. To date, PMB has colour-matched 42 colours to re-stock. A number of colours have also been re-matched to allow Sifam to dispose of stock containing lead and cadmium based pigments.

www.sifam.com
www.pmb.co.uk

Four-channel, 12-bit resolution PC oscilloscope

Pico Technology has announced the immediate availability of its new PicoScope 3424 PC oscilloscope. The four-channel oscilloscope has 12-bit resolution, 20MS/s sampling rate and a 512k memory buffer. The addition of a USB 2.0 connection makes connecting and installing the oscilloscope easy and enables rapid display updates. The USB 2.0 interface also powers the unit, eliminating the need for an external power supply.

The large memory buffer allows long-duration signals to be captured at its top sampling speed of 20MS/s. It offers 1% voltage accuracy and 100ppm timebase accuracy. Timebases from 500ns/div to 50s/div and voltage ranges from +/- 20mV to +/- 20V make it suitable for a wide range of applications, including general analogue, audio and digital design and repair. With its 12-bit resolution, the oscilloscope produces high-quality waveforms that can be vertically zoomed to reveal even higher levels of detail. This resolution gives the instrument a 72dB dynamic range, which enables it to detect low-level harmonics when used in spectrum analyser mode, for applications such as noise and vibration analysis.

www.picotech.com

White LED driver IC offers protection

Toshiba Electronics Europe has announced a new IC for driving white LEDs used to backlight LCD panels in mobile phones, PDAs, portable gaming equipment and other mobile devices. Designed to provide precise brightness control and to minimise external component count, the TB62737FUG white LED driver IC incorporates an over-voltage protection function and operates at a high efficiency to maximise battery life.

Toshiba has engineered the device to provide an optimum combination of over-voltage protection, high-precision current regulation and high efficiency. This optimised design reduces total circuit size and helps engineers to minimise the form-factor of their portable system.

The TB62737FUG incorporates an over-voltage detection pin that minimises the need for external components by enabling protection against over-voltage conditions such as those caused by an open LED. At 87%, the device's operating efficiency is 2% higher than that of previous products, facilitating longer rechargeable battery life. A guaranteed, high-precision current regulation of ±5% suppresses white LED brightness fluctuation to ensure exact control of backlight brightness.

www.toshiba-components.com

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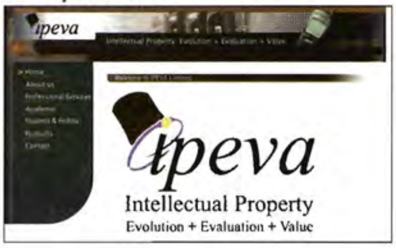

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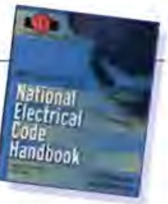

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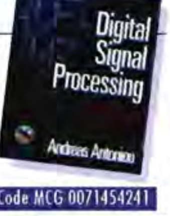

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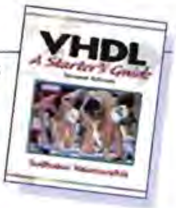
By Sudhakar Yalamanchili



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