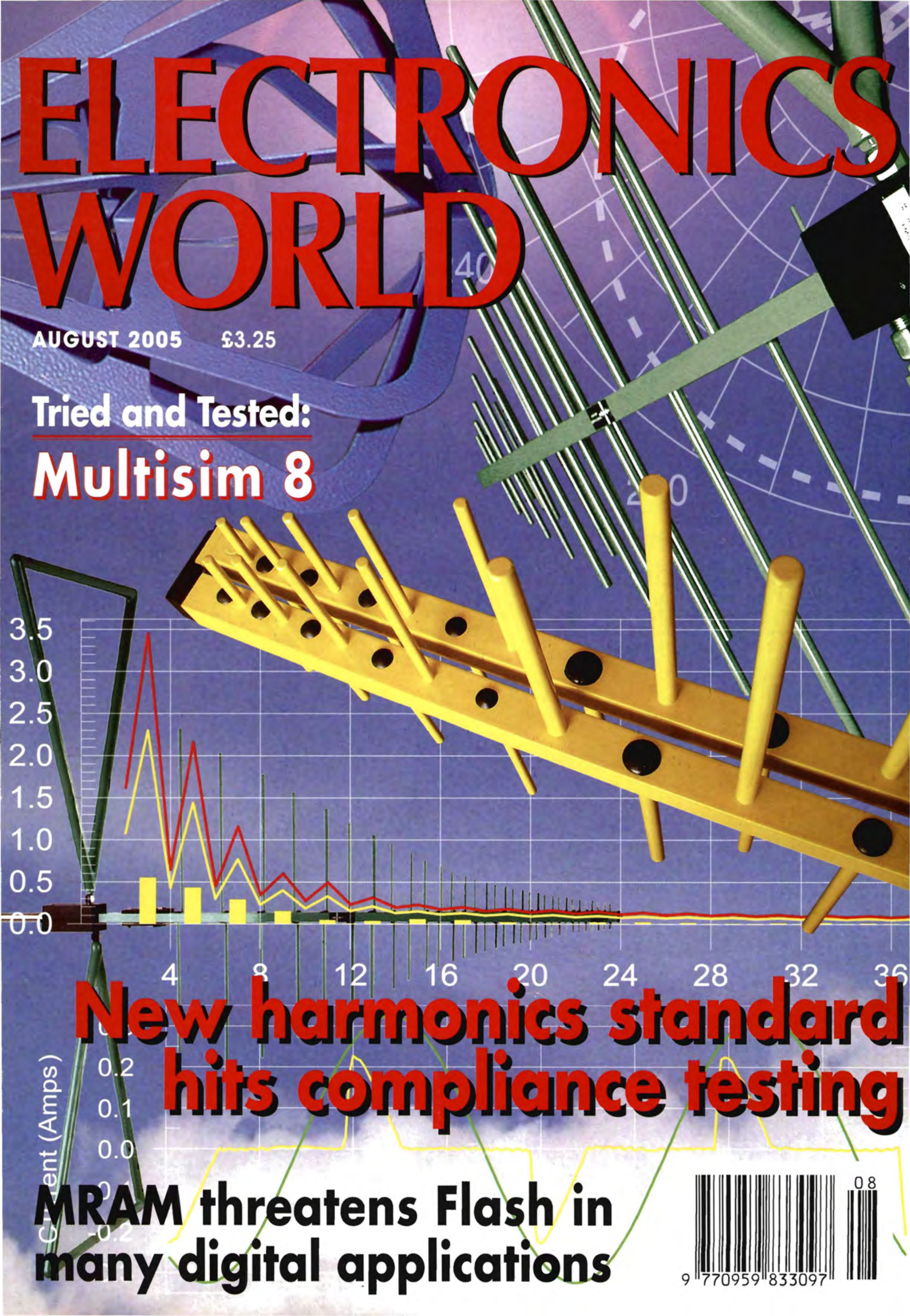
ELECTRONICS WORLD

AUGUST 2005 £3.25



Tried and Tested: Multisim 8

New harmonics standard hits compliance testing

MRAM threatens Flash in many digital applications

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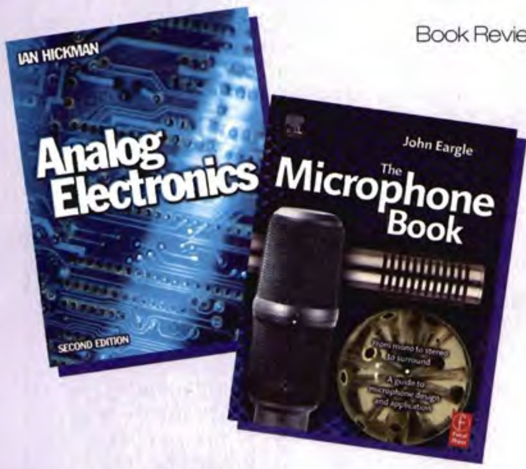

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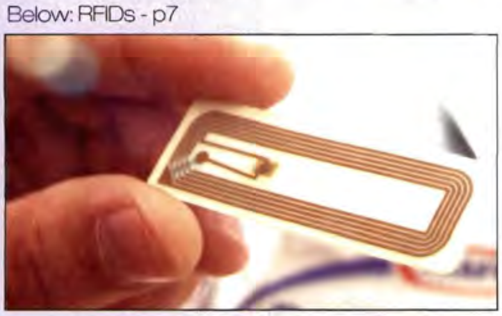

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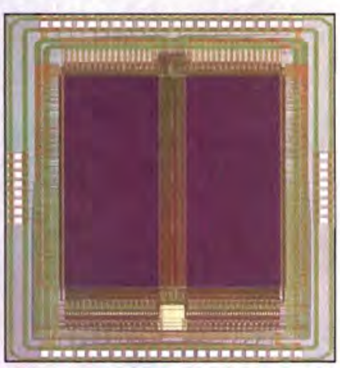

Competition

Win a Microchip PICSTART Plus programmer – p44

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Front cover image supplied courtesy of Schaffner

Book reviewing – *it could not be simpler*

Our recent initiative for technical book reviewing has taken off to the point that book publishers keep sending us more books! So, here, you will find an even longer list of books for grabs. All you'll need to do is select a favourite, write us a short review and you get to keep the book.

We already have reviewers that come from all corners of the world – Australia, The Netherlands, the UK, Belgium, Canada and others. Thank you to all of those readers who subscribed to our idea of reviewing books for Electronics World, but I'd like to emphasise that the invitation is open to all readers interested in reviewing technical books.

At present, we have the following selection waiting to be reviewed. Please call us or email us to leave your details if you would like to participate too.

Svetlana Josifovska
Editor

Robots
Daniel Ichbiah

Video Demystified (4th edition)
Keith Jack

Recording Tips for Engineers
Tim Crich

Building Valve Amplifiers
Morgan Jones

PC-based Instrumentation and Control (3rd edition)
Mike Tooley

Short-range Wireless Communication (2nd edition)
Alan Bensky

Networking and Internetworking with Microcontrollers
Fred Eady

Demystifying Switching Power Supplies
Raymond A. Mack, Jr.

Beebop to the Boolean Boogie (2nd edition)
Clive Maxfield

The Digital Consumer Technology Handbook
Amit Dhir

The design Warrior's Guide to FPGAs
Clive Maxfield

Designing Autonomous Mobile Robots
John M. Holland

Op-amp Applications Handbook Analog Devices,
edited by Walt Jung

Op Amps for Everyone (2nd edition)
Ron Mancini

Introduction to AutoCAD 2005 2nd and 3rd design
Alf Yarwood

Embedded Systems Architecture
Tammy Noergaard

Building Interactive Worlds in 3D
Jean-Marc Gauthier

Advanced Systems Design with Java UML and MDA
Kevin Lano

User Interface Design and Evaluation
Stone, Jarrett, Woodroffe, Minocha

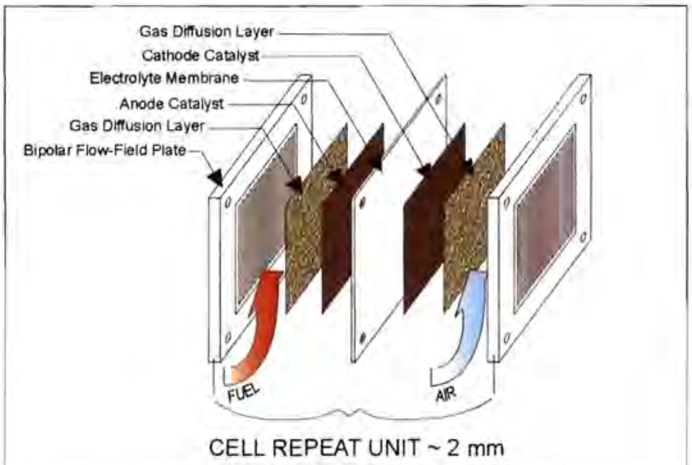
Practical Process Control for Engineers and Technicians
Wolfgang Altmann

EDITOR: Svetlana Josifovska **E-mail:** s.josifovska@highburybiz.com **EDITORIAL E-mail:** EWeditor@highburybiz.com
EDITORIAL ADMINISTRATION: +44 (0) 1322 611274 **E-mail:** EWadmin@highburybiz.com
PRODUCTION EDITOR/DESIGNER: Jane Massey **E-mail:** J.Massey@highburybiz.com
SUBSCRIPTIONS: Customer Interface Ltd, Cary Court, Somerton, TA11 7BR **Telephone:** 0870 4287950, **Fax:** 01458 271146
SUBSCRIPTION RATES: 1 year: £38.95 (UK); €95 (Europe); $125 US & worldwide
DISPLAY SALES EXECUTUVE: Reuben Gurunlian +44 (0) 1322 611261 • **SALES MANAGER:** Paul Monaf +44 (0) 1322 611262
PRODUCTION EXECUTIVE: Dean Turner +44 (0) 1322 611206 **E-mail:** d.turner@highburybiz.com
PRINTER: William Gibbons Ltd • **ORIGINATION:** Impress Repro A1 Parkway, Southgate Way, Orton Southgate, Peterborough, PE2 6YN
NEWSTRADE: Distributed bySeymour Distribution Ltd, 86 Newman St, London W1T 3EX. • **PUBLISHING DIRECTOR:** Tony Greville
If you are experiencing problems getting copies through your newsagent, please call Debbie Jenner on +44 (0) 1322 611210

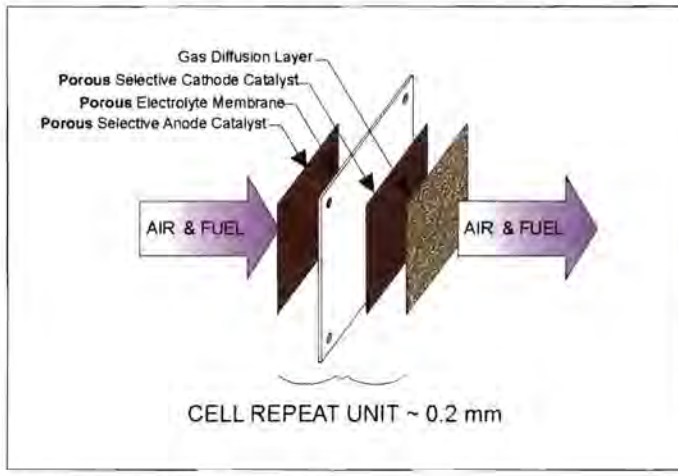
ISSN 0959-8332

Electronics World is published monthly by **Nexus Media Communications, Media House, Azalea Drive, Swanley, Kent, BR8 8HU** Nexus Media Communications is a trading name of Highbury Business Communications Limited, a subsiduary of Nexus Holdings Limited. Registered in England. Registered Number 5346404. Registered Office: Hanover House, 14 Hanover Square, London W1S 1HP

New fuel cell does not give batteries room for manoeuvre



CMR's new fuel cell structure



Conventional fuel cell technology

Conventional battery technologies' days are numbered, says a small British firm that invented a new fuel cell stack structure. CMR Fuel Cell from Cambridge has departed from the full-plate membrane structure that lies at the heart of a fuel cell, in favour of a perforated membrane that conducts the air-fuel mixture through the structure itself. In conventional fuel cells, the electrolyte membrane acts as a physical barrier between the fuel and the air/oxygen. A catalyst layer at the anode oxidises the fuel, while the cathode catalyst reduces the oxygen. The electrolyte and electrocatalyst layers are bonded together to form an impermeable membrane electrode assembly (MEA). Several such MEAs are assembled together with intermediary bipolar flow-field plates and gas-diffusion layers to form a fuel cell stack.

In CMR's novel Compact Mixed Reactant stack, the reactants are mixed first and then fed through a porous membrane, which makes the design thinner, lighter and cheaper. The fuel used is methanol.

This approach has reduced the size of the cell stack by a factor of ten, extended the fuel cell's runtime by a factor of four and made its assembly considerably easier and, hence, more cost-effective.

"Conventional battery technology has no room to develop into," said John Halfpenny, CMR's CEO and formerly of ARM. "We have the ability to create a totally solid state stack, making it robust and easy to fit in any application that requires a battery source."

This technology breakthrough now promises to acquire a big chunk of a $2bn-market expected to open up by 2010, considering that conventional battery technologies are running out of steam. Among the applications that CMR hopes to tap into are power tools, electric scooters, consumer portable systems and, eventually, even move into the automotive market.

Although the company demonstrated a working prototype last month, it is unlikely to begin volume manufacture of such cells sooner than 2008. "We've proven that the technology works, despite the incredulity of many," said Michael Priestnall, CMR's CTO and formerly of the Generics Group, "but there's a lot more work to do, such as optimising the system, having better engineered components, better supply relationships and so on."

CMR is VC-funded. It plans to manufacture these cells fablessly, but hopes to enter into strategic partnerships with interested parties.

One QuadraView offers four computer screens

Rose Electronics, the KVM (keyboard-video-mouse) solutions expert, is bringing a unique product to market in its quad display switch called QuadraView, says its general manager Giles Prewitt. "The QuadraView is not a typical product. If you take any KVM switch, an ordinary monitor and the QuadraView, you will have a split-screen into four sectors that you can work on at the same time. And for a direct link, such as a coax cable, there's no delay in what you see on the screen."

QuadraView is a quad display switch that allows any four of several connected KVM switches or computers to be viewed on the same screen simultaneously. Each sector can display VGA or DVI images from any source. A user can work on any of them by simply rolling the mouse across from one sector to another. This is particular useful in financial environments, such as stock floors for example, data centres, classrooms, industrial applications, receptions and others.

Staccato believes in its own UWB market success

UWB demonstration set-up

A two-year old start-up from San Diego, US, called Staccato Communications, claims will be the first firm to ship all-CMOS Ultra-Wide Band (UWB) chips in volumes. "Our single die solution will start sampling in Q3 this year, with volumes to follow in early 2006," said Eric Rosser, vice-president of sales of Americas and EMEA. "We already have partnerships with companies that are using our Ripcord development kit to create the [UWB] drivers."

Although SiGe and BiCMOS are seen to yield better performances in RF applications, Staccato has chosen CMOS to implement the UWB front-end in as this process technology advances faster, it is more widely available, it is much cheaper and it offers better wafer yields. Staccato's whole UWB offering includes the chip, the PHY, MAC, the crystal, the filters, transceiver switch and matching circuits. Per node implementation will cost less than $10 at connectivity of 480Mbps. Fujitsu will be fabricating these chips in its 110nm process.

However, the only place where UWB products could be shipped today is the US, where the FCC has already allocated spectrum to this standard. This is not the case in Europe, where UWB operating frequencies are close to the noise floor of the 3G spectrum, potentially interfering there, to the greatest chagrin of some mobile phone operators. It is believed that UWB will not be frequency-harmonised across the world, which might mean that Staccato and similar suppliers will have to ship different UWB chips to different markets.

"We can provide a chip that will offer low out-of-band power so that it does not interfere with other [wireless] standards," said Rosser. "By using a harder filter for the out-of-band and yet using the same radio technology – so providing [the solution at] low power and [at] wide frequencies – we can ship the same product everywhere."

In a separate announcement, the Bluetooth SIG has agreed to ship its next generation of products with an integrated UWB front-end.

New PoE standard for Cat 5

A new standard for Power over Ethernet (PoE) is being proposed that will allow motorised closed circuit TV cameras to be powered and controlled directly from Ethernet cables.

PoE technology is already well established for providing wireless networking access points without having to co-locate them with power sockets. Almost all wireless LAN providers have at least one line of access point with built in PoE and 90% of all enterprise-wide installations – particularly in places such as airports – use the technology, says Igal Rotem, chief executive of Israeli company PowerDsine that has set up a free certification programme for PoE designs.

The new standard would provide between 31W and 35W over the existing Category 5 data cables, compared to 15.4W over the same 42V-56V range today. This would allow cameras with pan, tilt and zoom to be powered, as well as biometric sensors.

A working group for the technology is due to be voted on in July, with an IEEE standard following in early 2008, he said.

Ian Pearson, the head of BT's futurology unit, says that emotions could be created for computers through chemical imbalances, similar to those created in the human brain. "If you were on an aeroplane that was more afraid of crashing than you, it would do everything to stay in the air until it was supposed to be on the ground," he said.

One application that is already being worked on in labs is an interface that will translate human senses into computer programmes. "You could link computer systems to shake hands or cuddle across a network," added BT's Pearson.

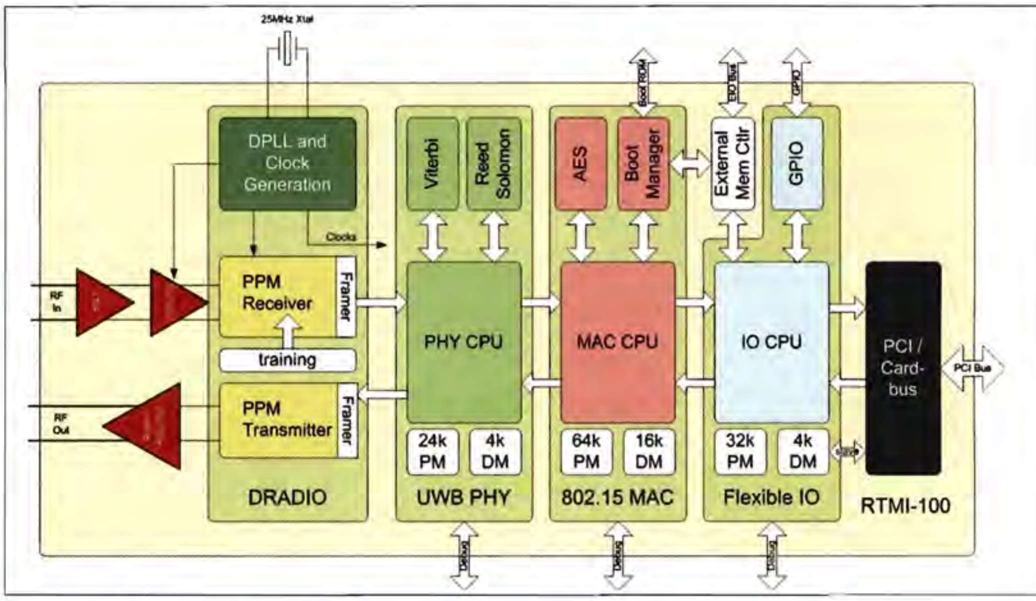
Ω

The development of the Semantic Grid is making nice progress toward seamless automation that will enable flexible collaborations and computations on a global scale, says Professor David De Roure of Southampton University. The Head of Grid and Pervasive Computing at the School of Electronics & Computer Science says that the Grid is a large-scale, self-managing, collaborative network. "Semantic Grid computing has allowed us to bring resources together to achieve something that was not previously possible. We now look forward to working on some of the remaining challenges, which include, for example, the intersection between the grid and the physical world through pervasive computing devices and the self-management, self-optimisation and self-healing, so-called 'autonomic' behaviour, necessary for large scale distributed computing.

Ω

Matsushita Electric (Panasonic) has developed VCSEL Laser with the world's highest data transmission rate. In addition, the optimisation of the device structure, employing current confinement by selective oxidation, has realised a low threshold current of 1mA and a high slope efficiency of 1.1W/A that is almost three times higher than the conventional value. This has resulted in a low operating current of 8mA for 12.5Gbps modulation. Panasonic aims to begin shipping the two types of surface emitting lasers (2.5Gbps and 12.5Gbps) in early 2006.

Artimi chip offers UWB and powerline connectivity



Artimi's RTMI-100 block diagram

Artimi, a fabless semiconductor company with R&D facility in Cambridge, has launched RTMI-100 – a single chip UWB mesh network device, capable of dual-mode wireless and powerline high-bandwidth multimedia transport. With an underlying 800Mbps transport and optional error correction and encryption, the RTMI-100 provides a flexible wireless or powerline connection between two or more multimedia devices.

The chip contains four main blocks that handle the radio (DRadio), the PHY, 802.15 MAC and the I/O interface. The main element of the DRadio section is a parallel DSP front-end, operating at over 2.4TOPs/s. The pulse position modulation (PPM) UWB receiver performs direct deconvolution of the radio channel, effectively acting as a Zero-IF PPM receiver. The PPM receiver is fed from an on-chip LNA and sampler, running at 10GHz. The PPM transmitter can send 200ps wide differential pulses, with a repetition rate of 200MHz. Pulse whitening circuitry built into the device ensures spectral compatibility with the FCC spectrum allocation for UWB devices.

The UWB PHY CPU is based on a 200MHz RISC engine. The CPU manages the DRadio block and co-ordinates the transmission and reception of UWB frames with or without the use of channel error correction, through the use of convolutional encoding/Viterbi decoding, interleaving and Reed Solomon block error correction. The third section is the MAC CPU, which is a dedicated 200MHz RISC engine that implements the 802.15.3 compliant MAC. This includes scanning and synchronisation, beaconing, stream mux/demux, contended and non-contended media access, piconet management, QoS control, security and power management. This CPU is also the boot master for the device and is responsible for loading the internal code memories from either serial or parallel external non-volatile memory.

The IO CPU is a third RISC CPU that manages the PCI interface and allows the device to control external PCI connected peripherals including Ethernet (10/100Mbit and Gbit). For larger applications, the IO CPU has access to the external memory bus, where it can access additional Flash and/or SRAM as required.

RTMI-100 requires very few external components. All that is required is a 25MHz crystal, connected to the internal crystal oscillator circuit, an additional LNA and TX/RX switch, controlled by the device, and an external non-volatile memory (either serial PROM or Flash ROM) to hold the device program. All internal firmware is developed by Artimi and is supplied with the device. The processors on the chip are license-free to reduce costs.

The chip is a combination of CMOS and SiGe.

Some 120 California-based companies have opened offices in the UK over the past few years, according to Think London, the official inward investment agency for London. Around 50% of these companies have selected London as their base, which makes this city one with the largest group of leading-edge companies in Europe, including names like Google, Yahoo and Apple. One in five California companies investing in London establishes a European headquarters operation here, with over than half locating sales and marketing offices
Over 75% of all California investments come from the IT and software sectors. Think London states that the economy, skilled talent pool and agile business environment attract California businesses to this city.

Ω

ITI Techmedia, the organisation that focuses on the Scottish economy, has announced a new R&D programme in which it will plough some £6.7m.
The programme will focus on ultra-wideband technology (UWB), which ITI Techmedia believes will be a source of major market opportunity in the next three to ten years. It is estimated that the global UWB market for consumer and computing applications could exceed $1.2bn by 2010, says ITI Techmedia.
The R&D programme will last two years and develop end-to-end UWB systems, including the hardware, software and mesh networking. Programme partners include TES Electronic Solutions, Elonics and Cambridge Consultants.

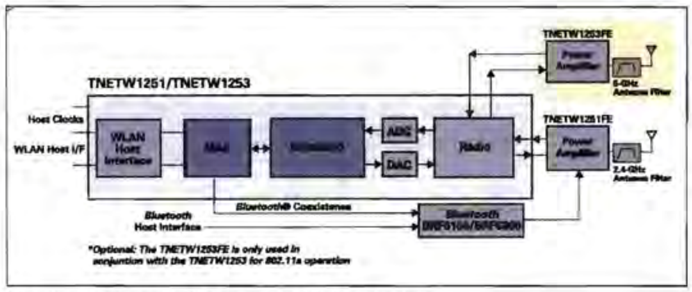
Ω

Nallatech and partners launched the FPGA High Performance Computing Alliance (FHPCA) last month to design and build a 64-node FPGA-based supercomputer, capable of achieving processing speeds in excess of 1Teraflop. The computer will be built using commercial off-the-shelf technology from alliance members. The new supercomputer will be owned and operated by Edinburgh Parallel Computing Centre at the University of Edinburgh. Currently, few standards exist to guide engineers developing FPGA-based computer systems, so, by collaborating in this development, the technology partners expect to be able to increase the interoperability and accessibility of their technology to engineers and scientists.

TI enables VoWLAN for mobile phones

Texas Instruments (TI) was showing its Voice over WLAN technology for use in mobile phones at this year's Wireless Connectivity show in London. There are two devices (TNETW1251 and TNETW1253) each providing a single-chip solution for VoWLAN, which is becoming increasingly important for WLAN usage. By incorporating this technology into a mobile phone, it will enable users to select the most cost-effective form of communication, whether via a cellular or Wi-Fi network or by using VoIP on the WLAN.

The chips, part of the WiLink 4.0 series, are fabricated using a 90nm CMOS process and TI's Digital RF Processor (DRP) technology to reduce the physical size (6x6mm BGA).



Block diagram of TI's new VoWLAN devices

The device consists of several circuit blocks. At the RF end of the chain is the radio that interfaces to a power amplifier for either 2.4GHz (TNETW1251 and 1253) or 5GHz (TNETW1253). Away from the antenna, the radio interfaces to ADC and DAC elements to provide the digital conversion. Thereafter, there is processing for the baseband signal. The MAC (Media Access Control) elements may also interface to external Bluetooth circuitry, allowing operation of the mobile phone on a variety of standards. The output from the MAC passes to the WLAN host interface circuitry and thence to other circuitry in the phone.

With the cellular industry moving swiftly toward a situation where a variety of wireless standards provide the optimal service for the user, ICs like those in the WiLink series such as the TNETW1251 and 1253 are likely to see an increasing level of use.

RFID not ready for shoppers' trolleys

RF scanning of trolleys full of groceries that will cut shoppers' queuing time to several seconds at the point of sale is unlikely to come to stores in the next five to eight years' time. This is despite RFID technology touted as being near-ready several years ago.

A chip containing an ID and an antenna would be attached to the grocery's packaging. However, the price of the chip has to drop to a tenth of a penny for such a system to be commercially viable.

Despite tag manufacturers, such as Texas Instruments and Intel using 130nm and below chip-manufacturing processes, which offer higher wafer yields and lower costs, it is claimed that the prices of RFID tags have not reached the desirable level yet. Tags at the moment cost between five and ten US cents (around 3p).


RFID chip

"Even with 90nm [chip making processes] the economics are not there yet. The physics [of the tag] is still not out-of-the-box," said Danny Edsall, Global Solution executive at IBM. "There are a lot of issues in terms of packaging: Do you embed the antenna into the substrate or etch it on top or even use magnetic resonant inks to print it on top? Then, there are issues with the efficiency of the tag readers and the business planning behind [the use of RFID technology]."

At the moment, RFID has only penetrated the busy warehouses of retailers such as Wal-Mart in the US and Tesco in the UK, and several shop-floor pilot schemes at Marks and Spenser's. But, even in the supply chain, there are issues with RFID, such as the correct placement of the tags, for example. "You don't want to place the tag over a bulk of material that absorbs RF," said Dr. Duncan McFarlane, research director at Auto-ID Labs.


Photo: Newscast

Nevertheless, Tesco will go RFID 'live' in 2300 back-end locations by the year-end and Wal-Mart will continue with the rollout of RFID in its stores in Europe and Canada. "The technology is making a difference," said Simon Langford of Wal-Mart. "On the positive side, there's no need for line of sight as with bar coding; identification and tracking of products in busy warehouses is a lot easier; and it's more accurate and robust than bar codes. But, on the negative side – especially in the food and drinks industry – there's the recyclability issue of RFID tags, especially their copper antennas."

Paxar, Bristol-based supplier of RFID tag antennas, is already experimenting with new technologies, such as the more environmentally friendly silver-based printable inks. "We'll introduce it in the next few years," said Pete Moylan, business development manager at Paxar.

SDR is good for the military but not commercial mobile phones

Software defined radio (SDR) will not fulfil its potential to take over the market for mobile phone base stations, says one of the major base station suppliers. Software defined radio (SDR) has been making significant progress in US military radio systems, where different 'personalities' of frequencies, demodulation schemes (based around frequency modulation) and message protocols can be loaded into a programmable FPGA in the radio.

However, there are significant problems with applying the technology to mobile phone base stations, says Hans Otto Scheck, principal engineer for Nokia Networks. "We are in the second cycle of industry hype in SDR," he said. "When all the fog disappears, we will get an improvement. But SDR is part of a trend, not a revolution. It is not a disruptive technology, as some people like to think, but it's an evolutionary one, and we have to take things step by step."

The military uses SDR.
[Photo: defenseimages.mod.uk]

Scheck points to significant technical and regulatory issues that hamper SDR's smooth progress into mobile phone base stations. "For each separate frequency band you need a separate filter – that's the point that is often overlooked," he said. "And how do you handle time domain modulation as well as frequency domain modulation?" Handling both FM and TDM is something that the military systems don't need to worry about as they all use FM, but commercial base stations would have to handle both to get the cost savings from simpler hardware.

"Then, what about GPS satellite navigation [for location based services] or [added value services such as] TV signals?" he said. "A wideband filter would leave the receiver low noise amplifiers (LNAs) unprotected from the high transmission power and there are very strict rules in each band for the modulation to prevent leakage."

He also points to radio regulations that require large, specific guard bands. Handling specific standards with a radio front-end allows the hardware to concentrate on specific frequency ranges, but having a very wide input would mean the guard bands of some technologies would fall directly on the signal bands of others, causing real problems.

Some supporters of SDR have said that the new technology means you don't have to worry about these elements, as they can be handled within the system, but Scheck disagrees.

"SDR doesn't make radio regulations and frequency planning obsolete – that's a dangerous statement," he said.

But companies at the heart of SDR such as FPGA vendor Xilinx still see it as a major market opportunity. "It seems to be closer than it's ever been before," said Chris Dick, DSP Chief Architect at Xilinx. "It looks like the network operators really are under pressure to force the equipment makers to cut the cost of base stations."

However, he sees no sign of SDR emerging from its use in the military sector any time soon, and when questioned says he can see no base station vendors committing to SDR as yet.

UK chip designer speeds up development of 3G phones

Cambridge-based TTPCom supplies hard IP for GSM, GPRS and 3G phones, and has now developed software to speed up the development and customisation of basic applications such as email and address books for these phones.

The platform, called AJAR integrates the applications into a phone design that uses either a single processor, a single chip with several processors or a multiple chip design. Previously the different hardware architectures needed different software development teams, which is expensive and time consuming for the phone makers who have to provide different user interfaces and 'look and feel' for the different operators.

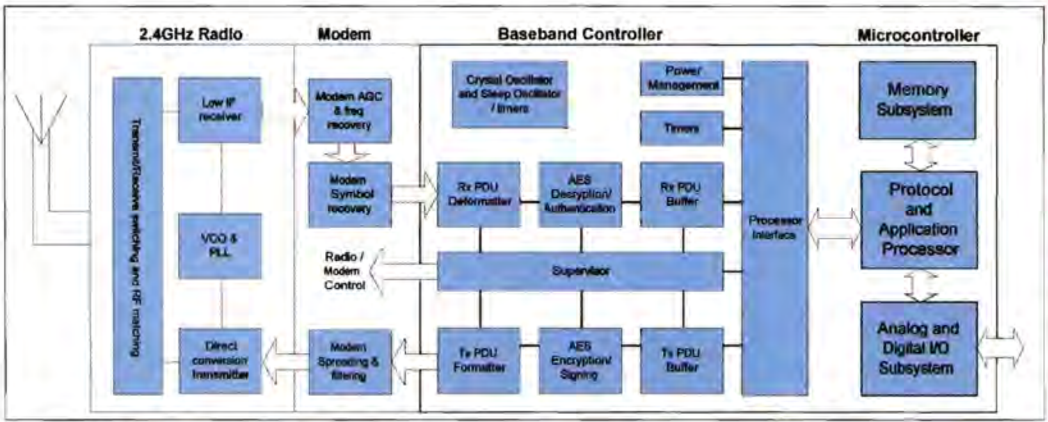
"These are some very significant forces at play as operators want more control over the phones," said Steve Baker, marketing director for the software business at TTPCom.

AJAR dramatically reduces the software requirement for the handset makers, he says, using a form-based approach and a set of standard APIs. "Instead of having a software team for each different phone, the OEM can have one team for the whole family and the different operators," said Baker.

TTPCom is using this to encourage designers to use its hardware solutions, however, designers are increasingly fitting it into other chipsets instead. SK Teletek in Korea is it for a GSM platform based on a chipset from Analog Devices, while phone maker Asustek in Taiwan is using it on a 3G phone platform using an Intel applications processor. Motorola has also licensed the technology for certain devices.

"The first customers are using AJAR on platforms with TTPCom chipset IP but we are not constrained to TTPCom baseband chips," he said. "It's not public yet but we are engaged with non-TTPCom [hardware] customers."

Single-chip ZigBee from Jennic



Jennic's ZigBee chip's block diagram

Jennic, a fabless semiconductor company based in Sheffield, launched the JS24Z121 single-chip solution for IEEE802.15.4/ZigBee applications. ZigBee, which adds the upper layers and enables inter-station connectivity for the IEEE802.15.4 standard, is aimed at low power sensor and control applications, particularly where power consumption must be minimised.

The new device provides a single chip solution for applications requiring microcontroller functionality with an in-built wireless link. It is fully compliant with the IEEE802.15.4 standard, providing robust spread spectrum communication with highly secure AES encrypted data flow. This device allows applications to be developed using either ZigBee or other proprietary networking layers. The device is highly integrated and only requires an external crystal, flash memory, decoupling components and a printed antenna to complete a solution for most applications.

In addition to the wireless functionality, a range of analogue (ADCs, DACs, comparators, temperature sensor) and digital (SPI ports, UARTs, timers, general purpose I/O) peripherals are provided. The device offers low system-power consumption, particularly in sleep mode. This is achieved by using an embedded clock oscillator on the chip and, also, by implementing the MAC functionality in hardware, thereby reducing the microcontroller activity. The IEEE802.15.4 software is supplied with the device and the ZigBee protocol stack is available separately from Jennic.

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A deal has been signed between NPL and the University of Surrey's Nano-Electronics Centre to appoint a visiting NPL Strategic Research Fellow to work jointly between UniS and NPL, in order to exploit new and future technological advances in the area of Carbon Nanotube Probes.

Researchers at Toshiba's Cambridge Laboratories today revealed their latest scientific breakthrough – a light source that can send single photons in a regular stream over a long distance optical fibre network – paving the way for the 'unhackable' network.

University of Surrey and University of Southampton researchers have won a £373,000 award from the EPRSC under the Next Generation Electrophotonics programme. The interdisciplinary team of physicists, engineers, material scientists and biological chemists will study optical non-linearity in carbon nanotubes.

Dr Richard Curry of the University of Surrey has been awarded a grant of £122,000 from the EPSRC to carry out research on hybrid quantum dot systems. Dr Curry will be joined by Korean researchers to study real-time kinetics of the energy transfer between organic complexes and colloidal quantum dots.

Professors Ben Murdin and Ortwin Hess from the Advanced Technology Institute, have been awarded a grant of £221,000 from EPSRC to study spintronic devices. In the field of spintronics, it is the electron spin which encodes information.

TOP 10 TIPS

TRADING WITH CHINA

- Don't be afraid of being foreign, but pay attention, show respect and don't be aggressive or loud. Listening is very important.
- Business culture is very different in China. Try to learn as much about it before you go by researching the subject, the markets and competitors there.
- Cultivate relationships within business and government circles.
- Put time into social occasions. For example, attend banquets, even if there are two or three in an evening – try to go to all of them. For the Chinese a banquet is dinner. It is formal and includes speeches.
- Don't fill the silences, especially in negotiations. Silence and patience is not difficult for the Chinese when in business discussions – to them it is natural.
- Do not be too modest about your achievements – the Chinese like to be associated with success.
- Never get angry or show your frustration when negotiations get tough.
- Play hardball, but courteously. It is worth having contingencies and options, as this will increase your chances of success rather than ending up in arguments.
- Never allow your business contacts or employees to 'lose face'.
- Negotiation never stops, even after the contract is signed. Chinese think very strategically and for the long term. It is not seen as devious to keep negotiating to get the best deal.

This month's Top Ten Tips were supplied by Peter Eales, Director of OI Solutions Limited, a business consultancy focusing on helping firms expand into overseas markets.
(www.oisolutions.com)

So, what use are FPGAs?

What do microprocessors and FPGAs have in common? Nick Martin explains

There are two ways of looking at the overall impact of FPGAs on the electronics industry. The first is to consider them as a cool way of implementing digital logic. This is the conventional model that sees FPGAs as better, cheaper, faster and field-configurable for implementing digital electronics. This view is simple and comfortable – doing the same thing in a more efficient way. It is not really disruptive, it just gives us access to more power at lower cost.

If, however, if we look at the bigger picture and where FPGAs are positioned, what we see is a technology that is part of a much larger trend in the development of electronic products – the move from 'hard' to 'soft' design. This is a more scary view of the world because it threatens the way we see the whole process of designing electronics.

The real clues as to what is really going on with FPGAs can be better understood if we first take a trip down memory lane. Let's go back to the early days of the microprocessor – perhaps the last real 'paradigm shift' to hit the electronics industry.

The first, real, microprocessors were developed by Intel, on contract as 'computers' for a desktop calculator product. Although their development was not part of any grand strategy, it wasn't long before their potential was spotted and the personal computer revolution ensued. The widespread use of microprocessors as 'embedded controllers', directly replacing 'hard' electronics, only came after their decreasing cost made them competitive with the old 'hard-wired' solution. Once this point was hit, the use of microprocessors in electronic systems exploded.

In general though, the important thing is not the microprocessor device itself, but rather the change in design trend that it enabled – the move of design content from the 'hard' to the 'soft' domain, which brings some very strategic benefits. The design can be split into two major parts – the design of the hardware platform (the 'dumb' part) and the development of the actual device behaviour (the 'intelligence'). This platform-based approach allows the same physical hardware to be manufactured with much lower risk, because we can modify the behaviour of the application after constructing the hardware.

Starting out life as a tool to increase the efficiency and scalability of designing electronics, the microprocessor ultimately rewrote the rules on what was demanded of an electronic device. It is no longer good enough to be cheap, reliable and efficient; today's electronic devices need to be 'smart'. 'Dumb' hard-wired electronic devices need no longer apply.

> *"As these devices are passing a crucial threshold, in terms of offering a sufficiently large-scale platform at a low enough cost, it doesn't take an oracle to see where this is going"*

When considering the history and potential of FPGAs, the analogy to microprocessors is striking. With FPGAs, the move from 'hard' to 'soft' design that started with the microprocessor revolution can now advance to the next level.

FPGAs started out life in the mid-1980s as a replacement for discrete logic, reducing chip count and improving our power to cost ratio in digital hardware design. Now, FPGAs allow us to take all of the digital hardware and describe it in a soft way (including the actual microprocessors) and then compile this into the design.

As these devices are passing a crucial threshold in terms of offering a sufficiently large-scale platform at a low enough cost, it doesn't take an oracle to see where this is going. Large parts of the system design hardware will inevitably flow onto the 'soft' FPGA domain and join the processor software as part of the 'embedded intelligence' of the product, rather than being part of the hard-wired platform. PCBs will be the physical platform and provide the connection between the 'real' design platform – the FPGA – and the outside world via analogue interfaces.

The fact that such a large part of the 'real' design can now be described in a soft way and then compiled into the physical hardware, forces us to review our whole approach to the design process. The designer can now make choices about how to split the system between software and 'soft' hardware implementation after the physical device is actually manufactured – even after the device is in the field.

To realise the true benefits that moving the entire system into the soft domain offers, design tools must support the convergence of software and hardware design within the transmutable environment of the FPGA. They must, therefore, support a much more holistic approach to the entire design process. In particular, the FPGA-hardware and embedded software domains must move towards becoming a singular, unified design process. When this happens, brace yourselves for a state change in the way we do electronics design and an explosion in innovative applications to rival that heralded by the introduction of the microprocessor itself.

Nick Martin is CEO and founder of Altium Ltd.

4ms. This is independent of the current and the requested frequency. Samples of the sine waves are generated by a program in the microcontroller (see '**The design procedure**' below).

My design is for the AT89C2051-24PI microcontroller (MCU). This is a 2MIPS controller from the Atmel 51 family. Generated samples are forced to a DAC. The DAC converts digital samples to quantised current samples. An op-amp generates the voltage samples and a low-pass filter attenuates the sampling frequency, which means we then have a pure sine wave.

The total program binary file is less than 1kB. The sampling frequency is 50kHz and the low-pass filter is a 4th degree with a cutoff frequency at 14kHz.

The microcontroller has 6 input bits for the frequency. If the number of bits is N, then in the next 4ms the output frequency will be N·250Hz. For example, if N=20 then the output frequency is 5000Hz.

DFT (Discrete Fourier Transform) calculations in samples generated from the MCU yield THD in the frequency band of 0-14kHz and it is better than -40dB (less than 1% accuracy).

The design procedure

After calculating some parameters, I program in C to generate tables for the microcontroller. Then, I code the microcontroller assembly program.

The algorithm is based on some calculations and look-up tables (LUTs). There are three LUTs – Mtable, LTable and SINTable (I have selected the names, based on my design vocabulary).

The sampling rate is based on the MCU's processing power, in this case 2MIPS. If the MCU is faster, the sampling rate is greater. The sampling rate, or the interval between samples, directly influences the Mtable and LTable.

I predict how many instructions can be executed in a sampling interval, then I generate the tables and then code the MCU program. If the instructions exceed my prediction, then I lower the rate (allowing more time between samples), reconstruct the tables and then code the program.

By trial and error, I have found that this MCU can run the algorithm in 20μs, in which case the sampling is 50kHz. The tables are based on these figures. There are samples every 4ms. Connecting the end of a sine wave to start another at the end of each 4ms interval makes a continuous wave. In 50kHz sampling, there are 200 samples.

A counter in the MCU clocks the samples and each time it counts to zero it re-initialises to 200. This creates the continuous wave generation.

The base frequency is defined as the minimum frequency that can be generated by the algorithm. Here that is 250Hz. Note that 4ms is the period of the 250Hz tone. If base was 333.333Hz, then the interval of the sine wave generation would be 3ms.

The MCU performs some simple calculations by N and counts the samples. These calculations result in two sets of numbers – L and M, which can be looked up in the LTable and Mtable, respectively. These numbers are then added to each other and the new number is X. The mapping of X to SINTable results in Y. Y is copied to the DAC port and a sample is created. The sample counter is updated and a new loop starts.

A synchronising pulse is generated by the MCU, as well, which also indicates the time when N can be changed. This is typically after the rising edge of the load signal. Upon this condition, the sine waves are connected to each other and a tone stream is generated.

Note that there are 40 MCU cycles in the sampling interval. The algorithm ends in 35 MCU cycles, which means that generating a new sample takes 35 machine cycles. My algorithm is designed to overcome all the conditions occuring during execution, such as initialisation of counters and registers, checking N and so on. I cannot process conditions if the sampling interval is less than 17.5us. Thus I have 2.5us to return interrupt and others. The algorithm is designed for this 8-bit microcontroller.

THD summary

The algorithm is simulated in C. The C program generates the exact same samples as the MCU does. The results of the algorithm are analysed by DFT. The sine function is

$Y=127 \cdot SIN(2\pi ft)+128$

The table on the next page ('**THD and maintone amplitudes**') shows the THD and the main tone amplitudes.

The tone amplitude has a max 0.3% ripple. The frequency stability is perfect as XTAL is the base for the MCU clock. If we use 30ppm XTAL for MCU, max drift of sine tone is 30ppm. For example, if XTAL was 30ppm, max drift is in 10kHz, which is 0.3Hz.

I have not used a spectrum analyser to check the harmonics or measure THD.

The algorithm

I have developed the algorithm to be better than -43.13dB. Developing algorithms to generate better sine waves can be achieved by decreasing the sampling rate to 40kHz and adding two new tables to the microcontroller program. By choosing ADC to 10 bits, sampling to 50kHz and with an improved algorithm, THD can be better than -59dB.

The algorithm is so powerful that can generate better than -60dB THD. However, its main restriction is the MCU's processing speed. For 8-bit MCUs, THD of -43.13dB is the lowest limit. Much better results can be achieved with a high-speed 16-bit MCU.

Other restriction could be the DAC's resolution; if we increase it to 10 bits or higher, THD can be improved beyond -60dB.

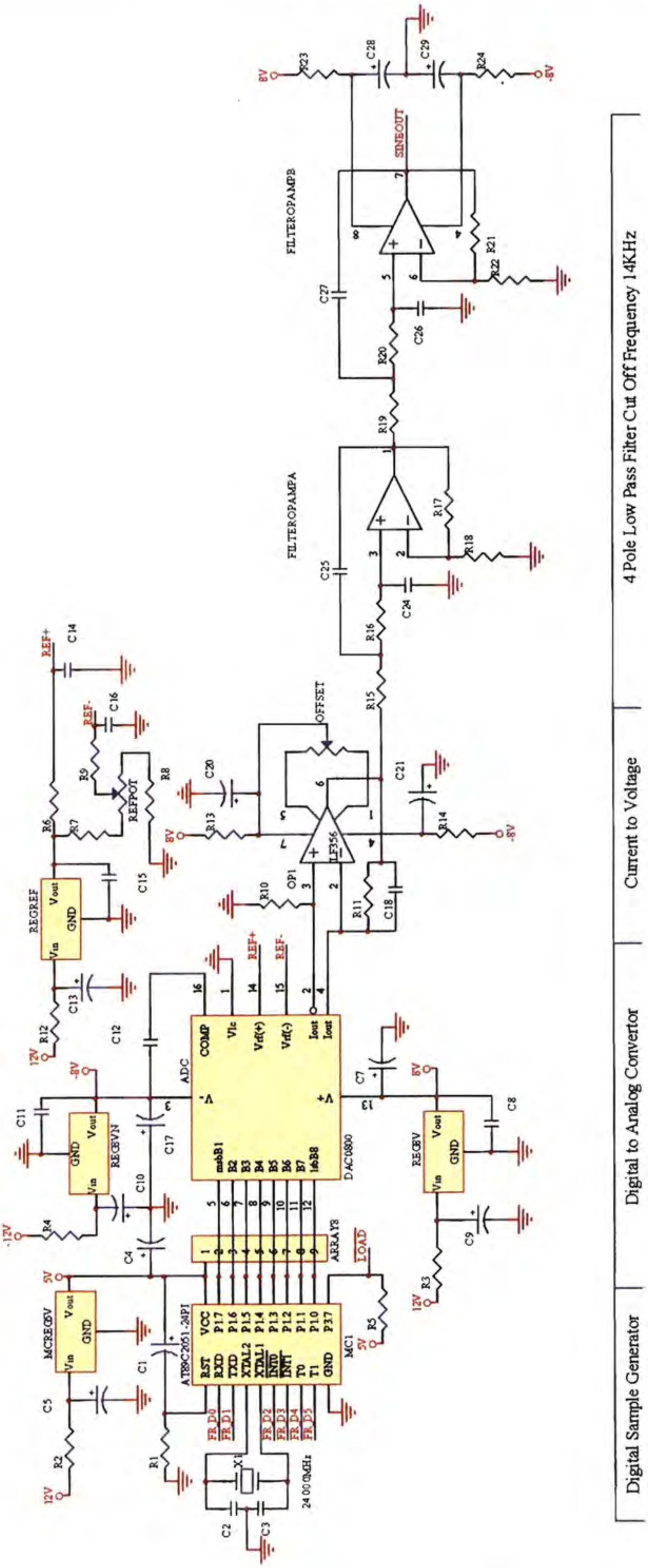
The algorithm is simple enough to be designed for FPGAs or ASICs. If an ordinary sine wave generator is the goal of design, the clock source of FPGA is two or three times that of the sampling rate. In digital devices, lower clock results in lower power consumption. I guess that with a simple FPGA, 2MHz sine waves can be generated.

Applications

There are many applications for this, including modulators that can be used as high reliability modems in HF radio communications systems, reference generators for PLLs, frequency meters and time-base generators, audiometers as multiple sine wave generators, audio measurement instruments and laboratory function generators, among others.

THD and main tone amplitudes

Tone(HZ)	MainLevel	THD(dB)
250	127.0785	-47.35
500	127.0080	-44.99
750	127.0376	-41.82
1000	127.1240	-39.95
1250	127.0856	-41.57
1500	127.0113	-43.26
1750	126.9777	-40.80
2000	127.1628	-40.43
2250	127.1101	-42.23
2500	127.1931	-40.35
2750	127.0373	-41.39
3000	127.1842	-41.60
3250	127.0404	-42.40
3500	127.0356	-40.64
3750	127.1309	-41.21
4000	127.2015	-42.24
4250	127.0137	-41.35
4500	127.1014	-40.51
4750	127.0412	-41.09
5000	127.3604	-41.40
5250	127.0491	-40.69
5500	127.0861	-40.80
5750	127.0286	-41.78
6000	127.1986	-41.35
6250	127.1396	-infinite
6500	127.0370	-41.26
6750	127.0813	-40.90
7000	127.1610	-40.24
7250	126.9902	-41.95
7500	127.2287	-41.72
7750	127.0117	-41.83
8000	127.2225	-42.50
8250	127.0505	-42.02
8500	127.0748	-40.14
8750	127.1123	-40.80
9000	127.1858	-40.67
9250	127.0461	-42.64
9500	127.0995	-41.23
9750	127.0259	-40.70
10000	127.3876	-41.24



ADSL2+ line driving solutions

Christophe Prugne, from the standard linear division at STMicroelectronics (ST), presents an overview of the ADSL application environment and gives examples of how to set up an ADSL2+ analogue line interface.

Digital Subscriber Line (DSL) is a technology that converts current twisted-pair telephone lines into access paths for multimedia and high-speed data communications. A modem is connected to a twisted-pair telephone line, creating three information channels. A high-speed downstream channel, a medium-speed upstream channel and POTS (Plain Old Telephone Service) split off from the modem by filters. These channels depend on the implementation of the architecture as described in **Table 1** opposite.

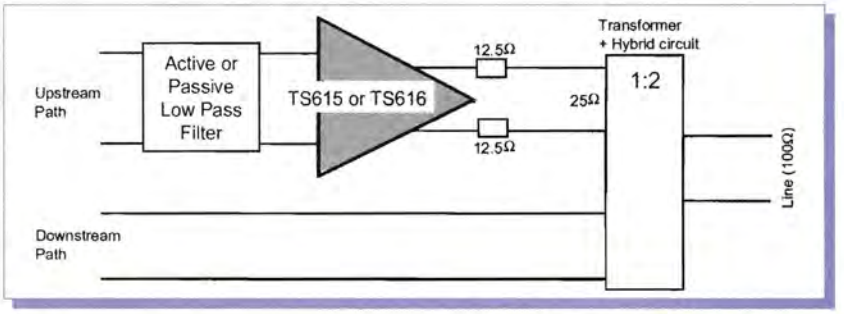


Figure 1: Typical ADSL line interface

Table 1: ADSL spectrum allocations

	POTS (4kHz)	*ISDN*	*Upstream (Hz)*	*Downstream (Hz)*	*Comments*
ADSL2+					
Annex A	yes		30k >130k	2.2M	
Annex B	yes	yes	64k >256k	2.2M	Over ISDN
Annex C					All digital loop. Over POTS
Annex I	no	no	4k >130k	2.2M	Large Upstream without ISDN
Annex J	no	no	4k >256k	2.2M	Long reach. Modulation chosen to increase the data rate on long lines.
Annex M	yes	no	30k >256k	2.2M	
ADSL2					
Annex A	yes		30k >130k	1.1M	
Annex B	yes	yes	64k >256k	1.1M	Transmission via ISDN line
Annex I	no	no	4k >130k	1.1M	All digital loop technology, transmitted via POTS
Annex J	no	no	4k >256k	1.1M	Large Upstream without ISDN
Annex L	yes	no	30k >130k	1.1M	Long reach. Modulation chosen to increase the data rate on long lines.
Annex M	yes	yes	30k >256k	1.1M	

The line interface – ADSL remote terminal (RT)

Figure 1 shows a typical analogue line interface used for ADSL. The upstream and downstream signals are separated from the telephone line by using a hybrid circuit and a line transformer. On this note, emphasis will be placed on the emission path. Several criteria must be recalled:

➢ **Power supply**

The choice of the power supply of the driver is directly linked to several factors:

- the turn ratio of the line transformer;
- the output capabilities of the driver (maximum output swing, output current, linearity versus load);
- the line matching technique;
- and the insertion loss of the hybrid circuit.

To fit with +5V and +12V power supplies available in multimedia equipment, we show here the implementation of drivers in +5V and +12V single supplies.

➢ **Temperature considerations**

ADSL drivers must adequately dissipate power in order to maintain an operating temperature range, where their linearity and stability are not affected. This aspect is very important to improve the SNR of the downstream signal and to improve the data reception rate. Here, we will focus on techniques that improve heat dissipation and the linearity of the

Table 2: Main characteristics of the drivers

		power down	Bw Gain=4 (MHz)	SR (V/µs)	Iout Typ. (mA)	Noise (nV/√Hz)	Icc per op. (mA)	HD2/HD3 (dBc)	Vout differential (Vpp min)	Packages
TS616	CFA	no	40	420	420	2.5	13.5 (@12V) 11.5 (@5V)	87/83*	20.7 (12V) 7.2 (5V)	SO8 Exposed Pad
TS615	CFA	yes	40	420	420	2.5	14 (@12V) 11.9 (@5V)	87/83*	20.7 (12V) 7.2 (5V)	TSSOP14 Exposed Pad

*) Differential 16Vpp/110kHz on 50Ω.

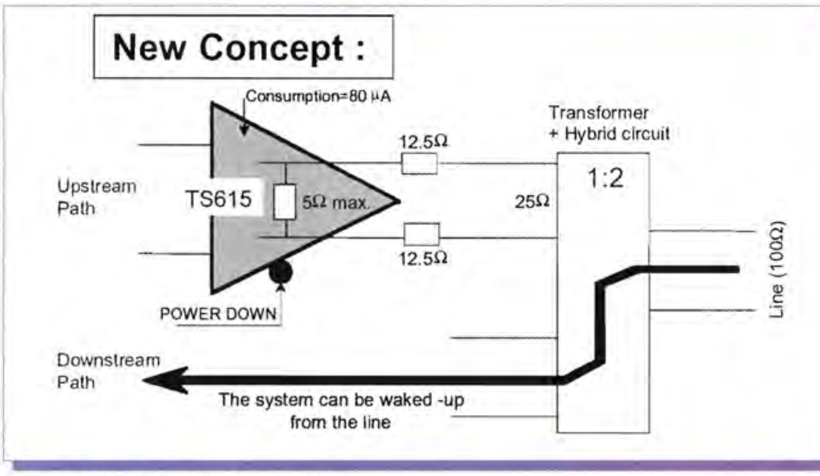


Figure 2: TS615 power-down mode

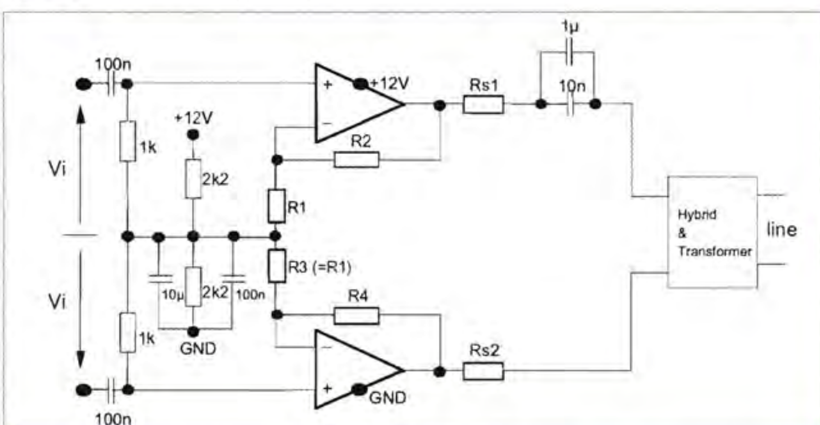


Figure 3: TS616 (or TS615) as a differential line driver with a +12V single supply

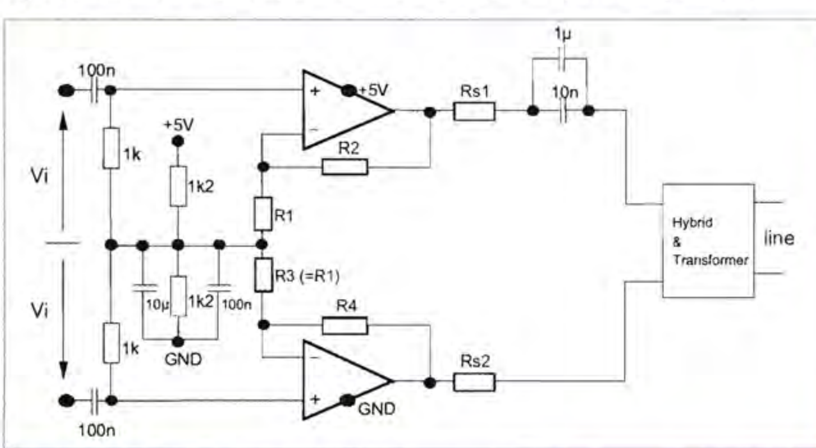


Figure 4: TS616 (or TS615) as a differential line driver with a +5V single supply

drivers, by showing the measurements of intermodulation products.

ST's TS616 is housed in an SO8 exposed pad plastic package with the same standard pin-out as the TS613. This feature allows the TS616 to be evaluated more easily on existing boards. The TS615 uses the same design as the TS616 and, in addition, offers the advantage of a power-down mode in order to minimise power consumption when the modem is not in communication. In power-down mode the TS615 shortcircuits the output short. As described below, this feature allows one to maintain a good impedance matching with the line while the modem is in sleep mode, as well as allowing one to wake-up the modem via the telephone line (an important advantage that ADSL modems have over POTS solutions).

12V power supply: Remote ADSL modem terminals must be designed to easily connect to a PC. For such applications, the driver should use a +12V single power supply, which is available via standard PCI connectors. Note that the TS616 and TS615 can also be powered by a dual +/-6V power supply.

Figure 3 shows a single +12V supply circuit with the TS613 as a remote terminal transmitter in differential mode. Note that one could also use the TS612 in exactly the same schema.

The aim is to decrease the power consumption of the line interface by reducing the power supply. As the output swing of the driver will be reduced, the magnetic transformer turn ratio must be increased to maintain the correct power level of the line. A turn ratio of 4.5 fits well with these requirements. TS616 (or TS615) as a differential line driver with a +12V single supply.

The power supply can only be reduced to the limit of the capability of the driver to drive a differential load below 10Ω, while maintaining good linearity (the linearity of an operational amplifier is directly linked to the load).

Thermal considerations

The choice of the package is directly linked to the evaluation of the junction temperature (Tj) of the driver while in communication. **Figure 5** shows the calculation of the power, which the driver dissipates.

Table 3 shows the accordance, by package and by power supply, of the maximum external temperature (Ta), which should be reached when the modem is in communication. We consider that

Table 3: Package specifications

	Package	Rthja (°C/W)	Iccmax (mA)	Static Dissipated Power (mW)	Dynamic Dissipated Power (mW)	Total Dissipated Power (mW)	Ta max (°C)
TS616 (5V)	SO8 e-pad	60	15	150	297	447	123
TS616 (12V)			17	408	322	730	106
TS615 (5V)	TSSOP14 e-pad	40	15	150	297	447	132
TS615 (12V)			17	408	322	730	120

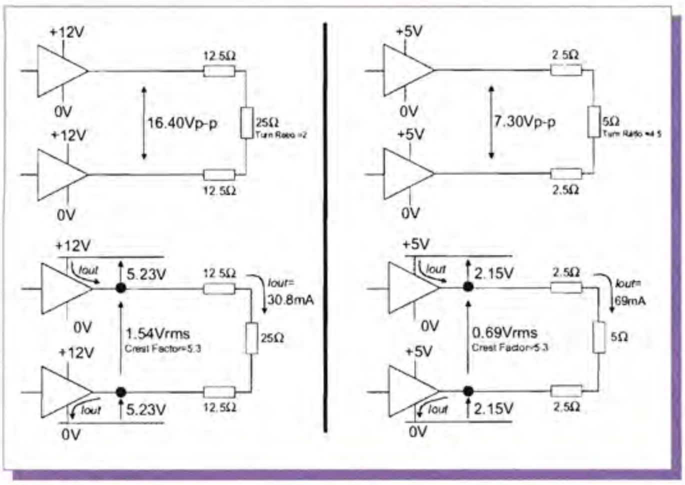


Figure 5: Power dissipation (+12V and +5V power supply)

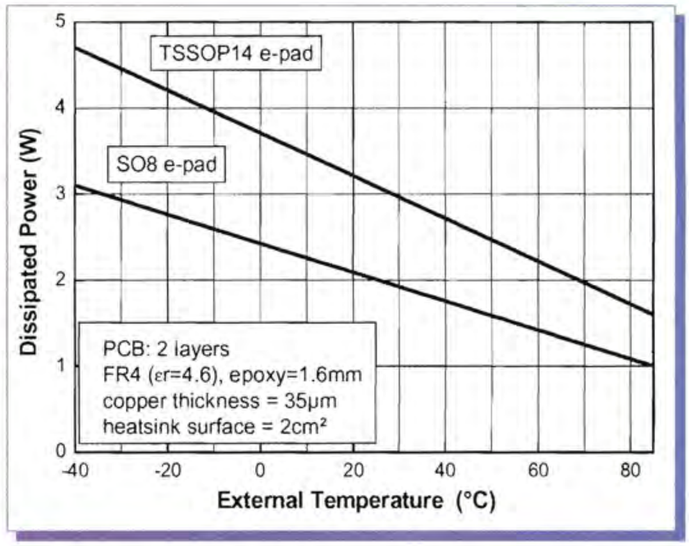


Figure 6: Thermal considerations: power dissipation of the packages vs temperature

Caution: The pad must be in thermal contact with the heatsink. If the pad and the heatsink are floating, their surface can create parasitic capacitors located on the substrate of the dice. To remove these parasitic capacitors, the copper layer must be connected to -Vcc (GND in case of single supply)

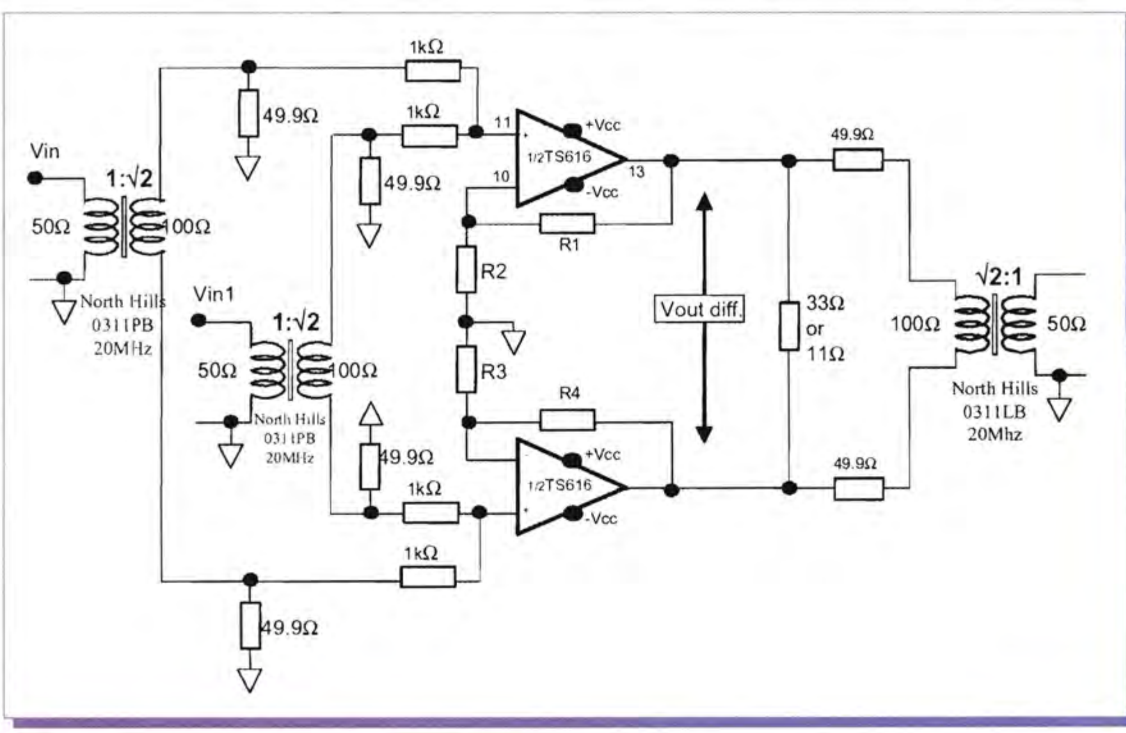
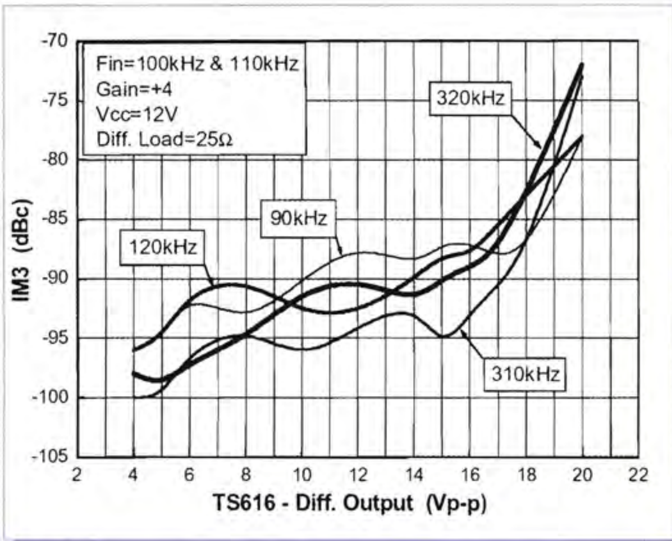


Figure 7: Implementation of the line driver for two-tone intermodulation measurements. The driver is used in non-inverting summation configuration



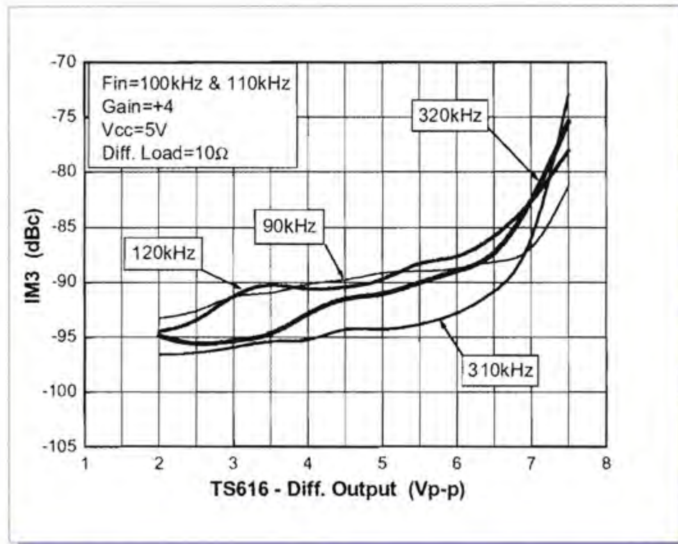


Figure 8 (left): Intermodulation of TS616 and TS615 on 25. load (Vcc=12V) **Figure 9 (right):** intermodulation of TS616 and TS615 on 10. load (Vcc=5V). Fin=100kHz and 110kHz, differential signal, producing intermodulation products on drivers located at 90kHz, 120kHz, 310kHz and 320kHz

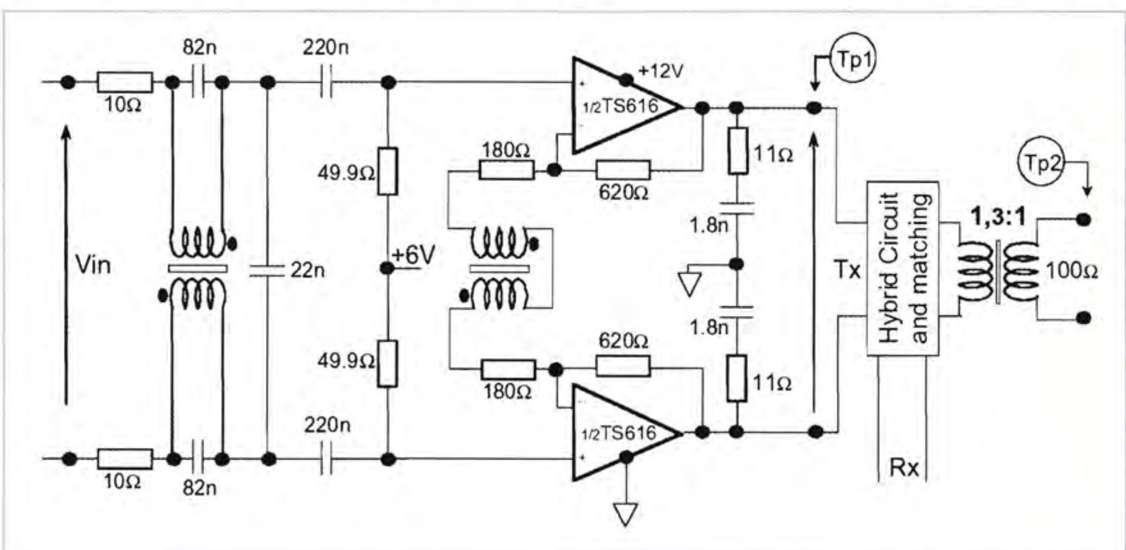
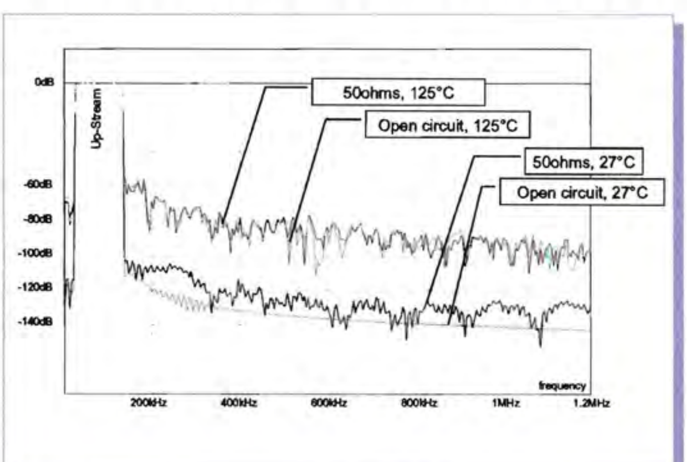
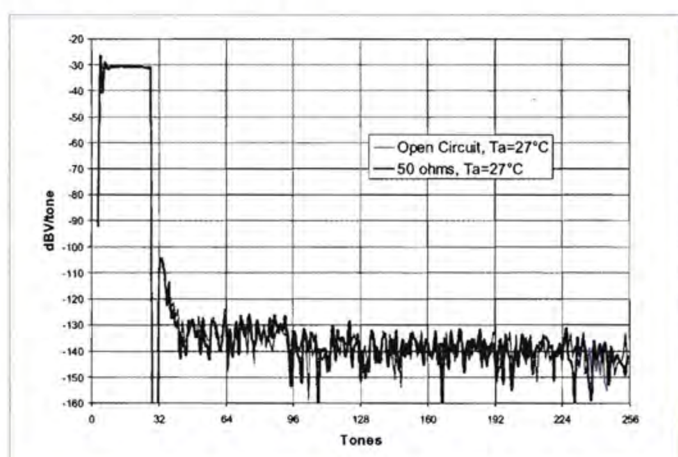


Figure 10: Line interface implemented on the ST's ADSL2+ solution. Hybrid circuit and matching are not described in this paper

Figure 11 (below left): Simulation results in TP. Simulation performed with the TS616 eldo model and the ADSL input signal eldo model (crest factor = 6.2). The temperature is the junction temperature. **Figure 12 (below right):** Measurements in TP2





Tj=150°C and that Power=(Tj-Ta)/Rthja, where Rthja is the junction/area thermal resistance of the product.

Calculations show that even while in communication, both drivers maintain safe behaviour over the entire temperature range given by the datasheets (-40°C to +85°C). The maximum operating temperature of +85°C can be considered as a guarantee. In terms of qualification of TS616 and TS615; Ta higher than 85°C is not guaranteed by ST.

These measurements have been done on a board with the following physical characteristics: 2-layer PCB, FR4 (Σr=4.6), epoxy=1.6mm, copper thickness = 35μm, heatsink surface = 2cm^2. Please see the evaluation board kit "KITHSEVAL/STDL", or its accompanying user manual for more information on boards.

Results over the ADSL spectrum

Finally, to achieve a very good SNR, Bilge Bayarakci of STMicroelectronics, Zaventem (Belgium) has set up the line interface. He uses the TS616 in a 12V single supply, with a mid-supply described in Figure 3 and a passive third-order, low-pass filter. L1, L2 and T2 are used to decrease the gain at higher frequencies with good common mode rejection. Decreasing the gain and applying a low-pass filter allow one to decrease the noise in the ADSL spectrum.

Figure11 shows simultations performed on TP1 considering a differential load of 50. and an open circuit. The focus is on the level of the noise in the down stream signal.

Figure 12 shows measurements of ADSL spectrum on the STMicroelectronics solution using the analogue front-end ST20184.

The attraction of magnetic RAM

With its characteristics, MRAM is a serious contender for dominance in certain digital applications, leaving flash memory behind, says Dr Faiz Rahman

You switch on the TV and it springs to life almost instantaneously. Do the same with a PC and it will take a few minutes to become operationally active. This delay is caused by the necessity to load a large operating system program from a hard disk drive medium (which is slow but offers permanent storage capability) to semiconductor memory (which is much faster but loses its contents once power is switched off). Thus, the inconvenience of long computer boot-up times is a result of the non-availability of an ideal memory technology that would be cheap, fast, long-life and non-volatile, all at the same time.

Present day memory technology offers a number of different types of memory devices, each with some outstanding characteristics but lacking in other desirable attributes. The result is that contemporary digital equipment has to be built from a multitude of different memory types, which leads to very complex systems that still fall short of performance goals. Clearly, the availability of an ideal memory technology with these desired attributes will be a great step forward in the continued development of all kinds of digital appliances.

Fortunately, such a memory will soon start appearing in consumer electronics systems, after years of steady development in some of the best industrial R&D labs in the world. This device, called Magnetoresistive Random Access Memory or MRAM, is a quite different technology when compared with other RAM devices.

Shared legacy

Being a magnetic storage technology, MRAM shares certain characteristics with legacy technologies such as core memory and bubble memory, which were prevalent during the initial days of digital computer technology. All of these store digital bits as one of two polarisation states of magnetic material. The more modern RAM technologies, in contrast, use completely electronic means for digital information storage that makes them much easier to use and has led to the complete obsolence of earlier magnetic storage technologies.

The emerging magnetic random access memory technology, however, is based on radically new concepts and offers economic and performance benefits that will be hard to beat by any other memory technology in existence today.

To begin with, MRAM, like all magnetic storage technologies, is inherently non-volatile, while, at the same time, offering a truly random access. Other present-day non-volatile memories like EEPROM and Flash also offer long-term power-free storage but at the expense of access speed, especially when it comes to write operations. MRAM offers access times of 25ns (Freescale's MR2A16A, 4Mbit Asynchronous Magnetoresistive RAM) that are comparable to that of leading static RAM (SRAM) families (around 10ns). Some devices that are still in the development stage have write times of around 4ns, which is shorter than that for most SRAM chips. This means that MRAM could also be used as cache memory in computer systems. Non-volatility also leads to reduced power drain of only about 495μW in standby mode – a distinct advantage for portable and handheld devices. Furthermore, MRAM is also the clear winner when it comes to read-write endurance, which refers to the number of times a memory location could be written to or read from, before permanent degradation sets in. This is a well-known issue with current flash memories because these require high-voltages for programming (write operation). However, extensive tests have validated the resilience of magnetic RAM technology in this respect. Commercially available chips now boast an endurance of greater than 100,000 read-write cycles and data retention periods of more than ten years. These performance attributes of MRAM are compared with that of generic SRAMs (see **Figure 1**).

As if this were not enough, the basic structure of MRAM is such that it leads to very dense memories, greatly reducing the cost of storage per bit. It is thus possible that, as this technology matures, it could well pose a challenge to the long entrenched dominance of dynamic RAM (DRAM) in mainstream computer applications. Magnetoresistive RAM is, therefore, almost a dream come true for digital system designers and no wonder it has been called the ideal memory for tomorrow's digital systems.

The technology also offers the promise of high efficiency multiport architecture for video and multiprocessor systems, radically new embedded logic products and system-on-a-chip (SoC) devices.

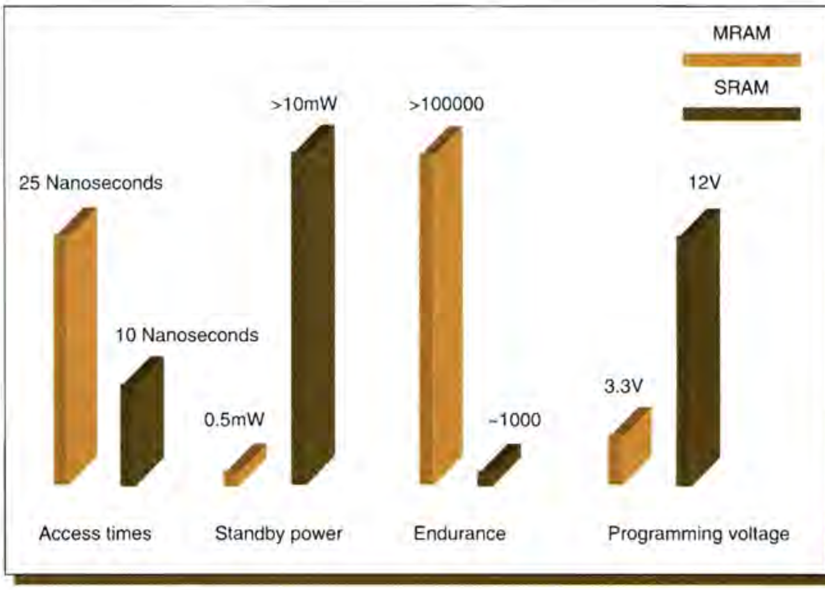
One mighty technology 'sandwich'

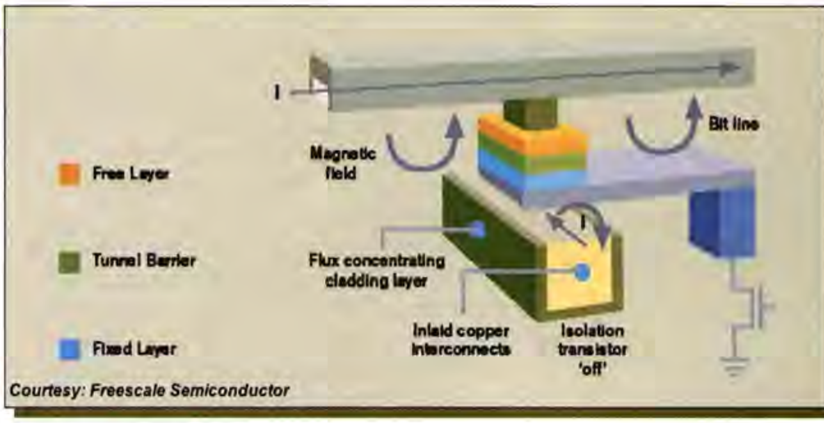
Magnetoresistive RAM hasn't emerged on the scene overnight. Its basic structure has been under development for many years. At the heart of an MRAM chip is a tiny sandwich of magnetic and insulating thin films called a Magnetic Tunnel Junction (MTJ). Essentially, it acts as a two-value resistor whose resistance depends on whichever of its two possible magnetic states it is in. This bistability lets an MTJ store a 0 or 1 bit, much in the same as the presence or absence of charge lets a DRAM device store information.

However, because the magnetic polarisation states of an MTJ don't need any power to survive (exactly as any ordinary magnet keeps its magnetism without any external energy expenditure), so unlike DRAMs and SRAMs, memories based on MTJs neither require periodic refreshing nor application of power to retain contents.

The basic structure of MTJs was developed way back in the 1970s by IBM researchers. Over the years, it was recognised that what appeared as a mere research curiosity could become the central element at the heart of a new type of solid-state memory device. Further development of MTJ-based memory was undertaken by IBM researchers at the company's Almaden labs in San Jose, California. That work, as well as work by several other companies, resulted in the development of what is now recognised as the standard architecture of MRAM chips.

Besides IBM, other companies that have been involved with the development and commercialisation of MRAM devices include Motorola (now Freescale Semiconductor), NVE Corporation, Hewlett-Packard, Honeywell, Infineon Technologies, Cypress Semiconductor, Samsung, Hitachi, Sony and NEC.





Courtesy: Freescale Semiconductor

Figure 1 (Top): Specification comparisons between MRAM and SRAM cells

Figure 2: MRAM cell's structure

The structure of a typical MRAM cell is shown in **Figure 2**. An MTJ, as described above, is found at the centre of each memory cell, just as a capacitor or a flip-flop is found at the centre of every DRAM or SRAM cell respectively. The tunnel junction itself is made of two layers of magnetic material separated by a thin layer of a material that is both, non-magnetic and non-conducting. One of the magnetic layers has a fixed permanent magnetic orientation, while the other is capable of switching its polarity from one orientation to the opposite one.

The two magnetic polarisation states of an MTJ correspond to the two magnetic layers having parallel and anti-parallel orientations. A current could be made to flow through the junction via a quantum mechanical tunnelling process and the amount that flows under a given bias voltage depends on the

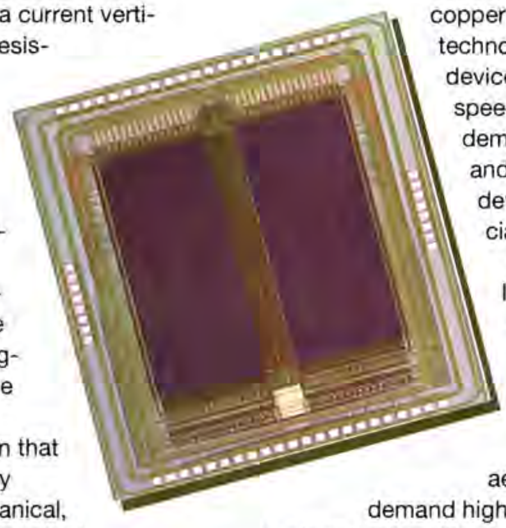


Figure 3: MRAM developed by Freescale Semiconductor

polarisation state of the magnetic junction. This is because electrons carry both electric charge and a magnetic polarisation and are, therefore, affected by the relative orientation of the two ferromagnetic layers. The parallel state offers less resistance to tunnelling current than the anti-parallel state. This is called the magnetoresistive effect.

The magnetic orientation of an MTJ is thus, quite simply, sensed by passing a current vertically through it and sensing the resistance of the sandwich. Detection of one of the two possible values then determines whether a 0 or a 1 is stored at that location. Setting the bit state is also quite straightforward and involves sending a small current in one of two directions, through the top layer of the MTJ structure, which sets its magnetic orientation to one way or the other, thus storing a 1 or a 0 bit.

Exhaustive lab tests have shown that the magnetic state of MTJs is very stable and is unaffected by mechanical, thermal and magnetic shocks. The actual cell access circuitry involved in accessing specific tunnel junctions is exactly the same as for other memory architectures and involves a bit-line transistor at each memory cell location that is used to select an MTJ for both, read and write access.

In addition to all this, the on-chip circuitry used for accessing the memory cell blocks on MRAM devices is the same as is used with more conventional memories so that the external chip interface looks no different than that of a commodity SRAM device. This essentially means that existing systems could be upgraded to use MRAMs without investing large amounts of redesign effort. So, a variety of digital devices could be improved with relatively little engineering work.

Close to market

Commercial development of MRAM technology accelerated in the late 1990s. IBM joined forces with Infineon in November 2000 to jointly develop and sell these products for both in-house and OEM customers. The first development of their joint venture, called Altis Semiconductor, was a 128kbit MRAM core fabricated with a 0.18µm technology.

Cypress Semiconductor has also developed its own proprietary MRAM cell architecture that, although easier to fabricate, is based on a larger cell size, with two MTJs and three access transistors. They have produced both 64kbit and 256kbit devices.

Freescale Semiconductor has developed MRAMs for use as stand-alone memory components as well as for integration in various embedded applications. Their design is based on a single MTJ and transistor architecture, stacked one on top of the other, which takes up little space and allows the fabrication of very dense memory architectures. The copper interconnect based technology also enables these devices to operate at high speeds. They have already demonstrated a 1Mbit chip and have a 256k x 16-bit device that is commercially available.

Freescale has also licensed its MRAM technology to Honeywell, where they are working on developing this product for military and aerospace markets that demand high-reliability, radiation hardened chips. Memories based on MTJs are not as susceptible to radiation-induced damage as are other mainstream memories. Furthermore, when magnetic memories are integrated with radiation resistant silicon-on-insulator (SOI) logic circuitry then the combination appears extremely attractive for applications in space, where survival from radiation exposure is a major challenge for electronic systems.

The outstanding characteristics of magnetoresistive RAM are likely to assure its dominance in many kinds of digital systems. Applications that require data to be quickly stored and recovered, for instance, will benefit greatly from the use of MRAMs, as will products where low power consumption and permanent storage are key requirements. These are certain to replace flash memory in digital data storage products. Use of MRAMs in all of these applications will mean that accidental data loss, due to power outages for instance, will become a thing of the past.

Commercial devices, available from several manufacturers, are now being incorporated into new product designs. These chips include both 5V and 3.3V parts, with access times of around 25ns. Handheld devices containing MRAMs, including PDAs and mobile phones, are expected to hit the market by the end of 2005. As time goes on, magnetic RAMs will gradually take over from other kinds of solid-state memory devices and one of their applications will ultimately make our PCs come to life instantly.

Not so scary Spice

Scary Spice is not only a pop star, but also a language for mathematically describing circuit behaviour to produce working conceptual models before committing to hardware. The editor of Electrical Times, Electronics World's sister publication, reviews Multisim 8.

BY BORIS SEDACCA

Before the age of computers, engineers waited until a design was completely assembled before testing their prototype board. For the majority of designs, this meant that testing occurred far too late in the design flow.

The first computers were programmed in a low level language, called assembler, which manipulated individual gates and switches, and was quite daunting for engineers.

Alternatively, they drew up a circuit schematic and gave it to a programmer to code up a model, allowing them to validate and optimise their circuits at an earlier stage of the design, and so circuit simulation modelling was born.

Then came the first computer language, Fortran, which allowed engineers and scientist to speak to a computer in a way that was familiar to them. It was not long before suites of Fortran circuit models were bundled together as a language on top of Fortran called Spice.

Originally written in Fortran, but latterly translated to C++, Spice needs to be fed with statements in a similar way to Fortran. Very few people today still code directly to Spice. To those who do, I say: we are not worthy.

Nowadays, you are more likely to enter parameters into neat dialogue boxes provided by a front-end GUI. Multisim is a front-end GUI on top of a Spice engine, which allows users to draw schematics and automatically generate Spice code. Also known as Electronics Workbench, the company is now owned by National Instruments.

In a recent survey, 80% of designers said that they would like to simulate before proceeding to PCB layout. In today's market there is constant pressure to bring products more quickly to market than ever before.

With Multisim, a circuit you draw is automatically ready for simulation, with virtual instruments that look and operate like real-world equipment, and which can even be changed while simulating to instantly see the impact on signals.

If you can't find the device you need in Multisim's 16,000 part library, you can import external models written in Spice or VHDL. Alternatively, the built-in Model Makers create Spice models from databook values.

Once your circuit has been proven in Multisim, you can export your design to any of a number of popular PCB layout tools, including Electronics Workbench's Ultiboard and Ultiroute layout and autorouting software.

Functionality includes:

- 'Change-on-the-fly' interactive simulation
- Instant simulation of any schematic
- Virtual Instruments (e.g. logic analyser, scopes, etc.)
- Simulated 'real' Agilent instruments
- Automatic Spice model makers
- Patented co-simulation with VHDL
- Circuit wizards
- Interactive, virtual and animated components
- Simulation advisor
- Comprehensive suite of analyses
- Integration with National Instruments's LabVIEW

Multisim 8 extends this through the addition of powerful and productive features such as:

- A 67% increase in simulation speed
- Simulated 'real' Tektronix instruments
- Robust measurement probes annotate circuit with dynamic values
- Support for design variants
- Simulation profiles (save and re-use Spice parameter sets)
- New circuit wizards and model makers
- New worst-case analysis
- Significantly enhanced schematic capture, including bus support
- Full support for hierarchical designs
- Comprehensive circuit-annotation capabilities

Test 1 – Frequency domain modelling

First let us start with a simple circuit taken from a text book as shown in **Figure 1**. This is a single-order active filter, based on a three-terminal, virtual op-amp. Although it has been redrawn with Multisim, because I'm too lazy to draw one by hand, don't panic – I'm going to start with a blank page and show you how to place components.

The circuit equation is given as 'voltage out' over 'voltage in', thus:

$$\frac{v_{out}}{v_{in}} = -\frac{\dfrac{R_2\dfrac{1}{sC_2}}{R_2+\dfrac{1}{sC_2}}}{R_1+\dfrac{1}{sC_1}} = -\frac{\dfrac{R_2}{sC_2R_2+1}}{\dfrac{sC_1R_1+1}{sC_1}} = -\frac{sC_1R_2}{(sC_2R_2+1)(sC_1R_1+1)}$$

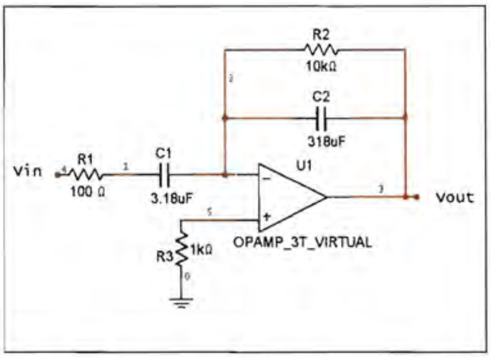
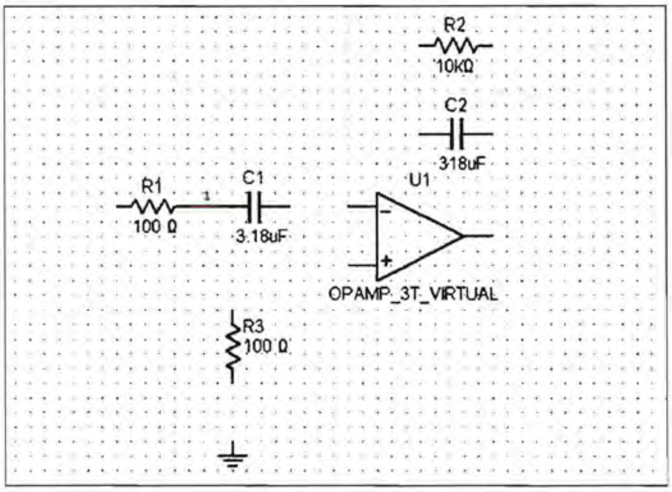


Figure 1 (Left): Single-order active filter

Figure 2 (Right): Placing components on grid

Figure 3 (Below): Completed circuit ready for simulation



Replacing values and ignoring the minus sign:

$$\frac{v_{out}}{v_{in}} = \frac{3.18\text{¥}10^{-2}s}{(3.18s+1)(3.18\text{¥}10^{-4}s+1)}$$

giving the corner frequencies:

$$f_1 = \frac{1}{2\pi 3.18} = 0.05Hz$$

and:

$$f_2 = \frac{1}{2\pi 3.18\text{¥}10^{-4}} = 500Hz$$

Now let's see if Multisim gives the same results. First, we start with a blank page and drop in the components, in this case by picking them from the virtual components shown in blue to the right of the third row, along the top of the workspace.

The first component is a 100Ω resistor. The default resistor value is 1kΩ, but this can be changed by double clicking on the component, whereupon a properties box pops up with the field values to be changed.

Then a capacitor is dropped in and its value is changed the same way, followed by a virtual op-amp, two more resistors and another capacitor. The orientation of a component can be changed by right-clicking on it and selecting horizontal or vertical flip, or 90° rotation.

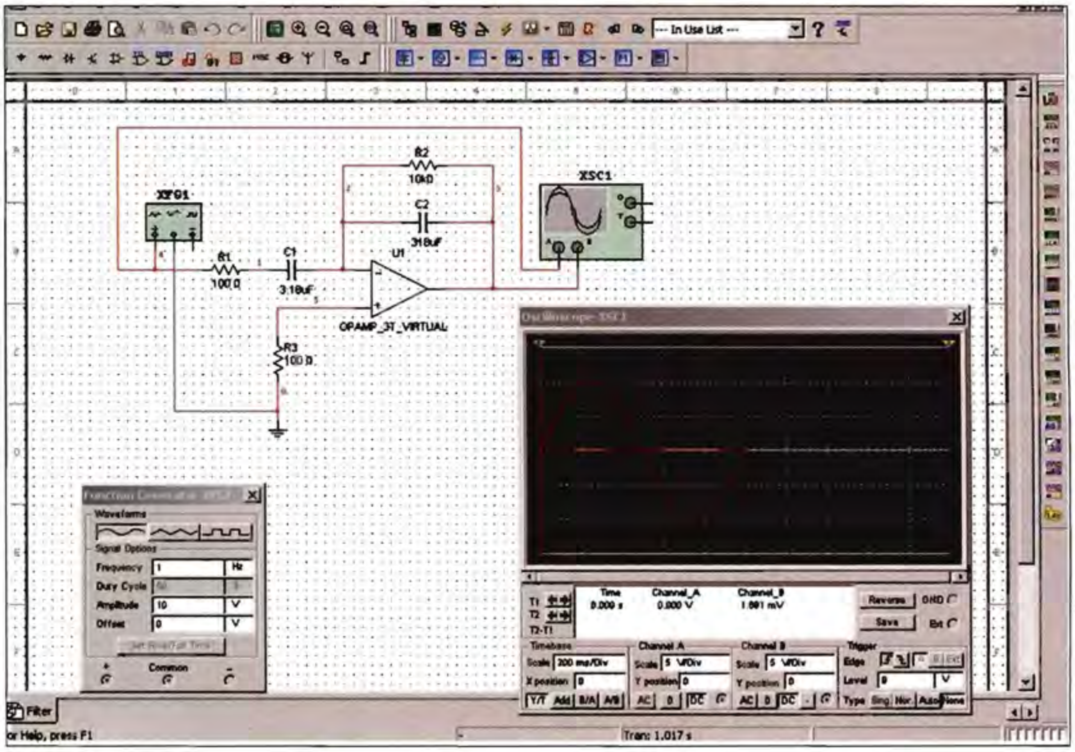
The grid is handy for aligning components to be connected. Once all the components have been dropped in, they can be wired together. They can also be moved about and the wires or circuit tracks will reposition themselves accordingly.

First, click on the right end of the first resistor (R_1) and then click on the left end of the first capacitor (C_1) to create node 1 automatically as shown in **Figure 2**.

You can change the node colour from red, which I am not mad about, to something else. Nodes are numbered consecutively. Any nodes that have an earth attached default to node zero - a convention of Spice.

A node that has several components linked together will keep the same unique number, as shown with nodes 2 and 3 in **Figure 3**. This shows the completed connections, together with a function generator and oscilloscope dropped in from the instruments buttons to the right of the schematic.

Double-clicking on the instruments opens up dialogue boxes. The function generator is set to 1Hz at 10V, and the scope timebase is 200ms per division, while both Channel voltages are set to 5V per division.



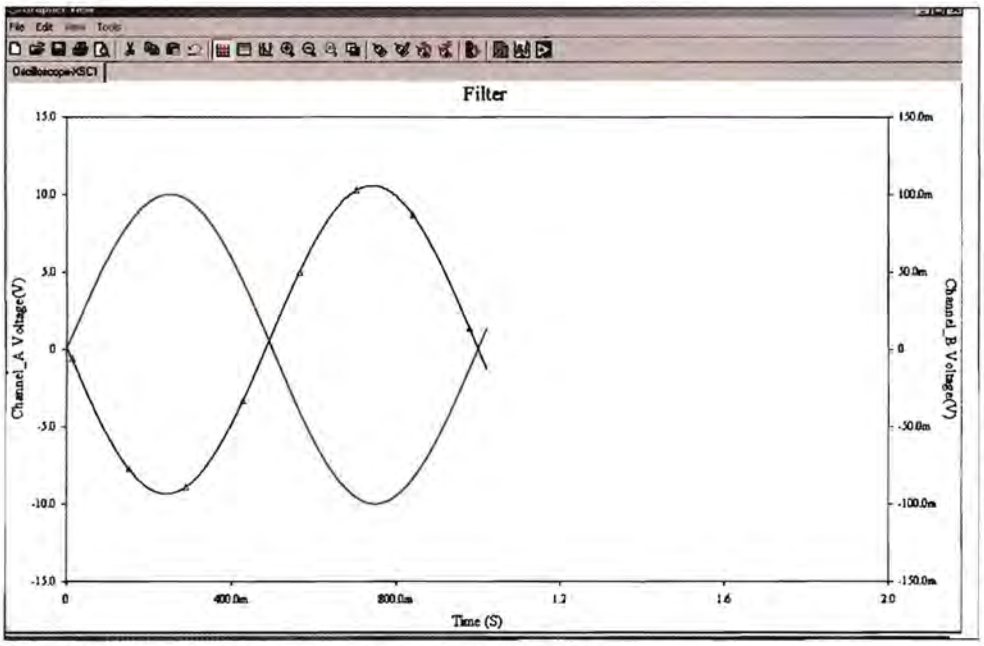
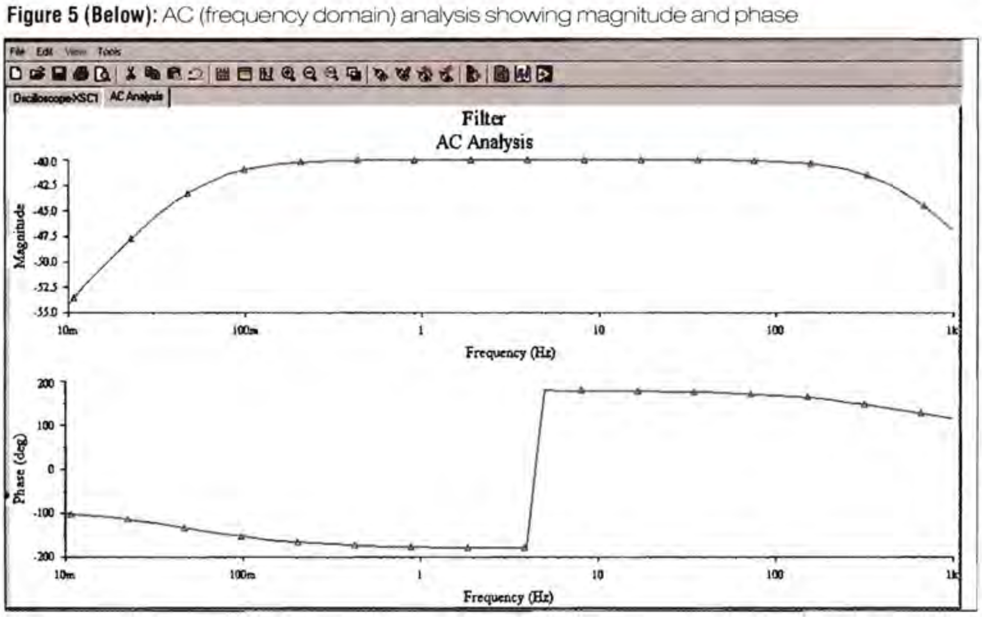


Figure 4 (Above): Enhanced graphical output from oscilloscope

Figure 5 (Below): AC (frequency domain) analysis showing magnitude and phase



Clicking on the button with the lightning symbol below the help menu brings down a dialogue box with simulation parameters. Ensure that you select the correct node for simulation – in this case, node 3, and then start the simulation. Let the simulation run for long enough to display one second on the scope.

As expected, the Channel A trace is clearly visible but the Channel B trace is almost flat. In other words, there is significant attenuation between the input and the output and, therefore, Channel B has to be scaled. The best way to do this is to drop down a graph window from the next button along, which can be made any size up to full screen.

In **Figure 4**, I have sized the window so as to leave the menu bar accessible, because from the tools menu, I can select an area to copy into the Windows clipboard to produce the JPEGs that I have used here.

By pressing the button with black/white squares, I have reversed the background colour from black to white. Then I changed the Channel B trace colour from red to blue and scaled the Channel B axis on the right – all from the properties button, the one which shows a pencil on a tag.

As expected, the Channel B shows the inverting output of the filter, but we are really interested the frequency domain behaviour of the circuit. We could add a sweep generator and a spectrum analyser or bode plotter, but now that we have introduced the grapher view, I find it easier to produce an AC analysis. This is done by reducing the size of the analyses window to expose the various buttons at the top of the main window, and clicking on the drop-down arrow next to the graph window button.

Selecting AC analysis from the list of available analyses (see shaded box) will produce a magnitude and phase diagram as shown in **Figure 5**. Note how a new AC analysis tab has been added at the top left of the graph window.

Selecting the phase section of the diagram and using the scissors button to cut it, leaves only the magnitude section. The left axis can be selected from the properties dialogue box as linear, logarithmic, decibel or octave.

I have chosen decibel as shown in **Figure 6** because it is easier to find the -3dB points from the drop down cursors, activated by clicking on the button to the left of the zoom (+) button.

The cursors show the -3dB points to be at 50mHz (0.05Hz) and 500Hz respectively, as borne out by the equations above. Multisim passes the first test with flying colours.

Test 2 – Time domain modelling

Now let us look at our next circuit, and this time we are going to use a real life op amp rather than a virtual one, to build a 0.5Hz square wave oscillator taken from page 17 of Texas Instruments's application note for the TL071 op-amp and reproduced here as **Figure 7**.

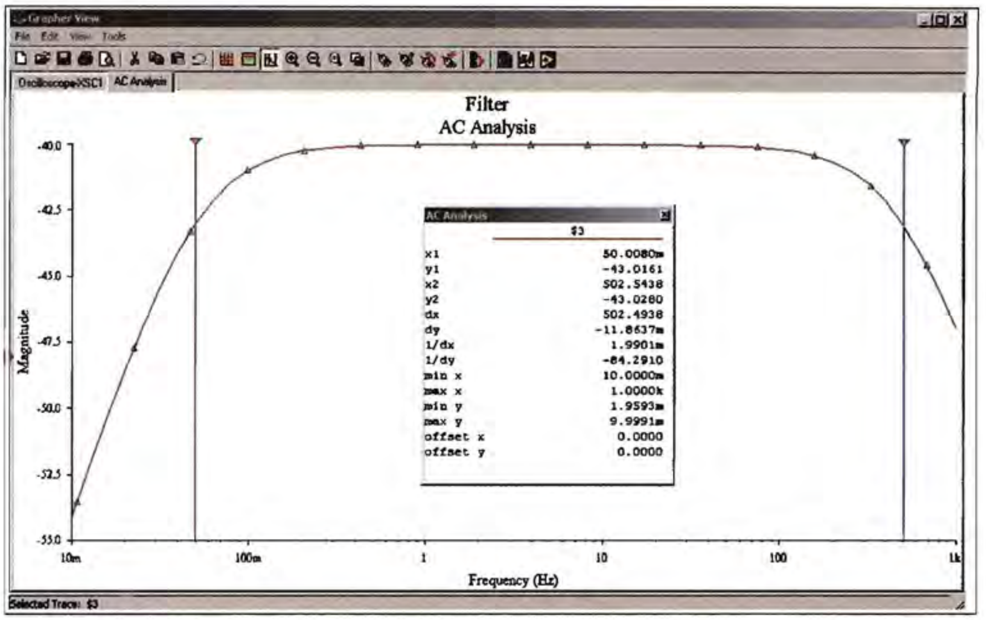
We need to select this op-amp from the components on the left, the fifth button along, called 'place analog', and then place the rest of the components as before.

Now click on the analyses drop down menu and select transient analysis, and in the dialogue box, enter the simulation time as 120 seconds. Do not forget to enter the correct node for analysis as well. Running the simulation yields an output as shown in **Figure 8**.

You can see that the circuit starts to oscillate after about 96 seconds and cycles roughly every two seconds as a square wave, as expected. I say 'roughly' because if you zoom into the area of the first few oscillations, the cycle time is slightly less than two seconds.

Perhaps it is not the most precise of oscillators, because the cycles are not quite square either. It could also be a problem in the Spice engine of Multisim, but somehow I doubt it. So, Multisim sails through the second test.

I have tried to keep down the number of screen grabs for this article, and now with eight, I feel as if I have barely scratched the surface.



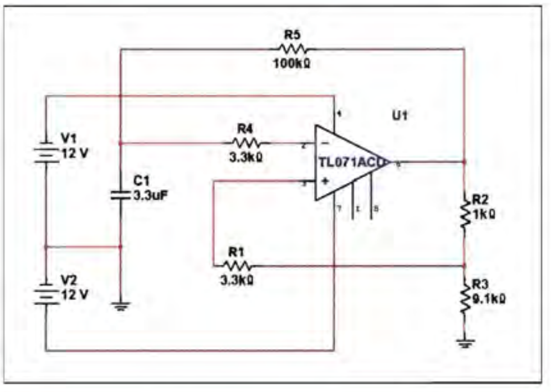


Figure 6 (Above): Magnitude-only diagram with measurement cursors

Figure 7 (Centre): 0.5Hz square wave oscillator based on the TL071 op-amp

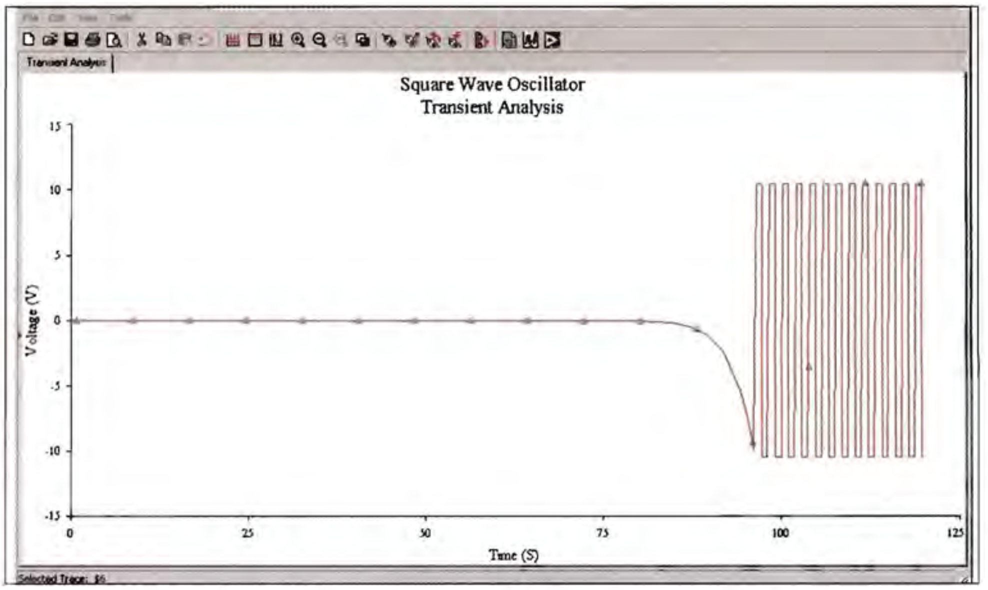
Figure 8 (Below): Square wave simulation output from the oscillator

Latest version

Multisim 8 includes 'real' Virtual Instruments from Tektronix. It also includes Dynamic Probes – an unlimited number of probes can be placed on the schematic to annotate a circuit with real-time, dynamic values such as current and voltage.

Simulation Profiles, another previously unavailable function, allows the user to configure, save and re-use complete Spice simulation parameter setups. Tool-tip Style Notes allow notes to be attached to any point in the circuit.

Design notes, annotations and comments from reviewers automatically pop-up when rolling the mouse over a circuit. The design engineer may toggle between all notes, no notes or notes made by a specific individual. Both Simulation Profiles and Tool-tip Style Notes are new functions that help Electronics Workbench users gain a competitive advantage by exceeding their time-to-market goals.



Other Multisim benefits include:

1. New Model Makers: this functionality supplements Multisim's extensive component library, facilitating the rapid creation of even more types of component models from data book values (such as transformers, converters, motors and others).

2. A New Worst-Case Algorithm: this function tests circuits under the worst expected conditions, incorporating the statistical variations of real world component values during the upfront simulation stage.

3. New Amplifier Circuit Wizard: this feature automatically creates circuitry that matches user-supplied parameters. This ability, like the other existing Multisim wizards, stems from the tight integration of Multisim's schematic capture and simulation features.

The capture engine uses the simulation functionality to 'look ahead' and create circuitry that behaves as specified by the user.

When using a wizard you do have to have prior knowledge of the kind of parameters that need to be entered, because this is not something for just having a go.

Conclusion

Throughout history, there have been tussles taking place between engineers and scientists. The latter can be described as analysts versus the former, the experimentalists.

The analysts have always insisted on rigorous mathematical proof of functional relationships. Oliver Heaviside ran into that problem over a century ago. He did not rigorously prove, but rather carefully checked, his results.

He pursued what he called 'experimental mathematics'. He instinctively invented a transform method for avoiding laborious differential calculus, by reducing the whole process to simple algebra.

He said: "Mathematics is an experimental science and definitions do not come first but later on."

The proof is not disputed today and did not come later, but about a century before with Laplace, who had mathematically established the theoretical relationship in the requisite analytically closed form. This, together with refinements to Heaviside's original transform methods, became the Laplace transform.

The point I'm trying to make is that you cannot sit down and think too much about how you are going to use a Spice simulator. You do have to try things out and see their effects when you change simulation parameters.

Try out the parameter sweep, for example, when you want to view the damping effect of a resistor on a step input function. Analysts and scientists would apply an equation for critical damping, but by a process of narrowing down the range of resistor values in the sweep, you can get a good enough answer for many applications.

Or for multiple component values you may want to try out the Monte Carlo method. Go on, have fun!

Analyses available

DC Operating Point Analysis	Transfer Function Analysis
AC Analysis	Worst Case Analysis
Transient Analysis	Pole Zero Analysis
Fourier Analysis	Monte Carlo Analysis
Noise Analysis	Trace Width Analysis
Distortion Analysis	RF Analyses
DC Sweep Analysis	Nested Sweep Analyses
DC and AC Sensitivity Analyses	Batched Analyses
Parameter Sweep Analysis	User Defined Analyses
Temperature Sweep Analysis	RF analyses

PROS AND CONS

- ✔ Easy schematics capture
- ✔ Mature, tested product
- ✔ Virtual Instruments and comprehensive analysis suite
- ✔ Simulated 'real' Agilent and Tektronix instruments
- ✔ Co-simulation with VHDL
- ✔ Circuit Wizards
- ✔ Integration with National Instruments's LabVIEW
- ✘ Can't read in older EWB files. I tried to import some but the wires were broken.
- ✘ Fewer proprietary component Spice models than earlier versions, although the storage previously taken up by ever-expanding model libraries probably made this inevitable.
- ✘ User guide. Tutorial in the user guide is a bit intimidating. New users would find a smaller circuit easier to cut their teeth on. Also there appears to be a section missing on the tools menu after Page 5-31 in the PDF version.
- ✘ Requirement for release code to launch product. This was a bit error-prone and cumbersome, and could be off-putting for first-time users.

SUGGESTED IMPROVEMENTS

- Instruments. The oscilloscope has black background, which I couldn't change, nor could I change the size of the window. Although you can pull down a larger graph, after completing the simulation and change the settings to make it more visible, it would be nice to see a larger window during simulation.
- Screen grab. When I referred to dialogue boxes, you may wonder why I did not show any of them. This is because you cannot access the screen grab function while a dialogue box is open.

the ELECTRICAL industry awards 2005

20th October • National Motorcycle Museum • Birmingham

The Electrical Industry Awards is a prestigious event that recognises the achievements of all who work in the diverse electrical industry. Organised by the industry's leading magazines Electrical Review, Electrical Times and European Power News, the awards are presented to companies that have excelled during 2005 and are your chance to prove to your employees, competitors, suppliers and customers that you are the best in your sector.

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I WISH TO ENTER THE FOLLOWING CATEGORY *(tick one box only*)*

- ☐ Electrical Contractor of the Year
- ☐ M&E Contractor of the Year
- ☐ Innovative Product of the Year
- ☐ Building Services Product of the Year
- ☐ Automation Project of the Year
- ☐ On-Site Power Product of the Year
- ☐ Energy Efficiency Project of the Year
- ☐ Wholesaler of the Year
- ☐ Best Marketing Campaign
- ☐ Test & Measurement Product of the Year
- ☐ Power Product of the Year
- ☐ Electrical Software Product of the Year
- ☐ Best Training Programme
- ☐ Lighting Product of the Year
- ☐ Lighting Project of the Year
- ☐ Safety Product of the Year
- ☐ Environmental Awareness Product of the Year
- ☐ Employer of the Year

**If you wish to enter more than one category, please use a separate form (photocopies acceptable).*

The 2005 categories:

- Electrical Contractor of the Year
- M&E Contractor of the Year
- Innovative Product of the Year
- Building Services Product of the Year
- Automation Project of the Year
- On-Site Power Product of the Year
- Energy Efficiency Project of the Year
- Wholesaler of the Year
- Best Marketing Campaign
- Test & Measurement Product of the Year
- Power Product of the Year
- Electrical Software Product of the Year
- Best Training Programme
- Lighting Product of the Year
- Lighting Project of the Year
- Safety Product of the Year
- Environmental Awareness Product of the Year
- Employer of the Year

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PICmicro: Microcontroller CCP and ECCP

The Capture, Compare and PWM (CCP) modules that are found on many of Microchip's microcontrollers are used primarily for the measurement and control of time-based pulse signals. The Enhanced CCP (ECCP), available on some of Microchip's devices, differs from the regular CCP module in that it provides enhanced PWM functionality – namely, full-bridge and half-bridge support, programmable dead-band delay and enhanced PWM auto-shutdown.

The ECCP and CCP modules are capable of performing a wide variety of tasks. The tips below describe some of the basic guidelines to follow when using these modules, as well as suggestions for practical applications. Additional information can be found at www.microchip.com

TIP 1: Periodic Interrupts

Generating interrupts at periodic intervals is a useful technique implemented in many applications. This technique allows the main loop code to run continuously and, then, at periodic intervals, jump to the interrupt service routine to execute specific tasks, such as read the ADC, for example.

Normally, a timer overflow interrupt is adequate for generating the periodic interrupt. However, sometimes it is necessary to interrupt at intervals that cannot be achieved with a timer overflow interrupt. The CCP configured in Compare mode makes this possible by shortening the full 16-bit time period.

Example Problem:

A PIC16F684 running on its 8MHz internal oscillator needs to be configured so that it updates a LCD exactly 5 times every second.

Step #1: Determine a Timer1 prescaler that allows an overflow at greater than 0.2s

a) Timer1 overflows at: Tosc*4*65536* prescaler

b) For a prescaler of 1:1, Timer1 overflows in 32.8ms

c) A prescaler of 8 will cause an overflow at a time greater than 0.2s 8 x 32.8ms = 0.25s

Step #2: Calculate CCPR1 (CCPR1L and CCPR1H) to shorten the time-out to exactly 0.2s

a) CCPR1 = Interval Time/(Tosc*4*prescaler) = 0.2/(125 ns*4*8) = 5000 = 0xC350

b) Therefore, CCPR1L = 0x50 and CCPR1H = 0xC3

Step #3: Configuring CCP1CON

The CCP module should be configured in Trigger Special Event mode. This mode generates an interrupt when the Timer1 equals the value specified in CCPR1L and Timer1 is automatically cleared (1). For this mode, CCP1CON = 'b00001011'.

Note 1: Trigger Special Event mode also starts an A/D conversion if the A/D module is enabled. If this functionality is not desired, the CCP module should be configured in "generate software interrupt-on-match only" mode (i.e,CCP1CON = b'00001010'.) Timer 1 must also be cleared manually during the CCP interrupt.

TIP 2: Modulation Formats

The CCP module, configured in Compare mode, can be used to generate a variety of modulation formats. The following figures show four commonly used modulation formats:

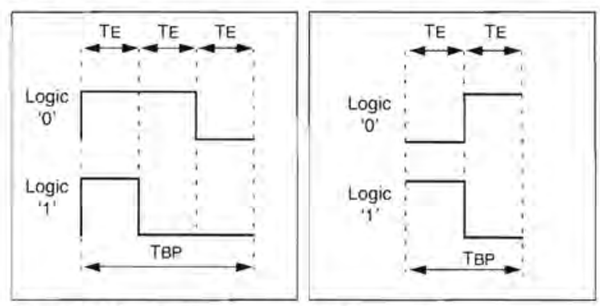


Figure 1a (above left) Pulse-Width Modulation

Figure 1b (above right): Manchester

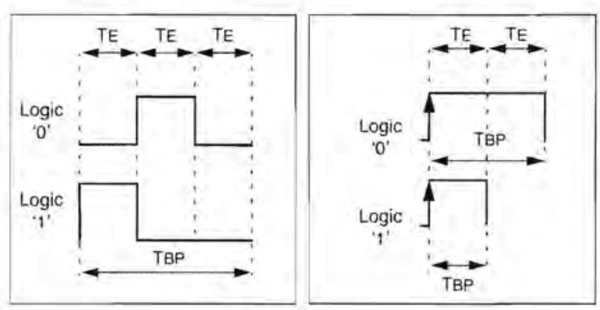
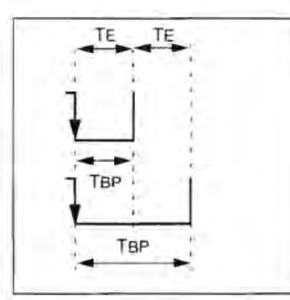


Figure 2a (above left): Pulse-Position Modulation

Figure 2b and 2c (above right and opposite): Variable Pulse-Width Modulation



The figures show what a logic '0' or a logic '1' looks like for each modulation format. A transmission typically resembles an asynchronous serial transmission consisting of a Start bit, followed by 8 data bits and a Stop bit.

TE is the basic timing element in each modulation format and will vary based on the desired baud rate. Trigger Special Event mode can be used to generate TE (the basic timing element). When the CCPx interrupt is generated, the code in the ISR routine would implement the desired modulation format. Additional modulation formats are also possible.

TIP 3: Generating the Time Tick for an RTOS

Real Time Operating Systems (RTOS) require a periodic interrupt to operate. This periodic interrupt or "tick rate" is the basis for the scheduling system that RTOS employ. For instance, if a 2ms tick is used, the RTOS will schedule its tasks to be executed at multiples of the 2ms. An RTOS also assigns a priority to each task, ensuring that the most critical tasks are executed first. **Table 1** shows an example of these tasks, the priority of each task and the time interval that the tasks need to be executed.

Table 1: Tasks

Task	*Interval*	*Priority*
Read ADC input 1	20ms	2
Read ADC input	2 60ms	1
Update LCD	24ms	2
Update LED array	36ms	3
Read Switch	10ms	1
Dump Data to Serial Port	240ms	1

The techniques described in TIP #1 (Periodic Interrupts) can be used to generate the 2ms periodic interrupt using the CCP module configured in Compare mode. For more information on RTOSs and their use, see Application Note AN777, Multitasking on the PIC16F877 with the Salvo RTOS.

TIP 4: 16-Bit Resolution Pulse Width Modulation (PWM)

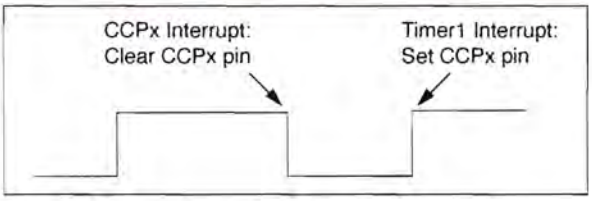


Figure 4: 16-bit resolution PWM

1. Configure CCPx to clear output (CCPx pin) on match in Compare mode (CCPxCON <CCPSM3: CCPxM0>).
2. Enable the Timer1 interrupt.
3. Set the period of the waveform via Timer1 prescaler (T1CON <5:4>).
4. Set the duty cycle of the waveform using CCPRxL and CCPRxH.
5. CCPx pin when servicing the Timer1 overflow interrupt(1).

CCPx Interrupt:
Clear CCPx pin
Timer1 Interrupt:
Set CCPx pin

Note 1: One hundred percent duty cycle is not achievable with this implementation due to the interrupt latency in servicing Timer1. The period is not affected because the interrupt latency will be the same from period-to-period as long as the Timer1 interrupt is serviced first in the ISR.

Timer1 has four configurable prescaler values. These are 1:1, 1:2, 1:4 and 1:8. The frequency possibilities of the PWM described above are determined by the equation:

FPWM = FOSC/(65536*4*prescaler)

For a microcontroller running on a 20MHz oscillator (FOSC), this equates to frequencies of 76.3Hz, 38.1Hz, 19.1Hz and 9.5Hz for increasing prescaler values.

TIP 5: Sequential ADC Reader

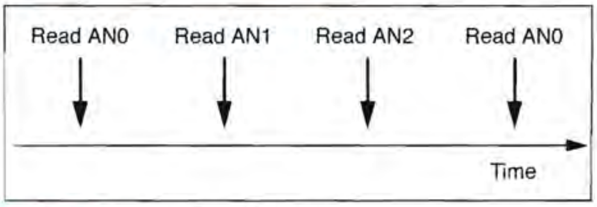


Figure 5: Sequential ADC reader

Trigger Special Event mode (a sub-mode in Compare mode) generates a periodic interrupt in addition to automatically starting an A/D conversion when Timer1 matches CCPRxL and CCPRxH. The following example demonstrates how to sequentially read the A/D channels at a periodic interval.

Example:

Given the PIC16F684 running on its 8MHz internal oscillator, configure the microcontroller to sequentially read analogue pins AN0, AN1 and AN2 at 30ms intervals.

Step #1: Determine Timer1 prescaler

a) Timer1 overflows at: TOSC*4*65536* prescaler.

b) For a prescaler of 1:1, the Timer1 overflow occurs in 32.8ms.

c) This is greater than 30ms, so a prescaler of 1 is adequate.

Step #2: Calculate CCPR1 (CCPR1L and CCPR1H)

a) CCPR1 = Interval Time/(TOSC*4*prescaler) = 0.030/(125ns*4*1) = 6000 = 0xEA60

b) Therefore, CCPR1L = 0x60, and CCPR1H = 0xEA

Step #3: Configuring CCP1CON

The ECCP module should be configured in Trigger Special Event mode. This mode generates an interrupt when Timer1 equals the value specified in CCPR1. Timer1 is automatically cleared and the GO bit in ADCON0 is automatically set. For this mode, CCP1CON = 'b00001011'.

Step #4: Add Interrupt Service Routine logic

When the ECCP interrupt is generated, select the next A/D pin for reading by altering the ADCON0 register.

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Adjustable crossfeed circuit for headphones

When listening to speakers, the right ear can hear the left speaker and vice versa. The duplication of this effect prevents the in-head localisation phenomenon while listening to headphones. The signals that are cross fed are passed though filters that provide some low-pass filtering and delay in the signal path from one channel to the other. One of the earlier circuits was suggested by Linkwitz [1] and explained in great extent. After that, other circuits were proposed [2-6] in attempt to emulate the same natural crossfeed. It turns out that they have rather different frequency responses.

The survey, composed from twelve different circuits [1-6] is shown in **Figure 1**. The low-pass filter is varied from 200Hz to 1000Hz and low frequency attenuation as varied from 0dB to 12dB.

It seems interesting to build a circuit, which crossfeeds the input signals, while the low-pass filter and crossfeed attenuation are adjustable. One of the possible circuits is shown in **Figure 2**. This circuit does not have the direct signal high-frequency rise, which is inherent to the most of realisations. This high frequency boost (up to 6dB) can be too bright.

Crossfeed can be adjusted by frequency control VR1, VR4 and level control VR2, VR5. It was found that feeding the circuit only from one stereo channel during adjustment (by input push-button SW1) helps placing the position of sound image. Both frequency and level controls allow changing the spatial width of the solo musical instrument (e.g. piano) or soloist. The crossfeed can be disabled by the switches SW2, SW3 for true binaural recordings or other surround sound sources.

The op-amps can be any type, unity-compensated, as they work with low-frequency spectrum and their load is insignificant for generating perceptible distortion. Any of the existing phone amplifiers can be used after volume control.

Dimitri Danyuk,
Kiev
Ukraine

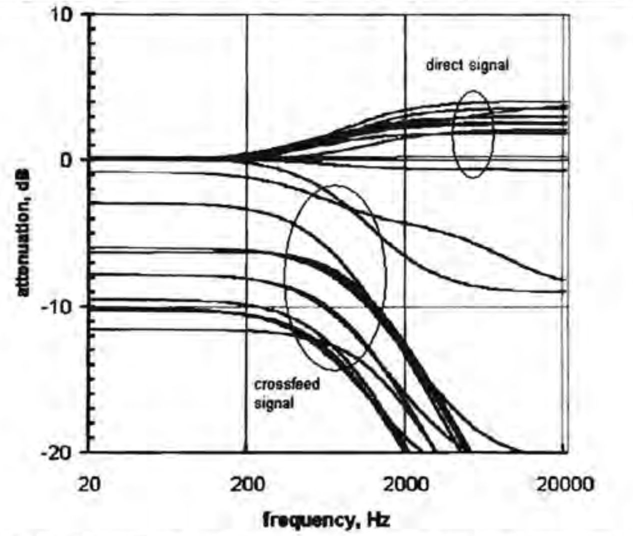
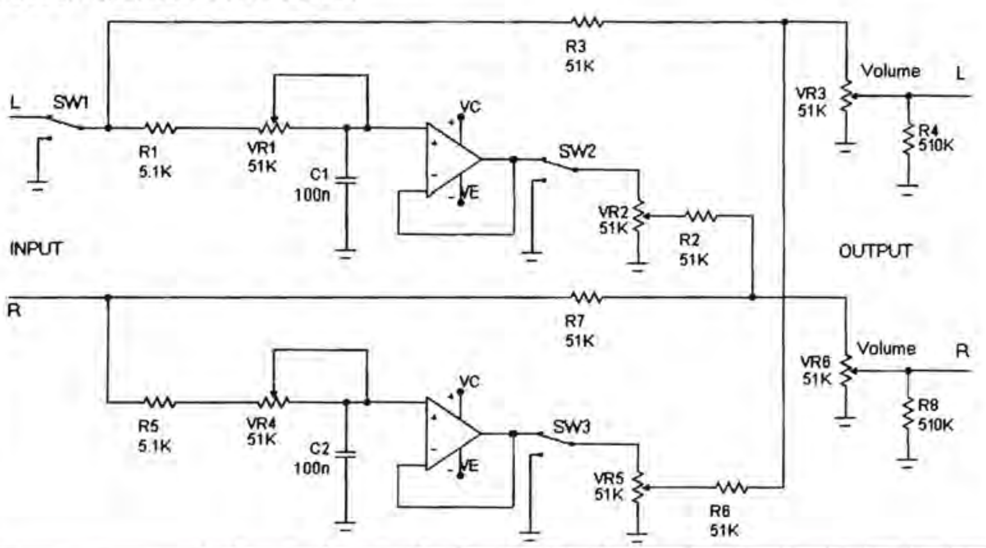


Figure 1: The frequency responses for twelve various crossfeed circuits [1-6]

Figure 2: Adjustable crossfeed circuit



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Simple handheld controller for servo applications

When my son and I are working with his radio-controlled model airplane, I have found that there are often times when it's not possible to set up the servo in his plane because it would interfere with the other flyers who are using the same radio frequency. I have made a simple handheld controller that can be used to adjust the position of the servo inside the model plane, without using the transmitter. This device makes it possible to set the servo to the 0 point and make sure that the plane is working correctly, without the problem of interfering with nearby fliers. (The plane will still need to be checked with the radio before flying.) The servo tester works with any Futaba compatible servo, except the digital ones. The servo tester is also useful for any project where servos are used. For example, in the building of a robot, a servo can be used to help set up your linkage without using a computer each time.

Circuit idea

I began with the servo tester diagram available at www.kronosrobotics.com web page. I used this tester and added a small modification – a button which can be pressed to make the servo go to its 0 point. I built the servo tester using the Athena Microcontroller by Kronos Robotics & Electronics.

Before using the Athena chip, it's necessary to build a port adapter. This adapter converts the voltage of the RS232 port on a computer to the correct levels for the microcontroller chip. I was able to order an inexpensive kit from Kronos Robotics, with a part number EZ232. The kit is indeed 'EaZy' to build with.

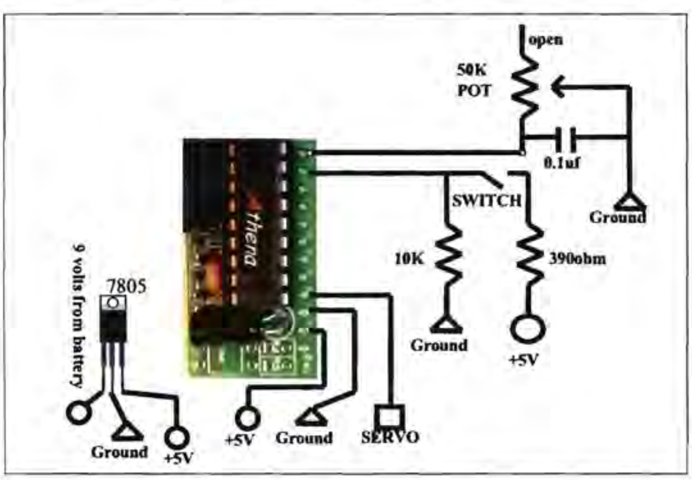
Next, it is necessary to order the Athena carrier board. On assembling the Athena carrier board just follow the assembly instructions, except for the headers. Instead of the 5-pin male, I changed it to a 5-pin female header. Now the EZ232 plugs directly into the Athena carrier. And, the spot where the 12-pin male header gets soldered in, I left empty. For the Athena's power, I used a 9V battery and then a 7805 voltage regulator. For the hook up from the Athena to the servo, I use a servo extension wire and cut the plug off the end that does not hook up to the servo.

The servo has three wires, usually red, black and white. The red is the plus, the black is minus (or ground) and the white is for the signal that comes from the Athena. The servo uses 4V8 to 6V. The signal is a 1-2ms pulse every 20ms. By changing the 1ms to 2ms, it changes the direction that you want the servo to go. A 1ms5 pulse would put the servo at 0 degrees. All of this timing is done with the Athena chip, which has built-in commands to talk to the servo.

Operation

I have two push-button switches and one potentiometer. One button is for the power. If you press this button and hold it, you can use the potentiometer to set the angle you want or check the movement by turning the potentiometer back and forth. The other button is for making the servo go to a 0 point. This can be done by pressing both buttons simultaneously. This rotates the servo to the 0 point. To keep it that way, just release the power button first.

Once you have finished building the circuit you are ready to program the Athena microcontroller. The programming language is just like Basic and is free from www.kronos-robotics.com. On one of my computers it came up instantly, but the other one took a moment (old computer), so loading times may vary. On the computer that is using the programming language to program the microcontroller you cannot use that RS232 port for anything else.




```
'Program
'athena

dim xpot
dim x
dim switch
output 8
input 1 ' input for the switch
loop:
switch = inp1

if switch = 0 then ' check to
see if the switch was pressed

 x=145
 else
  pot 0,2,xpot
  x= xpot +80
endif
servo 8, x
'print x, " ",switch
pause 22

goto loop
```

Program notes

The 145 in the program is the number I found worked best for me to send to the servo to move to the 0 point. (The Athena has lots of ports open, which is useful for adding additional buttons and features, such as making the servo move to a specific angle.) The 80 in the program is the adjustment for the potentiometer to make the number that is being sent to the servo that gives the best control. The pause in the program is to slow down some of the commands that are being sent to the servo.

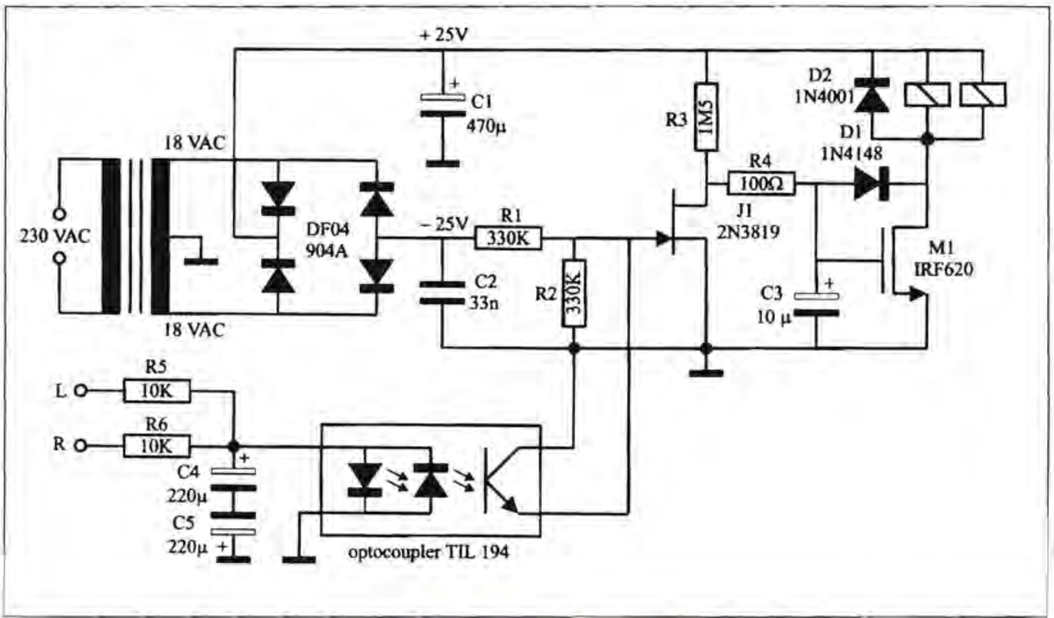
Robert Knoblauch
Piscataway
US

Hybrid muting relay

Most of today's transistor power amplifiers suffer from transients during turn-on and turn-off. A muting relay is primarily intended to protect loudspeakers against these transients. It is also important to note that (for loudspeakers destructive) DC faults can occur. For instance, in DC coupled amplifiers, if in dual-supply circuits one supply-rail fails. With only a small number of additional components, DC protection can be incorporated as well.

Muting relay circuit design is often based on bipolar transistors and diodes. However, specification demands for various circuit parts are quite different, so, optimal matching of the type of semiconductor to the specific behavioural demand of the circuit part is important.

For capacitor discharge and to energise the relays, a voltage-controlled switch is needed. Field Effect Transistors (FETs) are preferable for this function, rather then bipolar transistors, because the DC input current of bipolar transistors is disturbing the circuit function. Moreover, FETs have the advantage that we can make a choice between normally 'on' and normally 'off' devices, which is very useful in muting relay design.



Circuit description

This muting relay is based on best-choice component considerations for each circuit part. This optimisation results in selecting a JFET for timing capacitor discharge, a Mosfet to energise the relays and an optocoupler for DC protection.

For two reasons the circuit (Figure 1) has its own rectifier/capacitor part. Firstly, in spite of DC errors on the supply rails the DC protection function must act adequately. Secondly, the capacitance of C1 and C2 can be optimised for muting relay needs.

With AC power switched off, the circuit is well defined, with J1 being a normally 'on' device guaranteeing zero DC voltage at the timing capacitor C3. Both relays are not energised since M1 is a normally 'off' device. Applying rectified AC power results in a positive voltage on C1 and a negative voltage on C2. The positive voltage enables C3 to charge, forth energising the relays, whereas the negative voltage causes J1 to switch off. Voltage divider R1/R2 is used to reduce the negative voltage to protect J1 against gate-source breakdown. Besides the serial function of resistor, R1 is needed for the DC protection part of the design. This function will be discussed later.

When J1 is switched off, capacitor C3 charges through R3 and R4 until M1 turns on, energising the relays. With M1 switched on, clamping diode D1 takes over the current through R3 and R4, causing the voltage on C3 to clamp on a relatively low value. The importance of this phenomenon is firstly to achieve a short dropout time and, secondly, to protect M1 against destructive gate-source voltages.

Switching off AC power causes to discharge C2 through R1 and R2. The dropping gate-source voltage switches on J1, which in turn starts to discharge C3. R4 is a current limiting resistor. As a result M1 is turned off, de-energising the relays.

The reverse diode D2 in parallel to the relay coils prevents M1 from being damaged by inductive spikes created when the coil is suddenly de-energised.

For DC protection, the use of a so-called AC input optocoupler is beneficial. The AC input circuit provides a symmetrical threshold without the need for additional components. A symmetrical threshold is needed to cope with positive as well as negative DC voltages. In order to prevent false triggering on bass signals, so to suppress audio signals from the input, a RC low-pass filter (R5/R6-C4/C5) is needed at the input. Back-to-back electrolytic capacitors are used as a bipolar capacitor.

The electrical isolation between input and output of optocouplers enables the output transistor to adapt DC currents from nodes in the circuit on arbitrary DC levels.

When the optocoupler is activated by a DC offset voltage of either polarity, the output transistor of the optocoupler takes over the current through R1, causing the voltage on C3 to drop to approximately zero. As a result, J1 turns on, M1 turns off and the relays are de-energised. This condition will remain until the DC offset is removed.

Measurement results

The hybrid relay prototype circuit has been mounted on a PC board (Figure 2). The relays used are Amplimo loudspeaker relays, especially designed for the switching of loudspeakers. A standalone mains transformer is used for measurements. Note that the use of a standalone transformer makes the muting relay independent from the amplifier power supply transformer's AC voltages.

The relay pull-in time is approximately 2s, long enough for a silent start-up. The dropout time is about 40ms. The voltage drop at the electrolytic reservoir capacitors from the power amplifier are too small to create audible transients in that time interval. When the muting relay is switched 'on' immediately after it was switched 'off', the pull-in time is still 2s, illustrating the benefit of using a JFET for capacitor discharge.

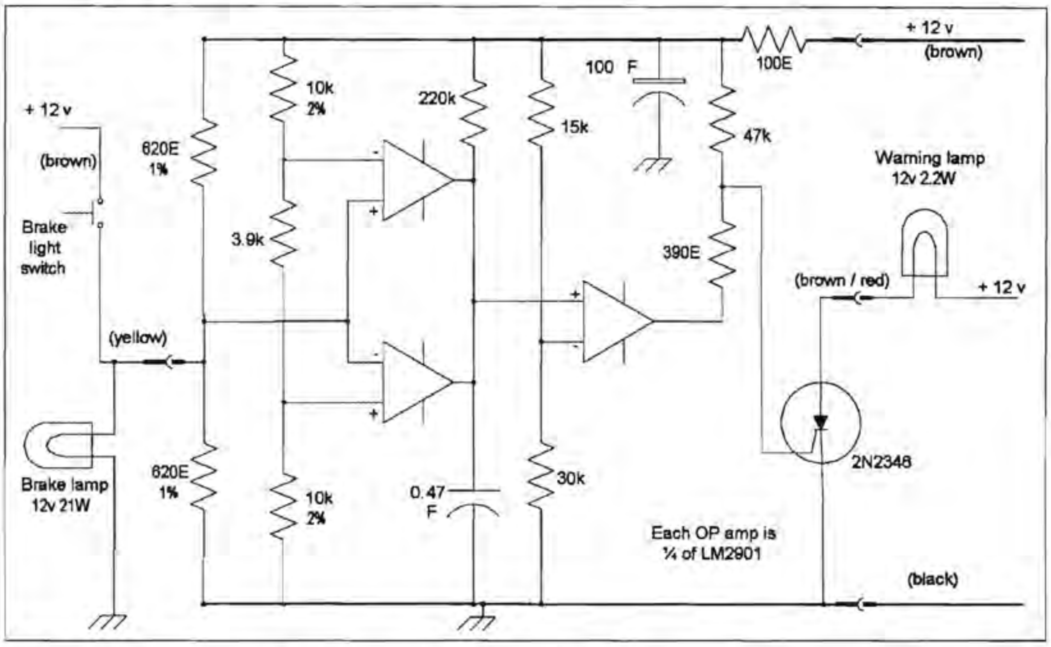
The trigger level DC offset is approximately ±2V. Full power (18VAC) low frequency limit is 5Hz.

Wim de Jager
Enschede
The Netherlands

Acknowledgement:
The author would like to express his thanks to Rien van Leeuwen for helpful comments.

Technical support:
The relays and the printed circuit board are obtainable from Amplimo Vossenbrinkweg 1, 7491DA, Delden, The Netherlands, tel.+31-74-376365, fax +31-74-3763132 www.amplimo.nl, e-mail: info@amplimo.nl

Lamp check circuit



During the restoration of a classic motorcycle of US origin, a unit was required to check the brake lamp circuit and drive the indicator lamp. Unlike most vehicle checking circuits that monitor the lamp current (and for which dedicated ICs are available), this wiring loom is built to monitor the lamp voltage or resistance.

The first two comparators are set as a window comparator, with the window set to half-rail voltage ±1V (10k + 3.9k + 10k). Under normal operation the brake lamp holds the comparator input near to ground (lamp 'off') or the battery pulls the voltage nearly to rail voltage (lamp 'on'). In these conditions, the output of the window comparator is 0. During the operation or release of the brake switch, the voltage will pass through the window area but the transit time will be too short for the integrator (220kΩ + 0.47µF) to react.

If the lamp fails, the window comparator input will rise to half-rail voltage set by the two 620E resistors and remain there, whilst the comparator output will switch to open circuit. The 0.47µF capacitor will charge through the 220kΩ resistor, reaching the threshold of the third comparator in a time approximately equal to the time constant (0.1s). At this point, the output will go high, allowing the thyristor to switch on via the 47kΩ gate resistor.

The thyristor, hence the warning lamp, will then remain on until the power is removed from the circuit.

The circuit components are not critical, provided that the fail input voltage is well within the "window" voltages. The comparators must be capable of having their outputs ORed together and the 47kΩ thyristor gate resistor may have to be adjusted for the gate sensitivity of the thyristor used. During testing, some spurious triggering of the thyristor was experienced from noise on the vehicle's circuits. This was cured by adding the power line decoupling with 100E + 100µF and changing to a less sensitive thyristor.

The circuit cannot indicate a fail during the period when the brakes are applied, but as this is a very low proportion of the running time of the vehicle, it is not considered a problem.

The prototype was built very easily on to a piece of Veroboard 18 x 18 holes.

Chris Gardiner
Chelmsford
UK

Send new circuit ideas to:
The Editor, Nnexus Media Communications, Media House, Azalea Drive, Swanley, Kent BR8 8HU
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ViaMichelin's latest GPS Navigation software is compatible with PDA platforms such as Palm OS and Pocket PC, and will turn a handheld device into an in-car navigation system with voice guidance. It comes equipped with a simple to use Plug-and-Drive DS card and, once inserted into a PDA, it's ready to go. The software has many added bonuses, such as an electronic version of the Michelin Guide, so when on the move you can always find a nice restaurant to stop off at!

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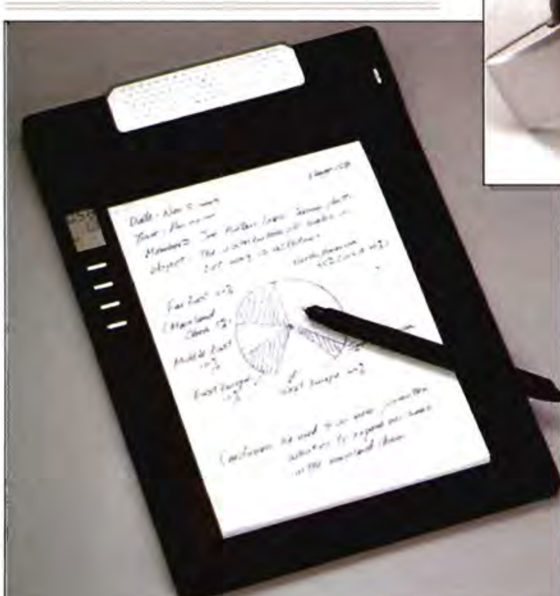

The DigiMemo digitally captures all doodles on paper, which you can then view, edit and organise in Windows. It can save up to 66 full pages of A5 hand-handwritten notes digitally via an internal flash memory. This number rises to an impressive 999 pages, if a CF card is fitted. There's an optional handwriting recognition feature to convert scribbles into Word documents. Portable and compact, the DidiMemo is a great idea for anyone who needs to take notes and keep them at hand wherever they go.

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The Microphone Book (Second edition)

John Eargle

Focal Press

Starting with a short history, John Eargle leads us through basic sound transmission, the various microphone types available, standards and specifications, connectivity and then on to accessories and studio techniques, including microphone care and maintenance, thus presenting us with a most comprehensive guide to microphone technology, applications and techniques, including wireless microphones and microphone arrays.

Many practical examples are given for studio recording, broadcast use and sound reinforcement, with help on everything from solo voice through to a full symphony orchestra.

Stereophonic and surround-sound microphone techniques are discussed and many of these have an associated CD reference, should you want to hear how this works in practice (and manage to obtain a copy of the CD referred to). The book concludes with a review of 'classic' microphones of the last 75 years and a short bibliography.

Whilst not burdening us with a lot of mathematics, there are nevertheless sufficient mathematical formulae and graphical data to explain the various characteristics under discussion, which would be of particular interest to any student wanting to grasp the physics behind the concepts.

Written by a highly respected veteran of the recording industry, this 377-page tome would be useful to anyone wanting information of the 'why' and 'how' behind choosing the right microphone for their needs. Naturally, given the background of the author, the book is biased toward the use of professional studio-grade equipment and techniques, but this does not mean that the principles under discussion cannot be related to the rather humbler equipment available to most amateur recording enthusiasts. Far from it, as modern electret designs have brought the price of 'acceptable quality' microphones down to the point where even those starting out can obtain a 'mic' worthy of the name.

Given the nationality of the author, it's perhaps not surprising that there is an American bias in the choice of microphones quoted and referenced, but, for all that, I found the book a comprehensive guide to its subject.

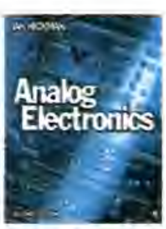
Even if you never need to record a full symphony orchestra, or a loud rock band, if you're into recording – you're certain to gain something from John Eargle's handy tome.

Graham Field

Analog Electronics (Second Edition)

Ian Hickman

Elsevier



I have many books on my shelves that claim to be "the" ultimate book on analogue electronics, but all have either proved to be too theoretical or too practical, so it was with great interest that I received Ian Hickman's book "Analog Electronics".

I found it an absorbing read. Having come across Ian's articles in Electronics World magazine over many years, it was pleasing to have his knowledge distilled into ten chapters of innovative design ideas and clear explanations of the fundamentals of analogue circuit design and calculation.

In the front of the book is a quote that nicely sums up this book: "Digital is easy. Analogue... that's professional". It will answer those troublesome questions about basic analogue theory and design philosophy, as well as offering genuinely practical design ideas.

I showed the book to students who were starting at HNC/HND, BTEC Higher National Engineering scheme and degrees and they thought, in many respects, it was a better source of information than the books that were on the reading list for their current courses.

The book, being concerned with analogue circuitry, does not deal with digital signal processing, but with the interfaces between the digital and analogue circuits such as A/D and D/A converters. There are devices that are intermediate in form and deal with the delay of analogue signals in digital form; these are covered in some detail.

The schematics give circuit values and semiconductor types, so it would be easy to reproduce should the need arise, although some of the circuits date back to the dawn of the semiconductor age and the values of some passive components are now very non-standard. As far as the thermionic valves is concerned there are just three mentions in the whole book. It is nice see design trends so well documented.

I found the layout of the text and chapters excellent, easily leading one topic on to the next, without having to resort to the index. The only complaint I have is that it is difficult to tie the schematic and drawing to the figure numbers as they are not always close to the text that they refer to.

I found a copy of the first edition in my local library and compared the two texts. The modern revision showed many enhancements. In particular, you'll now find an updated list of references at the end of each chapter and the addition of a set of questions that will tax the brain cells of many readers.

One disappointing point, however, is that the chapter on the "Tricks of The Trade" in the first edition has now fallen by the wayside. This is a shame as it contained many gems of electronic design.

To summarise, this second edition will complement many libraries devoted to analogue electronics, adding to the knowledge base. It would also help students with more practical aspects of design in college course work.

Contents:

Passive components; Passive circuits; Active components; Audio frequency signals and reproduction; Passive signal processing and signal transmission, Active signal processing in the frequency domain; Active signal processing in the time domain; Radio frequency circuits; Signal sources; Power supplies; Appendices; Index.

Keith Parker

Harmony – who needs it? (Part 2)

By Mike Brookes

In the last issue we reviewed the problems faced by the RFID industry conforming to the newly accepted Standard EN 302 208.

In the following weeks, progress towards pan-European acceptance of a pan-European standard produced by pan-European committees has been nil. So far, just two member states have put the necessary national legislation in place to permit manufacturers to make or sell UHF RFID – despite over four years of negotiations and a Europe-wide decision in favour.

Here, we discuss the subject of the 'Newly Harmonised Frequency Bands'. The Radio Telecommunications Terminal Equipment Directive (R&TTE) was a bold move by particularly enlightened members of the European Commission to remove Type Approval regulations, often used by member states as home market protection devices. A 'New Deal' was devised by which equipment manufacturers producing radio – including Short Range Devices (SRDs) in 'Harmonised Frequency Bands' could take responsibility for self-declaration of conformity and launch new products anywhere in the EU without National Type Approval or complicated equipment marking. This freedom was given, provided that the manufacturer designed equipment conforms to a European Standard of which Part 1 is voluntary (but contains all the really useful guidance notes) and Part 2 is mandatory, complying with the essential requirements of Section 3 of the R&TTE Directive.

"Meanwhile, the USA continues to recognise the rapid developments in radio technology and modify its regulations at a rate to guarantee a competitive edge"

If you are confused at this point, you will understand why this field is so well populated by consultants who are conversant with the mystic arts of EU regulation.

It is so confusing, in fact, that a special committee called TCAM (Telecommunication Conformity Assessment and Market Surveillance Committee), consisting of CEPT Radio Administrations and a few industrial representatives, was set up to interpret the R&TTE Directive and pass on "clarifications" to all.

These are available via the 'Europa' website, which is impenetrable to all but the most determined website gurus.

The best summary document to provide enlightenment to industry is the European Radio Office (ERO) website, www.ero.dk , which holds a document entitled CEPT/ERC Recommendation 70-03, relating to the use of Short Range Devices.

Around 10% of its text gives useful instructions on EU regulations and 90% on detailing the reasons that each member state has for not complying with the agreed regulations for a "common market".

Moving on to the 'Nearly Harmonised Bands', within TCAM a sub-committee has been reviewing, for around five years at three meetings per year in Brussels, 'candidate bands for harmonisation'. These are intended to further support European industry in allowing "Class 1 Operation" the self-declare, minimum regulation for frequency bands that some – but not all – EU states can or will free up.

In five years, no actual decisions have been made but a major step has been considered where the principle of the 'Lowest Common Power' is applied. In this, to overcome the continued obduracy of some states, the ERP (effective radiated power) is determined at such a low level that objections of unwarranted interference to other services will be avoided.

Needless to say, the levels chosen are so low as to be wholly useless for the duties intended.

Meanwhile, the USA continues to recognise the rapid developments in radio technology and modify its regulations at a rate to guarantee a competitive edge, matched by Asian indifference to European regulations.

The LPRA (Low Power Radio Association) is a European trade body that represents manufacturers and users of short range devices (SRDs).

It is active in the production of SRD Radio standards and regulations.

Mike Brookes is LPRA's chairman.

A puzzling model

The results in Mr. Burkhard Vogel's article (Electronics World, May 2005, p28) are most paradoxical. First, he proves that the thermal noise of a moving-magnet cartridge cannot be properly modelled with a simple LR series network with constant resistance. In the following sections, he shows that the calculated noise for the combination of a cartridge and an RIAA amplifier is accurate to within a fraction of a dB, when the cartridge is improperly modelled as an LR series network. I must say that this had me puzzled for a while.

The frequency-dependent effective series resistance can be roughly modelled by adding a parallel resistor across the inductance. This is, basically, a simplified version of the model B.I. Hallgren used in the Journal of the Audio Engineering Society, September 1975. I've done a couple of simulations with such a cartridge model and with a simple LR series network.

To be precise, I modelled a Shure V15-III cartridge as the series connection of a 1.3388kΩ resistor and a 460mH inductance, with or without a 75kΩ resistor in parallel with the inductance. With 75kΩ, this matches Richard Visee's impedance measurements (EW, October 2003) to within +/-2 degrees of phase error for frequencies up to 20kHz. The magnitude is within +4%/-2% for frequencies up to 14kHz, within +4%/-7% up to 20kHz.

The cartridge model was loaded with 275pF in parallel with 47kΩ. The three resistors (1.3388kΩ, 47kΩ and 75kΩ) were the only noise sources that were taken into account. The simulations show that adding the 75kΩ parallel resistor influences the total noise in two ways. The resistor adds noise current, of course, but it also increases the damping of the resonance of the cartridge inductance and cable capacitance. These two effects apparently almost cancel each other.

The results for the A- and RIAA-weighted noise integrated from 20Hz to 20kHz are summarised below. The noise is listed as an RMS value and in dB with respect to the case where all three resistors are in the circuit and generate noise.

A. With 75kΩ, all resistors noisy: 487nV (0dB)

B. Without 75kΩ, all resistors noisy: 470.9nV (-0.293dB)

C. With noiseless 75kΩ, all other resistors noisy: 417nV (-1.348dB)

D. With noisy 75kΩ, 47kΩ noiseless: 361.4nV (-2.59dB)

E. Without 75kΩ, 47kΩ noiseless: 268.2nV (-5.181dB)

F. With noiseless 75kΩ and noiseless 47kΩ: 259.5nV (-5.469dB).

The differences between case A and case C indicate that the 75kΩ resistor generates a significant part of the total noise. Comparing case B with cases A and C shows that the difference in response with 75kΩ (extra damping) almost completely cancels the effect of the noise of the 75kΩ.

Cases D, E and F are the same as A, B and C, but with a noiseless 47kΩ input resistor in the RIAA amplifier (as can be approximated with combinations of series and parallel feedback). In this case, neglecting the 75kΩ causes much larger errors: 2.591dB rather than 0.293dB.

I also checked the accuracy of the 3852Hz-rule derived in my article in EW October 2003. This rule says that an RIAA amplifier should be noise-optimised at 3852Hz, because the A- and RIAA-weighted effective cartridge impedance approximately equals the impedance at 3852Hz. My calculations were much less accurate than Mr. Vogel's, because I only wanted to get a reasonable estimate of the relative importance of current and voltage noise. In particular, I neglected all loading effects and modelled the magnitude of the cartridge impedance with a simple LR series network.

The 3852Hz-rule gives an effective impedance about 15.6% higher than simulated for the combination of the cartridge and its 275pF and 47kΩ load. In the case of a bipolar input stage, optimising the noise for a source impedance that is 15.6% too high causes less than 0.05dB of increase in the noise contribution of the input transistor. As the input transistor is usually far from dominant, the deterioration in the total signal to noise ratio is even smaller. In the case of a FET input stage, there is little to optimise: you simply take a large device and bias it at a high current.

Marcel van de Gevel
The Netherlands

Nature's 'first cycle distortion'

Having read Mr. Maynard's series of articles, I am convinced that there is no such thing as "First Cycle THD".

Examining Figure 2 of the July 2004 issue, where the phenomenon is introduced, the "distorted" signal only lasts for 50µs into the first cycle and does not repeat on subsequent cycles of the input signal. The signal shown in Figure 2 is aperiodic, it is just a ramp of 6V/ms – it could be the start of a 1kHz sinewave, just as easily as it could be the start of many other waveforms. The error voltage has returned to zero a long time before the next zero-crossing, which would define the signal's frequency. To claim that the error signal consists of harmonics (i.e. integer multiples) of the frequency of the input signal does not make sense.

What Mr. Maynard has actually observed is no more that the effects of a band pass filter. If a signal is passed through a filter that removes either the high- or low-frequency components of the input signal, then it stands to reason that the output signal and the input signal will look different, but in no way is the output signal "distorted". If this was the case, then one would have to say that any filtered signal is "distorted", like the individual outputs of an electronic crossover, or the output of an equaliser.

The input signal, a "sineburst" is the product of a sinewave, $V=V_0 \sin(\omega t)$ and the Heaviside (step) function $V=H(t)$, so $V_{input} = H(t).V_0 \sin(\omega t)$. A Fourier transform will give its spectrum.

$$G(f) = \int_{-\infty}^{\infty} H(t).V_0 \sin\omega t . e^{j\omega t} dt$$

The Fourier transform of the product of two signals is the convolution of the spectra of the two individual signals, so the spectrum of the combined signal can be established from known results, as the integral $\int_0^\infty e^{j\omega t}$ is somewhat tricky to evaluate.

The spectrum of the sinewave is simply $\delta(f)$ and the spectrum of the step function is $\delta(f)+1/j\omega$, giving a spectrum for the combined signal as shown below. Although this is the spectrum of the entire sine-burst, lasting from time $t=0$ until time $t=\infty$ is already clear that the signal contains components of every frequency from zero to infinity. See **Figure 1.**

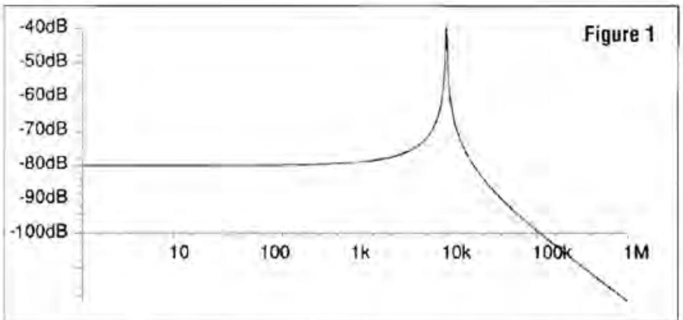


Figure 1

As only the first cycle of the sine-burst is being considered, it makes more sense to consider a sine-burst that is only one cycle long. This is again the product of two signals, the first being the sinewave and the second being a rectangular pulse of length equal to one period of the sinewave.

The spectrum of the combined signal is again the convolution of the two individual spectra, the spectrum of the rectangular pulse being:

$$G(f) = \frac{\sin(ft)}{ft}$$

The combined spectrum looks like **Figure 2**.

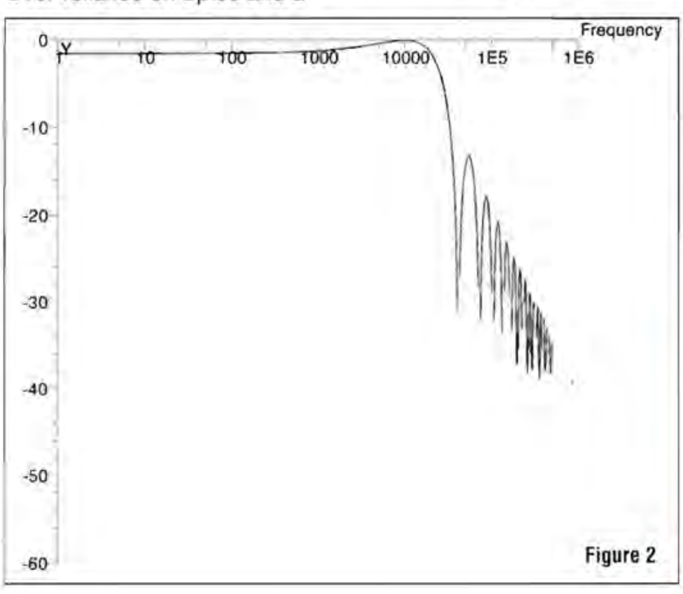


Figure 2

Its frequency response is only at -40dB at 1MHz, and extends all the way from DC to infinity. Any amplifier will, therefore, remove high- and low-frequency components from the test signal, resulting in an output signal that differs from the input signal; thus, we have a perfect explanation as to why the output signal doesn't look like the input signal, with no need to invent such spurious terms as "first cycle distortion".

The impulse response of the amplifier is simply the Fourier transform of its frequency response, and the time-domain response of the output signal is the convolution of the input signal with the impulse response of the amplifier; and it would be a whole lot easier to analyse if one were to use a rather simpler input signal than a sine-burst, such as a step-function. In fact, one could use a series of step-functions, otherwise known as a square-wave, which makes me wonder why Mr. Maynard has such strong objections to the use of square-waves for amplifier testing.

Mr. Maynard keeps asserting that we don't listen to sinewaves, although I'm sure that Baron Joseph Fourier would disagree if he was alive today; but one thing is for certain, we listen to music with our ears, we don't look at a Spice simulation of it on our computer screens. Over-reliance on Spice and a tendency to believe it rather than performing real measurements leads to faux pas like Figure 4 of the July issue, which shows a group delay of minus 800ns at 40Hz. So, the signal reaches the speaker before it leaves the amplifier? How does it do that, then?

The infinite bandwidth of the test signal also suggests that this is a signal that is highly unlikely to occur in nature. If one considers the nearest thing to a sine-burst that is likely to occur – the effect of a resonant metal bar being struck, the resonance will not start until the effect of the impact has travelled from the point of impact to the extremities of the bar and back again. The speed of sound in a solid is given by:

$$c = \sqrt{\frac{E}{\rho}}$$

where E is its Young's modulus and ρ is its density

For brass, $E=1.05\times10^{11}$Pa, and $\rho=8100\text{kg/m}^3$, giving c = 3600m/s and for a bar of 200mm in length this will take approximately 10µs, almost identical to the time constant at the front of the amplifier that Mr. Maynard was so strongly objecting to – so nature has its own "first cycle distortion"!

Mr. Maynard implies that a filter similar to that described in Figure 2 [July], with a time constant of 10µs is fitted to the input of many power amplifiers. However, with a time constant of $\tau = 10\mu s$ it has a -3dB frequency of $1/(2\pi\tau)$ which is 16kHz, so no self-respecting amplifier manufacturer would fit such a filter.

One final thought, if the transit response of the audio system is Mr. Maynard's main concern, then to blame the amplifier is missing the point.

Few manufacturers publish sine-burst test results, but this one is from Dynaudio who are one of the well respected and it can be seen that the response takes two whole cycles at 4kHz (500µs) to return, being identical to the input signal.

Ian Benton
UK

Please send your letters to:

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Azalea Drive, Swanley, Kent
BR8 8HU

e-mail:
ewletters@highburybiz.com

Capacitative touchscreen sensor

Zytronic has introduced Zypos, a highly durable, drift-free and internationally award-winning Zytouch projected capacitative technology (PCT) touch sensors. Zypos is aimed at high volume, cost-critical touch-screen applications such as in retail and gaming, for example.

Traditionally, touchscreen sensing technologies, such as capacitative, resistive and surface acoustic wave (SAW) are surface-active and, as such, more susceptible to surface variance effects during the screen's lifetime.

Capacitative sensor arrays are often subject to drift, which means that regular recalibration is required, which leads to more expensive maintenance.

Resistive touch technology is more prone to damage caused by sharp pointing devices such as a pen or the corner of a credit card. PCT does not suffer from such problems and so it is more durable and robust for various applications.

PCT is based on the principle of embedding an array of micro-fine sensing wires within a multi-layer laminated screen behind a protective front surface, ensuring that the sensing medium is well-protected from accidental and malicious damage. The sensor's thickness is 3mm; the response time it offers is less than 20ms.

www.zytronic.co.uk

New member joins the thermal team

DED Limited's Axiohm selection of thermal printers – the A600 series – has just received a new addition in the A632 system. Being made with vehicle space constraints in mind and a power supply of 12VDC, this device has already been awarded the 'e' approval for in-vehicle use. The device is only 108x147x72mm in size, has a 12VDC battery, 9-12VDC converter, supports the Windows drivers for 98/2000/XP and Pocket PC, and it can be used with a PDA as well.

The system's printing time is 55mm/s, supporting paper width of 58mm and offering battery life of up to 170 hours. The system weighs some 330 grams and it offers an RS232 interface and a choice of 24 or 40 column print width.

www.ded.co.uk

High-current PCB connectors

Camden Electronics has launched a new range of PCB connectors that can handle currents of up to 57A – the CTB77 family. They could be used in energy management and heavy duty industrial heating and ventilating applications among others.

The new connectors are moulded from UL94V0 flame retardant grey polyamide PA66 and are available in two and three pole interlocking types, with four or twelve poles.

The two and three pole types feature a double interlocking mechanism for added strength.

Specifications include voltage rating of up to 750V (UL 40A/300V) with insulation resistance greater than 50MΩ and 10mm^2 (6AWG) cable entry.

The connectors feature a zinc-plated steel clamp mechanism and guided pin alignment to ensure reliable connection. Solder contacts are 5mm tin-plated nickel, while the captive M4 screws are 7μm zinc-plated steel.

Operating temperature range is -20°C to +125°C.

www.camdenelec.com

Ultimate in wiring accessories

GET's Ultimate range of flat plate wiring accessories now offers interior décor versatility. Although renowned as the first screwless accessories to be generally available on the market in the UK, this range now comes with the option of a transparent or textured front plate that can suit any domestic or commercial interior.

The textured front plate design has a rubberised textured effect that complements to design trends.

The new designs retain Ultimate's signature ultra-slim, flat plate styling and smooth curves and incorporate all of the range's easy-fit features such as backed-out combination terminal screws for faster fixing and dual terminal colour marking for easier cable insertion. This is enhanced by Ultimate's tactile switch action, which incorporates a positive-drive switch mechanism that ensures a long and trouble-free working life. Both long and short screws are provided for maximum of installation flexibility.

A comprehensive range of Ultimate accessories is now available in both the transparent and textured options, including rocker and dimmer switches, socket outlets, coaxial and telephone sockets and fused connection units. On both models, the tamper-proof front plate clips securely to the mounting frame. The transparent plate is made from hardwearing and durable polycarbonate.

www.getplc.com

Varistors for PCB assembly

The VJ series of varistors from AVX incorporates a glass-passivated surface to protect the device from the reactants present during PCB assembly. As a result, the device has far more stable properties.

Zinc oxide is used in the construction of SMD varistors. The conductive properties of this material can be altered by chemical interaction with the resins, varnishes and flux residues present during PCB assembly. With its newly developed glass-passivated surface, the AVX VJ series can now overcome this problem by avoiding any such interaction.

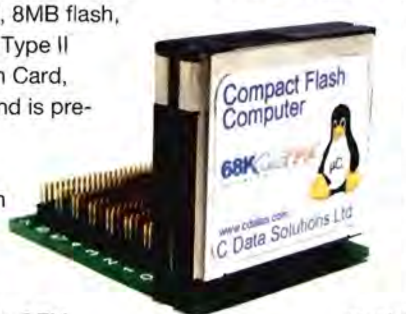
The series is available in case sizes from 1206 to 2220. The varistors are ISO7637 compatible and provide over-voltage protection, specified with a high-energy rating. They operate over the temperature rang -55°C to +125°C.

The VJ series is suitable for a range of applications, including automotive, security, measurement and medical equipment. Low leakage-current devices are available on request.

www.avxcorp.com

Carrier board for the Compact Flash Computer

C Data Solutions Ltd has released a new low-cost carrier board for its Compact Flash Computer. The Compact Flash Computer is a Freescale Coldfire MCF5272 processor, 32MB SDRAM, 8MB flash, packaged in a Type II Compact Flash Card, 42x37x5mm and is pre-loaded with uClinux. The Compact Flash Computer is available for $200 in small volume, $100 in OEM quantities. The low-cost development kit cost $400.



The carrier board has four Compact Flash connectors, two on top and two on the bottom. One is specifically used for the Compact Flash Computer, allowing the other three connectors for 3rd party CF+ I/O cards. The carrier board also has the bus expansion unit integrated onto it, which enables the Compact Flash Computer to directly address the CF+ I/O cards. The carrier board can be powered from 5-10V via a switching regulator or a 3.3V supply.

The 3-slot carrier board provides the basis for a lower cost development system and augments the existing 8-slot mother board development system. The carrier board is an ideal vehicle for developing portable, wearable and desktop units. Applications range from NAS, bridges, routers, wireless access points, data acquisition systems, etc. The 8-slot mother board system targets embedded computing in areas where PC104 is too big and the application volume does not warrant custom hardware design.

www.cdataszzzzz.com

Compact low-cost stepper driver

Astrosyn International Technology has launched a low-cost driver for two- and four-phase hybrid stepper motors. The P300 is a compact bipolar microstepping unit and is new to the European market. It provides maximum resolution of 12,800 steps/revolution.

In addition to full- and half-stepping, five microstepping modes can be selected. Output current is up to 1.0A per phase, with input voltages in the range of 18-36Vdc. The unit measures 22x55x88mm and weighs 150g. Its advanced design also minimises noise and vibration.

The P300 is suitable for applications where space and high performance are of critical importance, such as in medical OEM equipment and office automation products.

www.astrosyn.com

Enhancements for the Yokogawa WT3000 analyser

A number of new features have been added to the Yokogawa WT3000 precision power analyser. These include a 30MB of internal memory, auto-print function, and USB and Ethernet options, which provide enhanced communications with external devices and networks.

A USB port for connection to PC (Option /C12) uses a type B connector on the rear panel. Instruments with this option installed can be used in conjunction with the communication functions of Yokogawa's WTViewer software for data acquisition via the USB.

A USB port for peripherals with type A connectors can also be added (Option /C5). This allows data stored in the main unit to be saved in binary or ASCII format on a peripheral such as a USB storage device. It also allows a keyboard to be connected for easy input of user-defined mathematical expressions.

The Ethernet communications function (Option /C7) conforms to 100BASE-TX and 10BASE-T, and provides for data exchange with PCs or networks. The option supports file transfers via an FTP server, as well as FTP client (network drives), LPR client (network printers) and e-mail (SMTP client) functions.

The WT3000 does not have a built-in hard disk, and the FTP server function is available when a PC card or USB storage device is inserted or connected to the PC.

www.yokogawa.com/tm/tm-download.htm

Harting switches its connectors to lead-free

Harting has introduced lead-free (Pb-free) versions of all its electronics connector families, incorporating optimised surface finishes for solder, crimp, wire-wrap, IDC and press-fit products. Many Harting products have been lead-free for some time, but connectors involving solder termination have traditionally relied on tin-lead coating, which is prohibited under the RoHS Directive. The company plans to deliver 90% of its electronics connectors in lead-free form by August 2005, with the remaining 10% being completed by the 1st January 2006: well ahead of the European RoHS Directive coming into force on the 1st July 2006.

Harting carried out exhaustive tests – both in its own laboratories and in conjunction with independent test houses – on alternative materials, before selecting pure tin with a matt surface as the optimum finish.

The use of matt tin virtually eliminates the possible formation of tin whiskers – a suspected cause of short circuits and equipment failures, which can occur with bright finishes. The material qualified and coated by Harting has shown no evidence of any visible whisker formation.

Connectors based on this matt tin finish are suitable for use in modern high-temperature lead-free reflow soldering processes, where temperatures between 240°C and 270°C can be encountered.

www.harting.com

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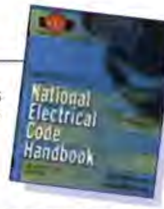

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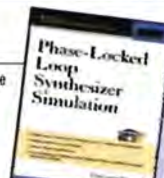

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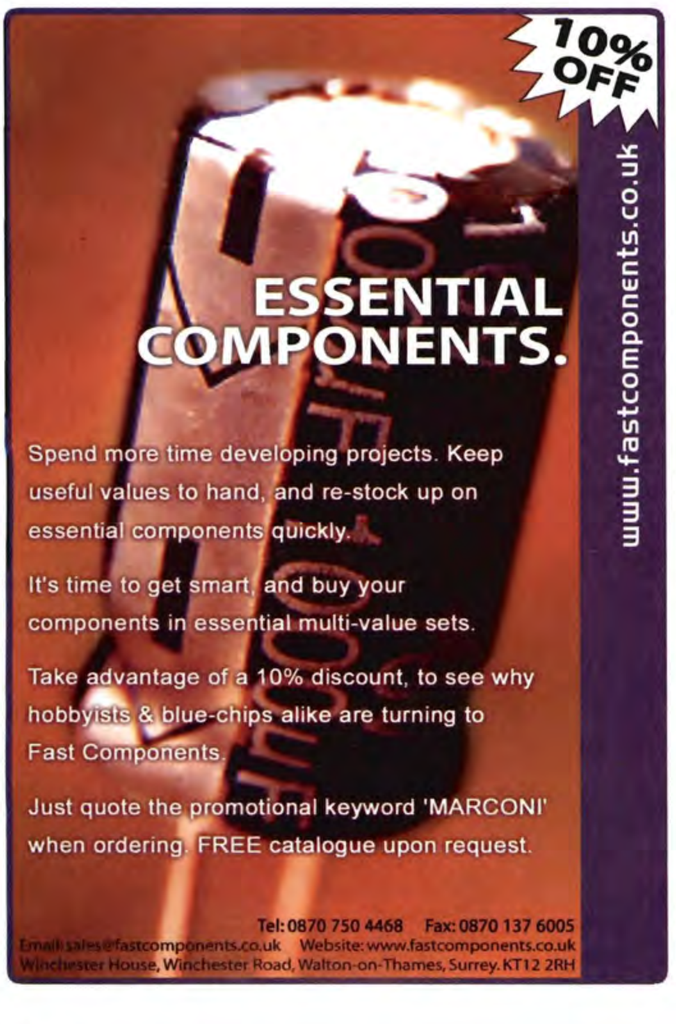

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