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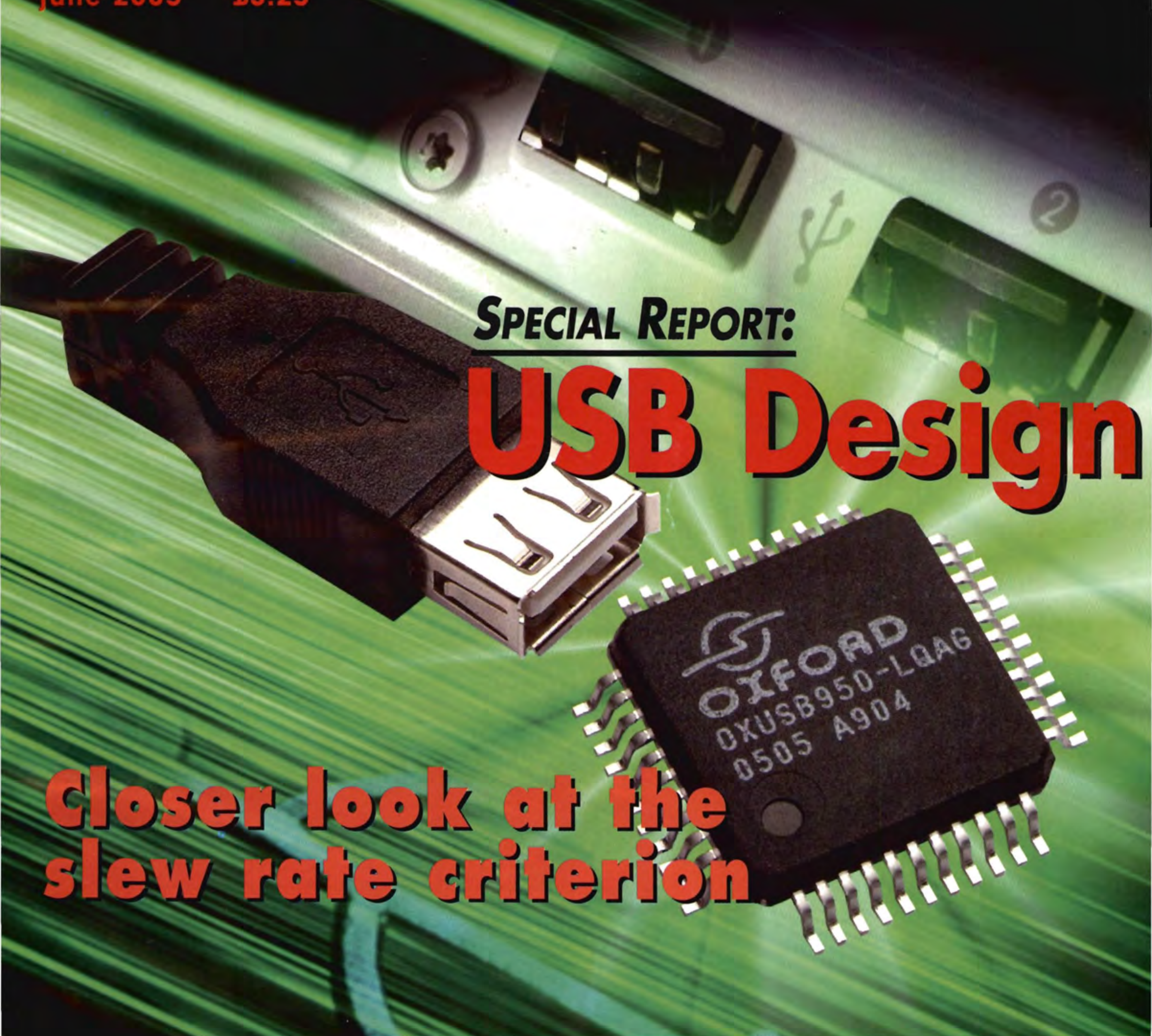

SPECIAL REPORT: USB Design

Closer look at the slew rate criterion

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• LED driver • 2nd order, multi-function, voltage-mode filter

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Front cover image supplied by Oxford Semiconductor

The analogue/digital divide

At a recent press briefing, National Semiconductor's product manager Uwe Kopp said that we are standing in front of a gap between analogue and digital. Interestingly, that gap seems to be shrinking as more and more digital replacements of analogue functions make their way onto the market. Some very old analogue circuits are being replaced with digital solutions. On-chip peripherals, such as timers, comparators and PWMs, are helping this migration.

Analogue has been critical in the signal chain, where it's the interface to the real world. But, companies are developing chips for the areas where analogue has traditionally reigned supreme, such as in conventional analogue-to-digital converters (ADCs) supported by many discrete components. For example, Analog Devices's (ADI's) new capacitance-to-digital converter (CDC) and impedance-to-digital converter (IDC) do away with up to nine discrete components, whilst taking the input directly from sensors. These new devices are totally integrated solutions, requiring only a few external components.

Silicon Labs is another example. Recently (see Technology in Electronics World, May 2005), Silicon Labs announced a direct interface for sensors for its 8-bit 8051-based microcontrollers. The controller includes an on-chip programmable gain amplifier, an offset digital-to-analogue converter and a 24-bit sigma delta analogue-to-digital converter. Low voltage sensors can be attached directly to the microcontroller.

However, despite all these advancements, digital circuitry will not replace all of the analogue circuits just yet. According to National Semiconductor's European marketing director Robert Hinke, the world of analogue has for the first time superseded the growth of microprocessors. The total available market for analogue components by 2007 will be worth some $40bn, whilst that for microprocessors will be at least $5bn lower, at $35bn (source: SIA November 2004 forecast). Last year, the standard linear business (including data conversion, interfaces, amplifiers and power markets) grew to $12bn. Analogue companies have already been heavily investing in this business, including National Semiconductor, which declares that up to 19% of its total sales have been ploughed back into investment for analogue R&D. Areas of growth for analogue devices are in high-speed communication, telecom infrastructure, automotive applications, printers, copiers, fax machines and medical applications, especially in portable medical equipment, which tends to require high-precision amplifiers, data converters and power management systems. Hinke believes that analogue will remain the differentiating factor and that there will be a gap between analogue and digital for some time to come.

When I was at university, every student in my year wanted to design digital circuits – it was considered easier and sexier. I found this trend continued during my work in industry, to the detriment of the firms concerned. We can see, with increasing frequency, that it is getting tougher for firms to recruit experienced analogue design engineers. So, it is certainly nice to see analogue design getting back the attention it deserves.

Svetlana Josifovska
Editor

EDITOR: Svetlana Josifovska **E-mail:** s.josifovska@highburybiz.com **EDITORIAL E-mail:** EWeditor@highburybiz.com
EDITORIAL ADMINISTRATION: +44 (0) 1322 611274 **E-mail:** EWadmin@highburybiz.com
PRODUCTION EDITOR/DESIGNER: Jane Massey **E-mail:** J.Massey@highburybiz.com
SUBSCRIPTIONS: Customer Interface Ltd, Cary Court, Somerton, TA11 7BR **Telephone:** 0870 4287950, **Fax:** 01458 271146
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GROUP SALES: +44 (0) 1322 611254 • **PRODUCTION EXECUTIVE:** Dean Turner +44 (0) 1322 611206 **E-mail:** d.turner@highburybiz.com
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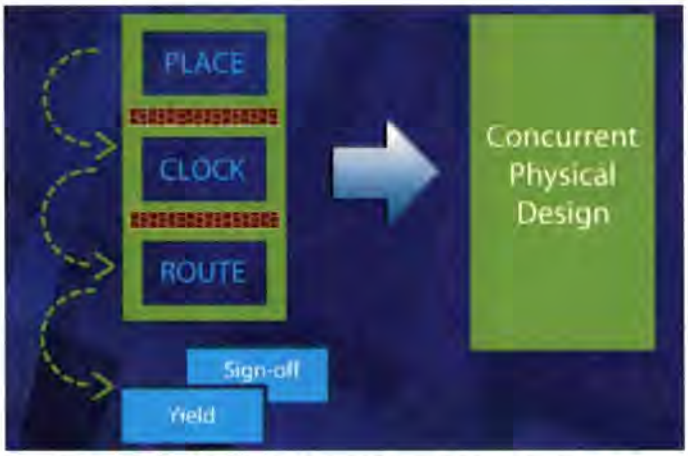
Synopsys IC Complier sees all

In the quest to ease the transition of semiconductor makers to process geometries of 90nm and below, leading EDA tool supplier Synopsys has announced a dramatic approach to physical implementation in its new tool – IC Complier. Built from the ground up, the IC Compiler's architecture handles physical synthesis and place and routing, including clock trees synthesis, in a single step rather than a series of separate processes as before.



IC Complier is key for sub-90nm designs, says Synopsys

Following logic synthesis, all of the device parameters and exact measurement data are processed at the outset of the design flow to allow the tool to allocate the routing and the clock trees optimally, earlier. The company says that this method will help tackle device complexities and the growing number of problems such as defects, leakage and signal integrity issues, hence improving yields and cutting the time to sign-off.

"In IC Complier, we extended synthesis to placement and to clock trees and routing. This offers reduced congestion, better timing predictability, and timing and signal integrity closure," said Bijan Kiani, marketing vice-president for the implementation group at Synopsys. "IC Compiler optimises for timing, area, power and yield – concurrently. By allowing common libraries, constraints, delay calculations, extraction and regressions to work together, we've been able to close that correlation gap."

Heading toward smaller geometries, the semiconductor industry is adding more than 8m gates per design, over 100 macros, between eight and nine routing layers, bringing a whole set of aggravating complexities with it, including increased congestion, increased impedance in the design, such as the resistance of the vias, signal integrity problems and so on. Synopsys believes that, going forward, only by solving these issues concurrently, would yields be improved.

According to Synopsys's executives, one of its customers validated IC Compiler on a 110,000-gate, 250MHz design in 90nm technology, showing improvements of 10% in area and 40% in time in the completion of both physical synthesis and routing, compared with the traditional Synopsys flow, which consists of Physical Compiler (PC) physical-synthesis tool and the Astro router.

A single annual licence for IC Compiler costs $735,000 and will be available from June.

UK's electronics sector weaker than Europe's

The annual DTI Value Scoreboard has found that UK electronics industry is weaker than that of Europe. The DTI has used seven measures including the relative size of the UK sector by value added (VA), the growth rate of VA and wealth creation. It has found that the UK sector is proportionately less than one third the size of the European sector and has lower average figures for VA growth and wealth generation.

In addition, there are 11 foreign-owned electronic companies in the UK 800, but eight companies in the electronics sector of the European 600 of which only one – Invensys – is from the UK.

Synopsys simplifies DFT

The challenges of testing devices built with 90nm and 65nm process technologies are giving test engineers a headache, says Synopsys. No longer is a relatively simple 'stuck at' fault test sufficient, as faults such as weak bridges, partial vias and transition faults mean a chip can pass the test but fail in use. But 'at speed' tests dramatically increase the number of test vectors, the time taken and the need for the expertise of a test engineer.

To tackle these problems, Synopsys has developed logic that can be easily integrated into the design flow by the design engineer at the synthesis stage to multiplex shorter scan chains in a design. All the test data generated through the design flow can then be carried through to the test stage for automatic test pattern generation (ATPG).

The adaptive scan module is a block of combinatorial logic that distributes the test vectors to all the scan chains, controlled by the input of two test pins. "There are multiple fan-out networks that are controlled adaptively," said Tom W. Williams, who at IBM published the essential paper on scan test in 1977 and is now an Engineering Fellow at Synopsys.

The results of the scan chains are combined at the end to reduce the complexity of the test system, and the vectors are generated automatically by the test tool. "We want to simplify test," said Williams. "When the tool was used by Micronas it gave a reduction in test time of ten times compared to what would have been needed for 'at speed' testing. STMicroelectronics is also standardising on the tool, called DFT compiler MAX.

New software will combat soft errors

Designers will have their nanometre-scale designs tested in the Alps

As process technologies move to 90nm and 65nm, soft errors become increasingly important, not only for memory subsystems but for the logic too. The smaller size of the transistors make the logic more vulnerable to strikes by alpha particles, and French company iRoC Technologies has developed several techniques to tackle the problem.

It uses a modelling tool to predict the effect of soft errors on memory and logic at the Spice and netlist levels, and tests customers' custom chips at an accelerator at Sandia National Labs in the US. Full-scale tests are also carried out, high up in the Alps where there's a greater incidence of alpha particles. "For nanometre designs, reliability and, in particular, soft error analysis are no longer just a process issue," said Jim Hogan, general partner of Telos Venture Partners in the US. "The growth in the amount of embedded memory and the lower activation energies of nanometre processes increase the risk of system reliability issues due to soft error strikes. And because soft errors can't be eliminated using classic reliability techniques, they must be addressed during the design phase."

The company has just introduced a new 3D modelling tool to quickly analyse the impact of soft errors on a design. The TFIT (transistor failure in time) tool simulates a strike on a block of IP and runs an analysis on an area in seconds, rather than overnight with Spice, and analyses a full IP block in a few days, rather than weeks.

As well as modelling a design, the company helps developers design for soft errors with three different approaches – triple redundancy of the logic, using a voting system to determine the best answer, hardening the cell by adding an extra transistor to the cell in vulnerable areas and using time redundancy. Time redundancy adds extra logic that is not sampled on the leading clock edge to see if there is any difference in the logic result, and uses combinatorial logic to give a 'go'/'no go' result.

IRoC has tested 500 devices in real time, 11,000ft up in the Alps. This showed the first failure in three days and three in the first two weeks, which was consistent with the modelling and the accelerated tests. These accelerated tests are cheaper because they use mixed lots, and are used by companies such as LSI Logic and Cisco.

City analysts don't feature obsolescence

The Component Obsolescence Group (COG) states that some 55% of the City analysts who monitor the 'at risk' sectors it polled recently recognise the issue of obsolescence but less than a third (30%) of them factor it into their analyses.

Only a quarter said that companies give them any information on the obsolescence problems they face and how they manage those. "While it is encouraging to see that component obsolescence is featuring on so many analysts' radars, it's disappointing that many organisations still do not seem to be actively volunteering information about this issue," said Michael Trenchard, COG's chief executive.

Yorkshire Forward is investing £9.65m in the region's Advanced Engineering and Metals (AEM) industry to help researchers and businesses develop, exploit and commercialise new technologies. A further £3.1m of private sector funding will also be ploughed into the programme, which is predicted to create more than 500 jobs. Universities and businesses will be able to bid for funding to develop projects in four preferred areas: near net shape processing, surface engineering, powder metallurgy and design modelling and simulation. The tenders will require that the work should be undertaken in the Yorkshire and Humber region.

Ω

The number of USB-enabled devices will rise from 705.7m in 2004 to 2.1bn in 2009, says market research organisation In-Stat. Growth will continue in all categories – PCs, PC peripherals, consumer electronics and communications devices – with the fastest growth to be seen in the communications category. "In the PC business in 2004, high-speed USB has nearly saturated the desktop market and now comprises over three-quarters of the notebook market, whose slower design cycles mean less rapid adoption," says Brian O'Rourke, In-Stat analyst.

Ω

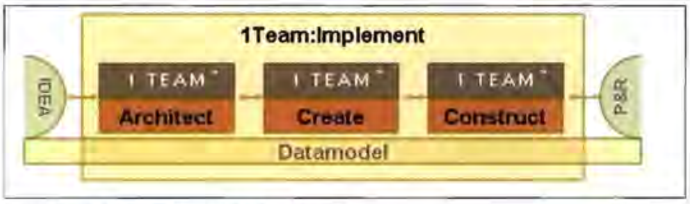
Toumaz Technology and Advance Nanotech have joined forces in the effort to bridge the gap between nanosystems and the macroscopic world. They are naming the joint venture Bio-Nano Sensium Technologies, which will focus on intelligent, ultra-low power sensor interfaces, using wireless communication, to create bio-nano sensors that can be implanted within the body to diagnose and treat a wide variety of medical conditions. The development effort will focus on the information and communication technology systems, necessary for these sensors to interact with their surrounding environment.

Ω

Predictive analysis moves to the architectural level

Atrenta is moving its predictive analysis tools up from the RTL level to tackle high level design issues. The rule-based tools capture best design practice – particularly in the physical implementation of RTL in sub-90nm designs – and applies it as high-speed, batch-operated analysis that also corrects errors in a design. The tools are used by nine out of ten of the largest semiconductor makers and 70 others, including companies such as Broadcom, Conexant and STMicroelectronics.

The move to high-level design is significant as it will allow analysis not only of floorplanning options and what they mean for implementation further down the design chain, but also the partitioning and analysis of hardware and software. This will allow different options at the architectural design level to be analysed for power consumption, area, cost and manufacturability, and the tools plug into the existing design flow via an Open Access database.



Atrenta's 1Team working together

The first parts of the tool, called 1Team, are for silicon analysis and verification, and will be launched in May. 1Team Implement allows automatic placement of mixed-size, multi-million instance designs with hundreds of hard macros in hours, rather than days.

In June, it is launching tools for system analysis and building embedded software that runs on he processors embedded in a system-on-a-chip, says Ajoy Bose, chairman, president and CEO. 1Architect will allow partial RTL, Verilog, VHDL, hard and soft IP and chip specifications to be analysed for timing, hierarchy, area, row utilisation, I/O pad placement and metal layers, and produces partitioned RTL and constraints that are carried through the rest of the design.

UWB proves a threat to Bluetooth's reign

UltraWideBand (UWB) technology's superior technical capabilities may curtail the reign of Bluetooth in consumer electronics. So says Mike Brookes, the chairman of the Low Power Radio Association (LPRA).

Current versions of Bluetooth provide data rates of around 500kbit/s, but future versions will support rates of above 100Mbit/s. "UWB will create radical changes in the Internet access, video and other data hungry applications. Its real potential is in consumer products, where Bluetooth is today. Major players, including Intel and Motorola, are working hard on the first generation of UWB chips," said Brookes.

All of these UWB benefits will be offered in same cost range as Bluetooth devices. "You'll get the same pence per unit [for UWB, as for Bluetooth], but you'll have a much wider bandwidth, better data rates and rapid access over longer distances," said Brookes.

Both standards are low-power RF technologies, suitable for multi-user environments, and can work up to 20m. UWB is spread spectrum based technology that works in the 3GHz to 10GHz band, whilst Bluetooth is frequency hopping technology covering the 2.4GHz range, soon to be also in the 5.7GHz range.

There are two types of UWB applied techniques. The first is pulse-based, where information is transmitted with a very short burst (ps to ns) of energy. The second technique is frequency hopping, where the UWB operating band is divided into groups of 500MHz sub-bands and then frequency-hopping protocol is applied within those sub-bands.

The US and some Far East countries are already conducting UWB trials. Europe, however, is slightly behind, since service operators like Vodafone and Orange are currently at loggerheads with the EC over UWB's operational frequency – UWB works near the 3G spectrum's noise floor. "They have paid an enormous amount of money for 3G licenses in the spectrum where UWB lives and are concerned that aggregation of ubiquitous UWB products will cause interference. They are keen not to allow UWB into that area. But if Europe doesn't get its act together on this one, it'll become backwater," said Brookes.

"The EC, though, is keen to get it allowed," he added.

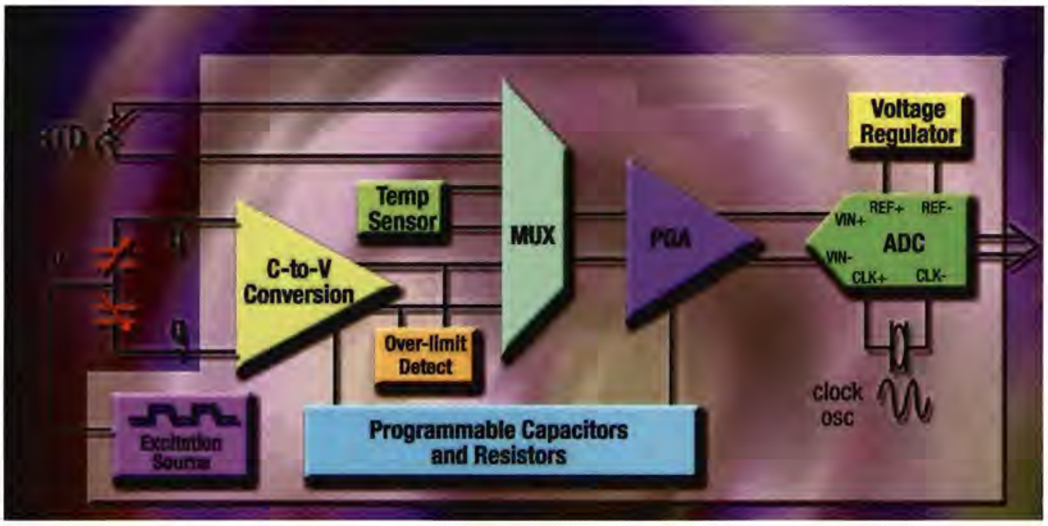
HDTV grows stronger

As of March 2005, 10 million homes around the world were watching HDTV programming on a high-definition TV set. By the end of 2005, this total is projected to reach 15.5 million, reports market research organisation In-Stat, with that figure rising to 52 million by the end of 2009.

"Even with the rise in the number of HDTV households, there are still challenges slowing the spread of HDTV service," said Mike Paxton, In-Stat analyst. "Foremost among these are: the need for more HDTV content, continuing the education of the public about the benefits of HDTV and widening the geographic availability of HDTV services, especially in Europe."

HDTV services are widely available in five countries: Australia, Canada, Japan, the US and South Korea.

Sensors get wired directly into digital devices



Block diagram of ADI's capacitance-to-digital converter, or CDC

Chipmakers are looking closely at linking directly to sensors as a way of reducing the complexity of measurement systems.

Silicon Labs has developed a direct interface for sensors for its 8-bit 8051-based microcontrollers. The controller includes an on-chip programmable gain amplifier, an offset digital-to-analogue converter and a 24-bit sigma delta analogue-to-digital converter. Low voltage sensors, such as magnetoresistive sensors in the 100mV to 1mV range, can be attached directly to the microcontroller. This will open up new areas for sensing, particularly in chemical sensors that previously needed conditioning electronics, making them bulky and expensive.

The controller can be used to handle an interface, for signal pre-processing or for proprietary communications protocols.

The limit is the micromachined (MEMS) sensors where there are very low currents, and the company is looking at adding a current DAC to use as a controller to support these applications.

Meanwhile Analog Devices Inc (ADI) has developed its first families of capacitance and impedance ADCs. The AD7745 capacitance converter replaces up to nine discrete devices, taking the input directly from a capacitative sensor. It uses an external capacitative bias to provide the offset levels in the same way that electrical bias is used in a traditional converter. Capacitative sensors are used in pressure sensors in industrial applications, blood pressure monitors and automotive applications, such as in position or level sensing and occupancy detection.

Internally, the capactitative ADC uses an op-amp to provide a capacitance-to-digital converter (or CDC, as Analog Devices is calling it) with a resolution of 20aF at 16.6Hz, feeding into a 24-bit sigma-delta ADC and programmable gain amplifier, giving a measurement accuracy of 2fF and a linearity of ±15ppm at Full Scale Reference (FSR).

ADI has done the same thing for impedance sensors. The AD5933 impedance ADC combines direct digital synthesis, analogue-to-digital conversion and hardwired digital signal processing for applications such as Electro Impedance Spectrometry and high-end medical equipment.

The sensor uses an internal DAC, coupled to the digital signal processing, to output a set of frequencies to excite the impedance sensor, while a 12-bit, 1Msample/s ADC is used to capture the output of the sensor. The output of the ADC is then processed via a 1024-point Discrete Fourier Transform (DFT) to give the result.

Two companies debut new parametric tester options

Agilent Technologies and Keithley Instruments have both announced DC/RF/pulse parametric testers last month, used for characterising devices built with 65nm process technology nodes and below. The instruments support short, 10ns pulsed IV measurements needed for extremely thermally- or charge-sensitive devices, including silicon-on-insulator (SOI) transistors or high-k transistors in high-speed logic applications. There are two instruments in the Agilent series of parametric testers – the 4075 and 4076. The 4076 tester supports measurements for currents of down to 1fA. Both of them support high-frequency and radio-frequency capacitance versus voltage (CV) behaviour, particularly important for ultra-thin gate MOSFETs, which are susceptible to electron tunneling.

Keithley, on the other hand, has added the third generation RF option to its testers. It offers an automated RF probe card changing, which removes the need for a lengthy, manual process as done previously.

Among its other benefits is the automatic continuous monitoring of measurement integrity, which detects events that would invalidate the RF calibration and triggers a corrective action.

M-Systems takes on SanDisk in embedded designs

Israeli flash memory company M-Systems is looking to replace the industrial CompactFlash market currently dominated by SanDisk.

M-Systems has launched a USB 2.0 version of its uDiskonChip that can boot Windows XP directly, which makes it very interesting for embedded designers.

This has required a workaround that has been approved by Microsoft, as usually an operating system (OS) has to boot to bring up the USB drivers. It has also implemented the drivers for its TrueFFS file system onto the controller ASIC so that no software drivers are needed, making the technology easily portable between designs.

Doreet Oren, director of product marketing at M-Systems points to the reliability issues when using the flash memory for an operating system. The TrueFFS file system allows the image of the OS to move around the memory map, avoiding lifetime problems. These occur when the OS is in one fixed area and user data is then constantly written on to another fixed, limited area of the memory map. With the TrueFFS approach, the image moves around and writes are spread throughout the memory map. In tests at a customer making gaming equipment with regular writes, this provides over 5m read/write cycles for uDiskonChip, says Oren, compared to 300,000 cycles for industrial compact flash.

This comes as SanDisk is migrating its CompactFlash onto industrial versions of its smaller SD format. It has also developed a package that includes a USB interface as part of an SD card.

SanDisk is migrating CompactFlash onto industrial versions

For M-Systems, the higher speeds of USB 2.0 support higher density memories (up to 4Gbit) with boot times comparable to a hard disk drive. It is almost twice as fast as an IDE module. Data access times of 3ms are achieved by interleaving blocks on two chips through a removable, or a 9-pin fixed, USB2 interface.

Magma targets designs of 90nm and below

Magma Design Automation is targetting sub-90nm designers with new tools that consolidate a number of technologies acquired over the last twelve months. The Cobra development has been key for the future of the company, says CEO Rajeev Madhavan. "The 18-plus months that have gone into this effort have delivered products that will significantly expand design options available to our customers as they no more and more design work at 90 and 65nm," he said.

There are nine new tools in the Cobra release, including a synthesis engine that can output to standard cell, ASIC or FPGA, and focusing on reducing the impact of synthesis on the design. Now the layout, routing and timing is analysed and optimised for signal integrity issues before synthesis to reduce the timing and area problems often faced in the logic synthesis stage. This 'interconnect synthesis' is vital at 90nm and 65nm, says Madhavan, balancing cell delays and wire delays with the shapes of the wires and the switching of neighbouring wires.

Although all the tools can operate from a single unified database for the Blastfusion and Blastcreate design flows, Magma has also added a standalone timing sign-off tool called Quartz Time/RC for timing and RC analysis and parasitic extraction in the design loop, rather than as a batch process that needs multiple iterations. This uses core algorithms developed at startup Random Logic.

Coming from Magma's acquisition of Mojave Design, the Quartz DRC and LVS tools give a fast turnaround for physical verification, using the core algorithms developed at Mojave. These provide verification of any chip in under two hours.

It has also added a statistical timing tool for manufacturability analysis, Quartz SSTA, that accounts for process variations and provides a parametric yield analysis for the design. This comes from the acquisition of Silicon Metrics. It provides the parametric extraction and timing, using the statistical library models from Magma's Silicon Correlation Division.

Risk assessment

- Look for the hazards
- Decide who might be harmed
- Evaluate the risks and whether existing precautions are adequate, or whether more can be done
- Record your findings
- Review and revise your assessment
- Reduce minor injuries
- Reduce reported injuries
- Reduce absenteeism and downtime
- Reduce insurance claims and premiums
- Reduce injuries related to hours worked

This month's tips have been extracted from Britain's Health and Safety Executive's (HSE's) new website: www.betterbusiness.hse.gov.uk, which is backing its newly launched campaign to persuade businesses that sensible health and safety management is not only beneficial for staff but good for the margins too.

If you'd like to send us your top five or ten tips on any subject you like, please write to theEditor at

EWadmin@highburybiz.com

The future of embedded speech

Embedded speech technologies are improving at a dramatic pace, whilst entering a wide range of applications, says Arnd Weil

Embedded speech applications share a common denominator – they take the "pain" out of using cumbersome applications by enhancing the interface experience between the device and the user. Entering a destination into a car navigation system, dialling a phonebook entry on a mobile device, or selecting a new song while driving, are all applications that speech technology makes much easier and safer.

Speech can greatly enhance the user experience also in other applications such as gaming, where certain commands and actions can be voice activated, or SMS reading. Removing that "pain" in the user interface is the key driver for embedded speech technologies today. This will continue to motivate future applications like mobile dictation and others.

Recently, a strong focus for embedded speech has been set in enhancing the vocabulary for destination-entry applications in automotive navigation systems. In the case of satellite navigation, original equipment manufacturers (OEMs) are demanding larger vocabularies such as all 70,000 cities in Germany or all 150,000 streets of California.

Speech companies have defined different strategies to reach that goal. Some of the progress is being made in improving the quality of embedded recogniser engines. One reason for that is successful integration of different embedded speech technologies (L&H, Philips, SpeechWorks) by combining and leveraging the best modules and in-car speech databases from all parties. Another important factor is to have an impressive network of partners, such as map data suppliers and platform manufacturers, and to closely co-operate with car manufacturers.

> *"In the near future, embedded speech engines will be able to recognise multi-lingual speech and understand more freely structured dialogues"*

But what about other applications and market segments like mobile devices? Here too advancements have been made. For example, a screen reader for mobile handsets is designed to be usable by a blind person. It includes a parametric text-to-speech system with very low response time and high intelligibility. Although such voices are easy to understand, they sound distinctively robotic. For that reason, natural sounding text-to-speech systems are been introduced to the mobile market for applications like SMS and e-mail reading.

While most of these applications can fit even on low-end feature phones, the handset evolution will open a world of new opportunities for speech-enabled applications, for example embedded SMS dictation. In parallel, the introduction of network-based services will be pushed by mobile operators, which will open new possibilities. The voice destination entry for Wayfinder's off-board navigation system is a good example of the convergence of the network and embedded speech business.

Wireless type telematic systems enable users to access live data and services that are relevant to specific localities – an example being the identification of the most popular Chinese restaurant in the immediate area by using a convenient speech interface.

Embedded speech recognition and text-to-speech engines will continue to develop, aided by the evolution of processor hardware. In the near future, they will be able to recognise multi-lingual speech and understand more freely structured dialogues that will allow users to make enquiries in day-to-day terms, such as, "I want to go to Edinburgh, what's the best route?"

Speech will also continue to enhance niche markets, including language learning and assistive technologies, warehousing systems, and gaming on both, mobile handsets and home entertainment platforms. One thing is certain, though, wherever there is a user interface that causes unnecessary "pain", speech will almost certainly be the solution that alleviates it.

Arnd Weil is senior manager for the Embedded Product Line at ScanSoft.

The 8-bit MCU is dea

By Nick Flaherty

With a set of new launches of 8-bit microcontrollers, nothing seems to shake this device's design dominance

Despite efforts to encourage designers to move from 8-bit directly to 32-bit microcontrollers, the 8-bit market continues to flourish, with several launches at the recent Embedded World show. Reducing the pin-count for smaller designs while keeping the same range of peripherals, and increasing the performance to full USB2 support are continuing to boost 8-pin controllers.

In a bid to challenge Microchip on its home ground, Zilog has launched an 8-pin, small footprint version of its Z8 Encore! XP microcontroller. This offers exactly the same on-chip functions as the larger devices through pin multiplexing, as well as a full-range temperature sensor, single pin debugger and trans-impedance amplifier.

"We are extremely excited about the numerous possibilities the Z8 Encore! XP 8-pin brings to the market, and we have already secured several design wins, receiving very positive, initial feedback from the design engineering community," said Ramesh Ramchandani, executive vice president of sales and marketing. "We are also optimistic about demand for this product from new sectors such as health and fitness, remote transmitters and receivers, smartcard readers and battery charger markets, among others."

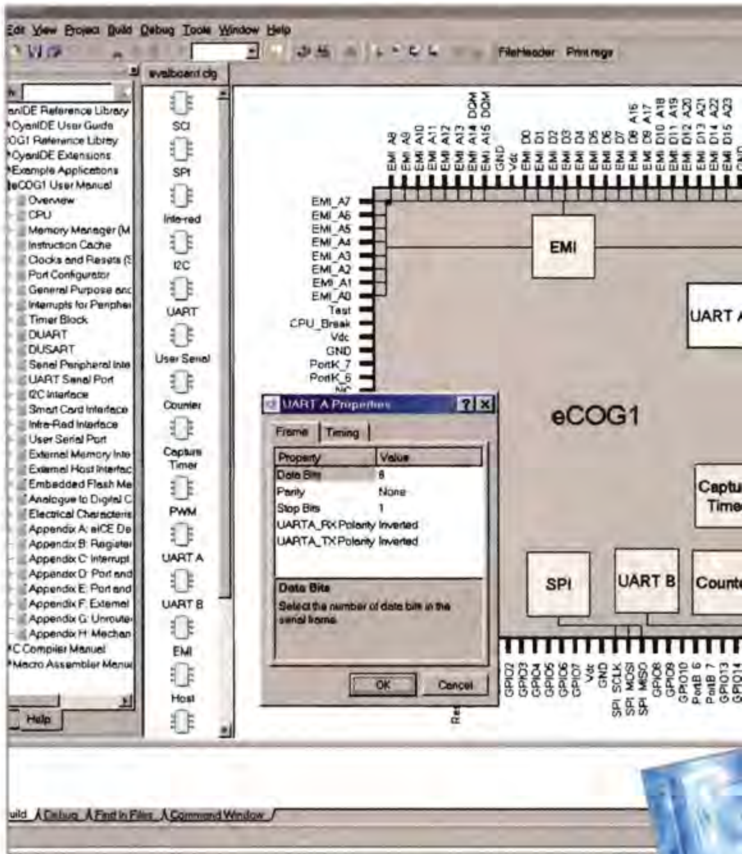
At the same time, Infineon Technologies has launched an 8-bit 8051 controller with 12kB of program flash and 4kB of data flash for less than a euro. The 26MHz XC866 includes an 8-channel, 10-bit ADC and three 16-bit timers.

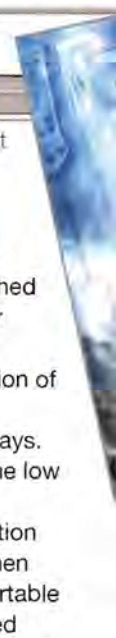
Atmel has also launched three new tinyAVR 8-bit controllers with internal temperature sensors. The ATiny25 has 2kB of flash memory, the 45 model has 4kB and the 85 has 8kB.

And STMicroelectronics (ST) has launched a 10MIPS 8-bit CPU, the uPSD3400 Turbo Plus, with a full speed USB2.0 interface. The 40MHz 8032-based core uses an internal 16-bit wide instruction path to handle two instructions at a time to meet the performance requirements of the 480Mbit/s USB2.0 bus. Using an 8-bit controller for a USB2.0 hub keeps the power consumption and the code size down.

Motorola launched an 8-bit controller particularly suitable for energy-efficient lighting systems. The HC908LB8 HC08-based controller includes power factor correction, two PWEM outputs and a 7-channel 8-bit ADC.

Despite a strong attempt to move designers to 32-bit microcontrollers, particularly the ARM architecture, there are still significant developments in 16-bit controllers, especially for low power.





Above: Cyan Technology's CyanIDE development environment

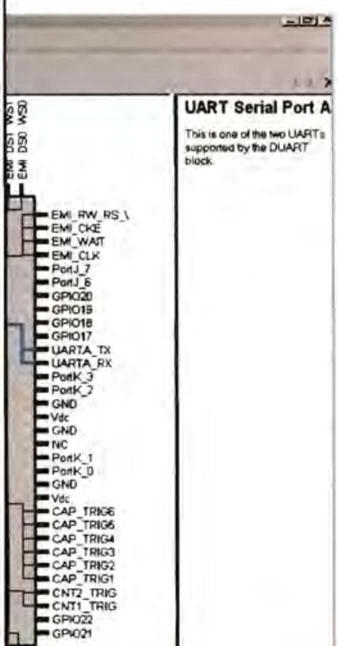
Right: Zilog launches a small footprint version of its Z8 Encore! XP microcontroller

In a bid to reduce the time taken to develop with a new processor, UK chip designer Cyan Technology has launched a new version of its ultra low power COG 16-bit controller with a key new development tool. The Version 1.1 of the CyanIDE development tool has automated the configuration of the peripherals, caches and memory management unit, reducing initial development times from weeks to a few days.

The new chip, the 25MHz uCOG1m, is also based on the low power XAP Harvard architecture core developed by Cambridge Consultants and provides a current consumption of 400nA in standby mode (CPU stopped) and 10.1µA when continuously clocked at 16kHz. This makes it ideal for portable and handheld devices as it includes an MMU and vectored interrupts to support major operating systems. This increased complexity makes the drag-and-drop approach of IDE for configuring the device even more vital.

The 8mm square, 81-pin chip is electrically equivalent to Cyan's 128-pin eCOG1k with a range of serial interfaces (dual UARTs, dual USARTs, SPI and IrDA), timers, 16-bit clock generator timers, general-purpose event counter timers, an A to D

, long live 8-bit MCU!



converter and communications interfaces. It has 60 digital I/O and analogue functions and 28 special GPIO pins that can be used as interrupts to wake up the MCU.

"For many applications developers have to make compromises on their choice of microcontroller in terms of peripherals, power consumption and physical size," said Paul Barwick, Cyan Technology's sales director. "By incorporating the highest density of peripherals, memory and digital I/O per square millimetre, the ultra-low power uCOG1m addresses all of these issues."

Using a simple 'drag and drop' facility in the IDE, the designer can select the required peripherals by dragging them onto a screen image of the uCOG1m.

The chosen peripheral is then simply 'right clicked' to display and set up its properties. This process saves reading hundreds of pages of a user manual and furthermore, if a mistake is made or conflicts are generated, the user is alerted and the design cannot continue.

Cyan has been through ups and downs in the market. The basic technology was licensed from Cambridge Consultants in 2000, but the company was resurrected two years ago with a new set of tools. Last year it sold one million units.

Other manufacturers are also extending their 16-bit range, and some are even moving into 16-bit for the first time.

German chip designer Micronas has developed low power 8/16-bit controller for automotive instrumentation, steering columns and smart junction boxes. The CDC16xxF family includes an EMI reduction module that smoothes the clock and so reduces the size of the capacitors and even the number of PCB layers needed to meet EMC emission requirements. It also adds three CAN controllers, a power saving module that shuts down the different peripherals when not in use and an LCD controller.

Some controller designers are even moving down from 32-bit. Processor core designer Imagination Technologies is developing a new embedded microcontroller core that uses a 16-bit version of the instructions already used in its META multithreaded processor. META is used in DAB digital radio and digital TV, handling four separate threads.

In contrast, the new MTC controller core will handle one thread with a 16-bit instruction set which reduces the core size to $0.26mm^2$ on a 0.13mm process and gives a power consumption of 0.09mW/MHz. It also includes the same co-processor interface, so chip developers can have a range of products from a low-end controller to a high-performance multimedia engine, all using the same CodeScape development tools and thread linker. An early version is currently being used by Renasas in its 7770 multimedia accelerator, but it is also being offered to other chip makers to include in system-on-a-chip devices, which will come onto the market early next year.

> *"We are optimistic about demand [for 8-bit MCUs] from new sectors such as health and fitness, remote transmitters and receivers, smartcard readers, battery charger markets and others."*
> **Ramesh Ramchandani, executive VP of sales**

This is part of a strategy to expand the META range both up and down, as Imagination is also developing new versions of its 32-bit META core, with a high-speed 250MHz version being developed for the end of this year and a low power version in the first half of 2006. A new architecture called META2 running at up to 500MHz is also due at the end of this year.

New process technologies mean that the core itself is an increasingly small component of the chip, and many more peripherals are being added to make these controllers even more cost-effective. Keeping the power consumption low and the memory size down helps to keep the system costs low. The increasing integration also helps to mop up more the system cost into the controller. New software to configure the devices such as Cyan's IDE, coupled with free software such as TCP/IP stacks, can only help bring more designers into using such devices and keep the 8-bit and 16-bit controllers alive and healthy. In applications where the memory space is restricted and 32-bit is not necessary, both 8-bit and 16-bit controllers are continuing to thrive. In August last year, market research company Semico predicted that the total value of the 8-bit microcontroller market will grow by 8% a year, from $4bn in 2002 to $5.8bn in 2008.

Closer look at the slew rate criterion

Even though the slew rate criterion is well known, failing to apply it to a circuit as simple as a standard inverting op-amp amplifier can lead to wrong measurements and false conclusions.

By Hugo Coolens

When one has designed a linear op-amp circuit, it is a good idea to check its performance by real measurements. Care should be taken to avoid non-linear distortion when comparing measured results with design predictions. For an op-amp circuit the most important mechanisms that could cause non-linear operation are saturation and slewing.

Consider the simple inverting op-amp amplifier in **Figure 1**. When we try to measure the frequency response of this amplifier, we should apply at the input a sinusoidal signal whose amplitude is large enough, since a large signal to noise ratio will be beneficial for the measurement. However, we should not make the amplitude too large to avoid saturation or slewing of the op-amp.

The amplitude of our sinusoidal input signal will be called hereafter $V_{I,P}$ and the maximum value which does not cause nonlinear distortion $V_{I,P,MAX}$. If we assume the saturation voltage of our op-amp is 2V less than the power supply voltage, which we take to be 15V, then $V_{I,P,MAX}$ =130mV will not cause saturation. Let us calculate this value for slewing using inequality (1), the well-known slew rate criterion:

$$\omega \cdot V_{O,P} < S_R \qquad (1)$$

Let us check for slewing in the passband of our amplifier (e.g. for f =100Hz) : $2\pi \cdot$ 100Hz · 13V =8168V/s < 500000V/s. This result is satisfactory. For typical parameters [1] of a 741, the circuit has a DC-gain $A_{CL,0}$ =100 and a closed loop bandwidth BW_{CL} = 9901Hz [2]. As we want to measure the frequency response, also in the roll-off region of the amplifier, let us check it there too, e.g. for f = 100kHz. At this frequency, A_{CL} = 9:85, thus the left hand side of inequality (1) becomes $2\pi \cdot$100kHz · 1.28V = 804000V/s. In this case, the slew rate criterion is clearly not met. Thus we should choose a smaller value for $V_{I,P}$. Instead of using a trial and error method, we can rewrite equation (1) which, as such, is not very useful for our purpose as it applies to the output of the amplifier:

$$2\pi f \cdot V_{I,P} \cdot \left|\overline{A_{CL}}\right| < S_R \qquad (2)$$

Rearranging inequality (2) and using

$$\overline{A_{CL}} = -\frac{-A_{CL,0}}{1+jf/BW_{CL}}$$

brings the slew rate criterion back to the input of the amplifier:

$$V_{I,P} < \frac{S_R\sqrt{1+\left(\frac{f}{BW_{CL}}\right)^2}}{2\pi f A_{CL,0}} = V_{I,P,MAX} \qquad (3)$$

One could be tempted to try to solve this inequality, which essentially would mean to solve a quadratic inequality. If you look, however, at the right hand side of it, you can see in **Figure 2** this function has a horizontal asymptote for $f \rightarrow \infty$. In fact, this result could be expected from inequality (1 too, as the left hand side of it has both a factor which increases linearly with frequency and one which decreases linearly proportional to frequency (assuming first order behaviour)).

Determining the above mentioned asymptote gives:

$$V_{I,P,MAX,\infty} = \frac{S_R}{2\pi A_{CL,0} BW_{CL}} \qquad (4)$$

Equation (4) can also be rewritten as:

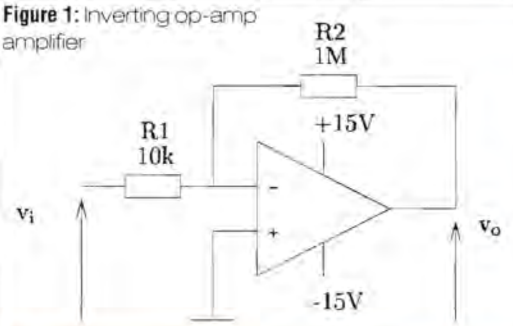
$$V_{I,P,MAX,\infty} = \frac{S_R}{2\pi |\alpha| A_{OL,0} BW_{OL}} \quad \alpha = -\frac{R2}{R1+R2} = \frac{-A_{CL,0}}{1+A_{CL,0}} \qquad (5)$$

Equation (5) has the advantage that it uses op-amp parameters directly. It can also be used for the standard non-inverting amplifier, in which case α =1.

From equation (5) it is clear that for two op-amps with the same slew rate, the one with the higher

References:
[1] unity gain frequency =1MHz and S_R = 0:5V/µs
[2] $(1 + A_{CL,0})B_{WCL} = A_{OL,0} B_{WOL}$

Figure 1: Inverting op-amp amplifier



bandwidth will yield the worst value for $V_{I,P,MAX,\infty}$.

Equations (4) and (5) show that $V_{I,P,MAX,\infty}$ is dependent on $A_{CL,0}$ for the inverting amplifier, whereas for the non-inverting amplifier it is not. For a unity gain amplifier $V_{I,P,MAX,\infty}$ may be twice as large for an inverting amplifier than for a non inverting one. Of course, the closed loop bandwidth will also be halved in that case. A more "physical" explanation is that for an inverting amplifier the input signal is attenuated by R1 before reaching the actual input of the op-amp.

Notice also that the graph in Figure 2 has a "corner frequency" equal to BW_{CL}. This means you can apply a $V_{I,P,MAX}$ that is √2 times $V_{I,P,MAX,\infty}$ at a frequency equal to BW_{CL} without causing slew rate distortion.

Using typical values for a 741, we can conclude from equation (4) that we should limit the amplitude of our sinusoidal input signal to $V_{I,P,MAX}$ =80mV to avoid slew rate distortion for whatever frequency. Using a unity gain frequency of 1.2MHz and a worst case slew rate of 0:3V/μs, this value is even further reduced to slightly less than 40mV, which is more than three times less our initial value based on the saturation criterion, but will yield an acceptable signal to noise ratio for most measurement setups.

This does not conclude our story yet. Real op-amps are higher order systems. This phenomenon will also be noticeable in the closed loop system response. Calculations for higher order op-amp models may become rather tedious. However, simulation programs like Spice can come in handy for this purpose. When we apply an AC-source of 1V at the input of our circuit and perform an AC-analysis, we obtain an output voltage V ([OUT]) which is numerically equal to

$$|\overline{A_{CL}}|$$

Performing some postprocessing on V ([OUT]) gives us

$$V_{I,P,MAX} = \frac{S_R}{2\pi f V([OUT])}$$

The result is shown in **Figure 3**.

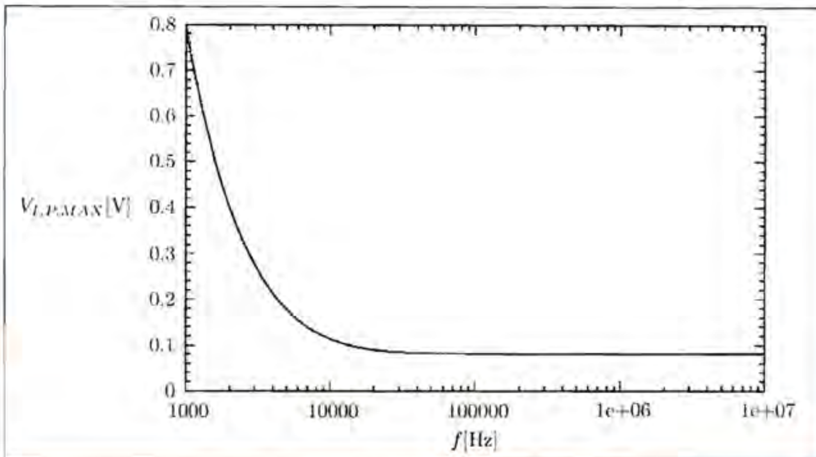


Figure 2: Maximum input amplitude versus frequency to avoid slew rate distortion for Figure 1 (R2/R1=100)

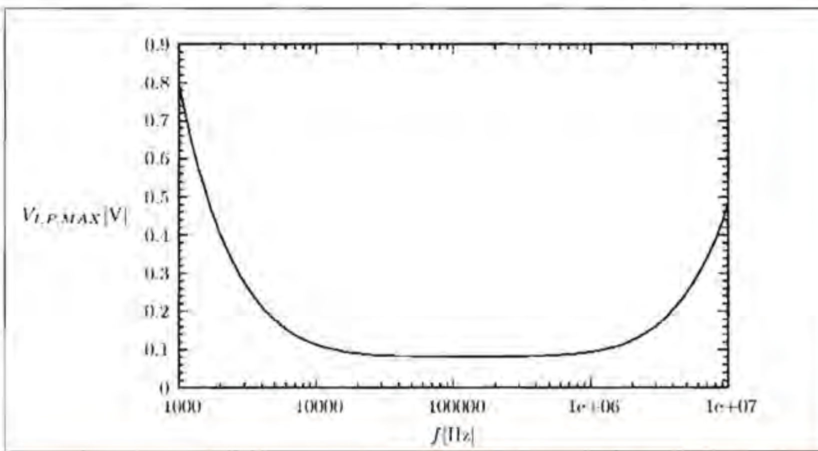
We now no longer have a curve with a horizontal asymptote but a U-shaped curve which has a minimum at 126kHz of 81mV, pretty close to the value we obtained with our first order approximation.

This method, based on the results of an AC-analysis, is not restricted to simple circuits as given in the example, but can easily be used for more complex linear op-amp circuits such as filters. You should choose an op-amp model that models real frequency domain behaviour closely and preferably not based only on typical but also on worst and best case performance. Keep in mind, however, that this method does not take into account capacitive loading of an op-amp output, which can deteriorate further slew rate performance.

Even though we focused in this article on the slew rate criterion, don't forget to have a look at the saturation criterion too. In fact, you can bring that back to the input of your circuit too in a similar way as was shown for the slew rate criterion:

$$V_{I,P} < \frac{V_{O,SAT}}{|\overline{A_{CL}}|}$$

Figure 3: Maximum input amplitude versus frequency to avoid slew rate distortion for higher order op-amp model



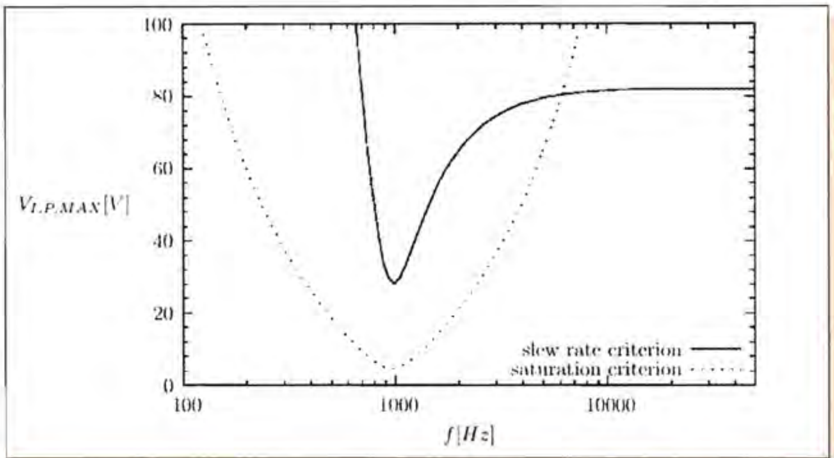


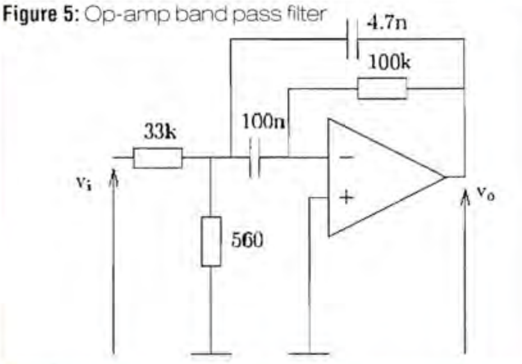
Figure 4: Maximum input amplitude versus frequency to avoid slew rate distortion and saturation for band pass filter

An AC-analysis with Spice, followed by a little post-processing, is sufficient to calculate $V_{I,P,MAX}$.

$$V_{I,P,MAX} = \frac{V_{O,SAT}}{V([OUT])}$$

It is not always obvious which of the two criterions will be the dominant one, therefore, you should plot both graphs to determine the maximum amplitude that you can apply to your circuit without causing slew rate distortion or saturation. An example of such graphs is shown in **Figure 4** for the op-amp band pass filter shown in **Figure 5**. It is clear that, in this case, the saturation criterion is the dominant one.

Figure 5: Op-amp band pass filter



I hope this article shows that there is more behind the standard slew rate criterion than inequality (1) or what standard handbooks of electronics usually tell.

Design of a USB interface

...for a data aquisition system

By Qian Xie and Wuqiang Yang

In terms of hardware, an electrical capacitance tomography (ECT) system is a typical data acquisition system, although its software is complicated. The basic function of ECT is to reconstruct permittivity distribution of a cross section, based on capacitance measurements. An ECT system has been developed at the University of Manchester (formerly UMIST) with a PCI data acquisition board from Arcom Ltd of Cambridge. One difficulty is that the system cannot be operated by a laptop.

To enhance portability, a USB-based data acquisition card has been recently developed, based on a USB interface module (USB-IFM) MOD2 with a FT8U245AM IC on it from Future Technology Devices International (FTDI) Ltd of Scotland. USB-IFM was selected because it provides an easy and cost-effective way of transferring data between peripheral devices and a PC at up to 8Mbits (1Mbyte) per second and also its simple FIFO structure. The accompanying software makes it easy for the users, who may not be familiar with the protocols of USB, to control other devices via I/O ports. **Figures 1 and 2** show the module and the block diagram of USB-IFM.

USB-IFM communicates with a PC via a USB link and with the peripheral devices via an 8-bit parallel data port (D0-D7). All low level operations involved in transmitting data between the USB-IFM and the PC, including the transitions between serial and parallel data, are handled internally by USB-IFM. When the PC sends data to USB-IFM, the data is stored in the FIFO Receive Buffer and can be read by the peripheral from the data port one byte at a time. Each rising edge of the RD# signal sent to USB-IFM causes a new byte to be transferred to the data port (see **Figure 3 (a)**). The peripheral sends data to the USB-IFM for transmission to the PC by writing one byte at a time onto the data port. Each falling edge of the WR signal sent to USB-IFM causes the byte to be transferred to the FIFO Transmit Buffer (see **Figure 3 (b)**).

The RD# and WR signals must be generated by the peripheral. Two signals, RXF# and TXE#, are automatically generated by USB-IFM to control the data flow. When the TXE# flag is "1", data cannot be written onto the USB-IFM data port. Similarly, when the RXF# flag is "1", data cannot be read from USB-IFM data port.

Data acquisition system

The overall data acquisition system is shown in **Figure 4**. It includes the USB-based data acquisition card, a signal generator card and up to six capacitance measurement cards, providing 12 capacitance measuring channels, one for each capacitance electrode. Two direct digital synthesiser (DDS) IC chips (AD7008) are used to generate two synchronised 500kHz sine-wave signals of 18V peak to peak, one as the excitation source and the other as the reference signal for phase sensitive demodulation (PSD). The analogue multiplexer (MUX) (ADG526) is used to select the DC signal from each capacitance measurement channel in sequence. A differential amplifier (INA105) subtracts the appropriate voltage produced by a 12-bit digital-to-analogue converter (DAC) to cancel the standing capacitance. The signal now represents the measured change in capacitance and is further amplified. A DC PGA with selectable gains of 1, 2, 4, 8 and 16 is required to deal with a large dynamic measurement range. The analogue signal is finally converted to a 12-bit digital signal by an analogue-to-digital converter (ADC) and then transmitted to the PC in two bytes.

The offset signal, which is used to balance the standing capacitance, comes from the DAC, which is on the data acquisition card. The offset signal can vary from 0 to 5V in 4096 steps, and is expressed as:

$$V = -V_{ref}\frac{D}{2^{12}}$$

where Vref is the reference voltage for the DAC and D is the digital input.

The ADC is configured for offset bipolar operation and operates over the range Vin = -1V to 4V. The digital reading is given by:

$$E = \frac{-V_{in} + 4}{F} 2^{12}$$

where F is the full measurement range of the ADC.

The system operation is controlled by the digital outputs port on the data acquisition card and provides the following functions:

➢ Control of CMOS switches to select the excitation and detection electrodes;

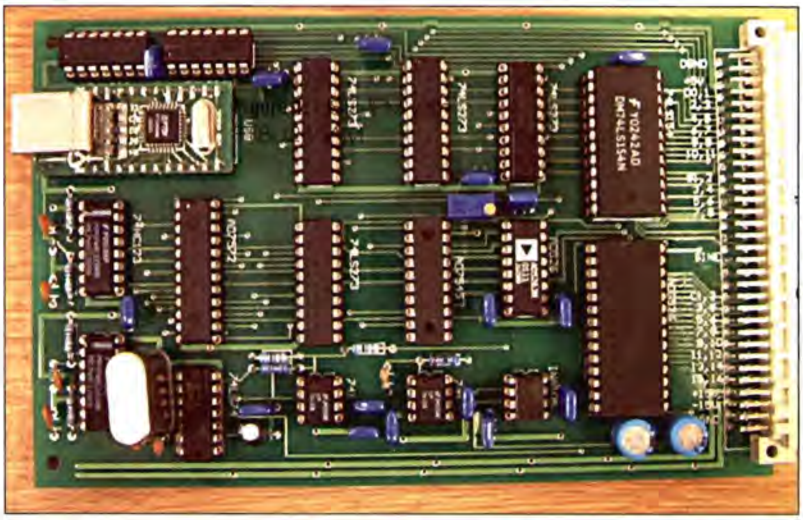
➢ Control of the amplitude and frequency of the excitation and the reference signals and the phase difference between them;

➢ Control of the MUX to select the DC signals in turn, from the capacitance measuring circuits;

➢ Control of the PGA gain to make full use of the measurement range of the ADC.

USB-IFM logic interface circuit

The basic logic circuit for interfacing USB-IFM to the electronic units in the data acquisition system is shown in **Figure 5**. This circuit enables the PC to select any unit and to transmit data to or receive data from any unit. The USB-IFM output RXF# is connected to the RD# input via an inverter. The 8-bit I/O port (D0-D7) of USB-IFM is taken to Latch (1) (74LS273), which is activated when the RD# signal goes high. The output of Latch (1) is divided into two parts, bits D0-D3 as a 4-bit Read Data Bus for all electronic units, and bits D4-D7 as a Control Bus to be taken to a 4-16 decoder chip (74LS154), whose 16 outputs are used as Control Lines to select individual units.



Above: USB acquisition board

Figure 1 (Left): USB-IFM with FT8U245AM

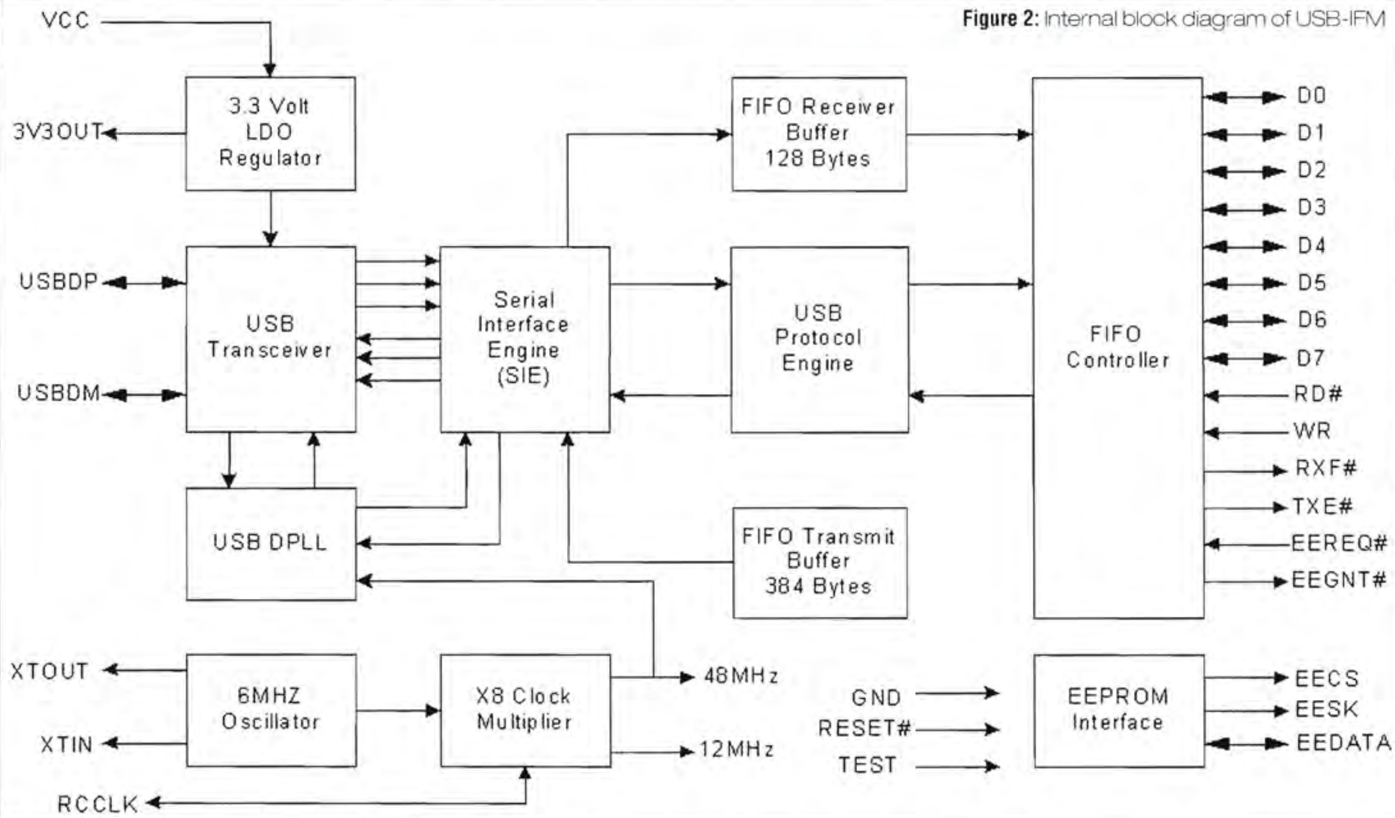


Figure 2: Internal block diagram of USB-IFM

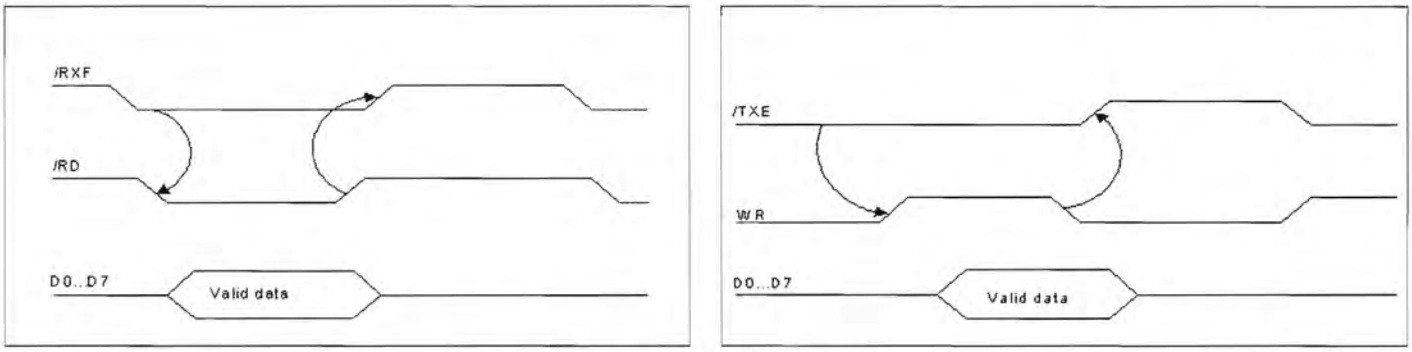


Figure 3 (a) and (b): USB-IFM timing diagram. **Left (a)**: Read cycle **Right (b)**: Write cycle

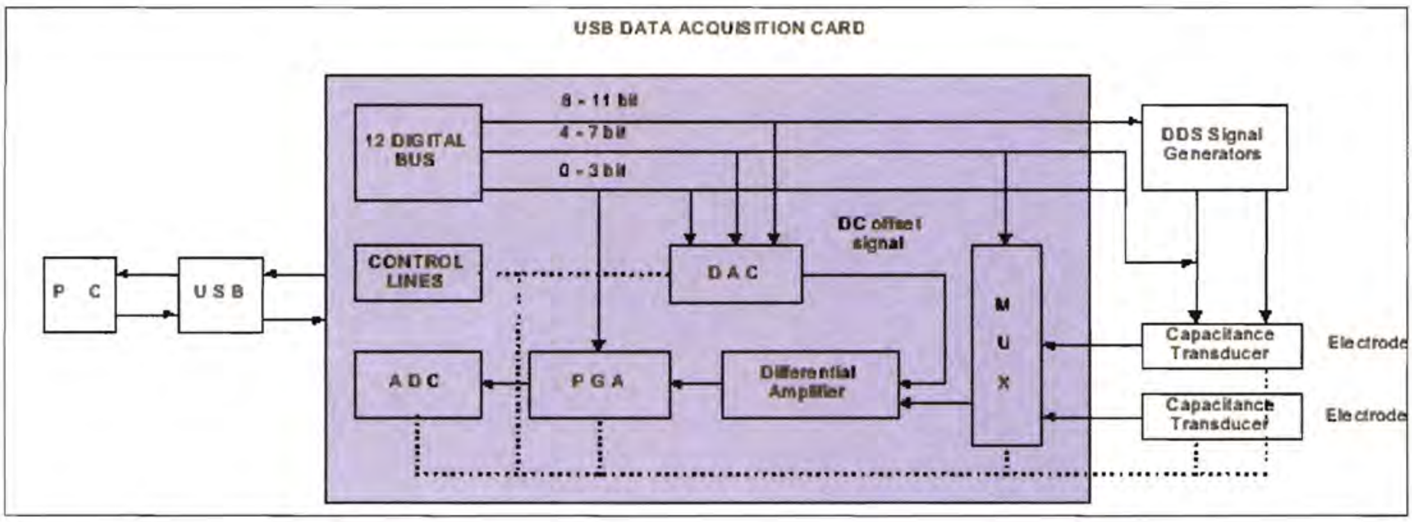


Figure 4: Data acquisition system showing the USB interface card

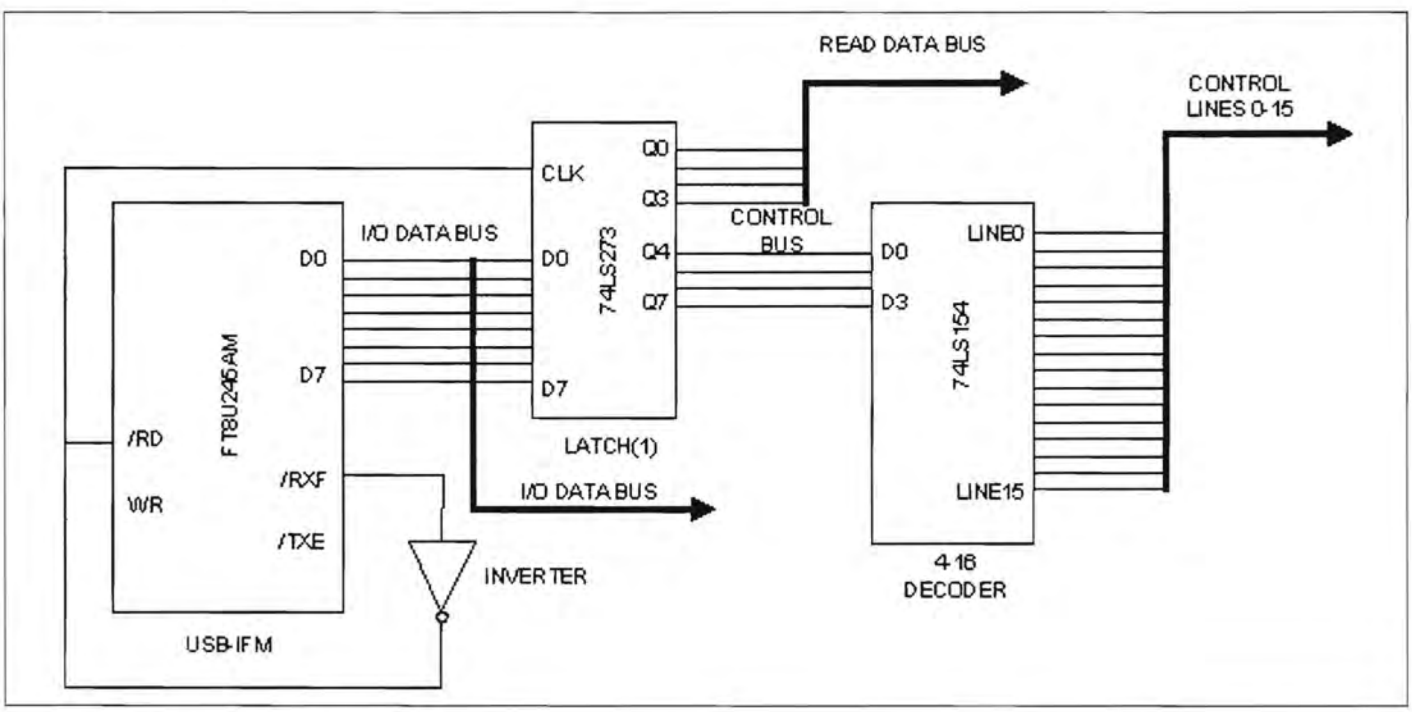


Figure 5: USB-IFM logic interface circuit

The operation is as follows: Initially the USB-IFM Receive Buffer is empty and so the output RXF# is "1" and RD# is "0". The PC sends a data byte to the USB-IFM Receive Buffer and RXF# is automatically set to "0". After a short delay, RD# and CLK of Latch (1) become "1" via the inverter. The data byte is latched into the Latch (1) and this also causes RXF# to become "1", indicating no more data is available to be read, which in turn sets RD# to low after short delay. The system is now ready to receive more data from the PC or to transmit data to the PC.

Control instructions and operations

The PC receives data one byte at a time from the USB-IFM Transmit Buffer using the instruction FT_Read. Similarly, it transmits data to the USB-IFM Receive Buffer one byte at a time using instruction FT_Write. Any data byte received by USB-IFM is divided by the logic circuit into two parts, the 4 least significant bits (LSBs) as the Read Data Bus and the 4 most significant bits (MSBs) as the Control Bus.

The Control Bus is taken to the 4-16 decoder to select one of 16 Control Lines, which activates 16 different ICs in the data acquisition and measurement circuits as listed in **Table 1**.

The full logic circuit for interfacing USB-IFM to the DAC is shown in **Figure 6**. The 4-bit Read Data Bus and 3 Control Lines of the basic USB logic interface circuit (see **Figure 5**) are used. The main consideration is to supply the 12-bit data input from the 4-bit Read Data Bus.

The 4-bit Read Data Bus is extended to give a 12-bit input signal to the DAC by two additional latches, Latch (2) and Latch (3). The 4-bit Read Data Bus is connected directly to input bus D8-D11 of the DAC, to Latch (2), which outputs go to input bus D4-D7, and to Latch (3), which outputs go to input bus D0-D3. A mono-stable chip (74HC123) is inserted in the Control Line (3) to ensure that the control signal width is adjusted for correct DAC operation. Control Lines 1, 2 and 3 activate Latches (2) and (3) and the DAC, respectively.

The method of loading a 12-bit signal into the DAC is as follows: The PC sends a byte containing bits D0-D3 of the signal plus binary 2 (the Control Line for Latch (3)). Latch (3) is activated and bits D0-D3 appear at the corresponding inputs of the DAC. The PC sends a second byte containing bits D4-D7 of the signal plus binary 1 (the Control Line for Latch (2)). Latch (2) is activated and bits D4-D7 appear at the corresponding inputs of the DAC. The PC sends a third byte containing bits D8-D11 of the signal and binary 3 (the Control Line for the DAC). Bits D8-D11 of the signal appear at the corresponding inputs of the DAC so that the complete 12-bit signal now appears at the DAC inputs bus. The Control Line (3) signal now locks out the DAC

Table 1: Control line connections

Control lines	*Activated unit*	*Board location*
0	Data acquisition Latch (4)	Data acquisition card
1	Data acquisition Latch (2)	Data acquisition card
2	Data acquisition Latch (3)	Data acquisition card
3	DAC	Data acquisition card
4	MUX+DC PGA	Data acquisition card
5	ADC	Data acquisition card
6	Measurement Latch (6)	Measurement channel PCB (6)
7	Measurement Latch (7)	Measurement channel PCB (7)
8	Measurement Latch (8)	Measurement channel PCB (8)
9	DDS Latch (1)	Signal generator PCB
10	DDS Latch (2)	Signal generator PCB
11	Measurement Latch (5)	Measurement channel PCB (5)
12	Measurement Latch (4)	Measurement channel PCB (4)
13	Measurement Latch (3)	Measurement channel PCB (3)
14	Measurement Latch (2)	Measurement channel PCB (2)
15	Measurement Latch (1)	Measurement channel PCB (1)

Table 2: DAC operation

USB-IFM instruction	*Activated unit*	*Control bus code*	*Read data bus code*
FT_Write	Latch (3)	2	Bits 0-3 DAC input
FT_Write	Latch (2)	1	Bits 4-7 DAC input
FT_Write	DAC	3	Bits 8-11 DAC input
FT_Write	(Reset)	8	Any data

inputs, so that the analogue output is held at the value sent by the PC.

The first FT_Write instruction sends data bits D0-D3 to Latch (3) and the second instruction sends data bits D4-D7 to Latch (2). The third instruction sends the data bits D8-D11 and activates the DAC with the complete data bits D0-D11. The final instruction does not activate a unit, but is used to reset the active Control Line to "1". It is used after all operations. The DAC operation is summarised in **Table 2**.

Logic circuit for interfacing ADC

The full logic circuit design for interfacing the USB-IFM to the ADC is shown in **Figure 7**. The 8-bit I/O Data Bus and Control Line (5) of the basic USB logic interface circuit (see Figure 5) are used. The 8 ADC output data lines D0-D3 (or D8-D11) and D4-D7 are connected to the 8-bit I/O Data Bus. The Control Line (5) is taken to the /RD input of the ADC via a D flip-flop (74LS74) and an AND gate.

The method of obtaining the 12-bit signal from the ADC is as follows: The PC sends a byte to USB-IFM containing binary 5 (the Control Line for the ADC) to activate the ADC conversion and the

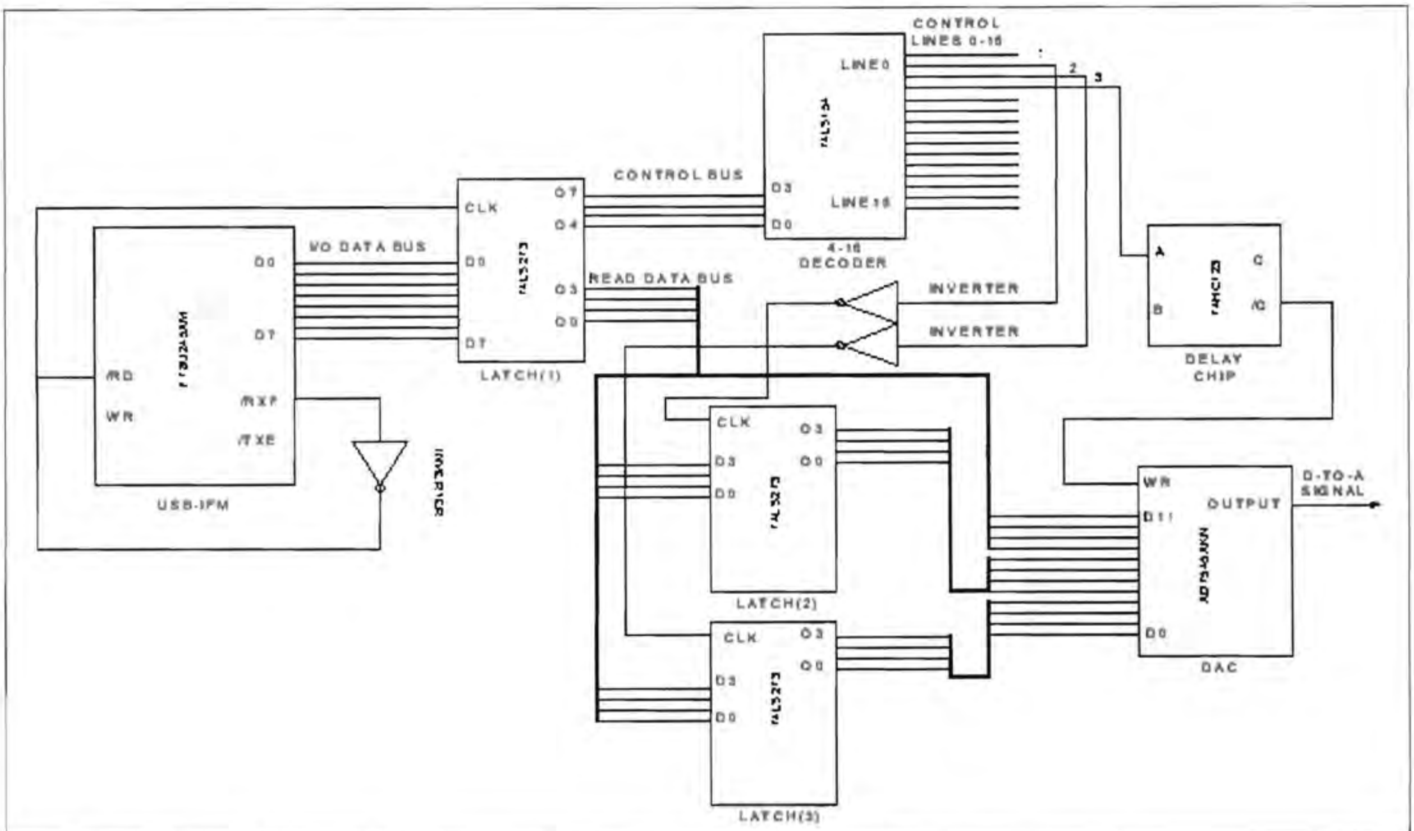


Figure 6: Interfacing USB-IFM to DAC

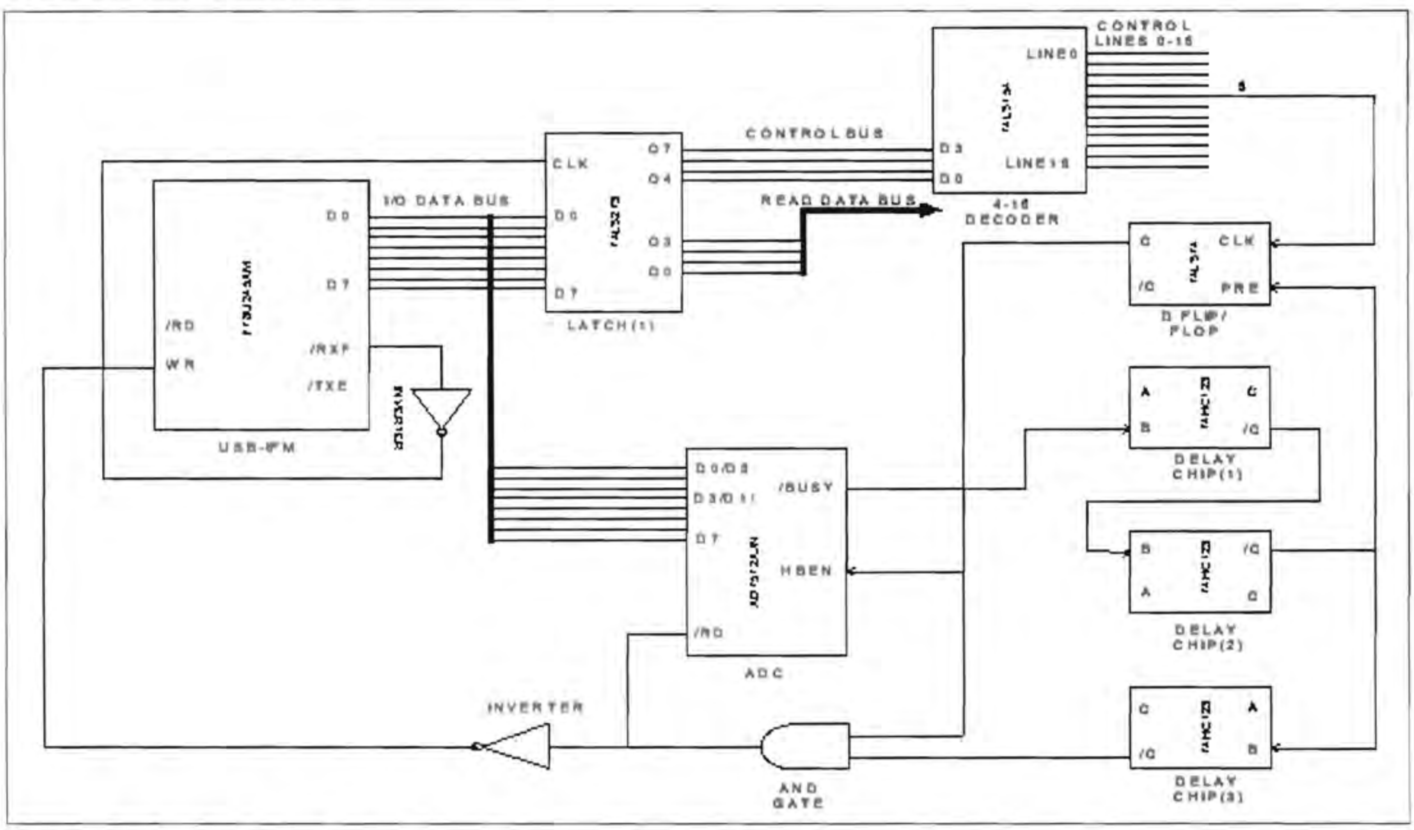


Figure 7: Interfacing USB-IFM to ADC

/BUSY signal goes low. At the end of conversion /BUSY goes high new data DB0-DB7 appear on the output lines of the ADC (since HBEN is low) and a sequence of three delay timers is initiated by using three delay chips (74HC123). After the first delay a WR signal is generated, which writes data DB0-DB7 into the USB-IFM Transmit Buffer. After the second delay HBEN is set high, the data DB8-DB11 plus four zeros appear on the ADC data output. After the third delay, a second WR signal is generated, which writes this data DB8-DB11 into the USB-IFM Transmit Buffer. The PC can now read the ADC conversion result from the USB-IFM Transmit Buffer in two bytes. The FT_Write instruction activates the ADC and also sends the result as two bytes to the USB-IFM Transmit Buffer via the logic circuits. The FT_Read instructions send these two bytes to the PC. They do not activate any unit or put any data on the Read Data Bus. The ADC operation is summarised in **Table 3**.

Interfacing USB-IFM to MUX and DC PGA

The full logic circuit design for interfacing USB-IFM to the MUX is shown in **Figure 8**. The 4-bit Read Data Bus and two Control Lines of the basic USB logic interface circuit (see **Figure 5**) are used. The 4-bit Read Data Bus is connected to Latch (3), whose outputs go to the input bus A0-A3 of the MUX. Control Lines (2) and (4) activate Latch (3) and the MUX, respectively.

The method of operating the MUX is as follows: The PC sends a byte to USB-IFM containing binary 2 (the Control Line for Latch (3)). Latch (3) is activated and the Read Data Bus data appear at the corresponding inputs of the MUX. The PC sends a second byte to USB-IFM containing binary 4 (the control line for the MUX). The MUX is activated, whose outputs select one channel according to the 4-bit Read Data Bus data.

The full logic circuit design for interfacing USB-IFM to the DC PGA is shown in **Figure 9**. The 4-bit Read Data Bus and two Control Lines of the basic USB logic interface circuit (see Figure 5) are used. The 4-bit Read Data Bus is connected to Latch (2), whose last three outputs go to input bus A1-A3 of the DC PGA. The Control Lines (1) and (4) activate Latch (2) and the DC PGA, respectively.

The method of operating the DC PGA is as follows: The PC sends a byte to USB-IFM containing binary 1 (the Control Line for Latch (2)). Latch (2) is activated and the Read Data Bus data appear at the corresponding inputs of the DC PGA. The PC sends a second byte to USB-IFM containing binary 4 (the Control Line for the DC PGA). The DC PGA is activated, whose outputs select a gain according to the last 3-bit Read data Bus data. Note that the Control Line (4) activates both the MUX and the DC PGA.

Table 3: ADC operation

USB-IFM instruction	*Activated unit*	*Control bus code*	*Read data bus code*
FT_Write	ADC	5	Any data
FT_Write	(Reset)	8	Any data
FT_Read	USB-IFM	X	X
FT_Read	USB-IFM	X	X

Table 4: MUX and DC PGA operation

USB-IFM instruction	*Activated unit*	*Control bus code*	*Read data bus code*
FT_Write	Latch (3)	2	Bits 0-3 MUX select
FT_Write	Latch (2)	1	Bits 1-3 DC PGA gain select
FT_Write	DC PGA and MUX	4	Any data
FT_Write	(Reset)	8	Any data

Table 5: Control lines operations of AD7008

USB-IFM instruction	*Activated unit*	*Control bus code*	*Read data bus code*
FT_Write	Data acquisition Latch (4)	0	3 (0011) activating RESET of AD7008
FT_Write	Data acquisition Latch (4)	0	0 (0000) activating /WR of AD7008
FT_Write	Data acquisition Latch (4)	0	6 (0110) activating LOAD of AD7008

Table 6: Data lines operation of AD7008

USB-IFM instruction	*Activated unit*	*Control bus code*	*Read data bus code*
FT_Write	Data acquisition Latch (3)	2	Bits 0-3 for DDS data lines
FT_Write	(DDS 1 only) DDS Latch (1)	9	Bits 4-7 for DDS data lines
FT_Write	(DDS 2 only) DDS Latch (2) 1	0	Bits 4-7 for DDS data lines
FT_Write	Reset	8	Any data

The operation of the MUX and the DC PGA is summarised in **Table 4**.

The first instruction sends data bits D0-D3 to the 4-input channel select bits of the MUX via Latch (3). The second instruction sends data bits D1-D3 to the three gain select bits of the DC PGA via Latch (2). The third instruction activates both the MUX and the DC PGA.

Implementing DDS signal generators

The DDS chip AD7008 is a complex device and its control is more complicated than other units in the data acquisition system. A schematic diagram of the DDS signal generator board controlled by the USB data acquisition card is shown in **Figure 10**.

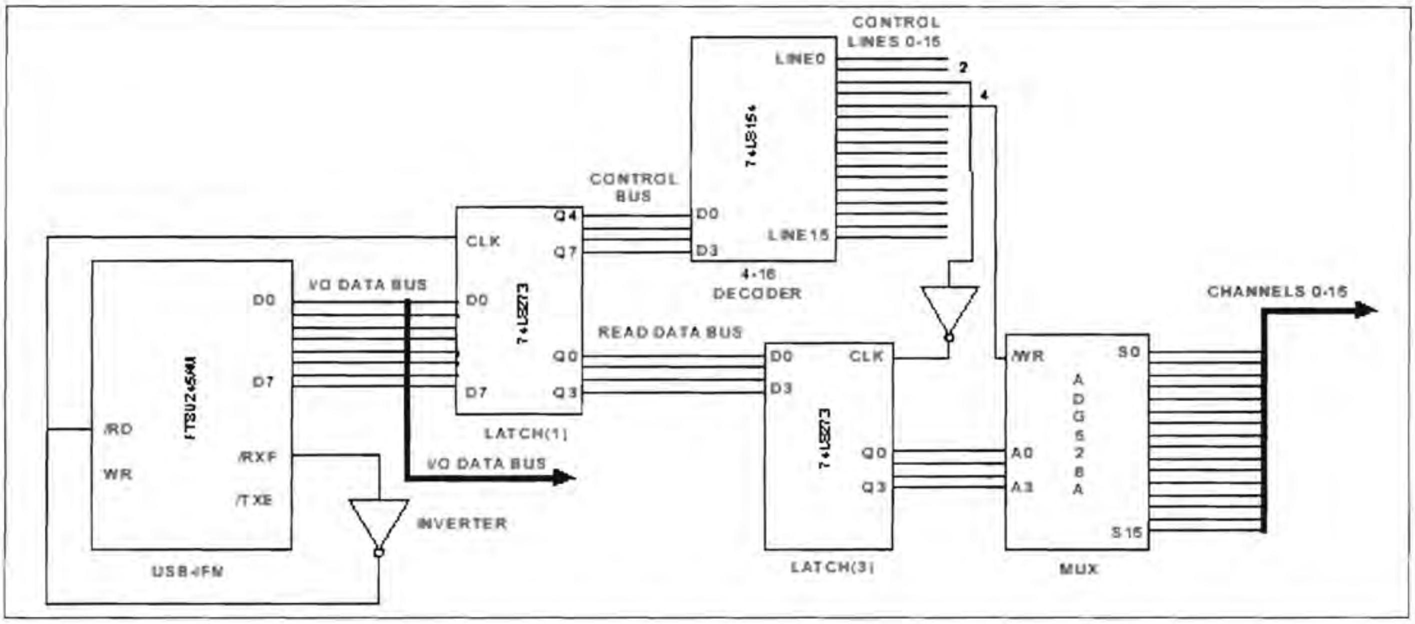


Figure 8: Interfacing USB-IFM to MUX

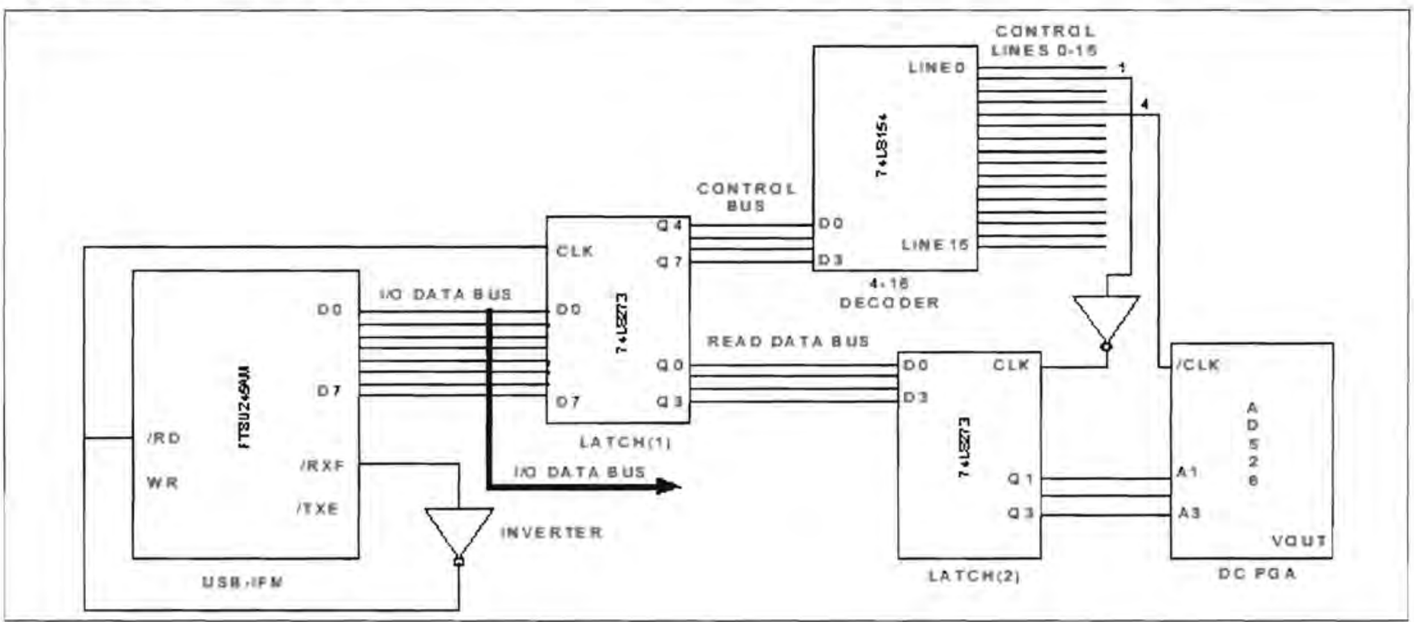


Figure 9: Interfacing USB-IFM to DC PGA

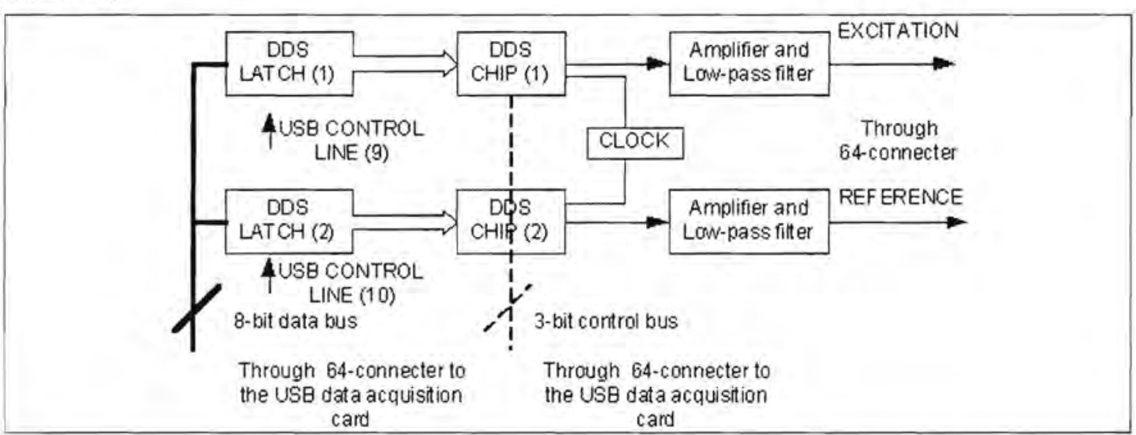


Figure 10: DDS signal generator board

The frequency, amplitude and phase of the DDS output sine waves are set by three internal registers, which must be loaded externally via the data inputs (D0 and D7) and a Parallel Assembly Register. The data inputs (D0-D7) of the DDS chips are supplied via the DDS latches. The input to these latches comes from data lines on the USB data acquisition card (4-bit Read Data Bus plus Latch (3)). The four LSBs of the DDS latch outputs are also connected to the DDS transfer logic inputs TC0-TC3. Once data has been written into the Parallel Assembly Register, these bits can be loaded into the appropriate internal register, according to the contents of TC0-TC3.

Control Lines (9) and (10) from the USB data acquisition card are used to set the DDS latches, but the control signals for the two DDS chips (i.e. RESET, /WR, and LOAD) are taken from the USB data acquisition card data lines to Latch (4) (bits 8 to 10).

The operation to set up the two DDS chips involves sending data to each chip via its individual latch and setting the three DDS control inputs via Latch (4) (on the USB data acquisition card) as listed in Tables 5 and 6. All control signals to AD7008 are connected to Latch (4) of the USB data acquisition card via a 64-connector. When the AD7008 is operated, the Control Bus is set to "0" and the Read Data Bus is set to activate the appropriate control input. The data lines of AD7008 are controlled by the USB data acquisition card through two latches DDS Latch (1) and DDS Latch (2). The first FT_Write instruction sends data bits D0-D3 to Latch (3) of the USB data acquisition card. The second instruction sends data bits D4-D7 and activates one of the DDS latches with the complete data bits D0-D7.

The software for the USB data acquisition card was written in Visual C++ 6.0, which is convenient for interfacing peripheral devices, display and design of user interface. **Figure 11** shows the Windows user interface. It has following functions:

- Control of the signal generator board;
- Management of the menu and setting of the system parameter and initialisation of the system;
- Control of the capacitance measurement boards and acquisition of the capacitance data;
- Control of the DAC and ADC to obtain the automatic DC offsets and gains functions;
- Real-time data acquisition.

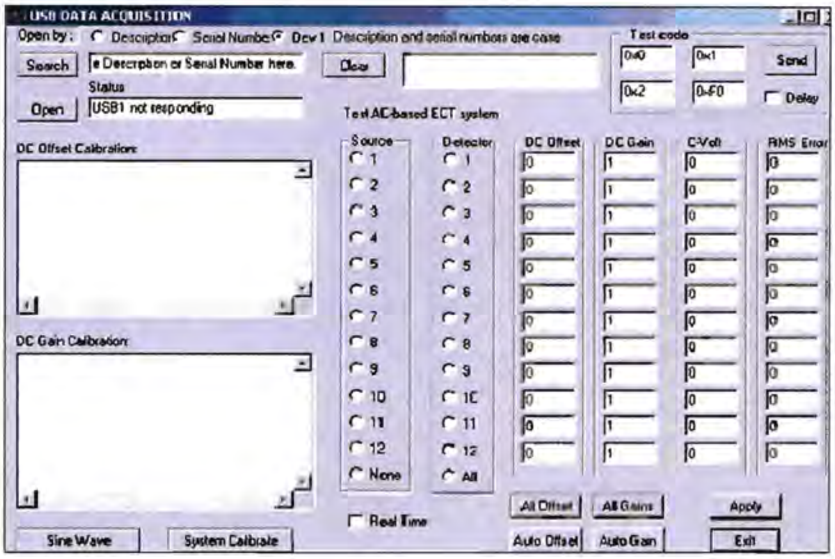


Figure 11: Windows user interface

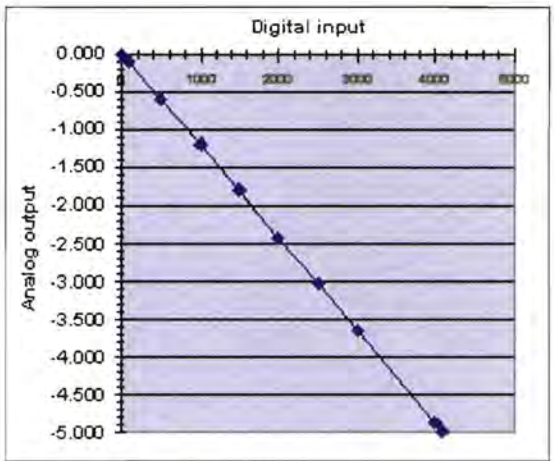


Figure 12: DAC test results

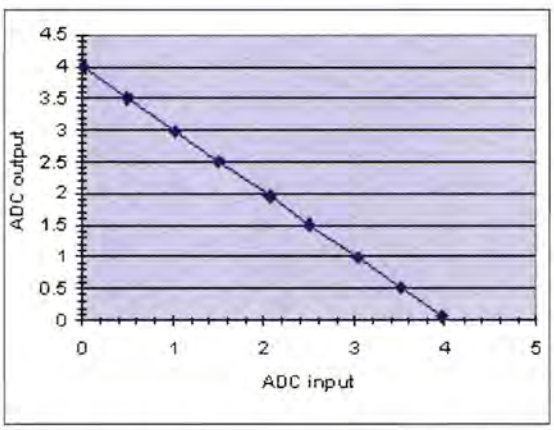


Figure 13: ADC test results

Experimental results

Figure 12 shows the test results of the DAC, showing the relationship between the input code and analogue output of the unipolar circuit. The test results show a maximum error of 0.03V (0.6% Full Scale) between the theoretical and actually DAC output.

Figure 13 shows the test results of the ADC, showing the relationship between the testing input voltages and the computer readings. The test results reveal that the computer reading has a maximum error 0.014V (0.35% Full Scale).

The generated sine-wave signals were examined using an oscilloscope as shown in **Figure 14**. Signal (1) was generated by DDS1 and signal (2) by DDS2. The results show that the signals are generated accu-

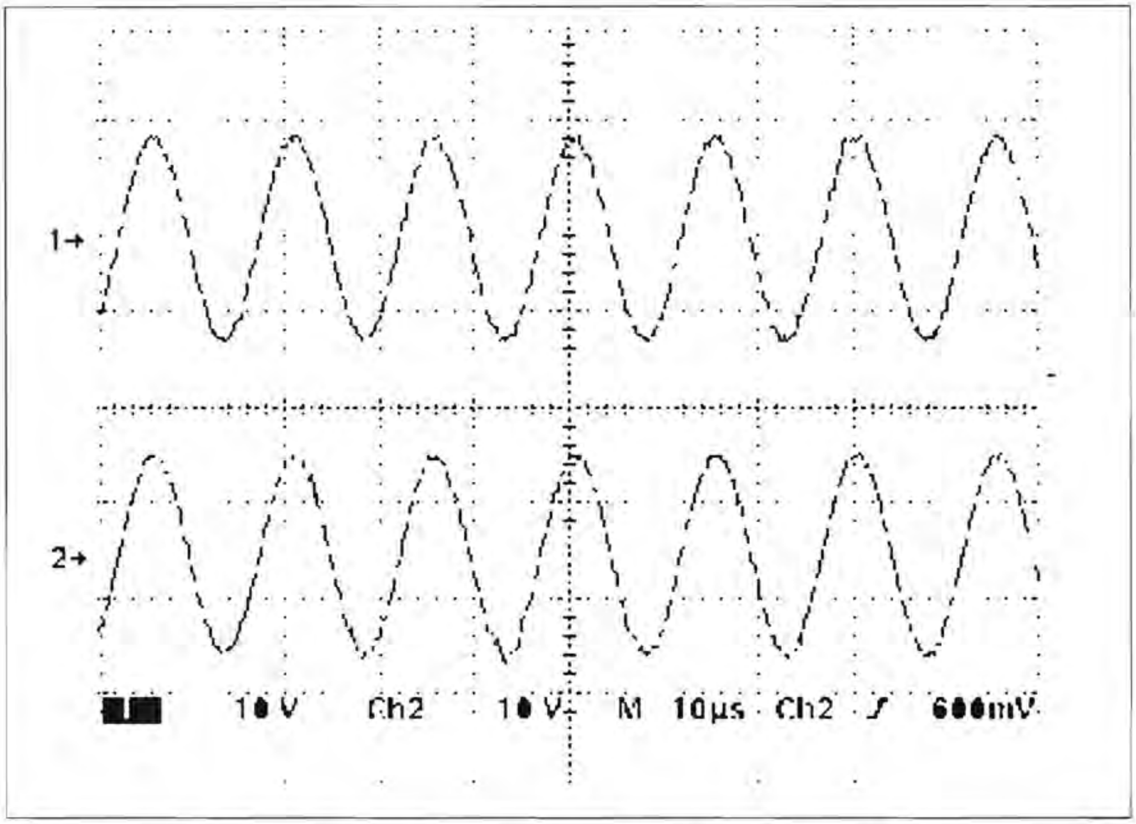


Figure 14: Sine-wave tests

rately in amplitude, frequency and phase difference, according to the values entered. With this generator, it is now possible to produce fully adjustable signals in terms of frequency, amplitude and phase difference.

The work described in this article was aimed at providing a high-speed USB data acquisition card for the new ECT system. The scope of the work included the design of the hardware of the card and the supporting software. The electronic circuits have been designed and a PCB has been made complying with the Eurocard standards. The card can support up to 12 capacitance measurement channels and has been successfully incorporated into the system. The software includes automatic calibration for obtaining the DC offsets to cancel the standing capacitance and the DC amplifier gain settings, and the collection of the measurement data for image reconstruction and analysis, together with a user friendly Windows interface.

The experimental results demonstrated that all functions designed are working satisfactorily. In principle, this design can be further developed to be a universal standalone data acquisition and signal generation unit.

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Creating USB device drivers from scratch

Mark Schultz, Staff Applications Engineer at Cypress Semiconductor, analyses in-depth the relationship between PC application software and the hardware that it controls. This article clears up some of the mysteries of Plug and Play and how the PC-based application software accesses a USB device

Have you ever wondered what is happening when Windows shows the message "New hardware found"? This is an example of Plug and Play, a Windows feature that allows for automatic configuration of PC hardware. For the developer, a deeper knowledge of the exact relationship between the Windows operating system and PC hardware will aid in developing Plug and Play products.

The purpose of this article is not to show how to write USB peripheral firmware nor is it to discuss PC applications. Rather, it is meant to tie the two sides so the interaction between them can be fully understood.

Windows 98 opens door to 'drivers'

Beginning with Windows 98, it was no longer possible for application software to communicate directly with PC hardware. This task was now the job of a "device driver". Device drivers are specialised pieces of code that are designed for specific pieces of hardware. When new hardware is detected, Windows attempts to load the applicable device driver.

But, how does Windows know what device driver to use with a certain hardware device? The answer is the core topic of this article. The piece of information that ties the whole process together is the information file, which usually resides in the \Windows\inf directory and has a file extension of ".inf". This file contains the name and location of the device driver to be used, as well as some identifying numbers used to match up device drivers to hardware devices. These numbers are the Vendor ID (VID) and Product ID (PID). Thus, when a USB device is attached, Windows interrogates the device to find its VID and PID and then searches the \Windows\inf directory to find information that binds the VID and PID to a device driver. That device driver is then loaded.

As the application software will need to communicate with the device, it first accesses the device driver by obtaining a "handle" to the driver and then checks to make sure that the hardware associated with this particular handle to the driver is, in fact, the hardware intended for this application. The application can then use the driver's Application Programming Interface (API) to make driver calls to perform input and output.

However, how does the peripheral get the information over to the operating system? The answer is that with USB, data structures called Device Descriptors are used. They contain the information about the attached device, including the VID and PID, the available endpoints, power requirements, etc. When Windows detects that a USB device has been attached, it needs to "enumerate" it, which consists of interrogating a device's descriptors and setting its logical address.

At this point, Windows has all of the information that it needs to talk to the USB device. Using information found in the descriptor data, it can then attempt to load a device driver specific to that device. The following section details how this connection is made.

Tying it all together

The piece that ties everything together is the information file, which contains the VID, PID and strings that we can use to help identify our device and a reference to the name and location of the driver file. This file is the key to making the design work. The Windows Plug and Play subsystem reads this file (or a copy of it) when the device is attached and loads the device driver specified in that file.

The first point of interest is the VID and PID section. In this case it is:

%USB\VID_1234&PID_5678.DeviceDesc%=CYUSB.Dev, USB\VID_1234&PID_5678

Note the reference to the VID and PID in this line. The hardware will report these numbers back to Plug and Play via the device descriptors.

At the bottom of the file is the strings section. This is where text associated with the device can be added. This text will show up in the Windows Device Manager as shown in **Figure 1**. Using the strings section is a good way to tell whether our design and associated device driver have actually connected properly.

VID_1234&PID_5678.DeviceDesc="Example USB Design"

If we look at the list of USB devices in Device Manager, we can see the string that was mentioned previously. This entry will appear in Device Manager each time our device is attached.

The final point of interest in the inf file is the driver section. Shown next is the section where the actual device driver is associated with the VID and PID of our device. This line contains a

Figure 1: Device Manager showing our example of a USB design

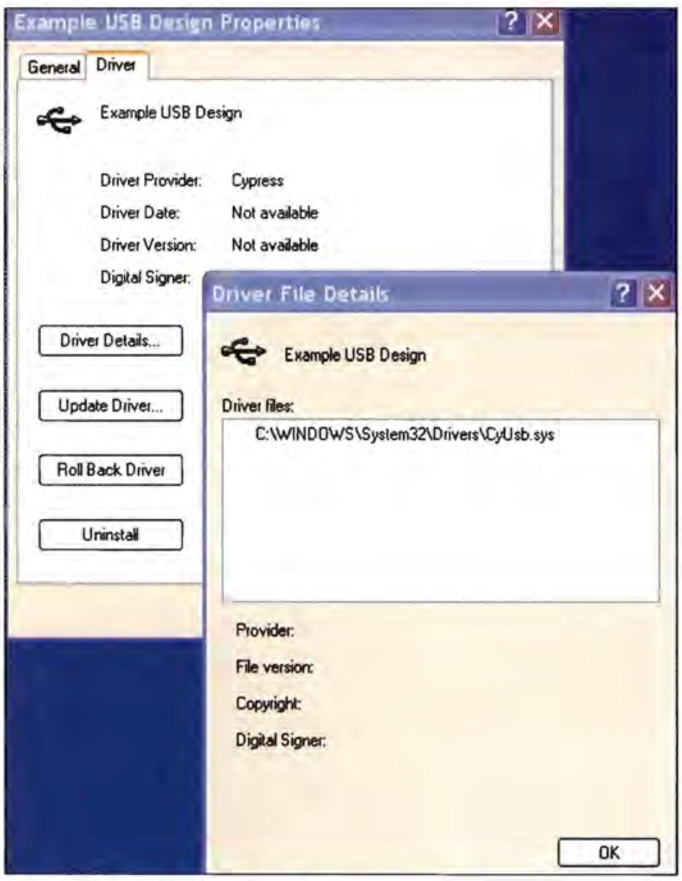


Figure 2: Driver details in Device Manager

reference to our device driver, or cyusb.sys. This is the information that Windows uses to load the driver associated with the device. **Figure 2** shows the driver properties of our device.

ServiceBinary = %10%\System32\Drivers\cyusb.sys

Hardware support for Plug and Play

USB communication occurs over logical pipes called endpoints. Each device endpoint has an associated descriptor. So, when Windows gathers all of a device's descriptors, there should be one or more endpoint descriptors used to specify input and/or output pipes that can be used by the application.

All of our descriptor information is stored in a file called dscr.a51. By viewing this file, we can see the same information that Windows will see after the Plug and Play process. To make our design unique, we will need to substitute in our own VID and PID. Note that the VID and PID are 16-bit values that must be obtained from the USB Interface Group. These numbers will be unique to your design. Information about how to obtain a VID and PID can be found at www.usb.org/developers/vendor/

For this particular example, I have created arbitrary VID and PID values. Please note that this is not an accepted practice. In an actual design, you will need to obtain a VID and PID using the URL listed above. We will also need to edit the endpoint information for our design.

As previously mentioned, all of the descriptor information for our design will be stored in one file. Portions of this file are shown in the following section. These descriptors will be used the Plug and Play subsystem to determine the characteristics of our USB device.

First, we start off by replacing the VID and PID fields in the Device Descriptor with our particular values. Here we can see that I have used a 1234 for the VID and a 5678 for the PID. Note that since our USB microcontroller contains an 8-bit CPU, we need to represent our VID and PID in Little Endian format. Thus, 1234 will be represented as 3412 and 5678 will be represented as 7856.

```
DeviceDscr:
  db DSCR_DEVICE_LEN    ;; Descriptor length
  db DSCR_DEVICE        ;; Descriptor type
  dw 0002H              ;; Specification Version (BCD)
  db 00H                ;; Device class
  db 00H                ;; Device sub-class
  db 00H                ;; Device sub-sub-class
  db 64                 ;; Maximum packet size
  dw 3412H              ;; Vendor ID
  dw 7856H              ;; Product ID (Sample Device)
  dw 0000H              ;; Product version ID
  db 1                  ;; Manufacturer string index
  db 2                  ;; Product string index
  db 0                  ;; Serial number string index
  db 1                  ;; Number of configurations
```

Next, we need to modify the endpoint descriptors. The only field that needs to be modified here is the "Endpoint number". USB allows seven bits for endpoint addressing. Thus, there can be a maximum of 128 endpoints connected to a USB port. The eight bit is used to determine the direction of communication. If this bit is set, then the direction is IN – from the peripheral to the PC. If this bit is cleared, then the direction is set to OUT.

```
;; Endpoint Descriptor
  db DSCR_ENDPNT_LEN    ;; Descriptor length
  db DSCR_ENDPNT        ;; Descriptor type
  db 04H                ;; Endpoint number, and direction
  db ET_BULK            ;; Endpoint type
  db 00H                ;; Max packet size (LSB)
  db 02H                ;; Max packet size (MSB)
  db 00H                ;; Polling interval
```

```
;; Endpoint Descriptor
  db DSCR_ENDPNT_LEN  ;; Descriptor length
  db DSCR_ENDPNT            ;; Descriptor type
  db 88H              ;; Endpoint number, and direction
  db ET_BULK          ;; Endpoint type
  db 00H              ;; Max packet size (LSB)
  db 02H              ;; Max packet size (MSB)
  db 00H              ;; Polling interval
```

Note that for the second descriptor, bit seven has been set in the Endpoint number field. This denotes that this is an IN endpoint.

Now, when the descriptors are read, Windows will see that there are two endpoints available for communication – one in the OUT direction, the other in the IN direction. The logical addresses of these two endpoints are 4 and 8.

Software access to the hardware

The first thing we need to do is to obtain a "handle" to the driver. A handle is nothing more than a 32-bit value, which is returned by Windows that can be used from here on out to access the device driver. You may have seen code similar to what is shown below. This is how one would access a PC COM port:

```
comOneHandle = CreateFile( "COM1",
        GENERIC_READ|GENERIC_WRITE, 0, 0,
        OPEN_EXISTING, FILE_ATTRIBUTE_NORMAL, 0);
```

Our case is not that different except that our filename will be "\\.\cyusb-0". So, our code will be:

```
DeviceHandle = CreateFile( "\\\\.\\cyusb-0", GENERIC_WRITE,
        FILE_SHARE_WRITE,
     NULL, OPEN_EXISTING, 0, NULL);
```

Next, we want to get the descriptor information for the device. To do this, we can use a DeviceIoControl call as follows:

```
bResult = DeviceIoControl( DeviceHandle,
        IOCTL_Ezusb_GET_DEVICE_DESCRIPTOR,
        NULL, 0, pvBuffer, sizeof(USB_DEVICE_DESCRIPTOR),
    &nBytes, NULL);
```

Using the information found in the descriptor, we can check the VID and PID to insure that the handle that we have acquired is for a driver that is truly bound to our devices as follows:

```
  UsbDesc = (PUSB_DEVICE_DESCRIPTOR)pvBuffer;

  if( (UsbDesc->idVendor == 0x1234) && (Usb_Desc-
>idProduct == 0x5678) )
  {
        bDeviceFound = 1;
  }
```

To write to our device, we can use the following code:

```
  Status = DeviceIoControl( DeviceHandle,
        IOCTL_EZUSB_BULK_WRITE, pBuffer,
        sizeof(BULK_TRANSFER_CONTROL), CfgData,
        count, &nBytes, NULL);
```

Note that CfgData is a data structure containing endpoint information that we had previously obtained from one of the USB descriptors.

Further enhancements

Now that we are familiar with using CreateFile to access the device handle and DeviceIoControl to perform input and output to the device, I should mention some new developments that have yielded a product, which is much friendlier to the application writer. The Cypress CyAPI is a C++ wrapper over the device interface discussed in the previous sections. With one line of C++ code, the device handle can be obtained as well as all descriptor information. The format of this new API is shown below:

```
  USBDevice = new CCyUSBDevice();
```

To write to the peripheral device:

```
  if(USBDevice->BulkOutEndPt)
        USBDevice->BulkOutEndPt->XferData(OutBuf, Size);
```

where OutBuf is a pointer to an array of bytes to write and Size is the number of bytes.

To read from the peripheral device:

```
  if(USBDevice->BulkOutEndPt)
        USBDevice->BulkInEndPt->XferData(OutBuf, Size);
```

where OutBuf is a pointer to an array of bytes that will be returned by the USB peripheral and Size is the number of bytes.

The new and improved driver API has a number of advanced methods as well, but using just these three, I have been able to create numerous applications.

Summary

In this article, we have seen the relationship between PC application software and the hardware that it controls. We have seen how to access a device driver from a PC application and how the device driver is matched to the hardware device via the inf file. Using a couple of simple techniques, we can easily create USB communication pipes for various applications. Further advancements have been made to streamline this process on both, software and hardware ends.

DESIGNERS NOTE: On the hardware side, Cypress provides a number of design templates, which can be easily adapted to meet the requirements of a particular application. These include examples of various types of USB transfers as well as various reference designs.

USB device access in C#

By Greg Nalder
Cypress Semiconductor

C# is a great language for quickly developing attractive Graphical User Interface (GUI) applications for Windows. However, the managed Common Language Runtime, on which C# programs depend, does not provide easy direct access to the Win32 Device I/O APIs (application programming interfaces). Consequently, programmers requiring low-level access to device drivers are confronted with a major obstacle when attempting to implement their applications in C#.

A common example of this is the need for the designer of a new USB device to whip up a little Windows utility program that can send the device a vendor-specific control endpoint command. Quickly creating the GUI for the utility is the strength of the C# environment. Unfortunately, when it's time to establish the actual communication path to the prototype device, the project becomes exponentially more complex.

This article will pursue the task of sending a control-endpoint request to a USB device that is served by Cypress Semiconductor's CyUSB.sys device driver.

Accessing the Win32 APIs

The Win32 API provides libraries of functions that are needed to access USB devices via their device driver. These functions are collected in the Windows files, kernel32.dll and setupapi.dll. The most used of these functions is the one that actually sends commands to the device driver, DeviceIoControl. This function, however, takes as its first parameter, a handle to the device. So, our first major task it to get a handle to the device.

Obtaining a handle to our USB device requires calling several other setupapi.dll functions. Here's a list of the Win32 API functions that are needed:

SetupDiGetClassDevsA
SetupDiEnumDeviceInterfaces
SetupDiGetDeviceInterfaceDetail
SetupDiDestroyDeviceInfoList
CreateFile
CloseHandle
DeviceIoControl

Accessing these Win32 functions from C# requires using what is called Platform Invoke (or Pinvoke, for short). Pinvoke involves declaring each function with a special C# attribute to indicate that the function will be imported from a Win32 DLL. In addition, it is extremely important to declare the external functions with a C# parameter list that will conform to the parameter list actually expected by the function in the DLL.

Table 1 opposite shows these seven functions with their normal C prototypes and their new, Pinvoke prototypes. These Pinvoke prototypes also refer to three new user-defined classes, which are defined as:

```
[StructLayout(LayoutKind.Sequential, Pack=1)]
public class SP_DEVINFO_DATA
{
    public int cbSize;
    public Guid ClassGuid;
    public uint DevInst;
    public uint Reserved;
}
```

Win32 C Prototype	C# Pinvoke Prototype
HDEVINFO **SetupDiGetClassDevs** (const GUID* ClassGuid, PCTSTR Enumerator, HWND hwndParent, DWORD Flags);	[DllImport("setupapi.dll", SetLastError=true)] public static extern IntPtr **SetupDiGetClassDevs** (ref Guid ClassGuid, uint Enumerator, IntPtr hwndParent, uint Flags);
BOOL **SetupDiEnumDeviceInterfaces** (HDEVINFO DeviceInfoList, PSP_DEVINFO_DATA DeviceInfoData, const GUID* InterfaceClassGuid, DWORD MemberIndex, PSP_DEVICE_INTERFACE_DATA DevInterfaceData);	[DllImport("setupapi.dll", SetLastError=true)] public static extern bool SetupDiEnumDeviceInterfaces (IntPtr DeviceInfoList, uint DeviceInfoData, ref Guid InterfaceClassGuid, uint MemberIndex, SP_DEVICE_INTERFACE_DATA DevInterfaceData);
BOOL **SetupDiGetDeviceInterfaceDetail** (HDEVINFO DeviceInfoSet, PSP_DEVICE_INTERFACE_DATA DevInterfaceData, PSP_DEVICE_INTERFACE_DETAIL_DATA DetailData, DWORD DataSize, PDWORD RequiredSize, PSP_DEVINFO_DATA DeviceInfoData);	[DllImport("setupapi.dll", SetLastError=true)] public static extern bool SetupDiGetDeviceInterfaceDetail (IntPtr DeviceInfoSet, SP_DEVICE_INTERFACE_DATA DevInterfaceData, byte[] DetailData, int DataSize, ref int RequiredSize, SP_DEVINFO_DATA DeviceInfoData);
BOOL **SetupDiDestroyDeviceInfoList** (HDEVINFO DeviceInfoSet);	[DllImport("setupapi.dll", SetLastError=true)] public static extern bool **SetupDiDestroyDeviceInfoList** (IntPtr DeviceInfoSet);
HANDLE **CreateFile** (LPCTSTR lpFileName, DWORD desiredAccess, DWORD shareMode, LPSECURITY_ATTRIBUTES securityAttributes, DWORD createDisposition, DWORD Flags, HANDLE hTemplateFile);	[DllImport("kernel32.dll", SetLastError=true)] public static extern IntPtr **CreateFile** (byte[] filename, [MarshalAs(UnmanagedType.U4)] FileAccess fAccess, [MarshalAs(UnmanagedType.U4)] FileShare fShare, int securityAttributes, [MarshalAs(UnmanagedType.U4)] FileMode fMode, int flags, IntPtr template);
BOOL **CloseHandle** (HANDLE hObject);	DllImport("kernel32.dll", SetLastError=true)] public static extern bool **CloseHandle** (IntPtr hObject);
BOOL **DeviceIoControl** (HANDLE hDevice, DWORD IoControlCode, LPVOID InBuffer, DWORD InBufSize, LPVOID OutBuffer, DWORD OutBufSize, LPDWORD BytesReturned, LPOVERLAPPED OverLapped);	[DllImport("kernel32.dll", SetLastError=true)] public static extern bool **DeviceIoControl** (IntPtr hDevice, uint IoControlCode, byte[] InBuffer, int InBufSize, byte[] OutBuffer, int OutBufSize, ref int BytesReturned, OVERLAPPED OverLapped);

```
          [StructLayout(LayoutKind.Sequential, Pack=1)]
          public class SP_DEVICE_INTERFACE_DATA
{
          public int cbSize;
          public Guid InterfaceClassGuid;
          public uint Flags;
          public uint Reserved;
}

          [StructLayout(LayoutKind.Sequential, Pack=1)]
          public class OVERLAPPED
{
          public uint   Internal;
          public uint   InternalHigh;
          public uint   Offset;
          public uint   OffsetHigh;
          public IntPtr hEvent;
}
```

Notice that these three new datatypes have been defined as classes and not as structs. This will prove a prudent choice when we get ready to pass instances of these classes in the actual calls to the setupapi.dll functions. Once all the Win32 APIs have been given C# Pinvoke declarations and the needed parameter classes have been defined, as shown above, we are finally ready to obtain a handle to a device.

Below is an important code snippet that demonstrates this process in C#. Those familiar with this process, from C or C++ programming, will recognise the five SetupDiXxxx function calls required. Rather than focus on the purpose of those calls, let's examine some C# nuances pertaining to them.

```
          public const uint DIGCF_PRESENT          = 0x00000002;
          public const uint DIGCF   _INTERFACE_DEVICE = 0x00000010;
          public const int  FILE_FLAG_OVERLAPPED         = 0x40000000;
          public static IntPtr INVALID_HANDLE       = new IntPtr(-1);

          // This is the GUID for the CyUSB.sys driver
public static Guid DrvGuid = new Guid ( "{0xae18aa60, 0x7f6a, 0x11d4, {0x97, 0xdd, 0x0, 0x1, 0x2, 0x29, 0xb9, 0x59}}" );


          private void GetDeviceHandle(uint dev)
{
          int predictedLength = 0;
          int actualLength = 0;

          IntPtr hwDeviceInfo = SetupDiGetClassDevs (ref DrvGuid, 0, IntPtr.Zero,
                              DIGCF_PRESENT | DIGCF_INTERFACEDEVICE);
          if (hwDeviceInfo.ToInt32() == -1) return;

SP_DEVICE_INTERFACE_DATA  devInterfaceData = new SP_DEVICE_INTERFACE_DATA();
devInterfaceData.cbSize = Marshal.SizeOf(devInterfaceData);
if (! SetupDiEnumDeviceInterfaces (hwDeviceInfo, 0, ref DrvGuid, dev, devInterfaceData)) return;

SetupDiGetDeviceInterfaceDetail (hwDeviceInfo, devInterfaceData, null, 0, ref predictedLength, null);

byte[] detailData = new byte[predictedLength];
detailData[0] = 5; // Set the cbSize field of what would be a SP_DEVICE_INTERFACE_DETAIL_DATA struct
if (! SetupDiGetDeviceInterfaceDetail (hwDeviceInfo, devInterfaceData, detailData,
predictedLength, ref actualLength,null) ) return;

// Move the chars of the DevicePath field to the front of the array.
```

```
        for (int i=0; i<(actualLength-4); i++) detailData[i] = detailData[i+4];
        hDevice = CreateFile (detailData, FileAccess.ReadWrite, FileShare.ReadWrite, 0, FileMode.Open,
        FILE_FLAG_OVERLAPPED,IntPtr.Zero);

        SetupDiDestroyDeviceInfoList(hwDeviceInfo);
}
```

In the above code snippet, let's first consider the call to SetupDiEnumDeviceInterfaces. You'll notice that, for the last parameter, the Win32 setupapi.dll is actually expecting a pointer to an **SP_DEVICE_INTERFACE_DATA** object. Since our variable, devInterfaceData, was defined as a class, rather than a struct, a pointer to our object actually gets passed without using the ref keyword in the parameter list. In contrast, the DLL expects a pointer to a GUID as the second parameter. Here, we must explicitly cause a pointer to be passed by qualifying the DrvGuid parameter with the **ref** keyword.

Even more interesting are the next two calls to SetupDiGetDeviceInterfaceDetail. Both take our devInterfaceData variable (now filled with valid data from the previous SetupDiEnumDeviceInterfaces call) as the second parameter. And, as in the previous call, we just pass the variable, not a **ref** to it, even though the DLL is expecting a pointer.

```
        SetupDiGetDeviceInterfaceDetail (hwDeviceInfo, devInterfaceData, null, 0, ref predictedLength, null);
```

The first call to SetupDiGetDeviceInterfaceDetail is made to find-out the size of buffer we need to pass in the second call. For this call we just pass null for the third parameter and 0 for the fourth. These values tell the function that we're really just asking for the buffer size required.

```
        byte[] detailData = new byte[predictedLength];
        detailData[0] = 5;  // Set the cbSize field of what would be a SP_DEVICE_INTERFACE_DETAIL_DATA struct
        if (! SetupDiGetDeviceInterfaceDetail (hwDeviceInfo, devInterfaceData, detailData,
                predictedLength, ref actualLength,null) ) return;
```

The second call to SetupDiGetDeviceInterfaceDetail is where things get dicey. Consider the third parameter in the call. The setupapi DLL expects a pointer to an **SP_DEVICE_INTERFACE_DETAIL_DATA** structure. However, in reality, it just wants a pointer to a block of contiguous bytes that we allocate before making the call. The **SP_DEVICE_INTERFACE_DETAIL_DATA** structure declaration is simply an access mechanism into the block of bytes, making it simpler to access the DevicePath field within the block.

The **SP_DEVICE_INTERFACE_DETAIL_DATA** structure is defined, in C, as:

```
        typedef struct _SP_DEVICE_INTERFACE_DETAIL_DATA {
                DWORD cbSize;
                TCHAR DevicePath [ANYSIZE_ARRAY];
        } SP_DEVICE_INTERFACE_DETAIL_DATA ;
```

So, just as we would do in C or C++, an array of bytes is allocated. In C or C++, we would then assign a pointer to a **SP_DEVICE_INTERFACE_DETAIL_DATA** structure to the beginning of the allocated buffer. This would allow us to conform to the function prototype syntax and pass a pointer to the right type of structure. C#, however, doesn't accommodate this structure imposition. So, instead, we just pass the block of bytes and manipulate it explicitly, given our knowledge of the **SP_DEVICE_INTERFACE_DETAIL_DATA** structure. Again, even though the setupapi DLL expects a pointer for the third parameter, we just pass the name of our byte array (detailData) and C# supplies a pointer when the call is made.

```
        // Move the chars of the DevicePath field to the front of the array.
        for (int i=0; i<(actualLength-4); i++) detailData[i] = detailData[i+4];
        hDevice = CreateFile (detailData, FileAccess.ReadWrite, FileShare.ReadWrite, 0, FileMode.Open,
                FILE_FLAG_OVERLAPPED,IntPtr.Zero);
```

Finally, we are ready to call CreateFile to get the handle to the device. The first parameter is supposed to be the DevicePath field from the **SP_DEVICE_INTERFACE_DETAIL_DATA** structure. As seen in the declaration above, this is really just an array of characters (C# bytes). The cleanest thing to do, at this point, is just to re-use our already declared detailData array of bytes, moving the DevicePath field to the front of the array, overwriting the cbSize field.

One last point of interest is that the kernel32 DLL wants a handle as the last parameter to CreateFile. We just want to pass a null handle. C#'s IntPtr class facilitates this with a member called Zero.

Data buffers and pointers

The DeviceIoControl function is designed to allow passing of a buffer of bytes whose content is specific to the servicing driver. That is, each driver will interpret the byte-buffer in its own way. It is common for this buffer to include some sort of protocol or parameter header, followed by a section of data bytes (or empty bytes ready to receive data). Rather than configure the parameter header of the transfer buffer one byte at a time, it is much more convenient to use a data structure, with named fields, for the buffer. Unfortunately, since the data portion of the structure is not constant, it is not desirable to statically define such a structure. Rather, the common practice is to dynamically allocate a raw buffer of bytes. Then, declare a pointer to a structure representing the transfer block (including header fields and data section). The structure pointer is then assigned to point to the allocated array of bytes.
In C++, the header structure needed by the CyUSB.sys driver looks like this:

```
typedef struct _SINGLE_TRANSFER {
        unsigned char bmRequest; // 1 byte
        unsigned char bRequest;          // 1 byte
        unsigned short wValue;           // 2 bytes
        unsigned short wIndex;           // 2 bytes
        unsigned short wLength;          // 2 bytes
        unsignted long ulTimeout; // 4 bytes
        bool     WaitForever;     // 1 byte
        unsigned char EptAddress;        // 1 byte
        unsigned long NtStatus;          // 4 bytes
        unsigned long UsbdtStatus;       // 4 bytes
        unsigned long IsoPacketOffset;   // 4 bytes
        unsigned long IsoPacketLength;   // 4 bytes
        unsigned long BufferOffset;      // 4 bytes
        unsigned long BufferLength;      // 4 bytes
} SINGLE_TRANSFER ;
```

And, we map it onto a data buffer like this:

```
unsigned char * buffer;
unsigned char * dataBlock;
int dataBufLen = 1024;

// Allocate a buffer large enough for the data and the SINGLE_TRANSFER header
dataBlock = new unsigned char [dataBufLen + sizeof(SINGLE_TRANSFER)];

SINGLE_TRANSFER *xferBloc = (SINGLE_TRANSFER *) buffer;

xferBloc->BufferOffset = sizeof(SINGLE_TRANSFER); // Tells where the actual buffer data bytes begin
dataBlock = buffer + xferBloc->BufferOffset;
```

We want to do something like this in C#, but, the above operation is pointer-intensive and C# requires some special constructs and constraints if we want to use pointers. First, in order for our structure mapping to work, the structure must be declared as a C# struct (not a class) and must not include any 'managed' datatypes such as arrays or strings. The SINGLE_TRANSFER structure, declared in C# for use in our pointer mapping would look like this:

```
[StructLayout(LayoutKind.Sequential, Pack=1)]
public struct SINGLE_TRANSFER
{
        public byte     bmRequest;        // 1 byte
        public byte     bRequest;     // 1 byte
        public ushort   wValue;           // 2 bytes
```

```
        public ushort   wIndex;              // 2 bytes
        public ushort   wLength;             // 2 bytes
        public uint     ulTimeout;      // 4 bytes
        public byte     WaitForever;         // 1 byte - note: not bool
        public byte     EptAddress;          // 1 byte
        public byte     NtStatus;            // 4 bytes
        public uint     UsbdtStatus;         // 4 bytes
        public uint     IsoPacketOffset;     // 4 bytes
        public uint     IsoPacketLength;     // 4 bytes
        public uint     BufferOffset;        // 4 bytes
        public uint     BufferLength;        // 4 bytes
}
```

unsafe

Any C# context that wants to use pointers must be declared with the **unsafe** designator. This designator can be applied to a method or to an entire class.

When the **unsafe** designator is used, the C# compiler must be instructed to allow **unsafe** blocks of code. In the Microsoft Visual Studio.NET environment bring up the Project Property Pages dialog by selecting the **Project | Properties** menu item. In the dialog, select the **Configuration Properties** folder and the **Build** subitem. In the **Code Generation** section, set the **'Allow Unsafe Code Blocks'** to **true**.

fixed

In order to map a structure onto an array of bytes, we need to employ the C# **fixed** construct. The **fixed** construct essentially pins a block of memory to a fixed location for the duration of the **fixed** context.

The following function calls DeviceIoControl to perform a control endpoint data transfer via the CyUSB.sys driver. The function maps our new C# **SINGLE_TRANSFER** structure onto a byte buffer that was passed-in as a parameter.

```
public unsafe override bool BeginDataXfer (ref byte [] buffer, ref int len,  ref OVERLAPPED ov)
{
        fixed (byte *buf = buffer)
        {
        SINGLE_TRANSFER *transfer                = (SINGLE_TRANSFER*) buf;

        transfer->SetupPacket.bmRequest          = (byte)(Target | ReqType | Direction);
        transfer->SetupPacket.bRequest           = ReqCode;
        transfer->SetupPacket.wValue             = Value;
        transfer->SetupPacket.wLength            = (ushort) len;
        transfer->SetupPacket.wIndex             = Index;
        transfer->SetupPacket.dwTimeOut                  = tmo;
        transfer->WaitForever                    = 0;
        transfer->ucEndpointAddress              = 0x00;             // control pipe
        transfer->IsoPacketLength                = 0;

        transfer->BufferOffset       = SINGLE_XFER_LEN;  // size of the SINGLE_TRANSFER part
        transfer->BufferLength                   = (uint) len;

        int Xferred = 0;
        bRetVal = DeviceIoControl (hDevice, IOCTL_ADAPT_SEND_EP0_CONTROL_TRANSFER,
                buffer, len, buffer, len, ref Xferred, ov);

        len = Xferred;

        UsbdStatus = transfer->UsbdStatus;
        NtStatus = transfer->NtStatus;
        }

        LastError = (uint) Marshal.GetLastWin32Error();
```

```
        return bRetVal;
    }
```

It is important that the variables **buf** and **buffer**, in the **fixed** construct, are of the same base type (i.e. **byte**).

The C# method, Marshal.SizeOf( ) requires an object as its argument, not a data type. So, rather than always having to create an instance of **SINGLE_TRANSFER**, just to take its size, I chose to create a constant, **SINGLE_XFER_LEN**.

Notice, also, that the ability to get the last Win32 error, using the Marshal.GetLastWin32Error( ) method, is enabled by the SetLastError=true statement in the function attribute for DeviceIoControl (see the Pinvoke declaration in Table 1).

Conclusion

The ability to access USB devices from C# applications consists of two primary tasks. First, we must obtain a handle to the target device, then, we need to be able to manipulate and pass data buffers to the device driver. The problem solution is also twofold. First, we must declare the necessary data structures and function prototypes needed to access the Win32 APIs and, second, we need to map data structures onto a data buffer to easily manipulate the contents of the buffer.

The sample code presented in this article derives from a port of the Cypress CyAPI.lib file from C++ to C#. CyAPI.lib is part of the Cypress USB Developers' uStudio. The resulting .net class library, CyUSB.dll, has been exercised from C#, VB.net and managed C++ applications.

> **DESIGNERS NOTE:** This driver is a free download from Cypress's website. It can be matched to any USB 2.0 - compliant device. **www.cyrpess.com**

Catching the USB wave

Adrian Brain and Martin Dennet, Oxford Semiconductor

The Universal Serial Bus (USB) is doing a good job of living up to its name. The four-pin connector is turning up everywhere, from the humble memory stick to musical instruments. USB's rapid growth has led PC makers to question whether they need to support serial or parallel ports at all. Many have taken the decision to drop them entirely from their products, leaving makers of devices that support serial ports with nothing to plug into, unless the user buys a PCI card to add them.

There are good reasons for moving to USB. PC users find it much easier to deal with than the old world of serial ports with interrupts, COM ports and DIP switches to set in their peripherals. 'Plug and play', offered by USB, has become the expected norm for PC users.

The problem is many embedded devices still have serial ports on them to attach to PCs and other hosts. Although a growing number of mobile phones now use Bluetooth, many still have serial connections to work with desktop computers that are not fitted with the wireless communications standard. In the industrial and instrumentation fields, the serial port remains the standard in wide use today, thanks to the reach of a serial cable and because it is easy to work with. A data logger may need nothing more than a simple 8-bit microcontroller to run its software. This level of microcontroller has no problem dealing with a UART, which will often be integrated, but USB is a much more complicated proposition.

Serial-USB dongle

Where has the complexity gone?

Migrating to USB means more than simply changing a connector. Although both have 'serial' in their names, USB behaves much more like a network than a traditional serial bus.

USB was designed to make life easier for the end user of the equipment. The move to USB removed the burden of setting interrupts and addresses. However, the complexity now lies in the hands of the peripheral equipment or embedded systems designer. That designer has to come up with software that does what the user used to and, also, auto-configures the device. And that is not all. The device has to manage a much larger array of data structures than it would with a simple UART.

Dealing with a UART at the software level is a simple process. There's very little overhead in terms of memory, as the interrupt handlers that send and receive data are dealing with just a byte at a time, and maybe some routines for flow control when dealing with a host that can sustain high transfer rates. USB is a different matter – it involves a less direct process.

With USB, communication takes place between software-defined endpoints. An embedded system attached to USB will often have more than one endpoint, each with its own 4-bit address. Endpoint 0 has to be used for control information. For data, you have to use Endpoints 1 to 15.

For complex peripherals, such as scanners or digital scanners, this is not a bad thing. It lets the designer construct different virtual pipes for different tasks. For example, one virtual pipe may relay commands to the camera to let a PC act as a remote control. Another pipe might be used for retrieving the pictures it takes.

Table 1: Serial bus comparision

Interface	*Signaling*	*Max Data rat*	*Reach (m)*	*Nodes*	*Topology*
RS-232	Single ended	20 Kbps	15	1 transmitter, 1 receiver	Point to point
RS-422	Differential	10 Mbps	1200	1 transmitter, 10 receivers	Multi-drop
RS-485	Differential	10 Mbps	1200	32 transmitters, 32 receivers	Multi point star
USB@LS	Differential	1.5 Mbps	3	1 transmitter, 1 host, 127 devices	Tiered star with hubs
USB@fS	Differential	12 Mbps	5	1 transmitter, 1 host, 127 devices	Tiered star with hubs
USB@HS	Differential	480 Mbps	5	1 transmitter, 1 host, 127 devices	Tiered star with hubs

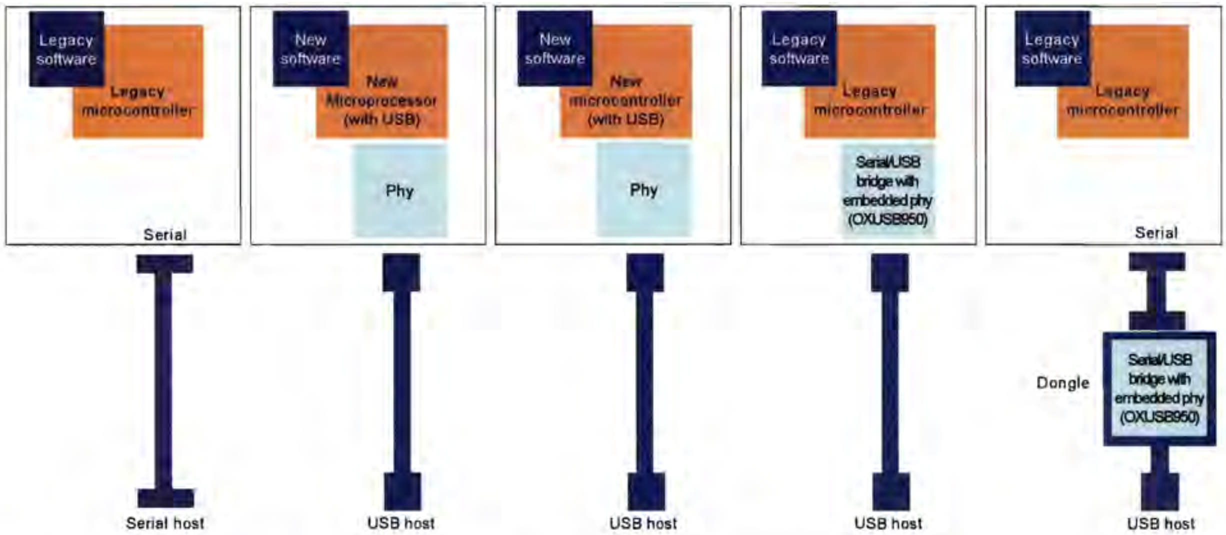


Figure 1: The options of migrating from serial to USB

The intricacies of USB operation

Unlike a serial port, USB does not transfer bytes one at a time. Everything has to be put into a packet, given a destination address and sent on its way. Equally, the USB peripheral cannot send packets when it has something to send. The USB host has to poll it first, a process that happens roughly every millisecond. USB interfaces carry out error checks as well, generating control messages that should result in a retransmission if there should be an error.

Getting the endpoints into place is not a trivial exercise. When the user plugs in a USB device to a computer's port, there is an enumeration phase. This is when the PC tries to work out what has just been plugged in, what address to give it and which types of transfer the device will support. Your embedded device has to be able to come up with the right answers to the questions that the host asks.

Although it behaves more like a network with its ability to be configured dynamically, USB is no Ethernet. It has a severely limited reach that is fine for a home or office PC but cannot support the long cable runs used in more industrial environments. As you can see in **Table 1**, USB's maximum cable length is three times lower than what is possible with an RS232 connection. The differential serial links, such as RS422, provide much greater cable lengths. More than 1km in total is possible. For those wondering why the low speed version of USB, running at 1.5Mbit/s, only has a maximum cable length of 3m, but the full- or high-speed versions can handle 5m, this is to do with cable quality rather than protocol issues. Low-speed peripherals, which will be devices such as keyboards and mice, are assumed to use low-quality cables that would degrade the signal too much to support the full 5m length.

Tackling USB design

Even if starting a new design from scratch, providing USB instead of a serial port is a formidable task unless your system is large enough to use a real-time operating system that has USB support already built in. For many 8-bit and 16-bit designs, this is not going to be the case. And, the chances are that you are not starting from scratch. You probably already have a design that works perfectly well with a serial interface. You may not have time or budget to design a new board with built-in USB and the firmware to go with it. It takes less than a day to come up with a serial driver and several weeks to implement basic USB support on a microcontroller. Or you may have a microcontroller with enough headroom to run its core software but not the memory to handle USB as well. What do you do then?

As illustrated in **Figure 1**, there's a number of options available, from buying a completely new microcontroller through to component choices that let you keep both your existing board and, perhaps more importantly, all of your existing software.

The biggest change is to replace your main microcontroller with one that has built-in support for USB. There are a number of problems with this approach. You will still have to produce new software to support the USB protocol stack – these microcontrollers have specific hardware support but the manufacturers cannot provide software for them that cover the range of possibilities that USB offers.

Perhaps the biggest problem with this approach is that you may have to rewrite your application. There are very few microcontroller architectures, if any, that do not have a family member with an integrated UART. The choice of microcontroller architectures with integrated USBs is very much smaller. A few vendors have made a point of providing USB-enabled microcontrollers but most have stuck with more traditional peripherals. In principle, this approach should have the lowest hardware cost but will, generally, work out to have the highest design

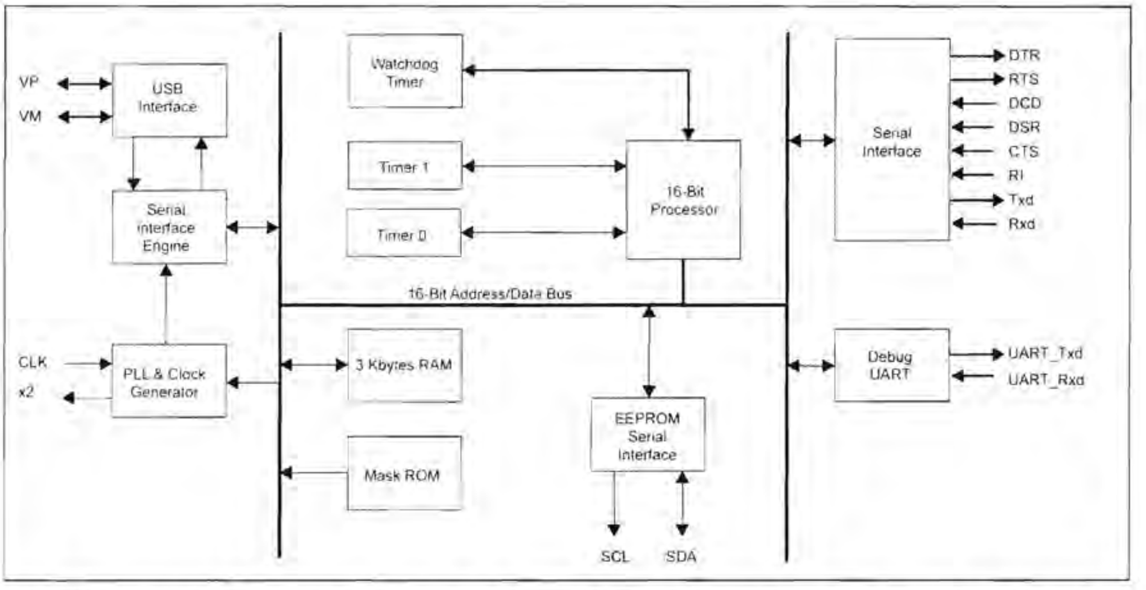


Figure 2: Block diagram of Oxford's OXUSB950 USB-serial bridge

costs. The question is, can you be sure to sell that many extra devices now that they have USB to justify the design cost?

If you want to keep your old microcontroller, you could just add one that does support USB to the board and then use bus transfers between two to pass data. This will involve rewriting some of the core software to support bus transfers rather than serial transfers, as well as the USB protocol software for the second microcontroller. This approach will command a higher hardware cost than the first option but will mean you get to keep most of your core software intact.

The third option is to have two microcontrollers as before but connect them through their integrated serial ports, assuming that both have them. Many dedicated USB microcontrollers do not have UARTs as well, which will restrict the choice you have for this option. There is a class of device that exists that not only provides a microcontroller with both USB and serial-port support but that implements the USB stack as well. This is the USB-serial bridge IC. An example is the Oxford Semiconductor OXUSB950 detailed in **Figure 2**. This type of device has the advantage of not demanding any changes to the device software. The microcontroller transfers bytes though the serial port as before. They are converted into a USB-friendly form by firmware running on the bridge on the other side of the serial interface. The main change to the design for this approach is to simply replace the old serial port connector and transceiver with the USB connector and bridge chip, which includes an integral PHY.

It is possible to add USB to a serial design without any design changes at all. This works by putting a USB-serial bridge into a cable or dongle and using that to map communications between the two protocols. This can work out to be the most expensive in terms of production costs, as you have to bear the cost of buying in an off-the-shelf cable or dongle if you do not want to design this additional product using a USB-serial bridge.

However, in markets where any hardware or software redesign will involve an expensive requalification process, this can be a cost-effective approach. The schematic of **Figure 3** shows a USB dongle implementation.

Great advantages?

The cable approach may have an advantage over integrating USB into the embedded device as it could allow the use of a longer serial cable on the device side, with a comparatively short connection to the PC. This way, you can get the reach of a serial standard such as RS422 and still work with USB-only PCs. The bridge chips generally have low enough power requirements to allow the dongle to be powered from the USB port. However, if cable length is not a consideration, the on-board use of a USB-serial bridge will often provide the best trade-off between redesign and production costs for moderate to high-volume products.

For certain high volume applications with occasional interface requirements, the USB dongle might actually represent the optimum solution, as in mobile phones, for example. When there's no room for integrating the interface into the product and, in any case, not every user wants the facility, it makes perfect sense to provide an interface cable as an accessory.

There is no need to be left off the USB bandwagon. The embedded systems designer has a number of ways of adding USB to an existing system and the arrival of dedicated bridge chips means that the burden of redesign can be reduced to a minimum.

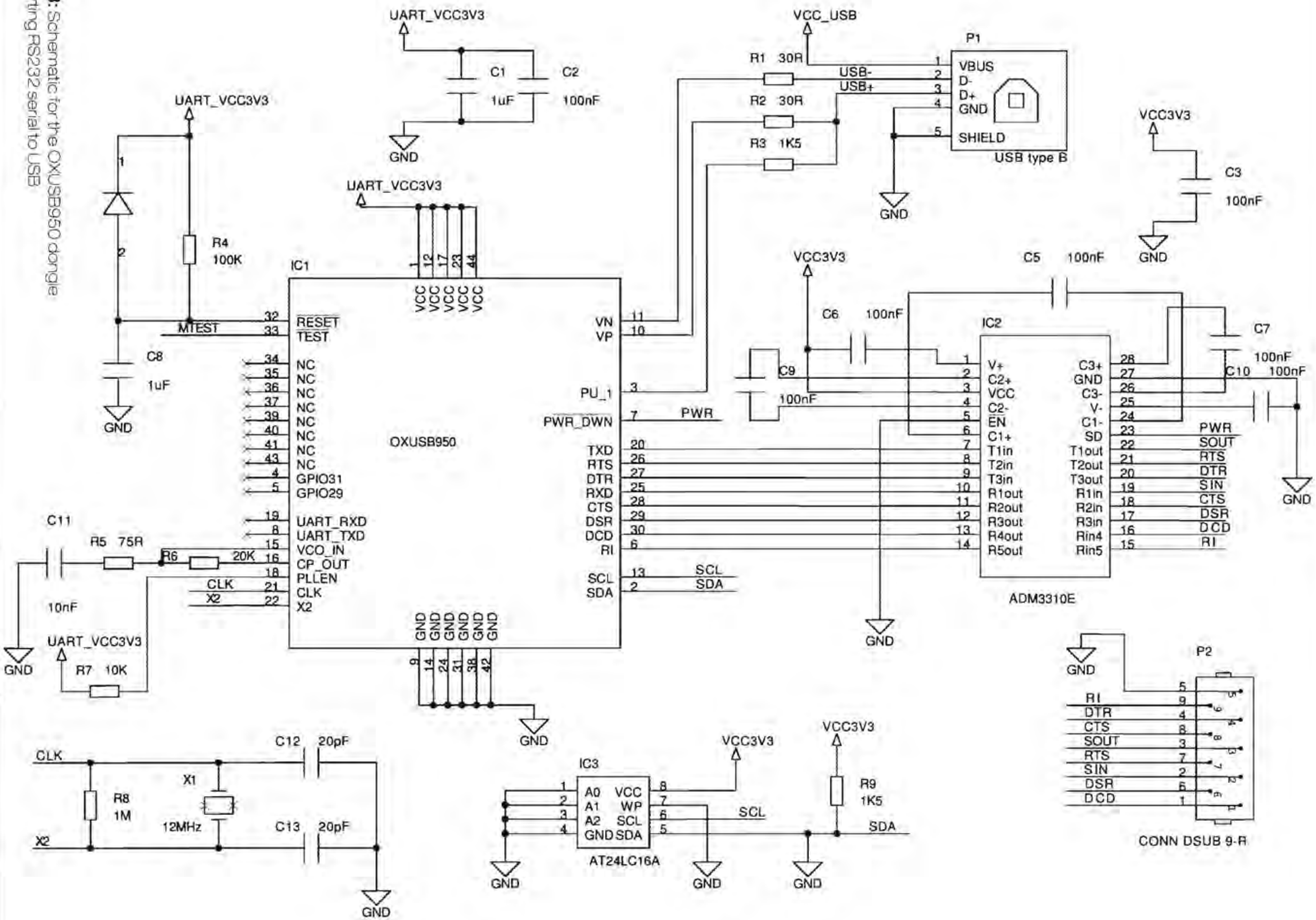


Figure 3: Schematic for the OXUSB950 dongle converting RS232 serial to USB

Let's fight the traffic jams

By Mike Brookes

The Short Range Radio industry is all set for an expansion supernova as unit prices fall and functionality improves. This is going to require careful management by suppliers and regulators to avoid massive 'traffic jams' – or mutual interference.

The prototype examples of this are WiFi and Bluetooth. Both use the universal licence-free 2.4GHz band and both have taken off in a big way, meaning that some organisations have to decide a radio usage policy – Bluetooth or WiFi – to avoid catastrophic mutual interference. Both are looking at the 5GHz spectrum for phase II residency.

And this is only the beginning. Wireless connectivity is set to explode for a whole range of consumer products – there are serious estimates of 1000 million devices in use throughout Europe in five years' time. This is matched by ever-greater numbers of RFID tags, automated metering and asset tracking – to say nothing of ZigBee and building automation.

"Radio Administrations are being urged to examine the deepest entrails of their spectrum allocations and licences to identify bands that could accommodate SRDs physically and politically"

The problem is: how are they all going to work together? They all need radio spectrum in which to work and, historically, this has been in licence-free bands. Given government enthusiasm for 'selling' spectrum, probability for giving 'free' access to new spectrum is questionable.

Nevertheless, the European Commission (EC) is gingerly grasping the nettle in the form of a strategy for the future of Short Range Devices (SRDs).

Radio Administrations and industry have been called together in an ECC (European Communications Committee) project team PT43, to match anticipated market demand to spectrum availability as background to the formulation of a pan-European policy – with a wary eye on the ultimate goal of worldwide compatibility. After all, it would be nice to believe that your SRD-based personal body monitor and systems built into your car work – legally – when you go abroad on holiday.

Radio Administrations are being urged to examine the deepest entrails of their spectrum allocations and licences to identify bands that could accommodate SRDs physically and politically.

Industry has to do its bit – by progressive adoption of spectral sharing techniques (LBT/AFA etc), by providing realistic market predictions, not just global guesses. It cannot expect regulators to cough up jealously guarded spectrum without real justification.

PT43 is in action right now. Focal points for Industry are LPRA, ETSI and EICTA. The PT43 Report and Recommendation is due at the EC in September 2005. This is a once in 10 years opportunity to get your industry sector needs registered as soon as possible.

The LPRA (Low Power Radio Association) is a European trade body that represents manufacturers and users of short range devices (SRDs).

It is active in the production of SRD Radio standards and regulations.

Mike Brookes is LPRA's chairman.

Multifunction voltage-mode filter, employing minimum number of active and passive elements

Voltage-mode filters employing current conveyors (CCs) have been receiving considerable attention nowadays. A great number of studies have been devoted to build multi-input single-output voltage-mode filters employing CCs. However, these filters employ excessive number of active and/or passive elements.

Here we propose a new second-order multifunction voltage-mode filter with three inputs and one output. The proposed filter uses a novel current conveyor called balanced dual input-dual output current conveyor (BDI-DOCC) and minimum number of passive elements (two resistors and two capacitors). The filter can create low-pass, band-pass, high-pass, notch and all-pass responses, depending on the applied input signals.

Also, the presented filter does not require passive element matching. The parameters angular resonance frequency (ω_o) and quality factor (Q) of the filter can be adjusted by changing the values of the resistors orthogonally. On the other hand, only resistors and no capacitors are connected to the X- terminals of the BDI-DOCC, which makes the proposed circuit suitable for operation at higher frequencies. To confirm the theoretical analysis, the filter is simulated using the Spice program.

Using standard notation for port relations of the CCs, the BDI-DOCC can be characterised as in the following matrix form (see below), where α_k and β_k (k=1, 2) are the frequency dependent current and voltage gains of the conveyor respectively, which, ideally, are equal to unity. Current convention is such that all currents flow into the BDI-DOCC. The proposed multifunction filter is shown in **Figure 1**. Routine analysis of that circuit, gives the following output voltage:

From **Equation 2**, it can be seen that:

- ➢ The low-pass response can be realised with $V_1 = V_2 = 0$ and $V_3 = V_{in}$
- ➢ The band-pass response can be realised with $V_1 = V_3 = 0$ and $V_2 = V_{in}$
- ➢ The high-pass response can be realised with $V_2 = V_3 = 0$ and $V_1 = V_{in}$
- ➢ The notch response can be realised with $V_2 = 0$ and $V_1 = V_3 = V_{in}$
- ➢ The all-pass response can be realised with $V_1 = V_3 = V_{in}$ and $V_2 = -V_{in}$.

From this equation, the parameters ω_o and Q of the filter are computed as **Equation 3**.

It should be noted that ω_o and Q are orthogonally controllable. It means that w0 can be adjusted without disturbing the Q by changing $R1$ and $R2$ simultaneously, keeping $R1/R2$ constant. Also, one can tune the parameter Q without disturbing the parameter ω_o by increasing $R1$ and decreasing $R2$ (or decreasing $R1$ and increasing $R2$) simultaneously, keeping $R1R2$ constant.

Sensitivity analysis of the filter gives **Equation 4**. Consequently, all of the passive and active element sensitivities of the filter are low.

Simulations

The BDI-DOCC is constructed using the schematic implementation as depicted in **Figure 2** with DC supply voltages of ±5V and bias voltages of V_{B1}=1V and V_{B2} = -1V. Moreover, the bias currents I_{B1} and I_{B2} are set to 50μA. All MOS transistors are operated in the saturation region. The simulations are performed using Spice program, based on 0.35μm TSMC CMOS technology tabulated in **Table 1**. The dimensions of the MOS transistors used in the BDI-DOCCII implementation are given in **Table 2**.

The filter is simulated using the MOS implementation of the BDI-DOCC given in Figure 2. The frequency domain performance of the proposed filter is tested. The following settings have been selected to obtain the low-pass, band-pass and high-pass responses with pole resonance frequency of f_0 = 318.3kHz and quality factor of Q = 1: $R_1 = R_2$ = 1kΩ and $C_1 = C_2$ = 0.5nF. The frequency responses of the filter are shown in **Figure 3**. It can be seen that the simulation and theoretical results are in good agreement.

Also, the large signal behaviour of the circuit in Figure 1 is tested by investigating the dependence of the output harmonic distortion of the band-pass response on the amplitude of the sinusoidal input signal. The obtained results are given in **Table 3**. As it can be seen from Table 3, the total harmonic distortion (THD) of the filter for a sinusoidal input voltage with peak value of 100mV at 318.3kHz (resonance frequency) is obtained as 2.59%. The total power dissipation of the filter is found to be 25.4mW.

Erkan Yuce, Shahram Minaei, Levent Oner and Oguzhan Cicekoglu
Yuce, Oner and Cicekoglu are from Bogazici University, Instanbul, Turkey. Minaei is from Dogus University, Istanbul, Turkey

Filter matrix

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_{Z-} \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_1 & 0 \\ 0 & 0 & 0 & \beta_2 \\ -\alpha_1 & 0 & 0 & 0 \\ 0 & \alpha_2 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X-} \\ I_{X+} \\ V_{Y1} \\ V_{Y2} \end{bmatrix}$$

Equation 2

$$V_{out} = \frac{s^2 C_1 C_2 R_1 R_2 V_1 + s C_2 R_2 \beta_1 V_2 + \alpha_1 \beta_1 V_3}{s^2 C_1 C_2 R_1 R_2 + s C_2 R_2 + \alpha_1 \beta_1 \beta_2}$$

Equation 3

$$\omega_0 = \sqrt{\frac{\alpha_1 \beta_1 \beta_2}{C_1 C_2 R_1 R_2}} \qquad Q = \sqrt{\frac{C_1 R_1 \alpha_1 \beta_1 \beta_2}{C_2 R_2}}$$

Equation 4

$$S^{\omega_o}_{C_1,\ C_2;\ R_1,\ R_2} = -\frac{1}{2} \qquad S^{\omega_o}_{\alpha_1,\ \beta_1,\ \beta_2} = \frac{1}{2} \qquad S^{Q}_{C_1,\ R_1} = -S^{Q}_{C_2,\ R_2} = \frac{1}{2} \qquad S^{Q}_{\alpha_1,\ \beta_1,\ \beta_2} = \frac{1}{2}$$

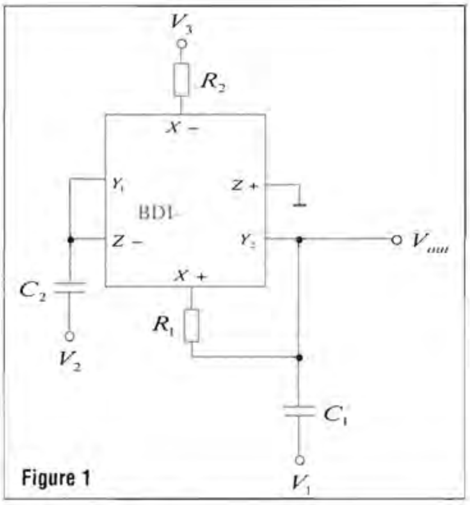


Figure 1

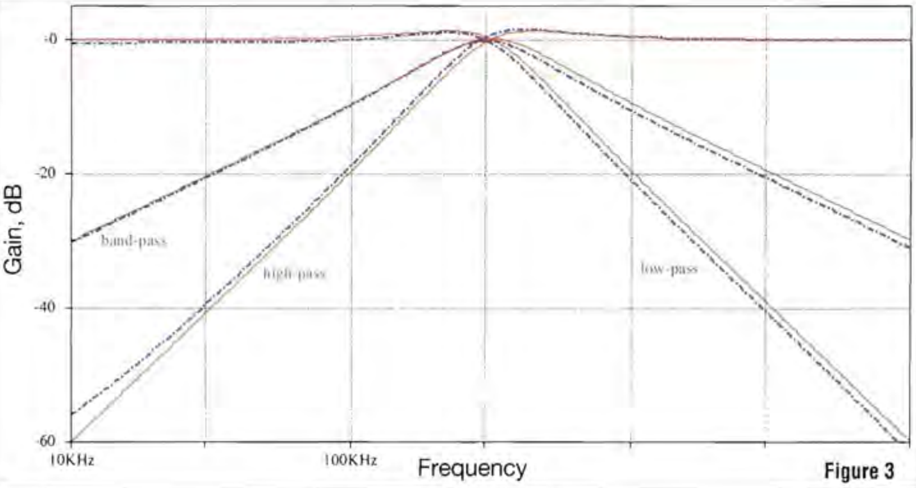


Figure 3

Figure 2

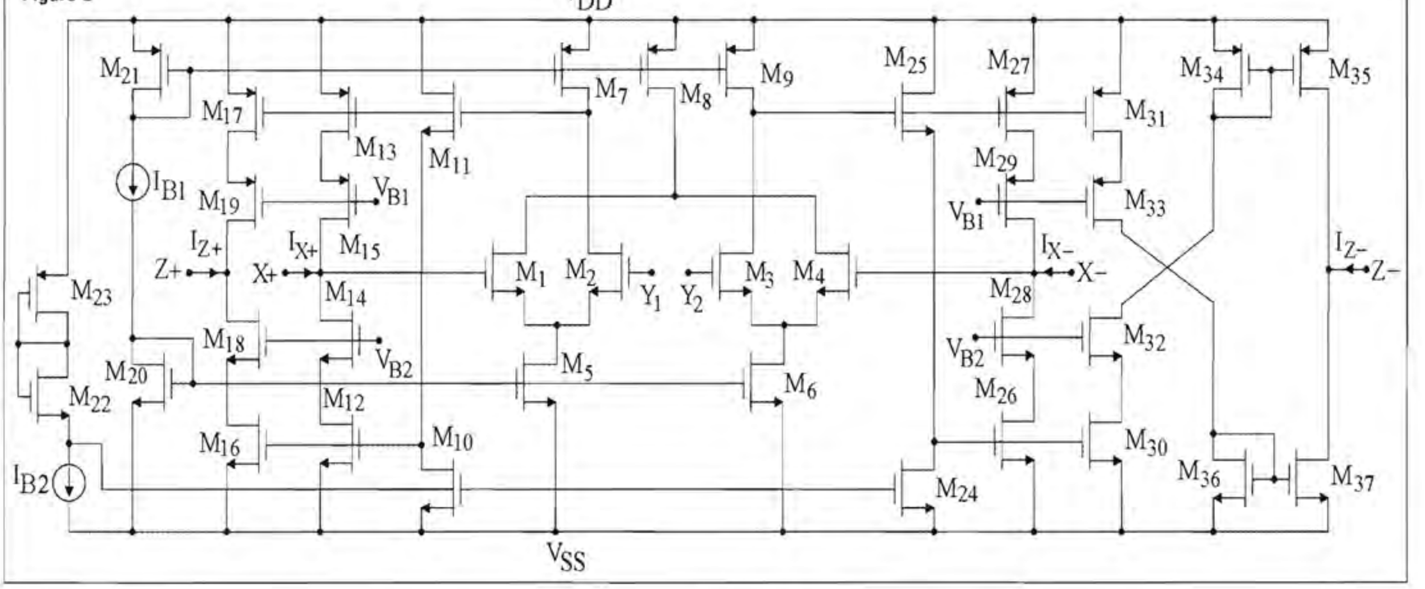


Table 1: Parameters of the CMOS transistors used in Spice simulations

0.35μm TSMC CMOS parameters

.MODEL CMOSN NMOS (LEVEL = 3

+ TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.5827871
+ PHI = 0.7 VTO = 0.5445549 DELTA = 0
+ UO = 436.256147 ETA = 0 THETA = 0.1749684
+ KN = 2.055786E-4 VMAX = 8.309444E4 KAPPA = 0.2574081
+ RSH = 0.0559398 NFS = 1E12 TPG = 1
+ XJ = 3E-7 LD = 3.162278E-11 WD = 7.046724E-8
+ CGDO = 2.82E-10 CGSO = 2.82E-10 CGBO = 1E-10
+ CJ = 1E-3 PB = 0.9758533 MJ = 0.3448504
+ CJSW = 3.777852E-10 MJSW = 0.3508721).

.MODEL CMOSP PMOS (LEVEL = 3

+ TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.4083894
+ PHI = 0.7 VTO = -0.7140674 DELTA = 0
+ UO = 212.2319801 ETA = 9.999762E-4 THETA = 0.2020774
+ KP = 6.733755E-5 VMAX = 1.181551E5 KAPPA = 1.5
+ RSH = 30.0712458 NFS = 1E12 TPG = -1
+ XJ = 2E-7 LD = 5.000001E-13 WD = 1.249872E-7
+ CGDO = 3.09E-10 CGSO = 3.09E-10 CGBO = 1E-10
+ CJ = 1.419508E-3 PB = 0.8152753 MJ = 0.5
+ CJSW = 4.813504E-10 MJSW = 0.5)

Table 2: Dimensions of the MOS transistors

PMOS Transistors	*W (μm)/L(μm)*
M_7-M_9, M_{13}, M_{15}, M_{17}, M_{19}, M_{27}, M_{29}, M_{31}, M_{33}- M_{35}	1.4/0.35
M_{21}	28/0.35
M_{23}	2.8/0.35
NMOS Transistors	*W (μm)/L(μm)*
M_1-M_6, M_{10}-M_{12}, M_{14}, M_{16}, M_{18}, M_{24}-M_{26}, M_{28}, M_{30}, M_{32}, M_{36}, M_{37}	0.7/0.35
M_{20}	14/0.35
M_{22}	1.4/0.35

Table 3: Dependence of output harmonic distortion of the band-pass response on input signal amplitude

Amplitude (mV)	*Total Harmonic Distortion (%)*
1	3.82
5	3.42
10	3.47
20	3.50
40	3.02
60	3.69
80	3.06
100	2.59
150	5.40
200	9.47

Novel approach to voltage-controlled astable multivibrator

An astable multivibrator is a rectangular wave-generating circuit. The astable multivibrator makes successive transitions from one quasi-state to another after a predetermined time interval, without the aid of an external triggering signal. The periodic time depends upon circuit time constants and parameters. Thus, it is just an oscillator, as it does not need any external pulse for its operation. Since its output oscillates in between 'on' and 'off' states freely, it is called free-running multivibrator. It is also named as square-wave generator based upon its application.

An astable multivibrator is used in a variety of electronic subjects. It may also be used as a synchronised oscillator and for driving sweep generators. However, conventional astable multi vibrators, realised using a 555 timer, suffer from various limitations, such as, frequency of oscillations cannot be controlled without changing component values, first cycle timing errors, non-realisation of 50% duty cycle and noise problems.

In the recent past, many circuits for controlling the output frequency with the voltage have been proposed, but suffer from limitation that the change in the output frequency is the non-linear function of the input voltage. In these circuits, the voltage is used to control the charging of capacitor, which is exponential in nature. However, in real-time applications, a linear control of voltage-to-frequency is highly desirable. Fortuitously, a number of passive and active components in the astable multivibrator circuit can eliminate most of these problems.

Figure 1 shows a voltage-controlled astable multivibrator.

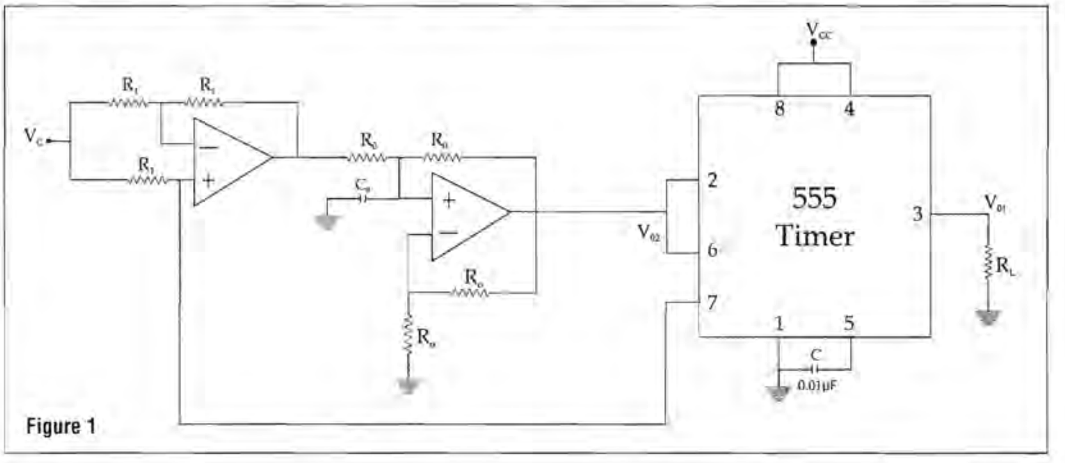


Figure 1

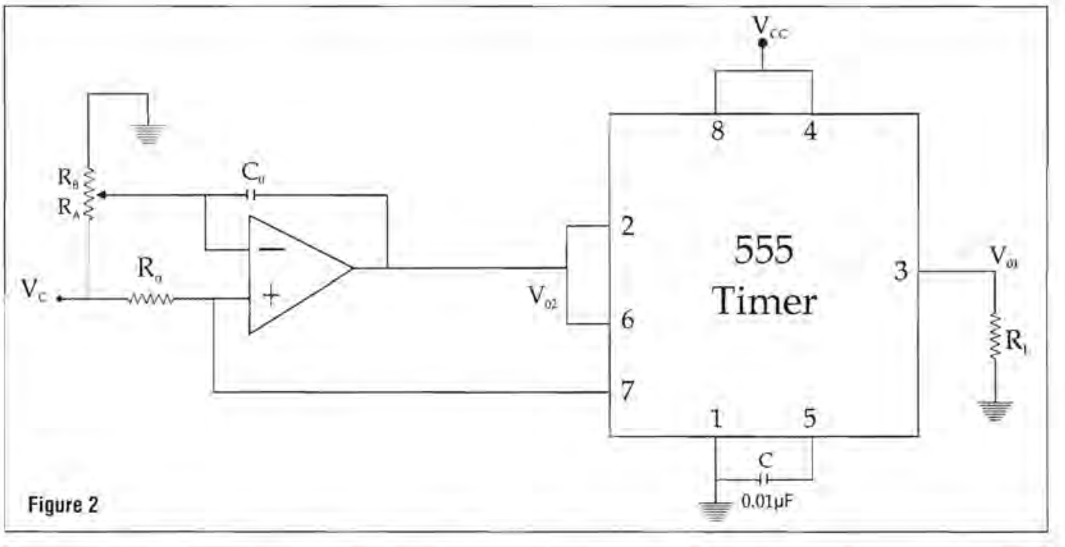


Figure 2

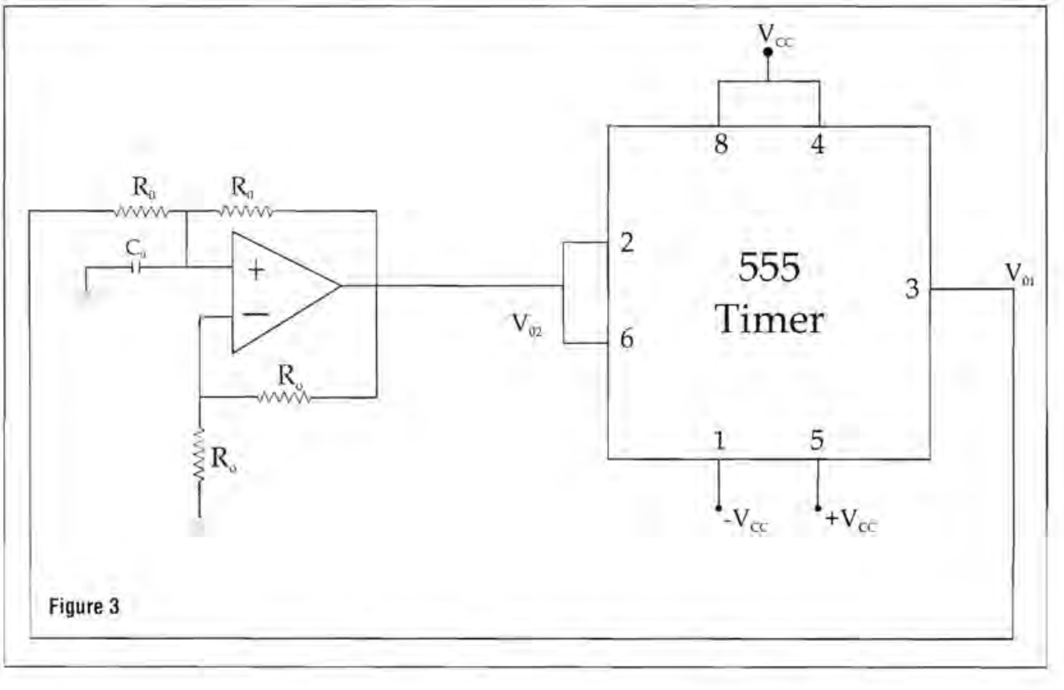
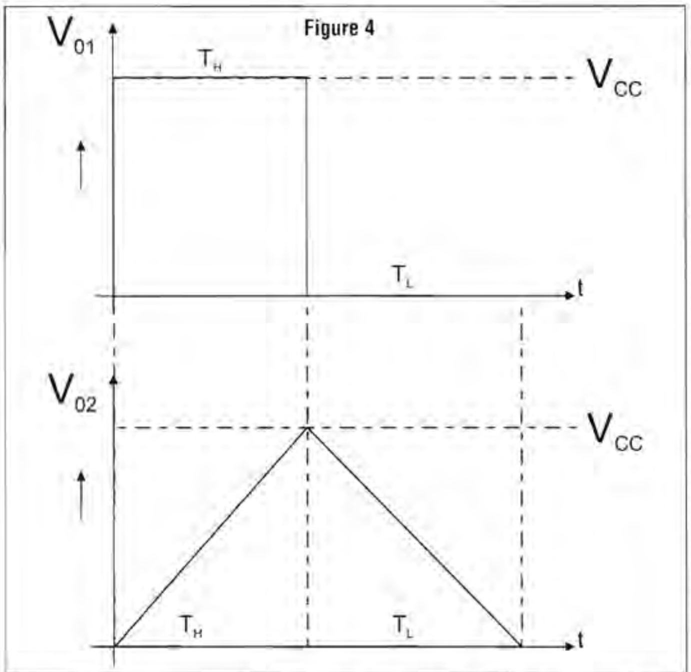


Figure 3

Figure 4



The circuit comprises two operational amplifiers, a 555 timer IC, resistors and capacitors. An external voltage V_C can be used to control the frequency of generation of square waves' 50% duty cycle. Hence, the circuit is that of a linear voltage-controlled square wave oscillator. A complete analysis of the circuit proves frequency to be directly proportional to V_C and inversely proportional to R_0, C_0 and V_{CC}. An appropriate selection of V_C, R_0, and C_0 can be used to obtain a frequency variation in desired range.

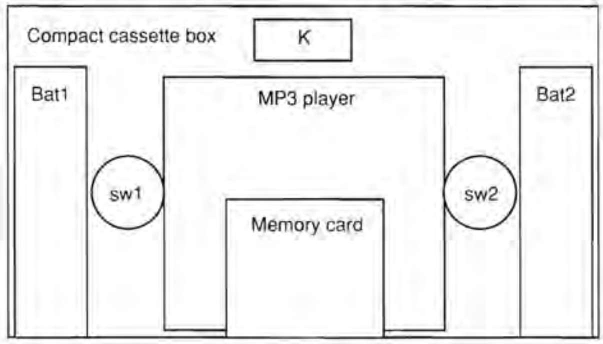
Figure 2 is a modification of the previous circuit – it uses a lesser number of components. In addition to frequency being controlled by external voltage, the duty cycle of the output rectangular wave can also be varied using a potentiometer. The duty cycle in this case is the ratio of R_A and R_B. The frequency, as before, is directly proportional to V_C.

Figure 3 is another modification to the circuit in Figure 1. The advantage of this circuit is that it is free from first cycle timing error. But the drawback is, neither the frequency nor the duty cycle of the output square-wave can be controlled. One advantage that is common to all the three circuits is that a triangular wave can also be obtained at the shorted pins 2 and 6 of the 555 timer. The general output waveforms are shown in **Figure 4**. The 555 timer as a voltage-controlled oscillator circuit is sometimes called a voltage-to-frequency converter as the output frequency can be changed by changing the input voltage.

Although the 555 timer has been used in a variety of unique applications, it is very hard on power supply lines, requiring quite a bit of current and injecting many noise transients. This noise will often be coupled into adjacent ICs, falsely triggering them. The 7555 is a CMOS version of the 555. Its quiescent current requirements are considerably lower than that of the 555, and the 7555 does not contaminate the power supply lines. It is pin-compatible with 555. So this CMOS version of 555 should be the first choice when a 555 timer IC is to be used.

Jivesh Govil
New Delhi, India

Almost universal MP3 player



By using a compact cassette (CC) box and a standard MP3 player, we can build an MP3 to be used on any CC player.

Two Hall Effect cells, combined with rotating magnetic discs, are used as SW1 SW2 for wind/rewind functions. A logic circuit can discriminate SW2 between winding and playing. Bat1 + Bat2 supply the player and K is a standard stereo head that works as the audio coupling to the CC player.

Rui Figueiredo
Lisboa, Portugal

An improved LED driver

Recently, many LED drivers using single battery (1.5V) have received great attention. The idea is to obtain high voltage generator from low power supply by the nature of both, the inductor and the oscillator.

Figure 1 is one example where the oscillator is an LC tank circuit with negative resistance, inductor and capacitor. Three transistors (Q1, Q2 and Q3) and two resistors of Figure 1 create this negative resistance described with the following equation:

$$I \approx \beta \frac{(Vdd - Vbe)}{R_1} + \beta \frac{Vbe}{R_2} - \frac{\beta}{R_2} V$$

Assume all transistors have the same gain

$$(h_{fe} = \beta)$$

and the leakage current of the transistor is neglected.

We should choose the value of the negative resistance, which is determined by the bias resistors (R1&R2) in Figure 1, to cancel the positive residual impedance and create an LC resonator.

Figure 2 is an improved LED driver. The inductor in Figure 2 is set in printed circuit bread, where there is a stray capacitance of about 3-10pF. Therefore, there is no need for an actual capacitor in Figure 2. Then, there is a high oscillating voltage (Vpk) at the terminal of the inductor, as well as the collector of the transistor.

Note that the anode of the LED is connected to the positive terminal of the power supply, and its cathode is connected to the terminal of the Q3's collector as well as the inductor. The induced voltage is Vpk at the inductor. Therefore, across the LED, there will be the combination of the voltages

$$(|Vdd| + |Vpk|)$$

that will turn it on with a 1V power supply (Vdd).

It is clear that there're less than two components and much more current is driving the combination of positive and negative voltage. The intensity of the white LED driver in Figure 2 is 20% higher than any LED driver, without the combination of the positive voltage and negative voltage at the same power supply.

This circuit can also be widely used in many applications at low power supply such as a laser diode, for example.

Tai-Shan Liao
National Applied Research Laboratories - Precision Instrument Development Center
Taiwan

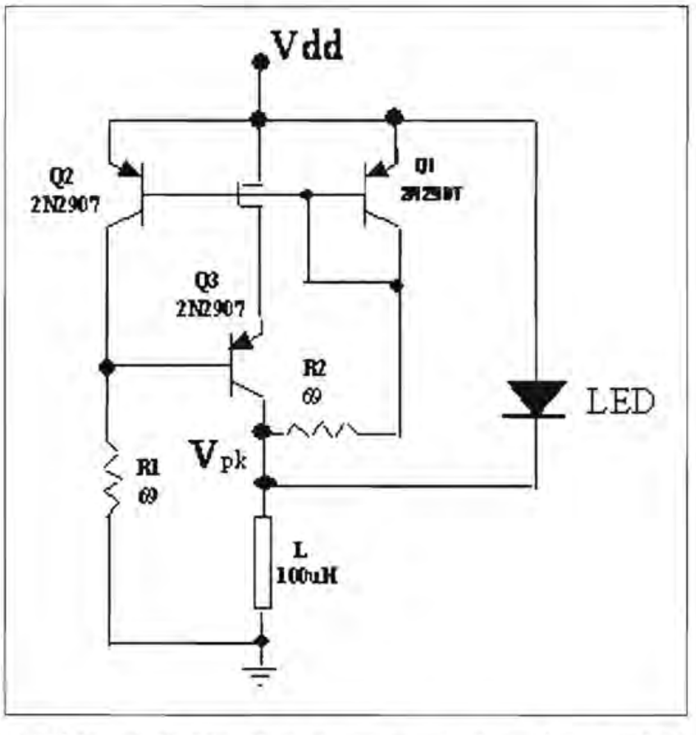


Figure1: Simplified white LED driver using supply voltage of less than 1.2V

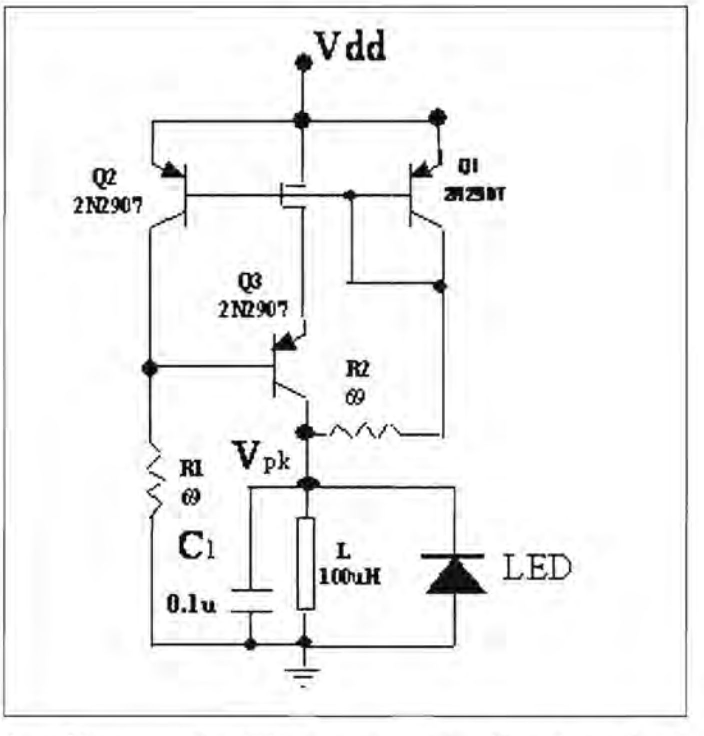


Figure 2: Improved white LED driver using supply voltage of less than 1V

Send new circuit ideas to:

The Editor, Nexus Media Communications, Media House, Azalea Drive, Swanley, Kent BR8 8HU

or email to: **ewcircuit@highburybiz.com**

For clocks and EM radiation

In reply to two letters in the January 2005 copy of Electronics World – 'Pendulum Conundrum' on p53 and 'Unmentionable hazard' on p51.

My father built an electric pendulum grandfather clock in the 1940s. The mechanism was purely mechanical i.e. hand filed cogs. The pendulum was driven by an electromagnet (two coils approximately three inches long by one inch in diameter) with a switch assembly about half way up the pendulum rod (using a piece of old spring as a 'hinge'). The switch was on one side of the swing (of the pendulum) and made contact only on the inbound stroke, and operated for a short time. It was powered by two PMG No 6 cells and these lasted many years (I only remember them being replaced once). The original 'design' probably came from Wireless World or Popular Mechanics.

As for electromagnetic radiation, this subject is still bouncing around. During the early 1960s, I was asked to find information on 'radio and light' radiation. I had access to all libraries and 'establishments' and a lot of unpublished data from all around the world, including Russia. There appears to be many spot frequencies and small bands, and power levels that have been extensively and accidentally explored by many people. My brief was to start at Rugby (16kHz) and stop at the then maximum frequency of 2GHz, and from the turn of the century (1900) to then in 1964. The symptoms ranged from headaches, body warming, to mood/character changes: these must have been obvious as the comments were made at times incidental to the main script. All this information was whisked away rather abruptly. All I am saying is, "Be careful, the jury is still out". If there are no adverse results after five generations (order of 150 years), only then can you say there is no effect. There is much more study needed to be done by responsible people.

John Ingram
South Australia

Clear statements

Ian Hickman (EW October 2004, p38) discusses where the electric charge that appears on the more negative conductor of a transmission line comes from. Ray G. Lee's comment (EW April 2005 on p49) that we have a model, not a theory, is irrelevant.

A model has to be clearly stated. If experts contradict each other, then we have two models, not one. This should be made clear to students, who will be examined on models as well as on theories.

Jane Lynx
Walsall
UK

Battling it out with Eircom

I hope you can help a struggling novice with the following problem.

After a six-months' running battle, I finally got the Eircom technicians to come and install the Internet connection to my mini-tower PC that I'd been waiting for. It turned out to be an Airspan Type 42 S.T. Service Interface Unit, connected to a small dish on an outside wall mounting and also running through a mains CPU. I then almost immediately discovered that the 56k external modem I'd bought in anticipation months before wouldn't work at all with this system.

Acting on advice from one of the many Eircom contact numbers, I then bought a LAN card and RJ-45 cable, installed the card and then realised that the RJ-45 socket on the Airspan machine was empty and closed with a removable plate. I have two other occupied sockets; the one labelled 'Home Network' is active and the one marked with a phone icon is not, but both of them are for ordinary phone plugs anyway and so not much use to me.

Can you please give me some pointers as to what parts I need to install to make the RJ-45 socket active (obviously apart from the socket itself!), good places to order them from (could be more than one of those listed in magazines or elsewhere) and, possibly even, how to install them when they arrive?

I hope the page of details about the Airspan machine's mainboard will be of some use:

Airpspan Networks packet S.T. card – 303-1110-500 rev08.4, S00031800T0348D, 303-1110-902 Rev3.

Empty chip space for 10BaseT connection from front to back, inside the board.

P29. Square. Two round solder spots and one round connecting hole on each side; these spots are presumably just for fixing RJ-45 socket. Row of one square and three round solder spots, row of four round above.

U5. Oblong. Row of eight oblong solder spots at the top and bottom. Spaces for pins of some sort at left-hand two spots both rows, pin-space centre right.

Y6. Square and small with square solder spot at each corner. Space for pin at top left, bottom right. Jutting into:

Y4. Oblong. At its right, long oblong solder spot top and bottom center. Eight pin spaces inside, cluster of 13 at top left-hand corner.

U30. Square. Row of line solder spots each side, too many to distinguish.

Cluster of five pin-spaces in centre, two outside/six inside bottom edge, five inside and outside left edge, six inside/eight outside right edge (I think), six inside/outside top edge.

C282 and C517. Small oblong, filled by two oblong solder spots each. Four pin spaces in various places.

L87. Small and oblong. Oblong solder spot on each side, row of six pin-spaces left of right solder, one pin-space outside the bottom left-corner.

J2. Long and narrow, 32 large pin-spaces. Smaller pin-space at bottom-left, another low on the left side, cluster of three higher up, two above top left edge, cluster of five low on the right.

Details given on the bottom of the machine's case are: V2, config. No. 616-0202-010 Rev; Hardware part no. 503-0025-102 Rev; Mainboard part no. 303-110-A02 Rev B.

POV2 hardware platform, with both voice ports enabled. Preloaded with software on 10/12/2003, main bank code: 1.7.15.0205, back-up bank code: 2.7.11.020.

MAC address:
00.01.aa.00.90.39
Serial no. S00031800T0348D

Just for the sake of completeness, my operating system is a version of Debian GNU/Linux.

John Verrill
Bantry
Ireland

Please send your letters to:

"Electronics World" Nexus Media Communications, Media House, Azalea Drive, Swanley, Kent BR8 8HU

ewletters@highburybiz.com

MEMprogL arrives

Slovakia-based device programming firm Elnec has introduced a new, simple and low cost programmer for memory chips. MEMprogL is the next member of Windows 95/98/ME/NT/2000/XP based Elnec specialised programmers. It is built to meet the demands of development labs and field engineers for a specialised low-cost memory programmer. MEMprogL supports memory types up to 32 pins - EPROM, EEPROM, NVRAM, Flash EPROM and serial EEROM, including low voltage types. In addition, MEMprogL also doubles up as a static RAM tester.

MEMprogL interfaces with the IBM PC compatible, portable or desktop personal computers through any parallel (printer) port. Performance, dimensions and speed of MEMprogL can be used mainly in the maintenance.

Important feature is the extensive MEMprog's device library which covers almost 6000 devices. This library can be downloaded free from the manufacturer's home page.

www.elnec.com

1812 common mode chokes operate to 10A

Steward's new CM1812x330R monolithic surface mount common mode chokes are designed for power and data line EMI filtering where high current, small size or high frequency performance is required. This new family of compact ferrite parts includes versions rated at 5A and 10A. All of the family members feature very low DC resistance to minimise signal distortion and low common mode impedance of 100MHz.

The devices are smaller, lighter and less susceptible to vibration than older-style wire-wound chokes, making them ideal for use in harsh environments and portable equipment. All of them are available in lead-free. RoHS-compliant variants exhibit DC resistance of 3W and 5W respectively.

The new series is suitable for a variety of applications, including EMI suppression on the DC power trances of PCBs, especially in applications greater than 3A.

High-speed I/O circuitry such as network and storage subsystems also need such common-mode EMI suppression, as do USB power lines, PCMCIA products, disk drives and others.

www.steward.com

WiMax gets its own antenna range

European Antennas has designed the Vector series of 20 sector and omni antennas specifically for WiMax applications.

The range meets the WiMax Forum's conformance and interoperability requirements.

The vector series can also be used for Fixed Radio Access (FRAU) and broadband networks. It is easy to install and features a wide range of operating bands (3.30-3.80GHz and 4.9GHz - 5.9GHz), effectively reducing the need to maintain a large variety of narrow band antennas.

Vector base station sector antennas are available with 600, 900, 1200 and 1800 azimuth beam-widths and feature built-in electrical down-tilt to benefit installation and operation.

While sector antennas provide up to 19dBi gain, European Antennas also offer 8dBi and 11dBi gain omni antennas in both, the 3.5GHz and 5.5GHz bands.

www.european-antennas.co.uk

Pressure sensor with media compatibility

Sensortechnics's new piezoresistive 40PC series from Honeywell offers gage pressure measurement in a wide pressure range from 67mbar to 35bar and is suitable for use in extreme temperature conditions.

The sensors feature 0.5-4.5V amplified output signal, providing a direct interface to an A/D input of a controller. The fully calibrated and temperature compensated sensor is very robust, built in a miniature 6-pin DIP package and is covering a wide range of temperature extremes from -45°C to 125°C. Additionally, the 40PC series is compatible with a broad array of gaseous and liquid media, from dry air to engine fuel and oil.

Typical applications include level control, environmental and medical applications and industrial and analytical instrumentation.

www.sensortechnics.com

Module with metric connectors

The latest addition to Harting's HM range of hard metric connectors, in accordance with the IEC 61076-4-101 standard, is the Har-bus HM combined module. This new product integrates different HM female connectors in a single unit and allows any combination of HM types A, B, AB and C to be assembled up to a maximum length of 6U.

The combined module is particularly suited to use on boards such as the CompactPCI 6U Eurocard, where it replaces five separate connectors on the daughtercard or three connectors on the rear I/O board. As a result, it will greatly speed manufacturing operations by reducing the number of press-in operations from five to one.

In addition to the resulting benefits in terms of reduction in manufacturing costs, it also offers additional process optimisation in the logistics area because only one part-number is involved.

The connector consists of five signal contact rows and provides a maximum of 535 contacts. It is available in both shielded and unshielded versions and is fitted with press-in contacts.

www.harting.com

KTL now tests smartcards

KTL has added an extra capability to its portfolio of services – the testing of interoperability between smartcards and readers to EMV Level 1 standard as well as the full range of test scenarios for EMV Level 2.

"Level 1 is targeted at applications such as set-top boxes, security and vending machines," said Karim Sharf, KTL's telecoms group manager. "It defines physical size, electrical performance, chip location etc. Level 2 is targeted more at financial transactions – such as EPOS."

In addition to this new service, KTL provides complete test solutions, making the firm's lab a one stop shop, says Sharf.

EMV is the globally recognised standard for JCB, MasterCard and Visa. The joint founders have developed the specification to define a set of requirements for interoperability between chip cards and terminals on a global basis, irrespective of the manufacturer, financial institution or geographical region.

www.ktl.com

Solving power issues with Dialog Plus

Riello Galatrek's new Dialog Plus is an on-line uninterruptible power supply (UPS), specifically designed to solve the power protection problems of Voice over IP (VoIP) telephony and Power over Ethernet (PoE) technologies. Both have capabilities that power disruptions can tamper with.

PoE is a way of providing electrical power to network ports along existing category 5 10BaseT and 100BaseT-TX Ethernet cabling. From the ports compatible equipment, such as PoE-compatible telephone handsets, cameras and security devices, can be powered, managed and controlled. VoIP telephony is a way of providing unified messaging and communication over remote IP addresses with greater cost-savings and efficiencies over traditional telephony.

The new Dialog Plus is available in 700VA to 3000VA power modules and both are floor standing and 19" rack mount formats to offer the maximum number of installation options. Each UPS has a number of output sockets from which uninterruptible power can be drawn continuously. To provide failure protection, Dialog Plus is available with a standard internal battery that can typically run for 13 minutes at full load.

The range starts from £499 plus delivery and VAT.

www.riello-ups.co.uk

New member joins the thermal team

DED Limited's Axiohm selection of thermal printers – the A600 series – has just received a new addition in the A632 system. Being made with vehicle space constraints in mind and a power supply of 12VDC, this device has already been awarded the 'e' approval for in-vehicle use. The device is only 108x147x72mm in size, has a 12VDC battery, 9-12VDC converter, supports the Windows drivers for 98/2000/XP and Pocket PC, and it can be used with a PDA as well.

The system's printing time is 55mm/s, supporting paper width of 58mm and offering battery life of up to 170 hours. The system weighs some 330 grams and it offers an RS232 interface and a choice of 24 or 40 column print width.

www.ded.co.uk

InstaPin offers low cost SoC testing

Agilent Technologies announced the InstaPin test programme for the Agilent 93000 system-on-a-chip (SOC) testers. InstaPin offers per-pin licenses that can be shared across pins of testers, testers on a test floor and production facilities anywhere in the world. InstaPin promises to deliver lower costs and yet a highly evolved testing for SOC devices. "InstaPin is a radical approach – nobody has thought of this before in the industry. It builds on the pin-scale technology, it is done with a high level of granularity which will also keep test costs in check," said Cristof Baschang, Agilent product manager.

The InstaPin test programme figures out automatically how many pins need testing and where, and asks for those licenses to run the test. Each pin of the 93000 pin scale digital cards can be software-scaled over a wide memory depth and speed range, allowing test systems to be configured to match device requirements, pin by pin.

www.agilent.com

VME64x bus mechanical switching connector

Harting has just launched the new Har-bus 64S, which is a passive mechanical switching connector for use in VME64x bus systems.

The 5-row, 160-way connector offers automatic daisy-chain functionality, with the mechanical switching elements guaranteeing the reliable switching of the daisy chain without contact losses.

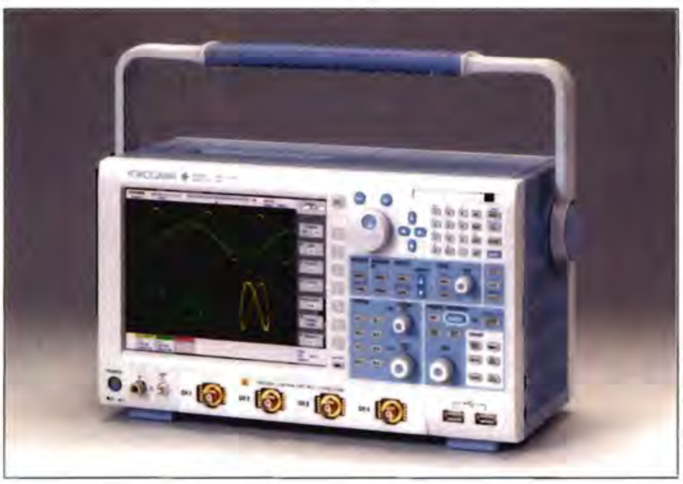
The switching elements close the daisy chain when no daughter card is inserted, eliminating the need for active components or jumpers on VME64x backplanes. Five pairs of switching contacts – in positions a21-a22, b4-b5, b6-b7, b8-b9 and b10-b11 – short-circuit the VME interrupt lines when the daughter card is removed, preserving the integrity of the entire system.

The new connector is an addition to Harting's Har-bus connector range and is fully compatible with Har-bus 64 daughter card connectors. It also offers full backward compatibility with existing standard VME systems based on 3-row Type C daughter card connectors on a 2.54mm in according to DIN 41612.

The Har-bus 64S connector uses the same PCB layout and hole configuration as existing Har-bus 64 connectors, and is pressed in with the same 'flat rock' press-in tools.

www.harting.com

Compact digital oscilloscope



The new SignalXplorer DL900 series of digital oscilloscopes from Yokogawa combines high-performance waveform display and analysis functions with a very compact and lightweight design.

The instrument features maximum frequency bandwidth of 1.5GHz, maximum sampling rate of 10GS/s and maximum memory length of 6.25MW.

It's a four-channel system that also features an enhanced waveform accumulation function for the acquisition and display of up to 450 million digitised points every second.

In addition, the oscilloscope offers a reduced power consumption, based on an AD conversion section where cascade-type 2.5GS/s 8-bit ADCs are run in parallel.

As for the signal-processing section, a proprietary advanced data stream engine (ADSE) has been implemented in a 0.13μm CMOS process, with the memory being integrated into the chip itself.

This section generates display information from the A/D-converted data and carries out the processing for waveform and parameter calculations.

The DL9000 measures 350x200x178mm and weighs 6.5kg. It incorporates an 8.4-inch LCD screen. The series consists of four instruments. Prices start from ¤ 10,995.

www.yokogawa.com/eu

Allegro sensor for automotive applications

The ATS625 from Allegro MicroSystems Europe is a zero-speed differential gear-tooth sensor that is optimised for automotive engine control, especially crank speed and position sensing.

By means of differential threshold detection and algorithms such as automatic gain control and automatic offset adjustment, the ATS625 offers very high levels of relative edge accuracy and switching, independently of the air gap. The combination of low jitter and edge repeatability is ideally suited to targets that have signature tooth or valley regions, which are common to engineering crank-speed sensing.

To meet the demanding environmental requirements of engine-control applications, the ATS625 also has enhanced EMC protection to reduce the effects of electrical transients on the input and output of the device.

An on-chip voltage regulator permits operation over a wide supply voltage range, while undervoltage lockout eliminates false switching during undervoltage conditions.

www.allegromicro.com

Adaptaflex's price list expands

Adaptaflex has just made available its latest price list of flexible conduit systems and accessories. The price list – Issue 6 – includes the company's latest product offerings in ranges of non-metallic and metallic flexible conduit systems, but also it covers the complete Elkay range of wiring accessories, terminals, connectors, cable glands and energy management systems.

Also included are the newly introduced pipe protection conduit, Big bore metric Adaptolok, underground service warning tape, safety site fencing, terminal strips, cable jackets, retrofit conduit and smooth inner and outer PVC conduit systems. These are in addition to the range of six Contractor Packs, including the new time-saving Installer Packs.

The products are cross-referenced throughout the Adaptaflex and Elkay catalogues and new products leaflet.

Copies of the new price list are available direct from Adaptaflex on telephone 01675 468222 or by email at sales@adaptaflex.co.uk

www.adaptaflex.com

New set of integrated power modules

International Rectifier (IR) has expanded its iMotion series of integrated power modules (IPMs) with parameters of 600V, 16A and 20A. They are expected to simplify the design of compact, high-performance variable-speed motion control power stages for air conditioners and commercial freezer, for example.

Designed specifically for 85V to 253V AC variable speed motor drives for energy efficient appliances, these new IPMs integrate IR's proprietary high voltage integrated circuit (HVIC) with a three-phase inverter power stage. The 16A device addresses the 750W to 1.2kW power range, while the 20A devices can accommodate 750W to 2.2kW. all of the new IPMs are packaged in efficient, single in-line packages (SIP) with improved thermal characteristics.

IR's iMotion integrated design platform consists of a development system, mixed-signal analogue chipset and power stage, which, when co-designed together, simplify motion control designs and bring energy-efficient, cost-effective solutions to market faster.

www.irf.com

Nepcon debut for Adaptsys BP 4710

Adaptsys Limited will use the Nepcon (Stand U401) show as a vehicle to showcase the new programming, marking and handling solutions system, the BP 4710. In addition, among its other products, it will also exhibit the Adaptsys LCMP Laser Component Marking System, not seen in the UK before.

The 4710 Automated Programming System from BP Micro Systems is claimed to be one of the most advanced around. Designed specifically for the latest high-density devices and their longer programming times, it is one of the fastest for programming Flash, while still offering the versatility to program FPGAs, antifuse FPGA, PLDs and microcontrollers, including MCUs with embedded Flash memory. It will handle all package types from DIP to µBGA.

The BP 4710 system provides the capability of programming devices with densities of up to 4Gbits. It incorporates the globally accepted high-speed USB 2.0 standard bus for communications and, by combining the industry's fastest universal programming technology with BP Micro's FX4 socket modules, the system can program up to 44 devices at the same time, resulting in four times the throughput. The fast programming times (up to 0.24s/Mbit) and exceptional throughput (up to 1400 devices per hour) translates to a very low programming cost per device.

www.adaptsys.com

LIF crimp terminal receptacles

Wieland Electric's Stocko range has gained a new range of low insertion force (LIF) – LIF 6.3 – receptacles for the crimp terminals. As well as increasing productivity through faster assembly, these crimp terminals reduce the risk of repetitive strain injury in users.

This range requires only 40% of the insertion force of conventional terminals and provides the same reliability and integrity of connection, with the same withdrawal force. The integrity of the terminals has been fully tested and verified in live tests under a range of conditions.

The Wieland Electric's Stocko range encompases a wide choise of wire sizes.

www.wieland-electric.com

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NEWNES GUIDE TO RADIO AND COMMUNICATIONS TECHNOLOGY

Ian Poole

This is a guide to the technology and applications of modern radio and communications equipment. The author's approach provides a useful foundation for college students and technicians seeking an update on the latest technology.

Jul 2003 ▲ 352 pages ▲ Index ▲ PB
Published in UK

Code 0-7506-5612-3 **£16.99**

DICTIONARY OF VIDEO AND TELEVISION TECHNOLOGY

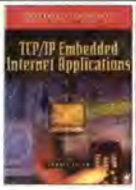
Jack Tsatsoulin

This work provides comprehensive and contemporary information on the essential concepts and terms in video and television, including coverage of test and measurement procedures. The CD accompanying the text includes an electronic version of the book.

Sept 2002 ▲ 365 pages & CD-Rom
Published in UK

Code 1-878707-99-X **£29.99**

TCP/IP EMBEDDED INTERNET APPLICATIONS



Edward Insam

This text highlights an engineer's approach to Internet protocols and applications, reducing R&D time for engineers. The book aims to be the main design guide for the cutting edge of Internet-enabled electronic products and systems.

Aug 2003 ▲ 384 pages ▲ Index ▲ Appendix
PB ▲ Published in UK

Code 0-7506-5735-9 **£32.50**

ELECTRONIC CLASSICS: COLLECTING, RESTORATION AND REPAIR

Andrew Emmerson

This text encompasses all aspects of buying, collecting, restoring, repairing, sourcing parts, professional services, clubs and societies. The first part covers technical aspects of restoration and details where components can be found. The second part presents useful information for collectors.

Aug 1998 ▲ 256 pages ▲ Index
10 halftones ▲ 50 line illustrations ▲ PB
Published in UK

Code 0-7506-3788-9 **£21.99**

INTRODUCTION TO DIGITAL SYSTEMS

John Crisp

This self-study text introduces digital electronics from first principles, before going on to cover all the main areas of knowledge and expertise. It covers the practicalities of designing and building circuits, including fault-finding and the use of test equipment.

Feb 2000 ▲ 302 pages ▲ Glossary ▲ Index
PB ▲ Published in UK

Code 0-7506-4583-0 **£18.99**

NEWNES DICTIONARY OF ELECTRONICS

S W Amos; R S Amos

Aimed at engineers, technicians and students working in the field of electronics, this dictionary provides clear and concise definitions, including TV, radio and computing terms, with illustrations and circuit diagrams.

4th edition ▲ Mar 2002 ▲ 394 pages
100 illustrations ▲ PB ▲ Published in UK

Code 0-7506-5642-5 **£12.99**

NEWNES GUIDE TO TELEVISION & VIDEO TECHNOLOGY

Eugene Trundle

An exploration of television and video technology. It covers the fundamentals of digital television (satellite, cable and terrestrial) and digital video, as well as providing a grounding in analogue systems.

3rd edition ▲ Feb 2001 ▲ 432 pages ▲ Index
PB ▲ Published in UK

Code 0-7506-4810-4 **£17.99**

NEWNES GUIDE TO DIGITAL TV

Richard Brice

Covering all aspects of digital television, this text encompasses the electronics of the equipment, data compression, television production, servicing and the different transition methods - terrestrial, satellite and cable. The text has been updated with developments since the 2000 edition.

2nd edition ▲ Oct 2002 ▲ 304 pages ▲ Index
45 illustrations ▲ 15 photographs ▲ HB
Published in UK

Code 0-7506-5721-9 **£24.99**

PRACTICAL ELECTRONIC FAULT FINDING AND TROUBLESHOOTING

Robin Pain (Design Engineer, Cotag International Ltd)

A text using simple circuit examples to illustrate principles and concepts fundamental to the process of analog and digital fault finding. It aims to help the reader tackle any job, from fixing a TV to improving the sound of a hi-fi. A digital multimeter and oscilloscope are needed for these jobs.

Apr 1996 ▲ 284 pages ▲ Index
50 line illustrations ▲ PB ▲ Published in UK

Code 0-7506-2461-2 **£21.99**

PRACTICAL ELECTRONICS HANDBOOK

Ian Sinclair

A collection of all the key data, facts, practical guidance and circuit design basics needed by a spectrum of students, electronics enthusiasts, technicians and circuit designers. It provides explanations and practical guidance, and includes new sections on SHF techniques and intruder alarms.

5th edition ▲ Feb 2000 ▲ 571 pages
Illustrations ▲ PB ▲ Published in UK

Code 0-7506-4585-7 **£16.99**

RSGB RADIO & ELECTRONICS COOKBOOK

Radio Society of Great Britain

Only a basic knowledge of electronics is assumed for this collection of electronics projects, and it is ideal for all electronics and DIY enthusiasts and experimenters. Designed by the RSGB, the UK radio amateurs federation, the projects are clearly explained step by step.

Nov 2000 ▲ 336 pages ▲ PB ▲ Illustrations
Published in UK

Code 0-7506-5214-4 **£17.99**

REFERENCE DATA FOR ENGINEERS: RADIO, ELECTRONICS, COMPUTERS AND COMMUNICATIONS

Mac E Van Valkenburg; Edited by Wendy Middleton

Written by professionals for professionals, this is a complete reference for engineers, covering a broad range of topics. As well as addressing radio technology data, it covers digital electronics, computers and communications.

9th edition ▲ Aug 2001
1568 pages & CD-Rom ▲ 1385 line illustrations
HB ▲ Published in UK

Code 0-7506-7291-9 **£90.00**

FUZZY LOGIC FOR EMBEDDED SYSTEMS APPLICATIONS

Dr Ahmad Ibrahim

Written by a recognised expert in the field, this covers all the basic theory relevant to electronics design, with particular emphasis on embedded systems. It shows how the techniques can be applied to shorten design cycles and handle logic problems that are tough to solve using conventional linear techniques. All the latest advances in the field are discussed, and practical circuit design examples presented.

Oct 2003 ▲ 312 pages ▲ PB

Code 0-7506-7605-1 **£35.00**

ANALOG INTERFACING TO EMBEDDED MICROPROCESSORS

Stuart Ball

Provides hard-to-find information on interfacing analog devices and technologies to the purely digital world of embedded microprocessors. Gives the reader the insight and perspective of a real embedded systems design engineer, including tips that only a hands-on professional would know. Covers important considerations for both hardware and software systems when linking analog and digital devices.

March 2001 ▲ 288 pages ▲ PB
100 line illustrations

Code 0-7506-7339-7 **£19.99**

HANDBOOK OF RF AND WIRELESS TECHNOLOGIES

Farid Dowla (Lawrence Livermore National Laboratory, University of California-Davis, USA)

Subjects covered include third-generation wireless, wireless sensor networks, RF power amplifiers, spread spectrum modulation, signal propagation and antennaes. This is far more than just a tutorial or reference guide—it is a "guided tour" through the world of cutting-edge RF and wireless design, combining theory, applications and philosophies behind the RF/wireless design process.

November 2003 ▲ 720 pages ▲ HB

Code 0-7506-7695-7 **£59.99**

DIGITAL INTERFACE HANDBOOK

John Watkinson, Francis Rumsey

A detailed manual for those who need to get to grips with digital audio and video systems. It sheds light on the differences between audio interfaces and shows how to make devices "talk to each other" in the digital domain. Also includes detailed coverage of all the regularly used digital video interfaces. New information included in this third edition: dedicated audio interfaces, audio over computer network interfaces and revised material on practical audio interfacing and synchronisation.

3rd edition ▲ September 2003 ▲ 392 pages 231 line illustrations ▲ PB

Code 0-2405-1909-4 **£29.99**

TV FAULT-FINDING GUIDE

Edited by Peter Marlow

A distillation of the most-used fault reports from 11 years of *Television* magazine. Arranged by make and model, it features over 200 reports on over 300 models of television, including diagnosis and repair advice.

Mar 2000 ▲ 387 pages ▲ Illustrations PB ▲ Published in UK

Code 0-7506-4633-0 **£20.99**

VALVE AMPLIFIERS

Morgan Jones

The author's straightforward approach, using as little maths as possible, should be of use to those with only a limited knowledge of the field as well as being the standard reference for experts in valve audio. Design principles and construction techniques are also provided.

3rd edition ▲ Aug 2003 ▲ 624 pages ▲ Index PB ▲ Published in UK

Code 0-7506-5694-8 **£29.99**

VCR FAULT-FINDING GUIDE

Edited by Peter Marlow

A distillation of the most-used fault reports from 11 years of *Television* magazine. Arranged by make and model, it features over 2000 reports on over 200 models of VCR, including diagnosis and repair advice.

Mar 2000 ▲ 447 pages ▲ Illustrations ▲ PB Published in UK

Code 0-7506-4634-9 **£20.99**

DESIGNING AUTONOMOUS MOBILE ROBOTS

John Holland

Covering topics such as advanced sensor fusion, control systems for a wide array of application sensors and instrumentation, and fuzzy logic applications, this volume is essential reading for engineers undertaking robotics projects as well as for undergraduate and graduate students studying robotic engineering, artificial intelligence and cognitive science. Its state-of-the-art treatment of core concepts in mobile robotics helps and challenges readers in exploring new avenues in an exciting field.

January 2004 ▲ PB & CD-Rom ▲ 352 pages

Code 0-7506-7683-3 **£35.00**

VIDEO AND CAMCORDER SERVICING AND TECHNOLOGY

Steve Beeching

A comprehensive guide to domestic VCR technology and repair techniques. This edition brings the information fully-up-to-date, with expanded coverage of camcorders, sections on DVD equipment and the latest VCR technology.

5th edition ▲ Apr 2001 ▲ 323 pages Illustrations ▲ PB ▲ Published in UK

Code 0-7506-5039-7 **£20.99**

VIDEO DEMYSTIFIED

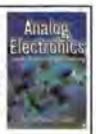
Keith Jack

This edition has been updated to include information on digital television, datacasting, interactive video, digital camcorders and VCRs, and video interfacing. Coverage is international, including European, Asian and North/South American video standards, methods and techniques.

3rd edition ▲ Jul 2001 ▲ 784 pages & CD-Rom References ▲ Glossary ▲ Index ▲ PB Published in UK

Code 1-878707-56-6 **£50.00**

ANALOG ELECTRONICS: CIRCUITS, SYSTEMS AND SIGNAL PROCESSING



D Crecraft (formerly Open University); S Gergely (formerly University of Coventry)

Designed to complement the digital systems modules and develop the essential skills needed for RF circuit design, this book demystifies the art of analogue circuit design and analysis. The content meets the requirements of first and second year electronics engineering courses.

May 2002 ▲ 435 pages ▲ 150 line illustrations PB ▲ Published in UK

Code 0-7506-5095-8 **£19.99**

AUDIO POWER AMPLIFIER DESIGN HANDBOOK

Douglas Self

This text on the design of audio amplifiers is based on Douglas Self's work in *Electronics World* magazine and a career at the cutting edge of audio design. This handbook aims to provide a practical guide to the state of the art, and includes detailed design and construction information.

3rd edition ▲ May 2002 ▲ 448 pages 62 line illustrations ▲ Index ▲ PB Published in UK

Code 0-7506-5636-0 **£24.99**

AVR: AN INTRODUCTORY COURSE

John Morton (University of Cambridge)

AVRs have certain strengths compared to other microcontrollers but are less well-known or understood. The author wrote this guide to introduce AVRs to those who have little or no microcontroller background and to encourage them to start using these useful devices with easy projects to try.

Sep 2002 ▲ 256 pages ▲ 150 illustrations Glossary ▲ Further reading ▲ Index ▲PB Published in UK

Code 0-7506-5635-2 **£16.99**

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Clive Maxfield

The second edition of this comprehensive introduction to contemporary electronics now has added material. It is written for the engineer, hobbyist or student who needs a thorough electronics reference, as well as for non-technical people, and is accompanied by a CD-ROM.

2nd edition ▲ Jan 2003 500 pages & CD-Rom ▲ 184 illustrations 187 photographs ▲ Glossary ▲ PB Published in UK

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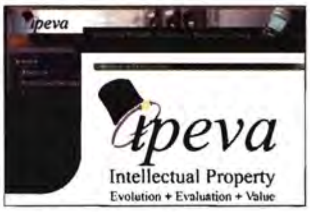

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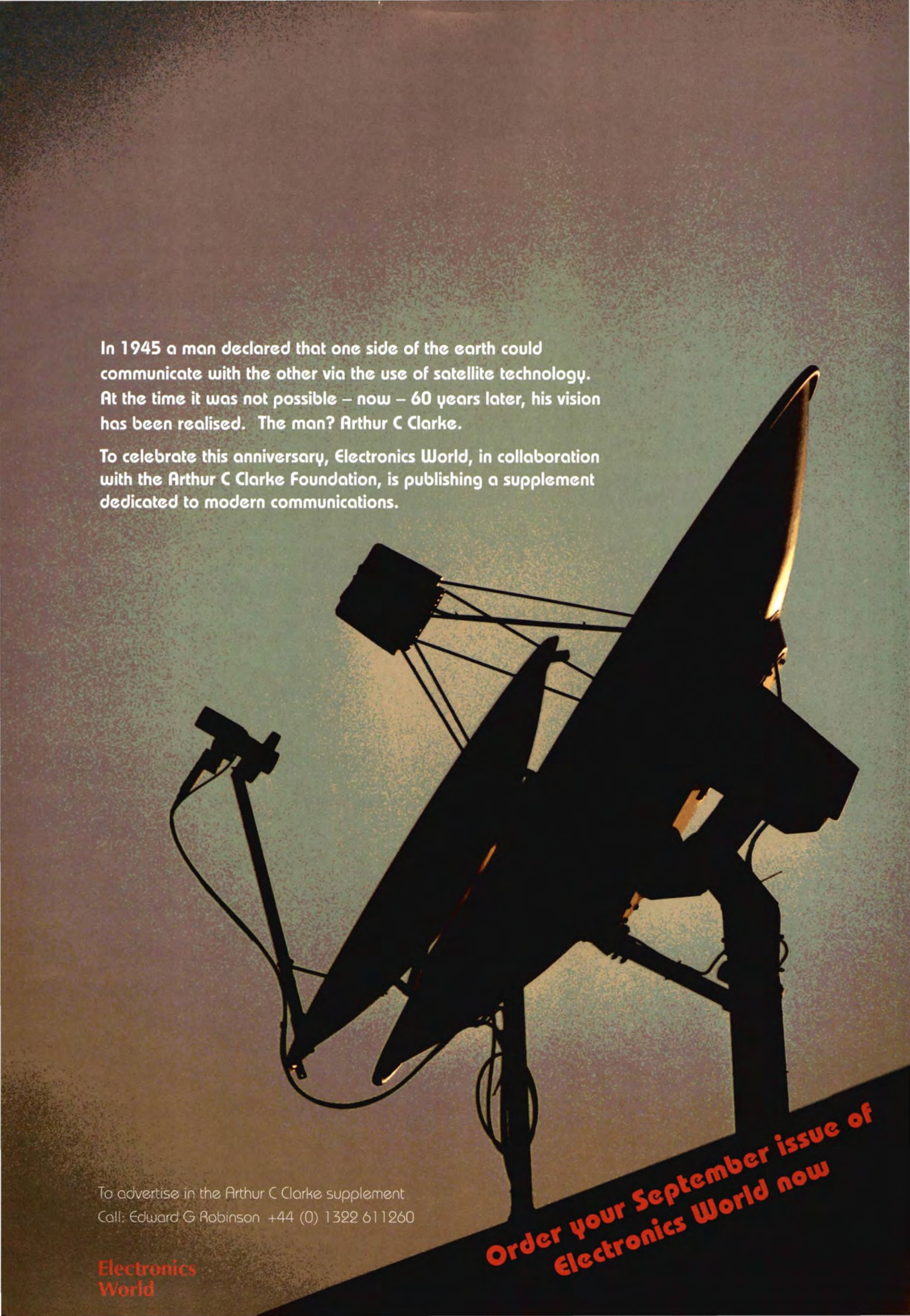
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Anritsu MA2444A 10MHz-40GHz Power Sensor	825	42
Anritsu ML2438A RF Power Meter (Dual Channel)	2520	102
Gigatronics 80301A 10MHz-18GHz Power Sensor	750	37
Gigatronics 80401A 10MHz-18GHz 200mW Mod Pwr Sensor	800	40
Gigatronics 8541C 18GHz RF Power Meter	1350	41
Marconi 6970/001 RF Power Meter	1350	55
POWER SUPPLIES		
Wide Range of AT/HP Programmable DC Supplies .....from	550	20
Farnell AP60/50 60V 50A Power Supply	1750	63
Farnell AP70/30 70V 30A 500W Power Supply	950	32
Farnell L12-10C 12V 10A DC Power Supply	450	36
Lambda LPD-422A-FM Dual 40V 1A DC PSU	495	30
Sorensen DCS600-1.7E 600v 1.7A 1.02W DC Power Supply	1250	54
TPULSE GENERATORS		
AT/HP 8011A 20MHz Pulse Generator	895	45
AT/HP 8012A 50MHz Pulse Generator	895	45
AT/HP 8130A 300MHz Pulse Generator	2750	112
AT/HP 8131A 500MHz High-speed Pulse Generator	5450	233
AT/HP 8133A 33-3000MHz Pulse Generator	13550	571
AT/HP 8160A 50MHz Pulse Generator	2650	107
Philips PM5786B 1Hz-125MHz Pulse Generator	1950	78
RF SWEEP GENERATORS		
AT/HP 8341A 10MHz-20GHz Synthesised Signal Generator	7750	310
AT/HP 8341B 20GHz Synthesised Signal Generator	8650	355
AT/HP 83623A 10MHz-20GHz Hi Power Synthesised Sweeper	19950	798
AT/HP 83640A 10MHz-40GHz Synthesised Sweeper	24995	1000
AT/HP 83752A 10MHz-20GHz Synthesised Sweeper	14500	435
Anritsu 68147B/02/11/14 10MHz-20GHz Synthesised Sweeper	11250	452
Anritsu 68347C 10MHz-20GHz Sweep Signal Generator	16350	655
SIGNAL & SPECTRUM ANALYSERS		
Advantest R3265A 100Hz-8GHz Spectrum Analyser	5950	234
Advantest R4131A 3.5GHz Spectrum Analyser	2595	104
AT/HP 3562A 100kHz Dual Channel Dynamic Signal Analyser	2950	118

	Sale (GBP)	Rent (GBP)
AT/HP 35660A 102.5kHz Dual Channel Dynamic Sig Analyser	3250	98
AT/HP 3585A 40MHz Spectrum Analyser	3500	106
AT/HP 53310A 200MHz Modulation Domain Analyser	2750	115
AT/HP 85024A 3GHz Active Probe	1350	46
AT/HP 8560A/002 2.9GHz Spectrum Analyser	3450	138
AT/HP 8563E 9kHz-26.5GHz Spectrum Analyser	15950	625
AT/HP 8563E/006/026 30Hz-26.5GHz Spectrum Analyser	19950	601
AT/HP 8564E 40GHz Spectrum Analyser	22250	890
AT/HP 8591A/010/021 1.8GHz Spectrum Analyser With TG	3950	119
AT/HP 8591E 1.8GHz Spectrum Analyser	3500	105
AT/HP 8593E/004/041/130 22GHz Spectrum Analyser	12750	383
AT/HP 8594E/041 2.9GHz Spectrum Analyser	4500	149
AT/HP 8595E/004/021/101/105 6.5GHz Spectrum Analyser	6750	204
AT/HP 8596E/041 12.8GHz Spectrum Analyser	10950	438
AT/HP 8901B/001 1.3GHz Modulation Analyser	1950	59
AT/HP 8903B/001/013/051 20Hz-100kHz Audio Analyser	1850	56
Anritsu MS2668C/03 9kHz-40GHz Spectrum Analyser	15750	473
Anritsu MS2711B/05 3GHz Handheld Spectrum Analyser	3650	110
Anritsu MS610B 10kHz-2GHz Spectrum Analyser	2150	65
IFR 2398 9kHz-2.7GHz Spectrum Analyser	4800	202
Marconi 2392 9kHz-2.9GHz Spectrum Analyser	2750	83
SIGNAL GENERATORS		
AT/HP 83711A/1E1 1-20GHz Synthesised CW Sig Generator	7950	239
AT/HP 83712A/1E1/1E5/1E8 0.01-20GHz CW Generator	12250	495
AT/HP 83731B/1E5 1-20GHz Synthesised Signal Generator	16500	660
AT/HP 8642A/002 1GHz Hi Performance Synth Signal Gen	1650	66
AT/HP 8644A 1GHz Synthesised Signal Generator	4595	190
AT/HP 8648A 100kHz-1GHz Synthesised Signal Generator	2500	100
AT/HP 8648C 100kHz-3.2GHz Synthesised Signal Generator	5650	228
AT/HP 8657A 1GHz Synthesised Signal Generator	1600	48
AT/HP 8657B/001 2GHz Synthesised Signal Generator	2350	71
AT/HP 8657D/001 1GHz DQPSK Synthesised Signal Generator	1350	41
AT/HP 8665B 6GHz Signal Generator	26950	1078
AT/HP 8780A 10MHz-3GHz Vector Signal Generator	4450	178
AT/HP 8782B 3GHz Vector Signal Generator	4950	198
AT/HP E4432A/1E5 3GHz Synthesised Signal Generator	5950	179
AT/HP E4432B/1E5 3GHz Signal Generator	8550	343
AT/HP E4433B 250kHz-4GHz Signal Generator	9350	374
Marconi 2032 10kHz-5.4GHz Signal Generator	8450	254
Marconi 2051/001 10kHz-2.7GHz Digital & Vector Sig Gen	5950	238
Marconi 2052 5.4GHz Digital & Vector Signal Generator	14450	580
National VP-7201A 500kHz RC Oscillator	485	45
R&S SME03/B11 5kHz-3GHz Signal Generator	5450	218
R&S SMIQ03B/B1/11/12/14/..... 3.3GHz Vector Sig Gen	11950	359
WIRELESS		
AT/HP 8923B DECT Test Set	4250	187
IFR 2967/12/16/21 Radio Comms Test Set With GSM & TACS	5950	179
Marconi 2935 GSM Test Set [Tri Band]	4950	179
Marconi 2945/05 Radio Comms Test Set	5950	150
Marconi 2955B 1GHz Radio Comms Test Set	3500	126
Marconi 2966A/12 1GHz Radio Comms Test Set with GSM	5850	176
R&S CMD55/B1/3/4/6/9/41/42/43/44/61 Rad Com Test Set	4950	198
R&S CMU200/B11/B21/K21/K22/K23/K24 Rad Com Test Set	27250	1090
Racal 6103/001/002 Digital Mobile Radio Test Set	3950	159
Racal 6103/001/002/014/420/430/04T Mobile Radio Test Set	4250	128
W&G 4106 GSM/DCS1800/PCN1900 Mobile Phone Tester	2250	70
Wavetek 4107 Mobile Phone Test set - Triband	2750	83
WaveTek 4202S Digital Mobile Radio Test Set - Triband	3950	158
Wavetek 4400M GSM Test Set	12950	467

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www.TestEquipmentHQ.com
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