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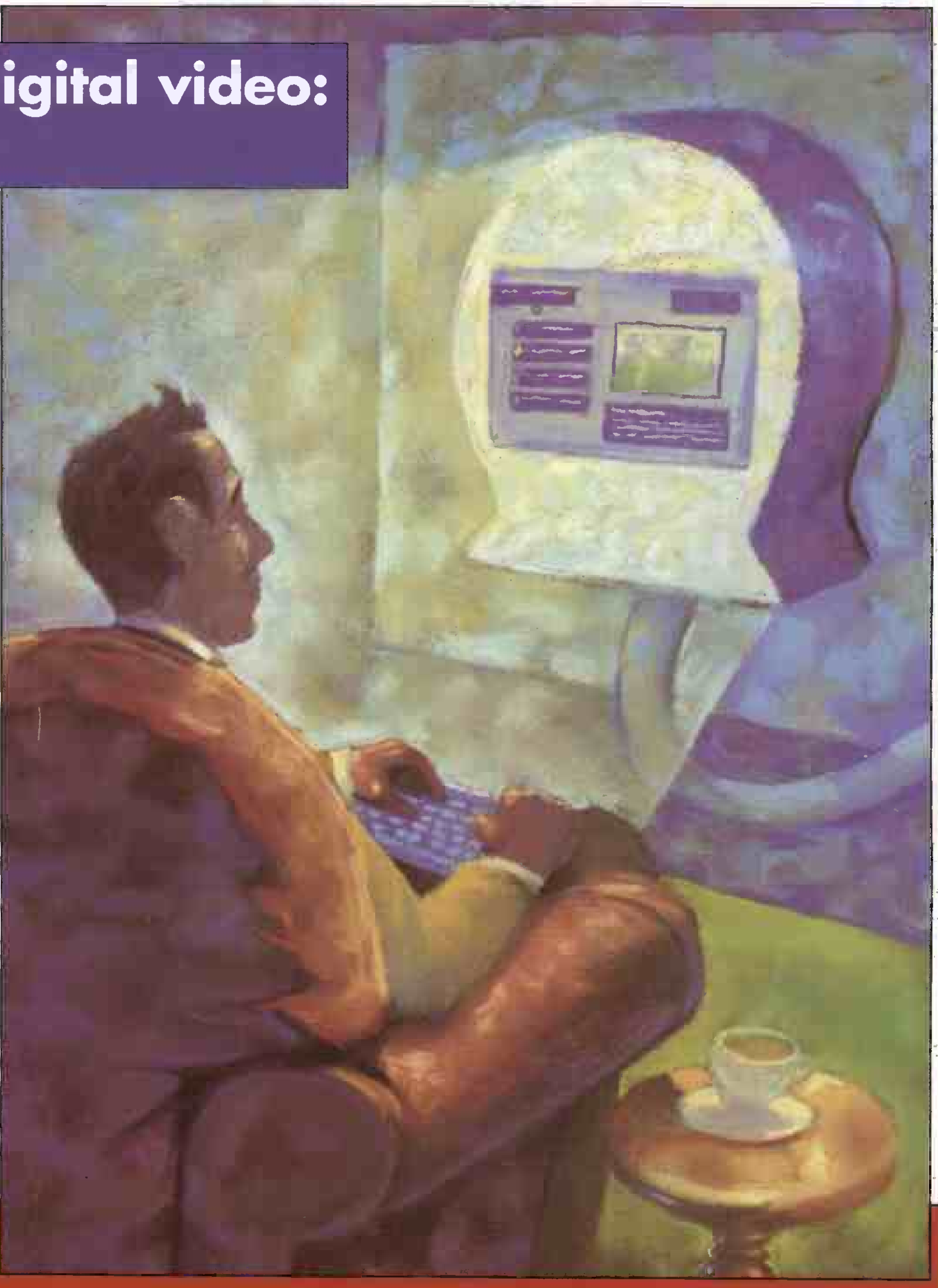

Tester for SDI digital video: PCBs available

USB made simple

Is power-line comms viable?

Indicator for Self's Class-G

One pot. for two channels

Supercaps in auto apps

VHF direction finder – pt II

Circuit ideas:

- Use two phones as an intercom
- Photovoltaic current sensing
- Optoelectronic square roots
- Simple full-wave audio-limiter
- De-rippler for EHT supply
- Clipping indicator

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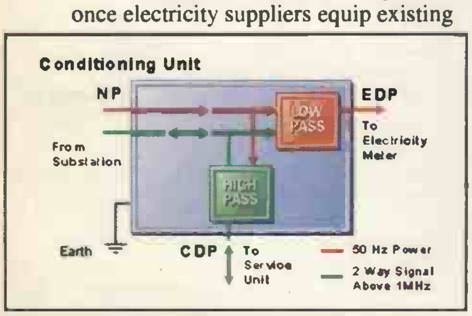

power linesto carry communications as well as energy. They believe they can revoke the laws of physics but others are not so sure. **Andrew Emmerson** examines the evidence.

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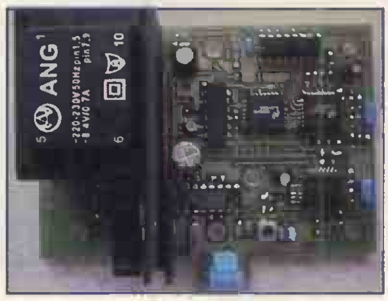
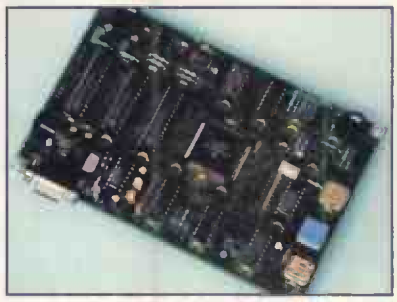
Illustration Jamel Akib



Testers for analysing SDI digital video streams can be expensive. Emil Vladkov's SDI generator and receiver described on page 18 provides a low-cost alternative without compromising on performance.



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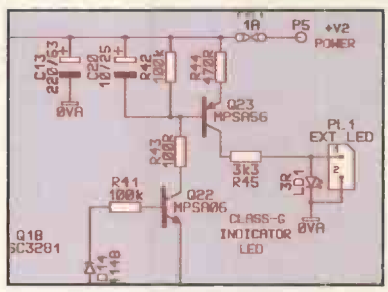

Class G? If you've built Doug Self's Class-G amplifier, you can find out how often it switches to the high-voltage rails by adding the LED indicator described on page 59.

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Another brick in the wall?

We live in an insecure world. We became jittery long before the terrible events of 11 September, and we have looked to technology to help us. But will the increasing sophistication of this technology pose a threat to individual liberty?

Just how far should we go? Is there a limit?

We have never felt secure. Ancient mankind lived in settlements protected by ramparts. Huge defences were built to keep invaders out or to delineate borders, such as Hadrian's Wall or Offa's Dyke.

Locks and keys were in use long before the birth of Christ. Padlocks were used by the Romans and the Chinese to protect their treasure. One Indian emperor used to protect his valuables by surrounding them with a pool of hungry crocodiles.

We can be more relaxed now as we have burglar alarms on our houses and we may soon be able to check our house security through a 3G mobile phone. To make sure we are who we say we are retina scan identity checks are promised at banks and places of work.

Street crime has always been a problem and an effective way to counter it is to install closed-circuit television Cameras. In August, the Government announced plans to spend £79m on new CCTV systems. The Home Office hopes to establish or expand some 250 schemes in city centres, housing estates, railway stations and car parks across England and Wales.

It is estimated that there are now more than a million CCTV cameras in operation in Britain. It is also reckoned that, on average, each person in London is caught on camera at least 300 times a day.

Around the City of London is the 'ring of steel' where CCTV cameras can read car number plates. If a car is seen that is on a list then an alert is sent out to the police. It has been known to make mistakes!

Ken Livingston wants to levy a "congestion charge" on London motorists and will police it with more cameras with this software.

However, programs are being developed that can recognise people from their mannerisms. This too could be attached to a database of "undesirables" and raise the alarm.

I wonder if Mr Livingston will be interested to use this software in his scheme? Perhaps he could prevent some MPs from getting to Parliament.

The Data Protection Act does set strict rules on the review and storage of CCTV data. However my worry is that you don't know who is looking at you. Surely cameras should have a plate attached saying who owns the camera and where the data is stored.

We are persuaded that CCTV is a good idea by the seductive argument that it reduces crime. I'm sure it does – but at what cost to individual liberty?

Of course you have nothing to fear if you are not doing anything wrong.

"If you want a picture of the future, imagine a boot stamping on a human face – for ever." – George Orwell, Nineteen Eighty-Four.

http://www.privacyinternational.org/bigbrother/

The Government is also spending more money on speed cameras, hoping to triple the number to 12 000. Although, to help the motorist who panics when he sees one, they are to be clearly visible – that is, painted bright yellow and not placed behind road signs. Again, sophisticated software will read number plates and relay the information to a central control, which will issue speeding tickets.

What happens if the software is inaccurate? I suppose it will be up to the motorist to prove that he or she is not guilty. Of course, you could always claim that you couldn't remember who the driver was, as one Detective Superintendent recently used in his defence.

Again, the seductive argument is that speed cameras save lives so we must have them, mustn't we?

I recently took my dog to the vet to have a tag inserted in his skin under the collar. This tag stores a unique number that can be read by a hand-held device linked to a database containing all his information.

How long will it be before babies have a tag inserted at birth that will store medical records, qualifications, residences – indeed, everything about them? The tag could also have a GPS chip that could tell the authorities exactly where the baby was. It could never happen, could it?

The Government tried to introduce identity cards in the UK just after 11 September. Their introduction is only a question of time. No doubt seductive arguments will be used to ensure that ID cards are adopted. They will reduce crime, help track undesirable people, and prevent terrorism.

Technology enables us to do some great things. But we have to be very careful that it doesn't take us prisoner. ■

Peter Marlow

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UPDATE

Airship communication satellites will stay aloft for five years

Airships aloft for five years at a time could replace costly communication satellites if a UK company can find development partners.

Bedford-based ATG is proposing a 200m long solar-powered blimp called StratSat that will hold a station in a 1km cube at an altitude of 20km under its own power.

"The wind at this altitude is mostly relatively benign. Only one per cent of the time do you get ferocious winds of 50m/s [110mile/h]," said ATG avionics engineer Ray Hills.

Electric motors will keep the balloon in position, although diesel power will be available. Solar cells will be attached to a strip on the top of the blimp. The blimp has no gondola and is symmetrical about its long axis so moving the internally-suspended payload will roll the balloon to keep its solar cells facing the sun.

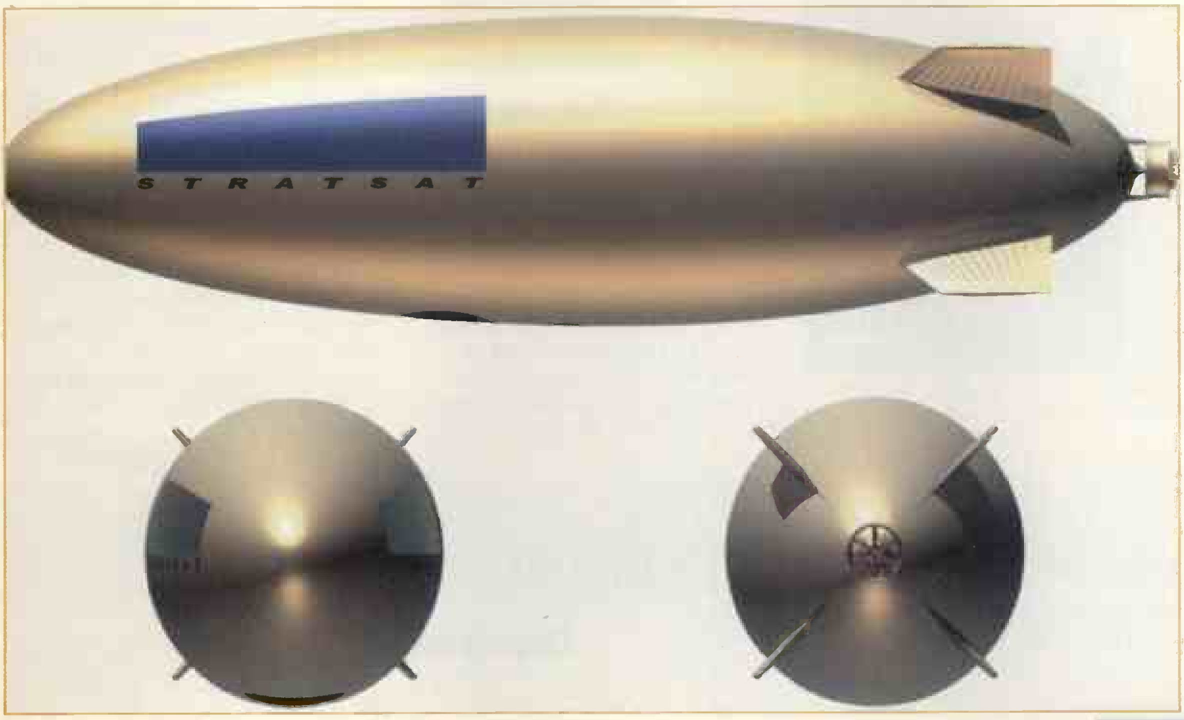
Batteries will run the propulsion system, airship services and provide power to the payload for up to 14 hours – the length of a winter night.

The outer shell of the blimp, which acts to keep helium in and weather out, is to be made from an ultraviolet-resistant Tedlar-Teflon fabric – probably with a gold film as a further barrier to solar radiation.

"The idea is to fly them over dense urban areas – 19 could cover the UK," said Hills.

A small prototype has already been flown.

● The name blimp may come from military classification. Airships or balloons were classed as 'B' category. Non-rigid ones were 'limp' and hence B-Limp.
www.airship.com



A fleet of 19 of these blimps could provide comms coverage for the whole of the UK.

Plastic LED company branches out

Light emitting polymer company Cambridge Display Technology (CDT) is adding to its display technology portfolio by licensing intellectual property from Luxell Technologies of Canada.

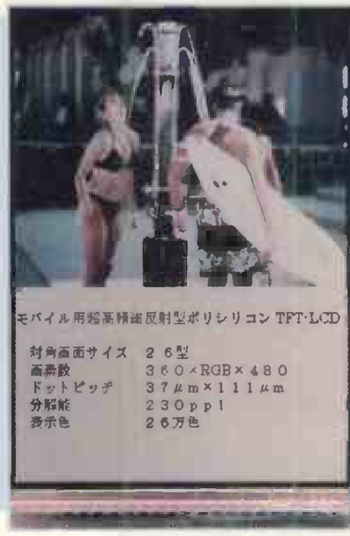
The agreement is the result of an evaluation by CDT and Luxell that demonstrated enhanced contrast in LEP displays that included Black Layer, as the technology is called.

Under the terms of the agreement, CDT acquires exclusive marketing rights to sub-license Luxell's Black Layer technology for LEP flat panel displays and Luxell will receive, subject to specified conditions, licensing fees, production royalties and other payments.

Black Layer consists of two added layers deposited behind the light emitting layer that are optimised to phase shift incident light and reflect it back, effectively eliminating it.

The deposition tools are the same as those now used in standard display manufacturing.

Next year's crop of mobile phones are expected to feature displays such as this one from NEC. A low-temperature polysilicon TFT, the LCD is split into a 352 by 288 pixel TV display and a text area. The so-called 'chip-on-glass' technique allows the driver circuits to be integrated on the display itself, reducing display size, cost and poer consumption. Up to 260 000 colours can be displayed.



Man-made buckyballs come a step closer

Buckyballs, the spherical molecules formed by 60 atoms of carbon, are fast becoming the holy grail of chemistry.

It is not that they cannot be found, it is that they cannot be made reliably.

So far, all scientists can do is filter them out of soot.

Recently a team from Boston College in Massachusetts lit a beacon of hope for chemists.

It specialises in designing custom molecules and has synthesised a flat lattice-like molecule $C_{60}H_{30}$ which is effectively an un-rolled buckyball with hydrogen atoms around the edge.

A UK team from Warwick University has taken the Boston molecule and rolled it into a C_{60} buckyball using a laser.

Close analysis confirms that the buckyballs are formed directly from curling molecules, not from the debris of blasted molecules.

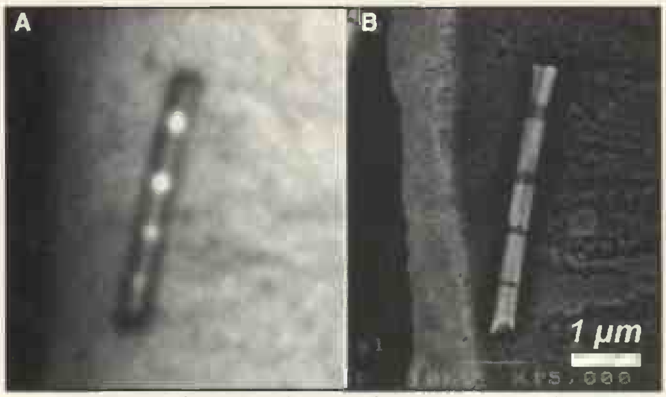
"It is not synthesis, but it is a very very big step in the right direction," said Warwick team member Thomas Drewello.

Boston is extending its work, trying to replace at least some of the hydrogen around the edges of its molecule with chlorine or chlorine-hydrogen combinations.

This, according to Drewello, will make it easier to set the carbon lattice free and may lead to a fully synthetic, non-laser, route to C_{60}.

Buckyballs are finding their way into various electronic devices including a new generation of plastic solar-cell semiconductors.

Tiny barcode strips tag minuscule biosamples



With stripe lengths in the tens of nanometre range, barcodes like this one could be used to tag biological samples.

Chemists from Pennsylvania State University in the US have manufactured striped metal 'barcodes' measuring just a few micrometres in length. They could be used to tag biological samples, the team hopes.

Several different metals, including gold, silver, nickel, platinum and copper, can be deposited in varying lengths along the tag, which has a width of less than a micrometre.

Multi-metal rods have been made with up to 13 layers, with lengths from 10nm to several micrometres.

The image shows a multiple stripe rod made from gold and silver. The gold stripes are around 550nm long while the silver have lengths of 240, 170, 110, and 60nm from top to bottom.

Optical reflectance microscopy is one technique that can be used to identify the tags, as the metal stripes used have different optical properties.

The team from Penn State, led by Dr Christine Keating, produced the stripes by depositing metal ions through electrochemical reduction into the pores of a membrane. The membrane's pore diameter sets the particle width, while the charge sets the length.

LCD revenue set to outstrip CRT's by 2003

A report from Reed Electronics Research says that by 2003, the liquid crystal display will have overtaken the CRT in terms of revenue.

Last year worldwide sales of CRTs amounted to $27.5bn, while LCDs came close reaching $25.0bn. The remaining $2bn of the total displays market came from technologies such as plasma, field emission, ferroelectric and polymer displays.

LCDs are expected to pass CRTs in 2003, and by 2005 LCDs will account for 56 per cent of the market, 49 per cent being active matrix and seven per cent being passive type LCDs.

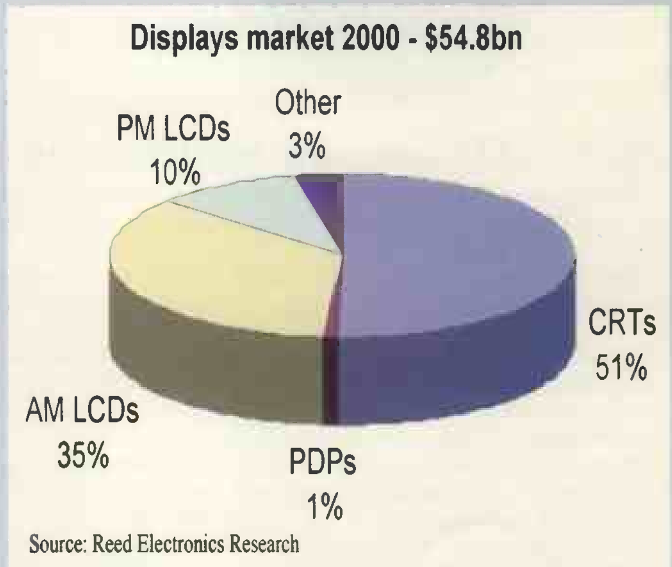
So while active matrix LCD will be worth over $41bn by 2005, CRT will only have grown to around $30bn, says RER.

The quicker growth of LCD, active matrix in particular, is down to notebook PCs, flat panels for desktop PCs, mobile phone displays and LCD TVs.

Meanwhile, several LCD manufacturers have either increased prices or signalled a halt in the price drop of the displays.

Samsung, Philips and Hitachi have all increased prices of 15in panels, while Sharp is expected to follow.

TFT LCD prices dropped from close to £1000 to under £300 during 2001. The sharp drop was blamed on new entrants from Taiwan who came into the market around a year and a half ago.



Design tools aid device-driver and API writers

UK design tool firm Beach Solutions has released software in its EASI range aimed at improving the development of device drivers and software models.

EASI (embedded application system interface) tools help bridge the gap between hardware and software engineers, said Terry McCloskey, CEO at Beach.

"We provide tools for customers to capture information on a system-on-chip [SoC] design into a centralised file," he said.

EASI-C++ is used to create a library of C++ classes and functions for controlling a peripheral over an SoC bus. This information can be used by the software engineer to quickly write the device driver or API for that peripheral.

This latest tool extends existing C-based software. The beauty of EASI is that the programmer does not need to know or understand the underlying hardware, said McCloskey. In fact, the hardware can change, and the EASI tool updates the API allowing the application software to remain the same.

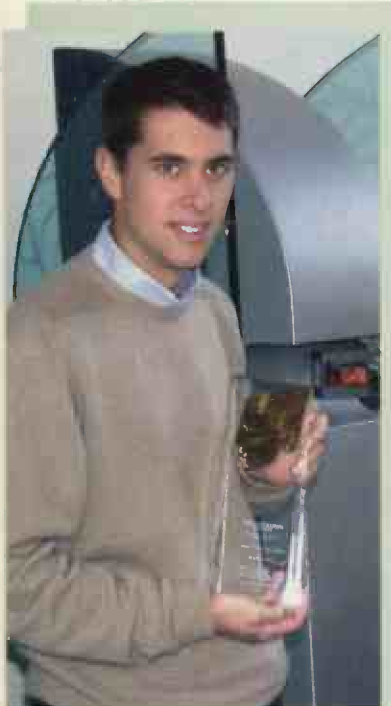
Beach, with offices in Cambridgeshire and Devon, also has tools for hardware engineers.

"On the hardware side we generate a bus interface in VHDL or Verilog for each of the peripherals," said McCloskey. Today Beach supports three main flavours of bus; the AMBA AHB or APB, CoreConnect and the VCI bus.

The tools produce a file containing the programmer's view of the SoC, including a list of the peripheral blocks, all the data and control registers and bit fields within those registers.

Using a single source for hardware and software can reduce the chance of errors being introduced, said the firm.

www.beachsolutions.com



How's this?

A cricket ball tracking system called HawkEye has won its inventors the Innovative Applications category at the Royal Television Society awards for Technical Innovation.

Roke Manor Research's Hawk-Eye uses multiple cameras to accurately track the path of a cricket ball, and was used by Channel 4 in its cricket coverage last year. The technology's inventor, Dr Paul Hawkins, is pictured with the award.

120Gbyte drives for notebook PCs

Hard disk drives with capacities of 60 and 120Gbyte have been launched by IBM. The 3.5in drives are aimed at the notebook and desktop PC markets respectively. The Deskstar 120GXP runs at 7200rev/min while the Travelstar60GH (pictured) hits 5400rev/min. Both drives have three platters.

World's first behind-the-ear speech processor

A low-power chip process from Zarlink has made possible the world's first behind-the-ear speech processor with built-in telecoil for telephone use and plug-in FM receiver, claims its maker Cochlear.

Called ESPrit 3G, the external part of the hearing aid includes Babel 24, an ultra low power mixed-signal chip jointly developed by the two companies.

"Our advances in ultra low-power microchip technology is influencing the development of all our medical integrated circuits," said Steve Swift, v-p for medical products at Zarlink.

Zarlink and Cochlear have worked together before and Babel 24 is only the most recent development in an eight-year relationship. Joint R&D teams in Australia and at Zarlink facilities in Europe and the US have developed core integrated circuits for the entire range of ESPrit speech processors.

Babel 24 uses a switched capacitor filter bank for programmable spectral analysis at low power.

The chip is designed in 0.35µm CMOS and is made at Zarlink's wafer fab in Plymouth, Cornwall.

A Cochlear-designed chip for the associated implant is manufactured at Zarlink's fab in Quebec.

The plug-in FM receiver allows users to listen to the TV via a wireless FM link.

www.cochlear.com www.zarlink.com

Thermal image of Mars reveals frozen CO_2

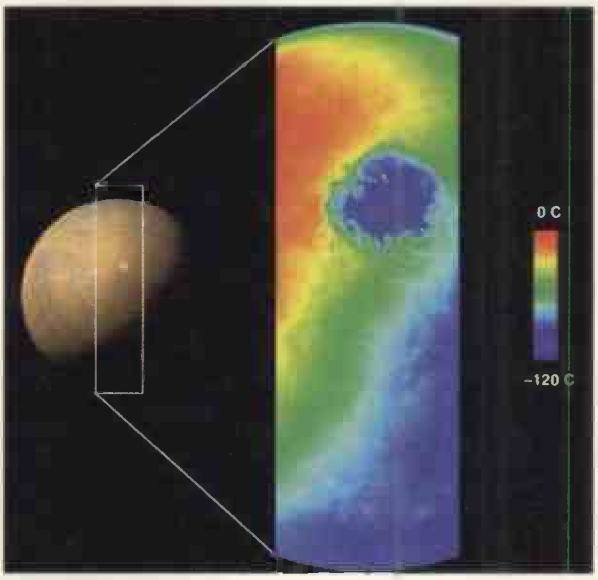
This thermal image of the surface of Mars was sent back by Mars Odyssey, the latest NASA probe to reach the red planet.

Frozen carbon dioxide at the Southern pole can clearly be seen, along with both the day and night sides of the planet.

At the moment Odyssey orbits Mars every 18 hours in a highly elliptical orbit, reaching a near point of 128km, and a high altitude of 27000km from which this image was taken.

Aero-braking using the thin atmosphere will eventually bring the spacecraft down into a circular orbit some 400km above the surface.

Odyssey's main computer used for command, control and data transfer back to Earth runs the VxWorks operating system from Wind River. This real-time OS will also be used to run the emergency descent capsule from the International Space Station.



CPLD meets FPGA

Chips that close the gap between complex programmable logic devices, or CPLDs, and the field-programmable gate arrays, FPGAs, have been developed by Lattice Semiconductor.

The US firm has developed a CPLD with on-chip phase-locked loops and high-speed I/O, alongside the traditional CPLD macrocells with their wide gating features.

The ispMACH5000VG is aimed at bridging between communications interfaces and different bus architectures.

In order to support more complex functions, the inputs to the macrocell arrays have been widened from 36 to 68 bits.

"We actually feed 163 product terms into the OR-array. You can build up quite large logic functions," said Bernie Perrin, European marketing manager at Lattice.

The size of the device – 1024 macrocells – and the mix of features such as PLLs and fast I/O, makes the device appear more like an FPGA.

"1024 macrocells is starting to approach the bottom end of FPGAs," said Perrin.

However, the size brings its own problems, particularly when it comes to routeing between logic blocks.

The 5000VG is split into eight segments, with each segment containing four generic logic blocks, each of which has 32 macrocells.

Routeing signals between blocks in a segment is straightforward, but in order to transfer data across the chip, the firm needed to add an extra level of routing.

"It does have an impact on speed if you try and go from one side of the chip to another," said Perrin. "But provided you stay in a segment you can get a 5ns propagation delay."

This 5ns is from pin-to-pin. Pin-to-pin going via logic in separate segments increases T_{pd} to 6.5ns.

"One of the problems we've got in programmable logic is that no one size fits all; you've got to make compromises," Perrin pointed out. "Do you want fast, wide or high density?"

The 5000VG seems to deliver on high density and wide inputs, but has to drop some speed for the longer signal routes.

The chip has four separate I/O banks, and pins can support several I/O standards such as LVTTL, LVCMOS, PCI, HSTL, SSTL, LVDS and GTL+.

Moreover, each I/O bank is able to set its own V_{cc}, V_{ref} and Gnd. This allows different standards to run on the same chip, enabling bridging between the standards.

In addition, for low voltage CMOS, the drive current is programmable. For example, a 3.3V output can be driven from 4 to 20mA in six steps.

Programming is in-system, and is IEEE1532 compliant. And unlike FPGAs, the device is active on power-up, storing its program in EPROM – not a separate flash chip that must be downloaded into SRAM.

Four function wireless remote

The maker of transmitters and receivers suitable for the wireless remote controller described in last month's issue is the Italian company Aurel.

http://www.aurel.it/

The main UK distributor for Aurel in the UK is Chartland Electronics:

http://www.chartlandelectronics.co.uk/

Tel: 01372 363666, Fax: 01372 363833, e-mail: Sales@chartlandelectronics.co.uk

Touch screen gives access to 23 million records

Fingerprint and facial recognition software has been added to a Volvo T5 used by the Kent Police Force. The vehicle has touch screen access to police databases along with voice activated systems such as lights and sirens. Automatic number plate recognition can check through 23 million records in under one second.

Researchers discover largest conductive particle

A collaboration between Toshiba Research Europe and the Universities of Cambridge and Nijmegen has uncovered the largest conductive particle yet.

Called a trion, the particle consists of two electrons and a hole and is 50nm across – compared with electrons that are 10^{-22}m across and nuclei in typical semiconductors that are 0.3nm apart, according to Toshiba.

"A trion is a bit like a hydrogen ion," said Dr Andrew Shields of Toshiba. "It forms when an electron joins an electron-hole pair. The electron is more attracted to the hole than repelled by the other electron."

Unlike an un-charged electron-hole pair, the trion is charged and moves in an electric field.

"An electron-hole pair is a neutral exiton that does not move in a field. The trion actually moves surprisingly quickly for such a large particle – only three times slower than an individual electron," said professor Michael Pepper, joint managing director at Toshiba.

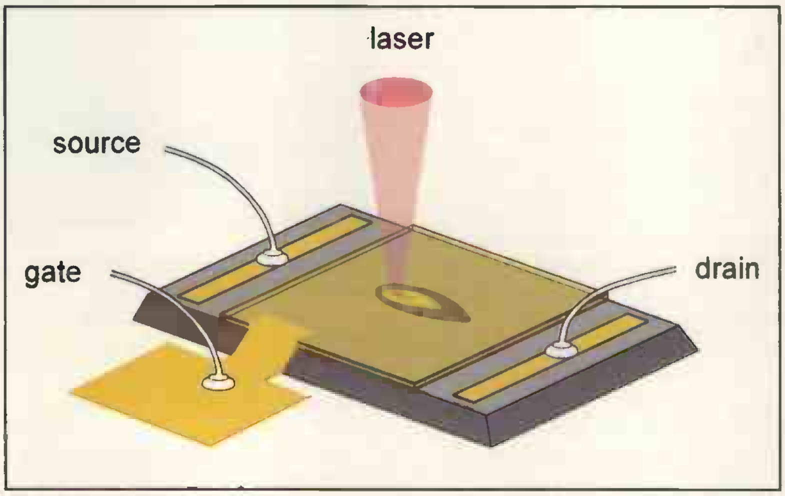
The trion was made by shining a laser onto GaAs to make electron-hole pairs, then adding another electron in a quantum well of a transistor structure, according to Shields.

The trion only lasts for about 1ns before one of the electrons falls into the hole, but before this happens, it can be moved a few micrometres.

Evidence for trion existence comes from the characteristic photon emitted on combination – which differs from that emitted by recombination in a neutral exiton.

Shields says that trions could be used as temporary mobile photon stores in future devices, and that they can in principle be made entirely electrically.

"For instance, in the future it may be possible to use this phenomenon to make light sources where we can modulate the output intensity or wavelength by moving the trions around in the chip," he said.



The biggest charged electrical particle so far discovered can be formed when a laser creates an electron-hole pair in an electron-rich quantum well. The hole attracts a further electron and the electron-electron-hole triplet called a trion can be detected drifting in an electric field before it decays into an electron and a photon.

Mathematical model may help improve damaged vision

Cornell University in New York State is constructing a mathematical model of human vision to help visually impaired people.

"It offers an opportunity to use computer graphics technology to make a real difference in people's lives," said James Ferwerda of the Cornell computer graphics programme.

The model will be based on actual visual processing, beginning with the absorption of light by rod and cone photoreceptors, moving through retinal processing and on to the multi-step processing that occurs in the brain.

By adding damage known to be caused by various diseases to the model, then understanding how images appear to the sufferer, Ferwerda hopes to pre-distort images so that they appear correct to a person with that particular disease.

For example, said Ferwerda, one way to aid people with macular degeneration might be to shift the central portion of the visual field to an undamaged part of the retina, then modify contrast at the image edge to make up for off-centre detail loss.

By the end of the project, he hopes to have created small hand-held devices that will help visually impaired people read and move around.

New additions to on-line design/prototype tool set

National Semiconductor has added simulators for flash microcontrollers to Webench, its online design and prototyping tools.

Webench 3.0 adds the simulator to the existing tools for the design of power supplies, PLLs and loop filters.

The microcontroller software allows designers to select a processor then configure on-chip peripherals, registers and interrupts, followed by code generation.

Last year the firm reckons some 41 000 power supplies were designed using its online tool. National claims each of these saved over 40 hours of design time. ■

Claimed to be the most powerful computer for open research, Terascale, the 6teraflops computer in Pittsburgh, has officially started work. Terascale has 750 quad-processor AlphaServers running Tru64 UNIX. Some 3400 litres of water per minute are used to take heat away.

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Track

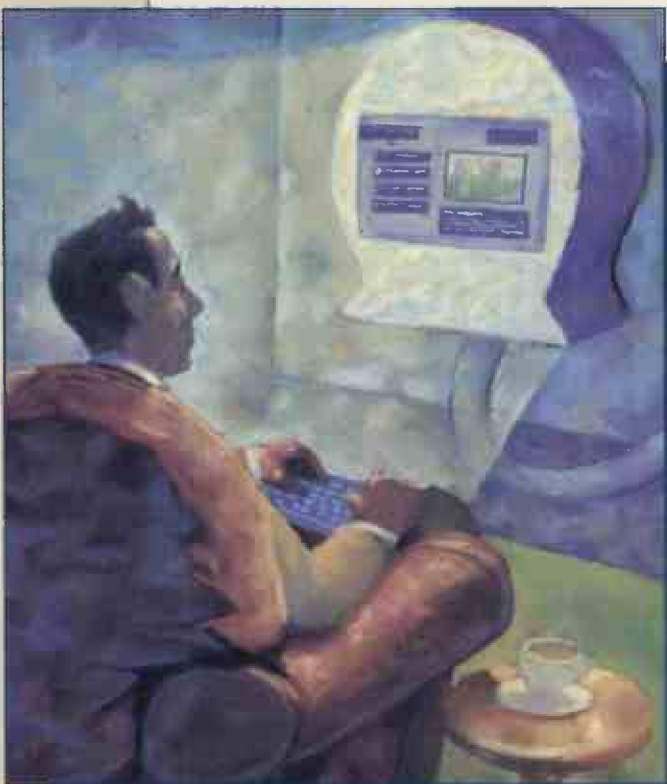
1 Washington Post March, Band, 1909
2 Good Old Summertime, The American Quartet 1904
3 Marriage Bells, Bells & xylophone duet, Burckhardt & Daab with orchestra, 1913
4. The Volunteer Organist, Peter Dawson, 1913
5. Dialogue For Three, Flute, Oboe and Clarinet, 1913
6. The Toymaker's Dream, Foxtrot, vocal, B.A. Rolfe and his orchestra, 1929
7 As I Sat Upon My Dear Old Mother's Knee, Will Oakland, 1913
8 Light As A Feather, Bells solo, Charles Daab with orchestra, 1912
9 On Her Pic-Pic-Piccolo, Billy Williams, 1913
10 Polka Des English's, Artist unknown, 1900
11 Somebody's Coming To My House, Walter Van Brunt, 1913
12 Bonny Scotland Medley, Xylophone solo, Charles Daab with orchestra, 1914
13 Doin' the Raccoon, Billy Murray, 1929
14 Luce Mia! Francesco Daddi, 1913
15 The Olio Minstrel, 2nd part, 1913
16 Peg 0' My Heart, Walter Van Brunt, 1913
17 Auf Dem Mississippi, Johann Strauss orchestra, 1913
18 I'm Looking For A Sweetheart And I Think You'll Do, Ada Jones & Billy Murray, 1913
19 Intermezzo, Violin solo, Stroud Haxton, 1910
20 A Juanita, Abrego and Picazo, 1913
21 All Alone, Ada Jones, 1911

Total playing time 72.09

21 tracks – 72 minutes of music.
Published by Electronics World. All recordings reproduced by Joe Pengelly.

Powerline communication

the dream that refuses to die



Bandwidth by the bucketload is promised once electricity suppliers equip existing power lines to carry communications as well as energy. They believe they can revoke the laws of physics but others are not so sure. Andrew Emmerson examines the evidence.

Will you be receiving broadband Internet and telephone service from your electric power company in a few years time? Delegates to the Powerline Communications World Congress held in Brussels during September 2001 were hoping so. Yet other observers dismiss the whole idea as yet another false dream – and a mighty expensive one too.

All the same it's an alluring notion. With governments banging the broadband drum and users yearning for low-cost bandwidth, it's hardly surprising that power companies scent money in this opportunity.

Telecomms vendors are equally keen to assist the electricity industry apply leverage to its existing assets and proclaim the effectiveness of their solutions most eloquently. The technology is cost-effective, it needs no new wires and everyone wants it. Or so you might believe.

What it is

Communicating over electricity mains uses the existing supply wiring – 117V, 230V, etc. – to carry information as well as energy. This concept can be applied to local-area networking using internal wiring within the home or workplace. It can also provide access to the public network over the feeders that connect consumers' premises to the local substation.

As a commercial proposition, it's the latter opportunity – providing access to the public network – that's exercising the minds of the power companies. With the delays and uncertainties of unbundling the European and US local loops and the stagnation surrounding broadband fixed wireless access, powerline technology is attracting considerable attention as a local-access technology.

What's in a name?

The terms powerline telecommunications, or PLT, and powerline communications, PLC, are used interchangeably in this field. Digital Powerline, abbreviated to DPL, is the proprietary name used by Nortel, while PLC also stands for powerline carrier – alias mains-borne – the low-speed data system used by electric power utilities for their own purposes.

Applications include telephony, computer networking and broadband data distribution for individual consumers as well as supervisory signalling for controlling the power companies' own equipment. For marketing purposes some people describe it as a kind of 'wireless' communication mode since the technology avoids the need for separate dedicated wiring for this communication purpose.

Greed and gullibility

We'll detail the underlying technology in a moment but first we need to see what's fuelling this feeding frenzy. Power generation and distribution is a highly competitive business and utilities would dearly like to tap into new revenue streams.

Adding a communications capability appears highly desirable since it uses existing infrastructure into customers' premises, requires far less new capital investment than competing wireline cable and wireless access technologies – under £500 per connection according to one report. It also offers supplier and consumer alike the advantage of one-stop billing.

According to Jarek Chylinski, vice-president of global marketing at hardware vendor Enikia, powerline offers, "a unique opportunity for utilities to provide bundled services to consumers, bypassing the need for multiple bills."

In view of this there's no shortage of utility companies keen to undercut incumbent carriers and deliver high quality voice and data services to businesses and homes using powerline technology. A key imponderable remains though. And it could prove a major stumbling block.

The issue is electromagnetic compatibility, or EMC for short; power lines carrying data signals are likely to radiate, interfering with broadcast signals. Bean counters make little of the issue and vendors argue that interference problems can be overcome. Others are less confident and are putting their faith in existing regulations against undesirable transmissions.

Up to now, debate has been mainly theoretical but with concerted tests having now started in Germany, many bodies will be observing the results. If these are successful and interference is contained, major deployment of the technology is forecast to follow, initially in Germany and also in Spain and Scandinavia.

What's on offer

Commercial applications for powerline communication include high-speed Internet access, entertainment distribution, voice telephony and fax using Voice over Internet Protocol (VoIP), building automation, meter reading and remote surveillance for building security and healthcare.

Data rates are not spectacular, however. Although products available currently work at up to 2Mbit/s, once several users are sharing the same data stream these speeds will drop significantly. Higher speeds are promised in future, however. Media Fusion speaks of individual network connections of 2.5Gbit/s – albeit without further substantiation.

Analysts see the USA and western Europe as the regions most likely to adopt powerline communication although whether it can compete is another matter. Although consumer demand for low-cost broadband is undoubtedly strong, cable TV/telecom penetration is already high – 75 per cent in the USA and higher in some west European countries.

Hardware vendor Ascom sees the chief marketplace in countries where the existing telecomms infrastructure

Web sites to watch

Adaptive Networks (vendor site)
http://www.adaptivenetworks.com/

Ascom Powerline Communications AG (vendor site)
http://www.ascom.com/

Clarent (vendor site)
http://www.clarent.com/products/

Enikia (vendor site)
http://www.enikia.com

European Telecommunications Standards Institute (sets EMC standards for powerline networking)
http://portal.etsi.org/portal_common/home.asp?tbkey1=PLT

HomePlug Powerline Alliance (forum for the creation of open specifications for high speed home powerline networking products and services)
http://www.homeplug.org/

Media Fusion (vendor site)
http://www.mediafusioncorp.com*

Oneline (vendor site)
http://www.oneline.de

Powerline Technologies (vendor)
www.powerline.com

Powerline World (online community for the development and deployment of powerline communication services and products)
http://www.ipcf.org/

**This site was out of action at the time of writing but the unavailability may be temporary – Ed.*

Prior art

The idea of using power lines for communication purposes dates back seventy years or more. Power companies ran telephone calls over high-tension cables, in connection with pioneer hydro-electric and rural electrification schemes. Regional electricity companies in Britain have for some years exploited low-speed 'mains-borne' data transmission for remote meter reading and control purposes.

Pioneer development of higher capacity systems was carried out jointly in Britain by telecomms vendor Nortel and comms operator Norweb Communications – born out of the power utility Norweb and since renamed Your Communications – starting 1995.

The two companies named a Manchester school as the world's first public user of their technology breakthrough in December 1997 but trials were abandoned two years later as a result of excessive interference from signal leakage.

is incomplete or under-developed. Again, whether these would produce adequate return on investment is debatable.

How it works – theory and practice

Two classes of hardware make powerline communication possible. A data concentrator, or 'outdoor device', installed at the neighbourhood substation connects data streams modulated onto the local supply mains with the main telecommunications trunk network.

The mains-voltage distribution network is used to bridge the last mile to consumers' home or offices, where an 'indoor device' or adaptor breaks out the voice and data signals and feeds them by coaxial cable to the user's PC, telephone and other applications.

In general the system is viable only in urban areas; the maximum signal reach is 350 yards. In rural areas the distance between transformer and consumer can be up to half a mile. Carrier frequencies for transmitting this data lie in the region 9kHz to 30MHz – the same part of the spectrum as used for a variety of radio communications.

Currently there is no consensus on technical standards, meaning that systems installed by one vendor may not be compatible with others. Implementation techniques vary too, using either single or multiple frequencies and a variety of spread spectrum and fast frequency hopping techniques with either frequency division or amplitude modulation. Because EMC standards are still under development, commercial roll-out must wait until they are ratified.

The problems start here

Power lines are a harsh environment for data transmission; impulsive noise and voltage spikes from electrical appliances, switching operations and distant lightning strikes can wipe out low-level signals.

NT's 'Digital PowerLine

One example of a system for communicating data over power lines is 'Digital PowerLine'. Developed by Northern Telecom and United Utilities, it is capable of transmitting data at a rate of 1Mbit/s over existing electricity infrastructure.

Through "conditioning" of the existing electricity infrastructure, electrical utilities can transmit regular low-frequency signals at 50 to 60Hz and much higher frequency signals above 1MHz without affecting either signal. The lower-frequency signals carry power, while the higher-frequency signals can transmit data.

Digital PowerLine uses a network, known as a high-frequency conditioned power network, or HFCPN, to transmit data and electrical signals. An HFCPN uses a series of conditioning units to filter those separate signals.

The conditioning unit sends electricity to the outlets in the home and data signals to a communication module or 'service unit'. The service unit provides multiple channels for data, voice, etc.

Base-station servers at local electricity substations connect to the Internet via fibre or broadband coaxial cable. The end result is similar to a neighbourhood local-area network.

The server

The Digital PowerLine base station is a standard rack mountable system designed specifically for current street electricity cabinets. Typically, one street cabinet contains 12 base station units, each capable of communicating over 1 of 40 possible radio channels. These units connect to the public telecommunications network over some broadband service.

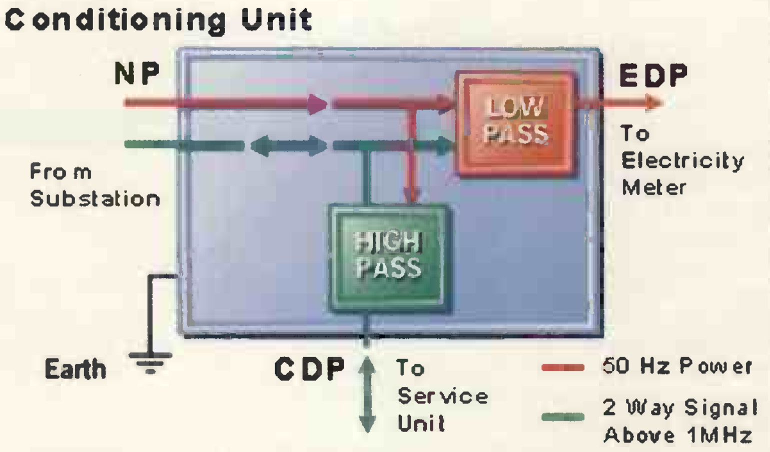
Several options – with different costs – can provide broadband Internet service to each base station. The simplest solution is connecting leased lines to each substation. This solution is potentially quite costly because of the number of lines involved.

A wireless system has also been suggested to connect base stations to the Internet. This option reduces local-loop fees, but increases hardware costs. Another alternative involves running high bandwidth lines, along-side electric lines, to substations. These lines could be fibre, ATM, or broadband coaxial cable. This option avoids local loop fees, but is beset by equipment fees.

The actual deployment of Digital PowerLine will probably involve a mix of these alternatives, optimised for cost efficiency in different areas and with different service providers.

These base stations typically serve approximately 50 customers, providing over 20MHz of usable spectrum to near-end customers and between 6 and 10MHz of useable spectrum to far-end customers.

The server operates via IP to create a LAN type environment for each local service area.



The 'conditioning unit' for the Digital PowerLine network is placed near the electric meter at each customer's home. This unit uses band-pass filters to segregate the electricity and data signals, which facilitate the link between a customer's premise and an electricity substation.

Modulation levels can be increased but then power lines become radiating feeders; radiation from street lamps during trials in Manchester gave rise to concerns over data security as well as fuelling opposition to further pollution of the airwaves. Powerline communications are anathema to broadcasters and listeners – not to mention government, amateur and CB users of the radio spectrum.

Radio Netherlands has warned that interference levels – even to reception of strong domestic signals – will be so high that the whole concept will have to be re-thought. Otherwise many urban dwellers will lose the opportunity to listen to foreign radio stations on AM radio.

The Radio Society of Great Britain has also voiced its concern, noting that German approval for powerline communication systems – strongly opposed by radio users in that country – allow higher levels of emission than those cited in the UK as a 'worst case' for acceptable interference. It concludes there is a European agenda to provide cheap wideband data systems and that the technical arguments for preservation of the HF spectrum appear to be ignored.

However, given the recent success of legal appeals under human rights legislation it is likely that any significant interference to citizens' ability to listen to authorised broadcast stations would be found unconstitutional and would lead to effective action against the 'jammers'.

Unsettled outlook

Powerline communication faces an uncertain future. Superficially attractive, its deployment may turn out to be unviable and technically problematic.

A report from UBS Warburg and the Smith Group argues that it will come so late that it will "miss the boat". By the time that manufacturers have equipment that meets EMC regulations, the roll-out of ADSL will be at an advanced stage. This may be unduly optimistic for ADSL, but only time can tell. ■

2Mbit/s Internet, 24 hours a day...

Oneline – one of the alternatives currently available for sending data over the power lines – allows in-home narrowband and broadband data transmission.

This is a modular system – components can be used on a stand-alone basis or in combination with one another.

Phone services based on the Oneline system are claimed to equal the voice quality of conventional wireline telephone systems. The system is compatible with existing telephony equipment too – even ISDN.

Oneline makes always-on Internet a available, with data transmission rates of up to 2Mbit/s claims the manufacturer.

Incorporating 'intelligent repeater' architecture, the Oneline system uses low signal levels and is said to comply with the tight emission limits likely to be adopted by the German regulatory authorities.

Oneline box in the electricity meter's cabinet. The box is part of the power utility's infrastructure.

Supercaps in the automotive field

Marc Juzkow* looks at how supercapacitors are helping to make cars and other road vehicles safer, more reliable and more efficient.

When designing a car, engineers must toil over the seemingly smallest factors to ensure the safety of the vehicle and its passengers.

Cars are still mostly mechanical in terms of the power linkages throughout the vehicle. These linkages have evolved in recent years though. Door locks, windows, steering and braking are often power assisted nowadays. In addition, there are more complex operations such as air bag deployment, regenerative braking, and a multitude of other features.

However convenient these power-operated features have become, safety remains a prime concern in car design. One major concern is that there is currently no secondary source of power for these operations should the primary battery/alternator source be lost.

Accident power problems

The importance of having a secondary power source may not become apparent until the vehicle is in an accident. In accidents, quite often the battery cable is severed.

If power from the main battery is lost, many functions of the car become inoperable. This issue is causing engineers to design a more reliable method of powering these operations and linkages with a back-up power source at the site of each application.

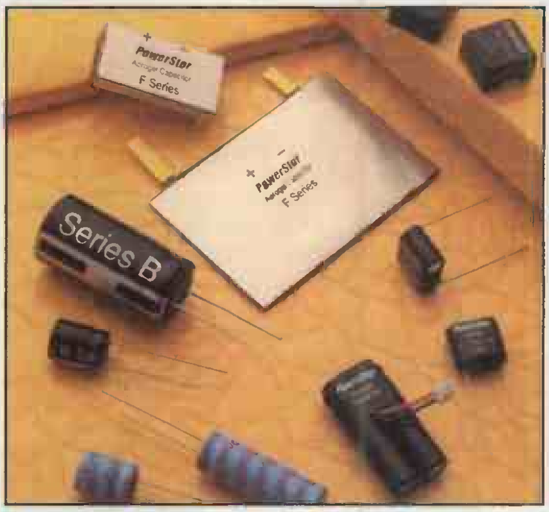
Supercapacitors should not be considered primarily as replacements for electrolytics or tantalum capacitors – although in some cases they may be used as such. Rather, they should be seen as miniature energy sources capable of high current discharges that need to be located close to an electronic or electromechanical device.

As vehicles become more electronic and less mechanical, supercapacitors are being tested as a back-up power source for everything from the high-energy primary battery downwards.

So why is back-up power important?

One application of such a supercapacitor back-up supply actuates solenoids that would release electronically-tensioned seat belts after a car comes to rest following a collision. Most current seat belt systems operate on mechanical linkages and often do not release after the car has come to rest and main power has been lost.

Marc is Marketing Manager with Cooper Electronic Technologies.



These supercapacitors are based on a novel type of carbon foam known as carbon aerogel. Made by Cooper Electronic Technologies, they have 2000 times the volumetric capacitance of standard aluminium electrolytic capacitors combined with equivalent series resistances ranging from tens to hundreds of milliohms depending on type. Values range from 1F up to 50F and low leakage currents mean that the devices can hold their charge for several weeks. A further feature is a very high charge-discharge cycle life – virtually infinite when compared to batteries.

Furthermore, a driver or passenger may want to send out a distress signal after an accident has occurred. This signal could be sent via radio to a navigation operator. A GPS receiving unit that could provide the disabled vehicle's location could be activated simultaneously.

Each of these electronic devices would have its own 'supercapacitor energised power supply' that would ensure that the related function remains operational even if the main power source is lost.

Another safety concern is emergency or hazard lighting. Implementation of a supercapacitor as a secondary power source would eliminate hazard light failure due to an electrical or battery failure.

To avoid possible combustion following an accident, a solenoid closing the gas line near to the fuel tank could be controlled by a roll-over detector – again powered by a supercapacitor located within the same module.

Green issues

Environmental concerns are also addressed through the use of supercapacitors. In each car battery, there are several pounds of lead, which is known to be a toxic element in our environment.

In contrast, the main component in a supercapacitor is carbon, which is a much more benign element. It is highly possible that future cars will contain a much smaller lead-acid battery and many lightweight supercapacitors that are located in various places around the vehicle and designed specifically to drive a particular device.

Passengers may also need to activate electric door locks to unlock the doors, or run motors to wind down the windows after an accident, but only after the vehicle comes to a complete rest. If the initial battery source is lost, supercapacitors could act as a back-up power source, storing enough power to operate the locks for a few cycles in such an event.

With a supercapacitor providing secondary energy storage, passengers would be able to escape from such electronically-controlled vehicles safely in the event of main power loss.

Though all of these issues are important safety concerns, the most obvious use of supercapacitors is for firing the squibs that open vehicle air bags.

Current technology requires a higher voltage squib. Individual supercapacitors are generally rated at 2.5 volts, but they possess high surge current capabilities of tens of amps. The capacitors used for air bag deployment are typically a combination of tantalum and electrolytics. Supercapacitors would allow cost savings and miniaturisation, as well as very close placement to the squibs.

Supercaps in non-safety-critical applications

In non-safety related areas, supercapacitors could provide the initial surge current necessary to start a motor under high load, such as in power seats. This would allow designers to use a fuse rated at the running current of the motor, as opposed to the in-rush current.

Furthermore, it would allow the designer to reduce the wire size used to connect the main battery to the different points in the vehicle that need power. This would result in significant savings and weight reduction. Heavier wires would only be needed for the very short distance from the local supercapacitors to their associated electric devices. Theoretically, the designer could also use supercapacitors to preheat the headlight filaments and enjoy similar cost and weight reduction benefits.

In addition, replacing mechanical operations with supercapacitors and electronic linkages will bring cost savings. Making simpler door mechanisms through the implementation of a single solenoid will reduce component count and assembly costs.

Car makers may also consider placing a supercapacitor power source close to a microcontroller that records all vehicle data in the event of a collision. For example, a car manufacturer may want to know exactly what the individual tyre pressures and temperatures were before, during and after an accident involving a blown tyre.

Even if the battery cable were severed, a supercapacitor-supplied power source located in the same module as the microcontroller could capture and store the data if primary power was lost.

Several car-industry giants are already testing supercapacitors for use as distributed power sources for small-scale vehicular operations. Car industry experts anticipate supercapacitors first being employed in distributed power applications as early as the 2003 model year.

Large-scale supercapacitors are even being evaluated in automotive power hybrid configurations. Here a supercapacitor and a battery are connected in parallel, the characteristics of each storage medium complementing the other.

Electric hybrid vehicles

Supercapacitors are being assessed for use in hybrid electric vehicles – or HEVs. Such vehicles have an internal-combustion engine and a battery working together to propel the car.

Many leading car makers are selling increasing numbers of HEVs. They are more efficient than a standard car because only the battery is used when the vehicle is stopped and during acceleration to a cruising speed before the engine starts.

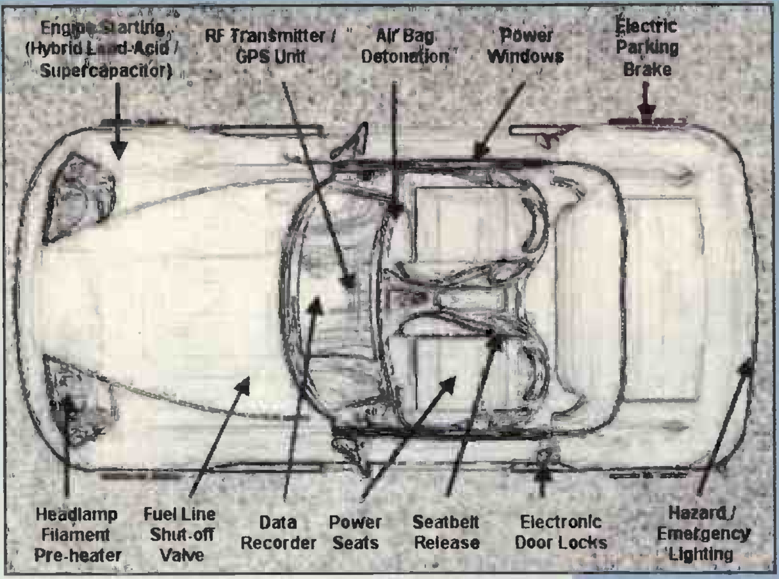
At cruising speed, a generator creates electricity to charge the battery and power the car. Running the combustion engine at a constant speed also works towards increasing efficiency.

In an HEV, a substantial amount of energy can be recovered during braking. When the brakes are applied, the braking energy is translated to electrical energy. However, the battery must be able to accept a fast, high-current charge.

Lead acid batteries, in particular, cannot handle such a quick charge. A supercapacitor and lead-acid battery working together in parallel accomplish effective regenerative braking.

Supercapacitors are also useful when a particular device has to operate frequently because they can be discharged and charged hundreds of thousands of times. A battery has a life expectancy of a few years before it loses its ability to recharge.

Though each of these elements is instrumental in achieving maximum power, energy storage and cost efficiency, the most important factor is safety. The implementation of supercapacitors in the manufacturing of cars will increase the safety features of the vehicles. It will do this by allowing designers to move away from costly, inefficient mechanical systems to electronic systems that offer the end-customer a wide variety of new features to enhance their driving experience. ■



If you thought that supercapacitors were only useful for memory back-up, think again. In the automotive field, they're even being considered for use alongside the main battery to boost its surge delivery capability and give better starting in cold weather. This illustration maps out some of the points where supercapacitors could be used in a distributed fashion to provide safety back-up and reduce motor start-up strains on the car's harness.

Supercapacitor applications in other vehicles

Within the automotive industry, but outside the realm of traditional passenger roadway vehicles, supercapacitors can be used for traction and engine ignition in golf carts, jet skis, wheelchairs, etc.

For example, battery-powered wheelchairs may have a supercapacitor to assist in acceleration and to increase power capability. Often, high-power supercapacitors are placed in parallel with a high-energy battery, forming a high-energy, high-power source to increase traction.

Industrial and recreational vehicles, including jet skis and snowmobiles, can utilise supercapacitors in an engine starting capacity. Many of these vehicles are often used in cold temperatures where traditional lead acid batteries do not operate well.

Furthermore, when lead acid batteries are not fully charged, their pulse power capability is reduced. In lower temperature environments, placing a supercapacitor in parallel with the battery makes ignition easier and adds power to the vehicle. As a result, designers can implement a smaller starting battery that operates more reliably at lower temperatures, conserving both cost and space.

Analyse your SDI

Emil Vladkov has designed a versatile test-pattern generator *and* receiver for the serial digital video standard SDI.

So what is SDI? The serial digital interface SDI was born to serve the transmission of digital video over existing infrastructure – usually comprising 75Ω cable.

The idea was to allow the move from analogue to digital video without the need to change kilometres of precision coaxial cable in the studios. Using SDI moves the modifications needed for the changeover to the equipment level – which has lower cost impact than altering the cabling.

As the name suggests, the digitised video in parallel form – usually to 10bits – is moved across the medium in serial form. The need for providing high picture quality of the picture means that bit rates for SDI are high, as you can see from **Table 1**.

The transmission medium for SDI signals is usually Belden 8281 75Ω coaxial cable. With modern chip sets – like the CLC0xx chip set from National Semiconductor – the signal can travel distances of up to 300m on such coaxial cable.

The serial digital interface can also be used with twisted-pair cables for shorter distances and with optical fibre cables for critical applications. The standard signal level is set to 800mV pk-pk.

The serial digital interface is well defined in many standards of the Society of Motion Picture and Television Engineers, or SMPTE. Because the high bit rates the SDI links can be used in the future for telecommunication purposes, the main SMPTE-standards have analogues as ITU-standards. This extends in general the scope and application possibilities of this article, and the device proposed within it, beyond the pure digital-video industry.

The most important standard is the ANSI/SMPTE 259M standard, defined as: 10-bit 4:2:2 Component and 4fsc Composite Digital Signals – Serial Digital Interface. This standard covers the standard-definition serial digital video with bit rates from 270 to 360Mbit/s.

For the bit-parallel digital interface – which has to be serialised to become SDI – the corresponding standard for the standard aspect ratio is ANSI/SMPTE 125M . This standard becomes ANSI/SMPTE 267M for 16:9 aspect ratio.

Standard SMPTE 259M covers standard definition video while SMPTE 292M deals with high-definition video, providing bit rates of 1.485Gbit/s. This article deals with standard definition, so the bit rates are limited to 360Mbit/s.

Of course there are many accompanying standards covering the transmission of ancillary data such as SMPTE 291M: Ancillary Data Packet and Space Formatting. There is also a standard for Error Detection and Handling (EDH), namely SMPTE RP 165: Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television).

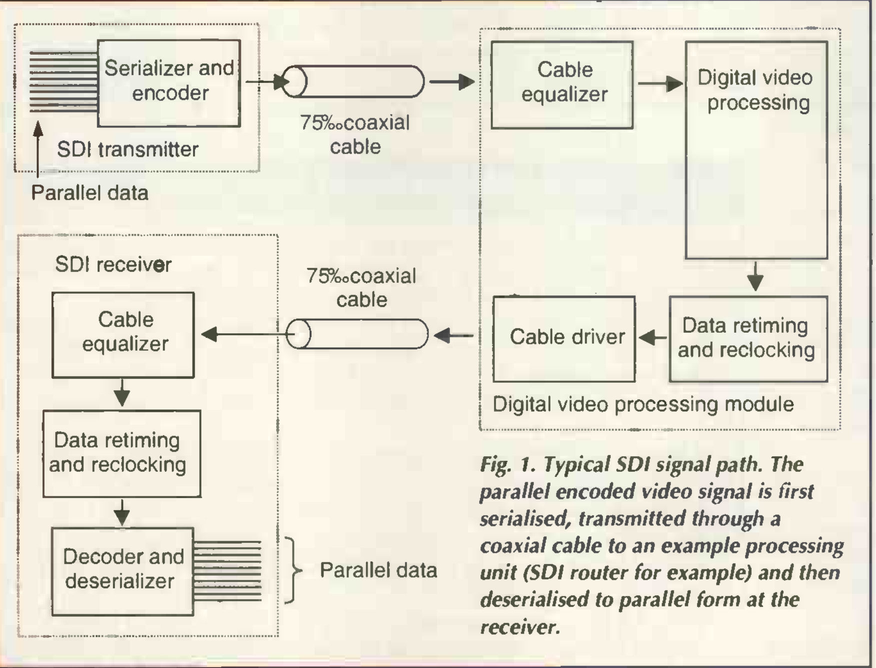
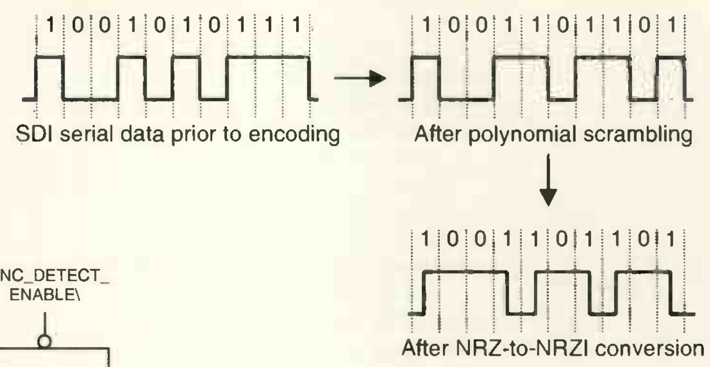


Fig. 1. Typical SDI signal path. The parallel encoded video signal is first serialised, transmitted through a coaxial cable to an example processing unit (SDI router for example) and then deserialised to parallel form at the receiver.

Fig. 2. Basic serial data stream signal shapes. After serialisation, the signal is scrambled with a polynomial generator and then converted from NRZ (non-return-to-zero) to NRZI (NRZ inverted). The last step makes the SDI-signal and its inverted version SDI\ equal, as '1' are coded with transitions and transitions remain transitions after inversion. So the video processing equipment can manipulate the polarity of the SDI stream without affecting the content.



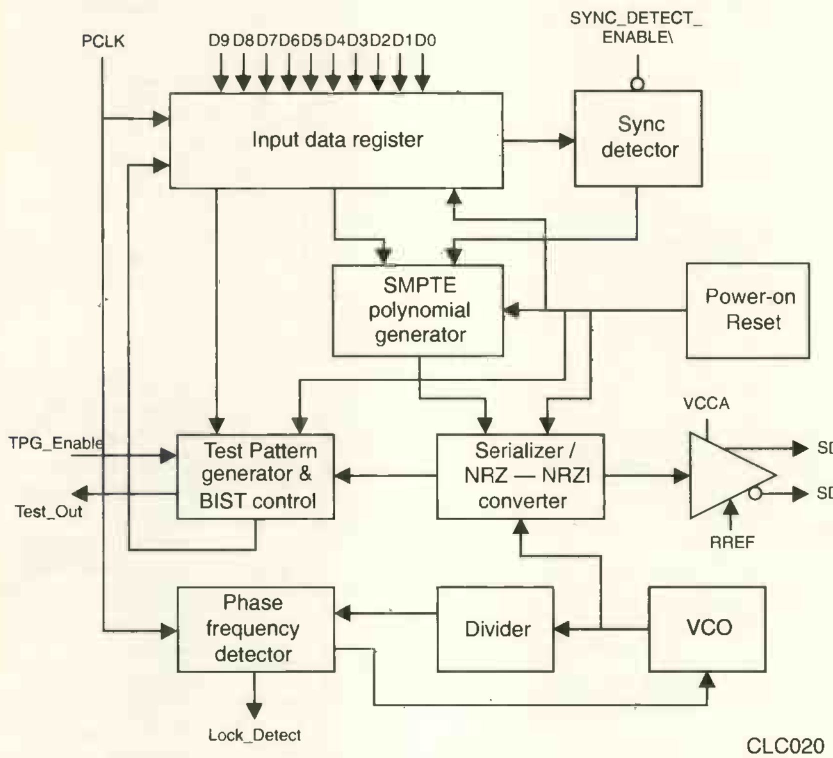


Fig. 3. Block diagram of National's CLC020 SMPTE 259M digital video serialiser with integrated cable driver. The chip performs all functions associated with the parallel to serial conversion and serial bit-stream encoding. It can directly interface a 75Ω coaxial cable.

When designing devices for SDI – especially test devices – it is best to conform to all prescribed standards. This is easy to do if standard chip-sets are used, such as the CLC-chip set of National Semiconductor, because the chips already conform to the standards.

A typical SDI-signal path is presented on **Fig. 1**. First the signal is transformed from parallel to serial and encoded, then the SDI signal is transmitted over coaxial cable. The digital video-processing module performs various operations on the digitised serial video, including routeing. It receives the serial signal through a cable equaliser, which compensates for cable losses.

Output serial data is retimed and reclocked to remove jitter and then fed into a cable driver. In the receiver subsystem, the signal is first equalised for cable losses. After retiming and reclocking it is decoded and deserialised to obtain the parallel representation again.

Next I will briefly explain the functions of the main blocks in the diagram in Fig. 1. Two of them – the serialiser and the receiver – are parts of the SDIT270 test pattern generator and receiver, which is the subject of this article.

Serialiser and encoder

Usually the main functions provided by this unit are:

- Parallel data to serial data stream conversion;
- SMPTE polynomial data encoding, according to the polynomial expression $1+X^4+X^9$: this conversion is necessary to provide the data with more noise-like appearance, suppressing strong spectral components. This means practically randomising the data, breaking long runs of '1' and '0';
- NRZ-to-NRZI data-format conversion: The purpose of this conversion is also to break long '1' and '0' runs, thus minimising DC spectral components. This is especially useful for data and clock recovery, where the PLL recovery circuits have to be synchronised with transitions. An example of a data serialisation and encoding with NRZ-to-NRZI conversion is presented[7] in **Fig. 2**. As is evident from the figure, '1's are encoded in the NRZI-stream as transitions between the two logical levels;
- Coaxial cable driving: this is accomplished by an integrated cable driver, which AC-couples the typical SDI ECL (or PECL) levels into back-matched 75Ω coaxial cable.

I was pleased to discover that all the above mentioned functions are integrated in a single chip – National

Table 1

Data rates for the different resolution TV standards.

Digital video resolution	Bit rate of SDI
Standard definition TV (SDTV)	270Mbit/s
Wide screen standard definition TV	360Mbit/s
High definition TV (HDTV)	1.485Gbit/s

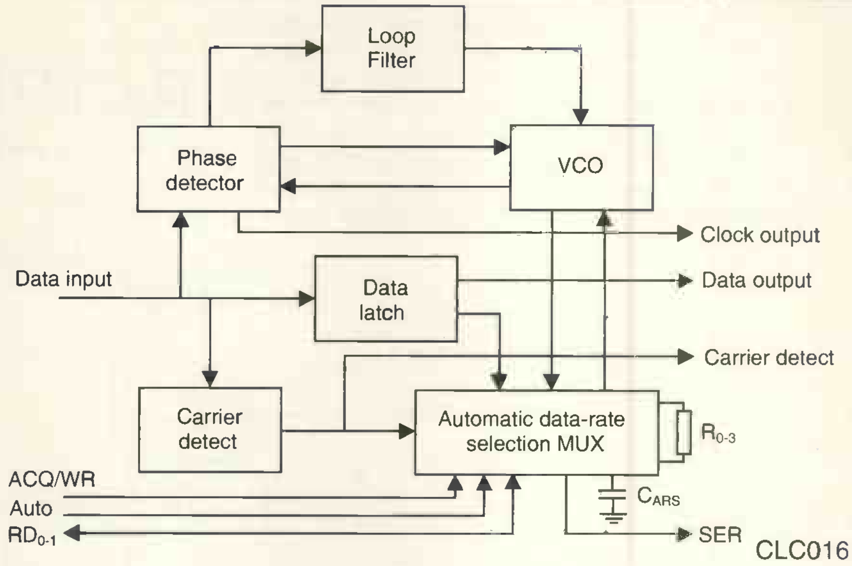


Fig. 4. Block diagram of the National's CLC016 data-retiming PLL with automatic data rate selection. This device performs all functions associated with the serial data retiming/reclock and extracts a clock signal from the bit-stream. The clock signal is necessary for the deserialiser CLC011. The retimer can lock to different standard preset data rates.

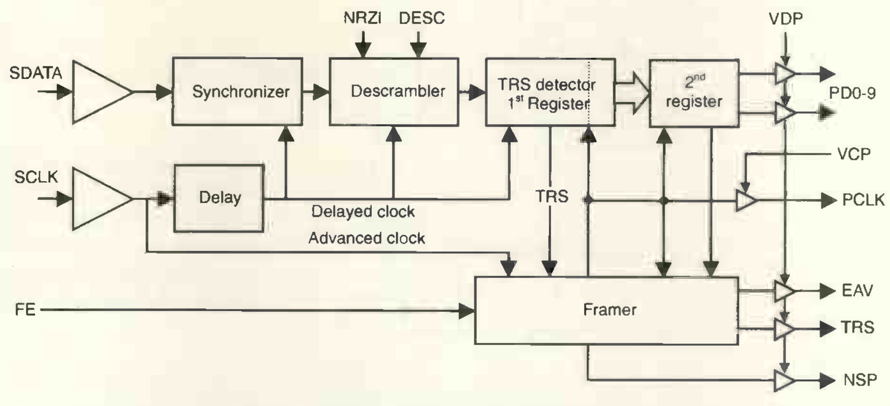


Fig. 5. Block diagram of the National's CLC011 Serial Video Decoder. The device unscrambles the serial bit-stream and converts it to parallel 10-bit words. It has many logical output signals, which are used in implementation to indicate if the SDI-signal is standard or corrupted.

Semiconductor's CLC020 chip. The block diagram of these useful devices is presented[4] in **Fig. 3**.

To provide a serial output data stream at 270Mbit/s at the differential outputs SDO and SDO\, an external clock signal is needed at the PCLK input. The 10-bit parallel data is applied to ports D0–D9.

By enabling the SYNC_DETECT_ENABLE\ the polynomial generator recognises the timing sync. words in the data streams:

Timing reference signal, TRS
Start of active video, SAV
End of active video, EAV

The circuit has built-in self-test (BIST) and a pass/fail signal is presented on port 'Test_Out'. After the internal VCO running at 10 times the parallel clock frequency has locked to the PCLK, an active high Lock_Detect output is provided.

There is an additional feature of the chip that I make extensive use of in my design – the integrated video test pattern generator, or TPG. It provides four component test patterns – reference black, PLL pathological, equaliser pathological and 75% colour bars. All test patterns are available in PAL and NTSC formats, so the generator presented is multi-standard.

Why use pathological patterns? The purpose of the pathological data patterns is to stress digital video processing systems, so that they perform in a margin situation, which will not normally occur in a standard video signal.

The pathological check fields are specified in SMPTE RP 178, where RP represents Recommended Practice[2]. The equaliser pathological test signal consists of a '1', followed by 19 '0's. This stream has a strong DC-component, making the work of a practical equalising circuit a difficult task.

The PLL-pathological signal consists of a sequence of '1's and '0's, repeated every 20 cycles, thus having a minimum of crossings. This makes the work of the clock-extracting PLL difficult.

Providing such useful testing pattern in an instrument like the SDIT270 makes it a must for every TV studio or cable provider dealing with digital video distribution and processing.

Receiver – deserialiser and clock recovery

As the serial data travels through the cabling and the digital-video processing systems, its jitter usually increases and the duty-cycle ratio is distorted. For this reason, in every SDI receiver – every good one that is – special care is taken to restore the correct transitions in the data stream. This is usually done by the so-called data reclock/retimer.

As an additional feature, the reclock /retimer unit produces – i.e. extracts from the data stream – the clock information, for use by the following deserialiser.

The retimer/reclock chip in National Semiconductor's chip set is the CLC016. As depicted in **Fig. 4**, the circuit[1,5] consists of a PLL-structure with a VCO, phase detector and a loop filter, which extracts the clock information from the serial data input.

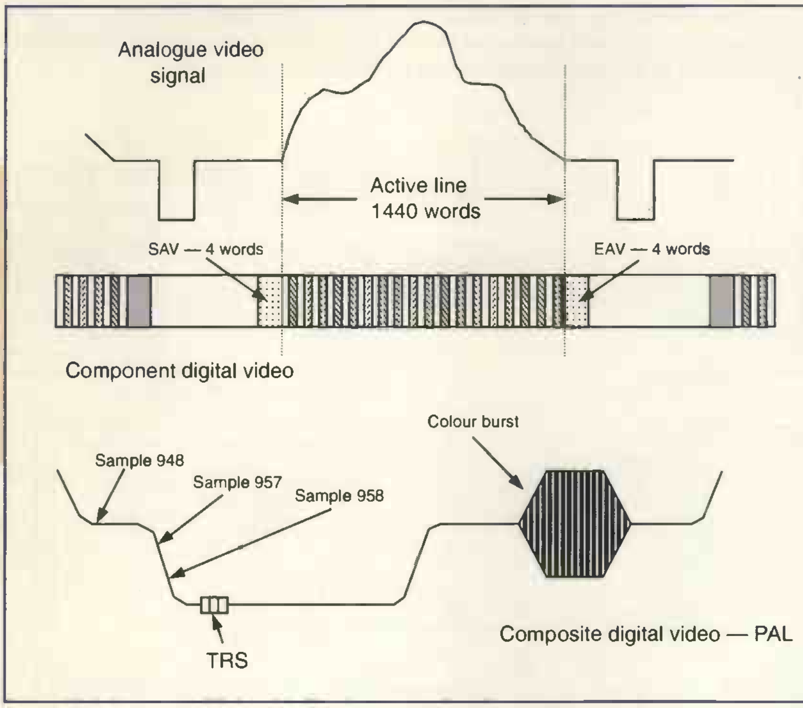


Fig. 6. Digital representation of the analogue video baseband signals – both composite and component. The most important sync. information embedded in the serial digital interface are the timing reference signal, or TRS, words. Additional timing information in the form of 'start of active video' SAV and 'end of active video', EAV, is available in the component format only. The actual 270Mbit/s data stream is component form.

Automatic data rate selection is provided by this unit, so that the PLL can lock on four different data rates. These are usually the data rates specified in the standards – 143, 177, 270 and 360Mbit/s. The data rates are defined by resistors $R_{0\text{-}3}$. The user can manually select data rates through the RD0-1 inputs/outputs, or be provided with logical indications of which data rate is currently selected.

The circuit has differential PECL open-collector outputs for both retimed data and extracted clock. An additional carrier detect/mute feature is very useful as when no valid data is presented on the input ports the outputs are automatically latched to prevent random transitions, which can stress the subsequent circuits.

The deserialiser performs the conversion of the serial encoded data into 10-bit parallel words with the word-rate clock. In the case of 270Mbit/s the word-rate clock is 27MHz. The chip that performs these functions, is the CLC011; it is also referred as SDV-decoder[6]. Its internals are shown in **Fig. 5**.

As is obvious from the diagram, the chip needs not only the serial retimed data SDATA, but also the extracted serial clock SCLK. This makes the use of the previously described CLC016 mandatory.

Parallel data on PD0-9 and the parallel word-rate clock PCLK have independent power supplies, namely VDP and VCP. This is done to provide flexibility in connecting to different logic families.

The NRZI-to-NRS reverse conversion and the polynomial descrambling can be switched off by means of the NRZI and DESC ports, providing additional flexibility in using the device. The CLC011 has many additional features, which I have used in the SDIT270 to perform error checking on the input serial data stream of the receiver.

The framer can be enabled by the FE port to resynchronise on the next timing reference signal – equivalent to horizontal sync pulse. From the serial data stream the TRS sync and the EAV end-of-active-video information is extracted and provided on ports TRS and EAV. I have used the TRS to monitor the sync pulses and as an indication that a valid video signal is presented on the receivers input.

A very useful signal is NSP – or new sync position. An active high appears on this pin if an alignment error in the

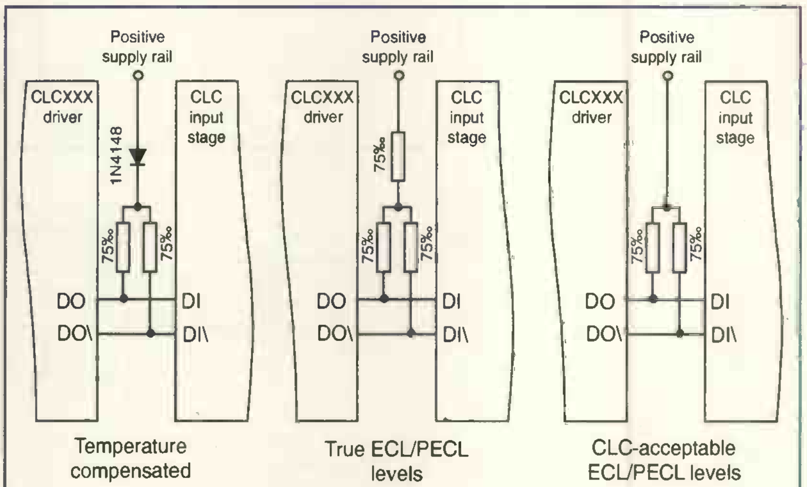


Fig. 7. Various types of PECL-outputs interfacing for the CLC-chip set. Output drivers of the CLC-chips are current-mode drivers. The 75Ω resistors are level-setting and terminating resistors at the same time.

TRS sequence is detected, i.e. if the TRS signal appears earlier or later than normal in the video sequence.

As the new terminology I have used in conjunction with the CLC011 and the other chips may be unfamiliar to many analogue video engineers, I have provided an

Circuit boards and kits for the generator

Circuit boards can be obtained from *Electronics World* for £38 all inclusive. These are double-sided boards with solder mask and component placement markings. Send a cheque made out to Cumulus Business Media to SDI PCBs, Electronics World, Anne Boleyn House, 9-13 Ewell Road, Cheam, Surrey SM3 8BZ together with your address. If possible please include a phone number – preferably a daytime one. You can also fax your credit card details and card-holder address 01782 878 233 (+441782 878 233). Depending on demand, we may have to have the boards produced as they are requested so please be patient. If you are interested in kits or ready-built end product, please send an SAE marked "SDI details please" to the address above.

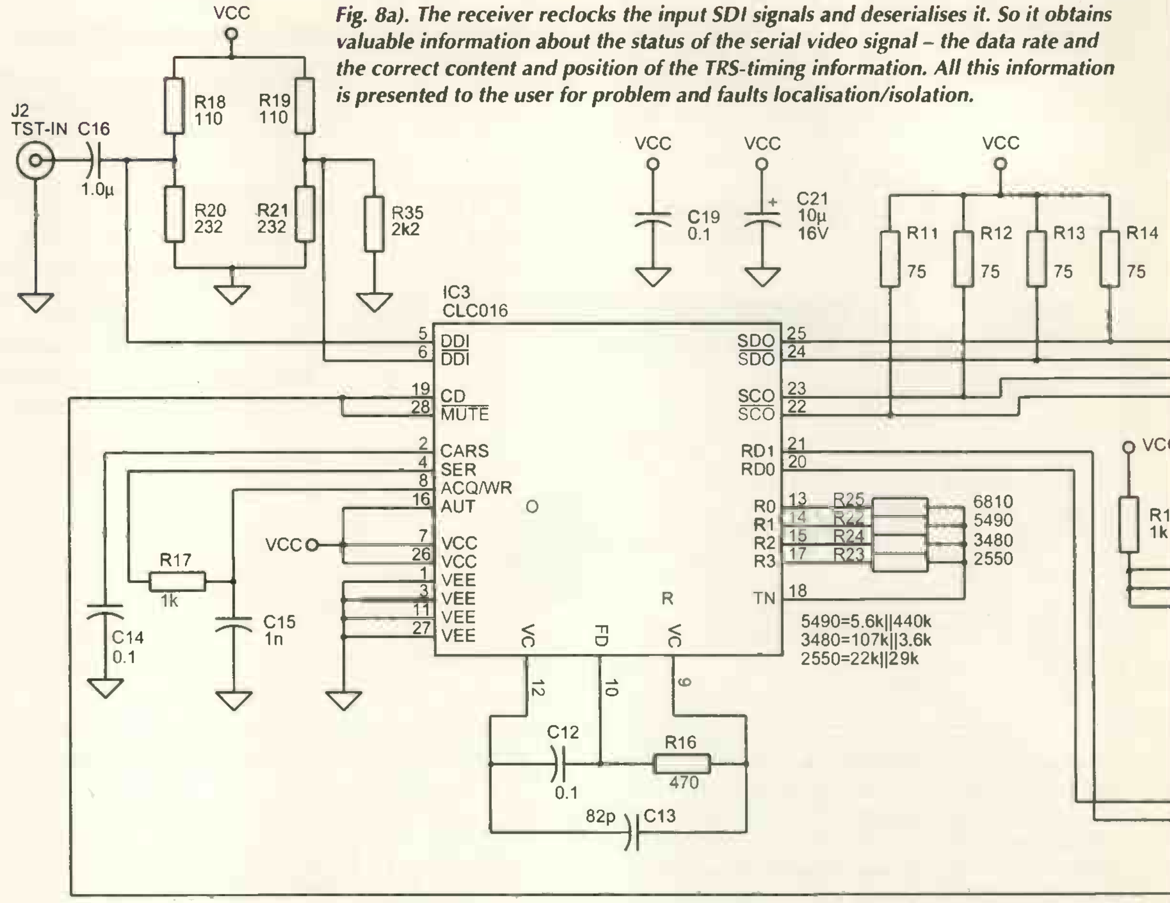


Fig. 8a). The receiver reclocks the input SDI signals and deserialises it. So it obtains valuable information about the status of the serial video signal – the data rate and the correct content and position of the TRS-timing information. All this information is presented to the user for problem and faults localisation/isolation.

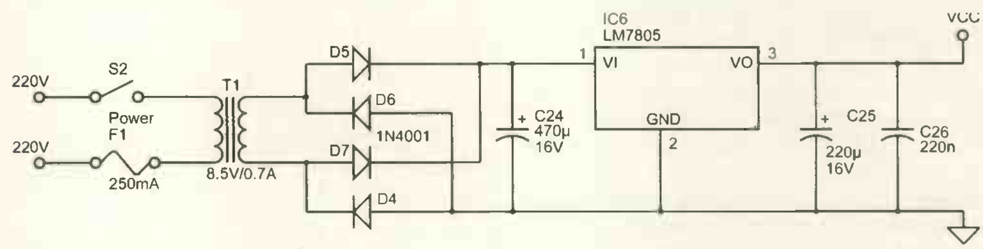


Fig. 8b). Power supply. This is a simple linear power supply. Switched mode power supply can be used with proper filtering provided to reduce the switching noise. Provide an adequate heatsink, as many of the CLC-devices are power hungry – remember – they work at 270Mbit/s and above!

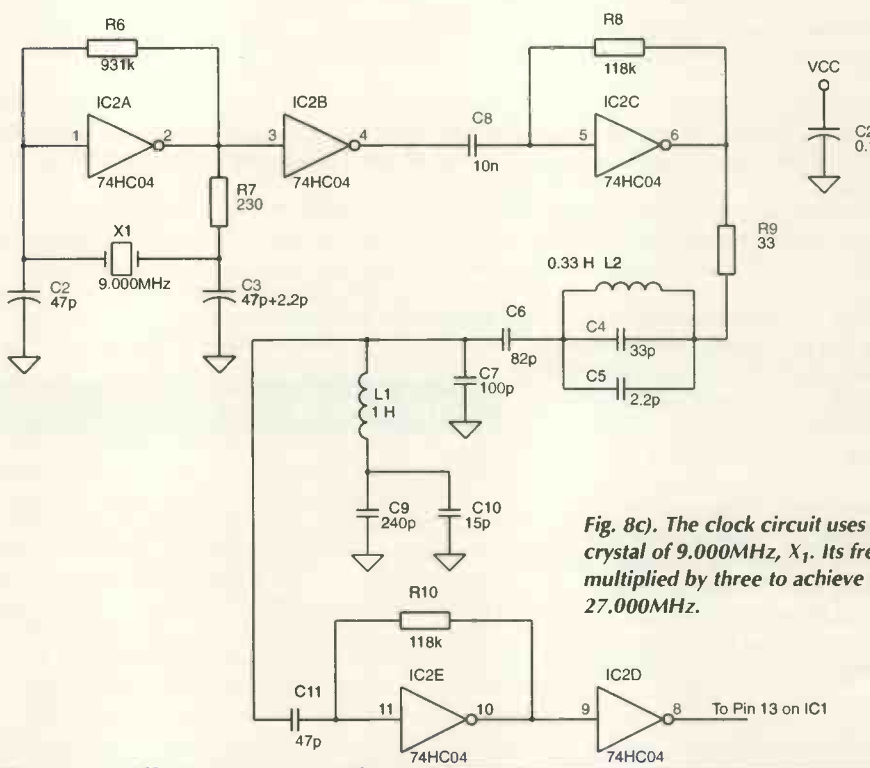
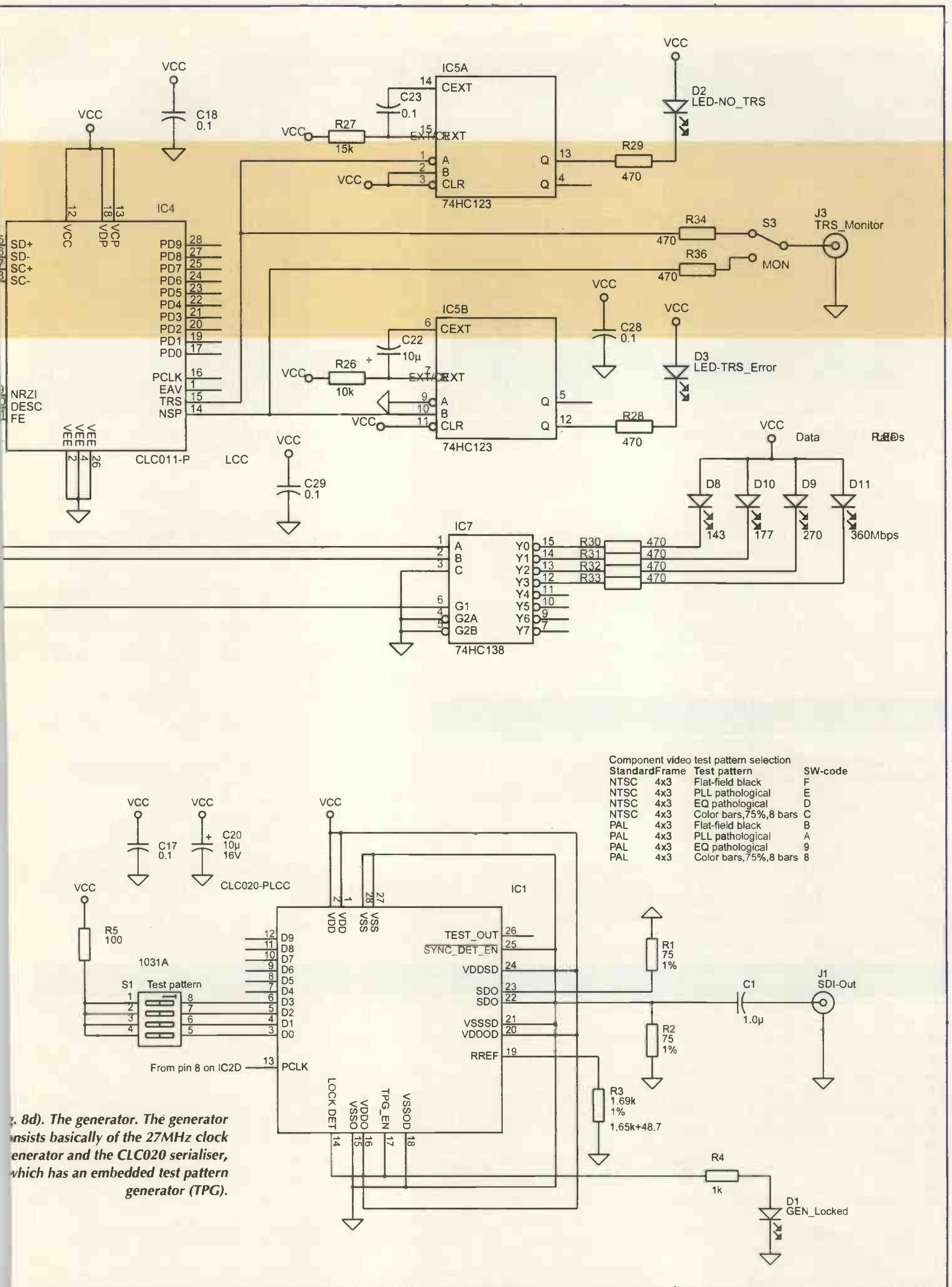


Fig. 8c). The clock circuit uses a selected crystal of 9.000MHz, X_1. Its frequency is multiplied by three to achieve the 27.000MHz.



…8d). The generator. The generator …nsists basically of the 27MHz clock …enerator and the CLC020 serialiser, …which has an embedded test pattern generator (TPG).

Fig. 9. Front View of the SDIT270 SDI generator and receiver. The device is housed in a plastic copper-shielded box.

Fig. 10. General view of the SDIT270 device. The position switch, which controls the output test pattern, is on the device's side panel.

elementary comparison between analogue – i.e. component – video and parallel digital data stream according[7] to ITU R.601 in Fig. 6. From the figure, the location of the SAV and EAV words is evident, but it should be mentioned that these are available only for component signals.

For composite signals only, TRS is available. The position of the three TRS words is also pinpointed in Fig. 6 for composite video. The three reserved TRS words are, in 10-bit systems, $3FF_{16}$, 000_{16}, 000_{16}.

Table 2

Switch positions for the different test patterns and video standards.

Switch code	Standard	Frame	Test pattern
8	PAL	4x3	Colour bars, 75%, 8 bars
9	PAL	4x3	Equaliser pathological
A	PAL	4x3	PLL pathological
B	PAL	4x3	Flat-field black
C	NTSC	4x3	Colour bars, 75%, 8 bars
D	NTSC	4x3	Equaliser pathological
E	NTSC	4x3	PLL pathological
F	NTSC	4x3	Flat-field black

More about logic level and terminators

As SDI is a high-speed data link the interface circuitry is usually implemented in emitter-coupled logic, or ECL, technology.

Today, most electronic systems run on a single supply, so providing a negative supply rail to support traditional ECL is unsuitable. As a result, another logic level scheme is implemented – PECL, which stands for positive ECL. The whole chip set used in this design is based on PECL interfacing.

The output drivers of the CLC chips are differential current sources. They use an external resistor to establish the correct voltage levels, but the same resistor also serves as back-matching termination.

Three different interfaces can be implemented between the ICs of the chip set, as shown in **Fig. 7**. These interfaces for the connection between the CLC016 data retimer and the CLC011 deserialiser in the receiver subsection are interesting. If a 1N4148 diode is used the output swing will have the similar temperature coefficient as 10K ECL. For the commercial temperature range, the diode can be replaced by a 75Ω resistor to set the correct level for VOH, the high logic level.

As many of the ICs of the CLC chip set do not require true ECL levels to operate correctly, the simplified

Features of the SDIT270 SDI test set

- 4:2:2 component test signal at 270 Mbit/s;
- Test signal 1: Full Field 75% Colour Bars (EBU Bars in 625/50, Colour Bars in 525/60);
- Test signal 2: Flat Field, Black – PAL and NTSC;
- Test signal 3: SDI pathological – EQ pathological, according to SMPTE RP178, PAL and NTSC;
- Test signal 4: SDI pathological – PLL pathological, according to SMPTE RP178, PAL and NTSC;
- Visual indication of the test pattern generator operation – PLL lock indicator;
- PLL receiver locks at four different data rates – 143, 177, 270 and 360 Mbit/s;
- Visual indication of the receiver signal data rate;
- No_TRS (missing timing reference signal) error check – "No valid digital video" indication;
- TRS_Error (new sync position of the TRS) error check – sync alignment error indication;
- Monitor output for sync. pulse observation or error counting;

The front panel view of the SDIT270 is presented on Fig. 9. A general view of the device is shown in Fig. 10 and the internal view of the authors PCB in Fig. 11 and 12.

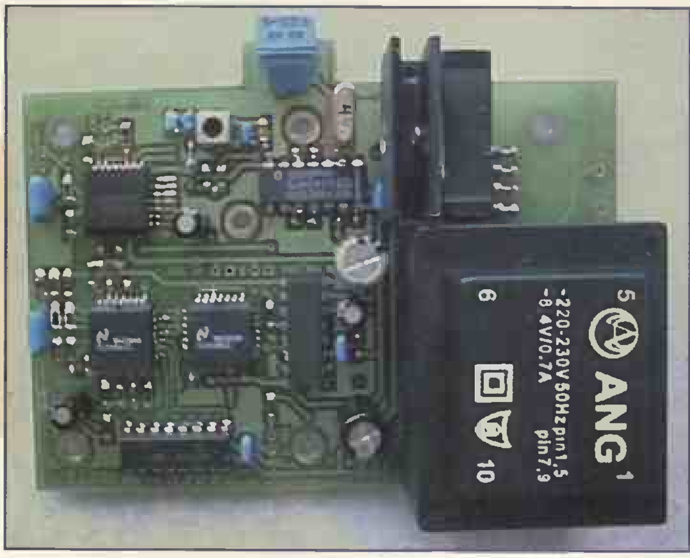


Fig. 11. The PCB of the SDIT270. Most of the components are surface mount, so some experience with soldering such devices is necessary.

Fig. 12. A second view of the internals of the SDIT270. The mains power supply is integrated into the unit, but you can easily adapt the design to use an external wall-mounted adapter.

structure can be used. This involves load terminating resistors connected directly to the positive supply rail.

The SDI-generator

I call this generator the SDIT270. It consists of two main independent parts – the SDI generator and the the SDI receiver. The generator produces standard video test patterns for both NTSC and PAL, i.e. component digital. The receiver can retime, reclock and decode bit rates from 143 to 360Mbit/s. The complete schematic diagram is shown in **Fig. 8**.

The test pattern generator is an embedded function of the CLC020, IC_1. For this purpose I have tied together the LOCK_DET output (14), which indicates that the internal PLL has locked to the external parallel clock, and the TPG_EN input (17), which enables the test pattern generator.

Visual indication that the internal PLL-based serial bit rate clock generator has achieved locking to the external clock is provided by the GEN_Locked LED, D_1. The same LED can be used to indicate that power is applied to the device as in normal operation it is always lit.

Output levels are controlled by the precision 1% resistor R_3 with its typical value shown. The CLC020 does not require serial back-matching resistors, but 75Ω back-matching resistors shown, R_1 and R_2, are shown connected to the SDO and the SDO\ outputs.

Capacitor C_1 couples the SDI output into the coaxial cable. As the CLC020 is not a dedicated TP generator but an encoder – i.e. serialiser and scrambler – it has ten data inputs for the input data to be serialised. Only the first four inputs $D_{0\text{-}3}$ are used to set the desired test pattern: all other data bits should be zero.

As all data inputs have an internal pull-down device only the bits $D_{0\text{-}3}$ that are '1' have to be pulled high. This is done by a Copal S-1031A coder, represented here by the switch S_1 with the pull-up resistor R_5 connected to the common pin of the coder. The possible test patterns with the corresponding standard, frame and coder switch position are listed in **Table 2**.

The CLC020 needs an external parallel data clock that is internally multiplied by 10 to obtain the serial data rate. For 270Mbit/s the external clock should be 27.000MHz. There are such crystal frequencies commercially available, but I had trouble finding one, apart from clock modules.

As it turned out later, not being able to get hold of a crystal was an advantage. Commercial generators are usually computer grade, which means that they are not very stable or accurate.

The SDI standard relies on the reclocking mechanisms embedded in every device that has an SDI-input, so no great clock accuracy is needed. However, the commercially available digital component test signal generators – such as Leader's LT425D – provide relatively great frequency accuracy – in the case mentioned, ±13.5Hz or 0.5 ppm.

I chose to achieve a comparable or better accuracy. The design incorporates a precise quartz generator with a selected – or in my case custom made – crystal of 9.000MHz, X_1. Its frequency is multiplied by three to achieve the 27.000MHz.

To provide a better stability (in time and temperature) I have used the heat generated by the on-board three-terminal regulator to build a sort of an oven. So the result was an ovened crystal stabilised generator with a better than ±10Hz accuracy.

So how does the 3× multiplier work? How good it is that there is a magazine like *Electronics World* around. In the February 2001 issue there's circuit idea working in the nearly the same frequency range[3]. This idea is implemented in my design by the use of a single 74HC04 IC.

Gate IC_{2A} with R_6, R_7, X_1, C_2 and C_3 forms the quartz oscillator, which is buffered by IC_{2B}. You'll need to adjust the values for the capacitors that make up C_3 carefully as they determine the quartz mode of operation and hence the frequency accuracy: values shown are for my design.

First a trimmer capacitor should be used to obtain 9.000000MHz – or as near as possible to that value – as measured with a precise frequency counter. Then, according to the value of the trimmer, the corresponding fixed value capacitors should be used as replacements.

Whatever method you are using, don't forget that the SDI frequency accuracy depends on this generator. The IC_{2C}, IC_{2D} and IC_{2E} with corresponding components $R_{8\text{-}10}$, $C_{4\text{-}11}$, L_1 and L_2, form the frequency tripler, described in detail in the above mentioned circuit idea. This 27.000000MHz ±10Hz clock is used as parallel word-rate

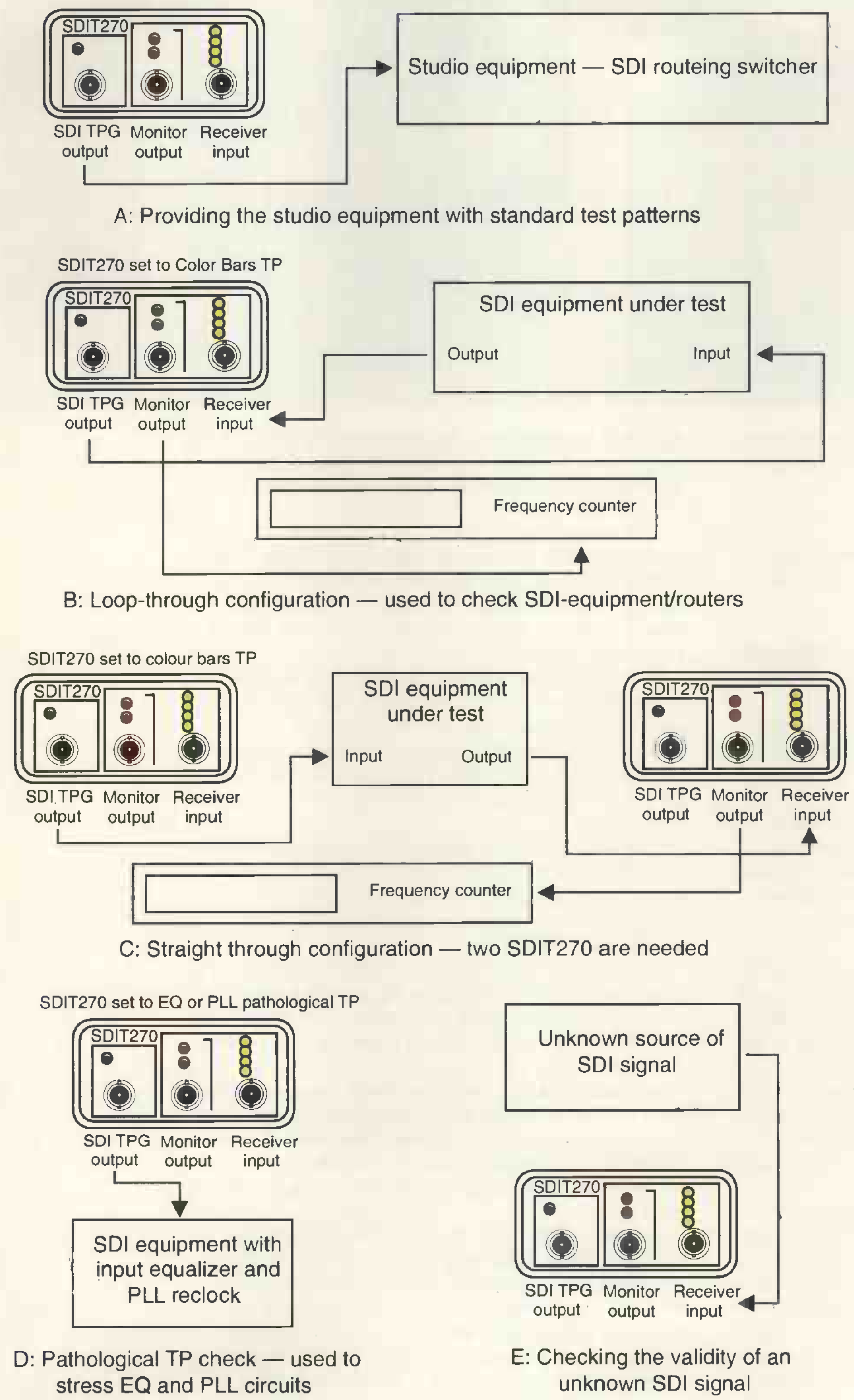


Fig. 13. What is the generator useful for? This diagram answers this question while giving you an idea of five most commonly used test and measurement configurations. As the unit has not only the test pattern generator, but also the receiver built-in, it proves to be useful in typical loop-through tests. In non-loop-through configurations the unit can be used as a classical studio test pattern generator or to analyse unknown digital video signal sources.

clock at pin 13 (PCLK) of the serialiser, IC_1.

The SDI-output is available on BNC connector J_1. The standard specifies BNC connectors for use with SDI signals.

Test receiver details

The SDI-receiver should receive, reclock, descramble and deserialise the input SDI signal – which is not necessarily from the SDI generator of the same unit. It should supply the user with additional information about how the signal was processed in terms of quality. If there is a problem with the signal or the equipment that generated it, this problem should become apparent here.

The receiver consists of the CLC016 retimer/reclock circuit IC_3 and the CLC011 digital video decoder IC_4 together with supporting circuitry. Input SDI signal at J_2 is AC-coupled through C_{16} to $R_{18\text{-}21}$ network (with R_{35} for noise immunity). This network matches the differential input of the CLC016 retimer.

'Automatic' PLL frequency selection is implemented on the CLC016. This means that the device sweeps through the four preset frequencies until it finds one that matches the input. For this purpose the AUTO input, pin 16, is tied to V_{CC}.

When the VCO has not matched the input data rate, the SER output, pin 4, goes high and enables the internal 2-bit counter and the associated automatic rate selection oscillator at ACQ/WR on pin 8 through the R_{17}/C_{15} network. The oscillator period is the period with which the device cycles through the available PLL frequencies. It is determined by capacitor C_{14}. When the VCO latches to the external data rate, SER goes low and the automatic search is over.

As the automatic data rate selection circuitry cycles through available bit rates outputs, RD0-1 on pins 20 and 21 reflect the changes in the internal 2-bit counter and provide so a feedback for the frequency/data rate currently being used.

The binary representation is decoded by the 74HC138 decoder, IC_7. For each selected data rate a single LED from the available four, i.e. D_8, D_9, D_{10} and D_{11}) is lit. Resistors $R_{30\text{-}33}$ are current-limiting resistors. The decoding process is gated at G1 of IC_7, pin 6, by the carrier-detect output, pin 19 of IC_3.

If there is no valid data at the

retimer input the outputs of the CLC016 are latched, preventing random oscillations. The carrier-detect signal is connected to the MUTE input of IC_3, pin 28, and decoder IC_7 is disabled so that no LED is lit, indicating that there's no valid data.

Data-rate selection resistors R_{22-25} should be accurate to 1% or better as for each resistor there is a range of rates for the VCO to lock on. Components C_{12}, C_{13} and R_{16} form the loop filter of the PLL. They connect to the control lines of the voltage-controlled oscillator, pins 12 and 9, and the frequency detector, pin 10. Values used are those recommended for the multi-rate case, where all four SMPTE data rates are used.

The CLC016 outputs differential data on SDO and SDO\ and a differential clock on SCO and SCO\. These signals are at ECL levels and interface directly with the SD+, SD–, SC+ and SC– inputs of the CLC011 deserialiser.

Resistors R_{11-14} are terminate and define levels according to the discussion about logical levels presented earlier in the article.

Deserialisation

After reclocking, the serial clock and serial data enters the CLC011 deserialiser/decoder, IC_4. As full decoding of the signal is necessary to see if the signal is received correctly the NRZI-to-NRZ converter, the descrambler and the frame resynchronisation are enabled through resistor R_{15}. This resistor connects the corresponding pins, NRZI, pin 9, DESC, pin 10, and FE, pin 11, to the V_{CC} supply.

Parallel data outputs PD0-9, the parallel clock PCLK and the end-of-active-video EAV signal are decoded and available. However, they are not used in the current design because there are other criteria for correct transmission and processing of the signal.

The timing reference signal TRS is one of these criteria. As it appears only if a valid serial digital video is available on the input of the receiver it can be used as a 'Valid Video' flag. I have decided to use negative (error) logic – if there is no 'Valid Video' a LED should be lit.

As the TRS markers are short in duration, they can not be observed visually by a LED. I used a 74HC123 monostable multivibrator, IC_{5A}. Its time-constant determining components are R_{27} and C_{23}.

If there is valid video on the input, the the TRS-signal from the CLC011 retriggers IC_{5A} continually so that a continuous pulse appears at the output, Q. This output connects through current-limiting resistor R_{29} to the NO_TRS LED, D_2. As in normal conditions an active high appears at Q, the LED is dimmed and so the user is provided with the feedback that there is a TRS.

If for some reason the serial digital signal is dropped or appears so distorted that the TRS can not be decoded, the TRS-output ceases to retrigger the IC_{5A} and Q goes low. The LED D_2 is lit indicating 'NO_TRS'.

Of course it is useful to have the TRS horizontal sync pulses as a test signal to be viewed on an oscilloscope. Protection resistor R_{34} and BNC connector J_3 feed this signal to the outside world. As this connector has shared functions, switch S_3 is provided. As low-frequency signals – sync pulses – are switched they are not critical so a normal switch can be used to commutate the signals.

'New sync position' error marker

There is another error marker decoded from the input signal. This is the new sync position, or NSP, signal.

If the received SDI signal is so distorted – through incorrect signal processing, cable losses/drops of signals or excessive jitter – that the receiver is resynchronised every time on a new TRS, then the TRS appears every time in a new position relative to the old TRS. Thus a high level is generated on NSP until proper alignment of the TRS on the parallel clock data rate is achieved again.

Output from NSP triggers monostable multivibrator IC_{5B} so that a low going pulse appears on its Q\ output. Time-constant determining components of this monostable are R_{26} and C_{22}. The resulting pulse – or long pulse obtained from several successive retriggering events on the multivibrator – lights LED D_3, labelled 'TRS_Error' through current limiting resistor R_{28}. So a TRS alignment error is indicated.

Determining a signal's corruption level

Sometimes it is useful to have some quantitative measurements of the errors presented in the signal. This can be done for example by counting the TRS alignment errors. For this purpose, the NSP output from the CLC011 is output on connector J_3 through the switch S_3 and protective resistor R_{36}.

If the user connects a frequency counter in pulse counting mode at this output, he or she can collect information about the numbers of TRS-hits during a long

Specifications of the SDI test

Video serial digital outputs	
Applicable standards	ITU-R656, SMPTE 259M
Output level	800mV pk-pk nominal ±10% Into 75Ω
Number of outputs	1 BNC
System	NTSC or PAL – switch selectable
Output impedance	75Ω
Sampling	4:2:2
Line/field rate	525/60 and 625/50
Rise and fall times	800ps
Data jitter	220ps
27MHz clock accuracy	27MHz ±10Hz
Video test pattern selection table	
Switch positions	Test pattern
8	Full field 75% colour bars PAL
9	Equaliser pathological PAL
A	PLL pathological PAL
B	Flat field black PAL
C	Full field 75% Colour Bars NTSC
D	Equaliser pathological NTSC
E	PLL pathological NTSC
F	Flat Field Black NTSC
SDI receiver	
PLL Data rate	143, 177, 270 & 360 Mbit/s
Impedance	75Ω internally terminated
Level	800mV pk-pk nominal
Error indicators	
No TRS:	Missing timing reference signal
TRS Error:	Timing reference signal Alignment error
Monitor output	
Mode 1:	Sync pulse (on TRS) observation – sync pulses can be viewed on an osclloscope.
Mode 2:	Error counting – TRS alignment errors can be counted with an universal counter.
Mode 1 and Mode 2 are selected with a front panel switch.	
Power requirements	
Power	6VA

time interval. A period of 72 hours for example is a common test.

There are several power-supply bypass capacitors in the design as a clean voltage is necessary for correct operation. These are C_{17-21}, C_{27}, and C_{29}. The power supply is a single +5V derived from the three-terminal LM7805 regulator, IC_6. An appropriate heatsink near the X_1 crystal provides the above-discussed oven effect.

Capacitor C_{24} and diodes D_{4-7} together with the mains transformer form a full wave rectified supply. Capacitors C_{25} and C_{26} are the three-terminal regulator filtering components.

Implementation considerations

The 270Mbit/s SDI signal has spectral components in excess of 1GHz. As a result, SDI equipment – especially large-capacity routers – is usually a strong source of electro-magnetic radiation. This means that proper shielding techniques should be applied to every device that generates SDI signals or uses local oscillators to reclock them.

My SDIT270 test pattern generator and receiver is housed in a plastic box. To make it conform to the EMI standards, I have shielded the device with isolated copper tin on the inside face of the box. The tinning is grounded.

When designing a printed circuit board, special attention should be paid to separating the output of the TPG and the input of the receiver as they are housed in one and the same box.

External bypass capacitors should be provided on the power supply lines and they should include both RF ceramic capacitors of, say, 0.01µF to 0.1µF, and tantalum electrolytic types[4] in the range 2.2µF to 10µF.

The two layers of the board (top and bottom) can be flooded with copper by placing a polygon plane, which will improve shielding and isolation. The polygon should be connected to GND (V_{SS}) with frequently allocated vias according to good RF design techniques.

Don't forget to remove the ground plane away from all transmission lines and component pads. Don't place a ground plane under the components on both sides of the PCB as this alters the transmission line impedance and increases unwanted parasitics.

Using the tester

Different applications exists for the SDIT270 ranging from trivial to sophisticated. **Figure 13** presents a summary of the most common applications.

Perhaps the most widespread use of the SDIT270 is as a standard test pattern generator for the studio environment as this is shown in example A. In this case, all test patterns can be used, but the receiver is not implemented.

As the SDIT270 uses a standard professional-grade internal test pattern generator – most common for studios is 75% colour bars – this application provides the possibility for the broadcast operator to obtain high-grade equipment at reasonable cost.

The next two configurations as shown in examples B and C are used to test digital equipment with SDI inputs/outputs. In this case it is not possible to apply stress with pathological patterns. The idea is simple. If you feed a SDI-router/cable plant with an SDI-signal – common 75% colour bars – at the input, you would also expect to obtain error-free SDI-signal at the output.

If the device under test distorts the signal in some way, in most of the cases this will lead to TRS alignment errors. In this case, the TRS_Error LED will be lit. If the signal drops, then the LED No_TRS will light.

If you want to test how many drops or alignment mismatches there are in 72 hours for example, then a conventional frequency counter connected to the monitor output can be used to count drops.

Example B shows the 'loop-through' configuration. This mode has the advantage that a single SDIT270 device is used to generate test patterns and to evaluate them.

Sometimes it is not possible to loop the signal back to the source. One example of such a situation is where a long cable, say 100m, goes from one location to a different location 100m away, but no other cable is available for return. In this case the C example with two SDIT270 devices proves to be useful. The first device generates the pattern, the second one evaluates it. This is the 'Straight through' configuration.

Example D shows the case where an SDI-capable device needs to be qualified in terms of performance of the internal equaliser and PLL reclock circuits. The best way to do this is to stress the equaliser with the special equaliser-pathological test pattern, and then to stress the PLL-reclock with the PLL-pathological test pattern.

If something can go wrong with the tested SDI equipment in this case, then it will go wrong – hence the term 'stressing'. In the most cases this situation will be detected and reported by the tested equipment. There is not much sense in looping the output of the tested device back to the SDIT270 receiver. In such pathological situations, errors tend to accumulate over cascaded devices, so it is most likely that the SDIT270 will report errors.

Yet another possible application is presented in example E. If you have an unknown source of some sort of signal, how can you find out whether it is a valid SDI signal or not? The simple solution is to connect the equipment output to the SDIT270 receiver input and to look for errors on the LEDs. You can also determine the data rate of the signal.

In summary

Although relatively simple as a schematic, this test generator and receiver incorporates powerful signal processing integrated circuits. The chip set used makes things possible that the average video systems user could even not dream of in earlier days – especially from such a handy and portable device.

Through the SDIT270, the video engineer or system integrator can obtain valuable information about a serial digital-video processing system. In most cases, he or she should be able to isolate a possible fault using the tester.

Of course the highly specialised video test sets from well-known vendors can provide much more information. Some have error-detection and handling features for example. But such in-depth analysis capabilities are not necessary for most tasks ■

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4. National Semiconductor, 'CLC020 SMPTE 259M Digital Video Serialiser with Integrated Cable Driver', February 2000.
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Send your ideas to: Jackie Lowe, Cumulus Business Media, Anne Boleyn House, 9-13 Ewell Road, Cheam, Surrey SM3 8BZ

De-rippler for EHT supply

The circuit shown was developed to reduce the ripple from a 600kV supply without resorting to additional high-voltage capacitors. Merely increasing the series resistor R_f was not appropriate either, since the electron-gun was sometimes run in a pulsed mode, resulting in voltage droop followed by slow recovery.

The ripple of 1V peak-to-peak, mainly at 100Hz, is sensed by integrating the current in the existing filter-capacitor C_f, according to $dV=Idt \div C$, and then fed forward in compensation.

In order to make adjustment easier, two op-amps are used. Amplifier A_1 acts as a current-to-voltage converter whose gain is set using P_1. Integration is performed by the second amplifier, A_2, with trimming of the equivalent series resistance by means of P_2. Since C_f is not a perfect capacitor, this trimming P_2 makes an appreciable difference to the performance achievable.

The amplifiers are powered from the ±12V battery already installed for the heater and auxiliary supplies of the electron-gun. Initially, the trimmers are set with the EHT switched off and a signal injected by means of a waveform generator.

Capacitance C_f is slightly voltage-dependent, and so some further iterative adjustment is needed after checking with an independent AC-divider stack when the full EHT is applied. I found that the ripple could ultimately be brought down to about 10mV – an improvement of one hundred-fold.

When the electron-gun was operated in pulsed mode, i.e. drawing a 10μA current pulse some 1ms wide, at a 10ms repetition rate, the capacitor droop of 1V was reduced to 10mV at the output. This technique is better than trying to apply a compensation waveform of fixed amplitude and phase, as in the traditional 'humdinger' method, since correction is made automatically for variations in source and load.

C J D Catto
Cambridge
UK
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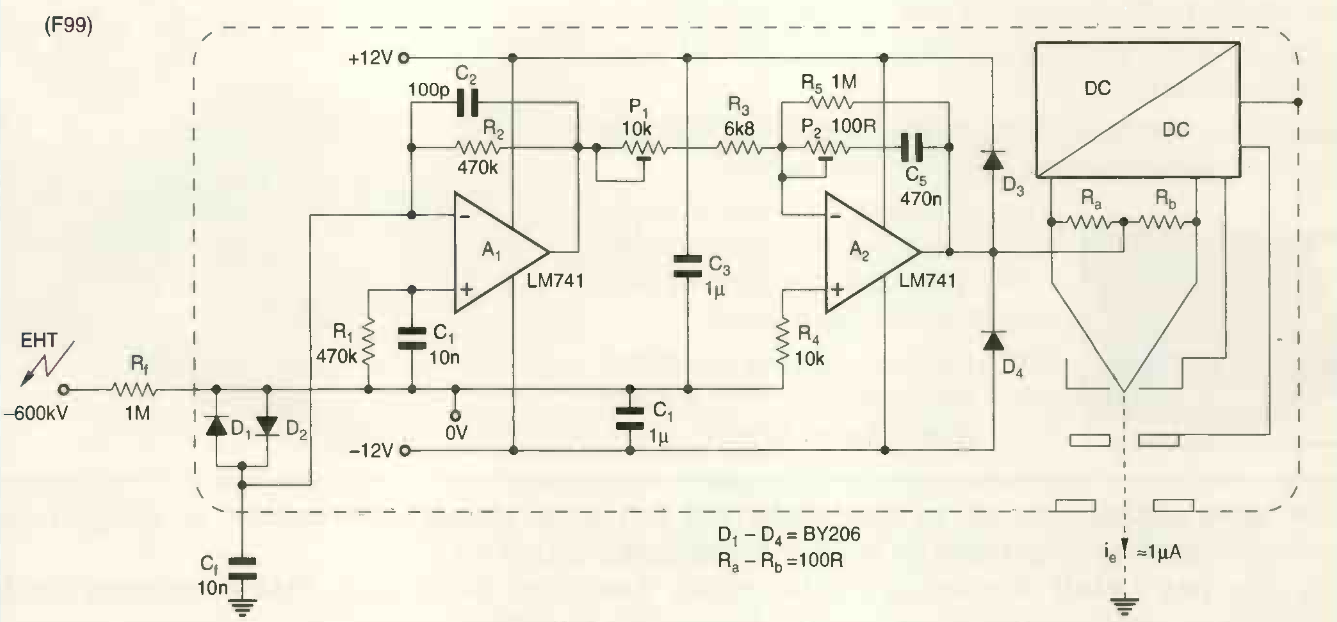


Reduce ripple on an EHT supply with this feed-forward circuit

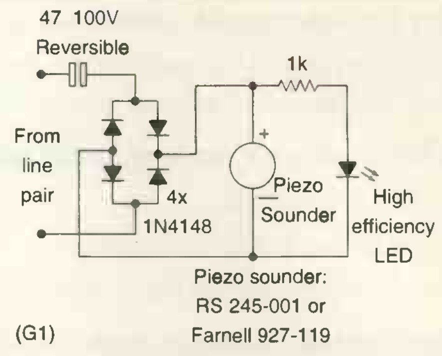
Connect two dial phones as simple intercom

The once ubiquitous dial and bell telephones are nearly indestructible and easy to modify but require a somewhat complex 17Hz, 70V ringing generator. However, the back emf of the bell coil can be pressed into service.

Remove one side of the bell coil from terminal T4 and reconnect to T8. The bell coil is now across the line on the line side of the hook switch. Connect the circuit in the figure across the line pair – the LED indicator is optional or a SPCO switch can be added to give audible or visual indication as required.

Modify two telephones similarly, wire both in series with each other and a 14V psu and the intercom is complete. Lift the handset and turn the dial to activate the piezo sounders. The sounder is easily heard throughout a house of medium size.

Peter Kenyon
Almancil
Portugal
G1



With two redundant old dial-and-bell telephones, this circuit makes a useful intercom.

Optoelectronic square-roots

The circuit shown produces an output voltage proportional to the square root of the input. An LED and LDR are mounted in a light-tight enclosure, with light from the LED illuminating the LDR. The conductance of the LDR is then approximately proportional to LED current which in this circuit is determined by V_{out}. Therefore the resistance of the LDR is,

$$R_{LDR} = a\frac{R_1}{V_{out}}$$

where a is a constant dependent on several factors: the sensitivity of the *LDR* used, *LED* efficiency, etc. As,

$$V_{out} = -\left(\frac{R_{LDR}}{R_2}\right)V_{in}$$

it follows that,

$$V_{out} = \sqrt{\left\{-V_{in}\left(a\frac{R_1}{R_2}\right)\right\}} = b\sqrt{-V_{in}} \qquad (1)$$

The minus sign means that the input voltage must have the opposite sign to the output voltage, with the LED connected with the appropriate polarity.

A standard red LED with diffuse encapsulation, and an LDR with a clear encapsulation, were used. These were mounted end-to-end in a piece of heat-shrink tubing, and then wrapped in black polyurethane foam to exclude stray light.

Separate measurements on this combination showed that it had a current-controlled LDR conductance of about $0.09\mu S\ mA^{-1}$ for LED currents in from 1.5 to 15mA, corresponding to a value of 1.11×10^4 V for the a constant above. The LDR conductance to LED current relationship had good linearity.

In the circuit shown, for V_{in} from –20mV to –1.2V,

$$V_{out} = b\sqrt{-V_{in}} + V_{offset} \qquad (2)$$

with an accuracy of better than 1%, for a V_{offset} of around 30mV.

The graph shows data as open circles, while the dashed line is a best-fit curve to equation 2. The best-fit value for b was close to that predicted from equation 1.

For smaller input voltage magnitudes, the square-root function became less accurate. For larger input magnitudes, the circuit became roughly linear, i.e. V_{out} proportional to $-V_{in}$ rather than to $\sqrt{(-V_{in})}$, possibly due to current limiting in the op-amp output stage maintaining a constant LED light output independent of V_{out}.

The slow response time of most LDRs to changes in illumination, and the possibility of thermal drift at higher LED currents, are potential sources of error in this circuit. However, if the constraints on input voltage are acceptable, it may be a low-cost alternative to dedicated analogue computation chips or more complicated log-antilog approaches to square root generation.

Mike J Toohey
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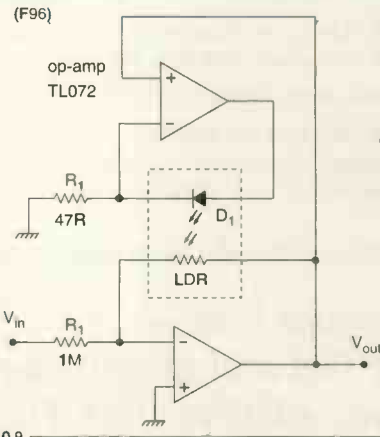

Fig. 1. Circuit for perform the square root function using a coupled LED and LDR.

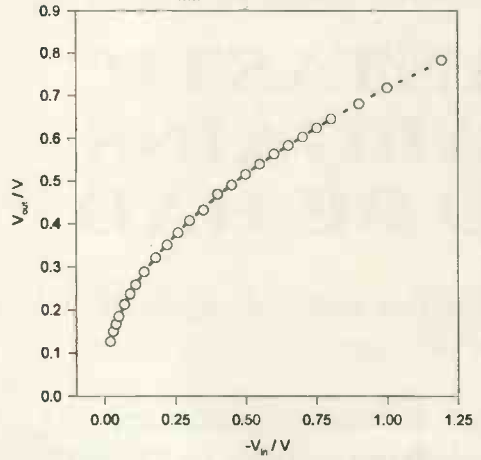

Fig. 2. Actual performance (circles) versus theoretical curve (dashes) of the optoelectronic square rooter.

Photovoltaic system current-sense circuit

The circuit here presented is for sensing current in photovoltaic systems using the MAX138 or similar a-to-d converter. The advantages of the circuit include a wide supply voltage range of 3V – 30V low supply current of <1mA, and single supply operation.

Supplies up to 60V are possible using the LT1787HV instead of MAX472, with modfified power supplies. Note that when low currents must be measured accurately, a negative supply voltage is necessary; use an ICL7660 for example.

The system measures the current supplied by the photovoltaic module (C), by the battery (B) or battery charging current (A). The circuit is applicable in photovoltaic systems monitoring solar powered instrumentation, marine instrumentation, power supplies, energy management systems etc.

The MAX472 current-sense circuit is used, together with current shunt and R_g, R_{out}. Output from the 472 is buffered by a voltage follower and inverting amplifier as presented in Harris application note AN9609.1.

Output of the inverting amplifier is presented to a MAX138 DVM chip. With slight modifications, the circuit could be used with any member of ICL71xx family or with MAX131 or similar ICs.

The output voltage of the MAX472 is given by,

$$U_{outIC1} = \frac{R_{sense} \times R_{out} \times I_{sense}}{R_g}$$

values shown are for 20A current range with a 200mV range a-to-d converter (100mV reference). For other ranges component values should be recalculated, according to the instructions in the references.

When direction as well as amplitude of the current must be measured, the minus sign on the LCD readout should be driven. Due to the negative output voltage of the inverting amplifier, it is necessary to control the LCD negative sign only when the sign output of MAX472 is high. Some additional logic is required in this case.

For very low power-supply voltages, a CD4016 with additional capacitor should be used for driving the LCD decimal point, instead of the common solution with a CD4070 using the test pin as reference.

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Jesenice
Slovenia
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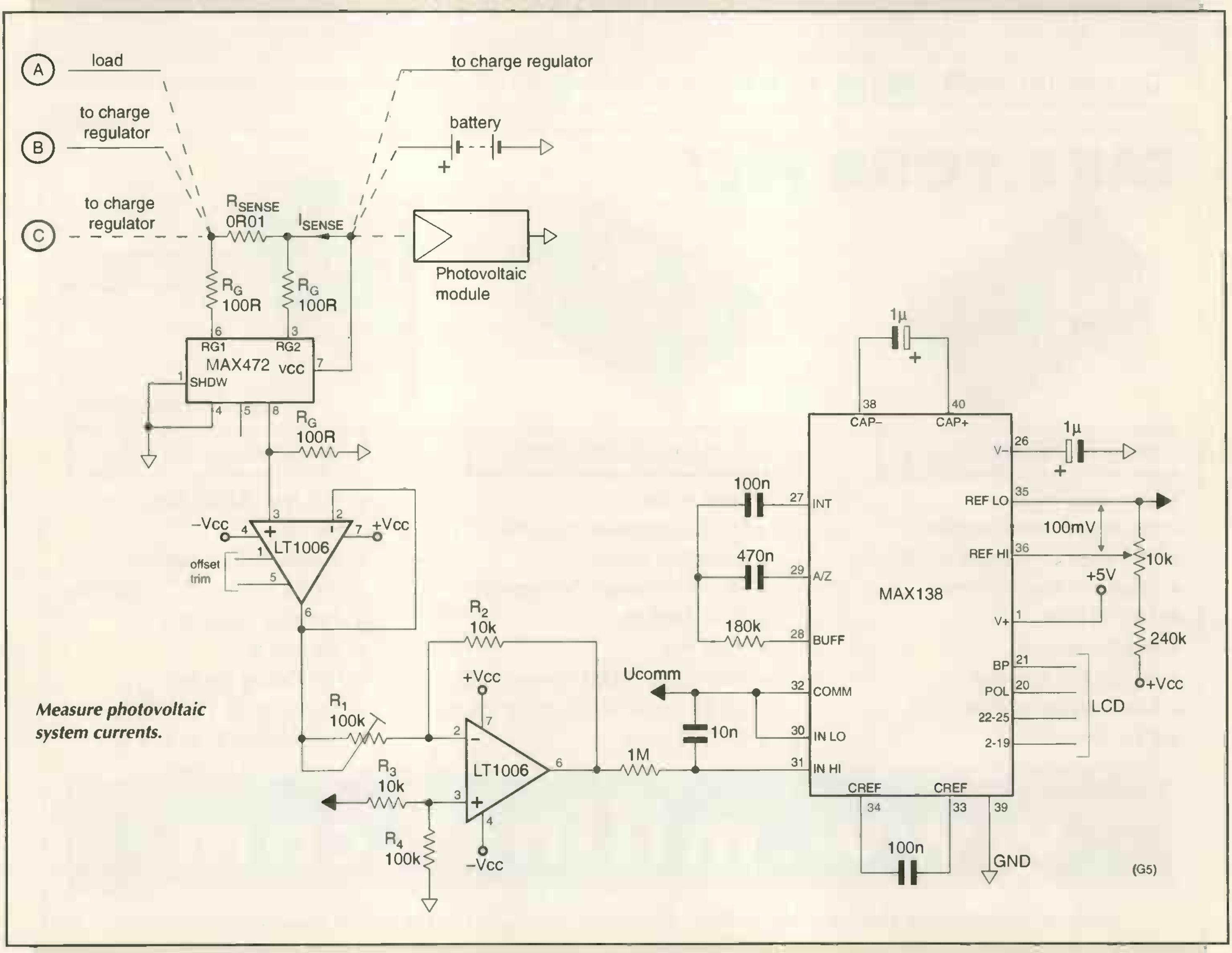
Further reading

Maxim: MAX472 Data Sheet
Maxim: MAX138 Data Sheet Harris: AN9609.1 – "Overcoming Common Mode Range Issues When Using Harris Integrating Converters".



Measure photovoltaic system currents.

Clipping indicator

Clipping indicators are common on PA and other amplifiers that are likely to be driven close to their maximum power ratings. Clipping is gross before it becomes audible – especially in situations where only one of several amplifiers is clipping – so a warning of the onset of clipping is useful. This circuit was built using components to hand, to prevent abuse of a small PA amplifier that lacked a clipping indicator.

It is also most instructive to fit a clipping indicator to a hi-fi amplifier. Since music has a high peak-to-mean ratio and voltage headroom rises as only the square root of output power, even a powerful amplifier will begin to clip peaks well before the volume becomes earth-shatteringly loud.

Those who do not believe that intermittent, short-term distortion is inaudible should note how much clipping has to take place before you can hear it. Restricting the input frequency range with, for example, a graphic equaliser can be seen to make much more headroom available; this is one way to choose crossover points and speakers for a 'multi-amped' system to maximise headroom.

In normal operation, both Tr_1 and Tr_2 are conducting. When the input approaches the supply rail closely enough to turn either transistor off, the polarity of the voltage applied to the inputs of the op-amp reverses and the output goes high, turning on the LED. The flashes may of course be very brief, hence the speed-up capacitor C_2.

A low value for R_{11} and a high-intensity LED makes the indication easier to see. The LED is returned to ground rather than –15V both to reduce the dissipation in R_{11} and to ensure that it turns off properly if the op-amp output will not swing all the way to the negative rail.

Input attenuator R_1/R_2 will need adjusting to suit the amplifier. This is easiest with an oscilloscope. The circuit as shown is designed for an amplifier of conventional architecture with ±60V supply rails and an emitter-follower output stage. The 'digital' nature of the output makes it easy to feed it to timer circuits to protect against continued clipping or gross DC offset.

The ±15V supply rails are available in most amplifiers to power things like protection circuitry, input signal conditioning and pretty flashing lights on the front panel. If only the main HT rails are available, it would be possible to omit the op-amp and connect D_1 and D_2 directly between the junctions of R_9/R_{10} and R_7/R_8, with suitable adjustment of values. In this case though, power dissipation would probably be a problem.

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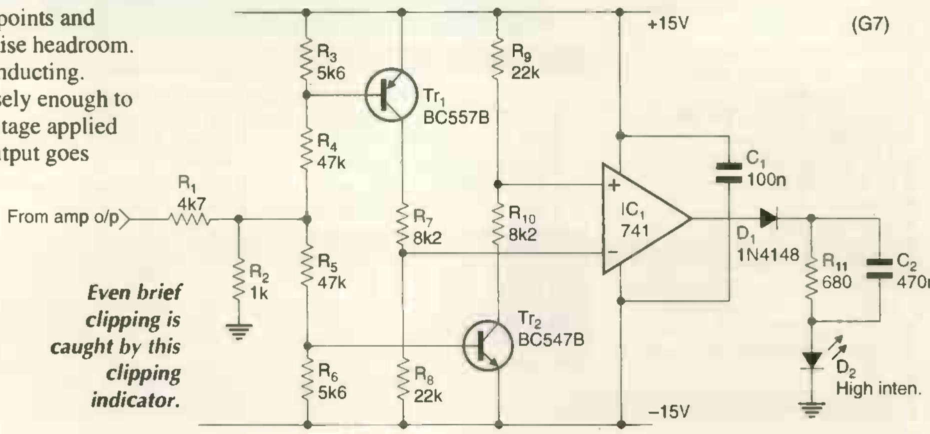

Even brief clipping is caught by this clipping indicator.

Simple full-wave audio-limiter

Needing a limiter for a public address system used by non-technical personnel, I developed this circuit. It is based on the NSL32 opto-isolator from Silonex. This unit comprises a low-distortion cadmium sulphide LDR optically coupled to an LED (Farnell code 316-8773).

Referring to **Fig. 1**, Tr_1 and Tr_2 are both normally on, maintaining point *B* near to 0V. When signal peaks at point A approach the supply rails V+ or V–, either Tr_1 or Tr_2 switches off, and point *B* moves towards V– or V+, respectively. Either Tr_3 or Tr_4 is switched on, supplying current to C_1 and the NSL32 LED.

Voltages V+ and V– can be stabilised in the usual manner using 78L and 79L 3-terminal regulators. However, the limiting level will be temperature dependent as the V_{be} of Tr_1 and Tr_2 change. Use the regulator in **Fig. 2a)**, in which D_1 and D_2 compensate for this V_{be} change.

If temperature stability is less important but the limiting level is required to track the supply rails – for example to maximise efficiency – use the ripple reducer in Fig. **2b)**. This should supply only Tr_1 and Tr_2. At 100Hz and 1.5mA, this regulator reduces ripple by 50dB, but drops only one volt.

Note that Tr_1 and Tr_2 may have the-combined V+ and V– supply appearing between collector and emitter. Use higher voltage devices if necessary, or add series zener diodes.

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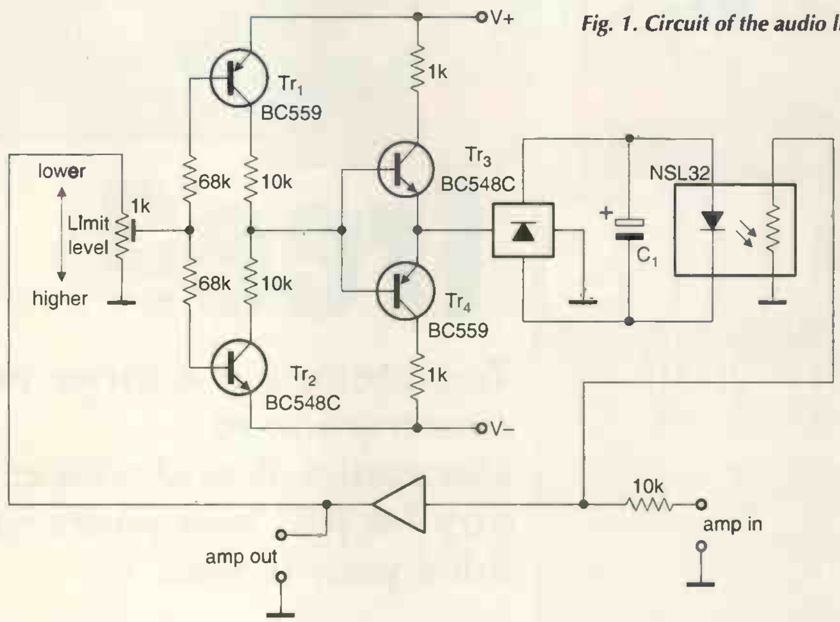

Fig. 1. Circuit of the audio limiter.

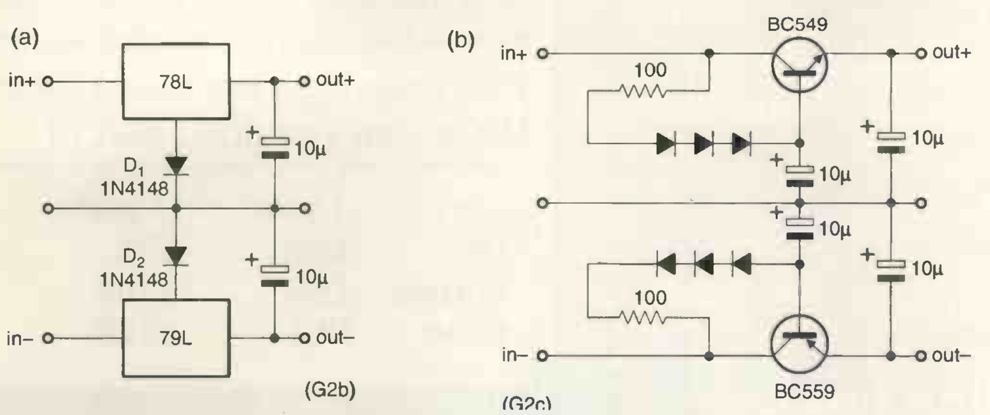

Fig. 2a) A simple compensated power supply, a). The version in b) works down to 1V headroom.

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NIC Eurotech
Tel: 01280 813737
www.niccomp.com

Logic family works below 1V

Texas Instruments has introduced a logic family that is optimised at 1.8V but also operates at sub 1V levels. Called the Advanced Ultra-Low Voltage CMOS (AUC) family, it consists of 'Little Logic' single, dual and triple gates, Octals and WideBus devices. All are optimised at 1.8V and have an operating voltage range of 0.8V to 2.5V. With a voltage tolerance of 3.6V, AUC extends the life of systems by allowing legacy devices to remain functional, said the company. In addition, the sub-1V feature allows AUC to be operated from a single cell. AUC also includes I_{off}, which protects the device by supporting partial power down applications. TI has been working closely with Philips and IDT to develop the specifications for the new AUC family. Initially, TI will release the 'Little Logic' parts and Philips will offer an alternate source. Subsequently, in 2002, IDT, Philips, and TI will release Octals and WideBus devices. Based on this collaboration, second source agreements are in place. The AUC family is available in single/dual/triple gate devices for portable consumer electronics. Consistent with the family, the Little Logic AUC devices are optimised at 1.8V, while maintaining high speed and low noise. The devices will be available in various packaging options, including the firm's NanoStar packaging.

Texas Instruments
Tel: 0049 8161 80 3311
www.ti.com

500W full-brick DC-DC converter gets 24V inputs

Lambda has added 24V input models to its 500W PAF range of full-brick DC-DC converter modules. The PAF500F24 series is designed for input voltages between 18V and 36V DC. It employs the firm's combination of Asic control with zero voltage

switching technology to give designers a three-fold increase in power density over conventional converters, said the company. Two versions are available: the 12V output unit with a maximum output current of 42A; and a 28V output unit with a maximum output current of 18A. Power density is up to 5.53W/cm^3. The PAF series offers efficiency at 90% for the 28V output model and 89 % for the 12V output model.

Lambda
Tel: 01271 856666
www.lambda.com

Display interface drives separate TFTs

Display Technology has introduced its latest Vampower-10 digital (PCI/AGP/ BUS) TFT interface cards. The V10 has the latest ATI chip set and can drive

Single-chip phone ring-tone generator

This sound generator IC from Rohm is optimised for mobile phone hand sets where it provides a single chip design for the output, customisation and download of ring tones. Rohm's BU8772KN melody generator IC can generate up to 16 simultaneous harmonies and offers 128 tones. The device can also output 47 drum sounds and 32 different sound effects as well as providing DTMF tones through a built-in DTMF generator. Incorporating a serial interface for direct microprocessor control, the BU8772KN IC features an integrated sequencer that minimises the processing load on the handset CPU. A FIFO buffer allows for the download of music data, while the firm claims that its patented pseudo square wave implementation maximises performance and minimises distortion from the small loudspeakers used in phone hand sets. The device has a built-in two-dimensional filter which allows for the selection of sine or square wave outputs for maximum effect and offers envelope fade-in and fade-out and independent control of tone volume. Stereo output is supported through a built-in stereo sound d-to-a converter, while master clock frequency is selectable between 12 and 20MHz. Supplied in a miniature QFN28V package measuring 5.0 x 5.0 x 0.8mm, the BU8772KN operates across a supply voltage of 2.7 to 3.6V.

Rohm
Tel: 01908 282666
www.rohm.co.uk

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two completely separate displays (LVDS or Panellink/TMDS) with different resolutions. The ATI chip is available with 8Mbit of memory, with the 16Mbit about to be released. This will allow one to drive two displays in parallel, in full colour mode with resolutions up to UXGA.
Display Technology
Tel: 01634 295555
www.displaytechnology.com

1GHz scope has runt and slew rate triggering

LeCroy has added a 1GHz model to its series of two- and four-channel digital oscilloscopes. The range offers 350MHz, 500MHz or 1GHz bandwidth, 1 to 4 Gsamples/s sampling rate, large colour displays, long data acquisition memory, and strong analysis packages. The scopes also have a trigger package offering runt and slew rate triggering. The model LT584 is a four-channel 1GHz DSO with 2Gsamples/s sampling rate, 250kpts of acquisition memory per channel. When using only two of its four inputs, the scope samples at 4Gsamples/s into 500kpts memory. Users can choose between memory options of 1 or 4 million points of acquisition memory per channel (interleaving to 2 or 8Mpts when using two channels). It is targeted at engineers who work on component design, digital electronics, medium speed communications protocols and automotive applications. All instruments come standard with an 8.4in colour TFT display. Also available are advanced waveform maths (WAVA) and application-specific signal analysis packages for measuring signal jitter/timing (JTA), power measurements (PMA1), advanced optical recording measurements (AORM) and testing of electrical telecom signals using standardised test masks (MT01 and MT02).
LeCroy
Tel: 001 800 453 2769
www.lecroy.com

Digital phase detector captures 75ns pulses

Pascall Electronics has introduced a 160MHz digital phase detector for use in interferometry systems, direction finders, instantaneous frequency measurement devices and test systems. It performs high-speed measurement of the absolute phase difference between two input signals and presents the result as an 8-bit word for further digital processing. The detector is capable of capturing pulse widths down to 75ns, provides phase measurements to ±3 counts and gives an amplitude linearity of ±1dB for both signals over the dynamic range 0dBm to –60dBm. External dimensions are 89.0 by 51.0 by 25.4mm, and power requirements are +15V, +5V and –5V with an operating temperature range of –40 to +85°C.
Pascall Electronics
Tel: 01983 817300
www.pascall.co.uk

Noise source for DSL modem testing

Admit has launched the ANS-1000 reference noise source, designed for new product development, conformity testing, and on-going product assessment of DSL modems. Working with a PC, each unit is individually calibrated to ensure signal tolerance. A library of crosstalk disturbers and impulse noise definitions are available meeting the requirements of T1.413, G992.1 (G.Dmt) and G992.2 (G.Lite). The Noise Builder toolkit allows the user to customise noise spectra to simulate their network measurements. All noise delivered by the ANS-1000 falls within the ITU G.996 test standard specification and integrated and calibrated according to that standard.
Admit
Tel: 01383 8288300
www.admit.co.uk

RF tag reader supports smart labels

Texas Instruments Radio Frequency Identification (RFID) Systems has announced a reader family to support the ISO15693

standard for smart labels and cards. The readers are designed for RF ID applications in supply chain management, product authentication, and asset control. All of the readers operate at 13.56MHz.
RFID Systems
Tel: 01234 840102
www.rfid.co.uk

Transient voltage suppressor/filter network

A transient voltage suppressor (TVS)/filter network is available from Hunter Electronic Components. The ProTek STF701 series is a TVS/filter combination network designed to reduce EMI/RFI noise on data I/O ports and provide transient voltage protection for hand-held electronic systems such as PDAs, notebooks and pagers. Suitable for both protection and noise suppression on transceivers operating up to 100MHz, this device is designed for use on digital circuits at less than 5V. It is packaged in industry SO-8 with a common ground pin for

28V DC-DC power module delivers up to 310W

Ericsson Microelectronics has extended its PKL 4000 series half-brick DC-DC power modules with a 90 per cent efficient, 36-75V input, 28.2V output version intended to address wireless power amplifier applications. This 310W output power module offers circuit protection and conforms to international safety and EMI regulations. The 28.2V, 11A PKL 4316 PIT model offers 90 per cent efficiency at full power and up to 106.7W/in^3. This module is capable of handling input voltages from 36-75V. The thermal design keeps the output Mosfets at less than 10°C above the baseplate temperature, contributing to an MTBF of greater than 2.2 million hours. The industry standard half-brick format has been enhanced with two additional output pins. All other pin assignments are fully compatible with the industry standard half-brick pin-out. This standards compliance offers a straightforward route for upgrading existing board designs to take advantage of the new power levels delivered by the 2.4 x 2.4 x 0.5in package.
The PKL 4000 series includes models with outputs voltages ranging from 1.8V to 12V at up to 60A output current (310W power limited). Samples are available from stock.
Ericsson Microelectronics
Tel: 01793 488 300
www.ericsson.com/microelectronics

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both TVS/filter networks. Each package consists of two networks, each to be used for common-mode protection against electrostatic discharge (ESD) in accordance to IEC 6100-4-2, EN61000-4-2. The individual TVS components will protect against an ESD pulse of greater than 25kV, said the company. SPICE model parameters are available for circuit simulation.

Hunter
Tel: 01628 675911
www.hec.co.uk

Temperature controller for semiconductor laser diodes

Analog Devices is offering its first single-chip thermoelectric cooler (TEC) controller for DWDM (dense wavelength division multiplexing) networking equipment. Based on the integration of several amplifier circuits, as well as other proprietary linear technologies, the ADN8830 is designed to improve control of the TEC, a critical component in maintaining laser temperature in optical communications systems. High channel-count DWDM systems – up to 160 channels per fibre – require high-precision

temperature control in order to stabilise specific laser wavelengths. The device features a patent-pending switching output architecture and a patented auto-zero front-end. It is this combination, said the company, which results in low noise for a "quiet" laser environment, which makes for more accurate signal transmission and reception.

Analog Devices
Tel: 0032 11300 635
www.analog.com/opnet

Quad output DC/DC converter with wide input range

Power-One is offering quad-output DC/DC converters based on a flyback converter topology, using all surface-mount components and planar magnetics. There are six IMX35 quad-output models. Models with four separate, electrically-isolated outputs of 5V at 1.35A ea., 12V at 0.65A ea., or 15V at 0.55A ea., have input voltage ranges of 9-36V. Models with an 18-75 V input range are available with outputs of 5V at 1.4A ea., 12V at 0.7A ea., or 15V at 0.6A ea. Outputs can be parallel and series connected, giving output variants from 5 up to 60V. Other input ranges, double and triple output voltages are also available.

Power-One
Tel: 01425 474 7521
www.power-one.com

Sub-rack for Compact PCI development systems

Rittal's CPCI developer sub-rack is for the test and debug CPCI front plug-in and rear-loaded I/O boards and avoids the use of extender cards, which may cause possible distortion to sensitive signals. Power for the backplane can come from an existing bench top supply. Alternatively, a pluggable power supply may be used in place of PCB slots, or an ATX power supply can be plugged directly into the backplane. It consists of an open frame with a pair of fans mounted in the bottom to assist in cooling the plug-in boards. Guide rails are fitted at front (160mm) and rear (80mm). A total width of 42HP provides mounting for a backplane with up to 10 slots of CPCI or VME64 ext.

Rittal
Tel: 01709 704000
www.rittal.co.uk

Audio generator and counter

The AG100 from Tecstar is a 10Hz to 1MHz audio generator providing sine and square wave shapes with an integral frequency counter and a range of 0.2Hz to 50MHz.

An external sync input enables the instrument to be locked to an external source. The external input also allows the counter to be used from external signal. A four step and variable attenuator is also standard.

Pre programmed standard frequencies can also be selected which adds to the convenience and can save time in repetitive applications.

The instrument is housed in a low profile modern case with tilt stand. A bright LED display with additional enunciators ensures a concise read-out of measured values.

The AG100 is primarily aimed at education, industrial and the service industries.

Tecstar Electronics Ltd
Tel: 01480 399499
www.tecstar.co.uk

Controller gets DSP engine

Microchip's latest dsPIC family of controllers feature a fully-implemented digital signal processor engine, 30Mips non-pipelined performance, a 2.5 to 5.5V operating range and C-compiler-friendly design. The first 20 dsPIC30Fxxxx devices feature between 12 and 144kbytes of on-chip secure flash program memory and up to 8kbytes of data memory. The devices will be available in three product families targeting motor control and power conversion, sensor, and general-purpose applications. Devices will be available in 18- to 80-pin packages. The DSP engine features a high speed 16-bit by

Please quote *Electronics World* when seeking further information

16-bit multiplier, two 40-bit saturating accumulators and a 16-bit bi-directional barrel shifter. Independent address generation units enable concurrent fetches of two operands for most of the DSP class of instructions. Communications capabilities include combinations of RS-485 type UART, I^2C, SPI, AC97, CAN, and I^2S for peripheral expansion. Analogue peripherals include 10-bit four-channel high-speed simultaneous sampling a-to-d converters, PWM, capture and compare 12-bit a-to-d converters, programmable brown-out detect, and programmable low-voltage detect. Low power operation modes are also available.

Microchip
Tel: 0118 921 5858
www.microchip.com

SONET/SDH aggregation device with 12-channel framing

Exar has introduced the first in a series of SONET/SDH telecom protocol aggregation products. The XRT94L43 (SONET/SDH STS-12/STM-4 to 12 DS3/E3/STS-1 mapper/ demapper) is capable of aggregating 12 DS3/E3/STS-1 into OC-12/STM-4. This device features a 12 channel DS3/E3 framing, Level 2 performance monitoring and on-chip clock smoothing functions. Applications are likely to include digital cross connects, concentrators, edge switches, access equipment and add/drop multiplexers. Additional aggregation products are planned for release over the next few quarters. The device incorporates a fully programmable on-chip synthesiser that generates all the necessary clocks from a single 12.28MHz external signal source. This can eliminate the need for a 622MHz clock for the serial interface, 77MHz for the telecom bus interface and additional clocks for the jitter attenuator at DS3, E3, and STS-1 data rates, said the company. It can be configured to map DS3/E3 data into SDH TUG-3/VC-3 (conforms to the ITU-T G. 707 standard). The XRT93L43 supports the mapping and demapping of 12 channels of DS3, E3, or STS-1 rate signals to and from STS-12/STM-4. Other features include the ability of the XRT94L43 to multiplex and groom four channels of STS-3/STM-1 onto a single STS-12/STM-4 signal

Exar
Tel: 01753 63120
www.exar.com

400W plug-in PSUs optimised for COMPACTPCI

APW has introduced a range of 400W AC and DC input power supplies, providing standard CompactPCI voltages of 3.3V/68A, 5V/25A, +12V/5A and –12V/1.5A. Housed in a 6U by 160mm by 8HP (2-Slot) module for use in computer, test and telecom systems, the units support *N*+1 redundant and hot-swap requirements and provide power sequencing on power up and power down. Power inputs are 100-240V AC at 47-63Hz and 40 to 72V DC; the mains unit has a PFC of better than 99% at full load, said the company. Features include zero wire current sharing on 3.3V, 5V and +12V outputs with a minimum hold-up time of 18ms typical at full load. Load regulation is 0.5 per cent with remote sense, and line regulation is 0.1 per cent over the entire operating range. Supply fail and enable/inhibit control lines UL logic signals are provided and a front panel LED has power supply status, input good, fail and over-temperature indicator. Over-current protection covers all outputs set to 115-135% of full rated load with automatic recovery; over-voltage covers all outputs set to 115-135% of nominal, reset by recycling input power and over-temperature protection provides automatic shutdown with automatic recovery.

APW
Tel: 01489 774500
www.apw.com

SONET/SDH transceivers 0.18µm CMOS

Vitesse Semiconductor has added to its family of SONET/SDH serialiser/deserialiser ICs developed using 0.18µm CMOS technology. The VSC8142, VSC8145, and VSC8147 expand the firm's line of 2.5Gbit/s transceivers for 2.5Gbit/s serial or 10Gbit/s parallel optical transponder modules, next generation metro Dense Wave Division Multiplexing (DWDM) systems, SONET/SDH transmission systems, or optical test equipment. A complete reference design including a small form-factor optical module is available. The range additions are extended multi-rate devices with integrated multiplexer, demultiplexer, clock recovery unit and clock multiplier unit functions. Devices support OC-48, OC-12, OC-3 with or without forward error correction (FEC), Gigabit Ethernet, Fibre Channel and 2x Fibre Channel, along with other various data rates. The VSC8147 supports OC-48 (with or without FEC). Applications requiring a 16-bit differential LVPECL low-speed host interface use the VSC8142 while the VSC8145 and VSC8147 support a 4-bit LVDS interface, electrically compliant with the OIF SFI-4 interface specifications.

Vitesse Semiconductor
Tel: 01634 671167
www.vitesse.com

75Ω micro-miniature connector

A range of 75Ω MCX connectors has been introduced by Vitelec Electronics to add to the existing 50Ω range of this micro-miniature connector. They have turned brass bodies and are available as standard in gold or nickel plating. Centre contacts are manufactured from beryllium copper with gold plating and the insulators are PTFE. Plugs, jacks and bulkhead jacks are available for RG179 and RD179 coaxial cable. PCB mounting options include straight and right angle jacks, and a straight plug. A surface-mount jack is available, with a tape-and-reel packaging option for automated pick and place board assembly. This range of 75Ω connectors can operate up to 6GHz. The snap-on coupling mechanism allows for mating and unmating with a minimum of 500 mating cycles. VSWR is 1.13:1 for straight-cabled connectors and 1:07:1 for right-angled cable connectors. Insulation resistance is 1000MΩ minimum and insertion loss at 1GHz is 1dB for straight-cabled products and 0.2dB for right-angled cable products.

Vitelec
Tel: 01420 488661
www.vitelec.com

Please quote *Electronics World* when seeking further information

Super bright LEDs up to 10 000mcd

Easby Electronics is offering a series of super-bright conventional light-emitting diodes employing GaIN/GaN technology. The blue, white and green models offer brightnesses up to 10 000mcd. The Para Light L5T3xxx series of LEDs are conventional 5mm diameter products with a 2.54mm pitch, water clear lenses and 300° viewing angle. The L5T3VB5C (blue), L5T3L-W5C (white) and L5T3LP-G1C (green) LEDs have rated brightnesses, at 20mA, of 5000mcd, 3000mcd and 10 000mcd respectively. The blue LBD emission wavelength is 470nm and the green is 525nm. All the LEDs are suitable for high pulse current operation.

Easby Electronics
Tel: 01748 828214

3G test systems for development and installation

Racal Instruments has introduced 3G test instruments covering base-station installation and commissioning, mobile design and development, base-station development and evaluation and network performance optimisation. The 6413 Base Station Test System is capable of working with multiple standards, initially delivering 3GPP FDD capability. It will support both operators and manufacturers in the rollout of new UMTS networks. The instrument interfaces to the base-station through both the network telecommunications port and the RF antenna port. The 6401 Air Interface Test System is a multi-standard instrument designed for the test and verification of 3G mobiles and terminals known as user equipment (UE). Focused on 3GPP FDD technology first, the system is capable of supporting UE development from R&D through to system integration, validation and conformance testing against the defined 3GPP specifications. There is also the 6511 Mobile Emulator which incorporates layers 1, 2 and 3 of the UMTS FDD protocol stack. Test and analysis of base stations is provided as well as end-to-end testing of the network through the RF interface. Both circuit-switched and packet-switched data can be emulated.

Racal Instruments
Tel: 01344 388000
www.racalinst.com/umts

Programmable DSP for a clearer photograph

Texas Instruments' programmable DSP intended for digital cameras is claimed to achieve a 100 per cent performance boost and 25 per cent power reduction over the previous generation device. The TMS320-DSC25 encodes and decodes CIF resolution (352 x 288) MPEG-4 I+P frame video at 20 frames per second. Power-down modes provide a reduction in overall system power consumption and prolonged battery life. The enhanced DSP subsystem supports higher imaging, video-processing and preview-engine performance, the addition of an external host interface and SD, Multi-media Card (MMC) and Memory Stick interfaces. It combines the TMS320C54x DSP with an ARM7TDMI Risc processor on a single device. Additional features include a digital liquid crystal display (LCD) interface and S-video output. There is also direct memory access (DMA) to external dynamic random access memory (DRAM). Software modules will be available for all major video-imaging compression standards, including JPEG, motion-JPEG, MPEG, MPEG-4 and H.263.

Texas Instruments
Tel: 0049 8161 80 3311
www.ti.com

DDR DIMMs are tested to JEDEC standard

Smart Modular Technologies has announced that its prototype 184-pin PC2700 registered FBGA-based DDR DIMMs have been tested and conform to the JEDEC DDR333 standard. The devices used on the PC2700 DIMMs are packaged in the industry-standard FBGA (fine pitch ball grid array) footprint. This standard is the first SDRAM to use the FBGA

Microcontrollers have 384kbyte memory-on-chip

Hitachi's latest H8 16-bit flash microcontrollers feature up to 384kbyte of on-chip flash memory and new peripheral sets. The range includes the H8/3062BF which combines 128kbyte flash/4kbyte RAM. Also available is the H8/3008, a ROM-less equivalent of the H8/3062BF; the H8/3064BF, which features a memory upgrade path to 256kbyte flash/8kbyte RAM; and the H8/3068F, which offers a memory upgrade path to 384kbyte flash/16kbyte RAM as well as a four channel DMA controller and a third SIO (USART). They operate at 25MHz/5V and feature a peripheral set of three 16-bit timers, four 8-bit timers, an eight channel 10-bit analogue-to-digital converter, a two channel 8-bit digital-to-analogue converter, two USARTs and 79 I/O lines. The microcontrollers are supported by a new evaluation kit, which includes an evaluation board in a solid metal case, an RS232 cable and manual for the H8/3068F, the board and accompanying software.

Hitachi
Tel: 01628 585163
www.hitachi-eu.com

QUASAR ELECTRONICS LIMITED

Dept. EE, Unit 14 Sunningdale, BISHOPS STORTFORD, Herts, CM23 2PA

TEL: 01279 467799 FAX: 07092 203496

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'PICALL' PIC Programmer

Kit will program ALL 8, 18, 28 and 40 pin serial AND parallel programmed PIC micro controllers. Connects to the parallel port of a PC. Supplied with fully functional pre-registered PICALL DOS and WINDOWS AVR software packages, all components and high quality DSPTH PCB. Also programs certain ATMEL AVR, serial EPROM and SCENIX SX devices. New PIC's can be added to the software as they are released. Software shows you where to place your PIC chip on the board for programming. Now has new-chip auto sensing feature for super-fast bulk programming.

Order Ref	Description	inc. VAT ea
3117KT	'PICALL' PIC Programmer Kit	£59.95
AS3117	Assembled 'PICALL' PIC Programmer	£69.95
AS3117ZIF	Assembled 'PICALL' PIC Programmer c/w ZIF socket	£84.95

ATMEL 89xxxx Programmer

Powerful programmer for Atmel 8051 micro controller family. All fuse and lock bits are programmable. Connects to serial port. Can be used with ANY computer and operating system. 4 LEDs indicate programming status. Programs 89C1051, 89C2051, 89C4051, 89C51, 89LV51, 89C52, 89LV52, 89C55, 89LV55, 89S8252, 89LS8252, 89S53 & 89LS53 devices. NO special software needed - uses any terminal emulator program (built into Windows). **NB ZIF sockets not included.**

Order Ref	Description	inc. VAT ea
3123KT	ATMEL 89xxx Programmer	£32.95
AS3123	Assembled 3123	£47.95

Atmel 89Cx051 and AVR programmers also available.

PC Data Acquisition & Control Unit

Use a PC parallel port as a real world interface. Unit can be connected to a mixture of analogue and digital inputs from pressure, temperature, movement, sound, light intensity, weight sensors, etc. (not supplied) to sensing switch and relay states. It can then process the input data and use the information to control up to 11 physical devices such as motors, sirens, other relays, servo motors & two-stepper motors.

FEATURES:

- 8 digital Outputs: Open collector, 500mA, 33V max.
- 16 Digital Inputs: 20V max. Protection 1K in series, 5.1V Zener to ground.
- 11 Analogue Inputs: 0-5V, 10 bit (5mV/step.)
- 1 Analogue Output: 0.2.5V or 0-10V. 8 bit (20mV/step.)

All components provided including a plastic case (140mm x 110mm x 35mm) with pre-punched and silk screened front/rear panels to give a professional and attractive finish (see photo). with screen printed front & rear panels supplied. Software utilities & programming examples supplied.

Order Ref	Description	inc. VAT ea
3093KT	PC Data Acquisition & Control Unit	£99.95
AS3093	Assembled 3093	£124.95

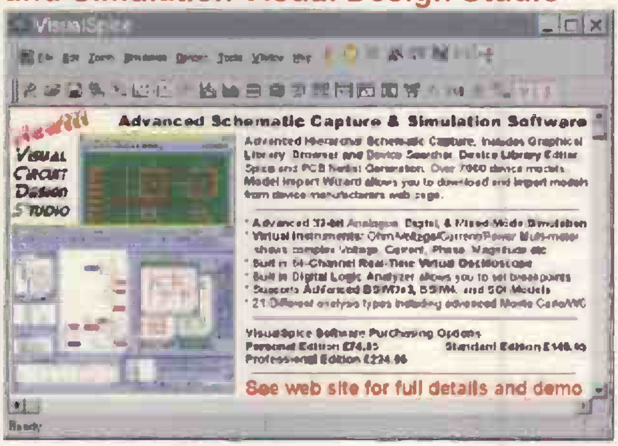
ABC Mini 'Hotchip' Board

ABC Starter Pack

Currently learning about microcontrollers? Need to do something more than flash a LED or sound a buzzer? The ABC Mini 'Hotchip' Board is based on Atmel's AVR 8535 RISC technology and will interest both the beginner and expert alike. Beginners will find that they can write and test a simple program, using the BASIC programming language, within an hour or two of connecting it up. Experts will like the power and flexibility of the Atmel microcontroller, as well as the east with which the little Hot Chip board can be "designed-in" to a project. The ABC Mini Board 'Starter Pack' includes just about everything you need to get up and experimenting right away. On the hardware side, there's a pre-assembled micro controller PC board with both parallel and serial cables for connection to your PC. Windows software included on CD-ROM features an Assembler, BASIC compiler and in-system programmer The pre-assembled boards only are also available separately.

Order Ref	Description	inc. VAT ea
ABCMINISP	ABC MINI Starter Pack	£64.95
ABCMINIB	ABC MINI Board Only	£39.95

Advanced 32-bit Schematic Capture and Simulation Visual Design Studio



Serial Port Isolated I/O Controller

Unit provides eight relay outputs and four optically isolated digital inputs. Can be used in a variety of control and sensing applications including load switching, external switch input sensing, contact closure and external voltage sensing. Programmed via a computer serial port, it is compatible with ANY computer & operating system. After programming, PC can be disconnected. Serial cable can be up to 35m long, allowing 'remote' control. User can easily write batch file programs to control the kit using simple text commands. NO special software required - uses any terminal emulator program (built into Windows). Screw terminal block connections. All components provided including a plastic case with pre-punched and silk screened front/rear panels to give a professional and attractive finish (see photo).

Order Ref	Description	inc. VAT ea
3108KT	Serial Port Isolated I/O Controller Kit	£54.95
AS3108	Assembled Serial Port Isolated I/O Controller	£69.95

Full details of these items and over 200 other projects can be found at www.QuasarElectronics.com

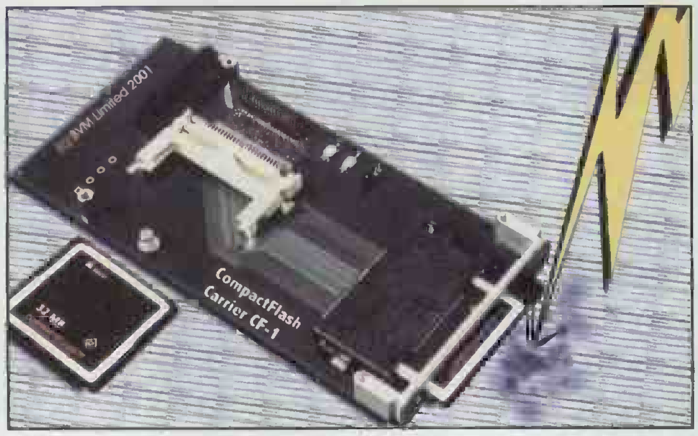
QUASAR ELECTRONICS Number 1 For Kits

www.QuasarElectronics.com

Credit Card Sales: 01279 467799

footprint, which requires more advanced manufacturing techniques, versus the traditional TSOP footprint. JEDEC completed the DDR333 memory device standard in May this year. Deployment is currently underway for 184-pin PC2700 registered DDR DIMMs.
SMT
Tel: 001 510 624 8291
www.smartmodular.com

CompactFlash carrier with up to 1Gbyte storage capacity



The CF-1 CompactFlash carrier from BVM holds two modules providing up to 1Gbyte of non-volatile storage. Designed as a PMC format module carrier can be used in host systems requiring only a vacant PMC site and an IDE controller interface. It is transparent to software and thus compatible with any operating system already supporting IDE disc drives such as Windows, Windows Embedded, Linux and various real-time operating systems. It can additionally be used as the boot device. Possible applications include simple data logging, data transport, providing a mechanism for field upgrade of embedded software, data backup, or as a means of adding non-volatile storage to a system.
BVM
Tel: 01489 780144
www.bvmitd.co.uk

DC-DC converter offers higher density with planar magnetics

Powerline is offering the ETA power block EP series of DC-DC converter modules that use a combination of planar magnetics and surface-mount construction to achieve their power density. The 50W EPB and 100W EDP series are available in a 58.4 by 61mm package with industry standard pin-outs. Input voltage range is 36-72V DC with a choice of five outputs from 3.3V to 24V DC. The 250W EPK series has additional input voltage range options of 20-32V and 220-400V, and are suited to use in industrial process control, telecommunications and distributed power systems. ■
Powerline
Tel: 01494 753800

Real-time digital filter

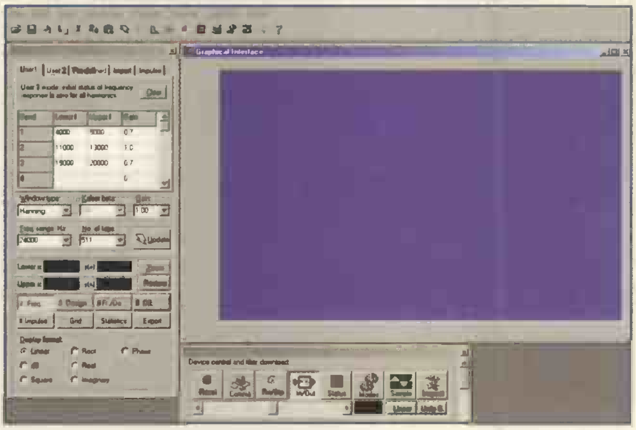
RTDF – a unique, integrated hardware/software system for designing, downloading and running very high performance filters in real time. Available only from *Electronics World.*

The RTDF 1.5 is a unique real-time audio-bandwidth digital filter with infinitely adjustable characteristics – all available at the click of a button. Filter design and execution is accomplished in two easy steps. In fact, you can have a no-compromise filter up and running within seconds.

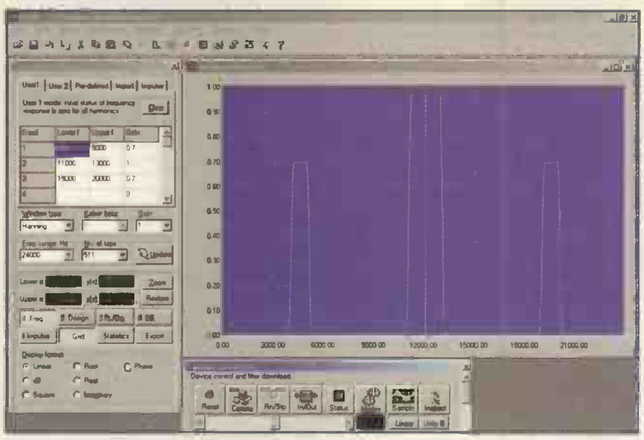
If you want to change the filter completely – low-pass, band-pass, high-pass or arbitrary – just repeat the two steps.

The RTDF filter system includes hardware based on an advanced digital signal processor, low-level firmware that implements the filtering operations, and a high-level PC-based software interface that designs the filter according to your requirements. Once a filter is designed, the software interface is used to download the filter to the hardware system via a serial link, where it is executed on demand.

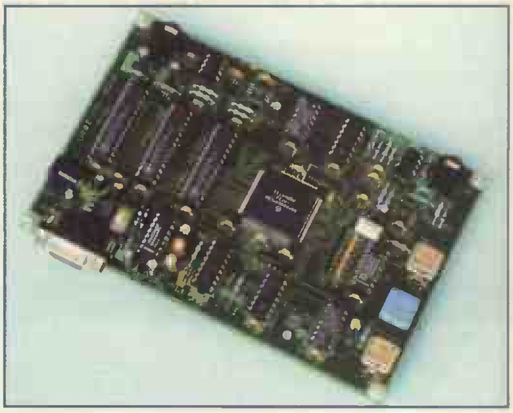
You don't need to know about digital signal processing theory or the mathematics associated with digital-filter design. But if you're a filter expert, you won't find yourself restricted by



Step 1 – Enter the characteristics of your filter, such as cut-off points and sharpness, in the Filter Design Interface Window on the left of the display.



Step 2 – Click on the Update button to view your result in graphical form, download it to the hardware module and run the filter from the hardware control panel – done!

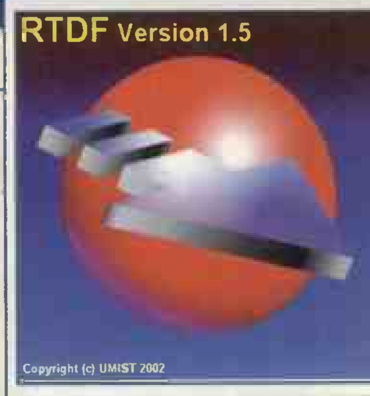


Filter hardware: a DSP56002 board with RAM and 16/18bit oversampling analogue converters for stereo i/o at up to 48kHz sampling.

RTDF - key features

- Runs under Windows 95, 98 or ME
- Generates FIR filters with a maximum of 1024 coefficients.
- Multiple pass, stop or arbitrary filters.
- Lower –3dB frequency 3.7Hz at 48kHz sample rate and 1.2Hz at 12kHz sample rate.
- Filter operates in single or dual channel modes.
- Import mode – ASCII import of any frequency response.
- Hardware module holds up to 16 filters, instantly selectable with one mouse click.
- Zero-phase distortion in the pass, transition and stop bands, ignoring input and output coupling.
- Choice of rectangular, Bartlett, Hamming, Hanning, Blackman or Kaiser Windows.
- Virtual control panel allowing run-time changes to filter gain and sampling rate.
- Includes frequency and time domain plots of filter performance.
- Frequency response plotted as linear, dB, square, root, real, imaginary or phase.
- Impulse, frequency and phase response exportable in a variety of formats (dB, power etc) as ASCII files for incorporation into standard spreadsheets.
- 18-bit resolution in single, 16-bit in dual-channel mode.
- Normal or turbo speed, software selectable.
- User selectable sample rates of 48kHz, 24kHz, 16kHz, 12kHz, 9.6kHz, 8kHz, 6kHz, 4.8kHz, 4kHz, 3.2kHz or 3kHz.
- Maximum input and output level 4V pk-pk

For more information, visit: http://www.umist.ac.uk/dias/pag/rtdf.htm



the easy-to-use interface. If you want to do it the hard way, you can even design your filter in long-hand then download the filter's frequency response as an ASCII file to the RTDF's control program!

The RTDF is a total filter solution. Due to its flexibility, it is particularly well suited to processing audio signals in real time. High-quality analogue signal conditioning and a dual-channel 16/18-bit resolution analogue-to-digital converter and digital-to-analogue converter provide a resolution sufficient for the most demanding applications.

In short, the RTDF brings the power of digital signal processing to any audio-bandwidth domain that requires high-performance electronic signal filtering. Applications include sensor linearisation, audio signal processing, signal analysis, vibration analysis, education and research in electrical, electronic and other physical sciences.

Low-pass, high-pass, multiple band-stop / band-pass filters may be combined to produce very complex filters for frequencies up to 24kHz.

The software can accept measured responses to define a filter template. This can be used for measurement equalisation or to search out signal signatures in noisy environments.

Since the filters are implemented using a symmetrical finite impulse response (FIR) method, no phase distortion occurs in the filtered signal – no matter how sharp the filter is. Because the processing module is so fast, it is possible to design filters with responses far beyond what is possible with traditional analogue techniques.

Windows software

The control program runs under Windows and provides a user-friendly filter-design tool that de-mystifies the process of specifying the filter. The filter design process simply becomes one of describing the desired frequency response.

The design package indicates the response that will be produced and any deviations from that specified. User designs may be stored for re-use and actual responses may be entered from measurements for simulation or equalisation purposes. Once designed, filters are calculated and downloaded to the hardware within seconds.

The software designs the filter according to the user's specifications. The filter is expressed as a set of FIR, zero-phase distortion coefficients or taps. Collectively, the coefficients of a filter are known as the impulse response.

The system's gain and sampling rate can be adjusted while the filter is running and you can switch instantaneously between a filtered or non-filtered signal.

Most importantly, the software includes a flexible filter design section. A window displays the frequency or impulse response of the realised filter in various formats. A hardware control section downloads a filter and provides for general communication with the filter module.

The DSP module

The hardware DSP module connects to the PC via a standard COM port using the cable supplied.

The 16/18-bit over-sampling dual-channel sigma-delta a-to-d and d-to-a conversion system can easily be set to any one of eleven sample rates, ranging from 48kHz down to 3kHz.

So how fast can the filter operate, and how many filter coefficients can it practically employ? The maximum number of taps at the highest frequency range of 24kHz, in single channel mode, is 527. At this range, the system is sampling at 48kHz. This represents a very sharp filter indeed.

Using a frequency range of 12kHz – sample rate of 24kHz – in single-channel mode, the system can operate a filter with a maximum of 937 taps. At any range below this, it can operate a filter with a maximum of 1024 taps. The performance of a 1024-tap filter is so extremely sharp that it is quite unlikely that you would ever need to use it.

In dual-channel mode, the maximum number of taps permissable at the highest frequency range of 24kHz is 191. With a frequency range of 12kHz , it is 397. Full details concerning tap numbers, frequency ranges and operating modes are provided with the on-line documentation. ■

Minimum system requirements

100 MHz PC running Windows' 95, 98 orME
SVGA display (800X600 pixels) or higher
CD ROM drive
10 Mbytes of free hard disc space
Serial port, capable of 19200 bit/s

System includes:

- Filter DSP board
- Windows filter design software on CD plus demonstration-filters
- Fully-worked help files – featuring tutorial
- Installation instructions
- Analogue i/o cables
- RS232 COM port download cable
- Power supply

Use this coupon to order your RTDF filter

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Make cheques payable to Cumulus Business Media.

Direction finder using VHF

If you use this direction finder within range of two VHF transmitters, you can determine your position – assuming you have a map of course. This project is equally useful as an example of good RF design though. It works at VHF and it involves receiving RF signals from two antennas using only one RF amplifier, eliminating the need for carefully-matched receivers. This is Ian Hickman's second article on the topic – there's one more to come.

The first article in this set of three described the two antennas and their associated RF stages. The output from each is split into two parts. One part is subjected to a 90° phase shift before being recombined with the un-phase-shifted component from the other channel.

This arrangement results in two versions of the signal being received. Their relative amplitude depends on the orientation of the two-antenna system relative to the azimuth direction of the station being received.

The advantage of this arrangement is that all of the phase-to-amplitude signal processing is accomplished at RF. As a result, only one superheterodyne receiver is needed to implement the rest of the system.

Figure 1 shows the full circuit diagram, including one of the two antennas plus RF stage together with the signal splitter and phase-delay cable blocks. There are two of these connected as shown in the block diagram of Fig. 1 in the previous article. The single receiver, which is shared between the two channels, is highlighted in Fig. 1 of this article.

Transformers T_1 and T_2 are hybrid types, representing the Σ boxes on the block diagram. Each is wound on a two-hole balun core. Any two-hole balun core is suitable, given that it will provide sufficient winding inductance at the operating frequency.

Thus the seven-turn winding should have an impedance that's large compared with 50Ω, say a reactance of j500Ω. With a seven turn winding, this means that a single turn should provide $j500/7^2$, or 10Ω approximately. So at the operating frequency of around 100MHz,

$$2\pi(100\times10^6)L=10$$

giving an inductance-per-turn figure, or A_ℓ, of 16nH.

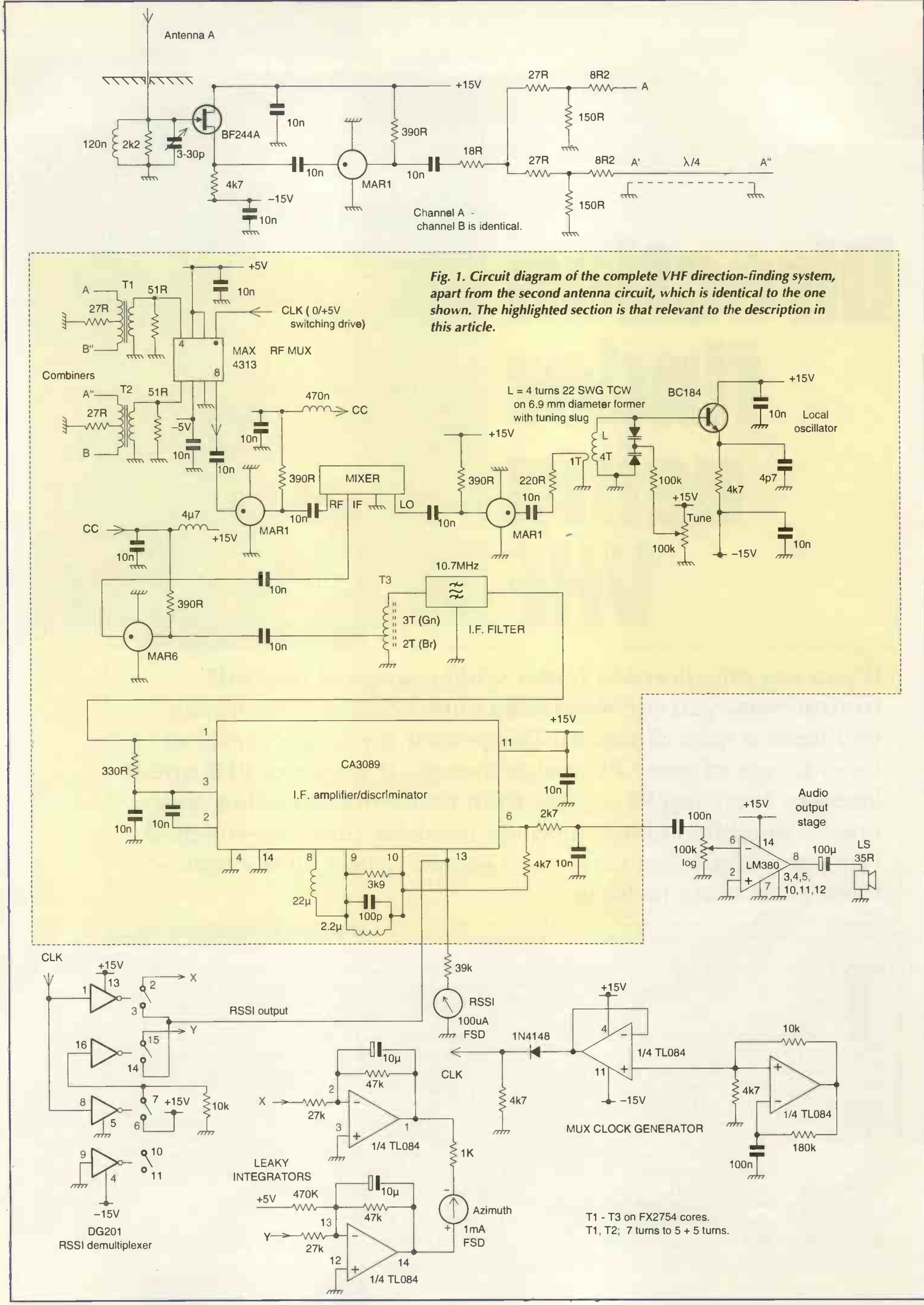

Fig. 1. Circuit diagram of the complete VHF direction-finding system, apart from the second antenna circuit, which is identical to the one shown. The highlighted section is that relevant to the description in this article.

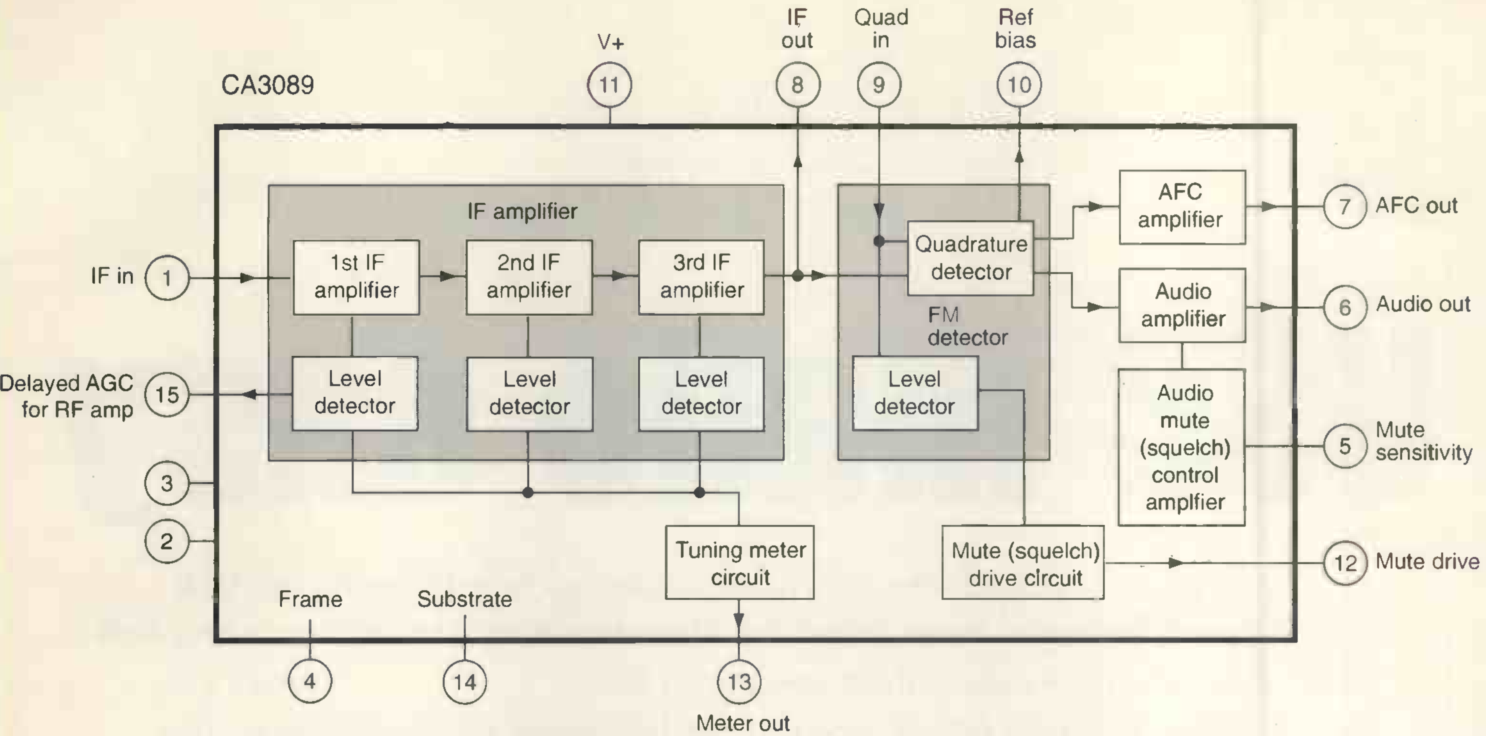

Fig. 2. Internals of the CA3089 integrated IF amplifier/discriminator IC.

The 5+5 turn windings should be wound with bifilar wire, or two strands twisted together, on top of the seven turn winding. Ideally, a hybrid sums the two inputs while providing a large degree of isolation between them, but with the simple construction used here, the isolation is rather limited, although still useful.

The two summed outputs, A+B″ and A″+B, are applied to the two inputs of a MAX4313. This IC incorporates a wideband video amplifier capable of drawing its input from either pin 4 of pin 5, under control of a standard logic signal applied to pin1.

Local 10nF decoupling capacitors are provided for this stage, as for other stages throughout the system. The output of the MAX4313 multiplexer amplifier is further boosted by a MiniCircuits MAR1 RF amplifier IC, before being applied to a passive double balanced mixer.

Mixer and local oscillator

A MiniCircuits type TFM-2 mixer was used, although many other types will be equally suitable. Like most passive double balanced mixers, the TFM-2 is designed to interface at 50Ω on all three of its ports.

The local oscillator signal is derived from a varactor tuned negative resistance oscillator using a BC184 transistor. For a description of how this versatile and useful oscillator works. there are details on this in the reference.

Tuning is accomplished by varying the reverse voltage on the varactor diodes by means of the 100kΩ 'Tune' potentiometer. My prototype used BB809 varactor diodes, but any VHF type of varactor should be suitable.

The slug of the coil is set to provide coverage of the international VHF broadcast band allocation from 88MHz to 108MHz. A one-turn coupling coil, close-wound at the earthy end of the main coil, taps off a small fraction of the local oscillator signal, without excessively loading the oscillator. Local oscillator signal is boosted by a MAR1 RF amplifier IC to provide a +7dBm drive to the mixer.

The 10.7MHz intermediate frequency (IF) output from the mixer represents the difference between the signal and the local oscillator. The local oscillator is designed to 'run high' so in order to cover the desired VHF FM broadcast band, the local oscillator needs to tune from 98.7 to 118.7MHz.

The IF strip

An MAR6 IC amplifies the IF output, which is then applied to a 10.7MHz ceramic filter. The filter is designed to run with 330Ω source and load impedances, so transformer T_3 is included. An autotransformer with five turns tapped at two turns provides a suitable ratio, transforming the 50Ω nominal output of the MAR6 to a little over 300Ω. However, as the primary has only two turns, a core providing an A_ℓ of around 200nH or more is appropriate.

Output from the IF filter is applied to a CA3089 IF amplifier/discriminator IC. This device has a high impedance input at pin 1, so a 330Ω resistor is used to terminate the filter's output.

Internal workings of the CA3089 are shown, in block diagram form in **Fig.** 2. In limiting, the device typically provides a signal-plus-noise-to-noise ratio well in excess of 60dB. Limiting typically commences with an input of 12μV.

With a 400Hz test input at ±75kHz deviation, distortion is typically 0.5% with the single tuned quadrature circuit connected between pins 9 and 10.

This can be reduced to 0.1% though, using a double-tuned quadrature coil. However, as the audio output is used merely to identify the station being received, a hi-fi standard of construction was not considered appropriate. In fact, the important output from the CA3089 in this application is not the audio, but the received signal strength indication, or RSSI, output. How this is used is described, together with the rest of the circuitry, in the third and final article. ■

Reference

1. Hickman, Ian, 'Negative-resistance oscillator', *Electronics World*, December 2000 pp. 977-980.

USB made easy

If you've looked into interfacing a design to a PC using the USB port, you may have found the idea daunting. But implementing USB is now now easier than you might think. Eddy Insam shows you why. This first article looks at the intricacies of the USB port. The second will illustrate how to develop a simple application in the form of an oscilloscope that will plug into your PC's USB port.

The universal serial bus, or USB for short, provides a new way of interfacing low and medium-speed peripherals to personal computers. That old workhorse, the RS232 connector, is fast becoming obsolete – even becoming absent in some recent purchased PCs.

The new USB standards are complex relative to RS232. To make things worse, there has been no easy route for designers wanting to add USB capabilities to their products that need to communicate with PCs. Fortunately, this situation is changing. New devices are becoming available that make this job easier. So easy in fact, that now you don't need to know anything about USB.

In this first article, I cover the basics of USB and show how it all works with the aid of simple sketches. In part two, I will present a simple oscilloscope as a practical example to show how easy it is to implement USB in your own designs.

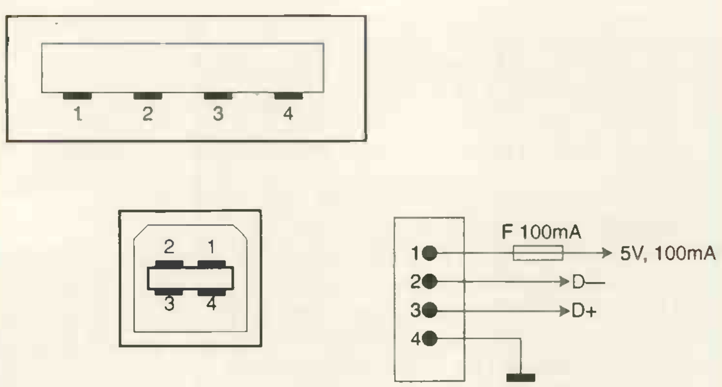

Fig. 1. USB connectors: These are known as type 'A' and 'B'. Looking closely inside a plug, pins 1 and 4 for the supply lines are a little longer than the other two for data. When the cable is plugged in, the supply lines are connected first, allowing the peripheral to power up before the data lines are connected. This also reduces the risk of electrostatic damage.

USB – in a nutshell

I will not be describing the inner workings of USB in great depth here. That's been done before. Besides, it is not necessary to understand USB in detail in order to use it. If you want more information, have a look at the excellent article by Tom Wong mentioned in the reference section. Here I will be covering only those aspects that are relevant to an applications designer.

USB uses a time-shared serial data stream. The PC acts as a master by polling all connected peripherals at regular intervals of one millisecond. Each peripheral responds by placing its data on the time-multiplexed bus at its allocated time within this 1ms frame. An addressing scheme allows up to 127 devices to be connected to the bus.

The current version of USB – namely V1.1 – supports two speed modes, 12Mbit/s and 1.5Mbit/s. These are selected in the hardware by tying one of the data lines to a supply via a pull-up resistor. The two speeds can live together, fast and slow speed bursts can co-exist on the same wire.

A four-conductor cabling system is used for USB. Two leads are used for power, 5V and GND, the other two for differential data. Unbalanced data patterns are used to transfer special 'end' codes. Different physical connectors are used for 'upstream' and 'downstream' connections. This is to avoid the user getting confused, **Fig. 1**.

Peripherals are not just wired together, but are connected to the PC via a tree of hubs. A typical PC will have an internal hub supporting two USB sockets on its back plane. If you need to attach more than two USB peripherals, you must purchase an external hub and attach it to one of the spare ports on your PC, then connect your peripheral to the new hub. This is somewhat like a mains extension lead.

The above is, as you would expect, only the simple version of events, with many extras and options under the surface. If you are new to USB, you should not be surprised to hear that there is already a new version of the standard with even more capabilities – Version 2. For the moment, I will be focussing only on the present version, Ver1.1.

The protocol

As I already mentioned, USB is a single-master bus, with all requests for activity originating from the PC. Data is transferred in packet bursts contained within frames separated by 1ms. Low-speed devices operate at a rate of 1.5Mbit/s, and the bit length is 667ns. Similarly, fast speed devices operate at 12Mbit/s and the bit length is 83.3ns.

Peripherals using USB have to synchronise their outputs to the frame start, so internal buffers are generally necessary to maintain a constant flow of data. The bit rate clock is recovered from the NRZI encoded data stream, Fig. 2.

A typical USB peripheral may have more than one 'endpoint'. Endpoints are nothing more than different destination registers sharing the same device address. Different endpoints can be used for initialisation and control, and for ordinary data transfers.

USB uses the term 'pipe' to denote a data transfer from the PC to a particular endpoint. To increase data rate, a peripheral may occupy more than one pipe at a time.

There are four basic methods of transferring information between a PC and a USB peripheral:

Control-transfer: This is used mainly to send control signals to the peripheral. These have high priority and incorporate inbuilt error protection. Control-transfer is mainly used for transferring initialisation information, but can also be used for general-purpose low speed data transfers. All USB devices must support control transfers.

Bulk-transfer: Storage devices mainly use this mode to transfer large amounts of data in a time independent manner. This is useful for printers, disk drivers etc. This method has low priority on the bus.

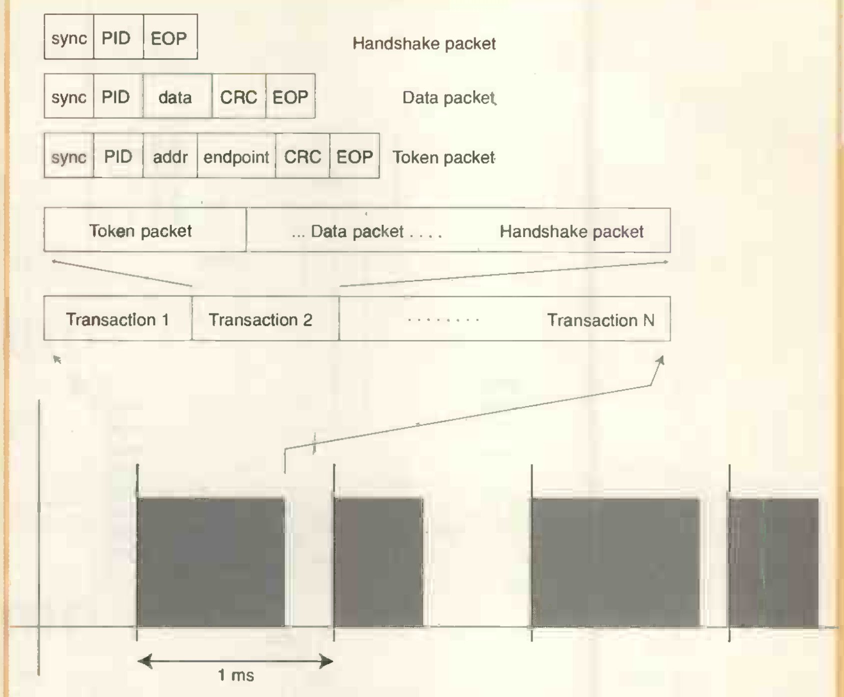

Fig. 2. All USB transactions are performed in 1ms frames initiated by the PC. Time division multiplexing is used to separate packets or transactions from different sources within each frame.

Interrupt-transfer: Used mainly by low-speed data peripherals such as mice and keyboards that need to send small amounts of data quickly and periodically to the PC.

Isochronous-transfer: Used by peripherals transferring large amounts of data at a defined data rate, e.g. sound cards. No error protection is included. The system must assume that some data may be lost.

Table. Summary of the four types of USB data transfer.

Transfer type	Control	Bulk	Interrupt	Isochronous
Data bytes/millisecond per transfer, maximum possible per pipe (full speed)	832, in thirteen 64-byte transactions	1216, in nineteen 64-byte transactions	64	1023
Data bytes/millisecond per transfer, maximum possible per pipe (low speed)	24, in three 8-byte transactions	not allowed	0.8, 8 bytes per 10 milliseconds	not allowed
Reserved bandwidth for all transfers of the type, max %	10%	none	90%, Int & Iso combined	90%, Int & Iso combined
Error correction?	Yes	Yes	Yes	Yes
Guaranteed delivery rate?	No	No	No	Yes
Guaranteed latency (max time between transfers)?	No	No	Yes	Yes

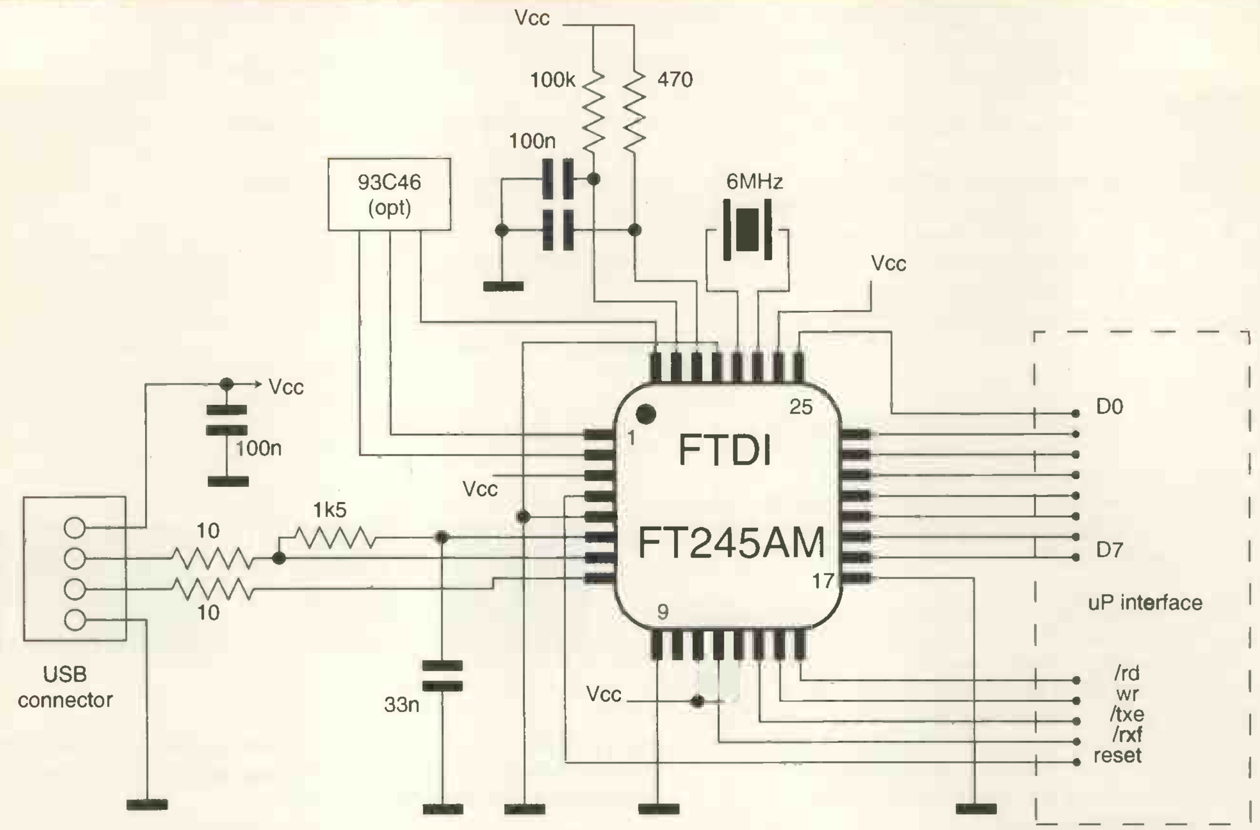

Fig. 3. This is all the front-end hardware you need to add USB to your project. It connects to your micro via eight parallel lines and four simple read/write and control lines. The FT245 chip contains an internal 384 byte FIFO character transmit buffer and a 128 byte receive FIFO buffer. The transfer rate can be up to 1 megabyte per second. The optional EEPROM can be used to store manufacturer's unique ID information.

The above are summarised in the **Table**. Even though USB is rated at 12Mbit/s, the final effective data rate in some cases can be quite low. For an error protected control link using the low speed bus for example, the guaranteed data rate is limited to only 800 bytes per second.

The PC side of the interface

Most PCs now include USB connector sockets at the back as standard. Support for USB is via kernel-level device drivers in the operating system.

If you do not have a driver installed, the USB port will not be available to you. This is very different from the good old times of parallel and serial ports where you could access the interface chips directly from your applications program. Each USB peripheral requires a driver of its own 'class'. These low-level drivers are usually supplied with the peripheral when purchased.

Peripherals are recognised one by one by the operating system during the boot-up sequence, which also causes the right drivers to be loaded. USB is a 'hot-wire' protocol. The PC can also recognise when a peripheral has been plugged or unplugged during normal work, and is able to load or unload the corresponding driver at the same time. This makes USB more or less transparent to the user.

In case you have not thought about the situation, most BIOSes will also include some form of built in primitive USB support for keyboard and mice, so these can be recognised as such before the boot sequence and before Windows starts.

Windows includes a number of 'ready-made' USB drivers for interfaces going under the generic name of 'human interface devices', or HIDs. These consist of mice, keyboards, pointers and joysticks. This allows a generic product, such as a mouse, to be plugged in without having to install a special driver.

The installation procedure is very simple. When the peripheral is plugged in, a polling signal by the hub causes Windows to send signals on the USB asking for identification. The peripheral responds with its own product and vendor IDs, or PIDs and VIDs as they're known. Windows then searches its directories for the correct driver assigned to that particular peripheral. If it cannot find one, it pops up a message requesting the user to install one.

The drivers are usually supplied on floppy or CD. Once the driver is installed, the application program carries on as normal.

How to implement USB in your design

If you wanted to add an RS232 interface to your product, you only needed to write simple comms software to drive or emulate a UART, add a small amount of RS232 level-shifting hardware and then write some simple protocol to transfer the data, perhaps using some simple error correction scheme.

Adding USB is a lot more difficult. You have few choices. You could obtain a micro controller with built in USB capabilities and develop your project around it, i.e. using its hardware functions and instruction set. On the other hand, you could buy a USB device designed as a peripheral, and interface it into your project. In both cases, you need to understand quite a bit about USB.

Many manufacturers offer microprocessors with built in

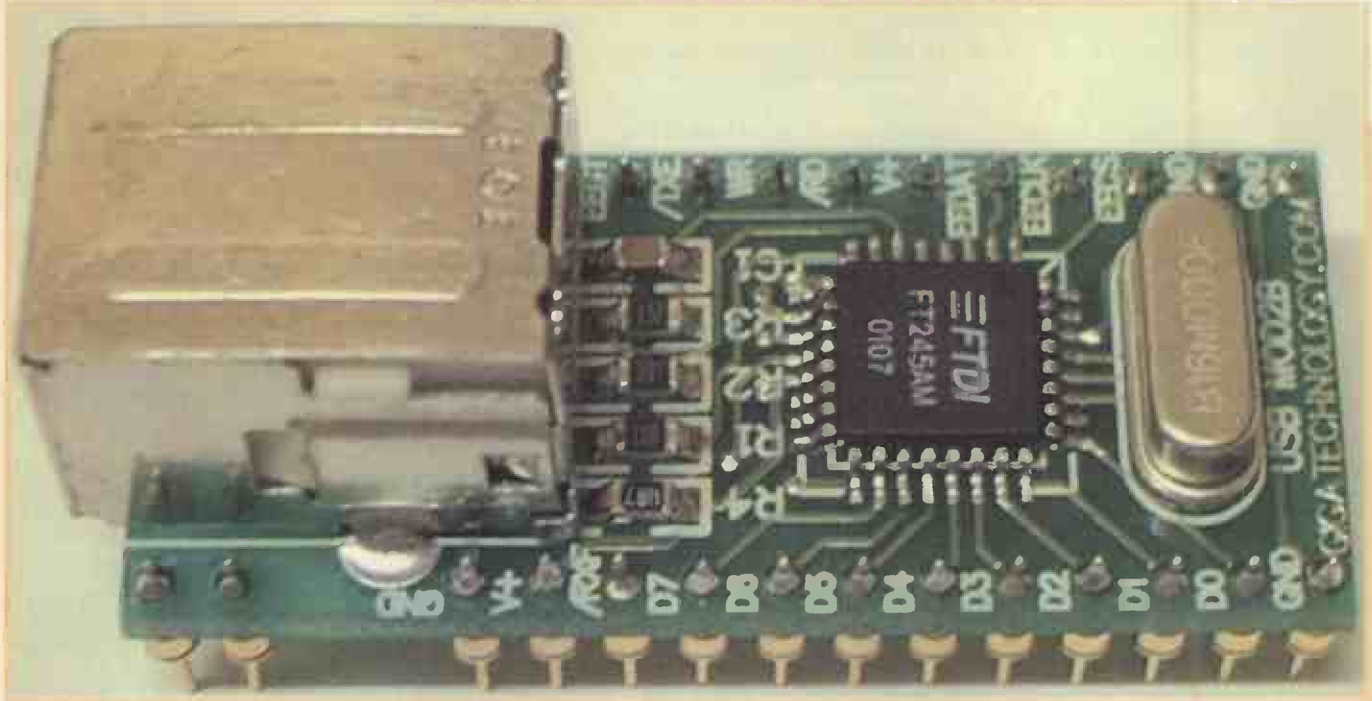

Fig. 4. The piggyback module from FTDI. Some extra components underneath the board add internal reset and decoupling. The module can be plugged into a breadboard for development.

USB capabilities – Cypress, Microchip and Philips among them. The simplest of these has just enough memory and processing power for the simplest of tasks, i.e. keyboard or mouse. More sophisticated USB processors are built around more advanced cores such as the 8051. These have a varied range of features.

USB support is provided in the form of firmware subroutines, which you link into your own code. In practice, the USB add-ons can take quite a big chunk of the microprocessors memory space and power.

Your involvement also includes creating the product and vendor description tables. Most of the information here will be provided by the chip manufacturer, and may need to be customised for your mode of operation.

You will need to obtain your own unique vendor and product IDs. These numbers make your peripheral uniquely recognisable by the operating system in order to load the right driver. For development and testing you can use the IDs allocated to the USB interface chip you are using. This is perfectly legitimate. More on this later.

The USB cable can provide some power for the peripheral. However, you should be conversant with the USB specifications, which allow for up to 500mA to be drawn when the peripheral is active, but only 500μA when inactive. This means you have to provide for means of switching the power off while the USB interface is in the suspend state.

As I'll be discussing soon, there is now the option of incorporating USB without any frills. This becomes no more complicated than adding an eight-bit parallel port buffer to your micro. You need know nothing about USB, or even how it works. So, you can more or less forget everything I've said!

Software at the PC end

Having developed your USB hardware and firmware on your peripheral, you will still need to write a bit of software to go at the PC end. You will need to write a low-level driver. You will need a different driver for each type of platform.

Fortunately, the various Windows versions have some things in common, so the same driver could be used for Windows 98, ME and 2000. Native NT does not support USB. A different set of drivers will be needed for Mac and Unix/Linux however.

Windows supports a range of basic ready made human-

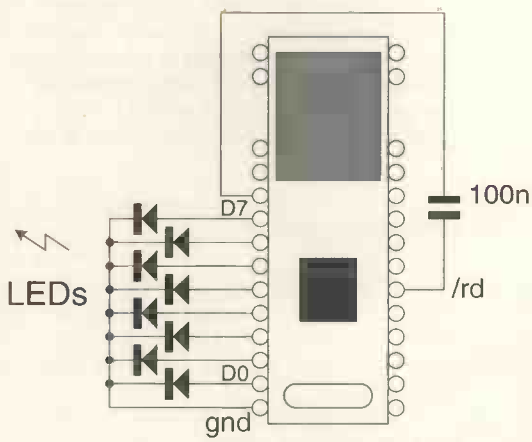

Fig. 5. USB Christmas lights: A simple test rig for the module. Just connect it to your PC running a standard terminal comms program set for the newly allocated COM port. The lights will flash as you type characters. The capacitor is needed to derive a short RD pulse from the RXEmpty signal.

interface device drivers off the peg, so if your project is one of these, call yourself lucky as you will not need to craft your own driver. In addition to HIDs, there are standard USB classes for sound cards, frame grabbers and printers. Most likely though, your project will not fit into any of these categories, so you will need to brew your own.

If you need to develop your own driver, there is some limited help available. The DDK Device Development Kit from Microsoft contains templates and samples of drivers for the most common USB applications. In addition, many samples and information notes are available for downloading from the Internet.

Still, writing a device driver is not a trivial exercise. Poorly written drivers can cause unexpected crashes and can make life very difficult for the inexperienced programmer.

Writing the driver is not the end of the story. You will need to adapt your application program to communicate with the driver. Windows programmers can use the *CreateFile* and *DeviceIOControl* API functions to communicate with USB peripherals. Fortunately, these are relatively easy to use.

Ready-to-bake USB

As I mentioned before, there is now a simple no brains way of adding USB to your project. By this, I mean at both ends – the PC software too is reduced to the lowest level of simplicity.

The design example used in this pair of articles is based on the FT8U245AM device manufactured by FTDI Ltd in Scotland, (*www.ftdichip.com*). This chip comes as a 32-pin surface-mount MQFP miniature package.

To work, the chip only requires a 6MHz crystal, some passives and the USB socket, **Fig. 3**. It interfaces to an external microprocessor via an 8-bit parallel port and four read write and control lines.

From the micro's point of view, the FT245 chip looks like a 384-byte first-in-first-out buffer, or FIFO, for transmit, and a 128 byte FIFO buffer on receive. The FT245 works in the USB full speed mode and can transfer data at around a megabyte per second.

Implementing the module

Using this chip is as easy as connecting a 74HC245 buffer to one of your micro parallel ports – maybe this has something to do with the naming of the device. The FTDI chip hides all the USB intricacies from the user.

To transmit a byte, you place your 8 bit data on the parallel bus, poll the 'transmit-buffer available' signal, /TXE, until it goes low, and then pulse the WR control line to push your byte into the transmit FIFO.

To receive a byte, you poll the 'byte available' signal RXE. This tells you that a byte is available for reading. You read it by pulsing the RD control line. That is all there is to it.

To make life even easier, a piggyback module known as USBMOD2 is available from FTDI. This incorporates the FT245 chip, a 6MHz crystal, a USB socket, and the required passive components onto a 23 pin piggyback module. This is ideal for prototyping as it can plug directly into a 32 pin bread-boarding socket, **Fig. 4**.

You may be wondering whether you still need to be involved in writing device drivers. There is no need, the drivers supplied by FTDI makes the USB interface appear to your PC as a regular comms port. Therefore, if your PC project software was written with the serial port in mind, you will have little work to do.

Instant satisfaction – testing the module

On receiving the module, it took me less than a few minutes to install the driver on my Windows PC. I was able to go to the Control Panel, under Device Manager, and see a new entry (COM3) added to the listing of my available comms ports.

I plugged the module into a breadboard plug-in strip. I then connected a few LEDs directly to the data ports, and a 100nF capacitor to crudely generate a RD pulse from the RXE line, **Fig. 5**. No power supply was necessary as the USB module is powered from the cable itself.

I then went to my PC and opened a simple terminal program set to communicate with COM3, typing some characters. The LEDs flickered in perfect harmony. Total time, less than fifteen minutes. Not bad. ■

The author

Dr Eddy Insam is a consultant in innovative applications of telecommunications and specialises in graphics and signal processing. He can be reached on *edinsam@eix.co.uk*.

Obtaining the parts

The USB module is available from FTDI in the UK for £23.50 inc VAT and pp. The company has local Agents in the US and Australia. Check their web site *www.ftdichip.com* for more up to date details on pricing and availability. An alternative device FT232 provides a serial output instead of a parallel one. This could be used as a direct replacement for systems using legacy RS232 interfaces. Full information is available from the FTDI web site.

For more information

Tony Wong 'Understanding USB' *Electronics World*, November 1999. A very good article describing the inner workings of USB.

http://www.usb.org – the web site of the USB organisation.

http://www.ftdichip.com – for more information on the USB chip and module.

J Hyde 'USB Design by Example' Wiley, NY 1999. *http://www.usb-by-example.com*

J Axelson 'USB Complete' Lakeview Research 1999. *http://www.lvr.com*

The last two references are good reference books on USB. They contain many examples and background information.

Next month, Eddy describes the circuit required to turn this module into a simple, fast voltmeter and oscilloscope.

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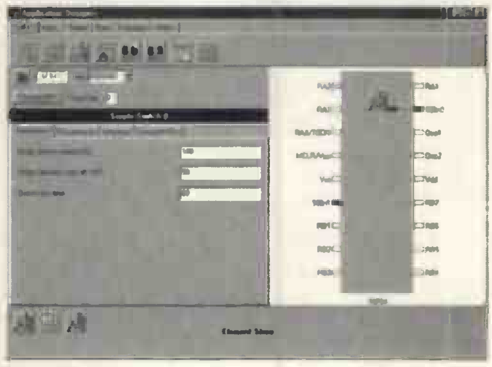

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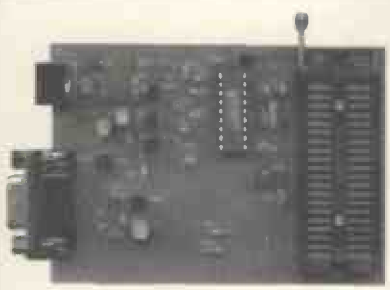

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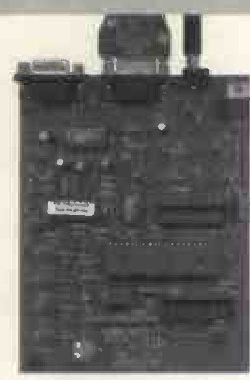

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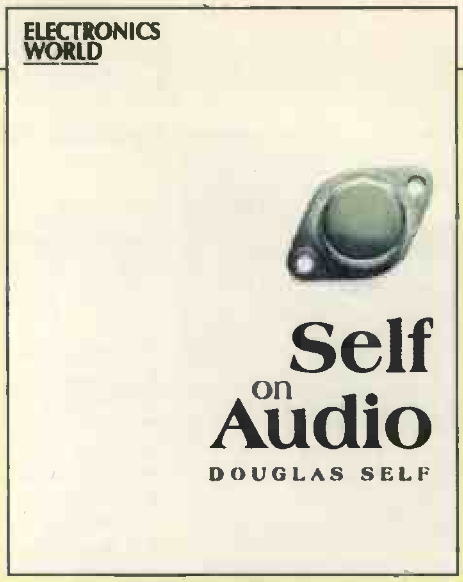

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Douglas Self has been writing for Electronics World and Wireless World over the past 20 years, offering cutting-edge insights into scientific methods of electronics design.

This book is a collection of the essential Electronics World articles, covering twenty years of amplifier technology but with a very strong bias towards more recent material. The articles include self-build projects as well as design ideas and guidance for the professional audio designer. The result is a unique collection of design insights and projects - essential for all audio designers, whether amateur or professional.

Contents: Introduction; PRE-AMPLIFIERS: An advanced preamplifier MRPI; High-performance preamp MRP4; Precision preamp MRP10; Moving-coil head amp; Preamp '96 I; Preamp '96 II; "Overload Matters" (RIAA overload); Balanced line inputs and outputs, part 1; Balanced line inputs and outputs, part 2; POWER AMPLIFIERS: FETs less linear than BJTs; Distortion in power amplifiers 1-8; Distortion residuals; Trimodal part 1, 2; Load-invariant power amp INVAR.DOC; Common-emitter amps; Two-stage amplifiers; SPEAKERS: Excess speaker currents; Class distinction (amp classification); Relay control; Power partition diagrams; Audio power analysis.

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Class-G mode indicator

Just how useful is Class-G? How often does it actually draw power from the upper supply rails? To answer these questions you don't need an oscilloscope – just the simple LED circuit presented here. Designed by Doug Self.

My Class-G amplifier PCB has an extra feature not documented – for the usual reasons of space and time – in the original articles. This is a mode-indication circuit that illuminates an LED whenever the amplifier switches over to draw power from the higher (or outer) supply rails. The circuit has a fast-attack slow-decay characteristic so that even short excursions into the high-power domain are clearly signalled.

The first question is how to define exactly what constitutes entering the high-power mode. I have taken this to happen when the commutating diodes become reverse biased; there is no doubt then that all the instantaneous power is being drawn from the upper supply rails through the outer power devices.

The circuit is shown in **Fig. 1**; its operation is as follows. When the output moves sufficiently positive the amplifier enters the high-power mode and Q_{18} turns on. The commutating diode D_{12} becomes reverse-biased, D_{14} conducts, and Q_{22} is turned on via R_{41} which limits the base current. The collector current of Q_{22} rapidly charges C_{20} through R_{43}, which again limits the current flowing to an amount that will not inconvenience Q_{22}.

Transistor Q_{23} now turns on and current flows through dropper resistor R_{45} to illuminate LED, LD_1. Resistor R_{42} makes the discharge time more predictable as most of the discharge current is flowing through a resistor rather Q_{23}'s base, with the beta-variations that this implies.

Provision is made for mounting the indicating LED directly on the PCB, where it acts as a useful indication that all is working properly; not everyone wants a comprehensive display of flashing lights while soaking up lute music.

If however you do want to mount the LED on the front panel a position is provided for a two-pin connector. This is not a good place to put it if you planning double-blind listening tests to determine the merits or otherwise of Class-G.

The LED's 0V connection must be made to a 'dirty' part of the grounding system and not mixed up with clean signal grounds. A separate wire back to the junction of the power supply reservoir capacitors is all that is required. Failure to get this right is likely to lead to crunching noises on the audio as the LED goes on and off.

Possible enhancements

The indicator circuit takes the power for its LED from between the outer supply rail $+V_2$ and 0V. The value and power rating of R_{45} can be adjusted to suit different $+V_2$ voltages and different brightness requirements. This is straightforward, providing you allow for the additional voltage drop in R_{44}.

For example, with a +50V rail, a 2V LED voltage drop and a desired LED current of 10mA, the total resistance required is

$$\frac{V}{I} = \frac{50-2}{0.01} = 4800\Omega$$

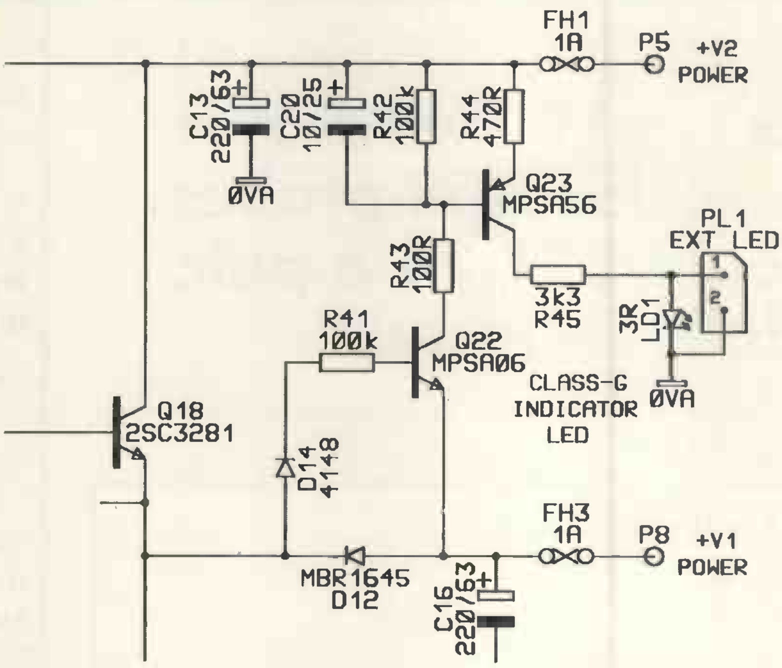
Subtracting the 470Ω of R_{44} gives R_{45}=4330Ω. Normally the nearest E12 value would be chosen, i.e. 3900Ω.

Power dissipated in R_{45} can now be found from $P=I^2R$, and is 390mW. A half-watt resistor will do nicely.

The value for C_{20} given here – 10μF – provides a decay time of approximately 500ms, to give a good clear indication even on fast transients. Reducing this to 2.2μF gives much snappier operation if preferred.

The indicator presented here is of course unipolar- it only respond to positive excursions into the high-voltage region. A fully comprehensive monitoring system would have a similar circuit working on the negative supply side. If it is built purely as the complement of the positive monitor, it would be a quite separate circuit driving its own LED.

Alternatively, it would be easy to connect the two monitor circuits together so that both activated the same LED. ■



Find out how much use your Class-G power amplifier is making of the high-voltage supply with this LED indicator. It has a fast turn-on, slow turn-off characteristic, making fast transients easy to spot.

Note!
Currently, the input capacitor for the Class-G amplifier is 1nF. This could be too demanding for some preamplifiers. If you have problems in this area, try reducing it to 100pF.

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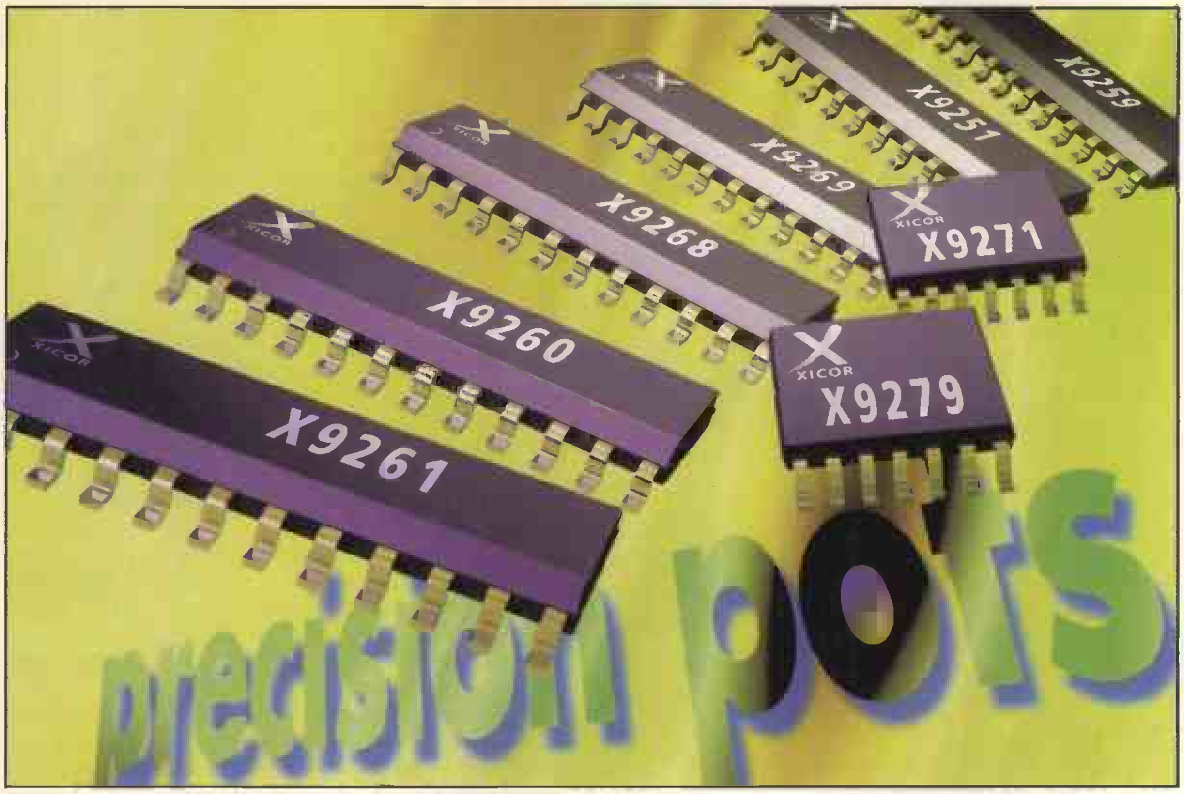


What signal conditioning circuit could possibly be easier to design than a dual-channel dc amplifier with a common tracking-gain control? Here, Xicor's Brian Gough explains how it is done using just one single-section potentiometer – or a DCP.

Two channels – one gain pot

The obvious way to control the gain of two channels simultaneously is to regulate the gain of each with matching sections of a dual-element, ganged potentiometer. Unfortunately though, ganged potentiometers – particularly the precision multi-turn variety – are pricey and often hard to find.

The circuit described here offers a viable alternative. It avoids the liabilities of dual potentiometers by controlling the gain of both channels with just one ordinary single-section potentiometer, marked *P* in **Fig. 1**.

The scheme hinges on the arrangement of *P* with its wiper terminal grounded. This set-up creates two mechanically linked but electrically independent variable resistances: KR and $(1-K)R$. Resistance *K*'s value represents *P*'s wiper position. Therefore, it goes from 0 to 1 as *P* is rotated from full counterclockwise – i.e. zero gain – to full clockwise, which is maximum gain.

Resistance *R* is *P*'s total element resistance. The net result for both op-amps A_1 and A_3 is a transfer function linear in *K*:

$$\frac{V_{OUT}}{V_{IN}} = K\left(1+\frac{R_G}{R}\right) = KG$$

With the example component values shown, $G=11$. Yet virtually any gain factor greater than unity can be accommodated by a suitable selection of resistors and op-amps.

Why this formula applies to A_1 is easy enough to see. Positive feedback from A_1's output to *P*'s CCW terminal results in constant current drive to the potentiometer, given by $I=V_1\div R$. So, the signal at A_1's non-inverting input is equal to:

$$I\times K\times R=\frac{V_1}{R}\times K\times R=K\times V_1$$

This voltage is boosted by A_1's non-inverting gain of

$$G = 1 + \frac{R_G}{R}$$

to produce overall gain as a function of K given by,

$$\frac{V_{OUT}}{V_{IN}} = KG$$

The story behind A_3's operation is slightly more complicated. Surrounding A_2 and P's CW terminal is a topology that produces a signal of,

$$V_2(1-K)\left(1+\frac{R}{R_G}\right)$$

at A_2's output. After attenuation by A_3's feedback network to $V_2(1-K)$, this voltage appears at A_3's inverting input. So the differential voltage seen by A_3 is,

$$V_2 - V_2(1-K) = V_2 \times K$$

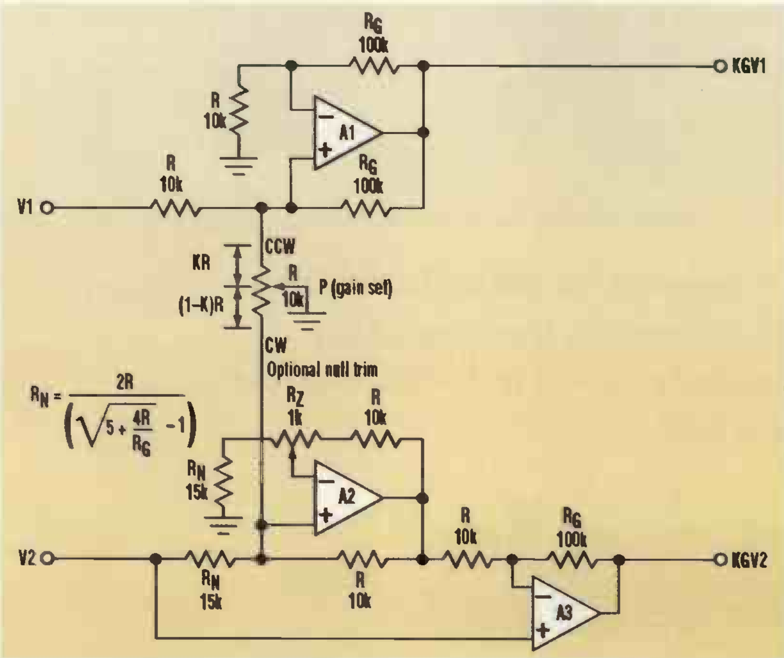
When amplified by A_3's gain of,

$$1 + \frac{R_G}{R} = G$$

this voltage becomes $V_2 \times K \times G$. Op-amp A_3's gain, accordingly, is equal to KG, just like A_1's.

For applications that are particularly sensitive to a non-zero gain error at K=0, an optional null-trimmer, R_Z, may be used to accommodate tolerances in the various resistance ratios. This ensures that A_1's and A_3's gains will simultaneously vanish when P hits its full counter-clockwise rotation.

Component selection criteria for potentiometer P include a low resistance-element temperature coefficient for good gain stability and a low wiper resistance for low interchannel crosstalk. Fortunately, potentiometers possessing the quality – and price points – sufficient that make all of this trouble worthwhile generally have excellent characteristics for these two design parameters.



Controlling the gain of two channels using one potentiometer does away with the need for a matched, ganged potentiometer – which can be very expensive.

Stereo audio applications

The application of this circuit to manually control gain in stereo/audio and similar contexts where P is a mechanical potentiometer is obvious. But the idea also has utility when P is an electronic digitally-controlled potentiometer (DCP) like the Xicor X9xxx series.

For example, P might form the basis of an automatic gain-control loop in applications like an ALC for stereo/audio recording. To provide ALC loop feedback, one channel's signal magnitude, or the sum or the greater of both channels' average signal magnitudes would be compared to a set point. The signal would drive both channels to the same tracking/balanced gain. ■

Xicor company background

Xicor designs, develops and markets a wide variety of programmable mixed-signal integrated circuits and nonvolatile memory products used in networking, computing, communication and industrial applications.

The company's products include digitally controlled potentiometers and system management ICs that allow system designers to digitally control analog functions in signal processing, microprocessor monitoring and power management.

Xicor product, corporate and financial information is readily available on the world-wide web at http://www.xicor.com.

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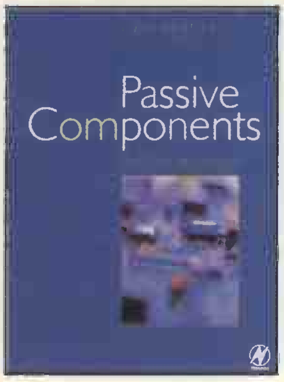

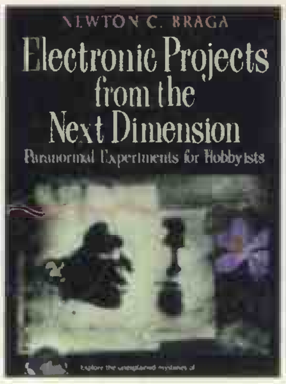

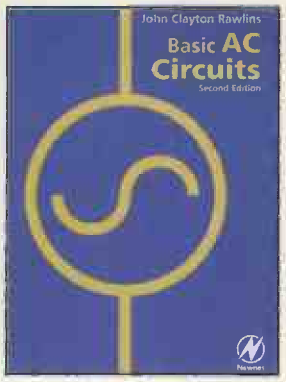

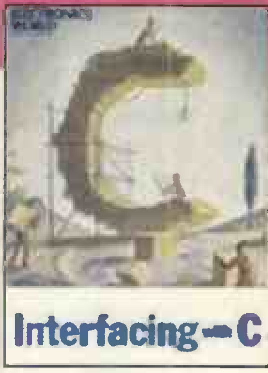

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e-mail j.lowe@cumulusmedia.co.uk using subject heading 'Letters'.

DAB debate

I am glad someone else thinks that DAB sound quality leaves something to be desired, referring to Dave Kimber's leader in the August 2001 issue.

I thought it was me, either having some sort of reception problem or being over-fussy!

I have had a Videologic tuner for some months. So far only the national channels are available at my location. I live about 25 miles from Holme Moss and Emley Moor, in what has always been a good reception area for TV and FM, on high ground, with a clear 'view' to the transmitters. Despite this, and despite using a five-element YAGI, I can only light up six units on the strength meter.

While I could no doubt improve on this by mounting a bigger antenna on an external pole – there isn't room for a bigger one in my loft area – what happens when my local DAB multiplex eventually starts up?

According to the web sites, it will transmit from different locations from the nationals. Will I need an aerial rotator, or am I missing something here?

On the subject of sound quality, I can only say that DAB seems extremely variable. The obvious comparison is between Radio 3 and Classic FM. For a start there is a 4-to-6dB difference in audio level, Classic being louder. However, Classic's quality seems much poorer.

Certain sounds, such as solo female voice, oboe, and trumpet often have a nasty edge to them; a type of granular distortion is the only way I can describe it.

In addition, limiter pumping tends to be *very* audible, even more so than on FM. This begs the question, is DAB technology capable of coping with local radio methods of operation, i.e. 'self-op' presenters who are more concerned with their content than with watching PPM needles!

I am assuming that Auntie still has some technical operator involvement in the Radio-3 programme chain. Even if that is not true, its quality is much more acceptable.

Another question springs to mind. How many sessions of code/decode are involved between say a CD at the studio and my ears?

In my local-radio days we used BT NICAM to get from studio to transmitter. Even for good old analogue FM, we were decoding from CD, re-coding to NICAM and then back to analogue again, before transmission. If you then simply add a third digital hop in MPEG-2 this cannot be good for quality. Or do they code in MPEG-2 at the studio these days?

Richard Barnes
Via e-mail

Try lighting a fire without any matches...

In the December issue's leader, entitled, 'Igniting the spark and fanning the flames', Patrick Gaydecki wrote an increasingly rare upbeat comment about 'fun and excitement' in scientific interests.

The Science Club for Youth that we ran for a decade or two saw some hundreds of youths pass through it. The Club had a modicum of the 'fun' Patrick intimated, plus the democracy of running it, and the Youth Hostelling, measuring the speed of light, operating the Amateur Radio station (G3SRE) – you name it. The young people involved were actually very keen.

But I assure you that the rapidly growing anti-science ethos latterly put an end to such possibilities. Many parents increasingly said things like, "I don't think it's healthy for him to fiddle about with all those dangerous bits of wire," and failed to encourage.

The Youth Service eventually indicated that such a Group was 'rather elitist' anyway, and took the room back. (The lads had named it 'The Faraday Room...') Thus the Club closed, and for the life of me, no one since has shown the slightest enthusiasm to restart something like it, in spite of lots of suggestions, etc.

Dr Gaydecki is quite right about the continuing lack of women getting involved with amateur and professional science activities too. In my university maths and electronics lectures, the number of men to women was static at around 45 men to 3 women, year after year.

The anti-technology ethos is really strident now. You should have heard the uproar at the public meeting about the proposal to erect a 4W mobile base station system on our village church tower. I felt that if many of the public there found out about my 50 watt 430MHz amateur radio station and mast, I would be lynched!

I wouldn't dare mention running an electronics/radio club for their kids – I would be treated like a child abuser!

Dr Ken Smith
Via e-mail

Reverse engineering a PCB

Drawing the circuit diagram from a PCB is not the easiest of tasks. The following procedure will make this less difficult.

Put the PCB copper side down in your scanner and make an image, adjusting the controls for a good contrast between copper and board. Alternatively, if you have a digital camera, take a shot of the copper side.

Open the image in your image processing software and flip it either horizontally or vertically.

You now have what is effectively an x-ray view of the board from the component side revealing the wiring.

Print this out magnified say 1.5 to 2 and then draw the components in place.

Producing a circuit diagram should now be easy.

Tony Meacock
Norwich , Norfolk

RIAA – a rare insight

I spent most of my career working for Ampex. Near the end of the analogue recording era, I was a frequent visitor to recording studios and disc-cutting rooms.

I learnt that disc-cutting engineers were respected and celebrated beings, whose special attributes included 'golden ears'.

I saw – and heard – the practice of listening to the tape on the cutting-room monitors and then setting the knobs on the equalisers and other devices in the chain to the cutting head.

Then, the master disc was cut and played back through the cutting room monitors, usually using an SME pick-up arm and whatever pickup cartridge the cutting engineer favoured.

In the rare event that the playback was considered unsatisfactory, the equalisers would be re-adjusted and the disc re-cut, but I hardly ever remember this happening.

I suppose that the play-back system equalisation would have followed the RIAA curve with an accuracy typical of good hi-fi equipment of the time, such as Quad. But the equalisation used for cutting discs was whatever the cutting engineer's experience had convinced him sounded good.

In my youth, I had spent hours measuring the frequency response of RIAA pre-amps, but in the studio world, I never heard tolerances on the standard curve mentioned! ■

Justin Underwood
Much Marcle
Herefordshire

Gas pipe wave guide?

In his book, "Wireless Telegraphy and Broadcasting", published in 1924 (ex. *IEE Journal* 1922), H.M. Dowsett quotes a note written, in 1880 by Prof., David Edward Hughes reporting on a meeting with a deputation from the Royal Society. The purpose of the meeting was for Hughes to demonstrate that he could receive signals from a small spark coil over a distance of several hundred yards using as a receiver a carbon powder microphone or a thermopile in series with a Bell telephone.

Hughes was of the opinion that the signals were transmitted by conduction through the air but the others thought the results were due to induction. Apparently neither side would yield and the meeting broke up in a rather acrimonious atmosphere.

Hughes said ... "they hardly paid any attention to the experiments, even to the one working through the gas pipe in Portland Street to Langham Place on the roof."

When he says, "working through the gas pipe" does he actually mean that? If so, it would be, perhaps, the first demonstration of a wave-guide. Does anyone know anything to the contrary?

Incidentally, Arthur Mee's Children's Encyclopaedia, in chapter five, shows a picture of Hughes walking down Portland Street with a telephone receiver pressed to his ear and a policeman looking at him somewhat suspiciously. This is the only place that I have encountered the picture. Does anyone know where the original resides?

S F Brown
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Anritsu MW98A Time Domain Reflector.
PI available - MH914C 1.3 - MH915B 1.3 - MH913B 0.85 - MH925A 1.3 - MH929A 1.55 - MH925A 1.3GI - MH914C 1.3SM - £500 + one P.I.
Anritsu MZ100A E/O Converter.
+ MG912B (LD 1.35) Light Source + MG92B (LD 0.85) Light Source £350.
Anritsu MZ118A O/E Converter.
+MH922A 0.8 O/E unit + MH923 A1.3 O/E unit £350.
Anritsu ML96B Power Meter & Charger £450.

Anritsu MN95B Variable Att. 1300 £100.
Photo Dyne 1950 XR Continuous Att. 1300 - 1500 £100.
Photo Dyne 1800 FA. Att £100.
Cossor-Raytheon 108L Optical Cable Fault Locator 0-1000M 0-10kM £200.
TEK P6701 Optical Converter 700 MC/S-850 £250.
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HP 4274 FX LCR meter – £1,500.
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HP 75000 VXI Bus Controllers + E1326B DVM-quantity.
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HP PREAMPLIFIER 8447A 0.1-400MC/S – £200. Dual – £300.
HP PREAMPLIFIER 8447D 0.01-1.3GHz – £400.
HP POWER AMPLIFIER 8447E 0.01-1.3GHz – £400.
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MARCONI 2610 True RMS Meter – £450.
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MARCONI 6950-6960B Power Meters + Heads – £400-£900.
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RACAL 1792 COMMUNICATION RX – £500 early – £1,000 late model with back lighting and byte test.
RACAL 1772 COMMUNICATION RX – £400-£500.
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TEK 7000 PI's – 7A11-7A12-7A13-7A18-7A19-7A22-7A24-7A26-7A29-7A42-7B10-7B15-7B53A-7B80-7B85-7B92A-7D15-7D20.
TEK 7000 – 7S11-7S12-7S14-7M11-S1-S2-S3A-S4-S5-S6-S51-S53-S54.
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HP 3585A 20Hz-40MC/S – £3,500.
HP 3588A 10Hz-150MC/S – £7,500.
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HP 8568B 100Hz-1.5GHz – £4,500.
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TEK492P 50kHz-21GHz OPT 1-2-3 – £3,500.
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HP 8901B AM FM Modulation ANZ Meter – £1,750.
HP 8903A Audio Analyzer – £1,000.
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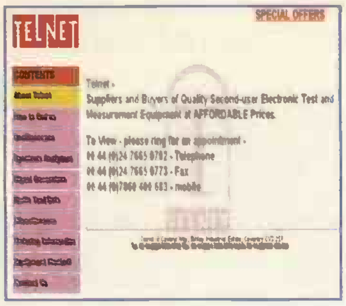

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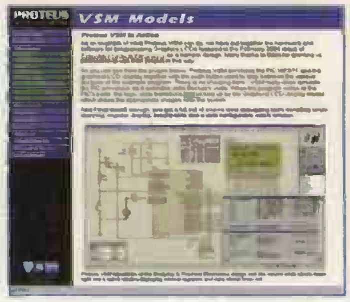

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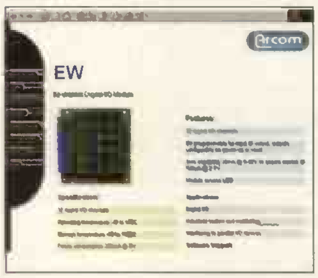

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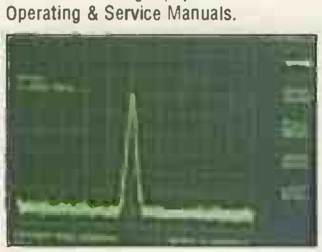

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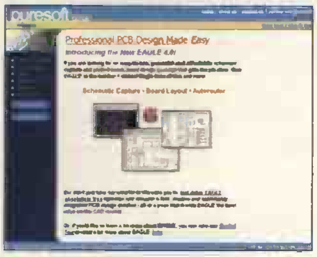

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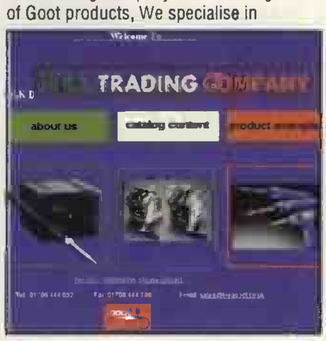

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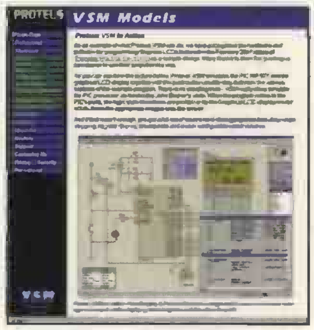

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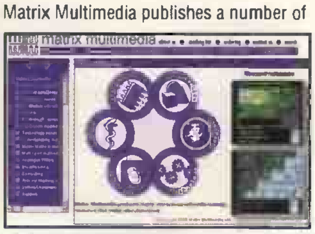

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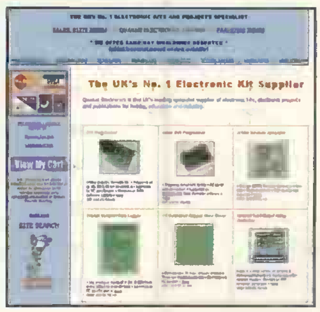

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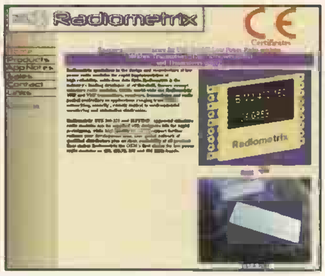

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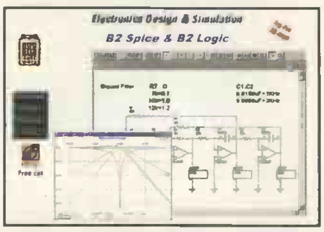

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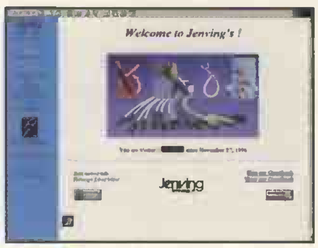

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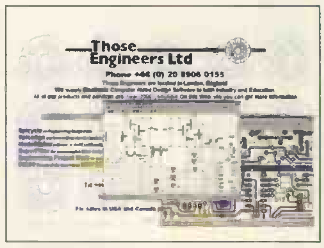

Working evaluations of SpiceAge mixed-mode simulator, Spicycle PCB design tools and Superfilter demo (synthesises passive, active, digital filters). Tech support, sales links and price list.

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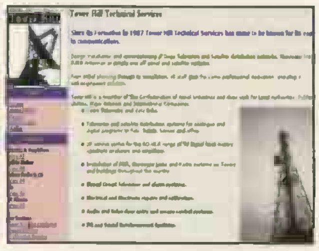

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UK MAILING LIST GROUP

http://www.egroups.com/list/uktvrepair

Following on from the newsgroup discussion last month there is a UK Email group for TV technicians where you can send an Email to everyone in the group. There's just over 30 people in the group at present. For more details and how to reglster look at the egroup home page. Just a general comment though - you do have to be careful who you give your Email address to so that you can avoid "spamming" - that is getting lots of unwanted Email about dubious Russian site (amongst others).

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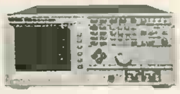

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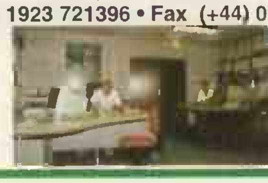

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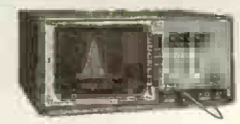

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