AUDIO ANALYSER

NEW SERIES
DIGITAL DESIGN
PART ONE

CONSTRUCTIONAL PROJECTS

GENERAL FEATURES

NEWS AND COMMENT

OUR SEPTEMBER ISSUE WILL BE ON SALE FRIDAY, 14 AUGUST 1981

NEW RANGE OF PROJECTS

NEXT month sees the introduction of a new range of possible projects for PE. Over the past years one area of electronics in which we have only participated in a limited way has been radio communication. We have published various receivers but never actively encouraged people to go "on the air" with publication of an amateur bands transmitter. PE has always seen this area of electronics as being rather specialised and generally separate from our normal projects, which can usually be built and used by anyone, anywhere without restriction. Use of amateur bands equipment, requiring as it does the passing of a (relatively simple) examination before a licence can be obtained, tends only to appeal to those who are licensed. Such people are well catered for in other areas of the electronics press.

With the introduction of CB the whole scene is about to change. Of course a licence will still be required to operate CB equipment, but the licence will not require any qualification or technical ability. It will be more akin to a TV licence, though no doubt it will place certain restrictions on users. Because of the new laws CB radio communication will soon be readily available to anyone that wishes to use it and, with this in mind, we feel it part of our duty to readers to keep up with the times. We will therefore be bringing you news, views and projects covering the technical side of CB.

If you are not in the least bit interested in CB please don't worry, it won't be swamping PE, it will simply be yet another area of electronics that we cover. Our coverage is always expanding and changing anyway, as electronics in general forges ahead. We won't be carrying endless rig reviews, publishing pages of club directories or reams of chat about the band, etc.

Our first "CB project" was the 27/28MHz Converter, published in the March issue. This project proved to be very popular and was highly acclaimed by readers. Since then we have published a Speech Processor (April issue) which had a variety of uses—CB included—and next month we start a short series on the PE Ranger 27FM (see page 40 for more details). This highly versatile CB rig will be one of the first CB transceiver projects published and, because of its ingenious design, should be a leader in the field. (It will also be interesting to licensed amateurs as it can be built to use on the 28MHz band, though that is not our primary target market.) The PE Ranger 27FM has been designed by the same highly respected contributors as the other two projects mentioned.

As we have said the publication of this design in PE is the true introduction of a new range of possible projects, designed to be used with the UK CB system; its popularity will be an indication of reader interest in this area.

EXTRA

Next month as an extra, and to enable us to still carry our normal range of projects, plus all our regular features, a free 20-page booklet will be supplied with all UK copies. The booklet will be an *Introduction to Legal CB* in the UK and will form a valuable handbook to anyone contemplating using CB. This free gift serves a twofold purpose: It provides a separate ready reference to CB which is self contained and therefore easier to keep handy and use, than a short series carried in our normal pages. It also prevents the magazine from being top heavy on CB for a few months, and so being of less value to those with other interests.

Mike Kenward

Technical Queries

We are unable to offer any advice on the use or purchase of commercial equipment or the incorporation or modification of designs published in Practical Electronics.

All letters requiring a reply should be accompanied by a stamped, self addressed envelope and each letter should relate to **one published project only**.

Components and p.c.b.s are usually available from advertisers; where we anticipate difficulties a source will be suggested.

Back Numbers

Copies of some of our recent issues are available from: Post Sales Department (Practical Electronics), IPC Magazines Ltd., Lavington House, 25 Lavington Street, London SE1 OPF, at 95p each including Inland/Overseas p&p.

Binders

Binders for PE are available from the same address as back numbers at £4·30 each to UK or overseas addresses, including postage and packing, and VAT where appropriate. Orders should state the year and volume required.

Subscriptions

Copies of PE are available by post, inland or overseas, for £11·80 per 12 issues, from: Practical Electronics, Subscription Department, Oakfield House, Perrymount Road, Haywards Heath, West Sussex RH16 3DH. Cheques and postal orders should be made payable to IPC Magazines Limited.

FIDELITY... ENTERS CTV MARKET

Fidelity Radio have taken a major step into the television market with the introduction of their first colour television; the CTV 14R. This is a fourteen inch portable set with infra red remote control, designed and produced by the company at its Acton factory.

The development of the CTV 14R follows the notable success achieved by Fidelity with its mono portables; the FTV 12 and the TVR 120 introduced last year.

The set which features a single board chassis has a power consumption of only 65 watts and a power output of 2 watts. The tube is a 90 degree in-line CRT with self convergence and full pin cushion correction. A surface acoustic wave filter is also incorporated into the design.

Controls consist of a push button step through channel selector with six preset tuning controls, red l.e.d. channel indicators, volume, brightness, contrast and colour controls.
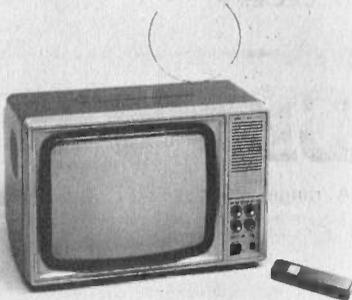
The set which measures 450×310×370mm weighs 11·5kgs and can be powered by a standard car battery with the aid of an adaptor.

Advance sales of the receiver have already outstripped the first year production target of 40,000 sets. The retail of the CTV 14R is expected to be around £200.

Fidelity have also introduced four new budget hi-fi products, new radio and clock radio ranges as well as their twin cassette system which includes a four waveband stereo FM radio.

The first of the two cassette decks is for record and playback and can be used to record from the second deck, radio, microphones and auxiliary whilst the second deck is for playback only.

The unit has an l.e.d. stereo indicator and twin power output l.e.d. meters. It has mono stereo and stereo wide selection with a total music power of 5 watts and rotary controls operate volume, balance and tone whilst there is an auto stop on the tape.

There are built in twin condenser microphones, facilities for external microphones and microphone mixing; sockets for DIN input and output, jack input and output, external jack speaker stereo headphone and a.c. mains input.

The twin cassette which is competitively priced has dimensions of 432 × 250 ×115mm and takes 6 HP2 or equivalent battery types.

Fidelity Radio, Victoria Road, London NW10.
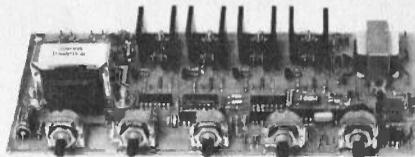
CHASER

L & B Electronic have introduced two new lighting modules into their current range.

The first is the Programmable-8 which is an eight channel chase-sequence unit which allows the user to program and store up to 128 patterns. With the program running, the complete sets are displayed in sequence and there is control over the lamps "on and off time" (movement from one pattern to the next). At the end of the program, the module re-cycles to the start and repeats. A pre-settable d.i.l. switch can reduce the program size to 64, 32 or 16 patterns.

The unit, which is CMOS based, utilises a RAM, is zero suppressed and requires no further power supplies or fusing. The fascia panel, anodised blue, comes fixed and complete with the module. The unit is priced at £114·90 plus VAT.

The second module, aptly named the Multi-4, provides a variety of four channel chase effects: forward, reverse, random direction, sound modulation, sound on chase and various combinations of these. The unit also incorporates audio a.g.c. if required, and control over the chase speed and odds of random change.

The use of potentiometers as "control zones" eliminates the need for mode switching. The module will accept virtually any sound signal, is zero suppressed and requires no further supplies or fusing. Price: £54·90 including VAT, Panel, knobs, l.e.d.s, switch: £9·70 inclusive.
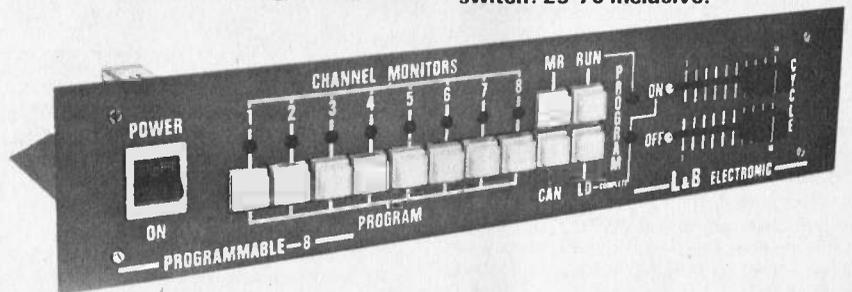
MARKET PLACE

MUSIC PROGRAM

Music Students who happen to have access to a 48K Sharp MZ80K computer will no doubt be interested to learn that Newbear have produced a program to aid them with their studies.

Newbear say that their "Music Composer—Editor" program gives a very sophisticated way of writing and illustrating composed music both visually and audibly. The notes are displayed as the editor is used, and the command mode has 27 directives. Full instructions are included in the program including a "Help" mode (one wonders if it draws the students attention to such compositional 'nasties' as parallel fifths or doubled thirds!).

The price of the Music Composer is £10·00 plus VAT. Further details are available from Newbear Computing Store, 40 Bartholomew Street, Newbury, Berks. (0635 30505).

CLUB EXPANSION

The ZX80 Users Club, which was founded last year as an independent user group, has now been expanded to cover the ZX81 microcomputer.

The Club caters for all types of user from the beginner through to the more experienced "object coder" wishing to expand his system. They produce a regular newsletter containing articles on basic computing, home computing, educational computing and of course ZX-80/81 hardware and software. A special feature of the magazine is the "Cambridge Hot-Line" with the latest news direct from Sinclair Research Ltd.

A software bank has been set up to provide members with programs at a minimal cost. The Club also provides technical support for all members.

The annual membership fee which includes the cost of the newsletter and softwear bank index is £6 for UK members and £10 for overseas members.

Further information will be supplied to prospective members on receipt of a stamped addressed envelope. ZX80/ZX81 Users Club, PO Box No 159, Kingston Upon Thames, Surrey.

VIDEO SYNTHS

The Chromascope C-101 video synthesiser is an electronic version of the kaleidoscope producing multi-coloured, moving patterns on a TV screen. The C-101, which simply plugs into the UHF socket of the TV, can also be used with hi-fi systems where the images will respond to the frequency of the music. The C-101 is priced at £295 including VAT.

The Chromascope P-135 (pictured above) is a professional video synthesiser which will accept visual sources such as a TVR or live camera. The unit incorporates external images in patterns and can superimpose patterns, shapes and colours onto the image provided and it can also put colour onto a black and white image.

Special effects facilities include: a mix fader, a sequence timer and a modification timer. Individual patterns can be held indefinitely and the shapes, textures and colours can be modulated by music.

The price of the P-135 is £675 inc. VAT. CEL Electronics Ltd., River Way, Harlow, Essex (0279 418611).

ROBUST CASE RANGE
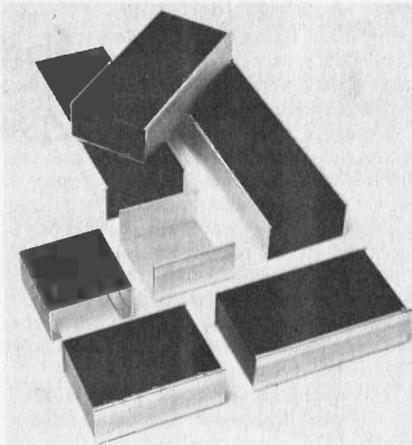
A range of robust yet attractive multi-purpose cases has been introduced by Zaerix Electronics. Known as Tuboxes, their design is simple and therefore cost-effective.

The base comprises of an extremely rigid anodised aluminium U-section extrusion 70mm wide by 40mm deep, into which slides a 1·5mm thick PVC coated cover with integral ends, secured by four self-tapping screws. The cases are available in 6 lengths ranging from 70mm to 220mm.

Zaerix suggest that the cases are ideally suited to hand-held equipment applications such as walkie-talkies or in-field test gear. Prices for Tuboxes range from £2·59 to £4·15, and they are available from Zaerix Electronics Ltd., 46 Westbourne Grove, London W2 5SF. (01-221 3642).

TRANSAM CATALOGUE

Transam Computers have just released a new catalogue covering their complete range of Tuscan Computer hardware.

The Tuscan is a flexible microcomputer system which is based around the S100 bus, the CP/M disk operating system and the Z80 microprocessor. Transam are now in full production with their Tuscan system with prices ranging from £299 for a 16K starter kit which includes the main board, 12A power supply and a 56 key keyboard plus 8K of user RAM and 8K TCL resident Basic to £2,225 for a full dual 8in. disk drive system.

The catalogue also covers an extensive range of plug-in S100 boards available from Transam which, generally speaking, break down into prototyping boards, memory expansion boards, video boards, I/O boards and disk controllers. Two new boards from Transam are the high resolution video board, produced using the state of the art "Graphics Display Processor" from Thomson CSF with high speed 512×512 graphics capabilities, and the brand new 64K Static Memory Board, using the recently developed 2K×8 CMOS Static Rams, pin for pin compatible with the popular 2516 Eproms.

A large range of disk drives, media, video terminals and monitors, printers, plus details of Eprom erasers and programmers, is included.

Transam's current hard disk development work, enabling 10 and 20 Megabytes of hard disk to be connected directly to the Tuscan, plus the new high resolution graphics capability, will make it one of the most powerful micros running CP/M 2.2.

The catalogue is available from Transam Products, 59–61 Theobalds Road, London WC1 for 40p plus a stamped addressed envelope.
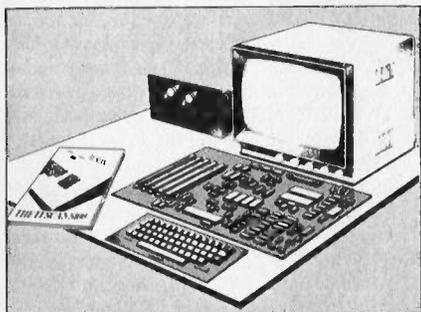
Mixer Amplifier
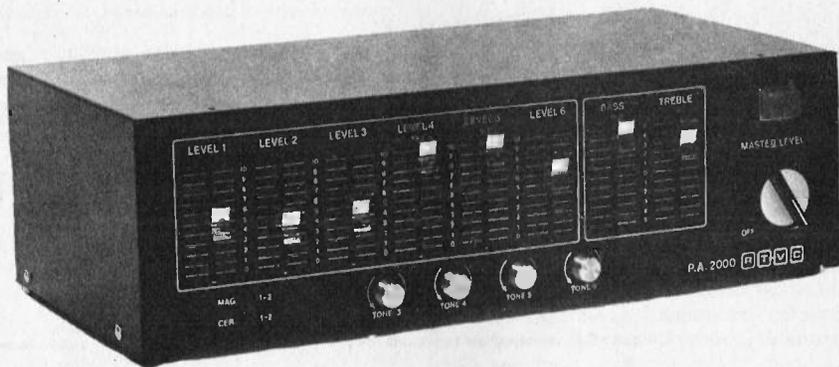
RT-VC have added to their range of ready built equipment with the recent introduction of the PA 2000 Mono Mixer Amplifier.

With an output of 50 watts r.m.s. into 4 ohms, it has six inputs—two pick-up (ceramic or magnetic), two mic, and two auxiliary. There are Master bass and treble controls, and individual treble controls on inputs 3–6.

The PA 2000 is guaranteed for one year from purchase date, and is priced at £39·95. Post and packing on mail orders is £3·70. For further information contact: RT-VC, 323 Edgware Road, London W2 (01-723 8432).

SONY LAUNCH BUDGET VIDEO RECORDER

Sony, whose top-of-the-market C7 video recorder has been a runaway success since its launch last year, have recently launched an attack on the lower end of the video market with the introduction of their C5 unit.

Though it is a budget model, the C5 still retains the attractive styling of the C7, and the designers have not sacrificed every feature of the C7—C5 has picture search, a fairly comprehensive timer, and in deference to economy, corded remote control. It does not have a freeze frame facility, but has a pause control which produces a still mono picture.

The C5 uses a rotary two head helical scan and has a maximum recording time of 3 hours 35 minutes with an L-830 tape.

The recommended retail price is £513, though most dealers are expected to sell it at around £450.

CLOCK/RADIO

The latest portable clock radio from Hanimex features a 2-band AM/FM radio and a quartz analogue clock in one cabinet. The HAR 001 comes complete with a carry pouch and has two independent circuits so that the operation of the radio does not affect the function of the clock. It has a wake to music facility and can be used either at the bedside, the office or kitchen. The HAR 001 should retail at under £20 complete with its pouch.

Hanimex (U.K.) Ltd, Hanimex House, Dorcan, Swindon (0793 26211).

MARKET PLACE

WANDER MIKE

The latest microphone from TVC Audio Systems is a cordless model which uses an antenna instead of the usual plug and lead.

All that is needed to operate the "Wander Mike" is an FM radio tuned to a pre-set frequency which acts as a receiver.

The mike is finished in polished stainless steel and comes complete with stand attachment, batteries, instruction leaflet and five metres of cable with a jack plug in case the user wishes to use it with a conventional sound system.

Watford Electronics are supplying the Wander Mike at a special introductory offer price of £39·50 ex VAT and p&p.

Watford Electronics, 33–35 Cardiff Road, Watford, Herts.

VOICE SYNTHESISER

The latest voice synthesizer from Easicomp is the EC-01 Phonetic Voice Synthesizer which is a completely self contained unit to phonetically synthesize continuous speech of unlimited vocabulary from low data rate inputs.

The speech is synthesized by combining phomemes (the building blocks of speech) in sequence and the EC-01 contains 64 such phomemes which are accessed by ASCII code. The unit has been designed to provide the computer user with a low cost flexible speech interface which requires the minimum of hardware support. An on board buffer of 1024 characters optimises the use of the EC-01 and allows long messages to be output to the unit without "tieing up" the processor whilst the message is being output.

To simplify the task of generating the code needed to produce the speech the unit accepts the phomemes as a mnemonic code. Two inputs are available for either an external amplifier or a 500mW speaker and a programmable inflection enables different meanings of the same word or phrase to be achieved.

Various versions of the EC-01 are available for most of the popular machines together with the connectors to simply plug in and go.

The unit which is priced at £149·95 ex. VAT and p&p is available from Easicomp Ltd, 57, Parana Court, Sprowston, Norwich NR7 88H.

Countdown . . .

Please check dates before setting out, as we cannot *guarantee* the accuracy of the information presented below.

BEX Portsmouth July 15–16. Centre Hotel. **K**
BAEC Amateur Electronics Ex. July 18–26. The Shelter, Penarth Esplanade, S. Glam. **B9**
Sussex Mobile Rally July 19. Brighton Race Course. **A4**
Microcomputer Show (& Seminars) July 29–Aug. 1. Wembley Conf. Centre. **O**
Microcomputer Show July 30–Aug. 1. London. **O**
Harrogate Int. Fest. of Sound Aug. 15–18. Royal Hall Exhibition Centre & Hotels. **X**
Solar Energy Exhibition Aug. 23–28. Brighton. **M**
BEX Cardiff Sept. 3–4. Centre Hotel. **K**
Business & Light Aviation Sept. 3–5. Cranfield Airport. **Z1**
Microprocessor Workshop Sept. 7–8. University of Liverpool. **D**
Laboratory Sept. 8–10. Grosvenor House, Park Lane, London. **I**
Personal Computer World Show Sept. 10–12. Cunard Hotel, London. **M**
West of England Electronics Show Sept. 15–17. Bristol Exhibition Centre. **O**
Microtest Sept. 21–24. University, Kent. **G1**
Microtest Sept. 21–24. (Symposium), Kent University, Canterbury. **G1**
Business Telecoms & Electronic Office Sept. 23–25. Royal Lancaster Hotel, London. **O**
BEX Edinburgh Sept. 30–Oct. 1. Assembly Rooms. **K**
Viewdata Oct. 6–8. Wembley Conf. Centre, London. **O**
BEX Bristol Oct. 14–15. Exhibition Centre. **K**
Video Show Oct. 16–18. West Centre Hotel, London. **Z1**
International Business Show Oct. 20–29. NEC, Birmingham. **A2**
Testmex Oct. 27–29. Wembley Conf. Centre, London. **T**
Computer Graphics (Ex. & Conf.) Oct. 27–29. Bloomsbury Centre Hotel, London. **O**
BEX Southampton Nov. 4–5. Polygon Hotel. **K**
Viewdata & TV User Nov. 4–6. West Centre Hotel, London. **Z1**
Breadboard Nov. 11–15. Royal Hort. Halls, London. **T**
IFSEC (Fire & Security) Nov. 17–19. RDS, Dublin. **V**
Compec Nov. 17–20. Olympia, London. **Z1**
Electronics Nov. 17–20. Olympia, London. **I**
BEX Plymouth Nov. 18–19. Holiday Inn. **K**

Intron Nov. 24–26. RDS, Dublin. **V**
Electronic OEM Assemblies Feb. 2–4 1982. Royal Hort. Halls, Westminster, London. **T**
Laboratory Edinburgh March 30–31 1982. Assembly Rooms, George St. **E**
Electronic Test & Measurement March 30–April 1 1982. The Forum, Wythenshawe. **T**
Sensors & Systems March 30–April 1 1982. The Forum, Wythenshawe, Manchester. **T**
Laboratory Manchester April 7–8 1982. New Century Hall, Corporation St. **E**
All Electronics Show April 19–21 1982. The Barbican, City of London. **E**
There are **Continuous Events & Permanent Exhibition** at the National Micro & Electronics Centre. **L1**

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A1	Inst. Electronics, Rochdale, Lancs
A2	Hart Browne & Curtis. ℰ 01-439 8556
A3	Sybex, 18 Rue Planchat, F-75020 Paris
A4	A. Baker. ℰ 07912 5327
B2	Brintex. ℰ 01-637 2400
B5	Robin Bradbeer, N. London Polytechnic
B7	Modmags. ℰ 01-437 1002
B8	Baroness International. ℰ 01-734 2907
B9	BAEC, Penarth, S. Glam. ℰ 0222 707813
C	Barry College Radio Soc. ℰ 0222 565656
D	Liverpool Univ., Brownlow Hill, PO Box 147
D1	Infopress, 58 Fleet St., London
E	Evan Steadman, Saffron Walden. ℰ 0799–22612
F1	ARS Electronica, 34 High St., Saffron Walden
G1	SERT, 8 Charing Cross Rd., London
I	ITF, Solihull. ℰ 021-705 6707
K	Douglas Temple, Bournemouth. ℰ 0202-20533
L1	World Trade Centre. ℰ 01-488 2400
M	Montbuild Exhibitions. ℰ 01-486 1951
O	Online, Northwood, Mddx. ℰ 09274 28211
Q	Exhibitions for Industry. ℰ 0883 34371
T	Trident, Tavistock. ℰ 0822 4671
V	SDL. ℰ Dublin 763871
V1	Jack Tootill, Ipswich. ℰ 0473 44047
X	Exhibition & Conference, Harrogate. ℰ 0423 62677
Y1	Norman Gutteridge, Birmingham. ℰ 021-422 9787
Z	BETA Exhibitions. ℰ 01-405 6233
Z1	IPC Exhibitions, Sutton. ℰ 01-643 8040
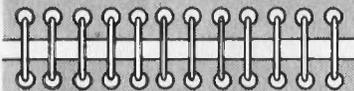
INDUSTRY NOTEBOOK

By Nexus

Capital Performance

The Electronic Engineering Association's recently published annual report is full of good news of the capital equipment sector which EEA represents through 36 leading companies in full membership and two associate members.

The retiring President, Dr Peter Trier of Philips, may well have been apprehensive when taking office last year. He could have presided during a year of disaster. In the event 1980 was a success and if we take into account world trading conditions it was something of a triumph.

Output was up by 15 per cent to £1,650 million of which £522 million was in direct exports. Imports barely advanced from the 1979 level so with increased exports the favourable balance of trade rose by £36 million. The major contributors to the favourable trade balance were land-based radio communications, avionic instruments, security systems and, surprisingly in view of the state of world shipping, marine radar. Even public broadcasting equipment, a notoriously difficult market, showed gains at home and abroad.

Employment, too, was up but only by a marginal three per cent over 1979 with a 1980 average of 99,200. This highlights the excellent productivity record of the capital goods sector but further improvements are anticipated through increased applications of computer-aided design, manufacture and testing (CADMAT) in which the EEA and the Department of Industry are co-operating in the establishment of standards and development.

The shortage of skilled people has eased somewhat because of lower demand from other sectors of industry but a general recovery could reverse the trend.

On the negative side profit margins have been squeezed with the high value of the pound resulting in some export orders being taken at a loss in order to preserve the market.

Overall, however, the capital goods sector remains buoyant and order intake suggests that the incoming 1981–82 president, Mr D. S. Barnes, will have an even more heartening story to relate during the coming year.

Mr Barnes is managing director of Sperry Gyroscope at Bracknell. He started in electronics as an apprentice with Philips and then joined R.E.M.E. spending some time as an instructor. He joined Sperry in 1954 after graduating in electrical engineering at London University. Since then he hasn't looked back. Yet another example of a keen apprentice making good. He was awarded the CBE in 1977.

Whither Technology

In conversation with an ex-bomber pilot, then a captain of a Viscount airliner in the BEA fleet some 20 years ago, he told me he always insisted on his junior co-pilot navigating by dead-reckoning instead of relying entirely on radio and instrument flying. This won him no popularity. What he was frightened of was loss of basic skill. Could someone completely out of practice in fundamentals be able to react successfully in an emergency?

I was reminded of that conversation when reading an account of Squadron Leader D. Cyster's commemorative flight from Dunsfold to Sydney by Tiger Moth in 1978, fifty years after the Australian Bert Hinkler became the first man to fly solo from England to Australia.

Hinkler had a brand new aircraft, an Avro Avian which was new and designed specially for the trip. He had no radio and only an atlas as a navigational chart. Cyster had radio and modern navigational charts but his Tiger Moth was four years older than he was!

In the age of Jumbos flying at 30,000ft Cyster found it difficult to obtain low-level wind speeds and directions. He was also obliged to fly to mandatory reporting points and keep to airways which made him fly a number of 'dog-legs' rather than direct. In the end he arrived at Sydney after 32 days against Hinkler's time of only 15 days.

Of course modern electronic air navigation is entirely appropriate to high speed, high altitude, organised commercial aviation and also to the Hunters and Lightnings of Cyster's professional life in the RAF. But he, too, sums up his experiences in the Tiger Moth (maximum cruise speed 70 knots) as 'becoming conscious that we are in danger of breeding a pilot/navigator who, because he has been brought up on a diet of radio beacons and radar systems, is losing the art of basic navigation'.

At another level we may ask ourselves if, with the universal use of pocket calculators, we are breeding a race of people losing the art of basic calculation? If the batteries run down can the practitioner revert to pencil and paper or even a slide rule? Or the machine operator manually turn his metal to drawing if his control tape fails?

My whole working life to date has been in technology-based industry but I still believe in the safety net of back-up systems. I keep oil lamps against power failure in the home and candles against the further possibility of the oil running out. My friends chuckle at my supposed lack of confidence. I call it good thinking, not so much against technical failure as against industrial anarchy.

Middle East

The Middle East and the Gulf, despite recent political upheavals, is still one of the fastest expanding markets in the world. Arms sales grab the headlines but this is only one aspect of total business. Take Qatar as an example. A few years ago few people knew of its existence with its tiny population of 201,000 people.

Today Cable & Wireless is installing a new switching centre for international telephone calls at a cost of £4 million. The number and duration of international calls is one of the finest measures of business activity. In 1975/76 Qatar handled under four million minutes. They have now increased to 23·5 million minutes and by mid-decade the projected figure is over 40 million minutes, a ten-fold increase in 10 years.

The telephone exchange hardware was put out to international tender. No European manufacturer had a suitable digital exchange available so the contract went to NEC of Japan on the basis of proven technology, best cost terms and delivery dates.

Marconi, however, has scored again in Egypt with a half million pound plus contract for updating an O.B. van from mono to full colour. Marconi played a large part in Egypt's switchover to colour TV in the mid-70s and the close relationship continues both in the supply of equipment and in training.

Sign Here

Security is big business and with so many crooks around it is getting bigger. Latest device on the market is Q-Sign, a signature verification system which compares a written signature with reference data either stored in a computer or encoded within a credit card. Comparison is not only in the written form of the signature but also in the 'rhythm' with which it is written. The manufacturers, Quest Automation, have developed the system from original work undertaken by the National Physical Laboratory.

Medal

The 1981 Martlesham Medal, reserved for British Telecom workers, was awarded to Mr Dennis Baker for his pioneer work on transistors for submarine repeaters. He now leads the team which coined the word microprocessor back in 1969 and is now involved in CAD of VLSI. Baker started in the Post Office as a repair and installation man. He studied at night school, earned himself a studentship at the Royal Military College of Science and gained an external BSc degree. He is now head of Telecom's microelectronics division. An example to us all.

AUDIO ANALYSER

Michael Tooley B.A. David Whitfield B.A. M.Sc.

PART 1

Analyses signals in eight octave bands over a dynamic range of 30dB

THE audio equaliser has become established with hi-fi enthusiasts as a means of tailoring the characteristics of the total audio chain to produce an optimally flat overall response. The technique allows the sound "colouration" introduced by unwanted room and loudspeaker resonances to be substantially eliminated, producing a subjectively cleaner sound on even the very best systems.

The Audio Analyser to be described is one way of providing the "missing link" in the process described above. It allows the frequency response characteristics of the audio signal to be simply and quickly measured and displayed. The basic unit described is capable of analysing signals in eight octave bands, over a dynamic range of 30dB. Expansion to eleven octave bands is simple, and the companion microphone preamplifier and noise source combine with the analyser to provide a total measurement facility.

GENERAL DESCRIPTION

A functional block diagram for the Audio Analyser is shown in Fig. 1. The analyser may be considered as being divided into three major sections; the audio processor section, the filter and display section, and the mains power supply.

The audio processor section handles stereo input signals from one of two sources; amplifier loudspeaker outputs may be routed via the analyser, or a tape monitor type of signal may be used for frequency analysis. Both inputs for each channel are buffered, and then a mono signal is derived by adding the left and right channel signals and halving the sum. A switch then allows selection of left, right or mono

signals for analysis. The selected signal then passes to a variable gain voltage amplifier where the amplitude is adjusted prior to analysis and display.

The filter and display section forms the heart of the analyser. It consists of eight octave filters and associated displays, together with an overall mean peak level monitor channel amplifier and display. All nine channels are driven by the output from the audio processor.

Each octave filter channel is essentially an active bandpass filter of fixed common Q. The lowest filter centre frequency is 64Hz, and the frequencies increase in octaves up to a centre frequency of 8192Hz. The filters are all of identical design, with only four components (two each of two types) different between channels. The filters are designed to produce an optimally flat response over the analyser's frequency range by arranging adjacent filters to overlap at their −3dB power points. This is done by selection of the appropriate filter Q value. After processing, the output from each filter is passed to its associated l.e.d. display. The display for each channel provides a resolution of 3dB per l.e.d. and a dynamic range of 30dB. Each display may operate in either bar graph or dot mode, and the physical arrangement of the analyser is such that it provides a display of amplitude against frequency.

The monitor channel retains the same format as the filter channels, with the exception that the active bandpass filter stage is replaced by a passive filter and an amplifier. The filter is a high pass type which removes low frequency signal components (rumble) and provides a mean peak level display over a 30dB range.

AUDIO PROCESSOR SECTION

The audio processor to be described is a basic design
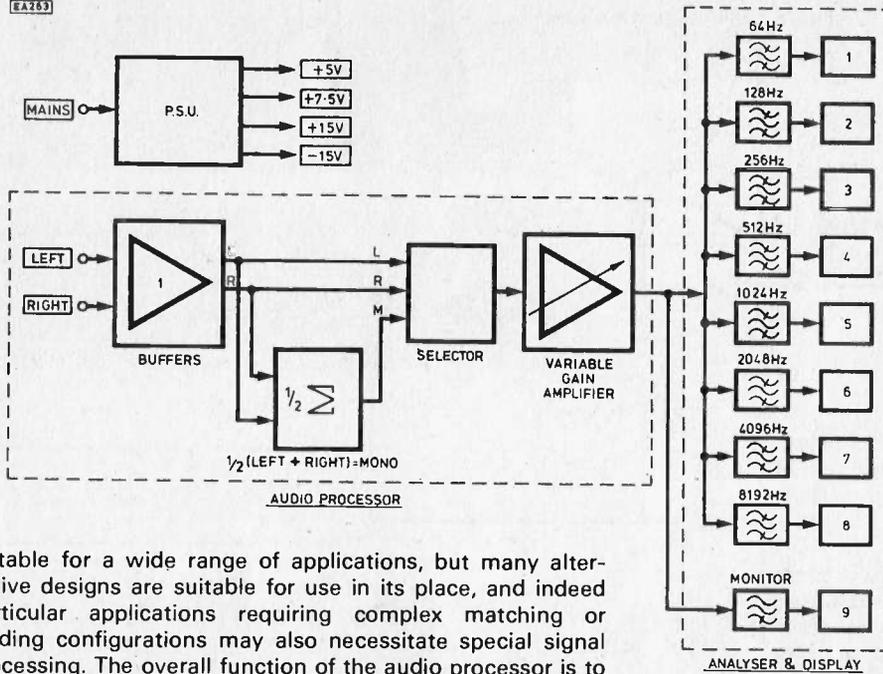
Fig. 1. Block diagram for the complete Audio Analyser

suitable for a wide range of applications, but many alternative designs are suitable for use in its place, and indeed particular applications requiring complex matching or loading configurations may also necessitate special signal processing. The overall function of the audio processor is to convert the required input signal into the form required by the filter and display section.

The basic audio processor is shown in block format in Fig. 2, with a detailed circuit diagram given in Fig. 3. The processor buffers the stereo input signals, derives a mono signal, allows selection of the signal for analysis, and adjusts the level to match the sensitivity of the filter and display section.

The analyser may take a stereo input from either an amplifier loudspeaker output or from a tape monitor type of signal source. The loudspeaker outputs are connected to SK50/SK53, and the loudspeaker system is connected to SK51/SK54. The attenuator networks R50/R51/R52 and R59/R60/R61 sample the loudspeaker signals, and the voltage followers IC50a and IC51a act to buffer the sampled signals. The tape monitor signal is applied to SK52, terminated by R57 and R66, and then buffered by IC50b and IC51b.

The outputs from the two buffer amplifiers in each channel are summed in two adders, IC50c and IC51c. This feature avoids the need for complex multi-wafer function switching and allows the addition of signals from two different sources. It does, however, mean that it is possible to

perform this addition unintentionally should unwanted sources remain connected and active.

The mono signal is generated by adding the left and right channel signals in IC50d, and attenuating the sum by 2. S50 allows selection of left, right or mono signals for analysis. The final stage is a variable gain voltage amplifier, IC51d, which allows matching of the input signal level to the sensitivity of the filter and display section.

FILTER AND DISPLAY

The filter and display section comprises of eight octave filter channels and a monitor channel. The monitor channel circuit is a modification of the basic filter channel and the differences will be detailed after the basic module has been described.

A block diagram for the basic filter and display module is shown in Fig. 4, together with a full circuit diagram in Fig. 5.

The input signal to each channel is buffered by IC1a which operates as a voltage follower. This stage presents a high input impedance and has a low output impedance: characteristics required to prevent loading of the audio processor output stage or affecting the performance of the active filter

Fig. 2. Block diagram for the audio processor section

Fig. 3. Audio processor circuit
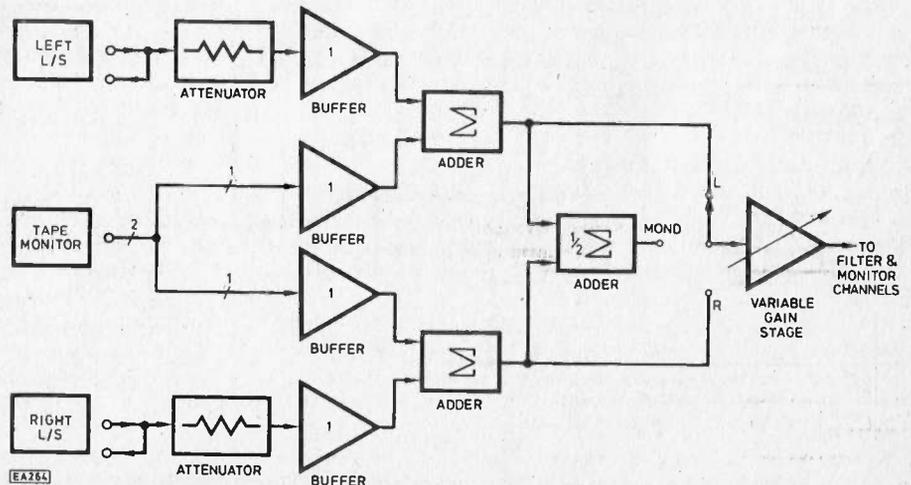
Fig. 3. Audio processor circuit
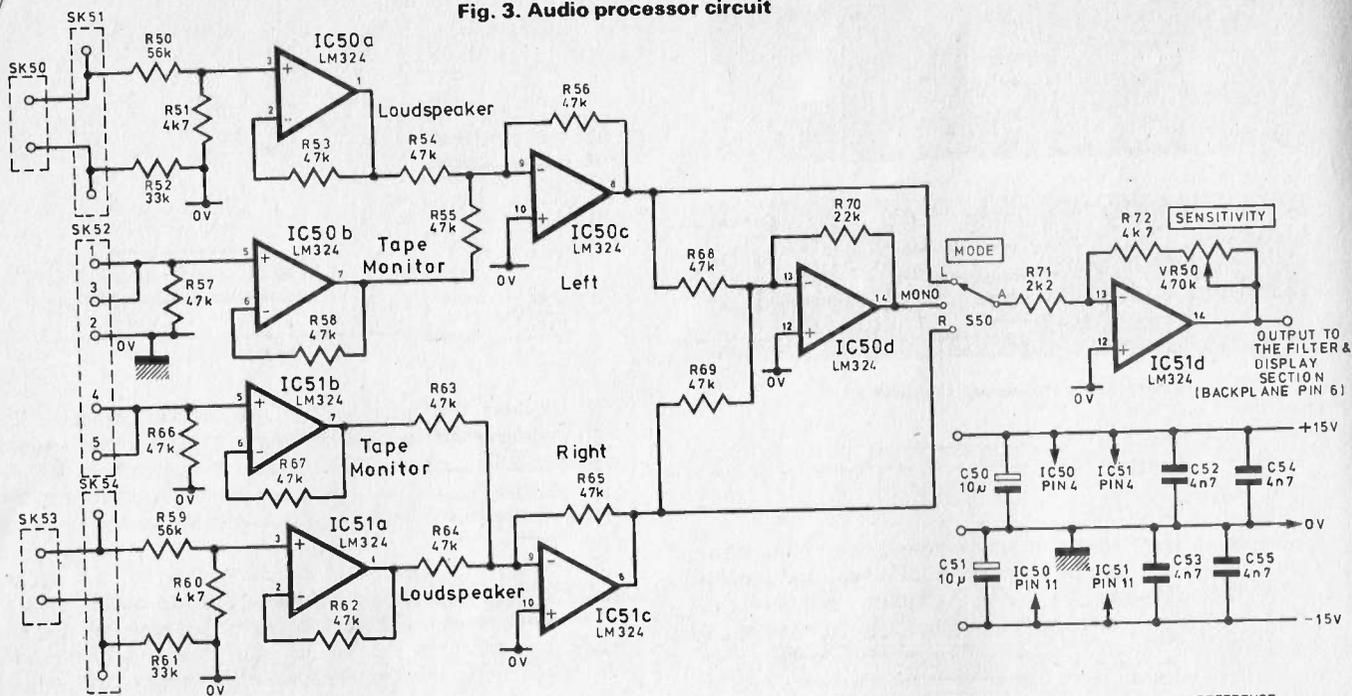
which follows.

Following the buffer, IC1b is configured as a Wien-bridge bandpass active filter. The Wien network, which is illustrated in its basic form in Fig. 6, gives a maximum response at a frequency of $f_o = (1/2\pi RC)$ Hz; f_o is known as the filter centre frequency. Positive feedback through R_A, R_B sharpens the response (increases the Q) without any change in the centre frequency. Thus, variation of the filter's Q may be achieved independently from changes in f_o. The sensitivity of f_o to changes in R and C is proportional to Q, but typically, using 1% resistors and 5% capacitors, f_o will be within $\pm 5\%$ of the theoretical value up to approximately 15 kHz. At high frequencies amplifier phase shift causes Q and f_o to depart from their nominal values. It is essential that the source resistance of the signal driving the filter should be $\ll R$ for predictable f_o, hence the reason for the inclusion of the buffer stage, IC1a.

Using the formulae given in Fig. 6, suitable values of R and C may be calculated for any given centre frequency. Table 1 shows suitable values, taken from the readily available ranges of capacitors and resistors, for the filters
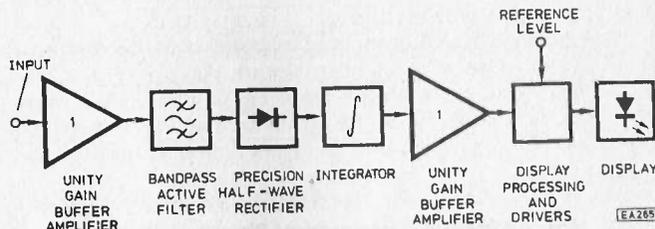
Fig. 4. Filter and display block diagram

used in the basic eight-octave analyser. Also included are suitable component values for three additional filters which may be added within the audio range. In general, these component values give nominal centre frequencies in close agreement with those required, but many alternative combinations of values may be used to give similar results. Large values of resistance, however, should be avoided as these may produce an output d.c. level of up to about 1V.

The values of the Q-determining resistors, R2 and R3, have been chosen to produce a filter overlap between adjacent channels at their −3 dB power points. A constant Q is maintained for all eight filters. Using the fact that the filters
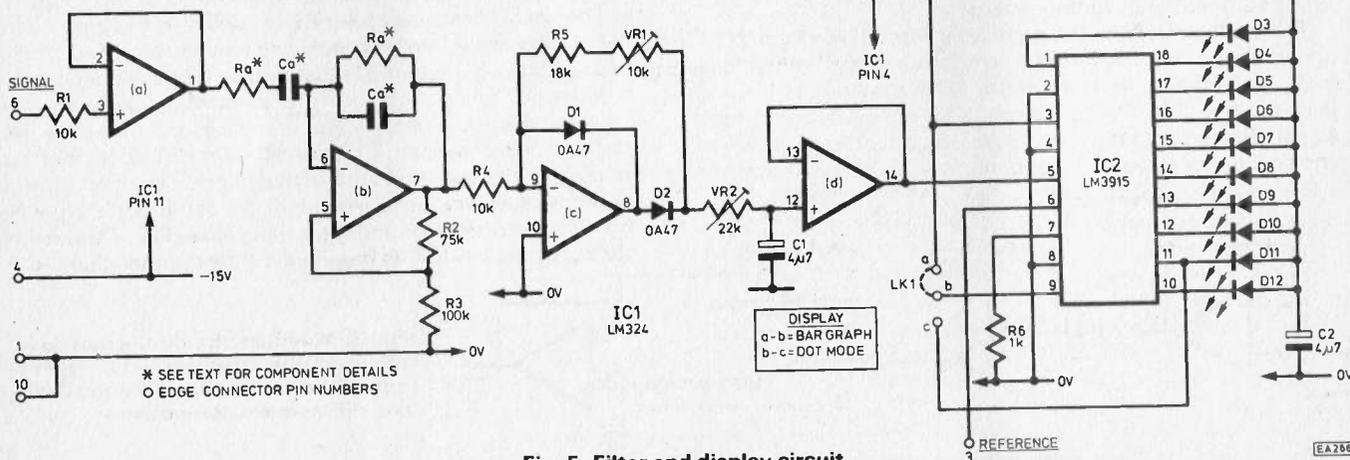
Fig. 5. Filter and display circuit

Front and rear view of Analyser
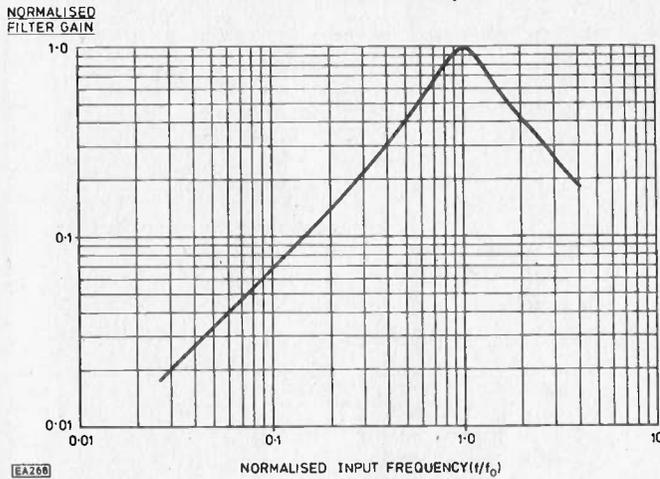
Fig. 7. Response for a typical filter ($f_o = 8192$Hz)

Fig. 6. Wien bandpass active filter

$$f_o = \frac{1}{2\pi CR} \text{ Hz}$$

$$Q = \frac{1}{2 - (R_B/R_A)}$$

$$A_v = \frac{3}{(R_B/R_A) - 2}$$

are spaced at octave intervals (i.e. each f_o is twice that of the adjacent lower channel), and the equations given in Fig. 6, the Q required comes out as 3/2, with $R_B/R_A = 4/3$. By comparison, to cover the same frequency range with 16 filters spaced at half-octave intervals would require a Q of 2·915 and R_B/R_A of 1·657; the filters would also have a higher voltage gain.

The output from the active filter is applied to the precision rectifier circuit formed by IC1c, D1 and D2. The gain of this stage has been made variable (via VR1) to allow compensation for the cumulative component tolerances for precise measurements. In most situations this is not really necessary, and provision is made on the p.c.b. to replace VR1 by a fixed value component.

The d.c. output from the rectifier is filtered by VR2 and C1 acting as a passive low pass filter (integrator). The value of VR2, for fixed C1, determines the time constant of the display, i.e. how fast the l.e.d.s go on/off for a changing input signal. The actual setting is very much a matter of personal choice, but the authors have found that a mid-way setting of

VR2 provides the most widely acceptable response. The p.c.b. is designed to accommodate a fixed value resistor (typically 10k) in place of VR2 should this be preferred.

IC1d is configured as a voltage follower to present a high impedance to the integrator, preventing errors due to circuit loading effects.

The frequency response characteristics for the buffer-filter-rectifier-integrator-buffer chain was measured in detail for a sample channel from the prototype analyser and the results are shown in Fig. 7. The graph shows how the filter roll-off characteristic closely follows the theoretical rate of 20 dB/decade, and the Q is very close to 3/2. The asymmetry of shape of the characteristic which appears at around 16kHz (i.e. $f/f_o = 2$) is that expected due to amplifier phase shift effects; this does not occur on the lower frequency filters.

The output from IC1d drives the display circuitry which converts a d.c. voltage in the range 0 to +7·5 volts to a 10-l.e.d. display operating in steps of 3 dB. The display circuit is built around the National Semiconductor LM3915, part of the family derived from the well known LM3914 dot/bar display driver i.c. The LM3915 is a monolithic integrated circuit that senses the analogue levels and drives 10 l.e.d.s, providing a logarithmic 3 dB/step analogue display.

Pin 9 provides the means to change the display from bar graph to moving dot, and the l.e.d. current drive is regulated and programmable by means of a single resistor. R6 sets the l.e.d. current at $I = 12·5/R$, where the current may be programmed to any value in the range 1 mA to 30 mA, taking care not to over-dissipate when operating in bar graph mode. An input buffer drives 10 individual comparators referenced to a precision internal resistor divider chain, which has an accuracy of typically better than 1 dB. The full-scale reference is the value applied to pin 6, and the display may be expanded to cover a 60 dB or even a 90 dB range.

The circuit described above is modified in the area round IC1b to provide the monitor channel facility. The active bandpass filter is replaced by a passive highpass filter and a fixed gain amplifier. This has the effect of removing the low frequency signal components (rumble) and boosting the signal level to provide a comparable amplitude to that appearing at the output of the active filters. No other component changes are necessary and the same p.c.b. may be used for both monitor and filter units alike. Fig. 8 shows the full circuit around IC1 as modified for the monitor channel.

Fig. 8. Modified circuit diagram for the monitor channel—this part replaces all of the circuit around IC1 in the filter and display modes

COMPONENTS

Resistors

R50	56k
R51	4·7k
R52	33k
R53	47k
R54	47k
R55	47k
R56	47k
R57	47k
R58	47k
R59	56k
R60	4·7k
R61	33k
R62	47k
R63	47k
R64	47k
R65	47k
R66	47k
R67	47k
R68	47k
R69	47k
R70	22k
R71	2·2k
R72	4·7k

All resistors are $\frac{1}{4}$W 5% carbon types

Potentiometer

VR50	470k log with DPST mains switch (S100)

Capacitors

C50	10µ 16V p.c.b. electrolytic
C51	10µ 16V p.c.b. electrolytic
C52	4·7n ceramic
C53	4·7n ceramic
C54	4·7n ceramic
C55	4·7n ceramic

Semiconductors

IC50	LM324
IC51	LM324

Miscellaneous

SK50	2-pin DIN chassis loudspeaker socket
SK51	2-pin DIN chassis loudspeaker socket
SK52	2-pin DIN chassis loudspeaker socket
SK53	2-pin DIN chassis loudspeaker socket
SK54	5-pin DIN chassis socket (180° type)

Printed circuit board and mounting hardware
Terminal pins

S50	4P3W rotary switch

FILTER AND DISPLAY BOARDS One set of components for each board

Resistors

R1	10k 5%
*R2	75k 2%
*R3	100k 2%
R4	10k 5%
R5	18k 5%
R6	1k 5%
**R7	33k 5%
**R8	100k 5%
Ra	See text 2%

All resistors $\frac{1}{4}$W carbon types

Potentiometers

VR1	10k ⎱ Miniature horizontal skeleton presets
VR2	22k ⎰

*Filter channel only
**Monitor channel only

Capacitors

C1	4·7 µF 16V electrolytic
C2	4·7 µF 10V electrolytic
C3	470 nF polyester film
*Ca	See text

Semiconductors

IC1	LM324
IC2	LM3915
D1	OA47
D2	OA47
D3–12	10 off 0·2in (5mm) wire-ended l.e.d.s, colour(s) to suit preference/application

Miscellaneous

Printed circuit board
10-way inter-p.c.b. connector (RS type: 467-582/
467-677 and pins)

POWER SUPPLY

Resistors

R100	4·7k
R101	4·7k
R102	4·7k
R103	100

$\frac{1}{4}$W 5% carbon types

Capacitors

C100	1000µ 16V p.c.b. elect
C101	470µ 25V p.c.b. elect
C102	470µ 25V p.c.b. elect
C103	220n polyester film
C104	220n polyester film
C105	220n polyester film
C106	470n polyester film
C107	470n polyester film
C108	470n polyester film
C109	220µ 10V p.c.b. elect
C110	220µ 16V p.c.b. elect
C111	220µ 16V p.c.b. elect
C112	470µ 16V p.c.b. elect
C113	4·7n ceramic
C114	220µ 10V p.c.b. elect
C115	10µ 16V p.c.b. elect
C116	10µ 16V p.c.b. elect

Semiconductors

IC100	7805 +5V regulator
IC101	7815 +15V regulator
IC102	7915 −15V regulator
BR100	BY164
BR101	BY164
D100	BZY88C7V5

Miscellaneous

Printed circuit board and mounting hardware
3 off plastic package PCB heatsinks (e.g. RS type;
401-863)
Terminal pins

|	
TR100	6V, 0·5A. 6V, 0·5A. Miniature 6VA mains transformer (e.g. RS: 196–296)
TR101	15V, 0·2A. 15V, 0·2A. Miniature 6VA mains transformer (e.g. RS: 196–397)
SK100	3-pin mains connector (optional) and mains lead
SK101	4-pin chassis DIN socket (optional auxiliary power outlet)
SK102	4-pin chassis DIN socket (optional auxiliary power outlet)
S100	DPST mains switch, included with VR50

Table 1. Frequency determining component values

Nominal Centre Frequency (Hz)	Resistance (Ra) (E24 series)	Capacitance (Ca) (E12 series)	Theoretical Centre Frequency (Hz)	Filter Board Coding (* indicates plug fitted in pin position)		
				8	7	5
16	100k	100n	16		N/A	
32	150k	33n	32		N/A	
64	110k	22n	66			
128	56k	22n	129			*
256	62k	10n	257		*	
512	68k	4·7n	498		*	*
1024	33k	4·7n	1026	*		
2048	3·6k	22n	2010	*		*
4096	39k	1n	4081	*	*	
8192	20k	1n	7958	*	*	*
16384	10k	1n	15916		N/A	

A filter and display board

MAINS POWER SUPPLY

The circuit diagram for the mains power supply is shown in Fig. 9. A ±15V regulated supply is provided by TR101, BR101, IC101, and IC102. This provides the supply for the operational amplifiers in all sections, and the +15V rail also powers the internal circuitry of the LM3915 display driver i.c.s. The ±15V supply is brought out to two optional rear panel sockets, SK101 and SK102, to provide power for the microphone preamplifier and noise source (see next month). A 4-pin DIN connector has been chosen to provide a non-reversible connector which does not occur elsewhere in audio systems.

The display full scale reference, +7·5V, is derived from the +15V rail by the regulator formed by R103 and D100.

The l.e.d. supply is provided by TR100, BR100 and IC100. The value of +5V for this supply has been chosen for simplicity and convenience, and allows the use of readily available components. With one l.e.d. per display segment, however, a supply as low as +3V or as high as +15V could have been used. In the circuits described for the analyser, the l.e.d. current has been set to approximately 12½mA. The power supply shown will provide adequate current to drive the nine channels in bar graph mode without causing over-dissipation in the display drivers. For higher display brightness, the value of R6 should be reduced. Care should be taken in bar graph mode, however, to avoid exceeding the maximum power dissipation of the LM3915, i.e. 600mW, or saturating the power supply. The maximum l.e.d. current which may be programmed is 30 mA, using R6 = 390.

Next Month: Constructional details. A special offer on a graphic equaliser will also be included.

Fig. 9. Power supply

UK 101 COLOUR BOARD REVIEW

MIKE ABBOTT

THE COLOUR BOARD by *Chromosonic Electronics* of North London is designed to allow a standard colour television, if you have one, to be linked either to a PET, or a UK 101/Superboard microcomputer system, hence allowing you to view colour graphics instead of those old black-and-white movies. Here, we look at the system in use with a UK 101; but before that, the all-important matter of how easily the kit slots together is reviewed. The Colour Board is only available in kit form, and costs about £85 for the UK 101 version. Either version is capable of generating eight colours.

The hardware you have to build is shown in the photographs, and is a two-tier uncased p.c.b. arrangement. The lower p.c.b. is the Video Board whose purpose is to pump out standard PAL encoded colour TV signals through a UHF modulator (the same type as that already fitted in the UK 101). This, of course, is designed to drive your television via the aerial socket (so that your TV need not be tampered with). The lower board is called the Colour RAM Board, or C-RAM board. Its job is to remember which background colours and character colours you require around the screen. This works on the standard *memory mapped video* character-slot resolution principle. See Fig. 1 for an example.
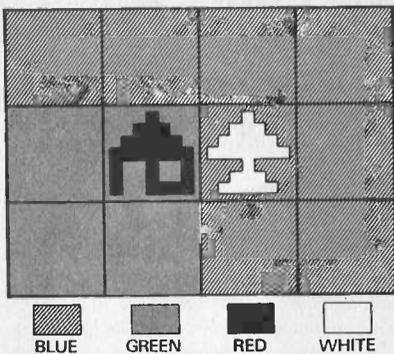
Fig. 1. Any character colour and any background colour may be selected using POKE

BLUE GREEN RED WHITE

The module runs entirely on +5 volts, which the supplier claims may be drawn from the computer's own PSU, although most Compukits in use are already mopping up almost every last milliamp the PSU has to offer. The system comes complete with flying ribbon cables and the necessary d.i.l. headers to plug straight into Compukits' video RAM sockets. You find yourself with two spare RAMs and a 7403 (IC70) after installation. All inputs are TTL compatible, and on the upper board is mounted a "Colour Screen Clear" switch which you might eventually prefer to be mounted remotely on the computer's front panel; or come to that, be driven from software, via the PSG's spare I/O port for example.

VIDEO BOARD

Construction commences with the Video Board. This, and the accompanying p.c.b., are both of excellent quality glass-fibre preparations with solder resist coating and all component positions clearly printed on them. Assembly was as easy as laughing. The accompanying fifteen page booklet (of the bound photostat variety) includes a section giving constructional advice to the neophyte. This explains colour coding of components and physical descriptions, along with basic fitting procedures. All the instructions are formatted as a check-off list, and ideal in their

simplicity, clarity and consideration for the constructor. There were some doubts about the two nondescript metal cans at first; one being the Data Decoder and the other being the PAL Encoder but since each module has different pin-outs there was ultimately no cause for alarm—each would not fit in the other's location!

C-RAM BOARD

The Colour RAM Board is a double-sided plated-through p.c.b., and again, thanks to the instructions being straightforward and thoughtful, this board allowed itself to be assembled like clockwork. The two boards screwed together sandwich fashion and all ribbon cables soldered in position, all that remained to be done was the removal of three i.c.s from the UK 101 (2 × video RAMS and IC70), plugging in the Colour Unit's flying leads and setting up for correct colour hues. What could I look forward to?

HOW IT WORKS

The objective in the design is to allow each character location across the screen an individual choice of background colour and foreground, or more accurately, character colour.

Two extra 1K × 4 bit RAMs (2114) are used in the C-RAM board, one of which stores the *background* colour for each screen cell, and the other remembers the *character* colour for each screen cell. Since the range of colours in each case is merely as follows, 4-bit RAMs are sufficient:

COLOUR	BACKGROUND		CHARACTER
BLACK	240		248
BLUE	241		249
RED	242		250
MAGENTA	243	POKE	251
GREEN	244	VALUES	252
CYAN	245		253
YELLOW	246		254
WHITE	247		255
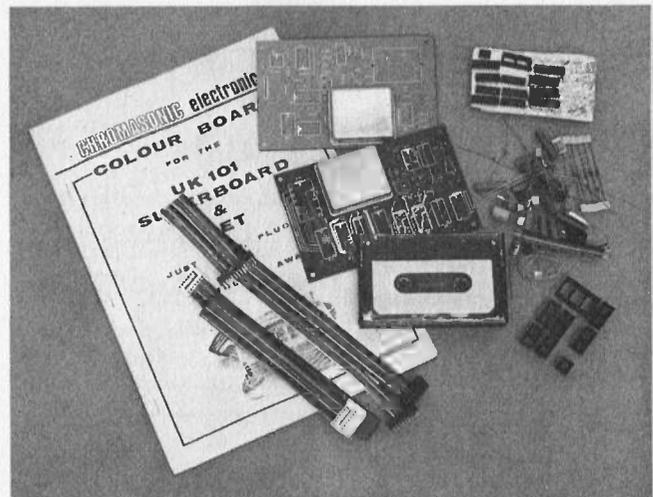
The UHF Modulator is absent from this photograph of the Colour Board, but this component, and *all* others, are supplied in the standard kit of parts.
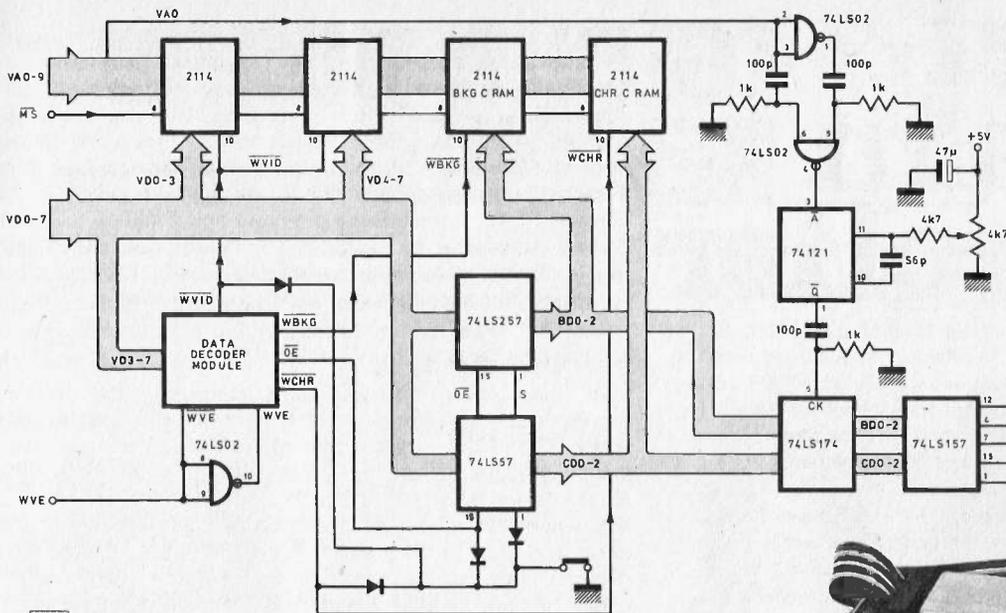
Since the UK 101 screen operating firmware runs independently of the C-RAM, the colour instructions may not be *scrolled* away and need be removed by reinstructing the C-RAM via software, or pressing the Colour Clear switch. Colour instructions may be directed to the screen using PRINT instructions, however.
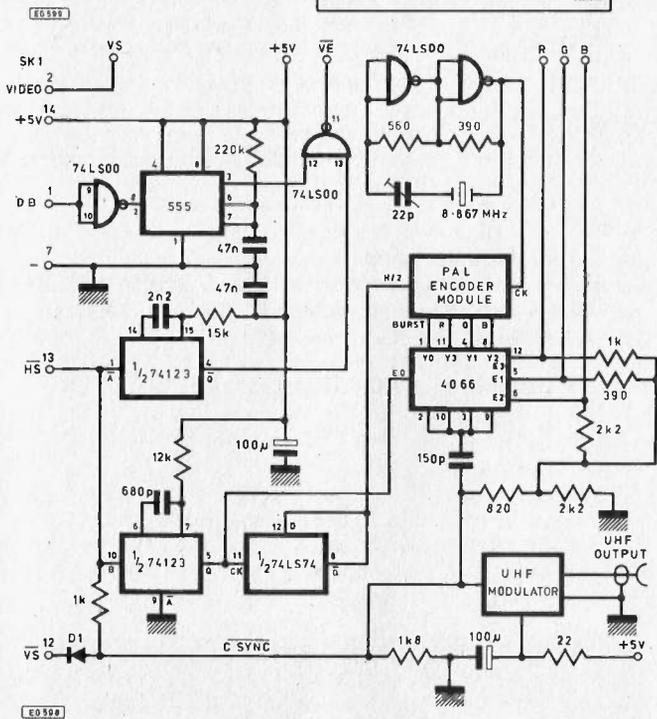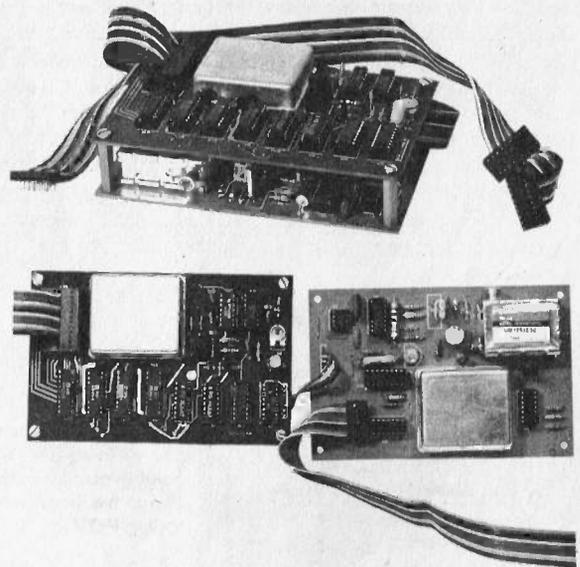
Fig. 3. Video board

To drive the system one simply POKEs the screen location with the necessary numbers taken from the table shown opposite. The system is entirely memory mapped, although you will notice that the latter ASCII codes 240–255 are singled-out by the colour unit's Data Decoder module, for colour instructions, and hence their original graphics symbols are lost. For example POKE S, 248 will no longer print the Greek letter π at screen location S, but will instead ensure that any character which *is* at location S will be coloured black. Similarly POKE S, 241 will not give you α, but instead produce a blue background square.

ADJUSTING THE COLOURS

For setting up, a cassette is supplied with two simple colour tests (the tape also includes a card game) and a trimming tool, and it is simply a question of adjusting one preset potentiometer and one trimmer capacitor. No special equipment is required,

nor any specialised knowledge, since the process is entirely based on subjective judgement using the test pictures available from the cassette. This process takes only minutes.

IN OPERATION

Anyone utilising the Cegmon monitor in their Compukit would find the definable window feature most handy when manipulating colours with this system. There is little one can say about using the Colour Board because it is a simple extension of the video techniques a Compukit owner will already be familiar with, but I feel bound to say that its application, whilst obvious in video games, is less apparent in more serious situations. Multiplot graphs, histograms and high yield data formatting are businesslike areas of programming which nevertheless obviously would benefit from the Chromosonics Colour Board.

In conclusion, I would say that there is nothing at all in the construction and setting up which would frighten off the reasonably competent constructor, and the end result is a highly rewarding feature which makes programming and programs still more exciting.

Finally, it should be pointed out that colour clarity is heavily dependent on the UHF modulator, one of which is supplied new with the kit so there should normally be no problem. Should you for one reason or another transfer the modulator from your Compukit, and like ours, it is a heat casualty, the localised colour definition will be impaired. ★

Model Train Controller

ANDY FLIND

LIKE thousands of other fathers, the author was persuaded last Christmas to buy a model railway set for his son. The one finally purchased was of a well-known British make, and the track and actual models were superb; the detail the manufacturers put in these days is truly faultless. The control unit supplied was a trifle crude however, having just three switched forward speeds and three again in reverse. The slowest of the three speeds provided being still quite fast, it proved impossible, for example, to bring the train realistically into a station, and using the ingenious gadget on the track for uncoupling carriages was tricky, to put it mildly.

DEFINING THE SPEC

In the general idleness that surrounds the holiday therefore, the concept of a better control unit began to take shape. The idea seemed simple at first, but as with so many small projects, surprising problems appeared when the actual design was attempted. The specification called for a single control knob with forward on one side, reverse on the other and stop in the centre. A variable track voltage was decided upon as the means of control as variable pulse-width systems tend to cause noise and overheating in the motors, but an 'unsticker' was incorporated into the design, superimposing very short pulses on the d.c. output to ensure smooth starting at low speed settings. Some inertia was built in, so that the train would accelerate and brake gently like a real one, and finally the unit was required to be short-circuit proof in case something metallic was dropped across the track.

CIRCUIT OPERATION

The full circuit appears in Fig.1. A control voltage is produced by VR1 and buffered by IC1a. the inertia is provided by C1 and C2, two capacitors, one to each rail, being used here to prevent the train from tearing off at full speed when the unit is first switched on.

If a single capacitor to the negative rail were to be used it would pull the input down whilst it initially charged and thus apply full throttle.

The output from IC1a goes to IC1b, which with transistors TR2 and TR3 forms a bidirectional current generator. The operation of this is as follows; R5 and R6 apply half the supply potential to the non-inverting input, and the op-amp will try to maintain this potential at its inverting input. Any voltage applied to R7 will cause current to flow through it, the direction depending upon whether the applied voltage is above or below half supply potential, and this current will appear from the collector of TR2 or TR3 depending upon its direction.

If the input voltage is greater than half supply the current will come from TR3 and flow to the negative rail through R11, setting up a positive voltage across this resistor. If it is less than half supply the current will come from TR2 and flow to the positive rail through the 'current mirror' TR1 and TR4. The 'reflected' current from TR4 again produces a positive voltage across R11. Thus when VR1 is central there is no voltage across R11, but moving it to either side results in a rising positive control voltage with a maximum value, when the unit is loaded by a train motor, of around six volts. This control voltage is translated into approximately 0-12 volts on the track by IC3a, which compares it against feedback from divider R16 and R17 and adjusts the drive to TR6 and TR7 accordingly.

Reverse is simple, IC2a compares the original control voltage after IC1b with the half supply reference and operates the reversing relay accordingly. The signal for this is taken after the inertia so that if the train is travelling in one
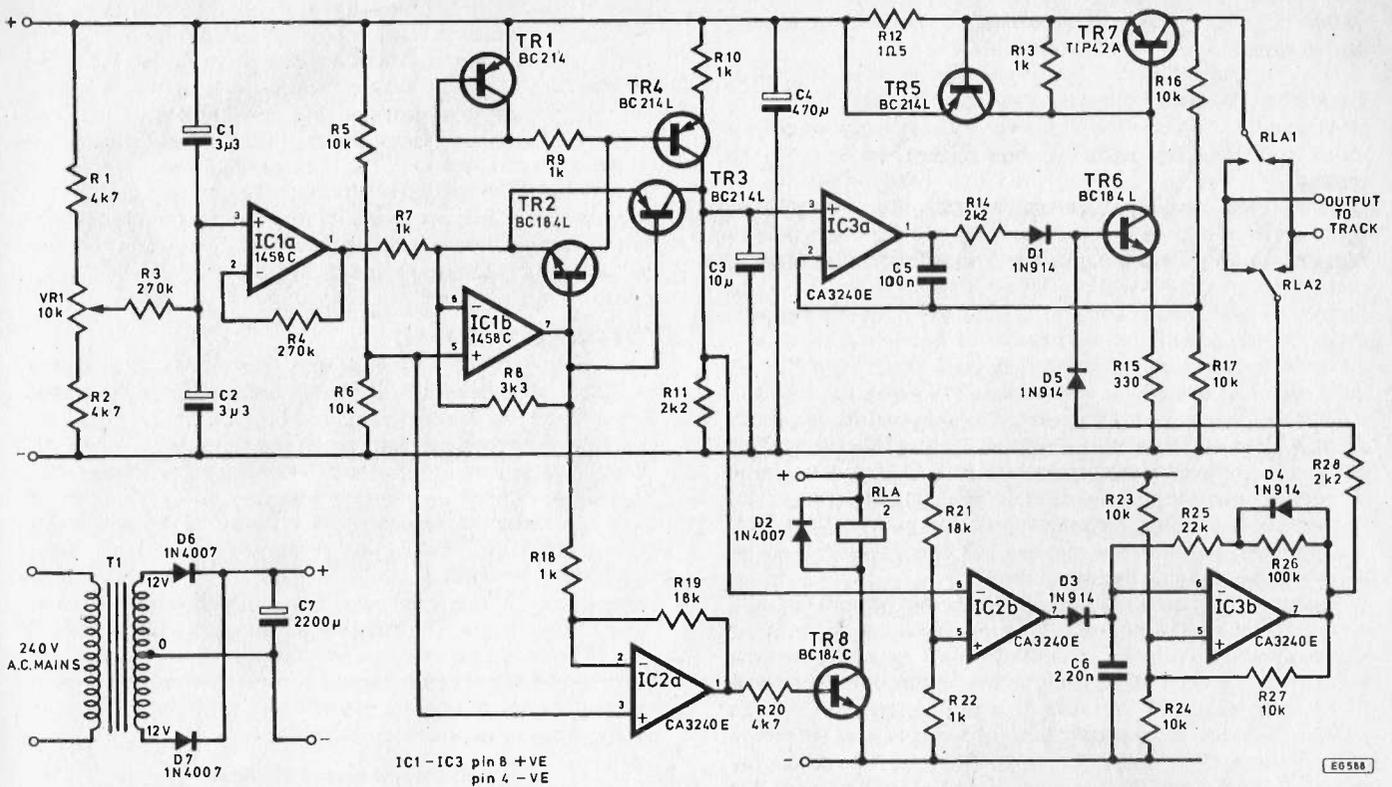
Fig. 1.   Circuit of Train Controller

COMPONENTS

Resistors

R1, 2, 20	4k7
R3, 4	470k
R5, 6, 16, 17, 23, 24, 27	10k
R7, 9, 10, 13, 18, 22	1k
R8	3k3
R11, 14, 28	2k2
R12	1R5
R15	330R
R19, 21	18k
R25	22k
R26	100k

All ⅓W 5% carbon

Potentiometer

VR1	10k lin. carbon

Capacitors

C1, 2	3·3μ 35V tantalum bead
C3	10μ 35V tantalum bead
C4	470μ 25V electrolytic
C5	0·1μ polyester
C6	0·22μ polyester
C7	2200μ 25V electrolytic

Diodes

D1, 3, 4, 5	1N914
D2, 6, 7	1N4007

Transistors

TR1, 3, 4, 5	BC214L
TR2, 6, 8	BC184L
TR7	TIP42A

Integrated Circuits

IC1	1458C
IC2, 3	CA3240E

Miscellaneous

T1, 12-0-12V at 250mA. or similar RLA, 12V operated type with d.p.d.t. contacts (Maplin 'Miniature Mains') 0·1in pitch Veroboard, 24 strips of 50 holes; also piece with 13 strips of 37 holes. S1, s.p.s.t. Case, Verobox type 202-21042L, 153×84×79mm, Veropins, pointer knob, screws, wire, etc.

direction and the control is suddenly thrown over to the other direction, it will brake smoothly to a halt and then accelerate the other way, just as its real life counterpart would.

Next comes the 'unsticker'; IC3b is connected as an oscillator and supplies very short drive pulses at low frequency to the output stage to 'unstick' the motor when moving off at very low settings. IC2b senses when the voltage across R11 is so low that the train should have stopped anyway and turns off the pulsing oscillator at this point.

Finally, TR5 provides the short-circuit protection. If the voltage across R12 rises above 0·6 volts, TR5 begins to conduct and sinks any further drive current supplied by TR6, preventing TR7 from being biased on any further. With the

value of R12 shown the current is limited to around 0.5 amps.

CONSTRUCTION

Most of the components of this project are fitted onto a stock size of 0.1in pitch Veroboard. Start by cutting the mounting holes and making the forty three breaks in the copper strips. Check the breaks with a strong magnifying glass as sometimes an almost invisible strip of copper remains around the edge of a break and this can cause real consternation during testing. Fit all the wire links, there are twenty two of these, and the twelve Veropins for external connections. Then fit all the passive components—resistors, capacitors and diodes. Temporarily hook up a supply of 18 volts (you can use two 9 volt batteries in series for this) and check the current drawn which should settle to about 2.8mA after an initial surge as the capacitors charge. This obviously wont verify that everything is correct, but any large deviation from the current quoted will indicate a need for some trouble shooting before progressing further. Next TR1, 2, 3, and 4 can be fitted and a quick check made that the current drain remains around 2.8mA.

Fitting of the remaining components can now begin. IC1 should be inserted first and VR1 temporarily connected. The supply should be hooked up and IC1 pin 1 monitored with a voltmeter. It should be possible to swing this voltage from 4 to 14 volts with VR1, but note that the voltage will change slowly and take several seconds to come to rest. If this is correct check the voltage across C3. With an 18 volt supply this should be about 9 volts at each end of VR1's travel, but zero in the centre. Again it will change slowly due to the inertia circuitry.

If all seems satisfactory fit IC2. The voltage on pin 1 of IC2 should be +16V when VR1 is turned anticlockwise, and zero when it is turned clockwise. Pin 7 should normally be at zero, but go to +16V over a small band at the centre of VR1's travel. Fit TR5, temporarily connect the relay coil, and check that the relay closes when VR1 is turned anticlockwise of centre.

IC3 and TR5 and 6 should now be fitted and TR7 temporarily connected. Check that the control VR1 will vary the output voltage from TR7, from zero at mid travel up to 12V plus at either end. This completes construction and testing of the main circuit board.

ASSEMBLY

With a little care the board and all the other components can be fitted into a Verobox measuring just $15\frac{1}{2} \times 8\frac{1}{2} \times 8\frac{1}{2}$
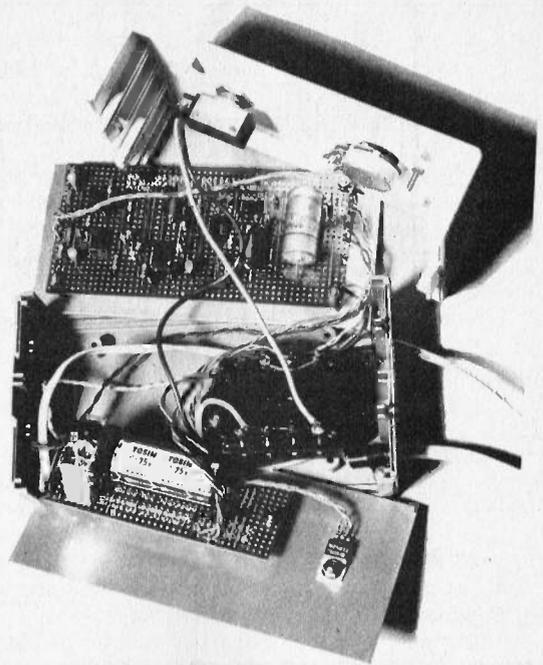
Exploded assembly detail

cm. The box specified has two aluminium side panels; the main board was fixed to one of these using 6BA screws and plastic spacers, and the transformer was bolted to the bottom of the box. The power supply components and the relay are mounted on another piece of Vero and attached to the other aluminium panel, which also conveniently doubles as a heatsink for TR7 (Fig. 2).

The wiring to the switch and the mains side of the transformer is of course live and therefore dangerous; care must be taken to ensure that none of this can ever come into contact with the low-voltage side of the circuit.

All the interconnections necessary are shown in the drawing (Fig. 3).

A final touch was the fitting of a round-headed screw to indicate the 'stop' position on the pointer knob fitted to VR1, so that this position may be found easily by touch alone— the operator may be watching the train instead of the controller.
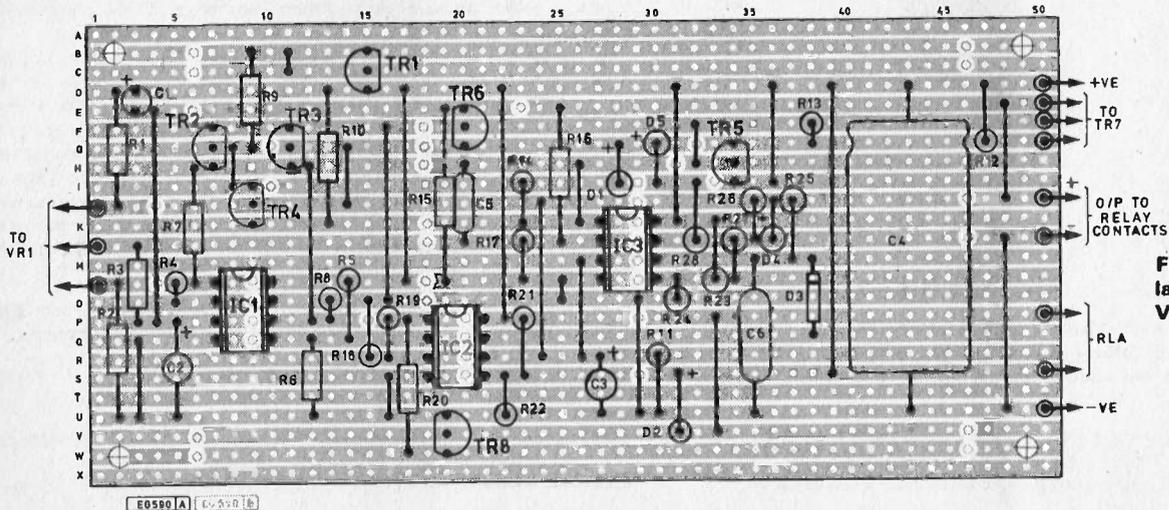
Fig. 2. Component layout for main Veroboard
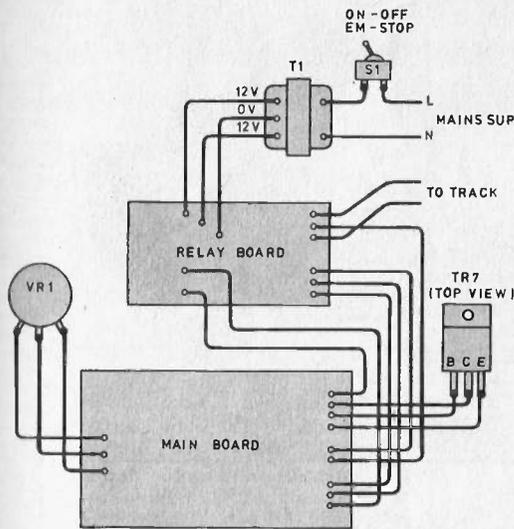
Fig. 3. Board interconnections
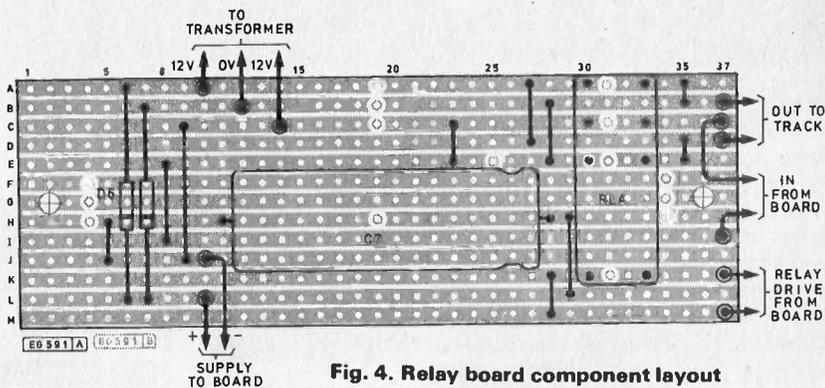
Fig. 4. Relay board component layout

Despite its complexity this unit is simple to operate and inexpensive to construct, costing no more than many commercial units with inferior performance. Many constructors may already have some of the more expensive parts such as the transformer and relay, and the cost could be reduced still further by practising a little carpentry to produce the case. Since its completion the prototype has been played with by quite a number of small boys, and has received unanimous approval from all of them. ★

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Semiconductor UPDATE...

FEATURING MM5439 ZN470 MD4101

R.W. Coles

MICRO TUNER

Microprocessors, as by now we cannot fail to be aware, are all set to rule the world. Not long ago we were assured that the living creature best suited to inherit the Earth when we humans have finally annihilated each other in a nuclear holocaust, will be that radiation resistant scavenger, the cockroach. Well, the day of the cockroach has not yet dawned (thank goodness!), but a benign takeover by those other "bugs" with even more legs is already well underway.

Microprocessors are getting into everything electrical and electronic, from washing machines to hi-fi, and before long, I am told, they will even be inside our credit cards. ("Z80? That'll do nicely, sir!" "Have a good day!")

My first offering this month is a device in the first wave of a microprocessor assault on the radio and television industry, and take it from me, before long no self respecting TV or tuner will be able to get by without a microprosessor in its entrails.

If you don't happen to be about to challenge the Japanese for supremacy in the television manufacturing field, don't skip to the next item just yet, because I think this device could be useful for lots of other applications when coupled up to your UK101 or NASCOM. The new device is the MM5439 microprocessor compatible tuning circuit from National Semiconductor, and what it does is turn a TV or radio into a mere peripheral of the omnipotent microprocessor. There are many microprocessor peripheral chips, such as UARTs and PIOs for example, but while the MM5439 falls into the same broad category as those other devices, it is unique in the bridge that it builds between microprocessor and consumer entertainment equipment.

The main feature of the new chip, although perhaps the most difficult to use in a hobby project, is a programmable phase-locked-loop (PLL) system which is intended for use as the heart of a tuning frequency synthesiser required, of course, so that the microprocessor can tune in to the radio or TV programme of its choice. More useful (for a hobby project) are the six "potentiometer" outputs which would normally be used by the micro' to adjust parameters such as volume, tone, brightness or colour, while it watches "Tomorrow's World" perhaps. Since these outputs are a simple form of digital to analogue converter, they could be used for many other applications where a microprocessor needs to produce analogue

control voltages. Each "potentiometer" output has six bit resolution and uses a pulse width modulation scheme which relies on an external integrating capacitor to build up an analogue voltage proportional to a digital word from the microprocessor. Also of interest are six latches forming a six bit parallel output port, which is always handy. A further seven package pins have a dual function as either an output or an input port, used in the tuner application to read a keypad or to control channel switching, for example. The microprocessor converses with the MM5439 via standard data and address bus lines and uses chip select and READ/WRITE strobes to convey its wishes to an array of eleven on-chip registers.

The chip arrives in a 40 pin plastic d.i.p. and utilises NMOS silicon gate logic running from a single 5 volt supply.

In a remote control TV or hi-fi system this chip will be dynamite, but I expect you will see all kinds of other ingenious uses for it!

ELECTRET CHIP

Since time immemorial, the telephone has had to depend on the archaic carbon microphone as its input transducer. The carbon mike relies on a variation in the resistance of a capsule of carbon granules caused when sound waves impinge upon a diaphragm forming one wall of the capsule. Because the capsule does not generate any voltage itself, it is necessary to provide a d.c. energising supply, the variations in resistance then modulate the current in the circuit and an a.c. speech signal can be picked off using a transformer. The principle works of course, but the carbon mike is a fairly unreliable component and has a poor frequency range responsible for much of the distortion we hear when talking to Granny on a Sunday evening. There have been a whole host of new microphone designs since the carbon granule system was first employed, but none of these has found its way into the telephone system because they could not be directly used with the existing exchange equipment due to insufficient output, electrical incompatibility, or high cost.

One of the latest developments in microphone technology is the use of an electret (the electrostatic equivalent of a permanent magnet) to produce a simple low cost device with high reliability and an excellent frequency response. Despite its many attractive features the electret mike is unfortunately still unsuitable as a direct replacement for the carbon capsules

because it needs additional amplification and matching circuitry, and that's where the Ferranti ZN470 comes in. This small chip can be installed within the telephone along with the electret microphone. It takes its supply from the energising voltage supplied by the exchange, and it has an on-chip diode bridge to cater for supplies of either polarity. Even surges resulting from a lightning strike are safely bypassed by protective circuitry within the ZN470, and standing d.c. line currents of from 1 to 100 mA are permissible. The chip has fixed, pin selectable, gain options of between 20 and 25.7 dB, and has a potential frequency response of up to 200kHz, which should be enough, even for Granny! In practical telephone circuits the frequency response will be limited by the choice of external capacitor values.

The Ferranti ZN470 is British to the core, comes in a 14 pin plastic package, and I hope British Telecom take the hint!

LEVEL SHIFTER

Running CMOS logic from 15 volt supplies reduces propagation delays and increases noise immunity, but connecting the 15 volt logic to other systems using TTL or even 15 volt CMOS can be tricky.

Going from a high voltage system to lower voltage logic isn't so hard. Just use a 14049 or 14050 hex CMOS buffer which will run from 5 volt supplies while accepting 15 volt input levels. Going the other way, from TTL to 15 volt CMOS for example, has up to now been more troublesome. When faced with this problem in the past I have resorted to using a transistor with a collector supply of 15 volts as a level shifter, but while this is practical for a few lines, the use of a transistor and three resistors for each channel can result in a bit of a clutter.

A new device from MITEL, the MD4101, solves this problem by providing a very comprehensive quad low to high voltage translation function. Comprehensive, because for each input you get a true and a complement output, each of which has three-state action controlled by a common Output Enable. The secret of the low to high conversion rests with the two V_{dd} supply pins (1 and 16) which have the restrictions that $Vdd0$ must be less than 18 volts, and $Vdd1$ must be less than or equal to $Vdd0$.

The MD4101 uses the successful MITEL ISO-CMOS process to achieve very fast operation, and it comes in a 16 pin plastic or ceramic package.

Fig. 1. Block diagram of the Echo Simulator

ECHO SIMULATOR

S.J. MUSGRAVE *

THIS inexpensive echo simulator is a very useful test set which is suitable for use with the PE Digisounder as well as many other types of echo sounders.

The straightforward circuit provides a stable output permitting variable depth simulation over the normal range of the equipment under test.

Construction is straightforward and the compact unit is connected, via a co-axial lead, as a replacement for the echo sounder's transducer.

The use of CMOS integrated circuits permits a wide range of supply voltages and the associated low current demand increases battery life.

CIRCUIT DESCRIPTION

The circuit consists of two monostable oscillators and an astable oscillator as shown in the block diagram of Fig. 1.

Monostable 'A' (IC1a, IC1b) provides a triggered variable time delay output to monostable 'B' (IC1c, IC2b) which controls the 'return' pulse duration. Astable oscillator (IC2c, IC2d), when gated produces a 150kHz square wave pulse

*Mr. Musgrave is a senior lecturer of Marine Electronics.

which is attenuated and coupled into the output socket. Thus, the generation of the 'return echo' pulse is delayed by a time determined by the period of monostable 'A'.

The circuit diagram is shown in Fig. 2. Two 4001B quad 2 input NOR gates are used to generate the 'echo return' pulses. Transmission pulses are coupled via C1 and detected by D1, R2 to produce a postive going trigger pulse applied via R1 to pin 2 of IC1a. When the input level exceeds the transfer voltage of the gate the monostable action of IC1a and IC1b is initiated. Due to the associated latching effect the trigger pulses need only be of short duration. Time delay is controlled by C2, R3, VR1 and varied by adjustment of VR1. The output from monostable 'A' (IC1a, IC1b) is inverted by IC1d to edge trigger monostable multivibrator 'B' (IC1c, IC2b). C3 and R4 control the 'return echo' pulse duration which is typically set to 0·5ms.
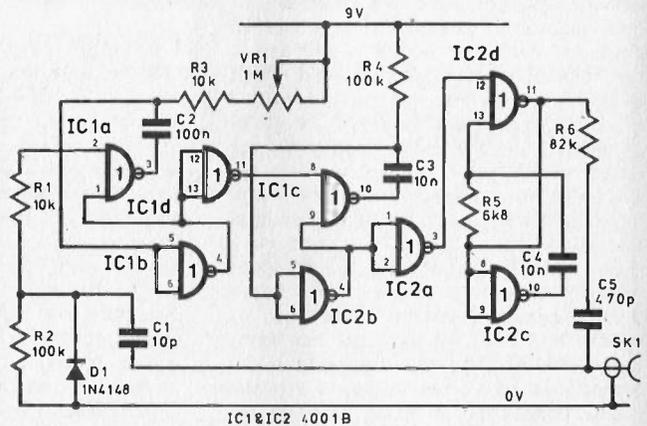
Fig. 2. Circuit diagram of the Echo Simulator

Gated astable multivibrator IC2c, IC2d is fed via inverter IC2a and when enabled by a logic '0' on pin 12 of IC2d oscillates at approximately 150kHz (determined by C4 and R5), producing a symmetrical square wave. Output from pin 11 of IC2d is applied to series attenuator R6 and coupled via C5 onto the common trigger/output socket.

The circuit is triggered repetitively by the output transmission pulses from the echo sounder and produces low level controlled duration pulses which are coupled as 'echo returns' after a simulated depth delay controlled by VR1.

CONSTRUCTION

The components are mounted on 0·1 inch Veroboard, as shown in Fig. 3, which in turn is edge mounted in the

Fig. 3. Veroboard layout

* LINK ON UNDERSIDE OF BOARD
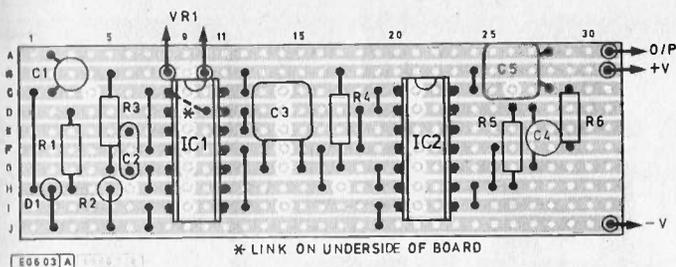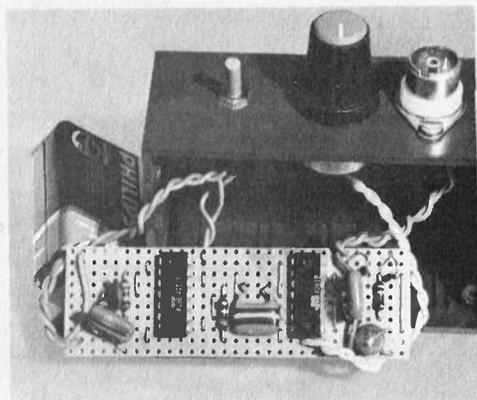
moulded supports within the plastic case. Holes are drilled in the side of the case for the on/off switch, the depth control potentiometer VR1 and the output co-axial socket.

It should be noted that a lead is included between the battery negative return line and the outer connection of the co-axial socket.

COMPONENTS...

Resistors
R1, R3	10k (2 off)
R2, R4	100k (2 off)
R5	6k8
R6	82k
VR1	1M linear

All resistors 0·25W 10% carbon.

Capacitors
C1	10p
C2	100n
C3, C4	10n
C5	470p

Semiconductors
D1	1N4148
IC1, IC2	4001B (2 off)

Miscellaneous
SPST miniature toggle switch
Veroboard (0·1in)
Plastic box
Battery connectors
Co-axial socket (surface mounting) with screws, nuts and washers
Control knob
Solder tag

No particular difficulties should be experienced with the construction and the circuit performs well over a range of component tolerances.

Note the inclusion of the connection on the rear of the board between pins 1 and 13 of IC1.

PARAMETERS

Component values have been chosen to provide an output pulse at approximately 150kHz—pulse duration 0·5ms and for operation over a simulated depth range 0–100 ft.

Should you want to modify these parameters for operation on echo sounders with different parameters this is possible by alteration of the following components.

VR1 — Range of simulated depth output
R4 — Pulse duration
R5 — Frequency of output
R6/C5 Output level.

Battery consumption is minimal and typically only 25µA–50µA dependent upon setting of VR1.
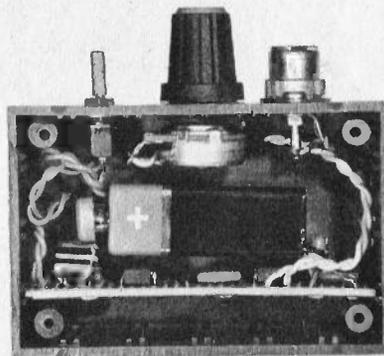
CALIBRATION AND TESTING

The unit can be used to ascertain the correct functioning of an echo sounder by connecting between the co-axial trigger/output socket on the 'test set' and the transducer output socket of the echo sounder under trial. With the variable depth control on the 'test set' at the anti-clockwise position the echo sounder should display an output depth indication around zero feet. Over the range of variation of VR1 the echo sounder display should be continuously variable between zero and 100 ft.
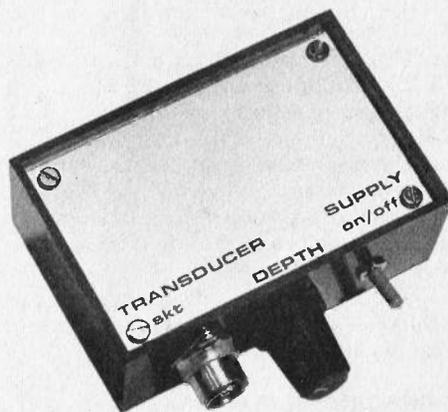
Initial calibration of the 'test set' can be achieved by operation on a 'known good' echo sounder. Direct readout from the echo sounder's depth scale will enable a range scale to be calibrated.

Subsequently the 'test set' may be used to assist in fault-finding by the elimination of the transducer and to check the calibration of an echo sounder. ★

Digital Design Techniques...

Tom Gaskell B.A.(HONS) ELEC. ENG.

THE last few years has been a very exciting time for everyone involved in electronics, from the raw beginner to the most qualified professional. It's been a time of rapid change, increasing complexity and sophistication, and dramatic reductions in the size and cost of electronic assemblies.

Those who have more than a basic understanding of electronics will know that the "microchip" (i.e. microprocessor) is merely a particular point along the road of digital integrated circuit development. After years of designing more and more complex devices, we now have the heart of a small computer in one cheap i.c. package; not a sudden invention, but part of a continuing evolution of electronic components, most of which is taking place in the field of digital, rather than analogue, circuitry.

You could be forgiven for feeling a little out of your depth by all this change around you, so here's where we come to the rescue with this new series on digital design. We're going to give you lots of facts, tips, and information. We'll point you in the right direction, give examples and guidelines. Most importantly, we'll look at 'tricks of the trade'; shortcuts, hints, safety margins, and practicalities that you won't learn any other way, apart from by spending hour upon hour finding it all out by experience.

Part 1 of this series is a theoretical introductory grounding in logic design, to establish some of the basic principles involved. There won't be any practical projects in the first part, but after that we'll have a number of "mini-projects" to build each month. We'll be starting off at 'gate level', and working up to microprocessors, so there's a lot of ground to cover, and we will be assuming a certain amount of knowledge initially.

WHAT YOU WILL NEED

As we work through experiments and projects, the parts lists and buying information will be provided as normal in PE. As a generality, we'll be using CMOS logic (for reasons given later) and fairly conventional passive components.

For instruments, you'll need a multimeter, the usual hand tools and preferably a logic probe and logic pulser—we'll have details on these later in the series. An oscilloscope is always useful, but by no means absolutely necessary, and we won't be assuming that you have access to one.

Part 1 Introduction to Logic...

Before we launch ourselves upon the detail of logic gates, Karnaugh/Veitch maps, etc., let us remind ourselves of what logic is all about; Yes/No decisions. Is a certain condition fulfilled; yes or no? Are certain voltages present; yes or no? Analogue voltages in circuits may have an infinite number of possible levels; all the circuitry must be based on a continuously variable signal level, but in logic it's a simple two state affair; yes or no? The more decisions that need to be made, the more complex the problem.

THE REPRESENTATION OF DECISIONS

We could say that if the answer to a particular question is 'yes', wave a red flag, and if it's 'no', wave a blue flag! Or for 'yes', turn on a light, and for 'no' switch the light off. Anything with two different states can be used to indicate an answer; for example, the operation of an electric drill, as in Fig. 1.1a.

There are two possible actions needed to cause the drill to run; it must be plugged into the wall, AND it must be switched on. Fig. 1.1a shows what happens to the drill for every possible combination of its switch and plug. For convenience, we could replace 'yes' by the number 1, and 'no' by the number 0.

Let's call the condition that the switch is in "condition A", the condition that the plug is in "condition B", and the drill running "result Q"; again, all for convenience. Fig. 1.1a is now changed into the 'shorthand' version, Fig. 1.1b. Because Fig. 1.1b tells the truth of the situation for every combination of conditions A and B, it is known as a 'Truth Table'.

This truth table can be simulated by using a simple electronic circuit with two inputs, A and B, and one output Q.

CONDITION		RESULT
Is the plug in the main socket?	Is the drill switched on?	Is the drill running?
NO	NO	NO
NO	YES	NO
YES	NO	NO
YES	YES	YES

Fig. 1.1a.

CONDITION		RESULT
B	A	Q
0	0	0
0	1	0
1	0	0
1	1	1

0 = NO
1 = YES

Fig. 1.1b. Truth table

Fig. 1.1c. The AND gate symbol

SWITCH A   SWITCH B

IF A AND B ARE BOTH ON, THE LIGHT IS ON

LIGHT Q
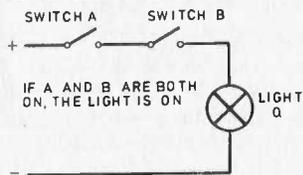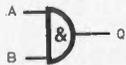
Fig. 1.1d. The equivalent circuit

We can say that number '1' in the truth table is a high voltage, and number '0' in the table is a low voltage. So, in this case, only when both inputs have a high voltage connected to them does the output Q go to a high voltage. This circuit is known as an AND gate (B AND A = Q); its symbol is shown in Fig. 1.1c. (Fig. 1.1d shows an equivalent simple circuit for this gate, using switches as the A and B conditions, and a lamp as the result Q.)

OTHER CONDITIONS

Although we've only looked at one example, that of an electric drill being represented by an AND gate, other conditions could apply. For example, A could be a simple switch, B could be another switch connected in parallel, and Q could be a light bulb. This time, if A OR B is operated, the light bulb Q will come on. The truth table for this is shown in Fig. 1.2a. The equivalent circuit is shown in Fig. 1.2b, and the symbol for this arrangement, which is known as an OR gate, is shown in Fig. 1.2c.

B	A	Q
0	0	0
0	1	1
1	0	1
1	1	1

0 = OFF
1 = ON

Fig. 1.2a. Truth table

SWITCH A
SWITCH B

IF A OR B IS ON THE LIGHT IS ON

LIGHT Q
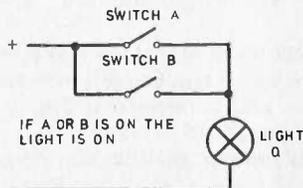
Fig. 1.2b. The equivalent circuit

Fig. 1.2c. The OR gate symbol

There are many more logic gates than just these two. In fact, we have AND, OR, NAND, NOR, EX-OR, and INVERT (sometimes called 'NOT'). There are even more, but they are not normally used. NAND and NOR gates are simply AND and OR gates with the 'Q' output reversed in state, i.e. the '1's become '0's and the '0's become '1's. The INVERT (or NOT) gate is a one input, one output gate which also reverses '1's and '0's; an inverted function is shown with a bar above it, e.g. $\bar{A}$, $\bar{B}$, etc., Fig. 1.3 shows a truth table encompassing all these gates and symbols.

THE EX-OR GATE

This is short for "EXCLUSIVE — OR". It means that the output Q = 1 if A OR B = 1, but not if A AND B = 1; in other words, it is an OR gate, but EXCLUSIVE of the conditions when both inputs are 1. The ordinary OR gate, for an equivalent reason, is sometimes known as "INCLUSIVE-OR" gate.

Note that this gate gives an output when the two inputs are not at the same logic level; it is sometimes referred to as a "NON-EQUIVALENCE" gate. An EX-OR gate followed by an inverter (technically an EX-NOR gate) is the reverse of this, its output is 1 if the two inputs are at the same logic level. Hence, it is known as an EQUIVALENCE gate; a very useful device, since it allows us to compare two logic levels with each other.

Finally, the EX-OR gate can be considered as a "programmable inverter". One input is the 'inverter' input, the other is a 'control' input. If the control input is at logic 1, the EX-OR gate inverts the input logic signal. If the control input is at logic 0, the EX-OR gate does not invert the input signal. In this case the gate acts as a BUFFER; i.e. a circuit whose logic output state is the same as its logic input state, although there is electrical isolation between them.

All the truth tables that we've looked at so far can be extended to many inputs, not just two. (With the exception of EX-OR, which is a bit of a problem, but you can't readily buy three (or more) input EX-OR gates anyway, so it doesn't really apply!) Again, for the output Q to be 1, A AND B AND C AND D, etc., must all be 1; or A OR B OR C OR D, etc., must be 1 to make the output 1, etc.

INVERTERS

Note that an inverter can be made in several ways; either by using a simple (INVERTER) gate, or by using NAND, NOR or EX-OR gates. (We've already looked at the EX-OR way of doing it.) To use either NAND or NOR, simply connect a gate's two inputs together! Working through the truth table of Fig. 1.3 will show that the gate now behaves as an inverter.

WHY ARE WE DOING ALL THIS?

Since we are talking about two state (or "binary") logic; 1 or 0, high voltage or low voltage; yes or no, etc., the circuit operation to implement these logic gates can be fairly simple. Transistors can be switched hard on or hard off, without having to be carefully biased into the linear region as they would need to be in most analogue circuits.

We can make the difference between the voltage levels used quite considerable; for example, we could say that logic 0 is below $\frac{1}{3}$ of the power supply voltage, and logic 1 is above $\frac{2}{3}$ of the supply. Circuit design then becomes non-critical and simplified because of the "invalid" area in the middle between $\frac{1}{3}$ and $\frac{2}{3}$ of the supply voltage; also, interference effects are cut down, because any spurious voltages present on a piece of wire must be very large to cause the logic level to appear to have changed from a 1 to a 0, or vice versa. Furthermore, 1's and 0's can be used as numbers in codes for doing arithmetic and code manipulation.

INPUTS		AND	OR	NAND	NOR	EX-OR	INVERT	
B	A	Q	Q	Q	Q	Q	$\overline{B}$	$\overline{A}$
0	0	0	0	1	1	0	1	1
0	1	0	1	1	0	1	1	0
1	0	0	1	1	0	1	0	1
1	1	1	1	0	0	0	0	0

SYMBOLS →

Fig. 1.3. Combined truth table for all logic gates

In conclusion, it seems that using 1's and 0's is a versatile, simple and effective way of processing and representing logical information. It can, however, get a little complex if dealt with on too simplistic a level, so we've got to bring in some rather unusual mathematics to help us design logic networks.

BOOLEAN ALGEBRA

In 1847, George Boole, an English mathematician, invented a mathematical system for manipulating binary numbers (1's and 0's) as a way of manipulating logical expressions described by the Ancient Greeks. And everyone thought "How clever!!" And "How impractical!!". However, electronic logic gates have given a new relevance to these mathematical techniques and Boolean expressions are used throughout digital logic design today. When we add the techniques of 'Karnaugh/Veitch mapping' to Boolean algebra we have a way of planning, simplifying and optimising networks of gates, which can enable you to design very complicated circuits and systems in the most efficient way possible.

BASIC EXPRESSIONS

Boolean algebra writes OR as + (i.e. the conventional add sign) and AND as . (i.e. the conventional multiply 'dot'). Sometimes AND is written as the multiplication sign x, but most usually the two variables are simply written adjacent to each other. For example, AB is the same as A.B is the same as A AND B. Pretty well the reverse of what we expect! In fact, the symbols are chosen to make it very easy to perform

PRACTICAL ELECTRONICS SYMBOL	AMERICAN MIL-SPEC SYMBOL	BRITISH STANDARDS SYMBOL	GATE TYPE	BOOLEAN EXPRESSION
			AND	Q = AB
			OR	Q = A+B
			NAND	Q = $\overline{AB}$
			NOR	Q = $\overline{A+B}$
			BUFFER	Q = A
			INVERTER (NOT)	Q = $\overline{A}$
			EX-OR (NON EQUIVALENCE)	Q = $A\overline{B}+\overline{A}B$ THIS CAN ALSO BE WRITTEN Q = A⊕B

`EG608`
Fig. 1.4. Boolean expressions for the gates

a fairly conventional type of arithmetic on the logic expressions, as we'll see later.

Invert, or NOT, is shown as a bar above a letter or expression:

The inverse of A is $\overline{A}$

The inverse of A OR B (i.e. A + B) is $\overline{A + B}$ (i.e. A NOR B). Fig. 1.4 shows the Boolean expressions for gates.

Note that the EX-OR function has a combination of terms. Looking back at Fig. 1.3 we see that for Q = 1, A must equal 1 and B = 0, or B must equal 1 and A = 0. We can combine this in the expression shown, so:

Q = 1 when A = 1 and B INVERTED = 1 (i.e. when A = 1 AND B = 0) OR Q = 1 when A INVERTED = 1 and B = 1 (i.e. when A = 0 AND B = 1) Hence, Q = $A\overline{B} + \overline{A}B$.

This expression demonstrates how we can start to use Boolean algebra in a similar way to other arithmetic. Assuming just the variable A to start with, here are the rules:

A + A = A (1)	AA = A (6)
A + $\overline{A}$ = 1 (2)	A$\overline{A}$ = 0 (7)
$\overline{A}$ + $\overline{A}$ = $\overline{A}$ (3)	$\overline{A}\overline{A}$ = $\overline{A}$ (8)
A + 1 = 1 (4)	A.1 = A (9)
A + 0 = A (5)	A.0 = 0 (10)

OR EXPRESSIONS   AND EXPRESSIONS

Brackets can be used, as in normal arithmetic. For example, take the expression:

Q = A + A$\overline{B}$

This is the same as Q = A (1 + $\overline{B}$)

And, since 1 + $\overline{B}$ = 1 from rule (4) above (i.e. ANY variable + 1 = 1)

Then Q = A

This is an example of factorisation and simplification.

DE MORGAN'S LAW

Let's draw out a truth table, and look at some extra functions besides the normal AND, NAND, etc., see Fig. 1.5. Looking across at the columns for the 'new' functions we have drawn, we can see that they each have a perfect match in one of the 'old' functions (AND, OR, NAND or NOR) that we drew up. If the columns match up, then the functions at the heading of those columns must also match up.

INPUTS		AND	OR	NAND	NOR	'NEW FUNCTIONS'			
B	A	AB	A+B	$\overline{AB}$	$\overline{A+B}$	$\overline{A}\overline{B}$	$\overline{A}+\overline{B}$	$\overline{\overline{A}\overline{B}}$	$\overline{\overline{A}+\overline{B}}$
0	0	0	0	1	1	1	1	0	0
0	1	0	1	1	0	0	1	1	0
1	0	0	1	1	0	0	1	1	0
1	1	1	1	0	0	0	0	1	1

Fig. 1.5. Truth tables for logic gates with "new functions"

For example, the column for the NAND function matches the column for the function $\overline{A} + \overline{B}$. Hence, the NAND function must be the same as $\overline{A} + \overline{B}$!

Looking through the truth table, we can see the following:

AB is the same as $\overline{\overline{A} + \overline{B}}$

A + B is the same as $\overline{\overline{A}\overline{B}}$

$\overline{AB}$ is the same as $\overline{A} + \overline{B}$

$\overline{A + B}$ is the same as $\overline{A}\overline{B}$

This demonstrates DE MORGAN'S LAW perfectly; in each case we have an expression which can be written in two different ways; one in AND or NAND terms (e.g. AB) and the other in OR or NOR terms (e.g. A + B).

De Morgan's Law states that to change any expression into its equivalent form:

1) Change the variables (A becomes $\overline{A}$, $\overline{B}$ becomes B, etc.).

2) Change the connective (+ becomes ., . becomes +).

3) Change the <u>WHOLE EXPRESSION</u> ((expression) becomes $\overline{(expression)}$, $\overline{(expression)}$ becomes (expression).

4) Change any 1's to 0's, and any 0's to 1's.

A whole equation does not have to be changed at once; you can change just a small part of it:

e.g. Take the equation $Q = D(\overline{A} + B) + B(A + C)$

Let's change the expression $(\overline{A} + B)$ by De Morgan;

so, $(\overline{A} + B)$ changes into $A\overline{B}$

The original equation now becomes $Q = DA\overline{B} + B(A + C)$. This could now be expanded and factorised further, and De Morgan's Law applied again if wished; there is no limit to how many times or to how many terms the law is applied. This is one of the most useful laws in the whole field of logic design; with it you can change any 'AND' type of expression to an 'OR' type, or vice-versa, enabling simplification and rationalisation of circuit.

A WORKED EXAMPLE IN LOGIC DESIGN

Rather than look extensively at every possible mathematical 'trick' and manipulation, we'll just work through one example of a practical design problem, to show a typical approach to Boolean logic design. We'll first design a network using mathematics to factorise and simplify the equations and obtain a practical circuit; then we'll do it all over again using a "Karnaugh/Veitch map", which is a fast and simple way to avoid using any maths at all!

THE VOTING SYSTEM

We are asked to design the circuit of a voting system for three voters and one chairman. The chairman is allowed to throw a casting vote if the three voters do not reach unanimous decision; if he votes 'YES' he adds 1 to the total vote; if he votes 'NO' he subtracts 1 from the total vote. The vote is carried (i.e. the answer is 'YES') if 2 or 3 votes in total (including the chairman's) are cast in its favour, otherwise the vote is 'NO'.

Let's call the total 'YES' vote 'Y', and the chairman's vote 'D'. We can draw up a truth table of each possible condition; see Fig. 1.6.

CHAIRMAN 'D' (If asked)	VOTERS C B C			TOTAL 'YES' VOTES	YES VOTE 'Y'	COMMENTS
NOT ASKED	0	0	0	0	0	Unanimous decision
0	0	0	1	0	0	Chairman votes no which subtracts one from the total vote
0	0	1	0	0	0	
0	0	1	1	1	0	
0	1	0	0	0	0	
0	1	0	1	1	0	
0	1	1	0	1	0	
NOT ASKED	1	1	1	3	1	Unanimous decision
NOT ASKED	0	0	0	0	0	Unanimous decision
1	0	0	1	2	1	Chairman votes yes which adds one to the total vote
1	0	1	0	2	1	
1	0	1	1	3	1	
1	1	0	0	2	1	
1	1	0	1	3	1	
1	1	1	0	3	1	
NOT ASKED	1	1	1	3	1	Unanimous decision

0=NO If the total vote (including chairman) is two or three
1=YES then the vote is carried (i.e. Y=1). Note the total votes cast are shown in conventional numbers (not 0's and 1's).

Fig. 1.6. Truth table for the voting system

BOOLEAN EQUATIONS FOR THE VOTING SYSTEM

Our Boolean equation can be drawn up from the truth table by listing every set of variables (A, B, C, D) which give an answer 'YES', i.e. Y = 1. We can see that Y = 1 if A AND B AND C are 1, OR when A AND D are 1, OR when B AND D are 1, etc. So our basic Boolean equation for the answer Y is:

$Y = ABC + AD + BD + ABD + CD + ACD + BCD + ABC$ (EQUATION 1).

We can factorise this equation exactly as in conventional algebra:

$Y = (ABC) + (ABC) + CD(1 + A + B) + AD + BD(1 + A)$

Looking back at our rules of Boolean algebra: Rule (1) says that A + A = A, Rule (4) says that A + 1 = 1 and Rule (9) says that A.1 = A. (These rules still apply whether we talk about A, B, C, D, or even (ABC) as the variable!) Using these rules to simplify the brackets, we obtain the equation:

$Y = ABC + CD + AD + BD$

Factorising once again:

$Y = \underbrace{ABC}_{\text{FIRST TERM}} + \underbrace{D(A + B + C)}_{\text{SECOND TERM}}$

This would seem to be the simplest form in which we can get it, so it's now ready to be translated into a circuit:

1) The first term, A AND B AND C, is obviously a 3-input AND gate.

2) The second term is a 3-input OR gate, 'AND—ed' with the D input signal.

3) The whole expression consists of the first term OR the second term.

The complete circuit is shown in Fig. 1.7a. The majority of gates used today are NOR and NAND, rather than OR and AND, since the extra inversion is a very useful feature. If we go back to De Morgan's Law, we see that we can replace an OR gate with a NAND gate if we invert its inputs; i.e. A + B is the same as $\overline{AB}$. Likewise with AND and NOR gates; i.e. AB is the same as $\overline{A} + \overline{B}$. Fig. 1.7a has been re-drawn into the more normal NAND and NOR configuration, as shown in Fig. 1.7b.
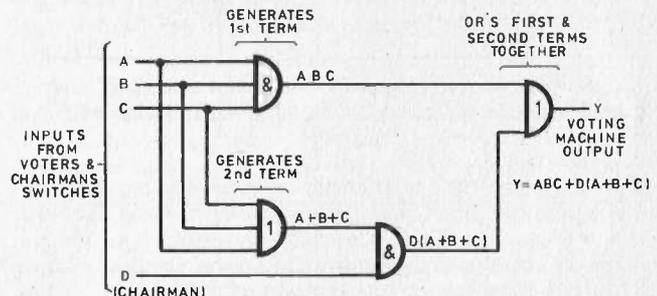


**Fig. 1.7a. Basic circuit**
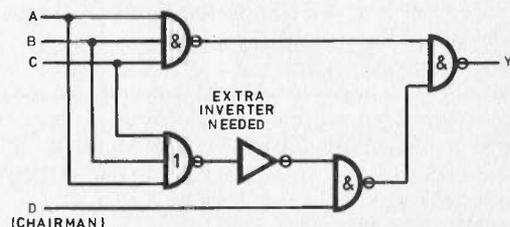
Fig. 1.7b. Circuit using NOR and NAND gates

THE KARNAUGH/VEITCH MAP

The mathematics we've just done might be a little difficult to understand at first attempt, but work through it and

hopefully it'll all fall into place. You can imagine how complex it gets, however, when there are not just a few logic gates, as in Fig. 1.7, but dozens! Fortunately, we have a much quicker way of going from a truth table to a circuit. This method, the Karnaugh/Veitch map, is shown in Fig. 1.8, and we shall use it to design the voting system once again. (Note that many books refer to this purely as a 'Karnaugh Map', and sometimes have slightly different ways of labelling the squares. We are actually using the 'Veitch' notation for the squares, which has been found to make the system somewhat more straightforward to understand and use.)
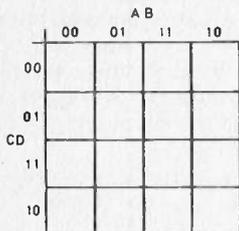

Fig. 1.8a. The basic map
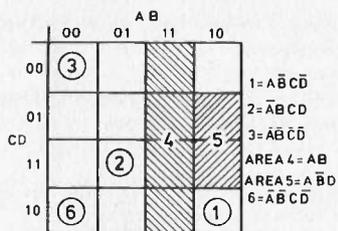
Fig. 1.8b. Allocation of squares
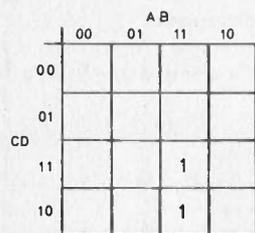

Fig. 1.8c. Term 8 of equation 1 (ABC)
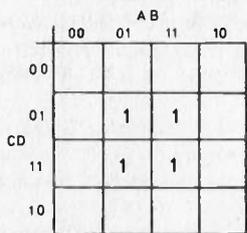

Fig. 1.8d. Term 3 of equation 1 (BD)
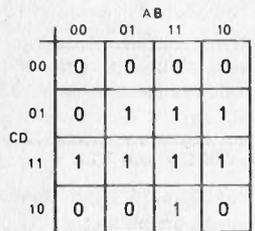

Fig. 1.8e. The full Karnaugh/Veitch map of equation 1
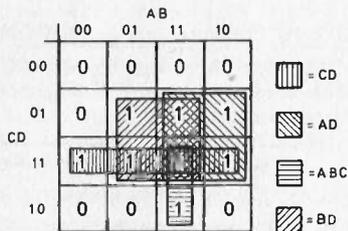
Fig. 1.8f. Map with the groups marked in

FILLING IN THE MAP

First draw the basic map or grid, as shown in Fig. 1.8a, on a piece of paper. Each square represents one condition only of the four variables, A, B, C and D. The vertical columns are terms in A and B, and the horizontal rows are terms in C and D. The numbers around the outside of the map show the relative states of the variables for that particular row or column; for example, the most right hand vertical column has 1 0 at the top of it; this means that for this column $A = 1$ and $B = 0$. We can say that the column $= 1$ if $A = 1$ AND $B = 0$, so the column is $A\bar{B}$.

This notation extends to cover all areas and squares in the map; each square has its own unique set of variable conditions. Hence, in Fig. 1.8b, the square number (1) is vertically in the column $A = 1$, $B = 0$, i.e. the column $A\bar{B}$, and horizontally in the row $C = 1$, $D = 0$, i.e. the row $C\bar{D}$.
Hence, square (1) is $A\bar{B}C\bar{D}$.
Similarly, square (2) is $\bar{A}BCD$ ($A = 0$, $B = 1$, $C = 1$, $D = 1$).

It can be seen that each square varies from every adjacent square to it by only 1 in any direction (except diagonal!). This applies off the edge of the map, too; imagine that the whole map was wrapped round on itself as if drawn on the surface of a small ball, with opposite sides touching. So, square (3)

in Fig. 1.8b is actually adjacent to square (6); again, they only differ by one change of state.

As you can see, the names that we are giving to squares and areas look just like terms in an equation. That's exactly what they are! Let's go back to equation (1), the basic equation for our voting system:

$$Y = \underset{\text{TERM 1}}{ABC} + \underset{\text{TERM 2}}{AD} + \underset{\text{TERM 3}}{BD} + \underset{\text{TERM 4}}{ABD} +$$
$$\underset{\text{TERM 5}}{CD} + \underset{\text{TERM 6}}{ACD} + \underset{\text{TERM 7}}{BCD} + \underset{\text{TERM 8}}{ABC}$$

We can fill in a basic map by putting a '1' in each and every square relating to a term in this equation. If more than one term covers any particular square, don't worry; if there's already a '1' there it doesn't need another. For example, Fig. 1.8c shows the term ABC, just two squares and Fig. 1.8d shows the term BD; four squares.

The full map for equation (1) is shown in Fig. 1.8e; as you can see, if there are any blank spaces we put a '0' in them.

GROUPING

We must now look for groups of '1's in the map; a group consists of 2, 4, 8 or 16 '1's adjacent to each other in squares or rectangles, with no '0's included. (If there are 16 '1's, then the map is full, and the solution is $Q = 1$; this is a rare and somewhat trivial case!) Groups can "fold round" the sides or the top. For example, in Fig. 1.8e you could form a '2 group' from square $A\bar{B}CD$ and square $\bar{A}\bar{B}CD$.

Groups that overlap each other are a very good thing, as they simplify the expression. You should make each group as large as possible and with as much overlap as possible, so long as by doing this you still enclose at least one '1' which would not otherwise have been contained in any other group. Fig. 1.8f shows the groups that we have selected. There is considerable overlap, yet only a small number of groups (considerably less than the number of terms in the original equation (1)), which is a very good thing.

DERIVING THE FINAL EXPRESSION

To derive the final, simplified Boolean expression from the map is now a simple matter of inspection, which is effectively the reverse of filling up the map with '1's in the first place. Inspect each group and write down only the variables which are common to that whole group.

For example, the '4 group' on the extreme right of the map contains the following squares:

$$\left.\begin{array}{l} A\,\bar{B}\,\bar{C}\,D \\ A\,\bar{B}\,C\,D \\ A\,B\,C\,D \\ A\,B\,\bar{C}\,D \end{array}\right\}$$ The only variables which are the same in all four squares are A and D. (The other two vary between squares).

As shown in Fig. 1.8f, that group is simply written as AD. All the groups can be labelled in exactly the same way, just by looking for the variables that are common to all squares in that group.

We can now write down the terms for all groups in the map of Fig. 1.8f. They are AD, BD, CD, ABC.

The final equation is simply all these terms 'OR'–d together; $Y = AD + BD + CD + ABC$.

Since D is common to all the first three terms, it is better to factorise and rearrange the equation to:
$Y = ABC + D(A + B + C)$ YES!! We're back to the answer! This is now drawn out as a circuit in exactly the same way as our original mathematical method.

CONCLUSIONS ABOUT BOOLEAN ALGEBRA

So there we have it; it seems like a real mouthful, doesn't it?! Karnaugh/Veitch maps are very, very fast to use once you've practised a little—try it and see! Make up your own basic equations, and try to simplify them and draw the cir-

cuits. Make sure that you start off with the basic equation though, with all the terms separated, as you can end up in difficulty if you start to simplify it mathematically then do a Karnaugh/Veitch map.

LOGIC IMPLEMENTATION

Essentially, we need to use two voltage levels; one for logic 0, and another for logic 1. There must be a 'threshold', or point of changeover between the logic 0 state and logic 1 state; below this threshold voltage the level is logic 0, and above it the level is logic 1. In practice, there are actually two thresholds, with a 'dead-band' in between, in which the inputs and outputs are in a fairly indeterminate state. If we take a simple inverter, as in Fig. 1.9, we can draw its inputs and outputs together on a graph. (Most logic gate inputs and outputs behave in the way shown.)
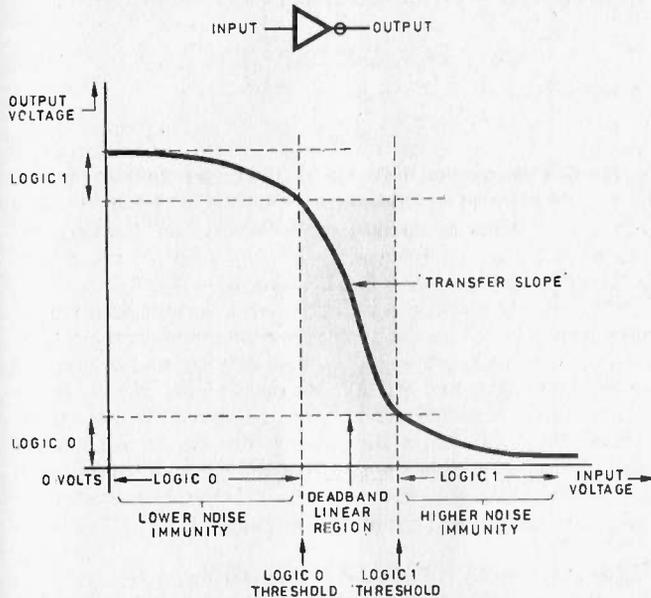

Fig. 1.9. Typical input/output graph for an inverter

The noise immunity for both logic 0 and logic 1 is defined as the amount of voltage change that a 'perfect' input can vary by before the output comes OUT of the logic state in which it currently sits. Note that this is a very complex matter! The exact nature of input/output characteristics causes different logic families to behave in different ways, especially in the deadband region. For most considerations though, Fig. 1.9 is a good approximation.

In the deadband region, the device has a tendency to act linearly, i.e. as a pure amplifier with defined gain. Outside this region, however, it is very much a 'saturated' amplifier; either hard off or hard on. All logic inputs/outputs can be drawn in a similar way to this graph, although in a gate with multiple inputs the effect of changing several inputs simultaneously can complicate the diagram.

LOGIC FAMILIES

A 'family' is a particular type of circuit design for logic i.c.s, such that all devices within this family will interact together and will drive each other's inputs satisfactorily.

Today we use two main groups of logic family; that based on 'bipolar transistors', of which TTL (Transistor–Transistor–Logic) is the most widely used, and that based on MOS FETs (Metal Oxidised Semiconductor Field Effect Transistors), known generally as MOS, the most common family of which is CMOS (Complimentary–MOS). TTL has various sub-families; SCHOTTKY input types (see later in this article), LOW POWER types, and a mixture of the two. MOS has

CHARACTERISTIC	CMOS	TTL (standard)
Normal supply voltage	+3 to 18V	+5V only
Typical logic 1 output level Typical logic 0 output level	Above 70% of supply Below 30% of supply	Above 2·4V Below 0·4V
Propogation delay (time difference between input state changing and output state changing)	40ns	6ns
Maximum usuable frequency	2 to 4MHz	50MHz plus
Typical power consumption per gate, for a fixed logic state*	Less than 1µW	22µW
Fan out (i.e. how many gate inputs can a gate output drive simultaneously)	50 plus	10
Worse case noise immunity	30 to 40% of supply	1V
Cost (typical)	4p per gate	3p per gate
Handling	Handle with care	No special precautions
Analogue signal handling capability	Analogue switches (i.e. analogue signals controlled by digital signals) available cheaply	None
Input impedance	Very high	Fairly low

*With CMOS power consumption rises with speed; it can become the same as TTL when it gets in the range of several hundred kilohertz.

Fig. 1.10. Comparison between CMOS and TTL

not only CMOS, but also NMOS and PMOS, which are used mostly for memory i.c.s and very large and complex i.c.s.

There are also such families as I²L (Integrated–Injection–Logic) which achieves an incredible number of separate devices on each i.c. 'chip' (the active slice of silicon at the heart of an i.c.), and ECL (Emitter–Coupled–Logic) which is the highest speed logic family readily available. These families, however, are rare, and are used only by specialists.

For most people the choice of logic family is between ordinary TTL or low power Schottky TTL (which is abbreviated to LSTTL), and CMOS. A comparison of their characteristics is shown in Fig. 1.10. It can be seen that CMOS power consumption (under normal conditions) is very much lower than TTL. A large p.c.b. full of TTL devices can easily take several amps of current, which necessitates very expensive p.s.u. designs. Also, TTL requires a very low impedance, stable voltage, well regulated supply, whereas CMOS needs only a very low power supply which need not even be regulated in many applications, and can be wide ranging in voltage.

TTL can 'sink' an output current of several milliamps—enough to directly drive l.e.d.s, etc., whereas most (but not all) CMOS cannot do this. CMOS has a much better noise immunity than TTL, especially at high supply voltages, and this can be a great help in maintaining a satisfactory performance in electrically noisy environments. Because of its much lower power dissipation, CMOS can have many more gates packed into the same area of i.c. chip than can TTL and

hence more complex circuits can be packed into less area using CMOS, keeping costs down.

HANDLING

TTL needs no special handling precautions; just be gentle with it, use a 'reasonable' soldering iron and work quickly. Try not to short the outputs to anything, although if you do, it won't necessarily be the end of the world!

CMOS needs special care. Because of its input impedance of several hundreds of Megohms, static charges built up on the body, and on tools, can damage the input circuitry; the early 'A' series of CMOS was especially vulnerable to this problem. The current 'B' series has been improved, with a diode and resistor network on each input to try and hold stray input voltages between the two supply rails; however, certain precautions should still be taken:

Avoid touching the pins with your hands. Use an earthed soldering iron, and try to avoid working with all-nylon shirts (or blouses) and nylon carpet. Best of all, work on a large piece of metal, fully earthed. Again, avoid short circuits, especially to high voltages, as in this case they can easily blow up the i.c. Solder the i.c.s to the circuit board after all the other components have been added, or use i.c. sockets and plug the devices into the sockets fairly quickly to avoid getting the package too hot. Whatever else happens, never put a signal into a CMOS i.c. until its power supply is switched on.

LOGIC AND PULSE SHAPING

Besides simply combining inputs together to give particular outputs, simple logic gates can also shape logic signals, both in amplitude (i.e. to clean-up noise effects and turn slowly charging voltages into precise logic levels), and in time, by delaying logic changes or by producing pulses from simple changes in logic level.

SCHMITT TRIGGERS

A Schmitt Trigger is a circuit which does nothing until the input exceeds a certain voltage threshold level; at this point the output suddenly changes logic state. If the input immediately starts decreasing, the output does not immediately change back—the input voltage has to drop a considerable way below the original threshold level before the output changes. The 'gap' between thresholds for positive versus negative changes in input is known as hysteresis. See Fig. 1.11.
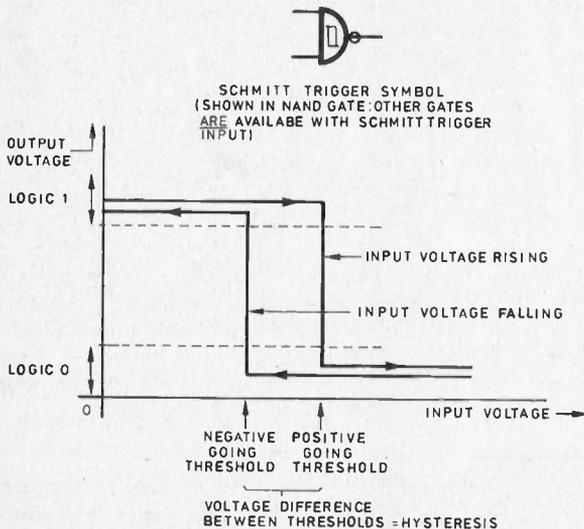
Fig. 1.11. The Schmitt trigger

The Schmitt Trigger can prevent noise on a slowly changing input voltage from causing spurious logic changes when the voltage reached the linear or 'deadband' area of logic operation; the 'snapping across' action turns any slow change into a definite logic state change. Most logic families have some of the more common gates available with Schmitt Triggers on each input; the symbol for a gate with this circuit added is shown in Fig. 1.11. We shall see later how the features of the Schmitt Trigger can be exploited.

LOGIC FOR DELAYS AND PULSES

The circuits we have looked at so far all work very rapidly; the "Propagation Delay" and "Maximum Usable Frequency" information of Fig. 1.10 shows this. It may be, however, that we want to deliberately slow down circuit operation to wait for a fixed time period before changing. This can be achieved by using simple resistor/capacitor networks; see Fig. 1.12.
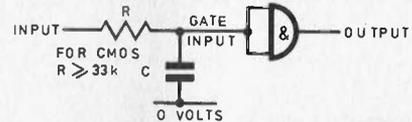
For CMOS resistor R should be 33k or greater (ideally) to prevent an overload of the previous stage
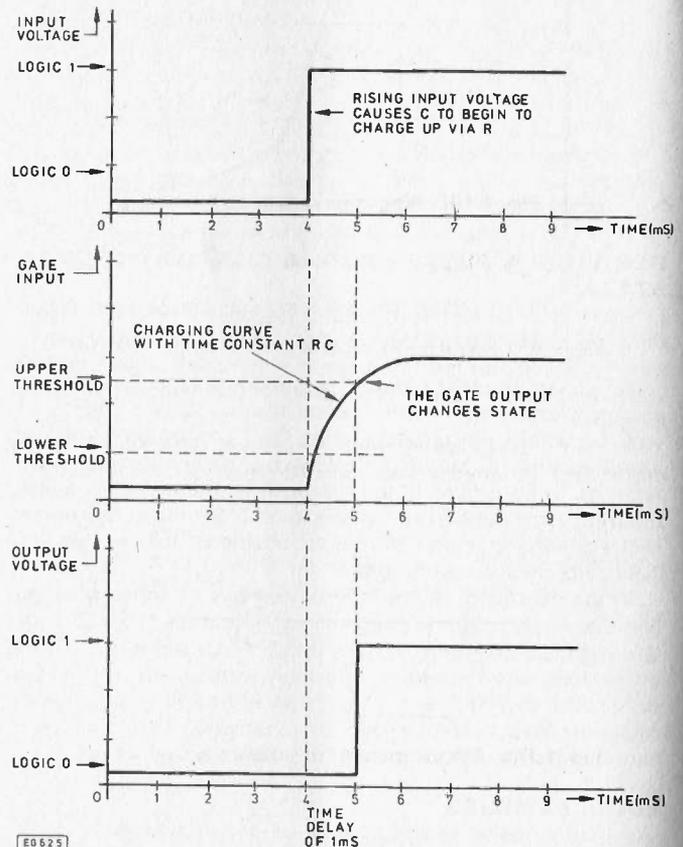
Fig. 1.12. Simple time delay

As can be seen, when the input goes high, the capacitor is slowly charged up via the resistor, until the voltage reaches the upper threshold; in our example, this occurs 1ms after the input goes high. So if the input changes at a time of T = 4ms, then the input to the gate (it can be any logic gate)

passes the gate's upper threshold point at T = 5ms, and hence the output of the gate changes to a logic 1. The effect of all this is to delay that logic change by, in this example, 1ms. A similar process will occur when the input signal changes back to logic 0. Note that the delay time will depend on the value of R and C used; the conventional capacitor charging and discharging equations will give the exact times at which various networks reach the threshold points, but a simple guide (for all R/C timing delays) is that the time taken is approximately the resistance in ohms multiplied by the capacitance in farads.

PULSE 'STRETCHING'

In a similar way, short pulses can be 'stretched' or made longer in duration, without delaying both the positive pulse edge (i.e. 0 to 1 change) and the negative pulse edge (i.e. 1 to 0 change). See Figs. 1.13a and 1.13b.
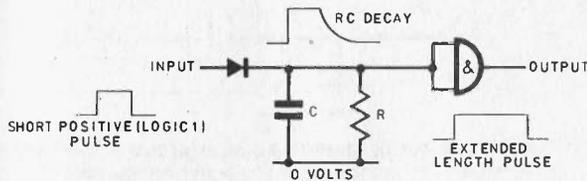
Fig. 1.13a. Positive pulse 'stretcher'
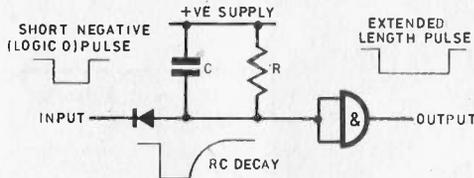
Fig. 1.13b. Negative pulse 'stretcher'

DERIVING A PULSE FROM A CHANGE OF LOGIC STATE

We may wish to turn a change in logic level into a short duration pulse, e.g. to reset a piece of circuitry when a button is pressed, but not to prevent that circuit from starting to work again even if the reset button is held firmly down for a long time.

As with pulse stretching, there are different circuits, depending on whether we want to generate a pulse on the

Fig. 1.14a. Simple circuit for positive going edges

Fig. 1.14b. Simple circuit for negative going edges
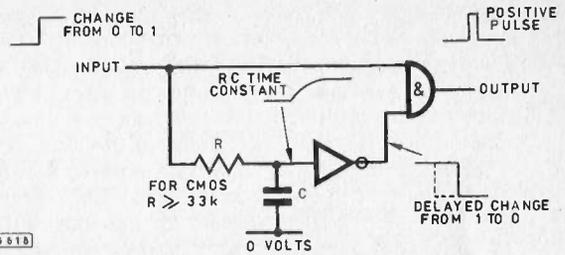
Fig. 1.14c. More sophisticated circuit for positive going edges
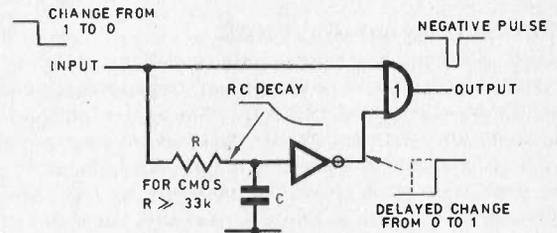
Fig. 1.14d. More sophisticated circuit for negative going edges

positive going edge (0 to 1) or the negative going edge (1 to 0) of the input. See Figs. 1.14a and 1.14b. These are fairly simple but effective circuits; more sophisticated circuits to perform the same function are shown in Figs. 1.14c and 1.14d. These use more components, but avoid large current surges (via the capacitor and diode) which can sometimes cause spurious pulses in the simpler circuits.

RULES OF THE GAME

These circuits are largely self-explanatory; they are simple exercises in R/C networks. There are pitfalls to avoid, though! Do make sure that the diodes are in, and the right way round, as they not only define which 'edge' the circuit operates on, but also prevent logic gate inputs being taken outside the supply rails by the capacitors. Be careful not to use too large a value of capacitor; remember that the previous circuitry, usually another logic gate, has to charge up this capacitor, often via a series diode only, and too large a capacitance can cause large currents to flow from the previous gate's output stage. In this respect, the circuits in Figs. 1.13b and 1.14a are better, because the maximum current flow is when the preceding gate output is at logic 0, and hence is 'sinking' current. (Logic 1 on an output 'sources' current, i.e. routes current from the positive supply rail to the output, and logic 0 'sinks' current, i.e. routes current from the output down to the negative or 0 volts supply rail.) Both CMOS and TTL are considerably better at sinking current than they are at sourcing it, in general. (The best circuits shown, for minimising surge currents, are, of course, those in Figs. 1.12, 1.14c and 1.14d.) As a rough guide, for CMOS, keep capacitors as small as possible; it would be nice to keep them below 1nF but probably impractical, so keep them below 1μF! Resistors should be below 2 or 3 Megohm, and above 1k. As we work through the series, we'll see typical values for R/C delays being used.

ACCURACY

The thresholds of CMOS vary considerably between different devices and packages; TTL also varies, but not so much. Since the thresholds determine at which point the
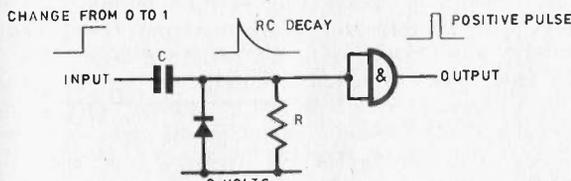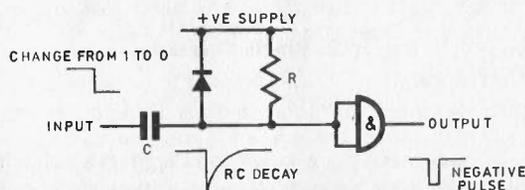
gate changes logic state, and hence the time delay, the timing is obviously not a very well defined figure. For CMOS, the time delay can vary by up to $\pm 60\%$ of nominal, although in practice it would be rare to vary as much as this. However, this does point out that for critical timing applications, these circuits should not be used! Go instead for the more expensive but more accurate timer or monostable i.c.s, like the 'CMOS 555' timer, or the 4047 or 4528 devices. These are integrated circuits specially designed for generating timing pulses of fairly high accuracy and of widely variable durations; up to several minutes in some cases. Being specifically designed for timing applications, they do not suffer any of the current surge problems associated with some simple R/C circuits. We'll look at some of these i.c.s later in the series.

SPROGGIES AND GLITCHES

The R/C circuits shown are excellent in non-critical applications, but they have 'hidden' degeneracy effects, especially so in the case of CMOS due to the fact that in the region around its threshold points it can become quite linear, i.e. its gain becomes fairly low, and it can act as an amplifier. I've even seen circuits for hi-fi preamps built out of CMOS gates, although I doubt if they'd meet DIN standards!

If a circuit has any noise or spurious voltages present on the input signal to a gate, then as the input voltage slowly passes through the linear region, noise can falsely shift the voltage below the lower threshold and above the higher one several times, causing spurious output pulses; sproggies and glitches. See Fig. 1.15. In many cases this noise effect might not matter; it all takes place over a very short space of time, and if the circuit only lights a l.e.d. or turns on a relay, or something similar, then no harm is done. But if this is the input to a counting device, for example, it will count all these spurious pulses!

Once again, the easiest (but most expensive) way out is to put in a CMOS 555 (not an ordinary 555, as they do horrible things to the power supply rails!) or a monostable i.c. In
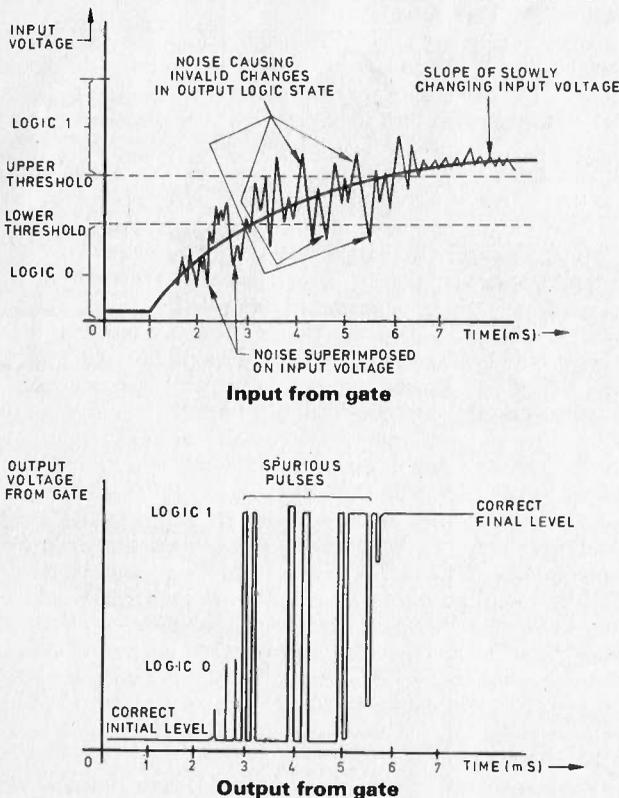
many cases, however, the gate used can be changed for a Schmitt Trigger input gate, as described earlier, and this will often 'clean up' the logic signal effectively. Note also that power supply spurious pulses can also manifest themselves as spurious pulses in logic signals, more so in TTL than in CMOS circuits. (We'll look at the problem of power supplies in a later article.)

INTERCONNECTING CIRCUITS

As a final note of caution when using this type of circuit, don't try driving other logic gates off points within an R/C timing circuit. Take a look at Fig. 1.16a. Output B will be
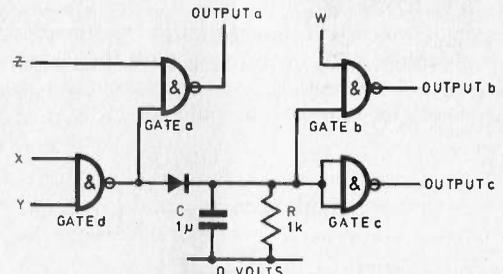
Fig. 1.16a. Badly designed circuit
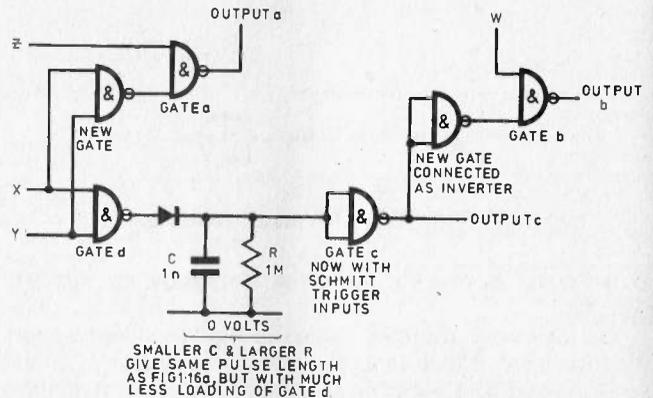
Fig. 1.16b. Improved design of the same circuit

noisy, as will output C, for reasons just described, and it would be better if gate B's input was taken from the output of gate C, inverted. Gate A is fed from the output of gate D, which will have a very poor 'shape' to its logic change; full of noise and very slow, due to it trying to charge C via the diode. This part of the circuit should be re-designed; it will not work properly. Gate C should be changed to a Schmitt Trigger input type of gate, to clean up the logic signal from the R/C timing circuit. The R/C network itself should be changed in value; 1k and 1μ will present a very considerable load to the output of gate D, causing poor charging characteristics and hence a noisy and spurious voltage-filled waveform. The same time constant can be achieved with much better values of components; 1n and 1M can be used. The re-designed circuit is shown in Fig. 1.16b.

NEXT MONTH:

Next month we'll start looking at more practical aspects; designing with gates, the sort of loads that can be driven, input requirements, p.s.u.'s, interfacing, and other associated subjects. We'll also start building the first of our 'mini-projects', and we'll look at breadboarding and constructional techniques.

Input from gate

Output from gate

Fig. 1.15. Spurious pulses caused by noise effect

Minute Chimer

James S.B. Dick

AS ANYONE who has ever processed photographic material in total darkness will know, there is nothing so annoying as not knowing how time is passing—and then having one's inner sanctum of tranquility shattered by the timer bell. The device described here is designed to restore some peace into the darkroom by chiming the minutes as they pass; one bleep after one minute, two bleeps after two minutes, and so on up to fifteen minutes, covering a very useful photographic range. Hence its name—the Minute Chimer!

CIRCUIT DESCRIPTION

The circuit is more easily understood at a block diagram level. (Fig. 1). The minutes counter consists of a 1Hz oscillator, the output of which is divided by sixty and fed to counter (A). To chime the minutes, a second counter, counter (B), is allowed to count up to the value of the first counter. The pulses to the input of the second counter (B) are used to gate a tone oscillator. The comparator detects when the two counters are equal and prevents (with the help of various gates) any further pulses reaching counter (B), which is reset each minute by detecting when the divide-by-sixty is at zero.

Proceeding to name the components, the 1Hz oscillator is provided by the ubiquitous 555 timer i.c. which, for the purposes envisaged, is accurate enough. The divide-by-sixty is performed by a 7490 decade counter and a 7492 divide-by twelve wired for divide by six. Counters (A) and (B) are 7493 4-bit binary counters. To compare the two counters, a 7486 quad EXCLUSIVE-OR gate is used. The EXCLUSIVE-OR gate is ideally suited to comparing the two counters, its truth-table is shown in Table 1. A 7402 quad NOR gate detects when all the outputs of the EXCLUSIVE-OR gate are zero (indicating that the two counters have reached parity) and prevents further pulses entering counter (B) by disabling the pulse-controlling AND gate.

Another 7402 quad NOR gate and 7408 quad AND gate sense when the divide-by-sixty is at zero, and rest counter (B).

The tone oscillator is another 555 integrated circuit which uses a diode gate to control the oscillations. The diode acts as follows: when the cathode is grounded, the diode is forward biased and hence conducts, preventing the 555's timing capacitor from charging above 600 mV—hence preventing the timing cycle and therefore muting the oscillator. However, when the anode is reverse-biased, no current flows through the diode and the timing cycle is unaffected. The diode is reverse-biased only when counter (B) is receiving pulses and its reset line is at zero volts.

The 10K resistor and 100n capacitor on the reset line to counter (B) are to prevent a glitch caused by IC8 resetting itself slightly before IC9.

CONSTRUCTION

Construction of the unit is best carried out using the printed circuit board layout shown in Fig. 5. The board is single sided and measures 110 × 105mm. It is better to use holders for the integrated circuits, but, if they are to be mounted directly on the board, it is essential to clean the printed circuit board pads just prior to soldering to assure that the solder flows evenly and quickly, giving the iron minimal time to heat the integrated circuit. An excellent and convenient cleaner is the abrasive pencil rubbers used by secretaries to correct errors (mainly before the era of liquid

Table 1. EXCLUSIVE OR truth table		
INPUTS		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	0
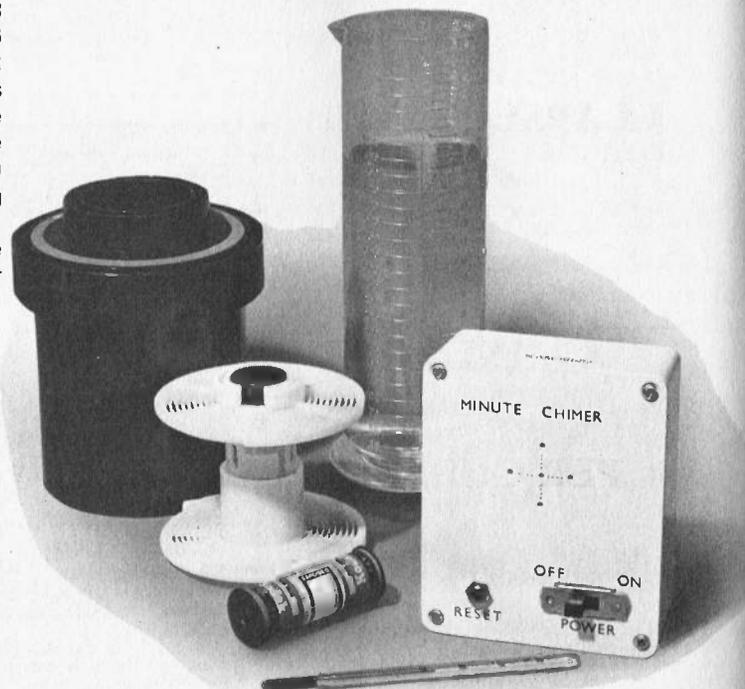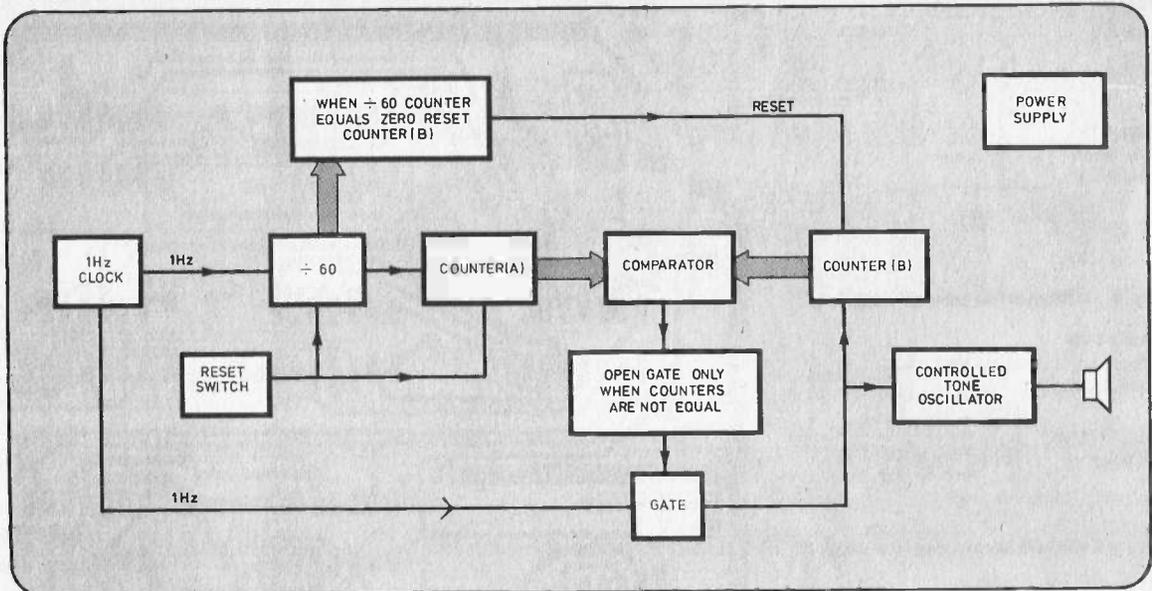
Fig. 1. Block Diagram
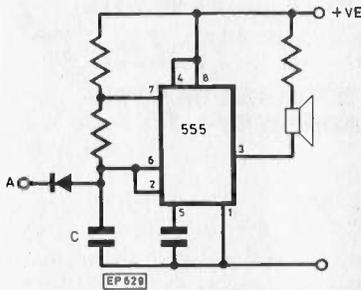
Fig. 2. The gated 555 oscillator. When A is at +5V the circuit will oscillate, but when A is at 0V the capacitor C cannot charge, so that the circuit output stays high

Fig. 3. Minute Chimer circuit diagram

ELAPSED TIME

WITH

A MINUTE

PER CHIME
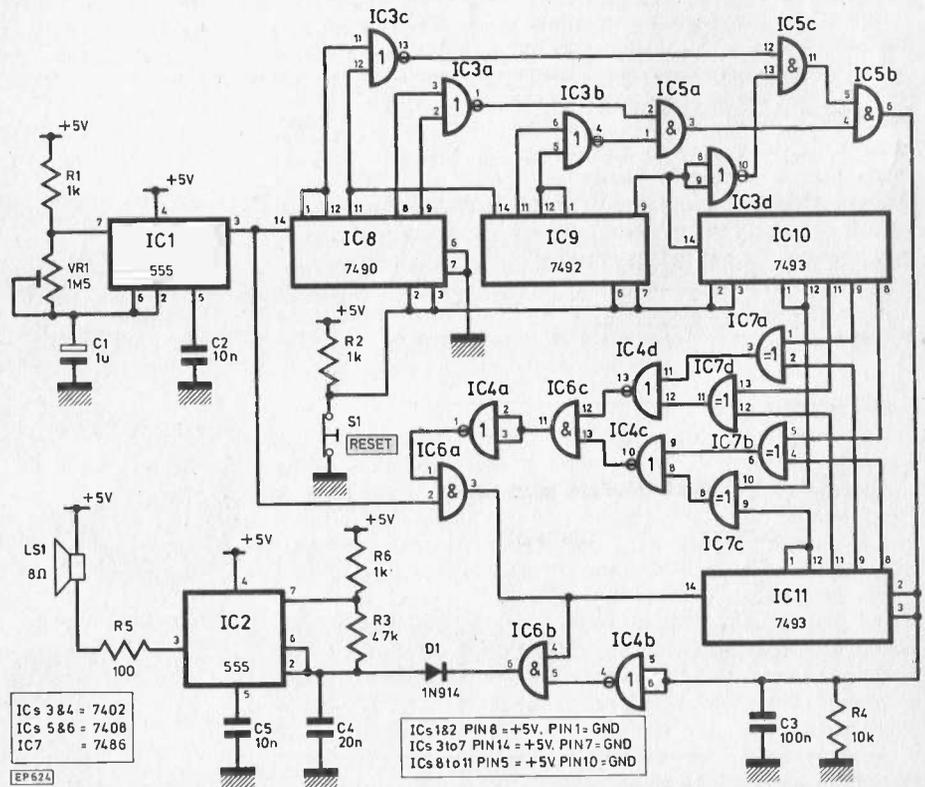
ICs 3 & 4 = 7402
ICs 5 & 6 = 7408
IC7 = 7486

ICs 1 & 2 PIN 8 = +5V, PIN 1 = GND
ICs 3 to 7 PIN 14 = +5V, PIN 7 = GND
ICs 8 to 11 PIN 5 = +5V PIN 10 = GND
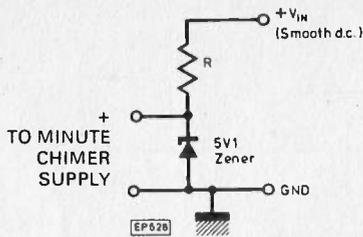
Fig. 4. Alternative power supply

Resistor value in Ohms =	$5 \times (Vin - 5)$
Power dissipation in R =	$(Vin - 5) \div 5$
Max power dissipation in Zener =	$(5 \times (Vin - 5)) \div R$

Fig. 5. Printed circuit layout (actual size)
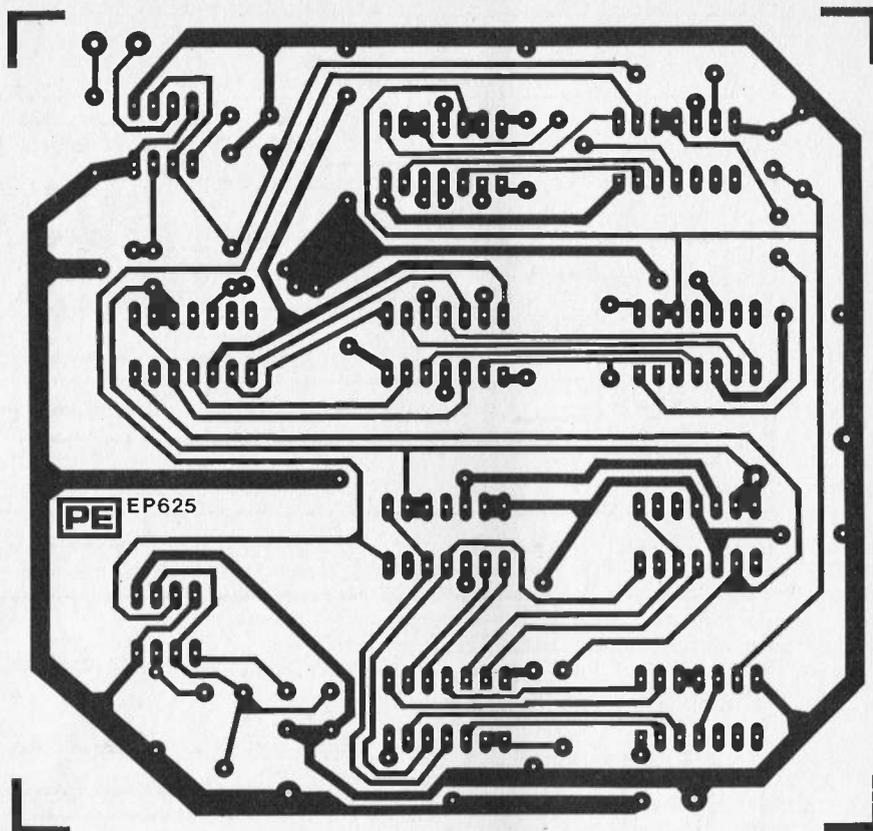
covering fluids!). With TTL circuits, there are no static precautions due to the low input impedance of the gates.

The power supply must be 5 volts (±250mV), with current capability of 150mA. The prototype used 4 AA size nickel-cadmium cells which gave the necessary voltage. If a 6 volt supply is used, inserting a IN4001 diode in the positive power line will reduce the voltage to around 5 volts. Alternatively an arrangement shown in Fig. 6 may be used.

The power requirement could be cut considerably by using pin-compatible low power TTL, although this is more expensive.

Physical construction is not important. It should be noted, however, that photographic chemicals are hostile to metals and the unit should therefore be housed in a plastic box. Small holes need to be drilled for the on/off switch, the reset button, and the loudspeaker part.

APPLICATIONS

The most obvious application for the device is photographic time keeping. Film developing takes many minutes and the unit provides a check on how time is progressing. Since the chimer will not switch off after a preset time, it enables the photographer to change development times at whim. Photographically it is ideal, providing a digital time output with no light emission.

As anyone with a family knows, no two people like their boiled eggs the same—some like them soft, others hard. The minute chimer also provided a useful indication of egg *hardness* giving each member of the family the possibility of a perfectly done egg, (for the first time perhaps?). Placed near the telephone, it will also provide a subtle reminder of how time is passing on those trunk calls!

Last, but certainly not least, the intrinsic displayless nature of the device makes it ideal for partially sighted, or blind persons who require a short interval timer. The two controls are easily understood and facility of use follows. Needless to say, as with any electronic device, the number of applications is only limited by the imagination of the user.

★

+5V

0V
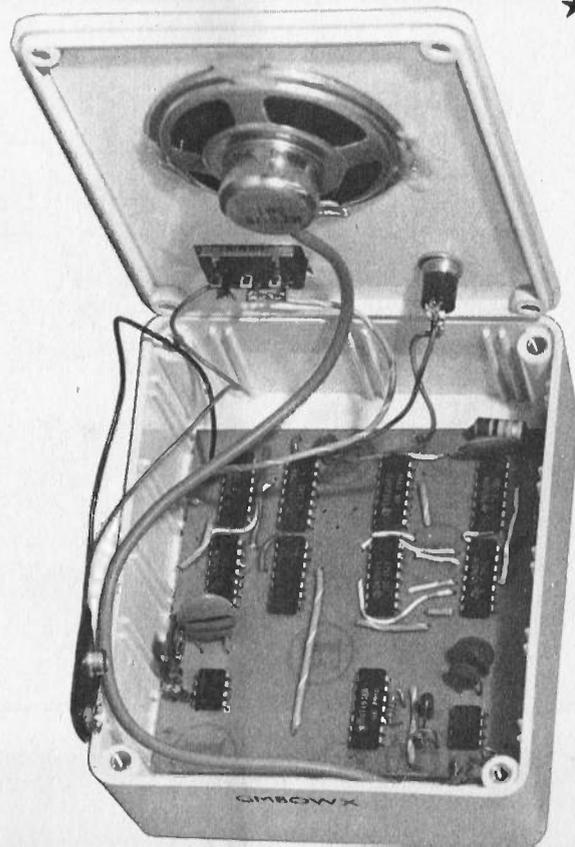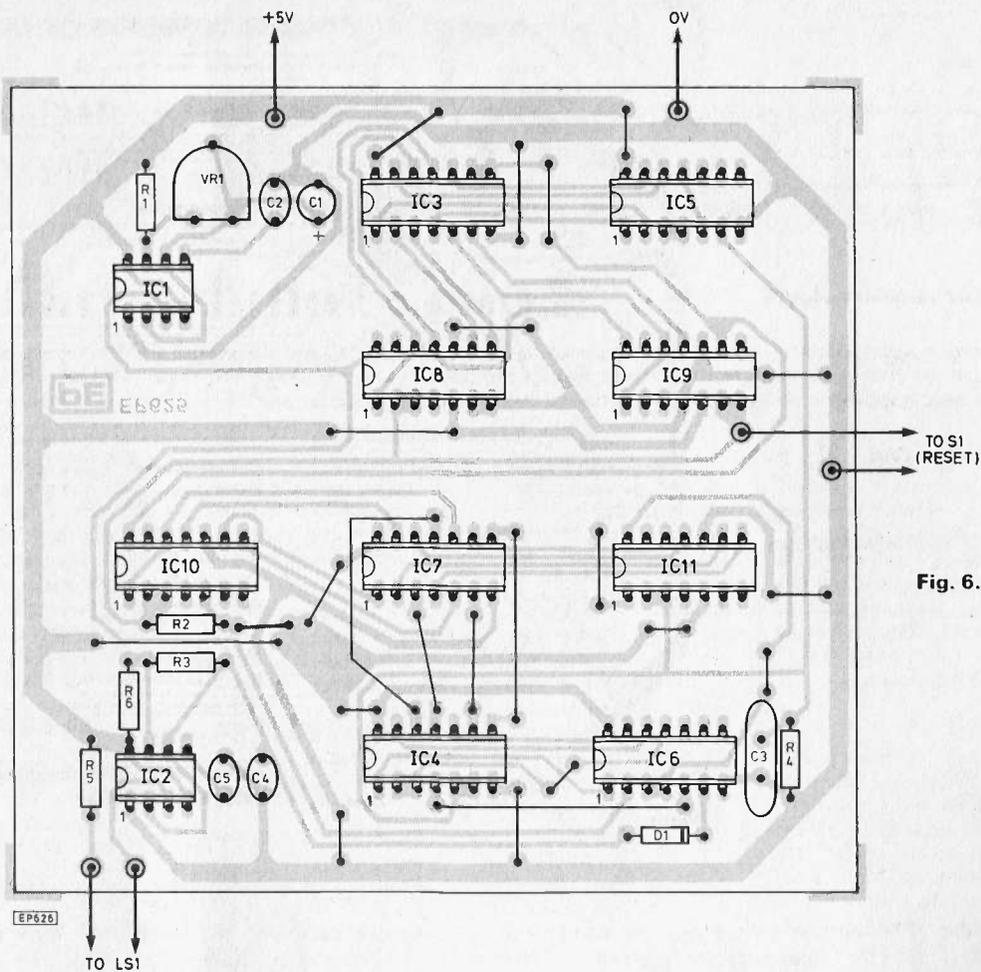
Fig. 6. Component layout

TO S1
(RESET)

EP626

TO LS1

COMPONENTS . . .

Resistors

R1, R2, R6	1k (3 off)
R3	47k
R4	10k
R5	100

All resistors ¼W 5% Carbon

Preset
VR1	1M5 miniature preset

Capacitors

C1	1µ	Tantalum 10 Volt
C2, C5	10n	Ceramic Disc (2 off)
C3	100n	Ceramic Disc
C4	20n	Ceramic Disc

Semiconductors

D1	IN914	Silicon Diode
IC1, IC2	555	timer (2 off)
IC3, IC4	7402	quad TTL NOR gate (2 off)
IC5, IC6	7408	quad TTL AND gate (2 off)
IC7	7486	quad TTL EXCLUSIVE-OR gate
IC8	7490	TTL b.c.d. decade counter
IC9	7492	TTL b.c.d. divide-by-twelve
IC10, IC11	7493	TTL 4-bit binary counter (2 off)

Miscellaneous

S1	Push to break switch
S2	On/Off Slide switch

Loudspeaker 8Ω 200mW 2 in. diameter
Suitable power supply.

MICRO-BUS

Compiled by DJD.

Appearing every two months, Micro-Bus presents ideas, applications, and programs for the most popular microprocessors; ones that you are unlikely to find in the manufacturers' data. The most original ideas often come from readers working on their own systems; payment will be made for any contribution featured.

THE following circuit will provide a microcomputer with the date, day, and time of day to the nearest tenth of a second, and will continue to keep accurate time even when the computer is switched off. Applications might include heading listings with the time and date they were printed, and recording information about when programs such as business packages were run. The circuit could also form the basis for a sophisticated desk diary and alarm clock using a micro.

CIRCUIT DESCRIPTION

The clock/calendar circuit is shown in Fig. 1. It uses the MM58174 clock/calendar chip which is directly interfaced to the microcomputer bus. The time and date information is supplied a digit at a time, and so only the lower four data lines are needed. The chip occupies 16 memory locations, and as shown these are addressed as \$C000 to \$C00F. The prototype was used with a 6800-based microcomputer, and so the NRDS and NWDS signals required by the chip were derived from ϕ_2 and R/$\overline{W}$ using a 74LS139 two-bit decoder; in a Z80 or SC/MP system these signals would be provided directly by the micro. To provide operation even when the main supply is switched off the clock chip is powered from a 3·6V nickel-cadmium battery, which is trickle-charged from the 5V supply at 1mA. In fact the standby current of the clock

is so low (10µA at 2·2V) that a pair of torch batteries would probably be adequate for a year's operation. The backup takes over automatically when power is removed, and the prototype kept perfect time even after being temporarily removed from the computer bus.

MM58174 CLOCK

The MM58174 clock/calendar is a 16-pin CMOS device from National Semiconductor. It divides down a 32768Hz crystal clock to provide BCD outputs which can be read as 4-bit numbers. The different registers are selected by four address lines, AD0 to AD3, and provide the following functions:

Address:	Function:	Mode:
0	Test	Write
1	Tenths of seconds	Read
2	Units of seconds	Read
3	Tens of seconds	Read
4	Units of minutes	Read/Write
5	Tens of minutes	Read/Write
6	Units of hours	Read/Write
7	Tens of hours	Read/Write
8	Units of days	Read/Write
9	Tens of days	Read/Write
10	Day of week	Read/Write
11	Units of months	Read/Write
12	Tens of months	Read/Write
13	Years	Write
14	Stop/Start	Write
15	Interrupt & Status	Read/Write

Registers 1 to 12 give the time and date information, and can be read in any order. The clock includes logic to protect against the data changing while reading the registers, and to appreciate the need for this, imagine reading the time at 11·59. The clock's counters could be updated to 12·00 half-way through reading the four registers, giving the incorrect time of 11·00. To protect against this the clock's outputs are set to the binary pattern '1111' every time the counters are updated; i.e. every tenth of a second. This state is cleared next time the clock is read. Therefore, if while reading the clock's registers a code of '1111' is found, the registers should be read again or an incorrect value may be obtained.

SETTING THE CLOCK

To set the clock it is first stopped by writing '0' into register 14. The time and date can then be set by writing to registers 4 to 13. The day of week counter counts cyclically from 1 to 7, and it is up to you whether you call Sunday 1 or 7. The clock automatically counts the correct number of days in each month, and it is therefore necessary to specify whether it is a leap year, or 1, 2 or 3 years after a leap year; this is done by writing 8, 4, 2 or 1 respectively into the year register, 13. Finally, the clock can be started by writing '1' into register 14.

As well as providing the current time and date, the clock can be used to generate interrupts; these take the open-drain interrupt output low, and on a 6800 system this should be connected to NMI or IRQ. The interrupt is initialised by writing to register 15, and the number determines the period as follows:

Function:	DB2	DB1	DB0
No interrupt	0	0	0
60-sec intervals	1	0	0
5-sec intervals	0	1	0
½-sec intervals	0	0	1

By setting DB3 in register 15 to '1' the interrupts will be continuous; otherwise they will be reset after the selected period. An active interrupt is shown by a '1' on reading DB3 of register 15, and reading this status resets the interrupt.

CLOCK PROGRAM

In use, the clock's registers are simply read by a program to give the current time or date information, and if any register reads as '1111' the registers should be read again to avoid an incorrect value. A program, TIME, to demonstrate the circuit's operation is shown in
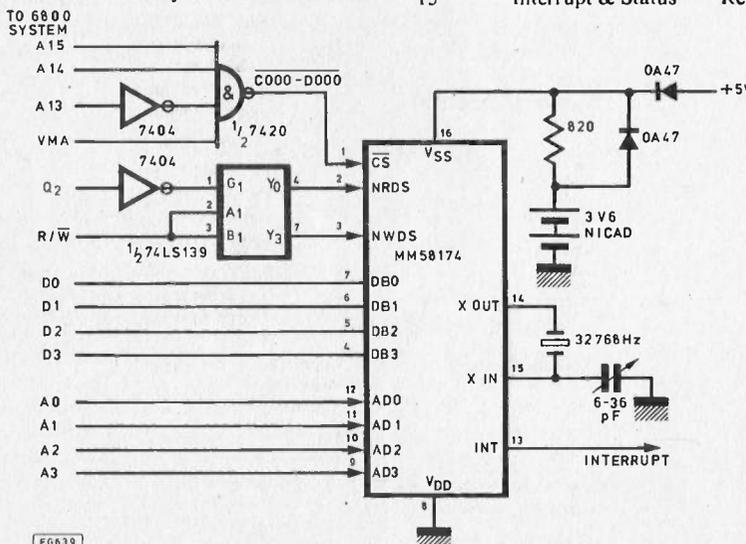
Fig. 1. Clock/calendar circuit interfaces to a microcomputer to give the time and date.

Fig. 2. It writes out the time on a VDU in the form: "THE TIME IS 12 06 49". The program uses two routines in the 6800's MIKBUG monitor: PDATA, which outputs a string of characters terminated by a '4', and OUT2HS which outputs a byte pointed to by the X register as two hex digits, and increments X.

```
                          NAM      TIMER
            C000   TIMER  EQU      $C000
            E07E   PDATA  EQU      $E07E
            E0CA   OUT2HS EQU      $E0CA
                          ORG      0
0000               H      RMB      1        BCD HOURS
0001               M      RMB      1        BCD MINUTES
0002               S      RMB      1        BCD SECONDS
                   *
0003 CE C002 READ  LDX     #TIMER+2
0006 A6 00   NEXT  LDA A   0,X
0008 84 0F         AND A   #$0F
000A 81 0F         CMP A   #$0F            DATA CHANGED?
000C 27 F5         BEQ     READ            START AGAIN
000E C6 04         LDA B   4               COUNTER
0010 44     SHIFT  LSR A
0011 76 0000       ROR     H
0014 76 0001       ROR     M
0017 76 0002       ROR     S
001A 5A            DEC B
001B 26 F3         BNE     SHIFT
001D 08            INX                     NEXT REGISTER
001E 8C C008       CPX     #TIMER+8
0021 26 E3         BNE     NEXT
0023 39            RTS
                   *
0024 BD 0003 TIME  JSR     READ
0027 CE 003A       LDX     #MESSG
002A BD E07E       JSR     PDATA
002D CE 0000       LDX     #H
0030 BD E0CA       JSR     OUT2HS          HOURS
0033 BD E0CA       JSR     OUT2HS          MINUTES
0036 BD E0CA       JSR     OUT2HS          SECONDS
0039 39            RTS
                   *
003A 54     MESSG  FCC     "THE TIME IS "
0046 04            FCB     4
                   END
```

Fig. 2. Program for the 6800 micro reads the clock circuit of Fig. 1 and prints out the time.

The program calls a subroutine, READ, which reads the clock's hours, minutes and seconds registers, and packs the six BCD digits into three bytes, H, M and S. If any register reads as 'OF' the process is repeated.

The subroutine could easily be modified to read date information as well, and the program could print out a message such as: "TODAY IS SUNDAY, THE 20TH APRIL". In fact, with this circuit, there is no reason why your computer shouldn't greet you with "GOOD MORNING", "GOOD AFTERNOON", or "GOOD EVENING" as appropriate!

MK14 VDU

Judging by the number of programs received by Micro-Bus for use with the Mk14 VDU there are many of these circuits still in use, despite the fact that they are sadly no longer available from Science of Cambridge. This month two programs are presented for use with the VDU: a logic monitor, and a horse-race game.

The Mk14 VDU is unusual in that it does not include any memory, but displays the contents of the memory on the Mk14 itself by stopping the SC/MP processor for the duration of each television scan line, and reading from memory by DMA. This slightly slows down the processor, but greatly reduces the cost of the VDU by eliminating the buffers normally needed between the processor and VDU memory. The standard Mk14 includes two pages of memory, addressed as OBOO-OBFF and OFOO-OFFF; these can each be mapped to either the top or the bottom half of the screen and displayed as a rectangle of either 64 (horizontal) by 32 (vertical) graphics cells, or 16×16 characters. Thus the overall

display can be graphics with a resolution of 64×64, or the rather peculiar format of 32 lines of 16 characters; alternatively, the display can be half graphics and half characters.

CLEAR DISPLAY

Either half of the VDU display can be cleared, for characters or graphics, with the short program of Fig. 3. As shown it clears the

```
             ; CLEAR MK14 VDU
             ;
        OBOO VDU     =           OBOO
0000 OF20            .=OF20
OF20 C40B    CLEAR:  LDI    H(VDU)
OF22 36              XPAH   2
OF23 32      LOOP:   XPAL   2
OF24 C420            LDI    X'20
OF26 CE01            ST     @1(2)
OF28 32              XPAL   2
OF29 9CF8            JNZ    LOOP
OF2B 3F              XPPC   3
        0000         .END
```

Fig. 3. Program for the SC/MP micro clears the Mk14 VDU in character mode.

block of memory from OBOO-OBFF for characters by writing spaces, code X'20, in every location. Register P2 is first set to OBOO, relying on the fact that its initial value is zero on reset, and it is then incremented until the low byte is again zero. To clear the other half of the display, OFOO-OFFF, the byte at OF21 should be changed to 'OF', and to clear the display for graphics the byte at OF25 should be '00' instead of '20'. The routine is relocatable, and can be moved to any convenient position in memory.

LOGIC MONITOR

The Logic Monitor program, submitted by *Mark Franklin* of Kent, gives a display on the VDU of the logic levels on the Mk14's two I/O ports. The logic levels are shown as 0's

```
        ; LOGIC MONITOR
        ; FOR MK14 + VDU
   OBOO VDU    =        OBOO
   OE20 RAMIO  =        OE20     ; RAM I/O PORT A
   OF1E XX     =        OF1E     ; COUNTER
   OF1F YY     =        OF1F     ; COUNTER
0000 OF20             .=OF20
   OF20 C402  BEGIN:  LDI    2
   OF22 C8FC          ST     XX
   OF24 C40E          LDI    H(RAMIO)
   OF26 35            XPAH   1
   OF27 C420          LDI    L(RAMIO)
   OF29 31            XPAL   1       ;P1=PORT A
   OF2A C40B          LDI    H(VDU)
   OF2C 36            XPAH   2
   OF2D C408          LDI    8
   OF2F 32            XPAL   2       ;P2=VDU
   OF30 C100          LD     (1)     ;READ PORT A
   OF32 01            XAE            ;PUT IN EXT
   OF33 C408  SETUP:  LDI    8
   OF35 C8E8          ST     YY      ;SET UP YY
   OF37 40    CONVT:  LDE            ;BRING BACK E
   OF38 1F            RRL
   OF39 06            CSA
   OF3A 9402          JP     CLEAR   ;IF NO CARRY
   OF3C 900A          JMP    NOCLR
   OF3E C430  CLEAR:  LDI    X'30    ;DIGIT "O"
   OF40 CEFF  LOAD:   ST     @-1(2)  ;PUT AT VDU
   OF42 B8DB          DLD    YY
   OF44 9C02          JNZ    SHIFT
   OF46 9009          JMP    PORTB   ;PORTA DONE?
   OF48 C431  NOCLR:  LDI    X'31    ;DIGIT "1"
   OF4A 90F4          JMP    LOAD
   OF4C 40    SHIFT:  LDE            ;GET VALUE
   OF4D 1C            SR             ;NEXT BIT
   OF4E 01            XAE            ;PUT BACK
   OF4F 90E6          JMP    CONVT
   OF51 C458  PORTB:  LDI    X'58
   OF53 32            XPAL   2       ;
   OF54 C101          LD     1(1)    ;PORT B VALUE
   OF56 01            XAE
   OF57 B8C7          DLD    XX
   OF59 9CD8          JNZ    SETUP
   OF5B C401          LDI    1       ;XX WAS ZERO
   OF5D CAB2          ST     OB2(2)  ;LABEL PORT A
   OF5F C402          LDI    2
   OF61 CAO2          ST     2(2)    ;LABEL PORT B
   OF63 90BB          JMP    BEGIN   ;CONTINUE...
        0000          .END
```

Fig. 4. Logic-monitor program for the SC/MP micro displays the states of 16 logic levels in DIL format.

and 1's in a 16-pin d.i.l. format, and a changing value is shown as a blurred digit. By wiring the ports to a 16-pin d.i.l. test clip, via a length of ribbon cable, the program can be used to test logic circuits in situ. The inputs will handle normal TTL levels, and since their impedance is about 500 kΩ they present a negligible load to the circuit under test.

The program uses VDU memory from OBOO to OBFF in character mode to display the digits, and this should first be cleared by running the program in Fig. 3. The Logic Monitor program, Fig. 4, should then be executed from BEGIN. It executes the main loop, from CONVT to PORTB, eight times for each port, shifting the bits one at a time into the carry bit and writing a '0' or a '1' to the displays depending on the bit's state. Finally it labels the rows 'A' and 'B' before repeating the process.

HORSE RACE

The following Horse Race program, written by *Mr. W. C. Stanbury* of Cheltenham, displays three horses racing at random across the Mk14 VDU in graphics mode, their legs moving at a gallop; see Fig. 5. When one horse reaches the right-hand end of the screen the race stops, and the program is ready for a new race.
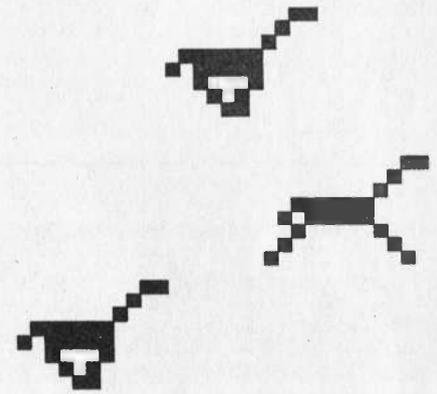
Fig. 5. Display produced by the horse-race program of Fig. 6.

The screen memory, from OFOO to OFFF, should first be cleared for graphics with the routine in Fig. 3, modified as described above. The program should then be executed from START, and the three horses will set off from the left-hand end of the screen.

PROGRAM DESCRIPTION

The program, shown in Fig. 6, is fairly straightforward, and could be translated for use on other micros. One point to note is that the variables are embedded within the program, and at two points (OABA and OAEA) the program modifies the offset of an instruction.

The bit patterns for the two horses, legs apart and legs together, are given at HORSEA and HORSEB. The program chooses alternately between these at GALLOP. Then, to decide which horse to move forward, a number between 0 and 7 is obtained 'at random' by taking a byte from memory, and ANDing it with 7. If the result is equal to 1, 2 or 4, a horse is drawn in the top, middle or bottom

```
                    ; HORSE RACE
      OF00    VDU      .=0A80      OF00     ;DISPLAY MEMORY
0000  0A80             .=0A80
0A80  00      HORSEA:  .BYTE  000,003,000,004,008
0A86  03               .BYTE  000,0F0,000,001,010
0A8C  03               .BYTE  000,0A0,000,060
0A90  03      HORSEB:  .BYTE  003,0F0,005,004,008
0A96  03               .BYTE  003,0F0,005,0F0,002,008
0A9C  04               .BYTE  004,004,008,002
0AA0          COUNT:   .=.+1
0AA1  C404    START:   LDI    4
0AA3  07               CAS                   ;SET GRAPHICS
0AA4  A8FB    GALLOP:  ILD    COUNT
0AA6  D401             ANI    1              ;ODD OR EVEN?
0AA8  9C06             JNZ    ODD
0AAA  C490    EVEN:    LDI    090
0AAC  C83D             ST     FETCH+1        ;MODIFY CODE
0AAE  9004             JMP    RANDOM
0AB0  C480    ODD:     LDI    080            ;HORSE A
0AB2  C837             ST     FETCH+1
0AB4  8FFF    RANDOM:  DLY    0FF            ;FOR DISPLAY
0AB6  A803             ILD    ADDS+1         ;MODIFY BYTE
0AB8  01               XAE
0AB9  C700    ADDS:    LD     @0(3)          ;MODIFIED
0ABC  01               XAE                   ;IN EXT
0ABC  C780             LD     @-128(3)
0ABE  D407             ANI    7              ;GET 0 TO 7
0AC0  01               XAE                   ;SAVE IN EXT
0AC1  C40F    MOVE:    LDI    H(VDU)
0AC3  35               XPAH   1
0AC4  01               XAE
0AC5  FC01             CAI    1              ;IS IT = 1?
0AC7  980B             JZ     ADD1+1
0AC9  FC01             CAI    1              ;IS IT = 2?
0ACB  980D             JZ     ADD2+1
0ACD  FC02             CAI    2              ;IS IT = 4?
0ACF  980F             JZ     ADD4+1
0AD1  90D1             JMP    RANDOM         ;NOT 1, 2, 4
0AD3  007     ADD1:    .BYTE  007            ;START ADDRESS
0AD6  A8FE             ILD    ADD1           ;ADD ONE
0AD6  31               XPAL   1
0AD7  900C             JMP    DISPLY
0AD9  4F      ADD2:    .BYTE  04F            ;START ADDRESS
0ADA  A8FE             ILD    ADD2           ;ADD ONE
0ADC  31               XPAL   1
0ADD  9006             JMP    DISPLY
0ADF  9F      ADD4:    .BYTE  09F            ;START ADDRESS
0AE0  A8FE             ILD    ADD4           ;ADD ONE
0AE2  31               XPAL   1
0AE3  9001             JMP    DISPLY
0AE5  08      COUNTC:  .BYTE  08             ;COUNTER
0AE6  C40A    DISPLY:  LDI    H(HORSEA)
0AE8  36               XPAH   2              ;P2 POINTS TO
0AE9  C490    FETCH:   LDI    L(HORSEB)      ;  BIT
0AEB  32               XPAL   2              ;  PATTERNS.
0AEC  C601    WRITE:   LD     @1(2)
0AEE  CD01             ST     @1(1)
0AF0  C601             LD     @1(2)
0AF2  CD07             ST     @7(1)          ;NEXT ROW...
0AF4  B8F0             DLD    COUNTC         ;HORSE DONE?
0AF6  9CF4             JNZ    WRITE
0AF8  C408             LDI    8              ;RESET COUNTC
0AFA  C8EA             ST     COUNTC

0AFC  C400             LDI    0              ;REMOVE LAST
0AFE  CDFF             ST     @-1(1)         ;  HORSE.
0B00  C400    REMOVE:  LDI    0
0B02  CDF8             ST     @-8(1)
0B04  B8E0             DLD    COUNTC
0B06  9CF8             JNZ    REMOVE
0B08  C408             LDI    8              ;RESET COUNTC
0B0A  C8DA             ST     COUNTC
0B0C  C400    WINNER:  LDI    0              ;A WINNER?
0B0E  31               XPAL   1
0B0F  C10F             LD     00F(1)         ;HORSE 1 WIN?
0B11  9C0D             JNZ    SAVE1
0B13  C157             LD     057(1)         ;HORSE 2 WIN?
0B15  9C0E             JNZ    SAVE2
0B17  C4A0             LDI    0A0            ;SET P2
0B19  31               XPAL   1
0B1A  C107             LD     007(1)         ;HORSE 3 WIN?
0B1C  9C0C             JNZ    SAVE4
0B1E  9084             JMP    GALLOP         ;ELSE LOOP...
0B20  C401    SAVE1:   LDI    1
0B22  01               XAE
0B23  9008             JMP    STOP
0B25  C402    SAVE2:   LDI    2
0B27  01               XAE
0B28  9003             JMP    STOP
0B2A  C403    SAVE4:   LDI    3
0B2C  01               XAE
0B2D  C407    STOP:    LDI    7
0B2F  C8A3             ST     ADD1           ;RESET ADDS.
0B31  C44F             LDI    04F
0B33  C8A5             ST     ADD2
0B35  C49F             LDI    09F
0B37  C8A7             ST     ADD4
0B39  3F               XPPC   3              ;RETURN.
      0000             .END
```

Fig. 6. Horse-race program for the SC/MP micro uses a Mk14 VDU in graphics mode.

row respectively, one place ahead of its previous position. The old version of the horse is then erased, at REMOVE, giving the impression that the horse has moved forward. The horses' positions are stored in the bytes at ADD1, ADD2 and ADD4.

At WINNER the program checks whether a horse has reached the end of the screen, and if not the process is repeated. When one horse has won, its number is put in the extension register, and the horse start addresses are restored at STOP before returning to the monitor. If RESET is pressed during a race the program should be entered at STOP to reset the horse addresses before running it again, or disastrous results may occur.

Since the program stops with the number of the winning horse in the extension register it would be a simple matter to change the display to character mode and display the winner's number, or even keep score over several races.

MORE ON ZX80 CLOCK

The last Micro-Bus presented a digital-clock program for the ZX80 which used a machine-code routine to call the display routine without exiting from the BASIC program. The following modifications, devised by *Mr. Tait* of Dorset, enable the machine-code routine, once entered, to be saved on cassette along with the BASIC program.

The first step is to reserve space for the machine code by entering a REM statement at line 5, followed by 53 characters. It is easiest to type "5 REM 1234567890123 . . ." etc. Then add the following lines to the original program:

```
10 LET K=USR(16427)
80 LET K=USR(16468)
250 FOR A=16427 TO 16479
```

Then proceed as described previously, and the machine-code routine will be stored in the REM statement, its 53 bytes replacing the 53 characters typed in. Note that after entering the machine code line 5 will appear as odd characters on the screen. However, the variables H, M and S can still be set, and the program will run normally.

EPROM Programmer...

J. DYSON

A SIMPLE inexpensive method of programming the single supply 2716 2K EPROM is to be presented. The technique has been developed for the UK 101 using a 6821 PIA and may be used with the PIA on the PE Decoding Module. The necessary additional hardware requirement is such that the component cost amounts to pence rather than pounds and can be easily executed.

Programming the EPROM with code, which is resident in the computer memory, is executed under the control of a BASIC program which is listed in Fig. 3.

The program should translate readily to other machines and the BASIC program is presented in such a way that modification for other interface devices is straightforward.

The single supply voltage 2716 EPROM is relatively easy to program. A single high pulse of 50ms duration is required for each addressed byte when data has been presented to the data pins. A 25V input at 10 to 20mA is required at Vpp (pin 21) throughout programming; this pin is at 5V for read operations.

The programming requirements can be seen clearly from the logic diagram.

For reading, $\overline{CE}$/PGM and $\overline{OE}$ are low and Vpp is at 5V.

Throughout programming $\overline{OE}$ is high and Vpp is 25V; when the appropriate address and data signals have been applied to address and data lines. the data is burned at that address by the application of a 50ms, high pulse at $\overline{CE}$/PGM (pin 18).

Although the programming routine employed here uses a PIA so as to achieve compatability with the PE Decoding Module, other devices such as a 6522 with its own timers, could have been used.

In order that programming can be achieved with a single PIA, the address lines A8, A9 and A10 are controlled by switches on the programmer board. These lines constitute what I have called the EPROM High Byte Address; the required setting for these switches is prompted graphically in the burning program. For example, if an EPROM was being prepared to reside at C800 to CFFF and the contents starting at CBOF, the "High Byte" address associated with A8, A9 and A10 would be 3. This would be prompted by:

"SET HIGH BYTE SWITCHES FOR ROM:

| 0 | 1 | 1 |

HAVE YOU DONE THAT?"

The low byte addressing in blocks of 256 bytes is taken care of by the program, using the PIA.

To burn the full 2K on the 2716, the operating program will require these switches to be set eight times during the course of the program using the PIA.

The circuit requirements are very simple and can be executed on a small piece of strip board; layout and connection means are dependent upon the termination of your PIA output socket. The circuit diagram indicates the connection between PIA and EPROM socket and the additional switches for addressing.

Fig. 1 gives the wiring of the programmer for use with the PIA on the PE Decoding Module.

A Read/Program switch has been provided. This facilitates reading the EPROM through the PIA. In order to avoid the exposure of the EPROM to incorrect $\overline{CE}$/PGM input prior to PIA initialisation, it is recommended that the switch be normally set to READ, changed to PROGRAM when the first high byte setting is called for, and switched back to READ when the routine is complete.

In preparation for programming the EPROM, the code to be entered should be corrected for the intended location of the EPROM within the computer memory map (JMP JSR etc., should be vectored to the addresses where they will be used). To facilitate this, I have fitted address changeover switches to my expansion board so that the addresses decoding of RAM and ROM may be interchanged. By these means the program can be run in RAM at its intended memory location. The Relocate and Move functions in the UK101 extended monitor are very useful in this context.

The corrected code should be resident in the computer memory, in an area which is protected from over-writing by BASIC. The decimal start and end addresses of the temporary location should be calculated, and the high byte and low byte of the EPROM start address should be calculated. The section of EPROM memory which is to be used should be in the erased state (containing 255 or FF). The EPROM may be programmed in blocks of any size, including a single byte.

Running the program without an EPROM (or even without a PIA) will clarify these requirements.

... FOR SINGLE-SUPPLY 2716 EPROMS

Table 1. Logic Diagram for 2716 (5V single supply)				
FUNCTION	$\overline{CE}$/PGM	$\overline{OE}$	Vpp	OUTPUT
PIN MODE	18	20	21	9–11, 13–17
READ	V_{IL}	V_{IL}	5V	OUT
STANDBY	V_{IH}	XX	5V	Hi Z
PROGRAM	Pulse 50ms V_{IH}	V_{IH}	25V	IN
PROGRAM INHIBIT	V_{IL}	V_{IH}	25V	Hi Z
VERIFY	V_{IL}	V_{IL}	25V	OUT
V_{IL} = logic 0	V_{IH} = logic 1		XX = DON'T CARE	
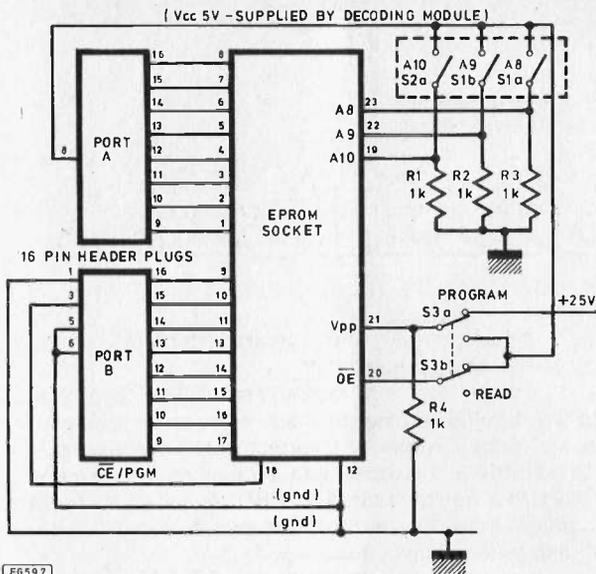
Fig. 1. Wiring arrangement.

The EPROM Data Lines (O0 to O7) are connected to the PIA PORT B (PB0 to PB7).

The EPROM Low Byte Address Lines (A0 to A7) are connected to the PIA PORT A (PA0 to PA7).

The EPROM High Byte Address Lines (A8, A9, A10) are selected, manually, by individual switches.

The EPROM mode is selected by S1:

— for Program : Vpp to 25V and OE to 5V

— for Read : VPP to 5V and OE

The programming pulse to CE/PGM is derived from PIA control Line CB2.

Vpp (Pin 21) requires a 25V (26·5V max.) supply.

COMPONENTS . . .

Resistors
R1–R4 1k (4 off)

Miscellaneous
24-pin socket for EPROM
16-pin headers (2 off)
S1, S2 d.i.l. s.p.s.t. switch, Maplin (2 off)
S3 Subminiature slide switch d.p.d.t.
Ribbon cable
Stripboard
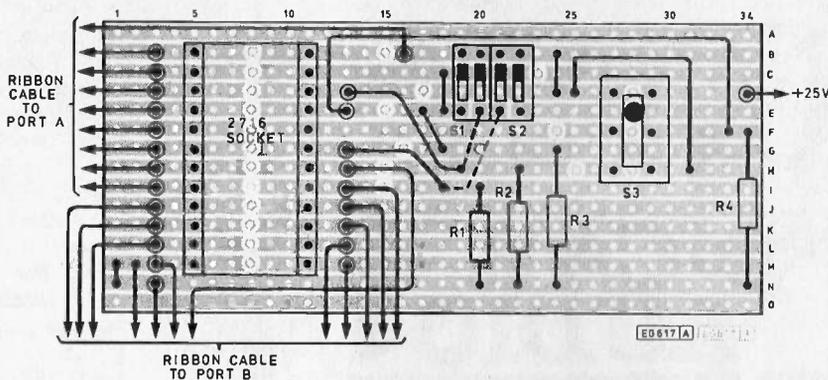
Fig. 2. Stripboard layout

```
10 REM     ROM BURNING ROUTINE
20 REM     IAN DYSON DEC 1980
30 PIA=54368:REM PIA IS MY 6821 BASE ADDRESS
40 POKEPIA+1,0:REM SETS DDR A
50 POKEPIA+3,0:REM SETS DDR B
60 POKEPIA,255:REM SETS PORT A FOR ADDRESS OUTP
70 POKEPIA+2,255:REM SETS PORT B FOR DATA OUTP
75 REM SETTING CONTROL REGISTER BITS 0 TO 7
80 REM CRB 5HI,4HI,3LO (32+16) SETS CB2 LOW
90 REM CRB 5HI,4HI,3HI (32+16+8) SET CB2 HIGH
100 REM CRA/B BIT2 HI SELECTS OUTPUT REGISTERS
110 POKEPIA+1,4
120 POKEPIA+3,52
200 FORZ=1TO5000:NEXT: PRINT CHR$(12):PRINT
201 REM CHR$(12) is revised ROM clear screen
202 REM replace with PRINT loop
210 PRINT:INPUT"ENTER RAM START ADDRESS";RS
220 PRINT
230 INPUT"ENTER RAM END ADDRESS  ";RE:PRINT
240 PRINT"MEMORY REQUIREMENT IS";RE-RS+1;"BYTES"
250 PRINT
260 IF RE-RS+1>2048 THENPRINT"EXCEEDS 2K; START AGAIN":GOTO200
270 PRINT
280 INPUT"ENTER HIGH BYTE FOR ROM START(0 TO 7)";HI
290 PRINT
299 P$="    set mode switch to PROGRAMME"
300 INPUT"ENTER LOW BYTE FOR ROM START (0 TO 255)";LO
310 Q$=STR$(256*(8-HI)-LO)
320 Q$="RESIDUAL MEMORY, "+Q$+" , IS INSUFFICIENT.          START AGAIN"
330 IF RE-RS+1>256*(8-HI)-LO THEN PRINT:PRINT   :PRINTQ$:GOTO200
340 P$="    set mode switch to PROGRAMME"
350 GOSUB 1000
400 REM  BURNING ROUTINE
410 REM RA=RAM ADDRESS:HI=HIGH BYTE IN ROM
420 REM X=DATA       LO=LOW BYTE IN ROM
430 FOR RA=RS TO RE
440 X=PEEK(RA)
450 POKE PIA,LO:POKE PIA+2,X
460 POKEPIA+3,60
470 FORZZ=0TO50:NEXT:REM ENABLE DELAY
480 POKEPIA+3,52
490 LO=LO+1
500 IFLO=256THEN LO=0:HI=HI+1:GOSUB1000
510 NEXT RA
520 PRINT CHR$(12):PRINT:PRINT:PRINT"     ROUTINE COMPLETE  "
530 PRINT
540 PRINT"    set mode switch to READ"
550 PRINT:PRINT
560 END
1000 PRINTCHR$(12): REM   HIGH BYTE SUB
1001 REM  CHR$(12) is revised ROM clear screen
1002 REM  replace with PRINT loop
1010 IF RA=RE THEN 1180
1020 PRINT:PRINT"SET HIGH BYTE SWITCHES FOR ROM: ":PRINT:PRINT
1030 PRINTTAB(15);CHR$(204);CHR$(148);CHR$(148);CHR$(148);CHR$(217);
1040 PRINTCHR$(148);CHR$(148);CHR$(148);CHR$(217);
1050 PRINTCHR$(148);CHR$(148);CHR$(148);CHR$(205)
1060 PRINTTAB(15);CHR$(140);:I=HI:II=INT(I/4):PRINTII;CHR$(149);
1070 I=I-II*4:II=INT(I/2):PRINTII;CHR$(149);
1080 I=I-II*2:PRINTI;CHR$(139)
1090 PRINTTAB(15);CHR$(203);CHR$(148);CHR$(148);CHR$(148);CHR$(215);
1100 PRINTCHR$(148);CHR$(148);CHR$(148);CHR$(215);
1110 PRINTCHR$(148);CHR$(148);CHR$(148);CHR$(206)
1120 PRINT:PRINT P$:P$=" "
1130 FORZ=1TO5000:NEXT
1140 PRINT:PRINT
1150 INPUT"HAVE YOU DONE THAT ";Z$
1160 PRINT
1170 IF LEFT$(Z$,1)<>"Y"THENPRINT"YOU MUST ANSWER YES";:GOTO1130
1180 PRINT" ROM IS BEING PROGRAMMED. PLEASE WAIT"
1190 RETURN
```

Fig. 3. ROM burning routine. PIA in line 30 should be changed to 61340 to be compatible with our published Decode Module. Lines 210 and 230 require addresses in decimal.

PROGRAM NOTES

The variable PIA is the base address of the 6821. It should be set to 61340 for use with the PE Decoder Module and should be changed to suit alternative location.

The address decoding for the 6281 should give low to CS2 and high to CSO and CS1 at address "PIA". If system addresses AO and AI are connected to the RSO and RSI pins of the 6821 the following register addresses will apply. This is compatible with normal usage, and follows that used on the Decoding Module.

PIA + 0   PORT A or DDR for Port A
PIA + 1   Control register for Port A
PIA + 2   PORT B or DDR for Port B
PIA + 3   Control register for Port B

If bit 2 in a control register is high the Port is addressed; if bit 2 is low then that address is directed to the Data Direction Register when each bit of the port can be set for input or output.

Statements 40 and 50 set the control registers for ports A and B so that addresses PIA and PIA+2 select the respective Data Direction registers. In statements 60 and 70 all bits of the Data Direction Registers are set high, selecting Port A

lines as output for addressing the EPROM, and Port B as output for Data to the EPROM.

In the remainder of the program bit 2 in each of the control registers is set high in order that the Ports are addressed for output to the EPROM at 'PIA' and 'PIA+2' for address and data respectively.

Other bits of control register B have to be set so that the output at CB2 can be set high for the programming pulse.

CRB bit 5 is set high to select CB2 for output
CRB bit 4 is set high then CB2 follows CRB bit 3.

Thus:

CRA bit 2 high   Poke PIA, 4
CRB bits 5, 4 and 2 high,
     3 low   Poke PIA, 52   for CB2 low
CRB bits 5, 4 and 2 high,
     3 high   Poke PIA+2, 60   for CB2 high

In the burning routine, for each address the address and data are output to the EPROM by poking PIA with the address and (PIA + 2) with the data (line 450). The high pulse to $\overline{CE}$/PGM is output from CB2 when bit 3 of CRB is set high (statement 460) for the duration of the delay (statement 470) and returned low (statement 480).

★

SPACEWATCH

FRANK W. HYDE

THE SECOND SHUTTLE FLIGHT

At Kennedy Space Centre the Shuttle project and launch site officials are planning the next mission. The care and dedication that is being applied to these matters must help to ensure a second history-making success. The problems are those of time and technology, and time is all important. It is important because there will be a new crew and sufficient time must be given to the psychological adaption of man and machine. The first mission was an unqualified success and the minds of those who have to make the vital decisions of moment to moment operation are very aware of their responsibilities. Technology in this area of activity has become more and more a partnership of the crew and their environment. It has been noticeable that as some of the new frontiers are explored, more and more attention is being paid to this aspect of the new world of the future. The astronauts have the first rank, but all those engaged in the programme are as much a part of the front line. In the critical days of the Apollo missions, there was the outstanding response during the troubles that befell Apollo 13 which brought every mind to the problems. The whole complex responded. This rapport is surely the heart of the matter and in these days of greater understanding of the reaction between minds focused on a goal, success will have a deeper meaning.

To this end the two astronauts, Colonel J. H. Engle of the United States Air force and Navy Captain Richard H. Truly will be going through their programme of preparation for a target launch date of mid to late October this year. Among the older members of the 'preparation overall' team managers there is a natural reluctance to reduce pre-flight tests and those who lean to the past methods of covering every angle of testing as a priority. This has to be considered well, when the younger and newer men come into the picture. But it is necessary to remember that the purpose of the Shuttle System was to bring the whole programme toward a space-airline operation. The confidence in the system has been boosted because of the outstanding performance of the first flight. No doubt there will be a compromise, but one and all will have full confidence. It is certain that the safety of the crew will be paramount.

Manpower fatigue and morale are very important in such a project as this and if the managers get their schedules in the form they are now aiming, the lift off for the second round could be October 19th 1981. In any case, allowing for the unexpected, the launch will at latest be by early November. Because of the longer period between the first and second tests, certain modifications are being introduced to balance this. It is the plan to reduce turnround time when the second vehicle is ready.

A number of the modifications were already decided before the refurbishing, and not all of them were brought about by the first experience. They are all therefore to be regarded as the natural update of moving technology and experience. During the preparations for the first flight there was some minor trouble with the fuel cells. These are now removed and will udergo modification. A new set will be installed which are the result of improvements not ready at the time of the first flight, though the fuel cells were not a problem of any consequence on the first mission.

There will be new structural changes to bring the design to the condition schedules for the full payload facilities. This was not required for the first flight. The modification is for the full utilisation of the shuttle potential. There will be three cryogenic sets of Oxygen and Hydrogen for the fuel cells, to enable a 7 day mission to be operated and to offer a margin for 5 day flights.

THE SHUTTLE TILES

Any fears that the missing tiles would be a hazard were not as well founded as some believed. There has been an intense and rigorous examination of various areas and the conclusions have resulted in some minor modification. The recordings of the re-entry temperatures were not complete because a recorder part-malfunctioned—possibly due to gravity changes. However, some of the problems have been resolved. Much of the damage is thought to be the result of heating and strain in the ascent phase. In certain areas there could have been higher temperatures than expected. The highest temperatures encountered, according to first figures given, were of the order of 2,400°F. These were later found to be in error, as some of the effects were due to ascent conditions and not all to re-entry. The final temperature for hottest area (based on the conditions observed) was about 2000°F. One area being modified is between the elevons and the fuselage. This was caused by, possibly, the propulsion system or the flow between the elevons and the fuselage during re-entry.

On the whole, the first results appear to be satisfactory. The required modifications will be made prior to the second flight. One of these modifications will be near the nosegear door. There was some surprise at the effect in this part. It is thought that some deflection arrangement will be suitable. There were no dimensional changes not anticipated and it seems that this area of activity will not be a hazard.

THE INFRARED TELESCOPE

The American built space telescope for the observation of all-sky infrared sources is in Holland for installation in a Dutch spacecraft. It is expected to be launched in August 1982. This date is in fact some 18 months later than was expected. The delay has been caused by a number of factors, not least escalating costs. The telescope presented certain problems in payload and cryogenics. There are many problems in working in the infrared part of the spectrum. To operate for long periods in the longwave part of the spectrum requires a large cryogenic installation over a long period. The programmed period is about a year.

Astronomers are of the opinion that as much as half of the energy in the Universe is emitted in the form of infrared energy. Much of this would be during the birth of new stars and at their decline. The new telescope, or to give its complete name, Infrared Astronomical Satellite (IRAS), should be able to detect this energy. The programme will cover the examination of the shroud of interstellar dust that hides the cenre of our own galaxy and also the Seyfert and Markarian galaxies. There is also the possibility of the discovery of large planets not visible because observations by earth based instruments are not able to detect them. Very little infrared energy reaches the earth and only then below wavelengths of 20 micrometres.

Work has been done by high aircraft, rockets and balloons but this is limited by time. So far some 2000 sources have been identified. The new telescope will improve this by many times. Its sensitivity is high when it is considered that an ordinary telescope standing on a table in a room, would be a source of infrared of ten million times greater than any observed 'bright' infrared source. This is the reason for the cryogenic system to be kept at 3°Kelvin, a little above absolute zero. Superfluid helium will be used. This has not been attempted before in space. It will be carried in a Dewar flask at 1·6 to 1·8Kelvin. The telescope will carry 74Kg of superfluid helium and 6Kg of supercritical helium. This will last for about 10 months. The telescope itself will have a useful life of 12 months. During that time it is expected that the IRAS will survey 10,000 sources a day and that over the period of its life it will have 'looked at' more than a million sources.

NEPTUNE'S THIRD MOON?

It is reported from the University of Arizona that two astronomers, working from two observatories in the Santa Catalina Mountains, have discovered what is thought to be a third satellite of Neptune. The astronomers were engaged in the observation of an occultation by Neptune of a star when they made their discovery. According to William Hubbard of the University of Arizona the body is some 160km in diameter. If the discovery is confirmed by independent observers the new moon will join Triton (thought to be the largest satellite in the solar system) 3700km dia. and Neried 480km dia.

INGENUITY UNLIMITED

A	B	V_OUT
0	0	0
1	0	V+
0	1	V−
1	1	Undef.

EP 535

MOTOR CONTROLLER

ONE of the problems in electronics is the inexpensive and reliable switching of analog voltages with digital signals. The described circuit has been designed as part of a control unit for a scientific instrument, to switch a d.c. motor between forward, backward and off, using only cheap components and no mechanics at all. It needs a split power supply, which powers the motor and the logic circuitry. Some of the components are connected to the stabilised voltages (+ and −), others to the unstabilised voltages (++ and −−) to limit noise and power consumption in the regulated section.

IC3 together with TR1 and TR2 forms a current booster amplifier. When input A and B are low, D5 and D6 are reverse biased, R5 pulls the input to IC3 to ground. If either input A or B high, then D5 or D6 is forward biased and the input voltage is V+ or V−, any voltage drop is eliminated by the very high open loop gain (except the input offset voltage of the 741s). D1 and D4 limit the input voltage of the gates to a safe value.

The same principle may be used to switch more than two voltages of either sign, by using more input stages, thus in the present case providing different digitally selectable speeds in both directions.

O. Albrecht,
London.

Rate	Distance	Time for 10p(ab) Time for 5p (L) in seconds	Required value R_t
Cheap	L	540	4M7
	a	288	2M7
	b	96	820k
Standard	L	180	1M5
	a	90	820k
	b	30	270k
Peak	L	120	1M
	a	60	560k
	b	20	180k

L = Local. a = Up to 56km. b = Over 56km
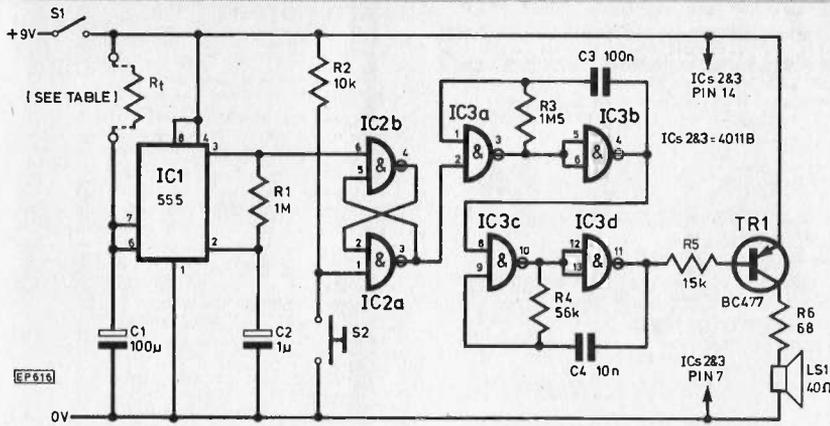
TELEPHONE TIMER

A SIMPLE telephone timer was required to give some indication of the cost of individual telephone calls. This circuit provides a timer which is manually started when the call is first connected and then gives audible indication thereafter on the consumption of one unit. (One unit = 5p for local calls or 10p for middle and long distance calls.)

IC1 is connected in its normal monostable configuration. On switch on its output (pin 3) is low, thus C2 is discharged and the trigger (pin 2) is also low. Hence IC1 immediately commences its monostable cycle with its output being high until C1 is charged to $\frac{1}{3}$ supply voltage via the selected resistor (R_t). R1 and C2 have a time constant much smaller than the monostable period, thus by the end of the monostable period C2 is fully charged (from the output via R2) and the trigger is effectively held high. At the end

of the monostable period C1 is rapidly discharged into pin 7 of IC1, the output falls, and C2 now begins to discharge into the output through R1, thus the trigger is momentarily held high before it falls below $\frac{1}{3}$ supply voltage at which point IC1 is retriggered and the cycle starts again.

This cycle produces one short (1·0s) negative pulse at the output at the end of each monostable period. This pulse is used to set the NAND bistable (IC2a+IC2b) which in turn gates the pulsed tone generator (IC3a–d). The tone generator drives a small loudspeaker via TR1 and gives audible indication that one unit has been used. The tone generator is silenced by resetting the bistable with S2. Since the output of IC1 is initially low on switch on then the tone generator will be triggered and it will be necessary to cancel it by depressing S2. The tone generator consists of two NAND astables, the first

(IC3a+IC3b) is gated by the bistable and runs at about 10Hz. This then gates the second astable (IC3c+IC3d) which runs at about 1kHz. In this way a 1kHz tone pulsed at 10Hz is produced.

R_t is chosen to give the required time period (see Table 1) and is selected using S3 and S4 as shown.

Alternatively, if unit costs of 5p and 10p are not convenient then new values of R_t may be calculated using the following formula.

$$R_t = \frac{t}{1.1C1}$$

Where t = Time period in seconds.
C1 = Value of C1 in Farads.
R_t = Value of R_t in Ohms.

C. Dakin,
Edgbaston,
Birmingham.

A CONVERSATION AID

HAVING a relative who is hard of hearing I designed this low cost amplifier for use with a high impedance crystal microphone and a pair of 8 ohm stereo phones wired in series. TR1–TR2 make up a preamplifier feeding a 741 in the role of a voltage follower with 100% negative feedback to minimise hum and noise. The volume control VR1 was added at the request of my relative who was very complimentary of the end product.

R. A. Maidment,
Bristol.
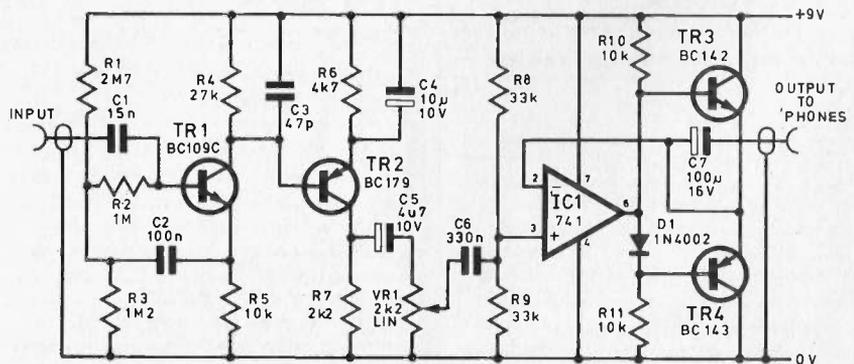
PATENTS REVIEW...

MOTIONAL FEEDBACK

Several electronics companies, notably Philips, have developed and sold motional feedback loudspeakers. In an MFB system, the amplifier is built into the speaker cabinet and a pickup transducer, mounted alongside the loudspeaker transducer, produces a signal which provides a constant tell-tale of the reproduced sound. This signal is compared with the amplifier input signal, and any errors corrected by feedback control. The pickup transducer can be a piezo crystal microphone or (as recently proposed in a Philips patent) it can be replaced by an opto-electronic motion sensor.

So far Bang and Olufsen, of Denmark, has not marketed a motional feedback loudspeaker (or at least marketed one in the UK with any commercial vigour) so it is a surprise to see British patent 1 582 634, from inventor Knud Bakgaard of B and O. According to Bakgaard the conventional MFB approach falls down because the feedback control signal is useful only in the frequency range under 100Hz. This is because the loudspeaker membrane does

Fig. 1

not oscillate as a rigid unit or piston at higher frequencies, and the pickup transducer will produce mis-correction signals from anomalous sensing. These will then be active on all the loudspeaker units. It follows that known MFB systems usually use a separate low frequency amplifier mounted alongside the low frequency woofer.

The B and O patent aims to liberate MFB designs from this constraint. Figure 1 shows the basic circuit. Woofer 12 is fitted with a pickup transducer 18 which produces an output signal as a function of the woofer diaphragm acceleration. High and mid frequency speakers 16, 14 have no such extra transducers. The three loudspeaker units are mounted together in a cabinet which is separate from amplifier 6. The amplifier is connected to filter P
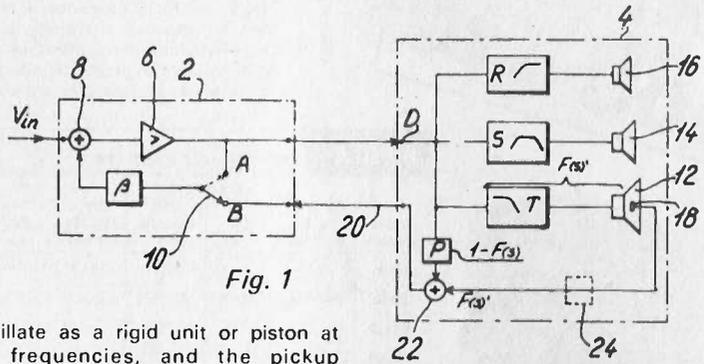
which feeds adder 22. The adder also receives the output from pickup transducer 18, and the output of adder 22 is switchable, at 10, to feedback adder 8.

The filter P replicates the crossover filter and internal characteristic of the woofer, so that the feedback signal will be constant when the actual transfer function of the woofer corresponds to the ideal transfer function. Any divergence from this ideal will produce a control signal on the amplifier tailored to re-establish an ideal transfer function. Inevitably of course, the system suffers from the inherent disadvantage of all feedback systems; errors can only be corrected *after* they have occurred and been detected.

INDOOR AERIAL

British patent application 2 029 112, from Alexander Murphy of Dumbartonshire, describes a flat foil aerial which the inventor has been advertising in this magazine. The aim is to provide a compact and cheap indoor TV aerial formed from metal foil stuck to a supporting surface of cardboard or similar material.

Figure 1 shows one such aerial. Half-wave dipole 1 is formed from two similar strips of metal foil 1a, 1b, 3cm wide and spaced apart by a 0·5cm gap. The overall length is one half the wavelength of the local UHF tv frequency band. Another strip of foil, 1·2cm wide and with length equal to 0·595 of the wavelength, is arranged 0·23 of the wavelength away from the dipole to serve as a parasitic reflector.

To unbalance the system, the dipole can be angled, by between 5° and 10°, with respect to an offset strip which serves as a director (Figure 2).

The inventor claims success with foil, such as aluminium, because at UHF frequencies the signal waves travel on the
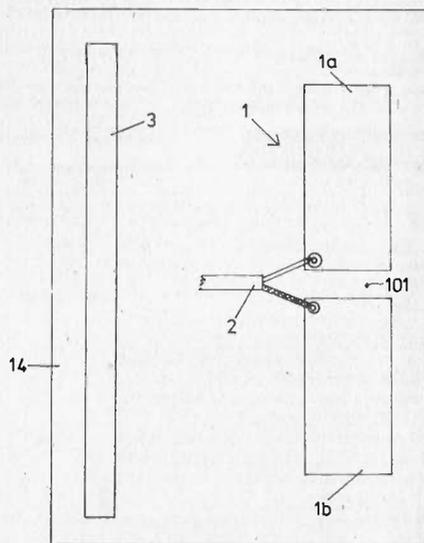

Fig. 1

Fig. 2

strip surface due to "skin" effect. Because the backing sheet is of flexible cardboard or
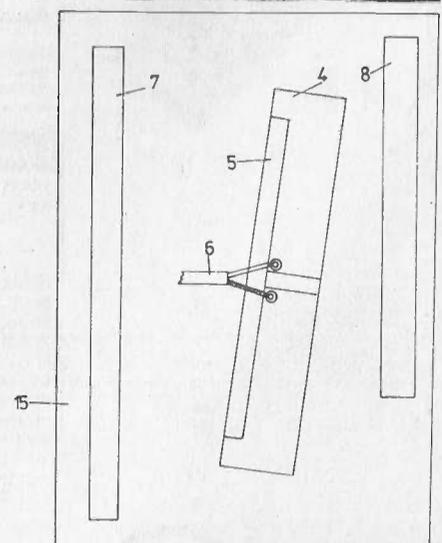
plastic, the aerial can be bent to fit inside a container such as a lamp stand.