Electronic Circuit Design

No. 2

€1.25

Selected Reprints from electronics today INTERNATIONAL

SPECIALS

TOP PROJECTS
Book 1+2: £2.50 + 25p P&P
Master mixer, 100W guitar amp., low power laser, printmeter, transistor tester, mixer preamp., logic probe, Ni-Cad charger, loudhailer, 'scope calibrator, electronic ignition, car theft alarm, turn indicator canceller, brake light warning. LM3800 circuits, temperature alarm, aerial matcher, UHF-TV preamp., metal locator, four input mixer, IC power supply, rumble filter, IC tester, ignition timing light, 50W stereo amp, and many more.

Book 5: £1.00 + 25p P&P
5W stereo amp., stage mixer, disco mixer, touch organ, audio limiter, infra-red intruder alarm, model train controller, reaction tester, headphone radio, STD timer, double dice . . .

Book 6: £1.00 + 25p P&P.
Graphic equaliser, 50/100W amp, modules, active crossover, flash trigger, "Star and Dot" game, burglar alarm, pink noise generator, sweep oscillator, marker generator, audio-visual metronome. LED dice, skeet game, lie detector, disco light show . . .

ETI CIRCUITS Books 1 & 2
Each volume contains over 150 circuits, mainly drawn from the best of our Tech-Tips. The circuits are indexed for rapid selection and an additional section is included which gives transistor specs, and plenty of other useful data. Sales of this publication have been phenomenal — hardly surprising when the circuits cost under 1p each!
£1.50 + 25p P&P.

TOP PROJECTS
Book 7: £1.25 + 25p P&P
ER II loudspeaker, CCD phaser, 3-channel tone control, bass enhancer, continuity tester, bench supply, LCD digital multimeter, digital frequency meter, wide range oscillator, ETI wet, egg timer, house alarm, porch light, torch finder, light dimmer, IB metal locater, electronic bongos, puzzle of the drunken sailor, race track, ultrasonic switch, tic-tac radio, rev counter, Transcendent 2000, spirit level.

ELECTRONICS — ITS EASY
Combined volume.
This, our latest work, is a complete collection of our ever popular beginners series. Previously published in three volumes.
£3.60 + 50p P&P.

ELECTRONICS TOMORROW
Comprised entirely of new material, the edition covers such diverse topics as Star Wars and Hi-Fi! The magazine contains projects for everyone — none of which have appeared in ETI — and a look at the future of MPUs, audio, calculators and video. How can you not read it?
75p + 25p P&P.

ORDER FROM
Specials Modmags Ltd, 145 Charing Cross Road, London WC2H 0EE
Postage and packing also refers to overseas. Send remittance in Sterling only. Please mark the back of your cheque or PO with your name and address.

FROM ETI

Electronic Circuit Design

Selected Reprints from electronics today INTERNATIONAL

No. 2

WINTER 1980

Introduction

This special publication from ETI magazine is the second in a series of three; the first was published in late autumn 1979.

The series comprises the best 250-300 pages selected from well in excess of 1500 published in ETI on aspects of circuit design during its history.

The articles included in this series are intended to give the reader an insight into how circuits work, how they are designed and to provide some fairly conventional 'building blocks'.

Keeping track of current design techniques is not easy due to the rapid introduction of new devices and new technologies: we hope this publication helps to cover the problem.

Halvor Moorshead
Editorial Director — ETI

Contents

Edited by: Halvor Moorshead, Peter Green
Production: Diego Rincón, Dee Camilleri
Thanks to: ETI-Canada (for cover design)

Electronic Circuit Design No 2 is an Electronics Today International Special
Published by: Modmags Ltd, 145 Charing Cross Road, London WC2H 0EE
Distribution by: Argus Distribution Ltd
Printed by: QB Limited, Colchester

OP AMPS

Open up any data sheet on a particular op-amp and you will be confronted with as many as forty different electrical parameters and performance graphs which should reveal all that you need to know about the device. Most of these parameters will be qualified by the conditions under which they were measured and the test arrangements used to make the measurements. This apparent 'overkill' of data is likely to be very confusing to the newcomer, however it need not be so. Tim Orr explains.

Let's discuss some basic principles. An op-amp (or operational amplifier) is just a high gain amplifier, you stick a voltage into it and a much larger voltage comes out of it. Op-amps have two inputs, inverting and non-inverting, which are denoted by — and + respectively. The op-amp amplifies the difference in the voltages applied to these two inputs, the output going positive if the + input is positive with respect to the — input, and vice versa, however this is virtually useless, because the voltage gain is uncontrollably large and the distortion high. The way in which both of these parameters are controlled is by the use of negative feedback. An op-amp with negative feedback is shown in Fig. 1. It employs two resistors to set the closed loop voltage gain, and as long as this is small compared to the open loop gain, it will be determined by the resistor ratio RF/RI. The open loop gain, the voltage gain when RF is removed, is typically of the order of 100 000. This massive gain is clearly much too large to be used without feedback. Closed loop voltage gains of 100 are about as much as it is practical to use.

Biased Example

The arrangement in Fig. 1 is known as a 'virtual earth' amplifier. The non-inverting input is connected to earth, and the inverting input is maintained by the feedback applied via RF at a voltage which is virtually earth potential.

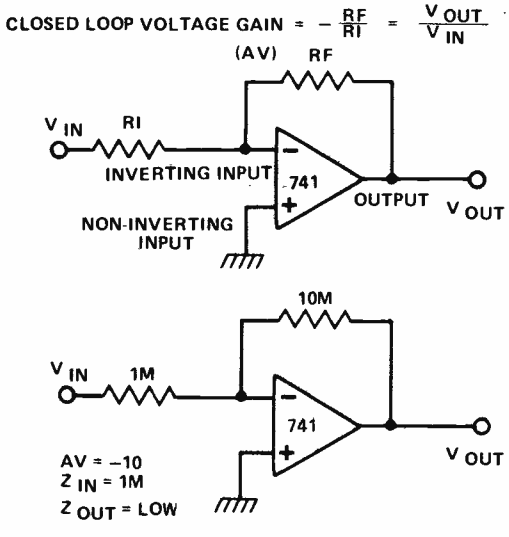
The input impedance of the amplifier in Fig. 1 is simply RI. The output impedance is a little more complicated, it is approximately

$$\frac{\text{output impedence of the op amp} \times \text{closed loop gain}}{\text{Open loop gain}}$$

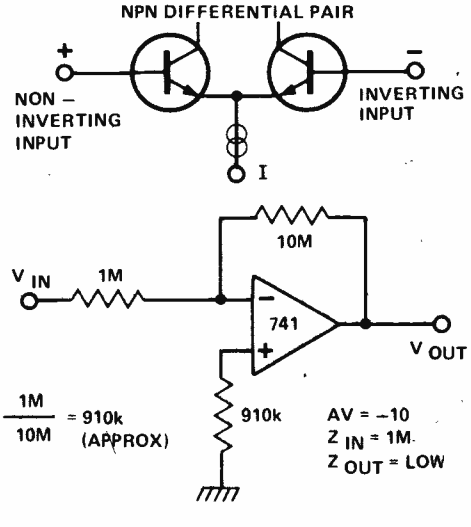
Suppose we want an amplifier with a gain of 10, and an input impedance of 1M. This means that RI is 1M. Therefore RF must be 10M (see Fig. 2). With a 1 V sinewave as the input signal we get a 10V sinewave as the output. However, when the input signal is held at 0V (ground potential), the output voltage is not 0 V, it is positive! This is an error voltage, which may be undesirable. The cause of the problem is the 'INPUT BIAS CURRENT' of the op-amp. The input of many op-amps looks like the circuit shown in Fig. 3. If these transistors are to operate correctly they need a standing emitter current which implies that they need an input base current. It is this base current which is the op-amp's 'INPUT BIAS CURRENT.' For a 741 this current can be as large as .05 uA. In the arrangement of Fig. 2 this current can only come through RF, which means that the output voltage could be as large as 0.5 uA × 10M, which is +5 V! One way to remedy this error is to use a circuit shown in Fig. 4. A resistor has been inserted between the non-inverting input and ground. This resistor has the value of RF in parallel with RI. It allows both the inputs to sink slightly and thus maintain the voltage balance at the inputs. The output voltage is then nearly 0 V. However, the two input transistors may not be that well matched, so the input bias currents may be different into each input. This is known as the 'INPUT OFFSET CURRENT' and its effect can be nulled by making the 910 k resistor in Fig. 4 a variable resistor. If the bias currents (for a 741 say) were zero, then the output voltage would still not be 0 V.

Get Set, They're Off

The output voltage could range between ± 60mV. This is due to the 'INPUT OFFSET VOLTAGE' which for a 741 can be as much as ± 6mV, which is then multiplied by



Figs. 1 and 2 (far left) show (upper) the basic inverting op-amp stage. Gain is given by the ratio of resistors RF/RI, input impedance is simply RI while the output impedance is more complicated (see text). Fig. 2 (lower) shows a stage with a gain of 10 and an input impedance of 1M.



Figs. 3 and 4 (left), show (upper) a typical op-amp input stage. This is a differential amplifier made up of a pair of NPN transistors driven by a constant current source. Fig. 4 (lower left) shows a 910k resistor in the + input of the op-amp. This reduces the effects of the INPUT OFFSET CURRENT.

the closed loop voltage gain of the stage (in this case 10) giving us ± 60mV. This can be compensated by using the circuit shown in Fig. 5. Terminals 1 and 5 on a 741 can be used to compensate for the input offset voltage. The input offset voltage is the V_{be} imbalance between the two input transistors.

Now that we know how to eliminate the spurious DC offsets, we can try designing some dynamic circuits and find out why they don't work as expected! For example, try putting a 1 V sinewave at 200 kHz into a circuit of Fig. 5. What you would expect is a 10 V, 200 kHz sinewave at the output — but you don't get one. What appears is a rather bent 200 kHz triangle waveform. This is because the 'slew rate' of the op-amp has been exceeded. The slew rate is the speed at which the output voltage can move, and for a 741 is typically 0.5V/μsec when it crosses zero, so the op amp faced with this demand just gives up and SLEW limits, drawing out straight lines as it does so.

Listen To The Band(width)

Another problem is 'BANDWIDTH.' A 741 has a GAIN BANDWIDTH product of approximately 1 MHz. This means that the product of the voltage gain times the operating frequency cannot exceed 1 MHz.

For example, if you want the amplifier to have a gain of 100, then the maximum frequency at which this gain can be obtained is 10 kHz. Fig. 6 illustrates this phenomenon. Curve A is the open loop response, note that the voltage gain is 1 at 1 MHz, hence the gain bandwidth product of 1 MHz. The slope of the curve is −20 dB/decade, which is caused by a single 30p capacitor inside the IC. Now, if the resistor ratio is set to give a voltage gain of 100, then the op-amp gives a frequency response shown by curve C, which is flat up until 10 kHz. A gain of 10 rolls off at 100kHz (D) and a gain of 1000 rolls off at 1kHz (B). Thus it is very easy to see just what the closed loop frequency response will be. However, don't forget the slew rate problem. You may be able to construct an amplifier with a voltage gain of 10, which works up to 100 kHz, but the output voltage will be limited to less than 3 V pp! Another problem is distortion in the op-amp. Negative feedback is used to iron out any distortion generated by the op-amp, but negative feedback relies on there being some spare voltage gain available. For instance, say the op-amp generates 10% distortion and there is a surplus voltage gain of 1 000.

$$\text{i.e.}\left(\frac{\text{open loop gain}}{\text{closed loop gain}}\right),$$

then the distortion will be reduced to approximately,

$$\frac{\text{open loop distortion}}{\text{surplus voltage gain}} = \frac{10\%}{1\,000} = 0.01\%$$

So, negative feedback is used to eliminate distortion products. However, if there is no surplus voltage gain, as in the case of a 741 amplifier working at 10 kHz, with a closed loop gain of 100, then the distortion will rise dramatically at this point.

Current Thinking

Most op-amps have a voltage output, although some have a current output. If you short-circuit a voltage output then large currents could flow and thermal destruction might follow. To overcome this problem, most op-amps have a current limited output so that they can suffer an indefinite short to ground. A 741 is limited to about 25 mA. Another current of note is the supply 'BIAS CURRENT. This is the current consumed when the op amp is not driving any load. For a 741 this current is typically 2mA, which makes it rather unsuitable for small battery applications.

There are some op-amps which can be programmed by inserting a current into them so that their supply current can be controlled. This means that they can consume only micropower when in their 'standby' mode, and they can be quickly turned on to perform a particular task.

Voltages Differently

In the few examples shown so far, the op-amp has been used to amplify voltages which have been generated with respect to ground. However, sometimes, it is required to measure the difference between two voltages. In this case you would use a 'Differential' amplifier, Fig. 7. By using two matched pairs of resistors, the formula for the voltage gain is made very simple. It is thus possible to superimpose a 1 V sine wave on both the inputs, and yet have the output of the amplifier ignore this common mode signal and only amplify any differential signals. The amount by which the common mode signal is rejected is called the CMRR (the Common Mode Rejection Ratio) and is typically 90 dB for a 741. Thus a common mode 1V signal would be reduced to 33 uV.

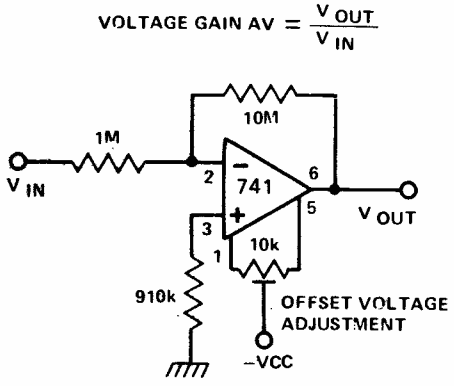


Fig. 5 A variable resistor connected between pins 1 and 5 of a 741 can be used to reduce the effects of the INPUT OFFSET VOLTAGE.

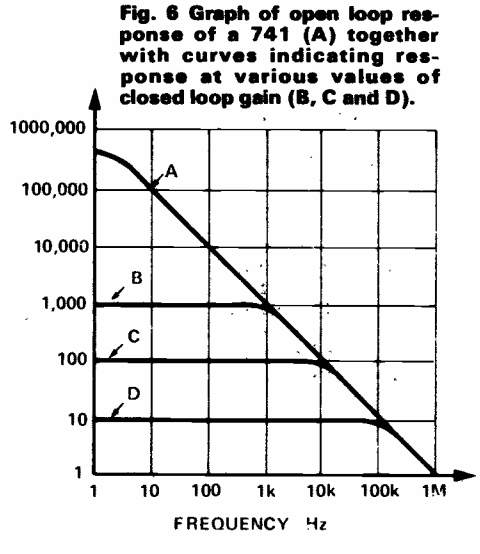


Fig. 6 Graph of open loop response of a 741 (A) together with curves indicating response at various values of closed loop gain (B, C and D).

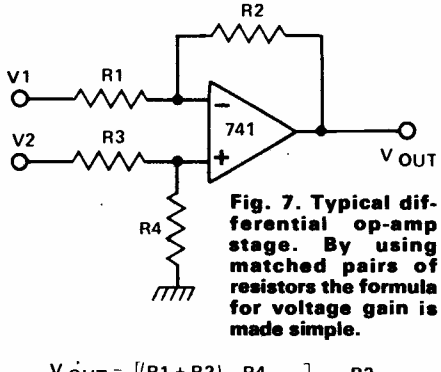


Fig. 7. Typical differential op-amp stage. By using matched pairs of resistors the formula for voltage gain is made simple.

$$V_{OUT} = \left[\left(\frac{R1+R2}{R3+R4}\right)\frac{R4}{R1}V2\right] - \frac{R2}{R1}V1$$

BUT IF WE MAKE R1 = R3
AND R2 = R4
THEN $V_{OUT} = \frac{R2}{R1}(V2 - V1)$

Another rejection parameter to be noted is the supply voltage rejection ratio. For a 741 the typical rejection is 90 dB, that is, if the power supply changes by 1 V the change in voltage at the op-amp output will be 33 uV.

When designing with op-amps it is very important to know what voltage range the inputs will work over, and the maximum voltage excursion you can expect at the output. For instance, the 741 can operate with its inputs a few volts from either power supply rail, and its inputs can withstand a differential voltage of 30V (with a power supply of 36 V).

This is not true of all op-amps, some have a very limited differential input voltage range, for instance the CA3080 will zener when this voltage exceeds 5 V and the amplifier performance will then be drastically changed.

The output excursion of the op-amp is also important. The 741 can only typically swing within about 2 V of either supply rail, whereas the CMOS op-amp can swing to within 10mV of either rail so long as the load into which they are driving is a very high impedance.

NON-INVERTING AMPLIFIER

An op-amp is used to provide voltage gain, but in this case the output is in phase with the input. The minimum gain is unity and occurs when RB is an open circuit. The op-amp has maximum bandwidth at unity gain, and any increase in the gain will cause a reciprocal decrease in bandwidth.

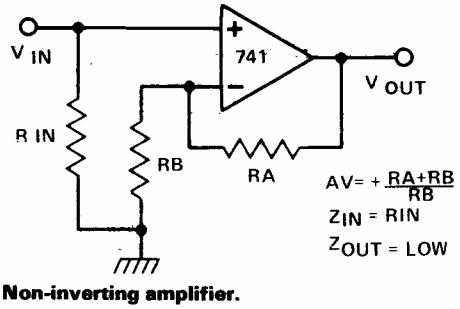


Fig. 8. Non-inverting amplifier.

HIGH SLEW RATE AMPLIFIER

The slew rate of the op-amp has been increased by increasing the overall current generating capability, by the addition of a pair of transistors. These transistors increase the output voltage range by allowing the voltage to swing to within 0V5 of either supply rails. The output of the op-amp hardly moves at all. Without an input signal, the output voltage is 0 V and the op-amp drains approximately 2 mA from the supply rails.

This current passes through the 180R resistors and sets up a voltage which is not quite sufficient to turn on either transistor. When a positive voltage is applied to the input, the op-amp tries to swing negative but it has a 47R (R4) resistor connected from its output to ground.

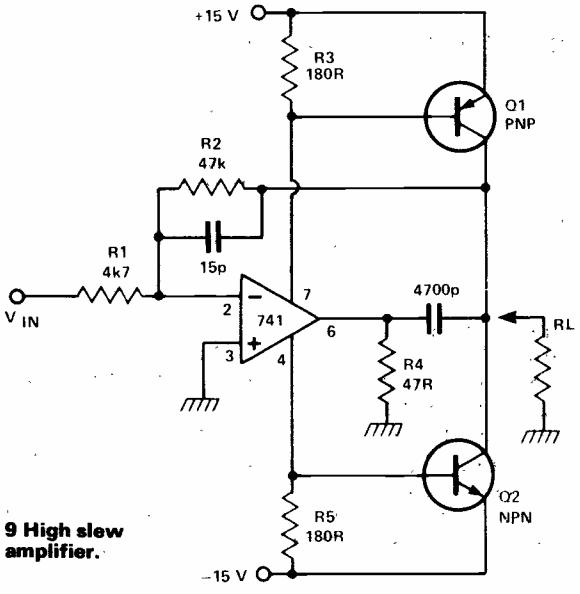


Fig. 9 High slew rate amplifier.

SIMPLE INTEGRATOR

An op-amp and a capacitor can be used to implement to a high degree of accuracy, the mathematical process of integration. In this case, current is summed over a period of time and the resultant voltage generated is the integral of that current as a function of time. What this means that if a constant voltage is imputed to the circuit, a ramp with a constant slope is generated at the output. When the input is positive, the output of the op-amp ramps negative.

In doing so it pulls the inverting terminal negative so as to maintain a 'virtual earth' condition. In fact the input current (Vin/R1) is being equalled by the current flowing through the capacitor, thus equilibrium is maintained. The equation governing the behaviour of a capacitor is $C \times dV/dt = i$, where dV/dt is the rate of change of voltage across the capacitor.

Therefore $\frac{dV}{DT} = \frac{I}{C}$ Thus $\frac{dV}{dt} = \frac{Vin}{R1C}$

So, when a square wave is applied to the circuit in Fig. 10, triangle waveforms are generated. R2 was added to provide DC stability. Its inclusion does slightly corrupt the mathematical processes, but not enormously. A good point about this integrator design is that it has a very low ouput impedance. You can put a load on the output and the op-amp will still generate the same waveform — that's what is so nice about negative feedback.

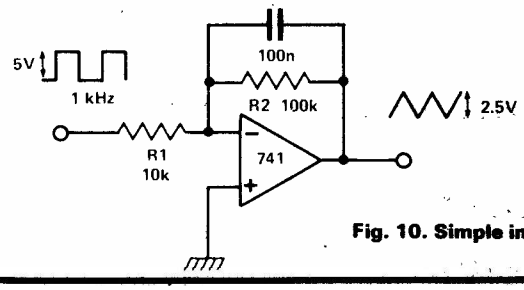


Fig. 10. Simple integrator.

Thus, as it tries to swing negative, it draws lots of current from the negative rail. This current flows through R5, and in doing so turns on Q2. This transistor then pulls R2 down and thus provides negative feedback. The same sequence of events occurs when the input is negative except that R3 and Q1 are then involved. Thus the high current capabilities of discrete transistors are combined with a high voltage gain of an op-amp to produce a moderately powerful amplifier. The voltage gain is set by R2/R1.

Transistors Q1 and Q2 introduce a phase shift, which may give rise to a high frequency instability and oscillation. This can be cured by some frequency compensation applied to the amplifier or by increasing the overall voltage gain.

No Noise Is Good Noise

The last op-amp characteristic to be discussed is Noise. The noise figures given in the specifications are very confusing. This is due to the fact that noise is specified in so many different ways that it is often difficult to compare devices. One may be specified in terms of Equivalent Input Noise and another device in terms of nV $\sqrt{}$Hz (nano volts per root Hertz)! As a generalisation it is true to say that most op-amps are relatively noisy. Some op-amps are labelled low noise, and these are quieter than the average op-amp but more noisy than a well designed discrete component amplifier. For audio work you can use ordinary op-amps for processing high level signals (100mV to 3V), but for amplifying low level signals (1 mV to 100mV) you would be advised to use a low noise device. The larger the voltage gain you obtain from an op-amp stage, the worse will be the noise, therefore keep the closed loop gain to a bare minimum.

That is the end of the theory, now for some practical examples of op-amps in use.

SIMPLE DIFFERENTIATOR

Mathematically, differentation is the reverse process to integration. Thus, in the differentiator circuit the C and the R are reversed with respect to the integrator circuit.

The input waveform is a triangle with a constant rise and fall slope. This constant slope, when presented to a capacitor will generate a constant current. When the slope direction reverses, then so will the current flow. This current when passed through a resistor (R1), will then generate a square wave.

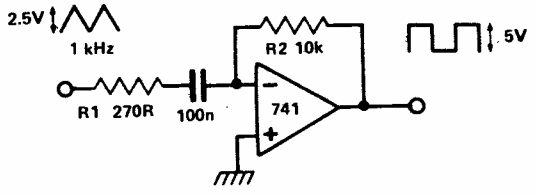


Fig. 11. Simple differentiator.

12 V REGULATED POWER SUPPLY

The large open loop voltage gain of an op-amp is very useful in providing a regulated low output impedance power supply. A 5V1 voltage reference is generated by a zener diode ZD1 (this voltage reference could be made more stable by running it at constant current). A PNP transistor is used as a series regulator. However, this transistor inverts the signal from the op-amp output, and so, in order to get negative feedback, the feedback is taken to the non-inverting input! The operation is as follows. The inverting input is held at 5V1. If the 'PSU OUTPUT' tries to fall, the voltage at the non-inverting input falls. Therefore the op-amp's output will also fall, thus turning on the PNP transistor which then pulls up the 'PSU OUTPUT.' Thus the output voltage is stabilised. Also, the output impedance is very low, due to this negative feedback. The output impedance at high frequencies (where the op-amp gain is low) is further reduced by the 10u capacitor. To squeeze the last drop of voltage out of the system, before a collapsing unregulated supply rail causes the regulated supply to drop out, a 5V1 zener diode (ZD2) has been included. This

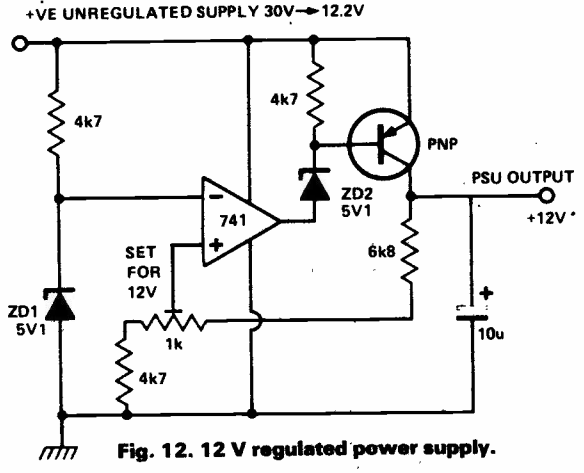


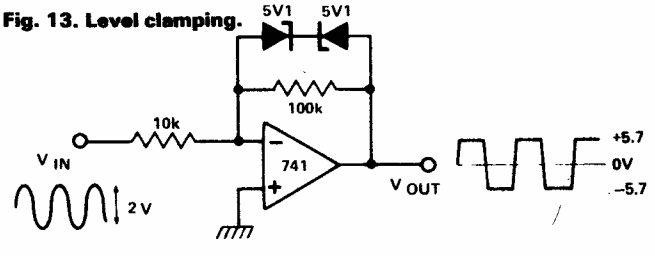
Fig. 12. 12 V regulated power supply.

allows the op-amp output to work at about 7 volts below the unregulated supply rail. Thus, a regulated output is maintained until the PNP transistor saturates. This means that the unregulated rail can fall to within about 200 mV of the regulated rail!

LEVEL CLAMPING

It is sometimes required to limit the excursion of the output voltage of a linear amplifier. This can be achieved by using non-linear feedback, in this case with zener diodes. Once the voltage at the op-amp's output exceeds the zener breakdown voltage plus a forward diode drop (0V7 from the forward biased Zener), the effective impedance of the feedback becomes very low. Thus the voltage gain, above this zener voltage, also becomes very low. The output voltage appears to be clamped at a fixed potential. By changing the zener value, this potential can be varied at will. Also, by making the two zeners have different values, correspondingly different negative and positive levels can be obtained. This circuit is, however, far from ideal. The zener diodes don't have very sharp 'Knees' in their transfer characteristics and the clamping can sometimes be very sloppy, particularly when low voltage zeners are used. Also, the zener diodes

Fig. 13. Level clamping.

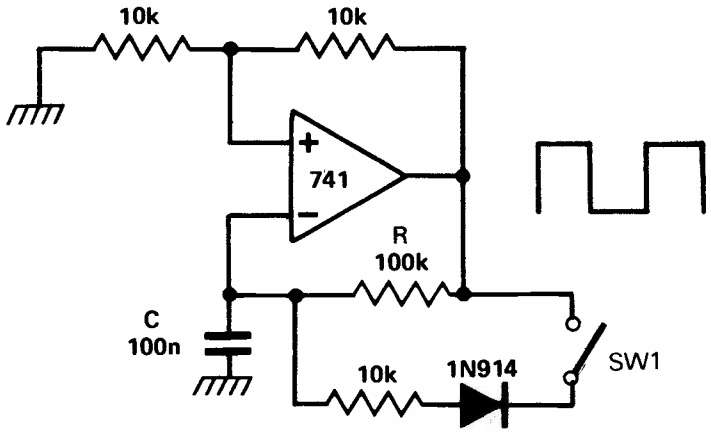


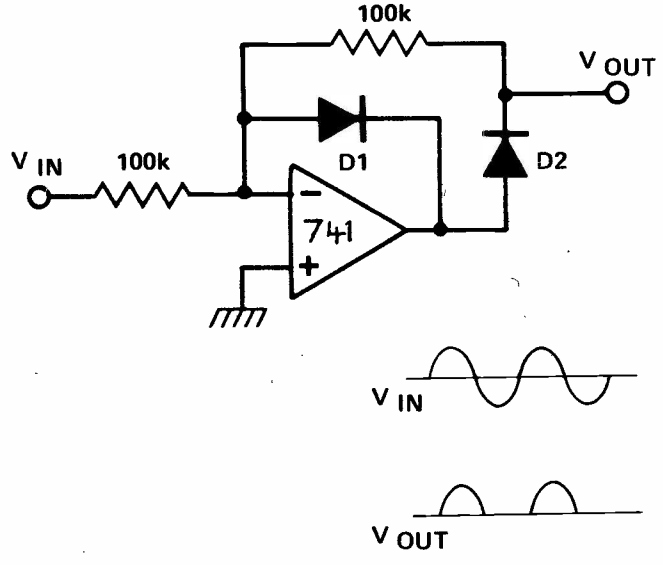
tend to have a large amount of charge storage, which impairs the high frequency performance.

Sometimes, however, sloppy clamping is considered useful. For instance, if the zeners are replaced by two ordinary diodes in parallel and pointing in different directions. Then any signal applied to the input will receive some non-linear distortion. This distortion is rich in odd harmonics, and is the basis of many FUZZ box designs for musical effects units.

Single Op Amp Oscillator

This circuit has a Schmitt trigger and a 'sort of integrator' all built around one op-amp. The positive feedback is via the 10k resistors. The 'integration', or rather, the timing, is controlled by the RC network. The voltage at the inverting input follows that of the RC charging exponential, except that it is confined to be within the upper and lower hysterysis levels. Thus the hysterysis levels and the RC time constant determine the frequency of the operation. It is possible to make the output square wave have a large mark to space ratio. By closing the switch SW1, the discharge time of the capacitor becomes eleven times faster than the rise time. Thus a square wave with an 11:1 mark space ratio is generated.

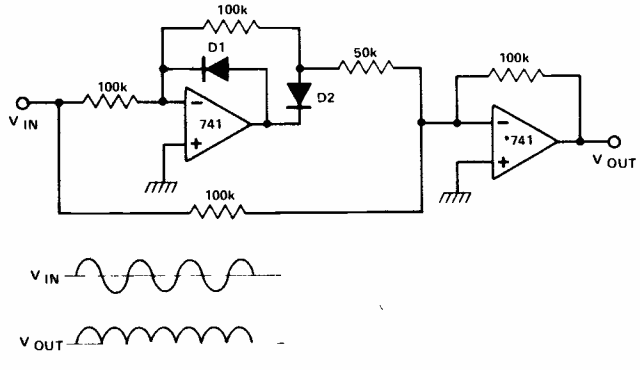




Precision Half Wave Rectifier

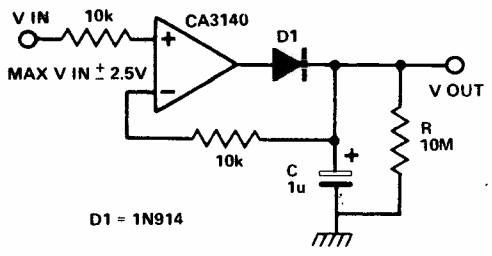
Rectifying small signals with any accuracy can be very difficult with just diodes due to their forward voltage drop of about 0.6 V. However, an op-amp can be used to reduce this voltage drop to apparently nothing. Consider the circuit shown. There is negative feedback so that 'virtual earth' circumstances exist. When Vin is positive, D1 conducts to maintain the virtual earth, D2 is reverse biased and so the output is just a 100k resistor connected to 0 V. When Vin goes negative, the output rises positively, D2 is turned on and D1 turned off. As the virtual earth is being maintained, the output voltage is the exact inverse of the input voltage. This is true for all negative inputs. Therefore, the output is composed of positive going half sinewaves. A precision half wave rectification has occurred. In fact the diode error is very small, being equal to

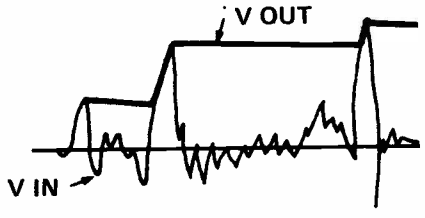
$$\frac{600\ \text{mV}}{\text{(surplus voltage gain)}}$$



Therefore as the input frequency increases, and the surplus voltage gain decreases, the amount of precision also falls.

By adding the original and the half wave rectified signals together in the right ratio, it is possible to fill in the half cycle gaps and thus to generate a precise full wave rectification. The addition of one summing op-amp and three resistors is all that is needed as shown opposite.



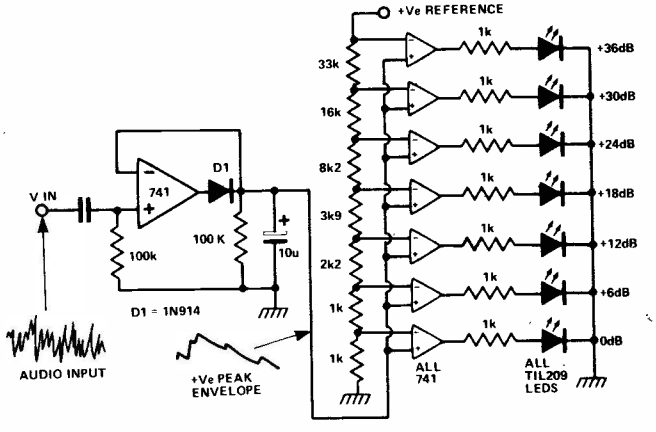


Precision Peak Voltage Detector with a Long Memory Time

The circuit shown has negative feedback only for positive signals. That is, the inverting input can only get some feedback when diode D1 is forward biased and this can only occur when the input is positive. When a positive input signal is applied the output of the op-amp rises until the inverting input reaches the same potential. In so doing, the capacitor C is also charged to this potential. When the input goes negative, the diode D1 becomes reverse biased and so the voltage on the capacitor remains there, being slowly discharged by the op-amp input bias current and the resistor R (10M). The op-amp used has a MOS FET input, having an exceptionally low input bias current of 10 pico amps. Thus the discharge of the capacitor is dominantly controlled by the resistor R, giving a time constant of ten seconds. Thus the circuit detects the most positive peak voltage and remembers it.

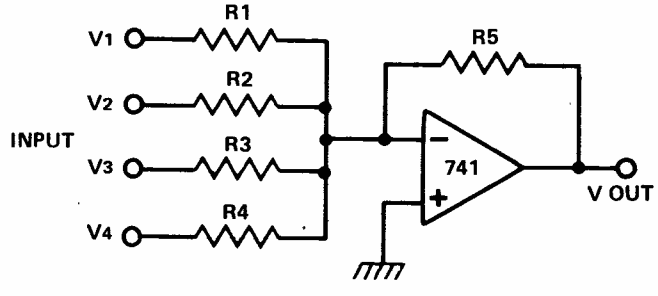
Led Bar PPM Display for Audio

The peak voltage detector can be used to control an illuminated audio level monitor displaying the same characteristics as a PPM (Peak Programme Meter). A bar column of LEDs is arranged so that as the audio signal level increases, more LEDs in the column light up. The LEDs are arranged vertically in 6 dB steps. A fast response time and a one second decay time has been chosen so as to give an accurate response to transients and a low 'flicker' decay characteristic. The op-amps that drive the LEDs are being used as comparators. On each of their inverting inputs they have a DC reference voltage, which increases in 6 dB steps up the chain. All of their non-inverting inputs are tied together and connected to the positive peak envelope of the audio signal. Thus as this envelope exceeds a particular voltage reference, that op-amp output goes high and the LED lights up. Also, all the LEDs below this are illuminated.



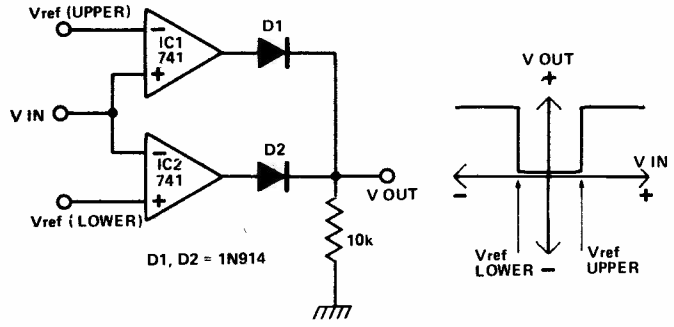
Basic Summing Circuit (Mixer)

A virtual earth amplifier can be used to mix several signals together. The output voltage is a mixture of all the inputs. The amount of an input that appears at the output is inversely proportional to the input resistor. If the input voltages are fed into potentiometers before being fed to the mixer, then their individual levels can be manually adjusted. This is the basis of most audio mixers, although only the cheaper units use op amps. Most op-amp mixers will degrade the signal to noise ratio of the signals by more than a good discrete component amplifier.



$$V_{OUT} = -R5\left(\frac{V1}{R1} + \frac{V2}{R2} + \frac{V3}{R3} + \frac{V4}{R4}\right)$$

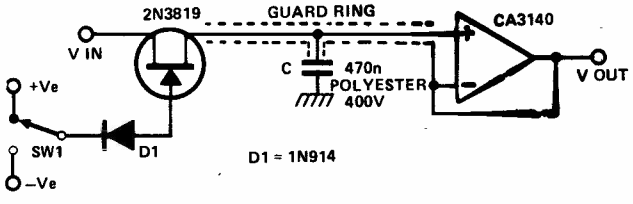
Window Comparator



A window comparator gives an output which in this case is 0 V, when an input voltage lies in between two specified voltages. When it is outside this 'window', the output is positive. The two op-amps are used as voltage comparators. When Vin is more positive than Vref (upper) the output of IC1 is positive and D1 is forward biased. Otherwise the output is negative, D1 reverse biased and hence Vout is 0 V. Similarly, when Vin is more negative than Vref (lower), the output of IC2 is positive; D2 is forward biased and thus Vout is positive. Otherwise Vout is 0 V. Thus only when Vin lies within the window set by the reference voltages is Vout 0 V.

High Performance Sample and Hold

It is often necessary to have a circuit that will sample an analogue voltage and then remember it for a long time without any significant corruption of that voltage. This is known as a sample and hold circuit and one use of it is to store the voltage from the keyboard connected to an electronic music synthesiser. The voltage is then used to control the pitch of a voltage controlled oscillator and so it is very important to have a high performance sample and hold. A drift of less than one semitone (80 mV) in ten minutes is required. A sample and hold is simply an electronic switch, a storage capacitor and a high input impedance voltage follower. In the circuit shown, when switch SW1 is positive the FET is turned on, and has a resistance of about 400R. Thus the input voltage charges up the capacitor through the FET. When SW1 is negative, the FET is turned off (pinched off), and can have a resistance of thousands of Megohms. To get a long storage time the op-amp must have a very low input bias current. For the CA3140, this current is about 10 pico amps, i.e., 10^{-11} amps. Therefore the rate at which the capacitor will be discharged by this current can be worked out from the equation, $C(dv/dt) = I$.



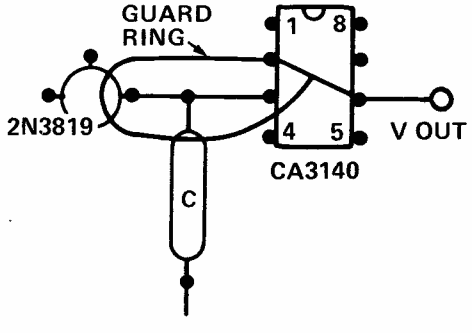
where dv/dt is the rate of change of voltage on the capacitor.
Therefore:

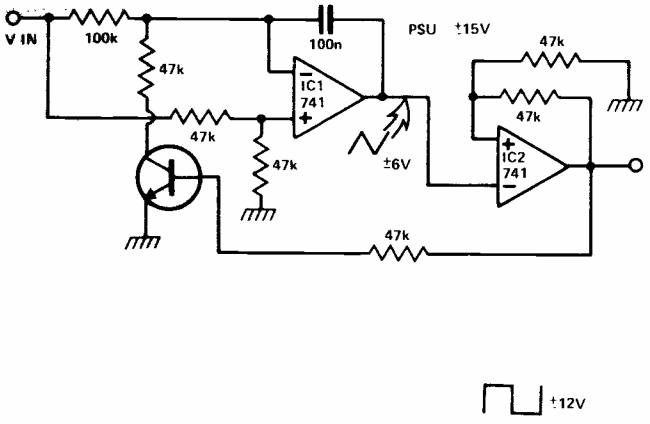
$$\frac{dv}{dt} = \frac{i}{C} = \frac{10^{-11}}{0.47 \times 10^{-6}} = 22\mu V/s$$

This is a very low drift rate, much better than we need. However, the actual drift rate will probably be in excess of this, due to surface leakage on the printed circuit board, leakage through the FET, and internal leakage in the capacitor. It is advisable to use a high voltage, non-polarised capacitor in this circuit to keep the leakage currents to a minimum. Also, to stop surface leakage a simple PCB trick can be used, that of making a guard ring around the sensitive components.

Normally any potential stored on the capacitor may leak to ground across the surface of the PCB, but if we make the surrounding surface a conducting track held at the same potential as that of the capacitor then the potential difference is virtually always zero, and hence the surface leakage is greatly reduced.

PRINTED CIRCUIT BOARD LAYOUT





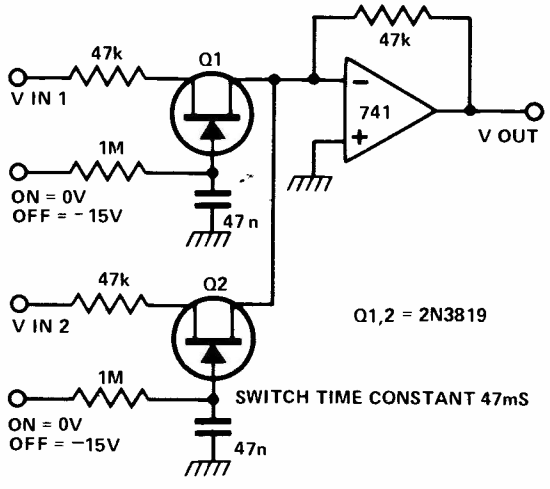
Linear Voltage Controlled Oscillator

This oscillator is very similar to the triangle square wave oscillator shown in Part 1, except that this one is voltage controlled. The integrator and Schmitt trigger action are the same as before, but the feedback has been altered. The input voltage Vin is applied differentially to the integrator via the resistor network. The larger the value of Vin, the faster the integrator ramps up and down. Thus the frequency of the operation is determined by an external positive control voltage. The frequency is linearly proportional to this control voltage.

When the output of the Schmitt is low, Q1 is off and so all the input voltage is applied to the inverting input. Half of the input voltage is always applied to the non-inverting input. Therefore the integrator's output ramps downward until the Schmitt flips into its positive state. Now, Q1 is switched on and the voltage at the inverting input is negative with respect to the non-inverting input. Hence the integrator now ramps upwards.

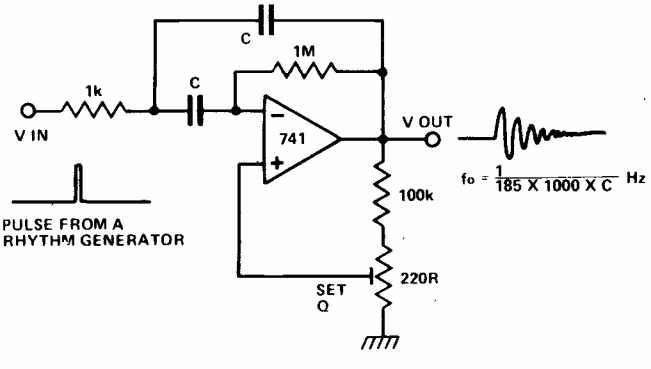
Silent Audio Switching

Sometimes electronic switches for audio signals are required. FETs can be used to perform the switching, but they can cause distortion, the resultant output impedance is not very low and clicks generated by the switching signal can break through. The circuit shown virtually eliminates all of these problems. By using an op-amp a very low output impedance is obtained as well as the possibility of selecting or mixing one or more of many input channels. Because of the virtual earth mixing, the voltage across any FET that is switched on is very small. If the input voltage is 1V and the FETs ON resistance is 470R, then the voltage across the FET is about 10 mV. When large voltages are applied to a turned on FET, the distortion is large, but if the voltage is small (10 mV, say), the distortion could be less than 0.1%. Thus the virtual earth mixing enables low distortion operation. Lastly, to stop the generation of switching clicks, a time constant of 47 msec has been enforced at the gate of the FETs.

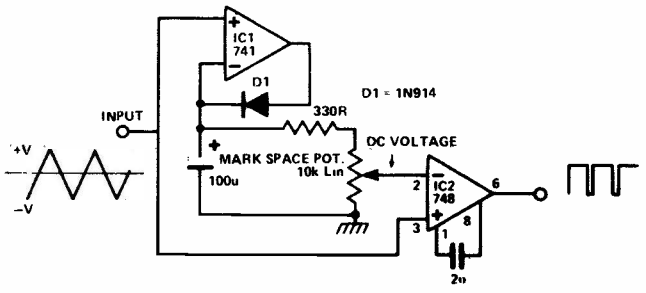


Simple Musical Chime Generator

The circuit shown is that of a multiple feedback band-pass filter. The preset is used to add some positive feedback and so further increase the Q factor. The principle of operation is as follows. A short click (pulse) is applied to the filter and this makes it ring with a frequency which is its natural resonance frequency. The oscillations die away exponentially with respect to time and in doing so closely resemble many naturally occurring percussive or plucked sounds. The higher the Q the longer the decay time constant. High frequency resonances resemble chimes, whereas lower frequencies sound like claves or bongos. By arranging several of these circuits, all with different tuning, to be driven by pulses from a rhythm generator an interesting pattern of sounds can be produced. There may be some stability problems when high Q or high frequency operation is involved. To achieve better performance, an op-amp with a greater bandwidth than the 741 should be used. Alternatively, a different structure, such as a state variable filter could be used. Qs of up to 500 can be obtained with this latter circuit.

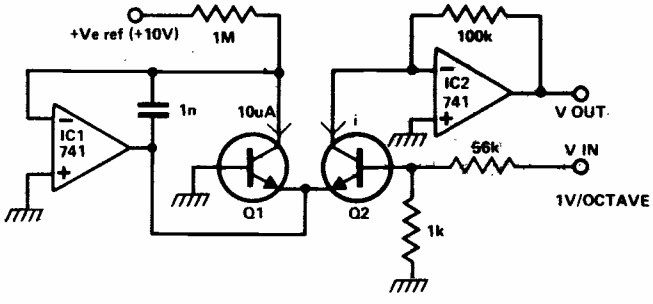


Variable Markspace Squarewave Generator with Automatic Level Adjustment



By putting a triangle wave into one input of a comparator and a manually controlled DC level into the other, it is possible to generate a variable ratio mark/space square wave. However, if the amplitude of the triangle varies then so will the markspace ratio. Alternatively, if you want the manual control to produce a very thin waveform at one end of its travel, then you will probably need a preset and a very stable triangle amplitude. However, this circuit solves these problems. The DC voltage is generated by a peak voltage follower, IC1, driven by the triangle itself. Thus the circuit tracks the peak voltage level. Secondly, only 97% of this voltage is ever fed to the comparator, IC2, and so at the end of the markspace pot, a 60:1 ratio square wave is generated. At the other end of the pot the ratio is 1:1. A 748 is used as the comparator because it has more bandwidth than the 741. As the frequency of the triangle increases, it may be necessary to use an even faster op-amp for IC2 or even a comparator.

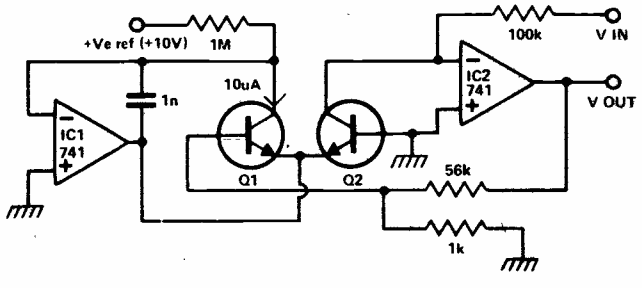
Exponential Voltage to Current/Voltage Converter



The circuit shown converts a linear input voltage into an exponential current or voltage. This type of circuit is used in music synthesisers to change linear control voltages into musical intervals. That is, if the circuit were used to control an oscillator, input increments of 1 V would change the pitch by one octave. The exponential characteristics of a transistor are exployed to generate the correct transfer function. Q1 and Q2 are a matched pair of transistors, preferably a transistor dual. IC1 maintains Q1 at a constant current. Thus, the op-amp serves only to bias the emitter of the second transistor Q2 into a suitable operating region. The purpose of Q1 is to generate this bias voltage. The base emitter junction of a transistor has a high temperature coefficient (—1.9 mV/°C) and so the reason for using a matched pair is to use the first transistor, Q1, to provide temperature compensation for the second.

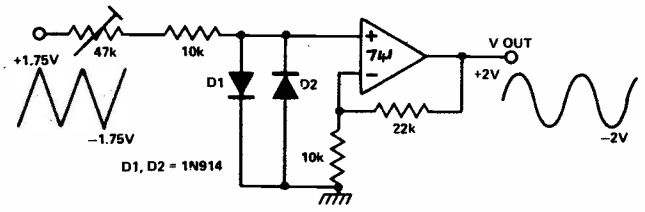
Logarithmic Voltage to Voltage Converter

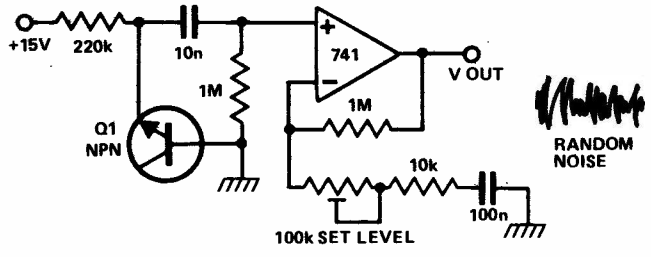
The output voltage is logarithmically proportional to the input voltage. The difference between this circuit and the previous is that the exponentiator is in the feedback loop of the op-amp and hence the mathematical function has been inverted. The circuit is useful for performing true logarithmic compression or for converting linear inputs into dBs.



Simple Triangle to Sinewave Converter

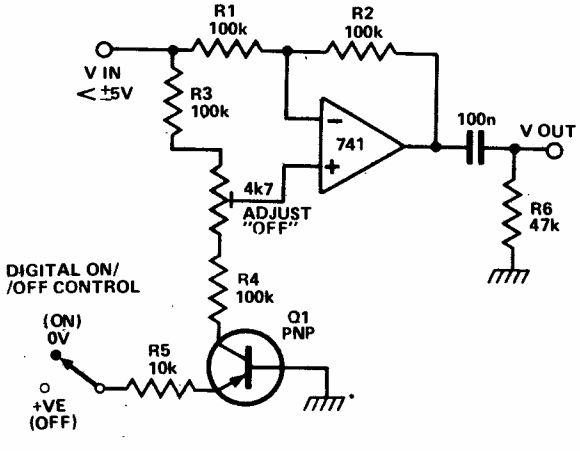
A simple way of converting a triangle to a sinewave is shown. The logarithmic characteristic of the diodes is used to approximate to that of a sine curve. The distortion to be expected is of the order of 5%. However, the distortion may be tolerable if the sinewave is only used to generate audio tones.





Noise Generator

The zener breakdown of a transistor junction is used in many circuits as a noise generator. The breakdown mechanism is random and so generates a small noise voltage. Also this voltage has a high source impedance. By using the op-amp as a high input impedance, high AC gain amplifier, a low impedance, large signal noise source is obtained. The preset is used to set the noise level by varying the gain from 40 to 20 dB.

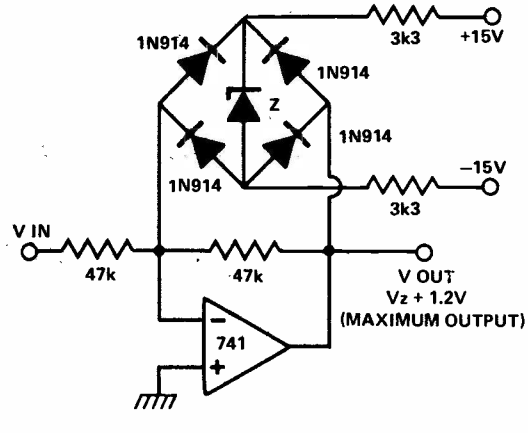


Transistor Used To Turn An Op Amp On Or Off

When transistor Q1 is switched off, the circuit behaves as a voltage follower. By applying a positive voltage to the emitter of Q1 via a 10K resistor, the transistor is made to turn on and go into saturation. Thus the lower end of R4 is shorted to ground. The circuit has now changed into that of a differential amplifier (see fig 7, Part 1), but where the voltage difference is always 0v. Now as long as the resistor ratios in the two branches around the op-amp are in the same ratio then there should be zero output. A 4K7 preset is used to null out any ratio errors so that the 'OFF' attenuation is more than 60dB. The high common mode rejection ratio of a 741 enables this large attenuation to be obtained.

Fast Symmetrical Zener Clamping

The problem with using two zeners, back to back in series to get symmetrical clamping are One: the knee of the zener characteristic is rather sloppy. Two: charge storage in the zeners causes speed problems and Three: the zeners will have slightly different knee voltages and so the symmetry will not be all that good. The circuit overcomes these problems. By putting the zener inside a diode bridge then the same zener voltage is always experienced. The voltage errors due to the diodes are much smaller than those due to the zener. Also the charge storage of the bridge is much less. Lastly by biasing the zener on all the time, the knee appears to be much sharper.

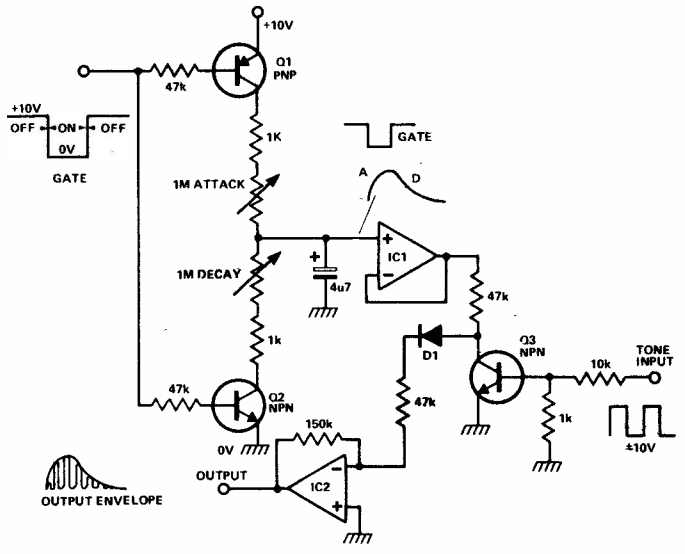


Musical Envelope Generator and Modulator

A gate voltage is applied to initiate the proceedings. When the gate voltage is in on the ON state, Q1 is turned on, and so the capacitor C is charged up via the attack pot in series with the 1K resistor. By varying this pot, the attack time constant can be manipulated. A fast attack gives a percussive sound, a slow attack the effect of 'backward' sounds. When the gate voltage returns to its off state, Q2 is turned on and the capacitor is then discharged via the decay pot and the other 1K resistor, to ground. Thus the decay time consant of the envelope is also variable.

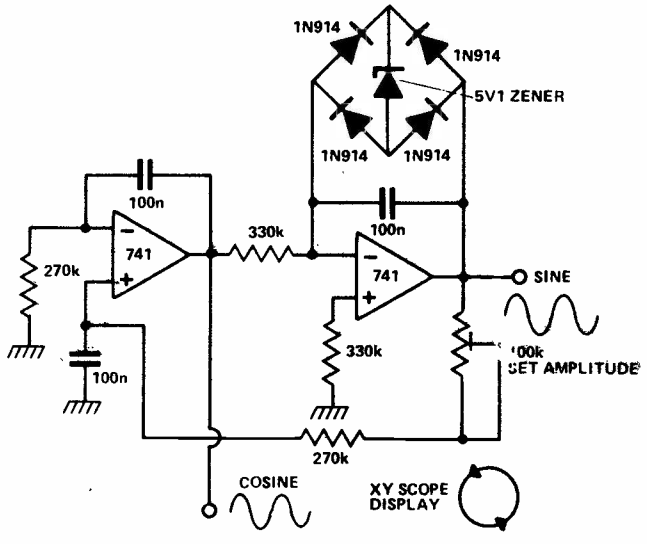
This envelope is buffered by IC1, a high impedance voltage follower and applied to Q3 which is being used as a transistor chopper. A musical tone in the form of a squarewave is connected to the base of Q3. This turns the transistor on or off and thus the envelope is chopped up at regular intervals, the intervals being determined by the pitch of the squarewave.

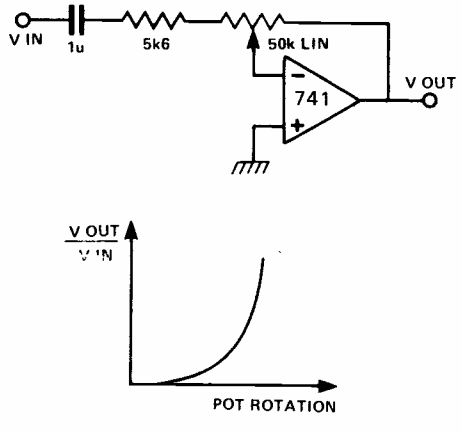
The resultant waveform has the amplitude of the envelope and the harmonic structure of the squarewave. IC2 is used as a virtual earth amplifier to buffer the signal and D1 ensures that the envelope dies away at the end of a note.



Drawing circles on a scope

The circuit is that of a quadrature sine and cosine oscillator. Two integrators are employed and there is overall positive feedback. Thus the system oscillates producing sinusoids. Amplitude stabilisation is obtained with a diode bridge and a zener diode. The process of integration produces a 90° phase shift. Therefore if there is a sine wave being put into an integrator, a cosine will appear at its output. Quadrature oscillators can be used to generate circular displays on oscilloscopes by connecting the two outputs to the X and Y inputs. Other uses include quadrature panning in voltage controlled audio systems and they are also used in audio frequency shifters.





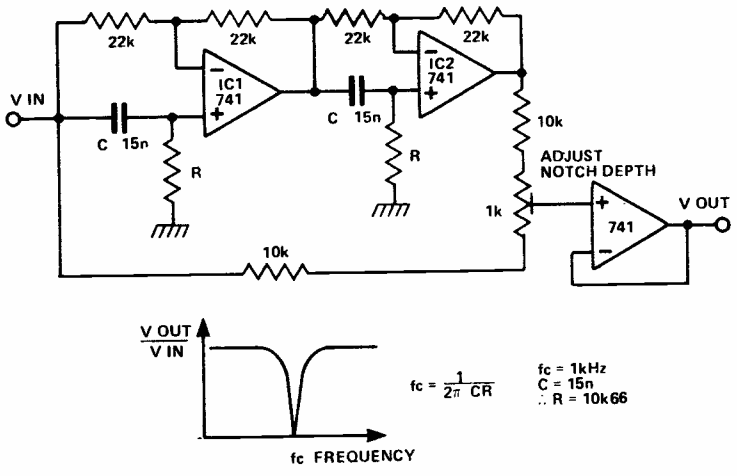
Turning a Linear Pot into a Log Pot

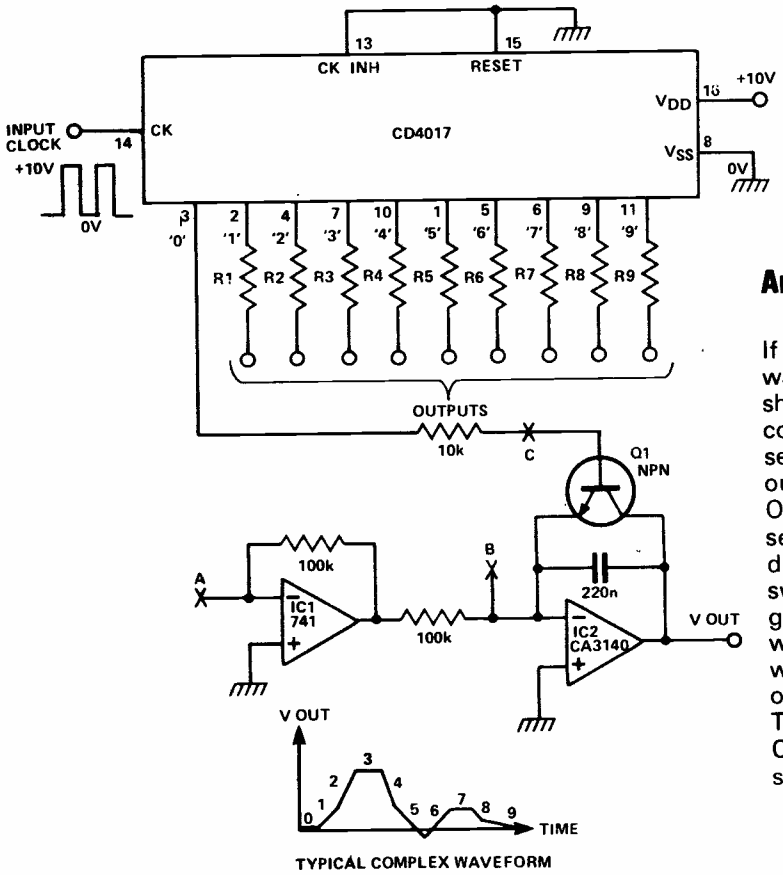
By using the virtual earth characteristic of an op amp, a linear pot can be made to have the characteristics of a log pot. It seems to be fair to say that low cost linear pots are far more linear than log pots are logarithmic. Thus the linear pot can be turned into a better log pot than the actual log pot itself. By varying the resistor ratio 5k6 to 50k, other laws can be produced, such as something in between log and linear or maybe a law that is even more extreme than a log law.

All Pass Notch Filter

Sometimes when processing analogue signals there is a constant tone which is causing a nuisance and so an active filter is called upon to notch it out. The filter can be tuned so that its notch is at exactly the same frequency as this signal so that it can be selectively attenuated. This method is sometimes used to remove unwanted mains hum from poor quality recordings. The circuit works as follows: IC1 and 2 are a pair of all pass filters. These filters have a flat frequency response, but their phase changes with frequency. Their overall maximum phase shift is 360°, a phase shift of 180° occurring at a frequency of 1 / 2CR Hz. At this frequency the signals are inverted. Thus, by mixing the phase delayed signal with the original, cancellation can be produced which forms a notch in the frequency response. The preset is used to get the deepest notch available. The operating frequency can be changed by varying the two resistors R. For instance for 50 Hz operation, R should be:

$$10.66k \times \frac{1000}{50} = 213.2k$$ Nearest E12 fit is 220k.





TYPICAL COMPLEX WAVEFORM

Analogue Linear Segment Drawer

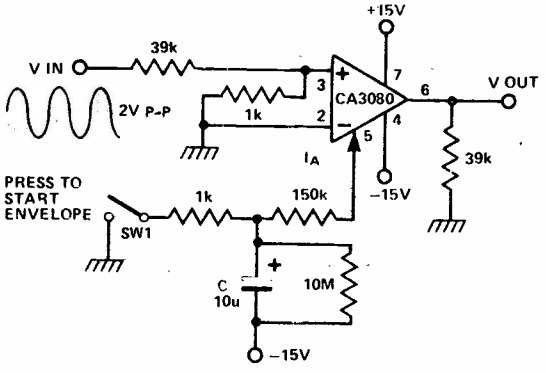
If you want to draw, repeatedly, a complex analogue waveform with up to 9 discrete sections then the circuit shown will enable you to do it. The CD4017 is a decade counter / decoder. A clock is applied to its input and a sequence of decoded outputs is generated. That is, output 0 goes high, then output 1, then output 2, etc. Only one output is high at any point in time. This is the sequence generator. There is also an inverter (IC_1) which drives an integrator (IC_2) which can be reset to zero by a switch. Thus, if we connect output 1 to A, the integrator's output will ramp upwards, if we connect it to B it will ramp downwards and if we connect it to C the switch will clamp the output to 0V. Also, by varying the values of R1 to 9, the integrator's ramp rate can be controlled. Thus by selectively routing the outputs to either A, B, or C and by selecting the resistor values, a complex 9 segment waveform can be drawn out.

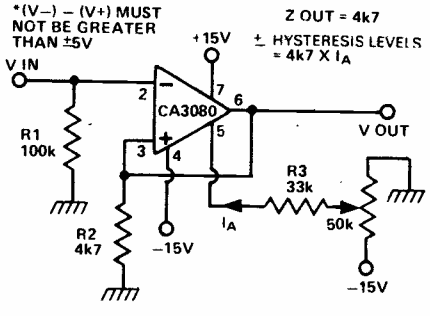
Simple Musical Envelope Generator

A simple generator can be constructed using the CA3080, made by RCA. This circuit will also enable the use of any audio waveform the harmonic structure of which will not be significantly affected as it is modulated. The CA3080 is an op amp with a difference. It has a current output and an extra input into which a current, I_A is fed. The output is the product of the input voltage X I_A. Thus the I_A can be used to control the amplifier's gain.

Also the input voltage range for low distortion operation is very low, of the order of ± 25mV.

In this circuit, the CA3080 is being used as a two quadrant multiplier. A small voltage, (± 25 mV), is applied to its non-inverting input. When the switch S1 is closed, the capacitor C is charged up and a current of about 150μ A flows into the I_A input terminal. When S1 is opened, C discharges through the 150k resistor into the I_A input. This current dies away exponentially. As the output is the product of the input voltage × I_A, then an exponential envelope is generated. Breakthrough after the decay is very good, better than —80 dB.



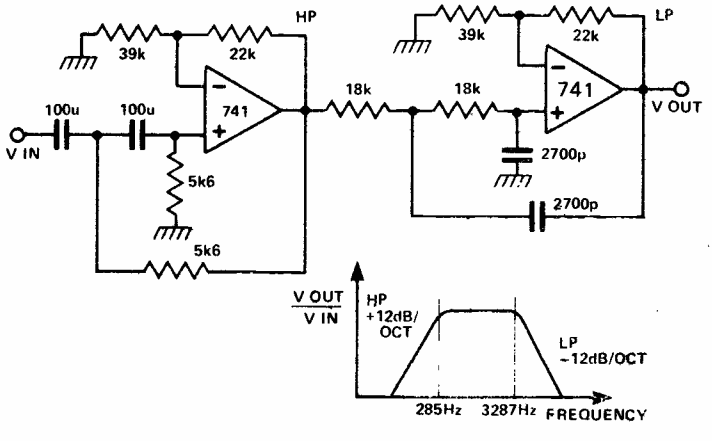


Simple Schmitt Trigger with Programmable Hysteresis

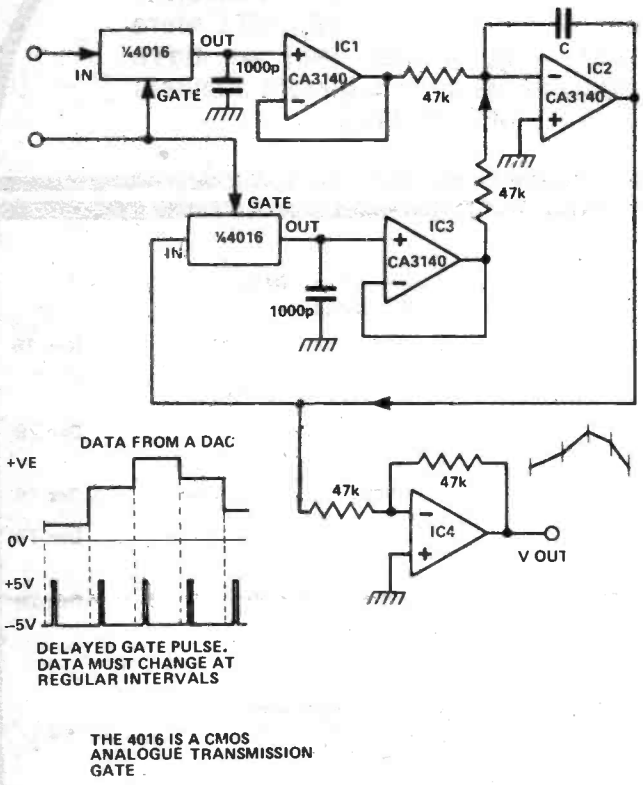
Again the multiplier qualities of a 3080 can be used to produce a versatile schmitt trigger. DC positive feedback is used and so a schmitt trigger action is produced, although the size of the hysteresis levels is determined by I_A. All of the I_A current flows out of the amplifier's output and through R2, thus setting up the hysteresis level. Therefore increasing I_A will increase this level and vice versa. The positive and negative hysteresis levels are symmetrical about 0V.

Simple Speech Filter

The telephone system has been designed for speech communication. The bandwidth of the system is 300 Hz to 3400 Hz, which has been arrived at after many years of experimentation. Thus, it is true to say that much of the information in speech is contained between these frequency limits. The circuit shows a filter structure that will simulate the telephone bandwidth. It could have many uses, for instance as a 'speech filter' for noisy radio reception or land line communications, or as a voice detector for a light show.



Cleaning Up Digitally Generated Signals With 2 Sample and Holds and an integrator

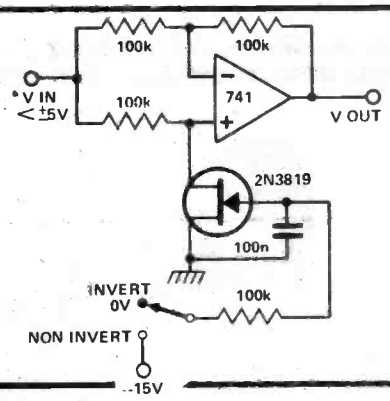


THE 4016 IS A CMOS ANALOGUE TRANSMISSION GATE

The output from a digital to analogue converter (DAC) is composed of a series of steps which have been selected by a series of binary numbers. The output of the DAC may represent the result of some computation done by a microprocessor or the contents of a digital memory. If the number of bits that control the DAC is low (less than 8), then the output will look like a series of discrete steps, plus lots of digital 'glitches'. Therefore, if this signal is to be displayed on an oscilloscope, the overall picture quality will be very poor. One way to clean up things would be to join up all the steps with straight lines and if done successfully a great improvement can be obtained. The only problem is that the distance between steps is continuously varying and so the slope of the straight lines will need to be variable as well. This process is known as linear point interpolation and can be achieved with two sample and holds and an integrator.

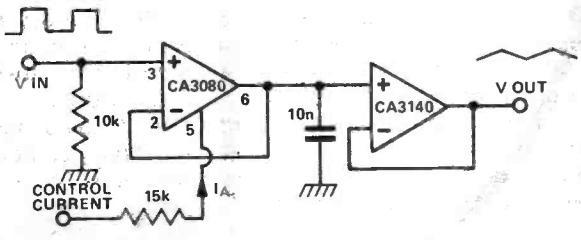
A delayed gate pulse is generated, so that once the DAC's output has settled the sample and hold switches momentarily open, sample the information and then close. The output of the first sample and hold (IC1) drives an integrator (IC2), the output of which drives the second sample and hold (IC3). The second unit provides negative feedback around the integrator, but it is delayed by one time interval. Thus a momentary positive going signal will pass through the first sample and hold and cause the integrator to ramp in a negative direction. When the next time interval arrives, the first sample and hold returns to 0V, and the second obtains a negative voltage. This then makes the integrator ramp positively. The size of the integrator's capacitor C should be chosen to suit the clock speed of the DAC. An inverter, IC4 has been included to correct the inversion caused by the integrator.

Digitally Controlled Invert/Non-Invert



The FET is digitally controlled to be either ON (a few hundred ohms shorting the non-inverting input of the IC to ground), or OFF (an open circuit). When the FET is OFF, the circuit is that of a voltage follower. When the FET is ON, the non inverting input is, to all intents and purposes, grounded, and so the circuit is that of a virtual earth amplifier with a voltage gain of —1, that is, an inverter.

Controllable Slew Limiter



The current output of a CA3080 can be used to produce a controllable slew limiter. The 3080 is used as a voltage follower, but with a capacitive load. Thus it is possible for this stage to correctly follow small signal variations, but to slew limit when the input signal is larger. The speed of the slew limiting is determined by the current I_A. A high input impedance voltage follower (CA3140) is used to buffer the signal. This circuit is sometimes used as a non-linear filter to limit fast signals; also, it can be used as a portamento circuit for a music synthesiser.

ETIPRINTS

ETIPRINTS are a fast new aid for producing high quality printed circuit boards. Each ETIPRINTS sheet contains a set of etch resistant rub down transfers of the printed circuit board designs for several of our projects.

ETIPRINTS are made from our original artwork ensuring a neat and accurate board. We thought ETIPRINTS were such a good idea that we have patented the system (patent numbers 1445171 and 1445172).

PARTS LIST

Shown below is the listing for the last year's ETIPRINTS.

Earlier sheets are available, ring Tim Salmon for details.

026	Motor Speed Controller (2 Boards For Controller) Battery Indicator	July 79
027	CCD Phaser Rev. Monitor	Project Book Seven
028	Race Track, Spirit Level Egg Timer, Bongos Bench Supply, Oscillator	Project Book Seven
029	Bass Enhancer Digital Freq. Meter (4 boards)	Project Book Seven
030	ETIWET, Continuity Tester Metal Locater, Light Dimmer Ultrasonic Switch (2 boards)	Project Book Seven
031	Tone Control House Alarm (2 boards) Torch Finder	Project Book Seven
032	LED Audio Display (2 boards) (underside pattern)	Aug 79
033	LED Audio Display (2 boards) (topside pattern) Bench Amp NICD Charger	Aug 79
034	Cable Tester Reaction Tester Speech Compressor Preamp Power Supply Rectifier & De-Thump Board Power Amp (2) (price £1.60)	Nov 79
035	Oven Leakage Detector Pinball Wizard	Nov 79
036A	3 x Display Board Relay Activator Points Controller	Nov 79
036B	Data Distributor (double sided)	Nov 79
036C	Train Speed Controller Track Cleaner & Electronic Pot (double sided)	Nov 79
036D	Power Switch Selector (double sided)	Nov 79
037A	Encoder (double sided)	Dec 79
037B	Decoder (top side)	Dec 79
037C	Decoder (bottom side)	Dec 79
038A	Long Period Timer Rain Alarm Touch Switch Flash Trigger Pseudo Random Noise Gen	Dec 79
038B	Hum Filter Dice Logic Probe	Dec 79
038C	Function Generator	Dec 79
039	Buffer Moving Coil Preamp Process Controller	Jan 80

HOW IT WORKS

Lay down the ETIPRINT and rub over with a soft pencil until the pattern is transferred to the board. Peel off the backing sheet carefully making sure that the resist has transferred. If you've been a bit careless there's even a 'repair kit' on the sheet to correct any breaks!

BUY LINES

ORDER TODAY

Send a cheque or P.O. (payable to ETI Magazine) to:

ETI PRINT, ETI MAGAZINE
145 Charing Cross Road, London WC2H 0EE

80p INC P & P

TRANSISTOR OPERATING POINT

Designing a transistor amplifier? Take the guessing out of finding the correct DC or static operating point of a transistor with this simple approach by W. R. Masefield.

In the design of transistor amplifiers, one of the first considerations is to establish the correct DC or static operating point for the transistor. Probably the most common method used by the amateur is that of having a guess, followed by trial and error juggling with components on the breadboard.

There is no need for that; there *is* a way of predicting the operating point and finding some of the circuit component values to be optimised before leaving the drawing-board. Nor is any advanced mathematics used, but it is as well to have a calculator with logs to base e facility.

Common Law

Whatever circuit configuration is used, common emitter, common base, common collector (emitter follower), the fact does not alter that there is a certain relationship between the base-emitter voltage V_{BE} and the emitter current I_E. This relationship is exponential, and, because of this, a plot of $\ln I_E$ against V_{BE} is a straight line as in fig. 1.

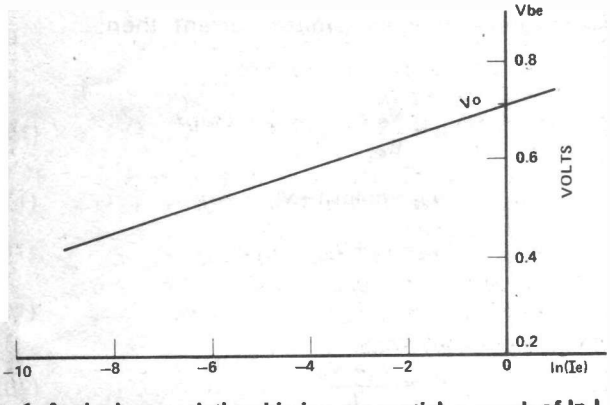


Fig. 1. As the I_E, v_{be} relationship is exponential, a graph of ln I_E against V_{BE} is a straight line.

It is a simple matter to verify this, using the circuit of fig. 2. The voltmeter must have a high impedance, otherwise the value of I_E will be incorrect.

As the graph is a straight line, it can be described by the linear equation:

$$V_{BE} = m(\ln I_E) + V_0 \quad \ldots\ldots\ldots\ldots \quad (1)$$

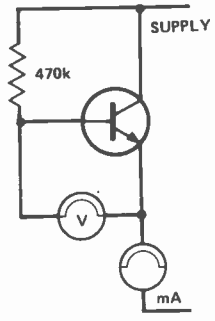


Fig. 2. The circuit used to verify the relationship between I_E and V_{BE}.

This equation is extremely useful, and it is worthwhile determining the slope, m, and the intercept, V_o for any transistor to be used in the circuit under development.

As the graph is a straight line, only two points are needed to determine it. One point is given by the intercept on the V_{BE} axis. This is V_o and is the base-emitter voltage when the $\log_e$ of the emitter current is zero, i.e. when I_E = 1 mA.

If the emitter current is now changed to I_E, and the corresponding base-emitter voltage is V_{BE}, then the slope, m, is given by

$$m = \frac{V_0 - V_{BE}}{\ln 1 - \ln I_E} \quad \ldots\ldots\ldots\ldots \quad (2)$$

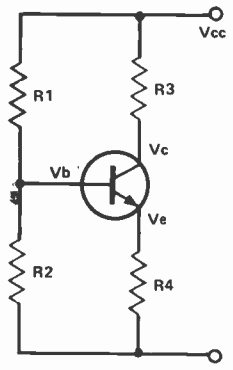
This turns out to be of the order of 30×10^{-3} when V_{BE} is in volts and I_E is in mA.

The only other parameter required is h_{FE}. Note that this is *not* h_{fe} which is the dynamic forward current transfer. h_{FE} is the static forward current transfer, and can be determined by measuring I_c and I_b. Then:

$$h_{FE} = \frac{I_c}{I_b} \quad \ldots\ldots\ldots\ldots \quad (3)$$

Armed with these three parameters, m, V_o and h_{FE}, the operating conditions in any circuit can be found. These are summarised below. The resistor suffixes have been so chosen to make things easier when writing a calculator program for speeding up the calculations.

Fig. 3 Common Emitter Mode with base potential bias



The given conditions will be supply rail voltage, V_{cc}, the desired collector voltage V_c, generally half rail voltage, the collector load, R_3, to give a suitably low output resistance and economical I_c, and the potential divider R_1, R_2 to take a current that is likely to swamp the base current and so give a fixed reference voltage, usually about 2V at the base. Then:

$$V_B = \frac{V_{cc} \cdot R_2}{R_1 + R_2} \quad \ldots\ldots (4)$$

$$I_c = \frac{V_{cc} - V_c}{R_3} \quad \ldots\ldots (5)$$

$$I_E = I_c\left(1 + \frac{1}{h_{FE}}\right) \quad \ldots\ldots (6)$$

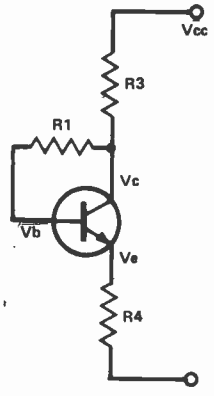
$$V_{BE} = m(\ln I_E) + V_0 \quad \ldots\ldots (7)$$

$$V_E = V_B - V_{BE} \quad \ldots\ldots (8)$$

$$R_4 = \frac{V_E}{I_E} \quad \ldots\ldots (9)$$

This sequence therefore enables the critical resistor R_4 to be determined accurately.

Fig. 4 Common Emitter with Base-Collector Resistor Bias



Given the supply rail voltage, V_{cc}, the collector voltage V_c about half V_{cc}, and the emitter voltage, V_E generally 1 volt, the load R_3 is again chosen as a compromise between low output resistance and low collector current, then:

$$I_E = I_c = \frac{V_{cc} - V_c}{R_3} \quad \ldots\ldots (10)$$

$$R_4 = \frac{V_E}{I_E} \quad \ldots\ldots (11)$$

$$I_B = \frac{I_E}{1 + h_{FE}} \quad \ldots\ldots (12)$$

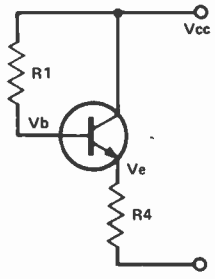
$$V_{BE} = m(\ln I_E) + V_0 \quad \ldots\ldots (13)$$

$$V_{R1} = V_c - V_{BE} - V_E \quad \ldots\ldots (14)$$

$$R_1 = \frac{V_{R1}}{I_B} \quad \ldots\ldots (15)$$

This sequence enables both R_1 and R_4 to be determined accurately.

Fig. 5 Common Collector (Emitter Follower)



Given the supply rail voltage, V_{cc}, the emitter voltage, V_E, usually half the rail voltage, and the emitter load, R_4 is chosen to give a compromise between low output resistance and economical emitter current, then:

$$I_E = \frac{V_E}{R_4} \quad \ldots\ldots (16)$$

$$V_{BE} = m(\ln I_E) + V_0 \quad \ldots\ldots (17)$$

$$V_B = V_E + V_{BE} \quad \ldots\ldots (18)$$

$$I_B = \frac{I_E}{1 + h_{FE}} \quad \ldots\ldots (19)$$

$$R_1 = \frac{V_{cc} - V_B}{I_B} \quad \ldots\ldots (20)$$

This sequence allows R_1 to be found accurately.

Although, on paper the above sequences look laborious, if a programmable calculator is available, it is possible to put all of them into program memory, and all data in the data registers, then try different values of resistors until optimum values are found. At this stage the breadboard may be prepared, in the knowledge that the values obtained will be close to those actually needed.

40 CMOS CLOCKS

There are many ways of using the CD4001 and CD4011 CMOS ICs to make bistable, astable and monostable multivibrator circuits. Ray Marston presents the definitive work on the subject, with 40 practical circuits.

The amateur and professional circuit designer often finds himself in the situation where he needs to use a minimum-cost CD4001 or CD4011 CMOS pulse or clock generator circuit, or where he needs to use a few spare CMOS NAND or NOR gates from an existing circuit to make up a multivibrator that will meet his specific design needs. In either case, the designer will find a concise guide to practical NAND- or NOR-gate CMOS multivibrator circuits of inestimable value.

This is just such a guide. It presents some forty different ways of using the low-cost CD4001 and CD4011 quad 2-input gate CMOS integrated circuits in bistable, astable and monostable multivibrator applications. All of the circuits shown can be operated over the full five volts to fifteen volts supply range when used with 'B' series CMOS.

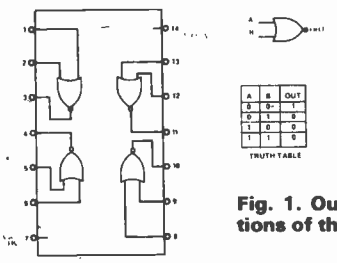


Fig. 1. Outline and pin connections of the CD4001.

THE CD4001 and CD4011 ICs

Figures 1 and 2 show the outlines and pin connections of the CD4001 and CD4011 integrated circuits. These two ICs are quad 2-input gates. The CD4001 provides NOR gate functions and the CD4011 provides NAND gate functions. Fig. 1 shows the truth table of each of the four NOR gates of the CD4001. Note that the output is high if both inputs are low, but goes low if either or both inputs go high. Fig. 2 shows the truth table of each of the four NAND gates of the CD4011. The output is normally high and goes low only if both inputs are high.

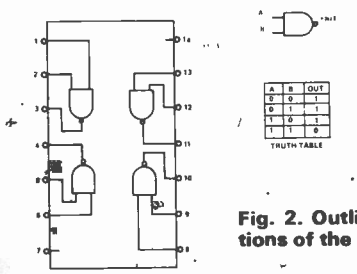


Fig. 2. Outline and pin connections of the CD4011.

The CD4001 and CD4011 are very inexpensive ICs. They typically retail at about 16 pence each in one-off quantities (allowing for some variation between suppliers), which works out at about 4 pence per gate. They can be used in a wide variety of very useful two-gate multivibrator applications and are thus highly cost-effective devices.

Bistable Multivibrator Circuits

The CD4001 and CD4011 can both be used in two-gate R-S (Reset-Set) bistable multivibrator circuits, but have quite different input triggering requirements. Fig. 3 shows the practical circuit and waveforms of a pulse-triggered NOR version of the bistable. The circuit has two outputs, a normal output from IC1a and an inverted output from IC1b. When a positive-going trigger pulse which switches between roughly zero and full supply is applied to the IC1b input, the normal output sets high and locks in this state irrespective of any further signals at the input of IC1b. The output can only be reset low again by applying a positive-going pulse to the input of IC1a, at which point the output goes low and is then immune to any subsequent trigger pulses at the input of IC1a.

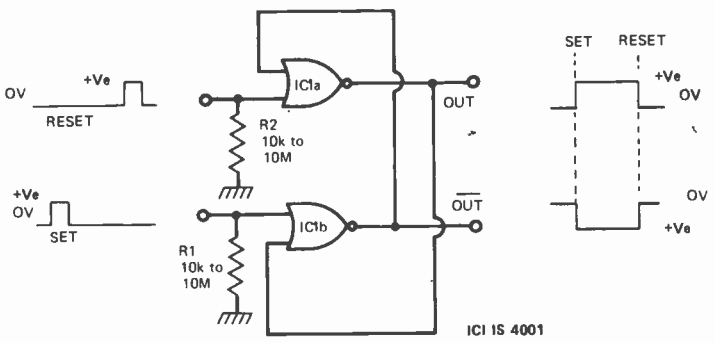


Fig. 3. Practical circuit of a pulse-triggered NOR bistable.

Note that the input terminals of IC1a and IC1b are tied to ground (the zero-volts line) via R1 and R2: these resistors can have any convenient values in the range 10k to 10M. If inputs to IC1a and IC1b are direct-coupled from preceding logic networks, however, R1 and R2 can be omitted from the circuit.

Manual NOR Gate

Fig. 4 shows a manually-triggered version of the Fig. 3 NOR gate circuit. This type of circuit is often referred to as a 'noiseless' switch, since its output is unaffected by the contact bounce, etc., of its two control switches.

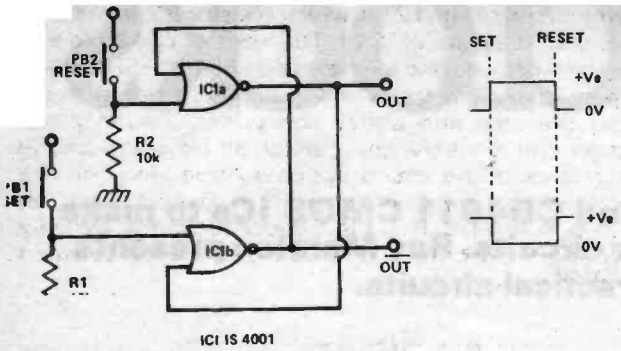


Fig. 4. Manually triggered NOR bistable.

NAND Bistable

Fig. 5 shows the CD4011 NAND gate version of the bistable circuit. This circuit is almost identical with that of Fig. 3, except for the positioning of R1 and R2. Note, however, that the NOR gate circuit needs positive-going trigger pulses, while the NAND circuit needs negative-going pulses, and that the set pulse is applied to IC1b in the NOR circuit, but to IC1a in the NAND circuit.

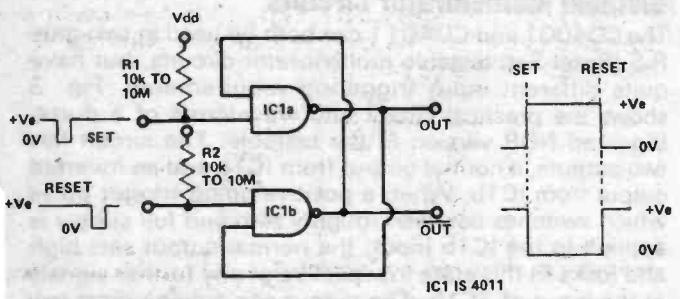


Fig. 5. A CD4011 NAND bistable, pulse triggered.

Manual NAND Bistable

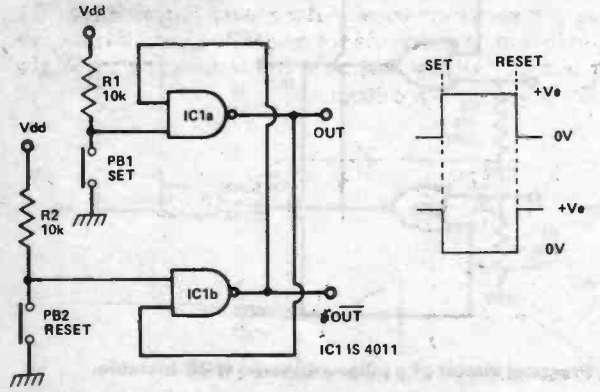


Fig. 6. Manually triggered NAND bistable.

Fig. 6 shows the manually-triggered version of the NAND-type bistable. Note here that although R1 and R2 are shown as having values of 10k, they can in fact have any resistance values from a few thousand ohms up to about 10M, depending on the precise details of the specific application. This versatility leads to the development of the touch-triggered NAND bistable circuit of Fig. 7, in which R1 and R2 have values of 10M, and the circuit can be triggered by placing any resistance that is significantly less than 10M (such as finger resistance) across the touch contacts. R3 and R4 are used in this circuit to protect the inputs of the two gates.

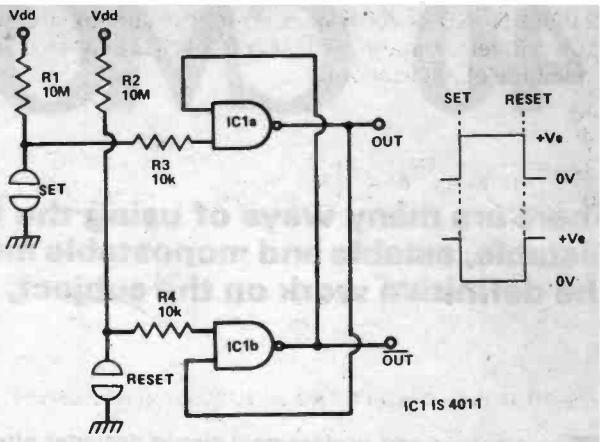
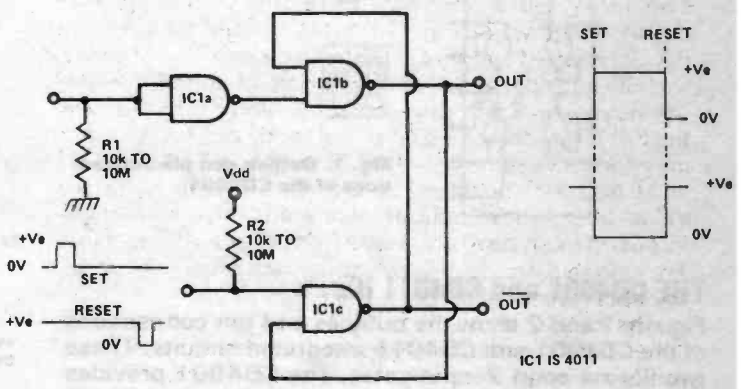


Fig. 7. Touch-triggered NAND bistable.

The bistable circuits that we have looked at so far all use same-polarity (either both positive or both negative) trigger signals. In some applications, however, it is necessary or convenient to use opposite-polarity signals to trigger the bistable, and this type of action can be obtained by placing an inverter stage in series with one or other of the normal bistable input terminals. Figs. 8 and 9 show two alternative circuits of this type.



Using opposite-polarity signals to trigger a 4011 bistable, Fig. 8 (above), and a 4001 bistable, Fig. 9 (below).

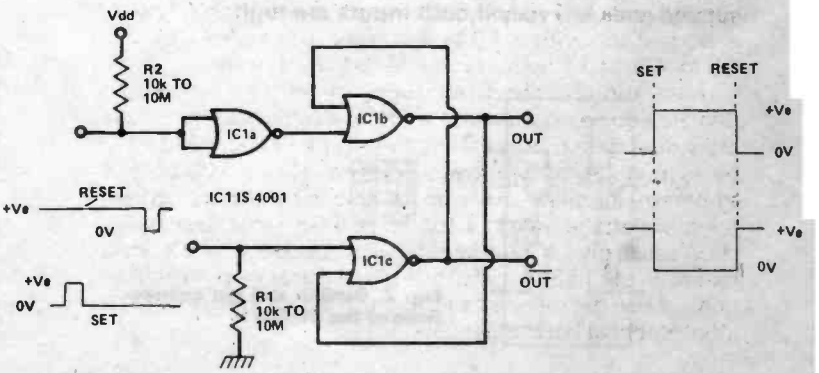


Fig. 10 shows alternative ways of connecting a 2-input NAND or NOR gate so that it acts as a simple pulse inverter stage. These circuits are useful in a multitude of applications.

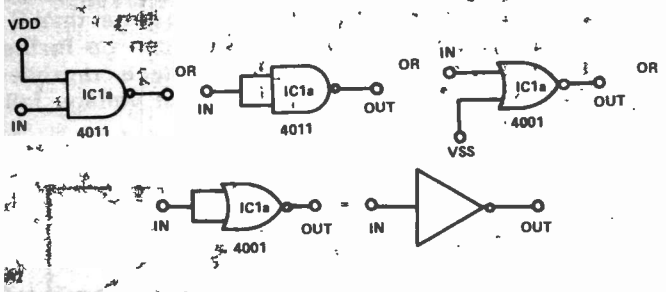


Fig. 10. Using a 2-input NAND or NOR gate as an inverter.

Basic 2-Gate Astable Circuits

The CD4001 and CD4011 can both be used in a variety of basic 2-gate astable multivibrator circuits. In these circuits the gates are connected as simple inverters, so the two types of IC give identical performances.

CMOS Astable

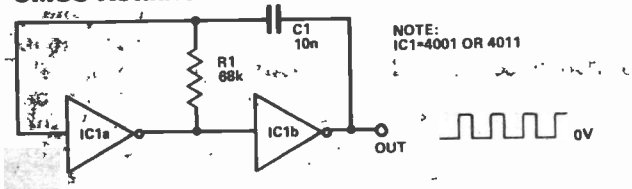


Fig. 11. Circuit of the basic 2-gate CMOS astable.

The most basic and useful 2-gate CMOS astable circuit is shown in Fig. 11. This circuit generates a decent square wave output, has excellent thermal stability and operates at about 1 kHz with the component values shown. The frequency is inversely proportional to the C-R time constant, so the frequency can be raised by lowering the values of either C1 or R1. In practice, C1 must be a non-polarized capacitor, and can have any value from a few tens of picofarads to a few microfarads. R1 can have any value from about 4k7 to 10M. For variable frequency operation, wire a fixed and a variable resistor in series in the R1 position.

The output of the Fig. 11 astable circuit switches (when lightly loaded) almost fully between the zero and positive supply voltage levels, but the junction of R1 and C1 is prevented from swinging below zero or above the positive rail levels by the built-in clamping diodes at the input of IC1a. This characteristic causes the operating frequency of the circuit to be somewhat dependent on supply rail voltages. As a rough rule of thumb, the frequency falls by about 0.08% for each 1% rise in supply voltage. Typically, if the frequency of this astable is normalised with a 10 volt supply, the frequency will fall by 4% at 15 volts, or rise by 8% at 5 volts.

Also, the operating frequency of the Fig. 11 circuit depends somewhat on the transfer voltage value of the individual gate that is used and can be expected to vary by as much as 10% between individual ICs. The output symmetry of the waveform is also dependent on the transfer voltage value of the IC and, in most cases, the circuit will give a non-symmetrical output. In the vast majority of 'hobby' and other non-precision applications, these deficiencies of the basic astable circuit are of little practical consequence.

Some can be minimised by using the 'compensated' astable circuit of Fig. 12, in which resistor R2 is wired in series with the input of IC1a. This resistor can have any value between two and ten times that of R1, and its main purpose is to allow the R1-C1 junction to swing freely below the zero and above the positive supply rail voltages during the switching action and thus reduce the dependance of the circuit operating frequency on the supply voltage. Typically, when R2 is given a value ten times greater than R1, the frequency varies by only about 0.5% when the supply voltage is varied between 5 and 15 volts.

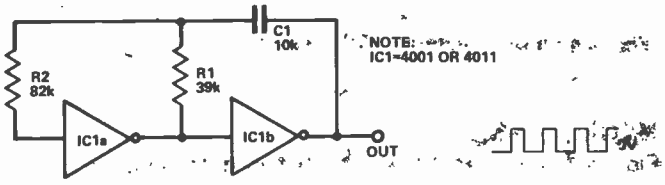


Fig. 12. A compensated astable circuit.

The basic and compensated astable circuits of figs. 11 and 12 can be built with a good number of detail variations. Some of these are shown in Figs. 13 to 18. In the basic astable circuit, for example, C1 alternately charges and discharges via R1. Figs. 13 to 15 show how the basic circuit can be modified to give alternate C1 charge and discharge paths.

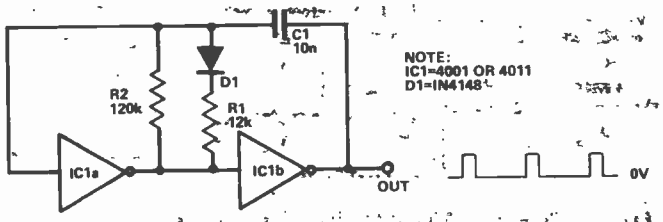


Fig. 13. Modifying the circuit to give C1 alternate charge and discharge paths and produce a non-symmetrical output waveform.

Fig. 13 shows one way of modifying the astable so that it gives a non-symmetrical output waveform. Here, C1 charges in one direction via R1 and R2 in parallel, to give a high output, but discharges in the reverse direction via R2 only, to give a low output.

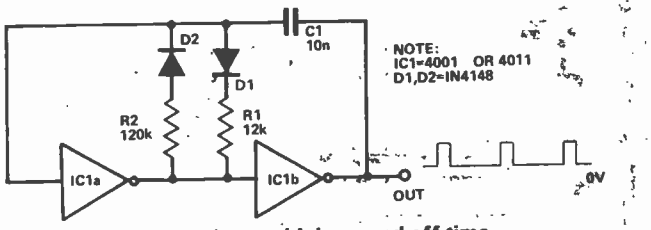


Fig. 14. Controlling the astable's on and off time.

On/Off Control

Fig. 14 shows how the circuit can be further modified by also wiring a diode in series with R2, so that the ON time of the output is controlled only by R1, and the OFF time is controlled only by R2. These two circuits can be made to give variable outputs by replacing either or both of their timing resistors with a fixed and a variable resistor in series.

Variable Symmetry

Fig. 15 shows how the astable can be modified to give a variable symmetry or M/S-ratio output, while maintaining a near-constant frequency. C1 in this circuit charges in one direction via D1-R2 and one half of RV1 and in the other direction via D2-R1 and the other half of RV1. The M/S-ratio can be varied over the range 1:10 to 10:1 via RV1.

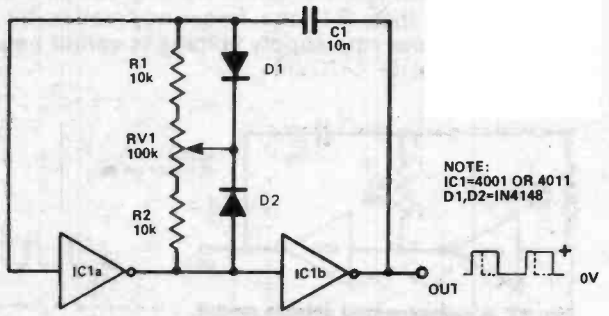


Fig. 15. Controlling the mark/space ratio.

Fig. 16 shows the circuit of a multi-tone push-button activated astable. Normally, when all push-button switches are open, R5 holds the input of IC1a (and thus the output of IC1b) low. Resistors R1 to R4 all have values that are low relative to R5, so the circuit acts as a normal astable when any one of the push-button switches is closed. This circuit can be used in multi-tone musical instruments and gadgets, etc. and has the major advantage that it draws negligible current when in the standby mode. There is no limit to the number of push-button switches that can be used with the circuit.

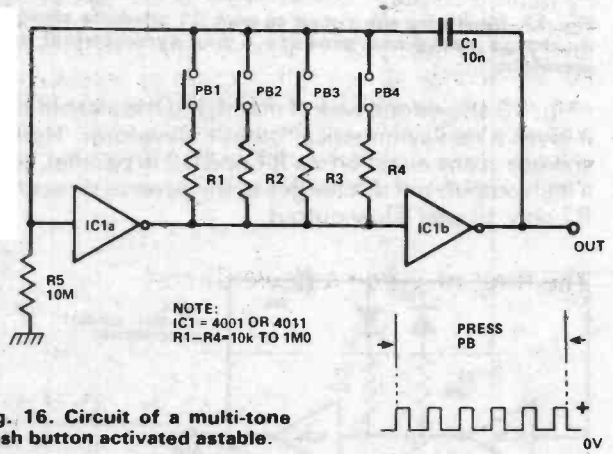


Fig. 16. Circuit of a multi-tone push button activated astable.

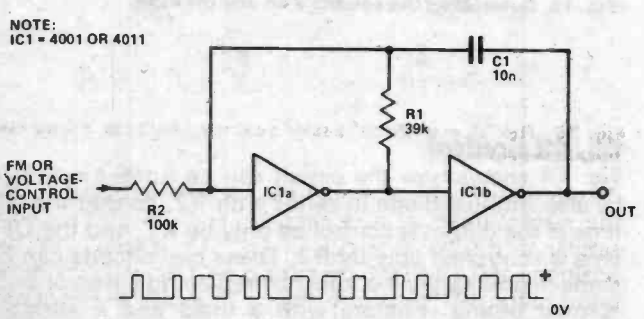


Fig. 17. Frequency modulation of an astable.

Frequency Modulation

Fig. 17 shows how the astable can be subjected to frequency modulation or voltage control of frequency by simply feeding the FM or voltage-control signal to the input of IC1a via a resistance that is much larger than R1 and Fig. 18 shows how the circuit can be further modified to act as a special-effect voltage-controlled oscillator that shuts off when the input voltage falls below a pre-set value.

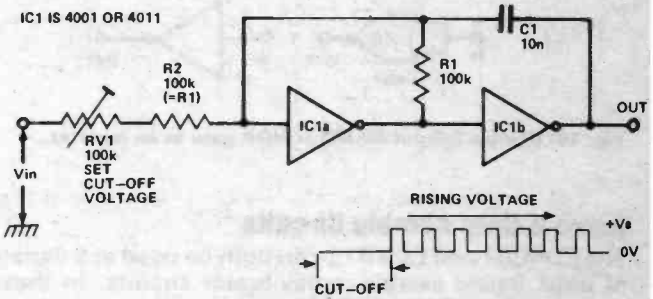


Fig. 18. Using an astable as a voltage-controlled oscillator with an output cut-off.

Gated 2-Gate Astable Circuits

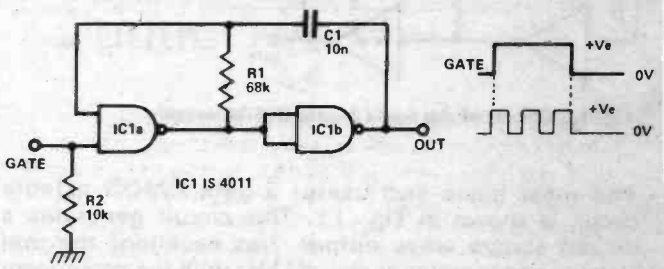


Fig. 19. A NAND astable with a normally-low output, gated by a high input signal.

All of the astable circuits of Figs. 11 to 15 can be modified for gated operation, so that they can be turned on and off via an external signal, by simply using a 2-input NAND or NOR gate in place of the inverter in the IC1a position and applying the input control signal to one of the gate input terminals. The CD4001 and CD4011 ICs can both be used in this type of application, but give quite different types of gate control and output operation. Figs. 19 and 20 show the two basic versions of the gated astable circuit.

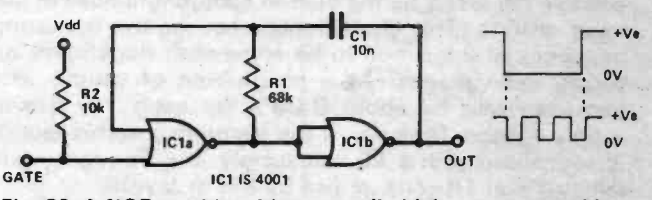
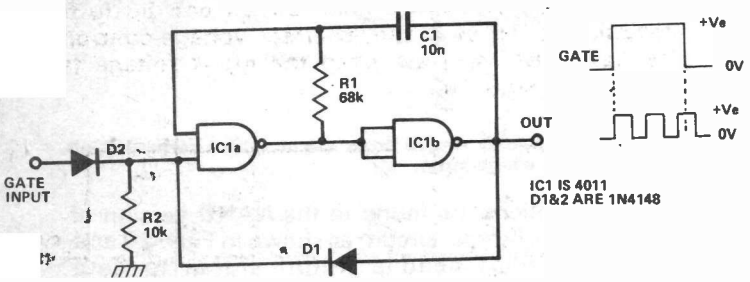


Fig. 20. A NOR astable with a normally-high output, gated by a low input signal.

Note that the Fig. 19 NAND astable circuit has a normally-low output and is gated by a high input signal, while the fig. 20 NOR astable has a normally-high output and is gated by a low input signal. Also note that, although R2 is shown in the diagram as having a value of 10k, R2 can in fact have any value in the range 10k to 10M and can be omitted altogether if the gate signal is applied from a preceeding logic state.

Note in the Fig. 19 and 20 circuits that the output signal terminates immediately the input gate signal is removed. Consequently, any noise present at the gate terminals of these circuits also appears at their outputs.



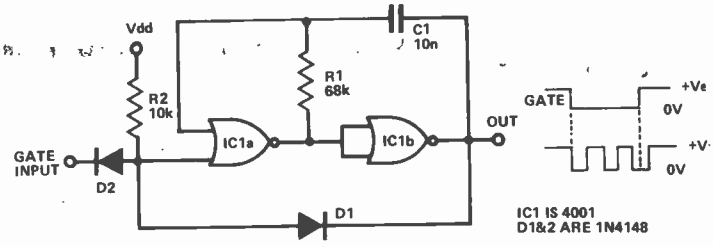


Fig. 21 (above) and Fig. 22 (below) overcome the problem of noise appearing at the gate terminals.

Figs. 21 and 22 show how the circuits can be modified to overcome this defect. Here, the gate signal of IC1a is derived from both the outside world and from the output of IC1b via diode OR gate D1-D2-R2. As soon as the circuit is gated from the outside world via D2 the output of IC1b reinforces the gating via D1 for the duration of one half astable cycle, thus eliminating any effects of a noisy outside world signal. The outputs of the circuits are complete numbers of half cycles. Note that R2 is an essential part of these circuits.

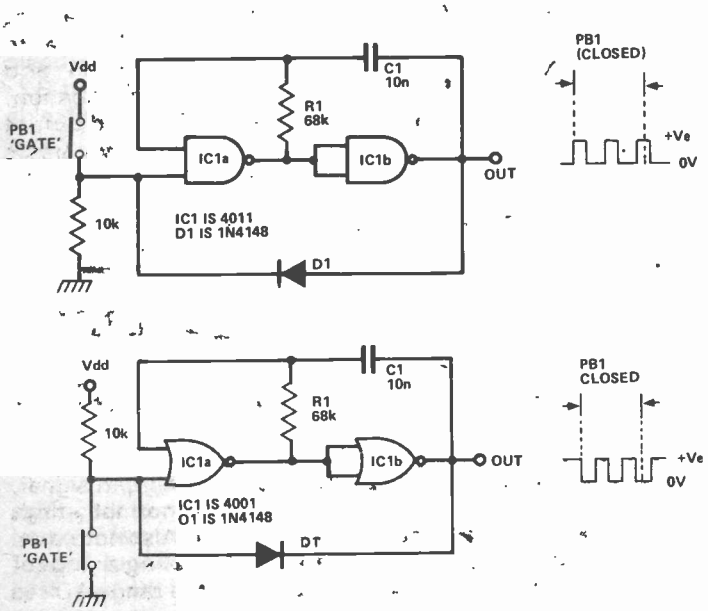


Fig. 23 (top) and Fig. 24 (above) show manually-triggered astables with noise-elimination networks.

Figs. 23 and 24 show manually-triggered versions of the Fig. 21 and 22 circuits. These circuits are of particular value when they are used as low speed clock generators, operating at about 5 Hz: when PB1 is briefly stabbed, the generate a single clean clock pulse: when PB1 is held down, they generate five clean clock pulses per second.

Clock Generator Circuits

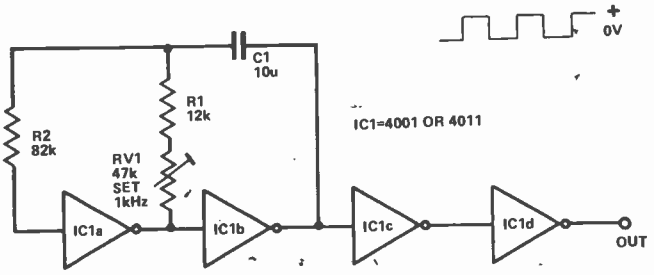


Fig. 25. Speeding up the rise and fall times of the astable output to produce clean clock signals.

The 2-gate astable circuit is generally not suitable for direct use as a clock generator with fast-acting counting and dividing circuits. Such circuits require the use of clean clock signals, with fast rise and/or fall times. The problem is that 2-gate astables designed around 'A' series or non-buffered CMOS produce clock outputs with rather slow rise and fall times, whereas 2-gate astables designed around buffered-output 'B' series CMOS produce outputs with good rise and fall times, but tend to produce 'dirty' clocking if there is the slightest trace of noice on their power supply lines.

Fortunately, these problems can easily be overcome by wiring a couple of inverter-connected gate stages in series with the output of the astable circuit, as shown in the example of Fig. 25. These inverter stages speed up the rise and fall times of the astable output waveform and also produce effective level shifting between the output of the astable and the clock input terminal of any external device, thereby reducing or eliminating the effects of noise on the clock circuit.

The Ring-of-Three Astable Circuit

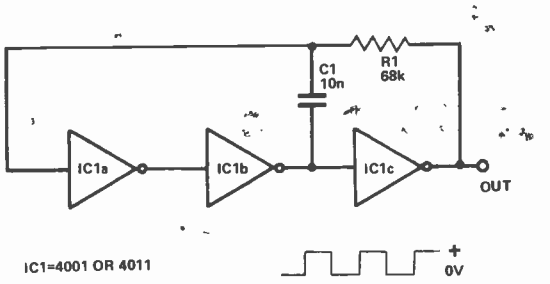


Fig. 26. The 'ring of three' astable circuit produces a very clean output waveform.

An alternative way of making a clock generator is to use the 'ring-of-three' astable circuit of Fig. 26. This circuit is similar to the basic circuit of Fig. 11, except that the positions of R1 and C1 are transposed, and the inverting input stage (IC1a) of the Fig. 11 circuit is effectively replaced by an ultra-high-gain non-inverting stage (comprising IC1a and IC1b in series) in the Fig. 26

circuit. Because of the very high gain of its composite input stage, the Fig. 26 'ring-of-three' circuit produces a very clean output waveform, with excellent rise and fall times, and is directly suitable for use as a clock generator.

The 'ring-of-three' astable circuit can be subjected to all of the basic design variations shown for the 2-gate astable. For example, C1 alternatively charges and discharges via R1 in the same way as in the Fig. 11 circuit, so the circuit can be subjected to all of the variations shown in Figs. 13 to 15. It can be designed in either basic or 'compensated' versions, etc.

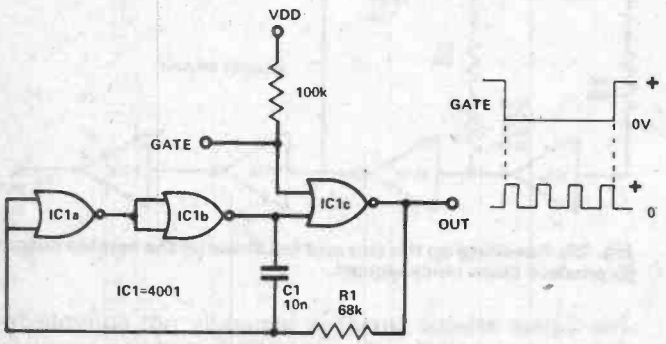


Fig. 27. A gated NOR 'ring of three' circuit with a normally low output, gated by a low input.

The 'ring-of-three' circuit offers interesting possibilities when it is used in the gated mode, because it can be gated on and off via either its IC1b or IC1c stages. Figures 27 to 30 show four variations on this theme.

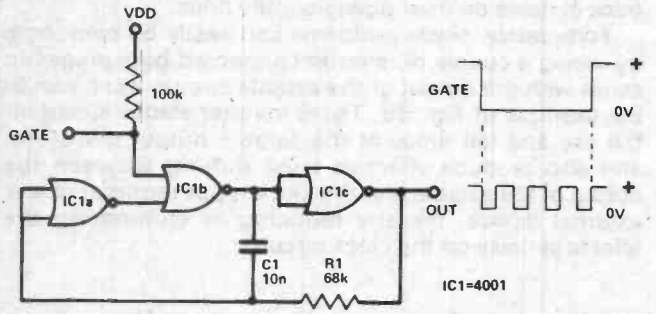


Fig. 28. A gated NOR 'ring of three' circuit with a normally high output, gated by a low input.

Figs. 27 and 28 show alternative versions of the gated NOR-type 'ring-of-three' circuit. Both circuits need a 'low' signal to gate the astable on. Note that the output of the circuit is normally-low if the gate signal is applied to IC1c, or is normally-high if the gate signal is applied to IC1b.

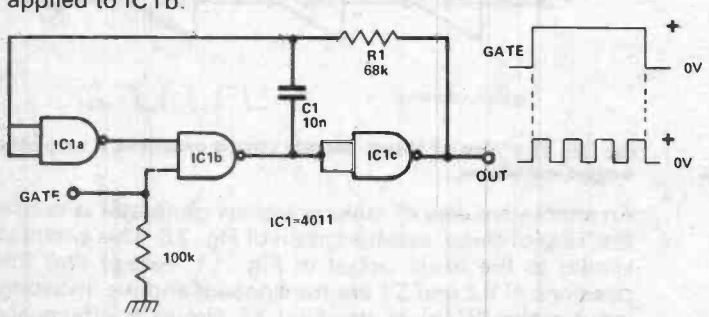


Fig. 29. A gated NAND 'ring of three' circuit with a normally low output, gated by a high input.

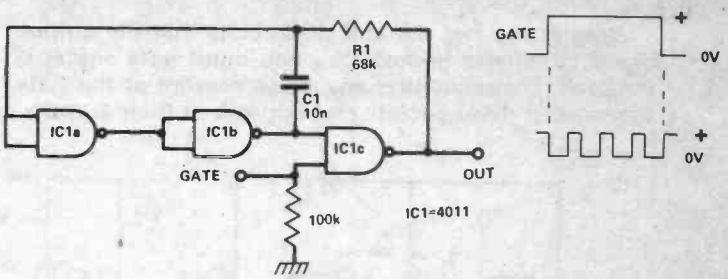
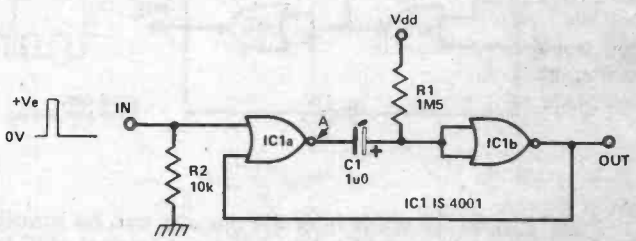


Fig. 30. A gated NAND 'ring of three' circuit with a normally high output, gated by a high input.

Similar variations are found in the NAND version of the gated 'ring-of-three' circuit, as shown in Figs. 29 and 30. These circuit need a 'high' signal to gate them on, and have a normally-low output if the gate signal is fed to IC1b, or a normally-high output if the gate signal is fed to IC1c.

Monostable Multivibrator Circuits



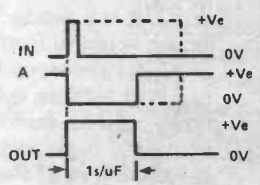


Fig. 31. A 2-gate NOR monostable multivibrator.

The CD4001 and CD4011 can both be used to make an exceptionally useful type of 2-gate monostable multivibrator or pulse generator circuit. The two basic versions of this circuit are shown in Figs. 31 and 32. In these circuits the duration of the output pulse is determined by the values of R1 and C1, and approximates one second per microfarad of C1 value when R1 has a value of 1M5. In practice, C1 can have any value from roughly 100 p to a few thousand u, and R1 can have any value from about 4k7 to 10M.

One outstanding feature of these circuits is that the input trigger pulse or signal can be direct coupled and has no appreciable effect on the length of the circuit's output pulse: the trigger pulse can be shorter or longer than the output pulse. The NOR version of the circuit has a normally-low output, and is triggered by a positive-going input pulse, while the NAND version of the circuit has a normally-high output and is triggered by a negative-going input pulse.

A signal feature of these circuits is that the pulse signal appearing at point "A" has a length that is equal to that of either the output pulse or the input trigger pulse, depending on which is the greater of the two. This feature is of value when making pulse-length comparators and over-speed alarms, etc.

The Fig. 31 and 32 circuits have only two significant defects. One of these is that the pulse length depends somewhat on the transfer voltage value of the individual IC that is used in the circuit. The other is that the pulse length also depends somewhat on the supply voltage value that is used with the circuit, just as the operating frequency of the basic 2-gate CMOS astable varies slightly with the supply voltage value. These defects are of little consequence in most practical applications, however.

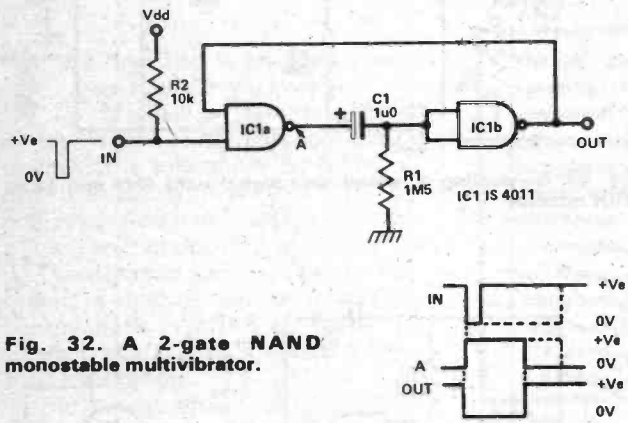


Fig. 32. A 2-gate NAND monostable multivibrator.

If a number of the Fig. 31 and 32 circuits are to be interconnected to give cascaded delays (as in a delayed-pulse generator, for example), an inverter stage must be interposed between the outputs and inputs of successive monostables, to give correct-polarity trigger signals. Figure 33 shows the basic system.

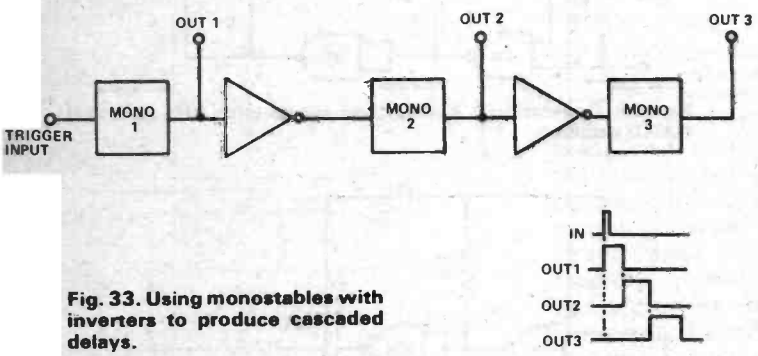


Fig. 33. Using monostables with inverters to produce cascaded delays.

Alarm Call Sound Generator Circuits

A single CD4001 or CD4011 IC and one or more transistors can readily be used to make a variety of types of very useful alarm call sound generator circuits. Figs. 34 to 41 show some practical circuits of this type. In all cases, the circuits can be powered from any supply in the range 5V to 15V and can be used with any speaker in the range 3R to 100R. Output powers range from tens to hundreds of milliwatts, depending on speaker impedances and supply rail voltages used, but can readily be boosted to tens of watts by using additional transistor power-boosting stages.

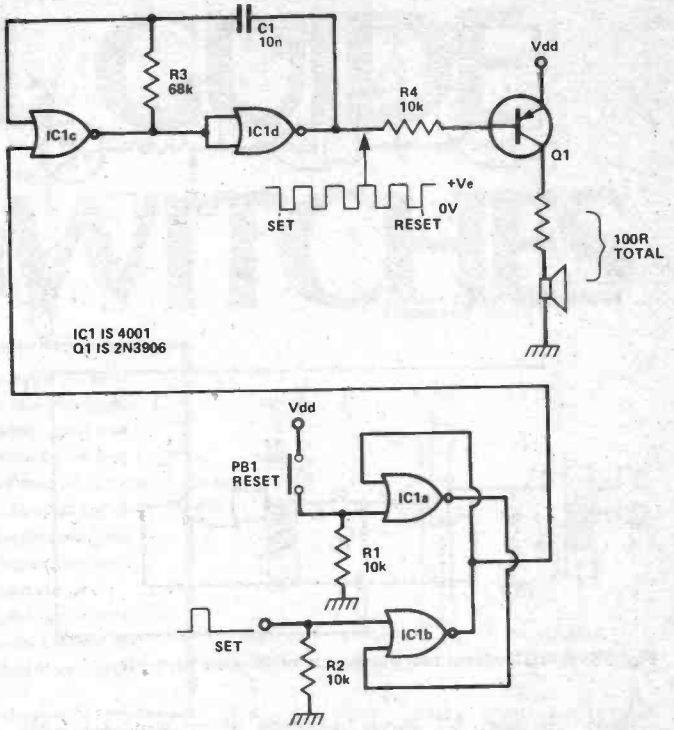


Fig. 34. Circuit of a NOR latching monotone alarm call generator.

Figs. 34 and 35 show two versions of a latching monotone alarm call generator. IC1a and IC1b are wired as a bistable multivibrator and when a trigger pulse is applied to the circuit the IC1a-IC1b bistable self-latches and switches on the IC1c-IC1d-1kHz astable tone generator. The circuit can be reset to the OFF state by momentarily closing PB1.

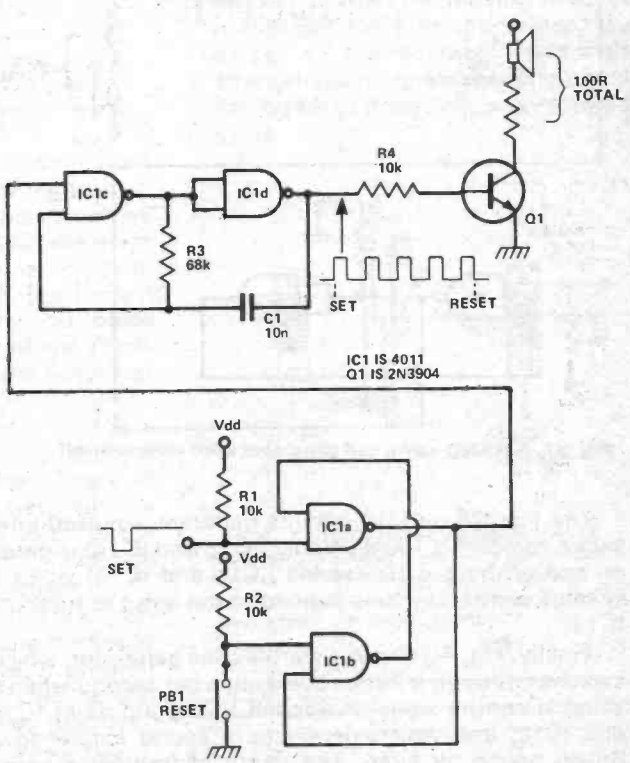


Fig. 35. Circuit of a NAND latching monotone alarm call generator.

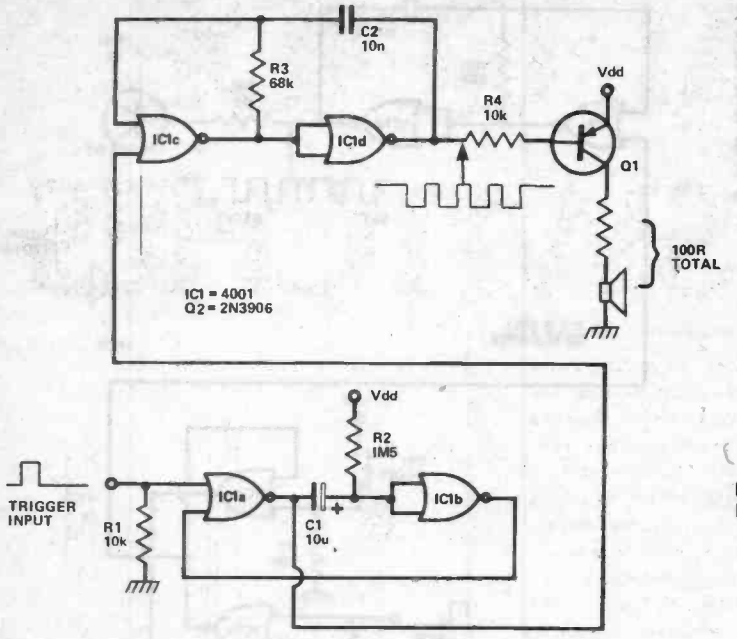


Fig. 36. A NOR alarm call generator with auto turn-off.

Figs. 36 and 37 show versions of an auto-turn-off monotone alarm call generator. IC1a and IC1b are wired as a monostable multivibrator, which turns on the IC1c-IC1d astable for about 10 seconds each time that it is triggered.

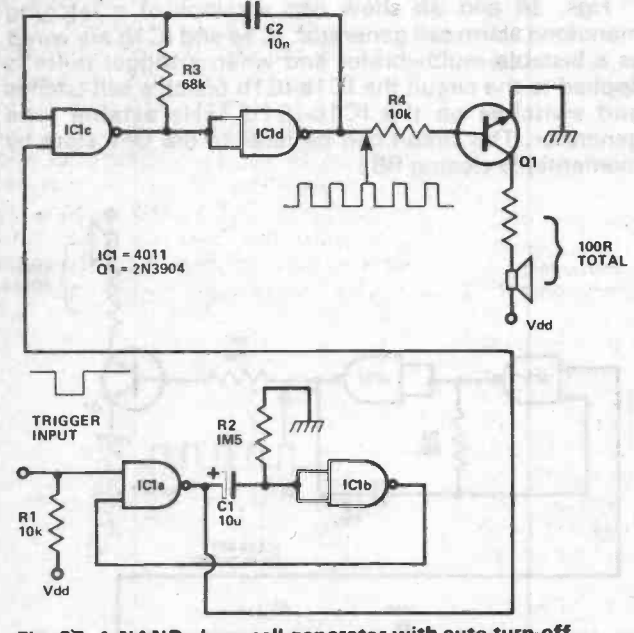


Fig. 37. A NAND alarm call generator with auto turn-off.

The Fig. 38 and 39 circuits generate a pulsed-tone signal, in which a 1 kHz astable (IC1c and IC1d) is gated on and off by a 6 Hz astable (IC1a and IC1b) when a suitable control signal is applied to the input terminal of IC1a.

Finally, Fig. 40 shows a warble-tone generator, which switches through a 2-tone cycle once per second when a suitable control signal is applied to the inputs of IC1a and IC1c, and which generates a sound similar to a British police car siren. The depth of frequency variation of the circuit is determined by R3, which can have any value in the approximate range 120k to 1MO.

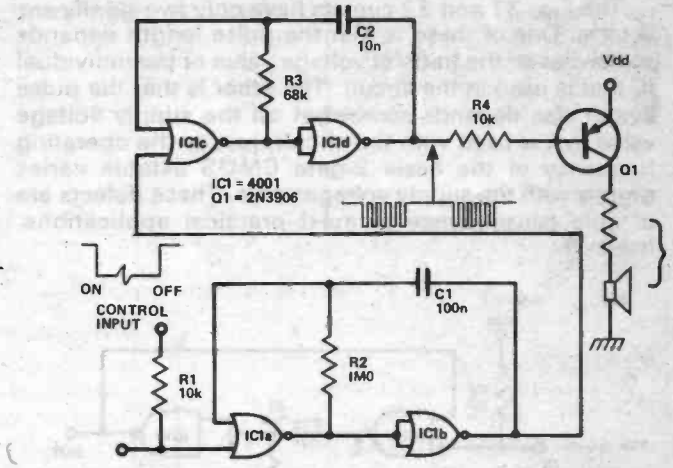


Fig. 38. Generating a pulsed-tone signal with 6Hz and 1kHz NOR astables.

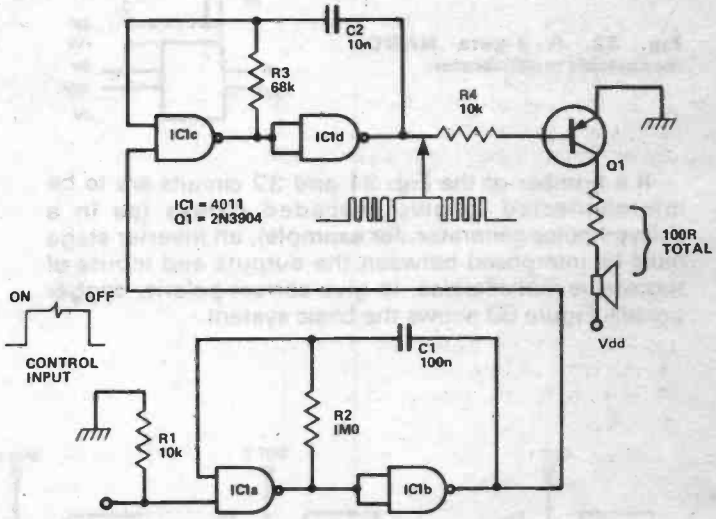


Fig. 39. Generating a pulsed-tone signal with 6Hz and 1kHz NAND astables.

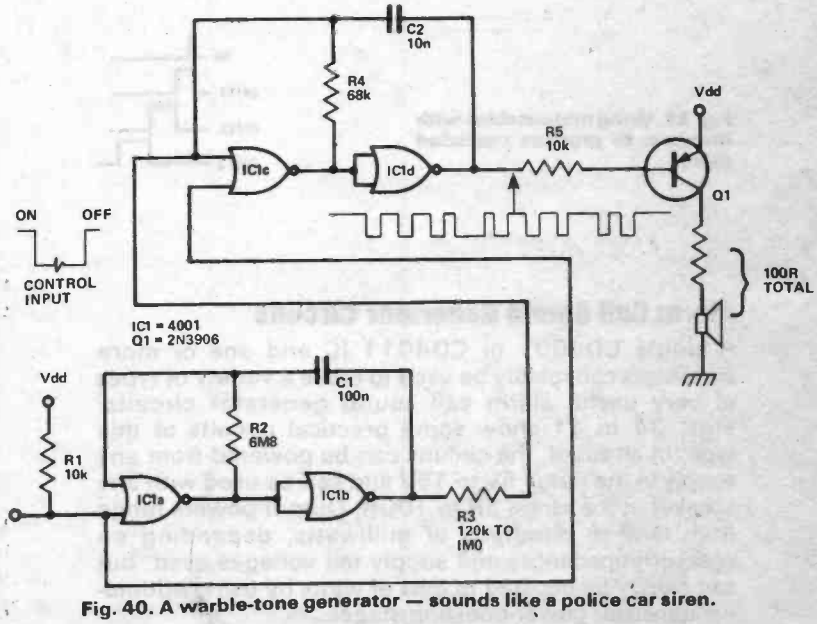


Fig. 40. A warble-tone generator — sounds like a police car siren.

PRACTICAL GUIDE TO REED SWITCHES

The reed switch is functional and versatile. It is almost the simplest elemental form of switch and has innumerable applications — from straightforward functions in which switch actuation is initiated by the proximity of a permanent magnet — to complex logic and computing functions, using hundreds of electromagnetically driven reeds. The practical three-part series, by Collyn Rivers, explains how and why they are used.

The dry reed is an almost perfect low-current switch.

It is fast — operating times of less than one millisecond are typical. It is reliable — as many as one billion operations can be achieved. And it is cheap — quantity price is well under 25p.

The dry reed switch is not by any means a new device for it was invented back in 1945 by Dr W. B. Ellwood of the USA's Western Electric Corporation.

But it was ahead of its time. It remained practically unnoticed by the engineering world until a decade ago when it was 'rediscovered' by the telephone industry.

And since then reed switches are receiving interest and acceptance at an ever increasing rate.

In its basic form, a reed switch is a magneto-mechanical relay. In other words it relies upon a magnetic force to initiate a mechanical switching action.

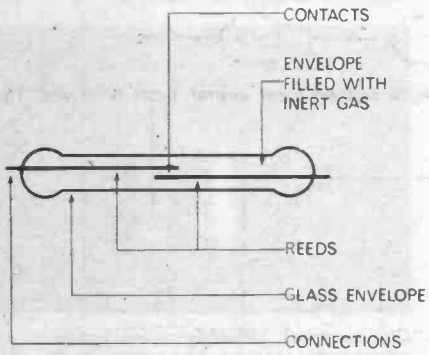


Fig. 1. The basic reed switch.

THE BASIC SWITCH

A typical reed switch is shown in Fig. 1. It consists of two flattened ferromagnetic reeds sealed in a glass tube. The reeds are fixed, one at each end of the tube, so that their free ends overlap in the centre but with a 0.01" gap between them.

During the sealing operation the air inside the tube is pumped out and replaced by dry nitrogen so that the contacts operate in an inert atmosphere.

When the reed switch is brought within the influence of a magnetic field (either from a coil or a magnet) the reeds — being ferromagnetic — become a flux-carrying portion of the magnetic circuit. The extreme ends of the reeds will assume opposite magnetic polarity, and if sufficient flux is present, the attraction forces overcome the stiffness of the reeds and they flex towards each other and touch.

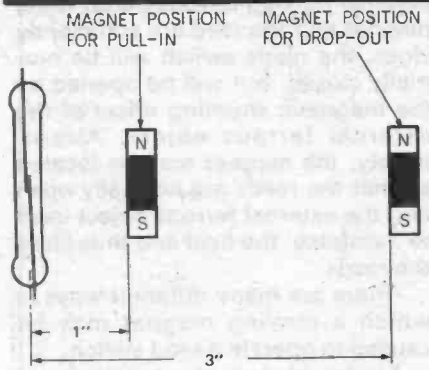


Fig. 2. The reeds close when the magnet is brought within one inch, and will remain closed until the magnet has been moved at least three inches away.

When the magnetic field is removed the reeds spring back to their original positions. There is however a difference between the value of field required to close the reeds, and the reduced value that will allow them to open again.

A typical example of this is shown in Fig. 2. In this example the reeds close when the magnet is brought within one inch, but they will remain closed until the magnet has been moved about three inches away.

This phenomena — which is caused by magnetic hysteresis in the reeds — can be considerably reduced by introducing a second magnet, of opposite polarity, on the further side of the switch. This is illustrated in Fig. 3. The fixed magnet must not be mounted within the normal pull-in position for single magnet operation, otherwise the reed switch will be held in a closed position by the second magnet and will open when the moving magnet is brought close to the switch. By selecting the correct types and strengths of magnets the differential can be set to practically any required value.

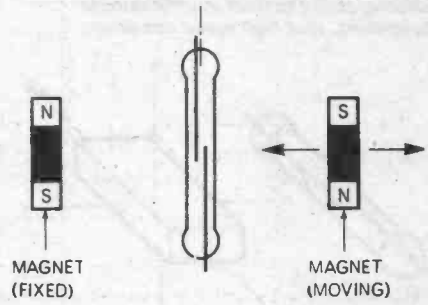


Fig. 3. A fixed magnet of opposite polarity to the moving magnet may be used to reduce pull-in, pull-out differential.

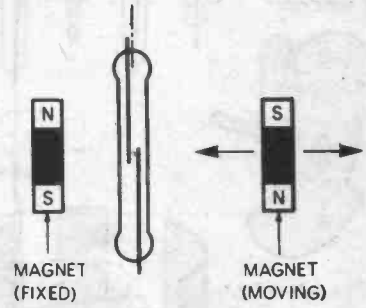
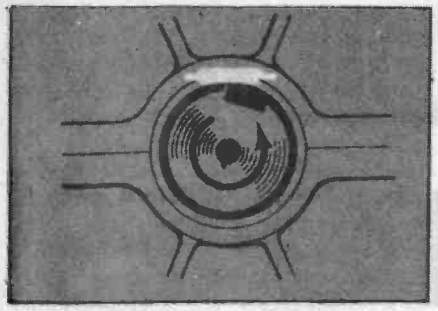


Fig. 4. 'Normally closed' operation can be obtained by biasing a 'normally open' reed switch with a fixed magnet. The moving magnet cancels out the fixed magnet and thus allows the switch to open.

Fig. 5. This type of reed switch may be used for either change-over, or normally closed operation.



Tachometer applications, requiring the simplest addition to the moving part and offering ability to work in unfavourable conditions, plus high speed operation.

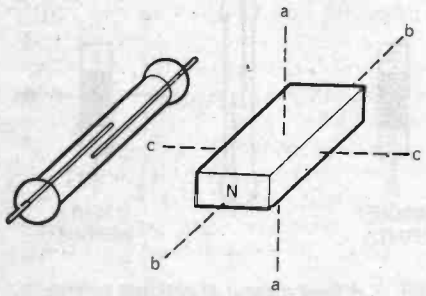


Fig. 6. Linear planes of operation; movement of the magnet in any of the planes indicated may be used to actuate the switch.

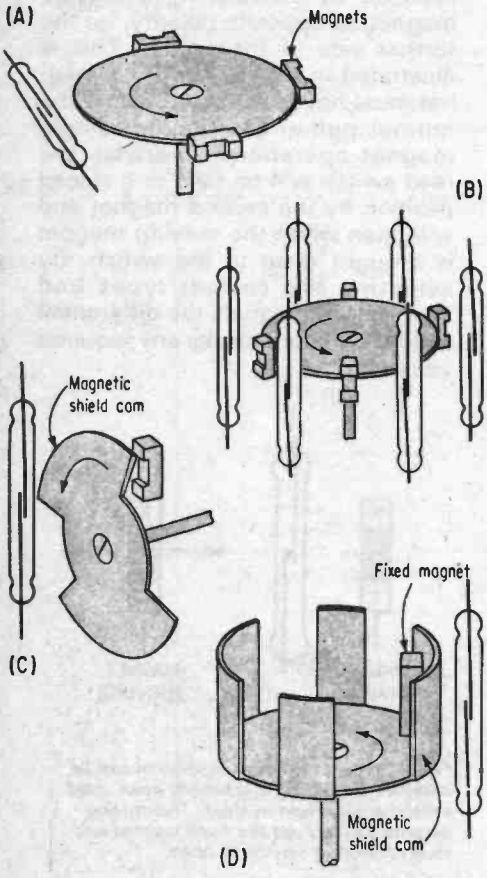


Fig. 7. Rotary motion may also be used to actuate a reed switch. In A and B the switches are stationary and the magnets rotate. In examples C and D both the switches and the magnets are stationary and the switch operates whenever the cutout portion of the magnetic shield is between magnet and switch.

OPERATING MODES

As can clearly be seen in Fig. 1, the reed switch is 'normally open'. The reeds close when a magnet is brought close to the switch enclosure.

However there are many applications where the switch is required to be 'normally closed' and to open when the magnet is introduced. This can be done either by biasing the switch with a second magnet (as shown in Fig. 4), or by using a reed switch with change-over contacts (Fig. 5).

In most applications where a reed switch is opened or closed by a permanent magnet, the magnet is fitted to a moving part, and the reed is fitted to a stationary part.

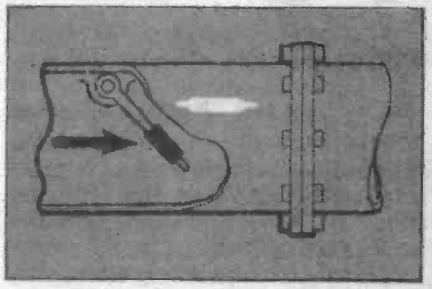
There are, however, a number of applications in which both the magnet and the reed must be located on a stationary component. Operation may then be effected through distortion of the magnetic field by an external moving ferrous mass. If the magnet and the reed are sufficiently close, the reeds switch will be normally closed, but will be opened by the magnetic shunting effect of the external ferrous object. Alternatively, the magnet may be located so that the reeds are normally open and the external ferrous object used to 'reinforce' the field and thus close the reeds.

There are many different ways in which a moving magnet may be caused to operate a reed switch.

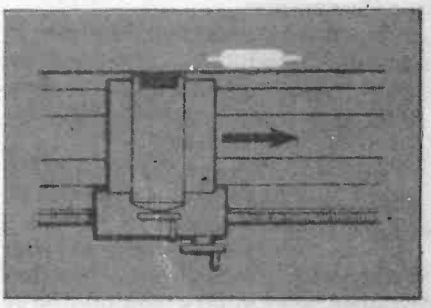
Linear planes of operation are shown in Fig. 6; movement of the magnet in any of the planes a-a, b-b, and c-c will operate the switch. Magnet selection is fairly ciritical if the switch is operated in mode b-b, spurious operation may be caused by negative peaks on the magnet's field pattern curve. If these are large, the reeds will pull-in three times as the magnet is moved from one end of the switch to the other.

Rotary motion may also be used. Various ways of achieving this are shown in Fig. 7. (A most versatile and simple impulse generator can be put together in a few minutes by placing one or more magnets on a gramophone turntable and fastening a reed switch to the motor base board (Fig. 8). Switching rates from approx one every two seconds to well over 2,000 a minute can be selected merely by changing the turntable speed and/or using more magnets!)

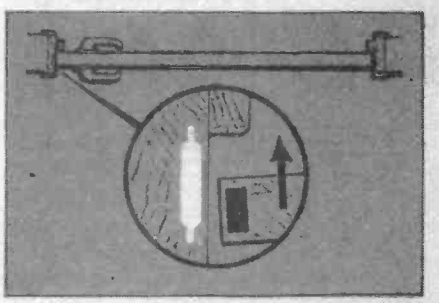
Since the reed switch is truly a



Flow control and indication, minimising restraint on the moving part and avoiding perforation of the container wall.



Position control and indication, obviating mechanical contact with its implications of wear, and simplifying mounting.



Door switches, obviating mounting and adjustment problems, and offering total concealment for security devices.

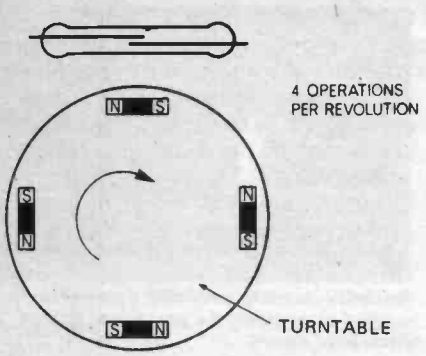
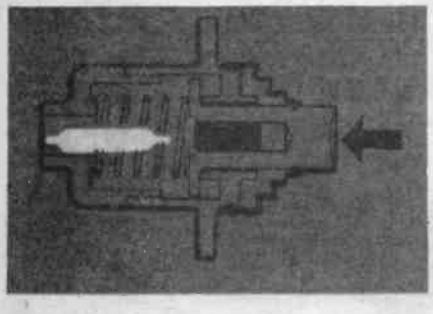


Fig. 8. Simple yet versatile impulse timer can be improvised by placing one or more magnets on a gramophone turntable.

sealed device, it can be used in applications where conventional switches are not permitted, or where they have very limited life. Reed switches are frequently used in simple on/off push buttons, and outdoors, in dusty areas such as cement plants, especially in areas where explosive gases may be present.

OPERATING LIFE

The operating life and load carrying characteristics of reed switches are interrelated. A switch may operate for 100 million or even 1,000 million closures providing it is switching very low currents. But the same type of switch may fail after half a dozen switching cycles if the load greatly exceeds the designed rating. The majority of reed switches are manufactured with contact ratings between 0.1A and 3.0A.



Switching in explosive atmosphere, obviating ignition risk; in dust filled atmospheres where conventional contacts would be unreliable; and in extremely cold conditions were ordinary switches would freeze up. In radioactive environments, magnetic operation can maintain integrity of shielding.

The current handling capacity of reed switches varies from type to type. In general the rating will be determined by the size and surface plating of the reeds, for the reed is an electrical conductor, and current rating will be a function of contact area.

The maximum rated contact loading is only applicable for purely resistive loads. If the load is capacitive or inductive the switch must either be drastically derated, or the switch contacts protected in a suitable fashion.

Four suitable methods of contact protection are shown in Fig. 9.

In dc circuits all that may be required is a resistor shunted across the load (Fig. 9A). Where the load is a relay coil or operating solenoid a resistor of approximately eight times the coil resistance is adequate to absorb a major portion of the induced energy when the circuit is interrupted. The addition of the resistor will of course increase the steady-state current flow but this extra load is negligible.

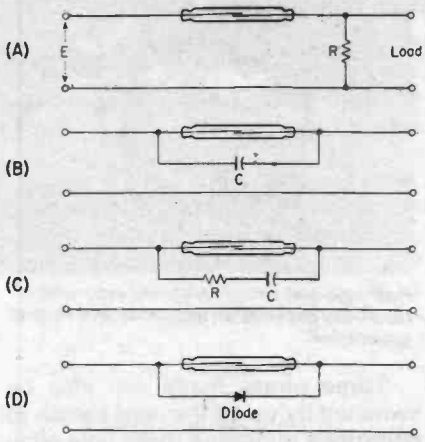


Fig. 9. Contact protection techniques: A — Resistor shunting load. B — Capacitor shunting contact. C — Resistor-capacitor series network for ac loads. D — Diode shunting.

Another cheap and simple way to protect the reed switch is to wire a capacitor across the contacts. The required value depends upon load current, but something between 0.1 uf and 1.0 uf will be sufficient. (Fig. 9B).

The most generally used method of protection is the resistor-capacitor series network shown in Fig. 9C. This circuit must be used if the switched load current is ac. The resistor should be approximately 160 ohms and the capacitor somewhere between 0.1 uf and 1.0 uf. That this is an extremely effective method was proven by a recent trial during which a motor starter was switched 50 million times without failure.

The component values may either be determined empirically (as described below) or mathematically. In the latter case, the component values can be obtained from —

$$C=\frac{I^2}{10}\mu F,\ R=\frac{E}{10\times I(1+50/E)}\ \Omega$$

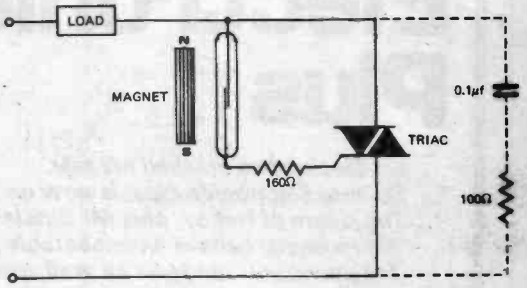
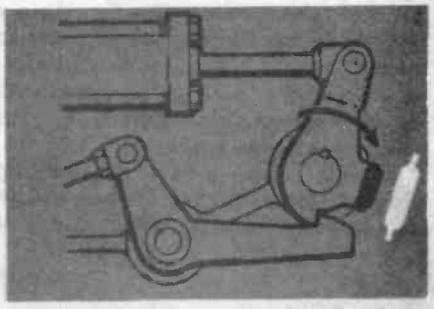


Fig. 10. Reed switch / Triac combination may be used to switch single phase loads as high as 125 Amps. Components shown in dotted lines must be included if the load is reactive.

SPECIFICATIONS	STANDARD	MINIATURE
Maximum voltage	150 Vdc 250 Vac	50 Vdc 150 Vac
Maximum current	2.0A	0.5A
Maximum power	25W	6W
Max. initial resistance	50 m.ohms	100 m.ohms
Max. end-of-life resistance	2 ohms	2 ohms
Peak breakdown voltage	500V	300 V
Closure rate	400 Hz	2000 Hz
Insulation resistance	5000 M.ohms	1000 M.ohms
Temperature range	—55°C to +150°C	—55°C to +150°C
Contact capacitance	1.5 pF	0.5 pF
Vibration	10G at 10-55Hz	10G at 10-55Hz
Shock	15G minimum	15G minimum
Life at rated load	5×10^6 operations	5×10^6 operations
Life at zero load	500×10^6 operations	500×10^6 operations

Table 1. Typical specifications for standard and miniature reed switches.



Safety interlock switching, giving extreme reliability and simplicity of application to complex mechanical layouts. Reed insert completes circuit to illuminate warning lamp or permit further stage of operation.

in pocket calculators. Non-volatile memories are the types using pre-set registers (such as read-only memories or ROMs) or which use magnetic tapes or cores or other types of storage which are not erased when power is switched off. A simple type of volatile memory is a SISO shift register with its output connected back to its input so that the information is read back in after one complete set of clock pulses; this type of memory can only deliver its contents in the order in which they are stored. If the register has parallel outputs with gates, however, it becomes possible to find which digit (0 to 1) is stored in each flip-flop, so that, in the language of computing, random access is possible. This is a simple random access memory (RAM).

At this point it is worth pointing out that most memories in general use permit random access. The type of memories which we refer to as RAM are random access memories which can be written as well as read when suitable inputs are applied. They should properly be called random access read/write memories. Read only memories are usually also random access, but the information which is stored has been put there either by the manufacturer (in the design stage) or by the user (as with PROM) when the memory is first used. In the older types of PROM, using fusible links, the memory cannot be altered once programmed, except by fusing a few more links. The more modern UV erasable PROM's permit complete erasure and re-programming.

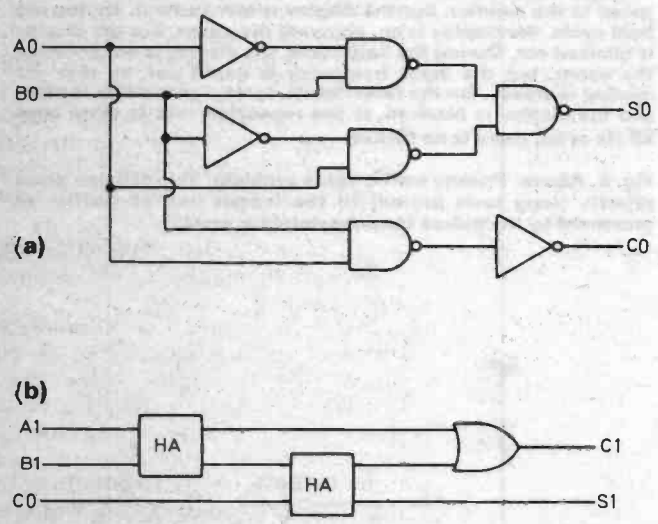


Fig. 3. Above: Adders (a) Half-adder circuit, using NAND-gates and inverters. (b) Full adder, using half adders and OR-gate.

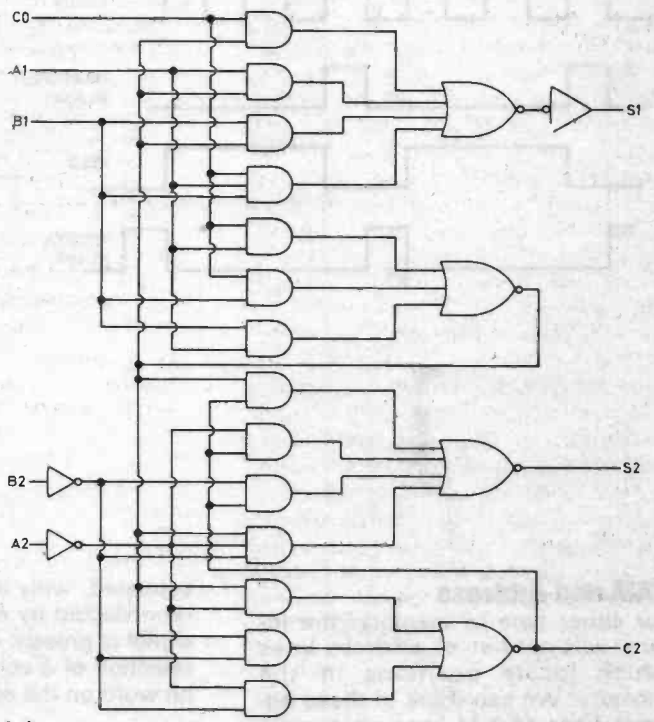


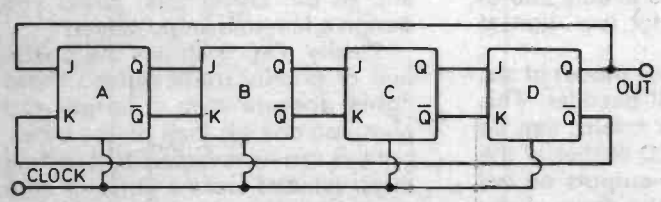
Fig. 4. Right: (a) Schematic of 7482 two-bit full adder. Note again the advantages of medium scale integration. (b) Truth table.

TRUTH TABLE

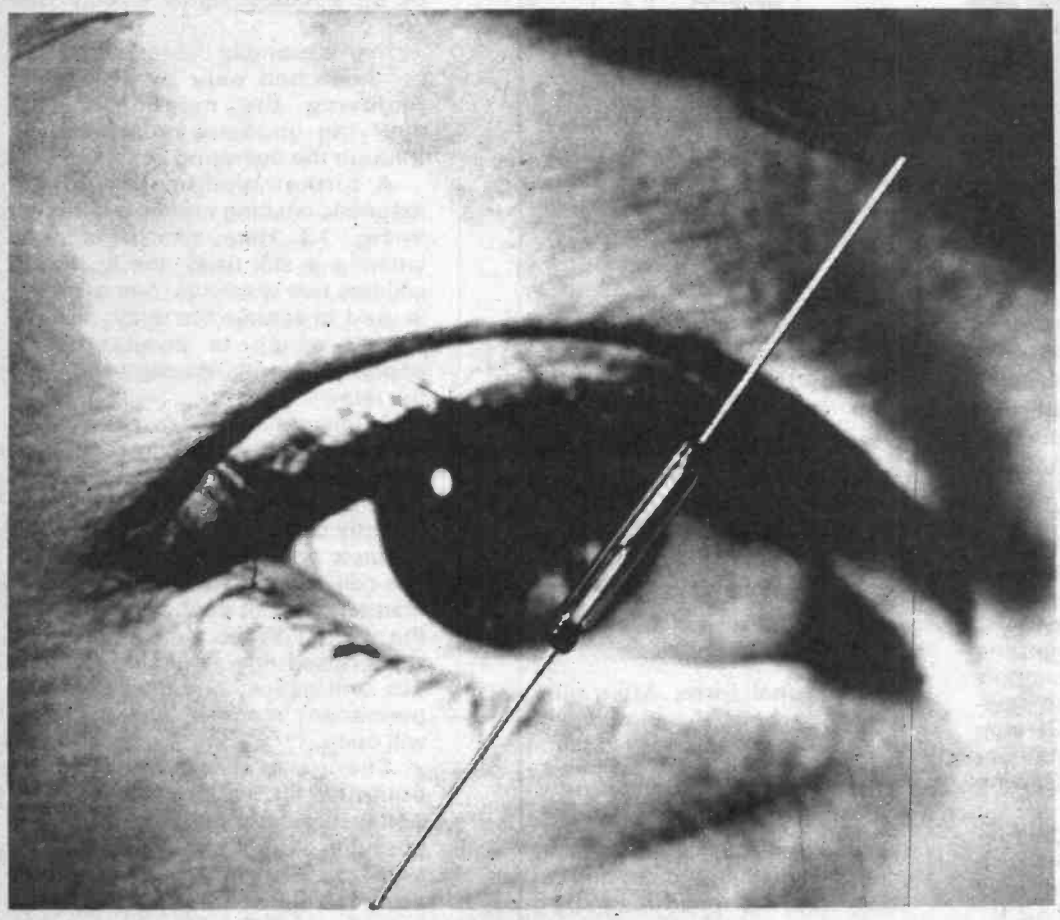
(b)

INPUTS				OUTPUTS					
				C0 = 0			C0 = 1		
A1	B1	A2	B2	S1	S2	C2	S1	S2	C2
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	0	1	0	1	1	0
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Fig. 5. Below: SISO shift register connected as a memory — the information must be read out in serial form.



PRACTICAL GUIDE TO REED SWITCHES Part 2



In the second part of this series, Collyn Rivers explains how reed switches may be electrically actuated.

Reed switches are actuated by a magnetic field.

This field can be generated by a permanent magnet, or by an electrically energised coil. When coils are used, the reed switch is simply inserted within the coil former and it is then closed (or opened) when current is passed through the coil.

It operates, in fact, as a relay, and in this form reed switches are used by the million, in telephone systems around the world.

When a reed switch is to be electrically actuated, an indication of the magnetic field strength that is required is generally quoted by the manufacturer in terms of so many ampere-turns. This figure may range from 50 AT to 250 AT (but as ex-

		Turns	7,520		9,600		11,900		15,000		19,500		25,000		36,000		43,100		53,000		66,500		86,800	
		Ohms	219		355		550		855		1,390		2,380		4,320		6,380		9,900		16,000		25,000	
Switch Sensitivity	50AT		1.5	6.5	1.8	5	2.3	4.2	2.8	3.3	3.5	2.5	4.8	2	6.1	1.4	7.3	1.2	9.4	0.8	12	0.75	15.7	0.6
	100AT		3.0	13	3.6	10	4.6	8.4	5.7	6.7	7.1	5.1	9.5	4	13	2.8	14.7	2.3	19	1.9	24	1.5	31	1.2
	150AT		4.5	20	5.3	15	6.9	12.6	8.5	10	11	7.6	14	6	18	4.2	22	3.5	28	2.7	36	2.3	47	1.8
	200AT		6.0	26	7.0	20	9.2	17	11	13	14	10.2	19	8	24	5.6	29	4.6	38	3.8	48	3.0	94	2.4
	250AT		7.5	33	8.8	25	11.5	21	15	16	18	12.7	24	10	30	7.0	37	5.8	47	4.6	60	3.8	110	3.0
			v	ma	v	ma	v	ma	v	ma	v	ma	v	ma	v	ma	v	ma	v	ma	v	ma	v	ma

Table 2. Data for standard size reed switch operating coils — bobbins to be 2" long × 0.220" inside diameter, winding build up will be approx. 0.2".

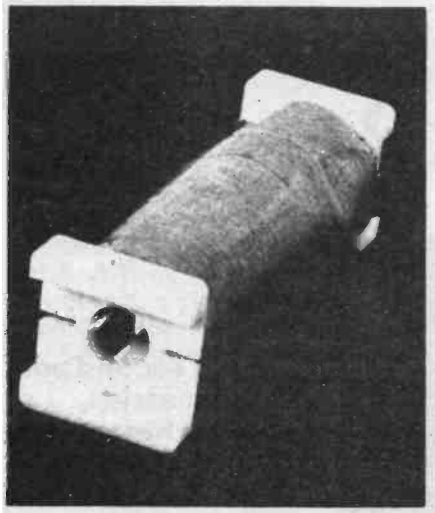


Fig. 11. Bobbin for standard sized reed switch.

plained later, this may be substantially reduced by the judicious positioning of a bias magnet).

Various combinations of turns, wire sizes and dimensions may be used to close any specific type of switch, and these parameters will in turn be determined not only by the required number of ampere-turns, but also by the circuit voltage and current that is available. For example a switch that requires 100 ampere-turns may be actuated by a 220 ohm winding drawing 13 mA at 3.0 V., or by a 25,000 ohm winding drawing 1.2 mA at 31 V.

Table 2 provides all the data required to design operating coils for a wide variety of standard sized reed switches (ie, 2.75 overall, 2.0 long, 0.217 diameter).

The operating coil may either be wound on a bobbin manufactured specifically for the purpose (Fig. 11) or made up from a length of paper, aluminium or plastic tubing that is a neat fit over the outside diameter of the glass reed.

Another method of making operating coils is to wind them, using a cement coated wire, onto an arbour that is shaped to create the desired final form. After removal from the arbour, the winding should be protected by a layer of insulating tape.

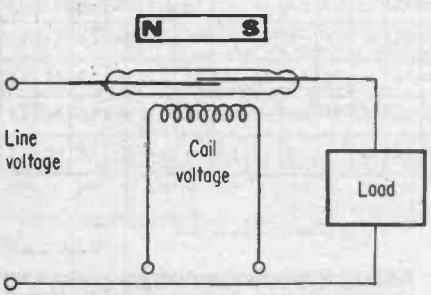


Fig. 12. Magnet assists reed switch to close, and thus reduces coil energy requirement.

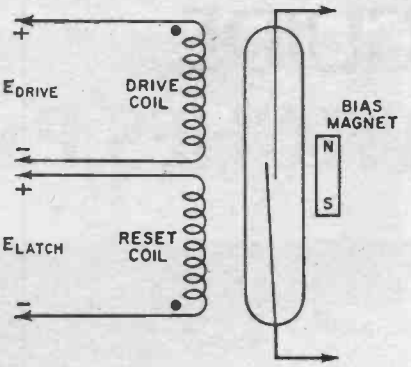


Fig. 13. In this circuit, reed switch is latched by aiding permanent magnet, and reset by magnetic opposition from reset coil field.

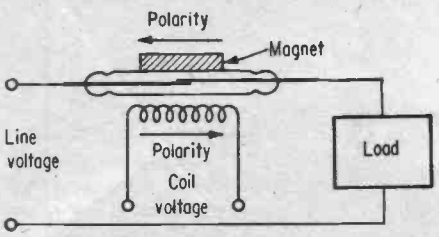


Fig. 14. Normally closed operation using magnetic bias.

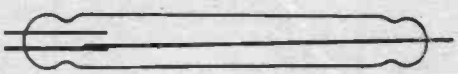


Fig. 15. This type of reed switch may be used for either change-over or normally closed operation.

EXTERNAL MAGNETIC FIELDS

A reed switch is influenced by a magnetic field regardless of whether that field is produced by the operating coil or by some other magneto-motive force. The magnetic force generated by the field winding can be modified or even completely cancelled by the field from a nearby permanent magnet, or by the alternating flux from a nearby choke, transformer or other inductive device. Even the proximity of a sheet steel chassis may affect the energy at which a reed switch will just actuate.

But the effect of external magnetic influences may be usefully exploited to modify the characteristics of the basic reed switch assembly.

For example the ampere-turns required to close any given switch, can be halved by placing a magnet a short distance away from the coil — the magnet's polarity must be the same as that of the operating coil. The positioning of the magnet is fairly critical and is best determined by trial and error (Fig. 12).

A similar method can be used to obtain a latching action. In this case the method exploits the magnetic hysterisis of the reed switch. The magnet is placed far enough away from the coil so that it does not close the reeds magnetically, but sufficiently close so as to hold the reeds closed once they have been actuated by an electrical signal through the coil.

In this example the reed relay can be unlatched only by physically removing the magnet, or by applying opposite polarity drive through the operating coil.

A further modification of the magnetic latching principle is shown in Fig. 13. Here, whilst magnetic latching is still used, the operating coil has two windings, one of which is used to actuate the relay, and the other, which is connected in opposite polarity, is used to unlatch the relay.

A magnet may also be used to convert a normally open reed relay to normally closed operation. This is done by locating the magnet sufficiently close to the reed so that the contacts are held closed. (Fig. 14). The coil is wound so as to produce a magnetic flux of opposite polarity to the magnet. When the operating coil is energised, the resultant magnetic flux will cancel out that from the permanent magnet, and the reed will open.

Change-over action may be obtained either by using a reed switch specially made for the purpose (Fig. 15) or by using a magnet and two normally open reed switches actuated by a common operating coil (Fig 16).

It is possible to actuate a number of separate reed switches located inside one large operating coil, but due to variations in the sensitivity between one reed and another, and the positioning of individual reed switches within the operating coil, it is not possible to predict the contact action sequence. All other things being equal the most sensitive reed will operate first. This will then act as a magnetic shunt, retarding the

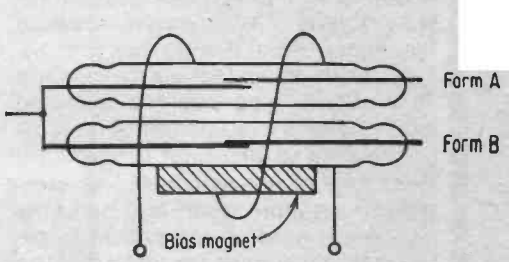


Fig. 16. Change-over action may also be obtained by combining a magnet and two normally open switches actuated by a common operating coil.

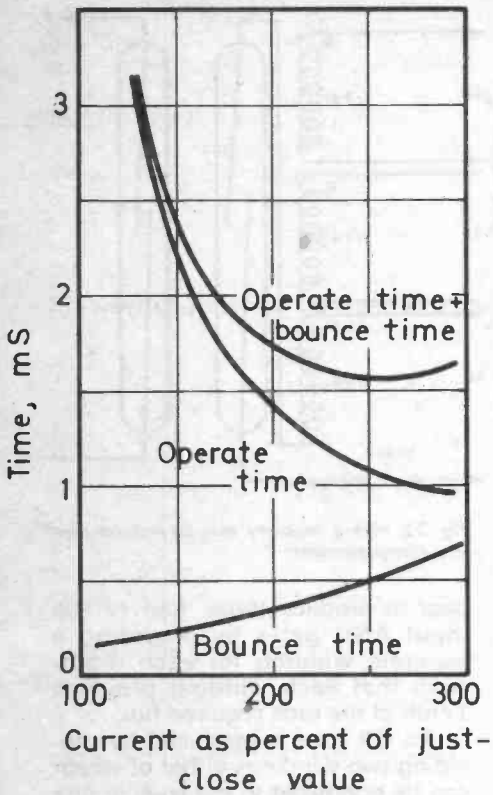


Fig. 17. Variation of operate and bounce time with energising current.

operation of the remaining reed switches. This is a major difference from conventional electro-mechanical relays where a single armature or card drives all of the movable contacts and any pair of contacts can be adjusted to ensure synchronous operation or a specific contacting sequence.

Nevertheless if a current at least 150% of the just-operate ampere-turns of the highest rated switch of the group is applied suddenly, this effect is less noticeable, and in most applications may be virtually neglected.

SWITCHING CHARACTERISTICS

The moving blades inside a reed switch have very low mass and move only a few thousandths of an inch. The operating coil is not iron cored and so has little self-inductance thus allowing a magnetic field to build-up very rapidly. These factors combine to ensure that a reed relay is an inherently quick-acting device, in fact, operating times of less than one millisecond are quite typical.

The speed at which any specific reed relay closes is primarily a function of the number of ampere-turns in the operating coil. But when the contacts close they normally bounce two or three times and the harder the relay is driven (ie, the greater the number of ampere-turns) the greater the number of times that the contacts bounce. In general reed relay coils are designed so that nominal rated coils are designed so that nominal rated voltage produces approximately 50% more ampere-turns than the just-operate value. This gives optimum total operate time including the contact bounce time (Fig. 17).

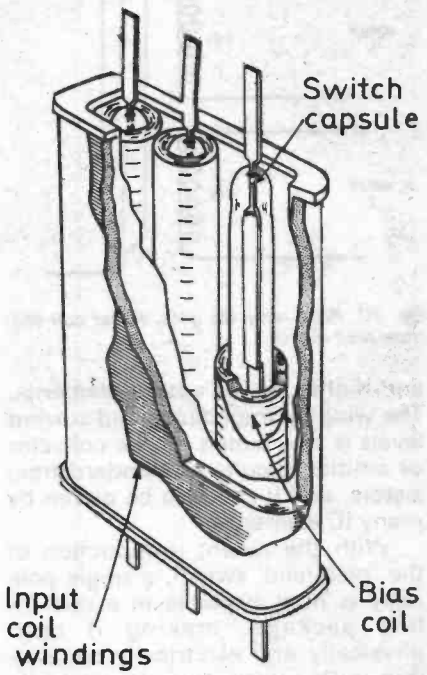
Fig. 18. Reed switch logic module.

After the contacts have closed and have stopped bouncing, the reeds continue to vibrate for a short time. This vibration produces magnetostriction contact noise — a damped oscillatory voltage that decays to zero — and this may cause problems in low signal level circuits.

With no suppression devices across the operating coil, reed release time is very fast — it may be as short as 25 micro-seconds. Adding a suppression diode has little, if any effect on the operate or bounce times, but it does significantly lengthen the release time. For example, the release time of a standard type of reed without a suppression diode may be 50 micro-seconds, but with a diode the release time may be extended to a milli-second or so.

Due to the geometry of the reed switch construction, the capacitance between contacts is low, and with standard sized reed relays this will be about one pico-farad. The capacitance between the reeds and the operating coil will be about 2.5 pico-farads but this can be reduced to approximately 0.5 pico-farads by interposing a grounded electrostatic shield between the coil and the reed.

Some thermal EMF will be generated at the junction of dissimilar metals in reed switches due to the heating produced by energising the coil. This thermally-generated EMF may be undesirable if the reeds are



used to switch low level analogue signals — as for example in data-logging or thermocouple measurements.

For applications where the thermal EMF must be held to the minimum a bi-stable latching reed relay should be used. A short pulse to the set coil operates the relay, no heat generating holding current is then required. Another short pulse to the reset coil releases the relay. Using this type of operation, the latching relay thermal EMF remains below five micro-volts, compared to as much as 100 micro-volts for continuously energised relays.

REED SWITCHES AS LOGIC ELEMENTS

The reed relay is almost an ideal buffer between solid state devices

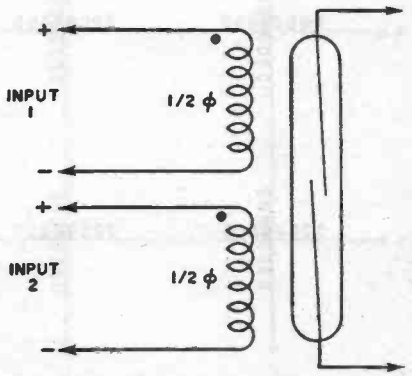


Fig. 19. The reed relay as an AND gate. Each coil can produce ½ a 'flux unit', and an output is obtained only when voltages are applied to both inputs.

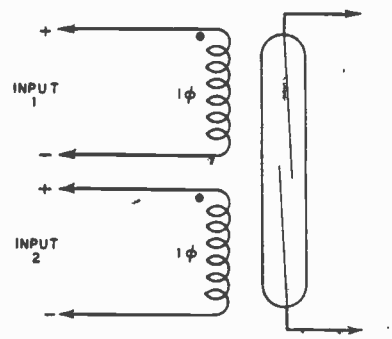


Fig. 20. Reed relay OR gate. Either coil can close reed switch.

and higher power output elements. The winding impedance and current levels is well suited for the collector or emitter circuits of standard transistors, and it can also be driven by many IC elements.

With the recent introduction of the 'pico-reed' switch, a single pole relay is now available in a dual-in-line package, making it both physically and electrically compatible with integrated circuit components. And as reed relays become smaller their operating speeds increase, so that a pico-reed relay can be made to follow 1 kHz pulses.

Reed switches are finding increasing use as logic elements for use in adverse environments. They are capable of performing a large variety of logic functions including AND, OR, EXCLUSIVE OR, and NOT operations. The relays can be used to construct flip-flop circuits, and these can be used in binary, binary coded decimal and decimal counters, ring counters, up-down counters and shift registers.

Whilst operating speed is very considerably slower than with solid state logic elements, there is not the same necessity for precise voltage and frequency regulation, nor the susceptibility to voltage transients. And for these reasons reed relay logic circuits are becoming increasingly used in industrial equipment.

A wide range of reed relay logic elements are commercially available — generally in a configuration similar to that shown in Fig. 18. The individual reed switches are surrounded by bias coils, and these in turn share a common input winding coil. By adjusting the ampere turns level to both input winding and the individual bias windings, a multiplicity of functions can be obtained. A permanent magnet can also be used in this type of logic element to provide memory or latching functions.

When designing reed relays as logic elements, the amount of magnetic flux that is required to close the relay is regarded as one flux unit. Thus a two input AND gate consists of one reed switch surrounded by two windings each of which can generate one half a 'flux unit' (Fig. 19).

It is possible to expand the concept to produce three, four or five input AND gates by providing a separate winding for each input, such that each winding provides 1/nth of the total required flux.

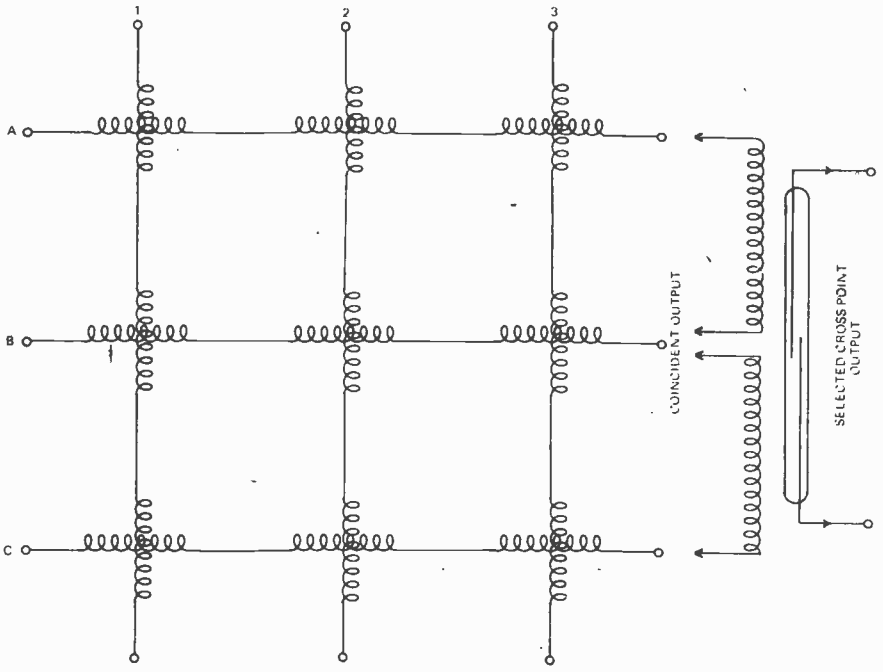


Fig. 21. Cross-bar matrix switching, the appropriate relay will close whenever both coils of any given relay are coincidentally energised.

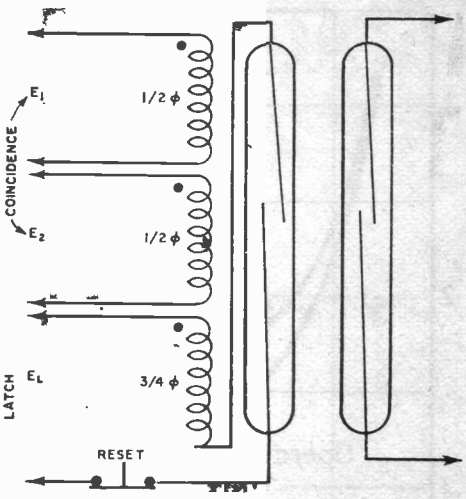


Fig. 22. How a 'memory' may be incorporated in a matrix element.

An OR gate is produced by providing two windings either of which can be energised to the level of one flux unit (Fig. 20). Thus a voltage in either winding can cause the relay to close. Again as with the AND gate, a number of windings may be used provided each one can provide one full flux unit.

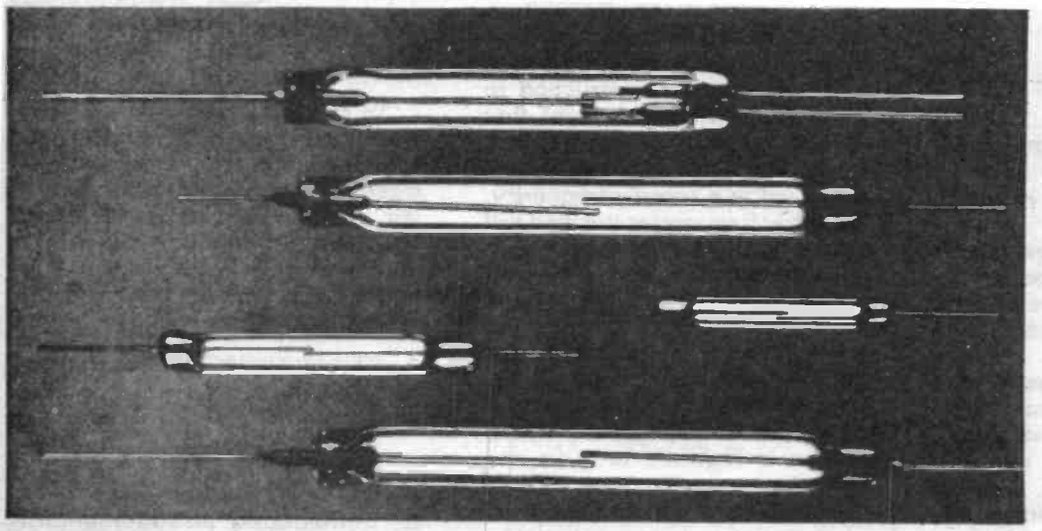
The basic OR gate can be used as an exclusive OR gate simply by reversing the direction of one winding. In this application if either one or the other winding is energised then the relay will close, but if both are energised then the resultant magnetic fields will cancel out and the relay will remain open.

Inverted operation is provided by using relays that are magnetically biased into normally closed operation.

Cross-bar matrix switching is readily achieved by using a double wound relay, in which each winding provides half a flux unit, at each selection point, ie, A1, A2, A3, etc (Fig. 21). The appropriate relay will close whenever both coils of any given relay are coincidentally energised.

The cross bar switching system may be used with a magnetic or electrical memory if required. Fig. 22 shows how two reed switches can be used, together with a latching winding, to provide an electrical memory in a reed relay cross bar switching system. In this form the matrix will remember the inputs after they have been removed, until the latching power supply is interrupted.

PRACTICAL GUIDE TO REED SWITCHES Part 3



Final part of this series describes reed switch applications.

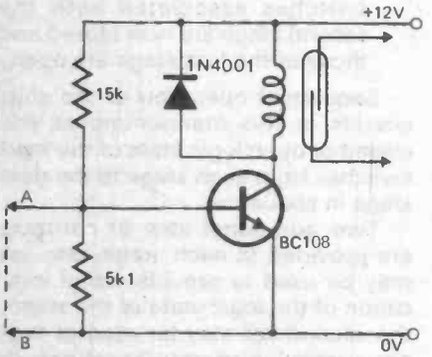


FIG. 23

Reed switches can be combined with solid-state electronic components to provide extremely reliable and maintenance free circuitry.

The low operating current of the actuating coil is well within the collector current rating of practically any transistor (and most linear integrated circuits). Many simple practical circuits can be constructed using a single transistor and a reed switch.

The circuit shown in Fig 23 is commonly used to open or close a relay when an external circuit is made or broken. It is commonly used in simple burglar alarm installations.

In operation, the transistor is cut off by a short circuit across points 'A' and 'B' (shown as dotted lines). Because the transistor is cut off, the reed relay operating coil in the transistor's collector circuit is not energized, and the relay contacts are open.

If the short circuit is removed from points 'A' and 'B', the transistor is biased on via the 15k resistor, the relay coil is energized and the reed switch is closed. Current consumption of this circuit — whilst the relay is de-energized — is less than one milliamp.

The circuit shown in Fig. 24 has a similar function to that of Fig. 23, except that the relay will close when a short is placed across points 'A' and 'B'.

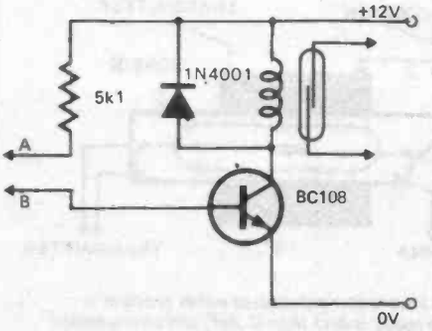


FIG. 24

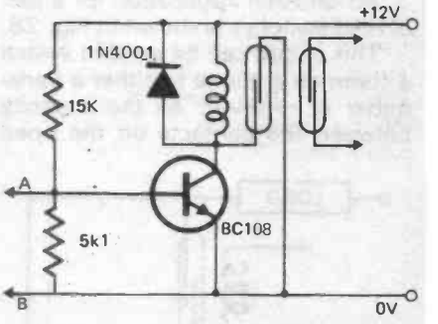


FIG. 25

It is often necessary to arrange for the relay to remain closed even though the actuating signal is only momentary. This can be done by using an actuating coil, containing two reed switches, and using one of the reed switches to short out the transistor the moment the coil is actuated — Fig 25 refers.

A very sensitive circuit that can be used as a moisture sensing switch is shown in Fig. 26. This circuit has a gain of well over 2500.

The relay will close whenever the resistance between points 'A' and 'B' fall below a few hundred thousand ohms. The 100k potentiometer is not an essential part of the circuit, but may be included as a 'sensitivity'

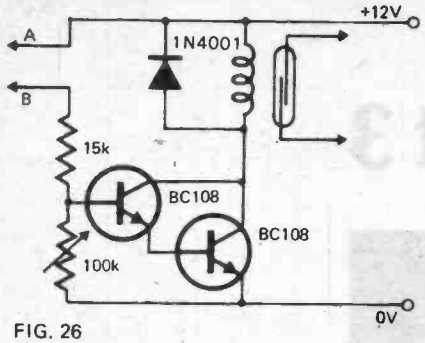


FIG. 26

control. The current consumption of this circuit, when the relay is de-energized, is less than one micro-amp.

Any of these circuits (Figs. 23, 24, 25, 26) may be combined with the Triac actuating circuit shown in Fig. 27 and used to switch very high current loads.

For example the moisture sensing circuit shown in Fig. 26 can be combined with the Triac switching circuit to energize a large motor driven pump. If necessary, three reed switches may be combined in one energizing coil to switch three Triacs in a three phase circuit. Using this principle loads of several hundred Amps may be switched without using a single contact.

An unusual application for a pair of reed switches is shown in Fig. 28.

This circuit can be used to switch a common antenna to either a transmitter or receiver. As the capacity between the contacts on the open

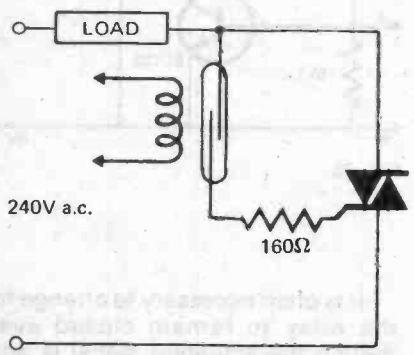


FIG. 27

reed is less than 0.2 pF, the system may be used at very high frequency.

Time delays of up to 10 seconds can be obtained using the simple circuit shown in Fig. 29. The delay is adjusted by the 50k potentiometer. It is not practicable to obtain longer delays than 10 seconds by increasing the size of the capacitor.

RESONANT REEDS

Resonant reed switches are basically similar in construction to normal reed switches, except that one reed is designed to resonate mechanically when its operating coil is energized at a specific frequency. At the other frequencies the reed will not move to any extent.

As the reed only makes contact for a portion of each cycle, it is usually necessary to arrange for latching action, or for some form of storage or pulse lengthening circuit.

Resonant reed switches are used for a variety of applications where response is required only to one specific frequency — these include communications, selective signalling, data transmission, telemetry, frequency monitoring etc.

Reed switches may also be used in very sophisticated logic circuits, usually in applications where their immunity to noise causes them to be chosen in preference to the generally cheaper solid-state components.

Fig. 30 shows a four-stage shift register which uses reeds as magnetically latched devices in simple magnetic circuits. The information in each stage is stored as closed or open switches, and the condition of each stage is transferred to the next as the shift control is operated. Only a single contact set is used for control purposes in each stage, as the state of a stage is stored as a capacitor charge during the shifting interval. However each stage has auxiliary switching contracts for output purposes.

The basic principle of operation can be considered as a series of latching relays. Momentarily closing the 'set' contact energizes coil S1

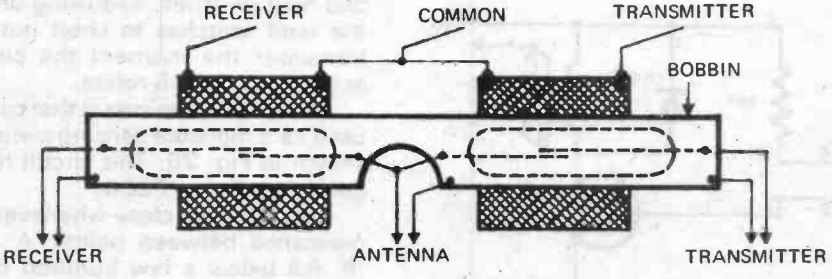


Fig. 28. Here reed relays are used to switch a common antenna to either receiver or transmitter. As the capacitance between the reeds is less than 0.2pF, the arrangement may be used at very high frequency.

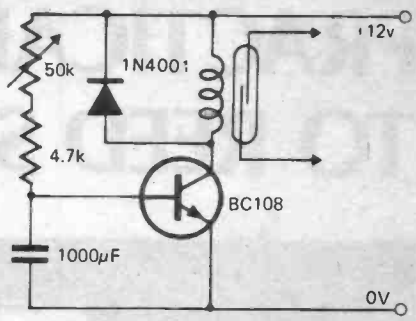


FIG. 29

and closes reed switches STG1. The associated bias magnet latches these switches closed, thus allowing the 'set' contact to be re-opened. The logic state of the first stage may now be shifted to the second stage by operating the shift contacts in this sequence:

a. Closing contact A, thus charging capacitor C2.
b. Closing B for a few milliseconds and thus unlatching STG1 switches.
c. Opening contacts A and B.
d. Immediately and momentarily closing contact C. Capacitor C2 now discharges through coil C2 via contact C. Switches STG2 now close and are latched by the associated bias magnet. The switches associated with the second stage are now closed and those of the first stage are open.

Sequential operation of the shift circuits in this manner moves the closed or open logic state of the reed switches from each stage to the next stage in sequence.

Two additional sets of contacts are provided in each stage, one set may be used to provide visual indication of the logic state of the stage, the second set may be used to trigger particular operations whenever required.

Reed switches may also be used in many types of coding and decoding systems. A simple decimal to binary encoder is shown in Fig. 31. In this circuit, the input is from a decimal keyboard energizing reed relay coils, while the output is in four-bit binary. Single, double, and triple switch relays are required for this application.

MERCURY WETTED CONTACT RELAYS

The mercury wetted contact relay overcomes the problem of contact bounce that is inherent in the dry reed switch.

The construction of the mercury wetted switch is shown in Fig. 32. It consists of a glass encapsulated reed

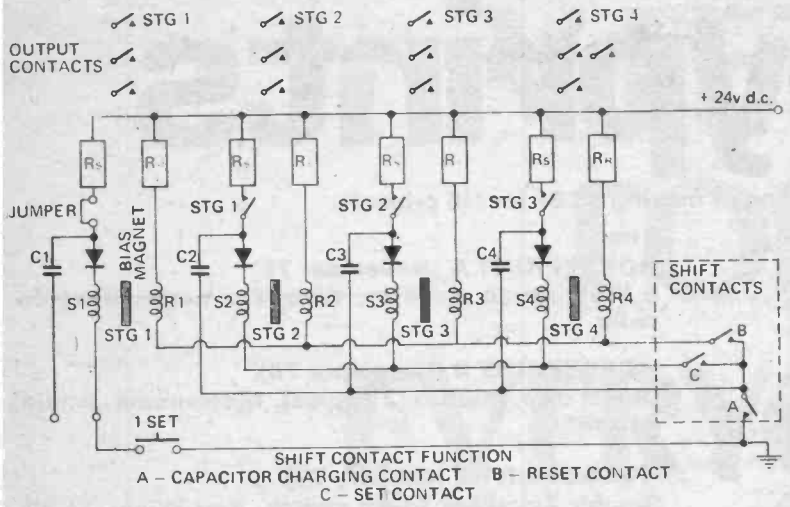


Fig. 30. This four-stage shift register uses reed relays.

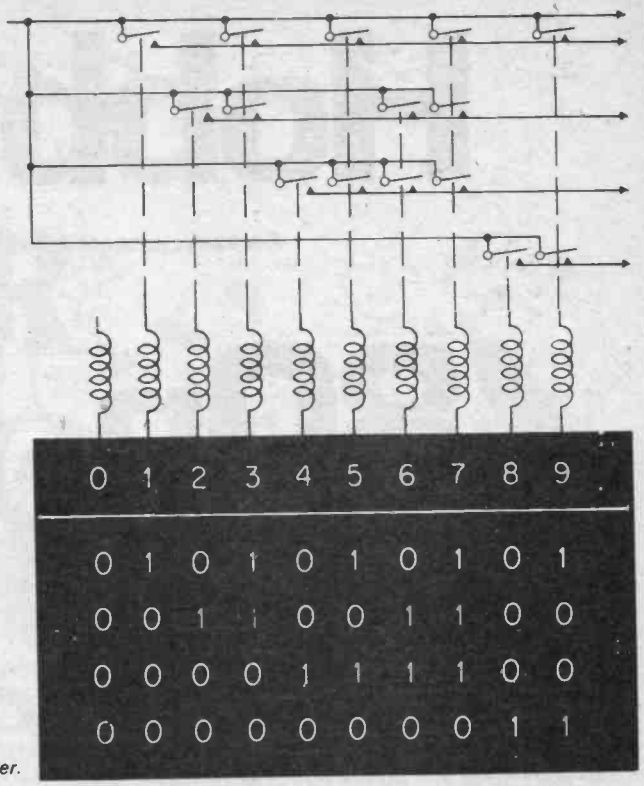


Fig. 31. Reed switch decimal binary encoder.

which has one end immersed in a pool of mercury. The other end of the reed is capable of moving between two sets of stationary contacts. The mercury flows up the reed by capillary action and wets the surface of the fixed and moving contacts. Thus a mercury to mercury contact is maintained whilst the contacts are closed.

The resistance of mercury is very low and contact to contact resistances of mercury wetted switches rarely exceed 50 milliohms. This is somewhat less than if the contacts were permanently soldered together!

The mercury wetted switch may be opened and closed in a similar fashion to its dry reed counterpart. Operating times are typically 10 milliseconds at normal coil current, falling to three milliseconds at twice the normal ampere-turn rating. The release time is typically four milliseconds under any conditions.

Apart from their high current carrying capacity, mercury wetted reeds have extremely long life since contact erosion is eliminated.

The disadvantages of mercury wetted reeds are poor resistance to shock and vibration, and the need to mount the reed vertically.

FUTURE DEVELOPMENTS

A lot of development work is currently being undertaken — particularly toward the use of cladded reed material.

Nickel-iron reeds combine optimum magnetic characteristics with the high internal damping that is required to minimize contact bounce; but the material is by no means an ideal conductor, and because of this, high resistivity losses within the switch are appreciable at high current loadings.

Cladding with gold or copper substantially reduces many of the undesirable characteristics of the nickel-iron reeds. This cladding reduces the effect of skin resistance. — which can be appreciable at high frequencies — and if the cladding is continued right to the ends of the external lead-outs — it virtually eliminates the thermal emfs generated when a copper wire is soldered to a nickel-iron reed in a conventional reed switch.

Another problem currently being investigated is that of reed switch contacts failing to separate, especially after they have been held closed for long periods at high temperatures. This is caused by molecular migration and the resultant metallic bond cannot be broken by the low separating force available. This problem has not yet been completely overcome but current development is toward heat treatment to produce a diffusion of gold into the nickel-iron base, and multilayer diffusion techniques.

Prices of reed switches are still decreasing, and as they become cheaper, new markets are opening up.

The motor industry in particular is using reed switches in fuel injection and ignition systems. The security industry appreciate the reliable maintenance-free service that can be obtained. Machinery manufacturers are beginning to use reed switches in applications in which adverse environments preclude open switch contacts.

For what other type of switch can remain static for twenty years and then work perfectly the first time that it is actuated?

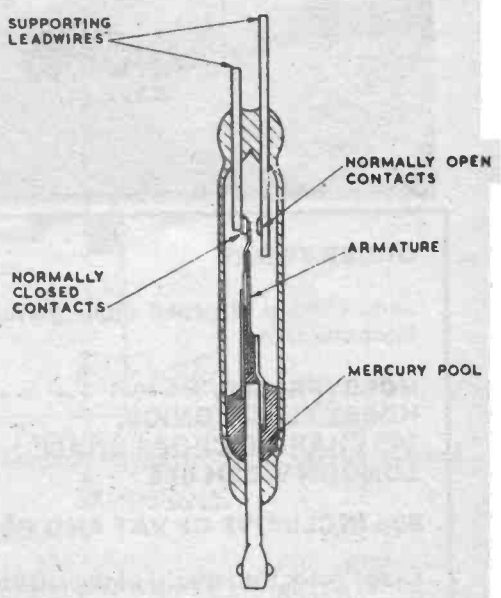
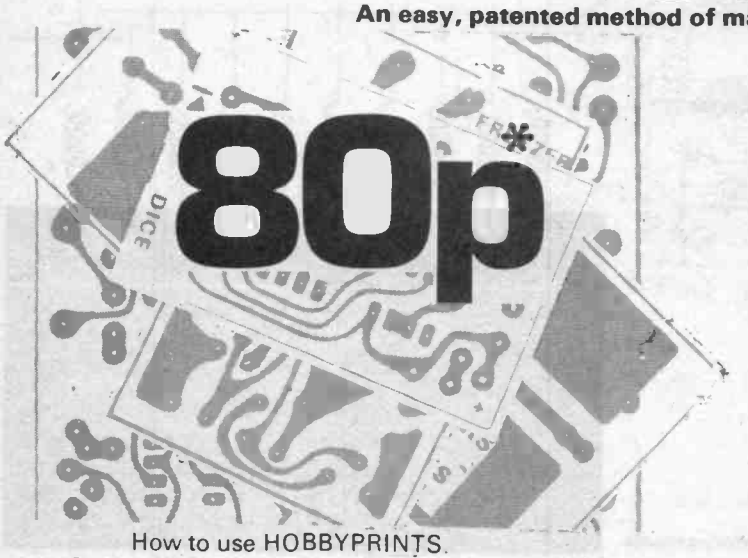


Fig 32. Construction of a mercury wetted reed switch

Hobbyprints

An easy, patented method of making PCBs for HE projects.



How to use HOBBYPRINTS.

1. Clean the PCB as you would for any work giving it a rub down with fine sandpaper (we even supply this in the kit). A quick wipe over with lighter fuel will help to remove any grease marks.

2. Lay down the HOBBYPRINT and rub over with a soft pencil until the pattern is transferred to the board. Peel off the backing sheet carefully making sure that the resist has transferred. If you've been a bit careless there's even a 'repair kit' on the sheet to correct any breaks!

3. Cut the board to size and put it in the Ferric Chloride.

4. When etching is completed, wash the board and use the sandpaper or a scouring powder to remove the resist. The resist pattern is pretty hardy but is easily removed at the final stage.

5. All you've got to do now is drill the board. Time? Only about ten minutes from beginning to end plus etching time (15 minutes usually with a good acid).

ORDER TODAY

Send cheque or postal order (payable to Hobby Electronics) to:

HOBBYPRINTS,
HOBBY ELECTRONICS,
145 CHARING CROSS ROAD
LONDON WC2H 0EE

80p INCLUSIVE OF VAT AND POSTAGE.

Please mark the letter(s) of the HOBBYPRINTS on the outside of the envelope.

HOBBYPRINT A (November 78)
5 Watt stereo amplifer, Waa-Waa pedal, Bedside radio.

HOBBYPRINT B (December 78)
Digital dice, Photon (2 copies), Metronome, Audio mixer.

HOBBYPRINT C (January 79)
Graphic Equaliser, Touch switch, Vari-Wiper, Flash Trigger.

HOBBYPRINT D (February 79)
Short Wave Radio, Sine/Square generator, Scratch/Rumble filter, Car Alarm.

HOBBYPRINT E (March 79)
Light Chaser, Photo Timer, Casanova's Candle, (2 copies), Tone Control (2 copies).

HOBBYPRINT F (April 79)
Train controller, Cistern Alarm, Transistor Tester

HOBBYPRINT G (May 79)
Parking meter timer, Digibell, Power supply, Sound effects unit

HOBBYPRINT H (June 79)
GSR Monitor, Drill Speed controller, Envelope Generator.

HOBBYPRINT I (July 79)
Shark, Baby Alarm, Point Controller, Linear Scale Ohmeter.

HOBBYPRINT J (August 79)
Home Security System, LED Tachometer, Injector/Tracer, Constant Volume Amplifer.

HOBBYPRINT K (September 79)
Combination Lock, Light Dimmer, Starburst, Ultrasonic Switch.

HOBBYPRINT L (October 79) £1.20
Tantrum, Hobbytune, Analogue Frequency Meter, Multi-Siren.

HOBBYPRINT M (November 79)
Hebot, R2-D2 Radio, Guitar Tuner.

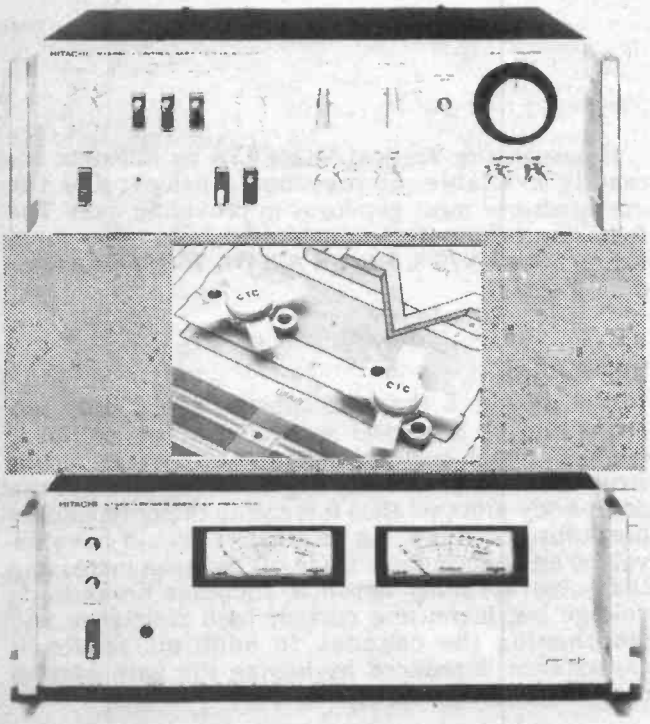
HOBBYPRINT N (December 79)
Scalextric Controller, Ring Modulator, Bargraph Voltmeter, Hebot II.

*Except Hobbyprint L

V·FETS FOR EVERYONE!

This article, by Wally Parsons, first appeared in our Canadian edition. We think that V-FETs represent a large step forward in power amplifier technology and so we have reprinted it.

The first part of 'V-FETs for Everyone' covers the theory behind V-FETs and what their specifications mean. Part two will describe how V-FETs are used at present and how to design V-FET circuitry.



Since the semi-conductor is precisely that, a battery across the ends of a *p*-type or an *n*-type bar will cause current to flow through the material, just as it does through a vacuum tube. If a *p*-type material is joined to the surface of an *n*-type bar, located between the battery terminals, a *pn* junction is formed, and if this junction is reverse biased, a space charge or field is produced of opposite polarity which will inhibit current flow, just as the control grid inhibits current flow in a vacuum tube. Changing this reverse voltage causes a large current change, and therefore amplification results.

A simple FET (J-FET) is shown in Fig. 1. With a given drain — source voltage, maximum current flows under zero gate voltage conditions and at some reverse levels, no current will flow. Also, as in the vacuum tube, load characteristics are not reflected to the input circuit, because current is not controlled by carrier injection as in bipolars, but by voltage levels.

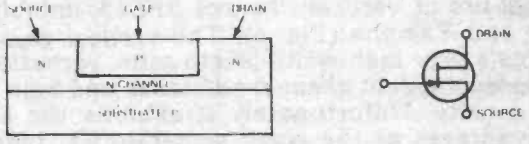


Fig 1: N-channel JFET construction and symbol

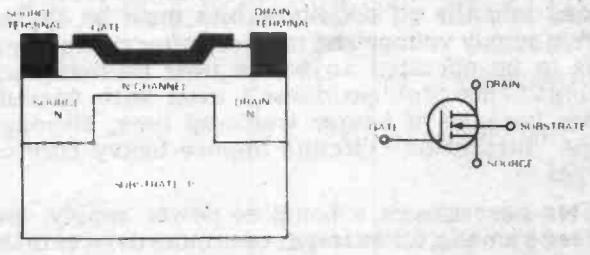


Fig 2: N-channel depletion horizontal MOSFET construction and symbol

A variation is the *M*etal *O*xide *S*emi-conductor *F*ield *E*ffect *T*ransistor. (MOSFET) (Fig. 2) a far more versatile device whose technology is virtually the cornerstone of modern computer technology,

although it has had less use to date in linear applications such as audio amplification.

MOSFETS come in two basic types. In both types the gate consists of a metal electrode separated from the channel by a thin oxide layer. In the depletion type current flow is controlled by the electrostatic field of the gate when biased. Voltage relationships are the same as for the J-FET, except that when the J-FET is forward biased current will flow through the junction (after all, it *is* a *pn* junction). This does not contribute to amplification, and may even destroy the device. When a depletion MOSFET is so biased it may result in increased current flow and, provided current, dissipation, and breakdown ratings are suitable, the device may be driven on both sides of the zero volts point as with vacuum tubes. Unlike vacuum tubes under these conditions, the gate draws no cirrent and therefore does not require the driver to deliver power.

The enhancement type MOSFET shown in Fig. 3, is more widely used. The source and drain are separated by a substrate of opposite material, and under zero gate volts no current flows. However, when sufficient forward bias is applied to the gate the region under the gate changes to its opposite type (e.g. *p*-type becomes *n*-type) and provides a conductive channel between drain and source. Carrier level and conduction are controlled by the magnitude of gate voltage. Although J-FETS, and especially MOSFETS, have certainly delivered on their original promise, in one area they are particularly conspicuous by their absence, and that is in the area of power. Unfortunately, the channel depth available for conduction is limited by the practical limits on gate voltage. The lower current density has been the primary limitation due to the horizontal current flow.

VMOS

Recent years have seen the introduction and commercial use of Vertical Channel J-FETS, notably by Sony and Yamaha (Fig. 4). The vertical channel permits a very high width-length ratio, permitting a decreased inherent channel resistance and high current density. Unfortunately it exhibits the same disadvantages as the small signal J-FET, plus, in available devices, a very high input capacitance, ranging from 700pf to around 3000pf, limiting high frequency response. In addition, since they must be biased into the off condition, bias must be applied *before* supply voltage and removed after the supply if it is to be operated anywhere near its maximum ratings. This problem doesn't exist with vacuum tubes because of heater warm-up time, although some "instant-on" circuits impose heavy turn-on surges.

This necessitates a complex power supply, and indeed Yamaha, for example, uses more devices in the supply than it does in its amplifier circuits. However, the construction does make possible the design of complementary types and Nippon Electric and Sony both have high power devices available. Unfortunately, neither company seems anxious to make detailed information available, so there is little to disclose here beyond the fact that they are said to have characteristics similar to those of triode tubes.

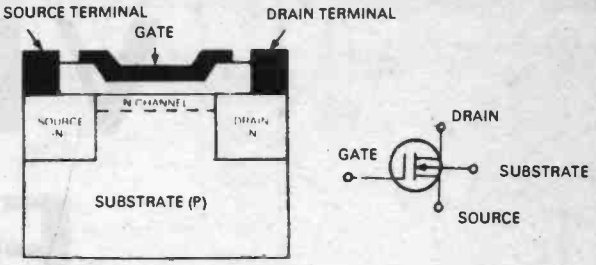


Fig 3: N-channel enhancement horizontal MOSFET construction and symbol

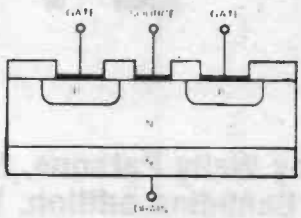


Fig 4: Vertical junction FET construction

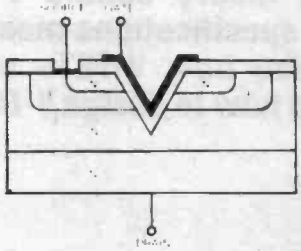


Fig 5: Vertical MOSFET construction (Siliconix)

However, the Vertical MOSFETS by Siliconix are readily available, at reasonable prices, and the manufacturer most generous in providing data. The following information is extracted from their application note AN76-3, Design Aid DA 76-1, plus device data sheets.

The Device

Notice in Fig. 5 that the substrate and body are opposite type materials separated by an epi layer (similar to high speed bi-polars). The purpose of this structure is to absorb the depletion region from the drain-body junction thus increasing the drain-source breakdown voltage. An alternative would have involved an unacceptable trade-off between increasing the substrate-body depth to increase breakdown voltage but increasing current path resistance and lengthening the channel. In addition, feedback capacitance is reduced by having the gate overlap n-epi material instead of $n+$.

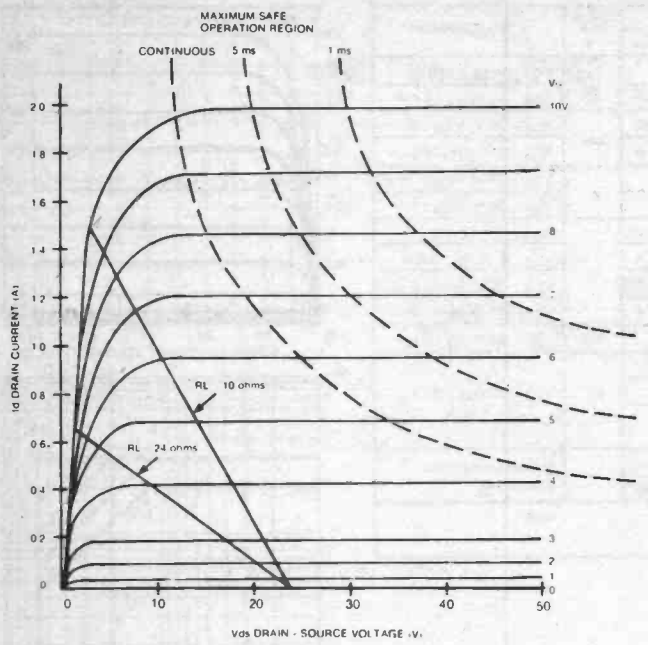


Fig 6: Output characteristics VMP1

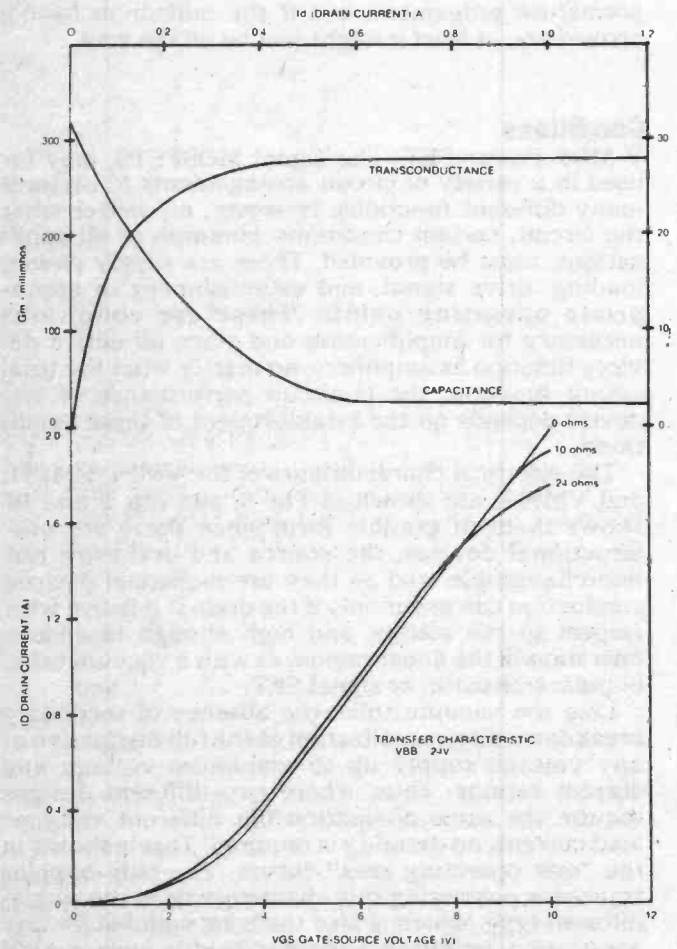


Fig 7: Other VMP1 characteristics

In manufacture, the substrate-drain and epi layer are grown, then the *p*-body and *n*+ source diffused into the epi layer, in a similar manner as the base and emitter of a diffusion type transistor. A V groove is etched through the device and into the epi layer, an oxide layer grown, then etched away to provide for the source contact and an aluminium gate deposited. It is apparent that this type of device allows current flow in one direction only; this is not always so with a similar type of horizontal FET, where source and drain may be identical in structure and of the same material. Therefore, no reverse current flows (we hope!) when used in switching applications, as was also the case with vacuum tubes.

In-circuit operation is refreshingly simple: Supply voltage is applied between source and drain, with the drain positive with respect to the source, under which conditions no current flows, and the device is off. This is an enhancement type device and is turned on by taking the gate positive with respect to the source and body. The electric field induces an *n* channel on both surfaces of the body facing the gate, and allows electrons to flow from the negative source through the induced channel and epi and through the substrate drain. The magnitude of current flow is controlled almost entirely by the gate voltage, as seen in the family of curves (Fig. 6 and 7) with no change resulting from supply voltage changes above 10V.

Advantages

The vertical structure results in several advantages over horizontal MOSFETS.

1) Since diffusion depths are controllable to close tolerances, channel length, which is determined by diffusion depth, is precisely controlled. Thus, width/length ratio of the channel, which determines current density, can be made quite large. For example, the VMP1 channel length is about 1.5 us, as against a minimum of 5 us in horizontal MOSFETS, due to the lower degree of control of the shadow masking and etching techniques used in such devices.

2) In effect, two parallel devices are formed, with a channel on either side of the V groove, thus doubling current density.

3) Drain metal runs are not required when the substrate forms the drain contact, resulting in reduced chip area, and thus reduced saturation resistance.

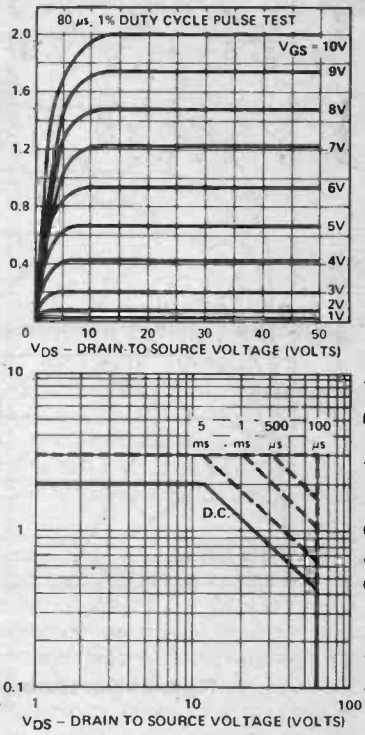
4) High current density results in low chip capacitance. Also, unlike horizontal MOSFETS, there is no need to provide extra drain gate overlap to allow for shadow mask inaccuracies, so feedback capacitance is minimized.

In comparison with bi-polars, especially power devices, the advantages are even more impressive.

1) Input impedance is very high, comparable to vacuum tubes, since it is a voltage controlled device, with no base circuit drawing current from the driver stage. A 7 V swing at the gate, at virtually O A, represents almost O W of power, but can produce a swing of 1.8 A in output current. This represents considerable power gain and will interface directly with high impedance voltage drivers.

2) No minority carrier storage time, no injection, extraction, recombination of carriers, resulting in very fast switching and no switching transient in

		Characteristics		VMP 11			VMP 1			VMP 12			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			60			90			V	V_{GS} = 0, I_D = 100 μA
2		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{GS} = V_{DS}, I_D = 1 mA
3		I_{GSS}	Gate-Body Leakage			0.5			0.5			0.5	μA	V_{GS} = 15 V, V_{DS} = 0
4		$I_{D(off)}$	Drain Cutoff Current			0.5			0.5			0.5		V_{GS} = 0, V_{DS} = 24 V
5		$I_{D(on)}$	Drain ON Current*	1	2.0		1	2.0		1	2.0		A	V_{DS} = 24 V, V_{GS} = 10 V
6		$I_{D(on)}$	Drain ON Current*	0.5			0.5			0.3				V_{DS} = 24 V, V_{GS} = 5 V
7	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance*		2.0	2.5		3.0	3.5		3.7	4.5	Ω	V_{GS} = 5 V, I_D = 0.1 A
8					2.4	3.0		3.3	4.0		4.6	5.5		V_{GS} = 5 V, I_D = 0.3 A
9					1.2	1.5		1.9	2.5		2.6	3.2		V_{GS} = 10 V, I_D = 0.5 A
10					1.4	1.8		2.2	3.0		3.4	4.0		V_{GS} = 10 V, I_D = 1 A
11		g_m	Forward Transconductance*	200	270		200	270		170			m℧	V_{DS} = 24 V, I_D = 0.5 A
12	DYNAMIC	C_{iss}	Input Capacitance		48			48			48		pF	V_{GS} = 0, V_{DS} = 24 V, f = 1 MHz
13		C_{rss}	Reverse Transfer Capacitance		7			7			7			
14		C_{oss}	Common Source Output Capacitance		33			33			33			
15		t_{ON}	Turn ON Time**		4	10		4	10		4	10	ns	See Switching Time Test Circuit
16		t_{OFF}	Turn OFF Time**		4	10		4	10		4	10		
*Pulse Test **Sample Test Pulse Test Pulse Width = 80 μsec, Duty Cycle = 1%														VMC*



Figs 8, 9 & 10: Electrical characteristics of the VMP devices from Siliconix, a freely available VFET.

class B and AB amplifiers. Switching time for a VMP1 is 4 ns for 1 A, easily 10-200 times faster than bi-polars, and even rivalling many vacuum tubes.

3) No secondary breakdown, and no thermal runaway. VMOS devices exhibit a negative temperature coefficient with respect to current, since there is no carrier recombination activity to be speeded up with temperature. Thus, as current increases so does temperature, but the temperature rise reduces current flow. It is still possible to destroy the device by exceeding its maximum ratings, but a brief near-overload does not result in an uncontrollable runaway condition. Usually, simple fusing and/or thermistor protection is sufficient for maximum safety, and even this may be unnecessary with conservative design. Absence of secondary breakdown means that full dissipation can be realized even at higher supply voltages. In this respect they resemble vacuum tubes.

Available Devices

Seven devices representing three families are available. Types VMP-1, VMP-11, and VMP-12 are 2 A, 25 W dissipation devices intended for switching and amplifier use and differ only in voltage rating (60 V, 35 V, 90 V, respectively). Types VMP-2, VMP-21, VMP-22, are 1.5 A, 4 W devices rated at 60 V, 35 V, 90 V respectively, and are intended mainly for high speed switching, but would also be useful for low power amplifiers and as linear drivers for bi-polars, where the latter offer advantages. And finally, type VMP-4, 1.6 A, 35 W, specifically intended for VHF amplifier use. All except VMP-4 devices feature gate protection to withstand static discharges and over-voltages, and all are currently available except the VMP-4. All are *n*-channel. One hesitates to pass premature judgement, but if the millenium hasn't arrived yet, at least it might just be on the way.

Conditions

V-MOS Power FETs like signal MOSFETS, may be used in a variety of circuit arrangements to perform many different functions. However, no matter what the circuit, certain conditions, common to all applications, must be provided. These are supply power, loading, drive signal, and establishment of appropriate operating points. These are conditions necessary for amplification and since *all* active devices function as amplifiers, no matter what the total circuit function, the in-circuit performance of any device depends on the establishment of these conditions.

The electrical characteristics of the VMP1, VMP11, and VMP12, are shown in Fig. 8, and Fig. 9 and 10 shows them in graphic form.Since these are unidirectional devices, the source and drain are not interchangeable, and as they are *n*-channel devices conduction can occur only if the drain is positive with respect to the source, and high enough to ensure operation in the linear region, as with a vacuum tube, bi-polar transistor, or signal FET.

Like the vacuum tube, the absence of secondary breakdown allows realization of the full dissipation at any voltage supply up to maximum voltage and current ratings. Thus, where two different designs require the same dissipation but different voltage/load current, no derating is required. This is shown in the "safe operating area" curves. The only bi-polar transistor possessing this characteristic is the single-diffused type, which is also the least suitable for any application requiring wide bandwidth and/or high speed.

V·FETS FOR EVERYONE Part 2

In general these devices may use any of the types of output circuits in general use with valves and bi-polars, including transformer coupled (Fig. 12) where the benefits of the absence of charge carrier storage become apparent in the absence of severe ringing at the cross over point, conventional series output such as in Fig. 1 which is a straightforward transformation from a bi-polar circuit (1), and single-ended output with current source, also transposed from an excellent bi-polar circuit (2) (Fig. 2).

We have received a note from Siliconix giving the following changes in type number — VMP-11 becomes 2N6656; VMP-1 2N6657; VMP-12 2N6658; VUP-21 2N6659; VMP-2 2N6660; VMP-22 2N6661.

Bias and Drive

These series of devices are *n*-channel, enhancement type MOSFETS, and may be biased and driven using methods appropriate to signal types and bi-polars. The drain is made positive with respect to the source and the gate enables conduction by being forward biased with respect to the source, that is to say it is biased in a positive direction. Unlike bi-polars, however, they are voltage, rather than current controlled, and circuit values are selected to provide the required voltage. Any current drawn is by the bias network itself.

Three bias methods are shown; Fig. 3 shows bias supplied from a fixed bias supply. It is the simplest possible method, allows extremely high input impedances, since *Rg* may be almost any very high value desired, and its stability is limited only by the stability of the bias supply.

The design shown in Fig. 4 has the advantage of requiring no extra supply voltage since it is taken from *Vdd*. Disadvantages are those of impedance and stability. Input impedance consists of the parallel combination of R1 and R2 (disregarding input capacitance of the MOSFET and the very low input leakage). There are practical limits as to how high this combination can become; if for example, we have a 60 volt supply and require 6 volts bias, we might have some difficulty obtaining higher values than 9 megohms and one megohms for R1 and R2.

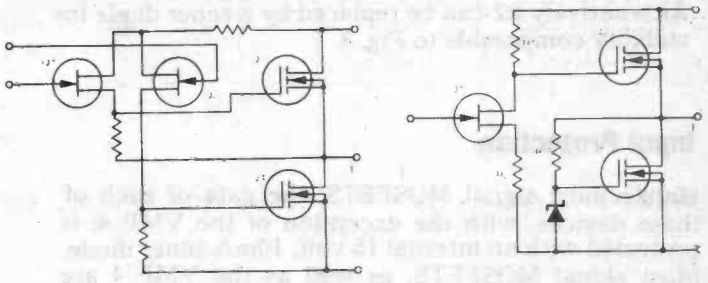


Fig. 1. Series output arrangement and Fig. 2 single-ended output with current source.

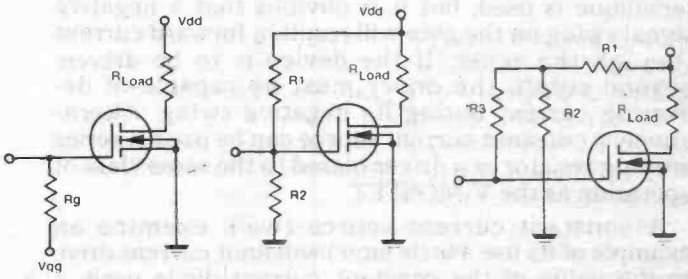


Fig. 3. High-impedance separate bias supply, Fig. 4 moderate impedance supply and Fig. 5 high-impedance common supply.

"Computerwise — I'd say it's artificial intelligence and simulation of behaviour!"

Higher values become more difficult to obtain, stability becomes less reliable, internal inductance and distributed capacitance become problems, and overcoming these difficulties usually costs money. In addition, if *Vdd* is subject to variation, then bias varies. In a class AB amplifier this could be quite serious, since *Vdd* varies considerably with output level; at high levels, *Vdd* can be expected to drop, causing a reduction in bias.

While this may reduce the danger of over-driving the device, it will be forced to operate in its non-linear region which may result in unacceptable performance characteristics unless taken into consideration in the overall circuit design (e.g. choice of feedback values). It does provide some degree of overload protection, and with correct choice of values can

provide for class AB operation at low levels, shifting to class B at high levels. With these considerations in mind, and/or where moderate impedances are required, it offers a low cost, simple, and reasonably reliable method of establishing the operating point.

The method used in Fig. 5 is similar except that with the addition of R3 higher input impedances are possible. Its configuration is similar to a noiseless biasing system frequently used in low-level bi-polar amplifiers and integrated circuits (e.g. National LM381A) but its function is somewhat different. Resistors R1 and R2 form a voltage divider as in Fig. 4 but their junction now forms a fixed bias source as in Fig. 3. Resistor R3 can be quite high since no current flows. Meanwhile, since the parallel combination of R1 and R2 are effectively in series with R3 they can be reduced to more manageable values. Alternatively R2 can be replaced by a zener diode for stability comparable to Fig. 3.

Input Protection

Unlike most signal MOSFETS, the gate of each of these devices, with the exception of the VMP 4, is protected with an internal 15 volt, 10mA zener diode. Most signal MOSFETS, as well as the VMP 4 are unprotected, or where extremely high impedances are not required, are protected by back to back zeners. I have no information as to why this different technique is used, but it is obvious that a negative signal swing on the gate will result in forward current through the zener. If the device is to be driven beyond cutoff, the driver must be capable of delivering current during its negative swing. Alternatively a constant current source can be used, a series limiting resistor or a driver biased to the same class of operation as the V-MOSFET.

A constant current source (we'll examine an example of its use a little later) will limit current drive to the value of the constant current diode used; a series resistance will drop the drive voltage as the diode draws current. In both cases, diode current must be limited to 10mA maximum. Higher currents will damage the protective zener diode.

However, if a class B output is used, conduction only occurs during positive half-cycles. Therefore, drive signal is not required during negative half-cycles. If a source or emitter follower driver stage is biased so as to pass no negative drive, the problem does not occur. However, great care must be exercised in the design of such a stage to ensure that drive does not disappear before the output device is cut off.

This is not too difficult with a class B or near class B stage; if the output device is operated at zero bias, then a small amount of bias on the driver will ensure conduction during slightly more than 180 degrees. Class AB operation is a little more tricky. If conduction is to occur for 270 degrees, for example, the driver should conduct for slightly more than this period.

Two types of drive circuits familiar to designers of bi-polar circuits are the Darlington and Super beta, commonly used together to provide a quasi-complementary circuit. Both circuits are current amplifiers designed to provide a compound device with very high h_{fe} and provide base current to the output device. However, similar circuits can be used with these devices to provide phase inversion in a series output stage.

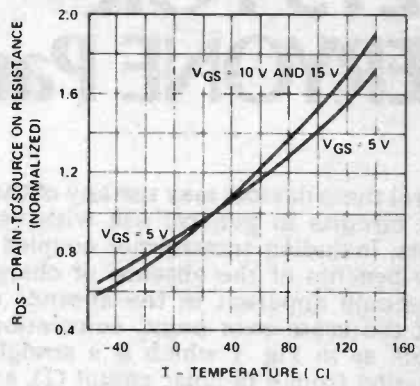
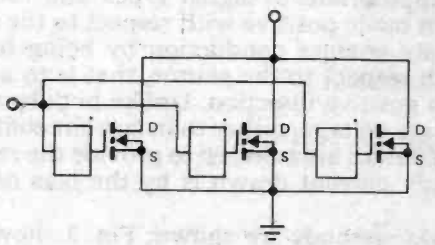


Fig. 6. Drain to source resistance against temperature (Siliconix).



*TO PREVENT SPURIOUS OSCILLATIONS, A 500 Ω 1K Ω RESISTOR OR FERRITE BEAD IFOR HIGHER SPEEDI SHOULD BE CONNECTED IN SERIES WITH EACH GATE.

Fig. 7. Basic circuit for parallel operation.

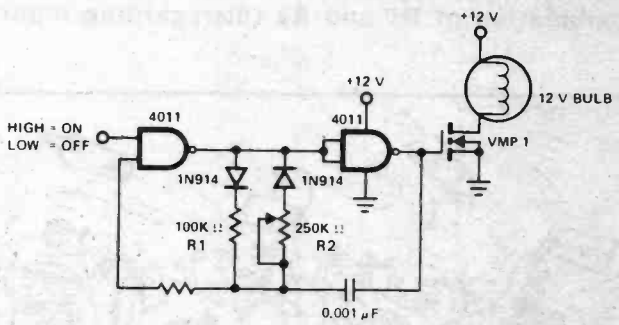


Fig. 8. Circuit of a high-efficiency light dimmer.

Thermal Considerations

As described earlier these devices exhibit a negative temperature coefficient with respect to current, so that as temperature rises, current is reduced, thus providing a self-inhibiting action which provides some protection against overload. However, this is not an unconditional effect. Fig. 6 shows the

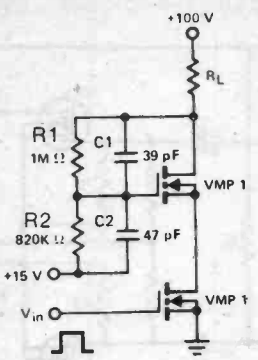


Fig. 9. Diagram for series operation.

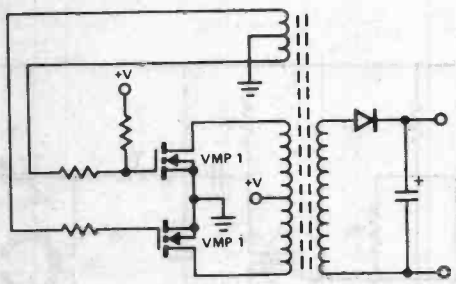


Fig. 10. A DC to DC converter (Siliconix).

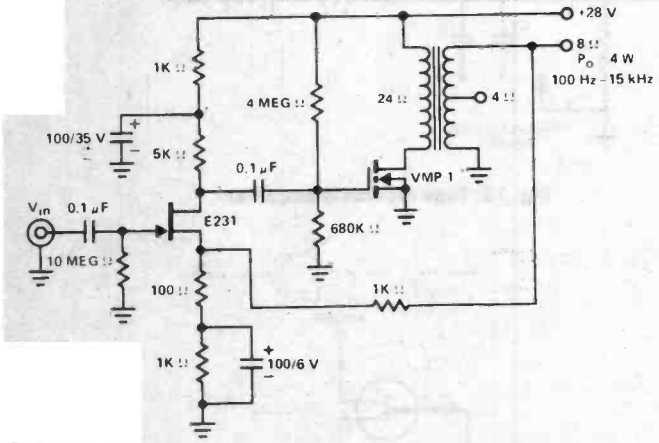


Fig. 11. Simple single-ended transformer-coupled audio power amplifier (Siliconix).

relationship between RDS (on) and temperature (3), based on a worst case temperature coefficient of 0.7 per cent per degree C.

Suppose that the device when on passes a current of 1 amp which causes it to heat up. The on resistance increases (which is why current drops), increasing the voltage drop across the device and the device dissipation. Now, if adequate heat sinking is used there is no real problem but if it isn't, the on resistance and junction temperature will rise to the point where extra charge carriers are generated, thus stabilizing RDS(on). That's great, except for the fact that this doesn't occur until the maximum safe junction temperature of 150 degrees has been exceeded.

You'll remember that we said earlier that the device was free of thermal runaway problems because of its negative temperature coefficient, but it isn't free of thermal destruction problems, and in any case, excessive temperatures will reduce output conductance. Heat-sinking requirements are, therefore, similar to those of bi-polars. The calculations of thermal operating conditions are beyond the scope of this article, but interested readers are referred to the Siliconix literature listed in the references, (4).

Extending The Ratings

The current handling capacity and therefore total dissipation capability may be easily increased by simply connecting several devices in parallel (Fig. 7). No ballast resistors are needed to ensure proper current sharing since if one device draws more current than another it simply gets a little warmer which causes it to draw less (assuming adequate heat sinking, of course). The only major precaution needed is to keep lead inductance in the gate and source connections to a minimum to prevent parasitic oscillations, unless the devices are driven from a low impedance source.

It may be advisable to insert "stoppers" – small resistors (500 to 1000 ohms) in series with each gate, wired directly to the socket, or ferrite beads mounted on the leads close to the socket terminals. An additional plus when paralleling several devices is that the gm is multiplied by the number of devices used. Mutual conductance gm is specified as the ratio of a large change in current to a small change in control voltage. If, for example, a change of 0.4 volts on the gate produces a change of 0.1 amp through one device, connecting two devices in parallel will give us an output swing of 0.2 amps, but it will still require only the original 0.4 volts gate swing. Since voltage gain A = gm x RL, if gm is increased, A is increased.

In real use, of course, the internal resistance of two devices in parallel is less than of one, the optimum load is less, so in amplifier applications, the net amplification A is the same. But notice that the drive requirements have not changed. With bi-polars current would have to be supplied to each base, thus increasing the output requirements of the drivers. Indeed, with many high-power amplifiers using multiple output devices the drivers are also power devices.

We can also extend the voltage ratings by series operation of two or more devices; Fig. 9 shows the technique. Resistors R1 and R2 bias Q2 on while C1 and C2 ensure fast switching. Input control signal is inserted between gate and source of Q1. Ordinarily the bottom of the divider chain is at ground potential for signal frequencies, so that circuit is really a cascode.

Maximum current and gm are the same as for one device.

Some Practical Applications

An efficient light dimmer circuit as proposed by Siliconix is shown in Fig. 8. The 4011 acts as a pulse width modulated oscillator whose duty cycle is determined by the ratio of R1 to R2, with R2 adjusted to control the brightness of the bulb. Of special interest here is the fact that with its fast switching time, the VMP1 is especially suited to pulse width modulation at power levels and suggests it as being suitable for use in switching, or class D linear amplifiers.

A DC to DC converter is outlined in Fig. 10. The VMP1s form an oscillator with positive feedback provided by the additional coil in the gate circuits. In operation the upper V-MOSFET is biased on, and the lower V-MOSFET is off. When power is applied the upper device conducts causing current to flow from Vdd through the upper half of the transformer primary and the upper V-MOSFET to ground. The induced current flow through the feedback coil develops a voltage such as to shift the bias in the upper device off (if the winding is connected with the correct polarity) and the lower device on. This causes current flow from Vdd through the lower half of the transformer primary and the lower V-MOSFET to ground.

The secondary circuit consists of a single rectifier and filter. The resistor in the upper gate prevents shorting out of gate bias, and the one in the lower gate keeps both sides balanced. In addition, each resistor limits current through the protective diodes. These are expensive devices for such an application, but the high reliability, the reduced RF radiation (due to reduced switching transients) and the circuit simplicity easily make up for the cost. The very high circuit impedance allows for running frequency to be set by the self resonance of the transformer.

A single ended and push-pull transformer coupled amplifier for audio applications are shown in Figs. 11 and 12. Both designs utilise the biasing system described in Fig. 4. A load-line drawn on the output characteristic will show the optimum load to be 24 ohms. In Fig. 11 gate drive is supplied by a single junction FET, and voltage feedback is taken from the output transformer secondary and series fed to the source of the input device. Distortion is under 2 per cent at full output (try to get *that* with a single ended valve or bi-polar) and could probably be reduced even further by adopting a source follower output stage.

A push-pull version of Fig. 11 is shown in Fig. 12 using a differential input to provide phase splitting, drive, and a feedback point. Although the transformer winding ratio implies the use of a low impedance loudspeaker, a step-up ratio could be used for direct coupling to an electrostatic speaker, a balanced transmission line (both with some modification of the feedback circuit) an unbalanced transmission line, or a 70 volt speaker distribution line.

Notice in both circuits, and in the biasing circuits shown that no source resistors have been used, either for local feedback or for bias setting. In valve and bi-polar circuits it's a useful technique, and with bi-polars can be used to stabilize bias and control thermal runaway by using the increased current flow to increase the voltage drop, thus reducing base-emitter voltage. However, if used with these devices, it will actually impair the self-limiting action of its negative temperature co-efficient. If temperature

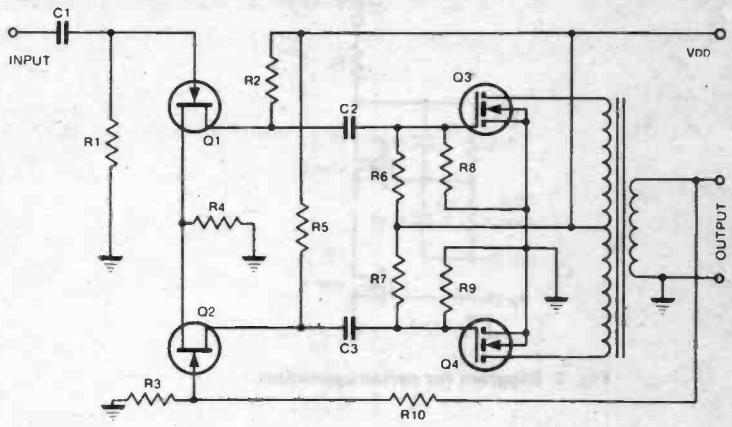


Fig. 12. Transformer-coupled output.

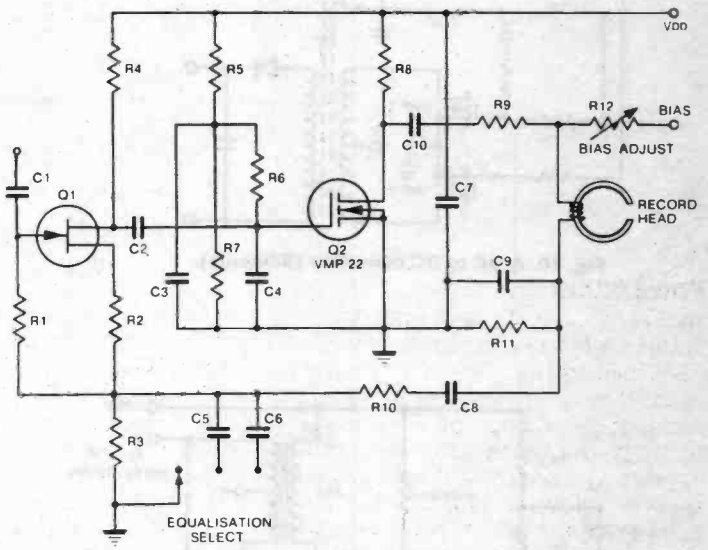


Fig. 13. Tape recording amplifier.

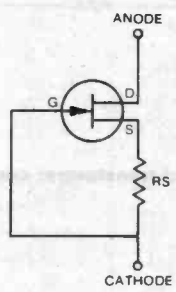


Fig. 14. A FET as a constant-current source.

rises due to nigh current, current flow is reduced. This would reduce the voltage drop across a source resistor, lowering the source voltage and increasing the gate-to-source voltage, causing an *increase* in current flow. The circuit would work great while it lasted – which wouldn't be for long.

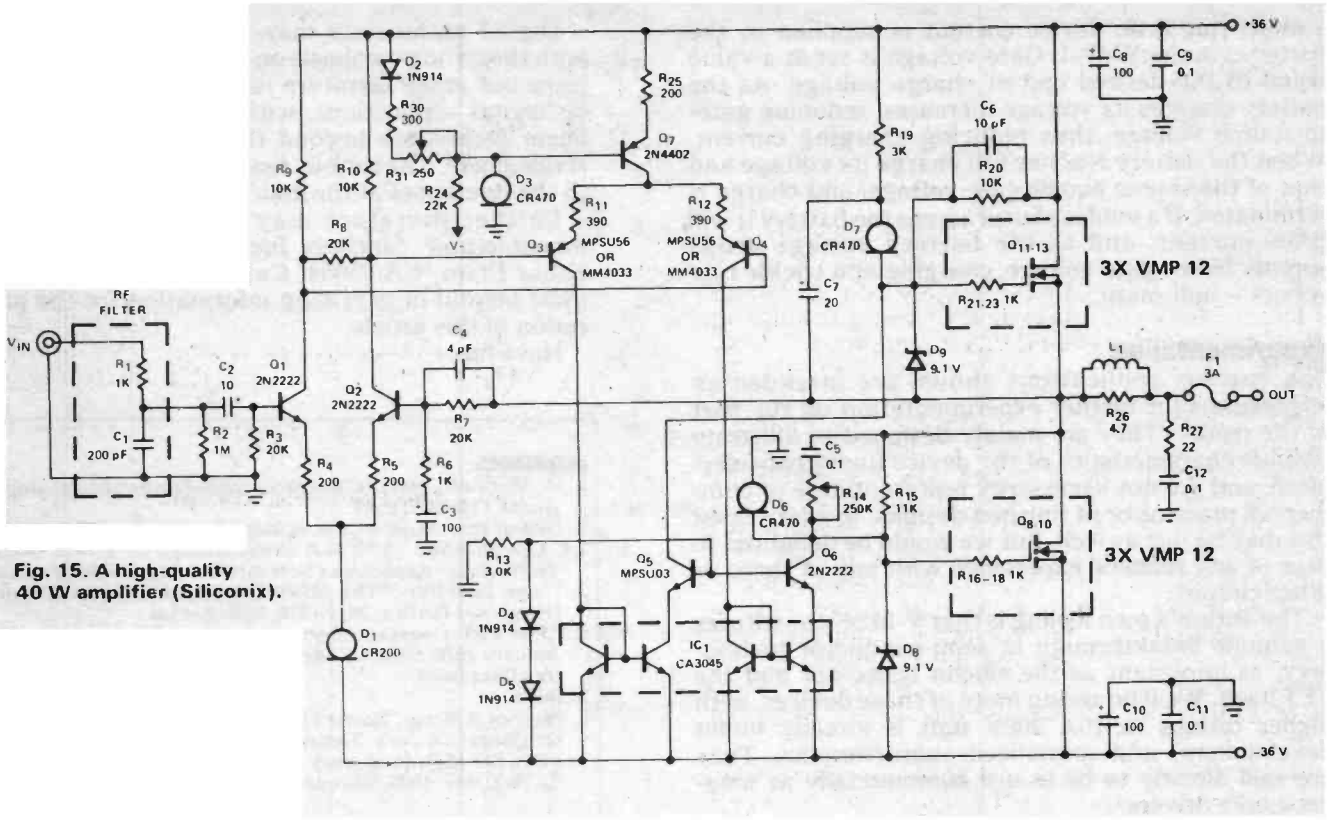


Fig. 15. A high-quality 40 W amplifier (Siliconix).

Power Amp

In Fig. 15 we have a high quality power amplifier designed by Lee Shaeffer of Siliconix Inc. (5) and described in their application notes. Output current capability is increased by using three VMP12s in parallel; providing for 6 amp current, 75 Watt dissipation and optimizing the load at 8 ohms. Q11-13 operate as a source follower, while Q8-10 form a quasi source follower. This is accomplished by applying local feedback from drain to gate via R14, R15, and driving the gate by a modified current source. This consists of a cascode circuit with a constant current diode as the load.

For the benefit of those not familiar with these devices, a constant current diode is really a FET connected internally as shown in Fig. 14. Since current in a FET is controlled essentially by the gate-to-source voltage, changes in load or in applied drain to source voltage have negligible effect since gate-to-source voltage is held constant. This is a current analogue to the zener diode and is described in detail in Siliconix literature (6).

The design is push-pull from input to output, thanks to differential circuitry throughout, prior to the drivers. Open loop distortion is low, bandwidth wide, allowing satisfactory performance with only 22dB of feedback.

Complete construction plans including PCB layout are available from Siliconix (7). A word of caution, however. Readers accustomed to construction articles in which the writer does everything but hold your soldering iron will find these plans rather sketchy. They consist of a spec sheet, schematic, board and parts layout, two paragraphs of construction suggestions, initial adjustments, and a parts list. Parts, generally, are specified as to value and rating, and that's it. These plans are excellent, but they assume some knowledge and experience on the part of the constructor. Regular 'eti constructors' should have little difficulty.

Finally, how about something elegant for its simplicity, such as the Tapered Current Voltage Limited battery charger shown in Fig. 16. This is especially useful with Ni-Cad batteries which are intended for stand-by use and are permanently on charge, such as

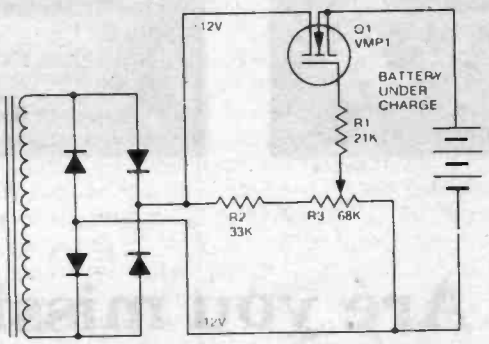


Fig. 16. Tapered-current voltage-limited battery charger.

electronic clocks. Overnight shut-downs of a few hours are occasionally but irregularly experienced. You know what this can do to clocks. Especially alarm clocks which are supposed to make noises, turn on radios, start the coffee at a pre-set time in the morning so you can go to work. Battery operation is not too satisfactory if the readout is on continuously, and Ni-Cads should not be on permanent floating charge.

With this little device current is supplied to the battery via the VMP-1. Gate voltage is set at a value equal to the desired end of charge voltage. As the battery charges its voltage increases, reducing gate-to-source voltage, thus reducing charging current. When the battery reaches full charge its voltage and that of the source equals gate voltage, and charge is terminated. If a load is placed across the battery it will draw current, and as the battery voltage drops slightly below gate voltage, charging at a trickle rate occurs – automatic.

Experimentation

The various applications shown are intended as suggestions for further experimentation on the part of the reader. They are mainly designed to illustrate various characteristics of the device under consideration, and are not necessarily representative of commercial practice or of finished designs. In some cases this may be just as well. But we would be delighted to hear of any readers' experience with any of these or other circuits.

The author's own feeling is that V-MOS constitutes a genuine breakthrough in semi-conductor technology, as important as the silicon transistor and the FET itself. We'll be seeing more of these devices, with higher ratings (a 10A 200V unit is already under development) and specialized characteristics. They are said already to be in use commercially as magnetic core drivers.

Digital enthusiasts may be somewhat impatient with the strong emphasis on audio applications in this piece but other literature has placed great emphasis on digital applications, with little attention paid to linear techniques beyond the 40 watt amplifier described here. The serious reader in all areas is referred to the references at the end.

Further literature may be obtained from the manufacturer, Siliconix Inc., 2201 Laurelwood Rd., Santa Clara, CA 95054, California. They have been most helpful in providing information for the preparation of this article.

Have fun.

REFERENCES

1. W. Marshall Leach: "Construct a Wide Bandwidth Preamplifier" Audio, Feb 1977, p. 39.
2. Nelson Pas: "Build a Class A Amplifier" Audio, Feb. 1977, P. 29.
3. 4. Lee Shaeffer: "VMOS-A Breakthrough in Power MOSFET Technology" Application Note AN76-3, May 1976, Siliconix Inc.
5. 7 Lee Shaeffer: "The MOSPOWER FET Audio Amplifier" Design Aid DA76-1, May 1976, Siliconix Inc.
6. "The FET Constant Current Source" Design Idea D171-1. January 1976. Siliconix Inc. Also Siliconix Field Effect Transistors Data Book.
7. Ref. 5.
8. Bascom H. King: "Power FETs" *Audio*, Feb. 1975, p. 42.
9. Ed Oxner: "A New Technology: Application of MOSPOWER FETs For High-Frequency Communications" Tecnhical Article TA.76-2, Nov. 1976. Siliconix Inc.

CHOOSING AND USING TRANSFORMERS

A mains transformer is often the single most expensive item in a project — H. E. Clayton of Reading Windings takes a close look at this often neglected item.

Transformers are used to increase or decrease either an AC voltage or an AC current level.

All transformers change both AC current and voltage levels simultaneously, but no transformer significantly changes power levels, as the input power equals the output power plus losses which are in general, negligible. Transformers can also be used to transform impedance from one level (in the primary circuit) to another level in the secondary circuit, the impedance transfer ratio being the square of the transformer turns ratio.

It is often possible to use transformers in the opposite mode to that for which they were designed e.g. by feeding into the secondary of a step down transformer and using it to step up in voltage. This will, however, usually give an output voltage below the rated value because the turns ratio is normally made less than the rated transformation ratio to compensate for voltage drops in the windings.

Power transformers can usually be operated at frequencies higher than that for which they were designed, e.g. a 50Hz transformer can be used at 60Hz, but not vice versa.

What we want is . . .

Before deciding on a transformer for a particular application, it is helpful to list one's requirements and to have some idea of what options there are. It is hoped that the following outline will help.

RMS input voltages and supply frequency: In addition to the nominal input voltage the maximum value to which this can rise should also be considered. Most transformers will operate satisfactorily at about 6% overvoltage for short periods of time but if it expected to exceed this figure it is advisable to increase the rated input voltage. Primary windings can be tapped to cater for several voltages but this adds considerably to the cost of the transformer and may detract from performance. Twin series — parallel windings on the other hand, although adding a little to the cost, do not substantially interfere with efficiency as all of the winding is in use for both series and parallel connections. They are however limited to dual input voltage applications where one voltage is twice the other e.g. 240/120V.

Output Currents and Voltages: Unless otherwise agreed, the nominal or rated output voltage is that at full load output current based on resistive load. Again, several voltages can be provided by tapping and, unlike the primary taps, several secondary tappings can be used simultaneously to supply a number of loads. If, however, there is a significant difference between the load currents at different tappings, it may be preferable to have separate windings.

NB: The information above is the minimum which must be decided by the user, all the following requirements may remain unspecified unless circumstances demand otherwise, always remembering that special features can add considerably to a transformer's cost.

Regulation (usually Maximum Value): The regulation is defined as the difference between a secondary terminal voltage on open circuit and the secondary terminal voltage at rated full load current.

Maximum permissible Temperature rise: This is often decided by the manufacturer rather than the user as it may depend on the materials used. Higher standard temperature rises are associated with lower ambient temperatures.

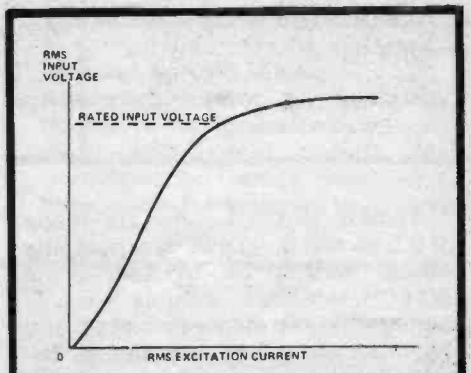


Fig. 1. Plot of excitation currents vs. RMS input voltage for typical transformer. The transformer should not be operated for long periods above the 'knee' of this curve.

Input Current (or Excitation or Magnetising Current): The no load input characteristic is shaped as in Fig. 1 and care should be taken not to use the transformer for long periods

with voltages much higher than the "knee" of the curve.

Electrical requirements: Limitations to distortion of secondary waveform, any special phasing requirements etc.

Insulation requirements: The basic standard requirement is for a 2kV RMS test between the input and output windings and between any winding and the core if accessible.

Impregnation etc: Transformers without hygroscopic materials (those that absorb moisture) are often varnish dipped while those using absorbent materials such as paper are varnish impregnated. Both of these processes are effective for minimising lamination vibration and sealing against ingress of moisture.

Dimensions: Any limiting dimensions and/or fixing centres.

Construction: Some of the common alternatives are described below.

What Core

Interleaved laminations are widely used for small power transformers, the most common shape being the no-waste 'E' and 'I' in which the 'I's are cut from the 'E's (see Fig. 2) and the coils assembled over the centre limb (shell type construction). These are available in .50mm and .355mm thickness in various grades of hot rolled silicon iron and in 0.355 mm grain-orientated silicon iron.

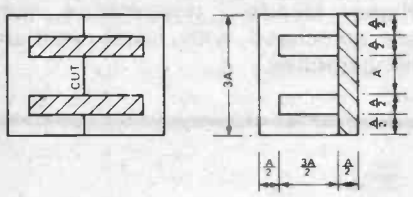


Fig. 2. No-waste E and I construction of transformer laminations.

Toroids and 'C' cores are made of 0.355 and 0.10 mm thickness, the thicker material being used in the 50-60Hz devices. Toroids have a highly efficient magnetic circuit and by virtue of their circular shape, low leakage flux. They are sometimes chosen because they can be used to make a "low profile" i.e. low height transformer.

Because the cost of toroidal transformers can be three times that of an E and I laminated transformer, a compromise between the two which is sometimes used for low profile units uses U and I laminations with the coils on the long limbs of the 'U'. (Core type construction).

Winding Things Up

Moulded bobbins are widely used for smaller transformers. They have the advantage that they can be wound on high speed machines. Insulation thickness between windings and core and between windings can be assured. The winding space factor (ratio of area occupied by active copper and total winding area) is high and terminal tags can be mounted on the bobbin cheeks. Certain bobbins may be fitted with shrouds encasing the windings and giving good mechanical and electrical protection.

Ending It All

The cheapest terminations are solder tags on the bobbin cheeks. For applications where solder connections are not convenient terminal blocks can be mounted on the transformer. For larger transformers terminal panels with turret lugs or bolted connections are used.

Mounting Up

Mounting brackets are available for the range of standard no-waste E and I laminations. They take the form of 'U' clamps with two hole fixing which are crimped on to the smaller sizes (up to about 50VA) and flanges and frames secured to the larger transformers with core bolts and providing four fixing slots on each of their four sides (universal mounting). At the small end of the range (up to about 5VA) pin terminations can be used for PCB mounting.

Electrical Performance

In its simplest form a transformer consists of an input and output winding magnetically coupled with an iron core. The windings represent an impedance in series with the load and the core can be considered to be an impedance shunting the load. The winding impedances cause voltage drops proportional to the load current and a watts (copper) loss proportional to the square of the load current. The core impedance does not directly produce a voltage drop but is associated with an energy (iron) loss approximately proportional to the square of the volts per turn for a fixed supply frequency. The total losses (copper and iron) determine the operating temperature rise of the transformer which is usually the most important factor limiting the use of the transformer.

Watts A VA

Although the transformer total losses depend on both voltage and current, they are independent of the phase factor. For this reason transformers are rated in maximum VA and not in watts although with resistive loads VA = watts.

Transformer windings also have "self inductance" which can be thought of as a reactance in series with the winding resistance and the load and is usually referred to as the "leakage reactance". This does not usually effect the performance of small power transformers (below about 100 VA size) particularly when used with resistive loads.

Physical Performance

As transformers increase in VA rating and physical size, the working flux density and the winding current density are reduced, but even over a relatively large range of sizes, the variation is small enough to assume that they are constant.

With this premise, it is interesting to consider the effect on various parameters of change in physical size for the same overall shape.

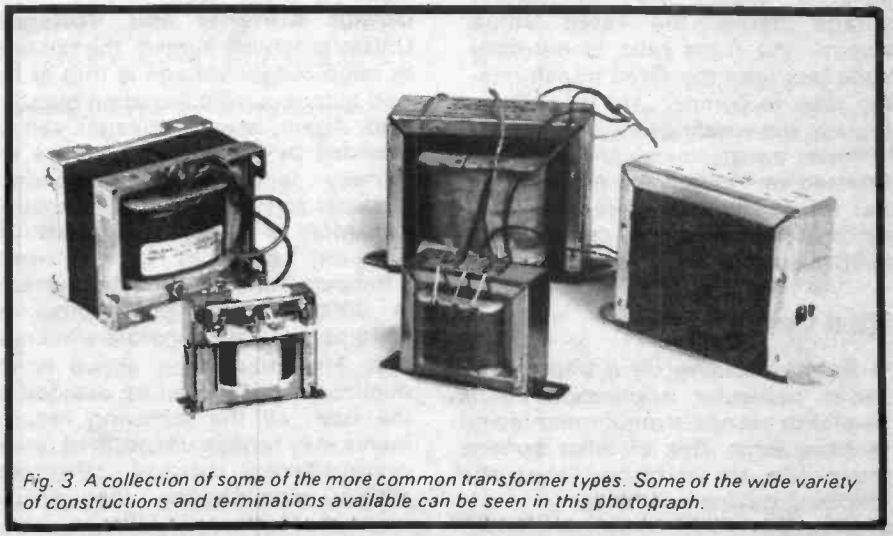


Fig. 3. A collection of some of the more common transformer types. Some of the wide variety of constructions and terminations available can be seen in this photograph.

We can show that

1) The regulation of small transformers with resistive loads decreases in inverse ratio to the increase in any linear dimension and
2) The reactive voltage drop increases while the resistive drop decreases linearly with dimensions.

Figure 4 shows the relationship between transformer VA rating, volume (or weight) and regulations. The volume here is the length × width × height, not the displacement. This is based on mains transformers using E and I no waste laminations and operating at 50 Hz. It is often possible to increase the output current of a power transformer beyond the rated value if one can accept a temperature rise higher than the designed value. Overloading the transformer in this way will, however, cause the output voltage to fall because of the increased voltage drops in the windings.

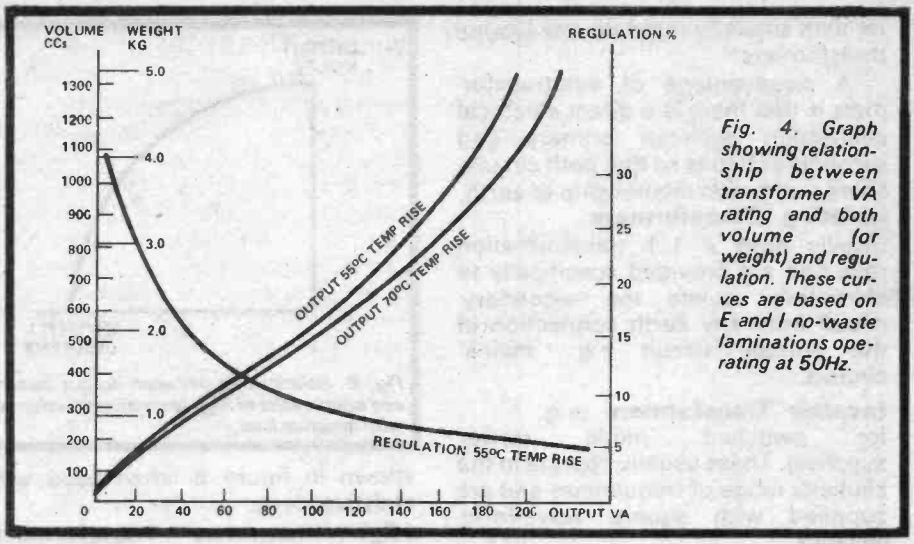


Fig. 4. Graph showing relationship between transformer VA rating and both volume (or weight) and regulation. These curves are based on E and I no-waste laminations operating at 50Hz.

Trying Time

The following tests can be used to establish basic transformer characteristics.

Turns Ratio: Apply a known voltage, less than the rated value, to the primary winding and measure the secondary voltage. Care should be taken, especially with transformers below about 20VA rating, that the instrument used does not impose a significant load on the transformer.

Excitation Characteristic Connect as in Fig. 5 and apply the rated input voltage to primary terminals and measure input current and voltage.

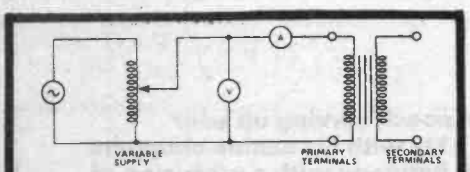


Fig. 5. Connections for the excitation or open-circuit test. The rated input voltage is applied to the primary and the excitation current is shown by A.

Winding Resistance Measure the primary and secondary DC winding resistances with a multimeter or Wheatstone bridge.

Phasing. Where windings can be interconnected e.g. with series/parallel designs, it is important to establish the relative polarity of terminations. This can be done by connecting the windings concerned in series, applying an alternating voltage to one and measuring the overall voltage (Fig. 6). If this measured voltage is greater than the applied voltage, then the windings are in phase. Conversely, if the measured voltage represents the difference of the two winding voltages the connection is in anti-phase.

It Takes All Sorts

Transformers Feeding Rectifiers. A common application for small transformers is to supply full wave rectifier circuits including capacitor input filters. The most common are the bridge and bi-phase circuits shown in Fig. 7.

For the same power rating, the transformer for the bi-phase circuit will be larger than that for the bridge circuit because its secondary produces twice the voltage and carries current during each half cycle only. Ideally the secondary winding for the bi-phase transformer occupies $\sqrt{2}$ times the space of the primary winding. Although transformer cost is higher, rectifier costs are lower for the bi-phase circuit.

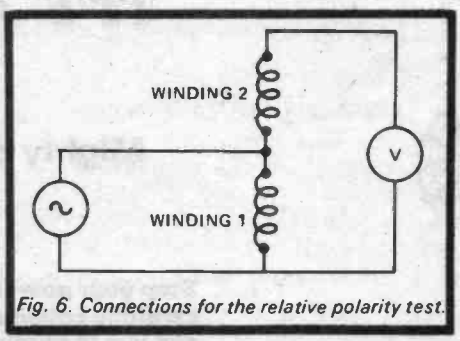


Fig. 6. Connections for the relative polarity test.

The relationship between the average DC voltage and the RMS secondary voltage is complex and is dependent on the smoothing capacitance, the supply frequency, the transformer series impedance and the load impedance. Curves illustrating this and other relevant relationships are published by rectifier manufacturers but neglect the effect of transformer leakage reactance which may be significant on some larger transformers. Because the waveform of the transformer current is very 'peaky' the effective reactive volt drop is greater than may be expected by considering RMS values.

Autotransformers have a single tapped winding to provide both input and output circuits. With transformation ratios near unity, autotransformers can be much smal-

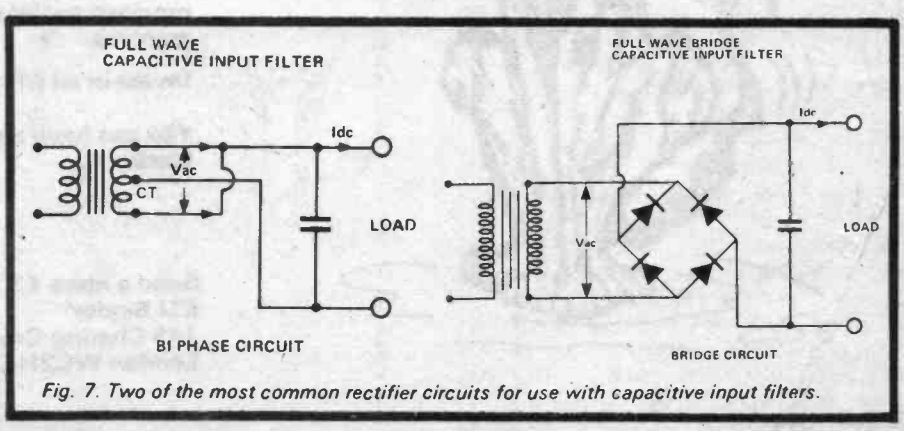


Fig. 7. Two of the most common rectifier circuits for use with capacitive input filters.

ler than similarly rated double-wound transformers.

A disadvantage of autotransformers is that there is a direct electrical connection between primary and secondary circuits so that both circuits share a common relationship to earth.

Isolating Transformers usually have a 1:1 transformation ratio and are provided specifically to electrically isolate the secondary circuit from any earth connection in the primary circuit e.g. 'mains' circuits.

Inverter Transformers (e.g. for switched mode power supplies). These usually operate in the kilohertz range of frequencies and are supplied with square wave-form voltages.

High Impedance Transformers are used for a variety of purposes a few of which are mentioned below.

Short-Circuit Proof transformers are designed to continue in operation without damage when the secondary terminals are short-circuited. Small transformers (below about 5VA size) are sometimes made with sufficiently high winding resistances to restrict the short circuit current but with larger transformers an adjacent winding structure is used with an intermediate magnetic shunt. This gives an output characteristic as shown in figure 8 when used with resistive loads.

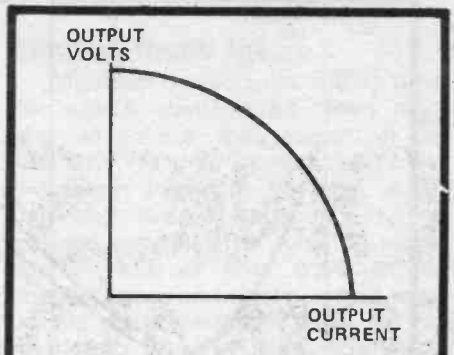


Fig. 8. Relationship between output current and output volts of high reactance transformer with resistive load.

High Frequency Transformers. The foregoing is concerned with transformers operating only at a constant supply frequency and with sinusoidal waveforms. Transformers used in communication circuits are required to handle a wide range of frequencies and waveforms, although any repetitive waveform can be expressed as a series of sine wave components. Such transformers are often used in an *impedance matching* role. It is well known that to transfer the maximum amount of energy into a load from a voltage source the load impedance should equal the source impedance.

SCREENING

Stray magnetic fields produced by power transformers can cause hum in high gain amplifiers in the same locality. Screening around the power transformer is not normal because a large percentage of the stray flux, which is emitted in all directions, would strike the screen at right angles and pass through it rather than be diverted. On the other hand inputs (e.g. microphased transformers) are often enclosed in a screen of magnetic material to reduce pick-up.

PRODUCTION METHODS

Coil winding techniques and machinery have improved immensely in recent years. Unfortunately it is not always possible to make the best use of these improvements which are mainly geared to high volume production of standard products. Although some degree of standardisation in small transformers has been achieved equipment designers still expect transformers to be tailor-made, often in small quantities, to their particular electrical and dimensional requirements.

Summarising, before seeking a special transformer, consider first if readily available standard transformers can be used. It will often be cheaper to use two or more standard transformers than one special unit.

DIGITAL ELECTRONICS BY EXPERIMENT

IAN SINCLAIR'S SERIES IS DESIGNED TO IMPART THEORETICAL KNOWLEDGE THROUGH SIMPLE PRACTICAL EXPERIMENTS.

Many experienced constructors with several acres of transistor circuits behind them still fight a little shy of using digital integrated circuits. The reasons for this are not difficult to see. Most of the transistor circuits with which an experimenter learns his trade are fairly simple and show rather well how a transistor works, giving a feeling of confidence to the user.

The many excellent projects using digital integrated circuits which have been published do not give any such help to the constructor, however. They may be comparatively easy to build on a prepared PCB, they may even be reasonably easy to understand, but they *do not* give the constructor the experience which enables him to design confidently with ICs.

This series is intended to remedy that deficiency, so that the reader will gain a firm grasp of the principles of digital IC behaviour, how they work, and also a considerable amount of "hands-on" experience on a board designed to make experimenting with digital ICs particularly easy. We shall confine ourselves to the smaller scale ICs so that nothing as involved as a microprocessor will be used — the components however are chosen so that they give a good range of experience with some useful devices.

One and none

We can assume that any reader of ETI will already have *some* knowledge of what digital circuits are about, but perhaps a very brief reminder may be of some use. Digital ICs are made up from transistor circuits of very high gain, designed to run with inputs and outputs which can take up only two possible states which we call 1 and 0. In most applications, 0 will mean a voltage very near to earth potential, and 1 near to the full supply rail.

The ICs we shall use in this course will be from the well-known TTL series, developed by Texas, and also available from several other manufacturers. There are several reasons for this: the devices are readily available and at very low prices and advertised in ETI, they are much less easily damaged electrically than the alternative CMOS.

Going places with nothing

When an input of a TTL gate is left open-circuit it automatically reverts to a "1". The reason for this is that the input to TTL gates is to one emitter of a multiple-emitter transistor whose base is connected through a limiting resistor to the +5 V line. Leaving an input o/c means that the emitter terminal will take up the same voltage as the base terminal. This cannot be done when CMOS devices are used.

For our course on digital electronics we shall need seven digital ICs and one "jumbo" display, a full inventory of semiconductors being shown in the parts list and in addition we shall also need a few other assorted components as noted therein. Where a source of 5 V supply is not available, a stabiliser can be included on the board, so that the experiments can be carried out using a car battery or any dc supply in the 6 V to 12 V range. Note that the current taken will be up to 350mA.

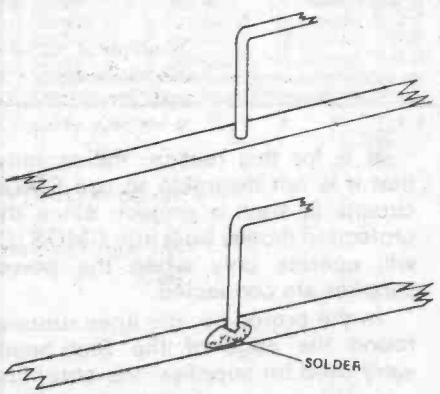


Fig. 1. The method of attaching components to the Blob Boards. The "leg" can be simply bent to one side and then solder "blobbed" over the lead to hold it. Since the boards are tinned, and the leg ought to be, a sound joint is ususally obtained.

Heart to heart

The heart of the whole project is the circuit board on which the ICs and all other components can be mounted. This is one of the series of "Blob Boards" in this case the ZB-8-IC. Blob Boards consist of wide strips of tinned copper on the usual insulating board, and their main feature is that components are mounted on the same side of the board as the strips.

This, of course, is not a new principle in digital IC construction, since this method has been used for some time where digital ICs are mounted on double-sided boards.

Housing and boarding

The ZB-8-IC as its name suggests, has mounting pads for eight ICs, including the display which we have specified. The suggested layout for the ICs is shown in Fig. 3, where we can see that the top left hand corner houses the 7414 Schmitt inverter, and the 7400 Nand gate; the top right hand corner has the two 7476 J-K flip-flops. At the bottom left hand corner, we have a 7494 shift register and the 7490 decade counter. The bottom right hand corner contains the 7447 BCD-7 segment decoder-driver and the display. All of the ICs have conventional DIL fourteen or sixteen pin bases, but the display has a base which is an eighteen pin type with several pins omitted, so that this will just fit the pads on the board. The spacing between the lines of pins (0.6") is a little on the large side compared to the other ICs, but with

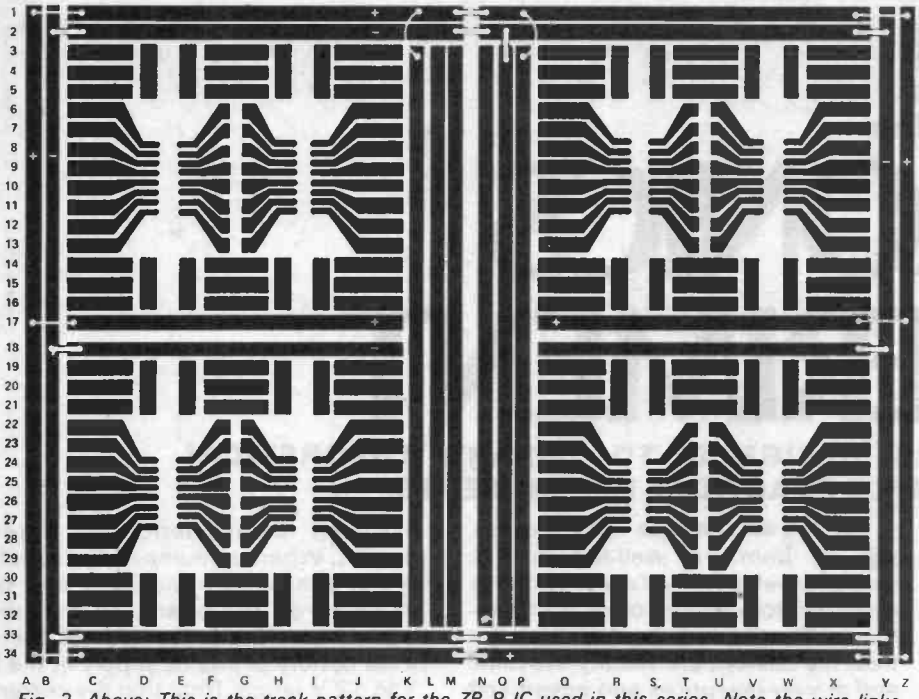


Fig. 2. Above: This is the track pattern for the ZB-8-IC used in this series. Note the wire links which need to be made in order to more easily facilitate application.

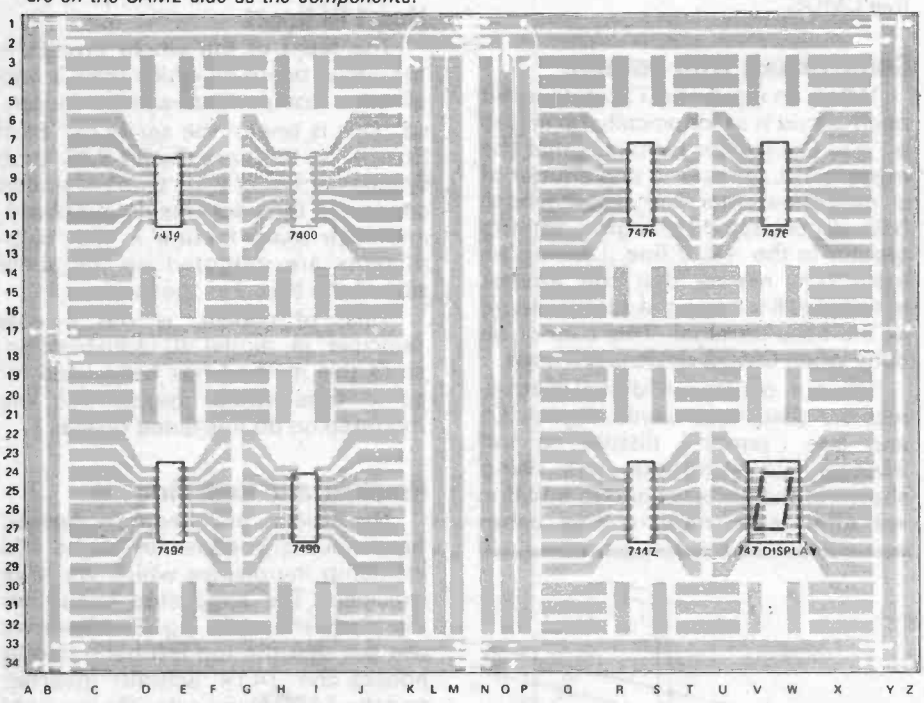


Fig. 3. Below: Components in place on the board. Note that unlike our usual overlays, the tracks are on the SAME side as the components.

care it can be accommodated. In the circuits which we are using we shall not normally need the decimal point on the display, but its connection may as well be made just in case.

Before any experiments are started then, it is advisable to solder all the ICs and the display on to the board, so that this does not have to be done when it becomes cluttered by other components. Since each circuit mounts on to pads which are isolated unless other connections are made, no harm is done by leaving an IC soldered on to the board.

It is for this reason, incidentally, that it is not desirable to use CMOS circuits in such a project, since the protection diodes built into CMOS ICs will operate only when the power supplies are connected.

In the prototype, the lines running round the edge of the Blob-board were used for supplies, the outer line taken as the positive 5 V line, and the inner as earth. It is quite convenient also if the shorter lines running across the board between each pair of IC pads are also used as 1 and 0 lines as well. The vertical lines at the centre of the board may also be used. If a stabilised 5 V supply is available for operating the board then little else needs to be done other than connecting the power pack to the lines at the edge of the board.

Fig. 4. Top Right: The layout for the digital TTL series. This is looking down at the device from above. Usually, but NOT always power is applied to pin 14 and pin 7 is earthed.

Fig. 5. Bottom: Positioning the ICs onto Blob-Board pads. Make sure the legs line up.

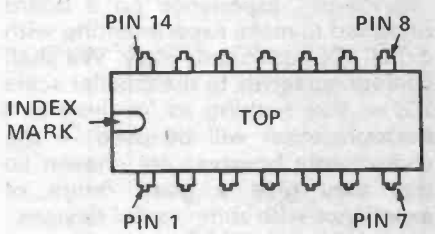
Stable lines

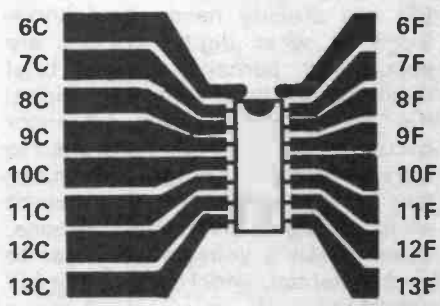
If a stabilised supply is not available, however, a stabiliser should be built on to these lines. A suitable circuit is shown in Fig. 7 using a BD131 and 2N697, both of which are readily obtainable.

It is extremely important that TTL circuits should not be operated at voltages above 5.25 V AT ANY TIME, since the inputs to TTL circuits are to the emitters of transistors, with the bases connected to the positive supply. If the inputs to the emitters are earthed (at 0V), too much current will flow in the base-emitter junctions, though if all the inputs are earthed, over-voltage is much less likely to cause much harm.

Led about the board

Above and below each mounting pad there are several short pads usually three horizontal and two vertical, and these are very useful for mounting components such as LEDs, which are used to indicate the state, 0 or 1, of any output. Note that on most LEDs there is a flat portion of the plastic case near the leadout wires which indicates which leadout wire is





HOW IT WORKS

The action of the circuit is as follows. The connection of the 1k resistor between the collector and the base of the BD131 normally ensures that the BD131 remains conducting, but the 4.3 V zener diode ZD1 will set the voltage at the base of the 2N697 at about 4.3 volts less than the voltage at the emitter of the BD131. The 2N697 will start to conduct when its base voltage is approximately 0.6 V positive to its emitter voltage, that is when the emitter of the BD131 is at about 4.9 V positive.

An increased voltage here will cause more current to flow in the 2N697 (each 80 mV increase of voltage at the base of a conducting transistor causes the collector current to rise tenfold), drawing current through the 1k resistor and therefore lowering the voltage at the base and emitter of the BD131; in this way the circuit stabilises at about 4.9 — 5.0 V. The second zener diode, ZD2 is a 5.6 V type which is a safety measure should the BD131 ever fail to a short circuit. In the event of such failure, ZD2 could absorb the extra current until the power supply fuse melted. If a battery is used as a source, a 500 mA fuse should be included.

Later models of the ZB-8-IC Blob Board may have a different track layout to that shown here. This should only affect the positioning of the voltage stabiliser components.

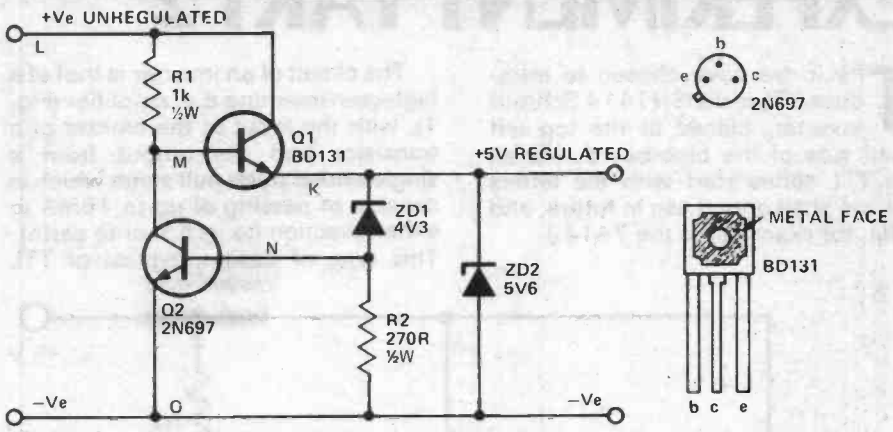


Fig. 7. Above: Circuit diagram for a suggested power supply to run the experiments, and, Fig. 8, below, a layout to build this circuit onto the board itself.

the cathode. Since we are using the LEDs to light on a "1" state, the cathode of each LED is connected to earth, and the anode through a limiting resistor to the IC output. This resistor value is higher than we would normally use, but suits this application, as we do not want the LEDs to draw too much current from the IC outputs. When we come to use the display, we shall also use large value limiting resistors.

With all the ICs mounted in place, we are ready to start our work.

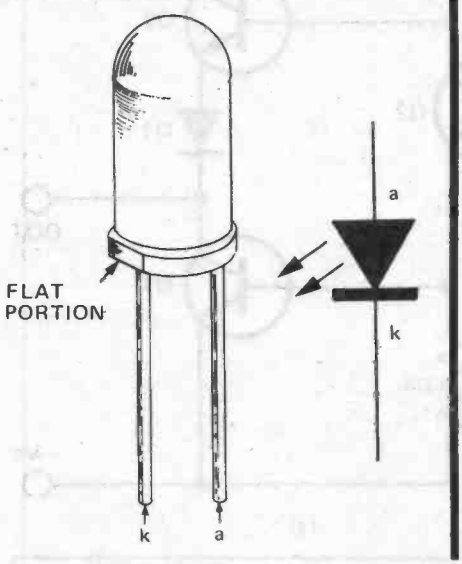
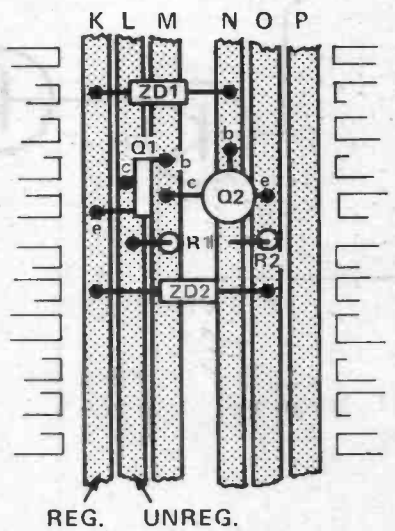


Fig. 6. Identifying led connections has caused many a paralysed moment of doubt-look for the flat bit, if there's one present then your problems are over.



PARTS LIST

COMPONENTS NEEDED FOR THE SERIES

Note: Only the essential basic components are listed here. For various additional suggested experiments, additional resistors and capacitors will be needed; these values will be critical.

SEMICONDUCTORS
1 x SN7414N
1 x SN7400N
2 x SN7476N
1 x SN7494N
1 x SN7490N
1 x SN7447N
1 x 747 Display

OTHER COMPONENTS
1 x 0.1uF
1 x 1.0uF
1 x 10uF
1 x 100uF
1 x 680uF
1 x 1000uF
All the above 10V working, or more.
10 x 470R resistors, 0.125W or more
6 Miniature push-button switches (Sintel)
5 metres of single-core wire

STABILISER COMPONENTS
1 x 2N697
1 x BD131
1 x 4V3 Zener Diode
1 x 5V6 Zener Diode
1 x 270R 0.5W
1 x 1k, 0.5W

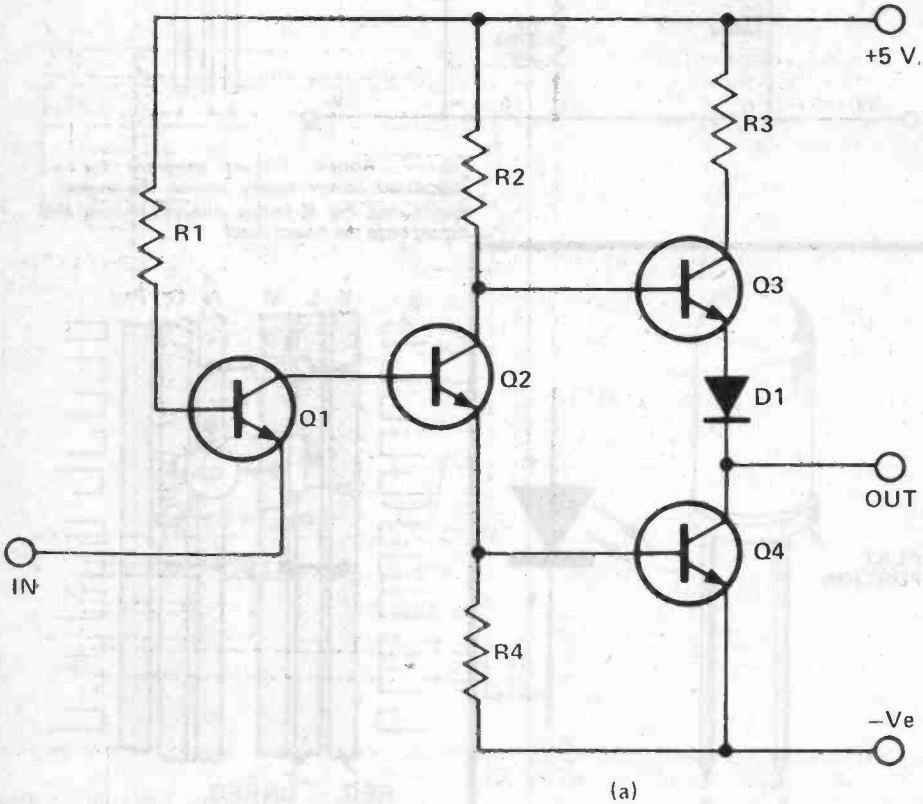
BOARD
1 ZB-8-IC Blob-Board

For a few applications in later parts of this series, a silicon NPN transistor may be used as an alternative to some long stretches of wiring (to connect a reset terminal on a counter). For this application, any working small signal type is suitable.

DIGITAL ELECTRONICS BY EXPERIMENT PART 2

The ic we have chosen to introduce TTL is the SN7414 Schmitt inverter, placed at the top left hand side of the blob-board. (As all the TTL series start with the letters SN, we shall omit these in future, and refer, for example, to the 7414.)

The circuit of an inverter is that of a high-gain inverting d.c. amplifier (Fig. 1), with the input at the emitter of a transistor and the output from a single-ended push-pull stage which is capable of passing of up to 16mA in either direction (to + 5 V or to earth). This type of design, typical of TTL circuits, has several important implications for us.



(a)

"Valve salesman were you? I used to sell computer time."

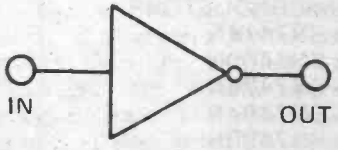
Source or sink

One important result is that the input impedance is fairly low when the input stage is conducting. If the input is left floating, the connection of the base of the first transistor to + 5 V will ensure that the emitter terminal will also be at high (+5V) voltage: The first transistor will be cut off in this state. The normal action of an inverter is that a high (or "1") input produces a low ("0") output, so that Q_2 is switched on by the high voltage at the collector of Q_1, and connects the output terminal to earth through Q_4. As mentioned above, this will allow a current of up to 16mA to pass from a positive source; in TTL language, the output stage will sink a current of up to 16mA.

Thank you fans

When we connect the input of the inverter to earth (0), what we are doing is to earth the emitter of Q_1, with the base still connected, through its current limiting resistor, to + 5 V. When this is done, a current of about 1.6 mA (set by the value of the limiting resistor) will flow from base to emitter, and it is very important that any resistance between the emitter (input) and earth should be small enough to prevent the emitter voltage rising above about 0.5V in normal use. This is ensured when we drive a TTL input from the output of another TTL device, since a TTL output can sink a current of up to 16 mA, the current from ten inputs, without the emitter voltages rising too high for reliable operation. This is referred to as a "fan-out" of ten at the output.

Since in these circuits we are interested only in high and low signal levels, we must make sure that there is no uncertainty about either of these



(b)

Fig. 1. A typical TTL inverter circuit (a). The value of R1 is about 3k, to limit the base current to 1.6mA. (b) Symbol.

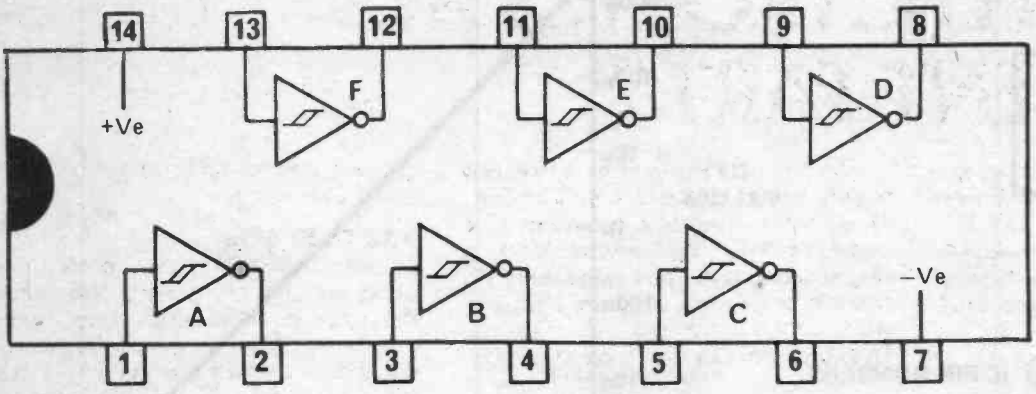


Fig. 2. Pin-out of the SN7414N Hex Schmitt inverter.

levels, and the usual TTL limits are: maximum of 0.8V for the low; minimum of 2.2 V for the high. We prefer if possible not to approach these limits too closely, and if we drive a TTL input from any other type of output, we must be sure that the source impedance of the driver output will be low enough to allow a current of 1.6mA to be sunk at a voltage level of 0.5V or less; this corresponds to an output impedance of 300R or less.

Starting work

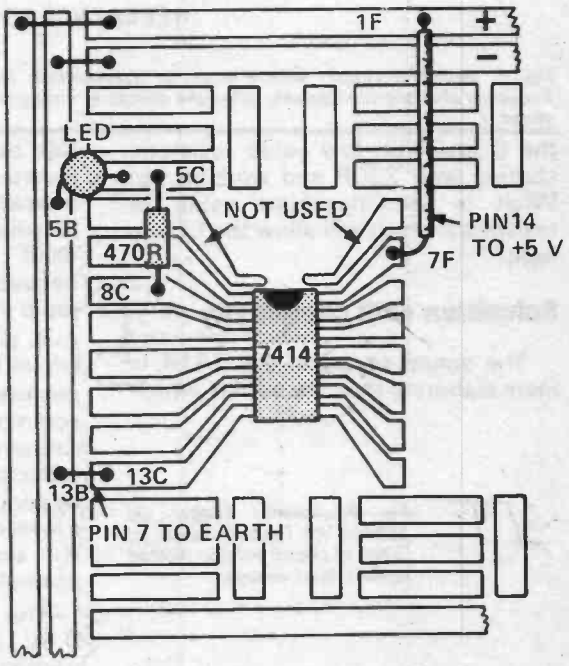
Ensure that the 1 and 0 lines on your blob-board are fully linked up and, if you are using it, connected to the stabilised supply. Join + and — leads to the power supply. If you have a separate stabilised supply, these leads, which should be colour coded, will connect directly to the 1 and 0 lines on the board. If you are using the built on stabiliser, the leads should run to the stabiliser input.

With no other connections made (none of the ICs wired to 1 or 0 lines) ensure that the voltage between lines 1 and 0 is between 4.75 V and 5.25 V with the supplies on. Switch off again. This check should be repeated whenever the board is used from a variable voltage supply, since TTL circuits will be damaged if any input is taken to 0 with the applied voltage too high.

Four for four uses

Connect the supplies to the 7414, pin 14 to +5V, pin 7 to earth. These connections, like all the connections which follow, are made by soldering short lengths of insulated wire between pads on the blob-board, as shown in Fig. 3. These connections, once made, can be left permanently.

Fig. 3. Connections to + and — lines using wires. This also shows the LED and its limiting resistor (Fig. 4) in place.



(With no other connections made, the IC will draw a current of about 85 mA.)

Now connect a 470R resistor and an LED to form the circuit of Fig. 4. This is done by tinning each end of the resistor and LED leadout wires, and then butting these tinned wires, in turn, against the blob-pad and touching wire and pad with a hot iron until the lead "blobs" into place. For this particular joint, we can use a spare pad, as shown in Fig. 3, with the resistor connected from pin 2 of the 7414 to the spare pad, and the LED connected from the spare pad to the 0 line. Note that the LED case is usually marked with a flat section at the wire which should be connected to the 0 line.

The LED will now light when the output of No 1 inverter (there are six inverters in the pack) is high. Switch on — the LED should remain unlit, since with the input, at pin No 1, floating high, the output will be low. Now check what happens when pin 1 is temporarily earthed through a wire link (no need to solder) placed with one end on the pin 1 blob-pad and the other end on the 0 line.

Bridge over troubled pads

Remove the wire, and try bridging between the blob-pad for pin 1 and

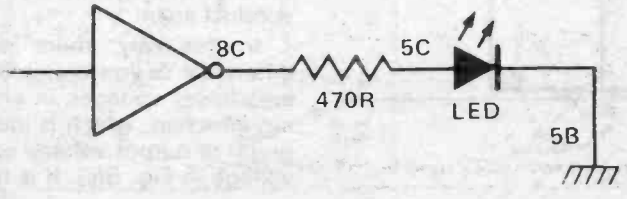


Fig. 4. LED indicator circuit.

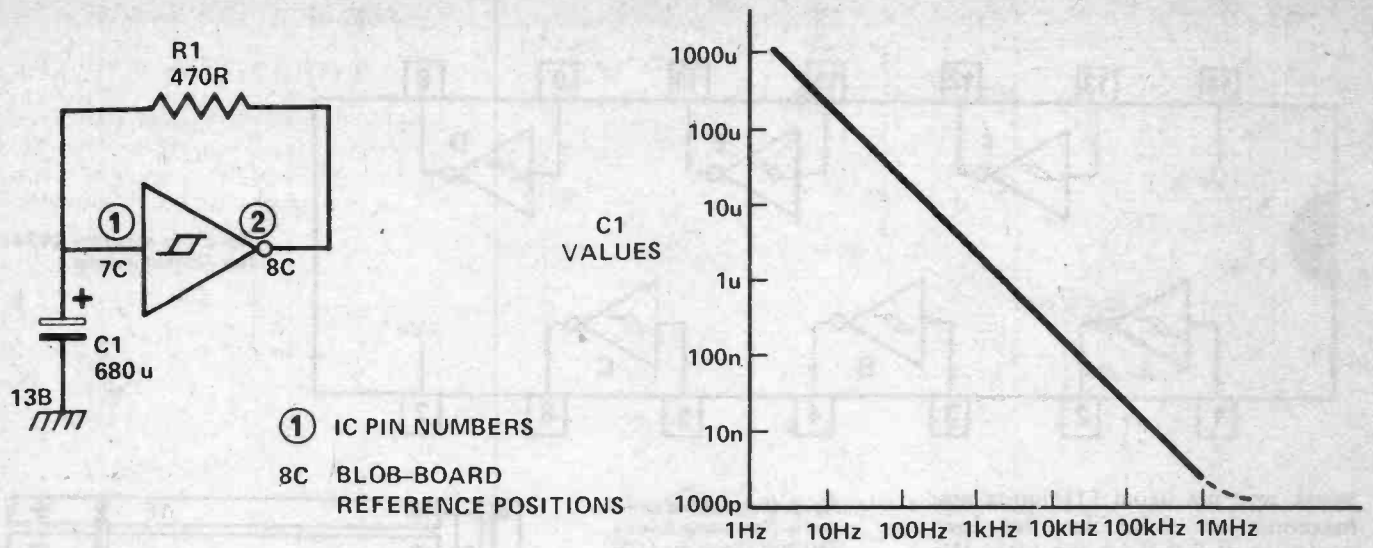
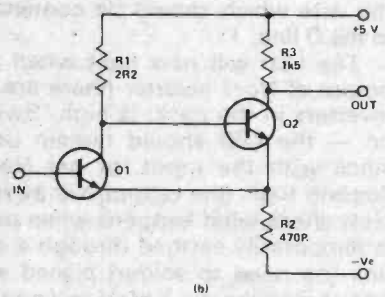


Fig. 6. Oscillator circuit, with a graph of approximate frequency against capacitor value. The frequency changes considerably when the operating voltage is changed, also as the resistor value is varied.

the 0 line with low value resistors, starting with 220R and working up. What is the maximum value of resistance which will allow the LED to light?

Schmitten with complexity

The actual circuit of the 7414 is more elaborate than the outline which has been shown in Fig. 1. These inverters are Schmitt trigger inverters, indicated by the symbol of Fig. 5(a), in which some positive feedback is used to make the changeover between 1 and 0 very much more rapid than that of an amplifier alone.



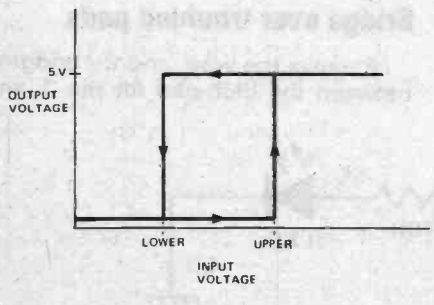


Fig. 5. Schmitt Trigger. (a) Symbol. (b) Typical circuit. (c) Graph of output voltage plotted against input voltage.

A simple discrete Schmitt trigger circuit is shown in Fig. 5(b), with the positive feedback applied by using a common load, R_2, for the two emitters. With the base of Q_1 at 0, the collector of Q_1 will be at 1, and Q_2 will be conducting, with its base voltage at a level decided by the values of R_1 and R_2, say 1.3V for the sake of an example.

The emitter voltage will be about 0.6V (since we are using silicon transistors) less than the base voltage of Q_2. If we now slowly increase the voltage at the base of Q1, nothing will happen until we reach a level of 1.3V in our example, at which level Q_1 will start to conduct.

When this happens, the voltage at the collector of Q1 starts to drop, reducing the base voltage of Q_2. Since every 80 mV drop on base voltage causes collector current to reduce to one tenth of its previous value (a useful rule and true for all silicon transistors), Q_2 will rapidly cut off, with the current now switching to Q_1 because of the positive feedback through the emitters.

If the base voltage of Q_1 is reduced again, it must be to a value less than the base voltage of Q_2 before Q_2 can conduct again.

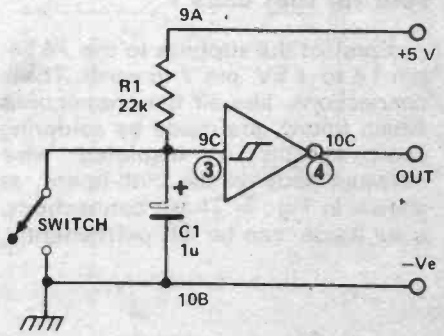
In this way, there is a voltage difference or *hysteresis* between the switchover voltages in either switching direction, which is indicated on a graph of output voltage against input voltage in Fig. 5(c). It is the shape of this graph which is used as the symbol for a Schmitt stage.

Slow, slow, quick quick . . .

Since the normal type of TTL circuit consists of a very high gain d.c. amplifier, there is a risk of positive feedback, causing high frequency oscillations, if the amplifier is ever operated, even momentarily, in a linear region, that is with the input biased so that the output voltage is between 1 and 0, or slowly changing. There is no problem if the change between 1 and 0 is fast, 30 ns or so, but slow in this context can mean 1 µs!

Slowly changing waveforms are most likely to be found when other circuits such as photocell amplifiers, microswitches or tacho-generators are connected to TTL inputs. This is an interface problem. Using a Schmitt stage at the input solves this, assuming we have a low enough impedance to drive the Schmitt, since the Schmitt action will give a 30 ns rise or fall time at its output for any

Fig. 7. Switch de-bouncing circuit.



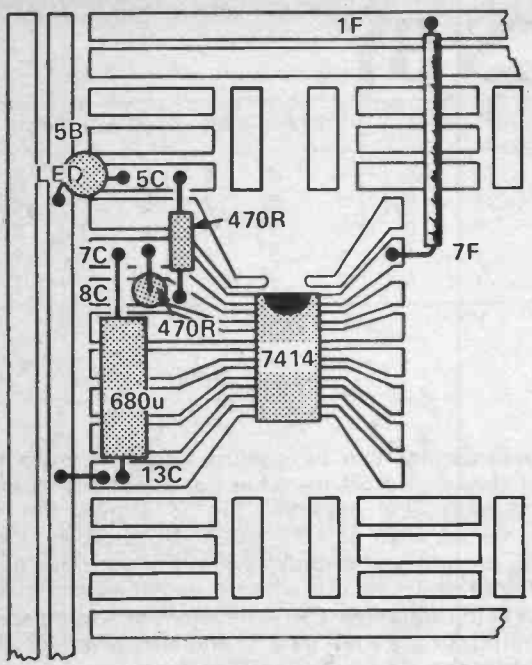


Fig. 8. Layout of the oscillator circuit on the Blob-board.

type of input, however slowly changing. Once the Schmitt has triggered, a comparatively large voltage swing is needed to make it change back. A Schmitt stage with high input impedance is also available (SN72560).

They call it de bounce

One of the unique features of this type of stage is that it can very simply act as an oscillator or as a switch de-bouncer. Oscillator action is achieved by connecting a resistor of between 330R and 820R between output and input, with a capacitor between input and earth. The circuit is shown in Fig.6. The output waveform is a square wave with very short rise and fall times, and unequal mark and space times.

When mechanical switches are used to provide waveforms for TTL circuits, contact bounce may cause problems. It occurs as contacts close, and causes a TTL input to be left briefly floating during the time of the bounce.

The effect of this can be to cause several output pulses from the switch where only one is intended. This is harmless if the switch is simply setting d.c. levels, but causes errors if the pulses are being counted. To *de-*bounce a switch, the circuit of Fig.7 can be used. The principle is that the time constant is longer than the bounce time of the switch, so that the voltage change when the contacts bounce is small, less than the hysteresis of the Schmitt circuit, hence no change in the trigger output when the bounce occurs.

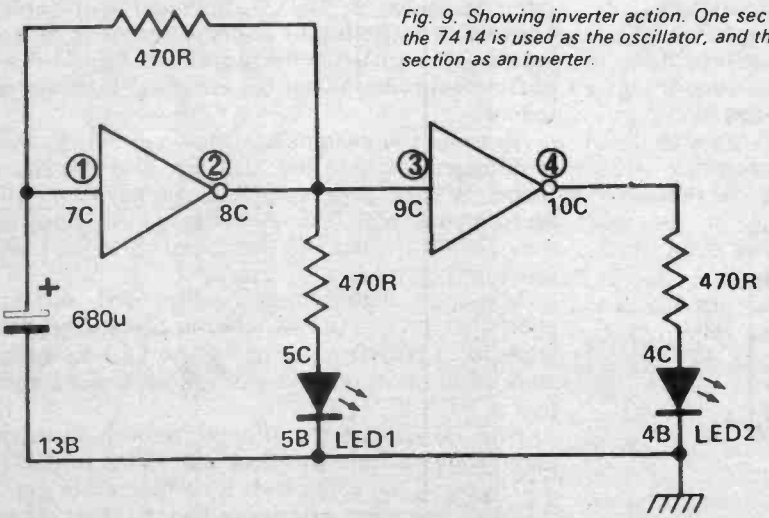


Fig. 9. Showing inverter action. One section of the 7414 is used as the oscillator, and the next section as an inverter.

Back to the Blob-Board

Using unit 1 of the 7414, make up an oscillator using a 680R resistor and a 680 µF capacitor as shown. Keep the connections previously made to the LED, since this can now be used to check that the oscillator is working.

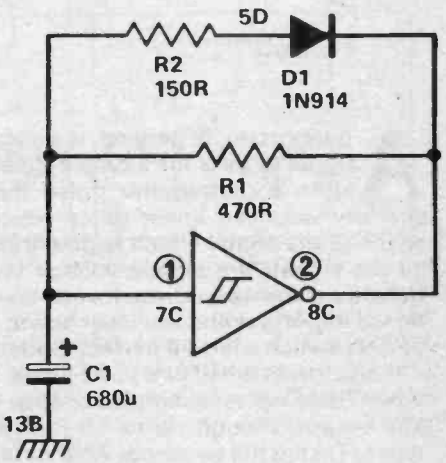


Fig. 10. Modification of the oscillator circuit for equal mark-space ratio. This is not needed for any of the applications in this series.

Estimate the frequency by counting the number of LED flashes in one minute, and then dividing the number counted by 60. Demonstrate the inverter action by using unit 2 as shown in Fig. 9. Wire a connection from pin 2 to pin 3 of the IC, and a 470R resistor from pin 4 to a spare pad. Connect another LED between this pad and earth to indicate when unit 2 output is high. Switch on again, and the two LEDs should blink alternately.

The oscillator can be modified for equal mark-space ratio by using the circuit of Fig.10. Some trial and error is needed to find the correct resistor value.

Organ Bank

Note that the 7414, with its six separate inverter circuits, can be used as the oscillator for an electric organ. Two 7414s will give a basic twelve note scale, and dividers can be used to produce lower frequencies.

Later in this series, the 7414 units will be used as oscillators to provide slow clock pulses, as inverters, and as switch de-bouncers. The connections made during this month's experiments can be left in place.

DIGITAL ELECTRONICS BY EXPERIMENT PART 3

A gate circuit, in general, is a circuit which will allow a signal to pass for a time defined by another signal, often a rectangular pulse (Figure 1a). In linear circuitry we need linear gates which do not affect the shape of the signal which is gated, but in digital circuitry all the signals are steady voltage levels, 1 or 0, or fast transitions between these levels, so that speed of operation is important and *no* linear action is needed. Ideally, a perfect switch is also a perfect digital gate.

Logic gates are of two basic types, the AND and the OR type. The simplest examples of each have two inputs and one output, though up to 13 inputs are found in some types. Taking the two input AND gate, the output is a logic 1 when, and only when, both inputs are also at logic 1 (A *and* B are at 1); the output is zero for any other combination of inputs. The two input OR gate gives a logic 1 output when *either* input is a logic 1, or when both are at logic 1 (A *or* B *or* both).

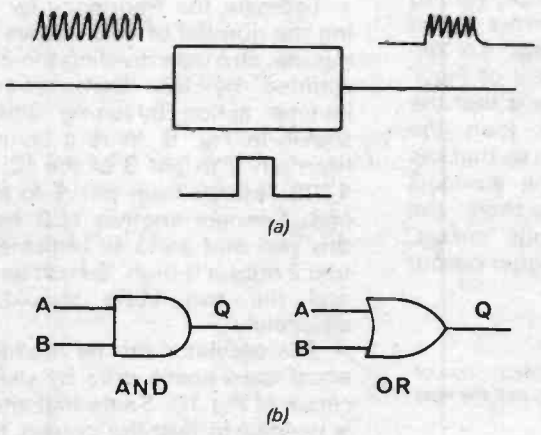


Fig. 1. Gates. (a) General gating action. (b) Logic gate symbols.

AND–GATE		
A	B	Q
1	1	1
1	0	0
0	1	0
0	0	0

(a)

OR–GATE		
A	B	Q
1	1	1
1	0	1
0	1	1
0	0	0

(b)

Fig. 2. Truth tables. (a) AND-gate. (b) OR-gate.

These actions can be summarised in a truth table which shows at a glance what combinations of inputs and outputs are possible. Fig 2 shows the truth tables for the AND and OR gates. Truth tables, though useful, become rather bulky when the gate has a large number of inputs, so that a better way of memorising the action is to remember that only when all inputs are 1 is the output of the AND gate 1, and only when all inputs are zero is the output of the OR gate zero.

NAND and NOR gates have outputs which are the inverse of the AND or OR gates respectively, as the truth tables of Fig. 3 show; internally these gates are AND/OR gates with inverters at the outputs. Another gate encountered at times is the exclusive-OR (XOR) which has the truth table and symbol shown in Figs. 3c, d. Note that the action is that of the OR gate, except that the output is 0 when both inputs are 1.

Working over a 7400

The second IC we shall deal with in this series is a 7400 quad NAND gate. This consists of four separate two-input NAND gates, and like all the other ICs used in this series is a TTL circuit. An unconnected input will therefore float to logic 1, and will need a current of 1.6 mA to be sunk to hold it down to logic 0.

Start work on this gate by connecting the power supply leads. Pin 7 is taken to the negative line by a wire connection, and pin 14 is similarly taken to the +5 V line. The connections to the gates are shown in Fig. 4; we shall start by using gate 1.

Connect a 470R resistor between pin 3 and a spare pad, as shown in Fig. 5. Now connect another LED between the spare pad and the zero line to act as an indicator to light when the output is at logic 1 — we could obtain inputs by soldering in wires, but this is rather tedious.

Wire up the switches as shown in Fig. 5, wiring the terminals directly to the "0" line and the spare pads. Since these are press-to-make switches, their effect will be to give a logic 0 when pressed, the input to which they are connected will then float to logic 1 when the switch is released.

Miniature slide switches were tried, but found to short 1 to 0. With the switches in place, check the truth table for a NAND gate, using the LED to indicate the state of the output. The truth table should agree with that of Fig. 2a.

Now investigate the effect of adding an inverter, by joining a wire from pin 3 of the 7400 to pin 1 of the 7414, using the LED which is connected to pin 2 of the 7414 as the output indicator (Fig. 6). This connection,

NAND–GATE		
A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

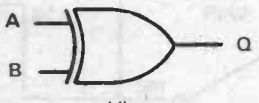
(a)

NOR–GATE		
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

(b)

X–OR GATE		
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

(c)



(d)

Fig. 3. Truth tables. (a) NAND-gate. (b) NOR-gate. (c) X-OR-gate. (d) Symbol for the X-OR-gate.

using the switches to provide inputs to the 7400, should give the truth table for an AND gate.

We find, however, that if we invert each input before applying to the 7400 inputs (Fig.7) that we do not obtain an AND gate this way. What truth table do we find?

To try it out, connect the switch outputs to the inverter inputs instead of to the 7400, one to pin 1 and the other to pin 3 of the 7414. Join pin 2 of the 7414 to pin 1 of the 7400 and pin 4 of the 7414 to pin 2 of the 7400, using single strand insulated wire. Use the LED which is connected to pin 3 of the 7400 as an indicator.

Having done this, could you design a NOR gate, and construct one? Try out your circuit and draw up a truth table.

The exclusive-OR circuit needs rather more thought. One possible circuit is shown in Fig.8. Construct this, using the 7400 and 7414 units, and check that the truth table agrees with that of Fig.3c.

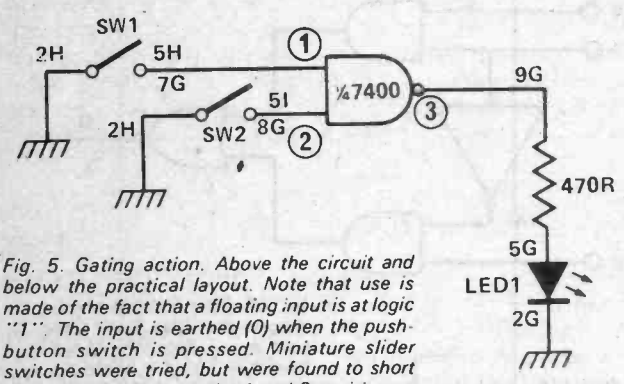


Fig. 5. Gating action. Above the circuit and below the practical layout. Note that use is made of the fact that a floating input is at logic "1". The input is earthed (0) when the push-button switch is pressed. Miniature slider switches were tried, but were found to short momentarily between the 1 and 0 positions.

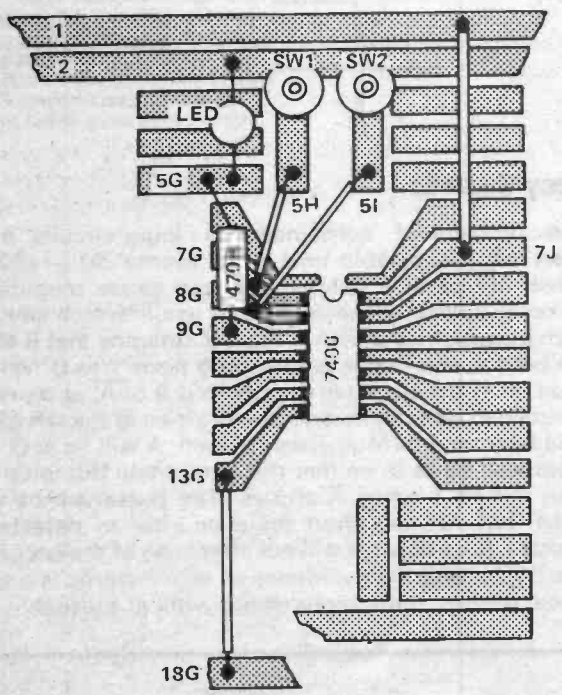
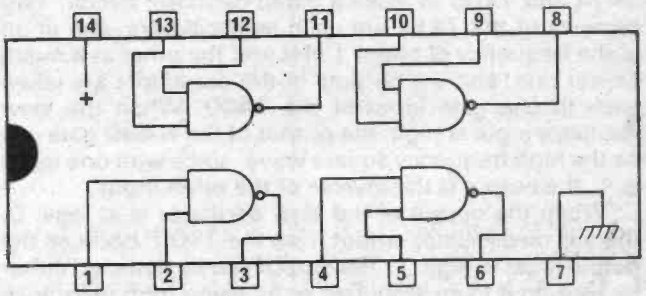


Fig. 4. Pin-out diagram for the 7400.



Combinational Logic

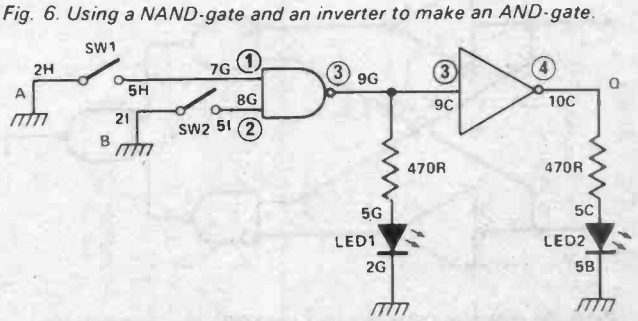
Circuits which contain only logic gates are called combinational logic circuits, because the output can always be predicted from the combination of inputs which is present. As we shall see later in this series, there are circuits in which the previous inputs matter as much as the present ones. Combinational logic circuits obey the rules of Boolean algebra, which will not be dealt with here, but have been discussed in ETI.

Because the output can always be predicted from the inputs which are present, logic gates can be used for control circuits. We can, to take a simple example, control the heating of a house by having logic gates control the circulating pump (or fan), by way of a thyristor or triac.

The inputs to the gates will be the signals from room thermostats, perhaps an outside thermostat, a boiler thermostat, a hot-water tank thermostat, and a timeswitch or two. There will be another output from the gates to control the operation of the boiler.

For such a system, logic gates easily carry out AND and OR actions which would need much more wiring

Fig. 6. Using a NAND-gate and an inverter to make an AND-gate.



and space to carry out with relays, but the full advantage of using logic gates is obtained when all the thermostats and other signal generating equipment and timing are also electronic.

Bawdy Work

An application of gating is shown in Fig.9, using the 7414 and 7400 to make a gated oscillator circuit. Two sections of the 7414 are used as oscillators, one at an audio frequency of about 1 kHz and the other at a much slower rate, and the outputs of the oscillators are taken each to one gate input of the 7400. When the slow oscillator input is high, the output of the NAND gate will be the high frequency square wave, since with one input at 1, the output is the inverse of the other input.

When the output of the slow oscillator is at logic 0, there is no oscillator output from the 7400, because the output is set to logic 1. The output can be detected either by feeding it to an amplifier, or by using high resistance headphones connected through a capacitor, or by using a capacitor and a 1k resistor in series with a small earpiece from a transistor radio.

Could you now design and construct a circuit whose output was a two-tone oscillation (HI-LO-HI-LO-). Remember that the output of the NAND gate in Fig.9 was a logic 1 when not oscillating. Do NOT be tempted to combine the outputs of two gates by joining output pins, this will BURN OUT YOUR IC, because very large currents will flow if one output is at 1 and the other at 0. One possible scheme uses three of the 7414 inverters as oscillators and one as an inverter, with three NAND gates also used.

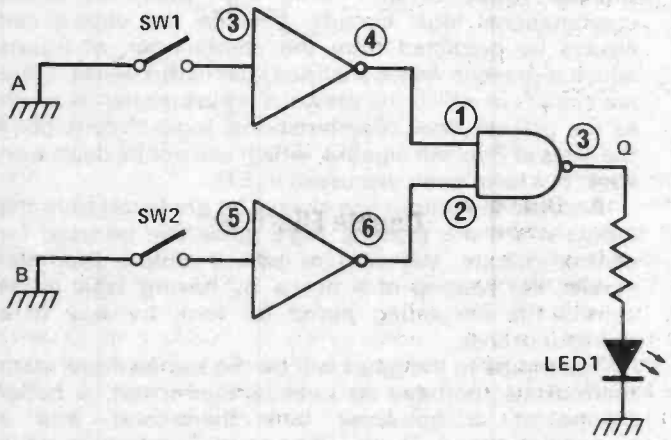


Fig. 7. What is the truth table for this circuit?

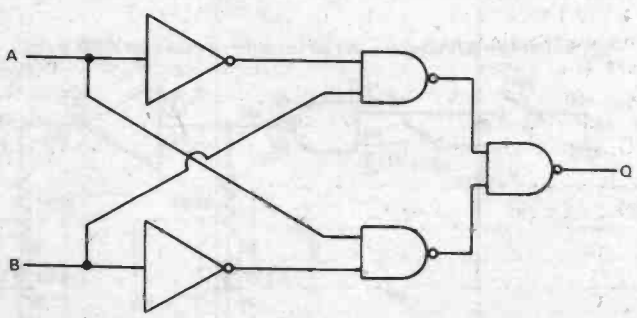
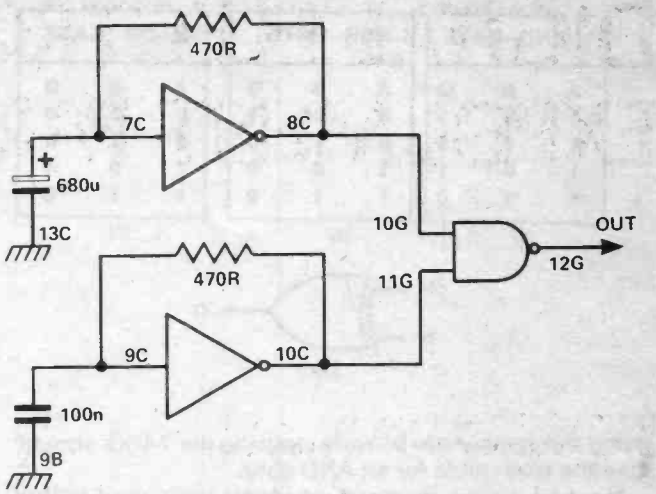


Fig 8. An exclusive-OR gate built from NOR-gates and inverters.



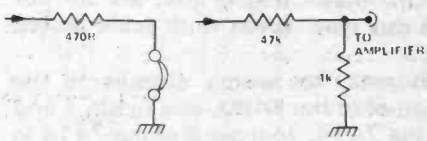
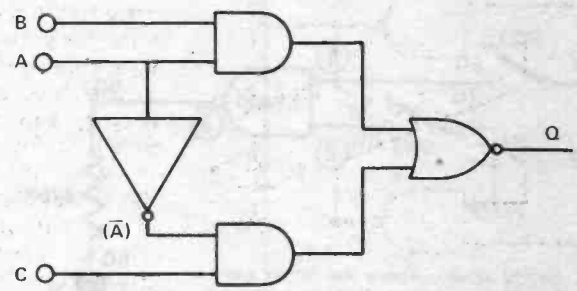


Fig. 9. A gated oscillator. (a) Circuit. (b) using an earphone to detect the note. (c) Connecting the output to an amplifier.



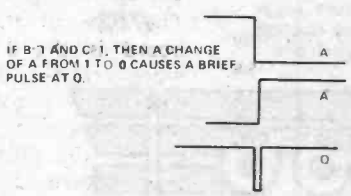


Fig. 10. Race hazards. If we imagine that lines B and C are both at one, then the change from A = 1 to A = 0 should cause no change in the output. Because of the delay in the inverter, however, A goes low just before Ā goes high so that there is a narrow negative pulse developed at the output. This could cause problems if a counter were being driven from the output.

Racy Hazards

One problem of combinational logic circuits is the short but measurable time delay (some 30 – 80 ns) which occurs in a gate, which can cause momentary spikes to appear in the outputs. A circuit which can give such a problem is shown in Fig.10. Imagine that B and C are both 1 and that A is changing from 1 to 0. With B and C at 1, the output of the circuit is A or $\overline{A}$, and since $\overline{A}$ is obtained from an inverter it will arrive at the OR gate a little later than A. Momentarily, then, A will be at 0, and $\overline{A}$ will still be at 0, so that the output will dip to 0, and then rise to 1 when $\overline{A}$ arrives. The pulse will be very short, but not too short for a counter to detect and register. Race hazards will not affect any of the circuits in this series, and the avoidance of race hazards is a topic which is beyond the scope of our work at present.

DIGITAL ELECTRONICS BY EXPERIMENT PART 4

In this part of our series we shall look into sequential logic by using the 7400 IC.

Set the IC up on the board to make a circuit using two of the logic gates as shown in Fig. 1. The gate with its output taken to the LED should have its spare input marked R, while the spare input to the other gate should be marked S.

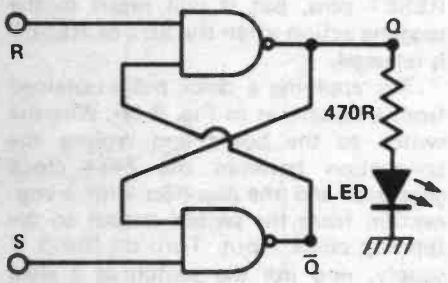


Fig. 1. Cross-coupled NAND gates forming an R-S flip-flop.

This circuit is a flip-flop, as you may have guessed from the cross-connection of inputs and outputs. Complete the table shown in Fig. 2, and note that the output for R = 1, S = 1 is *not* the same in each case.

Sequential Logic

The R-S flip-flop, as this is called, is an example of a sequential logic circuit, in which the output depends on the *sequence* of signals at the input – in other words, the state of the output depends on the previous signals as well as the present ones. Strictly speaking this circuit is more of a *latch,* a circuit which temporarily stores an output while both inputs are high. Note that in normal use, we want two outputs Q and $\bar{Q}$ to be complementary ($\bar{Q}$ is always the inverse of Q) so that the input R = 0, S = 0 must not be used, since this gives Q = $\bar{Q}$ = 1.

In logic circuits, clocked flip-flops are much more common. A clocked flip-flop changes state only when a timing, or clock pulse is received. This is done by combining the flip-flop action with gating so that the signal inputs have no effect until the gating (clock) pulse arrives.

R	S	Q
0	1	
1	1	
1	0	
1	1	

Fig. 2. Part truth table for R-S flip-flop. When you complete the table, taking readings from your blob-board circuit, be sure to work through each state in sequence.

One type of clocked flip-flop is the D-type, and a typical truth table is shown in Fig. 3. In this type of circuit the signal (0 or 1) which is present at the D (for Data) terminal is transferred to the output at the clock pulse, and remains unchanged until the data changes *and* the clock pulse arrives.

Clocked Flip-Flop

The type of flip-flop chosen for this board is the J-K flip-flop. This is a more versatile device which combines clocking with gating to achieve a wide range of actions. On the type we have chosen, the SN7476, the action is the type known as "Master-Slave", which means that the input signals are accepted on the leading edge of the clock pulse, but the outputs do not change until the trailing edge comes along. This avoids problems which would occur if outputs were connected back to the inputs, as we shall see later.

The J-K flip-flop has five inputs and two outputs. The inputs are labelled J, K, Clock, Set and Reset (the Reset is sometimes called clear, and the Set terminal is sometimes called preset). The outputs are Q and $\bar{Q}$, with $\bar{Q}$ always the inverse of Q. We shall check the action of the J-K flip-flop using signals generated on the board.

From previous work you should have available one section of the 7414 connected as a low speed oscillator. This provides an ideal slow clock pulse, and you should already have an LED connected to the output of the 7414 to monitor this pulse.

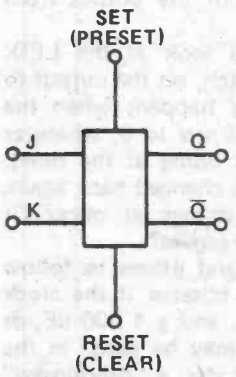


Fig. 4. J-K flip-flop symbol.

Double Flip-Flops

The connection diagram of the 7476 is shown in Fig. 5. From this you will see that the 7476 contains two J-K flip-flops which are completely independent. For the first series of practical exercises we shall use only one half.

Solder connections from pin 13 of the 7476 to earth, and from pin 5 to the +5 V line. Now solder an insulated wire connection from the clock oscillator output to pin 1 of the 7476, so that flip-flop number 1 is activated.

Connect pins 4 and 16 to earth so that J = 0 and K = 0, and connect switches so that the reset pin (pin 3) and the set pin (pin 2) can be connected momentarily to earth as needed. The

D SIGNAL	Q BEFORE CLOCK	Q AFTER CLOCK
0	0	0
0	1	0
1	0	1
1	1	1

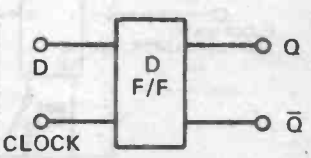


Fig. 3. D-type flip-flop and truth table. Note that, unlike the R-S flip-flop, changes take place only when the clock pulse arrives.

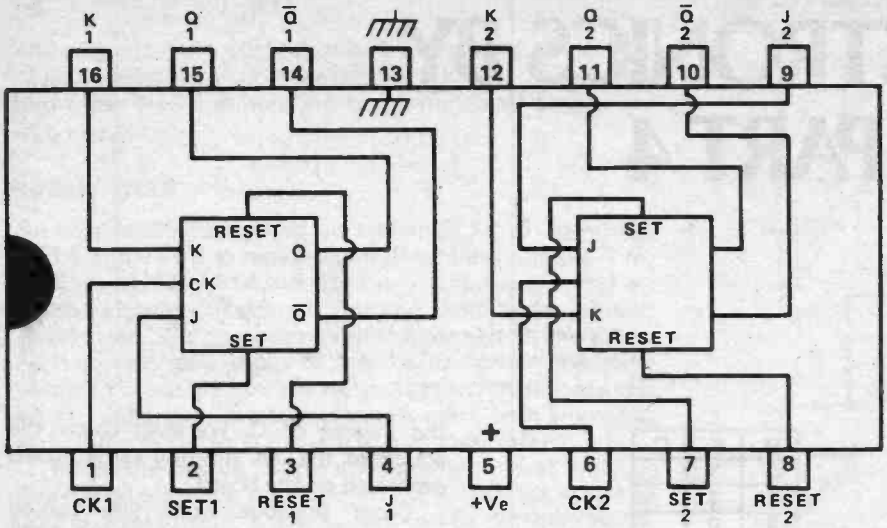


Fig. 5. Pinout of the SN7476 dual master-slave J-K flip-flop.

circuit is now as Fig. 6 , and the appearance of the board is shown in Fig. 7.

Now connect a resistor from pin 15 (Q) to a spare pad, and an LED from the spare pad to earth. This LED will indicate the state of the output from the flip-flop at Q.

Switch on, and look at the LED. Using the SET switch, set the output to give logic 1 (This happens when the SET switch is returned to 0, whatever the clock pulse is doing at the time). When the switch is changed back again, does the output change at once? Or when a clock pulse arrives?

These changes and others to follow may be easier to observe if the clock pulse is very slow, and a 1 000 uF, or greater, capacitor may be used in the oscillator circuit. Later, a "debounced" switch will be used.

Complete the sequential truth table, in which Q_{n-1} is the value of Q just before the clock pulse arrives, and Q_n is the value of Q just after the end of the clock pulse (the 1 to 0 change). Can you decide when the change, if any, occurs? Is it on the leading or the trailing edge of the clock pulse?

Now switch off, and disconnect one end of the link between K pin (pin 16) and earth, so allowing K to float to 1. Now we have J = 0 and K = 1. Switch on and observe the output. Change the output by using a switch (which one will you use SET or RESET?). Does the clock pulse affect the output after the switch has been returned to normal?

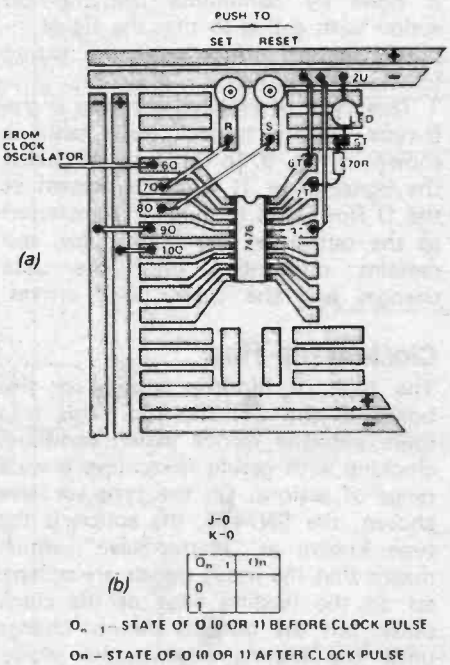


Fig. 7. (a) The layout on the board, with the LED in position.
(b) Form of part truth table.

Switch off again and reverse the connections so that J = 1 and K = 0, and repeat your readings. Enter all the readings on the sequential truth table of Fig. 8.

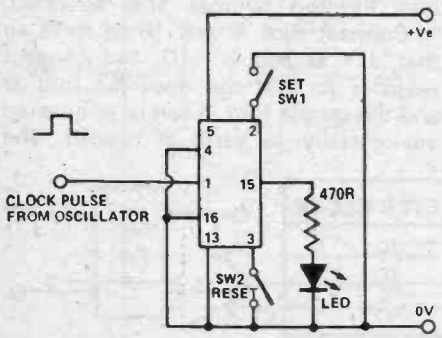


Fig. 6. Circuit for checking J-K action, see text for details.

From these exercises you wi found that the action of the J-K flip-flop can be controlled by the J and K inputs, which act to force the output to either 1 or 0 when the clock pulse arrives. The SET and RESET pins act independently of the clock, making the output go to 0 or 1, and holding it there until the reset or set voltage rises to 1 again, when the next clock pulse will cause whatever output is forced by the J and K voltages.

Toggling

With the power off, disconnect the wires from both J (pin 4) and K (pin 16). Switch on again, and observe both the output and the clock LEDs. Now complete the truth table of Fig. 8 (c). In this arrangement the J-K flip-flop is acting as a divide-by-two stage, for there is one complete output pulse for each two complete input pulses – we say that the flip-flop is *toggling*. At any time during this action, the output may be forced to 1 or 0 by the action of the SET or RESET pins, but it will revert to the toggling action when the SET or RESET is released.

Try applying a clock pulse obtained from a switch, as in Fig. 9 (a). Wire the switch to the board and replace the connection between the 7414 clock generator and the flip-flop with a connection from the switch output to the flip-flop clock input. Turn on the 5 V supply, and use the switch as a slow clock generator. You will probably find that the output is erratic, sometimes seeming not to change the output when the switch is operated.

This is caused by switch contact bounce.

De-Bounce De Switch

With power off, rewire the switch with a resistor and a capacitor to one of the spare sections of the 7414, as shown in Fig. 9 (b). This is a simple de-bouncing circuit.

Solder a resistor and an LED to the output of the 7414 in the usual way to show the state of the clock pulse, and connect the output also to the clock input of the 7476. You should find that the action is perfect, and the very slow clocking which is now possible will show that the changes which take place at the output do so when the clock pulse goes low, that is, from 1 to 0.

J=0 K=1

Q_{n-1}	Qn
0	
1	

J=1 K=0

Q_{n-1}	Qn
0	
1	

J=1 K=1

Q_{n-1}	Qn
0	
1	

Fig. 8. Remaining truth tables for J-K action.

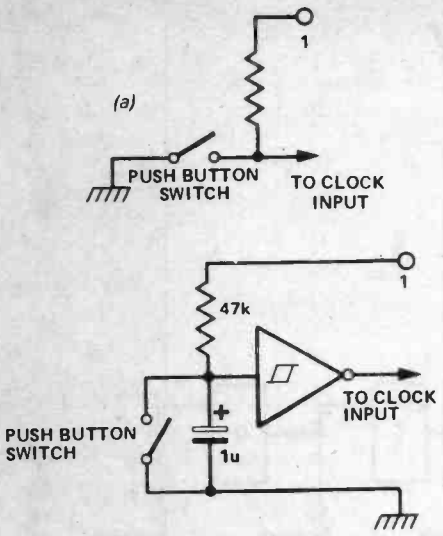


Fig. 9. (a) Using a push-button switch as a clock pulse supply.
(b) A debounced switch circuit.

Note that other flip-flop types may not have the same sequence of actions. Some, for example, are edge triggered, meaning that all the flip-flop action takes place on the leading edge of the clock.

When you are using flip-flop circuits, you must be careful to use the same type of flip-flop as that specified, since circuits which suit one type may not suit another. In particular, the 7476 "Master-Slave" type of flip-flop has a particularly complex action.

In essence, the action is that on the leading edge of the clock, the information which is present (1 or 0) at the J and K inputs is stored and once the clock pulse has reached its 1 value, these inputs are locked out, meaning that changes in J and K will now have no effect. At the trailing edge of the clock pulse, the flip-flop action takes place to change the output. The reason for this construction is that several types of circuits, some of which we shall build in this series, use feedback connections between the output of the flip-flop and its J or K inputs.

If all the action of the flip-flop happened at the leading edge of the clock, such feedback would cause indeterminate action — any change in Q would cause a change in J or K, which might cancel the effect on Q, and the flip-flop would probably oscillate at the high frequency. Because of the Master-Slave action, this does not happen — the changes in Q happen at the trailing edge of the clock pulse, by which time the J and K inputs are locked out and their voltages cannot affect the action until the leading edge of the next clock pulse.

Investigation

You should already have one section of the 7414 set up as a high frequency oscillator with earphones, or similar, to detect the output note. What is the effect of leading the output of the 7414 oscillator to the clock terminal of the 7476 with J = 1 and K = 1? Listen to the output wave from Q and compare it with the signal from the oscillator.

Can you now design an "octave" oscillator? This circuit will use a single oscillator, but its output will be alternately at oscillator frequency, then at half oscillator frequency (one musical octave below) according to the input to the gate. The gate input could then be obtained from another slow oscillator.

Finally, Fig. 10 (a) shows the complete truth table for the 7476. Fig. 10 (b) shows a changes truth table, in which the settings of J and K to produce certain changes (or non-changes) are listed. In the last table, X means "don't care", signifying that the value may be 1 or 0, and the action will be the same. Check that this last table agrees with the full table of Fig. 10 (a).

You may want to copy these tables, since we shall refer to them several times in Part 5 of this series.

Fig. 10. Truth table for J-K flip-flop

(a Complete truth table

J–K FLIP–FLOP

INPUTS		OUTPUT	OUTPUT
J	K	Q BEFORE CLOCK	Q AFTER CLOCK
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(b) Shortened truth table for changes only

J	K	Q_{n-1}	Qn
0	X	0	0
1	X	0	1
X	1	1	0
X	0	1	1

DIGITAL ELECTRONICS BY EXPERIMENT PART 5

We have seen in this series how the toggling action of a 7476 J-K flip-flop, which occurs when J = 1 and K = 1, gives an output pulse train at half the frequency of the input clock pulses. We can use this output as the clock pulse for a second flip-flop, and we will make up a circuit to find the practical outcome of this.

Frequency Divider

With power to the board switched off, set up the first flip-flop as before with J=1, K=1. Connect a wire link from pin 15 (Q1) to pin 6 (CK 2), and attach a resistor and LED in the usual way to pin 11 (Q2) and a spare pad. This LED will indicate the state of the output of the second flip-flop whose J and K pins can be left floating.

With power applied, the output pulses from Q2 should now be at one quarter of the frequency of the oscillator so that this complete circuit is a divide-by-four, producing one complete pulse at the output for each group of four complete clock pulses into pin 1. This is shown in the clock pulse diagram of Fig. 1(b).

With the supply disconnected again, connect up both halves of the second 7476 as shown in Fig. 2, so that we now have four toggling flip-flops in sequence.

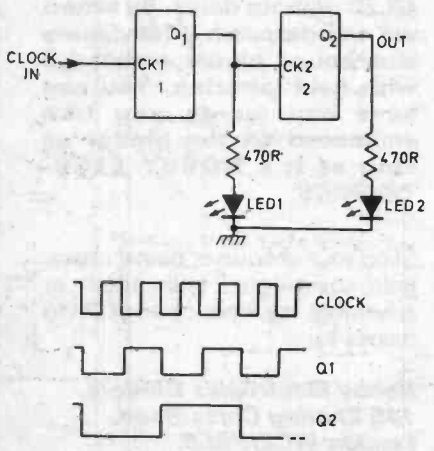
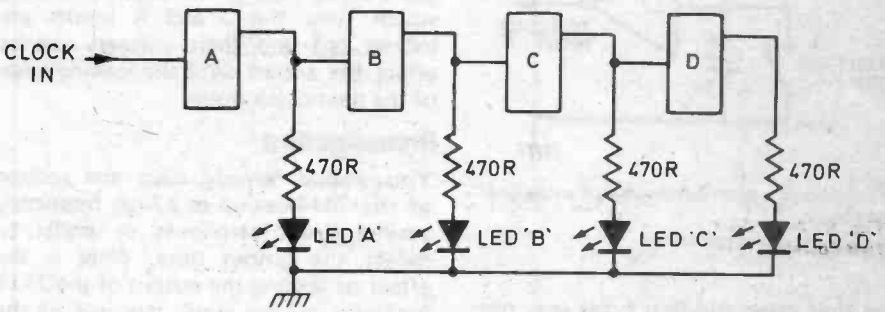


Fig. 1. Cascading 7476 J-K flip-flops.
(a) Circuit.
(b) Pulse diagram.



Connect a resistor and LED in the usual way onto the final Q output.

Can you predict what the count number of this circuit will be? (The count of a circuit is the number of complete pulses in to give one complete pulse out.) Using the slow clock pulse from the 7414 oscillator, count input pulses for one complete output pulse (0 to 1 to 0), and draw a clock pulse diagram.

Asynchronous Counters

The type of circuit described above is a frequency divider, with each stage dividing the clock frequency by two. It can also be thought of as a scale-of-two counter, with a serial input and a parallel binary output.

Let us explain this.

The pulses into the first clock input need not be at a steady rate, so long as each is separated from the next. This is a serial input – meaning one after the other. The output of each flip-flop can be read, by means of an LED attached to each Q output, for example, and since all can be read together, this is a parallel set of outputs. Our counter, therefore, has serial input and parallel output.

More important, if we started putting the pulses into the input when the output of each flip-flop was zero (the counter cleared, or reset), we could tell how many pulses had appeared at the input if we stopped counting at some stage.

If we label our flip-flops A, B, C, and D (Fig. 2), with A the flip-flop at the

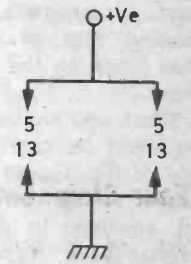


Fig. 2. Four cascaded flip-flops formed from the two 7476s.

input and D at the other end of the line, then we could also label B as 2, C as 4, and D as 8. We are able to do this because, starting at zero, QB will go to 1 after two input pulses (and back to zero on pulse number four), QC will go to 1 after four input pulses (and back to zero at eight), and QD will go to 1 after eight pulses, returning to zero at the sixteenth pulse. We would expect, for example, that after seven pulses QD=0, QC=1, QB=1, and QA=1 because 4+2+1=7.

PULSES	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1
16	0	0	0	0

Fig. 3. Truth table for four cascaded flip-flops.

This circuit is a binary asynchronous counter — binary because the counting is carried out in the scale of two instead of the more familiar ten, and asynchronous because the flip-flops are being clocked at different rates. The truth table of Fig. 3 shows the relation between the binary figures (the outputs from the Q terminals) and the number of pulses in (using decimal figures). Note that this arrangement counts to 15, and that all the flip-flops reset to zero on the sixteenth pulse.

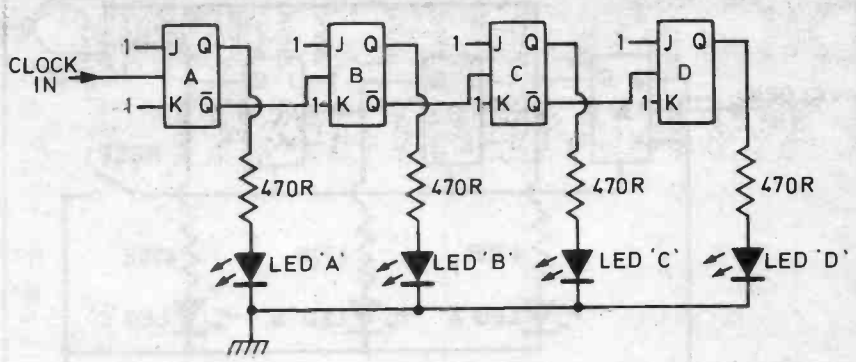


Fig. 4. Cascading from the $\overline{Q}$ terminals — what does this counter do?

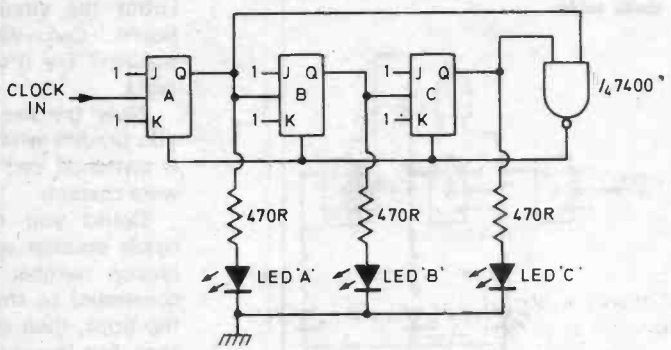


Fig. 5. A scale-of-five counter.

Four-Stage Counter

Set up a four stage asynchronous counter on your board with a resistor and LED to indicate the state of each Q output. Label the LEDs to avoid confusion — QD furthest from the pulse input should be labelled 8, QC labelled 4, QB labelled 2, and QA labelled 1. Take the oscillator output through a gate which can be controlled by a switch, and connect the reset terminals (pins 3 and 8 of each 7476) to another switch so that all the outputs can be reset to zero by pressing the switch to connect the reset pins to the 0 V line. Now apply power and check that the count sequence is as shown in the truth table of Fig. 3 when the gating switch is ON. Try switching the gate off and resetting.

Switch off the power and alter the connections between flip-flops A, B, C and D so that $\overline{Q}$A is connected to clock B, $\overline{Q}$B to clock C, and $\overline{Q}$C to clock D. Leave the LED indicators connected to the Q outputs as before (Fig. 4). Now switch on, and start the count. What is happening now?

Could you, not necessarily using only the ICs on the board, design a counter using two 7476s which would count either up to 15 and reset, or down to zero (resetting) according to the position of a single switch, or the voltage on a gate? The number of gates needed makes this impossible on our board.

Interrupted Counts

We seldom want a counter which counts up to 15 and then resets to zero. We may want a decimal counter (0 to 9 and then reset to zero), or a counter which stops at some definite count, or which counts to some number, resets to zero and then stops. These operations can be achieved by using the J and K terminals of the flip-flops together with gates.

Suppose, for example, that we want to count up to four, reset to zero at the fifth pulse, and then start again. What we need is some way of detecting the output at a count of five and using this to operate a reset. Detecting a count of five is easy enough since it is when QD=0, QC=1, QB=0, and QA=1. We can detect this by taking the Q outputs from C and A and connecting them to the inputs of a NAND gate, as shown in Fig. 5. When QC=1 and QA=1, the output of the NAND gate will be zero. The simplest and most obvious way to use this is to connect the output of the NAND gate directly to the reset line of the flip-flops, replacing the reset switch we used previously.

Set up this circuit on your board. Use wire connections from QC and QA to the inputs of one of the 7400 NAND gates, and disconnect the switch from the reset line. Now switch on, with the slow oscillator input to the flip-flop first clock, and observe the count.

Can you now design a counter using four flip-flops which would reset at the tenth inward pulse? This will be a scale-of-ten (decimal) counter. Remember that ten in the binary scale is when QD=1, QC=0, QB=1, and QA=0. If, for any reason we want to use a separate switch-operated reset with this counter, we shall have to arrange an input through either an OR gate or a NOR gate as shown in Fig. 6.

Fig. 6. Using a push-button reset with the circuit of Fig. 5. This could be implemented in several other ways.

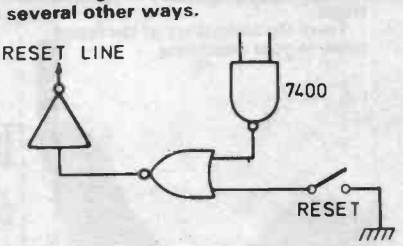
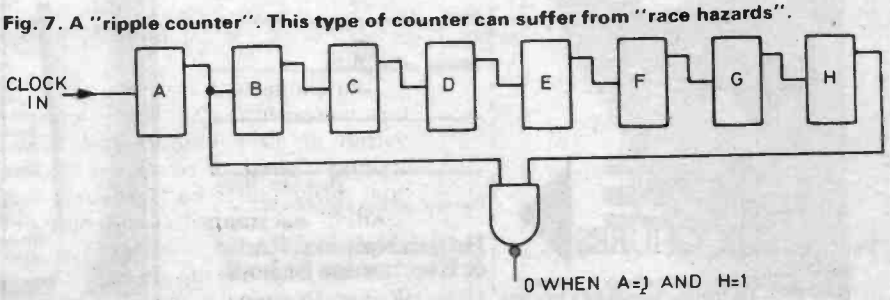


Fig. 7. A "ripple counter". This type of counter can suffer from "race hazards".



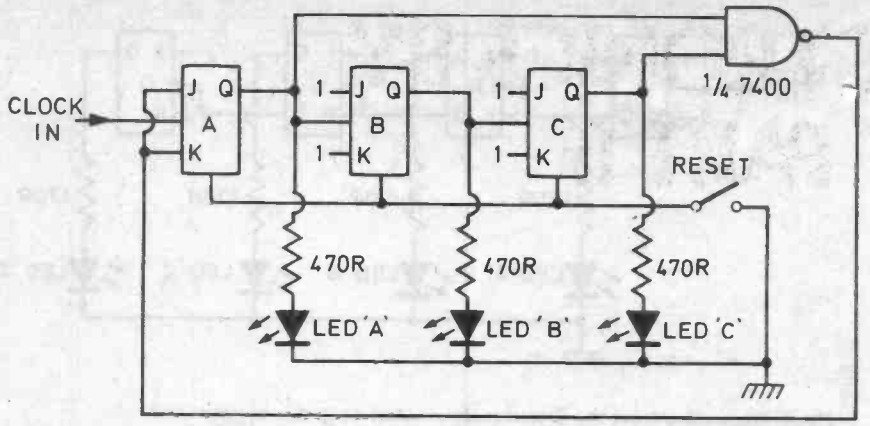


Fig. 8. What does this counter do? Build the circuit on your blob-board and draw up a truth table.

Ruined By Ripple

We can use this gating system to construct asynchronous counters which reset at the highest designed count number, but the system runs into problems with large count numbers and with high speed operation. For example, the first stage counter runs at the speed of the input pulses, and if these pulses are fast, then we may find "Race Hazards" — problems caused by the time delay in each flip-flop.

To take an example, we may be detecting the state 10000001. Now the 1 on the flip-flop H (Fig. 7), called "The Most Significant Figure", appeared just after the count had been 01111111, and if there is a time delay in the system flip-flop A may have gone to zero, to 1 and back to zero again before the clock pulse to flip-flop H has had time to work its way through all the stages in the counter. This time delay, caused by the need for a change to *ripple* through all the flip-flops, gives us the name "Ripple Counter", and can cause miscounting at high speeds.

Leaving this problem aside for the moment, our simple asynchronous counter has used the reset line for its reset action. For other types of count interruption we can make use of the J and K terminals of the J-K flip-flop, which is why they are provided. Construct the circuit of Fig. 8 on your board. Can you predict what will happen? Try it out and draw up a count table.

Now try the circuit of Fig. 9. Can you predict what will happen when this is switched on? Try it and see if you were correct.

Could you now design and try a ripple counter which could start at any binary number selected by switches connected to the SET terminals of the flip-flops, then count down, stopping at zero, but leaving the reset terminals free to be used with a switch?

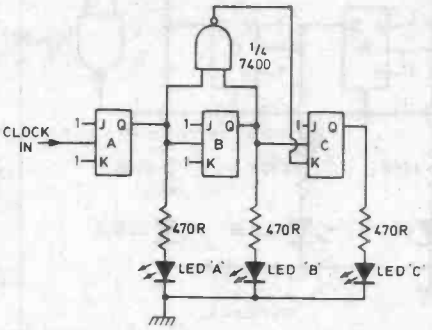


Fig. 9. What does this circuit do? Try to find out in theory, and then build the circuit on the blob-board.

DIGITAL ELECTRONICS BY EXPERIMENT PART 6

Ripple counters are useful and simple, but they are not ideal for high counting speeds, nor for large counter chains. The problem arises from the use of the output of each flip-flop as the clock for the next fli-flop, so that changes must "ripple through" all the stages of the counter. This, as indicated in the previous section, causes difficulties with time delays.

Although these delays are not large, perhaps 60 nS or less per flip-flop, they accumulate to a significant amount over a large number of counter stages and can cause the race hazards mentioned earlier.

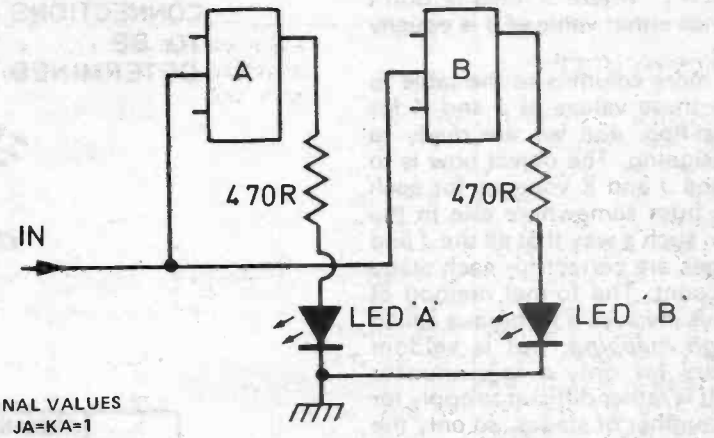
Synchronous Counters

A different principle is used for synchronous counters. The input pulses are used to clock *each* flip-flop of a chain, hence the name synchronous. The count sequence is then determined by voltages applied to the J and K terminals, and these voltages must be obtained in such a way that any given count on the flip-flop will cause the J and K voltages to be set to the voltages needed to change to the next digit up or down.

This is much more easily illustrated by an example which we can test on our board. In this example we shall follow the pattern of design steps (with some modifications) which is usually used for synchronous counters.

Basic Two-Step

Let us imagine a very basic counter using two flip-flops and resetting at the count of four. We must start by making a table showing the count, the present state, and the next state for each flip-flop. This means that for each number of the count we list the value of Q (1 or 0) and also the value to which Q will change at the next count. For example, when the count is 1 (01), the next count is 2 (10) and both outputs will change — A from 1 to 0, and B from 0 to 1. On the next count (3), A changes from 0 to 1, and B does not change. The complete table for two flip-flops is shown in Fig 1(b).



FINAL VALUES
JA=KA=1
JB=KB=QA

	A		B		J K VALUES			
COUNT	Q PRESENT	Q NEXT	Q PRESENT	Q NEXT	JA	KA	JB	KB
0	0	1	0	0	1	X	0	X
1	1	0	0	1	X	1	1	X
2	0	1	1	1	1	X	X	0
3	1	0	1	0	X	1	X	1

Fig. 1 (Above) A simple synchronous counter, no J-K connections shown.
(a) Circuit. Note that the input clock is taken to each stage.
(b) Table of changes, with J and K values for the changes.

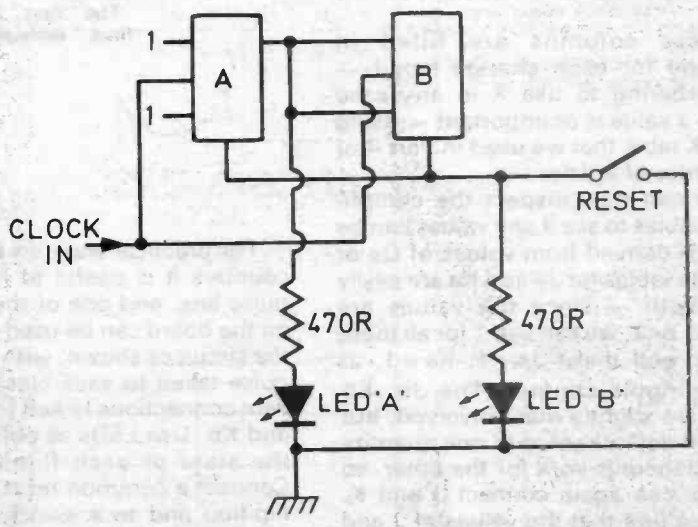


Fig. 2 (Above). Complete two-stage synchronous counter circuit, with J-K connections shown. Try this out on your blob-board.

Now we have to decide what voltages are needed at J and K of each flip-flop to carry out the changes from present state to next state. Here we have some options — for example, if we want to change from 1 to 0, we may have J = K = 1, or J = 0 and K = 1; either state will carry out the change. When this is possible, we can write J = X, K = 1, where X means don't care, since either value of J is equally suitable.

Add more columns to the table to indicate these values of J and K for each flip-flop, and we are ready to start designing. The object now is to obtain the J and K voltages for each flip-flop from somewhere else in the circuit in such a way that all the J and K voltages are correct for each stage of the count. The formal method of doing this involves a technique called *Karnaugh mapping*, but is seldom necessary for only a few counter stages. It is rather difficult to apply for a large number of stages, so only the 'intuitive' look-and-see method will be discussed here.

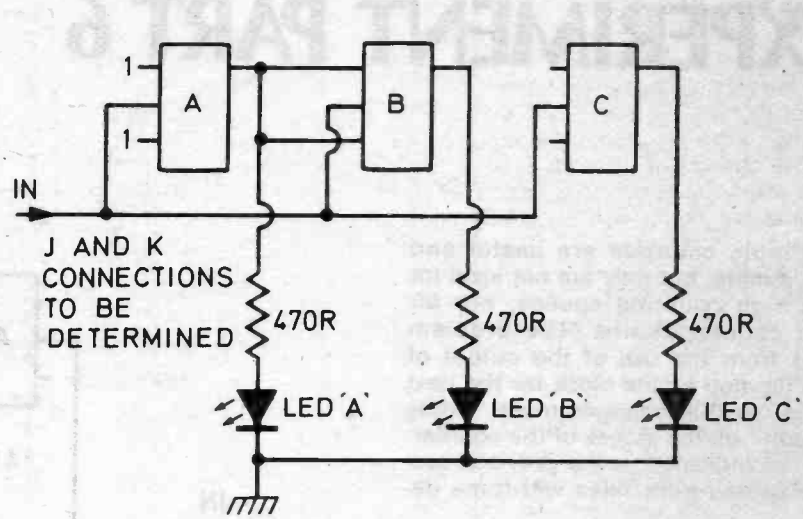
Table Talk

At the zero count, Qa = 0, Qb = 0 and the change at the end of the clock pulse will be from Qa = 0 to Qa = 1. This will happen if Ja = 1 and for Ka = 0, or Ka = 1. We therefore fill in a 1 in the Ja column, and an X (either value) in the K column.

Still at the zero count, Qb = 0 and does not change at the end of the clock pulse. This can be done if Jb = 0, Kb = X, so that these values 0 and X appear in the Jb and Kb columns.

These columns are filled in similarly for each change listed — remembering to use X in any case where a value is unimportant — using the J-K table that we used in Part 4 of this series of articles.

We can now inspect the complicated tables to see if any values can be fixed or derived from values of Qa or Qb. The tables for Ja and Ka are easily dealt with — since the values are either 1 or X, we can use 1 for all these values, and make Ja = 1, Ka = 1, as for the ripple counter. The Jb, Kb tables are slightly more involved, but for each definite value of one quantity (J or K) there is an X for the other, so that we can again connect J and K. We then find that the values of J and K are identical to the values of Qa, so that Jb and Kb can be connected to Qa.



COUNT	PRESENT QA	QB	QC	NEXT QA	QB	QC	JA	KA	JB	KB	FIRST JC	KC	FINAL JC	KC
0	0	0	0	1	0	0	1	1	QA	QA	0	X	0	0
1	1	0	0	0	1	0	1	1	QA	QA	0	X	0	0
2	0	1	0	1	1	0	1	1	QA	QA	0	X	0	0
3	1	1	0	0	0	1	1	1	QA	QA	1	X	1	1
4	0	0	1	1	0	1	1	1	QA	QA	X	0	0	0
5	1	0	1	0	1	1	1	1	QA	QA	X	0	0	0
6	0	1	1	1	1	1	1	1	QA	QA	X	0	0	0
7	1	1	1	0	0	0	1	1	QA	QA	X	1	1	1

JC=QA AND QB
KC=JC

Fig. 3 (Above). A three-stage synchronous counter.
Top: (a) Circuit, J and K connections still to be determined.
Bottom: (b) Table of changes, showing how J and K values are determined.
The "first" Jc-Kc table shows possible values of Jc and Kc, the "final" table shows the most convenient values to use.

For practical work on synchronous counters it is useful to have a clock pulse line, and one of the spare lines on the board can be used. Connect up the circuit as shown, with a slow clock pulse taken to each clock input, and wire connections linked from Qa to Jb and Kb. Use LEDs as before to check the state of each flip-flop output. Connect a common reset line to each flip-flop and to a switch so that the counter can be reset. Switch on and check that the count is correct and that resetting to zero is possible.

Third Stage Development

Let us now extend this to a third stage, building on what we have done before. Once again we can build up a table of values of Q, J and K for each stage, but we have made life easier for ourselves by having done the two stage counter, so we can ignore the Ja, Ka and Jb, Kb columns and concentrate on the Jc, Kc column.

Using the same principles as before, we fill in the values of J and K which will be needed at each clock pulse or flip-flop, concentrating on the necessary values, and putting an X

where the value is immaterial. When we do this (Fig. 3b) we find two important states. One is at the count of 3, where Jc must change from 0 to 1; the other is at the count of 7 when Kc similarly changes from 0 to 1.

The change of Jc from 0 to 1 occurs when the count changes to 110 so that we could use an AND gate connected to Qa and Qb. The output of this gate will be zero for any count up to 2 and then will be 1 at a count of 3. It will change to zero again to become 1 at the count of 7, but the value of Jc is unimportant beyond the count of 3 anyway.

Looking at Kc we find that the important value of 1 occurs at a count of seven when Jc may also be 1. We can therefore connect Jc and Kc together and feed from an AND gate supplied with Qa *and* Qb.

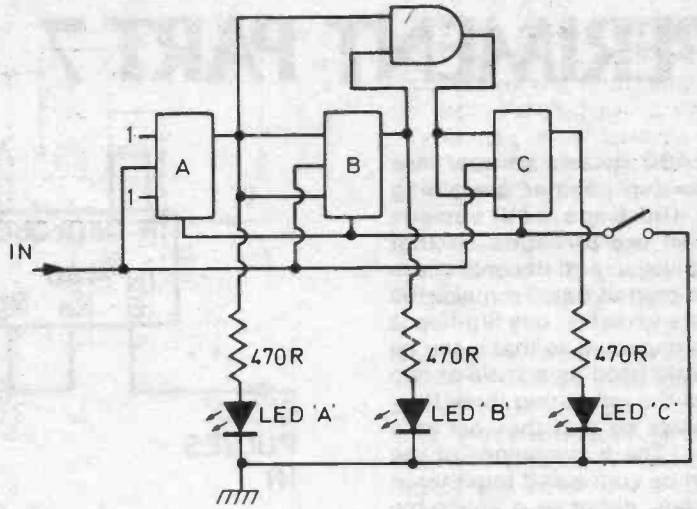
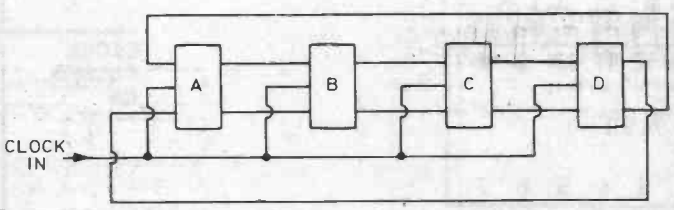


Fig. 4 (Above). The circuit of the three-stage synchronous counter. Try this out on your blob-board.

Third Stage On Board

Making up a three-stage synchronous counter on the circuit board needs some additional connections. Since we are not using AND gates, the gate used will have to be made up from a NAND gate and an inverter. As the 7400 contains four two-input NAND gates and the 7414 contains six inverters, one of which is used for the clock oscillations, there is no shortage of gates. We are working with a low frequency clock, so there should be no ill-effects caused by the number of wires soldered across the board, but a high speed counter would have to be built on a PCB designed for the purpose, using copper tracks on each side and with decoupling capacitors between +ve and —ve lines close to each flip-flop.

Can you now go one step further to design a four stage synchronous counter and try it out on the board?



NO RESET LINE SHOWN

CLOCK	JB QA	KB $\overline{Q}$A	JC QB	KC $\overline{Q}$B	JD QC	KC $\overline{Q}$C	KA QD	JA $\overline{Q}$D
0								
1								
2								
3								
4								
5								
6								
7								

Fig. 5. A Johnson counter of four stages.

Top: (a) The circuit, note the "twisted ring" connection.

Bottom: (b) Table to complete so that the counter action can be predicted.

Below: (c) Truth table. Build the circuit on your blob-board and complete this table.

COUNT	A	B	C	D
0				
1				
2				
3				
4				
5				
6				
7				

Twisted Logic

A different type of synchronous counter is shown in Fig. 5. This is a Johnson, or 'twisted-ring', counter and consists of four flip-flops connected so that the output of one drives the J and K inputs of the next. Three of the connections are made up with Q to J and $\overline{Q}$ to K, but the feedback connection is made with Q to K and $\overline{Q}$ to J — hence the alternative name of twisted-ring. Remembering that $\overline{Q}$ is always the inverse of Q, can you plan out the values of Q and $\overline{Q}$ for each counter? Use the table headings shown in Fig. 5(b) and remember that Qa = Jb, Qb = Jc, Qc = Jd, Qd = Ka and so on.

A Johnson counter uses a completely different count sequence from conventional binary counters, and the maximum count number is twice the number of flip-flops. The counters are synchronous, very easy to design and also very simple to decode for use with lamp indicators.

Build up the four stage (count of 8) Johnson counter of Fig. 5(c) on your circuit board and check that your calculations are correct.

DIGITAL ELECTRONICS BY EXPERIMENT PART 7

The 7490 decade counter is a single-chip counter containing four flip-flops and various gates, which are arranged so that frequency division and decimal counting can be carried out. To make the counter more versatile, one flip-flop is separately connected so that it can be independently used as a scale-of-two counter and the remaining three flop-flops are gates so that they act as a scale-of-five. The two sections of the counter can be connected together in different ways, either as a divide-by-ten circuit, or as a decimal counter with BCD outputs.

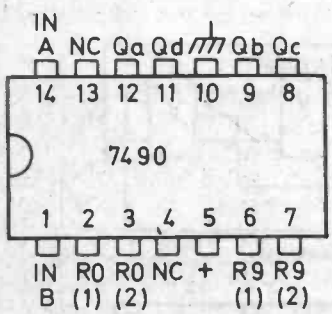


Figure 1. Pinout of 7490 Decade counter.

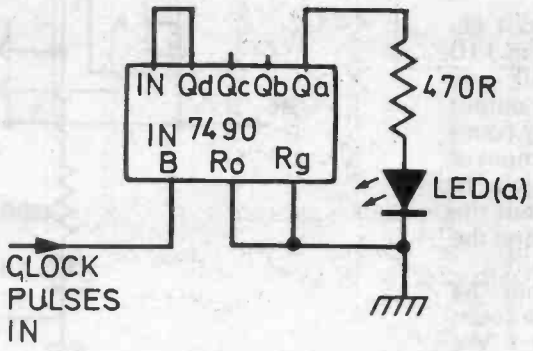


Figure 2. Connections for frequency division by ten — note that the symbol does not show the true pin positions.

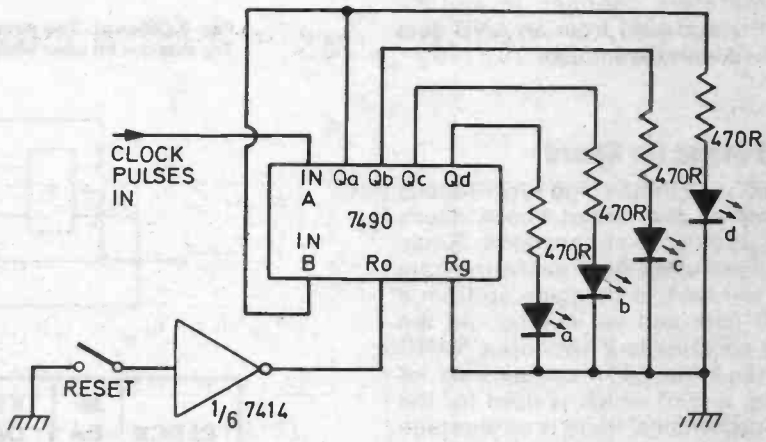
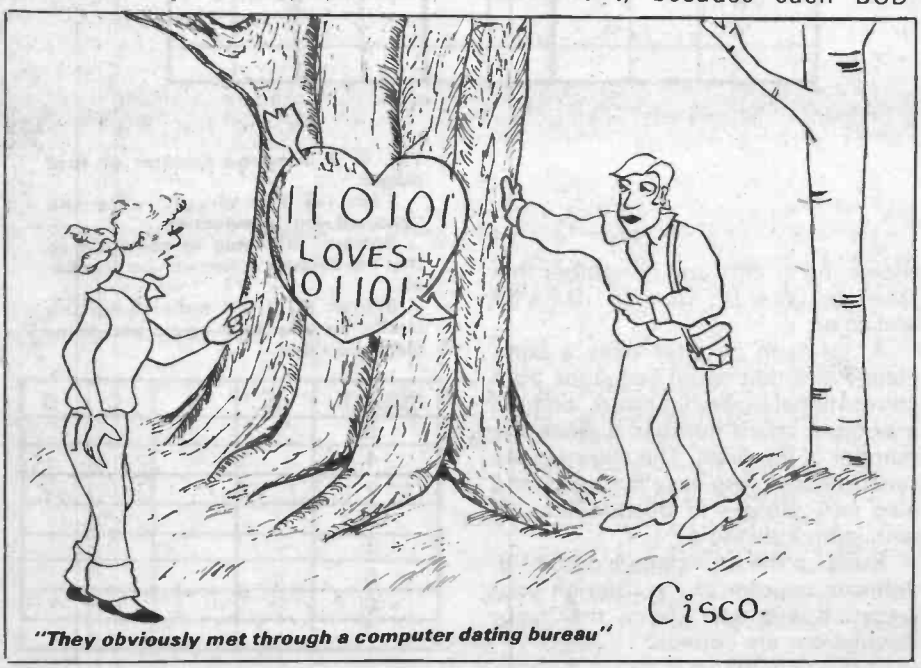


Figure 3. Connections for BCD counting, with reset switch. The reset pin must be kept at logic zero for counting, and taken to logic 1 for reset, so that an inverter must be used along with the push-button switch.

Twos Into Tens

BCD — meaning Binary-Coded-Decimal — is a form of binary code which is particularly useful if decimal numbers have to be displayed. In a BCD count, each figure of a decimal number is represented by its binary equivalent, so that the number 85 (decimal) becomes 1000 0101, binary 8 and binary 5. Although more convenient, because each BCD counter can then drive a display unit, this form is longer than a pure binary number (binary 85 = 1010101, only seven figures), and BCD numbers are not so simple to add and subtract as pure binary numbers.



"They obviously met through a computer dating bureau"

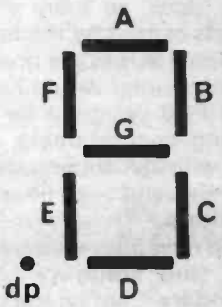


Figure 5. Arrangement of segments in a seven-segment display. The decimal point, which may be on the other side of the figure, is always energised separately, often from a range switch.

BCD in Practice

Connect the power supplies to the 7490 with pin 10 to earth and pin 5 to +5 V. Pins 2 and 7 should also be

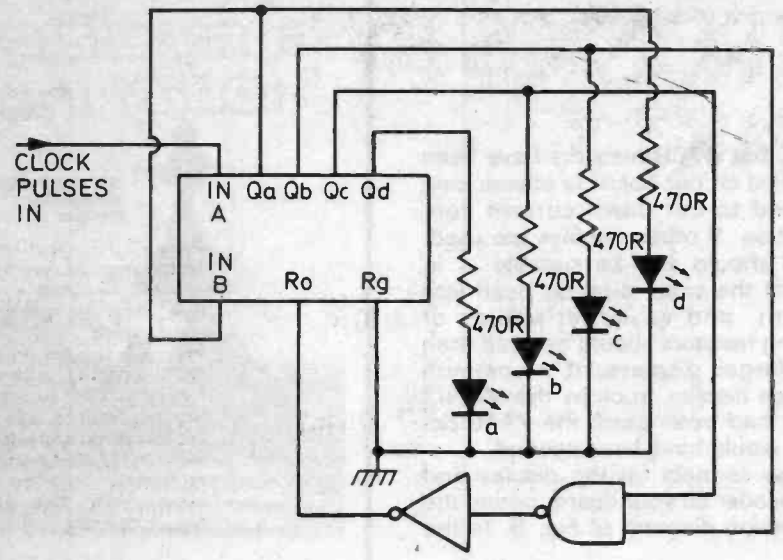


Figure 4. A terminated count. At some stage in the count, the gate will force the counter to reset. When does this happen?

Number/ Character	a	b	c	d	e	f	g
0	x	x	x	x	x	x	–
1	–	x	x	–	–	–	–
2	x	x	–	x	x	–	x
3	x	x	x	x	–	–	x
4	–	x	x	–	–	x	x
5	x	–	x	x	–	x	x
6	–	–	x	x	x	x	x
7	x	x	x	–	–	–	–
8	x	x	x	x	x	x	x
9	x	x	x	–	–	x	x
[(10)	x	–	–	x	x	x	–
ɔ(11)	x	x	x	x	–	–	–
⌊(12)	–	x	–	–	–	x	x
⊆(13)	x	x	–	x	–	x	x
⊧(14)	–	–	x	x	x	x	x
Blank (15)	–	–	–	–	–	–	–

x - lit
– - unlit

Figure 6 (left) Truth table for figure and character displays.
Figure 7 (above). Truth table for a common-anode display, figures only.

	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	1	0	0	1	1	1	1
2	0	1	0	0	0	0	1	0	0	1	0
3	1	1	0	0	0	0	0	0	1	1	0
4	0	0	1	0	1	0	0	1	1	0	0
5	1	0	1	0	0	1	0	0	1	0	0
6	0	1	1	0	1	1	0	0	0	0	0
7	1	1	1	0	0	0	0	1	1	1	1
8	0	0	0	1	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0

earthed for most of the experimental work in this section, although we may use pin 2 later for resetting to zero. Now connect LEDs and their limiting resistors, using the spare pads on the board, to Qa on pin 12 and Qd on pin 11. Connect the clock pulse from the slow oscillator to input A (pin 14) and by watching the clock LED and the LED connected to pin 12 (Qa), note the action of this section of the counter.

Switch off, transfer the clock pulse input to input B on pin 1, and switch on again, watching the clock LED and the Qd LED on pin 11. Note that the counter will operate only if the reset pins are earthed. There are two pairs of reset pins, each pair being inputs to an AND gate which operates the reset. Pins 2 and 3 are the reset to zero pins, and earthing either of them enables the counter. If both are allowed to float to logic 1, or are taken to logic 1, the counter resets to zero. Pins 6 and 7 also act through an AND gate, but with both high the reset is to BCD 9 (1001) rather than to zero.

To use the 7490 as a frequency divider (Fig. 2), we connect Qd (pin 11) to INa (pin 14) and take the clock pulse to INb (pin 1). The output will appear at Qa, on pin 12, and the state of this output is monitored by an LED already. Connect up the clock pulse from the slow oscillator on the board, and by counting pulses, confirm that the correct division ratio is being obtained.

For a BCD count, the connections must be changed around (Fig. 3). We now need LED indicators on the Qb (pin 9) and Qc (pin 8) outputs as well as on Qa (pin 12) and Qd (pin 11), and the cross-connections are different, with Qa connected to input B and the clock input taken to input A on pin 14. Label the LEDs as A, B, C, and D, and switch on, noting the values at each stage of the count. Use de-bounced switch as a clock supply if the oscillator is too fast to follow. Note that in the circuit of Fig. 3 a reset switch has been used; because we are using push-to-make switches, an inverter must be used as shown.

Because the 7490 is on a single chip it may be convenient to adapt it for counts of less than 10, rather than use separate flip-flops. This is made easier by the arrangement of the reset lines, connected through AND gates. Ignoring the reset-to-nine pins, we can arrange for pin 2 to be driven by a gate whose output must be zero during the count, rising to 1 at the end of the count. Pin 3 must be kept high, or the count will not be interrupted.

Try the circuit of Fig. 4 — can you work out what the count figure will be? Connect up and try the circuit out.

Displays

Though several other forms of display exist, the most convenient type for use with TTL circuits is the seven-segment LED display. The type used for this board, the BI-PAK DL747 (Jumbo) is one of the largest displays of this type available at the time of writing, and has been selected from the point of view of easy reading at a distance. If any other type is substituted, care will have to be taken with the pin connections, since there are several pinout standards for this type of display.

As the name suggests, the seven-segment display consists of seven LEDs made in one chip in the arrangement of a figure-of-eight, as shown in Fig. 5. The letters allocated to the strips are also shown (fortunately these are standardised).

Looking at the arrangement of the segments, we can draw up a table of the segments that will have to be activated (ON) for each number we want to display. Fig. 6 shows such a

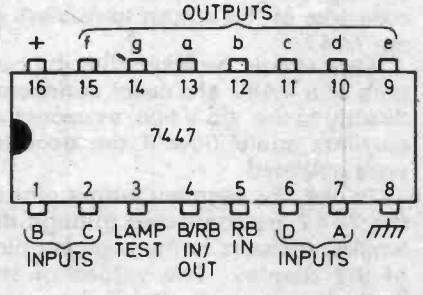


Figure 8. Pinout of 7447 BCD to 7-segment decoder-driver.

table for the numbers 0 to 9, and also some of the other characters which can be obtained. We now have to translate this ON/OFF table into terms of logic 1 and 0.

The next step depends on the type of display that is being used — common cathode or common anode. As the name suggests, the common cathode display has all of the LED cathodes connected together to logic 0, and each anode must be taken to logic 1 to be illuminated. To prevent excessive current flowing — because the normal forward voltage across the LED is less than the +5 V of the logic circuits — we must wire a limiting resistor in the connection to each anode. We cannot use one single resistor in the cathode lead, as this would cause the brightness of the display to alter according to the number of segments lit.

The other possibility is to connect the anodes of the LEDs together and take the cathodes out to separate pins. In this common-anode type of display, the segments will be lit when their respective cathodes are at logic zero, and once again limiting resistors must be used between each cathode and the TTL driving stage.

The type of display specified for this board is a common anode type, with several of the pins on the display connected to the common anode. Only one of these pins need be connected to the 5V line.

Decoders

To obtain a decimal readout from the BCD output of the 7490 counter, a decoder stage is needed with the truth table shown in Fig. 7.

The type used here is the 7447 BCD-to-seven segment decoder/-driver, which has output stages of transistor collectors with no loads. In this eay, the combination of LED and limiting resistor acts as load for the collectors of the output transistors in the 7447.

Care should be taken that the outputs of a 7447 are never connected directly to the +5 V line, as excessive currents could flow if the decoder were operated.

In use, the segment output pins of the 7447 are connected through the limiting resistors to the segment pins of the display. The values of the limiting resistors used will determine the brightness of the display. For the 7447 display we can use 150 R resistors, but 470R resistors have been specified on our board to ensure long life and to cut down current consumption. If other displays are used, 470R should also be suitable — in general the small displays need less current, and so larger values of limiting resistors should be used than with larger displays. If a common cathode display, such as the MAN-3 types, had been used, the 7448 decoder would have been needed.

Now connect up the display and the decoder on your board, noting the connection diagram of Fig. 9. In the

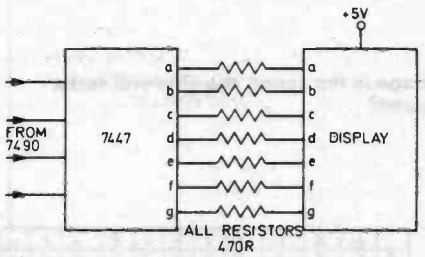


Figure 9. Connection of 7447 to display — not that the arrangement on the board is tidy as the diagram would suggest!

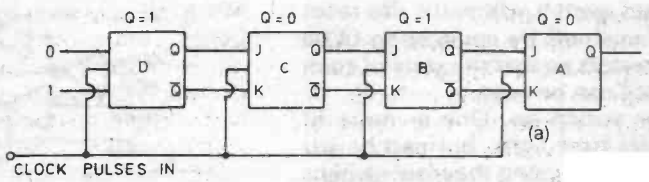
prototype boards, the very small resistors used for limiting could be passed under the body of the display, so avoiding long paths around it. The +5 V supply is taken to pin 16 of the 7447, and earth is taken pin 8. The outputs of the 7447, all on the side facing the display, and marked on the circuit diagram with small letters, are taken through the 470R limiters to the correspondingly lettered pins of the display. The inputs indicated by the capital letters A,B,C and D on pins 1,2,7 and 6 of the 7447 are for the BCD input from a 7490 and should be connected to the appropriate Q outputs from the 7490 counter.

Testing and Blanking

Note that pin 3 of the 7447 is labelled "lamp test." Taking this pin to logic 0 illuminates all segments of the display irrespective of what stage the count has reached, and is a useful check on the operation of the display. For example, an operator can check that a steady display of 3 is not just a display with two segments faulty.

Pins 4 and 5 on the 7447 are for blanking, used mainly when the display is one of a set, to suppress zeros occuring before the first significant figures and after the last one. When pin 4 is low, the display is blanked out, though counting is unaffected.

DIGITAL ELECTRONICS BY EXPERIMENT PART 8



CLOCK PULSE	QD	QC	QB	QA
0	1	0	1	0
1	0	1	0	1
2	0	0	1	0
3	0	0	0	1
4	0	0	0	0

(b)

Fig 1. A shift register made up from J-K flip-flops. (a) Arrangement of the flip-flops. (b) Truth table, showing the effect of clock pulses.

A shift register is a set of flip-flops, each of which can be set by its PRESET terminal to store a 1 or 0, so that the complete set stores a "word," (complete number). For example, four flip-flops could store numbers such as 0101, 1000, 1101, and so on. In addition, we can apply clock pulses to all of the flip-flops and so cause the stored numbers to shift from one flip-flop to the next in line on each clock pulse; several designs make this possible in either direction (right-left shift).

Fig. 2 shows an example of this in action. We start with the number 1010 stored, so that LEDs on the B and D outputs will be lit. The input of the first flip-flop is connected with J=0; K=1, so that at the clock pulse its Q output will change to zero. The two outputs of the first flip-flop, however, are connected to the J and K inputs of the next flip-flop in line (compare the Johnson counter, which is very simply obtained from a shift register). With J=1 and K=0 on the second flip-flop, from the outputs of the first, the clock pulse will cause the output of flip-flop C to change from 0 to 1. Similarly, with Jb=0, Kb=1, flip-flop B is forced to change from 1 to 0, and flip-flop A is forced to change from 0 to 1. The effect is as if a zero had been forced in at the left-hand side and has caused all of the stored numbers to shift one place along.

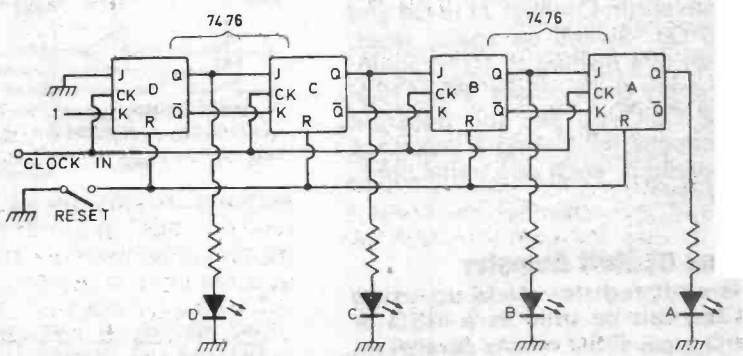
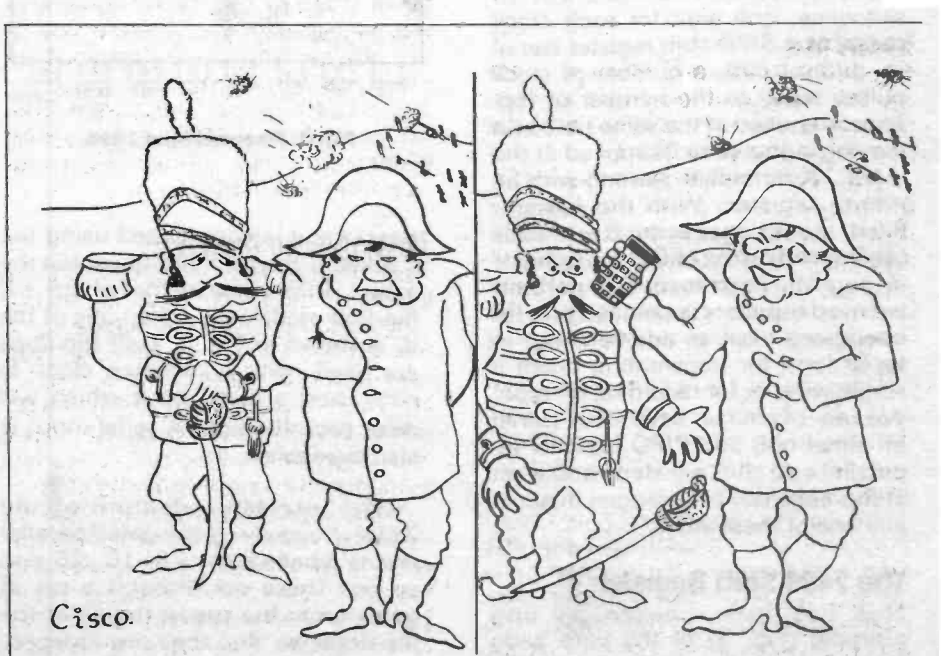


Fig 2. Connections of 7476 flip-flop to form a shift register on the 8-IC Blob-board.

A Simple Shift Register

Use the two 7476 J-K flip-flops (Fig. 2) on your blob-board to make up a four-stage shift register. Connect the clock inputs to one of the spare pads of the blob-board, and run a line from this pad to the output



"Now you try and work out a problem without looking at the keyboard."

of the slow oscillator or the debounced switch. Blob short connecting wires from each Q output to the next J input, and from each $\overline{Q}$ output to the next K input. Blob a wire from Ja to the earth line, leaving Ka floating. Connect the reset pins to a reset line (a spare blob-pad) and so to the reset switch so that pressing the reset switch will earth the reset pins. Finish off by connecting LEDs and resistors so that the state of each Q output can be read.

Now switch on. One or more of the LEDs may light, but can be extinguished by using the reset switch. Now set up a number by using the preset terminals. By temporarily bridging from each preset pin to earth, using a wire bridge, set two of the flip-flops to 1, preferably so that 1010 is stored. Now apply clock pulses and observe what happens; this is easier to follow if the debounced switch is used.

Now switch off, and disconnect Ja from earth. Connect Ja to Qd and Ka to Qd. Switch on again, reset, and set to a display of 1010 again. Now apply clock pulses. What happens? Can you see the possible applications for storing a sequence of operations, such as a traffic lights sequence?

Types of Shift Register

The shift register made up using 7476s can be used as a PISO or SIPO type. PISO means parallel in, serial out; the information is set up on each flip-flop, perhaps at the same time, and is read out in sequence, one digit for each clock pulse. In a SIPO shift register (serial in, parallel out), a number of clock pulses equal to the number of flip-flops is applied at the same time as a varying signal (0 or 1) applied at the input J-K terminals, starting with an empty register. With the register filled, the voltages at the Q terminals can be read (using LEDs for example) in parallel. Each type is important; we need numbers in parallel form for operations such as addition, but in serial form for transmitting down a single wire, or for recording on tape. We can, of course, have SISO (serial in- serial out) and PIPO (parallel in-parallel out) shift registers, and a set of flip-flops can be arranged to act in any one of these ways.

The 7494 Shift Register

This has been chosen as one example (Fig. 3) of the very wide variety of shift registers that are available. Like most integrated shift registers, it is constructed using the clocked S-R type of flip-flops, but the action is the same as that of our J-K flip-flop model; the schematic of the IC is shown in Fig. 4. Four flip-flops are used, with a common clock to each, and a clear input which will reset each flip-flop. A serial input is also available.

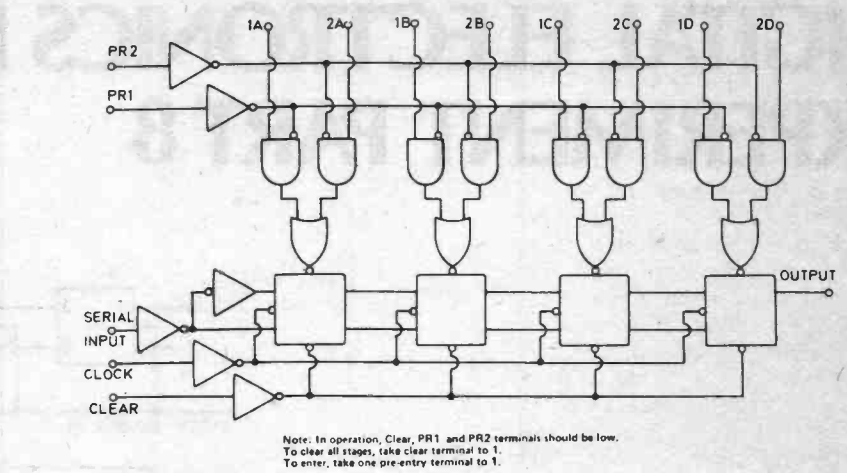


Fig 4. Schematic diagram of the 7494 shift register. Compare the number of flip-flops gates and inverters in this single chip with the number of packages needed to make this from 7400's and 7476's.

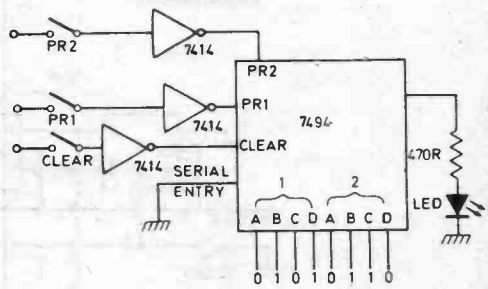


Fig 5. Connecting up the 7494 on the blob-board. Note that inverters have to be used on each switched line, as the preset and clear lines must be held at logic 0 for normal operation.

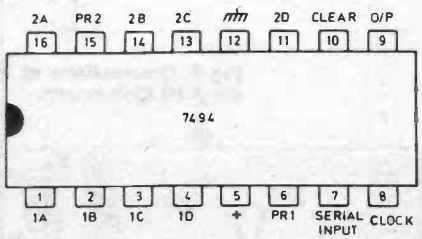


Fig. 3. Pinouts of the 7494

The interesting feature of the 7494, however, is the gated parallel inputs labelled 1A, 2A, 1B, 2B and so on. These act through a set of gates on to the preset inputs of the flip-flops, so that they are independent of the clock pulses. The gating is arranged so that either one or the other set of inputs can be "read" into the register. For example, imagine that the inputs with the 1 prefix are each connected to a signal input, 0 or 1, and that the inputs with the prefix 2 are each connected to another set of signals. We can use the pins marked preset 2 and preset 1 now to select which set of inputs is chosen and placed in the register. Imagine that preset 1 is at logic 1 and that preset 2 is at logic 0. Because of the inverters connected to the preset inputs, all the inputs with the 1 prefix are gated through to the OR gates which control the flip-flop presets. Because all the inputs with the 2 prefix are gated out, there will no input from these gates. The opposite process takes place if preset 2 is at logic 1 and present 1 is at logic 0. Note that these inputs must be operated so that both do not enter at the same time. The inputs should remain at logic zero during normal operation.

The output from the register is from pin 9, and will consist of one bit, 0 or 1 for each clock pulse fed in to the clock input, and at the leading edge of the clock.

Blob-board Work

Connect the supply lines to the 7494, +5 V to pin 5 and earth to pin 12. Now blob a connecting wire from the output of the debounced switch to the clock input of the 7494 on pin 8. Connect the preset 1 pin (pin 6) to an inverter whose input is from a push-button switch so that this pin can be momentarily set to 1; leave the other preset entry pin (pin 15) earthed. Now set up signals to enter on the 1-set of inputs, A, B, C, D on pins 1, 2, 3 and 4. For example, we can connect pins 1 and 3 to logic 1, and pins 2 and 4 to logic 0, so setting up the number 1010. This will be entered when the Pr1 pin is momentarily set to 1 by the inverter and switch, and the flip-flops will be set up to the number 1010.

Detector Work

We can detect this only at the output, (since we cannot connect to the Q outputs of the intermediate flip-flops) by connecting an LED and limiting resistor to the output pin, pin 9. Now blob a connection from the serial input, pin 7, to earth, so that as each clock pulse arrives a zero is fed into the first stage of the register. This ensures that the register stores 0000 after four clock pulses.

One Clock

Now switch on, and press the enter switch briefly. Use the clock switch to apply four clock pulses, and note the output on each pulse. The contents of the register should now be 0000, so that further clock pulses will not produce any "1" output. Another entry can be made by pressing the entry switch at any time. By connecting the second set of entry pins, and using the second pre-enter (Pr2) pin, we can enter another number. Connect up the second set of entry pins (16, 14, 13, 11) to give another number, and connect up the Pr2 (pin 15) terminal to the output of another spare inverter. Connect another push-button switch between the inverter input and the earth line, and try out the circuit again, entering the second number (after clearing) by pressing the enter switch momentarily. Check that this number is then read out at the output when the register is clocked.

DIGITAL ELECTRONICS BY EXPERIMENT PART 9

Arithmetic Units

So far, the work which we have carried out on ther blob-board has covered gating, flip-flops, counter and display stages and the use of a register. Within the limitations of 8 IC's, we cannot, of course, hope to cover every possible principle of digital electronics, and the IC's which were selected for the board were designed to reflect the applications of digital electronics most often seen in published circuits.

The two important topics of arithmetic and memory have not been specifically mentioned, partly because small projects seldom need arithmetic or memory (and large projects can make use of the more flexible facilities of a microprocesser, particularly if this incorporates a memory) and partly because the building blocks of arithmetic units (gates) and some types of memory (flip-flop) have been covered.

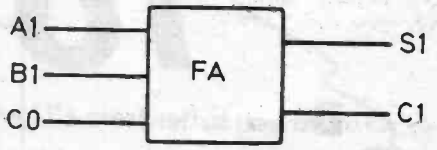
Nevertheless, in this last part we shall look at some of the circuitry we have not covered previously, and also at some systems which can be tried out in the board. In addition, it is useful to note that the board can now act as a very useful intermediate unit for experimental work on more advanced systems, since it can provide up to six clock oscillators, four flip-flops, four NAND gates, one register, and a complete circuit-and-display for one set of BCD digits.

Adding

Binary addition can be **serial** or **parallel,** of which parallel addition is more common. The **half adder** has the truth table in Fig. 1 and is used for the least significant digits of two numbers. Its output will be the sum (the digit which will appear in the final figure) and the carry which will be added to the next significant figure. The **full adder** circuit is used for all the next stages of the adder unit and has three inputs and two outputs; its truth table is shown in Fig. 2. The inputs to the full adder are the two digits A_1, B_1, and the carry C_0 from the previous half-adder stage. The outputs once again are the sum and another carry C_1 which is taken to the next stage. The total number of adding stages which will be needed must equal at least the total number of binary digits in the sum of the numbers.

A0	B0	S0	C0
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Fig 1. Half-adder symbol and truth table.



A1	B1	C0	S1	C1
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Fig. 2. Full adder symbol and truth table.

Half-adders and full adders can be made up using gates (Fig. 3) but once the principles have been checked it is easier to use IC's made for the job. The 7482 is a two bit full adder, whose internal circuitry, with truth tables, is shown in Fig. 4. From the diagram, we can see that the inputs are Co from the previous half-adder (which would be either an integrated full adder with no carry input, or made up from gates) and the second significant digits A_1 and B_1. The sum of this stage is obtained at the terminal marked S1, and the carry is internally connected into the second stage of the adder, whose inputs are B_2 and A_2 with outputs sum S2 and carry C_2. The next step up is the 7483, which is a four-bit adder and any requirements greater than this is dealt with by arithmetic units of much greater complexity.

In general, if more than a simple addition is needed, it is more economic to use LSI arithmetic units.

Memories

Memory units which are used in digital work come in several varieties. One class of memory is the volatile memory, based on flip-flops, which is cleared wherever power is switched off; this type could be used

in pocket calculators. Non-volatile memories are the types using pre-set registers (such as read-only memories or ROMs) or which use magnetic tapes or cores or other types of storage which are not erased when power is switched off. A simple type of volatile memory is a SISO shift register with its output connected back to its input so that the information is read back in after one complete set of clock pulses; this type of memory can only deliver its contents in the order in which they are stored. If the register has parallel outputs with gates, however, it becomes possible to find which digit (0 to 1) is stored in each flip-flop, so that, in the language of computing, random access is possible. This is a simple random access memory (RAM).

At this point it is worth pointing out that most memories in general use permit random access. The type of memories which we refer to as RAM are random access memories which can be written as well as read when suitable inputs are applied. They should properly be called random access read/write memories. Read only memories are usually also random access, but the information which is stored has been put there either by the manufacturer (in the design stage) or by the user (as with PROM) when the memory is first used. In the older types of PROM, using fusible links, the memory cannot be altered once programmed, except by fusing a few more links. The more modern UV erasable PROM's permit complete erasure and re-programming.

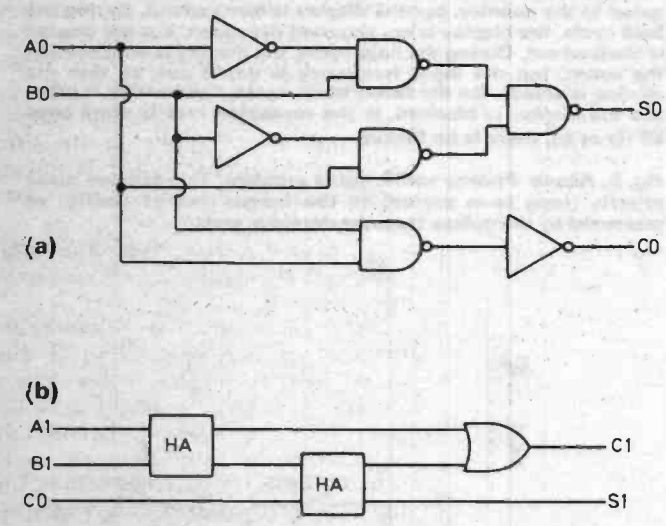


Fig. 3. Above: Adders (a) Half-adder circuit, using NAND-gates and inverters. (b) Full adder, using half adders and OR-gate.

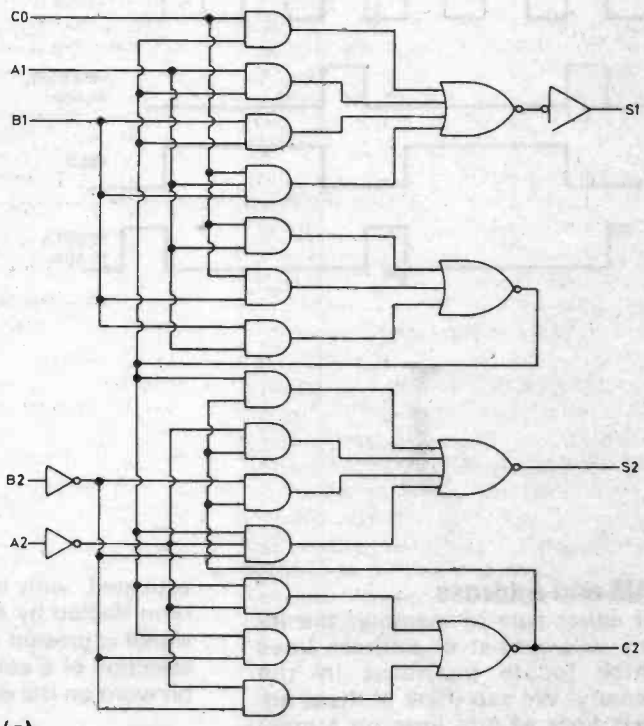


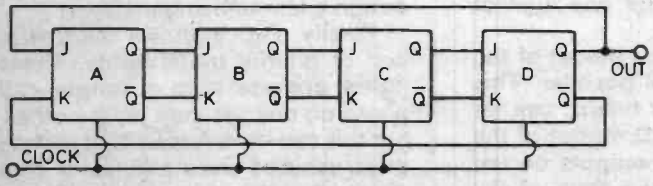
Fig. 4. Right: (a) Schematic of 7482 two-bit full adder. Note again the advantages of medium scale integration. (b) Truth table.

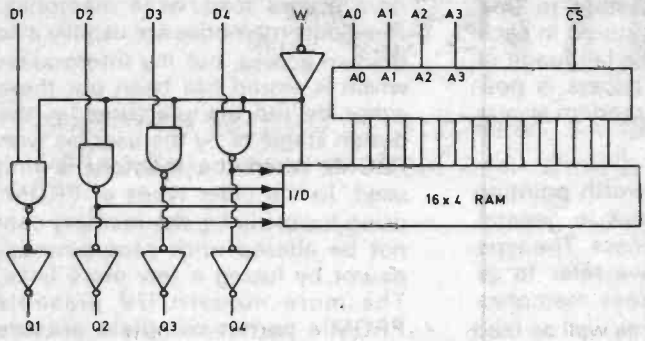
TRUTH TABLE

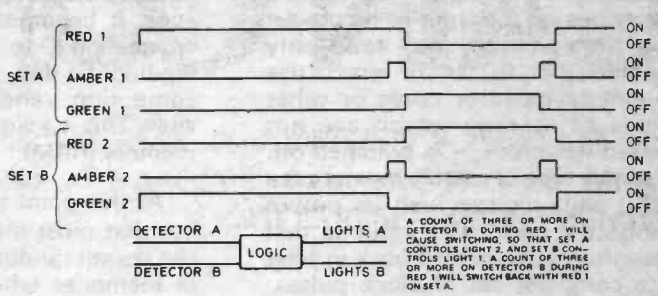
(b)

INPUTS				OUTPUTS					
				C0 = 0			C0 = 1		
A1	B1	A2	B2	S1	S2	C2	S1	S2	C2
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	0	1	0	1	1	0
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Fig. 5. Below: SISO shift register connected as a memory — the information must be read out in serial form.







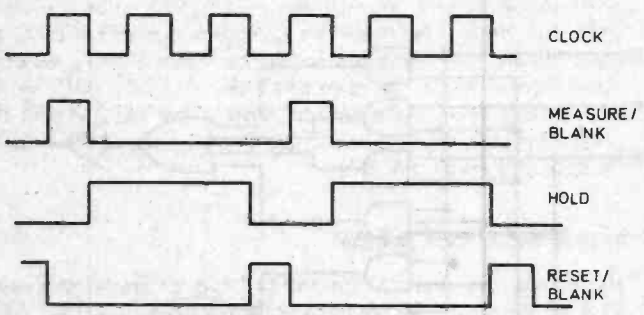


Fig. 6. Above left: 7489 RAM schematic, showing addressing system for 16 4-bit words.

Fig. 7. Below left: Pulses for frequency meter. During the measure/blank cycle, the input frequency being measured is gated to the counter, but the display is blanked out. During the hold cycle, the display is on, showing the count, but the display is blanked out. During the hold cycle, the display is on, showing the count, but the input frequency is gated out, so that the reading is steady. On the reset/blank cycle, the counter is reset and the display is blanked. If the repetition rate is more than 50 Hz or so, there is no flicker.

Fig. 9. Above: Priority traffic lights problem. This scheme gives priority (long term period) to the longer line of traffic, as measured by the pulses from the detector pads.

RAM and Address

For either type of memory, the inputs will consist of address lines which locate positions in the memory. We can think of these address lines as grid lines on a map, with each pair of crossing lines locating a point. When a point is addressed by voltages on the lines which 'cross' at the point, then the output will be the digit, 0 or 1, stored at that point.

As an example of addressing, Fig. 6 shows the arrangement of the 7489 RAM which is a 64 bit memory which uses four rows of 16 columns of storage. The rows are addressed by the inputs D_1, D_2, D_3, D_4, so that a four bit word can be read into each of sixteen columns. The columns are addressed by another four-bit word which is decoded (1011 = column 11; 0110 = column 6) by a decoder stage which then drives the column.

To write, a four-bit word is placed on the D inputs, and the write gate is activated, with the appropriate column slected by A_0—A_3. To read, no signal is present on the D lines, and selection of a column places a four-bit word on the output Q1—Q4.

Suggestions for Future Board Work

Figure 7 shows the sequence of pulses which are needed by a frequency meter. The system here is that pulses are counted for one unit, count is held on display, then cleared so that the system can be cleared for another (updating) count. The ICs on the board enable you to try this system out for one digit of counter.

Figure 8 shows the pinout of the 74141 BCD-decimal decoder. This IC, not used on our board, can be connected to the BCD output of the 7490 and will give outputs on ten pins, according to the state of the count. The active state is represented by a **zero** output on a pin, so that a zero output on the '7' pin (pin 10) represents a count of 7, and so on. Using this, could you design a ten-note jingle player?

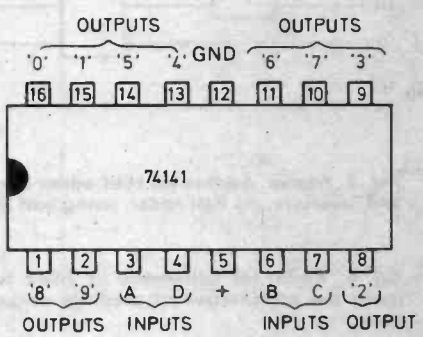


Fig. 8. Pinout of the 74141 BCD-Decimal decoder.

Finally, Fig. 9 shows the operation of priority traffic lights. These lights operate with a longer red phase on one set than on the other, but this can be reversed if more than three vehicles cross a detector strip during the long red period on one set of lights. This scheme needs a clock pulse, counters, register and gates, could you make one?

GAIN CONTROL

Tim Orr takes a detailed look at how gain can be controlled by another electronic signal, be it squarewave, sinewave or voice signal. This leads to some interesting circuits — from ducks to filters!

There are many cases in signal processing where the control of the gain is necessary. Some common examples are automatic volume controls in cassette recorders and in the IF sections of radio receivers. Also in professional audio equipment there is a whole range of compressor, expander, limiter and noise gate devices which find great use in recording and broadcast studios. Maybe you have wondered how the volume of the music drops when the DJ starts to talk and then fades up over up again when he stops. This process, known as voice over or "ducking" uses *voltage control of gain*.

Noise reduction systems such as Dolby and dBX employ voltage controlled amplifiers. Synthesisers and sound processors obtain effects such as ring modulation, automatic panning, frequency shifting, dynamic filtering, tremolo and envelope shaping also by the use of this technique.

Gaining gain

There is a wide variety of methods which can be used to obtain the gain control. This can be anything from constructing the variable gain element yourself from basic parts, to buying an IC or module designed specifically to solve your particular problem. Generally the solution is some sort of compromise, because unfortunately the problem of making high performance controlled gain cells (multipliers), is rather difficult and therefore the IC's tend to be rather expensive.

However with a bit of care a cost effective solution can usually be produced.

A good example is the AGC in a transistor radio. The transistors in the IF section have an h_{fe} that varies widely with the magnitude of their collector current. Thus, by sticking three transistors in series it is possible to vary their overall gain by about 40 dB, (x100), merely by controlling their collector currents. The AGC stops the audio output of the radio from varying as the radio reception conditions alter..

Electronic multipliers

When it is required to control the level of one signal with that of another, an electronic multiplier is used. This process is analogous to arithmetic multiplication. If input A is positive, Fig. 1, and input B is positive then the product (the output), will also be positive. If A goes negative then the product will be negative. If both A and B are negative then the product will be positive thus preserving the arithmetic rules.

If A and B are limited to be only one sign each then

Fig. 1

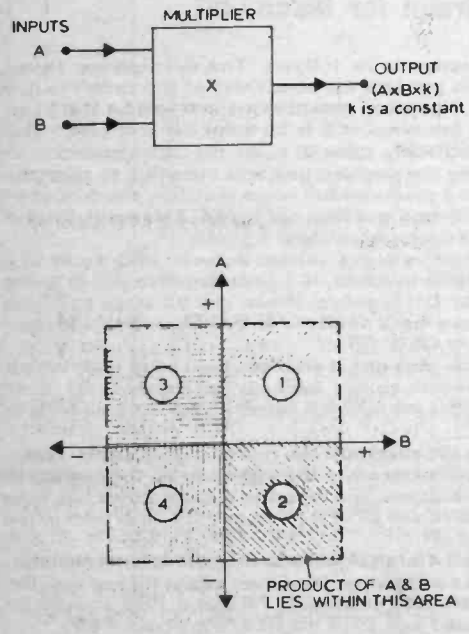
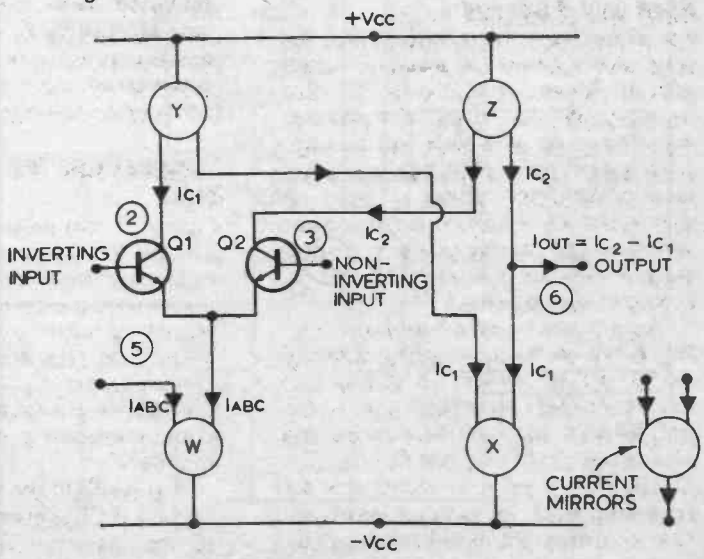


Fig. 2



Left: the principle behind electronic multipliers. The graph shows the possible outputs for a variety of combinations of input polarities.
Above: Internal workings of a CA3080, an Operational Transconductance Amplifier. Say that too fast and you'll need a new set of teeth.

the multiplier is known as a one quadrant multiplier. That is the product can only lie in one quadrant. If A can be both +ve and —ve, and B only of one sign then the multiplier is known as a two quadrant multiplier. This is what is called an amplitude modulator. The audio signal which is bipolar is A and the control voltage is B.

If A and B can be both +ve and —ve, the product can lie anywhere in the four quadrants and hence the multiplier is known as a four quadrant multiplier. This type of device is found in frequency shifters and ring modulators.

CA3080 — An OTA!

The CA3080 is a two quadrant multiplier, or to give it its full title, it is an Operational Transconductance Amplifier. It has a differential input and a single quadrant current input known as I_{ABC}, (amplifier bias current), Fig. 2. The differential transistor pair is used to steer the I_{ABC} current between the two transistors Q1, Q2. There is a region where the input differential voltage is linearly proportional to the percentage of current steered between the two transistors. This voltage region is fairly small, being about 20mV, but using the CA3080 in this area then a reasonably linear 2 quadrant multiplier can be obtained.

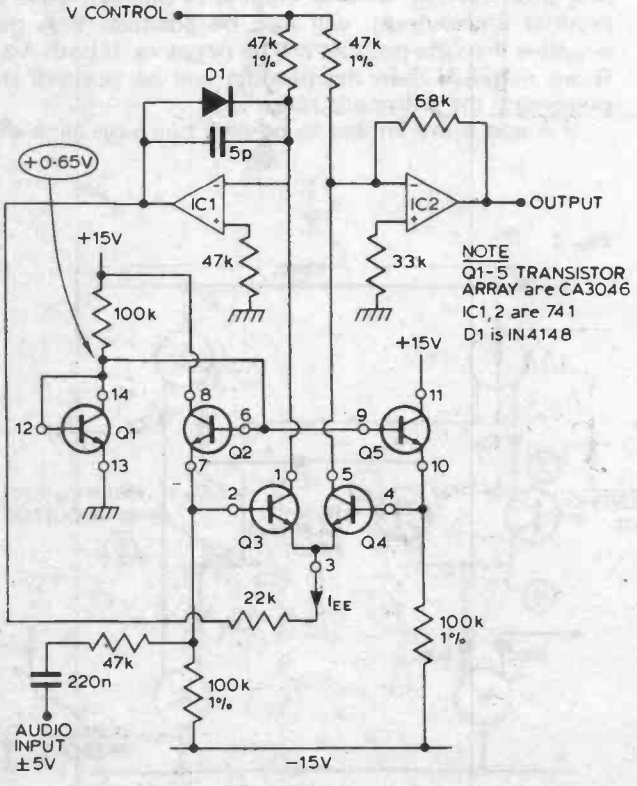
What has happened is the I_{ABC} current has been multiplied by the input voltage. The product is the difference between the two collector currents. This difference is extracted by the use of mirrors, current mirrors that is. The current mirrors can be attached to either the +ve or the —ve supply rail.

They have two terminals, and whatever current flows into one terminal, then the same flows into the other, which is why they are called mirrors.

What we want to do is take the difference between the collector currents of Q1 and Q2, I_{C1} is reflected from mirror Y and then from mirror X and then appears at the output. I_{C2} is reflected from mirror Z and then appears at the output. The two currents are subtracted from each other and the output current is thus $(I_{C2}—I_{C1})$, which is the product of $I_{ABC} \times V_{in} \times K$, where K is a constant. Note that the I_{ABC} current is also reflected from a current mirror on the negative rail.

The CA3080 is a low cost two quadrant multiplier and can be used to perform a wide variety of multiplication functions. The linearity of the device holds true for I_{ABC} variations of over three decades. When using this device keep I_{ABC} below 0.5 mA.

VCA Using CA3046 Array



The CA3046 is an array of 5 transistors which are all well matched and relatively cheap. Q3, 4 forms the differential transistor pair, IC1 controls the current and IC2 extracts the differential output current and turns it into an output voltage. The audio input is inserted into the base of Q3 but also connected to this node is the emitter of Q2. Q2 and Q5 serve to predistort the input signal, but they distort the signal the opposite way to which the multiplier distorts it. This is known as distortion cancelling, and it allows a larger signal level to be applied to the multiplier for the same percentage of distortion at the output. The larger input signal allows a higher signal to noise ratio to be obtained. Transistor Q1 is used to bias the bases of Q2, 5 to a suitable operating region.

Stereo Voice Over (Ducking) Circuit for Disco Unit

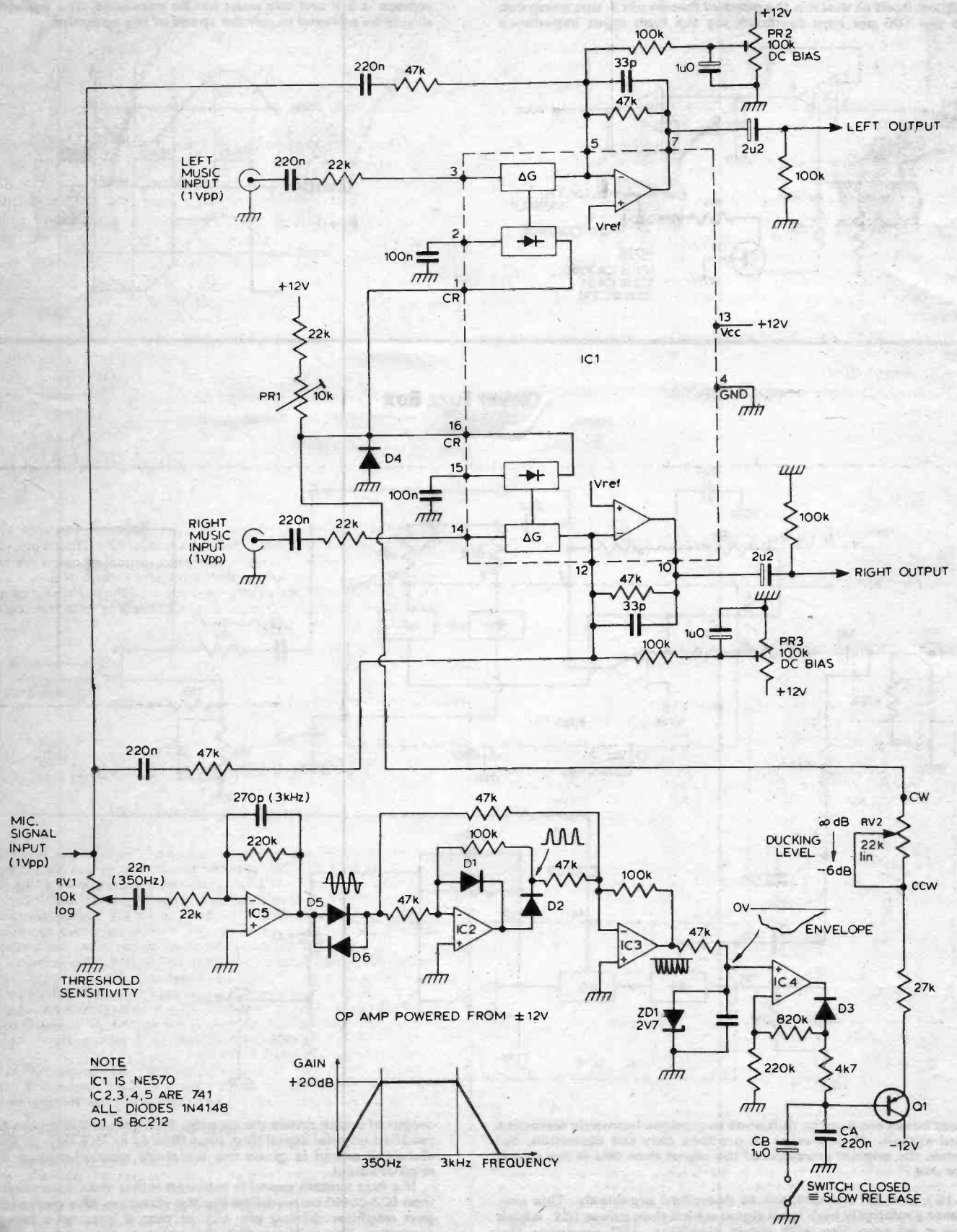
The circuit operation is as follows. The microphone signal comes via RV1. This pot sets the sensitivity of the circuit to the microphone signal. If it is too sensitive the unit will be 'ducking' every time the DJ breathes. IC5 is an amplifier and filter. The filter has been specifically tailored to fit the characteristics of speech, thus making the ducking unit less sensitive to spurious noise. IC2, 3 forms a precision full wave rectifier, the output of which is low pass filtered and then fed to IC4. This wave form is the envelope of the microphone input signal.

IC4 is a peak, negative going, voltage detector with a gain of x 5. When the DJ begins to speak, IC4 goes negative and in doing so pulls the base of Q1 negative. When the DJ stops speaking the base of Q1 rises back towards O V with a time constant determined by CA or CA + CB.

This is the release time and it controls the speed with which the faded down music comes back to full volume. Q1 is an emitter follower and is job is to rob current from the gain cells in the NE570.

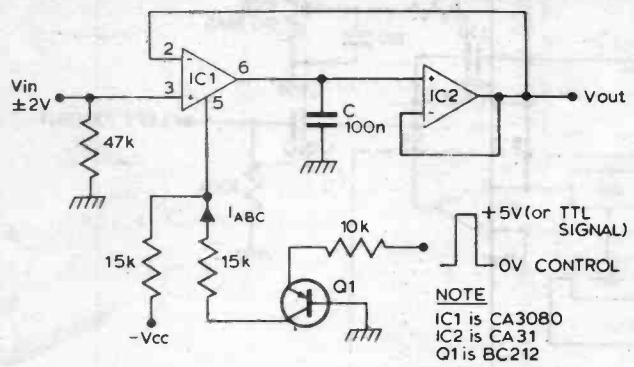
This current sets the volume of the two music channels. When the base of Q1 is pulled down to the negative rail, the amount of robbed current is maximum, and when no current flows into pins 1 and 16 of the NE570 and all of it flows into Q1, then both music channels are turned off.

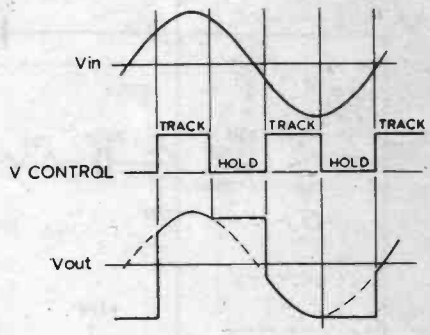
To set up PR1, put a large signal into the microphone channel, set RV2 so that it is a short circuit and then adjust PR1 so that the two music channels just close off. PR2 and PR3 should be adjusted so that pins 7 and 10 of the NE570 are both +6 V.


+12V
PR2
100k
DC BIAS
100k
33p
1u0
47k
220n
47k
LEFT OUTPUT
2u2
100k
LEFT
MUSIC
INPUT
(1Vpp)
220n
22k
ΔG
Vref
100n
CR
+12V
22k
PR1
10k
13
Vcc
+12V
IC1
4
GND
16
CR
D4
15
100n
Vref
RIGHT
MUSIC
INPUT
(1Vpp)
220n
22k
14
ΔG
100k
12
10
2u2
RIGHT OUTPUT
47k
33p
1u0
100k
PR3
100k
DC BIAS
+12V
220n
47k
MIC.
SIGNAL
INPUT
(1Vpp)
RV1
10k
log
22n
(350Hz)
22k
270p (3kHz)
220k
IC5
D5
D6
47k
100k
D1
IC2
47k
D2
100k
IC3
47k
CW
∞ dB
DUCKING
LEVEL
-6dB
RV2
22k
lin
CCW
0V
ENVELOPE
IC 4
27k
ZD1
2V7
820k
D3
220k
4k7
Q1
CB
1u0
CA
220n
-12V
SWITCH CLOSED
≡ SLOW RELEASE
THRESHOLD
SENSITIVITY
OP AMP POWERED FROM ±12V
NOTE
IC1 IS NE570
IC 2,3,4,5 ARE 741
ALL DIODES 1N4148
Q1 IS BC212
GAIN
+20dB
350Hz
3kHz
FREQUENCY

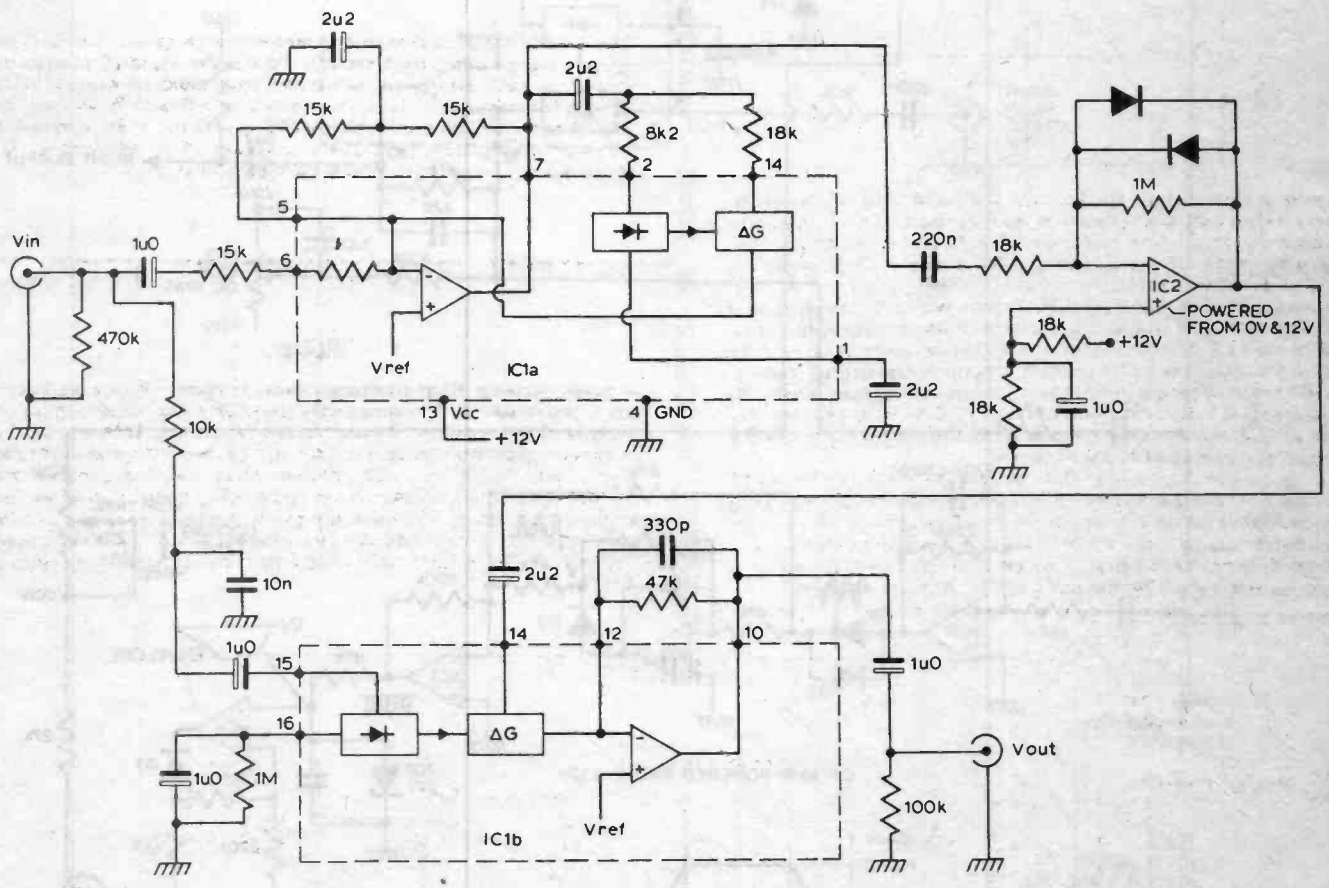
Track and Hold

In this example the CA3080 is used as a current controlled switch. When the control voltage is high, I_{ABC} is maximum, (0.44 mA) and the OTA gain is maximum. The voltage at pin 2 of IC1 adjusts itself so that it is the same as that on pin 3, this being due to the 100 per cent feedback via the high input impedance voltage follower IC2. When the control voltage is OV, I_{ABC} is zero and hence the gain of the OTA is zero. Therefore no current comes out of its output and so the voltage at the output of IC2 remains frozen (Hold mode). The maximum differential input voltage is 5 V and this must not be exceeded. The capacitor C should be selected to suit the speed of the operation.





Clever Fuzz Box

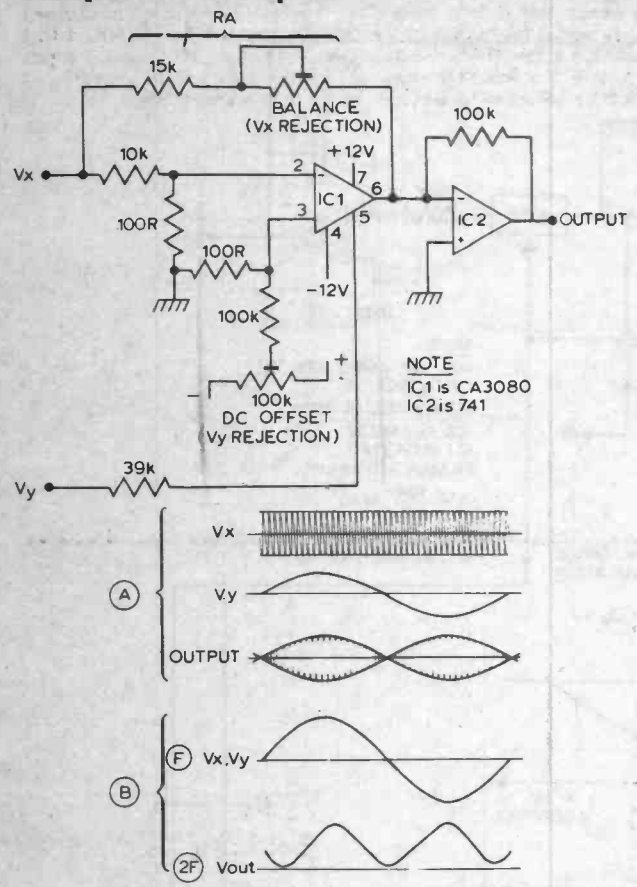


Fuzz boxes are used by guitarists to produce harmonic distortion and sustain. If you want to produce only the distortion, but retain the original envelope of the signal then this is the circuit for you.

IC1 is a 2:1 compressor as described previously. This produces a relatively high level signal which then drives IC2, which is a x 50 amplifier with diode clamping. IC2 produces the distorted (fuzz) found. This is then fed into the IC3 gain cell, the output of which drives the op amp. This gain cell is driven by the rectified original signal (low pass filtered at 1k5 Hz), so that the distorted sound is given the envelope characteristics of the original sound.

If a fuzz sustain sound is required rather than a dynamic fuzz then IC3 could be modified (by the inclusion of a clamped high gain amplifier driving pin 15) so that it acts as a low level expander. This will squelch the noise at the end of the fuzz period.

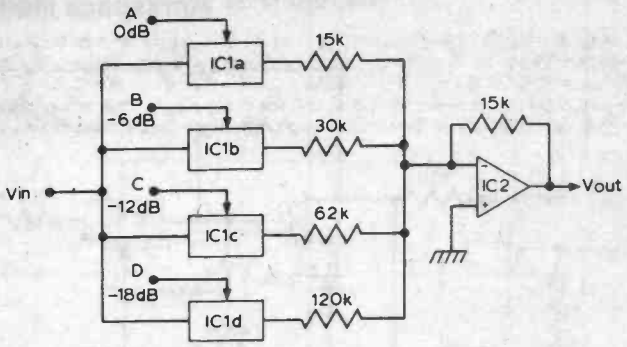
Four Quadrant Multiplication



By using a few circuit tricks, the CA3080 can be made to perform 4 quadrant multiplication. In fact the CA3080 performs 2 quadrant multiplication and the trick is to move the axis on the multiplying graph. If we ignore the RA resistor chain then we have a 2 quadrant multiplier circuit similar to that shown previously. Imagine that V_x is a 1kHz sine wave 1 Vptp and V_y is at 0V. The output of IC2 is a sine wave of fixed amplitude. Now if we connect RA, and adjust the balance control, it will be possible to cancel out the output, because the signal coming from IC1 is out of phase with that from the RA resistor chain. So with V_y set at 0 V there is no output for IC2. If V_y goes +ve, the output of IC1 will become greater than the current via the RA chain and the output of IC2 will grow.

If V_y goes—ve the current through the RA chain will exceed that from IC1 and the output of IC2 will grow, the phase being opposite to that when V_y was a sinewave from an oscillator, then this circuit could be used to generate ring modulation effects.

When V_x is set to 0V there may be some V_y breakthrough and this can be minimised by adjusting the V_y rejection preset.



0 ≡ -6V
1 ≡ +6V

A	B	C	D	GAIN
1	0	0	0	0dB
0	1	0	0	-6dB
0	0	1	0	-12dB
0	0	0	1	-18dB

POWERED BY ±6V

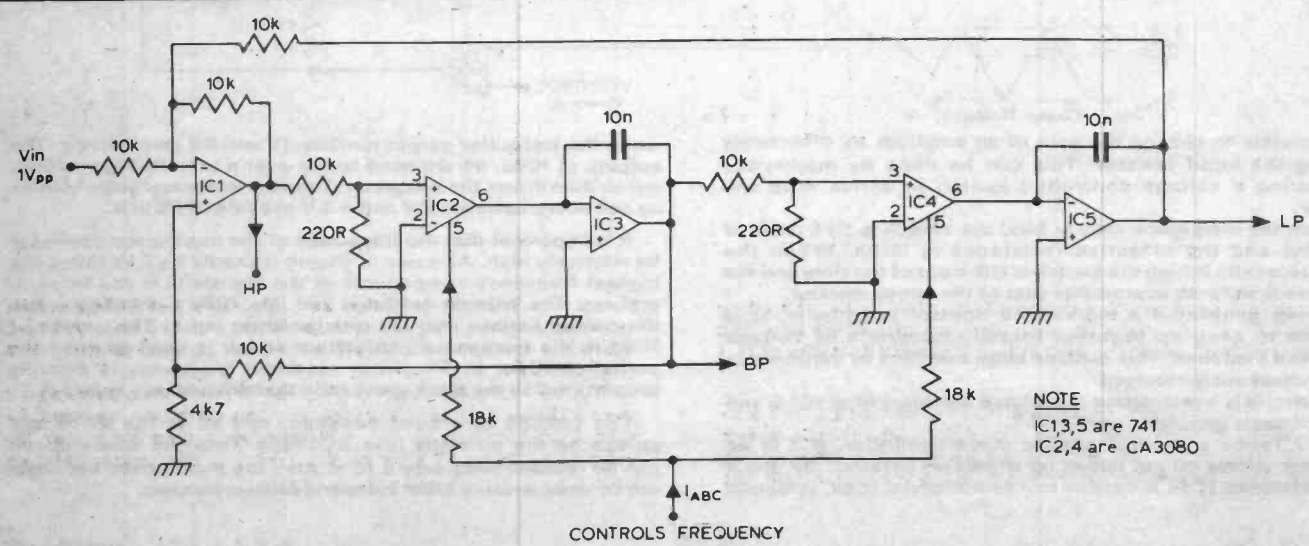
NOTE
IC1 is 4016
IC2 is 741

Voltage Controlled (Switched) Attenuator

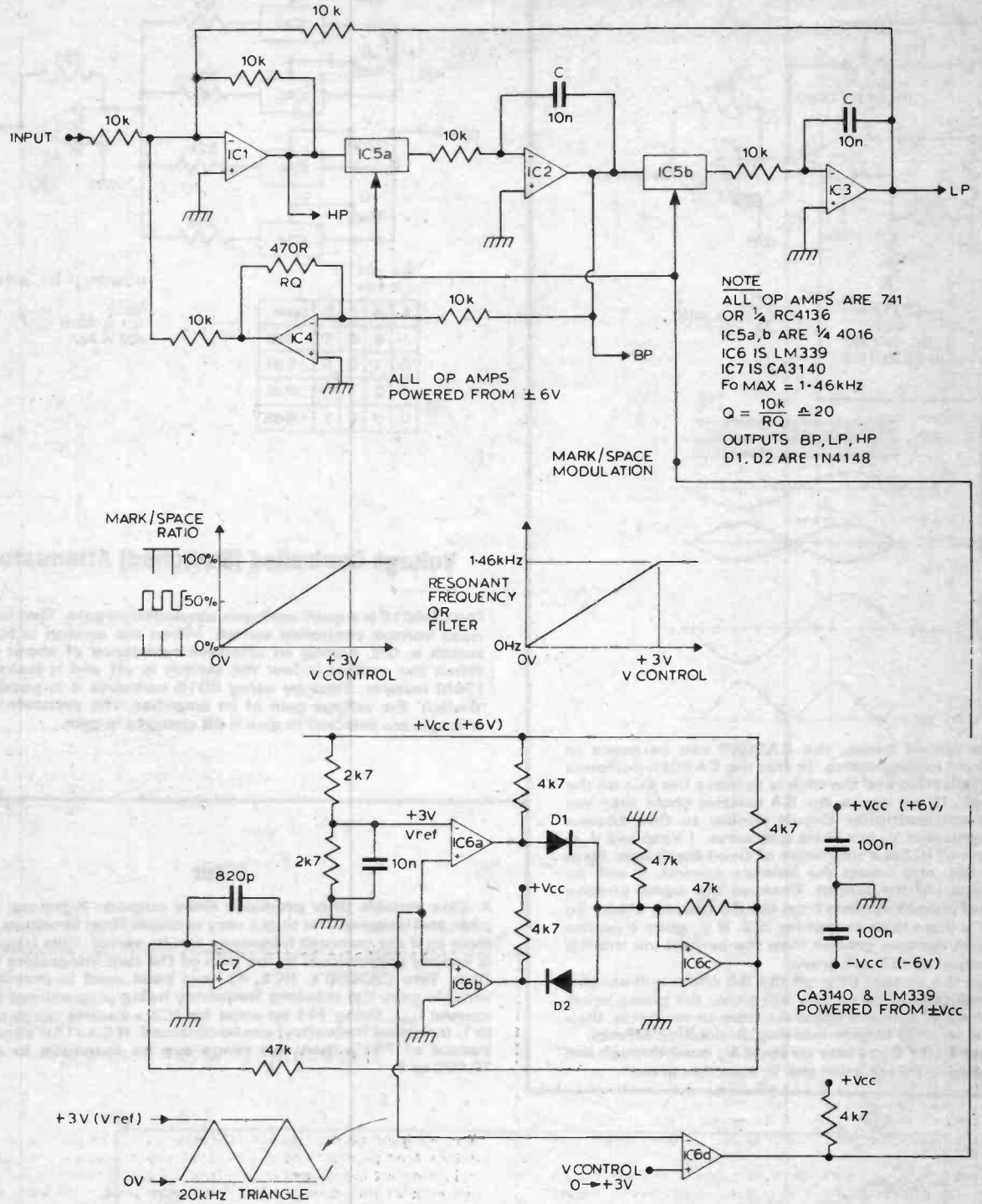
The CD4016 is a quad analogue transmission gate. That is, it is a quad voltage controlled switch. When the control is high the switch is ON, having an effective resistance of about 400R. When the control is low the switch is off and it looks like a 100M resistor. Thus by using 4016 switches it is possible to 'Switch' the voltage gain of an amplifier. The resistors in this example are selected to give 6 dB changes in gain.

Filter

A state variable filter produces three outputs: highpass, bandpass, and lowpass. It is thus a very versatile filter structure, even more so if the resonant frequency can be varied. This frequency is linearly proportional to the gain of the two integrators in the filter. Two CA3080's, (IC2, 4) have been used to provide the variable gain, the resonant frequency being proportional to the current I_{ABC}. Using 741 op amps for IC3 a control range of 100 to 1, (resonant frequency) can be obtained. If CA3140's are used instead of 741's then this range can be extended to nearly 10,000 to 1.



Markspace Modulated Universal Filter



It is possible to change the gain of an amplifier by effectively altering the input resistor. This can be done by markspace modulating a voltage controlled switch in series with the resistor.

When the markspace ratio is low, the switch is OFF most of the time and the effective resistance is large. When the markspace ratio is high the switch is ON most of the time and the effective resistance approaches that of the series resistor.

Having generated a markspace control waveform, it is possible to gang up together literally hundreds of voltage controlled switches. This enables large numbers of variables to be simultaneously changed.

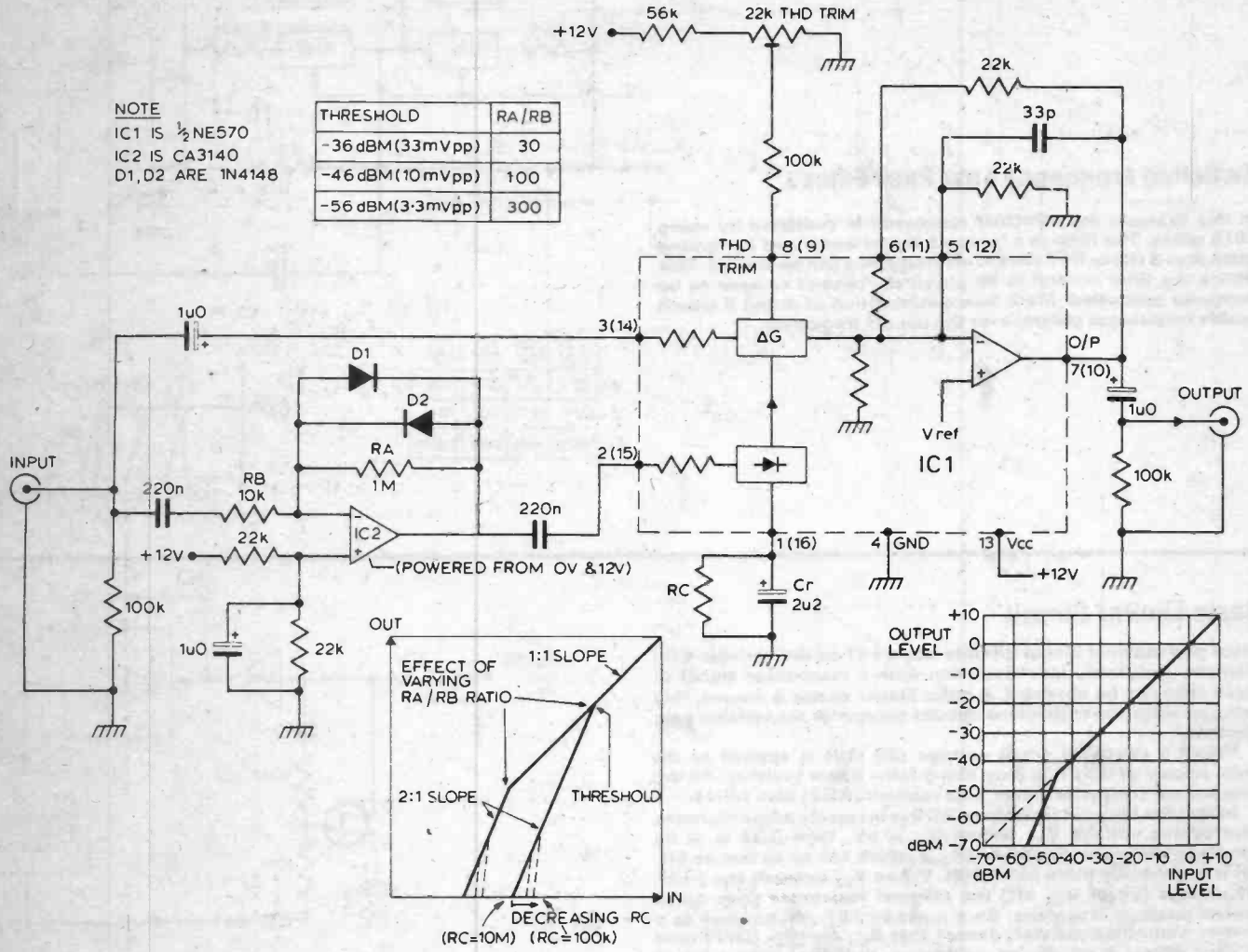
The circuit is a markspace modulated universal filter IC1-5 and the markspace generator itself IC6-7.

IC6-7 forms a triangle square wave oscillator. IC7 is an integrator whose output ramps up and down between OV and a + 3 V reference. IC6a, b, c are all fast comparators. IC6a, 6b detect when the integrator output reaches 3V and 0V respectively. The outputs of IC6a, 6b are used to flip over a schmitt trigger IC6c, which then drives the integrator. Thus the integrator output ramps up and down between OV and +3 V at a rate of 20 kHz.

It is important that the frequency of the markspace oscillator be relatively high. As a rule of thumb it should be 2 ½ times the highest frequency components of the signals that you hope to process. The triangle output is fed into IC6d's inverting input, the control voltage into the non inverting input. The output of IC6d is the markspace modulation which is used to drive the switches IC5a, b. The filter resonant frequency is directly proportional to the mark space ratio that drives these switches.

The LM339 is a quad package, and so is the 4016 and so can be the op amps (use RC4136). Thus the whole circuit can be realised with only 4 IC's. Also the mark space oscillator can be used to drive other independent comparators.

Two Channel Low Level Expander/Noise Gate



It is often required that a rather noisy signal be cleaned up a bit. This is not possible to do continuously, but it is possible to clean up noise in what was initially the gaps. The results of this cleaning up process can quite often be heard when telephone conversations from "foreign correspondents" are broadcast.

By turning down the signal level in the gaps, (by performing a low level expansion) the perceived sound quality improves dramatically.

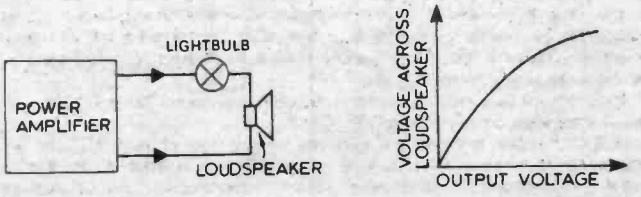
The circuit performs just such an expansion. The input signal passes through the variable gain cell and then appears at the op amp output. The gain of the gain cell is controlled by the signal coming from IC2. This is a high gain amplifier with diode clamping, so that the output swing is limited to about 1VO ptp. Therefore for input signals of 10 mV pp to 10 V pp, the output of IC2 remains at about 1VO ptp to 1V2 ptp.

So, for this range of input voltages the gain of the gain cell remains roughly static. Now when the input level drops below 10mV, the output of IC2 will start to fall and so will the gain of the gain cell. This produces a 2:1 downwards expansion curve, which means that the output then gets quieter at a rate faster than the input. To accentuate this effect, a bleed resistor can be placed in parallel with Cr.

The resistor robs some of the current that would have otherwise gone to the gain cell and causes the input output curve to roll off much more rapdily at low signal levels. Also, by varying the resistor ratio of RA/RB, the expansion threshold level can be altered.

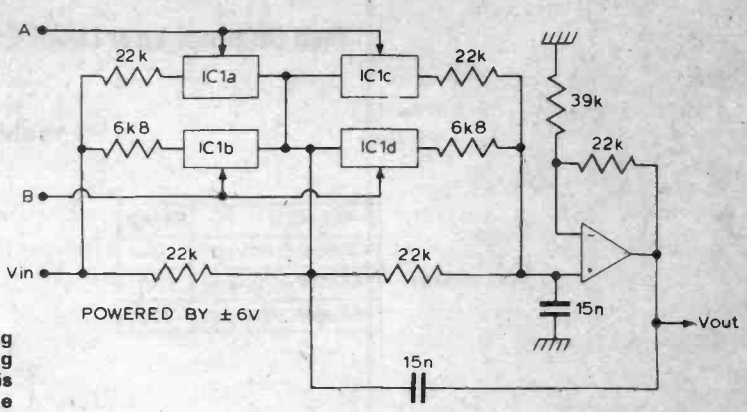
Incredibly Simple Compressor

Not all gain control systems need be complicated or indeed active. One product which I saw advertised was a compressor to help prevent loudspeaker overloads. All it was was a lightbulb in series with the loudspeaker. When the power exceeds a certain level, the lamp will turn on, glow, its resistance increases dramatically and hence a bigger percentage of the power output is dissipated in the lamp. A nice, simple solution, but I think it would require some experimentation to find the right sort of car headlamp bulb!

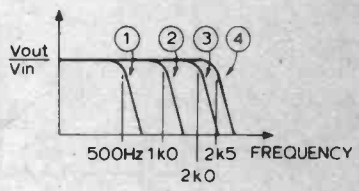


Switched Frequency Low Pass Filter

In this example the effective resistance is switched by using 4016 gates. The filter is a lowpass Butterworth and by turning gates A or B ON or OFF the cut off frequency can be altered. This allows the filter control to be physically remote or even to be computer controlled. Mark Space modulation of A and B would enable continuous control over the cut off frequency.



	①	②	③	④
A	OFF	ON	OFF	ON
B	OFF	OFF	ON	ON
Fc	500Hz	1kHz	2kHz	2·5kHz



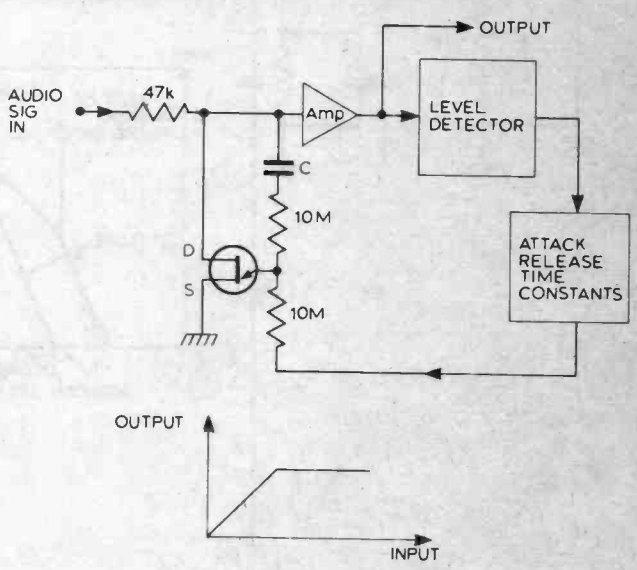
Basic Limiter Circuit

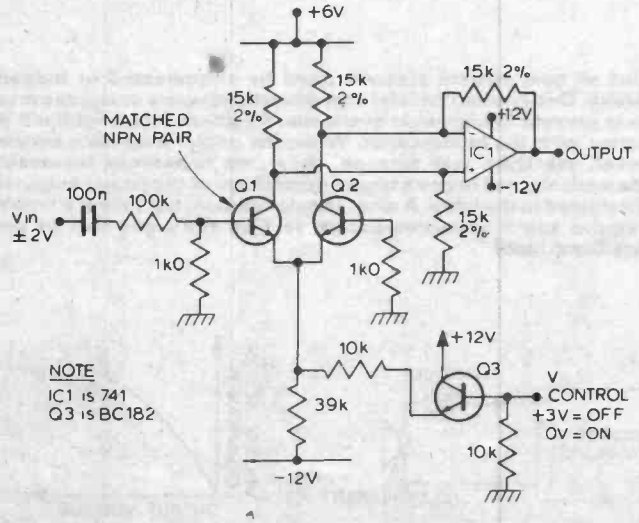
Most professional limiter circuits use a FET as the variable gain element. Relatively low distortion with a reasonable signal to noise ratio can be obtained. A basic limiter circuit is shown, this being no different to previous circuits except for the variable gain element.

When a relatively small voltage (20 mV) is applied to the drain source of a FET, it acts like a fairly linear resistor. As the gate source voltage is varied, this resistor (RDS) also varies.

In fact the channel resistance RDS is inversely proportional to gate source voltage V_{GS}. When V_{GS} is oV, then RDS is at its generally minimum resistance (R_{ON}) which can be as low as 5R, but it is generally more like 100R. When V_{GS} exceeds the pinch off voltage (Vp or V_{GS} off) the channel resistance goes up to several hundred Megohms. So a junction FET can be used as a voltage controlled resistor, except that R_{ON} and V_{GS} (OFF) tend to vary widely from device to device. However with a bit of perseverance suitable devices can be selected and made to work.

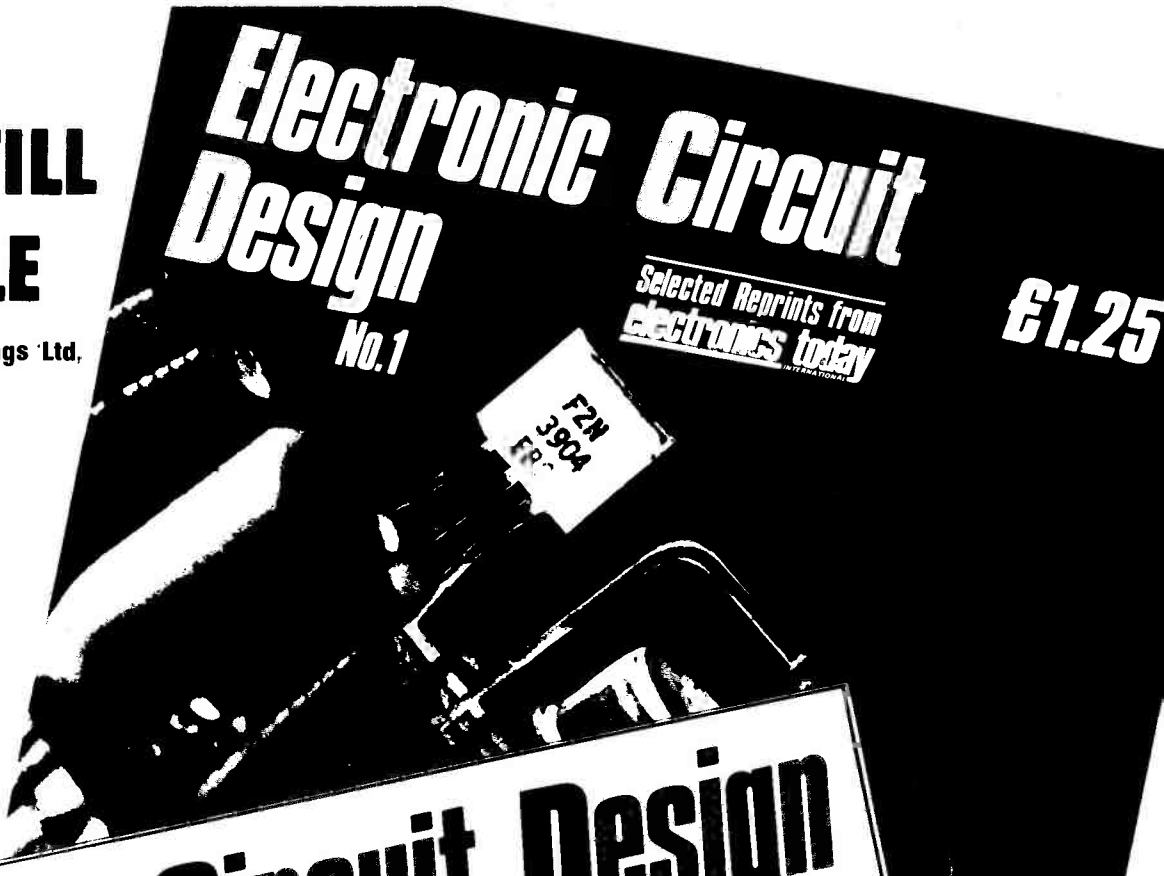
One circuit trick that greatly reduces distortion is shown here. Half of the audio signal at the drain of the FET is presented to the gate. This is superimposed on top of the control voltage and produces a distortion cancelling effect. Distortion levels below 0.1% can be achieved using this technique.





Transistor VCA

A circuit similar in operation to a CA3080 can be constructed with a matched pair of transistors and an op amp. Transistors Q1, 2 form a differential transistor pair which is used to steer whatever current is available between the two collectors, just as in the CA3080. the difference between the collector currents is equal to the product of the input voltage times the current I_{EE} times a constant. This difference is extracted by the differential amplifier IC1. The current I_{EE} is controlled by Q3. As the control voltage goes positive, Q3 robs most of the current flowing down the 39k resistor, and hence I_{EE} and the output of IC1 decrease.



Electronic Circuit Design No. 1

Selected Reprints from electronics today INTERNATIONAL

AUTUMN 1979

Introduction

Since ETI was originally launched in Britain in April 1972 we have published nearly 5000 pages of editorial matter; much of this has been devoted to electronic projects of course. In our history we have republished the best of these projects in Top Projects No 1-No 7, we have also reprinted the Tech-Tips and other circuits in Circuits Book No 1 and No 2 and our beginners series Electronics-It's-Easy is now on its third reprint.

We have not however, until now, brought together the best features dealing with electronic design. Nearly 1500 pages have been devoted to this in recent years and this special is the first of a series of three which will bring together the best 250-300 of these.

Although some features are from quite early issues they have only been included because we feel that 'age has not withered them'.

We hope that the contents help the reader understand at least some of the aspects of electronic circuit design.

Halvor Moorshead
Editorial Director — ETI

Contents

Edited by: Halvor Moorshead, assisted by Margaret Hewitt and Steve Braidwood

Production: Diego Rincón, Dee Camilleri, Loraine Radmore

...ada (for cover design)

...ternational Special
...2H 0EE

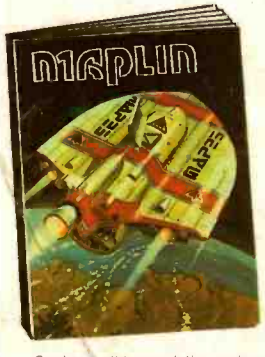
MAPLIN

A 63-key ASCII keyboard with 625-line TV interface, 4-page memory and microprocessor interface. Details in our catalogue.

Our catalogue even includes some popular car accessories at marvellous prices.

A 10-channel stereo graphic equaliser with a quality specification at an unbeatable price when you build it yourself. Full specification in our catalogue.

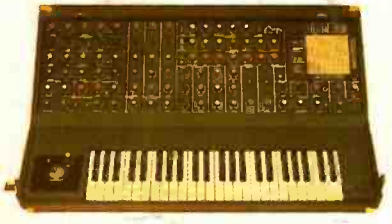
These are just some of the metal cases we stock. There are dozens of plastic ones to choose from as well.
See pages 52 to 57 of our catalogue.



A massive new catalogue from Maplin that's even bigger and better than before. If you ever buy electronic components, this is the one catalogue you must not be without. Over 280 pages – some in full colour – it's a comprehensive guide to electronic components with hundreds of photographs and illustrations and page after page of invaluable data.

Our bi-monthly newsletter contains guaranteed prices, special offers and all the latest news from Maplin.

Mobile amateur radio, TV and FM aerials plus lots of accessories are described in our catalogue.



A digitally controlled stereo synthesiser the 5600S with more facilities than almost anything up to £3,000. Build it yourself for less than £750. Full specification in our catalogue.

A superb range of microphones and accessories at really low prices. Take a look in our catalogue – send the coupon now!

An attractive mains alarm clock with radio switching function and battery back up! Complete kit with case only £18.38 (incl. VAT & p & p) MA1023 module only £8.42 (incl. VAT).

Post this coupon now for your copy of our 1979-80 catalogue price 70p.

Please send me a copy of your 280 page catalogue. I enclose 70p (plus 37p p&p). If I am not completely satisfied I may return the catalogue to you and have my money refunded. If you live outside the U.K. send £1.35 or ten International Reply Coupons.
I enclose £1.07.

NAME

ADDRESS

ECD2

A superb technical bookshop in your home! All you need is our catalogue. Post the coupon now!

A hi-fi stereo tuner with medium and long wave, FM stereo and UHF TV sound! Full construction details in our catalogue.

Add-on bass pedal unit for organs. Has excellent bass guitar stop for guitarists accompaniment. Specification in our catalogue.

MAPLIN ELECTRONIC SUPPLIES LTD

All mail to:–
P.O. Box 3, Rayleigh, Essex SS6 8LR.
Telephone: Southend (0702) 554155.
Shop: 284 London Road, Westcliff-on-Sea, Essex.
(Closed on Monday).
Telephone: Southend (0702) 554000.