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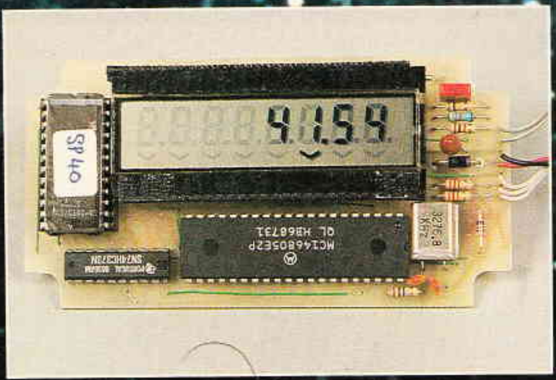

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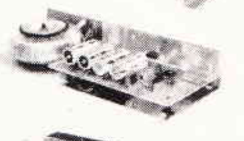

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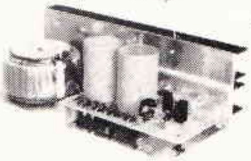

OMP/MF300 Mos-Fet Output power 300 watts R.M.S. into 4 ohms, Frequency Response 1Hz - 100KHz −3dB, Damping Factor 350, Slew Rate 60V/uS, T.H.D. Typical 0.0008%, Input Sensitivity 500mV, S.N.R. −130dB, Size 330 × 147 × 102mm. PRICE
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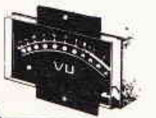

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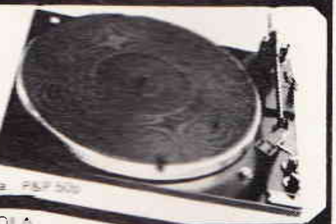

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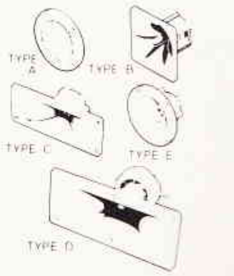

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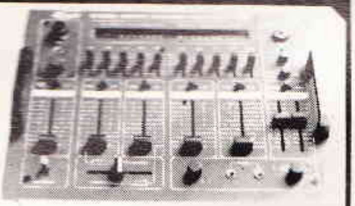

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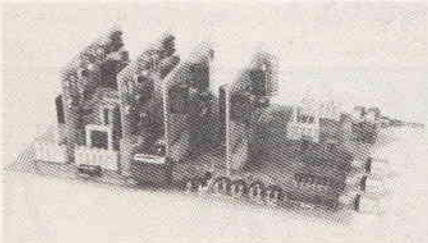

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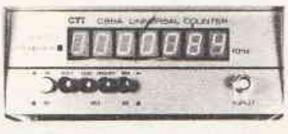

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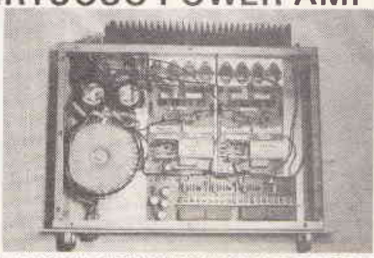

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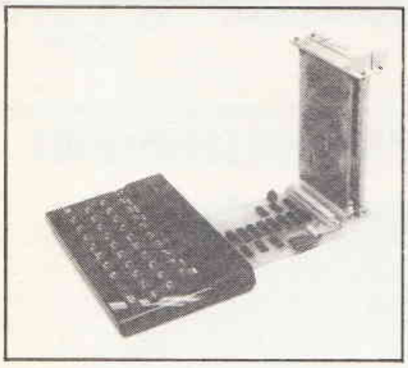

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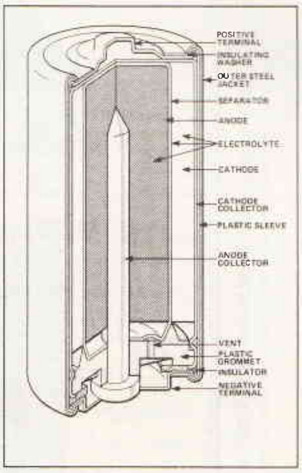

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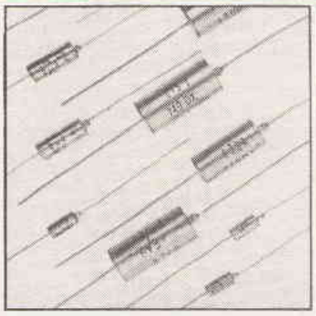

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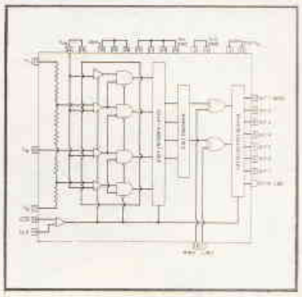

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Dynamic Noise Reduction
This month's *First Class* project for beginners is a hi-fi noise reduction system for Manu Mehra which requires no special source material.

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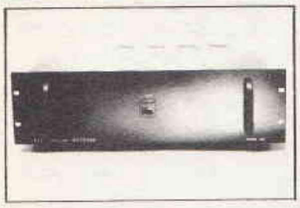
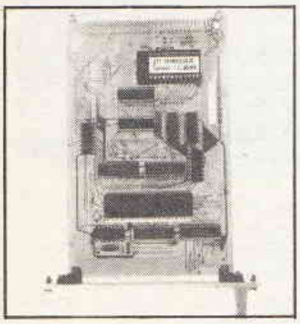
MAY 1988

34 **Special Offer**



36 **Virtuoso Power Amplifier**

Graham Nalty continues to build his top flight power amplifier. This month it's the all-important power supply which takes shape.



40 **Spectrum Co-processor**

Graeme Durant rounds off this ingenious project with a discussion of the software and presents the co-processor operating system listing and a demonstration Spectrum Basic program to use the complete system.

46 **Tech Tips**

More circuits from readers around the world
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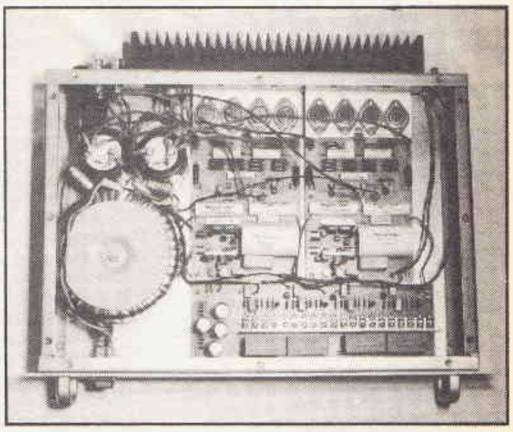
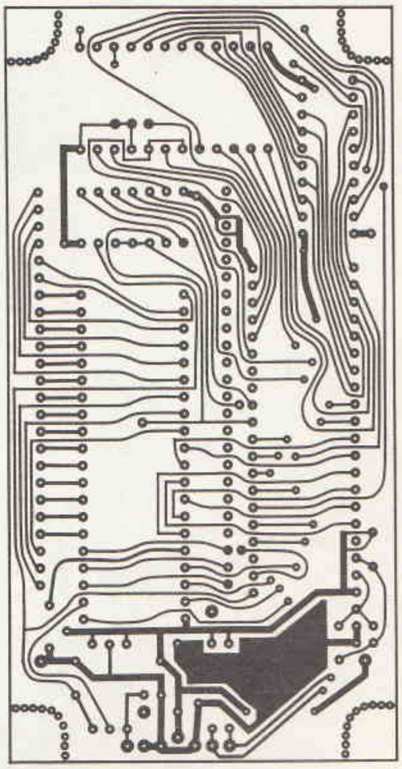




Cover background photograph courtesy Don Carroll and The Image Bank. Bicycle from Cycle Logical, New Cavendish Street, London W1.

NEWS

KICK ASTRA

The delay in getting the Astra STV satellite into the skies has enabled them to rejig the twiddly bits and increase the power.

Inside the improved 52dBW footprint the transmissions should now be receivable on a 60cm dish (but try before you buy) rather than the 85cm required before the requirement.

Astra now has a definite Arianne comprising launch date (well *another* definite launch date) in the last week of October and should be operational within three weeks of blast-off.

Satellite Technology Systems of Bristol will be producing half a million 60cm dishes next year for British and European systems suppliers and is keen to introduce dishes in pastel colours to blend into the environment (right on man!).

For details of Astra's elevation and azimuth see January's ETI.

Satellite Technology Systems are at Satellite House, Blackswarth Road, Bristol BS5 8AU. Tel: (0272) 554535.

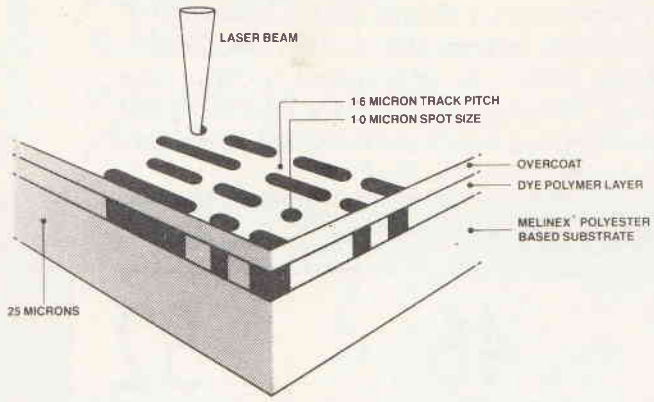
STRIPPERS COME OF AGE

Ceka (the toolmaker) has introduced a new wire stripper that can be precisely set to the wire diameter and length of insulator to be cut, enabling fast and accurate stripping.

The stripper cuts axially (see photograph) which will be useful in tight corners where conventional strippers are cumbersome.

The price for accuracy is quite high — the wirestripper currently retails at £25.50. Contact Ceka, Pwllheli, Gwynedd LL53 5LH. Tel: (0758) 612254.

DIGITAL PAPER



Indelible optical data storage medium at ⅓p for a megabyte is the impressive claim ICI is making for Digital Paper — 'a new concept in data storage.'

ICI Digital Paper is a dye polymer optical recording medium coated onto a polyester based substrate so the paper can be flexible and rolled onto tapes or stuffed into cassettes.

A ½in tape on a 10½in spool is capable of storing 600 gigabytes — enough to store 1000 CDs or 300 full length feature films.

Creo of Vancouver is working with ICI on a drive for a one terabyte tape (on a 12in spool with tape 35mm wide).

Digital Paper flexible disk drives are also being developed. Watch this space for developments.

Contact ICI, PO Box 6, Bessemer Road, Welwyn Garden City AL7 1HD. Tel: (0707) 323400.

PASS THE PORT

User ports can be added to the Amstrad PCW using a new parallel input/output interface from SM Engineering.

The interface measures 11×5×3cm and connects to the Amstrad's expansion socket using an IDC edge connector and 50-way ribbon cable.

Four 8-bit ports are provided with 5V and 10V supply lines for whatever you choose to plug into it.

SM is also selling a range of add-ons to be used with the interface, including an 8-channel ADC, a 'breakout' module (no, *not* the game — it provides further facilities for add-ons) and an I/O test module which checks if your software does what you think it does.

The interface itself costs £55.95, the breakout is £18.95 and the ADC is £39.95. Modules get 10% discount if bought with the interface.

Contact SM Engineering, St Georges, Lion Hill, Stone Cross, Pevensey, East Sussex BN24 5ED. Tel: (0323) 766262.

THE LIGHTS GO DOWN

Lights can be dimmed at the touch of a pinkie with the latest kit from Electronic and Computer Workshop.

The kit can handle a 2A lighting load and switches on or off at a brief touch, dimming up and down in a 3½ second cycle if contact is maintained — in a similar manner to the ETI programmable touch dimmer back in April 1980.

The kit is available for £16.22 inclusive from ECW, Unit 1, Cromwell Centre, Stepfield, Witham, Essex CM8 3TH. Tel: (0376) 517413.

WANTED

International Education Services of Tokyo is looking for graduates and professionals to teach in Japan. The employment contract usually lasts for a year and involves teaching anything from technical briefings to learning to shake hands properly.

British teachers are especially welcome but should be prepared for a hard working week and the culture shock of living in a very different country.

Interested applicants should write to International Education Services, Shin-Taiso Building, 10-7, Dogenzaka 2-chrome Shibuya-ku, Tokyo 150, Japan.

THE LISTENING BANK

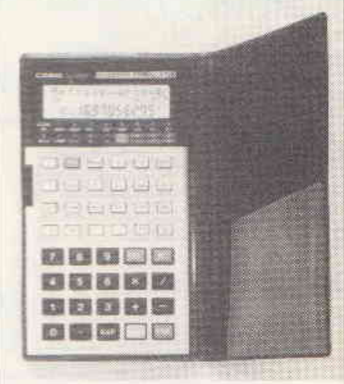
Bankers with the Royal Bank of Scotland can now phone their local branch computer direct and make transfers and order services by speech recognition.

The service is called Phoneline and is operating in only four branches at the present time. Customers are given a PIN and can choose their own password (within reason . .). These are compared to the caller's voice by British Telecom's Telephone Banking System which responds with the dulcid tones of a sampled Royal Bank of Scotland employee.

Facilities available are statements, details of your last six transactions, transfer between accounts and bill paying to certain accounts (such as BT themselves).

The bank and BT are running an example transaction phone-in, which you can hear on (0473) 227848. For full details of the service ring The Royal Bank of Scotland on 031-556 8555.

SPECIAL fx



If you are searching for a calculator to see you through the summer, the new Casio fx-5000F is worthy of consideration — although it may take you several weeks to learn to use it.

The fx-5000F carries a mammoth 288 functions, which include 128 common formulae (which unfortunately cannot be unprogrammed for exams, honest they can't Sir).

Your own programs can be up to 675 steps and can be edited versions of the preprogrammed formulae, a reasonably simple task which saves a lot of time.

The fx-5000F also handles hex, octal and binary and can convert to and from decimal.

And not only does it handle alphabetic characters, it even has the whole Greek alphabet.

The fx-5000F retails at £39.95 and is available from all Casio stockists.

CHIP KITS FOR KIDS

Chip Kit is a complete low cost electronics teaching package aimed at GCSE physics and electronics departments across the country.

The Polytechnic of Wales has developed the three modules covering transistors, op-amps and logic design. They are designed to fit precisely to the syllabus and provide all the necessary theory and background for both the teacher and student.

In many schools electronics is being taught by rather confused metal and woodwork teachers as part of the Craft, Design and Technology courses. The Polytechnic is offering training courses to enlighten these wary non-specialists and the workbooks use a step by step approach which can provide a course structure and simplify teaching.

The kits could also be useful for companies and graduates working in fields other than electronics who require a basic grounding in practical circuits and theory.

The three kits each cost about £35. For full details contact Dr Murray-Shelley, The Electronics Centre, The Polytechnic of Wales, Pontypridd, Mid-Glamorgan CF37 1DL. Tel: (0443) 480480 ext 2536.

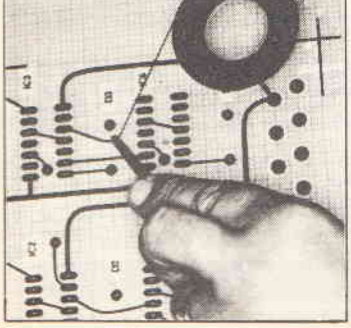
ON DRAUGHT

The new catalogue of draughting aids for electronics designers is now available from Circuitape in Aylesbury.

The 52 page catalogue contains just about every artwork symbol you can think of for PCB design and circuit diagrams — and several that we couldn't understand.

Circuitape can also produce custom printed draughting aids for those really obscure symbols that you've invented yourself.

The catalogue and price list are available from Circuitape, Chamberlain Road, Aylesbury, Bucks HP19 3DF. Tel: (0296) 23451.



HIRE PLACE

Alpha Electronics has introduced a hire department offering normally prohibitively expensive test equipment on a daily, weekly or monthly basis.

A leaflet outlining the system is available free from Alpha with prices and hire information.

Prices are about 5% of retail price for a week's hire.

Contact Alpha, Unit 5, Linstock Estate, Atherton, Manchester M29 0QA. Tel: (0942) 873434.

BATTERY ASSORTMENT

STC is offering a free 8-page colour brochure covering their range of cells and batteries — useful to have at hand after you've read Vivian Capel's treatise on the world of batteries in this month's issue.

The catalogue ranges from the normal zinc-carbon and large lead-acid products to memory protection lithium chromium oxide and lithium oxide types.

For your copy contact The Battery Group, STC, Edinburgh Way, Harlow, Essex CM20 2DF. Tel: (0279) 626777.

DIARY

Electronic Packaging Seminar — April 7th
The Welding Institute, Cambridge. Report on recent visit to Japan. Contact The Welding Institute on (0223) 891162.

HF Radio Systems And Techniques — April 11-13th
The IEE, London. Conference organised by the IEE and The Institute of Mathematics and its Applications. Contact IEE on 01-240 1871.

Safe Nuclear Power — April 12th
Scarborough Lecture Theatre, University of Durham. Lecture by C Smitton. Contact IEEIE on 01-836 3357.

Scottish Computer Show — April 12-14th
Scottish Exhibition Centre, Glasgow. Contact Cahners Exhibitions on 01-891 5051.

Computer Recruitment Fair — April 15-16th
New Century Hall, Manchester. Contact Intro Ltd on (0491) 681010.

Computer Recruitment Fair — April 22-23rd
Watershed, Bristol. Contact Intro Ltd on (0491) 681010.

Softeach 88 — 23-24th April
Heathrow Penta Hotel, London. Contact Softsel on 01-568 8866.

ATE 1988 (Automatic Testing & Test Instrumentation) — April 26-28th
Metropole Exhibition Centre, Brighton. Contact Network Events on (0280) 815 226.

British Electronics Week — April 26-28th
Olympia, London. Contact Anne Jackson on (0799) 26699.

Miltest 1988 (Military Testing Equipment) — April 26-28th
Olympia, London. Contact Network Events on (0280) 815 226.

Second Power Sources And Supplies Conference — April 26-28th
Olympia, London (at British Electronics Week). Contact Anne Jackson on (0799) 26699.

Electronics And The Stock Exchange — April 28th
IEE, London. Lecture by D C Marlborough. Contact IEE on 01-240 1871.

Electronics And The Space Program — May 4th
IEE, London. Lecture by J Egan. Contact IEE on 01-240 1871.

TITLE 88 (Technology In Tourism & Leisure Exhibition) — May 17-19th
Business Design Centre, London. Contact PLF Communications on (0733) 60535.

Rural Telecommunications — May 23-25th
IEE, London. International conference. Contact IEE on 01-240 1871.

Computer North — May 24-26th
G-Mex Exhibition Centre, Manchester. Contact Cahners Exhibitions on 01-891 5051.

Engineering Products And Technology North — May 25-26th
Exhibition and Conference Centre, Doncaster. Contact Trinity Exhibitions on (0895) 58431.

Special Effects Seminar — June 3-5th
Pinewood Studios. Contact British Kinematograph Sound and Television Society on 01-242 8400.

Information Technology And Office Systems Exhibition — June 7-10th
Barbican Exhibition Centre, London. Contact BED on (09328) 65525.

European Satelite Broadcasting — June 8-9th
Tara Hotel, London. Contact Online International on 01-868 4466.

Electronic Publishing 88 — June 14-16th
Wembley Conference & Exhibition Centre, London. Contact Online International on 01-868 4466.

Software Tools 88 — June 14-16th
Wembley Conference & Exhibition Centre, London. Contact Online International on 01-868 4466.

PACKING A PUNCH

Last month we received in the post a large polythene sack containing semishredded sheets of paper. An attached note from the Post Office apologised that 'an unfortunate accident' had occurred because of 'thin or unwieldy packaging.'

Disgorging the contents onto the ETI carpet we were amused to discover the ravaged sheets were advertising the Internepcon Show featuring The Electronic Packaging Centre!

Ah well, back to the parcel tape . . .

Next Month in ETI ELECTRONICS TODAY INTERNATIONAL

It takes nearly one hundred years to grow the trees from which ETI is made. While the Crystal Palace lay smouldering on the grassy slopes south of London, while the Metropolitan underground line first opened its doors to the fare dodgers and while Australia was celebrating its centenial, brave pioneering Canadians first planted the tiny larch saplings in the snow-capped Rockies.

Felled by teams of check-shirted lumberjacks the mighty logs are floated down the rushing, foaming, relatively pollution-free torrents of the Hudson to the coast to await shipment to the hungry pulp mills of Golden Square.

It takes more than 200,750 hours of sunshine and 2,628,000 gallons of water to feed the trees in their long life. 750 men work long hours for months on end to fell, ship and pulp the wood to make the June issue of ETI.

After all that work, it would be a shame to miss it.

The June 1988 issue of ETI includes the last part of the Virtuoso Power Amplifier project, the stand-alone Lucid Dream Stimulator, the ETI Universal Panel Meters (OK, so we promised that for this month but next month it's a cert) and a metal detector as the First Class beginners project. Plus, there's the first part of a feature and project on the much maligned analogue computer and a bumper bunch of test gear Tech Tips.

The June ETI — out May 6th

The articles listed are planned for the next issue but may not appear due to circumstances beyond even our control

READ\WRITE

SIMPLE WALSH

Prospective Walsh Synthesists (Music Circuit Potpourri, January 1988 ETI) who intend only to use Walsh functions for music or audio purposes rather than for, say, a bench function generator, may be relieved to know a much simpler circuit than the one published can be used.

Just as the Fourier series:

$$F(t) = \sum_{a=0}^{\infty} (A_a \sin(a\omega t)+B_a \cos(a\omega t))$$

can be reduced to:

$$F(t) = \sum_{a=1}^{n} |C_a| \sin(a\omega t)$$

for practical purposes, so may the Walsh functions be reduced. There are four stages of reduction of the Fourier series.

- The term where a=0 is a constant and makes no useful contribution to an audio signal.
- In practice it is only necessary (and possible) to use a finite series.
- Since the ear is not sensitive to phase, the sine and cosine terms can be collected together in one term with one coefficient, C.
- Lastly, −sin is only sin with a phase shift so only positive coefficients C are required.

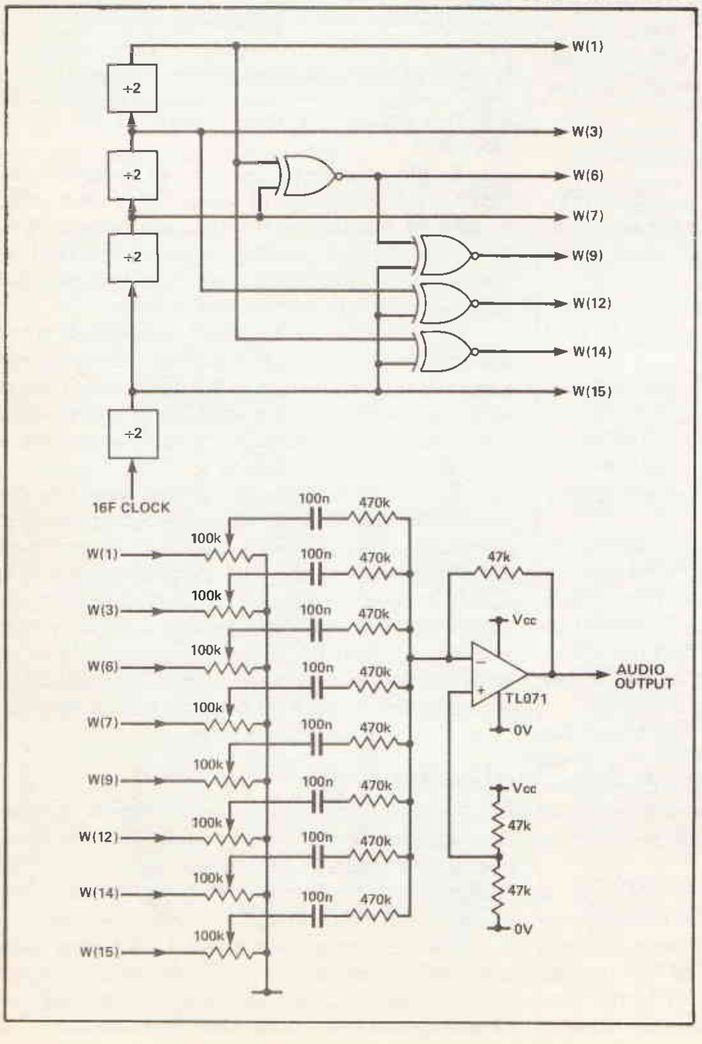
All these stages are equally applicable to Walsh functions, so W(0) can be dropped and as pairs of Walsh functions are just phase shifted versions of one another (W(1) and W(2), W(3) and W(4) etc), one of each pair can also be dropped. The final reduction means that all the switches, op-amps in the mixer circuit can be removed to leave the simple circuit shown below.

Thanks to Bruno Hewitt for some very interesting circuits.

N D Thalmann
Address unknown

Your reductions certainly simplify matters considerably. Perhaps other readers may now be tempted into giving Walsh synthesis a go.

We should also be pleased to answer other points raised in Mr Thalmann's letter if he would drop us a line with his address.



NOW WITH ADDED SPINE

I have to express my amazement that Hugh Young should criticise ETI for publishing hex dumps of EPROMs used in projects. (READ/WRITE January 1988). Heaven forbid we should castigate ETI for giving us too much information!

Personally I believe it is an act of absolute spinelessness to purchase a pre-programmed EPROM when you can have all the fun of programming one yourself.

An EPROM programmer has got to be one of the easiest projects to build, requiring only a couple of binary counters to clock through the address lines and a 21-25V pulse to write in the data (surely this is the only use for a home computer!).

By 1 o'clock in the morning when you have finally got all the code correct, the feeling of satisfaction has to be experienced to be believed.

Whatever happened to the spirit of amateur electronics?

H Bramley
Hove, East Sussex

Are all ETI readers masochists or is it just something in the air in Hove? We're all pretty spineless at ETI and so we'd advocate pre-programmed EPROMs but if your fingers need exercising, the hex dumps are there.

MORE SPOONS LESS SCREAMS

I believe a good many readers may be interested in some work I have recently completed which involved careful editing of the entire last series of *Doctor Who* to remove absolutely all traces of Bonnie Langford.

The plot remains intact and the legendary spoon-playing scene is now twice its original length.

It takes a lot of time but doesn't half impress your friends.

Steven Plait
Kidderminster, Worcestershire

BLUEPRINT

Starting soon in ETI will be a new column (at the back of the mag, nestling amongst the *Playback*, *Keynotes*, *Once Over* and so on) called *Blueprint*. The aim of the column is to design circuits to order, to help readers out of a tight spot.

Of course, we cannot design an entire hi-fi amplifier to your specification but if you require a peculiar form of a standard building block or a complete device to solve a novel problem, *Blueprint* can help.

So, if that niggling problem has been holding up your latest masterpiece, jot down the details — what it is you want the circuit to do, what you have already tried (if anything) — and send it to Blueprint, ETI, 1 Golden Square, London W1R 3AB.

JOHNNY COME LATELY

In your April 1987 issue you mentioned new designs by John Linsley Hood for a new Audio Design amp and a new lower power design to replace the 30W amp. These would be published in the 'fairly near future' and it was said that kits from Hart Electronics would be available.

It's now 1988 and still no sign of these new designs from JLH. What if anything is happening?

Michael Lowe
Loughton, Essex

Where does a year go? It has indeed taken rather longer than expected for the new JLH amps to see the light of day.

*We can only offer solace with the assurance that these amps **will** appear in ETI soon(-ish). The new Audio Design amp is designed and in the process of testing and final 'tweaking.' A kit is being put together by Hart. Watch this space.*

Have you noticed how young postmen are these days? Well here is your chance to even the score. You can prematurely age a postman of your choice with a vast stream of mail to the ETI office. Of course the best thing to send is packets of gold bars and we can assure you these will be received with not inconsiderable pleasure. However, if this is not possible, a close second best is to send us a letter for publication on this page (well, not this page but a very similar one due out in a month's time).

Set down your thoughts in clear precise prose of words of not more than three syllables (we're not too bright here at ETI) and send the resulting literary masterpieces to:

ETI
1 Golden Square
London W1R 3AB

CELL, CELL, CELL!

Vivian Capel charges us to take a closer look at batteries and rechargeable ones in particular

One of the effects of the proliferation of electronic devices is the enormous increase in the use of batteries. Once upon a time torches and valved radios were virtually the only applications. Now almost everything — watches to lap computers, calculators to CB radios, remote controls to portable televisions, and a host of other things (including of course torches and portable radios) require a constant diet of batteries.

The result is a bewildering range of types and sizes. For users of commercial equipment, the choice is mainly between zinc-carbon, alkaline or NiCds of the appropriate size.

Cost is a major consideration here. NiCds are about twelve times the cost of zinc-carbon cells so if your radio requires new batteries every six months, it would take six years to recoup the cost (by which time the NiCds may be worn out anyway!)

However, if your high-powered ghetto blaster seems to eat batteries, NiCds would certainly be worth considering. Alkaline batteries too offer cost savings over ordinary cells although dearer to buy, unless the current drain is very low.

For designers and constructors, the choice is much less easy. In this article we will take a look at the various types in general use and their features, with a more detailed consideration of the increasingly popular NiCd.

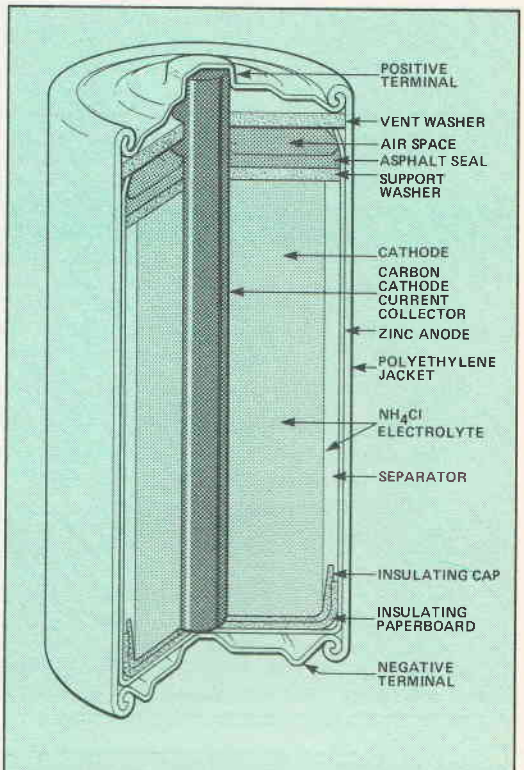


Fig. 1 The Zinc-carbon cell

Zinc-carbon

The basic, lowest cost cells are zinc-carbon (Fig. 1). These consist of a zinc case that serves as the negative terminal and a carbon rod which is the positive. The electrolyte is a paste of ammonium chloride. During discharge zinc is eroded from the inside of the case and hydrogen gas is formed around the carbon rod.

If discharge is heavy the hydrogen bubbles completely surround the rod thereby insulating it and blocking further action. This condition is termed *polarization* and the cell must be rested to allow the hydrogen to clear before it will deliver further current.

Manganese dioxide (which has a strong affinity for hydrogen) is introduced to minimise the effect and is known as a *depolarizer*. The oxygen in the chemical combines with the hydrogen to form water which thereby slightly thins the paste. The depolarizer takes a while to act, so the cell can still become polarized with a heavy discharge.

So zinc-carbon cells are not well suited for applications involving heavy discharges. Improved performance in this area is offered by the various high-power versions. These have modifications which include the use of more depolarizer which is especially pure and fast acting.

These cells are dearer but do not have a greater capacity. Their advantage lies in being able to sustain heavier currents for longer without polarizing. For example, a D-cell of normal construction will give 0.5A for about 18 minutes before polarising whereas a high-power version will run for up to three hours at the same discharge.

If the discharge is low or intermittent, there is no advantage in using high-power cells. Small cells, such as the AA type, are more likely to be subject to high currents in proportion to their size and capacity and so the standard cell has been superseded by the high-power variety.

It is worth noting that occasional small discharges will make a zinc-carbon cell last much longer that no discharge at all. This is the reason why doorbell batteries often last for years, while the same battery stored for a few months on a shop shelf would be useless.

Zinc-carbon cells are considered to be non-rechargeable and the manufacturers in particular point out that attempts to recharge could be dangerous – well they would wouldn't they! However, under special charging conditions, recharging has been successfully and repeatedly carried out with no ill effect. Charging from an ordinary battery charger or other DC supply is not recommended, not least because it is ineffective.

Alkaline Cells

Alkaline cells (Fig. 2) are made in the same sizes as the zinc-carbons. They use compressed manganese dioxide as the cathode instead of carbon which serves as its own depolarizer. The anode is again zinc and potassium hydroxide.

The cell has a lower internal resistance than the zinc-carbon and so will deliver a heavier current which it can sustain for longer periods before polarizing. It is also less affected by temperature extremes and has a longer shelf life.

The cost is around three times that of the zinc cell but with capacities about five times greater, so they are more economical as well as more convenient because battery changes are much less frequent.

With zinc-carbon cells, capacities differ according to discharge rate, being greatest for small intermittent currents and smallest for large sustained discharges. In the case of the alkaline cell, capacity differences between light and heavy discharges are much less, between 10-20%.

So unlike zinc-carbon cells capacities can be specified for average use. For standard cells these are:

C-cell 5,000mAH
AA cell 1,500mAH

Alkaline cell makers continue to improve their products to keep competitive with others and capacities of some 20% greater than the above average figures are now claimed.

Layer-type Batteries

When more than 6V is required, the standard round cell is somewhat inconvenient to assemble as well as being wasteful of space due to their cylindrical form. For this reason, the zinc-carbon batteries are made in a stacked rectangular configuration, the most common now being the PP9, PP6 and the PP3. Experience has shown that the maximum current before polarizing for these are:

PP9 65mA
PP6 25mA
PP3 10mA

There is an alkaline version of the PP3 which is very useful because it combines small size with reasonable capacity (about 300mAH). This is an excellent power source for small to medium current drains, having a greater capacity than the much larger zinc-carbon PP6.

For larger currents at 6V the lantern battery is very useful. The spring contacts can be partially unwound and block connectors fitted to the wire ends. It is one of the most cost-effective of the zinc-carbons and has an approximate capacity of 3,200mAH. Even so, this is less than the alkaline C-cell and much less than the alkaline D-cell.

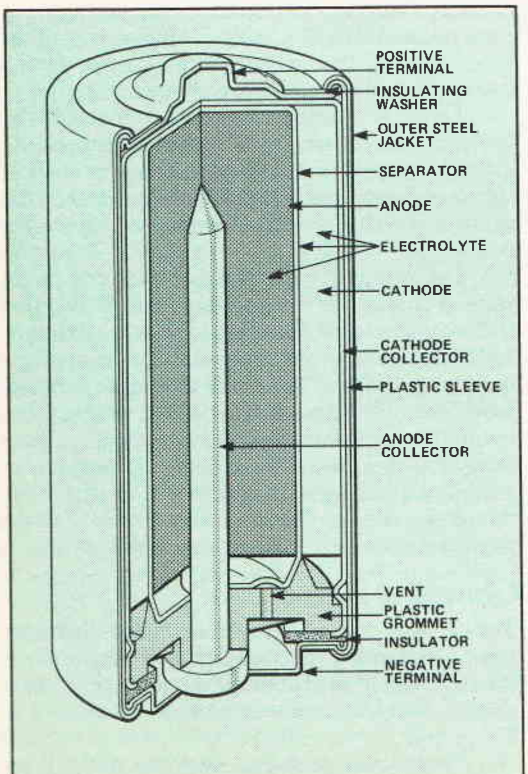


Fig. 2 The Alkaline-manganese cell

Lithium Cells

A more recent appearance on the scene, the lithium cell has a very long shelf life – in excess of six years – and a remarkable power/weight ratio which is typically 1248 watt-hours/kg. Nominal voltage is 2.95V per cell. An example is one cell which is slightly smaller than a C-cell which has a capacity of 1,000mAH, yet with a weight of only 20g.

Button Cells

The most common button cell is the mercury cell in which the negative electrode is zinc and the positive is compressed graphite and mercury oxide. The electrolyte is potassium hydroxide.

An unusual feature of this type of cell is that the voltage remains constant to the end of its life when it drops off suddenly. Off load, the voltage is 1.35V falling to 1.2V at the rated current. This is maintained until the sudden drop indicates the end of its life at below 1V.

The advantage is that there is no deterioration of performance of the device being powered during the life of the cell. The disadvantage is that the stage of the cell cannot be determined by its voltage and it can fail suddenly without warning.

Mercury cells are extensively used for watches, hearing aids, lapel microphones and any thing requiring small size with low current drain. Their low internal resistance and absence of polarization make them ideal for many applications including photographic equipment. They appear in a wide range of sizes and formats including an AA version with cell combinations to give up to 5.6V.

Button cells are also made in alkaline versions with about the same capacity for size but with a 1.5 terminal voltage. There are also rechargeable silver oxide cells.

Lead-acid

Now we come to the rechargeable or secondary cells of which the lead-acid type is the best known. All rechargeables can be charged and discharged (Fig. 4) many times though not indefinitely – after a specified number of charging cycles the cells lose their ability to hold a charge and progressively deteriorate.

The lead-acid cell consists of positive plates of lead peroxide interleaved with negative ones of spongy lead, immersed in an electrolyte of dilute sulphuric acid. They have high capacities and can deliver high currents for sustained periods – which is why they are used for car batteries.

The main snags are weight, size and danger of acid spillage. Another problem is that active material from the plates flakes off with age and eventually forms a conductive bridge across them at the bottom of the cell. With some models a sump is formed in the cell-case bottom which accommodates this debris and so delays the build-up but this reduces the capacity/volume ratio.

Acid spillage can be overcome by using jelly acid or porous separators that absorb most of the acid. In one type the plates and separators are

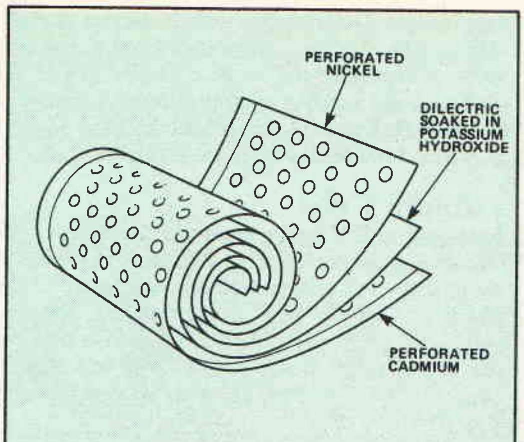


Fig. 3 The NiCd

compressed together in a block to obtain a high capacity/volume ratio and also retention of the active plate material. The disadvantage is that the power/volume ratio and power/weight ratio are impaired.

These have a zinc negative and silver oxide positive set of plates with potassium hydroxide for the electrolyte. This can be free or held in porous separators. Construction is similar to lead-acid types.

Power/volume and power/weight ratios are the highest of any secondary cell in general use. Silver-zinc cells are about a third the volume and weight of a comparable lead-acid battery. A feature is the nearly constant 1.5V over almost the whole of its discharge cycle. Furthermore, very high currents can be taken from the cell without damage. A cell can be discharged within a few minutes if required.

These cells can also be recharged at high rates very quickly, although care must be taken not to overcharge. However, as the voltage rises quickly to over 2V when fully charged, it is quite easy to arrange for a cutout on the charger.

Cost is one obvious disadvantage but another is the limited number of discharge cycles which can be expected. Up to 50 is specified for high discharges although up to 150 can be obtained with more moderate currents. This compares with some 500 cycles for lead-acid cells and up to 2,000 for NiCds.

NiCds

Believe it or not, the NiCd cell is over 86 years old. The first patent was taken out in 1901. However, practical cells took over 50 years to produce commercially.

Their construction (Fig. 3) is very similar to the electrolytic capacitor. A strip of perforated sintered nickel mesh and one of sintered cadmium are rolled up together separated with a dielectric strip impregnated with a solution of potassium hydroxide. The roll is inserted into a nickel-plated steel can with connections to the terminals and the can is sealed with a top plate having a vent to allow gas to escape under abnormal charging conditions.

This gives a big area of active material and permits large charging or discharging currents to flow. The C-cell will pass 4A and the D-cell 8A. The cylindrical cell construction is of similar size to the standard torch cells and allows NiCds to be used as chargeable replacements for them.

It should be noted though that the voltage is less (1.25V instead of 1.5V) which may affect device performance. NiCds are also made in rectangular batteries.

NiCds do not polarize or require rest periods to recover so they can support sustained currents – a valuable feature in some applications. Furthermore, the full current can be maintained until the cell is fully discharged.

Most cells deteriorate if kept inactive especially if stored in a discharged state. NiCds can be stored in any state of charge without deterioration although the charge itself will leak away slowly. However, charge retention is quite good and is dependent on temperature. At 20°C the loss of charge is about 10% of the full charge every 10 days, at higher temperatures the loss is greater – perhaps double (20%) per 10 days at 30°C.

Lower temperatures produce smaller losses. At freezing point 10% is lost after 30 days. So, at normal temperatures, some 70% of the charge is still available after a month and it takes 100 days to fully discharge.

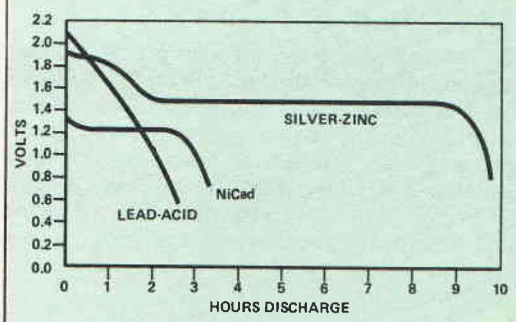


Fig. 4 Discharge characteristics of the three types of rechargeable cells of similar weight and discharge rate

NiCds will operate over a wide temperature range, from −22°F to 50°C, but the optimum is 20°C. Above and below this temperature the capacity decreases – 80% of maximum at freezing point and at 30°C, 70% at 35°C. Unlike most other types of cell, the performance is only slightly impaired at low temperatures.

Terminal voltage is also affected by temperature. There is a negative temperature coefficient of −4mV/°C, that is voltage is lower at high temperatures. The difference across the whole temperature range is about a third of a volt.

The actual voltage of a cell depends on its state of charge and the discharge rate, in addition to the temperature. On charge the voltage rises to 1.4V-1.5V. When fully charged the voltage drops quickly for the first 10% of the discharge to below 1.3V then it remains at 1.25V during light discharges, or 1.2V during heavier ones. For very heavy discharge rates the voltage may be as low as 1.1V. These voltages are sustained throughout the discharge until there is a rapid drop to 1.0V when the cell is considered effectively discharged.

Charging Rates

The capacity of a cell is governed by the discharge rate and is usually specified as that available when the cell is discharged at the 'five hour rate' – that is when a steady continuous current exhausts it in five hours.

Charge and discharge rates are denoted by the letter C which is the cell capacity combined with multipliers or sub-multipliers. The above discharge rate is described as C/5, while a rate of charge or discharge completed in one hour is C/1 and so on.

High rates of charge are given by the multipliers, twice capacity rate being 2C, four times 4C and upward.

A high rate means a fast time, the time being approximately but not exactly inversely proportional to the rate of charge. Table 1 lists the times required for fully charging typical sintered NiCd cells at different rates.

To use the D-cell as an example, the normal charge of this 4 ampere-hour cell at the 1 hour rate is 4 hours. At C/2 which is 2 amps, it is 2¼ hours. However, at 8A (2C) the required time is 27 minutes.

An important feature of NiCd charging is that overcharging is permissible only at low charging rates. The continuous charging sometimes employed for standby batteries in vital equipment can only be allowed at the C/8 rate or less. This rate takes 12 hours to complete from the fully discharged state and is the one normally recommended for maximum capacity and cell life.

Notice from the table that the maximum permissible overcharge decreases as the charging rate increases. At fast rates of 4C and higher there is no margin at all and the time to fully charge the cell is also the maximum. Charging must therefore be carefully timed and the cell must be fully discharged at the start otherwise it will be overcharged.

The absolute maximum charging rate is 10C for which the timing is very critical. When charging at these rates gas will escape from the vents so adequate ventilation must be allowed. In the case of D-cell, 10C charging would be at the rate of 40A. Maximum charging rate for AAA type cells and similar size is 2C.

Going in the other direction, the minimum charge for sintered cells is C/40, taking 70 hours. Below this there would be no charging effect.

Some small cells such as NiCd button cells and PCB types for direct mounting on circuit boards are of a different construction to the sintered type. They are termed *mass-plate cells* and cannot be subject to the high charging rates possible with the sintered variety.

For continuous charge, the rate should be C/100 and the maximum rate C/10. This rate takes 14 hours to fully charge but there is a wide overcharge tolerance of up to 300% – up to a permissible 42 hours.

Chargers

The low internal resistance of a NiCd cell means it is unwise to use an ordinary constant voltage charger. The current varies according to the voltage of the cell and so the calculation of precise charging time is difficult if not impossible because the voltage changes as the charge proceeds.

A fully discharged cell takes a high current initially. The use of an ordinary charging circuit is possible at low charging rates at which there is a large overcharge tolerance, and in particular for indefinite charge arrangements in back-up circuits.

For normal charging and particularly fast charging, a constant current charging circuit must be employed. With this the current is fixed throughout the charging cycle.

A phenomenon which is to be found with some NiCds is the so-called memory effect. If a cell has been only partly discharged before it is recharged, especially at the higher rates, it loses some of its capacity permanently. It is as though the cell remembers its level of discharge and this sets the capacity level for all subsequent charges. The effect is thought to be due to crystals forming in the active material.

Some makers claim their cells do not suffer from memory effect but in the absence of such an assurance it is prudent to fully discharge all cells before attempting a recharge.

By fully discharge I mean down to the normal 1.0V level at which the cell is deemed to be exhausted, not down to zero volts. However, there is no need to be too fussy about the exact voltage. The easiest way is to leave the equipment that it powers switched on until it is evident by the performance that the cells are well discharged.

There is a danger in discharging a battery of several cells. If discharged below the 1.0V point, the voltage drop can be rapid to zero. Now this does not harm the cell in itself but where several cells in series are taken down to this level, one may drop to zero before the others. They will continue to discharge through the load and will proceed to charge the fully exhausted cell in the opposite direction because the current flowing through it is of opposite polarity to that if its terminals. This reverse charge will damage it.

Cell type	Voltage	Capacity (mAH)	Max current A	Charging cycles	Energy/ weight ratio (WH/ Kg)	Energy/ volume ratio (WH/ litre)
Zinc-carbon D	1.5	2,000	0.5		35	48
Alkaline						
D cell	1.5	10,000			115	242
C cell	1.5	5,000			115	185
AA cell	1.5	1,500			88	100
PP3	9	300			53	120
Lithium	2.95	1,000			148	98
Mercury oxide Button cell	1.35	35-1,000				88-175
Lead-acid jelly	2.0	1-110AH	80-700	500	30-36	75-84
porous separator	2.0	4-90AH	20-200	500	22-35	42-70
Silver-zinc	1.5	1-10AH	40-400		40-70	65-125
NiCd						
D cell	1.2	4,000	8	2,000	29	77
C cell	1.2	2,000	4	2,000	30	60
AA cell	1.2	500	1	2,000	24	27
PP3	8.4	110	0.5	2,000	24	44
PP9	8.4	1,200	1.6	2,000	23	36

Table 1. Chart of cell characteristics

So for absolute safety, cells should be discharged individually if there is any chance of the discharge going below 1.0V. Otherwise discharge only to the 1.0V level.

A discharger can easily be made from one of the multiple cell holders used to series connect several cells. A 5R0 wire-wound resistor should be wired across each compartment. This will discharge cells at the rate of 200mA in a few hours depending on the amount of charge left in the cells. For C and D-cells a 2R0 resistor would give a faster discharge of around 500mA.

Some authorities say the discharge should be higher than normal to disperse any crystals that might have formed. So a value down to 1R0 could be used for the larger cells.

ETI

CAPACITY FOR THOUGHT

John Linsley Hood looks at audio circuits and tells you where to put your capacitors

CAPACITORS

Last month I looked at the construction of different types of capacitors and the materials that are used in their manufacture. Now that you've absorbed all that (haven't you..?) we can get to grips with their applications in audio circuits.

Circuit Applications

It is practicable to design audio amplifiers without very many capacitors at all and most IC op-amps only have one, used to stabilise the circuit at high frequencies by reducing its HF gain.

In audio circuitry, capacitors will be used as DC blocking elements such as C1 in Fig. 1 to prevent inadvertent DC offsets that occur in early stages of the system from being amplified along with the wanted AC signal and ending up as a very big DC offset at the speaker output terminals.

A similar function is performed by the series capacitor in a negative feedback circuit (C2 in Fig. 1) where 'A' is some kind of gain block (an op-amp or equivalent). The gain of this stage at some frequency where the impedance of C2 is low enough to be neglected is (R2+R3)/R2. However at DC, where the capacitor (if it is a perfect component) is an open circuit, the gain reduces to unity so any DC offset between the '±in' points of the amplifier will not be made worse by the AC stage gain. The corollary to this is of course that the gain of the stage will decrease as the operating frequency decreases and the impedance of the capacitor increases, so it must be big enough.

A further important function is in the decoupling of the supply lines to the amplifier (C3 and and C4 in Fig. 2).

Most amplifier circuitry is designed in the expectation that the ± DC supplies to it will be stable and free of ripple, unwanted signal components or general noise and rubbish. The performance of the amplifier may be impaired — especially in relation to its stability margins, which are very important — if any output signal can find its way back into the signal circuit by way of the supply lines. The easiest way to secure clean smooth supply voltages is in theory to decouple them to a good neutral '0V' line by way of a very low impedance capacitor.

The final circuit positions where capacitors are needed is in time-constant generation circuitry, in tone controls, frequency response shaping circuitry (such as RIAA), LF and HF filters, and HF loop stabilisation functions. Fortunately, in most of these positions the actual capacitance values required are fairly small, so problems of cost or physical bulk are usually minor ones.

Now let us look at these applications and see what characteristics are particularly required.

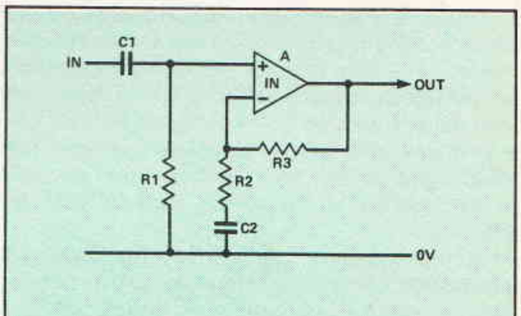


Fig. 1 Capacitors in audio amplification

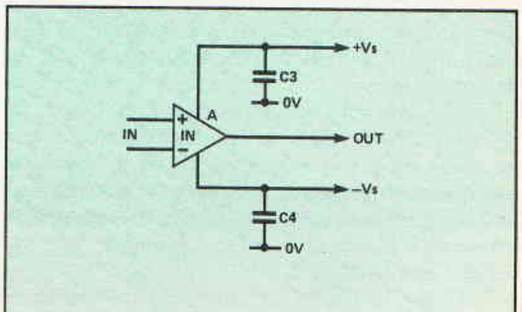


Fig. 2 Capacitors as supply decouplers

DC Blocking

Looking at the circuit in Fig. 1, the important needs are that the impedance of C1 at any valuable part of the audio signal bandwidth should be sufficiently low (in comparison with R1 and the input impedance of the gain block 'A') that the input signal is not attenuated significantly.

For the blocking function to be adequately performed, the leakage resistance of the capacitor must also be very high. Fortunately with modern film dielectric capacitors this can usually be taken for granted.

This might not be true in the case of electrolytics especially if the polarity is inadvertently reversed through careless installation or incorrect interpretation of circuit operating potentials.

Generally, in circuitry with hi-fi pretentions it is well to avoid electrolytics in this position and if necessary rearrange the circuitry so that large capacitance values are unnecessary.

The impedance presented by the other parasitic elements (inductance and series resistance) is unlikely to be significant, certainly in audio use, in comparison with the combined input impedance of R1 and the gain block.

It could also be argued that for hi-fi circuitry the effective capacitance value of C1 should remain constant (especially as a function of the voltage applied across it) so that it does not introduce subtle waveform distortion effects.

Once again, plastic film dielectric capacitors (the so-called 'non-polar' types) are unlikely to suffer from this defect at typical small signal voltage levels to an extent which is detectable. It might though be a problem with electrolytics.

Feedback Path Capacitors

The other DC blocking function is typified by C2 in Fig. 1. Here the problems are greater since circuit constraints are likely to force the use of a relatively low value for R2, and the LF roll-off frequency (the '-3dB' point) occurs where the impedance of C2 ($1/2\pi fC$) is equal in value to R2.

In the past, C2 would have almost always have been an electrolytic type, aluminium or tantalum, but in current practice it is likely that a non-polar component would be employed to avoid any possible 'dulling' of the sound. The values of R3 and R2 would be increased as much as other circuit demands allowed.

The same needs exist here as in the input DC blocking capacitor, but are all greatly magnified because the circuit impedance is usually so much lower so that small changes in series impedance or capacitance value are likely to be much more important.

Supply Line Decoupling

Here the overall need is for the effective impedance to be as low as possible and to remain low over the whole of the frequency spectrum. The preservation of a low decoupling impedance well beyond the limits of the audio range is important for loop stability reasons. Improvements in the purity of the supply lines are usually apparent in the sound quality.

Electrolytic capacitors are usual for this and have a relatively high series impedance by comparison with a non-polar type of the same value. Modern practice is to quote the 'equivalent series resistance' (ESR) of electrolytics in the manufacturer's specification (usually for power supply reservoir capacitor applications).

A low ESR component is usually a good choice if only because it implies that the manufacturers have tried to lessen the inevitable series resistive components by greater care in design or construction. At HF the problem need not be serious, since the main capacitor can always be bypassed by a smaller non-polar type and that if necessary bypassed yet again by a smaller one still.

The reason for this piggy-back activity is that the method of construction of large value bipolar units is likely to lead to higher values of inductance and winding resistances. Indeed for RF bypass use (as in the HF stages of FM tuners) small value disc ceramic capacitors are obligatory because of their very low self-inductance. No wound component would ever be adequate here. Unfortunately disc ceramic devices are usually only available at low working voltages, say 25-30V, a bit low for audio circuitry. Stacked film bipolar types are a good equivalent for audio circuit use.

At the very low frequency end of the passband no capacitor of any sensible size is ever likely to be entirely adequate, and here an electronically stabilised power supply is by far the best answer, especially since if it does its job effectively it will provide an absolute barrier between the operational circuitry and everything on the power supply side of the hardware. This frees the user from worries about whether he ought to replace his mains cable with quarter inch copper bars, or his mains transformer with a filing cabinet sized substitute.

Time Constant Components

Here the overriding need is for accuracy in value and for reasonably low levels of stray inductance, since this could have some effect on the characteristics of filters or feedback circuits. However, spurious inductance effects can normally be ignored for modern components used in sensibly designed AF circuitry, and the effects of stray series winding or loss resistances are likely to be swamped by the general circuit impedances.

Choice In Circuit Applications

In general and bearing in mind the manufacturing details discussed last month, my own order of preference in the capacitor world is polystyrene, polycarbonate, polypropylene and polyester. And I prefer film/foil to metallised foil.

The most critical application, in my opinion, is as the DC blocking capacitor in an NFB loop, though other DC blocking usages must be scrutinised.

Supply line bypass duty requires other qualities and a good quality electrolytic of adequate size and rating bypassed by one or more polyester capacitors of descending values will be quite adequate.

In HF stabilising or time constant duty, polystyrene is the first choice if available in adequate capacitance values. Otherwise use any close tolerance non-polar types.

Above all remember that no single type should always be first choice. It is a matter of 'horses for courses.'

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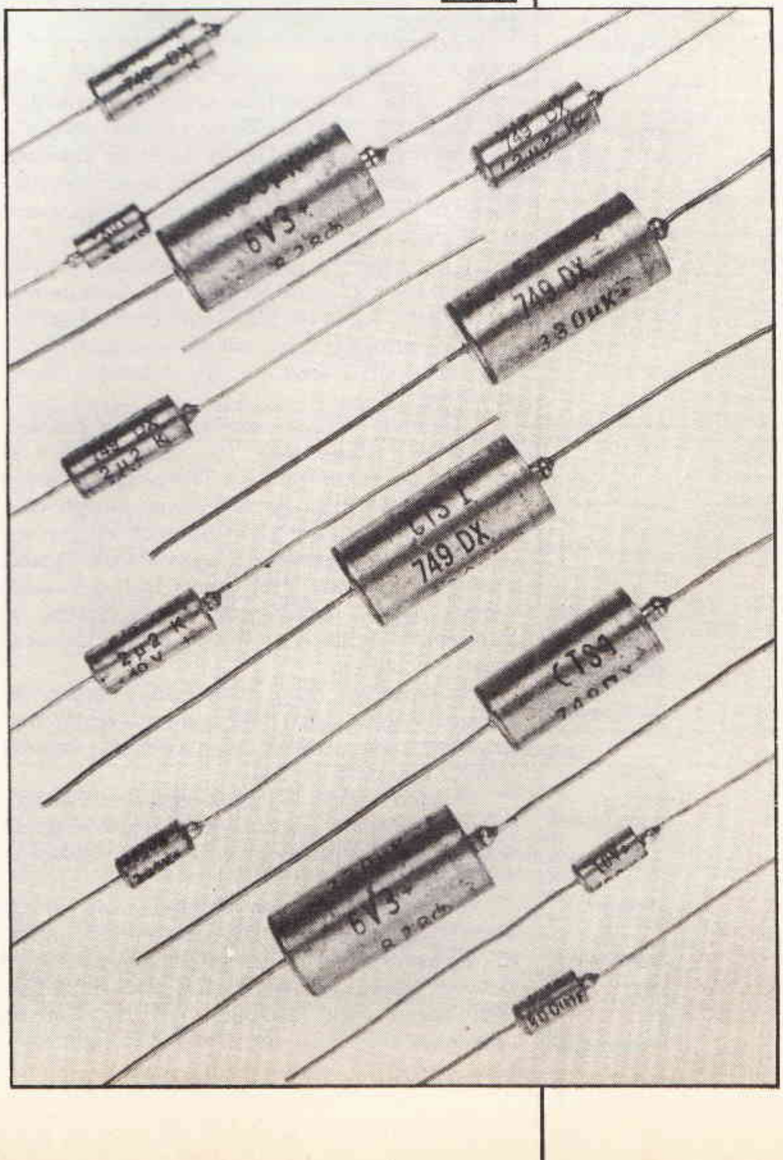


TRANSIENT CAPTURE

Mike Barwise examines the set-up of the ADC301 and ADC302 to achieve rapid data logging

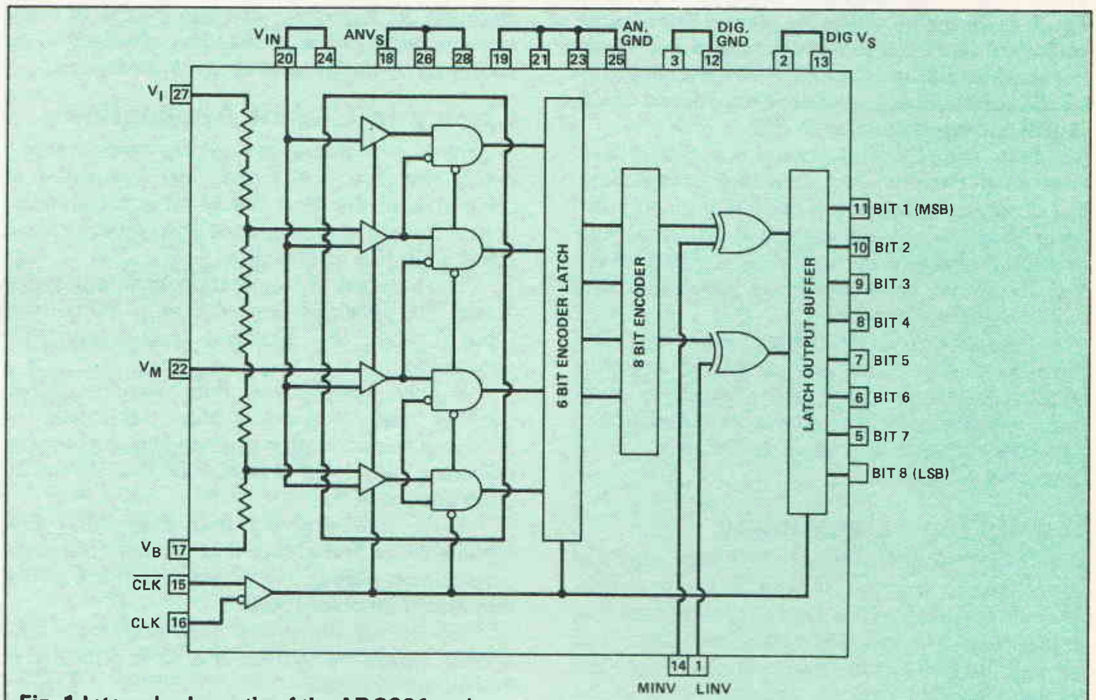


Fig. 1 Internal schematic of the ADC301 and ADC302.

Many designs for analogue data loggers have appeared in print (not least in ETI) over the last couple of years. This is definitely a growth area as more and more everyday monitoring and control jobs are automated, creating the need for precise signal analysis.

The majority of monitoring tasks are relatively low-speed and long-term — environmental monitoring, for example, requires data points generally no closer than a minute or so apart due to the inherent inertia of the systems being monitored.

There is however another class of problem altogether, where very fast data capture is required over short periods. This is often referred to as *transient capture* and comes into its own when events of very short duration and/or unexpected occurrence are being examined. Typical examples are body shell impact testing in automotive design, catastrophic failure testing in general mechanics and electrochemical experimentation.

In these and many other fields (increasingly frequently these days) data capture is required at sampling rates ranging from 0.1MHz through 20MHz and even beyond.

There is a general misapprehension that submicrosecond analogue conversion and storage are somehow almost impossible to achieve except at enormous expense.

It is true that for high resolution work (12 bits and above) there are some special considerations at very high speeds — there is generally a trade-off between speed and precision. It is also true that high speed high resolution systems can be appallingly expensive, even if you build them yourself — a 1MHz 12bit ADC can cost as much as £500 per chip.

Nevertheless it is perfectly possible and quite cheap to produce fast 8-bit analogue capture equipment. I intend to prove this by introducing the DATEL ADC-301 and ADC-302 analogue to digital converters. These are so-called flash (or parallel) 8-bit converters with maximum conversion rates of 30MHz and 50MHz respectively.

The very high speed of these devices necessitates their implementation in ECL (Emitter Coupled Logic) technology but as the conversion rates are well within the bandwidth of Fast series TTL, it is possible to interpose ECL/TTL interfaces to allow their use in the more familiar TTL logic environment. This is also beneficial due to the considerable cost and power dissipation of ECL memory compared with that of fast CMOS or NMOS devices.

The Datel Devices

Let us first look at the ADC chips themselves. Figure 1 is an internal schematic of both devices. Note that only a few of the 256 comparators are shown. One input of each comparator is connected to the signal input, and the other to the relevant point on a resistor chain fed by a reference voltage.

The outputs from adjacent comparators are ANDed together and fed to a latched 6-bit encoder which in turn feeds a latched 8-bit encoder. This means that there is a data delay of one clock cycle, data point 1 emerging at the chip output on completion of conversion 2 and so on.

Figure 2 gives a recommended circuit *which should not be departed from*. There is no room

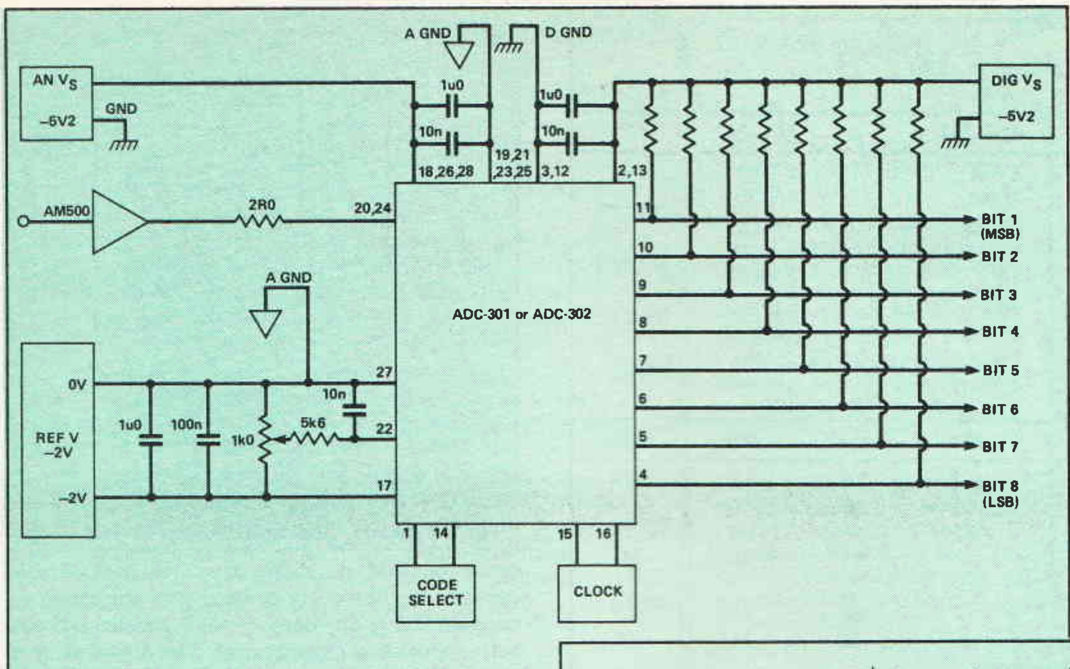


Fig. 2 Recommended connection diagram.

here for unorthodox approaches. Remember that in ECL, power supply polarity is reversed so rails are GND and -5.2V (the extra 0.2 matters! Use an adjustable regulator and *get it right*) and logic levels are *high* (logic 1) = -0.9V to gnd, *low* (logic 0) = -1.75V nominal.

All outputs are shown pulled down — this is to reduce signal reflections in the output bus. The two power supplies (analogue V_s and digital V_s) must be independent. The ideal method is to use two separate regulators.

Four items in Fig. 2 have been generalised — *code select, clock,* the *reference* and the *obligatory input amplifier*. Let us deal with each of these in turn.

Code Select allows the data format to be modified. As seen from Fig. 2, pins 1 and 14 (LINV and MINV) control exclusive OR gates as programmable inverters in the output path. MINV (controls the MSB bit 1) and LINV controls the other seven bits. It is thus possible to output true, inverted or two's-complemented data. The code select pins are either left open (logic 0) or pulled to ground via 3k9 resistors (logic 1).

It is worth pointing out here that the dynamic range of these ADC chips is 0V to -2V. Table 1 gives the various programming options and their resultant output codes.

Next, let us look at the *clock* input. The clock is a typical ECL two pin differential clock signal. The chip timing diagram (Fig. 3) shows us this. The critical timing constraints amount effectively to no more than *minimum half cycle periods*. The clock need not be 50/50 mark/space ratio. For the 30MHz part T1 must be not less than 25ns, and T2, 8ns. For the 50MHz part, T1 and T2 are minimum 15ns and 5ns respectively. Study the timing diagram carefully and you will be able to follow this. T1 is the *comparator settling time*, and T2 is the digital encode/latch time.

Driving the clock is no problem in ECL as line drivers with differential outputs are always used to distribute clock signals. We are going to cheat, however, but more of that later. Now let us look at the requirements for the *reference*.

Apart from the negative polarity, there is nothing odd about this reference. It can be just

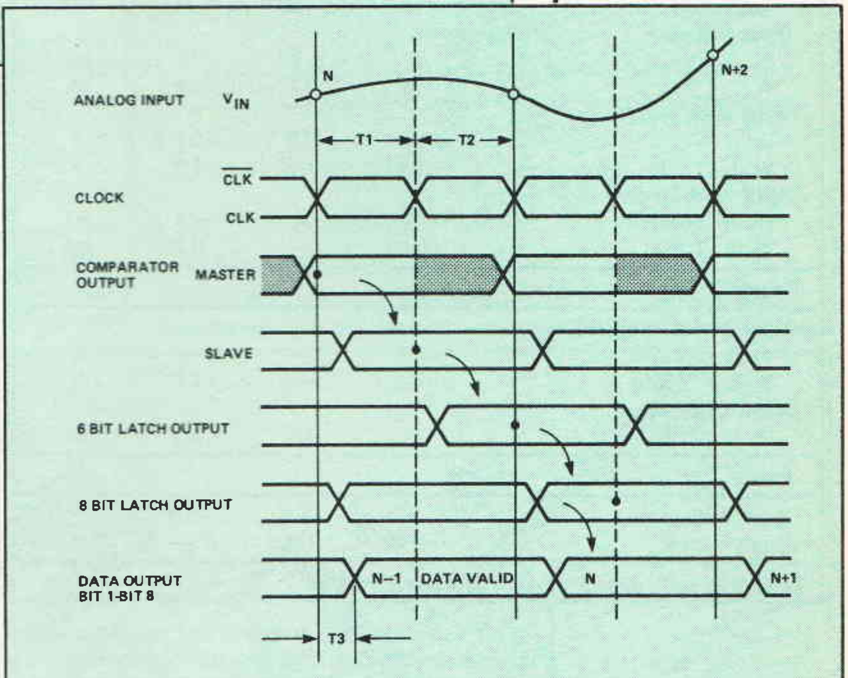


Fig. 3 Timing diagram for ADC301 and ADC302.

MINV LINV	0 0	0 1	1 0	1 1
0.0000V	1111 1111	1000 0000	0111 1111	0000 0000
-0.0078V	1111 1110	1000 0001	0111 1110	0000 0001
-0.9961V	1000 0000	1111 1111	0000 0000	0111 1111
-1.0039V	0111 1111	0000 0000	1111 1111	1000 0000
-1.9922V	0000 0001	0111 1110	1000 0001	1111 1110
-2.0000V	0000 0000	0111 1111	1000 0000	1111 1111

Table 1 Digital output codes for ADC301 and ADC302

about anything. Eight bit precision can be achieved using a conventional three-terminal regulator as a reference with care, or alternatively one of the various precision reference diodes can be used. In this case, the regulator has a distinct advantage. The reference current is quite high and the regulator can supply this current directly, whereas a reference diode has a very low output current so a buffer amplifier would have to be interposed between it and the ADC.

Functional Specifications
Typical at +25°C, V_s = –5.2V DC, V_B = –2.0V unless otherwise stated

Performance	ADC-301	ADC-302
Resolution	8 Bits	8 Bits
Conversion Rate (Min)	30MHz	50MHz
Non-Linearity (Max)	+½LSB	+½LSB
Diff Non-Linearity (Max)	+½LSB	+½LSB
Diff Gain (Max)	1.5%	1.5%
Diff Phase (Max)	0.5°	0.5°
Aperture Jitter (Typ)	45 ps	30 ps
Input Bandwidth (Typ)	15MHz	25MHz
Power Dissipation (Typ)	420mW	550mW

Inputs	Min	Typ	Max	Units
Reference Input Voltage	–2.2	–2.0	–1.8	V
Reference Resistance	70	80	100	Ohms
Analog Input Voltage	–2.2	—	0.1	V
Analog Input Capacitance	—	35	40	pF
Analog Input Bias Current				
(ADC-301)	—	60	90	µA
(ADC-302)	—	75	115	µA
Offset Voltage				
V_t	7	9	11	mV
V_b	15	17	19	mV
Digital Input Voltage				
V_h	–1.0	–0.9	–0.7	V
V_l	–1.9	–1.75	–1.6	V
Digital Input Current				
(V_h = –0.9V)	0	—	0.4	mA
(V_l = –1.75V)	–0.05	—	0.35	mA
Outputs				
Digital Output Voltage				
V_h (R_L = 620R)	–1.0	—	—	V
V_l (R_L = 620R)	—	—	–1.6	V
Output Data Delay				
(R_L = 620R)	—	4.0	5.0	ns
Power				
Supply Voltage, V_s	–5.7	–5.2	–5.0	V
Supply Current	–100	–75	—	mA

Table 2 Specifications for ADC301 and ADC302

This is relatively complex and can introduce thermal drifts which might decalibrate the system.

As to actual values, Table 2 gives the operating conditions and specifications of these chips. The –2V reference is fed into a resistance of 70R to 100R. For latitude let us say 50R.

So, we must be able to supply 40mA without the reference noticing.

A suitable device is the LM337 adjustable negative regulator. This comes in a TO-220 power transistor package with an output current of 1.5A. Line rejection (the ability to ignore input changes) is quoted at 0.07%/volt change in and thermal drift is quoted as worst case 0.04%/W and 0.6% over junction temperature range (0-125°C).

Considering that we are looking at 1 part in 256 or about 0.4% precision, we could finish up with an error of 1 LSB (least significant bit) if we calibrated the unit at a junction temperature of 0°C and then let it rise to 125°C. In the real world (18°C to about 100°C) there should never be more than ½ LSB error due to using this regulator as a reference.

The last of the less-than-obvious is the *input* amplifier. Why do we need one?

Although the comparator inputs have an inherently high DC resistance (probably in the

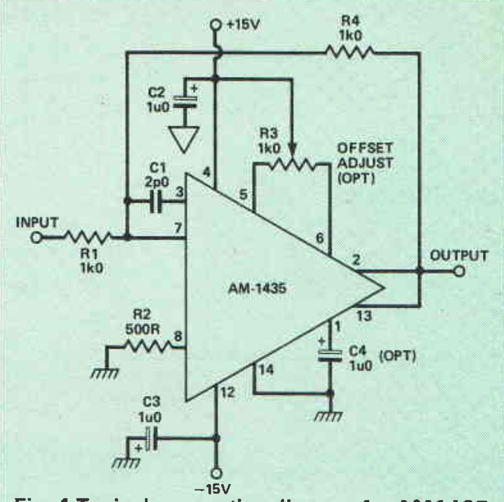


Fig. 4 Typical connection diagram for AM1435.

order of 10M or more) there is considerable capacitance at the signal input (not surprising — connect 256 of any component in parallel and you get a lot of stray capacitance). The actual value is 35-40p. Not a lot, you might think, but when you consider that the voltage across this capacitance has to be stabilised within half of T1 (Fig. 3) it becomes obvious that some pretty hefty currents are going to flow briefly.

So, to avoid dragging the input signal around, a buffer amplifier is required. This amplifier should have two important characteristics in addition to its ability to drive a load with high transient current demand. These are:

- a resistance to instability when driving capacitative loads;
- a high *slew rate.* Slew rate is a nominal parameter describing how quickly the amplifier responds to a change in input. The most common test is to apply a very fast (in this case 1-2ns) transition between nominal 0V and nominal maximum output swing to a unity gain configured specimen, and to measure how long it takes for the output to arrive at the same voltage, normally expressed in V/µs.

To take full advantage of the speed of these ADC chips, the amp must have a slew rate calculated as follows:

The maximum legal swing at the ADC is 0V to –2V, in other words normalised 2V. Assuming the faster component T1 is 15ns, the comparator input must be stable by halfway through T1, so we have a signal slew time of say 7ns. We must be able to slew 2V in 7ns, so the slew rate we need is 1000/7 × 2, or approx 285V/µs.

This would allow us (just!) to log a square wave with a frequency of half our maximum sampling rate. In practice, because of the Nyquist Limit (which imposes the condition that the sampling rate must be twice the frequency of the highest harmonic present) we can only log a sinusoid (no higher harmonics present) at the maximum sampling rate anyway, so this slew rate requirement can be relaxed to some extent.

I would not like to go much below 200-220V/µs though, unless the incoming signal is expected to be exceptionally free of transients and fast transitions. A suitable amplifier is the DATEL AM-1435 (Fig. 4), which has a slew rate of about 300V/µs.

Next month I will show you the principles of a couple of complete transient capture units using these chips.

ETI

PROJECT

BICYCLE SPEEDOMETER

Leycester Whewell not only knows where he's going but how fast he's getting there too

This article in fact describes my Mark II cycle speedometer. Since Mark I was built (in 1982) new semiconductor chips have enabled projects such as this to be built from fewer and more compact components and yet provide a greater number of features than originally possible.

As well as being suitable for a bicycle, this speedometer could also be adapted for other tasks of a similar nature.

The main aim of the design is to produce a unit low on power, simple to maintain and operate, reliable and capable of giving as much useful information as possible. I also wanted the Mark II version to behave more like a mechanical odometer in that it would not have to be turned on or off every time it was used and that the information would be preserved indefinitely without worrying too much about battery life.

Finally, since only a few units were to be built, the components had to be cheap and easy to use — no mass production here to bring down costs.

Mode	Display	Function
Set up Mode 0	—1—	X=0 for Imperial, 1 for metric units
Set up Mode 1	—2— XX. XX	Wheel size, from 18.00in to 28.00in
Mode 0	XXXXXX. XX	Total Distance (miles/km)
Mode 1	XXXXXX. XX	Trip Distance (miles/km)
Mode 2	XXXX.XX. XX	Total Time (HHHH.MM.SS)
Mode 3	XXXX.XX. XX	Trip Time (HHHH.MM.SS)
Mode 4	XXX. X	Current Speed (mph)/kmh)
Mode 5	XXX. XX	Top Speed (mph/kmh)
Mode 6	XXX. XX	Average Speed (mph/kmh)
Mode 7	XXX. 0	Time Trial Distance (miles/km)

Table 1 Display modes

Choosing Chips

Several families of CMOS microprocessors have become readily available since building the Mark I (which used the 1802). These include the 80C35 and 80C85 series, the HD6303 and HD6305 series and the 146805 series.

Apart from the HD6303 which has an awkward 0.07in pin pitch, each series has a suitable member for making a speedometer. The 146805 was chosen since I already had an assembler for it and knew several sources from which it was readily available.

The four digit LCD on the Mark I was a limitation when it came to displaying elapsed time. To fit in a decade of hours, the seconds count had to be reduced to tenths of a minute. After numerous hours riding, a mental conversion back to seconds had to be done before the reading became meaningful.

The advent of triplexed LCDs and their respective driver chips has enabled more digits to be fitted into a display without an absurd number of connections. An eight digit LCD has been incorporated into this speedo with an ICM7231BFIPL driver.

Elapsed time can now be shown in seconds, minutes and four decades of hours. Distances need no longer wrap around to zero after 999.9 miles. The other main advantage of the triplexed LCD used is the annunciator arrow — there is one beneath each digit and these are used to indicate the operation mode.

A useful feature of most single chip or related low chip count systems is the standby mode. The 146805 has two, called WAIT and STOP. In the WAIT state the crystal oscillator and timer operate but when the timer counts down to zero or there is an external interrupt then normal processing is restarted.

The speedometer enters the WAIT state between regular timing intervals and the external interrupt caused by one revolution of the wheel. During this period the current consumed is about 1.5mA compared to 7-8mA during normal processing.

The relative proportions of time spent processing and WAITing determine the overall power consumed by the speedometer. A fixed proportion of time is spent servicing the time interrupts but the amount spent on wheel interrupts is directly proportional to speed. So whilst stationary about a 2mA is consumed and this rises to 2.5-3mA at 20mph.

The STOP state consumes less current than the WAIT state, because the crystal oscillator and timer also stop. If after a period of about a minute there is no interrupt due to the rotation of the wheel then the speedometer will clear the display and enter the STOP mode. To the user this gives the impression of it having turned itself off.

An interrupt from the wheel ends the STOP state and the speedometer updates the display and continues as before. This obviates the need for an on/off switch and allows data to be preserved from one period of use to another. About 0.5mA is consumed during the STOP state, so a set of four NiCds with a capacity of 450mAh will last 28 days if the speedometer is used for two hours a day. Changing the batteries every two to three weeks will allow a safe margin for leakage and variations in cell capacity due to ageing.

To preserve data in the processor when changing batteries, a lithium data retention battery and a diode prevent the supply voltage from dropping below about 2.5V. The batteries should only be changed when the speedometer is in the STOP state, this prevents excessive use of the lithium battery and (worse) running the processor from a supply voltage that is too low for the crystal frequency used. If this happens and the processor crashes then all data contained within it will be lost.

The Hall effect switch used to detect rotation of the wheel in Mark I worked perfectly in all conditions. However, as it consumed a relatively massive 3mA, an alternative had to be found which would not drain a set of batteries in a few days. The only form of detector that does not require a steady current source involved direct contact switching. A reed relay mounted so its axis was parallel to that of a bar magnet mounted on the wheel and perpendicular to the adjacent spokes was found to be suitable.

Debouncing of the contacts is performed in software, the current consumption is reduced to grounding a pull-up resistor when closed and only two wires are needed from the speedometer.

Initial operation of the relay proved to be problematic, each wheel revolution caused the relay to close three times in quick succession. I found that the relay was passing too close to the magnet and induction through the relay contacts was responsible. Increasing the minimum separation between them to over 5mm for that particular magnet cured the problem.

Operating Modes

Ten modes of operation are available. Eight are for normal use with two special ones for parameter setting. Special mode 1 is entered after the power-on reset which occurs when the batteries are inserted for the first time only. This mode is used to set the units used — imperial units are represented by a 0 and metric units by a 1. Changing from one to the other is done by pressing the reset switch. A third option, number 2, has been reserved for metric units with speed in metres/second although the additional program to do this is not written.

Pressing the mode switch selects special mode 2 which selects the wheel size to be used. Eight of the most common wheel sizes are displayed in turn by pressing the reset switch and range from 18in to 28in with 700mm being displayed as 27.56in. Pressing the mode switch again then selects the first of the normal modes.

Each of the normal modes is associated with one of the annunciator arrows under each digit of the display. When the modes are changed, as listed in Table 1, the arrow moves one digit to its right and back to the digit on the far left when the Total Distance mode is re-entered. If both switches are pressed together for over a second then the special modes are re-entered for a change in units or wheel size.

HOW IT WORKS

There is not a lot to be said about this circuit that isn't already said in the main text. The full circuit diagram of the speedometer is shown in Fig. 1.

The microprocessor (IC1) contains its own clock oscillator, requiring only the external components, X1, R6, C3, 4. The two 8-bit ports of the chip's built-in PIA are used to directly interface the LCD driver chip (IC2), the two control keys (SW1, 2) and the reed relay sensor. The latter also acts on the processor interrupt input.

The EPROM (IC3) containing the speedometer program is the only external device occupying the memory space of the processor and is directly mapped using IC5c and IC4.

Power is provided by either the NiCd batteries B1 with protection diode D1 or through the standby data-retention cell B2. Power on reset is provided by R1, C1.

As their names suggest, the Total Distance and Time modes keep a record of the total usage of the speedometer. They cannot be cleared using the reset switch. Neither mode will wrap around to zero in a hurry — it takes a million miles/km or 10,000 hours to do so!

The Current Speed mode does just that, displaying with a resolution of 0.1mph/kmh and the Top Speed mode displays with a resolution of 0.01 mph/kmh. Measuring to 0.01 mph/kmh is meaningless as far as absolute readings are concerned because of the error in the diameter of the wheel but it is useful when a comparison is made to a previous effort. Top but not Current Speed may be reset.

The remaining four modes are linked by the need for a common measurement origin. Trip Distance and Time display data in the same format as their Total Distance/Time counterparts and Average Speed is simply their ratio. Average Speed uses a time base of 3.6sec (0.001hr), distance in units of 0.01 miles/km and produces a result in 0.01mph/kmh. Its accuracy increases with both distance and time, so after about an hour

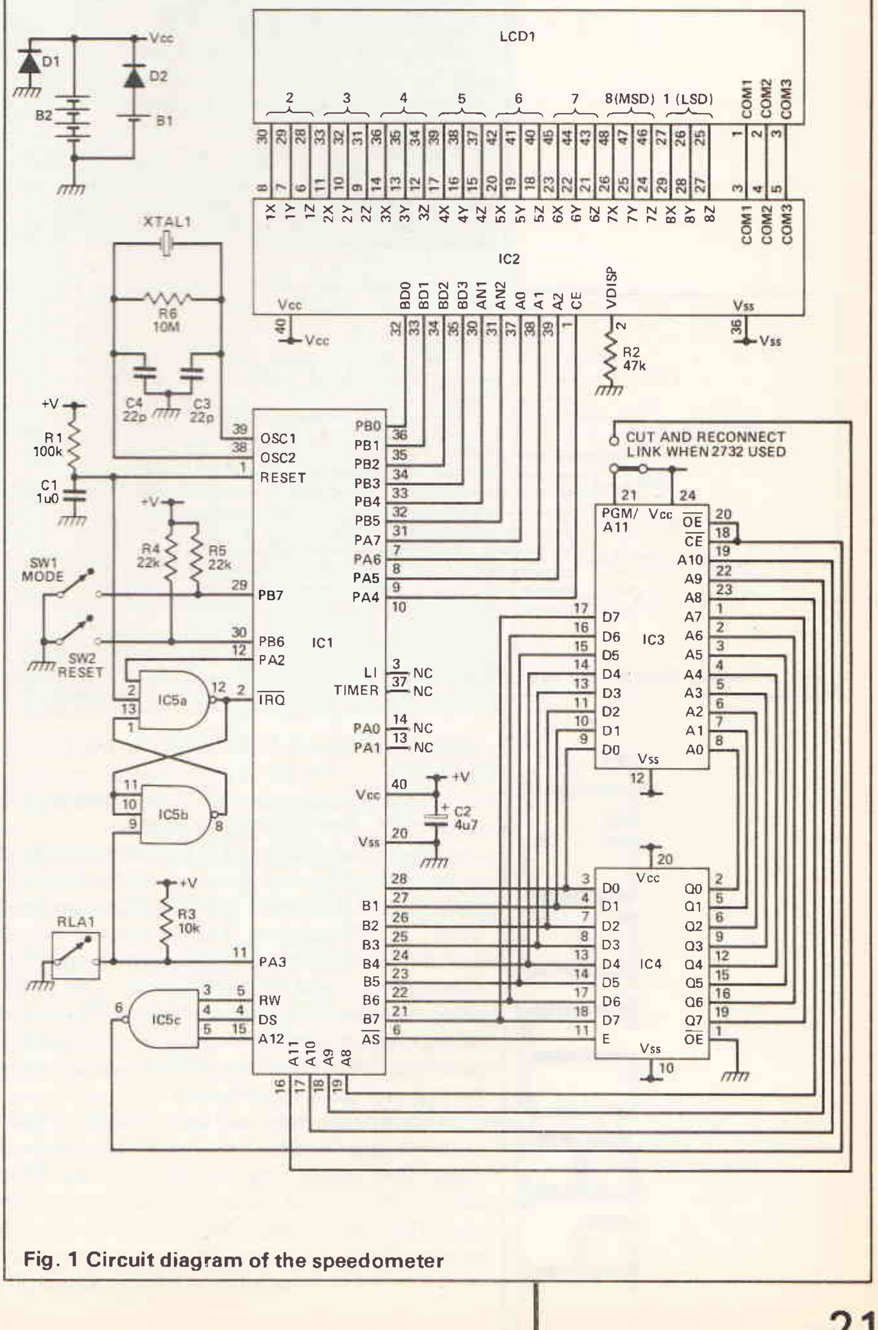


Fig. 1 Circuit diagram of the speedometer

THE 146805E2

The 146805E2 is a CMOS microprocessor based around a cut down version of the 6800. It contains one 8-bit accumulator (A), an 8-bit index register (X), a 5-bit condition code register, a 13-bit program counter (giving an 8K addressing range) and a 13-bit stack pointer.

The upper seven bits of the stack pointer are fixed so that the stack uses the top 64 of the 112 bytes of internal RAM (which runs from &0010 to &007F). All remaining locations in the memory map are available for use by external hardware with the interrupt vectors placed at the very top.

Two 8-bit I/O ports and their corresponding data direction registers are also in the zero page memory map along with the timer and its control register. The input to the timer may be from the processor clock or from the TIMER pin (or both ANDed) and a software selectable prescaler can be used to divide the input by powers of 2-128. The output from the prescaler goes into an 8-bit timer counter which can generate an interrupt when it counts down from &01 to &00.

An on-board oscillator simplifies the clock circuitry and crystals up to 5MHz may be used when V_{cc}=5V. The maximum crystal frequency allowed falls linearly with supply voltage to 1MHz at V_{cc}=3V.

Five clock periods are used per bus cycle, the relative timings for which are given in Fig. 2. To save pins, address lines 0-7 are multiplexed with the data bus. The falling edge of the address strobe (AS) latches the address in the earlier part of the cycle leaving the latter part of the cycle for data.

Data may be placed on the bus when the Data Strobe (DS) is high and is latched by the receiving device on its falling edge.

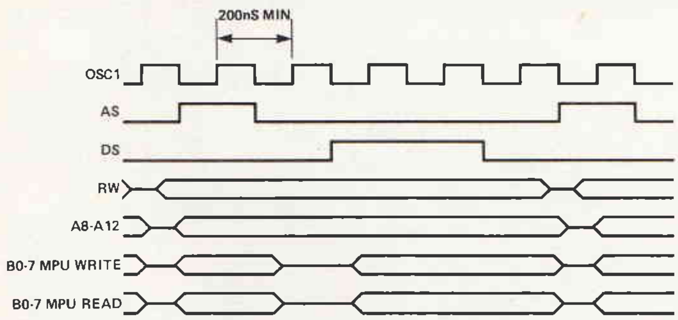


Fig. 2 Timing diagram for the 146805

some meaning can be attached to the 0.01mph/kmh digit.

Pressing the reset switch in any of the three modes will clear the data in all three.

The Time Trial mode is the most complicated to use and yet one of the most useful. This mode displays a trial distance in whole miles/km ranging from 1 to 100 inclusive. A short press of the mode switch will change to the next mode but if depressed for over a second then the trial distance will count round until it is released. Then on the falling edge of a press of the reset switch, the trip functions are all cleared and a decimal point on the far right of the display is set.

The speedometer will then function as normal until the Trip Distance reaches the value set in the Time Trial mode. The far right decimal point is then turned off and the trip functions are inhibited until they are reset. This allows the time and average speed at the trial distance to be preserved until a suitable time is found for them to be read.

Software

The Speedometer program is driven by two sources of interrupt, one from the internal timer which times out at 80Hz and the other from the wheel relay at one per revolution. The timer interrupts are used to update the time modes and scan the mode and reset switches. By making full use of the 8-bit counter the period of the wheel rotation can be measured to a resolution of 1/20480sec.

This leaves the diameter of the wheel as the sole source of any significant error. Each wheel revolution triggers a background program to update the distance and calculate the speed — average speed is only calculated when needed for display.

The main problem with having two independent interrupt sources is the potential for conflict when both occur together. This is more serious for the wheel interrupt since delays in reading the time at which it occurs will result in the wrong speed being calculated. To ensure wheel interrupts are not delayed, the timer interrupt routine clears its source immediately and enables interrupts before continuing with advancing the time.

In return, the wheel interrupt must be very short so there is no possibility of another timeout before the previous one has been properly processed. Therefore the wheel interrupt simply reads the current time (and checks if a timeout is imminent to check for overflows), sets a flag and terminates.

A background program continuously tests this flag and when set it updates the distance counters, calculates the speed (and average speed if need be) and checks for top speed. When that is done the flag is cleared ready for the next wheel interrupt. The time taken to do all that is comparable to the time interrupt period and therefore cannot be included within the wheel interrupt routine.

Each time a wheel interrupt routine has been processed by the background program, the display is updated. One consequence of this is that in the average speed mode, the reading will not gradually decrease while the bike is stationary simply because no wheel revolutions are occurring to trigger a new calculation and display update. If a wheel interrupt has not occurred for one minute then the display is blanked and the STOP mode entered.

When the background program is not being executed the power-saving WAIT state is entered. Processing halts although the crystal still oscillates and instruction execution commences on receipt of the next wheel or timer interrupt.

The setup modes determine several parameters for the main program. The wheel size determines the amount which is added to the sub 0.01mile/km distance counters each time the wheel revolves. Each time that 0.01mile/km is passed, an amount corresponding to 0.01mile/km is deducted from the counter and the trip and total distance registers are incremented. Both are kept in BCD format which makes it simple to send to the display — and saves a lengthy series of calculations every time the display is updated.

A binary count of the trip distance is updated in parallel to the BCD count. This is used for calculating the average speed in a form ready for division by the trip time.

The total and trip time registers are also updated in BCD format for the same reasons as

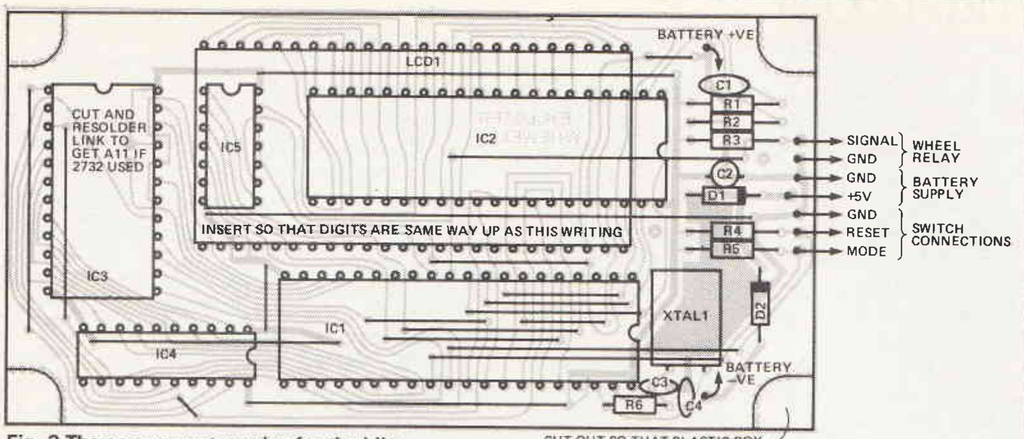


Fig. 3 The component overlay for the bike speedometer

the distance registers. A binary count of the trip time is also kept ready for calculating average speed. To save on processing time (and hence power) the average speed is only calculated in the mode in which it is displayed. Each time the display is updated the distance is multiplied by 1000 before a 32-bit division by the trip time takes place. This produces the result in the correct units for display. All that is left now is a series of divisions by 10 to convert the binary result into BCD.

When selecting between imperial and metric units, all that is done is to select a different table for the wheel sizes. Each entry in the metric list is 1.609344 times as big as its imperial counterpart so the distances come out in km rather than miles. No other changes are necessary since the time base used to calculate speed is the same in both cases.

One feature of the speedometer is that when a change of units is made, the total and trip distances are corrected accordingly. This involves converting the BCD counts to binary, scaling up or down by a factor of 1.609344 and then converting back from binary to BCD. Going to and from another set of units usually results in a loss of 0.01mile/km due to rounding off in the division routine.

Construction

A single sided PCB (see Fig. 3) has been produced for the speedometer which fits into a 120×65×40mm plastic box. Boxes of exactly the same size are also made in diecast aluminium and both have four 3mm screws to attach the lid to the rest of it.

The four corners of the PCB must be radiused so clearance is provided for the columns into which the lid screws fit. The PCB is marked for this.

The first thing to do is to solder the wire links into position on the PCB. There are nearly 20 of these and some run underneath the ICs. Insulating wire should be used (wire wrap is best) since a number of links are close together. The next stage depends on your use of IC sockets.

If the EPROM is the only device destined for an IC socket then the other ICs can be soldered straight in — paying particular attention to their orientation. The remaining passive components can also be soldered straight in — extra support should be given to the liquid crystal display with double sided sticky foam.

PARTS LIST

RESISTORS (all ¼W 5% unless specified)	
R1	100k
R2	47k (1%)
R3	10k
R4, 5	22k
R6	10M
CAPACITORS	
C1	100n ceramic
C2	4μ7 tantalum
C3, 4	22p ceramic
SEMICONDUCTORS	
IC1	MC146805E2 or CDP6805E2T
IC2	ICM7231BFIPL
IC3	ETC2716Q
IC4	74HC373
IC5	74HC10
D1	1N4001
D2	1N4148
LCD1	8-digit triplexed LCD
MISCELLANEOUS	
B1	4×1.2V NiCd batteries and holder
B2	3.6V AA lithium cell
SW1, 2	SPST push switch
RLA1	Reed relay
X1	3.2768MHz crystal

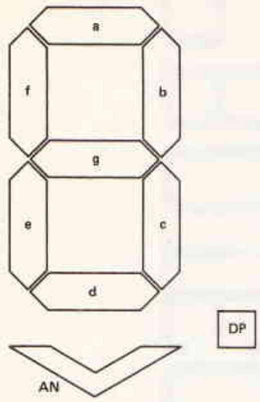
PCB. Bar magnet. 2×24-way socket strips for LCD (if required). Connecting cable. Case. Clear sticky plastic.

BUYLINES

A few of the components required for this project are difficult to come by. The processor (IC1) can be obtained from Jermyn Distribution (Tel: (0732) 450144) as can the LCD driver (IC2). The LCD itself can be purchased from Verospeed (Tel: (0703) 644555) or from Farnell Electronics (Tel: (0532) 636311) as part number 175-595. Farnell is usually unwilling to trade with the public but all Farnell components may also be obtained from Trilogic (Tel: (0274) 684289).

The author can supply programmed EPROMs for this project for £6 (if EPROM supplied — note this project uses a low power 2716) or £14 inclusive of the EPROM. The EPROM source code is available copied onto a BBC micro disk (40 or 80 track disk supplied) for £7.50 or with the 6805 cross assembler for £15. The author will also make up boards from the ETI PCB Service without the case or EPROM for £41.

Please address software board make-up enquiries and orders to Leycester Whewell, 1 Park Terrace, Berrington Road, Tenbury Wells, WR15 8EJ.



CONNECTIONS TO EACH DIGIT

	COM1	COM2	COM3
X	f	e	AN
Y	a	g	d
Z	b	c	DP

Fig. 6 Connections and multiplexing of the triplexed LCD

TRIPLEXING

An important consideration for the design of any display with a large number of independent elements is the arrangement of connections to the driver circuitry.

With large displays this is a large problem since the number of connections which have to be made means it is difficult to keep pins to a DIL format.

The simplest way to cut the number of connecting pins (and as a consequence, the complexity of the drive circuit) is to multiplex the display. This means that each character of the display is only active for a short period of time (of the order of several ms) before giving way to the next one.

The cycle for the whole display must be repeated at least 30 times per second so the human eye responds to a time-averaged light level from each character. It cannot normally detect that each digit is on for a fraction of a second.

Multiplexing LEDs is very straightforward. Each character of the display has either all the anodes (or cathodes) of the component LEDs joined together and these are fed to separate drive outputs. Each cathode (or anode) of a LED in a character is wired to the corresponding one in each of the other characters. These also go to a set of drive circuits.

So, for a 4-digit display of seven segments each, there would be four connections for the digit common wires and seven connections for the segment wires — a total of 11 wires to drive 28 display elements.

For each character in turn, current is allowed to flow through its common terminal only while current is allowed to pass through those segments of that character which are on. The remaining digits are all blank until it is their turn in the cycle.

Multiplexing does have limitations. For an n-character display, each can only be active for 1/n of the time for each cycle, so n is usually under 10. Otherwise there is a problem with overall brightness.

The same principle of multiplexing applies to liquid crystal displays as well. However, it is far more complex because an ordinary LCD is driven with alternating current — a feature which is necessary to prevent electrolysis of the display fluid.

A square wave signal (about 30-200Hz and 3-4V peak-to-peak) is applied to the backplane of the display. The amount of contrast produced by each element depends upon the difference in voltage levels compared with the backplane. An element which is off has the same voltage levels applied to it as the backplane so the difference is always zero. An element that is on has the opposite voltage to the backplane applied to it which keeps a constant difference between them.

Since each element must always be kept at the same or opposing voltage to the backplane, a new approach must be found for multiplexing. As indicated earlier, the contrast depends upon the difference in voltage levels between the segment and the backplane. Since the whole system is running on alternating current it is possible to calculate a root mean square (RMS) voltage difference between the two beyond which an element will appear to be on and below which it will appear to be off.

An RMS voltage of under 1.1V produces a low contrast so that the element appears to be off. Above 2.1V the contrast is such that the element is on. These thresholds decrease as temperature increases at a rate of about 7mV per °C.

The greater the ratio of RMS voltages for 'on' to 'off' elements the better because this also increases the display viewing angle.

In the display used in the speedometer there are three backplanes running parallel to another along the length of the display. Each digit has three connections to it called segment lines (they run across the display) which make a matrix of nine points with the backplanes.

A display element is placed at each crossing point (see Fig. 6) so there is sufficient capacity for the seven segment digit, a decimal point and an annunciator arrow.

A waveform must be applied to each of the backplates and to the segment lines so a sufficient RMS voltage can be created at any point in the matrix (and so turn on that element) while at the same time, the RMS voltage across the elements that are off is kept below 1.1V.

Care must be taken in soldering in the LCD. I have come across two types which are suitable for this display. One type has the pins bonded directly to the glass substrate and I strongly recommend that a socket is used for these as too much heat from can easily damage the tin/indium strip which connects the pins to the rest of the display.

The second type has a special contact strip for each side of the display. When assembled the whole can be soldered in directly to the board without much problem of heat damage. There will probably be 26 pins per strip for the display but only the middle 24 are needed, so the outer ones can be cut off.

If you use IC sockets throughout then check for clearance between the display driver chip and the display above it before soldering. The procedure for the rest of the assembly is as above.

The final component to be soldered is the data retention cell which is mounted on the underside.

```
0000  16 D9 19 63 1B ED 1E 77 21 01 22 46 22 FB 23 8B
0010  24 C5 28 DB 2C F1 31 07 35 1D 37 28 38 4C 39 33
0020  9B 9C A6 F4 B7 04 A6 F0 B7 00 A6 3F B7 05 3F 01
0030  A6 05 B7 09 A6 FF B7 08 CD 18 64 CD 1D 45 1F 09
0040  1D 09 8F 0F 1B 05 CD 1E 4B 1F 1B CD 1D 45 3D 16
0050  2A F0 04 00 04 3F 16 20 E9 3F 63 CD 1D EB 8E CD
0060  1D 45 20 DA 4F AE 54 E7 10 5A 2A FB 1E 34 A6 10
0070  B7 16 A6 05 B7 35 A6 28 B7 38 B7 39 A6 90 B7 3D
0080  10 62 81 3F 1C 3F 1D 3F 1E 3F 1F AE 20 38 23 39
0090  22 39 21 39 20 39 1F 39 1E 39 1D 39 1C B6 1C B1
00A0  24 25 32 26 16 B6 1D B1 25 25 2A 26 0E B6 1E B1
00B0  26 25 22 26 06 B6 1F B1 27 25 1A B6 1F B0 27 B7
00C0  1F B6 1E B2 26 B7 1E B6 1D B2 25 B7 1D B6 1C B2
00D0  24 B7 1C 3C 23 5A 26 B5 81 3F 1F 3F 1E AE 10 38
00E0  23 39 22 39 1F 39 1E B6 1E B1 26 25 16 26 06 B6
00F0  1F B1 27 25 0E B6 1F B0 27 B7 1F B6 1E B2 26 B7
0100  1E 3C 23 5A 26 D9 81 E6 00 B7 23 3F 1F AE 08 38
0110  23 39 1F B6 1F B1 27 25 08 B6 1F B0 27 B7 1F 3C
0120  23 5A 26 EB 81 BF 28 AE 03 E6 20 E7 24 6F 20 5A
0130  2A F7 3F 29 3F 1F 3F 1E 20 52 34 1C 24 1E B6 22
0140  BB 27 B7 22 B6 21 B9 26 B7 21 B6 20 B9 25 B7 20
0150  B6 1F B9 24 B7 1F B6 1E B9 29 B7 1E 34 1D 24 22
0160  B6 23 BB 27 B7 23 B6 22 B9 26 B7 22 B6 21 B9 25
0170  B7 21 B6 20 B9 24 B7 20 B6 1F B9 29 B7 1F 24 02
0180  3C 1E 38 27 39 26 39 25 39 24 39 29 3D 1C 26 AA
0190  3D 1D 26 C8 BE 28 81 4F B7 20 B7 21 B7 22 B7 23
01A0  A6 03 B7 2A 3F 1C A6 0A B7 1D CD 19 25 F6 44 44
01B0  44 44 BB 23 B7 23 24 0A 3C 22 26 06 3C 21 26 02
01C0  3C 20 3F 1C A6 0A B7 1D CD 19 25 F6 A4 0F BB 23
01D0  B7 23 24 0A 3C 22 26 06 3C 21 26 02 3C 20 5C 3A
01E0  2A 2A C1 9F A0 04 97 81 9F AB 04 B7 2A A6 03 B7
01F0  2B 3F 24 3F 25 3F 26 A6 0A B7 27 CD 18 83 B6 1F
0200  3A 2A BE 2A F7 CD 18 83 B6 1F 48 48 48 48 BE 2A
0210  FB F7 3A 2B 2A E5 81 15 00 1E 1B B6 08 27 06 A1
0220  01 27 F8 26 03 9A 9D 9B 40 97 B0 17 B7 19 B6 18
0230  A2 00 B7 1A BF 17 3F 18 B0 1F 09 07 00 05 0E 1B
0240  02 14 00 B6 18 A1 F0 24 0C 3C 18 A0 EF 26 06 B7
0250  10 B7 11 B7 12 B6 1B A8 01 B7 1B 01 1B 0F 9A CD
0260  1A A7 B6 34 2B 07 AD 06 AD 12 CD 1A BD 80 3A 38
0270  26 09 A6 28 B7 38 AE 52 CD 1C 09 81 0C 63 0D 3A
0280  39 26 09 A6 28 B7 39 AE 56 CD 1C 09 81 3A 3D 26
0290  14 A6 90 B7 3D 3A 16 0C 63 0B 9B 3C 3C 26 06 3C
02A0  3B 26 02 3C 3A 9A 81 AD 24 CD 1B 7D 0E 13 03 3F
02B0  15 81 0F 14 FA B6 15 2B F8 4C B7 15 A1 15 26 F1
02C0  B6 34 2B ED A6 FF B7 34 B6 36 B7 37 81 0E 01 24
02D0  B6 13 2B 0A 4C A1 04 25 02 A6 80 B7 13 81 BE 34
02E0  A3 07 26 F9 4C A1 A8 27 06 A1 B2 25 EE A6 A8 B7
02F0  13 CC 1B 5E 0E 13 03 3F 13 81 BE 34 A3 07 26 06
0300  B6 13 A1 A8 24 F1 3F 13 3C 34 26 05 A6 80 B7 34
0310  81 B6 34 2A 0B A1 81 26 03 CC 1C 4E 3F 34 20 07
0320  A1 08 25 02 3F 34 81 4F 3D 36 27 02 A6 08 BB 35
0330  48 97 D6 18 00 B7 41 B7 1C D6 18 01 B7 42 B7 1D
0340  3F 20 A6 00 B7 21 A6 04 B7 22 A6 65 B7 23 CD 19
0350  25 B6 21 B7 43 B6 22 B7 44 B6 23 B7 45 81 0E 63
0360  1B B6 62 AB 01 B7 62 AB 06 28 0B B7 62 AB 60 24
0370  0B B7 62 3C 61 81 3D 61 27 02 3F 61 81 0C 01 0E
0380  B6 14 2B 09 4C A1 04 25 02 A6 80 B7 14 81 0E 14
0390  03 3F 14 81 3F 14 0E 13 F4 B6 34 2B 14 27 EE A1
03A0  02 27 EA A1 04 27 E6 A1 07 27 20 A1 05 27 52 26
03B0  22 A1 80 26 0B 3C 36 B6 36 A0 03 25 02 3F 36 81
03C0  3C 35 B6 35 A1 08 25 02 3F 35 81 0F 63 03 3F 63
03D0  81 1E 63 4F B7 5E B7 5F B7 60 B7 3E B7 3F B7 40
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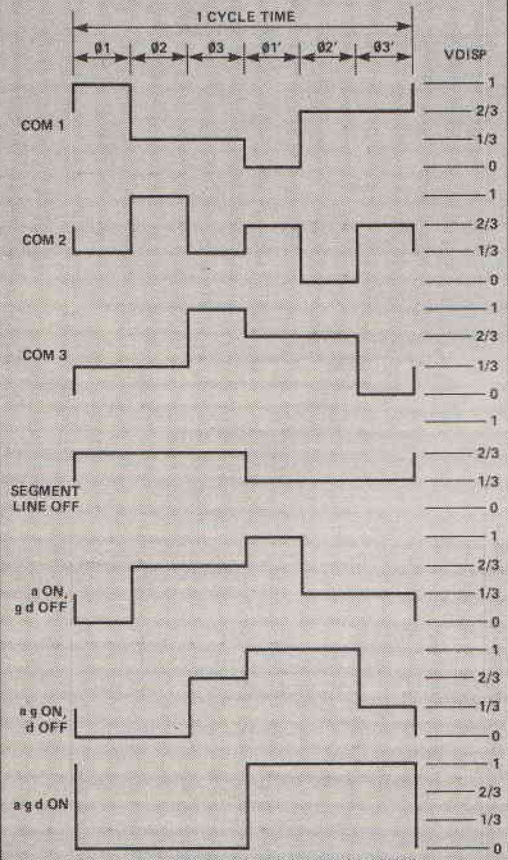
Listing 1 The hex dump of the used parts of the EPROM



COM1, COM2 & COM3 ACTIVE ON Ø1(Ø1'), Ø2(Ø2') & Ø3(Ø3') RESPECTIVELY
DIAGRAM SHOWS TIMINGS FOR SEGMENTS ON LINE Y OF DISPLAY

Fig 7 Timing of the triplexed LCD

Figure 7 shows the voltage waveforms that are applied to the three backplanes as well as some examples of segments that are off and on. Within the display driver chip there are three 75k resistors in series which are used to generate the intermediate voltage levels $\frac{1}{3}V_{DISP}$ and $\frac{2}{3}V_{DISP}$. One end of the resistor chain is attached to the +5V supply of the chip and the other is connected to another pin so the voltage across the display can be controlled.

Since this project is powered by NiCd batteries which have good voltage/discharge characteristics, a constant voltage can be applied across the display just by tying the open end of the chain to ground with a 1% resistor (R2).

The mean voltage applied to the backplanes is V/2. For the parts of the cycle in which a particular backplane is not being used its voltage is kept at either V/3 or 2V/3 — a difference of V/6. When it is in use, either V or 0V is applied which is a difference of V/2.

For a given backplane, if the segment on a particular segment line is off then the voltage applied to it is between V/2 and that of its backplane. This keeps the RMS voltage between the two as low as possible for that segment and yet not too high for the other segments in that line for them to be turned on when they shouldn't.

When a particular segment is on, the voltage applied to it is the complement of that on its backplane. This causes the RMS difference between them to go above the 'on' threshold and yet that of the other segments is still kept below the 'off' threshold.

The main drawback of multiplexing LCDs is that the RMS voltage across off segments is not zero (unlike non-multiplexed displays). This causes some polarisation of the fluid which reduces the display angle by perhaps 20°.

It is for this reason that it is difficult to read a computer LCD screen (greatly multiplexed) at more than 30° to the normal but not a simple LCD watch which does not have a multiplexed display. These problems have very little effect on the speedometer since the rider is viewing it from a nearly constant position.

This should not be connected until the batteries have been installed. This simplifies checking the power on reset and avoids draining the cell with the processor running. Foam strips with adhesive on both sides should be used to fix the cell to the board as well as insulate it from the tracks.

Before soldering, a piece of wire should be used to tie the cell to the underside of the board using the two remaining unused holes. Experience has shown that the contact leads on the cell are not strong enough by themselves to support it indefinitely against the vibrations of the road.

Alternatively, two wires could be used to join the cell to the board so that it is free to rest on the base of the case.

Once the PCB is completed, the EPROM (see Listing 1) can be inserted and some testing carried out by temporarily connecting the batteries, switches and reed relay. Correct operation can be verified by running through the operating modes of

```
03E0  B7 56 B7 57 B7 58 B7 59 B7 3A B7 3B B7 3C B7 4E
03F0  B7 4F B7 50 B7 51 A6 90 B7 3D A6 28 B7 39 1D 63
0400  81 4F B7 5C B7 5B B7 5A 81 E6 03 AB 01 E7 03 AB
0410  06 28 3A E7 03 AB A0 24 34 E7 03 E6 02 AB 01 E7
0420  02 AB 06 28 28 E7 02 AB A0 24 22 E7 02 E6 01 AB
0430  01 E7 01 AB 06 28 16 E7 01 AB 60 24 10 E7 01 F6
0440  AB 01 F7 AB 06 28 06 F7 AB 60 24 01 F7 81 B6 36
0450  B1 37 27 F9 4D 27 4B AE 4A AD 2B AE 4A CD 19 E8
0460  AE 4E AD 22 AE 4E CD 19 E8 3F 20 B6 3E B7 21 B6
0470  3F B7 22 B6 40 B7 23 AD 10 B6 23 B7 40 B6 22 B7
0480  3F B6 21 B7 3E 81 CD 19 97 A6 C9 B7 1C A6 2B B7
0490  1D CD 19 25 A6 7D B7 26 4F B7 27 B7 25 B7 24 CC
04A0  18 BB AE 4A AD 2B AE 4A CD 19 E8 AE 4E AD 22 AE
04B0  4E CD 19 E8 3F 20 B6 3E B7 21 B6 3F B7 22 B6 40
04C0  B7 23 AD 10 B6 23 B7 40 B6 22 B7 3F B6 21 B7 3E
04D0  81 CD 19 97 A6 7D B7 1C 3F 1D CD 19 25 3F 24 3F
04E0  25 A6 C9 B7 26 A6 2B B7 27 CC 18 8B 18 00 20 00
04F0  22 00 24 00 26 00 27 00 27 56 28 00 AE 2C B6 36
0500  E7 06 A6 0F E7 04 E7 05 E7 07 A6 01 20 29 BE 35
0510  58 D6 1C EC A4 0F AA 20 B7 31 D6 1C EC 44 44 44
0520  44 B7 30 D6 1C ED A4 0F B7 33 D6 1C ED 44 44 44
0530  44 B7 32 AE 2C A6 02 E7 01 A6 0F E7 03 A6 0A F7
0540  E7 02 CC 1D F1 BE 34 2A 06 A3 81 27 C1 26 AD 58
0550  DC 1D 53 20 0E 20 12 20 1D 20 1F 20 29 20 31 20
0560  37 20 39 AE 4A AD 47 20 04 AE 4E AD 41 B6 31 AA
0570  20 B7 31 CC 1D F1 AE 52 20 02 AE 56 AD 30 B6 2F
0580  AA 20 B7 2F 20 E7 AE 0F B6 12 AA 0F B7 12 20 02
0590  AE 59 3F 2C AD 1B 20 D5 AE 5D 20 F6 3F 2C B6 61
05A0  B7 2E B6 62 B7 30 A6 0F B7 32 AD 11 20 BF F6 B7
05B0  2C E6 01 B7 2E E6 02 B7 30 E6 03 B7 32 AE 06 E6
05C0  2C A4 0F E7 2D E6 2C 44 44 44 44 E7 2C 5A 5A 2A
05D0  EE 5F E6 2C 26 09 A6 0F E7 2C 5C A3 05 25 F3 BE
05E0  34 A6 10 EA 2C E7 2C 81 AE 07 A6 0F E7 2C 5A 2A
```

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05F0  FB B6 00 AA F0 B7 00 B6 33 0F 63 02 AA 20 B7 01
0600  19 00 18 00 1F 00 B6 2C B7 01 19 00 18 00 1D 00
0610  B6 2E B7 01 19 00 18 00 1E 00 B6 2D B7 01 19 00
0620  18 00 18 00 B6 31 B7 01 19 00 18 00 1C 00 B6 2F
0630  B7 01 19 00 18 00 1F 00 B6 30 B7 01 19 00 18 00
0640  1D 00 B6 32 B7 01 19 00 18 00 81 3D 34 2B 13 CD
0650  1E 63 CD 1E B5 CD 1E D8 CD 1E EB CD 1F 39 A6 10
0660  B7 16 81 B6 19 B7 27 B6 1A B7 26 3F 1E B6 43 B7
0670  1F B6 44 B7 22 B6 45 B7 23 CD 18 DD B6 22 A1 FF
0680  27 32 3F 26 A6 0A B7 27 CD 18 D9 B6 1F B7 12 CD
0690  18 D9 B6 1F 48 48 48 48 BB 12 B7 12 CD 18 D9 B6
06A0  1F B7 11 CD 19 0B B6 1F 48 48 48 48 BB 11 B7 11
06B0  B6 23 B7 10 81 B6 10 B1 5A 25 1C 26 0E B6 11 B1
06C0  5B 25 14 26 06 B6 12 B1 5C 25 0C B6 10 B7 5A B6
06D0  11 B7 5B B6 12 B7 5C 81 B6 47 BB 42 B7 47 B6 46
06E0  B9 41 B7 46 24 04 AE 4A 20 35 81 0C 63 30 B6 49
06F0  BB 42 B7 49 B6 48 B9 41 B7 48 24 22 3C 40 26 06
0700  3C 3F 26 02 3C 3E AE 4E AD 15 0F 63 11 B6 4F B1
0710  61 25 0B B6 50 B1 62 25 05 A6 40 B7 63 81 81 BF
0720  28 9F AB 04 97 5A F6 AB 01 F7 AB 06 28 0A F7 AB
0730  60 24 05 F7 B3 28 26 ED 81 B6 34 A1 06 26 3D B6
0740  3A BA 3B BA 3C 27 35 3F 20 B6 3E B7 21 B6 3F B7
0750  22 B6 40 B7 23 A6 03 B7 1C A6 E8 B7 1D CD 19 25
0760  3F 1D 3F 1C 3F 24 9B B6 3A B7 25 B6 3B B7 26 B6
0770  3C B7 27 9A CD 18 BB AE 5D CD 19 E8 81 80 00 00
0780  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0790  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
07A0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
07B0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
07C0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
07D0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
07E0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
07F0  00 00 00 00 00 00 1A 39 1A 39 1A 17 1F 7D 18 20
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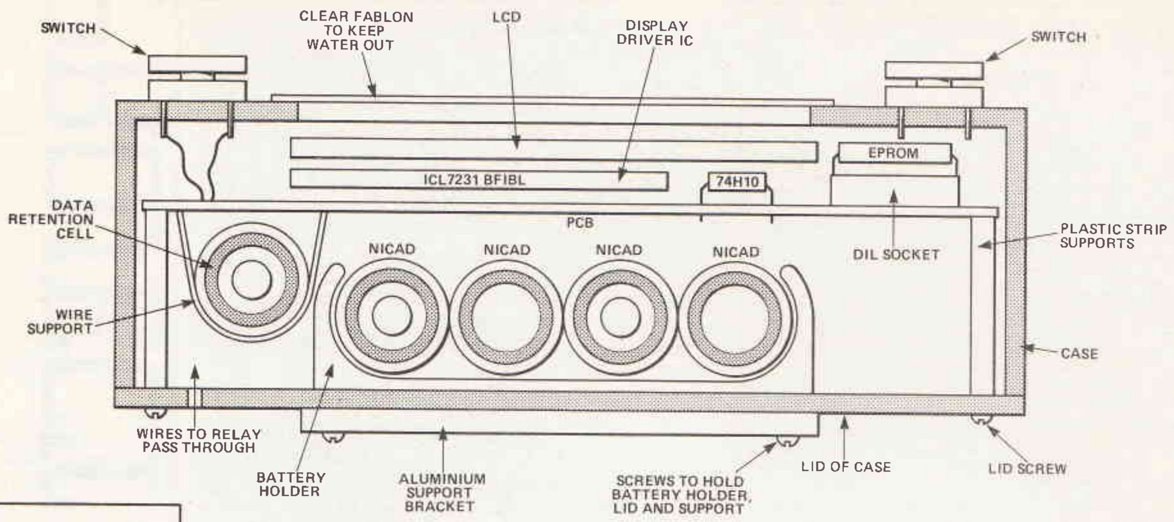


Fig. 4 Mounting the speedometer board in the recommended case

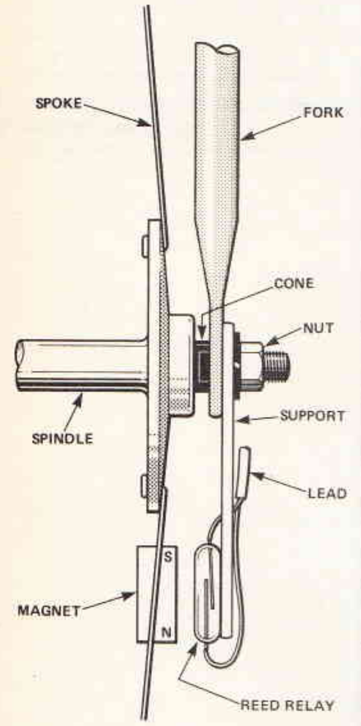


Fig. 5 The mounting of the reed relay and magnet on the bicycle forks and wheel

the speedometer, checking its function by opening and closing the relay with a magnet 'by hand.'

The plastic box normally includes some PCB supports which run in vertical grooves in the walls of the case. I have used these to hold the board at the correct height so the display can be seen through a hole cut in the case (Fig. 4). A little trimming of the board where the supports go may be needed in order to achieve a good fit.

To prevent rain getting into the case, it is used upside down so the lid is on the bottom with the display showing through what was the base. Clear self adhesive plastic film covers the display cutout to create a watertight seal.

The four AA NiCd cells are held in a 4×1 battery holder mounted at the base of the case, on the lid. The two screws holding the battery holder to the lid of the case are also used to attach it to the support bracket. I used a bent strip of aluminium to fix the speedometer box to the front brake assembly.

Low profile switches with short leads are the easiest to mount on the box. Two small holes were made in the case for each switch for the leads. Wires were soldered to the switches and passed through the case before gluing. No problems have ever been encountered in the rain with this arrangement of switches.

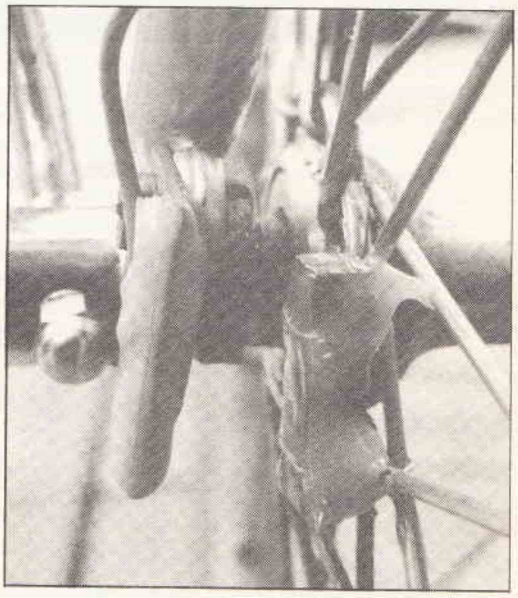
The reed relay lead passes through a small hole in the lid to where the relay is mounted at the bottom of the forks. If the clearance between the wire and the case is very small then no glue is needed to make a seal since surface tension will prevent water from seeping into the case.

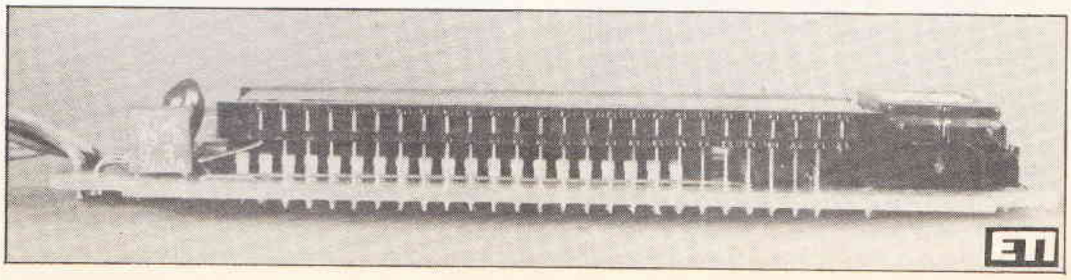
The relay can be mounted on a small aluminium bracket bolted to one of the front forks on the axle (Fig. 5). It is a good idea to encapsulate the mounted relay and any bare wiring to prevent triggering by rain. Silicone bath sealant or epoxy glue is suitable for this or even paint at a pinch.

The magnet is positioned on a spoke so that it passes within about 10mm of the relay (but does not touch it). The exact distance will vary with the type of magnet and reed relay used and must be found by trial and error.

The magnet can be fixed either by gluing/tying it to the spoke, by making another small bracket or by fixing it to one of the clip-on spoke reflectors which are easily and cheaply available from bike shops.

Once the reed relay and magnet are mounted and wired in, the case can be bolted to the handlebars, front brake calipers or wherever it can be conveniently read and operated and you can then peddle off into the sunset confident in the knowledge of exactly how fast you are going.





PROJECT

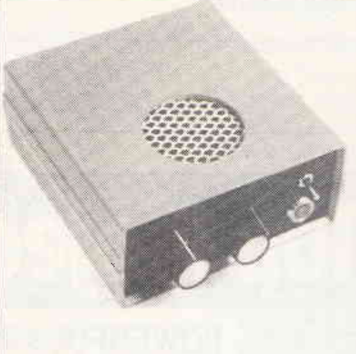
THE LUCID DREAM STIMULATOR

Paul Chappell's heavy breathing monitor can give you the night of your dreams

Let's face it, this is going to be an odd sort of project. Athletes, cyclists, swimmers, marathon runners and keep fit enthusiasts will find some good parts. Brainwave monitor owners have been considered, those with an interest in dreams will enjoy their bits and athletic brainy dreamers will get nourishing family goodness through and through. Let me explain.

It all started with the Dream Machine project, which you will no doubt remember from the November and December issues last year. The idea of the Dream Machine was to help you get a good refreshing night's sleep and to put you in the right frame of mind for some vivid and spectacular dream experiences. Shortly after the project was published, a letter dropped into the ETI mailbox — why not design a *lucid* dream stimulator? Then another, saying much the same. Then another. And another . . .

Well, we don't always go rushing off to design a project at the request of a single reader but the combined weight of a mailbag full of letters is something we have to take seriously.



The ETI Dream Machine and Brainwave Monitor, predecessors and possible basis for the Lucid Dream Stimulator

Many readers suggested modifying the Brainwave Monitor project to do the job but since it only appeared last year it's a bit too soon to think about doing another version. I'll give a few hints a bit later on, though, for anybody who has built one and would like to adapt it.

The way I eventually decided to tackle the project was to design a respiration rate meter (this is where the athletes come in) and to give it an output suitable for triggering a lucid dream stimulator. So this is what you get for your money: a short refresher course on sleep and dreams (lucid or otherwise), some *Tech Tips* style hints on modifying the Brainwave Monitor for lucid dream stimulation, a breathing rate meter for sports training and a breathing rate triggered lucid dream machine. Good value, eh?

Sleep And Dreams

When Bagpuss wakes up (and all his friends wake up) the chances are that he has dreamed, even although he may not remember anything about it (because he's stuffed).

Everybody dreams. Although dreams can occur at any time of the night, it is generally agreed that most of them happen during a special phase of sleep called *paradoxical* or *REM* (rapid eye movement) sleep. Not only are dreams much more frequent during the REM phase, they are also of higher quality and greater density.

The REM phases last for around fifteen minutes and may happen four or five times during the night. If you were watching someone else sleeping, you might notice that they became totally relaxed during these times. You might also see their eyes moving rapidly back and forth behind their closed lids.

When the REM phase was first discovered, it was thought to be nothing more than light sleep with dreaming. The brainwave traces in this phase then gave the first clue that something strange was going on — they looked just as if the sleeper was fully awake! Yet the muscles are more relaxed during this phase than in the deepest of ordinary sleep. Paradoxical indeed!

Many people have experienced a type of dream called a *lucid dream*, when the states of sleep and wakefulness become mixed up. In the mildest form, you might find yourself rushing downhill in a go-kart towards a pane of glass, and after a moment of panic think — so what? I'm only dreaming!

Some people manage to go a stage further and take control of their dream. Why have a pane of glass? Why not a feather pillow? And there it is, a nice, soft landing. Once you've got the hang of taking an active part in your dream life, there's no end to what you can do!

Lucid dreams can happen spontaneously and can often be brought on just by reading about them. But if they don't happen, there's not much you can do about it. Or is there?

One thing which seems to have a good success rate at bringing about lucid dreams is to disturb the sleeper slightly during a dream. A small electric shock seems to be the approved method — it sounds horrific but I'm talking about a little tingle, not an electric fencer zap.

The problem is — when do you administer the shock? Until someone comes up with a mind

PROJECT

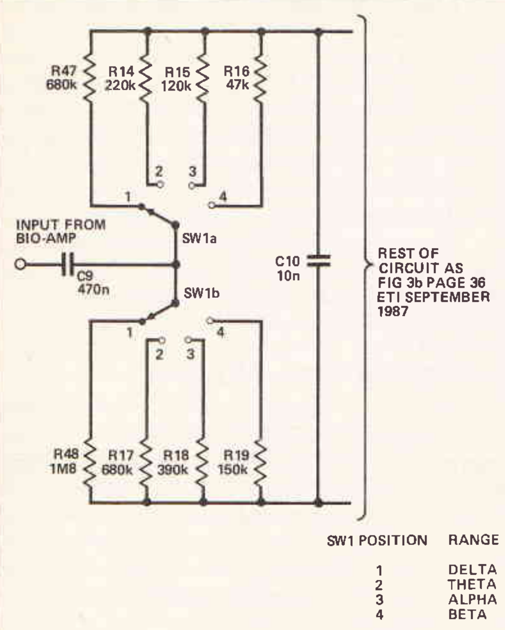


Fig. 1 Modification to the brainwave monitor for delta wave detection

occur from time to time and the trace begins to show evidence of the very slow delta waves.

The third and fourth stages both show large, slow delta waves — the third stage having some faster waves in evidence and the very deepest sleep of all being almost entirely delta waves.

During paradoxical sleep, a strange change in brainwave pattern takes place. Although the body is at its most relaxed, the brainwaves are those of alert wakefulness. One way to detect paradoxical sleep (with its high probability of dreaming) is to look for the reappearance of the faster daytime waves during the night.

If you are going to experiment with sleep and dreams, you may like to modify your brainwave monitor to pick up delta waves. I didn't make any provision for this in the original design, my reasoning being that if you were fast asleep, you wouldn't be awake to operate the monitor. Very logical it seemed at the time!

The mod is not strictly necessary but it's so simple that you might like to do it anyway. Figure 1 shows how. The three-way rotary switch selecting the ranges on the original monitor is replaced by a four way switch, and two extra resistors (R47 and R48) are added.

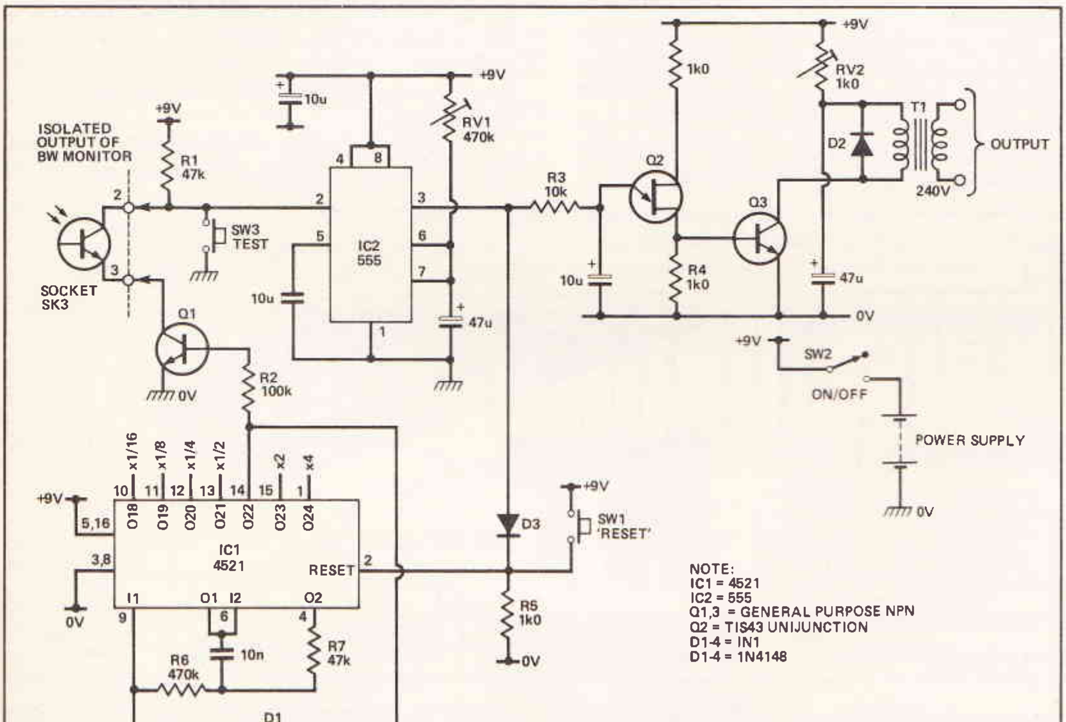


Fig. 2 Lucid dream shocker for the brainwave monitor

reading machine, there's no way to be absolutely sure when a sleeper is dreaming. The usual method is to detect the onset of paradoxical sleep and let statistics work for you: that's when there's the best chance of a dream taking shape. This is exactly what we shall be doing in this project, in several different ways!

Brainwaves And Lucid Dreams

Orthodox sleep is divided into four stages on the basis of brainwave traces. The first stage is drowsiness, which may or may not be followed by complete sleep. The alpha and beta rhythms of wakefulness diminish and slower theta waves appear. The overall EEG trace has a relatively low amplitude in comparison both with wakefulness and with deep sleep.

In the second stage, which could be called 'dozing off,' distinctive spindle-shaped waves

Compare Fig. 1 with Fig. 3b in the September 1987 Brainwave Monitor project and you'll soon see what needs to be done.

There is no room for the extra resistors on the PCB but they can be soldered directly to the switch (if you use a 3-pole 4-way type, it will have plenty of spare tags) and wires taken to the appropriate points on the underside of the PCB. It shouldn't look too untidy!

The pad type electrodes held on by pressure are perfectly good for daytime use but will soon become dislodged at night. Small disc type electrodes held on with sticking plaster are probably the best bet for home use.

There are two ways of detecting the onset of paradoxical sleep you might like to try. One is to look for the appearance of alpha waves during the night, for which the best electrode position will be the same as you use during the day. The other is to detect the eye movements associated with this phase of sleep. One active electrode on each temple and the reference electrode in the centre of your forehead will give a good signal from the eyes.

If you decide on the second approach, use the Alpha range on the monitor anyway to screen out theta and delta waves. Set the mode control to 'integrate' and adjust the gain control to the least sensitive point where the monitor reliably begins to sound after half a dozen or so eye movements. Don't forget to mute the output before settling down to sleep — you don't want to be woken up in the middle of a pleasant dream!

A suggested circuit to complete the lucid dream stimulator is shown in Fig. 2. The output of the circuit will give you a mild electric shock which should be just enough to disturb your sleep but not enough to wake you up.

The output, from a small mains transformer connected 'back-to-front', is taken to a pair of metal electrodes, which you can tape or bandage to your arm or leg. Both electrodes should be attached to the same limb to prevent a conduction path through your heart. As for all devices which make electrical contact with your body, it *must* be run from batteries and not from any kind of mains power supply.

With the electrodes in place, press the 'test' button and adjust RV2 to give something more than a tickle, but less than an aaaaaargh! Set RV2 to maximum resistance before you start — it's best to begin with a tickle and work your way upwards rather than the other way around! Set RV1 to give the duration of shock — a second or so should be enough.

When you are ready with all the electrodes in place, press the 'reset' button to clear the counter (IC1) and let yourself drift off to sleep. After about half an hour, the counter will have reached the point where O22 goes high. This arms the rest of the circuit and freezes the clock (via D1) so that it remains in a state of readiness until you dream.

When the brainwave monitor decides that you have entered the REM phase of sleep, IC2 is triggered which imparts your dose of electricity and resets the counter to disarm the circuit for another half an hour. With any luck, you'll be having a lucid dream in the meantime, and several more during the night at the start of each period of REM sleep.

The period of the counter can be altered as indicated in Fig. 2 by taking the output from a different pin of the IC. Fine control can be achieved by adjusting R7 — a larger value for a longer time period, a smaller value for a shorter one.

If you don't like the thought of an electric shock (however mild) you can probably rig up something to use the brainwave monitor's internal sounder to disturb you slightly. The only objection to using it unmodified is that it will continue to sound during the entire period of REM sleep, which may very well wake you up. Some kind of timer to allow it to sound for a few seconds and then shut it up for half an hour would be needed.

Since researchers into dreams seem to favour the shocks, I can only assume that they are more effective than the sounder in bringing on lucid dreams but the final choice is up to you.

Breathing Rate Monitor

Now we change direction and begin the breathing rate monitor. Anybody who takes a serious interest in sports or athletics (beyond watching them on TV!) will find this a very useful aid to training. On a very broad level, two guidelines to general fitness are your resting breathing rate (which should decrease as fitness improves) and the time your body takes to recover from exertion — the quicker the better.

The specific training requirement for different sports vary so widely that there's not a lot I can say about them here, other than to direct you to the sports section of your local library. If you belong to any kind of sports or fitness club, there will no doubt be somebody who can advise you on how best to train.

The main problem with designing a breathing rate monitor is that the information arrives so slowly! A common approach to rate meters of any kind is to count events over a certain period, updating the display at the end of each counting period. Let's suppose we do that with the respiration meter.

To make life easy, we could just count the number of breaths occuring over one minute, dump the result into a display and hold it while we collect another minute's worth of data. But what's the use of a display that only updates once a minute? A minute is an awfully long time if you're sweating away on an exercise cycle or pounding round a track! Cyclists will often train with thirty second bursts of maximum effort — they want to know what's happening while they're doing it, not a minute later!

OK, so how about we count the number of breaths over six seconds, multiply by ten to get the number of breaths per minute, then plonk that in the display and update it ten times a minute. But suppose the breathing rate is 15 per minute.

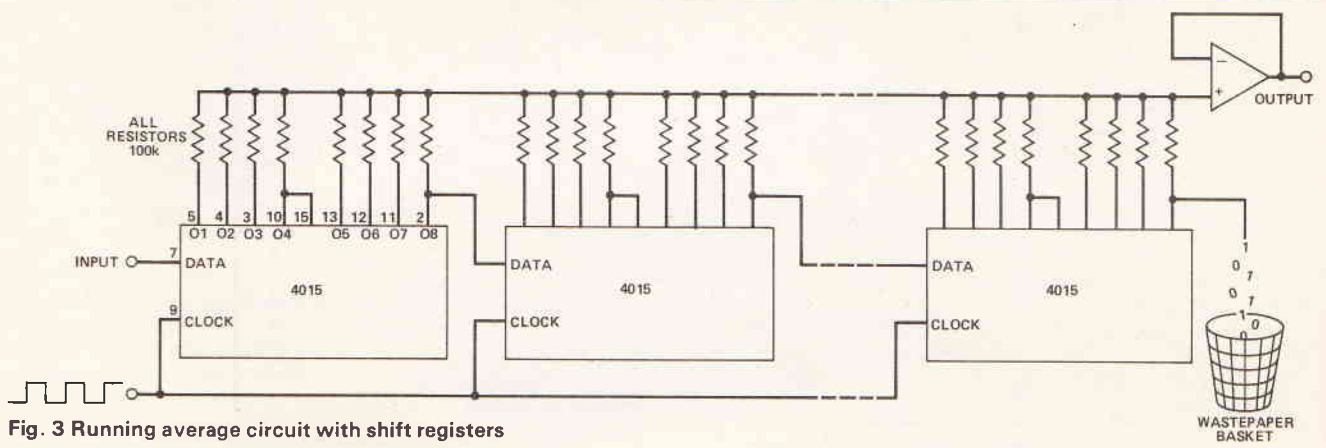


Fig. 3 Running average circuit with shift registers

During the six second sample period, one of two things can happen: we record one breath, or we record two breaths. There is no other possibility. Sometimes the display will show ten breaths per minute, sometimes it will show twenty. Never will it show fifteen! Reducing the sample period only reduces the resolution.

Right, we'll have twenty data collection units, each staggered by three seconds and updating the display in turn. Too expensive!

We'll measure the time between subsequent breaths, take the reciprocal and display that, updating after every breath. But will the input circuit reliably trigger at exactly the same point on each breath? Every bit of jitter will be displayed. Does the user really want to see the display flicking about as the time between subsequent breaths changes slightly? Probably not.

However the input is derived, we're clearly going to need some kind of running average circuit. One that settles fairly quickly and doesn't have excessive ripple. And so as not to bore you with my own analogue-versus-digital debate, I'll tell you without further ado: I'm going to do it digitally.

This sounds like heavy stuff — microprocessors, number-crunch ICs, crystal clocks and the like. No way! Do-it-all ICs may be convenient but they are also expensive and, unless you intend to use them to their full extent, not worth the silicon they're diffused on.

Figure 3 shows a little circuit for you to think about. In case you're just about to faint at the thought that I might be expecting you to solder a dozen shift registers together, let me reassure you quickly that it's not the circuit of the project, it just demonstrates the principle (although I did originally design it for a practical purpose but thereby hangs another tale, as they say).

The way it works is quite simple. Suppose that the clock is set so that any data at the input takes exactly one minute to make its way though the shift register chain and drop out of the other end. Suppose that each breath causes a single 1 to be fed into the first shift register. At all other times the input is zero.

When the circuit has been running for a while, the number of 1s making their way through the chain will be exactly equal to the number of breaths taken in the previous minute.

If you look at the output of the circuit, you'll notice that if the shift registers were entirely full of 1s, the output would be at $+V_{DD}$. If they were full of 0s, the output would be at V_{SS}. Suppose that there were 100 shift register sections in the chain, each connected through a resistor R to the output buffer. You might have a sneaking suspicion that each extra output that went to a 1 would step up the output voltage by 1% of V_{DD}. And you'd be absolutely right!

The voltage at the output measures the number of 1s in the chain, which measures the number of breaths taken over the previous minute.

Of course, there's no need for 100 shift register sections. By juggling the clock rate, the number of ICs and the gain of the output buffer, you can have any resolution, scale factor and averaging interval that your heart may desire.

The disadvantage of the circuit is plain to see. In a nutshell, too many IC's. If you enjoy logic puzzles, see if you can come up with a way of making this into a practical circuit. Oh yes, and I'd like a digital output suitable for driving seven segment displays please. I've got to do it in time for next month's issue, so wish me luck! ETI

DYNAMIC NOISE REDUCTION

Manu Mehra has cut noise to the minimum with this simple project for beginners to electronics

In many audio applications a 'complementary' noise reduction system such as a compander or Dolby cannot be implemented. These involve encoding the program material before recording it and decoding it prior to playback. The encoding involves compressing the dynamic range of part or all of the signal whilst decoding involves expanding the dynamic range back to its original form.

In systems where such complexity is not desirable or encoded material is unavailable, a non-complementary system proves more effective.

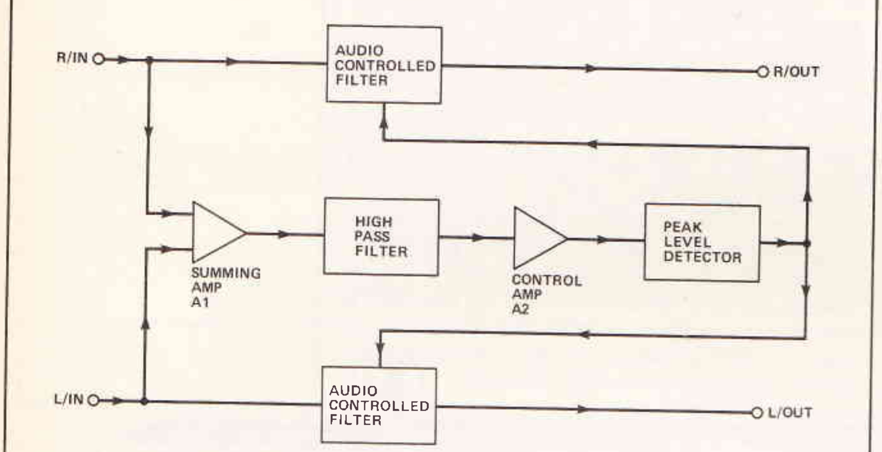
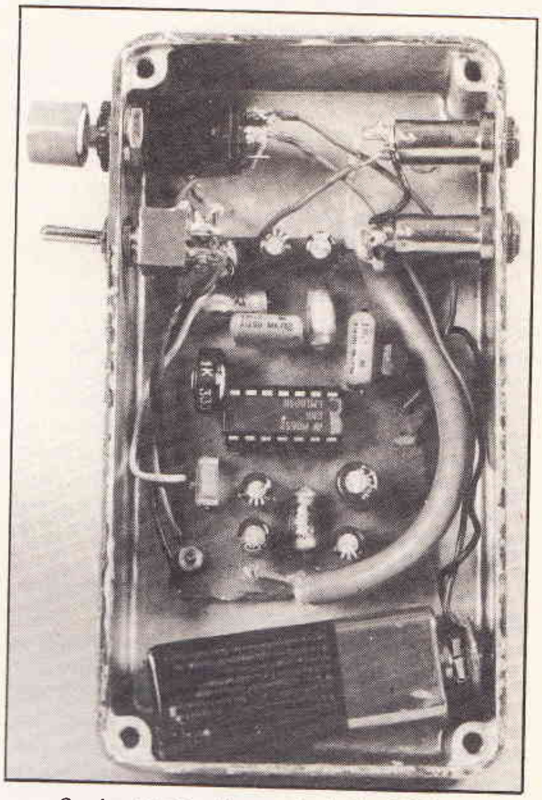


Fig. 1 Block diagram of the dynamic noise reduction system



Such applications include FM stereo receivers, cassette and tape decks without a noise reduction system or even a turntable where noise reduction would not go amiss.

The system described here is known as *dynamic noise reduction* and is introduced into the signal path between the source circuit and amplifier. The system is neatly packaged with a single IC — the LM1894.

Dynamic Noise

Dynamic noise reduction utilises three important facts for its functioning. The first is that noise caused in an audio channel by heating of resistive components in the circuitry (thermal noise) is distributed over the entire output bandwidth of the circuit (although its amplitude differs with signal frequency).

The second is that the total output noise level is proportional to the square root of the system bandwidth. So if the bandwidth is reduced, so is the total noise level at the output.

The third fact is known to anyone who has listened to a 'hissy' FM broadcast. Certain sounds seem to drown the noise and sound clearer. This is known as *auditory masking* and occurs due to the program sound stimulating the same regions of the ear as the noise and overshadowing the noise. It is

PARTS LIST

RESISTORS (all ¼W 5%)	
R1, 2	560R
RV1	1k0 vert. preset
CAPACITORS	
C1, 2, 6, 7, 8	1µ0 16V radial electrolytic
C3, 4	3900p polystyrene
C5	100µ polypropylene
C9	100µ 16V radial electrolytic
C10	100n ceramic
C11	1n0 polystyrene
C12	47n polystyrene
SEMICONDUCTORS	
IC1	LM1894
IC2	78L008
LED1	Red LED
LED2	Green LED
MISCELLANEOUS	
B1	PP3 battery
SK1-4	2 × Stereo 3.5mm jack socket or 4 × phono socket
SW1	SPST switch
SW2	DPDT switch

PCB or Stripboard. 14-pin IC socket. Case. Wire. Battery clip.

BUYLINES

The LM1894 is a relatively difficult IC to buy. It can be obtained from Macro Marketing (Tel: (06286) 4422) or from Thame Electronics (Tel: (084421) 4561).

1st CLASS

HOW IT WORKS

Figure 2 shows the full circuit diagram of the dynamic noise reduction system. Capacitors C1, 2 block any DC component of the input signal before it is passed to the variable low pass filters inside IC1.

These filters each consist of a variable transconductance amplifier followed by an op-amp configured as an integrator. C3,4 form the reactive feedback loop of this integrator and set the bandwidth permitted to 27Hz/µA of transconductance current. The transconductance itself is carried by the direct current provided by the control signal. The DC control signal therefore determines the amount of current supplied to the integrator and hence the bandwidth of the low pass filter.

The input signal is used to form the control signal. Both left and right channels pass to the inputs of the summing amplifier A1. The output of A1 is fed into a high pass filter with a cut-off frequency of 1.6kHz formed by C5 and RV1. As mentioned, this prevents low frequency, high amplitude sounds from fully opening the output bandwidth. RV1 also determines the amplitude of the control path signal and hence the width of the output bandwidth.

The high pass filter also serves to eliminate any low frequency signals which may amplitude-modulate the control path signal.

The control path signal is amplified by A2 and passed into the peak level detector. The detector can respond to a peak in the input signal of around 0.5ms. The time taken to respond to a peak (attack time) and then resettle (decay) is determined by C6.

C7 and C8 provide output coupling. IC2 is an 8V, 100mA regulator and together with C9 and C10 (to improve power supply rejection) forms an on board power supply to get a longer useful life from the battery.

Switch SW1 can be used to bypass the system when required. This is achieved by grounding the input of the peak level detector which causes the output bandwidth to fully open and let through input signal unaltered. A bypass is introduced in the control circuitry rather than the audio signal path to prevent switching noise and the unnecessary use of shielded cables to take the audio signal from its main path to the switch.

most prominent with high frequency sounds containing lots of harmonics.

This noise reduction system uses two low pass filters (one for each channel) to widen and narrow the system bandwidth in response to the input program signal (Fig. 1). The bandwidth is altered by controlling the cut off frequency of the low pass filters with a DC control signal derived from the program material's amplitude and frequency content.

Auditory masking is relied upon when the bandwidth is fully open to drown any noise — such a condition does not usually occur for too long during a piece of music or speech.

It must be appreciated that the circuit cannot respond immediately to a sudden change in program signal frequency and needs time to alter the cut off frequency of the bypass filters to allow the signal to pass through.

The LM1894 takes 0.5ms to adjust to this change. Fortunately the ear has difficulty responding to any distortion caused during this short change.

Note that only one control signal is used to control both left and right channel filters to maintain a stable stereo image. Note also that a high pass filter is included in the control path. This is to prevent low frequency, high amplitude sounds causing a high DC control signal to the filters and unnecessarily raising the cut-off frequency. This in turn would imply the bandwidth has been excessively widened and more noise can get through to the output. The high pass filter ensures the cut off frequency is just above the highest significant harmonic of the program material.

The output of the control path is not proportional to the input signal frequency. It is weighted to provide more noise reduction (greater control of signal amplitude) in the 2-10kHz band where the ear's sensitivity is greatest and noise most audible.

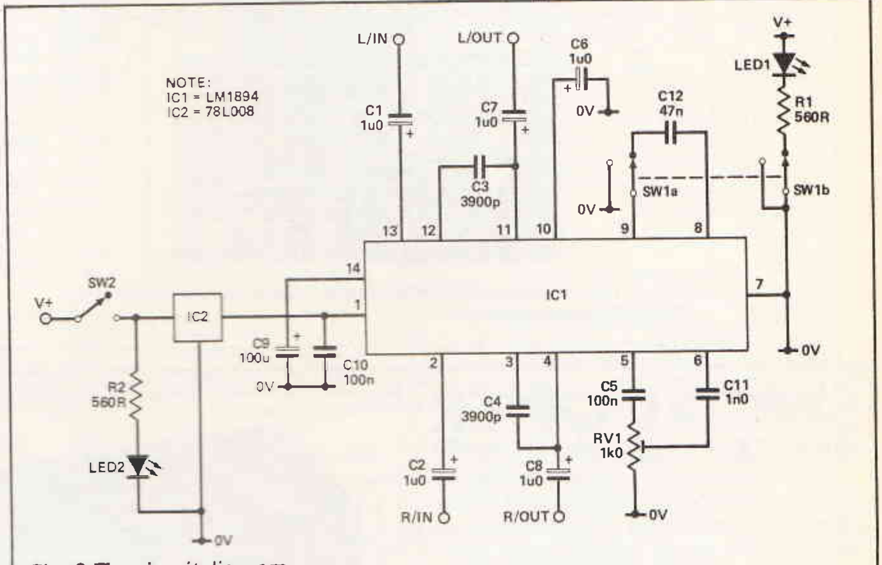


Fig. 2 The circuit diagram

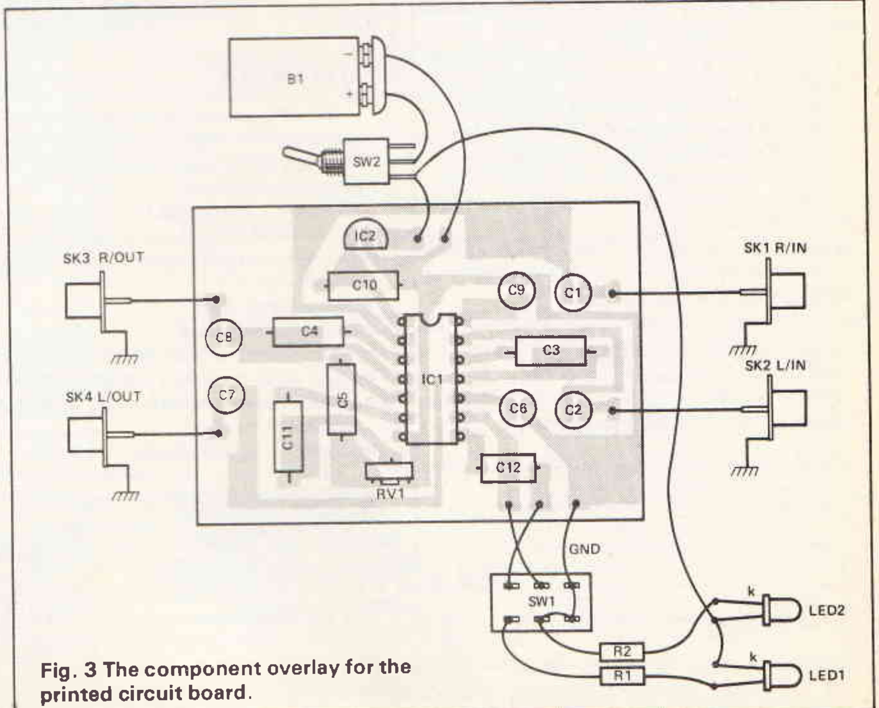


Fig. 3 The component overlay for the printed circuit board.

Construction

The noise reduction system can be built either on a PCB or using stripboard. Which you choose will depend on your expertise and your pocket.

The system is of a professional quality and so it does not pay to spare expenses. C3 and C4 should be polystyrene type capacitors while a polypropylene capacitor should be used for C5. Use the highest quality socket you can find for IC1.

Shielded, co-axial cables should be used to connect the input and output terminals to the signal source and amplifier. If the system is to be used in a stand alone configuration (not part of an audio system) stereo jacks should be used to take the audio signal to and from the circuit. Ordinary single core wires may be used to connect SW1 and the power supply to the circuit.

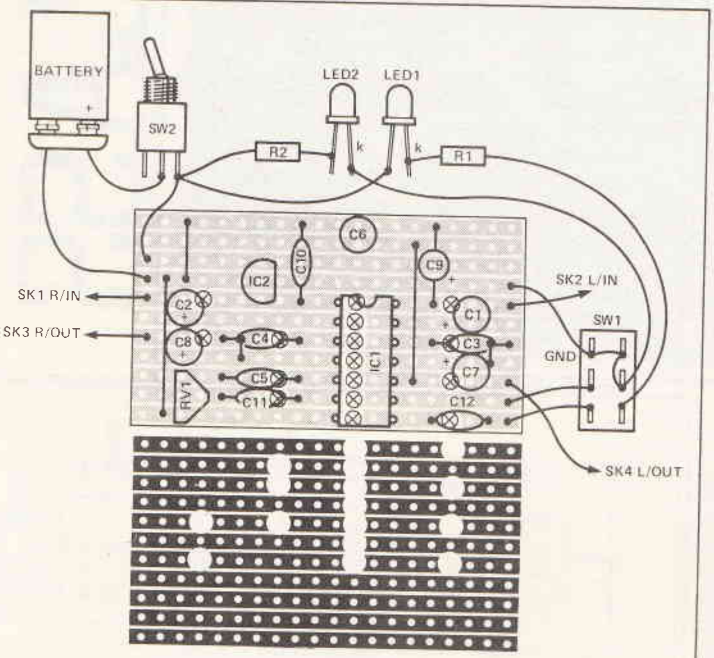


Fig. 4 The component overlay and track cut positions for the stripboard versions

Solder IC1's socket into the board first followed by the five wire links if you're working on stripboard. Next solder in all axial capacitors and cut off the excess leads. Checking polarity, solder IC2 followed by the electrolytic capacitors. Finally the shielded cables, battery and SW1 can be connected.

The PCB and a 9V battery will fit comfortably into a 125×50×25mm case. Use a metal case for shielding the circuit against radio interference.

The LEDs and their associated current limiting resistors (R1,2) are not essential and can be left out altogether.

Setting Up

Plug in a suitable signal source and amplifier. This project should be fitted between pre-amplifier and power amp. If you have an integrated amp the project can be connected into the auxiliary send/return loop like a graphics equaliser or even (at a pinch) between the cassette deck (the worst noise culprit) and the amp.

Switch on (SW2) and switch SW1 to the noise reduction position. RV1 should now be adjusted for the optimum noise reduction setting. Turning the preset clockwise will increase the amount of noise suppression.

Too much noise reduction will give a loss of high frequencies. The correct setting is a compromise and is best achieved by repeatedly switching the bypass in and out (SW1) as RV1 is adjusted to find the best setting for your system and your ears.

Although cassette systems are the worse noise offenders and stand to gain the most from this project, it will also perform well with tuners and even record decks as the sound source. ETI

VIRTUOSO POWER AMPLIFIER

Graham Nalty follows the regulation of his super-fi amplifier

I am sure it is not necessary to explain to ETI readers the sonic benefits of regulated power supplies in an high quality amplifier like the Virtuoso. The low current regulator here uses a very simple circuit modified to improve the sonic performance.

The basic circuit, probably familiar to many readers, is shown in Fig. 1. The output voltage is set by ZD1, Q2, R2 and R3.

It works like this.

If the voltage across the zener diode is 12V then the voltage at the base of Q2 is about 12.6V. Assuming the current through R2 and R3 is large compared with the base current of Q2, then R2 and R3 act as a voltage divider and the output voltage will be:

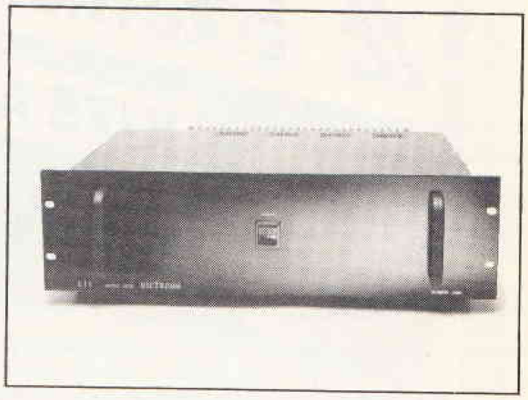
$$12.6 \times \frac{(R2 + R3)}{R3}$$

If the voltage falls, Q2 base current and collector current fall accordingly. This reduces the current through R1, thereby raising the voltage at the base of Q1 and hence restoring the output voltage.

If the output voltage rises, the current through Q2 increases and lowers the base voltage of Q1.

Better By Design

The power supply circuit is shown in Fig. 2. The design of the Virtuoso regulator is required first and foremost to achieve a good sonic performance.



For this reason, power transistors are used for all those transistors in which the dissipation varies with the voltage or current of the audio signal, even in the smallest way. They are also attached to a heatsink to ensure that temperature generated distortion is kept to an absolute minimum.

Another feature of the design is that apart from the reservoir capacitors, which are bypassed with plastic film capacitors for fast high frequency response, capacitors in the regulator circuit are kept to a minimum, and those that are used are of the highest quality (lowest loss factor).

In my experience low power zener diodes add distortion to the audio signal, so in the actual circuit the zener diode ZD1 of Fig. 1 is replaced by a transistor (Q11, Q12) and two resistors. Capacitors C11 and C12 are fitted to lower the

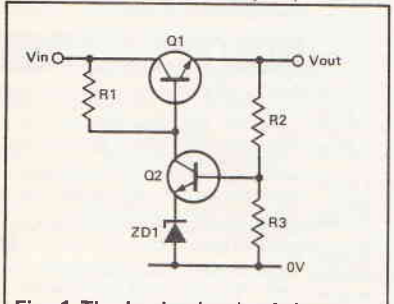


Fig. 1 The basic circuit of the regulated power supply

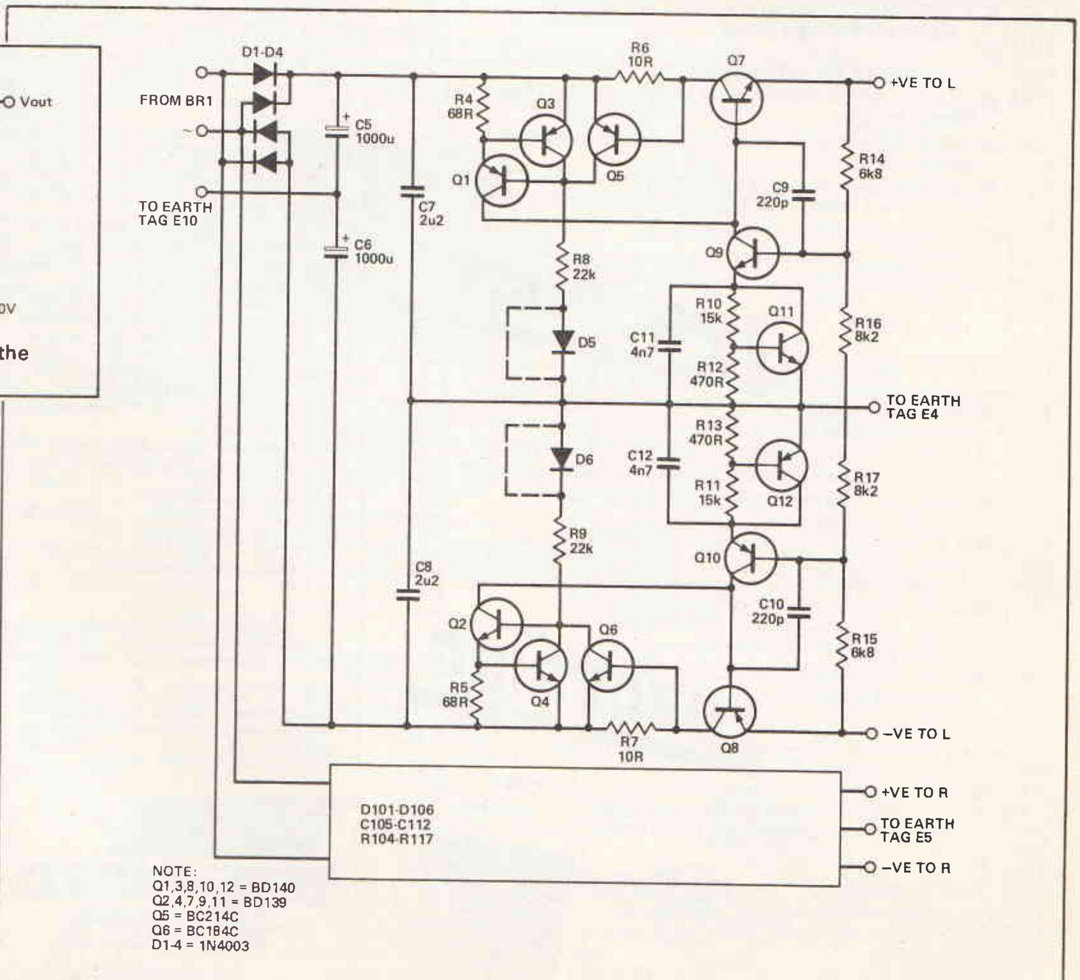


Fig. 2 Circuit diagram of the regulator board. The left channel is shown.

impedance of this circuit at high frequencies.

Another requirement for good sonic performance is low power supply ripple at the output. In the circuit of Fig 1, ripple voltages (due both to rectification and to variations in load current) at the input can be fed to the base of Q1 and the output ripple performance will not be too good. This can be improved considerably by replacing R1 with a constant current source.

In Fig 2, the constant current is provided by R4(R5), R8(R9), Q9(Q10) and Q11(Q12). This is a standard two transistor constant current source.

By adding constant current diodes D5 and D6 in series with R8 and R9 the impedance considerably increases, which raises the dynamic impedance of the current source feeding the regulator.

Current limiting is provided by Q5(Q6) and R6(R7). When the current limit of 60mA is reached, a voltage of 0.6V is reached across the base emitter junction of the transistor. This causes the transistor to conduct and to starve the base of Q11 of current.

In this way the current from the current source is reduced and the output voltage drops.

As the power dissipation of the series transistors is much greater than the power dissipated when the output is short circuited no further limiting is required.

C9 and C10 are fitted to maintain high frequency stability.

A Case Of Power

Two PCBs have been designed for the regulated power supply. For installation in the 2U case version a horizontal PCB is used, whilst a vertical PCB is used for the 3U case.

There are two major reasons for choosing to use a 3U case. Firstly it enables larger power supply components to be used in a mono bridged amplifier of around 200W to 400W rating into 8Ω.

Secondly the 3U version has been developed using much larger reservoir capacitors for the power supply to compensate for the effect that upgraded cables and passive components can have on the perceived balance between bass and treble instruments (better quality components allow more high frequency energy through while reducing lower resonances).

Other modifications on the 3U version include three bypass capacitors for each of the main reservoirs and the facility to use fast-recovery diodes on a heatsink for rectification.

The Ameliorated Amp

Before describing how to build the regulator, I want to say a few words about some of the special components used in the upgraded versions.

The Holco resistors listed are more expensive than standard metal film resistors, but when you consider how much you pay for metalwork and transformers in a big amplifier, the quality is well worth the cost. I have not suggested using bulk foil resistors, but that option is certainly open to constructors who want to get the absolute best performance.

Bypassing is used to speed up the response to all signals at all frequencies. The larger the capacitor the greater the inductance, and the more important it is to bypass it. That is why a high quality long life electrolytic capacitor is used as a bypass. The LCR EXFS/RP extended foil polystyrene capacitors were first used for the RIAA equalisation in the Virtuoso pre amplifier and have proved to be of the highest sonic quality.

The solder you use can affect your sound quality, and strong claims are made for an American solder called Wonder Solder. (Many manufacturers of very expensive interconnecting leads use it).

Construction

There is only one way to build the main power supply shown last month — slowly and carefully.

At the input side you are dealing with mains voltage, while the transformer secondaries have extremely high current capability and the reservoir capacitors will go bang very loudly if shorted.

The circuitry is easy but ensure you have checked and rechecked each connection, in particular the main input socket, the bridge rectifier connections, the earth connections and the reservoir capacitor polarity (a wrongly connected reservoir capacitor will give a low DC reading and gradually get warm, so can be detected before damage is done).

BUYLINES

All components that are not readily available from normal suppliers can be obtained from Audiokits, 6 Mill Close, Borrowash, Derby DE7 3GU. Tel: (0332) 674929.

PARTS LIST

Components X1, X2, X3 are used in the left channel of the board, components X101, X102, X103 in the right. Capacitors C7a, C7b refers to pairs of components used in the 3U version only.

	Standard	2U Upgraded	3U Bridgad
RESISTORS			
R4, 5, 104, 105	68R	68R1 Holco H8	68R1 Holco H8
R6, 7, 106, 107	10R	10R Holco H8	10R Holco H8
R8, 9, 108, 109	22K	22k1 Holco H8	22k1 Holco H8
R10, 11, 110, 111	15k	15k Holco H8	15k Holco H8
R12, 13, 112, 113	470R	475R Holco H8	475 Holco H8
R14, 15, 114, 115	5k6	5k62 Holco H8	5k62 Holco H8
R16, 17, 116, 117	6k8	6k81 Holco H8	6k81 Holco H8
CAPACITORS			
C5, 6, 105, 106	1000µ 63V radial	1000µ 63V radial	
C5a, 6a, 105a, 106a			4700µ 63V BHC ALS20A or 6800µ 63V LCR FAC114
C5b, 6b, 105b, 106b			100µ 63V Mullard 108
C7, 8, 107, 108	2µ2 MKC	3µ3 MKP	
C7a, 8a, 107a, 108a			4µ0 IAR Wonder Cap or 4µ7 Audiocap
C7b, 8b, 107b, 108b	10n 63V		LCR EXFS/RP
C9, 10, 109, 110	220p polystyrene	220p EXFS/RP	220p EXFS/RP
C11, 12, 111, 112	4n7 polystyrene	4n7 or 8n0 EXFS/RP	4n7 or 8n0 EXFS/RP
SEMICONDUCTORS			
Q1, 3, 8, 10, 12, 101, 103, 108, 110, 112	BD140	BD140-10	BD140-10 or selected BD244C
Q2, 4, 7, 9, 11, 102, 104, 107, 109, 111	BD139	BD139-10	BD139-10 or selected BD243C
Q5	BC214C	BC214C	BC214C
Q6	BC184C	BC184C	BC184C
D1-4, 101-104	1N4003	UF4003	BYW150 or MUR815
D5, 6, 105, 106	not used	J510	J510

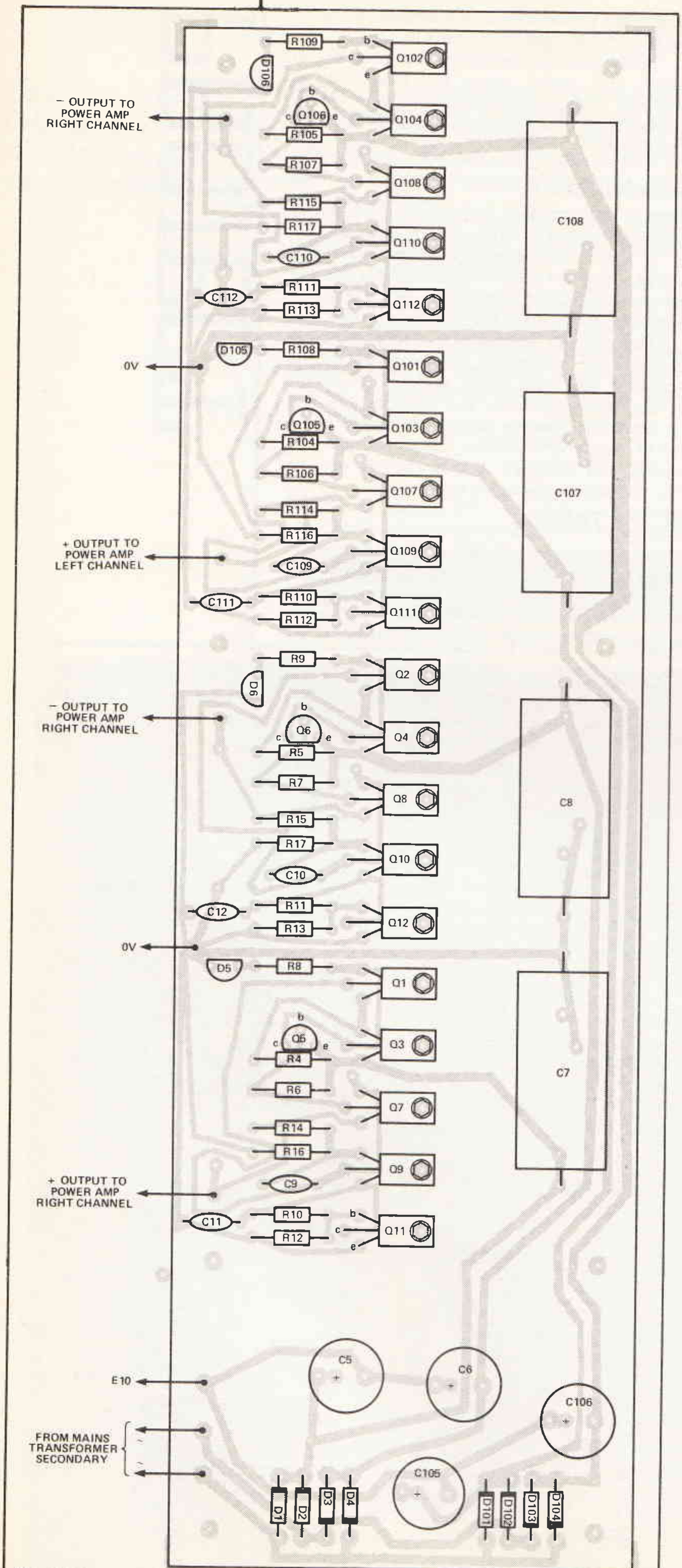


Fig. 3 Component overlay for 2U-version regulator board.

Building Regulation

Building the regulator boards is quite straightforward (the overlay diagrams are shown in Figs 3 and 4).

Components would be best installed in the order: resistors, small capacitors, diodes, small signal transistors, power transistors mounted on the heatsink, and finally the large capacitors.

Mount the resistors so that the colour codes or printed values (in the case of Holco resistors) can be easily read for error spotting.

Before testing the power supply and regulator you will need to make the AC connection from BR1 to the low current power supply as these and the leads from the mains transformer are attached to the same ¼in connector.

It is important to make sure the ends of these leads cannot short, and possibly the best way is to bolt the low current power supply PCB in place with the two relevant pins soldered on. The wires can then be attached to these pins.

It is always a wise precaution when testing new equipment to assume there is a short circuit at the input (just one wrongly connected diode could do precisely that). To this end I advise using a 22R to 100R carbon resistor in series with the supply before switching on.

Next check that the earths E4, 5 and 10 are connected to 0V.

Now switch on.

Each of the outputs should read +45V or –45V (or ±38V if you are using a 30V AC transformer and 4k75 for R16, 17, 116, 117).

Test Voltages

The DC voltage across each reservoir capacitor should read about 1½ times the rated AC voltage of the transformer secondary (±50V for a 35-0-35 transformer).

The voltages across the following components should all read 0.6V: R4, R5, R12, R13, Q7 base-emitter, Q8 emitter-base, Q11 emitter-base, Q12 base-emitter.

You should read 20 to 23V between Q13 and Q14 emitter to 0V. Across R16 and across R17 you should read 20.6 to 23.6V.

If you want to get the full output power from your amplifier, it is essential that the low current power supply is set to the maximum usable value. In practice when the mains is running low (5% below normal) the total voltage drop across the current regulator is not less than 2V. If the rectified DC reads 50V the regulator output should not be less than 45.5V.

The output voltage can be set by varying any of R10 to R17 but for convenience adjust the +ve supplies by varying R14, 114 and the -ve by R15, 115. The values shown in Parts List are carefully chosen but the optimum is affected by V_{be} and H_{fe} characteristics for Q11-14.

The output voltage can be calculated as:

$$V_o = V_{R16} \times \frac{(R14+R16)}{R16} + Q11I_b \times R14$$

where V_{R16} is the voltage across R16 and $Q11I_b$ is the base current of Q11 for a gain of 50.

$Q11I_b \times R14$ is typically about 1V.

I have purposely not used a preset here so that the sound quality will not be degraded. Changing resistor values is inconvenient but a small price to pay for quality.

So with your power ready and regulated, next month we can move on to examine the amplifier board that will complete the Virtuoso Power Amplifier.

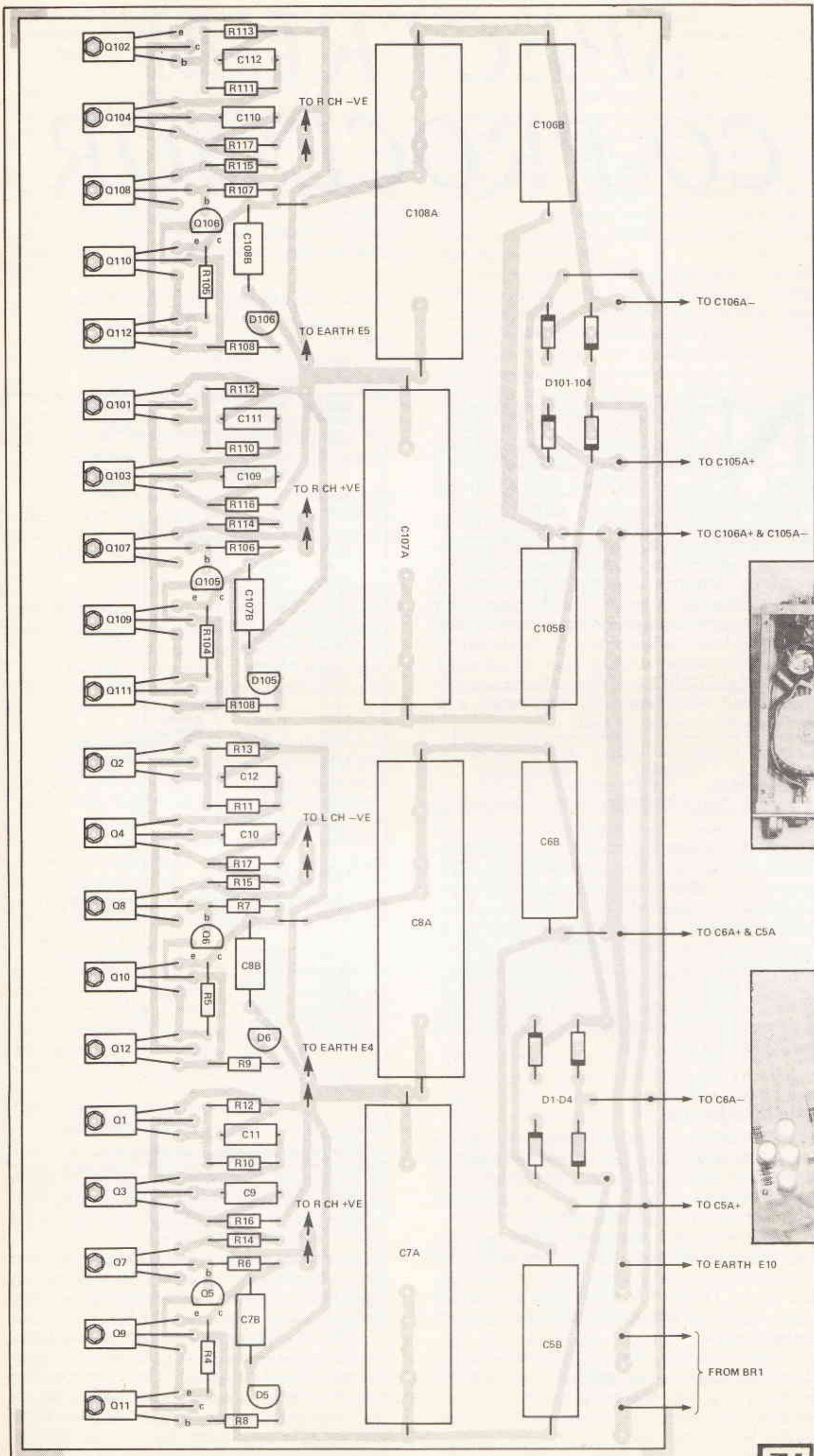
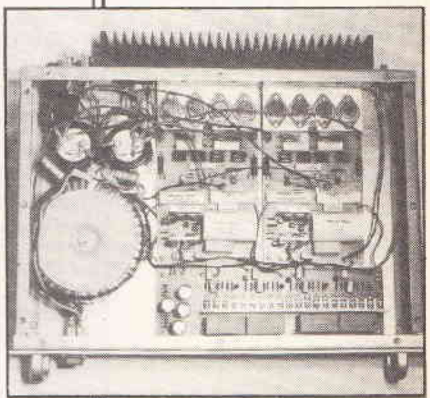
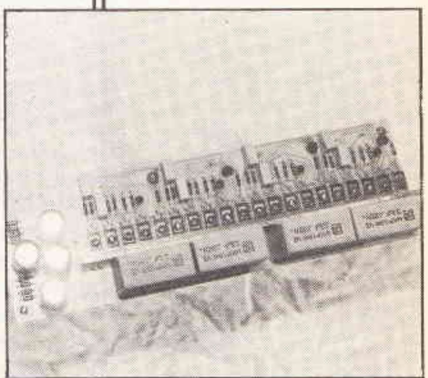


Fig. 4 Component overlay for 3U-version regulator board.





SPECTRUM CO-PROCESSOR

Graeme Durant rounds off his Spectrum's big brother with the operating system software and a look at putting it to work

Now the hardware is all assembled we should take a look at what actually happens in the co-processor, once it has received a valid command. Of course, this rather depends on what the command is.

When not executing commands, the co-processor is looping round a short routine, basically wasting time. When a command arrives, causing an interrupt to occur, the co-processor first disables its interrupt, thereby preventing other commands from interfering, and then copies the values from the four shared ports into four of its memory locations which form a command buffer called COM0-3, (see Fig 1). Having received a command, the co-processor must decode it to find out what it has to do next.

Self Test

If the command is decoded as Execute Self Test, the co-processor simply jumps off to execute this routine. Three tests are carried out on the system. The EPROM checksum is verified, the CPU scratchpad RAM is checked and the DRAM pages zero to seven are tested. The results of the self test are then encoded into two bytes and stored in two reserved RAM locations called TST0 and TST1 (see memory map) for subsequent examination.

The format of the results is shown in Fig 2. When the test is completed, the normal handshaking protocol described last month is used to return control to the host.

Block Moves

If the command is a block read or write, then a whole new handshaking scheme is entered, nested within the main command protocol outlined last month. The format of the block move command from the Spectrum is shown in Fig. 3.

The block move command makes use of all four shared registers at the same time. For the sake of clarity, we shall refer to the shared ports by the names TX0 to TX3 when they are used as output ports and RX0 to RX3 when they are used as input ports.

Looking at the command 'packet' above, port TX3 holds the command itself (block read or write) in its top four bits, with bit D7 set to force a co-processor interrupt. The required memory page (0-7) is held in the lower four bits of port TX3.

Port TX2 and TX1 hold the starting address within the selected page, from which the block move will begin. Port TX0 holds a number between 0 and 255, which represents the length of the block to be moved, in pairs of bytes. Note that in this case, 0 represents 256, and not zero!

Once the command packet has been received by the co-processor, the data starts to be moved. Again all four ports are used together to move two bytes of data at a time from the block.

The handshaking scheme repeatedly transfers these 'packets' of data until the entire block has been moved over the interface. The format of the block-move data packet from either the co-processor or the Spectrum is shown in Fig 4. Ports TX0 and TX1 hold the two data bytes themselves. Port TX3 holds a constant pre-defined label which identifies the information as a data packet. The

Address (hex)	Contents		Memory type
FFFF	For user's own applications		Main paged Dynamic RAM
:			
:			
1400			
13FF	For user's own applications		Scratchpad RAM on CPU card
:			
:			
1123			
1122	I reg	Z80 register shadows	
1121	IY hi byte		
1120	IY lo byte		
111F	IX hi byte		
111E	IX lo byte		
111D	H' reg		
111C	L' reg		
111B	D' reg		
111A	E' reg		
1119	B' reg		
1118	C' reg		
1117	A' reg		
1116	F' reg		
1115	H reg		
1114	L reg		
1113	D reg		
1112	E reg		
1111	B reg		
1110	C reg		
110F	A reg		
110E	F reg		
:			
110A	USECOM User command vect.		
110B	(110Bh = MS byte)		
1109	CODEXE Code running flag		NB Unlabelled areas of the scratchpad RAM are used by the co-processor for housekeeping functions.
:			
1105	TST1	Self test status	
1104	TSTO		
1103	COM3	Command buffer	
1102	COM2		
1101	COM1		
1100	COMO		
10FF	Top of Stack		
:			
:	V stack		
1000			
0FFF			Operating software EPROM
:			
:			
0000			

Fig. 1 The co-processor memory map

actual values of this label in the Spectrum and co-processor data packets were given last month.

Port TX2 holds a 'packet count,' termed the Datacount, which starts at zero and is incremented by one as each packet is sent. This value is used as the basis for the block-move handshaking protocol illustrated in Fig. 5.

As mentioned before, the handshaking involved in transferring the block-move command to the co-processor is exactly the same as the normal process described last month. The data movement itself is embedded into the section reserved for 'processing' in the command handshake scheme.

Regardless of whether a block read or write is taking place, the first part of the protocol is identical. The Spectrum sends the command packet described above to the co-processor, thus forcing an interrupt. Note that the contents of TX0-2 should be sent by the Spectrum before TX3, so that once the co-processor is interrupted all the command information is present and valid. This applies any time the command information consists of more than just port TX3.

The Spectrum then waits for a response from the co-processor, this time in the form of the DATA label in port RX3, signifying the start of a data block move.

Once the co-processor has received and decoded the command packet as a block move, it clears its Datacount port TX2, such that the value there is neither one nor zero. The basis for the data move handshake protocol is one of waiting for a Datacount value from the other processor, which is one greater than the last.

Once received, this signifies a readiness for data transfer. The very first value expected, signalling that data is ready or data is required, is either zero or one, depending on the direction of transfer in operation. Obviously, if the handshake port initially contains this expected value before the transfer is possible (as a result of a previous and unconnected command sequence) then an erroneous transfer will result. The initialisation of the contents of port TX2 avoids such a condition.

After port TX2 has been cleared, the DATA label is sent as an acknowledgement to the Spectrum that the command was received and understood. Then after the co-processor's Datacount variable has been initialised to zero, the co-processor waits for the Spectrum to signal its own readiness for entry line into the actual block-move routine. The Spectrum does this by sending a DATA label to co-processor port RX3.

Once the Spectrum receives the DATA label from the co-processor, it also goes on to clear its Datacount port TX2 for exactly the reason outlined above. Then the command interrupt is removed from the co-processor by sending a DATA label to the co-processor via port TX3.

This DATA label is an 8-bit value with its MS bit zero and also serves to tell the co-processor that the Spectrum is now ready to move data. Finally, before the data move routine itself is entered, the Spectrum Datacount variable is initialised to zero, as in the co-processor.

The data move routine is now started. It is from this point that the block read and block write schemes differ. However, the 'transmit' routine in the co-processor for block read is identical in operation (if not in implementation) to the 'transmit' routine in the Spectrum for block write. Similarly for the 'receive' routines.

We shall now look at the generalised transmit and receive routines in more detail.

The transmitting processor sends the next two bytes (initially the first two bytes) of data to the receiving processor via ports TX0 and 1. The current Datacount value (initially zero) is then written into port TX2 by the transmitter to signify to the receiver that data is now available for transfer. The transmitter increments its Datacount value and awaits this new incremented value from the receiver in port RX2 to show that the data has been collected.

Meanwhile the receiving processor reads port RX2 repeatedly until it contains its current Datacount (initially zero) and then reads the data stored in ports RX0 and 1, putting it into the appropriate memory locations. The receiver's Datacount is then incremented and sent to the transmitter via port TX2 to acknowledge the fact the data has been read. This newly incremented receiver datacount (and indeed the corresponding datacount value in the transmitter) now represents the number of data byte pairs transferred.

In both the receiver and the transmitter, these Datacounts are compared to the originally stated blocklength value from the Spectrum's command, to see if the block move has been completed. If the Datacounts are still less than the blocklength, then both the transmitting and the receiving routines loop back to transfer the next two data bytes.

If however the datacounts are equal to the blocklength, the most recently transferred byte pair was the last. The normal command handshake routine then takes over to complete the process, before a new command can be executed.

Location TST0 — DRAM page status

D7	D6	D5	D4	D3	D2	D1	D0	1=page OK
PGE7	PGE6	PGE5	PGE4	PGE3	PGE2	PGE1	PGE0	0=page fail

Location TST1 — EPROM/scratchpad status

D7	D6	D5	D4	D3	D2	D1	D0	&F=OK
EPROM test				Scratchpad test				&0=fail

Fig. 2 Self test results format

Port TX0	Port TX1	Port TX2	Port TX3 D7 . . . D0
Block length (byte pairs)	Start address LS byte	Start address MS byte	Command Mempage 0-7

Fig. 3 Block move command format

Port TX0	Port TX1	Port TX2	Port TX3
(n)th Data Byte	(n+1)th Data Byte	Datacount (Byte pairs)	DATA label

Fig. 4 Data packet format

Executing User Code

The other two commands left to look at in detail are the User Code Execution command and its associated Break from execution command. These also work within the 'processing' sections of the command handshake scheme but do not require the elaborate specialised handshaking that the block moves use. The scheme used is shown in Fig. 6, along with the format of the command packet from the Spectrum.

PROJECT

```
1 REM      INTERACTIVE Z80
2 REM DEVELOPMENT SYSTEM FOR
3 REM     USE WITH THE ETI
4 REM  SPECTRUM COPROCESSOR
5 REM
6 REM   G. Durant  1988
7 REM
8 REM        version 1.0
9 REM
10 REM Reserve space for code
12 CLEAR 47999
14 REM Set up screen colours
16 BORDER 0: PAPER 0: INK 7: CLS
18 REM Initialise constants
20 REM 1. Shared ports
22 LET tx0=159: LET tx1=191: LET tx2=223: LET tx3=255: LET rx0=159: LET rx1=191: LET rx2=223: LET rx3=255
24 REM 2. Labels from Co-proc
26 LET inval=224: LET idle=127: LET brkack=240: LET datid=254: LET busy=255
28 REM 3. Opcodes from                Spectrum
30 LET null=127: LET sdata=126: LET break=240: LET selftest=224: LET codeexec=192: LET blockwr=128: LET blockrd=160
32 REM Initialise ports
34 OUT tx0,0: OUT tx1,0: OUT tx2,0: OUT tx3,null
36 REM Dec to Hex conversion
38 DEF FN h$(n)="0123456789ABCDEF"(1+INT (n/16))+"0123456789ABCDEF"(1+n-16*INT (n/16))
40 REM Wait until Coproc idle
42 IF IN rx3<>idle THEN  CLS : PRINT "COPROCESSOR IS BUSY.          Host waiting for coprocessor to idle."
44 IF IN rx3<>idle THEN  GO TO 44
46 IF IN rx3<>idle THEN  GO TO 44
48 REM
50 REM ****************
52 REM Main menu options
54 REM ****************
56 REM
58 REM Option screen
60 CLS
62 PRINT AT 0,0;"Interactive Z80 Development tool";AT 2,0;"Menu options"
64 PRINT AT 5,0;"1. Load code/data into Spectrum from tape";AT 8,0;"2. Load code/data from Spectrum into Co-processor";AT 11,0;"3. Display Co-processor memory      contents";AT 14,0;"4. Execute user code in        Co-processor";AT 17,0;"5. Execute Co-processor       self test";AT 20,0; FLASH 1;">"; FLASH 0;"Select required option"
66 REM Wait for user selection
68 LET a$=INKEY$: IF IN rx3<>idle THEN  GO TO 40
70 IF a$="" THEN  GO TO 68
72 REM Go to selected routine
74 IF a$<"1" OR a$>"5" THEN  GO TO 68
76 LET option=VAL a$: CLS
78 GO TO (option*100)+100
80 REM
200 REM **********************
202 REM Load code into Spectrum
204 REM **********************
206 PRINT "Load code/data from Tape into   Spectrum reserved memory"
208 INPUT "What is the name of the file to be loaded? "; LINE f$
210 CLS
212 REM Ensure valid filename
214 IF LEN f$>10 THEN  PRINT "Invalid filename, try again": GO TO 208
216 REM Load data
218 LOAD f$CODE 48000
220 REM Return to menu
222 GO TO 40
224 REM
300 REM **********************
302 REM Move data into Co-proc
304 REM **********************
306 REM
308 PRINT "Move code/data into Co-processor": PRINT
310 REM Init address pointer
312 LET addpntr=48000
314 REM Get user start address
316 GO SUB 1000
318 REM Get user block length
320 GO SUB 2000
322 REM Handle block >= 512
324 IF blocklength>=256 THEN  LET blocklength=blocklength-256: LET blength=0: GO TO 330
326 REM Handle block < 512
328 LET blength=blocklength: LET blocklength=0
330 REM Send command to coproc
332 OUT tx0,blength: OUT tx1,lbyte: OUT tx2,hbyte: OUT tx3,mempage+blockwr
334 REM Wait for DATA label
336 IF IN rx3<>datid THEN  GO TO 336
338 IF IN rx3<>datid THEN  GO TO 336
340 REM Ensure tx2 <> 0,              send DATA label            and remove interrupt
342 OUT tx2,sdata: OUT tx3,sdata
344 REM Init datacount
346 LET datacount=0
348 REM Send two bytes of data            and current datacount
350 OUT tx0,PEEK addpntr
352 LET addpntr=addpntr+1
354 OUT tx1,PEEK addpntr: OUT tx2,datacount
356 REM Point to next data
358 LET addpntr=addpntr+1: LET datacount=datacount+1: IF datacount=256 THEN  LET datacount=0
360 REM Wait for datacount              from coproc
362 IF IN rx2<>datacount THEN  GO TO 362
364 IF IN rx2<>datacount THEN  GO TO 362
366 REM Repeat if not end
368 IF datacount<>blength THEN  GO TO 348
370 REM Remove data label and          wait for coproc idle
372 OUT tx3,null
374 IF IN rx3<>idle THEN  GO TO 374
376 IF IN rx3<>idle THEN  GO TO 374
378 REM Next block unless last
380 IF blocklength>0 THEN  LET hbyte=INT ((addpntr-48000+start)/256): LET lbyte=addpntr-48000+start-(hbyte*256): GO TO 322
382 REM Return to menu
384 GO TO 40
386 REM
400 REM **********************
402 REM Display Co-proc memory
404 REM **********************
406 REM
408 PRINT "Display code/data on screen": PRINT
410 REM Get user start address
412 GO SUB 1000
414 REM Init address pointer
416 LET addpntr=start
418 REM Get user block length
420 GO SUB 2000
422 REM Tabulate data for               display formatting            only
424 PRINT "Memory page    : ";mempage: PRINT "Start address : ";start: PRINT ': IF lbyte<>8*INT (lbyte/8) THEN  PRINT TAB 8+3*(lbyte-8*INT (lbyte/8));
426 REM Handle block >= 512
428 IF blocklength>=256 THEN  LET blocklength=blocklength-256: LET blength=0: GO TO 434
430 REM Handle block < 512
432 LET blength=blocklength: LET blocklength=0
434 REM Send command to coproc
436 OUT tx0,blength: OUT tx1,lbyte: OUT tx2,hbyte: OUT tx3,mempage+blockrd
438 REM Wait for DATA label
440 IF IN rx3<>datid THEN  GO TO 440
442 IF IN rx3<>datid THEN  GO TO 440
444 REM Ensure tx2 <> 1,              send DATA label            and remove interrupt
446 OUT tx2,sdata: OUT tx3,sdata
448 REM Init datacount
450 LET datacount=0
452 REM Wait for datacount              from coproc
454 IF IN rx2<>datacount THEN  GO TO 454
456 IF IN rx2<>datacount THEN  GO TO 454
458 REM Display valid data              and insert address           every eight bytes
460 IF addpntr/8=INT (addpntr/8) THEN  PRINT TAB 6-LEN (STR$ addpntr);addpntr;TAB 8;
462 PRINT " ";FN h$(IN rx0);: LET addpntr=addpntr+1
464 IF addpntr/8=INT (addpntr/8) THEN  PRINT TAB 6-LEN (STR$ addpntr);addpntr;TAB 8;
466 PRINT " ";FN h$(IN rx1);
468 REM Point to next data
470 LET datacount=datacount+1: LET addpntr=addpntr+1: IF datacount=256 THEN  LET datacount=0
472 REM Send current datacount
474 OUT tx2,datacount
476 REM Repeat if not end
478 IF datacount<>blength THEN  GO TO 452
480 REM Wait for coproc idle
482 IF IN rx3<>idle THEN  GO TO 482
484 IF IN rx3<>idle THEN  GO TO 482
486 REM Next block unless last
488 IF blocklength>0 THEN  LET hbyte=INT (addpntr/256): LET lbyte=addpntr-(hbyte*256): GO TO 426
490 REM Return to menu
492 PRINT '': PRINT AT 21,0;"Press any key to return to menu": PAUSE 0: GO TO 40
494 REM
500 REM **********************
502 REM Execute code in Co-proc
504 REM **********************
506 REM
508 PRINT "Execute user code in            Co-processor"
510 REM Get user start address
512 GO SUB 1000
514 REM Send command
516 OUT tx1,lbyte: OUT tx2,hbyte
518 OUT tx3,(mempage+codeexec)
520 REM Wait for BUSY label
522 IF IN rx3<>busy THEN  GO TO 522
524 IF IN rx3<>busy THEN  GO TO 522
526 REM Remove interrupt
528 OUT tx3,null
530 REM Code is now executing
532 CLS : PRINT "User code is now executing in   the Co-processor.               PRESS 'B' TO BREAK"
534 REM Wait for IDLE or user           break
536 LET a$=INKEY$
538 IF a$<>"b" AND IN rx3<>idle THEN  GO TO 536
540 IF a$<>"b" AND IN rx3<>idle THEN  GO TO 536
542 REM Handle break
544 IF a$="b" AND IN rx3<>idle THEN  GO SUB 3000
546 REM Return to menu
548 GO TO 40
550 REM
600 REM ********************
602 REM Run Co-proc selftest
604 REM ********************
606 REM
608 PRINT "Executing Coprocessor self test": PRINT
610 REM Send command
612 OUT tx3,selftest
614 REM Wait for BUSY label
616 IF IN rx3<>busy THEN  GO TO 616
618 IF IN rx3<>busy THEN  GO TO 616
620 REM Remove interrupt
622 OUT tx3,null
624 REM Wait for IDLE signal
626 IF IN rx3<>idle THEN  GO TO 626
628 IF IN rx3<>idle THEN  GO TO 626
630 REM Display results of test         Do block move of status
632 REM
634 REM Send command
636 OUT tx0,1: OUT tx1,4: OUT tx2,17: OUT tx3,blockrd
638 REM Wait for DATA label
640 IF IN rx3<>datid THEN  GO TO 640
642 IF IN rx3<>datid THEN  GO TO 640
644 REM Ensure tx2 <> 1,              send DATA label            and remove interrupt
646 OUT tx2,sdata: OUT tx3,sdata
648 REM Wait for Datacount
650 IF IN rx2<>0 THEN  GO TO 650
652 IF IN rx2<>0 THEN  GO TO 650
654 REM Process EPROM and sRAM          status and display            results
656 CLS : PRINT "Results of Self test": PRINT ': IF IN rx1=255 OR IN rx1=240 THEN  PRINT "EPROM checksum passed": PRINT '
658 IF IN rx1=255 OR IN rx1=15 THEN  PRINT "Onboard co-processor RAM passed": PRINT '
660 REM Scan page status byte           and display results
662 LET status=IN rx0: FOR b=7 TO 0 STEP -1: PRINT "DRAM Page ";b;" ";("passed" AND status>=2^b)+("failed" AND status<2^b): IF status>=2^b THEN  LET status=status-2^b
664 NEXT b
666 REM Complete handshaking
668 REM
670 REM Send new datacount
672 OUT tx2,1
674 REM Wait for IDLE
676 IF IN rx3<>idle THEN  GO TO 676
678 IF IN rx3<>idle THEN  GO TO 676
680 REM Return to menu
682 PRINT AT 21,0;"Press any key to return to menu": PAUSE 0: GO TO 40
684 REM
1000 REM ********************
1002 REM Input of Start address
1004 REM ********************
1006 REM
1008 INPUT "Select the required memory page in the Co-processor ";mempage
1010 REM Ensure valid input
1012 IF mempage<0 OR mempage>7 OR mempage<>INT (mempage) THEN  CLS : PRINT "Invalid memory page, try again": PRINT ': GO TO 1008
1014 INPUT "Select the required starting    address in the Co-processor ";start
1016 REM Ensure valid input
1018 IF start<0 OR start>65534 OR start<>INT (start) THEN  CLS : PRINT "Invalid start address, try again": PRINT ': GO TO 1014
1020 REM Convert address to high        and low bytes
1022 LET hbyte=INT (start/256): LET lbyte=start-(hbyte*256)
1024 RETURN
1026 REM
2000 REM ********************
2002 REM Input of block length
2004 REM ********************
2006 REM
2008 INPUT "Select the length of data block to be moved (2 to 16k bytes) ";blocklength
2010 REM Ensure valid input
2012 IF blocklength<2 OR blocklength>16384 OR blocklength<>INT (blocklength) THEN  CLS : PRINT "Invalid block length, try again": PRINT ': GO TO 2008
2014 REM Ensure length is even
2016 IF blocklength/2<>INT (blocklength/2) THEN  LET blocklength=blocklength+1
2018 REM Handle page overflow
2020 IF start+blocklength>65536 THEN  PRINT "WARNING : Page will overflow.    Block length will be reduced to avoid wrapround": PRINT ': LET blocklength=65536-start
2022 REM Convert length for byte        pairs
2024 LET blocklength=blocklength/2
2026 RETURN
2028 REM
3000 REM ********************
3002 REM User code break routine
3004 REM ********************
3006 REM
3008 REM Send BREAK command
3010 OUT tx3,break
3012 REM Wait for acknowledge
3014 IF IN rx3<>brkack THEN  GO TO 3014
3016 IF IN rx3<>brkack THEN  GO TO 3014
3018 REM Remove interrupt
3020 OUT tx3,null
3022 REM Wait for IDLE signal
3024 IF IN rx3<>idle THEN  GO TO 3024
3026 IF IN rx3<>idle THEN  GO TO 3024
3028 RETURN
```

Listing 1 Spectrum Basic Example program

PROJECT

On receiving a command from the Spectrum, the co-processor first disables its interrupt as described previously. Then, before it decodes the new command, the co-processor checks an internal flag called the Code Executing flag, to see if user code was being run when this command was received. This flag is an 8-bit value stored in a co-processor memory location (CODEXE) and takes the value of either the BUSY label when user code begins execution or the IDLE label when user code stops execution.

If code is not currently being executed, the command received is interpreted as usual. If this command is User Code Execute, then the co-processor sends the BUSY label to the Spectrum via port TX3 and sets the code executing flag to BUSY. The co-processor then waits for the Spectrum to respond by removing the initial command interrupt. This response is simply part of the standard command handshaking protocol described last month.

Once this occurs the co-processor is free to re-enable its interrupt, ready to detect a possible Break command later. Note that this is the only time that the co-processor enables its interrupt whilst a command is being executed. Once all this has happened, the user code can be executed. It is 'called' exactly like a subroutine, so the return address is stored on the co-processor stack for use later.

At the end of the user code itself, there must be a Z80 *return from subroutine* (RET) instruction. When this is encountered, as long as the co-processor stack is still intact, system control will return to the code execute routine in the co-processor EPROM. The co-processor interrupt will be disabled again, so Break and other spurious commands will have no effect now.

Next, a co-processor routine copies the current values held in all the Z80 registers into reserved memory locations for later examination (see Fig 1).

This feature is particularly useful when debugging assembly code running on the co-processor. These register values can be subsequently examined by using a block read into the Spectrum. Once the registers have been dumped into memory, the code executing flag CODEXE is reset to IDLE as code is no longer running. Finally the normal handshake protocol takes over to complete the process before the interrupt is again re-enabled in readiness for a new command.

If the code executing flag has been previously set to BUSY (code running) when a command is received, the co-processor expects to have received a Break command from the Spectrum.

If the command is not Break, an invalid command has been sent and user code execution should be continued. To achieve this, the co-processor sends the INVALID flag to the Spectrum via port TX3. It then waits for the host to remove the interrupting command — the response normally expected in the command handshake protocol.

Meanwhile, if the Spectrum receives an INVALID flag via its port RX3, it must remove the erroneous interrupt and await the normal IDLE flag before sending a command other than Break.

When the co-processor sees that the interrupt has been removed, it sets up the same conditions which existed before the invalid command was received. The BUSY label is sent to the host via port TX3. The interrupt is enabled. Finally, the co-processor returns to execute the user code from the point at which it was interrupted until either a RET instruction is encountered in the code itself or a valid Break

```
0000  F3 ED 56 C3 00 01 00 00 FB E9 00 00 00 00 00 00
0010  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0020  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0030  00 00 00 00 00 00 00 00 F3 F5 DB 9F 32 00 11 DB
0040  BF 32 01 11 DB DF 32 02 11 DB FF 32 03 11 C3 00
0050  02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0060  00 00 00 00 00 00 2A 0C 11 E9 00 00 00 00 00 00
0070  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0080  DB FF E6 80 20 FA 3E 7F D3 FF 32 08 11 C9 00 00

0100  31 FF 10 3E FF D3 FE 3E 00 D3 9F D3 BF D3 DF 3E
0110  FF D3 FF 18 0B 00 00 00 00 00 00 00 00 00 00 00
0120  21 00 00 3E 00 11 00 00 01 FF 0F 86 ED A0 EA 2B
0130  01 21 FF 0F BE 28 06 DD 21 00 00 18 04 DD 21 F0
0140  00 21 00 10 36 FF 3E FF 01 FF 03 11 01 10 ED B0
0150  21 00 10 01 00 04 ED A1 20 1E EA 56 01 FE 00 28
0160  09 21 00 10 36 00 3E 00 18 DE DD 22 05 11 3A 05
0170  11 F6 0F 32 05 11 18 04 DD 22 05 11 3E FF ED 47
0180  D3 FE 3E FF 21 00 14 36 FF 01 FF EB 11 01 14 ED
0190  B0 21 00 14 01 00 EC ED A1 20 21 EA 97 01 FE 00
01A0  28 09 21 00 14 36 00 3E 00 18 DE 3A 04 11 37 1F
01B0  32 04 11 ED 57 3D FE F7 20 C4 18 0A 3A 04 11 CB
01C0  3F 32 04 11 18 ED 3E FF D3 FE 2F ED 47 21 30 02
01D0  22 0A 11 3E 7F 32 09 11 CD 80 00 FB 18 FD 00 00
01E0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
01F0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0200  3A 09 11 FE FF 28 35 F1 3A 03 11 CB 7F 28 21 E6
0210  50 CA AD 02 3A 03 11 E6 F0 FE C0 28 5B 3A 03 11
0220  FE E0 CA 00 01 3A 03 11 FE F0 28 04 2A 0A 11 E9
0230  3E E0 32 08 11 D3 FF CD 80 00 ED 4D 3A 03 11 FE
0240  F0 20 1D 3E F0 32 08 11 D3 FF F1 CD 00 04 3E 7F
0250  32 09 11 31 FF 10 3E FF D3 FE CD 80 00 C3 DB 01
0260  3E E0 32 08 11 D3 FF DB FF E6 80 20 FA 3E FF 32
0270  08 11 D3 FF F1 FB ED 4D 3E FF 32 08 11 D3 FF 32
0280  09 11 3A 03 11 E6 07 2F D3 FE DB FF E6 80 20 FA
0290  3A 02 11 67 3A 01 11 6F CF F3 ED 56 CD 00 04 3E
02A0  7F 32 09 11 3E FF D3 FE CD 80 00 ED 4D 3E 7F D3
02B0  DF 3E FE 32 08 11 D3 FF 3A 03 11 E6 07 2F D3 FE
02C0  3A 01 11 6F 3A 02 11 67 06 00 DB FF F6 80 FE FE
02D0  20 FB DB FF F6 80 FE FE 20 F0 3A 03 11 CB 6F 28
02E0  2C 7E D3 9F 23 7E D3 BF 78 D3 DF 04 23 DB DF B8
02F0  20 FB DB DF B8 20 F6 3A 00 11 B8 20 E4 3E FF 32
0300  08 11 D3 FF 3E FF D3 FE CD 80 00 ED 4D DB DF B8
0310  20 FB DB DF B8 20 F6 DB 9F 77 23 DB BF 77 23 04
0320  78 D3 DF 3A 00 11 B8 20 E4 3E FF D3 FE CD 80 00
0330  ED 4D 00 00 00 00 00 00 00 00 00 00 00 00 00 00

0400  ED 43 10 11 ED 53 12 11 22 14 11 F5 C1 ED 43 0E
0410  11 D9 ED 43 18 11 ED 53 1A 11 22 1C 11 D9 08 F5
0420  C1 ED 43 16 11 08 DD 22 1E 11 FD 22 20 11 ED 57
0430  32 22 11 C9 00 00 00 00 00 00 00 00 00 00 00 00

0FF0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 BD
```

Listing 2 Hex dump of the Co-processor EPROM

command is received.

If the command received whilst code was executing is the correct Break code then the co-processor sends a Break Acknowledge flag (BRKACK) via port TX3 to the host. Again, the Z80 registers are dumped into reserved memory for later examination and the code executing flag is set to IDLE. Now the co-processor stack is purged (user code may have made use of the stack and so stopping execution midstream leaves it in an unpredictable state).

Meanwhile, on receiving the BRKACK flag from the co-processor, the Spectrum removes its interrupt according to the standard command handshake protocol. Then this protocol takes over at both ends of the interface to complete the process before a new command is sent to the co-processor.

New Commands

Having now looked in some detail at the five commands which can be accepted by the co-processor, a word or two about extending this capability.

If the co-processor receives a command not defined in its interpreter, its operating software jumps off to execute code pointed to by the contents of the reserved memory location called USECOM (see Fig 1).

During initialisation, the co-processor puts a default value into USECOM. If left unchanged, unlisted commands call a routine in the EPROM to

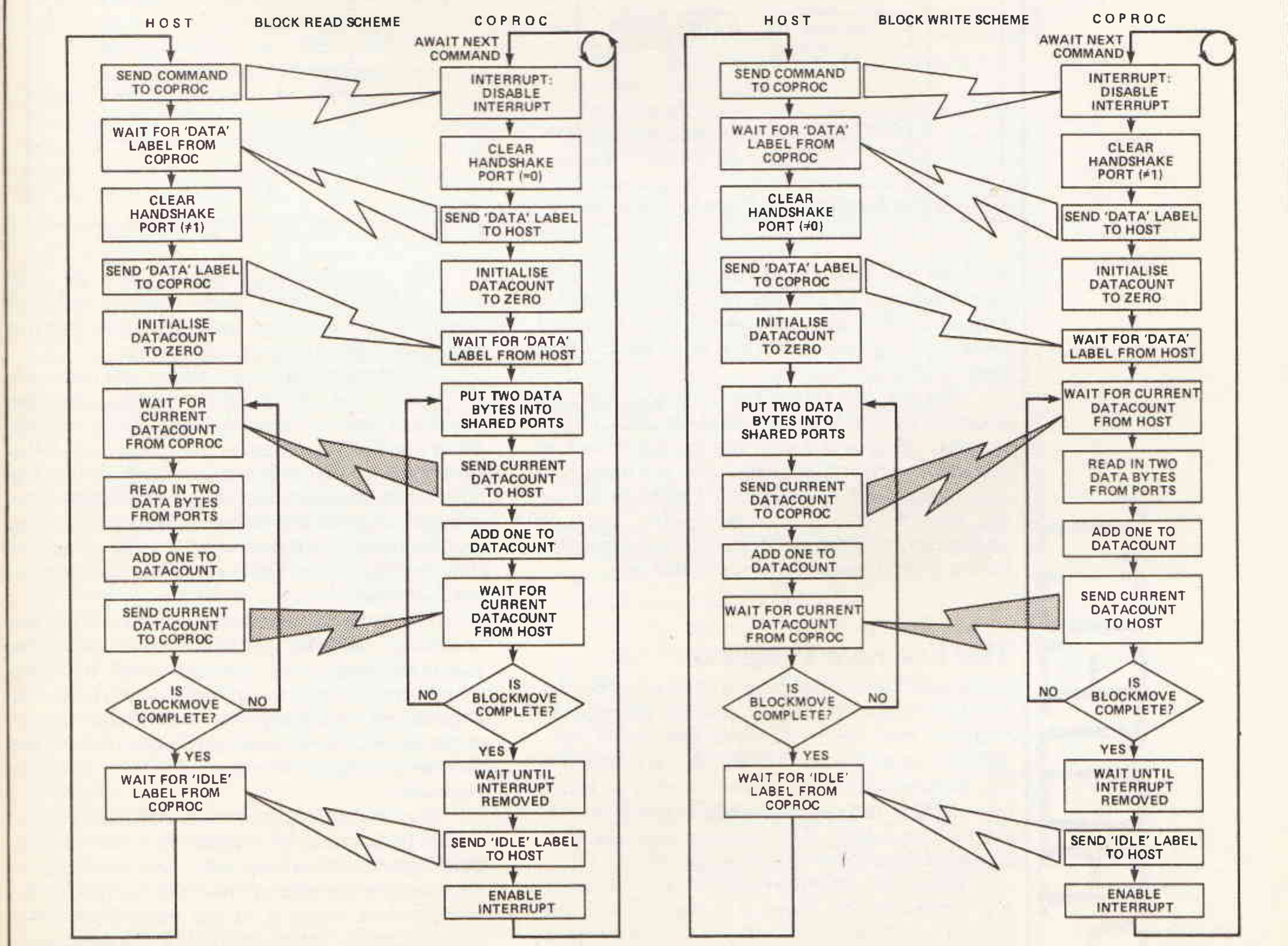


Fig. 5 The block-move flow diagrams

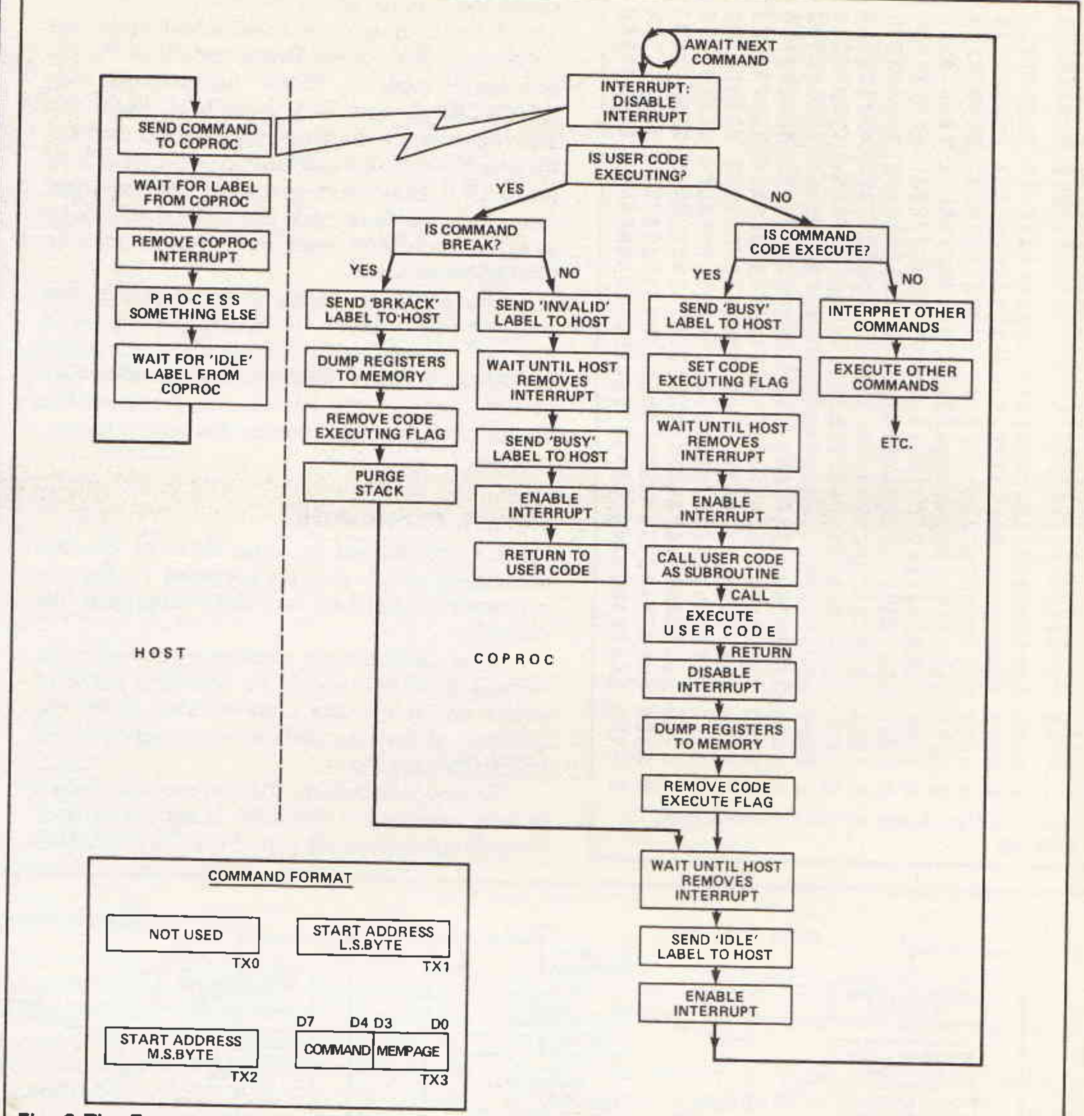


Fig. 6 The Execute User Code/Break execution flow diagram.

send the INVALID flag to the host and complete handshaking as normal before a new command is accepted. (Note also that this routine is executed anyway if a Break instruction is received whilst user code is not running).

The user can extend the range of commands accepted by changing the address in USECOM to the start address of a user routine somewhere in memory which will recognise and act upon new commands. Such an extension is quite simple but the user should have a reasonably thorough understanding of the workings of this co-processor before adding new commands in this way.

The Example Program

Looking at the flow diagrams is all very well but the time has come to look briefly at some real code. As promised last month, we reproduce here a complete listing in Spectrum Basic for the Interactive Z80 software development tool (Listing 1). It has been written not with efficiency in mind, but for absolute readability. The comments literally took longer to write than the program!

The idea is that you can type in the program (or squidge in the program if you still use the Spectrum rubber keyboard) in order to test and get to know your co-processor before writing new applications of your own.

The program has been written so that routines from the Basic can be poached and used again in completely new applications to satisfy the various handshaking protocols in use.

The more adventurous among you may wish to rewrite the handshaking routines at the Spectrum end in assembly code. Data transfer using this Basic program is pretty slow and if the handshake routine was implemented in assembly code it would speed things up dramatically. The example program was written in Basic primarily so that everyone can follow what is going on and so that changes can be easily made for experimentation purposes.

The program makes use of most of the co-processor's facilities — block moves, user code execution/breaks, self test and so on. It is fully menu driven and so using it should be self explanatory. However, a few words must be said about some of the software techniques used in the program, so they can be applied to the user's own code later.

The first point to remember is that data transfer via the interface is completely asynchronous. Reading and writing from either end can occur at any time. It is possible for one of the machines to be reading data which is at the same time being updated by the other machine. If the data being read has not had time to settle, then an erroneous transfer could result.

When the data being read is a single bit value, such as the presence of the interrupt bit from the host, then there is no problem — the bit is either one or zero and there can be no confusion. However, if the data being read is a multi-bit value then at the instant of the read, some of the bits could still be changing (having been updated fractionally before) whilst others could have already settled. The result is invalid data.

To avoid this problem without resorting to hardware arbitration, the software in both the Spectrum and the co-processor reads any handshake flag twice if it consists of more than one bit. The results of the two reads are compared and if they are identical then the flag is considered valid (such successive reads occur several microseconds apart). If they are different then further reads are performed until two consecutive results agree.

Note that it is unnecessary to treat ordinary non-handshaking data in this way, since the validity of this data is assured by the presence of the handshaking flag.

All Spectrum-to-co-processor commands, the co-processor-to-Spectrum flags and the shared port addresses themselves are given names at the start of the program to improve readability. The program then continues with the main menu screen handling and user input selection. At every stage the co-processor is being tested to ensure that it is idle and ready to receive a command.

If at any time the co-processor stops being idle without a new command having been sent (say, a hardware reset has occurred or the co-processor power has been removed) the Spectrum will wait for the idle state to return.

When the user selects an option, the program jumps to the appropriate routine to do the work. The first option loads data or code from cassette into the Spectrum starting at location 48000 (decimal) thus the longest block of data which can be loaded in one go is 16K.

The second option moves data from the Spectrum memory, starting from location 48000, into the co-processor memory starting from any desired location. Although the co-processor operating software only handles block moves of up to 512 bytes at a time, this Basic routine can handle up to 16K blocks in one go. This is achieved by actually moving the data in several 512 byte (or shorter) chunks.

The third option displays the memory contents of the co-processor from any desired starting address. Again blocks up to 16K locations may be displayed by moving several 512 byte blocks over the interface. Note that this routine only displays the transferred information. If it is necessary to store this data, a simple modification must be made to the program to poke the data into the Spectrum memory as it is transferred.

The fourth option runs user code previously moved into the co-processor and will start execution from any desired address. Once code is running, the user has the option of breaking from execution.

The fifth and final option runs the self test. After the co-processor has completed its self test, this routine goes on to execute a two byte block move of the test status data and displays the results obtained.

One point to note is that this application program can never send invalid commands to the co-processor so it never checks for the INVALID flag being returned. In some user applications such a check may be necessary and should not be omitted as it was here.

BUYLINES

To save you hours of laborious typing at the dreaded rubber keyboard, a copy of the Z80 Development Tool software, as listed in this article, is available on tape from the author for £3.00.

The two PROMs — one holding software, the other an address map — are available ready programmed and tested from the author. The co-processor operating software EPROM costs £10.00 and the address map PROM for the 256k DRAM card £6.00.

A comprehensively commented assembly listing for the co-processor operating system is also available for £3.50.

All prices include postage and packing. Please send cheques or postal orders made payable to the author at 52 Bishops Court, Trumpington, Cambridge CB2 2NN, allowing 28 days for delivery.

Co-processor Operating Software

Finally, with the Spectrum end of things out of the way, a few words about the co-processor operating software. This resides in the EPROM on the CPU card and implements the handshaking protocols described previously when triggered by new commands from the host.

Limitations in available space prevent a full listing of the co-processor source code (it runs to some twenty pages!). A hex dump of the EPROM contents (Listing 2) is reproduced for all those of you with enough spare time to type it all into a programmer. Alternatively, a copy of the listing and pre-programmed EPROMs is available from the author (see Buylines).

It should be quite possible to make use of the co-processor without reference to the operating software listing by following the flow diagrams presented in this and last month's issue, and by looking at the Basic example program reproduced here. However, to make full use of the software resident in the CPU EPROM, it is of great benefit to work in conjunction with the listing.

There are a couple of small points worth noting. Despite the limitations imposed, the co-processor stack is used as little as possible. This makes the co-processor less prone to errors caused by the stack being inadvertently corrupted by the user code.

In addition, at the end of every command routine the co-processor sets the memory page to zero regardless of what it was doing during the execution of the command. This acts mainly as a visual indication that the command has completed (by way of the page LEDs on the memory cards) and is a useful monitoring facility.

Having described each part of the co-processor hardware and software in some detail, it is now up to you to familiarise yourself with its operation, before using it in your own applications. All that remains is for me to wish you success with all your co-processor aspirations! ETI

ACKNOWLEDGEMENTS

The author wishes to thank the following companies for their help during the development of this project.
Sarel Ltd, Luton.
Inmos Ltd, Bristol
Dage (GB) Ltd, Aylesbury
Mogul Electronics, Orpington

TECH TIPS

Circuits and other ideas for Tech Tips should be sent to ETI at 1 Golden Square, London W1R 3AB. All items used will be paid for. Please include a SAE for acknowledgement

READERS CIRCUITS

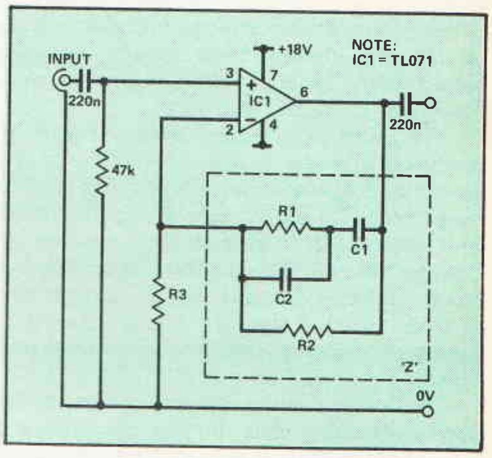
RIAA Computer Program

R Williamson
Peterborough

The mathematics of the complex networks for RIAA/IEC equalisation have been covered extensively in the June 1987 issue of ETI. If the designer decides upon one of the four possible configurations, finding the values of the two resistors and capacitors is straightforward arithmetic. However, whilst this may yield finite values, the problem of finding off-the-shelf real values remains. So, if one could arbitrarily choose say one of the resistors in a preferred value range, then by using a fast computer program it would be relatively easy to establish the other three components in easy-to-obtain values as well.

This short program, written in one of the advanced basic languages (Fast Basic by Computer Concepts for the Atari ST) does just that. It can of course be easily altered to any other Basic dialect, mainly by adding line numbers and modifying the syntax where appropriate.

I selected one particular configuration (b in Wilfred Harm's excellent June article) simply because it appeared to yield more readily near-preferred values for all four components. The designer can choose either one resistor (the principal one that decides the basic gain) or the Z of the network. Provided you also opt for a sensible degree of gain (not less than 30dB, for example) then the computation is to a high degree of accuracy. For a very extensive treatment of the subject, a paper written for and published by the Audio Engineering Society in 1978 by Professor Lipshitz of the University of Waterloo, Canada is valuable reading. This program was derived from his work.




```
    CLS:TXTSIZE 13
    PRINT:PRINT"   This is a CAD program
for an RIAA network"
start:PRINT:INPUT"   Choose R or Z by
typing R or Z:  "A$:PRINT
    IF A$="R" THEN GOTO one
    INPUT"   Select a value for Z (in
ohms @ 1kHz)  : "Z:R1=Z/1.25
    PRINT"   Computed value for
R1............         = ";R1" ohms":GOTO
rest
one:INPUT"   Select a value for R1 in
ohms....        : "R1:Z=R1*1.25
    PRINT"   Computed value for impedance
Z........ = ";Z" ohms"
rest:R2=R1*12.403:C1=2.3679E+8/R1:C2=C1/
2.916
    PRINT"            do.
............          R2 = ";R2" ohms"
    PRINT"            do.
............          C1 = ";C1" pF"
    PRINT"            do.
............          C2 = ";C2" pF":PRINT
    INPUT"   Now enter required gain in
dBs......    " ,DB:G=DALOG(DB/20)
    PRINT"   Voltage gain is........
          x ";G:R3=SQR(Z^2)/(G-1^2)
    PRINT"   Computed value for R3......
             ";R3" ohms":PRINT
    PRINT"   *    *    *    *    *    *    *
*    *    *    *    *    *    *    *":PRINT
    INPUT"   Repeat? Y or N :"R$:IF
R$="Y" THEN GOTO start
```

Electronic Blockbusters

W A Jameson
Chester

This circuit was devised to determine which of two players first hit their answer button and to allow a preset time for the answer when playing the 'Blockbusters' game from Waddingtons (based on the TV game).

The circuit gives both visual (an LED) and audible (a warble) indications that a button has been pressed and locks out the other button. A continuous tone is given as the 'time up' signal at the end of the allotted answering time.

IC1a,b and IC3a,b debounce the two answer buttons SW1 and SW2 respectively. Assuming Reset has just been pressed, both LEDs will be off and pin 3 of IC1b and IC3b will be low. One of these pins will go high if an answer button is pressed.

If SW1 is pushed, pins 12 and 13 of IC1c will both be high taking the output low. IC1d inverts this action, lighting LED1. Q2 is turned on supplying power to R8, C3 and R10 which switch on Q3 and power IC4 giving a warble from the piezo buzzer. Approximately 0.3s later Q4 is turned on cutting off the power to IC4 and curtailing the warble.

When IC8 goes high it takes pin 9 of IC2a and pin 12 of IC2b high also. This takes pin 13 of IC3 low, locking out the action of SW2.

If SW2 is pressed first, the action is reversed with SW1 locked out.

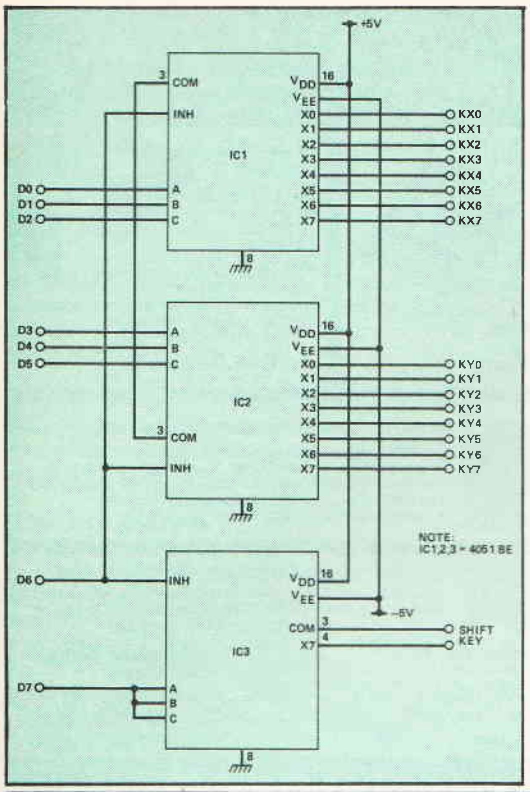
Whichever button is pressed, power is supplied via Q1 or Q2 to Q5 after C4 has charged (about 3.5s). After the delay Q5 conducts turning off Q6 and turning on Q7 which enables a continuous tone from the buzzer.

The whole system is reset by the switch SW3 which discharges C4 and resets the push button logic.

Current consumption is about 10mA in standby and 20mA when buzzing (depending on the buzzer used). A PP3 battery should cope without problems.

Extra switches can of course be added in parallel with the ones given for playing the game in teams.

READERS CIRCUITS



Pseudo Co-processing

A Thompson
Chester-Le-Street

This circuit provides a use for an old computer by placing it under the control of another machine. This can find applications as a printer buffer, for interfacing incompatible hardware, multi-processing, interfacing incompatible programs and many other ideas.

The principle is simply to control the old computer via its keyboard. The prototype system used a Sinclair QL controlling a Dragon 32. All that is needed on the new computer is an 8-bit output port.

The keyboard of the slave micro is controlled by the three analogue switch ICs. The outputs marked K are connected to the ribbon cable connected to the keyboard matrix in the slave machine. Experimentation is required to find which key is connected to which terminal of the ribbon connector.

64 keys can be controlled in this way. The shift key is required to be controlled separately (so it can be used in conjunction with the others). Bit 7 of the output port controls the Shift key.

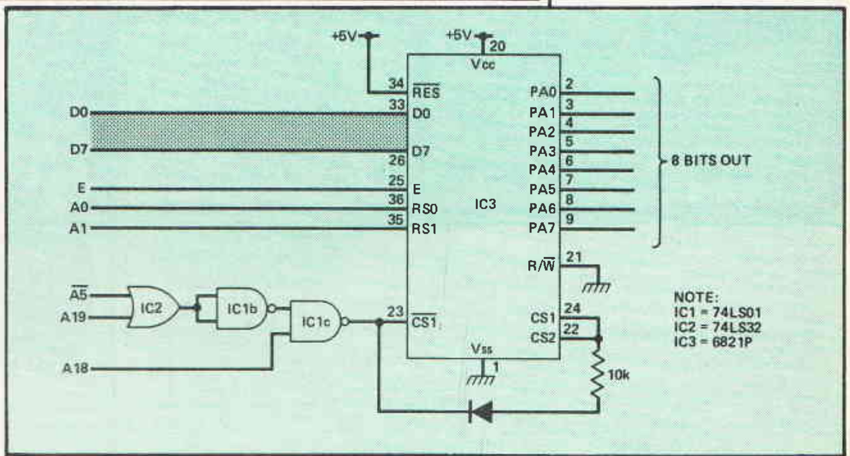
The host computer can, with this interface, type programs into the slave micro, run them, enter data and all manner of other tasks.

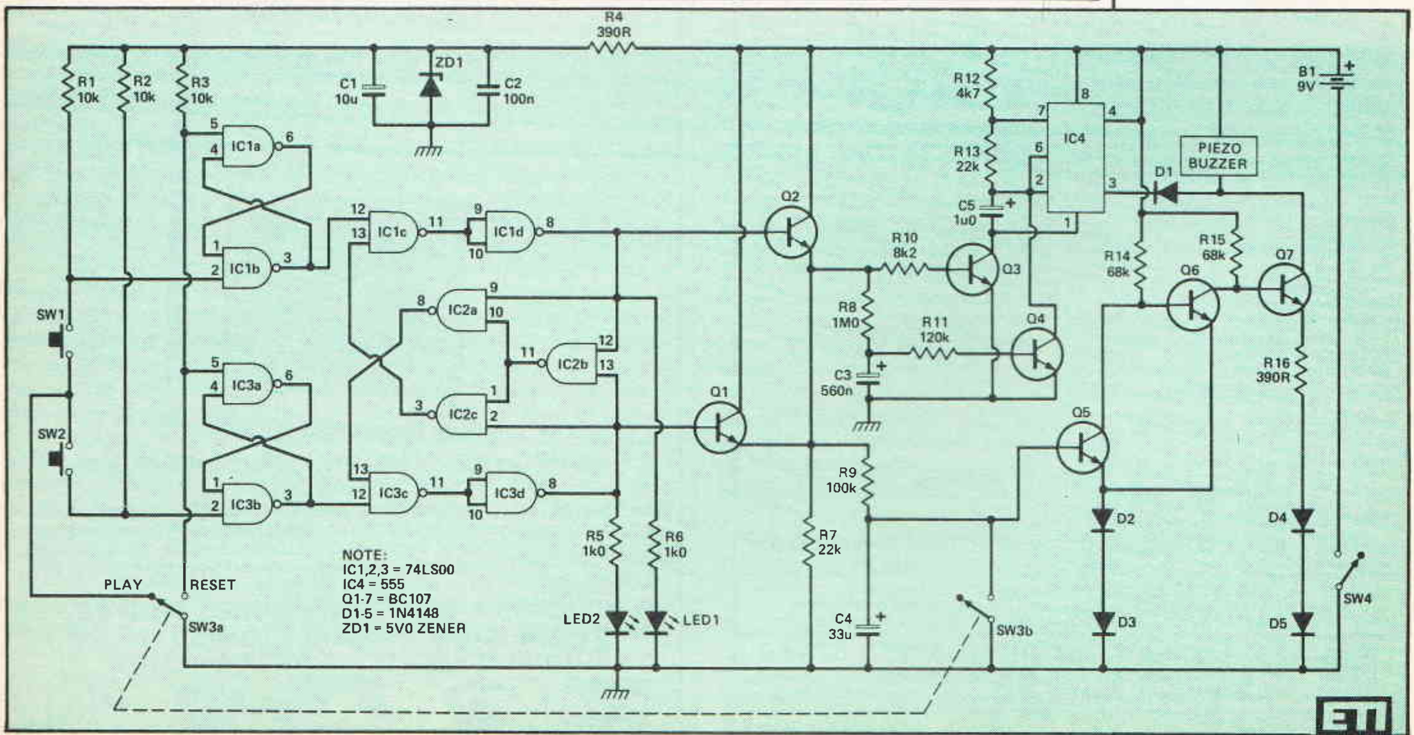
QL Output Port

A Thompson
Chester-Le-Street

This circuit provides just about the simplest ever add-on 8-bit output port for the Sinclair QL.

All the signals necessary are available at the QL's expansion socket.





PLAYBACK

The general standard of VHS video recorders has improved considerably over the last few years in terms of sound and picture. Of particular interest to me is the widespread introduction of 'hi-fi' sound. I have long been used to a sound quality from my video which, even with the Dolby switched on, sounded like Hissing Sid with the bass and treble attenuated.

Sound Advice

I shall not attempt to go into the technicalities of the hi-fi recording standard. Suffice it to say that a stereo audio signal is encoded in with the video information on hi-fi machines.

The previous sound standard, an analogue recording track at the edge of the tape, is also implemented in such machines, but in mono and without Dolby just to allow compatibility with old recordings (and to allow tapes recorded on the gleaming new design machines to play on older types).

Another sound facility which some machines offer is the ability to decode stereo television transmissions, as and when these become available. The Nicam stereo system was first tested by the BBC and rumour has it that they transmit some programs in stereo for test purposes. I haven't caught them at it yet but as the rumour also states that *Wogan* is the program they do in stereo from time to time, there is little chance of me catching a stereo transmission.

It appears that because the BBC is so short of money (?) they can't afford to move into full scale stereo in the near future. It is entirely possible that pressure from advertisers will force the independent channels to introduce stereo first. This could occur in as little as a year, though my guess is that it will take at least two.

Stereo Woe

As an aside, there is some difficulty in deciding how to make stereo TV into an advantage rather than a disadvantage. The difficulty is that it seems unrealistic to have people's voices coming from a direction significantly different from that of the screen. One idea is to keep speech in mono and have stereo background music, sound effects and so on.

I have compared the sound quality on several different machines, and would say that hi-fi sound represents a major improvement over analogue sound. To my ears, the sound quality is almost (but not quite) up to CD standard.

On one prerecorded rock music video, recorded in hifi and analogue stereo, it was possible to hear the pick hit the guitar string for the first time on a hi-fi machine.

Most hi-fi machines are designed with the casual user in mind and they incorporate automatic record level adjustment. This is not generally too obtrusive but for the truest sound it is better to have manual settings available. A few top of the range machines sport this facility.

As a logical extension of hi-fi sounds with video, some machines offer half speed hi-fi without video. This permits up to 8 hours recording on a VHS cassette, with a quality above that available from most other recording media.

Pseudo DAT

DAT it isn't but it would seem to perform the same function as far as most people are concerned. One distinct advantage of this recording medium is that it is available now, unlike DAT.

From many people's point of view it could be more attractive for home recordings than DAT. The size of cassette would be the main disadvantage. The advantage is that if you are going to have a video recorder anyway, why not record sound as well and save the £800 or so which a DAT machine would cost. With E180 cassettes offering six hours recording for around £4, the cost of digital audio cassettes would also appear uncompetitive.

'But,' I hear you say, 'DAT offers better quality.' No doubt this is true, but is it important? It is generally accepted that VHS is the worst videocassette system for both sound and picture, yet it dominates the market. Perhaps if video hire shops were to carry a large stock of 8mm films then 8mm would catch on in a big way. And if 8mm caught on, video films would be available in 8mm. This is a circle I doubt will be broken.

In the same way, it is possible that VHS recorders offering good quality half speed audio recording will cut the potential mass market away from DAT. It will be interesting to find out.

Andrew Armstrong

OPEN CHANNEL

About eleven years ago, somebody decided it would be a good idea if all computers could talk to each other. You may be proud to learn that in fact this somebody was the British delegation to an International Standards Organisation (ISO) Plenary meeting in 1977 when we proposed that the possibility of standards for computer interconnections should be looked into.

But, as you'll imagine, this would be no mean feat. For any computer anywhere in the world to be able to communicate with any other, a number of problems have to be overcome. Not least is the conformity which all computers would need in both hardware and (more particularly) software.

The Plenary ISO meeting decided to investigate the matter through a sub-committee, which came up with a reference model into which the necessary standards could fit, known as the *ISO Reference Model of Open Systems Interconnection* (OSI).

OSI is defined as comprising seven layers, incorporating hardware *and* software standards. Effectively these layers correspond to the different communications requirements of two communicating computers, from hardware through to software. The layers are known as: physical, datalink, network, transport, session, presentation, application.

OSI became rather a key word in the early part of the decade and many attempts were made to standardise the model itself but it wasn't until 1984 that the ISO actually published the standard (ISO 7498: 1984).

Bearing this in mind, it's not surprising that other relevant standards to get OSI up and running have been a long time coming (and will be a long time yet).

Many current communications standards have been used or adapted to form the lower layers of the model, where the model refers simply to straightforward wiring between plugs and sockets or the codes, tones and so forth which convey data across wires.

However, the higher layers are yet to be fully standardised. Too many computer manufacturers spoil the broth as the saying goes, and each manufacturer wants to get his oar in (or is it ladle?). Still, work is going on nicely, mostly concentrating on the application layer.

Talking Of Which...

Apparently, a new standards institute is to be set up to standardise standards throughout Europe, if that makes sense. Following a European Commission Green Paper last year recommending the opening up of telecommunications markets within Europe, many manufacturers feel that a more standard approach to the subject is required, and that common standards are required.

I thought the definition of a standard meant it *was* common. Oh well.

One + One = One

At last, it appears the proposed merger of GEC and Plessey's telecommunications divisions is to be allowed, following the Department of Trade and Industry's recent go-ahead.

Given that GEC is not allowed to buy more than a 15% share of Plessey and that nothing be done which would require referral back to the Monopolies and Mergers Commission, the merger looks set to take place once the Plessey shareholders agree to it.

At the time of writing merger had not been ratified but by publication of this month's ETI, things should have been decided.

The dream of GEC Plessey Telecommunications Holdings looks, eventually, like becoming a reality. Not before time. The increased marketing power (not to mention development power) the new company will have can only be of benefit to both GEC *and* Plessey, as well as being good for Britain.

Beep, Beep

If you have ever worked for an organisation which demanded that every employee be contacted quickly if needed, you'll know the benefits of radio pagers — those blasted little boxes people clip to their top pockets or belts which go 'beep, beep' at the most irritating times. Once paged, the user goes rushing off to the nearest phone to see who wants him and what for.

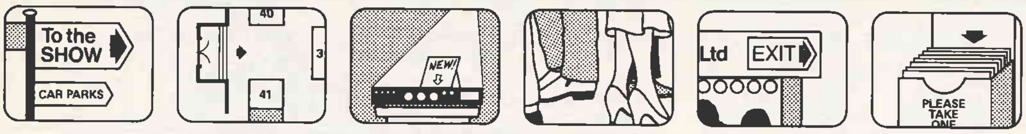
There are nearly half a million of these animals (yes, that's what I said, half a million!) currently in use in Britain in one form or another and forecasts suggest this figure will more than double in the next three years.

Showing Off

Incidentally, May sees one of the biggest exhibitions in the communications world (well, in Europe at least). Communications 88 runs at the National Exhibition Centre, Birmingham from 10-13 May. And it's a show not to be missed.

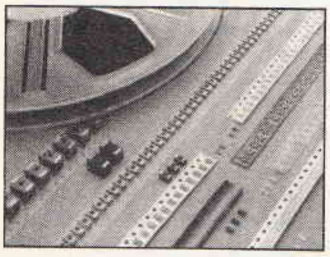
Keith Brindley

SMARTEX SURFACE MOUNT SHOW



If someone had told me two years ago that the new method of printed circuit board assembly was to use a PCB without holes, leadless components which are stuck onto the PCB with glue and then the PCB (held component side down) is passed through a wave solder machine which completely immerses the components in solder, I would have thought that person to be slightly wacko.

Such procedures, however, are definitely not the dealings of a demented engineer but are now one of the standard surface-mount component assembly methods.



The 1988 Smartex Exhibition at London's Barbican centre was an opportunity for engineers involved in electronics design and manufacture to see the latest SMT machines, components and materials.

The range of components available in surface-mount has expanded considerably since Smartex 87 and many more semiconductor manufacturers have committed themselves to SMD production. Familiar names such as Texas Instruments, Ferranti, Siliconix and Siemens were all represented, with sales engineers eager to acquaint you with the latest technology.

The limited range of capacitors available in SMD has been a handicap to circuit design. However, this situation is being rectified by companies such as Integrated Ceramic Components Ltd, Siemens, AVX, Syfer and Wimpey-Dubilier (Wellies and donkey-jackets not included).

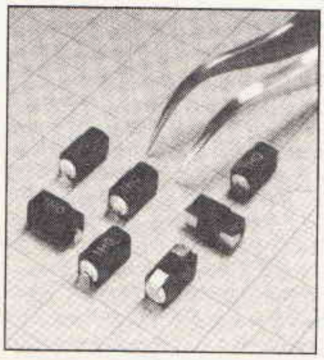
RBS Components Ltd demonstrated their ability to manufacture surface mount inductors but the range is limited to 1000µH and current ratings are rather on the low side.

The simplest way of 'populating' a surface-mount printed circuit board with components would be to pick up each component with a pair of tweezers and place it in the required position on the board. A fine tip soldering iron could then be used to solder it in place. This method would call for a very dexterous operator.

The work is made many times easier by manually operated pick and place machines, examples of which were exhibited by Coopertools and Groatmoor Ltd. These machines incorporate a manually guided head on which can be mounted an adhesive dispenser and a vacuum probe for picking up the SMDs. Glue dots are placed on the PCB where the body of the device is to be located and the device is then picked up by the vacuum probe and placed in the desired position. Soldering would then be performed by passing the PCB along a dual wave-soldering machine.

An alternative method is to use a solder paste dispenser to apply paste to the pads of the PCB and after placement of the SMD a hot air pencil is used to reflow the solder paste to effect the soldered joint. These manual machines are mainly intended for small production runs or prototype manufacture and are still somewhat dependent upon the dexterity of the operator, who needs to have 20-20 vision!

Automatic pick and place machines are a must for volume production and among the manufacturers exhibiting such machines were Universal Dynapert, Precima and Zevatron.

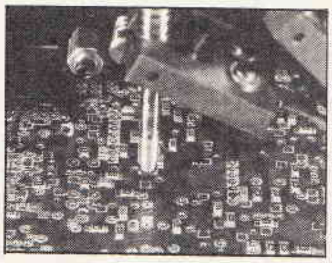


Components are supplied in tape and reel packing, and these machines have to be programmed either by an operator who simply 'teaches' the machine by moving its placement head to a component and then placing it in the desired position, or the x-y coordinates of each component's location are loaded in via a terminal or downloaded from a CAD system.

These machines can pick and place up to 5000 components per hour with an accuracy of ±0.1mm.

The manufacturers' representatives indicated that many refinements to their automatic placement machines had been made since Smartex 87 in an attempt to reduce down time and increase reliability.

There weren't any wave soldering machines on demonstration for obvious reasons of ventilation,



however there was a faint whiff of flux fumes in the air due to the presence of an infra-red reflow soldering machine and various re-work stations.

Solder re-flow is an alternative to wave soldering. The solder, in paste form, is printed onto the PCB pads and after component placement the solder is then melted by placing the entire PCB in a hot vapour atmosphere. A more up to date method is heating the board in an infra-red oven. The now molten solder flows around the component leads and completes the joint.

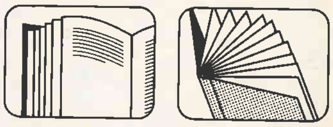
When things go wrong, soldering defects are often given colourful names such as the 'Drawbridge effect' (chip resistor or capacitor lifted at one end) and the 'Manhattan effect' (chip component actually standing on end).

Machine manufacturers are striving for 'Utopian' zero-defect production but in reality errors do occur and have to be rectified. Large expensive boards cannot be scrapped because of one or two faults and so inspection and rework facilities are essential.

Removing faulty resistors is comparatively simple but the removal of a 68-pin PLCC calls for something more sophisticated than a 15W iron and a solder-sucker. OK Industries exhibited their new GEC/Marconi hot gas rework system and on a smaller scale Zeltek demonstrated the DR Tresky Engineering improved hot air and vacuum pencil rework facility.

Surface mount is an exciting new technology and allows a considerable reduction in PCB sizes compared with conventional through-hole technology. The component prices in SMD however are disappointingly higher than their through-hole counterparts especially for discrete components. However, I am told prices will fall as production volumes go up. The manufacturing processes can be heavily automated which reduces labour costs although the purchase of the machines calls for heavy capital investment which many companies may think twice about.

BOOK LOOK



A couple of 'useful' enthusiast's books come under scrutiny this month. It seems there is no end to this type of publication. However, that must be a pretty good thing for those of us who are keen on the idea of electronics as a hobby.

CMOS Circuits Manual by R M Marston, Heinemann Newnes, £9.95

Mr Marston will be a familiar name to longer standing ETI readers. This is the first in what looks like a potentially enormous series of 'manuals' for Heinemann Newnes.

(Isn't it terrible when two publishing companies join together and both names are famous and so have to be kept — the result begins to sound rather like a local firm of solicitors. Anyway, back to the book).

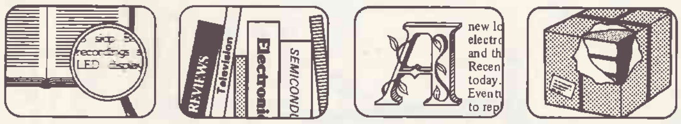
The CMOS circuits manual is really an organised collection of Tech Tips with some basic background theory thrown in for good measure.

The book starts off looking at what CMOS is, how basic CMOS gates work and why they don't mix too well with static.

All the equivalent circuits and transfer characteristics are quite interesting but it seems a little over indulgent in the light of the rest of the book.

This appears to be essentially a practical book aimed at actually working with the devices in question. I can't help feeling that many details of exactly what goes on inside the little black plastic lumps won't really find many takers.

Maybe it's just my inbred hatred of most things mathematical ... Still, the first chapter only lasts about a dozen pages so I shouldn't complain too much.



first place. It's hardly easy reading, it's not a text book to plough through and learn the subject nor is it really a reference work to pick up for snippets of information.

However, it is thoughtfully put together and covers the ground well. It taught me several things I didn't know and promises to teach me more as I use it again. If you're in that limbo state of beginning to grasp the fundamentals of electronics but a little unsure as to how to actually progress onto meaningful project design, this one will serve well.

Optoelectronics Circuit Manual by R M Marston. Heinemann Newnes. £10.95

The series blossoms. Don't ask me why this one's a quid more. It's marginally shorter and otherwise consists of very similar stuff.

Still, if the good lord had meant us to understand book prices he wouldn't have given us publishers.

This one very much follows the same line of attack as the CMOS tome. The first chapter looks at basic principles and this time they are a lot more basic — what are bulbs, neons, LEDs, LCDs, photocells and even (pushing it a bit, this) a look at cathode ray tubes.

Again, the other chapters are devoted to a subject each and go into in greater depth — LED display circuits; LED graph circuits; Seven segment displays; Light sensitive devices; Optocoupler devices; Brightness control techniques; Light beam alarm; and Remote control systems.

The whole tone of this book is a bit easier than the last. It is better suited to the beginner and to practical application. It also has the great advantage that it is great fun for the electronics beginner to play around with flashing LEDs and impress their friends with 'magic' infra-red broken beam switches.

So again, if you want to know that little bit more about using these good fun devices, if you're prepared to experiment a bit with relatively little help, this book will form the basis of an interesting and informative time.

If and when this collection of Marston manuals grows, the whole set will undoubtedly provide a solid basis for enthusiast knowledge.

The only problem is that at £10/11 a time (or are these the bottom end of a price curve?) few mere enthusiasts will be able to afford them all.

Martin Tame

Next is a whole chapter devoted to the 4007. This is again a little theoretical (and rather mathematical!) for me but it is a lot more useful at the same time. The 4007 is the basic building block of CMOS and so it does justify such attention.

There's quite a lot of good practical advice hidden amongst the equations and graphs too so it's well worth a read.

The rest of the book is split up into chapters covering particular functional areas. Each area is liberally illustrated with circuits of basic CMOS gates and the dedicated CMOS chips.

Many subjects are covered — Inverter, gate and logic circuits; Bilateral switches and selectors; Clock generators; Pulse generator circuits; Clocked flip-flops; Up and up/down converters; Down counters and decoders and various miscellany.

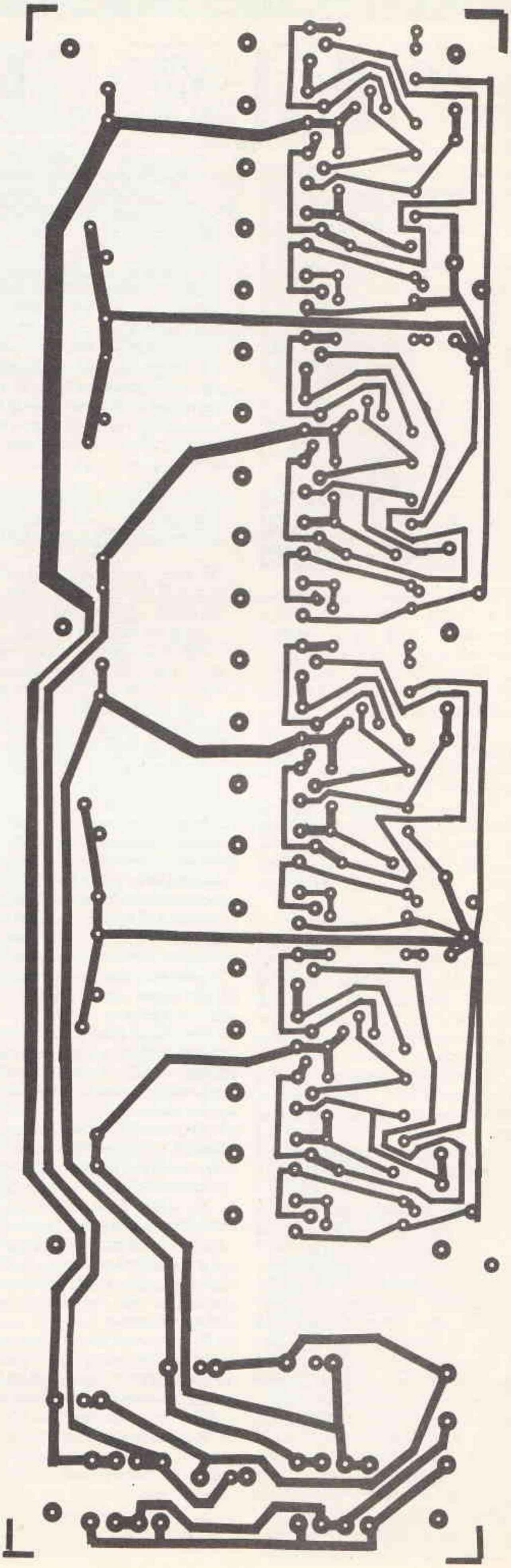
Each function area has a basic introduction and description, a look at some basic principles, tips and things to watch for, the relevant chips and some (rather contrived) example circuits.

The chapter on bilateral switches and decoders for example covers the 4016, 4066, 4051-3, 4067 and 4097, and has circuits for latching switches, touch switches, digital resistance, capacitance and gain control and a sample and hold circuit to name but most of them.

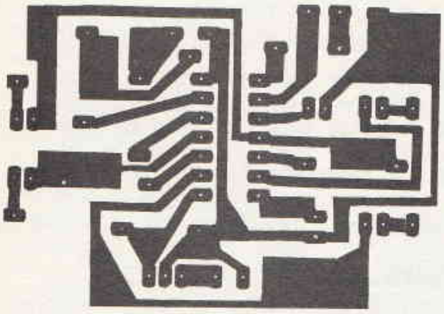
In the process of delving into all these subjects Marston manages to cover most of the common CMOS ICs. There are some notable exceptions (notable in my eyes at least) and absolutely no mention of 74HC series chips but I guess those really are another story.

The big problem with the CMOS Circuits Manual is why read it in the

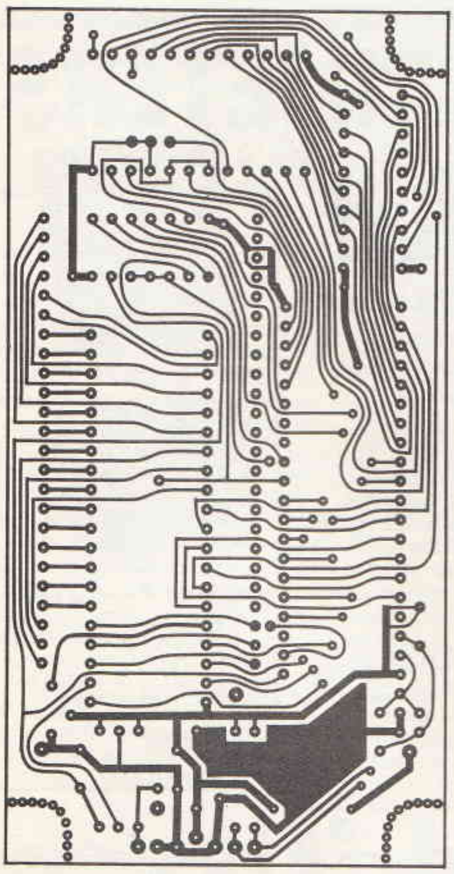
PCB FOIL PATTERNS



The Virtuoso Power Amp 2U case power supply board →



The Dynamic Noise Reduction system foil



The Bicycle Speedometer Board

OOPS!

MIDI Master Keyboard (June 1987)
In Fig. 3 and the Parts List there is some confusion as to the correct part numbers for some ICs. These should be: IC17 — 2764, IC18 — 6522, IC10, 21 — 74LS32.

Car Alarm (August 1987)
In Fig. 1 Q7 is not numbered and its emitter is shown unconnected. This connects to earth. The transistors in the parts list went a little awry. Q2-6 are BC237 and Q7 is a TIP31.

Boiler Controller (September 1987)
In Fig. 2 (a) the primary of T2 is shown connected to Earth. This should be neutral. In Fig. 2(b) one of the bridge rectifier diodes, D6-9, is shown the wrong way around. This is correctly shown in Fig. 5.

EEG Monitor (September 1987)
In Fig.3a the pins of IC1 connected to the power rails are shown swapped around. In Fig.4a R7 is unlabelled and is between C3 and C6. In Fig.5 C20 should be £10 and R18 is unlabelled. It lies between R17 and R19.

ETI Concept (October 1987)
The Power Board parts list wrongly lists R6 as 270R. This should be 270k. Also, note that the power board's 0V rail must *not* be connected to Earth or the 0V rail of the CPU board.

Printer Buffer (November 1987)
The software for the EPROM had three errors listed. The byte at 039A should read 20, at 039B 14 and at 0492 30. All numbers are in Hex.

Dream Machine (December 1987)
The transistors used in this project are ST1702. BC108s can be substituted.

Heating Management System
(December 1987)
A 4116 is not a suitable alternative to the 6116 specified. A 4016 RAM chip will suffice. In Fig. 1 the junction of R1/D5 should connect to D1-4/C1 and not cross. The zener diodes above the temperature sensor ICs (IC16-19) should be deleted. C4 should be 220n and not 220µ. C7-10 should be 10µ. Q2-7 should be 2N3904 and not BC3904.

RGB Auto-Dissolve (January 1988)
In Fig. 5 there are marked two D6's. The right hand one should be D5 (they are both 1N4148's anyway). In the text the reference to zener diode D5 should read zener diode ZD1.

PASSIVE INFRA-RED ALARM
(January 1988)
Fig. 2(a) shows the base of Q1 connected to ground and to R14. It should be connected only to R14.

Clean Up Campaign (January 1988)
In the component overlay (Fig. 3) ZD1 is incorrectly orientated. The positive terminal should be the southern end.

Spectrum Co-processor (March 1988)
Mogul Electronics, given in the Buylines as suppliers of the RAM chips, have moved to: Unit 11, Vestry Estate, Sevenoaks TN14 5EU. Tel: (0732) 741841.

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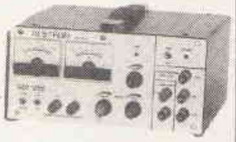

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