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digital handbook

Basic fundamentals of the Digital Integrated Circuit. . . with charts, schematics, and 8 easy-to-build projects for the hobbyist & experimenter

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When you see the Calectro label you can be sure you're purchasing the finest in electronic merchandise! You'll find a wide variety of electronic products - nearly 1000 in all, from digital integrated circuits to tools and accessories! Calectro truly offers you more - it's the new look in electronics!

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Forward

The Calectro Digital Book is intended to provide the Hobbyist and Experimenter with a basic understanding of how a Digital Integrated Circuit works, and a number of interesting circuits. Circuits of general interest have been selected.

All circuits have been built and thoroughly tested, but we cannot assume responsibility for their function or consequences of application. If normal care in construction is followed, you should find many hours of enjoyment in building your own circuits and employing them in your own creative applications.

The Calectro and Digital Handbooks contain many very detailed projects, an electronic symbols chart and other information helpful in learning to read schematics easily. Take your time, and enjoy yourself.

EDITED BY LYLE M. HANEY

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DIGITAL INTEGRATED CIRCUITS

What are integrated circuits? What can they be used for? Why should I use integrated circuits and not transistors, diodes and other discrete components? What is the difference between a digital circuit and other types of circuits, such as amplifiers? We are going to answer these questions and show how easy it is to use integrated circuits to build electronic equipment--equipment you will be proud to own and use.

We will work with only one type of digital integrated circuit in this book, the transistor-transistor logic, or commonly referred to as TTL. Every effort has been made in our explanations to use words with which everyone is familiar.

An integrated circuit is a very small package containing many transistors, diodes and resistors all assembled on a microscopic piece of material referred to as a chip. There is no need to know what goes on inside of an integrated circuit to be able to use it.

One low cost Integrated circuit can be used to replace many components normally used to build electronic equipment, making it much easier and less expensive to build.

A digital circuit is one which is either in an "off" or "on" condition, whereas, an audio amplifier can be adjusted to any volume--high, low or somewhere in between. The TTL digital integrated circuits, which we will be using, operate on 5 volts DC. It requires at least 2 volts to turn an input "on" and 0.8 volts or less to turn an input "off".

A very brief and simple explanation will be given in the next few paragraphs on how the different types of TTL digital integrated circuits work. After becoming more familiar with them, you may want to try your hand at designing your own circuits. For those of you who do, a more detailed and technical explanation is given on the specification sheets included in the appendix.

GATES

A gate is the electronic equivalent to just what the name implies; an electronic door that can be opened or closed when the correct code is used on the combination lock. All we need to know is the correct code to apply to the inputs of the gate to turn them "on" or "off". There are four basic kinds of gates: "or" gate, "and" gate, "nor" gate and "nand" gate. The symbol and code for each gate is shown in Fig. 1. The gates shown in Fig. 1 have two inputs, but some gates have 3, 4 and 8 inputs. Regardless of the number of inputs, the code remains the same. To turn one of the inputs "on", it may be connected to 5 volts DC through a 1000 OHM resistor and switch, or by connecting an input directly to the output of another gate or integrated circuit. To turn an input "off", it may be connected directly to ground, or to ground through a switch, or by connecting it directly to the output of another gate or integrated circuit. An input that has not been connected to ground or 5 volts DC assumes a turned "on" condition. The inputs should always be connected to ground or 5 volts DC, depending on how the gate will be used, or even if the input is not being used.

FIG. 1

SYMBOL	CODE
 "AND" GATE	Output is "on" only when all inputs are "on". Output is "off when any or all inputs are "off".
 "NAND" GATE	Output is "off" only when all inputs are "on". Output is "on" when any or all inputs are "off".
 "NOR" GATE	Output is "on" only when all inputs are "off". Output is "off" when any or all inputs are "on".
 "OR" GATE	Output is "off" only when all inputs are "off". Output is "on" when any or all of the inputs are "on".

INVERTERS

Inverters invert, simple enough? When the input is "on", the output is "off". When the input is "off", the output is "on". The symbol and code are shown in Fig. 2. The input is turned "on" and "off" the same way the inputs of the gates are turned "on" and "off".

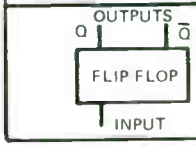
FIG. 2

SYMBOL	CODE
 INVERTER	Output is "on" only when the input is "off". Output is "off" only when the input is "on".

FLIP-FLOPS

A flip-flop can be compared with a push button switch connected to two lamps. When the button is pushed and released, one of the lamps will turn "on" and the other "off". If the button is again pushed and released, the lamp that was "off" will now turn "on" and the lamp that was "on" will turn "off". There are many different types of flip-flops, but they all operate basically the same. The difference is in the number and type of inputs.

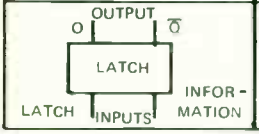
FIG. 3

SYMBOL	CODE
	"Q" output is "on" when "$\bar{Q}$" output is "off". "Q" output is "off" when "$\bar{Q}$" output is "on". Outputs change when the input is turned "off".

LATCH

A latch is a flip-flop designed for a particular job, which is to store information until it is needed. It has an extra input which we will call a latch. When the latch is turned on, the information on the input will be transferred to the "Q" output. When the latch is turned "off", the information that was on the input at the time the latch was turned off, will be stored on the "Q" output. The symbol and code are shown in Fig. 4.

FIG. 4

SYMBOL	CODE
	"Q" output will follow the information input. "$\overline{Q}$" output will always be the opposite of the "Q" output.

COUNTERS

Flip-flops are also used to make counters. They are connected so they will count the number of times the input has been turned "on" and "off". A counter can also be used as a divider. A digital counter does not count as you or I would -- 1, 2, 3 . . . . .etc. It counts 1, 2, 4, 8 . . . . .etc. Example: After having counted to the number 3, the outputs numbered 1 and 2 (See fig. 5) will both be turned "on". Outputs 4 and 1 will both be "on" when the count of 5 has been reached. Outputs 4, 2 and 1 are "on" when the counter reaches the number 7. The outputs of a counter are generally connected to an integrated circuit called a decoder, which automatically changes the 1, 2, 4, 8 method of counting to our more familiar 1, 2, 3 . . . . .etc. method. The two most popular counters are the divide-by-12 and divide-by-10 counters. Divide-by-12 counters are often used in clocks. Divide-by-12 counters can divide by 2, 3, 6 and 12. Divide-by-10 counters are used to count from 0 thru 9 and can divide by 2, 5 and 10. The counters will reset to zero after reaching the end of their count.

FIG. 5

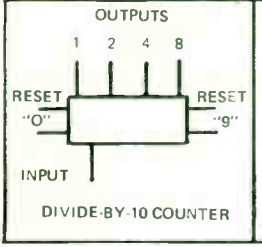
SYMBOL	CODE
 DIVIDE-BY-10 COUNTER	As the input is turned "on" and "off" the count is accumulated on the outputs. Refer to Table 1 to determine which outputs are turned "on" for each count. To reset the counter to "0" both of the "reset to 0 inputs" must be turned "on". To reset the counter to "9" both "reset to 9 inputs" must be turned "on". If the reset to "9" inputs are turned on the counter will reset to "9" even if the reset to "0" inputs are turned "on". If one or both inputs of both pairs of reset inputs are turned "off" the counter will count.

TABLE 1

COUNT	OUTPUTS "ON"
1	1
2	2
3	1-2
4	4
5	1-4
6	2-4
7	1-2-4
8	8
9	1-8
0	0

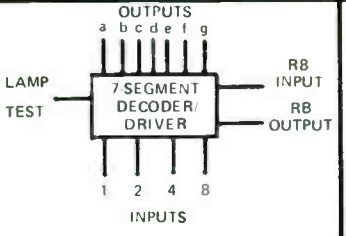
DECODER/DRIVER

A decoder/driver is used to decode the outputs of a counter and turn "on" the lamps to display a number. The four outputs of a counter are connected to the four inputs of a decoder. We are using a 7 segment decoder/driver to drive the seven lamps in our display. There are some displays which have 10 lamps and require another type of decoder/driver. An additional input has been included to test the lamps by turning the input "off" with a switch. A blanking input (RBI) and blanking output (RBO) are used to turn off the displays that have zeros displayed which are not needed. Example: In the number 000360, the first three left hand zeros are not needed and only tend to make the number hard to read. To prevent the leading zeros from being displayed, the RBI input of the leading display is turned "off" and the RBO output is connected to the RB input of the next display. All the remaining displays are connected the same way.

TABLE 2

COUNT	INPUTS				OUTPUTS						
	1	2	4	8	a	b	c	d	e	f	g
1	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON
2	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF
3	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF
4	OFF	OFF	ON	OFF	ON	ON	OFF	ON	ON	OFF	OFF
5	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
6	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
7	ON	ON	ON	OFF	OFF	ON	OFF	ON	ON	ON	ON
8	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
9	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

FIG. 6

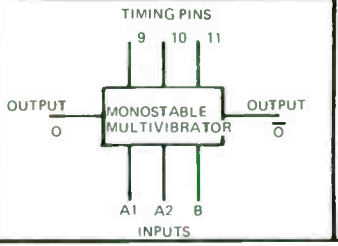
SYMBOL	CODE
	Outputs are connected to corresponding segments of 7-segment display. See Fig. 8. Inputs are connected to corresponding outputs from either the latch or counter. The 7-segment display may be tested by turning the lamp test input "off". Refer to text for explanation of blanking inputs and outputs. Table 2 shows which inputs and outputs are "on" and which are "off" for each number counted. Outputs that are "off" cause corresponding display segments to turn "on". When the outputs go "off" the lamps are shorted to ground, the other end of lamps are connected to +5 volts causing them to light.

MONOSTABLE MULTIVIBRATOR

This integrated circuit is also called a "one shot". Once a one shot is turned "on", it will remain "on" for a period of time determined by an external capacitor and resistor. The time can be varied from .04 micro seconds to 40 seconds by selecting the proper resistor/capacitor combination. Refer to Table 3 for approximate values of the resistor and capacitor needed for specified time intervals. Without external timing components, with timing pin 9 connected to pin 14 and pins 10 and 11 left unconnected, the minimum timing cycle of .03 micro seconds can be obtained. The length of time the input is turned "on" must be less than the length of time the output is turned "on". Three inputs are provided to turn the "one shot" on.

A timing resistor of approximately 2000 OHMS is provided internally by connecting Pin 9 to Pin 14. The positive end of the timing capacitor should be connected to pin 10 and the negative end to pin 11. A variable resistor may be connected between pins 9 and 14 to adjust the timing. For a fixed timing cycle, a fixed resistor is connected between pins 11 and 14, with pin 9 left unconnected. The proper symbol and code is given in Fig. 7.

FIG. 7

SYMBOL	CODE
	**Before timing cycle starts "Q" output is "off" and "$\overline{Q}$" output is "on". Inputs A1 and A2 start timing cycle when one or both are turned "off", if B input is "on". B input will start timing cycle when one or both of the "A" inputs are turned "off".**

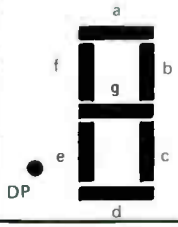
TIMING TABLE 3

TIMING RESISTOR	10 Pf CAP	47 Pf CAP	100 Pf CAP	470 Pf CAP	001mf CAP	0047 mf CAP	01 mf CAP	047 mf CAP	1 mf CAP	47 mf CAP	1 mf CAP	4 7 mf CAP	10 mf CAP	47 mf CAP	100 mf CAP	470 mf CAP	1000mf CAP
1800	0126	0592	126	592	1 26	5 92	12 6	59 2	126	592	1 26	5 92	12 6	59 2	126	592	1 26
2200	0154	0724	154	724	1 54	7 24	15 4	72 4	154	724	1 54	7 24	15 4	72 4	154	724	1 54
2700	0189	0888	189	888	1 89	8 88	18 9	88 8	189	888	1 89	8 88	18 9	88 8	189	888	1 89
3300	0231	1086	231	1 086	2 31	10 86	23 1	108 6	231	1 086	2 31	10 86	23 1	108 6	231	1 086	2 31
3900	0273	1283	273	1 283	2 73	12 83	27 3	128 3	273	1 283	2 73	12 83	27 3	128 3	273	1 283	2 73
4700	0329	1556	329	1 556	3 29	15 56	32 9	155 6	329	1 556	3 29	15 56	32 9	155 6	329	1 556	3 29
5600	0392	1842	392	1 842	3 92	18 42	39 2	184 2	392	1 842	3 92	18 42	39 2	184 2	392	1 842	3 92
6800	0476	2237	476	2 237	4 76	22 37	47 6	223 7	476	2 237	4 76	22 37	47 6	223 7	476	2 237	4 76
8200	0574	2698	574	2 698	5 74	26 98	57 4	269 8	574	2 698	5 74	26 98	57 4	269 8	574	2 698	5 74
10000	0700	3290	700	3 290	7 00	32 90	70 0	329 0	700	3 290	7 00	32 90	70 0	329 0	700	3 290	7 00
12000	0840	3948	840	3 948	8 40	39 48	84 0	394 8	840	3 948	8 40	39 48	84 0	394 8	840	3 948	8 40
15000	1050	4935	1 05	4 935	10 5	49 35	105	493 5	1050	4 935	10 5	49 35	105	493 5	1050	4 935	10 5
18000	1260	5922	1 26	5 922	12 6	59 22	126	592 2	1260	5 922	12 6	59 22	126	592 2	1260	5 922	12 6
22000	1540	7240	1 54	7 240	15 40	72 40	154	724 0	1540	7 240	15 4	72 40	154	724 0	1540	7 240	15 4
27000	1890	8880	1 890	8 880	18 90	88 80	189	888 0	1890	8 880	18 9	88 80	189	888 0	1890	8 880	18 9
33000	2310	1 086	2 31	10 86	23 1	108 6	231	1086	2310	10 86	23 1	108 6	231	1086	2310	10 86	23 1
39000	2730	1 283	2 73	12 83	27 3	128 3	273	1283	2730	12 83	27 3	128 3	273	1283	2730	12 83	27 3
TIME	μ sec.	μ sec.	μ sec.	μ sec.	μ sec.	μ sec.	μ sec.	μ sec.	μ sec.	m sec.	m sec.	m sec.	m sec.	m sec.	m sec.	sec.	sec.

7 - SEGMENT L.E.D. DISPLAY

The 7 - Segment Light Emitting Diode is one of the newer and more popular displays. The reasons for this popularity are: long life, low voltage requirements, ruggedness and the fact that it can be plugged into an I.C. socket. The symbol and code are shown in Fig. 8.

FIG. 8

SYMBOL	CODE
	All segments including the decimal point are common to pin 14. Pin 14 is normally connected to 5 volts DC. Each segment is then connected to ground through a 150 Ohm, 1/4 watt resistor and Decoder/Driver. The Decoder/Driver causes the proper segments to light to display a number. Caution: Do not try to light the display without using the 150 Ohm current limiting resistor, as the display will be ruined.

INTEGRATED CIRCUIT TIPS FOR TTL

1. The proper supply voltage is 4.75 to 5.25 volts and should never exceed 7 volts.
2. The voltage applied to an input should never exceed 5.5 volts.
3. The unused inputs of a NAND gate and the unused J, K, $\overline{\text{set}}$ and $\overline{\text{reset}}$ inputs of a flip-flop should be connected to a positive voltage of 2.4 to 5.5 volts maximum, through a 1,000 OHM resistor. Up to 35 inputs may be connected to one resistor.
4. The unused inputs of a NOR gate and the $\overline{J}$, $\overline{K}$, set, reset, clock and $\overline{\text{clock}}$ inputs of a flip-flop should all be connected to ground.
5. Unused gates and flip-flops should have all inputs connected to ground.
6. A 1-5 mfd,. 10 volt capacitor should be connected across the power supply line, at the point where the lines are connected to the board containing the integrated circuits. This will help to prevent any problems with line noise.
7. Connect one 0.01 mfd., 10 volt capacitor from Vcc to ground for every 8 integrated circuits. No integrated circuit should be more than 8 inches from a capacitor. This will help prevent high frequency noise problems.

PART NUMBERS AND DESCRIPTION

GC NUMBER	TTL NUMBER	DESCRIPTION
J4-1000	7400	Quadruple 2-Input Positive NAND Gate
J4-1002	7402	Quadruple 2-Input Positive NOR Gate
J4-1004	7404	Hex Inverter
J4-1010	7410	Triple 3-Input Positive NAND Gate
J4-1047	7447	BCD-to-Seven Segment Decoder/Driver
J4-1075	7475	Quadruple Bistable Latch
J4-1076	7476	Dual J-K Master-Slave Flip-Flop with Preset and Clear

GC NUMBER	TTL NUMBER	DESCRIPTION
J4-1090	7490	Decade Counter (Divide-by-Two and Divide-by-Five)
J4-1092	7492	Divide-by-Twelve Counter (Divide-by-Two and Divide-by-Six)
J4-1121	74121	Monostable Multivibrator
J4-1555	NE555	Timer

SOLDERING HINTS

1. Use a small soldering iron of 30 watts or less to solder transistors, diodes, SCR's, triacs and all integrated circuits.
2. Keep tip well tinned al all times. This is accomplished by melting rosin-core solder on the surface of the tip. Be sure the entire tip is tinned.
3. Just prior to use, clean the tip on a wet cellulose sponge.
4. Apply a small globule of rosin-core solder to the tip of the soldering iron.
5. Use this solder globule to heat the joint.
6. Apply rosin-core solder to the joint and not directly to the soldering iron tip. Do not heat joint longer than necessary. Apply only enough solder to cover the joint. The solder should not form a ball on the joint; this is usually an indication of insufficient heat.
7. Be sure the soldering iron tip is well tinned before it is returned to its' holder.

CONSTRUCTION HINTS

All of the projects in this handbook, with the exception of the Decade Counter, are constructed on perforated board (Calectro Cat. No. J4-601 and J4-602) using bread board terminals (Calectro Cat. No. J4-638.) The use of integrated circuit sockets (Calectro Cat. No. F2-998) is recommended, but not absolutely necessary. Terminals, components and wiring are shown in detailed drawings.

The selection of an enclosure is left to your discretion. Be sure that the enclosure is large enough to hold all of the necessary components. The enclosure that contains the power supply must be ventilated, as a considerable amount of heat is dissipated.

Do not attempt to use a large soldering iron, as the integrated circuits may be ruined.

For battery operation, "C" or "D" size nickel cadmium batteries are recommended. Four of these cells are connected in series to provide 4.8 volts DC. Each cell is rated at 1.2 volts.

Very small wire, such as No. 26 buss and teflon spaghetti tubing, will be easier to use than a larger wire size. Refer to the Calectro Handbook for hardware, chassis, sockets, etc.

POWER SUPPLY

This is a 5 volt, 1.4 Amp. regulated power supply capable of operating any of the projects in this handbook. Other projects requiring 5 volts DC at 1.4 Amps or less can also be operated by this supply.

The power transistor (Q1) must be mounted on a heat sink, such as Calectro Cat. No. K4-680 or to a metal cabinet if one is used. Mount the transistor with an insulation Kit (Calectro Cat. No. K4-650) and heat sink compound (Calectro Cat. No. K4-685).

Capacitor (C3) is only needed by the clock project when it is operated from 115 volts AC.

Refer to Fig. 1, 2, 3 and 4 for the component layout, schematic and wiring pictorial. All of the components not shown on the perferated board are mounted to a panel or chassis. Do not operate the power supply for extended periods of time without a load.

REGULATED POWER SUPPLY SCHEMATIC

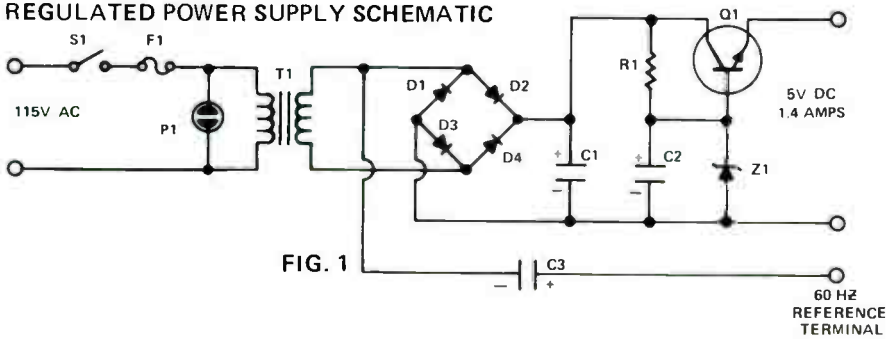


FIG. 1

POWER SUPPLY PARTS LIST

SYMBOL	QTY.	DESCRIPTION	CALECTRO CAT. NO.
S1	1	SPST Toggle Switch	E2-130
	1	Toggle Switch on/off Plate	E2-137
C1	1	2200 mf, 25 volt electrolytic capacitor	A1-134
C2	1	47 mf, 25 volt electrolytic capacitor	A1-129
C3	1	4.7 mf, 25 volt electrolytic	A1-126
F1	1	3AG2A Quick Acting Fuse	D2-132
	1	Fuse Holder	E2-495
P1	1	115 Volt Neon Lamp Assembly	E2-420
T1	1	12.6 V. AC, 2 AMP. Transformer	D1-747
	1	AC Line Cord	L3-717
R1	1	150 Ohm, 2 Watt Resistor GC Cat. No. 26-428	
Z1	1	6 Volt, 1 Watt Zener Diode	K4-560
Q1	1	NPN Silicon Power Transistor	K4-525
D1, D2, D3, D4	4	1 AMP., 50 Volt Silicon Diode	K4-555
	1	Heat Sink (see text)	K4-680

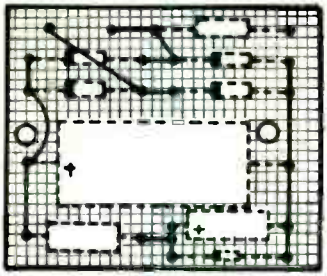


FIG. 2

POWER SUPPLY WIRING DIAGRAM

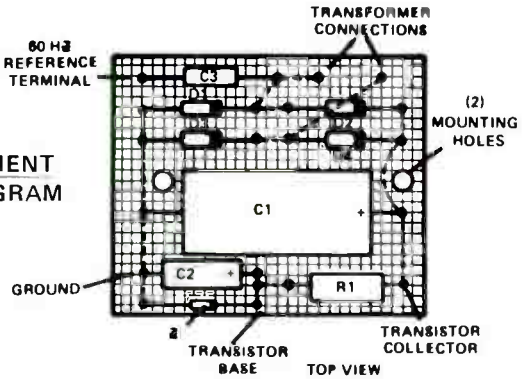
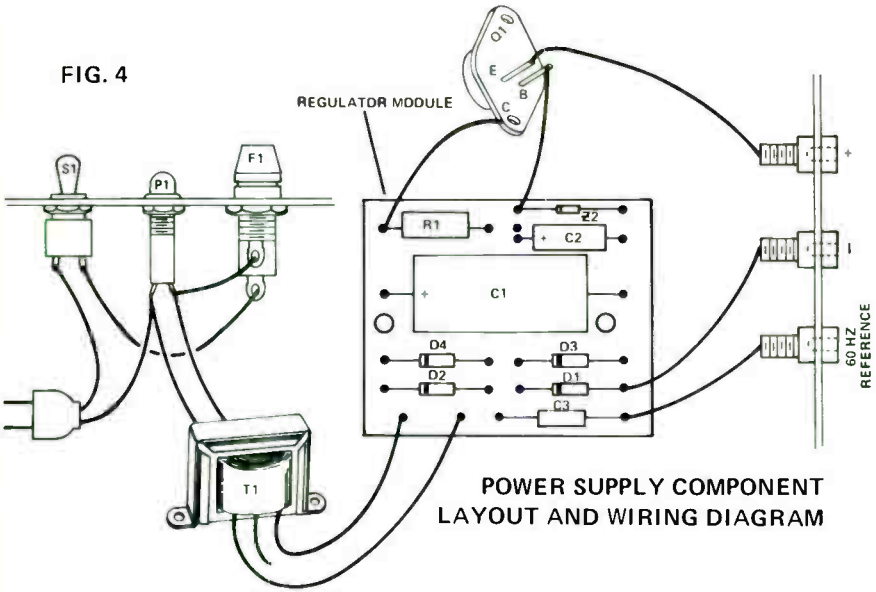


FIG. 3

POWER SUPPLY COMPONENT LAYOUT & WIRING DIAGRAM

FIG. 4



POWER SUPPLY COMPONENT LAYOUT AND WIRING DIAGRAM

DIGITAL TEST PROBE

This piece of test equipment is a very useful device for trouble shooting digital equipment. It does not require a battery or power supply, as it is connected directly to the equipment being checked.

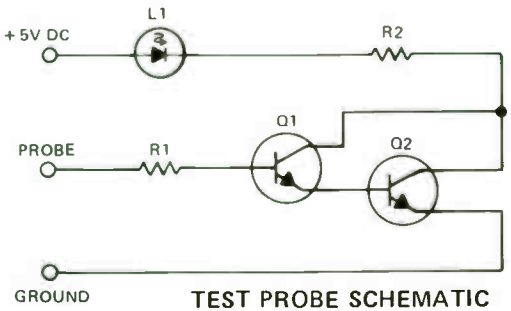
The probe can be built into a plastic tube with the L.E.D. lamp mounted on one end and a nail may be used as a probe on the other end. The plastic tube, from a GC Electronics Pen Oiler (Cat. No. 984), makes an excellent probe.

Connect the positive lead from the probe to a positive 5 volt DC terminal of the equipment to be checked and the negative lead to a ground terminal.The tip of the probe is then touched to the various inputs and outputs to determine if they are "on" or "off". If the lamp lights, this is an indication that the terminal is in an "on" condition, if it does not, then it is in an "off" condition.

PARTS LIST

SYMBOL	QTY.	DESCRIPTION	CALECTRO CAT. NO.
Q1, Q2	2	NPN Silicon Transistor	K4-507
R1	1	27,000 OHM, 1/2 watt resistor	B1-401
R2	1	150 OHM, 1/2 watt resistor	B1-374
L1	1	L.E.D. Lamp	K4-559
	1	GC Cat. No. 984 Pen Oiler	
	2	Jumper Wires	J4-650

FIG. 1



TEST PROBE SCHEMATIC

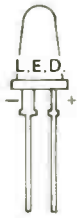
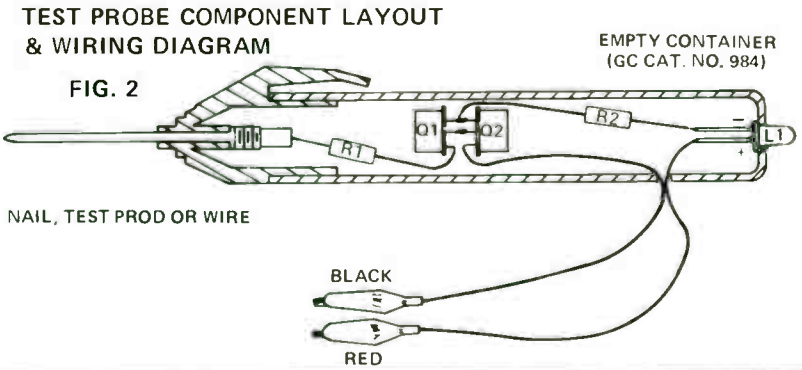


FIG. 3

TEST PROBE COMPONENT LAYOUT & WIRING DIAGRAM

FIG. 2



DECADE COUNTER

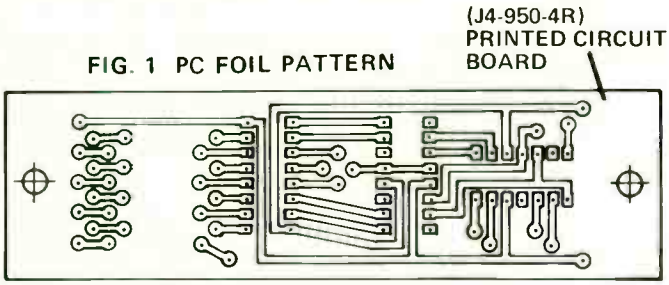
The assembly instructions are based on the assumption that the decade counter kit (Calectro Cat. No. J4-950) is used. Although the counter can be constructed on a perforated board with miniclips, it is recommended that the counter be built using the printed circuit board included with the kit.

Refer to the projects listed in the contents to determine the number of decade counters that are required for the particular project of interest.

DECADE COUNTER ASSEMBLY INSTRUCTIONS

1. Drill printed circuit board (Fig. 1) using a number 60 drill.

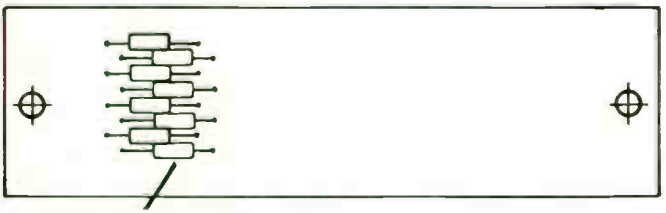
FIG. 1 PC FOIL PATTERN



DOTS INDICATE HOLES TO BE DRILLED

2. Bend and insert (8) 150 OHM, 1/4 watt resistors (Fig. 2) and solder to P.C. board. Clip off excess wire.

COMPONENT SIDE OF BOARD



(J4-975) 8-150 OHM, ¼ WATT RESISTORS

FIG. 2 RESISTOR POSITIONS

3. Insert and solder the integrated circuits (Fig. 3).

COMPONENT SIDE OF BOARD

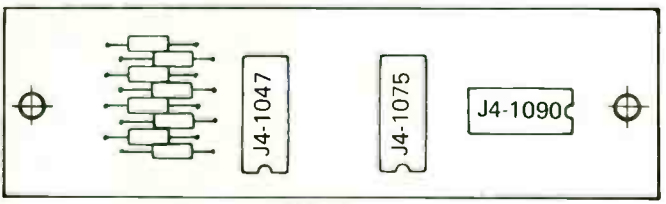


FIG. 3
IC POSITIONS

4. Remove seven pins from the I.C. socket (Calectro Cat. No. F2-998) (Fig. 4). Remove pins indicated by black dots.

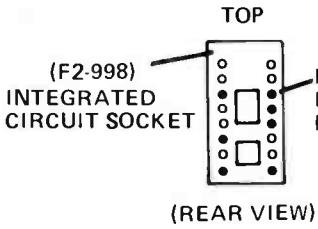


FIG. 4
REMOVE SEVEN
PINS FROM SOCKET

5. Cut 9 pieces of insulated solid wire one inch long. Remove 1/4 inch of insulation from both ends.
6. Solder one wire to each I.C. socket pin.
7. Solder the opposite end of each wire to the P.C. Board. (Fig. 5 & 6)

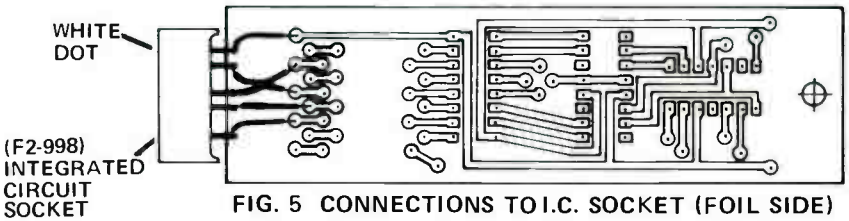


FIG. 5 CONNECTIONS TO I.C. SOCKET (FOIL SIDE)

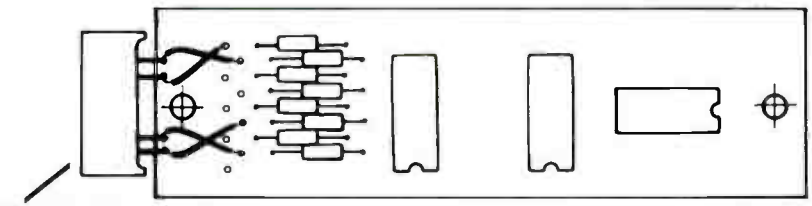


FIG. 6 CONNECTIONS TO I.C. SOCKET (COMPONENT SIDE)

8. Insert L.E.D. display into socket. (Fig. 7)

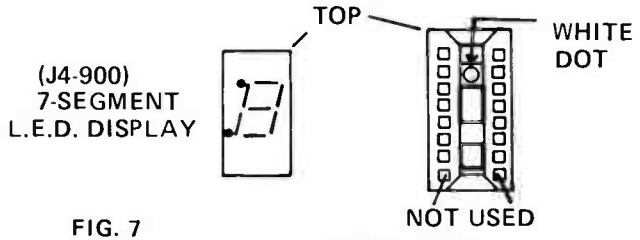
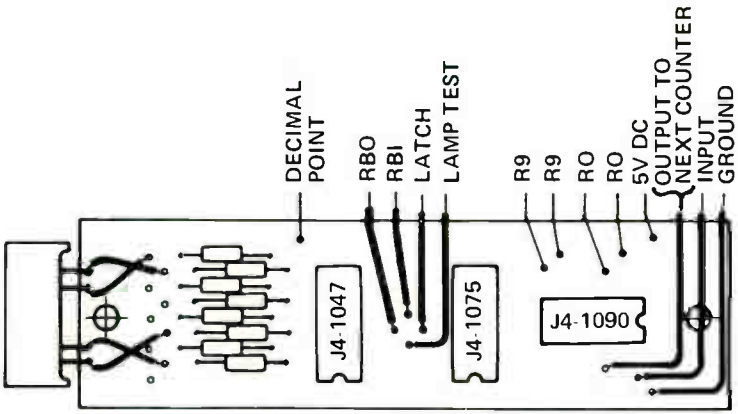


FIG. 7
L.E.D. DISPLAY

FRONT VIEW

9. Cut, strip insulation and solder interconnecting wires as shown in Fig. 8. If some other method of mounting and wiring is used, skip this step.



COMPONENT SIDE

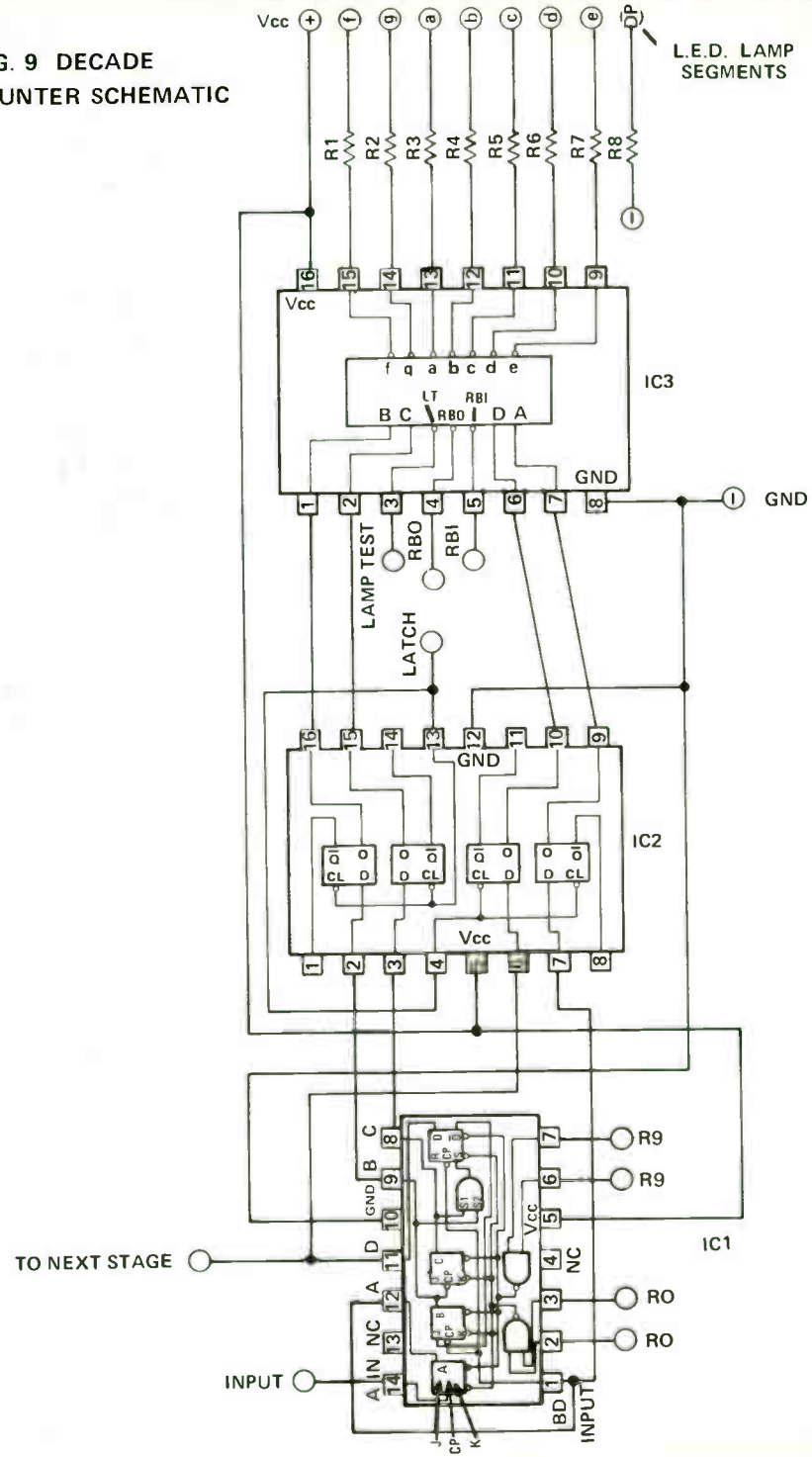
FIG. 8 INTERCONNECTING WIRES

10. Test assembly as follows: Connect terminal marked VCC to the positive terminal of a 5 volt supply. Connect the ground terminal to the negative terminal of the 5 volt supply. Connect one of the R0 and one of the R9 terminals to the ground terminal. Turn on the power supply, take the input wire and touch it to the ground terminal. Each time the input is grounded, some random number should appear on the readout. Next, ground the lamp test terminal and the number eight should appear. If the counter should fail to function properly, check for bad solder joints or improper wiring.

DECADE COUNTER PARTS LIST

SYMBOL	QTY.	DESCRIPTION	CALECTRO CAT. NO.
I.C. 1	1	Decade Counter	J4-1090
I.C. 2	1	Latch	J4-1075
I.C. 3	1	Decoder/Driver	J4-1047
R1 - R8	8	150 OHM, 1/4 watt resistors	J4-975
	1	16 Pin I.C. Socket	F2-998
	1	P.C. Board	J4-950-4R
L1	1	7-Segment L.E.D. Display	J4-900

FIG. 9 DECADE COUNTER SCHEMATIC



LINE FREQUENCY TIME BASE

This project provides a source of timing pulses from a standard 60 HZ line voltage, such as that used in your home. This circuit first changes the shape of the wave form from the normal sine wave to the necessary square wave needed to operate digital circuits. The circuit then divides the 60 HZ by 6, giving us 10 HZ, then it is divided again by 10, giving us 1 pulse per second which can be used to control a clock, stop watch or frequency counter etc. The input to the time base can be connected to a 6 or 12 volt transformer or the 60 HZ reference terminal on the power supply project.

LINE FREQUENCY TIME BASE PARTS LIST

SYMBOL	QTY.	DESCRIPTION	CALECTRO CAT. NO.
R1,R2	2	470 ohm, 1/2 Watt Resistor	B1-380
C1	1	10mf, 25 volt Electrolytic Capacitor	A1-127
C2	1	.01mf, 50 volt Disc. Capacitor	A1-029
C3	1	.1mf, 50 volt Disc. Capacitor	A1-032
Z1	1	4.7 volt 1 Watt Zener	
D1	1	50 Volt 1 Amp Silicon Diode	K4-555
IC1	1	Quad 2-Input Nand Gate	J4-1000
IC2	1	÷6 counter	J4-1092
IC3	1	÷10 counter	J4-1090

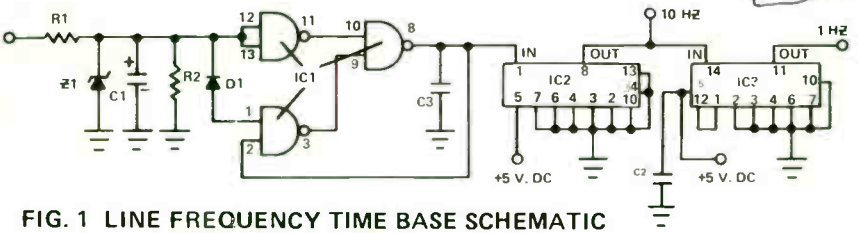
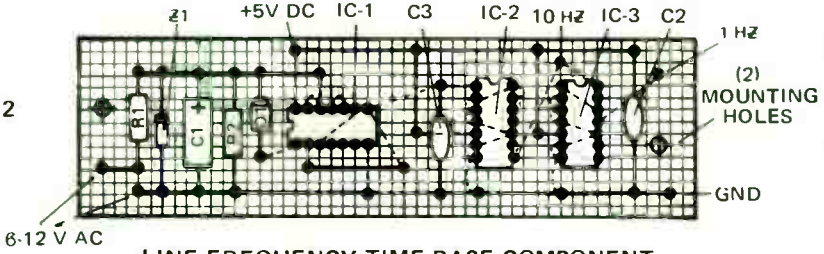


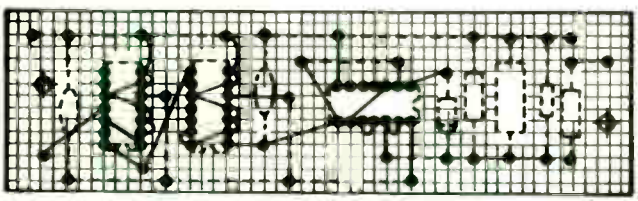
FIG. 1 LINE FREQUENCY TIME BASE SCHEMATIC

FIG. 2



LINE FREQUENCY TIME BASE COMPONENT LAYOUT & WIRING DIAGRAM

FIG. 3
BOTTOM VIEW



LINE FREQUENCY TIME BASE COMPONENT LAYOUT & WIRING DIAGRAM

ELECTRONIC DICE PROJECT

Electronic dice simulate, by means of logic circuit elements, the probability patterns of an actual pair of dice. TTL integrated circuits, along with light emitting diodes, are used exclusively in this dice project. A single J4-1000, 2 input NAND gate operates as a clock and waveshaping circuit at approximately 55 KHZ. This drives a divide-by-six "walking ring counter" consisting of one and one-half J4-1076 J-K flip-flops, which in turn drives a second divide-by-six counter. Each of these counters is decoded by one J4-1000 gate and one J4-1004 hex inverter, which directly drive seven L.E.D.'s, through current limiting resistors, for each die. An extra J4-1010 gate is used to automatically clear the counters of a "disallowed" state which can occur upon the initial application of power to the logic elements.

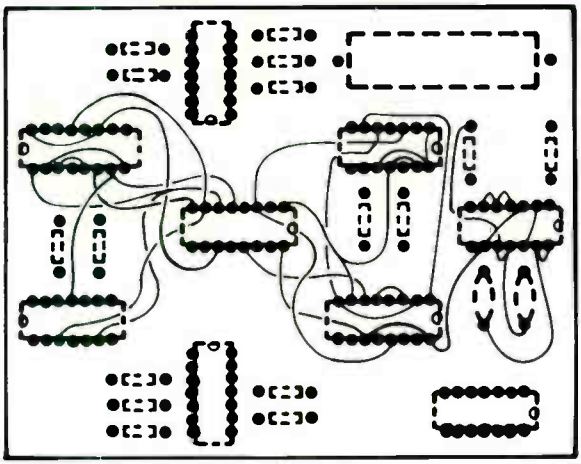
Note when making connections to the L.E.D.'s that the negative lead is thicker where it exits the molded bulb, than the positive lead. If you are not sure, wire them in and try them. They cannot be damaged with the 150 OHM series resistor on a 5 volt supply. If they do not light when trying to "throw" the dice, reverse the leads to the L.E.D.

An N4-065, 6 volt DC, 300 mA., or the 5 volt power supply project in this handbook will power the dice project. Note: If you want to observe the sequence of operation of the dice, connect a pair of 47 mfd electrolytic capacitors across the .01 disc capacitors (polarity is unimportant) to slow down the oscillator. You will be able to observe the dice cycling 1, 3, 5, 6, 4, 2, 1 etc.; one going through all six "spots" for each "spot" change of the other. This simulates a true pair of dice, which when thrown, simulate a 36-sided die!

BILL OF MATERIALS

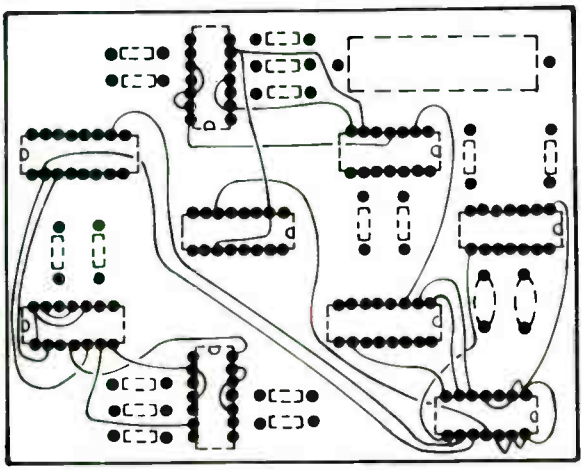
COMPONENT	CAT. NO.	DESCRIPTION
IC7, 8, 9	J4-1076	7476 IC
IC1, 2, 3	J4-1000	7400 IC
IC4, 5	J4-1004	7404 IC
IC6	J4-1010	7410 IC
LED-1 thru LED-14	K4-559	Light Emitting Diode
R1 thru R14	J4-975	150 ohm, 1/4 watt resistors, 8 per package
R15, R16	B1-380	470 ohm, 1/2 watt resistors
C1	A1-132	470 mfd 25V capacitor
C2, C3	A1-029	.01 mfd disc ceramic capacitors
SW-1	E2-141	N. O. momentary contact push button switch
J-1	F2-846	2.5 mm Jack
1	J4-726	Instrument Box
1	N4-065	6 volt 300 ma power supply
9	F2-998	IC Sockets (optional)
R17	B1-465 (4 needed)	100 ohm, 1 watt resistors, connected in parallel

FIG. 1 ELECTRONIC DICE WIRING DIAGRAM



BOTTOM VIEW

FIG. 2 ELECTRONIC DICE WIRING DIAGRAM



BOTTOM VIEW

REAR VIEW

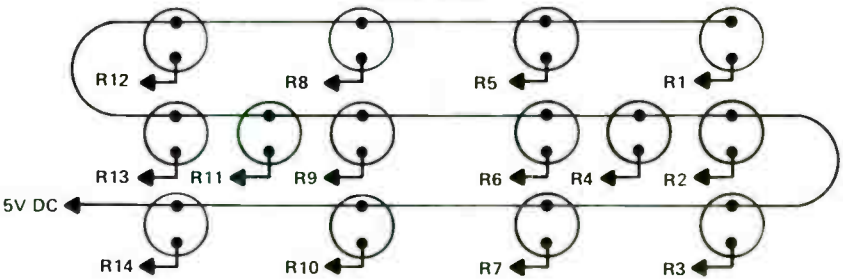
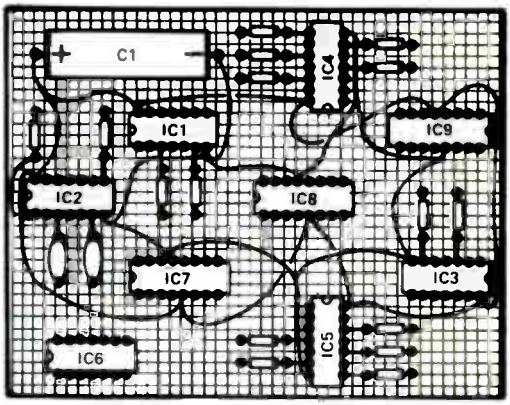


FIG. 4 ELECTRONIC DICE WIRING DIAGRAM



TOP VIEW

FIG. 3 ELECTRONIC DICE COMPONENT LAYOUT & WIRING DIAGRAM

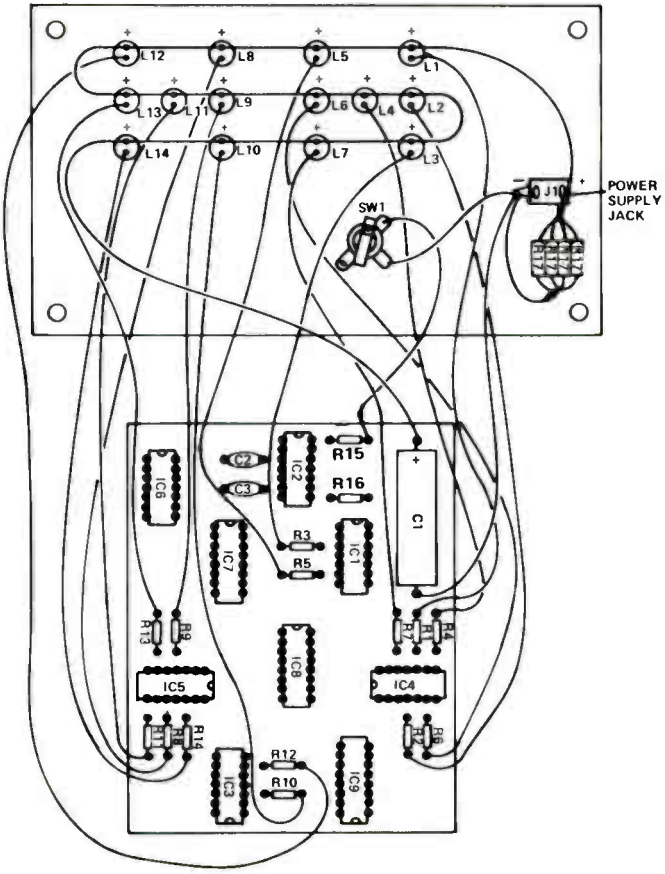
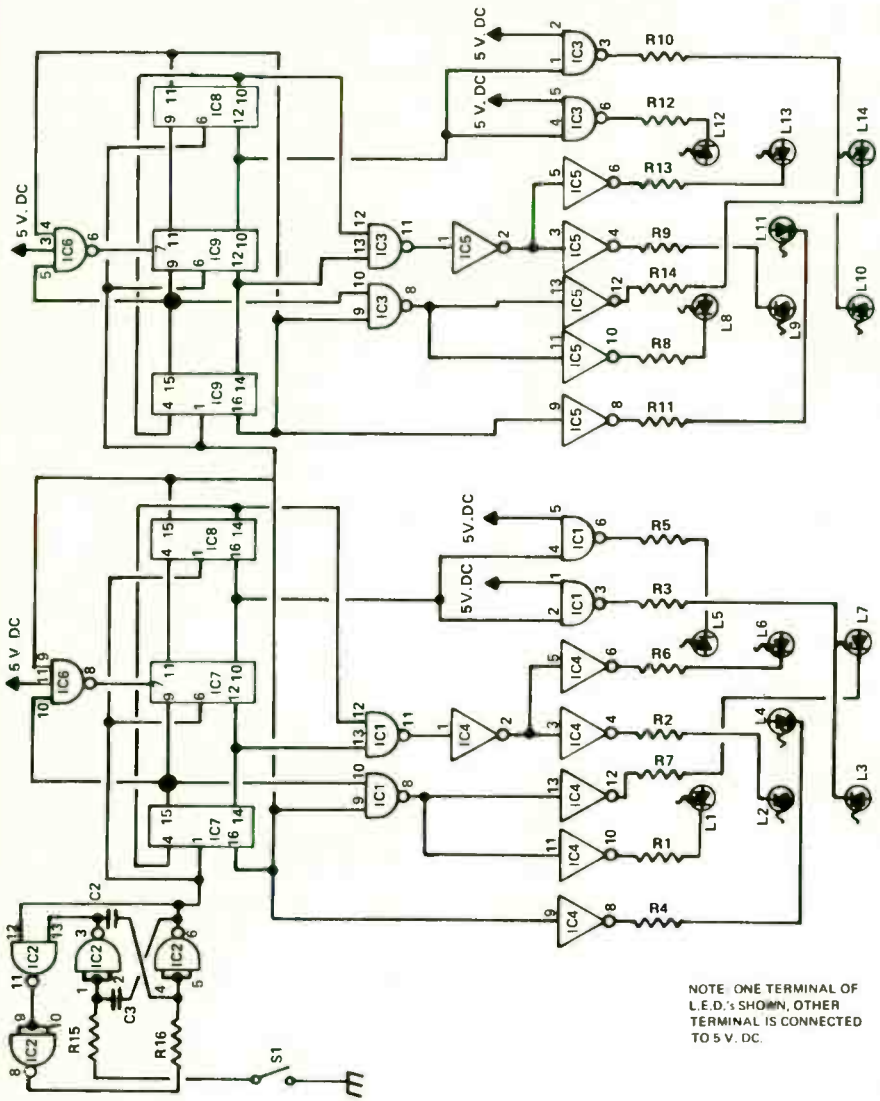


FIG. 5 ELECTRONIC DICE SCHEMATIC



NOTE: ONE TERMINAL OF L.E.D.'s SHOWN, OTHER TERMINAL IS CONNECTED TO 5 V. DC.

IC BURGLAR ALARM PROJECT

Two integrated circuits using timing logic form the basis for this IC burglar alarm project. All components, including the reed switch, may be mounted on a single piece of 4" x 4" perforated board. The entire alarm can then be mounted near the door or window you will be protecting. The alarm features an adjustable entry delay of from 2 seconds to 30 seconds, with the components shown, via R2.

Circuit operation is as follows: IC-1 is triggered "on" by the reed switch. IC1 then acts as a timer allowing a person time to turn the alarm "off". If the alarm has not been turned "off" in 2 to 30 seconds, IC1 then triggers IC2 "on". IC2 then turns the alarm "on" for a predetermined length of time, after which it will shut itself "off", via R4.

The alarm is designed to operate from +9 volts down to +6 volts, to allow for battery wear. Approximately 30 ma is drawn at +9 volts with the alarm in service, guarding a door or window. Six flashlight cells will operate the alarm for approximately 18 days (based upon the use of Eveready No. 950 "D" cells on an 8 hour per day basis) minimum. You will actually get a longer usage, as the figure shown is conservative. An N4-065 power supply set for 9 volts, connected across the batteries will give indefinite operating time.

External sounding devices, such as the Audiotex 30-9110 horn, 30-9100 bell or 30-9120 siren may be connected between the battery – and the N.O. relay contact. The reed switch may be mounted at the end of several feet of wire, but the wire must be a twisted pair. Do not use shielded wire. If erratic tripping of the alarm occurs, use a shorter wire between the reed switch and the alarm board. Be sure to provide some method for disconnecting the battery from the alarm when entering the protected room so that you can shut the alarm off before IC-1 (entry delay) times out.

BILL OF MATERIALS

COMPONENT	CAT. NO.	DESCRIPTION
R1	B1-396	10 Kohm, 1/2 watt resistor
R2	B1-645	50 Kohm potentiometer
R3	B1-374	150 ohm, 1/2 watt resistor
R4	B1-648	500 Kohm potentiometer
R5	B1-394	6.8 Kohm, 1/2 watt resistor
R6	B1-386	1.5 Kohm, 1/2 watt resistor
R7	B1-404	47 Kohm, 1/2 watt resistor
R8	B1-400	22 Kohm, 1/2 watt resistor
R9	B1-400	22 Kohm, 1/2 watt resistor
C1	A1-108	47 uf/12 volt electrolytic
C2	A1-032	0.1 uf disc ceramic cap.
C3	A1-026	.001 uf disc ceramic cap.
C4	A1-132	470 uf/25 volt electrolytic
C5	A1-112	220 uf/12 volt electrolytic
C6	A1-110	100 uf/12 volt electrolytic
C7	A1-029	.01 uf disc ceramic cap.
IC-1	J4-1121	74121 Monostable Multivibrator
IC-2	J4-1555	555 Timer
Q1	K4-506	NPN Silicon Transistor
Ry1	D1-966	6 volt DC relay
S1	E2-157	Reed Switch
Z1	K4-560	6 V.Zener Diode

FIG. 1 BURGLAR ALARM COMPONENT LAYOUT

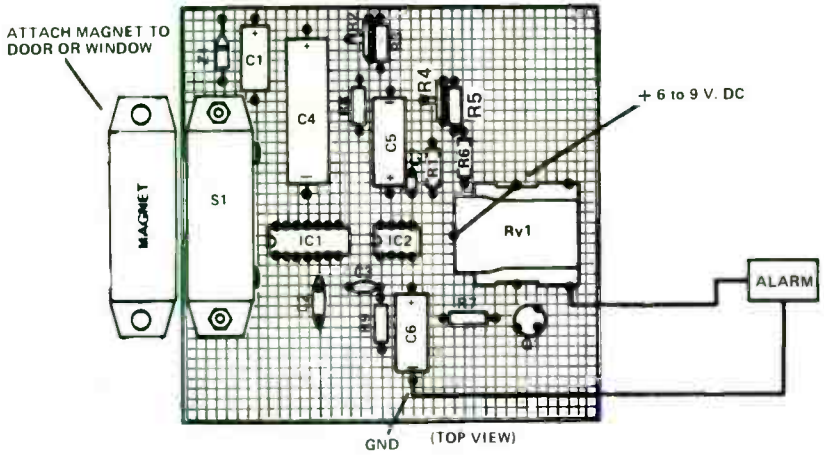


FIG. 2 BURGLAR ALARM SCHEMATIC

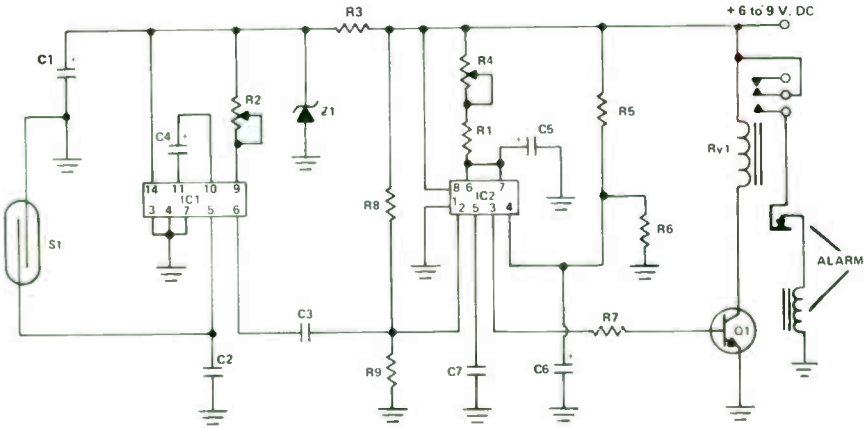
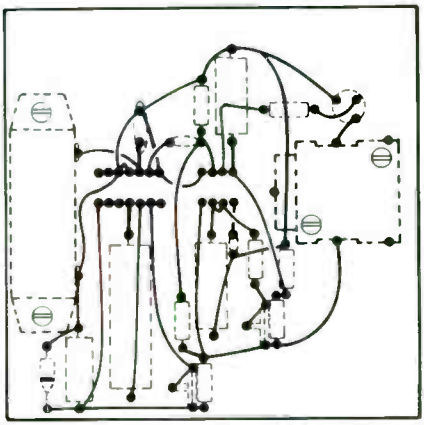


FIG. 3 BURGLAR ALARM WIRING DIAGRAM



DIGITAL CLOCK PROJECT

Construct your own digital clock with the components in the Calectro line by following the layouts shown here. Two different time bases may be used for this clock, the 60 Hz base or the 100 Khz base; the 60 Hz is shown in this booklet. There is sufficient room on the clock board for the 60 Hz time base, and wiring is shown for this base (refer to the article on this base for the components).

The digital clock features 12 or 24 hour readout, pushbutton advance of the minutes and hours, and a switch to stop the seconds for exact synchronization with another clock or WWV. The 60 Hz base is as accurate as your conventional clock; the power line has a maximum error at any given moment of 0.005%, which is corrected over a period of time to give a resultant zero error.

Circuit description: IC-13 receives the 1 Hz output from the time base and gates it on and off with command from the "seconds stop" switch. The 1 Hz pulse is fed to IC-7 which is a divide-by-ten circuit with Binary Coded Digit (BCD) output. This output feeds IC-1 which converts BCD signals to 7-segment display output. IC-1 contains, in addition to it's logic circuitry, 7 transistors which when turned on connect the LED display lamp segments to ground through the lamp protective resistors R-1 thru R-42. Therefore, IC-1 thru IC-6 may be expected to run somewhat hotter than the other IC's. This is normal. Pin 11 of IC-7 (part of the BCD output) delivers to IC-8 a negative going pulse after the numeral 9 is displayed, which advances IC-8 by one digit. IC-8 is a divide-by-six circuit, whose BCD output is decoded by IC-2 to display the numerals 0 thru 5. After 5, a negative going pulse is sent from pin 9 of IC-8 to IC-9 for minutes display, etc. IC-7, 9 and 11 are all divide-by-10; IC-8, 10 and 12 are divide-by-six. IC-11 and IC-12 must generate BCD outputs which generate numerals that do not reset to zero after "10" but go on to 11 and 12 and then reset to 01 rather than 00. A description of how this works follows.

IC-13 is wired in part to form a 3-input AND gate (all three inputs must be logic-1 to give a logic-1 output). The output of this gate resets IC-11 and IC-12 back to numeral 0 output. This will occur only when the A output (see data sheets for the ABCD decoding of the BCD outputs) of IC-12 is logic-1 corresponding to the numeral 1 in the displayed figure "12", and when the B output of IC-11 is logic-1 corresponding to the numeral 2 in figure "12", and when the A output of IC-11 just goes to logic-1 (in an attempt to display the figure "13"). At this moment in time, the AND circuit activates the resets, returning IC-11 and IC-12 to zero, which in turn shuts off the inputs to the AND circuit and shuts off the reset pulse before the above mentioned A output of IC-11 completely obtains the logic-1 level, thereby not interfering with this function and letting the A output complete its' state change to give a logic-1 output, or to display the numeral "01". The capacitor coupling between IC-10 and IC-11 is necessary to hold a charge during the above operations.

Pushbutton advancement of the minutes and hours is accomplished by "processing" the buttons with a pair of R-S flip-flops, using IC-14 to remove the bounce, and sending the resultant pulses thru capacitors to the inputs of IC-9 and IC-11.

Alternate wiring of IC-11, 12 and 13 is shown on the wiring diagram for 24 hour display.

DIGITAL CLOCK PROJECT PARTS LIST

SYMBOL	QTY.	DESCRIPTION	CALECTRO CAT. NO.
L1,L2,L3 L4,L5,L6 IC1,IC2,IC3	6	7 Segment L.E.D. Display	J4-900
IC4,IC5,IC6	6	Decoder Driver	J4-1047
IC7,IC9,IC11	3	Divide-By-Ten Counters	J4-1090
IC8,IC10,IC12	3	Divide-By-Twelve Counters	J4-1092
IC13	1	3-Input NAND Gate	J4-1010
IC14	1	2-Input NAND Gate	J4-1000
C1,C2	2	.05 mf, 50 Volt Disc. Capacitor	A1-031
C3,C4	2	.001 mf, 50 Volt Disc. Capacitor	A1-026
C5,C6	2	10 mf, 25 Volt Electrolytic Capacitor	A1-027
C7	1	.1 mf, 25 Volt Disc. Capacitor	A1-032
R43,R44	2	10K OHMS, 1/2 Watt Resistor	B1-396
R45	1	1K OHMS, 1/2 Watt Resistor	B1-384
R1- thru R42	42 (6 pkg.)	150 OHM, 1/4 Watt Resistor	J4-975
SW1	1	SPST Toggle Switch	E2-116
SW2,SW3	2	SPDT Momentary Switch	E2-141

FIG. 1 CLOCK SCHEMATIC

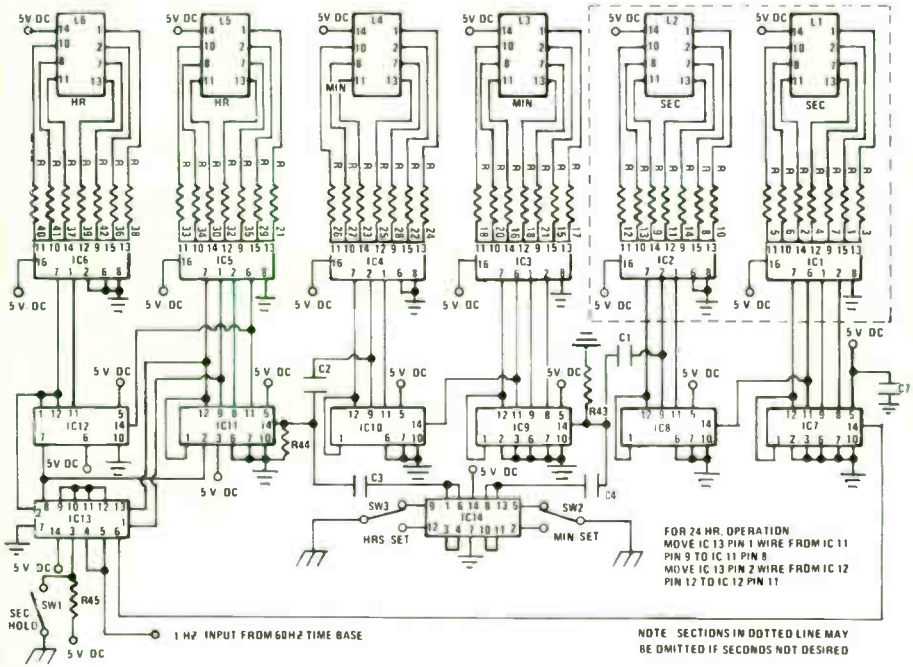


FIG. 2 CLOCK COMPONENT LAYOUT

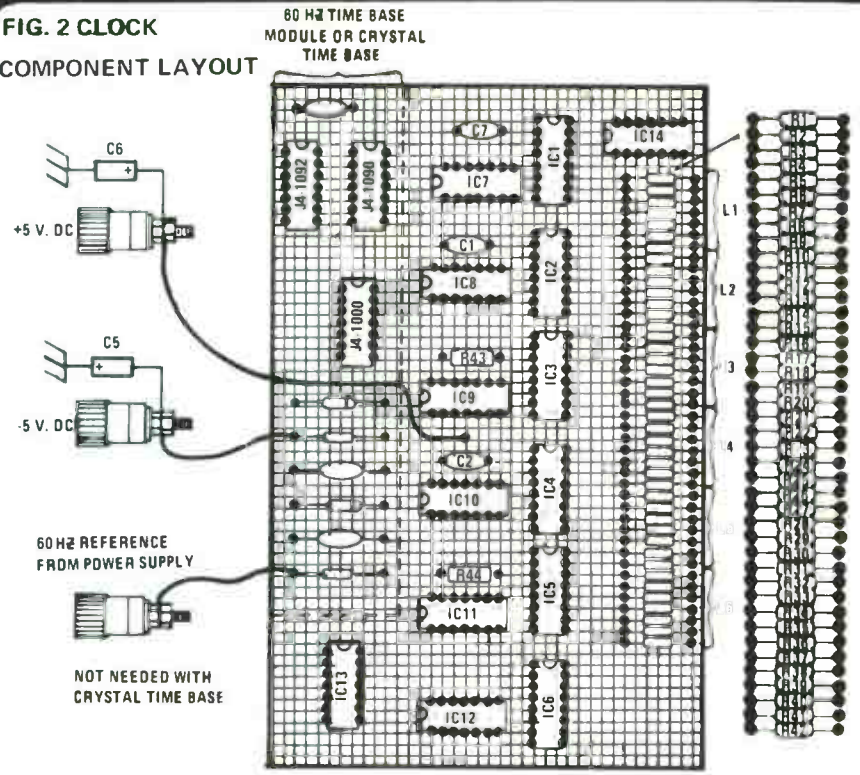
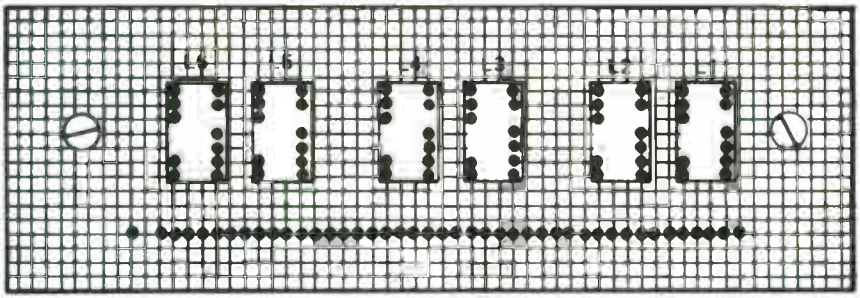


FIG. 3 CLOCK COMPONENT LAYOUT (DISPLAYS)



(FRONT VIEW)

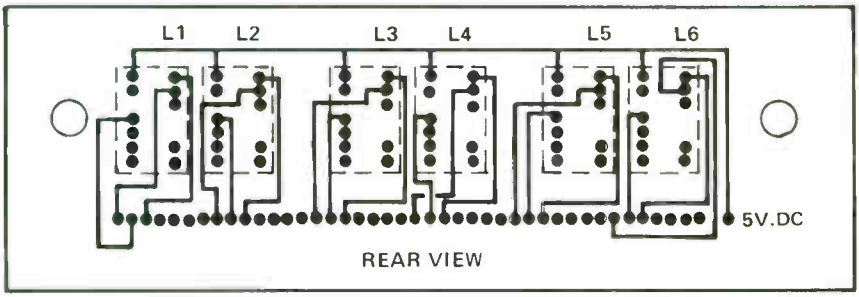
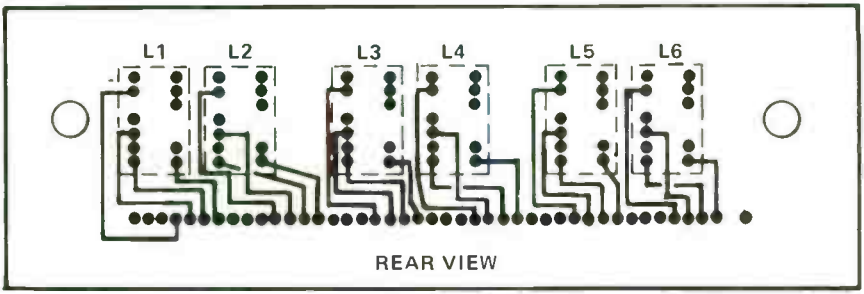


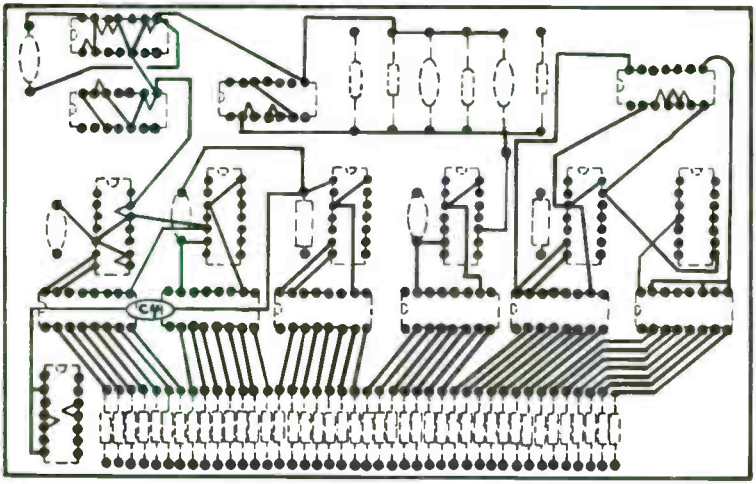
FIG. 4 CLOCK DISPLAY WIRING DIAGRAM

FIG. 5 CLOCK DISPLAY WIRING DIAGRAM



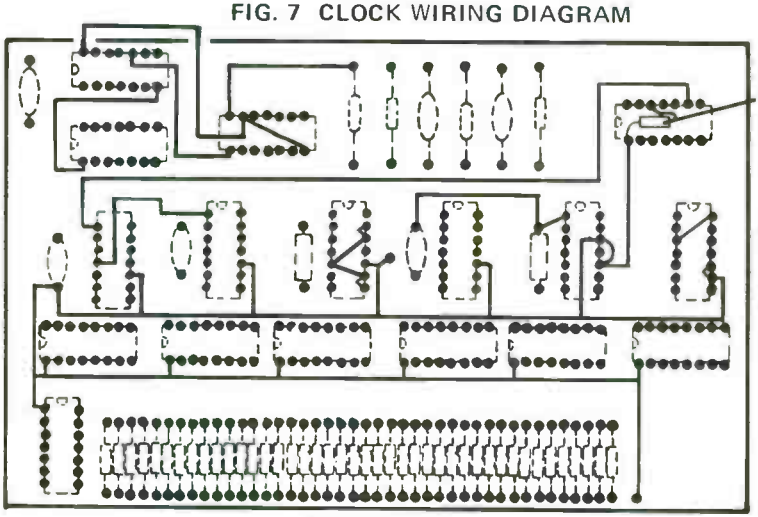
REAR VIEW

FIG. 6 CLOCK WIRING DIAGRAM



(BOTTOM VIEW)

FIG. 7 CLOCK WIRING DIAGRAM



(BOTTOM VIEW)

FIG. 8 CLOCK WIRING DIAGRAM

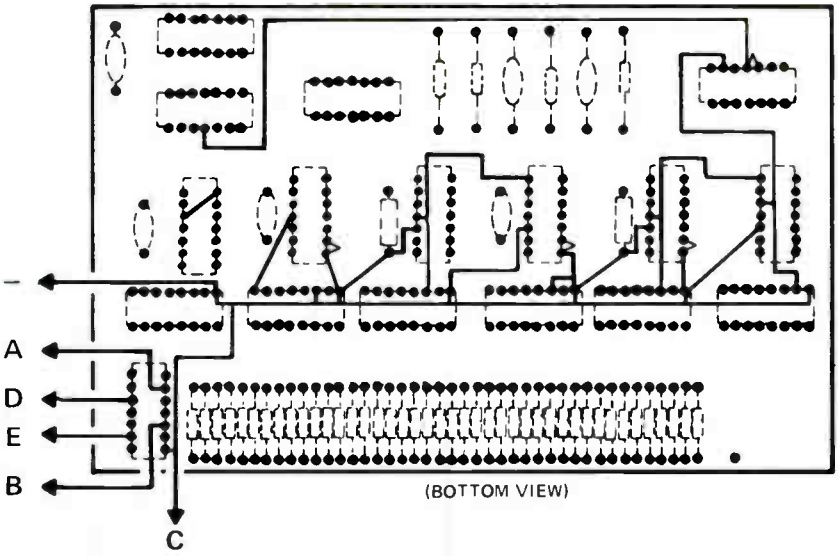


FIG. 9 CLOCK WIRING DIAGRAM

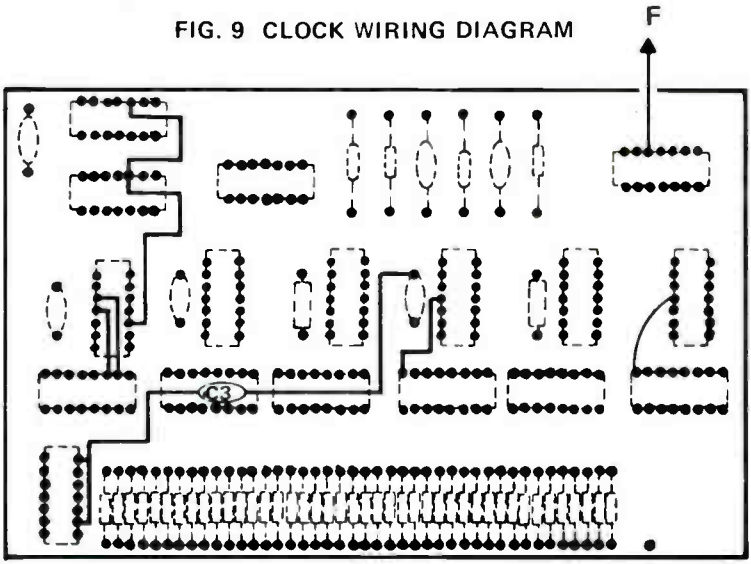
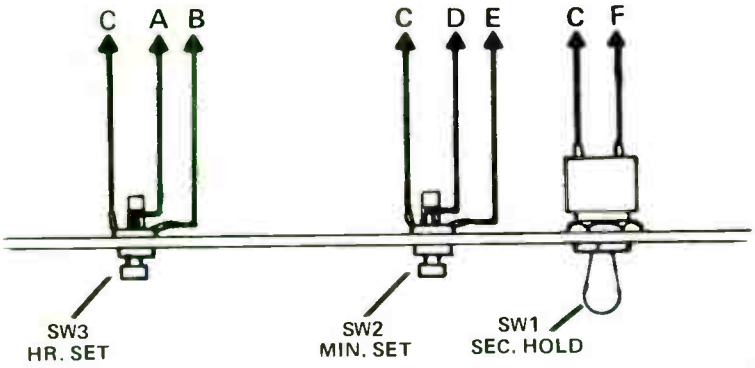


FIG. 10 CLOCK COMPONENT LAYOUT (SWITCHES)



(TOP VIEW)

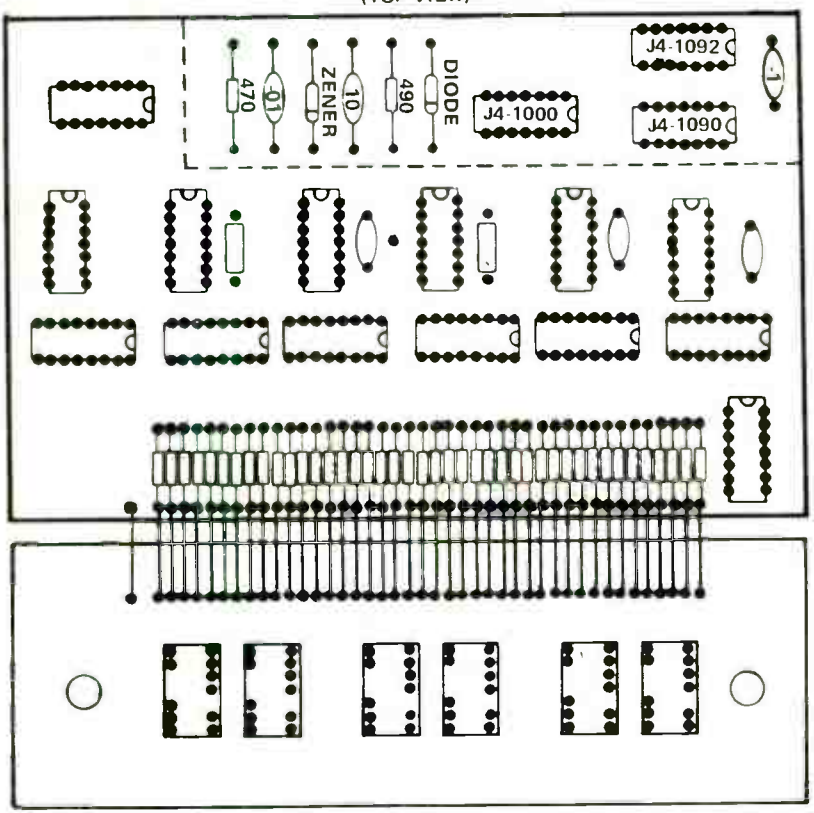


FIG. 11 CLOCK WIRING DIAGRAM

INTEGRATED CIRCUIT TIMER

Have you ever had to turn on a yard, porch or garage light and then try to remember to turn it off later? Or to turn off a battery charger to prevent overcharging? You probably have had many instances where you could have used a timer, either to turn an electrical device on or off, sometime later. There are other circuits available to build a timer, but this circuit is one of the most advanced. It uses a newly designed integrated circuit.

The timer can be started with push button (SW3) and reset with push button (SW2). The length of time it take s to turn a device off or on is set with a variable resistor (R1). There are two outlets available -- one is normally on and will turn off when the timer shuts off. The other outlet is normally off and will turn on when the timer shuts off. Momentarily pushing the reset button causes the timing cycle to start over. If the output terminals are connected across SW3 and SW2, the timer can be turned on or reset by remote control by using either a momentary push button switch or a relay activated by a photo cell, etc. Digital pulses from other circuits can be used to trigger the time to start or reset. A .001 uf., 50 volt capacitor (Cat. No. A1-026) must be used to couple the pulses to the trigger and reset terminals.

Follow the construction methods suggested previously. Refer to Fig. (1, 2, 3, 4), for parts layout and schematic diagram. Fig. (5) is a cutout to be glued to the panel. It is placed over the shaft of R1 before the hex nut is put on and tightened. To calibrate, plug an electrical clock into the normally on outlet, set the pointer knob to the first calibration line on the dial, set the clock to any convenient setting, push the start button on the timer. When the timer shuts off the clock, note the time indicated on the clock and mark the dial accordingly. Repeat the process for each calibration point on the dial. The maximum length of time is determined by R1 and C2 and can be made shorter by decreasing the values of R1 and/or C2 or longer by increasing them. The value used for R1 and C2 in the parts list gives over a three hour time interval. Any electrical device requiring less than three amps can be connected directly to the timer.

TIMER PARTS LIST

SYMBOL	QTY.	DESCRIPTION	CALECTRO CAT. NO.
T1	1	12.6 V AC Sec., 115 V AC Pri. Transformer	D1-750
SW1	1	SPST Toggle Switch	E2-119
SW2, SW3	2	SPST Momentary Contact Switch	E1-140
F1	1	3 AG 1/4A Quick Acting Fuse and E2-495 Fuseholder	D2-120
PL1	1	115 V AC Neon Lamp Assembly	E2-420
D1, D2, D3	3	50 PIV, 1 Amp Silicon Diode	K4-555
C1	1	470 mf, 25 V Electrolytic Capacitor	A1-132
C2	1	2200 mf, 25 V Electrolytic Capacitor	A1-134
C3	1	.01 mf, 50 volt Disc. Capacitor	A1-027
R1	1	5 MEGOHM Linear Taper Pot.	B1-693
R2, R3	2	27K OHMS, 1/2 Watt Resistor	B1-401
R4	1	220 OHM, 1/2 Watt Resistor	B1-376
RY1	1	6 V. DC Relay	D1-966
IC1	1	Integrated Circuit Timer	J4-1555

FIG. 1 TIMER SCHEMATIC

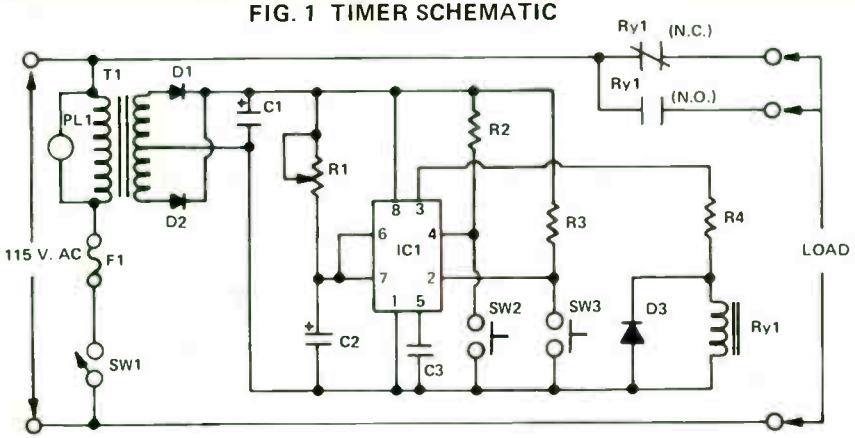


FIG. 2 TIMER COMPONENT LAYOUT & WIRING DIAGRAM

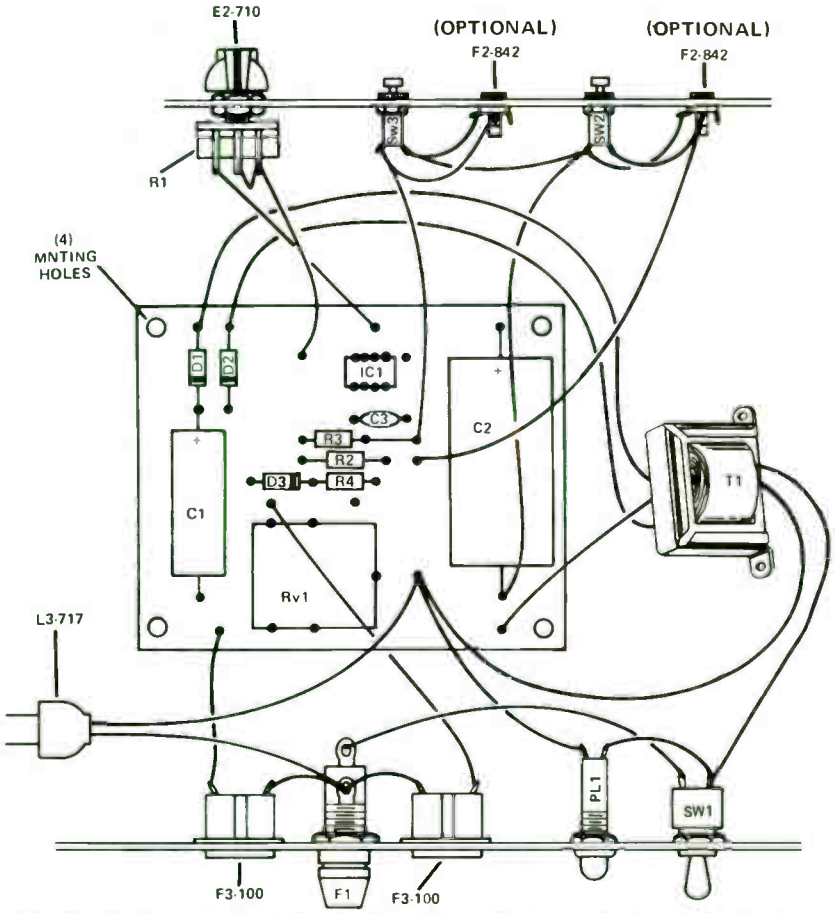
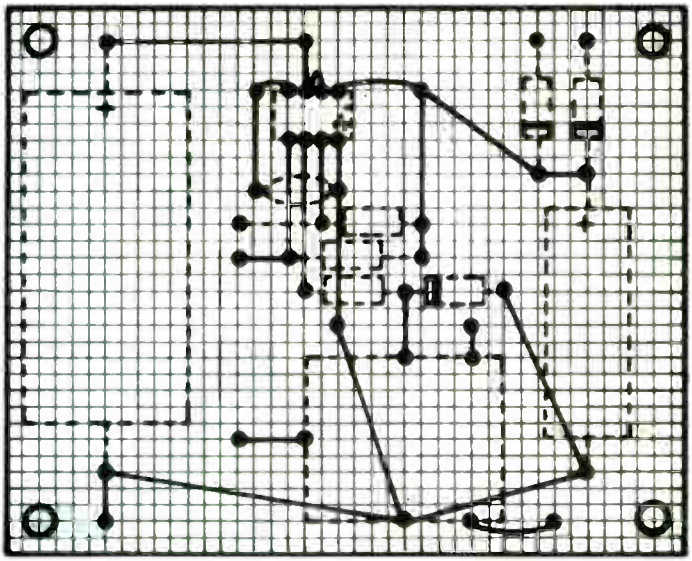


FIG. 3 TIMER WIRING DIAGRAM



BOTTOM VIEW

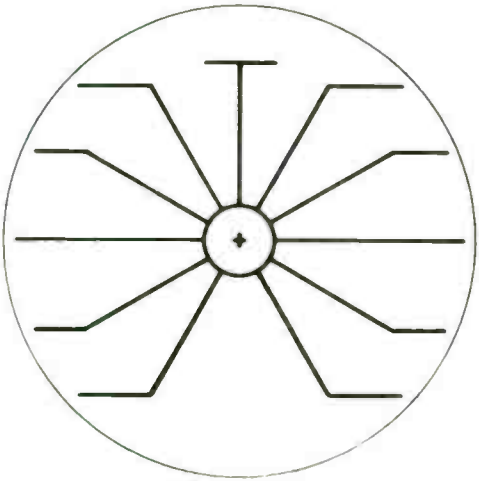
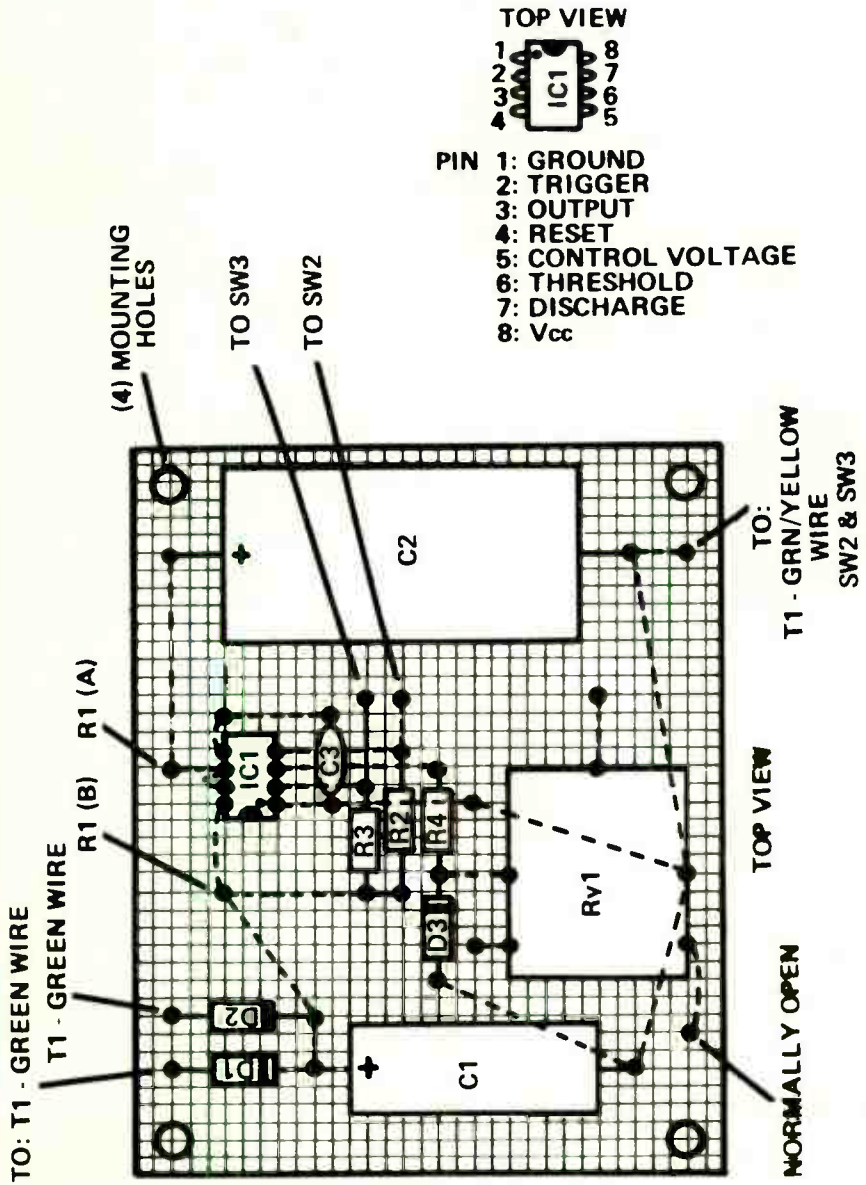


FIG. 5
TIMER DIAL FACE PLATE

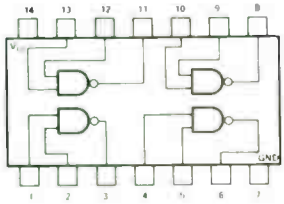
FIG. 4 TIMER COMPONENT LAYOUT



QUADRUPLE 2-INPUT POSITIVE NAND GATE

J4-1000

PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, T_A	0	25	70	C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400μA	V_{in} = 0.8V,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			40	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		−18		−55	mA

PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		14	27	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		8	16	mA

SWITCHING CHARACTERISTICS, Vcc = 5 V., $T_A = 25^{\circ}$ C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF	R_L = 400Ω		12	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

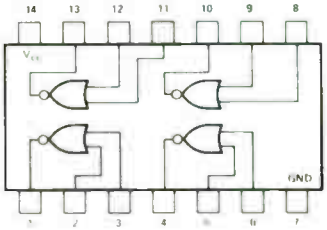
** All typical values are at V_{CC} = 5V, T_A = 25°C

† Not more than one output should be shorted at a time.

QUADRUPLE 2-INPUT POSITIVE NOR GATE

J4-1002

PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, T_A:	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			40 1	μA mA
I_{OS}	Short circuit output Current†	V_{CC} = MAX		-18		-55	mA

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		4	8	mA

SWITCHING CHARACTERISTICS, Vcc = 5 V. T_A = 25° C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		7	15	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		11	22	ns

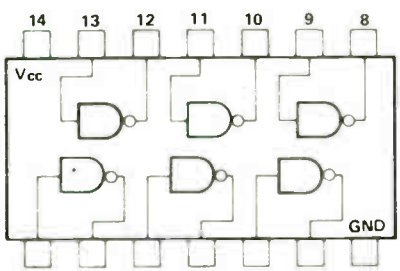
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

† Not more than one output should be shorted at a time.

HEX INVERTER J4-1004

PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, T_A	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400μA	V_{in} = 0.8V,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V			40	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		−18		−55	mA

PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		6	12	mA

SWITCHING CHARACTERISTICS, Vcc = 5 V., T_A = 25° C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		12	22	ns

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

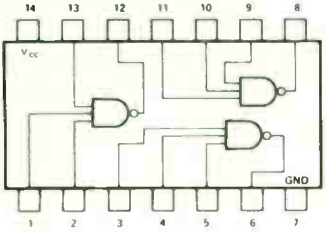
** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

TRIPLE 3-INPUT POSITIVE NAND GATE

J4-1010

PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, T_A	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400μA	V_{in} = 0.8V,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN I_{sink} = 16mA	V_{in} = 2V,		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			40 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = 5.5V		−18		−55	mA

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		9	16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		3	6	mA

SWITCHING CHARACTERISTICS, Vcc = 5 V., T_A = 25° C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		7	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		11	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

BCD-TO-SEVEN SEGMENT DECODER/DRIVER

J4-1047

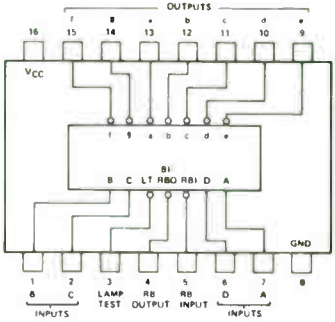
DESCRIPTION

The J4-1047 BCD-to-Seven Segment Decoder/Driver are TTL monolithic devices consisting of the necessary logic to decode a BCD code to seven segment readout plus selected signs.

Incorporated in this device is a blanking circuit allowing leading and trailing zero suppression. Also included is a lamp test control to turn on all segments.

The J4-1047 provides bare collector output transistors for directly driving lamps. The output transistor breakdown of the J4-1047 is 15 volts.

PIN CONFIGURATION



TRUTH TABLE

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	x	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	x	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	x	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	x	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	x	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	x	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	x	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	x	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	x	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	x	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	x	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	x	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	x	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	x	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	x	1	1	1	1	1	1	1	1	1	1	1	1	
BI	x	x	x	x	x	x	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	x	x	x	x	x	1	0	0	0	0	0	0	0	4

NOTES:

1. B1/BRO is wire-OR logic serving as blanking input (B1) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RB1) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.
2. When a ligical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.

3. When ripple-blanking input (RB1) is at a logical 0 and A = B = C = D = logical 0, all segment outputs go to a logical 1 and the ripple-blanking input/ripple-blanking output goes to a logical 0 (response condition).

4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.

SEGMENT IDENTIFICATION

SEGMENT IDENTIFICATION

NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1)		4.75	5	5.25	V
Continuous Voltage at Outputs a through g				15	V
Normalized Fan-Out From Outputs a through g to loads				12	
Normalized Fan-Out From BI/RBO Node to loads				5	
Output Sink Current, I_{sink}	J4-1047 Outputs a through g			20	mA
	J4-1047 BI/RBO Node			8	mA

NOTES:

1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any point	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	V_{CC} = MIN			0.8	V
V_{on}	On-state output voltage at outputs a through g	V_{CC} = MIN, I_{sink} = 40mA		0.27	0.4	V
$V_{out(0)}$	Logical 0 output voltage at BI/RBO node	V_{CC} = MIN, I_{sink} = 8mA		0.3	0.4	V
V_{off}	Off-state output voltage at outputs a through g	V_{CC} = MAX, I_{off} = 250 A	15			V
$V_{out(1)}$	Logical 1 output voltage at BI/RBO node	V_{CC} = MIN, I_{load} = 200 A	2.4	3.7		V
$I_{in(0)}$	Logical 0 level input current at any input except BI/RBO node	V_{CC} = MAX, V_{in} = 0.4V			-1.6	mA
$I_{In(0)}$	Logical 0 level input current at BI/RBO node	V_{CC} = MAX, V_{In} = 0.4V			-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except BI/RBO node	V_{CC} = MAX, V_{in} = 2.4V V_{CC} = MAX, V_{in} = 5.5V			40 1	μA mA
I_{OS}	Short-circuit output current at BI/RBO node	V_{CC} = MAX			-4	mA
I_{CC}	Supply current	V_{CC} = MAX		53	90	mA

SWITCHING CHARACTERISTICS, Vcc = 5 V., $T_A = 25^{\circ}$ C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	C_L = 15pF, R_L = 280 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	C_L = 15pF, R_L = 280 Ω			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	C_L = 15pF, R_L = 280 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	C_L = 15pF, R_L = 280 Ω			100	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

QUADRUPLE BISTABLE LATCH J4-1075

DESCRIPTION

The J4-1075 is a monolithic, quadruple, bistable latch with complementary Q and $\overline{Q}$ outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

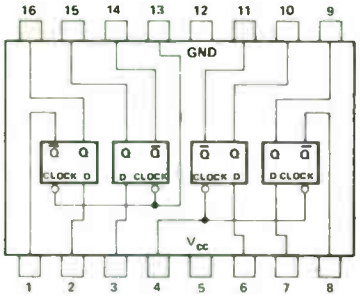
TRUTH TABLE

LOGIC

(Each Latch)		
t_n	t_{n+1}	
D	Q	$\overline{Q}$
1	1	0
0	0	1

NOTES:

1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse
3. These voltages are with respect to network ground terminal.



PIN CONFIGURATIONS

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3)	4.75	5	5.25	V
Normalized Fan-Out from Outputs			10	
Operating Free-Air Temperature Range, T_A	0	25	70	C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.4	V

ELECTRICAL CHARACTERISTICS (Cont'd.)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current at D	V_{CC} = MAX.	V_{in} = 0.4V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX.				-6.4	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX. V_{CC} = MAX.	V_{in} = 2.4V V_{in} = 5.5V			80 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX V_{CC} = MAX	V_{in} = 2.4V V_{in} = 5.5V			160 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX. V_{out} = 0		-18		-75	mA
I_{CC}	Supply current	V_{CC} = MAX.			32	53	mA

SWITCHING CHARACTERISTICS, Vcc = 5 V., $T_A = 25^{\circ}$ C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	6¶		ns
$t_{pd1(D\text{-}Q)}$	Propagation delay time to logical 1 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(D\text{-}Q)}$	Propagation delay time to logical 0 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		14	25	ns
$t_{pd1(D\text{-}\bar{Q})}$	Propagation delay time to logical 1 level from D input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		24	40	ns
$t_{pd0(D\text{-}\bar{Q})}$	Propagation delay time to logical 0 level from D input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		7	15	ns
$t_{pd1(C\text{-}Q)}$	Propagation delay time to logical 1 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C\text{-}Q)}$	Propagation delay time to logical 0 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		7	15	ns
$t_{pd1(C\text{-}\bar{Q})}$	Propagation delay time to logical 1 level from clock input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C\text{-}\bar{Q})}$	Propagation delay time to logical 0 level from clock input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		7	15	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at Vcc = 5 V., $T_A = 25^{\circ}$ C.

† Not more than one output should be shorted at a time.

¶ These typical times indicate that period occurirng prior to the fall of clock pulse (t_0) below 1.5 V. when data at the D input will still be recognized and stored.

DUAL J-K MASTER-SLAVE FLIP-FLOP WITH PRESET AND CLEAR

J4-1076

DESCRIPTION

The J4-1076 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information form master to slave.

TRUTH TABLE

LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES:

1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

CLOCK WAVEFORM

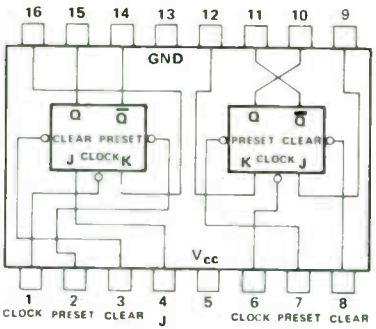
POSITIVE LOGIC

Low input to preset sets Q to logical 1

Low input to clear sets Q to logical 0

Clear and preset are independent from clock

PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	0	25	70	°C
Normalized Fanout from each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$	20			ns
Width of Preset Pulse, $t_{p(preset)}$	25			ns
Width of Clear Pulse, $t_{p(clear)}$	25			ns
Input Setup Time, t_{setup}	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA	2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{CC} = MAX,	V_{in} = 0.4V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear, preset, or clock	V_{CC} = MAX,	V_{in} = 0.4V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V			40	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear, preset, or clock	V_{CC} = MAX,	V_{in} = 2.4V			80	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	−18		−57	mA
I_{CC}	Supply current (each flip-flop)	V_{CC} = MAX,	V_{in} = 5V		20	40	mA

SWITCHING CHARACTERISTICS, Vcc = 5 V., T_A = 25° C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at Vcc = 5 V., T_A = 25° C.

† Not more than one output should be shorted at a time.

DECADE COUNTER J4-1090

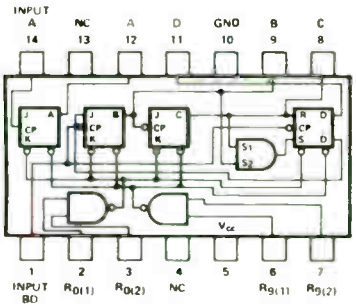
DESCRIPTION

The J4-1090 is a high-speed, monolithic decade counter consisting of four dual-rank, master-slave flip-flops internally inter-connected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical "0" or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be extrnally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a coventional "0" reset, inputs are provided to reset a BCD 9 count for nine's complement decimal applications.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.
3. For operation as a divide-by-two counter and divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

The J4-1090 is completely compatible with the Series 74 logic familes. Average power dissipation is 160mW.

PIN CONFIGURATIONS



LOGIC TRUTH TABLES

BCD COUNT SEQUENCE (See Note 1)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS $R_{0(2)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

NOTES

1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 of a logical 0 may be present.
3. Fanout from output A to input BD and to 10 additional Series 54/74 loads is permitted

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns
Operating Free-Air Temperature Range, T_A	0	25	70	°C

SWITCHING CHARACTERISTICS, Vcc = 5 V., $T_A = 25^{\circ}$ C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output C	C_L = 15pF,	R_L = 400Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output C	C_L = 15pF,	R_L = 400Ω		60	100	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at input A	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			80 1	μA mA
$I_{in(1)}$	Logical 1 level input current at input BD	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			160 1	μA mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	V_{CC} = MAX,	V_{in} = 0.4V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	V_{CC} = MAX,	V_{in} = 0.4V			−3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BD	V_{CC} = MAX,	V_{in} = 0.4V			−6.4	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,	V_{out} = 0V	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V		32	53	mA

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at Vcc = 5 V., $T_A = 25^{\circ}$ C.

† Not more than one output should be shorted at a time.

DIVIDE-BY-TWELVE COUNTER (DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

J4-1092

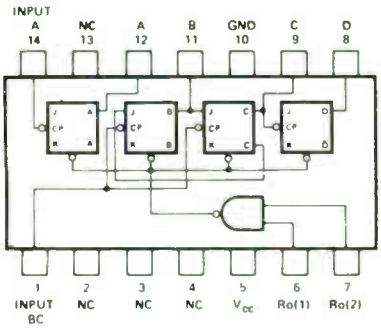
DESCRIPTION

The J4-1092 is a high-speed monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally inter-connected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flops outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous division of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table.
2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency division of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

The J4-1092 is completely compatible with the Series 74 logic families. Average power dissipation is 155mW.

PIN CONFIGURATIONS



TRUTH TABLE (See Notes 1 and 2)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1

COUNT	OUTPUT			
	D	C	B	A
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

NOTES:
1. Output A connected to input B.
2. To reset all outputs to logical 0, both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A	0	25	70	°C
Normalized Fan-Out from each Output, N			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX,	V_{in} = 2.4V			40	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at input A	V_{CC} = MAX,	V_{in} = 2.4V			80	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at input 8C	V_{CC} = MAX,	V_{in} = 2.4V			160	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX,	V_{in} = 0.4V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current input A	V_{CC} = MAX,	V_{in} = 0.4V			−3.2	mA
$I_{in(0)}$	Logical 0 level input current at input 8C	V_{CC} = MAX,	V_{in} = 0.4V			−6.4	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,	V_{out} = 0	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V		31	51	mA

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at Vcc = 5 V., $T_A = 25^{\circ}$ C.

† Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, Vcc = 5 V., $T_A = 25^{\circ}$ C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		60	100	ns

MONOSTABLE MULTIVIBRATOR

DESCRIPTION

This monolithic TTL monostable multivibrator features d-c triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to Vcc noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 nanoseconds to 40 seconds by choosing appropriate timing components. With no external timing components (i.e., pin 9 connected to pin 14 , pins 10 , 11 open) an output pulse of typically 30 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

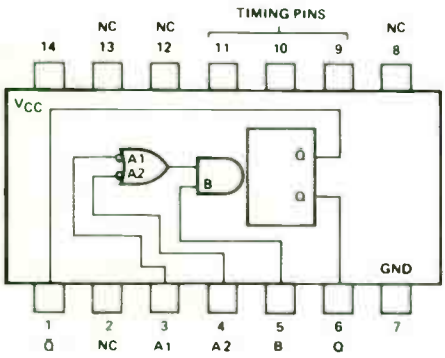
Pulse width is achieved through internal compensation and is virtually independent of Vcc and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and Vcc range for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 40kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 milliwatts at 5 volts (50% duty cycle) and a quiescent dissipation of typically 65 milliwatts.

Duty cycles as high as 90% are achieved when using R_T - 40kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

PIN CONFIGURATIONS



TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

1 = $V_{in(1)} \geq 2V$ 0 = $V_{in(0)} \leq 0.8V$

1. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
2. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
3. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of 30ns is obtained typically.
4. To use the internal timing resistor (2kΩ nominal), connect pin (9) to pin (14).
5. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.
6. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.
7. t_n = time before input transition.
8. t_{n+1} = time after input transition.
9. x indicates that either a logical 0 or 1, may be present.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:				V
	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Input Pulse Rise/Fall Time: Schmitt Input (B)			1	V/s
Logic Inputs (A1, A2)			1	V/μs
Input Pulse Width	50			ns
External Timing Resistance Between Pins (11) and (14) (Pin (9) open)	1.4			kΩ
External Timing Resistance:			30	kΩ
			40	kΩ
Timing Capacitance	0		1000	μF
Output Pulse Width			40	s
Duty Cycle: R_T = 2kΩ			67%	
			90%	
R_T = 40kΩ				

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA		0.22	0.4	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA	2.4	3.3		V
$I_{in(0)}$	Logical 0 level input current at A_1 of A_2	V_{CC} = MAX,	V_{in} = 0.4V		-1	-1.6	mA
$I_{in(0)}$	Logical 0 level input current at B	V_{CC} = MAX,	V_{in} = 0.4V		-2	-3.2	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

I_{in} (1)	Logical 1 level input current at A_1 of A_2	V_{CC} = MAX,	V_{in} = 2.4V		2	40	μA
		V_{CC} = MAX,	V_{in} = 2.4V		0.05	1	mA
I_{in} (1)	Logical 1 level input current at B	V_{CC} = MAX,	V_{in} = 2.4V		4	80	μA
		V_{CC} = MAX,	V_{in} = 5.5V		0.05	1	mA
I_{OS}	Short circuit output current at O or $\overline{O}$†	V_{CC} = MAX		-18	-25	-55	mA
I_{CC}	Power supply current in quiescent (unfired) state	V_{CC} = MAX			13	25	mA
I_{CC}	Power supply current in fired state	V_{CC} = MAX			23	40	mA

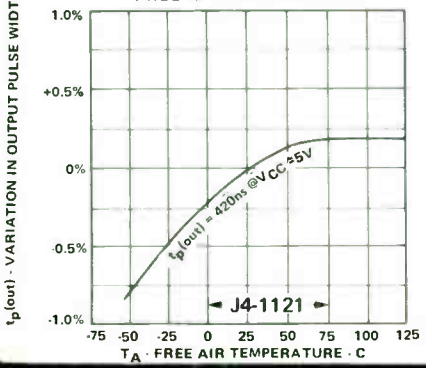
SWITCHING CHARACTERISTICS, Vcc = 5 V., $T_A = 25^o$ C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from B input to O output	C_L = 15pF,	C_T = 80pF	15	35	55	ns
t_{pd1}	Propagation delay time to logical 1 level from A1/A2 inputs to O output	C_L = 15pF,	C_T = 80pF	25	45	70	ns
t_{pd0}	Propagation delay time to logical 0 level from B input to $\overline{O}$ output	C_L = 15pF,	C_T = 80pF	20	40	65	ns
t_{pd0}	Propagation delay time to logical 0 level from A1/A2 inputs to $\overline{O}$ output	C_L = 15pF,	C_T = 80pF	30	50	80	ns
$t_{p(out)}$	Pulse width obtained using internal timing resistor	C_L = 15pF, R_T = Open,	C_T = 80pF Pin (9) to V_{CC}	70	110	150	ns
$t_{p(out)}$	Pulse width obtained with zero timing capacitance	C_L = 15pF, R_T = Open,	C_T = 0. Pin (9) to V_{CC}	20	30	50	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	C_L = 15pF, R_T = 10kΩ	C_T = 100pF, Pin (9) Open	600	700	800	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	C_L = 15pF, R_T = 10kΩ	C_T = 1μF, Pin (9) Open	6	7	8	ms
t_{hold}	Minimum duration of trigger pulse	C_L = 15pF, R_T = Open,	C_T = 80pF, Pin (9) to V_{CC}		30	50	ns

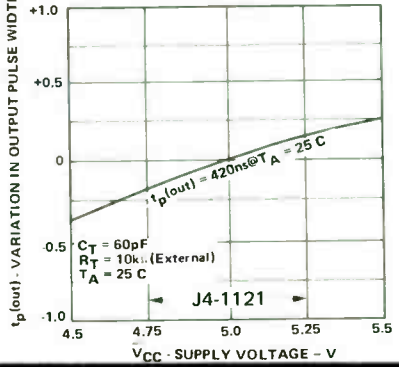
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

TYPICAL CHARACTERISTICS

VARIATION IN OUTPUT PULSE WIDTH VERSUS FREE-AIR TEMPERATURE

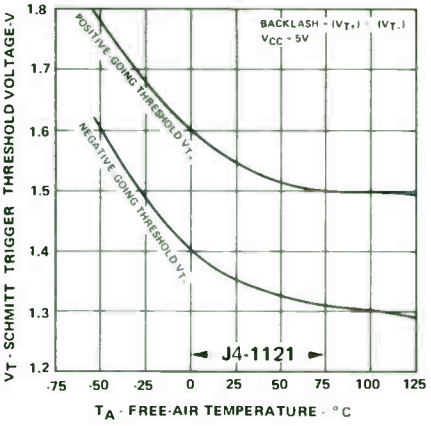


VARIATION IN OUTPUT PULSE WIOTH VERSUS SUPPLY VOLTAGE

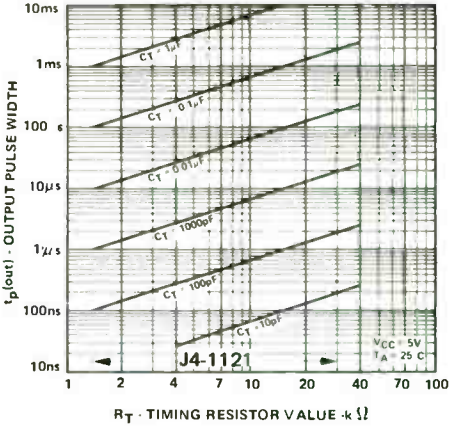


TYPICAL CHARACTERISTICS

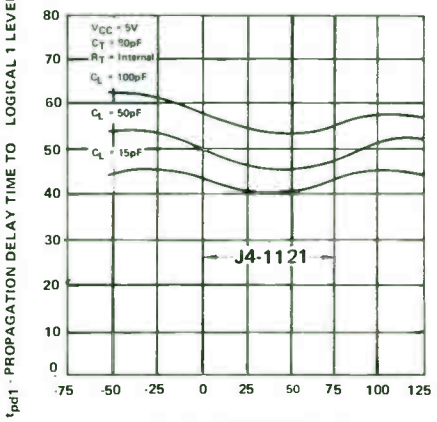
SCHMITT TRIGGER THRESHOLD VOLTAGE VERSUS FREE-AIR TEMPERATURE



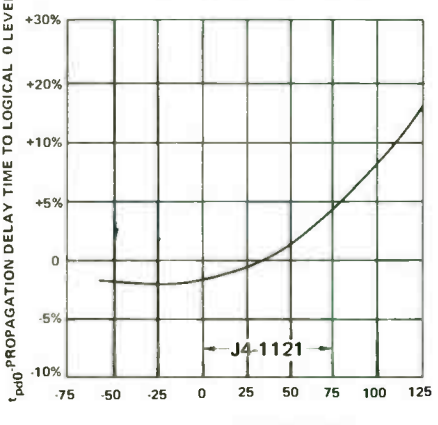
OUTPUT PULSE WIDTH VERSUS TIMING RESISTOR VALUE



PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL (B INPUT TO Q OUTPUT) FREE-AIR TEMPERATURE

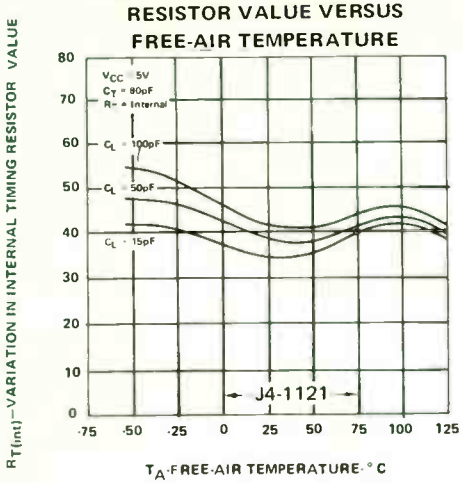


PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL (B INPUT TO Q OUTPUT) FREE-AIR TEMPERATURE



VARIATION IN INTERNAL TIMING RESISTOR VALUE VERSUS FREE-AIR TEMPERATURE

J4-1121



TIMER J4-1555

DESCRIPTION

The J4-1555 monolithic timing circuit is a highly stable controller capable of producing accurate time delay, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

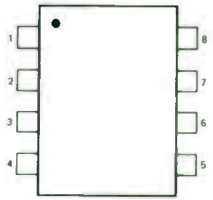
FEATURES

- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.005% PER °C
- NORMALLY ON AND NORMALLY OFF OUTPUT

APPLICATIONS

PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME DELAY GENERATION
PULSE WIDTH MODULATION
PULSE POSITION MODULATION
MISSING PULSE DETECTOR

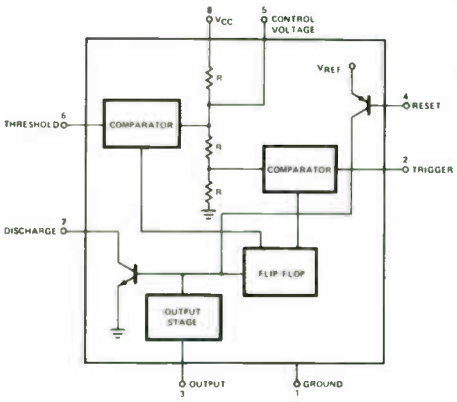
PIN CONFIGURATIONS



V PACKAGE
(Top View)

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
Power Dissipation	600 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

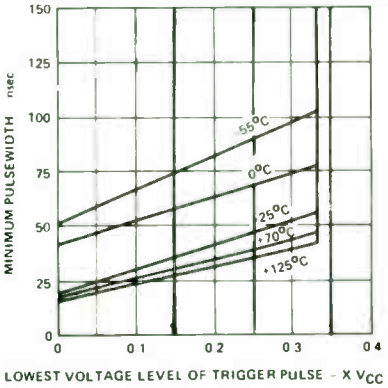
ELECTRICAL CHARACTERISTICS (T_A = 25° C, Vcc = +5 V. to + 15 unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE 555			NE 555			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V R_L = ∞		10	12		10	15	mA
	Low State, Note 1							
Timing Error	R_A, R_B = 1KΩ to 100KΩ							
Initial Accuracy	C = 0.1 μF Note 2		0.5	2		1		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.005	0.02		0.01		%/Volt
Threshold Voltage			2/3			2/3		X V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	.25		0.1	.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	.75	V
	I_{SINK} = 100mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25				V
	I_{SINK} = 5mA					.25	.35	
Output Voltage Drop (high)								
	I_{SOURCE} = 200mA		12.5			12.5		
	V_{CC} = 15V							
	I_{SOURCE} = 100mA							
	V_{CC} = 15V	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		nsec

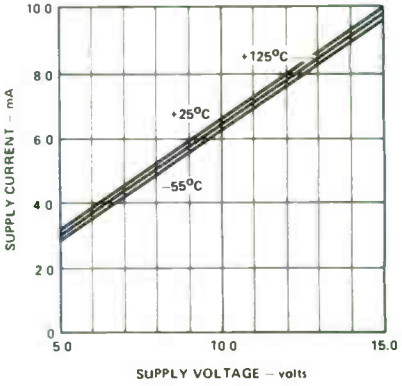
NOTES:

1. Supply Current when output high typically 1mA less.
2. Tested at Vcc = 5 V. and Vcc = 15 V.
3. This will determine the maximum value of R_A + R_B For 15 V. operation, the max total R = 20 megohm.

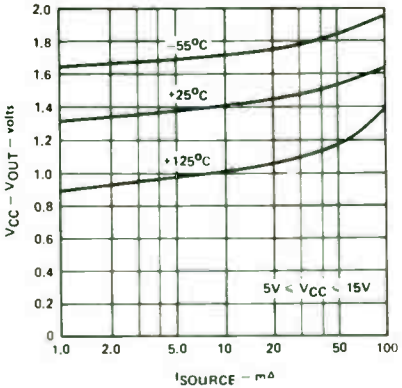
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



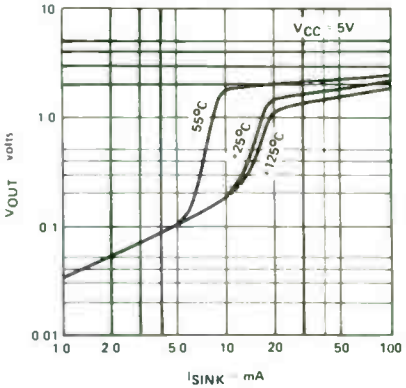
SUPPLY CURRENT vs SUPPLY VOLTAGE



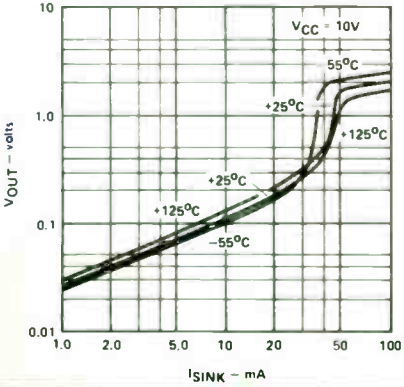
HIGH OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT



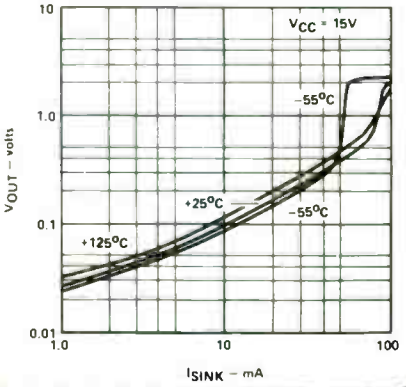
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



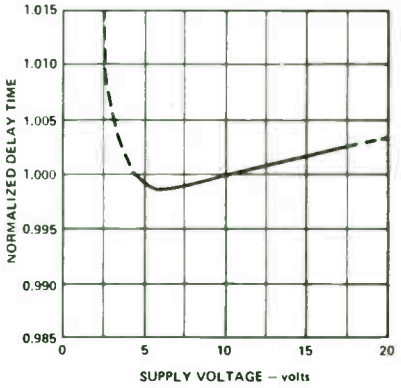
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



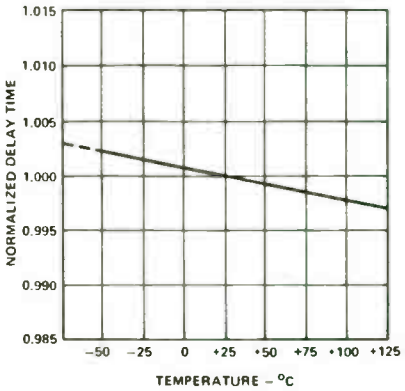
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



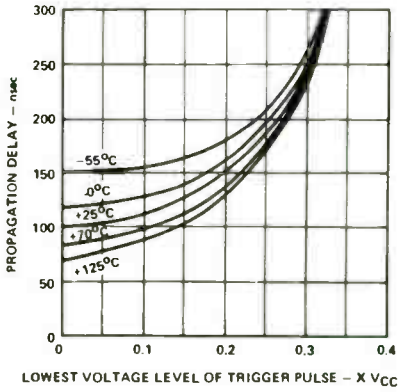
DELAY TIME vs SUPPLY VOLTAGE



DELAY TIME vs TEMPERATURE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



APPLICATIONS INFORMATION

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Referring to figure 1a the external capacitor is initially held discharged by a transistor inside the timer.

Upon application of a negative trigger pulse to pin 2, the flip-flop is set which releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor, now, increases exponentially with the time constant = $R_A C$. When the voltage across the capacitor equals 2/3 Vcc, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state. Figure 1b shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative going input signal when the level reaches 1/3 Vcc. Once triggered, the circuit will remain in this state until the set time is elapsed, even if it is triggered again during this interval. The time that the output is in the high state is given by $t = 1.1\ R_A C$ and can easily be determined by Figure 1c. Notice that since the charge rate, and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over again.

The timing cycle will now commence on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its low state.

When the reset function is not in use, it is recommended that it be connected to Vcc to avoid any possibility of false triggering.

J4-1555

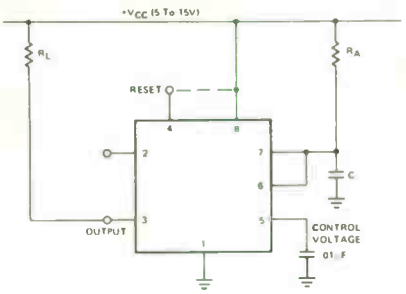
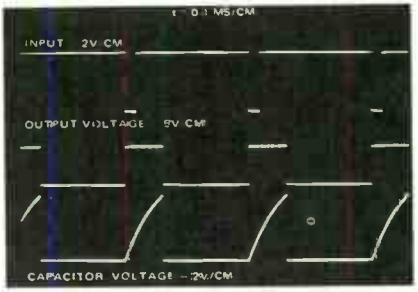


FIG. 1a.



R_A = 9.1 KΩ, C = .01 µF, R_L = 1 KΩ

FIG. 1b.

ASTABLE OPERATION

If the circuit is connected as shown in Figure 2a (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

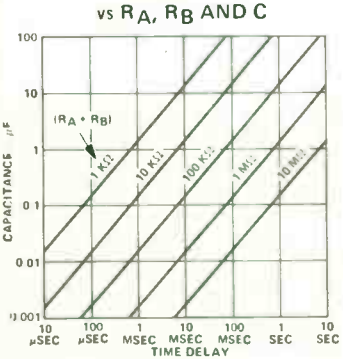


FIG. 1c.

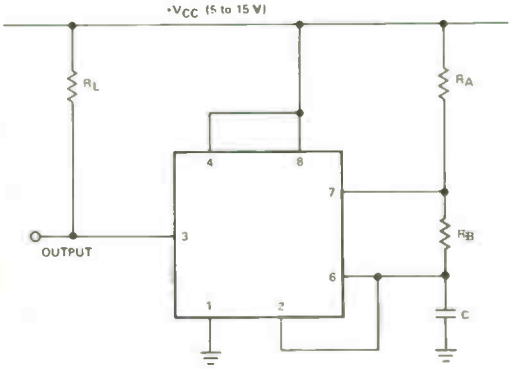
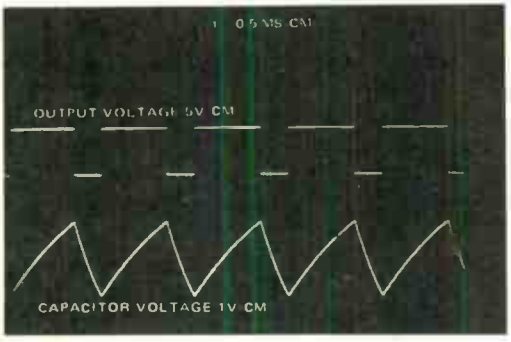


FIG. 2a.



R_A = 4 KΩ, R_B = 3 KΩ, R_L = 1 KΩ

FIG. 2b.

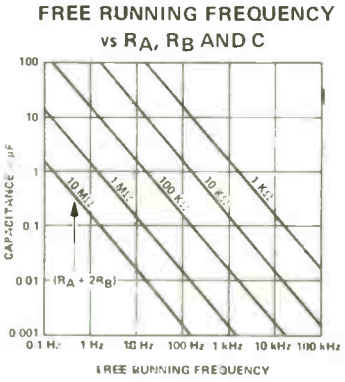


FIG. 2c.

In this mode of operation, the capacitor charges and discharges between 1/3 Vcc and 2/3 Vcc. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage. Figure 2b shows actual waveforms generated in this mode of operation.

The charge time (output high) is given by:

$$t_1 = 0.693 (R_A + R_B) C$$

and the discharge time (output low) by:

$$t_2 = 0.693 (R_B) C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.693 (R_A + R_B) C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$$

and may be easily found by Figure 2c.

The duty cycle is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

MISSING PULSE DETECTOR

Using the circuit of Figure 3a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 3b shows the actual waveforms seen in this mode of operation.

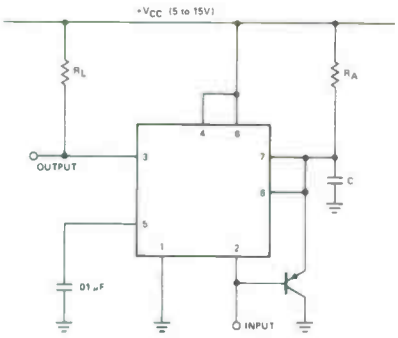
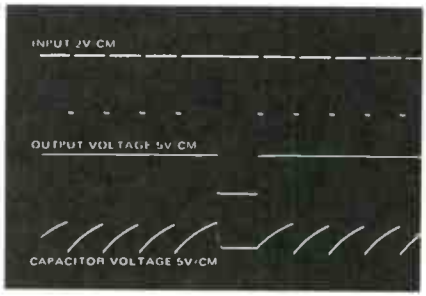


FIG. 3a.



R_A = 1KΩ, C = .09 μF

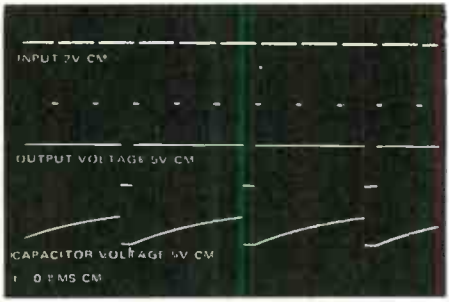
FIG. 3b.

FREQUENCY DIVIDER

If the input frequency is known, the timer can easily be used as a frequency divider by adjusting the length of the timing cycle. Figure 4 shows the waveforms of the timer in Figure 1a when used as a divide by three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.

PULSE WIDTH MODULATION (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 5a. The circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (pin 5). This has the effect of modualting the pulse width as the control voltage varies. Figure 5b shows the actual waveforms generated with this circuit.



R_A = 1250Ω, C = .02 μF, R_L = 1KΩ

FIG. 4

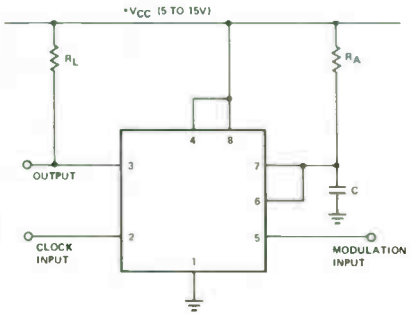
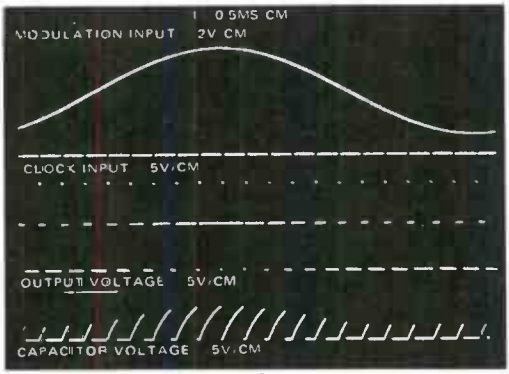


FIG. 5a.

PULSE POSITION MODULATION (PPM)

This application uses the timer connected for astable (free-running) operation, Figure 6a, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 6b shows the waveforms generated for triangle wave modulation signal.

FIG. 5b.



R_A = 10KΩ, C = .02 μF

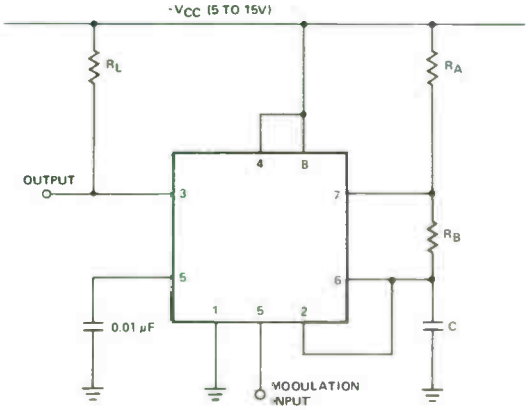


FIG. 6a.

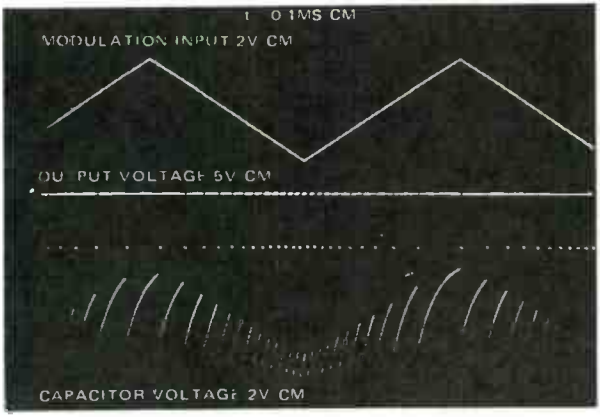


FIG. 6b.

R_A 3KΩ, R_B 500Ω, C = .01 μF, R_L = 1KΩ

TEST SEQUENCER

Figure 7 shows several timers connected sequentially. The first timer is started by momentarily connecting pin 2 to ground, and runs for 10 msec. At the end of its timing cycle, it triggers the second circuit which runs for 50 msec. After this time, the third circuit is triggered. Note that the timing resistors and capacitors can be programmed digitally and that each circuit could easily trigger several other timers to start concurrent sequences.

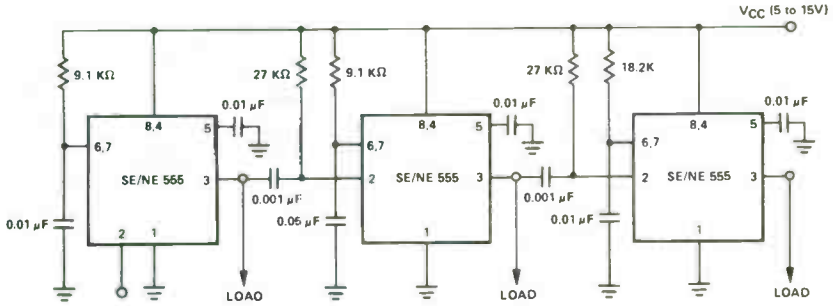
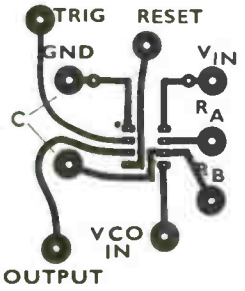


FIG. 7



SOLID STATE NUMERIC DISPLAY

USING GALLIUM PHOSPHIDE RED-LIGHT-EMITTING DIODES

Features:

- Large character size
- High brightness with high contrast
- Operates with standard ICs at IC power supply levels
- Low power
- Long-life—solid state reliability
- Mechanically rugged
- Single-plane character—wide-angle viewing
- No RFI problem
- Fast switching

Solid State Displays use the high efficiency electroluminescence from gallium phosphide diodes. The display shown in actual size is a 0.33 inch character, readable at a distance of 15 feet. The numeric indicator displays numerals or signs against a black background that is an integral part of the package; all internal interconnect patterns are hidden and a high contrast ratio exists between lighted segments and the black background. The segments are tightly spaced to give the character a pleasant continuous appearance and they have sufficient width to provide ease of reading which avoids the eye fatigue caused by narrow segments or segments comprised of small dots. The displays may be soldered directly into PC boards or inserted into sockets with 0.100 inch pin spacings (note 3). Standard decoder/drivers (note 2) may be used to directly drive the seven-segments with the addition of series current limiting resistors. The displays are operable over a broad range of current with varying light output—see curves of light output vs. current.

Type J4-900: The J4-900 is a seven-segment numeric display with a 0.33 inch character height. A decimal point to the left of the numeral is included. J4-900 displays insert into standard 14 pin dual-in-line sockets and may be mounted on horizontal centers as close as 0.4 inch.

Absolute Maximum Ratings

Power dissipation at 25°C . . . . . 750 mW
Power derating above 25°C . . . . . 10 mW/°C
Reverse voltage . . . . . 5.5 volts
Continuous forward current per cathode . . . . . 40 mA
Storage and Operating Temperature . . . . . −55°C to 100°C
Soldering Temperature 1/16 in. from case for 5 seconds . . . . . 260°C

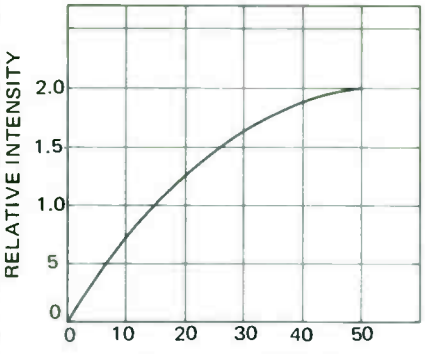
Optical Characteristics per cathode @ I_F = 15mA (25° C)

Symbol	Parameters	Min.	Typ.	Units
I	Luminous Intensity (Note 1)	0.35	1.0	mcd (millicandelas)
λ_p	Peak emission wavelength		690	nm
$\Delta\lambda$	Spectral half line width		85	nm
t - and t_f	Rise and fall time		450	nsec

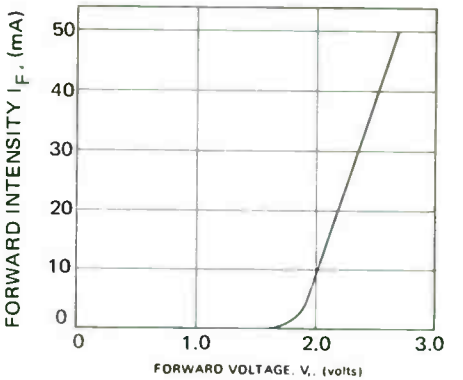
Electrical Characteristics per cathode (25° C)

Symbol	Parameters	Min.	Typ.	Max.	Units
V_F	Forward Voltage @ 15mA	1.8	2.1	2.8	volts
1_R	Reverse Current @ 5.5 volts			50	μA
C_o	Capacitance @ 0 volts, 1 MHz		100		pf

TYPICAL ELECTRO-OPTICAL CHARACTERISTIC CURVES



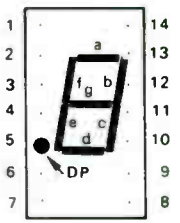
RELATIVE LUMINOUS INTENSITY VS. FORWARD CURRENT



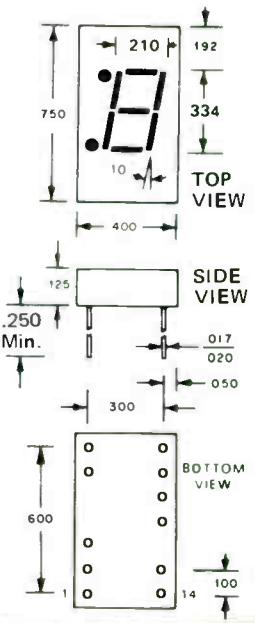
FORWARD CURRENT VS. FORWARD VOLTAGE

PIN CONNECTIONS
TOP VIEW

PIN NO.	
1	Cathode a
2	Cathode f
3	NC
4	NC
5	NC
6	Cathode DP
7	Cathode e
8	Cathode d
9	NC
10	Cathode c
11	CAthode g
12	NC
13	Cathode b
14	Common Anode



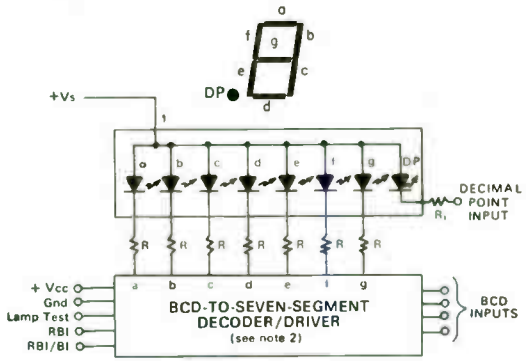
PACKAGE PHYSICAL DIMENSIONS



STANDARD 14 PIN DIP SPACING

All Dimensions In Inches

APPLICATION DIAGRAM WITH STANDARD BCD TO SEVEN-SEGMENT DECODER



The value of R may be adiusted to accommodate a wide range of V's and operating currents.

RB1 – Ripple Blanking Input
RB0/B1 – Ripple Blanking Output/Blanking Input

TYPICAL DISPLAY – DRIVER/DECODER TRUTH TABLE (see Note 2)

BCD INPUT A B C D	DISPLAY INPUT OR DECODER OUTPUT* a b c d e f g	DISPLAY FONT
0 0 0 0	0 0 0 0 0 0 1	0
1 0 0 0	1 0 0 1 1 1 1	1
0 1 0 0	0 0 1 0 0 1 0	2
1 1 0 0	0 0 0 0 1 1 0	3
0 0 1 0	1 0 0 1 1 0 0	4
1 0 1 0	0 1 0 0 1 0 0	5
0 1 1 0	1 1 0 0 0 0 0	6
1 1 1 0	0 0 0 1 1 1 1	7
0 0 0 1	0 0 0 0 0 0 0	8
1 0 0 1	0 0 0 1 1 0 0	9

*0 represents the low decoder output state when current flows in the LED segment

Note 2:
Standard BCD-to-Seven-Segment decoder/drivers are available from several manufacturers. The display font as determined by the decoders differs slightly in the case of each manufacturer; the above truth table shows a typical font. See manufacturers' data sheets for RBI, RBO/BI and Lamp Test input logic conditions.

Note 3:
Filters—Numeric Displays have high contrast ratio without the use of filters. If contrast enhancement is desired, red filters such as Plexiglass 2423 match the light output characteristics. Red circular polarizing plastics such as Polaroid HRCP7 may also be used to enhance contrast and block out wiring patterns on printed-circuit boards when these patterns are visible to the viewer.

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